RADIO FREQUENCY INTEGRATED CIRCUITS FOR WIRELESS AND

WIRELINE COMMUNICATIONS

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RADIO FREQUENCY INTEGRATED CIRCUITS FOR WIRELESS AND WIRELINE COMMUNICATIONS

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A Dissertation

Submitted to

the Graduate Faculty of

Auburn University

in Partial Fulfillment of the

Requirements for the

Degree of

Doctor of Philosophy

Auburn, Alabama
December 17, 2007

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Vasanth Kakani

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DISSERTATION ABSTRACT

RADIO FREQUENCY INTEGRATED CIRCUITS FOR WIRELESS AND WIRELINE COMMUNICATIONS

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Doctor of Philosophy, December 17, 2007
(M.S., University of Texas at Arlington, 2002)
(B.E., Osmania University, 1998)

146 Typed Pages

Directed by Fa Foster Dai

This dissertation presents my studies in design of high frequency circuits for wireless and wireline communication systems.

As a part of this effort a seven tap transversal filter has been designed using broadband amplifiers. The use of active devices instead of passive inductors to implement delay stages greatly reduces the required die area and also makes the filter more adaptive in nature. The designed chip is capable of adapting zeros at various frequencies up to 3.5 GHz, implementing various filter characteristics.

A detailed study of delay through Current Mode Logic (CML) gate operating at the GHz range has been done and optimal and novel biasing strategies have been

investigated to achieve higher operational speeds. “Keep alive” biasing technique has been proposed to reduce delay in CML latches. The optimal biasing strategy for CML circuits is obtained considering the circuit speed and power consumption.

Design challenges in the design of high frequency single phase and multiphase oscillators have been investigated followed by prototype designs. A novel Quadrature VCO (QVCO) is implemented in a 47 GHz SiGe technology. The QVCO is a serially coupled LC VCO that utilizes Silicon Germanium (SiGe) Hetero-junction Bipolar Transistors (HBT) for oscillation and Metal Oxide Semiconductor Field Effect Transistors (MOSFET) for coupling, resulting in 14% wide tuning range. Design of high frequency 25 GHz oscillator is also presented. The 25 GHz oscillator achieves phase noise of -82 dBc/Hz @ 500 KHz offset.

Design of a 1.2 V, 3.7 mW 8-bit LC tuned Digitally Controlled Oscillator (DCO) implemented in a 120 nm BiCMOS technology is presented. The varactor bank in the oscillator consists of eight binary weighted capacitors controlled by rail-to-rail CMOS logic values. The DCO oscillation frequency can be tuned from 4.2-4.7 GHz with 11.2% tuning range and an average frequency resolution of 2 MHz/bit. The DCO has phase noise of -103 dBc/Hz @ 500 KHz offset and exhibits -177 dBc/Hz figure of merit.

Design of 1.5 V second order phase locked loop is presented. The loop exhibits an in-band phase noise of -70 dBc/Hz @ 10 KHz offset and out-band phase noise of -110 dBc/Hz @ 3 MHz offset frequency from a 5 GHz carrier frequency.

ACKNOWLEDGEMENTS

I would like to express my appreciation for professor Foster Dai for his guidance and encouragement during my graduate study at Auburn.

I would like to thank professor's Richard. C. Jaeger, Guofu Niu and Charles. E. Stroud for their advice. I also thank professor Sushil Bhavnani for his comments and being an external reader for this dissertation.

Many thanks to my team members, Dayu Yang, Xuefeng Yu, Yuan Yao, Wenting Deng and Xueyang Geng for their help and assistance during my course of study.

Finally I would like to thank my parents for their encouragement and support through out this work.

Style manual: Guide to Preparation and Submission of Thesis and Dissertations. **A**uburn University**,** 2005.

Computer software: MS Word 2003, MS Visio 2003.

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Chapter 1: Introduction

This dissertation covers the design of Radio Frequency Integrated Circuits (RFIC) for wireless and wireline communications focusing mainly on programmable filters, phase lock loop circuits, oscillators and current mode logic circuits. Recently there has been an increased interest in the design of programmable RF filters using broadband amplifiers [7, 8, 9, and 10]. Programmable RF filters find numerous applications in communication systems. Inter Symbol Interference (ISI) coupled with noise is a fundamental problem in communication systems and sets the limit for an acceptable Bit Error Rate (BER). In electrical domain this problem can be solved by integrating the programmable filter at the receiver. In wireless domain for multiband wireless transceiver designs, programmable RF notch filters are needed to selectively reject the bands based on various wireless standards. RF notch filters are critical for removing unwanted signals such as images and interferers. Continuous time filters based on g_m-C ladder and switch capacitor filters have been explored previously for high speed applications, inherent problems like offset, charge leakage and mismatch in analog implementations have been tackled using circuit, layout and improved fabrication techniques. As the signal speed advances into gigahertz range these analog techniques are also ineffective calling for RF or microwave solutions. Microwave solutions incorporating delay lines made up of inductors and capacitors are bulky occupying large die size. Moreover, passive delay networks are always narrowband and are not tunable on the fly and consume large area on the die. Instead of using passive

delay stages, we can use active delay stages to overcome the above mentioned drawbacks of using passive delay lines. This dissertation presents design and analysis of programmable transversal filters that use amplifiers for implementing delay stages.

As communication systems use oscillators for frequency translation, the stringent signal to noise ratio requirements of the transceivers depend heavily on the phase noise performance of oscillators. The need for low power is also important as wireless communication devices are battery operated. Many modern transceiver architectures also require multiphase signals. There are various ways to generate quadrature signals: (i) a divide-by-two frequency divider following the oscillator running at the double the required Local Oscillator (LO) frequency. This approach generally shows poor phase noise and quadrature accuracy, as it requires 50% duty cycle Voltage Controlled Oscillator (VCO). (ii) A VCO followed by a passive polyphase RC complex filter. An integrated polyphase network is narrowband with poor quadrature accuracy. It also suffers from process variation on the RC time constants that lead to amplitude imbalance between the quadrature signals. (iii) Two oscillators are forced to run in quadrature using transistor or transformer coupling. This technique provides wideband quadrature accuracy and superior phase noise performance with a tradeoff of increased power, silicon area and reduced tuning range. By coupling two symmetric oscillators with each other, a Quadrature VCO (QVCO) generates wideband quadrature signals at high frequency. There are various ways to couple the two oscillators and inject-lock their oscillation frequency. The most common coupling mechanism is the parallel coupling proposed by Rofougaran et al. [42], where each oscillator consists of a cross-coupled feedback circuit and each oscillator output is connected to another oscillator using

transistors in parallel to the cross-coupled transistors. Oscillators can also be serially coupled by placing the coupling transistors in series with the oscillation transistors [44]. The proposed oscillator in this dissertation is a serially coupled VCO that utilizes Silicon Germanium (SiGe) transistors for oscillation and Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) for coupling, enabling it to have a wide tuning range. Arguably the oscillator and its following divider is the most challenging block of a frequency synthesizer design. The growing trend to move to higher oscillation frequencies to occupy the unlicensed bands has presented new design challenges to both oscillator and its following dividers design. Challenges involved in the design of high speed oscillators are discussed followed by implementation of a 25 GHz oscillator and a 1.5 GHz cryogenic oscillator.

High speed digital circuits have moved into the analog/RF domain and can no longer be treated as simple binary logic gates. Current Mode Logic (CML) has become the preferred logic style for implementing high speed digital gates in mixed signal environments. The maximum speed of CML circuits is limited by the RC open circuit time constants associated with the latches and gates. The time constants associated with each level of CML gates have been derived and their impact on overall delay of the gate has been investigated. Study of energy consumption and delay of current mode logic gate has been done and optimal biasing points for high speed and low power consumption have been identified. A novel biasing strategy for CML topology is proposed to achieve improved performance in terms of speed when the circuit is biased at 10% to 30% of the peak f_T current.

Recently there have been efforts to digitize the Phase Lock Loop (PLL) synthesizer design process [48] i.e. to synthesize the PLL on silicon using a hardware description language. As a part of this effort, designing and modeling Digital Controlled Oscillators (DCO), whose oscillation frequency is determined by a binary code is the main design bottle neck. Issues favoring the design of digitally controlled varactors as an alternative to analog controlled varactors which require continuous tuning are studied. Digitally controlled oscillators use a digital approach to frequency tuning by switching the varactor to one of the two distinct capacitance values that can correspond to "on" and "off" states of binary logic. The DCO topology is that of a differential LC oscillator and the digital frequency tuning is achieved by individually switching an array of capacitances. Design and layout issues involved in the design of 1.2 V, eight bit oscillator and its binary controlled varactor bank in a 0.12 μm Bipolar-CMOS (BiCMOS) technology is presented followed by a prototype design and its measured results.

Eight chips have been fabricated during this course of study, some individually and some as a part of team effort. A list of those chips and their brief descriptions are listed below. More in-depth details of the design and results of these chips are illustrated in the following chapters.

- A 3.5 GHz analog FIR filter in SiGe 5HP process has been designed and fabricated. The filter used the structure of an analog tapped delay line. It was a programmable filter whose transfer function could be tuned to implement different transfer function by varying the tap weights. The filter consisted of variable gain amplifiers, delay amplifiers, high impedance current sources, bandgap circuit and single to differential converters.

- A 3.5 GHz charge pump PLL in 90 nm FD-SOI research process was designed as a part of larger team effort. My responsibility included the design of multiphase oscillator and charge pump. The main challenge was the lack of RF models during design phase. The planned target frequency for the oscillator was 5 GHz. Four stages of single phase oscillator core were coupled to each other in a ring oscillator fashion to provide multiphase outputs.
- A 1.8 GHz oscillator in 45 GHz SiGe technology was designed as a part of larger team project involving circuit designs for extremely low temperature environments. The oscillator was followed by a chain of dividers to provide a 20 MHz clock signal to other blocks on the chip.
- A 20 GHz, 25 dB dynamic range variable gain amplifier in BiCMOS 8HP process was designed as a part of larger team project involving radio design. The variable gain amplifier followed a low noise amplifier. The structure of the variable gain amplifier was a Cherry-Hooper amplifier with source follower feedback.
- A 5 GHz serially coupled quadrature oscillator in 45 GHz SiGe technology was designed and fabricated. The coupling transistors used for generating quadrature signals are placed in series with oscillating transistors resulting in power saving. The oscillator used SiGe transistors for oscillation and MOSFETs for coupling to achieve wide tuning range.
- A 1.5 V, 8-bit, 5 GHz digital controlled oscillator in 0.12 micron BiCMOS technology was designed and fabricated. The capacitance values in the oscillator are binary weighted and can be controlled by binary logic. The output frequency

of the oscillator can be controlled using an eight bit code that is fed to the varactor bank.

- A 25 GHz Oscillator in BiCMOS 8HP technology was designed as a part of larger team project. This high frequency oscillator used microwave strip lines inductors instead of octagonal inductors. The 25 GHz signal was divided down to 13.5 GHz to provide a clock signal to other blocks on the chip.
- A 5 GHz second order charge pump phase lock loop was designed in BiCMOS 8HP technology. The design consisted of an oscillator operating at 5 GHz, an charge pump configured as an exclusive OR gate, fairly standard three state phase frequency detector, and a reference frequency of 39 MHz

1.1 Dissertation Organization

Chapter 2 of this dissertation discusses current equalization techniques in electrical domain. It explores the circuit requirements of the blocks to build a programmable filter and presents the design and implementation of a high speed analog programmable filter. The programmable filter presented is a seven tap transversal equalizer with cascaded Cherry-Hooper amplifiers for delay stages and Gilbert variable gain amplifier as tap weights. Design and implementation of a 3.5 GHz analog programmable filter RFIC is presented in detail followed by measured results.

Chapter 3 explores the design issues related to current mode logic topology used in high speed digital logic design. Detailed study of its delay model and its optimal biasing points are presented. A biasing scheme is proposed to improve the speed of the CML gates when they are biased at low currents.

Chapter 4 gives a brief introduction of the theory involved in the design of voltage controlled oscillators and presents a review of various phase noise models. Design and layout issues of implementing high speed, low phase noise single phase and multiphase oscillators are also discussed, followed by experimental results of two prototypes including a 25 GHz oscillator designed in a 120 GHz SiGe technology and exhibiting a phase noise of -82.5 dBc/Hz @ 500 KHz offset frequency. This is followed by a design of a 1.5 GHz SiGe oscillator that can operate well down till cryogenic temperatures.

In chapter 5 techniques for quadrature signal generation are discussed followed by a design of a novel coupling topology for quadrature signal generation with increased tuning range. Design and implementation of a 5 GHz quadrature oscillator fabricated in a 47 GHz SiGe technology is presented. This oscillator is a serially coupled LC VCO that utilizes SiGe transistors for oscillation and MOSFETs for coupling enabling it to have a wide tuning range of 15% and lower power consumption. This is followed by a design of a 3.5 GHz multiphase oscillator in a FD-SOI research fabrication technology and its measured results.

In chapter 6 low power, low voltage digital controlled oscillators are presented as an alternative to conventional analog oscillators which are useful for the digitizing phase lock loop design. Design and layout issues of implementing the digital varactor and the 1.2 V oscillator with 2 MHz/LSB resolution are discussed. This is followed by its measured results.

Chapter 7 discusses the theory of phase lock loop design and design of its building blocks charge pump, phase frequency detector, 5 GHz oscillator and dividers, followed by its experimental results.

Chapter 2: Integrated Transversal Filter

2.1 Introduction

Programmable Radio Frequency (RF) filters find numerous applications in communication systems. Inter symbol interference coupled with noise is a fundamental problem in communication systems and set the limits for data rate and transmission distance while maintaining an acceptable Bit Error Ratio (BER). Light traveling through a single mode fiber can have two modes of propagation due to cable asymmetry. The component of the signal traveling through the two modes have different velocities and are differentially delayed at the output causing pulse broadening, an effect commonly known as dispersion. In fiber communications, modal, chromatic and polarization mode dispersions are the major sources of transmission impairments. These transmission impairments depend on the length of the channel and determine the placing of repeaters in the communication system. Mechanical or optical solutions like placing dispersion compensated fibers that have negative dispersion compared to common fibers in long-haul systems tend to be bulky, costly with high insertion loss and slow tuning speed, if they are tunable at all.

In electrical domain this problem can be solved by equalization at the receiver. In communication system equalization is a process of correcting the distortions that the channel induces to the signal. The equalizers frequency response multiplied with the frequency response of the dispersive channel yields the actual channel response that was

used in the system design. Electronic transversal filters can be used to compensate fiber dispersions by constructing an inverse transfer function of the dispersive channel [1-4]. Electronic equalizers are much cheaper when mass produced and can also be integrated on the same die with the receiver. Electronic equalizers have also been popularly used in telephone systems and disk drives.

In wireless domain for multiband wireless transceiver designs, programmable RF notch filters are needed to selectively reject the bands based on various wireless standards. RF notch filters are critical for removing unwanted signals such as images and interferers.

This chapter discusses the design of transversal filters that can be employed for equalization techniques to overcome ISI. The design and implementation of a 3.5 GHz analog programmable filter chip is presented in detail. The RF filter is a seven tap transversal equalizer with cascaded Cherry-Hooper amplifiers for delay stages and Gilbert variable gain amplifier as tap weights. The SiGe programmable filter chip consumes 250 mW of power under 3.3 V supply and occupies 2.16 mm^2 of die area.

2.2 Transversal filter design

The filter is essentially a tapped delay line with the feed forward taps forming a Finite Impulse Response (FIR) filter. The filter can be implemented in either digital or analog domain. Digital FIR filters usually employ shift registers to implement the delay cell and require the data to be sampled and digitized requiring an analog to digital converter preceding the filter. This greatly increases the circuit complexity and power consumption at high speeds. On the other hand analog implementations remove the need for power

hungry data converters before equalization resulting in power savings. Continuous time filters based on g_m-C ladder and switch capacitor filters have been explored previously for high speed applications, inherent problems like offset, charge leakage, mismatch in analog implementations have been tackled using circuit, layout and improved fabrication techniques [5, 6]. As the signal speed advances in to gigahertz range these analog techniques are also ineffective calling for RF or microwave solutions. Transversal RF filters using Silicon Germanium (SiGe) technology have been reported previously [7-9] but no detailed information is provided about the circuit implementations. In [10] a fractionally spaced equalizer was designed in a distributed traveling wave fashion using passive transmission lines as delay elements. This design [59,66] is based upon a commonly used SiGe technology with f_T=47 GHz using broadband amplifier for implementing delay blocks and thus has the potential to be integrated in the whole receiver integrated circuit for cost reduction.

The block diagram of a transversal filter is shown in figure 2.1. The input signal $y(t)$ is delayed by each delay element as it propagates through the filter. The delayed version of the signal $y(t-kT)$ (where k =1, 2, 3… are the tap coefficients and T is the period by which the signal is delayed) are tapped along the delay line and summed to generate the filter output. The transfer function of the integrated filter can be adaptively adjusted by changing the tap coefficients (c(0)…c(k)) of its tap weights. Adjusting the tap weights it is possible to adapt zeros to various frequencies and implement different filter characteristics like notch, band pass, low pass and band reject. Changing the tap weights affects only the locations of the zeros, while the poles of the programmable filter are fixed. Hence, the filter is always stable.

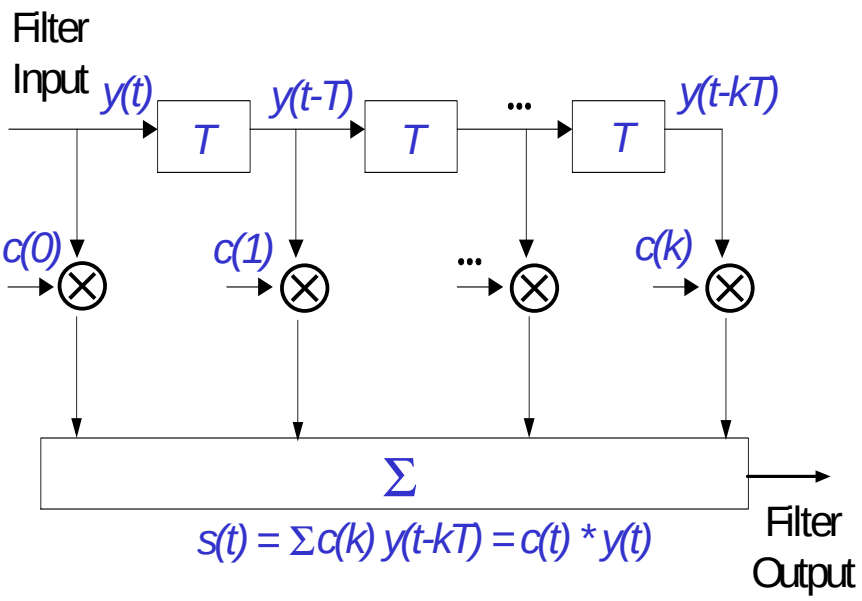

Figure 2.1 Block diagram of the transversal filter. T denotes the delay and ⊗ denotes tap weights.

2.2.1 Delay stage

Passive delay networks have losses associated with them and are bulky. Moreover, passive delay networks are always narrowband and are not tunable on the fly and consume large area on the die. Instead of using passive delay stages, active delay stages can be used to overcome the above mentioned drawbacks of using passive delay lines. Since a seven tap equalizer would require six delay amplifiers connected in series there is a requirement for individual delay amplifiers to have broadband characteristics with high cutoff frequency. As amplifier cells are cascaded, the total bandwidth at the output is reduced according to the following equation

$$BW_{tot} = BW_c \sqrt[m]{2^{\frac{1}{n}}-1} \tag{2.1}$$

where m is equal to two for first-order stages and four for second order stages and n is the number of identical stages having bandwidth BW_c [11]. For a seven tap equalizer with

six delay stages the individual delay stages need to have a bandwidth of at least 10 GHz for an overall bandwidth of 3.5 GHz. It is helpful to apply the principle of impedance mismatching between succeeding stages to improve the bandwidth, an example being a chain of alternating transadmittance stage and transimpedance stages. Series shunt cascaded Cherry-Hooper amplifier was chosen to implement the filter delay stages. As shown in figure 2.2, Cherry-Hooper amplifier [12–14] is a cascade of two feedback amplifiers, where the series feedback stage is a transconductance amplifier and shunt feedback stage is a transimpedance amplifier. Transistor Q1 and resistor R_E forms the serial feed back stage. Transistor Q3 along with R_F forms the shunt feedback stage.

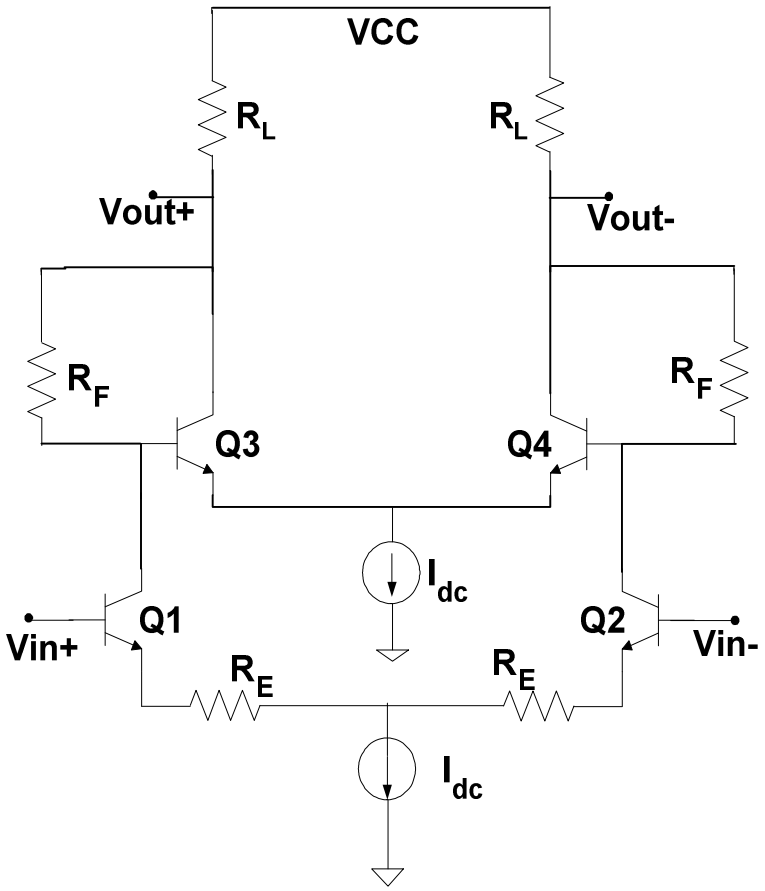

Figure 2.2 Series–shunt broadband amplifier.

The input and output resistance of this serial feedback stage can be calculated as

$$R_{in} = r_b + r_\pi + \beta R_E \tag{2.2}$$

$$R_{out} = r_o(1 + g_m R_E) \tag{2.3}$$

The input and output resistance of this shunt feedback stage can be calculated as

$$R_{in} = \left(\frac{r_b}{\beta} + \frac{1}{g_m}\right)\left(1 + \frac{R_F}{R_L}\right) \tag{2.4}$$

$$R_{out} = \frac{1}{g_m} + \frac{R_F + r_b}{\beta} \tag{2.5}$$

where r_b is the intrinsic base resistance, r_π is the small signal resistance between the base and the emitter and r_o is the output resistance of the transistor.

By cascading these two stages the high resistive input of the series feedback stage is driven from a low resistance voltage output obtained from the shunt feedback stage. Conversely, the low resistive input of the shunt feedback stage is driven from a high resistance current output obtained from the serial feedback stage. Due to this all the signal nodes have low resistance values yielding high frequency poles, which improves the bandwidth of the amplifier, due to the low time constants associated with them. This arrangement is advantageous since the impedance requirement will be automatically satisfied at the input and output of the amplifier while cascading several such delay stages. Emitter followers are used in between the delay stages for level shifting and creating stronger impedance mismatch between succeeding stages to improve the bandwidth. Another advantage of this impedance mismatch between succeeding stages is that it causes all the nodes to have low resistance values and so the influence of parasitic capacitance at those nodes are reduced. The input and output impedances of the amplifier stages are frequency dependent and at high frequencies the impedance mismatching can be degraded. To overcome this, additional elements can be used as shown in figure 2.3 (capacitors C_F & C_E) in the feedback path to improve the bandwidth.

The degeneration and feedback capacitors C_E and C_F introduce zeros in the frequency response and thereby maximize the amplifier bandwidth. Emitter degeneration R_E and C_E at the transconductance pair creates the first zero. The pole caused by R_F

and C_F in the feedback path of the transimpedance pair creates the second zero. These zeros enhance the bandwidth and eliminate the need for inductors.

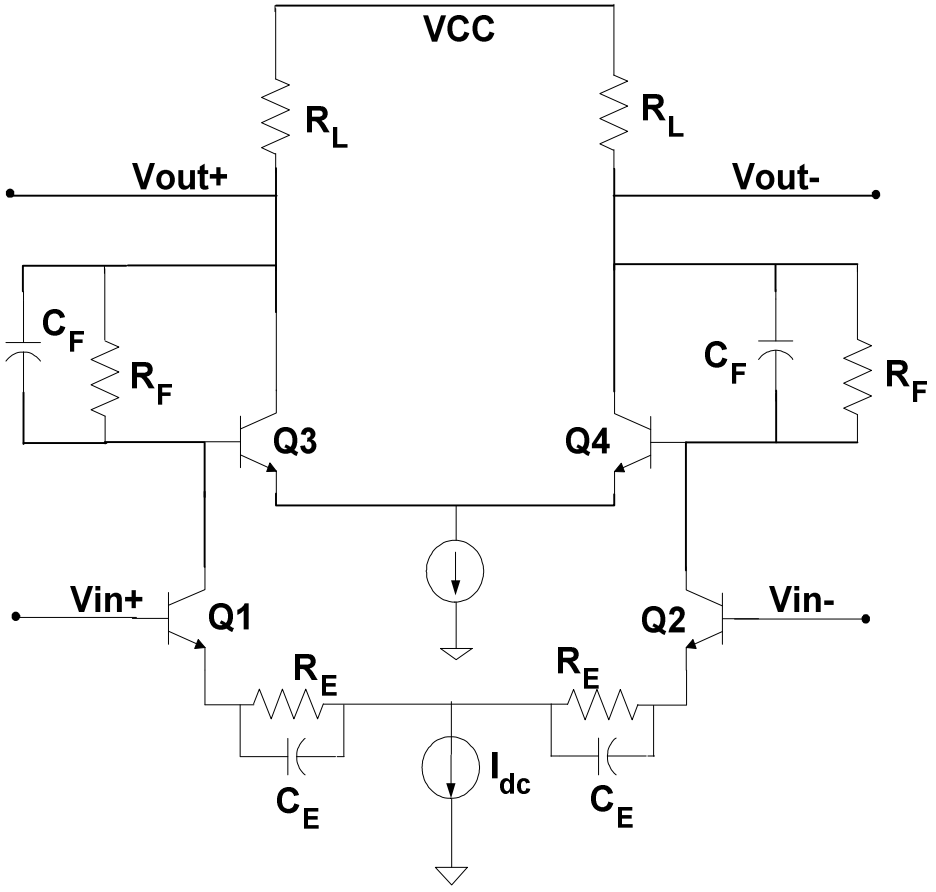

Figure 2.3 Cherry–Hooper amplifier used to implement delay stages.

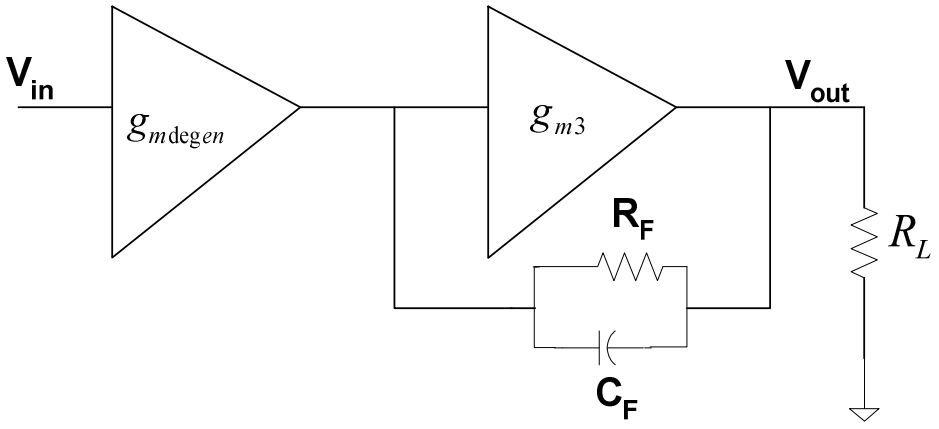

Figure 2.4 Block diagram of the amplifier cell.

Referred to figure 2.4, the transfer function of the Cherry–Hooper amplifier can be approximated as

$$\frac{V_{out}}{V_{in}} = \frac{g_{m1}(1+s\cdot C_E\cdot R_E)(1+s\cdot C_F\cdot R_F+g_{m3}\cdot R_F)}{g_{m3}(1+s\cdot C_F\cdot R_F)(1+s\cdot C_E\cdot R_E+g_{m1}\cdot R_E)} \tag{2.6}$$

where R_E and C_E are the degeneration resistance and capacitance respectively, R_F and C_F are the shunt feedback resistance and capacitance respectively. Figure 2.3 shows the simulated magnitude response of the amplifier. As shown in figure 2.5, the 3-dB cutoff frequency of the amplifier is 10 GHz.

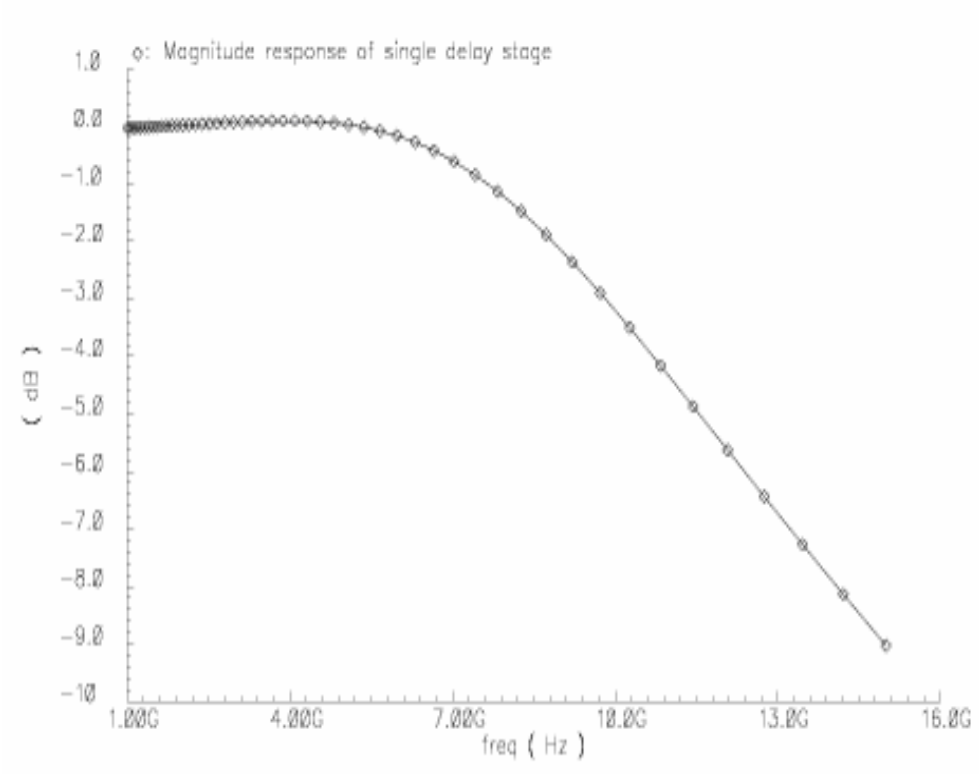

Figure 2.5 Magnitude response of the delay amplifier.

2.2.2 Gain stage

The function of the gain stage is to implement tap weight coefficients to adaptively adjust the transfer function of the transversal filter. The tap weights should be continuously adjustable between 0 and 1 and also be able to provide a phase shift of π to give negative tap coefficients. As shown in figure 2.6, the transversal filter tap with programmable gain is implemented using the Gilbert variable gain amplifier. The use of Gilbert cell to implement positive and negative tap coefficients was first reported in [15]. Transistors Q3, Q4, Q5 and Q6 form the gain control circuit. Signal Vagc is the differential gain control input used to set the tap weights. For large values of Vagc the entire current is steered to one of the top two differential pairs and the gain is either at its most maximum or most minimum value. When the differential Vagc signal is zero then the gain is zero. Tap weights are continuously adjustable between 0 and 1 of the CML logic level (200 mV differential). Thus the variable gain stage is in fact, a variable loss stage. Flipping the polarity of the gain control signal Vagc provides a phase shift of π that is needed for implementing negative tap coefficients. The degeneration resistors at the emitters of transistors Q1 and Q2 are used to provide better linear voltage to current conversion. The differential input signals are buffered with emitter followers biased with constant currents. Buffers and the gain stage satisfy the impedance mismatching condition between succeeding stages i.e. the Cherry-Hooper delay amplifiers, emitter follower buffers and core differential pair of the gain stage.

Figure 2.7 shows the small signal model of the gain control circuit in the Gilbert cell. The Gilbert cell is a current amplifier with the current gain transfer function given by equation 2.7.

$$I(s) = \{g_{m3}(1 + sc_{\pi 4}r_b) - g_{m4}(1 + sc_{\pi 3}r_b)\} \cdot$$
$$\left\{\left(g_{m3} + sc_{\pi 3} + \frac{1}{r_{\pi 3}}\right)(1 + sc_{\pi 4}r_b) + \left(g_{m4} + sc_{\pi 4} + \frac{1}{r_{\pi 4}}\right)(1 + sc_{\pi 3}r_b)\right\}^{-1} \quad (2.7)$$

Finally the summation required in the transversal filter is performed in the current mode. The output current signals of all the taps are tied together to an external pull up resistor via a current buffer, which is a common-base amplifier formed by transistors Q7 and Q8 in figure 2.6. Figure 2.8 shows the simulated magnitude response of the Gilbert variable gain amplifier. The 3-dB cutoff frequency of the amplifier is 14.5 GHz.

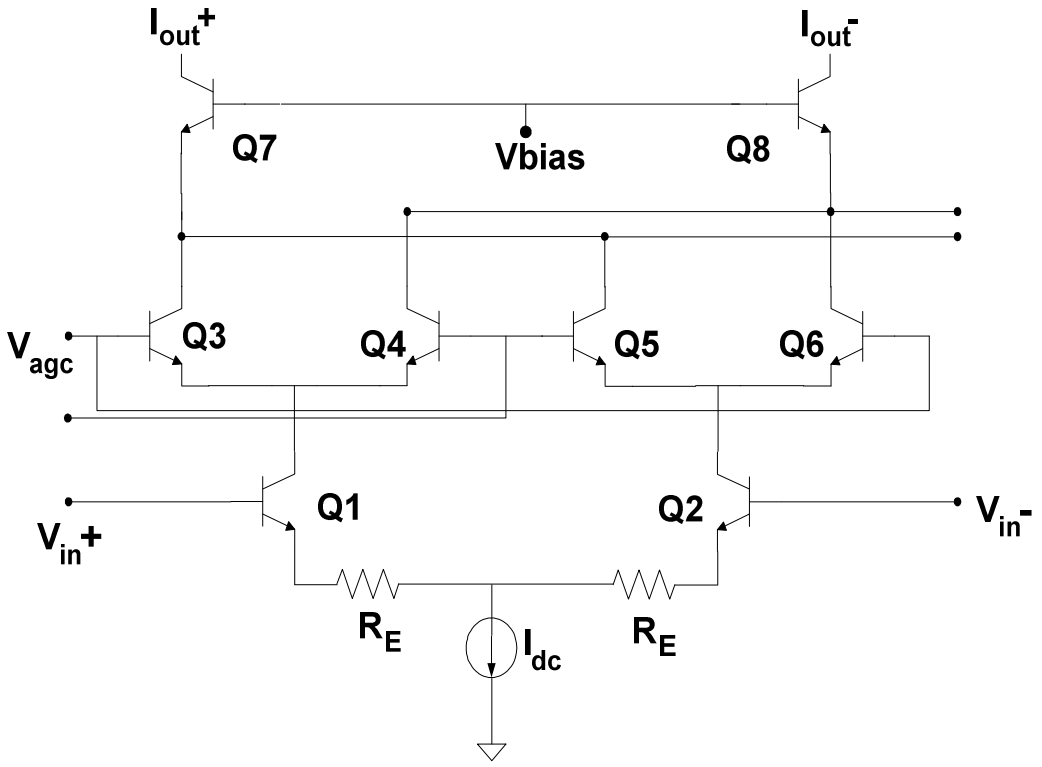

Figure 2.6 Tap weights implemented using Gilbert variable gain amplifier.

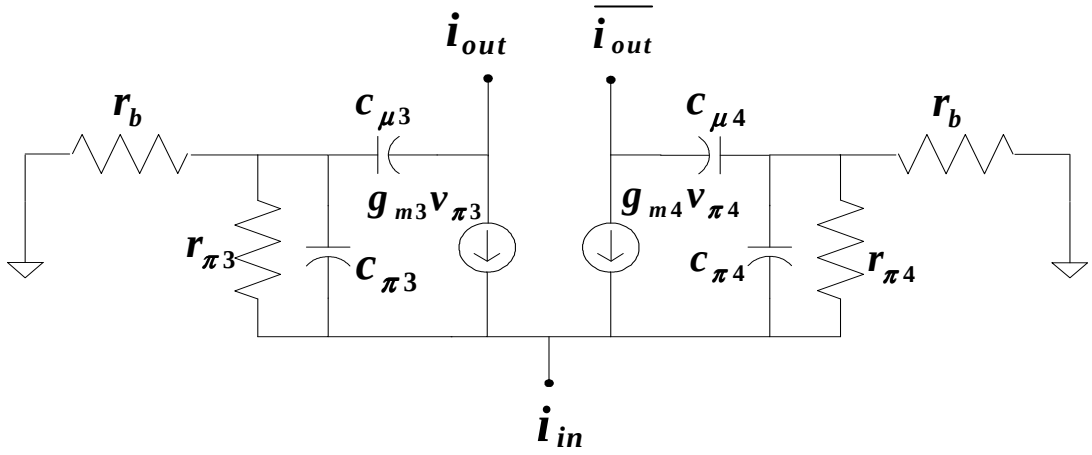

Figure 2.7 Small signal model of the gain control circuit.

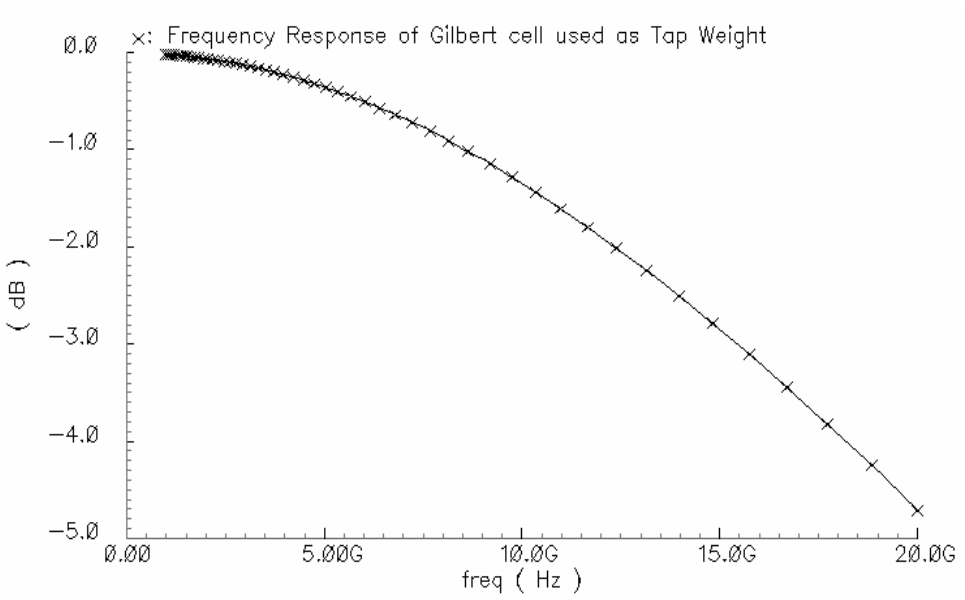

Figure 2.8 Magnitude response of the Gilbert variable gain amplifier.

2.3 Biasing blocks

Figure 2.9 shows the voltage reference bandgap circuit used in the design. The current flowing through resistor R1 is determined by the V_{be} (base to emitter voltage) difference of transistors Q1 and Q2. This current has a PTAT (Proportional to Absolute

Temperature) dependence. The value of this current is chosen by the ratio of Q1 & Q2 and resistor R1. For this design, current of $100\,\mu A$ was chosen, smaller current could be chosen, but it would be more susceptible to noise. Having fixed the current the ratio of Q1 & Q2 is selected as six. While any ratio could be chosen, it is recommended to keep this value smaller than ten because the matching capabilities start to degrade as the area spread becomes large [16].

$$R1 = \frac{V_T \ln(TransistorRatio)}{I_{PTAT}} \tag{2.8}$$

The value of R2 is chosen so that the current flowing through it has equal and opposite temperature coefficient than that of R1 and can be calculated from the following equation.

$$\frac{d(I_{PTAT})}{dT} = (1/R2)(\frac{d(V_{be})}{dT} \tag{2.9}$$

$$\frac{d(I_{PTAT})}{dT} = (1/R2)(V_{g0} - \frac{T}{T_r}[V_{go} - V_{be}(T_r)] \tag{2.10}$$

where V_{g0} is bandgap voltage at zero Kelvin, $V_{be}(T_r)$ is V_{be} at room temperature.

Having chosen the values of R1 and R2 we find in figure 2.9 that the current flowing at the collector of Q1 is the sum of PTAT and IPTAT currents, and we have a constant current at that node, the voltage drop across the resistor connected to the collector of Q1 (VQ1) is also temperature independent. However, Vref = VQ1 + V_{be}(Q3). Assuming that V_{be}(Q3) and the V_{be} of the bottom current transistors of bipolar CML circuits match, Vref can be used to drive the base of those current transistors to provide a constant voltage swing independent of temperature.

If we delete R2 then Vref becomes independent of temperature, and when used to drive the base of the bottom current source transistors of bipolar amplifiers, would provide constant transconductance.

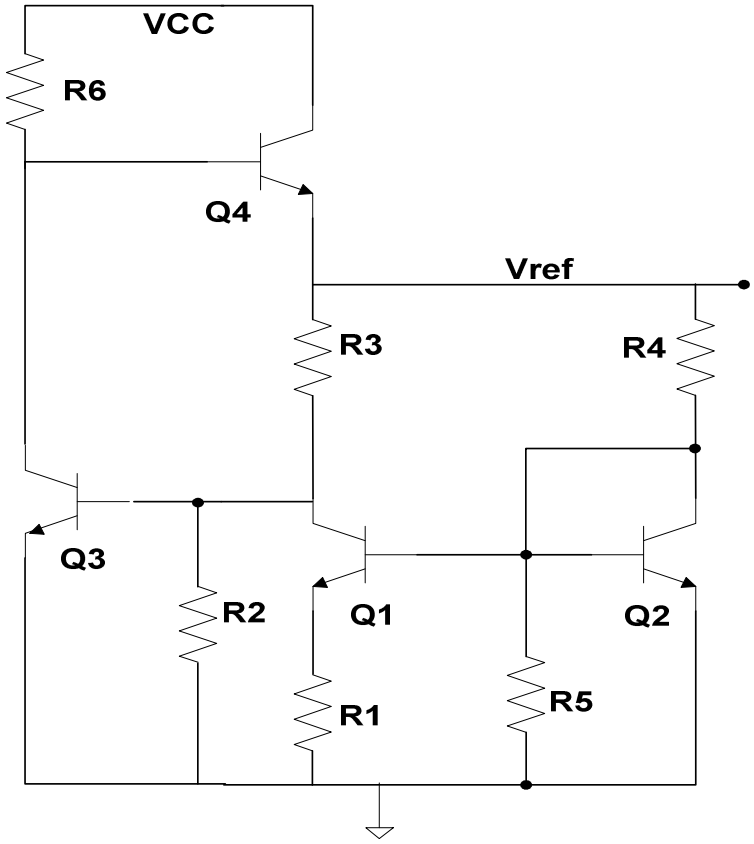

Figure 2.9 First order band gap circuit used to drive the amplifiers on the chip.

Figure 2.10 shows the single ended to differential converter. The circuit takes a single ended input and steers the current to one of the two transistors in the differential pair. The output logic level is given by the product of the current and the load resistor.

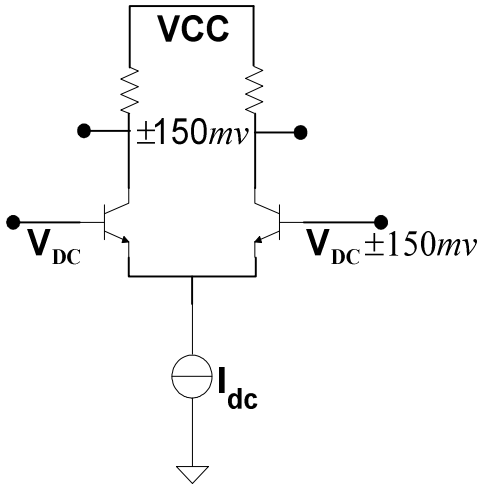

Figure 2.10 Single ended to differential converter for the tap weights.

2.4 Prototype design and measured results

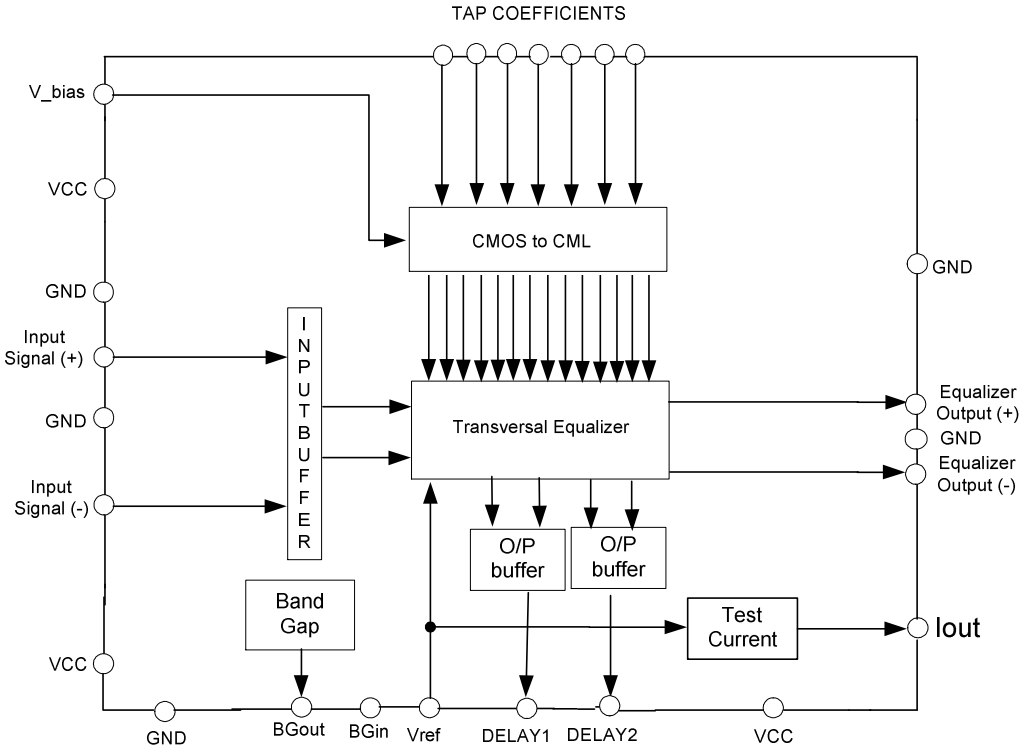

Figure 2.11 Block diagram of the transversal filter.

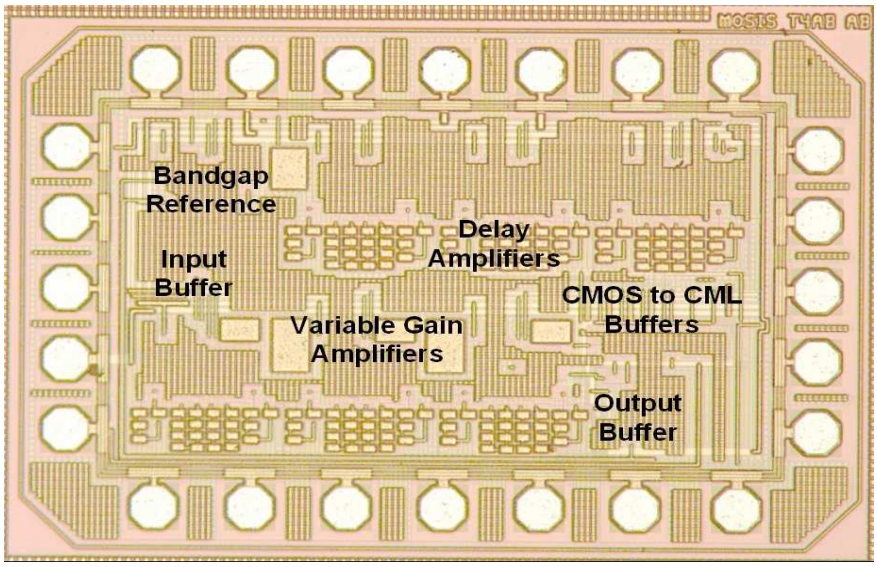

Figure 2.12 Fabricated transversal filter chip.

The 3.5 GHz transversal filter was implemented in a 45 GHz SiGe technology with a total 2.16 mm^2 die area including the pads. The chip consumes 250 mW of power. The filter RFIC includes a bandgap reference to provide temperature independent constant current sources for the amplifiers. The filter RFIC also includes an input buffer, output buffer and single ended to differential converter buffers. Figure 2.12 shows the die photo of the transversal filter chip.

The frequency response of the integrated filter was measured using a vector network analyzer. The measured filter transfer functions under different tap weights are shown in figures 2.13 to 2.17. As can be seen from the measured results the transfer function of the filter can be adaptively tuned by changing the tap weights. It can be noticed that by changing the tap weights the filter is able to change the location of zeros in its transfer function to implement different filter characteristics.

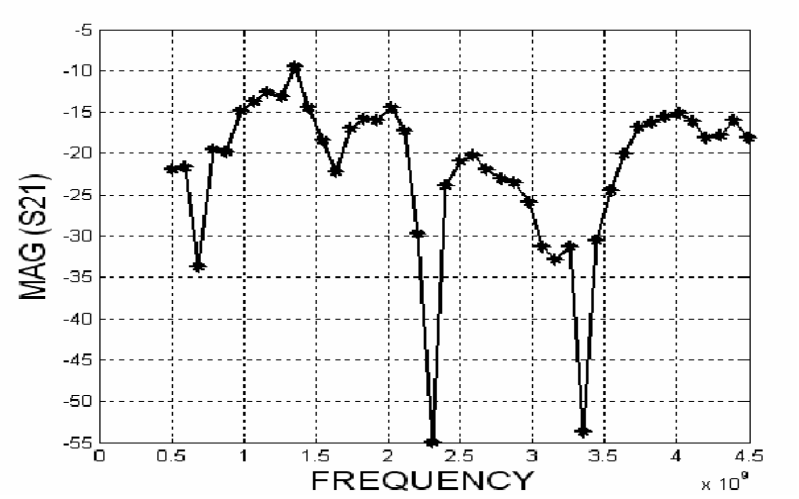

Figure 2.13 Filter transfer function with notches at 2.3 GHz and 3.3 GHz.

When the tap coefficients are set as -40, 75, -40, 75, -40, 75, 90 [mV], the magnitude of the notch is -55 dB, which provides -37 dB notch rejection compared to the pass band magnitude as shown in figure 2.13.

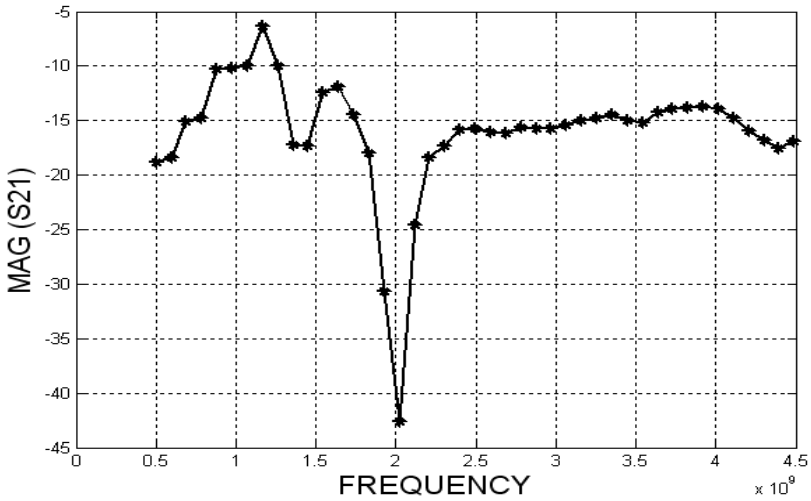

Figure 2.14 Measured filter transfer function with notch at 2 GHz.

When the filter coefficients are set as -85, 30, -20, 0, 30, 0, 0 [mV], the magnitude of the notch is -43 dB, which provides -30 dB notch rejection compared to the pass band magnitude as shown in figure 2.14.

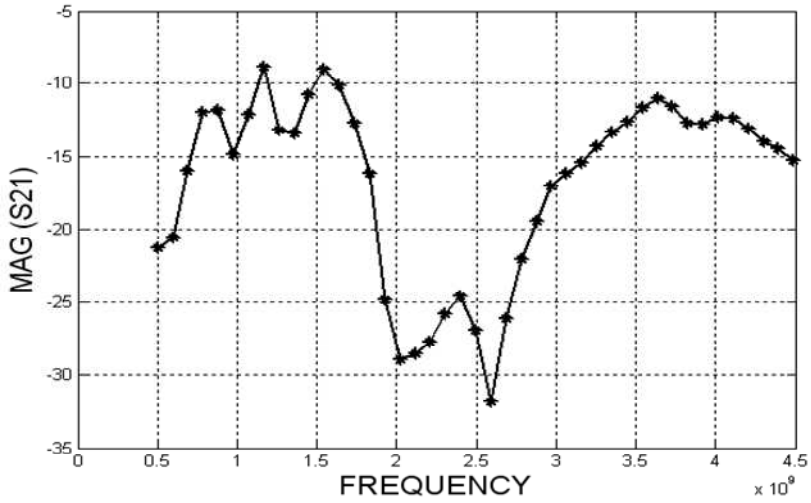

Figure 2.15 Filter transfer function with band rejection from 2 to 2.7 GHz.

When the coefficients are set as 0, 60, 0, 25, 0, 100, 60 [mV], the filter achieves a band-rejection of -20 dB from 2 GHz to 2.7 GHz as shown in figure 2.15.

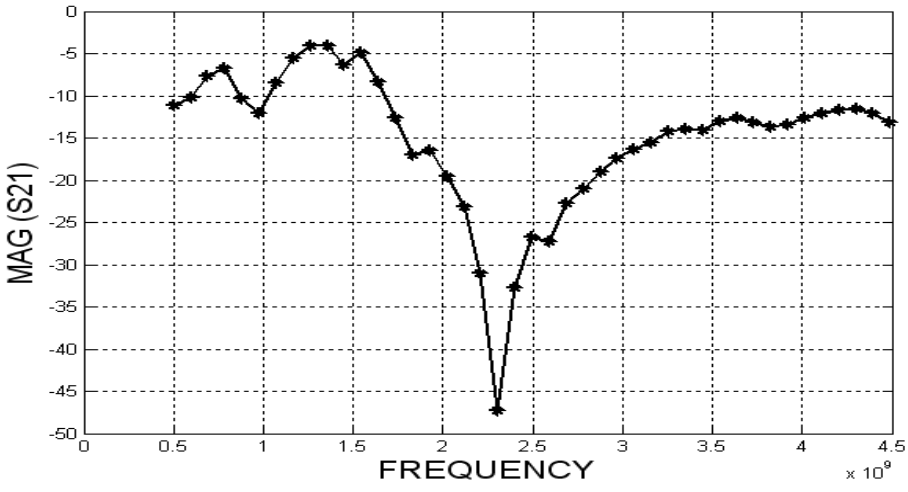

Figure 2.16 Measured filter transfer function with notch at 2.3 GHz.

When the filter coefficients are set as 100, -10, -10, 0, 55, 0, 20 [mV], the magnitude of the notch is -47 dB, which provides -33 dB notch rejection compared to the pass band magnitude as shown in figure 2.16.

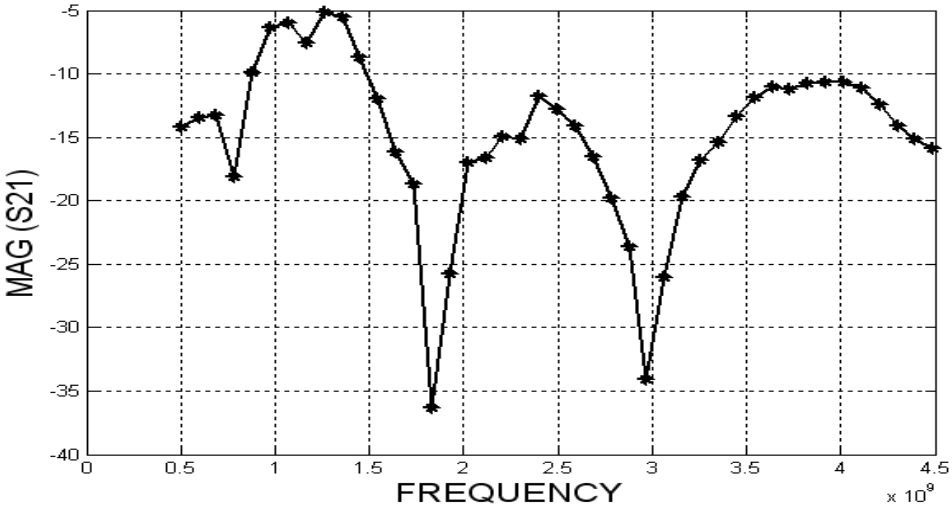

Figure 2.17 Filter transfer function with notches at 1.7 GHz and 2.9 GHz.

When the filter coefficients are set as 70, 0, -40, 0, -40, 35, 30 [mV], the magnitude of the notch is -45 dB, which provides -35 dB notch rejection comparing to the pass band magnitude as shown in figure 2.17.

2.5 Conclusions

A low power 3.5 GHz analog transversal filter in a 47 GHz SiGe technology has been implemented. The RF filter utilizes cascaded Cherry-Hooper amplifiers for delay stages and Gilbert variable gain amplifier for continuous gain tuning. The delay stage using active devices greatly reduces the die area compared to passive delay lines. Measured results show that by adjusting the tap coefficients, the integrated programmable filter chip

is capable to adapt zeros at various frequencies up to 3.5 GHz with various filter characteristics. Thus the integrated transversal filter can be used to mimic the inverse transfer function of dispersive communication channels for dispersion compensation. The measured noise figure of the entire filter is 32 dB. It can also be used as a programmable notch filter in wireless transceiver designs.

Chapter 3: Delay Analysis and Optimal Biasing for Current Mode Logic Circuits

3.1. Introduction

This chapter presents a delay analysis for Current Mode Logic (CML) circuits operating at the GHz range. The optimal biasing point for CML circuits is obtained considering the circuit speed and power consumption. In recent years, modern communication systems demand for high performance circuits has increased. Apart from the required high frequency of operation, low power consumption has become an important feature for wireless communication systems. In the design of these high performance circuits, series gated two level transistor topologies such as current mode logic and emitter coupled logic are typically used. A novel biasing strategy called "Keep alive" for CML topology is proposed to achieve improved performance in terms of speed when the circuit is biased at 10% to 30% of the peak f_T current. The proposed biasing scheme utilizes a regular bias that supports the normal CML operation and a small "Keep alive" bias that keeps the upper level transistors in "ON" states for speed improvement.

The maximum speed of CML circuits is limited by the RC open circuit time constants of the series gated latches and gates. It is therefore imperative to conduct a detailed study of delay through CML topology and develop techniques to extract its maximum performance. There are a few propagation delay models available in literature [18, 19, and 20]. The model presented in [18] is derived using sensitivity analysis and the model

presented in [20] is based on linearization of the device which is complex for use during pencil and paper design. The model presented in [19] has been used to evaluate the performance of CML gate with “Keep alive” biasing where the delay has been expressed as sum of RC time constants derived from the small signal model of the gate.

While CMOS logic circuit still tends to dominate the field of digital integrated circuits, it is not suitable for high speed designs as the turn on and turn off times limit its maximum operational speeds. Since the rail-to-rail CMOS voltage swing is large (from zero to power supply), the time taken to charge and discharge capacitors is also large. Moreover, the rate of charge and discharge of capacitors in CMOS circuits is not constant. The power consumption of CMOS circuits increases with frequency. The digital switching noise associated with the CMOS logic circuit is also much larger than CML circuits that use constant current sources. A better option for high-speed circuit designs would be to use CML or ECL topologies. The main advantages of CML logic lies in its high operation speed, its constant power consumption independent of operation frequency. The CML voltage swing is small making it suitable for high speed and low noise applications. Since its operation is normally differential, CML circuits generate less noise and result in lower dynamic power dissipation. However the main disadvantage of CML circuits is its static power dissipation. ECL gates consist of differential amplifier, temperature and voltage compensated bias network, emitter follower output. The operation of ECL circuits is similar to that of CML circuits. The power consumption in ECL is larger than that of CML due to the presence of emitter followers at the input and output.

3.2 Current mode logic: operation

A current mode logic gate in general consists of three components: pull up load resistors, constant current source and logic analyzing Pull Down Network (PDN). Figure 3.1 shows the general diagram of the CML gate.

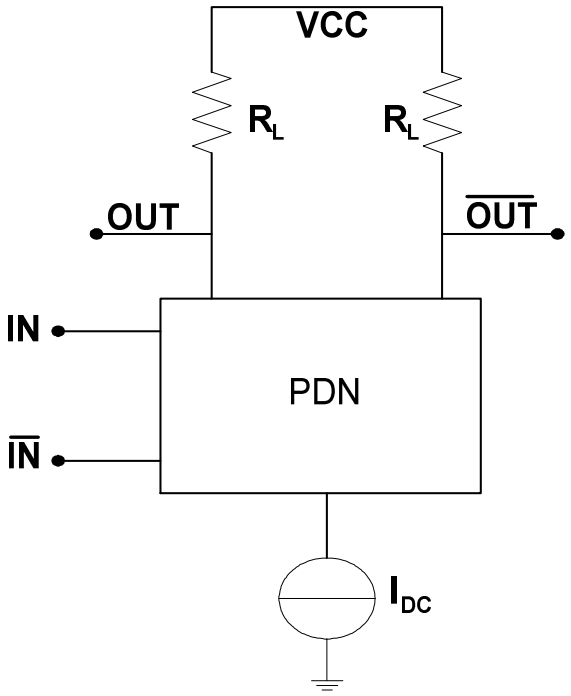

Figure 3.1 Current mode logic gate.

The input and outputs of the gate are differential, true and complement signals of all logic inputs must be available to the gate. The pull down network then evaluates the logic function and steers the current I_{DC} to one of the two load resistors. The load resistor R_L connected to the current source through the pull down network then has a voltage drop of $\Delta V = R_L \times I_{DC}$ across it. The other resistor has no current flowing through it and its output node is held at VCC. The voltage swing seen across the two outputs differentially is given by the voltage drop ΔV and is determined solely by the magnitude of the current

and the load resistors. This voltage swing is generally 200 to 400 mV. In mixed signal designs there are many advantages of using CML logic style. Owing to the fact that the switching takes place in current mode and the output logic levels are in the order of few hundred millivolts they can achieve very high speeds (GHz range). In mixed signal environments where analog and digital blocks are placed on the same substrate a constant current supply from the power supply is highly desirable since substrate noise and $\frac{dI}{dT}$ noise have become a serious issue in today's chips. Substrate, supply and ground bounce during switching of digital gates induce noise and can corrupt the single ended inputs as its reference point changes due to the bounce. These effects are in negligible in CML circuits in comparison with CMOS circuits since CML is a differential logic and inherently rejects common mode noise. It has also been shown that for some high speed applications the CML logic can consume less power than their CMOS counterparts while maintaining all the benefits of a differential logic style mentioned above [23]. The energy delay product for both the logic styles has been analyzed in [17, 21, 22, and 23]. The equation for the energy delay product for CML logic using MOS transistors is reproduced here [23].

Defining energy as the power delay product, N being the logic depth and C being the load capacitance on the output node we have

$$Power_{CML} = N \cdot I \cdot V_{dd} \tag{3.1}$$

$$Delay_{CML} = \frac{C \cdot \Delta V}{I} \tag{3.2}$$

$$Energy_{CML} = N \cdot C \cdot \Delta V \cdot V_{dd} \tag{3.3}$$

$$ED_{CML} = \frac{N \cdot C^2 \cdot \Delta V^2 \cdot V_{dd}}{I} \tag{3.4}$$

An interesting thing to note is that unlike CMOS logic the equation for the energy delay product of a CML gate (ED_{CML}) has no theoretical minimum value [23]. Since ED_{CML} is proportional to the square of the voltage swing ΔV and inversely proportional to the current I, one could keep reducing ED_{CML} by reducing ΔV or increasing I. However, in practice the minimum swing required and maximum current allowed is dictated by reliability and robustness required. Also ED_{CML} is proportional to logic depth N, and when compared to CMOS its performance degrades with increasing N. Since CML logic will consume current even when it is not switching, it is not preferred for gates operating at low frequencies, but for gates with high performance requirements CML can achieve better energy delay and power delay requirements compared to CMOS.

3.3 Series gated CML topologies

In this section, some common CML gates used in mixed signal designs are presented along with their advantages and disadvantages. Figure 3.2 shows two input NAND and MUX gates. All CML logic functions have one current source and two load devices. The pull down network used to analyze the logic function is designed using sets of differential pairs.

In figure 3.2 one can see that AND, NAND, OR, NOR gates have the same circuit structure. It is possible to realize those four gates just by changing the order of its inputs and outputs. This is advantageous since all the four gates would have the same area,

power dissipation and propagation delay. This leads to better estimation of timing issues, size and power consumption. This also reduces the need for Boolean manipulation to obtain inverting logic. However, as the logic depth increases the levels of series stacked differential pairs also increase calling for higher supply voltage and increase in static power consumption. Hence, it is advisable to reduce the logic depth of the function and restrict to three levels of logic per current tail.

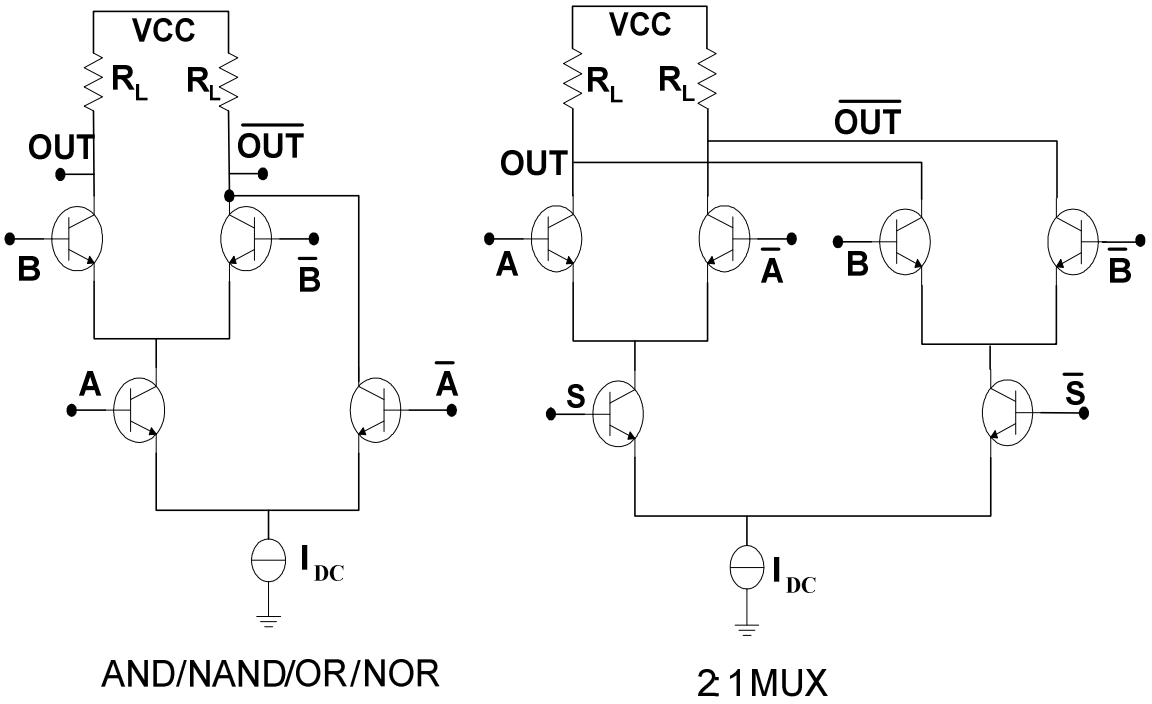

Figure 3.2 AND/NAND/OR/NOR and MUX CML gates.

3.4 Delay analysis of CML gate

In this section, the delay time constants of a series gated CML D-latch, which is the common basic building block of many switching circuits have been modeled. Figure 3.3 and figure 3.4 illustrate the circuit schematics of the D-latch and its small signal (half-circuit) model. For worst case propagation delay, the upper level data inputs are set as

constant and a step input is provided at lower level clock transistors [19, 20]. The analysis of the half circuit is sufficient for differential operations.

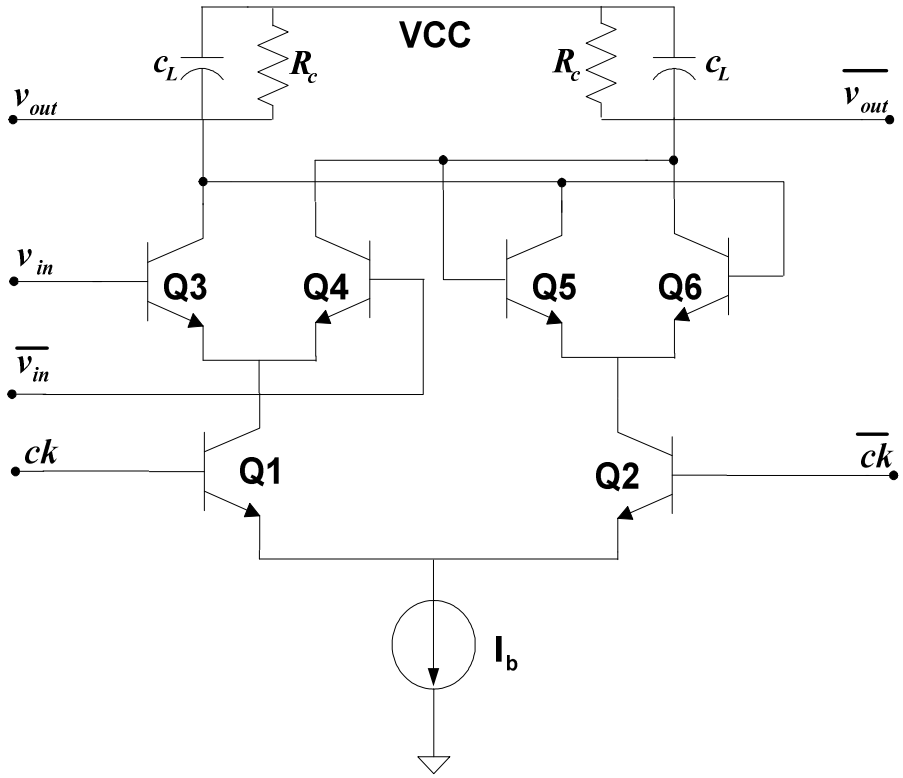

Figure 3.3 Schematic diagram of CML D-Latch.

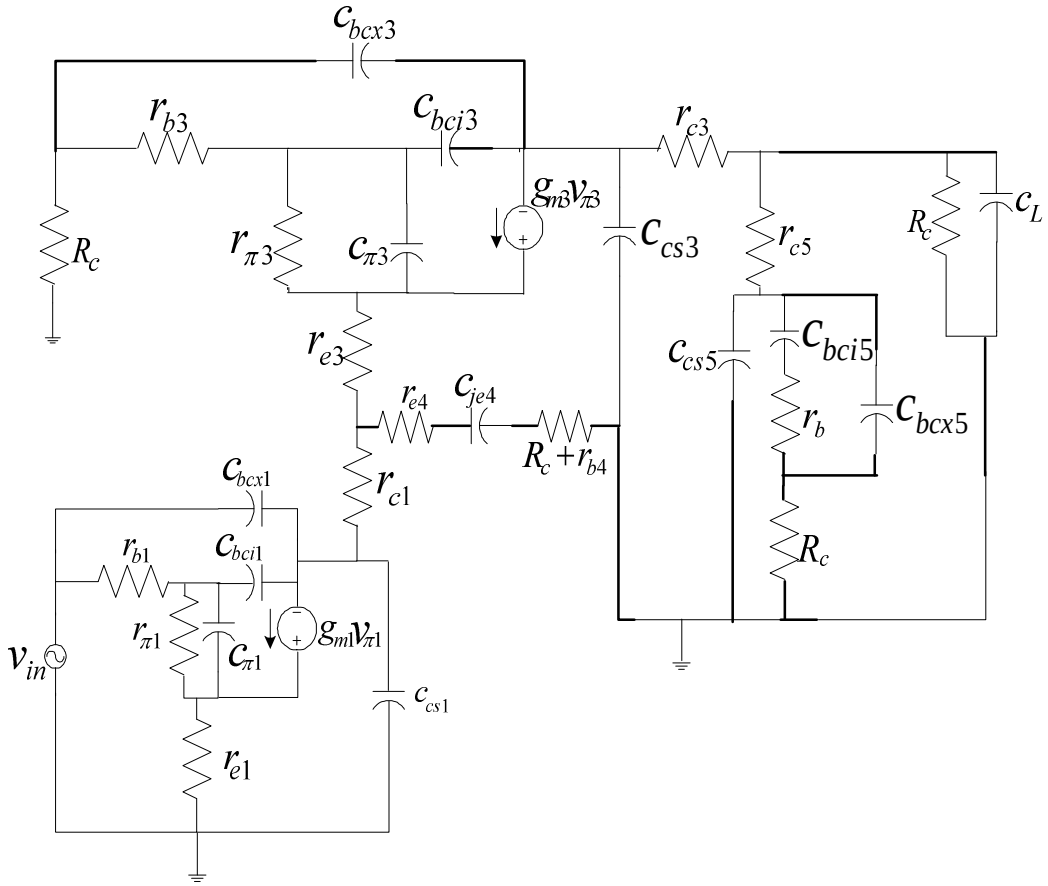

Figure 3.4 Small signal half circuit model of CML D-Latch.

The above figure is the small signal half circuit model of the CML D-Latch and the delay through the gate can be expressed as the sum of RC time constants, assuming dominant pole behavior. The open circuit time constants associated with various capacitors can be derived from the equivalent circuit model shown in figure 3.4. The time constants associated with lower transistors can be derived as

$$\tau_{\pi l} = \frac{r_{el} + r_{bl}}{1 + g_{ml} r_{el} + \dfrac{r_{el} + r_{bl}}{r_{\pi l}}} C_{\pi l} \qquad (3.5a)$$

$$\tau_{bcil} = \left[\begin{array}{l} \left(r_{cl} + r_{eu} + \dfrac{r_{\pi u} + r_{bu} + R_c}{\beta + 1} \right) + \\ r_{bl} \left(1 + \dfrac{g_{ml} \left(r_{cl} + r_{eu} + \dfrac{r_{\pi u} + r_{bu} + R_c}{\beta + 1} + r_{el} \right)}{1 + g_{ml} r_{el}} \right) \end{array} \right] \cdot C_{bcil}$$

(3.5b)

$$\tau_{bcxl} = \left(r_{cl} + r_{eu} + \frac{r_{\pi u} + r_{bu} + R_c}{\beta + 1} \right) C_{bcxl} \tag{3.5c}$$

$$\tau_{csl} = \left(r_{cl} + r_{eu} + \frac{r_{\pi u} + r_{bu} + R_c}{\beta + 1} \right) \cdot C_{csl} \tag{3.5d}$$

The time constants associated upper transistors are listed as

$$\tau_{\pi 3} = \frac{1}{\left(g_{m3} + \dfrac{1}{r_{\pi 3}} \right)} \cdot C_{\pi 3} \tag{3.6a}$$

$$\tau_{bci3} = \left(2R_c + r_{cu} + r_{bu} \right) \cdot C_{bci3} \tag{3.6b}$$

$$\tau_{bcx3} = \left(2R_c + r_{cu} \right) \cdot C_{bcx3} \tag{3.6c}$$

$$\tau_{bci5} = \left(2R_c + r_{cu} + r_{bu} \right) \cdot C_{bci5} \tag{3.6d}$$

$$\tau_{bcx5} = \left(2R_c + r_{cu} \right) \cdot C_{bcx5} \tag{3.6e}$$

$$\tau_{cs3} = \left(R_c + r_{cu} \right) \cdot C_{cs3} \tag{3.6f}$$

$$\tau_{cs5} = \left(R_c + r_{cu} \right) \cdot C_{cs5} \tag{3.6g}$$

$$\tau_{je4} = \left(R_c + r_{bu} + 2r_{eu}\right) \cdot C_{je4} \tag{3.6h}$$

$$\tau_{cload} = R_c \cdot C_{load} \tag{3.6i}$$

where subscripts “u” and “l” denote upper and lower transistors and “c”, “b”, “e” and “s” denote collect, base, emitter and substrate of the corresponding transistors. The delays associated with upper and lower transistors can be found out by summing all the delays in equation 3.5 and equation 3.6, respectively.

$$t_{lower} = \tau_{\pi l} + \tau_{bcil} + \tau_{bcl} + \tau_{csl} \tag{3.7a}$$

$$\begin{aligned} t_{upper} &= \tau_{\pi 3} + \tau_{bci3} + \tau_{bcx3} + \tau_{bci5} + \tau_{bcx5} \\ &+ \tau_{cs3} + \tau_{cs5} + \tau_{je4} + \tau_{cload} \end{aligned} \tag{3.7b}$$

$$t_{total} = 0.69 \times \left(t_{lower} + t_{upper}\right) \tag{3.7c}$$

The capacitances used in equations 3.5 and 3.6 are assumed to be constants when bias current varies, which is a good approximation when the swing is restricted to 150 mV.

3.5 Optimum biasing for CML circuits

Figure.3.5 plots the gate propagation delay with respect to the bias current normalized to the peak f_T current using equations 3.7a, 3.7b and 3.7c. It comes as no surprise that the optimum biasing current to provide minimum delay is indeed the transistor peak f_T current. According to figure 3.5, it is obvious that there is not much speed improvement obtained by increasing the biasing current beyond 60% of the peak f_T current [19]. Biasing the circuit close to the peak f_T current may cause the actual bias current to go

beyond the peak f_T current under temperature, supply and process variations, which leads to speed penalty as the result of current crowding and the conductivity modulation effects in the base region.

Unless absolutely high speed of operation is required, it is a good practice, to bias the CML circuit at 60% of the peak f_T current to save unnecessary power consumption. Figure 3.5 shows that biasing the CML circuits at 40% of the peak f_T current (the circled region in the figure) can achieve about 80% of the maximum speed that corresponds to the peak f_T current.

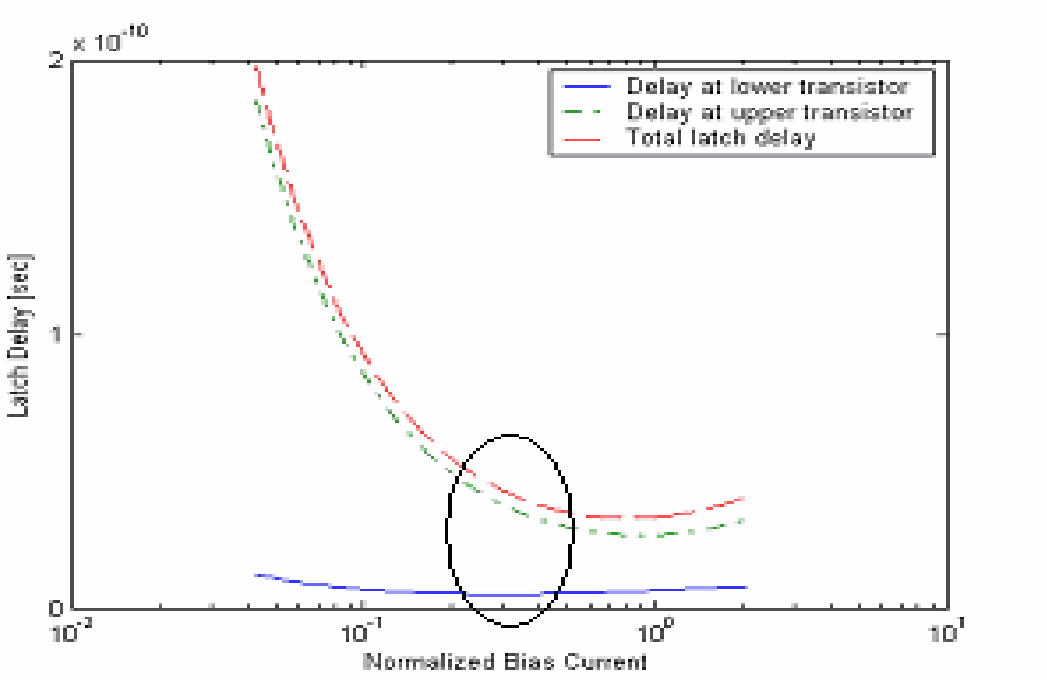

Figure 3.5 CML D-latch delay versus normalized bias current.

Also it can be seen from the above figure that the optimum bias current to give minimum delay is not the same for both upper and lower level transistors. The lower transistors have minimum delay at a lower bias current than the upper transistors. This is

evident from the fact that the upper transistors have more time constants associated with it. In the following section, a CML biasing technique is presented. The proposed biasing scheme utilizes a regular bias that supports the normal CML operation and a small "Keep alive" bias that keeps the upper level transistors in "ON" states for speed improvement when the circuit is biased at 10% to 30% of the peak f_T current.

3.6 "Keep alive" biasing technique

The delay model developed in the previous sections can be used to optimize CML circuit to further improve circuit performance in terms of power consumption and speed [62].

A dependence of CML latch delays on bias current is illustrated in figure 3.6. It is evident that the CML latch delay is dominated by the delay associated with the upper transistors. Note that the delay contributed by the upper level transistors decreases much faster than that contributed by the lower level transistors when the biasing current increases. In other words, increasing biasing current can dramatically reduce the delay at upper level transistors, yet there is not much effect for the delay improvement for lower level transistors. Hence, reducing the delay due to upper level transistors is critical to improve CML switching speed.

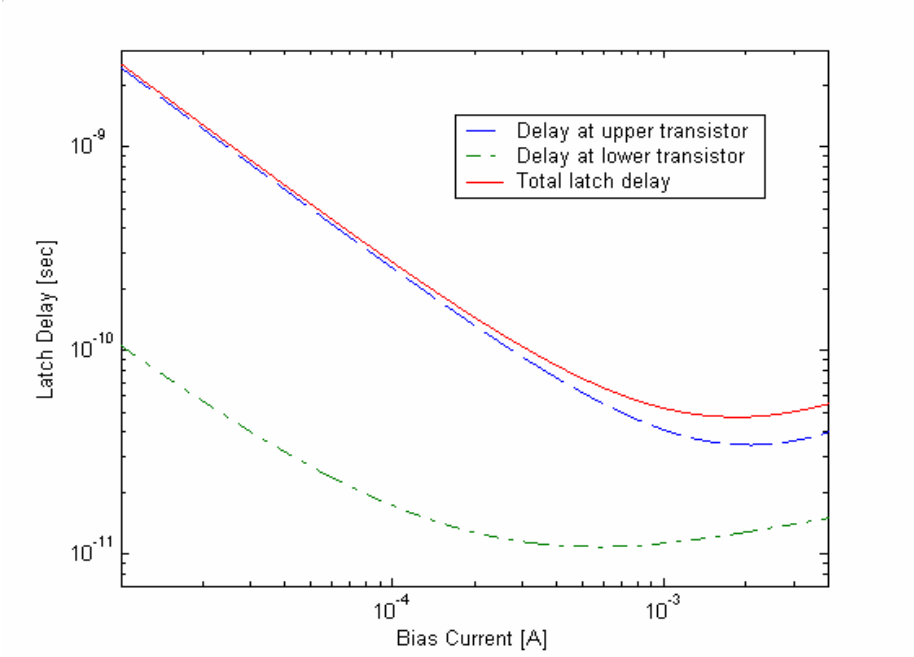

Figure 3.6 CML latch delays versus bias current.

Based on the previous discussion, it is intuitive that there will be a speed improvement if the circuit is biased in a manner, such that after the clock signal arrives the upper level transistors have slightly higher bias currents than the lower level transistors. The total bias current remains the same. The only difference from conventional CML biasing arrangement is that the biasing currents are split such that the upper level transistors are biased at slightly higher current than the lower level ones. For instance, the bias currents can be reduced by about 20% for the lower level clock transistors and supply the extra current to the upper level data transistors. Figure 3.7 shows a D-flip-flop biased in such a manner. This biasing technique is named as “Keep alive” since there will always be a small amount of bias current flowing through the upper level transistors, keeping them alive in slightly “turn-ON” states regardless of the clock and data. The main advantage of this type of biasing arrangement is that the data

transistors are always slightly “ON” independent of clock signal. As a result, the capacitors associated with the upper level transistors, which are the dominant contributors to the CML propagation delay, will be charged to a certain level. When the clock signal arrives, it takes relatively less time for the capacitors to reach their steady state values. Moreover, optimization can also be performed in terms of transistor sizing for upper and lower transistors.

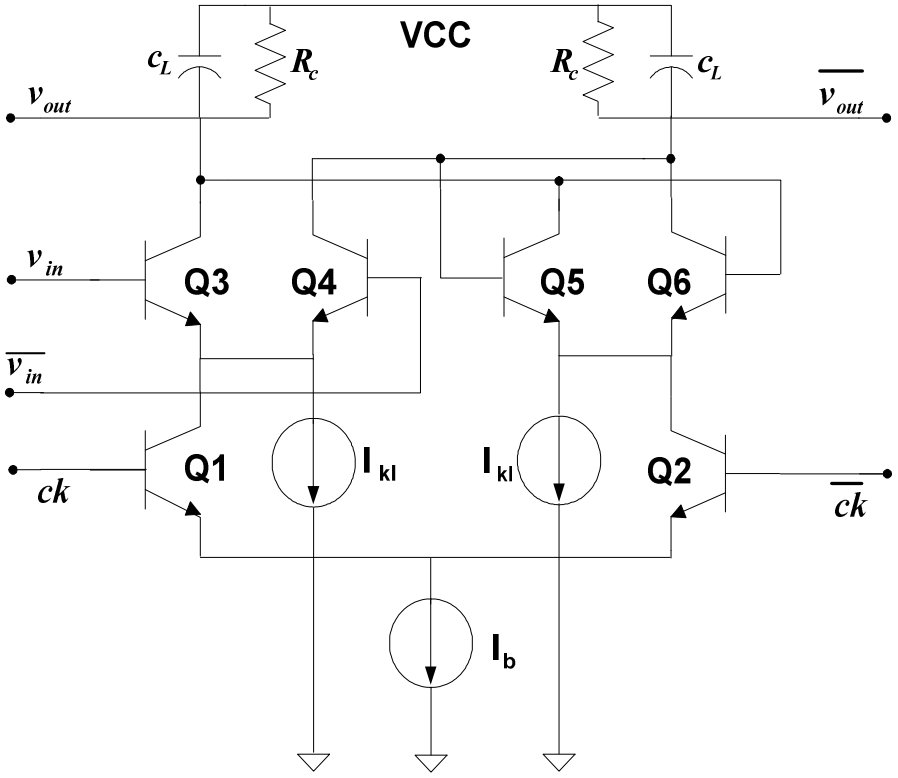

Figure 3.7 "Keep alive" biasing technique for CML D-latch.

3.7 Simulation results

The CML circuits with the proposed “Keep alive” biasing scheme has been simulated in a 47 GHz SiGe technology. A divided-by-two circuit is chosen to test the performance of the proposed CML D-latch. The propagation delay through a divide-by-two circuit

without a “Keep alive” is about 96 ps, as shown in the figure 3.8 and the propagation delay through the circuit with a “Keep alive” is about 85 ps, as shown in figure 3.9. Hence, a speed improvement of about 11% is achieved by using the proposed “Keep alive” biasing scheme.

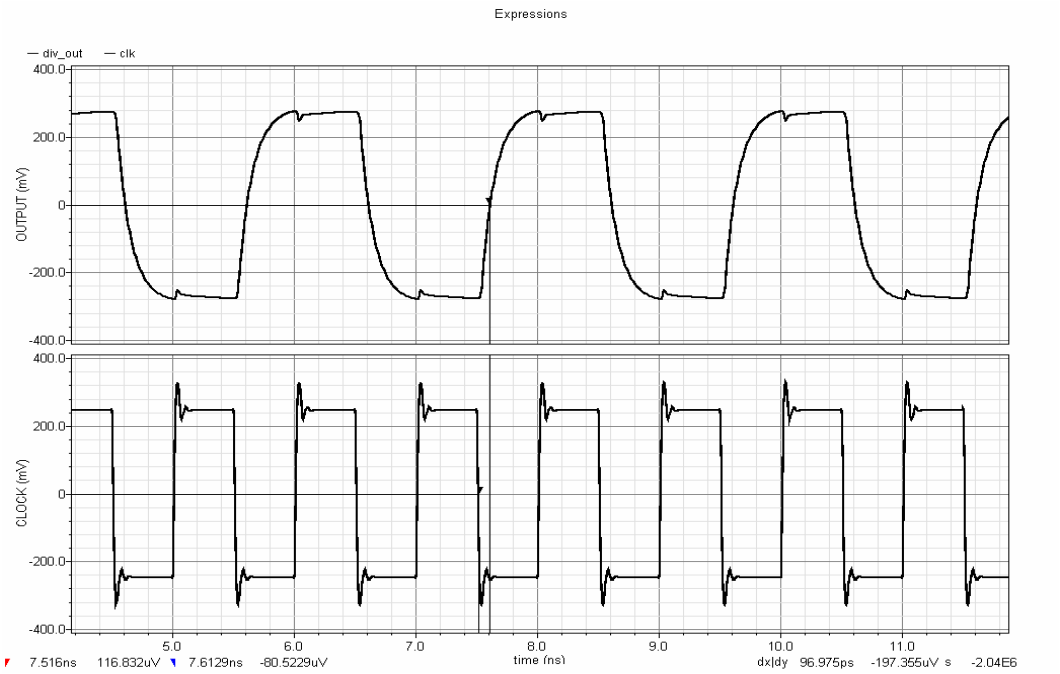

Figure 3.8 Propagation delay without "Keep alive" biasing.

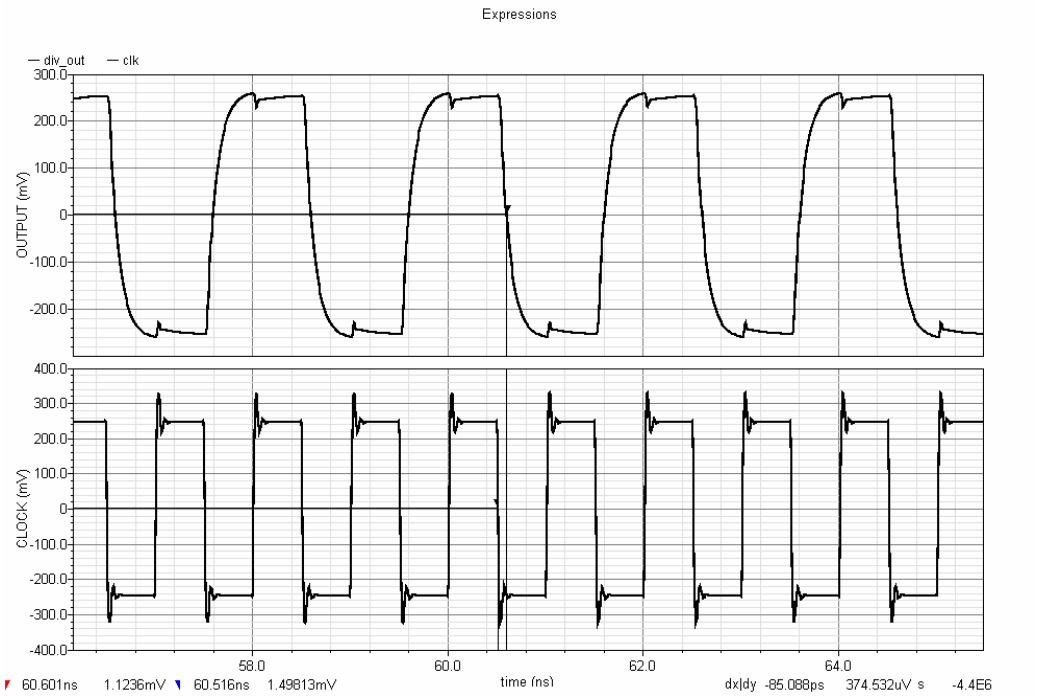

Figure 3.9 Propagation delay with "Keep alive" biasing.

3.8 Conclusion

The delay of a CML circuit is modeled in terms of its delay elements such as transistor junction capacitances. The contribution of these individual delay elements to the final propagation delay is analyzed to explore circuit and device optimization. Also studied are, optimal biasing and a novel “Keep alive” biasing scheme for CML circuits to be used in high speed and low power applications.

Chapter 4: Voltage Controlled LC Oscillators

4.1 Oscillator basics

An oscillator is a circuit that takes in DC power and noise as input and generates a periodic signal as the output.

Based on the implementation, oscillators can be classified as crystal oscillators, resonator based oscillators, ring oscillators, relaxation oscillator etc. In this chapter, we will confine ourselves to LC oscillators.

To predict whether the oscillator will start and produce a periodic signal it can be modeled as linear feedback system as shown below. Even though oscillators operate in weakly or strongly nonlinear regions linear analysis of the oscillation conditions provides sufficient design insights for reliable start up.

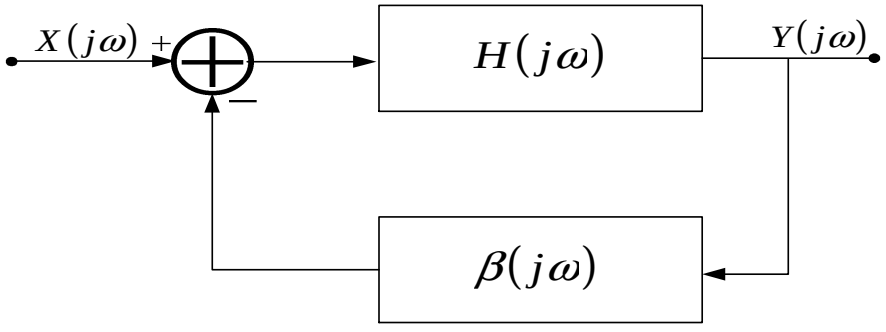

Figure 4.1 Feedback model for analyzing oscillator start up conditions.

The transfer function of the model shown in figure 4.1 is given by equation 4.1.

$$\frac{Y(j\omega)}{X(j\omega)} = \frac{H(j\omega)}{1 + H(j\omega)\beta(j\omega)} \tag{4.1}$$

Known as Barkhausen conditions [24], the conditions for steady state oscillations are :

$$\left|H(j\omega)\beta(j\omega)\right| = 1 \tag{4.2}$$

the above equation is known as the gain condition for steady state oscillations to occur. The above equation states the necessary conditions for steady state self sustaining oscillation to occur but not for oscillator start up. It is desirable that once powered up the circuit starts oscillating due to the noise in the circuit. In order to ensure reliable start up the open loop gain of the feedback system in figure 4.1 must be greater than unity. The gain condition for reliable start up is given by equation 4.3.

$$\left|H(j\omega)\beta(j\omega)\right| > 1 \tag{4.3}$$

Once the oscillation has started the open loop gain reduces to unity through mechanisms like self limiting or amplitude control. The other Barkhausen condition is known as the phase condition and is given as

$$\angle H(j\omega)\beta(j\omega) = (2m+1)180^{\circ} \tag{4.4}$$

The total open loop phase shift must be (2m+1)180 degrees where m is an integer. An LC oscillator can be modeled as a linear feedback system as shown in figure 4.2.

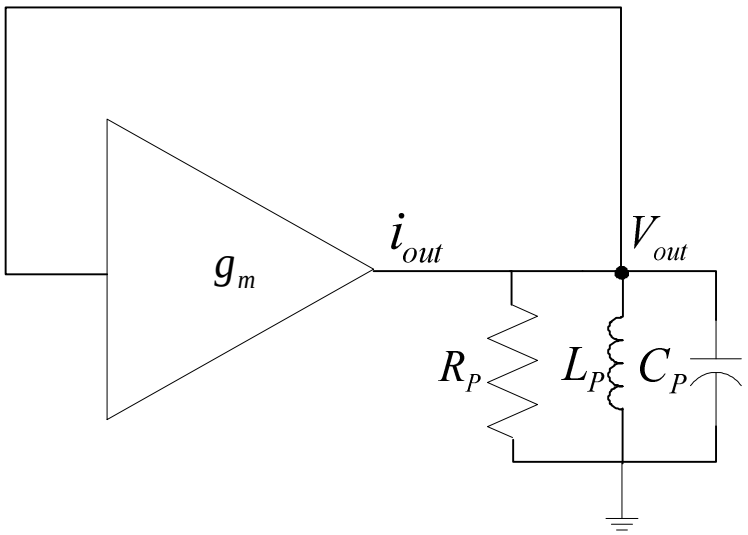

Figure 4.2 Linear feedback model of an oscillator.

The transfer function $H(j\omega)$ is given by the transconductance g_m and the feedback transfer function $\beta(j\omega)$ is given by the tank formed by inductor L_P, capacitor C_P and their associated losses R_P.

The tank transfer function can be calculated as

$$\beta(j\omega) = \frac{R_P}{1 + jR_P\left(\frac{\omega^2 - \omega_o^2}{\omega \times \omega_o}\right)Q_P} \tag{4.5}$$

where $\omega_o = \frac{1}{\sqrt{L_P C_P}}$ is the oscillation frequency and Q_P is the tank quality factor given by $Q_P = R_P\sqrt{\frac{C_P}{L_P}}$ (4.6)

at the oscillation frequency the open loop gain is $g_m R_P$ and for reliable start up $g_m > \frac{1}{R_P}$ at least by factor of three to four.

In negative resistance modeling of the LC oscillator the transconductor with positive feedback is modeled as negative resistance of $-\frac{1}{g_m}$ to compensate the losses in resonator.

4.1.1 Integrated inductors

The resonator quality factor Q_P is a very important physical parameter that greatly influences the performance of an oscillator. Oscillators with high quality factor resonators have lower phase noise and lower power consumption and higher tuning range. In most fabrication processes, below certain oscillation frequency (less than 40 GHz) the quality factor of the tank is dominated by the inductor quality factor.

During the past decade, implementation of high performance transceivers employed off chip inductors due their high quality factor. However, with the advancement of technology it is possible to integrate high Q inductors on chip. Planar inductors are widely used today because of ease of fabrication despite their large area. Integrated inductors and its parasitics are modeled as lumped RLC circuit to facilitate simulations during design. Figure 4.3 shows the lumped π model of the inductor [25, 26].

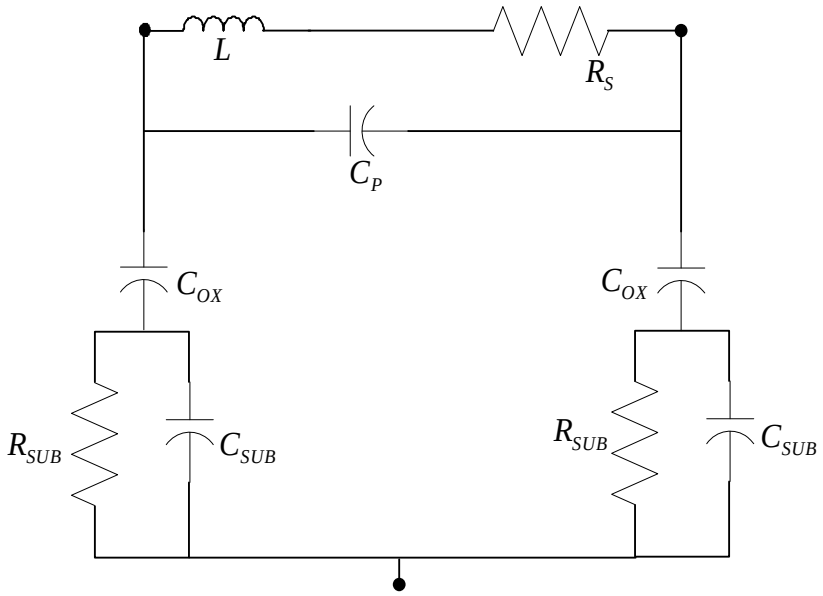

Figure 4.3 π model of the inductor.

L is the series inductance and R_s characterizes the series resistance of the metal caused by finite conductivity, skin effects and current crowding. C_P is the capacitive coupling between turns of the inductor and C_{OX} is the capacitance between the metal and the substrate. R_{SUB} and C_{SUB} model the ohmic losses and capacitance in the substrate. The purpose of modeling an inductor is to determine how the quality factor changes with frequency. The inductance L which is the main property of the inductor is determined by the magnetic field induced when an alternating current flows through the metal layer. The amount of the magnetic energy stored is determined by the magnetic flux density of the induced magnetic field. However, part of the transmitted energy is energy lost as heat caused by the resistance in the metal layer R_s. The substrate also presents a major loss mechanism. The electrical energy stored in the inductor is coupled to the substrate through the capacitor C_{OX}. The changing magnetic field of the inductor also induces an

alternating current in the substrate in the opposite direction, which reduces the effective inductance and increases the effective series resistance. To overcome these loss mechanisms modern fabrication processes provide five to six metal layers with thick top metal layers for inductors. Placing an insulating shield beneath the inductor has been shown to reduce the substrate losses and improve the quality factor [27, 28].

4.1.2 Frequency and tuning range

The frequency of oscillation can be varied by varying the capacitance C_P in the tank of figure 4.2. Typically varactors are implemented using junction diodes or MOS transistors. Typical capacitance characteristics of these varactors are shown in figure 4.4 below.

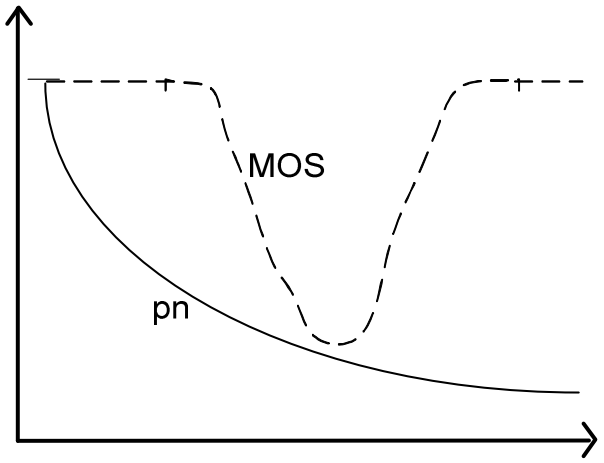

Figure 4.4 C-V characteristics of junction diode and MOS varactors.

The ratio maximal to minimal capacitance is an important parameter while designing an oscillator. The tank capacitance C_P consists of the varactor capacitance C_{var} and parasitic capacitance C_{par}. The varactor capacitance can be varied by a DC voltage

applied across it. The Q of a varactor is also an important part of the resonator and for MOS varactors Q improves with technology scaling [29, 30]. Technology scaling however brings in other design constraints like reduced power supply and break down voltages. This also deteriorates the ratio of maximal to minimal capacitance provided by the varactor and the linearity of the capacitance versus voltage curve (C-V curve) of the varactor.

At low supply voltages one of the methods to improve the tuning range and overcome the non linearity of the C-V curve is to digitally control the varactor. This technique along with its design complications are discussed in a future chapter.

4.1.3 Power dissipation

The power dissipation in an oscillator is largely influenced by Q of the resonator and the amplitude of the output swing required. The output swing is proportional to the impedance offered by the tank and the current generated by the bias circuitry of the oscillator. The output swing is also determined by the topology of the oscillator and its amplitude limiting mechanism. This also has strong implications for the phase noise performance of the oscillator as will be discussed later. In general, it is desirable to have large amplitude of oscillation to completely switch the LO inputs of up/down conversion mixer and dividers. In practical designs oscillators are designed to provide a swing between half and rail to rail. Current needed to generate such amplitude is largely influenced by the Q of the resonator and the topology of the oscillator.

4.1.4 Phase

Many modern transceiver architectures require quadrature signals, while some requiring more than two phases. Oscillators can provide single phase or multiphase outputs. There are many ways of generating multiple phase outputs. Multiple phase outputs are inherently available in ring oscillators but have poor phase noise performance. LC oscillators have superior phase noise performance compared to ring oscillators. If accurate multiphase signals with low phase noise are required then LC oscillators are the best option for a given transceiver design. Theory and circuits for the design of multiphase LC oscillators are discussed in the next chapter.

4.1.5 Phase noise

Practical oscillators have passive and active devices that generate noise. This noise can be viewed as an essential component as it serves as the input for the oscillator. In an ideal oscillator the noise is shaped and amplified at the resonance frequency ω_o to generate a periodic signal. However, in a practical oscillator the noise power close to the resonance frequency is also amplified by the loop gain of the oscillator and the output signal spectrum has its power distributed around the resonance frequency ω_o in addition to the power located at the harmonic frequencies. This undesired shaping and amplification of noise around the resonance frequency is called phase noise.

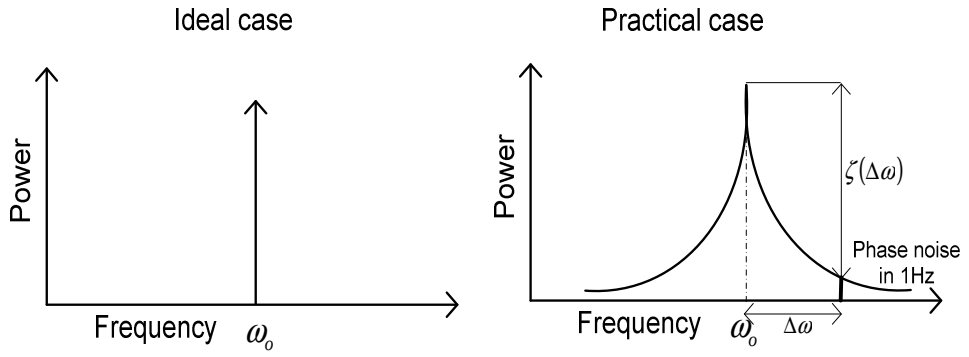

Figure 4.5 Phase noise in practical oscillators.

Phase noise $\zeta(\Delta\omega)$ is expressed as the ratio of the signal power at a particular offset frequency $\Delta\omega$ from the oscillation frequency ω_o to the signal power at the oscillation frequency.

$$\zeta(\Delta\omega) = 10\log\left[\frac{P(\omega_o + \Delta\omega)}{P(\omega_o)}\right] \tag{4.7}$$

where $P(\omega_o + \Delta\omega)$ is measured in a 1 Hz bandwidth.

4.2 Review of phase noise models

Modeling phase noise in oscillators has been a subject of theoretical and experimental research for a long time. Phase noise models can be broadly classified under time variant and time invariant models. An oscillator spectrum has phase noise side bands with three major regions as shown in figure 4.6.

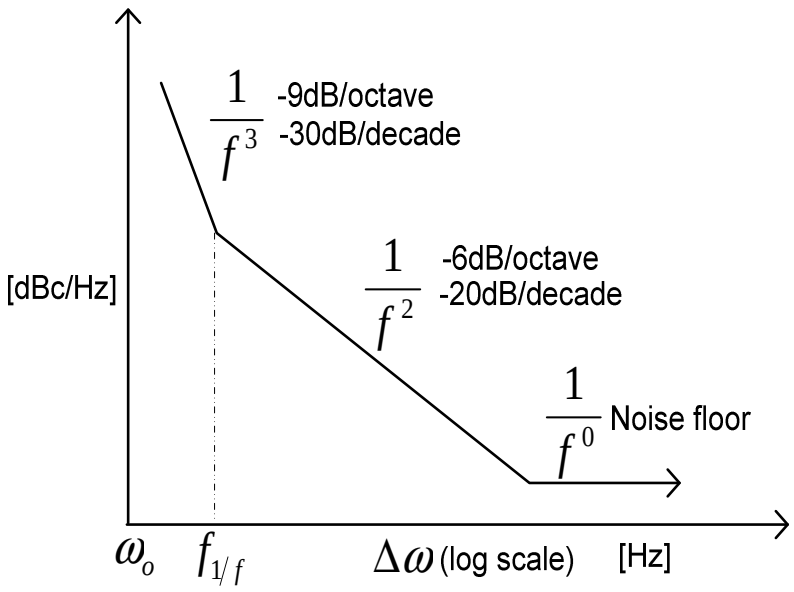

Figure 4.6 Phase noise spectrum.

The dominant part of the phase noise plot is the $\frac{1}{f^2}$ region with slope of -6 dB/octave and results from the noise shaping of the noise sources in the oscillator. This region starts at $1/f$ noise corner frequency $f_{1/f}$ and continues till the noise floor. The $\frac{1}{f^3}$ region is due to the up converted $1/f$ noise of the devices in to phase noise and has a slope of -9 dB/octave that continues till $f_{1/f}$ [31].

4.2.1 Leeson's phase noise model [32]

One of the early phase noise models for oscillators was given by Leeson in 1966 [32]. The semi empirical equation set up by Leeson for thermally induced phase noise is given by the equation 4.8.

$$\zeta(\Delta\omega) = 10\log\frac{2FKT}{P_{sig}}\underbrace{\left[1+\left(\frac{\omega_o}{2Q\Delta\omega}\right)^2\right]}_{1/f^2}\underbrace{\left(1+\frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)}_{1/f^3} \tag{4.8}$$

Where K is Boltzmann constant, T is the absolute temperature, P_{sig} is the signal power, Q is tank quality factor, ω_o is the signal frequency and $\Delta\omega$ is the frequency offset. F is an unspecified noise "fit" factor that depends on the oscillator topology. $\Delta\omega_{1/f^3}$ is the flicker noise corner frequency between the regions $\frac{1}{f^3}$ and $\frac{1}{f^2}$ shown as $f_{1/f}$ in the phase noise plot. The above equation shows two important ways to reduce phase noise. First is to increase the signal power or the oscillation amplitude. For practical oscillators the maximum allowable amplitude is limited by the power supply voltage or the break down voltage of the devices. The other more effective way is to increase the tank quality factor Q. Leeson's formulae includes many properties of real oscillators like the -6 dB per octave region of the phase noise. -9 dB per octave region of the phase noise is described empirically but no insight is provided into the flicker noise up conversion. Leeson's model is a linear time invariant model. In practice, bias conditions vary significantly as the oscillator works in a nonlinear mode and many nonlinear phase noise generation mechanisms are added to the total phase noise.

4.2.2 Rael and Abidi phase noise model [33]

Rael and Abidi [33] proposed a nonlinear time invariant approach to the analysis of phase noise of cross-coupled LC oscillators. This model takes into account the resonator

noise, tail current noise and the noise of the switching differential pair. In the analysis they model the switching differential pair as a mixer [34] to explain the up conversion and down conversion of noise from the tank and active devices into phase noise. The cross-coupled differential pair is treated like a mixing pair that down converts the noise from the harmonics and up converts the white noise sources from tank and active devices to contribute to the phase noise at the fundamental. This analysis leads to Leeson's like formulae for the thermally induced phase noise which is given by

$$\zeta(\Delta\omega) = F\frac{4kTR_P}{V_o^2}\left(\frac{\omega_o}{2Q\Delta\omega}\right)^2 \tag{4.9}$$

where F is the noise factor and is given by

$$F = 2 + \frac{8\gamma R_P I_{bias}}{\pi V_o} + \frac{8}{9}\gamma g_{mbias} R_P \tag{4.10}$$

where R_P is the parallel resistor representing the loss of the resonator, V_o is the peak voltage across the resonator, g_{mbias} is the transconductance of the tail current source and γ is the thermal noise factor of the MOSFET which is typically $2/3$. The first term in the noise factor F arises from the resonator (it is an integer because the total noise has been normalized to the noise from the resonator), the second term arising from the switching differential pair and the third term comes from the transistor used to provide the tail current. At low bias currents the output voltage V_o is solely determined by the magnitude of the tail current and R_P and is given by $(4/\pi)R_P I_{bias}$. In this region of operation, known as current limited region V_o increases with I_{bias} and phase noise improves with V_o^2 as shown by equation 4.9. After V_o is clipped to its maximum value due to any amplitude

limiting mechanisms the oscillator enters voltage limited region and further increase in the bias current I_{bias} does not increase the output amplitude thereby increasing the noise factor F (equation 4.10) and degrading the phase noise. Assuming that the oscillator is operating in current limited region and it is biased with an ideal noise less current source, the noise factor F reaches its theoretical minimum value given by $(2+2\gamma)$. Also this theory revealed an interesting fact that the noise factor F is independent of transistor size or the transconductance of the cross-coupled pair. Besides arriving at the same conclusions implied by Leeson's model regarding phase noise improvement, this theory also provides important design insights between active device dimensions and the noise factor F and also shows the importance of operating the oscillator, in a current limited regime rather than a voltage limited regime.

4.2.3 Hajmiri's phase noise model [38-40]

The main difference between the previous models and this model is that it is time varying in nature. It also assumes a linear relation as far as noise to phase noise transfer function is concerned. The basic idea behind this theory is that the noise sources injecting charge in to the tank have different impact on the out put phase depending on the instant of the output time period. This is characterized by the Impulse Sensitivity Function ISF (Γ) which measures the phase sensitivity of each point of the output wave form when injected by small current impulse as shown in the figure 4.7.

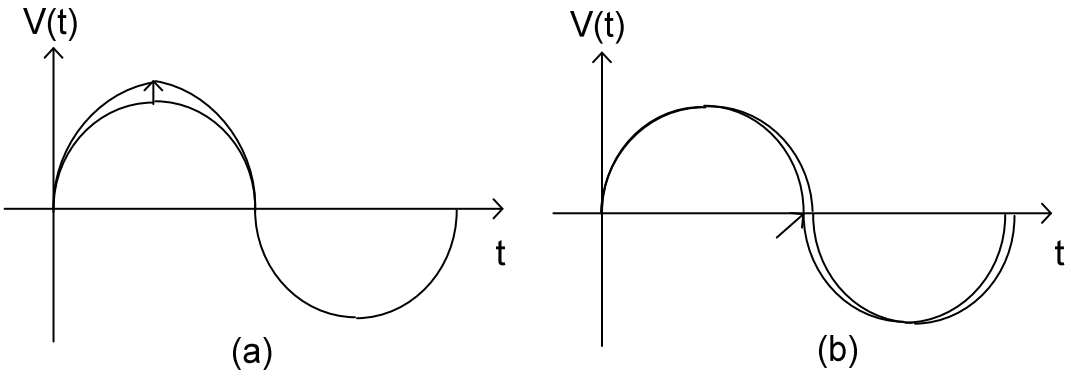

Figure 4.7 (a) minimum ISF (Γ) (b) maximum ISF (Γ).

Prediction of phase noise using this theory consists of two steps. First is to estimate the phase shift $\Delta\phi$ occurring at the oscillation node when a current impulse is injected.

$$\Delta\phi = \Gamma(\omega t)\frac{\Delta V}{V} = \Gamma(\omega t)\frac{\Delta q}{q} \tag{4.11}$$

where ΔV and Δq are the voltage variation and charge variation on an oscillation node with initial voltage V and charge q. Γ is the impulse sensitivity function. It is frequency independent, amplitude independent, dimension less quantity and has time period of 2π. The second is to include the cyclo-stationary properties of noise sources. This is done by multiplying $\Gamma(\omega t)$ with $\alpha(\omega t)$.

$$\Gamma_{eff}(\omega t) = \Gamma(\omega t)\alpha(\omega t) \tag{4.12}$$

where $\alpha(\omega t)$ is a dimensionless periodic quantity with maximum value of unity. Analyzing the impact of noise sources over a time period gives the phase noise expression as

$$\zeta(\Delta\omega) = \frac{1}{8\pi^2 f_m^2}\cdot\frac{1}{q_{\max}^2}\cdot\sum_n \overline{i_n^2}\Gamma_{rms,n}^2 \tag{4.13}$$

where Γ_{rms} is the RMS value of Γ_{eff} and can be calculated by the equation 4.14.

$$\Gamma_{rms}^2 = \frac{1}{2\pi}\int_0^{2\pi} \Gamma_{eff}^2(x)dx \tag{4.14}$$

Accurate determination of Γ_{rms}^2 is necessary for accurate prediction of phase noise in this model. For design and trade off purposes this model is not very useful as the determination of Γ_{rms} is a time consuming process requiring many transient simulations on a circuit simulator. The advent of RF simulators like Spectre has displaced ISF as a simulation tool. An important aspect of this theory is its ability to predict the $f_{1/f}$ corner frequency of the oscillator given the $f_{1/f}$ frequency of the devices. Although a time varying theory is needed to predict the oscillator phase noise accurately, many design insights that have been provided by phase noise theories [35-40] using time varying aspects, have been explained by using the time invariant models proposed by Abidi and Leeson with reasonable accuracy between phase noise values obtained by time invariant modeling and measurements.

4.3 A 25 GHz oscillator in SiGe BiCMOS technology

A microwave integrated LC VCO has been designed in IBM BiCMOS 8HP technology. High Q inductors and varactors are essential at this frequency for reliable start up and low phase noise. At this frequency previously discussed issues namely skin effect and current crowding reduces the self resonant frequency and quality factor of the inductor. The above losses become more significant as the frequency increases. The losses due to skin effect are proportional to $\sqrt{f}$, the conductance of the parasitic

capacitors also increases with f, the quality factor of the inductor given by $Q = R_{sub}/L\omega$ also reduces with frequency. The varactor has a Q of around 70 and the overall resonator Q is mainly limited by the inductor. To address these problems IBM SiGe technology offers transmission line inductors with thick metallization made of aluminum with two options: (i) a mesh of deep trench isolation under the inductor metal layer to isolate the inductor from the substrate and increase R_{sub} (ii) a metallic mesh placed beneath the inductor that serves to reduce the value of R_{sub}. It can be shown that the lossy power dissipation in the substrate P_{sub} depends on frequency and reaches a maximum when $R_{sub} = (C_{sub}\omega)^{-1}$. Hence at high operating frequency of 25 GHz it is preferable to increase the value of R_{sub} to minimize the loss mandating for deep trench isolation under the transmission line.

The circuit diagram of the oscillator is shown in figure 4.8. The oscillator core consists of cross-coupled transistors Q1 and Q2 to generate a negative resistance of $-2/g_m$. This negative resistance cancels the losses in the resonator and other losses due to the cascaded buffers. The inductors L1 and L2 are implemented as micro strip lines made of top level metal which is aluminum with layer thickness of $4\,\mu m$. The inductors have dimension of $350\,\mu m * 25\,\mu m$ and provide an inductance of 250 pH with a Q of around 10 at 25 GHz. At low frequencies the Q of the inductor is limited primarily due to the resistance of the metal layer, at high frequencies, Q degradation is dominated by the loss mechanisms caused by the substrate [41]. To minimize the Q dependence on the substrate resistivity, the tank was placed on top of a lattice of high resistance deep trench isolation to minimize the current injected into the substrate. The varactors used are hyper

abrupt junction varactors provided in the design kit and have a capacitance of 115 fF in the design. The base of the transistors Q1 and Q2 are biased from an external source. DC block capacitors are placed between the base and the collectors to prevent the transistors from entering in to deep saturation. The output buffers are terminated with 50 ohm external resistors. The phase noise was measured using the phase noise utility software in the Agilent 8563EC spectrum analyzer. The oscillator core consumes 10 mA current and the buffers consume 8.8 mA current from a 3.3 V supply. The measured phase noise is around -83 dBc/Hz at 500 KHz offset from 25 GHz carrier. The oscillation frequency can be tuned from 23.8 GHz to 26.3 GHz. Table 4.1 summarizes the oscillator performance. Figure 4.9 shows the fabricated die and figures 4.10 and 4.11 show the phase noise plots of the oscillator.

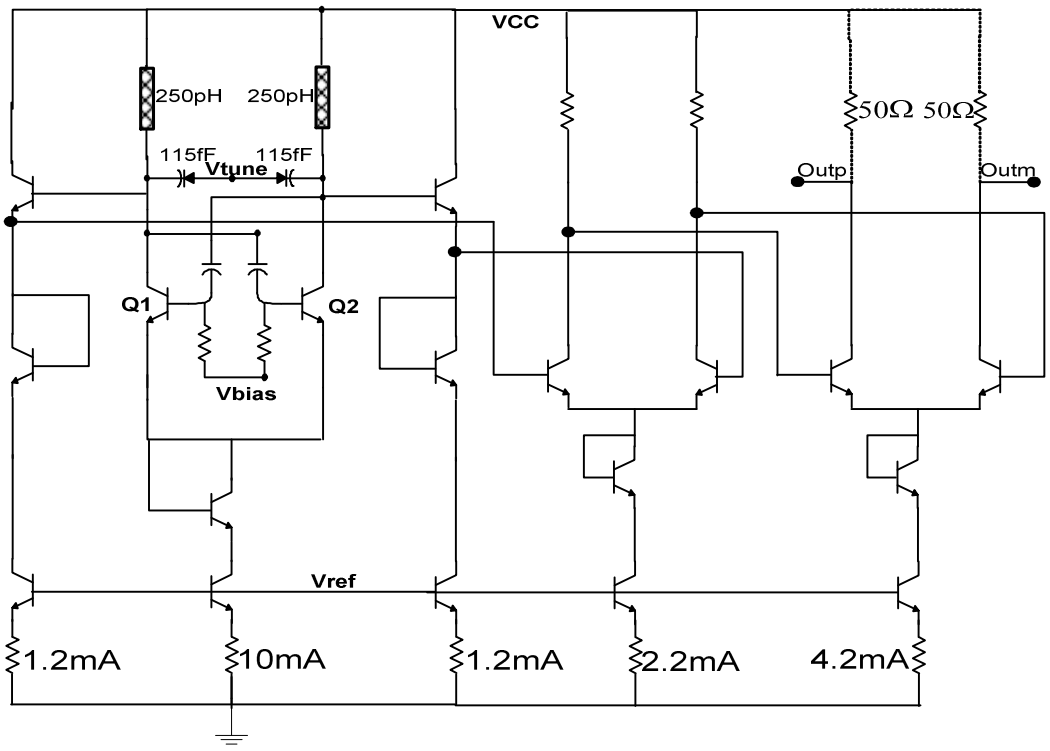

Figure 4.8 25 GHz oscillator circuit diagram.

Supply voltage	3.3 V
Oscillation frequency	25 GHz
Tuning range	10%
Core current	10 mA
Buffer current	8.8 mA
Phase noise @ 500 KHz	-82.5 dBc/Hz
Output power	-30 dBm
Area	560 μm *205 μm
FOM	-162 dBc/Hz

Table 4.1 Measured performance of the 25 GHz Oscillator.

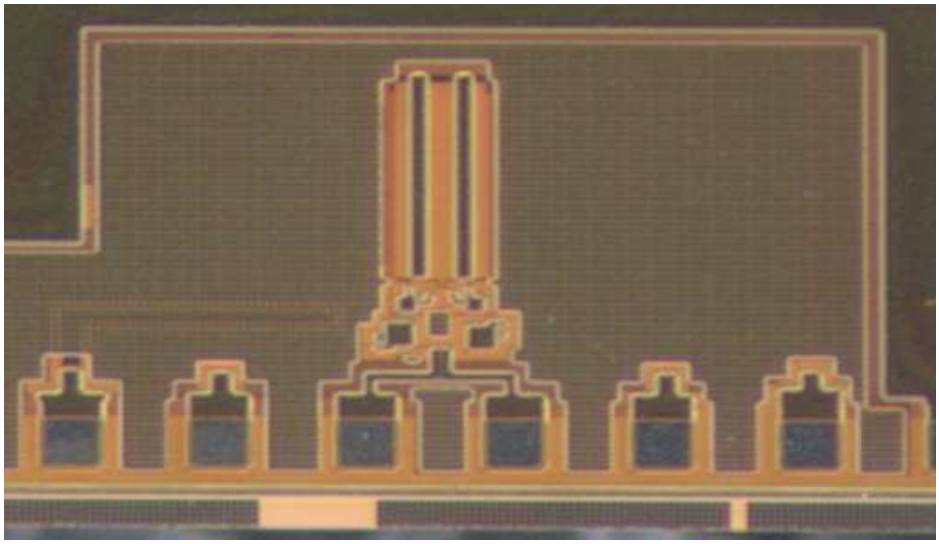

Figure 4.9 25 GHz oscillator die photo.

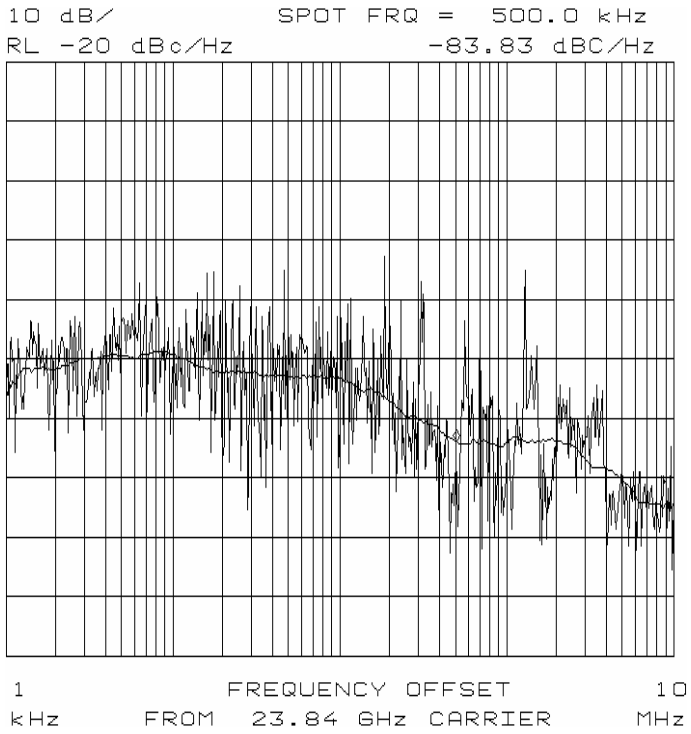

Figure 4.10 Oscillator phase noise plot from 23.8 GHz carrier.

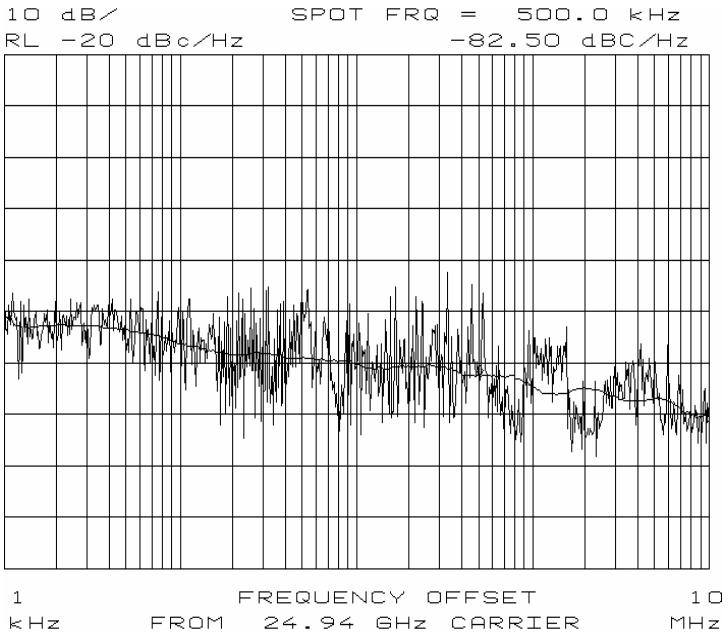

Figure 4.11 Oscillator phase noise plot from 25 GHz carrier.

4.4 A 1.5 GHz cryogenic oscillator in SiGe BiCMOS technology

A 1.5 GHz oscillator was designed in SiGe BiCMOS process. It consists of cross-coupled negative transconductance pair (Q1-Q2) and LC tank. In order for the oscillation to occur, the VCO has to satisfy the following oscillation condition:

$$g_{m,osc} \geq \frac{\chi}{R_{\tan k}} \tag{4.15}$$

where $R_{\tan k}$ is the effective resistance (loss) of the tank and χ is an empirical parameter with value from three to five to provide design margin for reliable VCO startup.

The tank consists of 5 nH inductors and junction diode varactors. The simulated Q is around 18 at room temperature and 1.5 GHz. The oscillator output is fed in to a chain of CML dividers which divides the signal by 64 to generate a 20 MHz output.

The die shown in figure 4.12 has been wire-bonded in a 40 pin DIP package and tested in a cryogenic chamber. Figure 4.13 shows the oscillator output spectrum at 1.4 GHz. The output power delivered to a 50 ohm load is -12 dBm. Figure 4.14 shows the output of the dividers which divide the oscillator output by 64 to generate 22 MHz output. The oscillation frequency versus temperature is shown in figure 4.15, the oscillation frequency increases with decreasing temperature. The measured phase noise at 1 MHz offset is around -124 dBc/Hz from 22 MHz carrier. The die consumes 3 mm^2 of area.

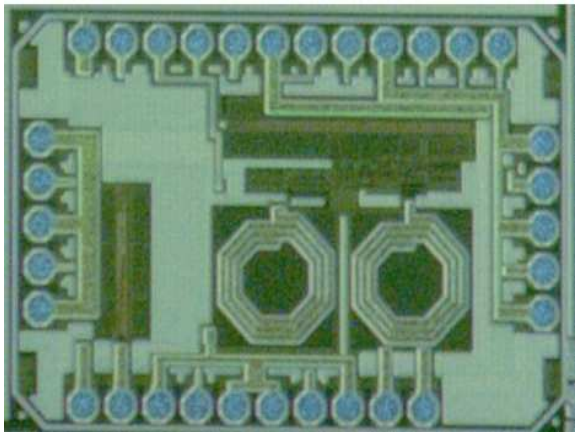

Figure 4.12 Die photo of the 1.5 GHz oscillator.

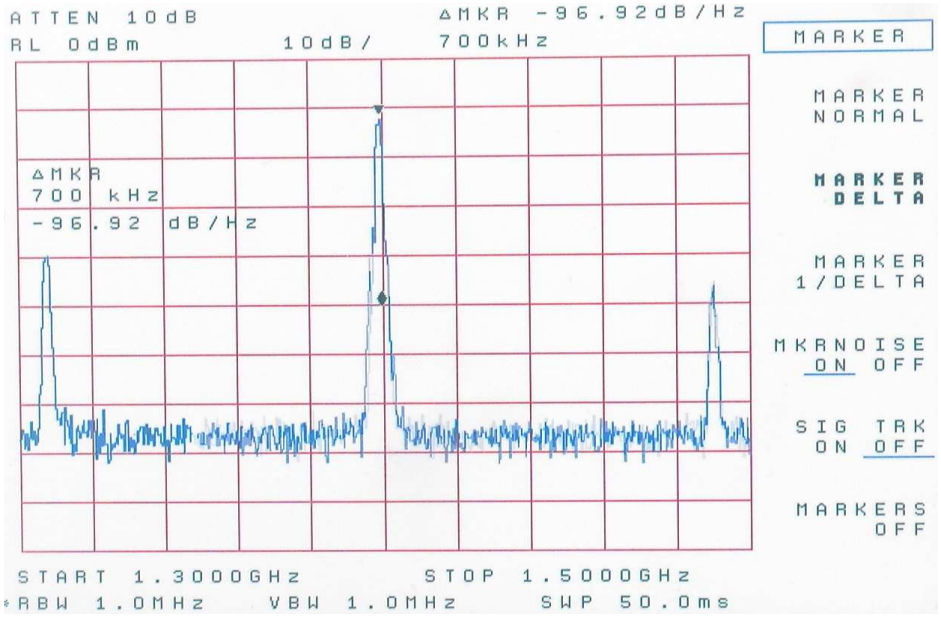

Figure 4.13 Output frequency at room temperature is 1.4 GHz, tuning voltage is 3 V.

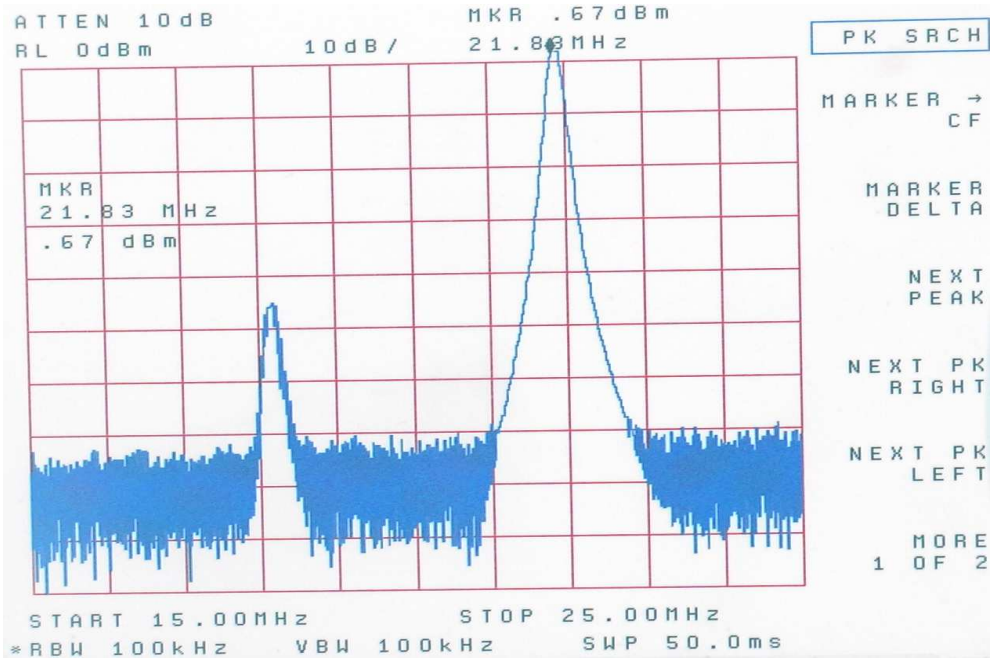

Figure 4.14 Output frequency of divide-by-64 is 21.88 MHz.

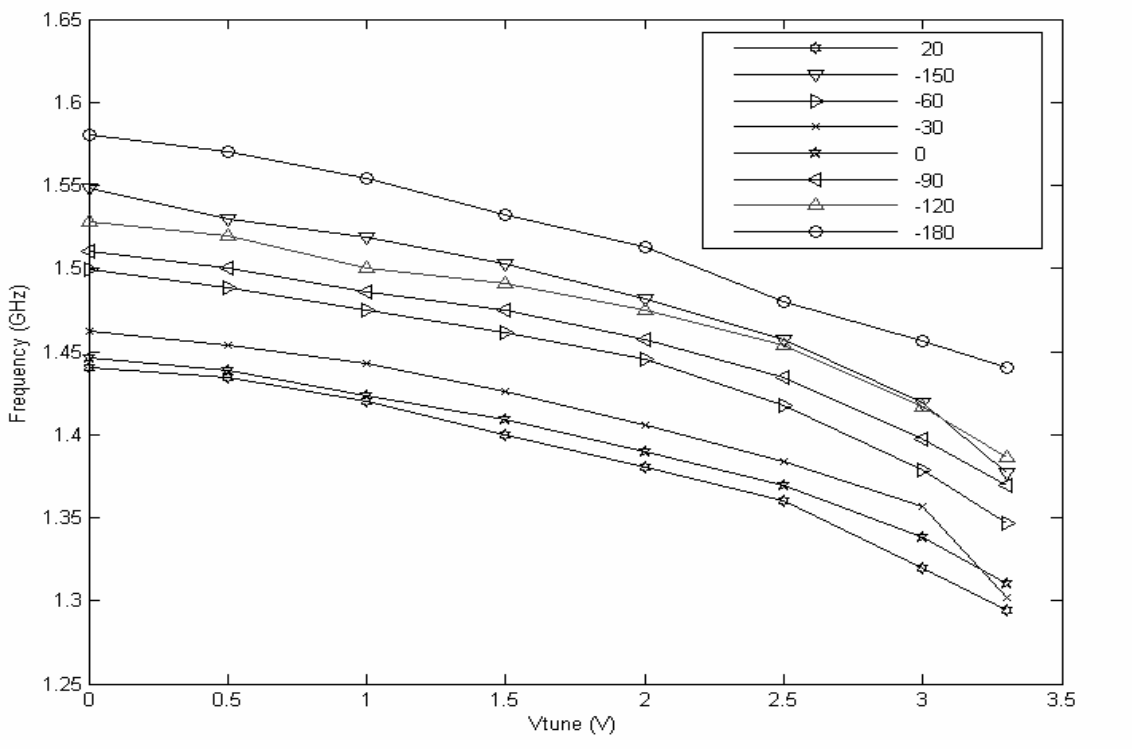

Figure 4.15 Frequency versus tuning voltage at different temperatures.

Supply voltage	3.3 V
Core current at 180° C	6 mA
Oscillation frequency	1.42 – 1.58 GHz
Divider range	22.5-24.6 MHz
Phase noise @ 1 MHz	-125 dBc/Hz
FOM	-139 dBc/Hz
Output power	-12 dBm

Table 4.2 Measured performance of the 1.5 GHz Oscillator.

4.5 Conclusions

This chapter presented basic design theory of oscillators and review of popular phase noise models followed by design of two single phase oscillator designs operating at high speed of 25 GHz and 1.5 GHz and their measured results.

Chapter 5: Multiple Phase LC Oscillators

5.1 Introduction

Many modern transceiver architectures require multiphase signals. Figure 5.1 shows direct conversion receiver architecture where the signal from the antenna is fed to quadrature mixer and directly down converted followed by low pass filter.

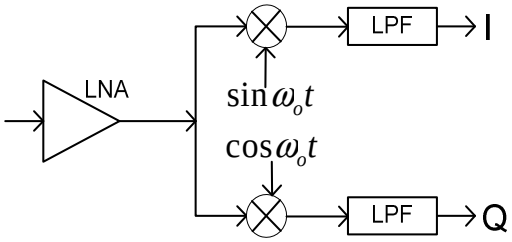

Figure 5.1 Direct conversion receiver architecture.

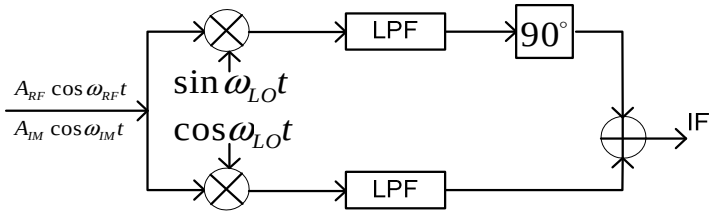

Figure 5.2 Image reject receiver architecture.

While implementing phase and frequency modulations the direct conversion receiver must have quadrature mixing. This is facilitated by quadrature LO signals generated from the oscillator. Phase and amplitude errors between the quadrature signals set the acceptable bit error rate by corrupting the down converted signal constellation. In the image reject receiver shown in figure 5.2 the problem of image suppression is tackled through signal manipulation unlike filtering technique in heterodyne architectures. There are mainly two types of image reject receiver architectures namely Hartley (figure 5.2) and Weaver. In this architecture, perfect canceling of the image requires perfect quadrature signals. Phase mismatches in the quadrature signals results in incomplete cancellation of the image and corrupts the down converted signal, which is not entirely avoidable in reality. The ratio of down converted desired signal to the down converted image signal is denoted by Image Rejection Ratio (IRR). A formula to calculate the IRR for a given phase and amplitude mismatches of quadrature signals is given in [57].

There are various ways to generate quadrature signals: (i) a divide-by-two frequency divider following the VCO running at the double the LO frequency. This approach generally shows poor phase noise and quadrature accuracy, as it requires 50% duty cycle VCO. (ii) A VCO followed by a passive polyphase RC complex filter. An integrated polyphase network is narrowband with poor quadrature accuracy. It suffers from process variation on the RC time constants that lead to amplitude imbalance between the quadrature signals. A typical RC phase filter also loads the VCO and has large loss, such that, a power hungry buffer is needed after the filter. (iii) Two oscillators are forced to run in quadrature using transistor or transformer coupling. This technique provides

wideband quadrature accuracy and superior phase noise performance with tradeoff of increased power and silicon area.

By coupling two symmetric LC tank oscillators to each other, a quadrature VCO (QVCO) generates wideband quadrature signals at high frequency. There are various ways to couple the two oscillators and inject-lock their oscillation frequency. The most common QVCO topology shown in figure 5.3 which is the parallel coupled topology, proposed by Rofougaran et al. [42], where each oscillator consists of a cross-coupled feedback circuit and each oscillator output is connected to another oscillator using transistors in parallel to the cross-coupled transistors. The Parallel QVCO (P-QVCO) delivers quadrature signals with low phase and amplitude errors, yet it consumes large current to bias both the oscillation and coupling transistors.

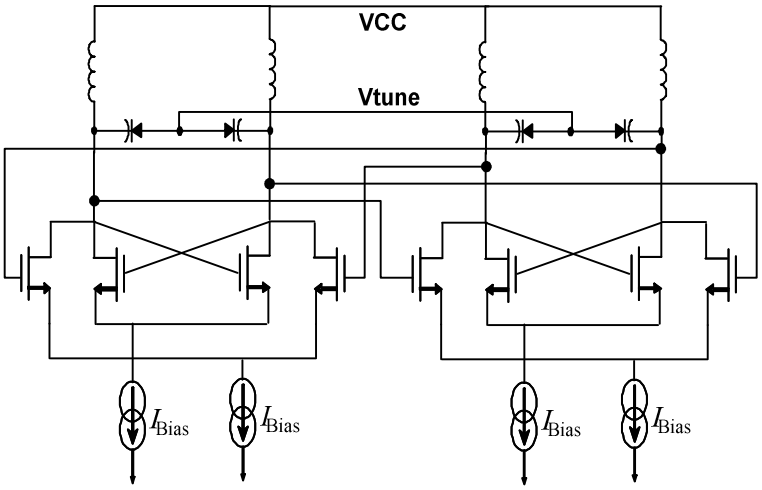

Figure 5.3 Parallel coupled quadrature oscillator.

Oscillators can also be serially coupled by placing the coupling transistors in series with the oscillation transistors [43]. By connecting the coupling transistors in series in a cascode current reuse topology, the Serial QVCO (S-QVCO) reduces the noise from the

cascode devices and provides better isolation between the VCO outputs and its current sources. The two QVCO topologies have been compared in [44]. For the pure MOSFET S-QVCO, the coupling transistors should be about five times larger than the oscillation transistors for good phase noise. For optimal coupling, the P-QVCO appears to have better quadrature amplitude and phase matching. However, under optimal coupling, the S-QVCO achieves better phase noise. In the P-QVCO and S-QVCO reported so far, the same types of transistors have been used for oscillation and coupling.

5.2 A 5 GHz low power series coupled BiCMOS quadrature VCO with wide tuning range

This design [58] presents a QVCO implemented in a 47 GHz SiGe technology. The proposed QVCO is a serially coupled LC VCO that utilizes SiGe HBTs for oscillation and MOSFETs for coupling. The oscillation NPN transistors achieve high oscillation frequency and low phase noise, while the NMOS coupling transistors provide more headroom, better isolation and increased tuning range.

The S-QVCO circuit is illustrated in figure 5.4, in which the NPN transistors Q1 and Q2 form a cross-coupled negative transconductance LC VCO and Q3 and Q4 form another identical LC VCO. The coupling between the two oscillators is realized using four NMOS transistors M1, M2, M3 and M4. Thus, S-QVCO utilizes different types of transistors for oscillation and coupling. The advantages of this technique will be discussed in the coming paragraphs.

Compared to a P-QVCO, the S-QVCO achieves lower current consumption, since the coupling and oscillation transistors share the same bias current. In a P-QVCO, the

coupling pair of transistors usually consumes an additional 25% to 30% of the core oscillator current for reasonable compromise between phase noise and phase error. In an S-QVCO, the coupling transistors are in series with the $-g_m$ transistors. Additional current sources are not required for coupling transistors, resulting in considerable power saving. Also, the coupling and oscillation transistors are connected in a cascode manner such that the noise coming from the coupling transistors and current sources are isolated. The phase noise and phase error are relatively independent of each other in this topology. However, under the same voltage supply, the S-QVCO has less voltage headroom for output swing due to the coupling transistors.

Previously, the same types of transistors were used in the S-QVCO topology. As known, NPN transistors can achieve higher oscillation frequency due to enhanced $f_{\max}$ of the transistor. On the other hand, NMOS transistors have higher output impedance, reduced voltage headroom, and much relaxed bias requirements compared to their Bipolar Junction Transistors (BJT) counterparts. Since both types of transistors are available in a BiCMOS technology, the advantages of both types can be combined to achieve better QVCO performance.

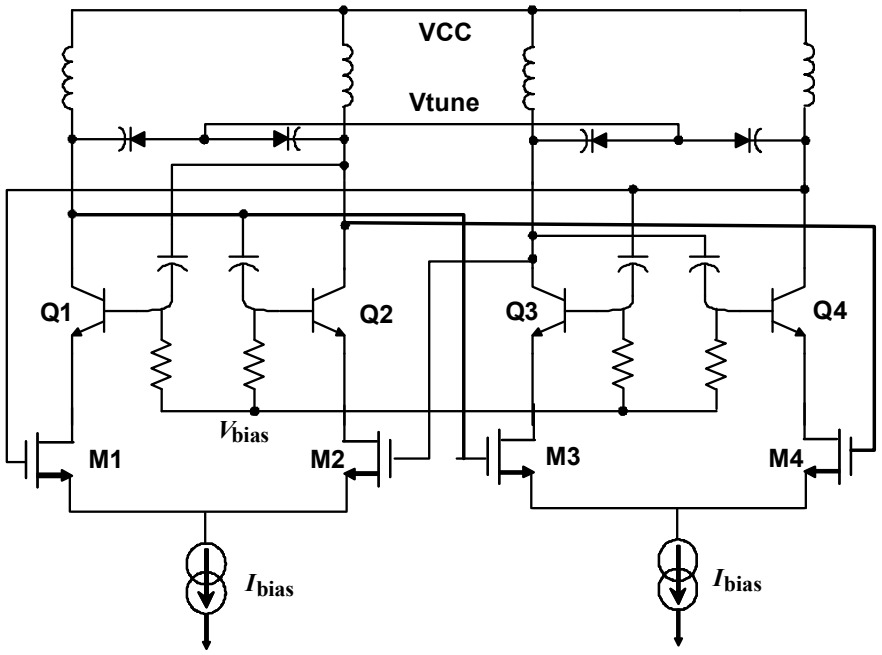

Figure 5.4 Proposed S-QVCO circuit schematic using NPN for oscillation and NMOS for coupling.

By using NPN transistors for oscillation, high oscillation frequency can be achieved and by using MOS transistors for coupling, higher voltage headroom can be provided for output swing due to the reduced headroom required by the MOS transistors. Moreover, better isolation between the current source and oscillation tank can be achieved due to the large output impedance of the MOS transistors. In the proposed S-QVCO, the MOS coupling transistors are directly connected to the VCO output nodes, providing a much easier biasing scheme.

In the S-QVCO design, the NPN transistor size is chosen for maximum speed and the bias current is selected to provide the transconductance of

$$g_{m,osc} \geq \frac{\chi}{R_{\tan k}} \tag{5.1}$$

where $R_{\tan k}$ is the effective resistance (loss) of the tank and χ is an empirical parameter with value from three to five to provide design margin for reliable VCO startup. The oscillation frequency is given by $f_{osc} = \left(2\pi\sqrt{LC_v}\right)^{-1}$, where C_v is the capacitance of the varactors. The frequency tuning range can be found as

$$FTR = \frac{C_p + C_{v\max}}{C_p + C_{v\min}} \tag{5.2}$$

where C_P is the fixed capacitance seen across the tank. This fixed capacitance is made up of the parasitic capacitance of the inductor, varactor, capacitance contributed by the coupling transistors and oscillating transistors. At high frequencies this fixed capacitance can contribute in a large portion to the overall capacitance and limit the tuning range and maximum attainable oscillation frequency. To first order the fixed capacitance provided by the oscillating transistor for the P-QVCO is $\frac{C_\pi}{2} + 2C_\mu$ for the bipolar version and $\frac{C_{gs}}{2} + 2C_{gd}$ for the MOS version.

The total fixed capacitance seen across the LC tank for S-QVCO and P-QVCO shown in figure 5.4 and figure 5.3 are given by:

$$C_p = 2C_\mu + \frac{C_{gs}}{2} + \frac{C_\pi C_{gd} C_{gs}}{2(C_\pi C_{gd} + C_\pi C_{gs} + C_{gs} C_{gd})} \tag{5.3}$$

$$C_p = 2C_{gd} + C_{gs} + \frac{1}{2}\left(\frac{C_{gd} C_{gs}}{C_{gd} + C_{gs}}\right) \tag{5.4}$$

As can be seen from the above equations the use of MOS transistors for coupling in serial fashion reduces the fixed parasitic capacitance seen across the tank due to the

increased capacitive degeneration (C_{gs} and C_{gd}) at the emitter terminals of the $-g_m$ pairs. This enables more tuning range and maximum attainable oscillation frequency. At high frequencies where the influence of parasitics becomes dominant the S-QVCO should be a better topology for quadrature signal generation compared to the P-QVCO.

The NMOS coupling transistors are sized such that, they provide about the same g_m as that of the NPN transistors. This balances the load impedance of the tanks, which leads to smaller quadrature phase/amplitude errors and improves the phase noise as well. While the above argument would also be valid if bipolar transistors are used for coupling instead of MOS, the fully bipolar version would require current consuming level shifters and the power saving advantage of this current reuse S-QVCO topology compared to P-QVCO would be lost.

The 5 GHz serially coupled quadrature oscillator was implemented in a 47 GHz SiGe BiCMOS technology with four metal layers. The circuit consumes an area of 0.88 mm^2 as shown in figure 5.5. The layout is suboptimal since the long interconnect between the two corner inductors introduces harmful parasitic resistance. The tank uses a pair of on-chip inductors with an inductance of 971 pH and a Q of approximately 12 at 5 GHz. The two varactors are implemented as a collector base diode and exhibit a Q of around 50 at 5 GHz. The VCO core consumes 6 mA of current from 3.3 V supply. As shown in figure 5.6 and 5.7, the quadrature oscillator achieves phase noise of -114.3 dBc/Hz @ 2 MHz offset from 4.65 GHz carrier frequency. The measured oscillation frequency versus the reverse bias voltage across the varactor is given in figure 5.7. The tuning range of the oscillator is from 4.32 to 5 GHz with tuning voltage covering the entire possible range from 0 V to supply voltage. This high tuning range of 15% is due to coupling MOS

transistors in series with $-g_m$ pairs. With the wide tuning range, the oscillator also achieves fairly linear tuning gain (K_{vco}), which is important to avoid VCO chirping and pulling in PLL synthesizer designs. The measured VCO gain is 206 MHz/V. Figure 5.9 shows the measured oscillator phase noise versus the tuning voltage. The maximum variation in phase noise at 2 MHz offset over the entire tuning range is 2.3 dBc/Hz. The VCO achieved better than -113 dBc/Hz phase noise @ 2 MHz offset over the entire tuning range. Table 5.1 summarizes the oscillator performance and table 5.2 compares it to other previous designs. Comparing to other 5 GHz QVCO designs, this P-QVCO design achieves one of the best Figure Of Merit (FOM) defined as $-10\log(L(\Delta f))-10\log\left(\frac{\Delta f^2}{f_{osc}^2}\frac{P_{diss}}{1mW}\right)$. The proposed S-QVCO also achieved the widest tuning range at 5 GHz with low power consumption compared to other LC-tuned QVCO designs. Reference [46] gives a 37% wide tuning range VCO using switch capacitor topology which is intrinsically noisy.

Supply voltage	3.3 V
Core current	6 mA
Oscillation frequency	4.32 – 5 GHz
Tuning range	14.6 %
Phase noise @ 2 MHz	-114.3 dBc/Hz

Table 5.1 Measured performance of the LC-QVCO.

Ref.	[42]	[43]	[45]	[46]	This work
Topology	P-QVCO	CMOS S-QVCO	P-QVCO	P-QVCO	BiCMOS S-QVCO
Frequency (GHz)	0.9	1.8	5	12	5
Tune range	17%	18%	6.4%	37%	14.6%
L (dBc/Hz)	-110	-140	-115	-112	-114.3
Offset	1 MHz	3 MHz	2 MHz	10 MHz	2 MHz
Core power	30 mW	50 mW	21mW	39 mW	19.8 mW
FOM	154	178	169	157	169

Table 5.2 Performance comparison of Quadrature oscillators.

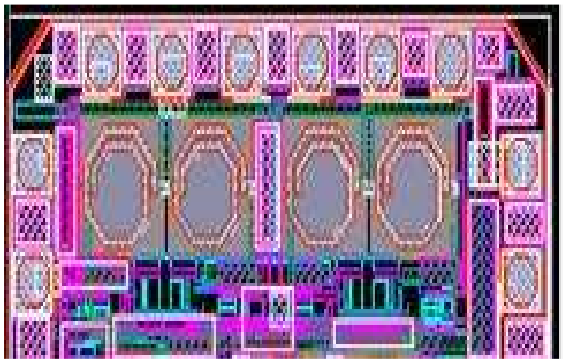

Figure 5.5 Layout diagram of the oscillator.

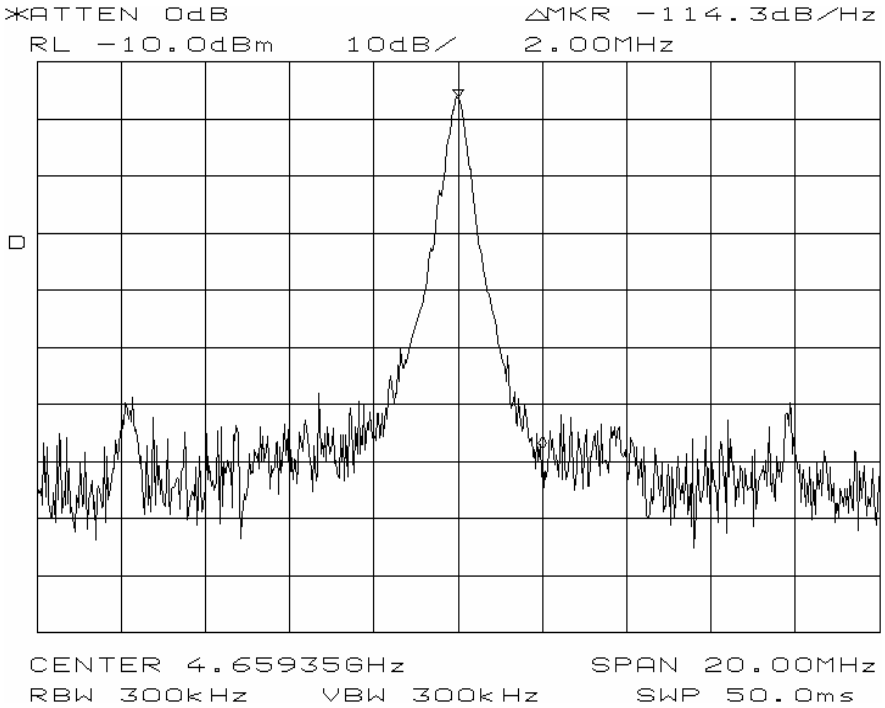

Figure 5.6 Measured QVCO output spectrum.

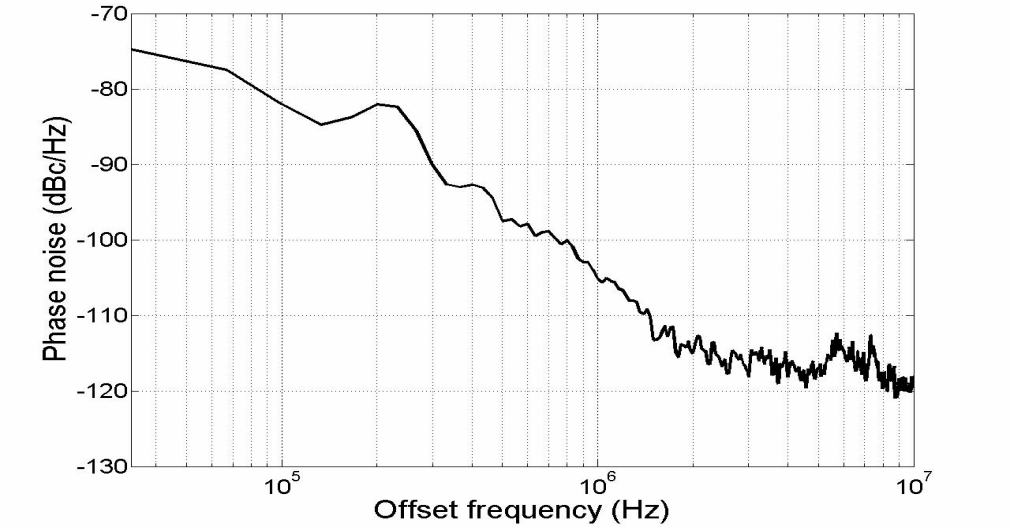

Figure 5.7 Phase noise versus offset frequency.

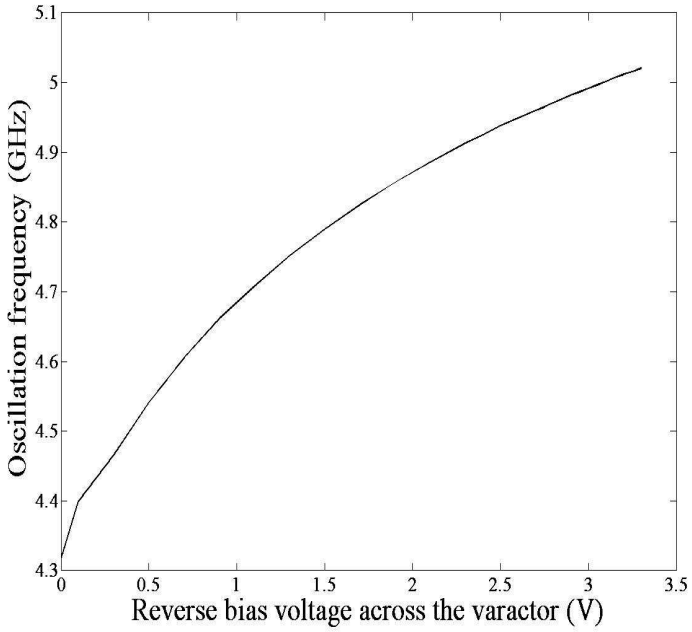

Figure 5.8 Oscillation frequency versus the reverse bias voltage across the varactor.

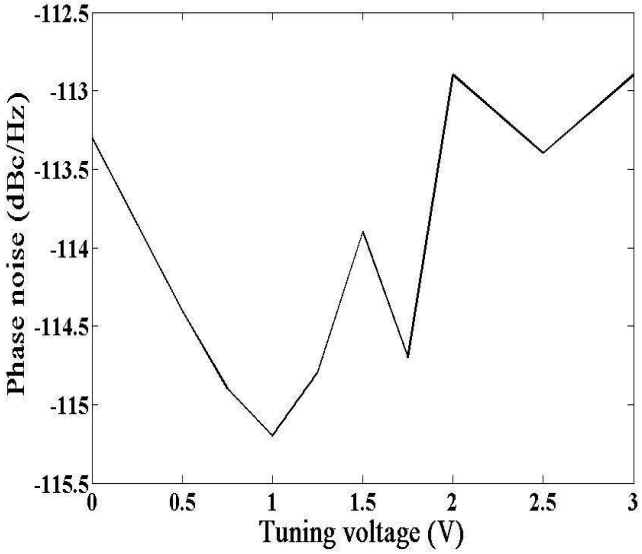

Figure 5.9 Phase Noise versus tuning voltage.

5.3 A 3.5 GHz multiphase oscillator in SOI technology

Silicon On Insulator (SOI) technology provides a promising solution to the ever increasing demand in low power analog integrated circuits fuelled by the growth in emerging wireless and wireline systems. SOI technology gains advantage over the silicon based CMOS due to its excellent RF performance. Compared to conventional bulk CMOS technology, the implementation of a thin isolation layer between the active transistor area and the substrate allows a higher substrate resistivity without degrading the threshold properties of the Field Effect Transistors (FET). As a result, the parasitics of the transistors are reduced, thereby increasing their f_T and $f_{\max}$. SOI provides better device isolation, lower parasitic junction capacitance and increased sub-threshold slope leading to higher speed and lower power consumption for RF circuits. In addition, passive components with higher Q factors and operation frequencies can be achieved. These improvements benefit the RFIC designs.

This design presents a multiphase voltage controlled oscillator design implemented in a 0.18 micron Fully Depleted SOI (FD-SOI) research process. This technology offers two levels of metal interconnects with three metal layers. The challenge for design lies upon the lack of RF models for targeted SOI technology and its devices. The circuit of a single oscillator core with its coupling transistors is shown in figure 5.10. It consists of four parts: an NMOS-PMOS core (Q1-Q4) to generate negative transconductance, coupling transistors to provide a phase shift, current source and LC tank. The transistors Q1-Q4 are sized to set the output DC level of the oscillator at Vcc/2 with equal transconductance

g_m. The single oscillator cores are then connected as a ring oscillator fashion with 180° phase shift between the first and the last core to generate multiphase outputs.

The fabricated SOI oscillator chip was directly wire-bonded to FR4 PCB for measurement. Under supply voltage of 1.5 V, the measured phase noise of the SOI oscillator, as shown in figure 5.12 is -104.7 dBc/Hz at 2 MHz offset from the 3.6 GHz carrier frequency. The oscillator core including its coupling transistors and output buffers consume total power of 22.5 mW per tank and delivers -12 dBm power to a 50 ohm load. Figure 5.13 shows the measured oscillation frequency versus tuning voltage. Table 5.3 summarizes the measured SOI oscillator performance. Figure 5.11 gives the die photo of the SOI VCO chip, occupying an area of 2.16 mm^2.

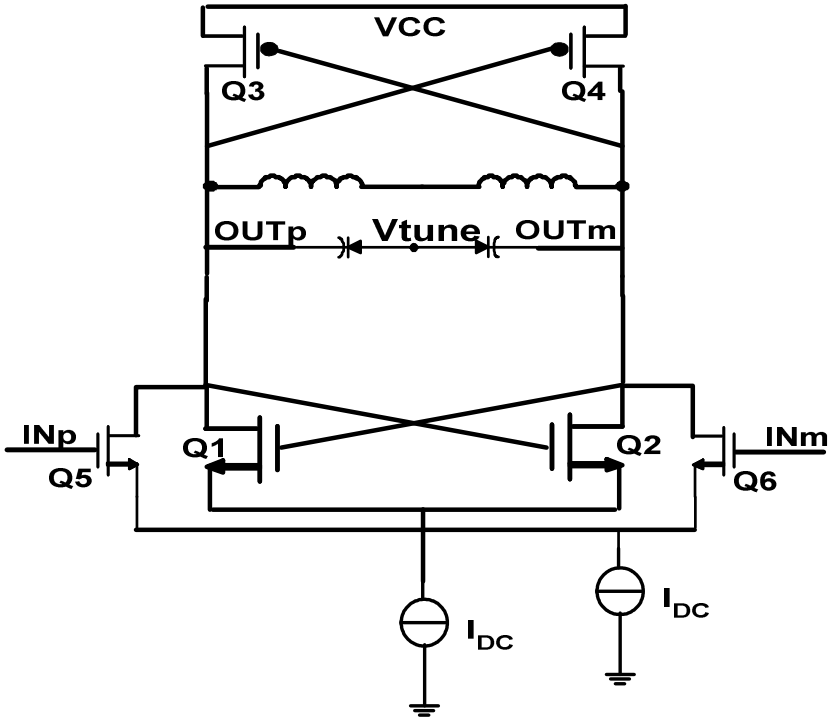

Figure 5.10 Single core of the multiphase oscillator.

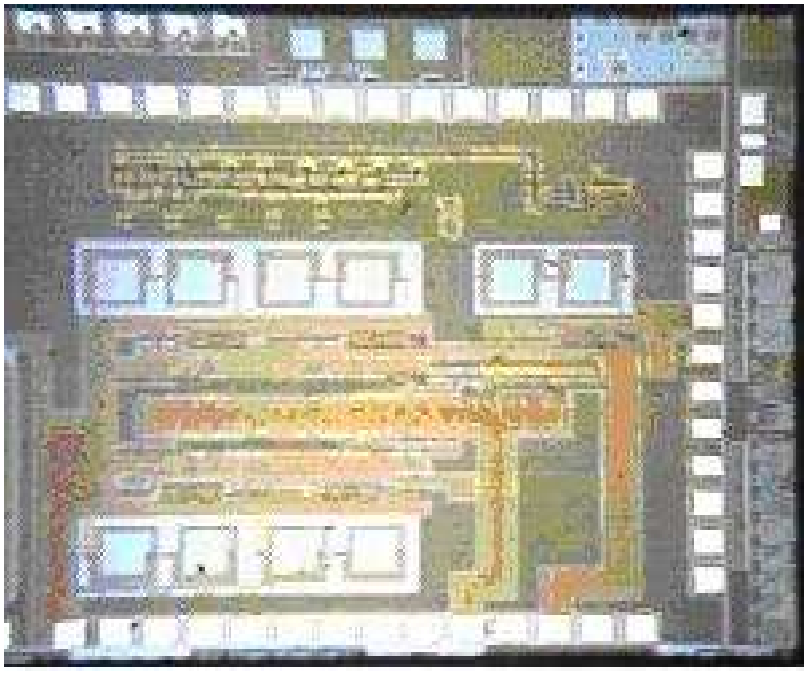

Figure 5.11 Die photo of the oscillator.

Supply voltage	1.5 V
Current	64 mA
Oscillation frequency	3.3 – 3.65 GHz
Tuning range	10 %
Phase noise @ 2 MHz	-104 dBc/Hz

Table 5.3 Measured performance.

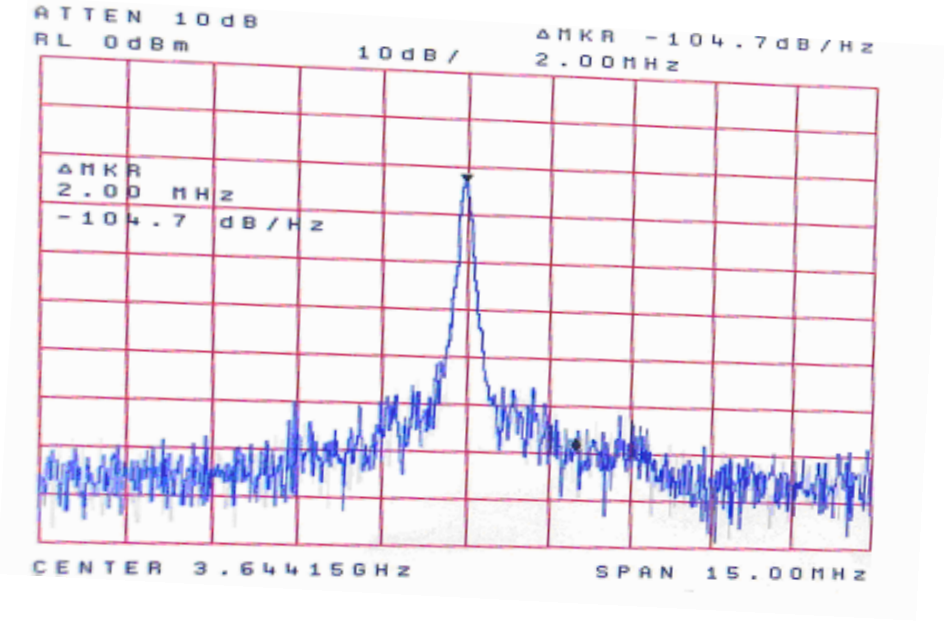

Figure 5.12 Phase noise at 2 MHz offset from 3.64 GHz carrier is -104.7 dBc/Hz.

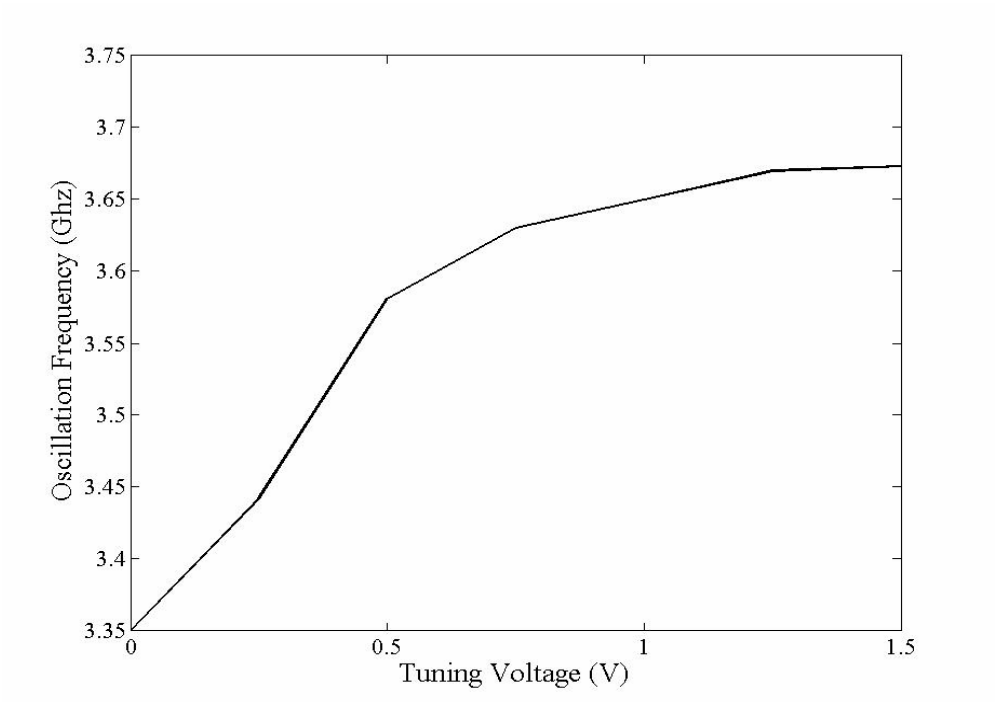

Figure 5.13 Oscillator tuning curve.

5.4 Conclusions

This chapter presented the design theory of multiphase signal generation using LC oscillators. A wide tuning range series coupled oscillator was implemented in a 47 GHz BiCMOS SiGe technology achieving one of the best figure of merit at 5 GHz oscillation frequency reported so far. This was followed by the implementation of multiphase oscillator in SOI technology.

Chapter 6: Digital Controlled Oscillator

6.1 Introduction

Digital controlled oscillators find wide applications in communication systems designed in low power CMOS process technologies. The commonly used oscillator topologies are the controlled delay ring oscillator that fall shy of performance for most RF applications and the conventional LC oscillators that use analog voltage to achieve frequency control. In deep submicron CMOS process, as the voltage headroom is reduced analog tuning for oscillators becomes more difficult. Unlike varactors in conventional CMOS process the varactors in deep submicron process are highly nonlinear. The linear region of operation for the varactor is largely reduced leading to an unreliable tuning curve and poor frequency resolution. Digitally controlled oscillators use a digital approach to frequency tuning by switching the varactor to one of the two distinct capacitance values. The DCO topology is that of a differential LC oscillator and the digital frequency tuning is achieved by individually switching an array of capacitances.

The varactors are designed using the PMOS transistor. The choice of PMOS is influenced by the fact that it is less susceptible to the noise from the substrate as it is well shielded by the n-well. The C-V characteristic of the PMOS varactor is shown in figure 6.1. The reduced linear range of the C-V curve in deep submicron process makes the

oscillation frequency very susceptible to process variations and noise due to the high oscillator gain (K_{vco}).

6.2 Binary weighted varactor bank

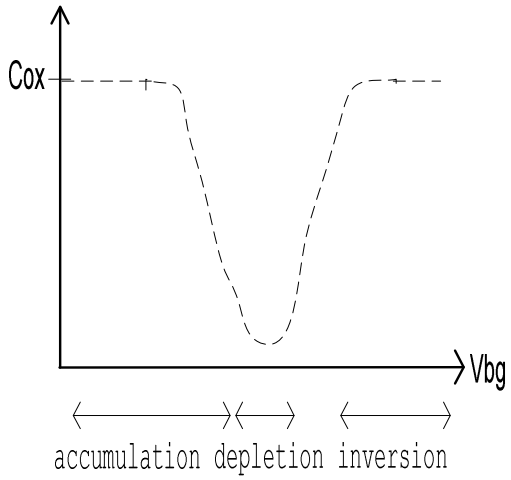

Figure 6.1 Typical C-V characteristic of a MOS capacitor.

In the C-V curve shown in figure 6.1 three distinct regions of operation for the MOS capacitor can be identified which are accumulation depletion and inversion [49]. In the case of PMOS varactor with S=D=B connection shown in figure 6.2, when gate to bulk voltage Vgb is more positive than flat band voltage, the voltage at the oxide semiconductor interface is sufficiently positive to enable the electrons to accumulate and the device is said to be operating in accumulation region. On the other hand, with bulk to gate voltage Vbg sufficiently larger than the threshold voltage an inversion channel with mobile holes build up and the MOS capacitor is in inversion mode [50].

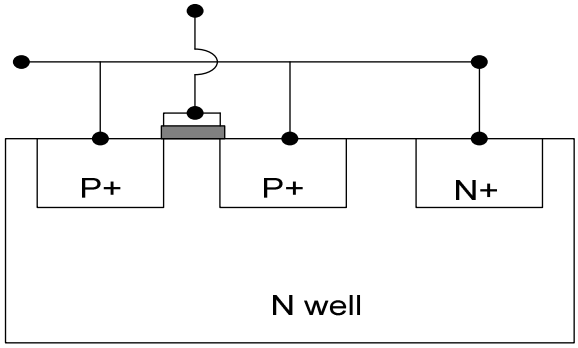

Figure 6.2 A MOS capacitor realized by connecting drain source bulk terminals together as one terminal and gate as the other terminal.

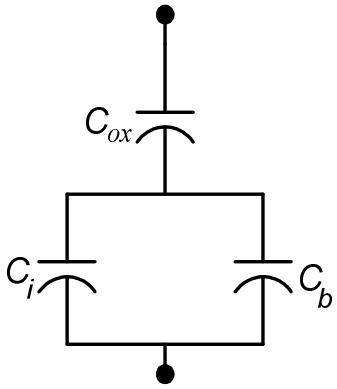

Figure 6.3 Small signal equivalent of the MOS capacitor shown in figure 6.2.

Representing the MOS capacitance as show in figure 6.3 where C_{ox} is in series with parallel combination of C_b and C_i, gate oxide capacitance is C_{ox}, C_b is due to the depletion region charge and C_i is due to inversion layer charge, in both accumulation and strong inversion the MOS capacitance is approximately equal to the oxide capacitance. Two other regions of operation that can be seen are the depletion and weak inversion. In these regions of operation there are nil or very few mobile holes at the oxide semiconductor interface and the MOS capacitance approaches the value of C_b in case of depletion or small values of C_i in case of weak inversion.

In order to have two distinct values of capacitance which can be considered as the on and off states [47] of capacitance the MOS capacitor can be prevented from entering accumulation by tying the bulk to the highest potential VDD as shown in figure 6.4. In this way the capacitor always operates in either depletion or strong inversion providing two distinct capacitance values at two distinct operating regions.

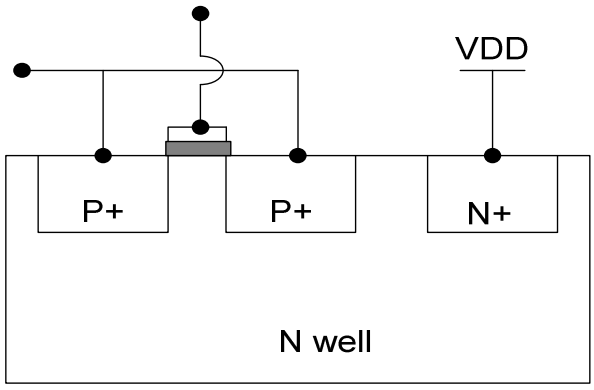

Figure 6.4 Inversion mode PMOS capacitor.

Q of the varactor is strongly dependent on the layout and is given by equation 6.1.

$$Q_{var} = -\frac{I_m(Z11)}{R_e(Z11)} \tag{6.1}$$

This quality factor is due to the parasitic resistor in series with the varactor. The series parasitic resistance is due to the combination of gate resistance, inversion channel resistance and the contact resistance of polysilicon and diffusion.

To avoid this large undesired resistance the varactors are laid out in a multi-finger structure as shown in figure 6.5. Using this approach, the gate resistance is considerably reduced since gate resistance R_{gate} is given by [51]

$$R_{gate} \alpha \frac{F.R}{N} \tag{6.2}$$

where F is the number of squares per finger, R is the square resistance of the polysilicon and N is the number of fingers.

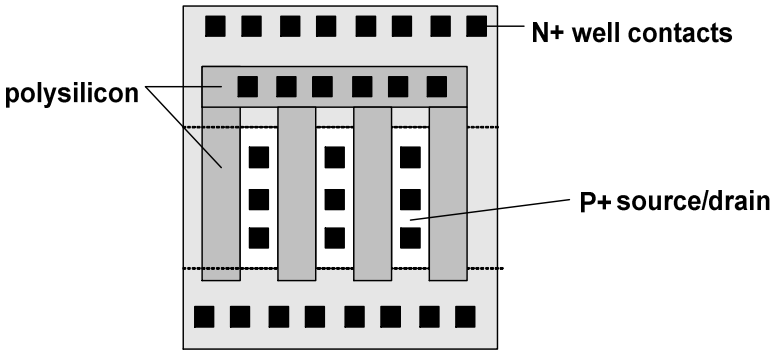

Figure 6.5 Multi-finger layout for RF MOS varactor.

Further reduction in gate resistance by a factor of $\frac{1}{4}$ is achieved by contacting the gate at both the ends. In the inversion region the PMOS channel resistance can be approximated as [53]

$$R_{mos} = \frac{L}{12 \cdot K_p \cdot W \cdot (V_{bg} - |V_t|)} \tag{6.3}$$

where K_p is the transconductance parameter. The above equation suggests that length L should be minimized to reduce the series resistance. Although PMOS varactor has higher parasitic series resistance than the NMOS, the choice of PMOS is influenced by the fact that it is less susceptible to the noise from the substrate as it is well shielded by the n-well. The entire structure was placed in a common n-well and n^+ ohmic bulk contacts connecting the n-well to the power supply between each finger section of the varactor.

The C-V characteristic of the single unit varactor used in the design was simulated using the setup shown in figure 6.6. The 0.75 V at the source/drain is the DC operating point of that node in the oscillator. The AC source represents the magnitude of the swing

at that node. Vg is the bias tuning voltage. The simulated C-V curves of the LSB varactor for S=D connection and S=D=B connection are shown in figures 6.7 and 6.8. The varactor is implemented in a differential fashion using two inversion mode transistors such that their drain and source are tied together to the tuning control voltage and the gates are connected in parallel to the inductor to form the tank. Hence the total capacitance seen across the tank is half the value provided by the single transistor.

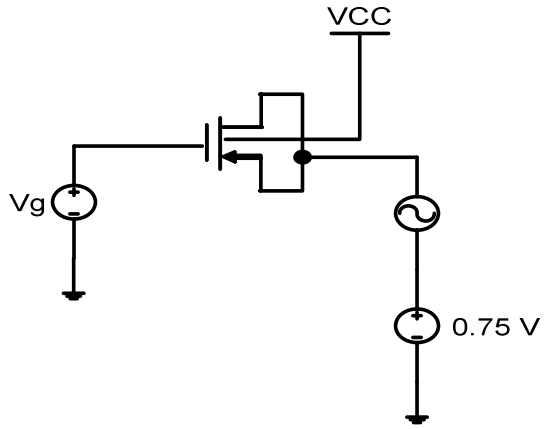

Figure 6.6 Schematic diagram for simulating C-V characteristic.

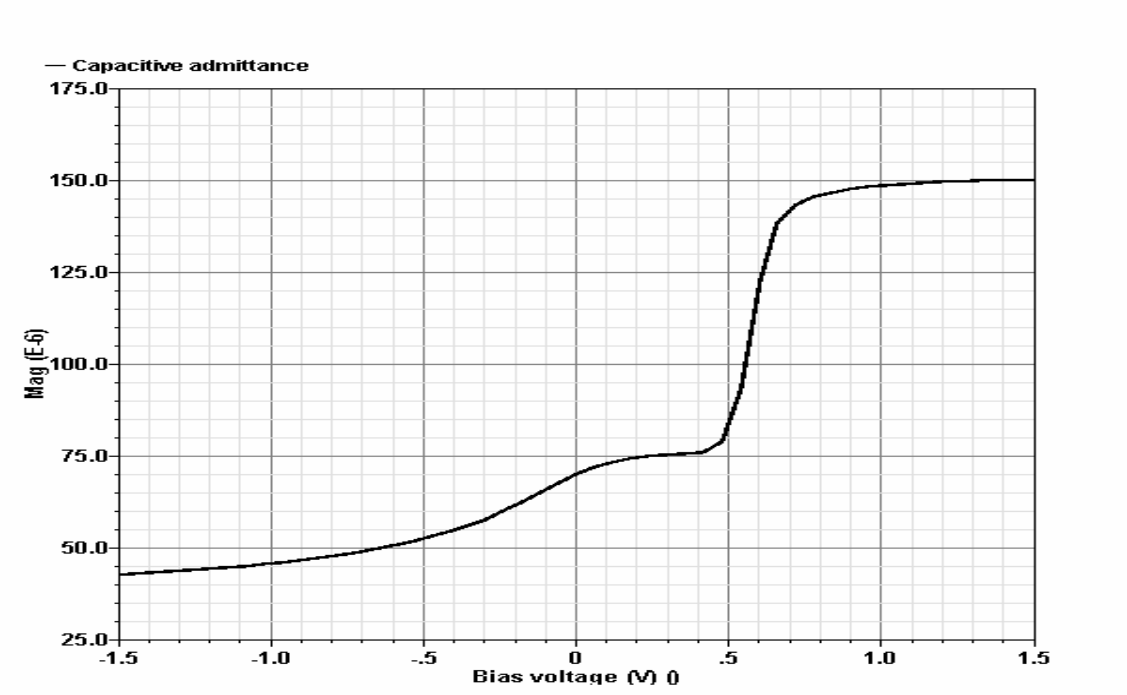

Figure 6.7 Simulated C-V curve of the LSB varactor with S=D.

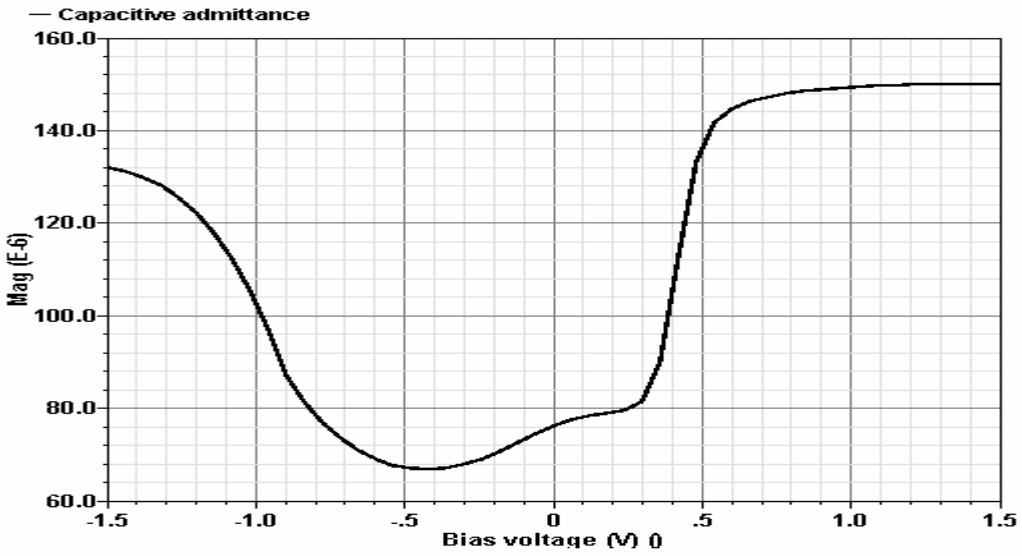

Figure 6.8 Simulated C-V curve of the LSB varactor with S=D=B connection.

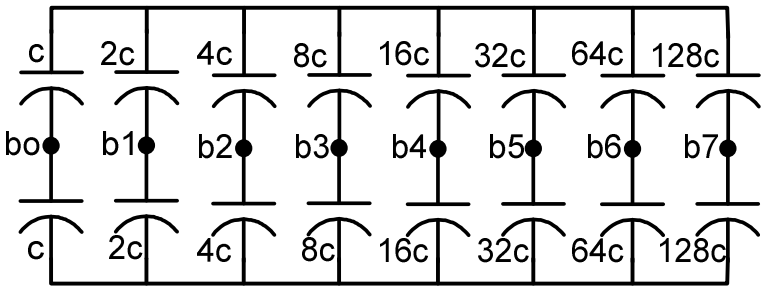

Figure 6.9 Binary weighted varactor bank.

The varactor bank consists of eight binary weighted capacitors shown in figure 6.9. The total varactor capacitance across the tank is controlled by an eight bit control word (b0-b7). The digital values for the control bits ensure that the varactors are in either depletion or inversion mode. The basic unit varactor cell controlled by bit b0 consists of a single MOS transistor with aspect ratio of 20.25/1. The next varactor cell consists of double the number of unit varactors than the previous one. This is mainly to ensure better component matching so that the parasitic fringing capacitance is also well ratioed among the varactors. Figure 6.10 shows the simulated plot of the effective switching capacitance provided by the varactor bank when all the bits are switched from zero to one. The “on” and “off” capacitances of the tank differ by about 175 fF as shown in figure 6.10.

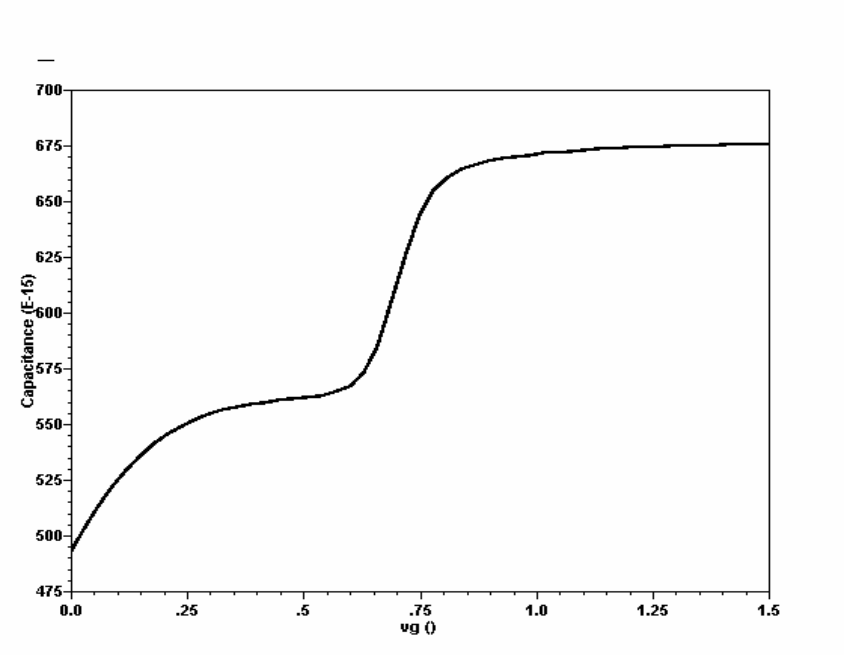

Figure 6.10 Simulated maximum and minimum capacitance values provided by the varactor bank.

6.3 DCO circuit design

The configuration consists of NMOS and PMOS cross-coupled pair provides a negative resistance of $-g_m$ to overcome the parasitic tank resistance. The transistors are sized such that each pair provides half the transconductance required to overcome the tank loss. The choice of NMOS PMOS combination is used because it effectively cuts the power consumption to provide the same negative resistance as compared to only NMOS or PMOS topologies. More over this topology has been shown to have reduced $1/f$ upconverterd noise [54]. CMOS inverters are used as buffer, they provide high impedance to the oscillator output and are biased with current sources to improve their drive capability. Figure 6.11 shows the oscillator circuit along with its output buffers.

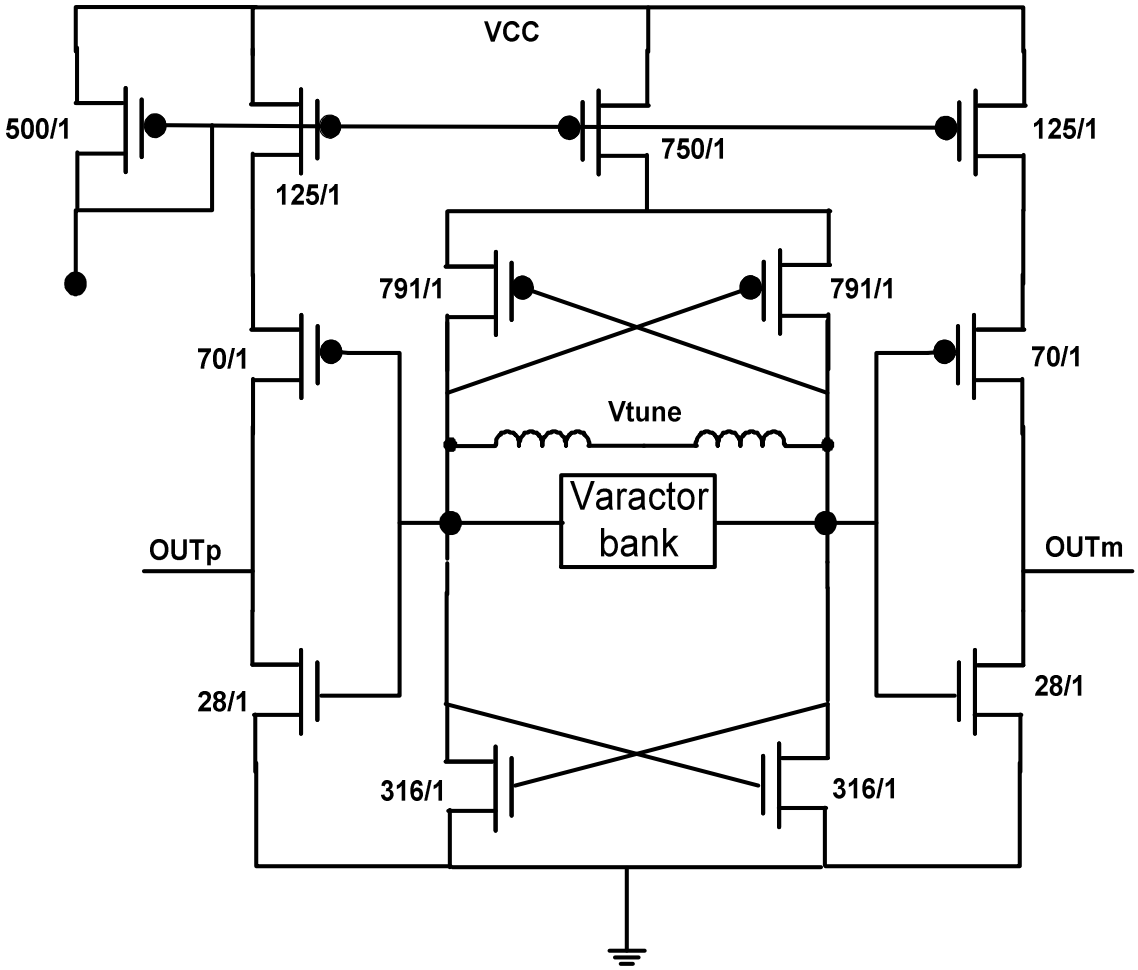

Figure 6.11 DCO design schematic.

When all bits are zero the oscillation frequency is given by

$$F_{osc} = \frac{1}{2\pi\sqrt{LC_{off}}} \tag{6.4}$$

where C_{off} includes the "off" capacitance of the varactor bank and the junction capacitances of the NMOS-PMOS pair. When the bits are turned on the oscillation frequency can be given as

$$F_{osc} = \frac{1}{2\pi\sqrt{L\left(C_{off} + \sum_{n=0}^{7} b_n 2^n \Delta C\right)}} \tag{6.5}$$

where ΔC is the switching capacitance provided by the corresponding bit. The frequency resolution of the DCO $F_{resolution}$ is given as

$$F_{resolution} = \frac{F_{\max} - F_{\min}}{2^b} \tag{6.6}$$

where $F_{\max}$ and $F_{\min}$ are the maximum and minimum oscillation frequencies and b is the number of varactor control bits.

6.4 Measured results

The DCO was designed and fabricated in a 0.12 μm BiCMOS process. This design oscillates from 4.2 to 4.7 GHz (11.2%) providing an average frequency resolution of 2 MHz /LSB. Figure 6.12 shows the K_{DCO} curve. Since the varactors are binary weighted maximum discontinuities in output frequency can be observed at the periodic intervals of two's power when the tuning code changes from 31 to 32 or 63 to 64 since the maximum number of unit varactors are turned off at that instant.

The die was wire-bonded directly to gold plated printed circuit test board to facilitate testing. Figure 6.13 shows the output spectrum of the oscillator. The power delivered to 50 ohm load is -7 dBm. The phase noise was measured using the phase noise utility in the Agilent 8563EC spectrum analyzer. Figure 6.14 shows the phase noise of the oscillator versus the offset frequency. The measured phase noise is -103 dBc/Hz at 500 KHz offset

from 4.7 GHz carrier frequency. This design achieves a high figure of merit of 177 dBc/Hz which is given by [55].

$$FOM = -10\log(L(\Delta f)) - 10\log\left(\frac{\Delta f^2}{f_{osc}^2}\frac{P_{diss}}{1mW}\right) \tag{6.7}$$

The oscillator core consumes a current of 3.5 mA from a 1.2 V supply. Figure 6.15 shows the DCO micrograph. The die area of the chip is 1.7 mm*1.3 mm.

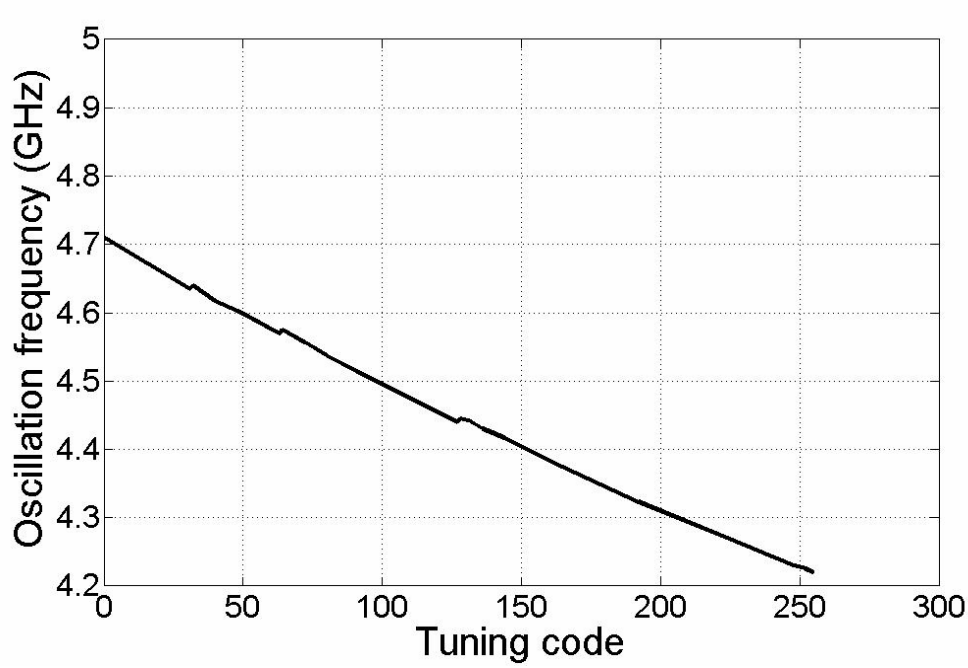

Figure 6.12 Output frequency of the oscillator versus tuning code.

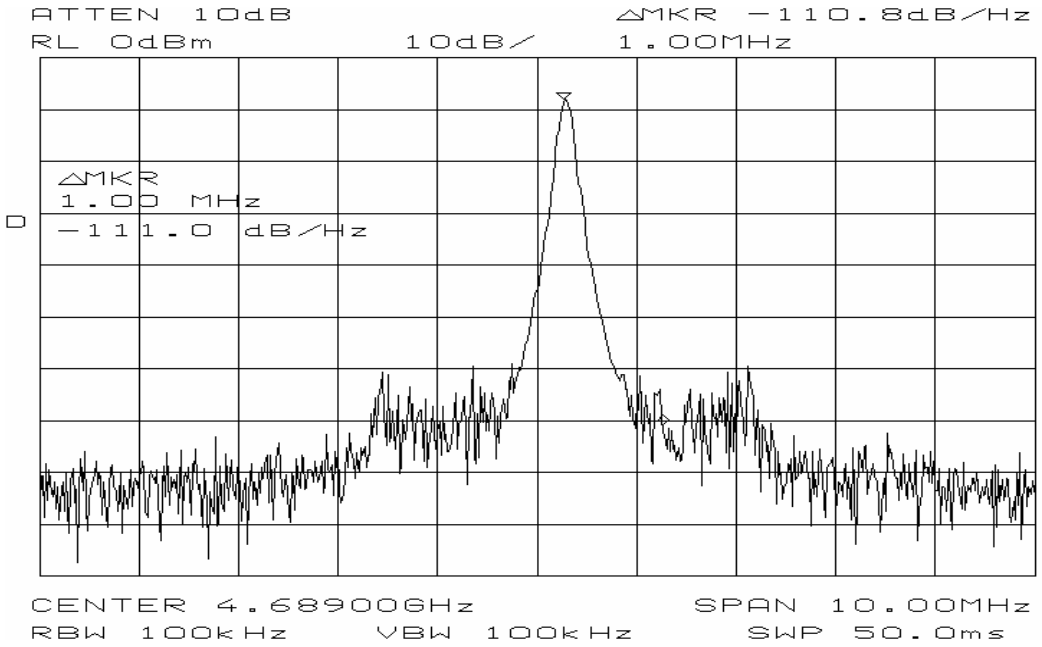

Figure 6.13 Output spectrum of the oscillator.

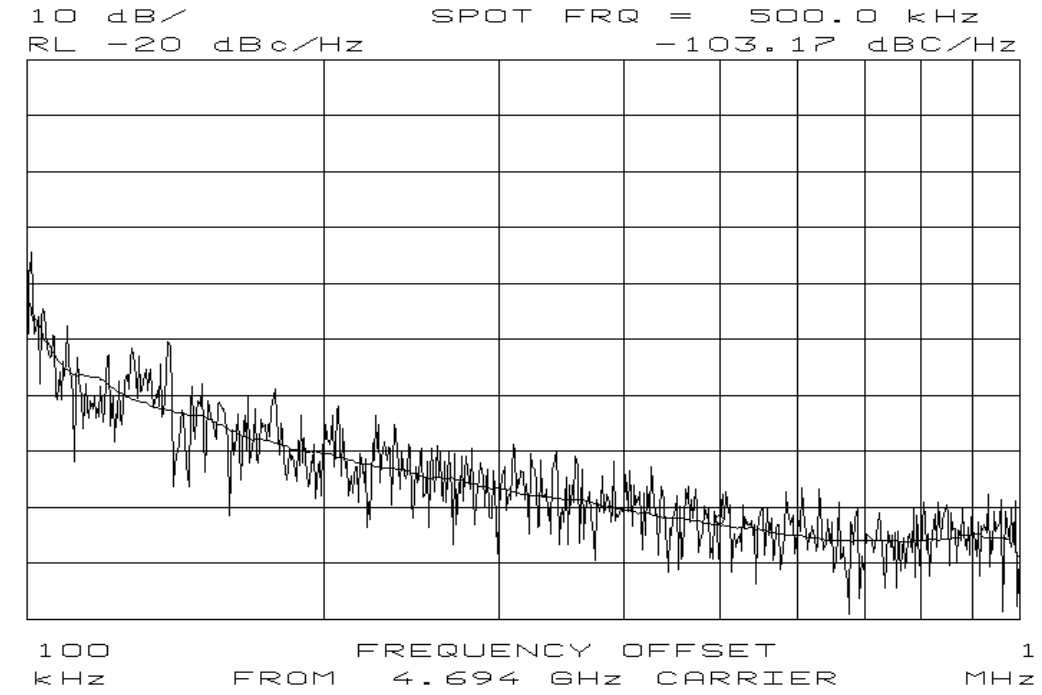

Figure 6.14 Phase noise vs. offset frequency of the oscillator.

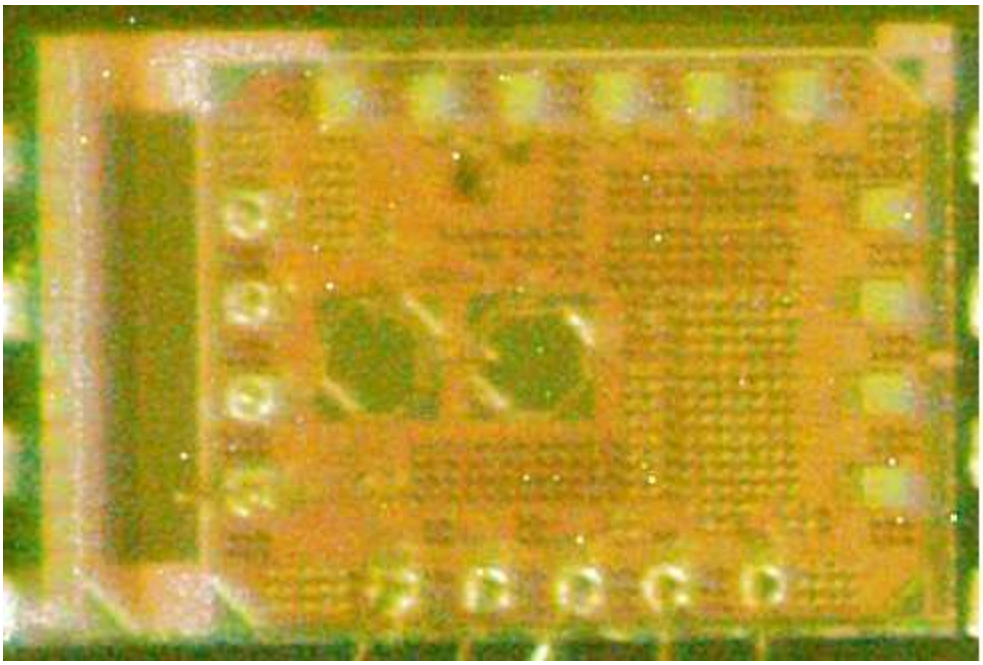

Figure 6.15 Die photo of the oscillator.

Supply voltage	1.2 V
Oscillation frequency	4.2-4.7 GHz
Resolution	2 MHz/bit
Core current	3.5 mA
Phase noise @ 500 KHz	-103 dBc/Hz
Output power	-7 dBm
Area	$2.2\,mm^2$
FOM	-177

Table 6.1 Measured performance of the DCO.

Ref.	[48]	[56]	This work
Technology	130 nm CMOS	65 nm CMOS	120 nm BiCMOS
Supply (V)	2.5	1.1	1.2
Frequency	2.4	10	4.5
Tune range	20.8%	10%	11.2%
L (dBc/Hz)	-112	-102	-103.17
Offset □f	500 KHz	1 MHz	500 KHz
Power	3.4 mW	3.3 mW	3.7 mW
FOM	-180	-177	-177

Table 6.2 Comparison with other DCO designs.

6.5 Conclusions

This chapter has presented the design of low voltage and low power 4.5 GHz 8-bit digitally controlled oscillator fabricated in a 120 nm BiCMOS SiGe technology. The oscillator operates from 1.2 V supply, takes 8-bit CMOS inputs and provides an average frequency resolution of around 2 MHz/bit delivering a good FOM of -177 dBc/Hz.

Chapter 7: Phase Locked Loop Design

7.1 Introduction

A Phase Lock Loop (PLL) is a feedback system that generates a signal with output frequency f_{out} from a reference signal of frequency f_{in} while maintaining a constant phase difference $\Delta\phi$ between the input and output frequencies. Figure 7.1 shows the block diagram of the PLL.

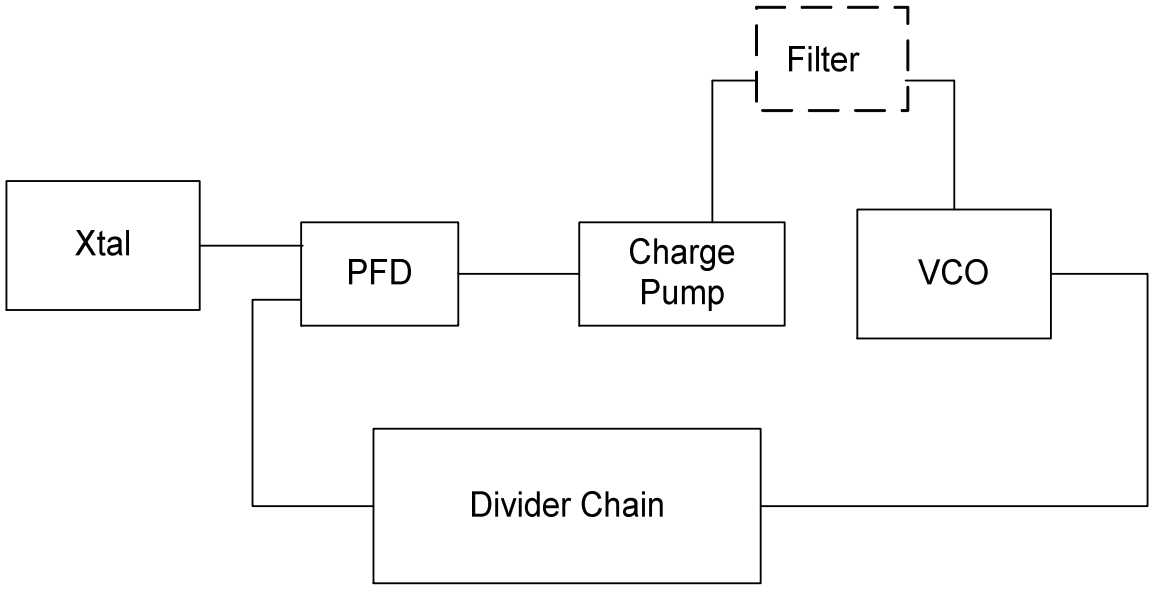

Figure 7.1 Block diagram of a PLL.

The loop starts with a stable crystal oscillator providing a reference frequency (F_{ref}). This is one of the inputs to the phase frequency detector. The Phase Frequency Detector (PFD) gives out a DC current that is proportional to the phase difference between the

reference frequency and the output frequency after it is divided by the divider. The PFD output current multiplied by the impedance of the loop filter forms the tuning input to the oscillator. When the loop is in locked condition there is a zero or constant phase difference between the two inputs of the phase detector. Since the frequency is the differential of phase, it implies that the frequencies are also matched.

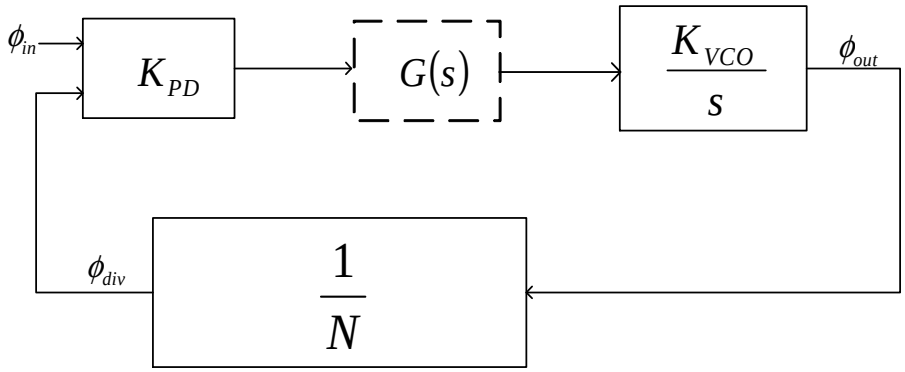

Figure 7.2 Linear model of a PLL.

Figure 7.2 shows the linear model of a PLL. K_{PD} is the phase detector and charge pump gain. The phase frequency detector (PFD) outputs a DC current that is proportional to $\Delta\phi$, where $\Delta\phi = \phi_{in} - \phi_{div}$. The constant of proportionality is given by the amount of current that the charge pump can source or sink in to the loop filter. K_{PD} is expressed in the units of $mA/2\pi$. $G(s)$ is the transfer function of the loop filter.

The transfer function of the oscillator can be expressed as

$$f_{out}(t) = K_{vco} \cdot V_{tune}(t) \tag{7.1}$$

where f_{out} is the output frequency of the oscillator, K_{vco} is the oscillator gain and V_{tune} is the tuning input of the oscillator. Integrating the above equation gives

$$\phi_{out} = K_{vco} \int_0^T V_{tune}(t)dt \tag{7.2}$$

which can be written in s domain as

$$\phi_{out}(s) = \frac{K_{vco} \cdot V_{tune}(s)}{s} \tag{7.3}$$

where K_{vco}/s is the transfer function of the oscillator. The transfer function of the closed loop can be determined as equation 7.3.

$$H(s) = \frac{\phi_{out}(s)}{\phi_{in}(s)} = \frac{NK_{PD}K_{vco}G(s)}{Ns + K_{PD}K_{vco}G(s)} \tag{7.4}$$

The order of the loop filter is determined by the number of poles in the closed loop and open loop transfer function. The type of the PLL is determined by the number of poles in the loop filter.

7.2 Charge pump PLL

A type II PLL is the most commonly used topology and is shown in figure 7.3. When the loop is in the locked state, PFD and charge pump detects any phase difference between the signals f_{ref} and f_{div}. When there is a phase error the phase detector generates either UP or DN signals that turn on one of the switches of the charge pump to create a small change on the tuning voltage of the oscillator to compensate for the phase error.

If the period of the input frequency of the PLL is T and $\Delta\phi$ is the phase difference between the signals f_{ref} and f_{div}, then the on time of the UP/DN signals is given by the

equation 7.5. The current through the charge pump can then be determined by equation 7.6 there by giving the phase detector gain as $K_{PD} = \frac{I_{cp}}{2\pi}$.

$$t_{on} = \frac{\Delta\phi \cdot T}{2\pi} \tag{7.5}$$

$$I_{cp} \cdot \frac{t_{on}}{T} = I_{cp} \cdot \frac{\Delta\phi}{2\pi} \tag{7.6}$$

The current through the charge pump is injected in to the loop filter and is converted as the tuning input to the oscillator. The loop filter shown in figure 7.3 is a second order loop filter. C1 acts as an integrating capacitor and generates a pole at DC, R2 introduces a stabilizing zero and C2 is used to reduce the glitches from the tuning line when the charge pump periodically outputs current every reference cycle [24].

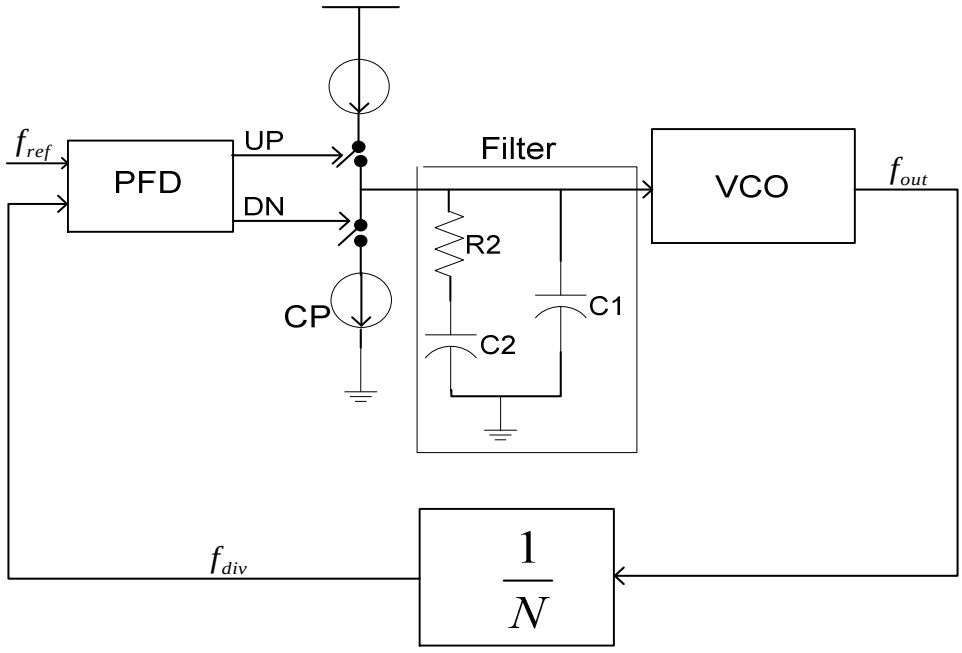

Figure 7.3 Type II charge pump PLL.

The transfer function of the loop filter is given by equation 7.7, the location of poles and zeros can be calculated by equations 7.8 and 7.9 respectively.

$$\frac{V_{tune}}{I_{cp}} = \frac{1 + sR2C2}{s^2 R2C1C2 + s(C1 + C2)} \tag{7.7}$$

$$\omega_z = \frac{1}{R2C2} \tag{7.8}$$

$$\omega_{p1} = 0, \omega_{p2} = \frac{1}{R2\left(\frac{C1C2}{C1 + C2}\right)} \tag{7.9}$$

Computing the open loop transfer function of the PLL, the open loop transfer function of the PLL is given by the equation 7.10 [63]. The phase margin of the loop can be calculated from the equation 7.11, where ω_c is the loop bandwidth.

$$H_{ol}(s) = \frac{K_{PD} G(s) K_{vco}}{N} = \frac{K_{PD} K_{vco}(1 + sR2C2)}{N\left(s^2 R2C1C2 + s(C1 + C2)\right)} \tag{7.10}$$

$$\phi_m = \tan^{-1}\left(\frac{\omega_c}{\omega_z}\right) - \tan^{-1}\left(\frac{\omega_c}{\omega_{p2}}\right) \tag{7.11}$$

Calculating the phase margin and maximizing it at the loop bandwidth by solving for $d\phi_m / d\omega_{\omega=\omega_c} = 0$ gives the solution $\omega_c = \sqrt{\omega_z \omega_{p2}}$ for maximum phase margin and the maximum phase margin can be calculated to be [63]

$$\phi_m = \tan^{-1}\left(\sqrt{\frac{\omega_{p2}}{\omega_z}}\right) - \tan^{-1}\left(\sqrt{\frac{\omega_z}{\omega_{p2}}}\right) \tag{7.12}$$

The location of pole and zero as a function of the loop bandwidth are given by equations 7.13 and 7.14.

$$\omega_z = \frac{\omega_c}{\sqrt{1+\frac{C2}{C1}}} \tag{7.13}$$

$$\omega_{p2} = \omega_c \sqrt{1+\frac{C2}{C1}} \tag{7.14}$$

At the maximum phase margin condition, we have $|H_{ol}(s)| = 1$ which gives the following value for the loop bandwidth.

$$\omega_c = \frac{I_{cp} K_{vco} R2C2}{N(C1+C2)} \tag{7.15}$$

The loop is designed to have a phase margin greater than 45° to ensure stable operation. A small phase margin results in small damping factor for the PLL causing large overshoot during the locking process.

7.3 Phase frequency detector

A Phase Frequency Detector (PFD) is used to detect both the frequency and phase difference between the reference signal and the divided oscillator signal. There are many types of phase frequency detectors but the most commonly used for phase locked loop applications is the one shown in figure 7.4. Its structure is that of a typical dead zone free phase detector with two edge triggered reset able D-flip-flops with their D inputs connected to logic high. In figure 7.4 signals A and B are the inputs to the phase frequency detector. UP and DOWN are the outputs. When A leads B rising edge on A produces a rising edge on UP and it continues to remain high till a rising edge on B

occurs. Rising edge on B produces a pulse on DOWN whose width is set by the width of the reset pulse. The difference between the average values of UP and DOWN signals represent the phase or the frequency difference of the input signals. Since the PFD has two outputs, four distinct states are possible. In three of them either UP or DOWN is high and are encountered during the lock acquisition phase. In locked state both the outputs react simultaneously to the edges on the inputs and become high, which is the undesired fourth state. Then the AND gate detects this state and resets both the flip-flops. The width of the pulses UP and DOWN is determined by the delay through the flip-flop and the delay through the AND gate. If the phase difference is small, then width of the pulses are too narrow, and they may not be able to properly activate the charge pump transistors, a problem commonly referred to as dead zone. When the loop reaches dead zone, the PFD stops responding to the phase difference between its inputs and the tuning voltage of the oscillator is no longer controlled by the charge pump, thereby operating the oscillator in open loop. If their widths are unequal, they will cause mismatch in the currents of the charge pump leading to ripple on the oscillator tuning line. To avoid the dead zone problem extra buffers and capacitors are placed in the feedback path of the PFD at the output of the AND gate. This buffered delay is designed to produce 1 ns wide pulses in lock condition. This ensures that the output pulses of the PFD are always sufficiently wide enough to turn on the source/sink transistors of the charge pump. The flip-flops used in design are constructed with two latches using NOR gates. Figure 7.5 shows the simulation result of the phase frequency detector.

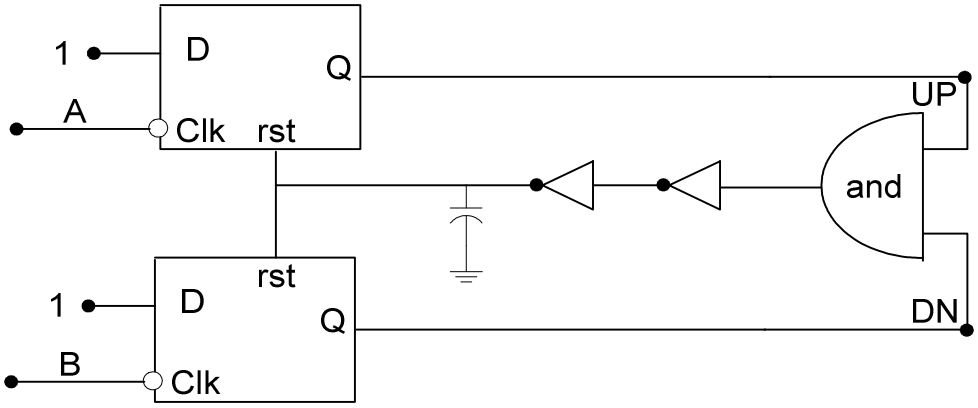

Figure 7.4 Phase frequency detector block diagram.

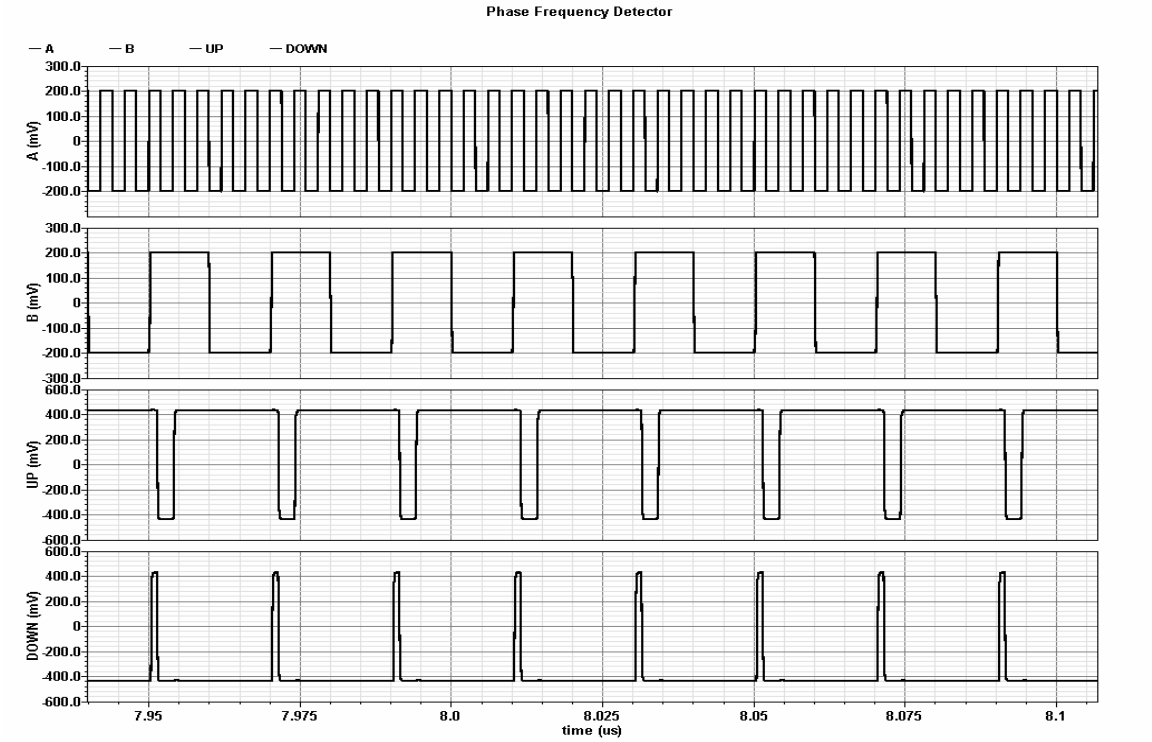

Figure 7.5 PFD simulation result.

7.4 Charge pump and loop filter

The phase frequency detector is followed by a charge pump having differential input and single ended output. In general the charge pump consists of two current sources that

serve to sink/source charge through the loop filter. These current sources are controlled by the signals coming from the phase frequency detector. The amount of charge these current sources sink or source from the charge pump is determined by the time they are turned on and off to set a proper voltage on the tuning line of the oscillator. Non idealities in the charge pump is one of the main reasons for the occurrence of spurious tones at the output of the PLL. There are two main reasons for the non idealities [64]: (i) leakage currents in the charge pump (ii) mismatch while sinking and sourcing current through the loop filter. Ideally the charge pump is not supposed to give out any current when the loop is locked, but when a leakage current is present in the charge pump, it tends to alter the tuning voltage of the oscillator. The only way to correct this situation then, is for the charge pump to output a current exactly equal to the leakage current at the next comparison cycle. As this process keeps repeating at every comparison cycle it leads to a ripple on the tuning voltage line of the oscillator. The magnitude of the ripple on the tuning line can be calculated from equation 7.16 [65]. Where A_m is the magnitude of the ripple, I_{leak} is the leakage current and $Z\left(j\omega_{ref}\right)$ is the impedance of the loop filter at the reference frequency. The magnitude of the ripple A_m does not depend on the bandwidth of the loop filter or the charge pump. It is solely determined by the leakage current and the impedance of the loop filter. Given then magnitude of the ripple at the charge pump output the magnitude of spurious tone A_{sp}, with respect to the carrier A, can be calculated by equation 7.17 [65].

$$A_m = 2I_{leak}\left|Z\left(j\omega_{ref}\right)\right| \tag{7.16}$$

$$\frac{A_{sp}}{A} = 20\log\left(\frac{A_m K_{vco}}{4\pi f_{ref}}\right) \tag{7.17}$$

The other main non ideality is the mismatch between the current sources used in the charge pump. If unequal currents flow through the current source and the current sink mirrors of the charge pump, then a net charge injection is performed at every reference cycle and the loop responds by locking with a non zero phase difference.

Shown in figure 7.6 the designed charge pump circuit has two switching differential pairs Q1-Q2 and Q3-Q4 which take in the PFD output signals and switch the current sources I_{source} or $I_{\sin k}$ to charge or discharge the loop filter.

The ordering of inputs to the switching pairs are placed in a complimentary fashion and thus during the process of acquiring lock when either the UP or DOWN signal is high, the actual current flowing through charge pump output is the sum of I_{source} and $I_{\sin k}$. Compared with conventional charge pump circuits where only one of the currents I_{source} or $I_{\sin k}$ flows through the charge pump output, this circuit effectively reduces the power consumption by half and also requires lesser sampling cycles to phase lock. During lock, the phase frequency detector outputs periodic UP and DOWN pulses during which both diodes connected transistors M1 and M2 turn on and no current flows in to the loop filter.

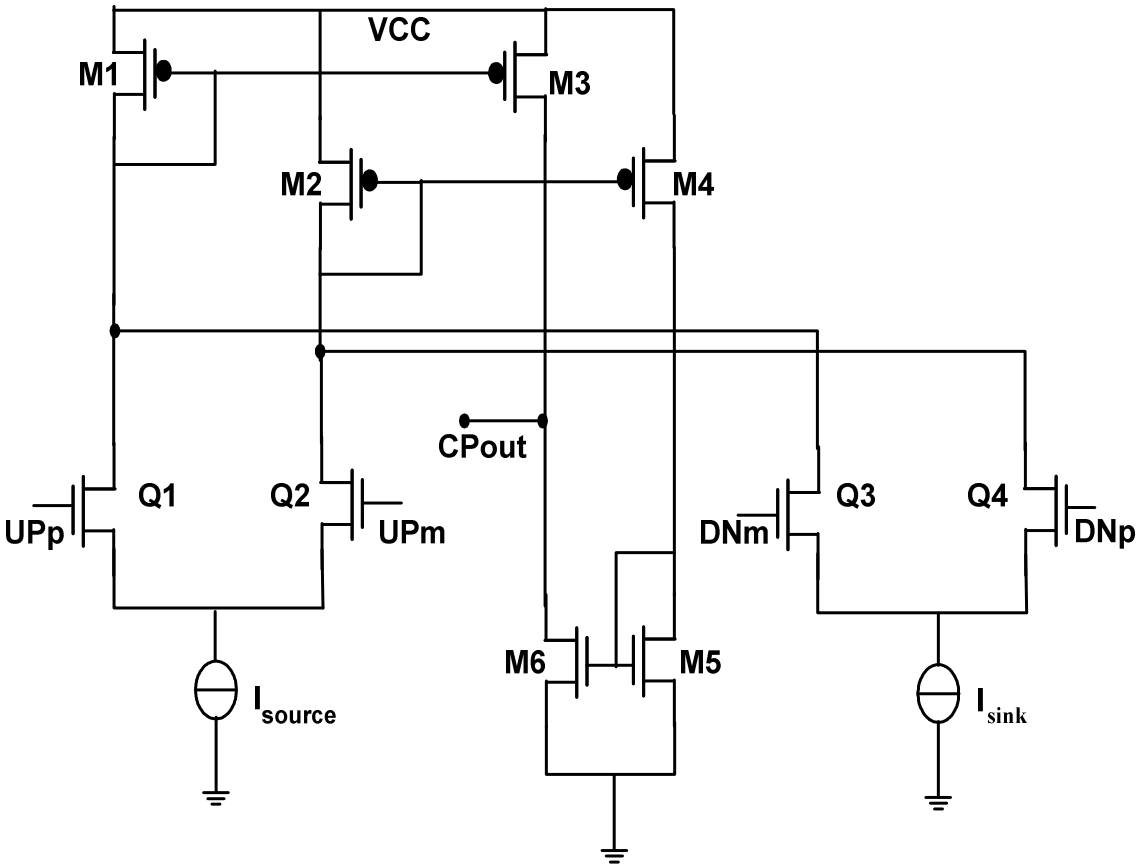

Figure 7.6 Charge pump schematic.

The switching time of the differential pairs in the charge pump is an important parameter and is determined by the load connected to the UP/DOWN pairs. Since both the switching pairs Q1-Q2 and Q3-Q4 share the same load, which are the diode connected transistors M1 and M2, the mismatches in the switching time of the differential pairs is also reduced. To ensure better current copying at the MOS current mirrors and have increased output resistance at the charge pump output node, large channel length of $2\,\mu m$ was used for all MOS transistors used on current mirrors. Figures 7.7 and 7.8 show the simulation results of the charge pump design. When signal A of the phase frequency

detector leads B the charge pump sinks current in to the loop filter and when signal B leads A the charge pump sources current from the loop filter.

When the loop is locked, the noise from the current mirror transistors M3 and M6 are injected in to the loop filter only when they are on during the periodic pulses generated by the PFD to avoid dead zone. This entails a tradeoff between the minimization of charge pump noise and minimization of the dead zone. When the charge pump is on, the output noise current from the charge pump i_{cp} is given by equation 7.18.

$$i_{cp}^2 = \alpha \cdot i_n^2 \tag{7.18}$$

$$\alpha = \frac{t_{on}}{T_{ref}} \tag{7.19}$$

α is the fraction of the time for which the charge pump is on in between two comparison cycles, i_n^2 is the output noise of the current sources. Figure 7.9 shows the simulated output noise current of the charge pump. The transfer function of this noise source to the output is given by equation 7.20. Charge pump noise along with the dividers are the main source of noise with in the loop bandwidth as the noise from the oscillator is diminished by the gain of the loop.

$$H_{cp}(s) = \frac{K_{vco} N Z(s)}{Ns + K_{PD} K_{vco} Z(s)} \tag{7.20}$$

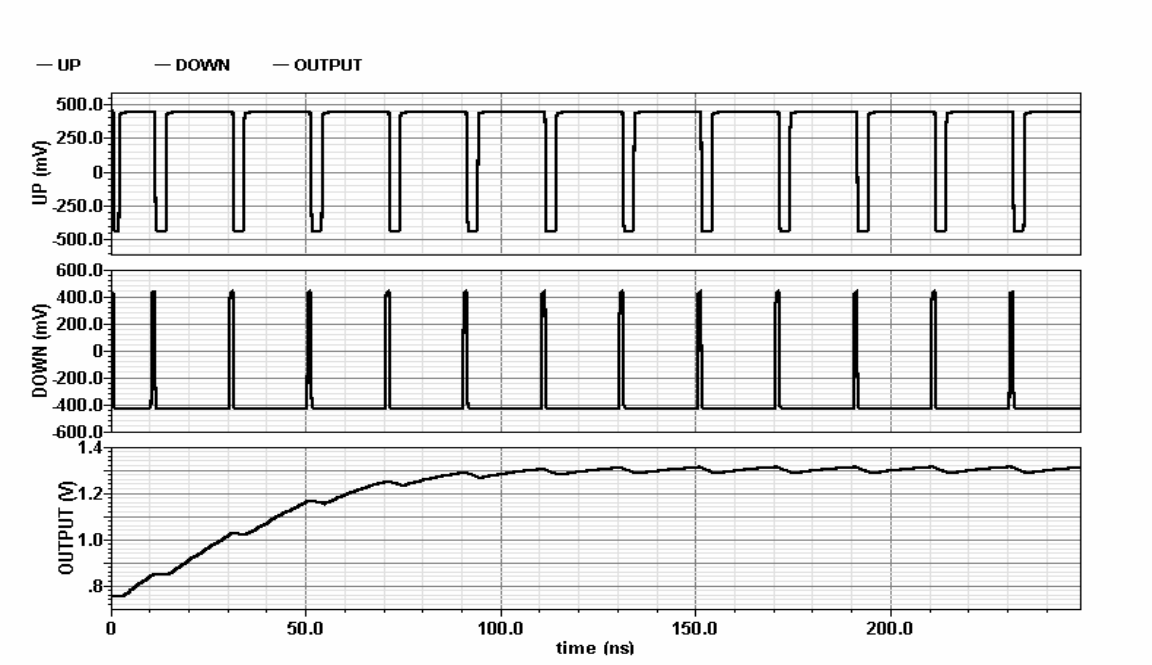

Figure 7.7 Charge pump simulation result while sinking current in to the loop filter.

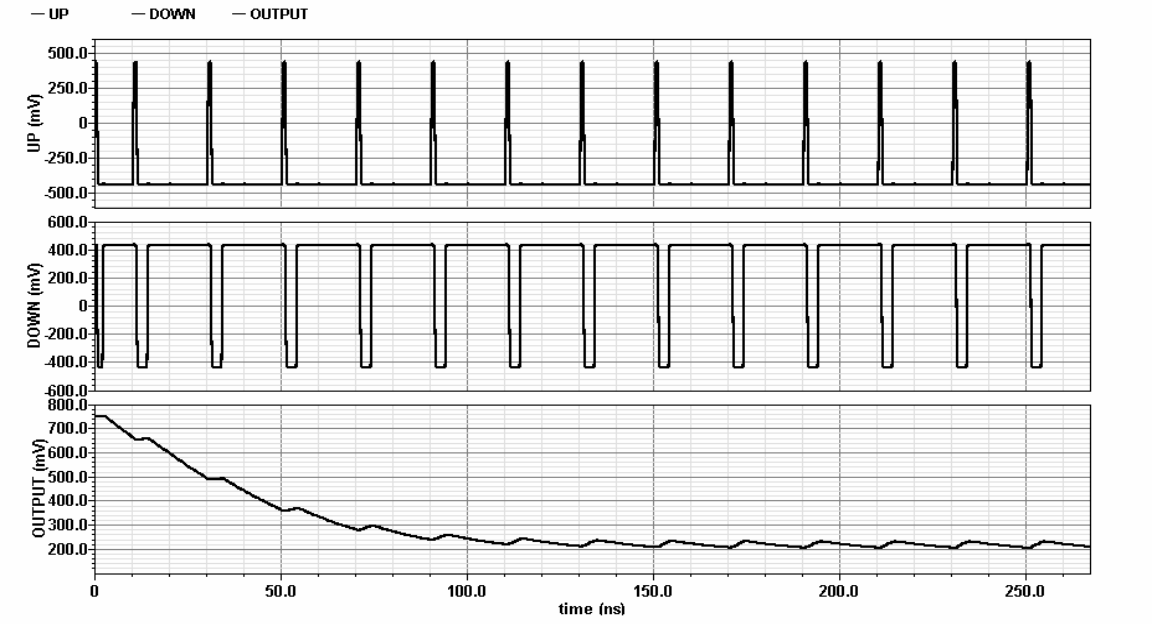

Figure 7.8 Charge pump simulation result, while sourcing current from the loop filter.

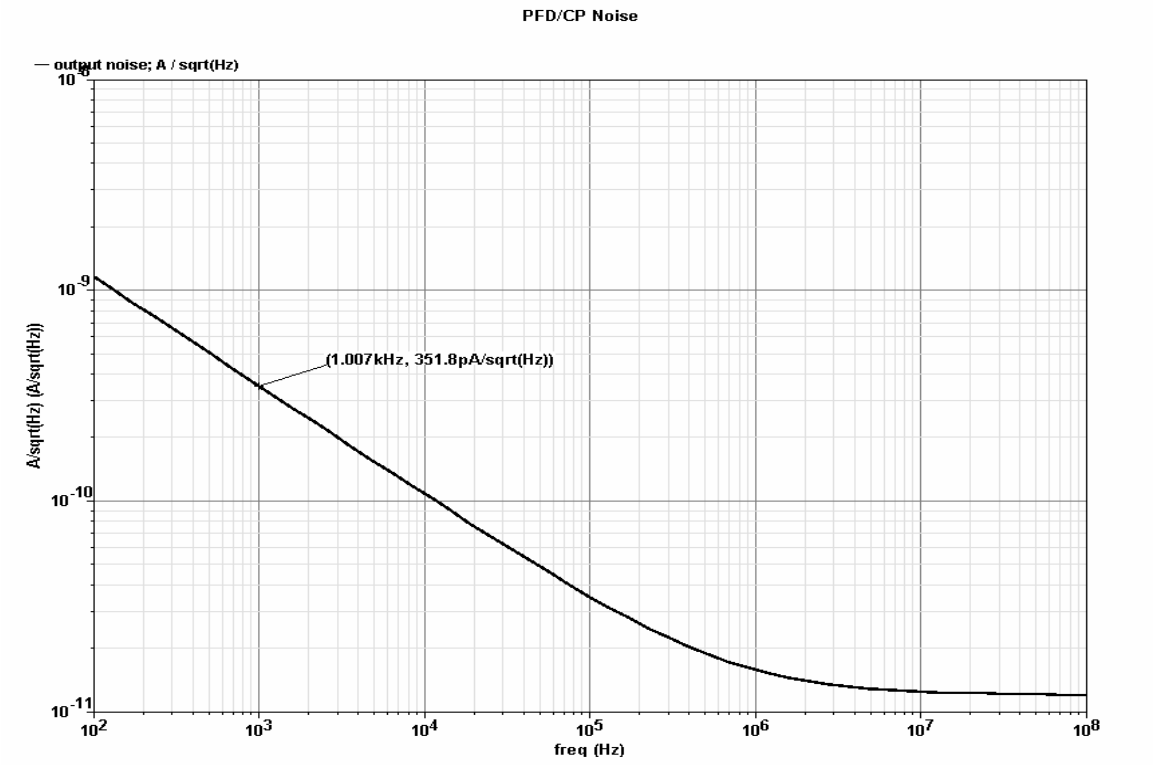

Figure 7.9 Simulated output noise current of the charge pump.

7.5 Oscillator and frequency dividers

A standard configuration of NMOS and PMOS cross-coupled pair oscillator was used in the design. Figure 7.10 shows the schematic of the oscillator. The cross-coupled transistors are sized such that each pair provides half the trans-conductance required to overcome the tank loss. The choice of NMOS PMOS combination was used because it effectively cuts the power consumption to provide the same negative resistance as compared to only NMOS or PMOS topologies. More over this topology has been shown to have reduced $1/f$ upconverted noise [54].

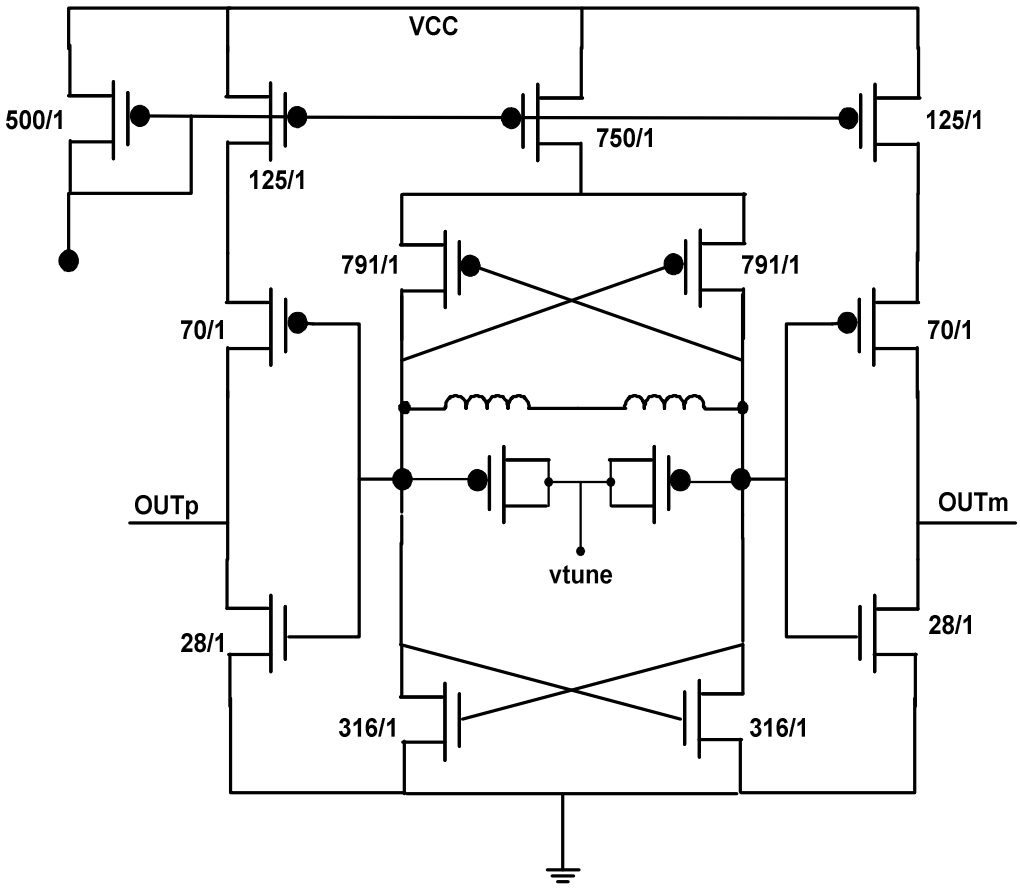

Figure 7.10 Oscillator schematic diagram.

Frequency dividers used in the design present an integer division ratio of 128. This is done by cascading a chain of divide-by-two circuits. Figure 7.11 shows the schematic diagram of the MOS current mode logic latch used in the divider. The latch consists of a sense pair formed by transistors M1, M2 for sensing the input and a regenerative pair formed by M3, M4 for storing the state. The clock pair of transistors formed by M5 and M6 select the sense and store mode of the latch.

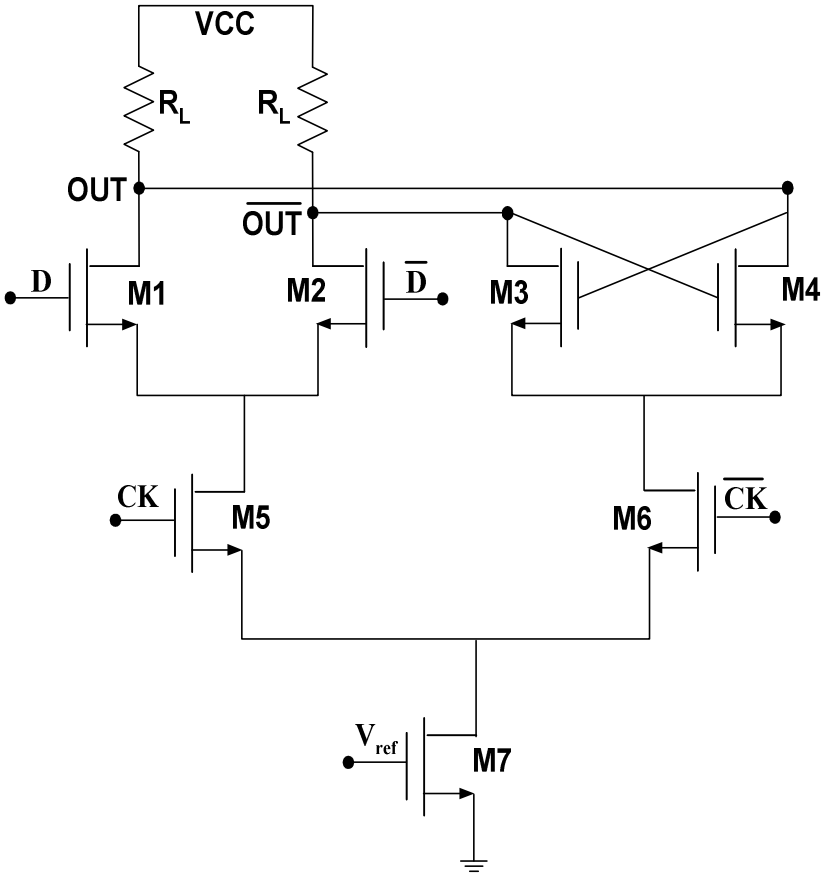

Figure 7.11 Schematic diagram of the D-Latch.

When clock goes high, the current through the tail transistor is steered to M1 and M2. When the clock goes low the sense pair is disabled and the store pair is enabled storing the logic state between its outputs. Figures 7.12 and 7.13 show the time domain periodic noise of the dividers.

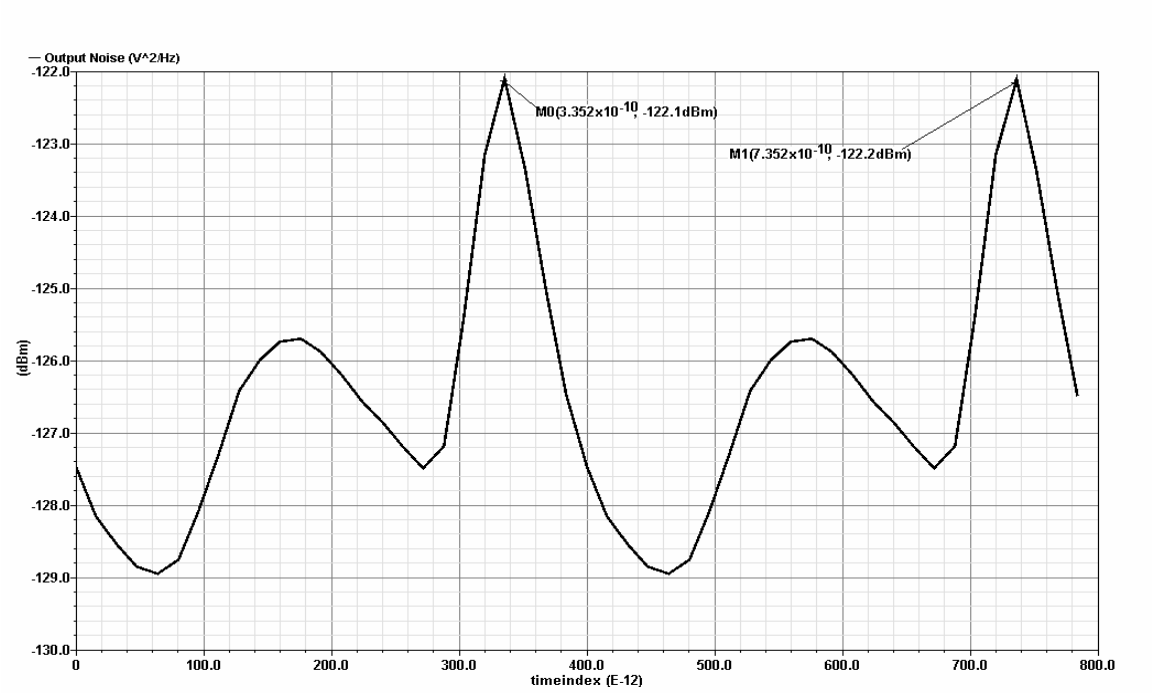

Figure 7.12 Periodic time domain noise of the divider.

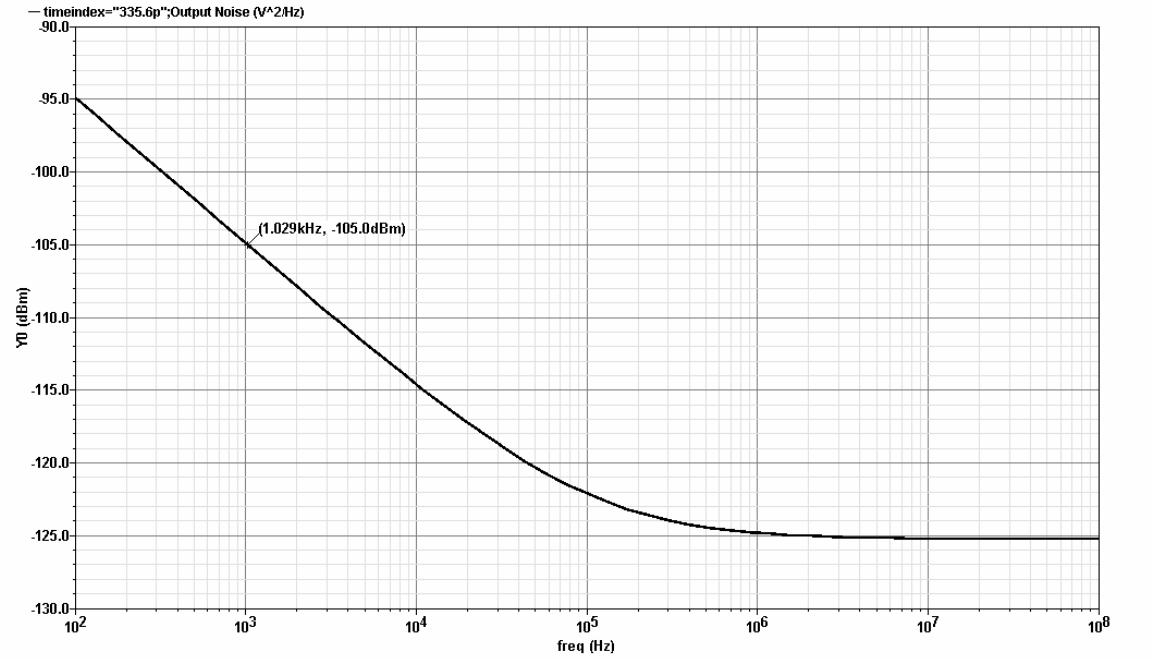

Figure 7.13 Divider output noise spectrum.

7.6 Measured results

The PLL chip was fabricated in 0.18 μm BiCMOS process using only CMOS part of the technology. It had a reference frequency of 39 MHz. The oscillator frequency is 5 GHz. The loop filter values have been chosen as R2 = 4K Ω, C2 = 1 nf, C1 = 59 pf to provide loop corner frequency of 200 KHz. The entire PLL operates from a 1.5 V supply, consumes 122 mA of current and occupies 2.5 mm^2 of die area. Figure 7.14 shows the layout diagram of the PLL chip. The close in-band phase noise which is dominated by the reference oscillator and charge pump was measured as -71 dBc/Hz @ 10 KHz offset and out-band phase noise which is dominated by the oscillator was measured to be -110 dBc/Hz @ 3 MHz offset from a 5 GHz carrier.

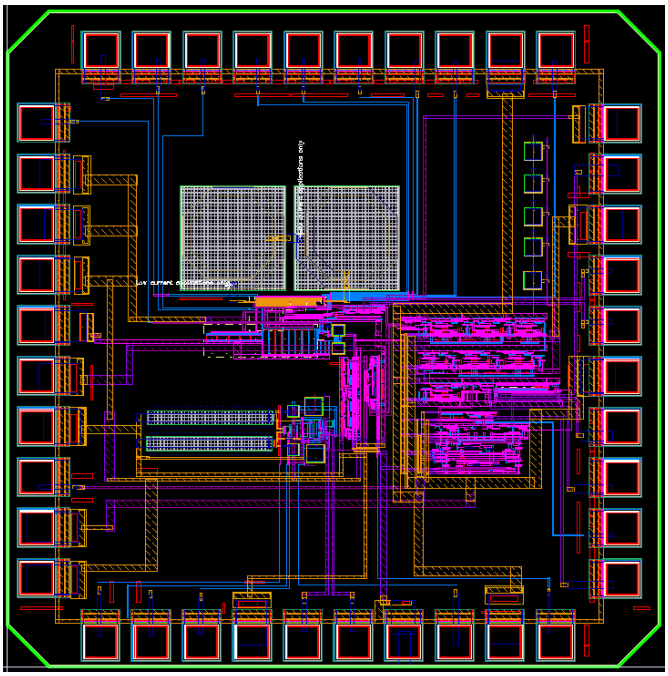

Figure 7.14 Layout diagram of the PLL chip.

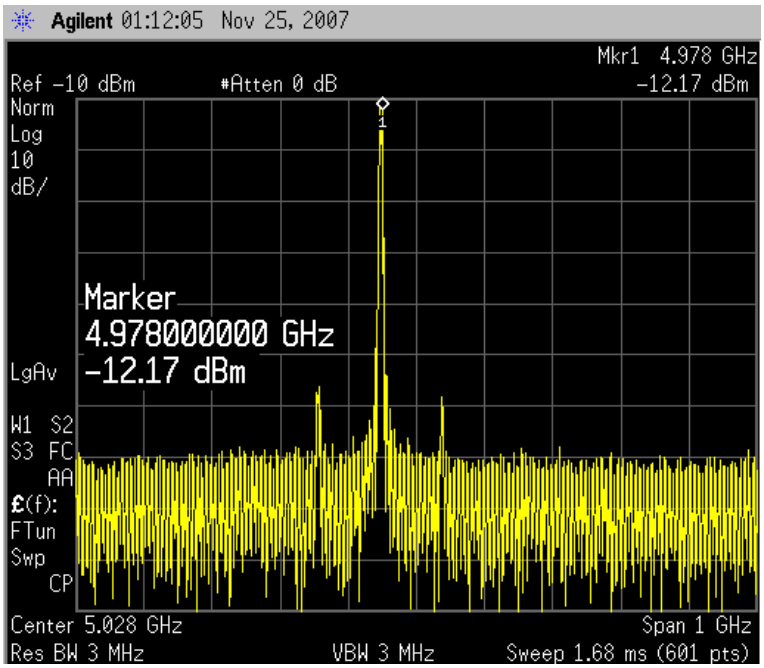

Figure 7.15 Oscillator output spectrum.

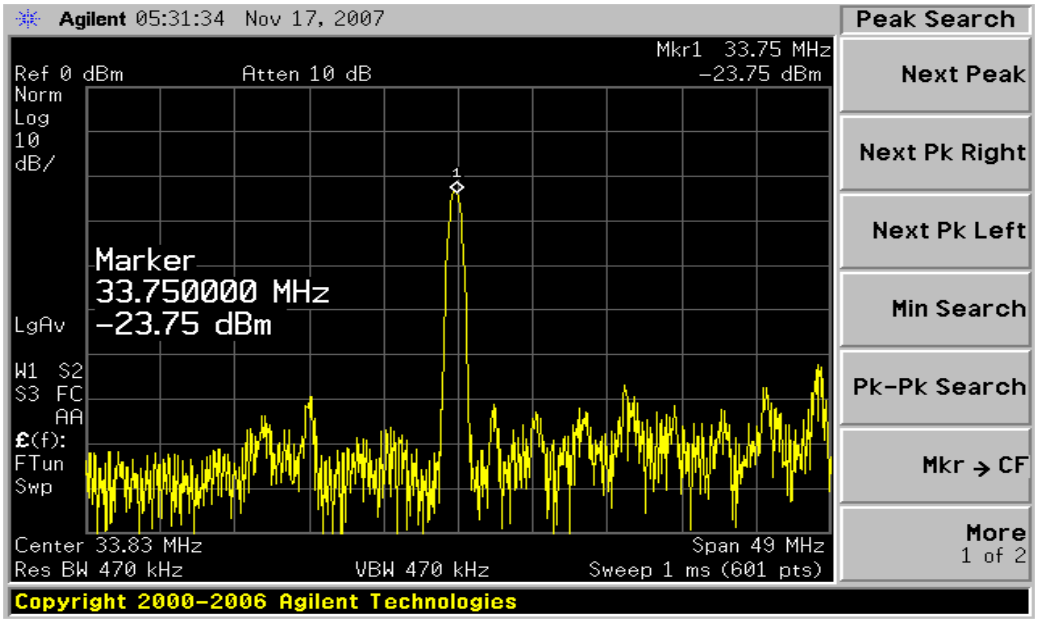

Figure 7.16 Measured divider output.

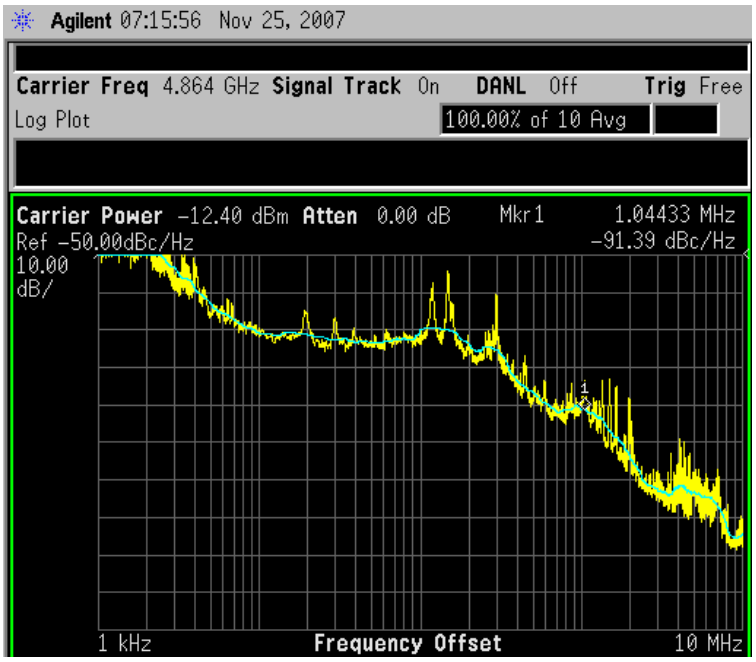

Figure 7.17 PLL output phase noise.

Supply voltage	1.5 V
Oscillation frequency	5 GHz
Output power	-12dBm
In-band noise @ 10 KHz	-70 dBc/Hz
Out-band noise @ 3 MHz	-110 dBc/Hz
Current	122 mA
Area	2.5 mm^2
Divider ratio	128

Table 7.1 Measured performance of the PLL.

7.7 Conclusion

This chapter presented the design of 1.5 V second order charge pump phase locked loop in $0.18\,\mu m$ BiCMOS technology. A single phase 5 GHz NMOS PMOS LC oscillator, phase frequency detector, charge pump and divider designs were presented. The loop exhibits an in-band phase noise of -70 dBc/Hz @ 10 KHz offset and out-band phase noise of -110 dBc/Hz @ 3 MHz offset frequency from a 5 GHz carrier frequency. The reference frequency was provided using a signal generator, causing the in-band phase noise to be slightly high. This chip is due for further testing.

Chapter 8: Conclusion

This dissertation has presented my studies on high frequency silicon based integrated circuits. A 3.5 GHz analog transversal filter was designed in a low cost 47 GHz SiGe technology using amplifiers as delay stages instead of bulky transmission lines. Measured results show that by adjusting the tap coefficients it is possible to adapt zeros at various frequencies up to 3.5 GHz and implement various filter characteristics to mimic the inverse transfer function of communication channels. In depth study of delay in a CML gate has been done and a biasing scheme has been proposed to improve the speed of the CML gate at low bias currents.

Review of phase noise models has been conducted and study of design techniques for LC oscillators has been done. A high speed single phase 25 GHz oscillator has been designed using transmission lines as inductors. The oscillator exhibits phase noise of -82 dBc/Hz @ 500 KHz offset with a figure-of-merit of -162 dBc/Hz. A 1.5 GHz oscillator was implemented for low temperature application and dependence of oscillation frequency with temperature is investigated.

Review of the theory of quadrature signal generation using coupled LC oscillators is done. Novel series coupled quadrature oscillator implemented in a 47 GHz BiCMOS SiGe technology has been presented. The BiCMOS S-QVCO uses NPN for oscillation, NMOS devices for coupling. The oscillator prototype achieves greater than 14% tuning range from 4.3 to 5 GHz, the phase noise of the oscillator is measured as -115 dBc/Hz @

2 MHz offset from the carrier. A 3.5 GHz multiphase oscillator was implemented in 90 nm SOI technology. A single oscillator core was connected in a ring oscillator fashion with 180° phase shift between the first and the last core to generate multiphase outputs.

As an alternative to conventional analog oscillators, a low voltage low power digital controlled oscillator has been designed. Design of a 4.5 GHz 8-bit digitally controlled oscillator using binary controlled varactors in a 120 nm BiCMOS SiGe technology has been presented. The oscillator operates from 1.2 V supply, takes 8-bit CMOS inputs and provides an average frequency resolution of around 2 MHz/bit delivering a good FOM of -177 dBc/Hz. Design of 1.5 V second order phase lock loop was presented. The loop exhibits an in-band phase noise of -70 dBc/Hz @ 10 KHz offset and out-band phase noise of -110 dBc/Hz @ 3 MHz offset frequency from a 5 GHz carrier.

ABBREVIATIONS

BER	Bit Error Rate
BiCMOS	Bipolar-CMOS
CML	Current Mode Logic
CMOS	Complimentary Metal Oxide Semiconductor
CP	Charge Pump
DC	Direct Current
DCO	Digital Controlled Oscillator
DIP	Dual In-line Package
ECL	Emitter Coupled Logic
FD-SOI	Fully Depleted Silicon On Insulator
FIR	Finite Impulse Response
FOM	Figure of Merit
IC	Integrated Circuit
IRR	Image Rejection Ratio
ISI	Inter Symbol Interference
LO	Local Oscillator
LSB	Least Significant Bit
LTI	Linear Time Invariant

MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PFD	Phase Detector
PLL	Phase Locked Loop
P-QVCO	Parallel-Quadrature Voltage Controlled Oscillator
Q	Quality Factor
QVCO	Quadrature Voltage Controlled Oscillator
RF	Radio Frequency
RMS	Root Mean Square
SiGe	Silicon Germanium
SOI	Silicon On Insulator
S-QVCO	Serial-Quadrature Voltage Controlled Oscillator
VCO	Voltage Controlled Oscillator

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