Capacitive Sensors and their Interface Circuits

by

Aditi Rane

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Approved by

Robert Dean, Chair, Assistant Professor of Electrical and Computer Engineering
Thaddeus Roppel, Associate Professor of Electrical and Computer Engineering
John Hung, Professor of Electrical and Computer Engineering

Abstract

An innovative technique has been developed to interface to capacitive sensors. This is a new technique where the unknown capacitance is connected with a resistance to generate a relative change of frequency in a CMOS inverter circuit. This change is proportional to the unknown capacitance. This frequency is then measured using a logical Frequency Locked Loop circuit which is programmed onto a general purpose FPGA board. This technique produces a nearly linear response, is tunable over different capacitance ranges and possesses a fast response time.

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Chapter 1

Introduction

Many types of sensors convert the measurand to a change in capacitance. This is especially true for sensors realized in Microelectromechanical Systems (MEMS) technology, where one or more sets of electrodes respond to a measurand by changing the electrotrode separation distance, relative orientation or overlap area. Some sensors also perform capacitive measurand detection through detecting a change in the permittivity of the dielectric material between one of more sets of electrodes. However, the sensor described here in undergoes a change in capacitance due to an interference in fringing fields.

Many electronic techniques have also been developed to interface to capacitive sensors. In this work, the frequency locked loop (FLL) is used to track frequency variations that are related to the capacitive sensor. A 12-bit FLL is implemented in a field programmable gate array (FPGA) using combinational and sequential logic.

A capacitive fringing field sensor was also developed and tested for measuring the mass of water using Printed Circuit Board (PCB) Technology. This technology is particularly useful for realizing this type of sensor architecture. Interdigitated electrode structures are patterned in the copper cladding on one or both sides of the PCB substrate. An object that interferes with the fringing fields will then change the measurable capacitance between these electrodes. This configuration was used as a sensor for the object (water in this case) that interferes with the fringing fields. This is called a capacitive fringing field sensor. These types of sensors have been used in many applications, such as water detection [1], moisture content measurement [2] and as proximity switches [3].

Chapter 2

Literature Review for Capacitive Sensors and their Interface Circuits

2.1 Capacitive Sensors

A capacitor consists of two conductors separated by a dielectric (solid, liquid, or gas) or a vacuum. The relationship between the charge Q and the difference in voltage V between the conductors is described by capacitance, C

$$C = Q/V \tag{2.1}$$

This capacitance depends on the geometrical design of the conductors and on the dielectric material between them, $C(G, \epsilon)$ where G stands for Geometric Arrangement. For example, for a capacitor formed by n equal parallel plane plates having an overlapping area, A, with a distance, d, between each plate, and an interposed material with a relative permittivity or dielectric constant, ϵ_r, the capacitance is

$$C \approx \epsilon_o \epsilon_r \frac{A}{d}(n-1) \tag{2.2}$$

where $\epsilon_o = 8.85$ pF/m is the dielectric constant for a vacuum. Note that Equation 2.2 ignores fringing effects.

Therefore any phenomenon or quantity producing a variation in ϵ_r, A or d, will result in a change in the capacitance, C, and can be in principle sensed by that device. In general, any change in the dielectric material or in the geometry can be considered for the sensing of the phenomenon producing it. The relative permittivity ϵ_r for air is approximately 1; for water it changes from 88 at 0° C to 55.33 at 100° C [4]. Therefore the substitution of water for air

as dielectric would result in a measurable change in capacitance. This can be applied, for example, to the measurement of the water level in a storage tank or to humidity measurement if a dielectric material is used that absorbs and dissipates water without hysteresis[5].

2.1.1 Spacing Variation

Spacing variation of parallel plates is often used for motion detection if the plate separation distance is much smaller than the square root of the plate area. The parallel plate capacitance formula shows that capacitance is inversely related to the plate separation distance. This yields a conveniently large value of capacitance at small spacing, but it does often require signal conditioning which can compensate for the parabolic capacitance-motion relationship. This can be accomplished by measuring impedance rather than capacitance, as impedance has a linear relationship related to displacement, as suggested in Figure 2.1.

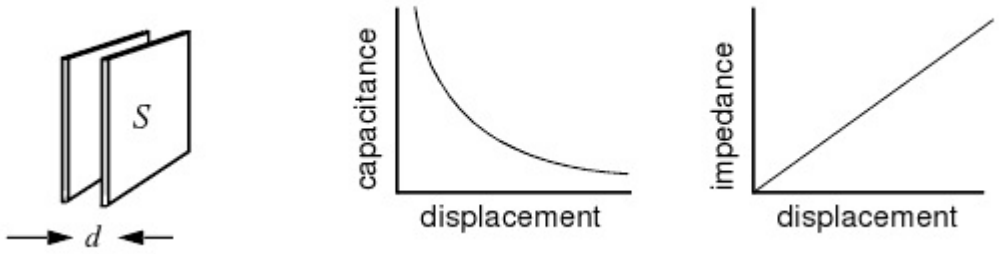

Figure 2.1: Illustration of Plate Spacing Variation

Several sources of nonlinearity corrupt the performance of a simple parallel plate sensor. A simple two-plate Z-axis sensor with same-sized plates will have unwanted sensitivity to [6]-

- Transverse displacement in X or Y axes
- Coupling from the back of the plate
- Tilt of one capacitive plate with respect to the other about the Z-axis

Coupling from the back side can be handled with a shield. The shield needs to be driven by the signal conditioning circuit to the same potential as the sense plate so it does not contribute to the measured capacitance. If, for example, the back plate above is driven by a signal source and the front plate is connected to a low-impedance (virtual ground) amplifier, the shield should be connected to ground. Then, only the interplate capacitance contributes to the amplifier output signal.

Transverse displacement sensitivity is easily handled by the methods illustrated in Figure 2.2. Having two plates of different sizes ensures that the two plates are constantly overlapping, and that any error caused due to XY axis displacement is avoided.

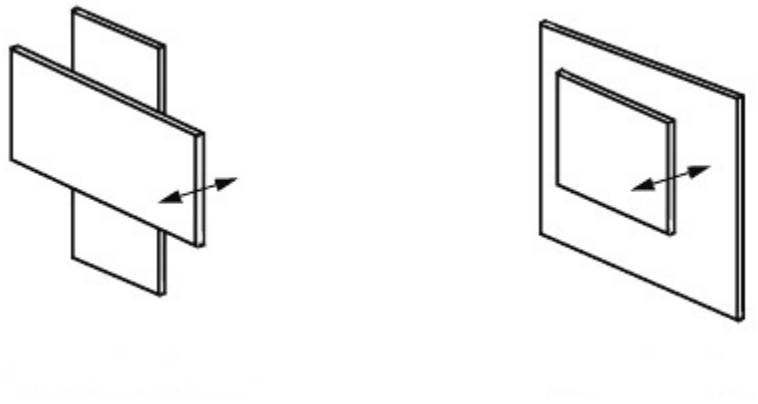

Figure 2.2: Examples of Overlapping Capacitive Plates

2.1.2 Area Variation

In the spacing-variation motion detectors above, when displacement increases to the dimension of the electrodes (considering that they are the same size or are square plates), measurement accuracy suffers from vanishing signal level. Area variation is then preferred. As these plates slide transversely, capacitance changes linearly with motion because the area, A, varies linearly with displacement, d. The impedance variation is of the form $1/d$. Quite long excursions are possible with good linearity, but the gap needs to be small and

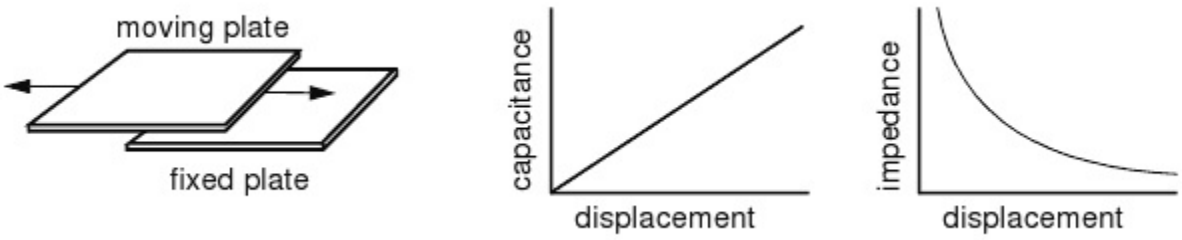

Figure 2.3: Area Variation

well-controlled. As with spacing variation, constant overlapping is needed so that unwanted sensitivities are minimized. Here, the unwanted sensitivities are [6]-

- Tilt in any axis
- Gap change
- Coupling from the back of the plate

Several methods help with tilt sensitivity, such as using a small pickup plate with a chevron-shaped driven plate. The rectangular pickup plate moves laterally above the

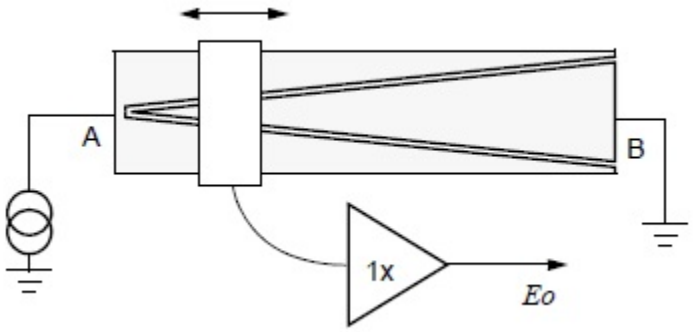

Figure 2.4: Chevron Shape to combat tilt

chevron, and it is spaced with a small (about 0.5 mm) gap. The chevron plates are driven with a signal voltage of, 5V at 100 kHz, and a high-impedance 1X amplifier is used. The amplifier output, Eo, varies linearly from 5V at the left side to 0V at the right side, and the output voltage is insensitive to pickup plate tilt and displacement in the vertical dimension.

2.1.3 Three Plate Systems

Adding a third electrode improves performance in several ways -

- Sensor capacitance is doubled
- Shielding is easier [7]

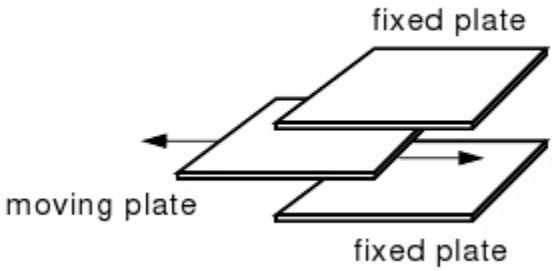

Figure 2.5: Adding a Third Electrode

The three-plate sensor can be used for either spacing-variation or area-variation sensors. With a two-plate sensor, the sensor capacitance is the measured variable. Any circuit which measures this capacitance will produce a ratio of the sensor capacitance to a discrete circuit element, a fixed capacitor or resistor. With three-plate sensors, two capacitances are formed, C_1 between top and center plate and C_2 between center and bottom plate (Fig. 2.5). The amplifier circuit, depending on its configuration, can generate a voltage proportional to $C_1 - C_2$ or C_1/C_2 or $(C_1 - C_2)/(C_1 + C_2)$. This makes ratiometric measurements possible, where one capacitor is variable with motion and the other is fixed. The ratio C_1/C_2 or $(C_1-C_2)/(C_1+C_2)$ can be arranged to track with temperature, for compensating for thermal expansion effects and to compensate for the small changes in air dielectric constants due to changes in humidity or pressure.

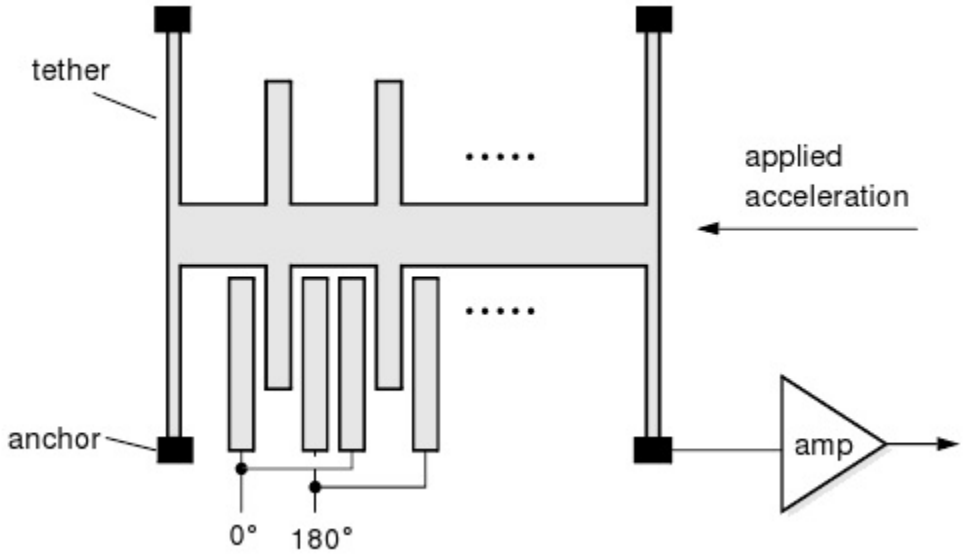

Figure 2.6: Parallel Multiplates

2.1.4 Multiple Plate Systems

The electrode structure of an Analog Devices surface-machined silicon accelerometer, the ADXL50 [8], with an overall size of 500 x 625 μm is illustrated in Figure 2.6. Its 42 silicon fingers are 100 μm in length with a 2 μm gap and a total capacitance of 0.1 pF. The H-shaped piece is elastically mounted using the good spring characteristics of silicon, and responds to acceleration in the X-direction with a small displacement. When this occurs, the common central plate or beam moves closer to one of the fixed plates while moving further from the other. The sensors fixed capacitor plates are driven deferentially by a 1 MHz square wave: the two square wave amplitudes are equal but are 180° out of phase from one another. When at rest, the values of the two capacitors are the same and therefore, the voltage output at their electrical center (i.e., at the center plate) is zero. When the sensor begins to move, a mismatch in the value of their capacitance is created producing an output signal at the central plate. The output amplitude will increase with the amount of acceleration experienced by the sensor. A demodulator (not shown) converts the displacement into acceleration [9]. As the limiting resolution of the sense amplifier is $20 \times 10^{-18} F$, a beam displacement of 20×10^{-12}

m can be measured. Despite the high accuracy of capacitance motion detection, system imperfections such as mechanical tolerance, unwanted tilt sensitivity and thermal noise limit the reasonable performance of a simple analog sensor to about 0.1% accuracy.

2.1.5 2D Sensors

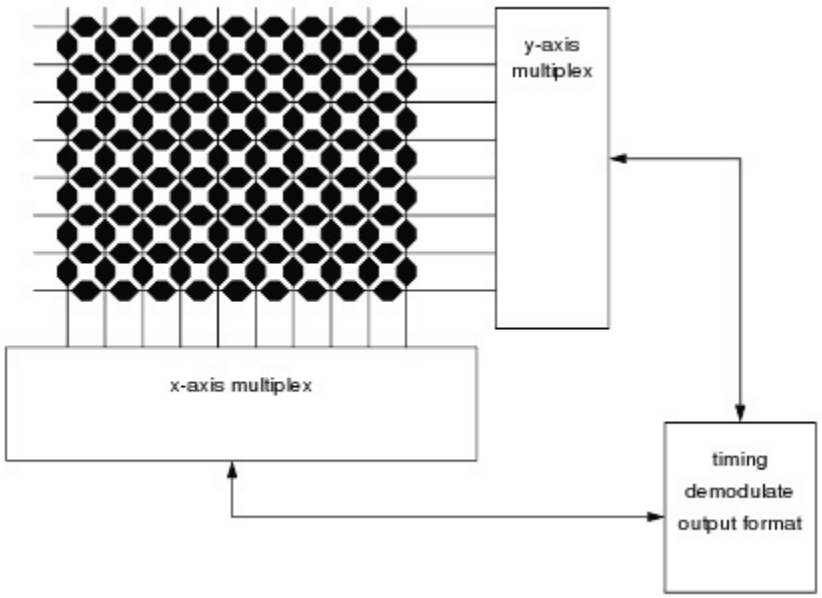

Figure 2.7: Finger Position Sensor [6]

A variety of two-dimensional capacitive sensors have been produced, including the finger-position sensor shown in Figure 2.7. This device, often found just in front of the keyboard on a laptop computer, drives a pulse in succession on each column and measures coupling to each row. By locating the coordinates of peak coupling and interpolating between adjacent rows, the location of a shielding human finger is measured to a fraction of a millimeter.

2.1.6 Sensing of other Variables

Capacitive sensors directly sense electrode motion, conductive or dielectric object motion, or the dielectric properties of a local material. All other variables must be first converted

into one of these. As the technology is capable of excellent, stable, low-noise sensing, this indirect method works well. As an example, a cube of brass one cm square expands sufficiently with temperature to make a good thermometer, with better than 1°C accuracy. The

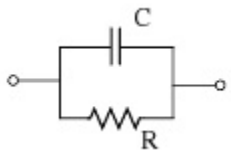

Figure 2.8: Equivalent Circuit

equivalent circuit of a capacitor can be approximated by this circuit, with small series resistance and inductance neglected for high-impedance uses. Good capacitor dielectrics have a very large shunt resistance; polypropylene capacitors have an RC product of over 300 hours [10]. Other materials have a much smaller shunt resistance, sometimes reaching $5 - 10\%$ of the impedance of the capacitor. Although the dielectric constant K of most materials is stable, the shunt resistance or its equivalent, loss tangent (The loss tangent is a parameter of a dielectric material that quantifies its inherent dissipation of electromagnetic energy[11]), may show considerable variation with material properties or with frequency. Water has a high K (80) and a loss tangent which peaks at low frequencies and again at 1010 Hz. With this high dielectric activity, the loss tangent or the dielectric constant of water can be used to detect the moisture content of materials. A characteristic of capacitor dielectrics which may have some use in detecting material properties is dielectric absorption (Dielectric Absorption refers to the inability of a capacitor that has been charged for a long time to completely discharge when briefly discharged[12]). It is measured by charging a capacitor, discharging for 10 s, and measuring the charge which reappears after 15 min. A relatively low-quality dielectric like metallized paper has a dielectric absorption of 10%.

2.2 Capacitive Sensor Interface Circuits

Signal conditioning circuits convert capacitance variations into a voltage, frequency, or pulse width modulation. Very simple circuits can be used, but simple circuits may be affected by leakage or stray capacitance, and may not be suitable for applications with very small capacitance sense electrodes.

2.2.1 Excitation frequency, F

The excitation frequency should be reasonably high so that electrode impedance is as low as possible. Typical electrode impedance is 1-100M ohms. Ideally, the excitation frequency will be high enough to reject coupling to power waveforms and also high enough so that the overall sensor frequency response is adequate; about 50 kHz is usually acceptably high. The frequency should also be low enough for easy circuit design. CMOS switches work well at 100 kHz and below. Excitation waveshape is usually square or trapezoidal, but a triangle waveform can be used to allow a simpler amplifier with resistive feedback and a sine wave offers better accuracy at high frequency. Square wave excitation produces an output bandwidth which can be higher than the excitation frequency by 10x or more, other waveshapes usually result in an output bandwidth 2x or 3x lower than the excitation frequency. Sensors excited with a continuous wave signal usually use synchronous demodulators. This demodulator type offers high precision and good rejection of out-of-band interference.[6]

2.2.2 Oscillator

An R-C relaxation oscillator can be implemented using the IC 555 or its CMOS update, the 7555. This can be used to convert capacitance change into a change of frequency or pulse width. The RC oscillator used with a spacing-variation capacitor will produce a frequency output which is linear with spacing, while an area-variation capacitor is linearized by measuring pulse width. The circuit as shown has no way of accommodating stray capacitance. If, for example, the capacitor is connected by a coaxial cable, the cable capacitance adds to

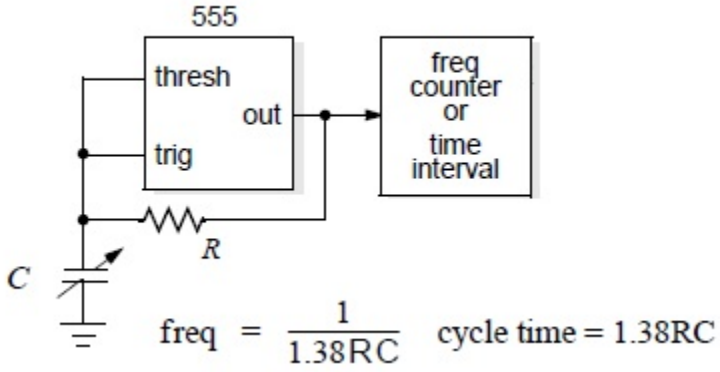

Figure 2.9: RC Oscillator

the measured capacitance and spoils stability and sensitivity. Often a computer can be used to calibrate these errors, but the synchronous demodulator circuits shown below are a more accurate choice.

Another drawback with the RC oscillator is that capacitance is measured relative to the fixed resistor, and the resistor stability and temperature coefficient may not track well. Synchronous demodulators allow the use of capacitance bridges so the reference capacitance temperature coefficient will track accurately, yielding higher accuracy sensors [6]. An example of such a technique is based on the use of a novel type of oscillator whose frequency is insensitive to low and high frequency interfering signals by the application of a third order high-pass filter and special dither techniques [13].

2.2.3 CMOS Schmitt Inverter

This circuit uses a CMOS schmitt inverter as an RC oscillator followed by a oneshot R_1C_1 (with a smaller time constant) followed by lowpass R_2C_2 (with a larger time constant). The output can be either capacitance-linear or 1/capacitance linear, depending on the location of the sense capacitor. It is, unfortunately, not particularly stable with temperature and power supply and it may require a floating sense capacitor [6].

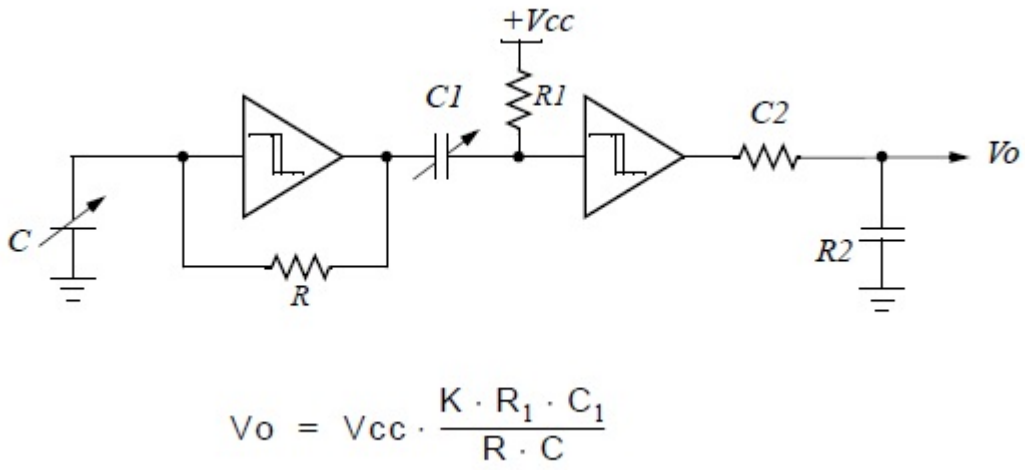

Figure 2.10: CMOS Schmitt Inverter

2.2.4 Synchronous demodulator circuits

A square wave excitation voltage, V, at 5 Vp-p feeds the variable capacitance (C_1, C_2, or both may be variable) and also a CMOS switch. A high-impedance unity-gain AC amplifier feeds the switch directly and also feeds an inverter. If the phase shift through the amplifier is low, the switch output is an accurate demodulation, probably contaminated by narrow spikes caused by switching transients. These transients are eliminated in the lowpass filter. An advantage of the synchronous demodulator is that out-of-band signal components are eliminated in the lowpass filter. This is important in applications where power line harmonics or other crosstalk contaminate the signal [6].

However, apart from these, many techniques have been developed to interface to capacitive sensors. One technique is using a simple digital capacitance meter which utilizes the RC discharge to test the frequency dependence of the capacitor[14]. Another technique is to realize a switched-capacitor interface for capacitive sensors based on a dual-slope analog-to-digital (A/D) conversion technique. The interface consists of a switched-capacitor integrator, a comparator, and digital control circuits. The integrator samples the sensor capacitance in the form of its proportional charge [15]. Also, a single-ended readout circuit is considered,

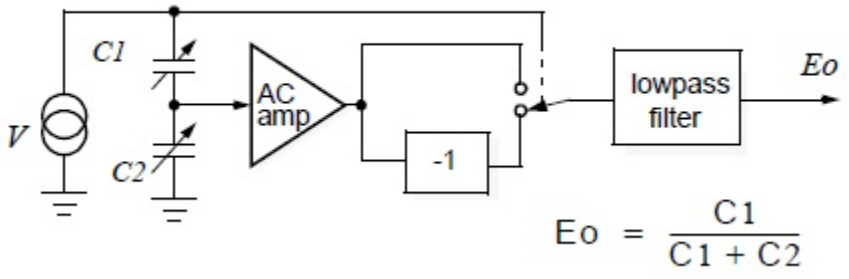

Figure 2.11: Synchronous Demodulator

using an AC-bridge with voltage amplifier [16]. Microcontrollers have also been used in order to measure capacitances by determining the charging and discharging time of an RC Circuit [17], [18]. A charge amplifier, realized using switched capacitor techniques, can be used to measure an unknown capacitance [19]. Other types of switched capacitor circuits are also employed [20].

2.3 Frequency Measurement Techniques

Many physical systems demonstrate cyclic behavior, that is, one or more of their properties vary in a periodic fashion before returning to the initial value and then repeating the cycle. Examples are the angular positions of the planets and satellites in the solar system, the pressure in a cylinder in a reciprocating engine, and the heights and fields associated with surface, acoustic, and electromagnetic waves. The duration of a single cycle, the period, may vary widely. The frequency, which is the inverse of the period, is the number of cycles, including fractions, occurring in unit time. The unit of frequency is the Hertz (Hz), named after Heinrich Hertz, who investigated the nature of electromagnetic radiation. Measurement of the characteristic frequencies of a system, and their variation with time or under changing conditions, yields valuable information on its properties and behavior. Together with temperature and voltage, frequency ranks as one of the quantities most often measured in modern science and technology.

The measurement of an unknown frequency requires a standard producing a fixed, stable, and known frequency, and a system or technique for the comparison of the unknown frequency with that standard. In the past, a wide variety of analog techniques and material standards have been employed. An example is the use of a tuning fork to tune a musical instrument, usually a piano. Analog frequency measurement techniques possessed two major disadvantages:

- The frequency of the standards depended upon the material properties and dimensions of critical components, which meant that they were prone to drift and affected by variations in the ambient temperature.
- In addition, optimum accuracy was achieved only when the unknown and standard frequencies were close or harmonically related.

Developments in electron-tube and later solid-state electronics improved the reliability of this technique. One example is the quartz crystal oscillator, in which a thin slice of crystalline quartz acts as the resonant element in an electronic feedback circuit. As a result of the sharpness of the resonance and the stable properties of the quartz element, this device provides a stable frequency in the range from 10 KHz to 100 MHz and remains the most common secondary frequency standard in use. In addition, a range of circuits were developed to generate more complex harmonic and subharmonic frequencies from a standard source. This led ultimately to the frequency synthesizer which, with an array of phase-locked loops, could be set to produce one of a very wide range of output frequencies. In use, however, it was still necessary to measure the beat or heterodyne frequency from the unknown frequency.

2.3.1 Frequency Synthesizer

A phase locked loop does for frequency what the Automatic Gain Control does for voltage. It compares the frequencies of two periodic signals and produces an error signal which is proportional to the difference between the input frequencies and phases. The error

signal is then low pass filtered and integrated, and used to drive a voltage-controlled oscillator (VCO), which creates an output signal. The output signal is fed through a frequency divider back to the input of the system, resulting in a negative feedback loop. If the output frequency drifts, the error signal will increase, driving the frequency in the opposite direction so as to reduce the error. Thus the frequency and phase are locked to the input signal. This input is called the reference and is derived from a precision crystal oscillator, which is very stable in frequency. The block diagram below shows the basic elements and arrangement of a Phase Locked Loop (PLL) based frequency synthesizer.

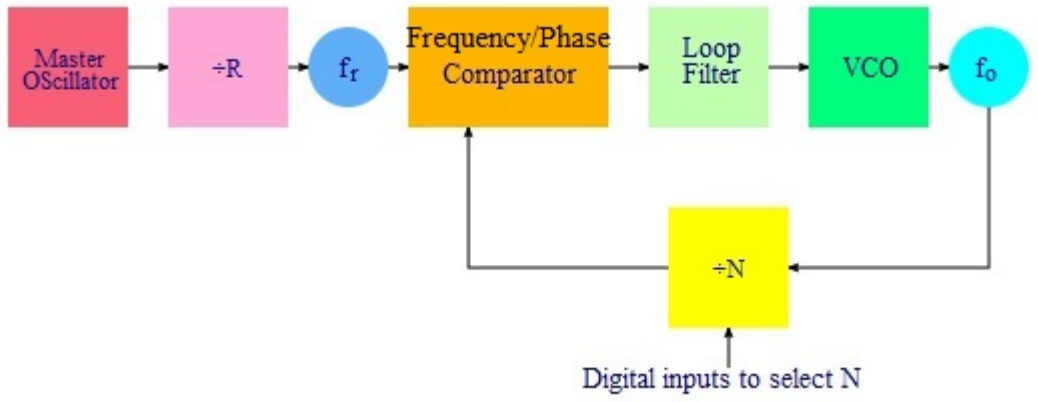

Figure 2.12: PLL based Frequency Synthesizer

The key to the ability of a frequency synthesizer to generate multiple frequencies is the divider placed between the output and the frequency/phase comparator input. This is usually in the form of a digital counter, with the output signal acting as a clock signal. The counter is preset to some initial count value, and counts down at each cycle of the clock signal. When it reaches zero, the counter output changes state and the count value is reloaded. This circuit is straightforward to implement using combinational and sequential logic circuits, and because it is digital in nature, is very easy to interface to other digital components or a microprocessor. This allows the frequency output by the synthesizer to be easily controlled by a digital system [21].

2.3.2 Solid-state Digital Circuits

Fast, inexpensive solid-state digital circuits have replaced analog frequency measurement techniques and many of their associated standards. The underlying principle of the digital technique is simple: the electrical signal from the sensor or transducer observing the physical system under test generally contains, from Fourier analysis, the fundamental frequency and components at integral harmonics of this frequency. It is filtered to select the fundamental component and converted into a rectangular waveform through clipping, representing transitions between the binary logic levels 0 and 1. A frequency measurement then consists of counting the number of positive- or negative-going transitions between the two levels in a known time.

In parallel with the production of counters capable of operating at frequencies up to around 1 GHz, frequency standards based upon selected atomic transitions rather than the properties of bulk materials have been developed. These have the advantage that the frequency produced from a particular transition is in principle universal; that is, it is largely independent of the design of the standard and the materials used in its construction, and of changes in the ambient conditions. The combination of high-speed digital counters and of very stable atomic reference sources allows a wide range of frequencies to be determined simply, inexpensively, and very accurately [22].

Chapter 3

Oscillator Circuits

3.1 Introduction

A relaxation oscillator is an oscillator based upon the behavior of a physical system's return to equilibrium after being perturbed. That is, a dynamical system within the oscillator continuously dissipates its internal energy. Normally the system would return to its natural equilibrium; however, each time the system reaches some threshold sufficiently close to its equilibrium, a mechanism disturbs it with additional energy. Hence, the oscillator's behavior is characterized by long periods of dissipation followed by short impulses. The period of the oscillations are set by the time it takes for the system to relax from each disturbed state to the threshold that triggers the next disturbance.

The Barkhausen stability criterion is a condition to determine when an electronic circuit will oscillate. It was put forth in 1921 by German physicist Heinrich Georg Barkhausen. It is widely used in the design of electronic oscillators, and also in the design of general negative feedback circuits such as op amps, to prevent them from oscillating. Barkhausen's criterion applies to circuits with a feedback loop. Barkhausen's criterion is a necessary condition for oscillation.

It states that if A, is the gain of the amplifying element in the circuit and $\beta(j\omega)$, is the transfer function of the feedback path, so β A, is the loop gain around the feedback loop of the circuit, the circuit will sustain steady-state oscillations only at frequencies for which [24]:

- The loop gain is equal to unity in absolute magnitude, that is, $|\beta A| = 1$,

- There must be a positive feedback i.e., the phase shift around the loop is zero or an integer multiple of 2π: $\angle \beta A = 2\pi n, n \in 0, 1, 2, \ldots$.

Many electronic relaxation oscillators store energy in a capacitor and then dissipate that energy repeatedly to setup the oscillations. There are many kinds of relaxation oscillators that can be implemented. For example, the capacitor can be charged toward a positive power supply until it reaches a threshold voltage sufficiently close to the supply. At that instant, the capacitor can be quickly discharged (e.g., shorted). Alternatively, when the capacitor reaches each threshold, the charging source can be switched from the positive power supply to the negative power supply or vice versa. In all such capacitor-based relaxation oscillators, the period of the oscillations is set by the dissipation rate(s) of the capacitor. Implementations of these two types of relaxation oscillators are shown here, but relaxation oscillators need not be electronic in general. Any oscillator whose oscillations are driven by a system that almost always is dissipating energy may be called a relaxation oscillator [25]. However, this study is limited only to RC relaxation oscillators using CMOS inverters.

3.1.1 LR Relaxation Oscillator

Unlike RC oscillator circuits, which calculate the time constant from the product of resistance multiplied by capacitance, inductor-resistor (L/R) circuits have a time constant determined by the quotient of inductance over resistance. The time constant difference between the two configurations results in corresponding changes in the oscillator circuit response. RC units have a more rapid response when working with low resistance and a slower response with high resistance, while L/R devices offer quicker response with high resistance and slower response with lower resistance. Much like capacitors in RC oscillator systems, the transformers within an L/R oscillator provide cross-coupling and positive feedback. The transformers also have collector windings that are alternately charged from the power supply current and discharged through a series of diodes.

In some types of L/R oscillators, the oscillation frequency is determined by the wire resistance of a collector winding. However, if base resistance drops below a certain level, the oscillation frequency is no longer dependent on the collector winding resistance and instead becomes the function of flux density. This mode of operation benefits from simplicity and can be effective in low-power applications, but the dissipation of base resistance may lead to an overall decrease in efficiency, reducing the accuracy and predictability of the oscillator circuits performance [26].

3.1.2 RC Relaxation Oscillators

Resistor-capacitor (RC) relaxation oscillators are generally produced using operational voltage amplifiers or integrated circuits equipped with timers. When power is applied, the amplifier causes a capacitor to begin charging toward the voltage threshold under a preset time constant. As it reaches half the voltage supply, the amplifier switches operation and the capacitor starts to discharge at the same time constant. This cycle continuously repeats, independent of the supply voltage.

Relying on current sources to charge the capacitor can yield stable triangle waves, but sometimes a low-noise oscillator may be more appropriate for an application, which entails a different design strategy. A simple circuit using an inverter array to form an RC oscillator can produce square waves and reduce sideband noise density to a significant degree. Even lower noise levels can be achieved using an external circuit that modulates output frequency. This arrangement can produce asymmetrical triangle waveforms and have the inverters switch the base drive polarity at each half-cycle interval. While these circuits yield very low sideband noise, they are also more sensitive to voltage supply changes than other types of oscillators [26].

3.1.3 Oscillators using Inverters

A ring oscillator is a device composed of an odd number of inverter gates whose output oscillates between two voltage levels, representing true and false. The NOT gates, or inverters, are attached in a chain; the output of the last inverter is fed back into the first. Because a single inverter computes the logical NOT of its input, it can be shown that the last output of a chain of an odd number of inverters is the logical NOT of the first input. An odd number of inverters connected in a ring can never achieve a stable state, therefore it oscillates, where as an even number is stable. This final output is asserted a finite amount of time after the first input is asserted; the feedback of this last output to the input causes oscillation.

A circular chain composed of an even number of inverters cannot be used as a ring oscillator; the last output in this case is the same as the input. An oscillator only requires power to operate; above a certain threshold voltage, oscillations begin spontaneously. To increase the frequency of oscillation, two methods may be used. Firstly, the applied voltage may be increased; this increases both the frequency of the oscillation and the power consumed, which is dissipated as heat. The heat dissipated limits the speed of a given oscillator. Secondly, an oscillator with fewer inverters may be fabricated; this results in a higher frequency of oscillation given a certain power consumption [27].

3.2 Experimental Validation

There were two adaptations of an RC Inverter Circuit that were bread-boarded and tested. A variable capacitor that ranged approximately from 8pF to 128pF was used. The oscillator circuits were connected to an oscilloscope, where the change in frequency by varying the capacitance, C and the resistance, R was measured. An LCR meter was also used to measure the change in capacitance and resistance. A power supply was also used to power up the IC chip. A block diagram of this setup is shown in Fig. 3.1.

The layout of the first circuit is shown in Figure 3.2.

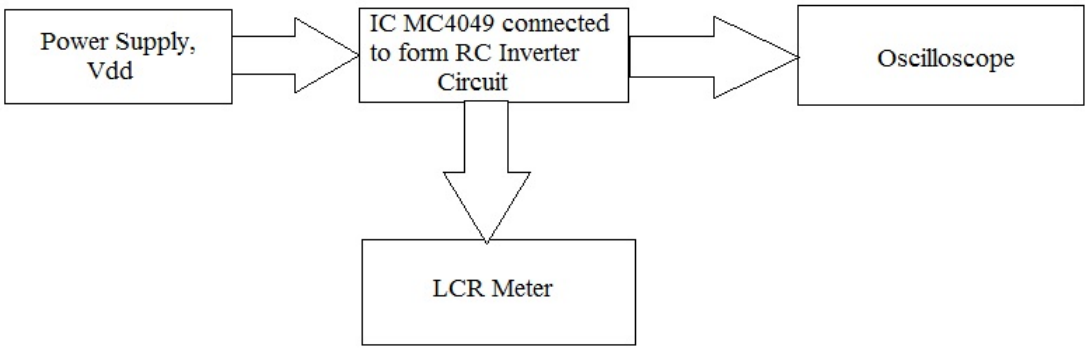

Figure 3.1: Block Diagram of Experimental Setup

The equation of the Frequency for this circuit in terms of the Resistance and Capacitance is-

Assumptions-

- $V_{dd} = 5V$
- $V_{th} = \frac{V_{dd}}{2}$

$$T = \frac{1}{f} = RC \ln\left(\frac{V_{dd}^2}{V_{th}(V_{dd} - V_{th})}\right) [28]$$

Therefore,

$$\begin{aligned} f &= \frac{1}{RC \ln\left(\frac{25}{2.5 \times 2.5}\right)} \\ &= \frac{1}{1.386RC} \\ &= \frac{0.721}{RC} \end{aligned} \tag{3.1}$$

The results were also obtained in terms of frequency by using the capacitance, C and resistance R as variables (Table 3.1).

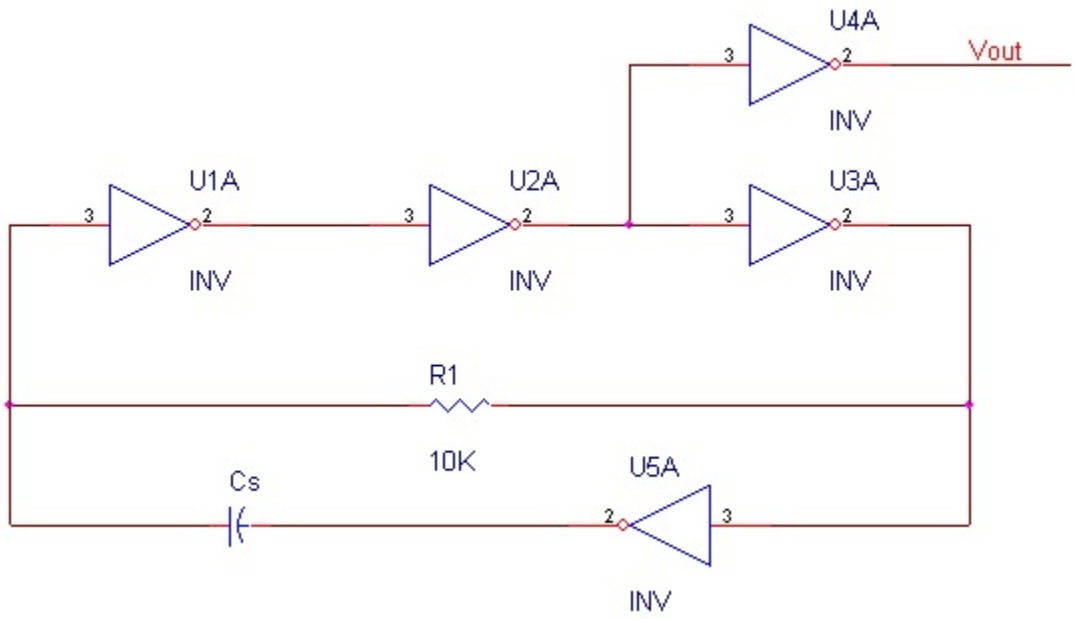

Figure 3.2: RC Inverter Oscillator Circuit 1

Capacitance (in pF)	R=1.5KΩ	R=5KΩ	R=10KΩ	R=47.7KΩ	R=75KΩ
5	2674	1724	1250	450.5	312.5
8	2294	1351	909.1	282.5	185.2
29	1706	832.9	540.5	150.2	99.01
48	1393	684.9	454.5	109.9	71.94
67	1250	609.8	357.1	90.09	58.82
86	1134	531.9	312.5	76.69	49.75
106	1027	476.2	277.8	68.03	44.25

Table 3.1: Variation of Capacitance and Resistance in terms of Frequency (in KHz)

The experimental data was used to plot a graph (Figure 3.3) depicting the frequency change. This plot is most helpful, as it can be used to select a particular value of resistance for any given capacitive sensor. The ideal frequency range should be between 100KHz and 1MHz as there is a considerable amount of distortion over frequencies of 1MHz.

Snapshots from the oscilloscope Frequency Readout are shown in Figures 3.4, 3.5 and 3.6.

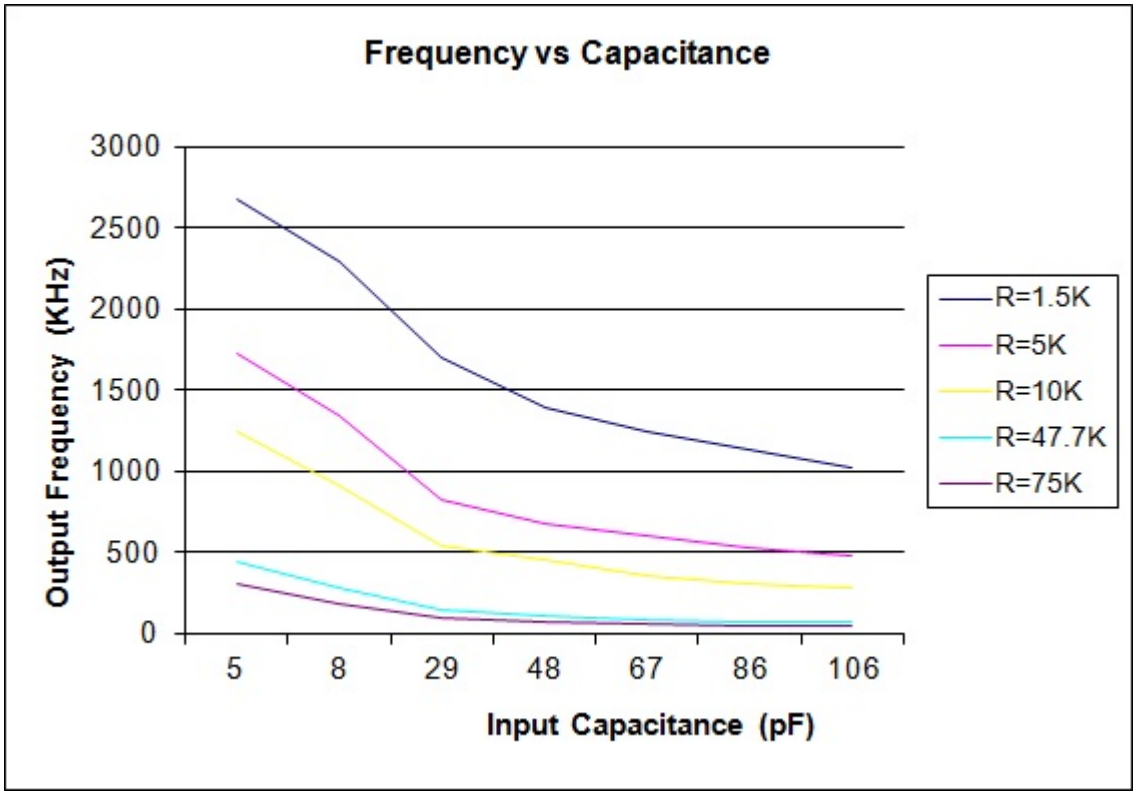

Figure 3.3: Frequency vs Capacitance

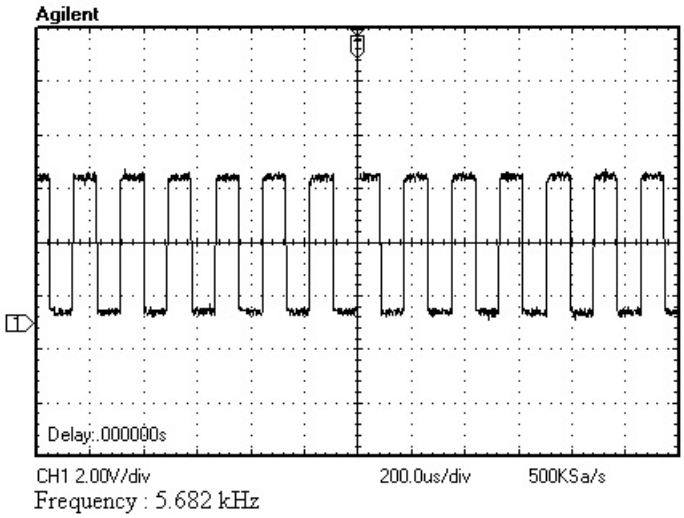

Figure 3.4: Output Frequency at C=1pF

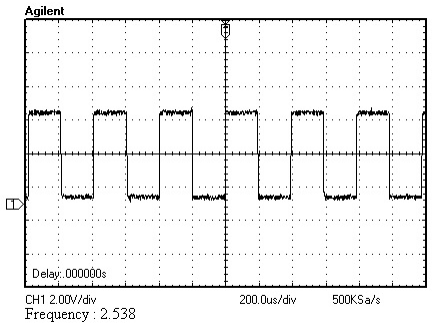

Figure 3.5: Output Frequency at C=15pF

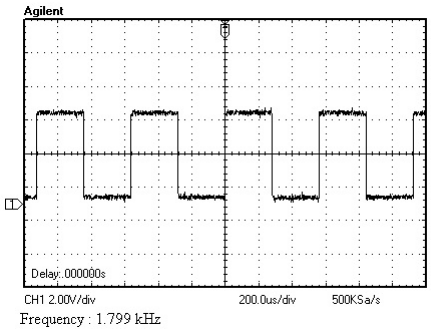

Figure 3.6: Output Frequency at C=28pF

Similarly, the second circuit that was tested is shown in the Figure 3.7.

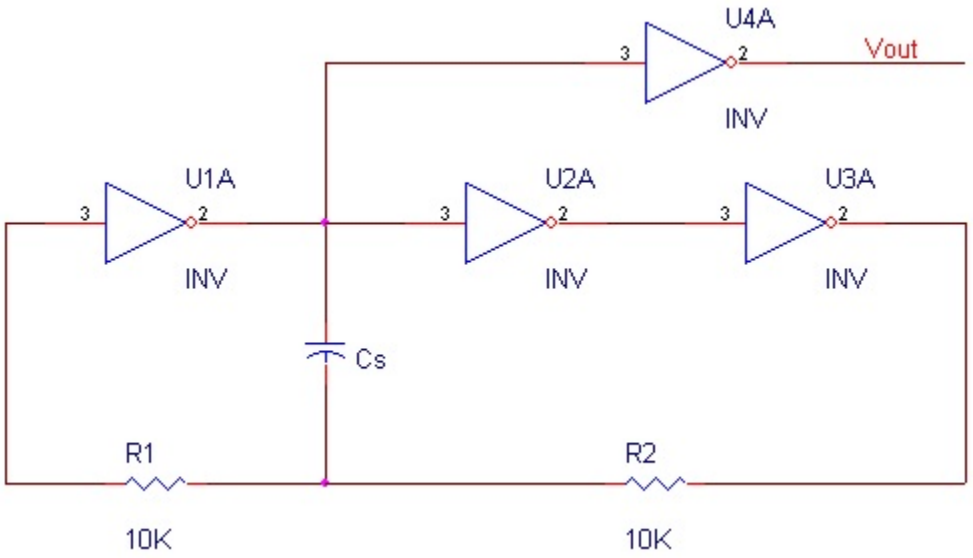

Figure 3.7: RC Inverter Oscillator Circuit 2

Equations for the frequency in terms of Resistance and Capacitance were mathematically calculated for this circuit as well-

Assumptions-

- Capacitance, C $\gg$ Input Capacitance of an Inverter
- Each inverter is "fast"
- The inverter trip voltage = $\frac{V_{dd}}{2}$

Hence, when $V_o = \frac{V_{dd}}{2}$ the system changes states. Therefore, RC time constant, τ determines f_o. Let

$$V_{dd} = 5V$$
$$\frac{V_{dd}}{2} = 2.5V$$

At switching time,

$$\frac{V_o}{V_s} = \frac{R}{s + \frac{1}{sC}} = \frac{s}{s + \frac{1}{RC}}$$
$$V_s(s) = \frac{7.5}{s}$$

Therefore,

$$V_o(s) = V_s(s)\left(\frac{s}{s + \frac{1}{RC}}\right) = \frac{7.5}{s + \frac{1}{RC}}$$
$$V_o(s) = 7.5e^{\frac{-t}{RC}} \tag{3.2}$$
$$\tag{3.3}$$

To find the value of t when

$$\begin{aligned} V_o(t) &= 2.5V \\ 2.5 &= 7.5e^{\frac{-t}{RC}} \\ t &= -RC\ln\left(\tfrac{2.5}{7.5}\right) = 1.0986RC \\ T &= 2t \rightarrow f = \tfrac{1}{2t} = \frac{0.455}{RC} \\ f &= \tfrac{0.455}{RC} \end{aligned} \tag{3.4}$$

This circuit was bread-boarded using the CMOS inverter chip MC4049, and the testing results (Table 3.2) were used to obtain a plot that would show the Frequency vs Capacitance

Capacitance (in pF)	R=1.5KΩ	R=5KΩ	R=10KΩ	R=47.7KΩ	R=75KΩ
8	2128	1471	751.9	249.4	169.5
20	1786	1111	581.4	163.9	109.9
45	1408	746.3	395.3	98.04	64.1
70	1190	606.1	298.5	74.63	49.02
90	1050	510.2	260.4	62.89	40.98
110	952.4	448.4	227.8	54.64	35.34
128	877.2	403.2	208.8	48.78	31.45

Table 3.2: Variation of Capacitance and Resistance in terms of Frequency (in KHz)

for different values of Resistance (Fig. 3.8). This circuit showed distortion for frequencies over 1 MHz as well. Snapshots from the oscilloscope Frequency Readout are shown in Figures 3.9, 3.10 and 3.11.

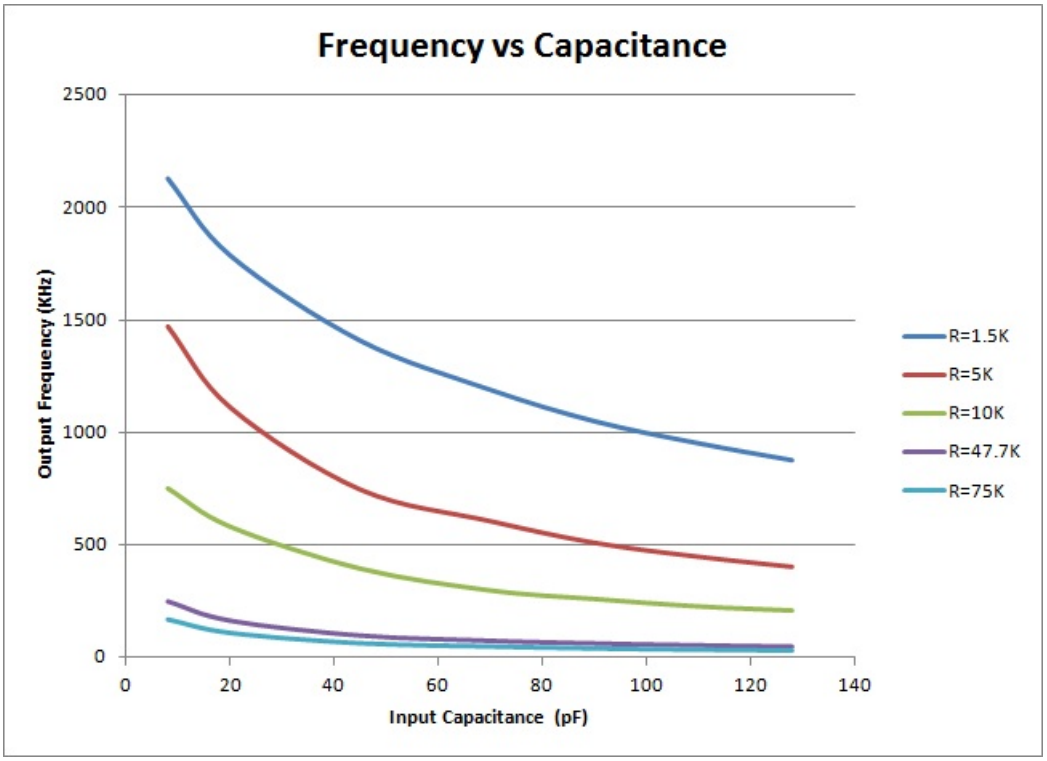

Figure 3.8: Frequency vs Capacitance

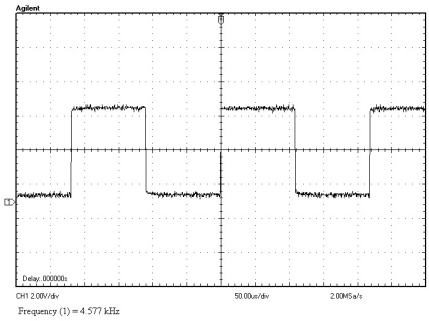

Figure 3.9: Output Frequency at C=1pF

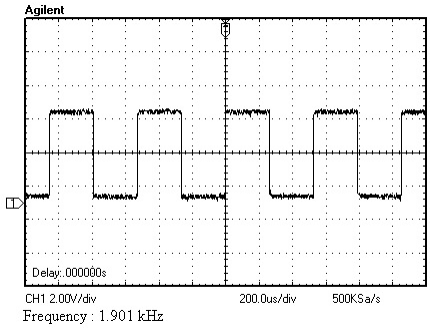

Figure 3.10: Output Frequency at C=15pF

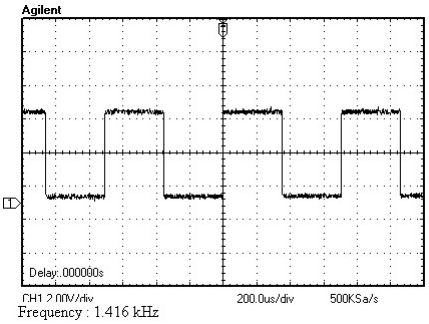

Figure 3.11: Output Frequency at C=26pF

3.3 Layout and Design

3.3.1 PCB Layout

Standard printed circuit boards (PCBs) consist of a dielectric substrate that has conductive traces on at least one surface that are used for electronic component attachment and electrical interconnection. If a PCB has traces on only one side, it is called a single-sided or a single layer board. If the PCB has traces on both sides, it is called a double-sided or a 2-layer board. A PCB with additional internal layers of traces is called a multilayer PCB. The substrate can be rigid, flexible or in-between (semi-flex). FR-4 is a commonly used rigid PCB substrate material and consists of one or more layers of woven glass cloth, typically E-glass, held together by an epoxy-resin. Rigid PCB's have a fairly large range of thicknesses, from tens of mils to over 100 mils. For example, 62mils is a typical thickness for a rigid PCB. The electrical traces are usually made by patterning a solid Cu foil layer.

Typical thicknesses for the Cu foil are 0.5 oz (0.7mils), 1.0 oz (1.4mils) and 2 oz (2.8mils). Traces can have minimum feature sizes as small as a few mils. Except for the portions of the traces that will be soldered to attached devices, the rest of the exposed surface of the PCB is usually coated with a polymeric material called solder mask. The primary purpose of the solder mask is to limit the flow of solder during the soldering process. Since Cu quickly oxidizes, which can make soldering difficult, the exposed Cu traces are usually plated with a surface finish such as Sn. Traces on different layers of the PCB can be electrically connected using plated through-holes. An illustration of a cross-section of a 2-layer PCB is presented in Figure 3.12.

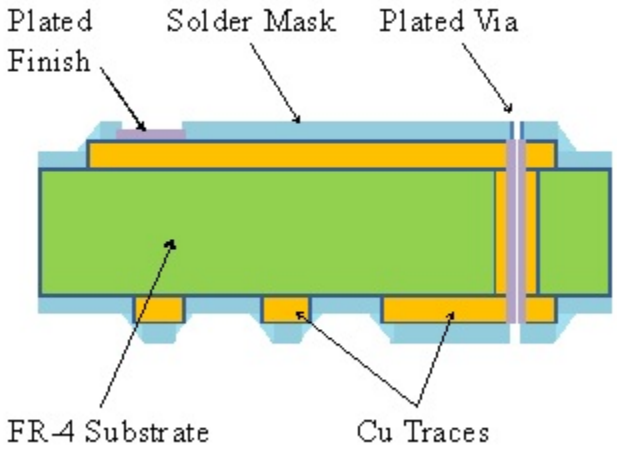

Figure 3.12: Cross Section of a two-layer PCB

Two relaxation oscillator circuits were implemented into a single PCB board. The layout for both the circuits was done using ViewMasterEz software. For the first circuit, a resistance of 10KΩ was selected for use along with a variable capacitor of 2-20pF using the graph in Fig. 3.3. The frequency range would then be approximately equal to 270KHz to 1.25MHz which would would minimize high frequency induced distortion.

The layout of the circuit in ViewMasterEZ is as shown in Fig. 3.13. The blue traces shown are part of the copper layer. These are the interconnects and the wiring for the circuit. Also, the pads on the layout are where the components are soldered to. On top of the copper

layer is the solder mask layer. The red traces are ones that are on the back side of the the PCB board and are connected to the components on the board using vias. A DPDT (Double Pole Double Throw) switch is also used so that the variable capacitance can be measured at any point of time by shifting the position of the switch.

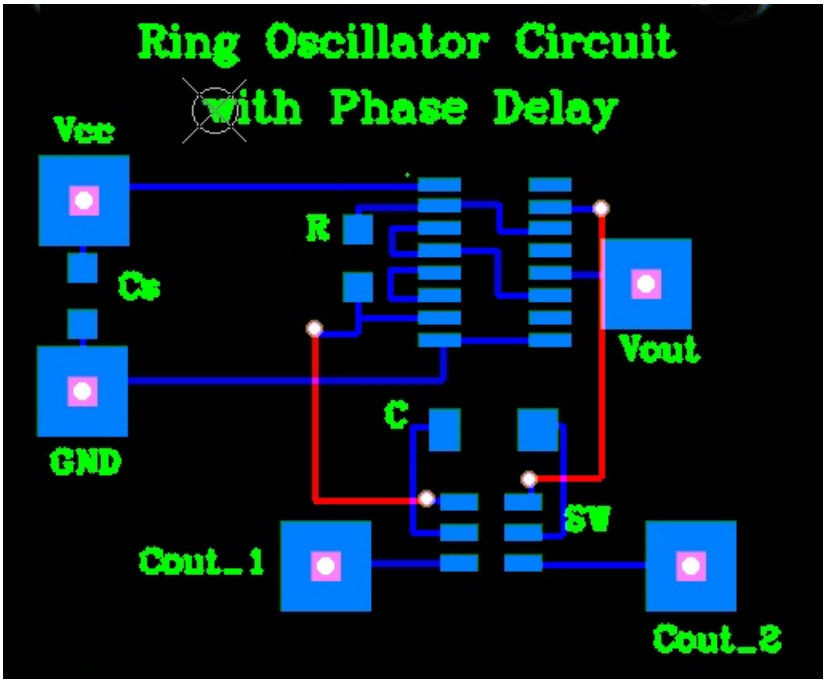

Figure 3.13: PCB Layout of Circuit 1 in ViewMasterEZ

For the second circuit, the two resistances were both selected to be 10KΩ by utilizing the Graph in Fig. 3.8. The capacitance was selected to range from 2-20pF. This gives an approximate frequency range of 200KHz to 750KHz. This circuit was laid out in the same manner as the first, with similar layers. It also used a DPDT switch as well. The layout of the circuit in ViewMasterEZ is as shown below in Fig. 3.14.

3.3.2 PCB Board with Components

All the components that were chosen earlier were hand soldered on to the board. The board was then ready for testing. As seen in the figure, the PCB consists of two oscillator circuits each with its own variable capacitor and DPDT switch.

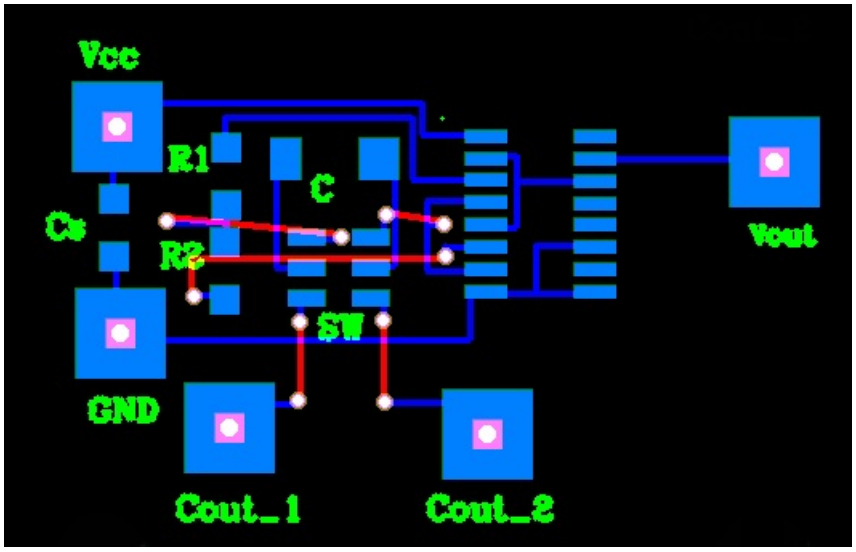

Figure 3.14: PCB Layout of Circuit 2 in ViewMasterEZ

Figure 3.15: Completed PCB

Chapter 4

Frequency Locked Loop Prototype

4.1 Theory and Prototyping

4.1.1 Introduction

A frequency-locked loop (FLL) is a negative feedback circuit that generates a square wave that is frequency locked, but not phase locked, with an input square wave. Since logic level square waves are input and output, the circuit can be realized in sequential and combinational logic. Therefore the FLL has a finite resolution and the generated square wave dithers around the frequency of the input square wave. A frequency-locked loop is an example of a control system using negative feedback. A frequency locked loop is composed of a frequency comparator, an up down counter, a synchronous counter and a logical comparator. The FLL produces a square wave signal that dithers in frequency around the input square wave. Its digital output signal is a digital representation of the frequency of the input square waver, with a 1/f response. The FLL can be realized using just combinational and sequential logic circuits. 4-bit, 8-bit and 12-bit FLL circuits were implemented in a XC3030A Xilinx FPGA and tested. The block diagram in Fig. 4.1 shows the various stages of the FLL circuit.

4.1.2 FLL Components

Frequency Comparator

The frequency comparator operates by comparing the state changes between the input square wave and the FLL output square wave. If either one has two state changes before a state change occurs in the other signal, the frequency comparator identifies this as a difference

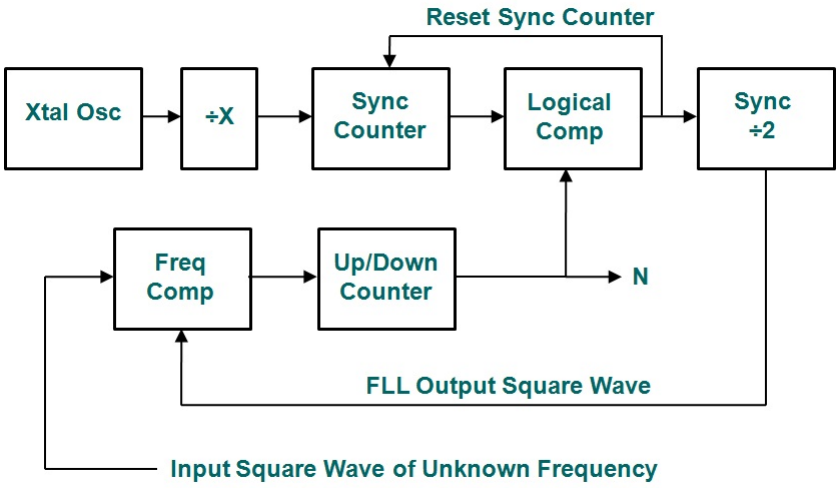

Figure 4.1: Block Diagram of FLL

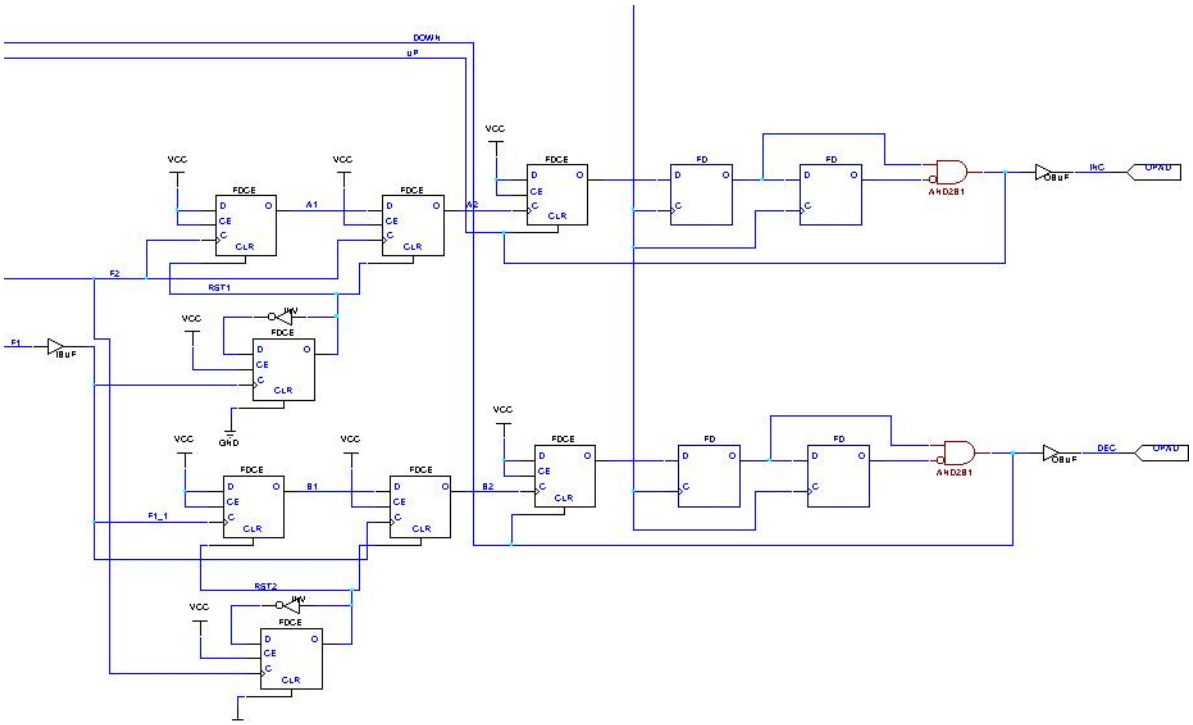

Figure 4.2: Frequency Comparator

in frequency. It then instructs the up/down counter to increment or decrement accordingly to reduce the difference in frequency between the two square waves.

Up/Down Counter Circuit

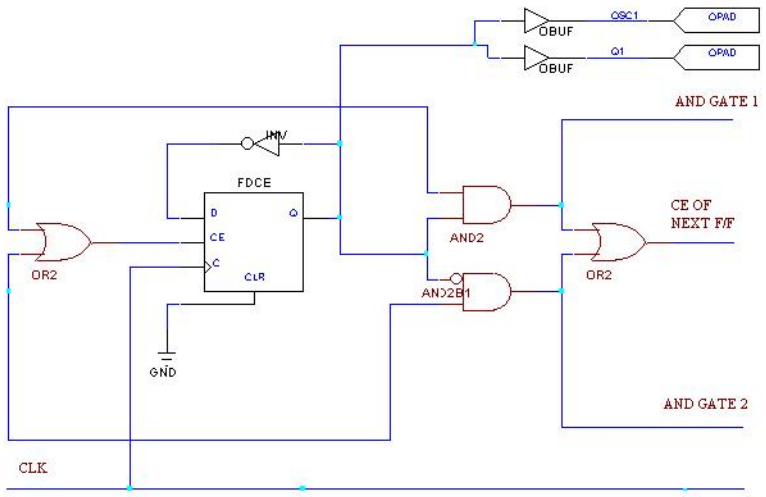

Figure 4.3: Up/Down Counter Circuit

A negative feedback loop was implemented in the FLL to minimize the error between the frequency of the input square wave and the FLL output square wave. The output from the Frequency Comparator was used to increment or decrement the up/down counter to change the factor N by which the high frequency clock signal was divided to produce the FLL output square wave. This continous feedback results in the output of the circuit slowly reaching a point where it is similar to or the same as the input given its resolution. Since the digital FLL has a finite resolution, after it reaches this state, it dithers around the frequency of the input square wave. A single unit of this Up/Down Counter Circuit is shown in Figure 4.3. If these units are added in a sucession to form a series, along with a feedback control, it will be able to adjust to the input frequency. The higher the number of bits, the higher the resolution of the frequency would be.

Synchronous Counter

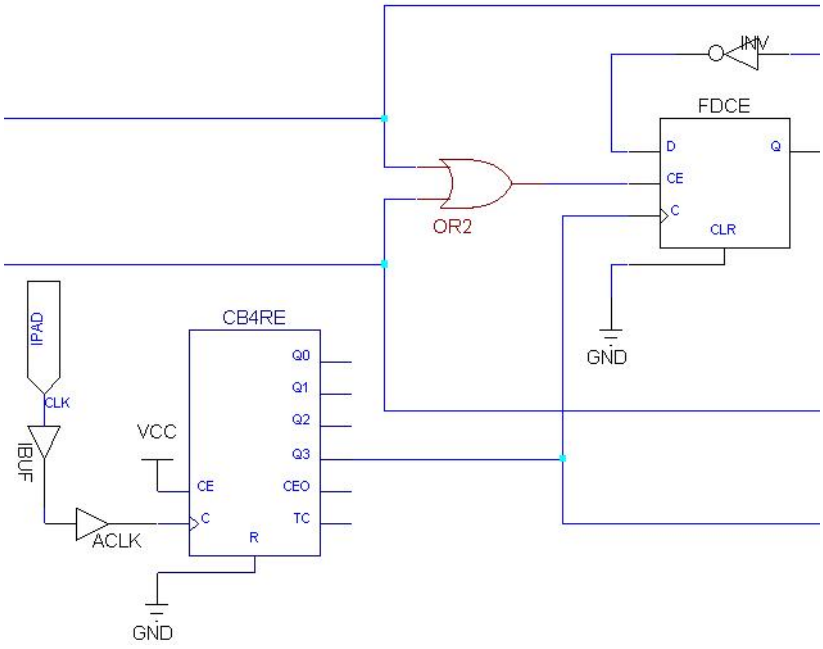

Figure 4.4: Synchronous Counter at Input

There were two synchronous counter chips that were used in the entire circuit. One of them was used to change the input clock frequency and divide it down by 16. The on board crystal oscillator frequency was about 10 MHz which was too high for this application. The output of the other counter was connected to the logical comparator. (Figures 4.4 and 4.5)

Logical Comparator

A comparator is a device which compares two voltages or currents and switches its output to indicate which is larger. A logical comparator circuit was used to divide the high frequency clock produced by the crystal oscillator by N to produce the FLL output square wave signal. It compared the output from the synchronous counter driven by the high frequency clock with the output of the up/down counter. When the two digital words were logically equal, its output went high, which reset the synchronous counter on the next rising edge of the high frequency clock. By using a one stage flip flop divide-by-two circuit,

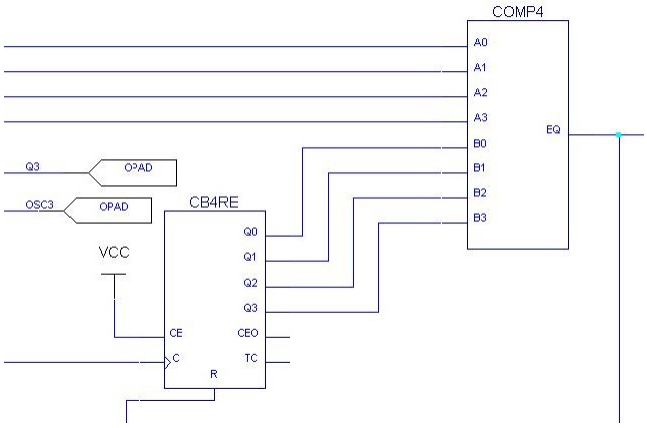

Figure 4.5: Synchronous Counter connected to Comparator

two of these comparator cycles produced one period of the FLL output square wave. (Refer to Fig. 4.6)

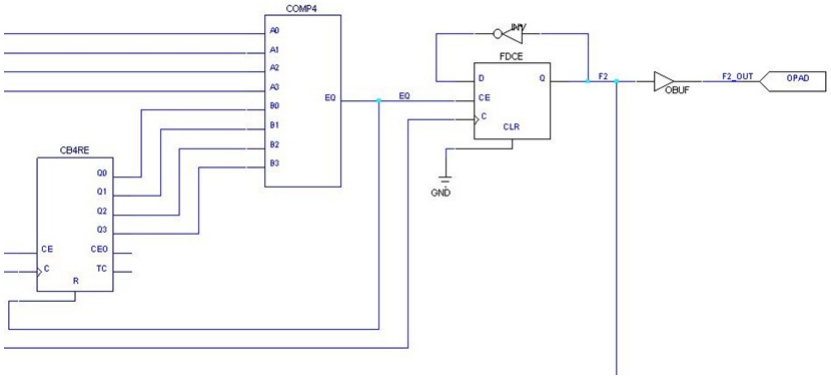

Figure 4.6: Logical Comparator

4.1.3 FLL Circuit Prototype

Implementation in the Xilinx FPGA

A field-programmable gate array (FPGA) is an integrated circuit designed to be configured by the customer or designer after manufacturing, hence "field-programmable". The FPGA configuration is generally specified using a hardware description language (HDL).

FPGAs contain programmable logic components called "logic blocks", and a hierarchy of reconfigurable interconnects that allow the blocks to be "wired together" somewhat like a one-chip programmable breadboard. Logic blocks can be configured to perform complex combinational functions, or merely simple logic gates like AND and XOR. In most FPGAs, the logic blocks also include memory elements, which may be simple flip-flops or more complete blocks of memory [29].

For implementation of the logic circuit, a Xilinx XC3030A FPGA chip was selected. A general-purpose FPGA board was designed for this chip. It consisted of a parallel port interconnect, 12 testing LEDs, 12 output pins, a 10MHz crystal oscillator and an EE-serial PROM insert. The EEPROM stored the FPGA configuration code used to program the FPGA when the power is first turned on. It was programmed using the ATMEL ATDH2200 FPGA Configurator and SEEPROM Programmer board. It was first plugged into this board, and using the parallel port (Fig. 4.10 and Fig. 4.11), and the ATMEL computer program (Fig. 4.12), the circuit layout data was programmed into it.

Circuit Design

Xilinx Foundation Series Schematic layout software was used to integrate all the various parts of the FLL. The simulation in the same was then used for the first tests. The output of the circuit was checked against the input of the FLL. As predicted, the output closed in towards the input frequency over multiple clock cycles till both were the same in frequency. Figures 4.7 through 4.9 show the FLL implemented in various resolutions.

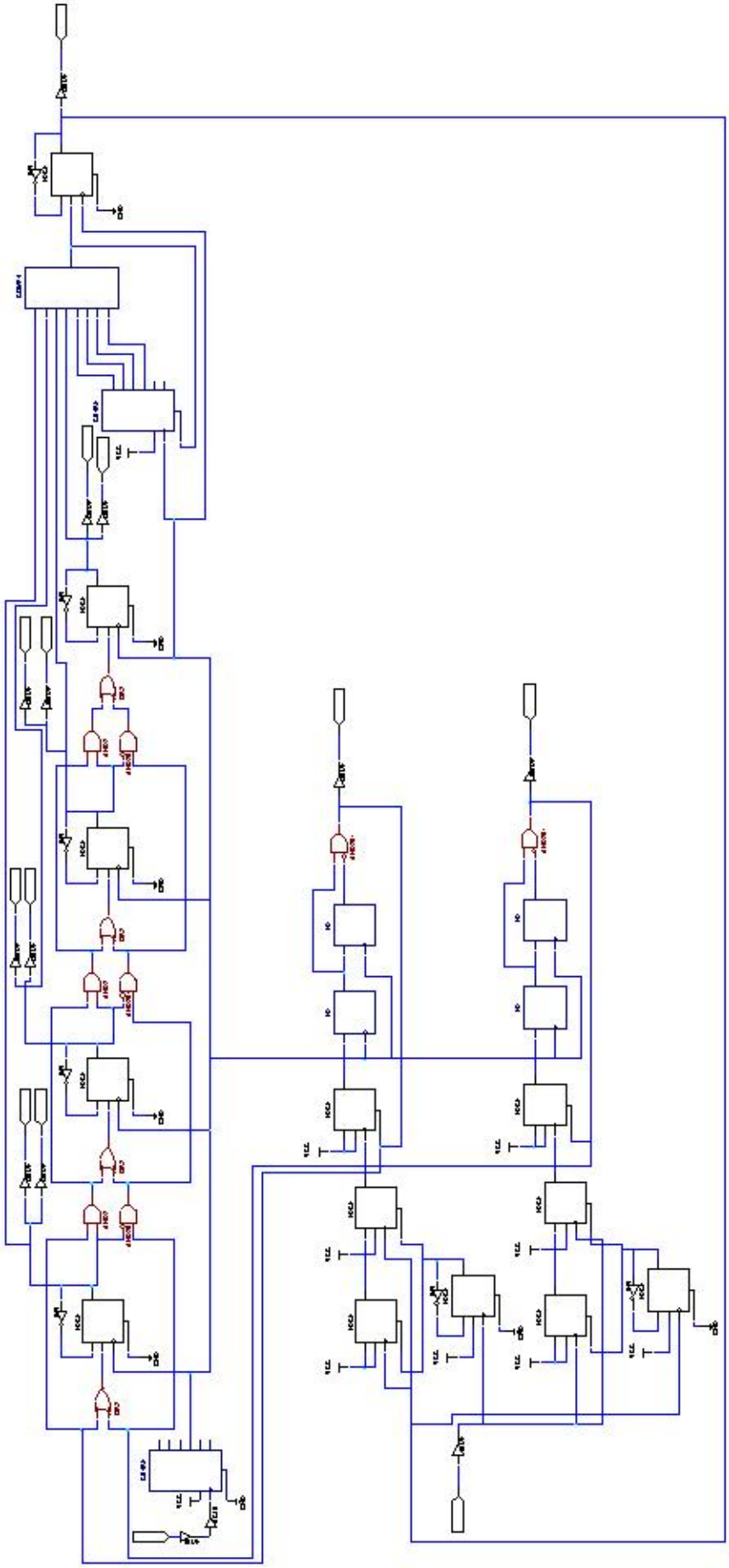

Figure 4.7: A 4-bit FLL circuit

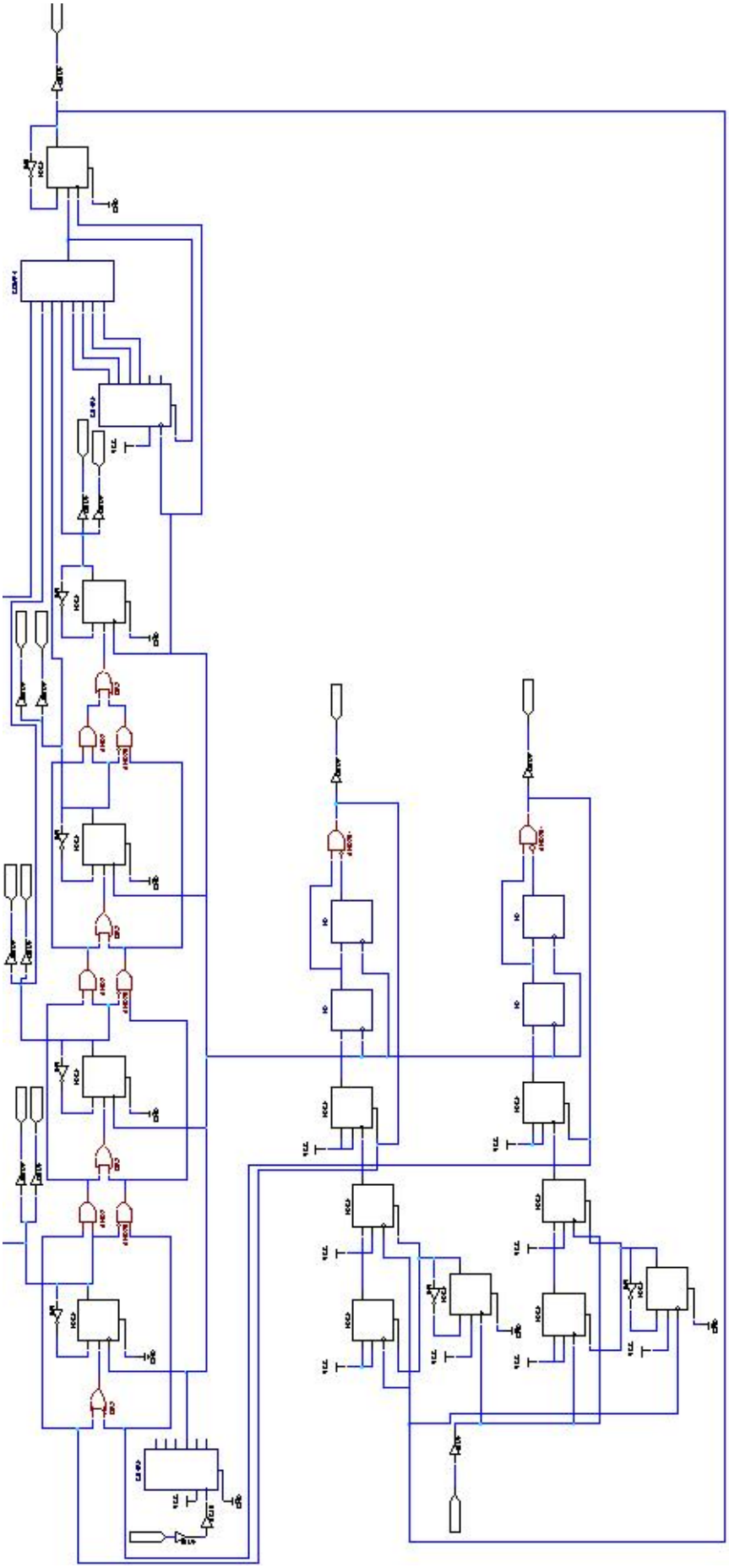

Figure 4.8: An 8-bit FLL circuit

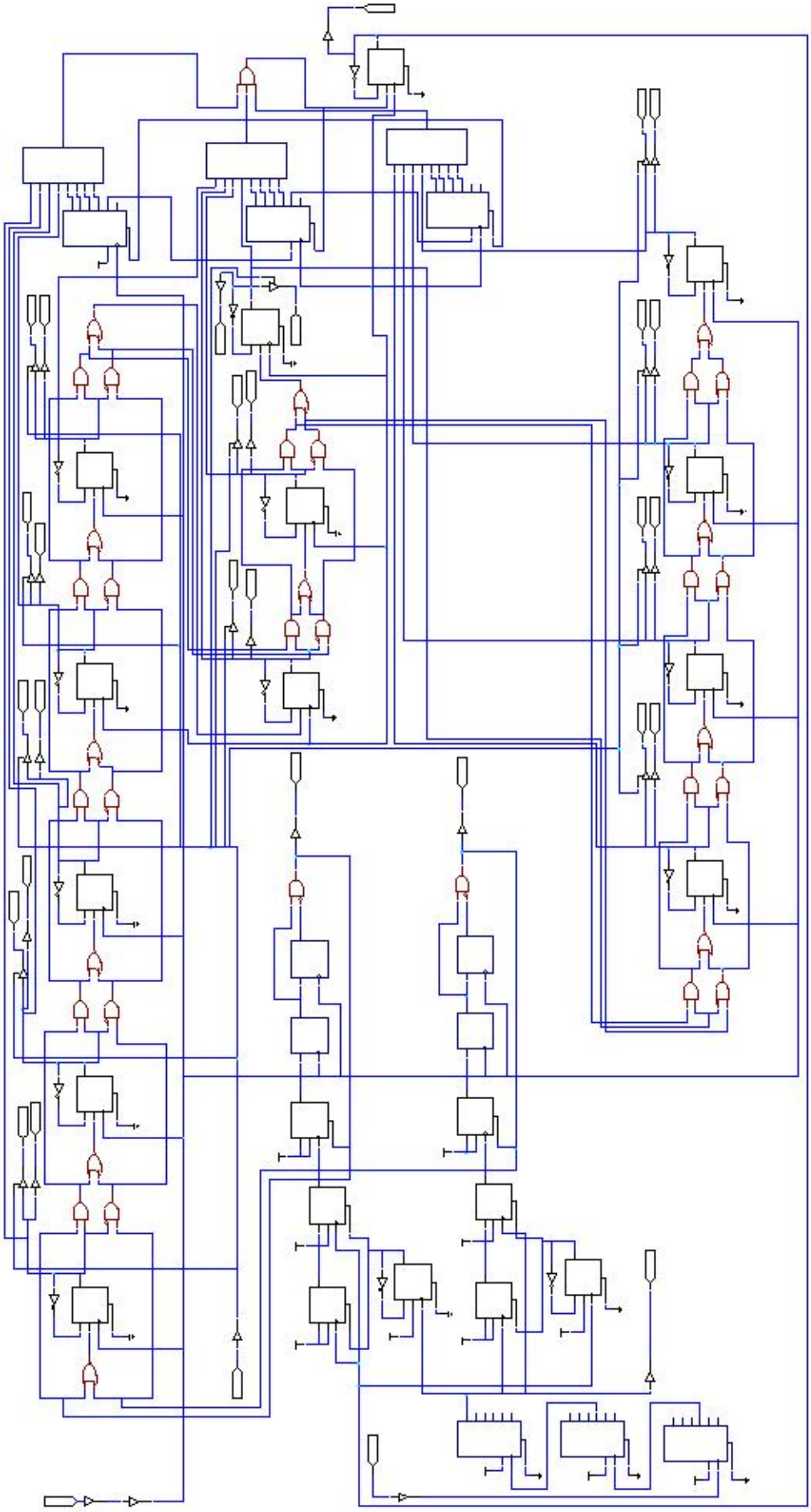

Figure 4.9: A 12-bit FLL circuit

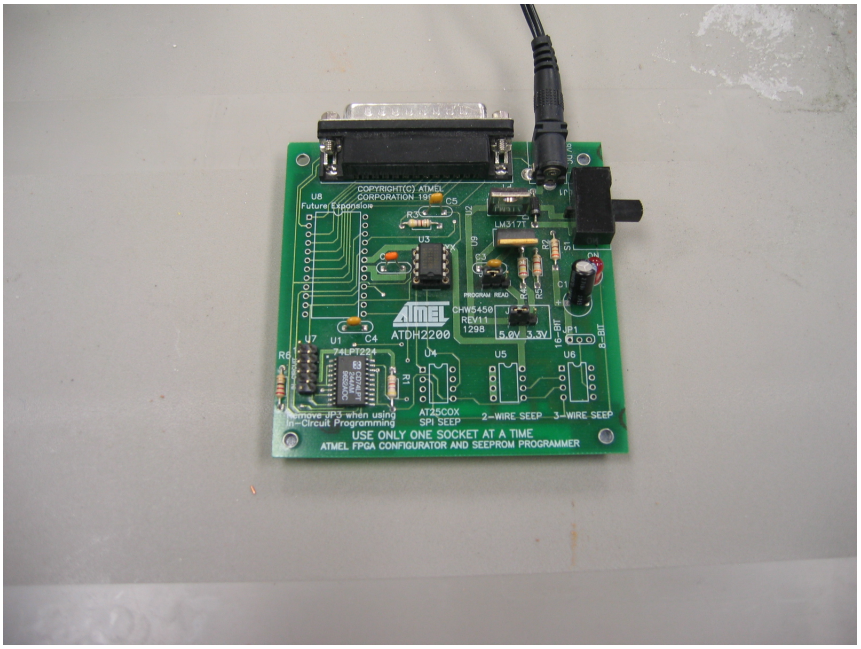

Figure 4.10: ATMEL Board which is attached to the parallel port on the PC

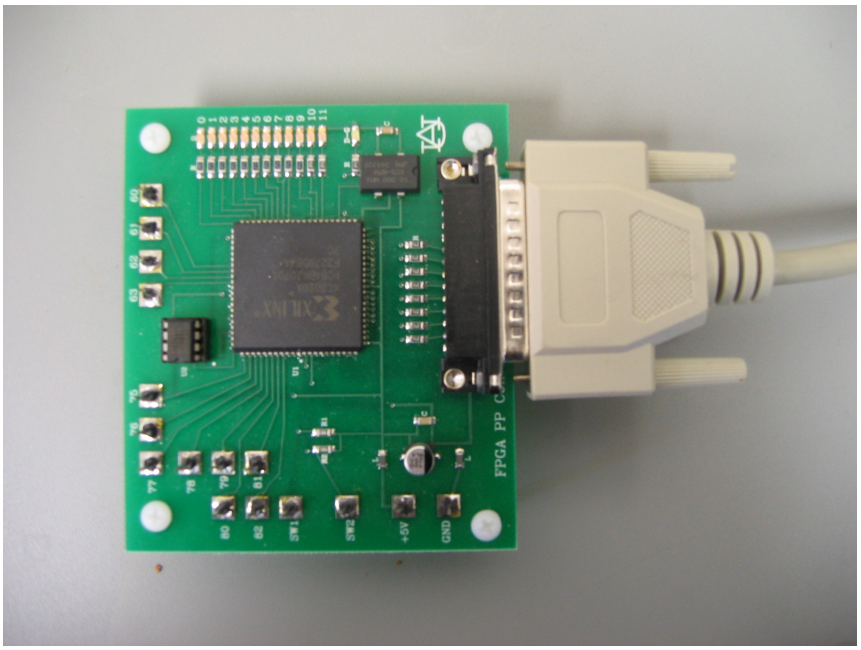

Figure 4.11: FPGA Board attached to the PC

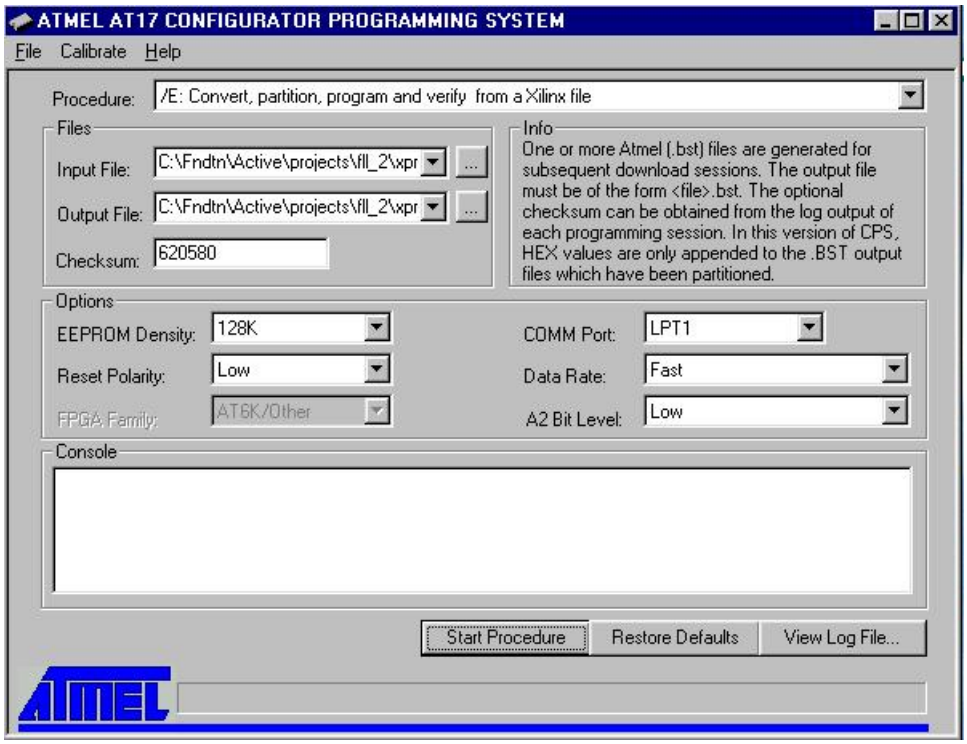

Figure 4.12: The output interface for programming the EPROM

4.2 Interfacing to the FLL and GUI

A GUI (Graphical User Interface) was designed in order to create an interface that would be able to display the output frequency, count or capacitance. This GUI was written in Visual Basic code. The parallel port was used to read in data from the FPGA board, which was then displayed as the output of the program. The biggest issue that was faced was the fact that the Parallel Port output has eight data bits, which were not enough for the twelve that were needed.

For the first 8 bits, pins 2-9 were used which are for D_o-D_7. These data bits were used as input to the code, using the function Inp(PortAddress), where the PortAdress given to the parallel port was &H378. The status port was used to read the last four bits that were needed for the program. The status port can be read in by adding 1 to the base address. Therefore, the status bit data could be read in by the function Inp(PortAddress+1).

Table 4.1 and 4.2 show the pin assignment for the parallel port and the status register respectively [30]. Four of the eight status pins were chosen to work as data bits. The four that were used were Bits 3-6, as they are not inverted at the output. Note that at the beginning of the GUI, the 5th bit of the control word is kept high in order to disable the bi-directional port option of the parallel port.

The logic used in the GUI is simple. At first, the bit value for the control word is checked. After the four bits, C_3-C_6 were obtained, they were shifted by 5 bits by multiplying times 32. This yielded a 12-bit word with the 1st eight bits as zero, and the last four bits as C_3-C_6. A logical OR function was executed with this word and the 8-bit data. The result was called the count.

Since a 10MHz clock was used, estimating the frequency was relatively easy.

$$f = \frac{10 \times 10^6}{Count \times 2} \tag{4.1}$$

Pin No.(D-Type 25)	Signal	Direction (In/out)	Register	Hardware Inverted
1	nStrobe	In/Out	Control	Yes
2	Data	Out	Data	No
3	Data	Out	Data	No
4	Data	Out	Data	No
5	Data	Out	Data	No
6	Data	Out	Data	No
7	Data	Out	Data	No
8	Data	Out	Data	No
9	Data	Out	Data	No
10	nAck	In	Status	No
11	Busy	In	Status	Yes
12	Paper-Out/Paper-End	In	Status	No
13	Select	In	Status	No
14	nAuto-Linefeed	In/Out	Control	Yes
15	nError/nFault	In	Status	No
16	nInitialize	In/Out	Control	No
17	nSelect-Printer/nSelect-In	In/Out	Control	Yes
18-25	Ground	Gnd	Gnd	No

Table 4.1: Pin Assignments of the D-Type 25 Pin Parallel Port Connector

Offset	Name	Read/Write	Bit No.	Properties
Base + 2	Control Port	Read/Write	Bit 7	Busy
			Bit 6	Ack
			Bit 5	Paper Out
			Bit 4	Select In
			Bit 3	Error
			Bit 2	IRQ (Not)
			Bit 1	Reserved
			Bit 0	Reserved

Table 4.2: Control Port

Capacitance could also be estimated from the GUI, however, that required a curve fit. This is explained in detail in the testing section of this chapter.

4.3 Software GUI

The following is a copy of the GUI which was written in Visual Basic.

```
{Dim PortAddress
Private Sub Command1_Click()
a = Text1.Text
PortAddress = &H378
'Print 2 * a
Out PortAddress + 2, 0
Out PortAddress, a
End Sub
```

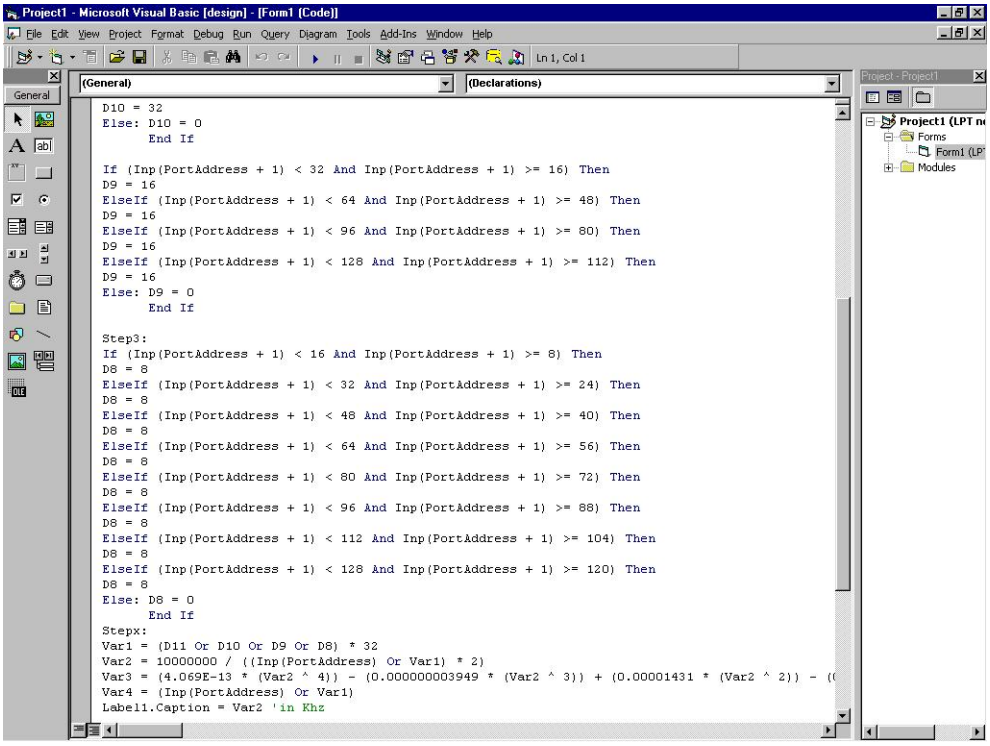

Figure 4.13: Screenshot of the GUI in Visual Basic

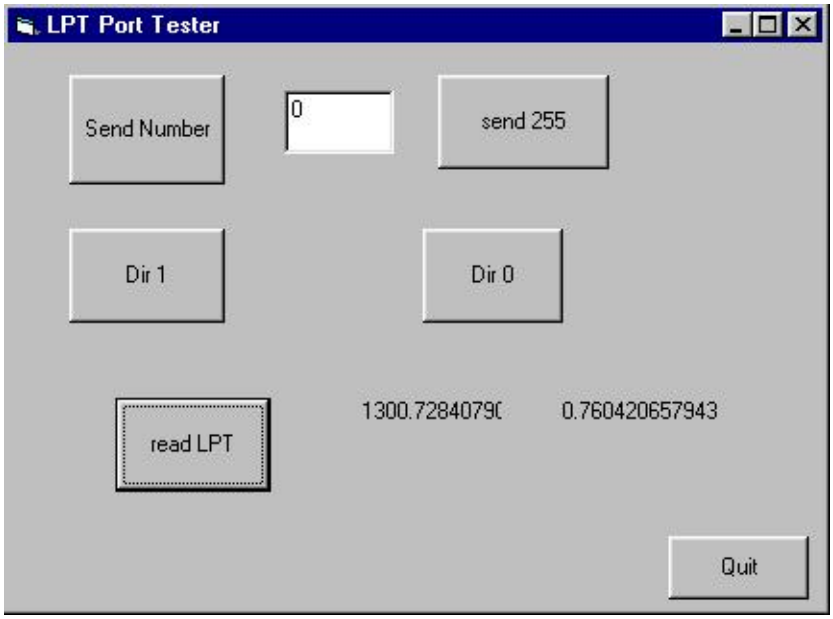

Figure 4.14: GUI Interface

```
Private Sub Command2_Click()
PortAddress = &H378
Out PortAddress, 255
End Sub

Private Sub Command3_Click()
Out PortAddress + 2, 36
Out PortAddress + 2, 32
PortAddress = &H378
If Inp(PortAddress + 1) >= 64 Then D11 = 64 Else D11 = 0

If (Inp(PortAddress + 1) < 64 And Inp(PortAddress + 1) >= 32) Then
D10 = 32
ElseIf (Inp(PortAddress + 1) < 128 And Inp(PortAddress + 1) >= 96) Then
```

```
D10 = 32
Else: D10 = 0
      End If

If (Inp(PortAddress + 1) < 32 And Inp(PortAddress + 1) >= 16) Then
D9 = 16
ElseIf (Inp(PortAddress + 1) < 64 And Inp(PortAddress + 1) >= 48) Then
D9 = 16
ElseIf (Inp(PortAddress + 1) < 96 And Inp(PortAddress + 1) >= 80) Then
D9 = 16
ElseIf (Inp(PortAddress + 1) < 128 And Inp(PortAddress + 1) >= 112) Then
D9 = 16
Else: D9 = 0
      End If

Step3:
If (Inp(PortAddress + 1) < 16 And Inp(PortAddress + 1) >= 8) Then
D8 = 8
ElseIf (Inp(PortAddress + 1) < 32 And Inp(PortAddress + 1) >= 24) Then
D8 = 8
ElseIf (Inp(PortAddress + 1) < 48 And Inp(PortAddress + 1) >= 40) Then
D8 = 8
ElseIf (Inp(PortAddress + 1) < 64 And Inp(PortAddress + 1) >= 56) Then
D8 = 8
ElseIf (Inp(PortAddress + 1) < 80 And Inp(PortAddress + 1) >= 72) Then
D8 = 8
ElseIf (Inp(PortAddress + 1) < 96 And Inp(PortAddress + 1) >= 88) Then
```

```
D8 = 8
ElseIf (Inp(PortAddress + 1) < 112 And Inp(PortAddress + 1) >= 104) Then
D8 = 8
ElseIf (Inp(PortAddress + 1) < 128 And Inp(PortAddress + 1) >= 120) Then
D8 = 8
Else: D8 = 0
      End If
Stepx:
Var1 = (D11 Or D10 Or D9 Or D8) * 32 '4-BIT CONTROL WORD
Var2 = 10000000 / ((Inp(PortAddress) Or Var1) * 2) 'COUNT
Label1.Caption = Var2 'in Khz 'FREQUENCY

End Sub

Private Sub Command4_Click()
End
End Sub

Private Sub Command5_Click()
Out PortAddress + 2, 1
End Sub

Private Sub Command6_Click()
Out PortAddress + 2, 0
End Sub
}
```

This version of the program calculated the estimated frequency as the output. To get an estimate of the capacitance, a curve fit had to be carried out with data from the LCR meter. This is explained in detail in the next section.

4.4 Testing with Oscillator Circuit I

The first circuit (Figure 3.2) was connected to the FPGA board, which was in turn connected to the parallel port on the PC. The PC was running the Visual Basic GUI. The capacitance was changed by approximately 1pF for each reading. A first set of readings were taken for a curve fit. The curve fit was generated using MATLAB. A fourth degree polynomial equation was obtained for each of the circuits to estimate frequency.

The polynomial equation for the first circuit was

$$C = [4.069 \times 10^{-}13 \cdot f^4] - [3.949 \times 10^9 - \cdot f^3] + [1.431 \times 10^{-}5 \cdot f^2] - [0.02306 \cdot f] + 14.07 \quad (4.2)$$

where

- f=Frequency
- C=Capacitance

To include estimation of capacitance in the GUI, the last part of the code was changed to the following.

```
Var1 = (D11 Or D10 Or D9 Or D8) * 32 '4-BIT CONTROL WORD
Var2 = 10000000 / ((Inp(PortAddress) Or Var1) * 2) 'COUNT
Var3 = (4.069E-13*(Var2^4))-(0.000000003949*(Var2^3))+(0.00001431*(Var2^2))
-(0.02306*(Var2))+14.07
Label1.Caption = Var2 'in KHz
Label2.Caption = Var3 'in pF
```

Measured Capacitance(pF)	Measured Frequency(KHz)	Actual Capacitance(pF)	Actual Frequency(KHz)	%Error (Capacitance)	%Error (Frequency)
28.511	1.778	28	1.779	1.83	0.06
28.117	1.792	27.597	1.792	1.88	0.00
27.416	1.819	26.853	1.818	2.10	0.06
26.213	1.867	25.633	1.873	2.26	0.32
24.973	1.92	24.402	1.923	2.34	0.16
23.768	1.976	23.159	1.976	2.63	0.00
23.034	2.012	22.413	2.016	2.77	0.20
21.764	2.078	21.242	2.075	2.46	0.14
21.083	2.115	20.572	2.119	2.48	0.19
19.516	2.21	19.725	2.212	1.06	0.09
18.138	2.304	18.214	2.304	0.42	0.00
17.317	2.364	17.44	2.358	0.71	0.25
15.964	2.474	16.101	2.475	0.85	0.04
15.161	2.545	15.258	2.538	0.64	0.28
14.372	2.621	14.441	2.618	0.48	0.11
13.459	2.717	13.468	2.717	0.07	0.00
12.451	2.832	12.425	2.841	0.21	0.32
11.771	2.917	11.701	2.924	0.60	0.24
10.629	3.071	10.508	3.067	1.15	0.13
9.432	3.25	9.264	3.247	1.81	0.09
8.291	3.441	8.17	3.448	1.48	0.20
7.805	3.528	7.639	3.521	2.17	0.20
6.835	3.717	6.711	3.704	1.85	0.35
5.634	3.987	5.521	4	2.05	0.32
4.572	4.284	4.526	4.274	1.02	0.23
3.83	4.553	3.713	4.545	3.15	0.18
2.185	5.246	2.132	5.263	2.49	0.32

Table 4.3: Experimental Analysis of First Oscillator Circuit

Following this, actual frequency was measured using the oscilloscope, model number Agilent DSO3202A, the estimated frequency and estimated capacitance through the GUI and the actual capacitance through the LCR meter. Again, readings were taken for every 1pF change in actual capacitance. Percentage error for capacitance and frequency were also calculated. Table 4.3 shows the readings that were obtained during testing of the first circuit.

Average error in capacitance was 1.59% and average error in frequency was 0.17%. The error in capacitance can be explained by the fact that the curve fit equation yields only a reasonable estimate of the capacitance. The frequency error can be explained by the resolution. Using a higher number of bits in the FLL will reduce the error percentage further. The graph is presented in Figure 4.15.

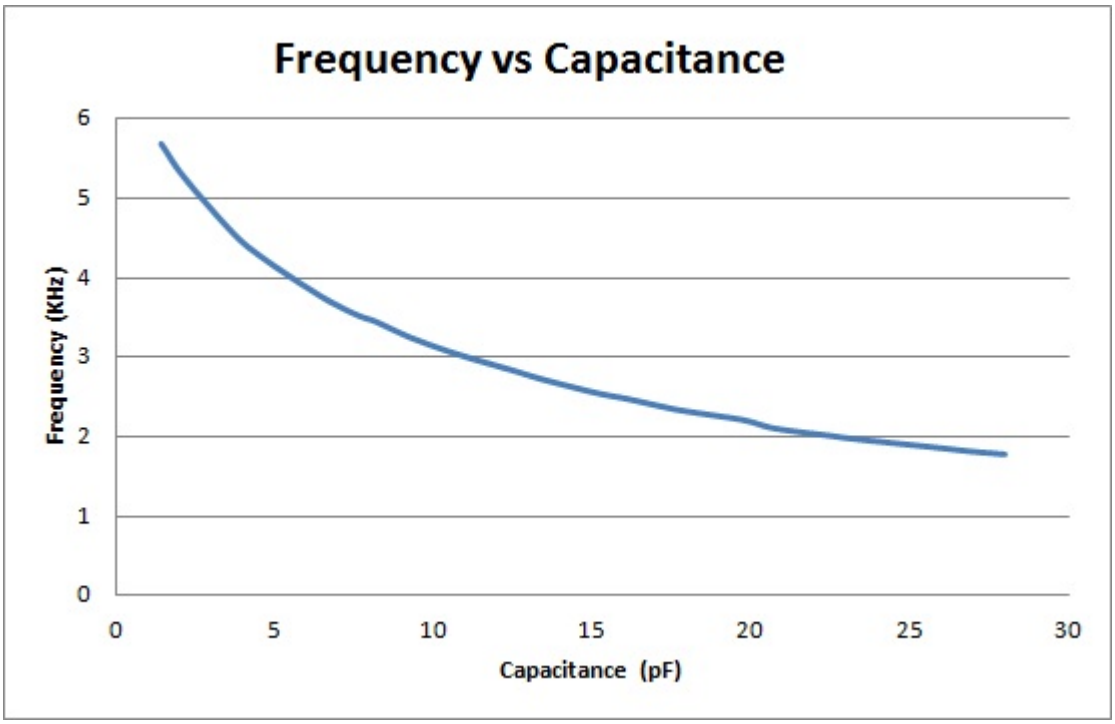

Figure 4.15: Experiment I : Frequency vs Capacitance

4.5 Testing with Oscillator Circuit II

Similar testing was performed with the second circuit (Fig. 3.7) as well, however, the equation for capacitance was different. A polynomial curve fit generated with MATLAB gave a fourth-order equation. The following equation was placed in the GUI.

$$C = [4.069 \times 10^{-}13 \cdot f^4] - [3.949 \times 10^9 - \cdot f^3] + [1.431 \times 10^{-}5 \cdot f^2] - [0.02306 \cdot f] + 14.07 \quad (4.3)$$

The GUI code was also changed to the following -

```
Var1 = (D11 Or D10 Or D9 Or D8) * 32 '4-BIT CONTROL WORD
Var2 = 10000000 / ((Inp(PortAddress) Or Var1) * 2) 'COUNT
Var3 = (4.069E-13*(Var2^4))-(0.000000003949*(Var2^3))+(0.00001431*(Var2^2))
-(0.02306*(Var2))+14.07
Label1.Caption = Var2 'in Khz
Label2.Caption = Var3 'in pF
```

The experimental results after analysis of the second circuit are given in Table 4.4 and the graph in Figure 4.16 shows the Frequency vs Capacitance. The percent error in capacitance was found to be 8.77% and the percent error in frequency was found to be 0.18%.

Measured Capacitance(pF)	Measured Frequency(KHz)	Actual Capacitance(pF)	Actual Frequency(KHz)	%Error (Capacitance)	%Error (Frequency)
25.143	1.416	26.5	1.425	5.12	0.63
24.278	1.451	25.437	1.453	4.56	0.14
23.325	1.491	24.285	1.493	3.95	0.13
22.742	1.516	23.6	1.52	3.64	0.26
22.099	1.545	22.857	1.548	3.32	0.19
20.664	1.609	21.26	1.618	2.80	0.56
19.981	1.642	20.543	1.645	2.74	0.18
18.936	1.694	19.41	1.695	2.44	0.06
18.218	1.732	18.673	1.73	2.44	0.12
16.933	1.803	17.34	1.805	2.35	0.11
16.027	1.857	16.47	1.852	2.69	0.27
15.381	1.897	15.807	1.901	2.70	0.21
14.048	1.986	14.46	1.992	2.85	0.30
12.916	2.069	13.484	2.066	4.21	0.15
12.031	2.14	12.63	2.137	4.74	0.14
10.763	2.253	11.415	2.252	5.71	0.04
9.867	2.343	10.591	2.347	6.84	0.17
9.058	2.433	9.792	2.433	7.50	0.00
7.842	2.589	8.596	2.584	8.77	0.19
6.824	2.745	7.667	2.747	11.00	0.07
5.889	2.917	6.704	2.915	12.16	0.07
4.934	3.125	5.722	3.125	13.77	0.00
3.916	3.387	4.667	3.378	16.09	0.27
2.951	3.671	3.774	3.663	21.81	0.22
1.47	4.212	2.447	4.219	39.93	0.17
1.145	4.591	1.736	4.587	34.04	0.09

Table 4.4: Experimental Analysis of First Oscillator Circuit

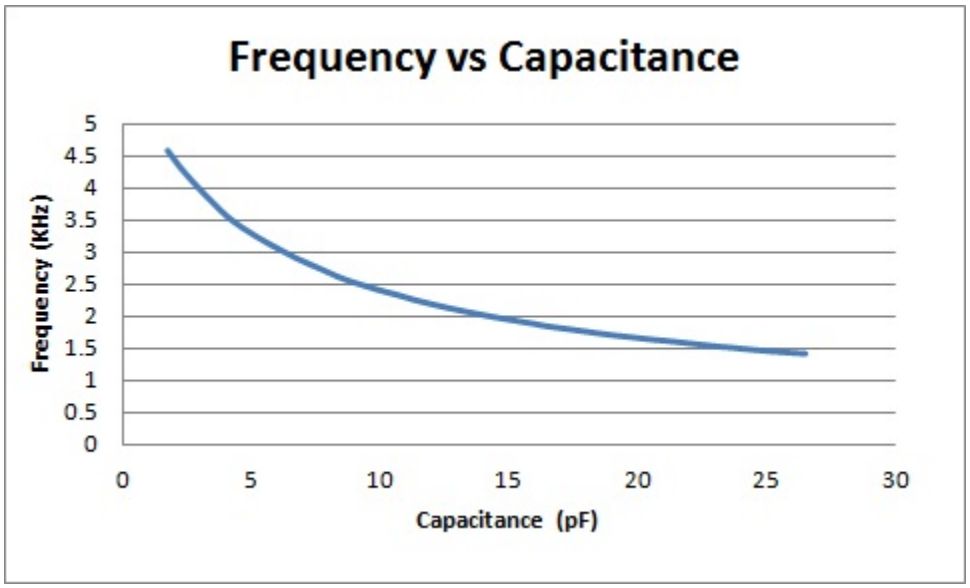

Figure 4.16: Experiment II : Frequency vs Capacitance

Chapter 5

Frequency Locked Loop Application: Mass of Water Drop Measurement

As a demonstration of the FLL, a application was developed for measuring the mass of small quantities of liquid water. A sensor was implemented in such a way that its capacitance could be measured as a function of mass of a liquid. More specifically it relates to the realization of fringing field sensors in printed circuit board (PCB) technology, where the interdigitated electrode structures are realized in the Cu foil on one or both surfaces of the PCB. Additionally, the Cu features are coated with a material, such as solder mask, to prevent the Cu features from being shorted together when the device is in contact with water.

5.1 Sensor Circuit

Consider a structure where n electrodes of area, a, are stacked in parallel, a fixed separation distance, d, apart, in a dielectric material of relative permittivity, ϵ_r, as illustrated in Figure 5.1. Every other stacked electrode is electrically connected together. This electrode configuration is referred to as two interdigitated electrodes, and is illustrated in the top-view drawing in Figure 5.1.

Assuming that the magnitude of the overlapping electrode area is much greater than the electrode separation distance, most of the capacitance between the electrodes is contained within the electric field directly between the electrode overlapping areas, and not due to fringing effects. However, since the perimeter around the electrodes is much greater than the perimeter around two parallel plate electrodes of the same total overlapping area with the same electrode separation distance, the fringing effects will be considerably greater in the

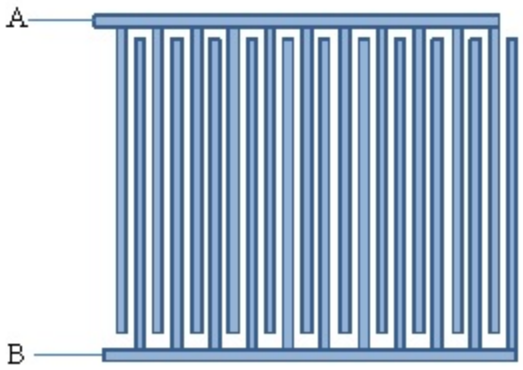

Figure 5.1: Two Interdigitated Electrodes

interdigitated electrode case. For n interdigitated electrodes, the equation for the capacitance is

$$C = \frac{(n-1)\epsilon_o \epsilon_r a \gamma}{d} \tag{5.1}$$

Equation 5.1 does not account for multiple materials with different relative permittivity values or for capacitance between the electrodes and the arms to which the opposite electrodes are physically attached. If the height of the electrodes is on the same order as the separation distance, much of the capacitance will be due to the fringing fields outside of the space directly between the interdigitated electrodes.

5.1.1 Capacitors as Sensors

Capacitor structures can be utilized as sensors for numerous applications. Any measurand that affects the electrode separation distance, the electrode overlapping area or the relative permittivity of the dielectric between the electrodes can be sensed with a capacitor structure. Additionally, if a measurand interacts with the fringing fields, thereby changing the measurable capacitance, a useful sensor can also be realized. Fringing field capacitive detection has the advantage of allowing the electrodes to be physically isolated from the

sensing environment, as the fringing electric field is projected into the object or material being detected without altering the electrode configuration. Interdigitated electrode structures are particularly suitable for this sensing technique, as they can be designed to maximize the capacitance due to fringing. Capacitive fringing field sensors have been developed for measuring soil moisture content [31], grain moisture content [32], for rain detection [33] as proximity sensors [34], as capacitive touch switches [35], as biomedical sensors [36] and as the sensing element in a MEMS accelerometer [37]. Many of these sensors operate by measuring the change in capacitance due to the fringing fields in air ($\epsilon_r = 1.0006$) and in water (ϵ_r =80)[38]. Since the ratio of relative permittivities of water and air is approximately 80:1, there is typically a very large change in capacitance due to the presence of water or an object containing water.

5.1.2 Implementation

The technology for implementing PCBs is also an excellent technology for implementing interdigitated electrode fringing field sensors. FR-4 and other PCB substrate materials provide a stable platform for interdigitated electrode structures, which can be realized from Cu traces on one or both sides of a double-sided PCB. The electrodes can be coated with solder mask to isolate them from the sensing environment, typically water based, to prevent electrical shorting. Additionally, the Cu thickness can be tailored to the solder mask thickness in order to minimize measurand-induced non-fringing capacitive effects directly between the electrodes. A cross-sectional illustration of this concept is presented in Figure 5.2, where interdigitated electrodes, "A" and "B", are only realized on one side of the PCB. The electric field, including fringing, is illustrated in Figure 5.3. Observe that the fringing field extends out beyond the solder mask layer where it can interact with objects or fluid in close proximity to the PCB. The other side of the PCB can also be used for additional interdigitated electrodes, a Cu ground plane or for attached sensor interface electronics.

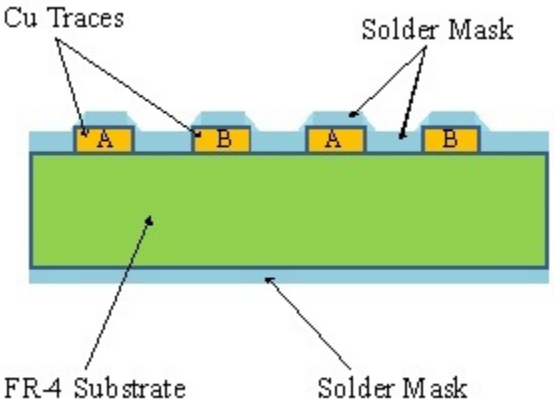

Figure 5.2: A cross-sectional drawing of interdigitated electrodes realized in the Cu foil on one side of a PCB

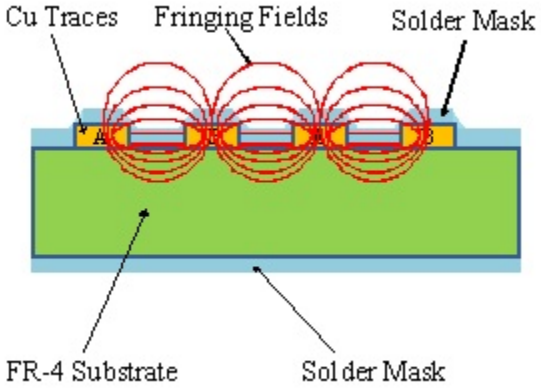

Figure 5.3: A cross-sectional drawing of interdigitated electrodes realized in the Cu foil on one side of a PCB where the red lines represent the electric field lines between the electrodes

Prototype PCB fringing field sensors were designed, fabricated and tested using a commercially available PCB fabrication process. This process resulted in a double-layer PCB on an FR-4 substrate with 1oz Cu traces and PSR-4000BN solder mask. The prototype devices were manufactured by Advanced Circuits, a commercial PCB fabricator. The process resulted in a double-sided PCB that was nominally 62mils thick, with 1.4mil tall Cu traces and a solder mask thickness of 0.7 to 1.3 mils. The prototype device was 1000mils by 1000mils in size with an interdigitated electrode structure patterned in the Cu foil on one side. A solid Cu plane was realized on the bottom side of the device directly under the interdigitated electrode structure on the top side. The electrodes were 6mils wide with a 6mil gap between adjacent electrodes. This device had 70 electrodes that overlapped 882mils. A 40mil diameter plated through-hole was fabricated in the center of each of the two electrical contact pads. A drawing of the interdigitated electrode structure for the prototype device is presented in Figure 5.4. The outline of the device is shown in light green. The outline of the solder mask openings around the two contact pads is shown in dark green.

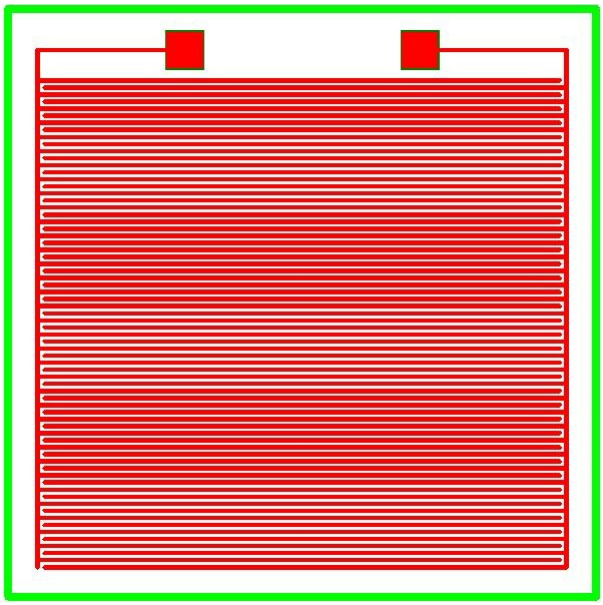

Figure 5.4: The interdigitated electrode structure for the prototype device

Wires were soldered into the two plated through-holes in the electrical contact pads. Then the exposed pads/wires were coated with silicone to insulate them from contact with water, which would electrically short the two wires together. A photograph of a prototype device is presented in Figure 5.5 next to a dime for a size comparison. The capacitance of the device was measured using a LCR821 meter. In air, the device had a capacitance of 63.9pF. When fully submerged, the device had a capacitance of 321.3pF. Additionally, the prototype device was evaluated by adding drops of water to the surface of the device so that the capacitance could be measured as a function of mass. Since the water did not wet the surface very well, the water beaded up so that the surface area of the water in contact with the device increased as the mass increased. A plot of the measured evaluation data is presented in Figure 5.6, which demonstrates a linear response of the sensor to variable quantities of water, which demonstrates the functionality of the sensor.

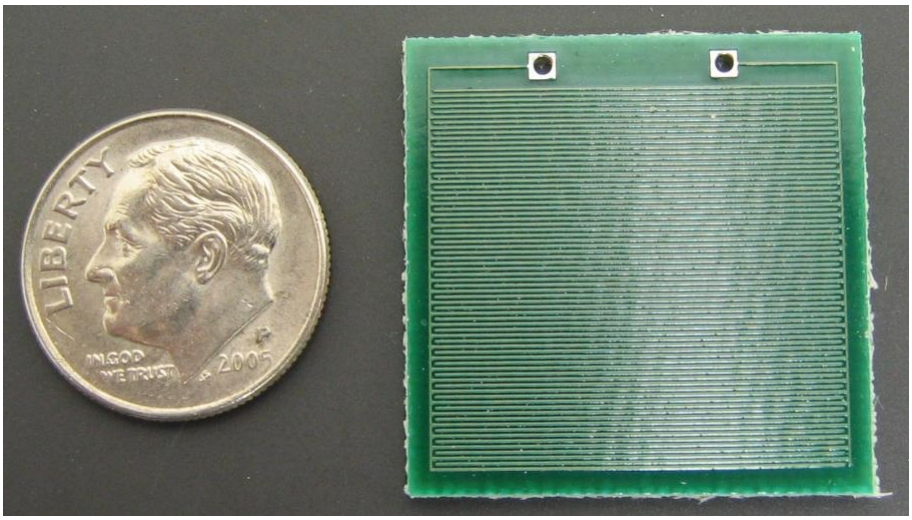

Figure 5.5: The prototype device next to a dime

5.1.3 Interfacing the Oscillator Circuit with the Fringing Field Sensor

One of the oscillator circuits was implemented on the same PCB board as the fringing field interdigitated sensor.

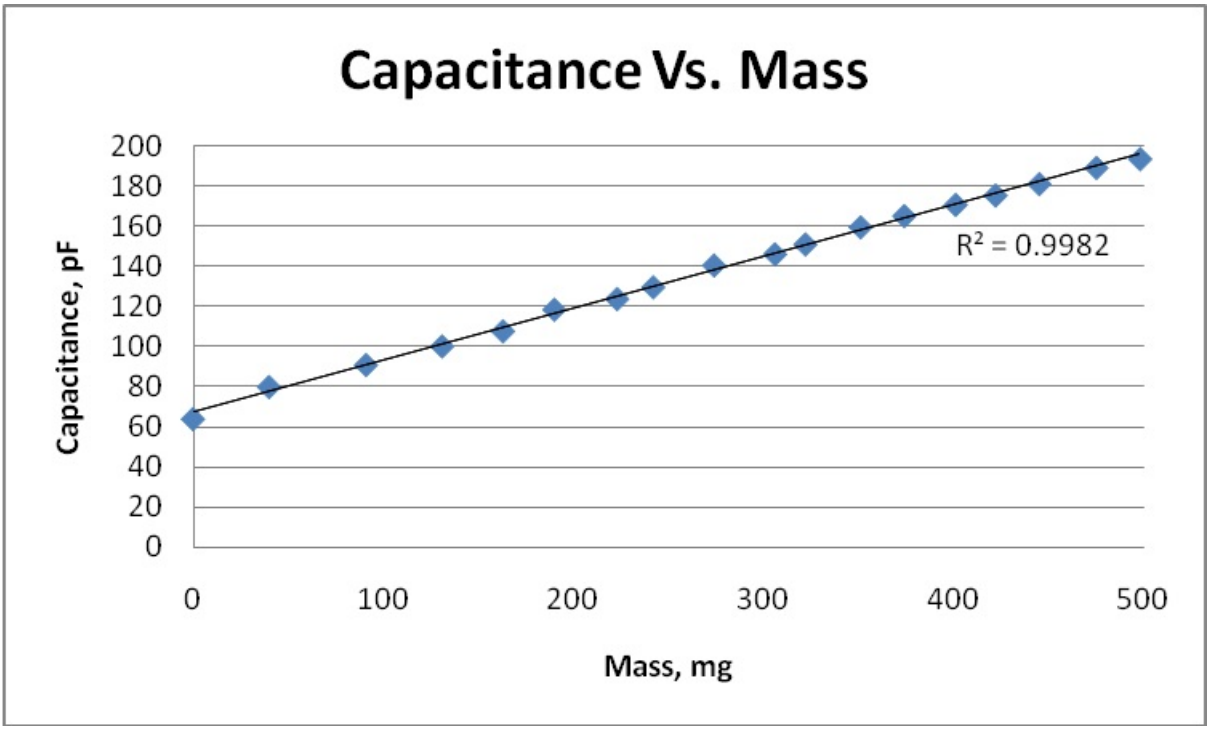

Figure 5.6: Data from testing the prototype device

A dam was laid down around the sensor, so that the water does not flow over to the circuit. The material used for the dam was Hysol FP 4451. A photograph of the PCB is shown in Figure 5.8. The second circuit (Figure 3.7) was used for integrating the circuit and the sensor on one board. The dimensions of the sensor that was used were 1000 $\times$ 1000 mils. Figure 5.7 shows the ViewMaster layout of the integrated sensor and circuit. A DPDT switch was used in order to measure the value of the fringing field capacitance using an LCR meter. This circuit was soldered with a different set of components as compared to the earlier one, because the variable capacitance range had changed from 2-20pF to approximately 70-190pF. Referring to Figure 3.8, the value of resistances that would be most ideal for this range are 1.5KΩ. In the actual circuit, however 1.7KΩ resistors were used. This gave an approximate frequency range of 1.6MHz to 2.8Mhz.

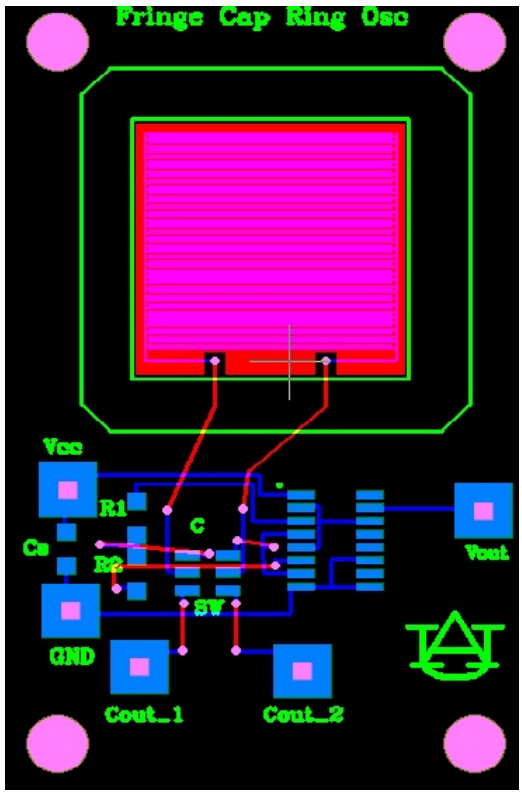

Figure 5.7: ViewMaster layout of the Integrated Sensor

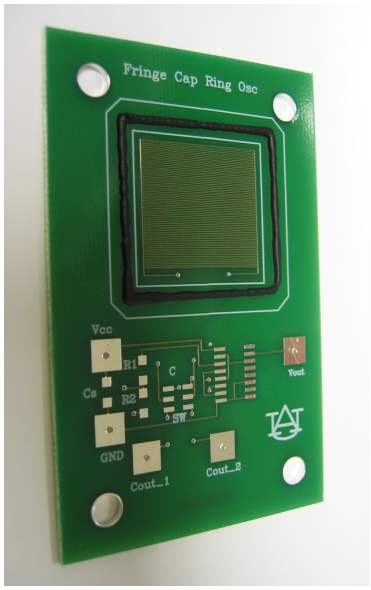

Figure 5.8: PCB with dam

5.2 Testing

Testing for this circuit required the use of a scale as the mass of each water droplet was to be measured. The circuit was then connected to the FPGA board which was programmed with a 12-bit FLL. This was then connected to the PC using the parallel port and similar to the testing done earlier, Visual Basic was used to read out the binary data from the parallel port.

The challenging aspect was to be able to read out the mass of each water droplet correctly, as the mass of each droplet is close to 20-30mg. This made it a little difficult as the digital scale that was used is accurate only to 0.001g≈1mg. The mass had to be stabilized to a single value before it could be connected to the LCR meter (to measure capacitance) and to the FPGA board (to measure the count).

Another condition to consider was the fact that as the water droplet spreads over the sensor, the capacitance changed. It started increasing slowly but steadily. To avoid this, the water droplet was kept at rest for a minimum of 10 seconds before a capacitive readout was taken. Centering of the water over the sensor was attempted, as its position can have a effect on capacitance.

The setup for testing this circuit is shown in Figure 5.9 and Figure 5.10. Figure 5.9 shows the circuit without any water on it, the weight of the circuit has also been zeroed out. Figure 5.10 shows the circuit with a drop of water. As can be seen, the drop of water has increased the weight to 44mg.

5.3 Results

The experimental setup for testing is shown in the following Figures. Figure 5.11 shows the circuit connected to the PC, the voltage supply and the LCR Meter. This part of the setup was used for capacitance measurement and reading out the count of the FLL. Figure

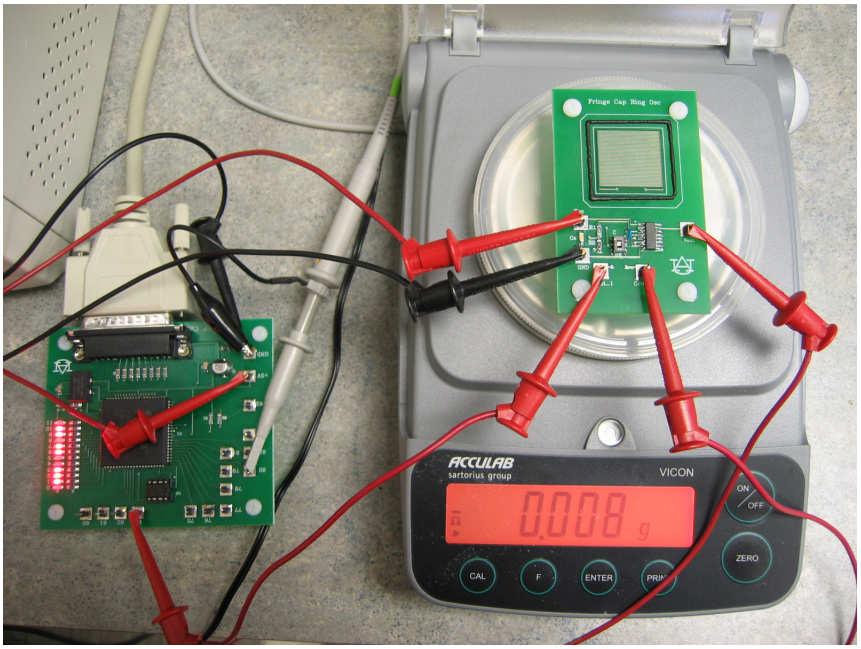

Figure 5.9: Without water and weight zeroed out

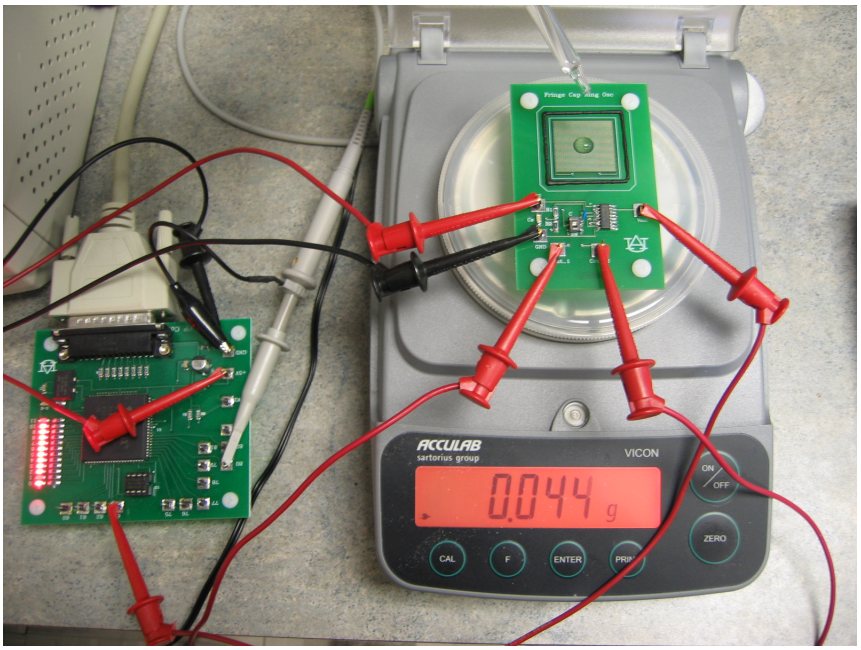

Figure 5.10: With water droplet

5.12 shows the circuit connected to the PC and oscilloscope, this setup was used for reading out the frequency at the output of the FPGA Board.

Figure 5.11: Circuit connected to LCR Meter and PC

The experiment was conducted a total of five times in order to obtain accurate readings and to obtain sufficient data for a circuit analysis (Refer Tables 5.1-5.5 and Figures 5.14-5.18). This data also would come in useful for a generating a curve fit equation which would make it easier to calibrate the Visual Basic code. This code would then be able to give an output that is a reasonable estimation of the capacitance or mass change due to the water droplet. Each set of readings was used to plot a graph that showed the change in capacitance compared to the change in the binary output of the FLL (Count). Some of the nonlinearity in the plots may be due to jiggling the circuit board while adjusting the DPDT switch to measure the capacitance with the LCR meter. A typical plot of Counts vs Mass of water is presented in Figure 5.13, showing a more linear response than generally observed in the Counts vs Capacitance plots. The Counts data was taken before the DPDT switch was switch was adjusted to measure the capacitance with the LCR meter. It is worth noting that the frequency of the relaxation oscillator is proportional to 1/C. and the FLL counts

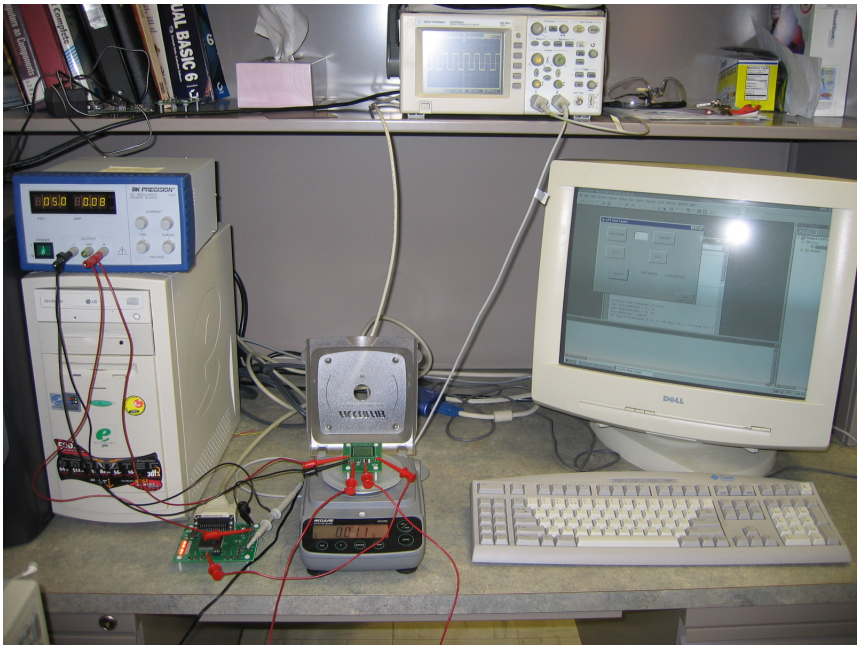

Figure 5.12: Circuit connected to Oscilloscope and PC

is proportional to 1/f, where f is the frequency of the square wave. The linear response plot in Figure 5.13 demonstrates that the FLL can be used to linearize the response of the 1/C characteristic of relaxation oscillators used as interfaces to capacitive sensors.

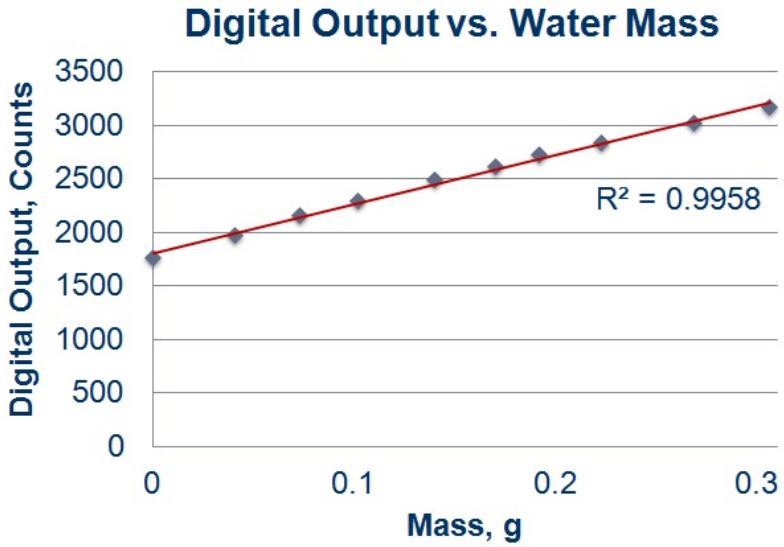

Figure 5.13: Plot of Digital Output Vs. Mass of Added Water

Actual Capacitance (pF)	Actual Frequency (kHz)	Mass (g)	Count
72.612	2.857	0	1746
80.419	2.717	0.014	1846
92.554	2.538	0.04	1975
100.44	2.381	0.065	2106
110.58	2.273	0.098	2207
120.08	2.128	0.122	2351
131.12	2.041	0.149	2446
140.26	1.923	0.165	2607
151.77	1.852	0.185	2703
155.95	1.799	0.205	2783
163.21	1.754	0.23	2851
175.8	1.65	0.258	3032
185.67	1.608	0.291	3113

Table 5.1: Change in Capacitance and Frequency as a function of Mass - Reading I

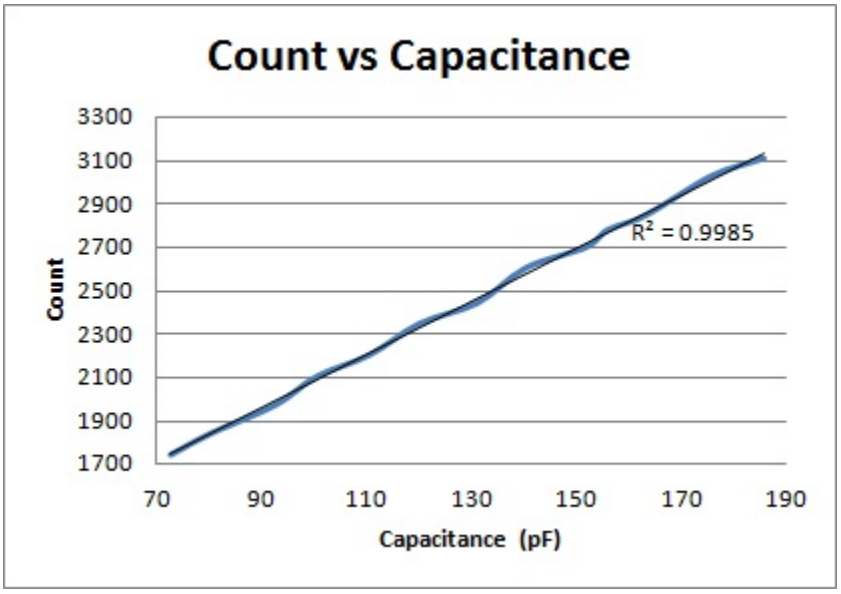

Figure 5.14: Count vs Capacitance

Actual Capacitance (pF)	Actual Frequency (kHz)	Mass (g)	Count
73.077	2.857	0	1752
88.551	2.564	0.029	1948
92.554	2.538	0.04	1975
102.93	2.326	0.057	2145
117.23	2.165	0.088	2313
126.89	2.049	0.116	2436
138.29	1.953	0.146	2559
149.19	1.852	0.184	2703
166.54	1.742	0.218	2870
171.75	1.661	0.244	3008
183.98	1.623	0.274	3082

Table 5.2: Change in Capacitance and Frequency as a function of Mass - Reading II

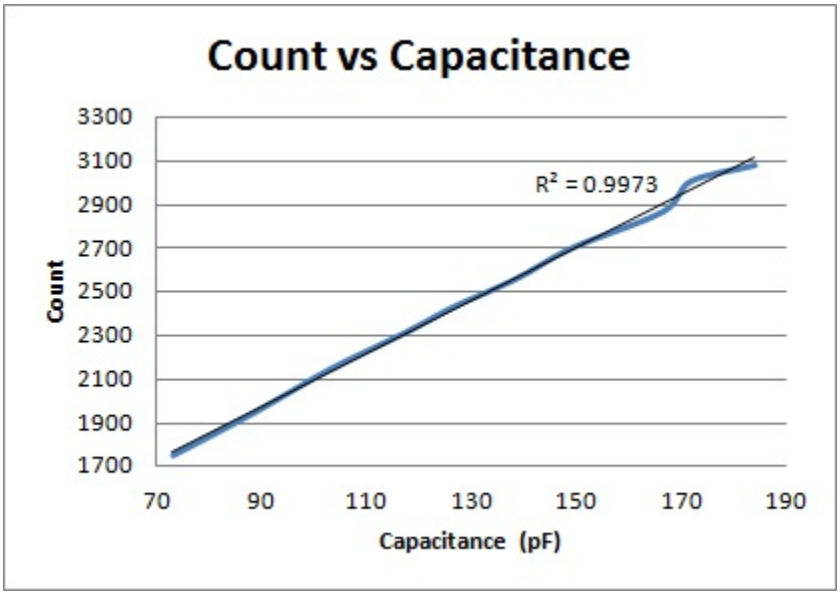

Figure 5.15: Count vs Capacitance

Actual Capacitance (pF)	Actual Frequency (kHz)	Mass (g)	Count
74.021	2.857	0	1755
90.115	2.577	0.031	1945
101.06	2.392	0.06	2087
112.41	2.222	0.088	2255
124.16	2.146	0.111	2323
134.56	1.976	0.146	2533
147.48	1.88	0.179	2659
148.28	1.866	0.207	2681
158.86	1.805	0.247	2769
171.8	1.672	0.277	2988
191.25	1.563	0.31	3200

Table 5.3: Change in Capacitance and Frequency as a function of Mass - Reading III

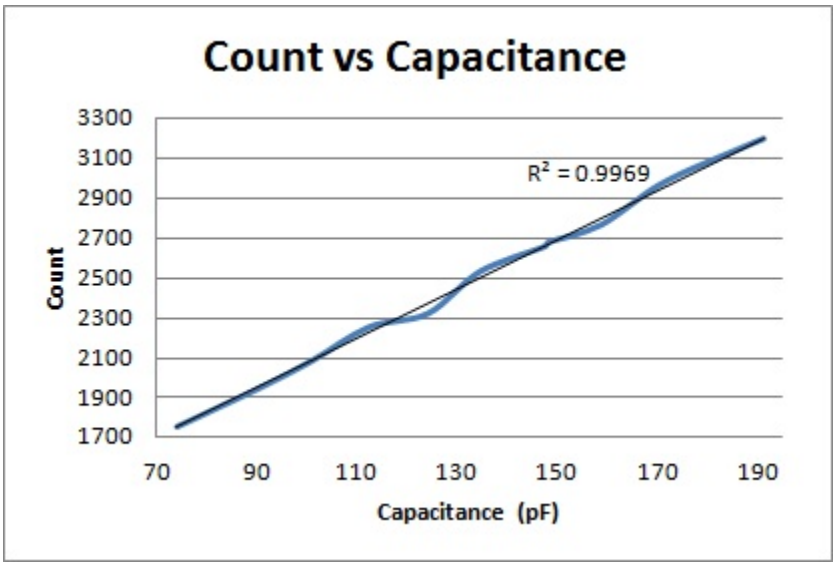

Figure 5.16: Count vs Capacitance

Actual Capacitance (pF)	Actual Frequency (kHz)	Mass (g)	Count
74.48	2.841	0	1756
92.067	2.538	0.041	1968
103.15	2.326	0.073	2148
117.86	2.183	0.102	2285
132.82	2.008	0.14	2485
142.2	1.923	0.17	2601
146.36	1.838	0.192	2716
161.69	1.767	0.223	2830
177.32	1.656	0.269	3020
190.85	1.577	0.306	3166

Table 5.4: Change in Capacitance and Frequency as a function of Mass - Reading IV

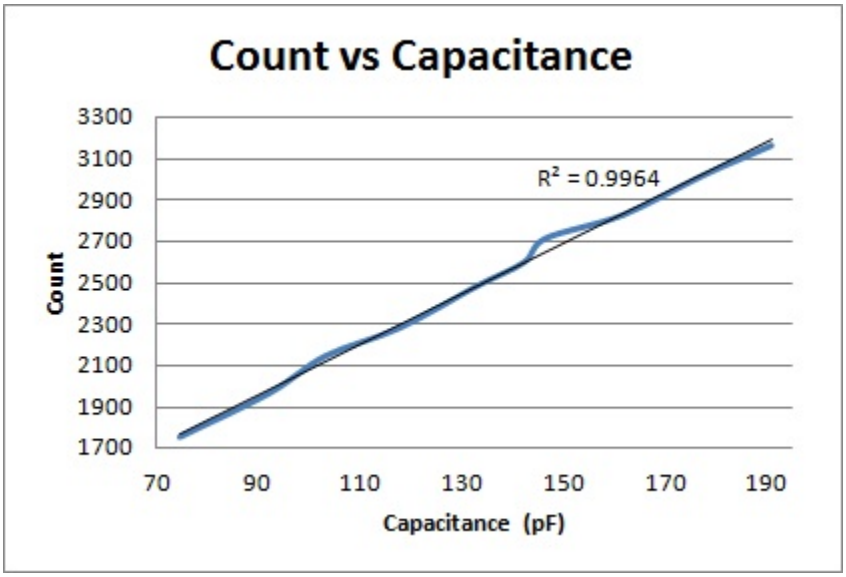

Figure 5.17: Count vs Capacitance

Actual Capacitance (pF)	Actual Frequency (kHz)	Mass (g)	Count
77.061	2.841	0	1758
87.248	2.632	0.019	1898
112.26	2.262	0.067	2209
114.34	2.222	0.094	2243
120.32	2.155	0.118	2318
130.59	2.058	0.148	2432
143.71	1.901	0.185	2620
150.93	1.838	0.219	2719
159.74	1.773	0.249	2818
169.48	1.701	0.29	2943
182.08	1.587	0.314	3149

Table 5.5: Change in Capacitance and Frequency as a function of Mass - Reading V

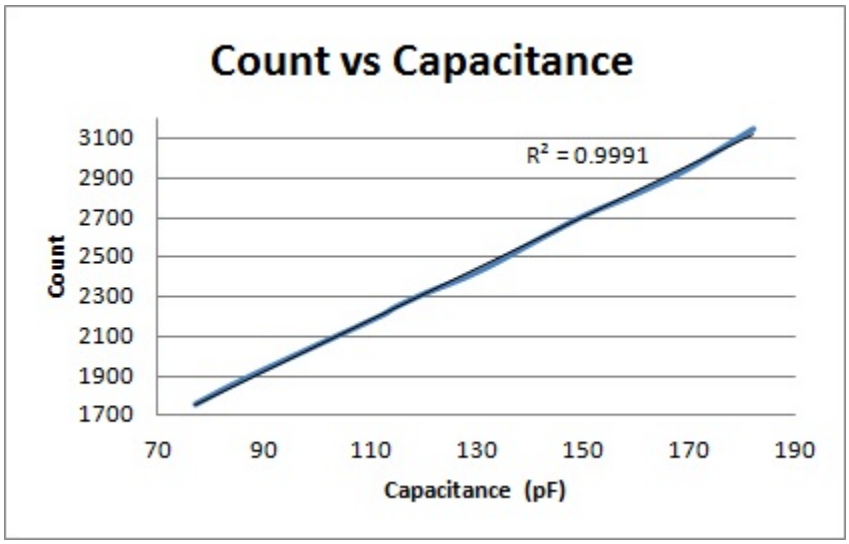

Figure 5.18: Count vs Capacitance

Chapter 6

Related Work [39]

6.1 Theory

Consider the schematic diagram of the single pole RC circuit depicted in Fig. 6.1.

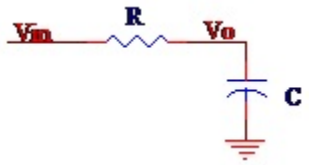

Figure 6.1: Single Pole RC Low Pass Filter Circuit

This circuit is the standard single pole passive low pass filter circuit, with a transfer function of

$$\frac{V_o(s)}{V_{in}(s)} = \frac{1/RC}{s + 1/RC} \tag{6.1}$$

Where

- Vo(s) = Laplace transform of the output voltage
- Vin(s) = Laplace transform of the input voltage
- R = resistance
- C = capacitance
- s = Laplace transform complex frequency variable

If a unit step function is applied to the input of the circuit and if the capacitor is initially discharged, the resulting time response of the output is

$$V_o = 1 - e^{\frac{-t}{\tau}} \tag{6.2}$$

Where

- Vo(t) = output voltage
- t = time
- τ = time constant

The time constant, τ, is

$$\tau = RC \tag{6.3}$$

Where

- R = resistance
- C = capacitance

Equation 3.2 can be rearranged to solve for the time, $t_{0.5}$, when $V_o(t)$ reaches one half the voltage of $V_{in}(t)$, yielding

$$t_{0.5} = 0.693\tau = 0.693RC \tag{6.4}$$

Where

- $t_{0.5}$ = the time for $V_o(t)$ to reach one half of $V_{in}(t)$
- τ = time constant
- R = resistance
- C = capacitance

Observe that, for a fixed value for R, $t_{0.5}$ is linearly proportional to C. Next consider the circuit depicted in Fig. 6.2, where a Complementary Metal-Oxide-Semiconductor (CMOS) inverter has been attached to the output of the RC circuit from Fig. 6.1, and C has been replaced with C_s, a capacitive sensor.

For this inverter, the trip voltage is approximately equal to one half of the inverter's power

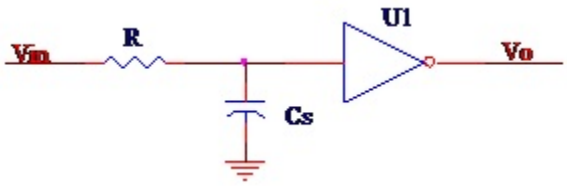

Figure 6.2: RC Circuit with an attached CMOS Inverter

supply voltage, V_{dd}. Since, ignoring additional protection circuitry, the input to a CMOS inverter is tied to the gates of an n-channel MOSFET and a p-channel MOSFET, the input resistance is very large, much larger than R. C is now the sum of two parallel capacitances, C_s and C_g

$$C = C_s + C_g \tag{6.5}$$

Where

- C = total capacitance

- Cs = sensor capacitance being measured
- Cg = capacitance associated with the gate structures of the MOSFETS in the inverter

If V_{in} is a step function with a final value of V_{dd}, then Equation 6.4 is the delay that U_1 experiences in switching states, compared to the same inverter circuit without the RC subcircuit being present. The output voltage of the inverter, V_o, will not be perfectly square, as compared to the plane inverter circuit. However, it can be squared up by adding one or more additional inverter stages.

Now consider the circuit in Fig. 6.3. This circuit has two inverter stages, one with the RC subcircuit and one without it, and two output voltages, V_{o1} and V_{o2}. Although the

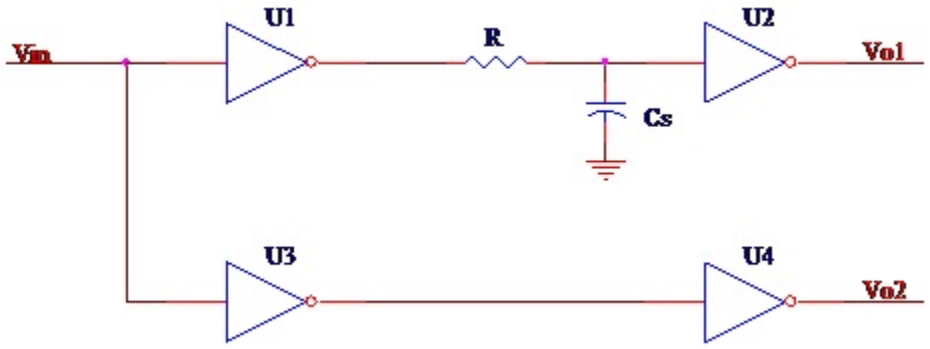

Figure 6.3: Multi-Inverter Circuit

use of a step function to obtain a one-time capacitance measurement is possible, it is not practical for most sensor applications. Therefore consider the case where Vin is a pulse train of frequency, *f*, and period, **T**, with a 50% duty cycle, and high/low voltage values of V_{dd}/0V, respectively. If **T** is much bigger than τ, such that C nearly fully charges or discharges between V_{in} cycles, then Equation 6.4 is still a reasonable approximation for the relative delay between V_{o1} and V_{o2}, and the relative phase difference between V_{o1} and V_{o2} is linearly proportional to C. However, the phase difference between the two output signals would be extremely small.

Therefore, consider the effect of decreasing **T**, resulting in significant charge remaining in C when V_{in} changes states. For the condition where V_{in} switches from 0V to V_{dd}, where V_c is the initial condition of C, the equation for $t_{0.5}$ becomes

$$t_{0.5} = -\tau \left(\frac{0.5V_{dd}}{V_{dd} - V_c} \right) = -RC \ln \left(\frac{0.5V_{dd}}{V_{dd} - V_c} \right) \tag{6.6}$$

Where

- $t_{0.5}$, = the time for V_o(t) to reach one half of V_{in}(t)
- τ = time constant
- R = resistance
- C = capacitance
- V_{dd} = power supply voltage
- V_c = initial condition of C

For a constant capacitance, C, the voltage, V_c, is a function of both the V_{in} pulse width/τ, and the number of cycles. In other words, for a new value for C, it takes a few cycles for V_c to converge to a steady state value at the moment that V_{in} switches states, so that Equation 6.6 is valid for determining the steady state phase delay between V_{o1} and V_{o2} [39]. This is illustrated in Fig. 6.4, where the V_c remainder, i.e. the absolute value of the difference between V_c and voltage across C as t $\rightarrow \infty$, is plotted as a function of the number of cycles or state changes of V_{in}, for various τ values between 0.2s and 1s, where the cycle time is 1s. This plot clearly shows that as the RC time constant, i.e. τ increases, the number of state cycles required for V_c to reach a steady state value also increases.

Therefore a numerical comparison was performed to evaluate the relationship between τ (and therefore C) and the state cycle time, T/2, in calculating $t_{0.5}$. For this comparison,

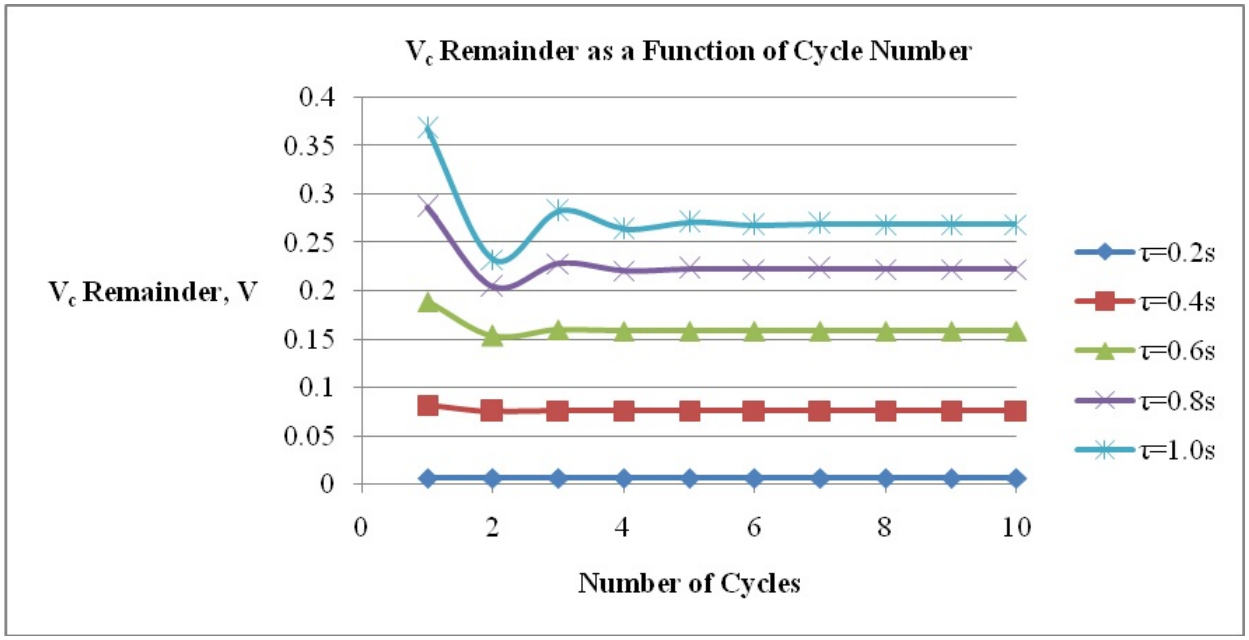

Figure 6.4: A Plot Of The V_c Remainder As A Function Of The Number Of State Cycles

ten state cycles were performed to obtain a steady state value for V_c, which was used with Equation 6.6 to determine the relative phase delay, $t_{0.5}$. This value for $t_{0.5}$, $t_{0.5}$-Real, was compared with $t_{0.5}$-Ideal, which was calculated using Equation 6.4. The resulting data is presented graphically in Fig. 6.4, where T was equal to 2s. Observe that for small ratios of τ:T, there is very little difference between $t_{0.5}$-Real and $t_{0.5}$-Ideal. A graph of the percent difference between $t_{0.5}$-Ideal and $t_{0.5}$-Real is presented in Fig. 6.6, using the data presented in Fig. 6.5.

From the data presented in Fig. 6.6, the percent error between $t_{0.5}$-Ideal and $t_{0.5}$-Real is 2.6% at τ equal to 0.25s. Since the relative phase difference between V_{o1} and V_{o2} is used to measure C and therefore Cs, the phase delay can be measured in degrees, with a phase delay of T referred to as a 360° phase delay. Therefore, from Fig. 6.6, if the permissible nonlinearity is limited to 2.6%, then the usable phase delay range for capacitance sensing would be 0° to 45°.

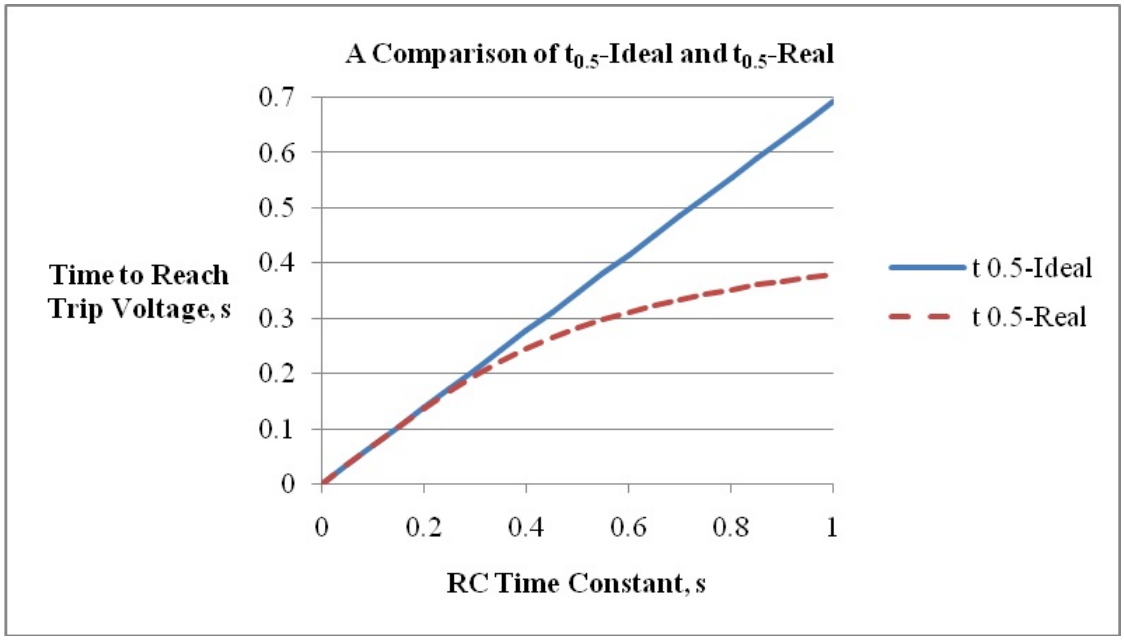

Figure 6.5: A Plot Comparing $T_{0.5}$-Ideal And $T_{0.5}$-Real

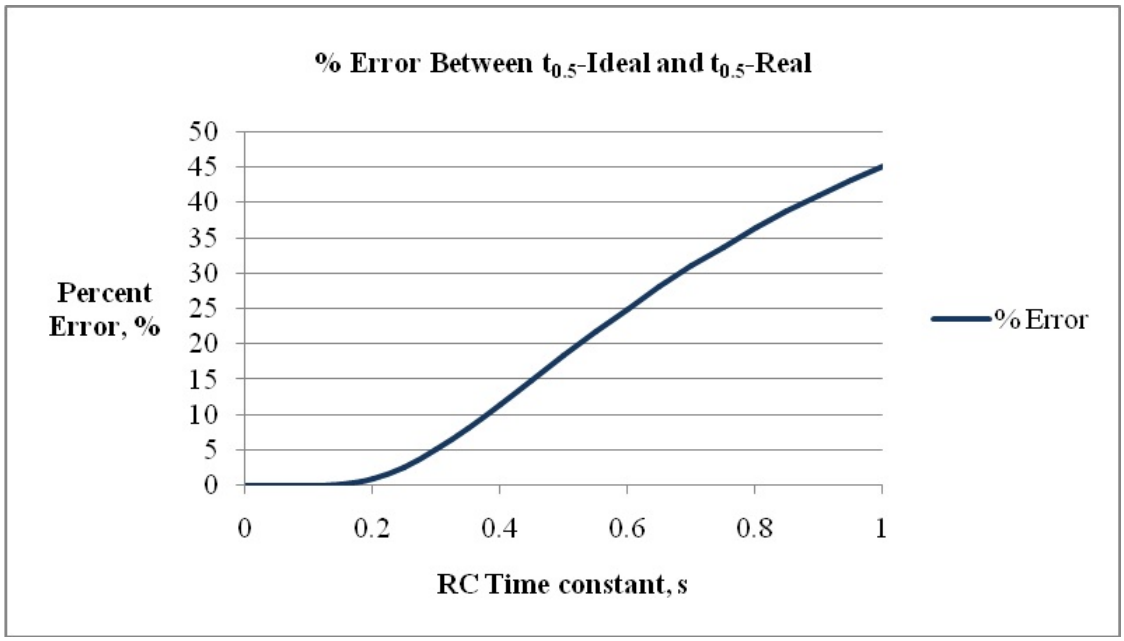

Figure 6.6: A Graph Of The Percent Error Between $T_{0.5}$-Ideal And $T_{0.5}$-Real

6.2 Implementation

The relative phase difference between V_{o1} and V_{o2} can be measured using a logical phase detector. Observe that the output values for V_{o1} and V_{o2} consist of logical "1's" and "0's." Therefore an Exclusive OR (EXOR) gate of a compatible logic family with the inverters can be used to detect the relative phase difference [23]. An EXOR gate, refer to Fig. 6.7, produces a high or "1" state only when the two inputs have opposite states. When the phase difference is 0°, the output is "0" and when the phase difference is 180°, the output is "1". If two 50% duty cycle pulse trains at the same frequency are input into the EXOR gate, with a relative phase difference between 0° and 180°, the output will be a Pulse Width Modulated (PWM) signal with a fundamental frequency twice that of the input pulse trains, where the duty cycle is linearly proportional to the phase difference. As the phase difference increases from 180° to 360°, the EXOR output duty cycle linearly decreases from 100% back to 0%. Therefore the EXOR gate is only useful as a monotonic phase detector for a phase difference range of 180°, either 0° to 180° or 180° to 360°. Furthermore, due to phase jitter, the EXOR phase detector operates best if the actual phase range avoids close proximity to either 0° (360°) or 180°.

Figure 6.7: Ex-OR Gate

Therefore to optimize the inverter circuit in Fig. 6.3 for use with an EXOR phase detector, two input pulse trains could be used that possess an initial phase difference of 45°. Then if the relative phase difference range resulting from the RC-inverter circuit is 0° to 45°, as could be the case with the circuit in Fig. 6.3 if the permissible nonlinearity is limited to 2.6%, V_{o1} and V_{o2} would have a phase difference range of 45° to 90°, which is within the optimal range for the EXOR phase detector. Since the duty cycle is proportional to C, a

suitable low pass filter will convert the PWM EXOR output signal to a Direct Current (DC) signal proportional to C.

6.3 Estimating Resistance and Capacitance

Now, consider the circuit shown in Fig. 6.8, where we are feeding in two inputs to the circuit. A counter and a D flip-flop is used to introduce delay in the inputs. This delays one of the inputs to the circuit by a phase difference of 45°. We have also added in a second resistance and capacitance between two of the inverters. The value of the constant capacitance is C_{min}, which is the minimum value of the variable capacitance, C_{ext}. A change in unknown capacitance, C_{ext} leads to a change in the phase difference between the two outputs V_{o1} and V_{o2}.

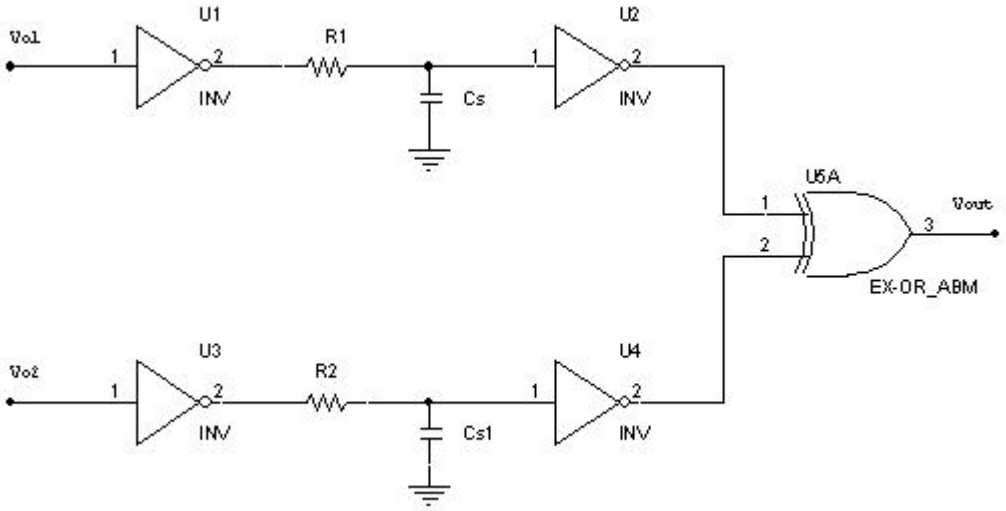

Figure 6.8: Two-input RC Inverter Circuit

Consider the capacitive sensor to have a capacitance range between 10pF to 150pF.

Hence,

$$\begin{aligned} \Delta C = & \quad 150 - 10 \\ = & \quad 140pF \end{aligned} \tag{6.7}$$

RC Delay, τ can be calulated to be

$$\begin{aligned} V_o = & \quad V_{in}\left(1 - e^{\frac{-\tau}{RC}}\right) \\ 2.5 = & \quad 5(1 - e^{\frac{-\tau}{RC}}) \\ \frac{1}{2} = & \quad 1 - e^{\frac{-\tau}{RC}} \\ e^{\frac{-\tau}{RC}} = & \quad 0.5 \\ \tau = & \quad -RC\ln(0.5) \end{aligned}$$

Hence,

$$\tau = 0.6931RC \tag{6.8}$$

Considering a clock of 1MHz, the output at the counter Q_o=500KHz which results in Time period, T = 2μs

Therefore,

$$
\begin{aligned}
R_1 &= \frac{\tau}{0.6931C} \\
&= \frac{2\times10^{-}6}{0.6931\times140} \\
&= 20.611K\Omega \qquad (6.9) \\
TotalDelay &= RC_{Tmax}\cdot 0.6931 \\
&= (20,611)\cdot(150)\cdot(0.6931) \\
&= 2.14\mu s \\
\tau_{min} &= RC_{Tmin}\cdot 0.6931 \\
&= (20,611)\cdot(10)\cdot(0.6931) \\
&= 0.143\mu s
\end{aligned}
$$

Therefore,

$$
\begin{aligned}
R_2C_T0.6931 &= 0.143\mu s \\
R_2\cdot(100pF)\cdot(0.6931) &= 0.143\mu s \\
R_2 &= \frac{0.143\times10^{-}6}{(100\times10^{-}12)\cdot(0.6931)} = 2061\Omega \qquad (6.10)
\end{aligned}
$$

6.4 Experimental Validation

The capacitance detection concept was implemented in circuit form for experimental validation. As shown in Fig. 6.9, the RC inverter circuit was implemented using an MC14049 CMOS inverter chip with a 100KΩ potentiometer and an external variable capacitor. The circuit was implemented on a breadboard and powered with +5V. The variable capacitor had a capacitance range of approximately 13pF to 133pF.

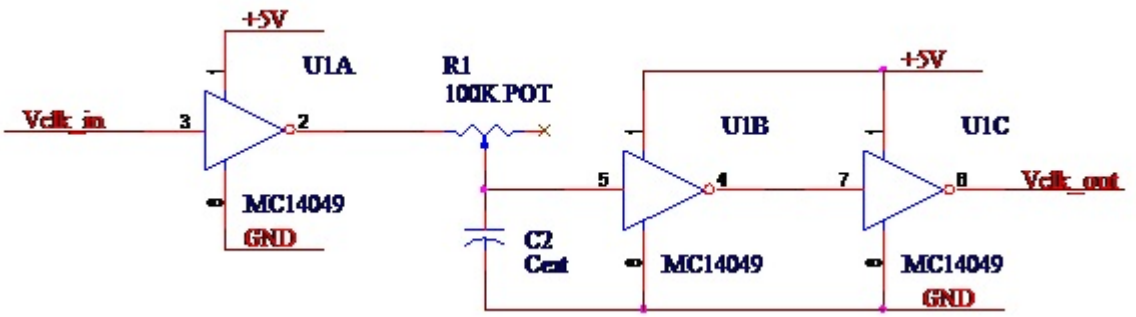

Figure 6.9: A Schematic Diagram of the Implemented RC Inverter Circuit

The RC inverter circuit in Fig. 6.9 was interfaced with a field programmable gate array (FPGA) [Xilinx XC3030A], general purpose I/O board, where the V_{clkin} generation circuit, the comparison pulse train circuit and the EXOR phase detector were realized. The output signal from the EXOR phase detector was input into a 4th order Butterworth lowpass filter with a 10KHz cutoff frequency to generate a DC voltage proportional to the capacitance being measured. Since the FPGA board had an onboard 20MHz clock oscillator circuit, a counter circuit was implemented to divide the clock frequency by 128 to generate a 156.25KHz 50% duty cycle clock signal to send to the RC inverter circuit as V_{clkin}.

The resistance of the potentiometer in the RC inverter circuit was selected by injecting a 156KHz clock signal, from a function generator, into the RC inverter circuit and into a second three MC14049 inverter circuit while monitoring the two output signals. An oscilloscope image of the output signals from both inverter circuits, with the potentiometer replaced by a short and the external capacitor removed, is presented in Fig 6.10(I). As expected, the phase difference between the two signals is approximately 0°. After the potentiometer and the external capacitor were reinserted into the RC inverter circuit, the external capacitor was set at its maximum capacitance of approximately 133pF. The potentiometer resistance was adjusted until a phase difference of approximately 45° between the two output signals was observed on an oscilloscope. A potentiometer resistance value of 6.07kΩ achieved this result. An oscilloscope image of the output signals from both inverter circuits, with the external

capacitor set to its maximum value and the potentiometer set to 6.07kΩ is presented in Fig 6.10(II), showing a phase difference of approximately 45°.

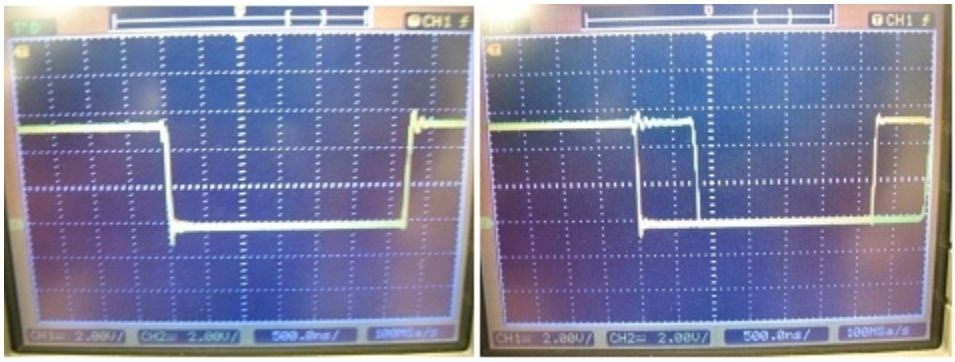

Figure 6.10: Oscilloscope Images Of (I) The Two Inverter Circuit Output Voltages With C_{ext} Removed And R Replaced By A Short (II) The Two Inverter Circuit Output Voltages With C_{ext} Tuned To Its Maximum Capacitance Value

An oscilloscope image of the output signals from both inverter circuits, with the external capacitor set to its minimum value and the potentiometer set to 6.07kΩ is presented in Fig 6.11(I), showing a phase difference of approximately 14°. An oscilloscope image of the output signals from both inverter circuits, with the external capacitor removed and the potentiometer set to 6.07kΩ is presented in Fig 6.11(II), showing a phase difference of approximately 8.4°. The phase difference in Fig. 6.11(II) is due to the product of the potentiometer resistance and the sum of the gate capacitance, C_g, of the inverter and all other stray capacitance in this part of the circuit. This capacitance, C_p, can then be estimated

$$\frac{C_{ex} + C_p}{C_p} = \frac{14°}{8.4°} \tag{6.11}$$

Where

- C_{ex} = external capacitance
- C_p = all other capacitance in the circuit

which results in a value for C_p of approximately 19.5pF. The data sheet for the MC14049UB specifies a typical input capacitance of 10pF and a maximum input capacitance of 20pF [40].

The second three inverter circuit was not used when the RC inverter circuit was interfaced with the FPGA board. Instead, its function was implemented inside the FPGA. A 7-bit synchronous counter circuit with a delay stage was implemented to produce the 156.25KHz clock signal, V_{clkin}, that was sent to the RC inverter circuit. The same counter, without the delay stage, was used to generate another internal 156.25KHz clock that was approximately 45° ahead of the return signal from the RC inverter circuit, V_{clkin}, when the external capacitance was at its minimum value. An EXOR phase detector was also implemented in the FPGA to compare V_{clkout} with the 45° phase leading clock. The PWM phase detector output signal was then fed into the 4th order Butterworth lowpass filter. The filter had an adjustable inverting gain stage and a level shifter that were tuned so that the minimum capacitance would result in 5V and the maximum capacitance would result in 0V.

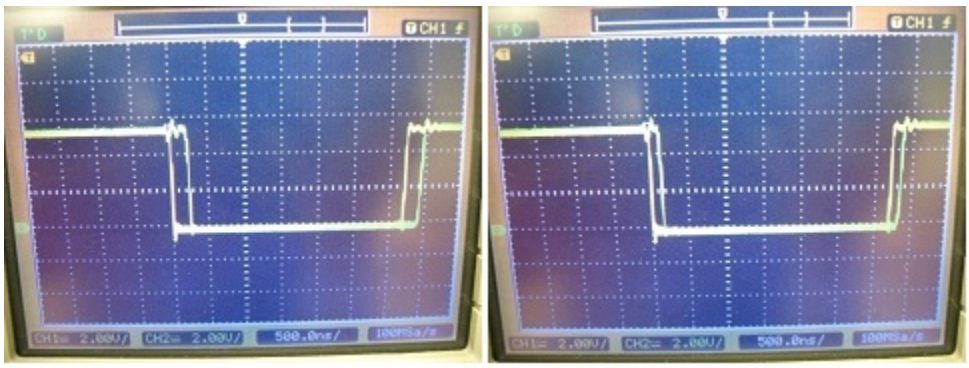

Figure 6.11: Oscilloscope Images Of (I) The Two Inverter Circuit Output Voltages With C_{ext} Tuned To Its Minimum Capacitance Value And (II) The Two Inverter Circuit Output Voltages With $R = 6.07k\Omega$ And C_{ext} Removed

Oscilloscope images of the PWM output signal from the phase detector for minimum and maximum external capacitance values are presented in figures 11A and 11B, respectively. For the minimum external capacitance value, the PWM EXOR output signal had a 26.56% duty cycle. With the maximum external capacitance value, the PWM EXOR output signal had a 43.75% duty cycle. The external variable capacitor was tuned to various capacitance values over its full range and the percent duty cycle for each tested value was obtained from

an oscilloscope, and used to produce the plot in Fig. 6.13. The plot shows an approximately linear response, with the majority of the nonlinearity due to observation uncertainty from obtaining the data from the oscilloscope screen.

A plot of the DC voltage values measured at the output of the low pass filter circuit as a function of external capacitance is presented in Fig. 6.14. The response is nearly linear, with a slight decrease in slope as the external capacitance is increased, which matched the model presented in Equation 6.6 and Fig. 6.5. A linear trend line has been added to the plot in Fig 6.14, with an R_2 value of 0.998. The interface circuit was tuned to the external variable capacitor to achieve a resolution of 41.76mV/pF.

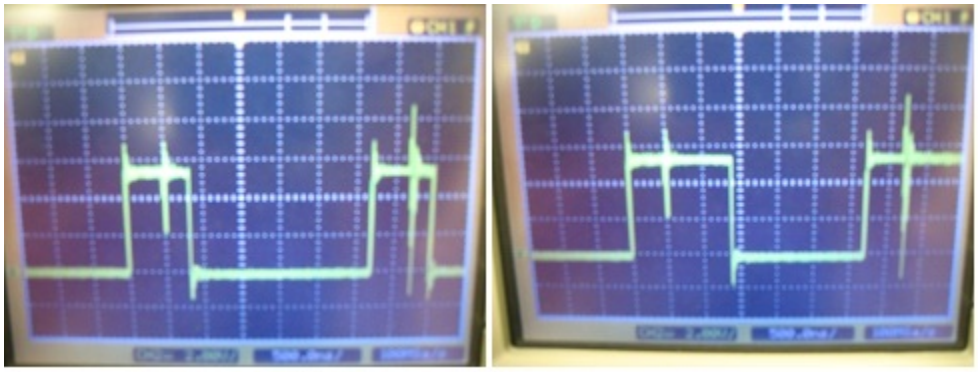

Figure 6.12: Oscilloscope Images Of (I) The Phase Detector Output With C_{ext} Tuned To Its Minimum Capacitance Value And (II) The Phase Detector Output With C_{ext} Tuned To Its Maximum Capacitance Value

Utilizing the data from Fig. 6.4, the V_c setting time would not exceed four state cycles. This corresponds to two T cycles. Therefore for this hardware implementation example, the capacitance detection rate would be 78.125KHz in the PWM signal. The low pass filter sets the detection rate achievable at the output DC signal, which in the example here would be a few KHz for a reasonable settling time. A higher order low pass filter with a much higher cutoff frequency would increase the detection rate at the output DC signal.

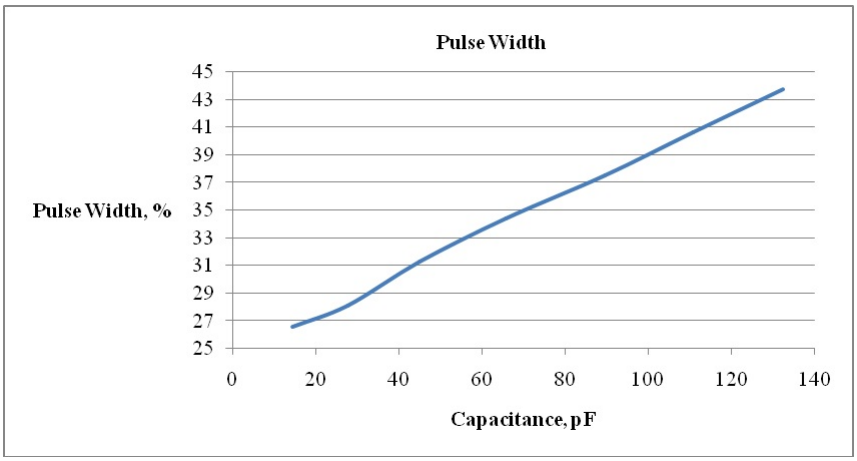

Figure 6.13: A Plot Of The Percent Pulse Width Of The EX-OR Output Signal As A Function Of External Capacitance

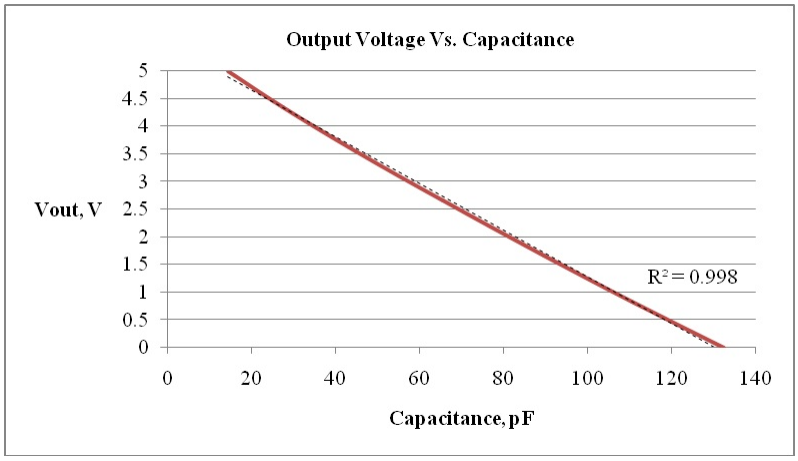

Figure 6.14: A Plot Of The Capacitance Detection Circuit Output Voltage As A Function Of Input Capacitance

6.5 Improved Implementation of this Technique [41]

An improved method for utilizing this capacitance measurement technique can be accomplished by adding an analog switch to fully discharge C_s before charging it during the subsequent measurement cycle. For this implementation, V_{in} is no longer a square wave with a 50% duty cycle. Instead, a narrow high-state pulse is used to fully discharge C_s and C_g through a low on-resistance n-channel MOSFET. The much longer low-state portion of the cycle is then used to measure C_s by delaying the state change through the RC network. A schematic diagram of an implemented prototype circuit is presented in Fig. 6.15. The low on-resistance n-channel MOSFET is utilized as an analog switch to discharge C_s and C_g every high cycle of V_{in}. When V_{in} is low, V_3 is low so that the MOSFET is off, and V_1 is high to charge C_s and C_g through R_1 until V_2 reaches the inverter trip voltage of 2.5V. Then V_{out} goes lows and stays low until V_{in} goes high at the beginning of the next cycle. Observe that V_{out} is a PWM signal where the duty cycle is proportional to C_s. No separate phase comparator is required for this circuit implementation. The value for R_1 and the frequency of V_{in} are selected so that C_{smax} results in Vout being high almost the entire period on V_{in}.

The 5V prototype circuit was implemented as a surface mount printed circuit board (2-layer, FR4) using a MC14049 CMOS hex inverter IC and a 2N7002K n-channel MOSFET. For C_s, a nominally 0.7-20pF variable capacitor was used. R_1 was a 100KΩ 1206 SMT resistor. Using these values, V_{in} was selected to be a 175KHz square wave with a 10.5% duty cycle generated using a BK Precision 4011A function generator. The DPDT switch was used to switch C_s from the measurement circuit to an external capacitance meter (Gwinstek LCR-821) so that the capacitance could be measured without disconnecting the circuit from the power supply (Agilent E3631A), the function generator and the oscilloscope (Agilent DSO3202A). Vout was subsequently low pass filtered, level shifted and amplified, using an inverting amplifier, to obtain the graph in Fig. 6.16. A linear trend line is included with the plotted data in Fig. 6.16 which shows the measurement of the unknown capacitance without any discernable nonlinearity in the measurement. V_{out} had a 61.4% duty cycle with

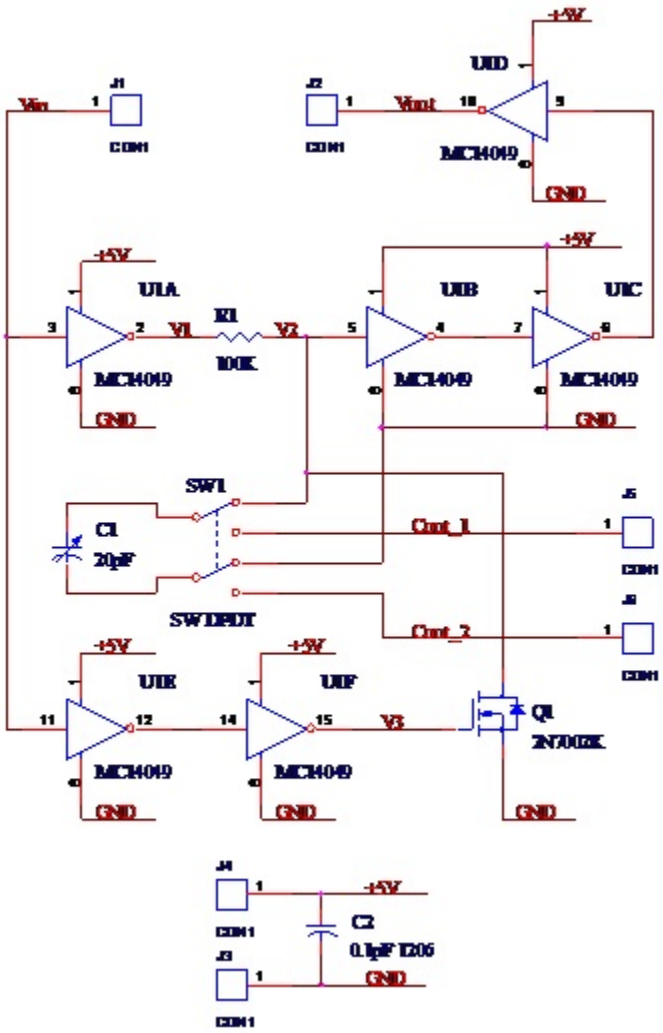

Figure 6.15: A schematic diagram of the prototyped improved capacitance measurement circuit based on phase delay

C_s disconnected from the circuit through the DPDT switch. This pulse width consisted of the 10.5% duty cycle C_s reset pulse width, the delay due to the R_1C_g product and the propagation delay through the four inverters in the RC delay circuit. With C_{smin}, measured as 2.27pF with the external capacitance meter, the duty cycle increased to 63.16%. When C_s was tuned to C_{smax}, measured as 21pF, the duty cycle further increased to 89.5%.

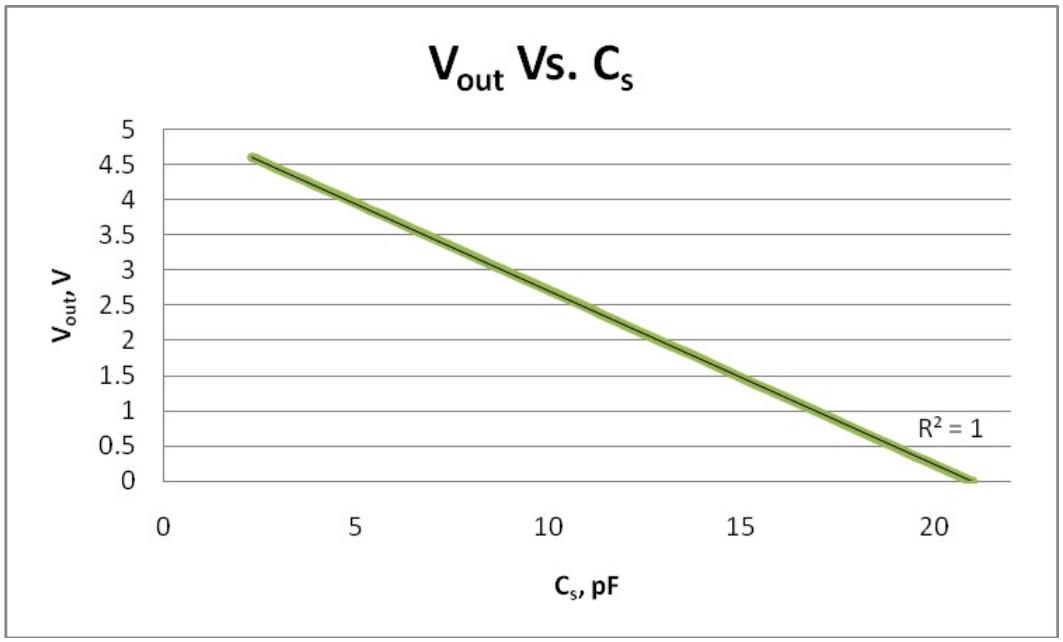

Figure 6.16: A plot of the measured output voltage versus C_s

Chapter 7

Conclusions

Many types of sensors and applications exist where an unknown capacitance needs to be accurately measured. One technique for accomplishing this is the use of a relaxation oscillator, where the frequency of the output square wave signal is proportional to 1/C. A frequency locked loop (FLL) technique was developed to convert the frequency of an input square wave to digital counts. The response of the FLL is proportional to 1/f, where f is the frequency of the input square wave. By combining the FLL with a relaxation oscillator, a linear response of counts versus capacitance can be obtained. This was demonstrated in an application where the mass of water was measured using a capacitive fringing field sensor implemented on a 2-layer PCB.

Additionally, two other capacitive interface circuit techniques were developed. The first technique measured capacitance by detecting the phase delay resulting from an RC product where C was the unknown capacitance. The second technique was similar to the first technique except that a switch was added to fully discharge the unknown capacitance between measurement cycles, yielding a more linear response.

Chapter 8

Future Work

Although the circuit response was just as expected, further improvements can be suggested. For the mass measurement technique, the mass should be calibrated in terms of the change in capacitance. This can be accomplished using the curve fitting tool in MATLAB.

Also, the capacitive sensor that was developed can be used for a variety of other purposes. For example, a touchscreen pad, a switch, to measure dielectric constant, etc. Basically, any parameter that changes the value of capacitance by interfering with the fringing fields can be calibrated with frequency. Hence, the value of that parameter can easily be read out using the Visual Basic GUI. This simple change in code will allow its use as a multiple sensor tool with varied applications. Furthermore, the FLL and the relaxation oscillator could be implemented as a CMOS ASIC and directly integrated with a MEMS capacitive sensor, such as a capacitive accelerometer or pressure sensor.

Bibliography

[1] R. Jachowicz, J. Weremczuk, Sub-cooled water detection in silicon dew point hygrometer, Sensors and Actuators A: Physical, Volume 85, Issues 1-3, 25 August 2000, Pages 75-83

[2] H. Eller, A. Denoth, A capacitive soil moisture sensor, Journal of Hydrology, Volume 185, Issues 1-4, 1 November 1996, Pages 137-146

[3] Marco Tartagni and Roberto Guerrieri, A Fingerprint Sensor Based on the Feedback Capacitive Sensing Scheme, IEEE Journal Of Solid-State Circuits, Vol. 33, No. 1, January 1998

[4] http://en.wikipedia.org/wiki/Relative_permittivity

[5] Rámon Pallás-Areny, John G. Webster "Sensors and Signal Conditioning" John Wiley & Sons, Inc., 1991

[6] Baxter, Larry, Capacitive Sensors, Design and Applications, IEEE Press, New York, 1997.

[7] Kenneth L. Kaiser "Electromagnetic shielding", CRC Press, 2006, Page 2-12

[8] http://pdf1.alldatasheet.com/datasheet-pdf/view/88616/AD/ADXL50.html

[9] http://www.analog.com/static/imported-files/data_sheets_obsolete/2044696ADXL50.pdf

[10] http://www.capsense.com/capsense-wp.pdf

[11] http://en.wikipedia.org/wiki/Loss_tangent

[12] http://en.wikipedia.org/wiki/Permittivity

[13] Frank M. L. van der Goes and Gerard C. M. Meijer, "A Novel Low-Cost Capacitive-Sensor Interface" IEEE Transactions on Instrumentation and Measurement, Vol. 45, No. 2, April 1996

[14] Nobumi Hagiwara and Takeo Saegusa "An RC Discharge Digital Capacitance Meter" IEEE Transactions on Instrumentation and Measurement, Vol. IM-32, NO. 2, June 1983

[15] Kazuyuki Kondo and Kenzo Watanabe, "A Switched-Capacitor Interface for Capacitive Sensors with Wide Dynamic Range", IEEE Transactions on Instrumentation and Measurement, Vol. 38, No. 3, June 1989

[16] Navid Yazdi, Haluk Kulah, Khalil Najafi, "Precision Readout Circuits for Capacitive Microaccelerometers" Center of Wireless Integrated Microsystems, University of Michigan, Ann Arbor, MI, USA

[17] Ferran Reverter, Manel Gasulla, and Ramon Pallás-Areny, "Ferran Reverter, Manel Gasulla, and Ramon Pallis-Areny", IMTC 2004 - Instrumentation and Measurement, Technology Conference, Como, Italy, 18-20 May 2004

[18] Jorge E. Gaitń-Pitre, Manel Gasulla, and Ramon Pallś-Areny, "Analysis of a Direct Interface Circuit for Capacitive Sensors", IEEE Transactions on Instrumentation and Measurement, Vol. 58, No. 9, September 2009

[19] Senturia, Stephen, Microsystem Design, Kluwer Academic Publishers, Boston, MA, 2001, pp. 393-394.

[20] Paemel, Mark, "Interface circuit for capacitive accelerometer", Journal of Sensors and Actuators, Vol. 17, 1989, pp. 629-637

[21] http://en.wikipedia.org/wiki/Frequency_synthesizer

[22] http://www.answers.com/topic/frequency-measurement

[23] Wolaver, Dan, Phase-Locked Loop Circuit Design, Prentice Hall, Englewood Cliffs, New Jersey, 1991, pp. 55-59.

[24] http://en.wikipedia.org/wiki/Barkhausen_stability_criterion

[25] http://en.wikipedia.org/wiki/Relaxation_oscillator

[26] http://www.thomasnet.com/articles/automation-electronics/relaxation-oscillators

[27] http://en.wikipedia.org/wiki/Ring_oscillator

[28] Cheng-Ting Ko, Sheng-Hsiang Tseng, and Michael S.-C. Lu, "A CMOS Micromachined Capacitive Tactile Sensor With High-Frequency Output", Journal of Microelectromechanical Systems, Vol. 15, No. 6, December 2006

[29] http://en.wikipedia.org/wiki/Field-programmable_gate_array

[30] Jan Axelton, "Parallel Port Complete", Lakeview Research, 1999

[31] H.A. Majid, N. Razali, M.S. Sulaiman and A.K. A'ain; "A capacitive sensor interface circuit based on phase differential method;" World Academy of Science, Engineering and Technology; Vol. 55; 2009; pp. 636-639.

[32] R.B. McIntosh and M.E. Casada, "Fringing field capacitance sensor for measuring the moisture content of agricultural commodities," IEEE Sensors Journal, Vol. 8, No. 3, March 2008, pp. 240-247.

[33] I. Bord, P. Tardy and F. Menil, "Influence of the electrodes configuration on a differential capacitive rain sensor performances," J. Sensors and Actuators B, Vol. 114, 2006, pp. 640-645.

[34] Z. Chen and R.C. Luo, "Design and implementation of capacitive proximity sensor using microelectromechanical systems technology," IEEE. Trans. On Industrial Electronics, Vol. 45, No. 6, Dec. 1998, pp. 886-894.

[35] A.P. Sample, A.J. Yeager and J.R. Smith, "A capacitive touch interface for passive RFID tags," Proc. of the 2009 IEEE Int. Conf. on RFID, Orlando, FL, April 27-28, 2009, pp. 103-109.

[36] F. Dewarrat, L. Falco, A. Caduff, M.S. Talary, Y. Feldman and A. Puzenko, "Measurement and simulation of conductive dielectric two-layer materials with a multiple electrodes sensor," IEEE Trans. on Dielectrics and Electrical Insulation, Vol. 15, Is. 5, Oct. 2008, pp. 1406-1414.

[37] Y. Isono and S. Aoyagi; "Surface micromachinable accelerometer using fringe electrical field of penetrating ferroelectric substrate and its characterization;" Proc. of 14th Int. Conf. on Solid-State Sensors, Actuators and Microsystems; Lyon, France; June 10-14, 2007; pp. 1219-1222.

[38] W.H. Hayt JR, Engineering Electromagnetics, McGraw-Hill Book Company, New York, 1981 p. 508.

[39] R. Dean, A. Rane and N. Hyatt, "A capacitive sensor interface circuit based on relative phase delay," Proc. of the ISA 55th International Instrumentation Symposium, League City, TX, June 1-5, 2009, (12pp).

[40] Technical Information Center, Motorola CMOS Logic Data, Series C, Motorola Literature Distribution, Phoenix, AZ, 1991, pp. 6-129 - 6-132.

[41] R. N. Dean and A. Rane, "An improved capacitance measurement technique based of RC phase delay," Proc. of the 2010 IEEE International Instrumentation and Measurement Technology Conference, Austin, TX, May 3-6, 1010, (4pp).