Fabrication of Macro Scale 3D Structures Using MEMS Technology

by

Colin Stevens

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Approved by:

Robert Dean, Chair, Assistant Professor of Electrical and Computer Engineering
Thaddeus Roppel, Associate Professor of Electrical and Computer Engineering
Thomas Baginski, Professor of Electrical and Computer Engineering

Abstract

The addition of Deep Reactive Ion Etching (DRIE) in the fabrication of micro-electro-mechanical-systems(MEMS) has enabled the creation of many new structures that were not previously feasible. By combining this technique with silicon wafer bonding Silicon-On-Insulator (SOI) technology and other silicon fabrication processes, a new large scale 3D structure has been created to support a large area single crystal Silicon membrane of 2-5 μm thick. The structure consists of a series of very high aspect ratio silicon ridges created using the DRIE process that are bonded using this silicon fusion bonding technique on both sides of the silicon membrane. This structure allows the membrane to withstand the stresses placed on it during vacuum testing by reducing the pressure of one side of the membrane to near vacuum.

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Chapter 1

Introduction

Over the last fifty years, advancements in integrated circuit processing technology have greatly improved our ability to create increasingly small patterns. For many years, however, the shape of the pattern could only be accurately controlled in two dimensions. The introduction of new technologies like Deep Reactive Ion Etching (DRIE) brought about the ability to create precisely controlled three dimensional structures, giving researchers the freedom to create many new designs. The goal of this project is to use DRIE along with other microfabrication techniques to develop a large area silicon membrane to act as a semitransparent window. This membrane needs to cover an area of 15mm X 15mm and be free of defects across the entire surface area. Also, the goal thickness is between $2 - 5\mu m$. This type of structure can have many different applications including uses as pressure sensors, microphones, and fluidic actuators. At the dimensions proposed, the window will be extremely weak and prone to damage due to tensile stress that will be applied during various processing stages. Therefore the membrane will need to be supported by a series of ridges that will be patterned onto the window area and protected during etching. These ridges will provide the strength required to protect the membrane during processing, as well as from any future stress to which the window might be subjected.

Although the supporting ridges provide the strength the membrane needs in order to scale to such a large surface area, they also have the undesired effect of masking some of the membrane surface area that would ideally be exposed. It is important, therefore, to create ridges that are as thin as possible to leave more of the surface area exposed, and to make the ridges as tall as possible to provide the strength necessary to support the large window area. To make a ridge as thin as possible, it is important that the thickness of the ridge not vary

at any point along the height of the ridge. This will allow the maximum amount of ridge area to support the membrane surface while providing the minimum amount of obstruction to the viewing area.

Another important factor is the strength of attachment of the ridge to the membrane. The attachment must be of sufficient strength to prevent the membrane from pulling too far away from its supporting structure; otherwise, the surrounding stress will become too great, causing the membrane to rupture. This thesis will focus on the fabrication techniques used in making a structure of sufficient strength to withstand the harsh processing techniques that a thin silicon membrane will be exposed to during fabrication, and will include design considerations taken into account in order to increase the process yield. The processes developed in this thesis were created for and in conjunction with the University of Missouri at Columbia. The remainder of this thesis will be organized as follows. Chapter 2 discusses the various fabrication techniques that have been applied to this project. Chapter 3 then provides a discussion of the equipment that has been used to implement the techniques listed in chapter 2. Chapter 4 then gives an explanation of the design decisions that were made as the project progressed, as well as the results that were obtained through each experiment, culminating in the fabrication of the final structure. Chapter 5 summarizes achieved goals of the project and provides a reference to the final processes developed. Chapter 6 then lists the options available for future improvements in the device structure and design, by recommending different pattern configurations, and discussing the use of new materials.

Chapter 2

Literature Review of Fabrication Processes

In this chapter, the basic concepts used in device fabrication will be explained. This includes the materials used, the techniques used to process the materials, and a review of selective existing literature on the subject.

2.1 Silicon on Insulator (SOI)

SOI technology is the process of creating a silicon wafer that consists of a silicon surface called the device layer, a buried oxide layer called the BOX layer, and a thick silicon supporting layer to provide mechanical strength called the handle layer. SOI wafers have become useful for creating very high speed CMOS circuits because of the BOX layer's ability to reduce the source to drain short channel leakage effect associated with nanometer scale devices. [21] SOI wafers can be fabricated in a number of different ways, and the thickness of the device and BOX layers can be very precisely controlled. In this project, the BOX layer protects the device layer during a silicon DRIE process to create a highly uniform thin silicon membrane over a large area.

The wafers used in this research are Silicon on Insulator wafers procured from Ultrasil Corp. The wafers have a handle thickness varying between 150μm and 500μm, an oxide thickness of 0.5μm, and a device layer thickness varying between 2 and 5μm. The wafers were fabricated by Ultrasil Corp. using a fusion bonding process in which one wafer is oxidized creating the desired thickness box layer, then another silicon wafer is fusion-bonded to the oxide layer to form the device layer. The device layer is then ground down using a chemical mechanical polishing (CMP) technique to the desired device layer thickness. The following sections describe the three main processes used to fabricate SOI wafers.

2.1.1 SIMOX Process

The SIMOX process uses ion implantation to deposit oxygen ions at specific depths which form the buried oxide layer. The depth of the implant is controlled by the energy of the beam, which controls the thickness of the silicon device layer at the surface. The width of the oxide layer is controlled by the duration of the implant. These two parameters can be tuned to create an SOI wafer with very precise dimensions. However, the increase in volume caused by the formation of oxide beneath the surface can create dislocations at the SI/SIO_2 interface which will increase with the width of the oxide layer. These dislocations can cause leakage between the source and drain of an electrical circuit fabricated on the device layer. Because ion implantation is used, the depth the oxygen ions can travel is limited, therefore only very then device layers can be created using this process on the order of 1μm. Also, the ion implantation process is very expensive to run, with slow wafer throughput. [3]

2.1.2 Bonded SOI Process

A second method of creating SOI wafers is to use Hydrophilic bonding and polishing. SiO_2 is grown on the surface of two silicon wafers which will become the Box layer. The surfaces of the wafers are made hydrophilic using a chemical solution, discussed in section 2.6.2, which will allow the two wafers to form an initial bond caused by Van Der Walls forces. The bond is then strengthened by annealing the two wafers in a furnace at a temperature above $1000°C$. After bonding, the backside of one of the wafers is ground down using a chemical mechanical polishing (CMP) process which can accurately thin the surface, with a total thickness variation (TTV) of approximately 1 - 1.5 μm on a 6mm wafer. Further increases in uniformity can the be achieved by using different polishing methods or by including a plasma etch to thin areas of the wafer which are out of tolerance. [10] The SOI wafers procured for this project were fabricated using the bonded SOI process in this subsection.

2.1.3 Smart-Cut Process

A final process called the Smart-Cut process attempts to combine the benefits of both the SIMOX and Bonded SOI processes. In this process a silicon wafer undergoes a hydrogen ion implant at the energy required to deposit atoms at the depth of the desired device layer. An oxide layer is also grown on the top of this wafer which will create the Box layer. A second wafer is then attached to a hydrophilic surface as discussed in the previous section. The two attached wafers are then placed into a furnace where they undergo a two step process. First, The wafers are heated to a temperature of between 400-600°C. At this temperature, microcavities filled with hydrogen gas form at the implanted depth, splitting the wafer along this plane. Second, the furnace is then heated to 1000°C to strengthen the bond of the hydrophilic attachment, thus completing the basic SOI wafer. The portion of the wafer that has been separated due to hydrogen expansion can then be removed, and the remaining silicon polished to remove the damage caused by the hydrogen bubbles. This process has an advantage over SIMOX in that the Si/SIO_2 interface is thermally grown and does not have the stress caused by ion implant [4]

2.2 RCA Clean

Before a silicon wafer can be processed, the surface must be clean of particles and impurities which can reduce the quality of the pattern, cause interference in the operation of electrical devices, and become a source of contamination in processing equipment such as the oxidation furnace. To remove these particles, William Kern, in 1965 with the RCA corporation, developed a cleaning process known as the RCA clean which has since become the standard in the industry. This process involves soaking the wafer in a series of chemical mixtures, each mixture serving a different cleaning purpose. Presented below is a table listing the standard processing steps used in the RCA clean to prepare the wafer for processing. [11]

Table 2.1: RCA Process

Process Name	Step	Mixture	Time	Temperature	Purpose
	A	IPA bath	1Min	Room Temp	Oil Removal
		DI Water Bath	1 Min	Room Temp	
SC-1	B	$1:30\%\ H_2O_2$ $1:29\%\ NH_4OH$ $5:DI\ H_2O$	5 Min	70°	Removes organic impurities
		DI Water Bath	1 Min	Room Temp	
	C	$1:49\%\ HF$ $50:DIH_2O$	30 Sec	Room Temp	Removes Hydrous Oxide
		DI Water Bath	1 Min	Room Temp	
SC-2	D	$6:DI\ H_2O$ $1:30\%\ H_2O_2$ $1:37\%\ HCL$	5-10 min	70°	Removes Heavy Metals
		DI Water Bath	1 Min	Room Temp	

2.2.1 Standard Clean 1 (SC-1)

The SC-1 solution is a mixture of 5 parts DI water, 1 part 30% concentration H_2O_2, and 1 part 29% concentration NH_4OH heated to 70°C. The wafer is submerged in this solution for 10 minutes. During this time, the H_2O_2 creates a hydrous oxide layer on the surface of the wafer, while the NH_4OH acts to remove this layer. This process repeats continuously and results in the removal of organic materials, light metals and other small particles on the surface of the wafer. Once this step is complete, the remaining hydrous oxide layer must then be removed. This is done by dipping the wafer in a mixture of 50 parts DI water, and 1 part HF acid at room temperature for approximately 30 seconds. [9]

2.2.2 Standard Clean 2 (SC-2)

The SC-2 solution is a mixture of 6 parts DI water, 1 part 30% concentration H_2O_2, and 1 part 37% concentration HCL heated to 70°C. The wafer is submerged in this solution for 10 minutes. This step removes heavier metals that are not removed in the SC-1 step. [9]

2.3 Masking Materials

When creating the masking layer for a macroscale MEMS pattern that will undergo plasma etching, a high selectivity between the masking material and silicon is desirable. If the selectivity is low, a thicker mask is required to withstand the hundreds of cycles of etching to which it is exposed. The selectivity of materials can vary with changes in the density, power, etching time, frequency, and chemical composition of the plasma. Changes in any of these variables to increase selectivity, however, can also have negative effects on the silicon etch rate, the amount of undercut, as well as the roughness of the sidewalls.

SiO_2 can be effectively used as an etching mask for both wet and dry etching with a high selectivity at about 100:1 silicon to SiO_2 when used in DRIE. Unfortunately, the time required to grow SiO_2 increases exponentially with thickness; therefore, growing enough oxide to withstand etching through a full wafer is not feasible.

For very deep structures, thick film photoresists, hence forth referred to as PR, can be used to mask the etching process. PR can have selectivities comparable to SiO_2, but can be applied in much thicker films. If the film thickness requirement becomes too high, the pattern resolution can be affected. Photolithography equipment can resolve patterns to a very high resolution. Associated with any particular resolution, there is a certain vertical tolerance called the depth of focus within which the pattern will remain in focus. Depth of focus can be defined by equation 2.1

$$DOF = \frac{k_2 R^2}{k_1^2 NA}, \tag{2.1}$$

where k_1 and k_2 are process dependent constants, NA is the numerical aperture, and R is the resolution to be achieved. In order to resolve a smaller feature, the depth of focus must be lowered. If the masking PR is too thick, the pattern will not maintain focus through to the surface of the resist, causing some areas to remain unexposed. [17]

2.4 Silicon Oxidation

It is well known that oxygen reacts with crystalline silicon to form SiO_2. This process is normally facilitated by exposing the silicon surface to either dry O_2 or H_2O vapor, and can be hastened by increasing the ambient temperature during exposure. This process can be modeled by equation 2.2. [17]

$$X_{ox}(t) = \frac{A}{2}\left\{\left[1 + \frac{4B(t+\tau)}{A^2}\right]^{\frac{1}{2}} - 1\right\}, \tag{2.2}$$

where A and B are the linear and parabolic rate constants determined by the crystal orientation, doping, pressure, and ambient temperature. The oxidation property of silicon is one of the major reasons silicon has found such widespread use in the electronics industry. The high electrical insulating property of SiO_2, and the ability to precisely control the thickness of SiO_2 that is formed, make it ideal for electronic devices such as MOS transistors and capacitors. Another property of silicon dioxide is that it is a very stable molecule both thermally and chemically, making this material useful for protecting the silicon during processing, and as a chemical etch mask.

2.5 Plasma Assisted Dry Etching of Silicon

The aspect ratio of a structure is a measure of the structure's longer dimension compared to its shorter dimension. The aspect ratio for the device being constructed is required to be very high, therefore the structure is fabricated by bulk micromachining a pattern of ridges using an ICP (Inductively Coupled Plasma) DRIE (Deep Reactive Ion Etching) system.

Plasma based etching of silicon has been around for many years, but only within the last twenty years has the technology evolved so that plasma based etching could be utilized for precise directional etching. The following sections will explain how plasmas are used to etch silicon, and discuss some of the modifications that have been made that have allowed for the anisotropic profiles created using the DRIE process.

2.5.1 Plasma Etching

Plasma is an ionized gas that consists of a high density of free electrons. This condition can be created by exposing the gas to a high electric field. As the energy from this electric field is imparted to the atoms in the gas, the electrons gain enough energy to break free of the atom and become ionized. Because the electrons are much lighter than the ions, they accelerate much faster in the presence of the electric field. As the electrons move in the electric field toward the electrode, some electrons can become trapped in the chamber wall creating a net negative potential, pushing away other electrons, and attracting ions. This force creates a sheath at the edge of the plasma with a very high electric potential thus accelerating the ions through the sheath, leaving a nearly charge neutral region at the center of the plasma. The benefit of creating a plasma when used for etching a material is that the energy imparted to the ions can cause reactions with other materials that would normally occur only when they are thermally excited to thousands of degrees K. By creating a plasma consisting of gas compounds that contain either fluorine or chlorine, silicon can be isotropically etched by placing the wafer inside the plasma allowing the excited species to chemically react with the silicon to form new gaseous species such as SiF_x or $SiCl_x$ which are the pumped out of the plasma chamber. This reaction occurs at all points where the etching gas comes into contact with the silicon and is directionless. [15] [18]

2.5.2 Reactive Ion Etching

Reactive Ion Etching is a modification of the plasma-based etching by positioning the silicon wafer at the bottom of the chamber below the generated plasma. This allows etching to occur through the physical bombardment of the energetic ions exiting the sheath of the plasma. In this method, physical sputtering and chemical reaction both occur to enhance the silicon etch. Noble gases such as argon can cause physical bombardment that can break off silicon atoms and give a directionality to the etch that is perpendicular to the surface, while remaining unreactive with the surface. Ions such as fluorine and chlorine also impact

the surface and contribute to sputtering, but upon impact they form a chemical reaction with the silicon converting it to a gas such as SiF_4. Other gasses like oxygen, when added to the plasma, have an opposing effect when reacting with the surface forming a passive SiO_xF_y layer. The SF_x ions also work to remove this passive layer. The alternating generation and removal of this layer also helps to change the profile of the etch. Therefore, the SF_6 to oxygen ratio is very important in controlling the anisotropic nature of the etch. [30]

2.5.3 Inductive Coupling of Plasma

A further modification of the plasma generation method is to use an inductive element that is tuned to the frequency of an RF power source. A large amount of current will flow through this inductive element, causing a varying magnetic field inside of the plasma. This changing magnetic field will cause an RF electric field in the plasma which accelerates the ions through the sheath. Generation using this approach can create higher plasma densities which increase both the directionality and the rate at which the silicon is etched. [8]

2.5.4 Deep Reactive Ion Etching

A further improvement in the Plasma etching process, referred to as the Bosch Process, because it was developed by Laermer and Schilp of Bosch, was to combine separate etching and passivating cycles to the Reactive Ion Etching process. [14] This is the process used at Auburn for anisotropic silicon etching. First, the standard cycle using SF_6 and O_2 plasma etches a trench in the surface of the silicon. Then a second cycle of C_4F_8 plasma reacts with the SF_6 to create a Teflon like coating that covers the bottom and sides of the trench to prevent further etching. The etching cycle is then repeated and the SF_6 and O_2 ions bombard the surface dissolving the passivation layer at the bottom of the trench and etching further into the silicon. Because the ions arrive mostly perpendicular to the surface, they do not dissolve the passivation layer on the sidewalls thereby leaving the silicon to the side

untouched. Very high aspect ratio trenches can be achieved using this process with reports as high as 107. [19]

2.6 Direct Wafer Silicon Fusion Bonding

Silicon fusion bonding is one method of bonding two silicon wafers together by annealing, under pressure, at very high temperatures. This method has distinct advantages over other methods such as anodic bonding and eutectic bonding, but can also be more challenging to perform a successful bond. An anodic bond can be established between a Si and a Borosilicate glass interface by applying a high electric field at a relatively low processing temperature of $300 - 450°C$. [22] Alternatively, a eutectic bond can be formed by placing an intermediate layer of a metal such as aluminum or gold that will form a eutectic with silicon, allowing it to melt at a much lower temperature, forming a eutectic bond that will hold the two silicon wafers together. While anodic and eutectic techniques have their uses, direct silicon fusion bonding has the distinct ability to bond two silicon interfaces without the need for an intermediate bonding material between the wafers. This is an advantage because it creates a very strong bond that, unlike the eutectic bond, can withstand high temperature processing.

Preparation of the wafers is very important to creating a successful bond. The two wafers must have a mirror finish and be completely free of particles. The surface should be very smooth and level, having a roughness of less than 10Å and a bow of less than 5μm. [22] To remove particles, the wafer surface can be cleaned with the standard RCA clean process in a clean room environment. Once the wafer has been cleaned, the surface must be made either hydrophobic or hydrophilic with each having a different theory of how the bonding mechanism occurs.

2.6.1 Hydrophobic Bonding

The first method used to bond silicon wafers, as shown by Q.-Y. Tong et al. [26], is to treat the surface with an HF bath prior to bonding. Without rinsing with DI water, the

wafer is spun dry and exposed to an infrared heat source to remove any moisture that might exist. This leaves the surface hydrophobic with hydrogen and fluorine molecules bonded to the surface from the HF bath. [26] When the wafers are brought together it is believed that the wafers are held together by a Van Der Wall force between the dangling $SI - F$ and $Si - H$ bonds across the surface. With a high temperature annealing, the bond strength increases.

2.6.2 Hydrophilic Bonding

The second and generally preferred method for bonding is to chemically treat the silicon wafer surface to make it hydrophilic. This can be accomplished by submerging the wafer in a solution similar to the SC-1 clean. R. Stengl et al. used a solution of 6 parts H_2O, 4 parts NH_4OH, and 1 part H_2O_2 heated to $50° - 60°C$. [23] The wafers are then rinsed with DI water, spun dry and heated above $45°C$. The wafers can then be pressed together to quickly bond due to the hydrophilic nature of the surfaces. By then annealing at a temperature around $1100°C$, the bond strength will increase forming a bond comparable to the strength of a $Si - Si$ bond. There are varying theories explaining the nature of this bond, but the popular theory is that the OH bonds on the surface of the wafer introduced by the hydrophilizing solution undergo the following chemical reaction at temperatures above $1100°C$. [7]

$$\equiv SiOH + HOSi \equiv \quad \longrightarrow \quad \equiv SI - O - SI \equiv + H_2O \tag{2.3}$$

2.6.3 Bond Analysis

Because of the sensitivity of the bonding process to particles and deformations, it is necessary to verify the success of the bond once the process is complete. There are numerous methods available to evaluate the bond. First, the wafer can be cleaved in two and the interface can be measured extremely accurately. This method, however, is destructive to the wafer and any devices on the wafer would be rendered non-functional. Other evaluation

methods that are non-destructive include x-ray topography, acoustic imaging, and infrared imaging.

2.7 Oxide Release and Stiction

One of the most important attributes that makes MEMS devices valuable is their use of structures that can move freely when exposed to an external force. One way to create these free moving structures is to etch the pattern into the device layer of an SOI wafer, and then dissolve the oxide layer below the pattern in a chemical bath. When the structures become very small, however, forces that were negligible at large scales become more important. In devices with a large mass, inertial forces are the predominant force explained by the equation $F = ma$, but as the device scales down in size, the mass reduces by the cube. Also as devices shrink, magnetic forces are significantly decreased. [6] Other forces, however, become very important at small sizes. Two of these forces include Van der Waals forces and capillary forces. Van der Waals forces are relatively weak forces caused by charge imbalances between many molecules. When two surfaces come into contact with each other, and these Van der Waals forces are stronger than the restoring spring force of the structures, then the structures will become stuck together. Capillary forces are characterized by the tendency of a liquid to be pulled into a small opening. This movement is caused by attractive forces between the liquid and the material of the wall. At large sizes the inertial force due to mass would overcome these small forces, but for MEMS devices these forces overcome the inertial forces causing the device to become stuck. Therefore, the sticking effect cause by these two events has come to be known as stiction, and they present a major challenge to the fabrication of MEMS devices that are not a consideration for non moving integrated circuits. The main occurrences of this effect is during the release process, and during operation in a non ideal environment. During fabrication, if the device was to be directly removed from the liquid and allowed to dry, the liquid remaining between the structures would pull the structures toward the surface and toward each other, possibly breaking the structure. A variety of

methods have been successfully tested by different research groups for releasing structures, including evaporation drying, sublimation drying, SAM (Self Aligning Monolayer) coating, and VPE (Vapor Phase Etching). [5, 28, 16, 1] In face one group from UCLA performed a comparative evaluation of all of these different release methods showing that in their results, Critical point Drying proved to be the cleanest and most consistent release method for the MEMS device they were testing. [13]

2.7.1 Evaporation Drying

Evaporation drying, the simplest form of drying, involves submerging the MEMS sample in a liquid that has a low surface tension with respect to air. The sample is then removed from the liquid and either allowed to air dry, or heated to a high temperature to evaporate the liquid. As evaporation occurs, the liquid will be pulled out from between the structures forcing them together. If the structures are too close together, and the surface energy is high enough, then stiction will occur. For two parallel structures, the force caused by the surface tension of the liquid to air interface is given as

$$F = \frac{2A\gamma_{la}\cos(\theta_C)}{g}, \tag{2.4}$$

where A is the surface area of the wetted region, γ_{la} is the surface tension of the liquid to air interface, g is the distance between the two structures, and θ_C is the contact angle between the liquid and the solid and determines if the surface is hydrophobic or hydrophilic. As the surface tension γ_{sl} increases, so does the force acting on the structures. [25] The γ_{sl} of DI water is relatively high at $73.05mN/m$. Isopropyl alcohol has a much lower γ_{sl} at $21.7mN/m$. Isopropyl alcohol will exert less than one third the capillary force during evaporation than DI water.

2.7.2 Supercritical CO_2 Drying

Critical point drying is a popular method for removing the liquid from between compliant structures. Once the structures have been released in the HF bath, the device is transferred to a solution of high purity alcohol and placed into a sealed chamber. Liquid CO_2 is allowed to slowly flow into the chamber while the alcohol is slowly purged. After all of the alcohol is purged, and the device is surrounded by only liquid CO_2, the chamber is then heated, causing an increase in pressure. When the temperature of the CO_2 increases above 31.1° and the pressure increases above 1070PSI, the CO_2 will reach a supercritical state in which the interface between the liquid and the gas disappears, and the surface tension becomes zero. When this point is reached, the chamber can be slowly purged. As the chamber is purged, the pressure decreases and the supercritical CO_2 becomes a gas. The gas can then be purged from the chamber thereby avoiding the stiction due to liquid surface tension.

2.7.3 Sublimation Drying

Some materials when brought to a very low pressure will convert directly from a solid to a gas, skipping the liquid phase. This process is called sublimation, and is useful in preventing stiction between microstructures because capillary action only occurs when there is surface tension created by a liquid-to-gas interface. Different Materials will sublimate under varying conditions, therefore some materials are more useful for sublimation drying than others. Some of the properties that make a material useful for sublimation drying include:

- Maintaining a liquid phase at room temperature.
- Having a freezing temperature at just below room temperature.
- Having a high vapor pressure at which the material can sublimate.

- Possessing minimal expansion when freezing.

A research group at Berkeley has successfully used a form of alcohol called Tert-Butanol as a sublimation material which has many of the properties previously mentioned. [28]

Chapter 3

Processing Equipment

The Alabama Microelectronics Science and Technology Center located at Auburn University is equipped with all of the tools necessary to facilitate the fabrication of MEMS devices. By changing the manner in which these tools were used, the outcome realized also changed significantly. This equipment, and the parameters by which theory was used, will be referenced heavily throughout this document. In the next few sections, a brief description of the most frequently used pieces of equipment and their operation will be discussed.

3.1 Cleaning Equipment

As explained in various sections of this paper, cleanliness plays an important role in the successful fabrication of microelectronic as well as MEMS devices. The STI Semitool Spin Rinse Dryer shown in Figure 3.1 is a tool designed to assist in maintaining a particle-free wafer.

Figure 3.1: Spin Rinse Dryer

There are two versions available in the lab to accommodate 4" and 5" wafers. This device sprays deionized water across the surface of the wafer, while spinning, to remove particles and other loosely held contaminants. The wafer then enters a drying phase where the spin speed of the wafer is increased, and heated nitrogen is blown across the wafer to remove the water from the previous rinse cycle. This step is important for cleaning wafers during multiple steps of the fabrication process.

3.2 Patterning Equipment

After cleaning the wafer, a pattern can then be transferred to the wafer that will realize the intended design. This pattern is normally created using PR. This is a material that is sensitive to light and acts as a masking material to other processes.

3.2.1 Hexamethyldisilazane (HMDS) Chamber

Before PR can be applied to the wafer surface, the wafer must be primed to accept the resist. At room temperature, water molecules from the air can attach to the wafer surface causing PR to attach to the water molecules instead of the silicon. To remove the water, the wafer is placed in a dehydration oven and heated to $120°C$ for twenty minutes. After dehydration, a primer of HMDS is then coated over the wafer which adheres well to both the silicon and the PR.

HMDS is normally applied in one of two ways. One way is to pour the HMDS onto the wafer in liquid form and spin the wafer until only a very thin coating of HMDS remains. The HMDS must then be dried completely before the resist can be applied. This method has the advantage of being easily added to the fabrication process, but has drawbacks in that most of the HMDS is wasted during spinning, and if the HMDS is not completely dry, the HMDS can break down the bottom layer of PR, reducing adhesion instead of improving it. [29]

The second method is to apply the HMDS in vapor form. Because only a few monolayers of HMDS are required to adhere to the resist, the HMDS can be allowed to evaporate and the vapor flows over the wafer. The molecules that attach to the wafer will provide a sufficient amount of coating needed for resist adhesion. This is the method used at Auburn. Shown below is the chamber in which the HMDS is allowed to evaporate and attach to the wafer.

Figure 3.2: Vapor HMDS Application Chamber

3.2.2 Photoresist Spinner

A photoresist spinner is used to accurately control the thickness of the PR film applied to the wafer. A uniform thickness is achieved by spinning the wafer at varying speeds and allowing the PR to spread over the entire surface area. Slower rpm's will give a thick coating, while faster rpm's will give a thinner coat. Longer spin times will help to increase the uniformity of the coating over the wafer.

Figure 3.3: Photoresist Spinner

3.2.3 Matrix Oxygen Plasma Asher

The Matrix oxygen plasma asher is a type of plasma etcher that is used to remove organic material from the surface of the wafer, usually PR. The oxygen plasma reacts with the PR forming an ash that is then removed by a vacuum pump. The parameters that can be modified include the power of the plasma, the flow of oxygen, and the time of exposure. This device has two main roles in MEMS processing. The first is called a descum step. This is a short interval treatment meant to remove excess unwanted PR from the UV exposed areas of a developed pattern. This step is particularly important when the process calls for a wet chemical etch. Even a very thin film of PR that has not been fully removed will

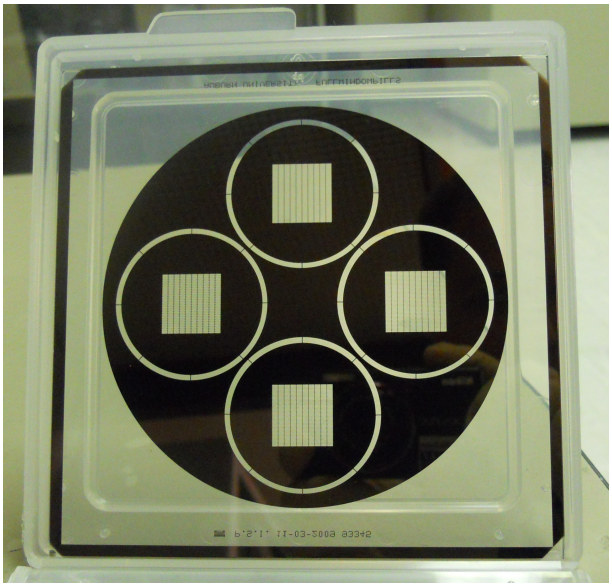
completely mask the pattern from etching. The second role this device plays is to fully strip the remaining PR after processing is complete.

Figure 3.4: Matrix Oxygen Plasma Asher

3.2.4 Karl Suss MA/BA6 Contact Aligner

This device creates a pattern on a PR film by bringing a patterned mask in direct contact with the surface of the wafer and subjecting the exposed areas to a UV light source. This equipment has the capability of achieving a maximum resolution of 0.7μm, and performing backside alignment functions which is essential for creating the 3D structures involved in this project. A high intensity Hg lamp provides a UV light source for PR exposure, which operates at 365nm (i-line) and 436nm (g-line). Wafer sizes of up to 150mm can be patterned using this equipment.

(a) Karl Suss MA/BA6 Contact Alligner



(b) 5” Soda Lime Photolithography mask with chrome pattern

Figure 3.5: Photolithography Equipment

3.3 Silicon Processing Equipment

Silicon is a very strong material with compressive strength up to 80% to that of steel, making this material very useful in MEMS devices. While having a very strong compressive strength, it lacks the ability to bend plastically, meaning that the material can fracture easily when bent. Specific tools have been developed that can create structures on the desired scale, while preventing fracture. Using a DRIE system, precise etching can make deep grooves in the silicon, and CVD systems can deposit silicon with very high accuracy. Furthermore, oxidation of the silicon to form silicon dioxide can protect the surface from chemical reactions, as well as forming an electrically insulating barrier.

3.3.1 Inductively Coupled Plasma (ICP) Deep Reactive Ion Etch (DRIE)

The STS Advanced Silicon Etcher (ASE), shown in figure 3.6, uses an inductively coupled plasma to etch the silicon surface using chemically reactive SF_6 ions. Using an induction coil to generate the plasma has the benefit of being able to create a very high density plasma, and because the coils are located outside of the chamber, contamination that is associated with other methods of plasma generation does not occur. The platen, onto which the wafer is attached for etching, is connected to a RF source that has two settings at either 13.56MHz or 380KHz. A Bosch process is implemented to create an anisotropic etching profile by subjecting the surface to multiple SF_6/O_2 etch and C_4F_8 steps. [14]

Figure 3.6: STS Advanced Silicon Etcher

Multiple parameters can be altered which modify the etch profile. These parameters include the following:

- Gas Flow Rate

  The mixture of O_2 to SF_6 determines how aggressively silicon is etched. The higher the ratio of SF_6, the faster and more isotropic etch is during each cycle.

- RF Power

The power of the plasma determines the amount of directionality the ions have toward the wafer surface. An increase in the power will cause a more anisotropically etched structure.

- Frequency

  There are two frequency settings available for use. The first is 13.6MHz and the second is 380KHz. Use of the 380Khz setting can a phenomenon known as footing at the interface between the Si and the SiO_2 etch stop layer in which energetic ions can become trapped in the SiO_2 layer giving it a positive charge. This charge deflects incoming ions as it approaches the surface, causing the etching species to etch the sidewalls at a higher rate. A common issue associated with DRIE etchers that can increase the likelihood of footing is an occurrence known as the bullseye effect. This effect is characterized by the non uniform etching of silicon across the surface of the wafer. The silicon has a tendency to etch at a faster rate toward the edge of the wafer than in the center. In order to completely expose the SiO_2 layer over the entire wafer, some portions will be required to be over etched. This over exposure of the oxide layer to ion bombardment increases the likelihood of footing. By using the low frequency setting, the surface can be over etched without resulting in the footing effect. [27]

- Etch cycle time verses passivation cycle time

  The ratio of etching to passivation plays a role in the aspect ratio of the structures. An increase in the etching ratio will allow more silicon etching during each cycle and increase the amount of lateral silicon etching under the pattern. An increase in the passivation ratio will increase the time required for the etching gas to break through the passivation layer, thus shortening the amount of time silicon is exposed for etching.

A number of different research groups have used the preceding variables to control the sidewall profile effectively. One group used an alternating sequence of the Bosch process with an isotropic dry etch to create tapered sidewalls with a precisely controlled angle. [20]

Another group created very high aspect ratio trenches by slowly increasing the flow of SF_6 during processing. This increase compensates for the reduced ability of the ions to reach the surface at deeper trench depths maintaining a consistently high aspect ratio. [2]

The Recipe MORGNSOI was used for etching all of the silicon wafers in this project. The parameters of this process are shown in Table 3.1.

Table 3.1: MORGNSOI DRIE Recipe

Cycles				
	O_2	SF_6	C_4F_8	Time
Etch Cycle	13 sccm	130 sccm	0 sccm	13Sec
Passivate Cycle	0 sccm	0 sccm	85 sccm	7 Sec
Power				
	Range	tolerance	match load	match tune
13.6Mhz connected to Coil	600W	99%	50%	50%
Platen connected to 13.56mhz	0-300W	99%	50%	50%
Helium Leakup				
Test Time	30 Sec			
Max Leakup Rate	30mTorr/min			

3.3.2 Oxidation Furnace

The oxidation furnace, used to oxidize silicon, is a three tube horizontal furnace that uses a controlled flow of oxygen, hydrogen, and nitrogen gas to control oxide growth. Pure oxygen can be used to grow extremely pure thin layers of oxide, while the addition of hydrogen allows for thicker but lower quality oxide layers. Nitrogen is also used to both prevent oxide formation, and to purge the chamber of impurities. The furnace is a three zone resistance heated furnace that can be set to temperatures between 400 and 1200 $^{\circ}C$.

Figure 3.7: Oxidation Furnace

3.4 Electron Beam Evaporation and Sputtering System

The CHA Mark 50 electron beam chamber shown in Figure 3.8 is used to deposit metal layers on the surface of a device with high accuracy. The electron deposits material by using a magnet to focus the electron beam onto a target crucible of the metal. The metal then evaporates and is deposited onto wafers suspended in a planetary above the crucible. This process takes place under a high vacuum which results in a very high quality film that can be deposited at a high rate (50-500nm/min). [17]

Figure 3.8: CHA Mark 50 dual E-beam/sputter/ion gun deposition system

3.5 Evaluation Equipment

While creating the fabrication process for these devices, each step had to be carefully analyzed to ensure the correctness of the procedure. The evaluation tools available at Auburn have greatly increased the speed and quality of the fabrication process. The following sections describe some of the evaluation equipment used, and their role in this project.

3.5.1 C-Mode Scanning Acoustic Microscope

The C-Mode Scanning Acoustic Microscope (C-SAM) is a tool that uses ultrasonic energy between the range of 5Mhz to 400Mhz to create an image of the object by recording the amount of acoustic energy reflected at various depths in the device being scanned. The C-SAM is the acoustic equivalent of RADAR. By using lower frequencies, the sound wave can

penetrate deeper into the object before reflecting back. Although these frequencies provide a lower resolution image, they can be used to create an image of the interior of the object. This tool has been useful in characterizing the wafer bond process to determine which processes worked and which did not.

Figure 3.9: C-Mode Scanning Acoustic Microscope (C-SAM)

3.5.2 Alpha-Step Profilometer

The Alpha-Step 200 pictured in Figure 3.10 measures variations in surface height from $500\mathring{A}$–$160\mu m$. This variation is measured by moving a stylus along the surface measuring its deflection over a series of points. This tool is useful for measuring PR thickness as well as silicon etch depth up to $160\mu m$.

Figure 3.10: Profilometer

3.5.3 Prometrix FT-750 Interferomemeter

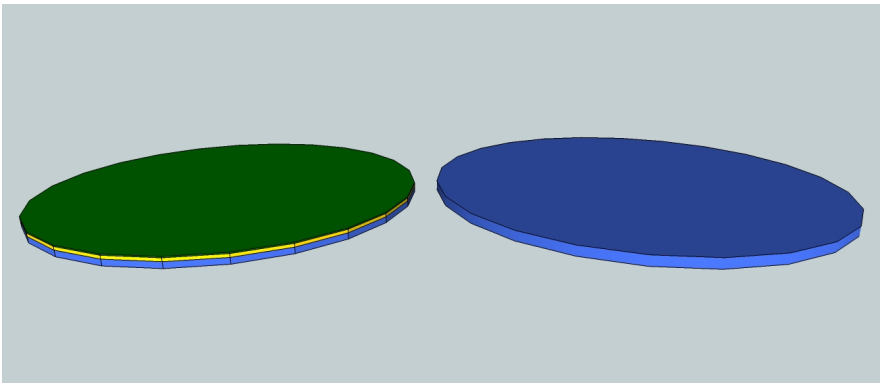
Another piece of equipment that was vital in analyzing the silicon structures is the interferometer shown in Figure 3.11. Auburn has two interferometers which perform different functions. The first is the Prometrix interferometer which can be used to determine the exact thickness of oxide grown on a silicon surface, as well as the thickness of spun-on PR. The second interferometer can determine the change in flatness of a surface using image processing. This was a valuable tool for measuring the silicon etch depth when the operating region is beyond the range of the Alpha-Step profilometer of the previous section.

Figure 3.11: Interferometer

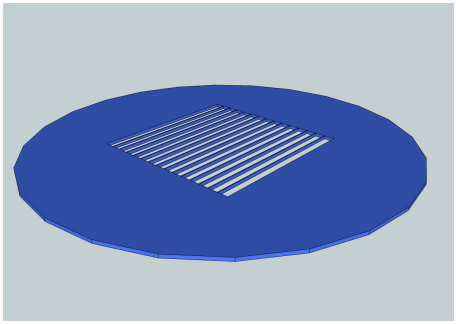
Chapter 4

Design and Fabrication

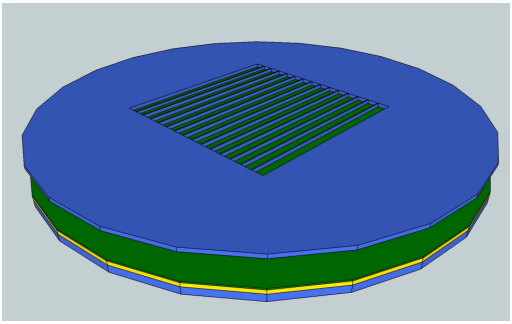
The general process flow for creating the desired structure, shown in Figure 4.1, begins by taking a double side polished, low resistivity wafer, and an SOI wafer with an extremely thin device layer. The first ridge pattern is transferred to the silicon wafer, and etched all the way through using DRIE (Figure 4.1(b)). The silicon wafer is then bonded to the device layer side of the SOI wafer (Figure 4.1(c)) by using a hydrophilic silicon fusion bonding technique described in section 2.6. After the two wafers are bonded together, the double wafer is then turned over, and the handle side is etched until the oxide layer, which is depicted in yellow, is exposed. The Box layer is then etched away in a solution of BOE which will expose the silicon membrane between the ridges on both sides of the wafer, and leave oxide beneath the ridges to secure the ridges to the membrane (Figure 4.1(d)). Once the oxide is removed, the device can then be stress annealed in a high temperature furnace at 1000°C and a layer of metal deposited on the surface to create a good electrical connection.



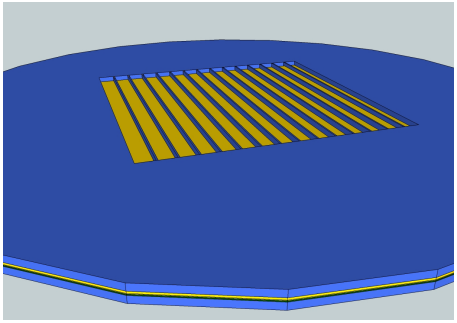
(a) Begin with Silicon and SOI wafers



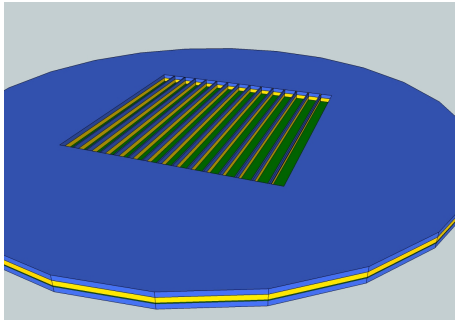
(b) Etch Through a Silicon Wafer



(c) Bond Etched Wafer to SOI



(d) DRIE Etch SOI Handle Layer



(e) BOE Etch Oxide layer

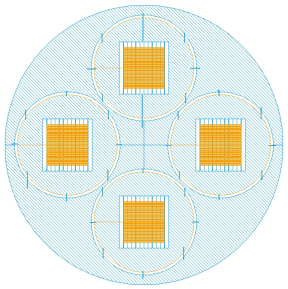
Figure 4.1: Process Flow

4.1 DRIE Undercut Evaluation

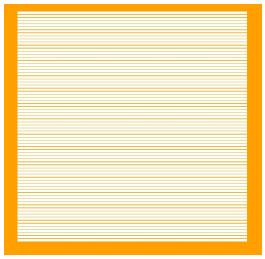
Minimizing the amount of undercut caused by the etching process is important to creating the strongest possible supporting structure while covering a minimum amount of membrane area. If there is too much negative undercut, meaning the ridge is thinner at the bottom of the trench than at the top, the membrane will have more space to flex and will cause a decrease in bonded surface area, increasing the potential of failure due to a weak bond. Conversely, The trench can have a positive undercut, meaning that the ridge is wider at the bottom of the trench than at the top. If this occurs the amount of exposed membrane will be decreased. The first step in the project for the University of Missouri is to determine what type of aspect ratio is achievable using Auburn's standard silicon DRIE recipe.

Two sets of test structures, shown in figure 4.2, were created using the MORGNSOI recipe detailed in Appendix 3.1. The pattern in figure 4.2(b) consists of a series of ridges that are $8\mu m$ wide with a spacing of $192\mu m$. The pattern in figure 4.2(c) contains a series of $60\mu m$ wide ridges with a spacing of $1470\mu m$ between them. To evaluate the amount of undercut that resulted, a cross section of the ridges was taken by potting the wafer in an epoxy, and grinding the wafer down until the side of the ridge was viewable under a microscope.

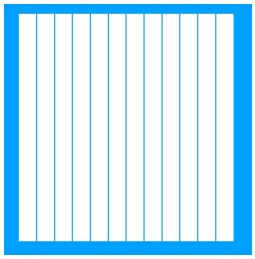
The patterns were exposed onto a $600\mu m$ thick single side polished silicon wafer with a $\langle 100 \rangle$ lattice orientation. The wafers have a p-type boron impurity doping with a sheet resistance of between $0.1 - 10\Omega/\square$. The $55\mu m$ pattern was etched $500\mu m$ into the wafer, while the $8\mu m$ pattern was etched $75\mu m$ with the expectation that an aspect ratio of 10:1 was achievable. As shown in figure 4.3, the large ridge pattern achieved an aspect ratio of 14.35:1 while the small ridge of figure 4.4 had no noticeable undercut at a depth of $75\mu m$.



(a) Full Wafer View



(b) Thin Ridges



(c) Small Ridges

Figure 4.2: Undercut Evaluation Masks

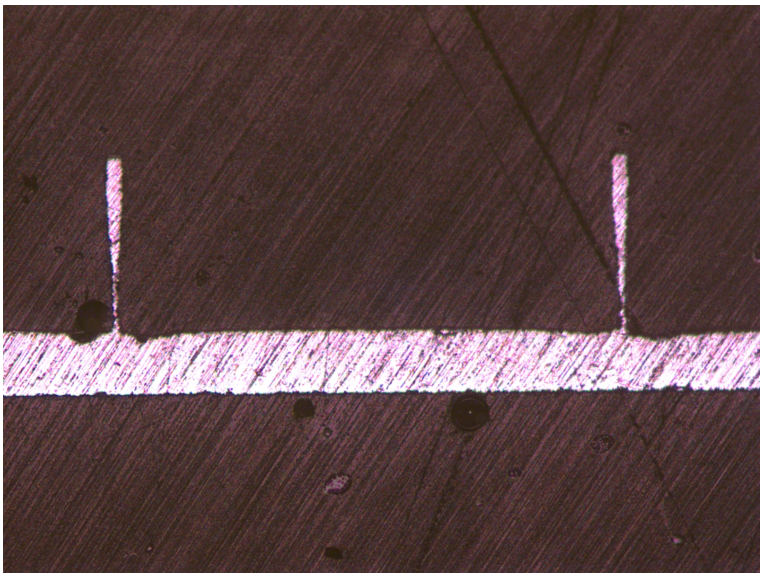


Figure 4.3: Large Test Ridges

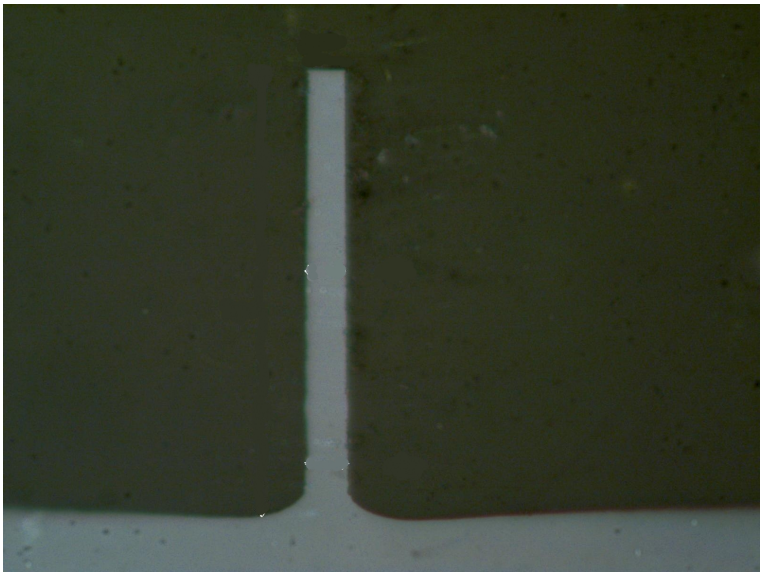


Figure 4.4: Small Test Ridges

4.2 Sacrificial Islands

By reducing the spacing between the ridges, the amount of undercut can be greatly reduced without changing the DRIE recipe. A new mask was designed with a blocking area filling in the spacing between each ridge shown in figure 4.5. A $40\mu m$ gap exists between the side of the ridge and the sacrificial island. This small gap limits the ability of the SF_6 to penetrate the passivation layer as the trench becomes deeper, thus reducing the isotropic etch time during each cycle. Once the wafer has been etched completely through, the island drops through leaving only a series of ridges with extremely high aspect ratio.

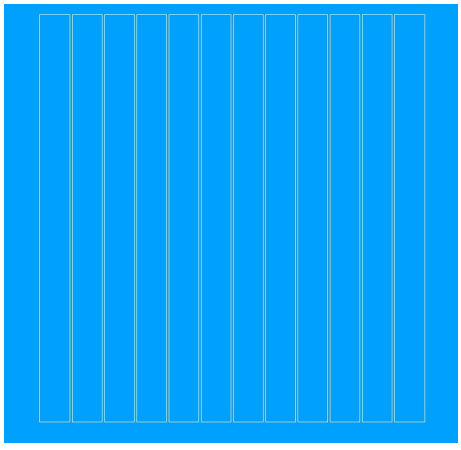
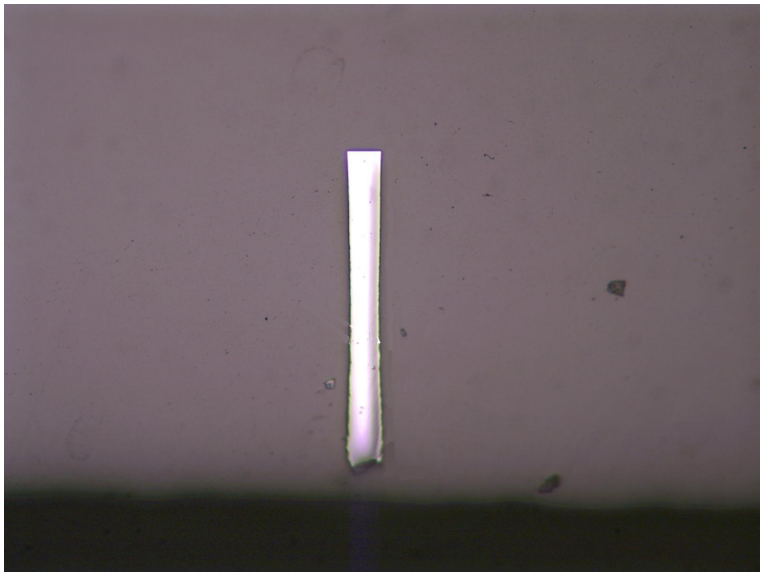
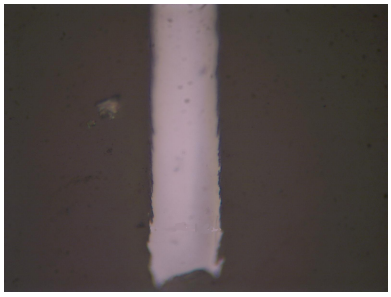


Figure 4.5: Sacrificial Island Pattern

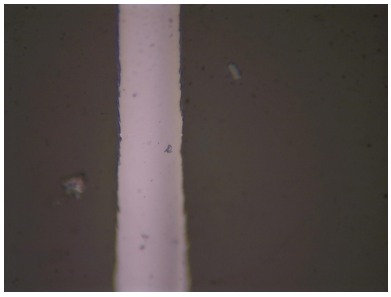
The ridge shown in figure 4.6 shows the results of an etch using this pattern. The undercut due to the isotropic etching has been greatly reduced, leaving a straight sidewall with a much improved aspect ratio of 41.6:1 to the center of the ridge, then correcting itself in the opposite direction as the ability of the plasma to penetrate the passivation layer decreases.



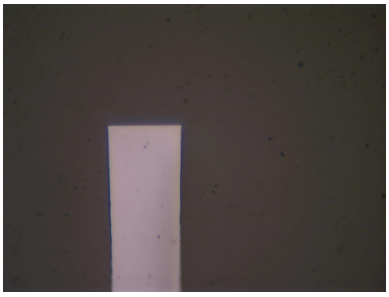
(a) Full Ridge



(b) Bottom of Ridge



(c) Center of Ridge



(d) Top of Ridge

Figure 4.6: Ridge formed with Sacrificial Island

4.3 Sacrificial Ridges

The addition of the sacrificial islands in the previous section works well for creating high aspect ratio sidewalls in wafers that will be etched completely through. If the wafer is not to be etched completely through, another method is needed. To resolve this problem, a new pattern was created to form a very thin ridge next to the sidewall that will be etched completely away when the correct depth is achieved. The pattern shown in Figure 4.7 contains two $6\mu m$ wide ridges positioned $40\mu m$ away from the sidewalls that are to be protected. Taking into account the 41.6:1 aspect ratio achieved by the test pattern, it is expected that the etching plasma will undermine the $6\mu m$ ridge at a depth of approximately $250\mu m$.

Figure 4.7: Unit Cell with Sacrificial ridges

The design of the width of the sacrificial ridges is very important. If the undercut is not enough, then the ridge will not break; if the undercut is too much the ridge will break too soon leaving a large peak that will not etch away. The figure below is a picture of an SOI wafer with the cell pattern etched into the $150\mu m$ device layer down to the oxide layer. At this point the sacrificial ridges are still intact because the amount of undercut was not enough to undermine the foundation of the ridges.

A $500\mu m$ wafer was also etched using this pattern. The ridges again broke at the designed $250\mu m$, but even though they were broken, they remained in place long enough to protect the silicon underneath as etching continued. After a few cycles, the ridge eventually disintegrated, but in its place was a large peak of unetched silicon. Once the oxide layer was exposed in other areas, an approximately $100\mu m$ peak remained. Further etching would

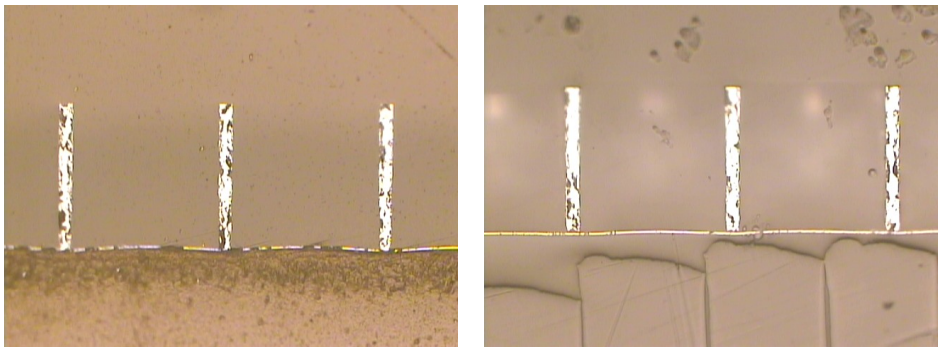
Figure 4.8: $6\mu m$ Sacrificial Ridges

remove this peak, but the $0.5\mu m$ oxide layer would not withstand the number of cycles required to complete the process.

The process was once again attempted on a $300\mu m$ device layer SOI wafer. The ridges again broke at around $250\mu m$ leaving a small peak which was etched away with only 20 extra cycles of etching. This was small enough for the oxide to remain intact after all of the silicon had been etched away.

Figures 4.9(a) and 4.9(b) show the cross sections of two patterns of $30\mu m$ ridges etched on the same $300\mu m$ device layer wafer. Pattern A contained no sacrificial ridges while pattern B contained the sacrificial ridges. The pattern without the ridges had an undercut of $5\mu m$ on each side over $300\mu m$ of etching, while the pattern with the ridges had an undercut of only $1\mu m$ on each side.

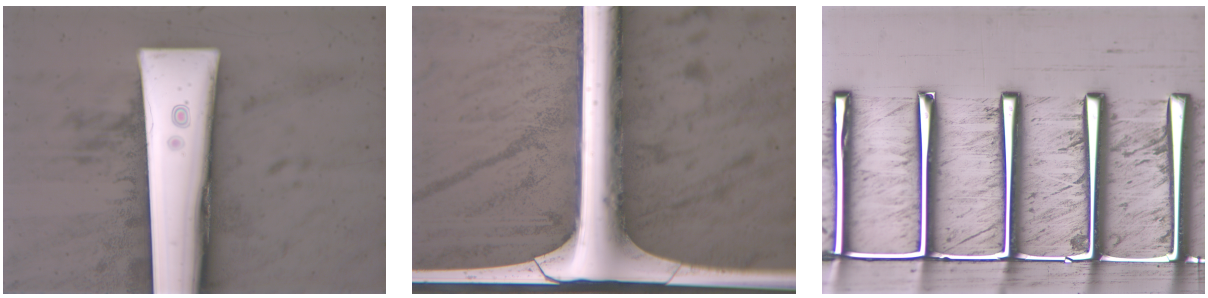
While not tested, it should be possible to extrapolate this process for thicker wafers. By making a thicker pattern for the sacrificial ridge, breakage will occur at a deeper level. Figure 4.10 shows a $500\mu m$ wafer etched to form $50\mu m$ wide ridges. The final width at the bottom of the ridge was $18\mu m$. The addition of sacrificial ridges designed for this pattern should be able to significantly improve the aspect ratio of the final $500\mu m$ tall structure.



(a) Pattern With No Sacrificial Ridges

(b) Pattern With Sacrificial Ridges

Figure 4.9: Sacrificial Ridge Comparison



(a) Top of Ridge

(b) Bottom of Ridge

(c) 10x View of Cross-section

Figure 4.10: $500\mu m$ etch with $400\mu m$ spacing

4.4 Bonding a Patterned Wafer

Once a window containing high aspect ridges has been etched into the double side polished silicon wafer, the ridges then must be bound to the device layer of the SOI wafer. This was accomplished using the hydrophilic fusion bonding method described in section 2.6.1. Bonding an SOI wafer to a wafer that has been etched through can be seen as both beneficial and problematic. Because the double side polished (DSP) wafer contains holes, the impact to the amount of bonded area caused by bubble formation between the wafers is limited. Conversely, in order to form a successful bond, all impurities introduced in processing such as PR residue must be completely removed. The options available for cleaning small feature size freestanding structure become greatly reduced. Listed below are the typical cleaning methods available in the AMSTC microlab.

- RCA Clean:

  The typical cleaning method, but some steps require heating to 70° and can become turbulent, possibly causing damage to the pattern.

- Ultrasonic Shaker:

  The AMSTC contains a Branson 5510 Ultrasonic shaker which will oscillate a liquid at 40Khz. Ultrasonic shaking can effectively remove particles from the wafer surface, but can not be used clean small MEMS patterns because the vibrating liquid can cause enough force to break the structures.

- Oxygen Plasma Etcher:

  The vacuum system used by this device can cause damage to small structures. During the plasma ashing, the wafer is supported by three pins pushing up on the wafer from beneath. An etched through wafer must therefore be supported by a backing wafer.

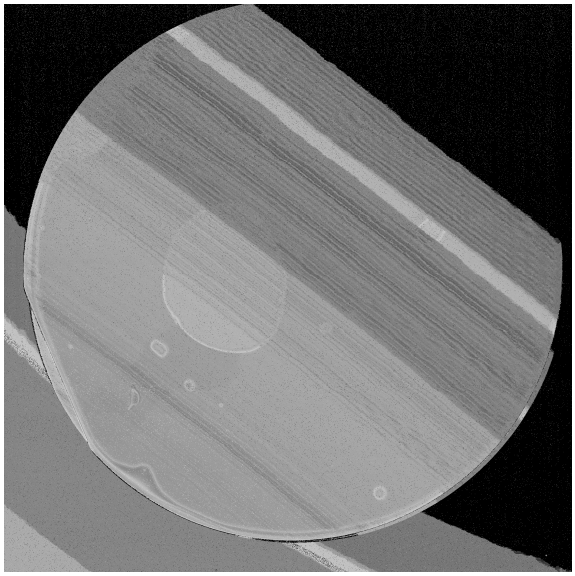
- Spin Rinse Dryer (SRD):

The Spin Rinse Dryer sprays water at approx 30psi which can cause extreme damage to freestanding structures.

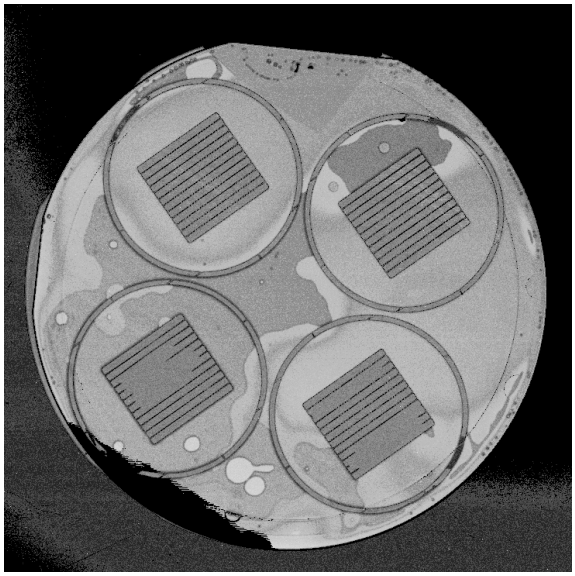
The figure below shows the progressive attempts made to achieve a successful bond between two wafers. While this was not the first overall attempt at bonding, it was the first that can be considered successful. The very first effort was to make the wafer hydrophobic using a 10:1 H_2O to HF dip before bonding. This resulted in a bond in only a small section of the wafer and was considered unsuccessful. The attempted shown in Figure 4.11(a) was performed with two clean wafers made hydrophilic with the B Clean. The wafers were placed in the Spin Rinse Dryer, and then prebonded at room temperature. The bond was then strengthened through annealing at 1050°C for 2 Hours. As shown, most of the wafer was successfully bonded except for a large bubble in the middle preventing the successful bond. It is possible that the size of this bubble could have been reduced through extra kneading of the wafers to work the bubble out prior to annealing. In the next attempt shown in Figure 4.11(b) a patterned and etched wafer was used. Bonding with an etched wafer has certain advantages as well as disadvantages to the previous unprocessed wafer. The spaces between the pattern can help the bonding process by allowing trapped air bubbles more routes for escape. On the other hand, the processing steps that the etched wafer is exposed to can introduce a number of contaminants and other defects that if not fully cleaned from the wafer surface will prevent a successful bond. Most of the normal cleaning methods are unavailable due to the fragile nature of the structures that have been created, therefore, Oxidizing the wafer surface before the processing steps proved helpful in keeping the underlying silicon surface free of particles. The Oxide layer was removed in a 10:1 H_2O to HF dip, and the surface made hydrophobic using the B clean. The largest particles on the wafer were picked from the surface, using a scalpel, but defects at the edge of patterns caused a number of small particles to form over portions of the wafer. This attempt resulted in about a 50% bond over the surface, which is not acceptable.

An improvement to the process was found during the next attempt, shown in Figure 4.11(c), by placing the etched wafer in the Spin Rinse Dryer prior to bonding. It was thought that the force of the water would damage the ridges, but because the trenches extend all the way through the wafer, most of the water passed harmlessly though the wafer, while the relatively thick $50\mu m$ width was strong enough to withstand the amount of water that does make contact. It should be noted, however, that a small percentage of ridges do break under the pressure, making this a source of reduced yield. The benefit of the successful bond outweighs the drawback of the reduced yield, therefore, the Spin Rinse Drier has been included as a part of the final process shown in Appendix B. Most of the wafer was bonded in this attempted and was considered a successful bond for the purposes of this project.

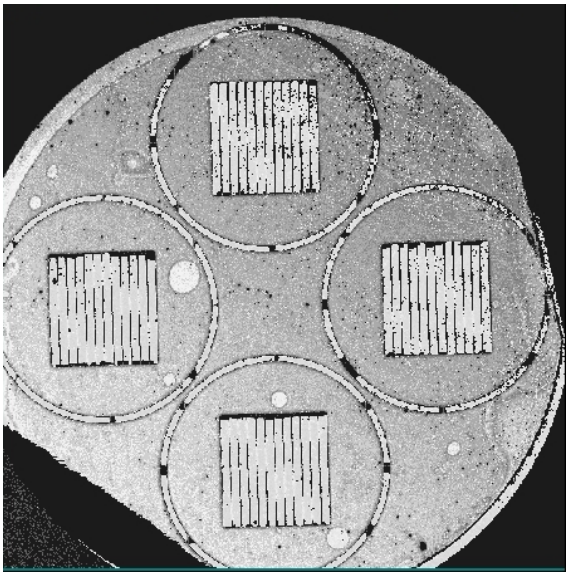
A final experiment was performed to enhance the bonding process, to clean the wafers in the Spin Rinse Dryer, pick the particles off with a scalpel, and the clean the wafers again in the Spin Rinse dryer. This resulted in no improvement over the previous attempt, and it is possible that during the time spent picking particles, the wafer was being exposed to more particles than were being removed. This attempt is displayed in Figure 4.11(d).



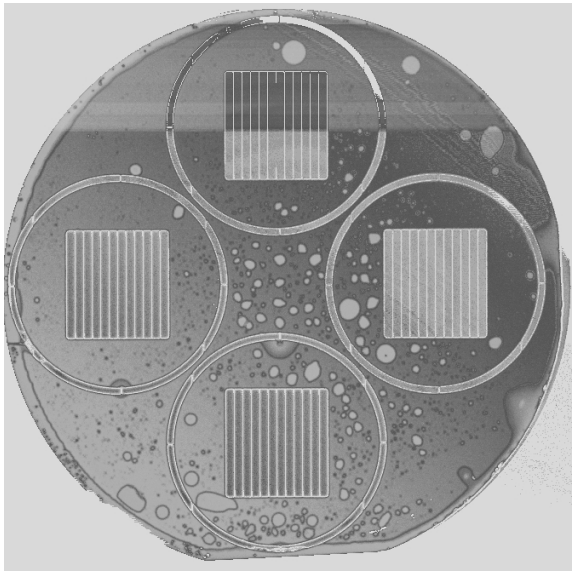
(a) 1st Attempt, No Pattern



(b) 2nd Attempt, Patterned wafer



(c) 3rd Attempt, Patterned wafer



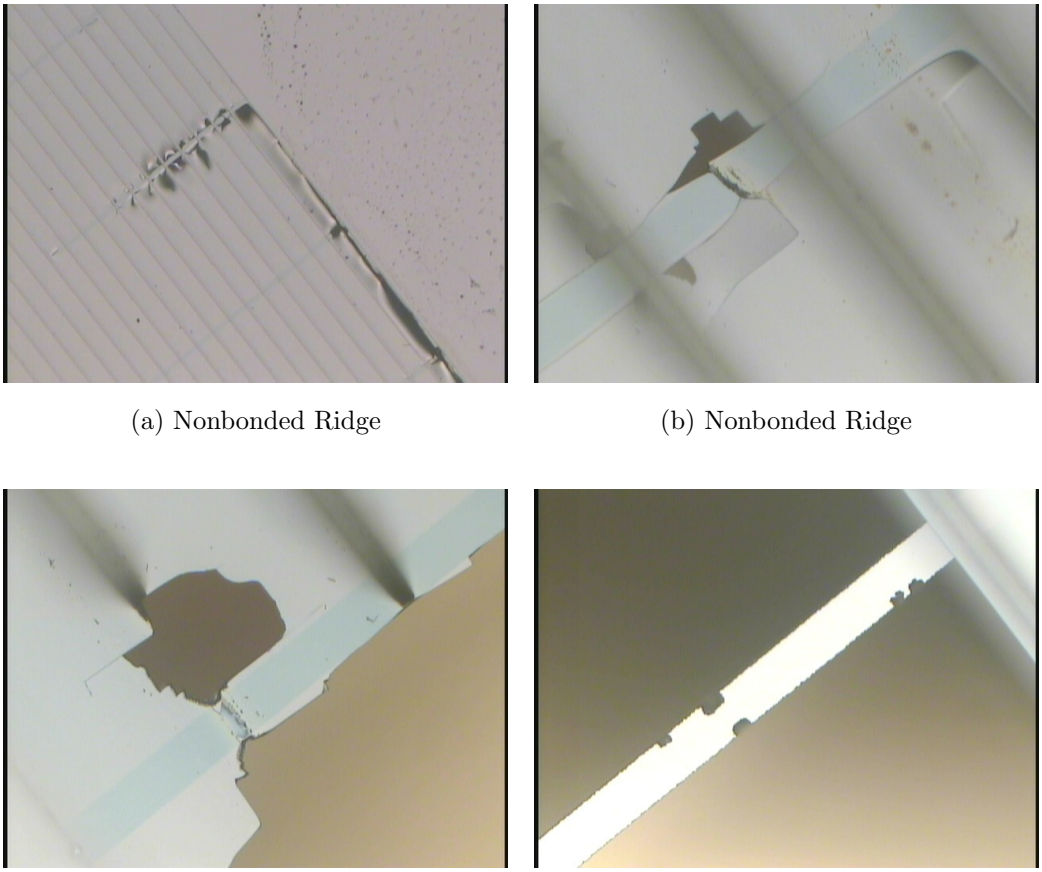
(d) 4th Attempt, Patterned wafer

Figure 4.11: Wafer Bond Attempts

4.5 Failure Analysis

After achieving successful wafer bonding, and creating ridge structures with sufficiently high aspect ratio, all of the major processes are then in place to create the structure on an SOI wafer. The first successful attempt at fabrication proved that a large area $2\mu m$ crystalline membrane can be fabricated, but the device was very delicate and broke easily under vacuum testing as detailed in section 5.2. By analyzing the break pattern, a stronger design can be realized. As can be seen in the figure 4.12(a), one ridge of this device was only partially bonded, allowing the membrane to deflect enough to cause the membrane to tear. The tear continued down the length of the bonded portion of the ridge until it hit the edge of the window. In other locations as in figure 4.12(c), it is apparent that the ridges are very well bonded to the membrane, but once part of the membrane failed, some of the small ridges did not have the strength to remain in place, thus pulling the membrane up in other locations. Also it can be seen that when the membrane broke, the fracture resulted in a square pattern breaking along the $\langle 100 \rangle$ lattice plane. Figure 4.12(d) shows another section of the non-bonded ridge where the membrane has been completely removed from the ridge.

The results here show that while the design may allow fabrication of a thin membrane, the design is not strong enough to withstand outside influence. If there is a ridge that is not fully bonded, or if there is a weakened area of the membrane, the current design exposes a large area of the window to failure. Taking this into account, a new design was proposed to place both sets of ridges on the same side. By doing this, the stress caused by a non-bonded ridge, or a weakened membrane, will be confined to a single cell instead of an entire row across the window.



(a) Nonbonded Ridge

(b) Nonbonded Ridge

(c) Breaking Point

(d) Breaking Point

Figure 4.12: Membrane Failure Pattern

4.6 Black Silicon

An issue observed with the use of the MORGNSOI recipe during the etching of silicon was the formation of phenomenon known as black silicon. [12] The black silicon effect is the formation of very thin columns of silicon on the surface of the trench due to incomplete removal of the masking layer during the Bosch process. As these columns grow longer than the wavelength of light, they can alter the angle of light reflection causing the surrounding surface to appear black. There are a number of causes for this effect during the DRIE process. Black silicon can occur immediately if the wafer has not been appropriately cleaned. Native oxidation of the silicon surface during etching can also act as a masking agent, causing the formation of these columns. Redeposition of masking material that has been etched is also a cause of formation. Typically, the formation of black silicon is seen as a positive result, because the ratio of the etching gasses SF_6/O_2 at which black silicon formation occurs is also the optimal ratio for anisotropic trench etching. [12] During the MORGNSOI process, black silicon begins to appear on the outer edge of the wafer at about $200\mu m$ trench depth, and spreads across the wafer as the trench becomes deeper. When etching very deep ridges of $500\mu m$ and more, instances have occurred whereby the black silicon does not etch away when the oxide layer of the SOI wafer is reached. Because of this, the black silicon only remains visible leaving no evidence that the SiO_2 is being etched. When this happens, the SiO_2 layer can be etched completely through without complete removal of the black silicon, thus destroying the membrane below.

Black silicon formation to the extent that the entire wafer is covered has only occurred twice and can be attributed to an unclean reaction chamber. A chamber conditioning process can be run to return the chamber to an optimal etching state. If large amounts of black silicon do form, the SF_6/O_2 ratio can be increased. This will cause a more isotropic etch and undercut the black silicon columns returning to a smooth trench surface. This increased ratio, however, also increases the amount of undercut beneath the pattern; therefore it is

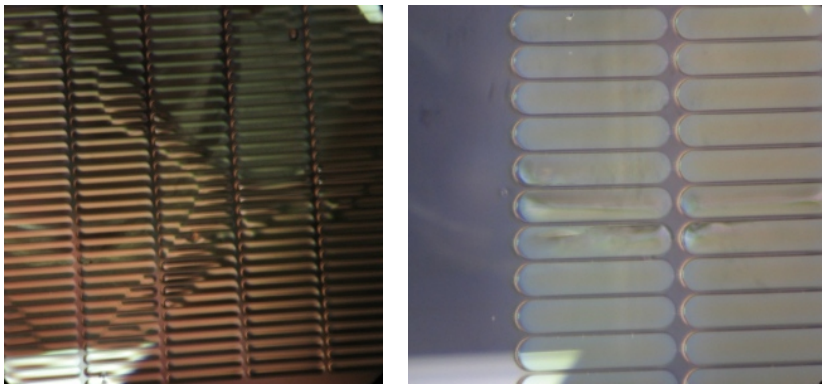
recommended that the program be returned to the normal ratio once the black silicon has been removed.

4.7 Backing Wafer Application

An important aspect of the manufacturing process that was not considered was the importance of the backing material used to secure the SOI wafer during etching. When etching large patterns through a wafer, the wafer must be secured to a backing wafer to have structural support so that the force from the stage does not break the wafer. Moreover, when etching down to a thin membrane less than $5\mu m$ thick, the material that secures the SOI wafer to the backing wafer becomes important. The material must be thermally conductive to dissipate heat from the etching process. The material must also be uniform in thickness across the wafer.

During etching, the wafer is held at a very low pressure and the membrane remains firmly secured to the backing wafer. Once the etching is complete, the membrane becomes very thin and pliable. When the pressure is then increased to remove the wafer, air fills the uniform areas of the PR causing deformation of the membrane. Figure 4.13(a) shows the deformation that has occurred in an etched SOI wafer still attached to its backing wafer as a result of nonuniform spreading of the PR adhesion layer. Figure 4.13(b) is a closeup view of an area where this deformation has caused a tear in the membrane.

A number of methods were investigated to mitigate this problem. First a different material was used called WaferGrip$_{tm}$. This material is similar to paper at room temperature, and melts at 105°C. When placed on a wafer and melted, the material creates a uniform adhesion layer that can create a strong bond between two interfaces after cooling. The substance can then be reheated and removed by sliding the two interfaces apart. The sliding action, however, made WaferGrip$_{tm}$ unsuitable for this project because the force required to separate the wafers caused stress on the membrane and broke it in some locations. For this reason the use of PR was revisited.



(a) Vacuum Stressed Membrane

(b) Broken Membrane

Figure 4.13: Backing Wafer Adhesion Issues

Multiple experiments were performed to obtain the best possible PR layer to form a uniform, thermally conductive temporary bond that would hold through the etching process. The variables tested are listed as follows.

- PR Type
- PR Thickness
- Bake Method and time
- Bonding Method

A silicon wafer was bonded to a pyrex wafer using AZ5214 photoresist in order to determine the uniformity of the PR across the wafer. The PR was spun onto the wafer at 1500rpms and the pyrex wafer attached. The PR showed fair coverage when first attached with small bubbles at various points on the wafer, but when placed on the hot plate the bubbles migrated toward the center of the wafer forming one large circle in which the wafers did not make contact. The bonded wafers were then brought to a vacuum of 80mTorr. As the vacuum increased, the bubble in the center of the wafer began pushing against the surrounding photoresist toward the outside of the wafer. when a pressure of about 120mTorr

was reached, the two wafers completely separated from each other long enough for the air bubble to escape the wafer, and then snap back shut. When the air bubble was no longer present, the PR, initially spread across the wafer, merged into the capillary pattern displayed in figure 4.13(a) which placed stress on the membrane.

It was thought that if a thicker PR was used then the PR would not move as much across the wafer. Different thicknesses of AZ4620 were tested using spin speeds on the range from 1000rpms to 5000rpms. Two issues arose from these tests. First, it was found that AZ4620 does not perform well as a thermally conductive interface. Second, with very thick layers, The wafers can separate during the DRIE process causing the pattern mask on the surface to burn away quickly.

AZ5214 was then tested at a spin speed of 3000rpms. This provided a very thin layer of PR for bonding. Again, the wafer separated during etching, because there was not enough coverage across the interface to keep it secure. AZ5214 was applied again at a speed of 1000rmps with better results, the wafer completed the etching process without any heat transfer issues, but the capillaries across the membrane remained.

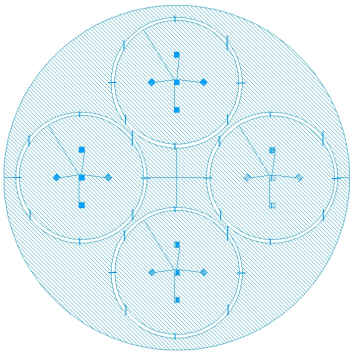
Different Heating times were tested ranging from 1 minute to 10 minutes at 105°C. A bake that is too short would not sufficiently bond the wafer, and a bake that is too long would cause the PR to become brittle again allowing it to separate during DRIE. 5 minutes was finally settled on as an appropriate bake time.

Finally, the bonding method was also found to have an effect on the strength of the bond. Air bubbles can be pushed out somewhat by bonding one side of the wafer first and then pressing across the rest of the wafer. Also, while not tested, it is believed that turning the two wafers slightly after they have been brought together will help spread the photoresist over the wafer and help hold the photoresist in place during the hotplate bake.

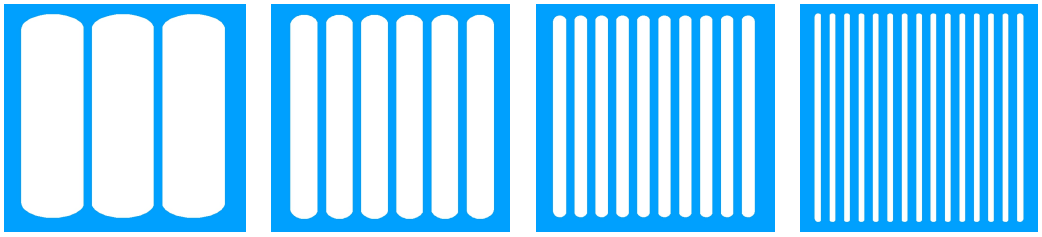
Backing wafer bonding is an issue that has still not been fully resolved, but at this time, the use of AZ5214 at a spin speed of 1000rpms with a soft bake at 105°C for 5 minutes has achieved satisfactory results.

4.8 Test Pattern

A new testing pattern was created to find a suitable ridge spacing that can hold up to an outside influence. The test patterns are approximately one-tenth the size of the original full window mask, and consist of a grid pattern with primary and secondary ridges on the same side. Each pattern then had a ridge spacing ranging between $50\mu m$ and $400\mu m$. The sides of the windows were also curved so that less stress would be placed along the crystalline plane. These test pieces did not include the ridges fusion-bonded to the device layer of the SOI wafer. Although the bonded ridges provide extra support, they also greatly increased the number of fabrication steps and potential for defects to be introduced into the membrane. If this cross pattern can hold up to testing, then the bonding may not be needed or could be added in the future to provide extra support.



(a) Test Pattern Wafer



(b) 400μm spacing window

(c) 200μm spacing window

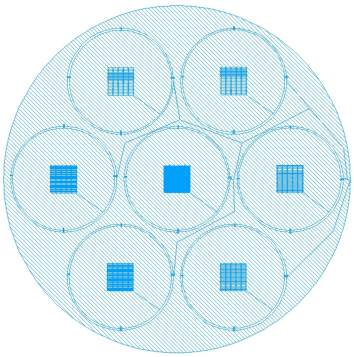
(d) 100μm spacing window

(e) 50μm spacing window

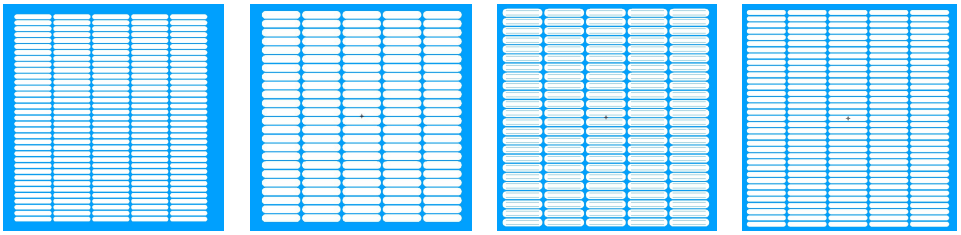
Figure 4.14: Test Pattern

4.9 Quarter Size Mask

All of the samples held up to vacuum well, so the patterns were scaled up to one quarter of the final size. This pattern is shown in figure 4.15. To test the larger membrane area, four patterns were designed. All the patterns had $50\mu m$ primary ridge widths, and $30\mu m$ secondary ridge width. The patterns were designed for wafers of thickness of $300\mu m$ or less. The spacings between the ridges were 200, 300, and $400\mu m$, with one pattern including sacrificial ridges.



(a) Quarter Window Wafer



(b) 400μm spacing cells

(c) 300μm spacing cells

(d) 300μm spacing cells with sacrificial ridges

(e) 200μm spacing cells

Figure 4.15: Quarter Window Pattern

4.10 Oxide Removal

In the original design for this device, the membrane was supported only by silicon ridges. To achieve this, complete removal of the Box layer beneath the ridges was required, so that that stiction would cause the ridges to attach to the device layer by Van Der Walls forces. The device was dipped in a solution of 49% hydrofluoric acid for 10 minutes. The chip could then be fusion bonded to the membrane using the high temperature furnace. Unfortunately, the capillary action between the sidewall of the ridges was stronger than the force between the membrane and the ridge. This action caused the ridges to become stuck to each other rather than to the membrane.

A few ways for removing the oxide layer without causing stiction were considered. The device was too large to fit in the critical point dryer in the AMSTC, so evaporation drying was tested using ethanol and isopropyl alcohol. These liquids are known to have low surface tensions with air, and thus a higher chance of successful oxide release. Unfortunately, these methods proved unsuccessful. Sublimation drying was also attempted with some successful results using tert-butanol alcohol, but it was finally determined that the oxide layer beneath the ridges would be sufficient to secure the structure.

The device was submerged in Buffered Oxide Etch, which has an etch rate of between $800 - 900\mathring{A}/min$, for 5-6 minutes until the oxide was removed from the surface of the membrane, but remained underneath the ridges. It has also been reported that agitation in the BOE provides a more anisotropic etch, but considering the fragility of the membrane, this was not attempted.

4.11 Metal Deposition

Once the structure has been produced, a solderable metal layer needed to be deposited on the outer ring of the device in order to ground it for future testing.

During this process, only the outer edge of the ring must be allowed to be deposited with metal. Therefore, a masking material must be placed in the path of the evaporated material covering the window. Similar to the DRIE chamber, the chamber in which the electron beam evaporation operates must be pumped down to high vacuum. It is therefore important that no air be allowed to become trapped on either side of the membrane during the pumping process. To prevent this, a mounting structure was created to suspend the window portion of the device approximately $1500\mu m$ above a mounting platform, with a masking layer suspended approximately $1500\mu m$ above the window.

Once mounted inside of the chamber, layers of chrome, nickel, and gold respectively are deposited over the exposed areas of the device. The full evaporation program is detailed in apppendix D.1. Chrome is used for its good adhesion to silicon. Nickel acts as a barrier between the chrome and gold, and also becomes the primary interface with the solder. The gold increases the wettability of the solder allowing the solder to attach to the contact as well as prevents the nickel layer from oxidizing.

Chapter 5

Device Strength Testing and Performance

After the fabrication of each design, initial pressure testing was performed by the University of Missouri, to determine how reliably the device could withstand a pressure difference from one side of the membrane to the other. A system was built that would slowly decrease the pressure on one side of the membrane until a near vacuum was reached, while the opposite side of the membrane would remain at atmospheric pressure. All data in the following sections of this chapter have been provided by Peter Norgard of The University of Missouri.

5.1 Pressure Testing Equipment

Figure 5.1 is a picture of the vacuum equipment used in pressure testing the Devices. Figure 5.2 is a schematic detailing each piece of equipment. A Welch 1402 pump passes through an oil-vapor filter to pre-evacuate the the chamber and a cryopump. A CTI Cryotorr8 pump with an 8" standard flange is used to achieve high vacuum. Pneumatically actuated values control the roughing process on both the cryopump and the chamber.

A TC536 thermocouple pressure probe is used to measure pressures from 1000 torr to 1 torr. A D902 capacitive pressure probe measures pressure from 2 torr to 10 mTorr. An IG563 ion gage pressure probe measures the pressure from 10mTorr to less than 1 μm Torr. A residual gas analyzer is used to measure gas escaping from the chamber.

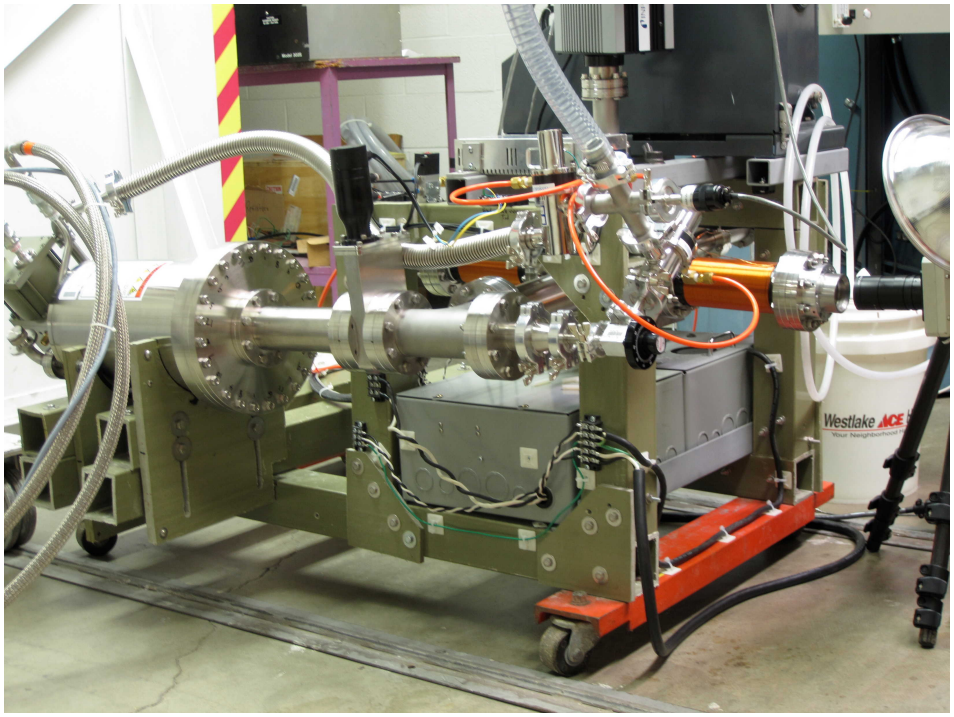


Figure 5.1: Vacuum System Setup

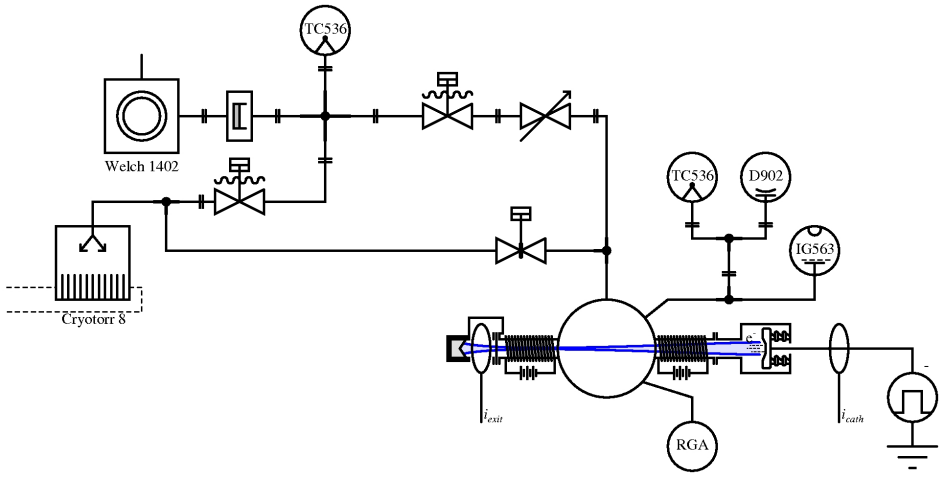


Figure 5.2: Vacuum System Schematic

5.2 Pressure Testing Results

As shown in the results from Table 5.2 the first set of windows fabricated using the original mask with one set of ridges on each side of the membrane did not withstand the pressure testing. A section of the membrane broke at just below atmospheric pressure on

each window fabricated. During this test, the ramp down speed of the pressure was very high, which could have contributed to the early rupture, but also as detailed previously in the Failure Analysis section 4.5, this design was thought to be highly susceptible to defects in processing.

Window	Pumpdown Rate	Break Pressure
1	100 Torr/s	766 Torr
2	100 Torr/s	728 Torr
3	50 Torr/s	728 Tor

Table 5.1: Pressure Test Data on Original Design

Using the information collected from this first test, the photolithography mask was redesigned as detailed in sections 4.8 through 4.9. The silicon wafer specifications were also varied in order to realize a thicker membrane. The thickness of the handle layer of the SOI wafer was also varied. A thinner handle layer was found to provide a more uniform bond by making the wafer more compliant to the opposing surface. Also because the silicon etching process is not uniform over the wafer surface, a thinner handle layer allowed for a decrease in etching time making the nonuniformity less significant. The varied SOI wafer parameters are shown in figure 5.2.

Device Layer Thickness	Oxide Thickness	Handle Thickness	Doping
$3\mu m$	$.5\mu m$	$300\mu m$	Boron
$3\mu m$	$.5\mu m$	$300\mu m$	Phosphorous
$2\mu m$	$.5\mu m$	$150\mu m$	Boron

Table 5.2: Silicon Wafers Used in Quarter Window Test

All of the windows fabricated during the second round of testing were made using the quarter scale mask. This set of devices all had both sets of ridges on one side of the wafer, with one direction having $50\mu m$ wide ridges and the other direction having $30\mu m$ wide ridges. two methods of wafer mounting were tested including Wafer Grip adhesion, and PR adhesion. Various Spacings between the ridges were tested, as well as device thicknesses of 2 and 3 μm. Specific material parameters for each tests are shown in table E.1 of Appendix E. As can be

seen from tables E.2, E.3, E.4, and E.5, while there were still breakages that occurred due to defects in the membrane, devices fabricated with a thicker membrane achieved a lower average final pressure when compared to the $2\mu m$ membranes.

Chapter 6

Conclusion

In this project a large area thin silicon membrane was created and bonded on both sides to very high aspect ratio silicon ridges which provide structural support to the membrane. In order to realize this multi-layer three dimensional structure, multiple new processes had to be developed and combined with existing mature processes. The devices created were were able to withstand preliminary vacuum pressure testing performed at the University of Missouri with further testing to be performed on the redesigned devices.

New methods for creating high aspect ridges were developed by using photolithography to create mask patterns. These mask patterns were then used to create structures designed to protect the sidewalls of the trenches from lateral etching due to off-angle bombardment of energetic SF_6 ions. A technique for bonding silicon was studied and successfully implemented to secure the ridges to the membrane. Complete processes designed to increase the strength of the supporting structure were developed. A process developed to create a structure that protects the membrane through supporting ridges on both sides is detailed in Appendix B. Another process using a design that created structures that protect on only one side of the membrane is detailed in Appendix A.

Chapter 7

Future Work

Further work is needed to increase the strength of the supporting ridges while reducing the coverage area. There are many more designs that may have better results in stabilizing the membrane. The resultant design for this project was conservative because fabrication issues had the effect of lowering yield. The process has matured to the point that thinner membranes may be possible that were not feasible in previous tests. Also, the width of the ridges may also be shrunk. During the preceding trials, a ratio of $10\mu m$ ridge height to $1\mu m$ ridge width was adhered to. A pattern containing a $30\mu m$ ridge width was the thinnest ridge width attempted using a $300\mu m$ wafer thickness. With the successful test of the sacrificial ridges' ability to protect the ridge sidewalls thus increasing the width at the bottom of the trench above the SIO_2 layer, it may be possible to reduce the target ridge width below the $10\mu m$ ratio previously designed.

As stated previously in section 2.5.4, an alternating sequence of etching and passivating cycles during the DRIE process can greatly increase the aspect ratio of a silicon trench. Also, as discussed in section 3.3.1, there are a number of variables in these cycles that can be altered to affect the aspect ratio. During this project, the MORGNSOI program was not altered, but tuning of these variables can be performed which can alter the amount of undercut produced during the etch. Any change in this program, however, will also have an effect on the efficiency of the of the sacrificial ridges. As one example, the Ratio of SF_6 to O_2 can be reduced to create a more positive aspect ratio. This change in combination with the use of the sacrificial ridges designed for the previous recipe, will cause the ridges to break at a much lower level, leaving un-etched silicon remaining after the SIO_2 layer has been reached.

Furthermore, the present single side protected design did not include wafer bonding. While the addition of the bonding step adds the potential for reduced yield, it also has a number of potential benefits including extra support for the membrane as well as an added ability to dissipate heat from the device, should that need arise. Improvements can be made in the uniformity of the silicon bond by researching better methods of wafer cleaning before bonding. One method proposed by H Takagi et al. involves cleaning a surface with an Argon ion beam in vacuum, followed by bonding the wafers together in the vacuum. [24]

Improvements in backing wafer application in preparation for the DRIE process should also be studied. Brewer Science Inc. has introduced a new temporary bonding material that may provide more protection to the membrane during device processing than the previously used PR adhesion method. Brewer Sciences also claims to have created a method for removing this adhesive with much less stress than previous methods. The use of this material and process could help to reduce membrane thickness without sacrificing yield.

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Appendices

Appendix A

Single side Process Traveler

I. RCA Clean

1. A Clean
   (a) Acetone Bath 1 minute
   (b) DI water Rinse 1 minute
   (c) IPA bath 1 minute
   (d) Di water Rinse 1 Minute
2. B Clean
   (a) 5-1-1 mixture $5 : DI\ H_2O\ 1 : 30\%\ H_2O_2\ 1 : 29\%\ NH_4OH$ heated to 70° for 5 Minutes
   (b) DI water Rinse 1 Minute
3. C Clean
   (a) HF bath for 30 Seconds
   (b) DI water Rinse 1 Minute
   (c) Second DI water Rinse for 1 Minute

II. Spin Rinse Dryer

III. Dehydration Bake

IV. Backing wafer Application

1. Spin photoresist

(a) Photoresist:AZ5214

(b) Speed:1000RPM

(c) Ramp Speed: 300 R/sec

(d) Time: 9sec

(e) Expected Thickness: $3\mu m$

2. Attach SOI wafer to backing wafer device layer side down

3. Soft Bake

(a) Temp:$100°C$

(b) Time:3 Minutes

V. Photolithography

1. Deposit HMDS Vapor

(a) Temperature: Room Temperature

(b) Time: 5 Minutes

2. Spin Photoresist

(a) Photoresist:AZ4620

(b) Speed:2100RPM

(c) Ramp Speed: 450 R/sec

(d) Time: 45sec

(e) Expected Thickness: $8\mu m$

3. Soft Bake

(a) Temp: $100°C$

(b) Time:4 Minutes (Longer Bake Time to prevent Bubble Formation)

4. UV Exposure

(a) Channel 2 (275 Watts)

(b) Exposure Type: Hard

(c) Cycles: 6

(d) Exposure Time: 8 seconds with 20 seconds wait time

5. Pattern Developement

(a) Developer: AZ400

(b) Mixture: 3 parts DI Water to 1 Part Developer

(c) Time: 2 Mintutes with agitation

VI. Inspect Pattern In 5 places to ensure complete development.

VII. Descum

1. Power: 300W

2. Time: 15 Seconds

VIII. DRIE

(a) Program:MORGNSOI

IX. Backing Wafer and Photoresist Removal

(a) Acetone Bath

(b) Isoproponal Bath

(c) DI Water Bath

(d) Weak Piranha Clean

i. 4 parts H_2SO_4 1 part H_2O_2

ii. Let solution stand for 5 minutes to cool to $70°C$

iii. time: 5 minutes

iv. 1 minute DI Water Bath

v. Isoproponal Bath

(e) Separate individual devices from wafer

(f) BOE Bath

i. Isoproponal bath to remove Surface tension

ii. DI Water Bath

iii. Etch Rate: Approximately 1000Å/min

iv. Time: 5 Mintues Until Oxide is no longer Visible

v. DI Water Bath 1 Minute

vi. Isoproponal Bath 1 Minute

vii. Allow to Air Dry

(g) Stress Anneal of membrane in Oxidation Furnace

i. Insert Devices into Furnace at $400°C$

ii. Program: ColinStressAnneal

A. Flow Rate: 5 SLM N_2 for entire program

B. Initial Temp: $400°C$

C. Ramp: $5°C$/minute

D. Temp: $1000°C$

E. Time at Temp:1 Hour

F. Ramp: 5C/minute

G. Final Temp: $400°C$

iii. Remove Devices from Furnace

(h) Metallization

i. Mount Circle 1mm m above Supporting wafer

ii. Argon Ion Abasement: 5 Minutes

iii. Metal Composition: 400ÅCR, 1000ÅNi, 500ÅAu

Appendix B

Dual Side Process Traveler

I. RCA Clean

1. A Clean

   (a) Acetone Bath 1 minute

   (b) DI water Rinse 1 minute

   (c) IPA bath 1 minute

   (d) Di water Rinse 1 Minute

2. B Clean

   (a) 5-1-1 mixture $5 : DI\ H_2O\ 1 : 30\%\ H_2O_2\ 1 : 29\%\ NH_4OH$ heated to $70°C$ for 5 Minutes

   (b) DI water Rinse 1 Minute

3. C Clean

   (a) HF bath for 30 Seconds

   (b) DI water Rinse 1 Minute

   (c) Second DI water Rinse for 1 Minute

II. Spin Rinse Dryer

III. Dehydration Bake

IV. Oxidation

1. Insert Wafer and run Program: Oxidation (details in Appendix C.1)

2. remove Wafer

V. Primary Ridge Photolithography

1. HMDS Vapor
   (a) Temperature: Room Temperature
   (b) Time: 5 Minutes
2. Spin photoresist
   (a) Photoresist:AZ4620
   (b) Speed:1600RPM
   (c) Ramp Speed: 450 R/sec
   (d) Time: 45sec
   (e) Expected Thickness: $11\mu m$
3. Soft Bake
   (a) Temp: $105°C$
   (b) Time:4 Minutes
4. UV Exposure
   (a) Channel 2 (275 Watts)
   (b) Exposure Type: Hard
   (c) Cycles: 6
   (d) Exposure Time: 10 seconds with 20 seconds wait time
5. Pattern Developement
   (a) Developer: AZ400
   (b) Mixture: 3 parts DI Water to 1 Part Developer
   (c) Time: 3 Mintutes with agitation

VI. Inspect Pattern In 5 places to ensure complete development.

VII. Descum

1. Power: 300W
2. Time: 15 Seconds

VIII. BOE Etch 3 Minutes (Until Oxide Removed from pattern)

IX. Backing wafer Application

1. Spin photoresist
   (a) Photoresist:AZ5214
   (b) Speed:1000RPM
   (c) Ramp Speed: 300 R/sec
   (d) Time: 9sec
   (e) Expected Thickness: $3\mu m$
2. Attach silicon wafer to backing wafer
3. Soft Bake
   (a) Temp: $105°C$
   (b) Time:3 Minutes

X. DRIE

1. Program:MORGNSOI (Program Details in Appendix 3.1
2. Etch for 150 cycles
3. remove wafer and rotate $90°C$
4. Etch for 150 cycles
5. remove wafer and rotate $90°C$

6. Etch for 150 cycles
7. remove wafer and rotate $90°C$
8. Repeat steps of 50 cycles until Silicon has been removed from patterned area

XI. Backing Wafer and Photoresist Removal

1. Soak in Acetone for a minimum of 24 hours.
2. Isoproponal Bath
3. DI Water Bath
4. Phirana Clean
   (a) Mixture: 4:H_2SO_4
   (b) Temperature: $70°C$
   (c) Time: 10 Minutes
5. RCA B Clean
   (a) 5-1-1 mixture 5 : $DI\ H_2O$ 1 : 30% H_2O_2 1 : 29% NH_4OH heated to 70° for 5 Minutes
   (b) DI water Rinse 1 Minute

XII. Silicon Fusion Bonding wafer Preparation

XIII. HF Bath

1. Mixture: 10: H_2O - 1: 49% HF in Nagalene Container
2. Time: 10 Minutes

XIV. RCA B clean for both Ridge wafer and SOI wafer

1. 5-1-1 mixture 5 : $DI\ H_2O$ 1 : 30% H_2O_2 1 : 29% NH_4OH heated to 70° for 5 Minutes

2. DI water Rinse 1 Minute

XV. Spin Rinse Dryer

1. Rinse: 200 Seconds
2. Dry: 120 Seconds

XVI. inspect wafer and pick off visible particles with scalpel under Low Magnification Microscope

XVII. Prebond Wafer

XVIII. Bond Wafer in Oxidation Furnace

1. Program: ColinBond see Appendix C.2 for Program details
2. insert Prebonded wafers when Temperature has reached $800°C$

XIX. inspect Wafer using C-SAM

XX. Phirana Clean

1. Mixture: 4:H_2SO_4
2. Temperature: $70°C$
3. Time: 10 Minutes

XXI. Dehydration Bake

1. Temperature: $120°C$
2. Time: 2 Hours

XXII. Attach 3 Inch Wafer to protect Ridge pattern during Backside Patterning

1. Attach WaferGrip$_{tm}$ to center unpatterned section of wafer
2. heat on hotplate at 105°C

3. attach 3” wafer to cover Ridge pattern

XXIII. Secondary Ridge Photolithography

XXIV. Spin photoresist

1. Photoresist:AZ4620
2. Speed:3000RPM
3. Ramp Speed: 450 R/sec
4. Time: 45sec
5. Expected Thickness: $6.5\mu m$

XXV. Soft Bake

1. Temp: $105°C$
2. Time:2 Minutes

XXVI. UV Exposure

1. Channel 2 (275 Watts)
2. Exposure Type: Hard
3. Cycles: 4
4. Exposure Time: 10 seconds with 20 seconds wait time.

XXVII. Pattern Developement

1. Developer: AZ400
2. Mixture: 3 parts DI Water to 1 Part Developer
3. Time: 3 Mintutes with agitation

XXVIII. Inspect Pattern In 5 places to ensure complete development.

XXIX. Matrix Descum

1. Power: 300W
2. Time: 15 Seconds

XXX. Replace 3" protection wafer with 4" DRIE backing wafer

1. hot plate temperature: $105°C$
2. Slide 3" wafer carefully off Ridge Wafer
3. carefully swab off remaining wafergrip with Amyl Acetate without touching the Photoresist on backside of wafer.
4. Spin photoresist onto 4" Silicon backing wafer
   (a) Photoresist:AZ5214
   (b) Speed:1000RPM
   (c) Ramp Speed: 300 R/sec
   (d) Time: 9sec
   (e) Expected Thickness: $3\mu m$
5. Soft Bake Back 4" Silicon Backing Wafer in Soft Bake Oven
   (a) Soft Bake Oven Temp: $105°C$
   (b) Time: 3 Minutes

XXXI. DRIE Secondary Ridges

1. Program: MORGNSOI (Program Details listed in Appendix 3.1)
2. cycles: 50
3. Remove Wafer and Rotate $90°C$
4. cycles: 50
5. Remove Wafer and Rotate $90°C$

6. cycles: 50
7. Remove Wafer and Rotate 90°C
8. Etch 25 cycles at a time until all silicon is removed from pattern

XXXII. Backing Wafer and Photoresist Removal

1. Soak in Acetone for a minimum of 24 hours.
2. Isoproponal Bath
3. DI Water Bath
4. Phirana Clean
   (a) Mixture: 4:H_2SO_4
   (b) Temperature: 70°C
   (c) Time: 10 Minutes

XXXIII. Stress Anneal of membrane in Oxidation Furnace

1. Insert Devices into Furnace at 400°C
2. Program: ColinStressAnneal
   (a) Flow Rate: 5 SLM N_2 for entire program
   (b) Initial Temp: 400°C
   (c) Temp: 1000°C
   (d) Time at Temp:1 Hour
   (e) Ramp: 5°C/minute
   (f) Final Temp: 400°C
3. Remove Devices from Furnace

XXXIV. Metallization

1. Mount Circle 1mm m above Supporting wafer

2. Argon Ion Abasement: 5 Minutes

3. Metal Composition: 400ÅCR, 1000ÅNi, 500ÅAu

Appendix C

Oxidation Furnace Programs

C.1 Program: Oxidation

Table C.1: Program: Oxidation

Oxidation								
Step	Type	Initial Temp $^{\circ}C$	Ramp $^{\circ}C/Min$	Final Temp $^{\circ}C$	Hold Time $Minutes$	O_2 slm	H_2 slm	N_2 slm
Step1	Step	400	—	—	0	0	0	5
Step2	Ramp	400	1000	—	—	0	0	0
Step3	Static	—	—	1000	5	0	0	5
Step4	Static	—	—	1000	5	5	0	0
Step5	Static	—	—	1000	45	3	5.5	0
Step6	Static	—	—	1000	5	5	0	0
Step1	Step	400	—	—	0	0	0	5

C.2 Program: ColinBond

Table C.2: Program: ColinBond

ColinBond								
Step	Type	Initial Temp $^{\circ}C$	Ramp $^{\circ}C/Min$	Final Temp $^{\circ}C$	Hold Time $Minutes$	O_2 slm	H_2 slm	N_2 slm
Step1	Step	400	—	—	0	0	0	0
Step2	Ramp	400	1075	—	—	0	0	5
Step3	Static	—	—	1075	60	0	0	5
Step4	Step	400	—	—	0	0	0	5

C.3 Program: ColinStresAnneal

Table C.3: Program: ColinStressAnneal

ColinStressAnneal								
Step	Type	Initial Temp $^{\circ}C$	Rate $^{\circ}C/Min$	Final Temp $^{\circ}C$	Hold Time $Minutes$	O_2 slm	H_2 slm	N_2 slm
Step1	Step	400	—	—	0	0	0	5
Step2	Ramp	400	5	1000	—	0	0	5
Step3	Static	—	—	1000	60	0	0	5
Step4	Ramp	1000	5	400	0	0	0	5
Step5	tatic	—	—	400	1000	0	0	5

Appendix D

Electron Beam Metal Deposition

Table D.1: Electron Beam Metal Deposition Recipe

Ion Beam Parameters	
Pressure	1×10^{-6} Torr
Ion Beam Duration	3 minutes
Ion Beam Cathode Current	6.46 Amps
Ion Beam Discharge Voltage	2.78 Volts
Ion Beam Current	205 Amps
Ion Accelleration Current	4 Amps
Neu emmission Current	264

Electron Beam General Parameters	
Discharge Voltage	55.1
Accelleration Voltage	102
Filiment Current	5.12 Amps
Layer Index	3

Metal Deposition Parameters						
Metal Layer	Crucible	Emmission	Voltage	Deposition Rate	Power	Thickness
Chromium	5	.018	9.85	1.8 Å/sec	42%	400Å
Nickel	4	.0078	9.98	.5 Å/sec	55.6%	1000Å
Gold	2	.264	9.96	2 Å/sec	93.9%	500Å

Appendix E

Vacuum Testing Results

Redesigned Window Vacuum Test Materials							
Int. Ref.	**Device Thick.**	**Rib Height**	**Rib Spacing**	**Rib Width A/B**	**Window Scale**	**Material Type**	**Mount Method**
Q001	3	300	400	30/50	1/4	p	PR
Q002	3	300	300	30/50	1/4	p	PR
Q003	3	300	300	30/50	1/4	p	PR
Q004	3	300	200	30/50	1/4	p	PR
Q005	3	300	400	30/50	1/4	n	WG
Q006	3	300	300	30/50	1/4	n	WG
Q007	3	300	200	30/50	1/4	n	WG
Q008	3	300	200	30/50	1/4	n	WG
Q009	2	150	400	30/50	1/4	p	PR
Q010	2	150	400	30/50	1/4	p	PR
Q011	2	150	300	30/50	1/4	p	PR
Q012	2	150	200	30/50	1/4	p	PR
Q013	2	150	200	30/50	1/4	p	PR

Table E.1: Vacuum Test Material Legend

Quarter Window Test Results 300μm With PR Mounting			
Test	**Int. Ref.**	**Window Break?**	**Final Pressure (Torr)**
1	LWI Q001	No	505
2	LWI Q001	Yes	428
3	LWI Q002	Maybe	574
4	LWI Q002	Yes	506
5	LWI Q003	No	506
6	LWI Q003	No	388
7	LWI Q003	No	81.5
8	LWI Q003	No	30
9	LWI Q004	No	386
10	LWI Q004	No	96
11	LWI Q004	No	12

Table E.2: Quarter Window Test Results 300μm With PR Mounting

Quarter Window Test Results 300μm With WG Mounting			
Test	**Int. Ref.**	**Window Break?**	**Final Pressure (Torr)**
12	LWI Q005	Yes	682
13	LWI Q006	No	400
14	LWI Q006	No	90
15	LWI Q006	No	2
16	LWI Q007	No	406
17	LWI Q007	No	82
18	LWI Q007	Yes	12
19	LWI Q008	No	394
20	LWI Q008	No	78
21	LWI Q008	No	2

Table E.3: Quarter Window Test Results 300μm With WG Mounting

Quarter Window Test Results 150μm With PR Mounting			
Test	**Int. Ref.**	**Window Break?**	**Final Pressure (Torr)**
22	LWI Q009	Yes	596
23	LWI Q010	No	401
24	LWI Q010	Yes	288
25	LWI Q011	Yes	576
27	LWI Q012	No	404
28	LWI Q012	No	82
29	LWI Q012	No	4
30	LWI Q013	No	448
31	LWI Q013	Yes	396
32	LWI Q004	No	4

Table E.4: Quarter Window Test Results 150μm With PR Mounting

Quarter Window Test Results: Retest of Non-Broken Devices			
Test	**Int. Ref.**	**Window Break?**	**Final Pressure (Torr)**
32	LWI Q004	No	4
33	LWI Q004	No	10
34	LWI Q003	No	2
35	LWI Q003	No	6
36	LWI Q012	No	2
37	LWI Q012	No	6

Table E.5: Quarter Window Test Results: Retest of Non-Broken Devices

Appendix F

Listing of Lab Equipment by Room#/Laboratory

- **Room # 455-461 Microfabrication Laboratory**
  - STI Semitool 200 Spin Rinse Dryer
  - Tencor Alpha-Step 200 Profilometer
  - Imperial IV Ultra-Clean 100 Dehydration Oven
  - Blue M OTP-120 Dehydration Oven
  - Tousimis Samdry PVT-3D Critical Point Dryer
  - CHA-Industries Mark 50 E-beam/Sputter System
  - Thermco 4000 Horizontal Tube Oxidation Furnace
  - Prometrix SpectraMap FT750 and Prometrix SpectraMap SM200/e
  - Karl Suss MA6/BA6 Contact Mask Aligner
  - Nikon 203338 High Magnification Microscope
  - Olympus SZ-PT Zoom Stereo Microscope
  - Matrix System One Oxygen Plasma Etcher Style 303
  - CEE Spin Coater
  - Hot Plate
  - YES 450-PB8-2P-CP Vacuum Bake Oven
  - YES 5 Dry Vacuum Bake Oven
  - STS Multiplex ICP Advanced Silicon Etcher

  - Dicing Machine
  - UV Flood Exposure System
  - Branson 5510 Ultrasonic Shaker

- **Room# 466 MEMS Testing Lab Room#**
  - Micromanipulator Manual Probe Station
  - HP 4156A Precision Semiconductor Parameter Analyzer

- **Room# 103 Laboratory for Electronics Assembly and Packaging**
  - Sonix C mode Scanning Acoustic Microscope
  - Nikon Measurescope MM-11 with Quadra-Check 2000 Measurement System

- **Room# 464 Advanced Packaging Print and Fire Laboratory**
  - Buehler Automatic Grinder/Polisher
  - Buehler VibroMet Vibratory Polisher
  - Low Power Microscope
  - Digital Scale