3D DEVICE SIMULATION OF SEU-INDUCED CHARGE COLLECTION

IN 200 GHZ SIGE HBTS

Except where reference is made to the work of others, the work described in this thesis is my own or was done in collaboration with my advisory committee. This thesis does not include proprietary or classified information.

Hua Yang

Certificate of Approval:

Foster Dai Associate Professor Electrical and Computer Engineering	Guofu Niu, Chair Professor Electrical and Computer Engineering
Stuart Wentworth Associate Professor Electrical and Computer Engineering	Stephen L. McFarland Acting Dean Graduate School

3D Device Simulation of SEU-Induced Charge Collection in 200 GHz SiGe HBTs

Hua Yang

A Thesis

Submitted to

the Graduate Faculty of

Auburn University

in Partial Fulfillment of the

Requirements for the

Degree of

Master of Science

Auburn, Alabama
December 16, 2005

3D DEVICE SIMULATION OF SEU-INDUCED CHARGE COLLECTION

IN 200 GHZ SIGE HBTS

Hua Yang

_____

Signature of Author

_____

Date

VITA

Hua Yang, daughter of Wenlin Yang and Yin Hua, was born on October 30, 1980, in Wuxi, Jiangsu Province, P. R. China. She received her Bachelor's Degree from Fudan University, majoring in Electrical Engineering. In August 2003, she was accepted into the Electrical and Computer Engineering department of Auburn University, Auburn, Alabama, where she has pursued her Master's Degree.

Her research interests include 3D device simulation of radiation effects on SiGe HBTs, modeling and characterization of low-frequency noise in RF devices and device physics.

THESIS ABSTRACT

3D DEVICE SIMULATION OF SEU-INDUCED CHARGE COLLECTION IN 200 GHZ SIGE HBTS

Hua Yang

Master of Science, December 16, 2005
(Bachelor of Science, Fudan University, Shanghai, China, June 2003)

124 Typed Pages

Directed by Dr. Guofu Niu

This thesis presents three dimensional device simulations of SEU (single-event upset)-induced charge collection in 200 GHz SiGe HBTs. The device was constructed and simulated using Davinci.

The charge collected by each terminal of the device is a strong function of the location of the ion strike. The sensitive regions of charge collection for each terminal are identified based on analysis of the device structure, the ion strike positions and the simulation results. For a strike between the deep trench edges, most of the electron and holes are collected by collector and substrate terminals, respectively. For a strike between the shallow trench edges surrounding the active emitter area, base terminal collects appreciable charges. The emitter terminal always collects negligible charges.

A new junction passing / deep trench (DT) confinement model for angle strike dependence is supported by the simulations. Angled strike does NOT mean increased effective linear energy transfer (LET). Angled strike in DT isolated HBT in general

produces less charge collection. DT isolation ring limits the reach of charge collection available to the collector/substrate (C/S) junction. An ion that does not pass either collector-base or collector-substrate junctions produces little charge collection for lightly doped substrate.

Then we propose new back junction approach to reduce charge collection in SiGe HBTs, and demonstrate its effectiveness in a 200 GHz SiGe HBT technology using 3-D device simulation. A wider n+ sinker around the deep trench perimeter helps by enhancing back junction charge collection, hence reducing charge collection at the sensitive collector node. A thinner p-type "substrate" layer also effectively decreases collector charge collection.

ACKNOWLEDGMENTS

I am very much grateful to Dr. Guofu Niu for his technical, educational support during my master's study; without him, this work could never possibly be done. I always admire his diligence and talents; he sets a perfect example of a person devoted to scientific research, which inspired me and pulled me through the toughest moments. I would also thank Dr. Foster Dai and Dr. Stuart Wentworth for serving on my committee.

I would like to thank Ramkumar Krithivasan for layout generation, Yun Shi for device simulation; Kejun Xia for expert explanations on device physics; Muthubalan Varadharajaperumal for single-event-upset related materials; Zhiming Feng and Yan Cui for Cadence simulation and noise modeling; Jin Tang, Zhengrong Jin for noise measurements; Jun Pan for high frequency experiments.

This work was supported by DARPA under the Radiation Hardening By Design (RHBD) program, NASA-GSFC under NASA Electronic Parts and Packaging Program, and DTRA under the Radiation Hardened Microelectronics Program. Special thanks are owed to J.D. Cressler, P. W. Marshall, R. Reed, R. Ladbury, K. Label, L. Cohn, and A. Joseph.

I appreciate Jun Wang and Liang Yu for their support as good friends. Last but not least, I am deeply indebted to my beloved parents, you are always there for me, sharing the happiness and soothing the sorrow. Thank you!

Style manual or journal used IEEE Transactions on Electron Devices (together with the style known as "aums"). Bibliography follows van Leunen's *A Handbook for Scholars*.

Computer software used The document preparation package TEX (specifically LATEX) together with the departmental style-file `aums.sty`. The plots were generated using PSPICE®, MATLAB®, Microsoft Visio®, Adobe Illustrator®and Taurus Visual®.

TABLE OF CONTENTS

List of Figures

LIST OF TABLES

CHAPTER 1

INTRODUCTION

1.1 Motivation

The operation of electronic systems in a space environment presents a host of challenges for device, circuit, and system designers. It has been recognized since the beginning of the space program in 1950s that earth orbit presents an amazingly hostile environment and is seething with lethal levels of radiation [1]. As Silicon Germanium Heterojunction Bipolar Transistor (SiGe HBT) technology has become an important semiconductor technology for both wired and wireless telecommunications applications because of its superior analog and RF performance, together with its CMOS integration capability, their radiation response is of interest to spacecraft designers ready to insert the latest technology into their system [2]. For space applications, as fabricated SiGe HBTs were shown robust to ionization and displacement damage [1]. However, recent testing [3], [4], and quasi-3D simulations [5] have shown that SiGe HBT logic circuits could be vulnerable to single event effects (SEE). To understand the SEE in SiGe circuits, it is necessary to investigate the charge collection behavior in the transistors.

This thesis presents full 3D simulations of heavy-ion induced charge collection in the 200 GHz state-of-art SiGe HBT technology. The sensitive areas of charge collections for each terminal are identified based on analysis of the device structure and simulation results from ion track position dependence study. A new junction passing / deep trench

(DT) confinement model is supported in this 200 GHz SiGe HBT by angle strike dependence study. Further more, a new back junction approach for reducing charge collection was presented at 2005 *IEEE Nuclear and Space Radiation Effects Conference* under the title, "A New Back Junction Approach For Reducing Charge Collection in 200 GHz SiGe HBTs," [6].

1.2 SiGe HBT Device Physics

The use of SiGe alloys in the base of SiGe HBTs is a successful attempt at employing bandgap engineering in the Si material system, similar to the one employed in III-V devices, and has enabled the realization of Si-based RF and microwave circuits. For space applications, we are more interested in high speed digital SiGe HBT circuits. SiGe films are often grown epitaxially on Si using the ultrahigh vacuum / chemical vapor deposition (UHV/CVD) technique.

The energy bandgap of Ge is smaller than that of Si (0.66 eV versus 1.12 eV), and therefore the bandgap of SiGe is smaller than Si, facilitating bandgap engineering in Si. There is also additional bandgap shrinkage due to compressive strain associated with SiGe alloys. There is about 7.5meV reduction in bandgap for every 1% of Ge introduced. This Ge-induced band offset occurs predominantly in the valence band, which is ideally suited for n-p-n transistors.

The DC and AC characteristics of SiGe HBTs offer performance advantages over Si BJTs. The presence of the Si-SiGe heterojunctions at the EB and CB junctions contribute to this performance improvement in SiGe HBTs over Si BJTs. The effects that

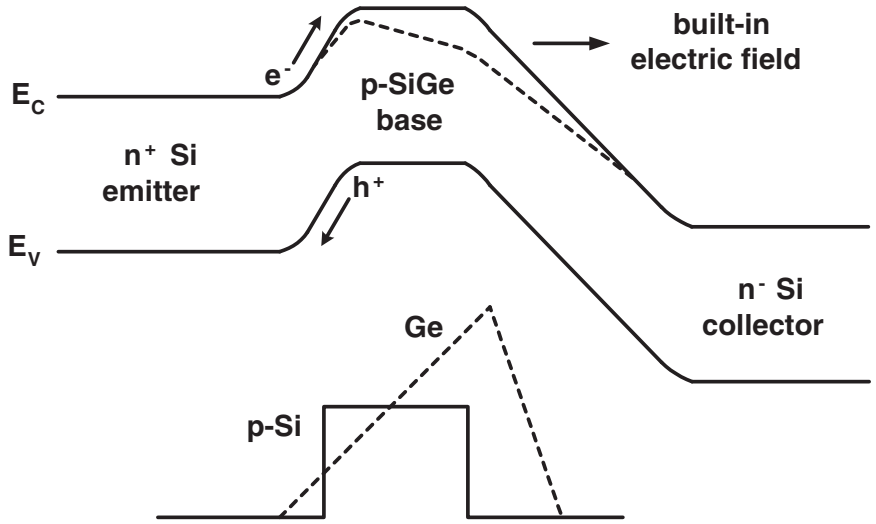


Figure 1.1: Energy band diagram of a graded-base SiGe HBT as compared to an identically constructed Si BJT. Source: [1].

result due to presence of these heterojunctions are depicted in the energy-band diagram of these devices shown in Figure 1.1. The band diagram shows a finite band offset at the EB junction [$\Delta E_{g,Ge}(x = 0)$] along with a larger band offset at the CB junction [$\Delta E_{g,Ge}(x = W_b)$]. The position dependence of the band offset is expressed in terms of a bandgap grading term [$\Delta E_{g,Ge}(grade) = \Delta E_{g,Ge}(W_b) - \Delta E_{g,Ge}(0)$], which induces an electric field in the neutral base region. The presence of the electric field is conducive for the transport of minority carriers (electrons) from emitter to collector, thereby improving the frequency response.

Addition of Ge in the base causes the collector current density (J_C) to increase. This is made possible due to increased electron injection at EB junction, yielding more emitter-to-collector charge transport for a given EB bias. This increase in J_C results in

an increase in current gain β as a result of the introduction of Ge. From a device-physics point of view, the intrinsic carrier concentration is reduced by a factor of exponential of the Ge-induced bandgap offset in the base, as given by the following expression [1]:

$$n_{ib}^2(x) \;=\; \gamma\, n_{io}^2\, e^{\Delta E_{gb}^{app}/kT}\, e^{\left[\Delta E_{g,Ge(grade)}\, \frac{x}{W_b \times kT}\right]}\, e^{\Delta E_{g,Ge(0)}/kT} \tag{1.1}$$

where $\Delta E_{gb}^{app}/kT$ is the bandgap narrowing due to heavy doping in the base and $\gamma = N_C N_V(SiGe)/N_C N_V(Si)$ represents the reduction in the effective density-of-states product due to increasing Ge content in the base. The expression for J_C can be obtained in closed form using the Moll–Ross relation [1], given by,

$$J_C \;=\; \frac{q\,(e^{qV_{BE}/kT} - 1)}{\int_0^{W_b} \left(\frac{N_b(x)}{D_{nb}(x)\, n_{ib}^2(x)}\right) dx} \tag{1.2}$$

where W_b is the quasi-neutral base width at bias V_{BE}, and D_{nb} is the minority electron diffusivity in the base. Note that all of these results assume low-injection conditions.

Using Equations (1.1) and (1.2), an expression for collector current density can be obtained as a function of bias and temperature [1]:

$$J_{C,SiGe} = \frac{qD_{nb}(e^{qV_{BE}/kT} - 1)\, n_{io}^2\, e^{\Delta E_{gb}^{app}/kT}}{N_{ab}^- W_b} \left[\frac{\widetilde{\gamma}\widetilde{\eta}\, e^{\Delta E_{g,Ge}(0)/kT} \Delta E_{g,Ge}(grade)/kT}{1 - e^{-\Delta E_{g,Ge}(grade)/kT}}\right] \tag{1.3}$$

where the " $\widetilde{}$ " refers to a position-averaged quantity, N_{ab} indicates the active doping level in the base, and $\eta = D_{nb}(SiGe)/D_{nb}(Si) > 1$ accounts for the strain enhancement of the minority electron mobility with increasing Ge content in the base. The effect of

Ge profile is captured by the second term of Equation (1.3). Therefore, improvement in β in a SiGe HBT over a similarly-constructed Si BJT can be expressed as the ratio of their respective J_C's, to give [1]:

$$\frac{J_{C,SiGe}}{J_{C,Si}} = \frac{\beta_{SiGe}}{\beta_{Si}} = \widetilde{\gamma}\widetilde{\eta}\frac{\Delta E_{g,Ge}(grade)/kT\, e^{\Delta E_{g,Ge}(0)/kT}}{1 - e^{-\Delta E_{g,Ge}(grade)/kT}} \tag{1.4}$$

This ratio is larger than unity for finite Ge content. As β is influenced strongly by the content and profile of Ge in the base, it can be tailored for a specific need and also effective *decouples* β from the specifics of the base doping profile. For example, base doping can be increased further without comprising the current gain (as it is in Si BJTs). This reduces the base resistance (R_b), leading to enhanced frequency response and improved broadband noise performance. In addition, β can be made independent of temperature with this Ge lever, which can be important from a circuit standpoint. The Gummel characteristics for identically-constructed SiGe HBTs and Si BJTs show a remarkable improvement in gain for the SiGe HBT due to increase in J_C (Figure 1.2).

Another important DC consequence of a graded Ge profile is the exponential enhancement of output conductance, which is reflected in the Early voltage (V_A) [1].

$$\frac{V_{A,SiGe}}{V_{A,Si}} = e^{\Delta E_{g,Ge}(grade)/kT}\left[\frac{1 - e^{-\Delta E_{g,Ge}(grade)/kT}}{\Delta E_{g,Ge}(grade)/kT}\right] \tag{1.5}$$

The "current gain–Early voltage product" (βV_A product), which is an important figure of merit for analog applications such as high-speed data converters and precision current

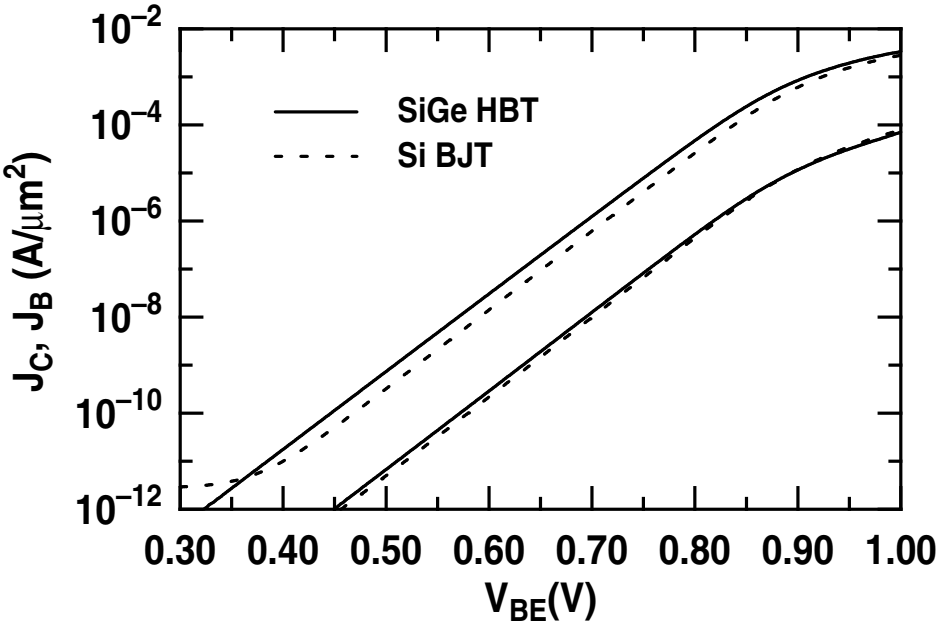


Figure 1.2: Typical Gummel characteristics of a SiGe HBT as compared to a Si BJT of identical construction. Source: [1]

sources, and is strongly enhanced in SiGe HBTs over Si BJTs [1].

$$\frac{\beta V_A|_{SiGe}}{\beta V_A|_{Si}} = \widetilde{\gamma}\,\widetilde{\eta}\, e^{\Delta E_{g,Ge}(0)/kT}\, e^{\Delta E_{g,Ge}(grade)/kT} \tag{1.6}$$

Observe that the βV_A product in a SiGe HBT depends exponentially on both the EB band offset and the Ge grading, and can thus be made arbitrarily large in applications that require it.

The transistor frequency response limits system performance in most RF and microwave circuit applications. An important figure-of-merit in bipolar transistor is the unity-gain cut-off frequency (f_T). For low-injection, f_T in a bipolar transistor can be

written generally as [1],

$$f_T = \frac{1}{2\pi}[g_m(C_{te}+C_{tc})+\tau_b+\tau_e+\frac{W_{CB}}{2v_{sat}}+r_cC_{tc}]^{-1}. \quad (1.7)$$

where $g_m = \frac{kT}{qI_C}$ is the intrinsic transconductance at low-injection, C_{te} and C_{tc} are the EB and CB depletion capacitances, τ_b is the base transit time, τ_e is the emitter charge storage delay time, W_{cb} is the CB space-charge region width, v_{sat} is the saturation velocity, and r_c is the dynamic collector resistance. the base, collector and emitter transit times, respectively. With the introduction of Ge, τ_b decreases due to built-in electric field induced by the Ge grading across the neutral base region. Physically, this effect is due to rapid acceleration of carriers across the base [1].

$$\frac{\tau_{b,SiGe}}{\tau_{b,Si}} = \frac{2}{\eta}\left(\frac{kT}{\Delta E_{g,Ge}(grade)}\right)\times\left[1-\frac{1-e^{-\Delta E_{g,Ge}(grade)/kT}}{\Delta E_{g,Ge}(grade)/kT}\right] \quad (1.8)$$

In addition, due to the reciprocal relation between τ_e and ac β, the band offset at EB junction also serves to improve the SiGe HBT frequency response, since [1],

$$\frac{\tau_{e,Si}}{\tau_{e,SiGe}} = \frac{\beta_{SiGe}}{\beta_{Si}} = \widetilde{\gamma}\widetilde{\eta}\frac{\Delta E_{g,Ge}(grade)/kT\, e^{\Delta E_{g,Ge}(0)/kT}}{1-e^{-\Delta E_{g,Ge}(grade)/kT}} \quad (1.9)$$

A more relevant figure-of-merit for practical RF and microwave applications is the unity power-gain frequency, or maximum oscillation frequency (f_{max}), since it depends

on both the unity-gain frequency (f_T) and the device parasitics, as given by [1],

$$f_{max} = \sqrt{\frac{f_T}{8\pi C_{cb} r_{bb}}} \tag{1.10}$$

where C_{cb} is the total CB capacitance and r_{bb} is the total ac base resistance. Introducing Ge into the base region helps improve both f_T and r_{bb} [1].

The ECL gate represents the fundamental building block for modern high-speed bipolar-based digital system. The ECL ring oscillator remains today a simple and powerful metric for assessing overall technology performance, since it provides more information than that captured by f_T and f_{max}, and yet is much simpler to design and test than a static or dynamic frequency divider. The fundamental basis of the ECL gate is the differential amplifier, or from a digital viewpoint, more appropriately referred to as the "current switch". A current switch combined with emitter-follower output drivers forms the basic single-level ECL gate, as depicted in Fig. 1.3. The ECL gate is a low-logic-swing, nonsaturating logic family that thus provides high-speed switching, and also combines powerful logical functionality and efficient capacitive load driving capability. Typical ECL characteristics include: 400-800mV logic swing, 1-10mW power dissipation, 3.3-3.6V supply and sub-20-picosecond unloaded gate delay [1].

1.3 Radiation Effects

Radiation damage to on-board electronics may be separated into two categories: total ionizing dose and single event effects. Total ionizing dose (TID) is a cumulative

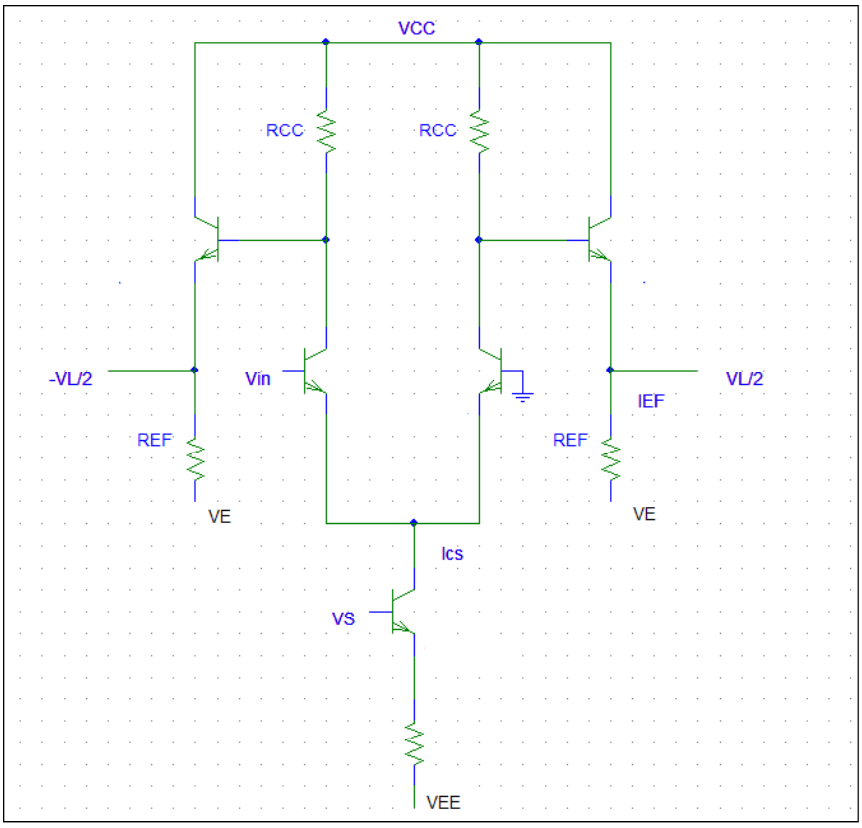


Figure 1.3: Circuit schematic for a generic ECL digital logic gate. Source: [1]

long-term degradation of the device when exposed to ionizing radiation. Single event effects (SEEs) are individual events which occur when a single incident ionizing particle deposits enough energy to cause an effect in a device.

There are many device conditions and failure modes due to SEE, depending on the incident particle and the specific device. It may be convenient to think of two types of SEEs: soft errors and hard errors. Soft errors are nondestructive to the device and may appear as a bit flip in a memory cell or latch, or as transients occurring on the output

of an I/O, logic, or other support circuit. Also included are conditions that cause a device to interrupt normal operations and either perform incorrectly or halt. Hard errors may be (but are not necessarily) physically destructive to the device, but are permanent functional effects. Different device effects, hard or soft, may or may not be acceptable for a given design application [7].

Single event phenomena can be classified into three effects in order of permanency [8]:

1. Single event upset, soft error.
2. Single event latchup, soft or hard error.
3. Single event burnout, hard failure.

Single event upset (SEU) is concerned in this work.

Single Event Upset (SEU) is defined by NASA as "radiation-induced errors in microelectronic circuits caused when charged particles (usually from the radiation belts or from cosmic rays) lose energy by ionizing the medium through which they pass, leaving behind a wake of electron-hole pairs." [Ref: NASA Thesaurus].

SEUs are transient soft errors, and are non-destructive. A reset or rewriting of the device results in normal device behavior thereafter. An SEU may occur in analog, digital, or optical components, or may have effects in surrounding interface circuitry. SEUs typically appear as transient pluses in logic or support circuitry, or as bit flips in memory cells or registers. Also possible is a multiple-bit SEU in which a single ion hits two or more bits causing simultaneous errors. Multiple-bit SEU is a problem for single-bit error detection and correction (EDAC) where it is impossible to assign bits within a

word to different chips (e.g., a problem for DRAMs and certain SRAMs). A severe SEU is the single-event functional interrupt (SEFI) in which an SEU in the device's control circuitry places the device into a test mode, halt, or undefined state. The SEFI halts normal operations, and requires a power reset to recover.

The SEUs are caused by two different space radiation sources: high energy protons, and cosmic rays, specially, the heavy ion components of either solar or galactic origins.

The latter heavy ions cause direct ionization within a device. While protons typically do not cause an upset through direct ionization, but rather through complex nuclear reactions in the vicinity of the sensitive node. Fig. 1.4 is the illustration of the two different SEU mechanisms.

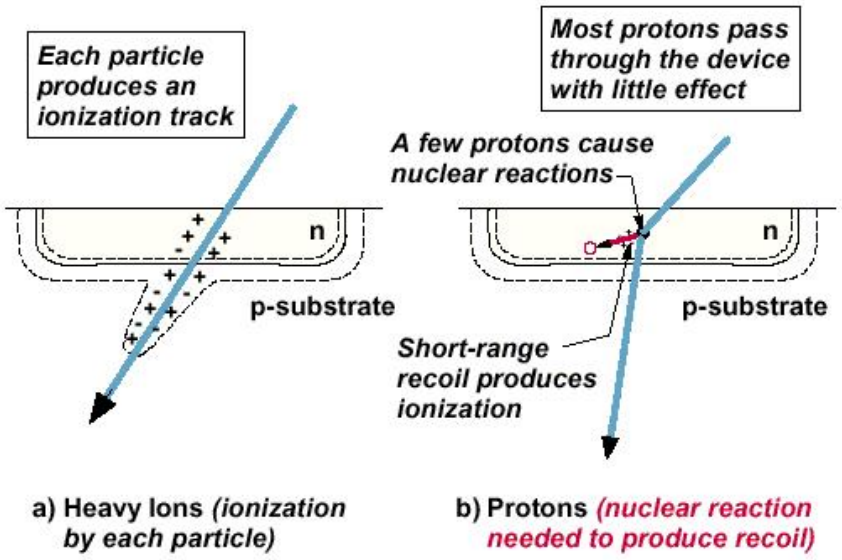


Figure 1.4: Source: "Space Radiation Effects on Microelectronics," NASA Jet Propulsion Laboratory.

1.3.1 Linear Energy Transfer

Linear Energy Transfer (LET) is a measure of the energy transferred to the device per unit length as an ionizing particle travels through a material.

When an energetic charged particle passes through a semiconductor, it generates electron-hole pairs along its path as it loses energy. When all of its energy is lost, the particle comes to a rest in the semiconductor, and the total path length it travelled is referred to as the particle's *range*. LET is the term we frequently use to describe the energy loss per unit path length of a particle as it passes through a material. LET has a unit of $MeV/cm^2/mg$ and maybe quoted independent of the target, because the energy loss per unit path length (MeV/cm) is normalized by the density of the target material (mg/cm^3). The LET of the particle can be easily related to the charge deposition per unit path length, because for a given material it takes a known amount of energy to generate an electron-hole pair. For instance, in silicon, one electron-hole pair is generated for every 3.6 eV of energy loss, and silicon has a density of 2328 mg/cm^3, so that an LET of $97 MeV/cm^2/mg$ corresponds to a charge deposition of $1 pC/\mu m$. This conversion factor of about 100 is used in Davinci to convert between LET and charge deposition [1].

1.3.2 Critical Charge

Device immunity is determined by its *linear energy transfer threshold* (LET$_{th}$). The LET$_{th}$ is defined as the minimum LET to cause a single-event effect at a particle fluence of 10^7 ions/cm^2. SEE-immune is defined as a device having an LET$_{th}$ > 100

$MeV/cm^2/mg$ [10]. Low LET_{th} implies proton sensitivity. If a device is not SEU immune, the device is analyzed for SEU rates and effects.

The present trends (e.g., device size and power reduction, line resolution increase, increased memory and speed) will only heighten the SEU susceptibility. This is easily seen when one considers the device as a simple capacitor (C) upon which the ionized particle deposits sufficient charge (Q) to result in a voltage (i.e., logic state) change. SEU occurs when LET > Q_{crit}.

Since the LET_{th} is equivalent to the LET required to produce a voltage change (V) sufficient for an SEU, then mathematically:

$$LET_{th} \propto \Delta V = Q/C$$

As the size of these active devices decreases, the capacitance will decrease and so the charge necessary to induce the SEU. This critical charge is that charge necessary to flip a binary "1" to a "0" or vice-versa, but is less than the total stored charge. Specifically, Q_{crit} is then the difference between the storage node charge and the minimum charge required for the sensing amplifier to read correctly. In SRAM circuits, Q_{crit} depends not just on the charge collected but also the temporal shape of the current pulse [8].

1.3.3 Parallelepiped-shaped Model

Parallelepiped-shaped Model: A very elementary model of SEU behavior can be formed using the concept of LET through some depth of a parallelepiped-shaped device

[8]. A first-order estimate of the minimum LET required for causing an SEU can be computed. Consider a parallelepiped of dimensions a, b, c where c is the device depth as in Fig. 1.5, the minimum LET corresponds to the maximum chord length possible, which is the diagonal of the parallelepiped.

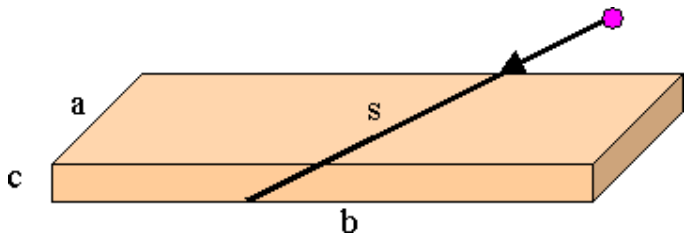


Figure 1.5: Parallelepiped-shaped device model of dimensions a, b, c where c is the device depth.

Critical Angle, θ_c : As the incidence angle deviates from normal, the path length traversed by the radiation increases. The angle from incident at which upsets occur for a given particle LET is known as the critical angle. As in Fig. 1.6, a parallelpiped particles incident at an angle θ have a path that is $1/\cos(\theta)$ longer than the path at normal incidence, thus producing more ionization charge. However, as we will discuss later in Chapter 5, this "cosine law" fails in our 200 GHz SiGe HBTs, hence we propose a new model to explain the angle dependence of charge collecion.

1.3.4 Cross Section

As in nuclear physics, the probability of a given SEE can be expressed with the concept of SEE *Cross section* (σ), σ = #errors/ion fluence. The units for cross section are cm^2 per device or per bit. Typically, for incident ions with sufficient LET to induce

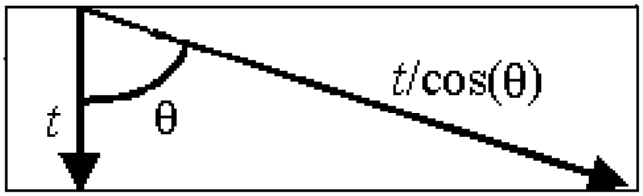


Figure 1.6: Cosine Law.

an SEE, the measured cross section is correlated with the physical location (volume) inside the device or circuit that is most vulnerable to upset. *Sensitive volume* refers to the device volume affected by SEE-inducing radiation. The geometry of the sensitive volume is not easily known, but some information is gained from test cross section data.

Recent work [11] has demonstrated that SiGe HBT logic from IBM and Jazz, as well as the IBM CMOS incorporated in the SiGe BiCMOS process all show significant sensitivity which varies with data rate and is often characterized by complex burst errors as opposed to single bit errors. Paul Marshall et al proposed a new Circuit for Radiation Effects Self Test (CREST) approach which was implemented as a 127-bit shift register. They have completed testing the shift registers using an Anritsu MP1750A BERT and characterized each of the registers in the 5AM CREST ASIC with heavy ions at Texas A&M University cyclotron and also at the NRL pulsed laser SEE test facility. The five styles of flip flops are: 1) standard master-slave with 1 μm transistors and a nominal current of 0.6 mA; 2) standard master-slave with 2.5 μm transistors and a higher current of 1.5 mA; 3) standard master-slave with triple-redundant 1 μm transistors (referred to as current shared hardened) with a nominal current of 0.6 mA each (for a total of 1.8

mA); 4) dual-interleaved master-slave with 2.5 μm transistors and a higher current of 3 mA; and 5) cross-coupled NAND gate with 1 μm transistors and a nominal current of 0.6 mA.

Example results are shown in Fig. 1.7 which plots the Event Cross Section (irrespective of the number of errors associated in the case of burst events) against the effective LET for each of the 5 register designs [12]. Though there are significant differences in trends noted near the threshold LET, the results are similar given the 5 substantially different register designs.

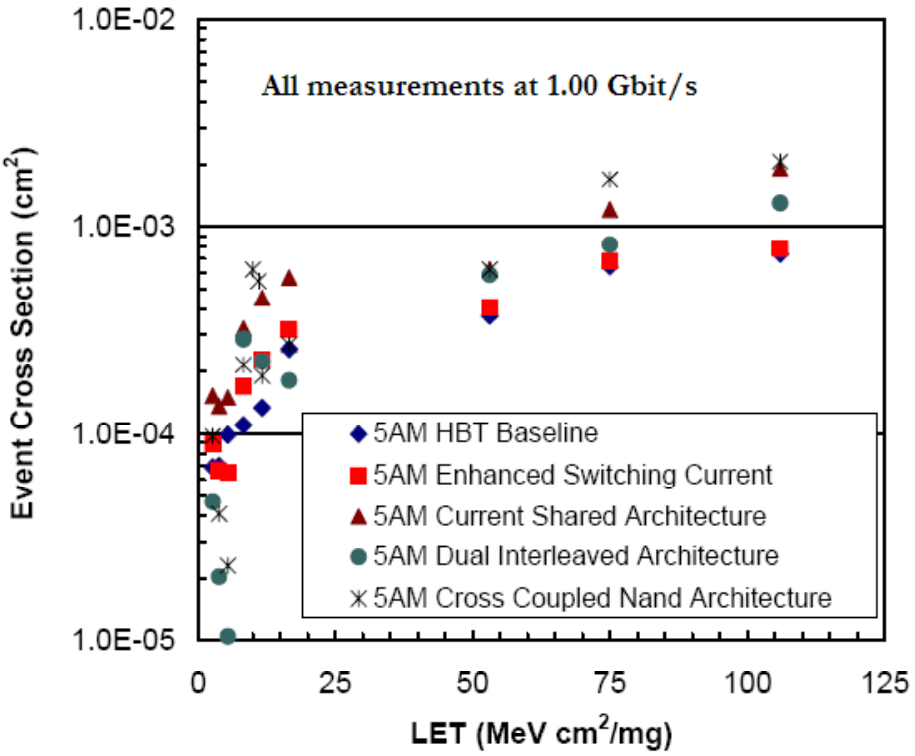


Figure 1.7: The event cross section versus LET for the 5 SiGe HBT shift registers. Data rate is 1 Gbit/s. Source: [12].

1.3.5 Practical SEU Rate Calculation

The upset rate may be reported as errors per day per chip, or errors per day per bit (errors/bit-day). Error rates of hardened devices can be of the order of 10^{-8} errors/bit-day; unhardened devices are generally several orders of magnitude higher.

There are three basic steps in the calculation of SEU Rates, refer to Fig. 1.8 [8]:

1. Measure the cross section (σ) versus LET for example using accelerator testing. The device cross section is defined as the ratio of the number of upsets to the particle fluence. The experimentally determined cross section is a function of particle energy (LET).

2. Determine the *sensitive device volume*. The sensitive volume is smaller than the actual device physical volume. The sensitive volume is generally different for SEE from heavy ions and protons, as well as SEL. The sensitive geometry and critical charge are the most difficult parameters to determine.

3. To determine the device error rate, integrate the cross section and sensitive device volume with the LET spectrum.

Device simulation can be used in this process for more accurate results.

1.4 SEU-induced Charge Collection

When a particle strikes a microelectronics device, the most sensitive regions are usually reverse-biased p/n junctions. The high field present in a reverse-biased junction depletion region can very efficiently collect the particle induced charge through drift processes, leading to a transient current at the junction contact. Strikes near a depletion

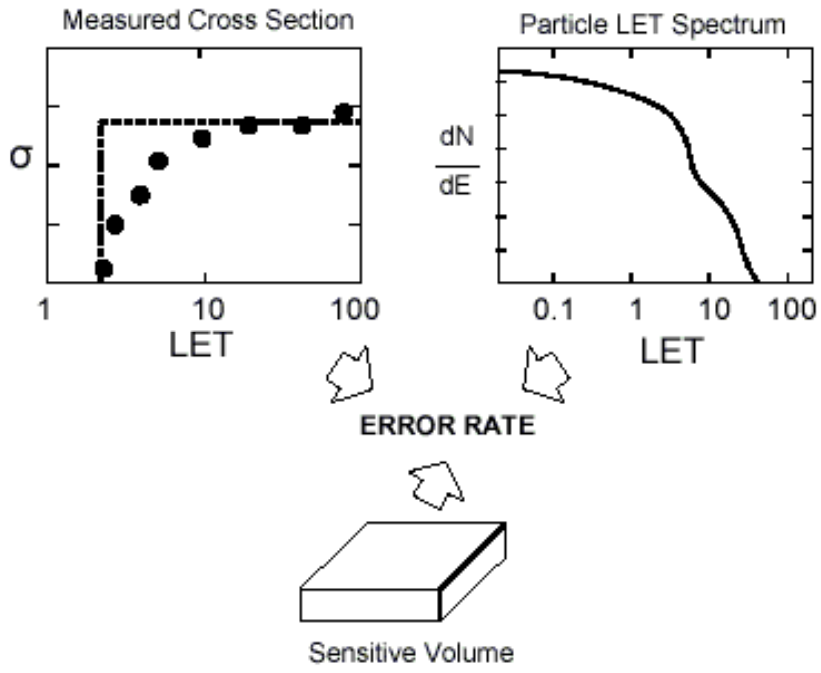


Figure 1.8: Source: "Space Radiation Effects on Microelectronics," NASA Jet Propulsion Laboratory

region can also result in significant transient currents as carriers diffuse into the vicinity of the depletion region field where they can be efficiently collected. IBM researchers discovered the "field-funneling effect" during their study of alpha-particle-induced charge collection in p/n junctions. As shown in Fig. 1.9, the transient disturbance in the junction electrostatic potential is termed "field funnel". Charge generated along the particle track can locally collapse the junction electric field due to the highly conductive nature of the charge track and separation of charge by the depletion region field. This funneling

effect can increase charge collection at the struck node by extending the junction electric field away from the junction and deep into the substrate, such that charge deposited some distance from the junction can be collected through the efficient drift process [2].

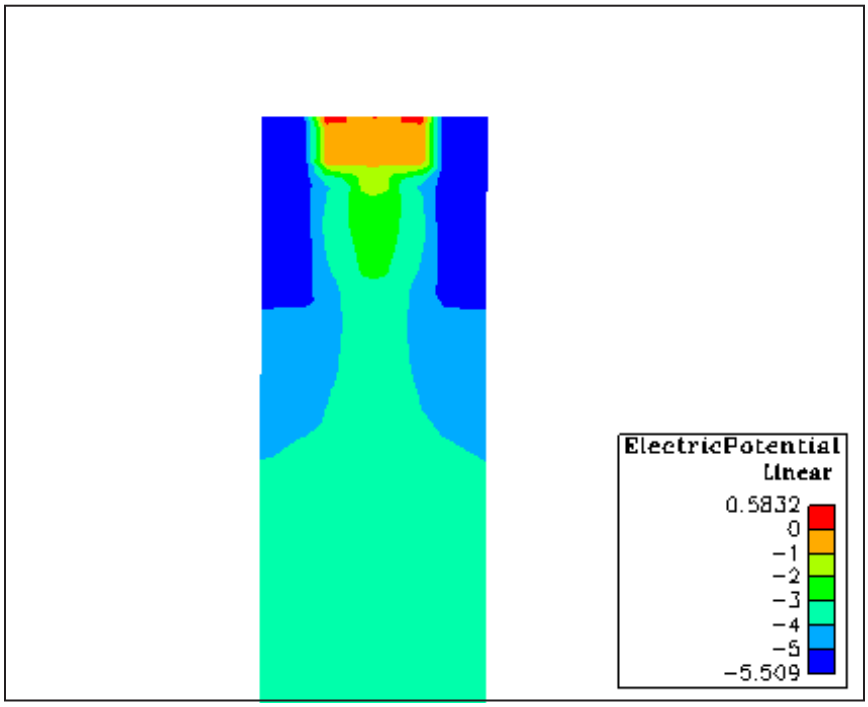


Figure 1.9: Illustration of funneling following an ion strike,electrostatic potential.

1.5 Thesis Contributions

- *New back junction approach for reducing SEU-induced charge collection*

- *Sensitive area identification of SEU-induced charge collection for each terminal*

- *A new junction passing / deep trench (DT) confinement model for angle strike*

This thesis is organized as follows: Chapter 2 introduces device simulation concepts and full 3D device simulation for SEU-induced charge collections. Chapter 3 details SEU-induced charge collection characteristics and internal device behavior in 200 GHz SiGe HBT. Chapter 4 investigates on ion strike position dependence and identifies sensitive areas of SEU-induced charge collections for each terminal. Chapter 5 explores on the angle strike charge collection and proposes a new junction passing / DT confinement model. Chapter 6 presents the new back junction approach for reducing SEU-induced charge collection in SiGe HBTs. The last chapter concludes the results obtained.

CHAPTER 2

SEU DEVICE SIMULATIONS

Semiconductor simulation capability enables comprehensive "what if" technology development studies that are not experimentally feasible from the standpoints of time and money. In the radiation effects arena, the use of device simulation tools to study single-event phenomena is fairly widespread.

2.1 The Need for Three-Dimensional Simulation

As an incident-charged particle passes through the device and loses energy, electron-hole pairs are generated along the particle path, thereafter drifting and diffusing under the influence of potential and carrier concentration gradients. This is clearly a 3-D problem. Although 2-D simulations may provide basic insight, 3-D simulation is necessary for truly predictive results. In a 2-D simulation, all quantities are assumed to be extruded into the third dimension, hence either the correct generated charge density or the correct total generated charge can be simulated, not both. Quasi-3-D simulations were developed to provide correct generated charge density and total charge, based on cylindrical symmetry and coordinate transformations. Because the calculations are still performed in two spatial variables (radius and depth), the computational burden is no greater than a standard 2-D. However, the cylindrically symmetric simulations do not accurately reproduce true 3-D results due to its incorrect geometry. A comparison of the effects of simulating an ion strike in different dimensions is shown in Fig. 2.1 [13].

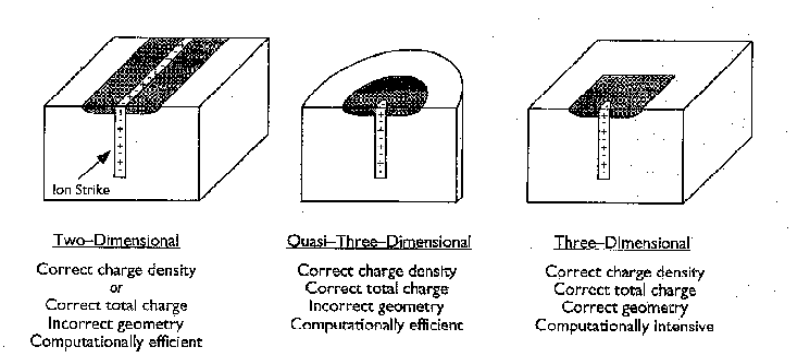


Figure 2.1: Illustration of the effects of simulating an ion strike in different dimensions [13].

2.2 Modeling Methodology

The most commonly used technique for device modeling is that of the drift-diffusion models. The primary function of Davinci (the full 3-D simulation tool we use in our work) is to solve the three partial differential equations self-consistently for the electrostatic potential, ϕ, and for the electron and hole concentration, n and p, respectively. The electrical behavior of semiconductor devices is governed by Possion's equation [9]:

$$\epsilon \nabla^2 \phi = -q(p - n + N_D^+ - N_A^-) - \rho_s. \tag{2.1}$$

and continuity equations for electron and holes [9]:

$$\frac{\partial n}{\partial t} = \frac{1}{q} \overrightarrow{\nabla} \cdot \boldsymbol{J}_n - \boldsymbol{U}_n. \tag{2.2}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\vec{\nabla} \cdot J_p - U_p. \tag{2.3}$$

Throughout Davinci, ϕ is always defined as the intrinsic Fermi potential. N_D^+ and N_A^- are the ionized impurity concentrations and ρ is a surface charge density that may be present due to fixed charge in insulating materials or charged interface states. U_n and U_p represent net electron and hole recombination, respectively. From Boltzmann transport theory, $\vec{J_n}$ and $\vec{J_p}$ can be written as function of ϕ, n, and p, consisting of drift and diffusion components.

$$\vec{J_n} = qn\mu_n\vec{E} + qD_n\nabla n. \tag{2.4}$$

$$\vec{J_p} = qp\mu_p\vec{E} - qD_p\nabla p. \tag{2.5}$$

where $\mu_n$and μ_p are the electron and hole mobilities and D_n and D_p are the electron and hole diffusivities [9].

Because of the assumptions they are based on, the drift-diffusion models are ill suited to treat many effects becoming important in ever smaller geometry devices, such as velocity overshoot, carrier heating, and quasi-ballistic transport.

The next step up in the device simulation hierarchy is hydrodynamic and energy-balance codes, which begin to treat nonlocal effects, based on five equations of state. The top rung is Monte Carlo simulation, which describes carrier transport on a fundamental, microscopic scale using classical equations of motion.

The less assumptions are made, the more accurate the results are and the more computationally intensive the simulation becomes. The drift-diffusion methods remain the major simulation tools because of their computational efficiency [13], and are employed in this work.

2.3 Device Construction

3D device simulations are performed using Davinci. First the device is constructed from the layout and process information. Then ion track is placed; after selection of necessary physical models, the input deck is ready for SEU simulations.

2.3.1 Process Information

The device is fabricated layer by layer using specific materials through different process techniques. The layout provides the exact geometry of material boundary; the cross section provides the internal view of device regions. The 3D structure of the device is gained through the combination of the layout and cross section.

Fig. 2.2 is the layout that we used to construct the device, which clearly shows each mask from all layers. We need the cross section information to determine exactly the device structure to be implemented into simulation tools. Fig. 2.3 shows the schematic cross section of the raised extrinsic base SiGe HBT, not to scale. The substrate, collector, raised extrinsic base, emitter are all silicon; while the intrinsic base is SiGe, and all the isolation DT (Deep Trench) and STI (Shallow Trend Isolation) are of SiO_2.

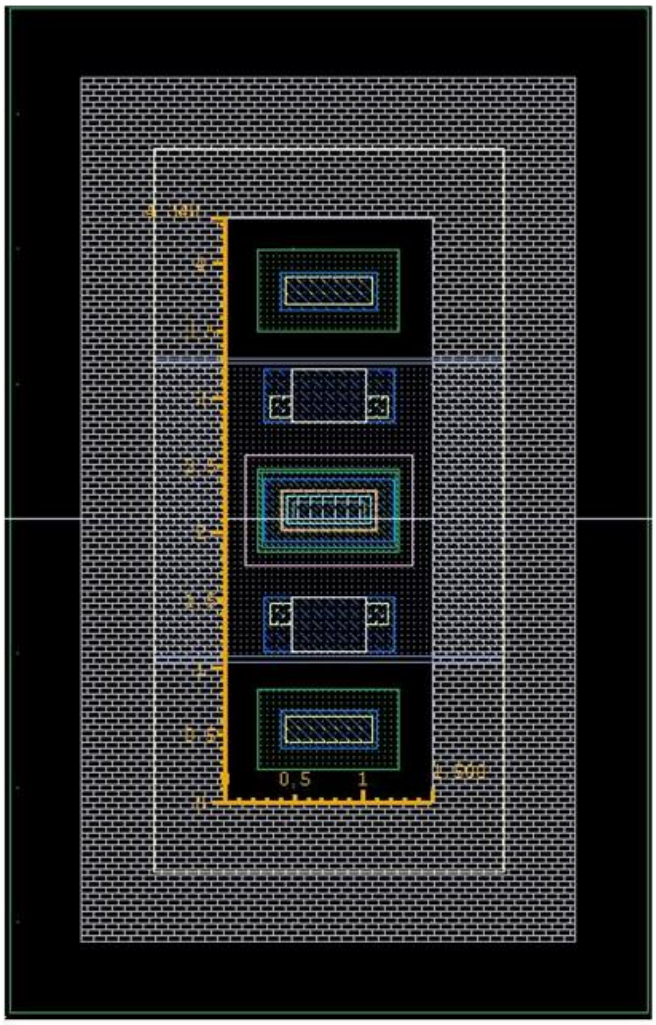


Figure 2.2: Layout of SiGe HBT used in this work. $A_E = 0.12 \times 0.52\mu m^2$, area inside DT = $4.34 \times 1.5\mu m^2$. Source: IBM.

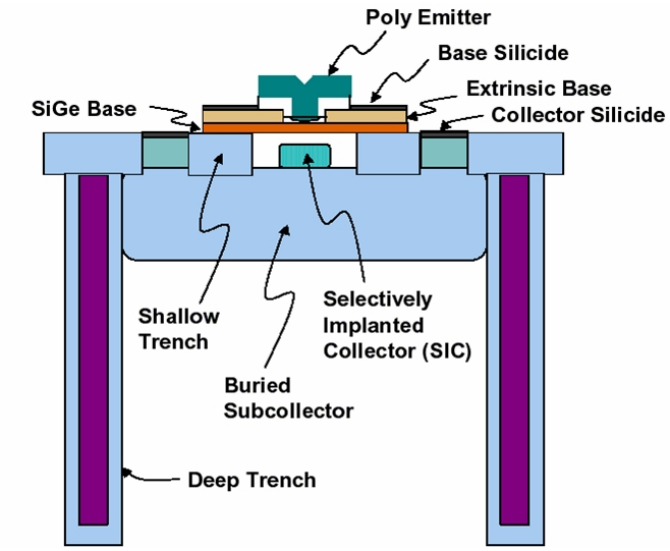


Figure 2.3: The schematic cross section of the raised extrinsic base SiGe HBT, not to scale. Source: [14].

2.3.2 Structure for Simulation

The structure of the device is created in Davinci through MESH. X.MESH, Y.MESH, Z.MESH statements specify the number and placement of grid lines in the structure. Then various regions of the device, such as semiconductor, insulator, and electrodes, are defined by the REGION statements. Then the ELECTRODE statements specify the locations of electrodes within the device. Impurity profiles are read from the SIMS files for the intrinsic device and generated analytically for the other parts.

2.3.3 Mesh and Gridding

Gridding, or mesh generation, is an issue central to any device simulation. For accurate solutions, the more grids/finer mesh, the better. However, as the three governing equations have to be solved at every node, and the solution time increases exponentially with the increase of nodes, reduction of unnecessary nodes is clearly of great importance. There is a tradeoff between accuracy and efficiency here.

X.MESH and Z.MESH are used to specify different layers of the device while Y.MESH is to define the depth of the device. Lines are placed at critical boundaries and finer mesh is placed in the intrinsic part.

Davinci provides regridding based on the total photogeneration.

```
PHOTOGEN            X.START=3.17  X.END=3.17
+                   Z.start=1.75 Z.end=1.75
+                   Y.START=0.0  Y.END=12
+                   DCHR=0.2
```

```
+                    T0=4.0E-12  TC=2.0E-12  C1=0.07 PC.UNITS  GAUSS

comment     grid refinement based on total photogeneration
regrid      photogen factor=1.2 smooth=-1 y.max=20
+           out.file=8hp_compfine2
```

Comparison of fig. 2.4 and fig. 2.5 clearly shows that finer mesh is placed along the ion track after regridding.

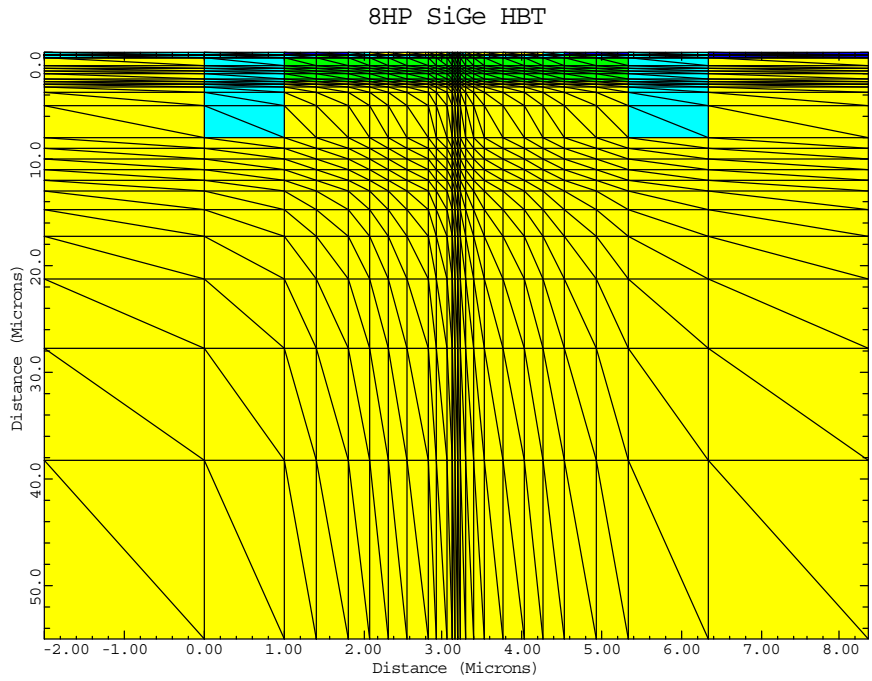


Figure 2.4: Davinci graphical output generated by PLOT.2D showing the grids and materials of entire device.

The effects of regrid are not very obvious in our simulations as in Fig. 2.6, because, for center strike, we have already been using very fine mesh along the ion track.

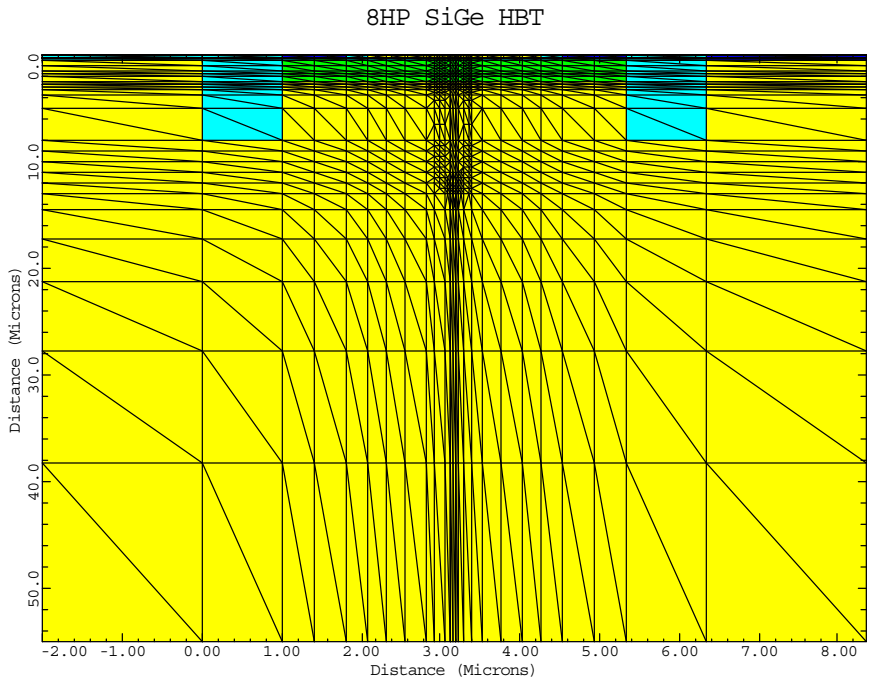


Figure 2.5: Photogeneration based regrid. Finer mesh is generated along the ion track.

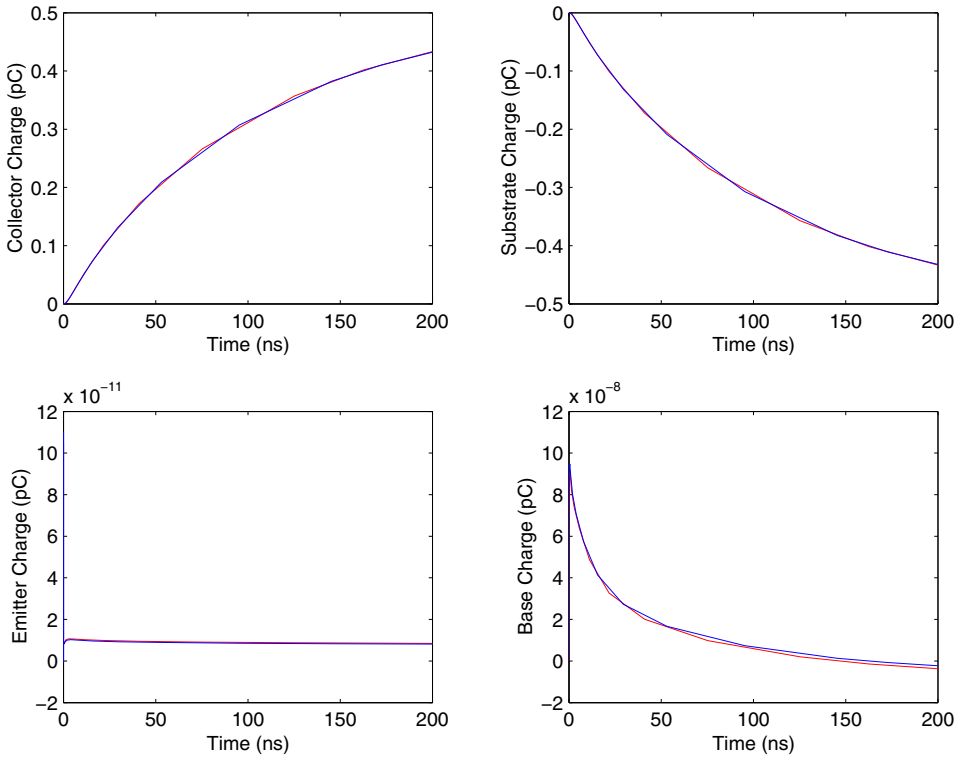


Figure 2.6: Comparison of charge collection with and without regrid.

2.3.4 Region Definition and Contact Placement

In Davinci, REGION statement is very convenient to use, because, the later REGION statement overwrites the former REGION statement if there are region overlaps. The whole device structure is divided into several layers to be put into the simulator. The code and the detailed explanation are as follows:

```
$ below DT  8-55
region    name=1  silicon y.min=8 y.max=55


$ $ DT & psub & n buri 0.5-8
region    name=2c  silicon y.min=0.5 y.max=8


region    name=2a  oxide y.min=0.5 y.max=8
+         x.min=0 x.max=6.34 z.min=0 z.max=3.5
region    name=2b  silicon y.min=0.5 y.max=8
+         x.min=1 x.max=5.34 z.min=1 z.max=2.5


$ $ ST & Coll contact & Emitter Hole  0.16-0.5
region    name=3a  oxide y.min=0.16 y.max=0.5
region    name=3b  silicon y.min=0.16 y.max=0.5
+         x.min=1.25 x.max=1.82 z.min=1.25 z.max=2.25
region    name=3c  silicon y.min=0.16 y.max=0.5
+         x.min=2.82 x.max=3.52 z.min=1.25 z.max=2.25
```

```
region    name=3d  silicon y.min=0.16 y.max=0.5
+         x.min=4.52 x.max=5.09 z.min=1.25 z.max=2.25


$ $ EB layer 0-0.16
$  around
region    name=4a  oxide y.min=0 y.max=0.16
$  intrinsic base
region    name=4b  silicon y.min=0.12 y.max=0.16
+         x.min= 2.07 x.max=4.27 z.min=0.5 z.max=3
$  raised base
region    name=4c  silicon y.min=0 y.max=0.12
+         x.min= 2.07 x.max=4.27 z.min=0.5 z.max=3
$  spacer
region    name=4d  oxide y.min=0 y.max=0.12
+         x.min= 3.05 x.max=3.29 z.min=1.43 z.max=2.07
$  emitter
region    name=4e  silicon y.min=0 y.max=0.12
+         x.min= 3.11 x.max=3.23 z.min=1.49 z.max=2.01

$ intrinsic base SIGE
region      name=6a sige     x.min=2.07 x.max=4.27 z.min=0.5 z.max=3
```

```
+                          y.min=0.11 y.max=0.115
+                          x.mol=0 x.end=0.06 y.linear
region      name=6b sige   x.min=2.07 x.max=4.27 z.min=0.5 z.max=3
+                          y.min=0.115 y.max=0.12
+                          x.mol=0.06 x.end=0.06 y.linear
region      name=6c sige   x.min=2.07 x.max=4.27 z.min=0.5 z.max=3
+                          y.min=0.12 y.max=0.13
+                          x.mol=0.06 x.end=0.25 y.linear
region      name=6d sige   x.min=2.07 x.max=4.27 z.min=0.5 z.max=3
+                          y.min=0.13 y.max=0.14
+                          x.mol=0.25 x.end=0.25 y.linear
region      name=6e sige   x.min=2.07 x.max=4.27 z.min=0.5 z.max=3
+                          y.min=0.14 y.max=0.155
+                          x.mol=0.25 x.end=0 y.linear
```

The device is constructed from bottom up. The first layer is the p-substrate below DT and is defined to be silicon as in Fig. 2.7. The second DT layer is first defined to be silicon as in Fig. 2.8; the next REGION redefines the region enclosed by the outer boundary of DT to be oxide as in Fig. 2.9; then the region within DT inner boundary is redefined again as silicon as in Fig. 2.10. The STI layer is first defined to be oxide all over as in Fig. 2.11, then the collector and their contact holes are made by redefinition into silicon as in Fig. 2.12. The EB layer is first oxide as in Fig. 2.13; then intrinsic base (Fig. 2.14) is defined to be silicon as well as the extrinsic base region (Fig. 2.15);

after oxide spacer is placed (Fig. 2.16), the emitter area is redefined to be silicon as in Fig. 2.17. The SiGe intrinsic base is defined according the Ge profile and overwrites the previous defined silicon area.

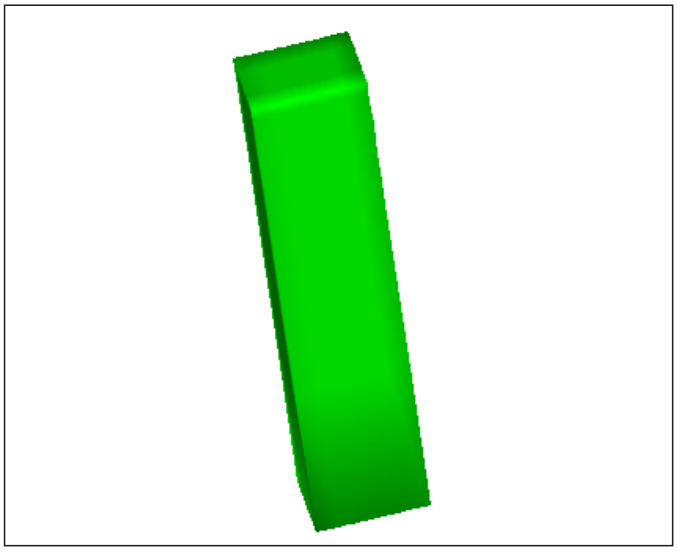


Figure 2.7: The whole structure below deep trench is defined as silicon.

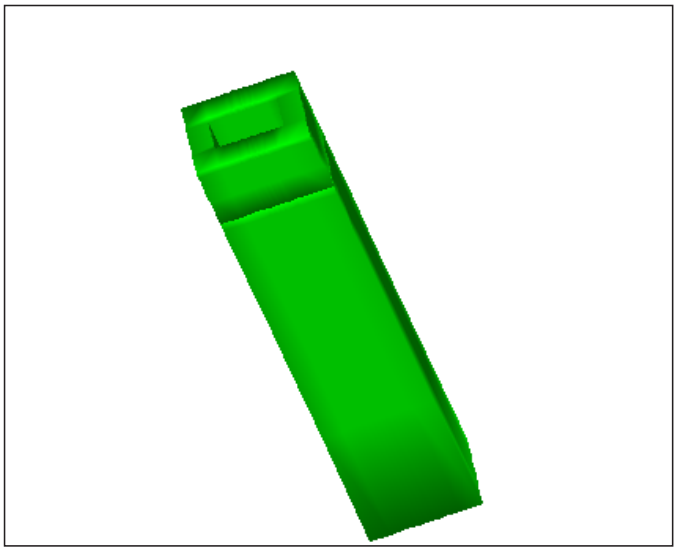


Figure 2.8: The DT layer is defined as silicon.

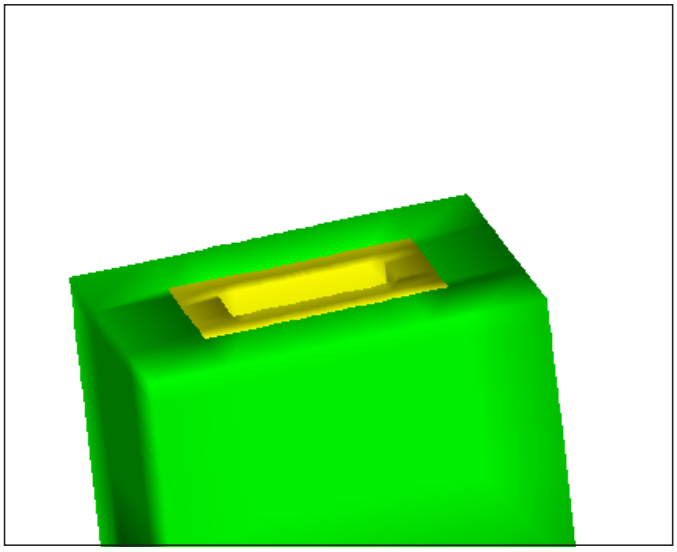


Figure 2.9: The region within outer boundary of DT is defined as oxide.

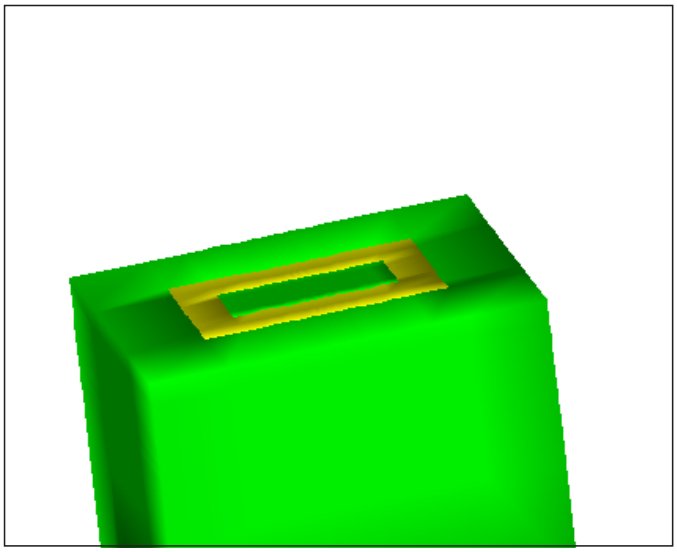


Figure 2.10: The region within inner boundary of DT is overwritten into silicon.

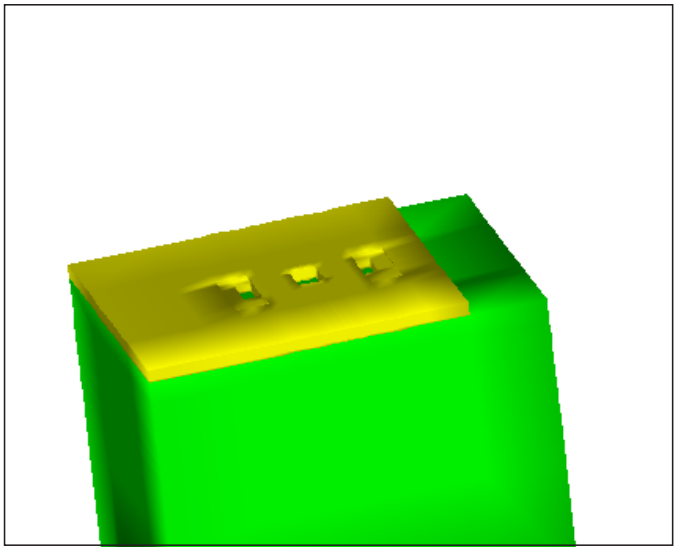


Figure 2.11: The whole region for STI layer is defined as oxide.

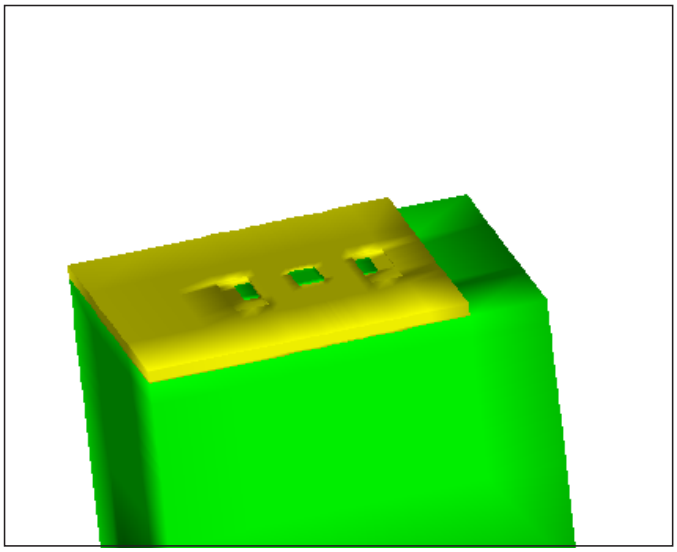


Figure 2.12: The collectors as well as their contact holes are redefined into silicon.

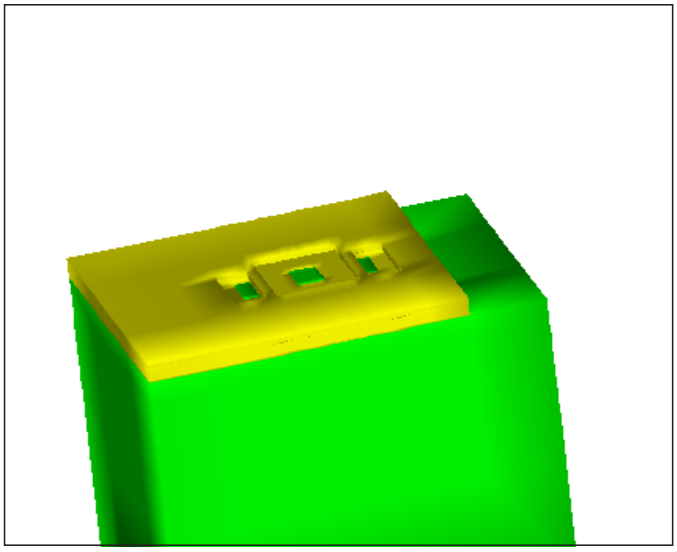


Figure 2.13: The EB layer is defined as oxide overall.

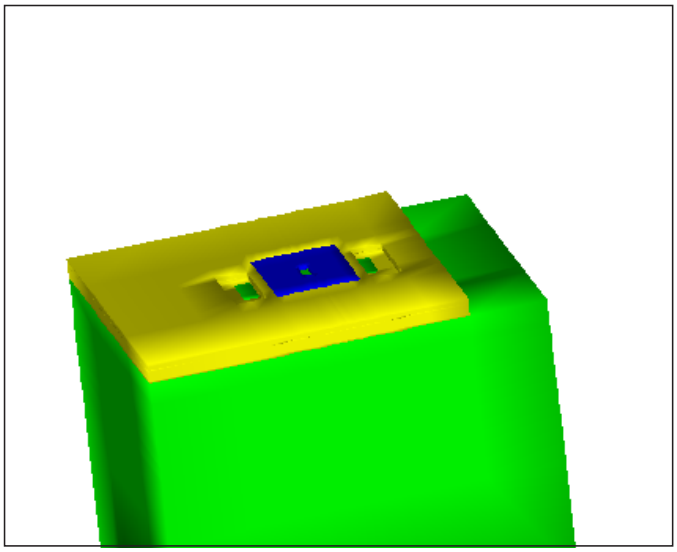


Figure 2.14: The intrinsic base is redefined into silicon.

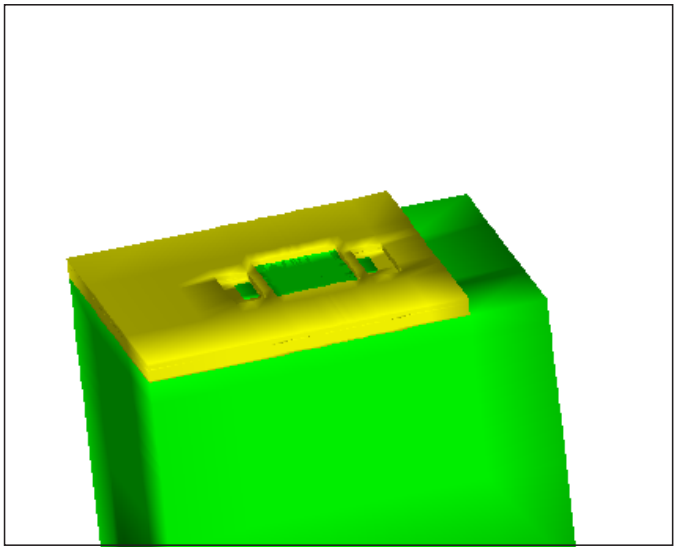


Figure 2.15: The extrinsic base is redefined into silicon.

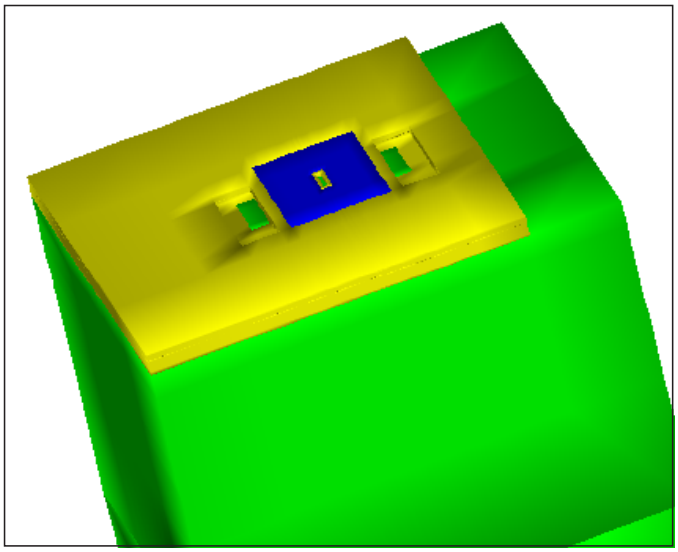


Figure 2.16: The spacer enclosed area is redefined into oxide.

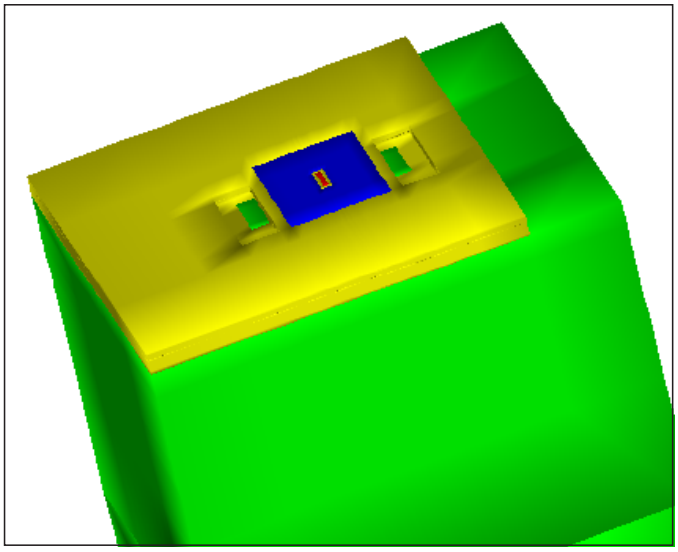


Figure 2.17: The emitter is redefined as silicon.

Contact boxes are used to make contact through oxide without redefining the reachthrough area to metal, which saves extra steps as well. Fig. 2.18 shows the contacts for double collector and Fig. 2.19 is the top contact for substrate on the right. The contacts for base and emitter are invisible in the simulator as they are sheets with no thickness theoretically.

```
electr      name=coll1    x.min=1.0 x.max=1.95  z.min=0.5 z.max=2.5
+                         y.min=0 y.max=0.3
electr      name=coll2    x.min=4.5 x.max=5.5  z.min=0.5 z.max=2.5
+                         y.min=0 y.max=0.3
electr      name=psub     x.min=6.34 x.max=8.34  z.min=-2 z.max=5.5
+                         y.min=0 y.max=0.6
```

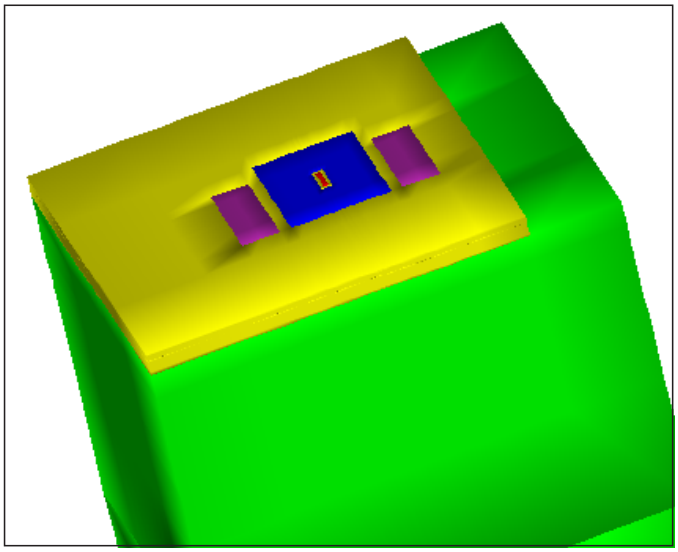


Figure 2.18: Contact boxes for double collectors.

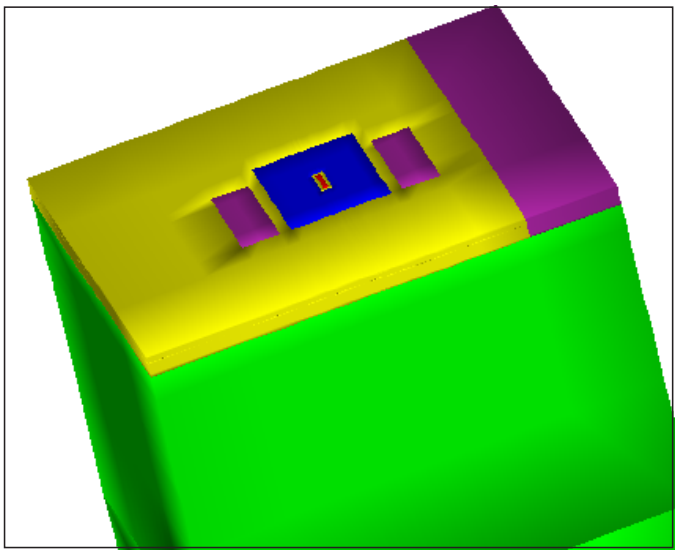


Figure 2.19: Contact box for substrate.

2.3.5 Doping Profile

Uniform doping is used for extrinsic device, while the intrinsic doping is read from the SIMS file as in the following code. X.CHAR is used to define the characteristic length of the profile in the x-direction outside the range X.MIN and X.MAX. Y.CHAR and Z.CHAR play similar roles in y-direction and z-direction, respectively.

```
$ psub 2-8    below ST n+Buried
profile      p-type   n.peak=5e15 y.min=2 y.max=8 y.char=0.0001
+                     x.min=1 x.max=5.34 x.char=0.0001
+                     z.min=1 z.max=2.5 z.char=0.0001
....
profile      1d.ascii in.fil=asBuri.dat y.col=1 n.col=2
+                  y.direct
+                  y.max=3
+                  x.min=1 x.max=5.34 z.min=1 z.max=2.5
+                  x.char=0.0001  z.char=0.0001
....
```

2.3.6 3D and 2D Views of Structure

Fig. 2.20 is the 3D view of the entire device constructed. The red area is emitter and the blue area is the raised extrinsic base region. The emitter is only $0.12 \times 0.52 \mu m^2$, while area enclosed by DT is $4.34 \times 1.5 \mu m^2$. The black line indicates where we do the 2D cut to show the intrinsic portion of the device as is in Fig. 2.21. The device

has a p-type substrate, the p^+ reachthrough outside DT is for top contact of substrate. DT is $8\mu m$ thick, and on top of it sits the STI and intrinsic device. The n^+ buried layer is heavily doped to reduce the collector resistance. The portion of collector right beneath the emitter is a SIC (Selected Implanted Collector). And the rest area within the collector window and surrounding the emitter is lightly doped collector. The heavy doping under the emitter is to reduce the base-widening effect, and the low doping in parasitic-collector is to reduce the total collector-base junction capacitance. An SIC can be easily obtained by selective ion implantation. The raised extrinsic base is heavily doped to reduce base resistance, and the intrinsic base is made of SiGe and its doping is from SIMS file.

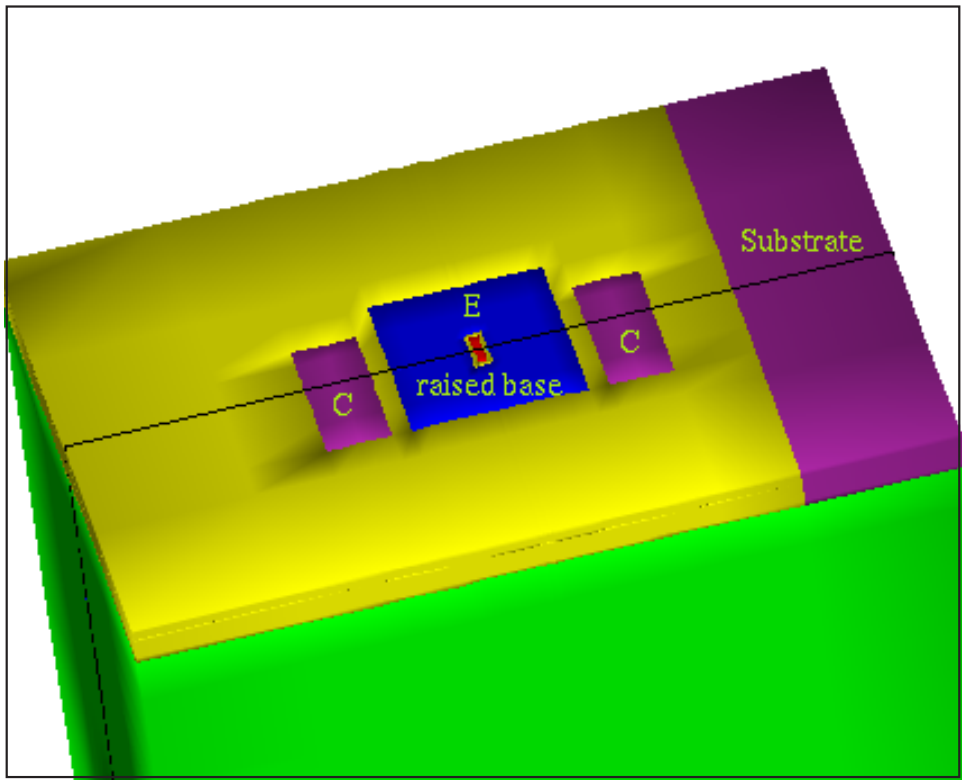


Figure 2.20: 3D view of the entire device. $A_E = 0.12 \times 0.52\mu m^2$, area inside DT = $4.34 \times 1.5\mu m^2$.

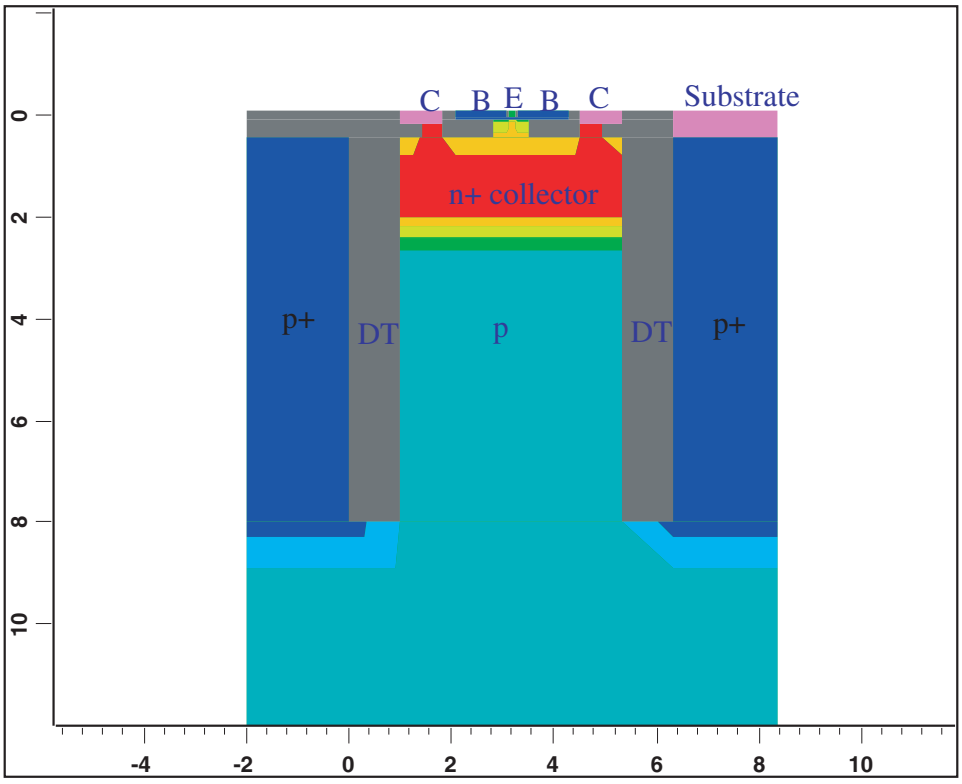


Figure 2.21: 2D view of the intrinsic portion of the device.

2.4 SEU Simulation

The potential ϕ, the electron and hole concentration, n and p, are three basic variables to be solved in device simulations. Due to the rapid change of electron and hole concentration caused by the generated electron-holes, a higher density of grids is needed along the ion track. Grid refinement is hence necessary.

LET is frequently used to describe the Linear Energy Transfer from the incident particle to the target material. Davinci has a photogeneration mode for SEU simulation, in which different LET can be specified for different cases. The terminal current waveforms and the integrated charge collections are two important facts we use to examine SEU in SiGe HBTs.

2.4.1 Ion Track Generation

In Davinci, the generation term which is applied to the continuity equations has the following form:

$$G_n(l,r,t), G_p(l,r,t) = L(t) \cdot R(r) \cdot T(t). \tag{2.6}$$

where l is the distance from the incident point and r is the distance from the track. The time dependent term T(t) can be chosen from four forms and we are using Gaussian:

$$T(t) = \frac{2exp[-(\frac{t-T0}{TC})^2]}{TC\sqrt{\pi}erfc(-\frac{T0}{TC})}. \tag{2.7}$$

where TC is the characteristic time of the generation pulse and T0 is the time offset for the generation pulse, also peak of the time Gaussian [9].

To mimic the worst case deep ion strikes that traverse the entire device through the center, we assumed charge deposition throughout the entire simulated structure. We chose a $0.1 pC/\mu m$ charge deposition, which is equivalent to an LET of $10 MeV/cm^2/mg$ for its relevance to orbital applications. The charge track was generated over a period of 10 picoseconds using a gaussian waveform. The 1/e characteristic time scale is 2 picosecond and the 1/e characteristic radius is 0.2 μm. The peak of the gaussian occurs at 2 picoseconds. The simulator does not support the variation of these constants with LET.

2.4.2 Physical Model Selection

To achieve high accuracy of the simulations to the reality, physical model selection is very important. In our case, the Philips unified mobility model is chosen because it separately models majority and minority carrier mobilities and is appropriate for addressing bipolar devices. The concentration dependent Shockley-Read-Hall recombination, Auger recombination and velocity saturation are included due to the high concentration of electrons and holes as well as high electric fields. Bandgap narrowing is taken into account too.

2.5 Summary

In this chapter, we explained the necessity of full 3D device simulation for SEU simulation and compared the pros and cons of every modeling methodology. We detailed the 3D device simulation process for 200 GHz SiGe HBTs, step by step. In the

following chapters, we will investigate on SEU-induced charge collection characteristics in the state-of-art SiGe HBTs.

CHAPTER 3

CHARGE COLLECTION CHARACTERISTICS

After the ion strikes the device, charges generated along the particle track can locally collapse the junction electric field due to the highly conductive nature of the charge track and separation of charges by the depletion region field. While electrons and holes drift or diffuse under the influence of electric field or concentration gradient, the terminals see transient currents and collects charges.

3.1 Substrate Thickness Selection

To mimic worst case deep ion strikes that traverse the entire device, we have assumed charge deposition throughout the whole simulated structure. Initial simulations were performed on simple diode with a 50μm thick structure and a 100μm thick structure, and no difference was observed in charge collection as in Fig. 3.1 or terminal transient current as in Fig. 3.2.

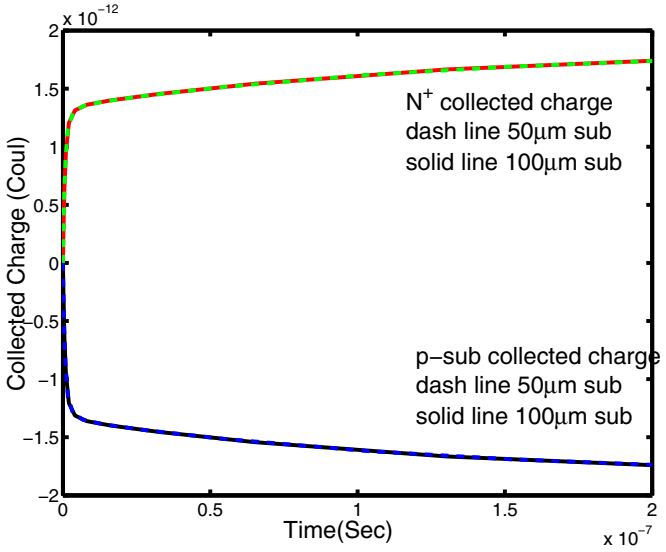


Figure 3.1: Charge collected by the terminals as a function of time for different substrate thickness.

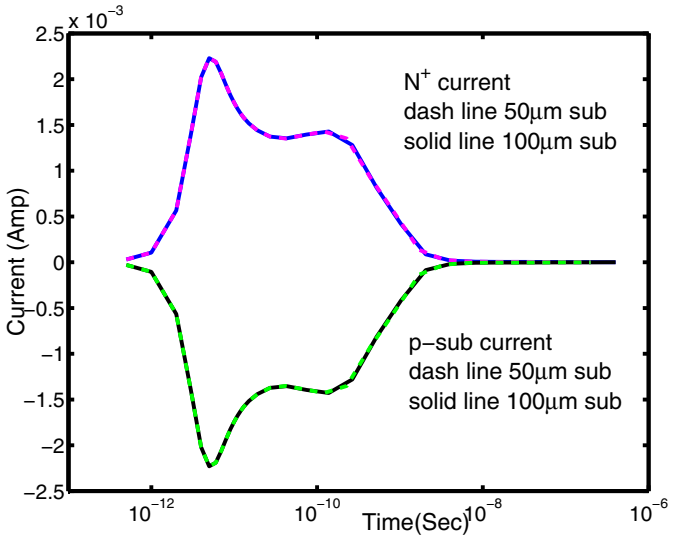


Figure 3.2: Transient terminal currents as a function of time for different substrate thickness.

3.2 Charge Collection Characteristics

The substrate was biased at -5V and all other terminals were grounded. This represents the worst bias situation in a SiGe HBT digital circuit. Each transient simulation was performed until the current decayed to zero. For full 3-D device simulation using Davinci, one transient simulation takes only a couple of hours on a dedicated Sun Blade 2000 workstation with 1.8GB memory, much more efficient than Dessis.

We chose a $0.1pC/\mu m$ charge deposition, which is equivalent to an LET of 10 MeV/cm^2/mg for its relevance to orbital applications. The charge track was generated over a period of 10 picoseconds using a gaussian waveform. The 1/e characteristic time scale is 2 picosecond and the 1/e characteristic radius is 0.2 μm. The peak of the gaussian occurs at 2 picoseconds.

Fig. 3.3 shows the transient terminal currents as a function of time. Fig. 3.4 shows the charges collected by individual terminals as a function of time. Most of hole charge collection occurs through the p-type substrate terminal. The base collects a small amount of hole charge. Most of electron charge collection occurs through the collector terminal. The emitter collects a small amount of electron charge.

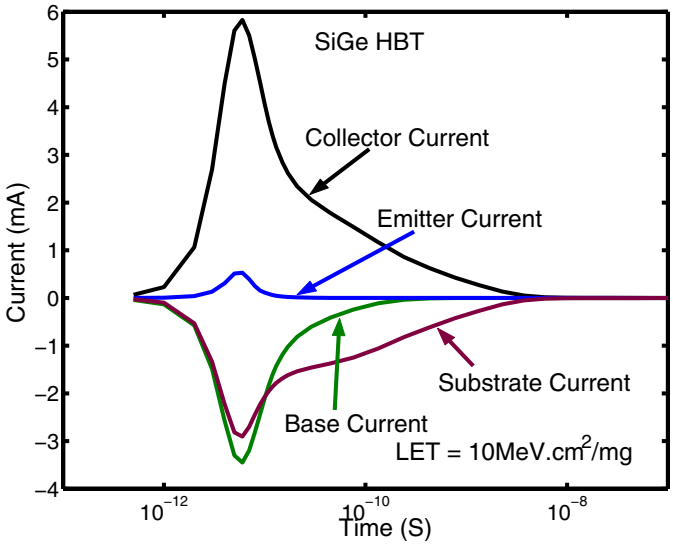


Figure 3.3: Transient terminal currents as a function of time. LET= $0.1 pC/\mu m$

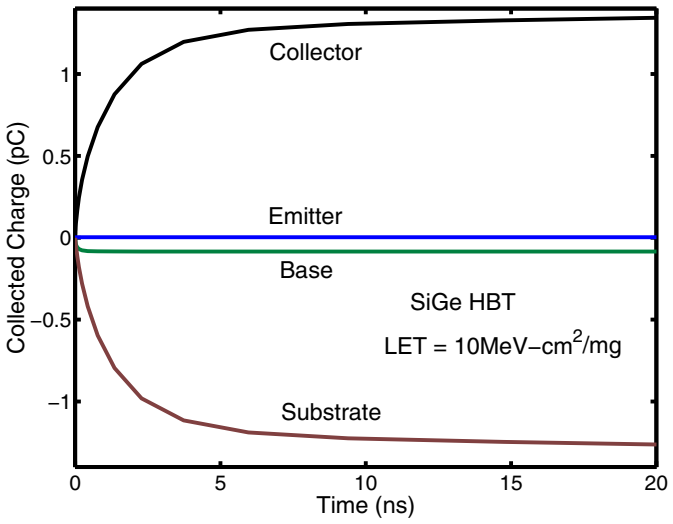


Figure 3.4: Charge collected by the terminals as a function of time. LET= $0.1 pC/\mu m$.

3.3 Internal Device Behavior

A funneling behavior is evident by examining the potential contours in the series of plots from Fig. 3.5 to Fig. 3.11. Before the ion strikes, the equipotentials are parallel to the junction. At 1.0 psec (Fig. 3.5), the equipotentials begin to extend into the substrate due to the voltage drop along the charge column. The funneling reaches its peak at 4.0 psec (Fig. 3.6). At 10.0 psec the funnel starts to collapse, and the drift current starts to decrease as charge is swept from the depletion region. At 10.0 nsec, the depletion region is effectively restored and only diffusion charge collection is occurring.

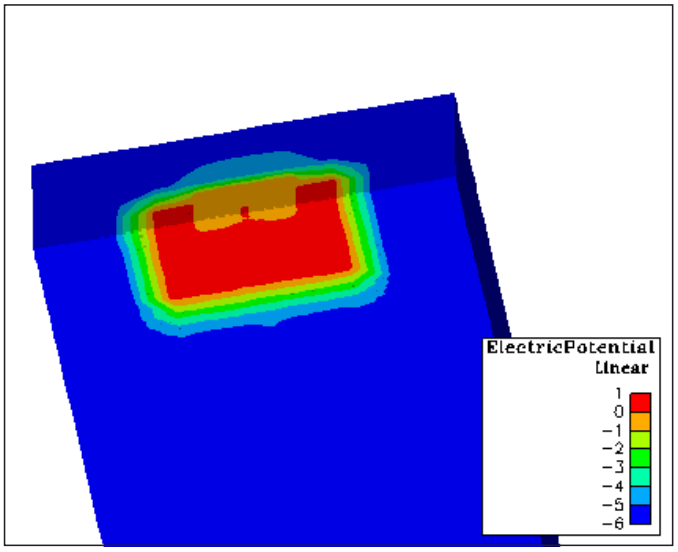


Figure 3.5: Electrostatic potential of 1 psec after an ion strike.

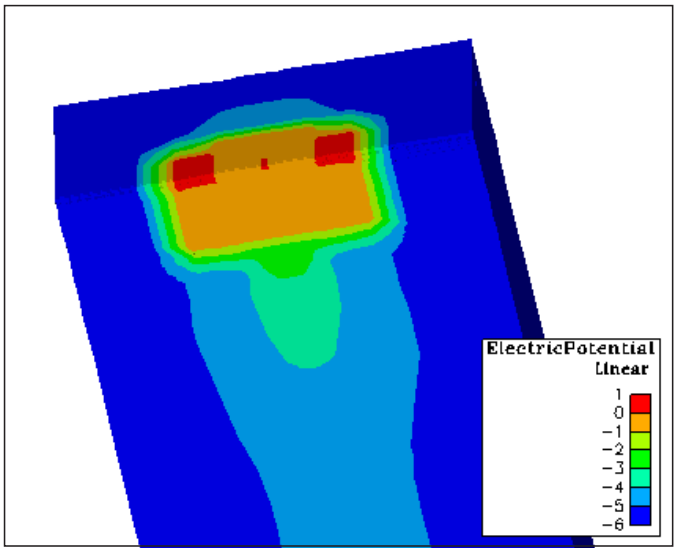


Figure 3.6: Electrostatic potential of 4 psec after an ion strike.

3.4 Summary

In this chapter simulation substrate thickness is carefully chosen, and the charge collection characteristics are presented in the state-of-art 200 GHz SiGe HBT. Internal device behavior gives much insight into the transient physical phenomena after an ion strike.

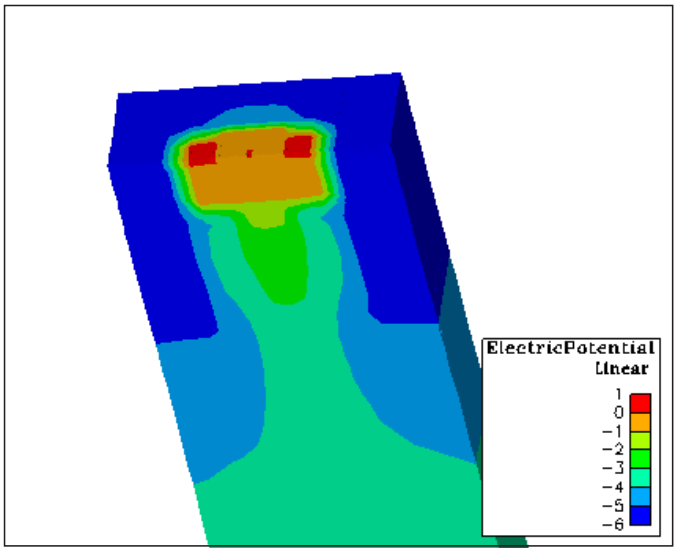


Figure 3.7: Electrostatic potential of 8 psec after an ion strike.

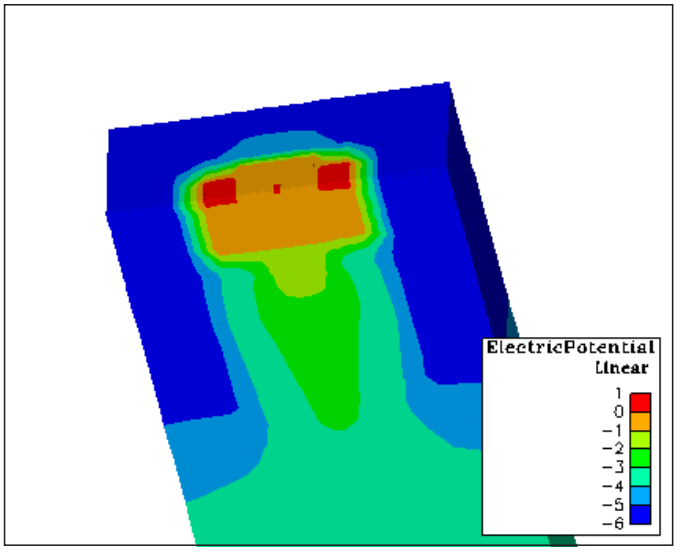


Figure 3.8: Electrostatic potential of 10 psec after an ion strike.

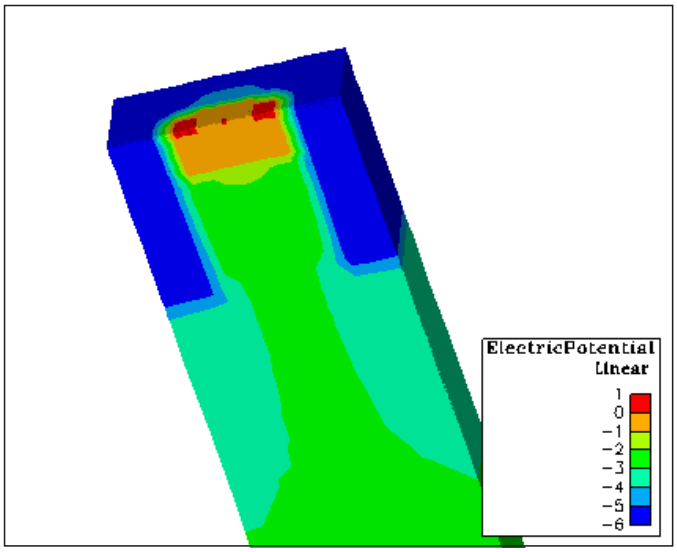


Figure 3.9: Electrostatic potential of 100 psec after an ion strike.

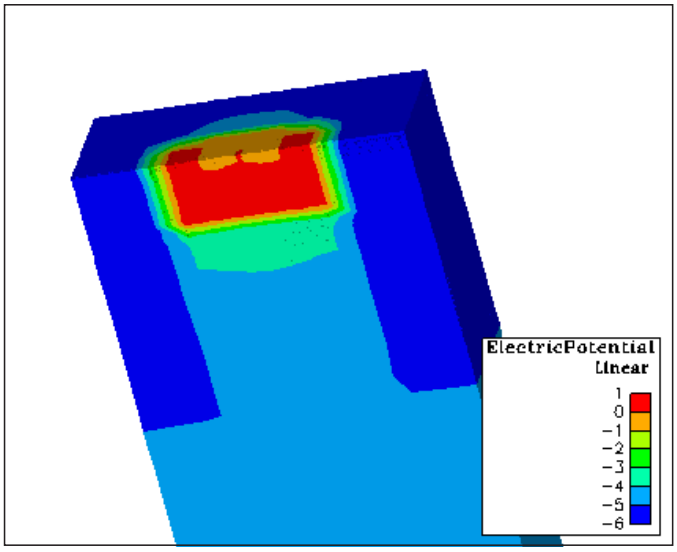


Figure 3.10: Electrostatic potential of 1 nsec after an ion strike.

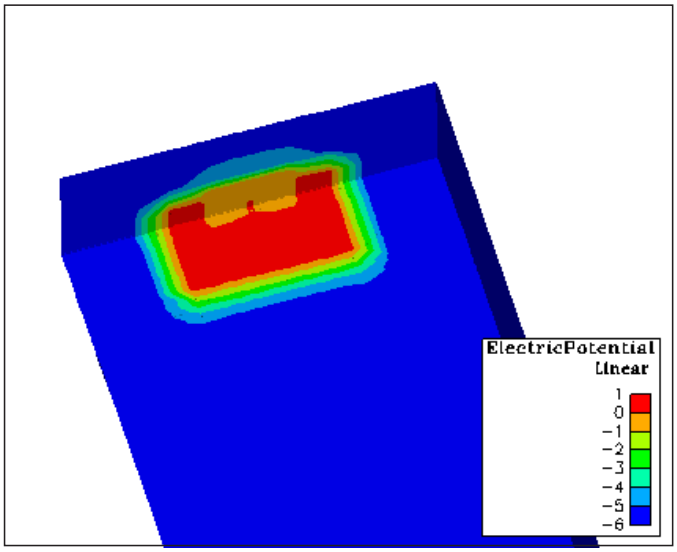


Figure 3.11: Electrostatic potential of 10 nsec after an ion strike.

CHAPTER 4

CHARGE COLLECTION SENSITIVE VOLUME

If all the cells in an IC memory were physically and electronically identical, the curve of SEU cross section (σ) versus LET_{eff} would consist of a step function at the threshold linear energy transfer (LET_{th}), with a constant σ for increasing LET_{eff}>LET_{th} as in Fig. 4.1 [15]. The step at LET_{th} would correspond to the critical charge. However, it is well known that the experimentally determined σ is a convex downward curve with a critical threshold LET as seen in the preceding figure. Also, an asymptotic value of σ can be discerned in the limit of large LET_{eff}. One reason for the actual behavior of σ is that memory cells are not identical due to manufacturing vagaries-some are more sensitive than others. Thus individual cells can upset over a range of LET_{eff} about a threshold LET [16]. Sensitive region/volume is useful in calculating cross section and hence the probability of an SEE.

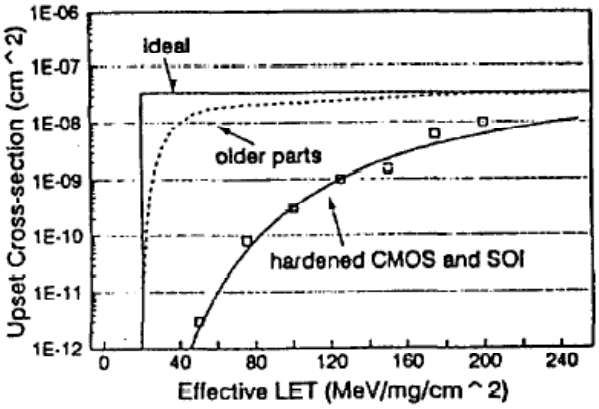


Figure 4.1: Representative SEU cross sections. The step function depicts the ideal where all IC memory cells are identical. Source: [15].

4.1 Sensitive Regions Identification

The charge collections by each terminal of a given device is highly dependent on the location of the ion strike. There are certain sensitive regions within which the charge collection is appreciable for a certain terminal, while negligible charges are observed outside such regions. Hence sensitive regions are identified based on the analysis of the device structure and simulation results of different ion strike locations.

Because the 3D device simulation is time consuming, it is not feasible to simulate all the possible representative incident locations. Hence, the ion tracks are placed within the critical cross section we shown over and over again earlier. Fig. 4.2 shows the positions of different ion tracks; the center strike is within the shallow trench isolation, there is one between deep trench and shallow trench isolation, the rest are all outside of the deep trenches.

From Fig. 4.3, the charges collected by the base, collector and substrate are a strong function of ion track positions, while emitter always collects negligible charges. For collector and substrate terminals, deep trench marks the edge for drastic charge collection change, outside which, the collected charges decreased dramatically, hence the area enclosed by deep trench is determined to be the sensitive area for collector and substrate charge collection as shown in Fig. 4.4. However, shallow trench isolation plays the similar role for base as DT for collector and substrate, and therefore, the shallow trench isolation enclose the sensitive area for base charge collection as indicated in Fig. 4.5. The 3D views of both sensitive regions are indicated in Fig. 4.6.

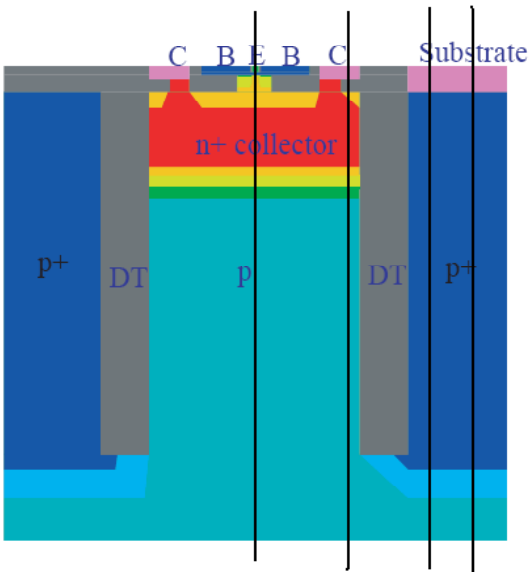


Figure 4.2: Different ion track positions.

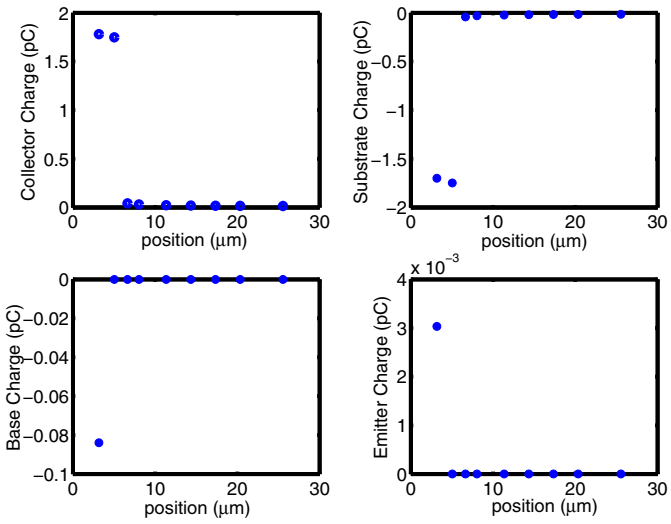


Figure 4.3: Charge collected by the terminals as a function of ion track position. "Fat device".

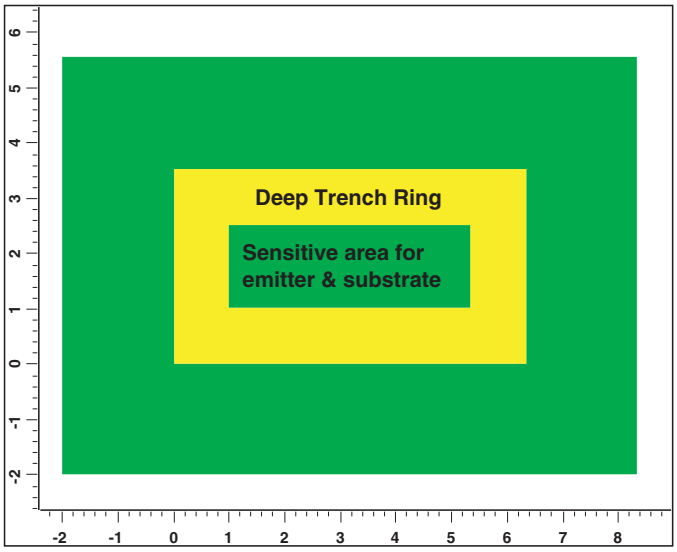


Figure 4.4: 2D view of SEU sensitive area for collector and substrate charge collection.

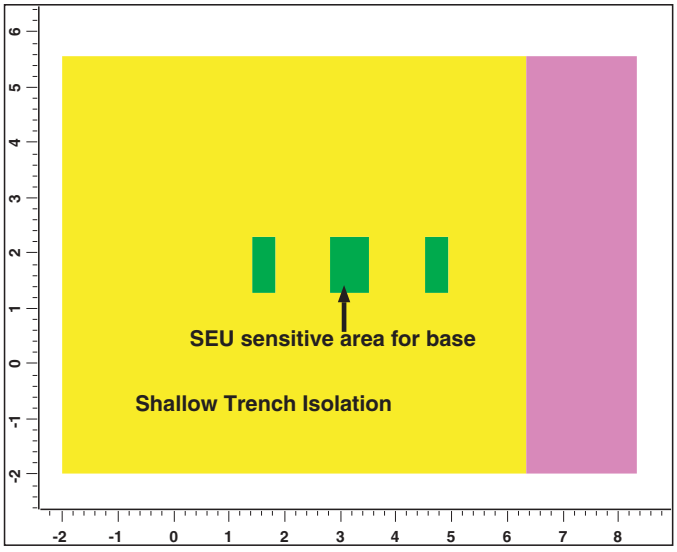


Figure 4.5: 2D view of SEU sensitive area for base charge collection.

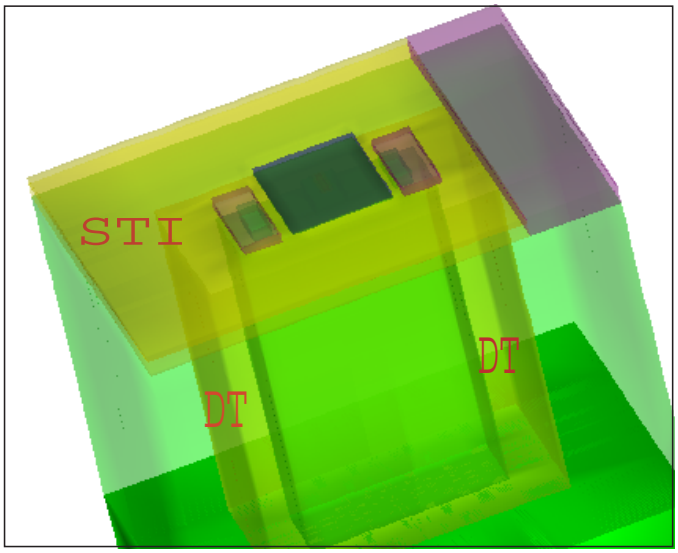


Figure 4.6: 3D view of SEU sensitive areas.

4.2 Structure Domain Selection

Note that the device is "fatter" than in the previous chapters. It is because for ion strike outside DT, the charge would be reflected by the limited boundary and be collected by the terminal, hence produce unrealistic charge collection as in Fig. 4.7. In reality, the spacing between devices are large enough for the charge to decay and not "reflected"; to save time in simulation, we extend the spacing to larger than the range of the incident particle.

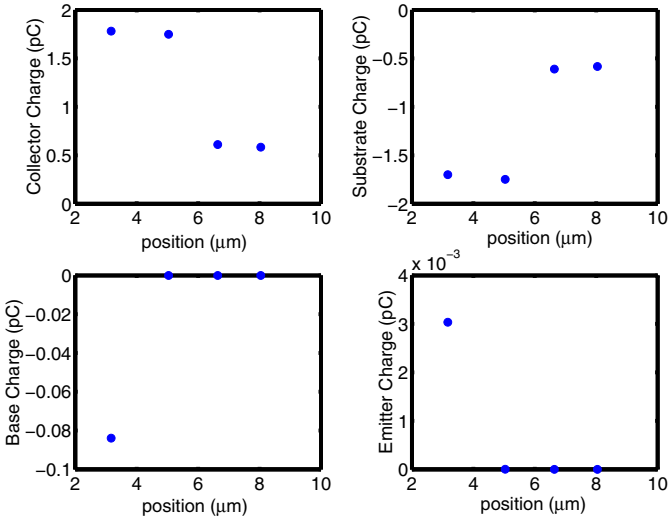


Figure 4.7: Charge collected by the terminals as a function of ion track position. "Thin device".

4.3 Summary

We identified the sensitive region for each terminal in the state-of-art 200 GHz SiGe HBT. The structure domain selection issue was also discussed for accurate device simulations.

CHAPTER 5

ANGLE STRIKE DEPENDENCE

As we mentioned earlier, a parallelpiped particles incident at an angle θ will have a path that is $1/\cos(\theta)$, which is longer than the path at normal incidence, thus producing more ionization charge under the assumption that only charges deposited in the cube are collected. This assumption does not hold for SiGe HBTs as we will investigate below. Based on careful investigations on several representative angle strike results, we propose a new junction passing / DT confinement model.

5.1 Angle Strike Path Selection

For angle strike, charge collection depends on the existence of junction (drift) along ion path or ion path being close to a collection junction (diffusion), or both. In Fig. 5.1, the white lines indicate the n^+ buried layer to p-substrate (C/S) junction and the collector/base (C/B) junction. The C/B junction is much shorter than the C/S junction. If the angle strike path does not go through any junctions, it traverses either the n^+ buried layer, or the lightly doped p-substrate layer. We expect little charge collection from the path confined within DT and n^+ buried layer, because the heavy doping means short life time, high recombination rate, hence little diffusion. However, diffusion will cause some charge collection when the path is through lightly doped p-substrate where life time is high. If the angle strike path goes through C/S junction, then drift will cause major charge collection.

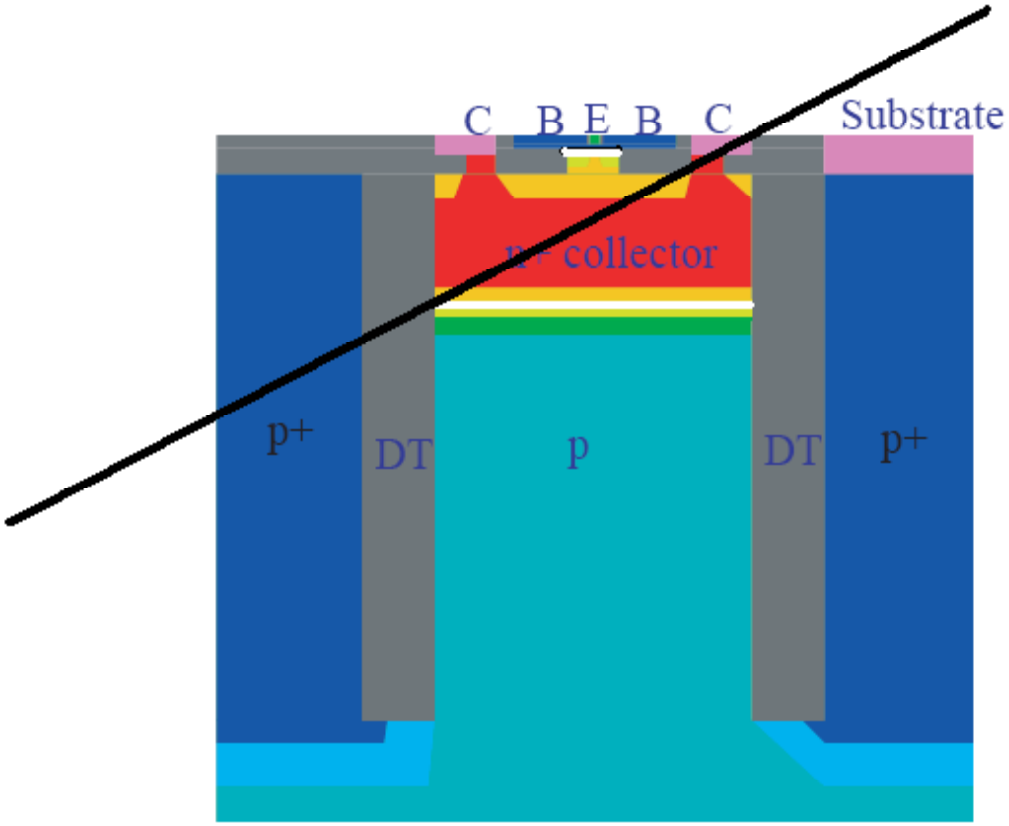


Figure 5.1: Graphic illustration of angle strike.

We carefully choose 6 representative angle strike paths as in Fig. 5.2. They intersect the C/S or C/B junction differently and have different length within DT. Path 1, 2, 3, 4 are all in parallel.

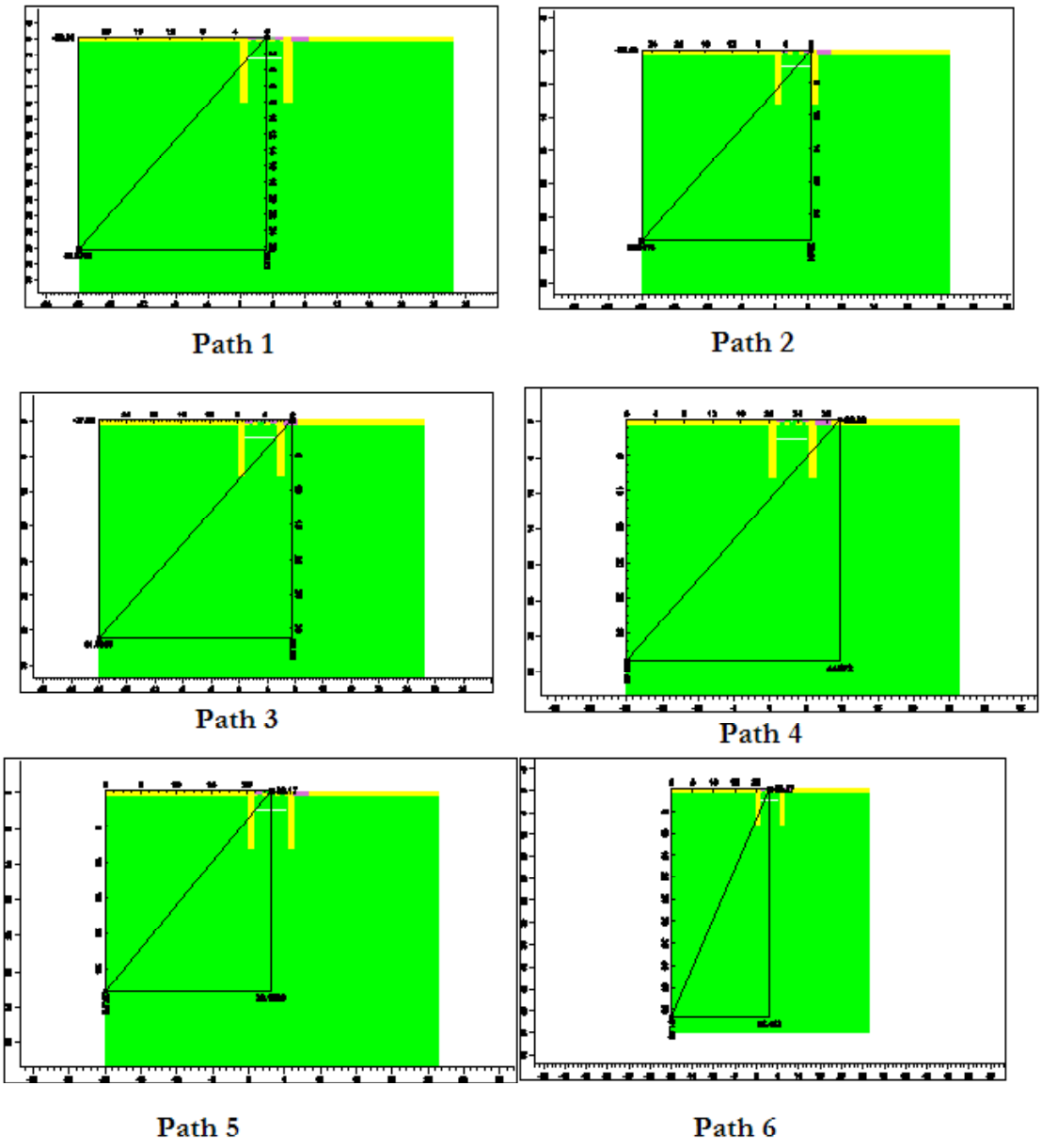
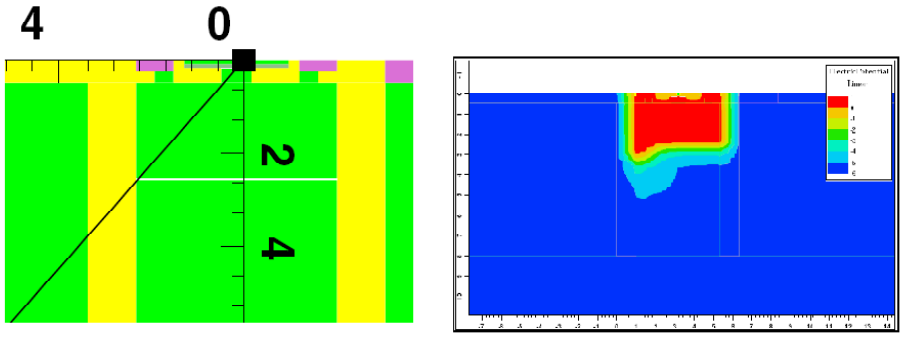


Figure 5.2: 6 representative angle strike paths under investigation.

5.2 Results Analysis

Path one passes the edge of collector/substrate (C/S) junction as in Fig. 5.3. The path length within DT is 3.478 μm, with 0.1 pc/μm deposition, the total charge deposited within DT should be 0.34 pC. However only 0.17 pC is collected due to the small intersection with C/S junction. Most of the charges generated are recombined within the heavily doped buried layer where life time is low. As seen from the potential contour at 4 psec, the potential funneling happened mostly on the lightly doped p-substrate side.

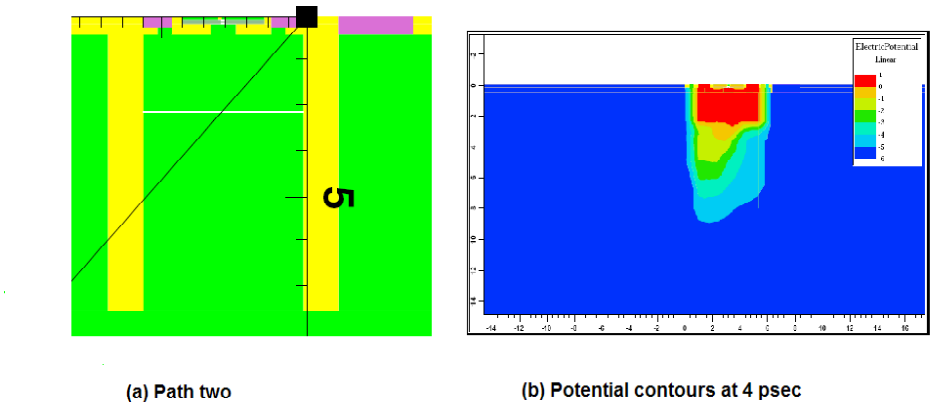


(a) Path one

(b) Potential contours at 4 psec

Figure 5.3: Path one.

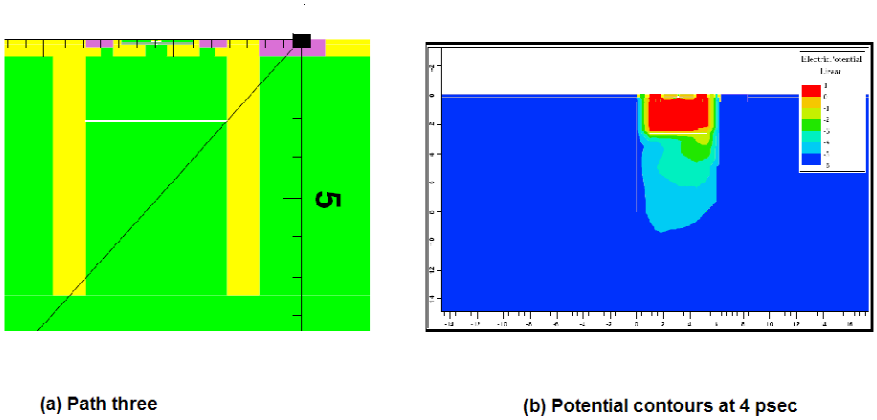
Path two intersects the center of C/S junction as in Fig. 5.4 and is in parallel with path one. The path length within DT is 6.53 μm; the portion in p-sub is 3.26 μm, hence the total charge deposited within DT should be 0.326 pC. However 0.78 pC is collected which is more than the deposited charges. This amount can be explained to come of diffusion from charge deposited outside DT.



(a) Path two (b) Potential contours at 4 psec

Figure 5.4: Path two.

Path three has the largest intersection with C/S junction as in Fig. 5.5 and is in parallel with path one and two. The path length within DT is 5.36 μm, hence the total charge deposited within DT is 0.536 pC. Ion path is not interrupted by the left DT much, leading to 1.29 pC charge collection, of which a large amount is diffusion from charge deposited outside DT.

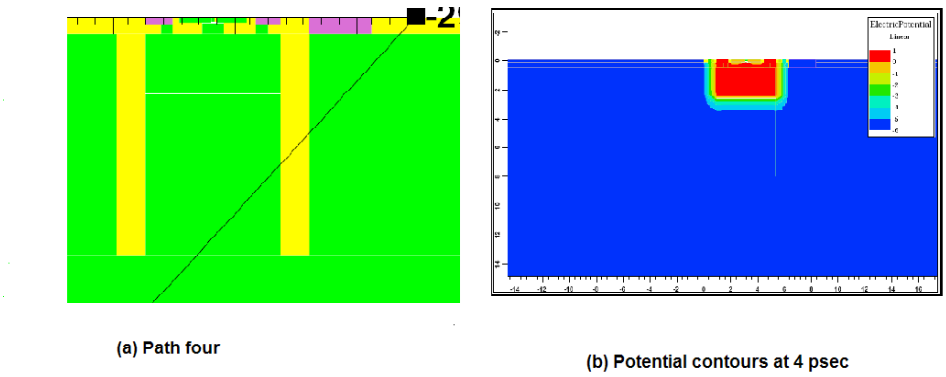


(a) Path three

(b) Potential contours at 4 psec

Figure 5.5: Path three.

Path four has no intersection with C/S junction as in Fig. 5.6 and is in parallel with path one two and three. The path length within DT is 6.5 μm, hence the total charge deposited within DT should be 0.65 pC. A total of 0.7 pC charge collection is seen. The potential contours show no funneling effects at all, indicating diffusion as the main charge collection mechanism in this case.

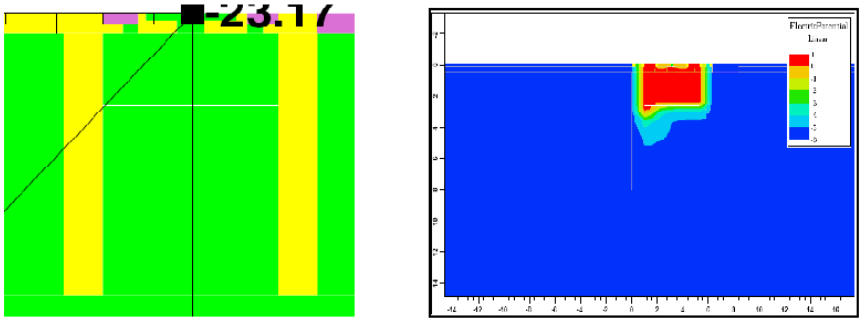


(a) Path four

(b) Potential contours at 4 psec

Figure 5.6: Path four.

Path five passes the E/B junction but barely intersects with C/S junction as in Fig. 5.7. The path length within DT is 3.38 μm, hence the total charge deposited within DT is 0.338 pC. A total of 0.15 pC charge collection is seen, which can be explained by the similar reason of path one.

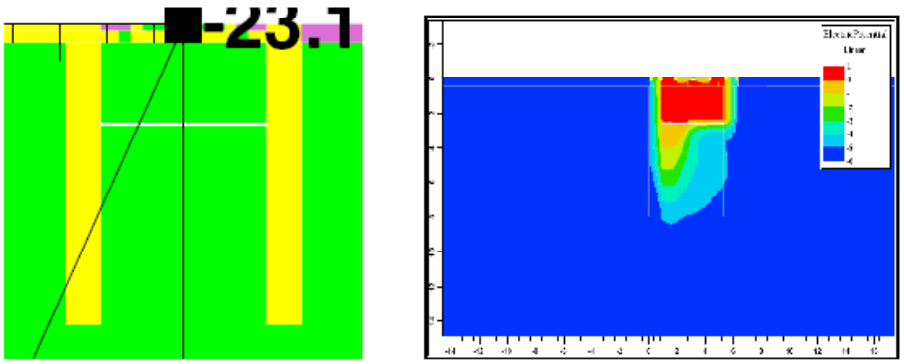


(a) Path five.

(b) Potential contours at 4 psec

Figure 5.7: Path five.

Path six intersects with C/S junction on both sides as in Fig. 5.8. The path length within DT is 5.2 μm, with 2.6 μm in lightly doped p substrate, hence the total charge deposited within DT is 0.26 pC. A total of 0.78 pC charge collection is seen. The extra charge comes from diffusion.



(a) Path six

(b) Potential contours at 4 psec

Figure 5.8: Path six.

The results are summarized in Table 5.1.

Table 5.1: Simulation results for angle strike dependence

Angle Strike Path	Collector Charge	Charge Deposited within DT
1	0.171	0.348
2	0.781	0.326
3	1.292	0.537
4	0.716	0.655
5	0.156	0.339
6	0.776	0.260

5.3 Junction Passing / DT Confinement Model

Simulations of carefully chosen angle strike paths supports the new junction passing / DT confinement model. Diffusion is the only mechanism for charges along path inside DT that does intersect with any junction. Charges deposited outside DT only get collected via slow diffusion in the lightly-doped p-substrate where lifetime is high. While the charge deposited above the N+ buried layer / p-substrate junction is recombined quickly within the n^+ buried layer where life time is low, leaving little diffusion charge collection. Overall angle strikes actually produce less charge collection than normal strike, which is contrary to conventional model .

5.4 Summary

In this chapter, carefully selected angle strike results analysis defied the conventional parallelpiped-shaped model. We have proposed a new junction passing / DT confinement model instead, which well explained the phenomena we observed.

CHAPTER 6

BACK JUNCTION APPROACH FOR REDUCING CHARGE COLLECTION

Single event upset is of concern in high-speed SiGe HBTs, because of the existence of the n^+ buried layer to p-substrate junction. A natural approach to mitigate the SEU problem is to fabricate the SiGe HBT on an SOI substrate, thus eliminating the n^+ buried layer to p-substrate junction. A practical problem with the SOI SiGe HBT is compatibility with SOI CMOS processes, however, which often use a very thin silicon film, making collector resistance high. Recently, the buried oxide was etched away to form a low resistance n+ collector in the p-substrate underneath the buried oxide in a SiGe technology [18]. This SOI approach, however, makes the SiGe HBT on SOI equivalent to a bulk SiGe HBT from a charge collection standpoint.

We propose a new back junction approach to reduce charge collection in SiGe HBTs and demonstrate its effectiveness in 200 GHz SiGe HBTs using full 3D device simulation. The basic idea is to add another n^+ layer below the p-type substrate to form a *back* pn junction, as detailed shortly. This back junction structure is designed to reduce charge collection in several ways. First, the total amount of charge that can be collected is now limited by the thickness of the p-layer. Second, the charge deposited in the p-layer will be collected by both the normal n^+ buried layer to p-layer junction and the added back junction, further reducing charge collection by the sensitive transistor collector node. In addition, the path of diffusion from substrate towards the collector in the conventional SiGe HBT is cut off by the back junction.

6.1 Back Junction Structure

The effectiveness of the back junction approach to reduce charge collection is demonstrated by comparisons between the back junction and the conventional SiGe HBT discussed in the previous chapter. Figs. 2.20 and 2.21 show the 3D, 2D cross section views for the conventional SiGe HBT, respectively. This conventional 200 GHz SiGe HBT features a raised extrinsic base to reduce base resistance and collector-base capacitance. This SiGe HBT has a lightly doped p-type substrate, an n^+ buried layer for reducing collector resistance, a selectively implanted collector, epitaxial intrinsic and raised extrinsic base, a polysilicon emitter, and shallow and deep trench isolation.

Fig. 6.1 shows the 3D structure of the back junction SiGe HBT, with the black line in the center indicating where we do the cut to obtain the 2D cross section in Fig 6.2. Both the two SiGe HBT have active emitter areas of $0.12\times0.52\ \mu m^2$, which is only a very small portion of the total silicon area enclosed by deep trench ($1.5\times4.34\ \mu m^2$). Double base and collector contacts are used to realize high speed for this technology represented by the conventional SiGe HBT. For the back junction SiGe HBT, the contact to the n^+ layer of the back junction is made from the top on the left side, and the contact to the p-layer of the back junction is made from the top on the right side. The n^+ layer of the back junction is termed as n^+ sinker, which is $2\mu m$ wide originally; we will refer to its terminal as "back junction" thereafter. We will continue to refer to the p-layer as "substrate" for consistency with notations in the regular HBT. The p-layer is 8 μ m thick. The supporting substrate below the p-layer is assumed to be n^+ for simplicity in simulation. For reducing collector charge collection, this n^+ layer only needs to be

a few microns thick, similar to the n^+ collector buried layer, sitting on top of a p-type supporting substrate.

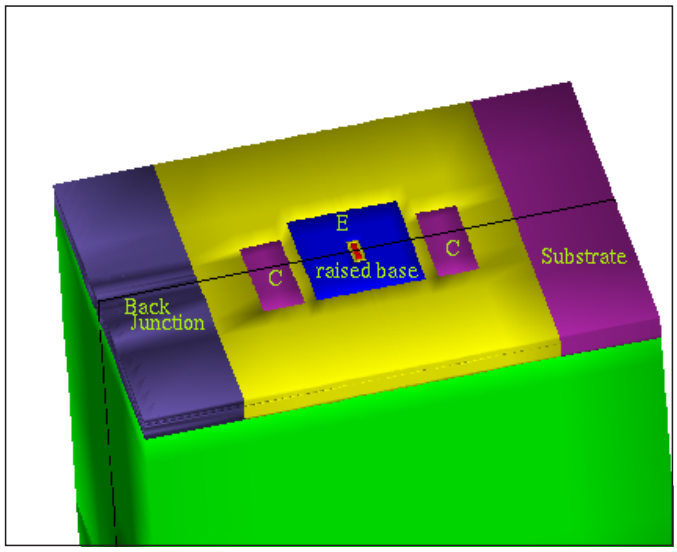


Figure 6.1: 3D structure of the back junction SiGe HBT. $A_E = 0.12 \times 0.52\mu m^2$, area inside DT = $4.34 \times 1.5\mu m^2$.

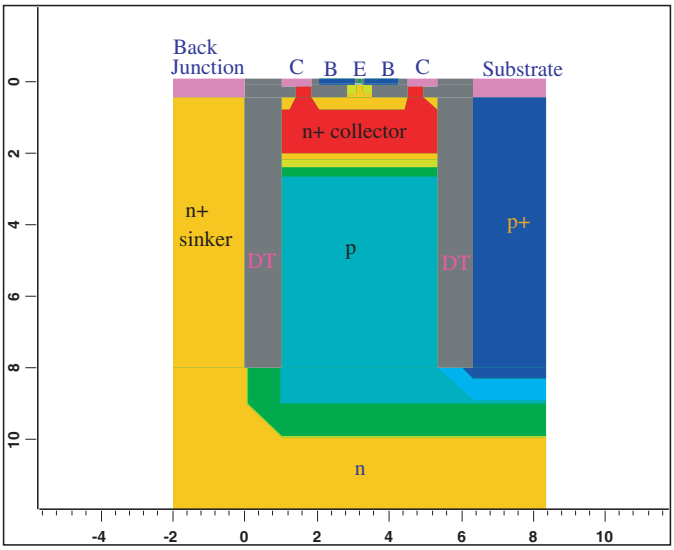


Figure 6.2: 2D cross section of the back junction SiGe HBT. 2μm wide n^+ sinker, 8μm thick p-layer.

6.2 SEU Device Simulation

The 3D device simulation is done in a similar way as for the conventional SiGe HBT in previous chapter. We chose a 0.1pC/μm charge deposition, which is equivalent to an LET of 10 MeV-cm^2/mg for its relevance to orbital applications. The charge track was generated over a period of 10 psec using a Gaussian waveform. The 1/e characteristic time scale is 2 psec and the 1/e characteristic radius is 0.2μm. The peak of the Gaussian occurs at 4 psec.

An ion strike through the center of the emitter is assumed and fine gridding is placed around the charge track. The physics simulated includes concentration dependent Shockley-Read-Hall recombination, Auger recombination, the Philips unified mobility model. Unless specified, the p-type "substrate" contact was biased at V_{EE} = -5 V, and all the other terminals were grounded, which represented a worst bias condition in a SiGe HBT digital circuit. Each transient simulation was performed until the current decayed to zero. Initially, a very long time period was specified to make sure it was long enough to simulate the whole transient process; frequent check of the instant transient current determined whether or not the simulation was complete, hence saving time and memory usage.

6.2.1 Charge Collection Characteristics

Fig. 6.3 shows the transient terminal currents as a function of time for the back junction SiGe HBT, and Fig. 6.4 shows the charges collected by individual terminals as

a function of time. Figs. 6.5 and 6.6 of the conventional SiGe HBT are presented here for comparisons .

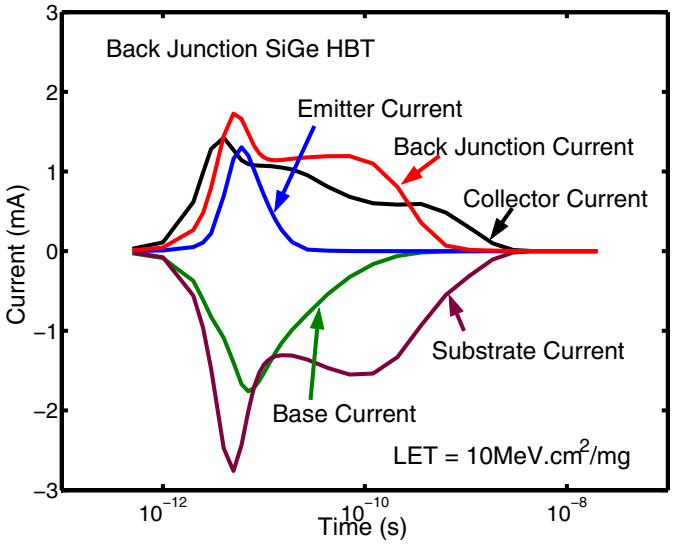


Figure 6.3: Transient terminal currents as a function of time. The p-layer of the back junction is 8 μm thick.

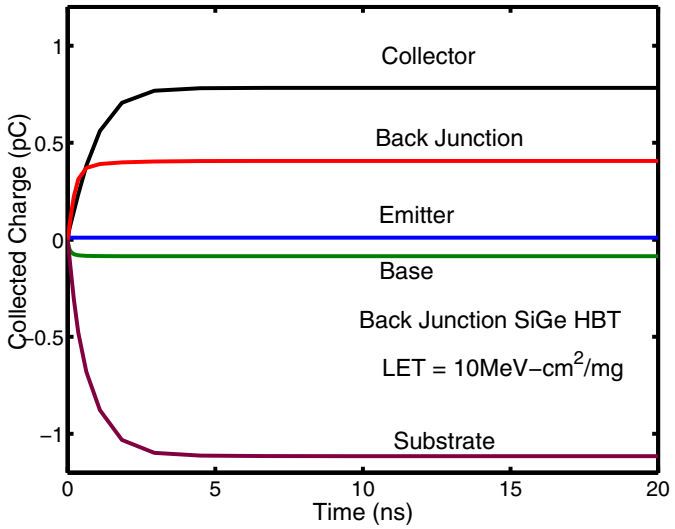


Figure 6.4: Charge collected by the terminals as a function of time. The p-layer of the back junction is 8 μm thick.

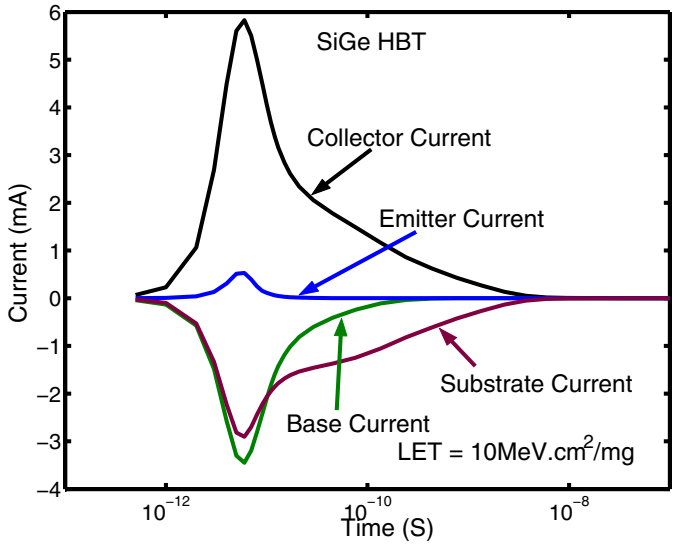


Figure 6.5: Transient terminal currents as a function of time for conventional SiGe HBT.

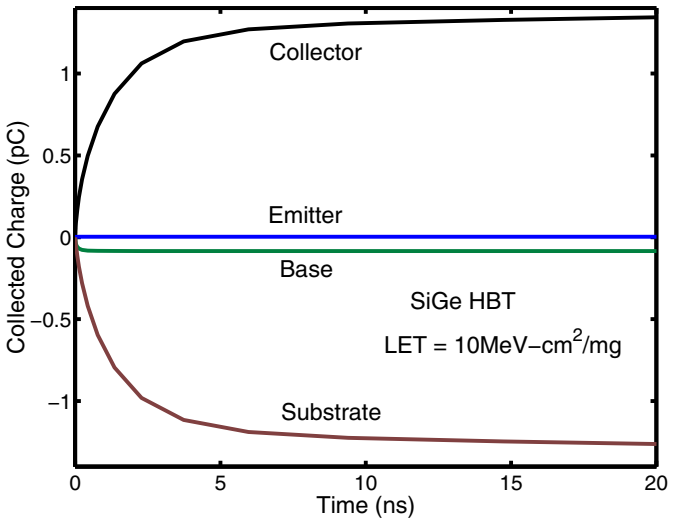


Figure 6.6: Charge collected by the terminals as a function of time for conventional SiGe HBT.

Observe Fig. 6.5 and Fig. 6.3, the peak of collector transient current decreased from near 6mA to round 1.5mA, a reduction of more than 75%, due to the diffluence of the back junction, which sees a peak current of near 2mA. As seen from Figs. 6.6 and 6.4, for back junction, most of hole charge collection occurs through the p-type substrate terminal. The base collects a small amount of hole charge. The emitter collects a small amount of electron charge. The collector collects 0.8 pC electron charge, while the back junction collects 0.4 pC electron charge. The total positive charge collected in the back junction SiGe HBT is also less than the conventional SiGe HBT.

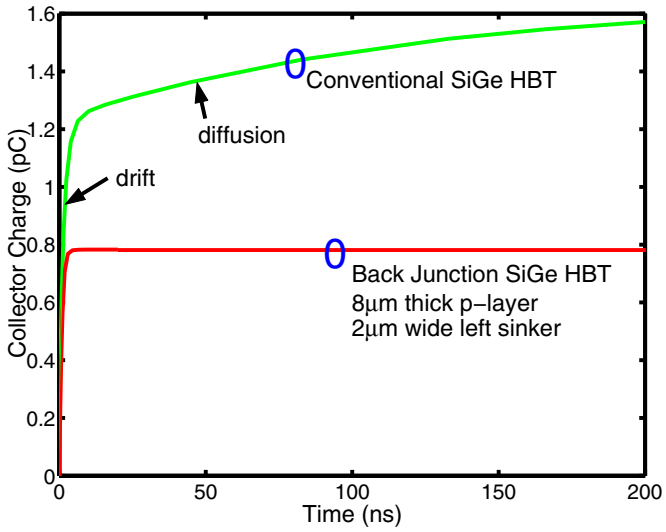


Figure 6.7: Comparison of collector charge collection in the back junction SiGe HBT and the conventional SiGe HBT. The p-layer of the back junction is 8μm thick.

Comparison of collector charge collection is shown in Fig. 6.7, a reduction of collector charges from 1.6 pC in the conventional SiGe HBT to 0.8 pC in the back junction SiGe HBT is clear. The charge collection in back junction is complete within 2 ns, and

is mostly due to drift. While in the regular HBT, charge collection takes much longer time, because of the diffusion charge collection within the lightly doped substrate. In the back junction HBT, charge collection primarily occurs within the p-layer. The potential funneling in the collector n^+ to p-substrate junction now interacts with the potential funneling in the back junction, thus speeding up the overall charge collection. This should produce an obvious advantage for SEU. A comparison of the potential contours at 4 psec between the back junction and conventional SiGe HBTs is given in Fig: 6.8. This time instant corresponds to the peak of the Gaussian waveform for electron-hole pair generation.

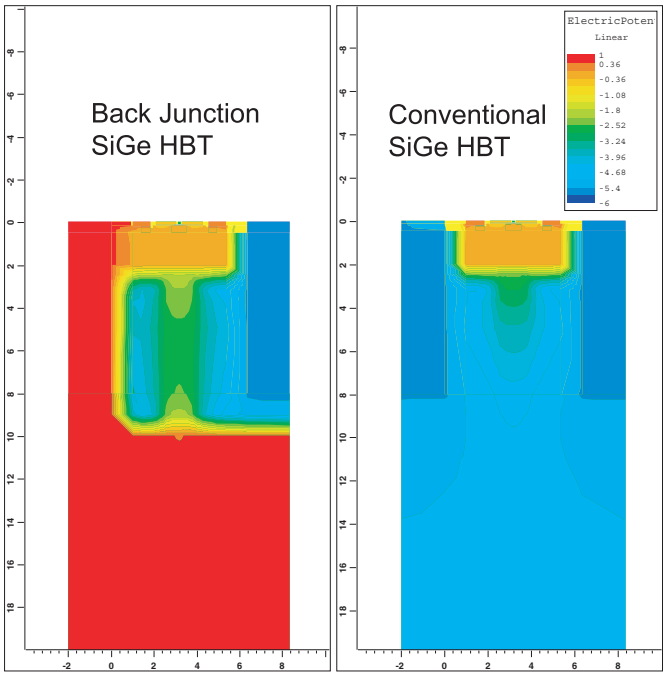


Figure 6.8: Comparison of potential contours at 4 psec in the back junction SiGe HBT and the conventional SiGe HBT. The p-layer of the back junction is 8μm thick.

6.2.2 Back Junction n^+ Sinker Design

The simulation details show that the resistance of the n^+ sinker for contacting the n^+ layer of the back junction is important for the overall charge collection through the back junction. To explore this, we then increased the n^+ sinker width to 4 μm and place the n^+ sinker on the left, top and right of the deep trench isolation ring, which effectively reducing the impedance to the back junction. The terminal charge collection results are summarized in Table 6.1.

Table 6.1: Terminal charges collected in pC for different n^+ sinker to back junction designs and regular HBT.

	Back Junction		Regular
	2.5μm sinker left	4.0 μm sinker perimeter	
back junction	0.41	0.48	N/A
collector	0.78	0.52	1.56
substrate	1.12	0.93	1.53
emitter	0.011	0.009	0.041
base	0.085	0.085	0.078

Fig. 6.9 compares the collector charge collection of the back junction SiGe HBT with different n^+ sinker designs as well as the conventional SiGe HBT. With the 4μm n^+ sinker back junction design, the amount of collector charge sees a 3× reduction from 1.56 pC in the conventional SiGe HBT to 0.52 pC.

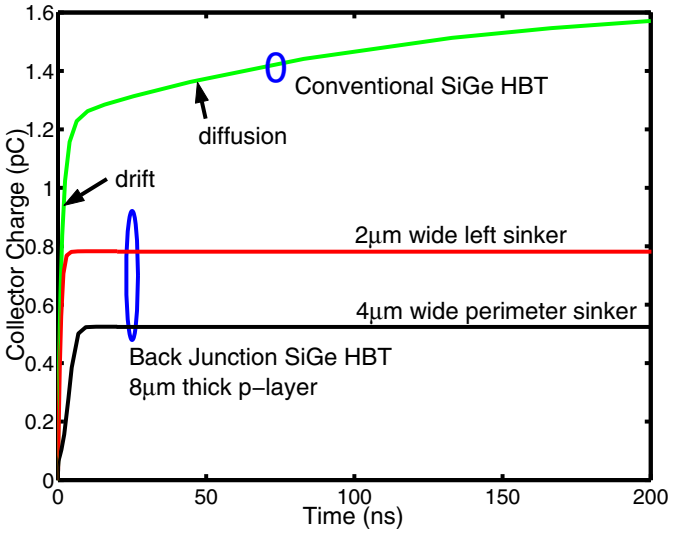


Figure 6.9: Comparison of collector charge collection in the back junction SiGe HBT with different n^+sinker designs, as well as the conventional SiGe HBT. The p-layer of the back junction is 8μm thick.

6.2.3 P-layer Thickness Consideration

As we mentioned earlier, the p-layer thickness limits the total amount of drift charge collection, and thus a thinner p-layer should lead to a further reduction of collector charge collection. Fig. 6.10 shows the simulated collector charge collection characteristics for different p-layer thicknesses. The n^+ sinker for contacting the back junction is 2 μm and placed on the left side for all of the p-layer thicknesses. By decreasing the p-layer thickness to 4 μm, we can further decrease the collector charge collection to 0.2 pC, a significant improvement over the 1.6 pC charge collection in the conventional SiGe HBT. Caution must be taken as the p-layer thickness is decreased to under 4μm;

the p-layer doping must be increased and the reversed bias V_{EE} should be reduced to -3V to prevent punchthrough.

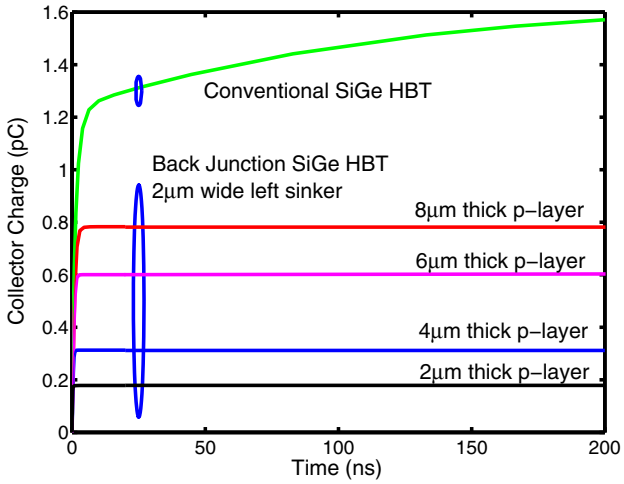


Figure 6.10: Comparison of collector charge collection for different p-layer thickness. The n^+ sinker for contacting the back junction is 2 μm and placed on the left side.

Fig. 6.11 shows the simulated potential contours at 4 psec in the back junction SiGe HBT for various p-layer thicknesses. The comparison shows clearly that the funneling is well confined within the p-layer, and the length of the potential funneling region is proportional to the p-layer thickness, as theoretically expected. Consequently, a thinner p-layer thickness will result in less collector charge collection, as was shown in Fig. 6.10.

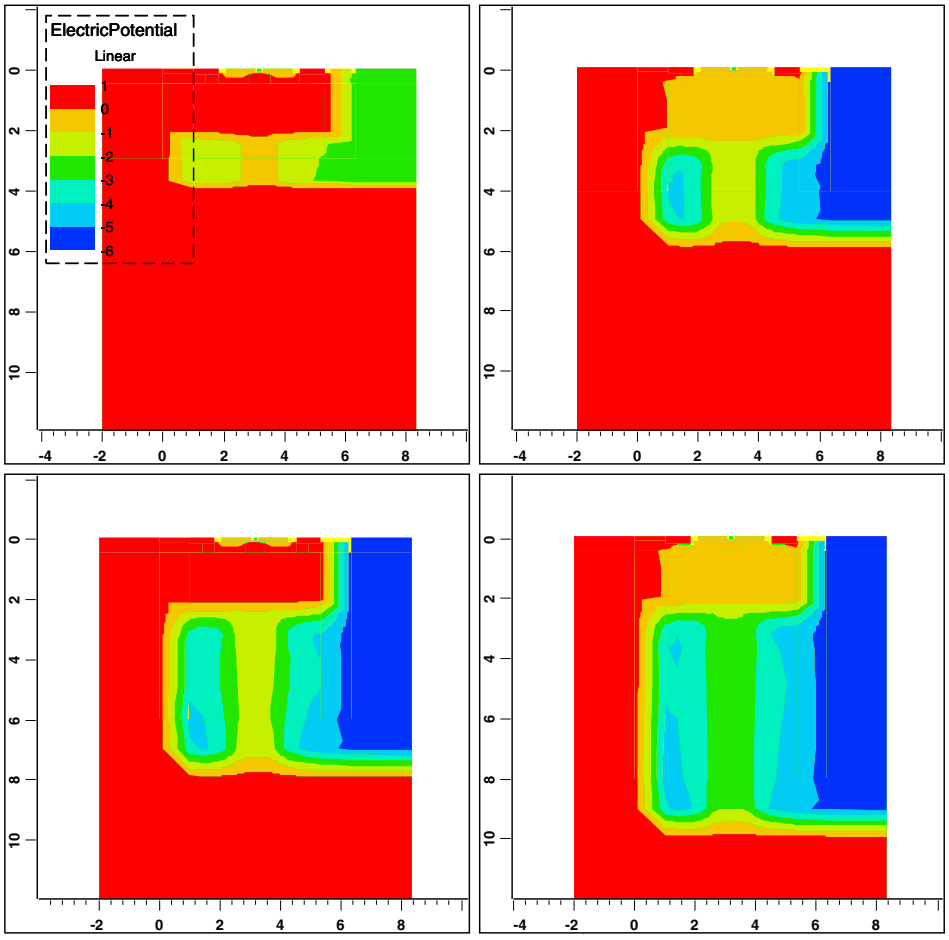


Figure 6.11: Comparison of potential contours at 4 psec in the back junction SiGe HBT with 2μm, 4μm, 6μm and 8μm p-layer thickness.

6.2.4 Device Fabrication Considerations

A straightforward way to fabricate the proposed structure is to start with a p-type supporting substrate, create a relatively heavily doped n-layer by diffusion for formation of the back junction, grow several microns p-type layer, and then create the n^+ collector buried layer, again by diffusion. The rest of the processing would be the same as for a conventional SiGe HBT. Alternatively, one might form the back junction the doping level of the p-type "substrate" layer. The n^+ collector buried layer can then be made the same way as for a conventional SiGe HBT.

6.3 Summary

The back junction approach is presented and its effectiveness is demonstrated with the 3D device simulations of the 200 GHz state-of-art SiGe HBT. The back junction limits potential funneling to within the p-layer, thus placing an upper limit to the total amount of drift charge collection. The path of diffusion charge collection in the conventional HBT is also cut off by the back junction. A wide n^+ sinker around the deep trench perimeter helps by enhancing back junction charge collection, hence reducing charge collection at the sensitive collector node. A thinner p-type "substrate" layer also effectively decreases collector charge collection.

CHAPTER 7

CONCLUSION

We have presented full 3D simulation of single event upset induced charge collection in a state-of-art 200 GHz SiGe HBT technology. The terminal transient current/ final charge collection characteristics are studied as well as internal device behaviors. The dependence of ion position and incident angle is simulated.

Sensitive areas of charge collection for each terminal are identified. The deep trench surrounds the area for maximum charge collection of collector and substrate while the shallow trench surrounds the area for maximum charge collection of base.

Different incident angle strike simulations support a new *Junction Passing / DT Confinement Model*. Angled strike in DT isolated HBT in general produces less charge collection. DT isolation ring limits the reach of charge collection available to the C/S junction. An ion that does not pass either collector-base or collector-substrate junctions produces little charge collection if it is confined within the heavily doped n^+ buried layer. Charge deposited outside DT can be collected by diffusion through lightly doped p-substrate.

A new back junction approach to reduce SEU-induced charge collection is proposed and verified. The back junction limits potential funneling to within the p-layer, thus placing an upper limit to the total amount of drift charge collection. The path of diffusion charge collection in the conventional HBT is also cut off by the back junction. A wide n^+ sinker around the deep trench perimeter helps by enhancing back junction

charge collection, hence reducing charge collection at the sensitive collector node. A thinner p-type "substrate" layer also effectively decreases collector charge collection.

BIBLIOGRAPHY

[1] J. D. Cressler and G. Niu, *Silicon Germanium Heterojunction Bipolar Transistors*, Artech House, Boston, 2002.

[2] P. E. Dodd and L. W. Massengill, "Basic mechanisms and modeling of single-event upset in digital microelectronics," *IEEE Transactions on Nuclear Science*, vol. 50, no. 3, pp. 583-602, 2003.

[3] P. W. Marshall, M. A. Carts, A. Campbell, D. McMorrow, S. Buchner, R. Stewart, B. Randall, B. Gilbert, and R. A. Reed, "Single event effects in circuit-hardened SiGe HBT logic at gigabit per second data rates," *IEEE Transactions on Nuclear Science*, vol. 47, pp. 2669C2674, Dec. 2000.

[4] R. A. Reed, P. W. Marshall, H. Ainspan, C. J. Marshall, H. S. Kim, J. D. Cressler, G. Niu, and K. A. LaBel, "Single event upset test results on a prescalar fabricated in IBM^{a}s 5 HP silicon germanium heterojunction bipolar transistors BiCMOS technology," in *Proceedings of IEEE Nuclear Space Radiation Effect Conference Data Workshop*, 2001, pp. 172C176.

[5] G. Niu, J. D. Cressler, M. Shoga, K. Jobe, P. Chu, and D. L.David L. Harame, "Simulation of SEE-induced charge collection in UHV/CVD SiGe HBTs," *IEEE Transactions on Nuclear Science*, vol. 47, pp. 2682C2689, Dec. 2000.

[6] G. Niu, H. Yang, M. Varadharajaperumal, Y. Shi, J. Cressler, R. Krishnavasan, P. Marshall, R. Reed, "A New Back Junction Approach For Reducing Charge Collection in 200 GHz SiGe HBTs," accepted by *IEEE Nuclear Space Radiation Effect Conference*, 2005.

[7] "Single Event Effect Criticality Analysis", *http://radhome.gsfc.nasa.gov/*, Feb. 15, 1996.

[8] "Single Event Effects", *http://www.eas.asu.edu/ holbert/eee460/*.

[9] DAVINCI, 3D Device Simulation Software, *Synopsys*, 2004.

[10] K. LaBel, "Single event effects specification," *radhome.gsfc.nasa.gov/*, 1993.

[11] P. Marshall, M. Carts, A. Campbell, R. Ladbury, R. Reed, C. Marshall, S. Currie, D. McMorrow, S. Buchner, C. Seidleck, P. Riggs, K. Fritz, B. Randall, and B. Gilbert, "A Comparative Study of Heavy Ion and Proton Induced Bit Error Rate Sensitivity and Complex Burst Error Modes in Commercially Available SiGe BiCMOS," *IEEE Transactions on Nuclear Science*, Vol. 51, No. 6, pp. 3457-3463, 2004.

[12] P. Marshall1, M. Carts, S. Currie, R. Reed, B. Randall, K. Fritz, K. Kennedy, R. Krithivasan, C. Siedleck, R. Ladbury, J. Cressler, D. McMorrow, S. Buchner, C. Marshall, K. LaBel, and B. Gilbert, "Autonomous bit error rate testing at multi-Gbit/s rates using a Circuit for Radiation Effects Self Test (CREST)", accepted by *IEEE Nuclear Space Radiation Effect Conference*, 2005.

[13] R. E. Dodd, "Device simulation of charge collection and single-event upset," *IEEE Transactions on Nuclear Science*, vol. 43, no. 2, pp. 561-575, 1996.

[14] J.S. Rieh; B. Jagannathan, D.R. Greenberg, M. Meghelli, A. Rylyakov, F. Guarin, Z. Yang; D.C. Ahlgren, G. Freeman, P. Cottrell, P.; and D. Harame, "SiGe heterojunction bipolar transistors and circuits toward terahertz communication applications," *IEEE Transactions On Microwave Theory and Techniques*, vol. 52, no. 10, pp. 2390-2408, October 2004

[15] L.W. Massengill, M.L. Alles, S.E. Kerns, and K.L. Jones, "Effects of Process Parameter Distributions and Ion Strike Locations on SEU Cross Section Data," *IEEE Transactions on Nuclear Science*, vol. 40, no. 6, Part 1-2, pp. 1804-1811, December 1993.

[16] G. C. Messenger and M. S. Ash, *Single Event Phenomena*, Chapman & Hall, 1997.

[17] P. Marshall, M. Carts, A. Campbell, D. McMorrow, S. Buchner, R. Stewart, B. Randall, B. Gilbert and R. Reed, "Single event effects in circuit-hardened SiGe HBT logic at gigabit per second data rates," *IEEE Transactions on Nuclear Science*, Vol. 47, No. 6, pp. 2669-2674, Dec. 2000.

[18] H. Rueker, B. Heinemann, R. Barth, D. Bolze, J. Drews, O. Fursenko, T. Grabolla, U. Haak, W. Hoeppner, D. Knoll, S. Marschmeyer, N. Mohapatra, H. H. Richter, P. Schley, D. Schmidt, B. Tillack, G. Weidner, D. Wolansky, H. Wulf, and Y. Yamamoto, "Integration of high-performance SiGe:C HBTs with thin-film SOI CMOS," *IEDM Technical Digest*, pp. 239–242, December 2004.

APPENDICES

APPENDIX A

3D DEVICE STRUCTURE GENERATION INPUT DECK

```
title             8HP SiGe HBT  Mesh Generation

comment           grid generation and initial biasing


comment           initial mesh specification

mesh              ^diag.fli  out.fil="8hp_mesh_top30"


$ x.mesh    6.34   $$+2+2

x.mesh     x.min=-2      width=2 n.space=1


x.mesh     width=1       n.space=1


x.mesh     width=0.82    n.space=2

x.mesh     width=0.25    n.space=1


x.mesh     width=0.75    n.space=3

x.mesh     width=0.23    n.space=2

x.mesh     width=0.06    n.space=1


x.mesh     width=0.12    n.space=5 h3=0.02
```

```
x.mesh     width=0.06    n.space=1

x.mesh     width=0.23    n.space=2

x.mesh     width=0.75    n.space=3


x.mesh     width=0.25    n.space=1

x.mesh     width=0.82    n.space=2


x.mesh     width=1       n.space=1


x.mesh     width=2       n.space=1
```

```
$ z.mesh    3.5  +2+2

z.mesh    z.min=-2   width=2 n.space=1


z.mesh    width=0.5  n.space=1

z.mesh    width=0.5  n.space=1

z.mesh    width=0.25 n.space=1

z.mesh    width=0.18 n.space=1

z.mesh    width=0.06 n.space=1
```

```
z.mesh    width=0.52 n.space=5 h3=0.02


z.mesh    width=0.06 n.space=1
z.mesh    width=0.18 n.space=1
z.mesh    width=0.25 n.space=1
z.mesh    width=0.5  n.space=1
z.mesh    width=0.5  n.space=1


z.mesh    width=2 n.space=1



$ y.mesh    vertical profile  0.16 + 55



y.mesh   depth=0.12 n.space=5 h2=0.005
y.mesh   depth=0.04 n.space=6 h1=0.005 h2=0.005
y.mesh   depth=0.34 n.space=5 h1=0.02 h2=0.05
y.mesh   depth=1.5  n.space=4 h2=0.2


y.mesh   depth=1    n.space=4 h1=0.5 h2=0.2
y.mesh   depth=5    n.space=4 h1=0.2
```

```
y.mesh   depth=2    n.space=2
y.mesh   depth=45   n.space=8 h1=1




comment     region definition

$ below DT  8-55
region    name=1  silicon y.min=8 y.max=55

$ $ DT & psub & n buri 0.5-8
region    name=2c  silicon y.min=0.5 y.max=8

region    name=2a  oxide y.min=0.5 y.max=8
+         x.min=0 x.max=6.34 z.min=0 z.max=3.5
region    name=2b  silicon y.min=0.5 y.max=8
+         x.min=1 x.max=5.34 z.min=1 z.max=2.5

$ $ ST & Coll contact & Emitter Hole  0.16-0.5
region    name=3a  oxide y.min=0.16 y.max=0.5
region    name=3b  silicon y.min=0.16 y.max=0.5
```

```
+         x.min=1.25 x.max=1.82 z.min=1.25 z.max=2.25
region    name=3c  silicon y.min=0.16 y.max=0.5
+         x.min=2.82 x.max=3.52 z.min=1.25 z.max=2.25
region    name=3d  silicon y.min=0.16 y.max=0.5
+         x.min=4.52 x.max=5.09 z.min=1.25 z.max=2.25



$ $ EB layer 0-0.16
$  around
region    name=4a  oxide y.min=0 y.max=0.16
$  intrinsic base
region    name=4b  silicon y.min=0.12 y.max=0.16
+         x.min= 2.07 x.max=4.27 z.min=0.5 z.max=3
$  raised base
region    name=4c  silicon y.min=0 y.max=0.12
+         x.min= 2.07 x.max=4.27 z.min=0.5 z.max=3
$  spacer
region    name=4d  oxide y.min=0 y.max=0.12
+         x.min= 3.05 x.max=3.29 z.min=1.43 z.max=2.07
$  emitter
region    name=4e  silicon y.min=0 y.max=0.12
+         x.min= 3.11 x.max=3.23 z.min=1.49 z.max=2.01
```

```
$ intrinsic base SIGE
region      name=6a sige     x.min=2.07 x.max=4.27 z.min=0.5 z.max=3
+                            y.min=0.11 y.max=0.115
+                            x.mol=0 x.end=0.06 y.linear
region      name=6b sige     x.min=2.07 x.max=4.27 z.min=0.5 z.max=3
+                            y.min=0.115 y.max=0.12
+                            x.mol=0.06 x.end=0.06 y.linear
region      name=6c sige     x.min=2.07 x.max=4.27 z.min=0.5 z.max=3
+                            y.min=0.12 y.max=0.13
+                            x.mol=0.06 x.end=0.25 y.linear
region      name=6d sige     x.min=2.07 x.max=4.27 z.min=0.5 z.max=3
+                            y.min=0.13 y.max=0.14
+                            x.mol=0.25 x.end=0.25 y.linear
region      name=6e sige     x.min=2.07 x.max=4.27 z.min=0.5 z.max=3
+                            y.min=0.14 y.max=0.155
+                            x.mol=0.25 x.end=0 y.linear


comment     electrodes

electr      name=emitter  x.min=3.11 x.max=3.23 z.min=1.49 z.max=2.01 top
```

```
electr      name=base1    x.min=2.3 x.max=2.8   z.min=1 z.max=2.5 top
electr      name=base2    x.min=3.5 x.max=3.98   z.min=1 z.max=2.5 top

electr      name=coll1    x.min=1.0 x.max=1.95
+                         z.min=0.5 z.max=2.5 y.min=0 y.max=0.3
electr      name=coll2    x.min=4.5 x.max=5.5
+                         z.min=0.5 z.max=2.5 y.min=0 y.max=0.3

electr      name=psub     x.min=6.34 x.max=8.34
+                         z.min=-2 z.max=5.5 y.min=0 y.max=0.6


comment     read in impurity profiles from ASCII
$ psub 8-55   below DT
profile      p-type   n.peak=5e15 y.min=8 y.max=55 y.char=0.0001
+            out.file=8hp_profile_top30

$ psub reach through 0.5-8
profile      p-type    n.peak=1e19  y.min=0.5 y.max=8  y.char=.0001
+                      z.min=-2   z.max=5.5 z.char=.0001
+                      x.min=-2   x.max=0 x.char=.0001
```

```
profile      p-type    n.peak=1e19  y.min=0.5 y.max=8  y.char=.0001
+                      z.min=-2   z.max=5.5 z.char=.0001
+                      x.min=6.34   x.max=8.34 x.char=.0001

profile      p-type    n.peak=1e19  y.min=0.5 y.max=8  y.char=.0001
+                      z.min=-2   z.max=0 z.char=.0001
+                      x.min=0   x.max=6.34 x.char=.0001

profile      p-type    n.peak=1e19  y.min=0.5 y.max=8  y.char=.0001
+                      z.min=3.5   z.max=5.5 z.char=.0001
+                      x.min=0   x.max=6.34 x.char=.0001

$ psub 2-8    below ST n+Buried
profile      p-type   n.peak=5e15 y.min=2 y.max=8 y.char=0.0001
+                     x.min=1 x.max=5.34 x.char=0.0001
+                     z.min=1 z.max=2.5 z.char=0.0001

$ n+buried 0.5-2
profile      1d.ascii in.fil=asBuri.dat y.col=1 n.col=2
+                  y.direct
+                  y.max=3
+                  x.min=1 x.max=5.34 z.min=1 z.max=2.5
```

```
+                  x.char=0.0001  z.char=0.0001

$$  ST 0.16-0.5

$ collector SIC
profile      1d.ascii in.fil=phos.dat y.col=1 n.col=2
+                  y.direct
+                  y.max=3
+                  x.min=3.11 x.max=3.23 z.min=1.49 z.max=2.01
+                  x.char=0.0001  z.char=0.0001

$ extrinsic coll 0.16-0.5
profile      n-type n.peak=1e16  y.min=0.16 y.max=0.5 y.char=0.0001
+                     x.min=2.82 x.max=3.11 x.char=0.0001
+                     z.min=1.25 z.max=2.25 z.char=0.0001
profile      n-type n.peak=1e16  y.min=0.16 y.max=0.5 y.char=0.0001
+                     x.min=3.23 x.max=3.52 x.char=0.0001
+                     z.min=1.25 z.max=2.25 z.char=0.0001
profile      n-type n.peak=1e16  y.min=0.16 y.max=0.5 y.char=0.0001
+                     x.min=2.82 x.max=3.52 x.char=0.0001
+                     z.min=1.25 z.max=1.49 z.char=0.0001
profile      n-type n.peak=1e16  y.min=0.16 y.max=0.5 y.char=0.0001
```

```
+                       x.min=2.82 x.max=3.52 x.char=0.0001
+                       z.min=2.01 z.max=2.25 z.char=0.0001

$ coll plug
profile      n-type n.peak=1e20  y.min=0.16 y.max=0.5 y.char=0.0001
+                       x.min=1.25 x.max=1.82 x.char=0.0001
+                       z.min=1.25 z.max=2.25 z.char=0.0001
profile      n-type n.peak=1e20  y.min=0.16 y.max=0.5 y.char=0.0001
+                       x.min=4.52 x.max=5.09 x.char=0.0001
+                       z.min=1.25 z.max=2.25 z.char=0.0001



$$ base&emitter 0-0.16
$ intrinsic base
profile      1d.ascii in.fil=boron.dat y.col=1 p.col=2
+                  y.direct
+                  y.max=3
+                  x.min=2.07 x.max=4.27 z.min=0.5 z.max=3
+                  x.char=0.0001  z.char=0.0001
$ raised base  (Deep into the SiGe layer doubled)
profile        p-type n.peak=1e19  y.min=0 y.max=0.16 y.char=0.0001
+                       x.min=2.07 x.max=3.05 x.char=0.0001
```

```
+                       z.min=0.5 z.max=3 z.char=0.0001
profile         p-type n.peak=1e19  y.min=0 y.max=0.16 y.char=0.0001
+                       x.min=3.05 x.max=3.29 x.char=0.0001
+                       z.min=0.5 z.max=1.43 z.char=0.0001
profile         p-type n.peak=1e19  y.min=0 y.max=0.16 y.char=0.0001
+                       x.min=3.05 x.max=3.29 x.char=0.0001
+                       z.min=2.07 z.max=3 z.char=0.0001
profile         p-type n.peak=1e19  y.min=0 y.max=0.16 y.char=0.0001
+                       x.min=3.29 x.max=4.27 x.char=0.0001
+                       z.min=0.5 z.max=3 z.char=0.0001

$ emitter 0-0.12
profile      1d.ascii in.fil=as.dat y.col=1 n.col=2
+                    y.direct
+                    y.max=3
+                    x.min=3.11 x.max=3.23 z.min=1.49 z.max=2.01
+                    x.char=0.0001  z.char=0.0001



save                 out.fil="8hp_mesh_top30.tif"
+                    mesh TDF potentia holes electron doping x.mol
```

APPENDIX B

3D SEU DEVICE SIMULATION INPUT DECK

```
Comment   SEU Device Simulation
mesh      in.file="8hp_mesh_top30"
model     phumob fldmob consrh auger bgn
call      file=newslotboom
SYMB      GUMMEL  CARRIERS=0
METHOD    DAMPED ICCG
solve
assign    name=id c.value=top30a02
LOG       OUT.FILE=@id"seu.log"

COMMENT   Switch to Newton and two carriers and
+         solve for the time=0 reverse bias solution.
SYMBOL    NEWTON  CARRIERS=2
SOLVE
SOLVE     V(coll1)=0
+         v(coll2)=0
+         v(base1)=0 v(base2)=0
+         v(emitter)=0
+         v(psub)=0
```

```
+         electro=psub
+         vstep=-1.0
+         nstep=5

METHOD    ITLIMIT=10
PHOTOGEN  X.START=3.17  X.END=3.17
+         Z.start=1.75 Z.end=1.75
+         Y.START=0.0  Y.END=55
+         DCHR=0.2
+         T0=4.0E-12  TC=2.0E-12  C1=0.2 PC.UNITS  GAUSS

COMMENT   Simulate the first 200ns of transient response.
SOLVE     TSTEP=0.5E-12  TSTOP=2.0e-7  out.file=@id"sol00"
```