Layout and Assembly of a High Efficiency Multi-Phase Buck Converter Utilizing Chip Scale GaN Devices

by

Stephan Wenz Henning

A thesis submitted to the Graduate Faculty of
Auburn University
in partial fulfillment of the
requirements for the Degree of
Master of Science

Auburn, Alabama
August 2, 2014

Keywords: Power Conversion, Buck Converter, Switch Mode Power Supply

Copyright 2014 by Stephan Wenz Henning

Approved by

Robert N. Dean, Chair, Associate Professor of Electrical and Computer Engineering
Stuart Wentworth, Associate Professor of Electrical and Computer Engineering
Michael Hamilton, Assistant Professor of Electrical and Computer Engineering

Abstract

As the world becomes increasingly immersed in the Information Age, more and more supercomputers and datacenters must be built to keep up with humanity's demand for electronic information. As the number of these facilities and their physical size continue to grow, so do the power demands that they place on their local power grids. Much of this demand is a direct result of the processing hardware being utilized, but a large majority of this is wasted power, lost within the system due to various areas of inefficiency.

This work will describe the implementation of a prototype design for a Point of Load voltage regulator for use in power datacenter processors using new technology GaN FETs to generate efficiencies greater than 90%. This work will detail a process used to prototype with these chip scale package GaN devices, allowing for a faster development cycle of a converter design within organizations that may not have access to advanced assembly equipment. This process details how to assemble these GaN devices in a manner that provides very high yields, while considering the possible equipment limitations of most organizations.

This process is then used in the implementation of these GaN devices in the creation of a Point of Load prototype to demonstrate the improved efficiencies possible by using these GaN devices. Design, layout, assembly, and testing stages are discussed for two versions of the prototype, detailing many of the decisions made during the design process to fully utilize these

devices. This work provides information useful to any organization considering using these new generation GaN devices in future designs by demonstrating their capabilities, discussing the features of the technology, reviewing some guidelines that may be beneficial during the design stages, and by providing a high yield assembly method that can be implemented within most well equipped organizations.

Acknowledgments

I would like to thank my friends and family for their constant support and encouragement, without them this would not be possible. I would also like to thank Kristina for her unwavering love and faith, especially when deadlines loom large and require many late nights to stay on schedule. I would like to thank Dr. Dean for his mentorship, encouragement, and financial support over the course of this project, along with his freely given advice about life in general. I would like to thank Dr. Hamilton for the many discussions about technical matters related to this project and his support in general. I would like to thank Dr. Wentworth for his support and encouragement throughout my undergraduate carrier and his continued support of me as I continued in my academic pursuits. I would also like to thank Dr. Johnson for his management of this project, without which this work would not have been possible. I am grateful for the advice, encouragement, and assistance provided by my fellow students on this project, without them this project could not succeed. I would also like to thank John Tennant, Joe Haggerty, Linda Barresi, and Mike Palmer for their patience and assistance whenever I ran into a problem that needed their input.

Table of Contents

Abstract ii

Acknowledgments iv

List of Tables viii

List of Figures ix

Nomenclature xiii

Chapter 1 Introduction 1

Chapter 2 Background and Previous Work 5

2.1 DC Distribution 5

2.2 Point of Load Converters 7

2.3 Wide Band-Gap Devices 11

Chapter 3 Design Goals and Approach 19

3.1 Scope and Goals 19

3.2 Converter Selection 21

Chapter 4 GaN Technology Implementation 24

4.1 EPC Device Packaging 24

4.2 Manual Assembly 27

4.3 Primary Manual Assembly Method 28

4.3.1 Preparation 30

4.3.2 Placement 32

4.3.3 Alignment 34

4.3.4 Reflow 36

4.3.5 Inspection 37

4.4 Secondary Manual Assembly Method 40

4.4.1 Preparation 41

4.4.2 Placement and Alignment 43

4.4.3 Reflow 44

4.4.4 Inspection 45

Chapter 5 Point of Load Version 2 48

5.1 Design 49

5.2 Layout and Implementation 55
5.3 Assembly 62
5.4 Testing and Analysis 63
5.5 Lessons Learned 72
Chapter 6 Point of Load Version 3 74
6.1 Design 74
6.2 Layout and Implementation 85
6.3 Assembly 91
6.4 Testing and Analysis 97
6.5 Conclusions 108
Chapter 7 Conclusions 110
7.1 Summary 110
7.2 Future work 111
References 113
Appendix A: POL V1 Schematics 120
Appendix B: POL V1 Layout 124
B.1 Feedback 124
B.2 Synchronous Buck 125
B.3 Asynchronous Buck 126
B.4 Load 128
B.5 Power 130
Appendix C: POL V2 Schematics 132
Appendix D: POL V2 Layout 137
Appendix E: POL V3 Schematics 143
Appendix F: POL V3 Layouts 145
F.1 Carrier Board 145
F.2 Buck Daughter Card 150
Appendix G: Software, Scripts, and Code 152

G.1 Buck V2 Matlab Plotting Code..152
G.2 Buck V3 Stages 1-3 Matlab Plotting Code...157
G.3 Buck V3 Stages 7-9 Matlab Plotting Code...163

List of Tables

Table 1: Power Draw of Top Systems 2

Table 2: Wide Band-gap Material Properties [24] 12

Table 3: GaN Technology Advantages [25] 14

Table 4: EPC Device Electrical Characteristics 17

Table 5: Comparison of Device Characteristics 17

Table 6: Point of Load Design Objectives 21

Table 7: Comparison of Device Packages [26] 25

Table 8: EPC Recommended Equipment and Materials 27

Table 9: Required Equipment and Materials 29

Table 10: Secondary Method Materials and Equipment 41

Table 11: Device Electrical Charactereistics 52

Table 12: Version 2 Areas Requiring Improvement 73

Table 13: Version 3 Priority Design Areas 74

Table 14: Power stage configurations 102

List of Figures

Figure 1: Traditional AC Distribution System.................... 6

Figure 2: High Voltage DC Distribution System.................... 7

Figure 3: Refined DC Distribution System.................... 8

Figure 4: Theoretical Limits of GaN, Si, and SiC [21].................... 13

Figure 5: Typical GaN Device [26] 15

Figure 6: EPC eGaN Device [26] 16

Figure 7: Auburn/UT DC Distribution System.................... 20

Figure 8: Typical Multiphase Buck Circuit 22

Figure 9: Chip Scale Packaging used by EPC on a U.S. penny.................... 26

Figure 10: Process Groups 29

Figure 11: Footprint before pads are 'bumped'. 31

Figure 12: Correctly ‘bumped’ footprint pads. 32

Figure 13: Footprint after tacky flux application..................... 33

Figure 14: X-Ray image of misaligned device. 36

Figure 15: X-Ray image of properly aligned device. 36

Figure 16: X-Ray image of properly soldered device..................... 39

Figure 17: Assembled Version 1 Buck Converter 48

Figure 18: Version 2 Controller, FPGA Interface & dsPIC 51

Figure 19: Version2 Gate Drive Circuit 53

Figure 20: Version2 Converter Circuit 54

Figure 21: Final Version2 Converter Component Placement 57

Figure 22: Version2 Converter, 4 Phases. 57

Figure 23: Initial Version2 Controller Component Placement 58

Figure 24: Initial Placement, all Components 59

Figure 25: 2x2 Oriented Converter Phases 60

Figure 26: Final Version2 Layout 62

Figure 27: Assembled Version2 Board 63

Figure 28: Close up of Assembled Converter Phases 1 and 4 64

Figure 29: Back of board showing assembled Phase 4 64

Figure 30: Assembled load board. 65

Figure 31: Phase 1 efficiency data 66

Figure 32: Phase 4 efficiency data 67

Figure 33: Average of the data from Phase 1 and Phase 4 67

Figure 34: 2 Phase operation efficiency data 68

Figure 35: Circuit waveforms at 1.8A output 70

Figure 36: Circuit waveforms at 5.6A out 71

Figure 37: Version 3 gate drive circuit 76

Figure 38: Version 3 converter circuit 79

Figure 39: Full version 3 converter stage 79
Figure 40: Version 3 ControlCard interface 81
Figure 41: Converter phase status check 82
Figure 42: User programmable converter status LEDs 82
Figure 43: User programmable pushbutton inputs 83
Figure 44: Use programmable LED indicators 83
Figure 45: Converter daughter card interface 85
Figure 46: Version 3 gate drive layout 87
Figure 47: Version 3 converter power stage daughter card layout 88
Figure 48: Version 3 carrier board layout 91
Figure 49: Version 3 unassembled converter daughter card 92
Figure 50: Assembled version 3 converter circuit. 93
Figure 51: Duaghter card installed in carrier board 94
Figure 52: Unpopulated carrier board 95
Figure 53: Populated control side of carrier board 95
Figure 54: ControlCard installed in carrier board 96
Figure 55: Converter daughter card installed and being tested 97
Figure 56: Default converter circuit assembled 98
Figure 57: Efficiency data for power stage 1 99
Figure 58: Efficiency data for power stage 2 99
Figure 59: Efficiency data for power stage 3 100

Figure 60: Average of efficiency data stages 1, 2, and 3 101
Figure 61: Average frequency efficiency delta 101
Figure 62: Assembled power stage 7 103
Figure 63: Assembled power stage 8 104
Figure 64: Assembled power stage 9 104
Figure 65: EPC2014 under high current load 105
Figure 66: Efficiency data for power stage 7 106
Figure 67: Efficiency data power stage 8 107
Figure 68: Efficiency data power stage 9 108

Nomenclature

Acronyms

GaN	Gallium Nitride
FET	Field-Effect Transistor
POL	Point of Load
EPC	Efficient Power Conversion
DC	Direct Current
AC	Alternating Current
CPU	Central Processing Unit
HVDC	High Voltage Direct Current
PDU	Power Distribution Unit
Si	Silicon
CMOS	Complementary Metal-Oxide-Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
SiC	Silicon Carbide
BFoM	Baliga's Figure of Merit
HEMT	High-Electron-Mobility Transistor
RF	Radio Frequency
AlN	Aluminum Nitride
AlGaN	Aluminum Gallium Nitride

2DEG	2 Dimensional Electron Gas
eGaN	Enhancement mode Gallium Nitride
CSP	Chip Scale Package
ESD	Electrostatic Discharge
PCB	Printed Circuit Board
BGA	Ball Grid Array
IO	Input/Output
FPGA	Field Programmable Gate Array
ADC	Analog to Digital Converter
SMT	Surface Mount Technology
SMD	Surface Mount Device
MLCC	Multi-Layer Ceramic Capacitor
LED	Light Emitting Diode
DIP	Dual in-line Package
IC	Integrated Circuit
DIMM	Dual in-line Memory Module
RAM	Random Access Memory
SMPS	Switch Mode Power Supplies

Terms

IR	Conduction Losses

Chapter 1 Introduction

In June of 2011 a new leader rose to the top of the TOP500 supercomputing list [1]. This newcomer to the list was the K computer built by Fujitsu and installed at the RIKEN Advanced Institute for Computational Science in Kobe, Japan. This supercomputer currently stands as the largest supercomputer in the world with a reported computing rate of 8.1 petaflops consuming 9.9MW of power, far besting its closest competitor, the Tianhe-1A with a reported rate of 2.5 petaflops which consumes 4MW. As of the most recent update of this list in November 2013 [2], the top system is now the Tianhe-2, with a computation rate of 33.86 petaflops requiring 17.8MW of power from the grid.

In this modern age, computing has become an integral part of our culture. It would be very difficult for anyone living in a technological society to make it through an average day without interacting with some kind of computer system. Not only has the level of computer integration into our daily lives increased, the scale of the computers necessary to power the daily workings of a modern world has also increased. As the scale of these large computers continues to expand, the power requirements of these systems grow as well. The largest of these supercomputer and datacenter systems have grown to the point where their power requirements are in the megawatt range, a consumption rate equivalent to that used by thousands of average suburban households. Table 1 shows the power requirements of several of the largest computing systems and their equivalent household draw. Reducing the power requirements of these facilities, thereby reducing stress on the power grid and facility operating costs, is the main reason for this push to increase power system efficiency. The implementation of more efficient

data centers becomes more and more important as energy costs continue to rise as countries like China continue to modernize at astounding rates, their energy requirements growing with them, putting pressure on global energy reserves.

Table 1: Power Draw of Top Systems

Machine	**Location**	**Processing Power** ***(TFlops/s)***	**Power Draw** ***(kW)***	**Equivalent # US Households** [3]
Tianhe-2	China	33862.7	17808	14396
Titan	USA	17590.0	8209	6636
Sequoia	USA	17173.2	7890	6378
K computer	Japan	10510.0	12660	10234
Mira	USA	8,586.6	3,945	3189

Not only is the operation of these large scale computer systems very expensive, the addition of these large datacenters places increased strain on local power grids. Unfortunately, a significant portion of the power draw by these supercomputers never reaches the processors, instead being lost as heat in the electronic systems that supply the power to these processors. While large strides have been made in reducing the power requirements of the processors, as much as 35% of the power supplied to these systems may be lost in the power supplies that support them.

Addressing this relatively low overall efficiency has become vital to the development of new systems as the yearly cost of power to operate and cool these new installations begins to rival the costs associated with the construction of the facility. Additionally, any power that is wasted due to system inefficiency is burned off as heat. This only adds onto the cost of running the system as more power must now be used to operate the cooling systems needed to remove this extra heat.

Increasing the efficiency of a power system for such large facilities becomes a complicated systems problem with many separate sections that must be addressed. The focus of this work is on the Point of Load (POL) section of the power system that is being developed at Auburn University, in collaboration with the University of Tennessee where work on the other sections of the power system occurred. The POL portion of the power system typically comprises the final section of the supply, providing power directly to the processing units. Due to the lower voltages and higher currents required by modern processing units, POL stages face efficiency issues due to factors such as device resistance and circuit I^2R losses, in addition to any losses inherent in the circuit topology used in a design.

This work will address these losses by looking at efficiency improvements related with the use of gallium nitride (GaN) devices in the POL power stage. Chapter 2 will provide a background on previous research in the area as well as additional discussion related to the motivation of the work. Chapter 2 will also provide an overview of wide band-gap technology, some of the features of GaN devices, and how these devices help improve efficiency when used in power converter designs. This is then followed in Chapter 3 by a discussion of design considerations for this project in the implementation of the POL power stage. Chapter 4 will discuss the implementation of these GaN devices by utilizing an assembly solution that allows for rapid prototyping of design changes. Chapter 5 will discuss the implementation of the GaN devices into version 2 of a functional converter prototype and lessons learned from the initial design. Chapter 6 provides a detailed description of the design for version 3 of the POL and discusses improvements from the version 2 design. Chapters 5 and 6 detail the design goals, provide analysis of the design and test data, and highlight areas where further improvement

could be made. Chapter 7 will provide a summary of the completed designs and describe future work that can expand on the efforts developed in this portion of the project.

Chapter 2 Background and Previous Work

While the problem of power system efficiency is not new, the rapid rates of improvement in computer processing power and the ever increasing demands for larger and more powerful installations has begun to exceed the capabilities of the power system technology available. While it is necessary to consider the power system as a whole when discussing efficiency, the high power, low voltage – high current, nature of the POL portion of the power system creates the opportunity for large device and conduction losses within the subsystem. This chapter provides some background on high efficiency POL regulators and previous work done in this area.

2.1 DC Distribution

As datacenters have grown in size and scale, their power requirements have also changed. Recent trends in processor design have created chips that are becoming ever more efficient in terms of their processing capacity per watt while also being installed in denser and denser rack system, allowing for very high CPU and core counts in current generation high density servers. While these new processors are more energy efficient, their size, and hence power demand, continue to increase, so the rest of the power system cannot be ignored when the goal is to create a power efficient datacenter.

For many years the typical datacenter power system architecture was based on an AC distribution system that would then convert AC to the DC needed by the computer systems with the server rack level. An example of such an architecture is shown below in Figure 1 and is

discussed by Smedman in [4], Oliver in [5], Bindra in [6], and Murrill and Sonnenberg in [7]. While these systems are well understood and easy to implement, the multiple AC/DC conversion steps and relatively low efficiency of the rack level AC/DC power supplies can bring total system efficiency down into the 70% range.

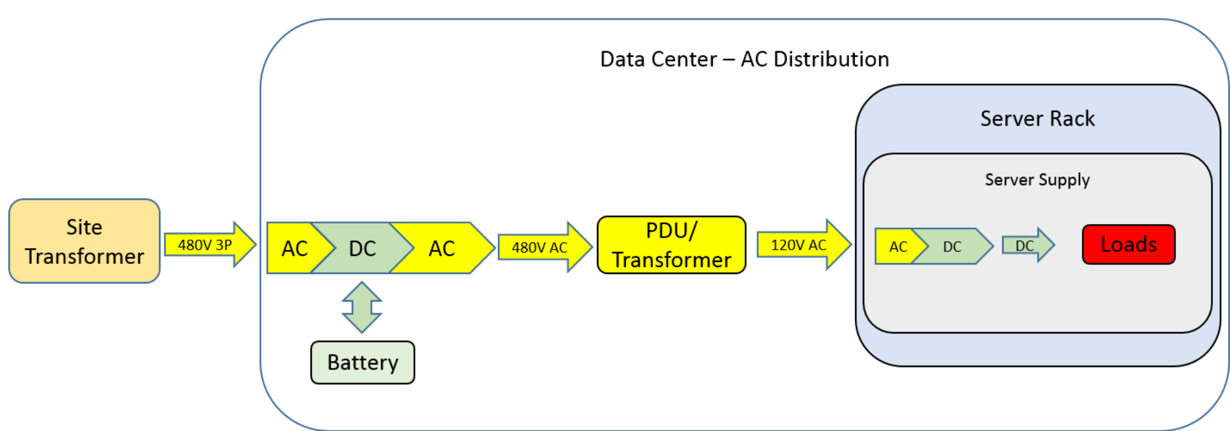


Figure 1: Traditional AC Distribution System

With the advancements in processing power and data storage, new power distribution systems have been developed to better power these datacenters. While some new generation systems are still utilizing AC distribution to great effect [8], many installations are beginning to transition to HVDC based distribution systems, such as the Sakura Ishikari Data Center in Japan which is utilizing a HVDC system to simplify its power system and while boosting power efficiency, generating cost savings that will allow to Sakura to compete in new technology markets [9]. While there is some variation in the specific architecture used as discussed in [10], [11], [4], [12], and [13], most facilities use a system similar to what is shown in Figure 2.

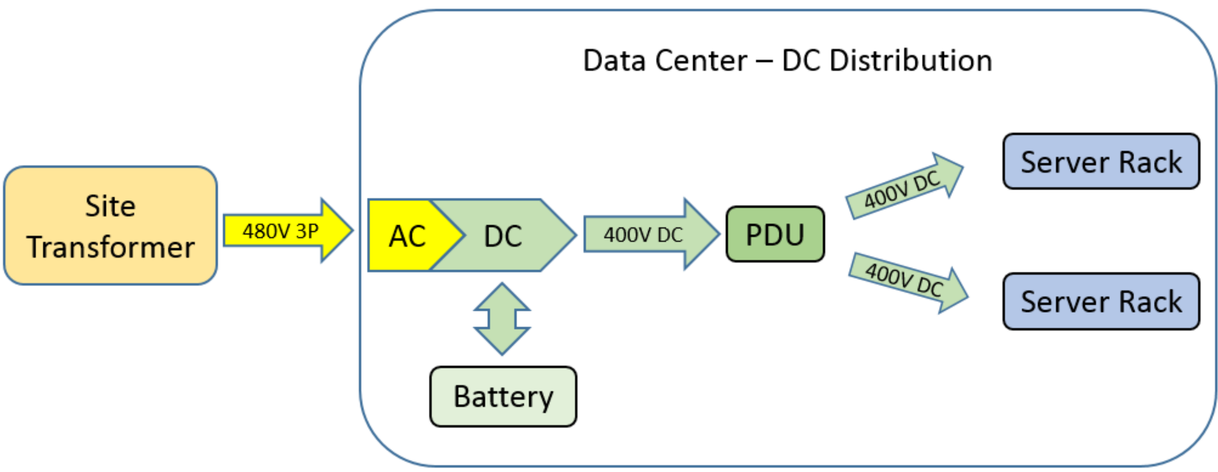


Figure 2: High Voltage DC Distribution System

This type of DC distribution system utilizes few AC/DC conversion steps, allowing for increased efficiency gains. However, this new type of system creates a need for more advanced DC supplies capable of performing DC-DC conversions to provide the computing equipment with the required DC voltages for storage media and processor cores. Companies such as Vicor [14] [5] rose to the challenge with new high efficiency DC product lines. For many large scale installations this would not be sufficient, requiring the adoption of advanced power systems using recent advancements in Si and GaN semiconductors in power converter design to further increase efficiencies within the DC supplies, providing substantial long term cost benefits considering their considerable power usage.

2.2 Point of Load Converters

This newer DC distribution architecture requires the bulk of the conversion processes to occur at the rack level in the overall system. In order to achieve this, the DC power supplies used need to maintain high efficiency while maintaining a low volume, to avoid a negative impact to

current rack processor densities. Figure 3 enhances the previous DC system diagram in and shows a further breakdown of the power system within the confines of the computation rack itself, with two possible options being shown.

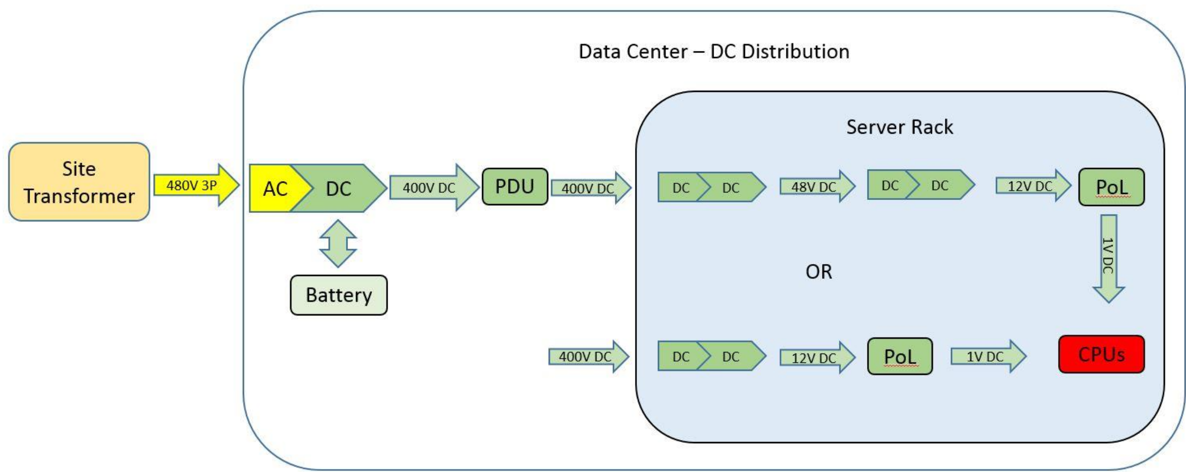


Figure 3: Refined DC Distribution System

Within this DC distribution architecture, the Point of Load (POL) supply now becomes a main focus of the design due to its low output voltages and high current levels, requiring careful design in order to maintain the operating efficiencies needed to ensure overall system efficiency remains high.

In order to reach these efficiency goals, the POL supply needs to be mounted in close proximity to the processor cores in order to minimize conduction losses. This creates volumetric problems as the POL supply must have a small enough footprint to ensure that inter-card spacing can be kept small enough to maintain processor core density levels. Casey and Martin were one of the early investigators into board level POL converters and describe in [15] the utilization of a high frequency resonant converter for use as a 50W, 40V to 5V POL supply, but were limited by the components available to them at the time. Fisher et al. continued this work, using a simplified

version of the circuit in [16] and alternate fabrication methods to demonstrate a 100W 40V to 5V converter, but they also experienced fabrication issues and thermal problems due to lower than expected efficiencies of approximately 79%.

In [17] Nagar et al. provide a low output voltage ripple solution though the implementation of filter networks. Two separate options were presented, with the final recommendation utilizing a two stage LC filter in conjunction with a control system to maintain operational stability. The discussed combination of output filter and control algorithm provided a significant decrease in voltage ripple, but at a detriment to system efficiency and response rate.

Ng, Seeman, and Sanders demonstrated a CMOS based switched-capacitor POL converter with peak efficiency of 93%, with 80% over a 7mA to 1A range. This was achieved through the construction of Dickson type circuit fabricated on a chip using CMOS manufacturing techniques, as demonstrated in [18]. While the topology is impressive, the current requirements for this work are not comparable to the low current available from this implementation on the CMOS level.

Zhou, Donati, Amoroso, and Lee investigate a control system solution to improving buck topology regulators light load efficiency in [19]. They were able to demonstrate dramatic improvements at light loads of less than 1A by using drive signals specific to the load condition. This method allows for the improvement of light load efficiencies while maintaining efficiency levels at higher output currents of 8A as well. This method of control adjusts frequency as load levels increase and decrease, while also adjusting the on/off time of the synchronous rectifier, forcing the inductor to operate in discontinuous mode. This control is managed by sensing the inductor current by using changes in duty cycle in operation due to load level transitions. This requires additional logic to be implemented, either in discrete components or in the coding of the

control system. If this control method can be properly implemented, this forcing of the circuit to operate in discontinuous mode coupled with the reduced switching losses of the lower frequency operation are shown to provide great improvement at light loads without sacrificing performance at higher loads.

Xu, Wei, and Lee propose in a modification to the buck topology that allows for operation at larger duty cycles, while still maintaining the large input/output voltage ratio necessary for modern process voltage regulators. The novel topology described in [20] is called a multiphase coupled buck converter and uses coupled tapped inductors between the buck phases, combined with an active clamping circuit to handle voltage spikes that would otherwise damage the MOSFET switches. An implementation of the tested circuit resulted in a four phase $12V_{In}$, $1.5V_{Out}$, 50A converter that was operated at 300kHz with a peak efficiency of 89% and full load efficiency of 85%. This improvement over a comparable standard four phase buck converter which presented peak efficiency of 84.5% and full load efficiency of 81.5% was a result of significantly reduced switching losses, but this gain was decreased slightly from higher conduction losses in the synchronous switch.

While there has been significant work in the area of POL regulators, none of the current research solves the problem set specific to the demands of the newer generation of high current processors. Based on these previous works and other research into the area, it is believed that a combination of these methods and the implementation of next generation wide band-gap GaN devices will provide the efficiency levels needed.

2.3 Wide Band-Gap Devices

Silicon has been the dominant semiconductor material for most applications for many decades. Research and development in silicon technology has brought the technology to the point where devices are now near the theoretical limits for the material, and in cases such as super-junction devices and other advanced structures, past the theoretical limits as described by Lidow and Strydom in [21] and by Sherman and Herbsommer in [22]. Even with these continued advancements, as a mature technology silicon still cannot meet the needs of certain applications.

Wide band-gap devices have been in discussion since the 1950's, when William Shockley gave the introduction at the first Silicon Carbide Conference in 1958. Despite this, most research has focused on silicon devices, so much so that the first commercial wide band-gap devices were not available until 2001, with the introduction of a silicon carbide (SiC) Schottky diode by Rohm [23]. Since then fabrication processes have continued to evolve and more and more devices have reached the market, finding niche areas in which the performance advantages of wide band-gap materials make them competitive with mature silicon devices.

As research into wide band-gap devices continues, two materials have come to dominate most research and development, gallium nitride (GaN) and silicon carbide. While there are other materials that fall into the category of wide band-gap, SiC and GaN are the main materials used due to their materials properties and their relative ease of use in manufacturing as described by Kaminski in [24]. Table 2 below outlines some relevant material properties for GaN and SiC as compared to silicon (Si) and diamond.

Table 2: Wide Band-gap Material Properties [24]

Parameter		Silicon	4H – SiC	GaN	Diamond
Band-gap E_g	eV	1.12	3.26	3.39	5.47
Intrinsic Conc. n_i	cm^{-3}	$1.4 \cdot 10^{10}$	$8.2 \cdot 10^{-9}$	$1.9 \cdot 10^{-10}$	$1 \cdot 10^{-22}$
Critical Field E_{crit}	MV/cm	.23	2.2	3.3	5.6
Electron Mobility μ_n	$cm^2/V \cdot s$	1400	950	1500	1800
Permittivity ε_r	-	11.8	9.7	9.0	5.7
Thermal Cond. λ	W/cm·k	1.5	3.8	1.3	20
BFoM: $\varepsilon_r \cdot \mu_n \cdot E_C^3$	rel. to Si	1	500	2400	9000

From this table several advantages to wide band-gap materials are apparent. Their lower intrinsic carrier concentration coupled with their higher band-gap, leakage currents for devices built from these materials are lower, requiring significantly higher temperature to reach comparable leakage currents to Si devices. The higher critical field of these materials means that for devices of the same width, devices manufactured with wide band-gap materials will have a higher breakdown voltage as compared to a Si device. The so called Baliga's figure of merit is a method of measuring the materials contribution to the on-resistance of a unipolar device and is defined as in ($BFoM = \varepsilon_r \cdot \mu_n \cdot E_C^3$) in [24]. While these values show favoritism toward the wide band-gap materials, on-resistance is based on many factors and device design must be taken into account when comparing between the materials. Figure 4 shows a comparison of theoretical on-resistance vs breakdown voltage for Si, GaN, and SiC.

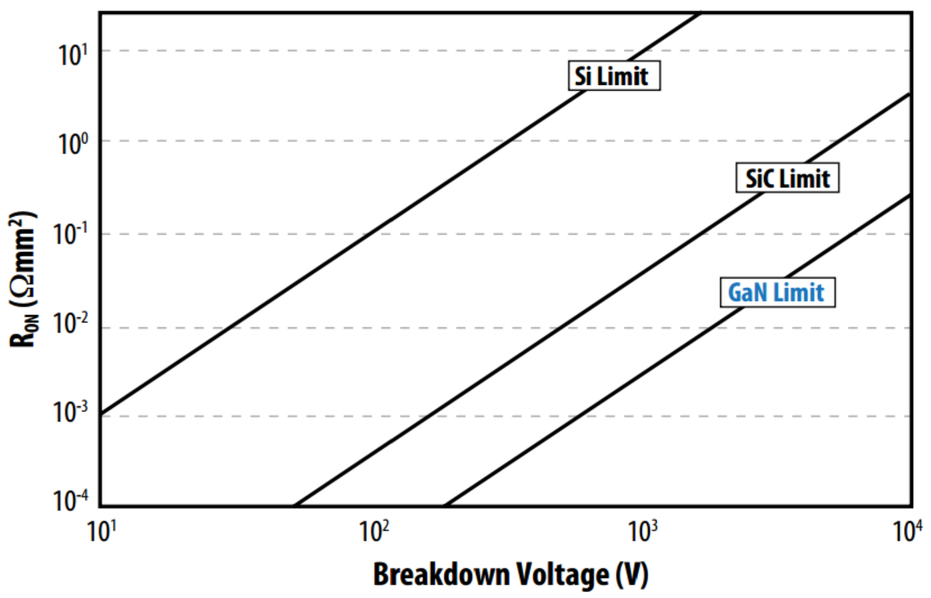


Figure 4: Theoretical Limits of GaN, Si, and SiC [21]

Market penetration by wide band-gap devices is still in the early phases. In many cases Si still dominates as its low price point due to mature fabrication techniques makes it difficult for expensive wide band-gap devices to compete. GaN is beginning to gain popularity in power electronics as it has been used in the optoelectronics industry for many years and that market has helped push the advancement of the technology. In addition, fabrication processes that allow for GaN to be grown on sapphire and recently on standard silicon wafers are giving GaN a large boost in the area of materials cost as SiC remains an order of magnitude more expensive to produce. These cost issues along with challenges in the manufacturing process have largely kept SiC out of the switch market, giving GaN an opportunity to gain market share. Table 3 describes some of the needs present in power electronics design and how GaN meets these needs [25].

Table 3: GaN Technology Advantages [25]

Need	Enabling Feature	Performance Advantage
High Power/Unit Width	Wide Band-gap, High Field	Compact, Ease of Matching
High Voltage Operation	High Breakdown Field	Eliminate/Reduce Step Down
High Linearity	HEMT Topology	Optimum Band Allocation
High Frequency	High Electron Velocity	Bandwidth, μ-Wave/mm-Wave
High Efficiency	High Operating Voltage	Power Saving, Reduced Cooling
Low Noise	High Gain, High Velocity	High Dynamic Range Receivers
High Temp Operation	Wide Band-gap	Rugged, Reliable, Reduced Cooling
Thermal Management	SiC Substrate	High Power Devices with Reduced Cooling Needs
Tech Leverage	Direct Band-gap Enabler for Lighting	Driving Force for Technology, Low Cost

Despite these advantages, GaN and SiC have both faced major issues in the penetration of the power electronics market. This difficulty was because of the nature of the materials, early switch devices that were fabricated from both materials were normally-on devices. While normally-on switches have their place, this is a disadvantage for most power electronics designs as additional circuitry would be needed in order to properly control these switches during operation, especially during startup sequences to ensure no short circuit faults occur before the switches can be driven into an off-state.

The first of these HEMT based depletion mode GaN devices grown on SiC appeared on the market in 2004, with the first HEMT GaN device on a Si substrate appearing in 2005. [21]. These devices were both RF transistors and GaN continued to gain more popularity in RF applications, but the difficulty in using depletion mode devices kept GaN from entering other markets, including power electronics. Usage of GaN remained confined to RF markets until the introduction of the first enhancement mode GaN device grown on a Si substrate, specifically for use as a power MOSFET, by Efficient Power Conversion (EPC) in June of 2009 [26].

EPC begins its manufacturing process with Si wafers using a process that is similar to typical depletion mode GaN devices. In typical devices, a layer of aluminum nitride (AlN) is grown on the Si wafer. This AlN layer serves as a base onto which the GaN can be grown. Once a suitable layer of GaN is present, a layer of AlGaN is added. Drain and source contacts are then added in a manner that pieces this AlGaN layer, creating Ohmic contacts to the two dimensional electron gas (2DEG) that exists below the AlGaN layer. This creates a short circuit between the drain and source that is the basis for the normally-on behavior of these devices. In order to control the device, a gate electrode is placed on the top of the AlGaN layer, which then depletes the 2DEG when a negative voltage is applied to it. Figure 5 shows a representation of the typical construction of a GaN device.

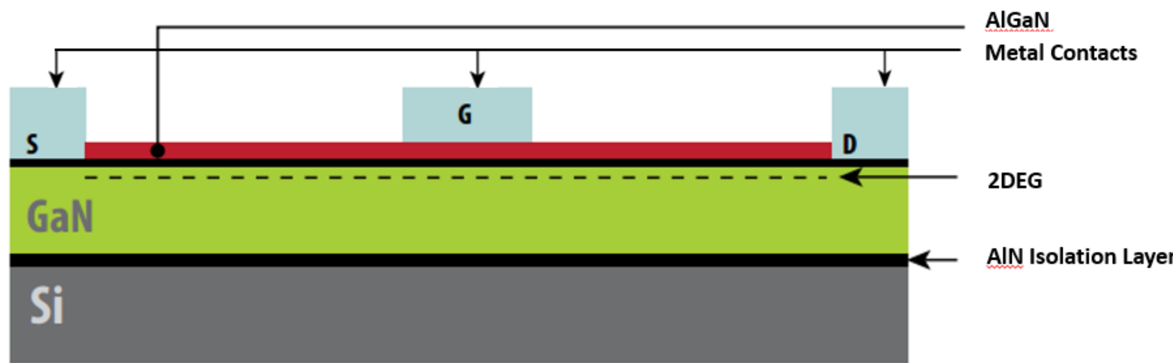


Figure 5: Typical GaN Device [26]

EPC's enhancement mode GaN devices utilize the same basic structure, but use a processing step to create a gate under the AlGaN layer. This creates a depletion region within the 2DEG. Appling a positive voltage to this gate structure then allows a channel to be reestablished within the 2DEG, creating the enhancement mode operation that is preferable for MOSFETs in

power electronics. The structure is then repeated laterally to create the eGaN device. Figure 6 shows a representation of this enhancement mode structure utilized by EPC.

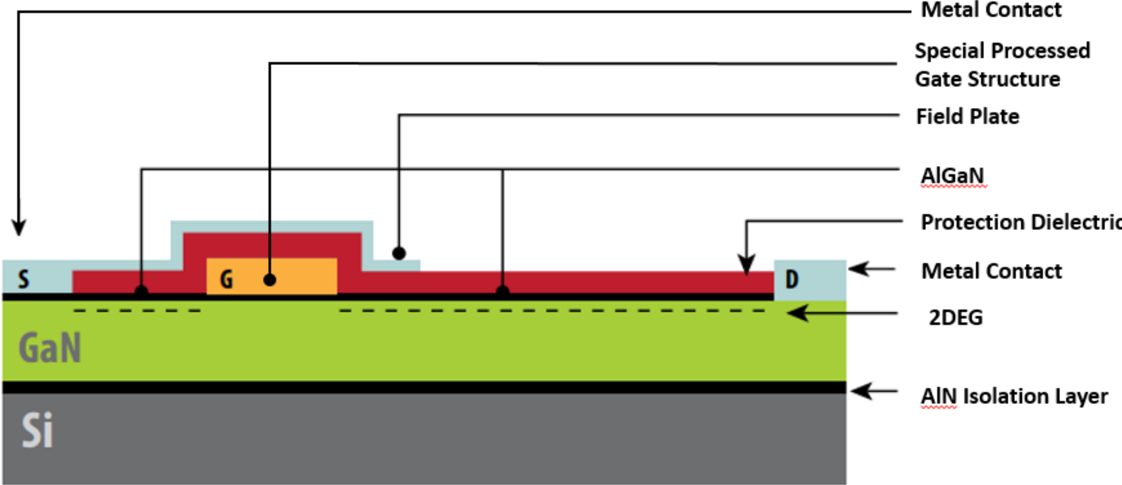


Figure 6: EPC eGaN Device [26]

The device structure implemented by EPC allows for the creation of devices that are well suited to power electronics. These eGaN devices have R_{ON} values and R_{ON} vs V_{GS} curves that are similar to Si MOSFETs but with lower temperature coefficients, allowing for easy substitution in many designs and for better performance in higher temperature environments. Drive requirements for EPCs eGAN devices are also similar to Si parts with an expected gate voltage of 4-5V. The threshold voltage is lower than typical Si devices, which requires careful design of the gate-source path to ensure the device transitions to fully off during high speed switching operation. High speed operation is enabled by low device capacitance, allowing the device to switch high power levels in the MHz frequency range. The eGaN structure has very low C_{GD} and C_{GS}, with C_{GS} being much larger than C_{GD} but still much smaller than comparable Si devices.

The structure of the eGaN device also creates a 'body diode' that operates similar to those present in Si MOSFETs, but with a larger forward voltage than in silicon transistors [26] that may necessitate the use of a circulation diode. Table 4 lists the metrics for several EPC devices and Table 5 compares EPC devices to similar Si devices.

Table 4: EPC Device Electrical Characteristics

Metric	**EPC2014** [27]	**EPC2015** [28]	**EPC2001** [29]
V_{DS}	40 V	40 V	100 V
I_D	10 A	33 A	25 A
V_{GS}	5 V	5 V	5 V
T_J	-40 to 150 ˚C	-40 to 150 ˚C	-40 to 125 ˚C
$R_{DS(ON)}$	12 mΩ	3.2 mΩ	5.6 mΩ
Q_G	2.48 nC	10.5 nC	8 nC
Q_{GD}	.48 nC	2.2 nC	2.2 nC
C_{OSS}	150 pF	575 pF	450 pF

Table 5: Comparison of Device Characteristics

Metric	**Infineon** [30] **BSC010NE2LS**	**NXP** [31] **PSMN5R6-100PS**	**TI** [32] **CSD17306Q5A**	**EPC** [28] **EPC2015**
V_{DS}	25 V	100 V	30 V	40 V
I_D	100 A	100 A	24 A	33 A
V_{GS}	5 V	5 V	5 V	5 V
T_J	-55 to 150 ˚C	-55 to 175 ˚C	-55 to 150 ˚C	-40 to 150 ˚C
$R_{DS(ON)}$	1.1 mΩ	4.3 mΩ	3.3 mΩ	3.2 mΩ
Q_G	64 nC	141 nC	11.8 nC	10.5 nC
Q_{GD}	6.8 nC	43 nC	2.5 nC	2.2 nC
C_{OSS}	1700 pF	561 pF	890 pF	575 pF
Package	TDSON-8	TO-220	SON 5mmx6mm	LGA 4.1x1.6
Area	$34mm^2$	$\geq 48.5mm^2$	$30mm^2$	$2.5mm^2$

From the performance data in Table 4 and Table 5 it is clear that the technology of GaN devices has reached a point where they have become a viable option for use in power electronics design as they are comparable to present generation silicon devices in all performance metrics and their small board footprint is an enabling characteristic for the next generation of high power density systems. It is believed that combining devices constructed on GaN technology with well executed circuit design and system control would allow for the creation of a high efficiency, high power density system capable of supporting the increasing power demands of current and future advanced processor systems.

Chapter 3 Design Goals and Approach

As datacenters grow larger with ever increasing power demands, the role of power system efficiency in the expected operational cost of a new facility has become more prevalent. This new attention has allowed big names in power supply design to bring new, more efficient products to market, but it has also forced facility planners to look at how to best utilize their new technology options to create the most cost effective system possible. It was from this line of thinking that Auburn University was brought in on a team with the University of Tennessee to help develop a power system for next generation datacenters. Auburn's role in this project consisted of two main tasks, first to evaluate wide band-gap devices for possible use in the various stages of the power system, and second, to develop a prototype Point of Load converter to meet the load requirements of the system processor.

3.1 Scope and Goals

At the inception of this project, a survey was performed on the current available solutions for datacenter power systems; some of the references discovered during this survey are discussed in Chapter 2. The results from this survey demonstrated that a DC distribution based system as shown in Figure 7 using wide band-gap technologies had the potential to produce a system with an overall efficiency as high as 90%, allowing for significant operational savings for a large facility. From this architecture the input and output requirements for Auburn's POL prototype were generated based on the anticipated designs for the primary and intermediate stages.

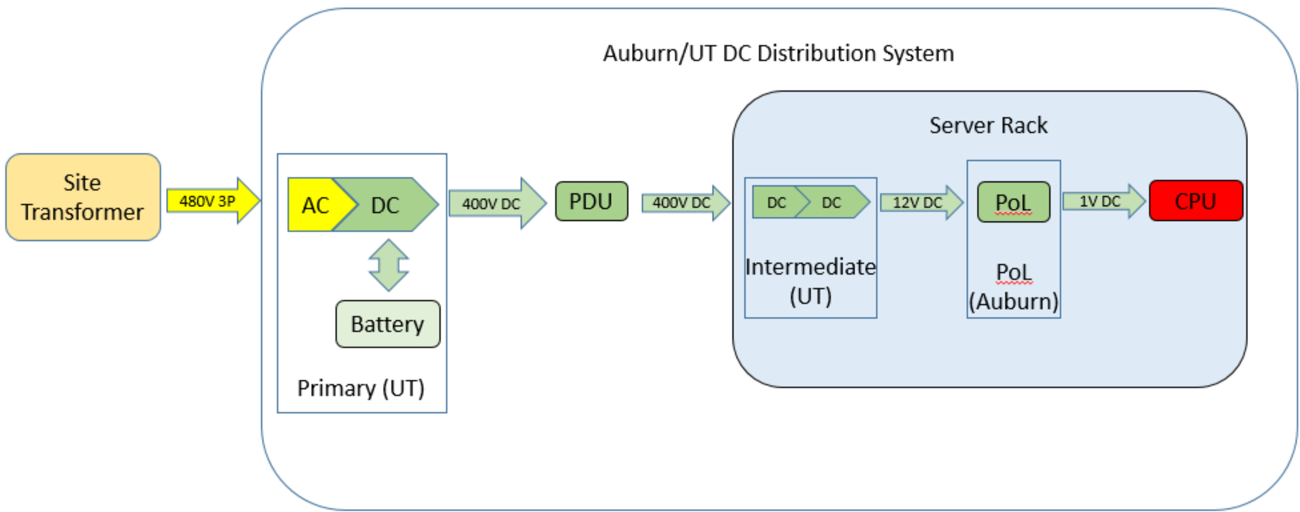


Figure 7: Auburn/UT DC Distribution System

The requirements for the POL portion of the power system were introduced to the project team and are shown in Table 6, with an additional goal of maintaining the highest power density possible in order to reduce design size to enable the POL supply to be placed directly on the CPU card. With these requirements in hand, the team began the process of selecting a converter design best suitable to meet these requirements while taking into account the specifications of the various devices currently on the market, including the wide band-gap devices that were being evaluated.

Table 6: Point of Load Design Objectives

Metric	Goal
Output Power	150 W
Input Voltage	12 VDC
Output Voltage	1 VDC
Output Current	150 A
Output Current Ripple	± 5%
Max Current Slew Rate	300 A/µs
Output Voltage Ripple	±30 mVDC

Several types of testing were done to evaluate the possible performance of a wide assortment of wide band-gap devices in the various sections of the power system. This testing included device performance metric characterization tests, switching tests, and reliability tests. From the conclusion of this testing and from a review of the literature on voltage regulator circuits, a traditional multiphase buck style converter was chosen in combination with several devices, those being the EPC eGaN devices, with the EPC2014 and EPC2015 being the primary devices under consideration for use within the POL stage.

3.2 Converter Selection

The traditional multiphase buck converter as shown in Figure 8 was chosen based on its simple design and its ability to operate well at both high and low load conditions. The buck topology is also able to maintain very high operating frequencies in order to handle potentially large transient load changes during operation, and still provide the tight output voltage regulation needed to meet the project goals [33] [34] [35] [36] [37]. The use of a multiphase system also provides advantages in that it allows for power phases to be deactivated during light load conditions, and by also providing for a measure of redundancy, allowing the system to continue operating at a reduced capacity should one phase encounter a failure.

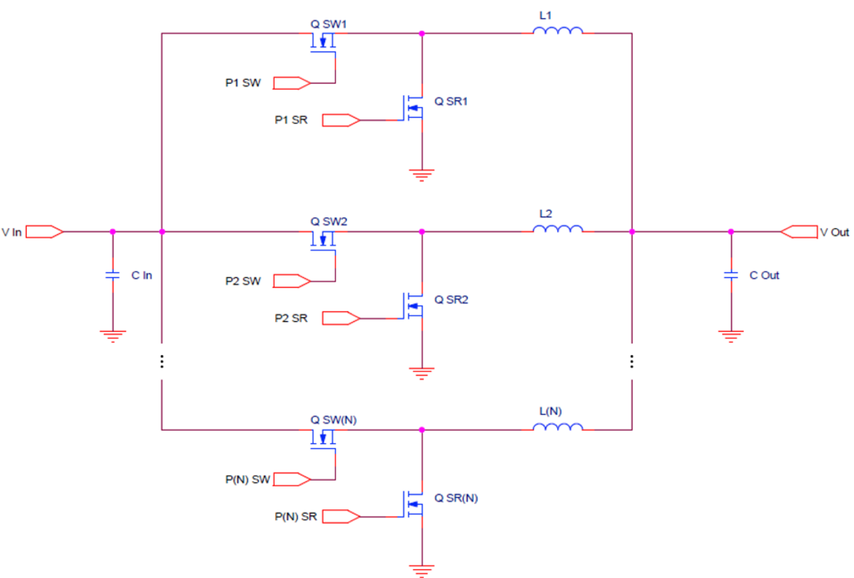


Figure 8: Typical Multiphase Buck Circuit

Other converter topologies such as switched capacitor [38] [39] [40] and other forms of both isolated and non-isolated resonant converters were considered [41] [42] [43] [44] [45] [46] [47] [48] [49], but many of these designs have technical limitations such as lower response rate, inability to handle large load swings, or require devices with such high current or voltage capabilities that the design would grow in physical size and not provide a reasonable power density figure in the final design.

The selection of the multiphase buck converter as the topology of choice guided the selection of the EPC eGaN parts for use as the high side switch and synchronous rectifier. Unfortunately the packaging used by EPC for these devices makes them difficult to prototype with, so the initial v1 design was done as a proof of concept for the buck topology using standard

Si technology parts in a more user friendly package that allowed for the project to make forward progress while an assembly method was being developed that allowed for these EPC devices to be populated in large numbers for testing and rapid prototype development.

Chapter 4 GaN Technology Implementation

With the decision to use the eGaN devices produced by EPC, a means of implementing the technology within the design was needed. Most typical power devices are produced in through-hole or large surface mount packages to aid in device cooling, which allows for very easy assembly operations either manually or through automated processes. The chip scale packages being utilized by EPC to aid in lowering device package parasitics and manufacturing cost are of a bumped die variety, which is very difficult to use in a prototype environment where automated assembly equipment may not be available. This created the need for a manual assembly method that would allow us to implement these eGaN devices in the POL design process and for device testing.

4.1 EPC Device Packaging

While the EPC eGaN devices offer better electrical characteristics than many other devices on the market, this level of performance does not come without a penalty. In order to achieve these values, EPC has chosen to package their devices as bumped die in an effort to avoiding the parasitics that are added when a device is packaged in a larger, more traditional package while also taking advantage of their high performance nature and lower cooling requirements by reducing their physical footprint. Table 7 shows an example of EPCs device packages compared to more traditional surface mount packages of devices with similar performance levels.

Table 7: Comparison of Device Packages [26]

<table>
<tr><th>Device</th><th>LGA package</th><th colspan="3">Equivalent MOSFET packages</th></tr>
<tr><td>40 V
4 mΩ max</td><td>4.1 x 1.6 mm</td><td rowspan="5">5 x 6mm PQFN</td><td>6.3 x 5 mm DirectFET</td><td>5 x 6 mm PolarPak</td></tr>
<tr><td>40 V
16 mΩ max</td><td>1.7 x 1.1 mm</td><td>4.8 x 3.9 mm DirectFET</td><td></td></tr>
<tr><td>100 V
7 mΩ max</td><td>4.1 x 1.6 mm</td><td></td><td></td></tr>
<tr><td>100 V
30 mΩ max</td><td>1.7 x 1.1 mm</td><td>4.8 x 3.9 mm DirectFET</td><td></td></tr>
<tr><td>200 V
100 mΩ max</td><td>1.7 x 0.9 mm</td><td>6.3 x 5 mm DirectFET</td><td>5 x 6 mm PolarPak</td></tr>
</table>

In many applications, these additional parasitics do not affect the device or the circuit negatively as the parasitics are minimal when compared to the characteristics of the device itself. However, the eGaN devices produced by EPC are low loss and the addition of a larger package would reduce the performance level of these devices due to the increased package inductance, capacitance, and resistance. The decision by EPC to use the device with minimal packaging after being diced from the wafer as a bumped die chip scale package (CSP) removes the possibility of

reduced device performance due to package characteristics, providing the engineer with the best foundation possible to begin their design.

While this provides the engineer with a device with outstanding electrical characteristics, the decision to use a bumped die CSP, as seen in Figure 9, may generate some difficulties during the assembly process. Due to the size and material composition of the device, automated assembly is the recommended means of assembly in order to ensure proper alignment and placement of the small device and to ensure that the rather fragile silicon substrate the device is built upon does not fracture during handling. Unfortunately, automated assembly of prototype level designs may not be feasible due to the time and costs involved with processing a design when compared to what can be accomplished manually by a skilled technician. As a result of this, a manual method must be developed that allows for rapid assembly while maintaining appropriately high levels of die attachment quality and process uniformity and repeatability.

Figure 9: Chip Scale Packaging used by EPC on a U.S. penny

4.2 Manual Assembly

EPC has made an effort to assist the engineer with prototype assembly by publishing guidelines for a manual assembly approach that requires precision silkscreen markings to aid in part alignment while using a hot air reflow process for die attachment [50]. This method is outlined below and Table 8 lists the materials needed.

Table 8: EPC Recommended Equipment and Materials

Item	Process Group
Anti-Static Mat, ESD wrist strap, ESD lab coat, ESD gloves	ALL
Hot Plate or IR PCB Heater	Prep
Tacky Flux	Prep, Placement, Alignment
Compatible Solder, spool	Prep
Microscope	Prep
ESD Safe tools	ALL
Reflow Oven	Reflow
X-Ray Inspection	Alignment, Inspection
Flux cleaning agent	Prep, Inspection
Soldering Iron	Prep

This method, while being relatively simple, does not generate highly reliable or consistent results, primarily due to deviations in die placement and lack of post assembly inspection to check for defects. An alternative was needed to ensure consistent and highly reliable assembly for use in these high power prototype circuits.

In response to the issues found with the recommended process, a new method was developed to take advantage of the advanced assembly technology available to our project, while still allowing for a fully manual process that allows for very rapid assembly while maintaining the high levels of quality and uniformity necessary for prototype development of high efficiency

power converters. This method has proven itself after the assembly of many hundreds of devices and was published in [51], with less than 1% of these devices requiring rework after the initial assembly process. This process allows for defects to be found and corrected before the affected prototypes advance any further in the assembly process, preventing the significant effort needed to rework the defective devices once a circuit assembly had been fully completed. This method relies on the use of two specific pieces of equipment that may or may not be readily available to most research groups, an X-Ray inspection tool and a multi-zone reflow oven. In an effort to make this method more accessible to other groups that may wish to use these devices in a similar manner who do not have the required equipment available, a secondary method was developed that uses alternative equipment that may be more accessible for those institutions.

4.3 Primary Manual Assembly Method

The primary manual assembly method used in this work generates a high quality solder attachment while being a very rapid process that allows for many assemblies to be built in a short amount of time. This is accomplished through process implementations that take advantage of the material properties of solder and flux to ensure a reliable final product. The required equipment and materials for this process are listed in

Table 9. As in the original EPC process, ESD and material handling precautions must be taken into account to ensure the die are not damaged physically or electrically during the process. It is also highly recommended that this process be completed start to finish before any other components are attached to the assembly.

This process is broken down into five separate process groups as shown in

Figure 10. These groups may be assigned to separate operators and assemblies should move through the groups in a linear fashion. If a large number of assemblies are to be processed through at a given time, it is recommended that they be done in batches and passed through each process group as a batch instead of individually, unless a specific assembly requires extra attention. The PCB device footprint used in this process is a rectangular version of the standard PCB pad listed for each footprint. It is highly recommended that the PCB designer use the recommended pad layout as deviations could result in assembly defects or failures during device operation.

Figure 10: Process Groups

Table 9: Required Equipment and Materials

Item	Process Group
Anti-Static Mat, ESD wrist strap, ESD lab coat, ESD gloves	ALL
Hot Plate or IR PCB Heater	Prep
Tacky Flux	Prep, Placement, Alignment
Suitable Solder, spool	Prep
Microscope	Prep
ESD Safe tools	ALL
Reflow Oven	Reflow
X-Ray Inspection	Alignment, Inspection
Flux cleaning agent	Prep, Inspection
Soldering Iron	Prep

4.3.1 Preparation

The preparation portion of the process establishes a foundation onto which the following steps are built. Proper completion of the preparation portion is vital to ensure proper finished assembly quality. The preparation process can be completed in advance and the PCB's stored without any degradation to the process, although another cleaning step would be recommended to ensure no contaminates are present on the substrate before beginning the placement process. The preparation process is explained in detail below:

1. Ensure the operator is aware of and follows proper ESD protocols.
2. Place the following materials and equipment within easy reach of the operator: hot plate, flux, solder, soldering iron, flux cleaning agent, microscope
3. Place the hotplate/IR heater in the work area beneath the microscope.
4. Warm the assembly PCB to approximately 120°C-150°C. This temperature is dependent on the substrate used and the operator should ensure that it remains below the glass transition temperature of their substrate. Increasing the temperature beyond 150°C may yield some improvement in process completion time, but it is not advisable to exceed the published value for the substrate being used or the operator risks placing unneeded stress on the substrate.
5. Place a small amount of flux on the pads of the parts being assembled.
6. Using a small tip on the soldering iron, add a small amount of solder to each individual pad of the device footprint. There should be sufficient solder to raise the pad and form a convex surface, but not enough to cause a bridge to another pad. It is recommended that the operator attempt to achieve a uniform shape across all pads. The operator should also ensure that the solder being used is compatible with the solder used by EPC to create the

solder bumps on their devices. An incompatible alloy could generate future reliability issues.

7. Allow the PCB assembly to cool.
8. Clean any remaining flux off of the PCB assembly.
9. Visually inspect the ‘bumped’ footprint pads looking for any defects or voids in the solder areas. Any defects should be corrected before proceeding, followed by an additional cleaning step. An example of an appropriately bumped footprint can be seen in Figure 12 compared to the preprocessed footprint in Figure 11.
10. If a double sided design is being assembled, it is recommended that any device pads that exist on the back side be put through the prep process before the assembly is advanced any further.

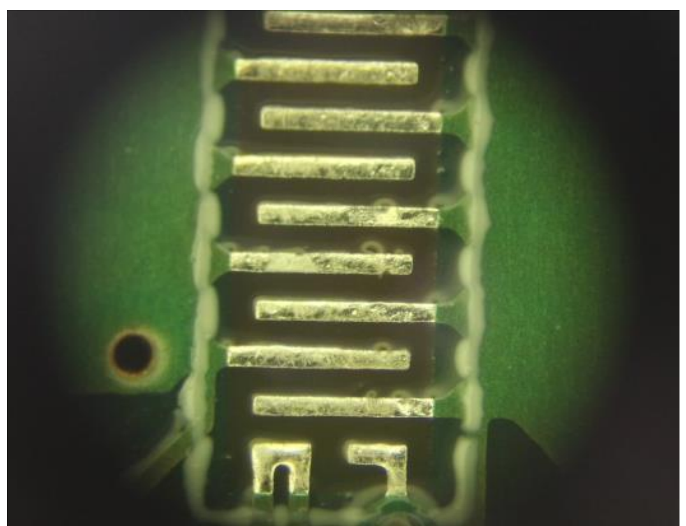


Figure 11: Footprint before pads are 'bumped'.

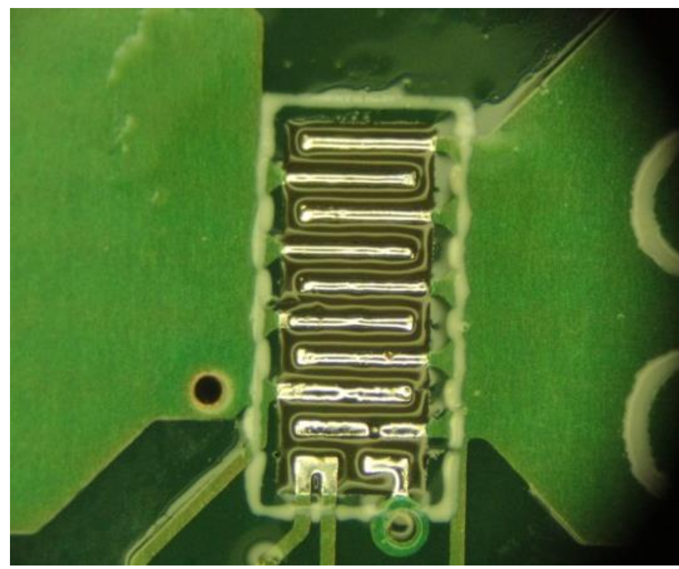


Figure 12: Correctly ‘bumped’ footprint pads.

4.3.2 Placement

The placement process is relatively simple and may be accomplished very quickly. If only a small volume of assemblies are to be made, this process can be combined with the Prep process at a single workstation. The process steps are listed below:

1. Ensure the operator is aware of and follows proper ESD protocols.
2. Ensure the PCB assembly is clean before beginning.
3. Place a small amount of tacky flux on the device footprint as shown in Figure 13. A water soluble flux is recommended for this step to aid in cleaning. RF771 tacky flux by Kester has been used successfully for this process. Tacky flux is used as it aids the operator by preventing the device from shifting should the PCB assembly be subjected to a minor bump during these processes. This step can be done for all devices on the same side of the board.

4. Using a set of ESD-safe fine tweezers, remove the device from its packaging and check for device orientation. The operator should be careful not to exert an excessive amount of force on the device as its exterior is very fragile and even small fractures can cause electrical malfunctions or reduce overall device performance and reliability.
5. Using the tweezers, place the device in its appropriate orientation in the flux over its pads.
6. The operator should visually align the part to the best degree possible, taking into account visual discrepancies generated by the flux.
7. Using very light pressure, the operator should ensure the device is making contact with the footprint pads and is not floating on the flux.
8. If a double sided design is being processed, the first side must be advanced through the rest of the process before the second side can be done.

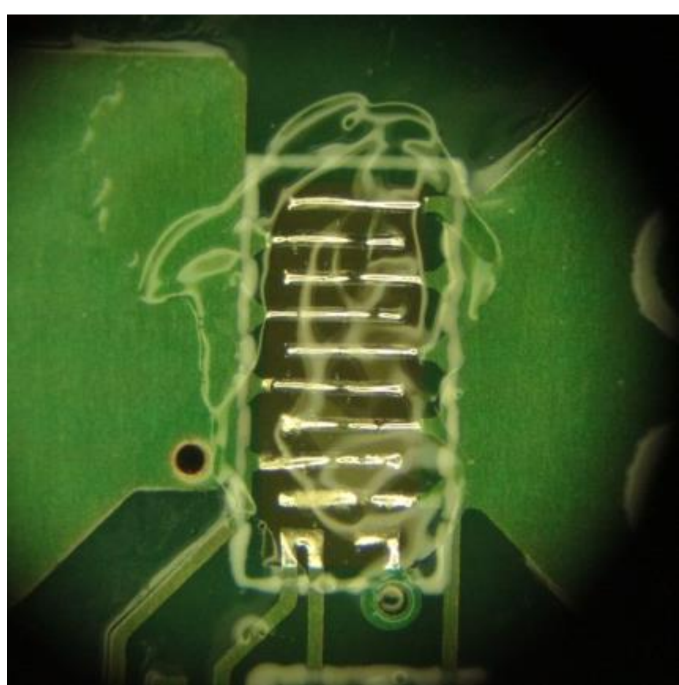


Figure 13: Footprint after tacky flux application.

4.3.3 Alignment

The alignment process is done utilizing an X-Ray inspection device, specifically the Phoenix X-Ray pcba|analyser [52]. This machine allows the operator to exactly align the device solder bumps with the pads on the PCB assembly, generating a very high quality solder joint once sent through the reflow process. This portion of the process is vital to the quality of the solder joint and under no circumstances should any deviations from this process be done to accelerate the process unless the operator can ensure that no defects will be generated. If the alignment process is not done correctly and the assembly is sent through the reflow process it can be very difficult to remove and rework the device without damaging the PCB assembly if defects are then found in the inspection process. The alignment process is detailed below:

1. Ensure the operator is aware of and follows proper ESD protocols.
2. Place the PCB assembly in the X-Ray machine to achieve a top down view of the device. If several assemblies are to be processed, they may be inserted together, assuming the machine has a large enough capacity. It is recommended that the devices be placed on some kind of tray to make handling easier for the operator. If the reflow oven to be used has an X-ray compatible tray, it is advised to use it to help reduce the chances of the devices shifting after alignment while the assemblies are being moved.
3. Energize the X-Ray using appropriate safety measures for the particular machine being used. Under no circumstances should an untrained operator attempt to use the machine without proper supervision.

4. With the machine energized, zoom into the relevant device area of the assembly and adjust the settings on the machine until a clear view of the device and its footprint is achieved.
5. If the device is not aligned appropriately, the operator will see separation between the device and the PCB footprint as shown in Figure 14. If the device is appropriately aligned there will be very little or no distinction between the device and its footprint as seen in Figure 15. While it is not required to have a perfect overlap between the device and its footprint, it is recommended that any Theta offset be kept to the barest minimum and that there be no more then 1/4th of the narrow length of the pad offset in the corresponding dimension and no more then 1/4th of the wide length of the smallest pad on the device in the corresponding dimension. If the operator allows for any offsets larger than this, the risks of possible defects later in the process greatly increases.
6. De-energize the X-Ray machine and make any adjustments necessary to bring questionable devices within appropriate alignment tolerances. It is recommended to adjust devices using very light pressure on the side of the device package using a set of tweezers. The operator should be aware that the device will tend to want to sit with its solder bumps between the bumps on its footprint pad, and it may take a slightly larger amount of force to adjust the device so it is sitting on the top of the pads appropriately.
7. If the assembly contains more than one device, view and adjust them separately, ensure that all previously aligned devices are checked after the last device has been adjusted.
8. De-energize the X-Ray machine and remove the assembly from the machine.

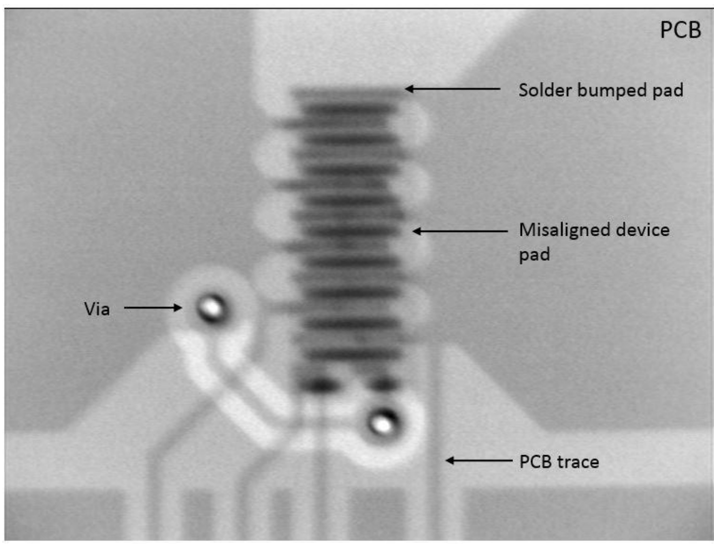


Figure 14: X-Ray image of misaligned device.

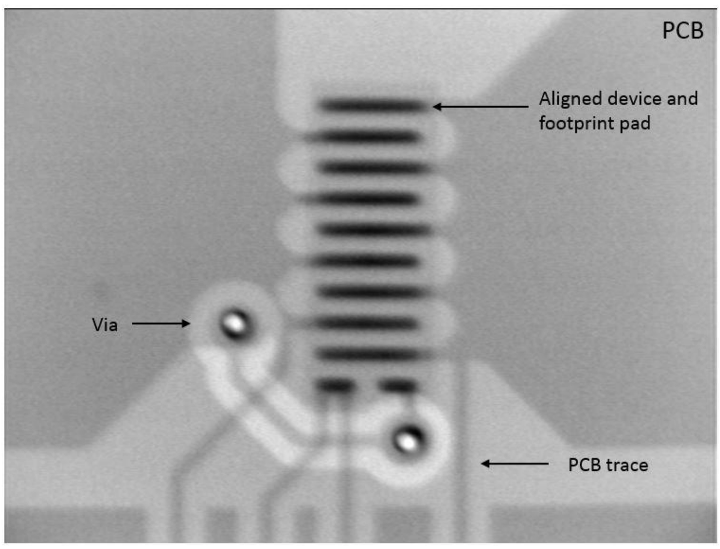


Figure 15: X-Ray image of properly aligned device.

4.3.4 Reflow

The reflow process should not require much input from the operator beyond the initial creation of the reflow profile for the oven being used. It is recommended that this profile be

generated to correspond with the information provided by EPC for the solder alloy used on their devices. If the solder alloy that was used in the prep process requires a profile that differs significantly from what EPC recommends for their devices, it is recommended that the operator contact both EPC and the solder manufacture for input before proceeding. In this case a Heller 1800ESL nine zone reflow oven is being used with a general lead free solder reflow profile that is compatible with the EPC devices. The reflow process is outlined below:

1. Ensure the operator is aware of and follows proper ESD protocols.
2. Program the reflow oven to match the profile specified by EPC or a suitable alternative.
3. Ensure the oven has achieved proper operating temperatures before sending through any assemblies.
4. Place the assemblies in the oven directly or on a suitable carrier tray. If a carrier tray is used, it is recommended that temporary standoffs be placed under the board to ensure that no adhesion between the bottom side solder pads and the tray or between any excessive flux on the substrate and the tray takes place.
5. Allow the assembly to cool once exiting the oven.

4.3.5 Inspection

The inspection process is the last step and ensures that no assemblies are allowed to proceed if there are any placement defects with the devices. Extra care is recommended to ensure that all assemblies are of appropriate quality as these CSP devices are exceedingly difficult to rework once the entire circuit has been assembled, often requiring that the entire assembly be scrapped. Even if the assembly can be reworked successfully, the operator must be mindful of the fact that an assembly can only be put back through the process a finite number of times

before substrate and circuit component degradation may begin to occur. The inspection process is described below:

1. Ensure the operator is aware of and follows proper ESD protocols.
2. Clean the assembly with an appropriate flux cleaner to remove any remaining residue. While thorough cleaning can be accomplished through several methods, a combination of rinsing and ultrasonic cleaning has proven to be very effective in removing any flux residue. It is also recommended that the assembly be baked according to the flux manufactures specifications to ensure full cure of the flux to prevent the possibility of dendrite growth between pads, resulting in device and circuit failure once the assembly is in operation.
3. Visually inspect the device for any physically damage and for any obvious signs of misalignment.
4. Using the X-ray machine from the alignment phase, check the device for proper alignment with the device footprint as in Figure 16. A misaligned device is usually visually obvious, but the operator should be aware that a shift in the long axis of the part could cause the part to sit properly on its pads, but with a one pin offset. This type of misalignment may not be easy to spot depending on the settings of the X-Ray, so the operator should verify that the correct number of pins is visible to ensure proper alignment.
5. If any defective devices are found, it is recommended that a hot air tool be used to remove the devices to prevent any damage to the device footprint from physical contact by the operator. Once the device has been removed, it is recommended that the PCB

assembly be taken back to the prep phase of the process in order to ensure the replacement device is attached correctly.

6. It is recommended that once these devices have been verified by X-ray to be properly assembled that they be affixed to the substrate using an adhesive to ensure that they do not shift during any future assembly stages that they may be subjected to, such as the population of the bottom side of the board. The 'Chip Bonder' #3621 adhesive manufactured by Loctite has proven to be acceptable for this purpose. Ensure that any instructions from the manufacturer relating to proper curing of the adhesive are followed.

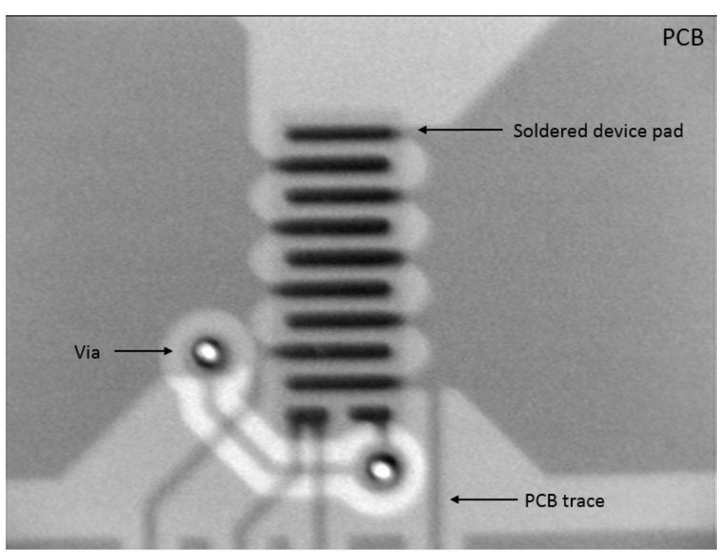


Figure 16: X-Ray image of properly soldered device.

Assuming that all previous steps are followed appropriately, the resulting assembly should be of the quality needed to ensure that there are no circuit failures that can be attributed to defective solder joints. Should the designer experience any issues that can only be traced back to the assembly process, it is recommended that they double check their conformance to any unique requirements of the materials they may be using. It is also recommended they insure proper

compatibility between PCB assembly plating, solder used to bump the device footprint, and the solder on the device itself with the temperature profile of the reflow oven. If the PCB assembly being processed contains many layers or if it contains higher density copper, the temperature profile may need to be adjusted to ensure that both the board and the device are achieving the required temperatures for the solder process.

4.4 Secondary Manual Assembly Method

The secondary method created for the assembly of these CSP EPC devices evolved from a need for an attachment solution that did not require the use of an X-Ray machine for part alignment. The X-ray machine, while allowing for very precise part placement, is a very complex and expensive piece of equipment that may not be available to many groups that wish to use these EPC devices in their projects. As discussed previously, EPC provides a solution for part placement that does not rely on an X-ray machine, but the quality and repeatability of the assembly process is not up to the levels required for these power stage prototypes. This method is the result of an effort to try and create a compromise between the two assembly techniques that allows for high quality assemblies while using more commonly available equipment.

This secondary method can be implemented with several different types of machine, but they all carry one common element necessary for this process, split optic alignment. Split optic alignment presents the viewer an overlapping view of the device footprint on the PCB as well as a view of the bottom of the pads on the device. This overlapping view allows the operator to adjust the relative position of the device versus the board to ensure that the device is in perfect alignment with its footprint on the board. The implementation of this alignment step will be relatively universal across all machines with this capability, but depending on the machine, the

reflow step may be accomplished by the machine after alignment, instead of requiring the assembly be removed and sent through a separate reflow oven. A machine such as a BGA rework machine would allow the operator to accomplish the alignment and reflow steps with a single machine, while a manual placement split optic machine will also allow for proper placement, but will require the operator to send the assembly through the reflow oven once alignment is complete. The materials and equipment needed for this method are given in Table 10 followed by a description of the procedure.

Table 10: Secondary Method Materials and Equipment

Item	Process Group
Anti-Static Mat, ESD wrist strap, ESD lab coat, ESD gloves	ALL
Hot Plate or IR PCB Heater	Prep
Tacky Flux	Prep, Placement, Alignment
Suitable Solder, spool	Prep
Microscope	Prep
ESD Safe tools	ALL
Reflow Oven	Reflow
Split Optic Placement Machine	Placement, Alignment
Flux cleaning agent	Prep, Inspection
Soldering Iron	Prep

4.4.1 Preparation

The preparation phase for this process is almost identical to the new method presented above. The operator may need to adjust the amount of solder added to the bumped pads based on the results of the reflow process.

1. Ensure the operator is aware of and follows proper ESD protocols.

2. Place the following materials and equipment within easy reach of the operator: hot plate, flux, solder, soldering iron, flux cleaning agent, microscope
3. Place the hotplate/IR heater in the work area beneath the microscope.
4. Warm the assembly PCB to approximately 120°C-150°C. This temperature is dependent on the substrate used, and the operator should ensure that it remains below the glass transition temperature of their substrate. Increasing the temperature beyond 150°C may yield some improvement in process completion time, but it is not advisable to exceed the published value for the substrate being used or the operator risks placing unneeded stress on the substrate.
5. Place a small amount of flux on the pads of the parts being assembled.
6. Using a small tip on the soldering iron, add a small amount of solder to each individual pad of the device footprint. There should be sufficient solder to raise the pad and form a convex surface, but not enough to cause a bridge to another pad. It is recommended that the operator attempt to achieve a uniform shape across all pads. The operator should also ensure that the solder being used is compatible with the solder used by EPC to create the solder bumps on their devices. An incompatible alloy could generate reliability issues further down the line.
7. Allow the PCB assembly to cool.
8. Clean any remaining flux off of the PCB assembly.
9. Visually inspect the ‘bumped’ footprint pads looking for any defects or voids in the solder areas. Any defects should be corrected before proceeding, following by an additional cleaning step.

4.4.2 Placement and Alignment

The placement and alignment portion of this process differs in that both steps are combined, using the vacuum pickup and the split optic alignment to align and place the device in one step. The placement phase still includes the application of flux as described in the first method. Alignment of the device is accomplished in conjunction with placement as the split optic system aligns and then places the part. Alignment is accomplished by movement of the device in X, Y, and Theta orientations to match the orientation of the device footprint on the PCB assembly. Should the flux cause issues with viewing of the device footprint, it is advised that the operator thin out the flux layer to make the pads more visible. Should the solder bumps on the pads cause difficulties with placement once the flux has been thinned, the operator may need to reduce the amount of solder applied to the pads.

1. Ensure the operator is aware of and follows proper ESD protocols.
2. Ensure the PCB assembly is clean before beginning.
3. Place a small amount of tacky flux on the device footprint as shown in Figure 13. A water soluble flux is recommended for this step to aid in cleaning. The RF771 tacky flux by Kester has been used successfully for this process. Tacky flux is used as it aids the operator by preventing the device from shifting should the PCB assembly be subjected to a minor bump during these processes. This step can be done for all devices on the same layer of the board.
4. Program/setup the machine with an appropriate reflow profile to match the recommended solder manufacturers profiles.
5. Using a set of ESD-safe fine tweezers, remove the device from its packaging and check for device orientation. The operator should be careful not to exert an excessive amount of

force on the device as its exterior is very fragile and even small fractures can cause electrical malfunctions or reduce overall device performance and reliability.

6. Using the tweezers, place the device in a matching orientation to its footprint on the staging section of the vacuum pickup.
7. Activate the vacuum pickup and lift the part from the staging area.
8. Align the device with its footprint in X, Y and Theta orientations. Ensure that the overlap shown in the optic system has not been distorted by the flux on the PCB.
9. Activate PCB heater/back heater if available. Bring the PCB to ~150°C before proceeding. This temperature may vary depending on substrate used, ensure that a proper temperature is chosen for the materials used.
10. Activate the placement operation of the machine. Ensure that the placement head does not exert an excessive amount of pressure on the device as this could lead to fractures in the device and electrical failure during operation.
11. With the device placed, the placement head can now be retracted and the hot air nozzle moved into place or the board removed from the machine for the reflow profile.

4.4.3 Reflow

The reflow process will vary depending on the type of split optic machine being used as some machines may or may not have a built in heating element. If the machine being used does contain a suitable heated section, the reflow process can be done directly after placement and alignment without removing the PCB from the machine, reducing the risk of disturbing device placement. Using the documentation for the machine being used, a suitable reflow profile must be programmed into the machine. For machines utilizing hot air as the primary medium for heat

transfer it is recommended that the air flow be reduced to a suitable level to ensure that the device does not get blown off of its pads. Machines that contain a back plate heater, usually infrared, are preferred for this step as it allows for a reduction in the amount of hot air necessary to reflow the solder.

1. Ensure the operator is aware of and follows proper ESD protocols.
2. Ensure the machine has a proper reflow profile programmed. If a reflow oven is to be used, ensure it is at the appropriate temperature before sending the PCB assembly through.
3. If the hot air capabilities of the placement machine are to be used, with the device placed on its pad, activate the reflow process of the machine. Make sure that the airflow of the machine is minimized to ensure the part does not blow off the pad. If a reflow oven is to be used, place the assemblies in the oven directly or on a suitable carrier tray. If a carrier tray is used, it is recommended that temporary standoffs be placed under the board to ensure that no adhesion between the bottom side solder pads and the tray or between any excessive flux on the substrate and the tray takes place. Allow the assembly to cool after the reflow process.

4.4.4 Inspection

The inspection phase of this method differs from the previous method in the lack of X-Ray inspection. It is still recommended to X-Ray devices if possible to ensure proper placement, but if an X-Ray is unavailable, a reasonable high quality inspection can be done using high magnification optical inspection of the side view of the device to check for proper alignment after the reflow process. Proper cleaning and curing of any remaining flux or other materials

resulting from the solder process is also highly recommended to ensure that there are no materials left on the PCB that could cause a device failure once the assembly is placed into operation.

1. Ensure the operator is aware of and follows proper ESD protocols.
2. Clean the assembly with an appropriate flux cleaner to remove any remaining residue. It is also recommended that the assembly be baked according to the flux manufactures specifications to ensure full cure of the flux to prevent the possibility of dendrite growth between pads, resulting in device and circuit failure once the assembly is in operation.
3. Visually inspect the device for any physical damage and for any obvious signs of misalignment.
4. Using the X-Ray machine if available or high magnification optical inspection, ensure that the device is appropriately aligned with its footprint. If using optical inspection, it may be advantageous to view the device from the side to check for alignment between the footprint pads and the device pads.
5. If any defective devices are found, it is recommended that a hot air tool be used to remove the devices to prevent any damage to the device footprint from physical contact by the operator. Once the device has been removed, it is recommended that the PCB assembly be taken back to the prep phase of the process in order to ensure the replacement device is attached correctly.
6. It is recommended that once these devices have been verified by inspection to be properly assembled that they be affixed to the substrate using an adhesive to ensure that they do not shift during any future assembly stages that they may be subjected to, such as the population of the bottom side of the board. The #3621 adhesive manufactured by Loctite

has proven to be acceptable for this purpose. Ensure that any instructions supplied by the manufacturer relating to proper curing of the adhesive are followed.

Chapter 5 Point of Load Version 2

The implementation of a GaN based synchronous buck converter began with the design of version 2 of the POL prototype boards. Earlier versions of the design were done with Si based parts using an asynchronous topology, with version 0 being a breadboard design and the version 1 modular components being manufactured to our designs by Advanced Circuits. Figure 17 shows an assembled single phase version 1 design, including control, load, regulator, and power input boards. A circuit schematic and gerber files for the version 1 design are available in Appendix A and B. Lessons learned from these early designs were applied in the development of the version 2 board as the design was transitioned to a GaN based synchronous converter.

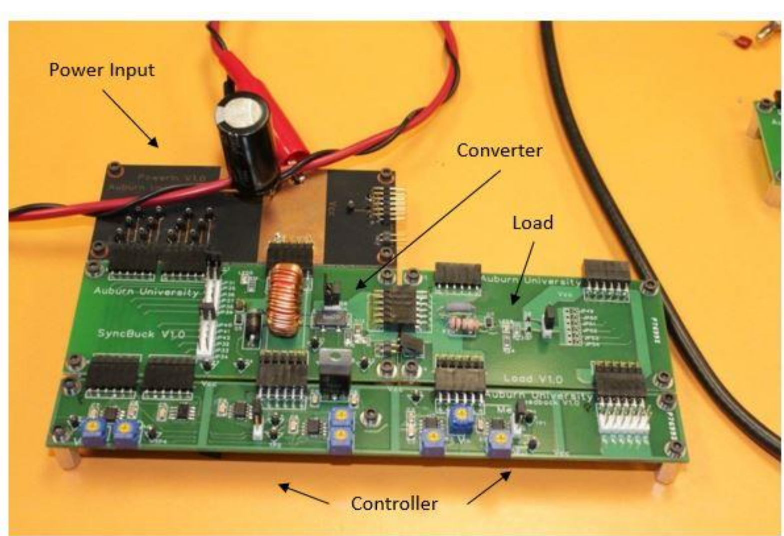


Figure 17: Assembled Version 1 Buck Converter

5.1 Design

The Version 2 of the POL design was the first effort into implementing a synchronous buck converter utilizing advanced technology GaN devices in place of the more commonly used Si devices. As previously mentioned, these GaN devices offer the potential for dramatic efficiency improvements over Si devices in converter applications due to their lower $R_{DS(ON)}$, fast switching capabilities, low gate charge, and reduced package parasitics. In order to achieve this, it was decided to implement the eGaN devices produced by EPC in a multi-phase asynchronous buck topology.

There are two main aspects of each V2 buck board, the controller and the power stages. The design of the controller and the control algorithm was an important part of the design as the selection of a suitable microprocessor to allow for continued design updates as the design team became more knowledgeable about the system greatly influenced device selection. The microprocessor chosen for controller development was the Mircochip dsPIC30F2023 [53]. The selection of this microprocessor placed a restriction on the design due to the number of IO lines available for control and sensing of the converter power stages. This restricted the converter design to having only four power phases.

In preparation for possible future expansion of the controller hardware requirements and to allow for more flexibility on the controller side of the design, the design team decided to augment the microprocessor with the addition of an external interface that would allow for the connection of an external FPGA board, should the control algorithm develop to the point where the microprocessor was no longer capable of controlling the system. A set of bypass jumper pins were added between the microprocessor and an external interface that would allow for the connection of a Digilent Atlys FPGA board [54]. This would allow for the FGPA to take direct

control of the gate drive lines for all four converter phases should the algorithm development for system control reach the point where an FPGA became necessary. Voltage sense lines for the individual phase nodes and load voltages were not made available to the external FPGA connector. A jumper connection between the FPGA connector and the dsPIC was created to allow this status information to be shared, should the control develop to the point where the FPGA became required. In such a situation, the dsPIC would act as an ADC and supply the FPGA with information on circuit state while the FPGA then creates the PWM signal to drive the switching components. The circuit schematic for the dsPIC and FPGA portion of the controller is shown in Figure 18, with the full circuit schematic available in Appendix C.

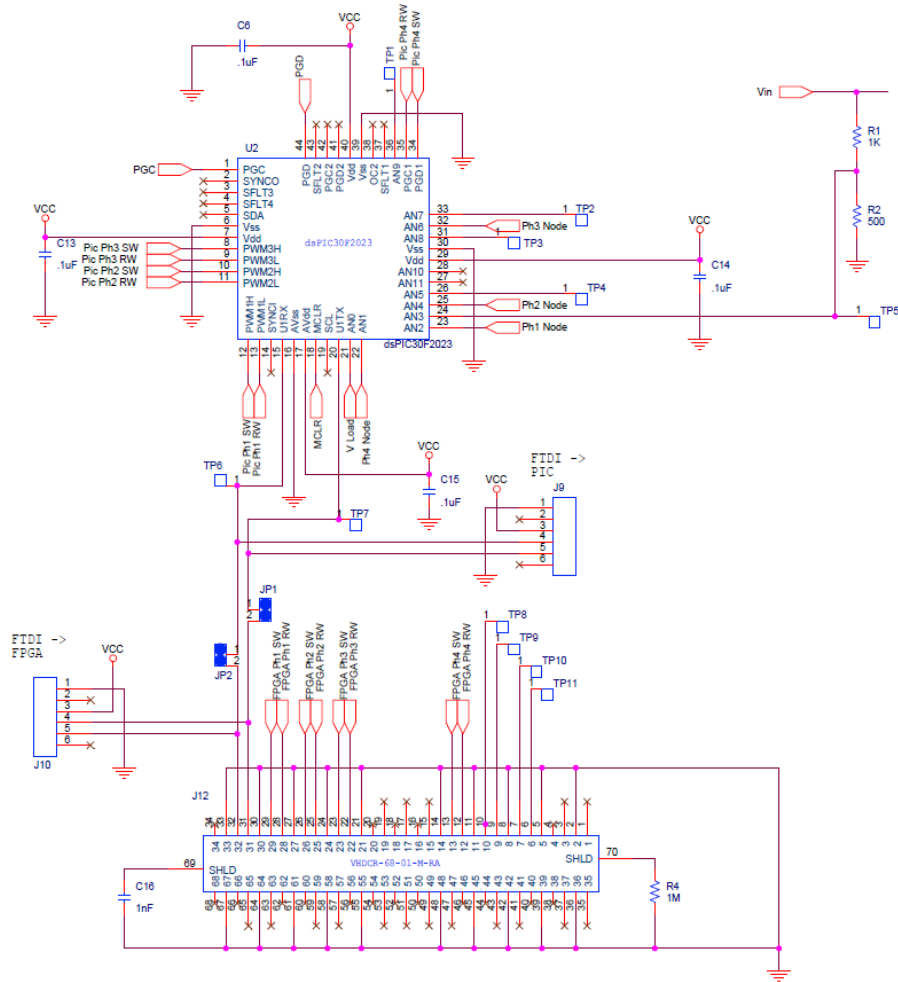


Figure 18: Version 2 Controller, FPGA Interface & dsPIC

Selection of the components for the power stages began with reviewing available data on EPC’s device offerings. Previous testing of EPC’s eGaN devices provided the team with additional data on the available devices and their capabilities. Two devices are needed for the synchronous buck topology, as described previously, a voltage switch and a synchronous rectifier. A device used for the voltage switch needs to have low gate charge to allow for fast switching with low losses, while the synchronous rectifier needs to be able to handle higher current peaks. Based on this, the devices chosen for version 2 were the EPC2014 [27] for the

high side voltage switch primarily due to its low gate charge, and the EPC2015 [28] for the low side synchronous rectifier primarily due to its smaller $R_{DS(ON)}$ and increased current capacity. Table 11 provides a comparison between the specifications of these two devices. With the chosen devices, the power stage was expected to be capable of ~20A output per phase.

Table 11: Device Electrical Characteristics

	EPC2014	**EPC2015**
$R_{DS(ON)}$	12 mΩ	3.2 mΩ
Q_{gate}	2.48 nC	10.5 nC
V_{GS}	5 V	5 V
V_{DS}	40 V	40 V
I_D	10 A	33 A
C_{OSS}	150 pF	575 pF

With the selection of the controller and the eGaN switches for the converter accomplished, a suitable drive circuit was needed to ensure proper interface between the controller and the switches. Component selection was driven by the need to supply the EPC devices with suitable gate currents to ensure proper turn on, while providing the necessary reference to each switch's source terminal to prevent an overvoltage condition on the gate. The EL7158 [55] gate driver from Intersil was chosen as the driver for the switches due to its fast response, large current capabilities, and level shifting abilities, as well as its use in EPC reference designs for their GaN devices. A LTC4440-5 [56] driver chip from Linear Technologies was also added to the design to ensure proper gate drive reference voltage levels from the controller for the high side switch and its EL7158. A diode was added to the voltage input of the gate drive

circuitry for each phase to prevent transients from affecting other converter phases. The resulting gate drive circuit with the selected components is presented in Figure 19.

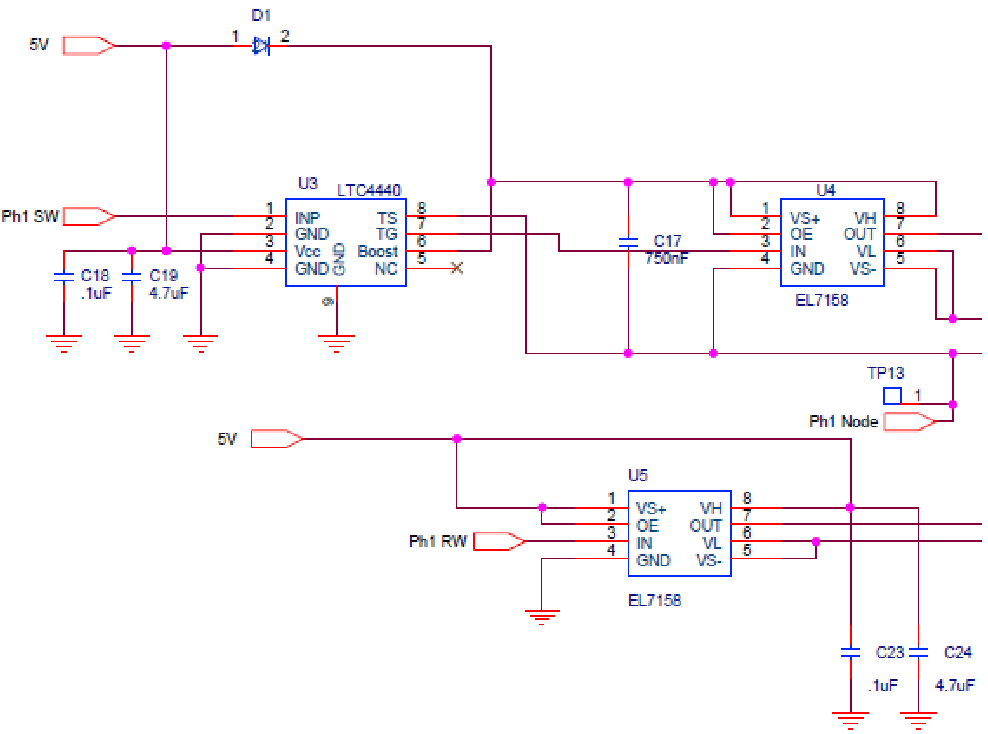


Figure 19: Version2 Gate Drive Circuit

With the switches and the drive circuit components chosen, the remaining components for the synchronous buck topology were selected. A MBRB4030T4G [57] Schottky diode from ON Semiconductor was added to the design as a circulation diode across the EPC2015 synchronous rectifier to ensure that no issues would arise from possible conduction by the body diode in the EPC2015. The EPC2015 parts have been tested and shown to have body diodes with forward voltages in the 1.8V range. The addition of the circulation diode removes the possibility of conduction by the body diode during the switching transitions of the synchronous rectifier

switch, while minimally impacting the converter efficiency. Sourcing of a suitable inductor proved to be challenging as the specifications of the inductor impact the potential switching frequency of the system. A Wurth 7443556130 [58] 1.3uH shielded inductor was chosen to meet the design goal of 300kHz switching frequency, in addition to its high current rating, low loss, and SMT package. The decision to use such a large inductor was primarily driven by a desire to keep the ripple current as small as possible while allowing the circuit to operate at light loads without creating negative current circulation. A small bank of ceramic SMT capacitors was also added at the output voltage rail to help smooth output ripple, which was calculated to need a minimum of 40μF of capacitance to hold the output ripple within the 30mV specification. An example of the calculations can be found in the code presented in Appendix G with good references to the basic calculations presented in [59], [60], and [61]. The final converter phase design is shown in Figure 20.

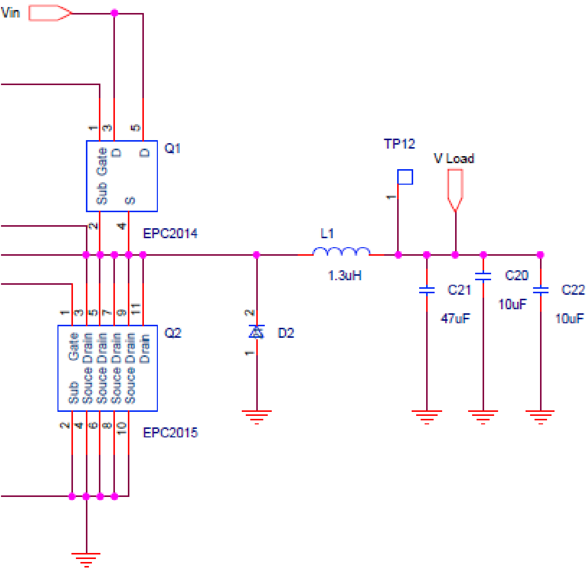


Figure 20: Version2 Converter Circuit

5.2 Layout and Implementation

With the circuit design complete and all the components picked, the process of laying out the circuit began. This design was expected to be capable of ~20A output per phase, requiring care in the selection of current paths in order to minimize losses within the board and to minimize ringing within the switching sections of the circuit. If the lengths of these paths are not decreased as much as possible, converter performance will suffer due to the transients present in the design. EPC specifically states that the gate drive and return line lengths need to be kept as short as possible in order to maintain efficiency and prevent oscillations on the gate lines.

The layout process began with the placement of the converter section components of the design. The components that make up the converter sections were separated based on which regulator phase they were a part of, and then placement of the parts began with the gate driver, level shifter, and EPC switches. These parts were arranged in such a way as to reduce the amount of crossovers needed in the gate circuitry and to minimize the path lengths of the high current paths. The LT4440-5 driver was placed on the back of the board as this allowed for direct connections to the drive line of the high side EL7158 gate drive. The EL7158 gate drivers were arranged with the EPC2014 and EPC2015 in a manner that allowed for a very short, straight connection into their respective gate lines. This allowed for just enough separation between the EPC switches for a substantial copper pour for the inductor node, while allowing their pads to be aligned to make connections easier.

With the connections between the switches and drive components arranged, the circulation diode and inductor were brought in. As in the drive circuitry, care was taken to

shorten the current paths as much as possible. To that end, the circulation diode was moved to the back of the board to allow for a more direct connection to it from the converter switch-inductor node and ground. Placement of the diode on the backside of the board directly behind the node area allows for a large number of stitching vias to be used to maintain a low resistance path. The output ripple capacitors were then also added on the backside of the board to take advantage of the reduced paths available between the output node and ground, removing the need for placement around the exterior of the large surface mount power inductor.

With the diode, inductor, and output capacitors placed, the remaining components were added in. This consisted of the bootstrap diode for the LTC4440-5, as well as the various input and bias capacitors for the ICs in the driver circuit. Capacitors required for the EL7158 gate drivers were placed on the backside of the board to minimize path lengths and to allow for the tight spacing of the LTC4440-5, EL7158, and the EPC GaN FETs, while the bias capacitors for the LTC4440-5 were placed on the topside of the board directly over it. The bootstrap diode for the LTC4440-5 was placed at the top of the gate driver area to allow for a short path between it, the LTC4440-5 and its connection to the high side EL7158.

Once the last converter components were placed, the test points were moved in and added to ensure ease of measurement in the final design. With these in place, the placement of the components in the converter section is complete, with the final arrangement shown in Figure 21. This arrangement was copied for all 4 phases to ensure uniformity in the design. This is shown in Figure 22.

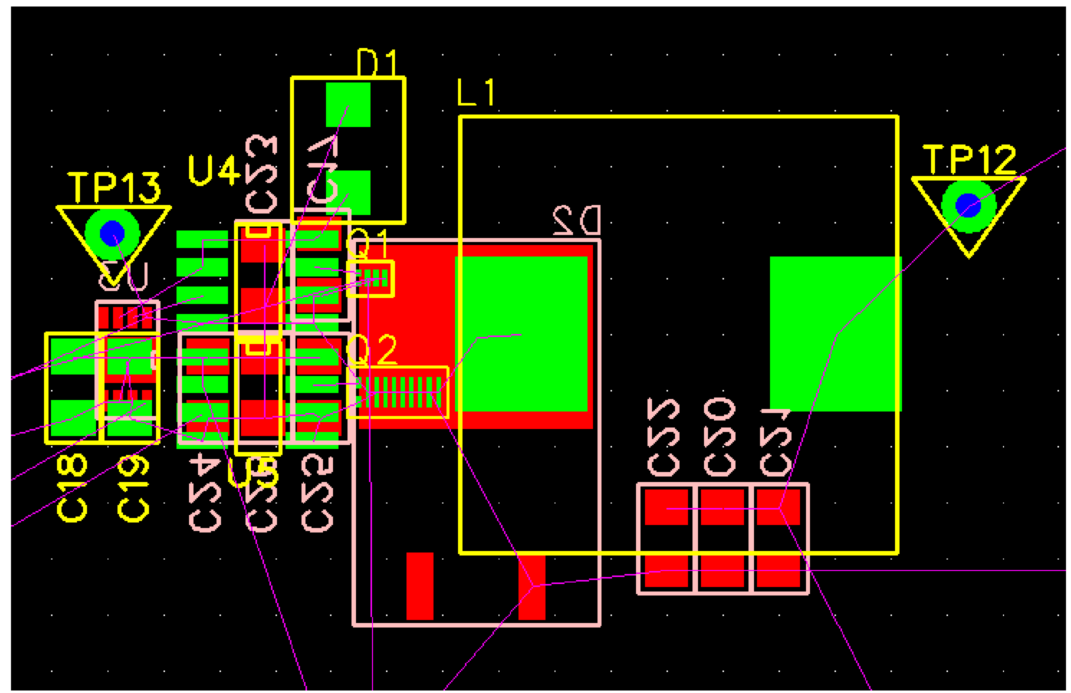


Figure 21: Final Version2 Converter Component Placement

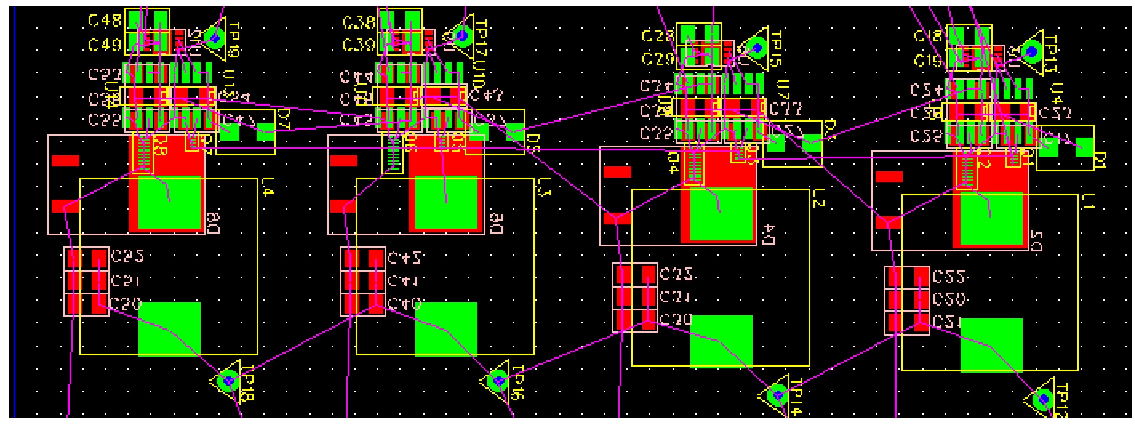


Figure 22: Version2 Converter, 4 Phases.

With the placement of the converter components complete, the arrangement of the controller section could begin. The space occupied by the converter sections created a reasonably

large amount of space that could be used by the controller components, so while an effort was made to maintain compactness in the circuit, priority was given to routing gate drive lines and voltage sense lines cleanly. This generated the initial placement of components as seen in Figure 23. This placement allowed for easy access to headers for programming and interfacing with the controller, as well as to test points for any necessary measurements. The dsPIC was first placed centrally in the available space, and then components were placed radially outward in a manner that kept their interconnections as clean as possible. The FGPA connector was placed toward the bottom of the board for easy access, and the jumpers used to swap control between the FPGA and dsPIC were placed between the two, with the resulting output arranged to align with the correct converter phase.

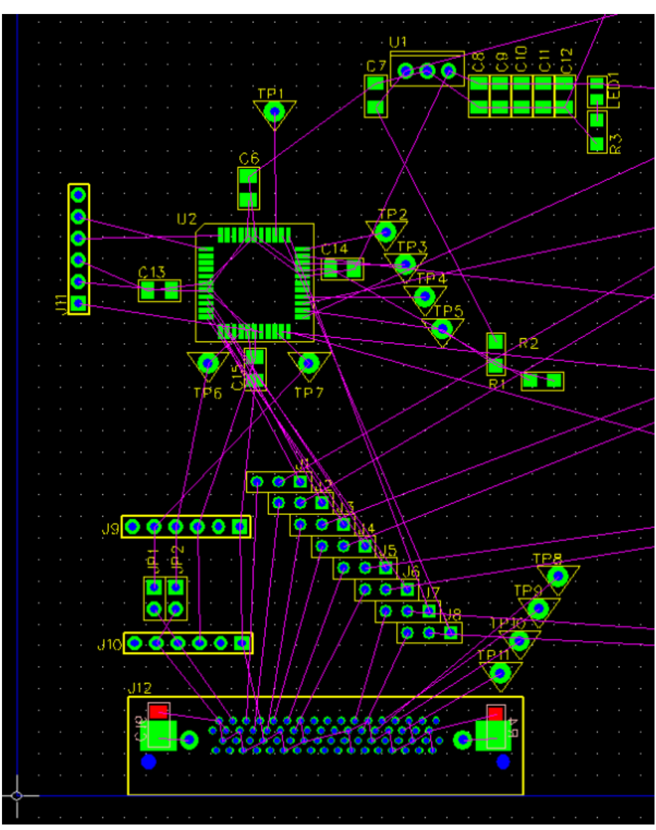


Figure 23: Initial Version2 Controller Component Placement

Once the initial placement of the controller components was completed, the resulting placement of the controller and converter phase was as shown in Figure 24. From this, the process of manually drawing in traces and copper fill areas began. This process was done manually to provide flexibility as the design progresses, and to ensure that areas where adequate routing was difficult were immediately addressed. The autorouter packages available for the layout tool used were not robust enough to handle routing a design of this complexity.

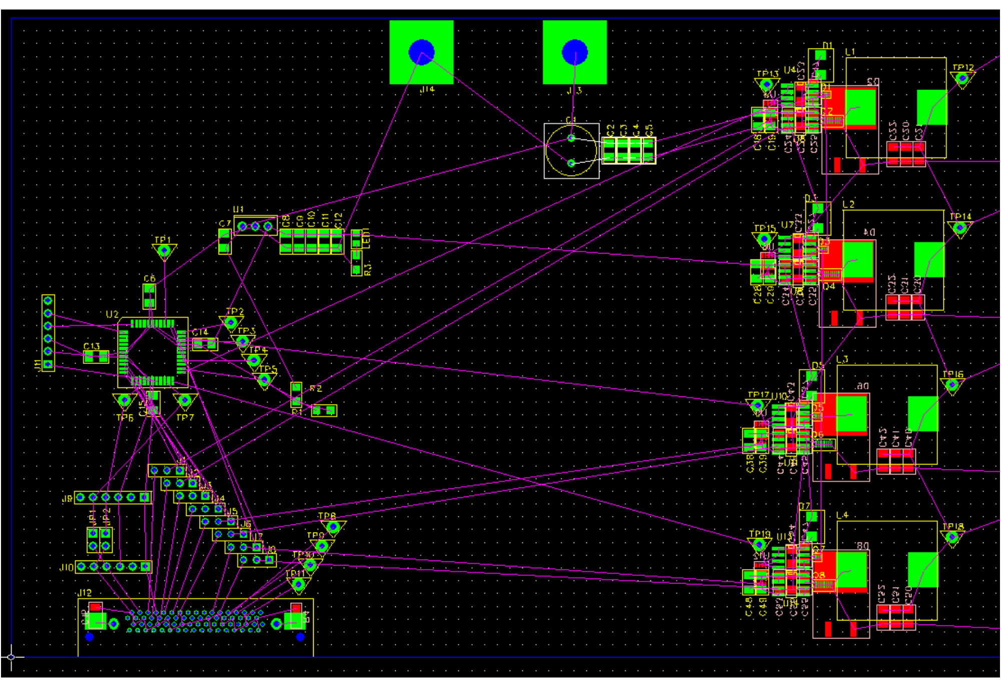


Figure 24: Initial Placement, all Components

During the process of laying out traces, it is not unusual to find issues with component placement that require parts to be moved to maintain integrity of the layout. In this design, the location of the 4 phases in a vertical line complicated the routing of the V_{In} and V_{Out} rails, requiring either additional copper layers be used or the interleaving of power and control lines,

neither being a favorable solution. Closer inspection of the geometry of the converter components suggested a possible solution in a mirrored 2x2 placement of the converter stages. Implementation of this allows the V_{In} rail to drop vertically between the 4 stages and connect directly to the EPC2014 high side switch. Initial adjustments to the layout showed this to be a promising solution, with the possibility of shortening the length of the high current V_{Out} rail by running it horizontally between the 4 phases. This required the V_{Out} rail to be run on the bottom of the board, but allowed for dense via connections to maintain current carrying capabilities, while causing minimal disturbance of the backside ground plane. Figure 25 shows a block diagram of the implementation of this layout and its expected impact to the ground plane.

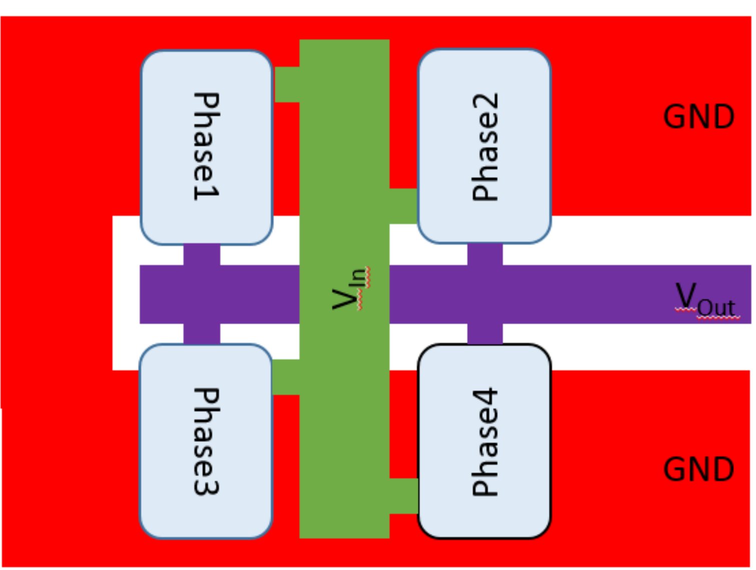


Figure 25: 2x2 Oriented Converter Phases

With this approach applied to the converter stages, traces for the drive circuitry and copper pours for the high current rails were created. Additional high current connection points were added for V_{In}, V_{Out}, and GND. Stitching vias were used to ensure low resistance

connections in high current paths that transition from top copper to bottom layers. Location of the GND, V_{Out}, and V_{In} copper pours were chosen to minimize trace runs from other components if possible. An example of this can be found in the layout for the output capacitors for each converter phase. These capacitors sit on the backside of the board and straddle the border between the V_{Out} and GND pours, allowing them to directly connect without the need for additional trace length.

Component placement in the controller section of the board was also modified slightly during the trace routing process, the majority of this taking place in the area of the FPGA-dsPIC jumpers to enable cleaning connections to the converter circuits. The outline of the board was also modified to better fit the circuit area and to accommodate the needs of the edge mount FPGA connector. The final version of the board can be seen in Figure 26, and the gerber files used to have the board manufactured are shown in Appendix D. This board was ordered from Advanced Circuits on 62mil FR4 with 1oz copper as a two layer design using their standard fabrication process.

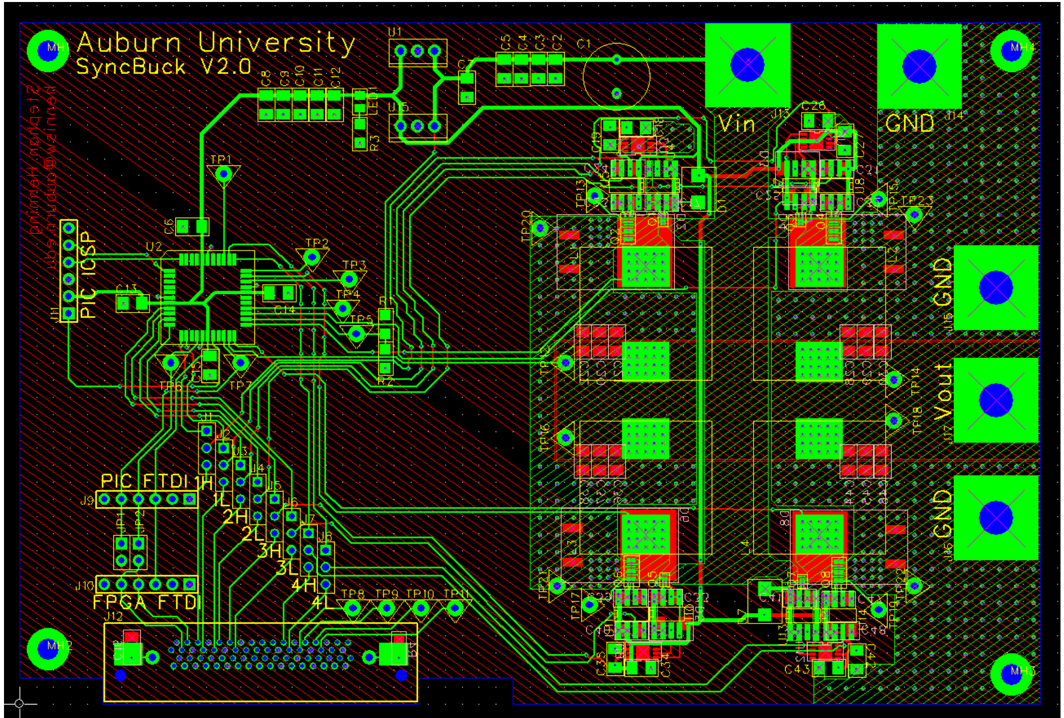


Figure 26: Final Version2 Layout

5.3 Assembly

Population of these buck boards was done using the process developed for these chip scale packages documented in Chapter 4. Other SMD and through hole components were either assembled by hand or with a reflow process, depending on how much of the board was being populated. The large copper pours utilized for the high current power rails generally made hand soldering difficult due to their large thermal mass, so when possible, all compatible components were sent through the reflow process. Due to the double sided design, backside components were sent through the reflow process first and then tacked to the board with Loctite #3621 adhesive to ensure the component placement was not disturbed during topside reflow. The backside of the board was done first as the lower components count required fewer adhesive applications and

less risk of a component being missed and becoming dislodged during topside reflow. Components such as connectors and headers required hand soldering, which was done with a high wattage, temperature controlled iron.

5.4 Testing and Analysis

Assembly and testing of the design was done in several stages. Initially only two converter phases were populated to provide a basic test platform for final code development and control. Typically these were phases 1 and 4 as these two phases had the tightest gate layouts. Figure 27, Figure 28 and Figure 29 show an example of a board with two populated phases.

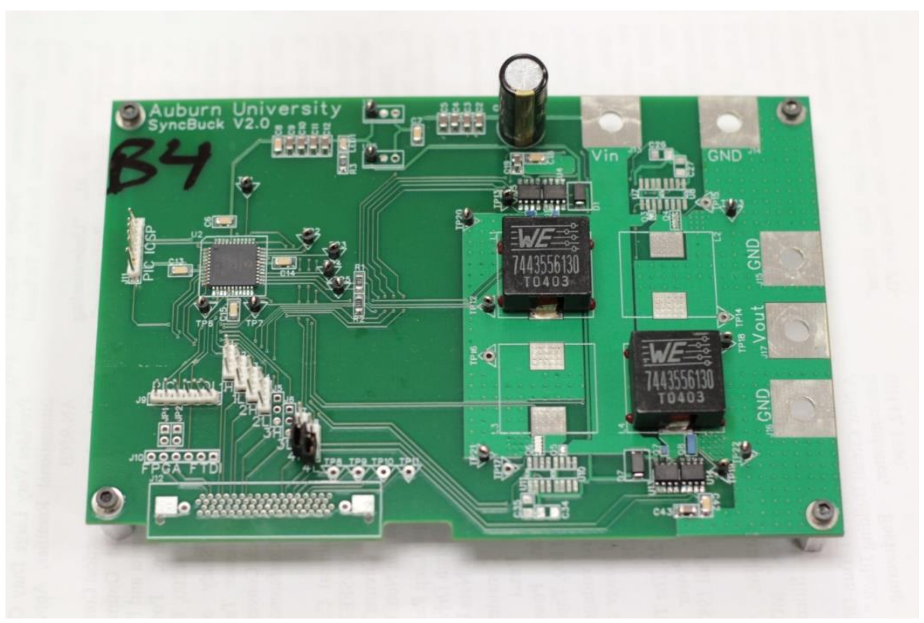


Figure 27: Assembled Version2 Board

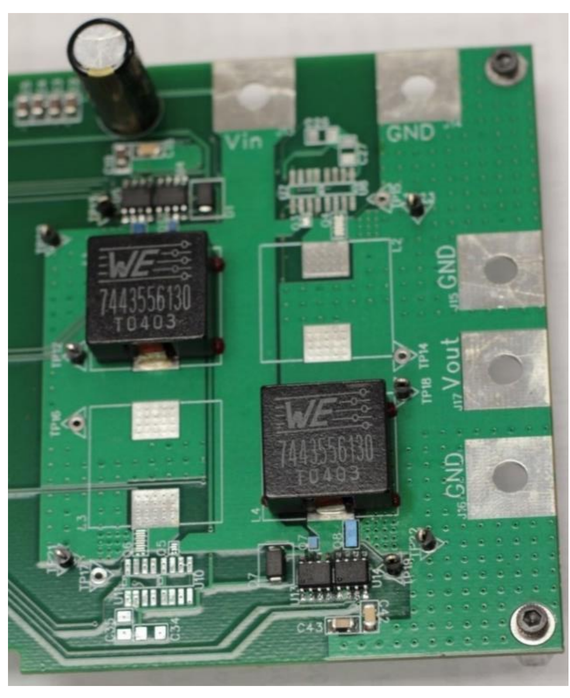


Figure 28: Close up of Assembled Converter Phases 1 and 4

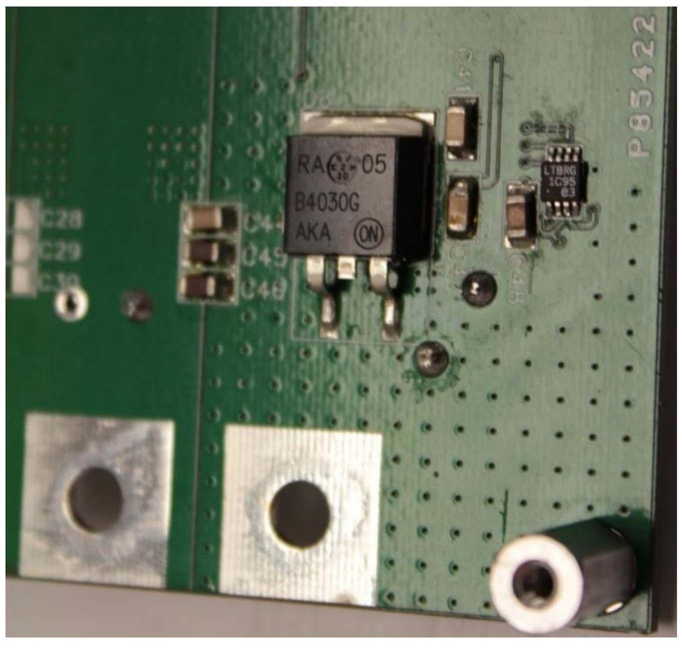


Figure 29: Back of board showing assembled Phase 4

Once the controller was functional, initial testing began with only one phase active at lower current outputs. Testing was done with various input and load levels by using an adjustable bench-top power supply and an adjustable load board. The load board was designed for this project when the need arose for an adjustable resistive load for converter design testing. The load board contains 32 discrete resistors that can be switched on or off through a jumper header connected to a low $R_{DS(ON)}$ MOSFET. This functionality was later improved with the addition of a digital control daughterboard that allowed for more exotic load profiles to be created. An image of the load board is shown in Figure 30.

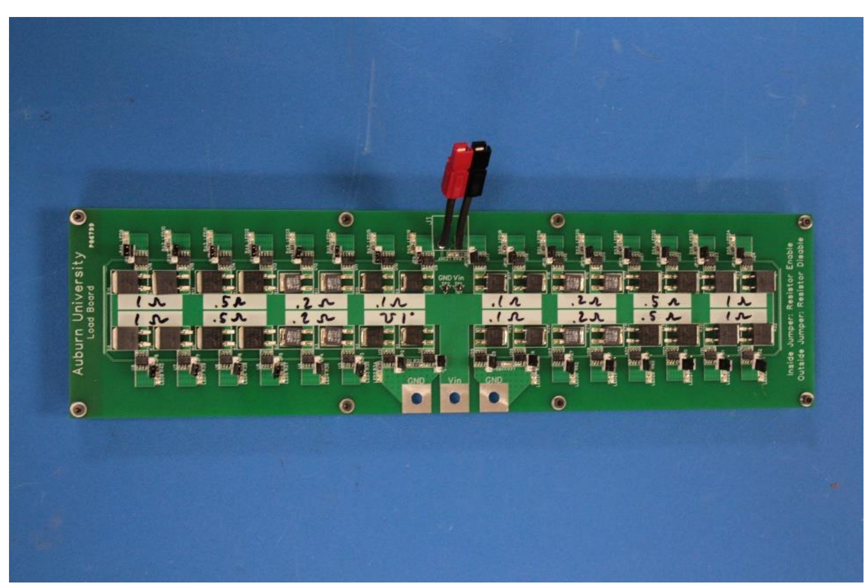


Figure 30: Assembled load board.

The results of initial testing done with a single phase active for the phase 1 circuit and the phase 4 circuit are shown in Figure 31 and Figure 32, respectively, with the average of the two circuits shown in Figure 33. These plots illustrate single phase efficiencies at V_{in}=2.5V, V_{out}=~1V, and at loads of 2A, 3A, 4A, 5A, and 6A for varying switching frequencies. These

efficiency values include the gate drive circuit power draw, but do not consider controller power usage. Efficiency levels were calculated from V_{In}, I_{in}, V_{Out}, and I_{Out} measurements taken from the circuit during testing. Input current and voltage levels were taken from the bench-top supply after its readings were verified, with output voltage and current taken from oscilloscope readings from the output rail and current probe. Power usage by the gate drive circuitry was then factored in to generate an overall efficiency for each phase.

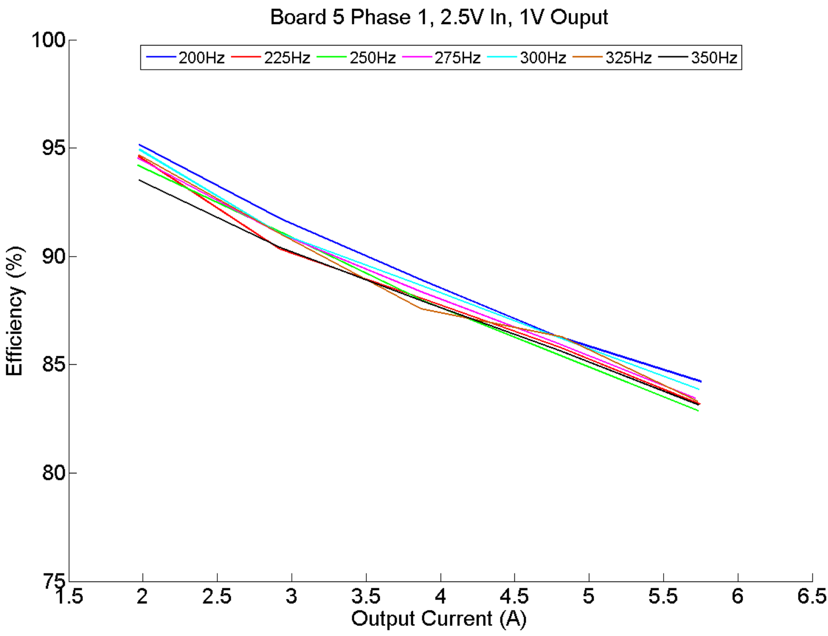


Figure 31: Phase 1 efficiency data

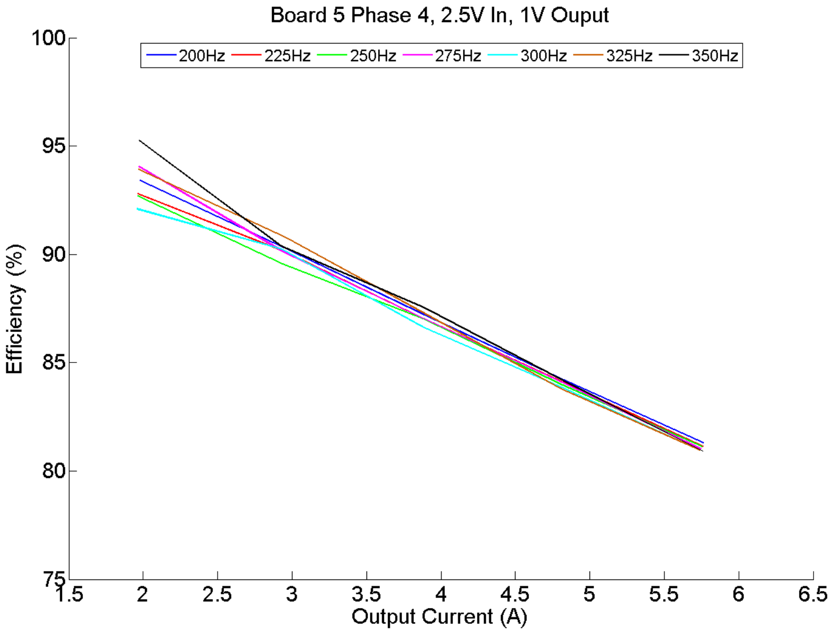


Figure 32: Phase 4 efficiency data

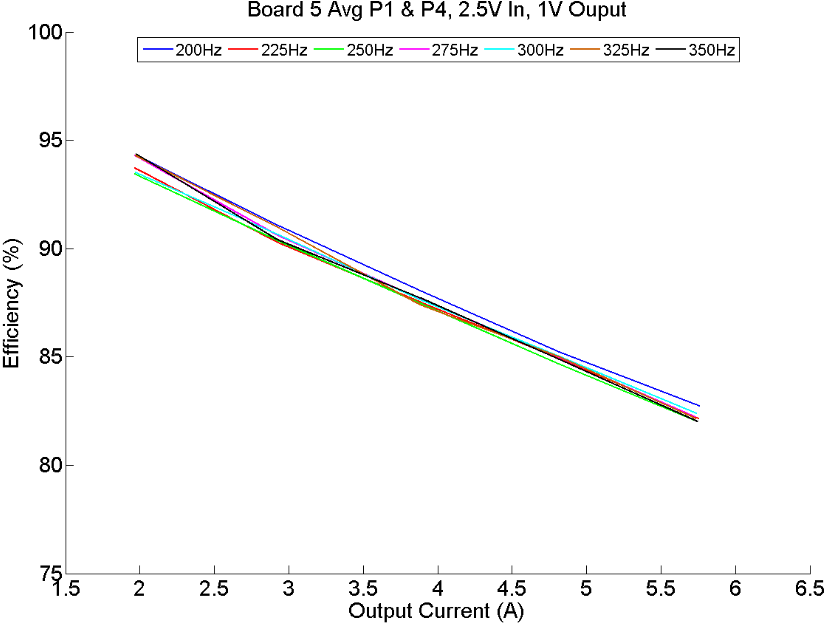


Figure 33: Average of the data from Phase 1 and Phase 4

Continued testing with the board using both populated phases, resulted in the efficiency plots shown in Figure 34. Notice that with increasing load levels the two phase configuration begins to outperform the single phase configuration as increased currents generate additional power loss within the inductor, diode, and through the synchronous rectifier EPC2015.

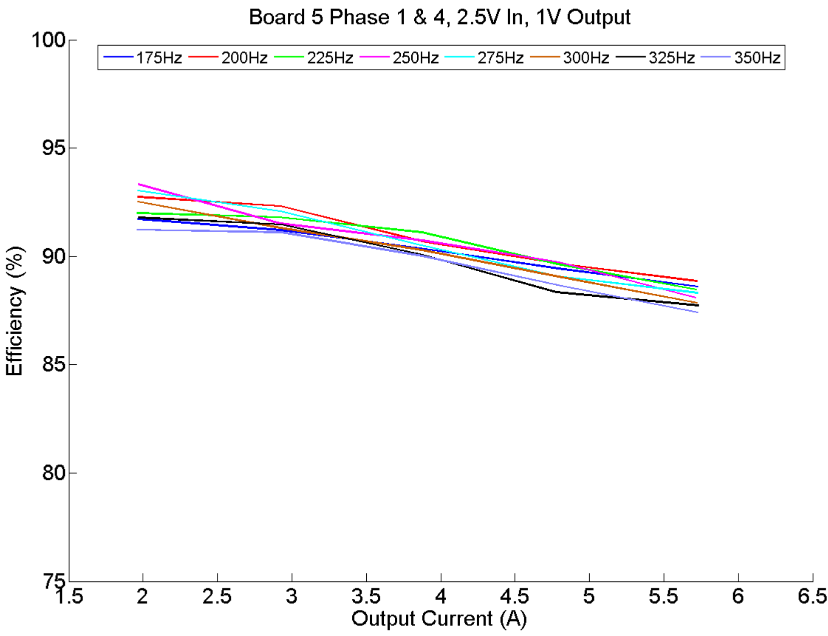


Figure 34: 2 Phase operation efficiency data

Although testing of these two phase boards provided promising results, gate-drain short and drain-source short failures occurred quite frequently as V_{In} and I_{Out} were pushed higher, which created delays due to the required rework. Once additional boards were populated to include all fours phases, these failures continued and generated a significant impact on schedule as many parts were only available from distributors in low quantities and sufficient stock was not

available to maintain operational test boards while failed boards were being reworked. Additionally, reworking failed boards usually required them to be passed through the reflow oven, subjected other undamaged components to additional thermal stresses that could result in performance degradation.

After a review of the available material from EPC on the characteristics of the EPC2014 when in operation and conversations with representatives of EPC, it was determined that there were several possible sources of the problems. A primary suggestion from EPC was the possible formation of dendrites due to the possible existence of uncured flux residue around the pads of the eGaN device, which could cause shorts and lead to failure. A discussion of methods to eliminate this as a cause resulted in the addition of the bake and clean steps to the assembly procedures in Chapter 4 to be used when populating any EPC eGaN device. Additional discussions with EPC suggested that transients present in the circuit may be high enough to cause device failures as these eGaN devices are not tolerant of even brief overvoltage conditions, especially on their gate lines. As a result of this discussion, more testing was done that included monitoring the switching waveforms during operation.

While the measured efficiency levels of the version 2 design were promising, the failures that were experienced at higher V_{In} and I_{Out} levels prevented the design from being fully tested. When the switching waveforms for the system were monitored while under test, it was found that the switch node was experiencing very large amounts of unexpected ringing. While some amount of ringing was to be expected even in the tightest layouts, the measured waveforms showed peaks between 30% and 50% higher than V_{In} on the switch node. Ringing this severe can cause the low side FET to exceed its V_{DS} rating (40V) and fail. Two examples of the severity of the ringing on the switch node while operating are shown below, Figure 35 at V_{In}=7.5V, V_{Out}=.97V

and I_{Out}=1.8A and Figure 36 at I_{Out}=5.6A. In these images channel 1 in yellow represents the switch node, channel 2 in blue represents the gate of the synchronous rectifier, channel 3 in purple represents the output voltage, and channel 4 in green represents the output current on a 10x probe.

Figure 35: Circuit waveforms at 1.8A output

Figure 36: Circuit waveforms at 5.6A out

Traditionally, ringing is caused by parasitic inductances within the circuit. Because of this, extra attention was paid during the layout process to attempt to minimize it as much as possible. Due to the severity of the ringing on the switch node it was determined that the parasitic inductances present in the area of the low side switch were significantly greater than expected based on efforts undertaken during the layout process to reduce them. This, combined with the very likely occurrence of unexpected parasitics in the layout surrounding the high side switch, led us to believe that these parasitics were the likely causes of the failures observed within the EPC2014 high side switch. Later conversations with representatives of EPC helped affirm these suspicions as they reported that the EPC2014 design is less tolerant of transient spikes when compared to their other eGAN FETs.

Potential modifications were briefly investigated in order to reduce the amount of ringing in the circuit as described in [62]. Many of these methods involve adding passives to various areas around the switches to slow their transitions, or involve adding snubbers to the switch node. All of these solutions have a negative effect on system efficiency, so with the major goal of the highest efficiency possible and due to the design's compact nature and the inherent difficulty of the rework processes, the decision was made to extract as much data as possible for the customer while beginning the process of a new design with an aim to further reduce the parasitics within the layout.

5.5 Lessons Learned

While efficiency testing of the v2 design showed promising results in the 95% range, the performance issues that arose due to unexpected parasitics within the circuit greatly reduced the usefulness of this design. Testing of the v2 design also revealed several areas needing improvement in overall system usability. Many of these concerns came from the high difficulty of the rework processes, which greatly slowed the testing process. Additional issues involved lack of sufficient measurement points in the circuit and lack of visual indicators as to system status. This was found to be a problem due to an error in the drive circuit in which the inverting nature of the EL7158 was not taken in account. This required the controller to be powered before the converter stages to prevent the EPC devices from coming up in an ON state, potentially shorting the V_{In} rail to ground. Many of these issues have been condensed and are presented in Table 12 along with their resolution priority for the new design.

Table 12: Version 2 Areas Requiring Improvement

Issue	Priority
Layout Parasitics	1
Easier Rework	1
Visual System Status	3
Additional Measurement Test Points	2
Additional Ground Test Points	2
User Interface	3
Individual Phase Current Measurement	2
Reduced Converter Footprint	2
Increased Efficiency	1

Chapter 6 Point of Load Version 3

Based on the issues encountered during the assembly and testing of the v2 design it became clear that greater efforts were needed during the development of v3 to ensure further progress toward the project goal of a POL prototype. While v2 proved the concept, its inability to run at higher input voltages and output currents reduced its overall usefulness in terms of project scope, accelerating the need for a redesign to correct the issues found within the design. While much of the focus of v3 was on correcting the issues in v2, the design still needed to push the project forward and provide a test bed for continuing design and development updates.

6.1 Design

Development of the v3 converter began with a survey of the issues in the v2 design to ensure these were fully addressed in the new design from an early stage. Table 13 lists the issues and their priority in the creation of the v3 converter design.

Table 13: Version 3 Priority Design Areas

Issue	Priority
Layout Parasitics	1
Easier Rework	1
Visual System Status	3
Additional Measurement Test Points	2
Additional Ground Test Points	2
User Interface	3
Individual Phase Current Measurement	2
Reduced Converter Footprint	2
Increased Efficiency	1

The needs pulled from this list weighted heavily on an improvement to the operational performance of the v3 design while maintaining a high level of usability. As this was a high priority, much attention was given to possible solutions to solve the issues in the v3 design while providing gains to efficiency for the converter section of the design.

The design process for v3 began with a hard look at the problems of device failures and switch node ringing that were present in the v2 design. Almost universally, the suggested solution to deal with issues involving switch node ringing in these synchronous converter design begins with improvements in the layout to reduce any stray parasitic inductances [63] [64]. For the v3 design we first approached the gate drive layout to implement some layout improvements.

The development of the gate drive for the v2 design did not result in a very robust circuit. Even though the driver chips selected had been used by EPC in the past, our implementation in the v2 design was not sufficient to allow them these devices to operate in conjunction with the rest of the circuit without submitting the gates on the EPC FETs to stresses from transients that potentially lead to failures. Fortunately, during the v3 design process a new driver chip was released by National Semiconductor shortly before they were acquired by Texas Instruments that had been designed in collaboration with EPC to drive the types of eGAN FETs being used in this project. This new chip, the LM5113 [65], allows for a compact single IC solution to the gate drive for both high and low side switches due to its built in floating high side drive circuitry, a substantial reduction from the original three ICs needed in the v2 design. This reduction in the number of ICs allowed for an immediate shortening in the overall length of the gate drive lines. Furthermore, the LM5113 has separate high-low drive pins for each gate along with a robust clamping circuit that prevents the gate drive lines from exceeding 5.2V, allowing for the on-off transitions for each gate to be controlled as needed to slow down transitions to reducing switch

node ringing with minimal sacrifice to converter efficiency while ensuring voltage levels on the gates remain within the safe range for the device [42] [62] [66] [67]. The LM5113 was complemented by the selection of passive components with as low of a package inductance as possible based on information gleamed from an AVX technical bulletin regarding inductance values for common MLCC capacitors [68]. This is more prevalent in the selection of the bypass and bootstrap capacitors where low package inductance capacitors were chosen. The selection of these low inductance capacitors helps reduce the loop length of the high current paths for the driver, helping prevent noise on the gate drive lines and ensuring reliable operation. The gate drive portion of the circuit can be seen below in Figure 37.

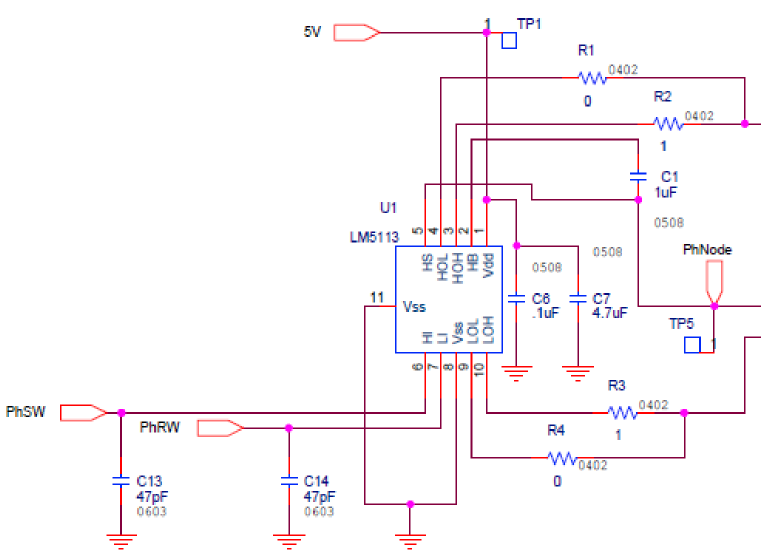


Figure 37: Version 3 gate drive circuit

With the LM5113 selected as the gate drive for the converter phases the next large area requiring attention was the switches themselves. The original selection of the EPC2014 as the high side switch was due to its low gate charge, allowing for faster switching with less losses.

While these traits make it a good selection for the high side switch, the reliability [69] [70] and rework issues experienced with the v2 design encourage us to review the EPC2015 for use in this role. While the EPC2014 does maintain a lower gate charge, the EPC2015 has a lower on resistance in addition to a lower package inductance. With the renewed focus to eliminate as much stray inductance from the circuit as possible to reduce ringing, changing to the EPC2015 for the high side switch would provide a significant step toward that goal. In addition to this, the EPC2015 footprint is similar enough to that of the EPC2014 to allow for an EPC2014 to still be placed as the high side switch, should the decision to test such a configuration be made. In addition to the change from the EPC2014 to EPC2015, capacitors were added to the V_{In} rail immediately in front of the high side switch in order to help reduce any transients. The capacitors selected for this were of sizes from 0.1μF to 10μF and were chosen in as small of a package as possible to reduce package parasitics as much as possible.

With the EPC2015 now selected for the high side switch, focus shifted to the low side switch. The v2 design included a single ECP2015 in this location, originally selected for its low on resistance. With much attention being paid to removing as much inductance as possible from the power path to help reduce switch node ringing the EPC2015 was determined to be a solid choice due to its low package inductance, but a further reduction over the v2 design was needed so an additional EPC2015 was added in parallel for the low side switch. This not only reduces the inductance, but also reduces the resistance, which should allow for a slightly more efficient converter. The addition of a second EPC2015 does add size to the layout requirement, so this section of the board will require attention to ensure the layout is get a tight as possible as to not negate the gains from adding the second EPC2015.

With adjustments to switch selection complete, a new power inductor was chosen to complement the revised design. The previous Wurth inductor was sufficient for the v2 design, but was physically large. Some research into other suitable choices produced the XAL1010-102ME from Coilcraft [71]. This inductor is significantly smaller than the Wurth used in the v2 design, while still having a high saturation current of 55A, a DC resistance of 1.0mOhm, and an inductance of 1.0uH, while having a footprint area of approximately half the space occupied by the previous Wurth inductor.

The power path design was then finished off with the selection of a hall-effect type current sensor, output capacitors and the reuse from the v2 design of the MBRB4030T4G diode from ON Semi as the circulation diode. The QC-2065 [72] from AsahiKASEI AKM was chosen for the current sensor to allow for per-phase current measurements with only a slight increase in power path resistance. The QC-2065 is a high-speed AC/DC current hall-effect sensor with an analog output capable of bidirectional sensing at up to 400kHz with only 100uOhm of resistance through its current path. The output capacitors chosen varied in size from 0.1µF to 100µF and were chosen in packages with the lowest possible inductance, similar to how the input capacitors were selected. The resulting capacitor array included five capacitors in packages including 0306, 0508, 0612, and 1206. With the last design choices made, the power section of the converter circuit appears as shown in Figure 38, with the final converter circuit shown in Figure 39 and in Appendix E.

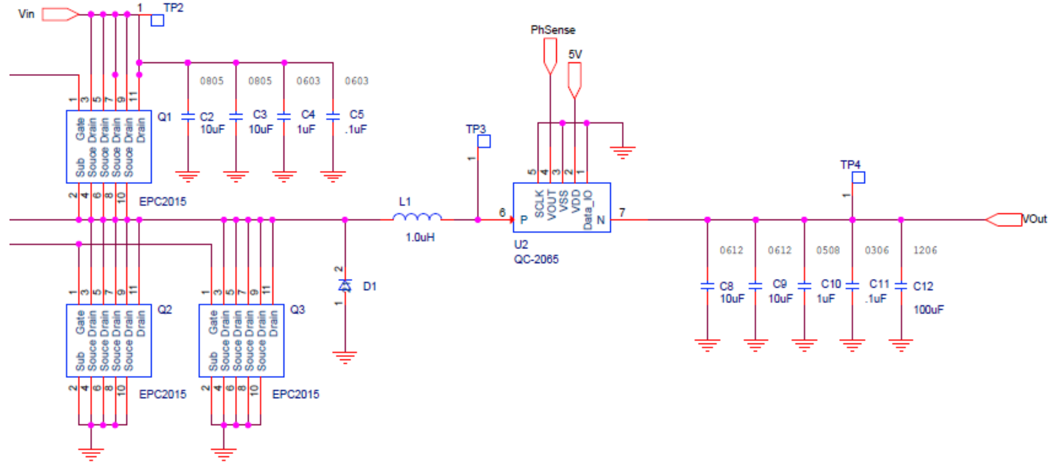


Figure 38: Version 3 converter circuit

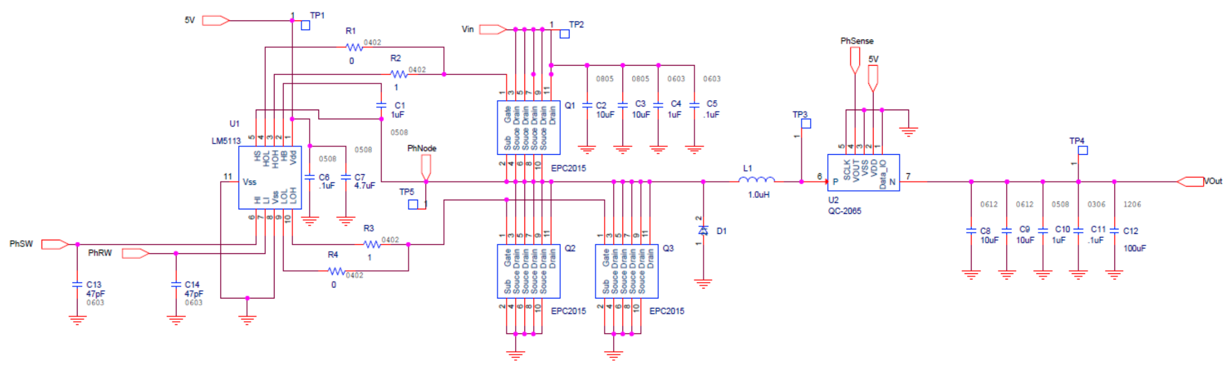


Figure 39: Full version 3 converter stage

With the design modifications to the converter circuit complete, the control portion of the system now came under scrutiny. While the controller circuitry does contribute to overall system efficiency, for the v3 design it was decided that a more user friendly design was needed and that reduction of size and power usage by the controller was best left for the Phase III commercialization phase of the project. As the controller evolved during testing of the v2 design

the control team determined that they needed more capability than the dsPIC could provide, but not so much as to justify the time and effort required to transition to the FPGA processor. An investigation into new processors was initiated and the resulting choice was the TI TMS320F28335 [73] implemented on a Ti Control Card [74] development platform. This chip provided the floating point processor and high speed ADC that the control team wanted, and was available in a preconfigured 'control card' design that allowed for easy integration into the project. In addition to providing increase capabilities for controller algorithm development, this new processor had additional IO lines that allowed for the number of converter phases in the final design to be increased from four to five, while still proving numerous lines of feedback from the converter phases to allow for new and novel controller design algorithms to be tested. Voltage divider networks were added to the sense lines from the converter phases to ensure their outputs were within the range for the TI control card. Three of the available daughter card slots included sense lines tied to the switch node. These connections allow the processor to sample these lines for the design of a current observer as a part of the control strategy.

Connectors were then added to the circuit for separate 5V inputs for the control and converter sides of the circuit, along with V_{In}, V_{Out}, and programming and interface headers. Additional supporting circuitry was added such as installed POL phase sense lines, LED indicators, push buttons, and DIP switches through the use of four NXP PCA9531 I2C IO expanders [75] to create a means to interact with the system without requiring a computer to be present during testing. These expanders give the Ti control card the ability to sense which phase slots of the carrier board are populated, allowing the processor to apply control signals to only the slots that have installed POL daughter cards. The DIP switches and pushbuttons make it possible for a user to control the operation of the circuit without a computer terminal connected

to the control card. Test programs can be written that would allow for various system parameters to be varied based on switch inputs, allowing greater flexibility in the implementation of control algorithms and during testing and demonstrations. Appropriate bypass capacitors were also added for each voltage rail and for each IC within the design. Sections of the controller circuit are shown in Figure 40 through Figure 44, with the full schematic available in Appendix E.

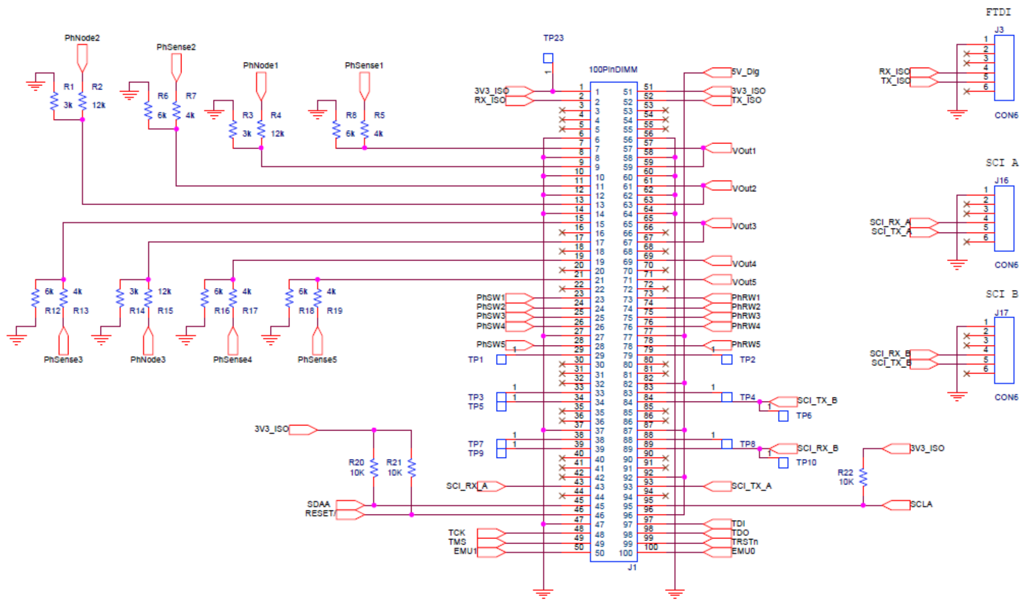


Figure 40: Version 3 ControlCard interface

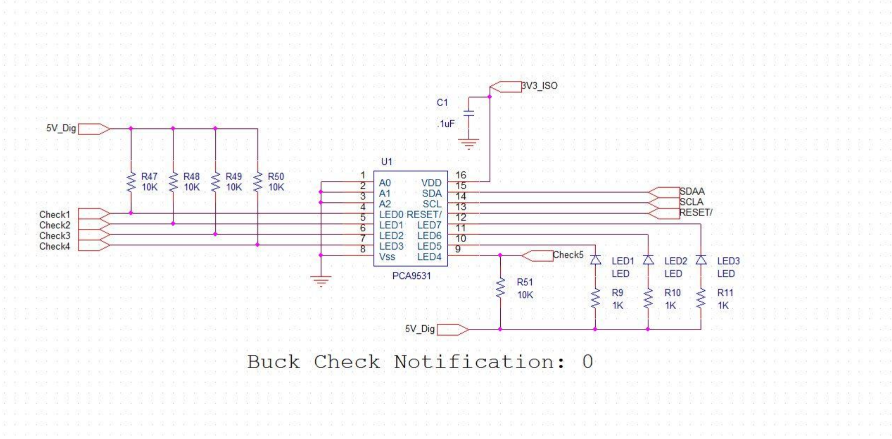


Figure 41: Converter phase status check

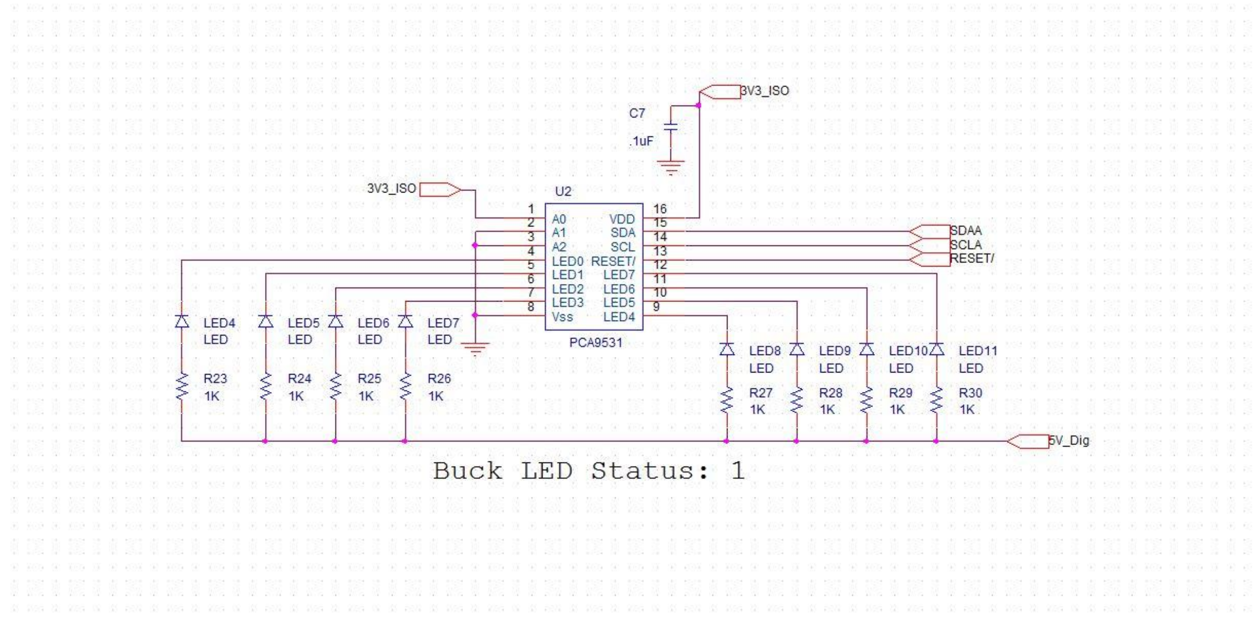


Figure 42: User programmable converter status LEDs

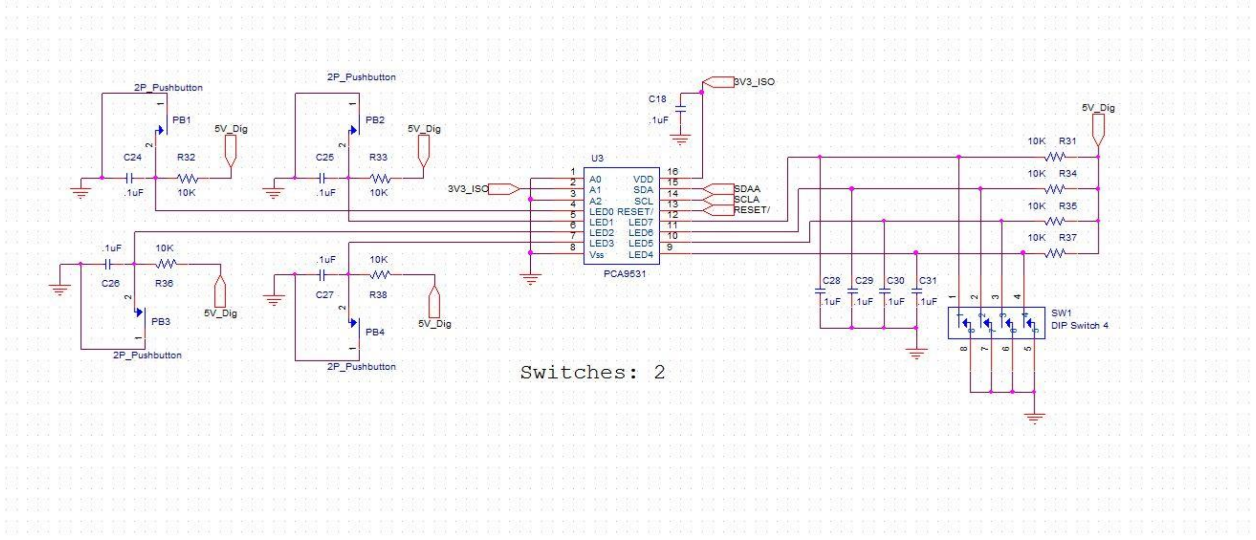


Figure 43: User programmable pushbutton inputs

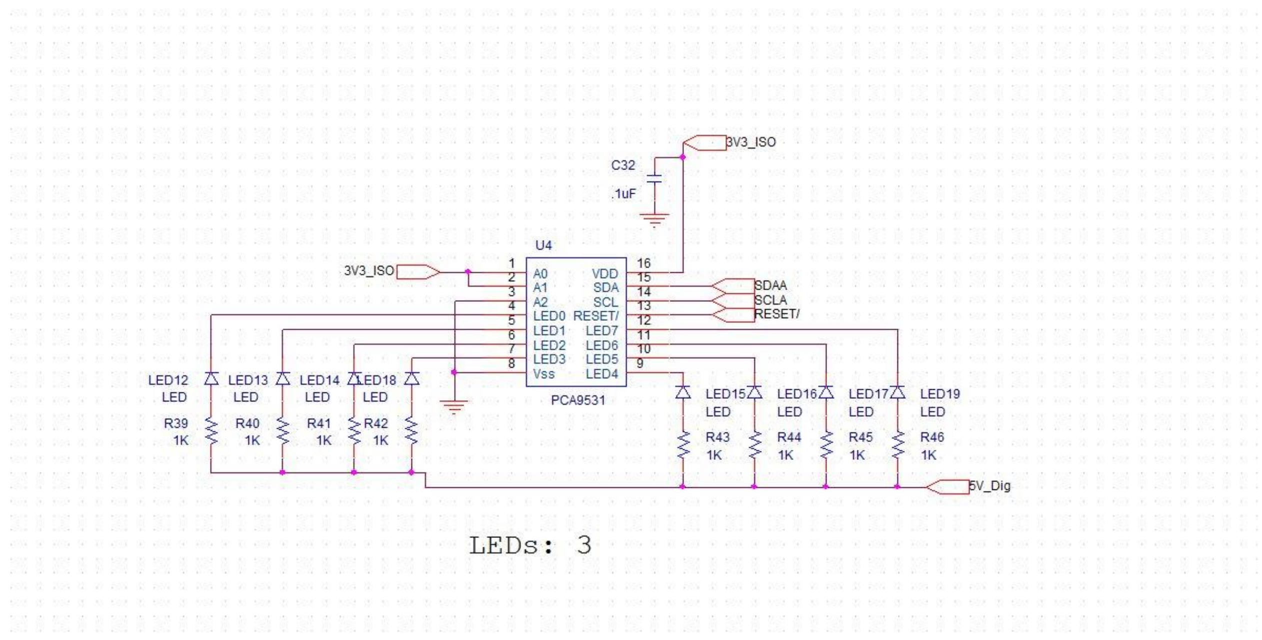


Figure 44: Use programmable LED indicators

With the change to this new controller came a shift in attitude toward the testing of the v3 design. The main focus of the project is on increased converter efficiency and as we experienced

with the v2 design, the results do not always match the expected performance. Because of this a radical change was made for the v3 design. Instead of being a single integrated circuit with a controller and five converter phases, a mother-daughter carrier design was implemented utilizing the controller card design of the TI TMS320F28335 as a template. In this design the controller supporting circuitry would be assembled on a carrier motherboard that would then have connector slots into which the TI control card and each individual converter phase would be plugged. While this type of system creates additional losses due to the extra connectors and longer trace length, along with extra challenges in having to manage what would now be at least 7 unique PCBs for a five phase converter design, the flexibility in testing and updating of the design greatly outweighs the cons associated with the slightly increased power loss. This mother-daughter type design also allows for more rapid design changes without requiring still functional portions of the circuit be scrapped. It will also allow for easier rework and repair as damaged sections of the circuit will be isolated to a specific board and can be removed from the rest of the system while a replacement board is then installed, allowing testing to continue with minimal interruption. The largest challenge in the implementation of this mother-daughter design was in the selection of suitable connectors for each board. The TI control card was designed to fit a specific type of DIMM connector, similar to what many types of computer RAM used, which was easily acquired from TI directly. Selecting a connector for the power stages was more difficult as there were few single connector solutions on the market that provided large enough power connections to handle the high current outputs of the regulator stages while having a suitably large number of signal lines available. In the end no suitable off the shelf connector was found, all options that would have been suitable required a custom order part, so a compromise was reached and a 100 pin 0.1 inch dual row strip header was chosen as the connector for the

power phases as it provided enough pins so that signals lines could be separated from the high current lines by a suitable distance while allowing for enough pins to sustain each high current rail. Figure 45 shows an example of the pinout used for this 100pin header with signal and voltage lines marked. Notice the alternating pattern of ground and signal lines used to minimize any potential signal coupling. With a connector solution found the design then transition into the layout phase.

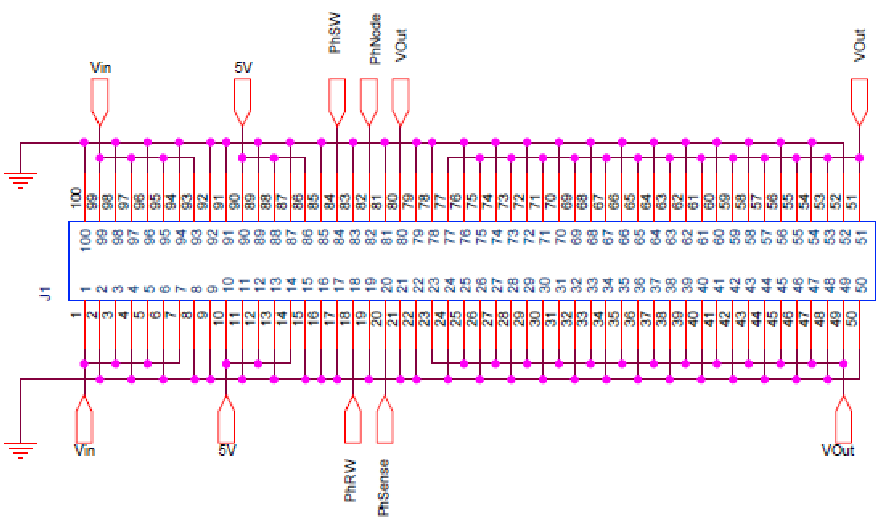


Figure 45: Converter daughter card interface

6.2 Layout and Implementation

With the decision to implement a motherboard – daughter card design for v3, the approach to the layout shifted slightly. In the v2 design efforts were made to contain the entire power stage section of the board into as small of an area as possible in order to reduce stray parasitic as much as possible. This kind of methodology is now impossible in v3 as the connectors require that a large amount of trace length exist between each converter phase.

Because of this more effort was given to the converter stages to ensure the layouts within each converter daughter card was as efficient as possible.

To begin the layout of the converter daughter card a footprint was drawn for the 100pin connector. As this connector was very long at 5 inches in length, it became the driving factor for the size of the daughter card. The pinout locations for this connector on the converter cards was selected to allow the regulator circuit to sit in roughly the center of the board. From here the rough layout began with the gate drive circuitry. The LM5113 was placed on the top layer of the board in order to keep the drive paths to the EPC FETs as short as possible. Footprints for the gate drive resistors and signal input capacitors were then placed around the driver chip and located in a manner that minimized the length of the gate drive lines. Once the placement of these components was accomplished, the bypass and bootstrap capacitors that were selected for their lower package inductance were placed with one bypass on the top of the board, the other bypass directly underneath it on the bottom of the board, and the bootstrap capacitor also placed on the bottom of the board. The placement of the bypass capacitors directly over each other and in close proximity to the LM5113 allows for a very tight current loop to help reduce transients. Similarly, the close proximity of bootstrap capacitor also aids in reducing transients. The final placement and orientation of these components is shown in Figure 46.

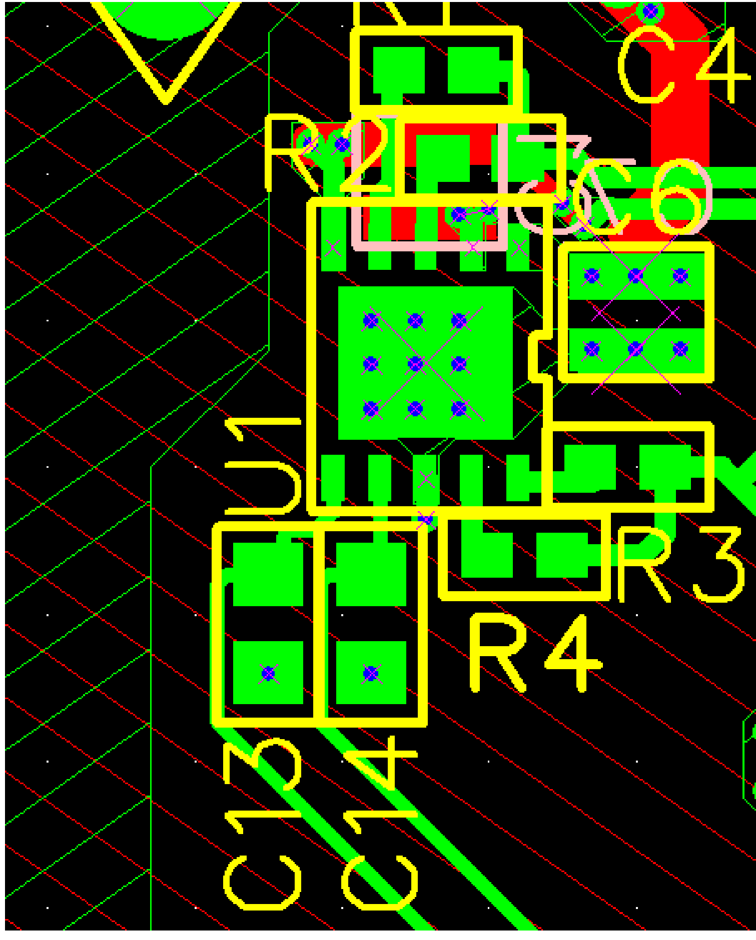


Figure 46: Version 3 gate drive layout

With the gate drive components placed the EPC eGAN FETs were then located in a way that minimized the length of the gate paths while still allowing for enough space for repair and rework. The rework that was performed on v2 of the design made it apparent that more space needed to be left around the EPC FETs in order to make it possible to replace them should they become damaged without causing harm to any of the neighboring components. The use of EPC2015 switches for both the high and low side allows more flexibility in the design as the EPC2014 is capable of fitting on the footprint of the EPC2015, should various switch configurations be desired. Once the switches were located, the circulation diode was placed

immediately behind them on the backside of the board behind the switch node, and the input capacitors were placed immediately above the high side switch on the V_{In} rail. With those components in position, the inductor, current sensor, and output capacitors where then placed, with the current sensor being located on the back of the board in order to tighten the layout and ensure current flow in the expected direction through the sensor. The output capacitors were placed around the terminal of the current sensor transitioning toward the area of the 100 pin header in order to better use the available space. Copper pours were then added to create the largest current paths possible, and then the signal lines were run to the 100 pin header with grounded pins isolating them from any high current pins. Thermal isolation on through-hole pins is avoided at all costs to ensure low resistance paths at higher currents.

The final layout for the converter phase was 5.1 inches long and 1.5 inches high, with the converter circuitry itself being approximately 1 inch long and 0.9 inches high, compared to the approximately 1.5 inches long and 0.9 inches high of the v2 converter stages. An image of the final converter daughter card is shown in Figure 47, with the gerbers for the layout being available in Appendix F. The gerbers were submitted to Advanced Circuits for manufacture and were produced on 62mil FR4 with 2oz copper.

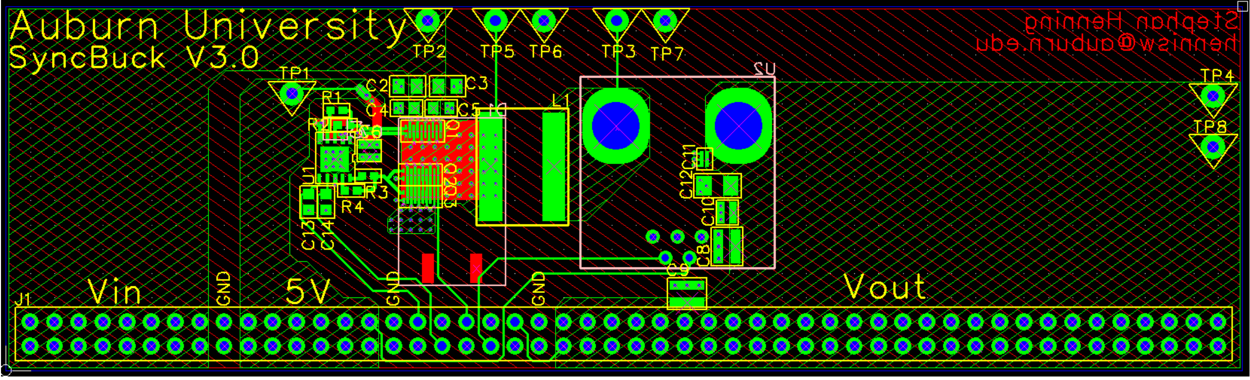


Figure 47: Version 3 converter power stage daughter card layout

With the layout of the converter card complete and its footprint requirement now known, the layout for the carrier board could now begin. Since the 100 pin connector became the driver for the long dimension of the converter card, the mating connectors for each of the five phases was placed first. Spacing of 1 inch was given between each connector to ensure that there would be no interference between components on adjacent cards and that there was enough space for adequate airflow to pass through. These connectors were placed parallel with the long axis on the right side of the mother carrier board.

With the converter card connectors placed, the controller card connector was then placed to the left of the converter phases in a manner that reduced the number of layer transitions in the phase drive lines to a minimum. This was rather difficult as the connector utilizes a four row design and narrow traces had to be used to weave between the relatively dense pin arrangements. Once the controller card connector was placed, the I2C expanders and their associated user interface components were placed on the left side of the control card near the left edge of the board. Their placement near the edge allows for easy access to the pushbuttons and switches while allowing enough room for text boxes to be placed that allows for the function of each switch or indicator to be written in as they become used. Communication, debug, and interface headers where then added above and below the control card connector to prove easy routing of these traces.

With the majority of the signal lines now routed, connectors for the power rails were added and copper pours for the voltage rails were drawn. High current connectors were made using large bolted down ring terminals, while lower current rails used Anderson Power Pole connectors. A 3rd inner layer was added to the board to ensure the copper pours for the voltage

rails has sufficient area for their expected currents. These pours were isolated into vertical sections on this inner layer, allowing them to occupy relatively large areas without having to cross over each other. This inner layer was sectioned off into separate pours for V_{Out}, V_{In}, GND, and included separate 5V supply lines for the converters circuits and the controller circuits, allowing for more accurate measurement of the power used by the gate drive components. A copper pour for the GND net was when added to the entire back side of the board. This was aided by the extra inner layer used for the voltage rails, allowing the ground pour on the back of the board to only be interrupted in small areas where a trace needed to transition over another node. Additional copper pours on the GND net were added to any open areas between converter phase signal lines on the top layer to reduce the probability of coupled noise and an additional V_{Out} pour was added around the output of the converter connectors and the V_{Out} connector pads. Any traces that required transitions to another layer to complete their path were routed to the back of the board instead of the inner layer to ensure their entire path length was visible in the event that any issues were discovered after production. Thermal isolation on through-hole pins is avoided at all costs to ensure low resistance paths at higher currents.

With the copper pours complete, test points were then placed in areas convenient to the nodes they were intended to measure. Additional ground points were also added along the board perimeter near signal and voltage test points, along with in open areas of the board to ensure that a ground point would always be available during the testing process. Once all the components were located, text markings were placed in appropriate areas to indicate the function of all connectors, test points, and known indicators. An additional text label was added to allow serialization of the board during the test process. Figure 48 shows an image of the final layout for the carrier mother board, with gerbers for the individual layers available in Appendix F. The

final board is 12 inches long and 6.5 wide and was manufactured by Advanced Circuits on 62mil FR4 with 2oz copper on the outside layers and 1oz copper on the inner layer.

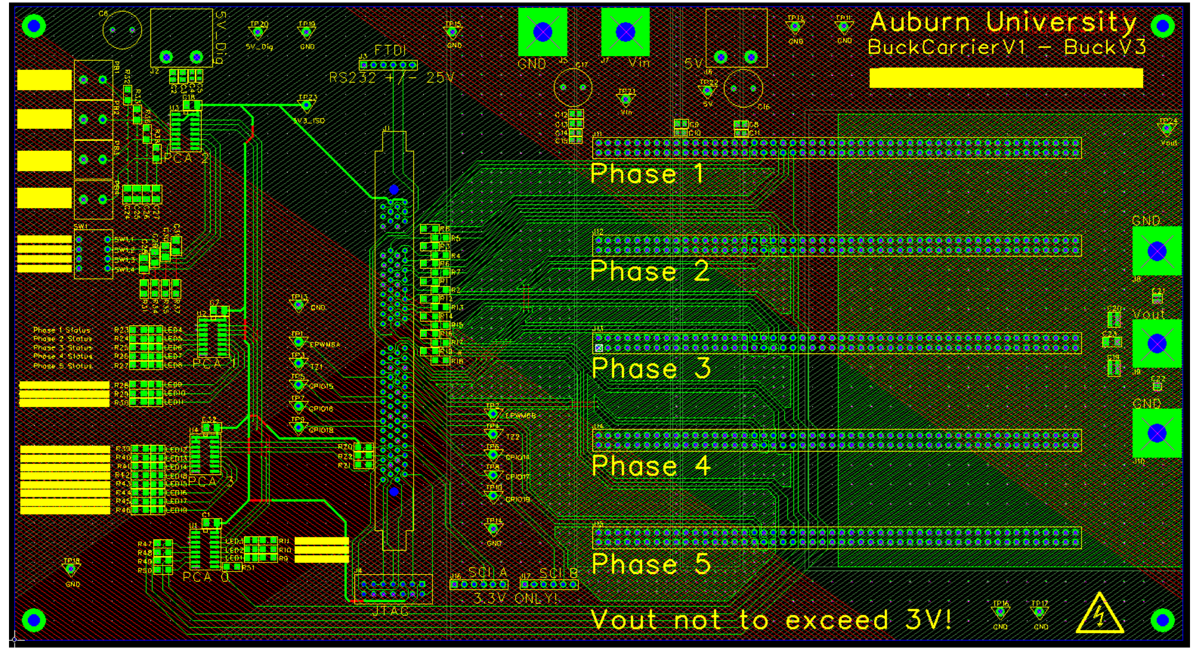


Figure 48: Version 3 carrier board layout

6.3 Assembly

While the shift to a mother-daughter design requires some changes to the design approach for the v3, the assembly process is very similar to what was done for the v2 design. Assembly of the POL daughter cards began by placing and soldering the EPC eGAN devices using the process described in Chapter 4. After the concerns expressed by EPC in reference to possible uncured flux causing dendrite growth issues, the cleaning and bake steps mentioned in Chapter 4 were added and used for all v3 boards. Most boards were populated with the EPC2015 in the switch and synchronous rectifier positions, but the layout permits EPC2014s to be used in the EPC2015 footprint if desired. A few boards were populated with EPC2014s as switches and

with a single EPC2015 as synchronous rectifier to act as comparisons against the base line design. Figure 49 shows a close up of the converter section of a bare board before assembly.

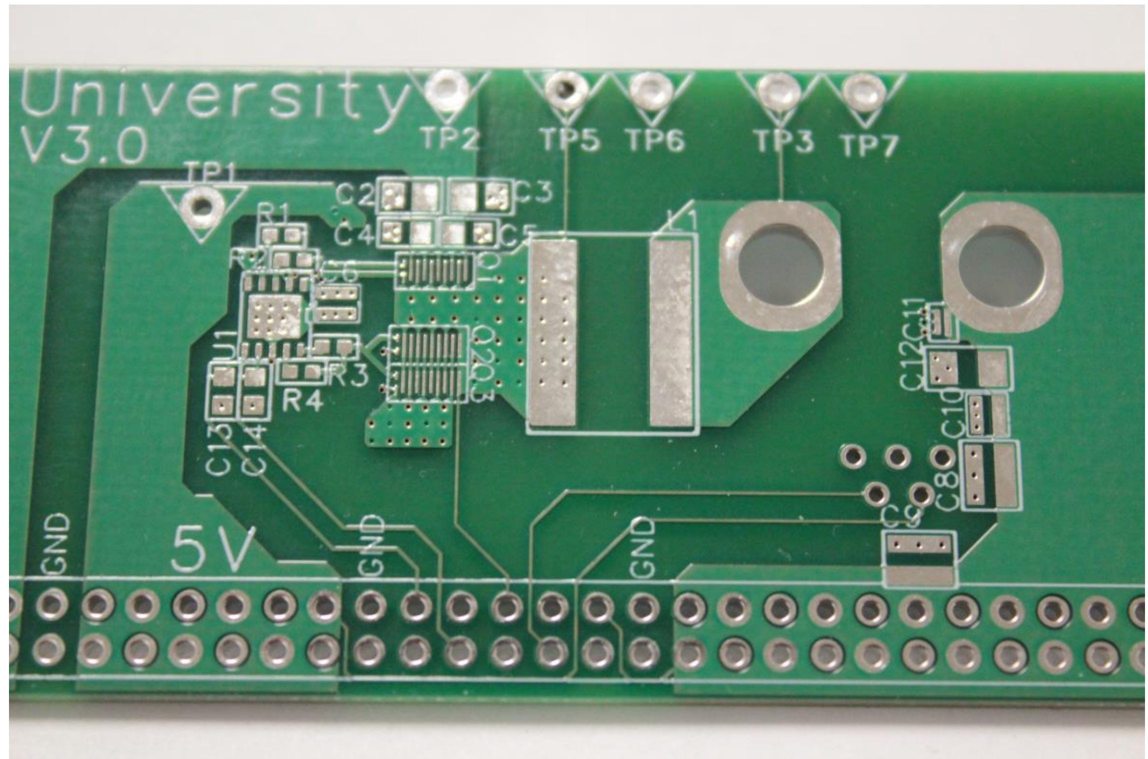


Figure 49: Version 3 unassembled converter daughter card

Once the EPC devices were soldered and verified via X-Ray, adhesive was placed on the edges of the parts to ensure there would be no movement while other components were soldered. The remaining surface mount components were usually soldered with the aid of the reflow oven, especially those connected to large copper pours, but components that could be done by hand typically were. These hand soldered components included the 0402 gate drive resistors, which while small, can be done by hand through the use of a quality soldering iron and ample workspace lighting and work piece magnification. Once all the surface mount components were

placed, the through-hole current sensor, test points, and 100pin connector were soldered on. These components are always done last as their plastics their packaging is composed of is usually unable to withstand the temperatures experienced in the reflow process. Figure 50 below shows a close-up of the regulator circuit on a POL daughter card, while Figure 51 shows an overview of a completely assembled and installed daughter card in the carrier mother board.

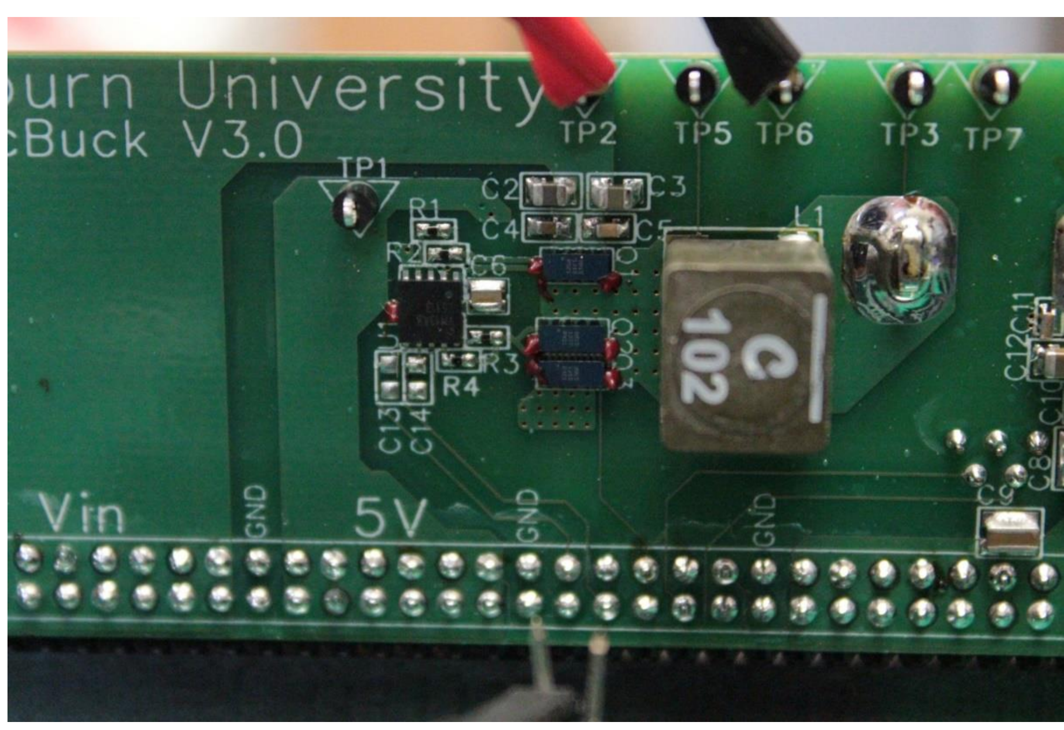


Figure 50: Assembled version 3 converter circuit.

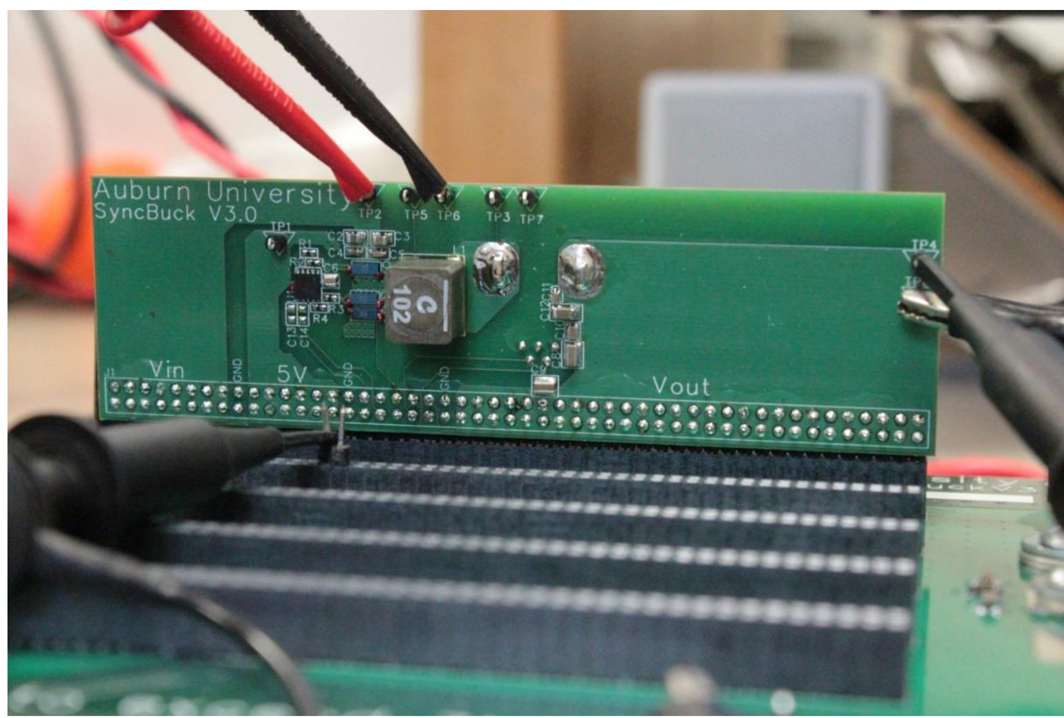


Figure 51: Daughter card installed in carrier board

Assembly of the carrier boards is relatively straightforward as the majority of the board is hand soldered, but if many boards are being populated at once the surface mount components can be placed and the board sent through the reflow oven. Figure 52 shows an image of an unpopulated carrier board. Due to the large number of connector pins in the design, boards that were intended to be used as control development platforms were only initially populated with one or two POL converter card connectors. Additional headers are easily added in the future should more be needed. The assembly process usually begins with the assembly of the passive components, along with the PCA I2C IO expanders. Figure 53 shows the left side of a populated carrier board.

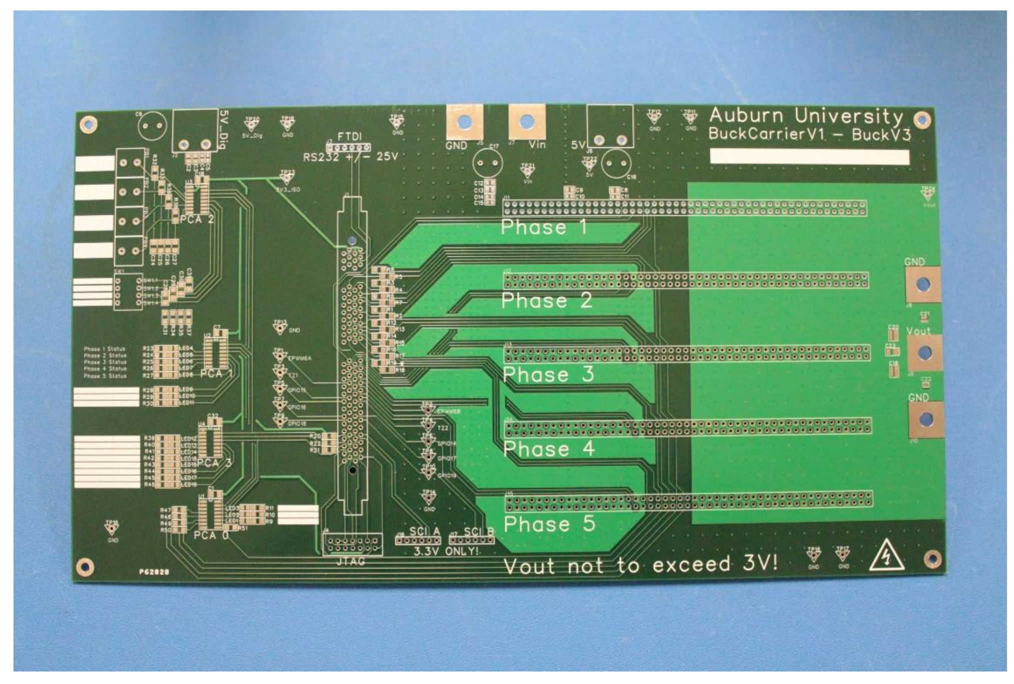


Figure 52: Unpopulated carrier board

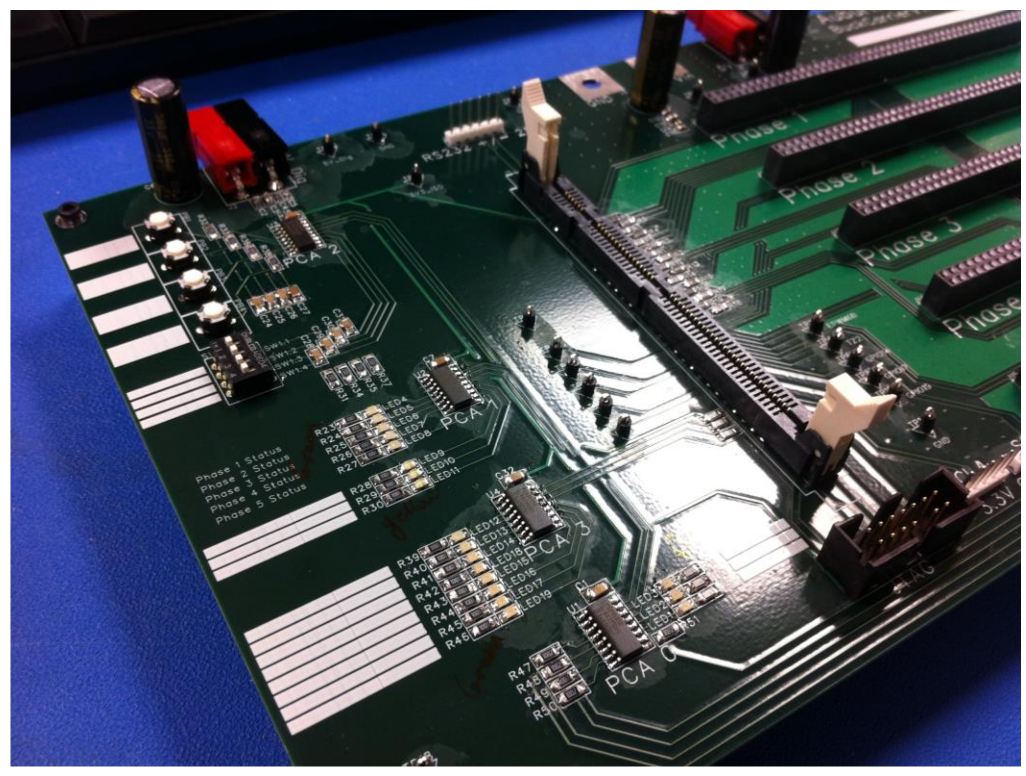


Figure 53: Populated control side of carrier board

Once all the surface mount components are in place, the board is flipped over and then the through-hole components are added in order of increasing height. Usually the 5V power connectors and the Ti Control Card header are the last components soldered in. The control card header requires the use of a finer tip on the iron and an appropriate flux to ensure clean joints with no bridging. The converter phase connectors and 5V power connectors and through hole capacitors typically require the use of a larger tip and a higher wattage iron with an appropriate flux to ensure enough thermal transfer in a short enough period of time to avoid damage to the board due to the large copper areas connected to this pins and the lack of any sort of thermal isolation on the pin pads. Figure 54 shows a control card installed in a carrier board with a converter card in the background, Figure 55 shows an alternate view of a single converter card installed in an operational carrier board.

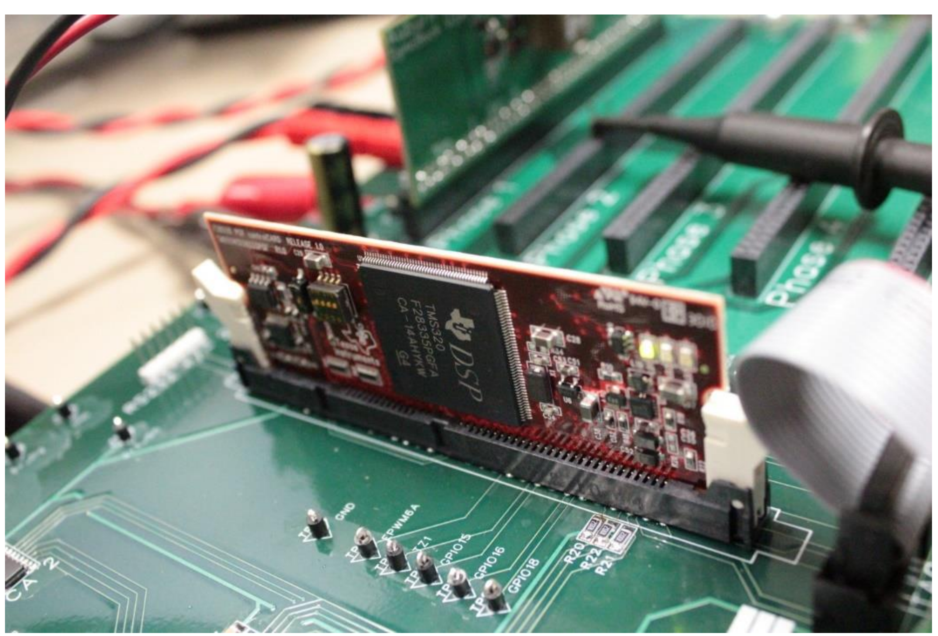


Figure 54: ControlCard installed in carrier board

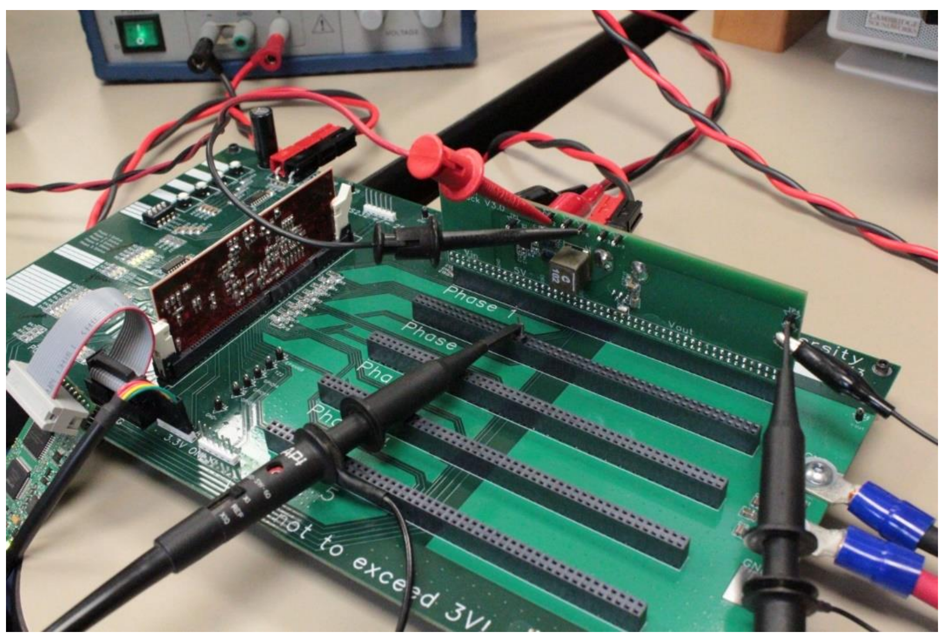


Figure 55: Converter daughter card installed and being tested

6.4 Testing and Analysis

Testing of the version 3 converter design began with several stages populated to the basic configuration of an EPC2015 switch and two EPC2015s as the synchronous rectifier. The new mother-daughter board design allowed for easy characterizations as stages could be inserted and removed as needed during the test process. This allowed for many boards to be tested within a short period of time, providing the opportunity for rapid advancements as our confidence with the new design grew. Characterization data taken from the first assembly power stages was done using open loop controls with none of the control groups algorithms implemented, allowing for pure comparisons between stages of the same configuration. Three stages that were assembled in the default configuration as shown in Figure 56 were separately installed into the carrier board and tested at various switching frequencies and at various loads by utilizing the adjustable load

board. Efficiency plots for each of these three converters at V_{In}=12V and V_{Out}=1V is shown in Figure 57, Figure 58, and in Figure 59.

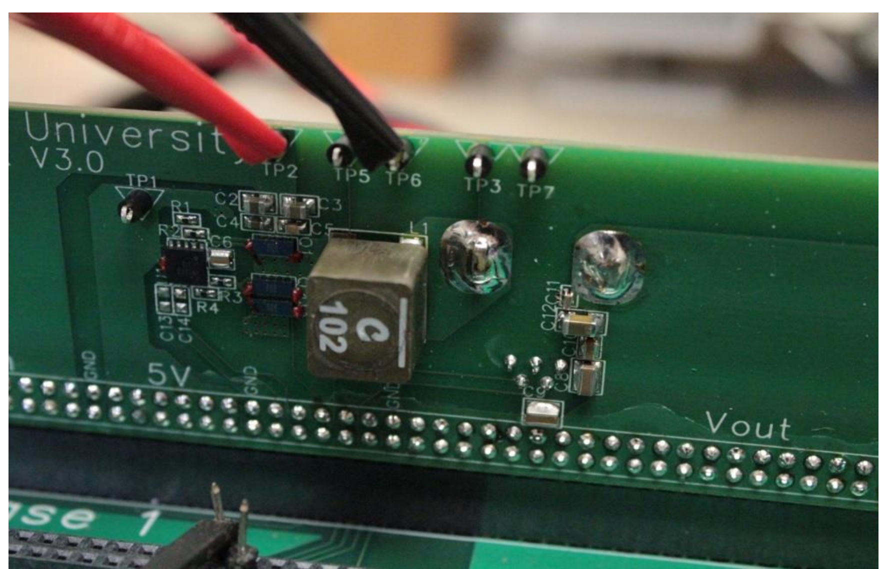


Figure 56: Default converter circuit assembled

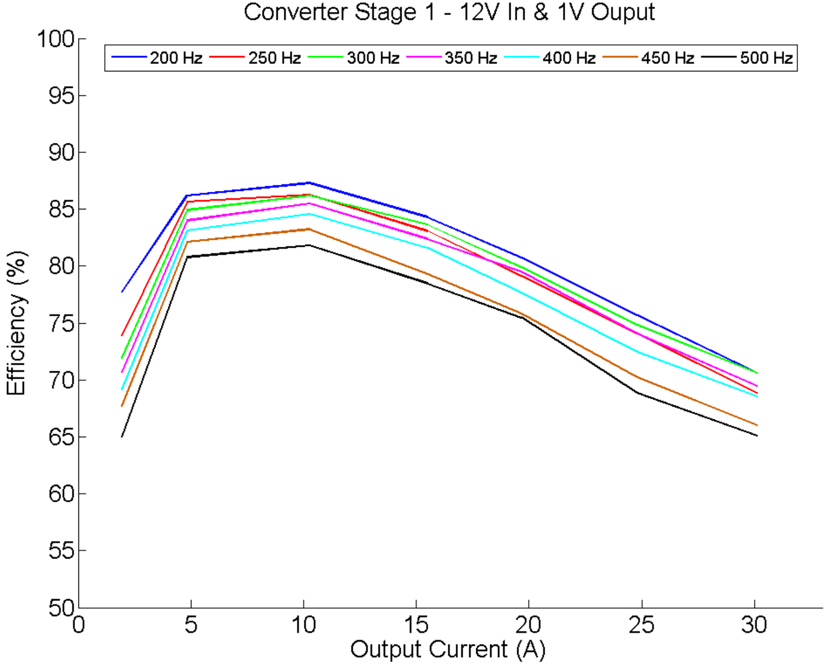


Figure 57: Efficiency data for power stage 1

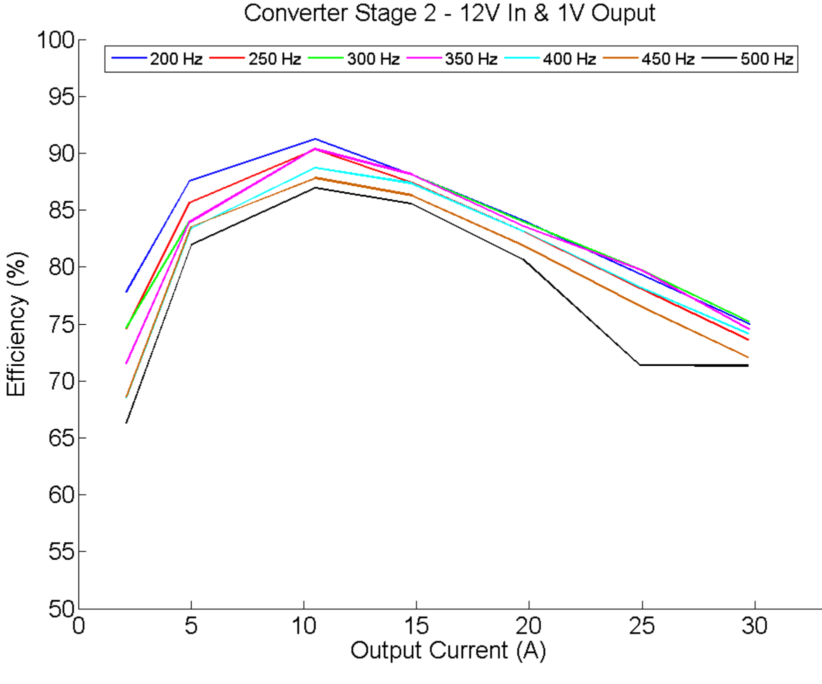


Figure 58: Efficiency data for power stage 2

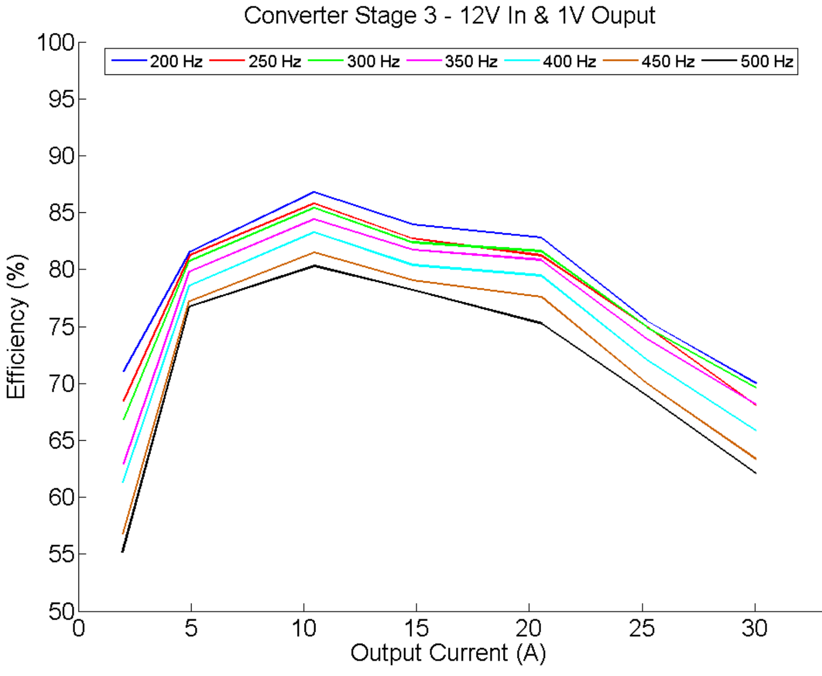


Figure 59: Efficiency data for power stage 3

Characterization runs of these three boards demonstrate the strong potential of the version 3 design, with boards 1 and 3 showing peak efficiencies in the range of 87% and stage 2 showing an efficiency of about 92%, with peak efficiency occurring at 10A load and 200kHz for each stage, with each stage maintaining efficiencies above 60% out to 30A load. Figure 60 shows an average of the three phase, displaying a peak efficiency of >88%. Also of note is the decrease in efficiency with increased operating frequency. This is due to increased switching losses, showing an almost linear relationship between an increase in frequency and a decrease in efficiency. Figure 61 shows a representation of this, showing the average delta in efficiency of the switching frequencies as the output current increases.

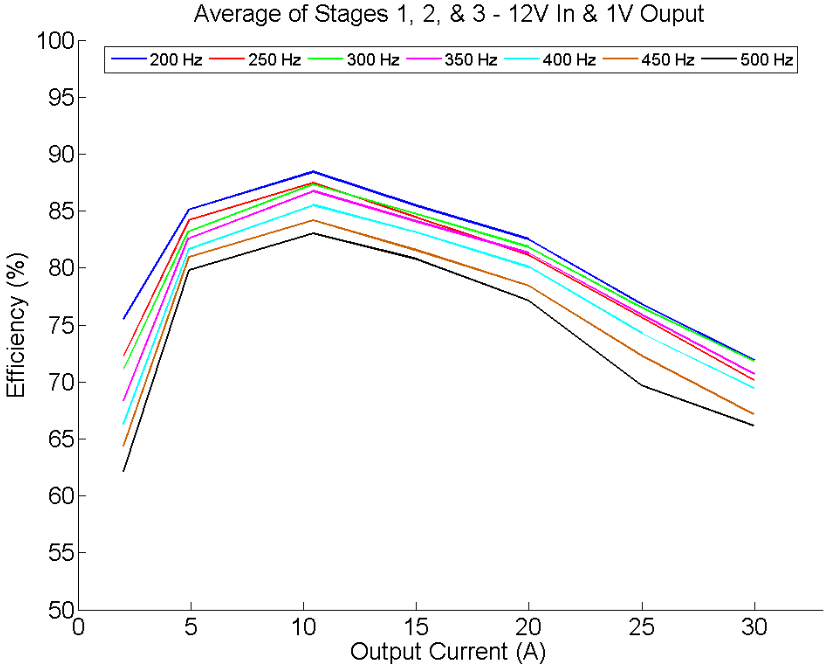


Figure 60: Average of efficiency data stages 1, 2, and 3

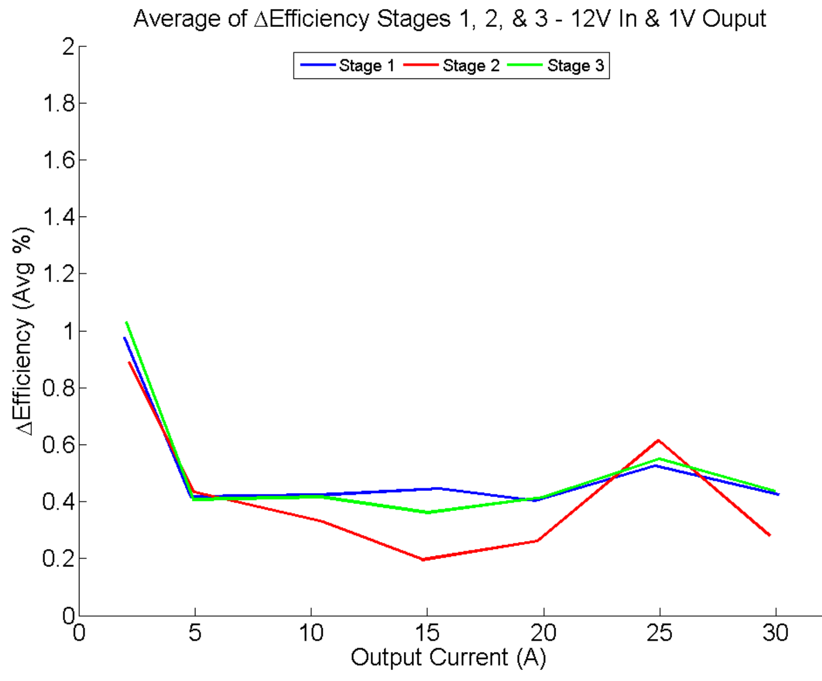


Figure 61: Average frequency efficiency delta

These metrics show a significant improvement over the version 2 design which had to be operated at very low V_{In} and I_{Out} to prevent circuit failure, showing version 3 immediately superior to the previous design in terms of performance potential. This difference in efficiencies between the individual stages was unexpected and has yet to be fully explained. The equipment, configuration, and setup for the testing of all three stages was identical, but it is known that testing of board 2 was done in a cooler room. Additional testing showed slight efficiency improvements with increased cooling, suggesting that the lower ambient temperatures, along with the possibility of slight differences in the quality of the assembly of the board may have contributed to the higher efficiency. Despite this, the circuit has shown to be very robust with power stages being run for hours at a time at high current loads without an operational failure, showcasing the robust nature of the version 3 design.

Once several default configuration stages had been characterized to prove operational functionality of the power stages and carrier board, several alternate FET configurations were assembled to provide comparison data. These boards were assembled utilizing the procedures in Chapter 3 with varied combinations of EPC2015 and EPC2014 FETs in order to test the capabilities of this combinations against the configuration of the default design. The combination of EPC2014 and EPC2015 devices used for each of these stages is shown below in Table 14.

Table 14: Power stage configurations

Stage #	Switch	Synchronous Rectifier
1,2,3	EPC2015	2x EPC2015
7	EPC2014	2x EPC2015
8	EPC2014	EPC2015
9	EPC2015	EPC2015

These boards were assembled in a similar order to the default configuration by utilizing the process in Chapter 4. Inclusion of the EPC2014 in this power stages complicated assembly slightly as the extra unused solder pads could pull the smaller EPC2014 off of the correct pads, requiring a rework process. Careful placement of the EPC2014 onto the pads and care during movement operations between assembly steps allowed for the EPC2014s to be populated without incident. Aside from the alternate switch configurations, these stages were populated in the same manner as the previously discusses stages. Figure 62, Figure 63 and Figure 64 show these alternate configuration stages fully populated.

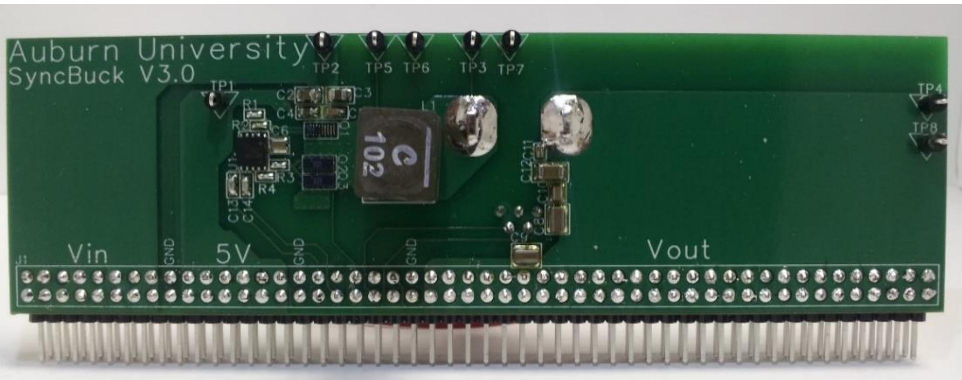


Figure 62: Assembled power stage 7

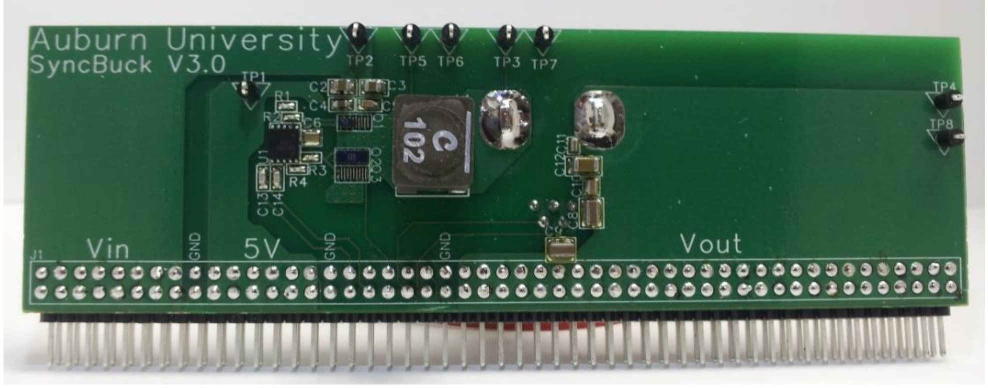


Figure 63: Assembled power stage 8

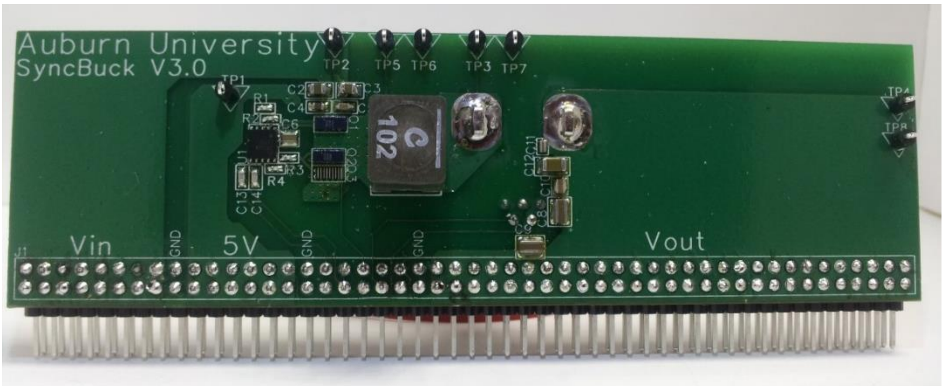


Figure 64: Assembled power stage 9

Testing of these stages was done in the same manner as the previous stages, with each being plugged individually into the carrier board and then test at various loads and various operating frequencies. Data from these runs shows some differences when compared to the previous default configuration stages, the primary difference being the inability of the EPC2014 to conduct the required amount of current to sustain high output loads. For this reason the data taken for the stages assembled with EPC2014 only show data points out to 20A of load as the

device quickly began to overheat, even with external cooling, at 25A. Figure 65 shows an image of stage 8 with the EPC2014 glowing under a 25A, 1V output load.

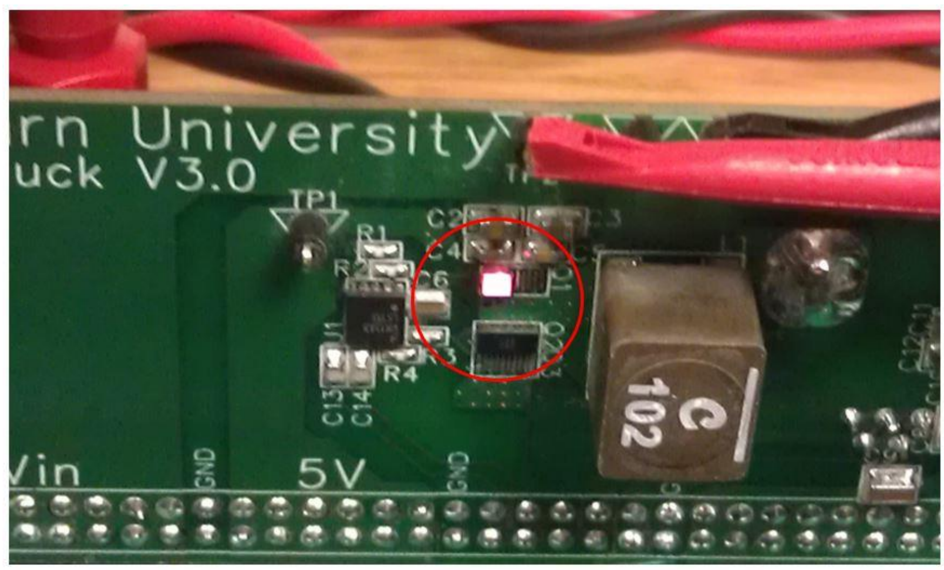


Figure 65: EPC2014 under high current load

Because of the limitation of the EPC2014, data for stages 7 and 8 is only presented to 20A output current. Data from stage 7 is shown below in Figure 66. This test was done at 12V V_{In} and 1V V_{Out}. From the data a similar trend to the default EPC2015 configuration can be seen, although the peak efficiency for this stage occurs below 10A. A closer look at the data also shows a decrease in the reduction in efficiency as operation frequency is increased. This is expected to be a result of lower switching losses in the EPC2014 based on its lower gate charge. While the efficiency at a max load of 20A is roughly on par with the efficiency of the default EPC2015 configuration at 20A, the EPC was unable to operate a high output currents so a full comparison with the default configuration cannot be made.

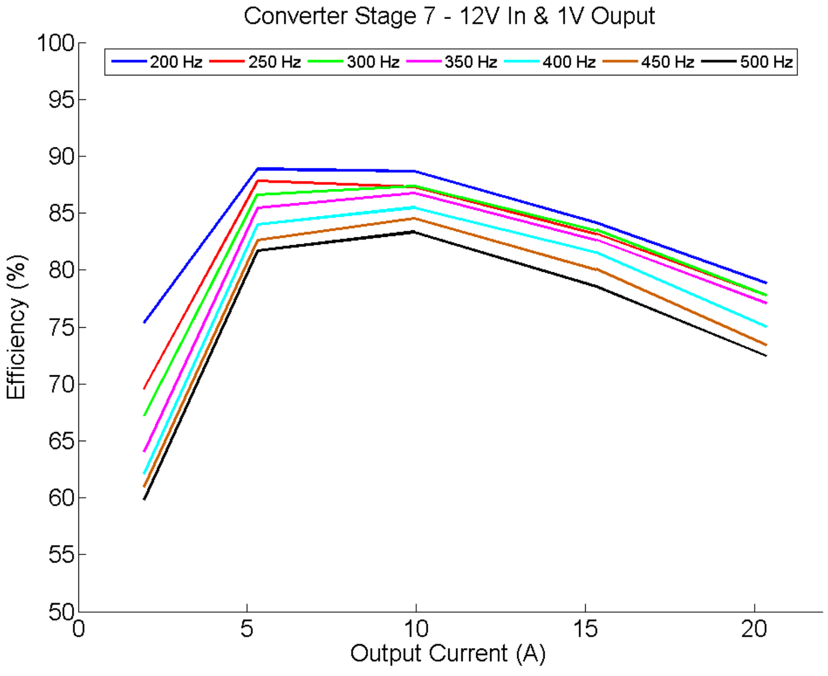


Figure 66: Efficiency data for power stage 7

Stage 8 was built using a combination of EPC2014 for the high side switch and a single EPC2015 for the synchronous rectifier. While this combination provides for lower switching losses, the use of only a single EPC2015 effectively doubles the resistance in the synchronous rectifier, and as shown in Figure 67 the efficiency of this stage suffers greatly because of it. The abnormality noted for the 200kHz dataset has been attributed to a very quick measurement on the stage before it came up to operational temperature. Notice that while the efficiency here is high, it does not exceed the efficiencies experienced by other stages. As with stage 7, testing for stage 8 stopped at 20A output load due to the inability of the EPC2014 to handle the current demands. Testing with stage 9 produced similarly low efficiencies as seen with stage 8 due to the singular EPC2015 being used as a synchronous rectified, while the effects of increased switching losses

with increased operating frequency at low current are very obvious from the data shown in Figure 68.

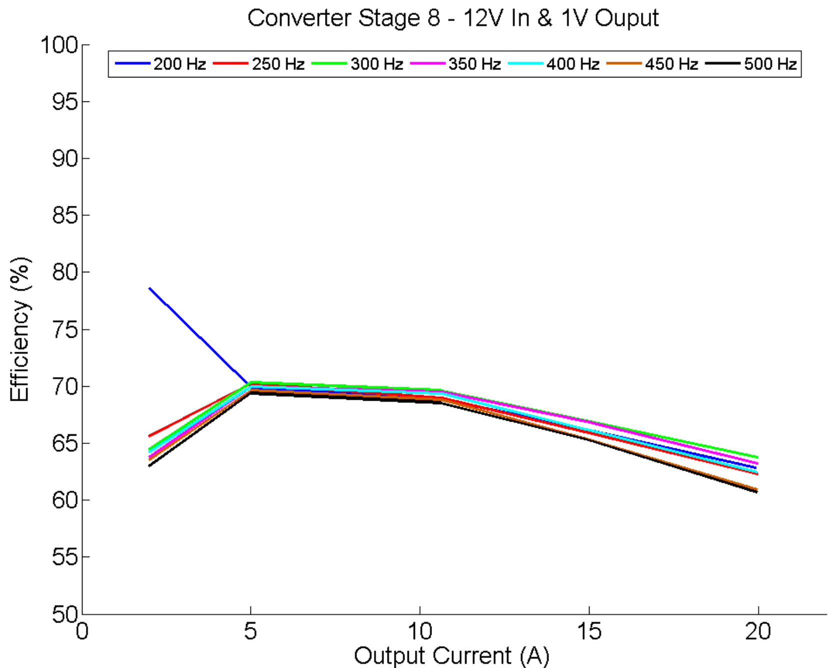


Figure 67: Efficiency data power stage 8

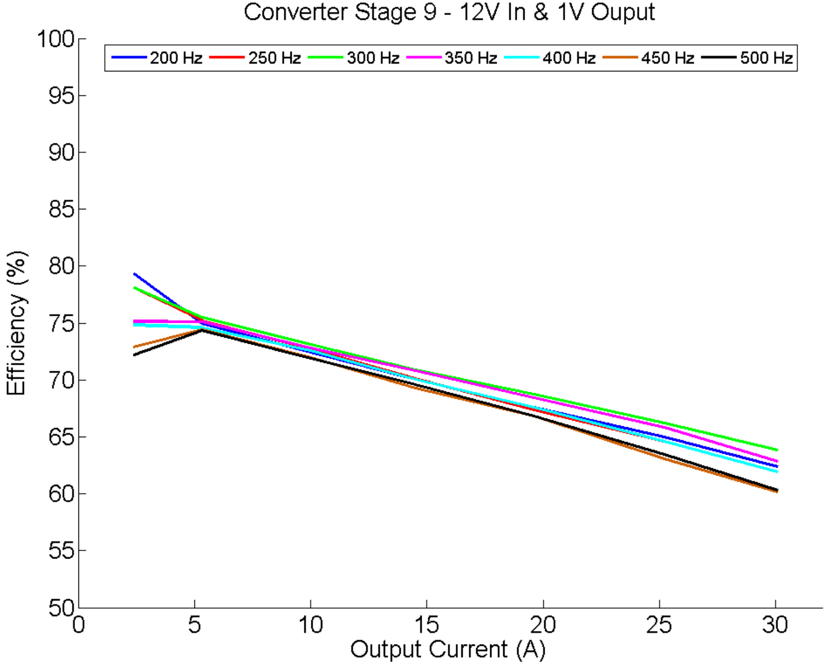


Figure 68: Efficiency data power stage 9

While testing did continue with additional converter stage boards, rapid updates in the design process generated updated power stages with higher realized efficiencies. As such, the version 3 design was never tested in a multiphase configuration and no data is available to present.

6.5 Conclusions

Testing of these alternate stages generated confirmation of the design decisions to use the EPC2015 in both the high side switch and synchronous rectifier positions, allowing the design to far exceed the performance capabilities of the version 2 design. The inability of the EPC2014 to operate at the higher currents needed for >20A output, combined with the issues encountered during reliability testing have resulted in the design team removing the EPC2014 from

consideration as a potential part for the high side switch in the POL converter. The testing of these altered stages also shows the efficiency advantages to be gained by using the EPC2015 in parallel to further reduce its on resistance. Based on conversations with EPC and according to the information published by them, paralleling up to four EPC2015 devices should continue to yield improvements, beyond four the returns begin to diminish substantially due to the additional gate drive requirements and increased switching losses [26]. This potential to decrease the on-resistance may prove to be very rewarding, especially at high currents, and will be investigated more in the future.

The version 3 design has shown to be very capable based on its ability to handle very large output currents while maintaining stable operation for long periods of time. The reliable operation it has delivered, coupled with its peak measured efficiency in the >90% range and efficiencies of >70% at 30A load further prove the capabilities of the design while it still has the potential to provide additional improvement as the testing discussed here was all done with open loop controls with efficiency measurements including losses associated with the 100-pin connector. Updates to the control software with implementation of multiphase operation and phase activation schemes mentioned in Chapter 2 and 3 would allow for even greater efficiencies to be realized utilizing the current converter circuit design. Future board revisions utilizing connectors such as the PCIB [76] and CBD [77] series from Positronic Industries Inc. would improve the design by allowing for a smaller daughter card design to be used, while lowering the connector insertion and removal forces.

Chapter 7 Conclusions

While GaN is still a young technology and its full capabilities have yet to be seen, the Point of Load converters demonstrated in this work show that it is possible to utilize these devices in a prototyping environment using limited tools to produce circuits capable of conversion efficiencies over 90%.

7.1 Summary

The version 2 converter board was the first implementation of GaN devices utilizing the novel assembly method described in Chapter 4. Using this method allowed for the creation of a multiphase buck converter that produced peak conversion efficiencies of 95%, with an average peak efficiency of 92%. Unfortunately this design did not take into proper account the sensitivities of the EPC2014 device, and repeated failures of the device during operation prevented this design from performing to its full potential. The issues within the design caused overvoltage conditions of the EPC2014 device when the input voltage was raised while the circuit was under load. It was determined that a maximum input voltage of only 2.5V allowed the circuit to operate for long enough periods to allow for data collection. Even with these issues, the version 2 design allowed for data to be collected on single and two phase operation of the converter, and demonstrated the potential of these GaN devices for use in high power converter designs.

The version 3 converter was built using the lessons learned from the version 2 design, and it proved to be a much more robust design. The version 3 circuit demonstrated peak

efficiencies in the 91% range with average peak efficiencies of approximately 87% utilizing a single EPC2015 for the high side switch, two EPC2015s as the synchronous rectifier, and the LM5113 gate driver. The version 3 circuit also demonstrated its ability to operate over a very large current range with a maximum output of 30A at efficiencies over 70% and to operate at high power levels for extended periods of time without performance degradation. The design change in the implementation of a mother-daughter board system allowed for rapid testing and updates to the design. This new structure allowed for other prototype converter circuits to be developed in parallel, using the base carrier board and control circuitry for the implementation of alternate circuits and devices.

7.2 Future work

One of the main issues when dealing with GaN devices is their susceptibility to any deficiencies within the layout, which prevents the circuit from meeting its maximum potential. Future versions of the converter circuit should continue to address layout optimization to fully realize the potential of these GaN devices as demonstrated in [78]. Steps should also be taken to ensure that the layout as a whole remains as tightly integrated as possible to ensure that parasitics that can create damaging transients within the circuit are kept to a minimum. This will allow the circuit to operate at higher switching speeds, allowing for smaller inductors and capacitors to be used in the design.

Additional updates to the design that further utilize the ability of the LM5113 to drive multiple parallel GaN devices should also be investigated in order to extract the maximum potential from these devices within this application, as discussed in [79]. Efforts should also be made to continue investigating new GaN and Si devices as they enter the market, as the ideal

choice of components for this design may be a hybrid approach that utilizes the best of what each technology has to offer. An implementation of this hybrid approach as a continuation of this work is discussed in [80]. Updates to the carrier-converter board connectors should also be made in order to further facilitate the ability to swap out converter cards for testing as needed and to further lower losses experienced within the testing circuit when operating under high load conditions.

References

[1] Prometeus GmbH, "TOP 500 November 2011," November 2011. [Online]. Available: http://www.top500.org/lists/2011/11/.

[2] Prometeus GmbH , "TOP 500 November 2013," November 2013. [Online]. Available: http://www.top500.org/lists/2013/11/.

[3] U.S. Energy Information Administration, "Frequently Asked Questions," 10 January 2014. [Online]. Available: http://www.eia.gov/tools/faqs/faq.cfm?id=97&t=3.

[4] K. E. Smedman, "A Power Supply System Application for a Large Telecom Data Center," in *Telecommunications Energy Conference, 1987. INTELEC '87. The Ninth International*, Stockholm, Sweden, 1987.

[5] S. Oliver, "High-voltage DC distribution is key to increased system efficiency and renewable-energy opportunities," November 2012. [Online]. Available: http://www.vicorpower.com/documents/whitepapers/wp-High-voltage-DC-Distribution.pdf.

[6] A. Bindra, "Is DC Power The Optimal Route For Data Centers To Improve Energy Efficiency?," August 2011. [Online]. Available: http://www.how2power.com/newsletters/1108/H2PowerToday1108_DigitalMedia.pdf.

[7] M. Murrill and B. Sonnenberg, "Evaluating the Opportunity for DC Power in the Data Center," 2010. [Online]. Available: http://www.emersonnetworkpower.com/documentation/en-us/brands/liebert/documents/white%20papers/124w-dcdata-web.pdf.

[8] Data Center Knowledge, "Special Report: The World's Largest Data Centers," [Online]. Available: http://www.datacenterknowledge.com/special-report-the-worlds-largest-data-centers/. [Accessed May 2012].

[9] SAKURA Internet, "Ishikari Data Center," 2011. [Online]. Available: http://ishikari.sakura.ad.jp/index_eng.html.

[10] Bomara Associates, "Alternative Big Data Center Power," [Online]. Available: http://www.bomara.com/powerware/wp_alternative_power.htm. [Accessed January 2014].

[11] R. Hallahan, "Data center design decisions and their impact on power system infrastructure," 2011. [Online]. Available: http://cumminspower.com/www/literature/technicalpapers/PT-9020-Data-Ctr-Design-Decisions.pdf.

[12] Data Center Knowledge, "Facebook Follows Google to Data Center Savings," 27 November 2009. [Online]. Available:

http://www.datacenterknowledge.com/archives/2009/11/27/facebook-follows-google-to-data-center-savings/.

[13] W. Tschudi, "DC Power for Improved Data Center Efficiency," March 2008. [Online]. Available: http://hightech.lbl.gov/documents/data_centers/DCDemoFinalReport.pdf.

[14] A. Bindra, "High-Voltage DC Distribution Improves Data Center System Efficiency," Hearst Electronic Products, January 2014. [Online]. Available: http://www.digikey.com/en-US/articles/techzone/2014/jan/high-voltage-dc-distribution-improves-data-center-system-efficiency.

[15] L. Casey and M. F. Schlecht, "A High-Frequency , Low Volume, Point-of-Load Power Supply for Distributed Power Systems," *IEEE Transactions on Power Electronics,* vol. 3, no. 1, pp. 72-82, 1988.

[16] R. Fisher, A. Yerman, G. Claydon and M. Kuo, "A 1 MHz, 100 W commercial, high-density point-of-load power supply using direct-bond copper and surface mount technologies," in *Applied Power Electronics Conference and Exposition, 1990. APEC '90, Conference Proceedings 1990., Fifth Annual*, Los Angeles, CA, 1990.

[17] S. Nagar, F. A.-Z. Said, M. Orabi and A. Abou-Alfotouh, "Design of High Performance Point of Load Converters with Ultra-Low Output Voltage Ripple," in *2010 IEEE Energy Conversion Congress and Exposition (ECCE)*, Atlanta, GA, 2010.

[18] V. W. Ng, M. D. Seeman and S. R. Sanders, "Minimum PCB Footprint Point-of-Load DC-DC Converter Realized with Switched-Capacitor Architecture," in *Energy Conversion Congress and Exposition, 2009. ECCE 2009. IEEE*, San Jose, CA, 2009.

[19] X. Zhou, M. Donati, L. Amoroso and F. C. Lee, "Improved light-load efficiency for synchronous rectifier voltage regulator module," *IEEE Transactions on Power Electronics,* vol. 15, no. 5, pp. 826-834, 2000.

[20] P. Xu, J. Wei and F. C. Lee, "Multiphase coupled-buck converter-a novel high efficient 12 V voltage regulator module," *IEEE Transactions on Power Electronics,* vol. 18, no. 1, pp. 74-82, 2003.

[21] A. Lidow and J. Strydom, "Gallium Nitride (GaN) Technology Overview," 2012. [Online]. Available: http://epc-co.com/epc/documents/papers/Gallium%20Nitride%20GaN%20Technology%20Overview.pdf.

[22] J. Sherman and J. Herbsommer, "Advancing Silicon Performance Beyond the Capabilities of Discrete Power MOSFETs," *Bodo's Power Systems,* no. 08-10, p. 5, 2010.

[23] ROHM Semiconductor, "Silicon Carbide Schottky Barrier Diodes," 2011. [Online]. Available: http://www.rohm.com/documents/11308/12928/ROHM_SiC+Diodes_wp.pdf.

[24] N. Kaminski, "State of the art and the future of wide band-gap devices," in *Power Electronics and Applications, 2009. EPE '09. 13th European Conference on*, Barcelona, 2009.

[25] U. K. Mishra, P. Parikh and Y.-F. Wu, "AlGaN/GaN HEMTs-an overview of device operation and applications," *Proceedings of the IEEE ,* vol. 90, no. 6, pp. 1022-1031, 2002.

[26] A. Lidow, J. Stydom, M. d. Rooij and T. Ma, GaN Transistors for Efficient Power Conversion, El Segundo: Power Conversion Publications, 2012.

[27] Efficient Power Conversion, "EPC2014 – Enhancement Mode Power Transistor," 2013. [Online]. Available: http://epc-co.com/epc/documents/datasheets/EPC2014_datasheet.pdf.

[28] Efficient Power Conversion, "EPC2015 – Enhancement Mode Power Transistor," 2013. [Online]. Available: http://epc-co.com/epc/documents/datasheets/EPC2015_datasheet.pdf.

[29] Efficient Power Conversion, "EPC2001 – Enhancement Mode Power Transistor," 2013. [Online]. Available: http://epc-co.com/epc/documents/datasheets/EPC2001_datasheet.pdf.

[30] Infineon, "BSC010NE2LS OptiMOSTM Power-MOSFET," 2013. [Online]. Available: http://www.infineon.com/dgdl/BSC010NE2LS_rev2.2.pdf?folderId=db3a304326dfb1300126fb3bec803f1a&fileId=db3a304326dfb1300126fb3d176a3f1b.

[31] NXP, "PSMN5R6-100PS, N-channel 100 V 5.6 mΩ standard level MOSFET in TO220," November 2012. [Online]. Available: http://www.nxp.com/documents/data_sheet/PSMN5R6-100PS.pdf.

[32] Texas Instruments, "CSD17306Q5A, 30V, N-Channel NexFET™ Power MOSFETs," July 2010. [Online]. Available: http://www.ti.com/lit/ds/symlink/csd17306q5a.pdf.

[33] G. Schuellein, "Multiphase buck converter design responds well to transients," EE Times, 13 September 2000. [Online]. Available: http://www.eetimes.com/document.asp?doc_id=1224753.

[34] T. Hegarty, "Benefits of multiphasing buck converters - Part 1," EE Times, 17 November 2007. [Online]. Available: http://www.eetimes.com/document.asp?doc_id=1273224.

[35] T. Hegarty, "Benefits of multiphasing buck converters - Part 2," EE Times, 24 November 2007. [Online]. Available: http://www.eetimes.com/document.asp?doc_id=1273225.

[36] H. Nguyen, Design, Analysis and Implementation of Multiphase Synchronous Buck DC-DC Converter for Transportable Processor, Blacksburg, Virginia: Virginia Polytechnic

Institute and State University, 2004.

[37] L. K. Wong and T. K. Man, "Tip of the Week: How to best implement a synchronous buck converter," EE Times, 26 April 2008. [Online]. Available: http://www.eetimes.com/document.asp?doc_id=1273245.

[38] J. W. Kimball and P. T. Krein, "Analysis and Design of Switched Capacitor Converters," in *Applied Power Electronics Conference and Exposition, 2005. APEC 2005. Twentieth Annual IEEE*, Austin, TX, 2005.

[39] V. W.-S. Ng and S. R. Sanders, "Switched Capacitor DC-DC Converter: Superior where the Buck Converter has Dominated," 17 August 2011. [Online]. Available: http://www.eecs.berkeley.edu/Pubs/TechRpts/2011/EECS-2011-94.pdf.

[40] O. Keiser, P. K. Steimer and J. W. Kolar, "High power resonant Switched-Capacitor step-down converter," in *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE*, Rhodes, 2008.

[41] L. Wuidart, "Topologies for Switched Mode Power Supplies," March 93. [Online]. Available: http://w5jgv.com/hv-ps1/pdf/topologies_for_switched_mode_power_supplies.pdf.

[42] Fairchild Semiconductor, "A Fresh Approach to Switching Regulator Topologies and Implementations," 2006. [Online]. Available: http://www.fairchildsemi.co.kr/Assets/zSystem/documents/collateral/onlineSeminars/A-Fresh-Approach-to-Switching-Regulator-Topologies-and-Implementations-PPT.pdf.

[43] B. Mammano, "Resonant Mode Converter Topologies," 2001. [Online]. Available: http://www.ti.com/lit/ml/slup085/slup085.pdf.

[44] B. Andreycak, "Zero Voltage Switching Resonant Power Conversion," 1999. [Online]. Available: http://www.ti.com/lit/an/slua159/slua159.pdf.

[45] ON Semiconductor, "Switchmode Power Supply Reference Manual," July 2002. [Online]. Available: http://www.onsemi.com/pub_link/Collateral/SMPSRM-D.PDF.

[46] Texas Intruments, "Power Supply Topologies," 2011. [Online]. Available: http://www.ti.com/lit/sg/sluw001e/sluw001e.pdf.

[47] M. Kamil, "Switch Mode Power Supply (SMPS) Topologies (Part I)," 2007. [Online]. Available: http://ww1.microchip.com/downloads/en/appnotes/01114a.pdf.

[48] A. Bersani, "Switch Mode Power Supply (SMPS) Topologies (Part II)," 2009. [Online]. Available: http://ww1.microchip.com/downloads/en/appnotes/01207b.pdf.

[49] R. Simanjorang, "Estimating performance of high output power density 400/400V isolated DC/DC converter with hybrid pair SJ-SBD for power supply of data center," in *Telecommunications Energy Conference, 2009. INTELEC 2009. 31st International*, Incheon, 2009.

[50] Efficient Power Conversion, "Quick Reference – Die Attach," [Online]. Available: http://epc-co.com/epc/documents/product-training/quick-reference-die-attach.pdf.

[51] L. J. S. H. C. W. J. T. J. M. M. P. a. R. D. S.W. Henning, "Manual assembly of 400um bumped-die GaN power semiconductor devices," in *Proc. of the IMAPS 2012 Symposium*, San Diego, CA, 2012.

[52] GE Measurement & Control, "phoenix|x-ray," GE, 2014. [Online]. Available: http://www.ge-mcs.com/en/phoenix-xray.html.

[53] Microchip, "dsPIC30F2023," [Online]. Available: https://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en026341.

[54] Digilent, "Atlys™ Spartan-6 FPGA Development Board," [Online]. Available: http://www.digilentinc.com/Products/Detail.cfm?NavPath=2,400,836&Prod=ATLYS&CFID=4473524&CFTOKEN=728f1bbc44133911-3A844CEE-5056-0201-022CEEFFCEB10295.

[55] Intersil, "EL7158 Ultra-High Current Pin Driver," [Online]. Available: http://www.intersil.com/content/dam/Intersil/documents/el71/el7158.pdf.

[56] Linear Technology, "LTC4440-5 High Speed, High Voltage, High Side Gate Driver," [Online]. Available: http://cds.linear.com/docs/en/datasheet/44405fb.pdf.

[57] ON Semi, "MBRB4030G SWITCHMODE Power Rectifier," [Online]. Available: http://www.onsemi.com/pub_link/Collateral/MBRB4030-D.PDF.

[58] Wurth Elektronik, "7443556130 WE-HCI SMD Flat Wire High Current Inductor," [Online]. Available: http://katalog.we-online.de/pbs/datasheet/7443556130.pdf.

[59] Texas Instruments, "AN-1197 Selecting Inductors for Buck Converters," May 2001, Revised 2013. [Online]. Available: http://www.ti.com/lit/an/snva038b/snva038b.pdf.

[60] B. Hutchings, "SMPS Buck Converter Design Example," 5 September 2006. [Online]. Available: http://www.microchip.com/webinars.microchip.com/WebinarDetails.aspx?dDocName=en528032.

[61] ROHM Semiconductor, "Capacitor Calculation for Buck converter IC," 2014. [Online]. Available:

http://rohmfs.rohm.com/en/products/databook/applinote/ic/power/switching_regulator/capacitor_calculation_appli-e.pdf.

[62] ST Microelectronics, "MOSFET Device Effects on Phase Node Ringing in VRM Power Converters," June 2005. [Online]. Available: http://tec.icbuy.com/uploads/2012/12/7/AN2170_MOSFET_Device_Effects_on_Phase_Node_Ringing_in_VRM_Power_Converters_1.1.pdf.

[63] M. Brown, "Considerations in Designing the Printed Circuit Boards of Embedded Switching Power Supplies," 30 April 1999. [Online]. Available: https://www.fairchildsemi.com/an/AN/AN-1031.pdf.

[64] E. Abdoulin, S. Colino and A. Nakata, "Using Enhancement Mode GaN-on-Silicon Power Transistors," 2011. [Online]. Available: http://epc-co.com/epc/documents/product-training/Using_GaN_r4.pdf.

[65] Texas Instruments, "LM5113," [Online]. Available: http://www.ti.com/product/lm5113.

[66] Z. Chen and I. Amaro, "Optimizing Low Side Gate Resistance for Damping Phase Node Ringing of Synchronous Buck Converter," [Online]. Available: http://www.onsemi.com/site/pdf/PID001.pdf.

[67] J. Klein, "“Shoot-through” in Synchronous Buck Converters," 25 April 2003. [Online]. Available: https://www.fairchildsemi.com/an/AN/AN-6003.pdf.

[68] J. Cain, "Parasitic Inductance of Multilayer Ceramic Capacitors," [Online]. Available: http://www.avx.com/docs/techinfo/parasitc.pdf. [Accessed January 2012].

[69] J. Moses, L. Jenkins, S. Henning, J. Tennant, C. Wilson and R. Dean, "Reliability testing of power semiconductors over 1000 hours," in *Proc. of the GOMACHTech-14 Conference*, Charleston, SC, March 31 - April 3, 2014.

[70] J. Moses and J. A. W. A. S. H. J. T. C. W. R. D. L.L. Jenkins, "GaN HEMT reliability at 125 oC for 1000 hours," in *Proc. of the IEEE Workshop on Wide Bandgap Power Devices and Applications*, Columbus, OH, Oct. 27-29, 2013.

[71] Coilcraft, "XAL1010 Series High Current Shielded Power Inductors," [Online]. Available: http://www.coilcraft.com/xal1010.cfm.

[72] Asahi Kasei Microdevices Coporation, "CQ-2065 Open Loop Current Sensor," [Online]. Available: http://www.akm.com/akm/en/product/datasheet1/?partno=CQ-2065.

[73] Texas Instruments, "TMS320F28335 Delfino Microcontroller," [Online]. Available: http://www.ti.com/product/tms320f28335.

[74] Texas Instruments, "TMS320F28335 controlCARD," [Online]. Available: http://www.ti.com/tool/tmdscncd28335.

[75] NXP, "PCA9531 8-bit I2C-bus LED dimmer," [Online]. Available: http://www.nxp.com/documents/data_sheet/PCA9531.pdf.

[76] Positronic, "COMPACT POWER CONNECTOR," [Online]. Available: http://www.connectpositronic.com/connectors/power/compact-power-connector/.

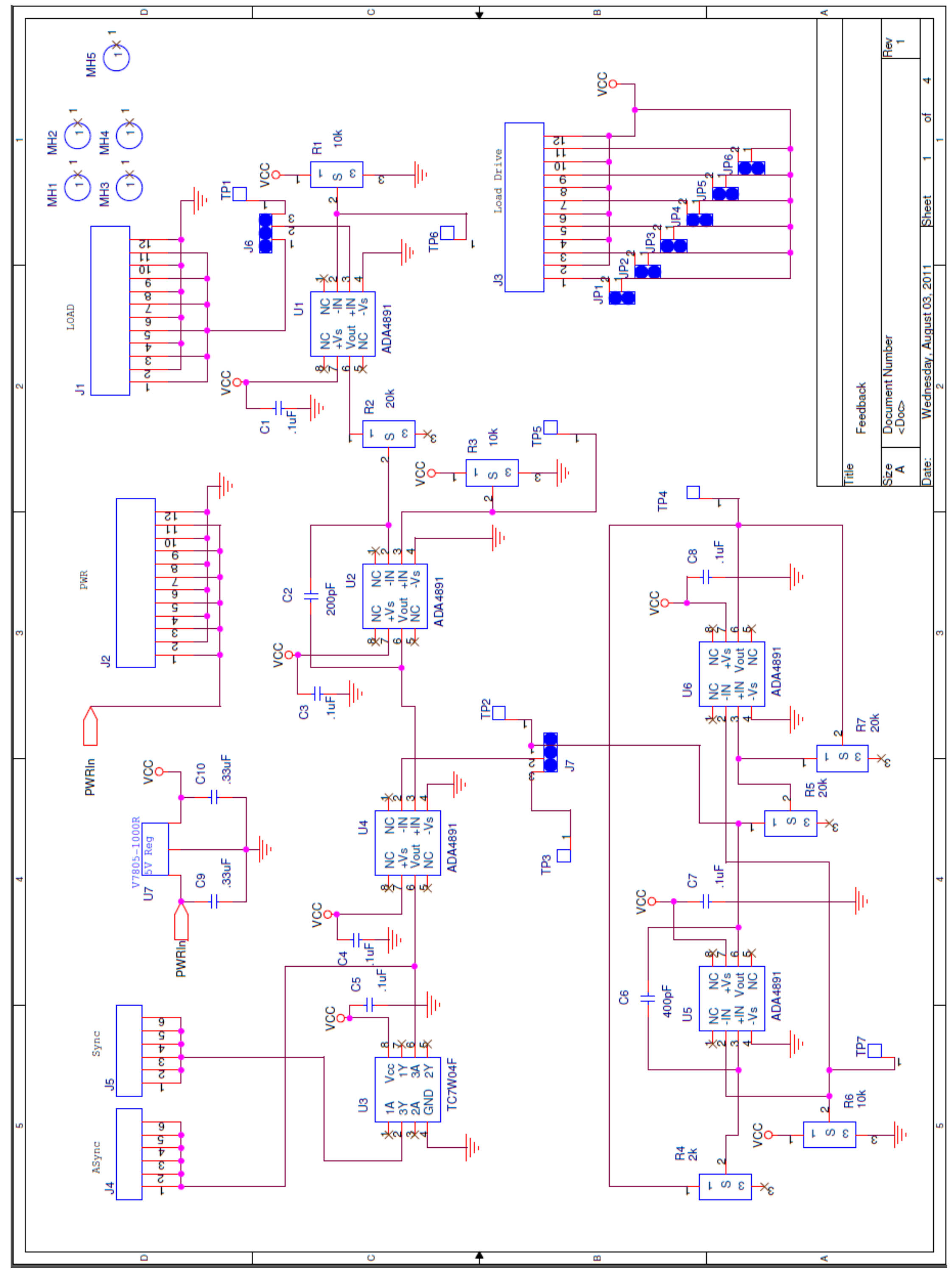
[77] Positronic, "COMBO-D," [Online]. Available: http://www.connectpositronic.com/connectors/power/standard-density-combo-d/.

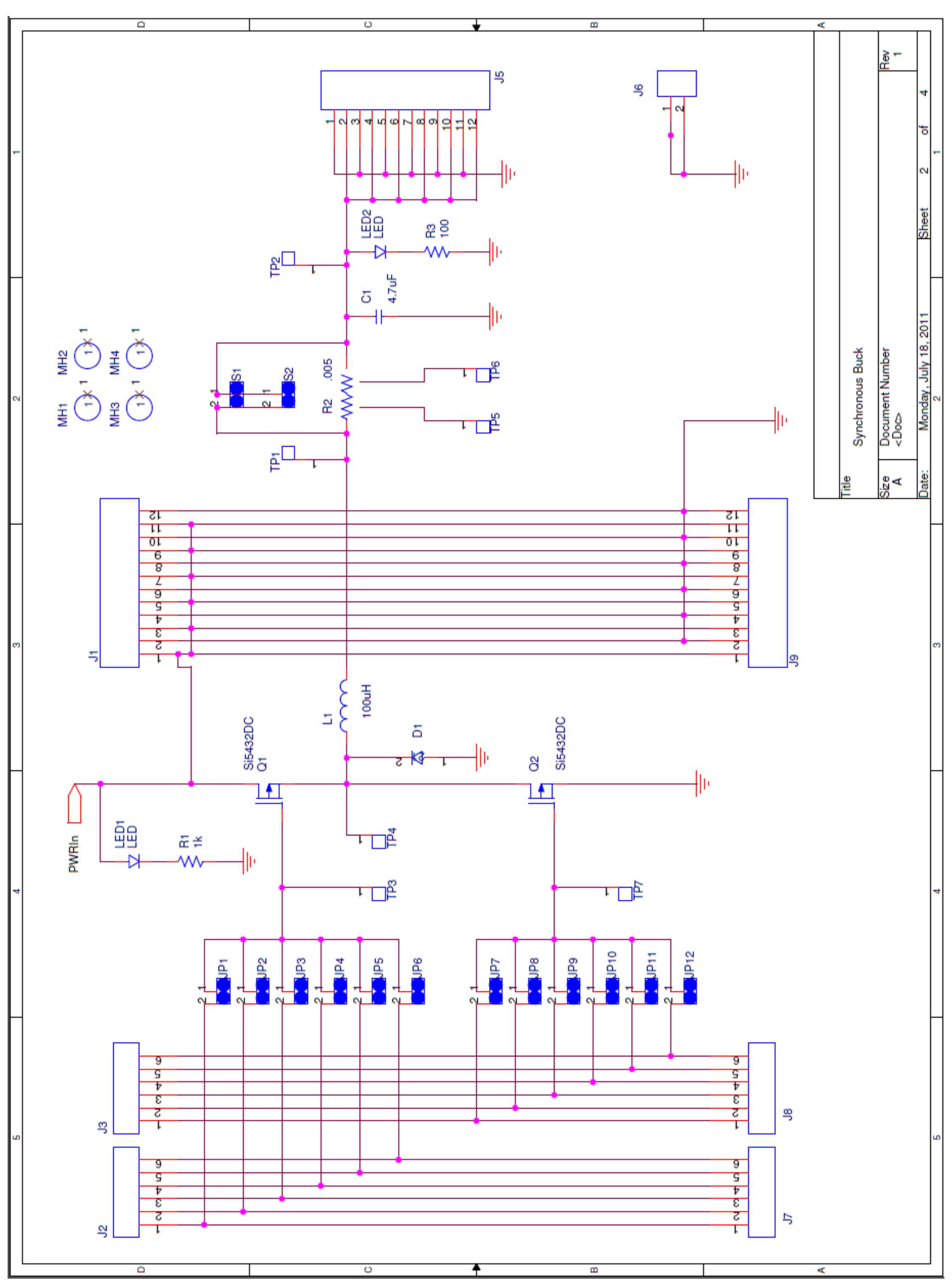
[78] L. Jenkins, C. Wilson, J. Moses, J. Aggas, B. Rhea and R. Dean, "Optimization of a 96% efficient 12-1 V gallium nitride based point of load converter," in *Proc. of the 2014 IEEE Applied Power Electronics Conference*, Fort Worth, TX, Mar. 16-20, 2014.

[79] L. Jenkins, C. Wilson, J. Moses, J. Aggas, B. Rhea and R. Dean, "The impact of parallel GaN HEMTs on efficiency of a 12-to-1 V buck converter," in *Proc. of the IEEE Workshop on Wide Bandgap Power Devices and Applications*, Columbus, OH, Oct. 27-29, 2013.

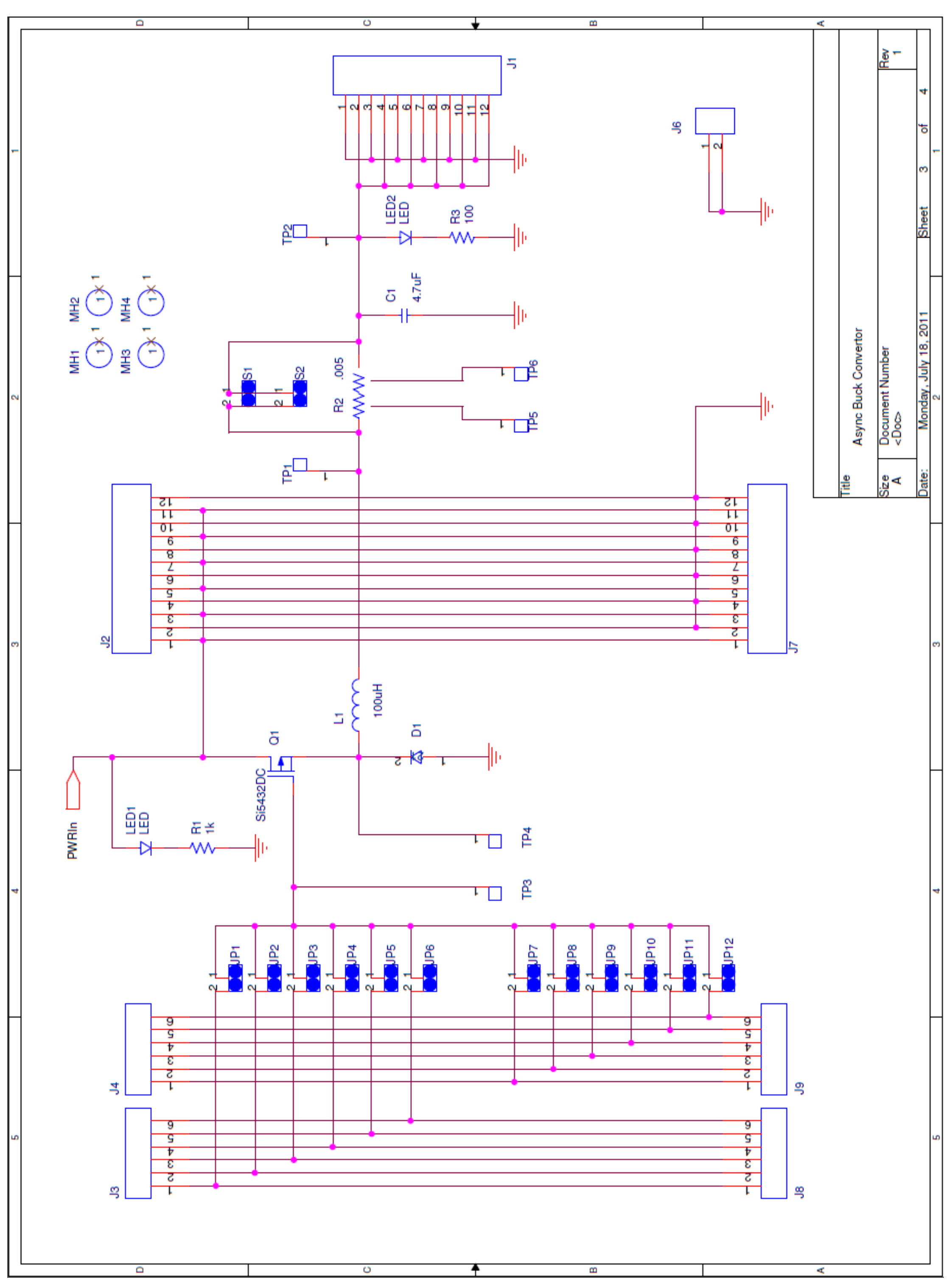
[80] L. Jenkins, C. Wilson, J. Moses, J. Aggas, W. Abell and R. Dean, "Performance comparison of multiphase GaN vs. GaN/Si hybrid 12/1 V POL converters," in *Proc. of the GOMACHTech-14 Conference*, Charleston, SC, March 31 - April 3, 2014.

Appendix A: POL V1 Schematics

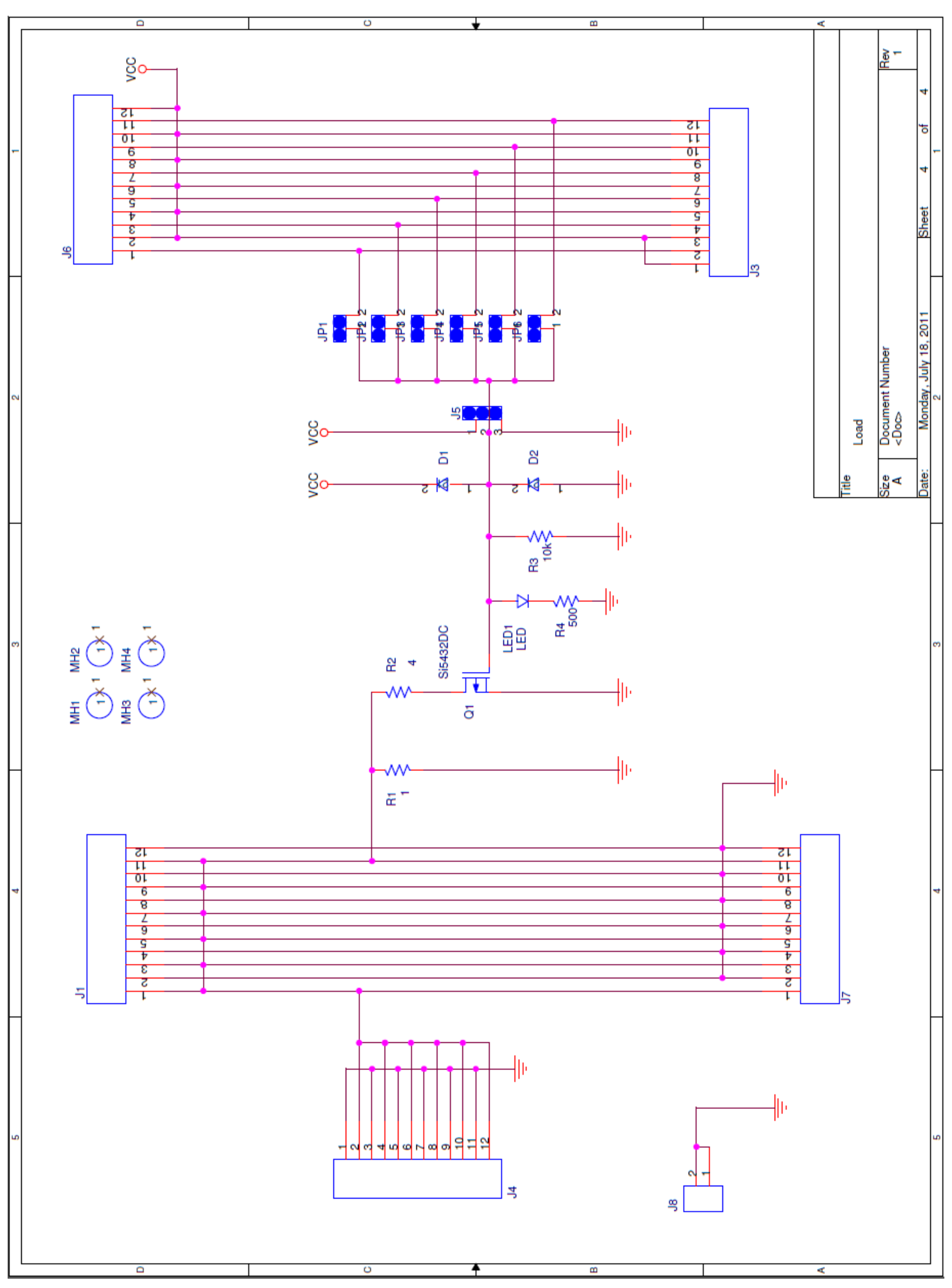




Title
Synchronous Buck
Size
A
Document Number
<Doc>
Rev
1
Date:
Monday, July 18, 2011
Sheet
2
of
4
PWRIn
LED1
LED
R1
1k
Q1
Si5432DC
Q2
Si5432DC
L1
100uH
D1
R2
.005
C1
4.7uF
LED2
LED
R3
100
S1
S2
TP1
TP2
TP3
TP4
TP5
TP6
TP7
MH1
MH2
MH3
MH4
J1
J2
J3
J5
J6
J7
J8
J9
JP1
JP2
JP3
JP4
JP5
JP6
JP7
JP8
JP9
JP10
JP11
JP12



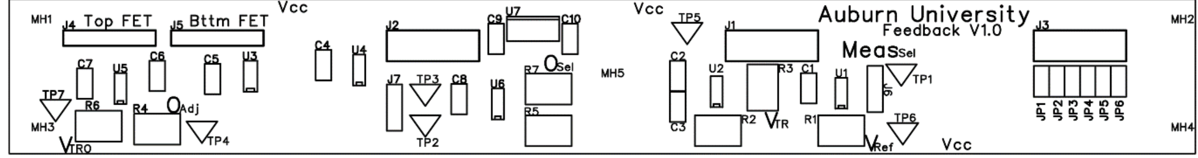
J1
J2
J3
J4
J6
J7
J8
J9
TP1
TP2
TP3
TP4
TP5
TP6
MH1
MH2
MH3
MH4
S1
S2
LED2
LED
R3
100
C1
4.7uF
R2
.005
L1
100uH
D1
Q1
Si5432DC
PWRIn
LED1
LED
R1
1k
JP1
JP2
JP3
JP4
JP5
JP6
JP7
JP8
JP9
JP10
JP11
JP12
Title
Async Buck Convertor
Size
A
Document Number
<Doc>
Rev
1
Date: Monday, July 18, 2011
Sheet 3 of 4


VCC
J6
J3
JP1
JP2
JP3
JP4
JP5
JP6
J5
D1
D2
R3
10k
R4
500
LED1
LED
R2
4
Si5432DC
Q1
R1
1
MH1
MH2
MH3
MH4
J1
J7
J4
J8
Title
Load
Size
A
Document Number
<Doc>
Rev
1
Date: Monday, July 18, 2011
Sheet 4 of 4

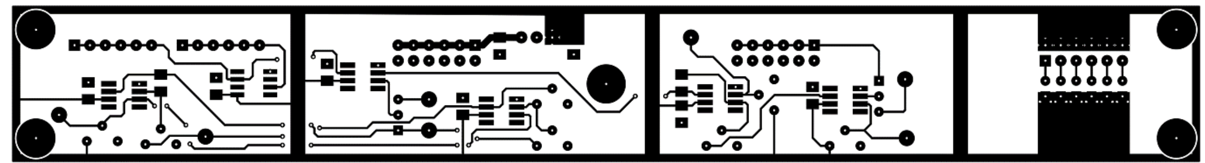
Appendix B: POL V1 Layout

B.1 Feedback

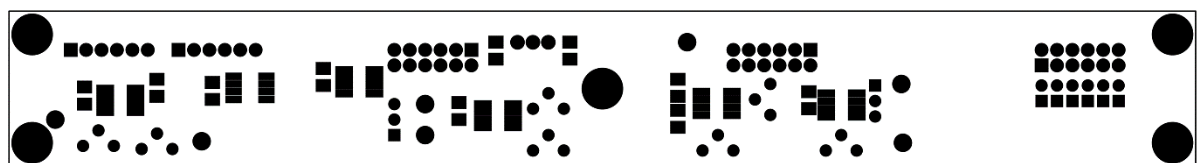
Top Silk



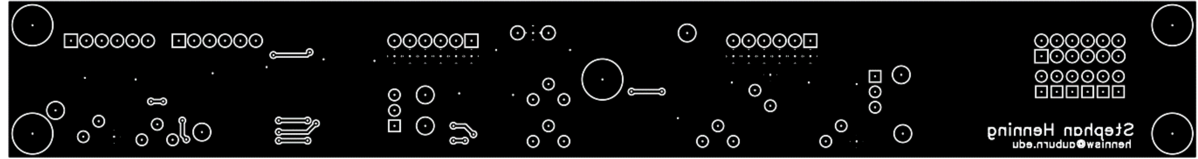
Top Copper



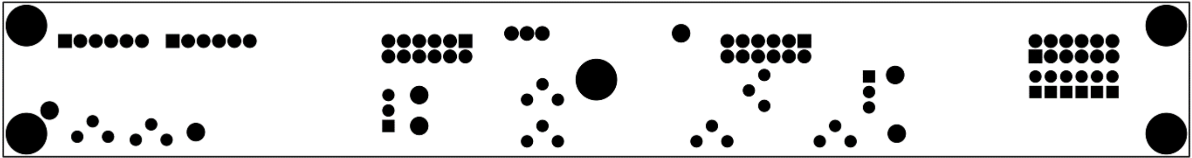
Top Soldermask



Bottom Copper

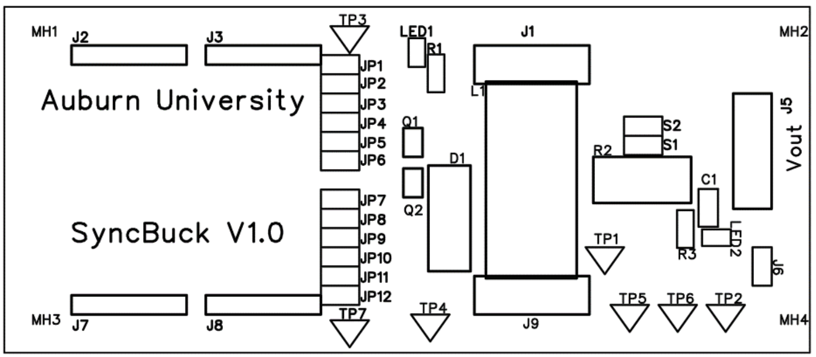


Bottom Soldermask

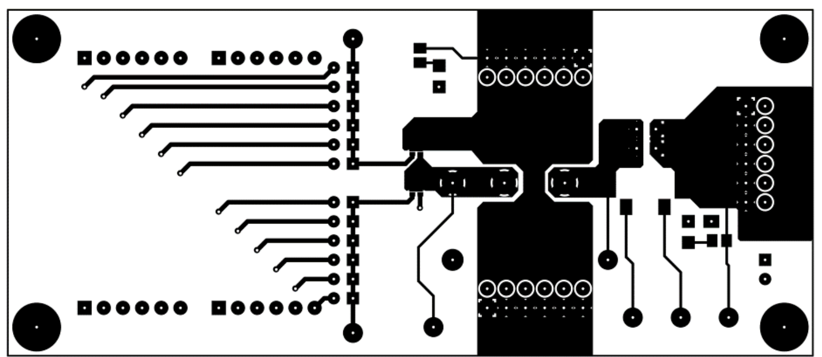


B.2 Synchronous Buck

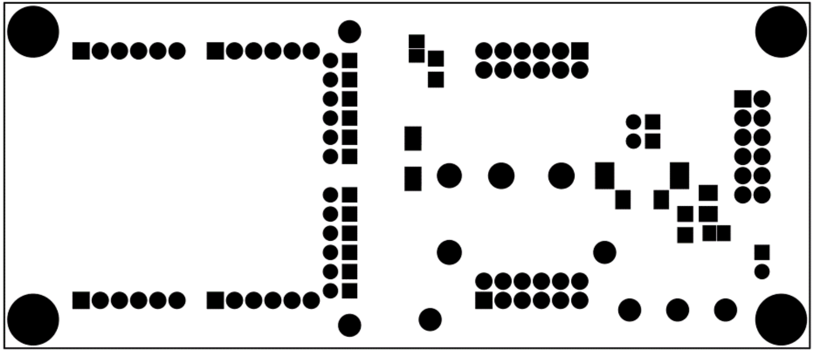
Top Silk



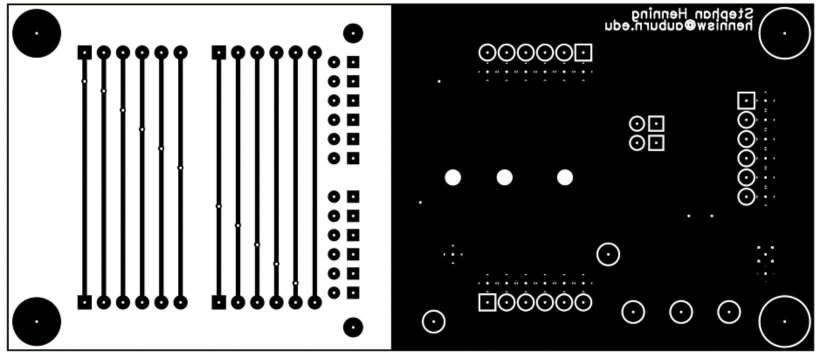
Top Copper



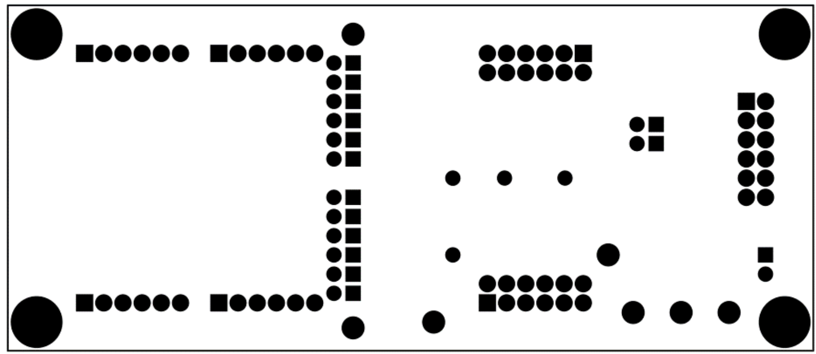
Top Soldermask



Bottom Copper

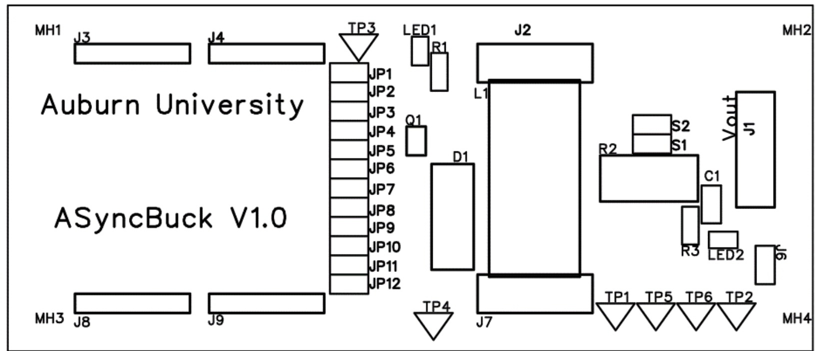


Bottom Soldermask

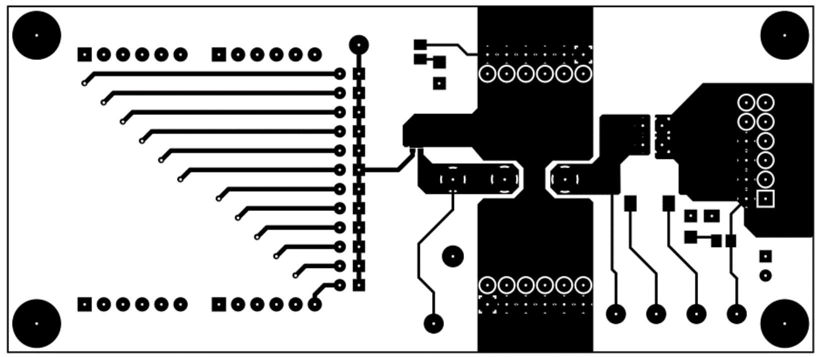


B.3 Asynchronous Buck

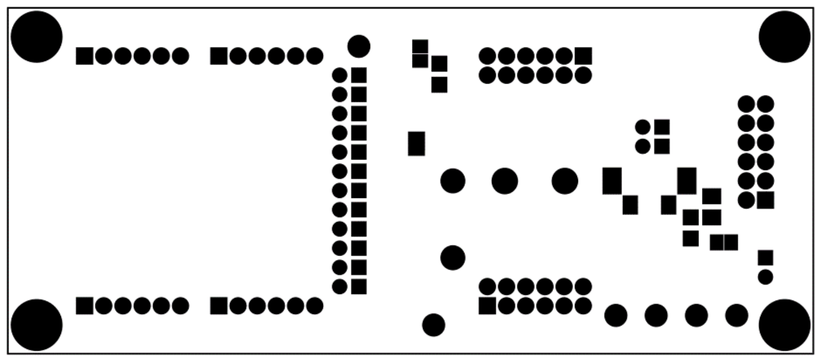
Top Silk



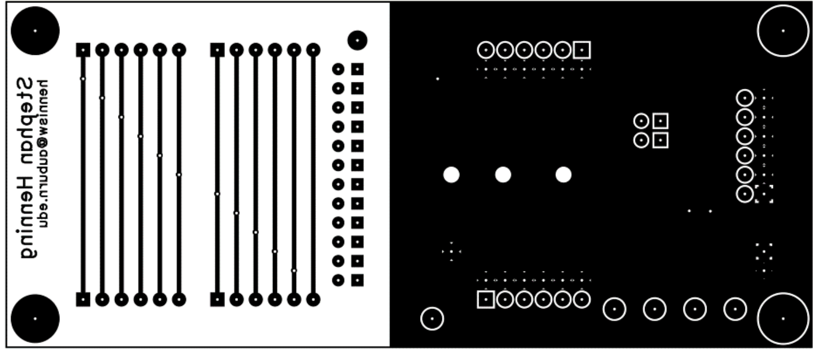
Top Copper



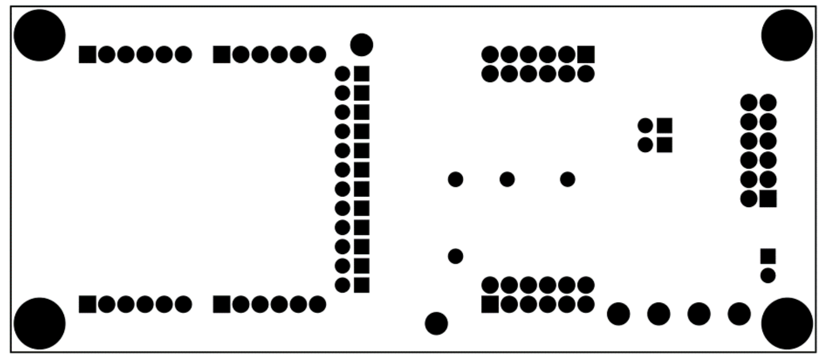
Top Soldermask



Bottom Copper

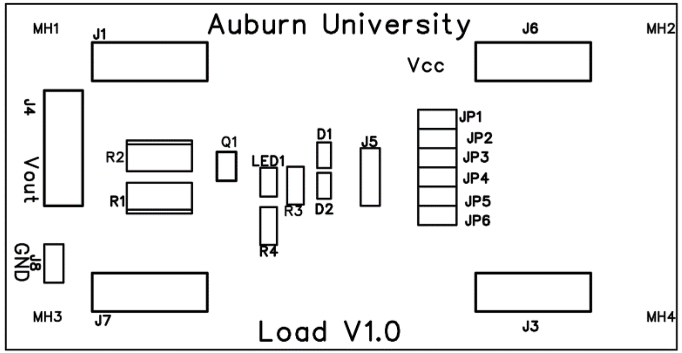


Bottom Soldermask

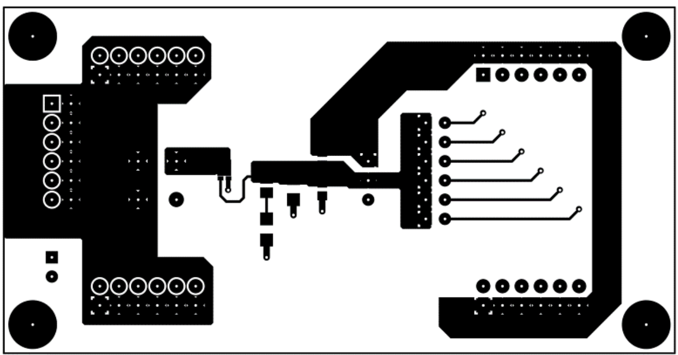


B.4 Load

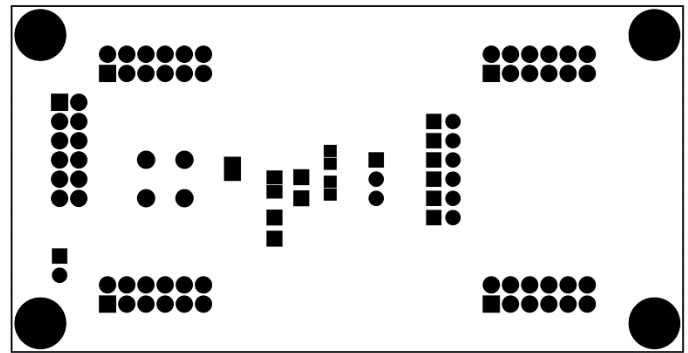
Top Silk



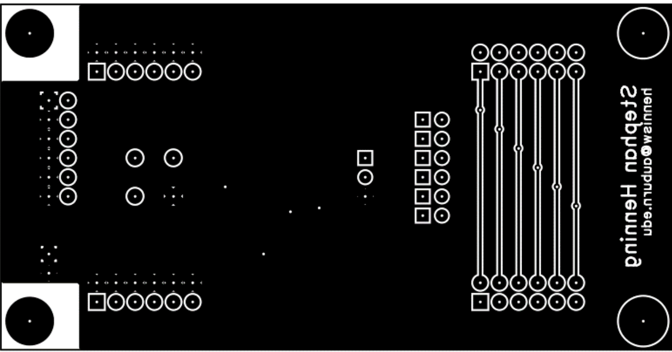
Top Copper



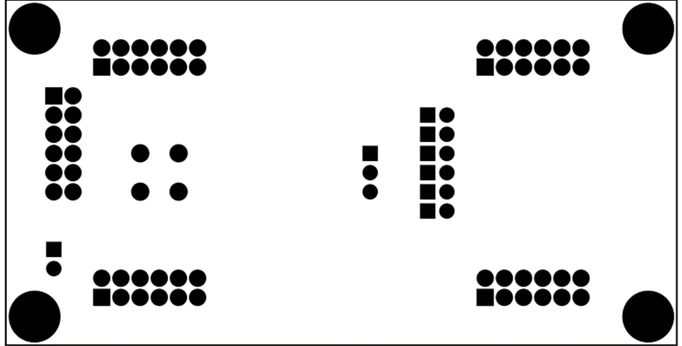
Top Soldermask



Bottom Copper

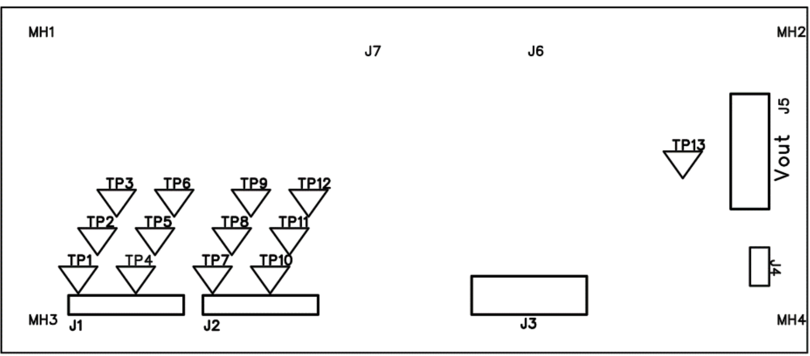


Bottom Soldermask

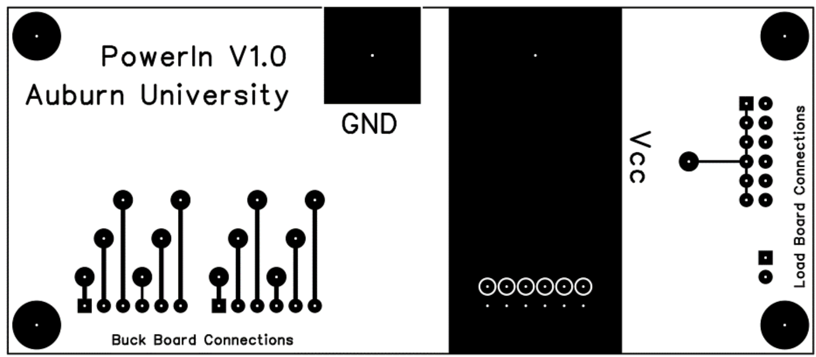


B.5 Power

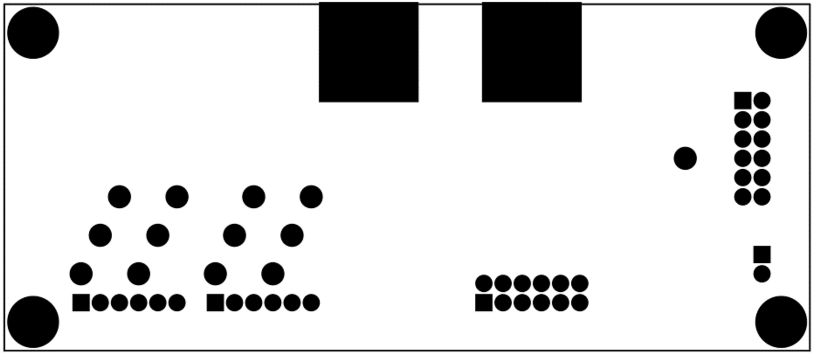
Top Silk



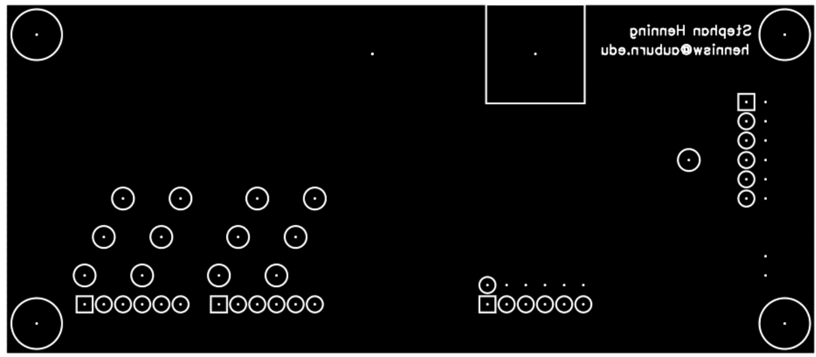
Top Copper



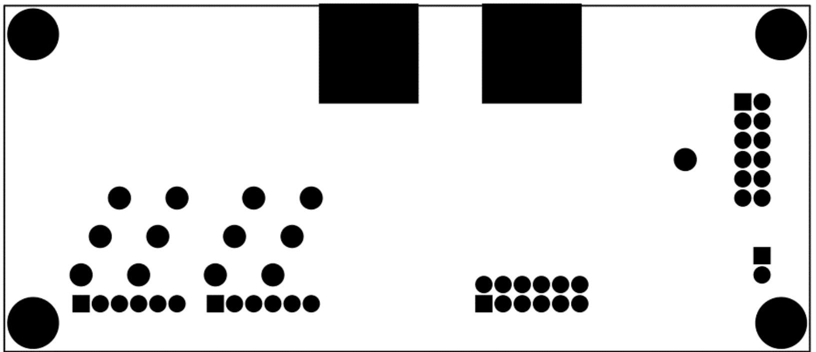
Top Soldermask



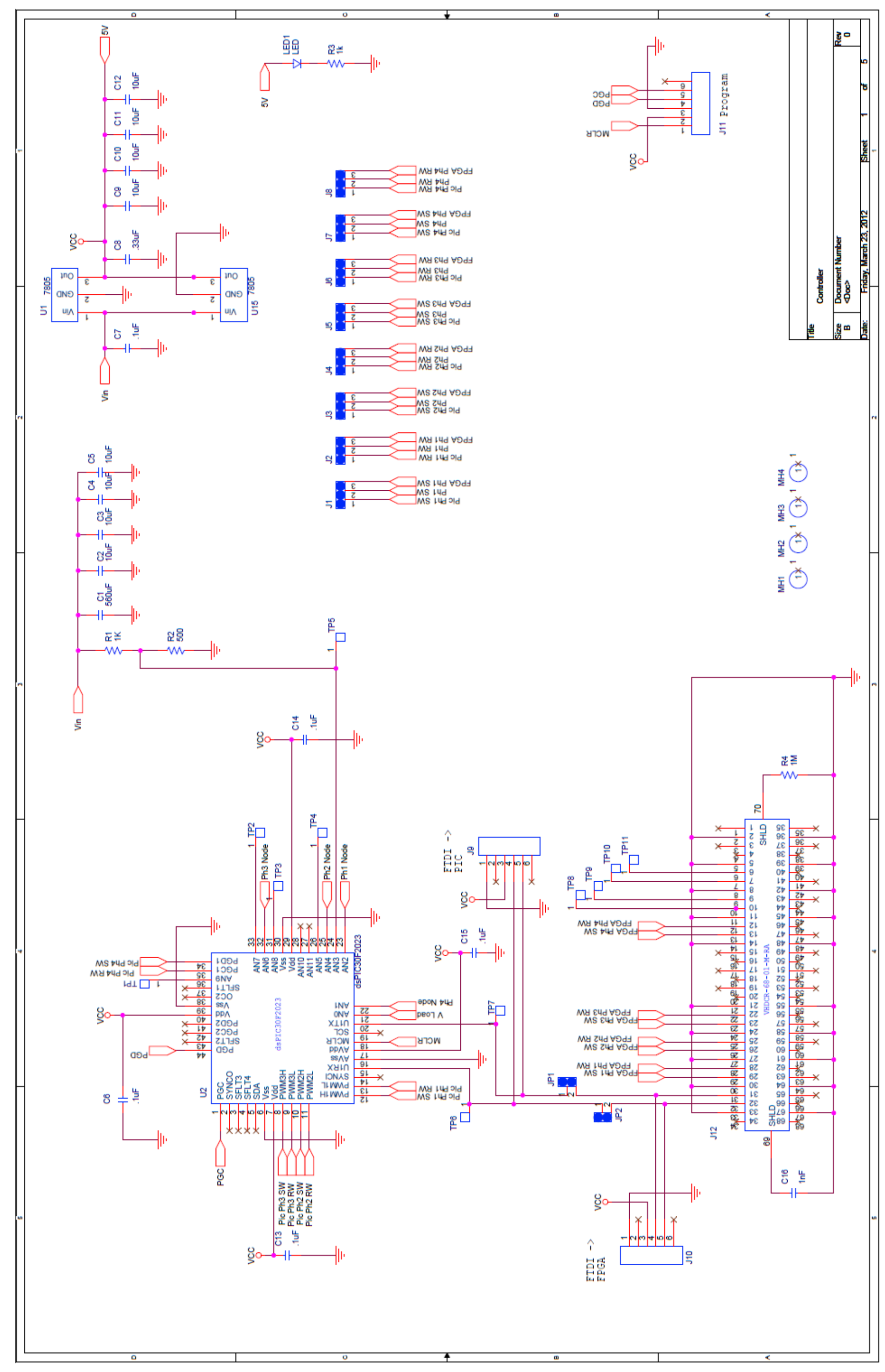
Bottom Copper

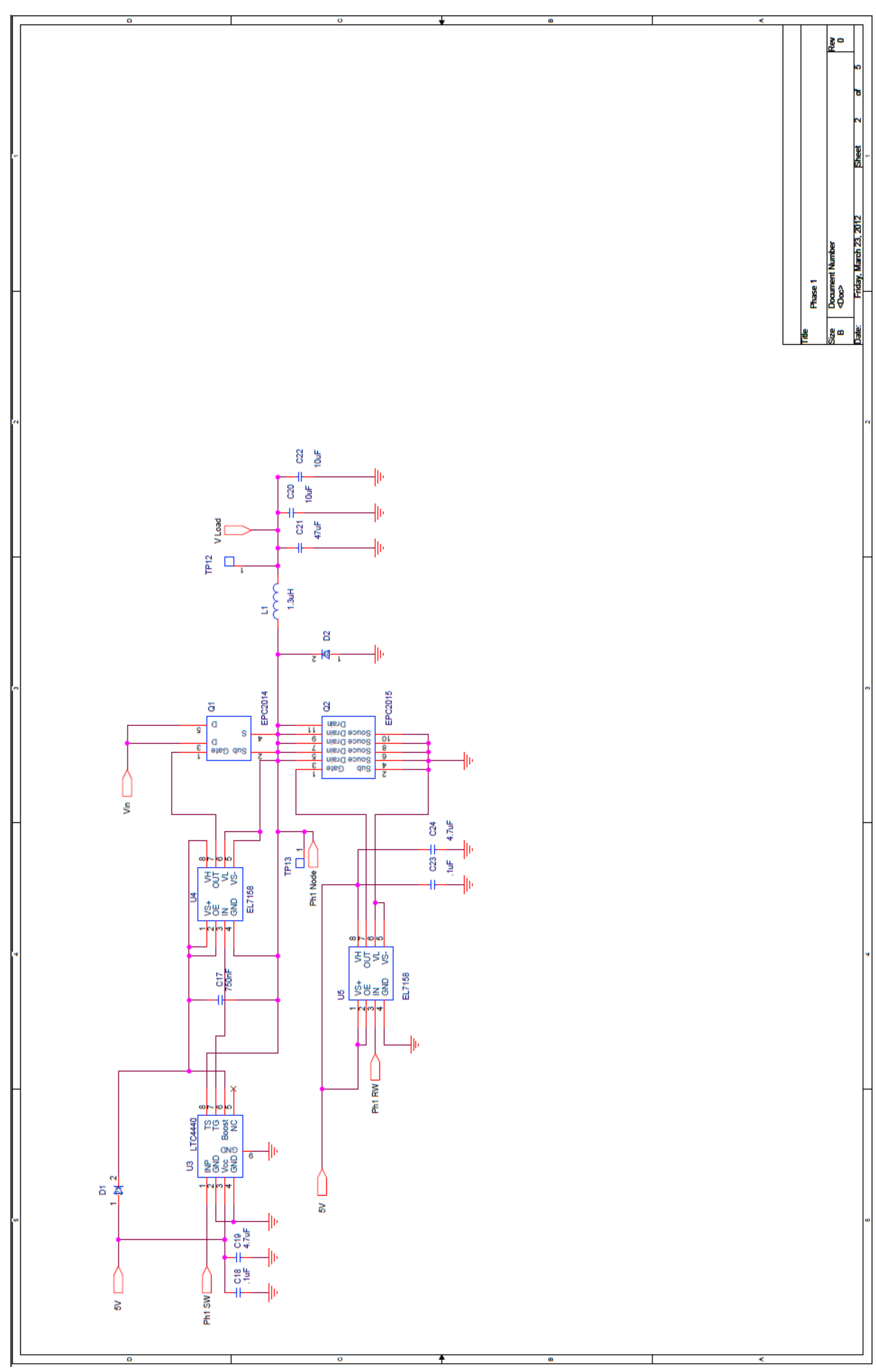


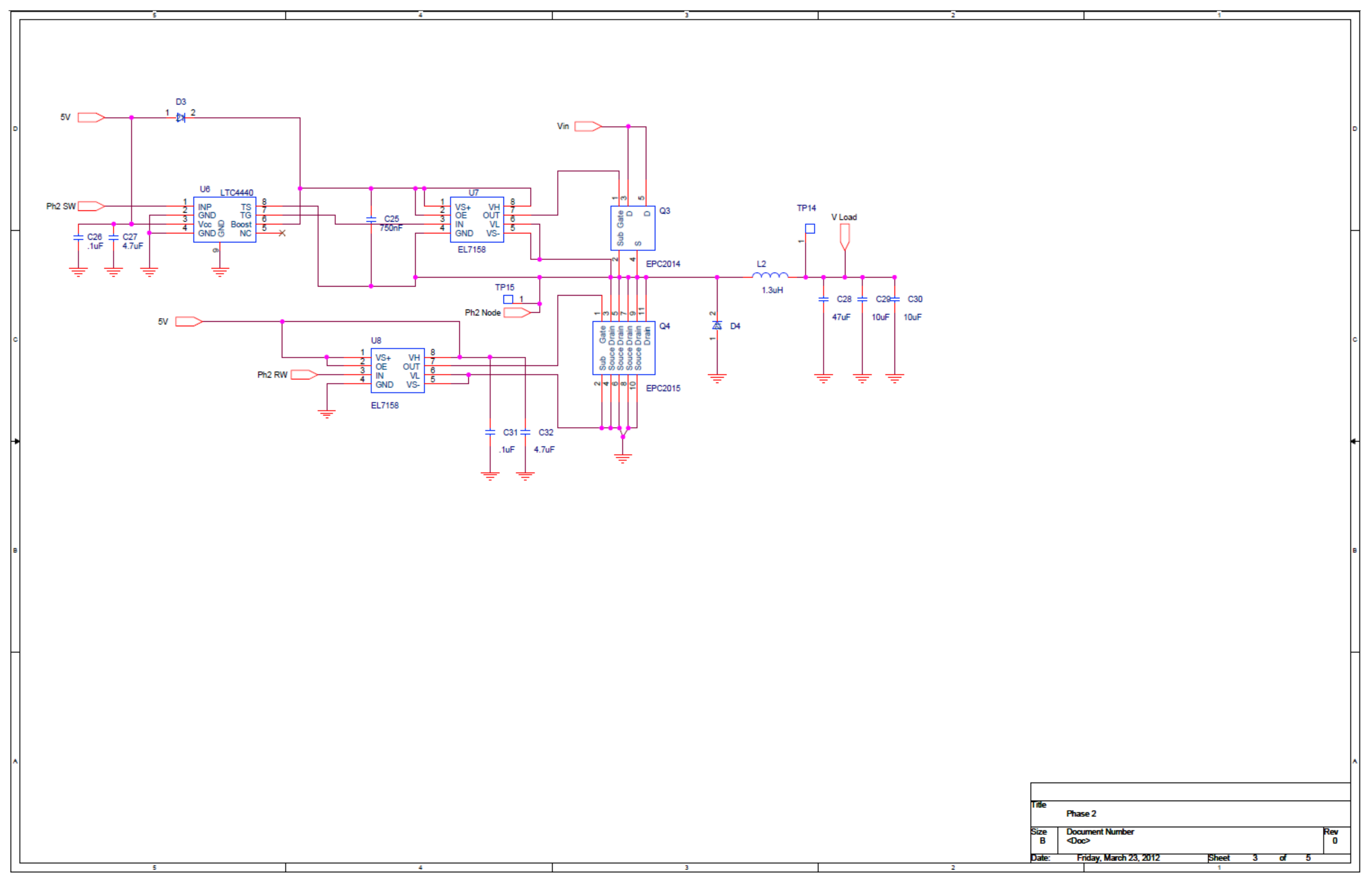
Bottom Soldermask



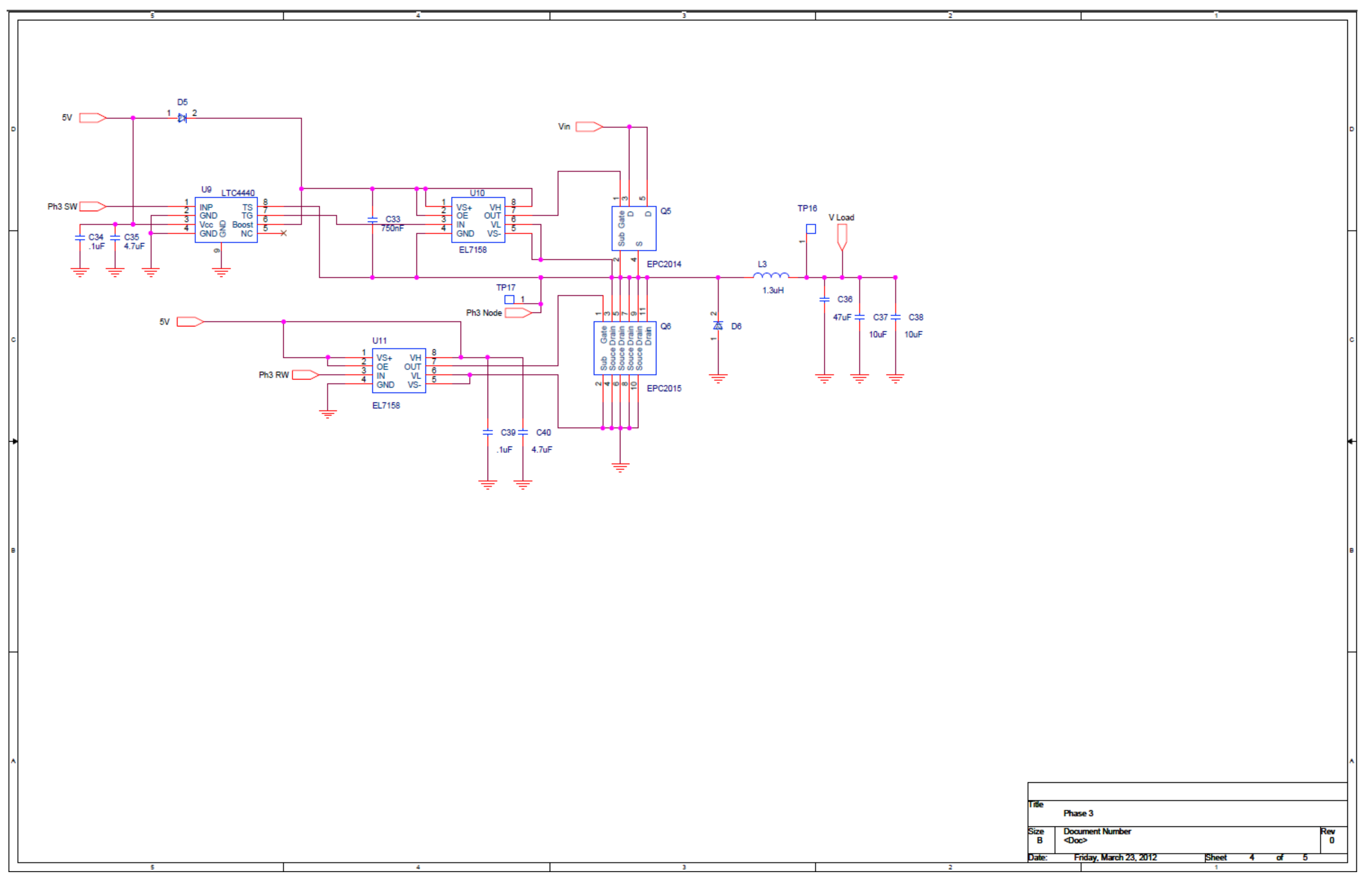
Appendix C: POL V2 Schematics



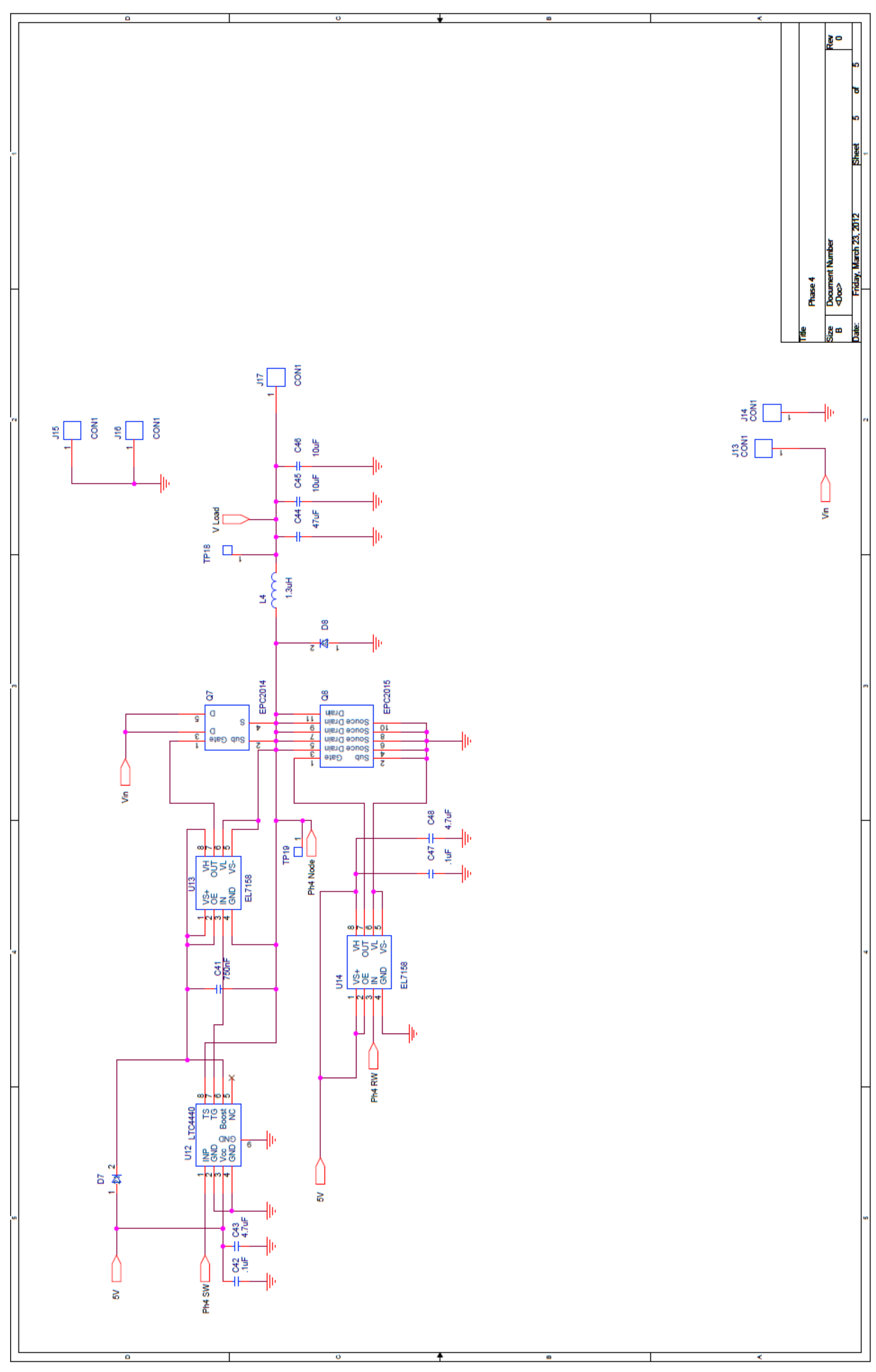




5V
D3
Ph2 SW
U6
LTC4440
INP
GND
Vcc
GND
TS
TG
Boost
NC
C26
.1uF
C27
4.7uF
C25
750nF
U7
VS+
OE
IN
GND
VH
OUT
VL
VS-
EL7158
Vin
Q3
EPC2014
Q4
EPC2015
TP15
Ph2 Node
5V
U8
VS+
OE
IN
GND
VH
OUT
VL
VS-
EL7158
Ph2 RW
C31
.1uF
C32
4.7uF
D4
L2
1.3uH
TP14
V Load
C28
47uF
C29
10uF
C30
10uF
Title
Phase 2
Size
B
Document Number
<Doc>
Rev
0
Date: Friday, March 23, 2012
Sheet 3 of 5

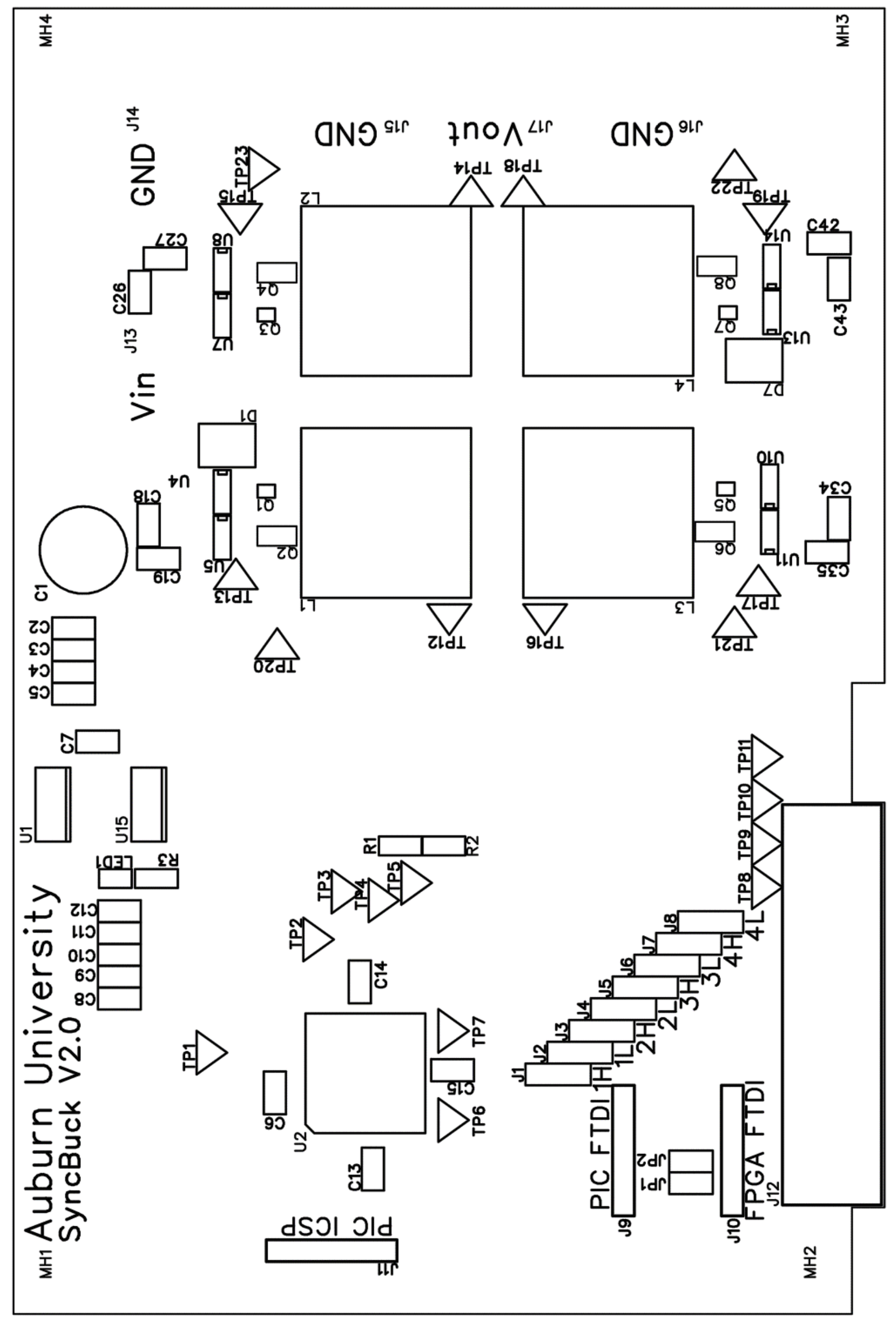


5V
D5
Ph3 SW
U9
LTC4440
INP
GND
Vcc
GND
TS
TG
Boost
NC
C34
.1uF
C35
4.7uF
C33
750nF
U10
VS+
OE
IN
GND
VH
OUT
VL
VS-
EL7158
Vin
Q5
EPC2014
Sub
Gate
D
S
TP17
Ph3 Node
5V
U11
Ph3 RW
EL7158
C39
.1uF
C40
4.7uF
Q6
EPC2015
Souce Drain
Drain
D6
L3
1.3uH
TP16
V Load
C36
47uF
C37
10uF
C38
10uF
Title
Phase 3
Size
B
Document Number
<Doc>
Rev
0
Date: Friday, March 23, 2012
Sheet 4 of 5

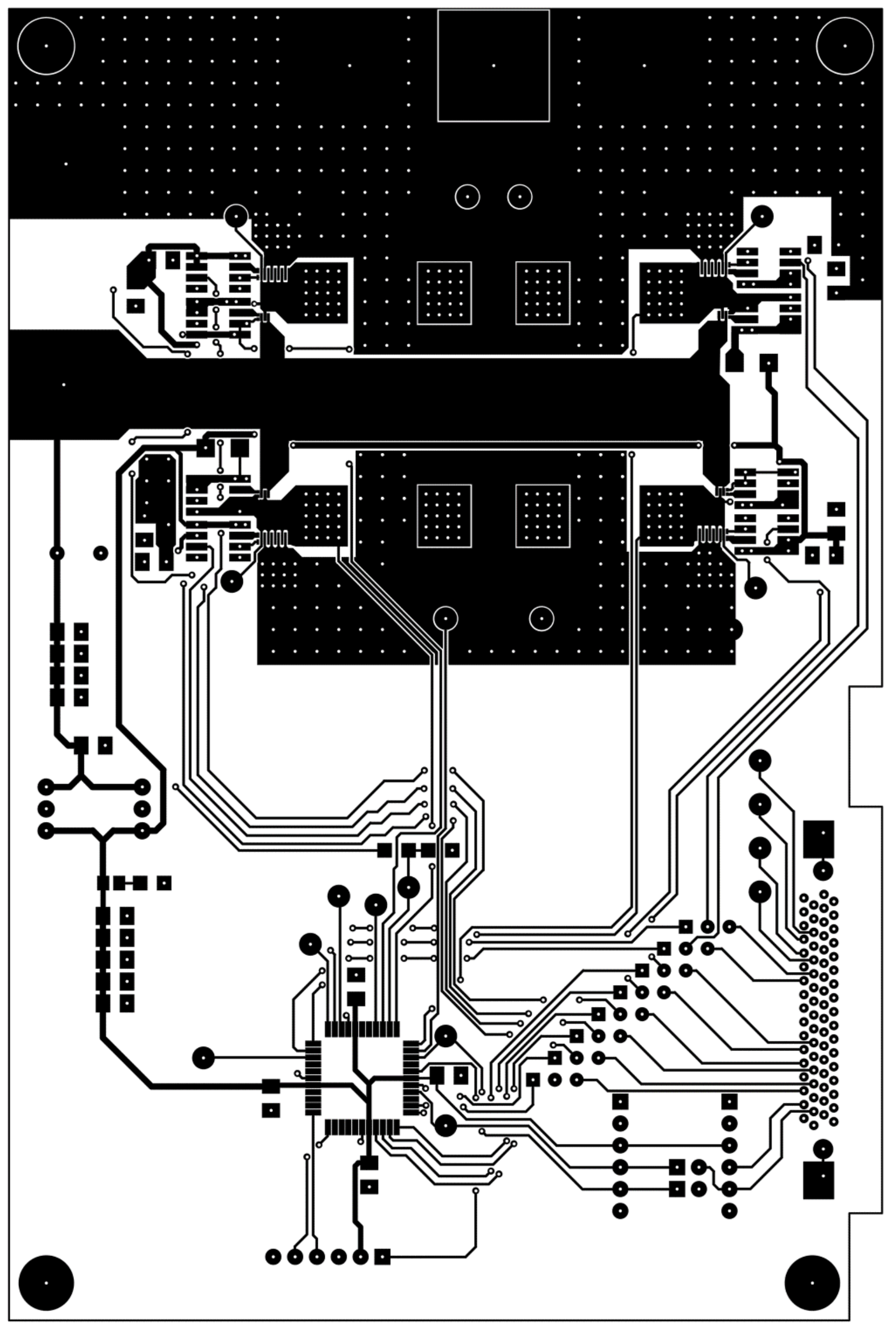

Title
Phase 4
Size
B
Document Number
<Doc>
Rev
0
Date: Friday, March 23, 2012
Sheet 5 of 5

Appendix D: POL V2 Layout

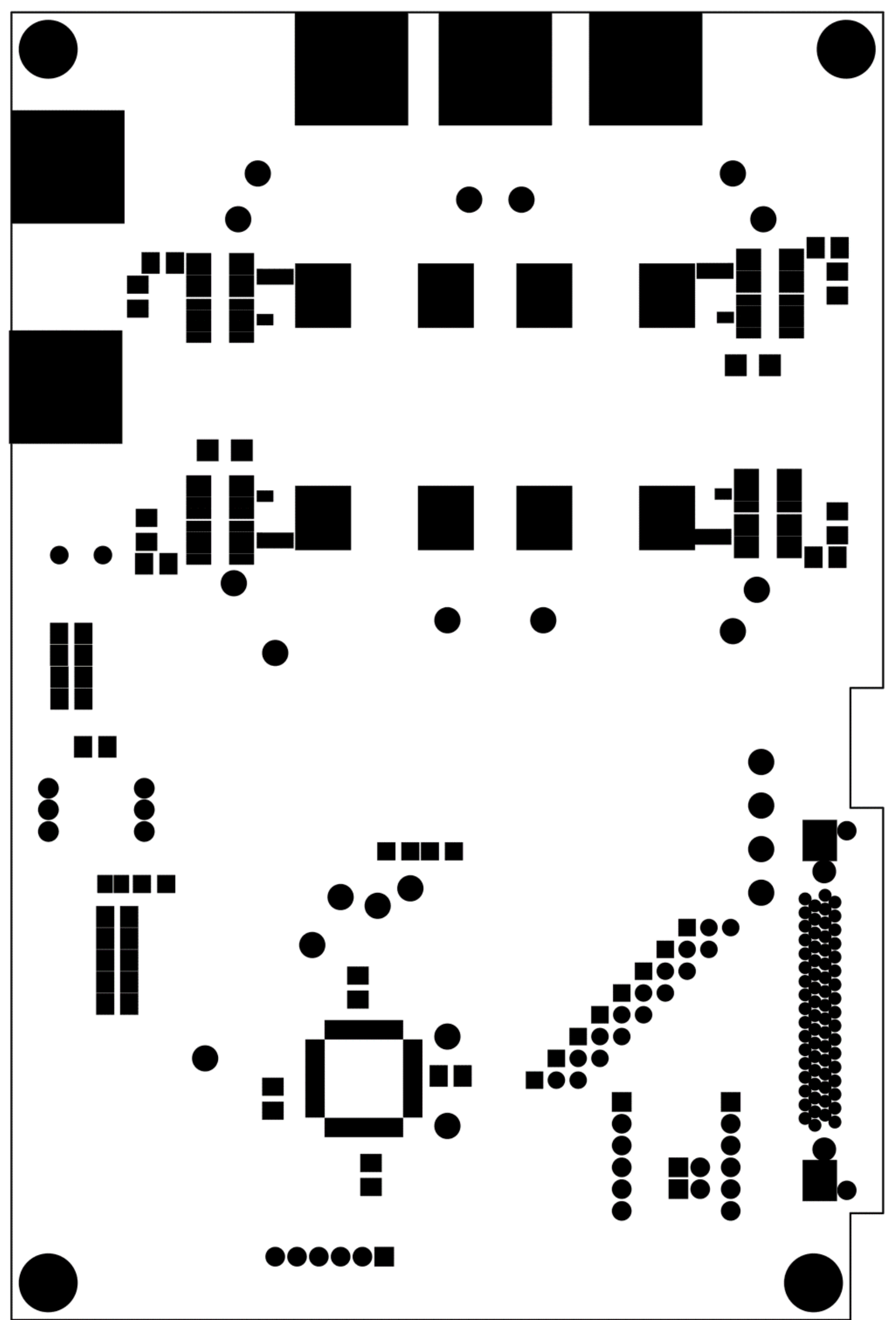
Top Silk



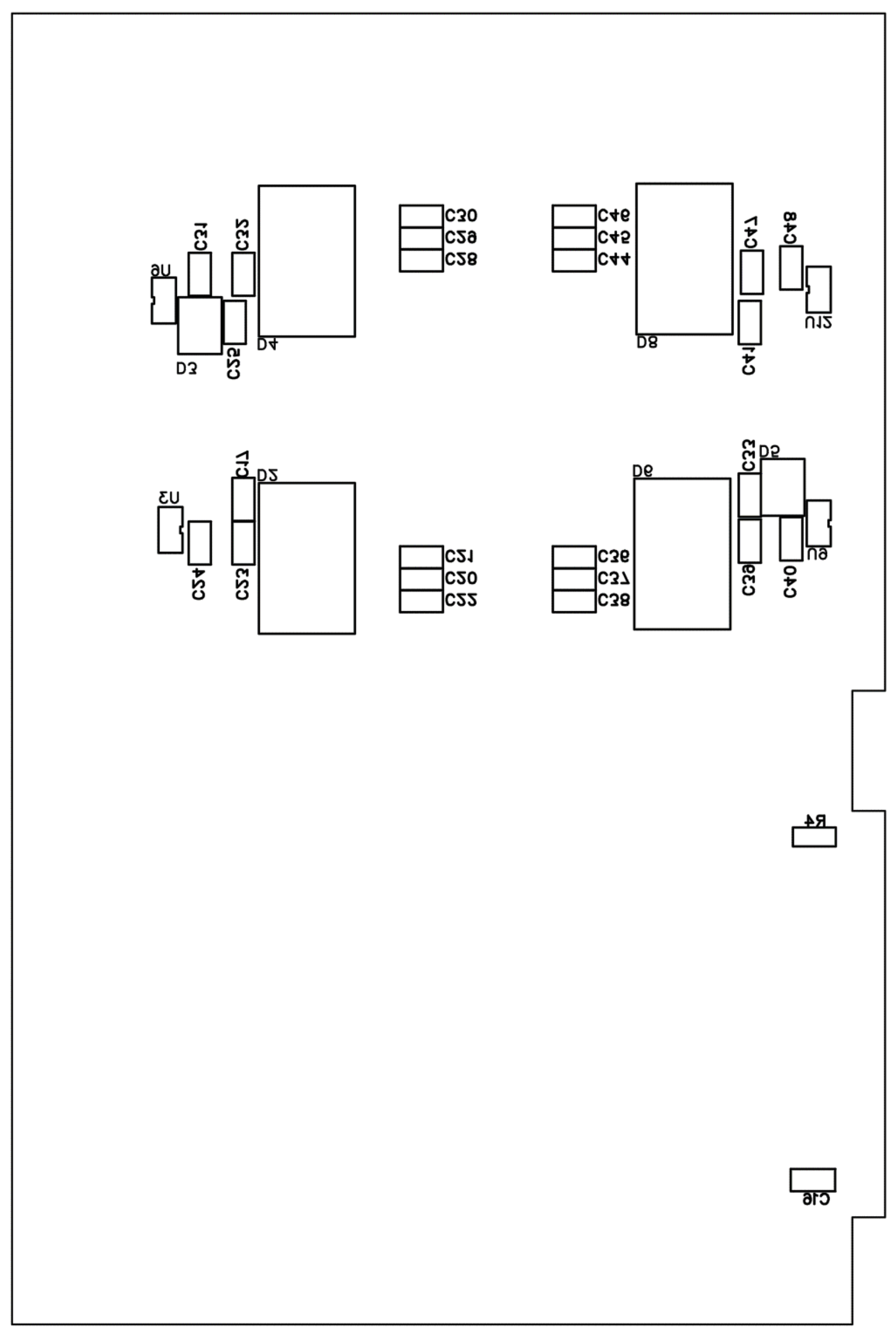
Top Copper



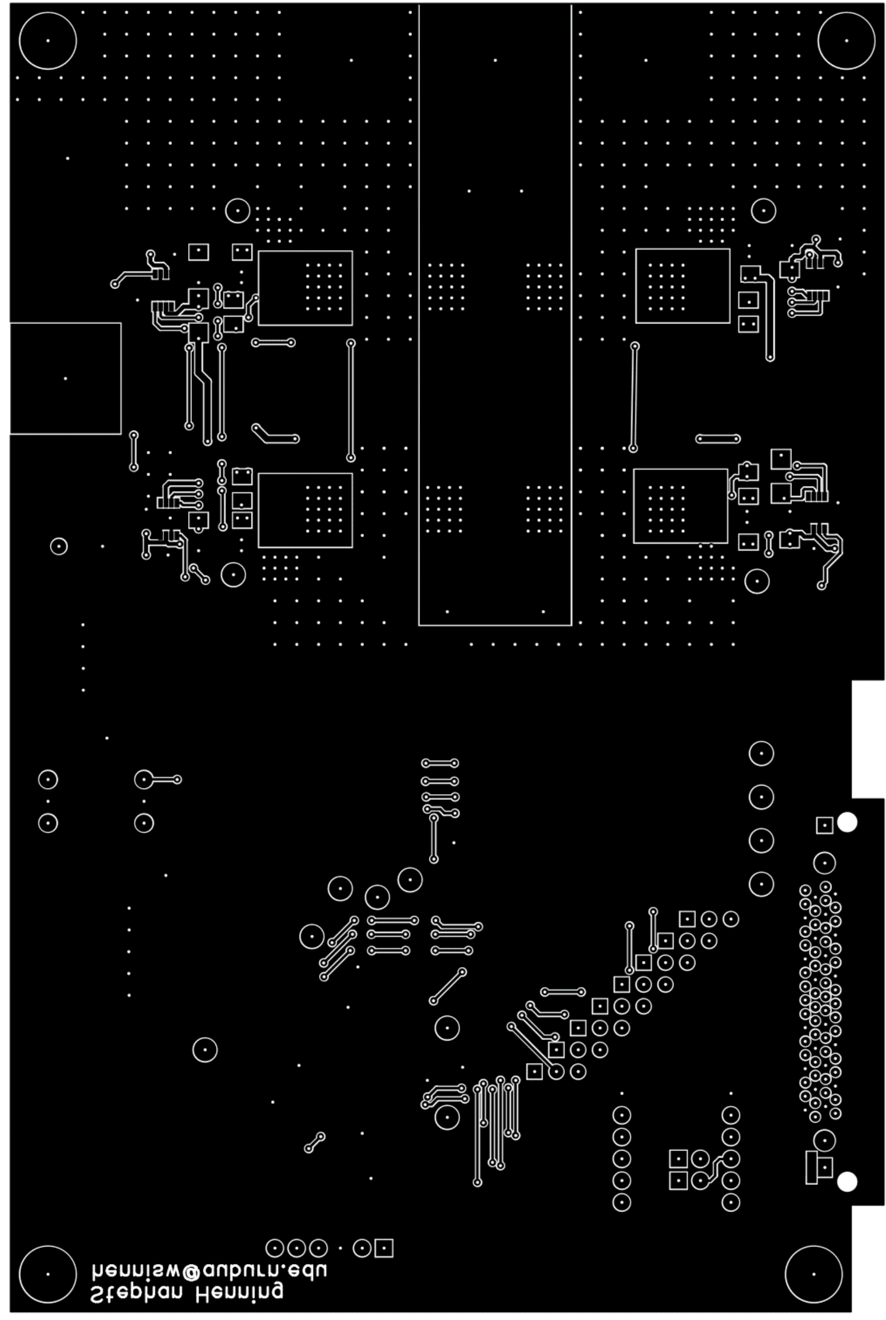
Top Soldermask



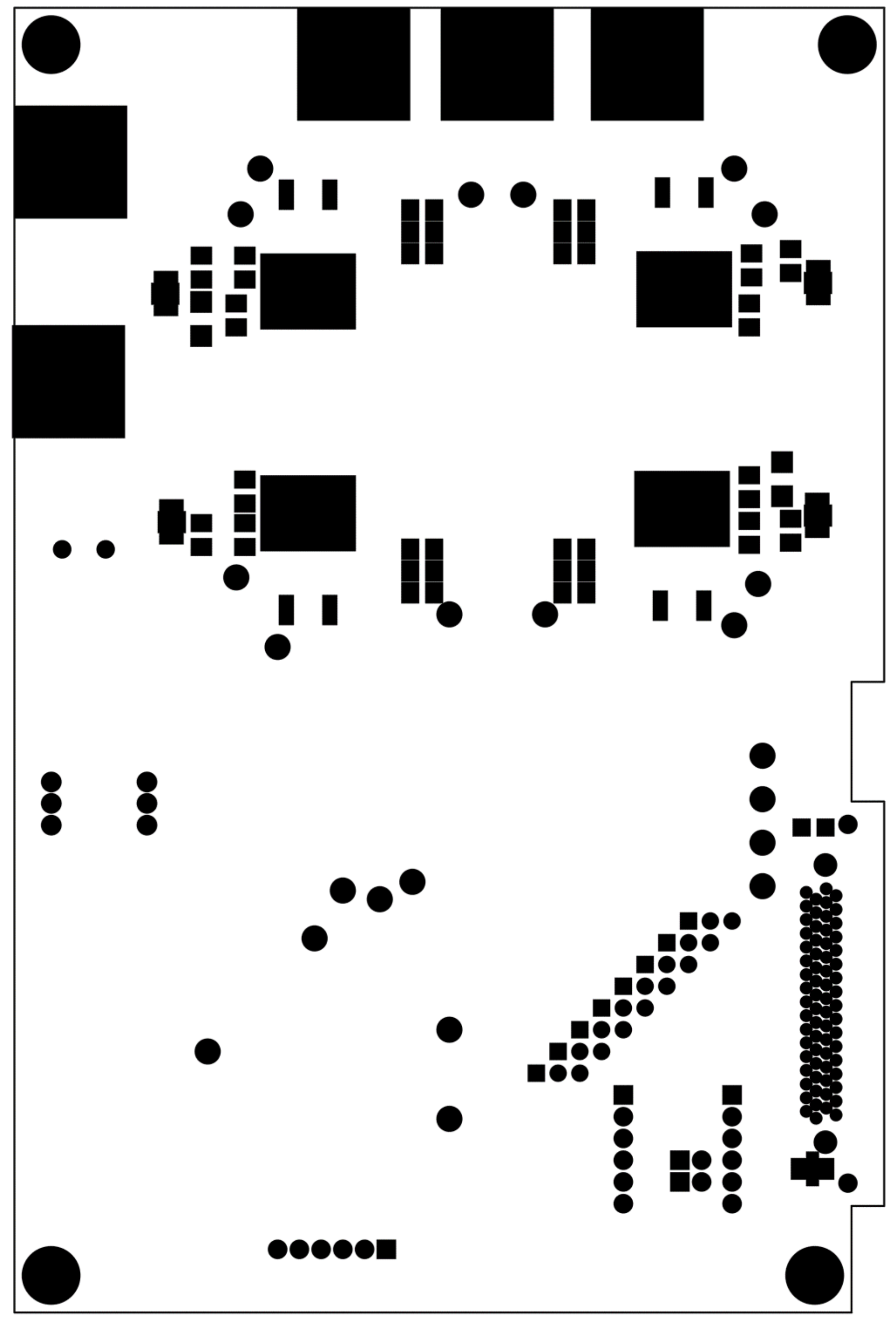
Bottom Silk



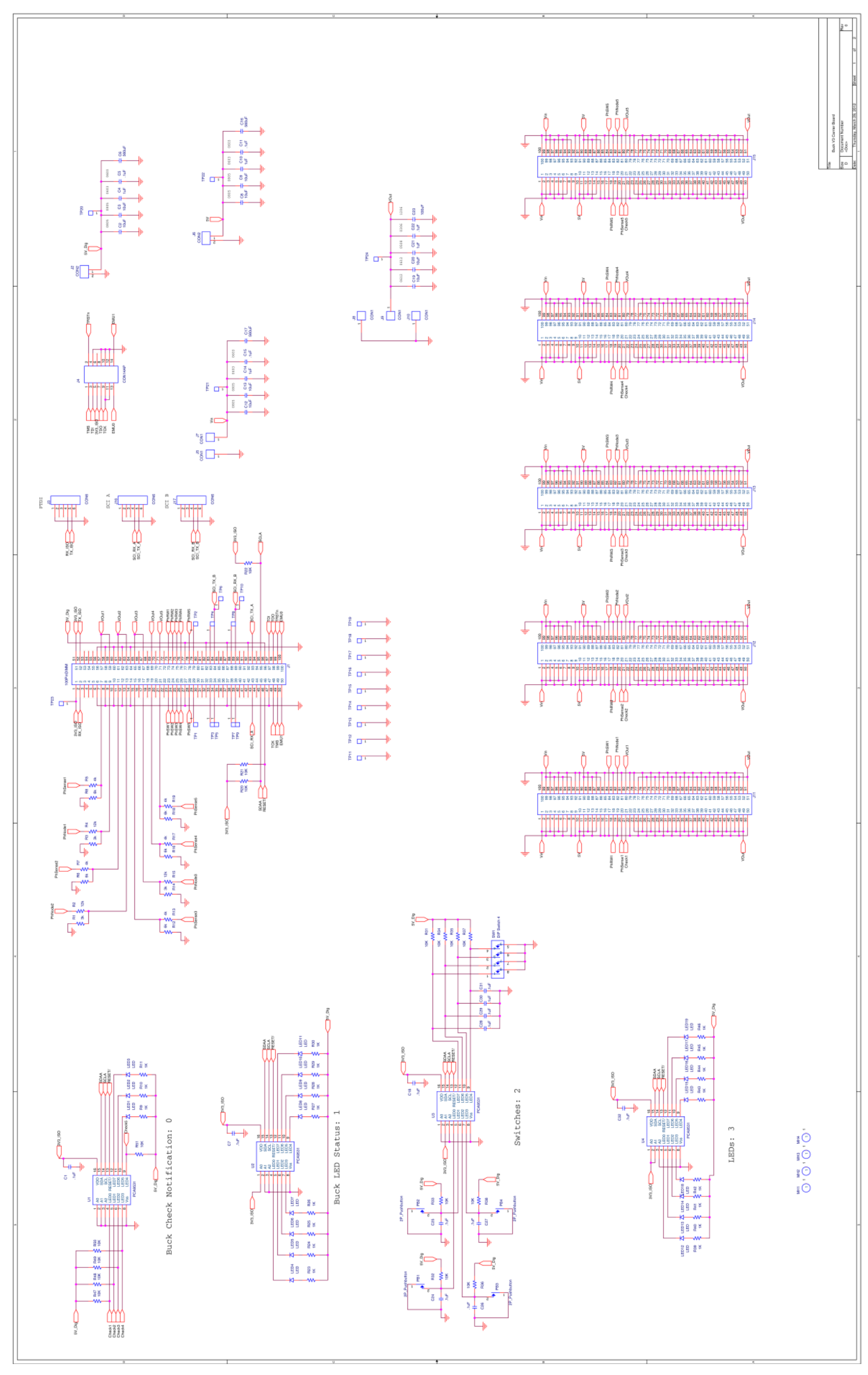
Bottom Copper

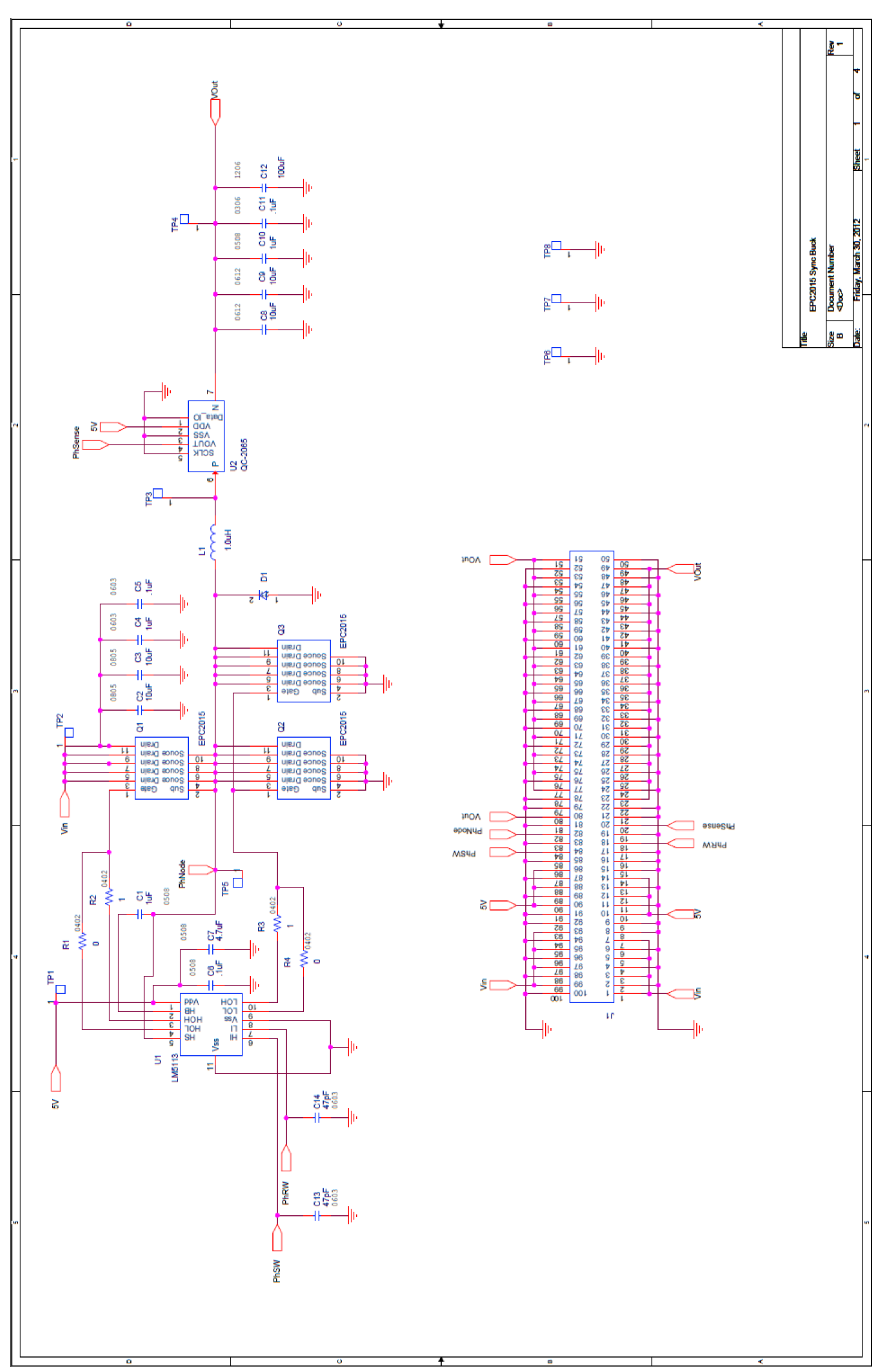


Bottom Soldermask



Appendix E: POL V3 Schematics



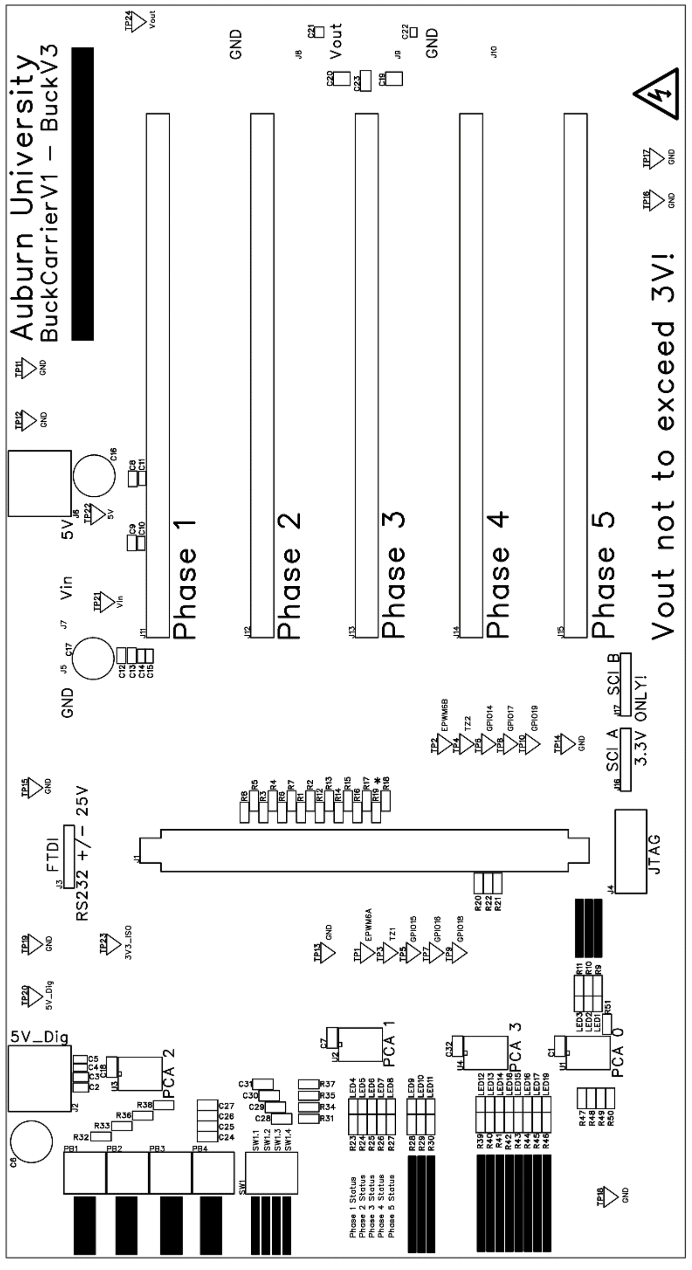


Title
EPC2015 Sync Buck
Size
B
Document Number
<Doc>
Rev
1
Date: Friday, March 30, 2012
Sheet 1 of 4
VOut
PhSense
5V
U2
QC-2065
L1
1.0uH
D1
Q1
Q2
Q3
EPC2015
U1
LM5113
PhNode
PhRW
PhSW
Vin
J1

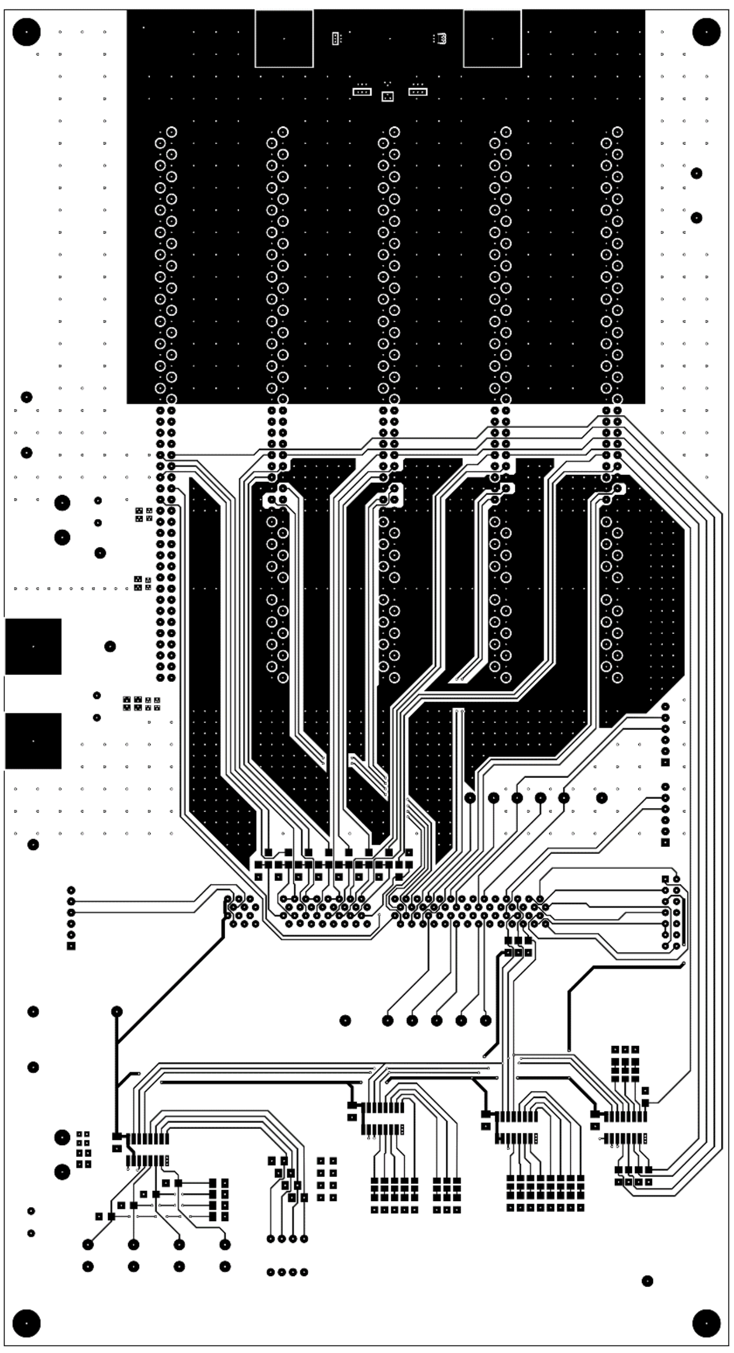
Appendix F: POL V3 Layouts

F.1 Carrier Board

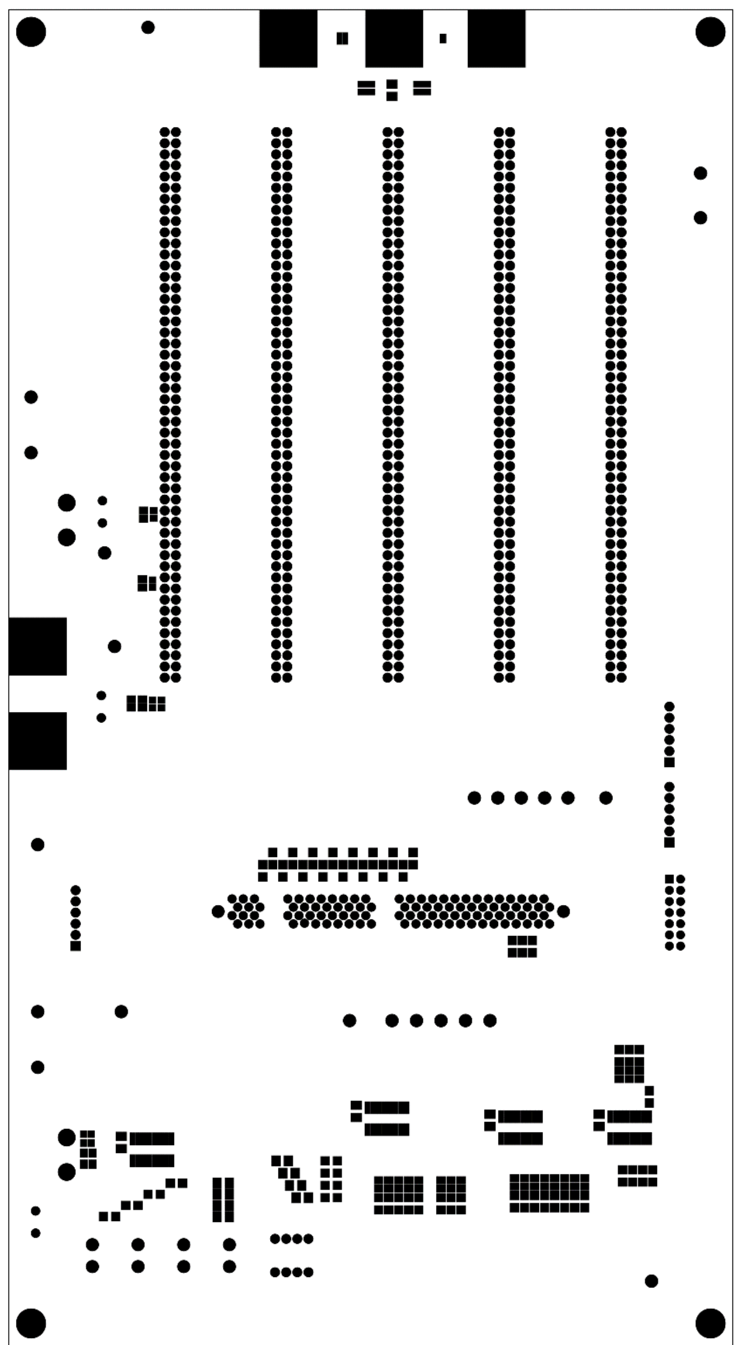
Top Silk



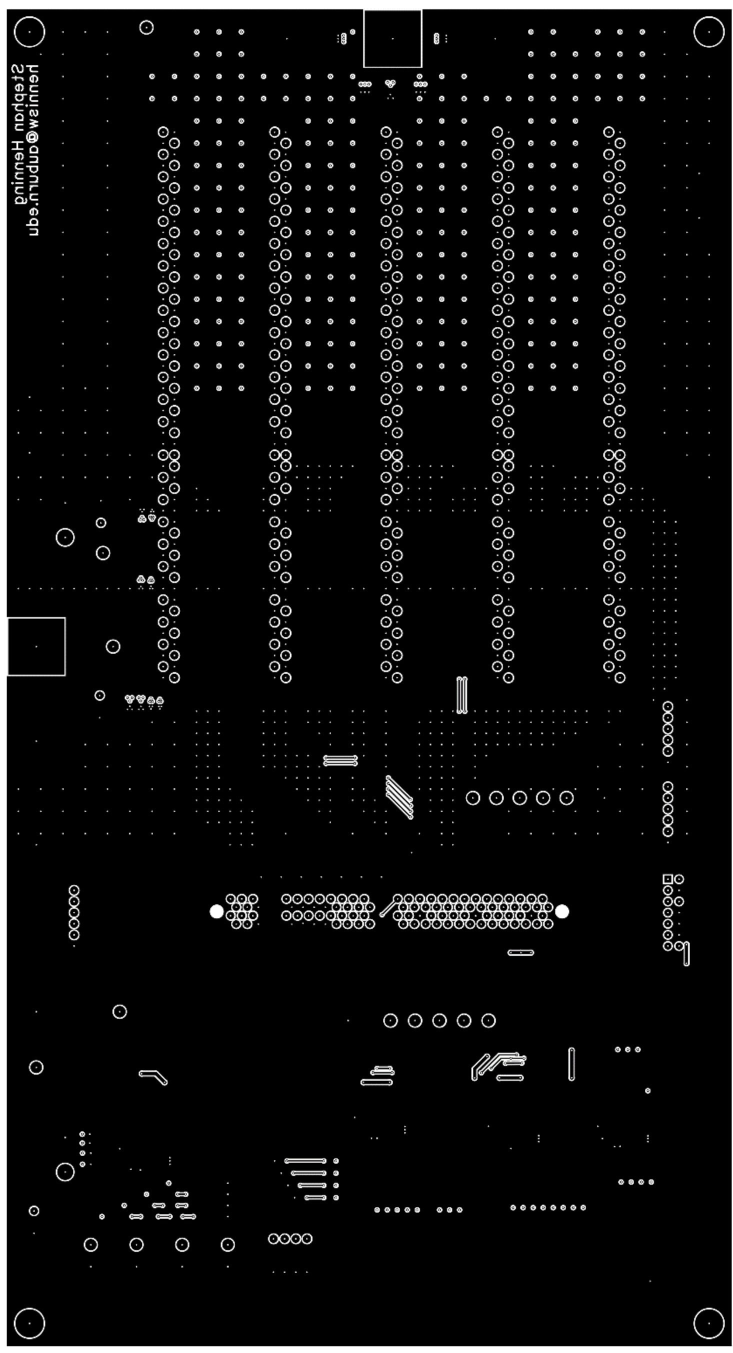
Top Copper



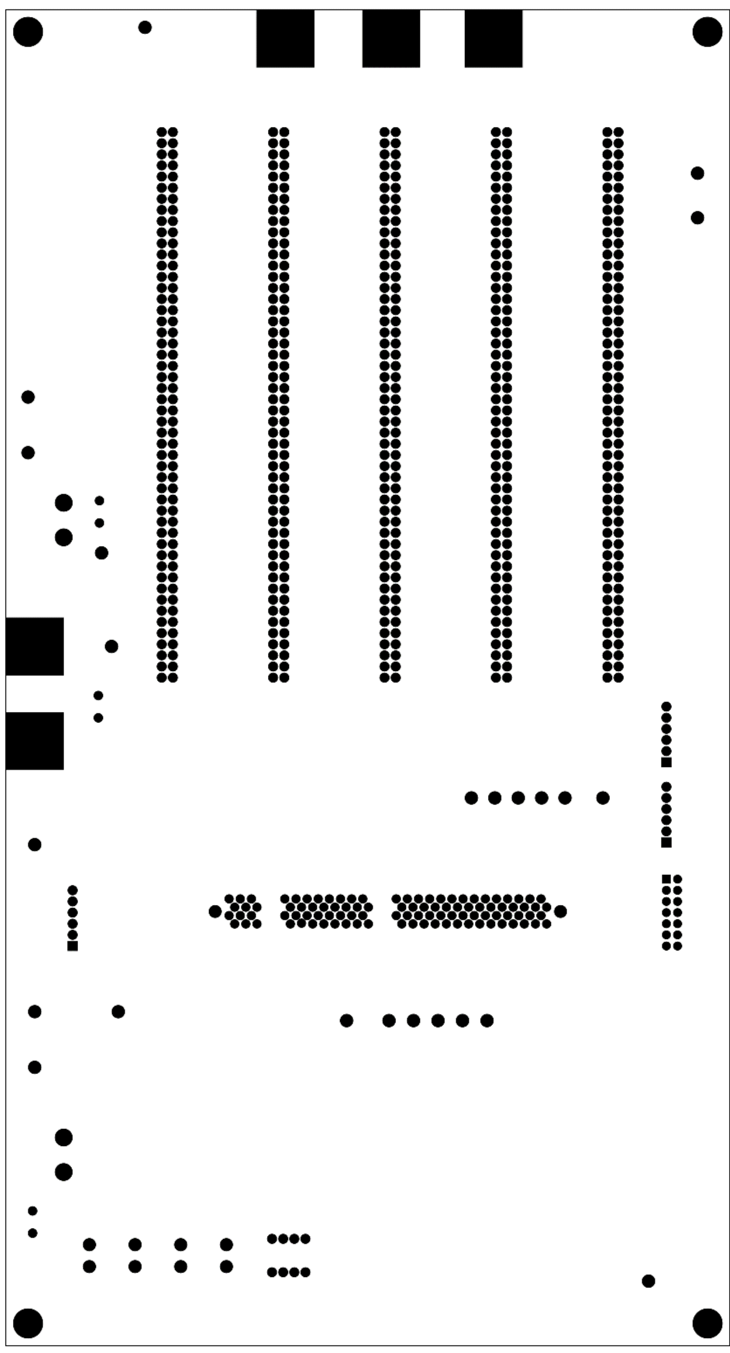
Top Soldermask



Bottom Copper

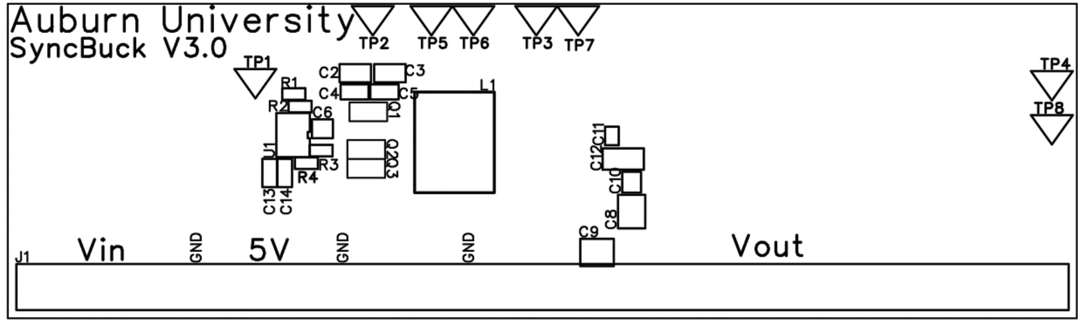


Bottom Soldermask

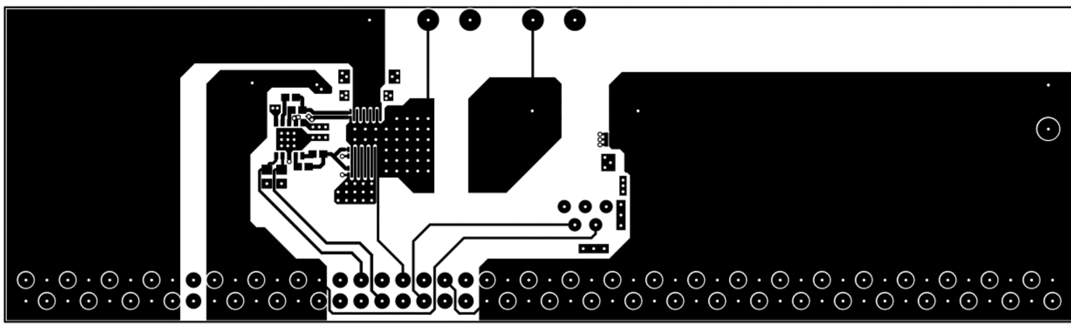


F.2 Buck Daughter Card

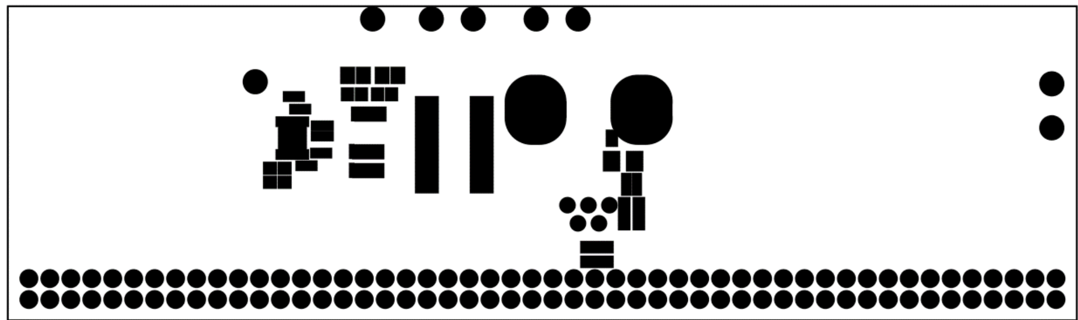
Top Silk



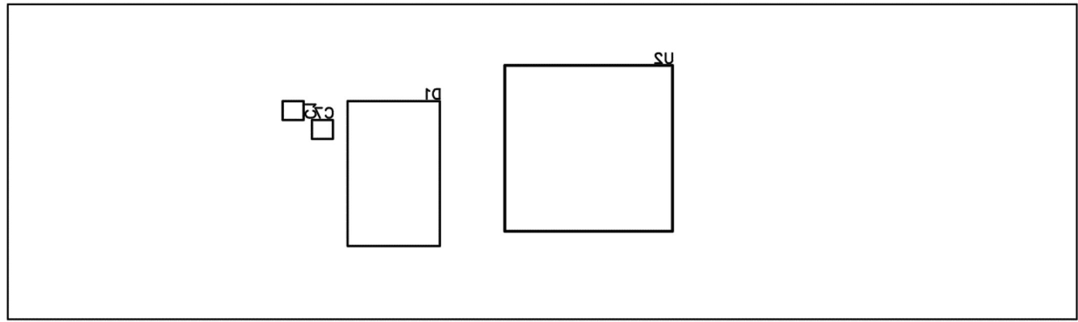
Top Copper



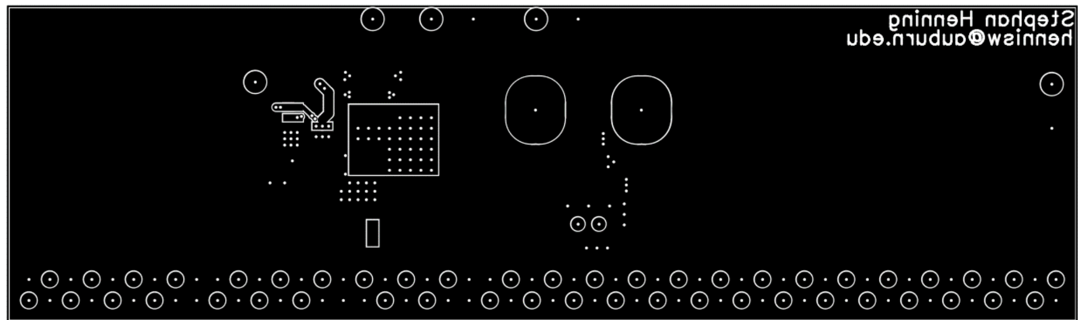
Top Soldermask



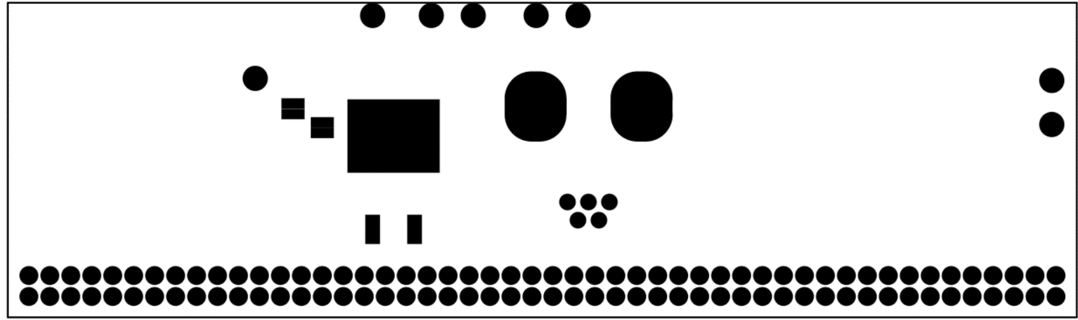
Bottom Silk



Bottom Copper



Bottom Soldermask



Appendix G: Software, Scripts, and Code

G.1 Buck V2 Matlab Plotting Code

```
load('C:\Users\Stephan\Dropbox\GRA\Thesis\Buck v2\BuckV2_Data.mat');


close all; clc;

option.directory = 'C:\Users\Stephan\Dropbox\GRA\Thesis\Buck v2\plots'; % Set
directory name

% Check if directory exists. If not, create it
if exist(option.directory)
    option.oldDirectory = cd(option.directory);
else
    mkdir(option.directory);
    option.oldDirectory = cd(option.directory);
end

%% Single Phase Operating

% Parse Data
numCurrents = 5;
freqVec = BuckV2Data(3:9,13);
startIndex = 0;
dataSpacing = 2;

% Parsing board 5 phase 1
p1DataMatrix = zeros(numCurrents,2,length(freqVec)); % Preallocate current,
efficiency, freq

for currentIndex= 1:numCurrents
    for freqIndex = 1:length(freqVec);
        p1DataMatrix(currentIndex,1,freqIndex) = ...
            BuckV2Data((currentIndex-1)*length(freqVec)+...
            dataSpacing*currentIndex+freqIndex, 11); % parse current
        p1DataMatrix(currentIndex,2,freqIndex) = ...
            BuckV2Data((currentIndex-1)*length(freqVec)+...
            dataSpacing*currentIndex+freqIndex, 2); % parse efficiency
    end
end

% Parsing board 5 phase 4
dataOffset = 46;
p4DataMatrix = zeros(numCurrents,2,length(freqVec)); % Preallocate current,
efficiency, freq

for currentIndex= 1:numCurrents
    for freqIndex = 1:length(freqVec);
        p4DataMatrix(currentIndex,1,freqIndex) = ...
            BuckV2Data((currentIndex-1)*length(freqVec)+...
```

```
            dataSpacing*currentIndex+freqIndex+dataOffset, 11); % parse
current
        p4DataMatrix(currentIndex,2,freqIndex) = ...
            BuckV2Data((currentIndex-1)*length(freqVec)+...
            dataSpacing*currentIndex+freqIndex+dataOffset, 2); % parse
efficiency
    end
end


% Calculate average of phase 1 and phase 4
avgDataMatrix = zeros(numCurrents,2,length(freqVec));

for freqIndex = 1:length(freqVec);
    avgDataMatrix(:,1, freqIndex) = mean([p1DataMatrix(:,1, freqIndex)
p4DataMatrix(:,1, freqIndex)],2); % Average Currents
    avgDataMatrix(:,2, freqIndex) = mean([p1DataMatrix(:,2, freqIndex)
p4DataMatrix(:,2, freqIndex)],2); % Average Efficiency
end

%% Two Phase Operation

% Parsing board 5 phase 1&4
numCurrents = 5;
twoPhaseFreqVec = BuckV2Data(95:102,13);
dataSpacing = 2;
dataOffset = 92;
p1_4DataMatrix = zeros(numCurrents,2,length(twoPhaseFreqVec)); % Preallocate
current, efficiency, freq

for currentIndex= 1:numCurrents
    for freqIndex = 1:length(twoPhaseFreqVec);
        p1_4DataMatrix(currentIndex,1,freqIndex) = ...
            BuckV2Data((currentIndex-1)*length(twoPhaseFreqVec)+...
            dataSpacing*currentIndex+freqIndex+dataOffset, 11); % parse
current
        p1_4DataMatrix(currentIndex,2,freqIndex) = ...
            BuckV2Data((currentIndex-1)*length(twoPhaseFreqVec)+...
            dataSpacing*currentIndex+freqIndex+dataOffset, 2); % parse
efficiency
    end
end






%% Plotting

hndls = setup_figures(4, [1200 800]);

% Plotting Board 5 Phase 1: 2.5V in, 1V
figure(hndls(1))
hold on
```

```
plot(p1DataMatrix(:,1,1), p1DataMatrix(:,2,1)*100,'b','LineWidth',2) %200Hz
plot(p1DataMatrix(:,1,2), p1DataMatrix(:,2,2)*100,'r','LineWidth',2) %225Hz
plot(p1DataMatrix(:,1,3), p1DataMatrix(:,2,3)*100,'g','LineWidth',2) %250Hz
plot(p1DataMatrix(:,1,4), p1DataMatrix(:,2,4)*100,'m','LineWidth',2) %275Hz
plot(p1DataMatrix(:,1,5), p1DataMatrix(:,2,5)*100,'c','LineWidth',2) %300Hz
plot(p1DataMatrix(:,1,6), p1DataMatrix(:,2,6)*100,'Color',[.8 0.375
0],'LineWidth',2) %325Hz
plot(p1DataMatrix(:,1,7), p1DataMatrix(:,2,7)*100,'k','LineWidth',2) %350Hz

set(gca, 'fontsize', 22, 'linewidth',1)
axis([1.5, 6.5, 75, 100])
l1=legend('200Hz', '225Hz', '250Hz', '275Hz', '300Hz', '325Hz',
'350Hz','Location', 'North', 'Orientation', 'Horizontal');
title('Board 5 Phase 1, 2.5V In, 1V Ouput')
ylabel('Efficiency (%)')
xlabel('Output Current (A)')
hold off
set(l1,'FontSize',16)
set(hndls(1),'PaperPositionMode', 'auto');

print -r0 -f1 -dpng Board5_Phase1
% saveas(gcf,'Board5_Phase1','jpg')

% Plotting Board 5 Phase 4: 2.5V in, 1V
figure(hndls(2))
hold on
plot(p4DataMatrix(:,1,1), p4DataMatrix(:,2,1)*100,'b','LineWidth',2) %200Hz
plot(p4DataMatrix(:,1,2), p4DataMatrix(:,2,2)*100,'r','LineWidth',2) %225Hz
plot(p4DataMatrix(:,1,3), p4DataMatrix(:,2,3)*100,'g','LineWidth',2) %250Hz
plot(p4DataMatrix(:,1,4), p4DataMatrix(:,2,4)*100,'m','LineWidth',2) %275Hz
plot(p4DataMatrix(:,1,5), p4DataMatrix(:,2,5)*100,'c','LineWidth',2) %300Hz
plot(p4DataMatrix(:,1,6), p4DataMatrix(:,2,6)*100,'Color',[.8 0.375
0],'LineWidth',2) %325Hz
plot(p4DataMatrix(:,1,7), p4DataMatrix(:,2,7)*100,'k','LineWidth',2) %350Hz

set(gca, 'fontsize', 22, 'linewidth',1)
axis([1.5, 6.5, 75, 100])
l2=legend('200Hz', '225Hz', '250Hz', '275Hz', '300Hz', '325Hz',
'350Hz','Location', 'North', 'Orientation', 'Horizontal');
title('Board 5 Phase 4, 2.5V In, 1V Ouput')
ylabel('Efficiency (%)')
xlabel('Output Current (A)')
hold off
set(l2,'FontSize',16)
set(hndls(2),'PaperPositionMode', 'auto');

print -r0 -f2 -dpng Board5_Phase4
% saveas(gcf,'Board5_Phase4','jpg')


% Plotting Board 5 Average of Phase 1 and 4: 2.5V in, 1V
figure(hndls(3))
hold on
plot(avgDataMatrix(:,1,1), avgDataMatrix(:,2,1)*100,'b','LineWidth',2) %200Hz
plot(avgDataMatrix(:,1,2), avgDataMatrix(:,2,2)*100,'r','LineWidth',2) %225Hz
```

```
plot(avgDataMatrix(:,1,3), avgDataMatrix(:,2,3)*100,'g','LineWidth',2) %250Hz
plot(avgDataMatrix(:,1,4), avgDataMatrix(:,2,4)*100,'m','LineWidth',2) %275Hz
plot(avgDataMatrix(:,1,5), avgDataMatrix(:,2,5)*100,'c','LineWidth',2) %300Hz
plot(avgDataMatrix(:,1,6), avgDataMatrix(:,2,6)*100,'Color',[.8 0.375
0],'LineWidth',2) %325Hz
plot(avgDataMatrix(:,1,7), avgDataMatrix(:,2,7)*100,'k','LineWidth',2) %350Hz

set(gca, 'fontsize', 22, 'linewidth',1)
axis([1.5, 6.5, 75, 100])
l3=legend('200Hz', '225Hz', '250Hz', '275Hz', '300Hz', '325Hz',
'350Hz','Location', 'North', 'Orientation', 'Horizontal');
title('Board 5 Avg P1 & P4, 2.5V In, 1V Ouput')
ylabel('Efficiency (%)')
xlabel('Output Current (A)')
hold off
set(l3,'FontSize',16)
set(hndls(3),'PaperPositionMode', 'auto');

print -r0 -f3 -dpng Board5_Phase_Average1_4
% saveas(gcf,'Board5_Phase_Average1_4','jpg')



% Two Phases Operating
% Plotting Board 5 Phase 1 and 4: 2.5V in, 1V
figure(hndls(4))
hold on
plot(p1_4DataMatrix(:,1,1), p1_4DataMatrix(:,2,1)*100,'b','LineWidth',2)
%175Hz
plot(p1_4DataMatrix(:,1,2), p1_4DataMatrix(:,2,2)*100,'r','LineWidth',2)
%200Hz
plot(p1_4DataMatrix(:,1,3), p1_4DataMatrix(:,2,3)*100,'g','LineWidth',2)
%225Hz
plot(p1_4DataMatrix(:,1,4), p1_4DataMatrix(:,2,4)*100,'m','LineWidth',2)
%250Hz
plot(p1_4DataMatrix(:,1,5), p1_4DataMatrix(:,2,5)*100,'c','LineWidth',2)
%275Hz
plot(p1_4DataMatrix(:,1,6), p1_4DataMatrix(:,2,6)*100,'Color',[.8 0.375
0],'LineWidth',2) %300Hz
plot(p1_4DataMatrix(:,1,7), p1_4DataMatrix(:,2,7)*100,'k','LineWidth',2)
%325Hz
plot(p1_4DataMatrix(:,1,8), p1_4DataMatrix(:,2,8)*100,'Color',[.5 .5
1],'LineWidth',2) %350Hz

set(gca, 'fontsize', 22, 'linewidth',1)
axis([1.5, 6.5, 75, 100])
l4=legend('175Hz','200Hz', '225Hz', '250Hz', '275Hz', '300Hz', '325Hz',
'350Hz','Location', 'North', 'Orientation', 'Horizontal');
title('Board 5 Phase 1 & 4, 2.5V In, 1V Output')
ylabel('Efficiency (%)')
xlabel('Output Current (A)')
hold off
set(l4,'FontSize',16)
set(hndls(4),'PaperPositionMode', 'auto');
```

```
print -r0 -f4 -dpng Board5_Phase1_4
% saveas(gcf,'Board5_Phase1_4','jpg')

%%
cd(option.oldDirectory)

close all
```

G.2 Buck V3 Stages 1-3 Matlab Plotting Code

```
% This scripts generates plots for converter stages 1, 2, and 3 based on data
% collected. Plots for each converter are generated, along with a plot of
% the averages.

load('C:\Users\Stephan\Dropbox\GRA\Thesis\Buck v3\BuckV3_Stages_1_2_3.mat');
% load('/home/sh2/Dropbox/GRA/Thesis/Buck v3/BuckV3_Stages_1_2_3.mat');

close all; clc; % Setup
hndls = setup_figures(5, [1000 700]);
option.directory = 'C:\Users\Stephan\Dropbox\GRA\Thesis\Buck v3\plots'; % Set
directory name
% option.directory = '/home/sh2/Dropbox/GRA/Thesis/Buck v3/plots'; % Set
directory name

% Check if directory exists. If not, create it
if exist(option.directory)
    option.oldDirectory = cd(option.directory);
else
    mkdir(option.directory);
    option.oldDirectory = cd(option.directory);
end

% plot(BuckV3Stage123(6:12,3), BuckV3Stage123(6:12,4));

% Data file is organized as f(Hz) , Iout2, Eff2, Iout1, Eff1, Iout3, Eff3

%% Plot stage 1
% Be aware that stage 1 is the second stage listed in the data file
figure(hndls(1))
hold on

plot(BuckV3Stage123(13:19,6), BuckV3Stage123(13:19,7),'b-','LineWidth',2) %
200Hz
% plot(BuckV3Stage123(20:26,6), BuckV3Stage123(20:26,7),'b--
','LineWidth',2.5) % 225Hz
plot(BuckV3Stage123(27:33,6), BuckV3Stage123(27:33,7),'r-','LineWidth',2) %
250Hz
% plot(BuckV3Stage123(34:40,6), BuckV3Stage123(34:40,7),'r--
','LineWidth',2.5) % 275Hz
plot(BuckV3Stage123(41:47,6), BuckV3Stage123(41:47,7),'g-','LineWidth',2) %
300Hz
% plot(BuckV3Stage123(48:54,6), BuckV3Stage123(48:54,7),'g--
','LineWidth',2.5) % 325Hz
plot(BuckV3Stage123(55:61,6), BuckV3Stage123(55:61,7),'m-','LineWidth',2) %
350Hz
% plot(BuckV3Stage123(62:68,6), BuckV3Stage123(62:68,7),'m--
','LineWidth',2.5) % 375Hz
plot(BuckV3Stage123(69:75,6), BuckV3Stage123(69:75,7),'c-','LineWidth',2) %
400Hz
% plot(BuckV3Stage123(76:82,6), BuckV3Stage123(76:82,7),'c--
','LineWidth',2.5) % 425Hz
plot(BuckV3Stage123(83:89,6), BuckV3Stage123(83:89,7),'Color',[.8 0.375
0],'LineWidth',2) % 450Hz
```

```
% plot(BuckV3Stage123(90:96,6), BuckV3Stage123(90:96,7),'y--
','LineWidth',2.5) % 475Hz
plot(BuckV3Stage123(97:103,6), BuckV3Stage123(97:103,7),'k-','LineWidth',2) %
500Hz

set(gca, 'fontsize', 20, 'linewidth',1)%, 'fontweight', 'bold')
axis([0, 33, 50, 100])
l1=legend('200 Hz', '250 Hz', '300 Hz', '350 Hz', '400 Hz', '450 Hz', '500
Hz','Location', 'North', 'Orientation', 'Horizontal');
title('Converter Stage 1 - 12V In & 1V Ouput')
ylabel('Efficiency (%)')
xlabel('Output Current (A)')
hold off
set(l1,'FontSize',14)
set(hndls(1),'PaperPositionMode', 'auto');
% keyboard
% saveas(gcf,'Stage_1','png')
print -r0 -f1 -dpng Stage_1
% keyboard



%% Plot stage 2
% Be aware that stage 2 is the first stage listed in the data file.
figure(hndls(2))
hold on

plot(BuckV3Stage123(13:19,3), BuckV3Stage123(13:19,4),'b','LineWidth',2) %
200Hz
% plot(BuckV3Stage123(20:26,3), BuckV3Stage123(20:26,4),'b--
','LineWidth',2.5) % 225Hz
plot(BuckV3Stage123(27:33,3), BuckV3Stage123(27:33,4),'r','LineWidth',2) %
250Hz
% plot(BuckV3Stage123(34:40,3), BuckV3Stage123(34:40,4),'r--
','LineWidth',2.5) % 275Hz
plot(BuckV3Stage123(41:47,3), BuckV3Stage123(41:47,4),'g','LineWidth',2) %
300Hz
% plot(BuckV3Stage123(48:54,3), BuckV3Stage123(48:54,4),'g--
','LineWidth',2.5) % 325Hz
plot(BuckV3Stage123(55:61,3), BuckV3Stage123(55:61,4),'m','LineWidth',2) %
350Hz
% plot(BuckV3Stage123(62:68,3), BuckV3Stage123(62:68,4),'m--
','LineWidth',2.5) % 375Hz
plot(BuckV3Stage123(69:75,3), BuckV3Stage123(69:75,4),'c','LineWidth',2) %
400Hz
% plot(BuckV3Stage123(76:82,3), BuckV3Stage123(76:82,4),'c--
','LineWidth',2.5) % 425Hz
plot(BuckV3Stage123(83:89,3), BuckV3Stage123(83:89,4),'Color',[.8 0.375
0],'LineWidth',2) % 450Hz
% plot(BuckV3Stage123(90:96,3), BuckV3Stage123(90:96,4),'y--
','LineWidth',2.5) % 475Hz
plot(BuckV3Stage123(97:103,3), BuckV3Stage123(97:103,4),'k','LineWidth',2) %
500Hz

set(gca, 'fontsize', 20, 'linewidth',1)%, 'fontweight', 'bold')
axis([0, 33, 50, 100])
```

```
l2=legend('200 Hz', '250 Hz', '300 Hz', '350 Hz', '400 Hz', '450 Hz', '500
Hz','Location', 'North', 'Orientation', 'Horizontal')
title('Converter Stage 2 - 12V In & 1V Ouput')
ylabel('Efficiency (%)')
xlabel('Output Current (A)')
hold off
set(l2,'FontSize',14)
set(hndls(2),'PaperPositionMode', 'auto');

% saveas(gcf,'Stage_2','png')
print -r0 -f2 -dpng Stage_2

%% Plot stage 3
figure(hndls(3))
hold on

plot(BuckV3Stage123(13:19,9), BuckV3Stage123(13:19,10),'b','LineWidth',2) %
200Hz
% plot(BuckV3Stage123(20:26,9), BuckV3Stage123(20:26,10),'b--
','LineWidth',2.5) % 225Hz
plot(BuckV3Stage123(27:33,9), BuckV3Stage123(27:33,10),'r','LineWidth',2) %
250Hz
% plot(BuckV3Stage123(34:40,9), BuckV3Stage123(34:40,10),'r--
','LineWidth',2.5) % 275Hz
plot(BuckV3Stage123(41:47,9), BuckV3Stage123(41:47,10),'g','LineWidth',2) %
300Hz
% plot(BuckV3Stage123(48:54,9), BuckV3Stage123(48:54,10),'g--
','LineWidth',2.5) % 325Hz
plot(BuckV3Stage123(55:61,9), BuckV3Stage123(55:61,10),'m','LineWidth',2) %
350Hz
% plot(BuckV3Stage123(62:68,9), BuckV3Stage123(62:68,10),'m--
','LineWidth',2.5) % 375Hz
plot(BuckV3Stage123(69:75,9), BuckV3Stage123(69:75,10),'c','LineWidth',2) %
400Hz
% plot(BuckV3Stage123(76:82,9), BuckV3Stage123(76:82,10),'c--
','LineWidth',2.5) % 425Hz
plot(BuckV3Stage123(83:89,9), BuckV3Stage123(83:89,10),'Color',[.8 0.375
0],'LineWidth',2) % 450Hz
% plot(BuckV3Stage123(90:96,9), BuckV3Stage123(90:96,10),'y--
','LineWidth',2.5) % 475Hz
plot(BuckV3Stage123(97:103,9), BuckV3Stage123(97:103,10),'k','LineWidth',2) %
500Hz

set(gca, 'fontsize', 20, 'linewidth',1)%, 'fontweight', 'bold')
axis([0, 33, 50, 100])
l3=legend('200 Hz', '250 Hz', '300 Hz', '350 Hz', '400 Hz', '450 Hz', '500
Hz','Location', 'North', 'Orientation', 'Horizontal')
title('Converter Stage 3 - 12V In & 1V Ouput')
ylabel('Efficiency (%)')
xlabel('Output Current (A)')
hold off
set(l3,'FontSize',14)
set(hndls(3),'PaperPositionMode', 'auto');

% saveas(gcf,'Stage_3','png')
print -r0 -f3 -dpng Stage_3
```

```
%% Calculate average values
% Create matrix of the average values
% Frequency, Avg Load, Avg Eff

avgValues(:,1) = BuckV3Stage123(13:end,1); % Copy Frequencies
avgValues(:,2) = mean([BuckV3Stage123(13:end,3) BuckV3Stage123(13:end,6)
BuckV3Stage123(13:end,9)],2); % Average Currents
avgValues(:,3) = mean([BuckV3Stage123(13:end,4) BuckV3Stage123(13:end,7)
BuckV3Stage123(13:end,10)],2); % Average Efficiency


%% Plot average values for the three stages.
figure(hndls(4))
hold on

plot(avgValues(1:7,2), avgValues(1:7,3),'b','LineWidth',2) % 200Hz
% plot(avgValues(8:14,2), avgValues(8:14,3),'b--','LineWidth',2.5) % 225Hz
plot(avgValues(15:21,2), avgValues(15:21,3),'r','LineWidth',2) % 250Hz
% plot(avgValues(22:28,2), avgValues(22:28,3),'r--','LineWidth',2.5) % 275Hz
plot(avgValues(29:35,2), avgValues(29:35,3),'g','LineWidth',2) % 300Hz
% plot(avgValues(36:42,2), avgValues(36:42,3),'g--','LineWidth',2.5) % 325Hz
plot(avgValues(43:49,2), avgValues(43:49,3),'m','LineWidth',2) % 350Hz
% plot(avgValues(50:56,2), avgValues(50:56,3),'m--','LineWidth',2.5) % 375Hz
plot(avgValues(57:63,2), avgValues(57:63,3),'c','LineWidth',2) % 400Hz
% plot(avgValues(64:70,2), avgValues(64:70,3),'c--','LineWidth',2.5) % 425Hz
plot(avgValues(71:77,2), avgValues(71:77,3),'Color',[.8 0.375
0],'LineWidth',2) % 450Hz
% plot(avgValues(78:84,2), avgValues(78:84,3),'y--','LineWidth',2.5) % 475Hz
plot(avgValues(85:91,2), avgValues(85:91,3),'k','LineWidth',2) % 500Hz

set(gca, 'fontsize', 20, 'linewidth',1)%, 'fontweight', 'bold')
axis([0, 33, 50, 100])
l4=legend('200 Hz', '250 Hz', '300 Hz', '350 Hz', '400 Hz', '450 Hz', '500
Hz','Location', 'North', 'Orientation', 'Horizontal')
title('Average of Stages 1, 2, & 3 - 12V In & 1V Ouput')
ylabel('Efficiency (%)')
xlabel('Output Current (A)')
hold off
set(l4,'FontSize',14)
set(hndls(4),'PaperPositionMode', 'auto');

% saveas(gcf,'Average_1_2_3','png')
print -r0 -f4 -dpng Average_1_2_3

%% Calculate the average delta between the efficiency of the different
frequencies
% Calculated as [(Eff(f1)-Eff(f2)) + (Eff(f2)-Eff(f3))
% +...(Eff(fn-1)-Eff(fn)]/n

firstIndex = 13; % starting index, skipping 175Hz
currentIndex = 7; % Number of current measurements at each freq

% Freq, current, eff, 3rd dimension is stage
tempDataArray = zeros(length(BuckV3Stage123(13:end,1)), 3, 3); % preallocate
```

```
tempDataArray (:,1:3,1) = BuckV3Stage123(13:end,[1 6 7]);
tempDataArray (:,1:3,2) = BuckV3Stage123(13:end,[1 3 4]);
tempDataArray (:,1:3,3) = BuckV3Stage123(13:end,[1 12 13]);

%% Calculate average current at each frequency

dataDeltaArray = zeros(currentIndex,2,3); % preallocate

for iStage = 1:3
    for iCurrent = 1:currentIndex
        for iFreq = 1:length(unique(tempDataArray(:,1,iStage)))
            dataDeltaArray(iCurrent,1,iStage) = ...
                dataDeltaArray(iCurrent,1,iStage) + ...
                tempDataArray((iFreq-1)*currentIndex+iCurrent,2,iStage);
        end
        dataDeltaArray(iCurrent,1,iStage) = ...
            dataDeltaArray(iCurrent,1,iStage)./ ...
            length(unique(tempDataArray(:,1,iStage)));
    end
end

%% Calculate average delta between each frequency

for iStage = 1:3
    for iCurrent = 1:currentIndex
        for iFreq = 1:length(unique(tempDataArray(:,1,iStage)))-1
            dataDeltaArray(iCurrent,2,iStage) = ...
                dataDeltaArray(iCurrent,2,iStage) + ...
                tempDataArray((iFreq-1)*currentIndex+iCurrent,3,iStage) ...
                - tempDataArray((iFreq)*currentIndex+iCurrent,3,iStage);
        end
        dataDeltaArray(iCurrent,2,iStage) = ...
            dataDeltaArray(iCurrent,2,iStage)./ ...
            length(unique(tempDataArray(:,1,iStage)));
    end
end


%% Plot Average of the delta between the efficiency of the different
frequencies
figure(hndls(5))
hold on

plot(dataDeltaArray(:,1,1), dataDeltaArray(:,2,1),'b','LineWidth',2.5) %
Stage 1
plot(dataDeltaArray(:,1,2), dataDeltaArray(:,2,2),'r','LineWidth',2.5) %
Stage 2
plot(dataDeltaArray(:,1,3), dataDeltaArray(:,2,3),'g','LineWidth',2.5) %
Stage 3

set(gca, 'fontsize', 20, 'linewidth',1)%, 'fontweight', 'bold')
axis([0, 32, 0, 2])
l5=legend('Stage 1', 'Stage 2', 'Stage 3','Location', 'North', 'Orientation',
'Horizontal')
```

```
title('Average of \DeltaEfficiency Stages 1, 2, & 3 - 12V In & 1V Ouput')
ylabel('\DeltaEfficiency (Avg %)')
xlabel('Output Current (A)')
hold off
set(l5,'FontSize',14)
set(hndls(5),'PaperPositionMode', 'auto');

% saveas(gcf,'Delta_Eff_1_2_3','png')
print -r0 -f5 -dpng Delta_Eff_1_2_3


%%
cd(option.oldDirectory)

close all
```

G.3 Buck V3 Stages 7-9 Matlab Plotting Code

```
% This scripts generates plots for converter stages 7, 8, and 9 based on data
% collected. Plots for each converter are generated.

load('C:\Users\Stephan\Dropbox\GRA\Thesis\Buck v3\BuckV3_Stages_7_8_9.mat');
% load('/home/sh2/Dropbox/GRA/Thesis/Buck v3/BuckV3_Stages_7_8_9.mat');

close all; clc; % Setup
hndls = setup_figures(3, [1000 700]);
option.directory = 'C:\Users\Stephan\Dropbox\GRA\Thesis\Buck v3\plots'; % Set
directory name
% option.directory = '/home/sh2/Dropbox/GRA/Thesis/Buck v3/plots'; % Set
directory name

% Check if directory exists. If not, create it
if exist(option.directory)
    option.oldDirectory = cd(option.directory);
else
    mkdir(option.directory);
    option.oldDirectory = cd(option.directory);
end

% plot(BuckV3Stage123(6:12,3), BuckV3Stage123(6:12,4));

% Data file is organized as f(Hz) , Iout2, Eff2, Iout1, Eff1, Iout3, Eff3

%% Plot stage 7
figure(hndls(1))
hold on

plot(BuckV3Stage789(3:9,2), BuckV3Stage789(3:9,3),'b','LineWidth',2.5) %
200Hz
plot(BuckV3Stage789(10:16,2), BuckV3Stage789(10:16,3),'r','LineWidth',2.5) %
250Hz
plot(BuckV3Stage789(17:23,2), BuckV3Stage789(17:23,3),'g','LineWidth',2.5) %
300Hz
plot(BuckV3Stage789(24:30,2), BuckV3Stage789(24:30,3),'m','LineWidth',2.5) %
350Hz
plot(BuckV3Stage789(31:37,2), BuckV3Stage789(31:37,3),'c','LineWidth',2.5) %
400Hz
plot(BuckV3Stage789(38:44,2), BuckV3Stage789(38:44,3),'Color',[.8 0.375
0],'LineWidth',2.5) % 450Hz
plot(BuckV3Stage789(45:51,2), BuckV3Stage789(45:51,3),'k','LineWidth',2.5) %
500Hz

set(gca, 'fontsize', 20, 'linewidth',1)
axis([0, 22, 50, 100])
l1=legend('200 Hz', '250 Hz', '300 Hz', '350 Hz', '400 Hz', '450 Hz', '500
Hz','Location', 'North', 'Orientation', 'Horizontal');
title('Converter Stage 7 - 12V In & 1V Ouput')
ylabel('Efficiency (%)')
xlabel('Output Current (A)')
hold off
set(l1,'FontSize',14)
```

```
set(hndls(1),'PaperPositionMode', 'auto');

% saveas(gcf,'Stage_7','png')
print -r0 -f1 -dpng Stage_7


%% Plot stage 8
figure(hndls(2))
hold on

plot(BuckV3Stage789(3:9,6), BuckV3Stage789(3:9,7),'b','LineWidth',2.5) %
200Hz
plot(BuckV3Stage789(10:16,6), BuckV3Stage789(10:16,7),'r','LineWidth',2.5) %
250Hz
plot(BuckV3Stage789(17:23,6), BuckV3Stage789(17:23,7),'g','LineWidth',2.5) %
300Hz
plot(BuckV3Stage789(24:30,6), BuckV3Stage789(24:30,7),'m','LineWidth',2.5) %
350Hz
plot(BuckV3Stage789(31:37,6), BuckV3Stage789(31:37,7),'c','LineWidth',2.5) %
400Hz
plot(BuckV3Stage789(38:44,6), BuckV3Stage789(38:44,7),'Color',[.8 0.375
0],'LineWidth',2.5) % 450Hz
plot(BuckV3Stage789(45:51,6), BuckV3Stage789(45:51,7),'k','LineWidth',2.5) %
500Hz

set(gca, 'fontsize', 20, 'linewidth',1)
axis([0, 22, 50, 100])
l2=legend('200 Hz', '250 Hz', '300 Hz', '350 Hz', '400 Hz', '450 Hz', '500
Hz','Location', 'North', 'Orientation', 'Horizontal');
title('Converter Stage 8 - 12V In & 1V Ouput')
ylabel('Efficiency (%)')
xlabel('Output Current (A)')
hold off
set(l2,'FontSize',14)
set(hndls(2),'PaperPositionMode', 'auto');

% saveas(gcf,'Stage_8','png')
print -r0 -f2 -dpng 'Stage_8'


%% Plot stage 3
figure(hndls(3))
hold on

plot(BuckV3Stage789(3:9,10), BuckV3Stage789(3:9,11),'b','LineWidth',2.5) %
200Hz
plot(BuckV3Stage789(10:16,10), BuckV3Stage789(10:16,11),'r','LineWidth',2.5)
% 250Hz
plot(BuckV3Stage789(17:23,10), BuckV3Stage789(17:23,11),'g','LineWidth',2.5)
% 300Hz
plot(BuckV3Stage789(24:30,10), BuckV3Stage789(24:30,11),'m','LineWidth',2.5)
% 350Hz
plot(BuckV3Stage789(31:37,10), BuckV3Stage789(31:37,11),'c','LineWidth',2.5)
% 400Hz
```

```
plot(BuckV3Stage789(38:44,10), BuckV3Stage789(38:44,11),'Color',[.8 0.375
0],'LineWidth',2.5) % 450Hz
plot(BuckV3Stage789(45:51,10), BuckV3Stage789(45:51,11),'k','LineWidth',2.5)
% 500Hz

set(gca, 'fontsize', 20, 'linewidth',1)
axis([0, 32, 50, 100])
l3=legend('200 Hz', '250 Hz', '300 Hz', '350 Hz', '400 Hz', '450 Hz', '500
Hz','Location', 'North', 'Orientation', 'Horizontal');
title('Converter Stage 9 - 12V In & 1V Ouput')
ylabel('Efficiency (%)')
xlabel('Output Current (A)')
hold off
set(l3,'FontSize',14)
set(hndls(3),'PaperPositionMode', 'auto');

% saveas(gcf,'Stage_9','png')
print -r0 -f3 -dpng Stage_9

%%
cd(option.oldDirectory)

close all
```