FABRICATION AND ASSEMBLY OF ULTRA THIN FLEXIBLE

ACTIVE PRINTED CIRCUITS

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FABRICATION AND ASSEMBLY OF ULTRA THIN FLEXIBLE ACTIVE PRINTED CIRCUITS

Tan Zhang

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FABRICATION AND ASSEMBLY OF ULTRA THIN FLEXIBLE

ACTIVE PRINTED CIRCUITS

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Tan Zhang, daughter of Xiangqiao Zhang and Bingqian He, was born on June 8, 1973 in Beijing, China. She entered the Beijing University of Aeronautics & Astronautics in 1992 in the Department of Materials Engineering. After graduating with a Bachelor of Science Degree in Polymer Science & Engineering in 1996, she joined the graduate school in Beijing University of Aeronautics & Astronautics and completed a Master of Science in Materials Engineering in 1999. She entered the Doctoral program in the Department of Electrical and Computer Engineering at Auburn University in 2001 with the award of Graduate Presidential Fellowship and Research Fellowship.

DISSERTATION ABSTRACT

FABRICATION AND ASSEMBLY OF ULTRA THIN FLEXIBLE

ACTIVE PRINTED CIRCUITS

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Doctor of Philosophy, May 11, 2006
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Tremendous attention has been focused on flexible printed circuits for their light weight, minimized dimension and three dimensional packaging capabilities. However, the traditional flexible circuit fabrication and assembly process can not meet the demands for the continuous reducing of flexible circuit dimensions, while increasing the packaging density.

In this study, an ultra thin polyimide and liquid crystal polymer (LCP) flexible printed circuit fabrication process was developed. The circuits had 8 mil line pitch pads and 3 – 4 mil diameter vias, which is comparable to flexible substrates for high density interconnection applications.

Thinned silicon flip chip were then assembled on the polyimide and LCP flexible printed circuit with a backside assembly scheme, which not only lowered the assembly

profile but also eliminated the need for a solder mask. With the development of an immersion flip chip solder bumping process, the overall assembly profile was lowered further and an hourglass shaped solder joint was obtained which has potential to improve the thermomechanical reliability.

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CHAPTER 1

INTRODUCTION

A great deal of attention is currently being focused on flexible circuits and packages for industrial electronics due to their light weight, high performance and high density of functions per unit volume. Advanced technologies are being forced to develop very rapidly in order to realize the full potential for these flexible applications. In 2005, the worldwide market value for flexible circuits is estimated to reach $ 5.9 billion and an average annual growth rate of 13.5% and market of $11.2 billion is expected in 2010, as indicated in Figure 1-1 [1].

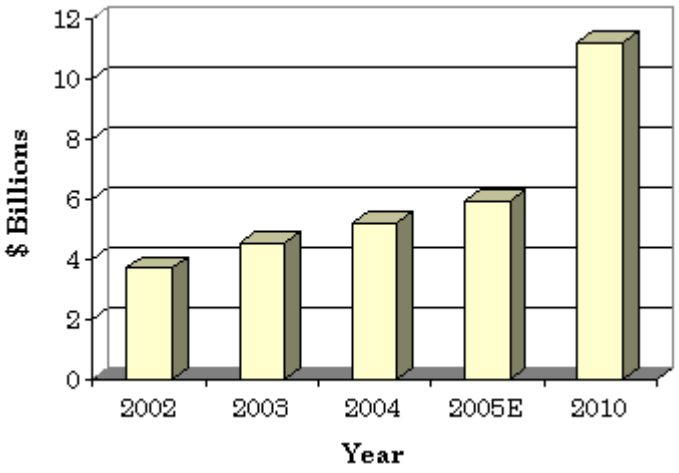


Figure 1-1 Worldwide Flexible Circuits Market Value [1]

Polyimide is the most popular choice for flexible circuit applications in industry because of its combination of electrical properties, mechanical properties and high

temperature capability. However, some of the major weakness of polyimide, including high moisture absorption and high coefficient of thermal expansion (CTE), limit it applications especially under harsher environment. The increasing attention has been focused on liquid crystal polymer (LCP) for its controllable CTE, low moisture absorption, chemical resistivity and dimensional stability [2-3].

Flexible circuits have a wide range of applications. The major applications for conventional flex circuits are in the automotive, military and computer area. Flex circuits with high density interconnections, line pitch less than 200 μm and via diameter less than 175 μm, are primarily used in disk drive, wireless communication devices and flat panel display, as illustrate in Figure 1-2 [4]. The continuous demands for reduced size, weight and increased function density have been a major driving force in flexible circuits industry.

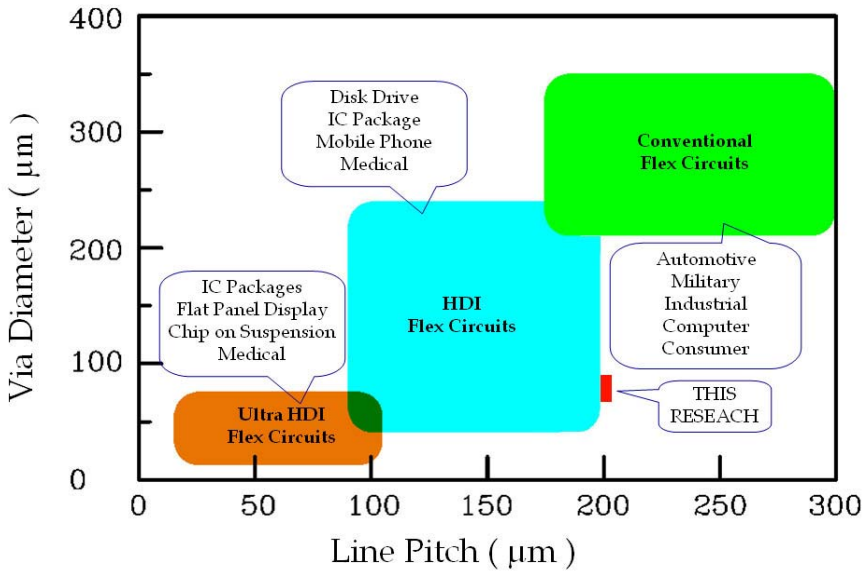


Figure 1-2 High Density Interconnection and Application [4]

The objective of this research was to develop a low profile flip chip assembly process with improved reliability. The overall packaging profile can be reduced by using thinned flexible substrate materials, thinned silicon chip and compact assembly or packaging structure. In this research, the 2 mil thick polyimide and LCP flexible substrates were selected for the studying of flexible circuit fabrication process. A circuit pattern of 8 mil in line pitch and 3 – 4 mil in via diameter was created. The feature dimension is comparable with HDI flexible circuits as indicated in Figure 1-2. The thinned silicon flip chip of 2 mil in thickness was then integrated on polyimide and LCP flexible circuits by using backside assembly structure, as illustrated in Figure 1-3. In this assembly, the flip chip was assembled through dielectric materials vias, which is the opposite direction to that of the copper circuitry patterns. The advantages of this structure include the elimination of solder mask and reduce the assembly height. The overall assembly profile can be further reduced by using the solder bump with lower profile.

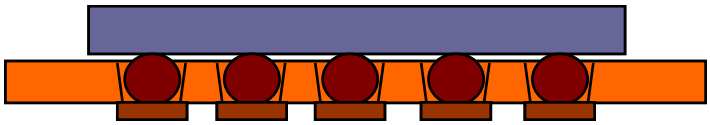


Figure 1-3 Backside Flip Chip Assembly

Chapter 2 reviews the flexible circuits fabrication processes, silicon thinning methods and thinned flexible circuits assembly approaches. The photolithography, wet etching, dry etching and surface finish process development techniques used for polyimide and LCP flexible printed circuits fabrication are presented in Chapter 3. Chapter 4 discusses the backside assembly of thinned flip chip assemblies on polyimide

and LCP flexible substrates, which includes an alternate solder bumping process, substrate treatment, materials selection and assembly process. Conclusions and suggestions for future work are summarized in Chapter 5.

CHAPTER 2

LITERATURE REVIEW

The increasing demand for new and innovative industrial applications and products such as wireless communication, high speed data storage and transfer is driving the markets for smaller, lighter, lower cost devices with more functions than ever before. Flexible circuits are a strong candidate for realizing the next step in electronics miniaturization with multi-functions as a result of light weight, high flexibility and high performance. In order to maximize the benefits of flexible circuits, materials properties, processing and applications must to be optimized. This study will examine some of the issues involved.

2.1 Flexible Circuit Substrates

2.1.1 Polymer Based Films for Flexible Circuits

Thin polymer films made of polyimide, polyester, liquid crystal polymers (LCP) and other materials are used as the base dielectric for fabrication of flexible circuits. The polymer film serves as the support structure for the electrical interconnection pattern.

2.1.1.1 Polyimide

Polyimides are the most commonly used material for flexible, high-density interconnection circuit applications. They belong to the family of high temperature thermosetting polymers originally developed by the DuPont Company, and have been mass produced since 1955 [5-6]. The nitrogen and carbonyl groups in its polymer network structure provide the material with the combination of excellent electrical insulation, high mechanical strength, high temperature endurance and excellent chemical resistance, which supports fine feature applications, roll-to-roll processing ability and harsh environment stability [2]. Polyimide base film materials are commercially available from E. I. DuPont de Nemours & Co., Ube Industries, Ltd., and Kaneka Corporation [7]. The copper cladding on the polyimide base film can be applied either with adhesive or in an adhesiveless fashion. The drawbacks of adhesive polyimide laminate include its overall thickness and weight, the sometimes poor strength of the adhesive at elevated temperatures and copper thickness limitations [7]. Compared with adhesive laminates, adhesiveless laminates are thinner and lighter, and may be used with fine features due to the availability of very thin copper, which typically ranges from 5 to 18 μm [7]. The adhesive copper clad polyimide laminate is commonly used for conventional flex circuits and tape automated bonding (TAB) applications, while the major applications for adhesiveless laminates include interconnections on hard disk drive and chip scale packages (CSPs) [7].

The primary applications of polyimide flex circuits substrate are in consumer products, such as laptops, cameras and mobile phones. However, one of the major disadvantages of polyimide lies in its high moisture absorption. Its water uptake is

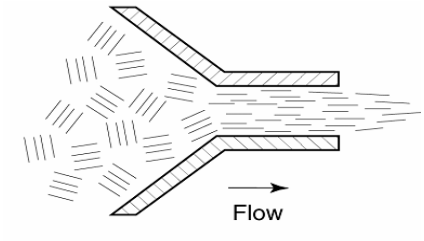
typically 1-3% water by weight [2], which will degrade signal performance at high frequencies because water is a very polar molecule [8].

2.1.1.2 Liquid Crystal Polymer

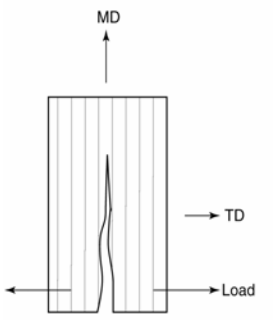
Liquid crystal polymers (LCPs), make up a broad class of thermoplastic aromatic polyesters, and offer an alternative for flexible circuit substrate that has recently attracted interest in the industry [3]. They are called liquid crystal polymers because the segments of the polymer can be aligned in a near crystalline structure in the molten or solvated state. The use of LCPs for application in multilayer circuits has been explored by a number of printed circuit manufacturers since the mid-1990s [4]. Teflon and ceramics based materials used to be the only choices for microwave engineers. LCPs are lower in cost than either of these, and at the same time offer a low loss (dissipation) factor of 0.004 and low dielectric constant (2.8 to 3) even at 35 GHz [4, 8–11]. Besides these excellent high frequency electrical properties, moisture absorption is also an important issue. LCP's moisture absorption is typically less than 0.1 %, which makes them more stable than polyimides and hence they are expected to extend the application of flexible circuits into more severe moisture environment and higher frequencies [10]. LCPs have a very low coefficient of thermal expansion (CTE), which minimizes the effects of CTE mis-matches between the silicon chip and the substrate and hence increases the reliability of the complete package. Other advantages of LCPs include high temperature capability, excellent dimensional stability and extraordinary barrier properties for hermetic packaging.

Like polyimides, LCP laminate is commercially available in the form of adhesiveless sheet materials from flex film suppliers 3M, W. L. Gore, Rogers Corporation, Sanmina-SCI and Foster-Miller [2,8].

The main difficulty with LCP processing originates from its rigid-rod nature and polymer molecules [12]. During the traditional extrusion process, polymer segments are aligned in the extrusion (machine) direction, which results in highly oriented micro-structure in the flow direction, as illustrated in Figure 2-1 (a) [13]. Tensile strength in the machine direction (MD) will thus be as much as one order of magnitude higher than that in transverse direction (TD), as shown in Figure 2-1 (b) [13]. These anisotropic film properties are not suitable for advanced electronics packaging applications.



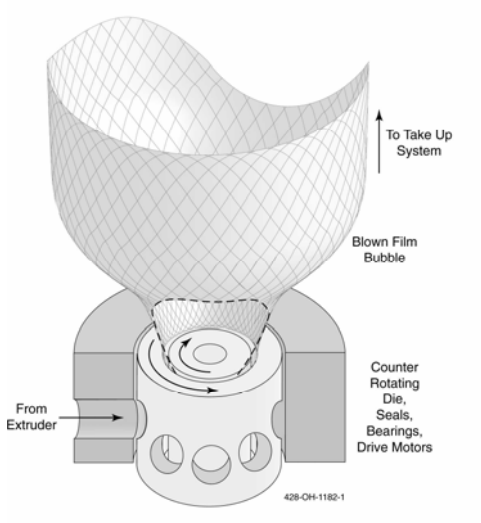
(a) Polymer Segment Alignment in Uniaxial Extrusion



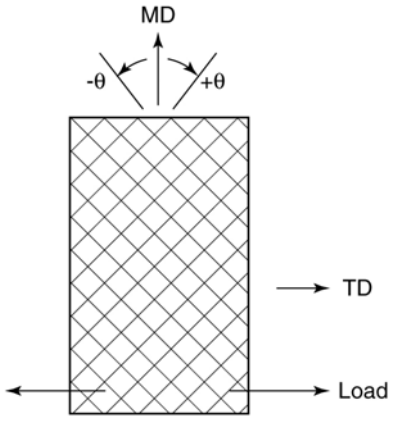
(b) Anisotropic Film Properties in the Machined Direction (MD) and the Transverse Direction (TD) under Load

Figure 2-1 Illustrate of Uniaxial Extrusion and Film Properties [13]

To address this issue, Foster-Miller developed a biaxial extrusion process, as shown in Figure 2-2 (a) [14]. By controlling the extrusion speed, counter die rotating rate, draw rate and blow up ratio, a specific combination of film properties, which include mechanical properties and the coefficient of thermal expansion can be obtained. The biaxial film is quasi-isotropic and has excellent mechanical strength and dimensional stability in both the extrusion and transverse directions, as in Figure 2-2 (b) [14].



(a) Biaxial Extrusion Process Developed by Foster-Miller



(b) Biaxial LCP Film Under Transverse Load

Figure 2-2 Biaxial Extrusion and Biaxial Film [14]

LCP from Rogers Corporation is referred to using its trade name of R/flex® series, which includes R/flex® 3600 and R/flex®3850, as shown in Figure 2-3 [15]. These feature a 1 or 2 mil thick dielectric film and 0.5 oz electro-deposit copper cladding. R/flex® 3600 is a single-sided copper clad LCP laminate circuit material with a melting temperature (T_m) of 290°C and a CTE of 17 ppm/K, while R/flex®3850 is a double copper cladding LCP with T_m of 315°C and CTE of 17 ppm/K. Both are adhesiveless laminates and can be used as single layer construction or inner layer cores in multilayer substrate construction with or without R/flex® 3908 bonding film, which will result in an all-LCP structure, as illustrated in Figure 2-4 [15]. Combined with epoxy, acrylic, cyanate ester, or PTFE resin systems, the properties of multilayer LCP structures can be enhanced as needed [15].

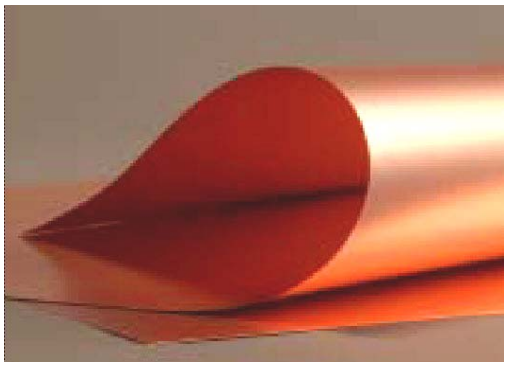
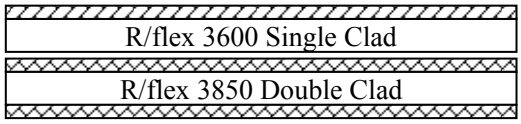
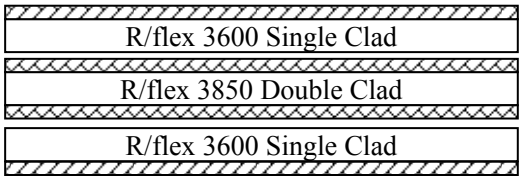


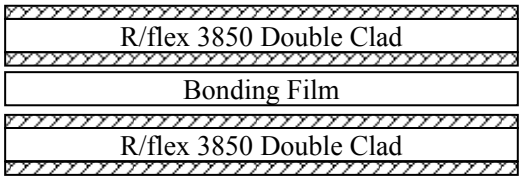
Figure 2-3 LCP Flexible Material [15]



(a) 3 Layer Build



(b) 4 Layer Build



(c) 4 or more Layer Build with Bonding Film

Figure 2-4 LCP Single Layer and Multi-layer Structure [15]

2.1.1.3 Polyester

Polyethylene terephthalate (PET) is a type of polyester which is commonly used as a flexible circuit material for its tensile strength and fatigue resistance. It is a cost-effective alternative to polyimide flex circuits in the non-hostile applications of membrane switches [16], point-of-sale (POS) terminals and medical equipment [17]. Polyethylene naphihalate (PEN), another type of polyester, has also been employed in flexible circuit applications. It is manufactured with a biaxial extrusion process, therefore it offers homogenous in-plane mechanical properties. Combined with its higher glass transition temperature, and better chemical resistance properties, PEN can be used in harsher environmental applications over PET. Major properties comparison of LCP, polyimide and polyester are listed in Table 2-1 [10, 18-19].

Table 2-1 Comparison of Selected Properties of Flex Circuit Base Materials [10, 18-19]

	Maximum Use Temperature (°C)	Dielectric Constant	Loss Tangent	Moisture Uptake (%)	Tensile Strength (kpsi)
PET	~ 105	3.2	0.005	0.3	25
Polyimide	> 300	3.5	0.005	~1.2-3.0	30
LCP	> 250	2.8-3.0	0.003	0.02-0.1	15-25
PEN	160 -180	2.9	0.004	1	30

2.1.2 Metal Cladding for Flexible Circuits

Copper foil is the most widely used metal foil used in the construction of flexible circuits because copper is a good electrical conductor and it is abundant, low in cost and compatible with many different chemical and mechanical processes. There are two categories of copper foil, rolled annealed copper foil and electrodeposited copper foil.

For rolled annealed copper construction, the roughened copper foil is laminated to the dielectric film, such as LCP, at high temperature. The roughened copper is mechanically locked into film surface as it cools [2]. This type of copper foil possesses better fatigue ductility, but some copper nodules are left behind during copper patterning, which will limit its use in flexible circuits that include fine pitch areas. Electrodeposited copper foil can also be laminated to dielectric film, such as polyimide. Compared with rolled annealed copper, electrodeposited copper is less rough.

An alternative copper metallization method is achieved by directly plating the copper onto a vacuum deposited metallic adhesion layer [7]. Microinterconnect Systems Divison (MSD) of 3M (St Paul, Minn.) developed this adhesiveless copper metallization approach, where a thin layer of sputtered chromium or nickel tiecoat is followed by a

copper seed layer and electroplated copper, as illustrated in Figure 2-5 [2, 7]. Features as fine as 30 μm pitch have been fabricated using this approach [2]. New modifications and approaches for using copper metallization continue to be developed to the seemingly endless demand for the miniaturization of electronics products and systems.

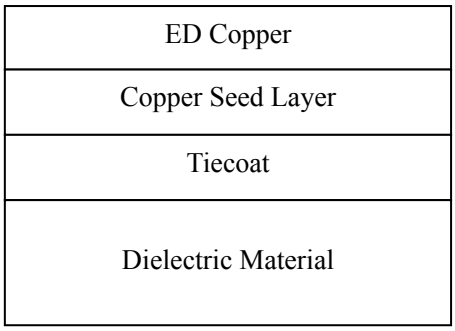


Figure 2-5 Typical Adhesiveless Flexible Laminate Construction [7]

Although copper is the most popular choice for flexible circuit construction, many other pure metal and metal alloy foils are being investigated, including aluminum, nickel, stainless steel, alloy 42, gold, silver, and copper alloys such as beryllium copper, and phosphor bronze [20]. Polymer thick films (PTF) are also suitable for creating conductive patterns on dielectric materials by means of stencil, screen or inkjet printing. Silver and/or carbon is dispersed in either thermoplastic or thermosetting resins to provide electrical conductivity.

2.1.3 Adhesives in Flexible Circuits

The main functions of adhesives are twofold, the first being to bond metal foil and base dielectric material together, and the other to be used between layers to create a multi-layer or rigid-flex construction. The selection of adhesive is critical, since the

electric properties of the adhesives will affect circuit performances for high frequency applications.

There are two categories of adhesive, thermosetting adhesives and thermoplastics adhesives. Commonly used thermosetting adhesives are butyral-phenolic, polyester, acrylic, epoxies, and thermosetting polyimide. Butyral-phenolic adhesive's attractive features include its low flow characteristics and moisture uptake. The low cost polyester adhesives have lower processing temperatures, which is an advantage for the bonding process, but also a disadvantage, due to their poor high temperature performance. They are typically used with polyester base films. Acrylic adhesives are usually used in polyimide flexible circuits for their excellent adhesion and ease of process control. Their disadvantages lie in their relatively high coefficients of thermal expansion (CTE) and swelling in hot alkaline solutions. Epoxies, with their universal bonding abilities, are also often used in flexible circuits. However, the downside of epoxies is their brittleness and high moisture absorption. Polyimide adhesives are also used in polyimide flexible substrates due to their high processing temperatures. Also, due to the similar properties of the adhesive and base material, "adhesiveless" flexible laminates can be constructed.

Thermoplastic adhesives options include fluorinated ethylene propylene (FEP) (e.g. Teflon®), polyether ether ketone (PEEK), polyether sulfone or polyether sulphone (PES), and polyether imide (PEI) [21]. These adhesives have high melting points, and hence require high temperature and pressure for bonding to occur.

2.2 Flexible Printed Circuits Processing

2.2.1 Copper Circuit Process

Copper is the most often used metal layer on flexible circuit substrates. There are four major process choices that can be used to create copper circuits, namely additive, semi-additive, semi-subtractive and subtractive process, as illustrated in Figure 2-6 [22].

Additive processing is not commonly used, but is a potential option. There are three ways to achieve additive processing. The first is to laminate negative photoresist images of the circuit pattern onto the dielectric, so the exposed dielectric can then be plated. However, the electroless plating rate is relatively low, usually 2 – 5 μm per hour [23]. The second method is a variation of the first, in which a reactive ink is printed onto the dielectric material and the circuit pattern is fused, followed by metal deposition using a plating process. In the third method a mirrored circuit is plated onto a second substrate, followed by lamination onto the dielectric material for circuit transfer.

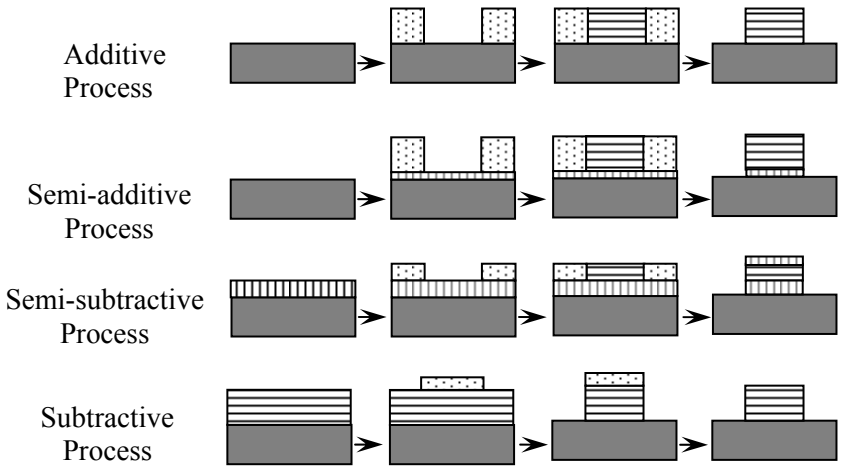


Figure 2-6 Copper Processing Options

In semi-additive methods, a thin layer of copper is deposited onto the entire dielectric

material area either by electroless plating or a sputtering process. Nickel or chrome serves as the adhesion layer between the copper and dielectric base materials [23-25]. This thin copper film is coated with photoresist then patterned, just as in the additive approach, and then electroplating is used to obtain the desired copper thickness. The photoresist, background copper and adhesion layer are removed by etching after plating [26].

The semi-subtractive approach is largely distinguished by the thickness of base copper. The base copper thicknesses for semi-subtractive, subtractive and semi-additive approaches are 4 to 5 μm, 12 to 18 μm and 0.5 to 2 μm, respectively. The semi-subtractive process is similar to the semi-additive method, but the circuits require an over plating in the semi-subtractive process to ensure accurate circuit features.

Subtractive processing is the most commonly used method for flexible circuits fabrication [26]. A photoresist is directly coated onto the copper to define the circuit pattern and then etched to create the circuit.

Variations of the above four major copper patterning processes can be used to achieve the best results for different circuit schemes and designs. Generally, additive processes produce the most accurate and finest features, but at a higher cost. Subtractive processes are most often used and are generally more straightforward, although the cross-section of the copper assumes a non vertical side wall as a result of isotropic chemical etching [27].

2.2.2 Dielectric Materials Processing

Mechanical drilling, laser drilling, chemical etching and dry etching (plasma etching) can be used to form holes or vias in the dielectric material of flexible circuits. Mechanical drilling is usually only suitable for holes or vias which are larger than 8 mils in diameter [28].

2.2.2.1 Laser Processing

IR lasers, whose wavelength lies in the infrared portion of the electromagnetic spectrum (>700 nm), are widely used in polymer processing. These lasers include carbon dioxide (CO_2), diode, and IR neodymium lasers. The heat of these lasers thermally evaporates the plastic to form holes or vias. Since each type of plastic behaves differently at each IR wavelength, a different type of IR laser may be required for each type of plastic [29-31].

UV lasers, such as UV neodymium, are a category of laser with wavelengths shorter than 400 nm. Compared to IR lasers, UV laser drilling is a "cold" processing approach. High energy UV photons break polymer bonds without heating up the local surface area, which can thus produce finer features with smoother edges.

The most commonly used lasers for polymers are CO_2 and YAG or UV assisted YAG. CO_2 lasers have a wavelength of 10.6 μm [32]. The beam typically passes through a mask to shape the image and focus it onto the processing surface. YAG lasers have a wavelength of 1064 nm. Figure 2-7 shows the configuration of a YAG laser system [32].

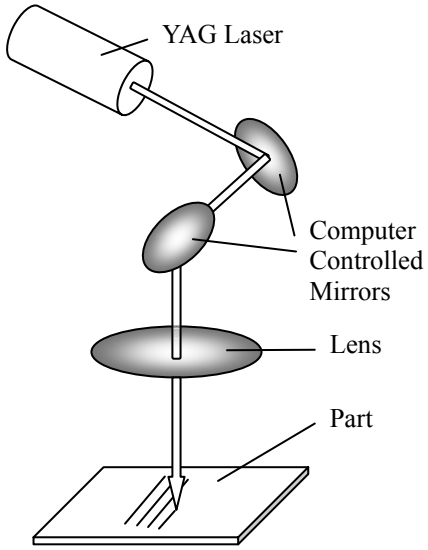


Figure 2-7 Configuration of YAG Laser System [32]

2.2.2.2 Plasma Processing

Gas plasma etching (or dry etching) can be used to etch most organic polymers. Dry etching technology can be divided into three separate classes, which are referred to as reactive ion etching (RIE), sputter etching, and vapor phase etching [33-35].

In RIE, the substrate is placed inside a reactor with one or more gases. The process combines chemical reactions and physical bombardment. The chemical part of plasma etching is isotropic, while the physical part is anisotropic. The plasma is composed of the ionized gas molecules that are created in the gas mixture using an RF power source. Ions are accelerated towards and react at the surface of the material being etched, forming a gaseous or vapor material. This is the chemical part of reactive ion etching. The physical part of plasma etching is the result of high energy ions that knock atoms out of the material surface. RIE is a flexible but difficult process to develop and control since it requires a careful balance of chemical and physical etching. Many parameters can be

adjusted during RIE, including the gas mixture, vacuum level, and power level. Different etch rates, surface topology, and side wall quality can be obtained under different etching conditions and chemical/physical balance [36-37].

Deep reactive ion etching (DRIE) is a subclass of RIE which is gaining in popularity. In this process, nearly vertical sidewalls with etch depths of hundreds of micrometers can be achieved. The primary technology is based on the Bosch process, in which two different gas compositions are alternated in the reactor [38]. The first gas composition creates a passivation layer on the sample to be etched, and the second gas performs the etching. Passivation is only built up on the sidewalls of samples, not on the horizontal surfaces. As a result, a high aspect ratio of etched features can be achieved. This process is usually applied to fine feature etching in thick films.

Sputter etching is similar to RIE but without the reactive ions. The etching mechanism is the ion bombardment carried out in the direction which is normal to the sample to be etched. Highly anisotropic vias can be obtained because there is little sidewall sputtering. The major limitation is its low etch selectivity, the ion bombardment will remove atoms from both the surface to be etched and the mask layer [39-40].

Vapor phase etching can be done with simpler equipment than that required by RIE. In this process the sample to be etched is placed inside a chamber and one or more gases are introduced. The material to be etched is etched at the surface in a chemical reaction with the gas molecules. One of the challenges in vapor phase etching is that by-products can be re-deposited on the sample to be etched. Therefore, the process must be carefully designed and controlled so that no by-products form due to the

chemical reaction that interferes with the etching process. Vapor phase etching also tends to be isotropic.

Dry etching is a relatively high cost technology. It is usually used when fine feature resolution, a vertical sidewall and a high aspect ratio are needed.

2.2.2.3 Chemical Etching

Compared with dry etching, wet chemical etching of dielectric materials is cost-effective especially in large volume processing. In polyimide chemical etching, the etchant is composed of a KOH solution and aliphatic amine [41]. Figure 2-8 illustrates the chemical reaction mechanism. When soaked in the etching solution, the imide rings are broken, hence polyimide is degraded and then etched away [42]. The etching rate varies with temperature and the structure of the polyimide. One of the major disadvantages of chemical etching is that it is difficult to obtain straight side walls, as shown in Figure 2-9.

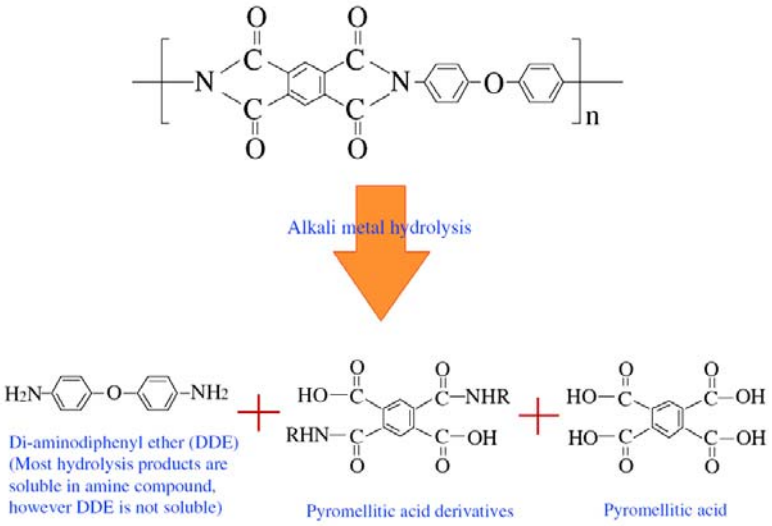


Figure 2-8 Polyimide Chemical Etching Mechanism [41]

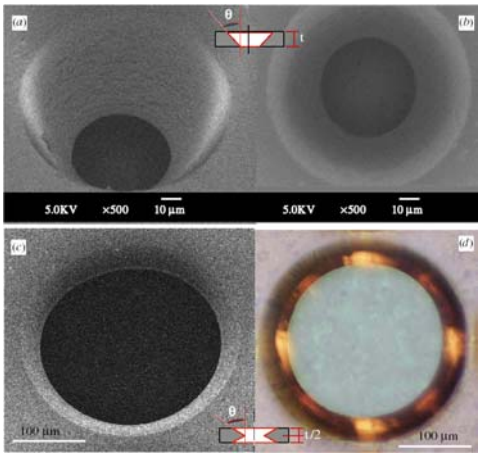


Figure 2-9 Polyimide Via Side Wall in Chemical Etch [41]

2.3 Silicon Thinning

Silicon backside thinning can be carried out by mechanical grinding or chemical mechanical polishing (CMP). In mechanical grinding, the wafer is cleaned and dried and then a protective film is applied on the front side of the wafer to protect it from damage. Figure 2-10 shows the machine configuration for mechanical grinding. The wafer is loaded into a cassette and then transferred onto a vacuum chuck. The chuck rotates relative to a cup shaped grinding wheel which also rotates on its own axis so every point of the wafer plane comes into contact with the grinding wheel. The chuck rotation rate, grinding wheel rotation rate and feed-in rate can be adjusted to control the silicon removal rate. The grinding wheels are classified by grit size and bonding materials. For coarse grinding, the grit size usually ranges from mesh #100 to # 700. In fine grinding, the grit sizes used are mesh #1000 to #4000. The precision of mechanical grinding can be controlled to the micrometer level.

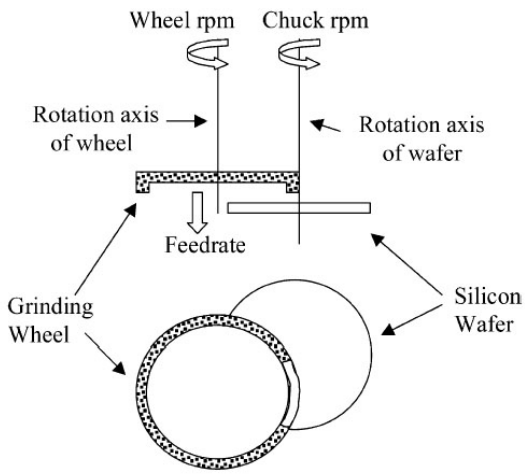


Figure 2-10 Silicon Backside Mechanical Grinding [43]

Chemical mechanical polishing (CMP), also known as chemical mechanical planarization, is currently the most commonly used planarization technique for multilayer wafer metallization for on-chip interconnections [44-46]. Figure 2-11 illustrates a schematic configuration of the CMP process. An abrasive and corrosive slurry is fed to physically grind flat the microscopic topographic features on a processed wafer, and to chemically react with the silicon, breaking silicon-silicon bonds, as shown in Figure 2-12 [47-48]. The polishing rate is affected by the chemical parameters of slurry composition, table and wafer holder rotating rate and wafer hold downward force. A surface roughness of 0.1 – 2 μm can be achieved using CMP.

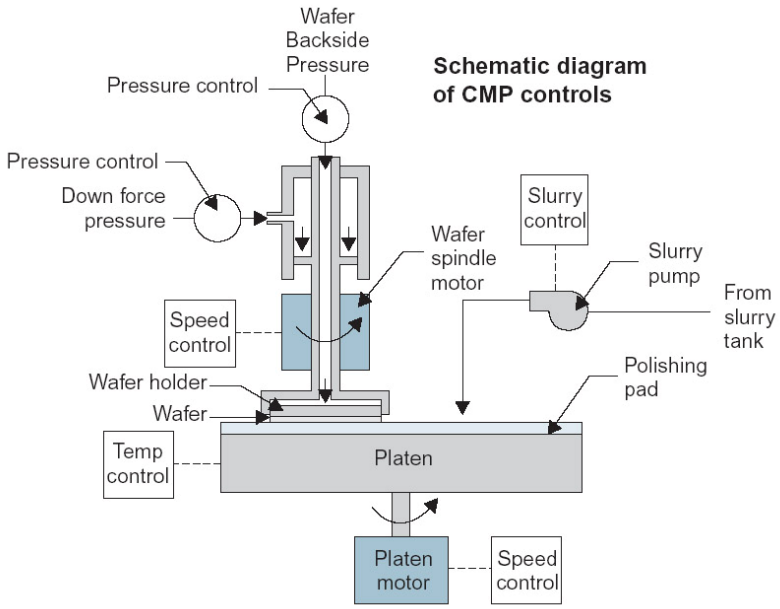


Figure 2-11 Side View of CMP Process [47]

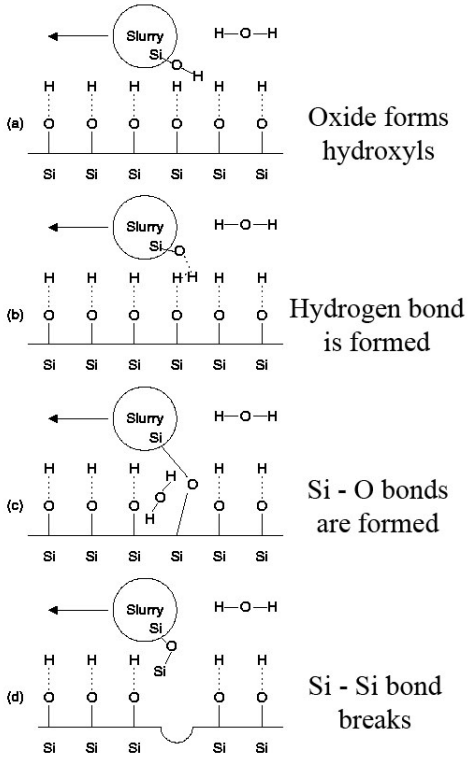


Figure 2-12 Silicon CMP Chemistry [48]

2.4 Flexible Circuit Assembly Approaches

Chip-on-flex (COF) is one of the promising assembly methods to realize high density interconnections packaging. Common COF assemblies include flip chip assembly with anisotropic conductive adhesives, stud bump bonding (SBB) flip chip assembly and solder.

2.4.1 Solder Based Flip Chip Assembly

In the solder based flip chip assembly process, flip chips are aligned and placed on the substrate pads, followed by reflow to form electrical connections. The choices for solder bumps are eutectic tin lead (SnPb), high Pb or Pb free solder. Flux is required in the flip chip assembly process and is applied by dipping the solder balls of the chip into the flux or printing the flux on the substrate to be assembled before placement. Underfill is needed to improve thermomechanical reliability of the flip chip assembly. The most popular selections for underfill are capillary and no flow (fluxing) underfill. Capillary underfilling is carried out after reflow. When no flow underfill is selected, the underfill is dispensed on the substrate to be assembled followed by placement and reflow, and is cured during reflow process. The structure of solder based flip chip assembly is illustrated in Figure 2-13.

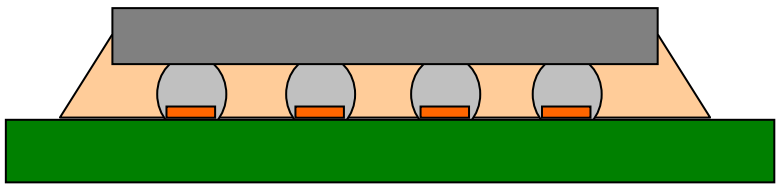


Figure 2-13 Structure of Solder Based Flip Chip Assembly

2.4.2 Anisotropic Conductive Adhesive Flip Chip Assembly

Anisotropic conductive adhesive (ACA) is also referred to as ACF, anisotropic conductive film. In ACA flip chip assembly, the film adhesive is first placed on the flexible substrate, heat and pressure is applied to bond the adhesive uniformly on the substrate. Then the flip chip is aligned and placed on the adhesive, electrical and mechanical interconnections are formed to the substrate under heat and pressure. Figure 2-14 [49] illustrates the complete ACA flip chip assembly process. The advantages of ACA flip chip assembly method include fine pitch compatibility, low temperature processing and no need for flux. The primary issue in the ACA flip chip assembly process lies in the high moisture absorption of the conductive adhesive film [50-52]. When the adhesive film absorbs moisture, it will swell and hence induce stress within the package. Moisture will also lead to corrosion and functional failure in high frequency applications [51]. Other considerations in ACA flip chip assembly include uniformity in electrical connections, contact resistance and limitation in high temperature applications.

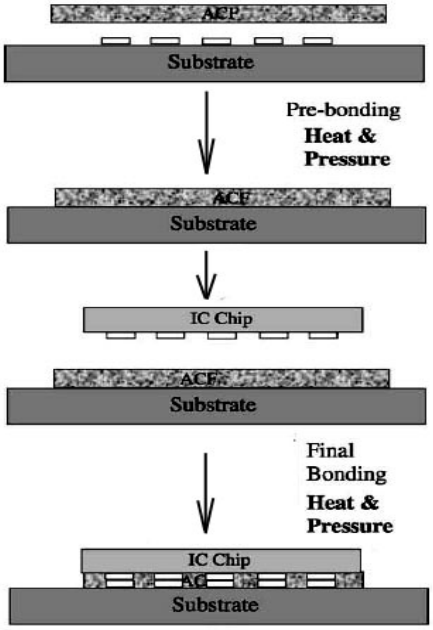


Figure 2-14 Anisotropic Conductive Adhesive Flip Chip Assembly Process

2.4.3 Stud Bump Bonding Flip Chip Assembly

Gold stud bump bonding (SBB) flip chip assembly has been used with rigid printed circuits board and it is expanding to flexible printed circuit assembly. The bonding pad is plated with wire bondable gold of at least 1 μm in thickness. Then the gold stud bumped flip chip can be thermo-compression bonded under the temperature of 300 - 350 ºC and pressure of 50 – 100 g per bump. The major applications of this assembly process are the optoelectronics and micro-electromechanical systems (MEMS) because of no flux contamination [53-55].

2.4.4 Adhesive or Solder Assisted Stud Bump Bonding Flip chip Assembly

In the adhesive assisted SBB flip chip assembly, the chip with gold stud bumps is first dipped into a layer of conductive adhesive. Then the chip is placed on the flexible

substrate, followed by underfill dispensing and curing. The cross-section of the structure is illustrated in Figure 2-15 [56]. The SBB flip chip assembly approach requires less assembly pressure than ACA assembly.

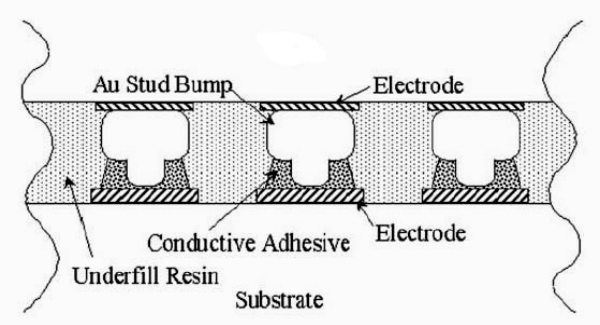


Figure 2-15 Schematics of SBB Assembly [56]

In solder paste assisted Au stud bumped flip chip assembly, a layer of solder paste is first printed on flexible substrate. Then the gold stud bumped flip chip is placed into the solder paste followed with a reflow process [57]. The cross-section of the interconnections before reflow is similar to adhesive assisted SBB assembly, as indicated in Figure 2-15, except that it is the solder paste on the metal pads instead of conductive adhesive.

Compared with gold to gold assembly, the interconnections can be obtained at lower temperature and pressure in adhesive or solder assisted stud bump bonding assembly. However, the maximum application use temperature is also lower. Besides, in the SnPb solder assisted stud bump assembly, the formation of brittle gold-tin intermetallic compounds will lead to solder joint cracks under thermal and mechanical stress [58].

2.5 Summary

Flexible printed circuits are a promising technology which have applications in many areas, including wireless communications, computer systems and medical equipments. The market for flexible printed circuits is expected to grow continuously with the demand of lighter weight, smaller size and higher packaging density.

Polyimide is the most used flexible dielectric material for flexible printed circuits in high-end applications for its good overall properties. However, the high moisture absorption and CTE of polyimide prevents it from being used in harsh environment and high frequency applications. More attention has recently been focused on LCP for its excellent combination of properties and potential applications in more advanced areas.

CHAPTER 3

FLEXIBLE PRINTED CIRCUIT FABRICATION

The use of thinned and flexible packaging and assembly processes offer a promising solution for creating light-weight and high density interconnection packaging in both consumer and military electronics. Polyimides are widely used in rigid-flexible printed circuits due to their excellent thermal and chemical stability. Liquid crystal polymers (LCPs) are another option for flexible applications that offer better dielectric performance, especially at high frequencies.

Typical construction of flexible substrate includes a base film of dielectric material with a thin metal layer on one or both sides of the dielectric film. In this study, 2 mil thick adhesiveless polyimide and LCP substrate materials were used for flexible printed circuit fabrication. Photolithography, wet etching, dry etching and surface finish processes were developed and optimized. 8 mil pitch patterns were created on both polyimide and LCP substrates, with a 5 mil width for the metal traces and a 3 – 4 mil diameter for the dielectric vias. The substrates produced were successfully utilized in solder based flip chip assemblies.

3.1 Flexible Substrate Sheet Materials

Two types of dielectric materials were used in this fabrication. One was a polyimide sheet material, Pyralux® AP 7125 E, a double-sided copper-clad film. The Cu was an

electrodeposited copper foil laminated onto the polyimide, there was no adhesive between the Cu and dielectric material. The other was double sided Cu clad liquid crystal polymer (LCP), CT. Detailed material properties are listed in Table 3-1.

Table 3-1 Polyimide and LCP Sheet Materials Properties [2, 3, 7, 10-11, 13, 19]

	Polyimide	LCP	Conditions
Dielectric Thickness, mil	2.0	2.0	-
Metal Cladding	Electro-deposited Cu	Rolled Annealed Cu	-
Metal Thickness, μm (oz/ft^2)	12 (0.3)	18 (0.5)	-
Tensile Modulus, GPa	8.5 GPa	3.9	IPC – 2.4.19
Tensile Strength, MPa	350 MPa	98	IPC – 2.4.19
In-Plane CTE ($T < T_g$), ppm/K	25	8	IPC – 2.4.41.3 (TMA 30 – 150 °C)
Solder Resistance, °C	400	288+	IPC – 2.4.13
Thermal Conductivity Coefficient, W/m-°C	-	0.5	Kemtherm QTM – D3
Melt Temperature, °C	-	Up to 350	DSC
Dielectric Constant	3.2 (1 kHz)	2.9 (1 – 10 GHz)	IPC – 2.5.5.5.1
Dissipation Factor	0.0015 (1 kHz)	0.002 (1 – 10 GHz)	IPC – 2.5.5.5.1
Surface Resistivity, ohms		3.4 E13	IPC – 2.5.17
Volume Resistivity, ohm – cm	>1E16	3.4 E15	IPC – 2.5.17
Dielectric Strength, V/mil	7200	4000	ASTM – D – 149
Chemical Resistance, Pass/Fail	Pass	Pass	IPC – 2.3.4.2
Water Absorption, %	1.8	0.04	IPC – 2.6.2 (23 °C/24 hrs)
Water Absorption Dimensional Change (CHE), ppm/% RH	9	4	60 °C
Flammability	-	VTM – 0	UL - 94

3.2 Definition of the Substrate Fabrication Process Sequence

The structure of the flexible substrate consists of dielectric material vias sitting in the center of a metal pattern exposed from the opposite side, as illustrated in Figure 3-1. To fabricate the flexible circuit substrate from double sided copper clad sheet material, the following key steps are required: copper circuitry patterning, via mask patterning, dielectric via formation, via mask removal and surface finish plating.

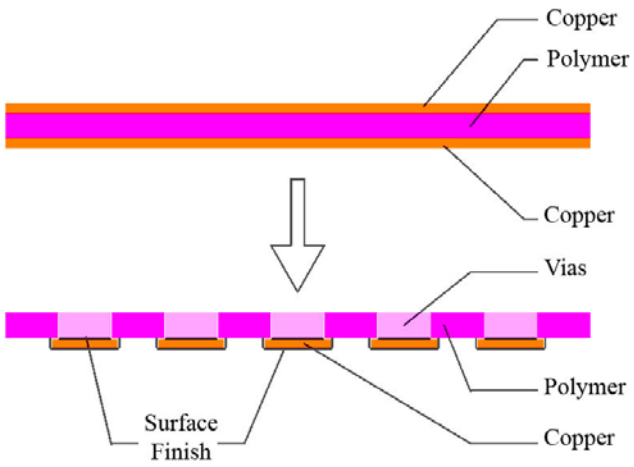


Figure 3-1 Sheet Material to Flexible Substrate Circuit

Obviously, the surface finish treatment needs to be the last step in the process in order to plate both the copper circuitry and vias simultaneously. However, there are three options for the processing sequences of via mask patterning, via formation and bottom circuitry patterning, as indicated in Figure 3-2.

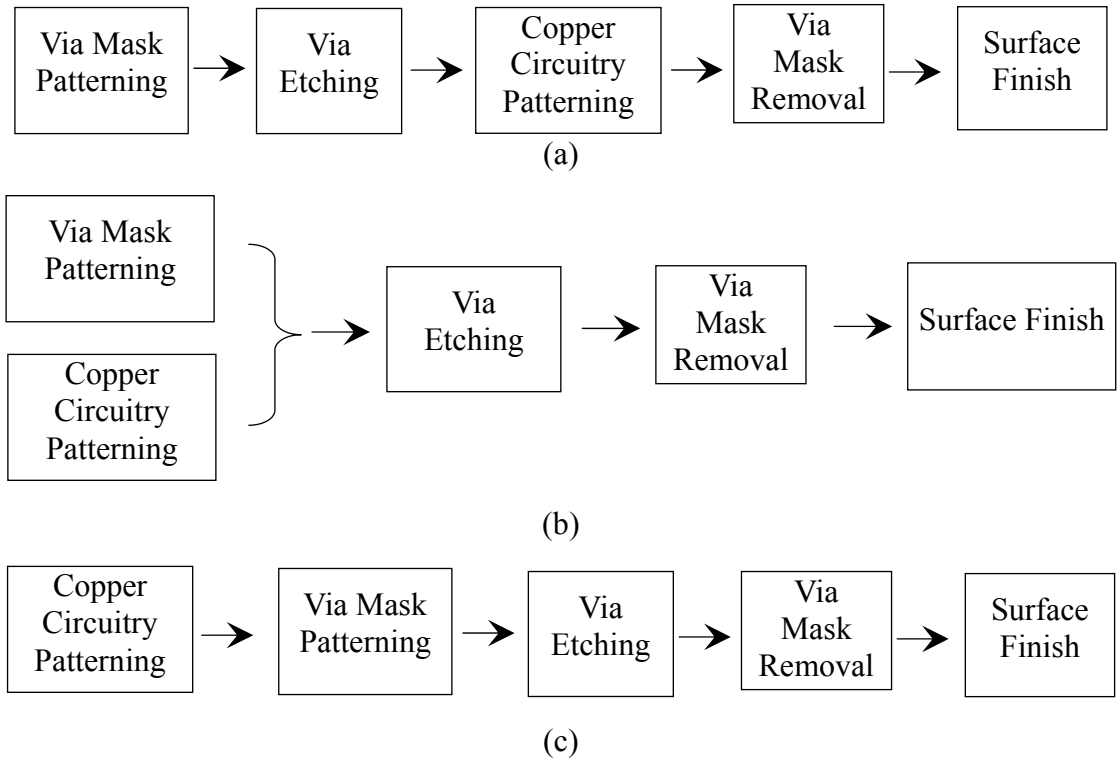


Figure 3-2 Three Possible Substrate Fabrication Process Sequences

The first option is to pattern the via mask, followed by etching the vias and then bottom side copper circuitry patterning, via mask removal and surface finish. This process looks very straight forward for structures such as flexible substrates because it builds the physical structure from top to bottom. However there are several disadvantages. First of all, the copper exposed in the vias will not be as shine as that on the bottom copper circuitry side, which will introduce difficulties when aligning the vias to the mask for the copper circuitry. In the via etching process, the flexible substrate was laminated onto a piece of silicon wafer with a layer of film adhesive attached on the copper circuitry side. Therefore, extra adhesive cleaning steps are required prior to copper circuitry patterning, which will not only introduce extra cleaning processes but also the possibility of scratching and contaminating the copper foil. Besides, via etching

is a more time consuming and a higher cost step compared with copper patterning. High value process steps should occur in the process sequence only after the lower cost steps and their associated yield loss have been successfully completed.

Since via mask etching and bottom circuitry patterning both involve copper etching, it appears possible to process them in parallel and then follow this with vias etching (option b). However, this process did not work well due to the following reasons. First, the copper area needs to be etched on the circuitry side is larger than that on the via side. According to the loading effect, the etch rate is proportional to the area to be etched. Therefore, via side copper will be over etched for the same etching time. Second, the photoresist is easily scratched during flipping and patterning the other side, which will cause defects in the copper etching.

Option C, which starts by patterning the bottom circuitry, followed by via mask patterning and etching, is the best choice for obtaining clean and accurate etched circuitry pattern.

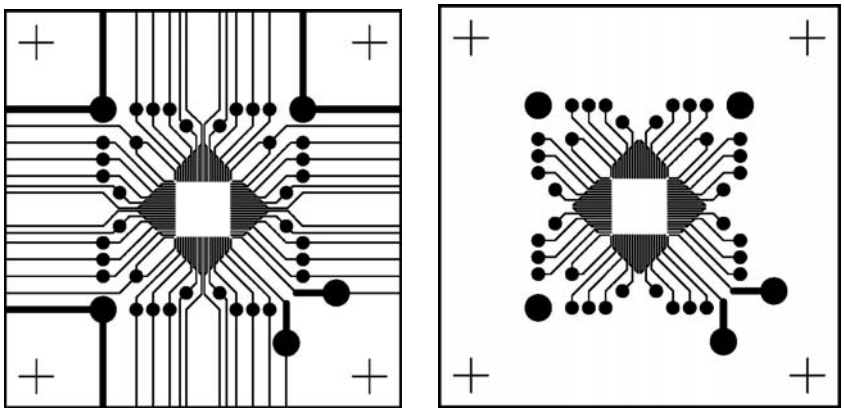
3.3 Substrate Pattern Design

The component assembled in this research was an 8 mil daisy-chained flip chip, as illustrated in Figure 3-3. A matching land pattern was designed using Lavenir (Viewmaster), a CAD software program for generating extended gerber files for circuit layouts.

Figure 3-3 Daisy-chained Flip Chip

3.3.1 Bottom Circuitry Pattern Design

Two daisy-chained land patterns were designed with Lavenir, as shown in Figure 3-4. Both patterns have probing points for each pair of interconnections within the daisy chains. Pattern (a) has all traces connected together for electroplating of the surface finish, while (b) is designed for electroless plating.



(a) Pattern for Electroplating (b) Pattern for Electroless Plating

Figure 3-4 Circuitry Pattern (Bottom Side)

3.3.2 Via Side Pattern Design

In the via side pattern design, the pattern is horizontally mirrored compared with the patterns from the circuitry side, as indicated in Figure 3-5.

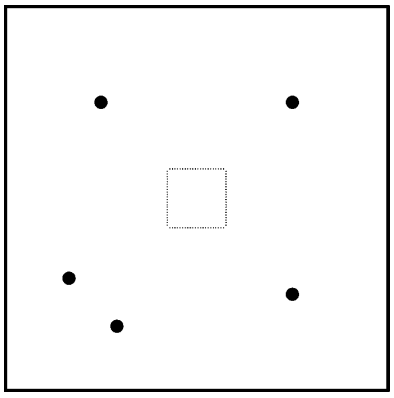


Figure 3-5 Via Side Pattern (Top Side)

3.4 Substrate Fabrication Process Development

The major process steps used in the substrate fabrication are illustrated in Figure 3-6.

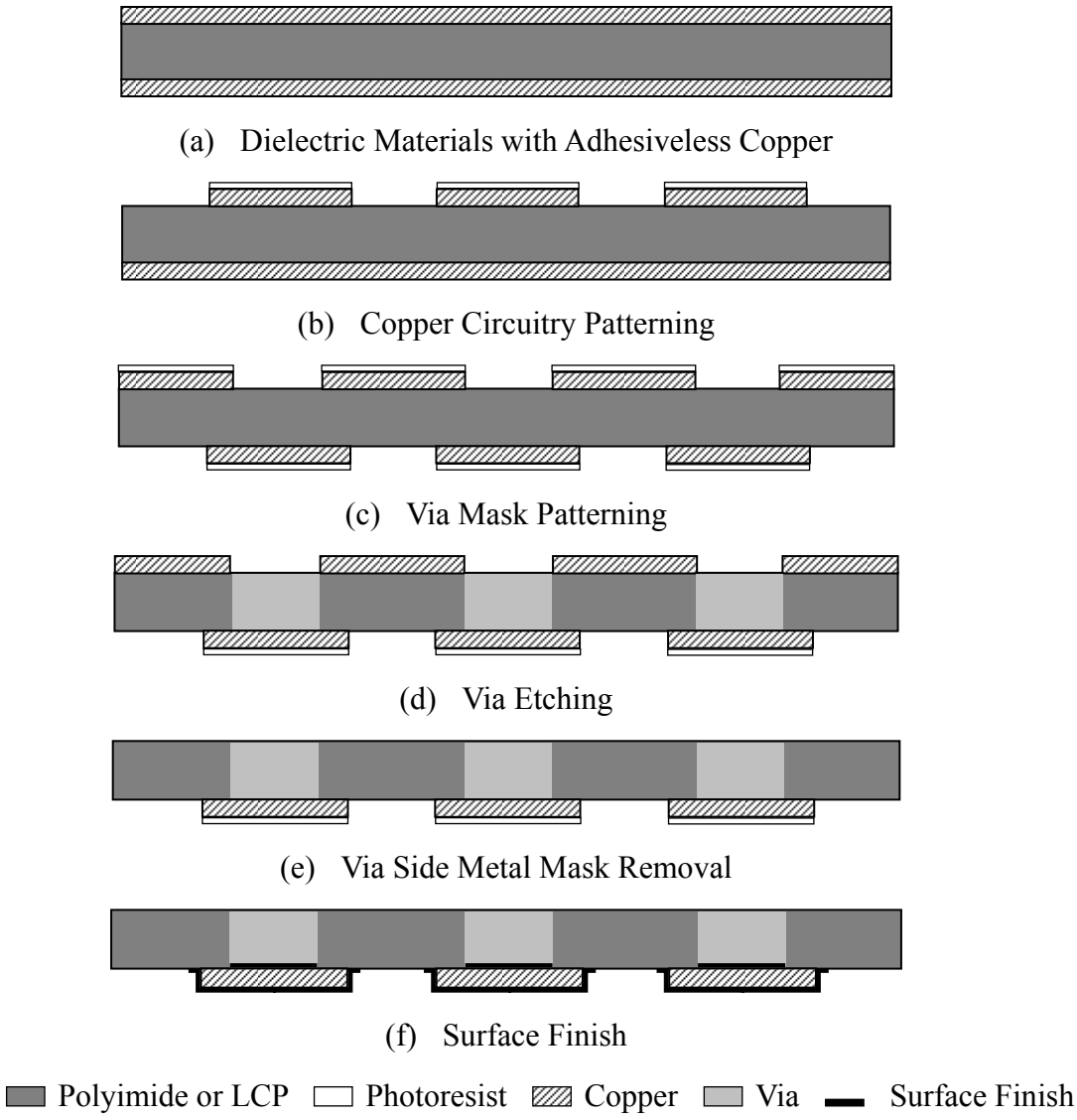


Figure 3-6 Substrate Fabrication Procedure

3.4.1 Copper Circuitry Side (Bottom Side) Patterning

Before patterning copper circuit, the flexible substrate material was taped with Kapton® tape around the edges onto a piece of 5" silicon wafer, which not only kept the

substrate material flat during the subsequent processing but also sealed the edges to prevent photoresist and etching chemistry from getting onto the copper on the backside. The following steps were used to create the copper circuitry on the flexible substrate.

Step 1 – 30 minutes vacuum dehydration bake at 125 °C, followed by 10 minutes vapor deposition of hexamethyldisilazane (HMDS). A very thin layer of copper oxide grew during the dehydration baking. Both this oxide layer and HMDS adhesion promoter provide better adhesion between the metal surface and the photoresist.

Step 2 – Photoresist spin coating. A positive photoresist, AZ® 5214 – E IR, was spin coated on the metal surface with a photoresist spinner. As indicated in Figure 3-7, when a spinning speed of 3000 rpm was used, the after-hard-bake thickness of approximate 1 μm was produced [59]. Hence, 3000 rpm was selected for the AZ® 5214 – E IR spinning speed.

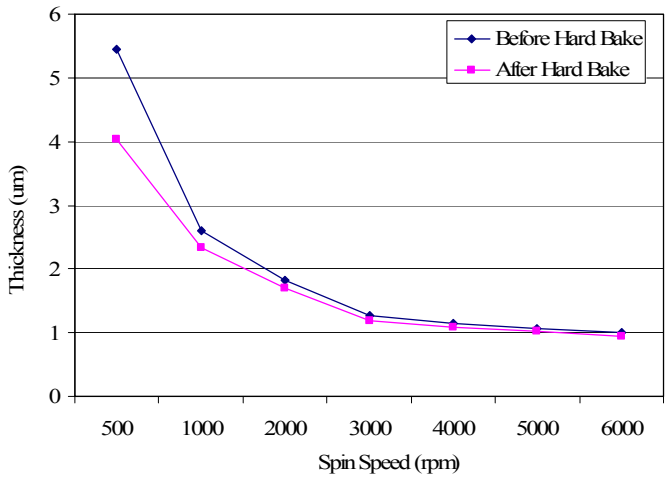


Figure 3-7 Photoresist AZ® 5214 Spin Curve [59]

Step 3 – Photoresist soft bake. After spinning, photoresist AZ® 5214 – E IR was soft baked at 105 °C for 60 seconds.

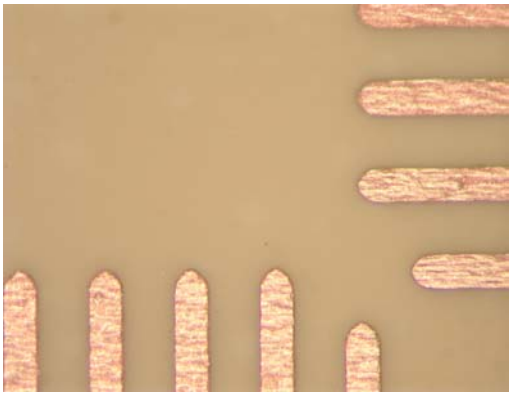
Step 4 – Photoresist UV exposure. Substrate with soft baked photoresist was exposed under UV light for 7.5 sec with a Karl Suss Mask Aligner.

Step 5 – Photoresist develop. After exposure, the substrate was soaked in diluted AZ® 400K developer (one part developer plus two parts of DI water) for 15 seconds to develop the photoresist pattern, followed with a DI water rinse and nitrogen blow dry.

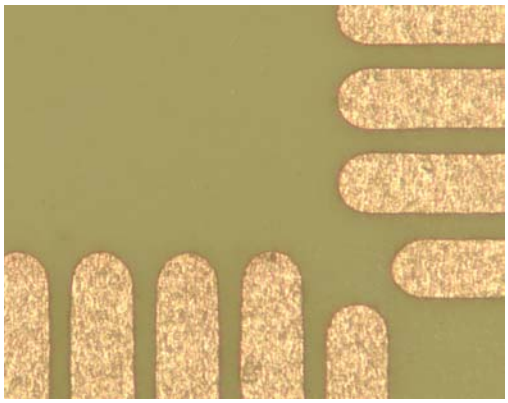
Step 6 – Patterned photoresist hard bake. The patterned photoresist was then hard baked at 120 °C for 60 sec.

Step 7 – Copper etch. Commonly used copper wet etch solutions include nitric acid, sulfuric acid/hydrogen peroxide, cupric chloride and ferric chloride. Both nitric acid and sulfuric acid/hydrogen peroxide are strong oxidizing agents and provide extremely high copper etching rate, but fail to provide fine features. The most popular etching process is controlled cupric chloride etching. An operated temperature of 49 – 54 ºC is usually used, with the effective etching speed of ½ oz copper /ft^2/min. Since the etching speed is a sensitive function of the free acid, colorimetric technology is used to control and replenish the etchant. On a lab scale this process is difficult to control.

In this study, ferric chloride was selected for copper etching since the reaction rate between copper and ferric chloride is less sensitive to the concentration of free ions, hence it is more convenient to control. Laboratory grade anhydrous ferric chloride powder was mixed with DI water at the ratio of 50 g to 150 ml. Copper etching was carried out at a solution temperature of 30 °C. Figure 3-8 shows the copper traces etched with sulfuric acid/hydrogen peroxide solution and ferric chloride solution. With the mask dimension of 7 mil, traces etched with sulfuric acid/hydrogen peroxide were 3 mil, which is narrower than the diameter of vias, while ferric chloride etched traces were 5.5 mil wide.



(a) Etchant – Sulfuric Acid/Hydrogen Peroxide



(b) Etchant – Ferric Chloride

Figure 3-8 Copper Pattern Etched with Different Chemicals

3.4.2 Via Side Copper Patterning

After patterning the circuitry side of the copper, the flex substrate was flipped over and taped with Kapton® tape on a silicon wafer. The same spin coating and soft bake processes for photoresist (steps 1 to 3 in 3.4.1) were followed. The substrate was then taken off of the silicon wafer, taped on a piece of glass and loaded into the Karl Suss Mask Aligner. Images of the copper circuit pattern on the bottom side were first taken with the microscope and then the via side copper mask was aligned to the images previously taken.

After alignment, steps 4 to 7 in 3.4.1 were repeated to pattern the copper on the via side. Figure 3-9 shows the copper via openings.

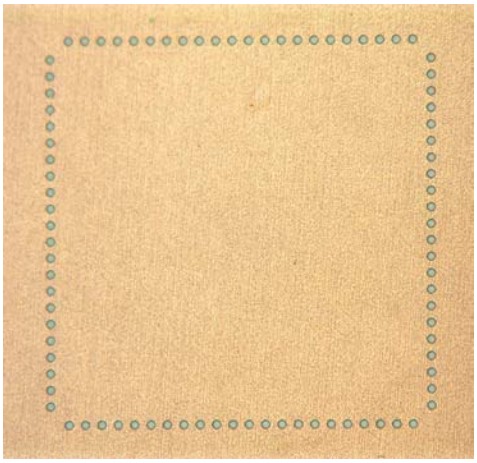


Figure 3-9 Via Side Copper Patterning

3.4.3 Dry Etch Processing of Dielectric Materials

3.4.3.1 Parallel Plate Reactive Ion Etching (RIE)

Polyimide dry etching was carried out in a parallel plate reactive ion etching (RIE) system with 14.56 MHz RF power, as illustrated in Figure 3-10 [60].

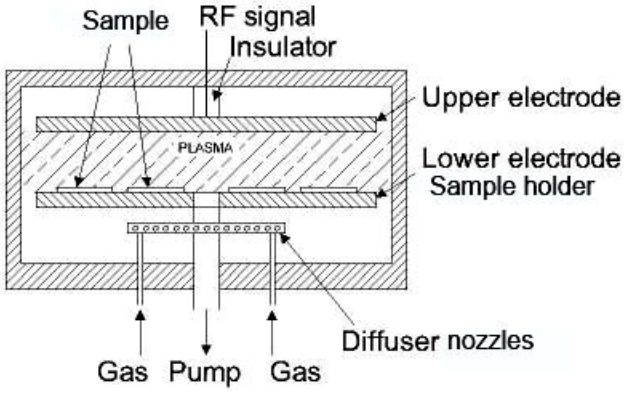


Figure 3-10 Illustration of Parallel Plate RIE System [60]

The polyimide etch rate and etched surface were examined as a function of RF power and gas chemistry and flow rate. The gas chemistries and flow rates tested were O_2 80 sccm, O_2 120 sccm and O_2 100 sccm/CF_4 8 sccm. The RF power range was from 100W to 300 W. Figure 3-11 shows the relation between etch rate and RF power for the three different gas conditions. The highest etch rate of 0.876 μm/min was obtained with O_2 120 sccm at 300 W. The etch rate increases with increasing O_2 flow and RF power.

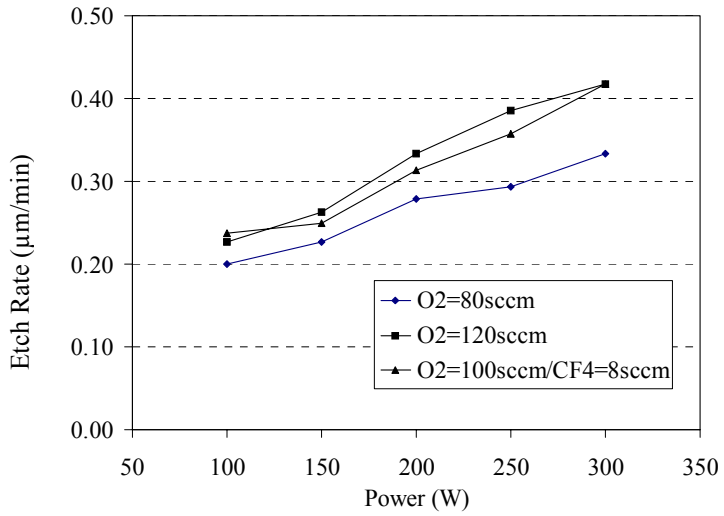
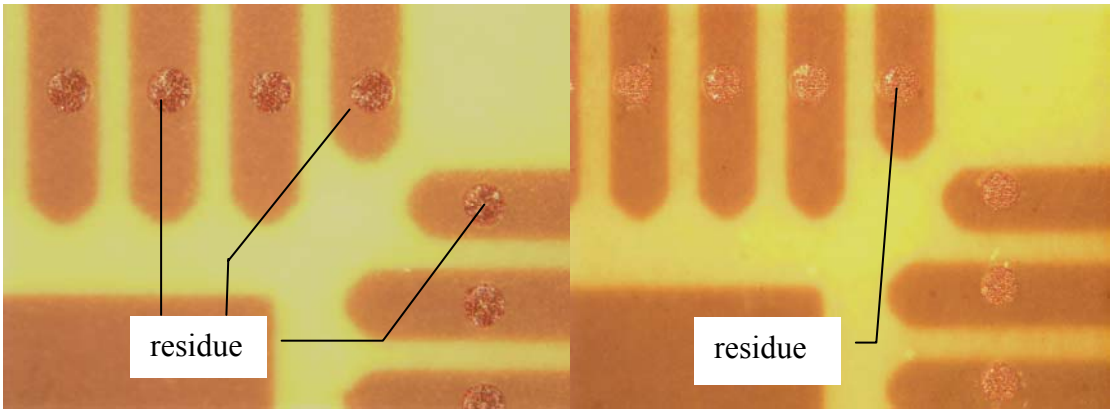


Figure 3-11 Etch Rate of Polyimide vs RF Power under Different Gas Chemistry

Changing the gas chemistry and flow rate in the RIE not only resulted in different etch rates but also affected the surface morphology. Figure 3-12 compares the etched polyimide surfaces. After pure O_2 etching, there were some white island-like residues left. There were fewer residues with O_2/CF_4 etching.



(a) O_2 Etching (b) O_2/CF_4 Etching

Figure 3-12 Vias in Polyimide after Parallel Plate Plasma Etch

The reactive ion etching for LCP was carried out in the same RIE system. Here the combination of gas used was 100 sccm of O_2 and 8 sccm of CF_4. The forward power was 350W and the reverse power was adjusted to 0. The dry etching reaction was paused every 15 minutes to cool down the aluminum plate reactor and rotate the substrate. It took around 60 minutes to etch a 2 mil thick LCP layer. The RIE was 0.8~1 μm/min. Figure 3-13 shows a cross-section of the LCP vias.

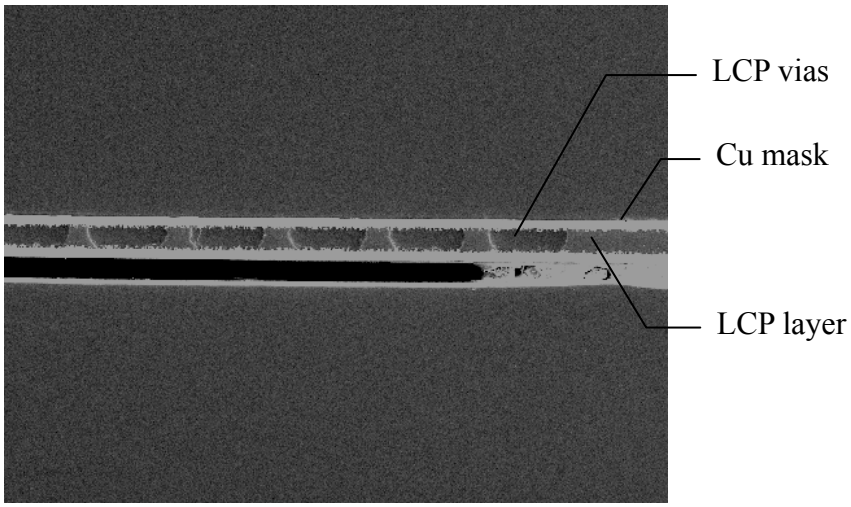


Figure 3-13 SEM Image for LCP vias

3.4.3.2 Inductively Coupled Plasma (ICP) Dry Etch

The advanced oxide etcher, AOE^{TM}, was first introduced by Surface Technology Systems (STS) in 1999. It was originally designed for SiO_2 deep etching and expanded into polymer etching.

Typically, inductively coupling of RF power (0.5-28 MHz) can produce ion densities in excess of 10^{12} cm^{-3} even at sub-millitorr pressures. An inductively coupled plasma is induced by a coil wrapped around a quartz chamber, as opposed to planar etching which occurs between two parallel electrodes, as in Figure 3-14 [61]. Low frequency or Radio Frequency cycles through the coil at its designated frequency and induces plasma formation in the quartz chamber as it couples at opposite sides of the coil [62].

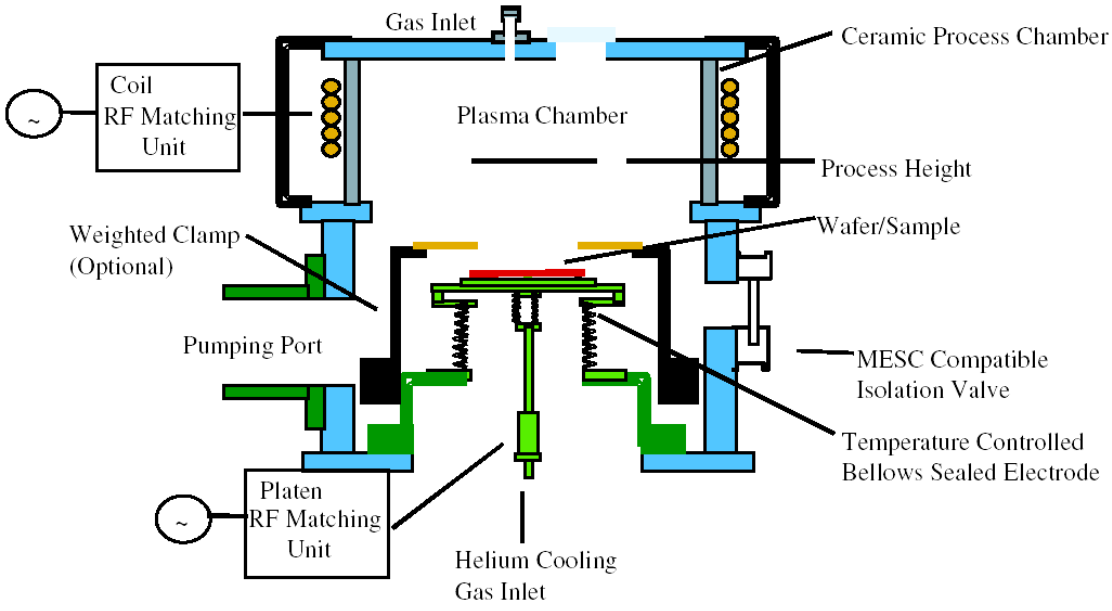


Figure 3-14 Illustration of ICP Dry Etching System [62]

Substrate materials were first mounted on a 5 inch silicon wafer with Dynatex blue adhesive. The 5 inch wafer was then loaded into the STS AOE^{TM} etcher. The process

pressure was pumped to 60 mTorr. Both the coil RF and the platen RF matching unit were activated simultaneously, with 500 W of power on the 13.56 MHz generator connected to the coil and 100 W of power on the 13.56 MHz generator connected to the platen. A gas combination of 35 sccm O_2 and 8 sccm CF_4 were used for polymer etching. The organic oxidation reaction is indicated in the following equation:

$$C_xH_y + O_2 \text{ plasma} \rightarrow CO + CO_2 + H_2O \qquad \text{Equation 3-1}$$

Compared with a parallel plate RIE system, AOE™ etched vias have more uniform dimensions and much straighter side walls, as shown in Figure 3-15 and Figure 3-16.

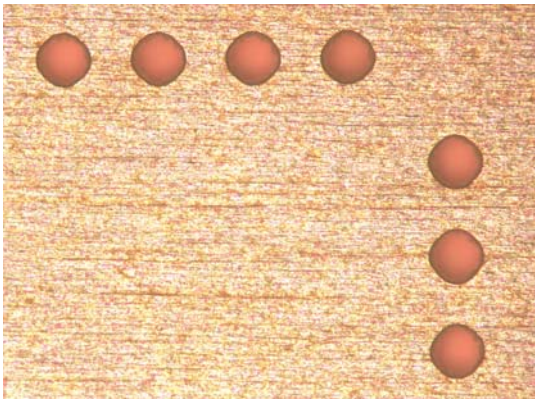
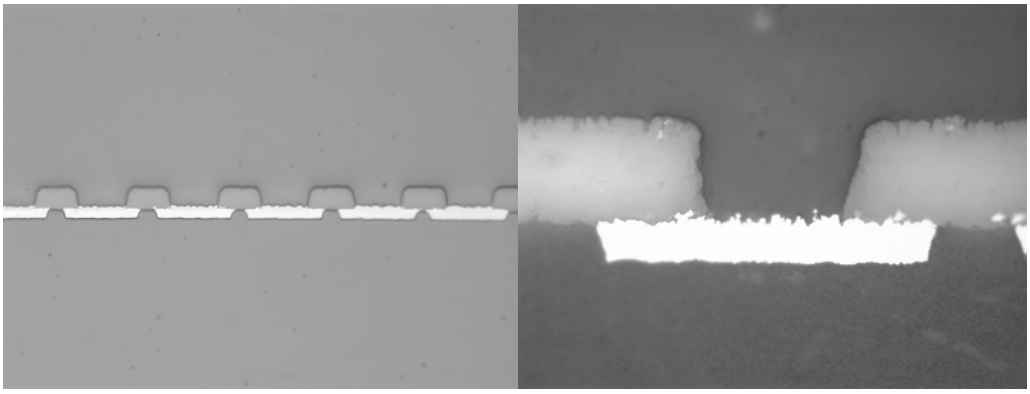
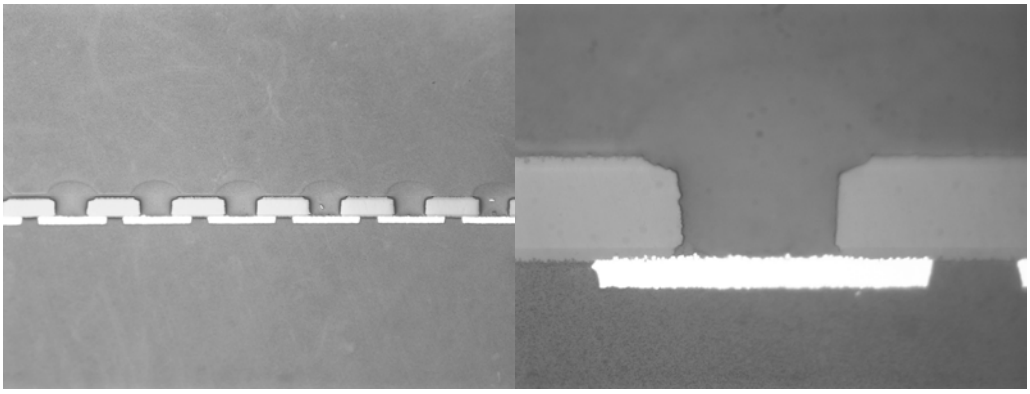


Figure 3-15 Flat Images of LCP Vias After Etching with AOE



(a) LCP Vias

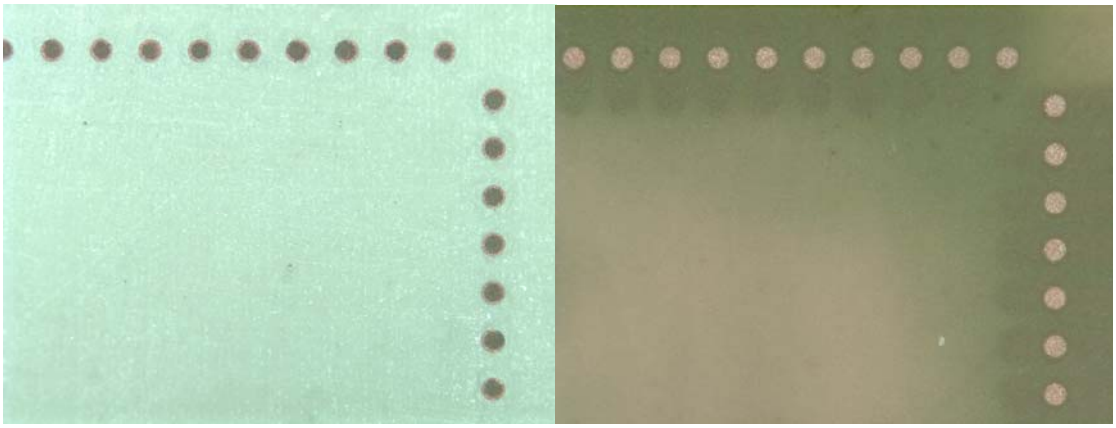


(b) Polyimide Vias

Figure 3-16 Cross-section of LCP and Polyimide Vias with AOE

3.4.4 Via Side Metal Mask Etching

To remove the metal layer on the via side, photoresist AZ® 5214 E – IR was spun and patterned again to protect the copper exposed at the bottom of the vias. The photoresist patterning process used was the same as that described in 3.4.1. After metal etching, the photoresist was cleaned with acetone. Images of the resulting vias are shown in Figure 3-17.



(a) LCP Vias (b) Polyimide Vias

Figure 3-17 Flat Images of Vias after Photoresist Cleaning

3.4.5 Surface Finish

The Ni/Au surface finish not only prevents copper from oxidation and corrosion, but also improves solder wettability. In this research, electroplating Ni/Au and electroless Ni/Immersion Au processes on the flexible substrate were examined.

3.4.5.1 Electroplating of Nickel and Gold

The final step in the substrate fabrication was plating of 4 μm of Ni and 0.5 – 0.8 μm of Au. Plating was conducted in a plating bath which was filled with electrolyte, metal and the substrate to be plated, as illustrated in Figure 3-18. The anode was connected to the positive terminal of the power supply. For Ni plating, the anode was bulk Ni and for Au plating, the anode was Platinum. The cathode was the substrate to be coated for both cases. A multimeter was used to measure the plating current.

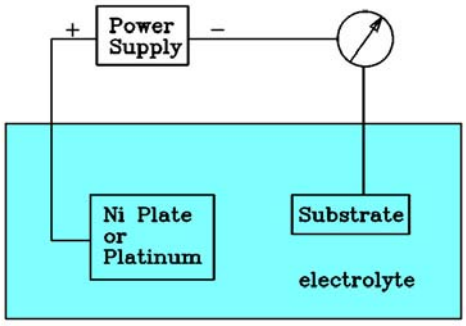


Figure 3-18 Schematic of Ni and Au Electroplating

The electroplating process was as follows.

1) Cleaning before Ni plating

Submerge the substrate into 60ºC Techni TSC 1501 soak cleaner for 2-3 minutes, then rinse with DI water to remove any light oil and handling residue from the Cu surface.

Dip the substrate into 5 vol% sulfuric acid at room temperature for 2-3 minutes, then rinse with DI water to remove the surface oxide from the Cu.

2) Wire up the plating circuit as shown in Figure 3-18.

Connect a piece of Ni plate to the positive terminal of the power supply. The nickel plating solution was mixed according to the following proportions:

Nickel sulfate 200g/L

Nickel chloride 5g/L

Boric acid 25g/L

Ferrous sulfate 8g/L

Saccharin 3g/L

3) Ni plating.

A 10 mA/cm^2 current density was chosen for Ni plating. The total plating area was 6cm^2. The plating current was calculated using the following equation,

$I = J \times A = 10\ mA/cm^2 \times 6\ cm^2 = 60\ mA$

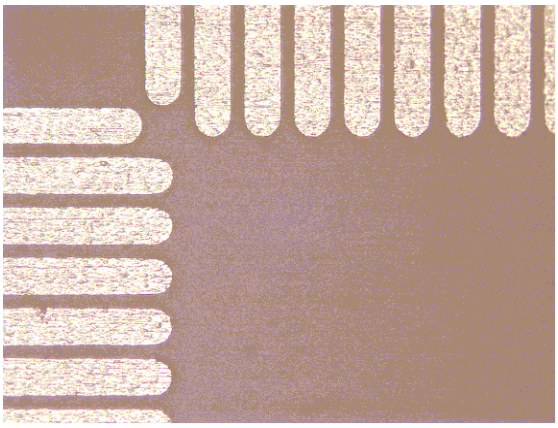
The power supply was adjusted until the current meter read 60 ± 3 mA. The total time for Ni plating was 10 minutes. The thickness of Ni was 3 to 5 μm. When finished, the substrate was rinsed with DI water.

4) Au pre-plating

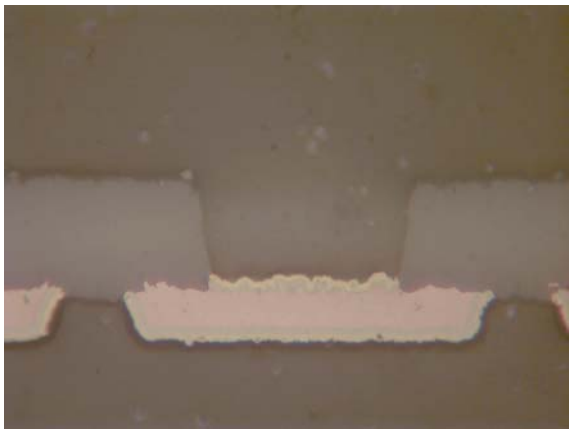
The wiring for Au pre-plating process was the same as for the Ni plating. The electrolyte was 37ºC Techni Orostrike. The positive terminal of the power supply was connected to the platinum bar in Orostrike and the plating current was adjusted to 2.0 mA. The total plating time was 2 minutes. After plating, the substrate was rinsed in DI water.

5) Au plating

The Au plating electrolyte Techni 434 HS was heated to 55 – 60 ºC. The plating current was 6.0 mA and a total plating time of 10 minutes was used. The thickness of the gold obtained was 0.5 to 0.8 μm. Figure 3-19 shows the LCP substrate with NiAu electroplating.



(a) Circuitry Side



(b) Vias

Figure 3-19 LCP Substrate with Electro Ni/Au plating

3.4.5.2 Electroless Nickel and Immersion Gold

The electroless nickel and immersion gold surface finish process was also investigated in this study. This process follows the same TSC 1501 and diluted sulfuric acid oxide cleaning process as that used in electroplating.

Direct electroless nickel plating was evaluated on the copper patterns for both polyimide and LCP. Less than 0.5 μm of nickel was deposited on the copper after soaking the substrate into the nickel plating solution for 20 minutes. To increase nickel plating, a

palladium activator was used to active the copper surface so that a complete and uniform electroless nickel could be selectively deposited to the desired thickness.

1 L of palladium activation solution was made up in the following proportions:

Techni Pd Activator Concentrate:	100 ml;
Hydrochloric Acid Electronic Grade:	170 ml;
Distilled or Deionized Water	730 ml.

Half of the final water volume was placed in a clean operating tank, then the hydrochloric acid was added, followed by the Techni Pd activator concentrate. Finally the remaining DI water was added to bring the solution to the final operating volume. Agitation was applied during the solution mixing process.

The optimum palladium activation operating range was as follows:

Palladium:	100 ± 20 ppm
Hydrochloric Acid:	175 ±25ml/l
Temperature:	25 ± 5°C
Immersion Time:	60 ± 15 secs.
Agitation:	Mild mechanical

Electroless nickel plating was carried out after palladium activation of the copper. Compared with the electroplating of nickel, electroless nickel plating is a more convenient method, not requiring electrical connections to all of the circuitry pattern. Techni En 2600 solution was used for this electroless nickel plating study. This is a medium-phosphorus electroless nickel process designed to meet most bright electroless nickel application requirements. Techni EN 2600 was supplied as 3 separate liquid concentrates. Techni EN 2600A and Techni EN 2600B were used for make-up and Techni EN 2600A and Techni EN

2600C were used for replenishment.

The electroless nickel solution was made up according to the following proportions:

Techni EN 2600A: 6% by volume

Techni EN 2600B: 15% by volume

DI water: 79% by volume (Balance)

The optimum operation range was as follows:

Nickel Metal Content: 0.75 ± 0.10 oz/gal;

Sodium Hypophosphite Content: 3.8 ± 0.6 oz/gal;

pH: 4.9 ± 0.3;

Temperature: 88 ± 5 ºC;

Plating Rate: 0.25 – 0.38 μm/min

Mechanical agitation was needed in electroless nickel plating.

To ensure optimum performance of the Techni EN 2600 process, the solution chemistry should be maintained at the optimum concentrations (0.8 oz/gal Nickel concentration, 4.0 oz/gal Sodium Hypophosphite concentration). For our study, 1 L of plating solution plated up to 40 pieces of substrate, with an average metal area of 4 cm^2 per substrate.

The pH value should be maintained in a specified range. 50% Ammonium Hydroxide solution was added to raise the pH and 25% reagent grade Sulfuric Acid solution was used to lower the pH value. All additions were slowly added to the working container with mild agitation.

Immersion gold plating followed immediately after electroless nickel plating. In this study, a non-cyanide immersion gold bath, Techni OROMERSE SO was used to

deposit up to 20 microinches of gold on the low phosphorous electroless nickel.

The solution make-up and optimum operating range is as follows:

Solution make-up (for 1 L plating solution):

OROMERSE SO (Part A):	934 ml
OROMERSE SO (Part B):	66 ml
Gold Concentration:	4.1 g/L;
pH:	8.8 – 9.0
Temperature:	70 – 73 ºC
Agitation:	Necessary for best results

At room temperature, OROMERSE SO Part A was added to the glass beaker, followed with OROMERSE SO Part B. Five minutes was allowed for the solutions to mix together. Citric acid was used to lower the pH, while 10 % sodium hydroxide was added to raise the pH value to the optimum operation range.

OROMERSE SO deposited up to 0.5 μm of gold directly on low phosphorous electroless nickel at a deposition rate of about 0.025 μm/min. To prevent the nickel from oxidizing and achieve good adhesion of the gold over the nickel film, the substrate was immediately dipped into an immersion gold plating solution after nickel plating and DI water rinsing, without the nitrogen blow dry step.

Due to nickel build up in the immersion gold plating solution, it was preferable to simply deplete the gold plating solution and start over with a new bath after plating 40 pieces of substrate with an average metal area of 4 cm^2 per substrate. Figure 3-20 shows an image of the electroless nickel and immersion gold plating obtained on an LCP.

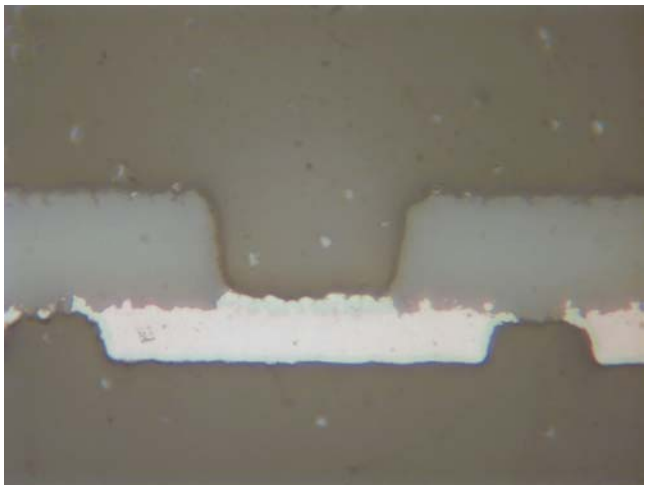


Figure 3-20 Electroless Nickel / Immersion Au on LCP

3.5 Key Issues in Substrate Fabrication

3.5.1 Lateral Etching in the Wet Etch Process

The wet etch (chemical etch) process for metal is an isotropic etching method. It almost invariably involves a certain extent of lateral etching. For our study, the substrate featured 8 mil pitch traces and 3 – 4 mil diameter dielectric material vias. As mentioned before, it is critical to land the vias accurately on the backside Cu traces. If bad alignment occurs, this will result in an opening in the dielectric next to the trace, which will allow solder flow during the flip chip assembly process. If the metal openings for the via etch increase in size and the circuit traces narrow, due to lateral etching of the copper, the same problem will occur. As shown in Figure 3-21, the white spots next to the traces show that the diameter of the metal opening for the via etch is larger than the width of the trace.

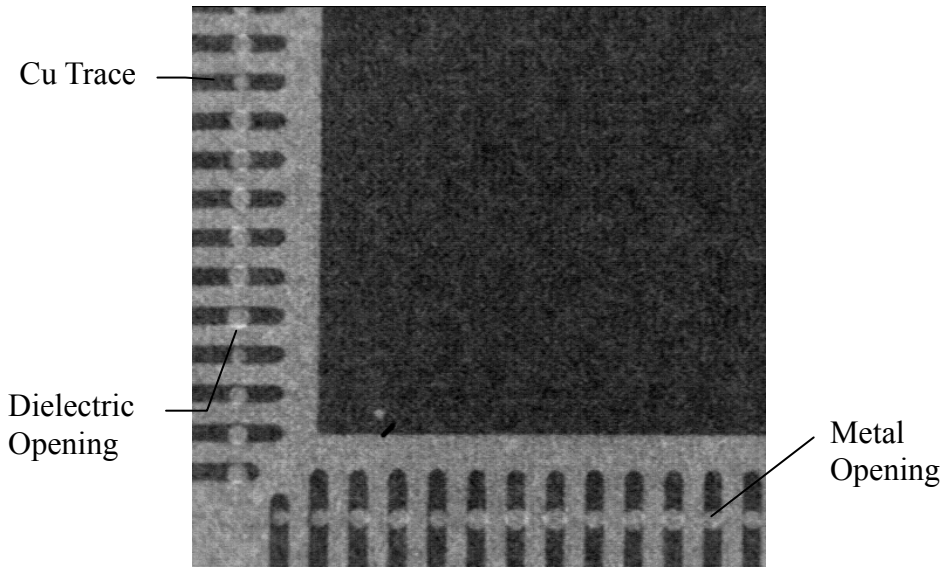


Figure 3-21 Metal Lateral Etching Results in Dielectric Opening (X-ray Image)

3.5.2 Via Side Metal Mask

In order to solve the via over etching problem, two sets of masks were designed. One featured a 2 mil mask opening, the other 3 mil. In this study, an alternative aluminum via side metal mask was also investigated. A 5000 Å thick layer of aluminum was deposited on the LCP surface by e-beam evaporation after etching the original copper foil. Steps 1 to 6, described in 3.4.1 , were repeated for the photoresist patterning. The aluminum film was etched with PAE 16-1-1-2 etchant (73% Phosphoric acid, 3.2% nitric acid, 5% acetic acid, 18.8% water). Figure 3-22 shows the via side aluminum.

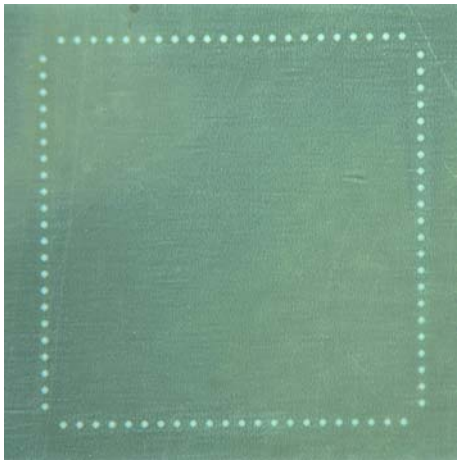


Figure 3-22 Via Side Aluminum

Patterning with the same mask can produce different metal opening dimensions and hence the polymer via dimensions, as indicated in Table 3-2. The Al mask gave results that were closer to the design value. However, it is not possible to conclude that Al performs better than Cu as the mask based on the results alone. The e-beam deposited Al had weak adhesion to the surface of the LCP. The elevated temperature during via etching caused the Al mask to peel off of the LCP. Both the Cu and Al etch masks have their advantages and disadvantages, as listed in Table 3-3.

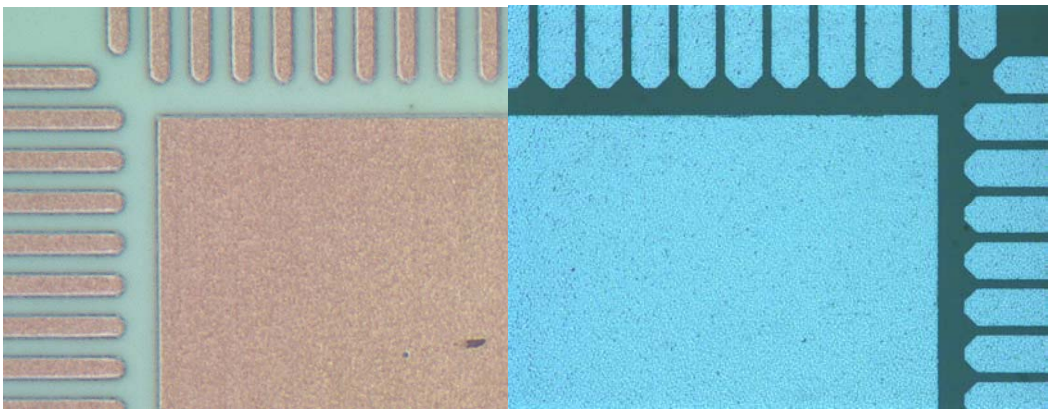
Table 3-2 Comparison of Cu and Al as the LCP RIE Mask

	Cu	Al
Metal thickness	0.5 mil	5000 Å (0.02 mil)
Metal opening using 2 mil opening mask	2.85 – 3.0 mil	2.5 - 2.65 mil
Metal opening using 3 mil opening mask	4.5 – 4.7 mil	3.6 – 3.7 mil
LCP via dimension using 2 mil opening mask	3.6 – 3.8 mil	3.1 – 3.5 mil

Table 3-3 Advantages and Disadvantages of Cu and Al Etch Masks

	Cu	Al
Advantage	Better adhesion between Cu and LCP; Size of LCP via is consistent.	Less over etching; Since Al etchant won't etch Cu, it is easier to remove Al after reactive ion etching of LCP.
Disadvantage	More over etching because of the thickness (trace designed 5.5 mil, get 4.0 mil after etching); Need to protect the bottom Cu exposed after RIE of LCP when stripping the top side metal, more steps than using Al as mask.	Due to the low adhesion between Al & LCP and the higher temperature during RIE of LCP, Al may be stripped during LCP RIE; Size of LCP via is not consistent.

From Table 3-3, the thickness of the Cu mask is 25 times that of the Al's. So the lateral etching partly results from the longer etching time for the thicker Cu. Figure 3-23 compares the trace etching results for different Cu thicknesses. The use of thicker copper will result in more lateral etching, while thinner copper could reduce the lateral etching problem.



(a) 0.5mil Thick Cu on LCP (b) 0.33mil Thick Cu on Polyimide

Figure 3-23 Thicker Cu Mask Results in More Lateral Etching

3.5.3 Electroplating Versus Electroless Plating

As previously noted, two circuitry patterns were developed in this study. Electroless plating could be used to both patterns. Electroplating could only be carried out on pattern (a) in Figure 3-4. The electroless pattern was initially favored for this study, because with the same substrate dimensions, electroless patterns can offer greater unpatterned space, which is easier to hold flat in the vacuum fixture with vacuum applied. Unfortunately, the electroless pattern could not be selected in the final substrate fabrication process since the study found there was a major issue in electroless plating. During the palladium activation step of the electroless nickel plating process, ideally, the palladium should only be deposited on copper. However, it also randomly deposited on the dielectric material depending on the roughness of the dielectric material surface, especially on LCP. One explanation is that the copper sheet is laminated on LCP at a high temperature under vacuum. When it cools down, the copper interlocks with the LCP at its surface. Wet etching the copper creates an extremely rough surface on the LCP, which allows the palladium to attach easier. The unwanted palladium deposited on the dielectric surface, which was then plated with nickel and gold, shorting the traces together, as shown in Figure 3-24. Therefore, electroplating of nickel and gold was selected for substrate surface finish plating as a result of its better process control.

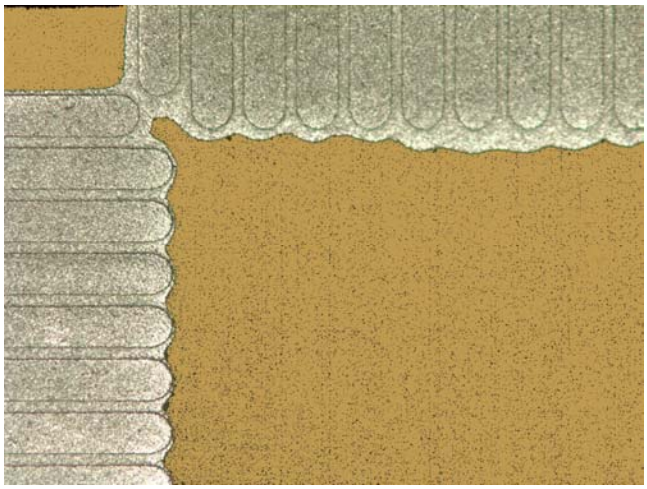


Figure 3-24 Bridging in Electroless Plating

3.6 Conclusion

In this chapter, the flexible substrate fabrication process for polyimide and LCP was discussed. Photolithography, wet etching, dry etching and surface finish processes were developed. Similar substrate fabrication processes were used to both polyimide and LCP. The properties of copper, including its thickness and the metal deposition method used are the main factors affecting the conductor trace quality, via uniformity and surface finish results. A thicker copper film results in extensive lateral etching, which affects the subsequent substrate fabrication steps and lowers the overall yield.

An oxygen plasma is the most common choice for dry etching of dielectric materials, and the addition of tetrafluoromethane (CF_4) produces vias with less residue. The O_2/CF_4 plasma etching can be carried out in either inductively coupled plasma (ICP) systems or parallel plate plasma systems. Compared with parallel plate plasmas, ICP offers much more stable control of the ion concentration. Therefore, less undercutting and straighter side walls for the dielectric materials vias can be achieved.

Finally, the electroplating of nickel and gold is a better selection for the surface finish on flexible printed circuits, especially for LCP. The plating rate can be controlled by adjusting the plating current. However, there are also disadvantages with electroplating, which include the specific design of the substrate and handling problems in the following flexible substrate assembly process.

CHAPTER 4

THINNED FLIP CHIP ASSEMBLY ON FLEXIBLE SUBSTRATES

4.1 Introduction

In this chapter, a thinned, low profile solder bumped flip chip assembly on a thin flexible substrate is discussed. This includes factor such as the materials selection, assembly process sequence development and different assembly approaches tested. Finally, an overall low profile flip chip assembly was achieved.

4.2 Thinned Flip Chip and Flexible Substrate Handling

4.2.1 Thinned Flip Chip Handling

The 8 mil pitch, 5 mm × 5 mm peripheral arrayed flip chip PB8 was thinned to 50 μm from its original thickness of 500 μm by APTEK Industries. Thin dies tend to curl, as indicated in Figure 4-1. In both the x and y directions, the curve radius ranged from 130 to 150 mm. This curvature results in uneven gaps between the solder bumps and pads on the flexible substrates, which cause non-uniform solder joint connections. A 500 μm thick silicon chip was attached to the thin die on the back side as a carrier, as shown in Figure 4-2. With the carrier, the curve radius was increased to approximate 750 mm. Therefore, the

thin die mounted on a carrier can be treated as a normal thickness die as it goes through the placement and reflow stages of the flip chip assembly process.

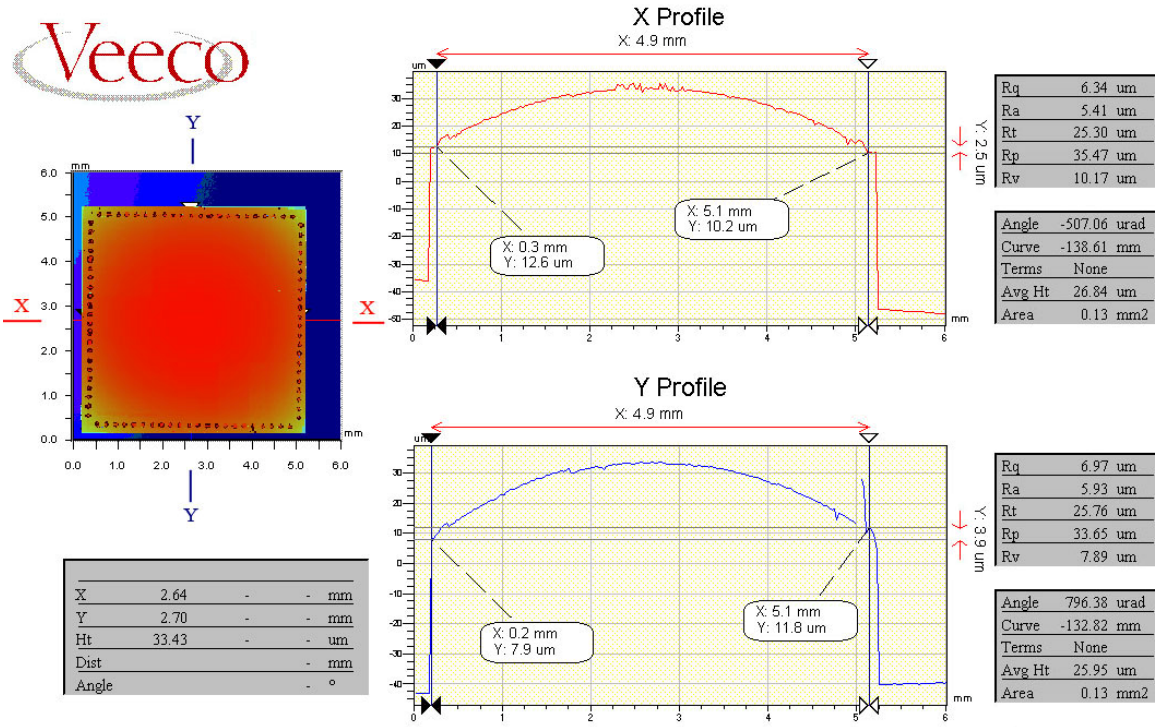


Figure 4-1 Surface Profile and Curvature for The 50 µm PB8 Die

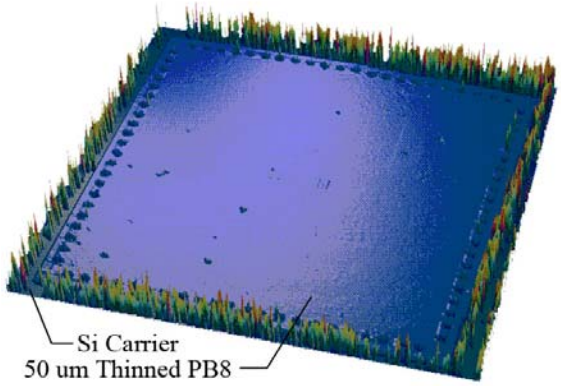
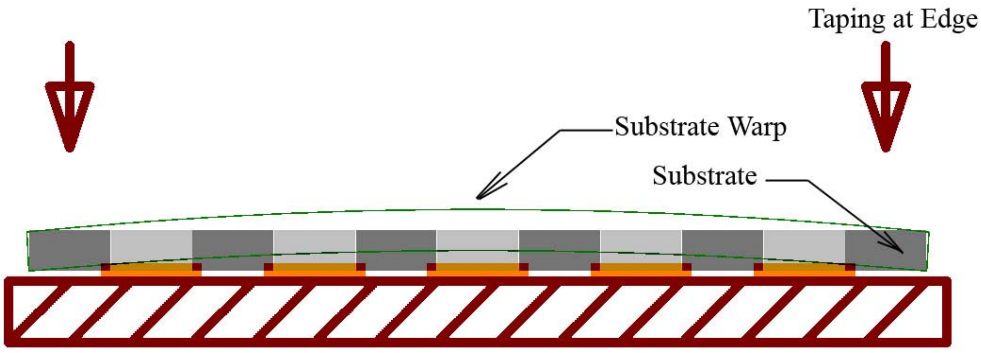


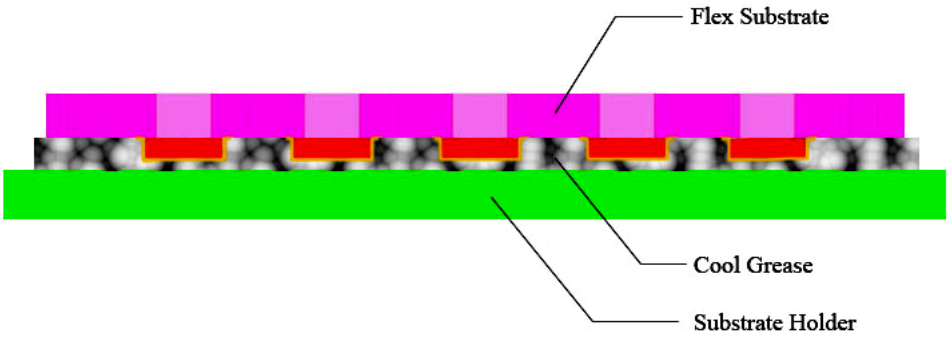
Figure 4-2 Thinned Flip Chip with Backside Carrier

4.2.2 Flexible Substrate Handling and Fixturing

As with thinned flip chips, LCP and polyimide flexible substrates of 2 mil thickness also tend to buckle. Different approaches have been investigated in order to hold these flexible substrates flat during the assembly process, which include the use of mechanical frames, taping and a grease-type adhesive, as illustrated in Figure 4-3. The first two approaches failed to flatten the center of the substrate, and although the grease adhesive method successfully held the entire substrate area flat, it introduced an additional cleaning step into the assembly process.



(a) Mechanical Framing or Taping



(b) Grease Adhesive

Figure 4-3 Flexible Substrate Fixturing Scheme

A vacuum fixture method was developed to address this problem. It consists of a piece of porous metal sitting on stainless steel which is connected to vacuum with a high temperature silicone hose, as shown in Figure 4-4. The Kapton® tape was used to mask off the vacuum not covered by the flex substrate. The substrate can be held down on the metal surface evenly when the vacuum is on, as illustrated in Figure 4-5.

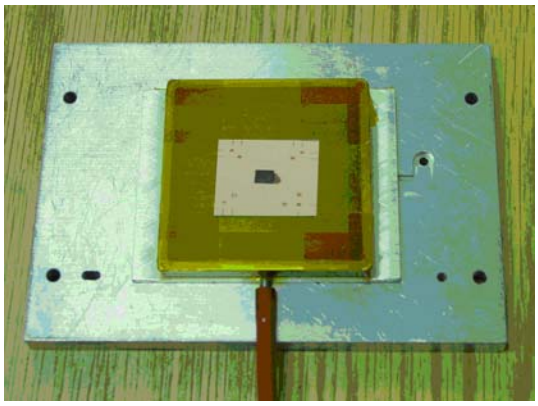


Figure 4-4 Vacuum Fixture

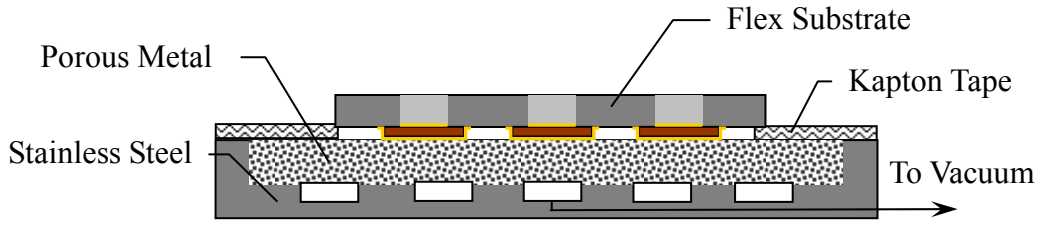


Figure 4-5 Schematic of Vacuum Fixture

4.3 Thinned Flip Chip Assembly Process

4.3.1 Flip Chip Solder Bump Formation

In flip chip bumping process, solder is usually deposited on the under bump metallurgy (UBM) on the silicon wafer bonding pads by electroplating or solder paste

printing, followed by the reflow process to form solder bumps. The solder bump height for the PB8 flip chip is normally 110 to 115 μm.

In this study, an immersion solder bumping process was developed. A flip chip PB8 wafer was purchased from Delphi Electronics with an Al/Ni/Au under bump metallurgy (UBM). After cleaning the wafer with 5:1:1 (DI water: Sulfuric Acid: Hydrogen Peroxide), water soluble flux Alpha Metal WS 619 was brushed onto the wafer. Then the wafer was dipped into molten eutectic SnPb solder of 220 ºC, as illustrated in Figure 4-6. After immersion solder bumping, PB8 wafer was cleaned with 10% DI water diluted Hydrex^{TM} AC solution at a temperature of 43 to 49 ºC for 10 minutes, followed by a DI water rinse and nitrogen blow dry to clean the flux residue. Low profile solder bumps were formed with a bump height of 13 – 15 μm, as shown in Figure 4-7.

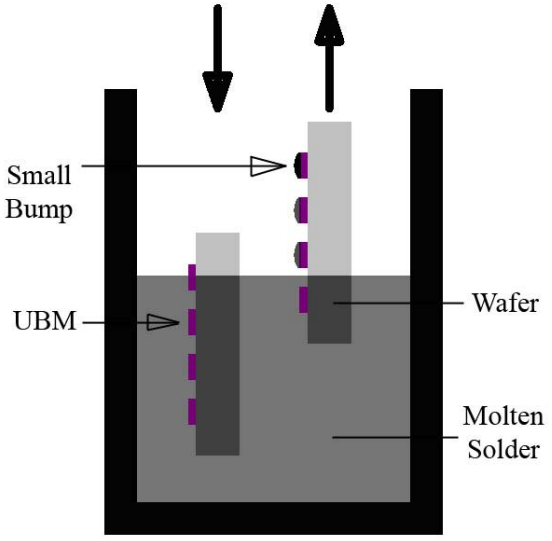
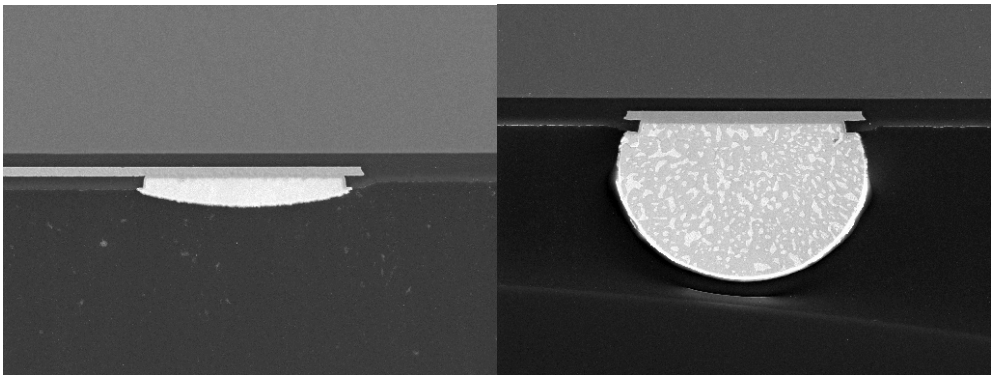


Figure 4-6 Immersion Solder Bumping

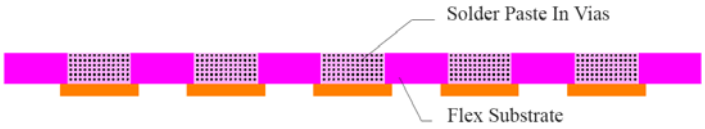


(a) Low Profile Bumps (b) Normal Solder Bumps

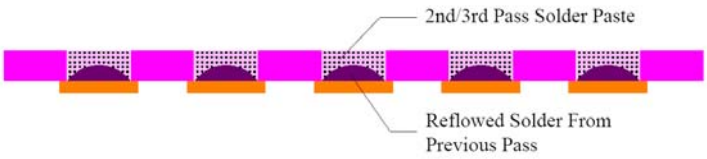
Figure 4-7 Low Profile and Normal Dimension Solder Bumps

4.3.2 SnPb Coating on Flexible Substrates

Eutectic SnPb solder paste, Aqualine 6023, was squeegeed into the flexible substrate vias followed by a 220 ºC peak temperature reflow, as illustrated in Figure 4-8. In order for the solder to reach the top of the via surface, three passes of solder paste squeegeeing and reflow were required. 10% Hydrex^{TM} AC cleaning at 43 – 49 ºC and DI water rinsing followed each reflow step.



(a) First Pass



(b) Second or Third Pass

Figure 4-8 Solder Paste Filling

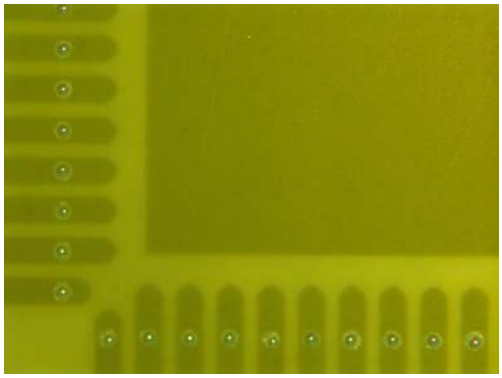
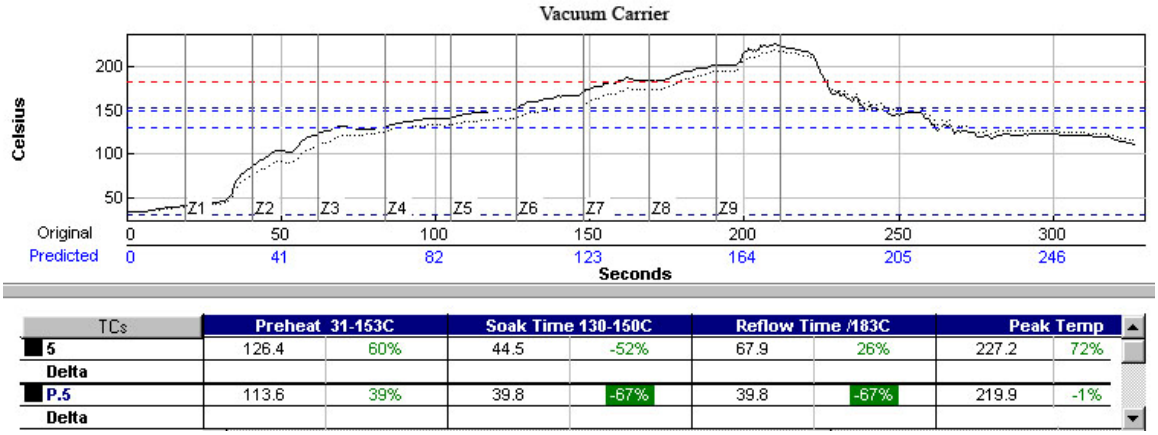


Figure 4-9 SnPb Filling in Vias

4.3.3 Normal Bump Flip Chip Assembly

The solder filled polyimide substrate was held on the vacuum fixture. The 500 μm thick normal solder bumped PB8 was dipped into a 35 μm thick film of Kester 6522 no clean flux and placed on the flexible substrate with a force of 5 N. Then the assembly was sent through the Heller 1800 reflow oven on the vacuum fixture with the silicone hose feeding through the oven. The peak reflow temperature was 220 ºC, as shown in Figure 4-10. After reflow, underfill Hysol FP 6100 was dispensed in a corner pattern and cured at 165 ºC for 30 minutes. Then the assembly was released from the fixture by turning off the vacuum. The substrate was held on the vacuum fixture during the entire assembly process, which included placement, reflow, underfill dispensing and curing. The x-ray image in Figure 4-11 shows the appearance of the solder joints after reflow. The SEM cross section in Figure 4-12 shows uniform solder joints.



TCs	Preheat 31-153C		Soak Time 130-150C		Reflow Time /183C		Peak Temp	
5	126.4	60%	44.5	-52%	67.9	26%	227.2	72%
Delta								
P.5	113.6	39%	39.8	-67%	39.8	-67%	219.9	-1%
Delta								

Figure 4-10 Reflow Profile

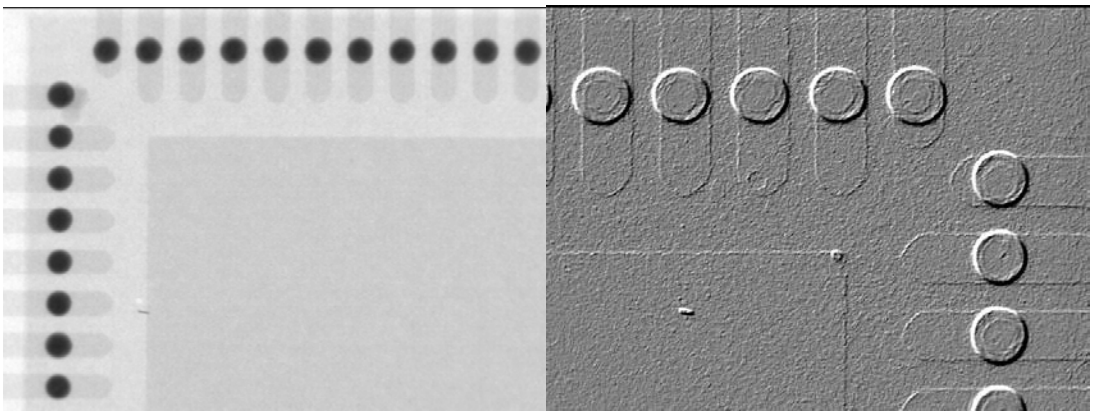


Figure 4-11 X-ray Image of Reflowed PB8 Assembly

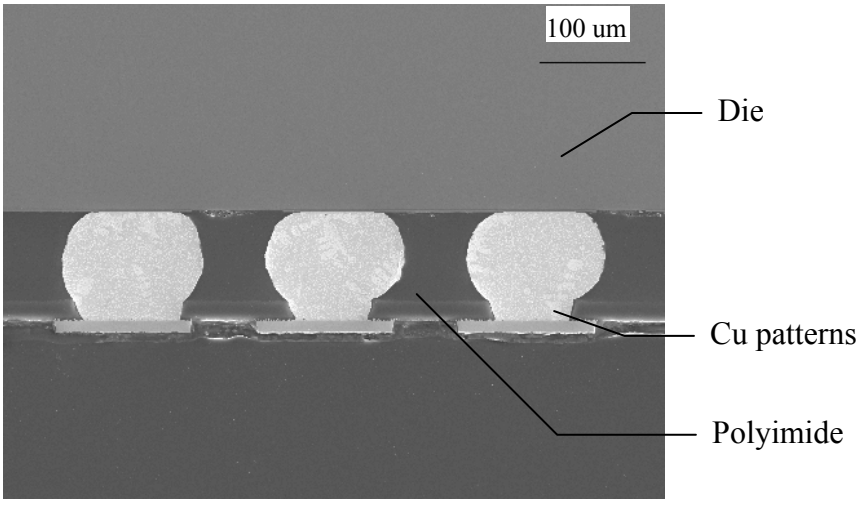


Figure 4-12 SEM Image of Solder Joints Cross-section

4.3.4 Thinned Low Profile Solder Bumped Flip Chip Assembly

For assembly, the flexible substrate was held on the vacuum fixture with the vacuum on. Kester flux TSF 6522 was brushed on the substrate, as indicated in Figure 4-13.

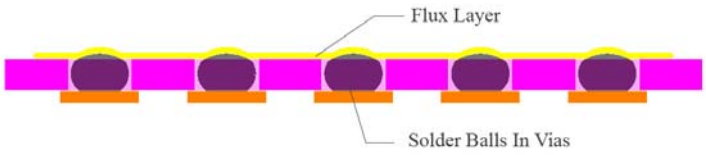


Figure 4-13 TSF 6522 Flux on Substrate

The thinned, small bumped PB8 flip chip with backside carrier was aligned and placed on the substrate with Karl Suss HP 4000 Flip Chip Bonder. The placement force was 5 N. The assembly was then reflowed in the Heller oven with a peak temperature of 220 ºC. The vacuum was on during the entire placement and reflow process. After reflow, the assembly was removed from the vacuum fixture and soaked in acetone to release the backside carrier of the thinned flip chip.

Lord Corp. underfill MTM 9086-71 was selected for use in this assembly. The underfill process has to be carried out after releasing the backside carrier since the underfill will form a fillet above the interface of the thin die and its carrier and make the subsequent release impossible. Before underfilling, the PB8 assembly was baked overnight at 125 ºC to drive out any solvent remaining from the carrier release process. An argon plasma treatment followed to enhance the underfill wetting of the substrate. The substrate was then held on the vacuum fixture with the vacuum applied. The stage on the Cam/alot dispense system was heated to 100 ºC to decrease the viscosity of the underfill during capillary flow under the die. An alternating, multiple pass underfill dispensing pattern,

with the starting and end points leading away from the die, was developed for this study and is illustrated in Figure 4-14. This dispensing approach provided a small amount of material at a time, thus allowing time for the underfill to flow beneath the thinned die instead of the underfill simply building up, which would cause the underfill to encroach onto the top of the die. After dispensing, the assembly was cured at 165 ºC for 30 minutes on the vacuum fixture. Figure 4-15 shows the cross-section of the thinned low profile solder bumped PB8 assembly after reflow and underfill.

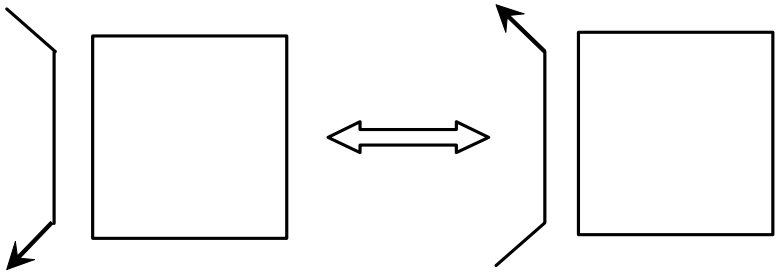


Figure 4-14 Multi-pass Underfill Dispensing Pattern

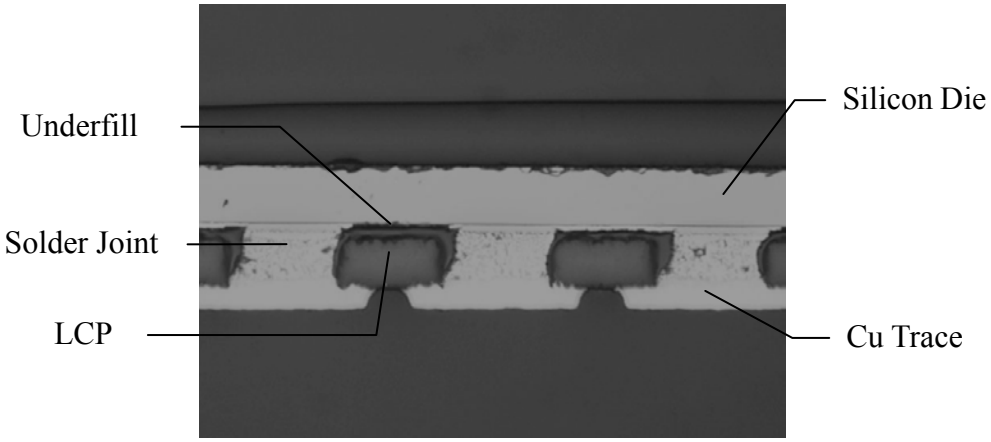
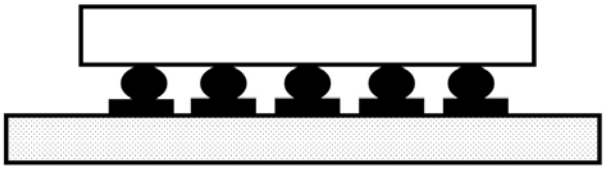


Figure 4-15 Cross-section of Thinned Low Profile Flip Chip Assembly

4.4 Thinned PB8 Flip Chip Assembly Discussion

4.4.1 Topside Versus Backside Flip Chip Assembly

The traditional flip chip assembly is a topside assembly, in which the die is assembled on the same side as the copper circuit traces are patterned (Figure 4-16 a). The topside assembly pattern can be either solder mask defined (SMD) or non solder mask defined (NSMD). In this research, an alternated assembly process was developed, as illustrated in Figure 4-16 (b). Vias were etched with reactive ion etching (RIE) in the LCP or polyimide to expose the underside of the copper pad. The PB8 flip chip was assembled from the side opposite to the copper pattern. In this type of backside assembly, the dielectric material, LCP or polyimide, serves as both the substrate material and solder mask. The advantages of backside assembly include eliminating the need for a solder mask layer and a reduction in the overall assembly thickness.



(a) Topside Flip Chip Assembly

(b) Backside Flip Chip Assembly

Figure 4-16 Topside and Backside Flip Chip Assemblies

4.4.2 The Necessity of Sn/Pb Coating in Vias

Initially, an attempt was made to assemble a normal bump PB8 flip chip directly on the flexible LCP or polyimide substrate. However, the diameter of a flip chip PB8 solder bump is 5 mils, which is larger than the flexible substrate via openings. After placement and reflow, the solder joints failed to form between the flip chip and metal pad exposed by the substrate vias, as shown in Figure 4-17.

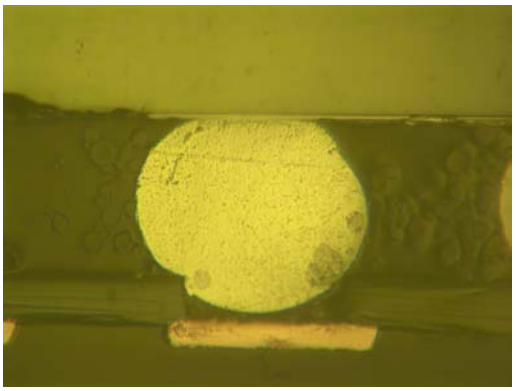
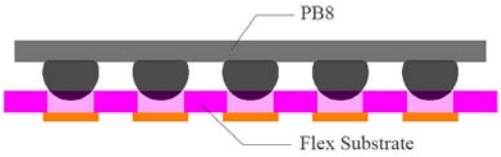
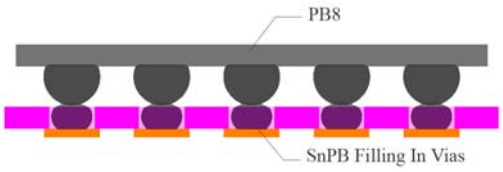


Figure 4-17 Floating Solder Bump after Reflow

With eutectic SnPb pre-coating in the flexible substrate vias, PB8 solder bumps were able to physically touch the solder coating in the via during placement and therefore formed a solder joint connection during the reflow process, as illustrated in Figure 4-18.



(a) No Coating



(b) with Coating

Figure 4-18 No Via Coating vs Via Coating During Placement

4.4.3 Comparison of Assembly with Low Profile Bumps Versus Normal Bumps

There are several advantages with using low profile solder bumps. First of all, low profile solder bumps can be obtained by fluxing and immersing the flip chip wafer into molten solder, as described previously in 4.3.1. This is a relative low cost strategy compared with eutectic solder bump electroplating or even stencil printing.

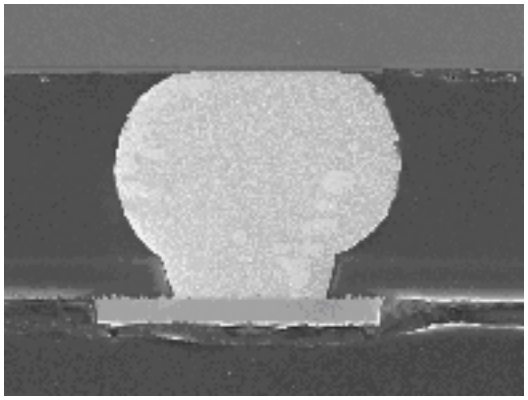
The low profile solder bumps offer a more flexible process sequence for the bumping process as it can be carried out either before or after wafer thinning. In contrast, the normal solder bumping process can only be carried out after the wafer thinning process since the large solder bumps are not compatible with current wafer mounting technology for thinning. In addition, the low profile bump flip chips are also compatible with both single die and entire wafer immersion.

Low profile solder bump assembly offers a lower overall assembly profile. The normal bump and low profile bump flip chip assembly thickness is listed in Table 4-1.

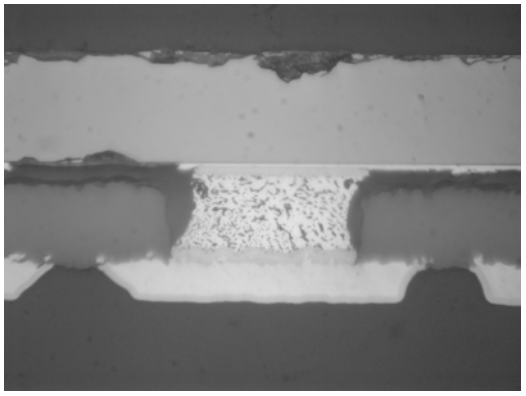
Table 4-1 Thickness for Backside Assembly

Height, μm	Normal Bump	Low Profile Bump
Solder Bump Height, μm	110 – 115	13 – 15
Die to Flex Height, μm	90 – 100	10 – 15
Total Assembly Thickness, μm	-	128 – 133

In the low profile solder bump flip chip assembly, the solder joint shape is different from that obtained using the normal solder bump assembly process. The solder joint in the low profile assembly displayed an hourglass shape, while the normal solder bump assembly had a barrel shaped solder joint, as shown in Figure 4-19. In this assembly structure, the underfill material MTM 9086-71 had the highest coefficient of thermal expansion (CTE). When the temperature decreases from the underfill cure temperature, the underfill materials contracts more than the SnPb solder, hence a compression force is applied on the solder joint. The sharp tip of the underfill at the die and underfill interface in a normal solder bump assembly has a higher tendency to initiate a crack in the solder, leading to failure of the solder joints in thermal cycling. Therefore, the hourglass is a preferred solder joint shape and the low profile solder bump assembly should have better reliability in temperature cycling applications [63].



(a) Solder Joint of Normal Solder Bump Flip Chip Assembly



(b) Solder Joint of Low Profile Solder Bump Flip Chip Assembly

Figure 4-19 Comparison of Solder Joint Shape

4.4.4 Underfill Selection

Hysol® FP 6100 was initially selected as the underfill for the low profile solder bump flip chip assembly system. This material features a low Young's modulus of 42 MPa, viscosity of 7900 cps, CTE of 94 ppm/K from 40 to 120 ºC, and a glass transition temperature, T_g of 0 ºC. Hysol® FP 6100 was selected since its low Young's modulus matched the flexibility of the thinned die and substrate. However, flexibility is not the only important criterion. The T_g of 0 ºC was a disadvantage for an assembly to be tested

over the temperature range of -40 to +125 ºC, since the material properties, including CTE and Young's Modulus undergo an abrupt change during the glass transition.

Lord Corp underfill MTM 9086-71 was then selected and investigated for use in the assembly process. Compared with Hysol FP 6100, MTM 9086-71 has a lower CTE, its relatively high T_g lies outside the testing and operating temperature range, and it has a lower viscosity. The disadvantage of MTM 9086-71 is its relatively high tensile modulus, which is less compatible with the flexibility of thinned flip chips and polyimide or LCP flex substrates.

Table 4-2 Underfill Comparison

Property	Hysol FP 6100	MTM 9086-71
Viscosity, cps @ 25 ºC Viscosity, cps @ 90 ºC	7900 -	2942 98
Filler content, % weight	-	60
Tg, ºC	0	163 (TMA result) 199 (DMA result)
Young's Modulus (< Tg), MPa	42	5000
CTE, ppm/K	94 (40 – 120 ºC)	30 (T < Tg) 101 (T>Tg)

4.5 Conclusion

In this chapter, a new ultra-thin flip chip backside assembly on a thin flexible substrate process was proposed and developed. The use of a thinned flip chip combined with a thin substrate offers very flexible complete packages, which have potential applications in many fields including low profile, foldable or wearable electronics.

Unlike the traditional flip chip assembly structure, solder joints were formed on the opposite side to the substrate circuitry. This not only eliminates the need for a solder mask, but also lowers the overall profile of the assembly, with potential applications in high density 3-D packages.

Both normal profile and low profile solder bumped flip chip assembly processes were investigated in this study. Low profile solder bumps can be formed by fluxing and immersing silicon die with UBM into molten solder. This low profile solder bumping process is compatible with current silicon thinning processes and can be carried out either on the whole wafers or on single chips.

Vias in polyimide and LCP substrates were filled and reflowed with eutectic solder paste, which helped to form the solder joint connections with low profile solder bumps. An hourglass shaped solder joint was formed in the low profile solder bump assemblies, which should offer better reliability than the more commonly found barrel shaped solder joint.

Finally, the underfill process was studied. In order to dispense the underfill beneath the die without any encroaching on the top, an alternating multi-pass dispensing pattern was developed, with the starting and ending point sweeping away from the flip chip corner. Two underfill materials were investigated in this work. Compared with Hysol FP 6100, underfill MTM 9086 -71 was selected due to its low CTE and high glass transition temperature, both of them will contribute to better reliability of the resulting chip chips assembly.

CHAPTER 5

CONCLUSION

Compared with traditional assembly, thinned flip chip assembly on flexible printed circuits offers a combination of desirable properties, such as light weight, flexibility and high density of interconnections. This ultra-thin flexible packaging and assembly process has many promising applications in both consumer and military electronics, including mobile communication systems, data storage and processing system and global position systems.

In this study, the 2 mil thick polyimide and LCP flexible print circuits for flip chip assembly were designed and fabricated. Flexible substrates were fabricated from sheet dielectric materials with double sided copper cladding. Photolithography, chemical etching, plasma dry etching and surface finish processes were developed. Vias were etched through polyimide or LCP to expose the copper pads from the backside.

Thinned PB8 flip chips were assembled on polyimide or LCP substrates with backside assembly. Solder paste was squeegeed and reflowed before assembly to ensure sufficient solder volume. The backside assembly structure not only eliminates the need to use a solder mask in the flip chip assembly process, but also lowers the overall assembly height.

An alternate immersion solder bumping strategy was realized. It is a low cost solder bumping process which can be carried out either at the flip chip wafer level or on a single die scale. Solder bumps as small as 13 – 15 μm were formed in the immersion solder

bump process, which can further lower the flip chip PB8 assembly profile.

Finally, a low CTE, high T_g underfill was selected and dispensed using an alternate multi-pass pattern that should improve the reliability of the thinned flip chip assembly on a flexible substrate that was developed in this study.

High density flexible printed circuits packaging technology has a wide range of application in data transferring, signal detection and wireless communications. Passive devices integration, high temperature application reliability and direct metal deposition on flexible printed circuits are suggested in the future work for improving fabrication yield and extend their applications.

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