Fabrication and Characterization of Compliant Off-chip Double Helix and Carbon Nanotube Interconnect

by

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Abstract

Microelectromechanical systems (MEMS) type double helix chip-level electrical interconnect structures are fabricated and characterized in this work. Due to their springlike structure, double helix interconnects have the potential to provide mechanical compliance to compensate for nonidealities, such as nonplanarity and thermal expansion mismatch between chips and substrates. A double helix configuration provides for structures with a high volumetric density of conductor for enhanced current carrying capability and lower electrical resistance. The fabrication process is compatible with wafer-level fabrication and packaging. Instead of using soldered interconnections, the double helix interconnects use pressure to make electrical connection and provide sufficiently low resistance, which is estimated to be approximately 35 ± 15 mΩ in this work. Large arrays of double helix structures have been fabricated and characterized with high yield. The mechanical and electrical models of the structures are presented. Reworkability tests were performed and the structures show a consistent resistance over 50 remating cycles. To characterize the high frequency performance, the double helix were designed and fabricated on top of coplanar waveguides (CPW) as flip-chip interconnects. The structure was characterized and simulated in High Frequency Structural Simulator (HFSS) up to 50 GHz. The measured insertion and reflection loss were less than -0.6 dB and -15 dB, respectively.

Other than using a structurally compliant interconnect, one can also use flexible material to gain compliance. A reliable solution-based process to fabricate thick carbon nanotube (CNT)

bumps has been developed and is presented in this paper. In contrast to other work of this nature, the process we have developed is capable of fabricating thick and densely packed CNT structures at room temperature with relatively high resolution and controllable film thickness or bump height. CNT structures fabricated using the developed method may find use in sensors or electrical interconnect applications. Raman spectroscopy was used to characterize the fabricated CNT bumps, verifying the CNTs are negligibly affected by the fabrication process. To study the potential application of these CNT bumps for flip-chip interconnections, we examined the deformation of the CNT bumps after flip-chip bonding and performed electrical characterization. The CNT bump interconnects display linear I-V curve with an average resistance of approximately 484 mΩ for a bump with 200 μm diameter and height of 12 μm. The solution deposited CNT interconnects have similar resistance to transferred CNT bumps grown by chemical vapor deposition. Temperature dependent measurements indicate that fluctuation-induced tunneling (FIT) is the most likely electrical conduction mechanism in the CNT bumps. The high frequency performance of the CNT bumps was also simulated in HFSS and characterized. The CNT bumps were deposited as flip chip interconnects on top of a CPW. The performance of the bumps were compared to similarly-sized gold interconnects. High frequency characterization was carried out up to 40 GHz. The return loss is below -15 dB and the insertion loss of the CNT interconnect is 0.3 dB higher than conventional gold bump interconnects per transition. Considering the negligible skin effect of CNT, they have the potential to out-perform conventional metal interconnects at higher frequency.

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List of Abbreviations

ITRS   International Technology Roadmap for Semiconductors

RC   Resistance-Capacitance

CTE   Coefficient of the Thermal Expansion

TAB   Tape Automated Bonding

C4   Controlled Collapse Chip Contact

WLP   Wafer Level Package

BEOL   Back End Of Line

PCSB   Polymer Core Solder Ball

CNT   Carbon Nanotube

SWNT   Single-Wall Carbon Nanotube

MWCT   Multi-Wall Carbon Nanotube

CVD   Chemical Vapor Deposition

MMIC   Monolithic Microwave Integrated Circuit

CPW   Coplanar Waveguide

AFM   Atomic Force Microscopy

SOLT   Short-Open-Load-Through

TDR   Time Domain Reflectometry

SDS   Sodium Dodecyl Sulfate

FIT   Fluctuation-Induced Tunneling

RBM   Radial Breathing Mode

FEA   Finite Element Analysis

LL   Luttinger Liquid

MIM   Metal-Insulator-Metal

VRH   Variable-Range Hopping

SEM   Scanning Electron Microscope

TEM   Transmission Electron Microscopy

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Chapter 1
General Introduction

1.1 Background information

According to Gordon Moore's observation of the semiconductor industry history, the transistor count, or functionality, of a chip doubles approximately every 2 years. This observation has been known as Moore's law, as shown in Figure 1.1 [1]. The Moore's law was sustained in the last four decades due to the rapid growth of semiconductor industry, which is majorly motivated by the size reduction of transistors, also known as scaling. Smaller transistors bring about lower fabrication cost per transistor, higher transistor density, faster speed and lower power consumption etc. However, as the scaling trend continues, the I/O density increases and therefore the interconnects between chip and substrate, namely off-chip interconnects, are required to have smaller pitch size. Table 1.1 shows the requirement of interconnect pitch size as the size of transistors shrinks from International Technology Roadmap for Semiconductors (ITRS) [2]. It is shown that with the decrease of device dimensions, pins and pads counts increases accordingly. In the year of 2018, the pitch size of area array flip chip pad is expected to reduce to 95 µm. This scaling trend also contributes to lower cost of the package (per pin) and higher working frequency.

Finer pitch size imposes reliability issues on off-chip interconnects, due to the lack of mechanical strength of smaller structures. Further, to reduce the RC (Resistance-Capacitance) and transmission line delay, low-K materials has been gradually adopted by the industry. In chips with low-K dielectric material, the thermo-mechanical stresses induced by the off-chip

interconnects could crack or delaminate the dielectric material causing reliability problems [3]. Therefore, off-chip interconnects that can reduce stresses are beneficial to mitigate these coefficient of the thermal expansion (CTE) mismatch caused problems. Another solution to mitigate the reliability problem is by using underfill. Epoxy-based underfills are often used in flip chip assembly to strengthen the solder joints and hence improve reliability [4]. However, the downsides of underfill process are higher cost, poor reworkability and delamination. In addition, as the pitch size of the interconnect further decreases, the difficulty of dispense underfill material drastically increases.
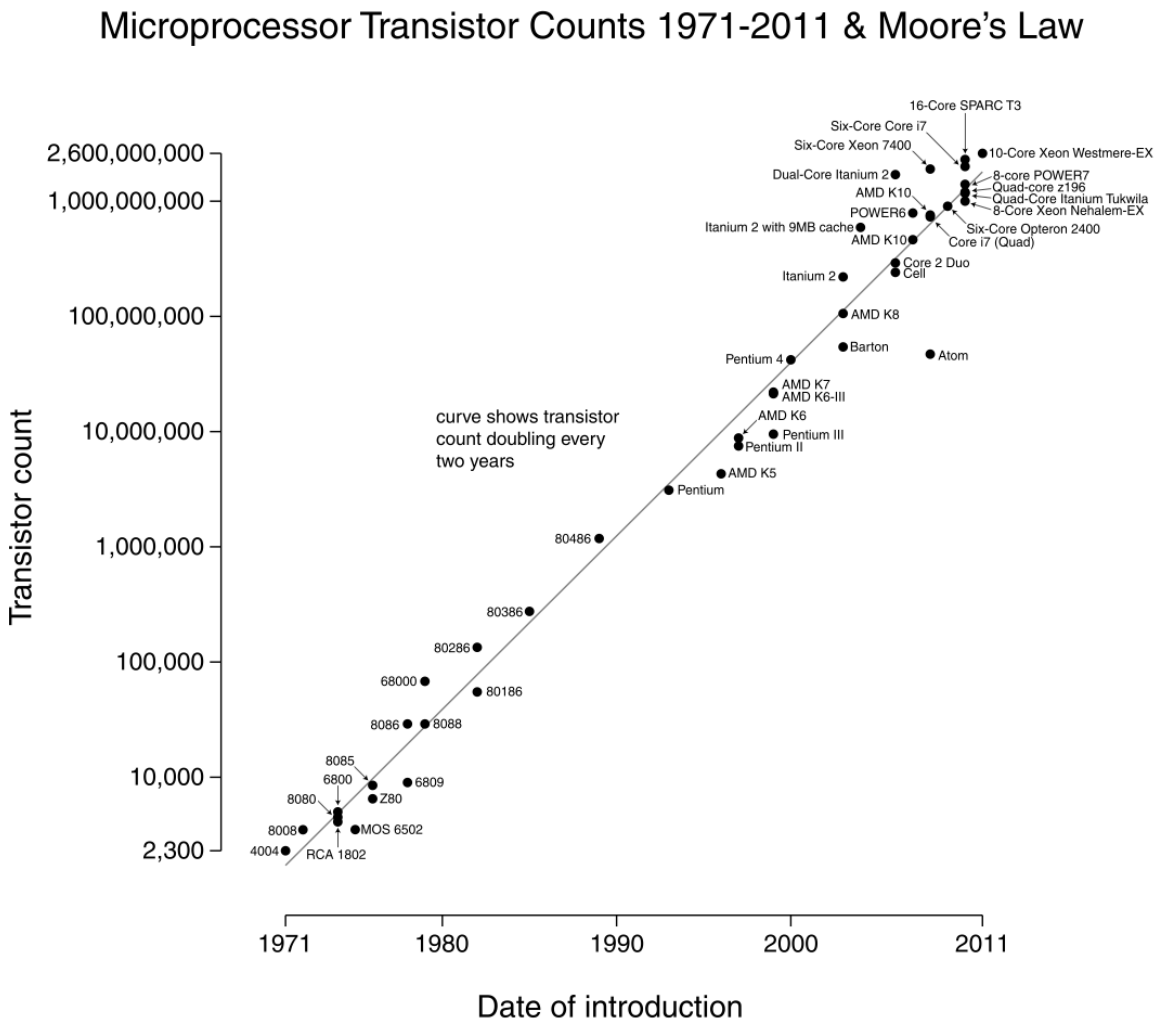
Figure 1.1. Moore's law [1].

Table 1.1. Trend and performance of packaged chip [2].

Year of Production	2013	2014	2015	2016	2017	2018
Flash ½ Pitch (nm) (un-contacted Poly)	18	17	15	14.2	13.0	11.9
DRAM ½ Pitch (nm) (contacted)	28	25	23	20.0	17.9	15.9
Number of Chip I/Os (Number of Total Chip Pads)—Maximum						
Total pads—ASIC High Performance unchanged	5,400	5,400	5,600	6,000	6,000	6,200
Signal I/O pads—ASIC high-performance (% of total pads)	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%
Power and ground pads—ASIC high-performance (% of total pads)	50.0%	50.0%	50.0%	50.0%	50.0%	50.0%
Number of Total Package Pins—Maximum						
Microprocessor/controller, cost-performance	800–3704	800–4075	880–4482	880–4930	960–5423	960–5966
Microprocessor/controller, high-performance	5616	5896	6191	6501	6826	7167
ASIC (high-performance)	5616	5896	6191	6501	6826	7167
Chip Pad Pitch (micron)						
Wedge bond	25	25	25	25	25	25
Area array flip-chip (cost-performance, high-performance)	110	100	100	100	95	95
2-row staggered-pitch (micron)	30	30	30	30	30	30
Three-tier-pitch pitch (micron)	40	40	35	35	35	35
Cost-Per-Pin						
Package cost (cents/pin) (Cost per Pin Minimum for Contract Assembly—Cost-performance)—minimum–maximum	.51–.87	.48–.83	.46–.79	.44–.75	.42–.71	.39–.68
Package cost (cents/pin) (Low-cost, hand-held and memory)—minimum–maximum	.20–.38	.20–.36	.20–.34	.20–.32	.20–.30	.20–.29
Chip Frequency (GHz)						
On-chip local clock	4.050	4.211	4.380	4.555	4.737	4.927
Maximum number wiring levels	13	13	13	13	14	14

In a broad sense, any electrically conductive path from one component to another can be considered as an electrical interconnect, no matter if the component is passive or active. The electrical interconnects in a system can be categorized into 6 levels as shown in Table 1.2. In this work, we are concerned about the level 1 interconnects, namely the off-chip interconnect connecting the chip to the first level of packaging.

Table 1.2. Electrical interconnect levels

Level 0	On-chip interconnects that connect devices, such as transistors. Usually multiple wiring levels are required to interconnect all devices.
Level 1	Off-chip interconnects that connect individual chip and the first level of packaging. The first level of packaging could be the package substrate or directly onto a board.
Level 2	Interconnect from package to board.
Level 3	Interconnect from board to board.
Level 4	Interconnect between sub-assemblies.
Level 5	Interconnect between two individual systems.

1.2 Conventional first level interconnect

For the first level interconnect, the most common technologies are wire bonding, tape automated bonding (TAB) and flip chip bonding. Wire bonding is the oldest technology but is still widely in use now. Wire bonding is a process that involves attaching a wire from one pad and then using the other end of the wire to connect to another pad, as shown in Figure 1.2. The attachment of wire to pad is usually performed using thermosonic or ultrasonic welding process. Aluminum, copper, silver and gold are some of the most common bond wire materials. Wire bonding has been used extensively in the last a few decades due to its cost-effectiveness and flexibility. As the oldest bonding technology, wire bonding also has the advantage of having a complete set of infrastructure. Wire bonding has also been known as a robust and reliable process, since the thermal-mechanical stress is distributed on the relatively long bond wire, making them suitable to connect substrate and chip with large CTE mismatch. However, the wire bonding has several disadvantages inherently. First, wire bonding is a serial process, which is not time-efficient. Additionally, wire bonding is not suitable for chips with high I/O count since full area arrays are preferred and wire bonding is not applicable for area arrays. Also, wire bonding does not meet the requirement of many high frequency applications since long and thin bond wire induces large inductance and resistance to the package.
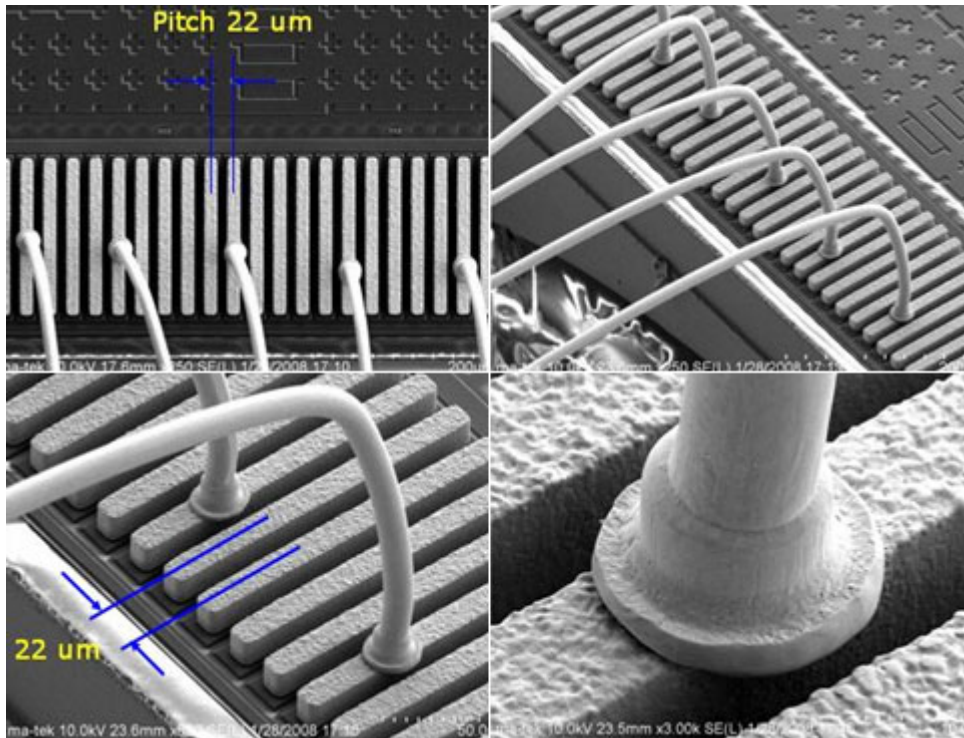
Figure 1.2. Wire bonding [5].

Tape automated bonding (TAB) process is a process that attaches metal coated polymer beam fabricated on a polymer tape, as shown in Figure 1.3. Chips are placed onto the beams and solders are applied for bonding. TAB allows gang bonding which means multiple bonds are made simultaneously, and is more time-efficient compared to wire bonding. Interconnection formed by TAB process is also robust and reliable. However, TAB process is relatively more expensive and does not support area arrays either. Further, even though the metal beam used in the TAB process is less resistive and inductive compared to bond wire, the resulted structure still has too much of inductance to be used in high frequency applications.

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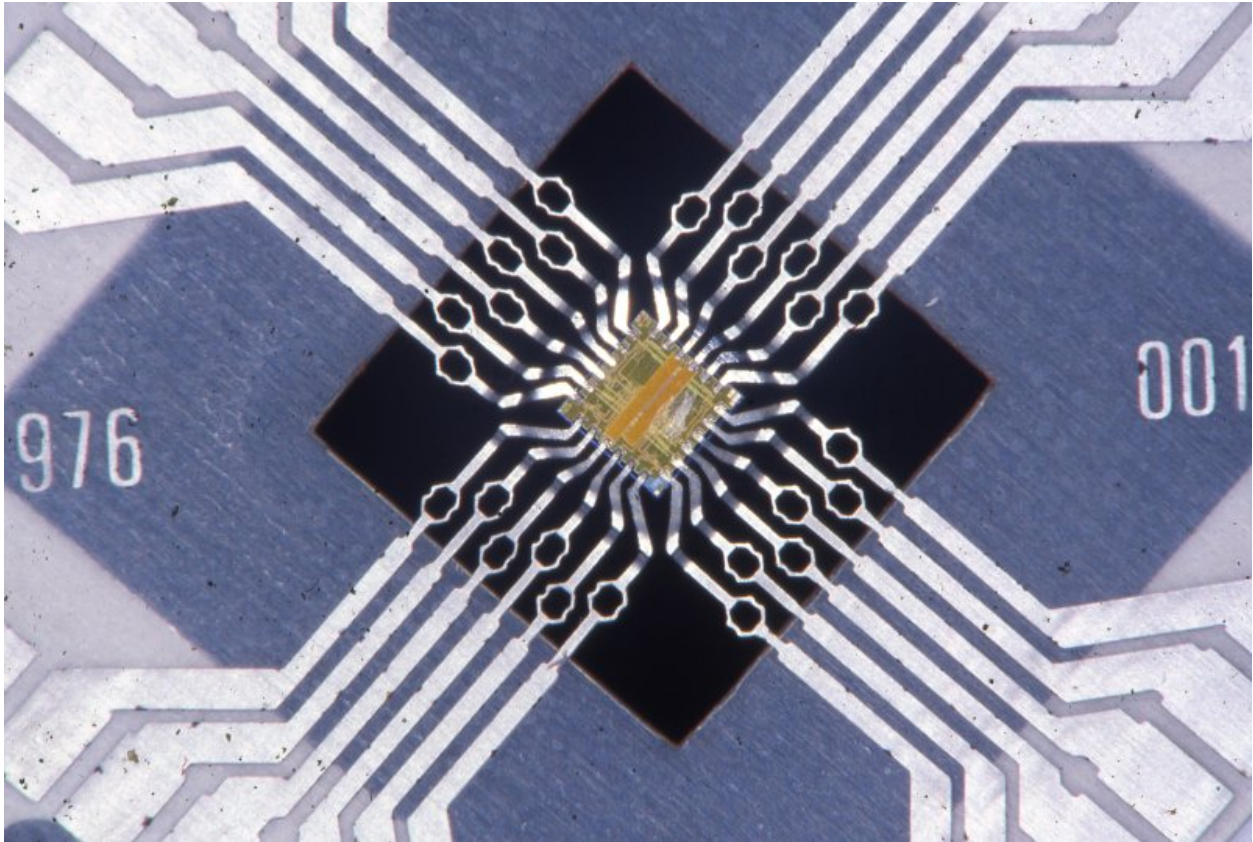
Figure 1.3. Tape automated bonding [6].

The flip chip bonding approach is gaining more popularity in recent years. The flip chip process uses C4 (controlled Collapse Chip Contact) technology. In the flip chip process, the chip is first flipped over to face down and the bonded to the substrate or board, as shown in Figure 1.4. Solder balls were applied onto the substrate or board and reflowed to form electrical connections. Flip chip has the advantage of high I/O density because it allows area array. Since the interconnects are essentially solder balls, they are short and have low inductance, which is critical for good high frequency performance. Flip chip bonding is also a cost and time efficient process. Another reason that flip chip bonding is becoming more widely accepted is because of its low profile and small footprint. However, one main issue with flip chip bonding is its

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reliability. Due to the short lead, the thermal-mechanical stress caused by CTE mismatch is very detrimental which could cause crack or delamination of the low-K dielectric material. Underfill process is necessary in flip chip process, which mitigates the reliability issue. However, some concerns about using underfill are cost, reworkability and time.
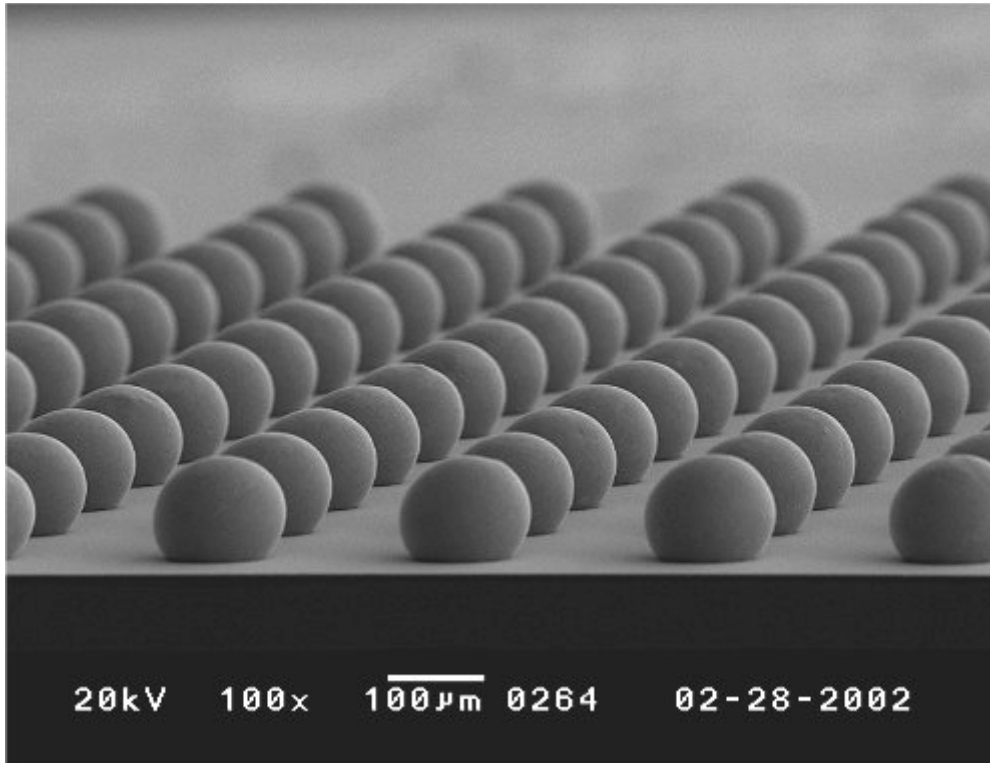
Figure 1.4. Solder ball array after reflow and ready for flip chip bonding [5].

1.3 Compliant off-chip interconnects

To mitigate the reliability issues of ball grid array interconnect, one solution is to use compliant interconnects. Compliant interconnects are mechanically compliant and flexible interconnect structures that can potentially replace flip-chip bonded solder bumps due to compensation for the CTE mismatch between the silicon chip and the organic substrate. Also, the need to use underfill can be eliminated by using compliant interconnect. In the last two decades, various compliant interconnect structures have been studied. The compliance of the interconnect is either due to the spring-like geometry of the structure or flexible nature of the used materials [7]–[18]. In this work, we research both structurally and materially compliant interconnects. Structurally, we used a double helix shaped interconnect. Materially, we adopted carbon nanotube as a compliant material to enable compliance of the interconnects.

1.3.1   Structurally compliant interconnects

One of the first versions of MEMS based compliant interconnect called MicroSpring was developed by FormFactor, as shown in Figure 1.5 [7]. Using MicroSpring as the first level interconnect, Formfactor was able to realize wafer level package (WLP). The fabrication process of MicroSpring is similar to conventional wire bonding. Starting with the attachment of one end of the bond wire to a pad, the bonding arm was programed to shape the bond wire and then cut the bond wire without attaching the other end to a pad. Since the bond wires are usually very thin, an electroplating process was followed to thicken the bond wire. The resulted compliant interconnect structures have high yield and uniformity. The resulted interconnect also passed reliability test such as thermal shock, thermal cycling, high temperature operation life and low temperature operation life test. Another possible

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application of these MicroSpring are probe cards. Due to the dependence of the fabrication process on wire bonding, the fabrication process is flexible. The limitation of the fabrication of MicroSpring is that since convention serial wire bonding process is used, the fabrication process is not time efficient when large I/O count is needed.
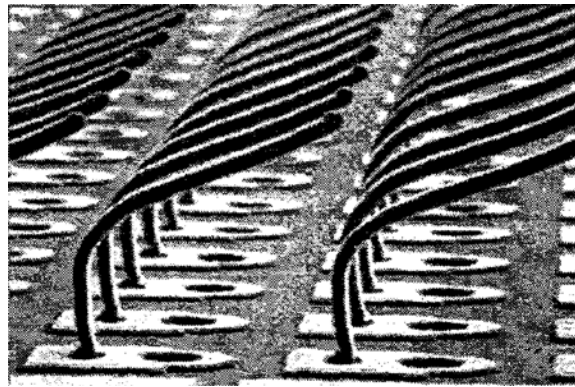
Figure 1.5. MicroSpring by FormFactor [7].

Other than using wire bonds, micro-springs can also be fabricated using conventional photolithography, sputtering and electroplating process. Using stress engineering method, the stress distributed in the metal strips can be adjusted such that one end of the metal strips stands up, and therefore the height of the micro-springs can be controlled [9], [12]–[14]. One example of the fabricated micro-spring using stress engineering is shown in Figure 1.6. The key step is the deposition of a metal layer with a large stress gradient. This is typically achieved by sputtering in changing pressure. After the stress metal layer being lithographically patterned into metal strips and subsequently released, the spring stress relaxes, lifting the tips out of the plane, forming a 3-D-compliant spring interconnect. To strengthen the metal strips, a metal electroplating process is usually preferred to thicken the

metal strips. Since the fabrication process is at low temperature, it can be integrated into the back end of line (BEOL) process. Due to the micro-fabrication based process, very high pitch size can be reached. High yield and uniformity have also been demonstrated [14].
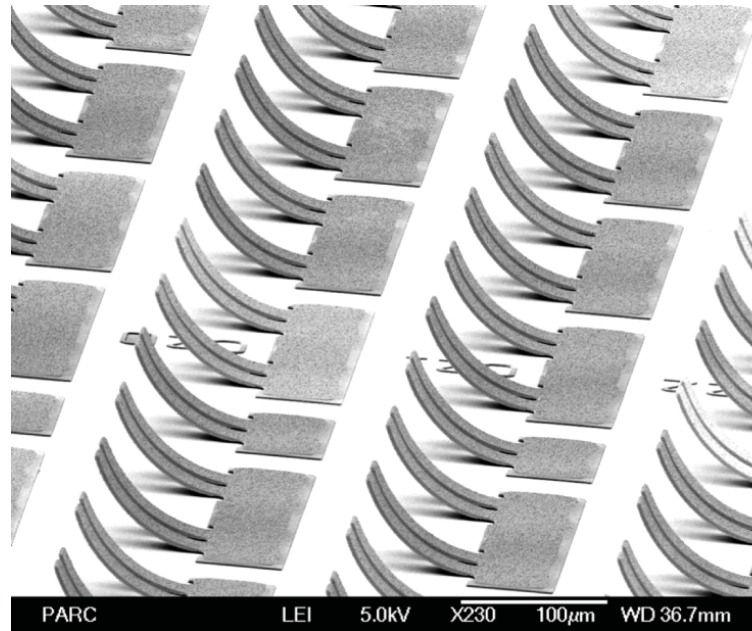
Figure 1.6. Stress engineered micro-spring structure [14].

Compliant interconnects using other geometry have also been demonstrated. FlexConnect, helix shaped interconnect and Sea-of-Leads interconnects have been researched using similar micro-fabrication method, as shown in Figure 1.7[10], [11], [15], [16]. By alternating photoresist patterning and electroplating, FlexConnect and helix type interconnect can be fabricated. Due to the adoption of micro-fabrication process, the interconnects have high uniformity, yield and pitch size. Compared to the micro-spring interconnects, these types of compliant interconnects have the advantage of lower resistance due to larger cross-section. Another advantage of the FlexConnect and helix shaped interconnects is their greater potential

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to scale down. Though the width of the micro-springs can be scaled down easily, the springs need be long enough such that they can curl to a sufficient height to provide the desired level of compliance, whereas FlexConnect and helix shaped interconnects don't have this limitation. However, the downside of FlexConnect and helix shaped interconnects is the more costly fabrication process since these structures generally require more fabrication steps and longer time.
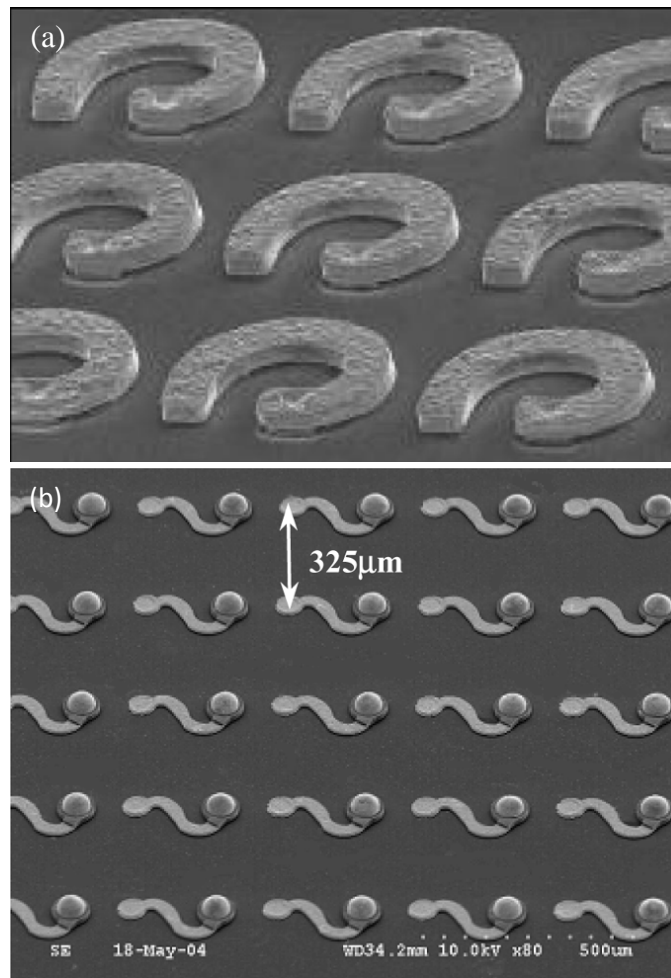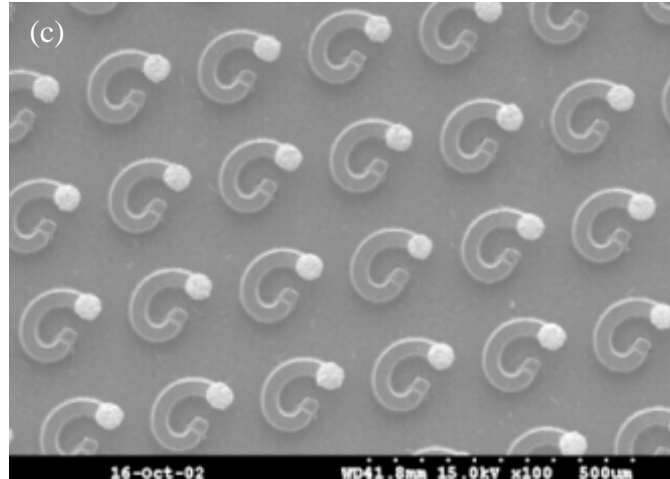
Figure 1.7. (a) Flexconnect [10]. (b) Sea-of-Leads interconnects [11]. (c) G-helix [16].

Planar microspring is another wafer-level packaging compatible compliant interconnect developed in the past a few years, as shown in Figure 1.8 [18]. A planar structure was designed to be laterally compliant. The substrate was etched such that the cavities form under the planar structures, which enable the compliant interconnects to move vertically. CMOS BEOL-compatible wafer-level fabrication process was adopted, which allows small pitch sizes. The planar microsprings were simulated up to 35 GHz to show the potential of the interconnects to be used for high frequency application without significant power loss.
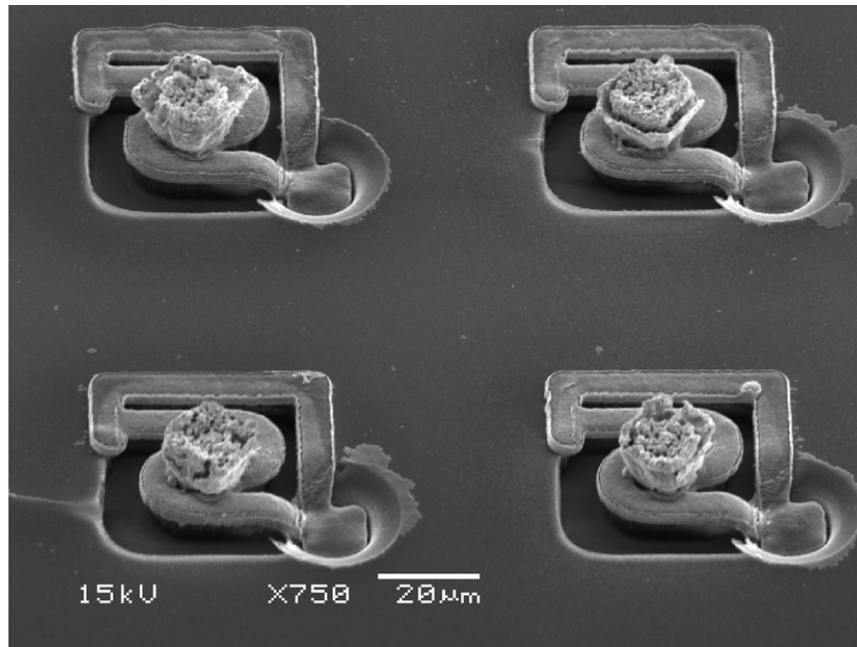
Figure 1.8. Planar microspring compliant interconnects [18].

1.3.2 Materially compliant interconnects

Another category of compliant interconnects takes advantage of materials with good compliance and flexibility. These materials can be electrically conductive or insulating. For the insulating flexible materials, metallic coatings are typically applied to enable electrical conduction.

One of the typical materially compliant interconnects is a variation from the Sea-of-Leads interconnects developed in the same group from Georgia Institute of Technology, which is named Sea of Polymer Pillars [17]. Instead of using a compliant mechanical structure, compliant polymeric material is used to enable compliance. Sea of Polymer Pillars is shown in Figure 1.9. In addition to lateral compliance which minimizes the stresses on the die's low-k dielectric, Sea of Polymer Pillars allows both electrical and optical signal transmission. This dual-mode technology can mitigate some of the performance insufficiency of electrical interconnections, especially bandwidth. The reliability test shows that the polymer pillars maintain good optical alignment between the chip and the board during thermal cycling. The fabrication process of these polymer pillars includes performing photolithography on a negative tone photoresist (Avatrel 2000P), which is followed by a metal coating step. This wafer-level compatible process allows for high pitch and aspect ratio pillars and high level of electrical and optical I/O interconnect process integration. Some challenges for the Sea of Polymer Pillars include adhesion issues between the pillar and substrate and high electrical resistance due to contact resistant and thin layer of metal coating on the polymer pillars.
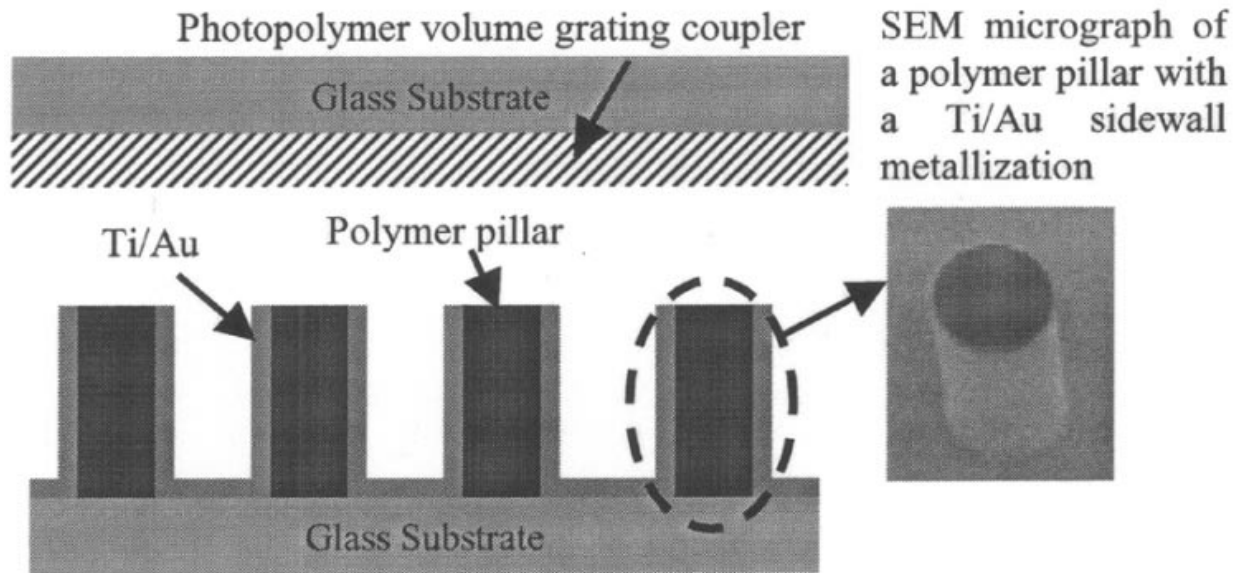
Figure 1.9. Sea of Polymer Pillars interconnects [17].

A wafer level packaging technology named ELASTec also uses resilient polymeric materials for compliant interconnects, as shown in Figure 1.10 [19], [20]. Compliant materials were applied under the metal interconnects, which allows an increase in reliability. Excessive strain caused by the CTE mismatch between the organic substrate and silicon chip can be mitigated because of the compliant polymeric under metal material. An additional advantage of using this contact scheme is that wafer probing is made easier due to the elastic contact system. The ELASTec interconnects have been fabricated and their reliability has been tested. For the 0.2 mm tall interconnects, a Weibull fatigue life of more than 6000 cycles was determined despite the high CTE mismatch between the FR-4 organic substrate and silicon chips. This is significantly better than conventional solder ball interconnects. One of the limitations to this ELASTec technology is the difficulty to scale down to smaller pitch sizes. The under metal material used in this case is printed silicone. Scaling down the silicone

domes laterally while maintaining their standoff height can be challenging.
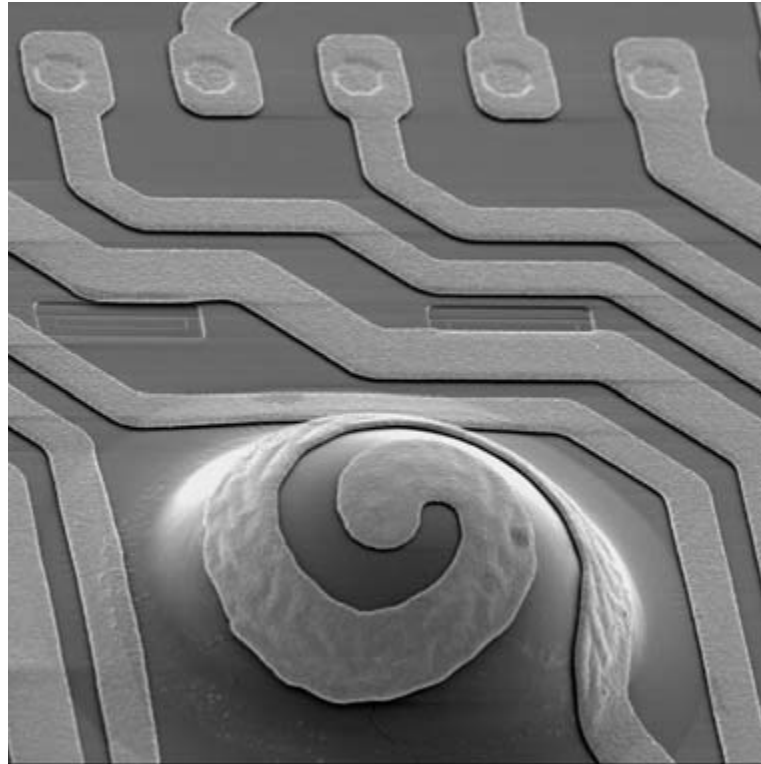
Figure 1.10. ELASTec compliant interconnects [19].

Sea of Polymer Pillars interconnects use micro-fabricated metal coated polymer pillars. A different strategy is to use ready-made metal coated polymer balls and place them onto desired locations [21]. Since the Young's modulus of these polymer core solder balls (PCSB) is much smaller than that of metal, they are more ready to relax the thermal caused strain. The PCSBs are shown in Figure 1.11. These PCSBs are fabricated by electroless plating followed by electroplating onto polymer cores. The fabrication process of these PCSB needs to be well-controlled such that uniform ball size is ensured. The test results show that the use of these compliant balls significantly enhances interconnects reliability, compared to conventional

solder balls without underfill. Full-wave electromagnetic analysis was performed, showing that these PCSB interconnect have excellent RF performance in the LTCC/BGA package up to millimeter-wave frequencies [22]. The downside of these PCSB interconnects is the slight increase of thermal and electrical resistance due to the insulating nature of the polymer cores. A 5% and an 8% increase in thermal resistance was measured for a carrier array ball grid array (CABGA) package and a plastic ball grid array (PBGA) package, respectively, compared to conventional eutectic solder balls [23]. Despite the slight increase of resistance, this PCSB interconnects are still a viable solution for applications that requires high reliability and small pitch size.
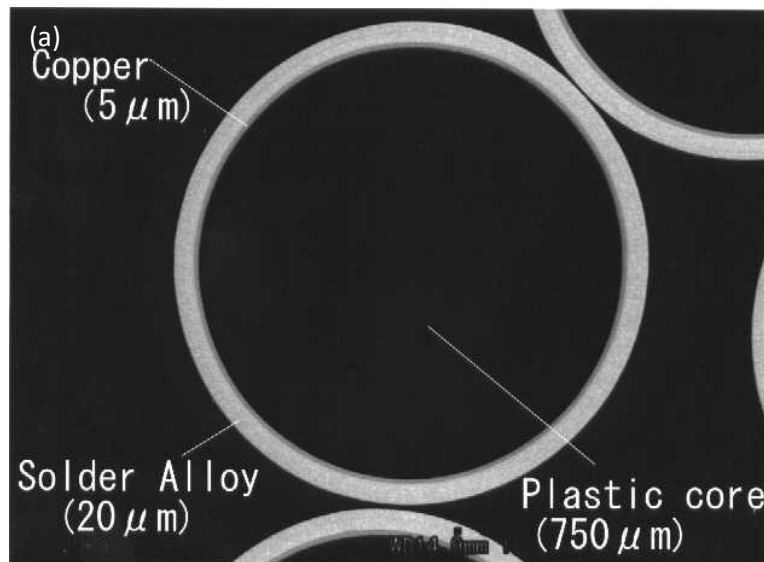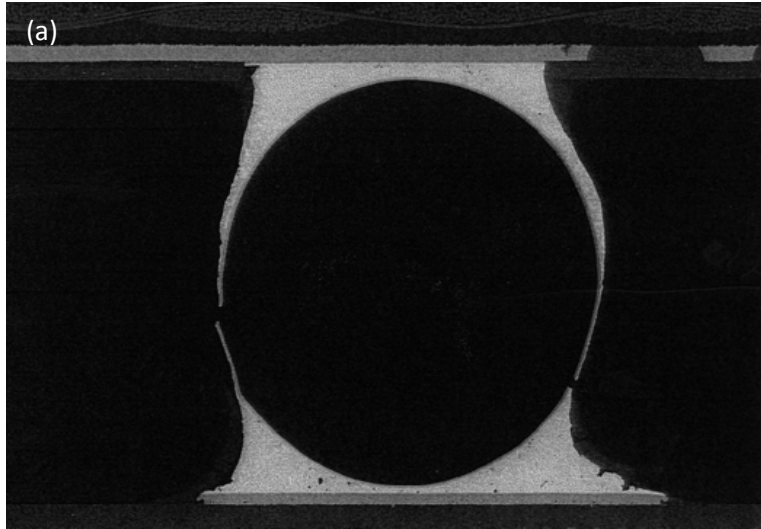
Figure 1.11. (a) Cross-section image of PCSB. (b) Soldered PCSB after thermal cycling test.

[21]

1.4 Introduction to carbon nanotubes and carbon nanotube interconnects

1.4.1 Background information of carbon nanotubes

Carbon nanotubes (CNT) are wrapped up graphitic sheets with a hexagonal lattice [24], as shown in Figure 1.12. With a cylindrical shape and a typical diameter smaller than 10 nm, the carbon nanotube is considered to be one of the materials with the highest aspect ratio up to 1.32×10^8 [25]. Depending on the number of layers of the graphitic sheets, CNTs can be categorized as single-wall carbon nanotube (SWNT) and multi-wall carbon nanotube (MWCT). Since their discovery in 1991 [26], CNTs have drawn worldwide attention of research due to their superb physical properties and therefore great potential for a huge variety of applications such scaffold materials for biomedical application, ropes, transistors, electrical interconnects, sensors/actuators, batteries and solar cells.

CNT has excellent mechanical properties and it has been known as one of the strongest materials yet discovered in terms of tensile strength and elastic modulus, with a Young's modulus an order of magnitude greater than that of stainless steel. The covalent sp^2 bond between carbon atoms is the main reason for CNT's strength [27]. The physical properties of CNT are different on different direction. In the axial direction, Young's modulus and the tensile strength are as high as 270-950 GPa and 11-63 GPa, respectively [28]. In comparison, CNTs are rather soft in the radial direction and radial Young's modulus is two orders of magnitude smaller than the axial modulus. In addition, it has been indicated that even the van der Waals forces between tubes can deform two adjacent CNTs [27].
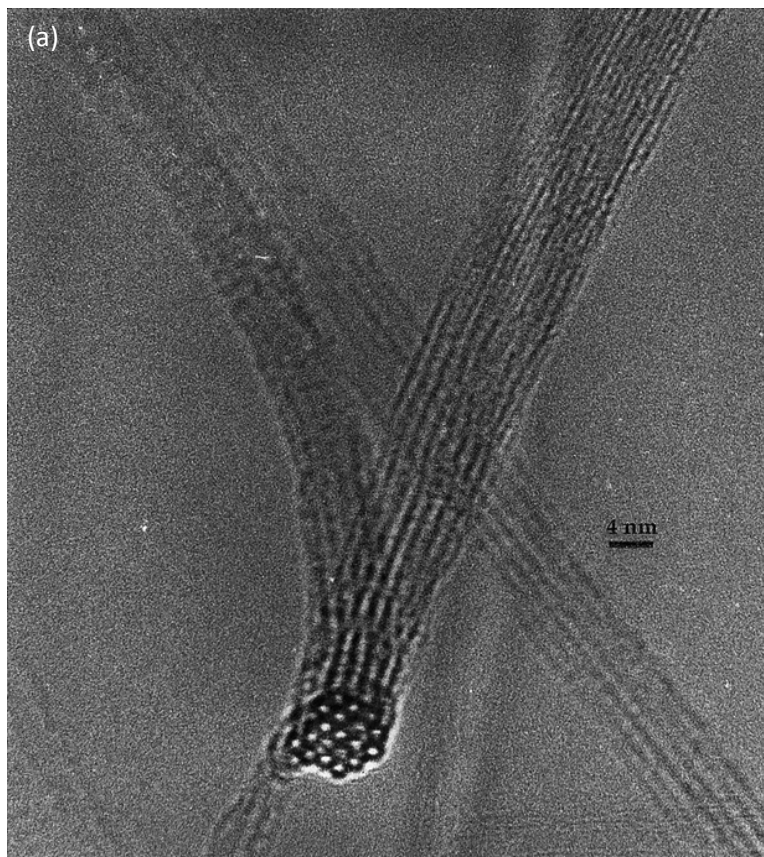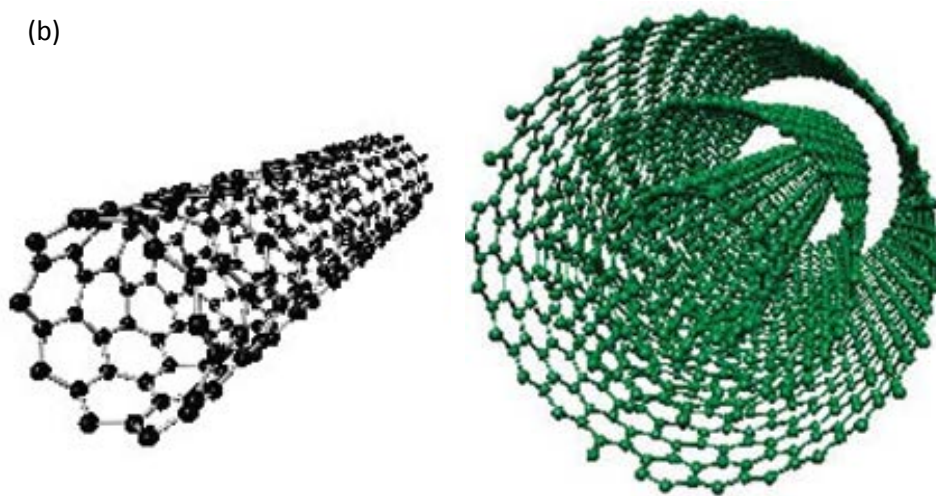
Figure 1.12. (a) Transmission electron microscopy image of bundles of chemical vapor deposited carbon nanotubes [29]. (b) Single-wall carbon nanotube (left) and multi-wall carbon nanotube (right) [30].

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Even though all types of CNTs have cylindrical shapes, the atomic configuration of the

carbon atoms is various, which has great impact on the physical properties of the CNTs. The

direction the graphene sheet is wrapped is represented by a pair of chiral vectors (n,m). The

integers n and m are the number of unit vectors along two directions in the crystal lattice of

graphene. The unit vectors are typically chosen along the neighboring centers of the

honeycomb hexagon, which a separation angle of 60°, as shown in Figure 1.13. If m = 0, the

nanotubes are zigzag, and if n = m, the nanotubes are called armchair nanotubes. Otherwise,

they are called chiral. The diameter of an ideal nanotube can be calculated from its (n,m)

indices as shown in Equation 1.1, where a = 0.246 nm.
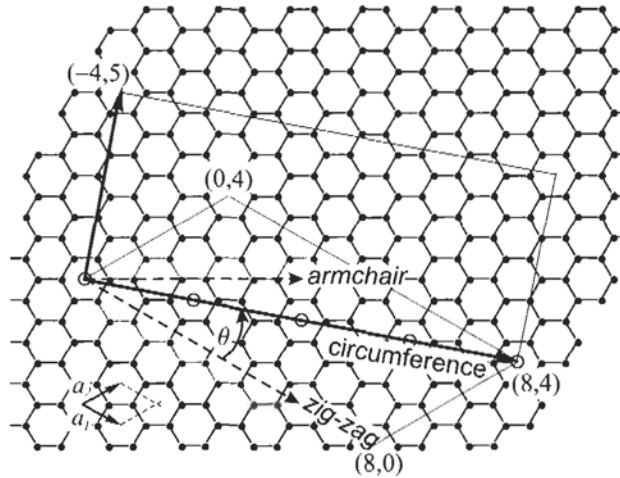
Figure 1.13. Graphene honeycomb lattice with the lattice vectors a_1 and a_2 [31].

$$d = \frac{a}{\pi} \sqrt{n^2 + nm + m^2} \qquad (1.1)$$

For single wall nanotubes, the electrical properties of the nanotubes strongly depend on

the chirality. Band gaps varying from 0 to 2eV are possible. For a given (n, m) nanotube, it can be either metallic or semiconducting, as shown in Table 1.3. Ballistic conduction of electrons happens along the axial direction of metallic carbon nanotubes and therefore metallic carbon nanotube shows higher electrical conductivity along the axial direction than the most conductive metal at room temperature. Superconductivity of CNT at cryogenic temperature has also been reported [32].

Table 1.3. Electrical property dependence of SWNT on chirality

Chirality	Electrical Property
n = m	Metallic
n – m = multiple of 3	Semiconducting with small band gap
Others	Semiconducting

Electromigration is a common phenomenon reported that limits the current carrying capability of metals. CNTs have been known to be capable of carrying a current density as high as 4×10^9 A/cm^2, which is 3 orders of magnitudes compared to conventional copper interconnects [33].

Similar to the directional electrical conductivity of the CNT, the thermal conductivity of CNT is good along the tube. In contrast, the thermal conductivity across the wall of the tubes is low enough to be insulating [34].

1.4.2 Carbon nanotube interconnects

Due to the excellent electrical and thermal conductivity of CNT, it has the potential to be used as interconnect. Also, CNT interconnects can be flexible and stress decoupled, which is beneficial to accommodate for coefficient of thermal expansion (CTE) mismatch [35]. In addition, carbon nanotube interconnects may be advantageous for high frequency application due to their reduced skin effect [36].

The most common method used for CNT growth on substrates is chemical vapor deposition (CVD) [37]. In a chemical vapor deposition process of CNTs, substrates are exposed to carbon containing gaseous precursors, which decompose on the areas of the substrates where catalyst layers were previously deposited to build up the CNTs. The thin catalyst layer serves as nucleating sites where carbon atoms deposits and forms tubes. By using CVD, CNT patterns are grown on predefined catalyst-seeded areas. Figure 1.14 shows a typical CVD setup for CNT growth. One limiting factor of this method is a high processing temperature, typically greater than 700 °C to yield structures of high quality CNT [37], which is not compatible with conventional microelectronics and CMOS process flows. Figure 1.15 shows SEM images of CNT interconnects grown using CVD [38].

Transferring CNTs grown on another substrate can mitigate the high processing temperature issue of the CVD process at the expense of additional steps to deposit and reflow solder or conductive paste patterns which stick to and carry CNTs during transferring [39]–[42]. Additionally, since the areas to be covered with CNT forest are defined by the application of solder or conductive paste, the areas of CNT forests are not as well-defined compared to photo-lithographically defined patterns. The CNT transferring process and transferred CNT interconnects are shown in Figure 1.16 and Figure 1.17 [39].

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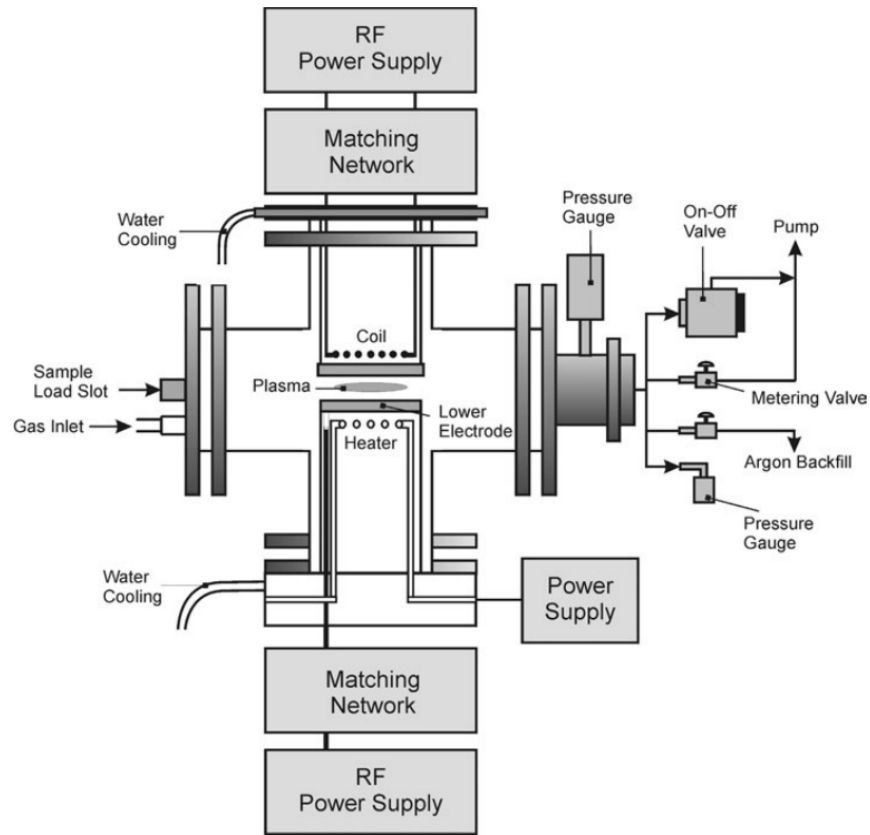
Figure 1.14. A typical CVD setup for CNT growth [37].
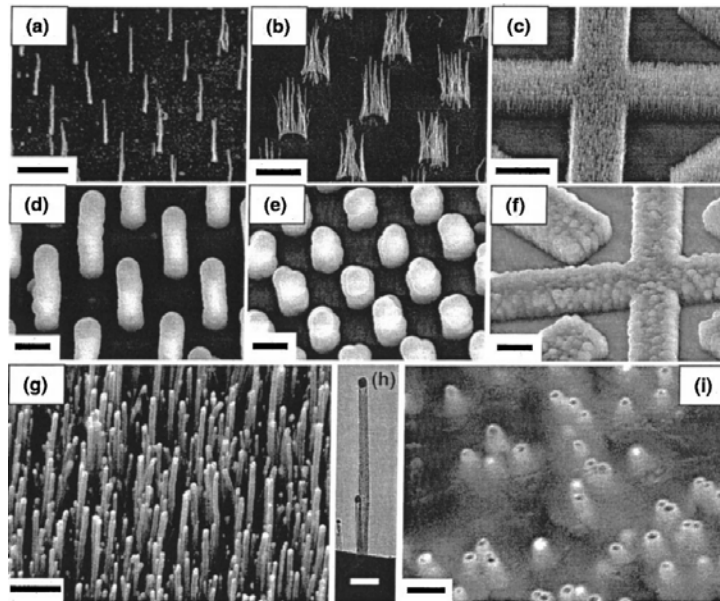
Figure 1.15. SEM images of CVD grown MWNTs. The scale bars are 5, 3, 10, 2, 5, 10, 1, 0.2, and 0.2 mm, respectively [38].
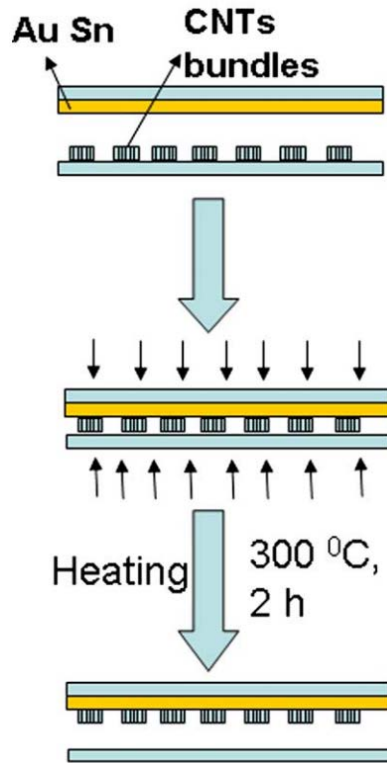
Figure 1.16. CNT interconnects fabrication process by transferring. CNTs are first grown on one

substrate and then transferring to another [39].
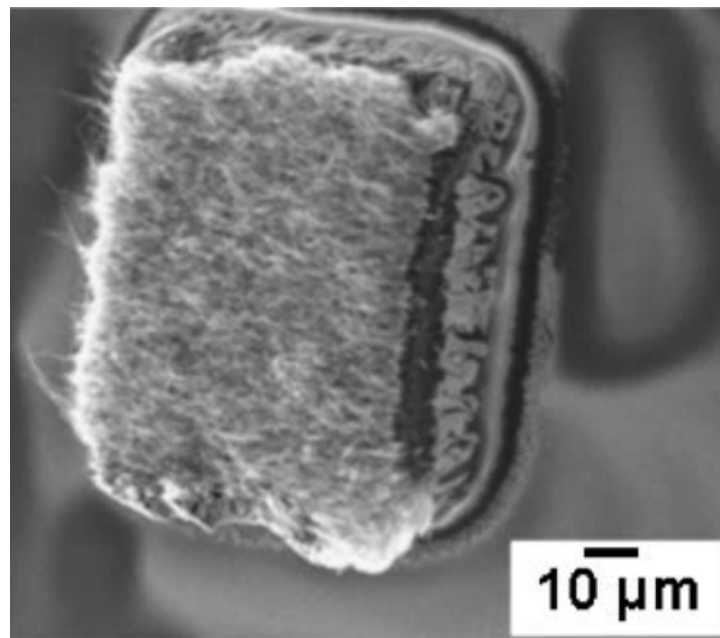
Figure 1.17. SEM images of CNTs transferred onto solder pads [39].

Chapter 2
Double Helix Interconnect

In the last two decades, various structures of MEMS type interconnects have been studied [7]–[23], [43]. Two contact modes are used in these structures: soldered contact and sliding contact. Soldered contacts use solder on the MEMS based compliant interconnect structure to make connection and have been used on a number of MEMS structures including microsprings [9], [10], [12]–[14], micro-helix structure [15], [16] and Sea-of-Leads [11], [17]. Soldered contacts provide good reliability and low electrical resistance. However, soldered contacts are detrimental to the reworkability of the compliant structures.

An alternative approach to make contact between the MEMS-type interconnects and a chip without solder is to use sliding contact [12]–[14]. Stress-engineered microsprings are found to be useful for sliding contact due to their highly compliant structure. By pressing a chip with contact pads against the microsprings, the microsprings bend and the tips of the microsprings touch and slide on the contact pads to make an electrical connection. Unlike soldered contacts, since the microsprings physically touch the contact pads, the assembly is easily disassembled and capable to be reused. We note that generally, implementations using the sliding mode contact require additional packaging structures to hold the chips in place and in contact with the substrate or interposer.

One downside of the stress-engineered microsprings is their relatively high electrical resistance. Cheng et al. designed and fabricated one of the most electrically conductive

compliant microsprings, which demonstrates a resistance of approximately 70 mΩ [14]. Their microsprings are essentially long thin and narrow pieces of curled-up metal fabricated on top of a chip. The tips of the microsprings touch the contact pads on a second chip to provide an electrical connection. The electrical performance is largely limited by the geometry because the cross-sectional area of the microspring and contact area to the contact pad are small. Another issue with the microspring is its inability to scale down. Though the width of the springs can be scaled down easily, the springs need be long enough such that they can curl to a sufficient height to provide the desired level of compliance.

In this work, we describe a double helix MEMS-type interconnect structure. Single-helix MEMS-type interconnects of different shapes (G-helix, β-helix etc.) have been studied in the last decade [15], [16]. However, all these interconnect use solder for permanent bonding and the geometry of the structures shows high resistance even in simulation [10]. The double helix compliant interconnect reported in this paper has low resistance and uses pressure to make electrical connection such that the need for solder and underfill is minimized or eliminated.

Due to the development of wireless applications in recent years, many research works have focused on millimeter-wave frequency range systems. One important aspect of these systems is module packaging. The proper strategy to assemble and interconnect monolithic microwave integrated circuits (MMICs) is critical to the performance of the system [44]. Flip-chip approach is considered to be the most promising approach to make interconnects and assemble chips due to its low reflection and insertion loss as well as low fabrication cost. The vertical off-chip compliant interconnects are used in combination with flip-chip bonding technology.

Despite the works on various structures of the compliant interconnect, to the best of our

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knowledge, none of them focused on the high frequency performance of the compliant structure. This work also presents the design and fabrication a flip chip bonded coplanar waveguide (CPW) structure using compliant double helix structures as interconnects [45]. The CPW serves as a test structure for characterization of the double helix interconnects. The performance of the structure was simulated and measured up to 50 GHz. The insertion loss and reflection loss were simulated and measured to be reasonably low.

In section 2.1, the fabrication process of the double helix MEMS-type compliant interconnects is described. Section 2.2 presents electrical characterization and reworkability results of the structure. Electrical and mechanical simulation results are included for comparison purpose. Section 2.3 includes the simulation and measurement results of the structure working at high frequency.

2.1 Fabrication of the double helix MEMS-type interconnect

Figure 2.1 schematically illustrates the fabrication procedure used to form the double helix MEMS-type interconnects, or double helix contacts. Only one helix of the pair is shown in Figure 2.1(a-g) for clarity purpose. The other helix is colored in semi-transparent purple in Figure 2.1(h). Starting with an oxidized silicon wafer, 50 nm Ti and 400 nm Cu were deposited as a seed layer for copper electroplating (Figure 2.1(a)). An AZ 9245 photoresist layer was applied to define the structure used for characterization, namely the underlying lateral metallization of a snake and comb structure (as described in the electrical characterization section), onto which the double helix structure was to be fabricated. Copper was electroplated to construct a 3 µm thick snake and comb structure (Figure 2.1(b)) and the applied photoresist was then removed (Figure 2.1(c)). Sequentially, another lithography step was performed to coat the snake and comb structure with an 8 µm thick photoresist pattern. This layer of photoresist was 5 µm taller than the snake and comb to allow the formation of patterns on top of the snake and comb. The photoresist was then exposed and developed followed by hard bake at 90 °C for 20 min and copper electroplating to form the bottom pillars of the double helix structure (Figure 2.1(d)). The hard bake of the photoresist is necessary before copper electroplating to prevent the possible outgassing and cracking of the photoresist caused by the following steps. The baking temperature was kept much lower than the softening temperature of the photoresist to avoid reflow. Careful preparation and tuning of the Cu electroplating resulted in uniform plating of the Cu to a level even with the defined photoresist. Without removing the photoresist, 200 nm of Cu was deposited to serve as a second seed layer for copper electroplating (Figure 2.1(e)). Similar to the electroplated bottom pillars, patterns were defined with 2.5 µm of photoresist and electroplated with copper to form lateral overhang

structures (Figure 2.1(f)). Steps from Figure 2.1(d) to Figure 2.1(f) were repeated to build up the structure to form a full turn of the double helix structure (Figure 2.1(g)). Note also that these steps could continue to be repeated to form taller structures with higher vertical compliance, which may be useful for chips that are to be mounted onto substrates with uneven surfaces. Additionally, the thickness of the lateral overhangs is a variable that can be optimized to balance electrical and mechanical performance, as well as ability to be fabricated. After finishing a complete turn of the double helix structures, seed layers and photoresist must be removed to expose the double helix structure. The structure was soaked in acetone, methanol and copper etchant alternatively with mild agitation until the seed layers and photoresist were completely removed. To ensure a thorough removal of photoresist, an oxygen plasma descum process was then performed. After etching the initial Ti seed layer using BOE, the double helix compliant interconnect structures are complete and ready for use (Figure 2.1(h)).

All of the copper electroplating steps were performed at a current density of 8 mA/cm2. Before each electroplating step, the substrate was dipped in 1% hydrochloric acid to remove any copper oxide on the surface of the Cu that was to be electroplated to ensure uniform plating. The copper electroplating solution used was an acidic copper plating solution consisting of copper sulfate (60 g/L), sulfuric acid (100 g/L), hydrochloric acid (0.2 g/L) and small amounts of brightener and suppressor (Cu electroplating additives). Note that since the photoresist layers were not removed before the complete double helix structure was fabricated, it is critical to control the copper plating time so that the height of the electroplated copper layers is close to that of the photoresist layers to allow a planar and uniform surface and facilitate the subsequent fabrication steps.

The fabricated double helix interconnects are uniform and of high yield, as shown in the

SEM image of Figure 2.2. The fabrication process is based on conventional photolithography and electroplating of Cu. All the steps were completed at the wafer level and performed at room temperature. Therefore, this process can be an extension of the standard back-end-of-line (BEOL) or wafer-level packaging process to provide chip interconnection with high I/O density [11]. At this point, the top surface of the Cu double helix is the native Cu surface and has not been optimized for best electrical performance. As described in the electrical performance section below, this surface is a source of considerable electrical resistance that can possibly be minimized through further fabrication and characterization efforts such as coating with Au or Cr or intentional nano-tailoring.

(a) Deposit
Ti/Cu
seed layer

(b) Pattern photoresist
and electroplate the
snake and comb

(c) Remove photoresist

(d) Pattern photoresist
and electroplate Cu
pillar

(e) Deposit Cu seed
layer

(f) Pattern photoresist
and electroplate Cu
overhang

(g) Repeat step (d) to (f)

(h) Remove photoresist
and seed layers
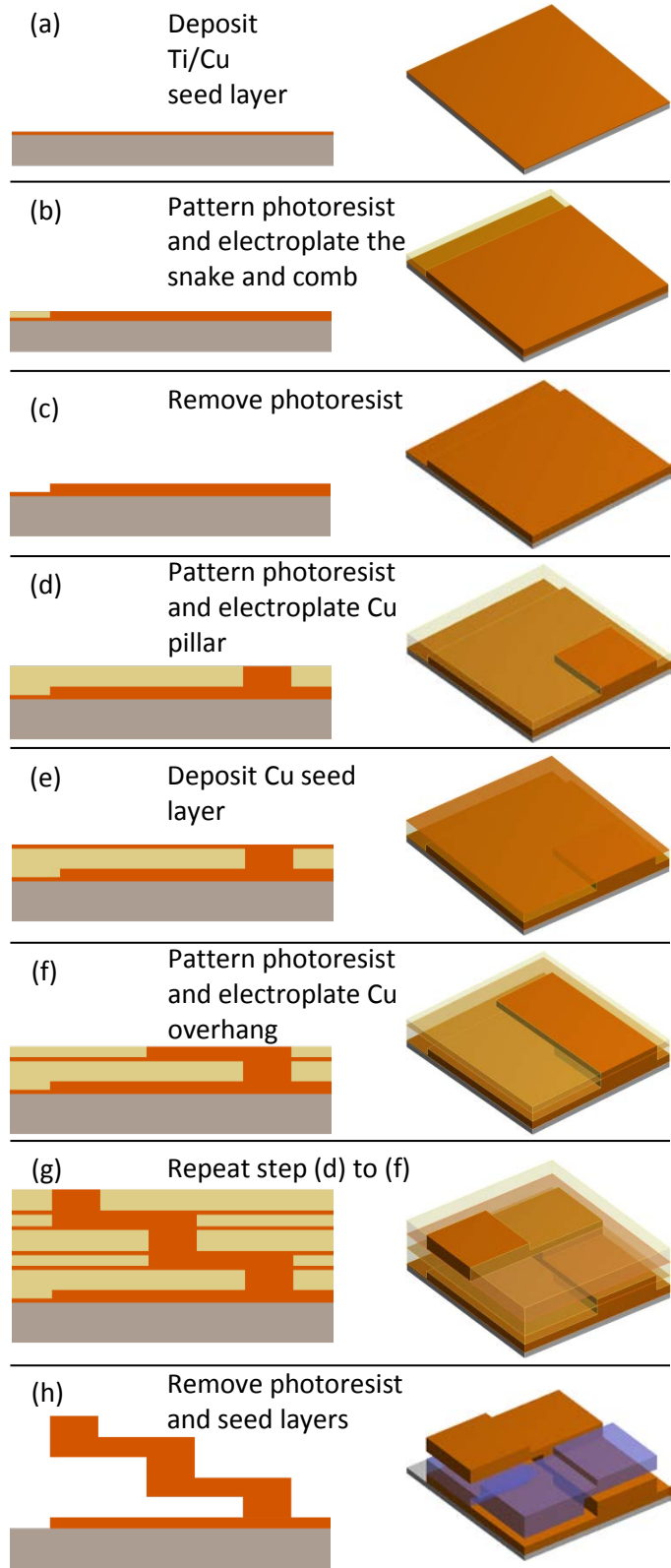
Figure 2.1. Schematic fabrication flow for double helix compliant interconnect structures. The cross-section schematics are shown on the left while the 3-D views are listed on the right. Only one helix of the pair is shown in Figure 1(a-g) for clarity purpose. Figure 1(h) shows the other helix in purple. Gray, yellow and orange represent oxidized silicon wafer, photoresist and copper, respectively.
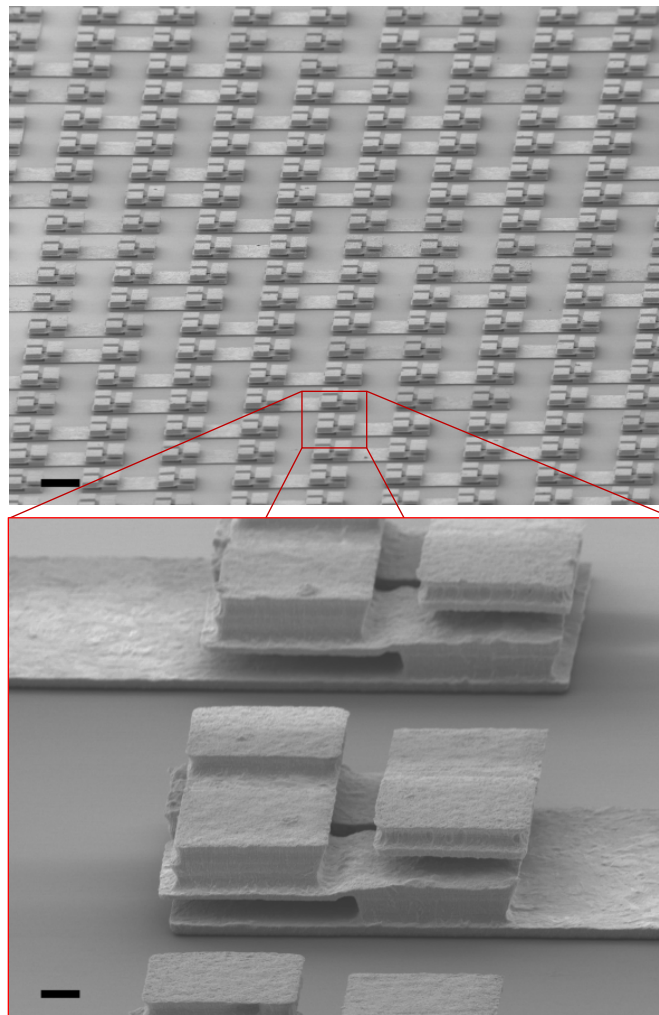
Figure 2.2. SEM images of an array of fabricated double helix contact structures prior to mechanical and electrical testing. (Scale bar: 100 µm (top image) and 10 µm (bottom image).)

2.2 DC electrical characterization

2.2.1 Experimental setup

Applying pressure is necessary for the double helix interconnects to electrically connect with contact pads on a corresponding second chip. Therefore it is useful to explore the impact of the applied load on the electrical resistance of the structure. To measure the resistance of the structure under varying forces, a flip chip bonder (FC-150) was used to apply various loads onto the double helix compliant structures.

The snake and comb structure for electrical characterization is illustrated in Figure 2.3. The snake is used for measuring resistance while the comb is used for detecting unwanted shorts. Note that the double helix interconnects chip described in the previous section only has half of the lateral metallization of the snake and comb structure (blue and green in Figure 2.3). A complementary snake and comb contact pads chip, with lateral metallization that completes the daisy-chain structure (blue and orange in Figure 2.3), is necessary to be assembled onto the double helix interconnect chip in order to make a complete snake and comb structure for resistance measurements. To fabricate the complementary contact pads chip, photolithography was again used to define the pattern on an oxidized silicon substrate and gold was electroplated on a previously deposited gold seed layer to make an approximately 1 µm thick gold contact pads pattern. The substrate was diced into chips after the photoresist and the seed layer were removed.
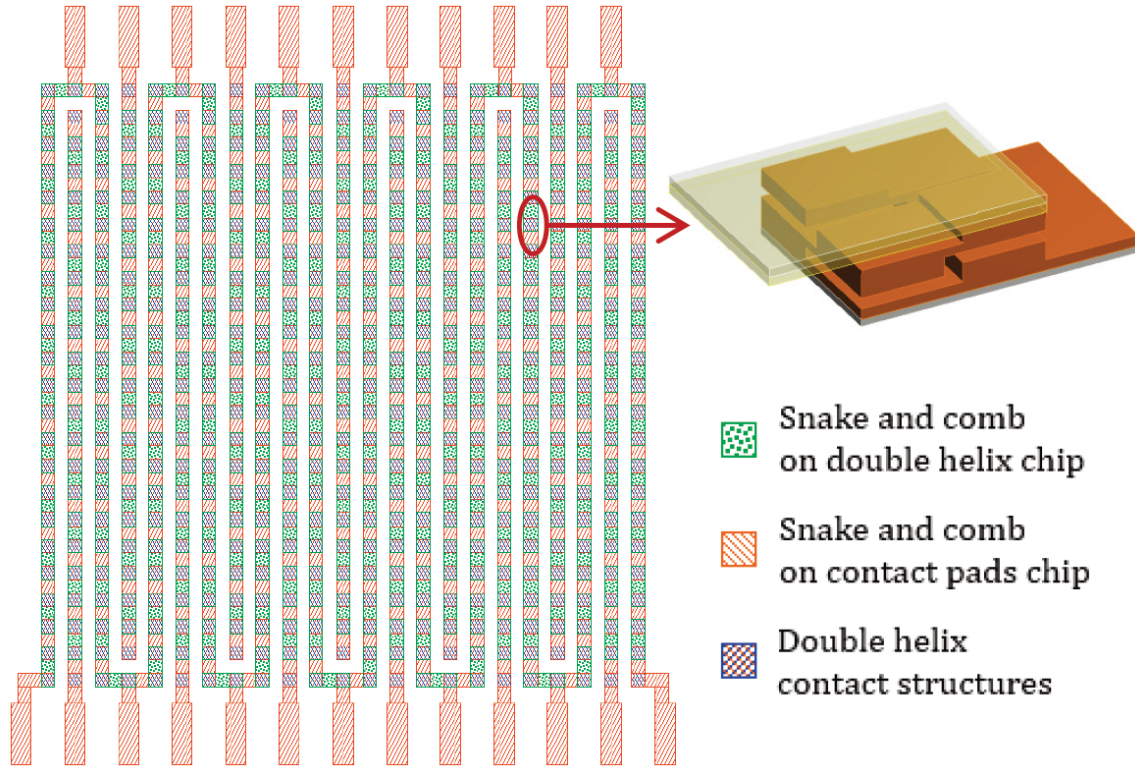
Figure 2.3. Mask layers of snake and comb test structure and double helix interconnects for electrical measurements. The double helix contacts are pressed against matching contact pads during measurement to form a complete chain. In the top right inset, gray, gold and orange represent oxidized silicon wafer, gold and copper, respectively.

Figure 2.4(a) shows a schematic of the electrical measurement set-up. The double helix interconnect chip was picked up by the arm of the flip chip bonder, held inverted, then aligned to and pressed against the matching contact pads chip. Since it is not practical to use micro-manipulated probes inside a flip-chip bonder to probe the chip, especially when 4-point resistance measurement is needed, electrical contacts to the contact pads on the edge of the contact pads chip need to be extended so that measurement can be performed using equipment outside of the flip-chip bonder. In order to do so, the contact pads chip was attached to an

alumina substrate and wire bonds were used to connect the pads of the contact pads chip to gold pads on the alumina substrate, as shown in Figure 2.4(c). Soldered wires were used to further extend electrical connections to the structure outside the flip-chip bonder, as shown in Figure 2.4(b). An Agilent 34420A Micro-Ohm meter was used to perform 4-point measurements.
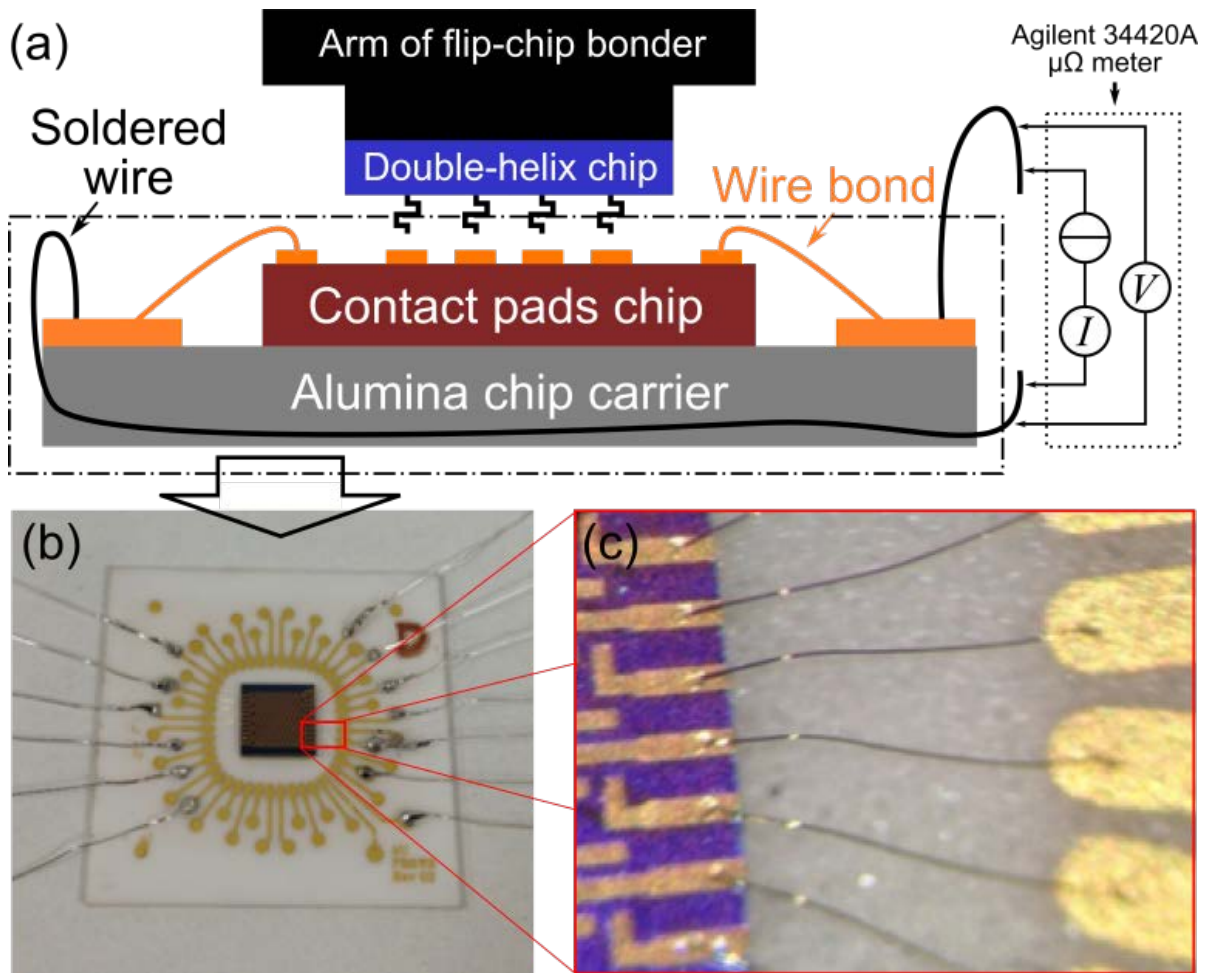
Figure 2.4. (a) The schematics of the electrical characterization. (b) Contact pads chip was attached to the alumina chip carrier with wire bonds and soldered wires to extend electrical access to the structure outside the flip-chip bonder for electrical measurement. The soldered wires were clipped and connected to the Micro-Ohm meter. (c) Zoom view of the wire bond between the contact pads chip and the alumina chip carrier. (d) FC-150 flip chip bonder.

2.2.2 Electrical resistance measurement and test fixture resistance extraction

The FC-150 was used to provide a controlled load onto the double helix interconnect chip over the range of 0 to 5 kg. The corresponding average applied force on each double helix

structure ranged from 0 to 92.6 mN, considering that there are 529 double helix structures on each chip. Using the snake and comb structure, no shorts were detected, indicating a complete removal of seed layers. The measured resistance of 22 double helix structures in series, including the resistance of the test fixture, is shown in Figure 2.5.

Since the measured resistance data includes the resistance of the lateral metallization and resistance of the test fixture (wire bonds and soldered wires), the resistance of individual double helix contact structure cannot be calculated by simply dividing the total resistance by the number of double helix structures. To accurately extract the resistance of individual double helix structures from the experiment data, an extrapolation method was used, as shown in Figure 2.6(a) and (b). The I-V curve was measured using a Keithley 4200 semiconductor characterization system. The I-V curve is linear, demonstrating high quality electrical interconnection. Consecutive chains of double helix structures were measured and the data points were linearly fitted and plotted against the number of double helix structures. As a result, the intercept of the fitted line and y-axis should approximate the resistance of the test fixture. The extrapolated resistance of the wire bonds and the soldered lead wire of the test fixture was found to be approximately 2.616 Ω, as shown in Figure 2.6(b). Direct measurement of the test fixture (lead wires, wire bonds and a small section of lateral metallization), using a four-wire method, gave a resistance value that was within 10% of the extrapolated value. Since the resistance of the test fixture is similar to the resistance of the string of double helix structures, it is necessary to account for it in the analysis of the resistance of individual double helix interconnect structures. By subtracting the resistance of the test fixture from the total resistance and then dividing the resulting resistance by the number of the double helix structures, the resistance of individual double helix structures (including a small portion of

lateral metallization) was obtained as a function of applied load, as shown in Figure 2.6(c).
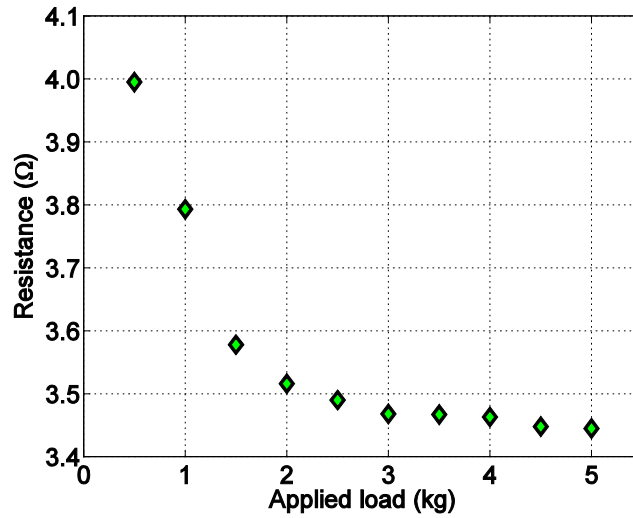
Figure 2.5. Measured resistance of 22 double helix structures in series under different forces.

Note that this includes the resistance of the lateral snake and comb metallization, as well as that

of the test fixture.
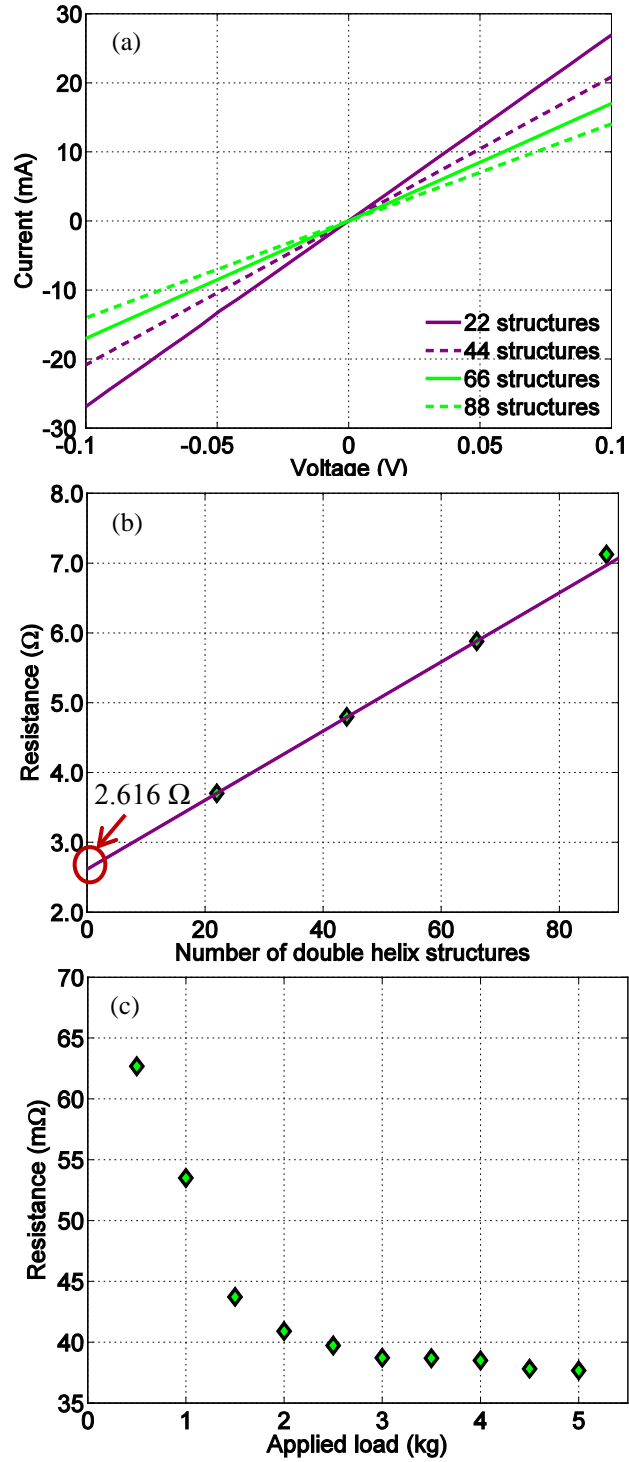
Figure 2.6. (a) I-V characteristics of the resistance of the double helix structures, including the test fixture. (b) Extrapolation of the resistance of the test fixture. (c) Resistance of one double helix interconnect structure versus load applied to full chip.

2.2.3 Mechanical and electrical analysis using FEA simulation

2.2.3.1 Mechanical

A representative structure was modeled and simulated using finite element analysis (FEA) software ANSYS Workbench 14.5, as shown in Figure 2.7(a). Since both the snake and comb structure and the double helix compliant interconnect contribute to the measured resistance, the contact pads of the snake and comb are included in the FEA model. The time independent plastic behavior of electroplated Cu was modeled using a bilinear kinematic hardening rule. The yield strength of electroplated copper was assumed to be 280 MPa. The Young's modulus and the tangent modulus were assumed to be 140 GPa and 4.67 GPa, respectively [46]. The maximum deformation in the vertical direction was approximately 2.6 µm when 0.5 kg of load was applied to the structure (this corresponds to approximately 9.26 mN of force per double helix structure). The compliance of the fabricated double helix structures is approximately 0.28 mm/N, comparably lower than other reported values [15]. However, we note that the compliance is adjustable by modifying the geometric parameters of the structure, such as overhang thickness, pillar length and height. When the applied load on each structure was greater than 0.62 kg, the gold contact pad chip touched the upper lateral overhang and created a shorter electrical path. This explains the significant resistance drop when the applied load increased from 0.5 kg to 1.5 kg, as shown in Figure 2.6(c). The presented results for chains of multiple structures are smoothed, due to an assumed slight variation in structure height due to fabrication tolerances. Additionally, more compression is expected to lead to more complete contact between the vertical and lateral sections of the double helix structure and is another reason that the resistance drops as the applied force increases. Although the low resistance at higher loads is helpful, the compliance of the structure is degraded. Therefore, the structure is

recommended to be used under low compressive load. The issue of resistance change due to varying loads at low compressive loads can be solved by using additional fixtures such as the balls/pits fixtures [14] to clamp the compliant structure at a fixed load.

2.2.3.2 Electrical

The resistance of the structure is also modeled in ANSYS Workbench. The electrical potential distribution was modeled by feeding a source current of 1 mA through the structure, as shown in Figure 2.8. The resistance was calculated by dividing the sensed voltage drop by the source current. The top contact pad is made of electroplated gold with a resistivity of 3 μΩ·cm. The rest of the structure uses electroplated copper with a resistivity of 2.4 μΩ·cm. The resistivity of the electroplated gold and copper was obtained from resistivity measurement using a corresponding Van der Pauw structure. All the components contributing to the total resistance of the structure were modeled except for the contact resistance between the contact pad and the double helix structure. Even though there are models for contact resistance, these models require additional parameters such as effective contact area and asperity deformation [47], [48]. To simplify the modeling, we modeled the contact resistance of the interface as a resistor and used it to fit the total measured resistance. The simulated resistance results are listed in Table 2.1.
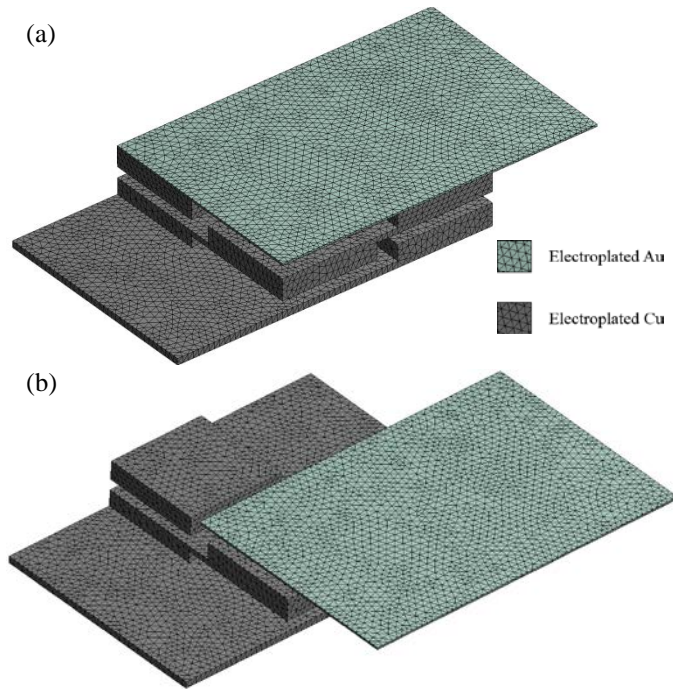
Figure 2.7. (a) The meshed 3-D FEA models of a double helix structure in full contact with the contact pads of the snake and comb. (b) The meshed 3-D FEA models of a double helix structure with only one of the two helixes making contact to the contact pads. (bottom contact pad size: 150 µm × 100 µm × 3 µm; top contact pad size: 150 µm × 100 µm × 1 µm; size of the pillar of the double helix: 45 µm × 45 µm × 5 µm; size of the lateral overhang structure of the double helix: 45 µm × 100 µm × 2.5 µm.)
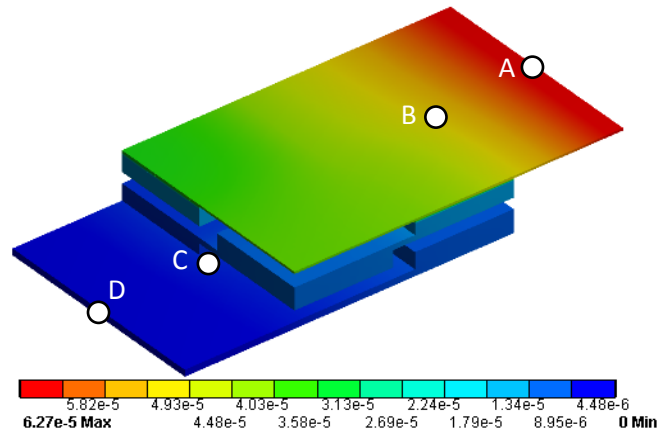
Figure 2.8. Electrical potential distribution of the double helix structure when a source current of

1 mA is fed through.

Table 2.1. Resistance components of the measured structure

Component	Resistance (mΩ)
Simulated top Au lead, R_{AB}	15.1
Simulated bottom Cu lead, R_{CD}	4.0
Simulated double helix, R_{BC} (no contact resistance)	11.4
Simulated double helix, R_{BC}' (including contact resistance)	43.6
Measured double helix, r_{BC} (including contact resistance)	19.5-51.3
Measured total resistance, r_{AD}	61-87

2.2.3.3 Scalability

Without considering the contact resistance, the simulated double helix structure has a resistance of 11.4 mΩ (r_{BC} in Table 2.1). To study the scalability of the interconnect structure, the structure was scaled laterally to half of its size and simulated. The scaled structure has a small increase of resistance to 12.7 mΩ. The mechanical compliance of the scaled-down structure was reduced. Therefore we further reduced the widths of the overhangs and pillars by approximately 3% to match the compliance of the original, non-scaled structure. By doing so, the resistance increased slightly to 13.5 mΩ. A small increase in resistance for structures with reduced lateral dimensions indicates the potential of the structure to be scaled down.

2.2.4 Extraction of the lateral resistance of the snake and comb metallization

Since the structure is only slightly bent at a load of 0.5 kg, the resistance at 0.5 kg was used and the contact resistance was swept to fit it in the ANSYS modeling. 10 chips were measured at 0.5 kg load and the resistance ranges from 61 mΩ to 87 mΩ with an average of 69.4 mΩ. In order to extract the resistance of the double helix structure without the lateral resistance of the snake and comb structure, an offset measurement was performed by slightly moving the top double helix chip during flip-chip pressing to only contact one of the two helixes of the double helix structure, as shown in Figure 2.9. The load on the structure was halved since only half of the structure was pressed. As a result, the resistance of both the single helix and the double helix structure, including the test fixture resistance and the lateral metal resistance, can be measured, as in (2.1) and (2.2). The single helix structure was assumed to have twice the resistance of the double helix, as in (2.3), because in the double helix the two single helixes are

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in parallel.

$$R_{M1} = R_L + R_t + n \cdot R_{SH} \tag{2.1}$$

$$R_{M2} = R_L + R_t + n \cdot R_{DH} \tag{2.2}$$

$$R_{SH} = 2 \cdot R_{DH} \tag{2.3}$$

R_{M1}, R_{M2}, R_L, R_t, R_{SH}, R_{DH} are the resistance of the measured single and double helix test structure chains, lateral metal, test fixture, a single helix and a double helix, respectively. n is the number of the measured helix structures. The resistance of the double helix can be extracted by subtracting (2.1) by (2.2), as in:

$$R_{DH} = (R_{M1} - R_{M2})/n \tag{2.4}$$

Equation (2.4) was verified using ANSYS simulation. The top chip was moved such that only one of the two helixes is making contact, as shown in Figure 2.7(b). Resistance of the single and double helix test structure chains (R_{M1} and R_{M2}) was simulated. The resistance of one double helix was calculated using (2.4). The calculated double helix resistance is 12.0 mΩ, which is close to the simulated resistance value of 11.4 mΩ, as shown in Table 2.1, indicating that equation (2.4) is valid for lateral resistance extraction.

Using (2.4), the measured resistance of the double helix structure was calculated, which varies from 19.5 to 51.3 mΩ, with an average of 35.4 mΩ, as shown in Table 2.1. This

variation is assumed to be mainly due to contact resistance variation. Therefore, the resistance of the structure has the potential to be significantly reduced if an improved contacting strategy or surface treatment is implemented. One method to improve contact resistance is by using closed-loop copper electroplating since it can provide a smoother contact region and make the fabrication process more controllable. Additionally, a difference in the actual structure between the fabricated structure and the simulated one and the natural copper oxide can lead to the resistance difference found between measurement and simulation as shown in Table 2.1. Given these sources of variation, as well as the fabrication-induced variation, we find that our measured and simulated performance is a reasonable match.

In comparison to other reported compliant interconnect structures that can be integrated into BEOL process or wafer level packaging processes [10], [11], [14], [15], the presented double helix structure shows relatively low resistance. Simulation results show that the Flexconnect [10] and β-helix [15] have a resistance lower than 50 mΩ, but no contact resistance was considered. Measurement data shows that the Sea-of-Leads has a low total resistance of 2.52 Ω per 54 interconnects [11], while the microspring interconnect has a resistance of approximately 70 mΩ [14].

Despite the low resistance of the double helix structure, the presented structure can be further improved in several aspects. First, the fabrication process is comparably more complex. One possibility to simplify the fabrication process is to replace the pillar and overhang structure with electroplated curved metal layers [49], [50]. By doing so, the number of metal deposition and electroplating steps can be reduced. Second, the stand-off height of the structure is comparably shorter. This geometric shortcoming can be mitigated by modifying the design of the pillar and the overhang. Furthermore, more refined fabrication processes are desired so that

higher performing and more uniform structures can be fabricated.
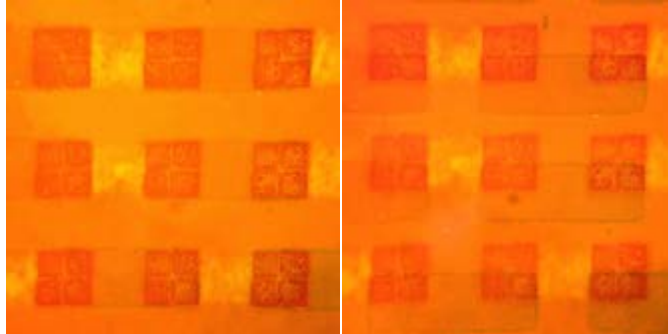
Figure 2.9. Flip chip bonding alignment observed from the microscope of the flip chip bonder. (a) Resistance measurement without offset. (b) Offset resistance measurement. Note that only half of the double helix structure was aligned to be in contact.
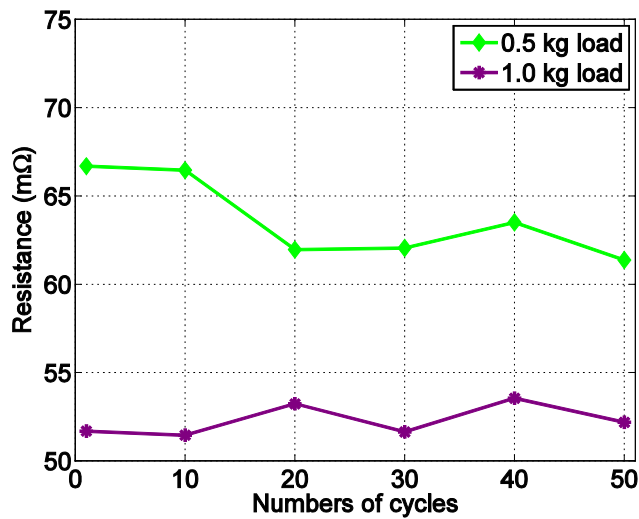
Figure 2.10. The resistance of the double helix interconnect (including lateral resistance of the snake and comb structure) after remating cycles.

2.2.5 Reworkability of the double helix interconnect

Compared to conventional solder bumps, one major advantage of the double helix MEMS-type compliant interconnect is reworkability. To study the reworkability of the structure, the flip-chip bonder was programmed to repeat applying either 0.5 kg or 1 kg loads for 50 cycles. In each cycle, the applied force ramps from 0 to its maximum in 20 s. The load was held at the maximum value for 10 s for resistance measurement and then it took another 10 s to decrease the load back to 0. The resistance of the structure was measured every 10 cycles. As shown in Figure 2.10, the resistance of the structure remains nearly constant after remating. The change of the resistance during reworkability test for both 0.5 kg and 1 kg load was less than 10%. The consistent measured resistance values of the double helix structure after multiple remating cycles indicate its potential application as a compliant and reworkable interconnect structure.

Furthermore, after remating the double helix interconnect structures for 50 cycles using a load of 0.5 kg, minimal structure change was observed as shown in Figure 2.11(a). This can be explained by observing that the applied load slightly exceeded the yield strength of the electroplated copper and caused a small amount of plastic deformation. ANSYS simulation indicates that the structure reaches the yield strength when the applied load is 0.396 kg. A 1 kg remating load causes significant deformation of the structure such that the upper lateral overhang was pressed down to touch, and remains in contact with, the lower structure, as shown in Figure 2.11(b). Though the electrical reworkability results of Figure 2.10 show the possibility for the structure to rework at 1 kg load, we see that the compliance aspect of the structure may be compromised by this plastic deformation. From these results, we see that 0.5 kg is an appropriate load to press the structure and make good electrical connection. We also note the possibility to construct structures that are more compliant and allow higher loads

through optimization of the structure (i.e., modified thickness of lateral metallization) or through the use of other metals.

In this work, 50 cycles of remating were performed since the expected number of chip upgrades and replacement is in the range of tens. Considering copper film can endure thousands of stress cycles if appropriate load is applied [51], we expect the structure being capable of remating many more cycles. The reliability test of the structure such as thermal cycling test and humidity test will be investigated in future works.
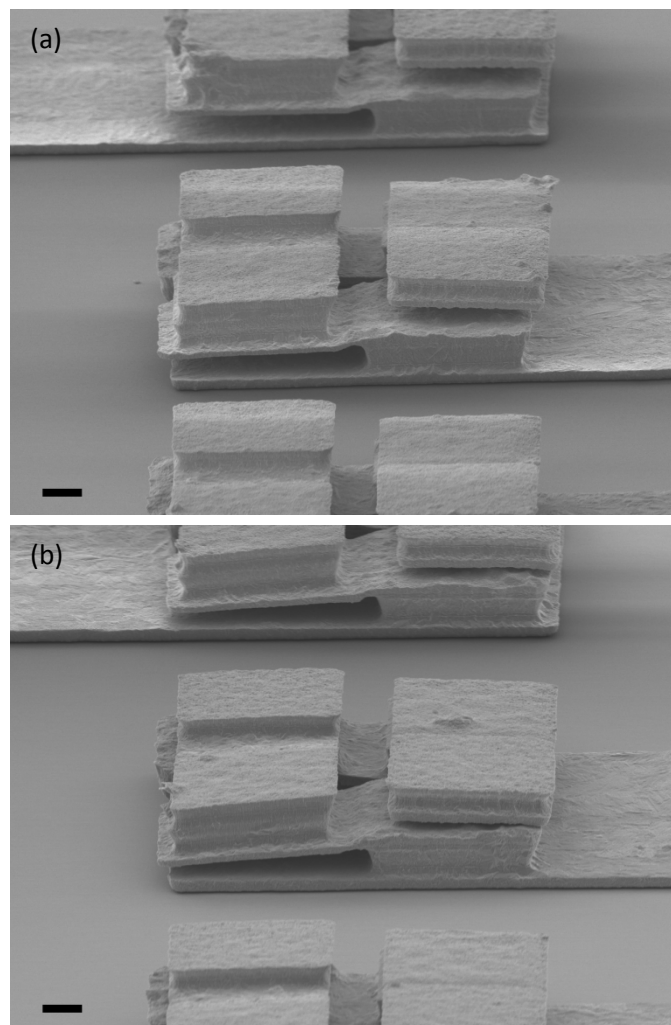
Figure 2.11. SEM image of double helix interconnect structures after 50 cycles of mating-remating under (a) 0.5 kg load and (b) 1 kg load.

2.3 High frequency performance of double helix interconnect

2.3.1 Design and fabrication of the flip-chip bonded CPW with double helix interconnects

The coplanar waveguides were used as test structure of the double helix interconnects. The schematic of the flip chip bonded CPW with double helix interconnects is shown in Figure 2.12 and the geometric parameters are listed in Table 2.2. Glass substrates were used due to their low dielectric loss. The structure was designed to have a characteristic impedance of 50 Ω. In this design, the high frequency signal transits from one CPW on the carrier to the other through 2 flip chip bonded double helix interconnects transitions and a CPW on the die. Since the signal loss through the CPW is low, the test structure provides insight on the high frequency electrical performance of the double helix interconnects.

To reduce the reflection at the interconnects, a staggered interconnects design is adopted. The center double helix interconnects were designed further away from the double helixes on the ground lines, resulting in characteristic line capacitance decreases and less reflection due to the field concentration in the air region [52].
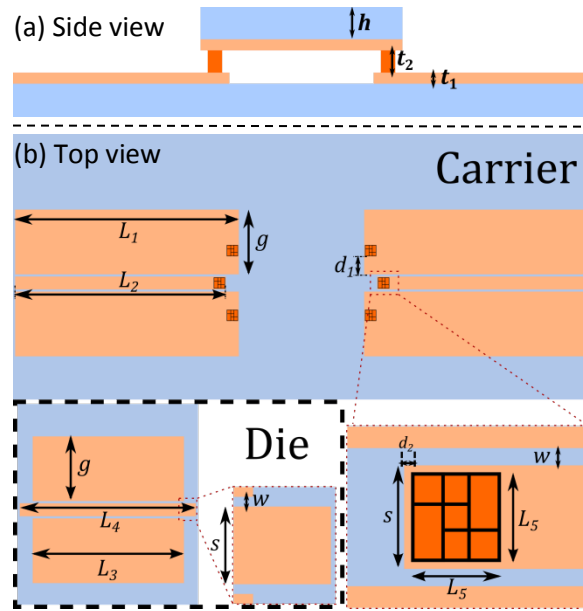
Figure 2.12. Geometry of the flip chip bonded CPW. The glass substrate, CPW lines and double

helix interconnects are in blue, light orange and dark orange.

Table 2.2. Geometrical parameters of flip chip bonded CPW design

Parameter (mm)	Value	Parameter (μm)	Value
L_1	1.9	s	120
L_2	1.78	w	20
L_3	9.60	d_1	175
L_4	1.2	d_2	10
L_5	0.12	t_1	2.5
h	0.5	t_2	25
g	0.6		

The double helix interconnect was fabricated using the method discussed in the previous sections. To fabricate indium bumps on the double helix structure, a thick photoresist layer needs to be carefully deposited onto the substrate and patterned. Since spin coating process is used in this work to deposit photoresist, it is critical to keep the spinning speed and acceleration low to avoid damaging the double helix structures. The indium bumps can also be fabricated on the other chip prior to flip chip bonding. The indium sulfamate plating bath is purchased from Indium Corp. A pulsed current plating process was used for more refined grain and better uniformity [53]. The waveform used indium plating is shown in Figure 2.13. Since large current density may induce hydrogen gas bubbles near the surface of the plated substrate and undermine the coverage of solution into the micro-scale patterns [53], the average current density was kept low to be 3 mA/cm^2.

The scanning electron microscopy (SEM) images of the fabricated double helix structures are shown in Figure 2.14. The fabricated structures have a high yield and uniformity. Figure 2.14(b) and 2.14(c) show the fabricated double helix interconnects with indium bumps and indium bumps directly deposited on the other chip, respectively. The seed layer in Figure 2.14 (c) was kept while in Figure 2.14 (b) the seed layer was removed and therefore the indium bumps got corroded during the seed layer removal process. Since the process is based on conventional photolithography and electroplating, it can be used to fabricate structures with finer pitch size. Also, it can be performed at the wafer level and be an extension of the standard back-end-of-line (BEOL).

The flip chip bond process was performed using a FC-150 flip chip bonder. The profile of the process is shown in Figure 2.15. Since the bonding load is required to be lower than the yield strength of the electroplated copper of the double helix interconnects, it is important to

estimate the yield strength of the structure. Using a finite element analysis software ANSYS Workbench 14.5, the yield strength of each double helix is determined to be approximately 2 mN and therefore the applied load should be less than 1.2 g because 6 double helix interconnects were pressured. Thus, a 1 g load was applied during flip chip bonding. In the ANSYS simulation, the yield strength of electroplated copper was assumed to be 280 MPa. The Young's modulus and the tangent modulus were assumed to be 140 GPa and 4.67 GPa, respectively [46]. The arm and the chuck of the FC-150 were heated to slightly higher than the melting temperature of indium at 180 °C during bonding. The bonded CPW with double helix interconnects is shown in Figure 2.16.
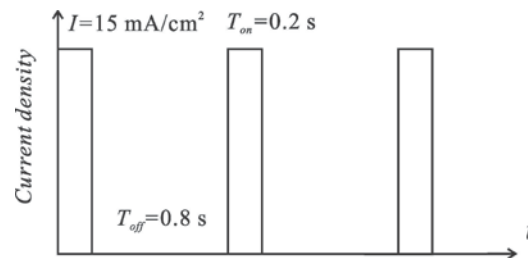
Figure 2.13. Pulsed current indium plating waveform.
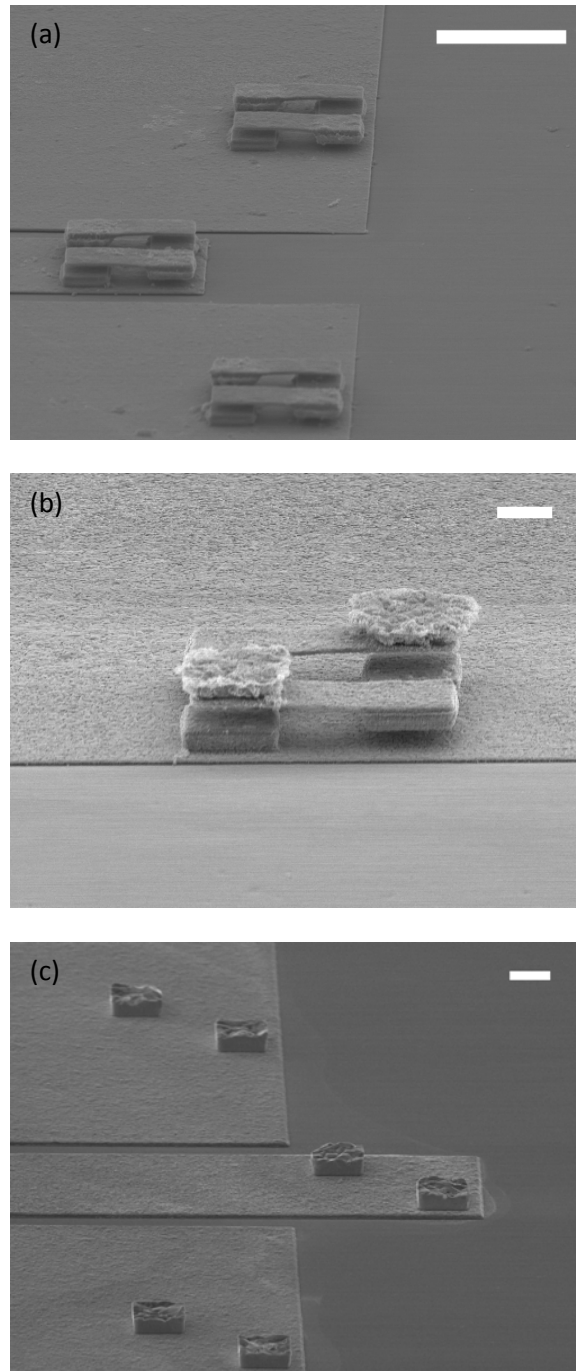
Figure 2.14. (a) Double helix interconnects on CPW with no indium bumps. Scale bar: 100 µm.

(b) Double helix interconnects with indium bumps on top. Scale bar: 20 µm. (c) Indium bumps

electroplated on the other chip for flip-chip bonding. Scale bar: 20 µm.
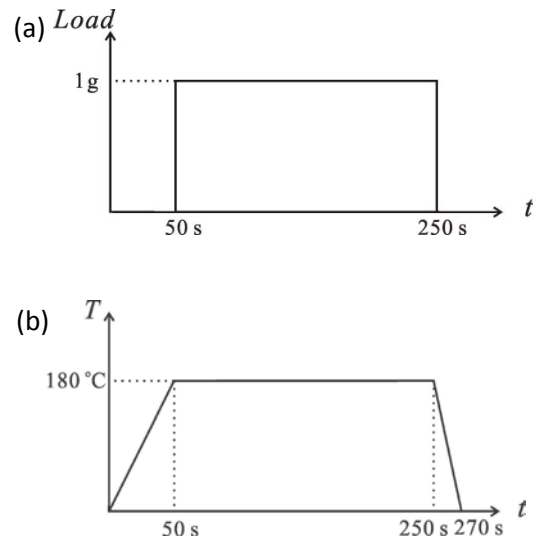
Figure 2.15. Load and temperature profile used for flip chip bonding.
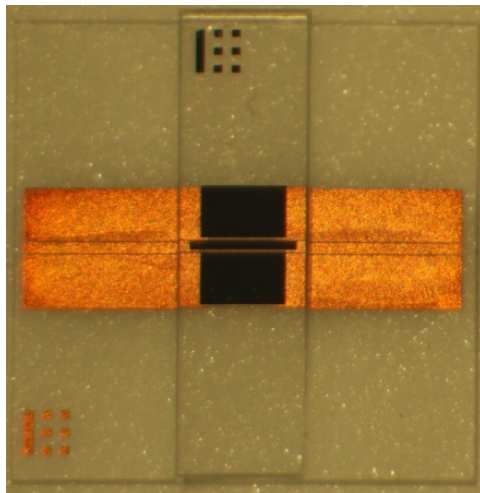
Figure 2.16. Flip chip bonded CPW with double helix interconnects.

2.3.2 High frequency characterization

The structure was modeled using HFSS 14.0. The resistivity of electroplated copper and

indium was assumed to be 2.4 μΩ·cm and 15.5 μΩ·cm, respectively [54]. Since the skin effect plays an important role at high frequency, it should be modeled. In this work, Groisse surface roughness model was used. Atomic force microscopy (AFM) was used to determine the root-mean-square (rms) surface roughness of the electroplated copper surface to be approximately 91.6 nm, as shown in Figure 2.17.
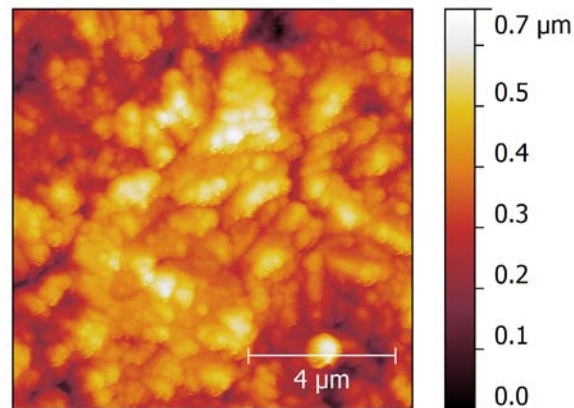
Figure 2.17. AFM image of the electroplated copper surface.

The high frequency characterization was performed using an Agilent N5227A PNA. The measurement setup is shown in Figure 2.18. On-wafer probing measurement was carried out using 150 μm-pitch Cascade ACP65 GSG probes. A full two-port Short-Open-Load-Through (SOLT) calibration was performed in order to move the reference plane close to the measured structure. The measured S-parameters were shown in Figure 2.19. The reflection loss was measured to be less than -15 dB up to 50 GHz and the insertion loss is less than -0.6 dB, including the influence of the CPW test structure. The simulation results match reasonably with the measurement results. The difference might be due to the fabrication tolerance and underestimation of the contact resistance of the indium bump. Since the flip chip bonding

process was performed at an elevated temperature in air, the copper and indium structures are easily oxidized, leading to higher resistance. Furthermore, the indium bumps were modeled in HFSS to be perfectly shaped rectangular cuboid, which is inaccurate since the indium bumps deformed during the bonding process and there might be voids remaining inside the indium bumps after bonding. With better process control, reduced loss of the structure is expected.
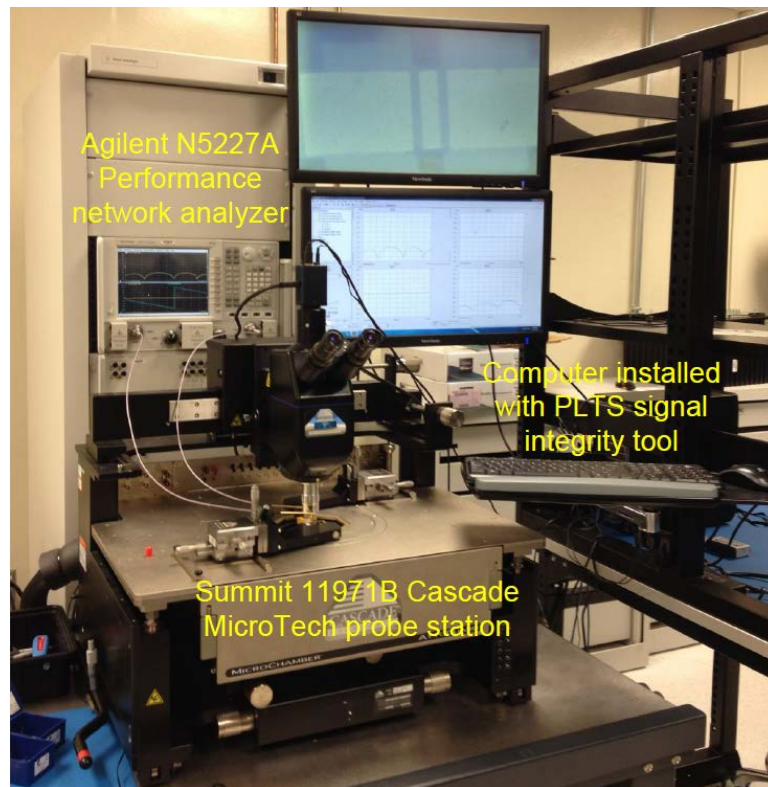
Figure 2.18. Network analyzer setup for high frequency structure measurement.
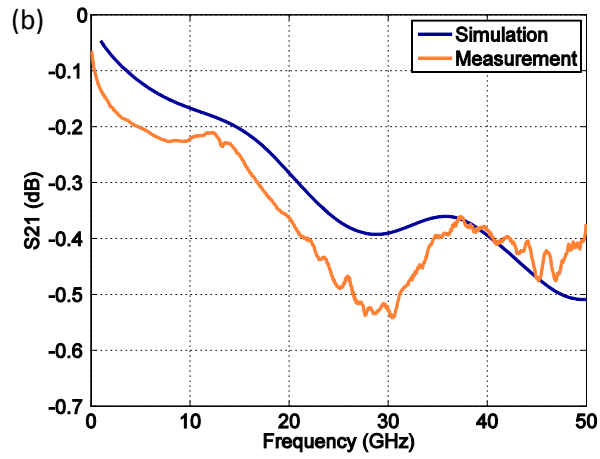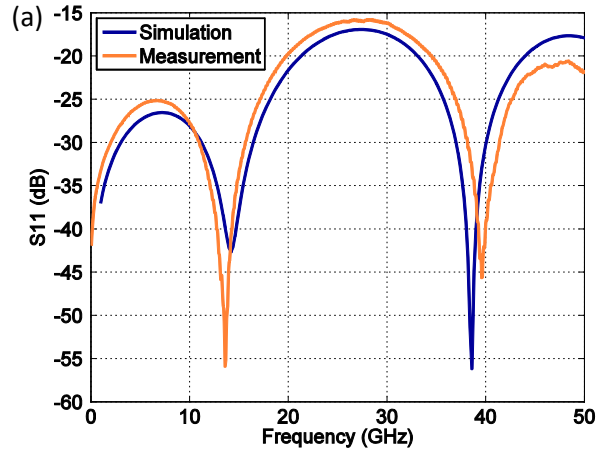
Figure 2.19. S-parameters of the Flip chip bonded CPW with double helix interconnects. (a)

Reflection loss S11. (b) Insertion loss S21.

2.3.3 Transient analysis of the double helix interconnects structure

Since the introduction of the double helix geometry affects the electrical properties of the interconnects, it is essential to understand the high frequency impact of adopting this double helix geometry. The high frequency performance comparison between the double helix interconnect and a cuboid shape interconnect of similar size is shown in Figure 2.20. The S-parameters are shown in Figure 2.21(a) and Figure 2.22(b), indicating that at steady state, the impact of using of double helix interconnects is slight.

Transient performance of high frequency interconnects is also considered to be of critical importance. Time domain reflectometry (TDR) impedance simulation was performed at 50 GHz. The TDR impedance data indicates that at the beginning of each input signal, the use of a double helix shape interconnect leads to a bigger overshoot of impedance, which is due to higher inductance and resistance of using the double helix structure. Overshoots are not desirable due to their potential of undermining the signal integrity of a system.
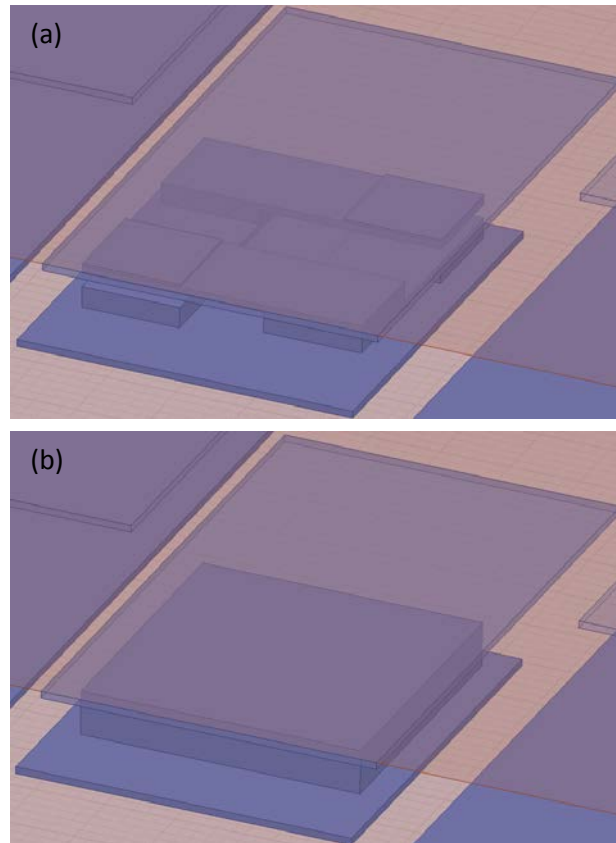
Figure 2.20. (a) HFSS model of a double helix interconnect and (b) HFSS model of a cuboid

interconnect of the same size.
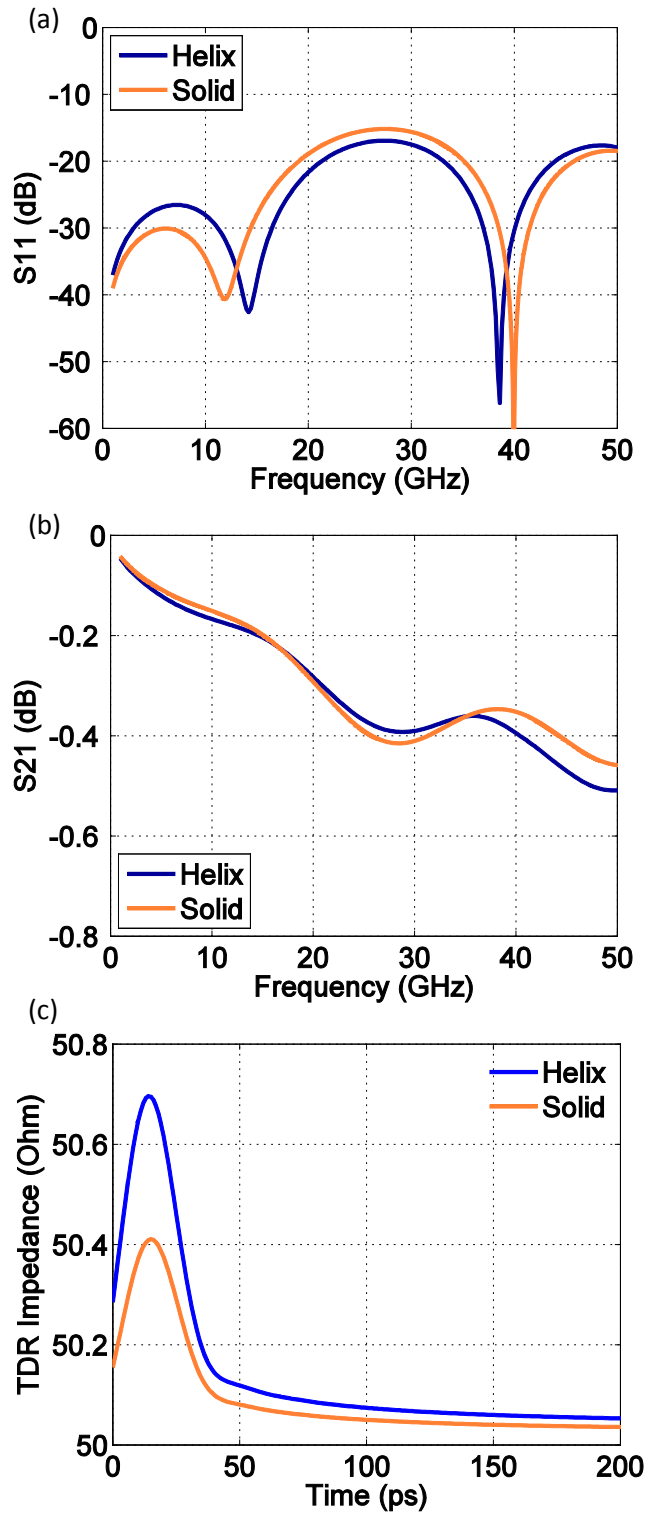
Figure 2.21. (a) S11, (b) S21 and (c) TDR impedance (at 50 GHz) of double helix of the double

helix interconnect, compared to a cuboid shape interconnect of the same size.

To further explore the impact of the impedance overshoot, transient analysis was performed using Cadence. The circuit parameters of the interconnects were extracted using ANSYS Q3D and the circuit model of the interconnect was constructed in Cadence, as shown in Figure 2.22. The interconnect is connected to a matched transmission line at 50 Ω and then terminated with a matching resistor. As a result, the impact of interconnect can be analyzed by comparing the input signal V_1 and output signal V_2. A sine wave signal input at 50 GHz and 1 V is used.

The transient performance of the interconnect is shown in Figure 2.23. Similar delays of input signal was observed on solid cuboid interconnect and double helix interconnects. It was also observed that despite the overshoot of TDR impedance, the transient performances of the double helix and the solid cuboid interconnects are similar, indicating the viability of double helix interconnects at high frequency.
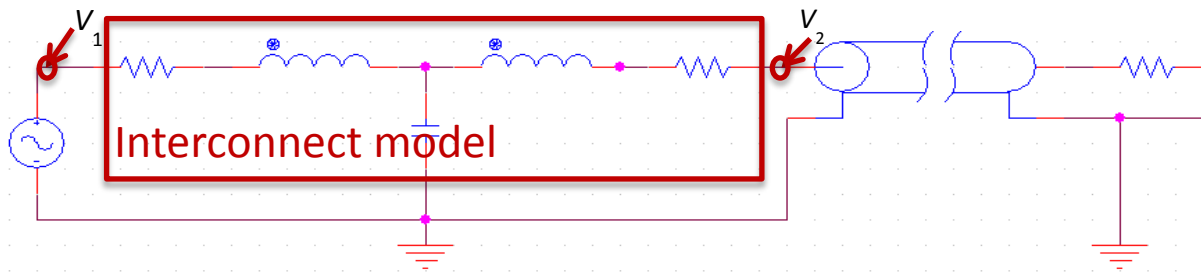
Figure 2.22. Interconnect model in Cadence.
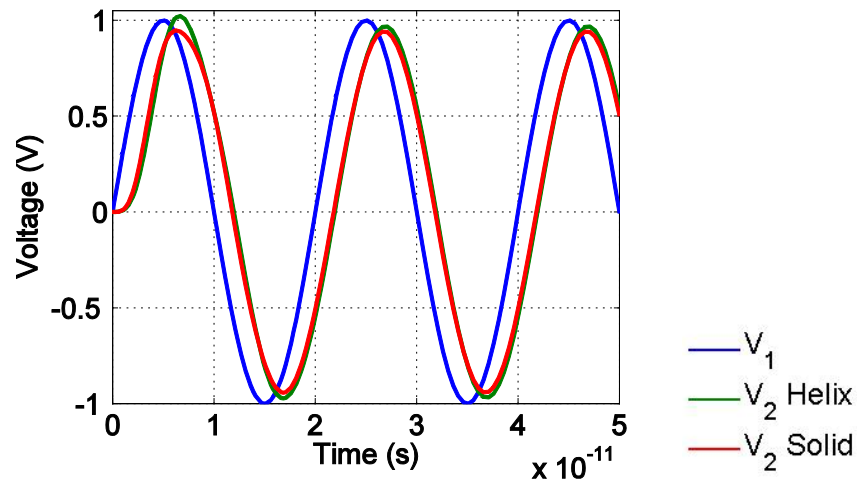
Figure 2.23. Transient performance of the interconnect simulated in Cadence.

Chapter 3
Carbon Nanotube Bump Interconnect

Carbon nanotubes (CNT) have been actively studied since their first observation in 1991 [26]. Due to their outstanding electrical properties, numerous potential applications in electronics have been proposed and investigated in the last two decades. However, the application of CNT in electronics is challenging, partially due to the difficulties in precisely placing and manipulating CNT [55]. Most of the current placement strategies can be categorized into two approaches: substrate growth of CNT arrays and deposition of CNT from solution. Substrate growth approaches include direct growth [37], [56], [57] and transferring direct-grown CNTs from another substrate [39]–[42], [58]. Solution deposition approaches include self-assembly of CNT directed by dielectrophoresis [59], [60] or magnetic field [61], spin or drop casting CNT solution onto a chemically modified substrate [62], [63] and inkjet printing [64].

The most common method used for CNT growth on substrates is chemical vapor deposition (CVD). By using CVD, CNT patterns are grown on predefined catalyst-seeded areas. One limiting factor of this method is a high processing temperature, typically greater than 700 °C to yield structures of high quality CNT [37], which is not compatible with conventional microelectronics and CMOS process flows. Transferring CNTs grown on another substrate can mitigate this issue at the expense of additional steps to deposit and reflow solder or conductive paste patterns which stick to and carry CNTs during transferring [39]–[42], [58]. Deposition of CNT from dispersion is another effective approach to fabricate CNT patterns,

and most of the recent work in this area focuses on fabrication of thin films of CNT [59]–[64]. Instead of CNT thin film, the work presented in this paper concentrates on solution-based fabrication of microscale CNT bumps with sufficient height range. In addition to fabrication of structures using CNT, this solution-based fabrication method can possibly be used to fabricate bumps composed of other nano/micro materials dispersed in liquid, for example Ag nanowires and graphene.

One possible use of the fabricated CNT bumps is for flip-chip interconnection. With the scaling and increasing number of inputs and outputs of IC devices, the dimensions of the interconnect structures are required to be increasingly smaller. Nanomaterials, such as carbon nanotubes, with superb physical properties may have the potential to replace current solder bump contact material and can provide means to form highly conductive interconnect structures. Since CNT is known to be a strong and flexible material, CNT interconnects have the potential to be flexible and stress decoupled, which is a useful characteristic for chips and substrates with non-planar surface and differing coefficient of thermal expansion (CTE). The distributed stress per length caused by CTE mismatch can be further reduced as the height of the CNT interconnects increases. CVD grown CNTs have been studied for flip-chip interconnects. However, either a high processing temperature [57] or additional transferring steps [41] are required. In this work we demonstrate the fabrication of CNT bumps using a solution based method, which can be performed at room temperature and is compatible with conventional microelectronics back-end of line (BEOL) fabrication and packaging processes.

The details of a solution-based fabrication process to produce CNT bump structures are presented in this work. Briefly, sodium dodecyl sulfate (SDS) was used as a surfactant to disperse CNT into deionized water. The CNT dispersion was then deposited from solution onto

a substrate with patterned photoresist and then allowed to dry. The excess CNT and photoresist were then removed, exposing the CNT bump structures, which are then ready for use. In this work, CNT bumps with a cylinder shape, a diameter of 200 µm and various heights are fabricated and characterized. We note that the height and shape of the CNT structure are controllable by controlling the thickness and pattern of the photoresist layer used in the process. Raman spectroscopy was employed to characterize the material composition of the CNT and SDS bump. CNT bump flip-chip interconnections were fabricated on a Kelvin structure for 4-point electrical resistance measurement. The average resistance of the CNT bumps (200 µm in diameter and 12 µm in height) was measured to be approximately 484 mΩ, which is comparable to the CNT bump resistance from other works using transferring CNT method [39], [40], [65], [66], after considering the influence of contact pad size, bump height and the used measurement method. A summary of fabrication parameters, measurement approaches and results of transferred CNT bumps from references is listed in Table 3.1, in comparison to this work. Furthermore, in order to study the mechanism that governs the electrical conduction in the CNT bumps, temperature dependent measurements were performed and fluctuation-induced tunneling (FIT) was found to be the most likely electrical conduction mechanism.

Table 3.1. A summary of fabrication parameters, measurement approcaches and results of

transferred CNT bumps

Ref.	Resistance per bump (Ω)	Contact pad size (μm^2)	Resistance × Area ($\Omega \cdot \mu m^2$)	Highest used temperature (°C)	CNT bump height (μm)	Measurement method
[40]	0.0056	3.14×10^6	1.76×10^4	240	90	4 point probe
[41]	100	2.5×10^3	2.5×10^5	150	56	2 point probe *
[65]	0.08	3.46×10^6	2.77×10^5	150	790	4 point probe
[66]	2.3	2.27×10^4	5.22×10^4	180	100	2 point probe†
This work	0.7	3.14×10^4	1.52×10^4	50	12	4 point probe

* No metal contact was deposited on the CNT bump before probe measurement, resulting in high contact resistance.
† The resistance of the daisy chain test structure is included in measurement.

The high frequency performance of solution deposited is also researched. The bumps have been fabricated on top of a coplanar waveguide (CPW) as flip chip interconnects. The CPW works as a test structure for high frequency characterization. DC measurement indicates that the CNT bumps have an average resistance less than 1 Ω. High frequency measurement was performed from 50 MHz to 40 GHz. Reasonably low reflection and insertion loss were measured, showing the potential of using CNT as flip chip interconnects.

3.1 Fabrication of CNT bump interconnects

3.1.1 CNT dispersion

The quality of CNT dispersion is critical for CNT film deposition. Sodium dodecyl sulfate (SDS) was used to assist in dispersion of CNT into deionized (DI) water. SDS and CNT were purchased from Sigma-Aldrich and Southwest Nanotechnology, respectively. CNT CG-200 was chosen in this work because the main component of CG-200 is single-wall nanotubes (SWNT) with high metallic nanotube content. For interconnection purpose, metallic CNTs are desired because of their high electrical conductivity. Other than storage of these materials in a nitrogen atmosphere, they were used as received.

SDS was added into DI water and stirred before adding CNT for 10 min to ensure complete dissolution. CNTs were then added to the solution and stirred for another 10 min. This quasi-dispersion was further dispersed using a tip sonicator (Misonix XL2020, power: 550 W, frequency: 20 kHz) with an amplitude of 40% for 60 min. To avoid overheating, the dispersion was placed in an ice bath and the ultrasonic vibration pauses for 5 s after every 5 s of working. After sonication, a 30 minute, 3000 rpm centrifugation step was performed to separate aggregates and precipitates from the dispersion. The supernate was carefully decanted and stored at approximately 10°C until it was used (described in the next section) in order to minimize aggregation. Before centrifugation, the SDS-assisted CNT dispersion had 0.2 wt% SWNT and 0.4 wt% SDS. After centrifugation, the concentration of materials in deionized water was marginally reduced because the SWNT and surfactant are well-dispersed and are minimally removed. The tip sonicator and well-dispersed CNT dispersion are shown in Figure 3.1.
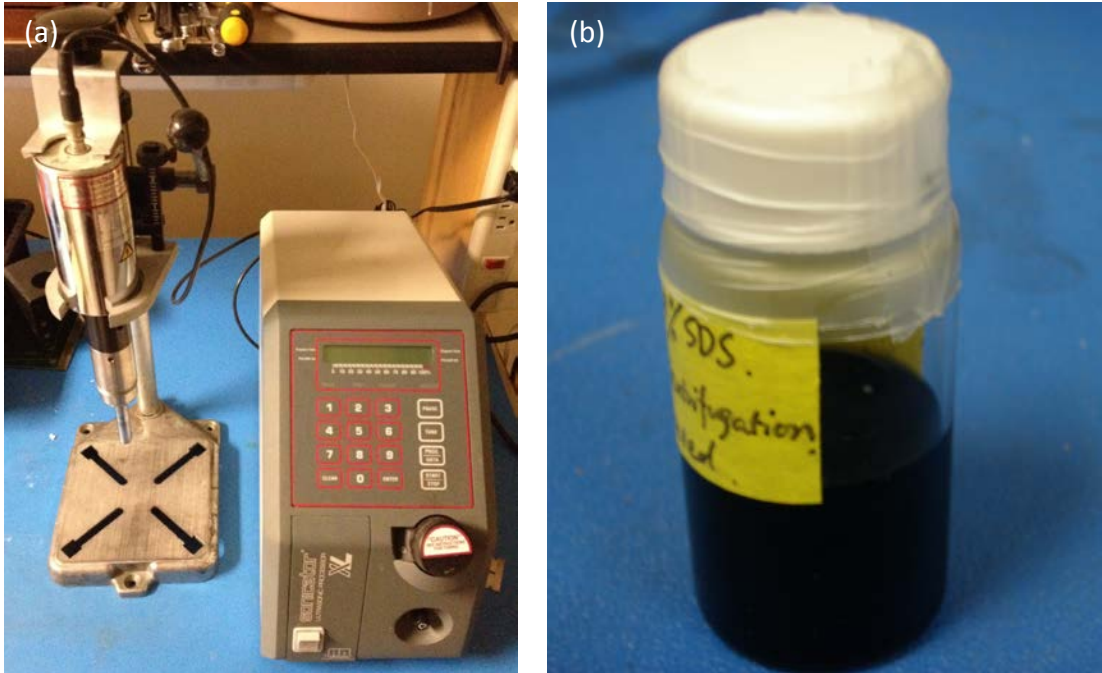
Figure 3.1. (a) Misonix XL2020 tip sonicator and (b) CNT dispersion

3.1.2 Solution-based CNT bumps fabrication

Figure 3.2 shows a schematic of the steps of the fabrication process to form CNT bumps onto a substrate with previously deposited and patterned metal (note that one representative bump is shown in this figure). AZ 4260 photoresist was spin coated, exposed and developed to define a pattern as illustrated in Figure 3.2(b). The patterned substrate is then placed into a liquid-tight frame, as shown in Figure 3.2(c). The previously described CNT dispersion was deposited to fill the cavity, as in Figure 3.2(d). Though the substrate was completely submerged into the CNT solution, the possibility exists that air bubbles were trapped in areas of the defined photoresist pattern where CNT bumps were to be formed. To release all the trapped air bubbles, the entire structure was placed into a vacuum system, which was then evacuated to approximately 5 kPa and then vented. This evacuation and venting process was

repeated three times to ensure removal of much of the trapped air in the structure. Next, the substrate was removed from the vacuum system and the CNT dispersion was evaporated in a vented box to form a CNT film, as shown in Figure 3.2(e). To accelerate the evaporation, the substrate was heated on a hotplate at 50 °C. A higher hotplate temperature may be used, but it should be able to keep the substrate temperature lower than the reflow temperature of the photoresist to avoid deformation of the photoresist.

We note that this method deposits CNT in the intended defined areas, as well as onto the surface of the photoresist. Therefore a two-step polishing procedure is followed after the dispersion evaporated in order to remove the CNT from the top surface of the photoresist and to allow removal of the photoresist while minimizing damage to the CNT bump structures. The two-step polishing process consists of a first polishing with P2400 sand paper until most of the photoresist was exposed. This is followed by a less aggressive polish using P4000 sand paper. This process removes the CNT from the surface of the photoresist and results in a reasonably smooth CNT bump surface as can be seen from SEM images. At the beginning of the polishing process, white powder-like material appeared on the sandpaper, indicating that the very top surface of the deposited material is likely composed of SDS. After approximately 1 second of polishing, black material showed up on the sandpaper, which is likely a mixture of CNT and SDS. More detailed analysis will be presented in the material characterization section. No water was applied onto the sand paper during the polishing process since water dissolves CNT-SDS bumps. This polishing process takes the chip from the step shown in Figure 3.2(e) to 3.2(f). Finally, the remaining photoresist is removed by washing with acetone and methanol, shown schematically as in Figure 3.2(g).

This fabrication process uses a conventional photo- lithography method to define patterns,

which enables the patterns to have relatively higher resolution compared to ink-jet deposition processes. The CNT bumps can be as tall as the photoresist, so the height of the CNT bumps can also be reasonably well-controlled by controlling the photoresist thickness. We note that in order to make the tall CNT bumps, sufficient CNT dispersion is needed; otherwise the center of the CNT bumps will be lower than the edges. In our case, to fabricate a 10 µm tall bump using the previously described CNT dispersion, the surface of the dispersion filled into the cavity (see Figure 3.1(d)) should be at least 1 cm in height above the surface of the photoresist layer. The water tight frame is shown in Figure 3.3.

The fabricated CNT bumps are shown in Figure 3.4. Figure 3.4(a) shows an array of CNT-SDS bumps fabricated on a gold pattern. The yield of the CNT bumps is high and less than 5% of CNT bumps were destroyed or moved from the predefined areas during the fabrication process. The yield may be further enhanced by improving the bump to metal adhesion. Additionally, since the polishing process was done manually, the uniformity of the bumps is not as high as desired and the shapes of the bumps slightly differ from each other. With better control of the polishing process, the uniformity of the CNT-SDS bumps is expected to be improved. Figure 3.4(b-d) are zoom views of CNT-SDS bumps of thickness approximately varying from 4 µm to 12 µm, fabricated with photoresist of similar thicknesses, demonstrating the feasibility of controlling bump height using photoresist thickness. We observe scratches on the top surface of the bump, which we believe are from the sandpaper polishing process and note that this indicates that finer/rougher sandpaper can be employed to further smoothen/roughen the top surface of the CNT bumps if necessary.

(a) Metallization

(b) Apply photoresist

(c) Install frame

(d) Fill with CNT dispersion

(e) Evaporate CNT
dispersion to form a film

(f) Polish CNT film to
expose photoresist

(g) Remove photoresist

Oxidized silicon wafer

Metallization layer

Photoresist

CNT dispersion

CNT film
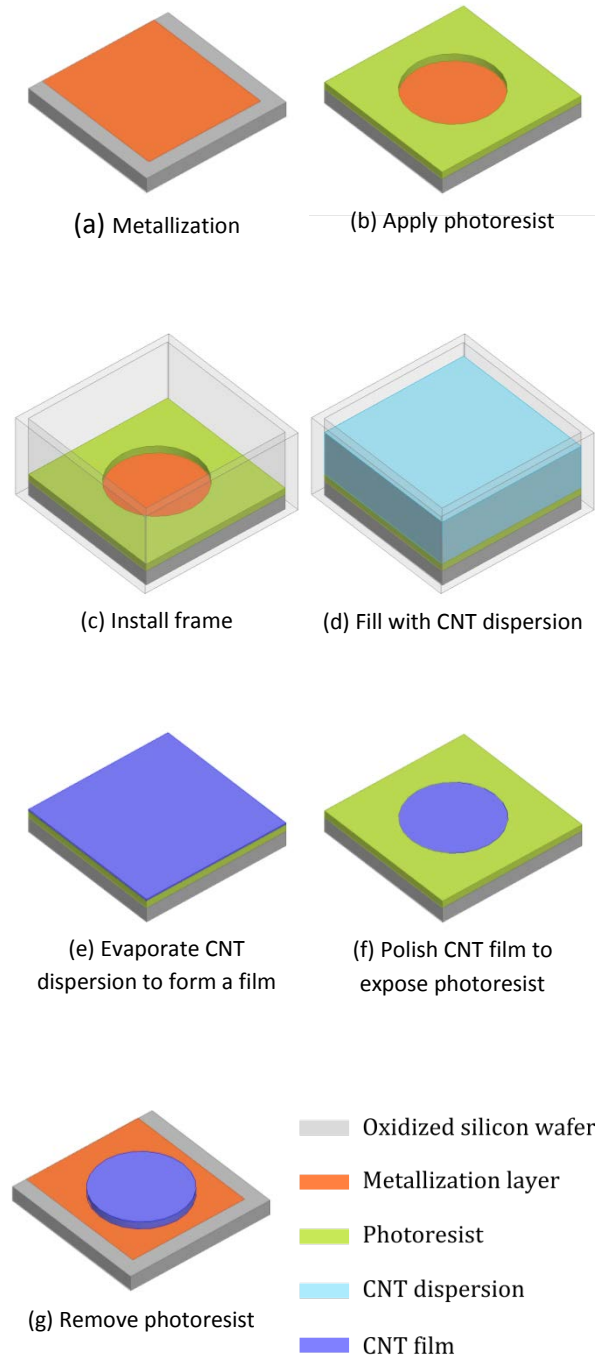
Figure 3.2. Representative schematic of solution-based CNT bump fabrication process.

Figure 3.3. Water tight frame for CNT bump fabrication.

(a)
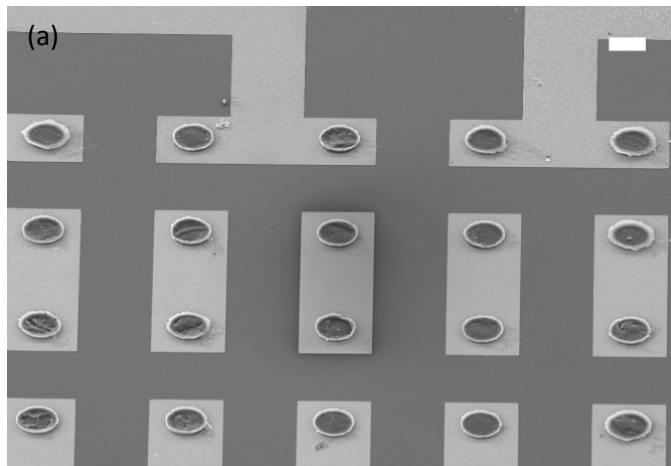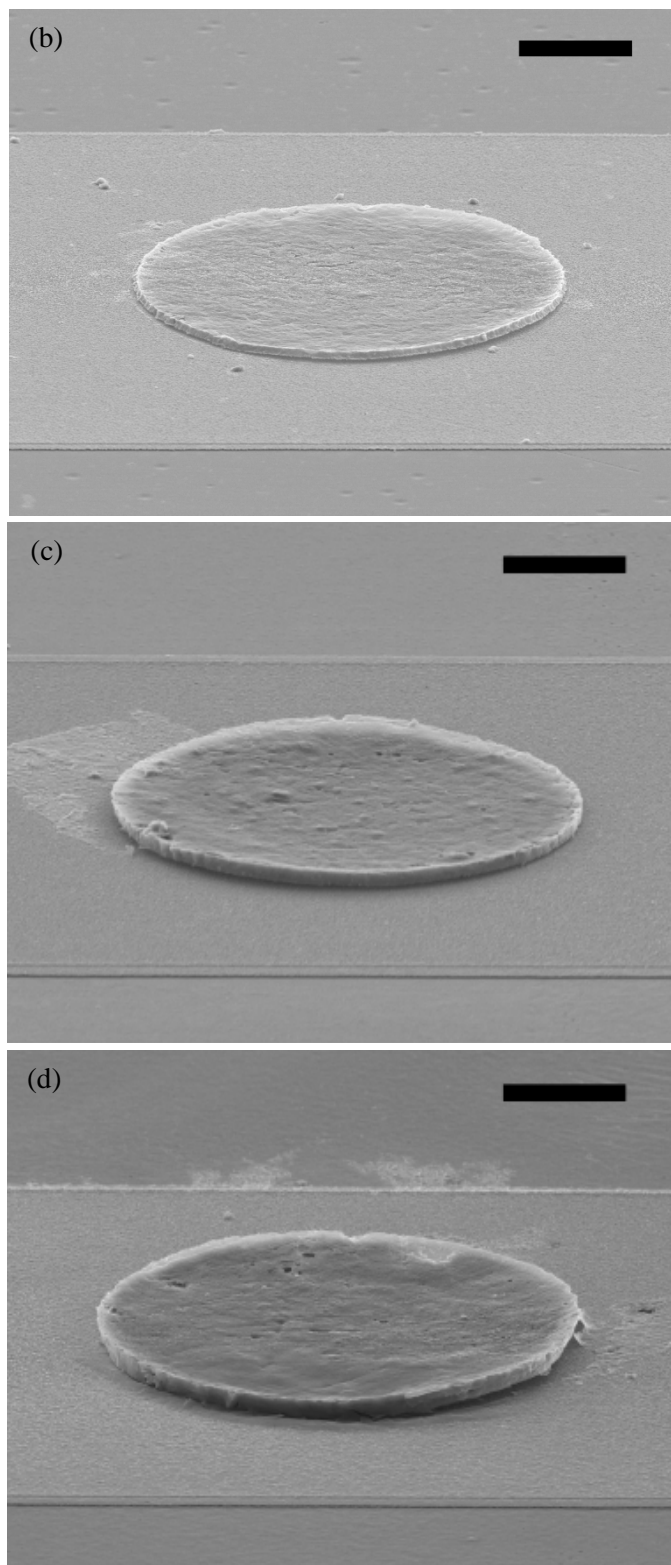
Figure 3.4. (a) Array of CNT-SDS bumps on a gold pattern. (b) 4 µm thick CNT-SDS bump. (c) 8 µm thick bump. (d) 12 µm thick bump. (Scale bar of (a): 100 µm, (b-d): 50 µm)

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3.2 Characterization of the CNT-SDS bumps

3.2.1 Material characterization

SEM images of the CNT-SDS bump were taken before and after polishing and photoresist removal, as shown in Figure 3.5. In Figure 3.5(a), we observe a relatively smooth surface and CNTs are barely observable before polishing and photoresist removal, confirming that the surface of the film was mainly composed of SDS. One plausible explanation for the formation of this SDS surface is that the unattached SDS is more soluble in water and less likely to aggregate compared to SDS that is attached to CNT. As a result, the unattached SDS is more probable to remain in the solvent in the drying process and thus it stays at the surface after the solvent completely evaporated. Figure 3.5(b) presents an SEM image of the surface of the CNT-SDS bump after polishing and photoresist removal. After the photoresist removal process, CNTs with SDS coating were observed.

Raman spectroscopy was used to confirm that the CNT bumps are not much affected by the fabrication process, as shown in Figure 3.6. A Raman spectroscopy system with an excitation wavelength of 441.5 nm was used. No appreciable peak shift and D band development was observed after the CNT-SDS bumps were polished and washed in acetone and methanol to remove photoresist, verifying that the mechanical polishing process minimally affected the chemical structure of the CNTs. The existence of single-wall carbon nanotubes (SWNT) was confirmed by the radial breathing mode (RBM) peaks that are characteristic for SWNT [67].
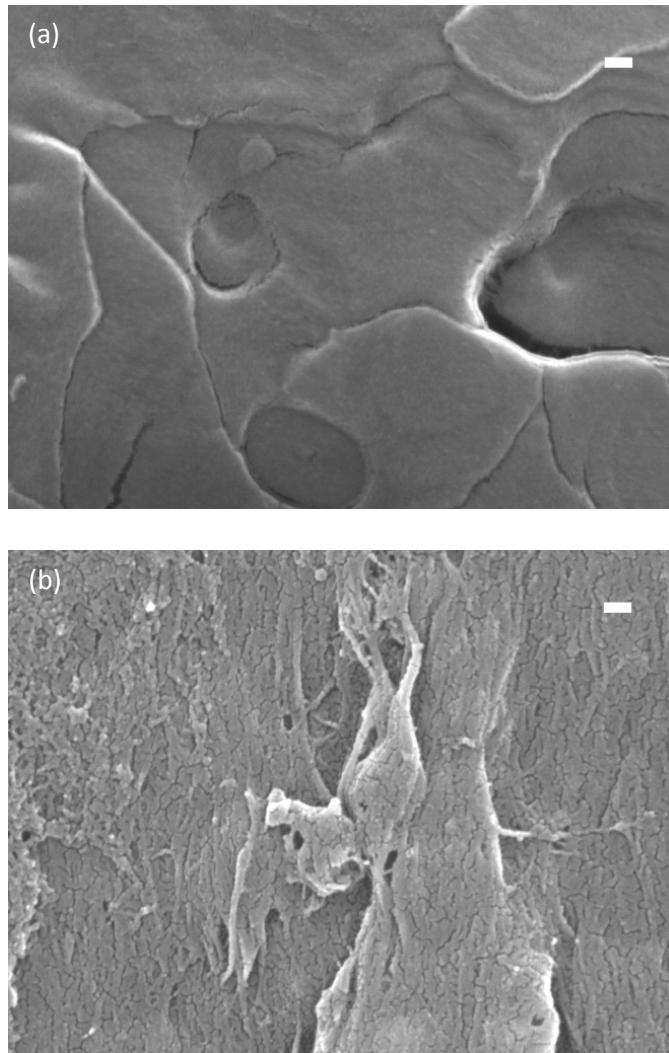
Figure 3.5. SEM images of CNT-SDS bump surface (a) before and (b) after polishing and

photoresist removal. (Scale bar: 100nm)
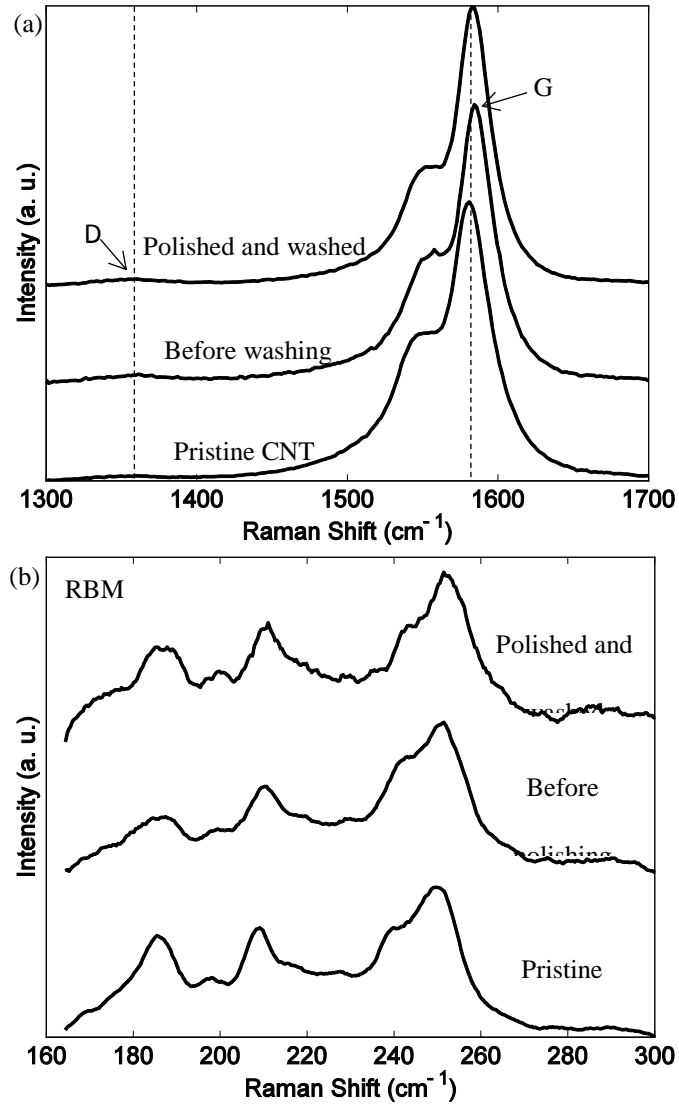
Figure 3.6. Raman spectra of CNT-SDS bump before and after polishing and photoresist

removal. Peaks are normalized. (a) G and D band. (b) Radial breathing mode.

3.2.2 Electrical characterization

In order for the CNT bumps to be used as flip-chip interconnects, their electrical resistance

need to be sufficiently low. To measure the resistance of the CNT bumps, Kelvin structures for

4-point probe measurement were fabricated, as shown in Figure 3.7. The Kelvin structure was assembled by flip-chip bonding a smaller chip on top of a larger one with matching metal patterns such that the CNT bumps (black-colored in Figure 3.7) are sandwiched between two metal strips (gold-colored in Figure 3.7). By forcing a current through two neighboring metal strips and measuring the voltage drop between the other two metal strips, the resistance of the CNT bump can be calculated by dividing the measured voltage drop by the forced current. Each bonded assembly contains four Kelvin structures, as shown in Figure 3.7. The four CNT bumps that were measured locate at the corners on the chip.

The fabrication steps of the Kelvin structures start with a glass wafer and electron beam deposited seed layer (50nm Ti and 100nm Au). AZ 9245 photoresist was patterned and 1 µm of Au was electroplated. The photoresist layer and the seed layers were then removed. Sequentially, another layer of photoresist was deposited to define a pattern for the CNT bumps. The wafer was diced and the CNT bumps were fabricated on the surface of the larger bottom chips. Epoxy (blue-colored in Figure 3.7) was then applied in the center of the four Kelvin structures as adhesive during flip chip bonding. The bonding load was set to 1 kg and the bonding temperature was set to 80 °C for 8 min to cure the epoxy.
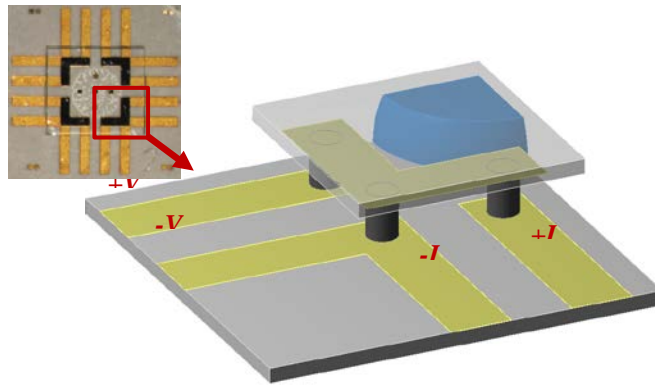
Figure 3.7. Schematic of the Kelvin structure used for 4-point probe measurement. Grey, gold,

blue and black represent the chips, metal strips, epoxy and CNT bumps, respectively.
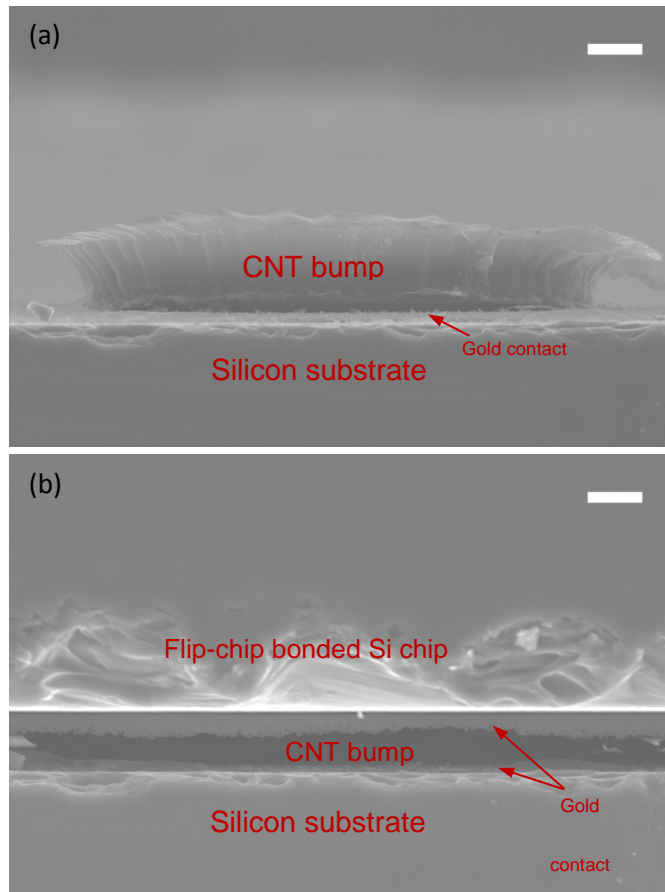
Figure 3.8. Side view of (a) CNT bump before flip chip bonding and (b) CNT bump after flip

chip bonding. (Scale bar: 10 µm)

Figure 3.8 shows side views of the same CNT bump close to the edge of a substrate before and after bonding. The CNT bump appears shorter after bonding, possibly because the bonding was able to press the non-uniformly raised areas on the perimeter of the top surface of the CNT bump down and make a more complete contact to the gold layer.

CNT bumps of various heights (4 µm, 8 µm and 12 µm) were fabricated and a Keithley 4200 semiconductor characterization system was used for resistance measurement. 12 samples of each height were measured and the results are shown in Figure 3.9. A big resistance variation from sample to sample was observed, possibly due to the difference of CNT bump surface uniformity. Some CNT bumps have non-flat top surfaces and the center of these bumps was significantly lower than their rough edges, possibly because too much pressure was applied during polishing or due to insufficient deposition of CNT-SDS dispersion, as shown in Figure 3.10. This leads to incomplete contact against the metal pads on the opposing chip and therefore a higher resistance because only the edge of the bumps was in contact with the other chip. Despite the large variation, all the measured bumps show linear I-V curves, indicating that a metallic CNT network forms in the bump, as shown in Figure 3.11. The contact resistance between the bump and the metal was roughly estimated to be 296.3 mΩ, by extrapolating the resistance data in Figure 3.9. The contact resistance is rather large presumably due to insufficient adhesion and work function difference between the CNT bumps and gold contact [68]. The average resistance of the 12 µm tall CNT bumps is approximately 484 mΩ, which translates to 1.52×104 Ωµm^2 (Resistance $\times$ Area), considering the bump has a 200 µm diameter.

Since the cross-bridge Kelvin structure has its limitation that the measured results become less accurate if the bridges have high resistance [69], it is important to verify the accuracy of

the measurement structure. The structure was modeled using a finite element analysis (FEA) tool ANSYS Workbench 14.5 (Electric Analysis). The metal strips used in this structure were 1 µm thick electroplated gold layers with a resistivity of 3 µΩ·cm and the CNT bump were modeled as a 250 mΩ resistor. The simulation result indicates the error of the measurement to be less than 1%. Since all the measured CNT bumps have a resistance higher than 250 mΩ, it is reasonable to assume that the measurement error due to the cross-bridge Kelvin structure is negligible.
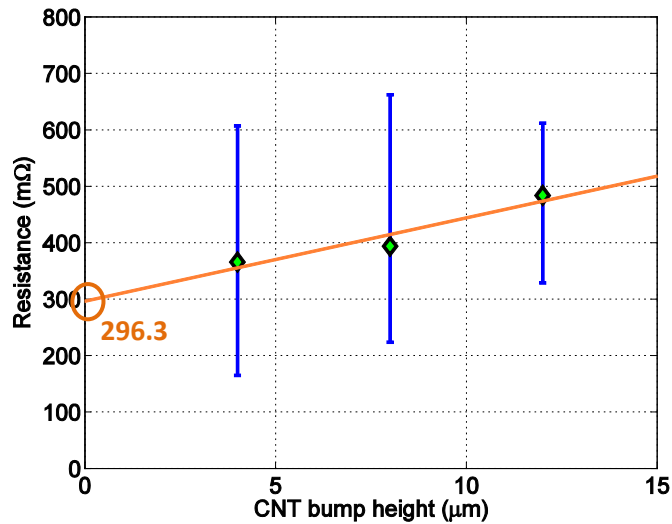
Figure 3.9. Resistance of the measured CNT bumps of different heights with the mean, minimum and maximum values.
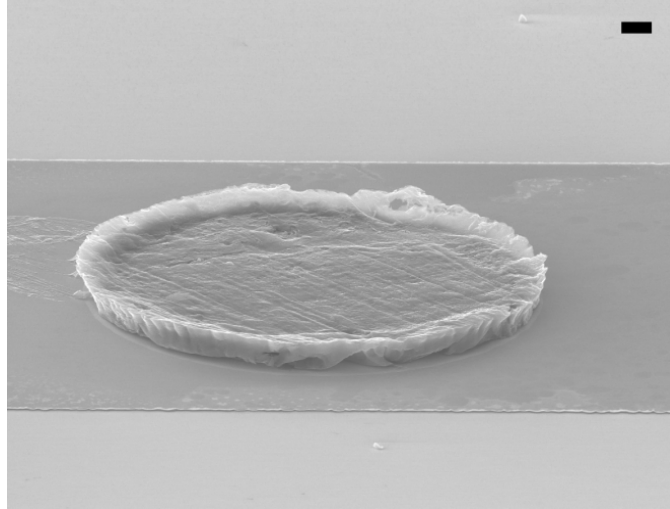
Figure 3.10. SEM image of a CNT bump whose edge is higher than its center. (Scale bar: 10 µm)
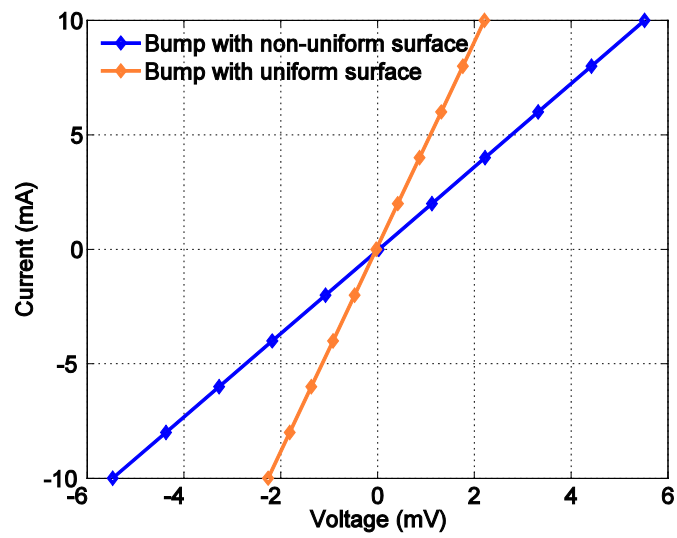
Figure 3.11. I-V curve of the measured CNT bumps.

3.2.3 Electrical conduction mechanism

The measured vertical resistivity of the CNT bump is 1.27 mΩ·m, which is 2 orders of magnitude higher than the reported lateral resistivity of a HiPCO CNTs film [70]. The anisotropy of the CNT film may contribute to this difference since the vertical and lateral resistivity of the CNT bump is different. However, it is unlikely to cause a discrepancy of 2 orders for a thick film even if all the CNTs are well aligned in one direction [71].

In order to explain this discrepancy, it is important to consider what contributes to the measured resistance. The electrical characterization performed using the cross-bridge Kelvin results in a resistance consisting of contact and bump resistance. To estimate the resistance contribution of the bump and extract the contact resistance, a 3 µm thick strip of CNT-SDS film was fabricated using the same solution based fabrication method as the CNT bumps. Silver paint was applied to provide good contact and four-point measurement was performed on the stripe to exclude contact resistance. The resistivity of the CNT-SDS film was calculated to be 11.46 µΩ·m, comparable to the reported resistivity of pure CNT network [70], despite the existence of the insulating SDS in the film. The low resistivity of the CNT film can be explained by the high percentage of metallic nanotubes used in this work and the close packing of the CNTs, as observed using the SEM.

Despite the anisotropy of the CNT film, the resistance of the bump without contact resistance can be roughly estimated using the resistivity of the CNT-SDS film to be 3.64 mΩ, which is negligible compared to the measured bump resistance. This suggests that the 2 orders discrepancy comes from the contact resistance. The estimation of the contact resistance in the previous section, though imprecise due to the large resistance variation, also indicates that the contact resistance plays an important role in the total resistance. The phenomenon of contact

resistance dominating CNT bump resistance is a common issue and can be explained by insufficient adhesion, small contact area and work function difference between the CNT bump and the gold contact [68].

In order to study the mechanism that controls the electrical conduction, the temperature dependence behavior of the dc conductivity was characterized. The Keithley 4200 semiconductor characterization system was connected to a cryogenic probe station (Advanced Research System PSF-10-1-4) and the resistance of the CNT-SDS bump and film was characterized as a function of temperature from 15 K to 395 K, as shown in Figure 3.12. It was seen that the measured resistance of the CNT bump was higher than the resistance estimated using the resistivity of the CNT-SDS film by 2 orders of magnitude over the entire temperature range.
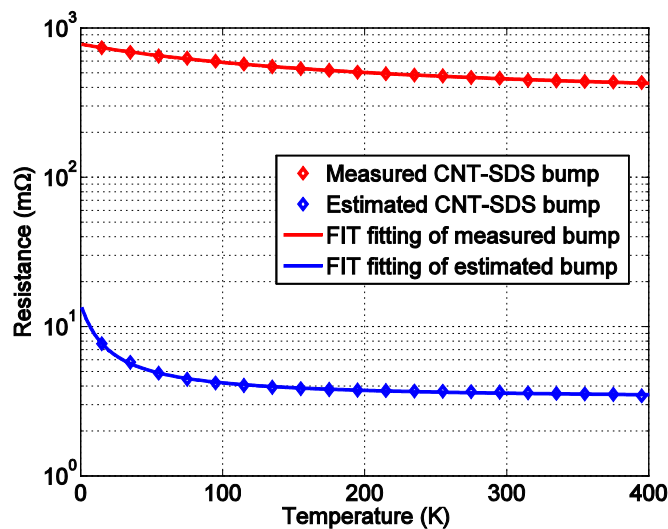
Figure 3.12. Temperature dependence of the resistance of the flip-chip bonded CNT bump interconnects. Note that the measured values include contact resistance and estimated values do not.

Since the CNT-SDS material shows a decrease of resistance as temperature rises, it can be inferred that inter-tube tunneling effect plays a more important role than intra-tube conduction in electron transportation [72]. Two models might be used for explaining this phenomenon.

Power-law transport mechanism model describes inter-tube and CNT to gold contact electron transport, assuming no insulating layers are in between. Considering that there might be small areas on the CNT surface with no SDS coating, it is possible to have such contacts, though the total area of such contacts might be comparably small. It has been known that electrons form a correlated ground state called the Luttinger Liquid (LL) in 1D metal [73] and power-law transport characteristics associated with the LL behavior have been observed in metallic CNTs [74]. Therefore the tunneling resistance in the linear-response regime is expected to vary proportionally to $T^{-\alpha}$ $(eV \ll k_B T)$, where α is a function of Luttinger parameter [72]. This model was used to fit the data. However, the curves were not sufficiently fitted, indicating that this mechanism plays a minor role in electron conduction.

An alternative model is called fluctuation-induced tunneling (FIT) [75]–[79]. This model essentially describes randomly distributed metal-insulator-metal (MIM) junctions with variable gaps of the insulating phases. Additionally, a 1D variable-range hopping (VRH) model can be used in combination, in order to account for the intra-tube metallic conduction involving the boost of conductivity at low temperatures where carrier backscattering is reduced [80]. However, since inter-tube resistance dominates the total resistance, it is reasonable to neglect the intra-tube resistance modeled using VRH [81].

Using the FIT model, the coatings of SDS on CNTs are considered insulating layers as parabolic shape potential barriers and electrical conduction happens when electrons tunnel through these barriers from tube to tube or from tube to gold contact. This model predicts the

following exponential relationship between the resistance and the temperature [75].

$$R = R_0 e^{T_1/(T+T_0)} \tag{3.1}$$

$$T_0 = 4\hbar S V_0^{3/2}/\pi^2 w^2 k_B e^2 \sqrt{2m} \tag{3.2}$$

$$T_1 = 2S V_0^2/\pi k_B e^2 w \tag{3.3}$$

In these expressions, S and w are the junction area and width. V_0, m and $\hbar$ are the height of the potential barrier, electron mass and reduced Planck constant, respectively. R_0 is the resistance at high temperature. This model fits well with the temperature dependent resistance data of both the measured and estimated CNT-SDS bumps as shown in Figure 3.12, indicating that SDS coating formed potential barriers in the bumps as well as on the contact region between the bump and the gold contact.

Since the CNT-SDS bump resistance minimally affects the measured resistance, the measured resistance approximates contact resistance and the estimated resistance can be considered to approximate the actual CNT-SDS bump resistance. The extracted T_0 and T_1 of the contact resistance are 247.1 K and 241.1 K, while that of the CNT-SDS bump are 20.86 K and 30.89 K. To understand the extracted T_0 and T_1 values qualitatively, it is helpful to examine the determining parameters S, w and V_0.

(1) Junction area S.

We assume that the junction area S of CNT to gold pad to be bigger than that of CNT to CNT, because the junction between CNT and gold pad is formed by a 1D tube and a 2D plane,

while the junction between tubes is 1D to 1D. The number of junctions is not accounted for in T_0 and T_1 and it plays a role in determining the prefactor R_0 [75].

(2) Junction width w.

The junction width w between CNT to gold is considered to be smaller since electron only needs to go through one layer of SDS to reach the gold contact as opposed to 2 layers of SDS in the case of electron transport from CNT to CNT.

(3) Potential barrier height V_0.

Metallic CNT and Au have similar work function. Therefore, the potential barrier heights V_0 are considered to be similar [68].

In brief, compared to CNT to CNT contact, CNT to Au contact has a bigger contact area, smaller junction width and similar potential barrier. Therefore, it is reasonable that their T_0 and T_1 values are much higher. This FIT reasonably describes the temperature dependence of the contact and bump resistance, therefore we believe it is the dominating mechanism of electrical conduction of the flip-chip bonded CNT-SDS bump interconnect.

3.3 High frequency performance of CNT bump interconnects

3.2.1 Design and fabrication of flip-chip CNT interconnects

The CNT bumps are fabricated at the end of a coplanar waveguide (CPW) as flip chip interconnects on a carrier (bottom chip). A die (top chip) with a matching CPW is flip chip bonded onto the carrier, as shown in Figure 3.13. The CPW was designed to have a characteristic impedance of 50 Ω. To compensate for the detuning effect due to the proximity of the die to the carrier, the width signal line of the die is reduced [82]. A glass substrate was used due to its low loss tangent. The gold CPW was fabricated by electron beam deposition of titanium and then gold seed layer, followed by gold electroplating. The metal lines have a thickness of approximately 3 µm. The CNT bumps were then fabricated using a solution based fabrication method, described in the previous sections. For comparison purpose, CPWs with gold bump interconnects were also fabricated. The gold bumps were fabricated to have geometry similar to the CNT bumps.

The scanning electron microscope (SEM) image of the fabricated CNT bumps is shown in Figure 3.14. The gold bumps are shown in the inset of Figure 3.14(a). The CNT bumps are well-shaped, though a few CNTs are out of the desired regions. As seen in Figure 3.14(b), the CNTs are densely packed despite small emptiness between CNTs is observed. The CNTs were coated with sodium dodecyl sulfate (SDS), which was used to assist dispersing CNTs into water. Since SDS is known to be highly resistive, the resistance of the CNT bumps can possibly be reduced if the SDS can be thoroughly removed after the fabrication process.

A load of 1 kg was applied onto the CNT bump interconnects in the flip chip bonding process. Since the CNT bumps are not capable of holding the die to the carrier, epoxy was applied next to the CPW for bonding purpose. Thus, the 1 kg load was distributed on the 6

CNT bumps as well as the epoxy. We note that the epoxy should have little impact on the performance of the structure since they are placed about 2 mm from the outer edge of the ground lines. For the gold bumps, a conventional thermo-compression bonding process was used. 60 Mpa of pressure was applied on the 6 gold bumps for 4 min while the die and carrier were heated to 180 °C and 300 °C, respectively. The fabricated structure with CNT bump interconnects is shown in the inset of Figure 3.15.
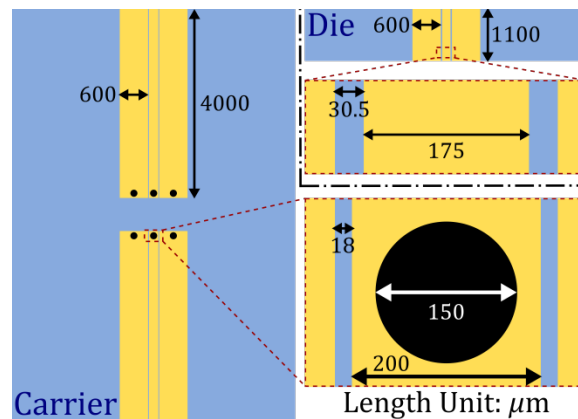
Figure 3.13. Carrier and die layout of 50 Ω gold CPW with CNT interconnects. Glass substrate, gold CPW and CNT interconnects are in blue, yellow and black, respectively.
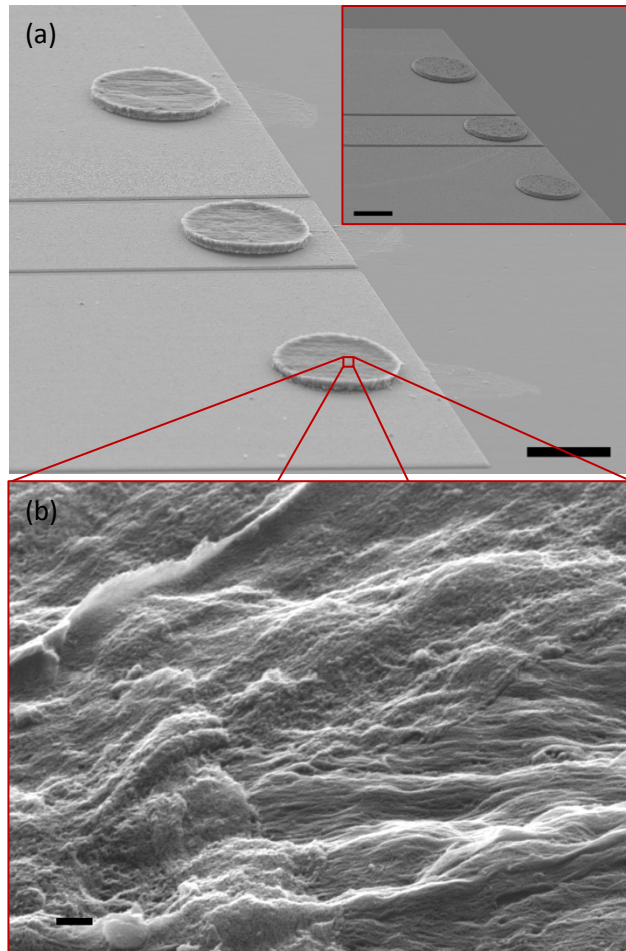
Figure 3.14. SEM images of the fabricated structure. (a) CNT bumps as flip chip interconnects on top of a CPW. Inset: reference gold interconnects. Scale bar: 100 µm. (b) Top surface of the CNT bump. Scale bar: 100 nm.
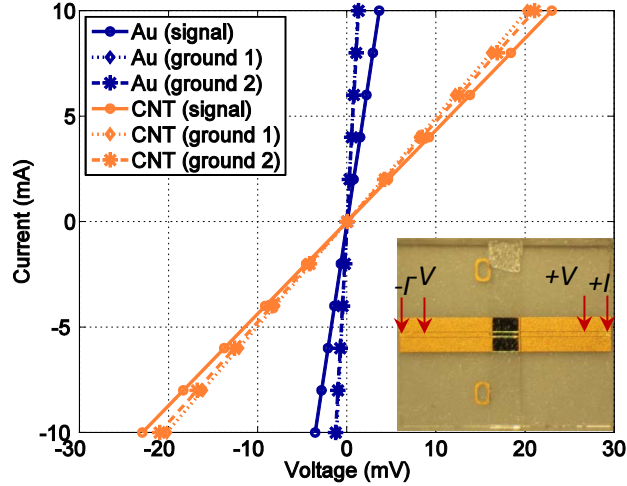
Figure 3.15. I-V curves of the signal or ground lines with CNT or gold interconnects. Inset:

optical image of the flip chip bonded CPWs with CNT interconnects.

3.2.2 High frequency characterization of flip-chip CNT interconnects

After the bonding process, DC resistance measurement of the ground and signal lines were carried out using a 4-point probe measurement, as shown in the inset of Figure 3.15. Current was inserted at the end of the metal lines and the voltage probes were placed approximately 0.5 mm from the current probes.

Therefore the measured resistance includes the resistance of the signal and ground metal lines, as shown in equation (3.4) and (3.5), where $R_{\text{m.CNT}}$ and $R_{\text{m.Au}}$ are the measured resistance of the lines with CNT or gold interconnects. R_{L} is the resistance of the metal line, which is assumed to be the same in (3.4) and (3.5) since the fabricated CPWs are from the same batch and have negligible difference. R_{CNT} and R_{Au} are the resistance of the CNT and gold bump interconnect, respectively.

$$R_{\text{m.CNT}} = R_{\text{L}} + 2R_{\text{CNT}} \tag{3.4}$$

$$R_{\text{m.CNT}} = R_{\text{L}} + 2R_{\text{CNT}} \tag{3.5}$$

The *I-V* curves of structures with CNT or gold bumps are shown in Figure 3.15. The ground lines have lower resistance than the signal lines due to the bigger line width. The resistance of CNT bumps can be estimated by subtracting (3.4) by (3.5). Since the resistance of Au bumps are negligible compared to the CNT bump resistance, R_{CNT} can be calculated by equation (3.6).

$$R_{\text{m.Au}} = R_{\text{L}} + 2R_{\text{Au}} \tag{3.6}$$

The average resistance of the CNT bumps is approximately 970 mΩ, which is more than one order of magnitude lower than the resistance of a 150×150 μm square-shape CNT interconnect fabricated using CVD, as described in [83]. The low resistance can be explained by the densely packed CNT bump as well as the high metallic content of the used CNTs. Compared to the transferred CVD grown CNT bumps in [39], [40], [65], [66], the solution deposited CNT bumps have similar "vertical resistivity" (resistance · area / height). The measured DC resistance of the CNT bumps is used in the high frequency simulation.

The high frequency performance of the fabricated structures was characterized using an Agilent N5227A PNA and 150 μm-pitch Cascade ACP65 GSG probes. A full two-port SOLT (Short-Open-Load-Through) calibration was performed to bring the calibrated reference plane to the probe tips. The structures were also simulated using ANSYS HFSS. All the parameters

used in simulation were obtained by measurement. The resistivity of the gold lines was measured using a Van der Pauw structure to be approximately 3 μΩ•cm. Since the surface roughness affects the loss of structure at high frequency, it is important to include the surface roughness into the simulation. In this work, Groisse surface roughness model was used. Atomic force microscopy (AFM) was used to determine the root-mean-square (rms) surface roughness to be approximately 120 nm.

Simulated and measured insertion and return loss of the structures are shown in Figure 3.16. Both structures (flip chip bonded CPW with CNT or gold interconnects) have return loss less than -20 dB up to 35 GHz and less than -15 dB from 35 GHz to 40 GHz. The CNT bumps have higher loss than gold bumps due to their higher resistance. However, the loss per transition of the CNT interconnect is only 0.3 dB higher than that of the gold interconnect, which is 1 dB less lossy compared to the CVD grown CNT interconnect in [83]. Furthermore, since CNTs have high kinetic inductance and therefore negligible skin effect, they are promised to have less loss than gold wires at high frequency [36].

For the CPW with gold interconnects, the simulation data matches well with the measurement data. However, for the CPW with CNT interconnects, the S-parameters are slightly mismatched. Two reasons might explain the difference. First, the gold bumps were fabricated using conventional gold electroplating which gives better control of the shape of the resulting structure. In contrast, a manual polishing process was involved in the fabrication of the CNT bump, which is damaging to the geometry of the bump. Second, the gold bumps were bonded to the opposing CPW on the die using thermo-compression whereas the CNT structure was bonded using epoxy applied next to the CNT bumps and the CNT bumps were merely pressed against the die. Therefore, the contact of the CNT bump to the opposing CPW is not as

good. Future work includes improvement of the fabrication process and the contact strategy of the CNT interconnects.
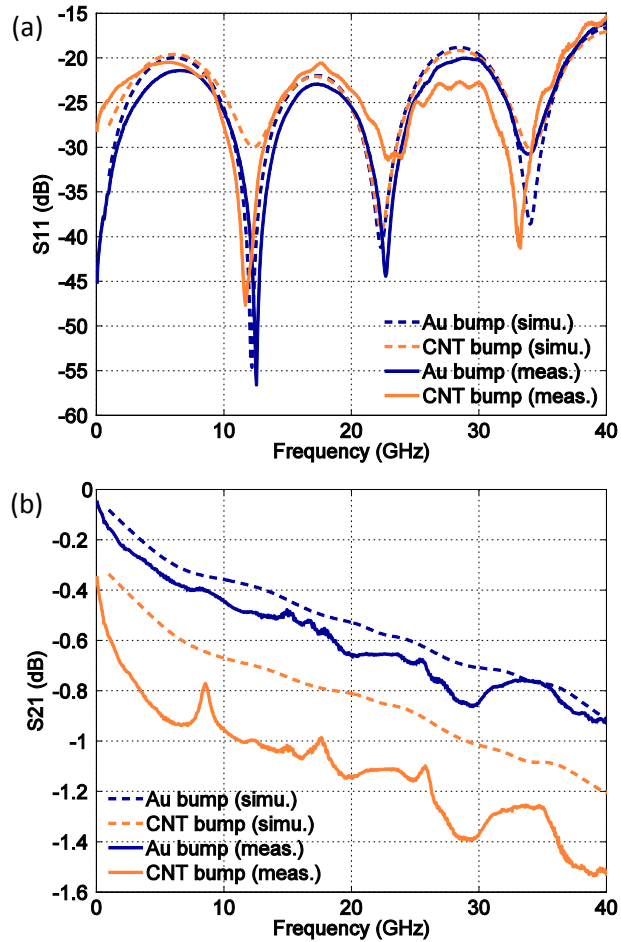
Figure 3.16. S-parameters of flip chip bonded CPW with CNT/Au interconnects. (1) S11 parameter. (2) S21 parameter.

Conclusion

Compliant interconnects are mechanically compliant and flexible interconnect structures that can potentially replace flip-chip bonded solder bumps due to compensation for the CTE mismatch between the silicon chip and the organic substrate. We designed, fabricated and characterized two different compliant interconnect structure. One uses compliant double helix geometry and the other one adopts carbon nanotube as a compliant material for interconnect purpose.

MEMS-based compliant double helix interconnects made using sequential steps of electroplated Cu have been fabricated and characterized. The structure provides a resistance of approximately 35 ± 15 mΩ, using a pressure contact and without optimization of the electrical contact surfaces. Measurement results correspond to simulated electrical and mechanical performance, allowing a reasonable level of predictability of the performance of modified double helix structures. The double helix interconnect structures are highly reworkable with a consistent resistance over 50 remating cycles. The high frequency performance of compliant double helix interconnect is simulated and measured. The measured insertion and reflection loss were less than -0.6 dB and -15 dB, respectively. The structure shows potential to replace or augment conventional flip-chip bonded solder bumps for implementations requiring compliance or reworkability.

A solution-based fabrication process has been developed to produce CNT bump structures at room temperature. The process uses photolithographically defined photoresist patterns as stencils and therefore gives relatively high resolution (micrometer scale) and controllable CNT bump height. The fabrication process negligibly influences the chemical structure of the CNT used to form the bumps. Compared to a CVD growth method and CNT transfer technique, this approach does not require high fabrication temperature or additional CNT handling and transferring steps. Electrical characterization of these bump structures have been performed. In summary, cylindrical bumps of CNT with a diameter of 200 µm and a height of approximately 12 µm were fabricated using a solution-based fabrication and electrically characterized to demonstrate an average resistance of 484 mΩ. Using temperature dependence measurements, fluctuation- induced tunneling was identified as the main electrical conduction mechanism. The CNT interconnect provides a return loss lower than -15 dB up to 40 GHz and an insertion loss only 0.3 dB higher than conventional gold interconnects. Due to the negligible skin effect of CNT, CNT interconnects have the potential to be used in future higher frequency applications.

Future Work

In this work, we researched double helix structures as structurally compliant interconnect. We focused on the electrical, mechanical, reworkability and high frequency performance of the interconnects. However, the scope of off-chip interconnects research is a rather broad and there are several other aspects to be explored. First, off-chip interconnects reliability is critical to the durability of a package. Reliability tests including shear test, humidity test, thermal cycling test, etc. of the double helix interconnect can be performed to explore the reliability of the interconnects. Additionally, the reworkability of the double helix interconnects can be further explained, since the high frequency performance of interconnects after reworking is another interesting subject for research.

As the first work describing solution based deposition process of carbon nanotube bump interconnects, we showed the feasibility of using these CNT bumps as interconnects and their high frequency performance. Various improvement, measurement and optimization strategies are available and will be considered in the future studies. One of the issues of the CNT interconnects is their higher resistance compared to conventional solder interconnects. We believe this is caused by the SDS dielectric coating on CNT and contact resistance between gold CPW and CNT. Possible methods to improve the performance of the bumps include more thorough removal of SDS, better work function match by doping the CNT bumps with metallic nanoparticles or adding a transition layer between CNT and gold contact. The addition of a

transition layer between CNT and gold contact may also enhance the adhesion of the CNT to the gold.

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