PACKAGING OF SILICON CARBIDE HIGH TEMPERATURE, HIGH POWER

DEVICES - PROCESSES AND MATERIALS

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_____

Yi Liu

Certificate of Approval:

_____

John Evans
Associate Professor
Industrial and Systems Engineering

_____

R. Wayne Johnson, Chair
Samuel Ginn Distinguished Professor
Electrical & Computer Engineering

_____

Thomas A. Baginski
Professor
Electrical & Computer Engineering

_____

Stuart M. Wentworth
Associate Professor
Electrical & Computer Engineering

_____

Stephen L. McFarland
Acting Dean
Graduate School

PACKAGING OF SILICON CARBIDE HIGH TEMPERATURE, HIGH POWER DEVICES - PROCESSES AND MATERIALS

Yi Liu

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PACKAGING OF SILICON CARBIDE HIGH TEMPERATURE, HIGH POWER DEVICES - PROCESSES AND MATERIALS

Yi Liu

_____
Signature of Author

_____
Date of Graduation

VITA

Yi Liu, son of Yucheng Liu and Yufang Zhou, was born in March 10, 1973 in Jilin, P.R.China. He attended Tianjin University in September 1991 and graduated with a Bachelor of Science degree in Mechanical Engineering in July 1995. After working as a mechanical engineer in Tianjin Yizhong Vehicle Safety Belt Factory for two years, he entered the Graduate School, Tianjin University in September 1997. He received the Master of Science degree in Mechanical Engineering in March 2000. Then he worked at Tianjin Assembly and Test Factory, Motorola China Inc. as a process engineer. In August 2001, he joined Ph.D. program of the Department of Electrical and Computer Engineering, Auburn University.

DISSERTATION ABSTRACT

PACKAGING OF SILICON CARBIDE HIGH TEMPERATURE, HIGH POWER DEVICES - PROCESSES AND MATERIALS

Yi Liu

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Silicon carbide (SiC) has unique electrical, thermal and physical properties compared to the Si and GaAs conventionally used in microelectronics as it can operate in the temperature range from 350ºC to 500ºC. However, there is a lack of reliable packaging techniques and materials for SiC, in particular substrates, die attach, die metallization and die passivation that can survive temperatures as high as 500ºC.

Direct bond copper (DBC) Al_2O_3 substrates in which a thick Cu foil is cladded on Al_2O_3 has been used for power electronics for many years because of its acceptable heat dissipation capability, high current carrying capability, low coefficient of thermal expansion (CTE) and high mechanical strength. AlN has a very high thermal conductivity and a CTE approximating that of SiC (AlN = 4.5ppm/°C vs. SiC = 4.4ppm/°C [1]).

However, with thick Cu metallization, the AlN is prone to fracture during thermal cycling due to its low flex strength and fracture toughness [2]. While Si_3N_4 does not have the thermal conductivity of AlN (Si_3N_4= 60W/m•K vs. AlN= 170-250W/m•K), the high fracture toughness of Si_3N_4 (2.4X AlN) allows thick Cu metallization and provides better thermal cycling performance.

Die attach is another key issue for high temperature operation. This study examined a transient liquid phase bonding technique using eutectic Au-Sn braze with a thick Au (20μm) layer electroplated on the DBC Al_2O_3 substrate. After brazing and annealing at 400ºC, the Sn from the eutectic preform diffused into the substrate Au, lowering the Sn concentration to less than 10% and raising the braze joint melting point to over 400ºC. Au-Ge and Au-Ge-Ag braze alloys were also evaluated.

Die metallization plays a role as an adhesion layer and diffusion barrier. It should not degrade during high temperature storage. A sputtered thin film stack of Ti/Ti-W/Au was examined to assess its performance, including its stability during high temperature storage.

In high voltage applications, insulation is required to prevent the breakdown of SiC device passivation or arcing around the edge of the die. Phthalonitrile and polyhedral oligomeric silsesquioxanes (POSS) nanoreinforced polyimides were characterized as high temperature high voltage passivation materials. Ceramic capacitors, one of the passive components needed in a power electronics module, were also examined for high temperature applications up to 300ºC.

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CHAPTER 1

INTRODUCTION

1.1 SiC Properties

Silicon has long been the dominant semiconductor material because of its major processing advantages: it can easily be oxidized to form silicon dioxide, which is not only a high-quality insulator but also an excellent diffusion barrier layer. GaAs is another widely used semiconductor material which has found many applications in analog and digital devices that require very high frequency operation. However, both Si and GaAs have relative narrow band gaps (the energy difference between the conduction band minimum and valence band maximum) which limit their applications in harsh environments. Wide bandgap semiconductors (SiC, GaN, etc.) are currently moving out of the laboratory into real world applications. The commercialization of SiC that started a decade ago has accelerated over the past few years. The improvements made in SiC semiconductor device technology for power electronics and optoelectronic applications are partially due to the commercial availability of SiC substrates of ever-increasing diameter and quality [3]. SiC offers unique electrical and thermophysical properties compared to Si and GaAs, these include [4]:

1. Wide bandgap. SiC can operate at extremely high temperatures without suffering from intrinsic conduction effects because of its wide energy bandgap. 4H-SiC has an intrinsic temperature of 1650°C for an extrinsic doping level of $10^{16}cm^{-3}$.

Another advantage of the large bandgap is the negligible leakage current up to 400°C [5]. Also, this property allows SiC to emit and detect short wavelength light which makes the fabrication of blue LEDs and UV photodetectors possible.

2. High critical breakdown electric field. With a higher breakdown electric field, SiC power devices can be designed to have $1/10^{th}$ of the thickness of equivalent silicon devices and with more than 10 times higher doped voltage blocking layers. For the majority carrier modulated devices such as power Schottky diodes and MOSFETs, $1/10^{th}$ the blocking layer thickness combined with 10 times the doping concentration can give SiC devices a factor of 100 advantage in resistance over that of the analogous Si majority carrier devices. For the minority carrier modulated devices such as PiN diodes, BJTs, and thyristors, a $1/10^{th}$ blocking layer thickness can yield a 100 times faster switching speed compared to the Si devices [6].
3. High saturated electron velocity. This property enables SiC microwave devices to operate at higher cut-off frequencies.
4. Significantly higher thermal conductivity. This allows enhanced thermal management for high power devices. Heat flows more readily through SiC than through other semiconductor materials, which enables SiC devices to operate at extremely high power levels while still dissipating a large amount of heat.

Silicon carbide (SiC), aluminum nitride (AlN), gallium nitride (GaN), boron nitride (BN), and zinc selenium (ZnSe) are wide bandgap materials that are now under development for high temperature, high frequency applications. However, SiC offers several advantages over other wide bandgap materials including the commercial

availability of the substrate, well understood device processing techniques, and the ability to grow a thermal oxide for use as a mask during fabrication, device passivation layers and gate dielectrics [7].

In addition to the SiC substrate providing the basis for SiC homoepitaxial device structures, SiC substrates are used for heteroepitaxy of GaN device structures, due to the close lattice match to GaN and excellent thermal conductivity. The properties of common semiconductor materials are presented in Table 1-1 [3].

Table 1-1 Properties of semiconductor materials [3]

Materials / **Properties**	**GaN**	**4H- SiC**	**6H- SiC**	**Si**	**GaAs**
Thermal conductivity (W/m•K)	130	490	490	130	50
Bandgap (Ev)	3.44	3.2	3.0	1.12	1.42
Saturated electron velocity (10^7 m/s)	2.7	2.0	2.0	1.0	2.0
Electron mobility (cm^2/V•s)	900	1000	600	1450	8500
E_b (Mv/cm)	12.2	9.7	10	11.8	12.8
Lattice constant (Å)	3.189	3.073	3.081	3.94	4.00

1.2 SiC Processing

Silicon carbide has more than 170 polytypes, the most common of which are cubic 3C-SiC, also referred to as β-SiC, the hexagonal 4H-SiC and 6H-SiC (α-SiC), and the rhombohedral 15R-SiC structures. These polytypes are differentiated by the stacking sequence of the biatom layers of the SiC structure [3]. Although 4H-SiC and 6H-SiC are commercially available, 4H-SiC is preferred over 6H-SiC because it has a higher and more isotropic electron mobility compared to 6H-SiC [5].

1.2.1 SiC Crystal Growth

Most single crystal semiconductor boules are grown by crystal pulling or seeded solidification from a melt composed of Si or Ge, or from compound semiconductors, such as GaAs. However, it is impractical to manufacture industrial quantities of monocrystalline SiC using these methods because of the thermodynamic properties of SiC. The SiC phase diagram exhibits a peritectic reaction at 2830°C with a total pressure of ~10^5Pa, calculations also indicate that the stoichiometric melting occurs only at pressures exceeding 10^5atm and temperatures above 3200°C [8]. It is possible to create extreme growth conditions such as this for small diamond boules, but such conditions are currently not feasible for commercial production of large diameter semiconductor grade SiC [3].

Large diameter SiC crystal growth technology has evolved from the original SiC sublimation method first developed by Lely [9] and lately modified as a seeded sublimation technique, physical vapor transport (PVT) process by Tairov and Tsvetkov [10]. This latter method has been further refined for the production of large diameter SiC boules, and various modifications of these techniques are now used at many laboratories worldwide [3].

In order to reduce the cost of SiC devices and gain the advantages of Si and GaAs device infrastructures, a large amount of effort has been given to grow high quality, large diameter SiC substrate materials [3]. Recently, 3 inch 6H and 4H SiC substrates have been offered commercially by Cree, Inc., and 4 inch 6H and 4H SiC substrates are under development.

1.2.2 SiC Defects

Defects in SiC include: 1) open-core dislocations (called micropipes); 2) low-angle boundaries; and 3) conventional dislocations [3]. Micropipes have been the main factor preventing the commercialization of many types of SiC devices. Several mechanisms have been identified as causing micropipes, including the seed surface quality, the growth process stability and cleanliness, and the specific parameters controlling nucleation density and growth rate. Recent developments in fabrication techniques have decreased the density of micropipes to 0.9 pipes/cm^2.

Low-angle boundaries near the crystal periphery caused by unoptimized process conditions are visible to the naked eye and sometimes extend through the entire thickness of the wafer. Recent efforts have result in substrates of up to 4 inch without low angle grain boundary defects [3]. Figure 1-1 shows these common SiC substrate defects [11].

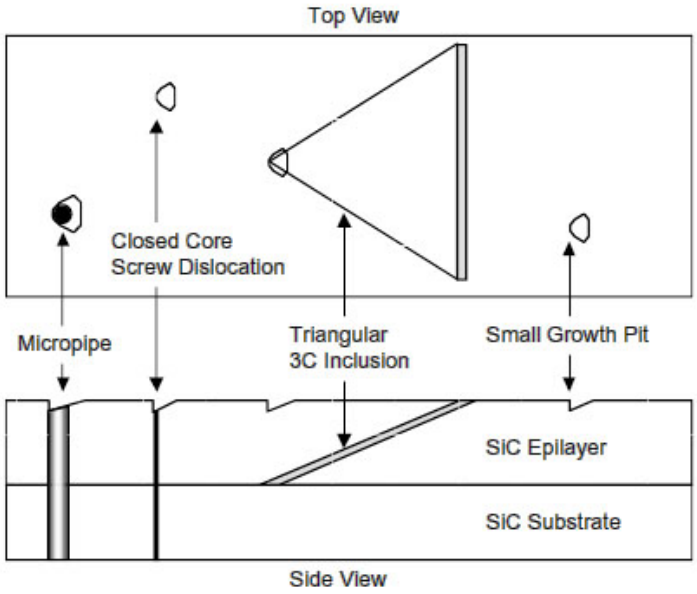


Figure 1-1 Common SiC defects [11]

1.2.3 SiC Doping

Epitaxial growth is used to deposit high quality active device layers. Ion implantation is often utilized for doping profiles, but epitaxy is required to form the starting material. Implants directly into substrates have generally been of poor electrical quality [12]. However, implantation is used for selective area doping because dopant diffusion is not feasible due to the high temperatures required. Both n-type and p-type doping have been achieved for SiC during vapor phase epitaxy (VPE). Dopants for n-type SiC include N, P, As and B; Al and Ga can be p-type dopants, with Al being the most common. Undoped SiC is typically n-type because of residual nitrogen. Both the n-type and p-type doping density of 4H and 6H SiC can be adjusted between 10^{14} and 10^{19} cm^{-3}.

1.2.4 SiC Etching, Dicing and Polishing

Wet etching of SiC is relatively difficult due to its high bonding energy which requires molten KOH at 450°C. Instead, reactive ion etching (RIE) has been found to be an effective dry etching method. For wafer slicing, a diamond abrasive cutting tool can be used. A diamond based polishing regime can be used for wafer polishing. However, it is often preferable to use an RIE treatment in order to remove residual subsurface damage, which is detrimental to the subsequent SiC epitaxial process [13]. Chemical mechanical polish (CMP) removes material at an even slower rate and is used for final processing after diamond slurry polishing. An RIE treatment followed by a CMP can significantly reduce subsurface damage [14].

1.2.5 SiC Contacts

All semiconductor devices have contacts and all contacts exhibit contact resistance, thus it is important to characterize the contact resistance. Contacts are

generally metal-semiconductor contacts. The first widely accepted theory for metal-semiconductor contact was developed by Schottky in the late 1930's [15]. True ohmic contacts exhibit a straight line current-voltage characteristic with a low value of resistance. The contacts must be able to supply the necessary device current, but at the same time the voltage drop across the contact should be small compared to the voltage drops across the active device regions, and the contact should not inject minority carriers. For high temperature, high power devices, an ohmic contact should not degrade under extreme conditions.

One of the primary uses of Schottky contacts on SiC is in efficient, solid state, high-voltage switching applications [16]. Most of the elemental metal layers deposited on n-type SiC exhibit a Schottky contact with a high barrier height in the as-deposited condition. Pt, Au, Ag, Ni, Cr and Al sputtered on n-type SiC produce a rectifying contact [17], while Au, Al, Ag, Ti and Ni form a Schottky contact on p-type SiC. Barrier heights on p-type SiC tend to be higher than those on n-types [18].

Many metals form Schottky contacts in the as-deposited form, but a short-term (2 minutes), high-temperature (>900°C) anneal can convert the Schottky contact to ohmic. After high temperature annealing, metals that form some kind of silicide. Ni, Ni/Cr, Co and Ti are widely used for the fabrication of ohmic contacts. The lowest reported value of contact resistivity to n-type SiC was less than $1x10^{-6}$ $\Omega \bullet cm^2$ [19]. It is difficult to form ohmic contacts for a p-type substrate because of the large band gap and work function of SiC. Al/Ti contacts are commonly used for p-type ohmic contact, being deposited either subsequently or simultaneously [20-22]. Spieb et al. [21] fabricated Al/Ti ohmic contacts

for p-type 6H-SiC with specific contact resistance values ranging from $5x10^{-6}$ Ω•cm^2 to $5x10^{-3}$ Ω•cm^2.

Contact resistance measurement techniques fall into four main categories: two-contact two-terminal, multiple-contact two-terminal, four-terminal and six-terminal methods. The transmission line method (TLM) is widely used to characterize ohmic contacts. A TLM test structure and a plot of total resistance as a function of contact spacing are shown in Figure 1-2 [22]:

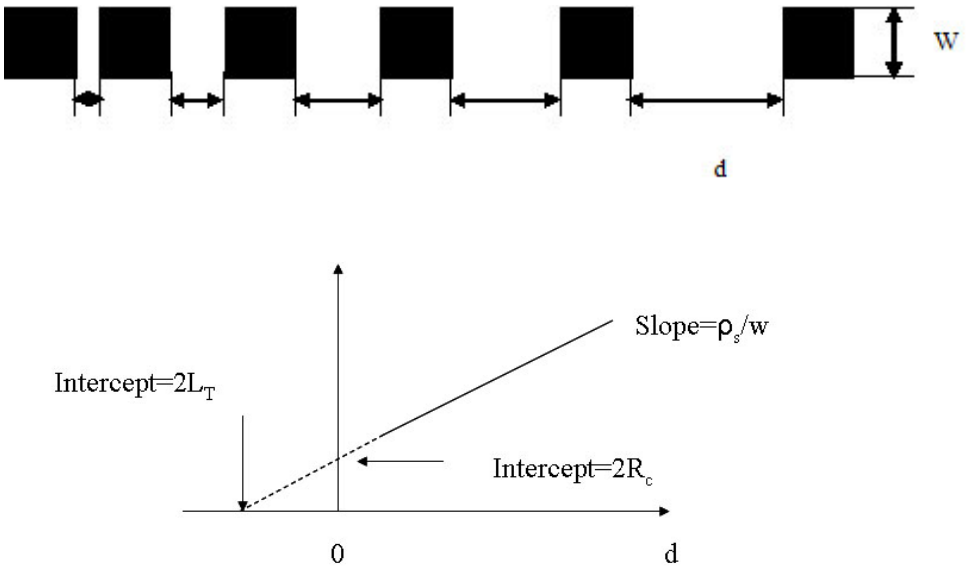


Figure 1-2 Total resistance as a function of d

Total resistance between any two adjacent contacts is expressed by:

$$R_T = \frac{\rho_s \times d}{w} + 2R_c \qquad (1.1)$$

- The slope ρ_s / w describes the sheet resistance
- The intercept at d =0 is R_T =2 R_c , giving the contact resistance

The transmission line model thus gives a complete characterization of the contact by providing both the semiconductor sheet resistance and the specific contact resistance.

1.3 SiC High Temperature, High Power Devices

Most traditional silicon integrated circuit devices are not suitable for applications at temperatures above 250°C. At low operational temperatures, the intrinsic carriers are negligible compared to the doping concentration, but the number of intrinsic carriers exponentially increases with temperature, which results in unacceptably high junction reverse leakage currents [23]. Eventually the semiconductor device operation is overcome by uncontrolled leakage current. SiC devices, however, can operate above 350 °C because of their higher bandgap energy, which requires greater energy to excite the electron from the valence band into the conduction band. High temperature devices operating from 350°C-500°C are in great demand for aerospace applications, nuclear power instruments, satellites, space exploration, geothermal wells and sensors. Table 1-2 shows some typical high temperature applications and technologies [24].

A variety of SiC devices has been demonstrated, including p-n junction diodes, Schottky diodes, bipolar junction transistors (BJTs), insulated gate bipolar transistors (IGBTs), MESFET, JFET and thyristors. MOSFETs with lifetimes of >700 years at 2 MV/cm and 350°C have been reported [25]. SiC has the potential to replace Si diodes and Si insulated gate bipolar transistors (IGBTs) because the on-state and switching losses are drastically reduced in SiC [26]. A 4H-SiC Schottky barrier diode (1400V) with a forward current density of 700 A/cm^2 at 2V has been demonstrated, and packaged SITs have produced 57W of output power at 500MHz [27]. Additionally, heterojunction devices such as the heterojunction FET (HFET) and heterojunction bipolar transistor (HBT) have been proposed and fabricated [28]. SiC bipolar junction transistors typically have low current gain in the common emitter mode due to minority carrier recombination

in their npn structures [29]. Heavily doping the emitter does not produce any significant improvement of the current gain due to the effect of bandgap narrowing (BGN). However, heterojunction structures using wide bandgap emitters or III-V nitride semiconductors may be able to improve the current gain and high-frequency response [7].

Table 1-2 High temperature applications [24]

High Temperature Applications	**Peak Ambient Temp. (°C)**	**Chip Power**	**Current Technology**	**Future Technology**
Automotive				
Engine control Electronic	150	< 1kW	BS & SOI	BS & SOI
On-cylinder& Exhaust Pipe	600	< 1kW	N/A	WBG
Electric Suspension & Brakes	250	> 10kW	BS	WBG
Electric/Hybrid Vehicle PMAD	150	> 10kW	BS	WBG
Turbine Engine				SOI & WBG
Sensors, Telemetry, Control	300	< 1kW	BS & SOI	WBG
	600	< 1kW	N/A	WBG
Electric Actuation	150	> 10kW	BS & SOI	WBG
	600	> 10kW	N/A	
Spacecraft				
Power Management	150	> 1kW	BS & SOI	WBG
	300	> 10kW	N/A	WBG
Venus & Mercury Exploration	550	~ 1kW	N/A	WBG
Industrial				
High Temperature Processing	300	< 1kW	SOI	SOI
	600	< 1kW	N/A	WBG
Deep-Well Drilling Telemetry				
Oil and Gas	300	< 1kW	SOI	SOI & WBG
Geothermal	600	< 1kW	N/A	WBG

BS= bulk silicon, SOI= silicon on insulator, WBG= wide bandgap (semiconductor)

1.4 Electromigration

SiC power devices designed for use in harsh environments must take into account the electromigration phenomena. Electromigration is the movement of atoms in a metal film due to the momentum transfer from the electrons carrying the current. When a potential is applied along a conductor trace, two forces act on metal ions: one is due to the electric field along the trace, and the other is due to the electron "wind" effect. The two forces act in opposite directions, and the combined result is the metal ion being in the direction of the electron motion. Under high current density conditions, this metal-atom movement causes voids in some regions which can eventually result in open circuits and metal pileups or "hillocks" in other regions which can cause short circuits between closely spaced conductors [30]. Failure modes are typically characterized by a certain percentage increase in the line resistance, by a line becoming an open circuit, or by adjacent lines becoming short circuited. Line degradation is a slow process and under normal device operating conditions can take many years. Hence, measurements are made under accelerated conditions at higher than normal temperatures and/or current densities. Accelerated tests typically use temperatures above 200°C and current density above 10^6 A/cm^2 [22].

1.5 Packaging of SiC High Temperature, High Power Devices

SiC high temperature, high power devices are of little advantage if they can not be reliably packaged to form a complete system capable of operation under harsh environments. The major challenges for such packaging technologies are the mechanical, physical and electrical stability of the packaging materials and the interactions among these materials [31]. The key issues involved in packaging high temperature, high power

SiC devices include: material oxidation, decomposition and intermetallic compound (IMC) formation under high temperature conditions, along with heat generation and dissipation (cooling technology) and coefficient of thermal expansion (CTE) mismatches between different materials.

In order to function correctly in high temperature, high power applications, innovative packaging material and packaging design concepts are required. Additionally, high temperature passive components, such as resistors, inductors, capacitors and transformers, must also be developed for operation in hostile conditions before the full system-level benefits of high ambient temperature power electronics can be realized [31].

1.5.1 Substrate Materials for SiC Power Electronics

The substrate plays a key role in heat removal, in addition to the mechanical support it provides and its use in chip backside electrical connections. Commonly used substrate materials include beryllium oxide (BeO), silicon nitride (Si_3N_4), aluminum nitride (AlN) and aluminum oxide (Al_2O_3).

BeO has the highest thermal conductivity commercially available for high power hybrid applications. Although it provides the best performance for heat dissipation, the high cost and toxicity issues associated with beryllium have led to its replacement with alternate ceramic substrate materials [32]. One alternative substrate material that is being considered, Si_3N_4, has a reasonable thermal conductivity and a lower CTE and 2.4X the fracture toughness of AlN.

AlN offers another alternative to BeO without the toxicity concerns. AlN has excellent electrical properties (dielectric constant, loss tangent, resistivity, and dielectric strength), mechanical properties and a near perfect CTE match to SiC. The thermal

conductivity of AlN decreases with temperature, however it is still slightly better than that of BeO in the high temperature range [33]. The thermal conductivity of AlN is significantly influenced by its chemical purity and density, the key to producing a high thermal conductivity AlN substrate is to fabricate an extremely pure and very dense AlN ceramic material [34].

Al_2O_3 based ceramics are popular as substrates because of their availability, low cost, good electrical properties and acceptable thermal conductivity. Al_2O_3 compositions range from 90 to 99 weight percent purity, with the other constituents being SiO_2, MgO and CaO. Typical substrate properties are presented in Table 1-3[35].

Table 1-3 High temperature substrate properties [35]

Materials / **Properties**	**Al_2O_3**	**Si_3N_4**	**AlN**	**SiC**
Thermal conductivity(W/m•ºC)	20	30-90	170-230	490
CTE (ppm/ºC)	6.7-7.1	2.7	4.5	4.2-4.8
Young's modulus (GPa)	380	310	330	450
Fracture toughness (MPa•m ½)	3.3-3.7	5-6.5	2.7	4.6
Flexural strength (MPa)	274	850	400	550

In order to carry a large current, thick copper metallization is required. Joining between metals and ceramics is difficult due to the dissimilar nature of the atomic bonding of the two materials. Direct bond copper (DBC), active metal brazing (AMB) and thin film/plated Cu have been developed to attach thick Cu to ceramic substrates.

The basic development of DBC process was undertaken by General Electric 30 years ago, and steady research and development in DBC technology has made possible the mass production of 5.5" x 7.5" substrates using a highly automated process [36]. The

DBC process was initially developed on Al_2O_3 substrates. The principle of the DBC technique relies on the phenomenon that oxygen decreases the melting temperature of pure Cu (1085ºC), the eutectic Cu/O melts at 1065°C in 1.4 at% oxygen. The Cu foil is in close contact with the Al_2O_3 and is heated to 1065°C to 1085°C, as illustrated in Figure 1-3 [37]. During this process, the Cu sheet forms a thin oxidation layer and a eutectic melt at the CuO and Al_2O_3 interface, while the Cu sheet itself remains solid. After cooling to room temperature, an excellent CuO to Al_2O_3 joint can be achieved due to the following spinell reaction: [37].

$$CuO + Al_2O_3 = CuAl_2O_4 \qquad (1\text{-}2)$$

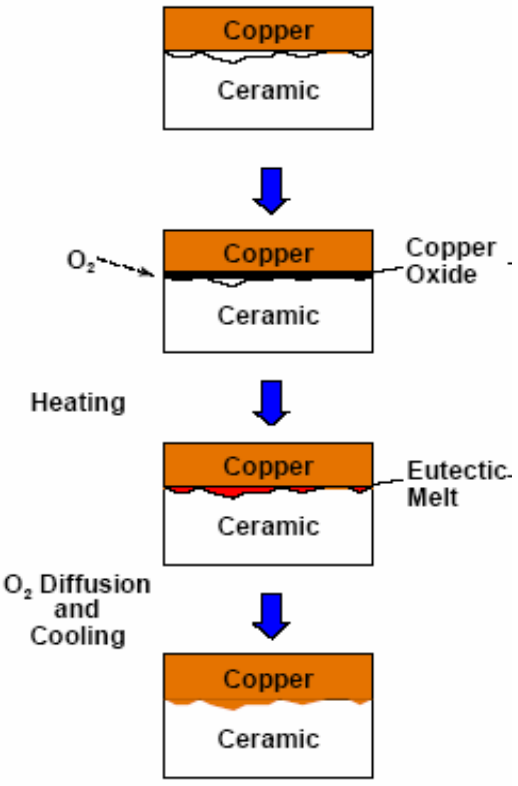


Figure 1-3 DBC Al_2O_3 process [37]

Direct Bond Copper (DBC) substrates have been used for power electronics for many years because of the following advantages:

- Low CTE in spite of the relatively thick copper cladding layer
- High current carrying capability due to copper's low resistivity
- High mechanical strength
- High heat dissipation capability

The excellent electrical conductivity and heat dissipation properties of DBC allow very high current flows; a 0.3mm DBC on 0.63mm thick Al_2O_3 only shows an increase in temperature of 17°C with conventional cooling and 100 A continuous current. Due to the high temperature involved in fusing of Cu to Al_2O_3, the adhesion of Cu to Al_2O_3 is very strong, and the strong joint between Cu and Al_2O_3 significantly constrains the CTE of the Cu surface to 7.2 ppm/ºc which is only slightly higher than that of Al_2O_3 (6.8 ppm/ºc) [37]. The DBC Al_2O_3 thus has excellent reliability under thermal cycling conditions. Experiments have shown that DBC Al_2O_3 can survive 1000 cycles from -55°C to +150°C test conditions [36].

Compared to a conventional metal package, DBC packages combine very high current carrying capability with only about 30% of the weight. Thus DBC substrates have become more and more important for aviation, military and space power electronic applications.

In order to increase the thermal properties of power modules, the DBC process has also been investigated on AlN substrates. An oxidation treatment of the AlN prior to the DBC process is needed to achieve good adhesion [38]. The process is illustrated in Figure 1-4 [37]. BeO substrate is also compatible with DBC process.

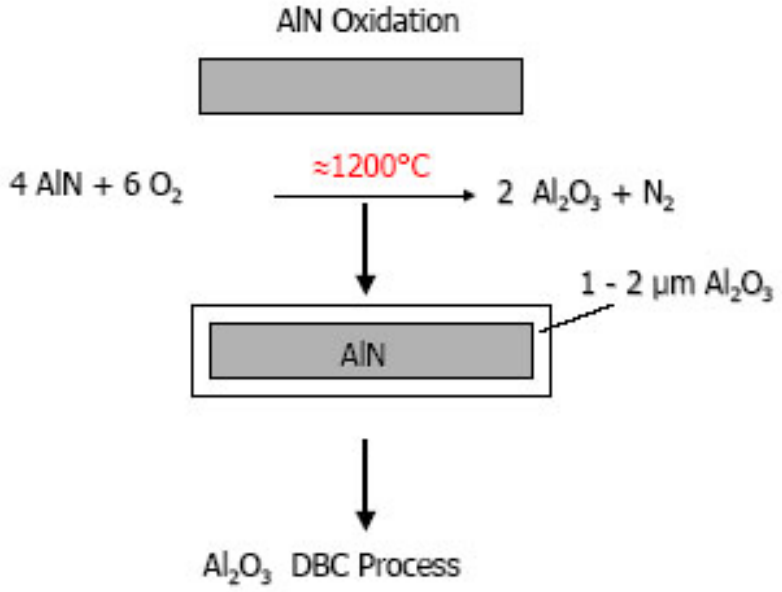


Figure 1-4 DBC AlN process [37]

The low surface tension of Si_3N_4 makes it difficult for many molten metals to satisfy the wetting condition in order for reactions to take place at the ceramic interface. The active metal brazing (AMB) method brazes copper foil on Si_3N_4 with a Cu-Ag eutectic alloy with the addition of about 8 wt% Ti. The high chemical reactivity of Ti with the Si_3N_4 enhances the wetting and bonding characteristics [39]. Recently, Kyocera announced its AMB Si_3N_4 substrate which achieved 5000 cycles of air-to-air temperature cycling from -60°C to 175°C without any failure [40]. The AMB Si_3N_4 substrate is much stronger mechanically than conventional DBC Al_2O_3 and DBC AlN substrates [40].

NiCr/Cu/Au thin film metallization has recently been studied [33] on AlN substrates, thick Cu layer can be achieved by subsequent electroplating of Cu to the required thickness. However, with a thick Cu layer, the AlN is prone to fracture during thermal cycling due to its low flexural strength and fracture toughness [2].

Copper metallized ceramic substrates (Si_3N_4, AlN and Al_2O_3) can be supplied with a standard Ni/Au surface finish. Typically 200μinch of Ni is electrolessly plated or electrolytically plated over the copper foil. On top of the Ni layer, a thin layer of gold is immersing plated to a thickness of 5-20μinch to prevent Ni oxidation.

Electroless nickel (EN) plating is also known as chemical or autocatalytic nickel plating. In contrast to the traditional electrolytic (galvanic) technique, chemical nickel plating baths work without an external current source. The plating operation is based upon the catalytic reduction of nickel ions on the surface being plated. Electroless nickel has the following advantages [41]:

- The need for complicated trace routing is avoided
- The unique throwing power of the solution
- The coating grows uniformly over the exposed surface

There are three main types of electroless nickel coatings: nickel-phosphorus, nickel-boron and poly alloys. Nickel-phosphorus is generally used for engineering applications. In the most widely used electroless technique, nickel is deposited by the catalytic reduction of nickel ions with sodium hypophosphite in acid baths at a pH of 4.9 and at a temperature of 88°C. The deposit typically contains 3 to 13wt % phosphorus depending on the chemical composition of the solution and the operating conditions. The phosphorus content significantly influences the nickel's chemical and physical properties in both the as-plated and after heat treatment conditions. Based on the phosphorus composition, electroless Ni:P can be divided into three categories [41]:

1. Phosphorus content between 3 and 7 wt %. These coatings have excellent wear resistance.

2. Phosphorus content between 9 and 12 wt %. Corrosion protection and abrasion resistance are good enough for most applications. The plating bath works particularly economically.

3. Phosphorus content between 10 and 13 wt %. The coatings are very ductile and corrosion resistant. They have the highest performances for corrosion resistance against chlorides and simultaneous mechanical stress.

1.5.2 Die Attach

Die attach is another key issue for high temperature operations. The joint must survive the high temperature while maintaining good electrical conductivity if the chip backside requires electrical connection. In order to achieve good die bonding, three methods can be chosen: adhesive bonding, diffusion bonding and braze bonding.

Adhesive bonding is a material jointing process in which an adhesive is dispensed between two facing surfaces, and cured to produce an adhesive bond. Based on its conductivity properties, the die adhesive can be categorized into two types: conductive and non-conductive. An electrically conductive adhesive is made by loading metallic particles in a polymer matrix. Table 1-4 presents typical conductive adhesives' compositions and properties. Conductive adhesives are not suitable for use above 250°C [42].

Table 1-4 Adhesive properties [42]

Basic resins	**Filling materials**	**Configuration of particles**	**Glass transition temp. (Tg)**	**Volume resistivity (Ω•cm)**	**Operating temperature range**	**Curing conditions**
Epoxy	Ag	Flakes	90°C	$6e10^{-5}$	-65~150°C	1h/130°C
Epoxy	Ag-plated Cu	Flakes	N/A	$4.5e10^{-3}$	20~160°C	30min/125°C
Epoxy	Ni	other	N/A	1	-50~150°C	2h/65°C
Polyimide	Ag	Flakes	249°C	$5e10^{-4}$	20~250°C	1h/140°C
Silicone	Ag-plated Cu	Flakes/balls	-55°C	$1e10^{-2}$	-55~125°C	168h/25°C
Silicone	Ag	Flakes	N/A	$6e10^{-4}$	-50~200°C	1h/150°C

Diffusion bonding is a method of joining metallic or non-metallic materials that relies only on interface solid state diffusion to create new metallurgical grains and bridge the gap, with no braze alloy or bonding agent required [43]. A seamless joint can be made by controlling the temperature, pressure, and time. Normally, a temperature of 50% - 70% of the melting point of the most fusible metal is used, and pressure is applied to aid in deformation of the interface and to remove any oxidation film. The bonding is usually done in a vacuum or in an inert gas environment.

Diffusion bonding has found applications in weapons industry, where the welding materials need to be isolated from the atmosphere, generally in a vacuum [44]. A technique has been developed where a thin film of silver (on the order of microns) is placed between the surfaces to be bonded. The temperature is raised to near silver's melting point to facilitate diffusion. The advantages of this process over traditional welding include the small amount of bonding material needed and it generate little particulate matter so it is a relatively clean process [44].

Braze bonding is a heating process in which two or more like or unlike materials are joined together by means of another metal alloy with a lower melting point. Usually the metal alloy has a eutectic composition. The term "eutectic" is from the Greek word eutektos, meaning "easily melted". To prevent oxidation, brazing is normally conducted in an inert gas or in a vacuum. Braze joints can be made exceptionally strong, sometimes stronger than the two metals being joined, and are able to withstand shock, vibration and normal temperature changes, providing good electrical conductivity and heat transfer between the die and the substrate.

Commonly used braze alloys include Au-Sn (80/20), Au-Ge (88/12), Au-Si (96.85/3.15) and Au-In (81/19) (composition in wt%) which have eutectic melting points of 280°C, 361°C, 363°C and 487°C, respectively. Au based brazes have good electrical conductivity, good thermal conductivity and good resistance to oxidation. Au based brazes can usually be bonded with good results in an inert (N_2) environment. Table 1-5 presents a list of the properties of common brazes [45]:

Table 1-5 Brazes properties [45]

Braze Composition	**Liquidus °C**	**Density (g/cc)**	**Electrical Conductivity (% of IACS)**	**Thermal Conductivity (W/m•K)**	**Thermal Coefficient of Expansion (ppm/°C) (20°C)**	**Tensile Strength (psi)**
80Au, 20Sn	280	14.51	7.7	57	15.9	40000
88Au, 12Ge	361	14.67	11.4	44	13.4	26900
96.85Au, 3.15Si	363	15.7	46.4	27	12.3	37000
81Au, 19In	487	14.72	8.4	28	14.7	33700

To achieve good wetting, the braze thickness and footprint must be carefully chosen. The following are the rules of thumb for small dies being joined using Au based brazes [46]:

- Thickness = 25 ~ 40μm
- Length = 90 percent of die length
- Width = 90 percent of die width

There are several methods that can be used to present the braze for bonding [46]:

Preforms: Preforms are pre-shaped brazes that are placed at the joint area before heating. This is the most common method because of its quick set-up time. Singulated preforms can be expensive to procure, but they enable flexible production because substrate designs and feed mechanisms do not need to be changed. Preforms are supplied in a variety of shapes and sizes, although they are difficult to handle at very small sizes.

Die backside metallization: Here, a metallization layer is applied to the back of the wafer as a part of the wafer fabrication process. The metallization layer can be plated, sputtered or evaporated.

Pre-deposition of braze on the substrate: In this process, the braze is electroplated on the bond pad when the substrate is produced. This is a cost-effective method, but deposits on individual substrates can be time-consuming.

Braze ribbon or automatic preform feeder: This is a cost-effective method to produce custom preforms using a ribbon spool feeder and a punch mechanism. The preforms are produced in a high-volume environment and the scrap braze ribbon is recycled. There is often a materials handling issue, however, as most preforms are only about 40μm thick, and ribbon less than 125μm thick is difficult to feed because the

material frequently folds over itself and jams the feeder (commonly referred to as "shingling") [46].

1.5.3 Wire Bonding

Wire bonding is an electrical interconnection technique using wire and a combination of heat, pressure, and/or ultrasonic energy. Wire bonding is a solid phase diffusion process. By bringing two metallic materials (usually Au and Al) into intimate contact, electron sharing or interdiffusion of atoms takes place, resulting in the formation of the wire bond. In the wire bonding process, the bonding force required leads to material deformation, breaking up the contamination layer and smoothing out surface asperity, which can be enhanced by the application of ultrasonic energy. Heat can accelerate atoms interdiffusion, and thus the bond formation [47]. There are three major types of wire bonding: thermocompression bonding, ultrasonic bonding, and thermosonic bonding, as shown in Table 1-6 [47].

Table 1-6 Wire bonding process comparision [47]

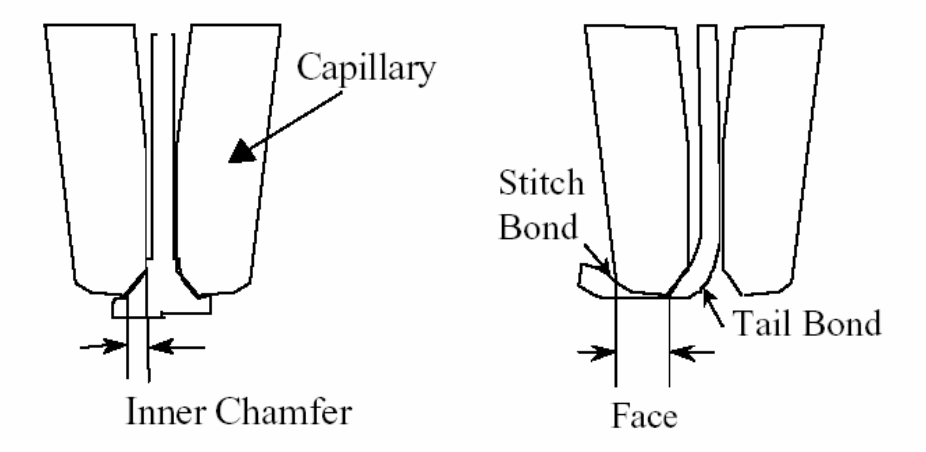
Wirebonding	**Pressure**	**Temperature**	**Ultrasonic energy**	**Wire**	**Bonding pad metallization**
Thermocompression	High	300-500°C	No	Au	Al, Au
Ultrasonic	Low	25°C	Yes	Au, Al	Al, Au
Thermosonic	Low	100~240°C	Yes	Au	Al, Au

There are two basic forms of wire bonds: ball bonds and wedge bonds. In ball bonding, a free air ball (FAB) is formed after the second bond, and the first bond is achieved by bonding the FAB to the pad. Consistent and symmetrical FAB is important to produce a consistent first bond. To achieve a consistent FAB size requires a consistent

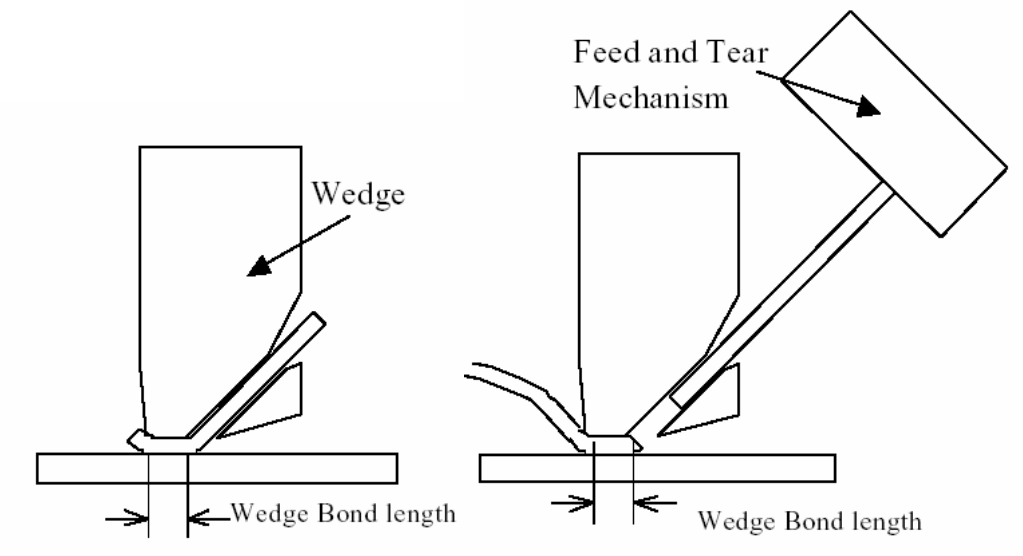
tail length after the second bond formation and consistent electronic flaming off (EFO) firing. A certain amount of tail bond, which is formed by the inside chamfer of the capillary, is left to allow pulling of the wire out of the capillary after the second bond (stitch bond) formation in preparation for the next FAB formation [48].

In wedge bonding, the wire is bonded directly to the pad by applying force and ultrasonic energy. The wire is broken by a cutter and the wire is then fed underneath the wedge. No tail bond is involved in wedge bonding. Figure 1-4 shows the first bond and second bond comparisons of ball bonding and wedge bonding [48].

Large diameter Al wire bonding is often used with silicon power devices. However at high temperatures, the mechanical strength of the Al decreases. Also, Al is incompatible with the Au wire bond pads used on SiC dies due to intermetallic formation and Kirkendall voiding at high temperature. In order to carry high current, large diameter wedge bonding with 250μm Au and Pt was developed for power packaging. Au wire provides higher conductivity than Pt, but Pt has a higher mechanical strength at high temperatures. Large Au wire has been successfully bonded to dies and to the Cu/Ni/Au substrate metallization [2].



(a)



(b)

Figure 1-5 First bond and second bond comparison, (a) ball bonding and (b) wedge bonding [48]

1.5.4 High Voltage Passivation

Devices operating at high power conditions may be exposed to high voltages, and as a result high voltage breakdown may occur between adjacent high voltage electrical connections and/or between high voltage electrical connections and the surrounding air. An effective dielectric passivation coating must be applied to ensure reliable package

operation. Suitable candidates are preferred that can be applied by dispensing or spin-coating, have a high dielectric breakdown voltage and high temperature stability. Polymers with easy processability, good mechanical properties, high thermal stability and high electrical breakdown voltage are usually chosen for electronic packaging applications.

Because of its long term thermal-oxidative stability in both nitrogen gas and in air, low moisture absorption, outstanding flame resistance and extreme high glass transition temperature (T_g) of 510°C, phthalonitriles have shown promise as materials that can be potentially used for a variety of high temperature applications [49]. In order to lower the initial processing temperature to less than 150°C and to increase the processing window between the melting point of the phthalonitrile and its polymerization temperature, low melting phthalonitrile oligomers which have aromatic ether groups linking the phthalonitrile endcaps have been developed. A larger processing window means that a higher concentration of curing additive can be used to control the polymerization rate and the viscosity changes that accompany the phthalonitrile cure. Flexible ether linkages were chosen for incorporation into the polymeric backbone to increase processability without sacrificing the exceptional thermal, mechanical and flammability properties of phthalonitriles. With a decrease in the cross-link density of the polymer and an increased flexibility due to multiple aromatic ether linkages, the low melting phthalonitrile polymers show an improved toughness when compared to the standard phthalonitrile system. When used alone or blended with phthalonitrile, the enhanced toughness of the low melting phthalonitrile polymer may alleviate potential micro-cracking problems that

could arise from thermal-cycling in aerospace and other high temperature applications [49].

The thermal-oxidative stability of the phthalonitrile polymers has been evaluated in nitrogen gas and in air by TGA analysis. Oligomeric phthalonitrile and phthalonitrile exhibit similar thermal stability up to 500 °C [49].

Polyimides are high temperature engineering polymers with a transparent, amber color. When compared to most other organic or polymeric materials, polyimides exhibit an exceptional combination of thermal stability (>500°C), mechanical toughness, chemical resistance and excellent dielectric properties. Because of their high degree of ductility and inherently low CTE, polyimides can be readily implemented into a variety of microelectronic applications [50].

In the fabrication of microelectronic devices, polyimide coatings are typically spin applied to the substrate and then thermally cured into a smooth, rigid, intractable polymeric film or structural layer. For optimal adhesion to silicon, oxides and most metals, adhesion promoters are required. Some polyimides have built in adhesion promoters, while others require the application of a separate adhesion promoter or coupler prior to polyimide application. Adhesion promoters are also applied by spin coating. While spin coating assures the best uniformity and coating quality, other application techniques that have been used for applying polyimides include draw, spray, extrusion, roller, dip and drop coating [50].

Curing the polyimide film involves the removal of the solvent carrier or other volatiles from the layer and the imidization or hardening of the polymer into an intractable polyimide film. This curing process is typically done in steps. Hot plates are

commonly used for the initial bake after the polyimide has been applied. Post apply bakes can range from 50°C to 150°C on one or more in-line hot plates. A furnace or programmable oven is used for the final cure. Final curing is usually done between 280°C - 400°C, depending on the application [50].

Polyhedral oligomeric silsesquioxanes (POSS) are a class of nanofillers for polymers. The term silsesquioxane refers to all structures with the empirical formula $RSiO_{1.5}$, where R is hydrogen or any alkyl, alkylene, aryl, arylene, or organofunctional derivatives of alkyl, alkylene, aryl and arylene groups. The silsesquioxanes include random structures, ladder structures, cage structures and partial cage structures, as indicated in Figure 1-6 [51].

POSS compounds embody a truly hybrid (inorganic-organic) architecture, which contains an inner inorganic framework of $(SiO_{1.5})_x$ that is externally covered by organic substituents. These substituents can be purely made up of hydrocarbon or may include a range of polar structures and functional groups, and making the POSS nanostructure compatible with polymer and biological systems [51].

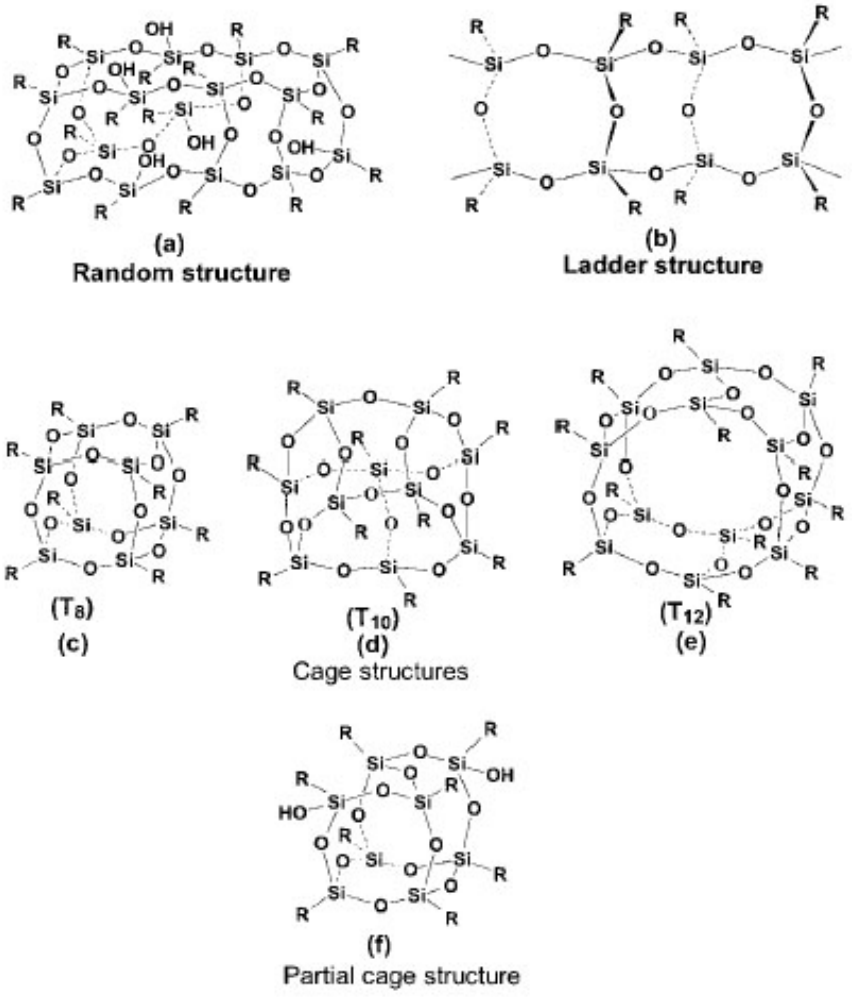


Figure 1-6 POSS structures [51]

A variety of POSS nanostructured chemicals have been prepared which contain one or more covalently bonded reactive functionalities that are suitable for polymerization, grafting, surface bonding or other transformation. The incorporation of POSS derivatives into polymeric materials can lead to dramatic improvements in polymer properties, including increases in the glass transition temperature, oxidation resistance, and abrasion resistance, as well as reductions in flammability, heat evolution and viscosity during processing. The POSS nanocomposites show great promise for use in semiconductor processing, bio-medical development and space applications [51].

1.6 Research Objectives

The goal of the project is to develop the assembly materials and processes for packaging silicon carbide power electronics, which will be used under extreme environments. As a part of the project, the dissertation work includes a study of die attach materials and processes, the substrates, the polymer passivations and capacitors for high temperature applications.

In Chapter 1, the properties, processing and device technology of SiC have been reviewed and some key issues in packaging of power electronics discussed, including: substrates technology, die attach materials, high temperature braze bonding and high temperature, high voltage passivation coatings.

Chapter 2 present details of the die attach technology, which includes the selection of a suitable braze, SiC die metallization, substrate preparation and mechanical strength and metallurgy investigations of the braze joint during high temperature storage and thermal cycling.

The electrical breakdown property of several polymers that may be suitable for the high temperature passivation coating is reported in Chapter 3. The electrical breakdown mechanism is also discussed.

In Chapter 4, the dissipation factor and capacitance of ceramic capacitors during high temperature storage are discussed.

Chapter 5 concludes the dissertation by summarizing the results and findings, and suggesting topics for future work.

CHAPTER 2

DIE ATTCH FOR SILICON CARBIDE PACKAGE

2.1 Introduction

The challenges of packaging SiC power devices for high temperature applications include their high operating temperatures, wide thermal cycle ranges, high currents and high voltages. In addition to providing the electrical interfaces between the contact pads on the SiC device and other components, the packaging also provides electrical insulation, mechanical and environmental protection and a path for heat conduction and removal. In SiC power packages, consideration must also be given to current carrying capability and high voltage insulation. As a result, the selections of chip metallization, die attach, substrate and insulation dielectric are crucial to a successful package design.

2.2 Chip Metallization

An effective chip metallization should provide the following features:

- Good adhesion to the wafer passivation and the contact (Ohmic or Schottky)
- Low contact resistance
- An effective diffusion barrier
- A metal stack that is compatible with wire bonding and braze metallurgy
- High temperature reliability

Evaporation and sputtering are two of the most important physical vapor deposition (PVD) methods used for depositing thin metal films. Sputtering offers several

advantages over evaporation due to its better film adhesion and ability to deposit alloys. A sputtered three layer thin film stack composed of Ti/Ti-W/Au (1000 Å /2000 Å /2000 Å) was evaluated as the chip metallization in this project. Ti provides good adhesion to the device contacts (Ni_2Si, an ohmic contact); Ti-90W functions as a diffusion barrier layer; and Au protects the underlying Ti-W from oxidation, as well as serving as a wire bondable and braze wettable surface.

2.3 Die Attach

2.3.1 Introduction

Polymer die attach materials are limited to operating temperatures below about 250ºC, while Au-Ge and Au-Si are not suitable die attachment materials for operating temperatures over 350°C. The use of thick film Au conductor material fired at 600ºC as a die attach material has been demonstrated by Auburn researchers [52]. However, the firing is performed in air, and the SiC contact pad stacks were not compatible with such high temperatures (600°C) in air, the pads are not wire bondable after die attach. This process has been refined by researchers at NASA Glenn Research Center [53].

Chuang and Lee have recently demonstrated a low temperature die attach process using Ag and In [54]. The In layer initially melts at low temperature, and then diffuses into the Ag layer, forming an Ag-rich phase and intermetallic crystals. The process can be performed around 200ºC by selecting the proper thickness ratio of Ag and In (Figure 2-1), and the resulting melting point after diffusion is over 600ºC.

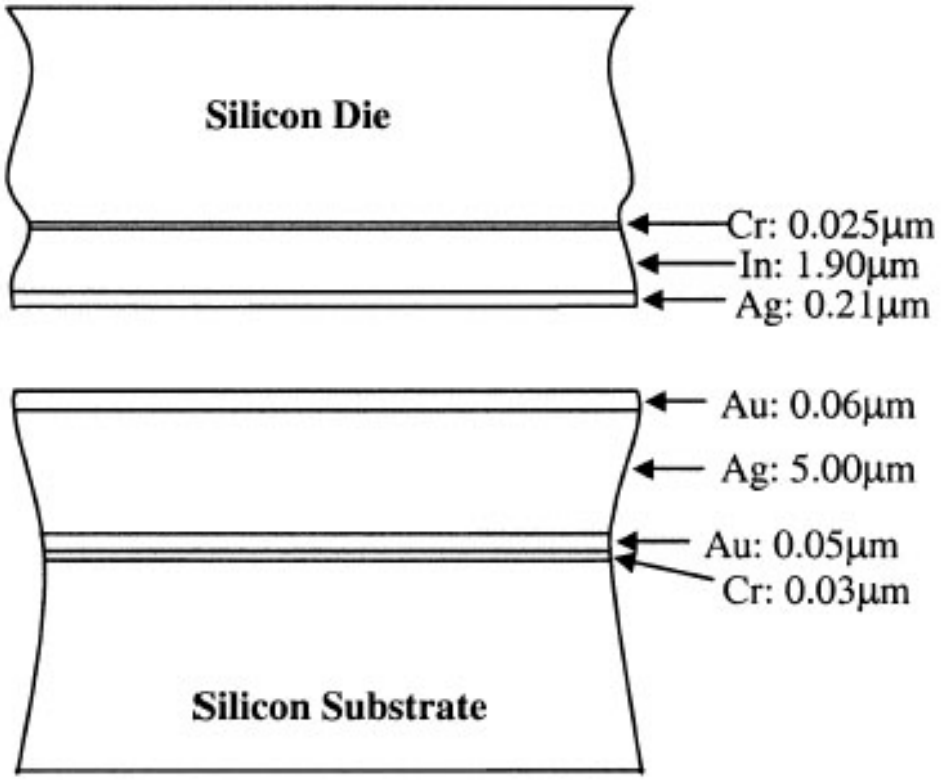


Figure 2-1 Metallization stack for Ag-In die attach [54]

While promising, there is significant concern over possible Ag migration under electrical bias at high temperatures. Auburn researchers have observed Ag migration between thick film Pd-Ag conductors during bias testing of thick film resistors at 300ºC with a bias as low as 10Vdc [55].

The technique developed (transient liquid phase bonding) in this work uses a eutectic Au-Sn preform with thick Au (20µm) plating either on the substrate or on the chip. With high temperature brazing and annealing at 400°C, the Sn from the eutectic Au-Sn preform diffuses into the thick Au layer, lowering the Sn concentration to less than 10 wt% and raising the alloy melting point to over 400°C.

2.3.2 Au-Sn Eutectic Alloy

The Au-Sn phase diagram is presented in Figure 2-2 [57]. The equilibrium phases are briefly described as follows [57]-[58]:

1. The liquid phase L.
2. The fcc solid solution, Au, having a maximum solid solubility of about 4.2 wt% Sn at 498ºC.
3. The β phase, which is composed of $Au_{10}Sn$ and is stable above 250ºC.
4. The ζ phase, which exists between 12 and 16 at% Sn at 225ºC and extends from 11.07 to 16.31 at% Sn at 275ºC, where the peritectic temperature of the L+ Au- ζ is 498ºC. The ζ - ζ' + Sn eutectoid composition appears to consist of 18.5 at% Sn at 190ºC. The L- ζ + AuSn eutectic occurs at 278ºC with 29.5 at% Sn. This is the most commonly used eutectic braze alloy, with Au 80 wt% and Sn 20 wt%.
5. The ζ' phase, which is stable at 17 at% Sn and below 160 ºC.
6. The δ phase, which is an AuSn intermetallic compound with a melting point of 419.3 ºC. The homogeneity range is 50~50.5 at% Sn.
7. The ε phase, which is the orthorhombic intermetallic compound $AuSn_2$; the peritectic L+ δ--- ε reacts at 309 ºC, giving a composition of about 72 at% Sn. The homogeneity range of this phase is very narrow.
8. The η phase, which is composed of $AuSn_4$. The peritectic reaction L + ε-- η is at 252 ºC, and the eutectic reaction L-- η+ occurs at 93.7 at% Sn at 217 ºC.

9. Terminal solid solution, βSn and αSn. The βSn solid solution has a solubility of up to 0.2 at% Au and αSn has a very limited solid solubility of less than 0.006 at% Au.

Au-Sn eutectic alloys already in preform shape were purchased from Williams Advanced Materials for use in this experiment. The preforms were supplied in the dimension of 3.3mm x 3.3mm x 0.025 mm, with a melting point of 280°C. The thickness ratio of Au: Sn is 1.5:1 for the eutectic 80 wt% Au-20 wt% Sn composition, but in order to achieve a melting point of over 400°C (Sn less than 10 wt%), the Au: Sn thickness ratio must be larger than 3.4: 1. Thus, at least 20μm Au had to be plated either on the substrate or on the chip.

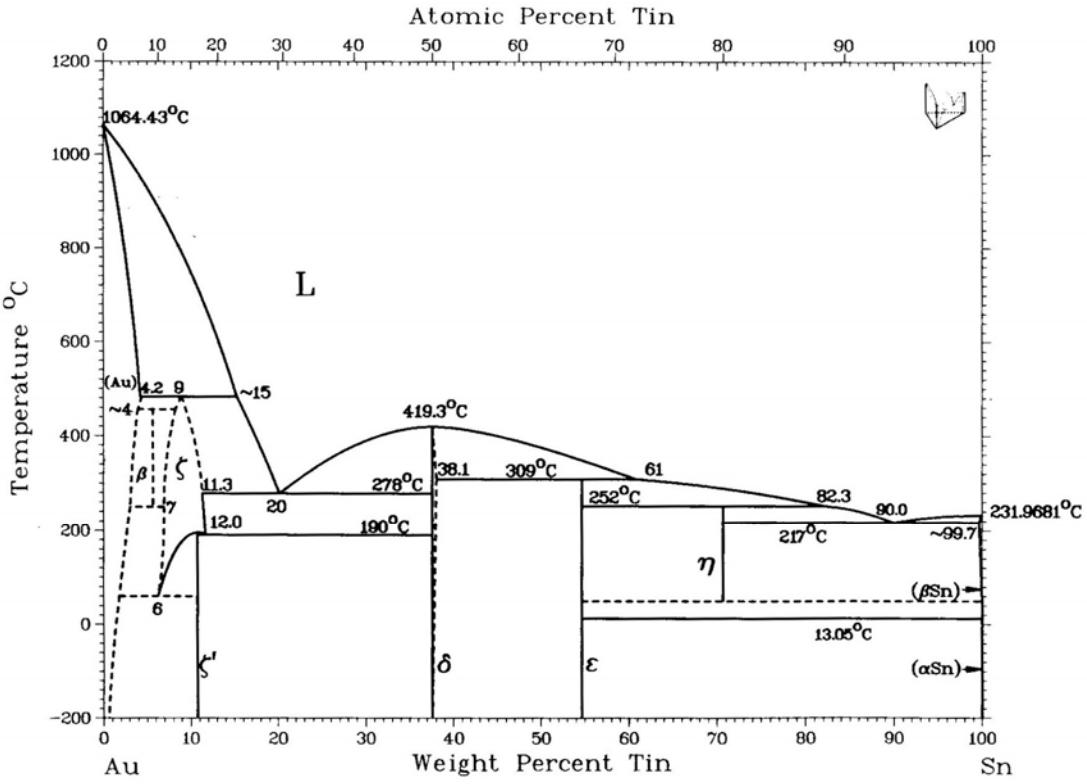


Figure 2-2 Au-Sn phase diagram [57]

2.3.3 Electroplating

Electroplating is the process of depositing a coating, commonly silver, gold, or nickel, on another metal by means of an electric current. The metal to be deposited is usually the anode and the article to be plated is the cathode in an electrolyte solution in which the plating metal is the cation. The process was conducted in a glass beaker containing the electrolyte solution. A standard gold plating setup is shown in Figure 2-3. The multimeter was connected in series with the circuit to monitor the current flowing through the solution. Electroplating of metals such as nickel involves the use of a nickel anode, whereas electroplating of gold involves the use of a platinized cadmium mesh as the anode, with the electrolyte solution acting as the source of gold. The platinized anode is used for gold plating due to its availability in pure form, inertness and lower oxidizing capability. When current is flowing through the solution containing the metallic ions, the positive ions are attracted to the cathode and the negative ions to the anode. The cathode releases electrons to neutralize the positive ions, resulting in deposition on the cathode. The surface to be plated must be carefully cleaned to remove any grease and oxidation before immersion into the plating bath.

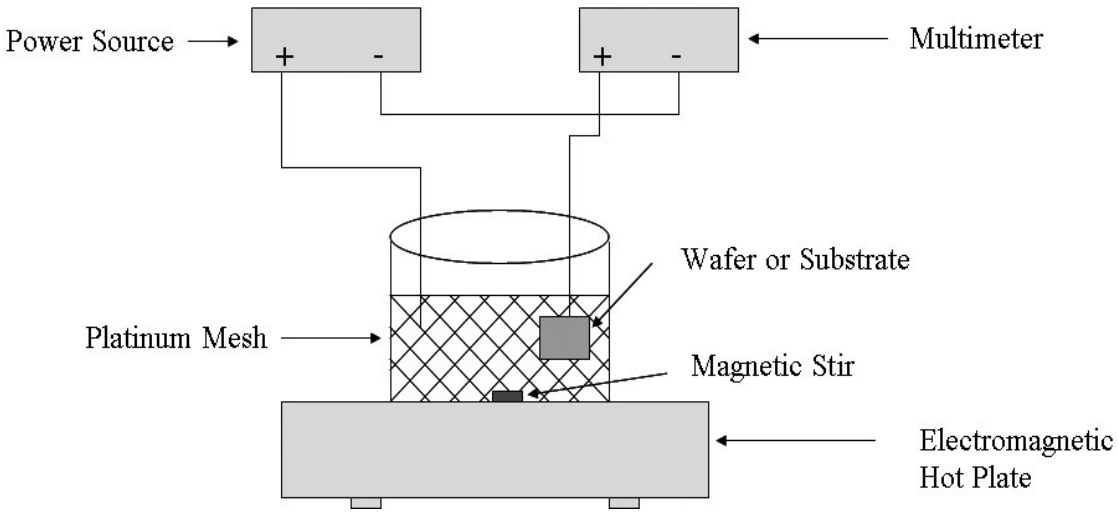


Figure 2-3 Gold plating setup

434 HS, supplied by Technic Inc., is a high speed neutral gold electroplating solution that may be used with either a pulsed DC power supply or a conventional DC power supply when the proper grain refiner is used. The operation conditions used for 434HS in this study were [59]:

- Temperature: 150°F
- pH: 6.0
- Anodes: Platinized anode to cathode ratio should be at least 1:1
- Current density: 5 ampere per square feet (ASF)
- Deposition rate: 3μm in 20 minutes @ 5ASF

TSC 1501 is a specially formulated soak cleaner for the removal of grease and oil; Orostrike C is an acid gold strike that insures excellent adhesion on most base metals. The process flow for gold electroplating was:

- TSC 1501 soak clean for two minutes at 65°C
- DI water rinse

- Degrease in a diluted 19:1 Deionized water: sulfacid solution for two minutes
- DI water rinse
- Orostrike C for 30 seconds @ 7.5 ASF, 40°C
- DI water rinse
- 434 HS plating, with the plating time dependent on the thickness required
- DI water rinse

A cross-section of a DBC Al_2O_3 substrate electroplated with 20μm Au is shown in Figure 2-4.

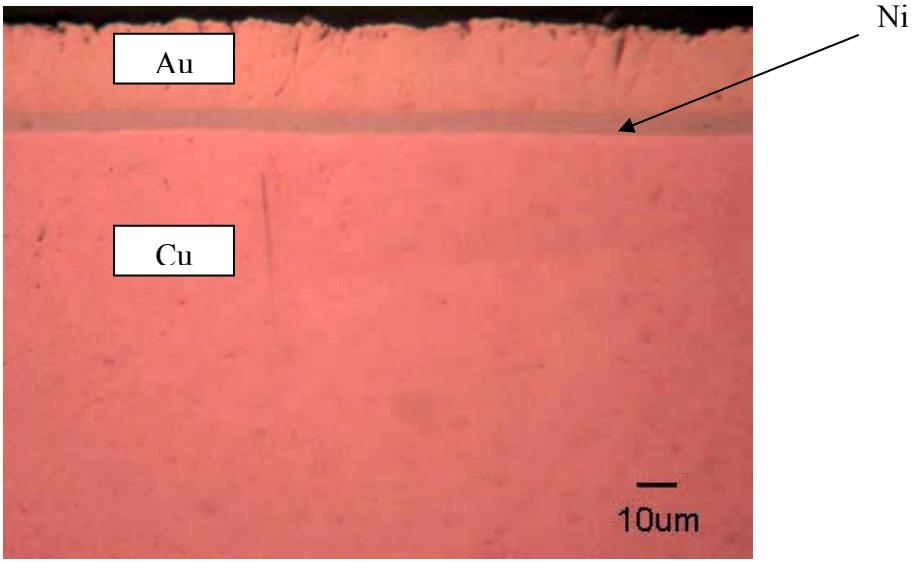


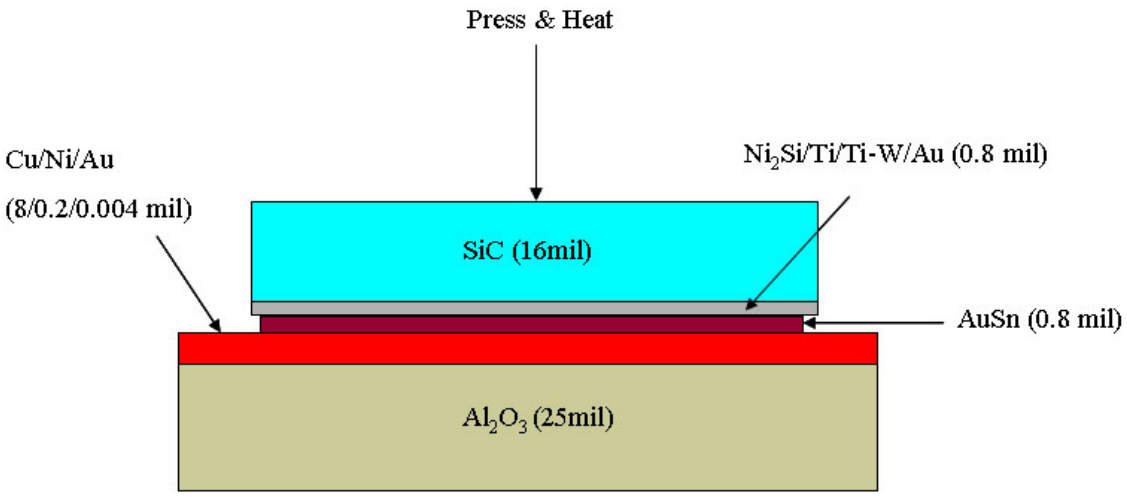
Figure 2-4 DBC Al_2O_3 substrate electroplated with 20μm Au

2.3.4 High Temperature Brazing

The brazing process was performed with an SST 3150 high vacuum furnace. The 3150 utilizes an oil-free roughing pump and a turbomolecular drag pump to achieve vacuum levels as low as 10^{-6} torr at temperatures of up to 500 °C. The brazing process can be done either in vacuum or in an inert gas with a pressure of up to 15 psig.

Voids in the bonding layer will significantly hinder the heat transfer from the chip to the substrate and weaken the braze joint strength. In order to obtain a void-free bond, the process was run in vacuum, and a 20g weight was placed on the assembly to squeeze out any remaining air bubbles. An illustration of the brazing setup is shown in Figure 2-5. The chip size was 150mil x 150mil with Ti/Ti-W/Au (20μm) metallization, and the DBC Al_2O_3 substrate size was 200 mil x 200mil.

The specially designed brazing profile is presented in Figure 2-6. It includes a 4 minute soak at 250°C to bake out moisture residue, then a 3 hour ramp from 250°C to 400°C, followed by a hold at 400°C for 30 minutes to allow Sn to diffuse into the Au layer.



Dimensions not drawn to scale

Figure 2-5 Brazing setup

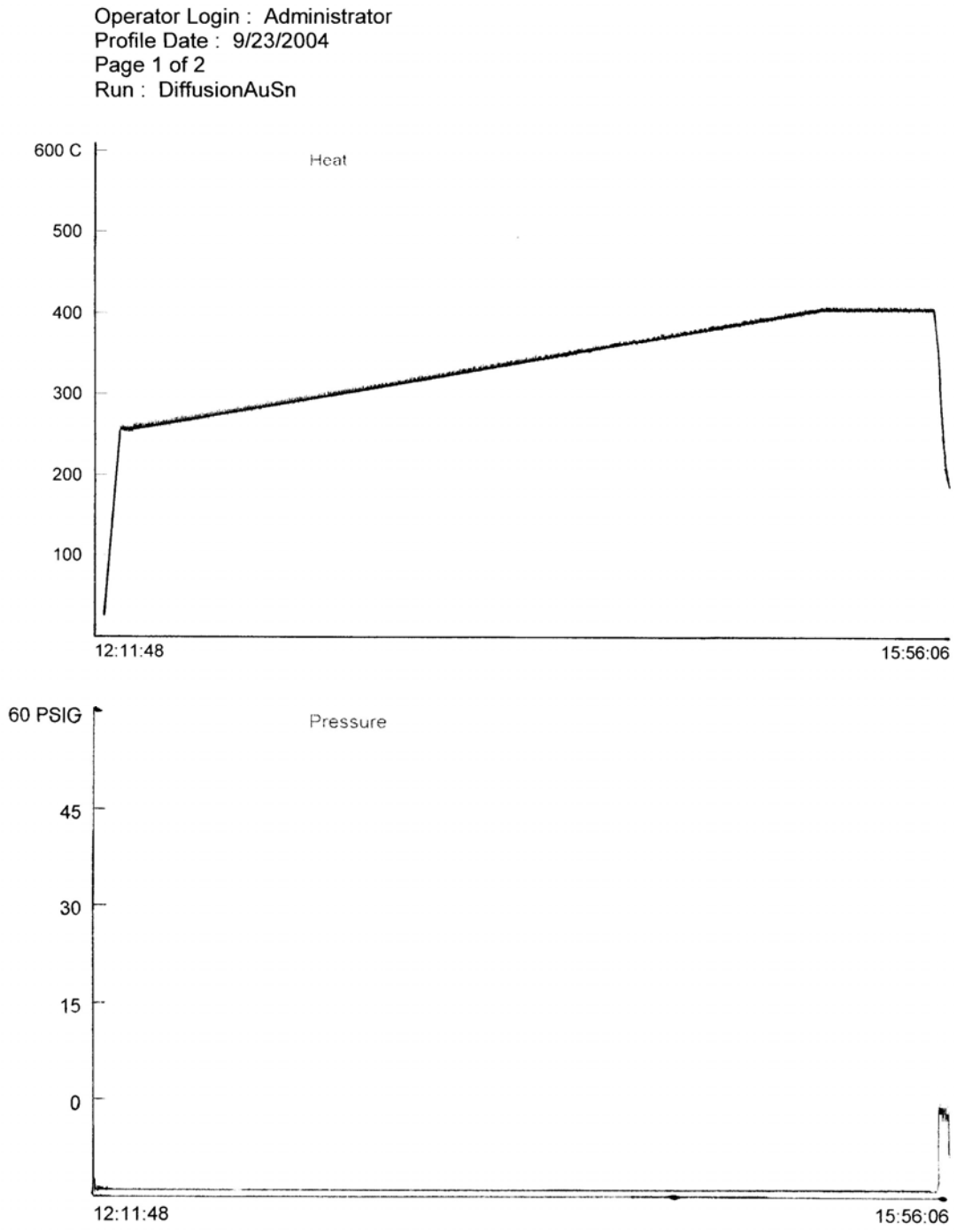
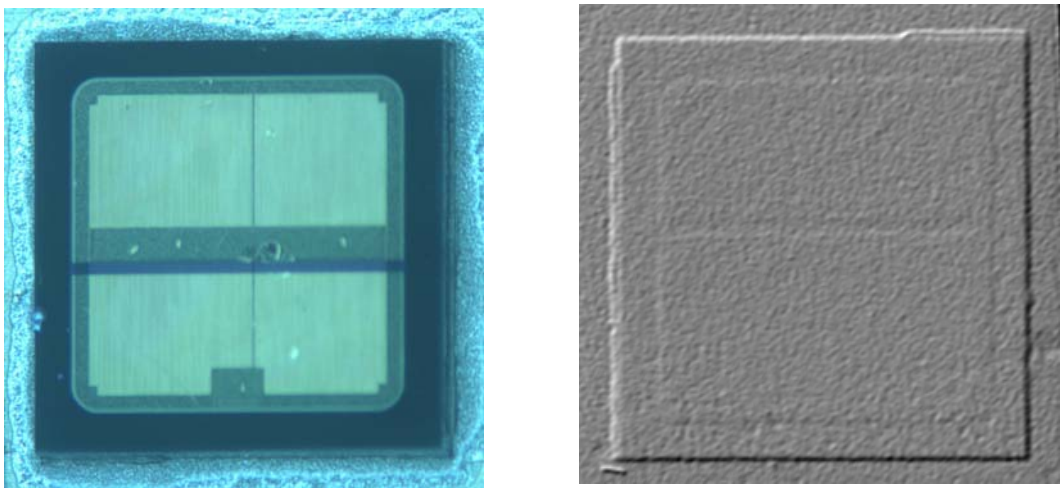


Figure 2-6 AuSn brazing profile

An optical image of an as-brazed sample is shown in Figure 2-7 (a), a void-free die attach was achieved, as shown in the x-ray relief mode image in Figure 2-7 (b). The bond strength was evaluated by a die shear test utilizing the Dage PC2400 system. The average as-brazed sample die shear strength was > 100kg-f (equipment limit). The sample size was 7.



(a) (b)

Figure 2-7 (a) as-brazed sample and (b) x-ray relief mode picture of as-brazed sample

Figure 2-8 shows the energy dispersive x-ray (EDX) elemental concentration plot across an AuSn as-brazed sample. The Sn concentration is about 6 wt% across the brazing layer, which corresponds to the Sn solid solubility limit in Au at 400°C. The Sn peak at the chip interface represents the reaction of Sn with Ti in the SiC metallization to form Sn-Ti intermetallic, while the Sn peak at the substrate surface is due to Sn-Ni intermetallic formation. Figure 2-9 contains the EDX element dot maps for an AuSn as-brazed sample, which show that the Sn is uniformly distributed throughout the Au layer, except for a peak at the substrate and the chip interface.

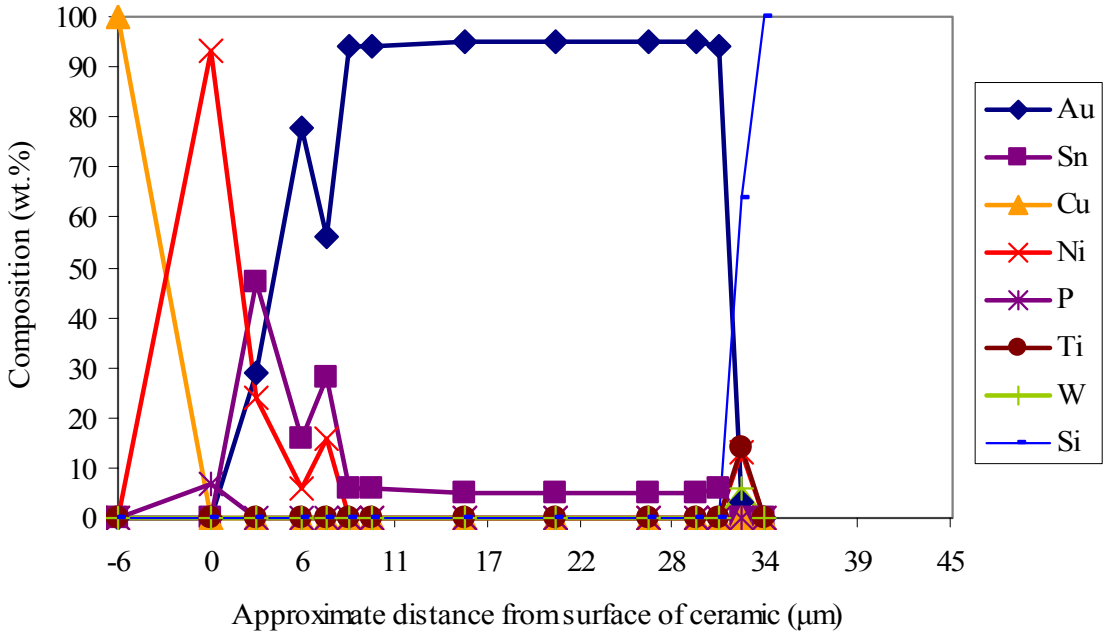


Figure 2-8 Element concentration plot across an AuSn as-brazed sample

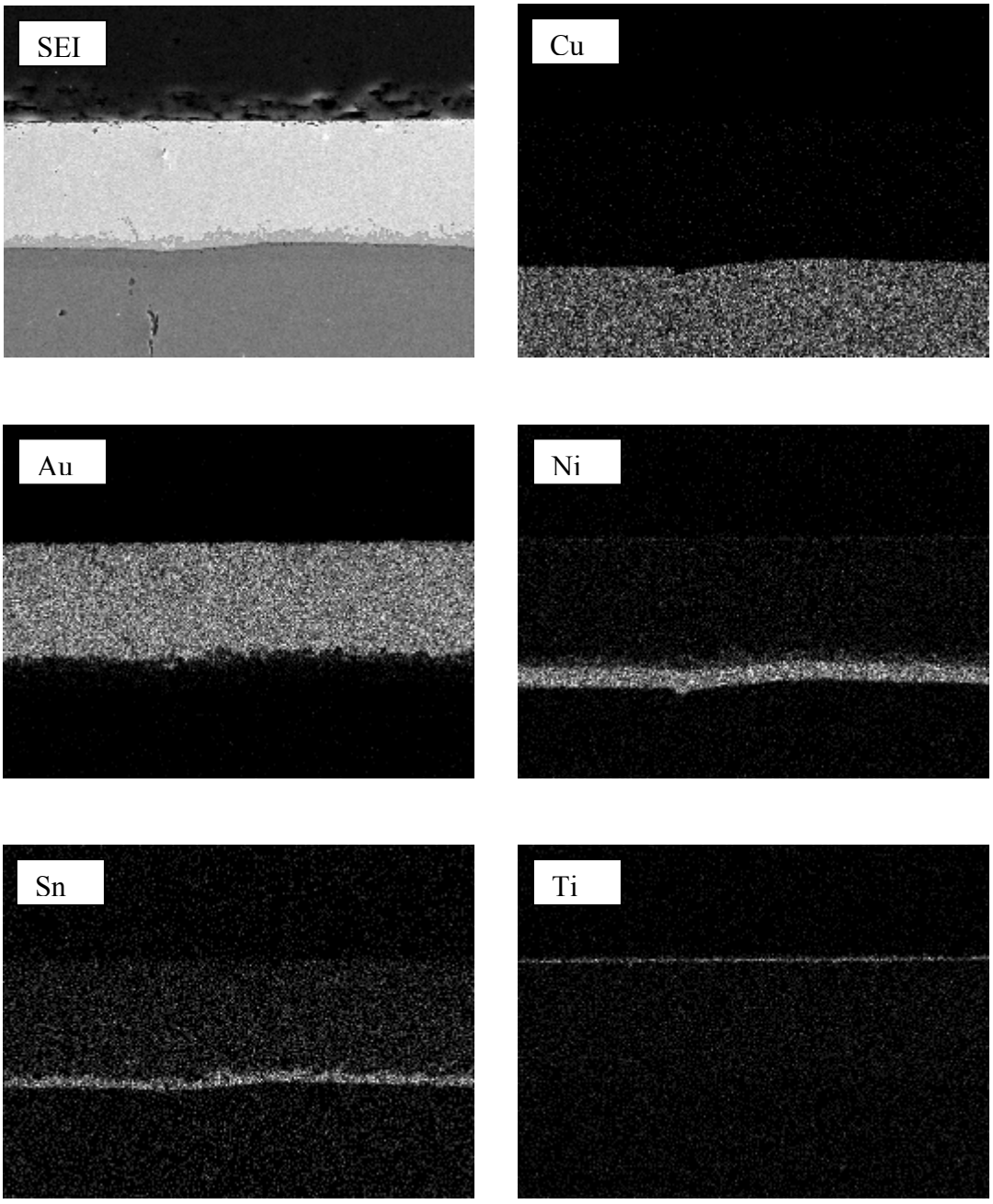


Figure 2-9 EDX elemental dot maps for an AuSn as-brazed sample

2.4 Reliability Test

2.4.1 High Temperature Storage Test

A high temperature storage test was used to determine the effect of time and temperature on the die shear strength. The apparatus used for this test was a Blue-M burn in chamber maintained at 400°C with ± 1°C accuracy over the entire test period.

In order to study the effect of Ni as a diffusion barrier and an adhesion layer, two types of DBC Al_2O_3 substrate were used in this test: DBC Al_2O_3 with electroless plated Ni:P and DBC Al_2O_3 with electrolytic plated Ni. The Ni layers were about 6μm thick, protected by a 0.10~0.20μm layer of immersion Au (IG). To lower the Sn concentration to less than 10wt%, a thick Au (20μm) layer was required, and two types of thick Au metallization were used in this study: thick Au on the chip backside and thick Au on the substrate. It is easier to electroplate the whole wafer (dicing the whole wafer into individual chips afterward) than to electroplate the individual DBC Al_2O_3 substrates, which is time consuming. On the other hand, with the IG surface finish, Ni and Cu will diffuse through the IG to the top of the substrate surface and oxidize in air during high temperature storage, so a thick Au layer (20μm) on the substrate was also used to test the effectiveness of this Au layer in retarding the diffusion and subsequent oxidation of the underlying Ni and Cu layers. In summary, four kinds of samples were built for the high temperature storage test:

- DBC on Al_2O_3 with electroless Ni:P, thick Au on substrate
- DBC on Al_2O_3 with electroless Ni:P, thick Au on chip
- DBC on Al_2O_3 with electrolytic Ni, thick Au on substrate
- DBC on Al_2O_3 with electrolytic Ni, thick Au on chip

The samples were tested at 100 hours, 250 hours, 500 hours, 1000 hours and 2000 hours with a group sample size of seven. A die shear test was used to evaluate the braze joint strength, and a cross-section sample was subjected to scanning electron microscopy /energy dispersive x-ray (SEM/EDX) analysis in order to detect intermetallic compound (IMC) formation and elemental interdiffusion during high temperature storage.

Figure 2-10 shows the die shear values for the four types of sample after aging at 400ºC. The Dage PC 2400 used to perform this test has a 100kg-f shear strength limit.

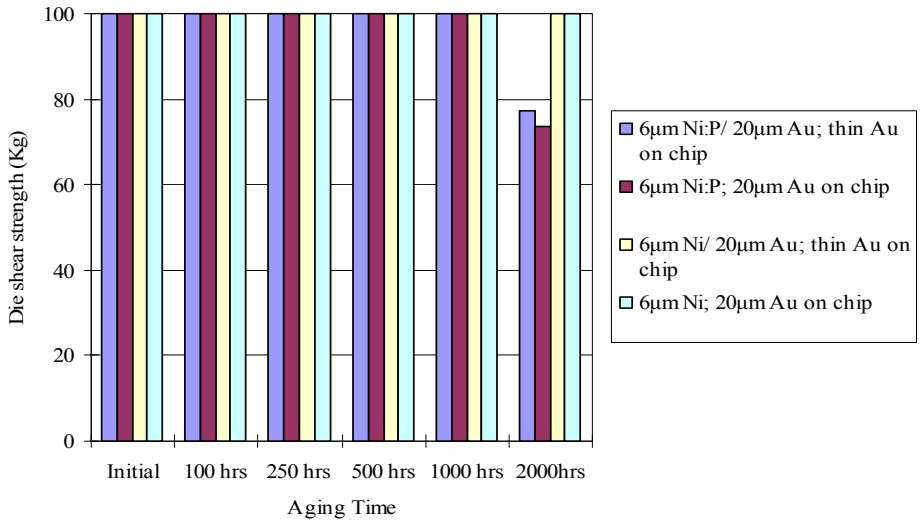


Figure 2-10 Die shear strength as a function of aging at 400ºC in air

The die shear strength of the electrolytic Ni samples (both thick Au on substrate and on chip) did not degrade after 2000 hours of thermal storage. However, the average die shear strength of the electroless Ni:P samples with Au on the substrate and Au on the chip degraded to 77.2kg and 73.6kg, respectively after 2000 hours aging at 400ºC in air.

Figure 2-11 shows an EDX element concentration cross-section plot of the sample after 2000 hours storage at 400ºC, and Figure 2-12 presents an EDX element composition cross-section analysis of the braze interface. In these two figures, the metallization of the

DBC Al_2O_3 substrate was Cu/ Ni:P/ immersion Au, with a thick Au (20µm) layer on the chip. By carefully studying these results, the following conclusions can be drawn:

1. Sn formed intermetallic compounds with Ti, resulting in higher Sn concentrations at the die surface.
2. A semi-continuous Ni:P:Cu layer formed during aging.
3. The AuSn braze layer was almost depleted of Sn, with only a residual level (about 1 wt%) of Sn remaining in the layer. Sn continued to react with Ni and Au, forming intermetallic compounds during aging. The Ni-Sn-Au intermetallic compounds were separated from the Ni:P:Cu under layer by a layer of 85 wt% Au-15 wt% Cu.
4. Cu was able to diffuse through the Ni:P and was found everywhere in the Au layer. Au was only able to diffuse into the Cu layer at the location where the Ni:P:Cu layer was broken.

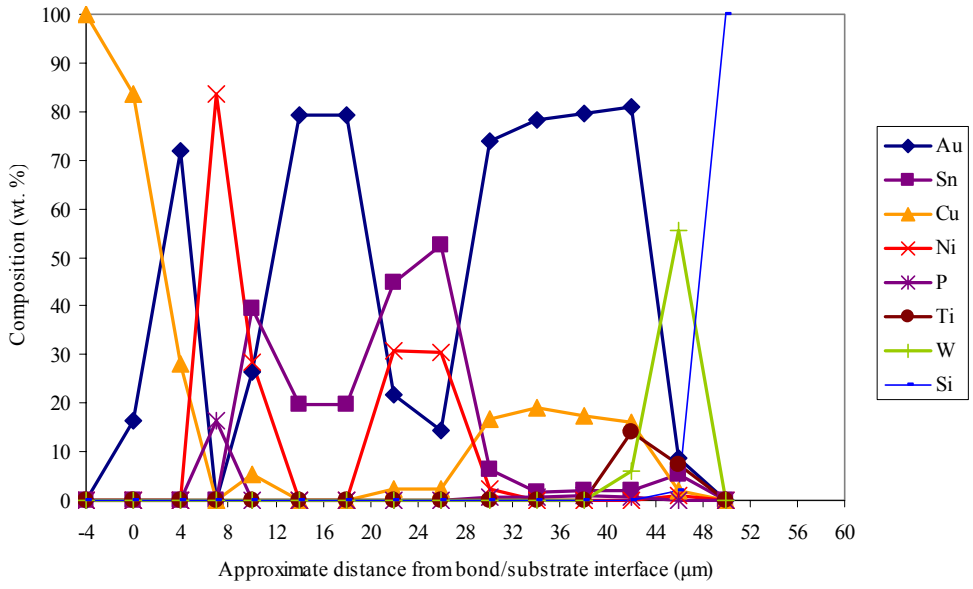
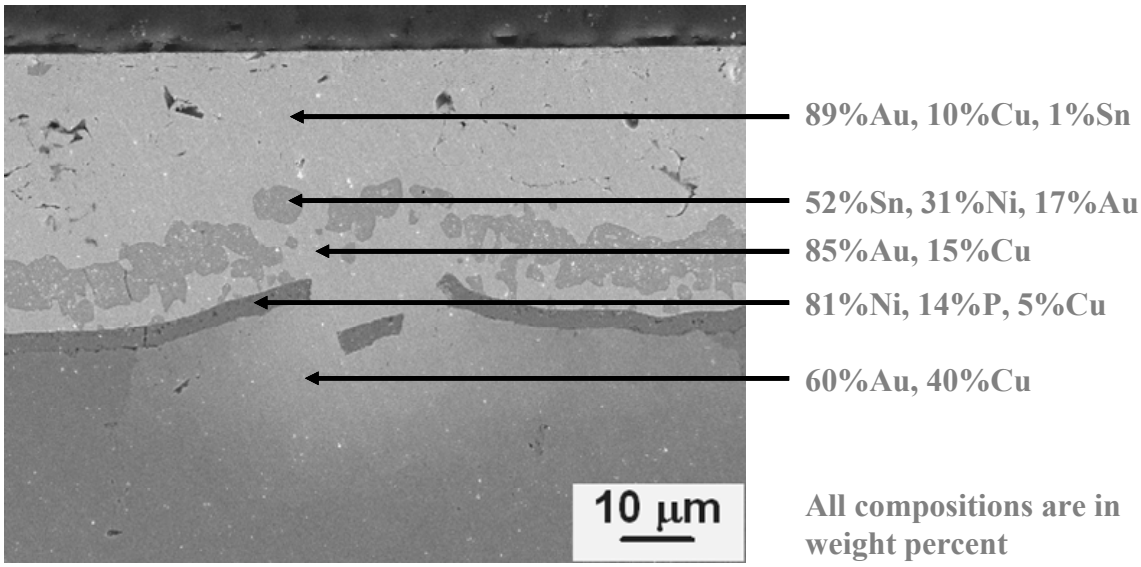
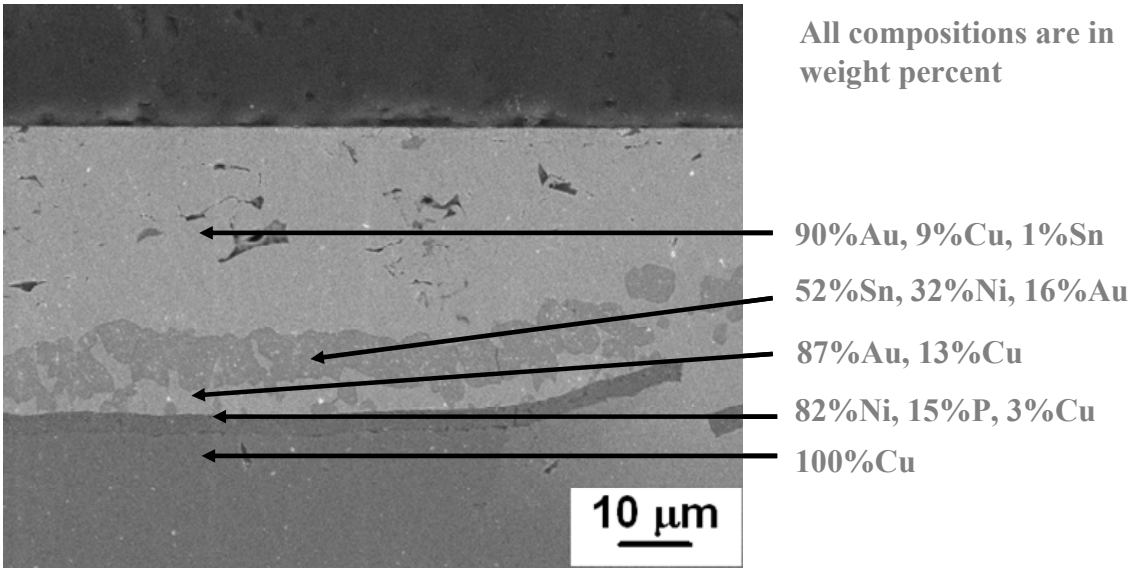


Figure 2-11 Element concentration plot across an AuSn brazed sample after 2000 hours storage at 400ºC, electroless Ni:P, thick Au on chip



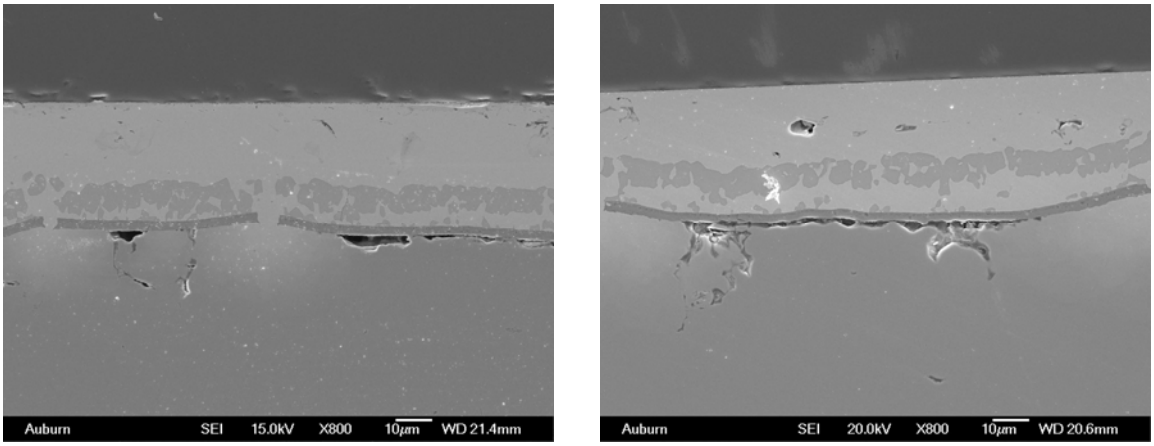
(a)



(b)

Figure 2-12 Cross-section of die attach after 2000 hours at 400ºC, electroless Ni:P, thick Au on chip, (a) at Ni:P:Cu broken area and (b) at Ni:P:Cu continous area

Figure 2-13 (a) shows voids that developed at the Cu-Ni:P interface after 1000 hours aging at 400ºC, and Figure 2-13 (b) shows a crack that developed at the Cu-Ni:P interface after 2000 hours aging at 400ºC. The Kirkendall effect may explain why the voids and cracks occurred. The Kirkendall effect is the formation of voids due to the different interdiffusion rate between two neighboring materials. The voids occur in the material having the greater diffusion rate. Figure 2-14 shows the Cu-Ni couple after 1 minute and 15 minutes aging at 1000ºC [60]. Cu and Ni are completely miscible. During high temperature aging, Cu diffuses into Ni and at the same time Ni diffuses in the opposite direction into the Cu at the Cu-Ni interface. However, the rates at which Cu and Ni diffuse are not equal. Cu diffuses more quickly than Ni does and the net result is that atomic-size vacancies are generated in the Cu to preserve the mass balance. As the diffusion proceeds, the vacancy concentration increases until super-saturation occurs, resulting in nucleation and the growth of voids.



(a) (b)

Figure 2-13 Cross-section of the die attach, (a) voids at Cu-Ni:P interface after 1000 hours aging and (b) cracks at Cu-Ni:P interface after 2000 hours aging at 400ºC

Figure 2-13 (b) shows Cu diffused into Ni:P and the braze layer, however, no Ni diffused into Cu layer. The different interdiffusion rate of Cu-Ni:P caused voids occur at the Cu-Ni:P interface after 1000 hours aging at 400ºC and the coalescence of these voids resulted in the cracks at the Cu-Ni:P interface after 2000 hours thermal storage. This observation is consistent with that reported by Kelly [61]. The lower die shear strength was due to occurrence of these cracks.

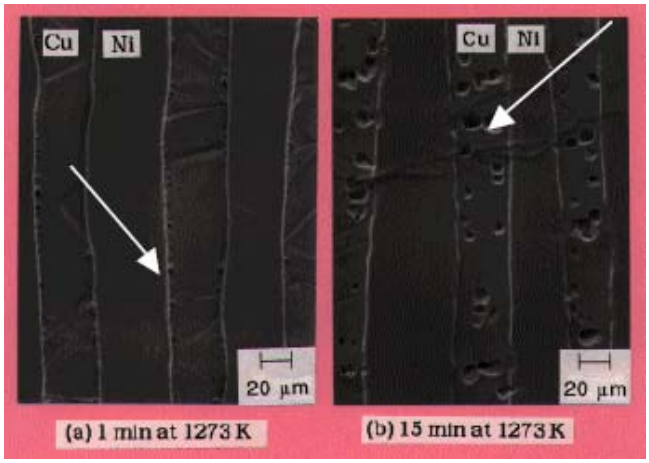


Figure 2-14 Kirkendall effect of Cu-Ni couple after 1 minute and 15 minutes aging at 1000ºC [60]

Figure 2-15 shows an EDX element concentration cross-section plot of the sample after 2000 hours storage at 400ºC, and Figure 2-16 presents an EDX element composition cross-section analysis of the braze interface after 2000 hours storage at 400ºC. In both these figures, the metallization of the DBC Al_2O_3 substrate was Cu/Ni/Au (20µm). By carefully studying these results, it is possible to draw the following conclusions:

1. A series of intermetallic compounds was formed, consuming the Sn and the Ni layer.
2. Cu was able to diffuse through the Ni into the Au layer.

3. The complex intermetallics formed had good adhesion and strength after aging.

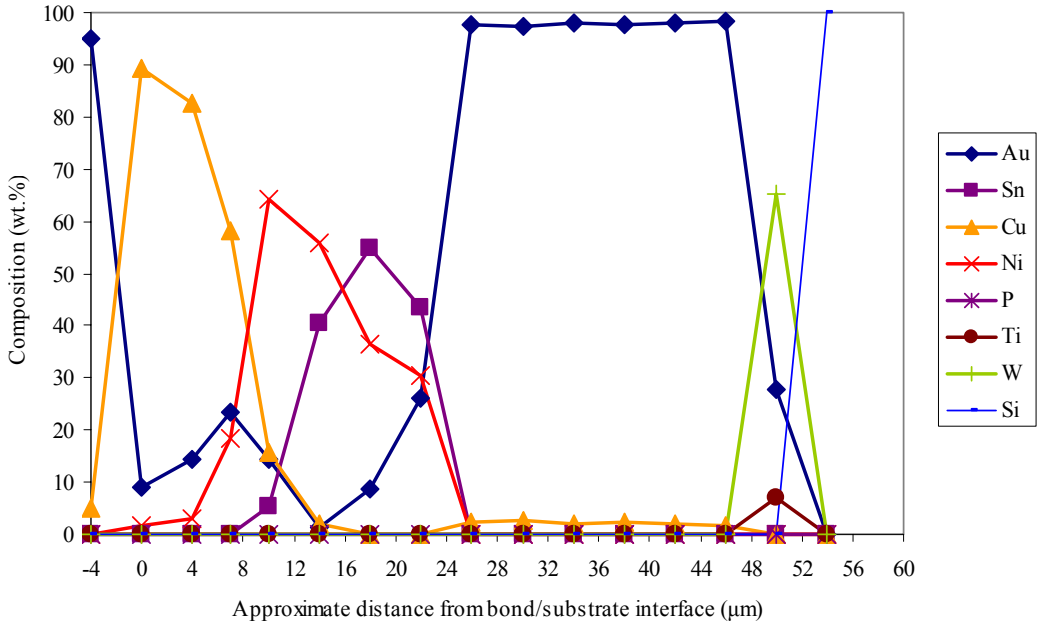


Figure 2-15 Element concentration plot across an AuSn brazed sample after 2000 hours storage at 400ºC; electrolytic Ni, thick Au on substrate

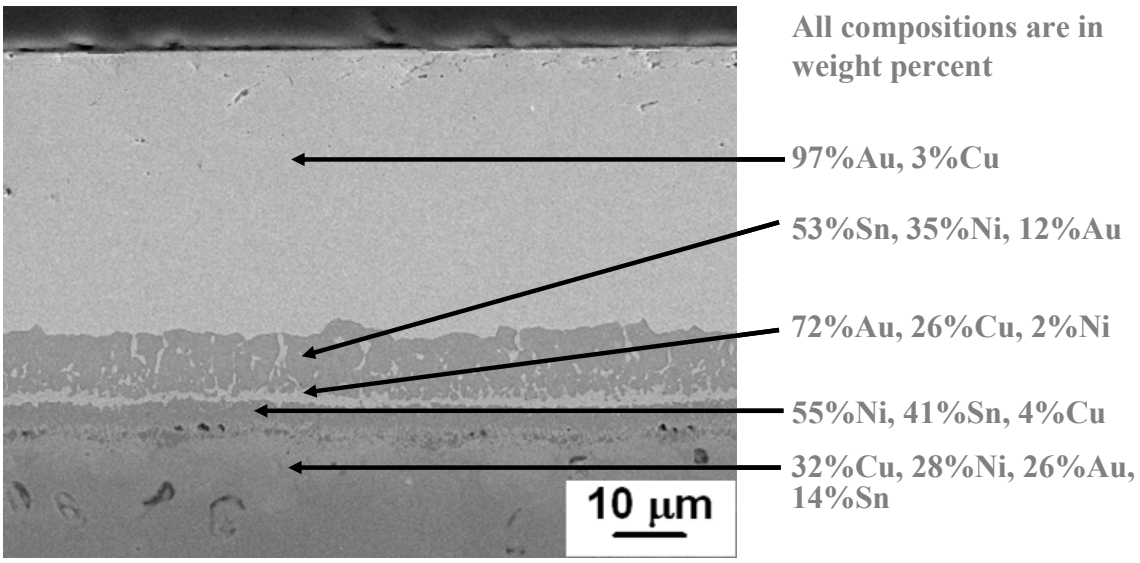


Figure 2-16 Cross-section of die attach after 2000 hours at 400ºC, electrolytic Ni, thick Au on substrate

Figure 2-17 shows voids that developed at the Cu-Ni interface after 2000 hours aging at 400ºC. The Kirkendall effect, discussed for the Cu-Ni:P couple, will also explain why the voids occurred at the Cu-Ni interface. Because Au, Ni and Sn diffused into Cu layer, the voids developed at the Cu:Ni interface were smaller than those developed at the Cu-Ni:P interface, and no crack developed at the Cu-Ni interface which ensured >100kg-f die shear strength after 2000 hours aging.

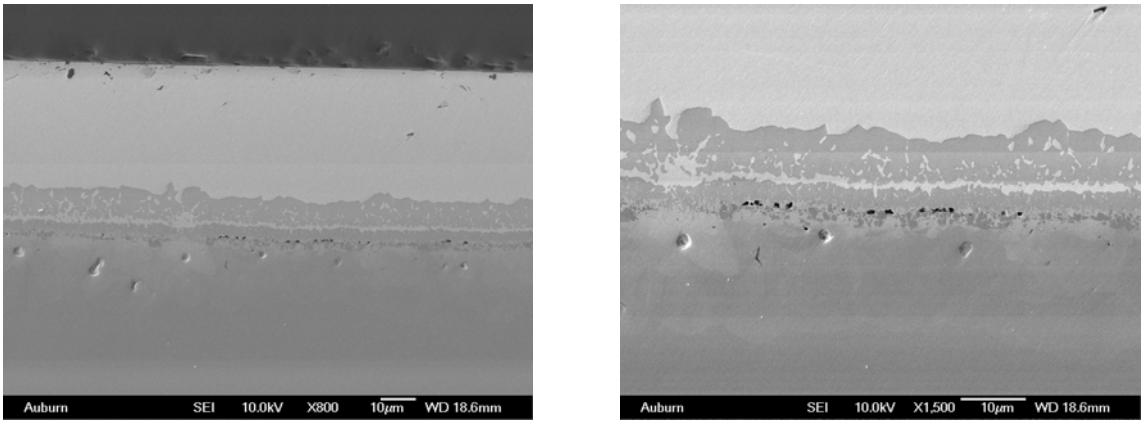


Figure 2-17 Cross-section of the die attach, showing voids at Cu-Ni interface after 2000 hours aging at 400ºC

A second test was performed to validate the die shear test results using DBC Al_2O_3 substrates with electrolytic Ni and electroless N:P at both 1µm and 6µm thickness. The die shear data for the samples built with 6µm Ni (both electrolytic Ni and electroless Ni:P) DBC Al_2O_3 substrates replicated the original results, as shown in Figure 2-18. Figure 2-19 shows the die shear strengths for the samples built with 1µm Ni (both electrolytic Ni and electroless Ni:P) DBC Al_2O_3 substrates after high temperature storage at 400ºC. The as-brazed samples initially had a die shear strength of >100kg-f, but after 500 hours, the average die shear strength for the four types of sample dropped to about 2.4 kg-f.

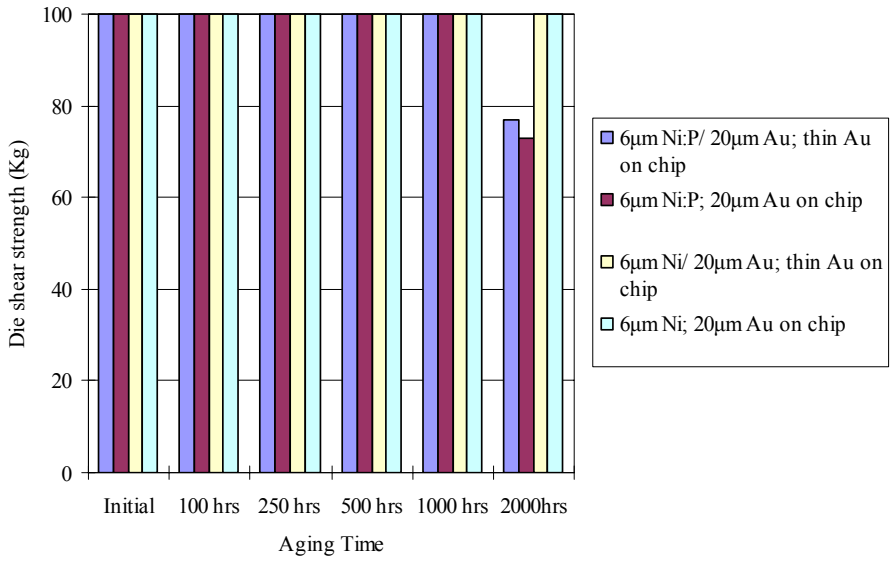


Figure 2-18 Die shear strength as a function of aging, confirmation test, 6 µm Ni DBC Al_2O_3 substrates, 400ºC in air

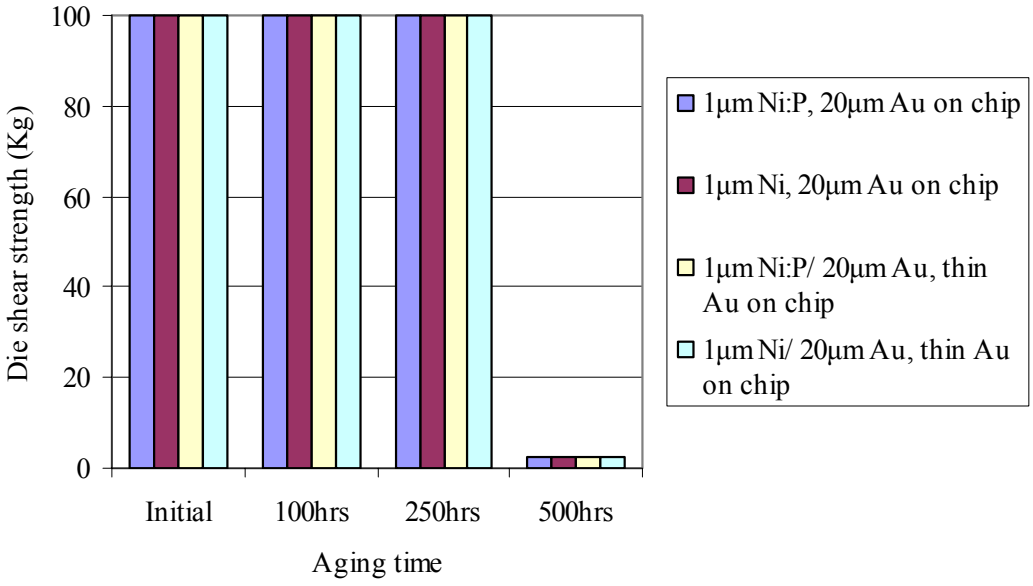


Figure 2-19 Die shear strength as a function of aging, confirmation test, 1µm Ni DBC Al_2O_3 substrates, 400ºC in air

2.4.2 Thermal Cycle Test

Thermal cycle tests were performed to determine the ability of the SiC assembly to withstand cyclic exposures at high and low temperature extremes. The tests were designed to simulate conditions encountered in typical applications. The thermal cycle profile consisted of 30 minutes ramp from 35°C to 350°C, then soak for 10 minutes, followed by 20 minutes cool down from 350°C to 35°C, as shown in Figure 2-20. Three high temperature substrates were evaluated in the test, Si_3N_4, AlN and Al_2O_3. All substrates had Cu/Ni/Au metallization and the SiC chip had 20μm thick Au metallization. Table 2-1 lists the dimension of the substrates used in this test. A thin film adhesion layer and plated copper were used on the AlN to achieve a thin Cu layer in order to minimize the CTE induced stresses on the AlN substrate. The Al_2O_3 substrate was direct bond copper foil, and the Si_3N_4 substrate had the copper foil attached by active metal brazing.

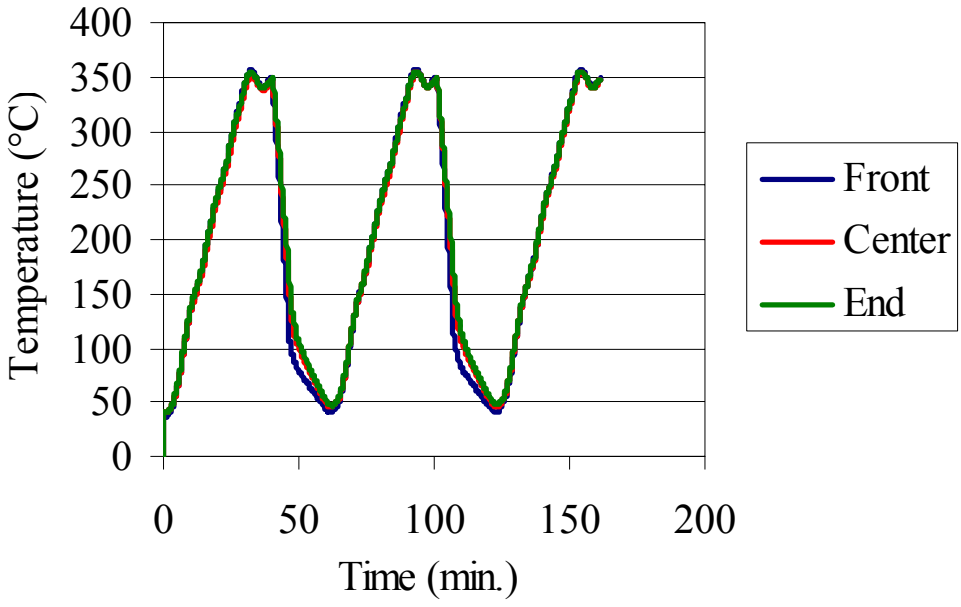


Figure 2-20 Thermal cycle test profile

Table 2-1 Substrates dimensions

Substrate	**Size (mil^2)**	**Ceramic Thickness (µm)**	**Cu Thickness (µm)**	**Ni Thickness (µm)**	**Type of Cu**
AlN	1000x1000	255	45	3	Thin film/plated
Si_3N_4	200x200	642	154	6	AMB
Al_2O_3	200x200	630	190	6	DBC
Al_2O_3	1000x1000	630	250	1	DBC

The samples subjected to thermal cycling were tested after 100 cycles, 250 cycles, 500 cycles and 1000 cycles with a group sample size of seven. A die shear test was used to evaluate the die shear strength, and a cross-section sample was subjected to SEM/EDX analysis to determine if any cracks developed during the test. Figure 2-21 presents the die shear strength after the thermal cycle test for the substrates tested. The initial die shear strength for all samples was > 100kg-f. Thermal cycle samples built with 1µm Ni DBC Al_2O_3 substrates failed after 100 cycles, with the average die shear strength degrading to 23kg-f. Thermal cycle samples built with 6µm Ni DBC Al_2O_3 substrates failed after 250 cycles, with the average die shear strength degrading to 30kg-f. Thermal cycle samples built with 6µm Ni AMB Si_3N_4 substrates failed after 500 cycles, with the average die shear strength degrading to 25kg-f. Thermal cycle samples built with thin film/plated Cu AlN substrates had an average die shear strength > 100kg-f after 1000 cycles.

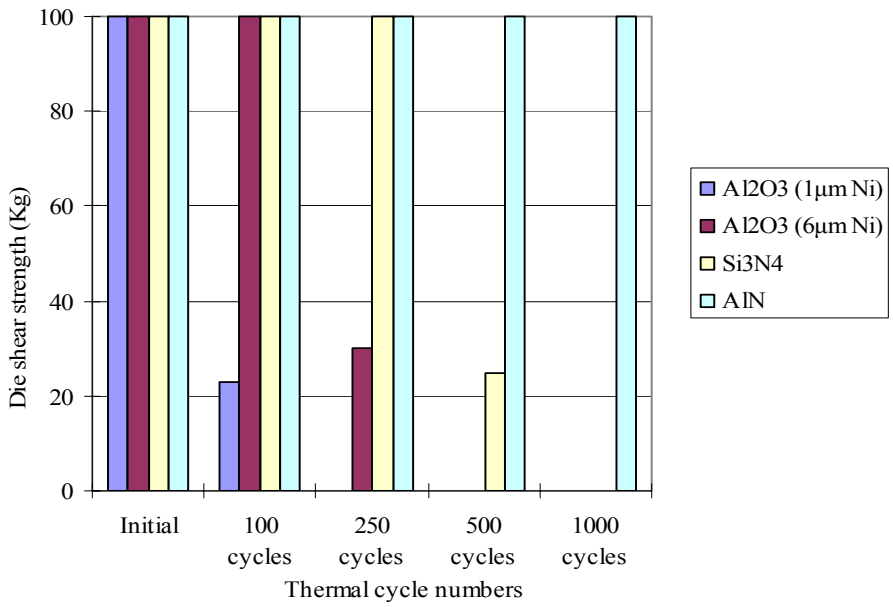
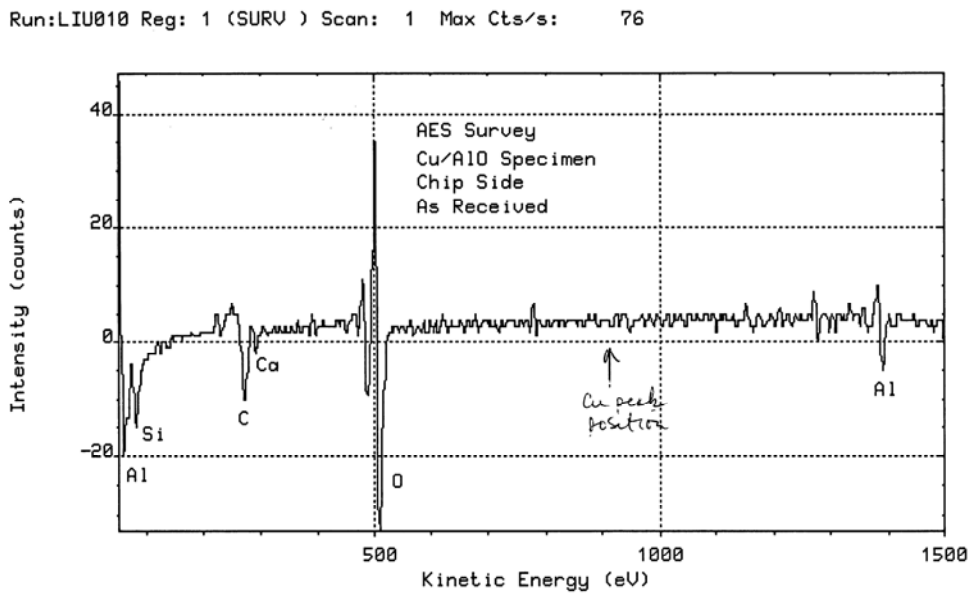
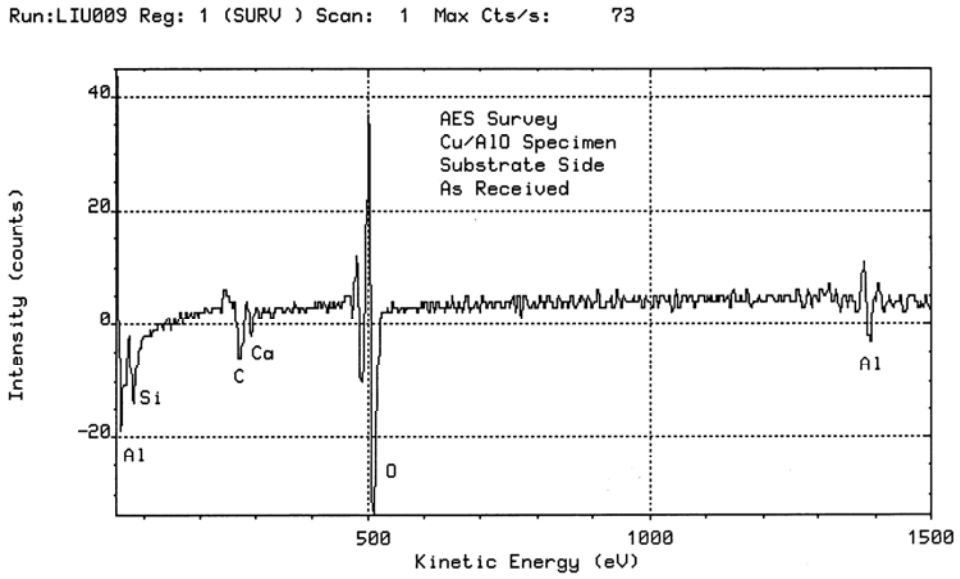


Figure 2-21 Die shear strength as a function of thermal cycle numbers

After 100 cycles, the direct bond Cu foil delaminated from the 1μm Ni Al_2O_3 substrate. Figure 2-22 shows the Auger emission spectroscopy (AES) analysis results on the delaminated substrate surface and Cu foil surface. Al, Si, Ca, O and C were detected on both surfaces. Al, Si, Ca and O are the composition elements of the Al_2O_3 substrate, while the C is a common contaminate on sample surface exposed to the atmosphere. It was also observed that no Cu remained on the Al_2O_3 substrate, and the Cu foil was covered with a thin layer of Al_2O_3, so it is reasonable to conclude that the Al_2O_3 substrate surface fractured during thermal cycle test as a result of the CTE mismatch induced stresses between the Cu foil and Al_2O_3 substrate.



(a)



(b)

Figure 2-22 AES results after 100 thermal cycles, DBC Al_2O_3 substrate with 1μm electroless Ni:P, (a) Cu foil surface and (b) substrate surface

Cracks in the braze layer and braze-TiW delamination also developed during thermal cycling. Figure 2-23 and Figure 2-24 show cross-section pictures of the samples with the 1μm electrolytic Ni DBC Al_2O_3 substrate and 1μm electroless Ni:P DBC Al_2O_3 substrate after 100 cycles, showing the braze crack and braze-TiW delamination that developed during thermal cycling.

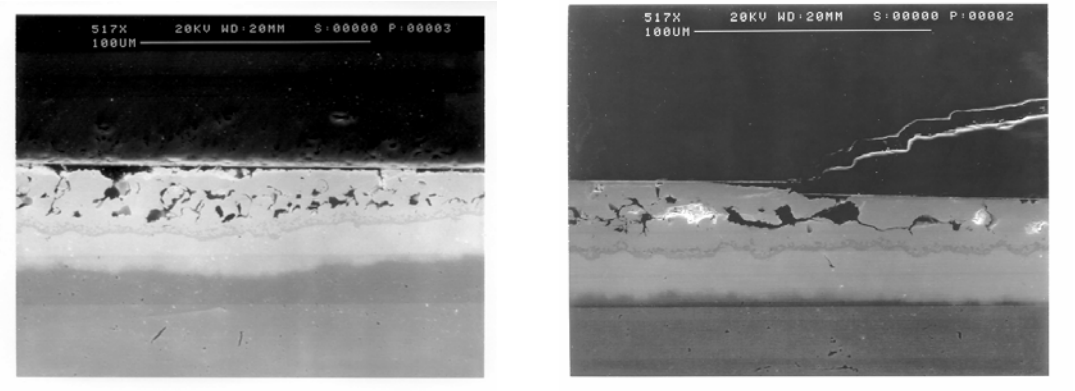


Figure 2-23 Cross-section of braze layer after 100 thermal cycles, showing crack in braze layer and braze-TiW delamination. DBC Al_2O_3 with 1μm electrolytic Ni

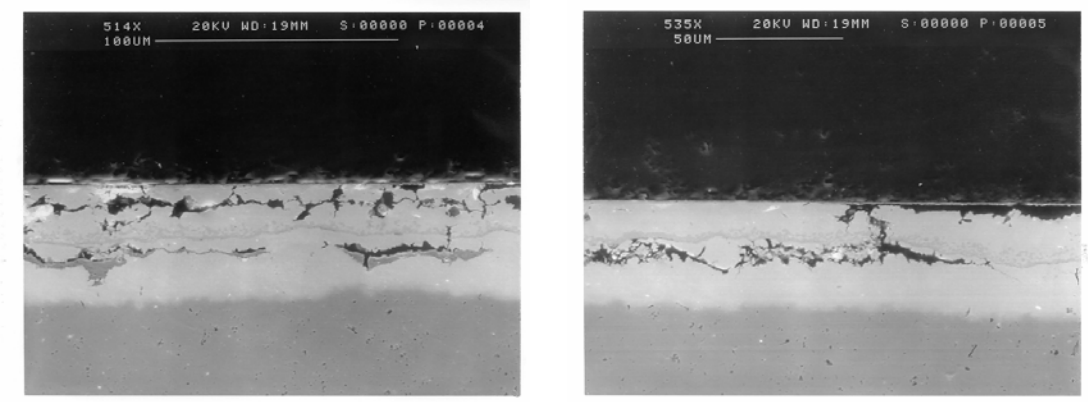


Figure 2-24 Cross-section of braze layer after 100 thermal cycles, showing crack in braze layer and braze-TiW delamination. DBC Al_2O_3 with 1μm electroless Ni:P

The direct bond Cu foil delaminated from the Al_2O_3 substrate with 6μm Ni after 250 cycles, as shown in Figure 2-25. By comparison the two types of DBC Al_2O_3 substrates (1μm Ni vs. 6μm Ni), it was found that the substrates with thinner Cu foil

(190μm vs. 250μm) had better thermal cycling performance due to the less CTE mismatch induced stress exerted on the Al_2O_3 surface.

Figure 2-25 Cu foil delamination after 250 thermal cycles

Figure 2-26 and Figure 2-27 show cross-section pictures of the samples built with the 6μm electrolytic Ni DBC Al_2O_3 substrate and 6μm electroless Ni:P DBC Al_2O_3 substrate after 250 cycles, showing that braze crack and braze-TiW delamination developed during thermal cycling.

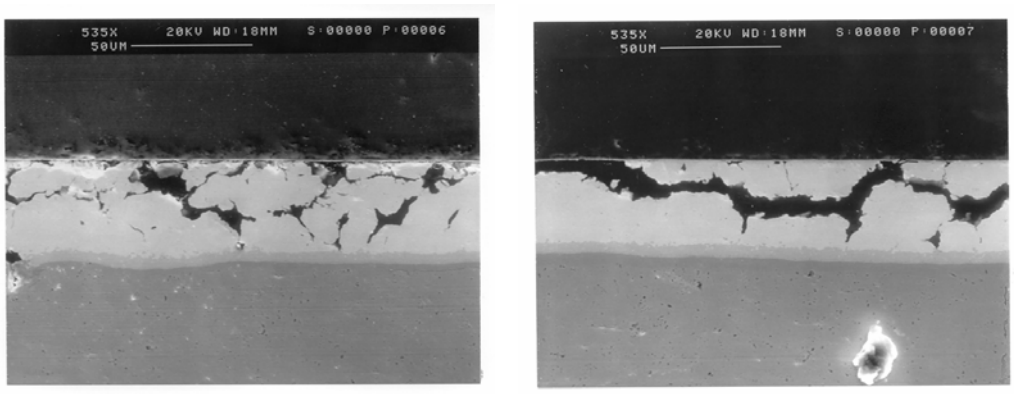


Figure 2-26 Cross-section of braze layer after 250 thermal cycles, showing cracks in the braze layer and braze-TiW delamination. DBC Al_2O_3 substrate with 6μm electrolytic Ni

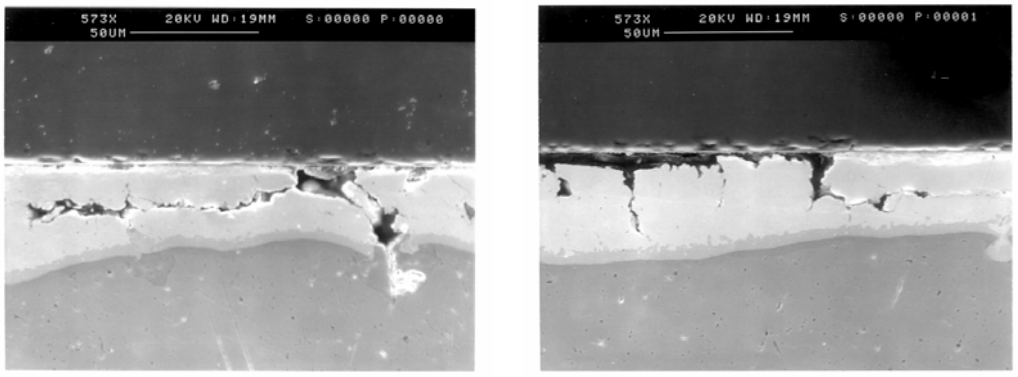
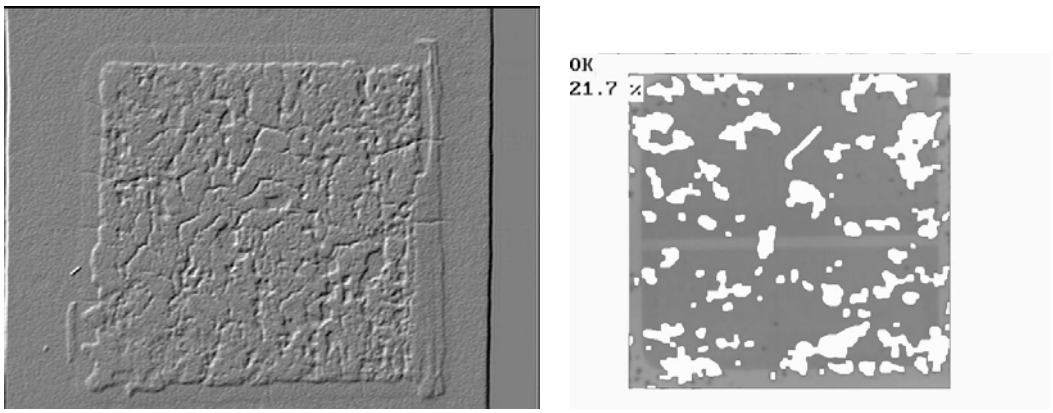


Figure 2-27 Cross-section of braze layer after 250 thermal cycles, showing cracks in the braze layer and braze-TiW delamination. DBC Al_2O_3 substrate with 6μm electroless Ni:P

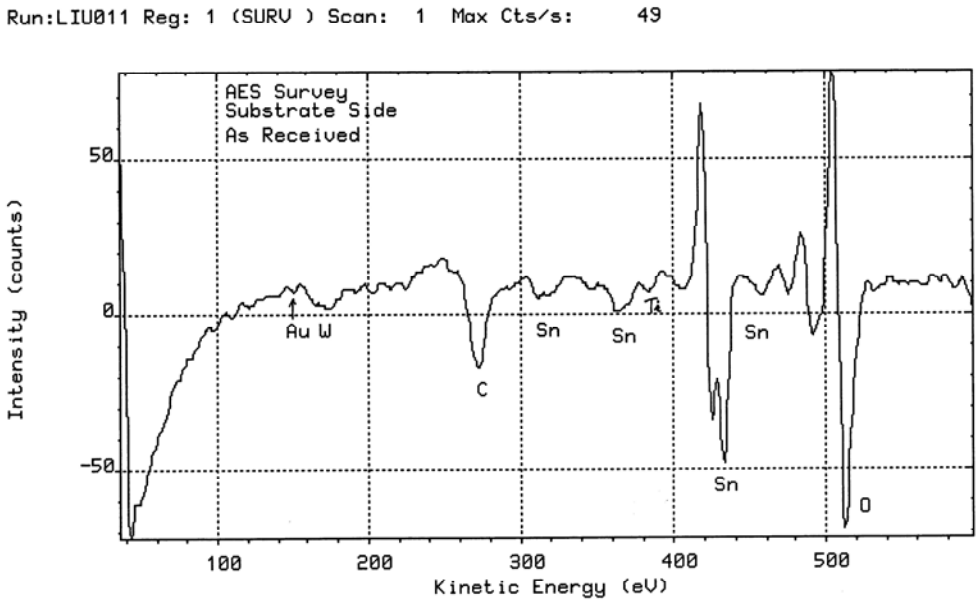
Figure 2-28 (a) shows an x-ray image of the DBC Al_2O_3 substrate (after the die shear test) in relief mode, showing the cracks that developed in the braze layer during thermal cycling. Figure 2-28 (b) shows an x-ray image of the corresponding chip (after the die shear test) in void calculation mode in order to calculate how much braze remained on the chip. The white area represents the AuSn braze residue. In total, the chip had 21.7% of its area covered by braze residue. Since most of the chip area was free of braze residue, the braze-TiW delamination was a major failure mode compared to the cracks developed in braze layer.



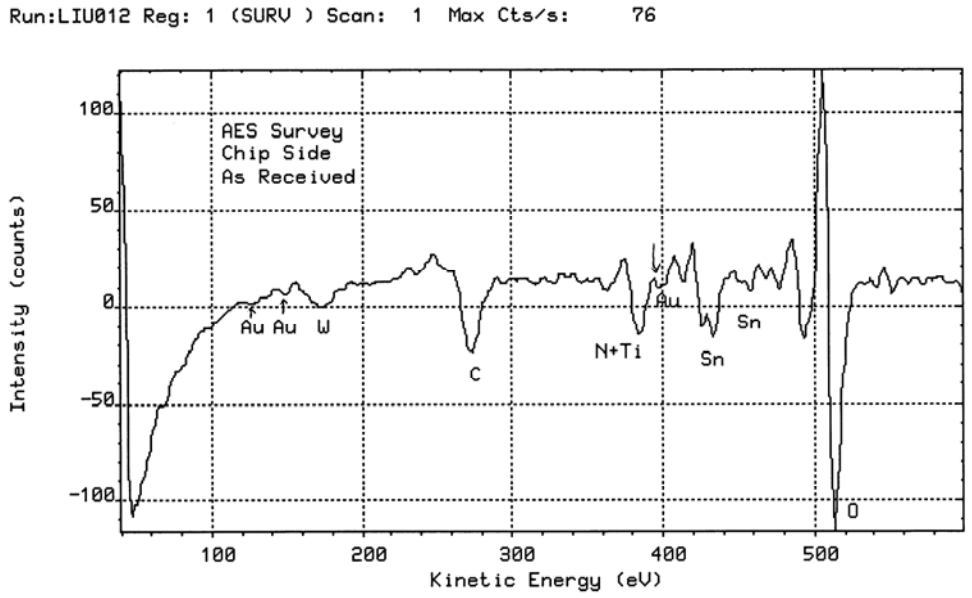
(a) (b)

Figure 2-28 (a) X-ray image in relief mode, showing cracks in the braze layer and (b) x-ray image in voids calculation mode, calculating braze residue area percentage on chip surface; DBC Al_2O_3 substrate with 6μm electroless Ni:P after 250 thermal cycles

AES analyses of the surface of the substrate and chip are shown in Figure 2-29. Here, the elements Au, Sn, Ti, and W are present on both the substrate surface and chip surface, although the intensity of the Sn on the substrate side and Ti on the chip side are significantly higher, and the elements C and O are the adventitious surface contaminates that are present on any "as received" sample exposed to air. The results proved that braze-chip delamination occurred at the braze-TiW interface.



(a)



(b)

Figure 2-29 AES results after 250 thermal cycles, DBC Al_2O_3 with 6μm electroless Ni:P, (a) substrate side and (b) chip side

Thermal cycling samples built with Si_3N_4 substrates failed at 500 cycles. Figure 2-30 shows an optical image of the Si_3N_4 assembly after 500 thermal cycles. The bottom copper foil delaminated from the Si_3N_4 substrate, but the top copper metallization only delaminated slightly at the edges because the SiC chip helped constrain the Cu. Figure 2-31 shows the AES analysis results for the delaminated copper foil surface and the corresponding substrate surface. Si, N, Cl, C and O were detected on both surfaces. Si, N and Cl are the composition elements of the Si_3N_4 substrate, while C and O are the contaminants that are present on any "as received" sample surface exposed to air. So it is reasonable to assume that the Si_3N_4 substrate surface fractured during the thermal cycle test. Compared to DBC Al_2O_3 substrate, the AMB Si_3N_4 substrate had longer thermal cycling life due to the thinner Cu foil and the higher fracture toughness.

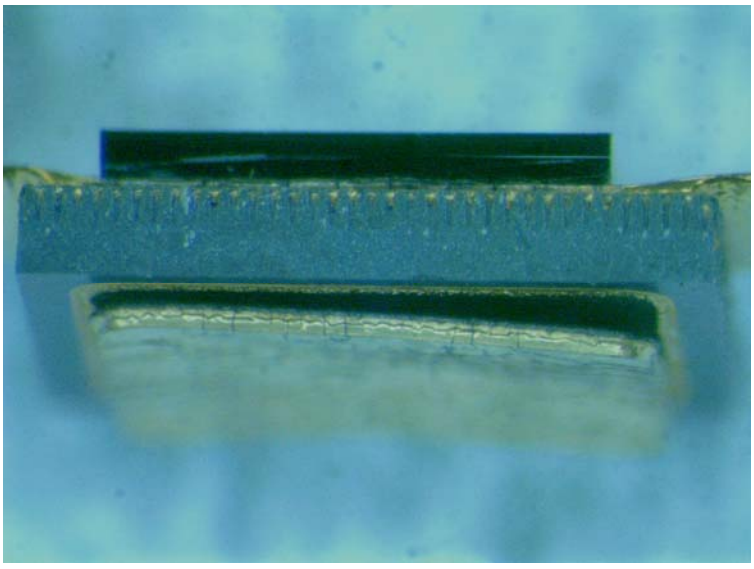
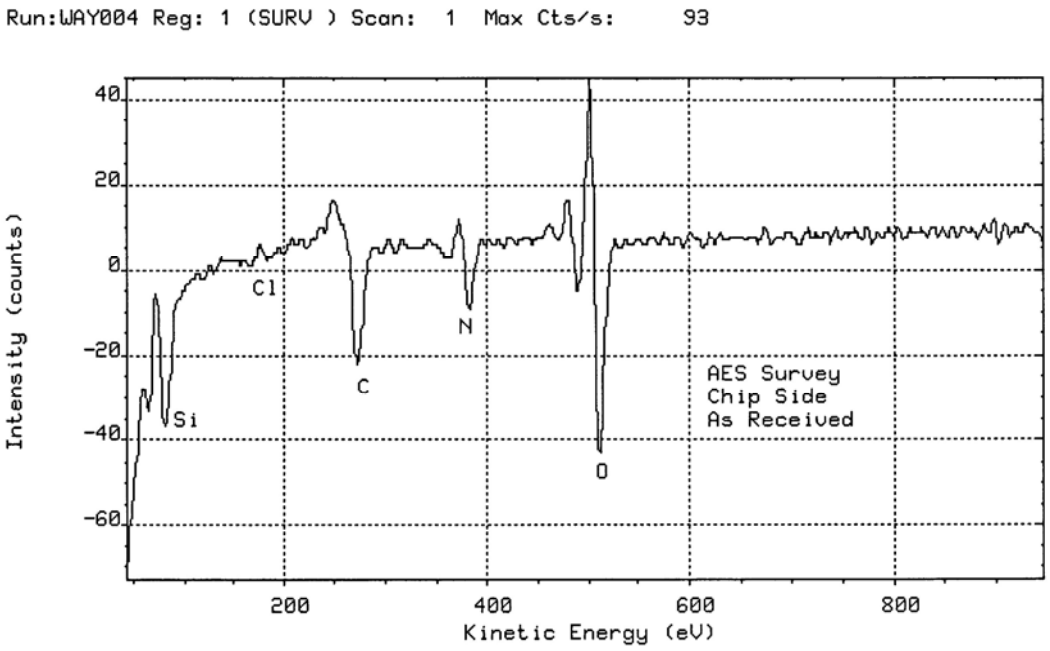
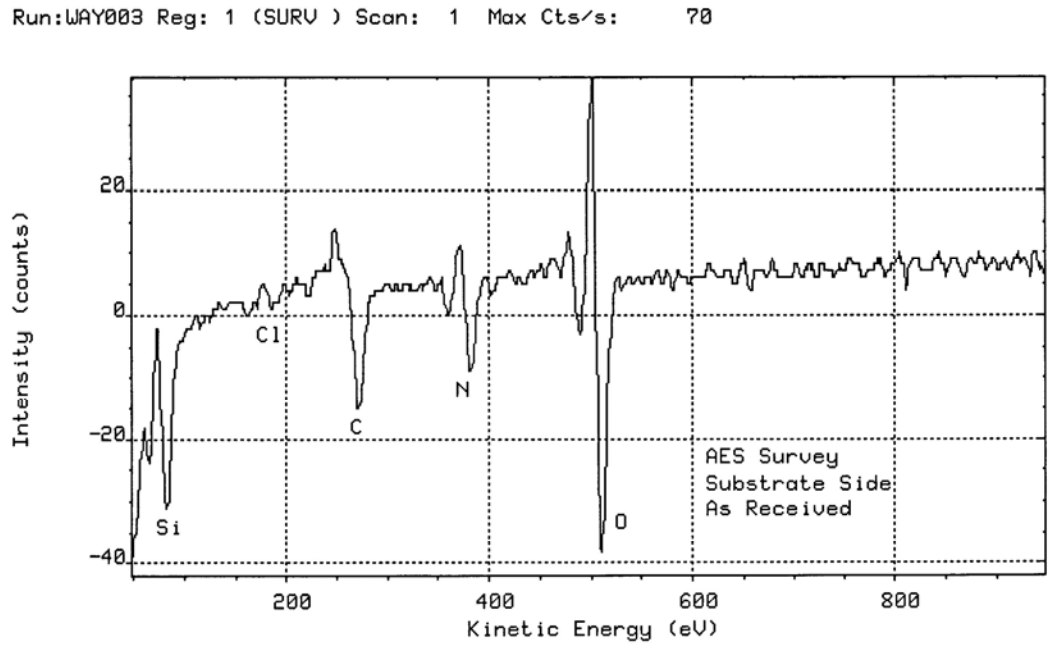


Figure 2-30 Si_3N_4 assembly after 500 cycles, showing the Cu foil delamination



(a)



(b)

Figure 2-31 AES results of Si_3N_4 substrate after 500 thermal cycles, (a) Cu foil surface and (b) substrate surface

The SEM cross-section pictures in Figure 2-32 show the cracks in the braze layer and the delamination at the braze-TiW interface that developed during thermal cycling, both of which were caused by CTE mismatches between the SiC die, the braze material and the Si_3N_4 substrate.

Figure 2-33 (a) shows an x-ray image of the substrate (after the die shear test) in relief modes, showing the cracking that developed in the AuSn braze layer during thermal cycling. Figure 2-33 (b) shows an x-ray image of the corresponding chip in voids calculation mode, where the white area represents the AuSn braze residue. The results show that only 3.8% of the chip area is still covered by AuSn braze. It is possible to draw the conclusion that the braze-TiW delamination was a major failure mode compared to the cracks developed in braze layer.

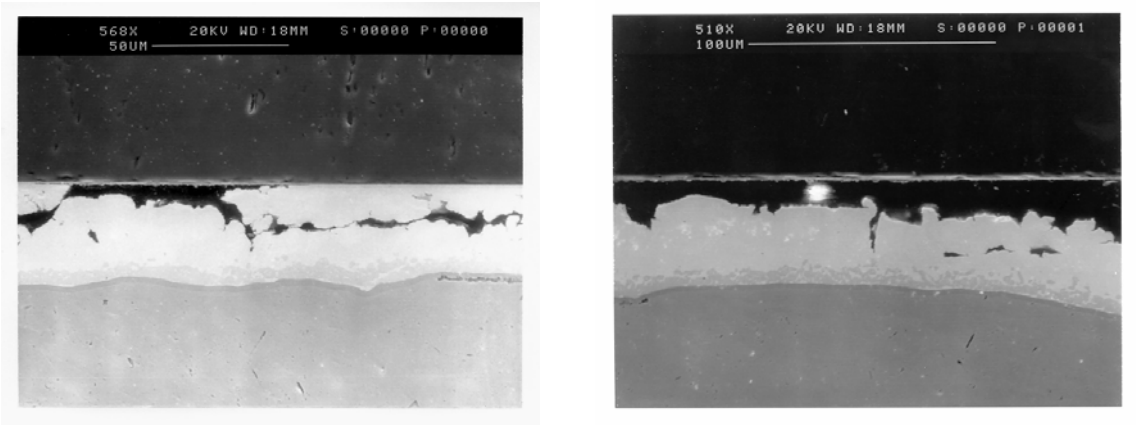
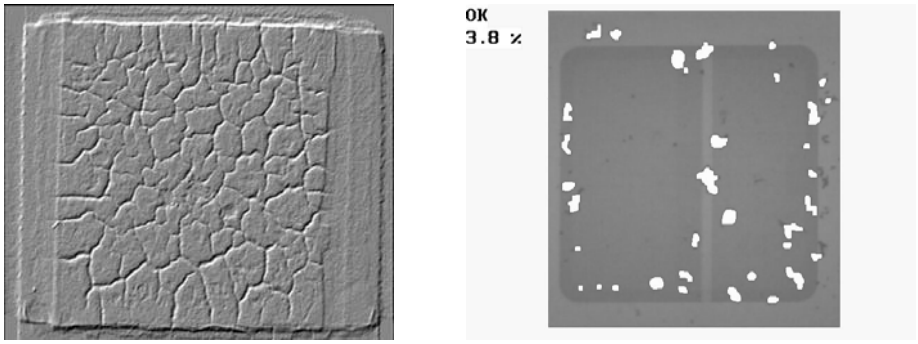


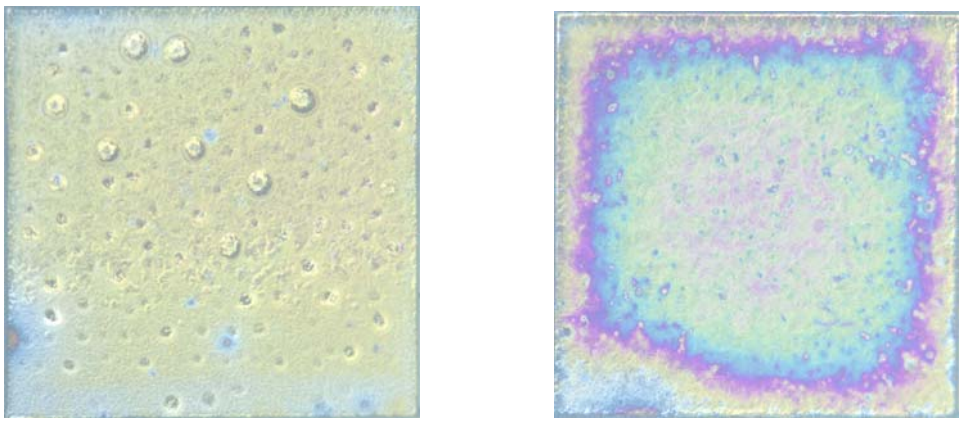
Figure 2-32 Cross-section of the braze layer after 500 thermal cycles, showing cracks in the braze layer and braze-TiW delamination. Si_3N_4 substrate after 500 thermal cycles



(a) (b)

Figure 2-33 (a) X-ray image in relief mode, showing cracks in the braze layer and (b) x-ray image in voids calculation mode, calculating braze residue area percentage on chip surface; AMB Si_3N_4 substrate after 500 thermal cycles

The AlN substrate samples had good die shear strength after 1000 cycles, although after 100 thermal cycles the thinner copper on the AlN had severe blistering, as shown in Figure 2-34. The blistering occurred randomly on one side of the substrate, while the other side showed no signs of blistering. This indicates some process variation in the thin film adhesion layer or in the plating on the front and back of the AlN substrate. For these wide temperature range applications, additional work is therefore necessary to understand the root cause of this problem.



(a) (b)

Figure 2-34 AlN substrate after 100 thermal cycles, (a) side with blistering and (b) side without blistering

2.5 Au-Ge Braze

Gold-germanium (Au-Ge) braze is used in the microelectronics industry for various assembly applications, but primarily for attaching dies to substrates and substrates to carriers. The braze alloy is of eutectic composition, with 87.5 wt% Au 12.5 wt% Ge, and has a melting point of 361°C. It is therefore ideal for high temperature applications. Figure 2-35 shows the Au-Ge phase diagram. The system is simple compared to AuSn alloy, being composed of [57]:

- Liquid phase L
- Terminal solid solution Au, having about 1 wt% solid solubility of Ge in Au
- Terminal solid solution Ge, with a very small solid solubility of Au in Ge (less than 13.6×10^{-4} at% at 361ºC)

Severe voiding has been encountered with AuGe braze material [62]. As the AuGe braze wets the Au coated surface (usually immersion Au), the Au coating is dissolved into the braze, and once the Au coating is completely consumed, the underlying material is exposed to the braze. Usually this layer is plated Ni, and the Ge reacts with the Ni to form low temperature Ni-Ge intermetallic compounds such as Ni_5Ge_3 and Ni_2Ge, as the Ni-Ge phase diagram in Figure 2-36 would suggest. As the Ge migrates, the braze is depleted of Ge. Once this occurs, the eutectic structure is destroyed and segregated gold-rich islands form, resulting in midline planar voids [62].

To solve this problem, a thicker gold layer (5μm) was plated on the substrate, and a low peak temperature (390°C) and a short time (60 seconds) at the peak temperature were used to ensure that there was good wetting but minimum gold dissolution. The reflow profile is shown in Figure 2-37.

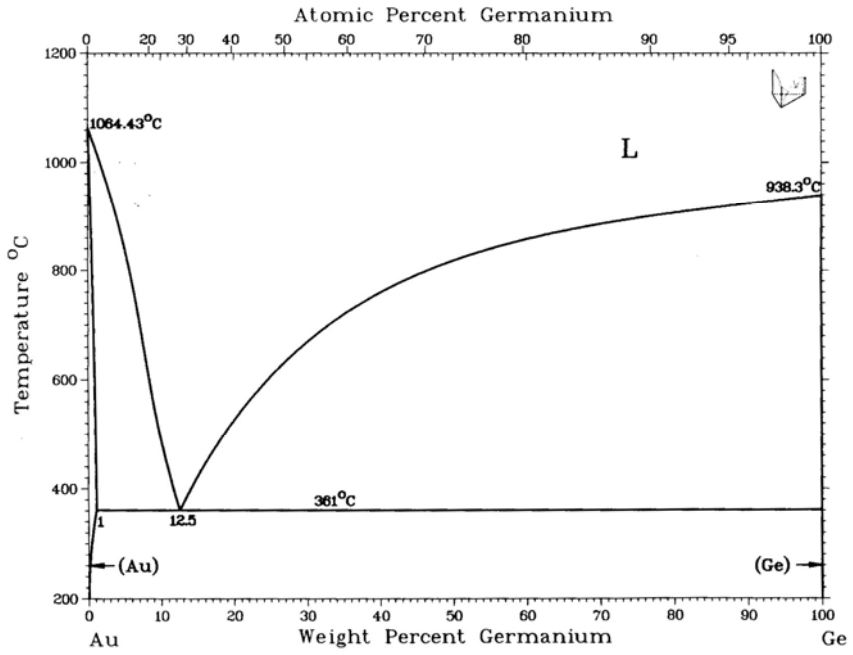


Figure 2-35 Au-Ge phase diagram [57]

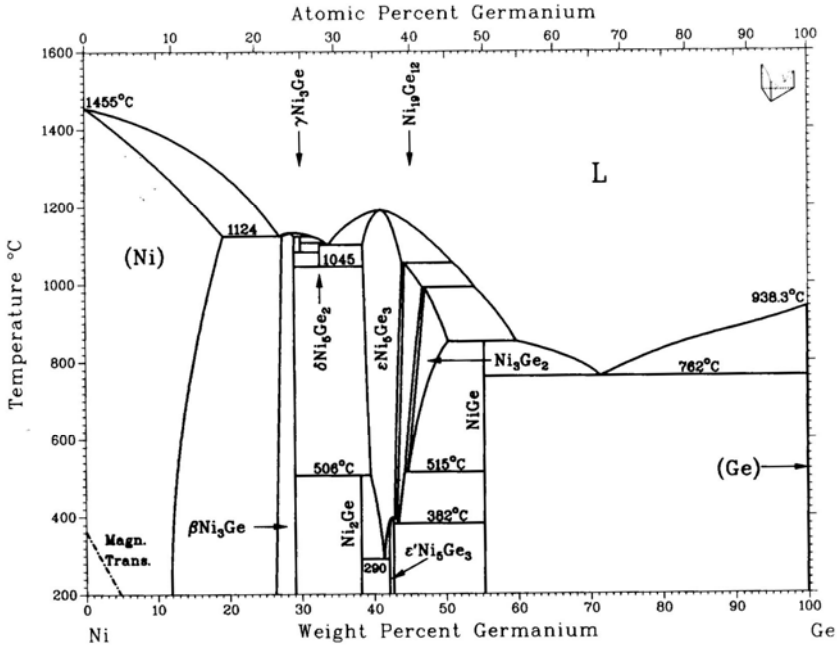


Figure 2-36 Ni-Ge phase diagram [57]

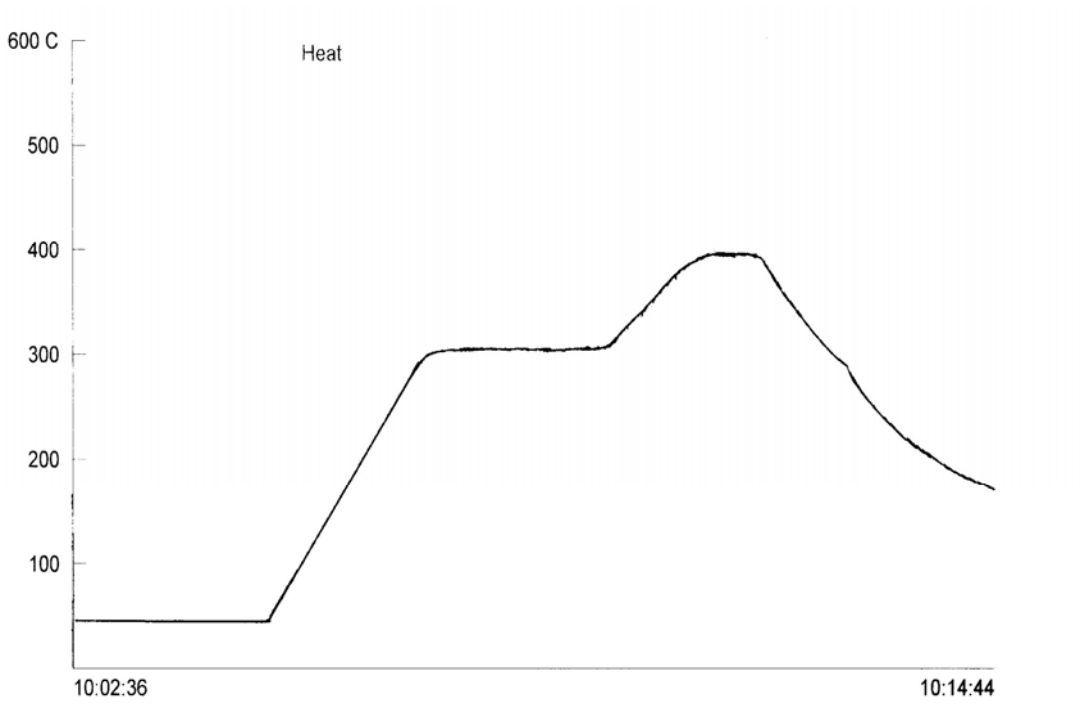
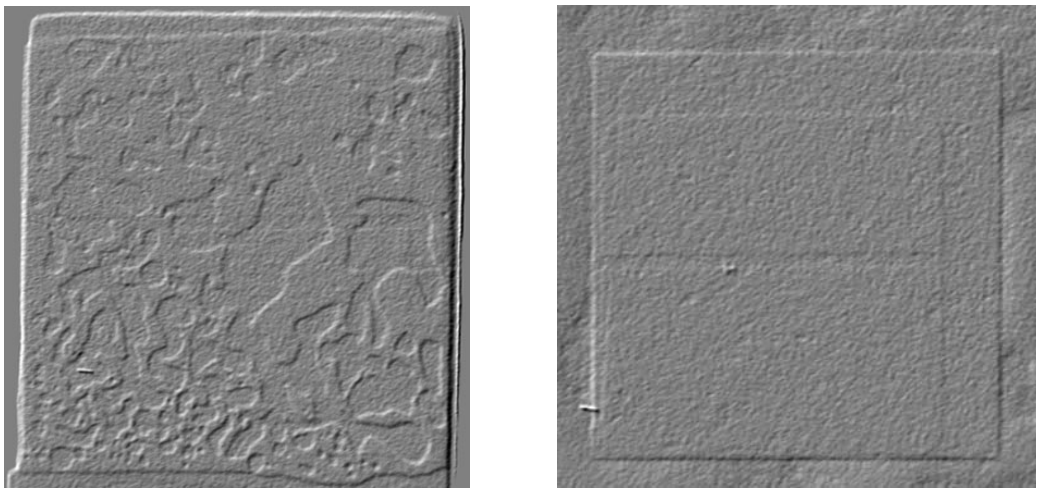


Figure 2-37 Au-Ge braze reflow profile

The braze joint quality was tested by x-ray image in relief mode. Figure 2-38 compares the results before and after the process optimization, showing the void-free bond that can be achieved with the above technique. The bond strength was tested by die shear test initially and after high temperature storage at 300ºC. Aging test samples were built with DBC Al_2O_3 substrates with both electroless Ni:P(6µm)/Au(5µm) and electrolytic Ni(6µm)/Au(5µm) surface finishing using the optimized process. The SiC die had Ni_2Si/Ti/Ti-W/Au (1000 Å /2000 Å /2000 Å) metallization. Figure 2-39 shows the die shear strength after aging at 300ºC. Once again, the sample size was 7. Initial die shear strengths were > 100kg-f. The results indicate that the die shear strength of samples built with electrolytic Ni DBC Al_2O_3 substrates degraded much faster than those built with electroless Ni:P DBC Al_2O_3 substrates, but both ultimately degraded.



(a) (b)

Figure 2-38 X-ray relief mode images of Au-Ge bond (a) before optimization and (b) after optimization

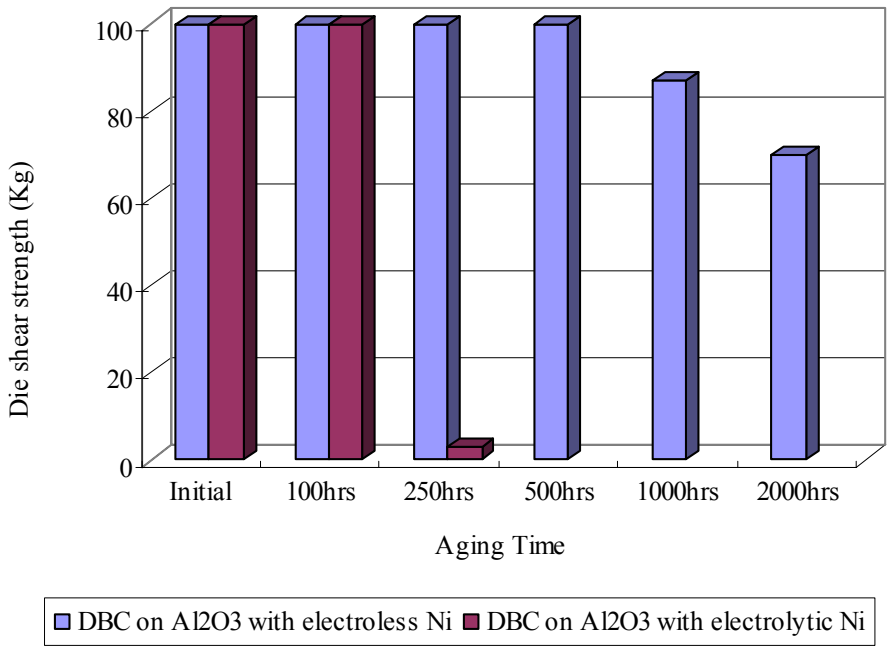


Figure 2-39 AuGe braze die shear strength as a function of aging at 300ºC

2.6 Au-Ge-Ag Braze

The Au-Ge braze alloy has a eutectic melting temperature of 361°C. If a noble metal is added into the binary system, then the melting temperature of this ternary system will increase. Silver was chosen for this purpose, and the ternary phase diagram of Au-Ge-Ag is presented in Figure 2-40. The DBC Al_2O_3 substrate was electroplated with 20μm silver, and if the silver is completely diffused into the Au-Ge, the ternary alloy will be composed of Au 55 wt% Ge 7.6 wt% and Ag 37 wt% and the melting point of this alloy will increase to 487°C. The silver plating setup was the same as that used for gold electroplating (section 2.3.3), except that the platinized anode is replaced with a silver bar. The silver plating process flow was:

- Soak in clean TSC-1501 for 2 minutes
- Rinse in DI water
- Soak in acid active TAS-1, at room temperature for 2 minutes
- Rinse in DI water
- Electroplating with Technic silver strike at room temperature, with 1volt potential applied for 1minute
- Rinse in DI water
- Electroplating with silver 1025 under 10ASF at room temperature for 20 minutes
- Rinse

TAS-1 is a blend of dry acid salts that replaces sulfuric and hydrochloric acid for pickling metals prior to electroplating, giving a cleaner, smut free, active surface that produces better adhesion and more uniform metal coatings. Silver Strike is used prior to

the application of the final silver plating layer to assure good adhesion. Silver 1025 is a potassium cyanide formulation, modified to achieve various hardness requirements for electronic purposes [59]. Figure 2-41 shows a DBC Al_2O_3 substrate plated with 20μm Ag.

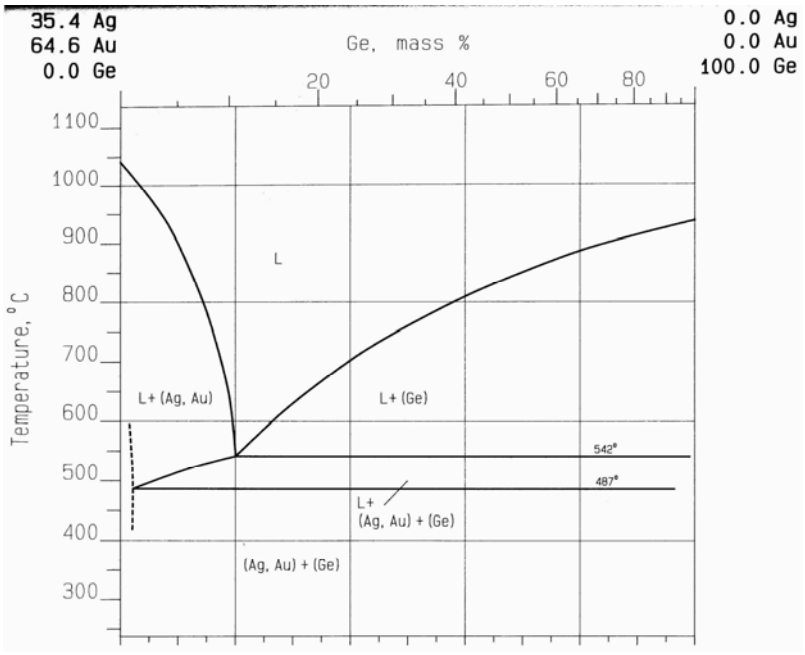


Figure 2-40 Au-Ge-Ag phase diagram [63]

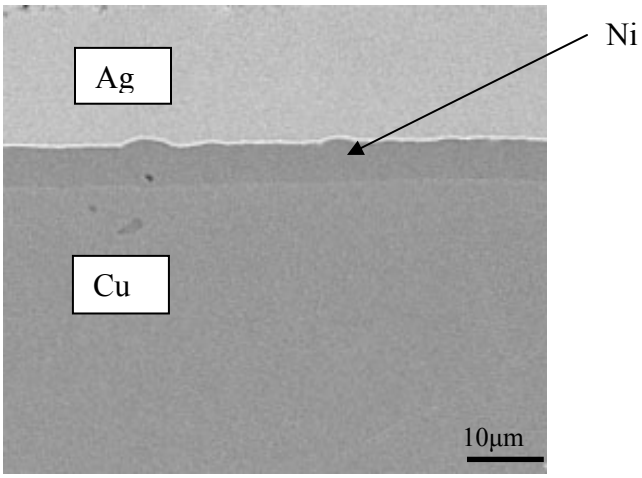


Figure 2-41 DBC Al_2O_3 substrate plated with 20μm Ag

As shown in Figure 2-42, the brazing profile for the Au-Ge-Ag braze started with 10 minutes at 400ºC to melt the Au-Ge alloy, which was followed by 3 hours at 350ºC to allow the Ag to diffuse into the Au-Ge. A void free bond was achieved, as shown in the x-ray image in Figure 2-43.

The Au-Ge-Ag braze had an initial die shear strength >100kg-f (equipment limit), but the die shear strength decreased significantly with storage at 400ºC after only 50 hours, as the Ge diffused into the Ni, forming weak IMC. The results were similar for both electrolytic Ni and electroless Ni:P, with electrolytic Ni failing slightly faster. Figure 2-44 presents the die shear strength after aging at 400ºC.

Figure 2-45 and Figure 2-46 show the energy dispersive x-ray elemental dot maps for Au-Ge-Ag braze on electroless Ni:P/Au, initially and after 100 hours storage at 400ºC. In the as-brazed sample, the Ge has formed separate crystals due to the limited solid solubility of Ge in Au and Ag. After 100 hours aging at 400ºC, the Ag and Au were mixed together, and the Ge and Ni layers almost completely overlapped, indicating the formation of IMC.

The energy dispersive x-ray elemental dot maps for Au-Ge-Ag braze on electrolytic Ni/Au, both for an initial sample and after 100 hours storage at 400ºC, are shown in Figure 2-47 and Figure 2-48, respectively. In the as-brazed sample, the Ge has formed separate crystals due to the limited solid solubility of Ge in Au and Ag. After 100 hours aging at 400ºC, similar phenomena to those observed in the electroless Ni:P were seen, and once again Ge and Ni almost completely overlapped.

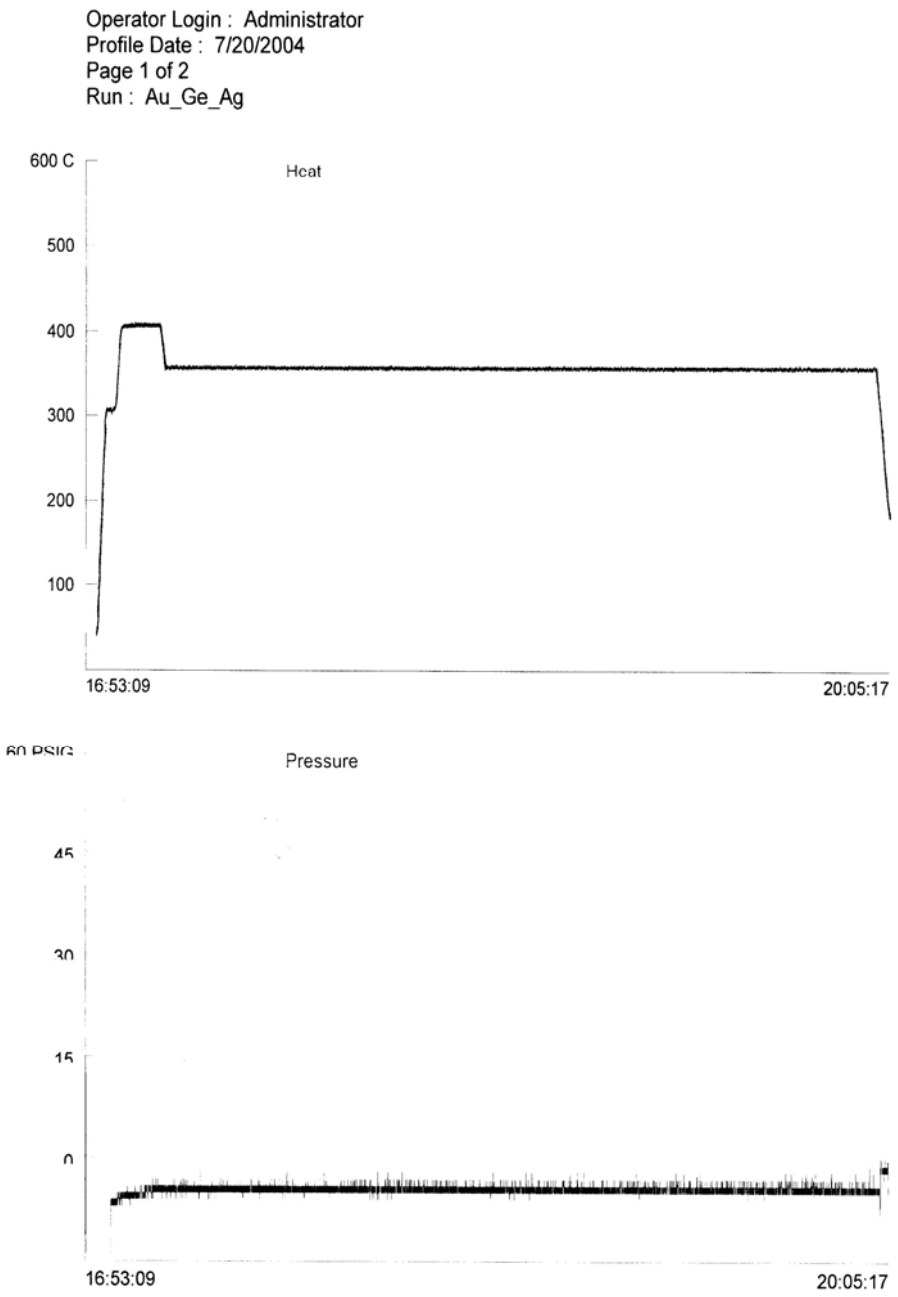


Figure 2-42 Au-Ge-Ag brazing profile

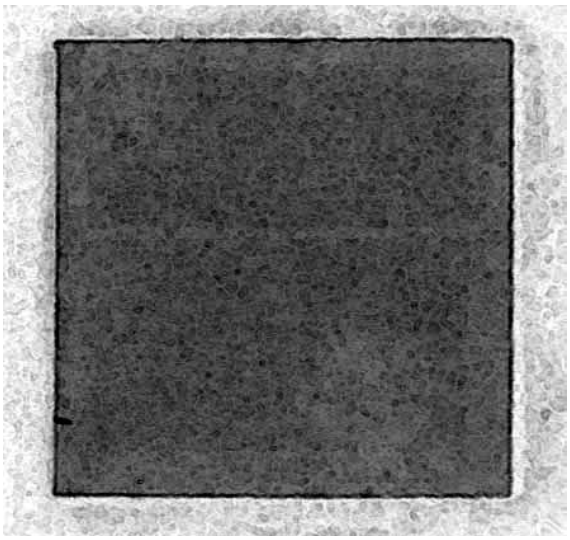


Figure 2-43 X-ray picture of Au-Ge-Ag as-brazed sample

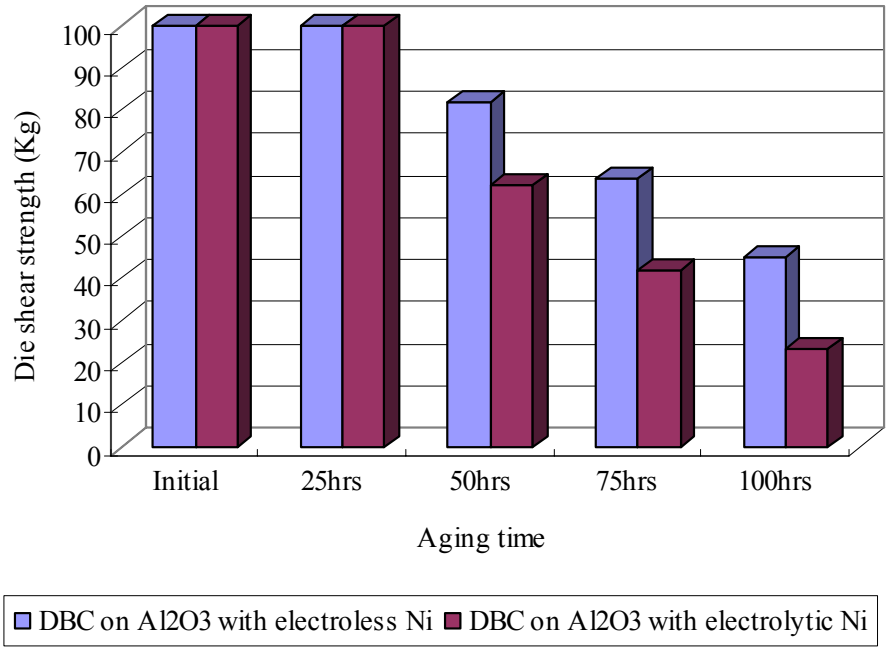


Figure 2-44 Au-Ge-Ag die shear strength as a function of aging at 400ºC

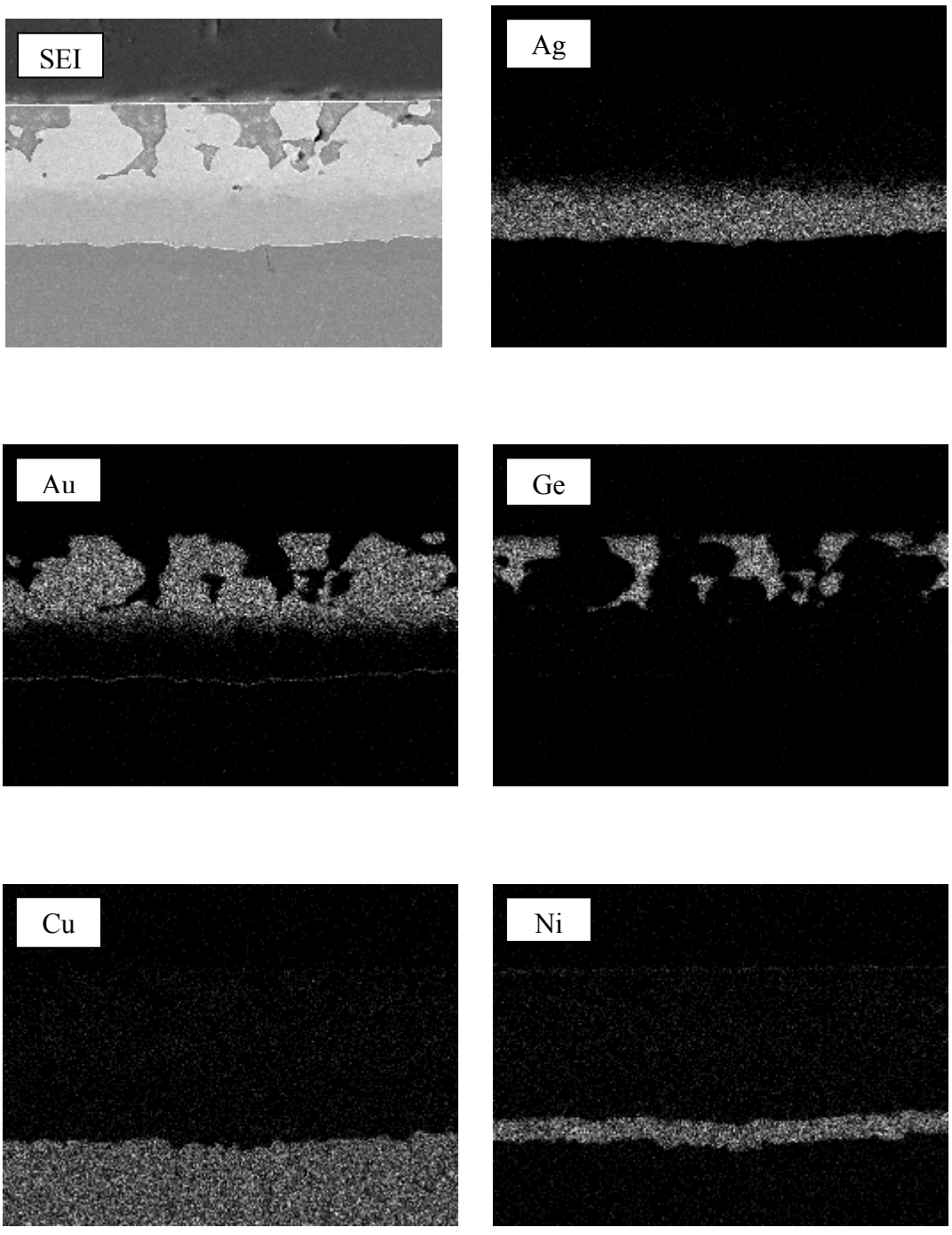


Figure 2-45 EDX elemental dot maps for Au-Ge-Ag on electroless Ni:P/Au, as-brazed sample

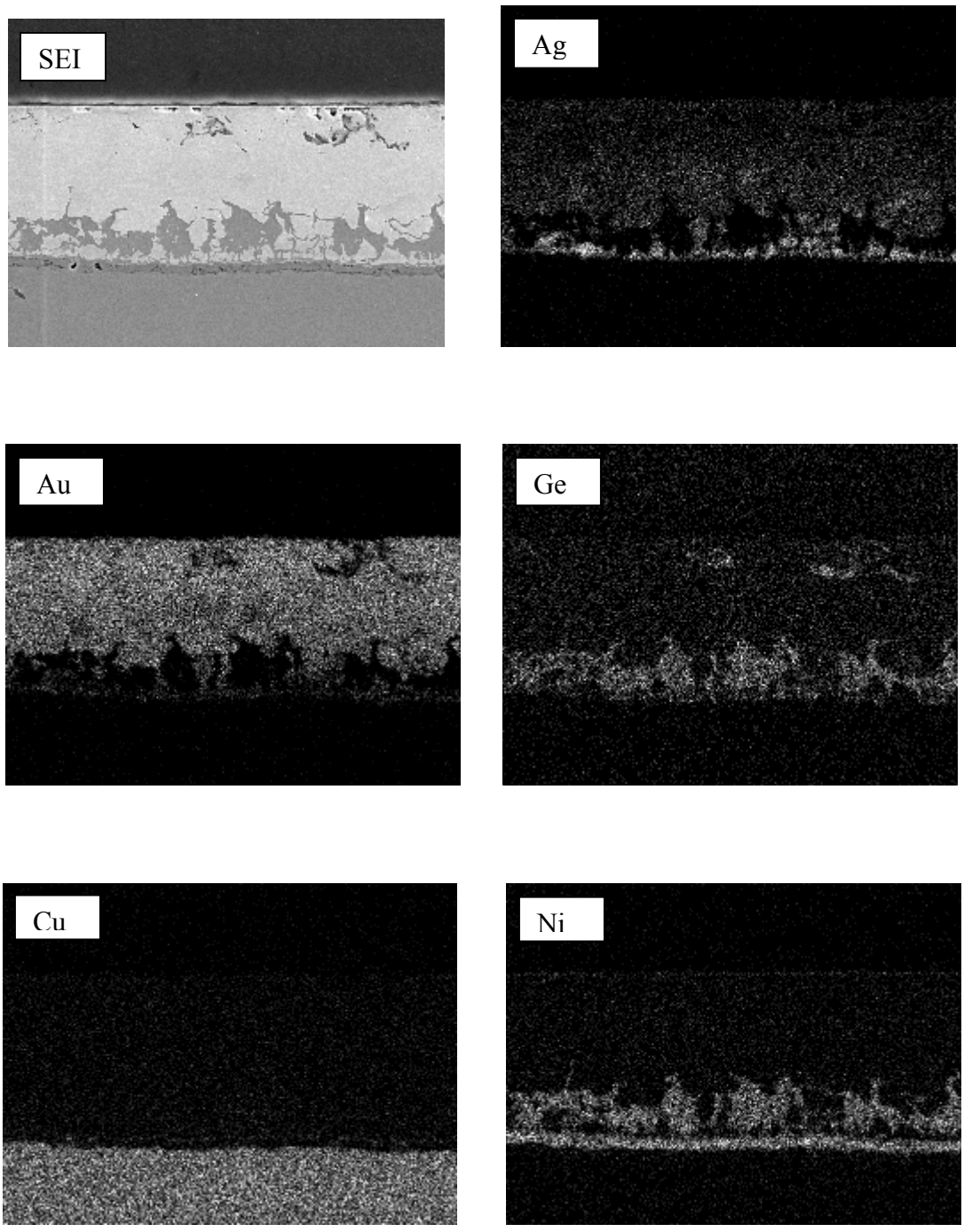


Figure 2-46 EDX elemental dot maps for Au-Ge-Ag on electroless Ni:P/Au, 100 hours storage at 400ºC

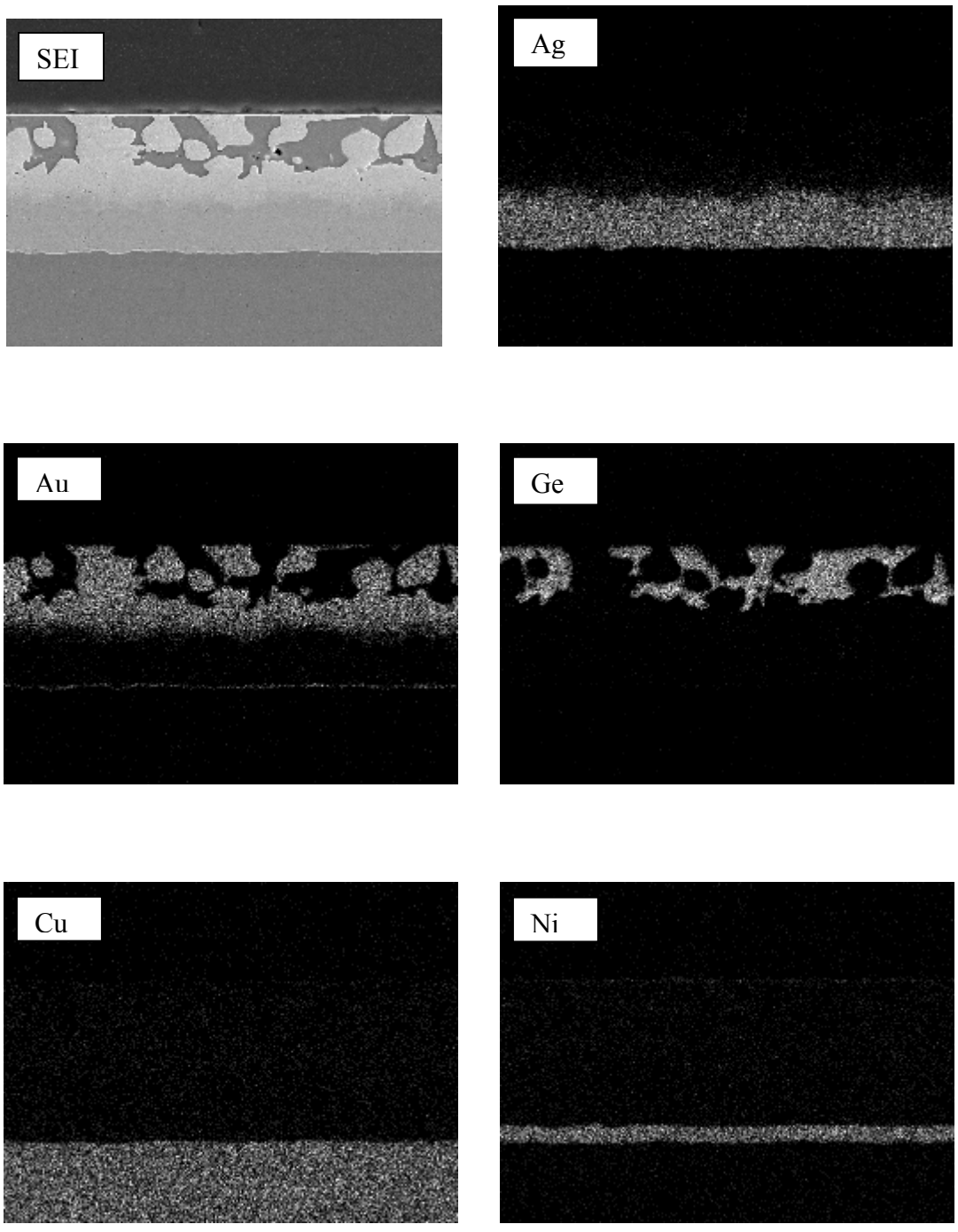


Figure 2-47 EDX elemental dot maps for Au-Ge-Ag on electrolytic Ni/Au, as-brazed sample

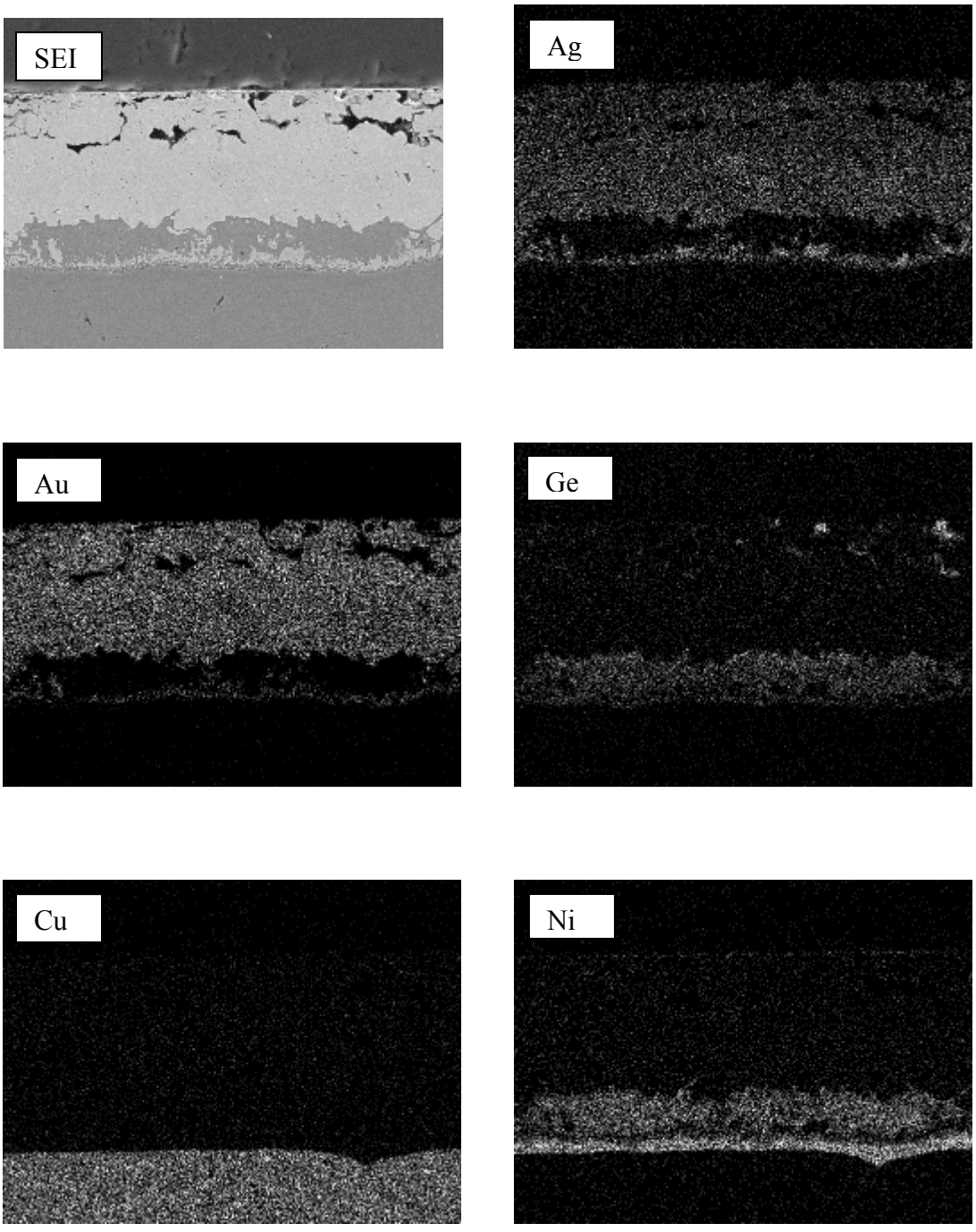


Figure 2-48 EDX elemental dot maps for Au-Ge-Ag on electrolytic Ni/Au, 100 hours storage at 400ºC

CHAPTER 3

Characterization of High Temperature Electrical Insulation Polymers

3.1 Introduction

The D.C. electrical strength of a polymer depends on the temperature. Nonpolar polymers exhibit no or a positive temperature dependence in the low temperature region and a negative dependence in the high temperature region. For polar polymers, a negative relationship has been observed in the low temperature region, with no apparent boundary between the low temperature and high temperature regions [64].

Polymers have been widely used as electrical insulation materials because of their excellent physical and chemical stability. The electrical properties of polymers under high electrical fields have received much attention, and many studies of electrical conduction and breakdown in polymers have been reported. However, the breakdown mechanism of polymers is not yet fully understood, and several breakdown theories have been proposed. At present, these can be summarized as follows [65]:

- Electronic breakdown theories
    - ❖ Intrinsic breakdown
    - ❖ Electron avalanche breakdown
- Thermal breakdown theories
    - ❖ Steady state thermal breakdown
    - ❖ Impulse thermal breakdown

- Electro-mechanical breakdown theories
- Secondary effect: Space charge, local heating and Maxwell stress, etc.

Low temperatures favor purely electrical breakdown. The intrinsic breakdown theory involves the introduction of a critical field strength above which substantial collision ionization begins within polymers. The collision ionization generates mobile electrons and relatively immobile holes, and the electrons and holes move in opposite directions under a field with different speeds, so the result is a distorted field that is stronger near the cathode and weaker near the anode. This distorted field in turn results in increased collision ionization, and this positive feedback process continues until a breakdown occurs.

The avalanche breakdown process is based on the assumption that above a critical field strength, a moving electron can produce another conduction electron by collision ionization, and the chain of collision continues until an avalanche occurs [65]. An avalanche usually presents a negative relationship between the electrical strength and the sample thickness and a positive temperature dependence [66]. Takai et al. [65] observed the electroluminescence of PPX thin film at -180°C and concluded that the electroluminescence was caused by the recombination of electrons and holes created by the hole collision ionization. Electroluminescence thus could provide direct evidence for avalanche breakdown when it takes place in the low temperature region. The theory of intrinsic breakdown yields values of the field strength at which collision ionization becomes an important process, and the theory of avalanche breakdown describes how the products of the collision ionization cause the build-up of breakdown current.

Thermal breakdown theory explains the breakdown process in terms of the Joule heat generated by the current flow and the conduction of this heat to the ambient. Thermal breakdown usually happens at high temperatures because the electrical conductivity increases and the thermal conductivity decreases with temperature [67]. The basic difference between thermal breakdown and electrical breakdown is that in the former the carrier multiplication is mainly due to the mutual feedback between the temperature rise caused by joule heating and the thermal excitation, while in the latter it is due to electronic processes other than thermal excitation. The electrical conduction at high fields is initiated by carrier injection from the injecting contact to the polymer by a tunneling process; the dominant carrier species responsible for electrical conduction depends on the type of carrier species injected from the injecting contact [68].

The electromechanical theory successfully explains the breakdown process of polymers in the high temperature region, where it postulates that the breakdown is caused by the mechanical deformation due to Maxwell stress under an applied electrical field. A decrease in the breakdown strength with Young's modulus around the glass transition point is a symptom of electromechanical breakdown [69] [70].

Space charge can be produced by collision ionization and/or by ionic migration. The effect of D.C. pre-stress on impulse breakdown is a typical example for the space charge [64]. Local heat generation was observed by Nagao et al. [71] with a thermograph method; their results showed that breakdown usually occurred in a localized hot point, which indicated that a thermal breakdown had taken place.

Recently, Muramoto and co-workers [72] [73] measured the space charge distribution and circuit current just before breakdown of a 125μm thickness polyimide

film at 90°C with the pulsed electro-acoustic method. Their results showed an insignificant change in the space charge distribution, and they conclude that the breakdown of polyimide film was not caused by space charge change. Instead, a thermal breakdown process due to the conduction current caused by a temperature rise in the sample was considered to be the most likely breakdown mechanism.

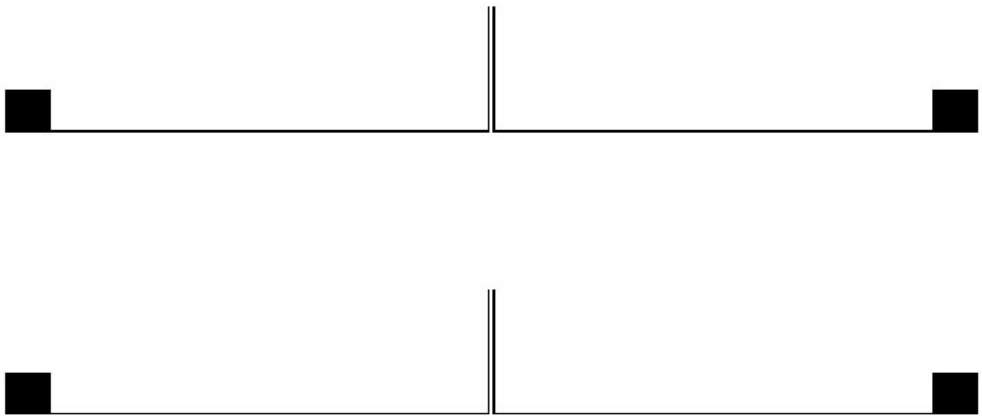
Hikita et. al. [74] measured the pre-breakdown current just prior to breakdown for several different kinds of polymeric materials. A sharp increase in the current on the order of 10^{-6}A at 10^{-5}s before breakdown was observed for polyimide samples at 150°C, and these experimental results indicated that a thermal activated conduction current resulted in the thermal breakdown for all tested samples.

3.2 Experimental Procedure and Results

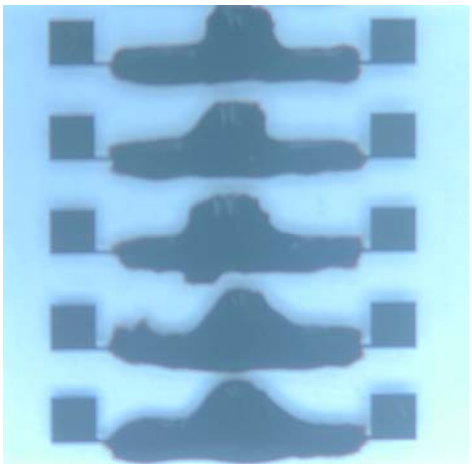
The test pattern was designed in the form of two 25μm wide, 3mm long parallel metal traces with a 100μm spacing; two 1mm x1mm probe pads were spaced 2cm apart. The patterns were fabricated on a quartz substrate; the metal trace was a sputtered Cr/Au (2000Å/1000Å) thin film. Figure 3-1 shows the test pattern. The polymer material was dispensed on the test pattern with a semi-automatic dispenser. The applied thickness was sufficient such that the breakdown path was between the two electrodes and not through the polymer to air. The material covered only the two parallel traces with the two probe pads left clear of material.

After the samples were fabricated, they were tested using a high temperature probe station, The temperature was set at 300°C with ±1°C accuracy controlled by the Signatone S-1045 system. The two contact pads were connected in series to a computer controlled SRS Model PS350 high voltage power supply (maximum voltage 5000V, ±1V

resolution; maximum current 5mA), a pico-ampere meter and a 1.6MΩ protection resistor. The circuit used is illustrated in Figure 3-2. The DC voltage was increased by 100V per step until breakdown occured. The breakdown voltage was measured from the power supply and the leakage current from the pico-ampere meter. During the test if the current exceeded the limit (5mA), the power supply automatically tripped (i.e. the voltage dropped to zero).



(a)



(b)

Figure 3-1 (a) Test pattern, (b) test pattern with cured PT material

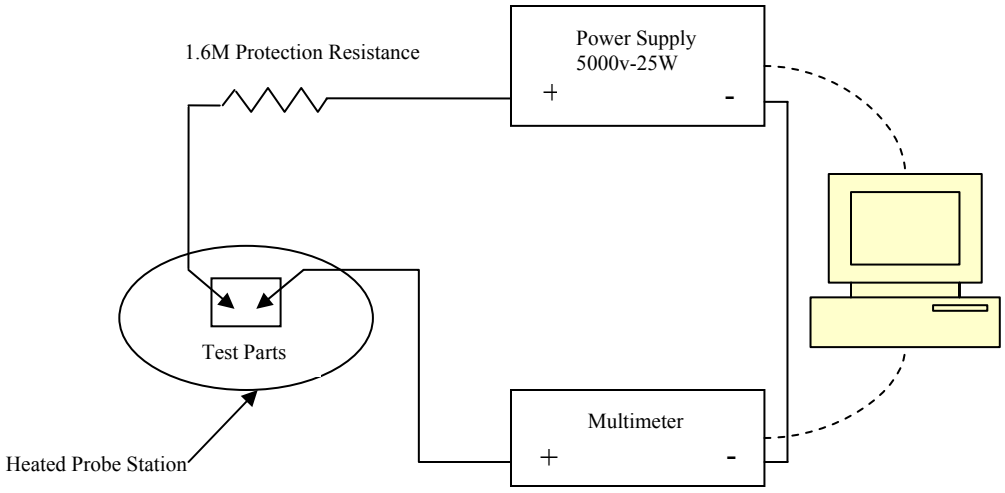


Figure 3-2 Breakdown voltage test setup

Three types of high temperature polymers were tested; phthalonitrile (PT), PM1215 and modified PI2611. Phthalonitrile is a high temperature polymer which has good thermal stability at temperatures up to 500ºC. Phthalonitrile was cured at 400ºC for 8 hours in nitrogen gas; the curing profile is shown in Figure 3-3 [49].

PM1215, which is a nanoreinforced polyhedral oligomeric silsesquioxanes (POSS) polyimide, was supplied by Hybrid Plastics, Inc. in two POSS concentrations of 10 wt% and 15 wt%. Upon exposure to oxygen, the POSS polyimide generates a nanoscopically thin glassy layer on the surface, providing a barrier to further oxidation and improves the surface for adhesion and bonding. PM 1215 has better flame retardancy, lower CTE and higher use temperature [75]. PM1215 was step cured at 100ºC for 2 hours, 200ºC for 2 hours and 300ºC for 1 hour in air.

PI-2611 is a high molecular weight, fully aromatic polyimide. It exhibits a desirable combination of film properties including low stress, low CTE, low moisture

uptake and high modulus, and is well suited for use as a dielectric layer for microelectronics applications. Some of its properties are presented in Table 3-1 [76]. PI2611 has previously been studied at Auburn University. In this experiment, the PI2611 was modified by adding POSS. Two variations of PI2611 were characterized, one with 5 wt% and the other with 10 wt% POSS additive. VM-652 is a solution of organosilane and was used to improve the adhesion of the PI2611 coatings to the assembly. For VM-652 application, a puddle of VM-652 was allowed to stand on the assembly for 20 seconds, and then it was spin dried at 3000 rpm for 30 seconds, followed by baking it at 120°C for one minute on a hot plate [76]. PI2611 was hand dispensed after applying VM-652 adhesion promoter, a soft-bake of PI2611 at 90°C and 150°C on a hot plate for 90 seconds each was performed. The final curing profile is shown in Figure 3-4. The profile ramped from 150ºC to 350ºC at a rate of 4ºC/min, and then held for 30 minutes at 350ºC [76]. The final cure was carried out in nitrogen.

Table 3-1 Properties of PI-2611 [76]

Property	PI-2611
Modulus (Gpa)	8.5
Moisture Uptake (%)	0.5
CTE (ppm/ºC)	3
Dielectric Constant (1kHz, 50%RH)	2.9
Dielectric Breakdown field (V/cm)	$>2x10^6$
Decomposition Temperature (ºC)	620
Stress (10μm film) (Mpa)	2

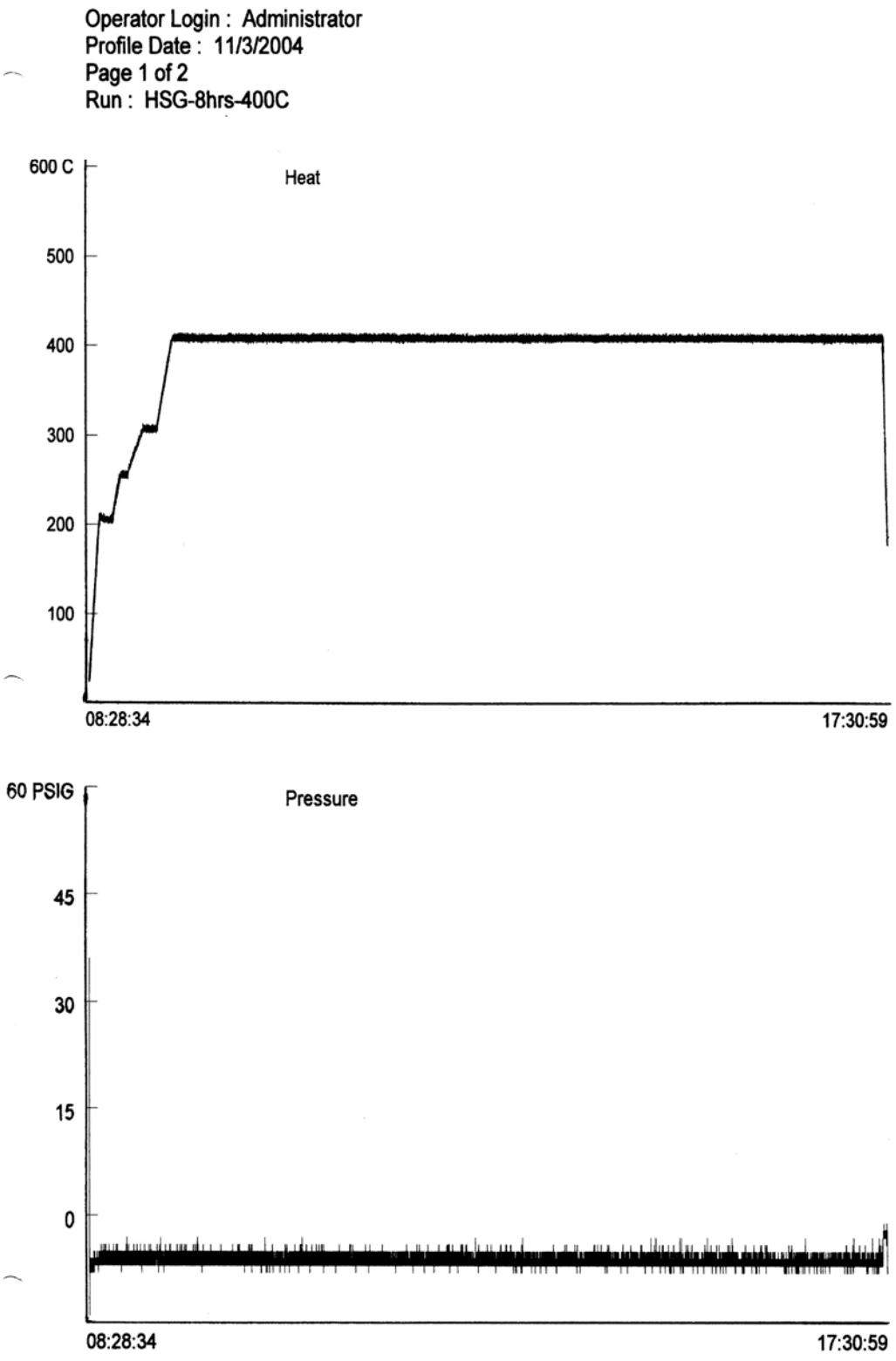


Figure 3-3 PT curing profile

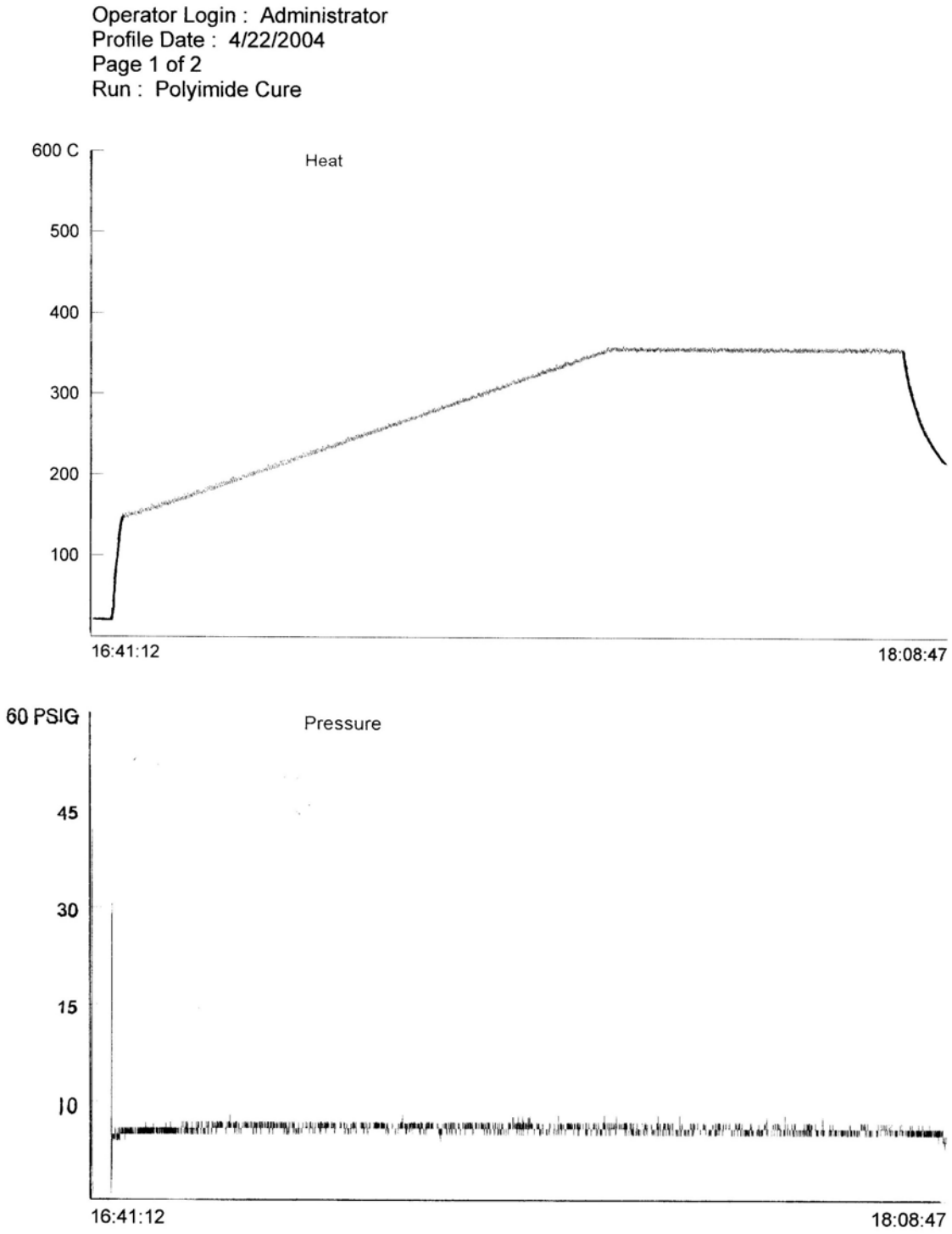


Figure 3-4 Curing profile of PI-2611 with POSS additive

The breakdown tests were performed at 300°C. The breakdown voltage data was collected as-made and after 100 hours, 250 hours, 500 hours, 1000 hours and 2000 hours of storage at 300°C, with a sample size of seven for each condition.

The initial leakage current was in the nA range when the applied electrical field was far below breakdown value and gradually increased with applied electrical field. Finally when breakdown occurred, there was a significant current increase to over 5mA, the equipment limit. Figure 3-5 illustrates the relationship of the leakage current vs. applied electrical field strength. Since the samples were tested at high temperature, the breakdown mechanism was attributed to thermal breakdown.

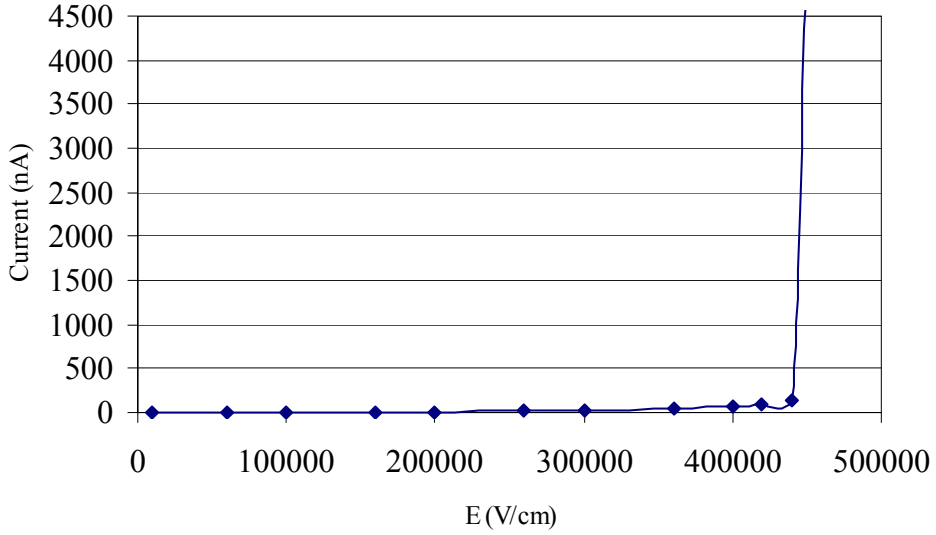


Figure 3-5 Leakage current vs. applied electrical field strength

Figure 3-6 presents the thermal aging data for the PT material. PT was observed to be very good initially and after 100 hours at 300ºC, the electrical breakdown field strength was over $5x10^5$ V/cm (the equipment limit). The PT material began to degrade

after 250 hours storage at 300ºC and eventually decomposed completely after 500 hours of thermal aging.

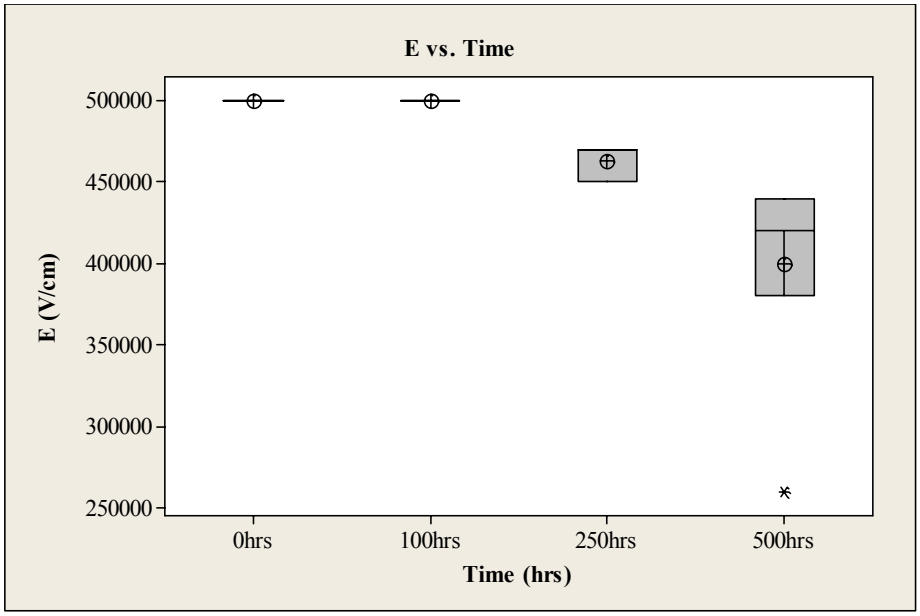


Figure 3-6 Electrical breakdown field strength for PT thermally aged at 300ºC

Electrical breakdown data for PM1215 is shown in Figure 3-7. The average breakdown field strength of the as-made samples was $4.3x10^5$ V/cm, which gradually decreased during aging to a minimum value of $2.6x10^5$ V/cm at 500 hours. After 2000 hours of storage at 300°C, the average breakdown field strength was $4.5x10^5$ V/cm. There was no significant difference between the 10% POSS and 15% POSS samples.

Figure 3-8 compares the electrical breakdown data for PI2611 mixed with 5% and 10% POSS. The average breakdown voltage dropped slightly after 100 hours storage, then increased and stabilized after 500 hours aging. The average breakdown field strength at 2000 hours is about $4.3x10^5$ V/cm. There was no significant difference between 5% and 10% POSS samples. When stored at 400C, the POSS-modified PI2611 coating disappeared after 250 hours.

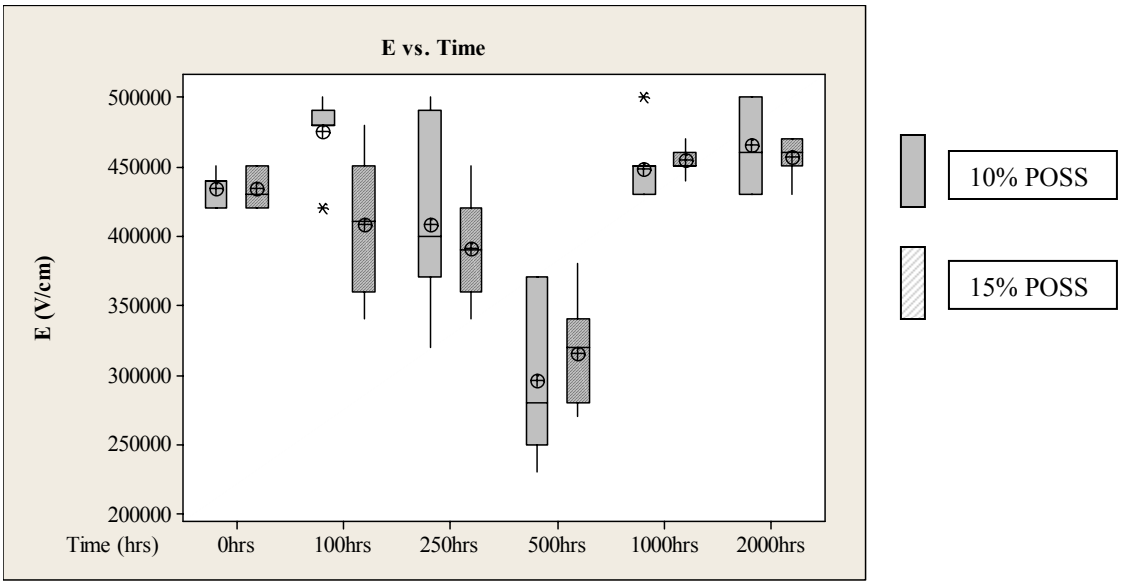


Figure 3-7 Electrical breakdown field strength for PM1215 thermally aged at 300ºC

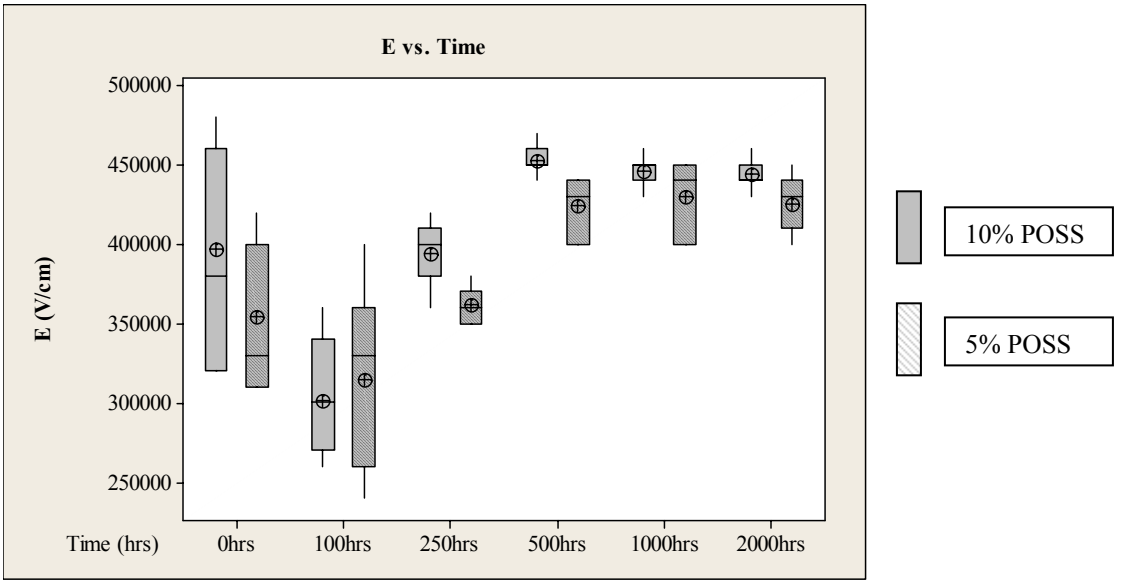


Figure 3-8 Electrical breakdown field strength for POSS-modified PI2611 thermally aged at 300ºC

CHAPTER 4

CHARACTERIZATION OF HIGH TEMPERATURE CAPACITORS

4.1 Introduction

Although active devices are the main elements used in high temperature electronics systems, passive components, including resistors, capacitors and inductors, are also required for systems capable of operating in extreme environments. Ceramic capacitors have various applications in electronic industries, being used for stored energy, blockage of direct current, coupling of circuit components, by- pass of an AC signal, frequency discrimination and transient voltage and arc suppression [77]. The term "ceramic chip capacitors" is used to describe a large group of capacitors which are made of polycrystalline dielectrics sintered at high temperature. Multilayer capacitors consist of many electrodes in a parallel arrangement, with very thin layers of dielectric material between opposing electrodes.The capacitance of a multilayer capacitor can be expressed as:

$$C = \frac{\varepsilon_o \cdot \varepsilon_r \cdot (N-1) \cdot A}{d} \qquad (4\text{-}1)$$

C : Capacitance, [F]

ε_o : Permittivity of vacuum, [8.85e^{-12} F/m]

ε_r : Relative permittivity

A : Effective electrode area, [m^2]

N : Number of electrodes

d : Electrode spacing, [m]

Capacitance is proportional to ε_r, A, and N and inversely proportional to d, so greater capacitance can be achieved by increasing the electrode area while decreasing the dielectric thickness, and also by using a multilayer structure.

The relative permittivity, ε_r, is proportional to the degree of material polarization that occurs under an applied electrical field. Polarization is the alignment of permanent or induced atomic or molecular dipole moments with an applied electric field. A dielectric material polarizes under an electric field, and the degree of polarization is related to the dielectric constant through the following equation:

$$p = \varepsilon_o \cdot (\varepsilon_r - 1) \cdot E \qquad (4\text{-}2)$$

p: Electric polarization, [F·V/m^2]

E: Electric field strength, [V/m]

The total polarization of a dielectric consists of four types of charge displacement: (a) electronic displacement, (b) ionic displacement, (c) orientation of permanent dipoles and (d) space charge displacement [77]. The polarization is dependent on the applied electric field strength and frequency. With increasing electric field frequency, the degree of polarization decreases because some polarization processes can not follow the changes in the applied field, and the dielectric constant is reduced. As a result, the capacitance decreases with increased frequency.

Dielectric materials can be divided into two categories: ferroelectric and non-ferroelectric. A ferroelectric dielectric shows a hysteresis relationship for the polarization versus applied electric field. The ferroelectric hysteresis loop changes shape with

temperature, until at a temperature near the Curie temperature of the dielectric, the hysteresis effect disappears and linearity is approximated. As a result, the dielectric constant is highly temperature dependent. The relationship of dielectric constant with temperature for $BaTiO_3$ is presented in Figure 4-1 [77]. Special additives can be used to shift or depress the high dielectric constant near the Curie point to achieve a relatively stable characteristic over a wide temperature range. Non-ferroelectric dielectrics follow a linear relationship of polarization to electric field. These materials exhibit lower dielectric constants, lower dissipation factors, and a negligible dependence of capacitance and dissipation factor on the frequency, voltage and temperature up to 200°C.

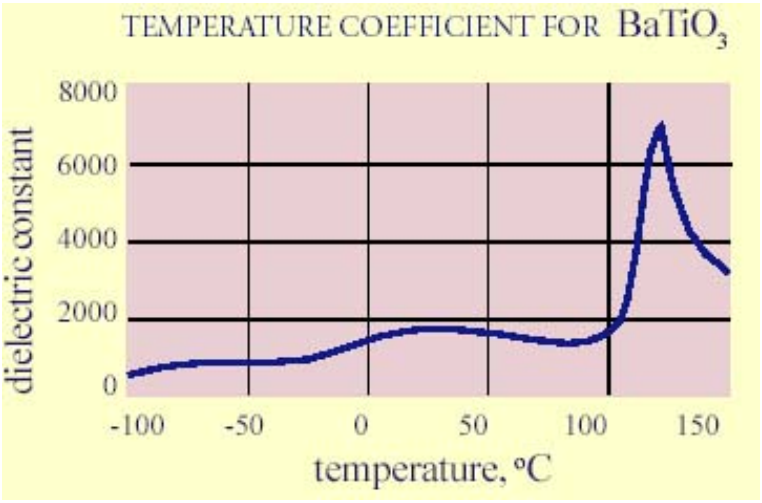
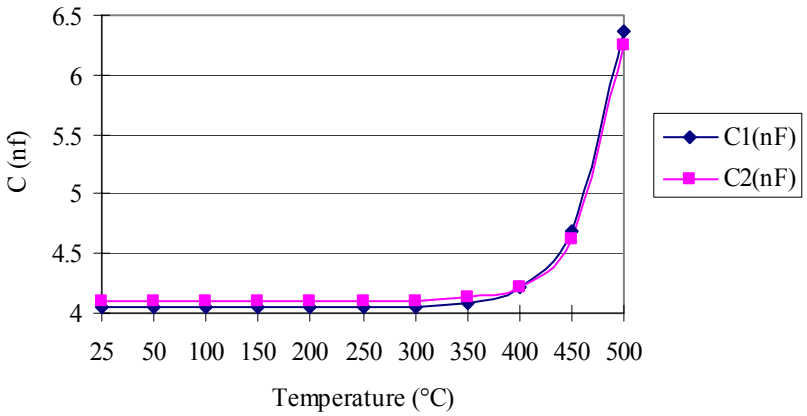


Figure 4-1 Dielectric vs. temperature for $BaTiO_3$ [77]

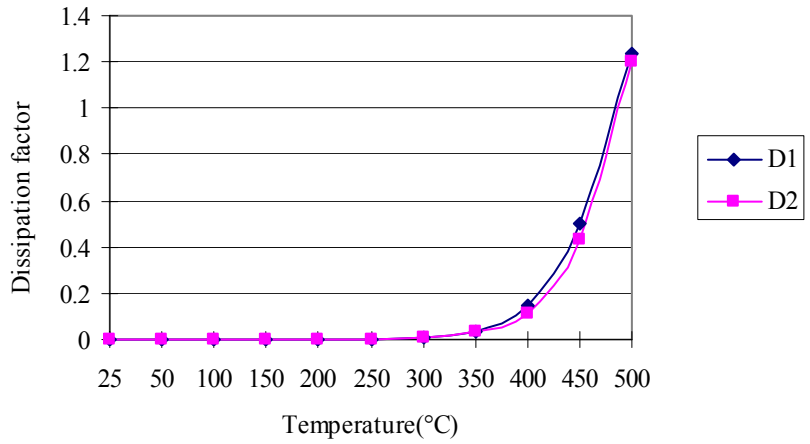
Depending on the composition of the dielectric, ceramic capacitors are classified into two groups:

Class I capacitors: Composed of non-ferroelectric dielectric with dielectric constants less than 200, these capacitors have a low loss at frequencies up to the UFH range, and the capacitance does not vary with voltage or frequency. They also have predictable linear capacitances with temperatures within the prescribed tolerance. Class I

capacitors are used in circuitry requiring stable capacitance properties, such as resonance circuits and filters [78]. Figure 4-2 shows a typical capacitance vs. temperature and dissipation factor vs. temperature curve for a class I capacitor for temperatures up to 500°C. Note that the dissipation factor and capacitance are relatively stable at temperatures below 300° C and change significantly above that.



(a)



(b)

Figure 4-2 (a) Capacitance vs. temperature and (b) dissipation factor vs. temperature curves for class I capacitor

Class II capacitors: Composed of ferroelectric dielectrics with dielectric constants ranging from 200 to 18000, these capacitors exhibit non-linear relationships of capacitance as a function of temperature, voltage and frequency. They have higher losses than class I and also higher capacitance values. Class II capacitors find applications in D.C. blocking, A.C. coupling and voltage suppression circuitry.

A practical capacitor can be viewed as an ideal capacitor in parallel with an ideal resistor. As a result, the current will not be 90° out of phase with the voltage in a real capacitor. The tangent of the angle by which the current is out of phase from ideal is defined as the dissipation factor or loss tangent. The dissipation factor is a material property and is independent of capacitor geometry. A material with a lower dielectric constant has a lower dissipation factor, and a high dielectric constant material has a higher dissipation factor. Class I dielectric materials show negligible variation in dissipation factor for temperatures up to 150°C, Generally, Class II dielectrics display a decrease in their dissipation factor with temperature. The energy loss is minimized above the Curie point because the ferroelectric domain no longer consumes energy. Both Class I and Class II dielectrics display an increase in dissipation factor with frequency.

Ceramic capacitors are supplied with either silver-palladium terminations or silver-nickel-tin terminations. Silver-palladium terminations have fair resistant to solder leaching and less tendency to tarnish than pure silver, while silver-nickel-tin terminations have excellent solderability and nickel is a good diffusion barrier, preventing leaching of the silver into the solder during assembly [78].

4.2 Experimental Procedure

The capacitance and dissipation factors were measured using an Agilent 4192A Impedance Analyzer. The 4192A employs a four terminal configuration, which has a significant measuring advantage for component parameter measurements requiring high accuracy in the high frequency region.

Generally speaking, any mutual inductance, interference with the measurement signals, and unwanted residual factors in the connection methods which are incidental to ordinary terminal methods significantly affect the measurement accuracy at high frequencies. The four terminal pair configuration offers an easy and effective method to solve this problem. The four terminal pair architecture consists of four connectors: high current (H_{cur}), high potential (H_{pot}), low potential (L_{pot}) and low current (L_{cur}). The purpose of the current terminals is to introduce a measurement signal current that flows through the sample, while the potential terminals measure the voltage drop across the sample. The high side signifies the drive potential drawn from the internal measurement signal source. To assemble a measurement circuit loop in a four terminal pair configuration, the H_{cur} and H_{pot} are connected to one termination of the capacitor and L_{pot} and L_{cur} are connected to the other. In addition, the shields of all the conductors must be connected together, as shown in Figure 4-3 [79].

The four terminal pair method combines the advantages of the four terminal method in low impedance measurements while providing the shielding required for high impedance measurements. Figure 4-4 illustrates the operational principle of the four terminal configuration [79]. The distinctive feature of the four terminal pair configuration is that the outer shield conductor works as the return path for the measurement signal

current. The same current flows through both the center conductors and the outer shield conductor, yet no external magnetic fields are generated around the conductors because the magnetic fields produced by the inner and outer currents completely cancel each other. Because the measurement signal current does not develop an inductive magnetic field, the test leads do not contribute additional measurement errors due to self or mutual-inductance between the individual leads. As a result, the four terminal pair method permits high accuracy measurements while minimizing any stray capacitance and residual inductance in the test leads or test fixtures. If the residual inductance is not avoided in the test leads, it will affect the measurements, and the resultant additional measurement error in capacitance increases in proportion to the square of the measurement frequency [79].

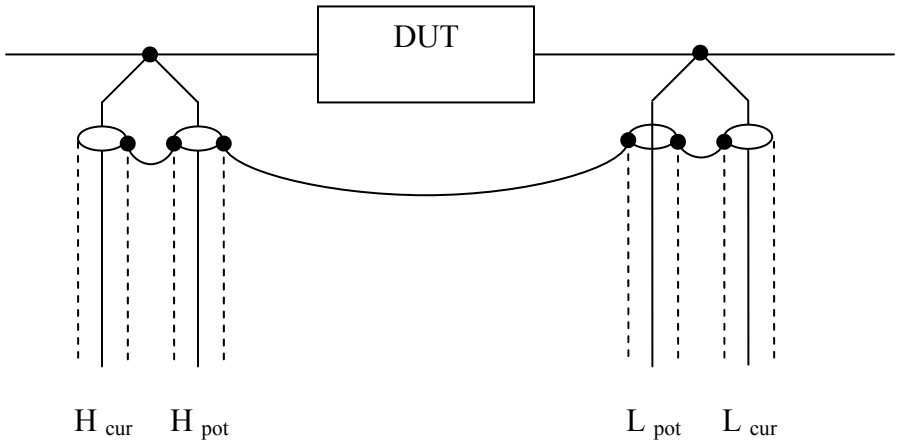


Figure 4-3 Four terminal pair connection [79]

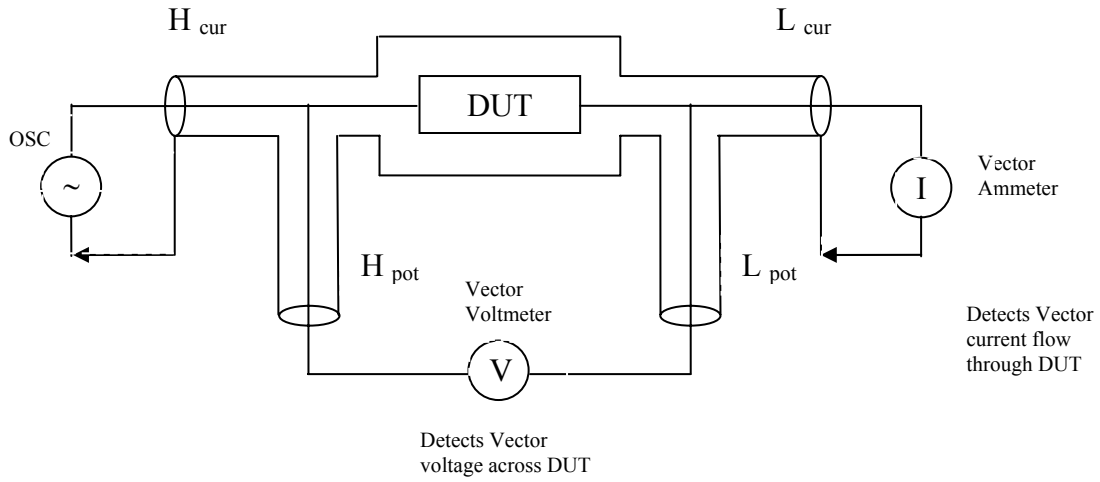


Figure 4-4 Four terminal pair measurement principle [79]

The experimental setup used to measure the capacitance and dissipation factor is shown in Figure 4-5. The capacitor was placed in a small ceramic cavity which was surrounded by a resistance heater. The temperature was controlled by a Watlow SD31 PID controller with ±1ºC accuracy and four 1 meter (electrical length) coax cables were connected to the four terminals on the 4192A, with the other ends connected to the capacitor terminations. To minimize the effects of parasitics on the measurements, zero short and zero open calibrations were performed at a specific frequency to ensure good measurement accuracy.

Figure 4-5 Experimental setup

The capacitors used in this experiment were obtained from Calramic Technologies LLC with a nominal value of 1μF, 100Vdc operation voltage and an operating frequency from 10 Hz to 200k Hz. The capacitors were fabricated with an X7R ceramic dielectric material (±15% maximum ΔºC from -55°C to 125°C, dissipation factor not exceeding 2.5% at 25°C) and the electrode band was printed with Pd-Ag. Figure 4-6 shows a typical capacitor. The capacitance and dissipation factor were measured at RT, 50°C, 100°C, 150°C, 200°C 250°C and 300°C. The test frequency was set at 10kHz, 30kHz, 50kHz, 100kHz and 200kHz. Twenty-five samples were tested for each set of conditions and the average value used for analysis. After measuring the initial data, the capacitors were thermally aged in a 300°C oven and retested at 100 hours, 250 hours, 500 hours, 1000 hours and 2000 hours.

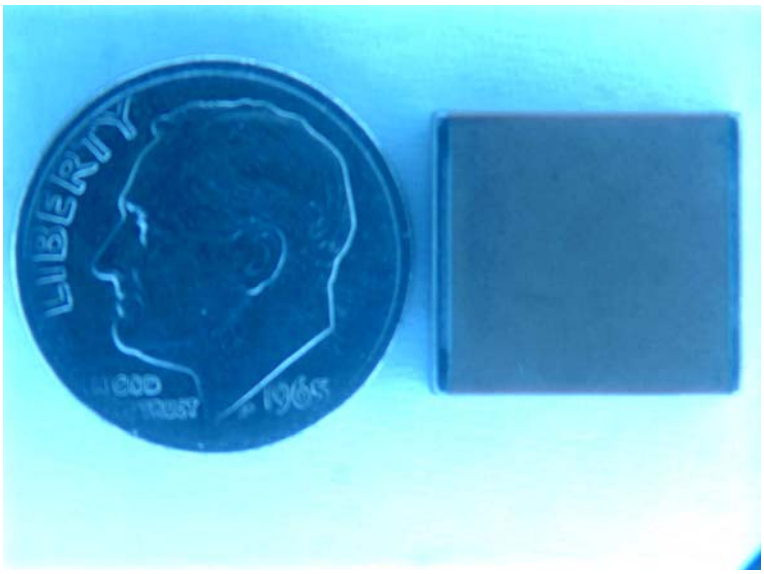


Figure 4-6 Ceramic capacitor

4.3 Results and Discussions

Figure 4-7 shows a plot of capacitance vs. temperature for each test frequency up to 300ºC, The initial values and those after 2000 hours of aging at 300ºC are compared. The profile presents similar tendencies, i.e., the capacitance initially has a gradual positive shift, reaching a maximum value near 130ºC, after which there is a sharp drop of capacitance with temperature. The reason for this change is that the dielectric constant varies with temperature, as explained earlier.

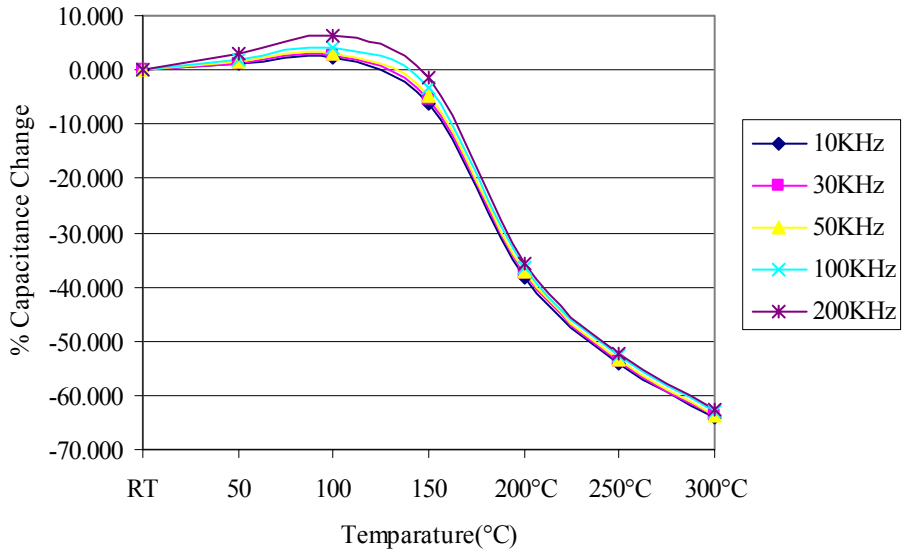
In Figure 4-8, the dissipation factor vs. temperature for each test frequency is shown. The dissipation factor generally decreases with temperature, tending towards a very low value, about 0.3% in most cases at 300ºC. This is because the energy loss consumed by the ferroelectric domains is minimized. The initial and 2000 hours data show similar tendencies.

Figure 4-9 shows the change of capacitance vs. storage time as function of frequency measured at 25°C and 300°C, respectively. Note that there appears to be an aging phenomenon that causes the capacitance to initially rise by approximately 2%~5% at room temperature (~14% at 300°C) and finally stabilize close to the new value in most cases.

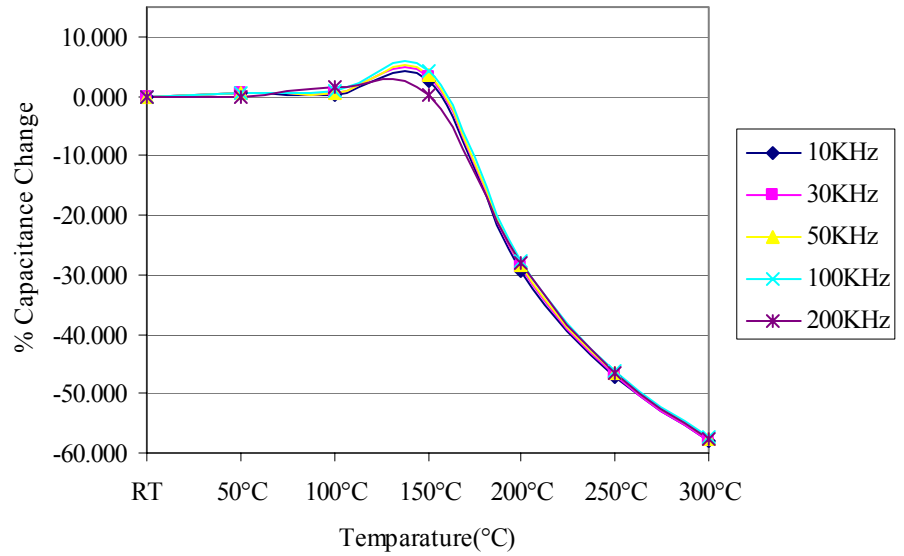
Figure 4-10 illustrates the variance of dissipation factor vs. aging time measured at 25°C and 300ºC, respectively. Again at each specific frequency there is a slight increase in dissipation factor up to 100 hours, followed by a gradual decrease that remains stable after 200 hours.

Figure 4-11 plots the dissipation factor vs. frequency at different temperatures, there is a gradual increase of dissipation factor with frequency, which is true for all tested temperatures.

Capacitance vs. frequency at each test temperatures is shown in Figure 4-12. Increasing the applied field frequency results in a decrease in the measured capacitance value in the low temperature range, this dependence is due to the net contribution of polarization to dielectric constant being reduced. At temperatures over the Curie point of the dielectric, the interaction of frequency and temperature makes the change in the capacitance complex, and there is no general trend visible in the results.

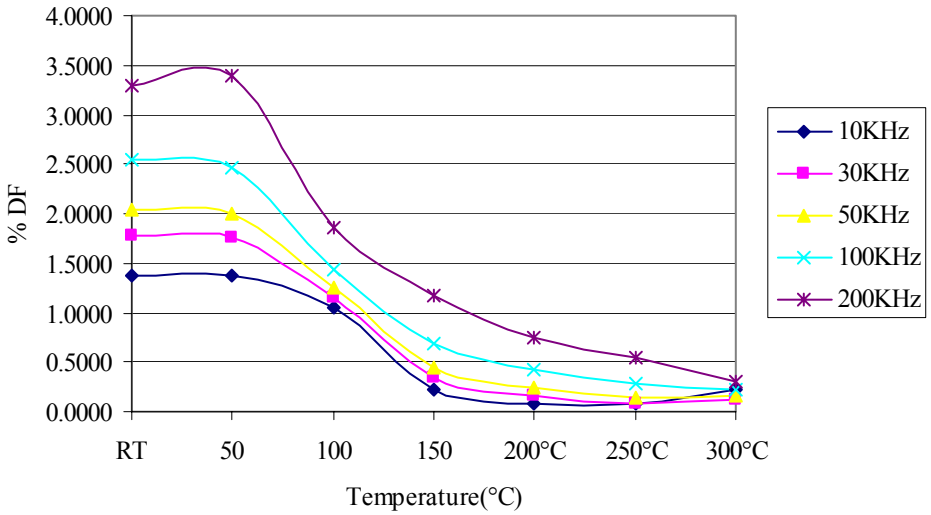


(a)

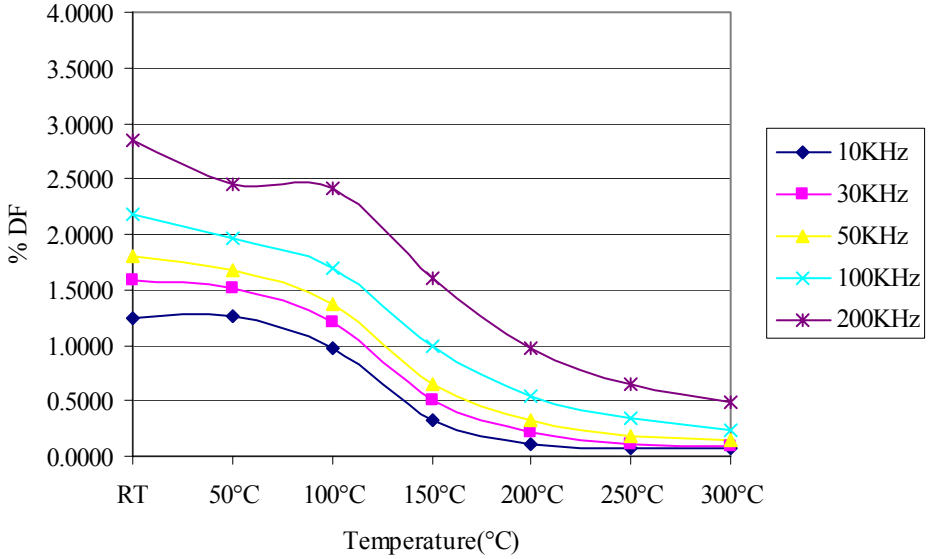


(b)

Figure 4-7 Capacitance vs. temperature for different frequencies, (a) initially and (b) after 2000 hours of aging

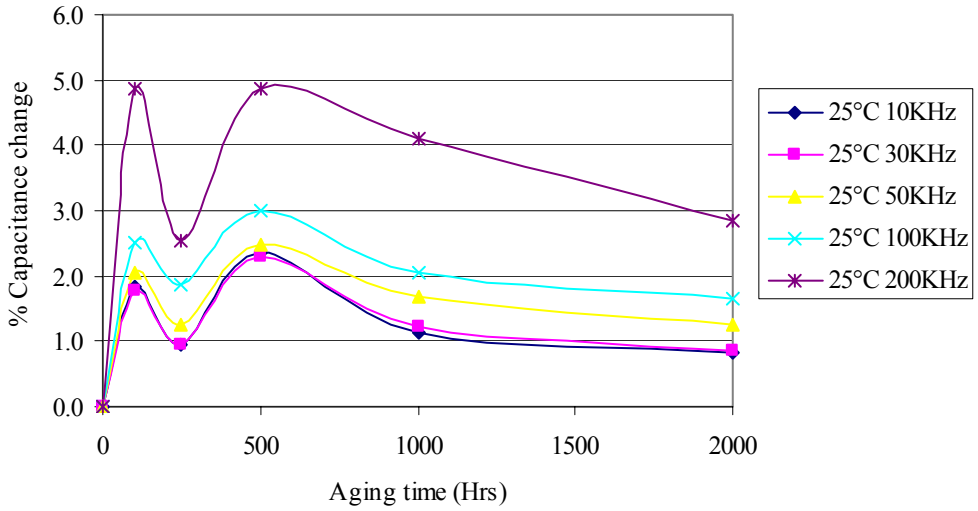


(a)

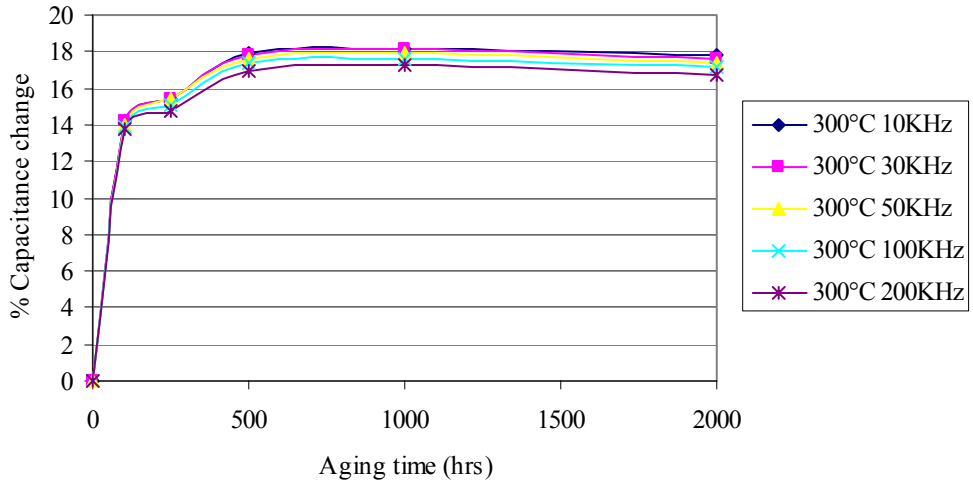


(b)

Figure 4-8 Dissipation factor vs. temperature for different frequencies, (a) initially and (b) after 2000 hours of aging

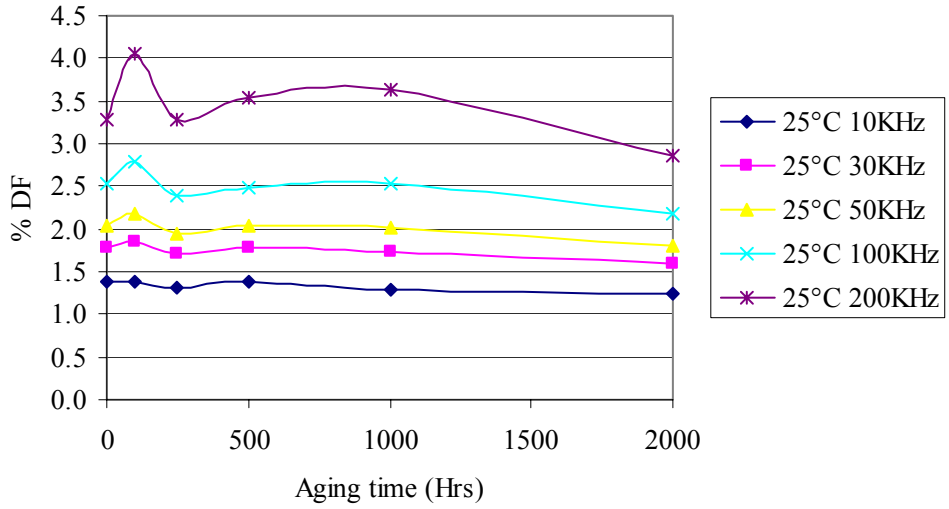


(a)

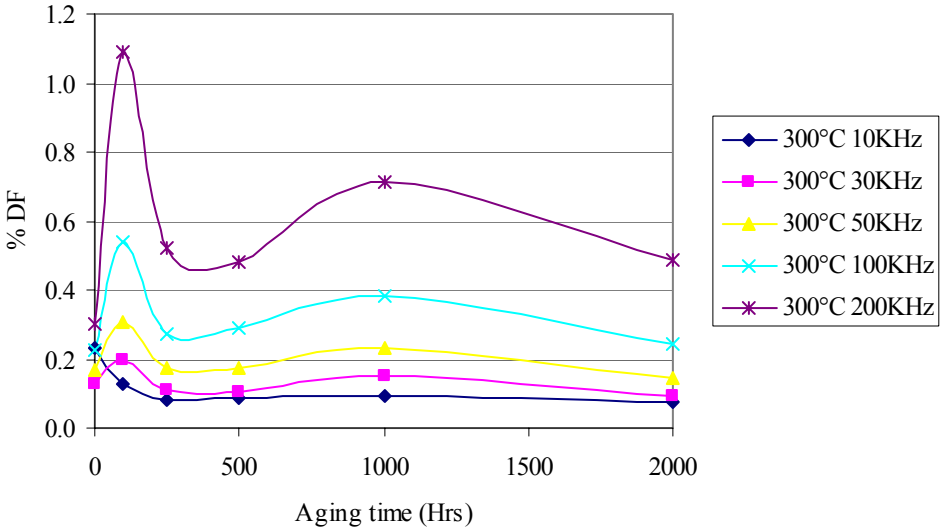


(b)

Figure 4-9 Capacitance vs. aging time, (a) at 25ºC and (b) at 300 ºC

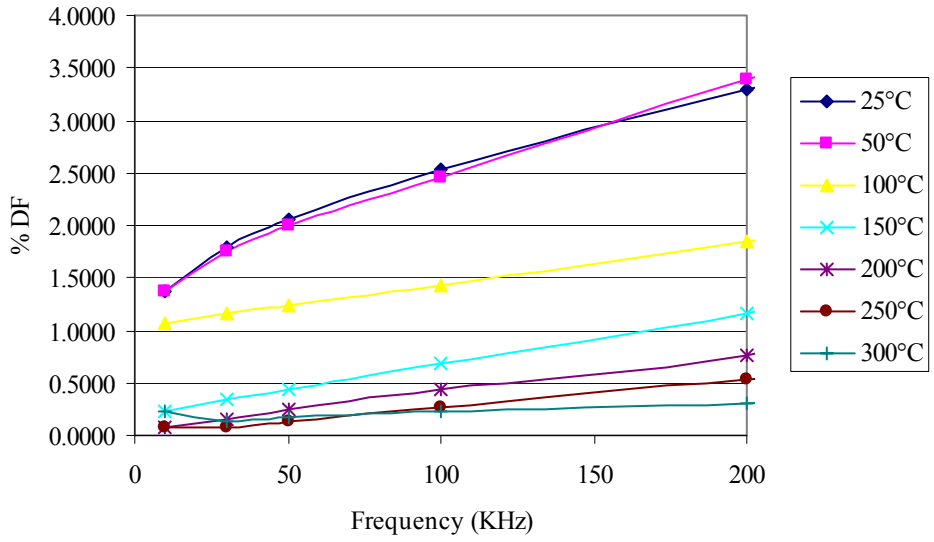


(a)

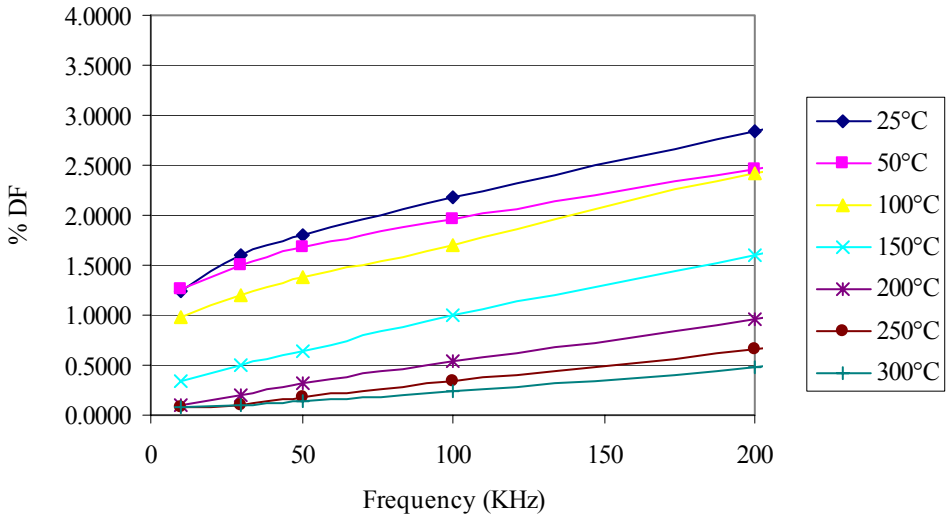


(b)

Figure 4-10 Dissipation factor vs. time for different frequencies, (a) at 25 ºC and (b) at 300ºC

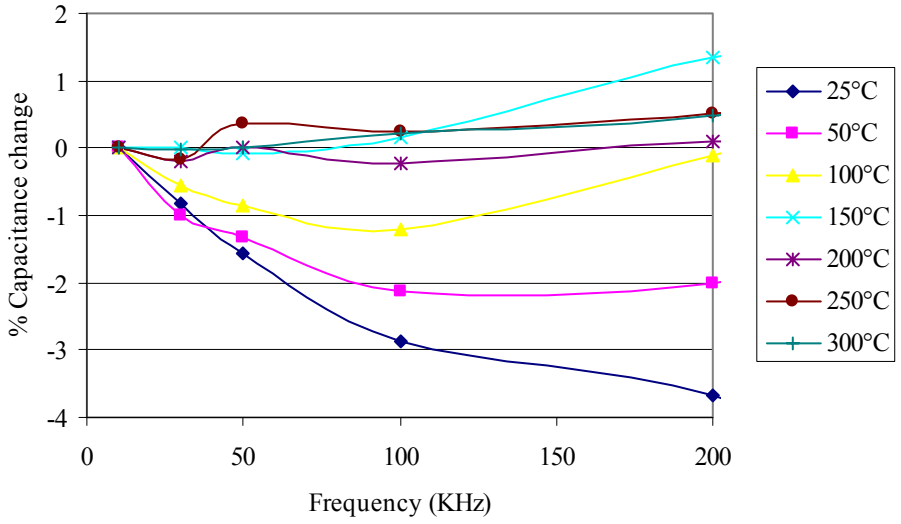


(a)

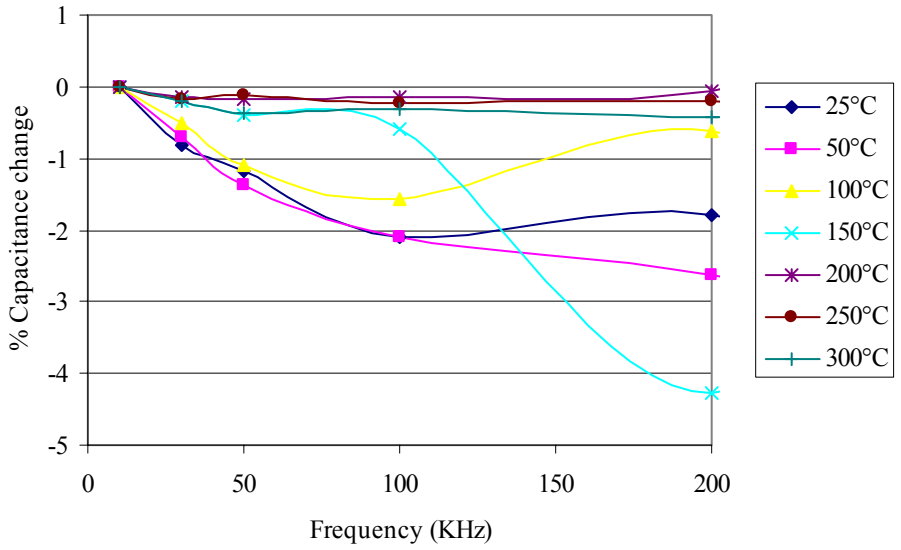


(b)

Figure 4-11 Dissipation factor vs. frequency at different temperatures, (a) initially and (b) after 2000 hours of aging



(a)



(b)

Figure 4-12 Capacitance vs. frequency at different temperatures, (a) initially and (b) after 2000 hours of aging

CHAPTER 5

CONCLUSIONS

5.1 Die Attach for SiC Packaging

In this study, a transient liquid phase bonding method using AuSn eutectic braze was successfully developed. Prior to this research, there was very little discussion of the Cu-Ni interdiffusion in the literature [60] [61] and no one has ever studied Cu-Ni:P interdiffusion, this is the first time in the electronics packaging industry that the thermal storage characteristics of Cu-Ni and Cu-Ni:P interdiffusion has been thoroughly studied at 400ºC. The die shear strength of samples fabricated with 6µm electrolytic Ni DBC Al_2O_3 substrates remained above 100kg-f after 2000 hours storage at 400ºC in air, while samples fabricated with 6µm electroless Ni:P DBC Al_2O_3 substrates degraded after 2000 hours storage at 400ºC in air. It was observed that voids developed at the Cu-Ni interface while cracks developed at the Cu-Ni:P interface after 2000 hours aging at 400ºC. The Kirkendall effect well explains why the voids and cracks occurred during thermal storage.

Original research on wide temperature range thermal cycling testing was also conducted. The thermal cycle test results showed braze-chip metallization delamination and cracks in the braze. The failure was caused by the CTE mismatches induced stress between the SiC die, the braze material and the substrate. Samples built with 1µm Ni DBC Al_2O_3 substrates showed early failure during thermal storage and thermal cycle test.

It is suggested that for the DBC Al_2O_3 substrates the minimum Ni thickness should be no less that 6μm.

AuGe eutectic braze was also evaluated as a high temperature die attach. Ge reacts with Ni, forming intermetallic compounds at high temperatures. Die shear values of samples built with electrolytic Ni DBC Al_2O_3 substrates degraded much more quickly than those built with electroless Ni:P DBC Al_2O_3 substrates.

Transient liquid phase bonding using AuGe eutectic braze and excess Ag from the substrate to lower the Ge concentration was also evaluated. The initial die shear strengths were >100 kg-f, but decreased significantly after only 50 hours storage at 400ºC. This was due to the Ge diffusing into the Ni, forming weak intermetallics. The results were similar for both electrolytic Ni and electroless Ni:P samples, with electrolytic Ni samples failing slightly faster.

5.2 Substrates for SiC Packaging

Ceramic substrates (Al_2O_3, Si_3N_4 and AlN) were used for SiC packaging. DBC Al_2O_3 substrates exhibited low thermal cycle reliability. The Al_2O_3 surface fractured after 250 thermal cycles, causing Cu foil delamination. Some AlN substrates with a thin film adhesion layer plus plated Cu metallization suffered severe blistering after only 100 thermal cycles which indicated a manufacturer process variation. Si_3N_4 substrates with active metal brazing Cu foil showed signs of copper foil delamination after 500 thermal cycles, the AES results showed the Si_3N_4 surface fractured during thermal cycling.

5.3 High Temperature, High Voltage Passivation

PM 1215, a nanoreinforced POSS polyimide, was evaluated for use in high temperature, high voltage passivation. The breakdown voltage results were promising at

300ºC, but higher temperature test results have shown rapid decomposition of the polyimide.

PI2611, modified by adding POSS nanofillers, showed no improvement in breakdown voltage at 300ºC and the POSS-modified coating decomposed after 250 hours storage at 400ºC. The initial results for Phthalonitriles were very promising, but the material degraded rapidly at 300ºC.

5.4 Ceramic Capacitors for High Temperature Applications

Ceramic capacitors were tested for high temperature applications. The dissipation factor and capacitance of Class I capacitors exhibited relatively small changes after 2000 hours aging at 300ºC.

5.5 Recommendations for Packaging SiC High Temperature, High Power Devices

Currently, the packaging options for SiC high temperature, high power devices are recommended as following:

- Die attach: AuSn transient liquid phase bonding for application temperatures up to 400ºC with limited thermal cycle requirements.
- Substrate: Active metal brazing Si_3N_4.
- Passivation: POSS-modified polyimide (PI2611) for application temperatures up to 300ºC.

5.6 Recommendations for Future Work

Although the AuSn braze has a superior high temperature storage performance, it does not have the desired thermal cycling reliability; other soft braze materials and processes have to be studied to fulfill both the high temperature and wide thermal cycle range requirements of today's applications. Additional work is also needed to improve

the thermal cycling performance of AMB Si_3N_4 substrates. In the meantime, alternate passivation materials need to be developed and tested for higher temperature and higher voltage applications.

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