An 8-bit 80-MS/s SAR ADC with Proposed S/H and Control Logic

by

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Abstract

In recent years, state-of-the-art Successive Approximation Register (SAR) ADCs have been operated at hundreds of MHz bandwidth or even GHz bandwidth by time interleaved for communication applications. This thesis proposes an 8-bit 80-Ms/s single-core SAR ADC implemented in 130nm CMOS.

The differential input signal is sampled by the bootstrapped switch with cross-couple paths and dummy switches for linearity improvement. A capacitive DAC with constant common mode, set-and-down principle, and shrunk MSB capacitor is implemented for increasing speed and reducing mismatch. A two-way alternate comparator structure is proposed for speed improvement which eliminates the reset time, mux logic chooses 2 of the 3 comparators for interleaving while the offset calibration is operated in the idle comparator. A modified DAC switching logic is proposed to decrease the delay of the D flip flop.

This design consumes 2mW from the 1.1V supply and occupies an area of 0.2952 mm^2.

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List of Abbreviations

ADC	Analog to Digital Converter
SAR	Successive Approximation Register
CMOS	Complementary Metal-Oxide-Semiconductor
SNDR	Signal to Noise and Distortion Ratio
DAC	Digital to Analog Converter
MSB	Most Significant Bit
S&H	Sample and Hold
LSB	Least Significant Bit
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
DNL	Differential Nonlinearity
INL	Integral Nonlinearity
SNR	Signal to Noise Ratio
SFDR	Spurious-Free Dynamic Range
ENOB	Effective Number of Bits
PMOS	P-type Metal-Oxide-Semiconductor
NMOS	N-type Metal-Oxide-Semiconductor
NAND	Negative-And
THD	Total Harmonic Distortion
FOM	Figures of Merit

Chapter 1: Introduction

1.1 Background and Motivation

In this fast-changing world, the evolution of the semiconductor industry has been remarkable. It plays an important role in economic growth around the world. Take the United States as an example: the semiconductor industry's contribution to the economy is more than 65 billion dollars, which makes it the third largest manufacturing industry in the United States [1].

In the real world, most data are represented as analog data, such as sound, temperature, and pressure. However, analog data is difficult to be measured and manipulated, while digital signal has the advantage of being easier to test, transmitting information with better noise immunity and providing better information security. So, analog to digital converters (ADCs) are used for converting analog signals to digital signals which could be manipulated by computers. There are a variety of ADC architectures, such as pipeline ADC, flash ADC, delta sigma ADC and successive approximation ADC. Pipeline ADC has higher bandwidth and speed but provides low resolution and more power. Flash ADC is the fastest converter but is very expensive and has large power consumption. Delta sigma ADC has high resolution and low power but is very slow. Successive approximation register (SAR) ADC has great tradeoff between speed and cost and is applicable to medium-to-high resolution, but the speed is limited to 2-5 mega samples per second. Among above ADC architectures, SAR ADC is more applicable for low power, medium resolution, and medium speed ADC [2]. With the rapid scaling of the CMOS devices, the performance of SAR ADC has been implemented to hundreds of MHz, which is used at wideband applications.

The SAR ADC presented in this thesis is implemented in 130nm CMOS with 56.8 SFDR and 42.8 dB SNDR. The Bootstrapped sample and hold with a cross-couple path and dummy switches is used to improve linearity. The DAC with the shrunk MSB, constant common mode, set-and-down principle reduces the DAC size and increase the setting speed. A two-way comparator structure is proposed for speed improvement which eliminates the reset time [3]. The structure is further changed to the procedure where two from the three comparators are chosen orderly to work while the idle comparator is doing the calibration at each sampling cycle. Additionally, a proposed DAC control logic is used to save time per bit. The ADC consumes 2mW at 1.1V power supply and only occupies an active area of 0.2952 mm^2.

1.2 Organization of the Thesis

This thesis is organized into five chapters. Chapter 2 presents an overview of basic principles of SAR ADC. Chapter 3 gives a detail discussion of proposed structure of S&H and control logic. Simulation Results and Measurements are presented in chapter 4. Chapter 5 draws the conclusion for the design.

Chapter 2: Basic Principles of SAR ADC

2.1 ADC Architecture

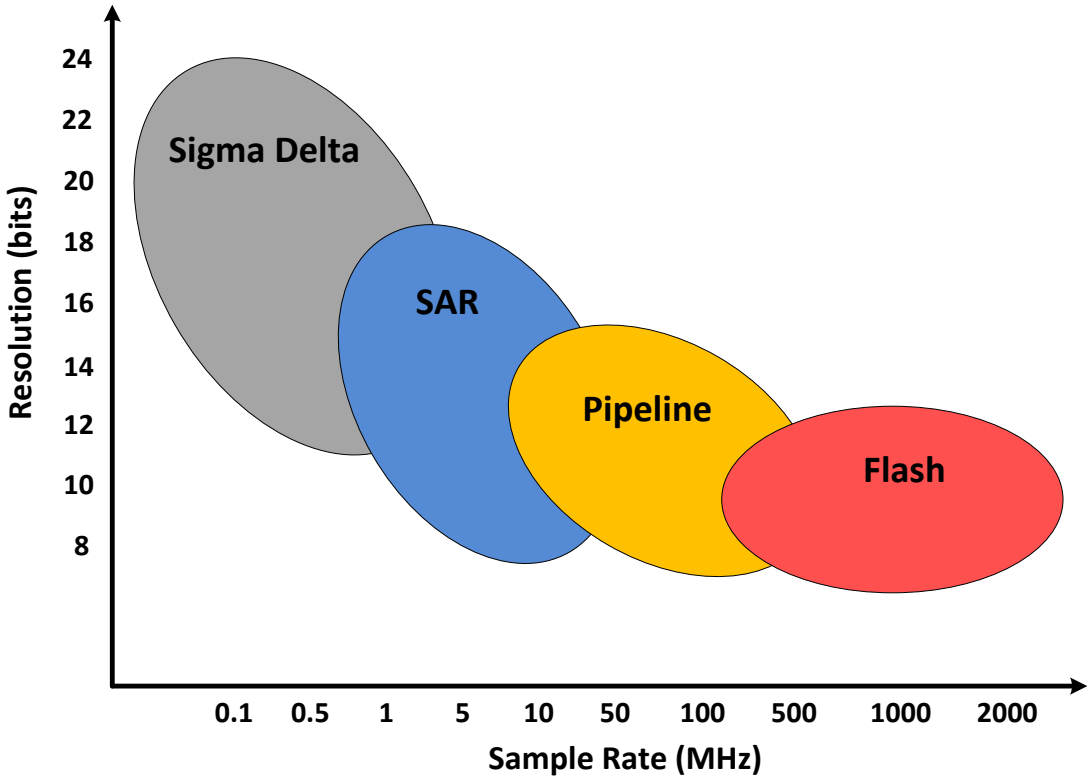

Fig. 2.1. ADC architecture vs resolution and sample rate.

Over the years, various ADC architectures have been developed to achieve the optimum sampling rate, resolutions, and power consumption as shown in figure 2.1. Those ADCs can be classified by sampling rate into Nyquist rate ADCs and oversampling ADCs. There are several Nyquist rate ADCs present in the data converter field such as flash ADC, pipeline ADC and SAR ADC. Delta sigma ADC is the most famous oversampling ADC. Also, those ADCs can be classified by applications into precision industrial measurement, data acquisition, and high speed. Delta sigma ADC is used in precision industrial measurement, and SAR ADC is the most popular ADC architecture for data acquisition application while flash ADC is for achieving the high speed.

Flash ADC is the fastest ADC architecture which is for large bandwidth application, but it has large power consumption and low resolution. Flash ADC is usually used in satellite communication, radar detection and electronic test equipment. Pipeline ADC is an important ADC architecture for sampling rate up to over 100 mega samples per second, and is usually used in ultrasonic medical imaging and base stations. Delta sigma ADC oversamples the desired signal and then filter the desired signal by digital filter, it achieves the high resolution and low power consumption which is used in precision industrial measurement and sensor monitoring. SAR ADC is becoming a great choice for medium to high resolution and 2-5 mega samples per second speed. It is usually used in data acquisition and industrial controls. Among above the ADC architectures discussion, SAR ADC is more applicable for medium speed, medium resolution, and low power consumption ADC.

2.2 SAR ADC Architecture

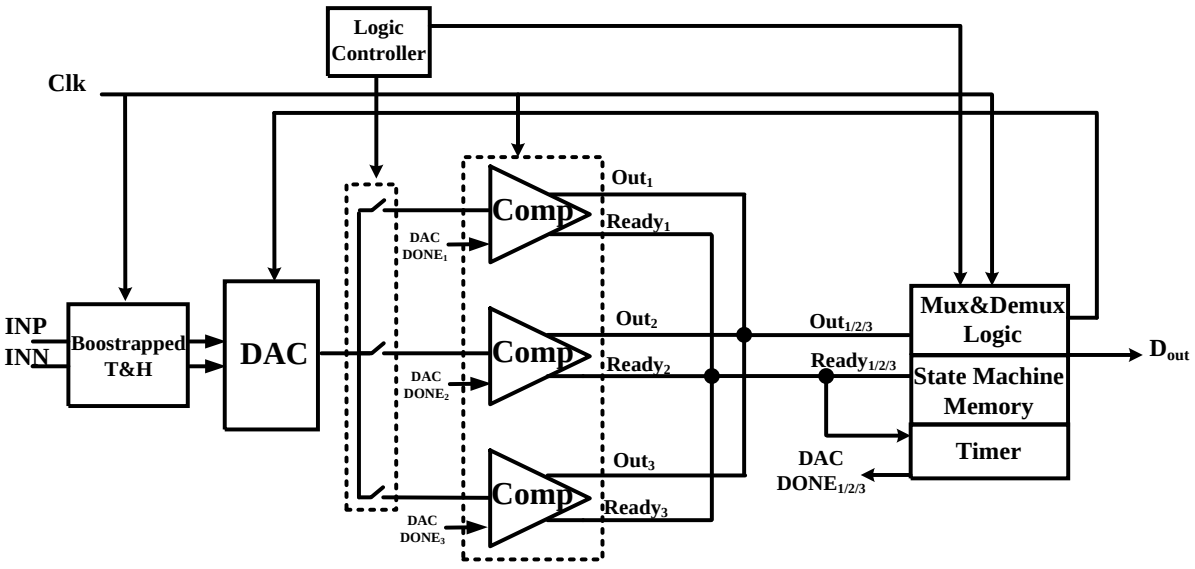

Fig. 2.2. SAR ADC architecture.

Figure 2.2 shows the architecture of the proposed SAR ADC. The differential input signal is sampled by the two bootstrapped switches with a cross-couple path and dummy switches for linearity improvement [4]. A capacitive DAC follows the T/H circuits and is implemented with set-and-down principle [5] and constant common mode technologies. The interleaved comparison is applied to eliminate the reset time of the comparator. To further introduce the calibration to comparators, 3 comparators instead of 2 are implemented to connect with the DAC. When the conversion process starts working, 2 of the 3 comparators (take comparator 1 and comparator 2 as an example) are chosen by the logic controller while comparator 3 is disconnected from the DAC and entering the calibration. In the next cycle, another set of 2 comparators are activated (take comparator 2 and comparator 3 as an example) while comparator 1 enters calibration mode, and so forth. Fully self-timed SAR control logic is applied in this design. When the comparator generates ready signals, which indicates a successful comparison is made. The SAR logic stores the value of the output into a temporary memory and the capacitive DAC redistributes correspondingly. A DAC timer also senses the ready signal and generate a DAC_DONE signal which indicates that the capacitive DAC has done settling. The delay between the ready signal and the DAC_DONE signal is designed to be equal to the digital logic delay by the structure of tracking DAC settling behavior [7].

2.3 Sample and Hold

2.3.1 Sample and Hold Architecture

Sample and hold circuit is the device to capture the voltage of varying given analog signal and store sampled value at the stable level as shown in Fig 2.3, which plays an important role in data converters. The sample clock is the control logic to determine whether to sample the input signal

or to hold the sampled value. When the sample clock is high, the given analog signal is sampled. When the sample clock is low, the given analog signal is stored for the specific amount of time.

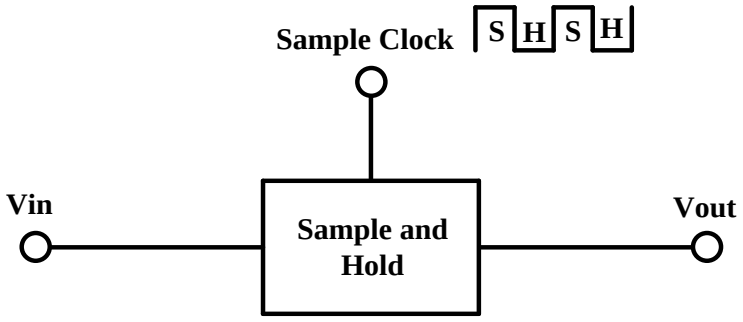

Fig. 2.3. Sample and hold architecture.

MOSFET is applied to be the switch as shown in Fig 2.4, and the sample clock controls the on and off function of MOSFET. The signal is sampled when the sample clock is high while the signal is held when the sample clock is low [7].

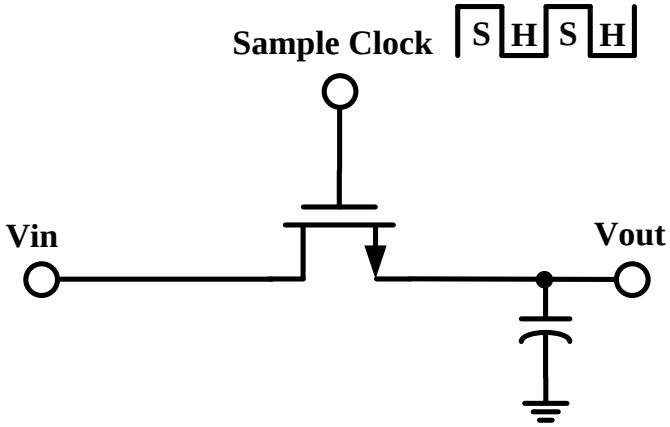

Fig. 2.4. Sample and hold architecture with NMOS switch.

2.3.2 Sample and Hold Parameters

There are many important parameters to determine the performance of sample and hold. First, acquisition time is the time for capacitor to charge back to the level as close as the input signal.

Second parameter is aperture time. Ideally the sample and hold is supposed to stop when the sample clock goes low. However, it still follows the input signal for a short length of time even after it gets the command from the sample clock because of the delay of switching. This delay time is called aperture time. Third, hold setting time is the amount of time that hold mode is settled with some error bands. Forth, voltage droop which describes the voltage of capacitor drop down because of the current leakage. Fifth, charge injection and clock feed through are important parameters caused by the parasitic capacitors between terminals. It will bring errors in the output.

2.3.3 Charge Injection

For charge injection, when MOSFET is on, the total charge in the inversion layer is

$$Q = WLC(V_{DD} - V_{in} - V_{TH}) \tag{2.1}$$

W is the width of the gate, L is the effective length of the gate, C is the capacitance of the oxide layer, V_{DD} is the supply voltage, V_{in} is the input voltage and V_{TH} is the threshold voltage of the device. When the MOSFET turns off, the charge injects into both the left and right sides as shown in figure 2.5. The charge which is going to the left side will not affect the performance because it is absorbed by input source, while the charge goes to the right side will bring the error because it stores in the sample and hold capacitors and changes the result.

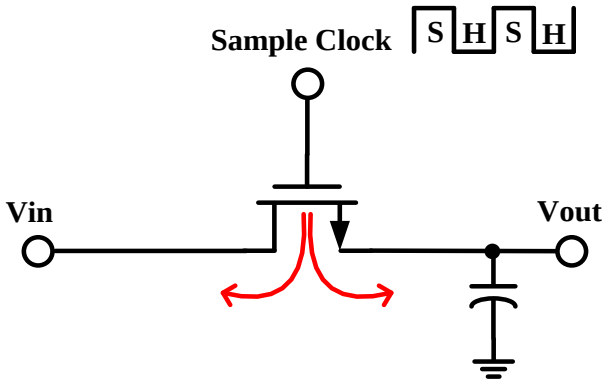

Fig. 2.5. Charge Injection.

Assuming 1/n of the charge is injected into the sample and hold capacitors C_{Hold}, the error will be

$$\Delta V = -\frac{WLC(V_{DD}-V_{in}-V_{TH})}{nC_{Hold}} \tag{2.2}$$

The output voltage will be

$$V_{out} = V_{in} - \frac{WLC(V_{DD}-V_{in}-V_{TH})}{nC_{Hold}} \tag{2.3}$$

As the worst case, we are assuming all the charge is injected into the sample and hold capacitors, the output voltage will be

$$V_{out} = V_{in} - \frac{WLC(V_{DD}-V_{in}-V_{TH})}{C_{Hold}} \tag{2.4}$$

From the analysis above, charge injection is a very important factor to hurt the precision of performance [8].

2.3.4 Clock Feedthrough

Clock feedthrough means the drain and source voltages are changed because of the change of clock signal on the gate through the gate to drain and gate to source overlap capacitances [9] as shown in figure 2.6. The error of clock feedthrough is

$$\Delta V = V_{clock}\frac{C_{overlap}}{C_{overlap}+C_{Hold}} \tag{2.5}$$

Where $C_{Overlap}$ is the overlap capacitance and C_{Hold} is the sample and hold capacitance, from the equation we know the clock feedthrough is very independent of the input signal.

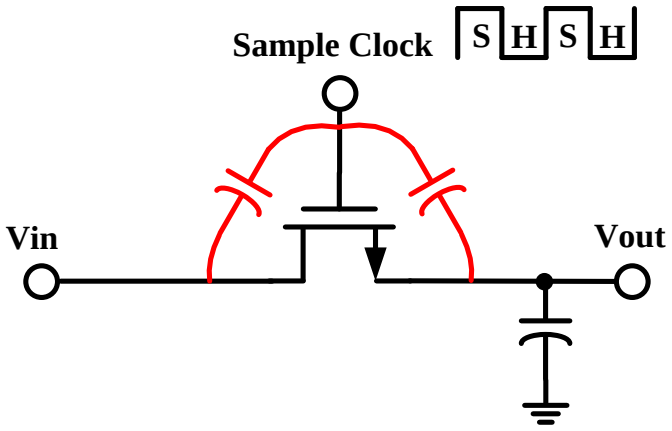

Fig. 2.6. Clock feedthrough.

2.3.5 Noise

KT/C noise is Johnson–Nyquist noise, which is present in electronic devices and generated by thermal agitation of electrons. When switch turns off, the noise will be stored in the capacitor. It brings the error which is approximately equal to $\sqrt{KT/C}$. Sample and hold capacitor should be large enough to get lower noise. Especially for SAR ADC, the total noise should be less than 1/2 LSB (Least significant bit) and $\sqrt{KT/C}$ is one of the noise in SAR ADC, so $\sqrt{KT/C}$ should be less than 1/2 LSB too. From the equation above, we will get the minimum size of DAC capacitor we are supposed to use.

2.4 Digital to Analog Converter

2.4.1 Digital to Analog Converter Theory

Digital to analog converter is a crucial component of SAR ADC because it determines the linearity of ADC, it convert the digital code from SAR logic to the analog value which is compared by comparator. The accuracy of the DAC depends on the accuracy of the reference input. Some ADCs use external references while others have the internal reference. Now plenty of SAR ADC use the

capacitive DAC with the charge redistribution principle to generate the analog output. Also, large amounts of power are consumed by switching capacitor arrays, so there are many new DAC architectures are proposed now.

2.4.2 Binary Weighted Capacitor Arrays

Binary weighted capacitor arrays are the most popular architecture. For the N bits binary weighted capacitor, it includes the scaled binary capacitors such as $2^{N-1}C$, $2^{N-2}C$, 2^{N-3}…2C, C, C. The last capacitor has the same value as LSB, so the total value of capacitor arrays is $2^{N}C$ [10].

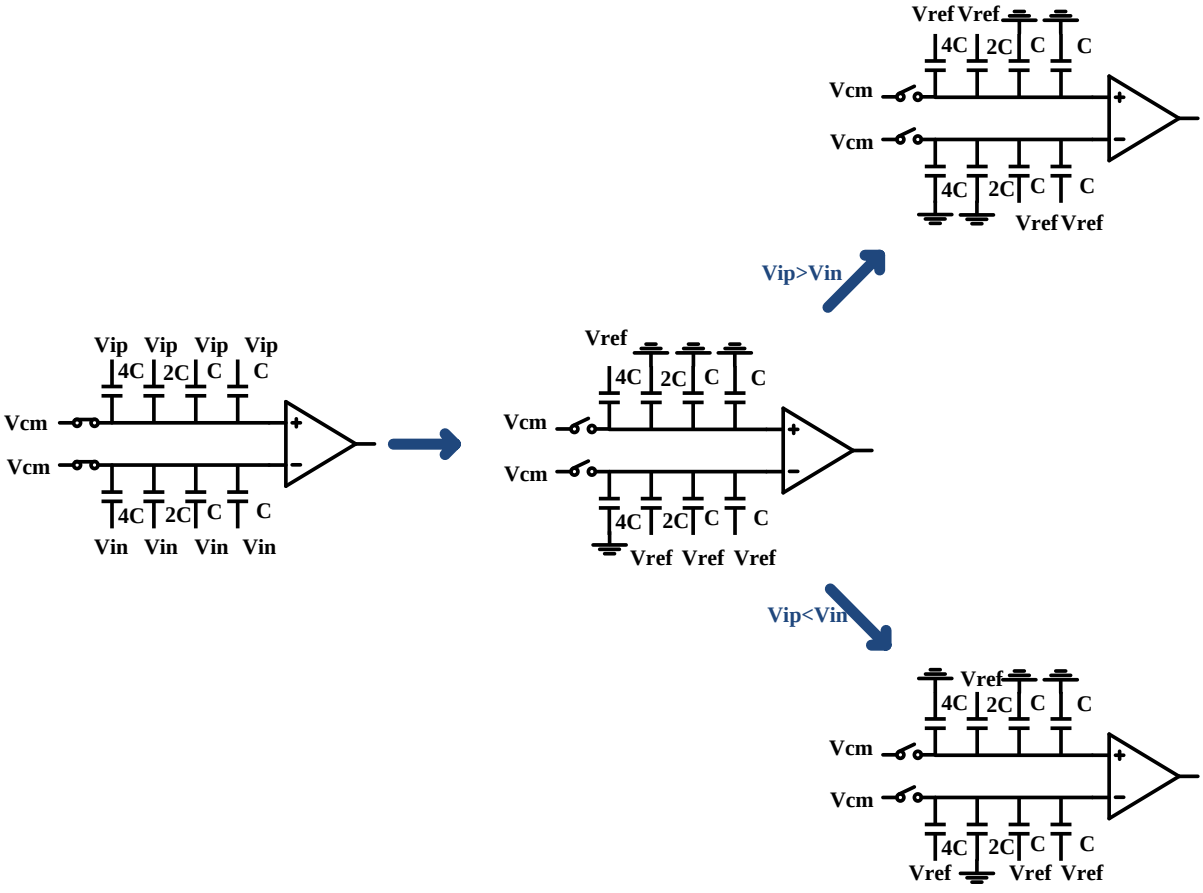

Fig. 2.7. Binary weighted capacitor arrays switching procedure.

Figure 2.7 shows the switching procedure of binary weighted capacitor arrays. Taking the positive side of capacitor arrays as an example, at the sample phase, the bottom plate of capacitors is connected to Vip while the top plate of capacitors is connected to common mode voltage. The total charge in capacitors is $8C(Vip - Vcm)$, after the sampling, the largest capacitor is switched to reference voltage $Vref$ while the rest of capacitors are switched to ground.

$$8C(Vip - Vcm) = 4C(Vref - Vcmp1 - Vcm) + 4C(0 - Vcmp1 - Vcm) \quad (2.6)$$

The value of Vcmp1 is

$$Vcmp1 = \frac{1}{2}Vref - Vip \quad (2.7)$$

Also, the value of Vcmn1 is

$$Vcmn1 = \frac{1}{2}Vref - Vin \quad (2.8)$$

Then comparator will compare Vcmp1 and Vcmn1, if Vcmp1 is greater than Vcmn1, then Vip is less than Vin, the second largest capacitor is switched to $Vref$ while the largest capacitor is switched to the ground in the positive side of capacitor arrays, and in the negative side of capacitor arrays the second largest capacitor is switched to the ground while the largest capacitor is switched to $Vref$. Comparator keeps comparing it again and repeat this procedure until the last bit LSB is resolved.

2.4.3 Set and Down Switching Method

Set and down switching method is to remove the largest capacitor so it helps to eliminate the half of total capacitors. After the sample phase, the comparator directly compares the Vip and Vin without any capacitor switching as shown in figure 2.8. Take the positive side of capacitor arrays as an example, the total charge in capacitors is $4C(Vip - Vref)$, If Vip is greater than Vin, the largest capacitor is switched to the ground

$$4C(Vip - Vref) = 2C(Vip1 - 0) + 2C(Vip1 - Vref) \tag{2.9}$$

So, the value of the $Vip1$ is

$$Vip1 = Vip - \frac{1}{2}Vref \tag{2.10}$$

The value of the Vin1 is still equal to Vin. Comparator keeps repeating this procedure until the last bit LSB is resolved. Set and down switching method reduces a large amount of power dissipation. The main drawback of using set and down method is the common mode voltage gradually drops through the switching of every bits. After the second switching, the common mode constant voltage is $Vip + Vin - \frac{1}{2}Vref$, which is smaller than the common mode constant voltage before switching $Vip + Vin$.

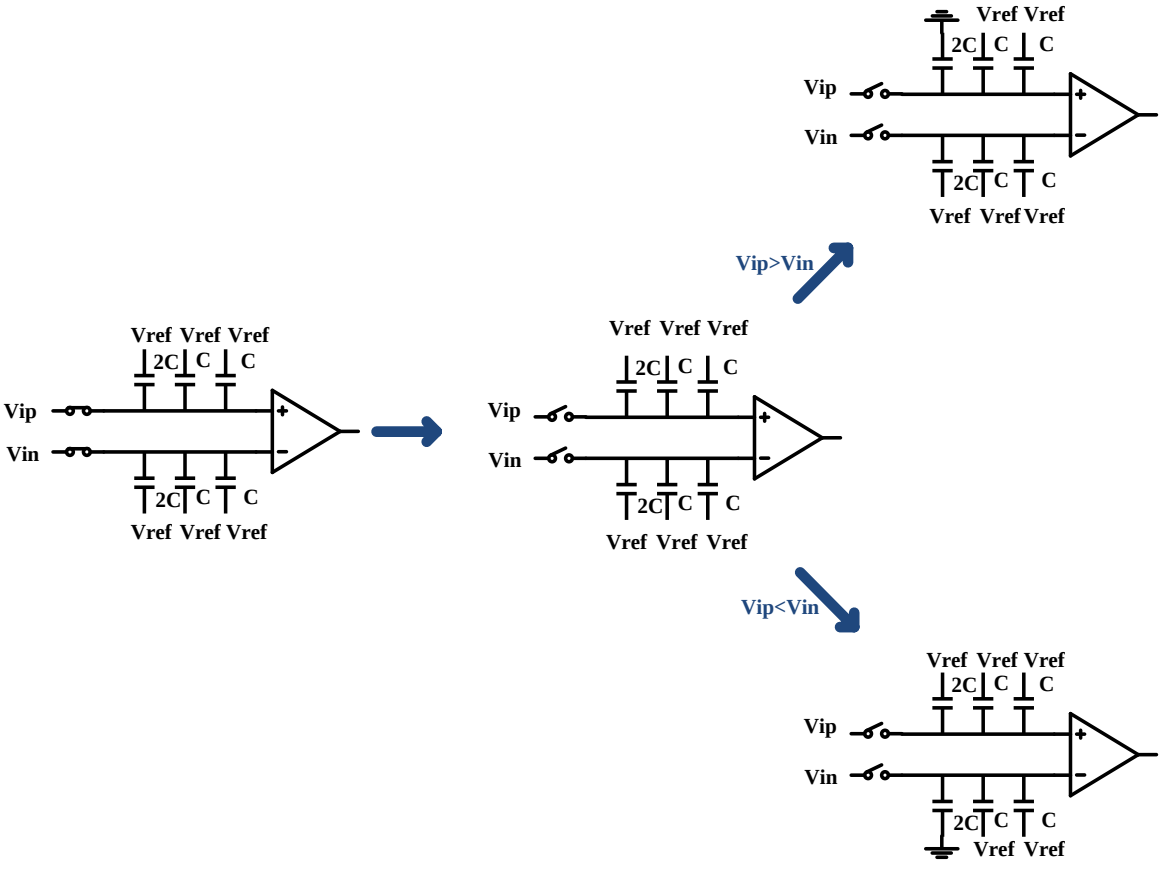

Fig. 2.8. Set and down switching procedure.

2.4.4 Double capacitor array Method

As we discussed above, the advantage of the set-and-down principle is eliminating the largest capacitors and improving the speed, but resulting in the lower common mode after every bit. Since the precision, stability and speed of the comparator is highly depending on the common mode voltage, so the capacitor array is doubled. The capacitors are switched to the opposite direction in both two set of capacitor arrays as shown in figure 2.9

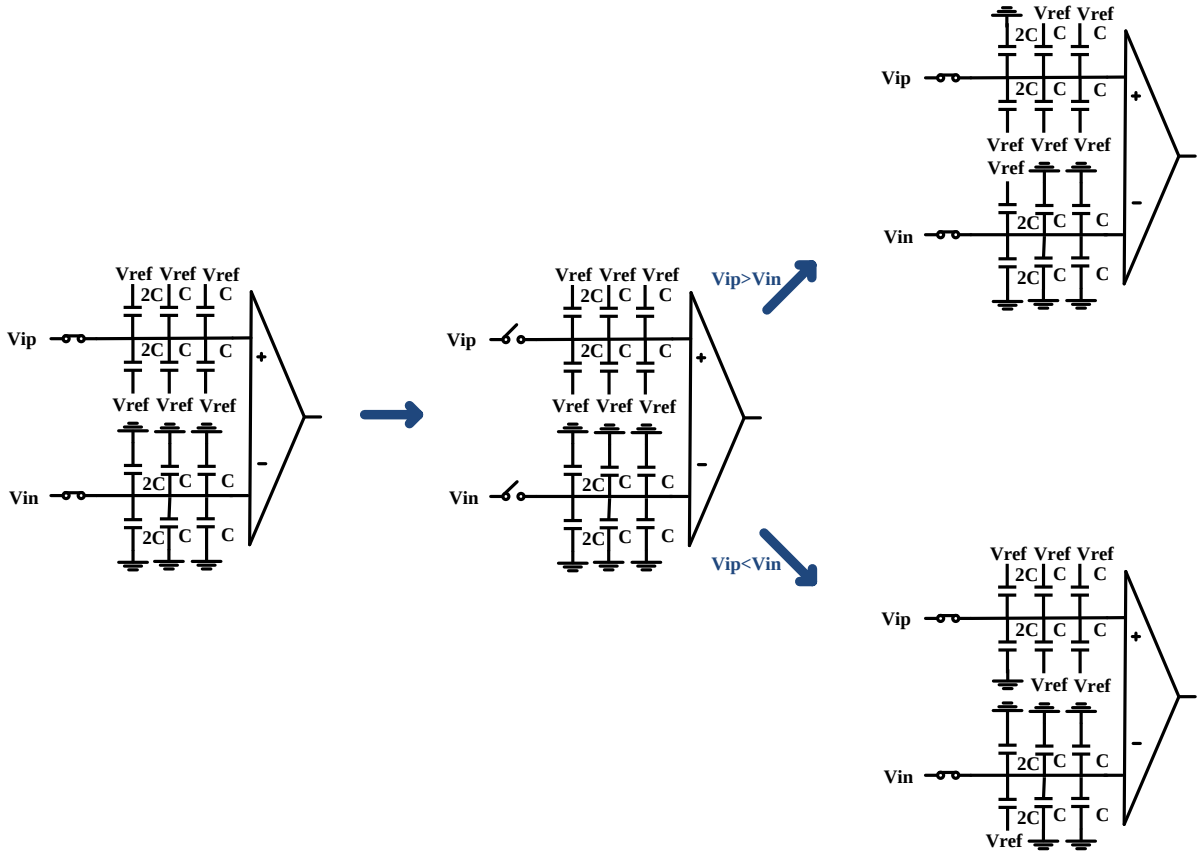

Fig. 2.9. Double capacitor array switching procedure

Take the second switching as an example, the total charge in positive capacitor array is $8C(Vip - Vref)$, If Vip is greater than Vin, one of the largest capacitor is switched to the ground

$$8C(Vip - Vref) = 2C(Vip1 - 0) + 6C(Vip1 - Vref) \quad (2.11)$$

The value of Vip1 is

$$Vip1 = Vip - \frac{1}{4}Vref \quad (2.12)$$

At the same time, the total charge in negative capacitor array is $8CVin$, if Vip is greater than Vin, one of the largest capacitor is switched to the $Vref$

$$8CVin = 2C(Vin1 - Vref) + 6CVin1 \quad (2.13)$$

The value of Vin1 is

$$Vin1 = Vin + \frac{1}{4}Vref \quad (2.14)$$

So, the comparator result is

$$Vip1 - Vin1 = Vip - Vin - \frac{1}{2}Vref \quad (2.15)$$

And the common mode voltage will be

$$Vip1 + Vin1 = Vip + Vin \quad (2.16)$$

As the result, the differential output is changed while the common mode voltage remains constant.

2.5 Comparator

2.5.1 Comparator Theory

Comparator is an important block of the SAR ADC, it compares two different analog signals and generates digital binary 0 or 1 outputs. SAR logic could use them to switch DAC and generate ADC outputs.

High gain amplifier is eligible to be used as the comparator, and its output swing must be high enough to drive the SAR logic. Also, latched comparator is more popular to be used now, it has

two different architectures, one is the latch only comparator, one is the combination of the preamplifier and the latch.

2.5.2 Static Characterization

The static characterization of comparator includes input offset voltage, kickback noise, gain and input resolution. Static input offset is caused by the mismatch of input devices which is inevitable, it might make comparator generate the wrong output. One way to reduce the input offset is to use preamplifier in the comparator architecture. The kickback noise is the voltage disturbance in the internal nodes of comparators. The exiting technology to reduce the kickback noise has adding preamplifier before comparator or inserting MOSFET transistor to the input nodes and opened during the regeneration phase. The input resolution is the smallest input voltage difference which can be caught by the comparator. At least comparator should be able to measure the LSB of ADC.

2.5.3 Dynamic Characterization

The dynamic characterization of comparator includes propagation delay, slew rate and speed. Propagation delay directly decide the speed of the comparator, it is the delay time between input and output signal.

2.6 SAR logic

2.6.1 SAR logic Theory

The function of the SAR logic is to decide the 0 or 1 of each bit based on the output of comparators, and generate control signals for DAC capacitance arrays. There are different logic types. Delay lines can be used as logic to generate clock and then output values are stored in D flip flops. Ring

counter and D flip flops are a good combination to be logic too. Also, D flip flops and combinational digital logic gates are used as well.

2.6.2 Delay Line

Delay line is the circuit to delay the input signal with specific increment time. It is usually adjustable and composed of series inductors, capacitors or even inverters. Take RC delay line as an example, the value and number of RC elements determine the length of delay, but delay line is very vulnerable of noise and easy to have jitters in generated clock.

Inverter delay line is composed of series inverters in a row as shown in figure 2.10. N inverters are needed if we need N generated clock. The length of delay is determined by the value of single inverter, the difference value between connected inverters and supply voltage. The disadvantage of the inverter delay line is imprecise because of the process, temperature and noise of supply voltage and ground.

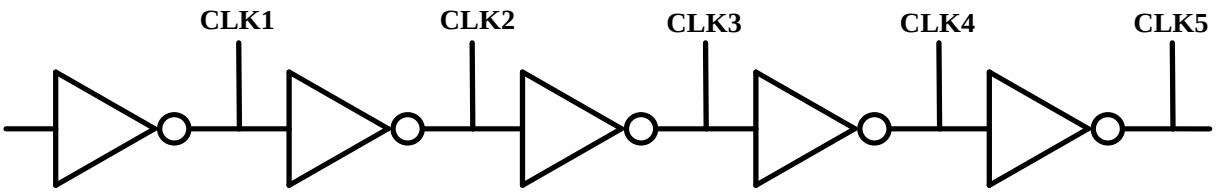

Fig. 2.10. Inverter delay line.

2.6.3 Ring Counter and Shift Register

The combination of ring counter and shift registers is commonly used as the SAR logic. The clocks are generated sequential and monotonic by the D flip flops triggered by ready signal of

comparators. At the positive edge of clock, D flip flop catch the value of comparator and stores as the SAR ADC outputs [11].

2.7 SAR ADC Performance Metrics

2.7.1 Differential Nonlinearity

Differential nonlinearity is the error between the ideal step 1 LSB and actual step. The completely ideal DNL is 0. If the actual step is 0.5 LSB longer than 1 LSB, the DNL error is +0.5 LSB; if the actual step is 0.5 LSB shorter than 1 LSB, the DNL error is -0.5 LSB. The DNL error less or equal to LSB is important because it assures the SAR ADC monotonic performance without missing code.

2.7.2 Integral Nonlinearity

Integral nonlinearity is the deviation from the straight line which is typically center of the input range. The distribution of the DNL error decides the INL. INL also can be characterized as the sum of the all DNL errors.

2.7.3 Offset Error and Full Scale Error

Offset error is the deviation between the first actual code transition and idea code transition. Full scale error is the deviation between the last actual code transition and idea code transition.

2.7.4 Missing Code

Missing code means digital value of the corresponding input voltage is missing. If DNL is less than 1 LSB, it means there is no missing code during the conversion process, if an error is more than 1 LSB in DNL graph, it's a sign that there is a missing code in conversion process.

2.7.5 Signal to Noise Ratio

Signal to noise ratio is the ratio of the power of the input signal to the power of total noise.

$$SNR_{dB} = 10log_{10}\frac{P_{signal}}{P_{noise}} \tag{2.17}$$

where P_{signal} is the power of the signal and P_{noise} is the power of the total noise.

For an ideal ADC

$$SNR_{dB} = 6.02N + 1.76 \tag{2.18}$$

where b is the number of bits of the ADC

2.7.6 Signal to Noise and Distortion Ratio

Signal to noise and distortion ratio is the ratio of the received power to the power of noise plus distortion components.

$$SINAD = \frac{P_{signal}+P_{noise}+P_{distortion}}{P_{noise}+P_{distortion}} \tag{2.19}$$

where P_{signal} is the power of the signal, P_{noise} is the power of the noise and $P_{distortion}$ is the power of the distortion.

2.7.7 Spurious-Free Dynamic Range

Spurious-free dynamic range is the ratio of the fundamental signal to the strongest harmonic tone in the output. It is a very crucial specification of the dynamic performance. As we know, due to

the noise and nonlinearity, even the best generator is not able to generate the pure signal without harmonics. It is easy to calculate SFDR by

$$SFDR_{dB} = A_{fundamental}(dB) - A_{strongest\ spurious}(dB) \tag{2.20}$$

where $A_{fundamental}$ is the amplitude of the fundamental signal, and $A_{strongest\ spur}$ is the strongest spurious signal.

2.7.8 Effective Number of Bits

ADC's resolution is the number of bits to represent the input value. Effective number of bits is obtained by SINAD and to define the accuracy of the ADC.

$$ENOB = \frac{SINAD - 1.76}{6.02} \tag{2.21}$$

where SINAD is the signal to noise and distortion ratio, 1.76 is the number from quantization error of the ideal ADC, 6.02 is from $10log_{10}2$.

Chapter 3: Proposed Structure of S&H and Control Logic

3.1 Proposed Structure of S&H

3.1.1 Bootstrapped Switch Theory

As shown in Fig 3.1, during the off phase, Clock turns off while Clock bar turns on. Devices M7 and M8 discharge the gate of M10 onto the ground. Meanwhile, V_{DD} charges the capacitor Cs through M4 and M3. M5 and M6 isolate the M9 and M10 from Cs when capacitor is charged. The charged capacitor Cs will be connected in the gate of M10 during the on phase.

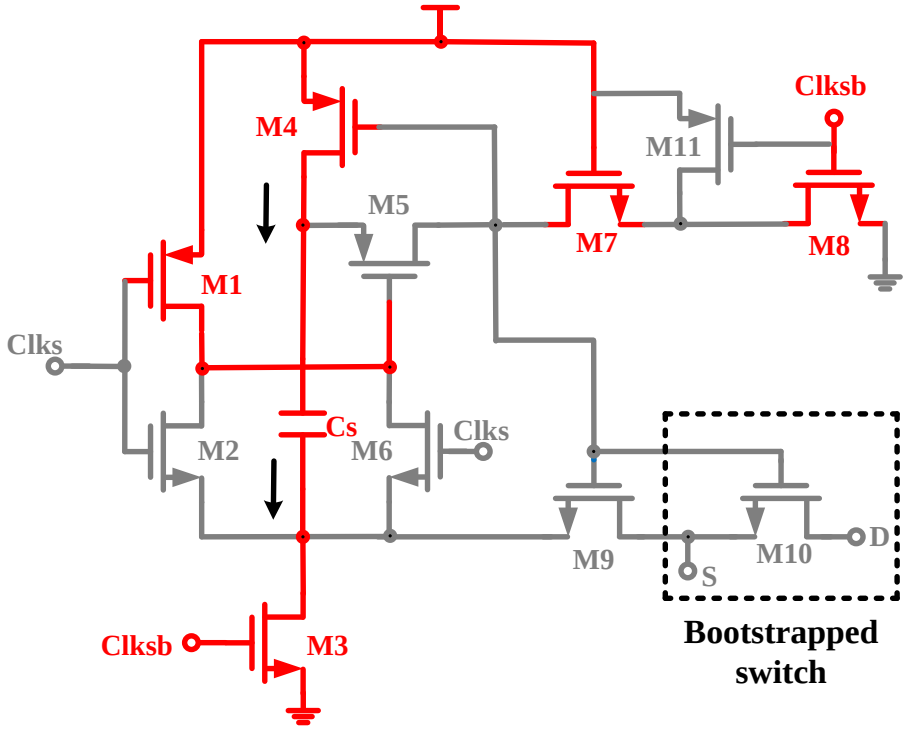

Fig. 3.1. Bootstrapped switch during off phase.

As shown in Fig 3.2, during the on phase, Clock turns on while Clock bar turns off. PMOS M5 is on, so the charge from the capacitor Cs flows through M5 to the gate of M9 and M10 to turn them

on. The gate of M10 will track the input voltage Vin plus V_{DD} from capacitor Cs, and keep the gate to source voltage constant despite the input signal [12] as shown in figure 3.3.

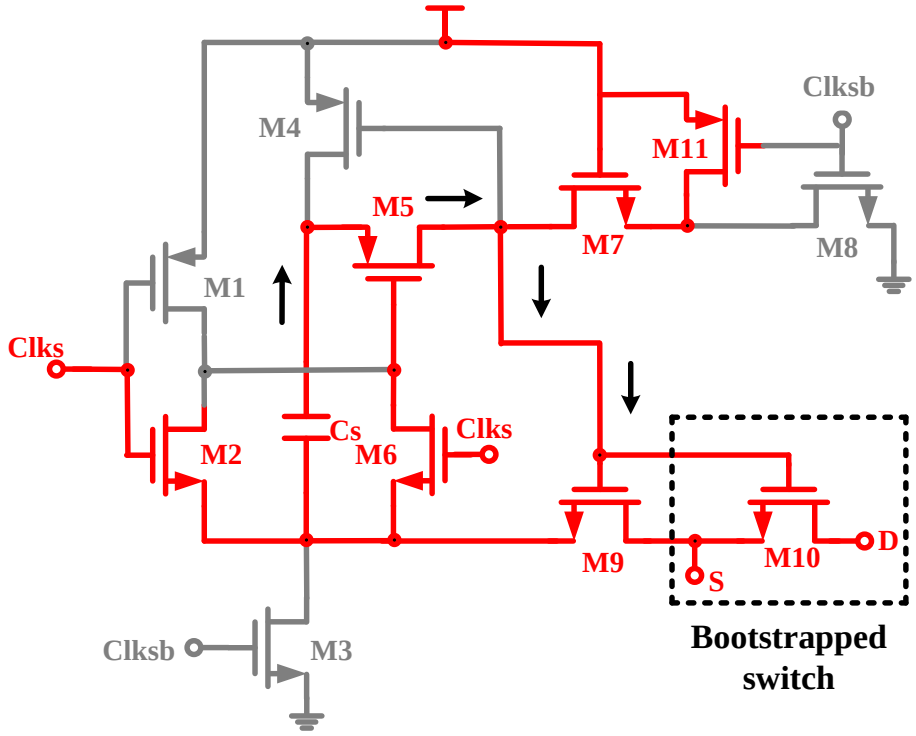

Fig. 3.2. Bootstrapped switch during on phase.

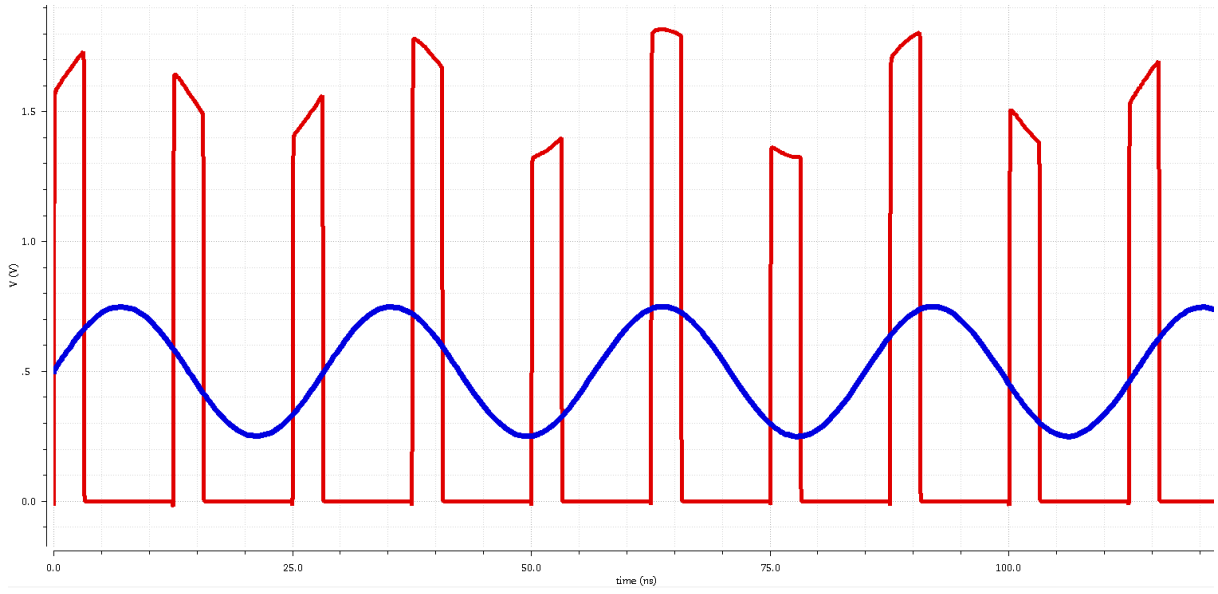

Fig. 3.3. Input signal with the clock pulses on gate of M10.

The resistant of the switch is

$$Ron = \frac{1}{uC_{ox}\frac{W}{L}(V_{GS}-V_{TH})} \tag{3.1}$$

The purpose of the bootstrapped circuit is to alleviate the problem of the variable on-resistance. The constant V_{GS} makes on-resistance relatively independent regardless of the input signal. The resistant of the switch will be

$$Ron = \frac{1}{uC_{ox}\frac{W}{L}(V_{DD}-V_{TH})} \tag{3.2}$$

It will improve the linearity and decrease the harmonic distortion of circuit.

To ensure sample and hold switch can track 99.9 percentage of the input signal, we should keep W/L of the switch big enough. Figure 3.4 shows the tracking time of the different W/L of the switch. If W/L is 3u/120n, it takes 2.53 ns to track 99.9 percentage of the input signal. Because the sampling time of our design is 2.08 ns, so the W/L of the switch must be greater than 3.65u/120n. I use 8u/120n as the W/L of the switch in this design to guarantee switch has enough time to track the input signal.

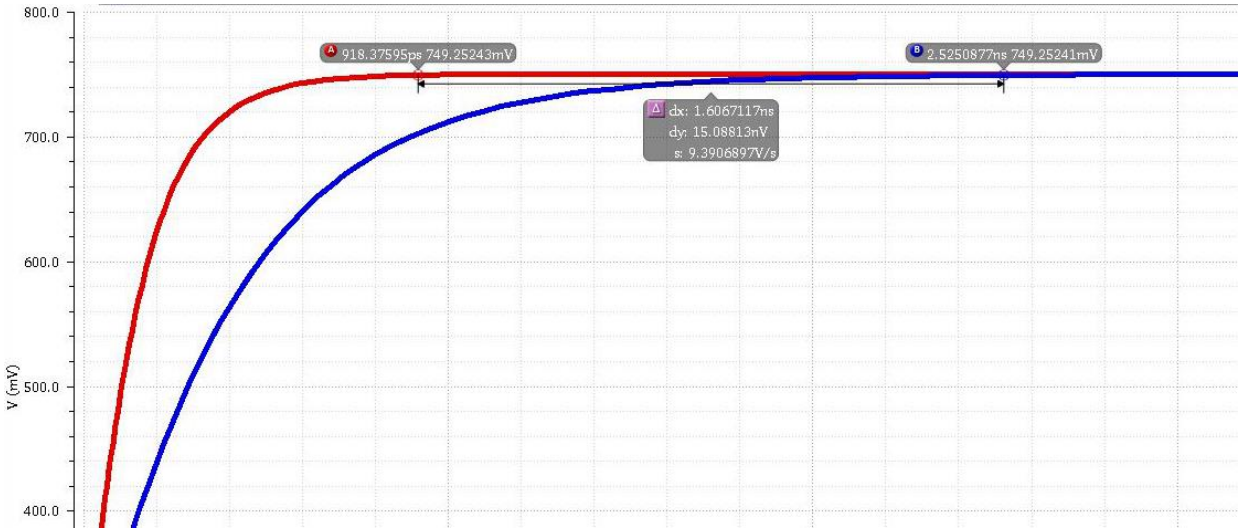

Fig. 3.4. Tracking time of the different W/L of the switch.

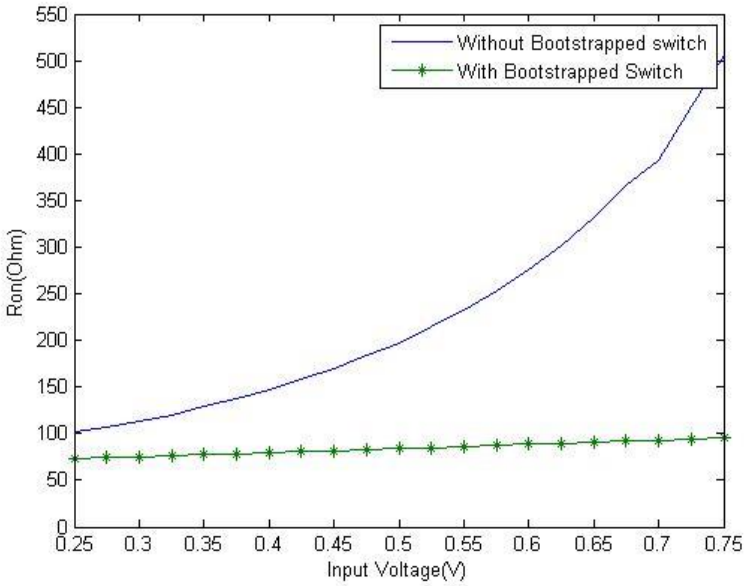

Fig. 3.5. Ron vs input voltage.

As shown in figure 3.5, with bootstrapped switch structure, on-resistant of the switch is minimized and relatively independent of the input signal.

3.1.2 Conventional and Proposed Bootstrapped Switch

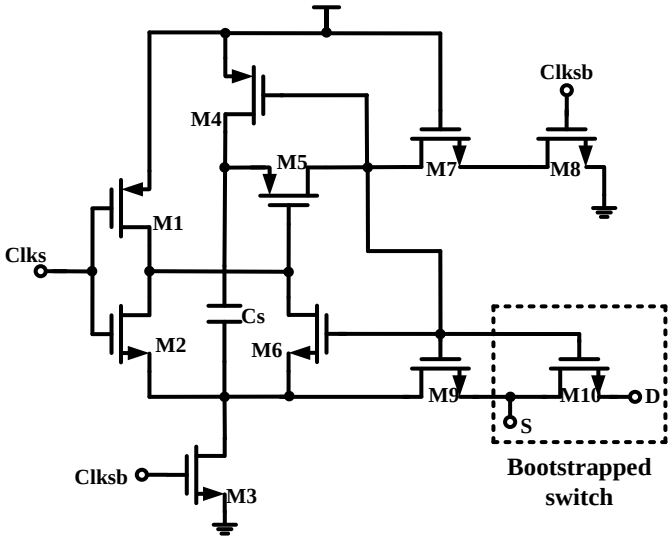

Fig. 3.6. Conventional bootstrapped switch.

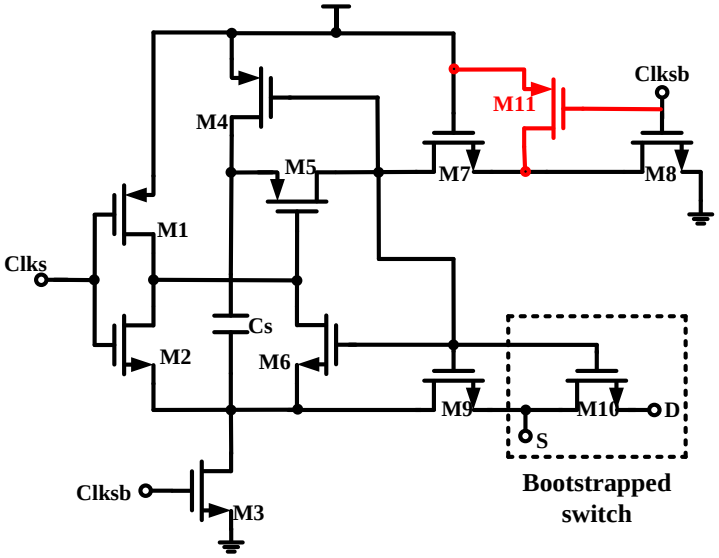

Fig. 3.7. Proposed bootstrapped switch.

In the proposed bootstrapped switch as shown in figure 3.7, we introduce the extra NMOS named M11 in conventional bootstrapped switch as shown in figure 3.6.

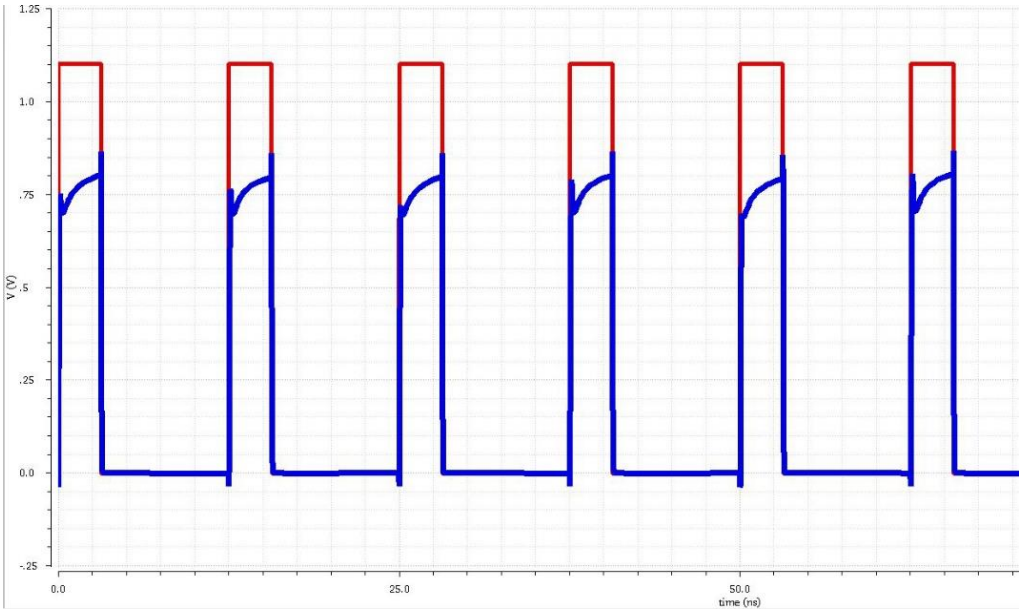

Fig. 3.8. Voltage of source of M7 between conventional and proposed switch.

During the on phase, Clock turns on while Clock bar turns off, so both voltages of gate and source of M7 are equal to V_{DD}, so the transistor is cut off and no electrons will flow between drain and source. However, without M11, the source of M7 is floating which brings noise to the gate of the switch as shown in figure 3.6. With M11, the source of M7 is charged to V_{DD}. Also, with M11, the leakage voltage of M7 will be reduced to improve the switch linearity as shown in figure 3.9 [13]. Using the proposed switch, we can reach better linearity.

Fig. 3.9. Voltage of gate of the switch between conventional and proposed switch

3.1.3 Bootstrapped S&H Circuit with Dummy Switch

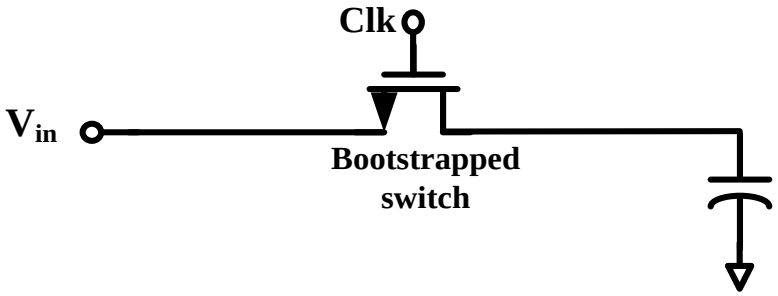

Fig. 3.10. Simple bootstrapped S&H circuit.

As shown in figure 3.10, the sample clock controls the on and off mode of the NMOS. The signal is sampled when the sample clock is high while the signal is stored when the sample clock is low.

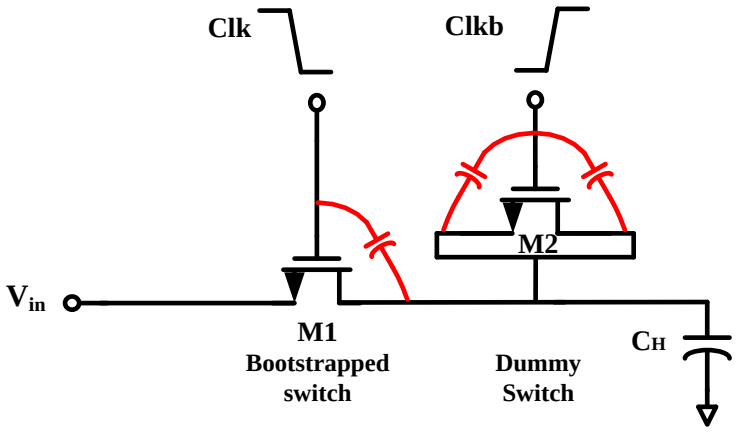

Fig. 3.11. Bootstrapped S&H circuit with dummy switch.

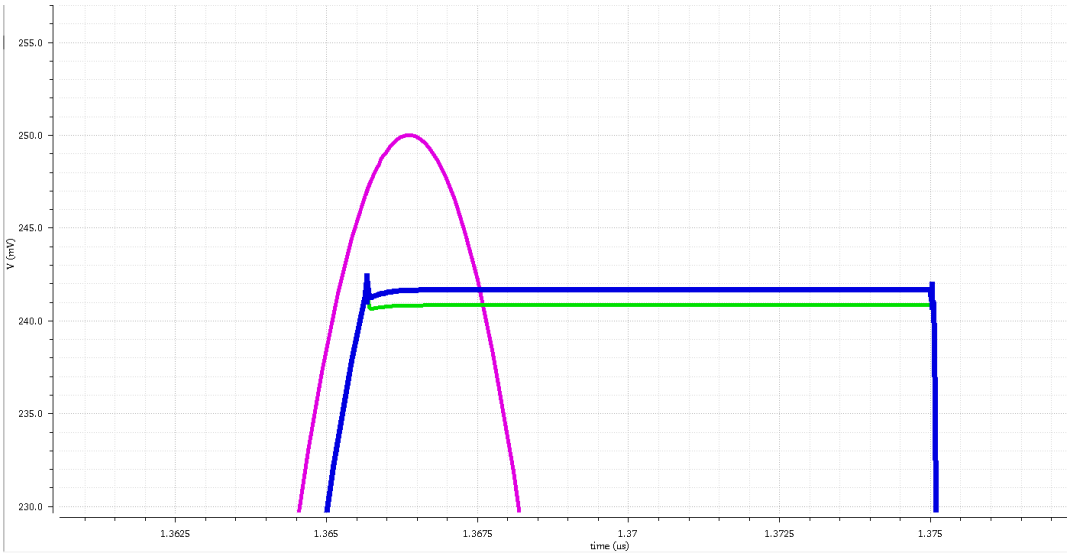

Fig. 3.12. Comparison of the bootstrapped S&H circuit with and without dummy switch.

As shown in figure 3.11, the dummy switch plays an important role in holding phase to make holding better. When Clock goes from high to low, at the same time, the Clock bar in the gate of dummy switch goes from low to high, the charge deposited in inversion layer in M1

$\frac{1}{n}WLC(V_{DD} - V_{in} - V_{TH})$ will be absorbed by the latter dummy switch. The error of charge injection is

$$\Delta V = -\frac{WLC(V_{DD}-V_{in}-V_{TH})}{nC_{Hold}} \tag{3.3}$$

Also, the gate-source overlap capacitance is switched to ground and introduces an error in the output voltage. When the Clock bar in the gate of dummy switch goes from low to high, the gate-source overlap capacitances are switched to the supply voltage, so the effect of the clock feedthrough is eliminated [14]. The error of clock feedthrough is

$$\Delta V = -V_{clock}\frac{C_{overlap}}{C_{overlap}+C_H} \tag{3.4}$$

To make sure the charge injected by the M1 is equal to the charge absorbed by the M2 and to suppress the effect of the clock through, we use L_1=L_2 and W_1=2W_2. The error of the charge injection is reduced because

$$-\frac{W_1L_1C(V_{DD}-V_{in}-V_{TH})}{nC_{Hold}} + \frac{2W_2L_2C(V_{DD}-V_{in}-V_{TH})}{nC_{Hold}} = 0 \tag{3.5}$$

and the total error from overlap capacitors is zero because $C_{overlap}$ is proportional to W

$$-V_{clock}\frac{C_{overlap1}}{C_{overlap1}+2C_{overlap2}+C_H} + V_{clock}\frac{2C_{overlap2}}{C_{overlap1}+2C_{overlap2}+C_H} = 0 \tag{3.6}$$

3.1.4 Bootstrapped S&H Circuit with Cross-Couple Path and Dummy Switch

When the switch goes from high to low, the input signal is coupled to the C_H through the parasitic capacitance between source and drain terminals, so the parasitic capacitor will introduce the error and cause the dynamic offset. The cross-couple path is proposed to cancel the error, because the Vin and Vip are the opposite signals and introduce the opposite charges to reduce the coupling effect.

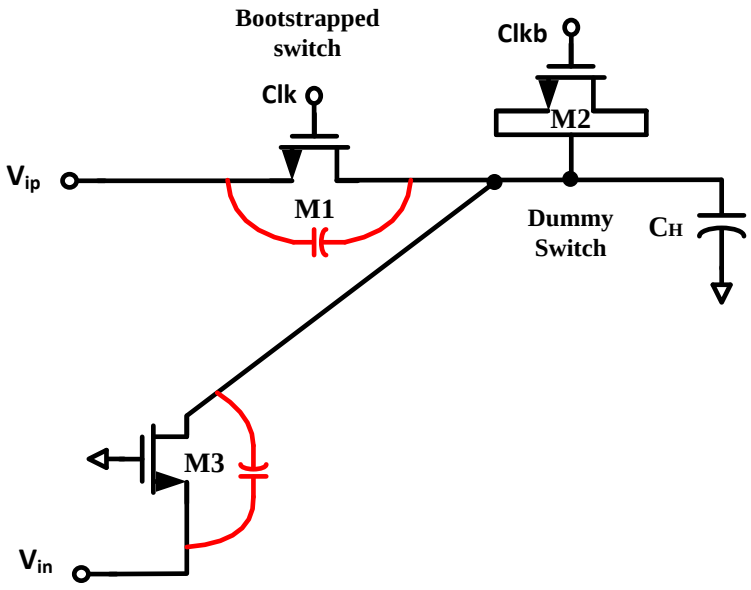

Fig. 3.13. Bootstrapped S&H circuit with cross-couple path and dummy switch.

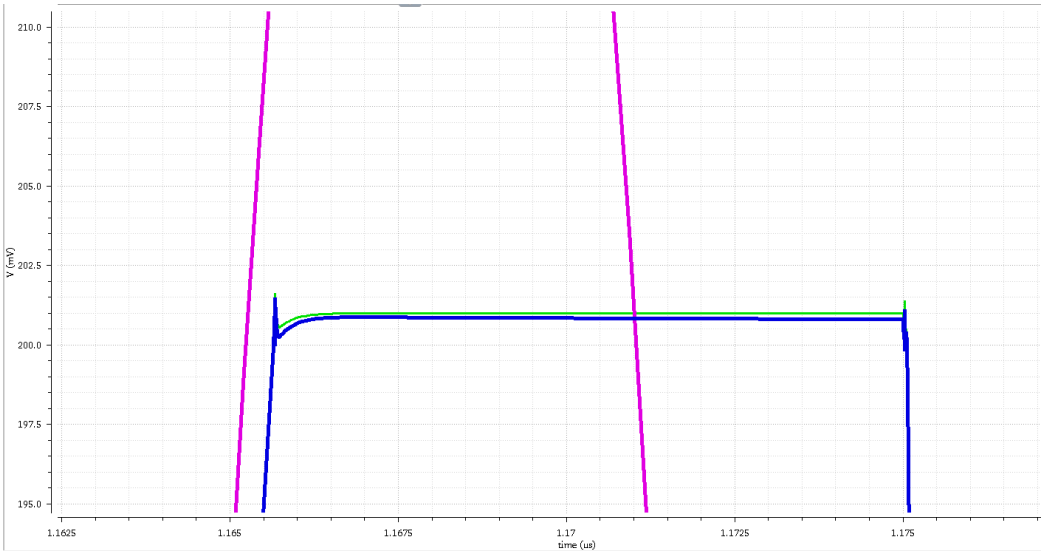

Fig. 3.14. Comparison of the bootstrapped S&H circuit with and without cross couple path.

3.1.5 KT/C Noise

The KT/C is one of the noise sources in the ADC and should be less than 1/2 LSB of the system. From KT/C noise, we will get the minimum capacitor we need to use for the cap DAC used in

SAR ADC. From this ADC, LSB is $0.5v/2^8$ is equal to 1.95mv. From the equation $\sqrt{KT/C}$ is less than half LSB, so the minimum capacitor is 4.3fF. In our design, the minimum capacitor is 17fF, which is greater than 4.3fF.

3.1.6 Simulated Spectrum

The simulated spectrum of a simple sample and hold is shown in figure 3.15, the input signal is 35.3125MHz with an 80MS/s sample frequency. The SFDR and SNDR in this architecture are 40.9dB and 40.4dB, respectively.

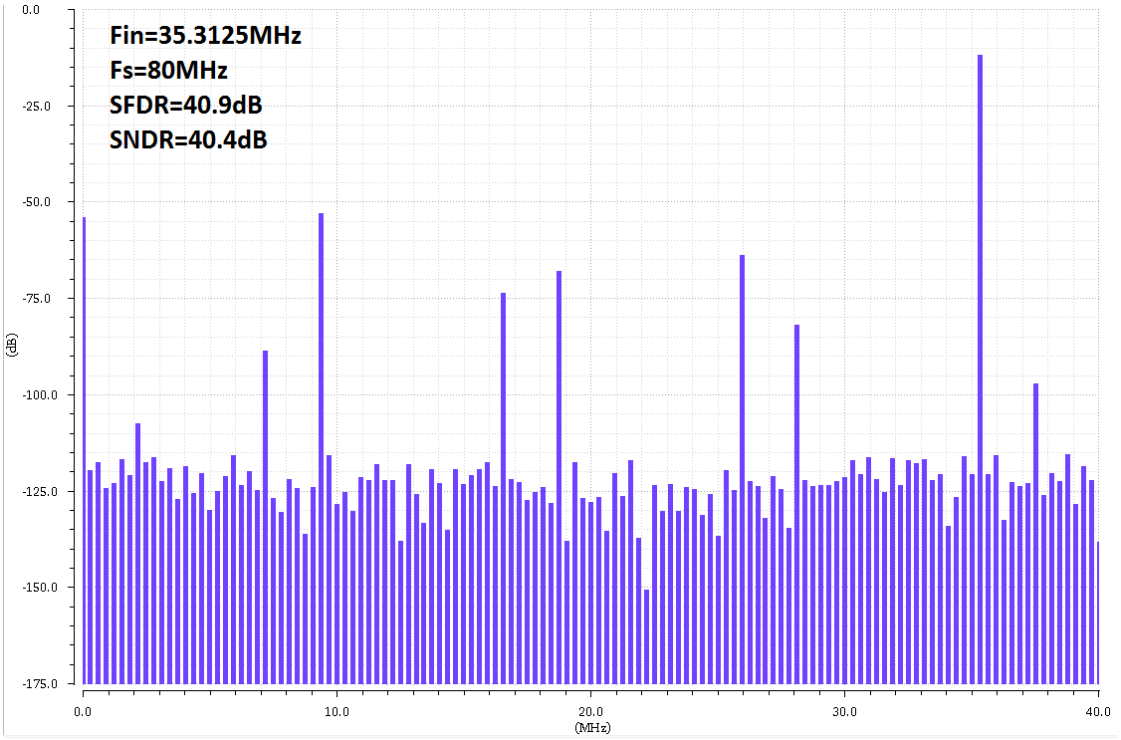

Fig. 3.15. Simulated spectrum at 80MS/s of conventional S&H architecture.

The measured spectrum of the proposed sample and hold is shown in figure 3.16. It achieves 90.9 dB SFDR and 87.8dB SNDR. We can reach a conclusion that the proposed sample and hold has better linearity and performance.

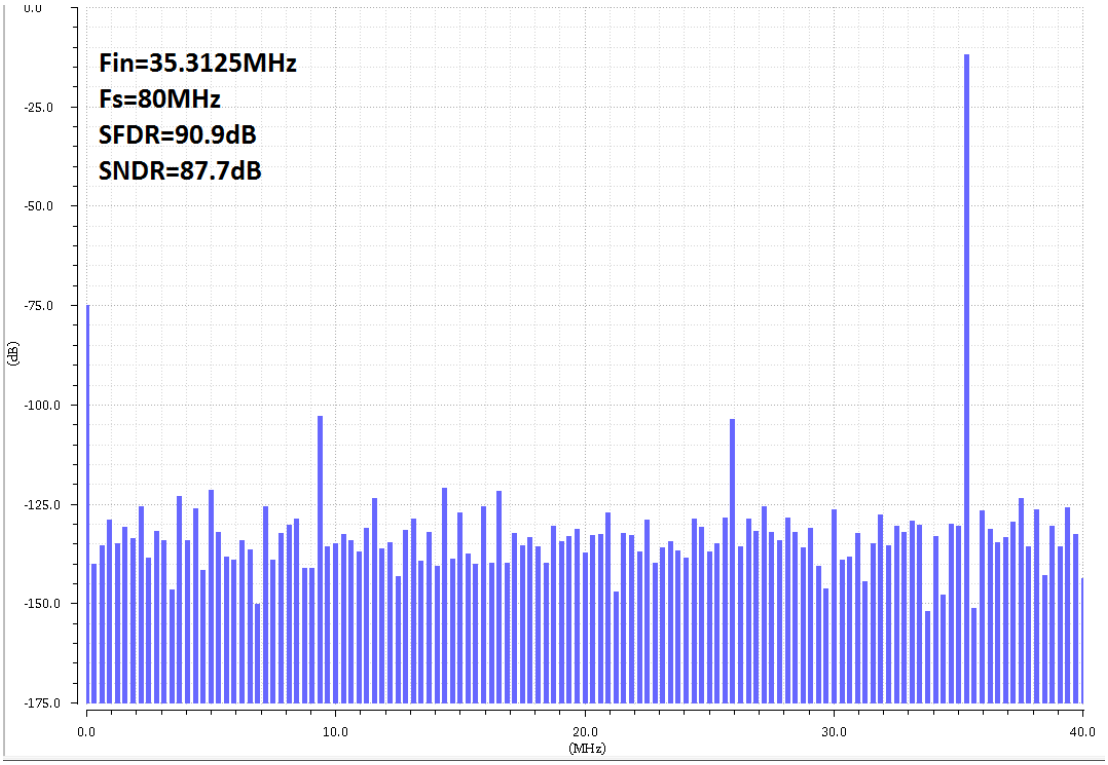

Fig. 3.16. Simulated spectrum at 80MS/s of proposed S&H architecture.

3.2 Proposed Structure of Control Logic

3.2.1 Overview of SAR ADC Control Logic

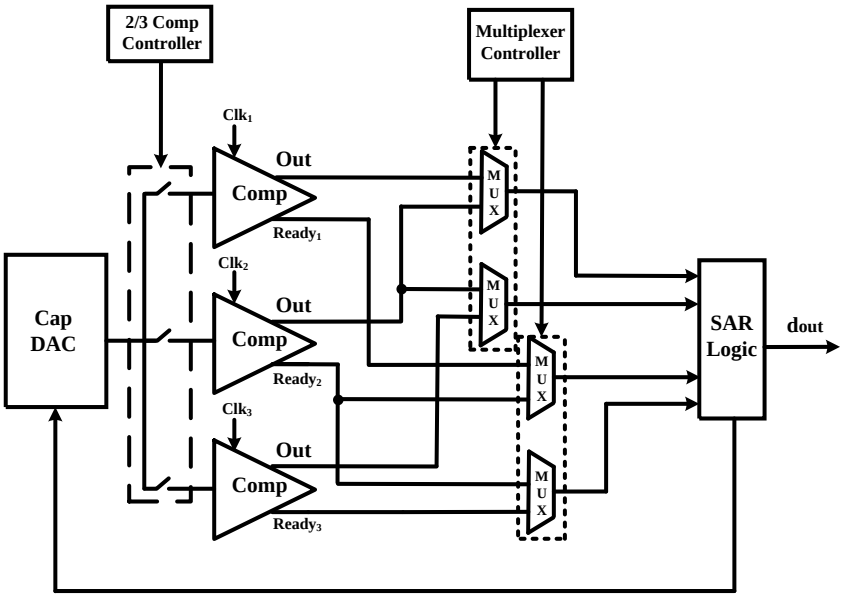

Fig. 3.17. SAR ADC control logic overview.

As shown in figure 3.17, in the first cycle, 2 of the 3 comparators (take comparator 1 and comparator 2 as an example) are chosen by the 3/2 logic controller while comparator 3 enters the calibration mode. In the next cycle, another set of 2 comparators (comparator 2 and comparator 3 in this example) are chosen and activated while comparator 1 enters the calibration mode, and so on. Then ready signals are selected by multiplexers, clock 1 to clock 8 are generated for the capacitor array to work on the monotonic switching procedure. The output bits of comparator are stored in memories, and DAC starts to redistribute based on the decided bit.

3.2.2 Mux Logic

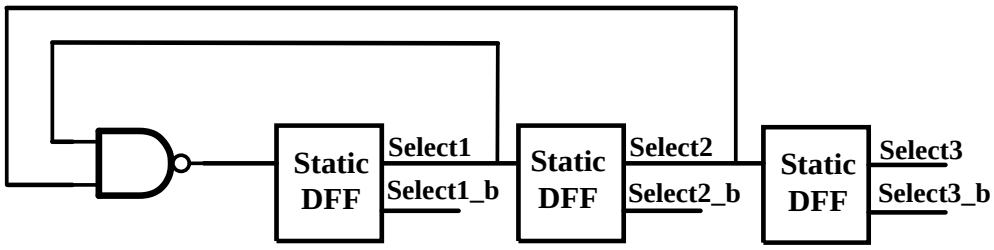

Fig. 3.18. Multiplexer control signal generator.

Fig 3.18 shows multiplexer control signal generator is based on the clock divider where the clock is divided by three with 2/3 duty cycle. Frequency divider plays an important role in phase related clock circuit. Dividing a clock by an even or odd number is not complicated, usually the arrangement of static D flipflop and different digital logic gates is the most popular method [15]. I use three static D flipflops and one NAND gate to accomplish it.

SN7474 dual positive edge triggered D flipflop is used in this multiplexer logic, it concludes six

NAND gates. This D flipflop stores the value of input as the output when the rising edge is triggered and will not change conditions at other times. Edge triggered feature helps to eliminate the unstable transitions of system, any unstable transitions could make system doesn't work or have critical mistakes.

NAND gate is used to generate low output if both inputs are high. If one of the inputs is low or both the inputs are low, output is high.

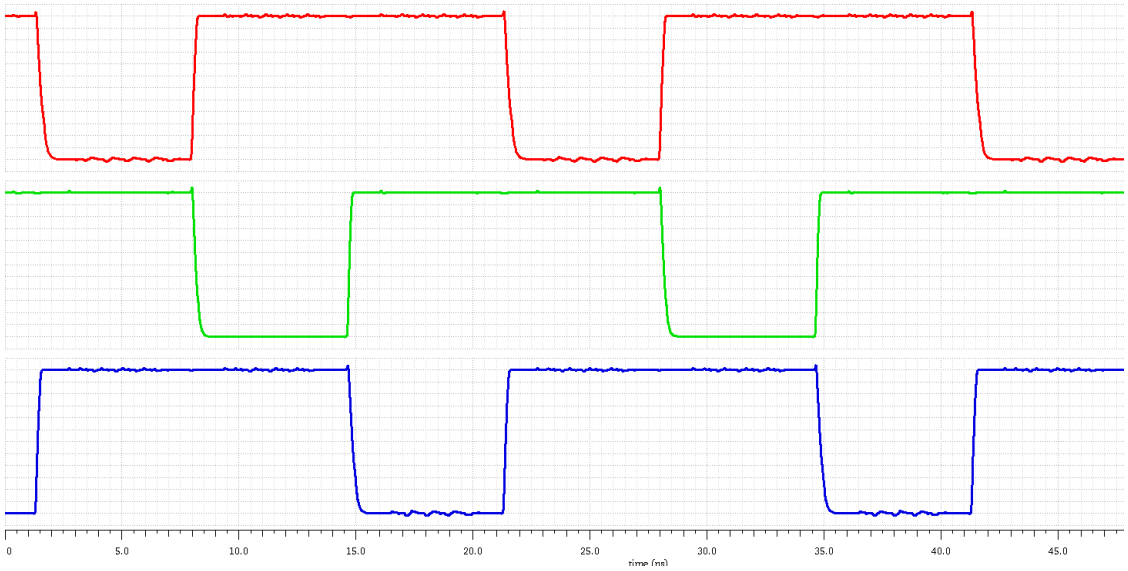

Fig. 3.19. Timing diagram for multiplexer control signal generator.

Because the comparator is interleaved by three, so two comparators are working while another is doing calibration per sample rate clock. Figure 3.19 shows the working order arranged by the multiplexer control signals. So, at the first sample rate clock, comparator 1 is doing calibration and comparator 2 and 3 are sampling the input; at the second sample rate clock, comparator 2 is doing calibration and comparator 1 and 3 are sampling the input; at the third sample rate clock, comparator 3 is doing calibration and comparator 1 and 2 are sampling the input.

3.2.3 Timer Logic

Because this design has three comparators and two comparators work per sampling rate clock, so timer logic as shown in Fig 3.20 can make sure timers track DAC settling behaviors and work in order. Timers are used for improving the ADC efficiency. Because settling time goes faster from MSB (Most significant bit) to LSB (Least significant bit), it will not efficient if comparators are waiting for the same long amount of time. Since timers can track the behaviors of DAC, so it can help to save time. The disadvantage of timer is adding more capacitors to track the DAC settling, so it will bring more power consuming and area.

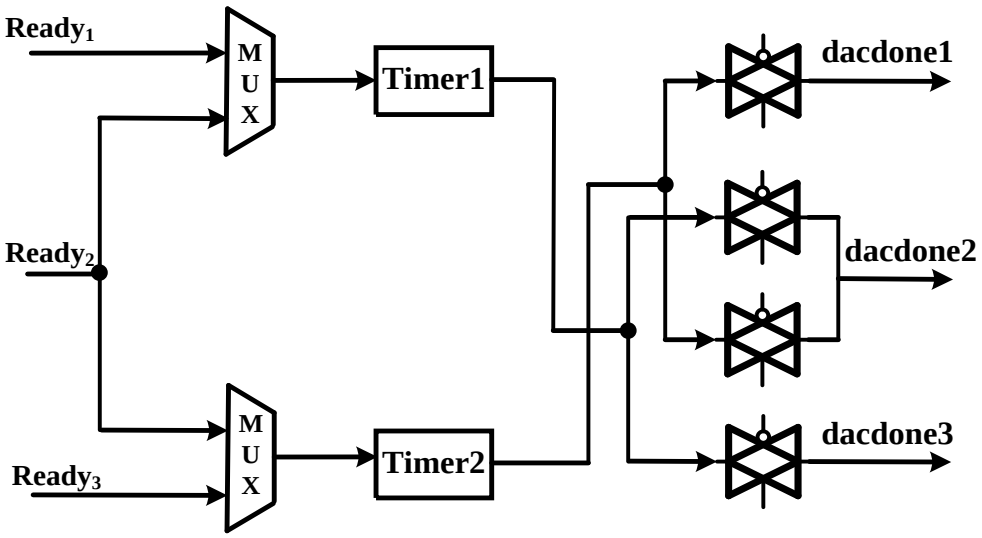

Fig. 3.20. Architecture of timer logic.

Figure 3.21 and figure 3.22 show ready signals and DAC done signals work in order per sampling rate clock. At first sampling clock, comparator 2 and 3 generate ready signals and DAC done 2 and 3 back to comparator 2 and 3. At second sampling clock, comparator 1 and 3 generate ready signals and DAC done 1 and 3 back to comparator 1 and 3. At third sampling clock, comparator 1 and 3 generate ready signals and DAC done 1 and 3 back to comparator 1 and 3.

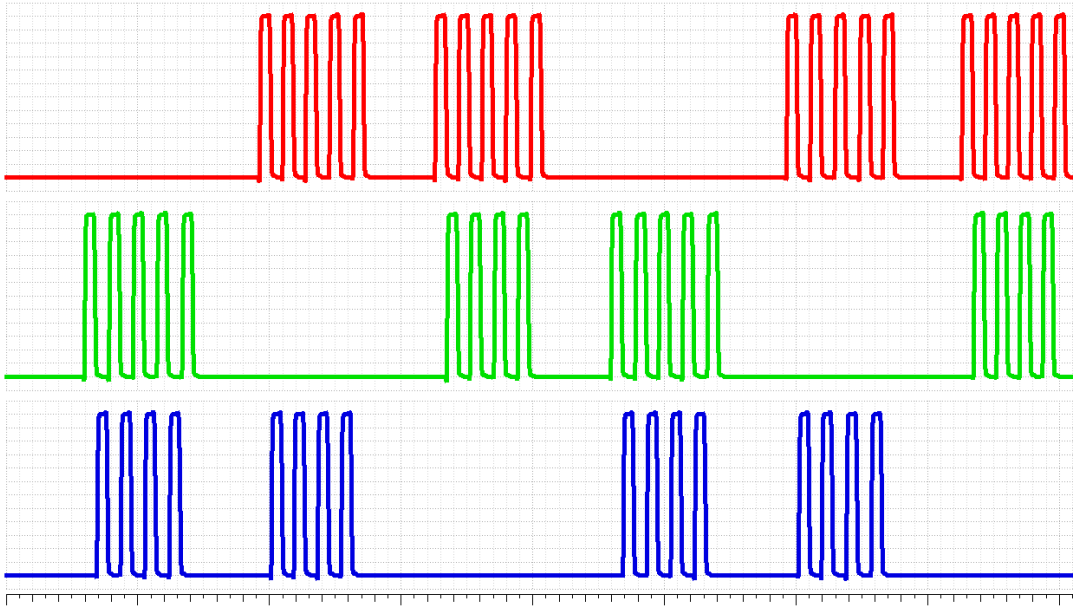

Fig. 3.21. Ready signals from three comparators.

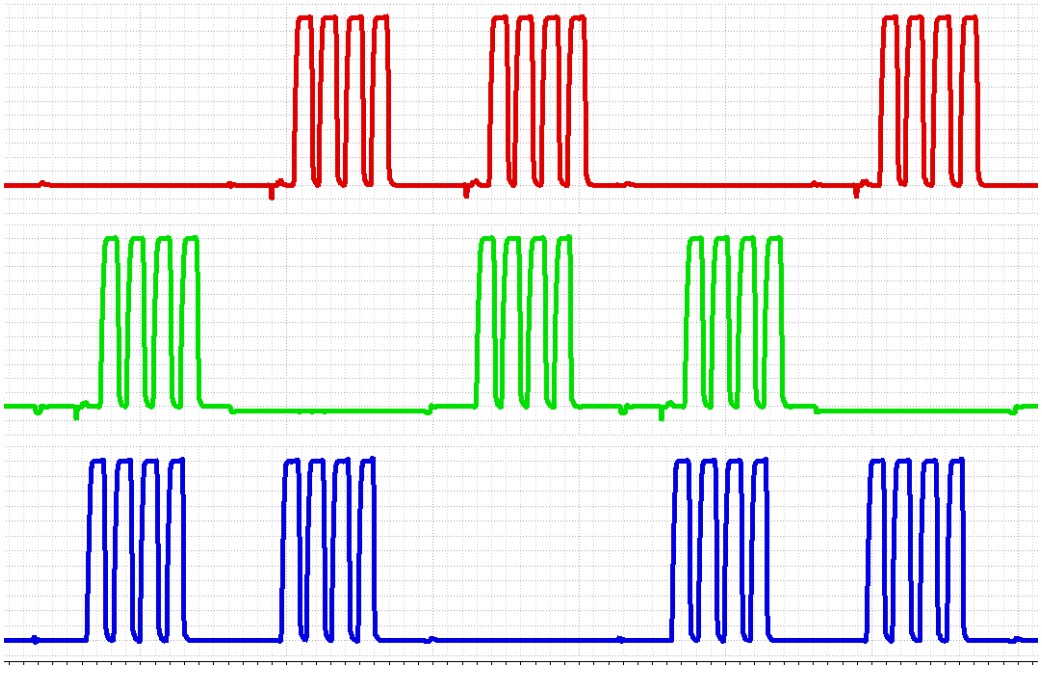

Fig. 3.22. DAC done signals from timers.

3.2.4 Bits Clock Logic

As shown in Figure 3.23, comparators generate three ready signals, then two signals are selected through multiplexers. Clock1 to clock 8 are generated by the dynamic D flip flops to sample the outputs of comparators according the orders and to control the capacitor array to work on the monotonic switching.

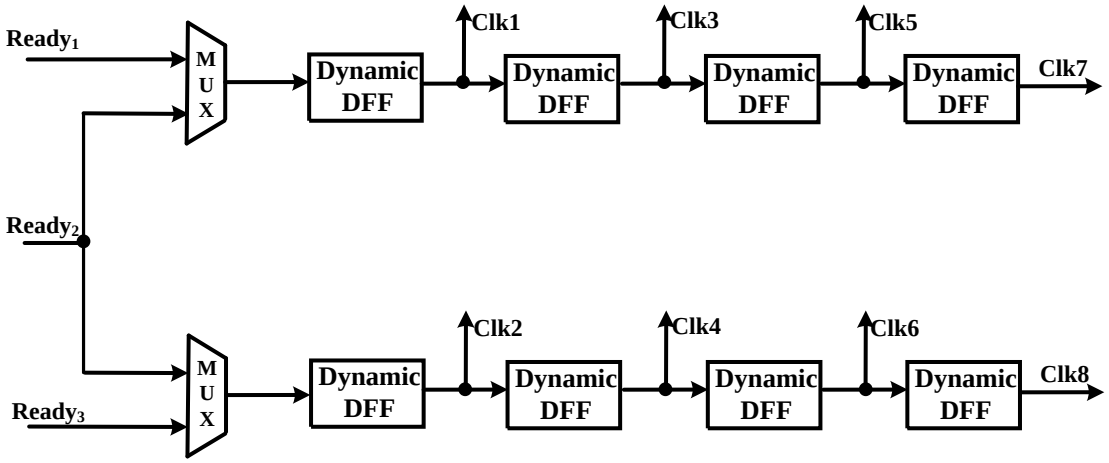

Fig. 3.23. Bits clock control logic schematic.

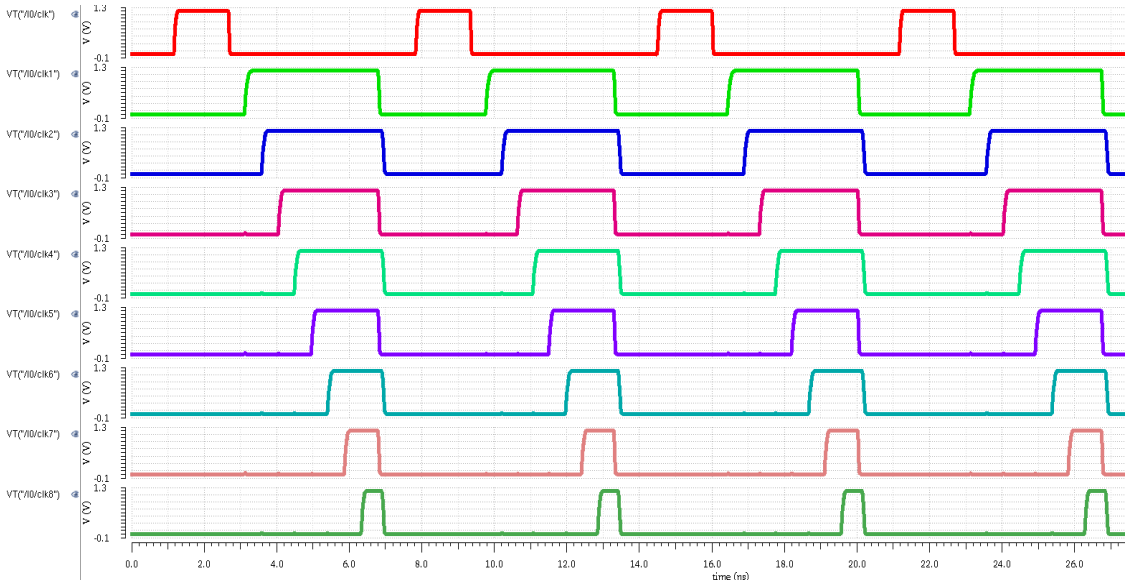

Fig. 3.24. Bits clock control logic timing diagram.

Dynamic D flip flop is used in this block. It is not a literally flip flop, but has the same functional role as static flip flop. As the static D flip flop is triggered by positive or negative edge, the clock level triggers the dynamic D flip flop, and the input signal will be stored in parasitic capacitances of circuits [16]. However, dynamic D flip flop cannot be implemented in low speed system because the charge which stored in parasitic capacitances is gradually leaking if it has enough time and cause critical mistakes. So, dynamic flip flop is normally used in high speed system and helps to reduce power consumption since it just has a few transistors.

3.2.5 DAC Control Logic

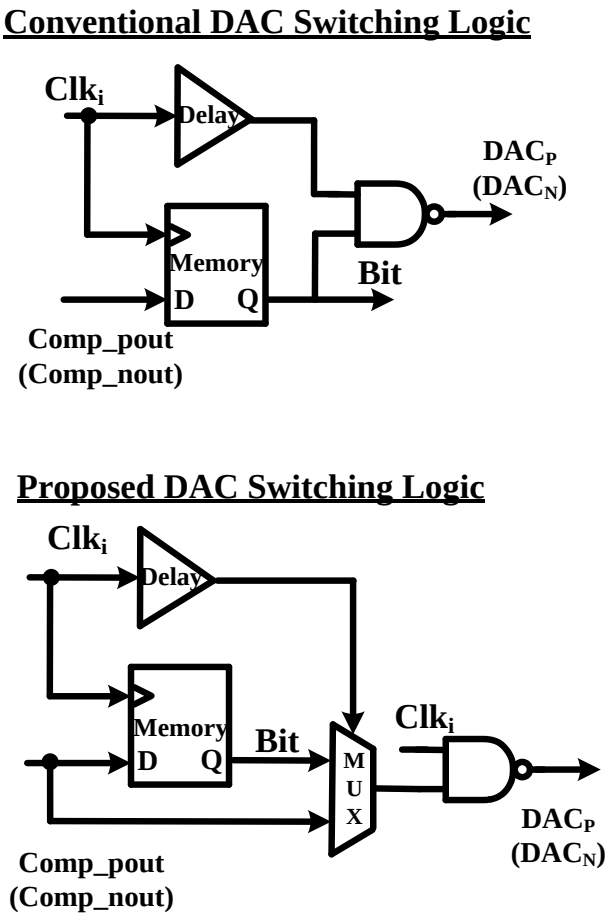

Fig. 3.25. Schematic of conventional and proposed DAC control logic.

Figure 3.25 shows the schematic of the conventional and proposed DAC control logic. Conventional DAC is switched after the output of comparator is successfully stored in memory while proposed DAC is switched before the output of comparator is stored in memory.

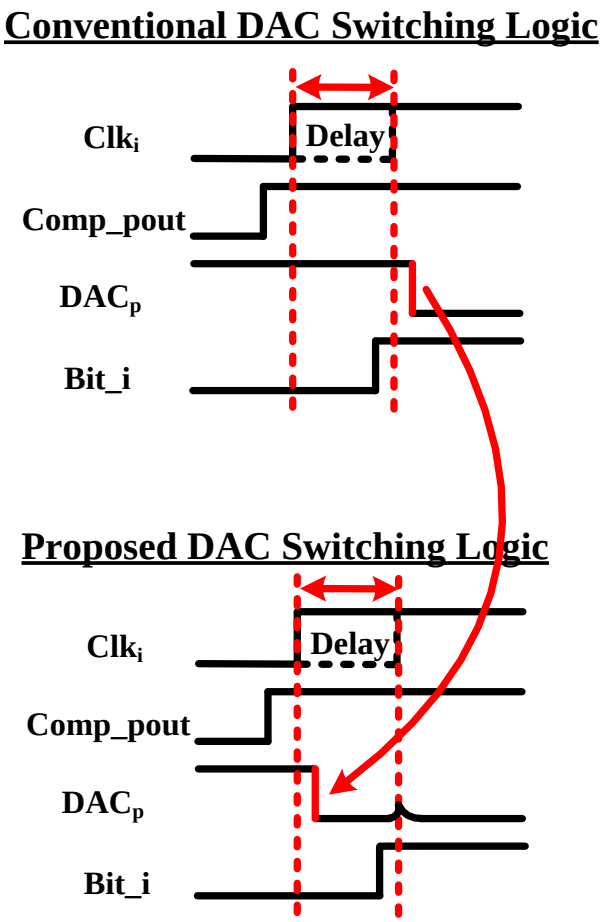

Fig. 3.26. Timing diagram of conventional and proposed DAC control logic.

As shown in figure 3.26, the bit-correlated clock signal is delayed for a certain amount of time based on the time of the output of comparator going through the memory to avoid unnecessary transitions, and then triggers the NAND gate to let the DAC redistributes based on the bits. The proposed switching strategy is the NAND gate is triggered right after the successful decision is

made by comparator which is initially connected with the multiplexer. The delayed signal is used as control signal for the multiplexer to switch the input of the NAND gate from the output of comparator to the settled output from memory, so the state of decided bit will be held. As the result, the delay of memory is therefore eliminated. When it applies on all the control logic of eight bits, the time saved will be multiplied by eight.

To make sure clock delay is long enough to avoid unnecessary transition, the simulation results of the delay time and D flip flop setting time with different corners and temperatures are listed in Table 3.1. The time variation with different corners and temperatures will not distort operation.

Corner / Temp	SS		TT		FF	
	DFF	Delay	DFF	Delay	DFF	Delay
0	31.1ps	124.7ps	26.3ps	103.7ps	22.3ps	85.6ps
27	32.3ps	128.8ps	27.1ps	107.3ps	23.2ps	88.8ps
120	38.5ps	140.5ps	31.2ps	118.2ps	26.4ps	99.0ps

Table. 3.1. Delay time and D flip flop setting time with different corners and temperatures.

Chapter 4 Simulation Results and Measurements

The SAR ADC chip was implemented in the 130nm CMOS technology with a core area of 480 x 615um^2. The die photo is shown in figure 4.1. The layout of the ADC is shown in figure 4.2 which includes the S&H, DACs, comparators, SAR logic, reference buffer, output buffer and timer, and the DACs, comparators, and SAR digital logic occupy most of the area. The ADC consumes 2mW from a 1.1V supply voltage for 80MS/s sampling rate, and the full-scale input of the ADC is 500mVpp.

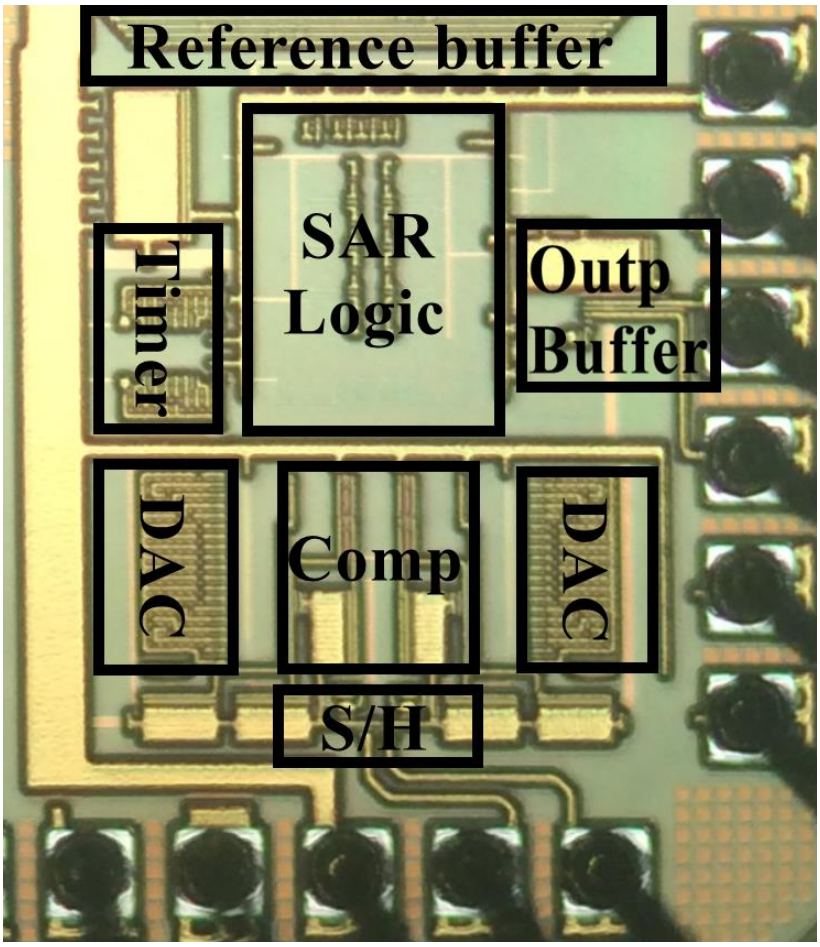

Fig. 4.1. Die photo of the SAR ADC.

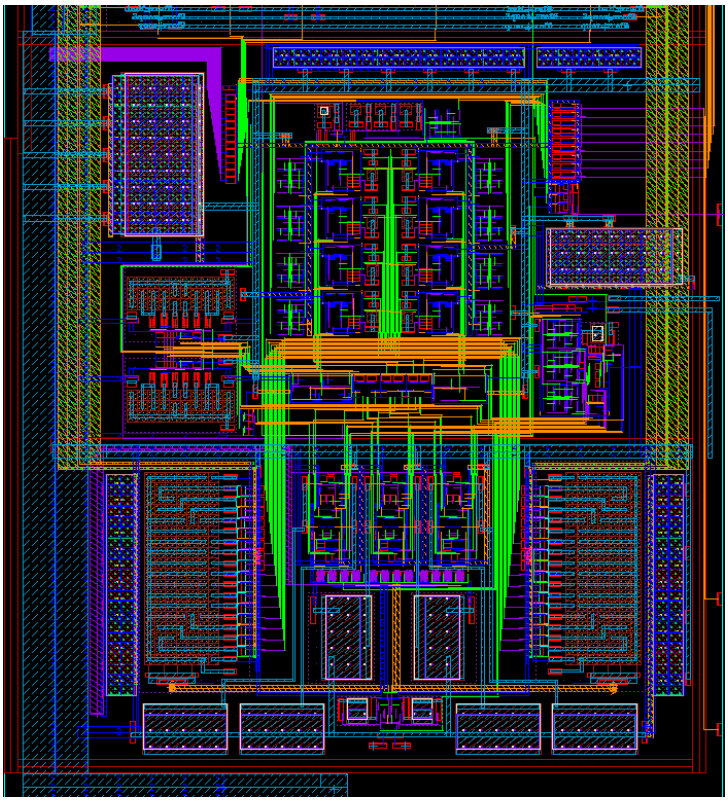

Fig. 4.2. layout of the SAR ADC.

Figure 4.3 and figure 4.4 show the measured static performance of this SAR ADC, it achieves the DNL within +0.9389/-0.8449 LSB and the INL within +0.9667/-1.006 LSB.

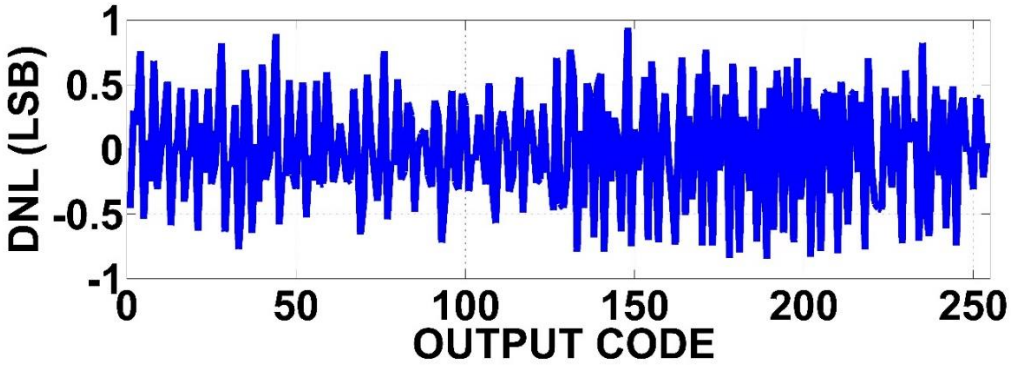

Fig. 4.3. Measured DNL.

Although the DAC does not have calibration block, the linearity performance is improved because the MSB capacitor is reduced by a fact of 2 and the LSB capacitor was increased by a fact of 4 which reduces 8 times of the difference between MSB capacitor and LSB capacitor.

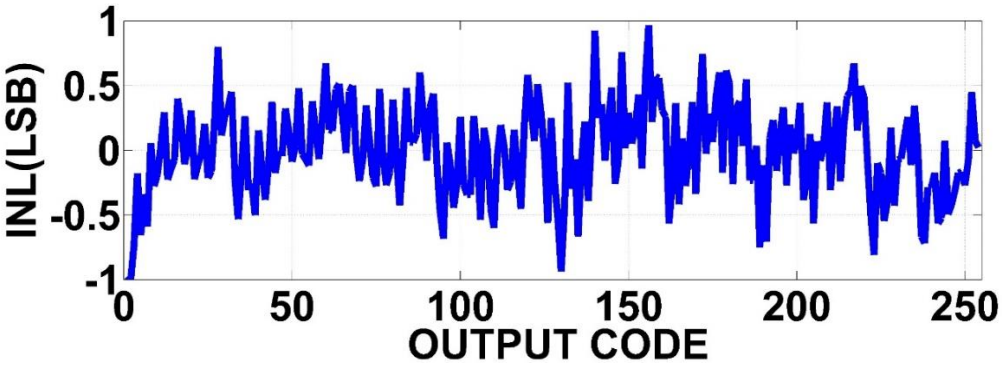

Fig. 4.4. Measured INL.

The measured spectrum of this ADC is shown in figure 4.5, the input signal is 36.1223MHz which is near the Nyquist band with an 80MS/s sample frequency. The ADC achieves 56.8 dB SFDR, 42.8dB SNDR, -53.3dBc THD with a 6.82 ENOB.

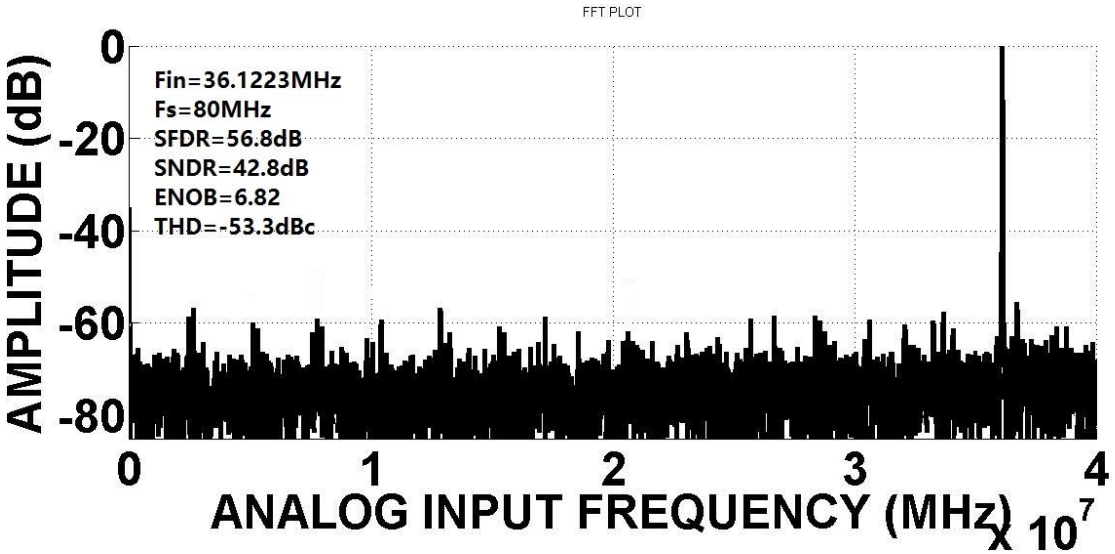

Fig. 4.5. Measured output spectrum of the ADC.

The FoM (Figures of Merit) equation is

$$FoM = \frac{Power}{f_s \times 2^{ENOB}} \tag{4.1}$$

The FoM is 221fJ/Conversion-Step.

Table 4.1 shows all the parameters for the designed SAR ADC chip.

Architecture	SAR
Technology	130nm
Resolution	8
Supply voltage	1.1 V
Sample rate	80MS/s
Full scale input	$500mV_{P-P}$
SFDR	56.8 dB
SNDR	42.8 dB
THD	-53.3 dBc
Power	2 mW
Area	0.295 mm^2
FoM	221fJ/Conversion-Step

Table. 4.1. Performance summary.

Chapter 5 Conclusion

In this thesis, an 8-bit 80MS/s single-core SAR ADC was implemented in 130nm CMOS technology. The Sample and hold with the bootstrapped switch improves the linearity. The DAC with a constant common mode, set-and-down principle, and shrunk MSB reduces the DAC size, settling time and mismatch. The two-way alternate comparator structure is proposed to eliminate the reset time from the critical path, and three-way comparator structure is used where 2 from the 3 comparators are orderly chosen by the logic controller while calibration is operated at the idle comparator. The proposed SAR ADC achieves 80MS/s operation speed with INL/DLN less than 1LSB and only occupies an active area of 0.2952 mm^2 in the 130nm technology. At the Nyquist band, the SNDR, THD, SFDR and ENOB are 42.8 dB, -53.3 dBc, 56.8dB and 6.82, respectively.

References

[1] Martti Parpala, "The U.S. Semiconductor Industry: A Key Contributor to U.S. Economic Growth," *Semiconductor Industry Association*, pp. 1-6, 2014.

[2] J. Fredenburg and M. P. Flynn, "ADC trends and impact on SAR ADC architecture and analysis," *2015 IEEE Custom Integrated Circuits Conference (CICC)*, San Jose, CA, 2015, pp. 1-8.

[3] L. Kull et al., "A 3.1 mW 8b 1.2 GS/s Single-Channel Asynchronous SAR ADC With Alternate Comparators for Enhanced Speed in 32 nm Digital SOI CMOS," in IEEE Journal of Solid-State Circuits, vol. 48, no. 12, pp. 3049-3058, Dec. 2013.

[4] C. C. Liu, S. J. Chang, G. Y. Huang and Y. Z. Lin, "A 10-bit 50-MS/s SAR ADC With a Monotonic Capacitor Switching Procedure," in *IEEE Journal of Solid-State Circuits*, vol. 45, no. 4, pp. 731-740, April 2010.

[5] Chun-Cheng Liu, Yi-Ting Huang, Guan-Ying Huang, Soon-Jyh Chang, Chung-Ming Huang and Chih-Haur Huang, "A 6-bit 220-MS/s time-interleaving SAR ADC in 0.18-μm digital CMOS process," *2009 International Symposium on VLSI Design, Automation and Test*, Hsinchu, 2009, pp. 215-218.

[6] R. Kapusta, J. Shen, S. Decker, H. Li and E. Ibaragi, "A 14b 80MS/s SAR ADC with 73.6dB SNDR in 65nm CMOS," *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers*, San Francisco, CA, 2013, pp. 472-473.

[7] A. J. Lopez-Martin, C. A. De La Cruz, X. Ugalde, R. G. Carvajal and J. Ramirez-Angulo, "Micropower CMOS S&H circuit for ambient intelligence applications," in *Electronics Letters*, vol. 41, no. 17, pp. 935-936, 18 Aug. 2005.

[8] Liang Dai and R. Harjani, "CMOS switched-op amp based sample-and-hold circuit," *Circuits and Systems, 1998. ISCAS '98. Proceedings of the 1998 IEEE International Symposium on*, Monterey, CA, 1998, pp. 476-479 vol.1.

[9] Weize Xu and E. G. Friedman, "Clock feedthrough in CMOS analog transmission gate switches," *15th Annual IEEE International ASIC/SOC Conference*, 2002, pp. 181-185.

[10] Jeong-Sup Lee and In-Cheol Park, "Capacitor array structure and switch control for energy-efficient SAR analog-to-digital converters," *2008 IEEE International Symposium on Circuits and Systems*, Seattle, WA, 2008, pp. 236-239.

[11] T.O. Anderson, "Optimum Control Logic for Successive Approximation Analog-to-Digital Converters," *Computer Design*, vol. 11, no. 7, pp. 81- 86, 1972.

[12] A. M. Abo and P. R. Gray, "A 1.5 V, 10-bit, 14 MS/s CMOS pipeline analog-to-digital converter," *1998 Symposium on VLSI Circuits. Digest of Technical Papers (Cat. No.98CH36215)*, Honolulu, HI, USA, 1998, pp. 166-169.

[13] C. J. B. Fayomi, G. W. Roberts and M. Sawan, "Low-voltage CMOS analog bootstrapped switch for sample-and-hold circuit: design and chip characterization," *2005 IEEE International Symposium on Circuits and Systems*, 2005, pp. 2200-2203 Vol. 3.

[14] C. J. B. Fayomi, G. W. Roberts and M. Sawan, "Low-voltage CMOS analog bootstrapped switch for sample-and-hold circuit: design and chip characterization," *2005 IEEE International Symposium on Circuits and Systems*, 2005, pp. 2200-2203 Vol. 3.

[15] Huagui Bao, Zhiqun Li, Qin Li and Zhigong Wang, "Design of a 24 GHz Programmable Frequency Divider in 65-nm CMOS Process," *Atlantis Press*, pp. 1854-1861, 2013.

[16] Sung-Hyun Yang, Younggap You and Kyoung-Rok Cho, "A New Dynamic D-Flip-Flip Aiming at Glitch and Charge Sharing Free," IEICE TRANS. ELECTRON., vol. E86-C, no. 3, pp. 496-505, 2003.