Radiation Hard Thin Film Transistors and Logic Circuits Based on ZnO and Related Materials

by

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Abstract

Thin film and thin film transistors (TFTs) and logic circuits based on zinc oxide (ZnO) and related materials, such as zinc tin oxide (ZTO), are designed, fabricated and characterized in this Ph.D. dissertation. ZnO as a metal oxide semiconductor provides many advantages such as non-toxicity, environmental stability, and transparency. Its wide band gap, high displacement threshold energy and large free-exciton binding energy make it a viable candidate for space-based radiation-hard electronics and optoelectronics. Therefore, it is meaningful to study and optimize the process of ZnO TFTs fabrication.

Focused on this work, most ZnO TFTs have been produced by low cost, simple set-up and high throughput sol-gel spin-coating. Temperature dependent IV measurement as a convenient and precise method for localized subgap density of states (DOSs) extraction has been applied to ZnO (especially sol-gel derived ZnO) transistors for the first time. According to the DOSs distribution calculation, the influence of annealing temperature on ZnO sol-gel derived transistors has been determined and gave a glean of optimizing ZnO TFTs fabrication process.

Sol-gel derived ZnO TFTs always have a negative threshold voltage, while RF magnetron sputtered ZnO TFTs are usually normally off. Besides that, the field effect mobility of RF magnetron sputtered ZnO is also larger than that in sol-gel derived ZnO TFTs. With the limitation of p-type ZnO and ZnO TFTs stably produce, sol-gel derived and RF magnetron sputtered n-type ZnO are combined to fulfill the basic function of logic circuits.

Based on ZnO radiation-hard characteristics, gamma-ray irradiation effect has been investigated. After the different doses of radiation, ZnO TFTs survive but show various degradations. ZTO, which is a ZnO related material, was first carried out to overcome the low field-effect mobility of sol-gel derived ZnO TFTs. Compared to ZnO TFTs, ZTO TFTs with proper fabrication process demonstrate extremely high stability in gamma-ray irradiation.

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List of Abbreviations

a-IGZO amorphous-indium gallium zinc oxide

AFM atomic force microscopy

ALD atomic layer deposition

APCVD atmospheric pressure chemical vapor deposition

CAGR compound annual growth rate

CdS Cadmium sulfide

CdSe cadmium selenide

CdTe cadmium telluride

CMOS Complementary metaloxidesemiconductor

CV capacitancevoltage

CVD chemical vapor deposition

DC direct current

DC direct current

DOSs density of states

GaAs gallium arsenide

GaN gallium nitride

GaP gallium phosphide

Ge germanium

H_2O_2 hydrogen peroxide

HCL hydrogen chloride

InAs indium arsenide

InP indium phosphide

InSb indium antimonide

LEDs light-emitting diodes

MBE molecular beam epitaxy

MEA monoethanolamine

MESFET semiconductor field-effect transistor

MN Meyer-Neldel

MOCVD metal-organic chemical vapour deposition

NH_4OH ammonium hydroxide

PEALD plasma-enhanced atomic layer deposition

PECCS photo-excited trap-charge-collection spectroscop

PECVD plasma-enhanced chemical vapor deposition

PL photoluminescence

PLA Pulsed laser ablation

PLD pulsed laser deposition

RF radio frequency

RIE	reactive ion etch
SEM	scanning electron microscopy
Si	silicon
SiC	silicon carbide
SiN_x	silicon nitride
SiO_2	silicon dioxide
TFTs	thin film transistors
TGA	Thermogravimetric Analysis
WBG	wide band-gap
XRD	X-ray diffraction
ZnO	zinc oxide
ZTO	zinc tin oxide

Chapter 1

Introduction

Zinc Oxide (ZnO), which has a long usage history, can be recorded back to the Bronze Age. At that time, people mainly used ZnO as a salve and an alloying agent for metallurgy [1]. Over thousands of years, people kept putting great effort on ZnO to broaden the edge of human technology. Since last century, with the rapid development of semiconductor research and industry, ZnO and its alloys have drawn a significant attention due to its highly attractive characteristics.

The first ZnO electronic application was made in the 1920s [2], where ZnO was combined with a copper wire, and it served as a Schottky barrier to fulfill the rectification demand in the radio set. After that, electron diffraction experiment was performed and the data was collected about ZnO in 1935 [3]. In 1954, temperature dependent Hall measurement was carried out for ZnO and its intrinsic n-type characteristics were proven [4]. However, ZnO had not been widely used in electronic applications until 1968 when varistor was invented [5]. Later, internet boom started in 1987, which surged the research for ZnO usage [5]. Back to the early years of the 1990s, researchers began to investigate ZnOs capability in increasing the efficiency of ultraviolet light-emitting diodes (LEDs) [6]. In the 21st century, p-type ZnO, metallic doped ZnO, transparent ZnO electronics $et\ al.$ started attracting more and more interests [5]. Fig. 1.1 shows the trend of ZnO publications comparing with gallium nitride (GaN) and the whole modern nano-research. It is evident that over tens of thousands of articles related to ZnO and ZnO alloys have been published since the 1900s and the annual ZnO publications are still climbing in the 21st century, while the research of gallium nitride (GaN) reached a stable number of annual publications after 2005. Comparing to GaN, ZnO shows advantages of higher bulk quality, easier crystal-growth technology and lower cost for devices fabrication [7]. Even though, ZnO

just makes a little portion of the whole nano-research, it is still of great significance for research and industrial implementation.

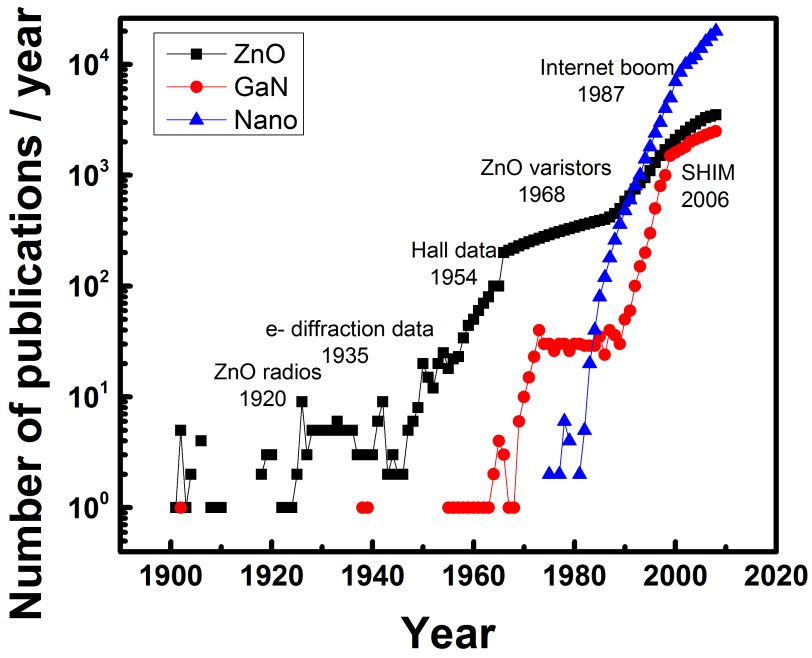

Figure 1.1: ZnO, GaN and nano materials publications trend with time changing [5].

It has been reported that global Nano ZnO market demanding an estimated $2,099 million in 2015 is anticipated to grow 20.4% compound annual growth rate (CAGR) and would be $7,677 million in 2022 [8]. Fig. 1.2 shows the tremendous growth of the main demand due to its climbing consumption in the rubber industry, pharmaceutical and cosmetic industries, textile industry, electronics and electrotechnology industries, photocatalysis and miscellaneous applications. ZnO electronics applications account for a large ratio among the whole ZnO market.

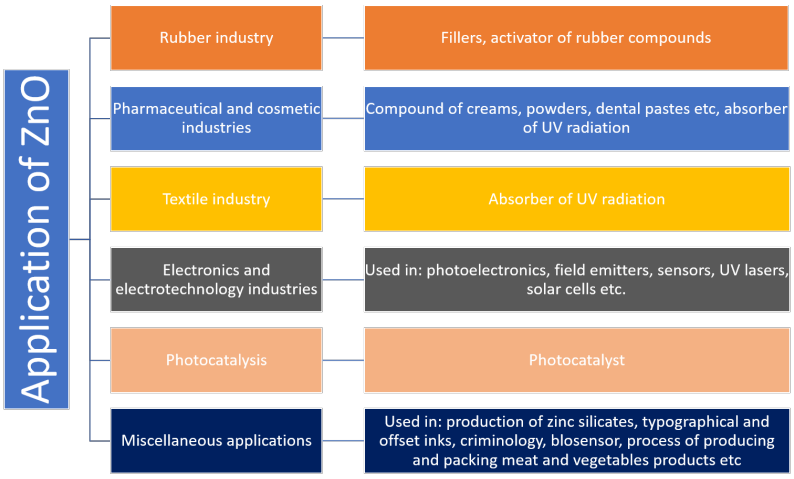

Figure 1.2: Applications of ZnO in industrial area.

Nowadays, both academic research and industrial demand drive ZnO electronics study to the further edge. Compared to well established but aged silicon (Si) technology, ZnO technology demonstrates some unique advantages. The significant properties of ZnO such as transparency [7], high energy radiation stability [9][10] and susceptibility to wet etching [11] make it worthy of formation investigation of transparent electronics, space electronics and small size devices. Meanwhile, low energy consumption fabrication, device defects investigation and harsh environment working performance research come well with ZnO devices study. Also, even though p-type ZnO attainment still remains an obstacle, the logic circuits fulfilled by using ZnO TFTs emerge diversely.

When this Ph.D. work started, making reliable devices was tempting for space exploration activities, nuclear power generation, and radiation-harsh environment rescue. Gamma-rays with the smallest wavelengths generated by radioactive atoms and in nuclear explosions have the most energy of any other wave in the electromagnetic spectrum. It can be chosen as the radiation source for material and device radiation tolerance testing. ZnO showing stability and reliability in Gamma-ray environment is attractive and seldom deeply explored by other groups. Since enormous temperature is another element following radiation in the radiation-harsh environment, it is worthy of characterizing ZnO devices under extreme temperature as well. Besides that, localized subgap defects for ZnO devices, especially sol-gel derived ZnO devices are still not clear.

In this Ph.D. work, ZnO material and devices reliability in Gamma-ray radiations and a cryogenic and relatively hot environment have been studied in detail. Defects of ZnO devices with various fabrication process have been investigated as well. As a supplement for ZnO related materials, zinc tin oxide (ZTO) has also been inspected. Below, properties of ZnO will be firstly introduced, then I will compare ZnO with other wide band-gap (WBG) materials and discuss the advantages of using ZnO for harsh environment applications. Then defects of ZnO and ZnO TFTs will be introduced. Following that, the basic logic circuit design for ZnO TFTs will be presented. After that, I will describe the methods for depositing ZnO. Finally, I will give an overview of the structure of my dissertation.

1.1 General ZnO properties

1.1.1 ZnO crystal structures

Zinc oxide (ZnO) is an II-VI compound that has three possible crystal structures: wurtzite structure, zinc blende structure and rock salt structure [2]. Specifically, ZnO shows crystallizing in the wurtzite structure at ambient pressure and temperature [7]. As shown in Fig. 1.3, Zn ion is located in a tetrahedral structure of O ions to form a hexagonal lattice. The wurtzite structure shows polar symmetry along the hexagonal. This kind of structure makes ZnO's unique properties, such as piezoelectricity, uninhibited polarization, easy crystallization and wet etching, meanwhile, also generating intrinsic defects [2].

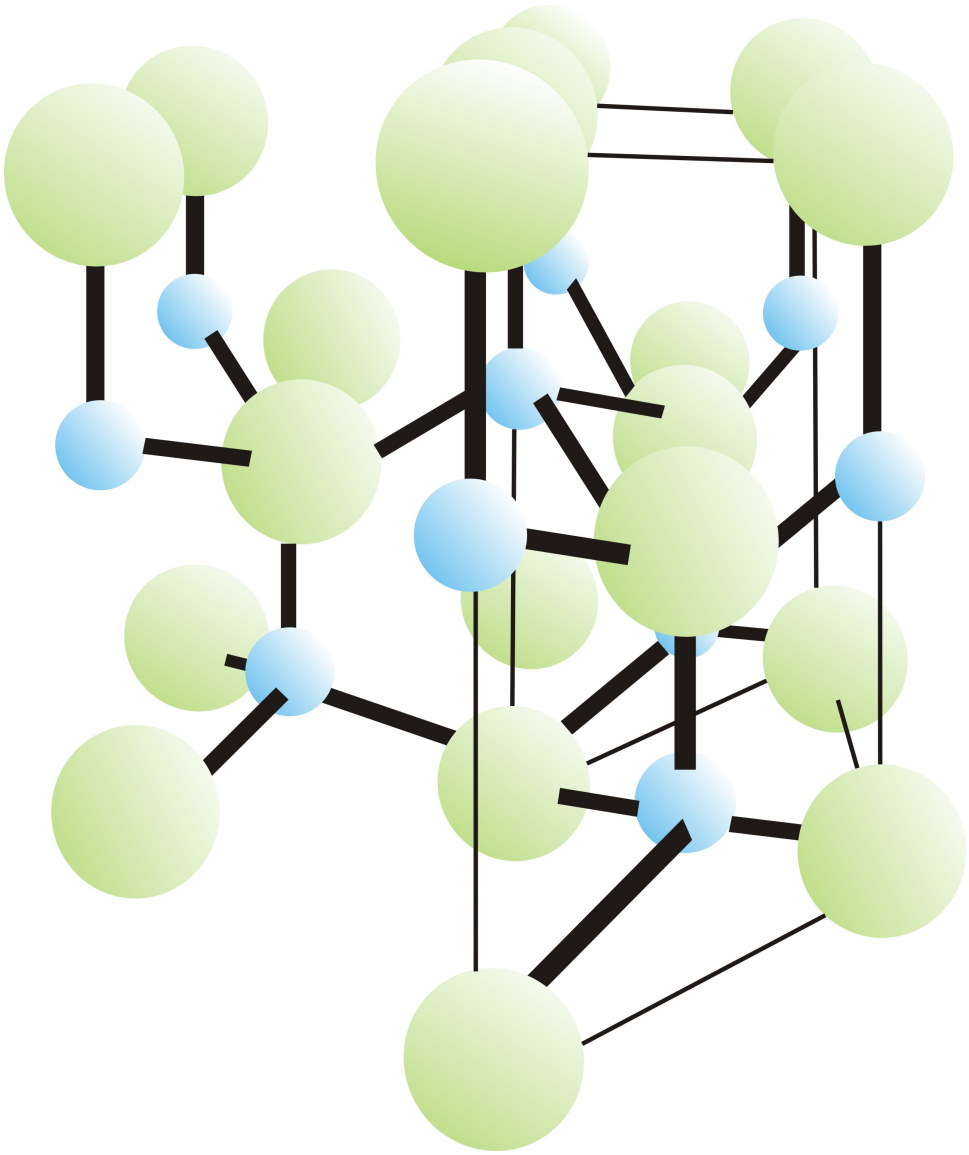

Figure 1.3: Schematic of ZnO wurtzite structure.

The other two ZnO structures: zinc blende structure and rock salt structure are displayed in Fig. 1.4. But, the zinc-blende ZnO structure (Fig. 1.4 (right)) is reported to only be obtained on the substrate of the corresponding crystal structures. Almamun Ashrafi A. B. M *et al.* have announced of growing zinc-blende ZnO films on gallium arsenide (GaAs) (001) [12]. Also, the formation of the rock salt structure needs static compression [13].

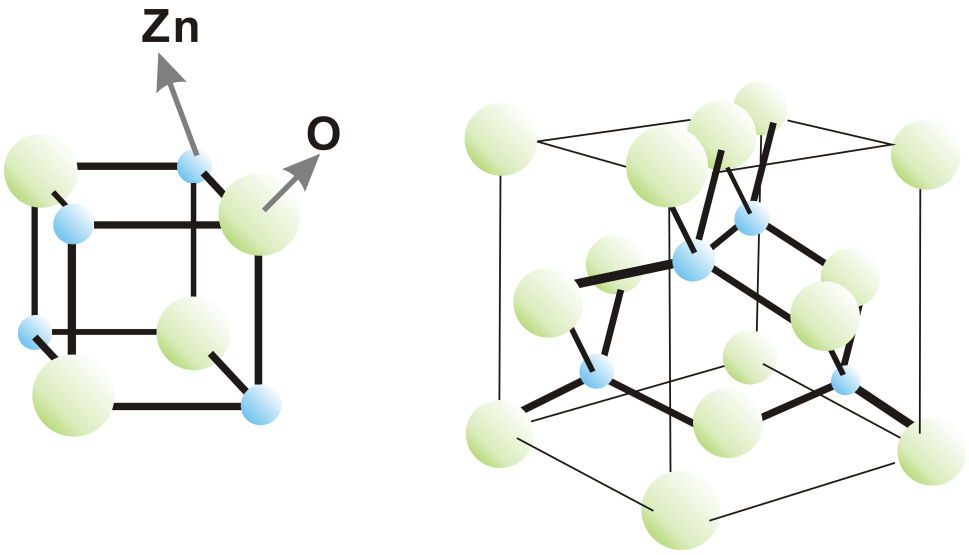

Figure 1.4: Schematic ZnO (left) rock salt structure and (right) blende structure.

1.1.2 Comparison of ZnO between conventional material based semiconductors and other wide bandgap semiconductors

ZnO is also a metal-oxide semiconductor with a wide and direct energy band-gap of 3.37 eV at room temperature [7]. The value of band-gap can be varied around 0.2 eV in different temperature and pressure [14]. As a wide band semiconductor, ZnO, GaN and silicon carbide (SiC) (with band-gap of 3.39 and 3.2 eV, separately) are considered as the 3rd generation semiconductors. On the other hand, Si is the 1st generation and GaAs and indium phosphide (InP) are the 2nd generation, respectively. However, the band-gap of Si (1.12 eV), GaAs (1.43 eV) and InP (1.35 eV) is not as wide compared to ZnO, GaN, and SiC. More detailed commonly used semiconductors band-gap can be seen in table 1.1 [15]. The band gap of a semiconductor is determined by the strength of the chemical bonds between the atoms in the lattice [15]. So the stronger the chemical bonds, the wider band gap, and more energy for an electron to escape from one site to another. Consequently, ZnO with wider band gap can be implemented in the electronics with lower intrinsic leakage currents and higher operating temperatures.

Material	Si	Ge	InSb	InAs	InP	GaP	GaAs	CdSe	CdTe	ZnO
Band gap energy (eV) at 0 K	1.17	0.74	0.23	0.43	1.42	2.32	1.52	1.84	1.61	3.44
Band gap energy (eV) at 300 K	1.11	0.66	0.17	0.36	1.27	2.25	1.43	1.74	1.44	3.2

Table 1.1: Commonly used semiconductor bandgap values at 0 K and 300 K, respectively.

Moreover, wider band gap energy can cause higher electrical breakdown field (E_C), which makes ZnO suitable for high supply voltage usage. Higher E_C also allows increase of the doping level. In other words, devices can be made thinner under a static E_C [16]. In RF application, ZnO with wider band gap can also ease impedance matching related to the higher voltage operation [17]. Table 1.2 has summarized the E_C of different commonly used semiconductors [18][19][20][21]. According to the results of S. Li *et al.* [18], there are three kinds of samples with three different levels of breakdown fields, which are (a) low breakdown field samples (L), (b) intermediate breakdown field sample (M) and high breakdown field sample (H). In order to make the comparison more comprehensive and more persuasive, table 1.2 includes all three types of ZnO E_C. It can be seen that ZnO (M and H) has higher E_C than the commonly used Si and GaAs. But it has lower E_C than the other WBG semiconductors. However, ZnO has some other advantages exceeding them and will be described in the next section.

Semiconductor	ZnO (L)	ZnO (M)	ZnO (H)	GaN	SiC	Diamond	Si	GaAs
E_C (MV/cm)	0.33	1.1	1.8	3	3	10	0.3	0.3

Table 1.2: Commonly used semiconductor breakdown field.

Furthermore, ZnO is also promising to be treated as UV-light emitter based on its large exciton binding energy (60 meV) [22]. Even though no natural p-type ZnO hampered ZnO UV LED marketing, more and more techniques, such as ZnO on p-$SrCu_2O_2$ [23], p-GaN [22] and p-AlGaN [24][25] have been investigated and used for solving this problem. J. H. Lim *et al.* have even claimed using doped p-type ZnO to form the p-n junction ZnO LED [26]. Table

1.3 shows the recent advances of ZnO based heterojunction LEDs [27]. And there are also numerous LEDs with ZnO nanostructures according to the survey of Y. S. Choi $et\ al.$ [27]. But for the pages limitation, they are not listed here.

Structure	Growth method	Emission color (nm)
n-ZnO/p-GaN	PLD	UV (375)
n-ZnO/p-GaN	MOCVD	Blue-violet (415))
n-ZnO/p-AlGaN	CVD	UV(385)
n-ZnO/n-MgZnO/ n-CdZnO/p-MgZnO	MOCVD	Blue, red
n-MgZnO/n-ZnO/ p-AlGaN/p-GaN	MBE	UV
n-MgZnO/CdZnO/ P-GaN	MBE	UV
p-ZnO/n-Si	MBE	UV (381) visible (485, 612,671)
p-ZnO/n-GaN	Rf-magnetro n sputtering	Blue-violet (409)
n-ZnO/p-GaN, n-ZnO/n-MgZnO/ n-ZnO/p-GaN	MBE	UV (375) visivle (415, 525)
n-ZnO/p-Si	MOCVD	Visible (580)
n-ZnO/u-ZnO/ p-Si	Magnetron sputtering	Visible (500-650)
p-$SrCu_2O_2$/n-ZnO/ ITO/YSZ	PLD	UV (382)
n-ZnO/p-GaN/ Al_2O_3	CVD	Blue (430)
n-ZnO/u-ZnO/ p-$CuGaS_2$/n-GaP	Helicon-wave-excited -plasma sputtering	Greenish-white
p-$CuGaS_2$/n-ZnO:Al	Helicon-wave-excited -plasma sputtering	IR (780)

Table 1.3: Structure, method and emission color for recent ZnO based heterojunction LEDs.

Compared to conventional materials, Si and GaAs, ZnO with wide band-gap energy has the potential to fit for electronics with smaller, more efficient benefits in high power and high-temperature electronics, RF applications and the optoelectronics and lighting industries [17].

Compared to GaN and SiC, which are also WBG materials, ZnO also shows advantages. The free-exciton binding energy in ZnO, GaN and SiC are 60, 25 and 27 meV, respectively [28][29][30]. This makes excitonic emission of ZnO at room and higher temperatures possible. Arabshahi reported that ZnO MESFETs also show better frequency response characteristics than SiC MESFETs [31].

1.1.3 ZnO implementation in radiation-harsh environment

Human space exploration has been carried out since the early 20th century. Because of the long time exposures, inevitable solar proton activities and also galactic cosmic ray irradiation, spacecraft have been suffering from power resets, safing, system failures $et\ al.$ For example, during the October and November in 2003, many spacecrafts experienced high systems data errors, increased noise in instruments and device failures [32]. Similar scenarios happened, where the sensors and control circuit can be affected when people are building nuclear power plants, where gamma-ray radiation and neutron radiation can be generated by nuclear reactors [33]. Moreover, the radiation harsh environment intentionally or unintentionally is created by human. For example, the place after nuclear explosions and nuclear power plant leakage can also produce different kinds of radiation rays that do harm on the functional electronics.

There are three main approaches that can be carried out to prevent electronic systems from damaging in the radiation harsh environment: (a) shielding the vital parts of electronics [34], (b) commercial parts in in excess and duplicative configurations, (c) radiation-hard material employed for making radiation-hard electronics. The first approach can protect the systems firmly. However, it can make the whole configurations larger and heavier and sometimes even cannot even be realized when there are space limitations. Besides these, the shield itself will also increase cost. The second approach is theoretically working, but it multiplies the cost and most time it is inoperable. For instance, the whole weight of the spacecraft should be light for fuel saving and cannot hold two identical configurations. Finally, the third one is practical,

which has low cost and high compactness compared to the other two approaches and can make electronics and systems resistant to both the particle radiation and electromagnetic radiation.

ZnO as one of the WBG material can be considered as a candidate for electronics and optoelectronics in a radiation harsh environment. The chemical bonds in conventional covalent semiconductors, such as Si, Cds and GaAs show intensely direct p or sp3 orbitals. It is easy for outside radiation to disorder the angle and the length of the bond and as a result, introduce localized defects [35]. In contrast, ZnO, as a post-transition metal oxide, has a strong ionic chemical bond and energy states close to the conduction band minimum mainly come from cation (Zn) -orbitals [36]. Consequently, the radiation effect cannot easily affect both bond angle and length disordering [37]. Comparing Tuomisto, F. $et\ al.$'s and Saarinen, K. $et\ al.$'s results, the introduction rate of the Zn vacancies shows 30 times lower than Ga vacancies in GaN [38][39]. It is recognized that ZnO is more radiation resistant than other semiconductor materials such as Si, Cadmium sulphide (CdS), GaAs, and even GaN [9][39].

Previously, ZnO deposited by different techniques was irradiated by protons [40] [41], electrons [42], ions [43], neutrons [44], and gamma-ray [35][36], and its radiation hardness was investigated. Table 1.4 summarizes the relative references related to the results of ZnO radiation hardness investigation.

Deposition methods	Device type	Radiation source	Radiation amount	Analysis	reference
NA	Schottky diodes	Protons	40 MeV	Current decrease	[40]
vapour-phase grown ZnO	Single-crystal	Protons	1.8 MeV	Defects introduction	[41]
vapour-phase grown	Bulk ZnO crystals	electrons	2 MeV	Defects introduction	[42]
MOCVD	Bulk ZnO layers	X^{e23+} ions	130 MeV	Defects introduction	[43]
PEALD	ZnO TFTs	Gamma-ray	1 MRad	Negative threshold voltage shift	[35]
PEALD /PLD	ZnO TFTs	Gamma-ray	100 MRad	Threshold voltage shift	[36]

Table 1.4: ZnO radiation hardness summary.

According to the summary, the radiation-hard characteristics attracted number of studies. Both single ZnO crystal and bulk ZnO and ZnO TFTs have been investigated under all kinds of radiations. However, no group has ever examined the gamma-ray irradiation effect on sol-gel derived ZnO TFTs. Since this technique of depositing ZnO is well established and widely used, it is worthy of studying the resistance to the gamma ray irradiation. Additionally, the sol-gel derived ZnO deposition method will be described in the following section.

1.1.4 ZnO defects and extraction techniques

ZnO is a natural n-type semiconductor and the reason for the n-type formation is widely studied and mostly attributed to ZnO intrinsic defects [4][45][46][47][48] and extrinsic defects (impurities) [49][50]. The intrinsic defects represent the imperfect parts in ZnO crystal lattice which only involves Zn and O elements. There are main types of intrinsic defects in ZnO and the idealized schematic structures: (a) oxygen vacancies, (b) oxygen interstitials, (c) zinc vacancies and (d) zinc interstitials [51]. And the defects also show neutral, singly charged and doubly charged states. Besides intrinsic defects, the extrinsic defects (or impurities) usually act as dopants and can be treated as donors or acceptors to change the carrier concentration in ZnO. Common impurities have been summarized and listed in table 1.5 as below.

Impurity	Character	Ionization energy	nmax or pmax (cm^{-3})
Al	Donor	120 meV	8×10^{20}
Ga	Donor	NA	1.1×10^{20}
In	Donor	NA	NA
F	Donor	80 meV	5×10^{20}
H	Donor	35 meV	NA
Li	Acceptor	NA	NA
Cu	Acceptor	NA	NA
N	Acceptor	100 meV	9×10^{16}

Table 1.5: Summary of common extrinsic defects (impurities) [52], The nmax or pmax demonstrate the date of the highest carrier concentration experimentally extracted by Janotti $et\ al.$ [53].

For ZnO TFTs, defects locating at the interface between ZnO and dielectric layer also have a significant effect on the performance of ZnO TFTs. Both intrinsic and extrinsic defects and interfacial defects can always be electrically active and will generate plenty of levels in ZnO band gap, which cause the transitions happen between different energy states.

Considering ZnO as a channel for ZnO thin film transistors (TFTs) fabrication, the defect of ZnO has a great effect on the TFTs electrical performance. It is worthy of studying the number and the influence of the defects in working ZnO TFTs. One of the common methods is to determine the subgap density of defects states or so-called DOSs, from which a valuable insight on various intrinsic electrical properties of the ZnO TFTs, such as the field effect mobility, the threshold voltage, and the subthreshold swing etc. can be gleaned. There exist many methods for studying sub-gap DOS distribution; photoluminescence (PL) [54][55], photo-excited trap-charge-collection spectroscopy (PECCS) [56], capacitancevoltage (CV) measurement [57] and temperature-dependent field effect measurement [58][59][60][61]. The CV measurement, PECCS, and temperature-dependent field effect techniques have been commonly used for probing traps in field-effect transistors. PL method is a straight forward technique to investigate defects in a semiconductor. However, it cannot be implemented on a working transistor [62][55].

Until recently, only a handful of research has been carried out on the determination of sub-gap DOS of ZnO. Lee $et\ al.$ [56] demonstrated the determination of DOS using photo-excited trap-charge-collection spectroscopy (PECCS) from the RF magnetron sputtered ZnO TFTs, where the DOSs information was collected by measuring the threshold voltage shift in the photo-electric experiment. Kimura $et\ al.$ [57] provided CV characterization for trap densities extraction for RF magnetron sputtered ZnO TFTs by using Poisson equation and carrier density equation. However, no study has been performed on the determination of sub-gap DOSs for sol-gel derived ZnO TFTs. Therefore, in this investigation, temperature dependent field effect measurement based on the Meyer-Neldel (MN) rule was applied to extract the DOSs of sol-gel derived ZnO TFTs with different annealing temperatures. This technique has been successfully applied to a-IGZO [58][59][60][61], ZTO [63] and Cu_2O [64]. However, it has never been adopted for the study of the sol-gel derived ZnO TFTs. Compared to other methods, the temperature-dependent measurement is advantageous since it was carried out in a vacuum, eliminating the effect of oxygen and water traps in the atmosphere and providing a more accurate insight on the sub-gap trap density. In this Ph.D. work, I use temperature dependent field effect measurement not only to verify the efficacy of this technique on sol-gel derived

ZnO TFTs, but also to investigate the annealing temperature effect on the evolution of sub-gab DOSs.

1.1.5 ZnO basic logic circuit design

So far, p-type ZnO still is a big obstacle for ZnO circuits development and industrial use. Even though a lot of progress has been made under various doping method, a reliable and repeatable p-type ZnO with high quality is still not achieved. There are plenty of reasons for this difficulty. One main reason could be the ZnO intrinsic defects that can neutralize the dopants [54]. Another reason might be that the dopants cannot be dissolved well in ZnO [65].

However, there are still lots of research on achieving the ZnO circuits. Mourey $et\ al.$ built hybrid organic-inorganic (ZnO/organic) CMOS integrated circuits [66]. Chiu $et\ al.$ tried p-type/n-type metal oxide semiconductors (SnO/ZnO) to make complementary circuits [67]. Lee $et\ al.$ use top-gate electrodes with different work functions to realize ZnO transistors with different threshold voltages, respectively, then applied for pseudo-nMOS inverter circuit [68].

A simple inverter can be realized by two kinds of TFTs which have threshold voltage difference. Figure 1.5 shows the schematic inverter by using pure n-type TFTs with threshold voltage difference.

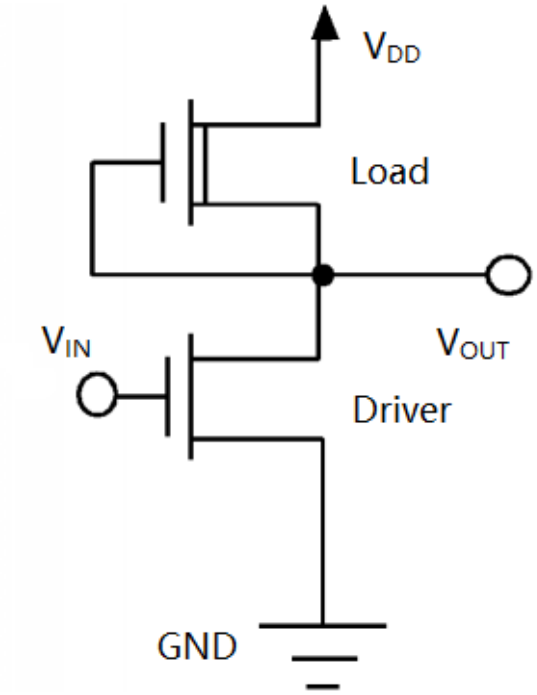

Figure 1.5: Schematic of nMOS inverter implemented by n-type TFTs with threshold voltage difference.

The upper transistor is the in depletion mode and always be turned on. It can be treated as a resistor. The bottom transistor is in the enhancement mode and can only be turned on when V_{in} is larger than a positive threshold voltage. Even though it is more power consuming compared to CMOS, it still can realize the basic function of a logic circuit.

In this Ph.D. work, ZnO TFTs in enhancement mode and depletion mode are achieved by using different deposition techniques and will be introduced and described in detail in later sections.

1.2 ZnO deposition methods

For the last twenty decades, numerous methods have been carried out for ZnO film deposition. The most widely used and significant techniques can be categorized as chemical vapor deposition (CVD), direct current (DC) or RF magnetron sputtering, plating molecular beam epitaxy (MBE), laser ablation and sol-gel deposition.

MOCVD was applied for ZnO deposition by Gorla $et\ al.$ in 1998 [69]. After that plasma-enhanced chemical vapor deposition (PECVD) [70], low pressure chemical vapor deposition

(LPCVD) [71] and atmospheric pressure chemical vapor deposition (APCVD) [72] have also been used for the growth of ZnO. There are plenty of advantages of CVD, such as forming elaborate shape, high purity and not restricted to high vacuum [73]. Also, it comes with disadvantages as well. For instance, the precursors are usually toxic (Dimethylzinc) [74], combustible (Diethylzinc) [71] and quite expensive [73].

ZnO can also be deposited by atomic layer deposition (ALD), which can be treated as a special modification of CVD technology [75]. Compared to traditional CVD and magnetron sputtering, ALD provides obvious benefits. It makes low-temperature deposition possible and generates high density film with no pinholes. Also, it has excellent step coverage and reproducibility and is easy to scale up. Besides that, the shortcoming is the expensive equipment and also the adjustment of the flow is critical. In other word, too much flow can cause clogging of valves but the too low flow will lead to under-performance.

DC magnetron sputtering for doped ZnO [76] and RF magnetron sputtering for pure ZnO [77] has been considered and implemented as another method for ZnO thin film deposition. Because of the low plasma density, the adhesion of the coating and the density of the sputtered ZnO layers are low. Magnetron sputtering can provide the layer with excellent uniformity and also some unique usage in ZnO application and will be talked in the later section.

Zu $et\ al.$, Bagnall $et\ al.$, and Ohgaki $et\ al.$ [78][29][79] have also demonstrated molecular beam epitaxy (MBE) for ZnO deposition. Just as CVD and ALD, MBE is also excellent for forming low defects and highly uniform film, and also provides extremely thin and precise film. Besides those, the crystal growth rate is very low (a few microns per hour) and needs a lot of effort to set up. The system involved is also complicated and highly cost [80].

Pulsed laser ablation (PLA)) is another unique technique for high quality c-axis oriented ZnO [81][82]. And it also has the shortcoming, such as high energy consumption and system complexity.

At last, the sol-gel method as a well-established has also been used for ZnO film deposition [83][84]. Compared to other deposition techniques, sol-gel is simple, economical and efficient. It can produce large area and highly pure products. Due to financial and system set up consideration, we also use this method for ZnO TFTs fabrication.

1.2.1 Sol-gel spin coat technique

Sol-gel technique is widely used and easily set up approach to make semiconductor materials. Researchers can achieve different composition and structures of semiconductors in nanometer scale by changing the concertation between metal salts and solvent and the process of formation. Specifically speaking, solid metal salts dissolved in the solvent and the particles form a colloidal suspension is called a sol process [85]. After that, a sol can be applied for dip-coating or spin-coating to generate thin films. The sol itself can gradually change from pure liquid to gel, which contains both liquid and solid phase [86]. Under the variable process of sol-gel, films, fibers, powders, ceramics or glass-like forms can be produced.

The starting compounds for sol preparation are called precursors consisting of metallic elements and the corresponding ligands. Besides the metallic elements, various kinds of ligands that usually can be categorized as Alkyl, Alkoxy, acetylacetonate, and acetate. An alkyl ligand is an alkane without one hydrogen, where an alkane is only carbon and hydrogen connected by single bonds [85]. On the other hand, an alkoxy ligand is an alcohol molecule without a proton on the hydroxyl (OH), where an alcohol is formed by combining a OH with an alkyl molecule or something else [85]. Acetylacetone is a bidentate ligand (table 1.6) and acetate anion is formed by removing one proton from acetate acid.

In our work, we chose zinc acetate dehydrate ($Zn(CH3COO)_2 2H_2O$) and isopropanol (C_3H_7OH) as the precursor and the solvent, respectively. After zinc acetate dehydrate was added into isopropanol, there will be a reaction as the following equation:

The zinc acetate dehydrate then will become mono-acetate [87][88][89]. After that monoethanolamine (MEA) will be added and the molar ratio between zinc and MEA is 1:1. The MEA works as a complexing agent to stabilize the solution from Zn condensation [89]. The reaction function between mono-acetate and MEA can be written as below:

The next step is the spin-coating. The first step is to locate a substrate (usually an oxidized silicon wafer or a glass wafer) on a spin-coater, the substrate should be stained tight. Then a small amount of sol will be dropped or poured on the center of the substrate, while the substrate is either rotated slowly or not rotated at all. After that, the substrate is set to spin at high speed

for a specific time so as to make sure the coating sol spread the whole substrate by centrifugal force [90]. Finally, the spin-coated thin film is always been calcinated on a hot plate for several minutes to evaporate the organic materials. By using spin coating, a very uniform films from nanometers to microns can be quickly and easily generated. The whole process is shown in Fig. 1.6 below and a uniform thin film will be produced.

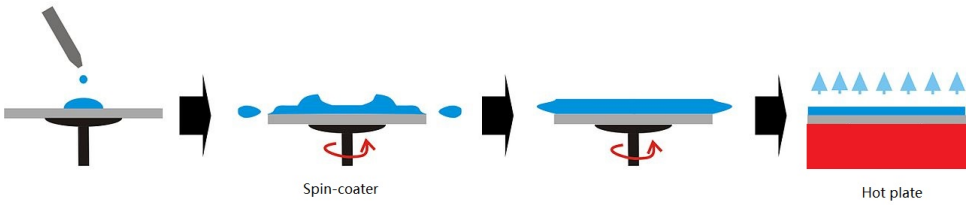

Figure 1.6: Spin-coating process [90].

1.2.2 Radio frequency magnetron sputtering technique

The second technique was carried out on doing the ZnO deposition is RF magnetron sputtering. Magnetron sputtering systems can be categorized as the devices using cold cathode (or target) to discharge for depositing. The systems can generate the plasma between the anode and cathode in either DC or RF mode. Usually, the pressures for sputtering is as low as in the mTorr range and the power is high. The atoms will be bombarded by the high power going through the target can then condense on a substrate and form a thin-film. The substrate usually directly faces to the target to make the formed film uniform [91].

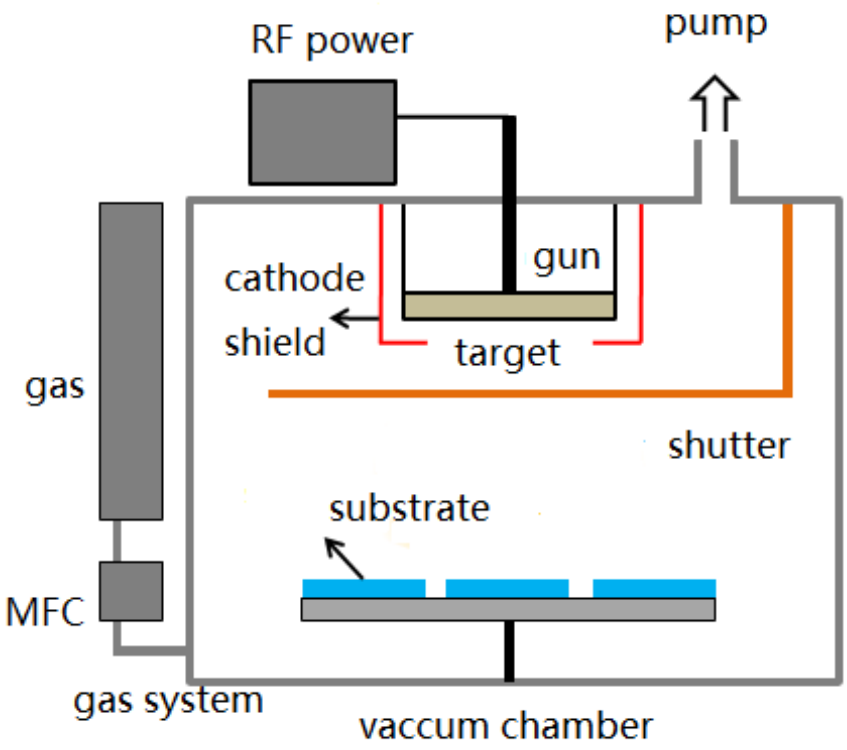

Figure 1.7: Schematic of RF magnetron sputter system [92].

Fig. 1.7 shows the basic function of RF magnetron sputter system. There are different usage between DC and RF magnetron sputtering. The use of DC magnetron sputtering requires electrically conductive electrodes. When dielectric films are directly deposited by using one or both non-conductive electrodes, the dielectric films would gradually cover the electrodes and interrupt the discharge. On the contrary, in the usage of the radio frequency power, positive charges accumulation in one period can be eliminated by electron bombardment in the next period. Since the conductivity of ZnO target is low, it is a better choice to use RF instead of DC magnetron sputtering for ZnO thin film deposition.

Sol-gel derived ZnO can fulfill most quests for this Ph.D. work, RF magnetron sputtering still provide ZnO with some unique characteristics for ZnO TFTs performance. Table 1.7 lists the threshold voltage (V_T) for RF magnetron sputtered ZnO TFTs found in the references. It can be seen that the RF magnetron sputtered ZnO TFTs are almost natural in the enhancement mode ($V_T > 0$ V), while the process we used for fabricating sol-gel derived ZnO TFTs have normally on threshold voltage ($V_T < 0$ V). The threshold voltage difference between these two

methods deposited ZnO TFTs make basic logic circuit implementation possible. So we chose both techniques for ZnO deposition. The logic circuit implementation part will be discussed in the later section.

RF magnetron sputtered ZnO TFTs	V_T
[93]	19 V
[94]	15 V
[95]	9 V
[96]	0.45 V
[97]	2.5 V
[98]	6.5 V
[99]	10 V
[100]	10 V
[101]	3 V

Table 1.6: Summary for RF magnetron sputtered ZnO TFTs.

1.3 Unique contributions

In this research, the unique contributions can be listed as follows:

1) Gamma-ray irradiation effect on ZnO TFTs was investigated.

2) ZnO TFTs were characterized at cryogenic temperature.

3) DOSs distributions for sol-gel derived ZnO TFTs were extracted via temperature-dependent IV measurement.

4) The optimal annealing temperature for sol-gel derived ZnO TFTs was determined.

5) Basic logic circuits based on ZnO TFTs were designed and achieved.

6) ZTO TFTs' radiation-hard characteristics were studied and the reliable and stable radiation-hard ZTO TFTs were produced.

1.4 Organization of the dissertation

This dissertation mainly focuses on the investigation of ZnO TFTs radiation-hard characteristics and localized subgap density of states and is organized as follow:

Chapter 2: Fabrication and measuring process.

Chapter 3: Gamma-ray irradiation and low-temperature effect on ZnO TFTs.

Chapter 4: Localized subgap density of states of sol-gel derived ZnO TFTs extraction.

Chapter 5: ZnO based logic circuits fabrication and testing.

Chapter 6: ZTO TFTs characterization and radiation-had study.

Finally, chapter 7 summarizes this work, draws conclusions from the ZnO project, and sets an outlook for future research.

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Chapter 2

Fabrication and measurement process

2.1 Introduction

Thin film deposition technology has been widely developed since the 20th century, a large number of its applications have been carried out in areas such as magnetic recording media, electronic semiconductor devices, LEDs, optical coatings, hard coatings, thin film solar cells and thin film batteries [1]. Specifically to thin film transistor (TFT), it shows merits of large-area fabrication, low cost, substrate flexibility and the ability to form any kind of electronic circuits comparing with conventional bulk-Si transistors [2].

ZnO and ZTO thin film and their transistors have also shown great attractions based on their transparent optical property, wide bandgap physical and electrical property as introduced in chapter 1.

In this chapter, the process of ZnO/ZTO thin film, thin film bottom gate transistors and logic circuits fabrication techniques will be introduced. After that, the corresponding thin film, TFTs and logic circuits characterization process will also be described.

2.2 Fabrication

2.2.1 Bottom gate TFTs

Before depositing ZnO/ZTO thin-film, an oxidized silicon substrate should be prepared. In our whole research experiences, two methods have been carried out: 1). Purchasing oxidized silicon wafers from University Wafers inc. 2). Thermal oxidizing pure silicon wafers.

The first method is convenient and the oxidized layer thickness is very accurate and consistent. But the price for oxidized wafers is too high and fabrication time is too long. As a result, the second method has always been preferred.

Before a highly doped p-type silicon wafer is thermally oxidized to form a silicon dioxide dielectric layer, the RCA-1 and RCA-2 silicon wafer cleaning processes were applied for cleaning silicon wafers, respectively [3] [4]. For RCA-1, the solution was made by ammonium hydroxide (NH_4OH), hydrogen peroxide (H_2O_2) and DI water. The silicon wafer was soaked for 15 minutes to remove organic residues. For RCA-2, hydrogen chloride (HCl), H_2O_2 and DI water were added sequentially at a ratio of 1:1:6 in beaker and then heated to 70 deg. C The unoxidized silicon wafers were dipped into the warm solution for 10 minutes to remove metal ions.

After the cleaning process, the thermal oxidization was carried out in the Thermal Oxidation Furnace System. Two types of thermal oxidation processes (dry oxidation and wet oxidation) can be used in the furnace. Dry oxidation which can form better quality and wet oxidation which has faster a growth and a reaction formula as follows;

The oxidant flow for dry and wet oxidization is also different. For dry oxidization, only oxygen flow is used. For wet oxidization, oxygen and hydrogen are flowing together and reacting to generate water vapor. The oxidation kinetics process is shown in Fig. 2.1

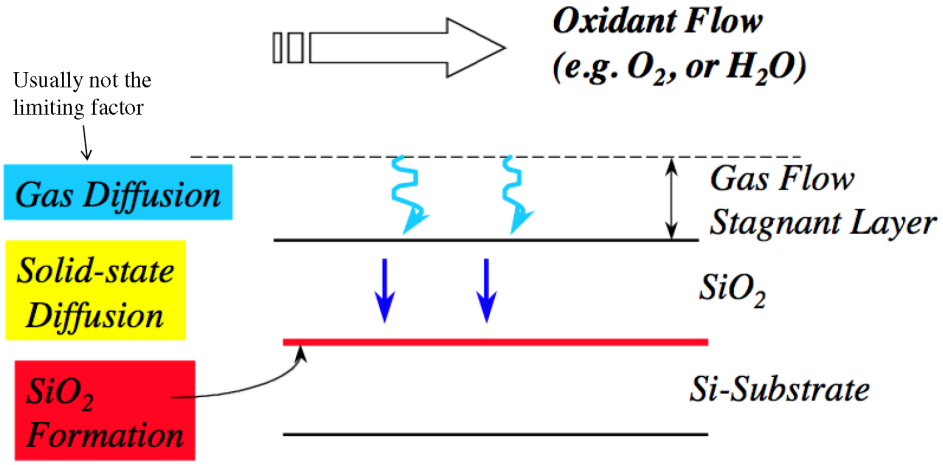


Figure 2.1: Oxidation kinetics process.

In our case, SiO_2 was used for the dielectric layer in ZnO TFTs, so dry oxidization was applied for produce high quality of SiO_2. The oxidation was set at 1050 °C for 2 hours. The oxidation thickness was 170 nm. Compared to CVD method, thermal oxidization is convenient, cheap and can form a dense thin film, which has a higher breakdown voltage and lower leakage current. However, the disadvantage of this technique is that it is difficult to be implemented on patterned gate thin film transistor. And this will be discussed later.

For the ZnO and ZTO thin film depositions, we used two methods: solution spin-coat and radio frequency (RF) magnetron sputtering.

The solution spin-coat process can be described as follows; For ZnO thin film deposition, the sol-gel precursor solution was prepared by dissolving zinc acetate dihydrate in monoethanolamine (MEA) and isopropanol with 1:1 molar ratio of Zn:MEA. For ZTO thin film deposition, the sol-gel precursor solution was prepared by dissolving zinc acetate dihydrate and tin chloride in 2-methoxtethanol with a constant Zn : Sn ratio of 7:3. Two different precursor concentrations were made as 0.05 M and 0.2 M, respectively. After that, the precursor solution was spin-coated on oxidized Si wafer at 3000 rpm for 30 seconds and then the wafers were calcined at 285 °C for 5 minutes. Fig. 2.2 and 2.3 show photos of spin-coater and hot plate, separately. Based on the thin-film thickness we wanted, the process (spin coating followed by calcination) was repeated from one to sixteen times. Subsequently, the coated wafer was diced into several individual pieces and annealed in the KSL-1100X furnace (Fig. 2.4) at various temperatures for one or more hours.

Figure 2.2: VTC-50 spin-coater.

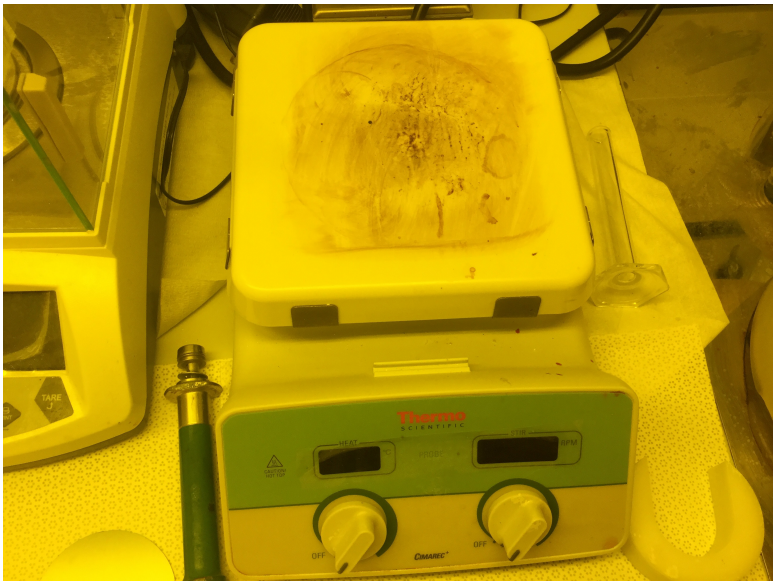


Figure 2.3: Hotplate.

Figure 2.4: Annealing furnace KSL-1100X.

RF magnetron sputtering was also used to deposit ZnO thin film. The RF sputtering system is shown in Fig. 2.5. 99.9% purity of ZnO target was set in the chamber and the chamber was pumped to vacuum. When the pressure was under 1.5×10^{-5} Pa, Pre-sputtering with shutter closed is used to remove impurity from the ZnO target (Fig. 2.6). Deposition starts when the shutter is open (Fig. 2.7). The parameters are summarized in table 2.1.

Target Material	ZnO (99.9% purity)
Pre-sputtering power (W)	160
Sputtering power (W)	160
Sputtering time (sec)	1200; 5400
Gas 1 (Ar) flow rate (sccm)	25
Gas 2 (O2/N2) flow rate (sccm)	1
Substrate heating	No intentional heating
Deposition pressure (mTorr)	50
Substrate	Thermally oxidized p-type silicon wafer
Estimated film thickness (nm)	70; 200

Table 2.1: RF magnetron sputtered ZnO recipe.

Figure 2.5: RF magnetron sputtering system.

Figure 2.6: Presputtering.

Figure 2.7: Sputtering.

The ZnO coated wafer is also diced into several individual pieces and annealed in the KSL-1100X furnace (Fig 2.4) at various temperatures for one or more hours.

After ZnO/ZTO coated on wafers, photolithography is done to pattern source and drain contacts. We used 5214 E positive photoresist (PR) and spin coat (Fig. 2.8) at 3000 rpm for 30 seconds. Then the wafers were soft baked at 100 °C for 1 min in the furnace (Fig. 2.9) and exposed to UV light for 35 sec. by using a mask aligner (Fig. 2.10). A metal contact layer was deposited by direct-current (DC) magnetron sputtering (Fig. 2.11) to form source and drain ohmic contacts. Device isolation was achieved by forming a mesa structure via a wet-chemical etching of the ZnO active layer (same as patterning ZTO), which need another photolithography and resulted in the reduction of the gate leakage current by more than four orders of magnitude. The length (L) and width (W) of the transistor channel were 80 and 1005 m, respectively, which corresponds to W/L ratio of 12.56. The bottom of each sample was lightly scratched to remove

the unwanted oxidized layer of the Si wafer and Ag paint was applied to attach to a copper or gold tape, serving as the bottom gate. A 2D cross-section of the finished device structure is shown in Fig. 2.12 and a surface picture from the top of the transistor under the microscope can be seen in Fig. 2.13.

Figure 2.8: Spinner.

Figure 2.9: Soft bake oven.

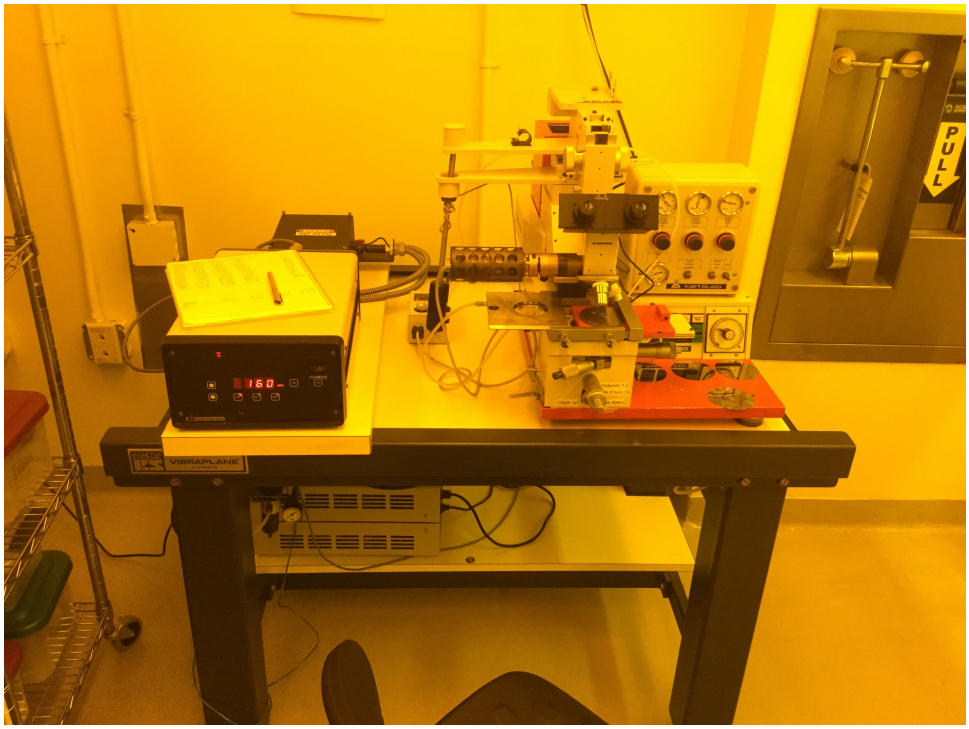


Figure 2.10: Mark aligner.

Figure 2.11: Direct current (DC) magnetron sputtering system.

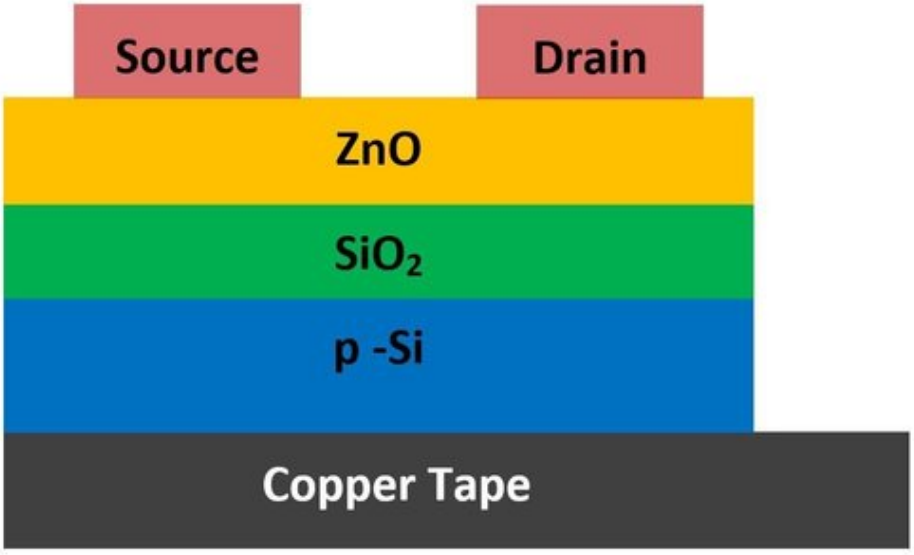


Figure 2.12: Schematic 2D cross-section of bottom gate ZnO TFT.

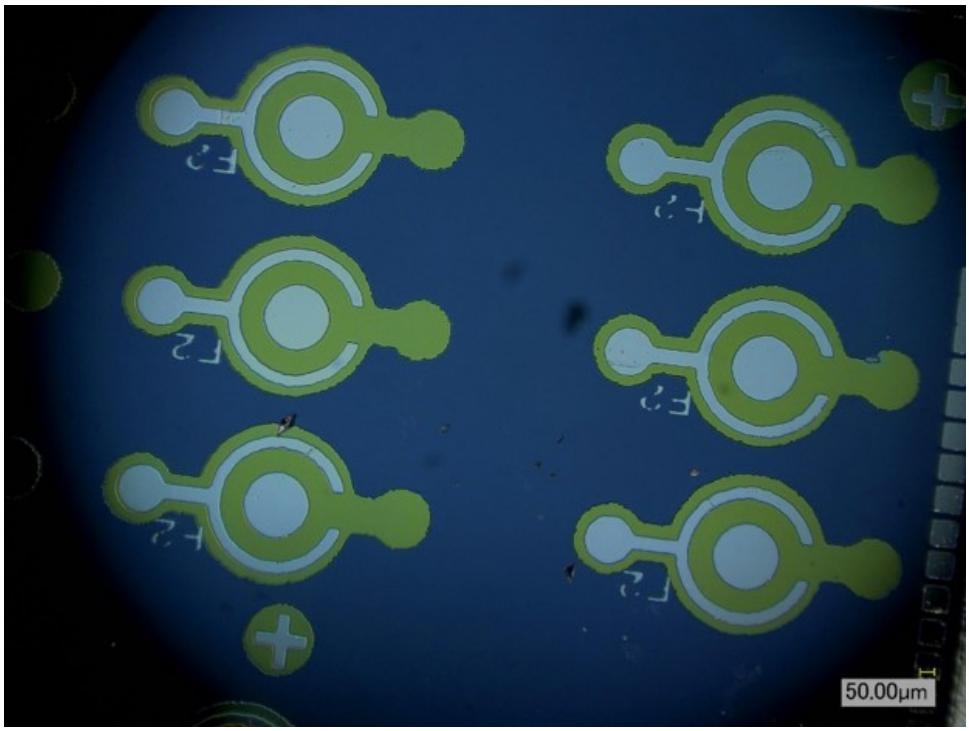
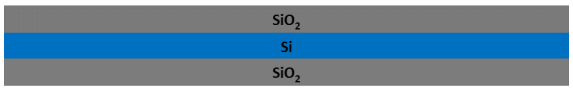


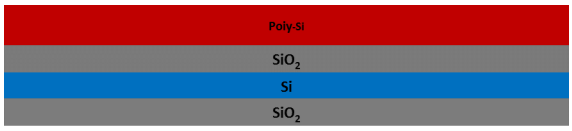
Figure 2.13: Optical microscopic image of bottom gate ZnO TFTs.

2.2.2 Patterned gate ZnO TFTs and the related logic circuits

Even though the bottom gated ZnO TFT has many merits, such as simple process, cheap equipment involved and low gate current leakage, the unpatterned gate still limit its application in building circuits. Wire bonding discrete devices has been used but is labor intensive and is not adapted to miniaturization. Patterned gate ZnO TFTs can avoid this kind of problem and make ZnO integrated circuits possible. Two types of patterned gate ZnO TFTs (bottom patterned gate ZnO TFTs and top patterned gate ZnO TFTs) and the related logic circuits fabrication will be discussed in this section.

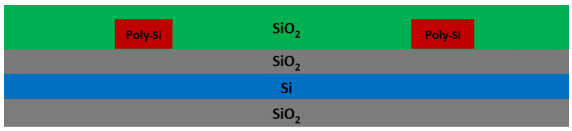


(a) Oxidized wafer prepared.

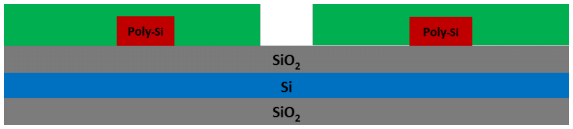


(b) Poly silicon deposited and phosphorus doped (diffusing).

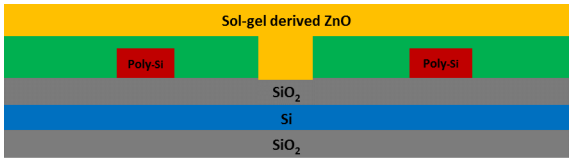
(c) Photolithography for patterning the gate layer and reactive-ion etch (RIE) to etch the rest of parts.



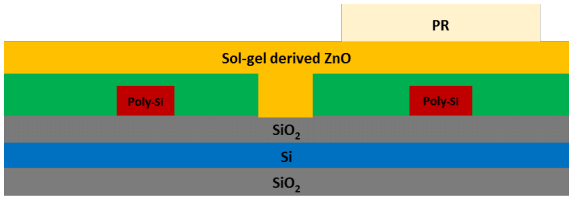
(d) LPCVD + annealing = dielectric layer.



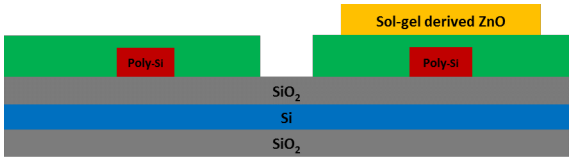
(e) Wet etch to pattern dielectric layer and make gate pad expose.



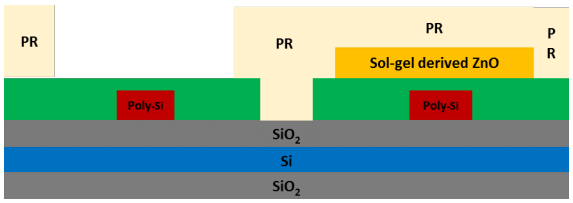
(f) Spin-coat sol-gel derived ZnO layer, anneal for one hour.



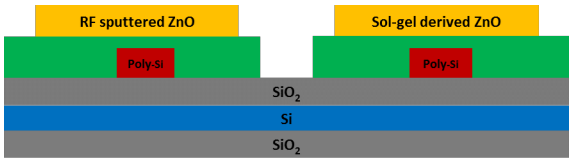
(g) Photolithography to pattern sol-gel derived ZnO layer.



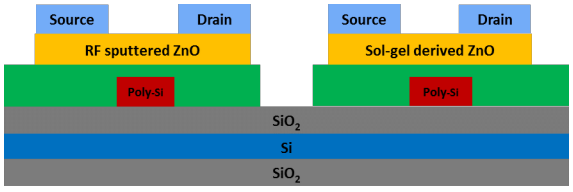
(h) Etch the uncovered part of ZnO and lift off.



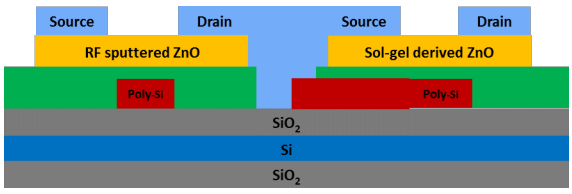
(i) Photolithography to protect the sol-gel derived ZnO and make pattern for sputtered ZnO.



(j) Lift off and anneal for one hour.



(k) Do the metallic contacts deposition and normally on and normally off transistors are on the same wafer.



(l) NOT gate cross-section.

Figure 2.14: Procedure for patterned bottom gate TFTs and logic circuits fabrication.

The patterned bottom gate ZnO TFTs and circuits fabrication process can be briefly summarized in the flow charts (Fig. 2.14) as below. The bottom gate which was chosen as poly

silicon was deposited *via* low pressure chemical vapor deposition (LPCVD). The reason of using poly silicon is to avoid metal contamination in the LPCVD chamber (Fig. 2.15). Phosphor has been chosen to dope poly silicon to make highly doped p-Si, which can be treated as a metal. The gate dielectric layer which was SiO_2 was also deposited by LPCVD and patterned through reactive-ion etch (RIE) (Fig. 2.16) to make gate exposure. The thicknesses of the patterned bottom gate, gate dielectric layer, sol-gel derived ZnO and RF magnetron sputtered ZnO are 300, 75, 100 and 70 nm, respectively.

Figure 2.15: Low pressure chemical vapor deposition (LPCVD) system.

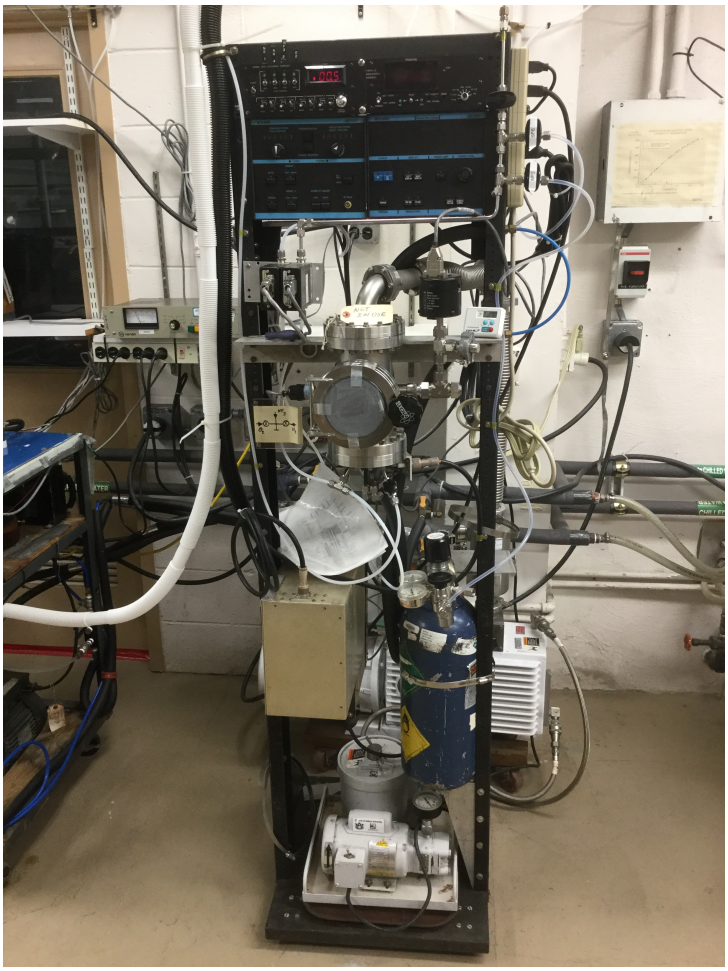
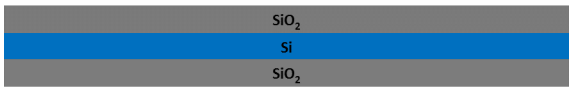
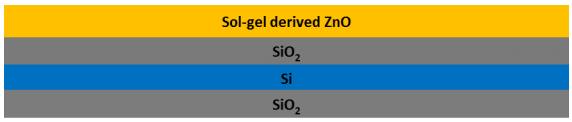


Figure 2.16: Reactive ion etch (RIE) system.

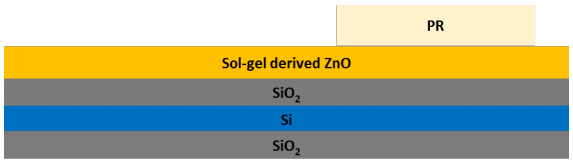
With patterned bottom gate ZnO TFTs it is possible to make ZnO TFTs and integrated circuits. However, the shortcomings are still obvious. To solve these problems, patterned top gate ZnO TFTs has been carried out. Compared to the patterned bottom gate ZnO TFTs and circuits, the top gate ZnO TFTs shows simpler fabrication process, low gate leakage current and and a planar ZnO channel.



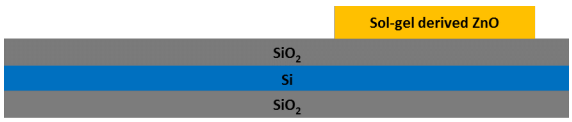
(a) Oxidized wafer prepared.



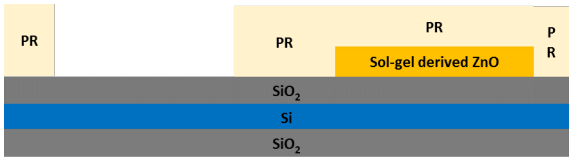
(b) Spin-coat sol-gel derived ZnO layer, anneal for one hour.



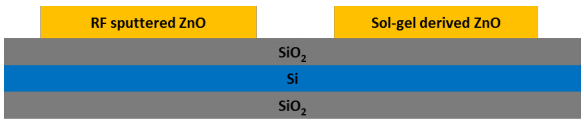
(c) Photolithography to pattern sol-gel derived ZnO layer.



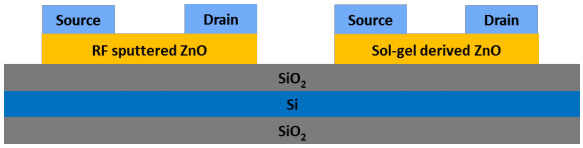
(d) Etch the uncovered part of ZnO and lift off.



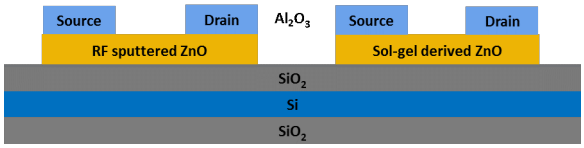
(e) 4. Photolithography to protect the sol-gel derived ZnO and make pattern for sputtered ZnO.



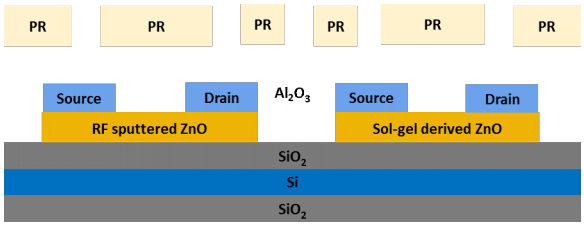
(f) Lift off and annealing for one hour.



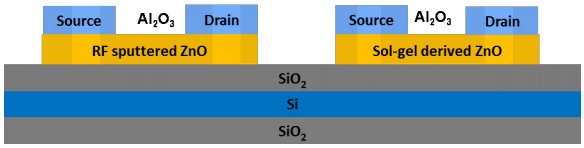
(g) Do the metallic contacts deposition and normally on and normally off transistors are on the same wafer.



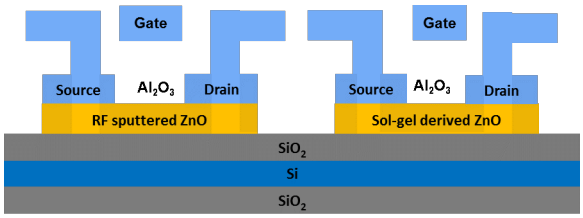
(h) Use ALD to deposit Al_2O_3.



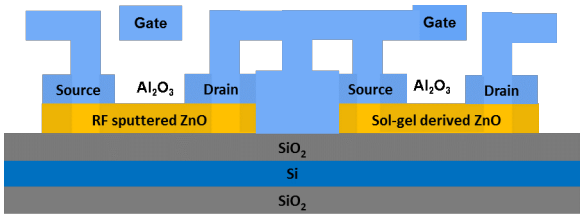
(i) Pattern the Al_2O_3 to expose parts of source and drain and isolate device.



(j) Etch away uncovered Al_2O_3 and lift off.



(k) Pattern the gate and deposit metallic contacts.



(l) Cross-section of NOT gate.

Figure 2.17: Procedure for patterned bottom gate TFTs and logic circuits fabrication.

The patterned top gate ZnO TFTs and circuits fabrication process is shown in the flow charts (Fig. 2.17) below. The gate dielectric layer was chosen to be Al_2O_3, which is a high-k

material. Using Atomic layer deposition (ALD) (Fig. 2.18), a dense and high quality gate dielectric layer can be formed. Compared to LPCVD, ALD can be operated at a relatively low temperature (100 °C) and produce a high-k dielectric layer with lower gate leakage current.

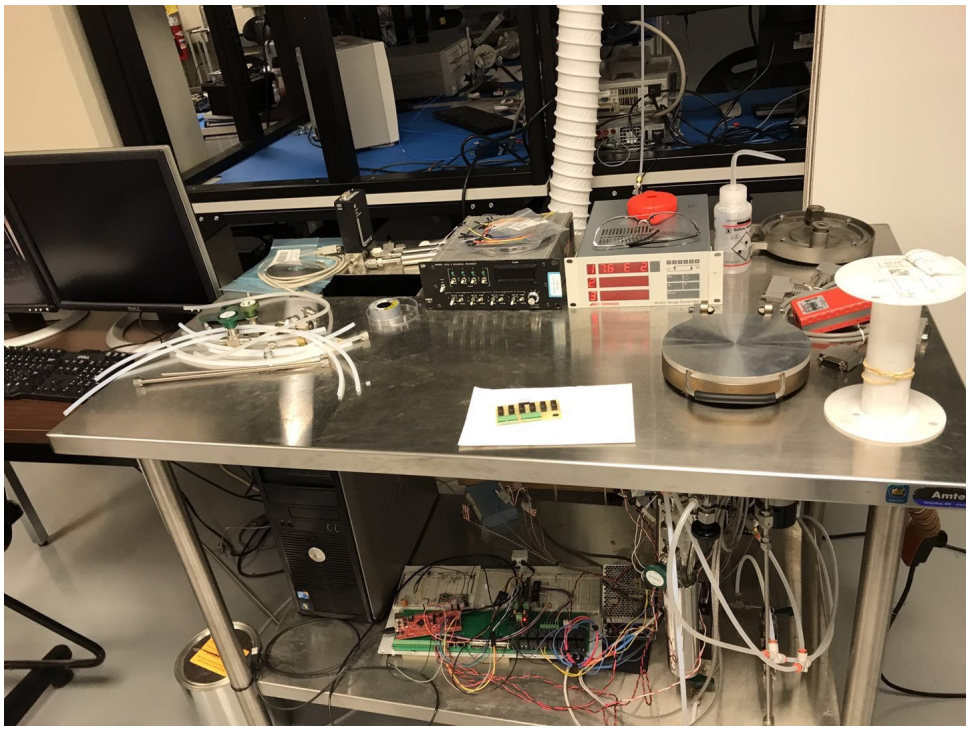


Figure 2.18: Home-made atomic layer deposistion (ALD) system.

2.3 Materials and device characterization

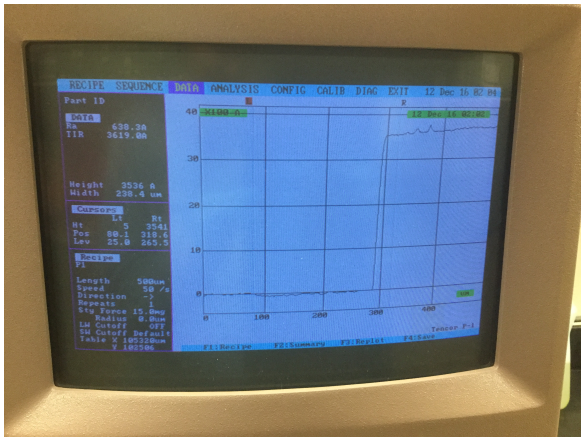
2.3.1 Thickness and surface structure measurements

Thin film and device characterization followed the fabrication of the devices. The first and crucial step for analyzing a deposited thin film is to check its thickness. Profilometry, atomic force microscopy, and ellipsometry were used to measure the thin film thickness. Profilometry, is the most straightforward method because it is cheap, simple to set up and fast, which explains its frequent use in labs.

Fig. 2.19 show the TENCOR P-1 profilometer used in our lab and the thickness result generated through it. The ZnO/ZTO samples were placed on the sample holder and a needle is mechanically dragged along the thin film surface to detect the differences of the height. As

it requires force feedback and contact with the surface, its sensitivity and destructive effect on soft surfaces can limit its usage.

(a) TENCOR P-1 profilometer



(b) Thin film thickness measured from profilometer

Figure 2.19: Profilometer and the thickness of thin film measured.

Atomic force microscopy (AFM) is another scanning probe microscopy. Compared to the stylus profilometer, AFM (Fig. 2.20) can be used for the surface topography imaging and many other material characteristic such as friction, thickness, roughness and even capacitance, conductivity and resistance mapping.

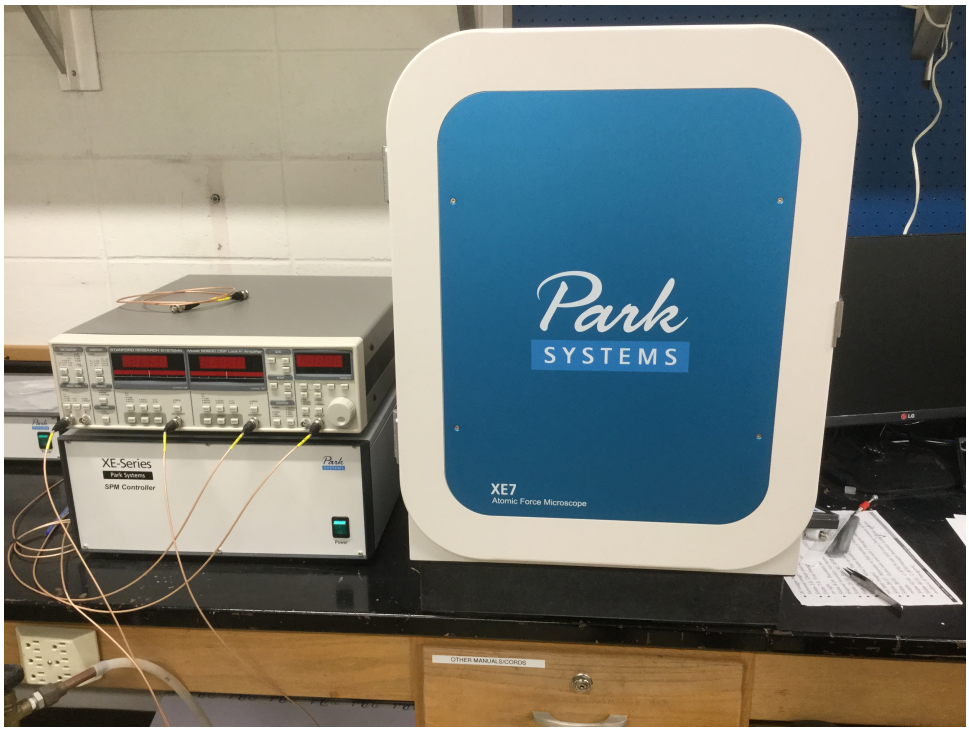


Figure 2.20: Park XE7 Atomic layer force (AFM) system.

The surface structure and properties of the material are studied by detecting the extremely weak interatomic force between the surface of the sample and the sensing tip of a cantilever probe. When measuring topography, the sample is scanned and the force distribution information is obtained by detecting minute strain on the cantilever. Then the surface topography information and surface roughness at nanometer resolution can be obtained through submicron scale movement of the tip from a piezoelectric driven stage. The 2D and 3D images of ZTO thin films will be presented in section 6.

Even though AFM has a lot of merits, such as providing lots of materials information, high surface resolution and material characterization, probe contact can still cause contamination when used in contact and tapping mode as it does in profilometry. The whole process is also very time-consuming. Focusing on oxide thickness characterization, ellipsometry measures a change in polarization as light reflects or transmits from a material structure, which will not contaminate or damage the surface of materials. ST-260 Spectroscopic Ellipsometer (Fig. 2.21) has also been used for measuring the thickness of dielectric layers in ZnO/ZTO TFTs.

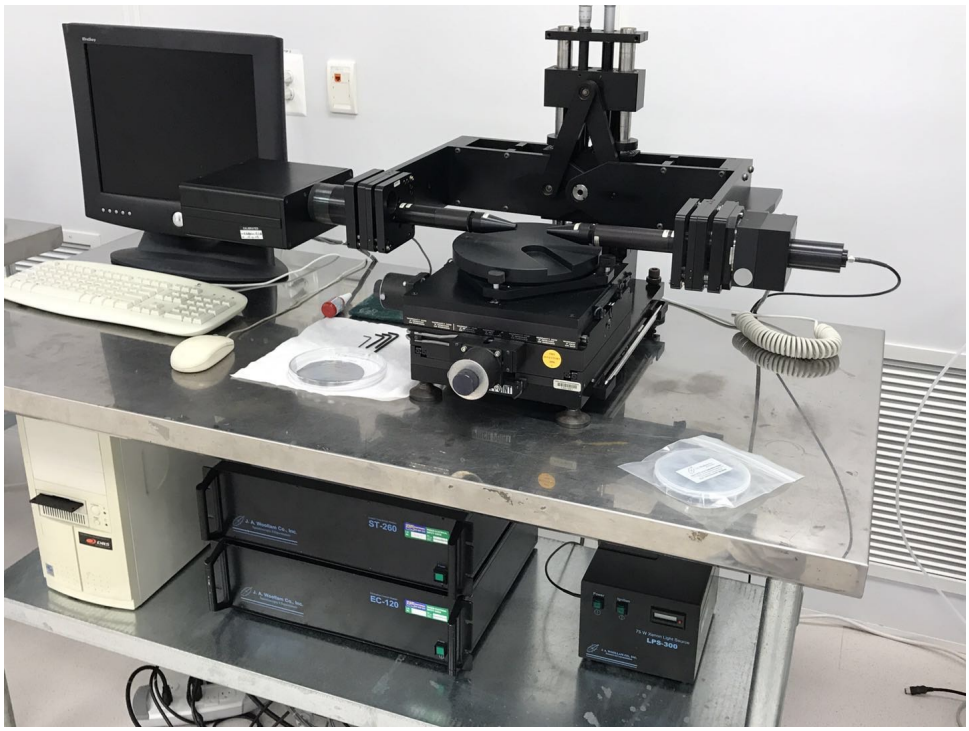


Figure 2.21: ST-260 Spectroscopic Ellipsometer system.

In our research, all three methods were used for different purposes. With profilometry rough but quick ZnO/ZTO thickness information was easily obtained, which was very useful to monitor parameters during process. For high resolution results and roughness details of the ZnO/ZTO surface (chapter 6), AFM was the best choice. While dielectric layer, such as SiO_2 and SiN_X, where any contact with probes will produce contamination and damage, were better measured with ellipsometry.

2.3.2 Raman spectroscopy and photoluminescence

Both Raman spectroscopy and photoluminescence attract great interest for characterizing the electronic properties of thin film semiconductors. They are both non-contact, non-destructive optical tools and can be merged together in a single system (Fig. 2.22). Our Raman system is a home-made set up using a Jobin Yvon spectrometer with a thermally-cooled charge coupled device (CCD) detector (2048 by 512 pixels). When analyzing a ZnO sample, our system which is a Micro-Raman system generates a laser beam that is focused on the thin film with a spot diameter around 7 um to analyze the crystal quality, of the ZnO poly-crystalline thin film.

The peak position (433 cm$^{(}$-1)) and the peak intensity will be used to determine the effect of gamma-ray irradiation on ZnO thin film quality.

Figure 2.22: Home-made Raman spectroscopy and photoluminescence (PL) system.

Photoluminescence (PL) is a similar material diagnosing tool in which the material under test absorbs photons sent by the light source and reradiates photons. Typically, the crystal quality, materials defect and intra band traps can be extracted from the spectrum peaks' width, position, and intensity. Specifically for ZnO analysis, a narrow UV peak and broad visible peak are obtained and attributed to the ZnO crystallinity and defects respectively. In this dissertation, photoluminescence was employed to study the gamma-ray irradiation (Chapter 3) and annealing temperature effect (Chapter 4).

2.3.3 X ray diffraction

X-beam diffraction stands out amongst the most widely used instruments for material characterization because of it gives most of the times a straightforward and reliable answer to queries on samples crystal structure. The atoms of a material diffract the X-beam into different particular directions and from which we can tell the crystal structure and its orientation. The

hexagonal phase ZnO Wurtzite structures index diffraction peaks corresponding to the lattice planes (100), (002), (101), (102), (110), and (103) based on the Joint Committee on Powder Diffraction Standards (JCPDS 36-1451) [5]. The (002) ZnO crystal plane indicates ZnO c-axis orientation, while ZnO crystals are oriented perpendicularly to the substrate. The most efficient charge transport orientation in TFTs is along its channel layer [6]. Specifically speaking, a preferable ZnO crystal orientation is believed to be (002) plane parallel to or c-axis perpendicular to the substrate [6]. As a result, the peak located at around 34 degrees was mainly studied when ZnO XRD analysis was carried out.

In this work, a Bruker D2 Phaser X-ray diffractometer (Fig. 2.23) was employed to analyze ZnO quality change as it was exposed to progressive doses of gamma-ray irradiation (Chapter 3) but also ZnO crystal quality in relation to annealing temperature (Chapter 4) and ZTO structure orientation as a function of different concentrations and deposition processes (Chapter 5)

Figure 2.23: Bruker D2 Phaser X-ray diffractometer.

2.3.4 Scanning Electron Microscopy

Scanning electron microscopy (SEM), produces fine qualitative images of the morphology of samples but also allows through EDS a quick test of material composition. Field emission-scanning microscope (FE-SEM, JEOL JSM-7000F, JAPAN) (Fig. 2.24) has been applied to ZnO surface and cross-section morphology study. Fig. 2.25 represents the surface of ZnO thin-film after one hour 800 °C annealing. As can be found in this image, uniform and densely

packed arrays of ZnO nanorods synthesized in a preferable c-axis orientation. Fig. 2.26 shows the cross-sections of one hour 800 °C annealed sol-gel derived ZnO thin film. 4 layers and 8 layers ZnO thickness are 100 nm and 170 nm, which are consistent with the results generated from profilometry measurement.

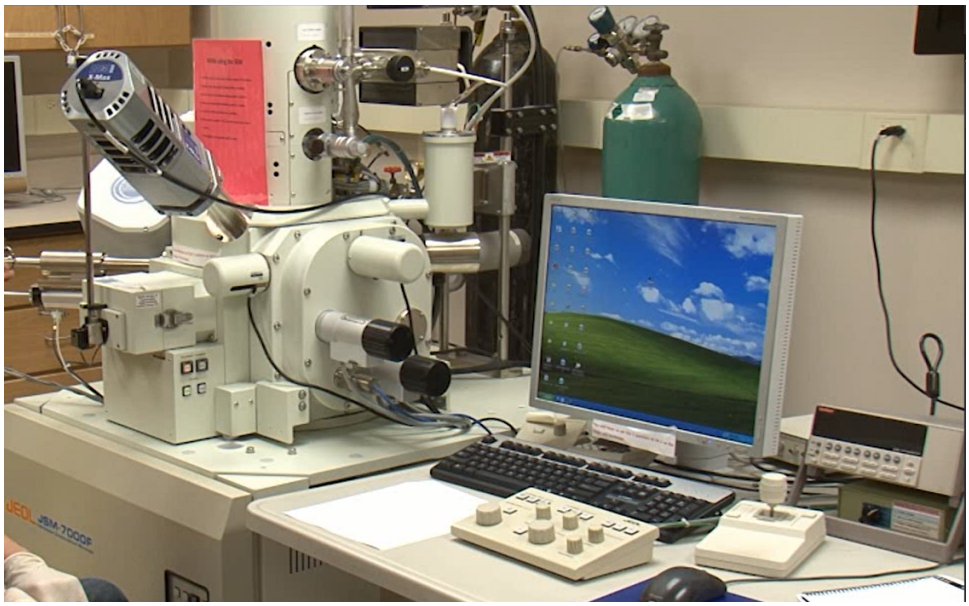


Figure 2.24: FE-SEM, JEOL JSM-7000F system.

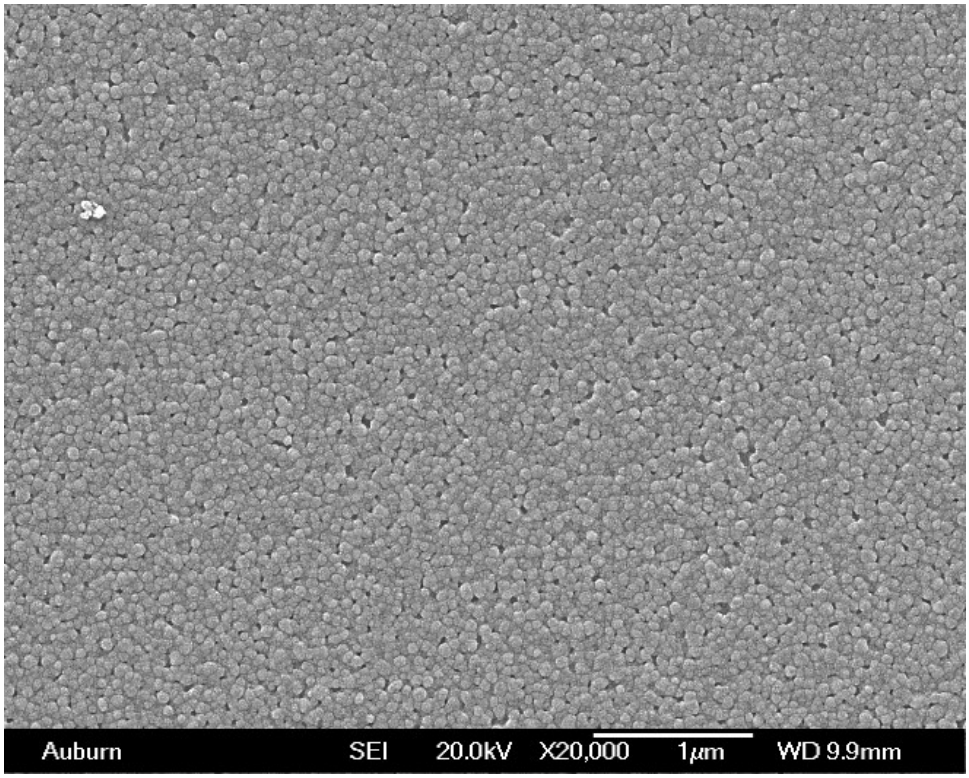


Figure 2.25: SEM surface morphology of ZnO layer annealed at 800 °C for one hour.

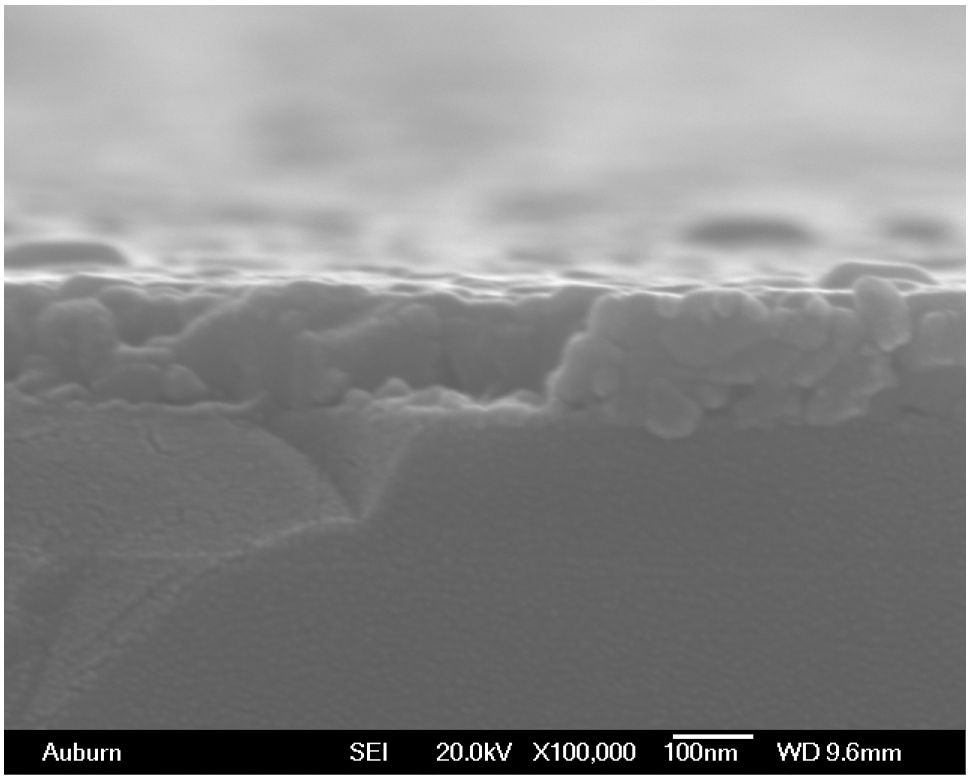


Figure 2.26: SEM cross-section of ZnO layer annealed at 800 °C for one hour.

2.3.5 IV measurement

The ultimate purpose of the material characterization done in this study is to guide the fabrication process and insure the high performance of the devices fabricated. Both ZnO/ZTO TFTs and the logic circuits made with them have to be characterized using the current vs voltage (IV) measurement method. A Keithley 4200-SCS (Fig. 2.27), HP 4156 A (Fig. 2.28) and Keithley 6517 (Fig. 2.29) were combined through a the control of a computer to build a comprehensive test system. For TFTs study, transfer IV measurements and output IV measurements (I_D-V_{DS}) were used. From transfer IV measurement, many key parameters, such as threshold voltage (V_T), turn-on voltage (V_{on}), transconductance (G_m), field effect mobility (μ_{FET}), on/off ratio, subthreshold swing (SS) and interface trap density (D_{it}) can be extracted. These parameters are useful to understand the different phenomena taking place in the device. The output IV curve directly reflects a transistor working condition.

Figure 2.27: Keithley 4200 (Semiconductor Characterization Systems) parameter analyzer.

Figure 2.28: HP 4156 A (Semiconductor Characterization Systems) parameter analyzer.

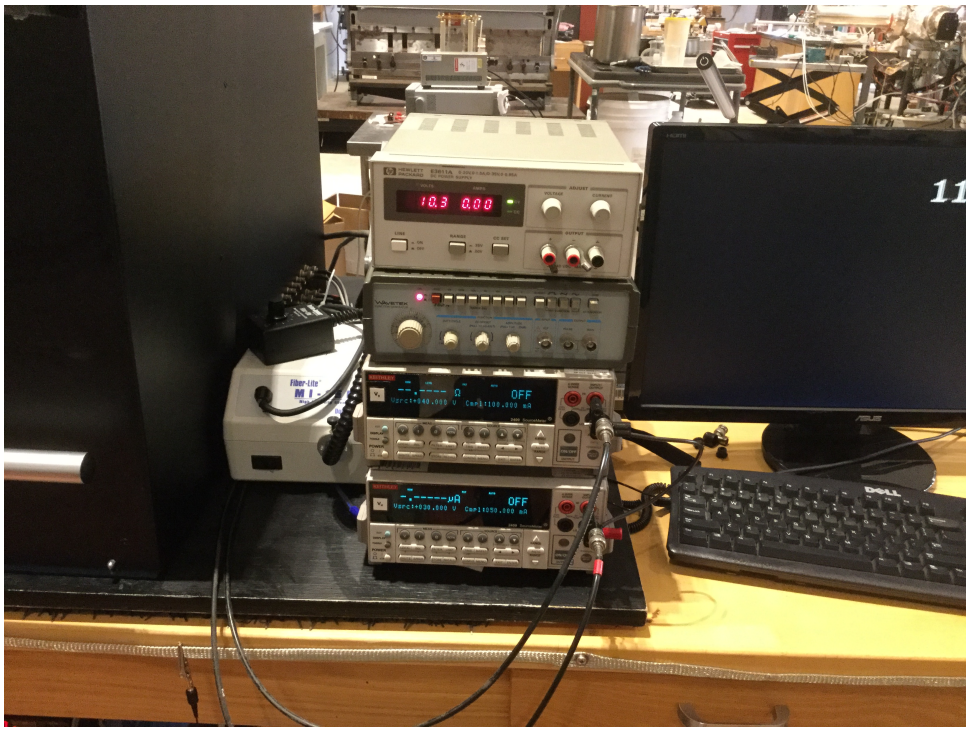


Figure 2.29: Keithley 6517 (Semiconductor Characterization Systems) parameter analyzer.

Low temperature and high temperature measurements were carried out in a cryogenic system. An ARS micro-manipulated cryogenic probe station (Fig. 2.30) was used to connect an analyzer to the sample. The ZnO sample was kept in the chamber and the pressure was maintained at 10^{-4} Pa to suppress moisture and oxygen effect on the sample [7]. Using a combination of heated chuck and liquid helium, the measurement temperature range was varied from 10 K to 410 K. Both low temperature effect (Chapter 3) and temperature dependent IV measurement (Chapter 4) were performed in this system.

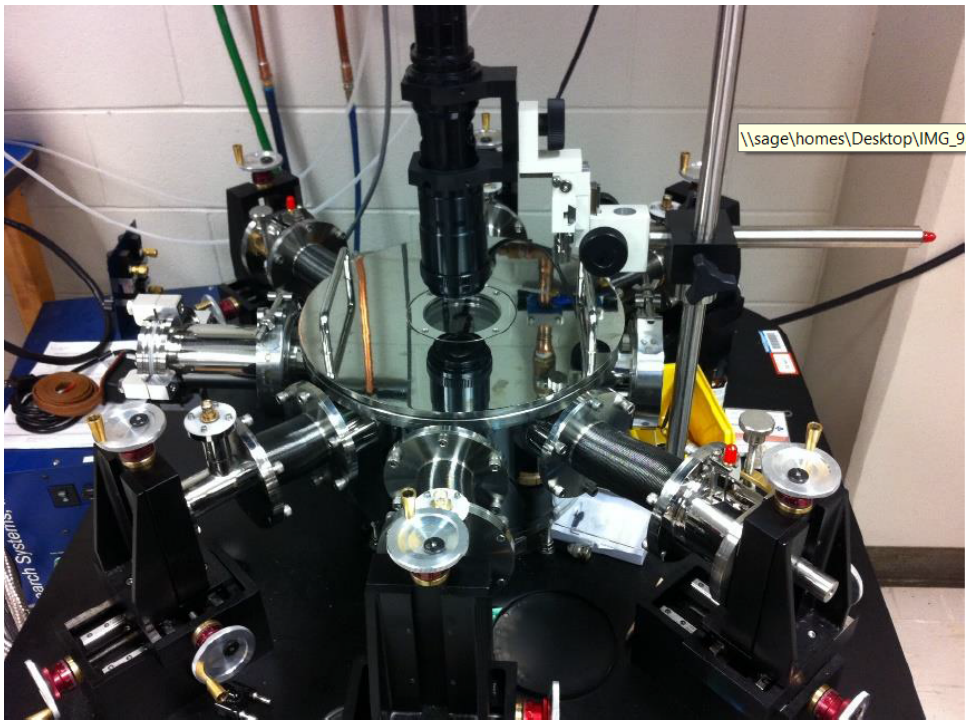


Figure 2.30: ARS micro-manipulated cryogenic probe station.

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Chapter 3

Gamma-ray irradiation and low temperature effect on ZnO TFTs

3.1 Background and motivation

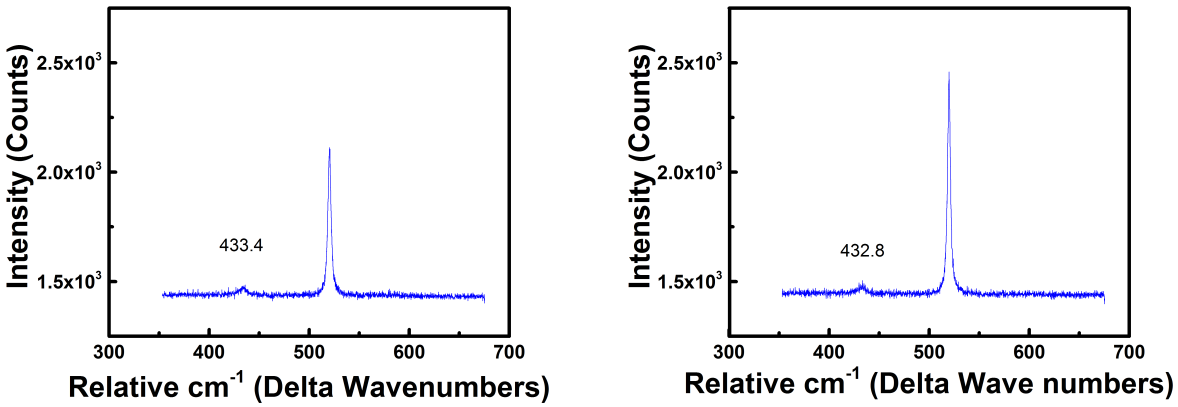
ZnO with a direct and wide energy band gap of 3.37 eV has been considered and demonstrated as a viable candidate for electronic and optoelectronic applications. Additionally, ZnO is known to be more resistant to radiation damage than other semiconductor materials and is considered for electronics in a radiation harsh environment such as space which has already been introduced in Chapter 1. In spite of this, only a small amount of research has been carried out on the analysis of radiation effects on ZnO transistors. Previously, ZnO thin film transistors based on plasma enhanced atomic layer deposition were irradiated with gamma-rays and its characteristics were analyzed [1]. However, no research has been reported on the study of gamma-ray irradiation of sol-gel derived ZnO transistors. Therefore, in this work, we have fabricated ZnO transistors with sol-gel derived active layer and studied gamma-ray irradiation effects. Additionally, the low-temperature performance of the devices was also investigated since low-temperature is another essential phenomenon prevalent in space.

3.2 Gamma-ray irradiation effect

3.2.1 Raman spectroscopy and PL analysis

Sol-gel derived ZnO thin-films with four layers (100 nm thicknesses) were irradiated under 10 MRad gamma-ray from ^{60}Co source. Micro-Raman spectroscopy of ZnO layers before and after irradiation has been plotted in Fig. 3.1 below. The observed peaks at about 433 cm^{-1} and 520 cm^{-1} are assigned to be high frequency E_2 mode of ZnO peak and silicon peak, respectively.

[2] [3] Negligible peak shift was observed. The intensity of ZnO peak before irradiation and after irradiation kept the same value of around 1472 counts.

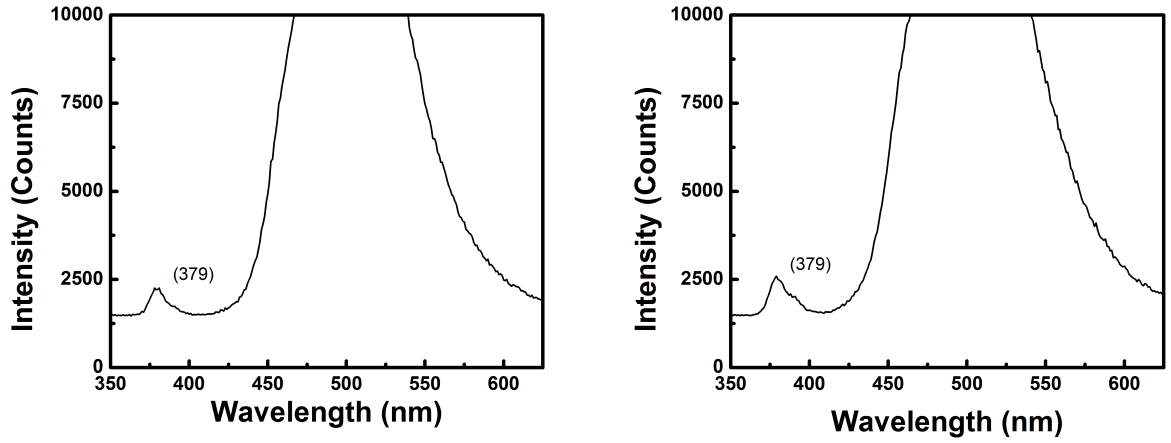


(a) Before irradiation

(b) After irradiation

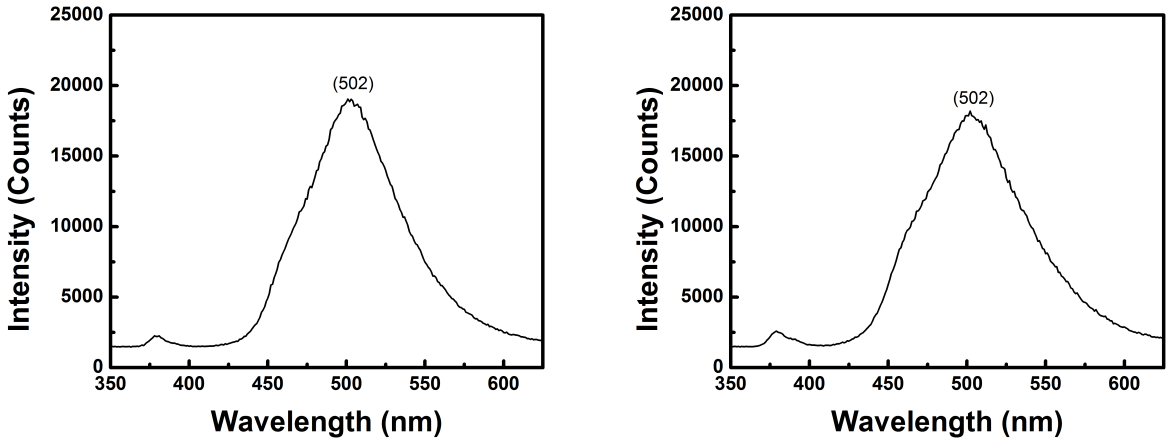
Figure 3.1: Raman spectroscopy for 4 layers (100nm thickness) of ZnO before irradiation (a) and after 10MRad irradiation (b).

Both Fig. 3.2 and Fig. 3.3 demonstrates the PL spectra of the ZnO thin film before and after 10 MRad. The spectra are composed of UV and visible bands. In Fig. 3.2, the position of the UV bands remained around 378 nm, and after 10 MRad gamma-ray irradiation, the intensity of UV band peak slightly increased from 2302 to 2567 counts. And the intensity of visible band peak (around 502 nm) increased from 18088 to 19038 counts. It is known that the visible bands are related to ZnO crystal quality and intrinsic defects. [4][5][6]. The rising of visible bands peak indicate the level up of ZnO intrinsic defects after gamma-ray irradiation.



(a) Before irradiation (b) After irradiation

Figure 3.2: PL focused in UV region for 4 layers (100nm thickness) of ZnO before irradiation (a) and after 10MRad irradiation (b).



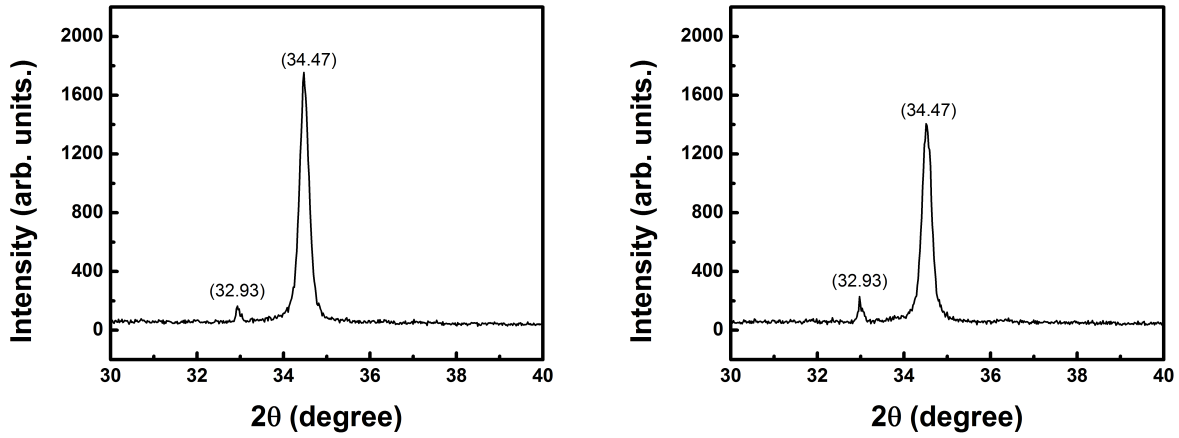
(a) Before irradiation (b) After irradiation

Figure 3.3: PL focused in visible region for 4 layers (100nm thickness) of ZnO before irradiation (a) and after 10MRad irradiation (b).

3.2.2 X-ray diffraction

XRD has also been employed for analyzing the gamma-ray irradiation effect (Fig. 3.4).The dose of gamma-ray is 13.8 MRad, which is still very low. After eliminated K-alpha peaks located around 69.3 degrees, the ZnO preferable (002) crystal plane and (100) crystal plane were observed at 2 theta around 34.4 degrees and 32.9 [7], separately. The peak intensity

for (002) crystal plane drops from 1800 to 1500 (arb. unites.), which can be attributed to the degradation of ZnO TFTs electrical performance after irradiation (section 3.2.3).



(a) Before irradiation

(b) After irradiation

Figure 3.4: XRD for 4 layers (100nm thickness) of ZnO before irradiation (a) and after 13.8 MRad irradiation (b).

3.2.3 IV measurement

Two types of 4-layer ZnO TFTs with different metallic contacts titanium (Ti)/ aluminum (Al) and titanium (Ti)/ Palladium (Pd) have been fabricated. 10 MRad and 13.8 MRad gamma-ray irradiation have been applied on these two samples. The figures of the device with Ti/Al ohmic contact indicate the severe damage dealt with the metal contact (Fig. 3.5). We assume the damage can be decreased by replacing aluminum with heavier atomic weight metals as the contact. The energy required to sublimate the metal contact atoms would be increased accordingly. The figures of the device with Ti/Pd show minimal damage to the contacts (Fig. 3.6).

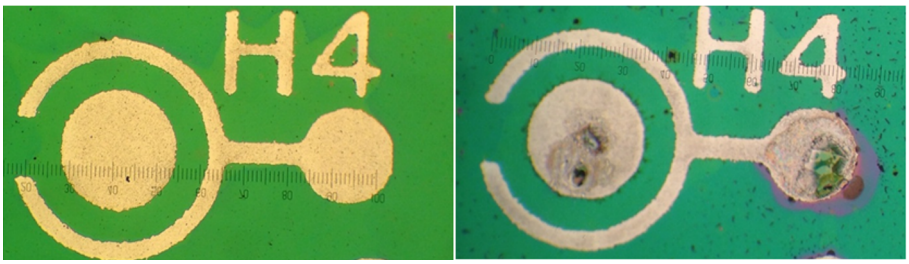


Figure 3.5: Device of Ti/Al ohmic contact without being irradiated (left) and a device with irradiation dose of 10 MRad (right).

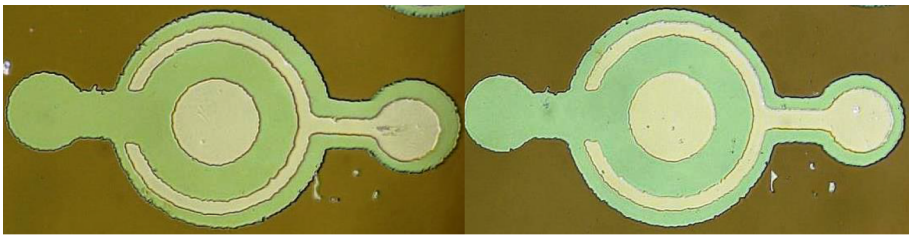


Figure 3.6: Device of Ti/Pd ohmic contact without being irradiated (left) and a device with irradiation dose of 13.8 MRad (right).

Most ZnO TFTs with Ti/Al metallic contacts didn't work because of the severe damage to contacts. We focused on ZnO TFTs with Ti/Pd electrodes study. The transfer and outputs IV curves for ZnO TFTs with and without gamma-ray irradiation have been carried out by Keithley 4200 A and plotted in Fig. 3.7 and Fig. 3.8. Both degradations after irradiation are evident. The damage occurred to the metallic layer and ZnO layer (XRD results) might cause the degradation.The transconductance (G_m) (Fig. 3.9) and field-effect mobility (μ_{FET}) (Fig. 3.10) were extracted from transfer IV curve. Degradation of the active layers transconductance and mobility is also apparent.

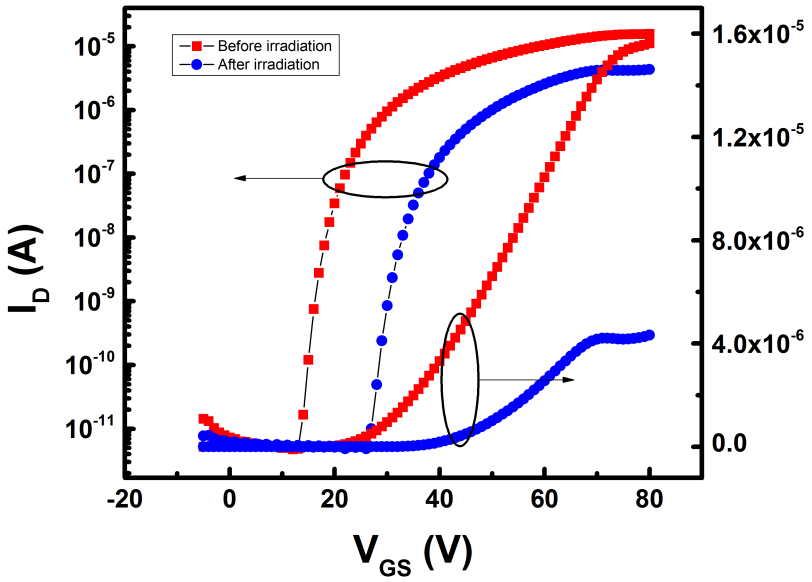


Figure 3.7: The transfer characteristic I-V curve.

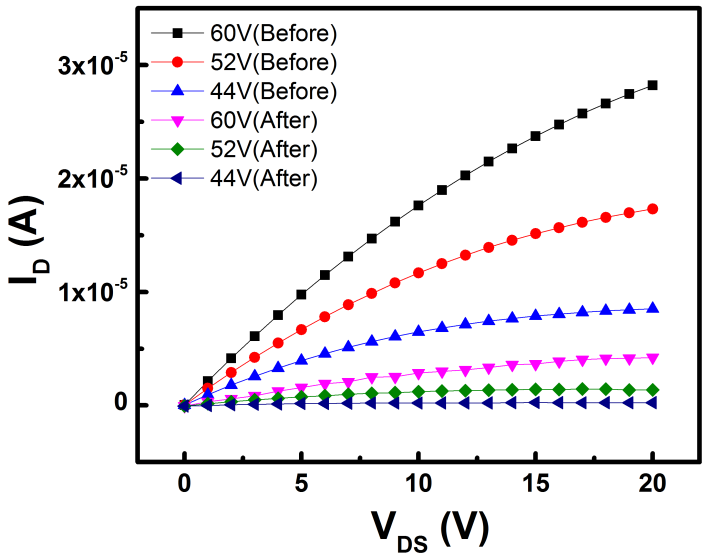


Figure 3.8: The output characteristic I-V curve.

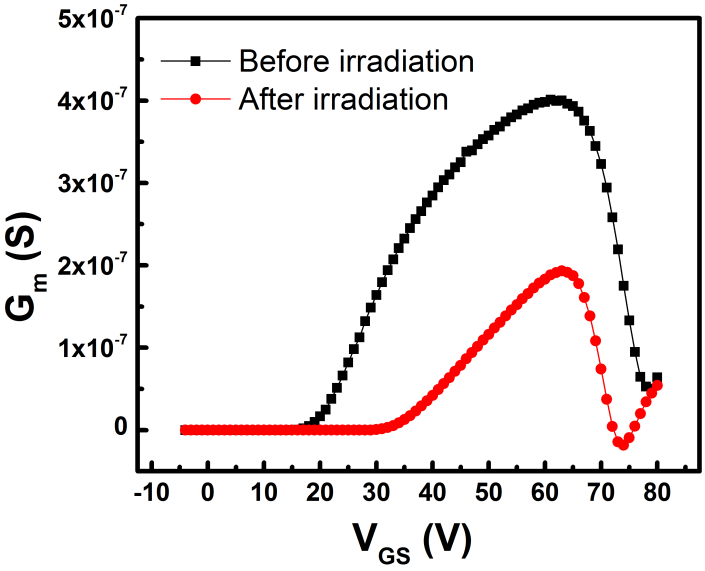


Figure 3.9: Degradation of the active layers transconductance.

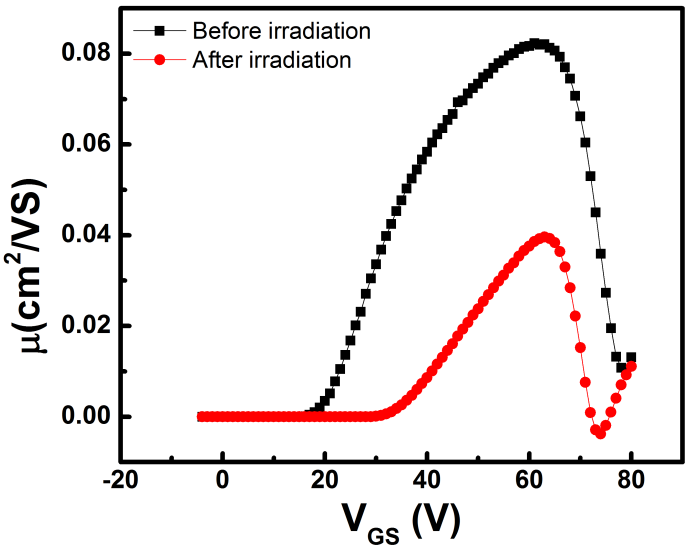
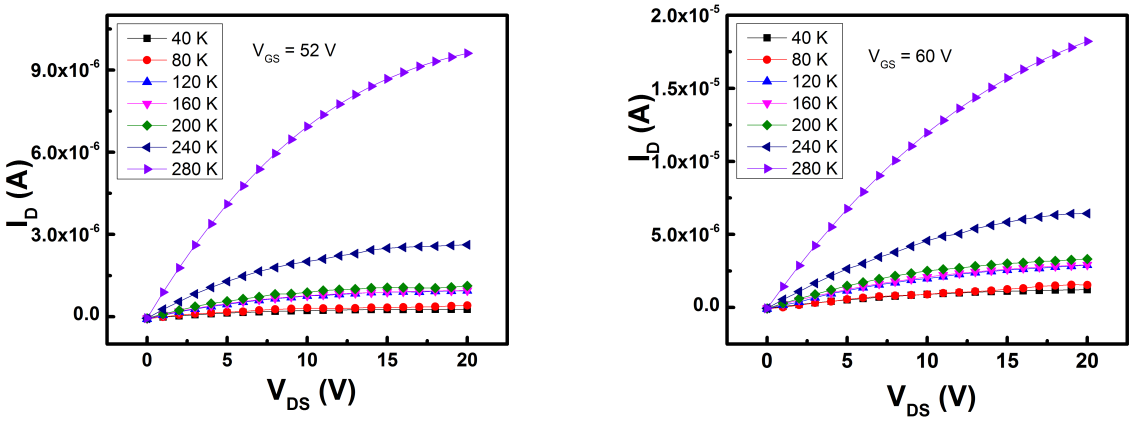


Figure 3.10: Degradation of the active layers mobility.

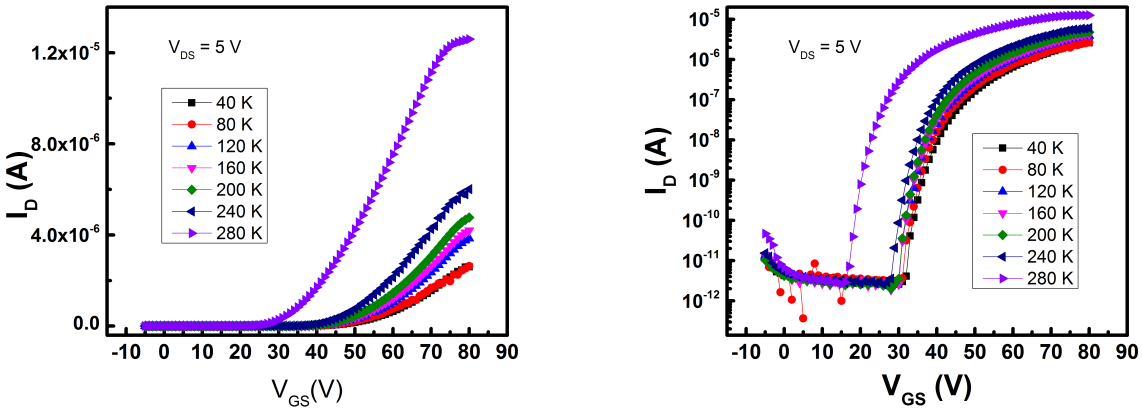
3.3 Low temperature effect

The transistor output characteristics at different temperatures (280 K - 40 K) for a typical device is shown in Fig. 3.11. The I_D - V_{DS} output curves of the transistor at different temperatures with V_{GS} = 52 V are shown on the left and V_{GS} = 60 V on the right. Degradation can be observed with temperature decrease, which verifies that ZnO TFTs output characteristic is temperature dependent. Fig. 3.12 shows the temperature-dependent I_D - V_{GS} transfer characteristic. The transfer characteristics of the transistor at different temperatures is shown in the linear region with V_{DS} = 5 V. The subthreshold slope didn't appear to be affected by temperature, which is approximately 0.8V/decade. The threshold voltage increase due to the decrease in their thermal energy and the on/off ratio decrease with temperature decrease indicated there were more electrons trapped at lower the temperature (Fig. 3.13). At the same V_{GS} - V_T, transconductance and carrier mobility in the linear region with V_{DS} = 5 V decrease with cooling (Fig. 3.14). Despite the aggravation imposed on the transistors, the devices fairly functioned well.



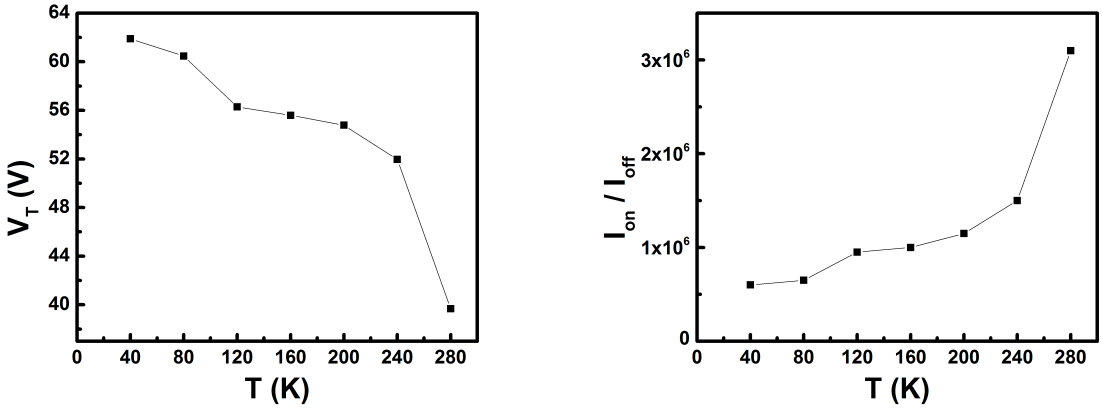
(a) V_{DS} = 52 V (b) V_{DS} = 60 V

Figure 3.11: Output IV curves for low temperature measurement.



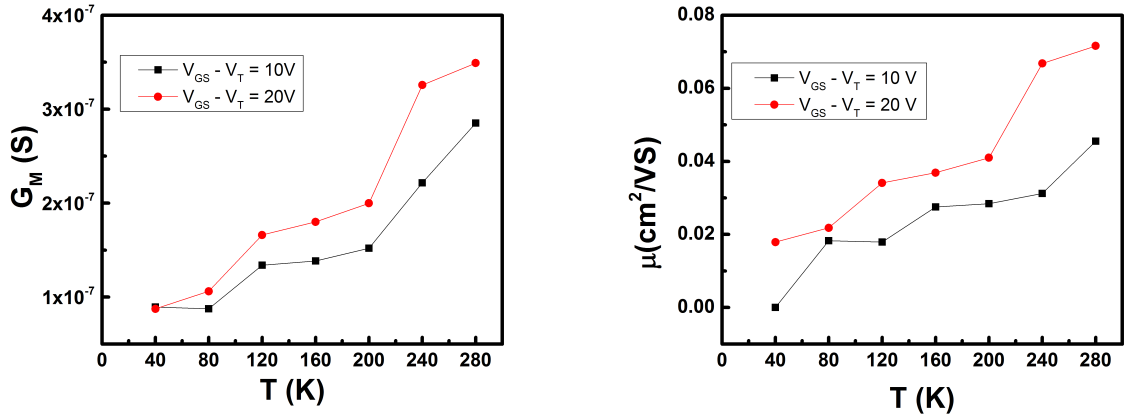
(a) Linear scale (b) log scale

Figure 3.12: Transfer IV curves for low temperature measurement.



(a) Threshold voltage shift (b) Drain current on-off ratio

Figure 3.13: V_T and I_{on}/I_{off} decrease with cooling.



(a) Transconductance

(b) Field effect mobility

Figure 3.14: G_m and μ evolution with temperature.

3.4 Summary

Effects of gamma-ray irradiation and cooling on the device performance of sol-gel derived ZnO thin-film transistors were investigated. In both cases, the degradation of device performance was observed. In the case of irradiation, both the metallic and the ZnO layer were damaged. For the low temperature study, the intrinsic transport of ZnO thin film followed the thermal activation process.

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Chapter 4

Electrical characteristics and DOSs of sol-gel derived ZnO TFTs with different channel annealing temperatures

4.1 Introduction

Both direct-current (DC)[1][2] and radio-frequency (RF) [3][4] magnetron sputtering have been commonly used to deposit ZnO at low temperatures. However, these deposition techniques require an expensive instrumentation and the throughput is limited. Compared to sputtering, sol-gel deposition technique offers several key advantages. It is a relatively low cost technique, simple to set up, and can allow a high throughput [5]. Therefore, in this investigation, the ZnO channel layers were grown via sol-gel technique, followed by transistor device fabrication.

Since the annealing of the ZnO channel layer is a critical part of the ZnO TFT fabrication step, it is of great importance to determine the optimal annealing temperature. The effect of annealing on both optical properties of ZnO active layer and electrical characteristics of TFTs is worthy of investigation. One of the methods to characterize the transistor characteristics is to determine the sub-gap density of states (DOSs), from which a valuable insight on various intrinsic electrical properties such as the field effect mobility, the threshold voltage, and the subthreshold swing etc. can be gleaned. Many methods exist for studying sub-gap DOS distribution; photoluminescence (PL) [6][7], photo-excited trap-charge-collection spectroscopy (PECCS) [8], capacitance-voltage (CV) measurement [9] and temperature-dependent field effect measurement [10][11][12][13]. The CV measurement, PECCS, and temperature-dependent field effect techniques have been commonly used for probing traps in field-effect

transistors. PL method is a straight forward technique to investigate the defects in semiconductors. However, the PL method sometime cannot be implemented on a TFT since only a thin region near the surface can be probed for a thick channel layer [6][7][14].

Until recently, only a handful of research has been carried out on determination of sub-gap DOS of ZnO. Lee $et\ al.$ [8] demonstrated determination of DOS using PECCS from the RF magnetron sputtered ZnO TFTs, where the DOSs information was collected by measuring the threshold voltage shift in the photo-electric experiment. Kimura $et\ al.$ [9] provided CV characterization for trap density extraction for RF magnetron sputtered ZnO TFTs by using the Poisson equation and the carrier density equation. However, no study has been performed on determination of sub-gap DOSs for sol-gel derived ZnO TFTs. Temperature-dependent field effect measurement based on the Meyer-Neldel (MN) rule has been successfully applied to extract the DOSs of a-IGZO, ZTO and Cu_2O TFTs [10][11][12][13][15][16]. However, it has never been adopted for study of the sol-gel derived ZnO TFTs. Therefore, in this investigation, this technique is applied to extract the DOSs of sol-gel derived ZnO TFTs with different annealing temperatures. We have carried out the measurement in a vacuum to eliminate the effect of oxygen and water molecules, thus providing a more accurate insight on the intrinsic sub-gap trap density. By using temperature-dependent field effect measurement, we not only verified the efficacy of this technique on determination of sub-gap DOSs of sol-gel derived ZnO TFTs, but also investigated the annealing temperature effect on the evolution of sub-gap DOSs.

4.2 Fabrication

A series of bottom-gate ZnO circular TFTs were fabricated as follows. Initially, highly doped p-type Si wafers were dry oxidized to form the oxide layer with a thickness of approximately 170 nm. The sol-gel precursor solution was prepared by dissolving zinc acetate dehydrate in monoethanolamine (MEA) and isopropanol with 1:1 molar ratio of Zn:MEA. The precursor solution was spin-coated on oxidized Si wafer at 3000 rpm for 30 seconds and then the wafers were calcined at 285 deg. C for 5 minutes. The process (spin coating followed by calcination) was repeated twice. The thickness of the ZnO layer measured by Tencor profilometer is 52 nm. The wafer coated with ZnO was diced into four individual pieces and annealed at 600, 700, 800,

and 900 °C for one hour, respectively. A Ti/Pd contact was deposited by direct-current (DC) magnetron sputtering to form source and drain ohmic contacts. Device isolation was achieved by forming a mesa structure via a wet-chemical etching of the ZnO active layer, which resulted in the reduction of the gate leakage current by more than four orders of magnitude. The length (L) and width (W) of the transistor channel were 80 and 1005

μ

m, respectively, which corresponds to W/L ratio of 12.56. The bottom of each sample was lightly scratched to remove the unwanted oxidized layer of the Si wafer and Ag paint was applied to attach to a copper tape, serving as the bottom gate. A 2D cross section of the finished device structure is shown in Fig. 4.1.

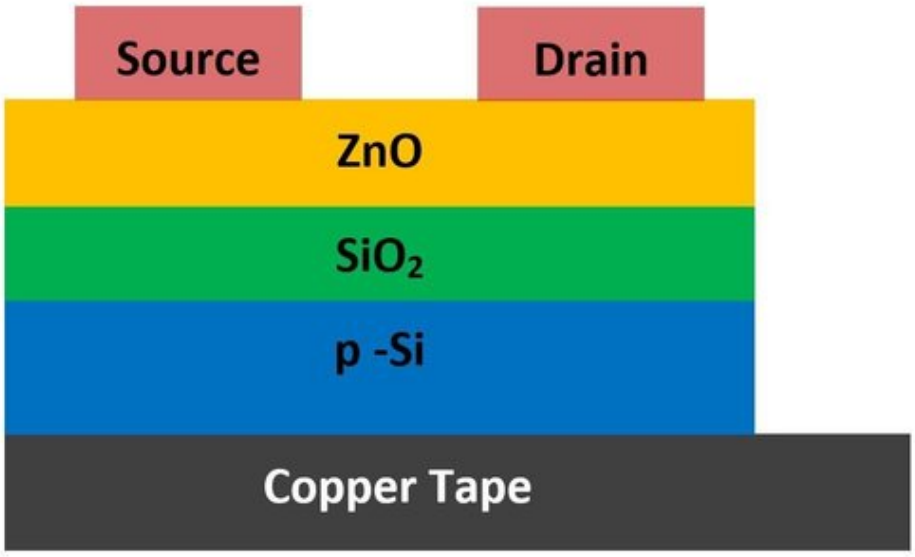


Figure 4.1: 2D cross section of the ZnO TFT device structure (not to scale).

4.3 ZnO thin film characterization

4.3.1 PL spectroscopy

Photoluminescence (PL) spectroscopy was performed at room temperature with J-Y spectrometer coupled with a continuous wave He-Cd laser with 325 nm line as the excitation source. The thickness of ZnO is 52 nm and the penetration depth of the light at 325 nm is 60 nm, which

was calculated from the absorption coefficient reported by Muth *et al.* [16]. Therefore, the UV light from the laser can penetrate the entire thickness of the ZnO film.

Fig. 4.2 shows the PL spectra of ZnO film annealed at 600, 700, 800, and 900 °C for one hour, respectively. The spectra are composed of two distinct bands; UV and visible bands. As can be seen from Fig. 4.2, the absolute intensity of the UV bands increases as annealing temperature increases. It is known that visible bands are related to intrinsic defects in ZnO films [17][18] and the intensity of this band observed from our spectra is very low.

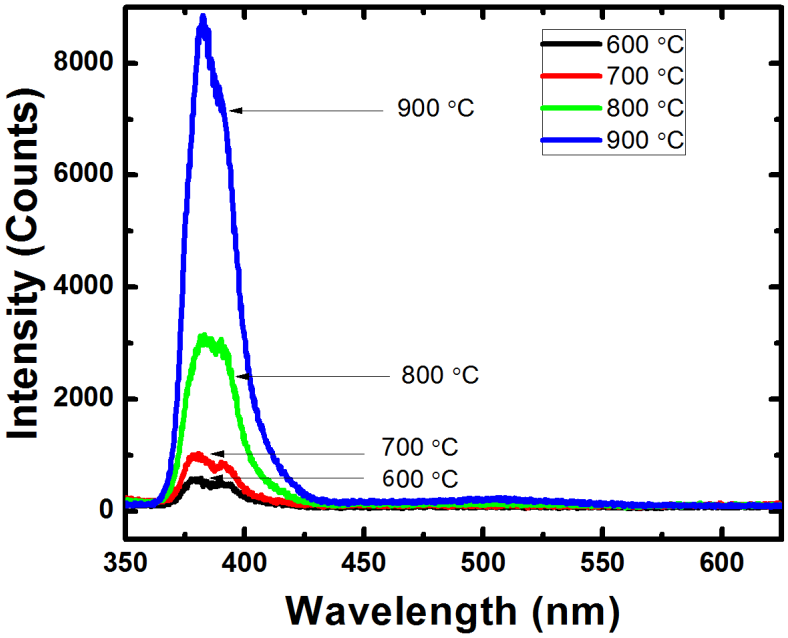


Figure 4.2: Photoluminescence spectra of ZnO annealed at 600, 700, 800, and 900 °C for 1 h, respectively.

Fig. 4.3 shows the ratio of integrated intensity ratio of UV to visible band (I_{UV}/I_{VIS}) as a function of the annealing temperature. The ratio increases as annealing temperature increases, which indicates that the quality of ZnO films improves as the annealing temperature increases.

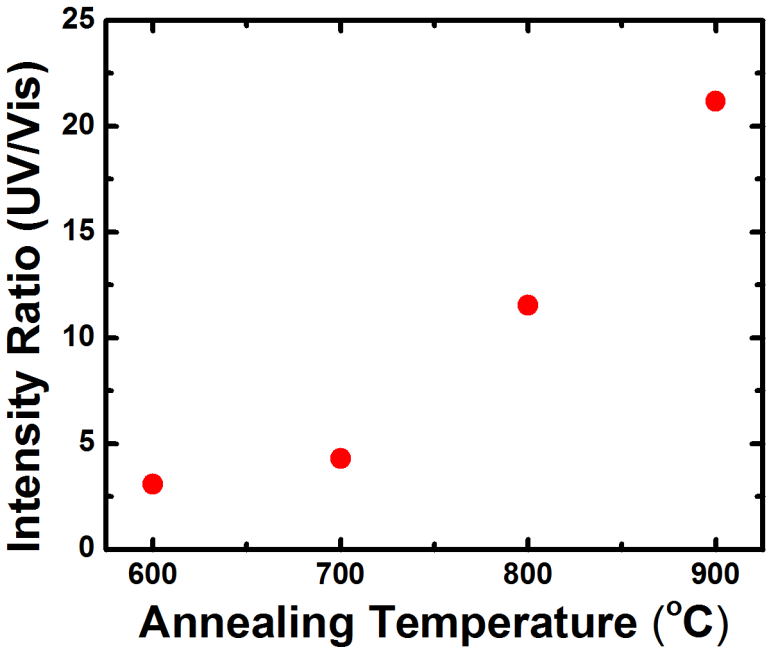


Figure 4.3: Ratio of integrated intensities of UV to visible band (and integrated visible band intensity) of 52 nm ZnO annealed at 600, 700, 800, and 900 °C for 1 h, respectively.

4.3.2 XRD

The c-axis orientation of ZnO with different annealing temperatures were measured by X-ray diffraction (XRD, Bruker D2 Phaser X-ray diffractometer). XRD patterns of the ZnO films annealed at 600, 700, 800 and 900 °C are plotted in Fig. 4.4. The results show that the preferred (002) c-axis orientation is observed and the peak intensity increases with annealing temperature increasing, which is consistent with PL spectra analysis.

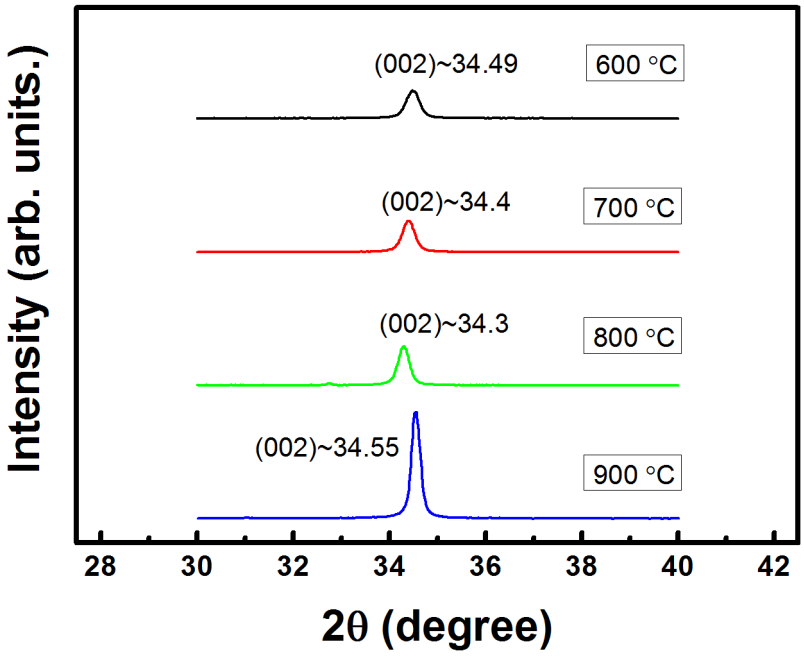
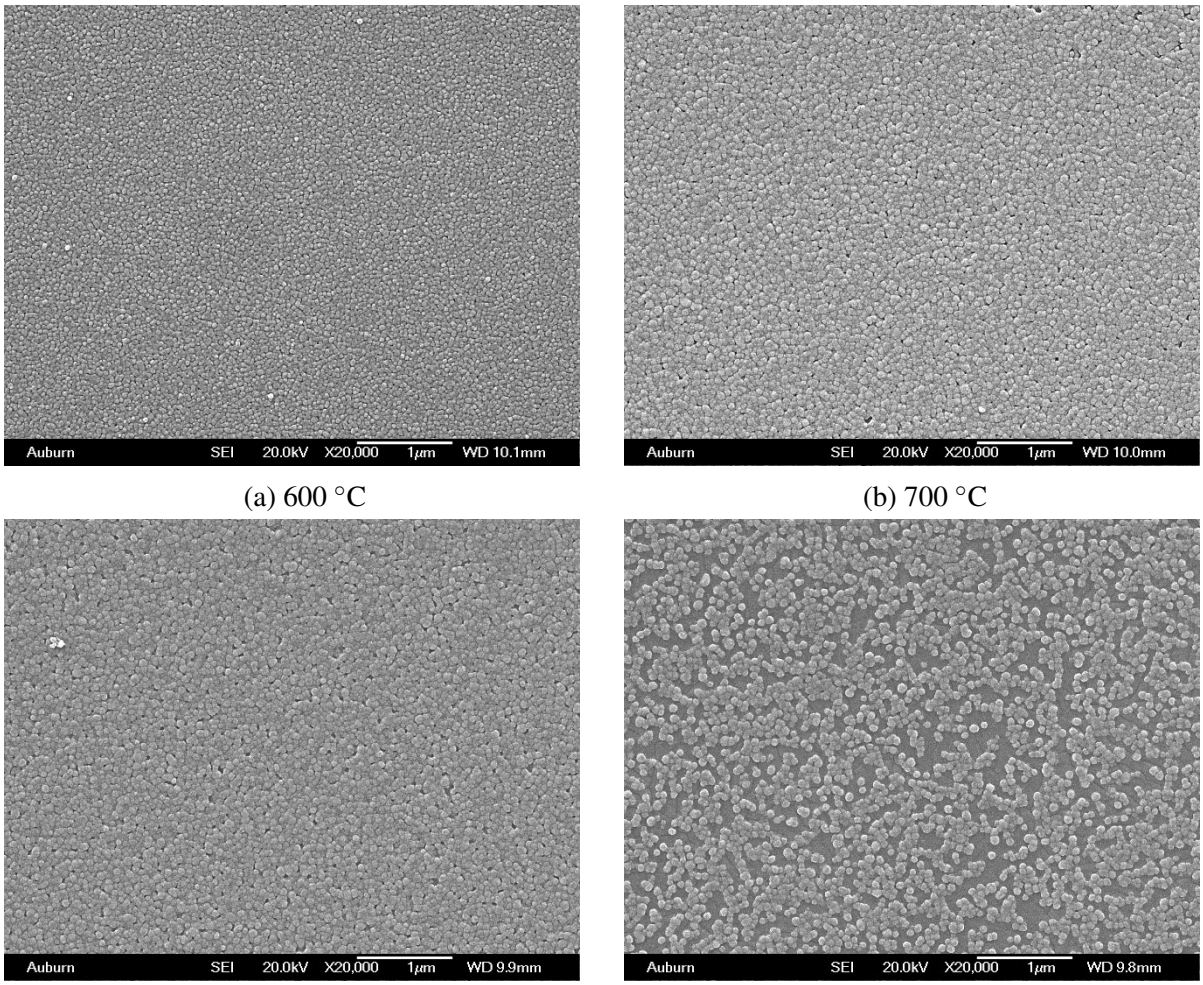


Figure 4.4: XRD patterns of ZnO with different annealing temperatures.

4.3.3 SEM

The surface morphology of deposited ZnO films were also studied by scanning electron microscopy (SEM, JSM-7000F, JEOL, JAPAN). The SEM images of the ZnO films annealed at 600, 700, 800 and 900 °C are shown in Fig. 4.5. The average grain size is increased with the annealing temperatures increasing and hence the amount of grain boundary defects reduced which must have a strong influence on modulating the density of states. The following localized subgap density of states extraction was consistent with SEM analysis. Fig. 4.5 a, b and c show uniform and continuous coverage of the ZnO grains. However, Fig. 4.5 d shows the non-continuous coverage of the ZnO film.



(a) 600 °C (b) 700 °C

(c) 800 °C (d) 900 °C

Figure 4.5: SEM images of the sol-gel derived ZnO thin film annealed at different temperatures: (a) 600 °C, (b) 700 °C, (c) 800 °C, and (d) 900 °C.

4.4 DOSs extraction

4.4.1 Transistor characterization

I-V measurements were carried out in vacuum at various temperatures. A HP 4156b semiconductor parameter analyzer was used. An ARS micro-manipulated cryogenic probe station was used to keep the vacuum pressure at 10^{-4} Pa. The transfer curve was measured by changing the gate voltage from -50 V to 80 V. V_{DS} was selected as 5 V, where transistors can have relatively high transfer current and still work in linear region. In linear region, the field effect mobility (μ_{FET}) and subthreshold swing (SS) can be extracted. Room temperature measurements for 10

devices of each annealing temperature are made first, followed by temperature-dependent measurements from 296 K to 330 K for 22 devices totally. In order to eliminate the influence of the contact about the temperature, probes were landed on the metallic contacts and left there for 20 minutes to keep the probes and the samples at the same temperature before each measurement.

Fig. 4.6 shows the transfer characteristics of the representative ZnO TFTs annealed at 600, 700, 800, and 900 °C, respectively. The off current which is defined as the drain current before drastically rising with the gate voltage increasing decreases as the annealing temperature increased from 600 °C to 800 °C. In the case of the TFTs with ZnO layer annealed at 800 °C and 900 °C, the off current maintains at the level of 10^{-12} A which can be considered as a noise level. The off current for 600 °C annealed sample is at the level of 10^{-9} A, which agrees well with the off current value for 600 °C annealed ZnO TFTs reported by other researchers [5]. However, our optimal TFTs with ZnO annealed at 800 °C exhibits 1000 times lower off current than that reported in the reference [5]. This indicates that low off current can be achieved by increasing annealing temperature. According to the double sweep transfer IV curves, the hysteresis decreases as the annealing temperature increased from 600 °C to 800 °C. However, hysteresis increases with further rising annealing temperature (900 °C). The positive and negative threshold voltage (V_T) with different temperature annealed transistors extracted as hysteresis differences [19] are 8.8, 5.9, 3.0 and 5.5 V, respectively.

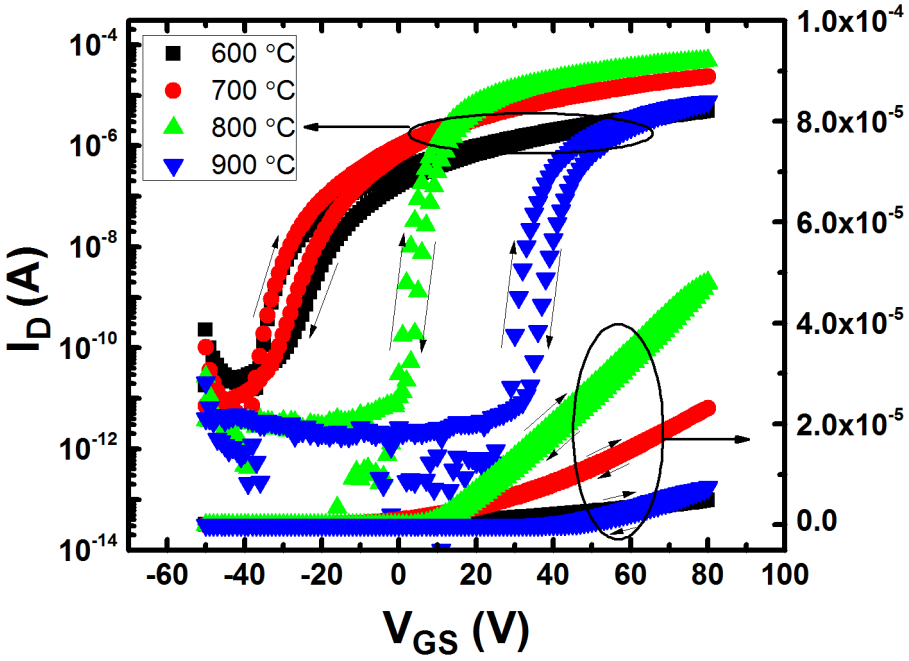


Figure 4.6: Transfer I-V curves for representative TFTs with ZnO layers annealed at 600, 700, 800, and 900 °C.

As is shown in Fig. 4.7, the turn-on voltage (V_{on}) which is defined as the voltage where drain current starts to drastically rise as annealing temperature increases. Both the threshold voltage (V_T) and field effect mobility (μ_{FET}) are extracted from the following equation;

$$I_D = \frac{W}{L} \times C_{SiO_2} \times \mu_{FET}(V_{GS} - V_T)V_{DS}, \tag{4.4.1}$$

where W and L are the width and length of the ZnO channel and C_{SiO2} is the dielectric capacitance per unit area. The threshold voltage (V_T) follows the same trend as the turn-on voltage (V_{on}). This trend can be explained as follows; In ZnO, interstitial Zn is considered as donor. With increasing annealing temperature, more and more interstitial Zn may evaporate [20]. Therefore, a higher annealing temperature leads to less electron carrier density and both V_{on} and V_T shift to a positive direction as the annealing temperature increases.

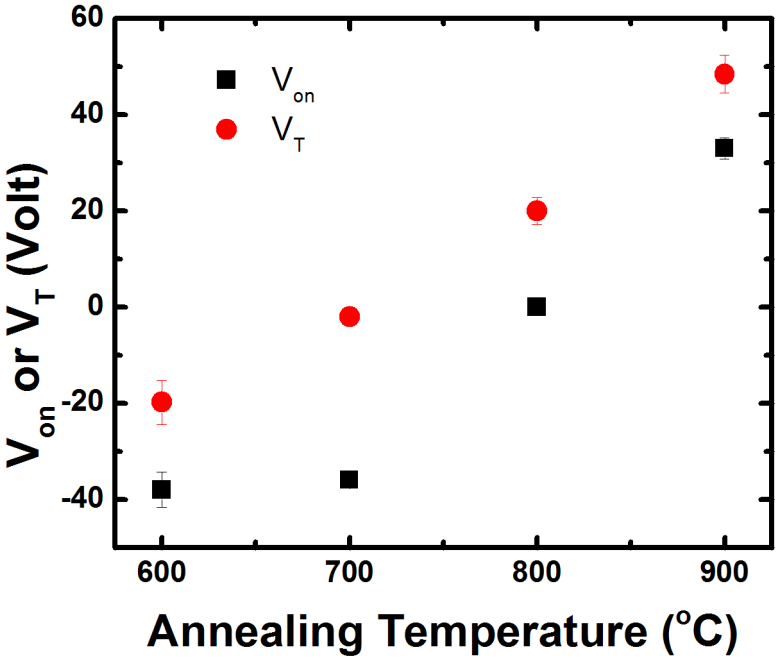


Figure 4.7: V_{on} and V_T as a function of annealing temperature (error bars of V_{on} and V_T for devices with 700 and 800 °C annealing are too short to be observed).

The sub-threshold swing (SS) can be extracted at the steepest point of the transfer IV curves in log scale using the following equation;

$$SS = \frac{d(log(I_D))}{d(V_{GS})}^{-1} \tag{4.4.2}$$

The SS decreases from 2.78 V/decade to 1.42 V/decade with increasing annealing temperature. The interface trap density (D_{it}) was determined by using the following simplified equation [21];

$$D_{it} = (\frac{SS}{ln10} \times \frac{q}{k_B \times T} - 1) \times \frac{C_{SiO_2}}{q}, \tag{4.4.3}$$

where q is the electronic charge and k_B is the Boltzmann constant. Fig. 4.8 shows the plot of the D_{it} of ZnO TFTs with different annealing temperatures. It shows that the corresponding D_{it} decreases from 5.9×10^{12} $eV^{-1}cm^{-2}$ to 2.9×10^{12} $eV^{-1}cm^{-2}$ as annealing temperature increases from 600 °C to 800 °C. When the annealing temperature reaches 900 °C, D_{it} keeps the same level as 800 °C. From SS and D_{it} analysis, it can be concluded that the interface trap density decreased with increasing annealing temperature, thus improving the TFT electrical

characteristics. This conclusion can be further consolidated from the analysis of the localized sub-gap density of states (DOSs) energy distribution presented in later sections. Since the ZnO TFTs have different V_T, the field effect mobility (μ_{FET}) was extracted and plotted in Fig. 4.9 under the same electron concentration (same V_{GS} - V_T). It shows that as annealing temperature increases, μ_{FET} rises more than two times at each annealing temperature. However, when the annealing temperature is 900 °C, μ_{FET} drops abruptly to the value obtained between 600 °C and 700 °C annealing temperature and the transistor output current (shown in Fig. 4.10) drops to the value obtained at 700 °C annealing temperature. As can be seen from the plot, the highest mobility was achieved with an 800 °C anneal.

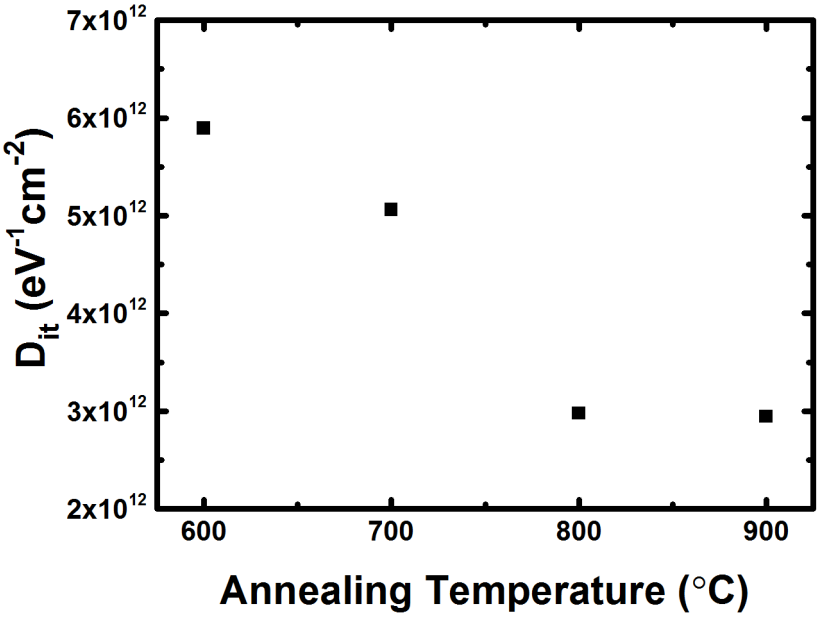


Figure 4.8: D_{it} as a function of annealing temperature.

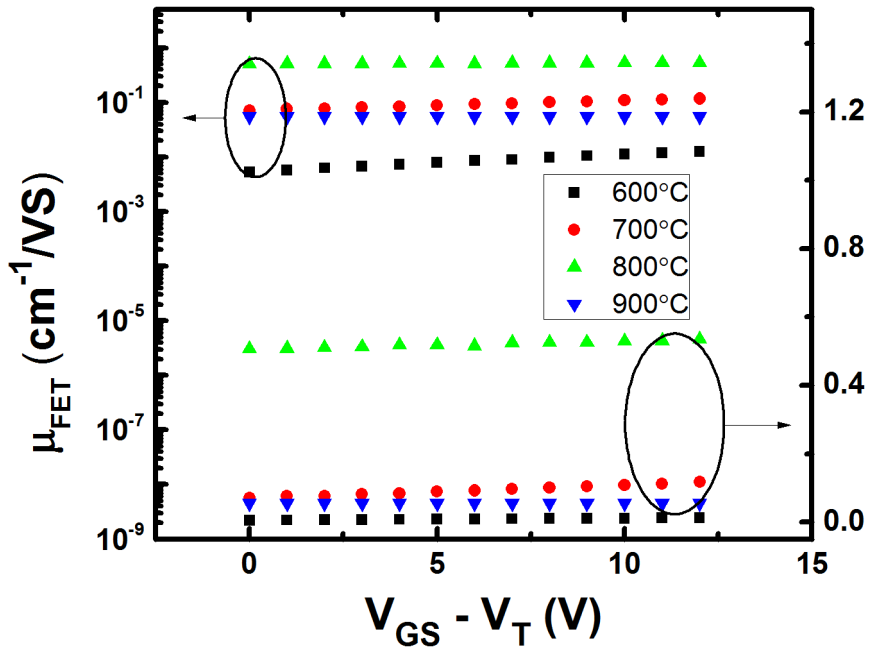


Figure 4.9: μ_{FET} of ZnO TFTs with annealing temperature under the same electron concentration (same V_{GS} - V_T).

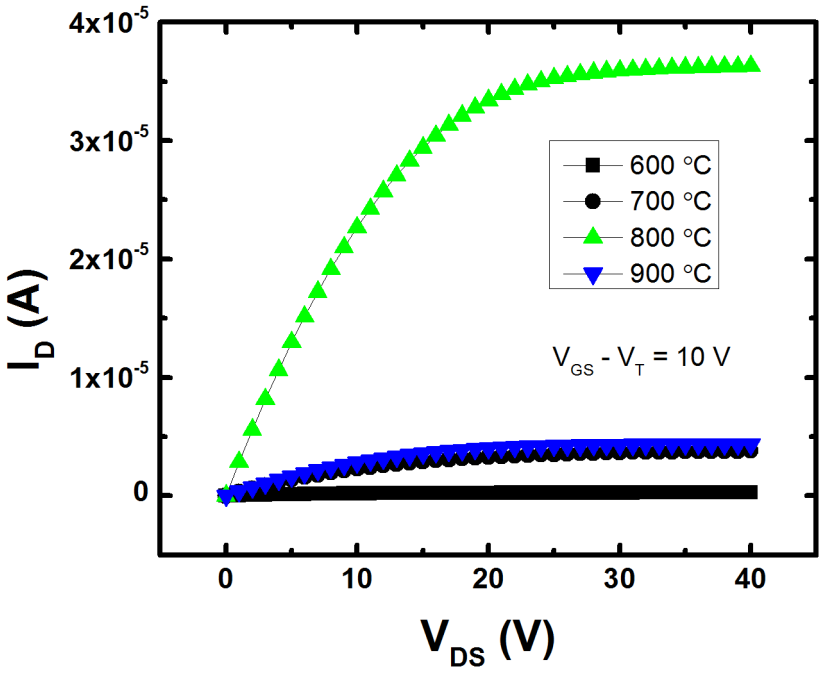


Figure 4.10: Transistor output I-V characteristics for 600, 700, 800, and 900 °C annealed ZnO TFTs under the same effective gate bias (same V_{GS} - V_T).

4.4.2 DOSs distribution calculation

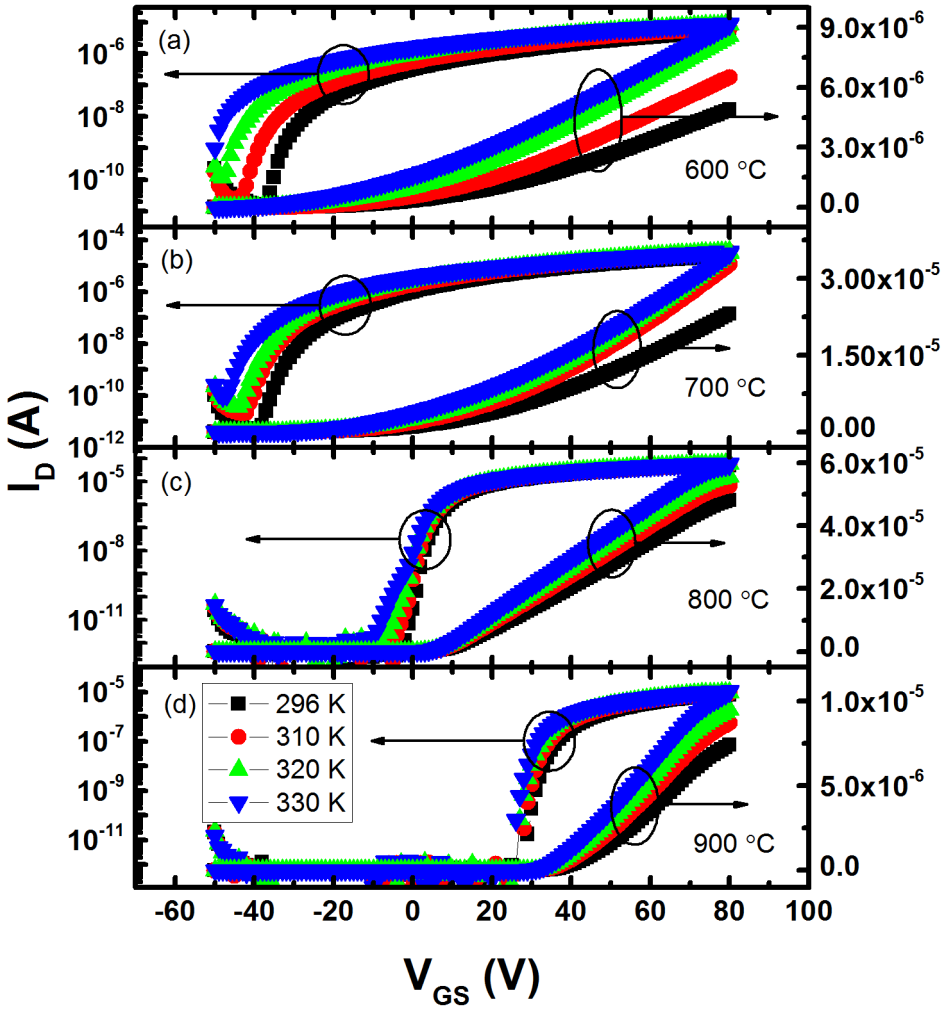


Figure 4.11: Temperature-dependent transfer I-V curves for representative TFTs with ZnO layers annealed at (a) 600, (b) 700, (c) 800, and (d) 900 °C.

In order to determine the sub-gap DOSs, temperature-dependent I-V measurements were performed. The I_D versus V_{GS} for over 20 TFTs with channel layers annealed at different temperatures were collected by changing the measurement temperature between 296 K and 330 K. Fig. 4.11 shows I_D - V_{GS} for ZnO TFTs fabricated with different annealing temperatures. For each annealing temperature, one representative data set was chosen for plotting. As can be seen

from Fig. 4.11, I_D for ZnO TFTs under the same V_{GS} shifts systematically as the measurement temperature increases, which indicates that conduction process in these TFTs are thermally activated and the temperature-dependent I-V data can be used to determine the localized sub-gap DOSs [10][11]. Then, the I_D (especially in subthreshold regime) should obey Arrhenius equation as follows [10][11][22][23];

$$I_D = I_{DP} \times exp(\frac{-E_a}{k_B T}), \tag{4.4.4}$$

where I_{DP} is a pre-factor, E_a is the activation energy and T is the measurement temperature, respectively. From the plot of I_D (in log scale) versus 1/k_{BT} in Fig. 4.12, E_a and I_{DP} for different annealing temperatures can be extracted by linear fits to the data. The activation energy E_a represents the average energy of electrons escaping from the localized sub-gap states and this is the difference between the conduction band minimum (E_C) and the Fermi level (E_F) as shown in Fig. 4.13.

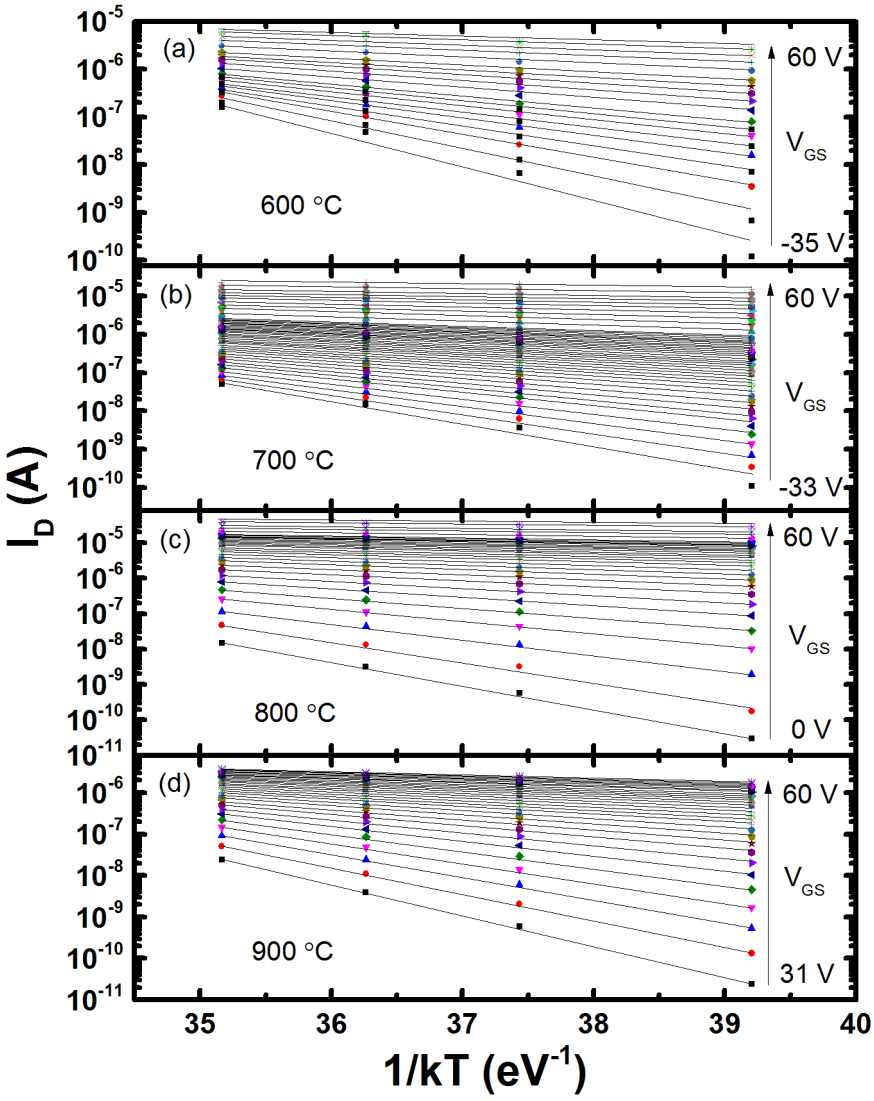


Figure 4.12: Temperature dependence of linear regime I_D for (a) 600, (b) 700, (c) 800, and (d) 900 °C annealed ZnO TFTs. The shapes are experimental data points and the lines are the fits to the Arrhenius relationship.

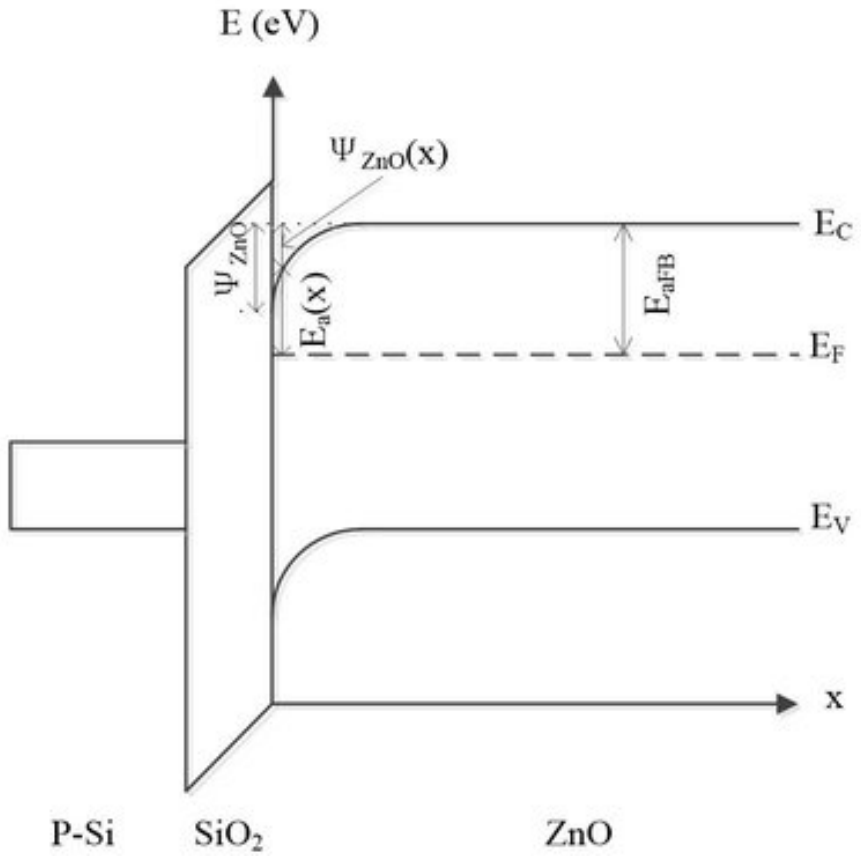


Figure 4.13: The energy band diagram of the ZnO TFT device.

In Fig. 4.14 and Fig. 4.15, both E_a and I_{DP} have independent relation with V_{GS}. And they change significantly in the subthreshold regime and vary little in the above threshold voltage regime. As can be seen from the Fig. 4.13, E_a drops rapidly as V_{GS} increases, which implies that the Fermi level E_F moves closer to E_C as V_{GS} is increased. The E_F variation is related to the DOS spread close to the E_C, which makes the determination of the localized sub-gap DOS possible. The Meyer-Neldel (MN) rule widely observed in the intrinsic material property study is also obeyed by the relation between E_a and I_{DP} in Fig. 4.16, which is described as follows [10][11]:

$$I_{DP} = I_{DPP} exp((\frac{-E_a}{k_B T}), \tag{4.4.5}$$

where I_{DPP} is the pre-factor of I_{DP} and A is the MN parameter. We can see that A and I_{DPP} have constant values in the subthreshold regime. However, A and I_{DPP} vary and A becomes smaller in the above threshold regime. As a result, for each annealing temperature, A and I_{DPP} have two defined regions which correspond to the deep states region (subthreshold regime) and

the band tail region (above threshold regime). In order to simplify the DOS calculation, we used two defined values of both A and I_{DPP} for the deep states region and the band tail region, as was employed by Chen *et al.* [10] for each annealing temperature TFT (Shown in Fig. 4.16).

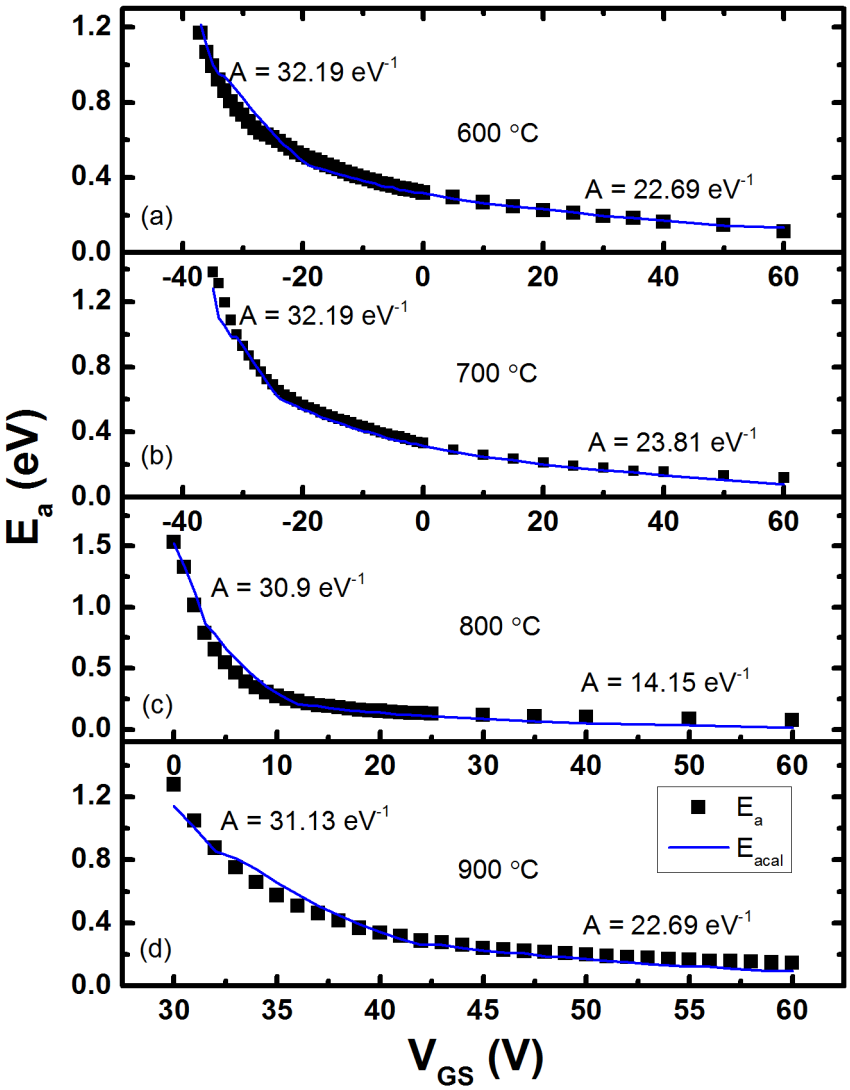


Figure 4.14: Measured activation energy (E_a) and calculated activation energy (E_{acal}) as a function of V_{GS} for (a) 600, (b) 700, (c) 800, and (d) 900 °C annealed ZnO TFTs under different MN rule parameters (A), which was determined in Fig. 4.16, in the subthreshold and the above threshold regimes. E_{acal} matches well with E_a.

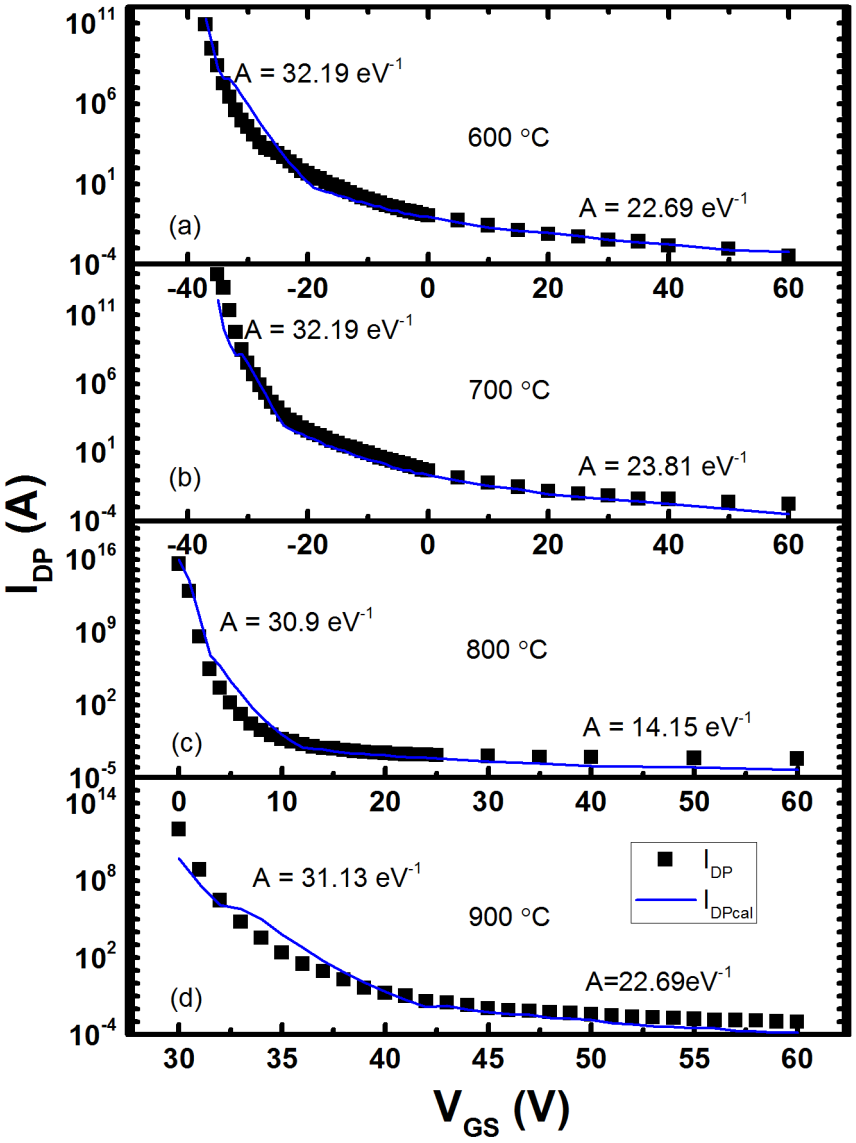


Figure 4.15: Measured drain current pre-factor (I_{DP}) and calculated pre-factor (I_{DPcal}) as a function of V_{GS} for (a) 600, (b) 700, (c) 800, and (d) 900 °C annealed ZnO TFTs. Under different MN rule parameters (A), which was determined in Fig. 4.16, in the subthreshold and the above threshold regimes. I_{DPcal} matches well with I_{DP}.

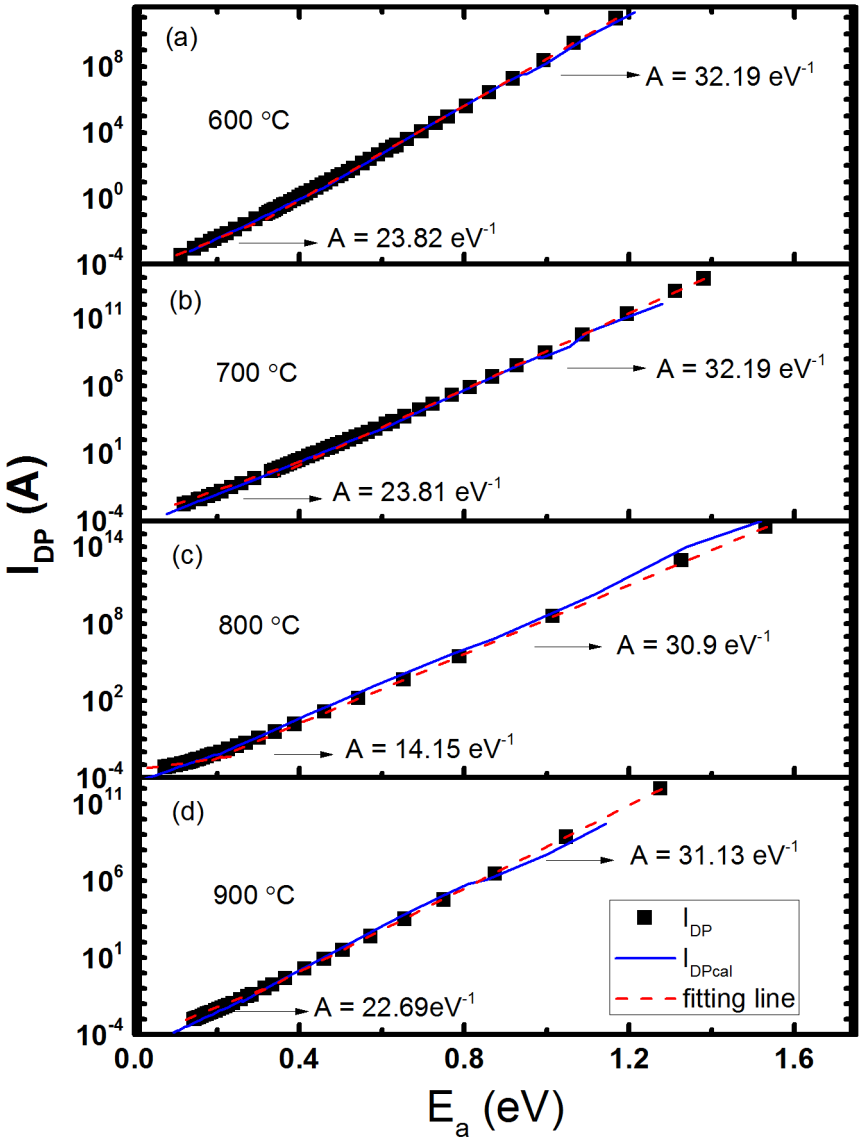


Figure 4.16: Measured drain current pre-factor (I_{DP}) and calculated pre-factor (I_{DPcal}) for (a) 600, (b) 700, (c) 800, and (d) 900 °C annealed ZnO TFTs as functions of E_a and E_{acal}, respectively. The MN rule parameter (A) was extracted in the deep states (the subthreshold regime) and tail states (the above threshold regime) by using two straight red lines to fit across the measured data points, respectively.

The procedures Chen *et al.*, Jeong *et al.*, and Kim *et al.* used to calculate the DOSs of a-IGZO TFTs were adopted [10][24][11] to extract the sub-gap density of states (DOSs) for ZnO TFTs with different annealing temperatures. By combining Eqs. (4) and (5), the expression for

I_D at a specific V_{GS} point can be rewritten as follows [10]:

$$I_D(V_{GS}) = I_{DPP} exp[(A - \beta)E_a(V_{GS})], \tag{4.4.6}$$

where

$$\beta = 1/(k_B T)$$

According to Fig. 4.13, E_a is determined by both V_{GS} and the distance x of the interface between ZnO and SiO_2. As a result, the extracted thermal activation energy at a specific V_{GS} point ($E_a(V_{GS})$) in Fig. 4.14 can be treated as the average effect on I_D created by the thermal activation energy along x (E_a(x)). Then, $I_D(V_{GS})$ can be described as below [10]:

$$I_D(V_{GS}) = \frac{I_{DPP}}{d_{ZnO}} \int_0^{d_{ZnO}} exp[(A - \beta)E_a(x)]d_x, \tag{4.4.7}$$

where d_{ZnO} is the thickness of the ZnO channel layer. E_a(x) can also be written as E_{aFB} - ψ_{ZnO}(x), where E_{aFB} is the activation energy under flat band condition and ψ_{ZnO}(x) is the band bending. By combining with Eqs. (7), the expression for I_D can be rewritten as follows [10]:

$$I_D(V_{GS}) = \frac{I_{DPP}}{d_{ZnO}} \int_0^{d_{ZnO}} exp[(A - \beta)\psi_a(x)]d_x, \tag{4.4.8}$$

where I_{FB} is the flat band current which can be written as follows[17];

$$I_{FB} = I_{DPP} exp[(A - \beta)E_{aFB}] \tag{4.4.9}$$

In order to determine ψ_{ZnO}(x) and the corresponding charge density (n_{ZnO}(x)) caused by the density of states in the ZnO channel layer [25], the Poisson equation needs to be satisfied in the electric field with varying V_{GS}. The corresponding Poisson equation can be written as follows [10]:

$$\frac{d^2\psi_{ZnO}(x)}{dx^2} = \frac{q n_{ZnO}(\psi_{ZnO}(x))}{\xi_{ZnO}\xi_0}, \tag{4.4.10}$$

where q is the absolute value of the electronic charge, ϵ_{ZnO} is the dielectric constant of ZnO, and ξ_0 is the permittivity in vacuum. By using Chen $et\ al.$'s self-consistent procedure, we can derive the expression for the surface band bending ($\psi_{ZnO_S}(V_F)$) as follows [10][11]:

$$\begin{aligned} exp[\beta - A)\psi_{ZnO_S}(V_F)] - (\beta - A)\psi_{ZnO_S}(V_F) - 1 = \\ \frac{\beta - A}{I_{FB}} \times \frac{d_{ZnO}}{d_{SiO_2}} \times \frac{\xi_{SiO_2}}{\xi_{ZnO}}[V_F I_D(V_F) - \int_0^{V_F} I_D(V_F^{'}) dV_F^{'}] \end{aligned} \tag{4.4.11}$$

where V_F is the difference between V_{GS} and the flat band voltage (V_{FB}), d_{SiO2} and ξ_{SiO_2} are the thickness and dielectric constant of the SiO_2 layer, respectively. Meanwhile, the corresponding surface charge density ($n_{ZnO_S}(\psi_{ZnO})$) can be presented as [10][11]:

$$n_{ZnO_S}(\psi_{ZnO_S}) = \frac{\xi_{SiO_2}\xi_0}{q d_{SiO_2} d_{ZnO}} \times \frac{I_{FB} exp[\beta - A)\psi_{ZnO_S}] - 1}{((dI_D)/(dV_F))} \tag{4.4.12}$$

Then, the calculated $\psi_{ZnO_S}(V_F)$ and $n_{ZnO_S}(\psi_{ZnO})$ under the subthreshold regime for different annealing temperatures are plotted in Fig. 4.17 and Fig. 4.18, respectively. $\psi_{ZnO_S}(V_F)$ increases with the same V_F as annealing temperature increases from 600 °C to 800 °C, and the $\psi_{ZnO_S}(V_F)$ remains the same level of values between 800 °C and 900 °C. In Fig. 4.18, $n_{ZnO_S}(\psi_{ZnO})$ as the opposite trend as annealing temperature changes from 600 °C to 800 °C, and it keeps the same level between 800 °C and 900 °C as well. However, the calculated $\psi_{ZnO_S}(V_F)$ and $n_{ZnO_S}(\psi_{ZnO})$ above the threshold regime does not follow the same trend. Since the DOS calculation in this regime cannot be valid as will be explained in the later section, the corresponding $\psi_{ZnO_S}(V_F)$ and $n_{ZnO_S}(\psi_{ZnO})$ plots are not included in this paper. In addition, the appropriate V_{FB} should be determined in order to extract valid ψ_{ZnO_S}, n_{ZnO_S} and the corresponding DOS which will be discussed later. By comparing the calculated activation energy (E_{acal}) with the experimental activation energy (E_a), we can choose the suitable V_{FB} for the extraction of ψ_{ZnO_S} and n_{ZnO_S}. The E_{acal} equation is described as follows [10][11]:

$$\begin{aligned} E_{acal}(V_{GS}) = E_{aFB} - \frac{I_{FB}}{(I_D(V_{GS}) d_{ZnO})} \frac{\sqrt{(\xi_{ZnO}\xi_0)q}}{\times} \\ \int_0^{\psi_{ZnO_S}} \frac{(\psi exp[(\beta - A)\psi])}{(\sqrt{(2\int_0^y n_{ZnO_S}(\psi')d\psi')}} d\psi \end{aligned} \tag{4.4.13}$$

where E_{aFB} is the flat band energy and can be rewritten from equation (9);

$$E_{aFB} = \frac{(ln(I_{FB}/I_{DPP}))}{(A-\beta)} \tag{4.4.14}$$

The I_{FB} can be directly obtained by interpolation at V_{FB} from I_D. From Fig. 4.14, a proper V_{FB} was chosen for each ZnO TFT with different annealing temperatures, and E_{acal} was well matched with E_a. The calculated pre-factor (I_{DPcal}) derived from E_{acal} is written as [10];

$$I_{DPcal}(V_{GS}) = I_D(V_{GS})exp[\beta E_a(V_{GS})] \tag{4.4.15}$$

which is also consistent with I_{DP} in Fig. 4.15. The corresponding MN rule for E_{acal} and I_{DPcal} is consistent with the one for E_a and I_{DP}, as is shown in Fig. 4.16. After choosing the proper V_{FB}, the final DOS distribution D (E) can be extracted under the assumption of 0-Kelvin Fermi statistics from the following expression [10][11];

$$D(E) = |\frac{dn_{ZnO_S}(_{ZnO_S})}{d\psi_{ZnO_S}}|_{_{ZnO_S}=E} \tag{4.4.16}$$

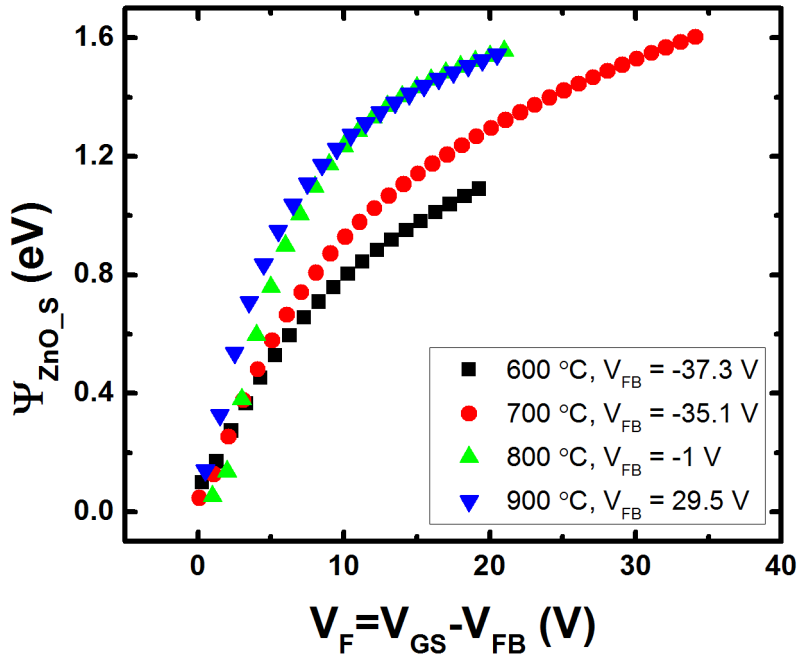


Figure 4.17: Extracted band bending at the ZnO-SiO_2 interface (W_{ZnO}) for 600, 700, 800, and 900 °C annealed ZnO TFTs as a function of V_F.

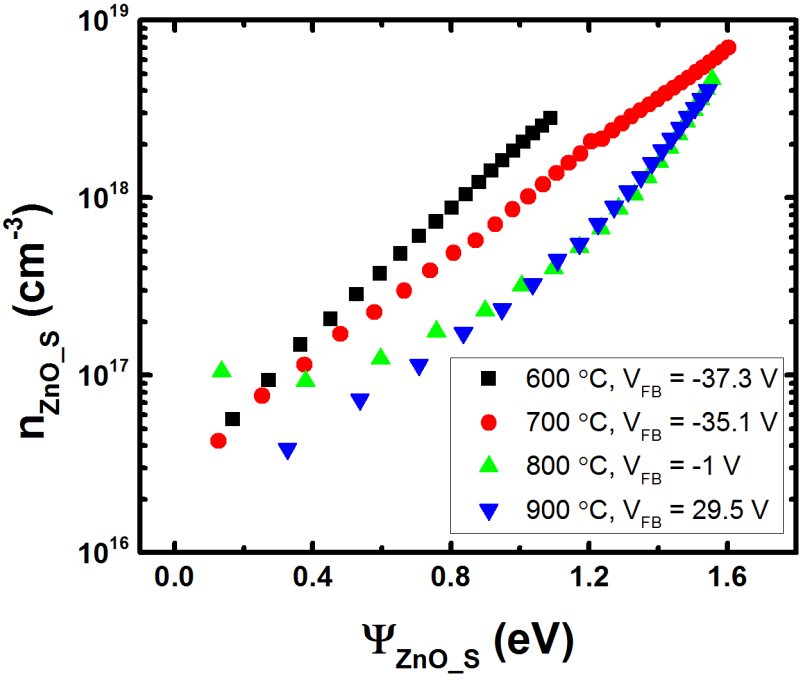


Figure 4.18: Induced charge density (n_{ZnO}) for 600, 700, 800, and 900 °C annealed ZnO TFTs as a function of V_F.

Finally, DOSs were calculated for both the subthreshold and above threshold regimes for all ZnO TFTs with different annealing temperatures and were plotted in Fig. 4.19 and Fig. 4.20. As can be seen in Fig. 4.19, the DOSs calculated in the subthreshold regime reduces as annealing temperature increases from 600 °C to 800 °C and the DOSs keep the same value between 800 °C and 900 °C, which is consistent with the D_{it}, as is analyzed before. Compared with D_{it}, which shows only the qualitative interface trap density information, the extracted D (E) provides the localized subgap states energy distributions [26].

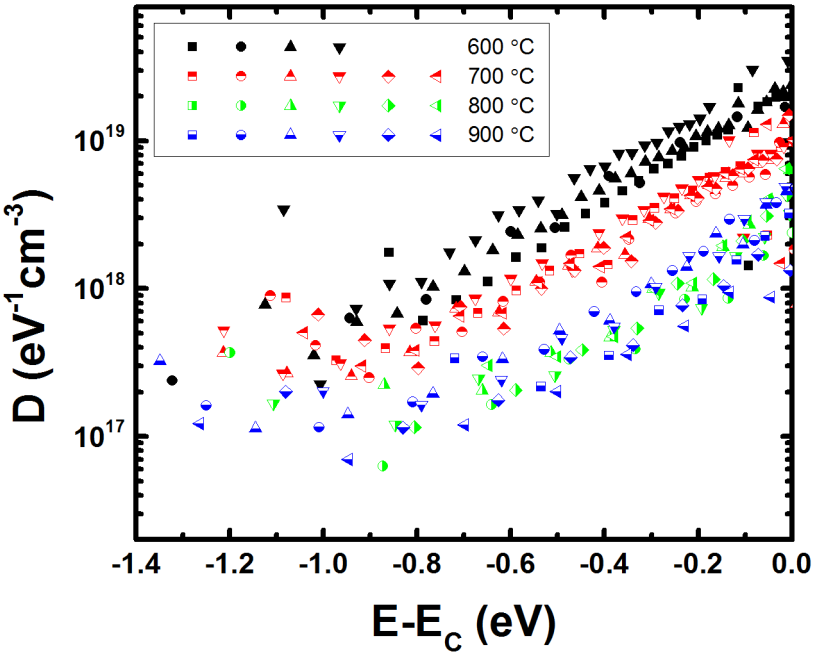


Figure 4.19: Calculated DOSs from the subthreshold regime for all measured ZnO TFTs with different annealing temperature. The DOSs of 600, 700, 800, and 900 °C annealed ZnO TFTs are black, red, green, and blue marks, respectively. The marks with different shapes represent different transistors that have been measured.

According to Chen *et al.*, the DOSs extracted from the above threshold regime cannot be valid due to the following reasons [10]; First, the free carrier concentration which was ignored in Eq. (16) for calculating the DOSs in the subthreshold regime should be considered for extracting DOSs from above threshold regime. Second, the characteristic energy is too close to the measuring temperature. As a result, the 0-Kelvin Fermi statistics assumption would introduce an error when calculating the final results. Regardless of these limitations, DOSs

extraction in the above threshold regime can still offer a deep intuitive understanding of the annealing temperature effect on the electrical properties of ZnO TFTs. As is presented in Fig. 4.20, the calculated DOSs in the above threshold regime is larger than those determined from subthreshold regime and exhibit a decreasing trend with increasing annealing temperature.

According to the experimental results obtained, it was found that increasing annealing temperature can improve the crystal quality of ZnO and reduce the DOSs, this also results in the field effect mobility increasing [27], but annealing at a very high temperature (i.e. 900 °C) will not further improve the performance of ZnO TFTs and can even cause the degradation. It was hypothesized that a very high temperature annealing can be detrimental due to the following reasons; 1) Interstitial Zn may evaporate at a temperature above 800 °C, resulting in the reduction of the concentration of electrons produced by ionization of Zn interstitials [20]. 2) Annealing in the oxidizing atmosphere can fill oxygen vacancies which act as donors and reduce the charge carrier concentration [28][29], thus reducing electrical conductivity and increase the threshold voltage [29]. 3) Electron mobility can be reduced from very high temperature annealing. The SEM image shows non-continuous film coverage for the samples annealed at 900 °C, which can be used to explain the electron mobility degradation. Combined with the I-V analysis and the results on DOS calculation, it can be tentatively concluded that 800 °C annealing temperature can generate the highest quality of ZnO film with the lowest DOSs and TFT with highest mobility.

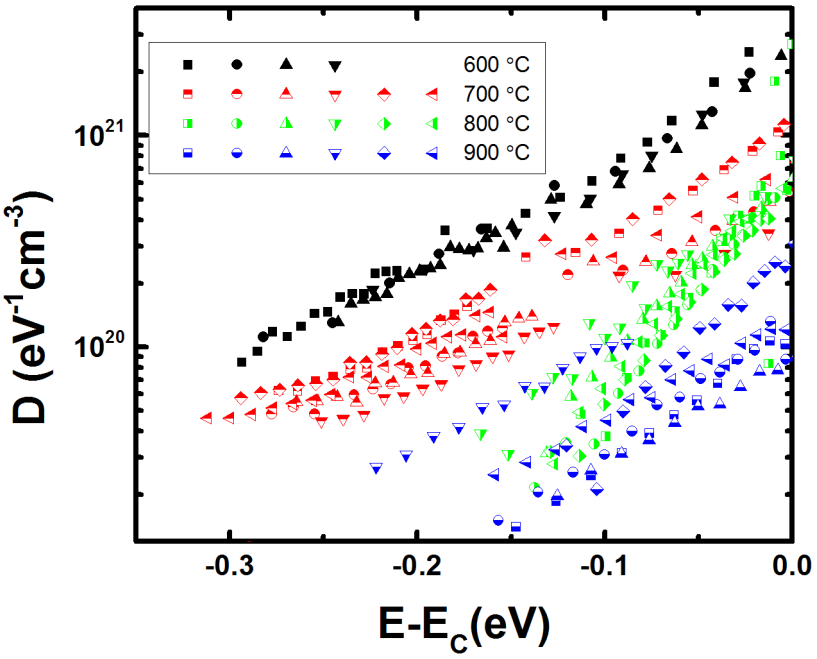


Figure 4.20: Calculated DOSs from the above threshold regime for all measured ZnO TFTs with different annealing temperatures. The DOSs of 600, 700, 800, and 900 °C annealed ZnO TFTs are black, red, green, and blue marks, respectively. The marks with different shapes represent different transistors that have been measured.

4.5 Summary

The ZnO channel layers were deposited on an oxidized Si wafer via sol-gel process and were annealed at different temperatures. It was found that the annealing temperature greatly affects the performance of sol-gel derived ZnO TFTs. With increasing annealing temperature, crystallite size became larger and hence the amount of grain boundary defects reduced which must have a strong influence on modulating the density of states, V_{on} (and V_T) increases and off current drops drastically. The SS and corresponding D_{it} decrease as the annealing temperature increases. However, the μ_{FET} and the output current peak at 800 °C and drop upon further temperature increase. The temperature dependent field effect measurement was used to gain an insight on the annealing temperature effect on ZnO TFTs electrical characteristics. By combing the MN rule and applying the self-consistent procedure in a-IGZO TFTs analysis, the DOSs of different temperatures annealed sol-gel derived ZnO TFTs were successfully extracted. The results show that DOSs decrease with annealing temperature increase in general, but too high

of a temperature anneal may not be beneficial in reducing DOSs. It was found that the TFT with ZnO layers annealed at 800 deg. C for one hour shows the best electrical performance.

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Chapter 5

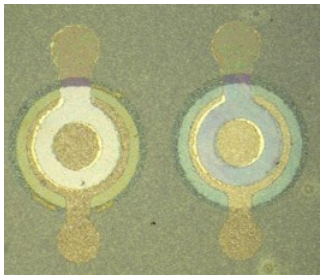
ZnO based logic circuits fabrication and testing

ZnO TFT has been deeply studied since its merits show great advantages for electronics application. The logic circuits based on ZnO TFTs attract a lot of attentions for new applications, such as radiation-hard logic circuits, transparent logic circuits, etc. However, unstable and unreliable p-type ZnO TFTs limits the ZnO TFTs logic circuits application (Chapter 1). In this chapter, two different designs for ZnO logic circuits have been introduced and the basic ZnO inverter circuit has been realized.

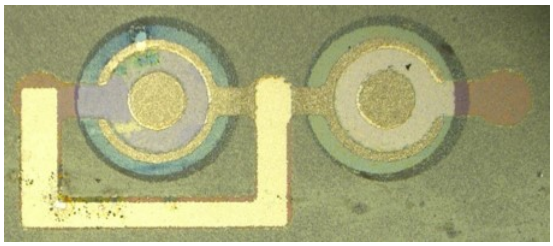
5.1 Patterned gate ZnO TFTs and the related logic circuits characterization

The design and fabrication of ZnO logic circuits were introduced in Chapter 1 and 2. The optical images for two types of patterned gate ZnO TFTs and the related logic circuits shown in Fig. 5.1 and Fig. 5.2 were characterized via HP 4156A semiconductor parameter analyzer. Because of the complicated fabrication process and the low quality of dielectric layer (SiO_2) deposited through LPCVD, the patterned bottom gate ZnO TFTs did not show a good reliability. The devices are easy to be broken down with large gate voltage (V_{GS}) and most transistors did not function properly. Fig. 5.3 shows transfer IV curves of the best working patterned bottom ZnO TFTs. Sol-gel derived and RF magnetron sputtered ZnO TFTs demonstrate normally-off and normally on characteristics. The extracted V_T for the two TFTs are -2.8 and 2.7 V for normally-on and normally-off devices, respectively. However, as shown in Fig. 5.4, the gate leakage current (I_G) for sol-gel derived and RF magnetron sputtered ZnO TFTs can reach as high as 10^{-7} and 10^{-6} A, separately. The high gate leakage in the ZnO logic circuit, such as

the NOT gate, will flow into ZnO channel and make V_{out} larger than V_{DD}, which results in a circuit failure.

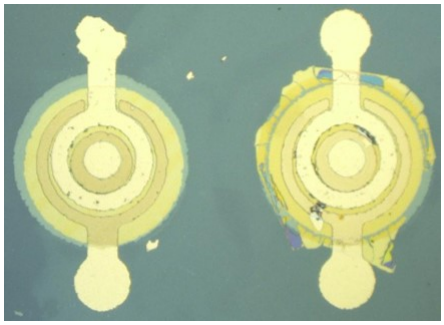


(a) Circle TFTs

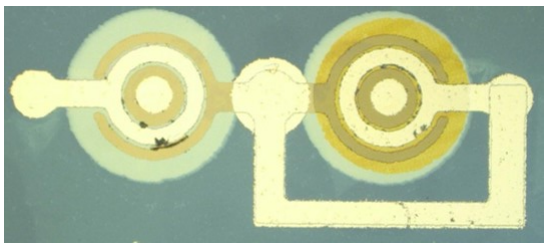


(b) Circle NOT gate

Figure 5.1: Images for Patterned Bottom Gate TFTs and Circuits.



(a) Circle TFTs



(b) Circle NOT gate

Figure 5.2: Patterned top gate ZnO TFTs and circuits

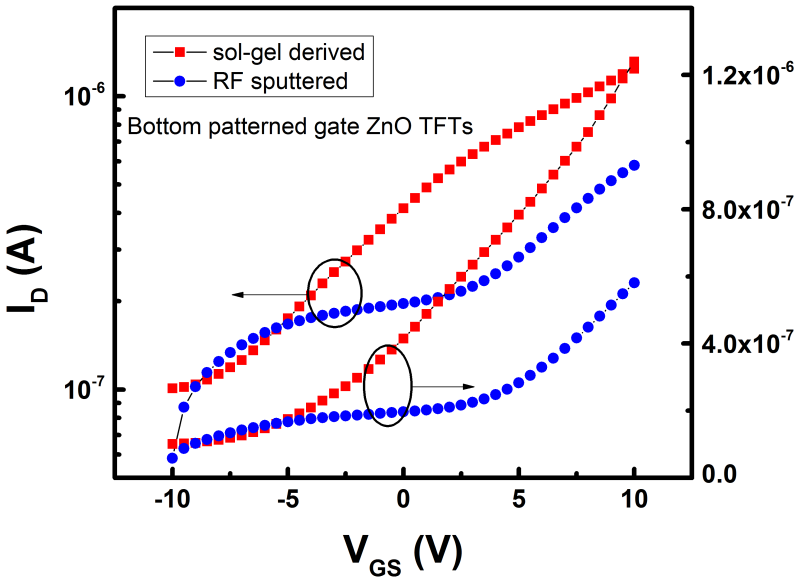
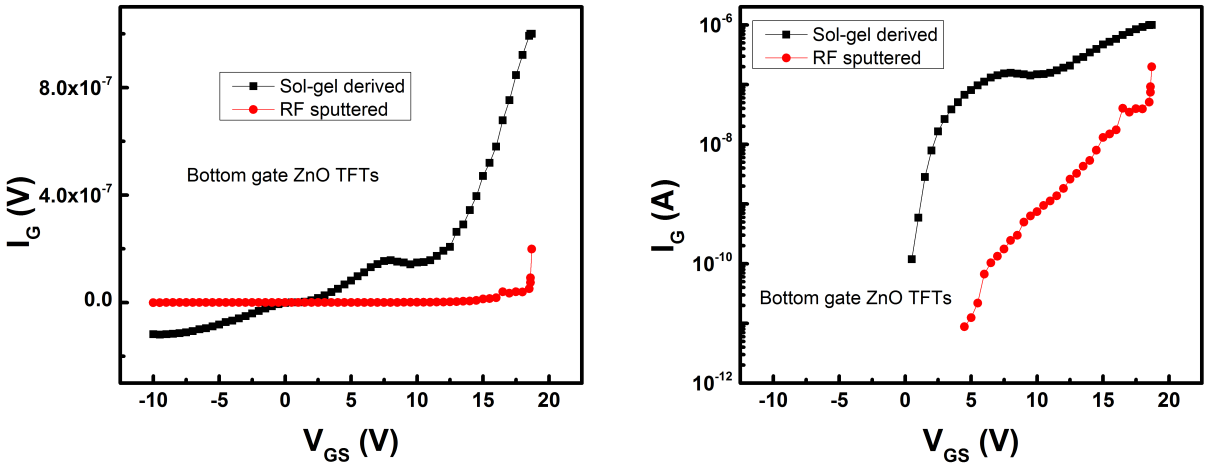


Figure 5.3: Transfer IV curves for patterned bottom gate ZnO TFTs.



(a) Linear scale

(b) Log scale

Figure 5.4: Gate leakage current for patterned bottom gate ZnO TFTs in linear (a) and log (b) scale.

To overcome the shortcomings of the patterned bottom gate ZnO TFTs and logic circuits, such as low breakdown voltage and high gate leakage, the patterned top gate ZnO TFTs and logic circuits have been brought out. The details of design and fabrication have been described in Chapter 2. A home-made ALD system has been used for high-k and dense Al_2O_3 dielectric layer deposition. Fig. 5.5 and 5.6 demonstrate the transfer IV curves and gate leakage current for best working patterned top gate ZnO TFTs. V_T for sol-gel derived and RF magnetron sputtered top gate ZnO TFTs are -1 V and 10 V, respectively. I_G was maintained at 10^{-11} A level. However, because of the limitation of the home-made ALD system, the diffusion of the aluminum into ZnO during Al_2O_3 deposition introduced free electrons and raised the off current. As a consequence, the on/off ratios for both TFTs were very low and the corresponding ZnO NOT gate circuit was not working correctly. Table 5.1 summarized the intrinsic parameters for both patterned bottom gate and top gate ZnO TFTs. Compared to the conventional unpatterned bottom gate ZnO TFTs, patterned gate ZnO TFTs show extremely small on/off ratio. The SS and corresponding D_{it} for patterned bottom gate sol-gel derived, patterned top gate sol-gel derived and patterned top gate RF magnetron sputtered ZnO TFTs demonstrate large value, which indicates that the interface defects level is too high for making working transistors. Even though SS and D_{it} for patterned bottom gate RF magnetron sputtered ZnO TFT are maintained

at a reasonable level, the high gate leakage current caused it not suitable for implementing in ZnO logic circuits.

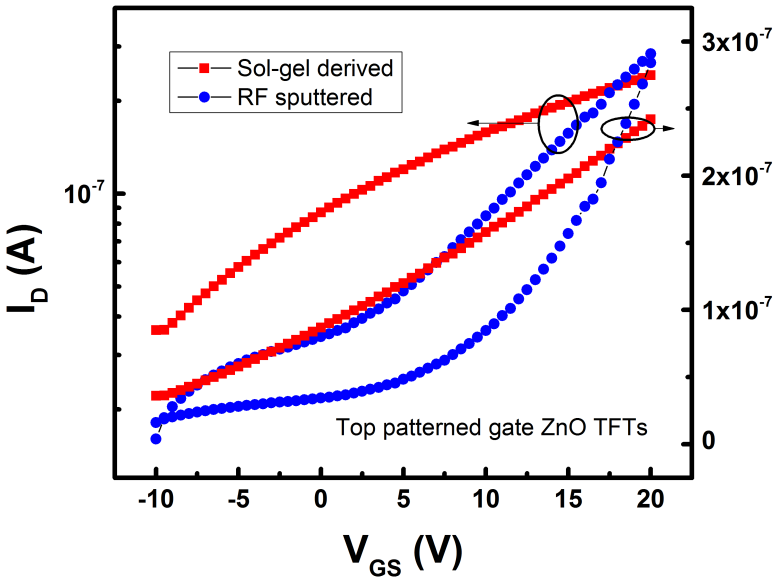
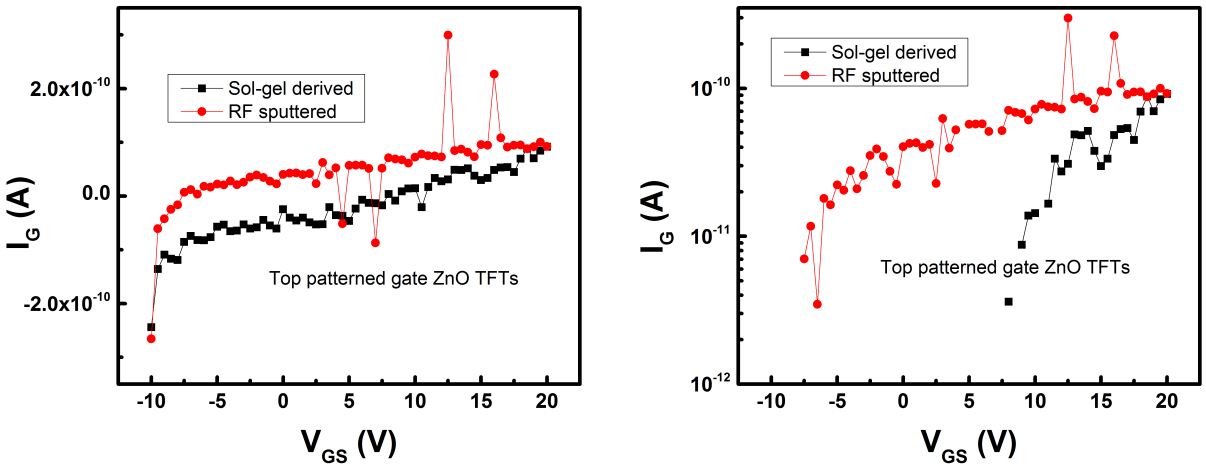


Figure 5.5: Transfer IV curves for patterned top gate ZnO TFTs.



(a) Linear scale

(b) Log scale

Figure 5.6: Gate leakage current for patterned top gate ZnO TFTs in linear (a) and log (b) scale.

Type	V_T (V)	μ (cm^{-2}/VS)	on/off	SS (V/decade)	D_{it} ($eV^{-1}cm^{-2}$)
Bottom gate sol-gel derived ZnO TFT	-2.8	0.303	20	15.0521	2.04×10^{13}
Bottom gate RF sputtered ZnO TFT	2.7	0.193	200	2.7648	3.68×10^{12}
Top gate sol-gel derived ZnO TFT	-1	0.026	7	21.8254	2.43×10^{14}
Top gate RF sputtered ZnO TFT	10	0.09	18	21.6534	2.414×10^{14}

Table 5.1: Intrinsic parameters for the two types of patterned gate ZnO TFTs

Based on the characterization, patterned gate ZnO TFTs with not-optimized home-made deposition system and complicated fabrication process did not show a good result for making working logic circuits.

5.2 Alternative ZnO logic circuits

Combing the patterned gate sol-gel derived and RF magnetron sputtered ZnO TFTs and fabricating them on the same piece of substrate is really a great attempt to make compact and easily handled logic circuit. However, the not-optimized fabrication system and process did not produce good working transistors and realize the basic function of logic circuits. Therefore, an alternative ZnO logic circuits design, fabrication, and characterization have been carried out.

5.2.1 ZnO TFTs and logic circuits packaging

The reason for making the patterned gate for ZnO TFTs is to make it possible to control individual load and drive transistors, independently on the same substrate. If controlling two devices on the same wafer is not the concern, the wire bonding packaging technique can be involved to make working ZnO logic circuits.

Wire bonding is a technique that utilizes thin metallic wires (usually small gold or aluminum wires) with 20 to 50 um diameter to connect devices to the metal pads on the outside package holder [1]. In our case, wire bonding was only used for connecting load and drive devices on the different substrate. Before that, a sample with individual devices was wedge wire bonded to a chip carrier to test the reliability and stability of this technique.

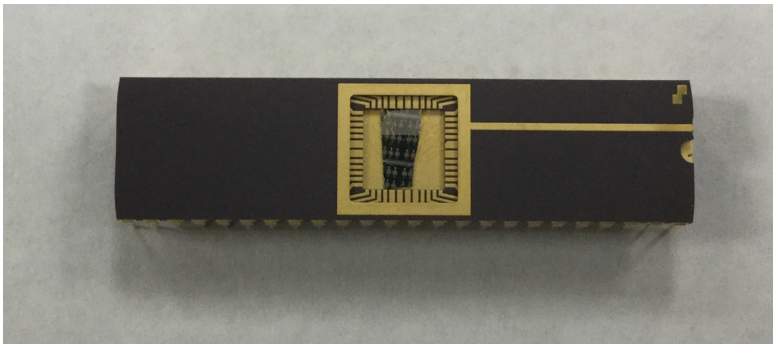


Figure 5.7: Wire bonded sample

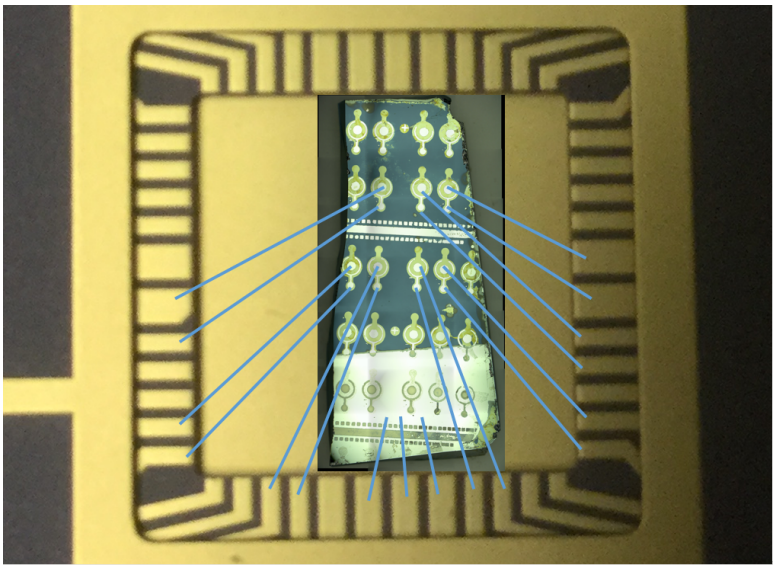


Figure 5.8: Schematic connections for wire bonded sample and chip carrier.

70 nm RF magnetron sputtered 700 C annealed ZnO TFTs with Al metallic contacts were fabricated. The wire bonded ZnO TFTs sample with chip carrier C-DIP 48pin KD-82293-C and the schematic connections between sample and chip carrier are shown in Fig. 5.7 and 5.8, respectively. The bottom of the sample was etched to expose the pure silicon layer, and an Al layer was evaporated to make gate electrode. The gold wires connected the source and drain

contacts and gate electrode from the sample to the gold pad. After that, the device characterization was carried out in a dark environment at room temperature with Keithley 6517 voltage source.

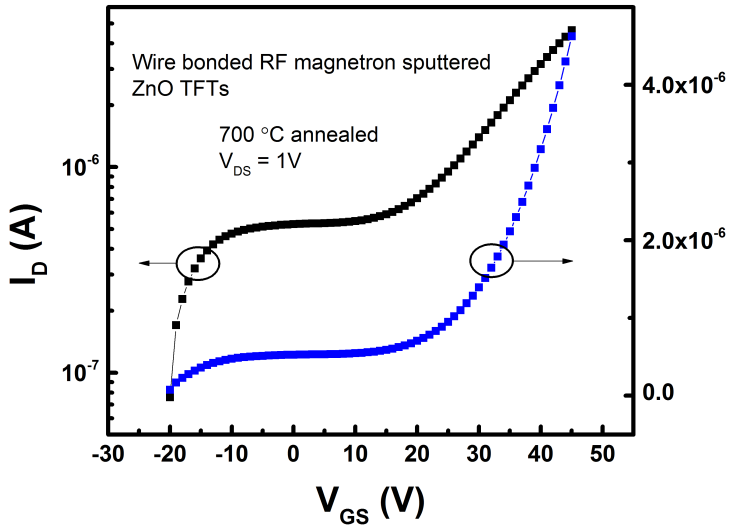


Figure 5.9: Transfer IV curves for the representative wire bonded ZnO TFT.

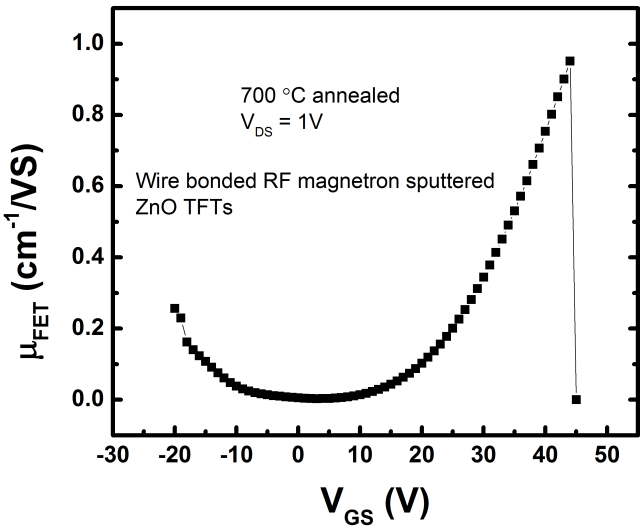


Figure 5.10: Field effect mobility for the representative wire bonded ZnO TFT.

Fig. 5.9 and 5.10 demonstrate the transfer IV curves and μ_{FET} for a representative ZnO TFT, which show that wire bonded ZnO TFT work correctly. Compared to the patterned gate ZnO TFTs, μ_{FET} for wire bonded sample can reach 1 cm^{-1}/VS, which is relatively high for

ZnO TFTs. The gate current leakage, as shown in Fig. 5.11, is lower than 10^{-10} A, which is not high. The output IV curves are plotted in Fig. 5.12. Despite the high off-current, the output IV curves demonstrate a good shape for a working transistor.

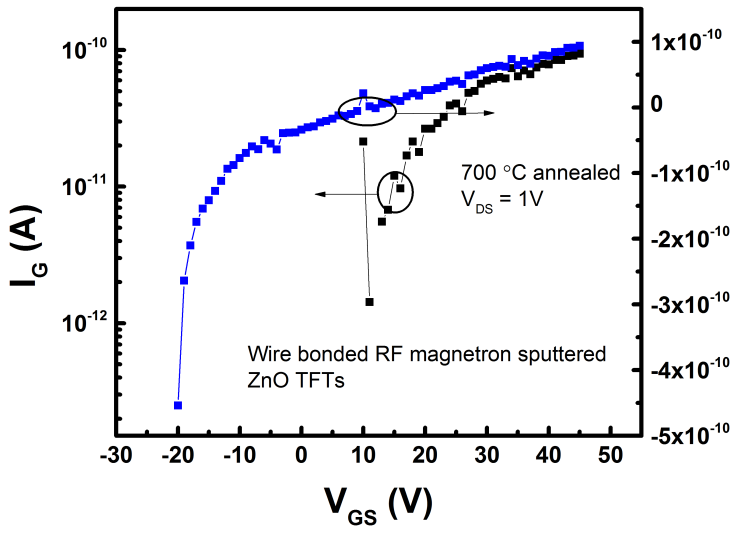


Figure 5.11: Gate leakge current for the representative wire bonded ZnO TFT.

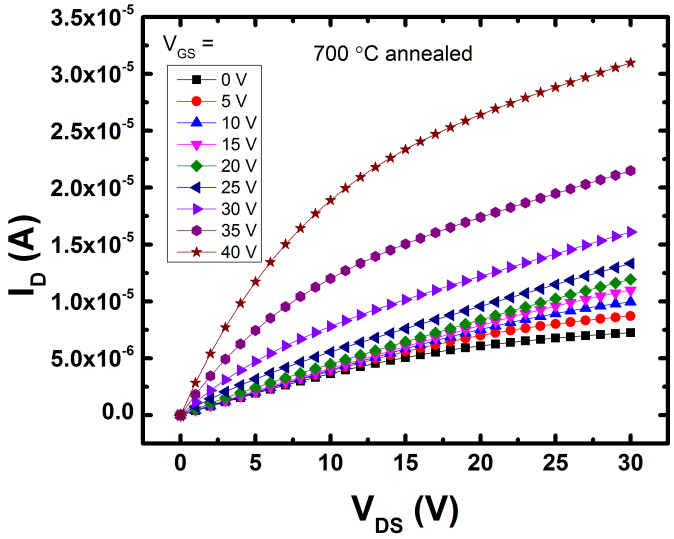
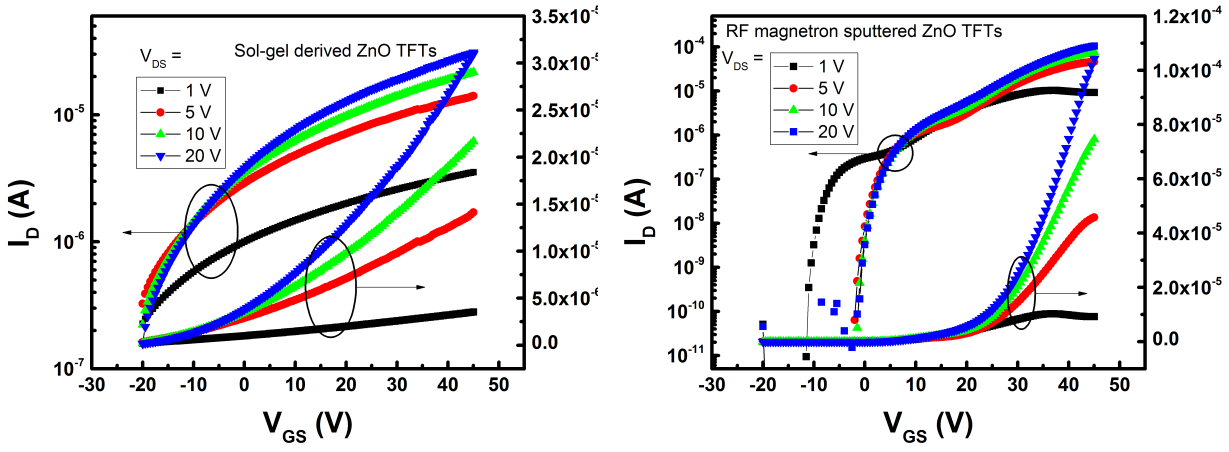


Figure 5.12: Output IV curves for the representative wire bonded ZnO TFT.

As the wedge wire bonding technique was verified, a new sol-gel derived ZnO TFTs sample and a new RF magnetron sputtered ZnO TFTs sample has been fabricated. Both of them have the unpatterned gate and were used to implement logic circuit *via* wedge wire bonding.

Before NOT gate circuits characterization, the sol-gel derived and RF magnetron sputtered ZnO TFTs were tested to verify that each component was working correctly.

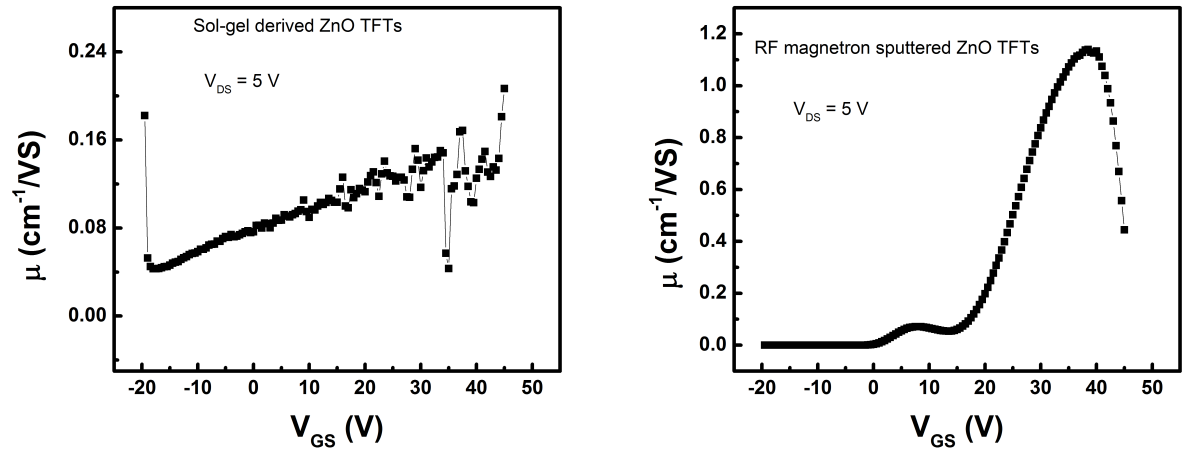


(a) Sol-gel derived ZnO TFTs

(b) RF magnetron sputtered ZnO TFTs

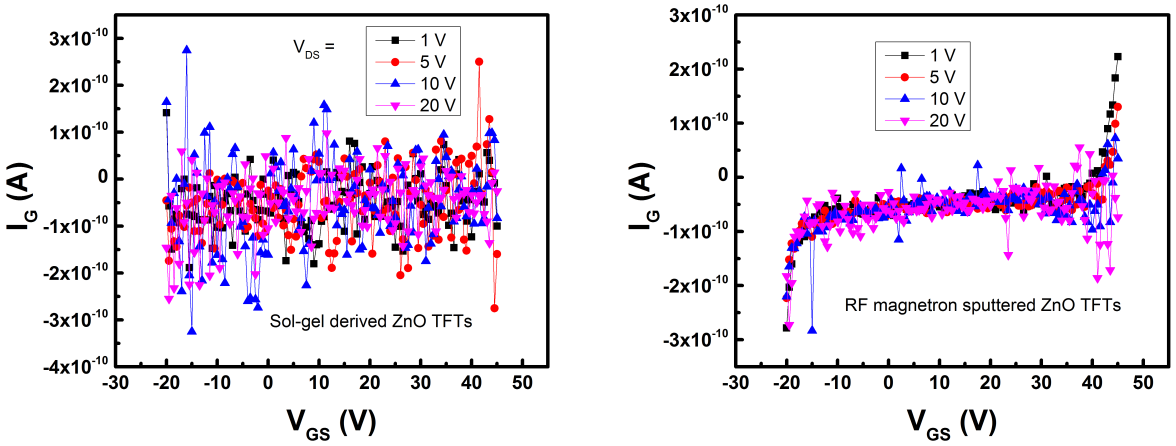
Figure 5.13: transfer IV curves for the representative sol-gel derived ZnO TFT as the load device and RF magnetron sputtered ZnO TFT as the drive device for alternative logic circuit.

As shown in Fig. 5.13, sol-gel derived ZnO load TFT and RF magnetron sputtered ZnO drive TFT were measured under different V_{DS}. It was observed that the drain current increases with increasing V_{DS}. V_T for load and drive ZnO TFTs at V_{DS} = 1 V are -12 V and 10 V, respectively. The μ_{FET}s in linear region (V_{DS} = 5 V) for ZnO TFTs were extracted in Fig. 5.14. μ_{FET} for drive ZnO TFT is ten times larger than the for the load ZnO TFT, which makes load ZnO TFT work as a resistor with a large resistance and the drive ZnO TFT easy to be turned off. Gate leakage currents were also plotted in Fig. 5.15, which is at a low level of 10-11 A. Finally, the output I_D-V_{DS} is shown in Fig. 5.16 with V_{GS} ranging from -40 V to 40 V. After the careful analysis, we confirm that the load and drive ZnO TFTs can be used to implement ZnO logic circuit.



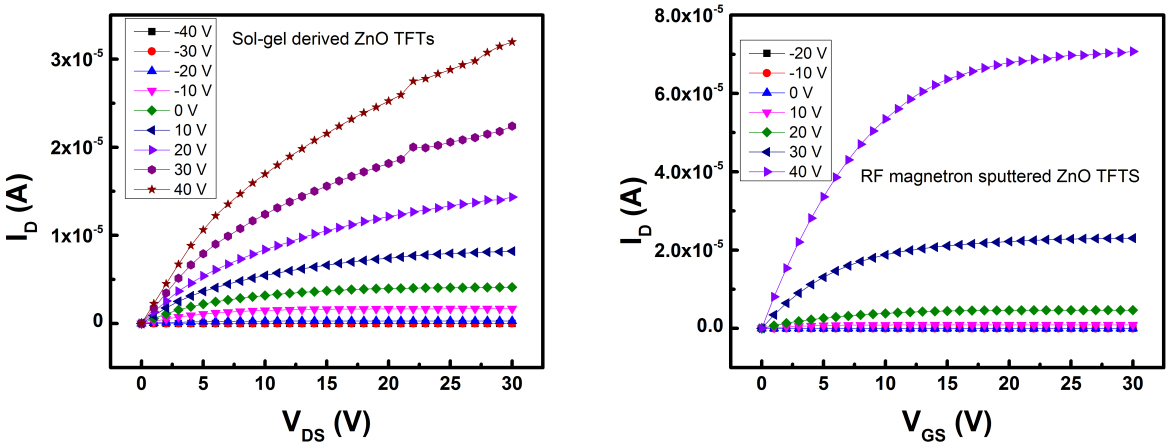
(a) Sol-gel derived ZnO TFTs (b) RF magnetron sputtered ZnO TFTs

Figure 5.14: μ_{FET} for the representative sol-gel derived ZnO TFT as the load device and RF magnetron sputtered ZnO TFT as the drive device for alternative logic circuit.



(a) Sol-gel derived ZnO TFTs (b) RF magnetron sputtered ZnO TFTs

Figure 5.15: Gate leakage current for the representative sol-gel derived ZnO TFT as the load device and RF magnetron sputtered ZnO TFT as the drive device for alternative logic circuit.



(a) Sol-gel derived ZnO TFTs

(b) RF magnetron sputtered ZnO TFTs

Figure 5.16: Output IV curves for the representative sol-gel derived ZnO TFT as the load device and RF magnetron sputtered ZnO TFT as the drive device for alternative logic circuit.

5.2.2 Alternative ZnO logic circuits testing

The schematic logic circuit structure combines the sol-gel derived ZnO TFT with RF magnetron sputtered ZnO TFT, as shown in Fig. 5.17. The sol-gel derived and RF magnetron sputtered ZnO TFTs were treated as a load and a driver component, respectively. As a working NOT gate circuit, the drain and gate of sol-gel derived ZnO TFT are biased via two fixed supply voltages (V_{DD} and V_L) and the source and gate of RF sputtered ZnO TFT are grounded and biased by a changing input voltage (V_{IN}). Finally, the output voltage (V_{OUT}) is set between the source of the load and the drain of the drive, separately. The optical microscopic image for wire bonded samples is shown in Fig. 5.18. The source contact of the sol-gel derived ZnO TFT was bonded to the drain contact of the RF magnetron sputtered ZnO TFT. Compared to Donghyuk Yeom $et\ al.$'s ZnO nanowire NOT logic circuit [2], our NOT logic circuit composed of thin-film ZnO TFTs shows an advantage of industrial application.

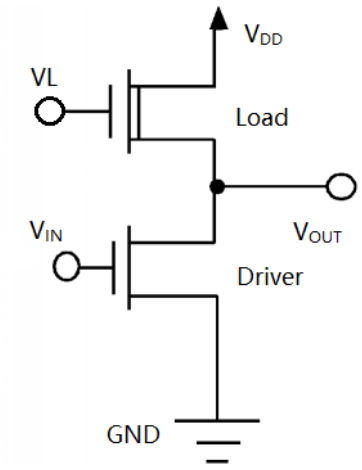
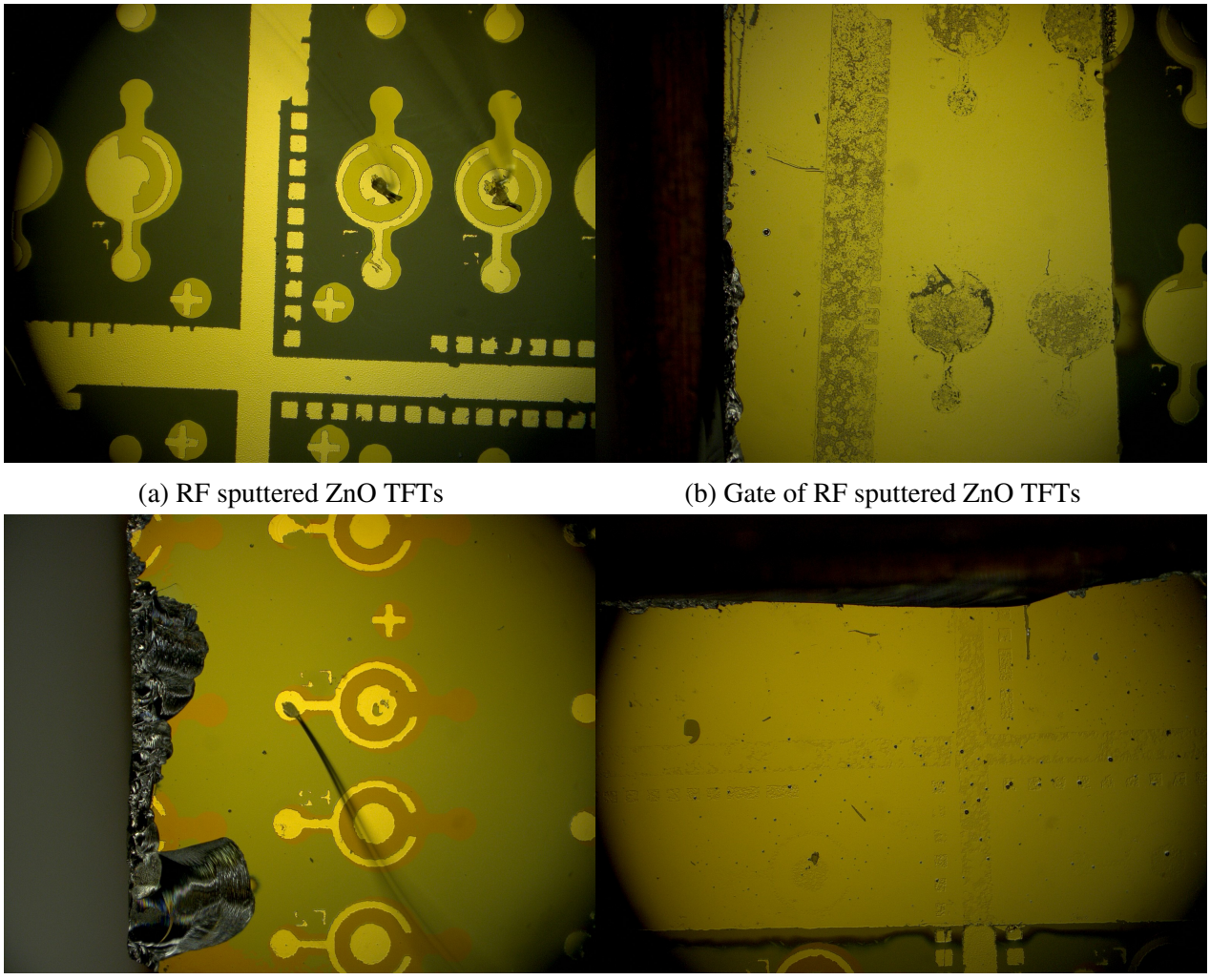


Figure 5.17: Schematic alternative NOT gate structure



(a) RF sputtered ZnO TFTs (b) Gate of RF sputtered ZnO TFTs

(c) Sol-gel derived ZnO TFTs (d) Gate of sol-gel derived ZnO TFTs

Figure 5.18: Wire bonded ZnO NOT gate.

The logic gate circuit operation processes are described as follows: 1) Maintaining V_L at 0 V and choosing three values for V_{DD} (1, 10 and 20 V), the NOT gate circuit was characterized with a range of V_{IN} from -10 V to 40 V. The operation result can be seen in Fig. 5.19. When V_{IN} was around -10 V, the normally-off drive ZnO TFT worked in the fully depletion region and compared to normally-on load ZnO TFT without gate bias, the channel resistance of the drive ZnO TFT is larger than that of the load. Then, the most voltage drop occurs at the drive TFT instead of load TFT. The V_{OUT} at this point is in the high state. However, the drive TFT started to turn on when V_{IN} was larger than V_{on} (-3 V) and fully turn on after V_{IN} became larger than V_T (10 V). As a consequence, the NOT gate began to be turned off at -3 V and work in a low state for V_{IN} larger than 10 V. The different values of V_{DD} determined the values of NOT gate on-off states.

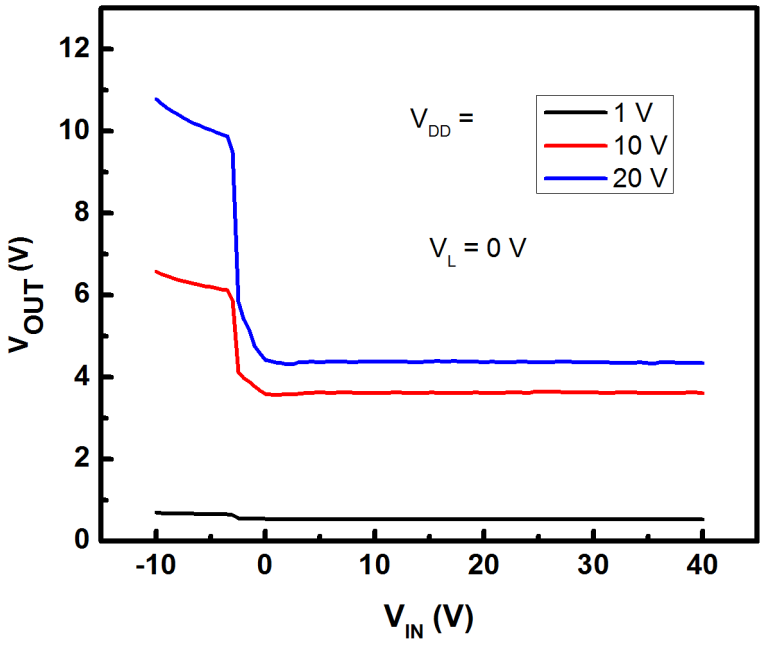


Figure 5.19: Voltage transfer characteristics of the NOT logic circuit with various V_{DD}.

Meanwhile, the effect of V_L effect on determining the NOT gate performance has also been examined and plotted as shown in Fig. 5.20. V_{DD} was fixed at 20 V, while V_L changed from -10 V to 10 V. The positive V_L resulted in a smaller voltage drop than the negative and 0 V of V_L. This can be explained by the fact that the channel resistance of the load TFT became

smaller with increasing V_L. However, there existed a resistance changing competition between the load and drive TFTs when V_L was changing. This can be attributed to that the voltage drops did not show maximum value when V_L is at the negative maximum.

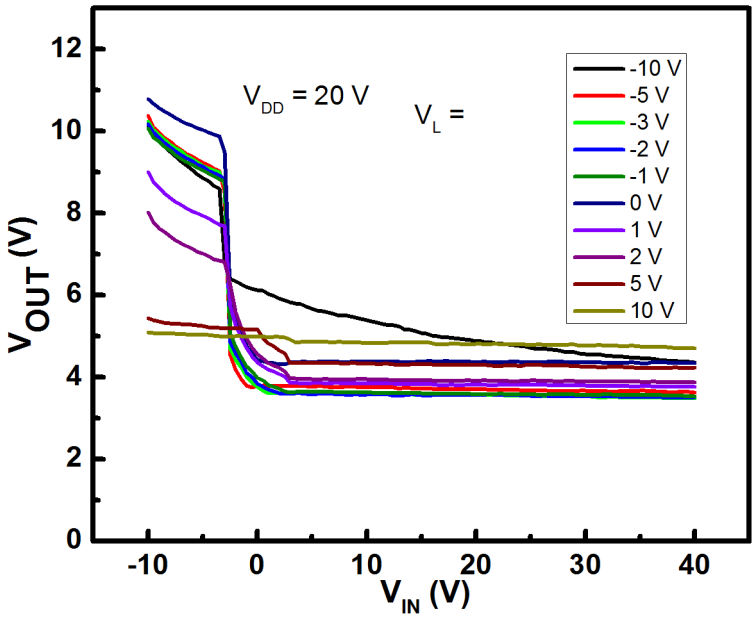


Figure 5.20: Voltage transfer characteristics of the NOT logic circuit with various V_L.

In conclusion, the operation of logic circuit based on sol-gel derived and RF sputtered ZnO TFTs via wedge wire bonding was demonstrated.

References

[1] M. Chiao, "Packaging (and Wire Bonding)," *Encyclopedia of Microfluidics and Nanofluidics*, pp. 1–6, 2013.

[2] D. Yeom, K. Keem, J. Kang, D.-Y. Jeong, C. Yoon, D. Kim, and S. Kim, "NOT and NAND Logic Circuits Composed of Top-Gate ZnO Nanowire Field-Effect Transistors with High-k Al_2O_3 Gate Layers," *Nanotechnology*, vol. 19, no. 26, p. 265202, 2008.

Chapter 6

ZTO TFTs characterization and radiation-hard study

6.1 Introduction

Radiation-hard electronics attract lots of interests in nuclear power application, outer space exploration and some other radiation harsh environment. Because of narrow band gap and low atom displacement threshold energy, regular silicon-based thin film transistors can be severely damaged even under a small dose of irradiation [1]. The wide band gap semiconductor materials, such as ZnO and GaN, have been investigated to make radiation-hard electronics. And it is recognized that ZnO is more radiation resistant than other semiconductors [2]. T. N. Jacksons group has done a lot of gamma-ray effect research on ALD deposited and RF magnetron sputtered ZnO TFTs and circuits [3][4][5][6][7]. Our group has studied sol-gel derived ZnO TFTs radiation-hard characteristics [8]. And it shows a promising result for radiation-hard ZnO based electronics application. Sol-gel technique compared to commonly used ALD and RF magnetron sputtering deposition demonstrates advantages of low cost, easy to set up and provide a high throughput [9].

Even though sol-gel derived ZnO shows lots of merits, the low mobility (smaller than 0.1 cm_{-1}/VS) limits its application. Various materials are tried to incorporate into ZnO to improve device field effect mobility. Some other ZnO related materials TFTs, such as indium zinc oxide (IZO) and indium gallium zinc oxide (IGZO) TFTs show higher field effect mobility. Indium acts as a motivator to improve the carrier mobility, but the transistor degrade heavily (V_{on} shift $>$ -15 V) even under low dose of gamma ray exposure [10][11]. Tin as another carrier motivator has been studied to improve the performance of ZnO related material thin film

transistors [12][13]. Comparing to pure ZnO, which has a 3.37 eV wide band gap, ZTO was reported to have a similar band gap of 3.35 eV [14]. ZTO also provides chemical stability with respect to oxidation and etching [15][14]. ZTO is also relatively cheap compared to widespread and heavily used indium [16]. These properties make ZTO an attractive promising solution processed materials with high channel mobility for radiation-hard, oxidizing environment, and acid resistance electronics applications. Electron [17] and ultra-violet [18] irradiation research has been conducted on ZTO, but no gamma-ray and proton radiation effect research on ZTO has been reported. Therefore, in this work, we fabricated different types of sol-gel derived ZTO TFTs and studied the gamma-ray irradiation effect on ZTO TFTs IV characteristics and determined the suitable fabrication process for radiation-hard ZTO TFTs.

6.2 ZTO field effect mobility enhancement

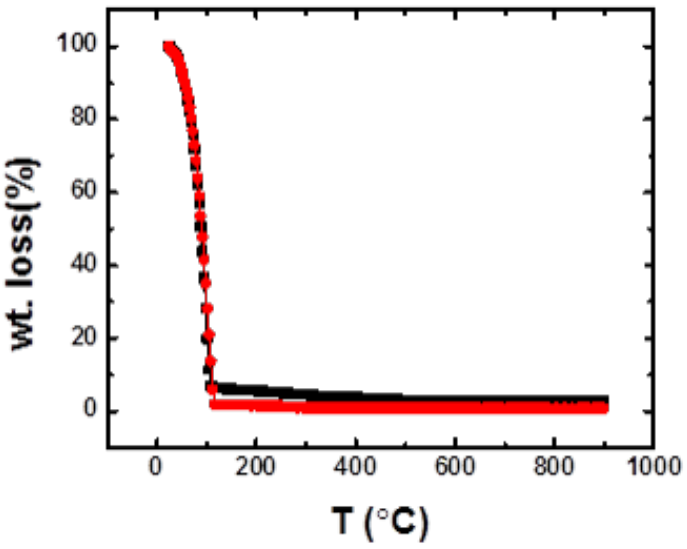
6.2.1 Fabrication

Three types of bottom-gate ZTO circular TFTs were fabricated as follows; Thermal oxidized Si wafers (University wafer) with 100 nm oxide layer (gate insulator: SiO_2) were used as substrates. The sol-gel precursor solution was prepared by dissolving zinc acetate dihydrate and tin chloride in 2-methoxtethanol with a constant Zn:Sn ratio of 7:3. The solutions with two different precursor concentrations (0.05 M and 0.2 M) were prepared. The precursor solutions were stirred for two hours, filtered through 0.22 um syringe filter and spin-coated on the oxidized Si wafers at 3000 rpm for 30 seconds and then the ZTO film was calcinated at 285 °C for 5 minutes. The first two types of ZTO thin films were repeatedly deposited four times by using 0.2 M and 0.05 M concentration precursors as follows; The 0.05 M concentration precursor was used to spin-coat for the first layer, the second layer was deposited by using 0.2 M concentration precursor. The third and fourth layers were repeated spin-coating 0.05 M and 0.2 M concentration precursors. This fabrication procedure results in an improvement of ZTO TFTs IV characteristics. After that, all three types of samples were annealed at 500 °C for one hour (KSL-1100X furnace). The Ti/Ir chosen as the metallic contacts were deposited through DC magnetron sputtering, where iridium (Ir) has a heavy atomic mass (192.2) and is supposed

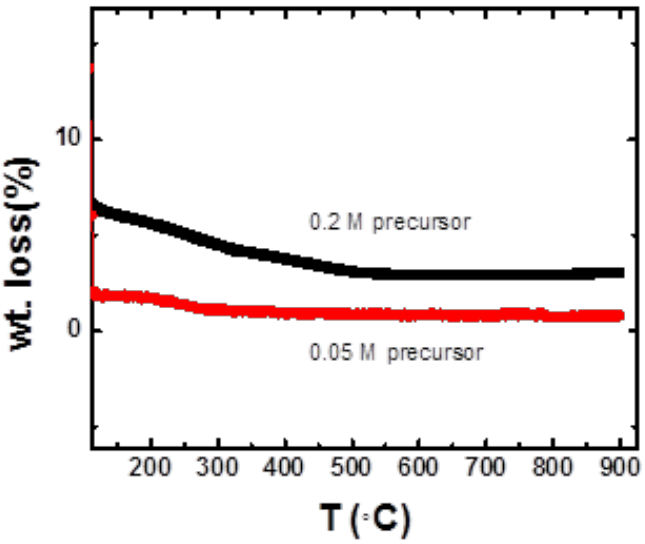
to be a more radiation-hard metallic contacts compared to commonly used aluminum (Al) [8]. Because of the weak acid resistance characteristics, the ZTO device isolation was achieved by applying BOE wet etching to form a mesa structure. The samples were slightly scratched on the bottom side to make the Si layer exposed and copper plates serving as the bottom gate were attached by via Ag paint stick. In order to investigate the gamma-ray direct effect on the ZTO TFTs, there are no passivation layers deposited on top of ZTO channel.

6.2.2 TGA

Thermogravimetric Analysis(TGA) was performed using Shimadzu-50H with a 20 μl alumina crucible. Approximately 10 mg of the precursor solution was heated from room temperature to 800 °C at a heating rate of 10 °C/min under 20 mL/min of nitrogen.Fig. 6.1 (a) and (b) shows the thermal behavior of ZTO precursor solution as determined by TG analysis. The weight loss below 110 °C can be attributed to the evaporation of the organic solvent and the additive assimilated into the precursor as the boiling points of solvent and organic additives are usually below 200 °C. The enlarged figure on the right shows that the total decomposition would occur above 500 °C. These results suggest that a heat treatment of 500 °C would be sufficient to form the ZTO thin film. Since the total decomposition stops at 500 °C, the material is supposed to be amorphous.



(a)



(b)

Figure 6.1: TGA of the precursor solution at 10 °C/min heating rate in nitrogen.

6.2.3 XRD

Thermal Phase transformation and crystallization were measured using X-ray diffraction (XRD, Bruker D2 Phaser X-ray diffractometer). Fig. 6.2 represents the XRD of the ZTO films. In all the three cases, the broad and small peak exhibited at 2θ = 34 degrees confirms that the films are amorphous as reported previously in the literature.

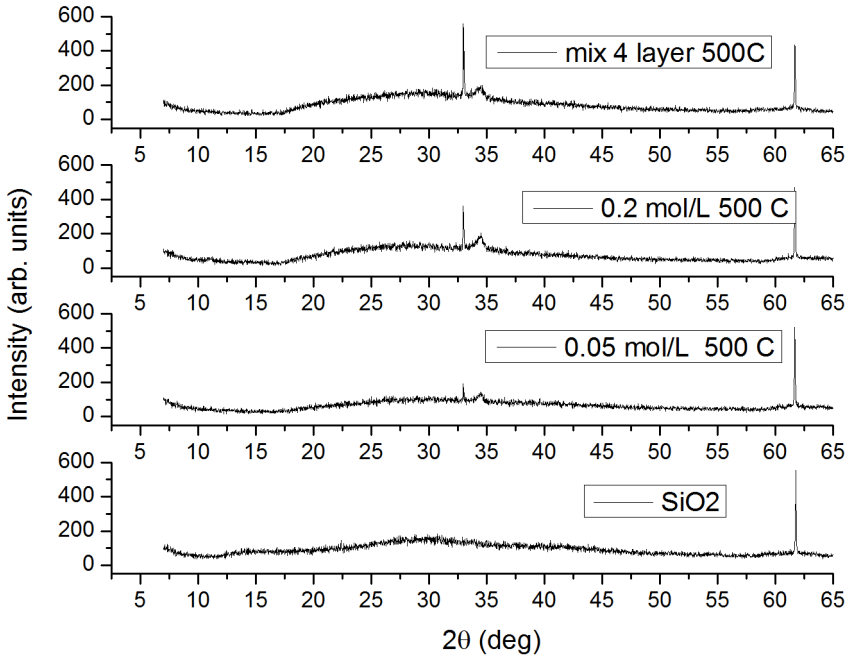
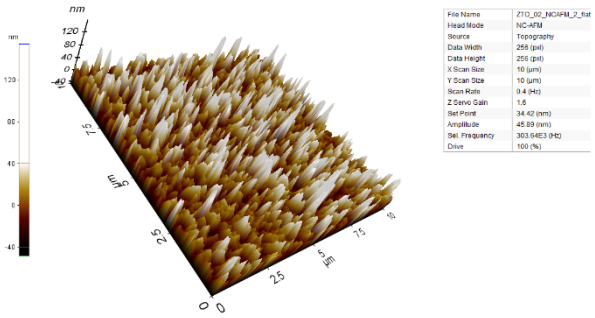


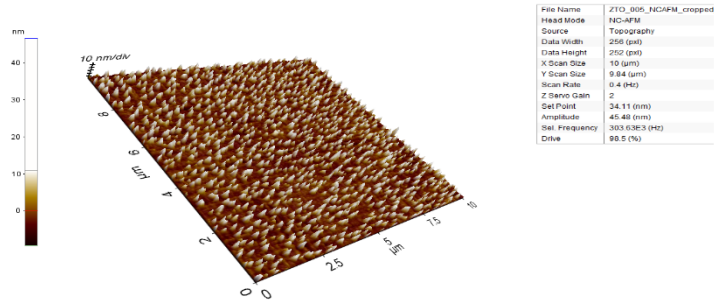
Figure 6.2: XRD for ZTO.

6.2.4 AFM

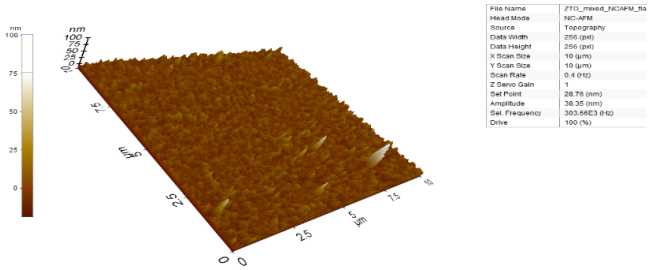
Fig. 6.3 and 6.4 show the 3D and images of 10×10 μm^2 area AFM scan. The roughness of the 0.05 mol/L sample and multi-stack sample is around 6 nm. The roughness of 0.2 mol/L sample is about 20 nm. The higher roughness will introduce more defects between ZTO channel layer and the insulator.



(a) 0.2 mol/L precursor ZTO layer

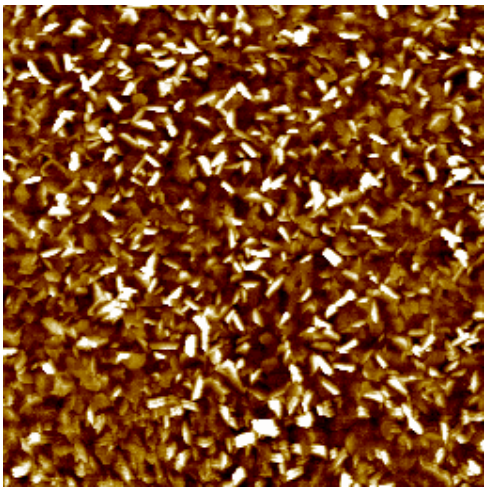


(b) 0.05 mol/L precursor ZTO layer

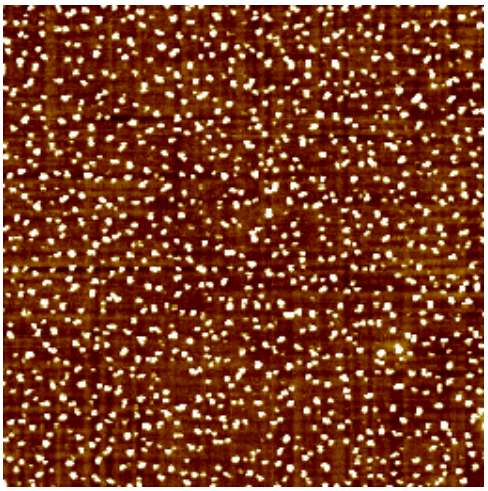


(c) Multi-stack ZTO layer

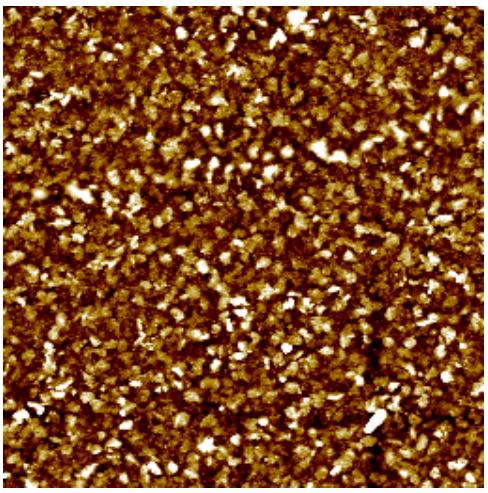
Figure 6.3: 3D AFM images of (a) 0.2 mol/L precursor ZTO layer, (b) 0.05 mol/L precursor ZTO layer, (c) Multi-stack ZTO layer.



(a) 0.2 mol/L precursor ZTO layer.



(b) 0.05 mol/L precursor ZTO layer.



(c) Multi-stack ZTO layer.

Figure 6.4: 2D AFM images of (a) 0.2 mol/L precursor ZTO layer, (b) 0.05 mol/L precursor ZTO layer, (c) Multi-stack ZTO layer.

6.2.5 Device characterization

The three types of devices characterization have been carried out *via* H-100 Signatone probe station equipped with Keithley 6517 voltage source. The transfer and output IV curves were plotted in Fig. 6.5 and 6.6 The multi-stack ZTO TFT demonstrated the highest drain current, while 0.05 M precursor prepared ZTO TFT to show the lowest. The intrinsic parameters for the three types of ZTO TFTs were calculated and summarized in table 6.1

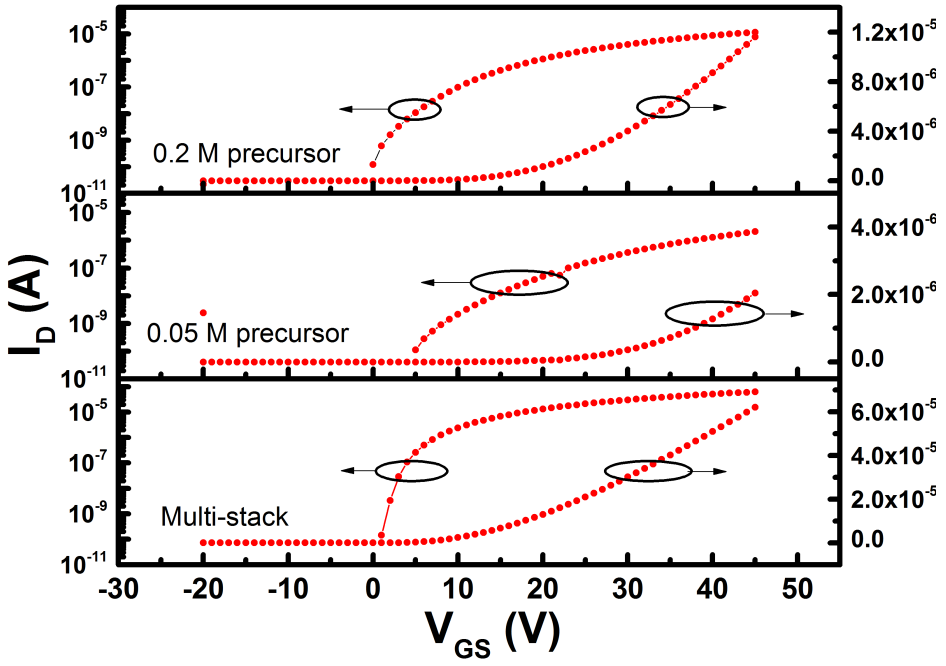


Figure 6.5: Transfer characteristics of the three types of ZTO TFTs.

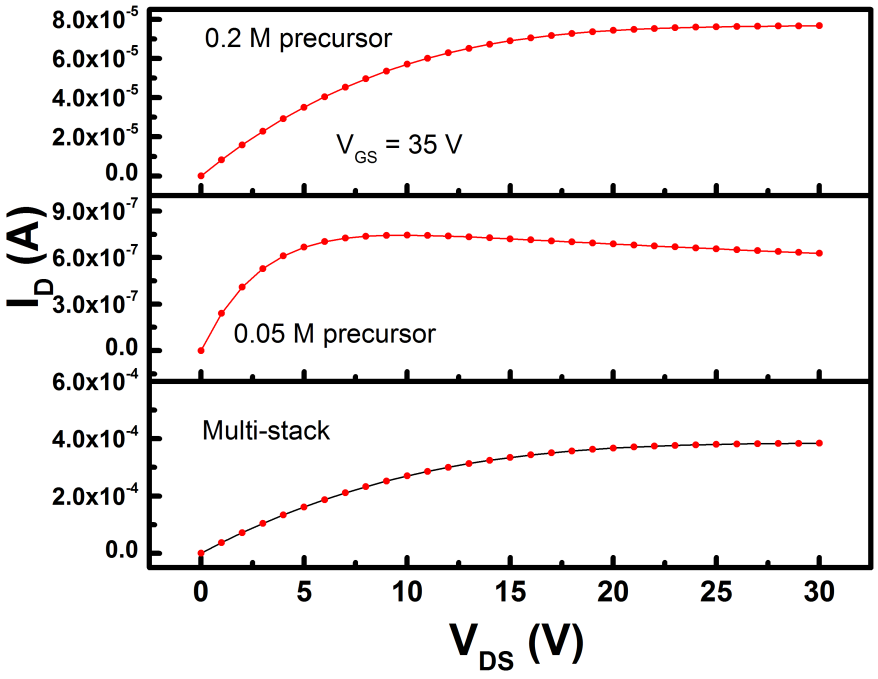


Figure 6.6: Output characteristics of the three types of ZTO TFTs.

Sample	μ_{FET}	On/off ratio	SS	D_{it}
0.2 M ZTO TFTs	1.45	10^6	1.49	5.84×10^{12}
0.05 M ZTO TFTs	0.45	10^5	1.57	6.69×10^{12}
Multi-stack ZTO TFTs	5.3	10^7	0.82	2.43×10^{12}

Table 6.1: Parameters summary for three types of ZTO TFTs.

As can be seen in table 6.1, the mobility of the film was found to be highly increased when the deposition pattern was changed. The stacking of layer was done as 0.05 M/0.2 M/0.05 M/0.2 M. As seen from the table, the mobility of the film produced by this process was about 5.3 cm_{-1}/VS, which is much higher than that of the other two. The electrical performance also seems to be improved with I_{on}/I_{off} ratio being increased, SS swing and the corresponding D_{it} being less. The density of the latter film also seems to be improved can be as seen from the AFM images. This could be attributed to the formation of the interface between the layers of the multi-structured active layers TFTs which might affect the electrical properties of the transistors. The first film made up of 0.05 M concentration of precursor solution might have

many porous regions and poor interface between the channel layer and the dielectric which might have been mitigated by another layer of higher concentration [19]. Also, the trap sites in the interface layer might have been depleted by the adsorbed oxygen molecules on the surface. Thus, the interface layer would not be able to disturb electron transport in the channel, resulting in the improvement of field effect mobility μ_{FET}.

6.3 Gamma-ray irradiation effect

6.3.1 Device characterization before and after irradiation

In order to investigate the gamma-ray direct effect on the ZTO TFTs, there are no passivation layers deposited on top of ZTO channel. The three samples were irradiated in the chamber and taken out at the dose of 10 MRad and 50 MRad, respectively. To see the gamma-ray radiation effect on ZTO TFTs electrical characteristics, both transfer and output IV measurements for all three samples have been carried out in a dark environment at room temperature before and after irradiation. 10 devices from each sample were measured for a statical study. The transfer characteristics at a fixed drain voltage (V_{DS} = 1 V) for representative ZnO TFTs were shown in Fig. 6.7. It is observed that there is an increase in drain current for all three types of ZTO TFTs at 10 MRad. Both 0.2 M precursor ZTO TFT and multi-stack ZTO show slight drain current change, while the increase ratio of the drain current in 0.05 M precursor ZTO TFT before and after irradiation is much higher than the rest of two samples. However, after 50 MRad irradiation, the three types of ZnO TFTs shows a drain current decrease compared to the devices after 10 MRad. It is observed that 0.2 M precursor prepared sample shows the extremely radiation-hard transfer characteristics with almost no degradation under the high dose of 50 MRad gamma-ray irradiation, while 0.05 precursor prepared and multi-stack ZnO TFTs demonstrate a relative large degradation of drain current.

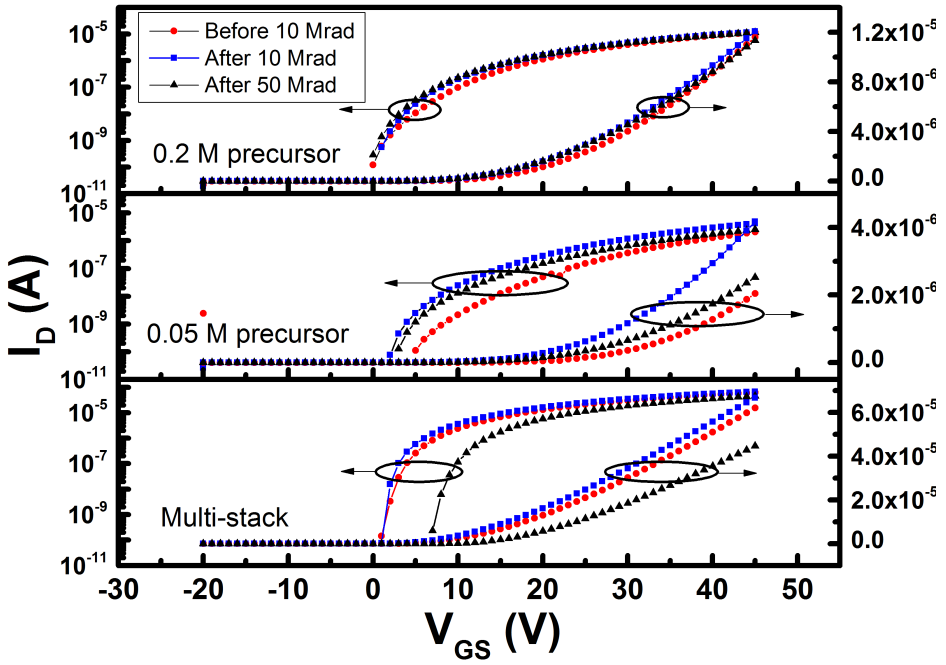


Figure 6.7: Transfer characteristics of ZTO TFTs before and after irradiation.

In Fig. 6.8, output IV curves for all devices were chosen at a constant V_{GS} = 35 V. Similar phenomenon has been observed for 0.05 M precursor prepared and multi-stack ZTO TFTs in the output IV curves. The output current for 0.2 M precursor prepared ZTO TFTs also degraded around 30% after 50 MRad dose. To test the reliability and stability ZTO TFTs, threshold voltage shift is a crucial parameter. The V_T is extracted from the equation (4.4.1) in chapter 4.

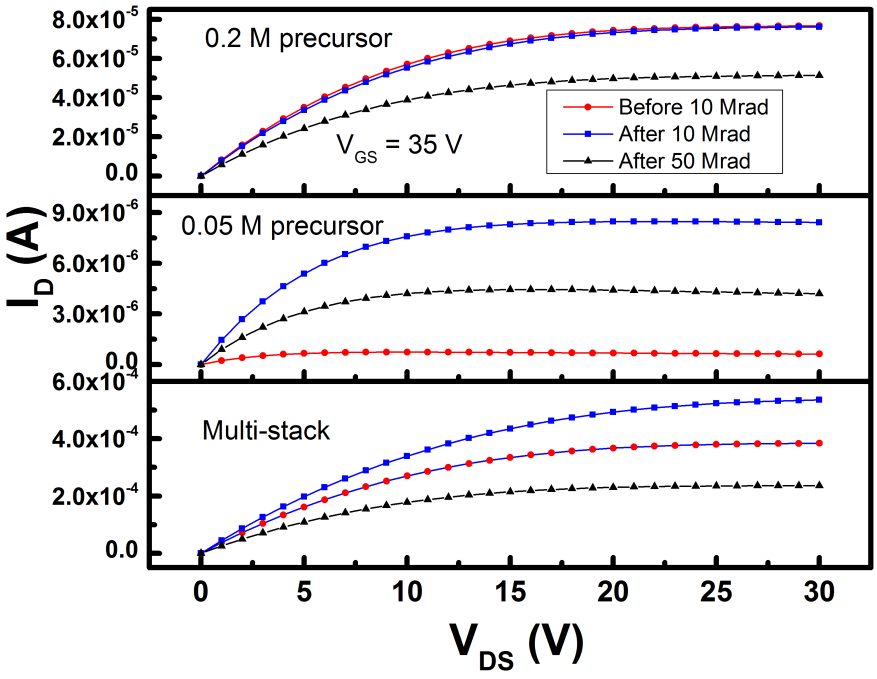


Figure 6.8: Output characteristics of ZTO TFTs before and after irradiation.

Fig. 6.9 shows the V_T of the representative devices under different amount of gamma-ray dose and the V_T shift (ΔV_T) was summarized in table 6.2. For 0.2 M precursor ZTO TFTs and multi-stack ZTO TFTs, V_T only shift to negative around 2 V at 10 Mrad gamma-ray irradiation, while the ΔV_T of 0.05 M precursor ZTO TFTs can reach -4.6 V. When the gamma-ray dose is 50 MRad, the V_T shift to positive. For the most stable ZTO TFTs that we measured in the 30 devices, the ΔV_T for the three types ZTO TFTs (not shown) are -0.3 V, -2.9 V and -0.3 V at 10 MRad and 0.4 V, 2.5 V and 1.2 V at 50 MRad, respectively. Compared to indium zinc oxide TFTs [20][21], ZTO TFTs under proper fabrication process show attractive stability in radiation-harsh environment. The V_T shifting and drain current increasing at the low gamma-ray dose (10 MRad) can be attributed to the electron-hole pair generation in the SiO_2 dielectric layer, while the high dose gamma-ray (50 MRad) might damage ZTO layer. This can be verified from following μ_{FET} analysis.

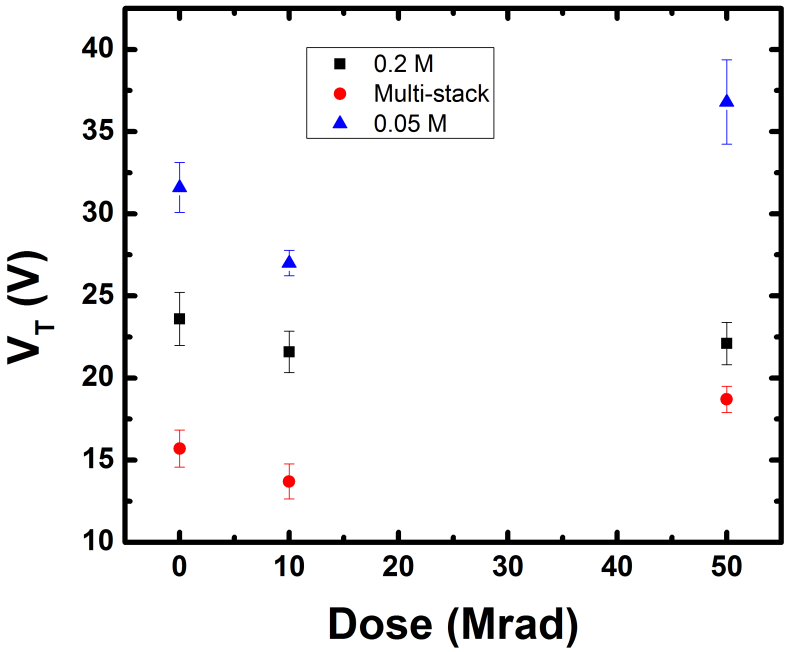


Figure 6.9: Threshold voltage shift of samples after gamma irradiation.

Sample	0.2 M ZTO TFTs	0.05 M ZTO TFTs	Multi-stack ZTO TFTs
ΔV_T (10 Mrad)(V)	-2	-4.6	-2
ΔV_T (50 Mrad)(V)	1.52	3.9	3

Table 6.2: V_T shift after irradiation.

The μ_{FET} for the three types of representative ZTO TFTs are plotted in Fig. 6.10. The μ_{FET} for 0.2 M precursor devices and multi-stack devices is nearly unchanged at 10 MRad. Meanwhile, the 0.05 M precursor ZTO TFT shows around 40% increase in the μ_{FET}. However, three types of ZTO TFTs degraded at different levels under 50 MRad, while 0.2 M precursor prepared sample shows the smallest degradation. As a result, multi-stack ZTO TFT has the highest μ_{FET} that makes it a more suitable radiation-hard device compared to the other two devices at the low dose of gamma-ray irradiation. But the lowest μ_{FET} degradation makes 0.2 M precursor ZnO TFT a perfect candidate to work at the high dose of irradiation.

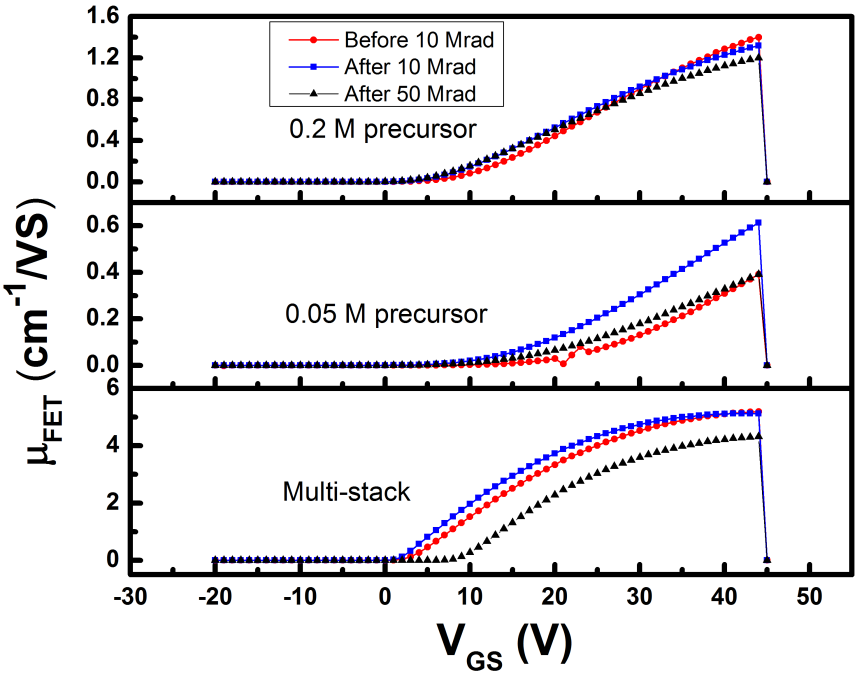


Figure 6.10: Field effect mobility of ZTO samples before and after irradiation.

Apart from those, the sub-threshold swing (SS) can be extracted at the steepest point of the transfer IV curves in log scale using the equation (4.4.2) in chapter 4. The corresponding trap density (D_{it}) was also determined.The extracted SS and D_{it} before and after 10 MRad and 50 MRad gamma-ray irradiation have been summarized in table 6.3 below. It can be observed that after 10 MRad gamma-ray irradiation, both SS and D_{it} decreased for all three types of ZTO TFTs. This could be explained as that the samples were in an annealing process during the relatively low dose of gamma-ray irradiation and some parts of the interfacial traps have been filled with oxygen atoms from the ZTO channel. Besides that, the vacancies of oxygen in the ZTO channel resulted in increasing electrons concentrations. When gamma-ray irradiated for 50 MRad, both SS and D_{it} increase, which indicate that the generation of defects at interface exceeds the interfacial traps filling process.

Sample	0.2 M ZTO TFTs	0.05 M ZTO TFTs	Multi-stack ZTO TFTs
SS (Unirradiated)(V/decade)	1.65	1.88	0.72
SS (10 MRad)(V/decade)	1.48	1.26	0.49
SS (50 MRad)(V/decade)	1.58	1.71	0.56
D_{it} (Unirradiated)($eV_{-1}cm_{-2}$)	5.84×10^{12}	6.69×10^{12}	2.43×10^{12}
D_{it} (10 MRad)($eV_{-1}cm_{-2}$)	5.22×10^{12}	4.41×10^{12}	1.58×10^{12}
D_{it} (50 MRad)($eV_{-1}cm_{-2}$)	5.59×10^{12}	6.05×10^{12}	1.8562×10^{12}

Table 6.3: SS and D_{it}.

6.4 Conclusion

In this work, the proper fabrication process for increasing μ_{FET} has been set up and verified. The electrical performance of ZTO TFTs shows a great improvement with multi-stack layer deposition. The effect of 10 MRad and 50 MRad gamma-ray irradiation effect on three different types of ZTO TFTs has been investigated. 0.2 M precursor ZTO TFTs demonstrate significant reliability and stability in electrical characteristics under different amount of dose of gamma-ray radiation, while multi-stack ZTO TFTs with the highest μ_{FET} show the radiation-hardness characteristics under the low dose of gamma-ray irradiation. The proper process fabricated ZTO TFTs show nearly unchanged V_T and μ_{FET}. The low dose of gamma-ray irradiation also has the potential of decreasing the SS and D_{it}. This can be fully investigated and applied for device fabrication. Sol-gel derived ZTO TFTs, compared to sol-gel derived ZnO TFTs and indium incorporated ZnO TFTs, have both relatively higher field-effect mobility and more radiation-hard advantages at the same time with proper fabrication process, which make them good candidates for radiation-hard electronics application in spacecraft and nuclear power plants.

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Chapter 7

Summary and future work

7.1 Summary

As a summary, ZnO thin film and ZnO TFTs have been investigated, designed, fabricated and characterized in this work. Gamma-ray irradiation effect has been investigated on both ZnO thin film and ZnO TFTs. Both Raman spectroscopy and photoluminescence show ZnO thin film a radiation-hard material with unshod peak position and barely changed peak intensity. For X-ray diffraction analysis, ZnO (002) crystal plane drops from 1800 to 1500 (arb. unites.), indicating that ZnO crystal quality slightly degraded after 10 MRad dose of gamma-ray irradiation. ZnO TFTs with different metallic contacts have also been tested before and after gamma-ray irradiation. Most of the ZnO TFTs with Ti/Al electrodes didn't work because of the serve damage of contacts. The ZnO TFTs with Ti/Pd electrodes showed less damage but still degraded because of both metallic contacts and channel layers degradation after gamma-ray irradiation.

Annealing temperature effect attracted a lot of interests when sol-gel derived ZnO TFTs were fabricated. The ZnO channel layers were deposited on an oxidized Si wafer via sol-gel process and were annealed at different temperatures. It was found that the annealing temperature greatly affects the performance of sol-gel derived ZnO TFTs. With increasing annealing temperature, crystallite size became larger and hence the amount of grain boundary defects reduced which must have a strong influence on modulating the density of states, V_{on} (and V_T) increases and off current drops drastically. The SS and corresponding D_{it} decrease as the annealing temperature increases. However, the μ_{FET} and the output current peak at 800 °C and

drop upon further temperature increase. The temperature dependent field effect measurement was used to gain an insight on the annealing temperature effect on ZnO TFTs electrical characteristics. By combing the MN rule and applying the self-consistent procedure in a-IGZO TFTs analysis, the DOSs of different temperatures annealed sol-gel derived ZnO TFTs were successfully extracted. The results show that DOSs decrease with annealing temperature increase in general, but too high of a temperature anneal may not be beneficial in reducing DOSs. It was found that the TFT with ZnO layers annealed at 800 °C for one hour shows the best electrical performance.

Apart from individual ZnO TFT characterization, logic circuits based on patterned sol-gel derived and RF magnetron sputtered ZnO TFTs have been designed and fabricated. The load and drive device components didn't show a good electrical performance with high gate leakage current. An alternative circuit design with wedge wire bonding solved the leakage current issue and made working NOT gate ZnO circuits. The positive load gate voltage (V_L) resulted in a smaller voltage drop between on and off state than the negative and 0 V. However, there was a resistance changing competition between load and drive channel, which can be the reason that the voltage drops didn't show maximum value when V_L is the negative maximum.

In addition, since ZTO shows higher field effect mobility in TFTs than ZnO, the ZTO TFTs with different layer deposition has been analyzed. The electrical performance of ZTO TFTs shows a great improvement with multi-stack layer deposition. The effect of 10 MRad and 50 MRad gamma-ray irradiation effect on three different types of ZTO TFTs has been investigated. 0.2 M precursor ZTO TFTs demonstrate significant reliability and stability in electrical characteristics under different amount of dose of gamma-ray radiation, while multi-stack ZTO TFTs with the highest μ_{FET} show the radiation-hardness characteristics under a low dose of gamma-ray irradiation. The proper process fabricated ZTO TFTs show nearly unchanged V_T and μ_{FET}. The low dose of gamma-ray irradiation also has the potential of decreasing the SS and D_{it}. This can be fully investigated and applied for device fabrication. Sol-gel derived ZTO TFTs, compared to sol-gel derived ZnO TFTs and indium incorporated ZnO TFTs, have both relatively higher field-effect mobility and more radiation-hard advantages at the same time with

proper fabrication process, which make them good candidates for radiation-hard electronics application in spacecraft and nuclear power plants.

7.2 Future work

In this research work, we primarily studied ZnO/ZTO TFTs' optimal fabrication process, gamma-ray irradiation effect on TFTs and the possibility of fabricating working logic circuit based on ZnO TFTs. However, the other ZnO/ZTO fabrication processes are still needed to be explored. Firstly, precursor concentration, spin-coat speed, annealing in different gas atmospheres effects for ZnO/ZTO thin film and TFTs fabrication will be investigated to further improve the field effect mobility, on/off ratio and Dit decreasing of ZnO/ZTO TFTs. Then the gamma-ray irradiation effect study will be carried out on ZTO TFTs and proton irradiation will be applied for both ZnO and ZTO TFTs. The suitable fabrication processes for the best radiation-hard ZnO/ZTO TFTs will be designed and tested.

By using wedge wire bonding, more complicated ZnO thin film logic circuits, such as NOR gate, NAND gate, ring oscillator and linear-feedback shift register (LFSR) will be designed, simulated, fabricated and tested. By applying the same technology, ZTO TFTs based logic circuits will also be designed and characterized. Even though the wire bonded logic circuits can successfully solve the basic function problem, the non-compact size will limit its usage in industry. As a result, the patterned gate ZnO/ZTO TFTs will still need to be investigated. Gamma-ray irradiation effect on ZnO/ZTO TFTs based working logic circuits will also be investigated.

ZTO TFTs show a relatively high field effect mobility and radiation-hard characteristic, in which tin acts as a motivator to improve the carrier mobility. S. Y. Lee et al. claimed that Si will act as an oxygen binder to reduce the oxygen vacancies [1]. As a result, SZTO TFTs will be investigated and the radiation-hard characteristic will also be tested.

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Appendices

Appendix A

Electrical Characterization of Sol-Gel Derived ZnO Thin-Film Transistors with Different Numbers of ZnO Layers

Sol-gel derived ZnO thin-film transistors (TFTs) with different numbers of layers were fabricated. Current-voltage measurements were acquired for the different devices, their electrical characteristics were analyzed and a calculation and comparison of the subgap density of states (DOSs) was performed.

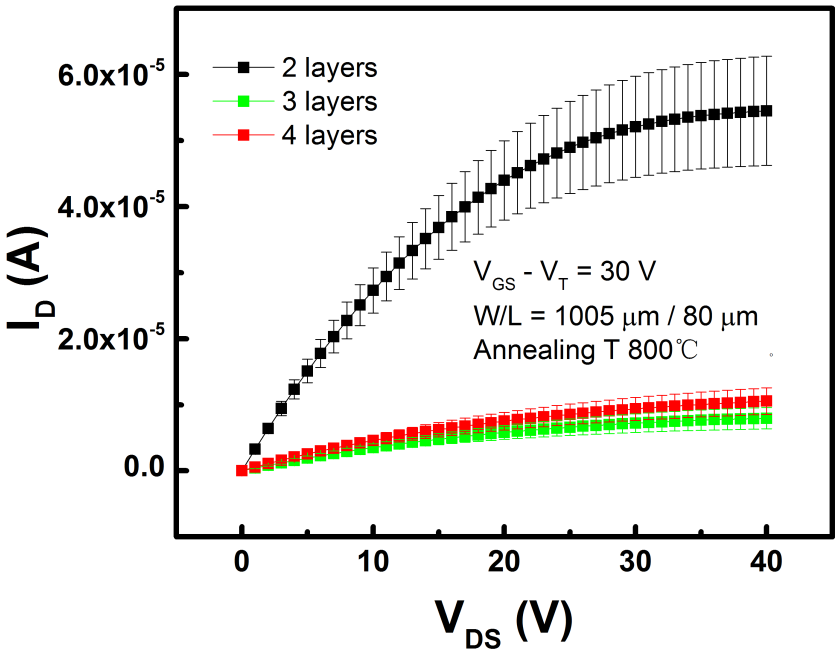

Figure A.1: Output I-V characteristics for 2, 3 and 4 layer ZnO TFTs under the same effective gate bias. 2 layer ZnO TFTs show higher output drain current for given V_{GS} - V_T. Variability is shown for 8 devices.

Four types of bottom-gate ZnO TFTs were fabricated with different numbers of layers. The thicknesses of the resultant ZnO layers were 30 nm, 52 nm, 72 nm and 100 nm for 1, 2, 3 and 4 layers, respectively. A Ti/Mo/Pd thin film was deposited by DC sputtering to provide

source and drain ohmic contacts. Eight TFTs in different regions of each sample were measured. The TFTs with a single layer of ZnO was mostly non-functional. We assume that the thickness of a single layer of ZnO is not sufficient for forming a continuous crystalline structure. Therefore, this study focuses on the 2, 3 and 4 layer ZnO TFTs. The output I-V curves with error bars and the transfer I-V curves are plotted in Fig. A.1 and Fig. A.2. The measurements indicate the better performance of the 2 layer ZnO TFTs compared to the 3 and 4 layer ZnO TFTs. The threshold voltage shifts in the positive direction as the number of the layers increases (Fig. A.3). The corresponding field effect mobility in the linear region (V_{DS} = 5 V) was extracted and plotted in Fig. A.4. Under the same electron carrier concentration, the 2 layer ZnO TFTs demonstrate approximately 6 times higher maximum μ_{FET} compared to the 3 and 4 layer ZnO TFTs.

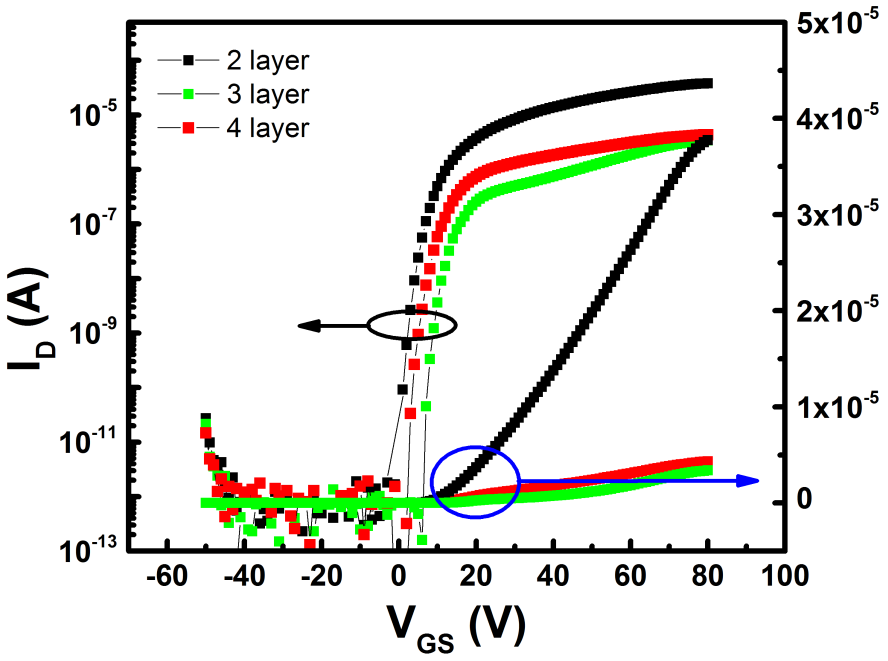

Figure A.2: Transfer I-V curve for 2, 3 and 4 layer ZnO TFTs. The 2 layer ZnO TFT shows higher transfer characteristics. The transfer I-V curves of these three TFTs are representative of all the TFTs that we have measured.

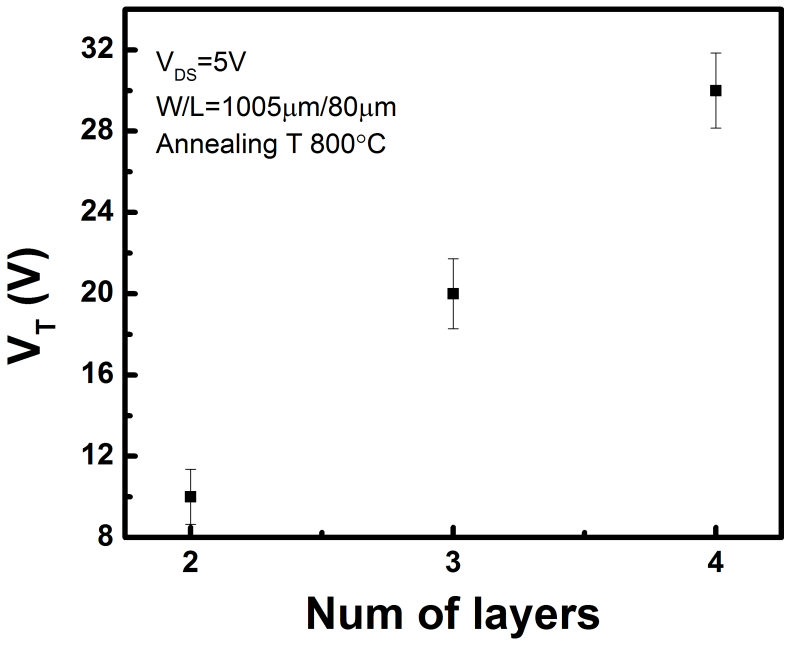

Figure A.3: V_T shifts positive as the number of ZnO layers increase.

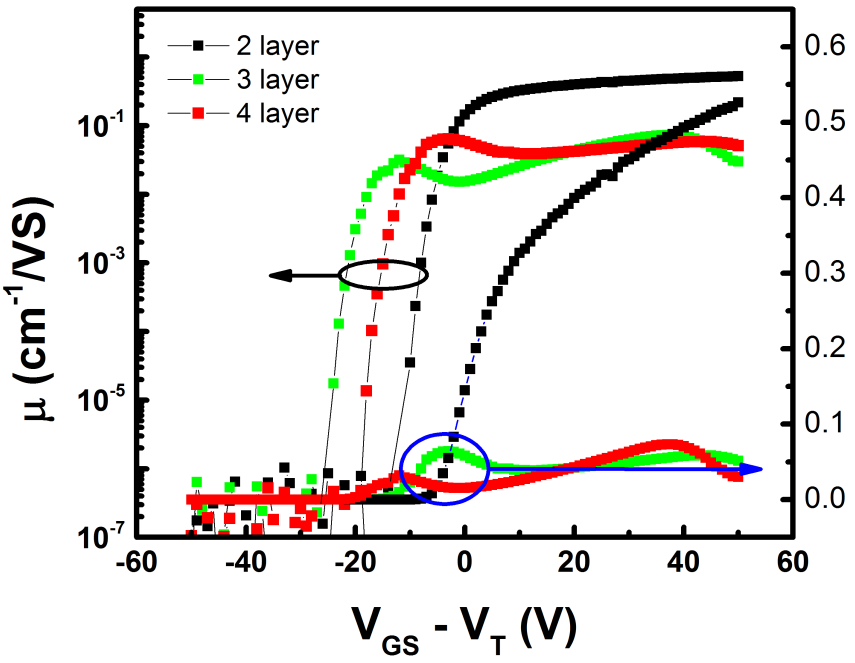

Figure A.4: μ_{FET} of ZnO TFTs with different layers under the same electron carrier concentration. The 2 layer ZnO TFTs demonstrate approximately 6 times higher maximum FET compared to the 3 and 4 layer ZnO TFTs.

Another set of samples were fabricated in an identical process mentioned above in order to measure the DOS of ZnO TFTs. In order to calculate the DOS, three ZnO TFTs with 2, 3, 4 numbers of layers, respectively, were measured from 296K to 340K, and the self-consistent DOSs extraction method used in Chapter 4 was implemented. The DOS in the subthreshold region for different layers ZnO TFTs (Fig. A.5) slightly decreases as the number of ZnO layers increases. These results agree with the subthreshold swings of the three TFTs, indicating that the subthreshold swing decreases as the number of layers increases.

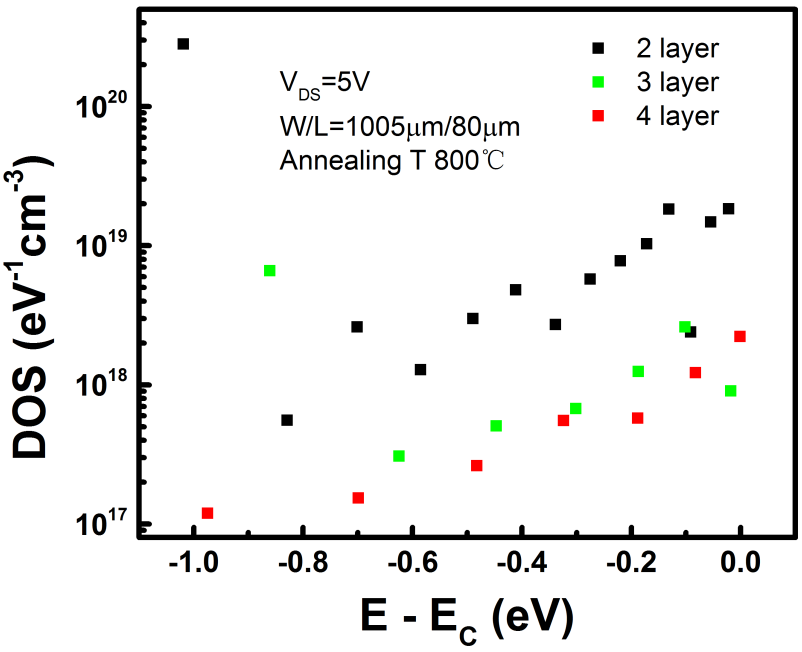

Figure A.5: DOSs in subthreshold region as functions of energy with respect to conduction band energy for 3 TFTs with either 2, 3 or 4 ZnO layers. DOS appears to decrease with the number of layers increasing. The subthreshold swings 1.01 V/dec, 0.72 V/dec and 0.71 V/dec of the 3 typical (2-, 3-, 4-layer) TFTs mentioned above, are consistent with the results obtained from the DOSs extraction.

In conclusion, we have investigated the number of layers effect on the performance of sol-gel derived ZnO TFTs. The results indicate that by lowering the number of layers, ZnO TFTs transfer and output characteristics and FET can highly be improved. In contrast, more ZnO layers demonstrate the possibility to decrease the subgap DOS.