DAMAGE PREDICTION OF LEAD FREE BALL GRID ARRAY PACKAGES UNDER SHOCK AND DROP ENVIRONMENT

Except where reference is made to the work of others, the work described in this thesis is my own or was done in collaboration with my advisory committee. This dissertation does not include proprietary or classified information.

____
Dhananjay R. Panchagade

Certificate of Approval:

George T. Flowers Alumni Professor Mechanical Engineering	Pradeep Lall, Chair Thomas Walter Professor Mechanical Engineering
John L. Evans Associate Professor Industrial and Systems Engineering	Robert L. Jackson Assistant Professor Mechanical Engineering

Joe F. Pittman
Interim Dean
Graduate School

DAMAGE PREDICTION OF LEAD FREE BALL GRID ARRAY PACKAGES UNDER SHOCK AND DROP ENVIRONMENT

Dhananjay R. Panchagade

A Dissertation

Submitted to

the Graduate Faculty of

Auburn University

in Partial Fulfillment of the

Requirements for the

Degree of

Doctor of Philosophy

Auburn, Alabama
May 10, 2007

DAMAGE PREDICTION OF LEAD FREE BALL GRID ARRAY PACKAGES UNDER SHOCK AND DROP ENVIRONMENT

Dhananjay R. Panchagade

Signature of Author

Date of Graduation

VITA

Dhananjay Panchagade, son of Shri. Ramchandra Sadashivrao Panchagade and Neelima Panchagade, was born on May 4th, 1976, at Mumbai, India. He did his schooling from St. Joseph's Boys' High School, Pune, India. He attended St. Vincent's Junior College, Pune, India for Higher Secondary education from 1992-1994. In 1994 he entered University of Pune, Pune, India and received a Bachelor of Engineering in Mechanical Engineering in 1998.

In 2000, he continued his education by entering the Graduate School, Wayne State University, Detroit, Michigan, USA for Masters degree in Mechanical Engineering. In August of 2002 he joined Ph.D. program at Auburn University, Auburn, Alabama, USA.

DISSERATION ABSTRACT

DAMAGE PREDICTION OF LEAD FREE BALL GRID ARRAY PACKAGES UNDER SHOCK AND DROP ENVIRONMENT

Dhananjay Panchagade

Doctor of Philosophy, May 10, 2007
(M.S., Wayne State University, 2001)
(B.E., University of Pune, 1998)

208 Typed Pages

Directed by Professor Pradeep Lall

The fatigue and damage of solder joints and also the potential for interface failure within BGA packages are caused by thermal cycling. In case of portable electronic products, fatigue is caused by repetitive drop and shock during transportation, or vibrations experienced in land-vehicles, air-planes, ships etc. The solder joint failure can then be attributed to the structural dynamics of the product. Therefore there is a need to develop predictive techniques for electronic failure mechanisms in shock and drop-impact. Drop survivability methodologies are developed using JEDEC drop testing methods.

Deformation kinematics of printed circuit board assembly using high-speed imaging at 150,000 fps has been studied. Explicit finite element models are developed for fine-pitch BGAs using smeared property approach and validated with experimental results.

Damage proxies for failure mechanisms at the copper-to-solder, solder-to-printed circuit board and copper-to-package substrate have been developed. Relative damage index based on transient strain history has been developed to show the damage progression w.r.t. number of drops to failure are investigated using damage superposition (Miner’s Rule). Various packages are studied such as plastic ball-grid arrays, flex ball-grid arrays for both 62Sn36Pb2Ag and 95.5Sn4.0Ag0.5Cu solder alloy compositions. Effects of thermal cycling from -40 degC to 125 degC, isothermal aging at 125 degC has been studied for life prediction of the packages. Structural dynamics of the printed circuit board has been studied using experimental modal testing techniques (laser vibrometers).

3-D Digital Image Correlation technique have been explored using ultra-high speed camera to study full-field strain and deformation of PCB populated with packages in shock/vibration testing. Failure modes and mechanisms have been studied using Scanning Electron Microscopy (SEM). Statistical Pattern Recognition (SPR) technique has been used to evaluate reliability degradation of electronic assemblies. It is observed that damage accumulated varies with surface finish of printed circuit board (ImAg, ImSn, and ENIG), drop height, solder joint composition, environment conditions and orientation.

ACKNOWLEDGMENTS

I would like to sincerely thank my research advisor, Dr. Pradeep Lall, who provided me with guidance and encouragement throughout the pursuit of this degree. I also wish to thank my dissertation committee members Dr. George Flowers, Dr. John Evans, Dr. Robert Jackson, and Dr. Michael Bozack for their advise on this work.

The author acknowledges for financial support received from the Semiconductor Research Corporation (SRC). I would like to recognize the help of the technical staff member John Marcell. Special thanks to all my colleagues, to name a few are; Ravi Karjatkar, Sachin Jambovane, Sangram Redkar and Kaysar Rahim for their love, encouragement, support and patience.

Finally, I would like to thank my father Shri. Ramchandra S. Panchagade, my mother Neelima R. Panchagade, and my brother Sanjay, who inspired me for Ph.D.

Style manual or journal used: Guide to Preparation and Submission of Theses and Dissertations

Computer software used: Microsoft Word 2003, Microsoft Excel, MATLAB, ABAQUS etc.

TABLE OF CONTENTS

CHAPTER 1 INTRODUCTION

CHAPTER 2 LITERATURE REVIEW

CHAPTER 6 HIGH SPEED DIGITAL IMAGE CORRELATION FOR TRANSIENT-SHOCK RELIABILITY OF ELECTRONICS

LIST OF TABLES

LIST OF FIGURES

CHAPTER 1

INTRODUCTION

1.1 Semiconductor Industry

According to a recent report, popularity of mobile electronic product is expected to grow from about 500 million in 2002 to nearly 1.5 billion in 2007. Transistors are shrinking in size which increases the power and space to perform better functions. This has made many stationary products portable [In-Stat/MDR 2003]. In 2003, communications segment such as mobile phone and Bluetooth were the largest sellers. Other products such as cameras, notebook PCs and MP3 players are contributing to the total sales. The computer product area is the most stable area and is expected to continue to do so in future. Products are classified as:

- Computer Products

  Notebook PC, PDA, Tablet PC, Smart Display
- Consumer Products

  MP3 Players, Digital Still Camera, Camcorder, Dual Mode Camera, Toy Camera
- Communications Products

  Mobile Phones, Wireless LAN, Bluetooth

While portable products are reducing in size, the push to increased feature content continues to drive electronic packaging and manufacturing industry to ever smaller packages. Acceleration of the miniaturization of consumer products such as cell phones (Figure 1.1), mp3 players, I-pods, cameras, laptops, etc. is an ongoing process. To satisfy these dynamic market demands, fine pitch and high density components such as Chip Scale Packages (CSPs) and Fine-Pitch Ball Grid Array Packages (FBGAs) are being used.

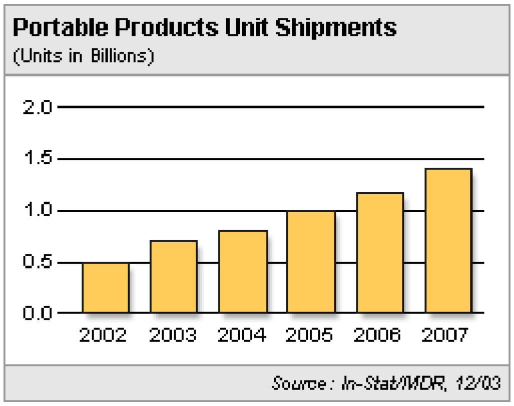


Figure 1.1: Growth in portable products

Fine-pitch ball grid arrays and chip scale packages (CSPs) are the most commonly used packages in portable electronic products. If the die size is more than 80% of the package area, it is mostly referred to as CSP. Generally the pitch is 1.0 mm and below for these packages. By reducing the size and spacing of passive components miniaturization can be efficiently achieved. Advantages of using CSPs over flip chip technology include, use of encapsulation, accommodation of die shrink without changing package footprint, etc. Testability using bare die assembly as compared to the traditional package based assembly, and use of wider liners and spacing on printed circuit board is the major advantage.

Recent technologies in electronic packaging industry includes nano-electronics, Single Electron Transistors (SETs), Carbon Nano Tube (CNT), Bioelectronics such as biomedical, bioengineering, biosensors and Organic/Printable Electronics bring interest to the semiconductor industry.

1.2 Lead-free Technology

Potential health hazard due to the toxic nature of lead has prompted electronic industry to come up with regulations on its usage. Europe, Japan and now US (not all states) has implemented the regulations suggested by Restriction of Hazards Substances (RoHS) and Waste from Electrical and Electronic Equipment (WEEE) directive. For most applications, due to this, eutectic tin-lead alloy in the solder joint has been replaced with lead free SAC alloys. Due to this change in technology, there arise new challenges (Figure 1.2). Most common health related diseases such has been reported due to the consumption or prolonged exposure to lead. Electronic industries in different countries world wide have appreciated the change in the technology and are trying to make an environment friendly electronics by implementing lead-free alloys. The new solder alloys and metallization are listed in

Table 1.1: and preferred lead-free surface finish materials are listed in Table 1.2: Figure 1.3 shows the preferred solder alloy combinations in Japan. Figure 1.4 shows the preferred solder alloy combinations in United Kingdom.

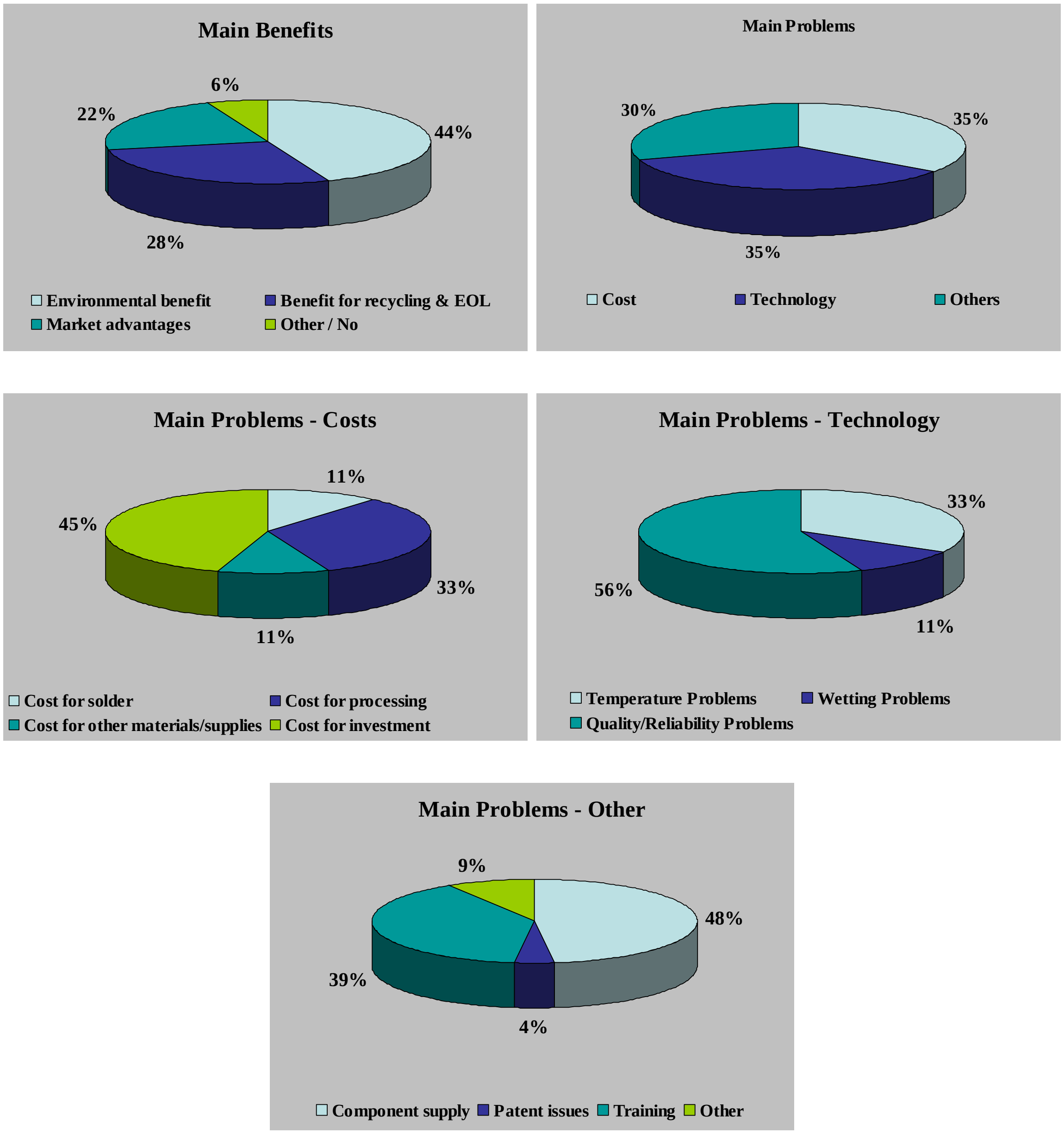


Figure 1.2: Statistics of Lead-free Technology

1.2.1 RoHS/WEEE Directive

RoHS: Restriction of the use of certain hazardous substances in electrical and electronic equipment. Starting 1st of July 2006 RoHS bans: Lead, Cadmium, Mercury, Hexavalent chromium, Polybrominated Biphenyls (PBB) or Polybrominated Diphenyl Ethers (PBDE). 0.1% by weight in homogeneous materials for all RoHS substances, except Cd which is set at 0.01%. [Kivilahti]

WEEE: Prevention of Waste Electrical and Electronic Equipment and in addition, the reuse, recycling and other forms of recovery of such wastes so as to reduce the disposal of waste.

Legislation in other countries

- China: Product scope similar to RoHS.
- USA: No federal legislation, many states have their own legislation. Example: California, Pb, Cd, Hg, Hex. Cr, 1st Jan 2007.
- Japan: Ministry of Trade and Industry (MITI) drafted a Recycling Law for certain electrical appliances coming into force in 2001 that suggested, but not mandated the removal of lead by 2005.

RoHS requires Lead-free 1st of July 2006

- Large household appliances
- Small household appliances
- IT and Telecommunication equipment
- Consumer equipment
- Light equipment (light bulbs and luminaries)
- Electrical and electronic tools
- Toys, leisure and sports
- Automatic dispensers

WEEE requires Lead-free

- Medical equipment systems (with the exception of all implanted and infected products)
- Monitoring and control instruments

RoHS Exemptions

- Medical equipment and control instruments
- Automotive, defense and aerospace industry equipment
- Network infrastructure equipment
- Storage and storage array systems (industrial applications) until 2010

Table 1.1: New combinations of solder alloys and metallization

PWB Coating	Component Coating	Lead-Free Solder
Ni/Au	Pure Sn	Sn0.7Cu
Ni/Pd/Au	Ag/Pd	Sn3.5Ag
OSP (on Cu)	Ni/Au	Sn58Bi
Pure Sn	Ag	Sn3.4Ag0.8Cu
Ag	Bi	Sn3.5Ag3Bi
Bi	UBMs	Sn9Zn

Table 1.2: Preferred lead-free surface finish materials in Europe (Source: ELFNET)

	Termination	Land	Solder Ball
Pure Sn	30%	18%	
SnCu	4%	9%	
SnAg	4%		
SnBi		3%	
Ag	4%	9%	
Au (Ni/Au; Ni/Pd/Au)	15%	27%	
Pd (Pd/Au)	4%		
SnAgCu	7%		23%
SnAgCuBi			
SnAgCuSb			
SnAgBi			
SnCuNi	4%	9%	15%
SnZn			
SnZnBi			
OSP	7%	12%	
Don’t know	22%	12%	62%

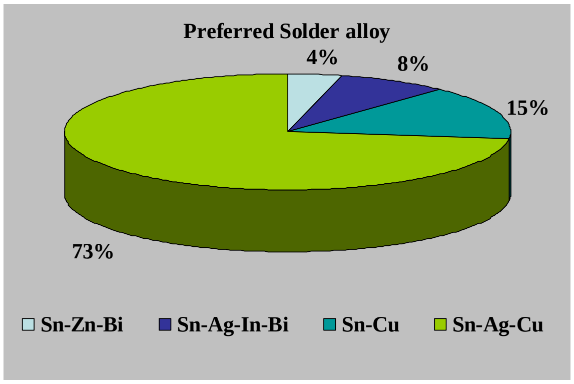


Figure 1.3: Preferred solder alloy in Japan

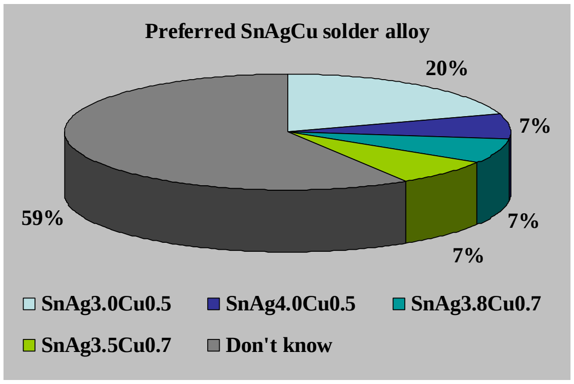


Figure 1.4: Preferred SnAgCu solder alloy in UK

1.2.2 Cost Considerations

- Materials and energy costs: Less important (<0.1% of the finished products)
- Implementation costs: Important

  But vary widely (includes process design and verification, reliability, testing, etc.)
- Yield loss: Important

  According to the calculations of the Cookson Group: assuming a lower first pass yield of, say, 92% [versus a standard baseline of 97%], but with the entire lost yield reworkable, the unit cost by about $0.5. Over a year of production, profits decrease by $350,000. But, if only 80% of the lost yield is reworkable, then unit costs rise by more than 4 times and profit drop by $1.4 million.
- Cycle times: Important

  If the cycle time is extended from 25 to 27 seconds due to higher peak reflow temperatures, almost $1 million profit is lost. An extra 1.5 hours of even maintenance per week as a result of using the higher reflow temperatures erodes away an additional $200,000 profit.

1.2.3 Reliability Issues for testing of lead-free electronics

- Lead-free technology has more complex reactions and more complex microstructures
- Testing is becoming ever more important since it is expensive
- Better understanding of failure mechanisms under different loading conditions is needed

- With the development of concurrent testing approaches one aims to simulate real loading conditions of components and assemblies:
    1. Thermal cycling combined with drop or vibration testing
    2. Power cycling combined with vibration testing
    3. Vibration testing of warm and hot components
    4. Vibration testing in corrosive environments
- Understanding the results of concurrent testing, calls for the employment of modeling and simulation tools.
- Impact of increasing functionality and performance on interconnection technologies
- Higher the contact densities, smaller spacing between components and boards, therefore higher strains and stresses
- Higher local T-gradients, micro structural coarsening, inferior mechanical performance

1.3 Models for Reliability Prediction of Fine-Pitch BGAs and CSPs in Shock and Drop-Impact

Portable products face the challenges of ever increasing functional density, shorter product cycles, and pressure to reduce cost. Increasing functional density has lead to the explosive growth in chip scale package (CSP) usage. The expected product life for a portable product is typically short compared to many other product categories; however, portable products must survive multiple drops.

The decreasing I/O pitch of CSPs and the resulting smaller pads and solder joints, make the drop requirement more challenging. There are two approaches to improving drop reliability. The first is the mechanical design of the product to minimize the shock and flexing of the printed circuit board that occurs when the product is dropped. This approach places pressure on the time-to-market constraint. The second approach is to use underfills to mechanically reinforce the CSP solder joints. Underfills add cost and cycle time to the manufacturing process. Development of a robust mechanical design, capable of resisting multiple drops is thus used more frequently as the preferred approach.

Electronics inside portable electronic products may be subjected from few hundred Gs to thousands of G’s during an accidental drop from near ear-level (on average approximately 5 ft drop height). Use of experimental approach to test out every possible design variation, and identify the one that gives the maximum design margin is often not feasible because of product development cycle time and cost constraints. There is a fundamental need for understanding and predicting the electronic failure mechanics in shock and drop-impact.

1.4 Models for Shock and Vibration Survivability of Electronic and MEMS Packaging

Test methods for drop reliability can be broadly classified into constrained and unconstrained or free drop. Examples of constrained drop include the JEDEC test method. The JEDEC test standard [2003] is often used to evaluate and compare the drop performance of surface mount electronic components for handheld electronic product applications. This is a component level test. The primary intent is to standardize the test board and test methodology to provide a reproducible assessment of drop performance of surface mount electronics. However, the correlation between drop-performance in the test and that at the product-level is weak. Product-level failures are often influenced by housing design, in addition to drop-orientation, which may not always be perpendicular to the board surface. Previous researchers have investigated constrained drop techniques for edge-drop orientation of the test board and shown good repeatability. Testing methods for free drops have been proposed using high speed photography. However repeatability of these drops is difficult because of the phenomenon of ‘clattering’ in which one corner of the product touches the ground first and the other corner rebounds repeatedly.

The analyst is typically interested in the cycles to failure that a package design configuration and cyclic loading condition will cause. This requires the utilization of a life prediction methodology in which a typical data provided can be translated into cycles to solder joint failure. Limited correlation has been achieved with acceleration, velocity and displacement time histories. Life prediction of electronics in shock-impact has been scarce. Use of the peak von-mises stresses and normal stresses with power-law relationships to predict drops to failure has been investigated.

Strain behavior of electronic assemblies is not elastic and the large transient deformation is often not accurately represented by the small strain theory. In addition, the final or the peak strain does not capture the final strain or damage state of the assembly. The rate-of-change of deformation and the latent damage in previous drops impacts the susceptibility to failure during successive drops.

Dynamic responses at board level at product level have been measured by previous researchers. Failure may not happen in the first drop, and damage may be cumulative. There is need for techniques and damage proxies which enable the determination of failure-envelopes and cumulative damage during overstress and repetitive loading for various packaging architectures. Presently, investigation of dynamic responses such as deflection, velocities, strains etc during the transient event gives us an insight about the failure mode and failure mechanism of solder joints. However, there are experimental limitations of measuring field-quantities and their derivatives at the board-solder joint interface, primarily because of the small size of interconnect in fine-pitch ball-grid array packages. There is need for damage proxies to interrogate state of the material and determine cumulative damage at any instant of time. In this dissertation, a methodology has been developed to determine the damage progression versus number of drops by studying the transient strain history of the test boards. The damage proxies developed in this dissertation can be used on strain response from simulations or from experimental data in controlled drop or shock tests. Damage proxies developed provide objective and quantitative failure definitions that allow for variation in orientation, component location, in addition to load history. Damage proxies also allow for determination of failure envelopes for component deployment in various product level applications.

1.5 Life Prediction and Damage Equivalency for Shock Survivability of Electronic Components

A methodology has been developed to determine the damage progression versus number of drops by studying the transient strain history of the test boards. The development of a solder-joint stress based relative damage index has been investigated to establish a method for damage equivalency. Deformation kinematics has been measured with the help of ultra high-speed data acquisition and video systems. Experimental data has been correlated to the finite element models. Modal Analysis, Wavelet Decomposition, and Explicit Finite Element analysis has been used to assess reliability and performance of the electronic boards. The damage proxies developed in this dissertation can be used on strain response from simulations or from experimental data in controlled drop or shock tests. Damage proxies developed provide relatively objective and quantitative failure definitions that allow for variation in orientation, component location, in addition to load history. Damage proxies also allow for determination of damage equivalency for component deployment in various product level applications.

1.6 High Speed Digital Image Correlation For Transient-Shock Reliability of Electronics

A methodology has been developed to identify the damage progression versus number of drops by studying the transient strain history of electronic assemblies from digital image correlation in conjunction with statistical pattern recognition. Manifestation of damage has been studied through analysis of failure modes and correlation with degradation in confidence value. The development of a statistical-pattern recognition based damage proxies has been investigated to establish a method for identification of impending failure. The damage proxies developed can be used on strain response from simulations or from experimental data in controlled drop or shock tests. Damage proxies developed provide relatively objective and quantitative failure definitions that allow for variation in orientation, component location, in addition to load history. Damage proxies are scalable and allow for identification of impending failure in product level applications. Digital image correlation technique has been used to investigate dynamic degradation due to drop, thermal aging, and thermal cycling. The damage accumulation due to progressive drop has been studied.

CHAPTER 2

LITERATURE REVIEW

Electronic equipment can be subjected to many different forms of vibration over a wide range of frequencies and acceleration levels. It can be said that all electronic equipment will be subjected to some type of vibration at some time in its life. If the vibration is not due to an active association with some sort of a machine or a moving vehicle, then it may be due to transporting the equipment from the manufacturer to the customer. Vibration is usually considered to be an undesirable condition and can produce many different types of failures in electronic equipment.

Mechanical vibrations can have different sources. In vehicles such as automobiles, trucks and trains most of the vibration is due to the rough surfaces over which these vehicles travel. In airplanes, missiles and rockets the vibration is due to jet and rocket engines and to aerodynamic buffeting.

Portable electronic devices such as pagers, palm-top organizers and compactly designed cell phones are vulnerable to damage from mechanical shock and vibration. With a drop from the desk or an inadvertent bump against a wall, closely assembled components can collide rendering the device inoperable.

Over a period of time, the post-shock ringing vibration can fatigue boards and connectors, creating hard to spot electrical problems. Therefore, the testing of the electronic assemblies should include shock and vibration analysis.

2.1 Board-Level Reliability of Lead-free solder

2.1.1 Effect of Underfill on Reliability

Underfill materials are often used to enhance the reliability of a variety of component types, including flip-chips, chip scale packages (CSPs), and ball grid arrays (BGAs) [Young 1999, Ghaffrian 2000, Hannan 2001, Peng 2001, Liu 2002, Tian 2003]. Most manufacturers that use flip-chips on board (FCOB) or a flip-chip in a package (e.g. FC-BGA) underfill them due to the large CTE mismatch between the silicon die and the substrates. The other packages may only be underfilled if there is either a perceived risk to the products (e.g. a cell phone may undergo frequent drops) or for a high reliability application (e.g. avionics). The CTE matching of the underfill materials is typically achieved through the addition of silica-based fillers. This addition lowers the CTE and thus provides a gradient between the silicon chip and the substrate.

Drop tests were performed to evaluate the relative performance of the underfills, and the results indicated that all of the underfills (5-6x) improved the reliability in the drop test to nonunderfilled parts. The most common reason to underfill CSPs is to improve their shock and vibration reliability (drop testing). However their widespread use has been limited due to complex application requirements that restrict the integration of underfills into SMT assemblies, and also complicate repair and rework [Yaeger 2001].

2.1.2 Effect of Surface Finish on Reliability

Various pad finishes such as ENIG (Electroless Nickel Immersion Gold), Solder on Pad (SOP), HASL (Hot Air Solder Levelling), Immersion Silver, Immersion Gold has been studied under high strain rate events such as cyclic bend tests, and vibrations caused due to drop impact. Performance of the Flip-Chip BGAs, CSPs are studied according to JEDEC standards [Jiang 2005], ball pull and shear tests [Bansal 2005, Song 2006], horizontal free drop of PCB assemblies in face-up and face-down position [Xie 2006]. Previous research involved comparative study of failure modes based on area percentage of solder remaining on the pad [Song 2006], crack progression based on cross-sectioned samples after failure.

It has been shown in the past that Flip-chip BGA substrates with SOP surface finish performs best compared to Electrolytic NiAu and ENIG under ball pull test [Bansal 2005]. Ni/Au performs better than OSP on board level drop tests [Jiang 2005]. ENIG was better than OSP and ImAg for bend test and drop test [Hossain 2006, Chong 2006], OSP pads generated more brittle failures in ball pull tests compared to ENIG [Song 2006], OSP enhanced drop performance compared to ENIG for PBGA packages subjected to ball pull tests [Chai 2005, Xie 2006].

Extensive work has been conducted to study the effect of PCB surface finish on the thermal fatigue reliability performance of lead-free solder joints and their underlying failure mechanism. However, very few papers have been published on the board level reliability under drop conditions [Wang 2003, Chong 2004, Lall 2004, Ratchev 2004, Alajoki 2005, Jiang 2005].

[Chong 2004] studied the influence of different package types and the impact of PCB surface finishes of OSP and ENIG (Electroless Ni/Immersion Au) were examined. The drop test results showed that lead-free solder joints on the ENIG finish have weaker drop reliability performance compared to the leaded and lead-free solders on an OSP finish.

OSP finished substrates consistently performed the best for high strain rate monotonic flex testing. Electrolytic NiAu had a lot more scatter because of mixed failure modes, but had acceptable performance. For 3-point and 4-point bend test at 25 degC and 125 degC, fatigue resistance of VQFN with OSP finish is slightly better than that of Ni/Au (ENIG) finish [Pang 2006]. OSP board finish is slightly better than ENIG in terms of cycles-to-failure [Tasooji 2006]. [Saha 2004] postulated the formation of Cu6Sn5 intermetallic reaction layer resulted in good metallurgical bond with the Cu pad at component and board interface in thin (30-100 mm) solder joint under drop and shock environment. [Chong 2004] showed lead-free on ENIG board finish were weaker than OSP surface finish.

2.1.3 Effect of Thermal Aging on Reliability

Customers expect their portable products to survive dropping after some use time in the field, so portable electronic products such as cellular phone should undergo thermal aging prior to the drop and bend tests. [Yang 1994, Chiu 2004] conducted drop tests and shear tests of ball grid arrays (BGAs) with Sn-Ag-Cu solder balls on Cu pads after thermal aging at 100^0C, 125^0C, 150^0C, 175^0C for 3, 10, 20, 40, and 80 days.

Kirkendall voids were observed at the Cu to Cu3Sn interface. Voids occupied 25% of pad/solder interface after only 3 days of 125^0C aging, and the void density increased with the aging time and temperature. The drop performance degraded 80% from time 0 to 10 days at 125^0C.

[Date 2004] performed miniature Charpy tests on solder balls bonded to Cu, which were subsequently aged at 150^0C for upto 1000 hrs. Ductile to brittle transition associated with the fracture inside the solder to within the interfacial intermetallic compound (IMC phase was seen as the aging time increased. [Ahat 2001] reported a study of interface microstructure and shear strength of 96.5Sn3.5Ag and 62Sn36Pb2Ag on Cu after aging at 250^0C for 0, 50, 250, 500, and 1000 hrs. The shear strength of both the Sn-Ag and Sn-Pb-Ag decreased with aging time, and the fracture mode changed from mixture of solder and IMC at zero aging time, to a complete fracture of the IMC layer after 1000 hrs aging.

[Mei 2005] carried out a study that focused on two issues: the conditions for void formation and the effect of voids on solder joint reliability. Drop tests showed aged BGAs did not fail at the voided interface; rather the failures occurred inside the solder joint or PCB laminate. The shock strength at 400 G of BGA packages aged for 20 days at 125^0C did not degrade.

2.2 Parameters Influencing Drop Reliability

The average strain-to-failure of Ni/Au BGA substrate improves with increasing reflow temperature, while Cu substrates show a reduction in drop performance.

A solder ball with larger diameter improves impact performance based from numerical simulation under drop impact. It is evident that the underfill decreases the plastic strain and improves the impact performance significantly. Underfill accelerates attenuation of the stress wave and reduces strain. Impact pulse affect the peeling stress in critical solder joints and thus affect the solder joint reliability performance of drop impact. Drop reliability depends on the amount of shock level given to the product. Input acceleration studied varied from 50,000 Gs to 6000 Gs for the time period of 0.5ms to 0.25 ms [Groothuis 2005].

One of the researches [Zhao 2006] involved modeling a mobile phone as two degree of freedom system with free drop in horizontal orientation with mold compound facing down. All the components on PCB including PCB board are considered one mass, and the spring was offered by the system by the elasticity of the PCB board. Outer casing acts as the other mass and the other spring. It was believed that a tall and thin solder joint would be more reliable for thermal cycling testing where CTE mismatch drives a shear loading mode. It was seen that effect of ball height on tensile stress was very weak, suggesting little influence on drop test performance. Small changes in the die stack or package materials would not have a large impact on the shock performance. The effect of package thickness and ball pattern may have largest impact on the reliability of a design. Sacrificial balls designed for temperature cycling may not provide adequate protection for functional balls in drop test. [Sharan 2006] showed low stiffness and mass ratio results in higher displacement. Higher mass and stiffness ratios can not be used as it will result in higher acceleration and ultimately higher dynamic stresses in the system.

2.3 Failure Criteria in Drop and Shock

[Tee 2004] drop tested TFBGA package on a test board according to JEDEC standards, the output results extracted from the FEM models were normal stress in PCB length direction, first principal stress, vertical normal stress or peeling stress, shear stress and Von Mises stress. All the stresses vary cyclically under PCB vibration. Comparing all the stresses at the same point, peeling stress had higher magnitude and was dominant compared to horizontal normal and shear stresses. Hence peeling stress can be used as a failure criterion. [Irving 2004] used a quarter symmetry model of flip-chip packages. Max Von Mises, max Shear stress and max plastic work was compared among different packages as a failure criteria.

[Zhu 2005] used effective plastic strain based failure criteria to determine the initial or yield in BGA solder joint. Effective plastic strain was accumulated and monotonically increased as PCB board oscillating after first shock and reached a constant level as vibration was damped out, which also reflects total damage. The effective stress (Von Mises) and peeling stress however was shown oscillating due to recoverable elastic deformation in PCB which results in difficulty to be used as failure criteria to quantify BGA reliability performance because the effect of wave form of responses which reflects stiffness of the board cannot be neglected in cross comparison between different board design. [Newman 2005] concluded interfacial voids appear to relate to observed brittle solder joint fractures. Fracture strength has been characterized by various measures of force and/or energy in these high speed shear studies. [Ou 2005] used impact toughness was the criteria to study the transition from ductile to brittle failure located at the place between UBM metallization layer and Ni(Cu)-Sn intermetallic compound.

2.4 Life Prediction Models

Dynamic responses at board level [Sogo 2001, Mishiro 2002] at product level [Lim 2002, 2003] have been measured by previous researchers. Failure may not happen in the first drop and damage may be cumulative. There is a need for techniques and damage proxies which enable the determination of failure-envelopes and cumulative damage during overstresses and repetitive loading for various packaging architectures. Presently, investigation of dynamic responses such as deflection, velocities, strains etc during the transient event gives us an insight about the failure mode and failure mechanism of solder joints.

Life prediction models based on strain range, accumulated creep strain or accumulated strain energy strain density during a temperature cycle have been proposed [Coffin 1954, Manson 1965, Darveaux 1995, Lee 2000]. Life prediction parameters used are Monkmann-Grant equation for creep rupture and time-fraction rule [Syed 2004]. Coffin-Manson fatigue models [Che 2004] have been implemented for packages subjected to temperature cycling. Various packages including TFBGA (Thin-profile Fine-Pitch BGA), VFBA (Very-thin-profile Fine-Pitch BGA), CSPs have been tested with thermal cycling and life prediction models based on Anand's constants provided by Darveaux [Ng 2005] have been spotted in the literature.

Linear superposition method by Miner's Law has been assumed for electronic assemblies subjected to vibration with clamped-clamped boundary conditions [Pang 2004, Wong 2004], the number of cycles required to produce failure are extracted from mean-time-to-failure (MTTF). The actual number of fatigue cycles accumulated in different environment was calculated experimentally. Stress based fatigue models are developed [Pang 2004, Perkins 2004] for flip-chip, and ceramic column grid array (CCGA) packages. For JEDEC drop tests of electronic assemblies, peeling stress and mean impact life based life prediction models have been proposed [Luan 2005].

2.5 Finite Element Analysis

Modeling technique with a comprehensive failure criterion including high strain rate effect is necessary to quantitatively evaluate and benchmark BGA package reliability performance for different board designs. Dynamic responses in CSP/BGA in different boards and product phone have been characterized by using nonlinear dynamic finite element software, LS-Dyna and Abaqus. Different failure criteria, such as plastic strain and stress based are investigated and compared. [Asme05] has shown good correlation between validation test and numerical result by using plastic strain based criterion.

There are several criteria quantifying the BGA package performance during dynamic shock load, such as stress based [2], force based [3], and plastic strain based [4-5]. Stress and force based criteria use peak responses in the BGA during shock vibration using linear material properties for the whole model including BGA solder. The advantage of these two criteria is to quickly evaluate design options and identify the weakest location of BGA by comparing the peak responses in a test board. Whereas plastic strain based criteria is to use accumulated plastic strain which enables to accumulate the solder damage not only during shock impact, but also in the post impact phase due to board oscillations.

To study the actual behavior of the package, 3D model with fine mesh and accurate material nonlinearity must be included in the model. With fine mesh, the computational time increases, hence global-local sub-modeling techniques are studied. Various modeling approaches have been pursued to reduce computational time required for simulation. [Zhu 2001] applied solid-to-solid sub-modeling technique to analyze BGA reliability for free board level drop. The explicit time-integration is most suitable for solving wave propagation problems such as drop impact [Lall 2003, 2004]. The simulation time is determined by the size of the time step which is directly proportional to the length of the smallest element in the model.

Smeared properties have been derived for the components followed by Clech. This approach was used from development of closed form models for solder joints subjected to thermal fatigue. [Lall 2006] previous modeling approaches include, solid-to-solid sub-modeling [Zhu 2001] using half test PCB board, shell-to-solid sub-modeling technique using a quarter-symmetry model [Ren 2003, 2004]. Inclusion of model symmetry in state-of-art models save computational time, but targets primarily symmetric mode shapes.

The most important advantage of the explicit dynamic formulation is its easy implementation and robustness. No equations are solved, no check of unbalanced forces is undertaken, and therefore, no convergence control is needed. As a consequence, the computational speed is higher and the memory requirements are less than those usually required by (implicit) quasi-static formulations. Major disadvantages are generally related to accuracy of the results (e.g. local stresses).

Fewer integration points are used as compared to the implicit formulation hence it saves computational time. Shell-elements (S4R) are used to model the PCB which accounts for large strains [Abaqus^{TM}]. The solder interconnects has been modeled using three-dimensional, linear, Timoshenko-beam element (B31) elements. Three-dimensional beams have six degrees of freedom at each node including three translational and three rotational degrees of freedom. The B31 elements allow for shear deformation. It is assumed that the strain in the beam is constant throughout the beam.

To further cut down computational time during explicit dynamic analysis, mass scaling technique is widely used. This approach is used in sheet-metal forming analysis [Silva 2004] and transient dynamic analyses [Towashiraporn 2006]. The cost of a numerical simulation depends only on the size of the model and the number N of time increments that are required to perform the entire shock event. Possible approaches to reduce the overall CPU time require either to increase the size of the time increments, Δt, or to reduce the total time t of the operation. The first approach known as mass scaling can be easily achieved by increasing the density of the material and thus artificially reducing the speed of the longitudinal wave.

2.6 Modal Testing of Printed Circuit Board

Due to variety of manufacturing, environmental, shipping and end-use conditions, circuit boards are subjected to potentially damaging mechanical shock loads. Electronic equipment can be subjected to many different forms of vibration over wide frequency ranges and acceleration levels.

The simplest form of periodic motion is harmonic motion, which is often selected for testing electronic equipment. Vibration-induced stress can usually lead to fatigue failure of electronic assemblies. Modal testing of flip chip on board assembly was studied subjected to sinusoidal vibration [Pang 2004]. [Pitarresi 2004] did modal analysis on a motherboard. The mass and the stiffness of these packages influence the motherboard response. Both shock response spectrum (SRS) method and an implicit direct integration (i.e. time marching) scheme was used to simulate shock response and its modal characteristics.

[Kim 2001, Pittarresi 1991] have done experimental and modeling work to characterize the natural frequencies, mode shapes, transmissibility and damping at the board level. Experimental and numerical modal testing of the complete cell-phone and portable digital assistants (PDAs) were analyzed in terms of impact forces, accelerations and strains [Tan 2005], multi stack package composed of logic chipset package at bottom and multi chip package [Shin 2006]. The severity of impact induced on the interior PCBs and their electronic components could be determined from product-level drop tests. Modal parameters were extracted and correlated. [Luan 2005, Lim 2005] developed numerical models for modal analysis of PCB. They showed the natural frequencies and the mode shapes are critical to solder reliability.

2.7 High Speed Digital Image Correlation

High speed photography has been used to measure deformation and strain sheet metal forming analysis, automotive crash testing, rail vehicle safety [Kirpatrick 2001], air-plane safety [Marzougui 1999], modal analysis of blades, disks, shearography which involves laser NDT for rapid honeycomb delamination tests, dynamic fracture phenomenon, tire tests, rotating components, exhaust manifolds, split Hopkinson bar tests, package integrity/hermiticity (MIL-STD-883) tests. High-speed cameras measure impact speed, force, and deformation due to shock, and thermal loading. It is also used for quantitative evaluation of in-plane deformation characteristics of geomaterials [Watanabe et al. 2005], and in medical fields to assess local failure of bone by implementing mechanical compression testing of bone samples [Thurner 2005].

However the measurement of field quantities is limited to a specific location or discrete target points. It is not feasible to extract data by using discrete targets as it involves time and money. Techniques such as Moiré Interferometry is an option to get the overall deformation contour, but it is often time consuming and involve expensive grates. Digital image correlation is the state-of-art technique which super-cedes the later as it is less time consuming. The sample preparation is simple and quick. The test specimens are speckle painted and with the help of high-speed cameras, full-field deformation can be measured on any oblong test specimen. Feasibility of this technique has been explored on electronic assemblies under free drop and constrained drop.

In electronics industry, digital image correlation has been used to study the stresses in solder interconnects of BGA packages under thermal loading [Zhou 2001, Yogel 2001, Rajendra 2002, Zhang 2004, Zhang 2005, Xu 2006, Bieler 2006, Sun 2006], material characterization under thermal loading [Srinivasan 2005, Gu 2006], parametric study of speckle size [Gu 2006], dynamic testing to study deformation for flexible bodies [Reu 2006], material characterization at high strain rate [Tiwari 2005].

Stresses and strain in flip-chip die under thermal loading [Kehoe 2006], fracture toughness of underfill/chip interface due to temperature and aging conditions [Song 2006]. Data is scarce for the behavior of the printed circuit board transient dynamics in shock, which is a major reliability issue in portable electronics.

2.8 Dynamic Material Property Testing

The US Air Force estimates that vibration and shock cause 20 percent if the mechanical failures in airborne electronics [Zhao 2000]. Static material properties of solder are not sufficient to simulate solder ball deformation at high strain rate. Dropping a cell phone produces high strain rates of the order 1000 per sec [Seah, Lim 2002]. Accurate material models are necessary to obtain meaningful results in computational simulation. [Ong 2004] developed material testing and process of developing a material model for solder under impact loading. This model incorporated the strain rate sensitivity of the Sn63/Pb37 solder using Split Hopkinson Pressure Bars. The accuracy of the material models was evaluated from experimental and finite element simulation. Examination of the fractured surfaces showed there is transition from ductile to brittle fracture as strain rate increased from 450 to 2720 per sec. There was a 2% increase in strain which resulted in stress to increase from 450 to 112MPa. [Seeling 2000] showed that tensile and compressive modulus is quite different for high rate events. Very limited data is available for material testing and to develop finite element models based on these material properties.

2.9 Research Objectives

The Main objective of this research was to develop damage prediction models for various packaging architectures such as chip scale packages (SnPb/lead-free), plastic ball-grid-array packages (PBGA), quad-flat-nolead (QFN) packages under overlapping stresses caused due to thermal cycling, thermal aging and repetitive drop. Research was divided into five parts and is presented in the following chapters.

Chapter 3 studies the transient dynamics of the printed circuit board during a 6ft vertical drop. Explicit finite element models have been developed using smeared property approach, reduced integration formulation includes- shell and solid elements. Model predictions have been validated with experimental data. Packages examined were 8mm chip scale packages, 15mm PBGA, PQFN, 16mm CCBGA. High-speed data acquisition system has been used to capture in-situ strain, continuity and acceleration data.

Chapter 4 includes developing damage proxies to model drop and shock survivability of electronic packaging. Data on damage progression under transient-shock and vibration in both 95.5Sn4.0Ag0.5Cu and 63Sn37Pb ball-grid arrays has been presented. The concept of relative damage index has been used to evaluate and predict damage progression during transient shock.

In chapter 5, the development of a solder-joint stress based relative damage index has been investigated to establish a method for damage equivalency. Modal Analysis, Wavelet Decomposition, and Explicit Finite Element analysis has been used to assess reliability performance of the electronic boards. Deformation kinematics has been measured with the help of ultra high-speed data acquisition and video systems.

Experimental data has been correlated to the finite element models. Failure predictions along with their modes and mechanisms have been discussed. Damage proxies for failure mechanisms in first-level interconnect have been developed. The approach is scalable to a wide variety of electronic applications.

Chapter 6 includes a methodology to identify the damage progression versus number of drops by studying the transient strain history of electronic assemblies from digital image correlation in conjunction with statistical pattern recognition. Manifestation of damage has been studied through analysis of failure modes and correlation with degradation in confidence value. The development of a statistical-pattern recognition based damage proxies has been investigated to establish a method for identification of impending failure. Damage proxies developed provide relatively objective and quantitative failure definitions that allow for variation in orientation, component location, in addition to load history. Damage proxies are scalable and allow for identification of impending failure in product level applications. Digital image correlation technique has been used to investigate dynamic degradation due to drop, thermal aging, and thermal cycling.

CHAPTER 3

MODELS FOR RELIABILITY PREDICTION OF FINE-PITCH BGAS AND CSPS IN SHOCK AND DROP-IMPACT

3.1 Introduction

Portable products face the challenges of ever increasing functional density, shorter product cycles, and pressure to reduce cost. Increasing functional density has lead to the explosive growth in chip scale package (CSP) usage. The expected product life for a portable product is typically short compared to many other product categories; however, portable products must survive multiple drops. The decreasing I/O pitch of CSPs and the resulting smaller pads and solder joints, make the drop requirement more challenging. There are two approaches to improving drop reliability. The first is the mechanical design of the product to minimize the shock and flexing of the printed circuit board that occurs when the product is dropped. This approach places pressure on the time-to-market constraint. The second approach is to use underfills to mechanically reinforce the CSP solder joints. Underfills add cost and cycle time to the manufacturing process. Development of a robust mechanical design, capable of resisting multiple drops is thus used more frequently as the preferred approach.

Electronics inside portable electronic products may be subjected from few hundred Gs to thousands of G's during an accidental drop from near ear-level (on average approximately 5 ft drop height). Use of experimental approach to test out every possible design variation, and identify the one that gives the maximum design margin is often not feasible because of product development cycle time and cost constraints. There is a fundamental need for understanding and predicting the electronic failure mechanics in shock and drop-impact.

Very limited work has published on correlation of experimental data during drop with prediction of transient dynamics. Modeling methodologies for accurately modeling and predicting deformation kinematics of electronics are largely unexplored.

3.2 Test Vehicle

Two test boards have been used to study the reliability of ball-grid arrays and chip-scale packages. Test Board A includes 8mm flex-substrate chip scale packages, 0.5mm pitch, 132 I/O. Each board has 10 CSP locations on one side of the board only (Figure 3.1). Test Board B includes, 15mm CSP, 16mm C2BGA, 27mm BGA, PQFN, and transformer. Two versions of the 8mm CSP were studied including, conventional eutectic solder, 62Sn/36Pb/2Ag and lead-free solder balls 95.5Sn/4.0Ag/ 0.5Cu. Table 3.1 shows the package attributes for both test boards.

Test board A is made of FR-4 and Test Board B is made of FR4-06 (Tg is approximately 165°C). Both test boards were based on standard PCB technology with no build-up or HDI layers. Test Board A was 2.95" by 7.24" by 0.042" thick. Test Board B was 4" by 3.5" by 0.042" thick.

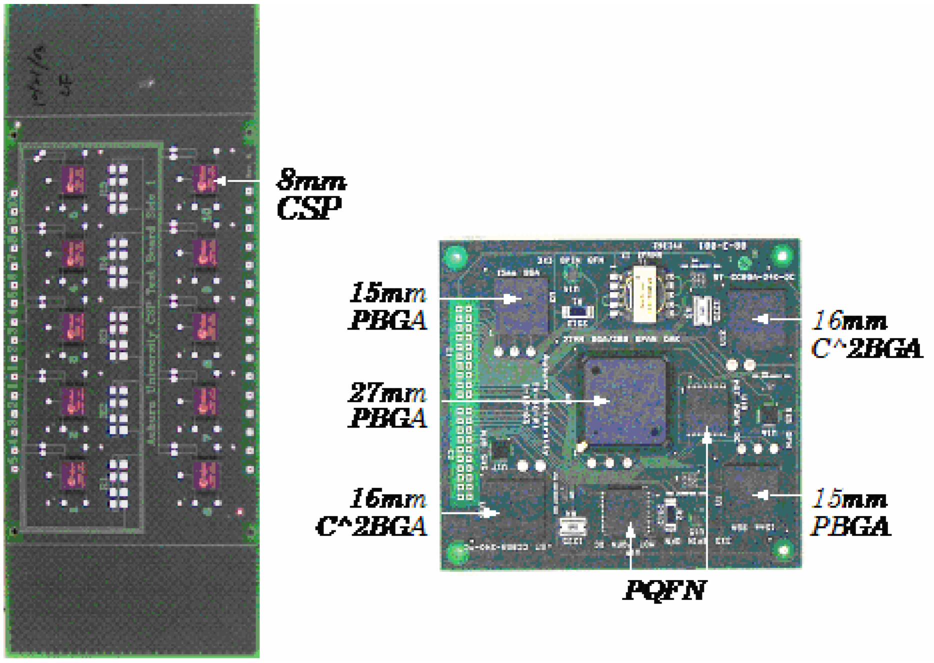


Figure 3.1: (a) BGA Test Board A (8mm Chip-Scale Package) and (b) BGA Test Board B.

Table 3.1: Test Vehicles.

Body Size	Ball Count	Ball Pitch (mm)	Thermal Balls	Die Size (mm)	Substrate Pad Diameter (mm)	Ball Diameter (mm)
Test Board A						
8mm 62Sn36Pb2Ag	132	0.5	None	3.98x3.98	0.28	0.3
8mm 95.5Sn4.0Ag 0.5Cu	132	0.5	None	3.98x3.98	0.28	0.3
Test Board B						
27 mm BGA	388	1	36 (6X6)	10X10	.5	.60
16 mm C2BGA	240	.8	None	5.0X5.0	.45	.53
15 mm BGA	193	.8	25 (5X5)	8.6X8.6	.4	.60

3.3 Kinematic Deformation

3.3.1 High Speed Imaging

The test boards were subjected to a controlled drop. The drop height was varied from 3 feet to 6 feet. Component locations on the test boards were instrumented with strain sensors. Strain data was acquired during the drop event using a high-speed data acquisition system at 5 million samples per second. The drop-event was simultaneously monitored with ultra high-speed video camera operating at 40,000 frames per second. Targets were mounted on the edge of the board to allow high-speed measurement of relative displacement during drop. Figure 3.2 shows the location of targets for Test Board A. The test boards were dropped in their vertical orientation with a weight attached to its top edge.

An image tracking software was used to quantitatively measure displacements during the drop event. Figure 3.3 shows a typical relative displacement plot measured during the drop event. The position of the vertical line in the plot represents the present location of the board (i.e. just prior to impact in this case) in the plot with “pos (m)” as the ordinate axis. The plot trace subsequent to the white scan is the relative displacement of the board targets with respect to the specified reference.

In addition to relative displacement, velocity of the board prior to impact was measured. This additional step was necessary since, the boards were subjected to a controlled drop to reduce variability in drop orientation. Measured velocity prior to impact was used to correlate the controlled drop height to free-drop height ($v = \sqrt{2gh}$). Thus velocity prior to impact for a 6ft drop (≈ 1.83 meter) will be 5.99 m/s.

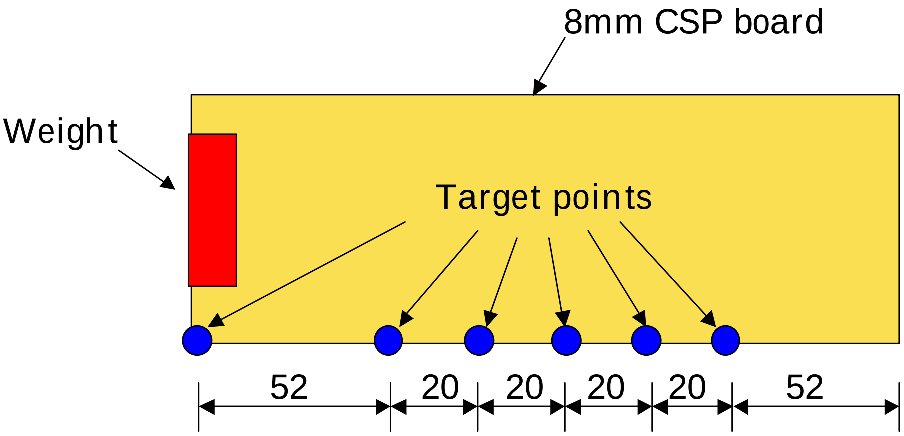


Figure 3.2: Location of target points for relative displacement measurement.

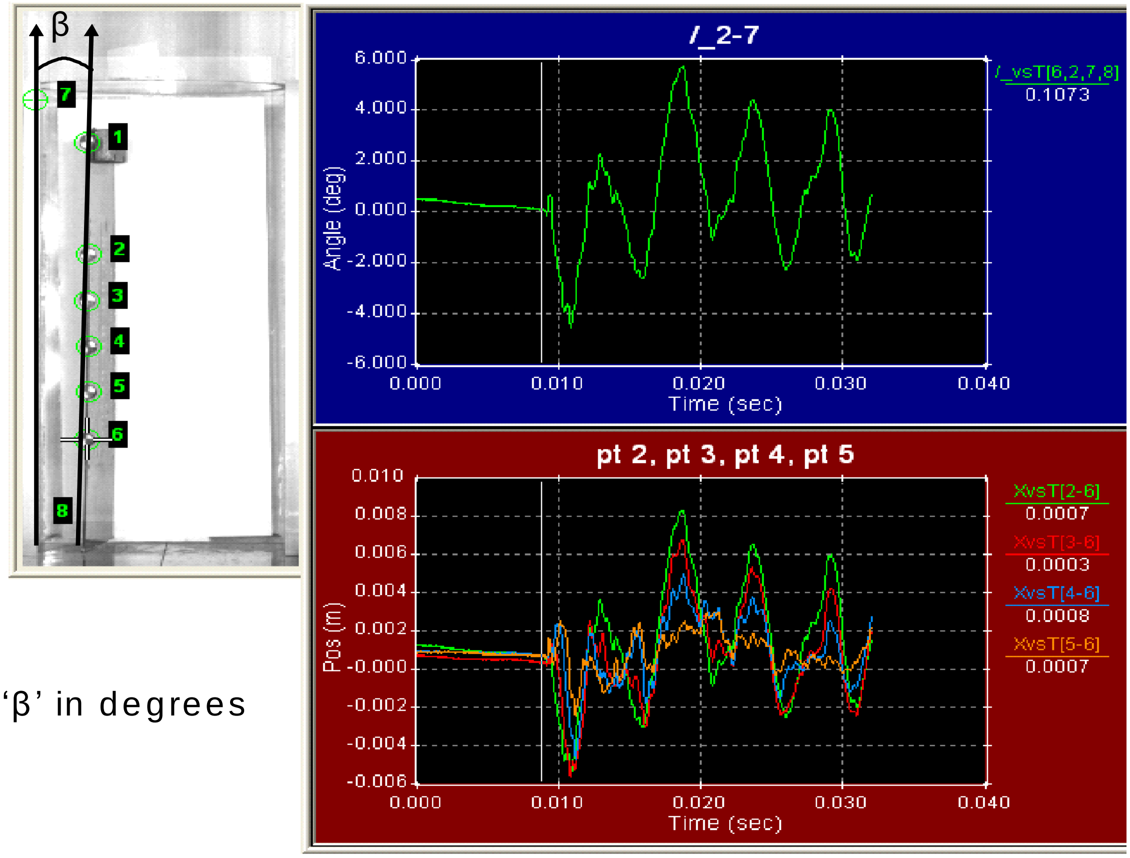


Figure 3.3: Measurement of initial angle prior to impact.

3.3.2 Drop Repeatability

Repeatability of drop orientation is critical to measuring a repeatable response. Small variations in the drop orientation can produce vastly varying transient-dynamic board responses. Significant effort was invested in developing a repeatable drop set-up. The repeatability was quantified by two parameters including angle of board prior to impact and relative displacement of the board after impact. The orientation of the board prior-to and after-impact (β) was measured relative to a known vertical stationary reference as shown in Figure 3.3. The repeatability of angle prior to impact is shown in Figure 3.4 for ten-consecutive drops. Since, the board is being dropped vertically a measured angle of impact close to zero will be desirable in this case.

Table 3.2 shows the mean values and standard deviation of initial angle prior to impact for test board A and B. Both test board showed a mean angle prior to impact in the neighborhood of 0.2 to 0.34 degrees with a standard deviation in the neighborhood of 0.9 degrees. Figure 3.5 shows the repeatability of relative displacement.

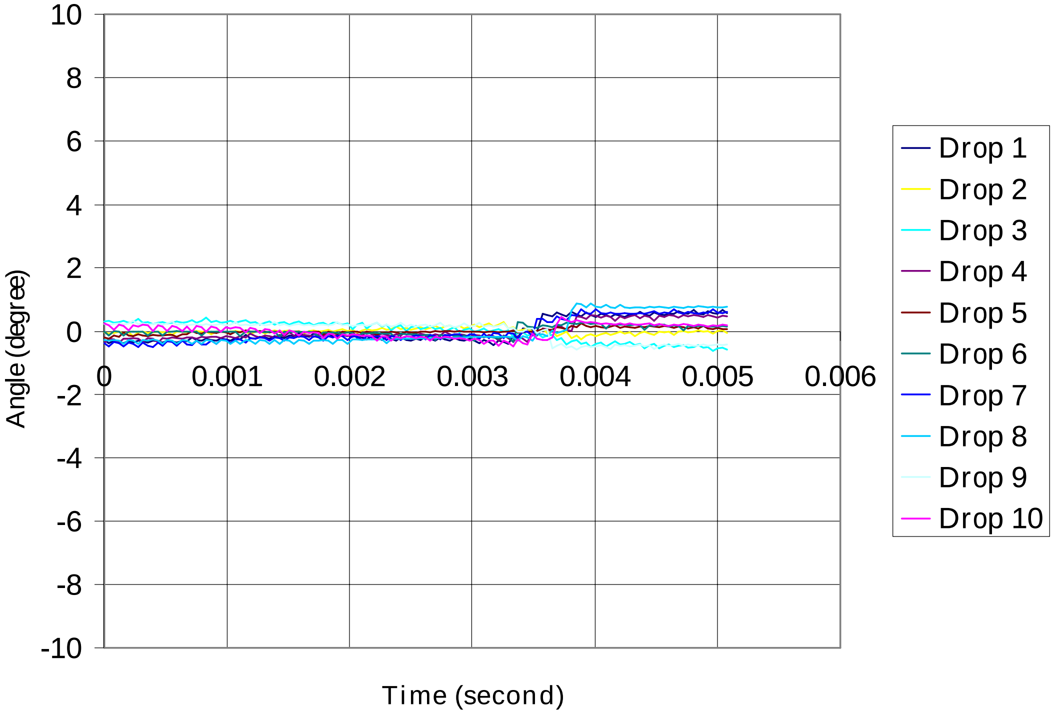


Figure 3.4: Repeatability of Initial Angle with Vertical Prior to Impact (Test Board B).

Table 3.2: Repeatability of Initial Angle Prior-to-Impact during 6ft Drop.

Test Board B		Test Board A	
Standard deviation (degrees)	Mean Value (degrees)	Mean Value (degrees)	Standard deviation (degrees)
0.87	0.2	0.34	0.90

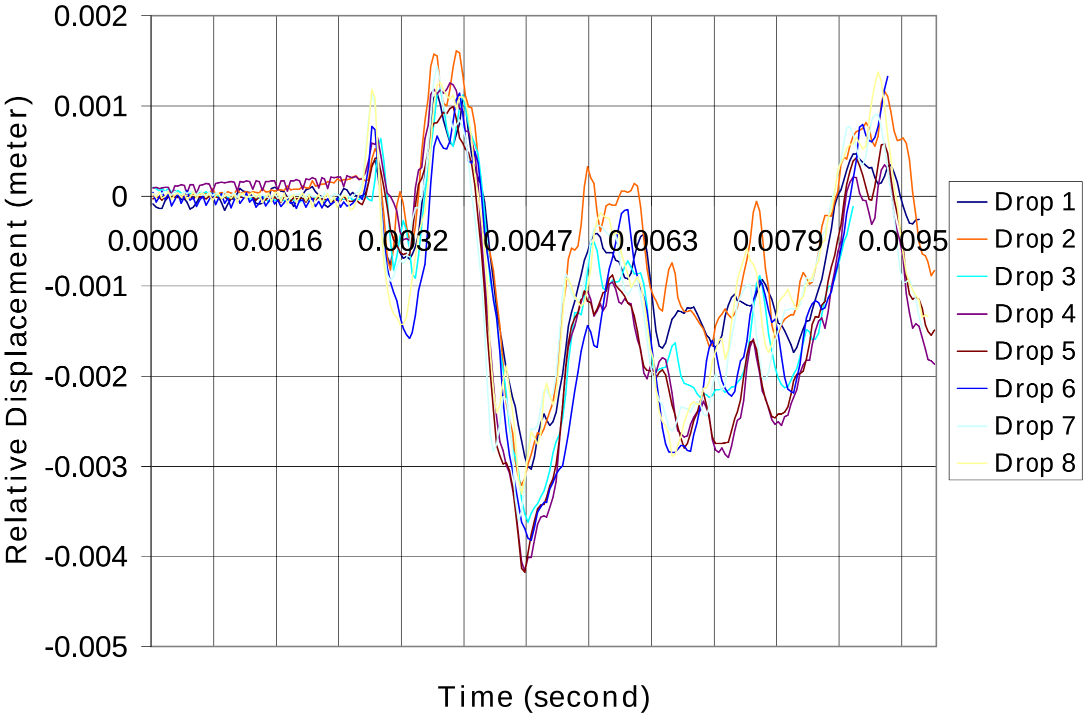


Figure 3.5: Repeatability of Relative Displacement (Test Board A).

3.4 Finite Element Analysis

3.4.1 Theory

The modeling effort has focused on prediction of transient dynamic response drop using explicit finite-element theory with reduced integration elements. The equation of motion for the board may be written as follows –

$$[M]\{\ddot{D}\}_n + [C]\{\dot{D}\}_n + [K]\{D\}_n = \{R^{ext}\}_n \tag{3.1}$$

$\{D\}_{n+1}$ and $\{D\}_{n-1}$ can be expanded using a Taylor Series about time $n\Delta t$.

$$\{D\}_{n+1} = \{D\}_n + \Delta t.\{\dot{D}\}_n + \frac{\Delta t^2}{2}\{\ddot{D}\}_n + \frac{\Delta t^3}{6}\{\dddot{D}\}_n + \ldots \tag{3.2}$$

$$\{D\}_{n-1} = \{D\}_n - \Delta t.\{\dot{D}\}_n + \frac{\Delta t^2}{2}\{\ddot{D}\}_n - \frac{\Delta t^3}{6}\{\dddot{D}\}_n + \ldots \tag{3.3}$$

Subtracting Equation 3.3 from Equation 3.2, the velocity and acceleration of the body is approximated by –

$$\{\dot{D}\}_n = \frac{1}{2.\Delta t}\left(\{D\}_{n+1} - \{D\}_{n-1}\right) \tag{3.4}$$

where $\{D\}$ is the displacement at various instants of time. Δt^2 and higher powers have been omitted. The formulas are thus second order accurate. Substituting for $\{D\}_{n+1}$ and $\{D\}_{n-1}$ in Equation (A) –

$$\begin{aligned}\left[\frac{1}{\Delta t^2}M + \frac{1}{2.\Delta t}C\right]\{D\}_{n+1} &= \{R^{ext}\}_n - [K]\{D\}_n \\ &+ \frac{1}{\Delta t^2}[M](2\{D\}_n - \{D\}_{n-1}) + \frac{1}{2.\Delta t}[C]\{D\}_{n-1}\end{aligned} \tag{3.5}$$

The above equation is a system of linear algebraic equations. If $[M]$ and $[C]$ are diagonal, then the equations are uncoupled and $\{D\}_{n+1}$ can be obtained without solving simultaneous equations. Starting from n = 0 requires $\{D\}_{-1}$ which can be computed from known initial conditions, a known displacement $\{D\}_0$ and velocity prior to impact $\{\dot{D}\}_0$ by:

$$\{D\}_{-1} = \{D\}_0 - \Delta t\{\dot{D}\}_0 + \frac{\Delta t^2}{2}\{\ddot{D}\}_0 \tag{3.6}$$

where terms with Δt^3 and higher have been omitted. $\{\ddot{D}\}_0$ is obtained from the equation of motion –

$$\{\ddot{D}\}_0 = [M]^{-1}\left(\{R^{ext}\}_0 - [K]\{D\}_0 - [C]\{\dot{D}\}_0\right) \tag{3.7}$$

To compute $\{D\}_{n+1}$ requires $\{R^{int}\}_n$. For nonlinear material constitutive laws that are functions of strain but not of strain rate, $\{R^{int}\}_n$ is easy to evaluate because $\{D\}_n$ and hence the strains at time of $n\Delta t$ are known. Explicit method is thus much better suited to treatment of material non-linearity.

Transient Dynamic Behavior of a populated printed circuit board during drop from 6ft. has been simulated using ABAQUS Explicit. An initial velocity of $\{\dot{D}\}_0 = 5.99$ m/s, equivalent of a 6ft drop has been assigned to the board, components and the weight at the top edge of the board. Two modeling approaches have been investigated. In the first model, the printed circuit board has been modeled with reduced integration shell elements. In the second model, the printed circuit board has been modeled with reduced integration solid elements. S4R shell and C3D8R solid elements have been used for the two modeling approaches respectively. The components have been modeled with solid C3D8R elements. The concrete floor has been modeled with rigid R3D4 elements. A reference node has been placed behind the rigid wall for application of constraints. Contact has been monitored between any PCB surface, CSP surface or Weight surface and only on the positive side of the floor. Node to surface contact has been used. An event length of 6 ms after impact has been modeled. Time history has been monitored at a time period of 0.1 ms at the corner of all CSPs.

3.4.2 Smeared Property Approach

Smeared properties have been derived for the components. The approach used for smeared properties in this dissertation follows the approach proposed by Clech [1996, 1998] for development of closed form models for solder joints subjected to thermal fatigue. The equation is:

$$\upsilon_C = \frac{\sum_{k=1}^{n} \upsilon_k h_k}{\sum_{k=1}^{n} h_k} \tag{3.8}$$

$$\frac{E_C h_C^3}{12(1-\upsilon_C)} = \sum_{k=1}^{n} \frac{E_k h_k^3}{12(1-\upsilon_k)} \tag{3.9}$$

$$\rho_C = \frac{\sum_{k=1}^{n} \rho_k v_k}{\sum_{k=1}^{n} v_k} \tag{3.10}$$

where

E = Elastic modulus

ν = Poisson’s ratio

ρ = Density

v = Volume

h = Layer thickness.

Subscript “C” = Indicates smeared material

Subscript k = Indicates individual materials.

The simulated weight of the model for all components and test board closely approximates the actual weight. Table 3.3 and Table 3.4 show the simulated and actual weights for test boards A and B.

3.4.3 Correlation of Experimental Results with Finite Element Models

Transient dynamic behavior of Test Board A and B has been predicted for both a 3ft and 6ft drop. Figure 3.6 and Figure 3.7 show the correlation of mode shapes from simulation and ultra-high speed video at 40,000 fps for test board A and B respectively. Three snap-shots have been shown in each case, at 2.4 ms, 4.5ms and 6ms after impact for test board A and 1.8ms, 3.9ms, and 4.8 ms after impact for test board B. The predicted transient mode shapes show good correlation with experimental data for both test boards.

Correlation of relative displacement prior to peak displacement both from model predictions and experiment have been shown in Figure 3.8 for test board A and in Figure 3.9 for test board B. The relative displacement has been plotted along the board length. The predicted displacement correlates well with experimental data. Correlation of the peak relative displacement for the solid and shell model for all component architectures has been shown in

Table 3.5. The error between the experimentally measured and predicted relative displacement peaks varies between 7% to 25%, with a majority of the values being between 7% and 20%. On average solid model performs better for majority of the component types in the study, with the model prediction exhibiting an error of 0.38% versus experimental data for test board A.

Table 3.3: Comparison of Actual and Simulated Component Masses (Test Board A).

Component	Actual (gm)	Shell Model Simulated (gm)	Solid Model Simulated (gm)
8 mm CSP	0.14	0.143	0.147
PCB	28.15	28.40	28.42
Weight	31.8	31.3	31.2

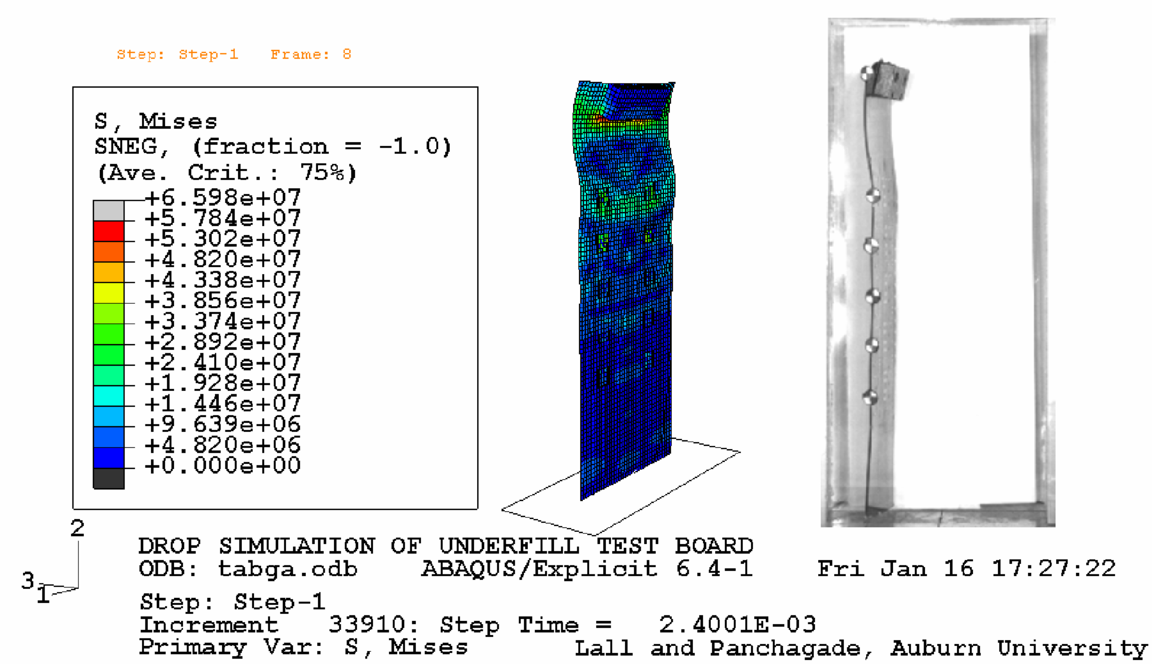
Table 3.4: Comparison of Actual and Simulated Component Masses (Test Board B).

Component	Actual (gm)	Shell Model Simulated (gm)	Solid Model Simulated (gm)
PCB	18.7	18.66	18.66
Weight	31.8	31.5	31.7
15 mm CSP	0.72	0.77	0.78
16 mm CSP	0.65	0.66	0.66
27 mm BGA	2.47	2.52	2.55
QFN	0.048	0.049	0.050
PQFN	0.59	0.61	0.62
Transformer	3.03	2.99	2.98

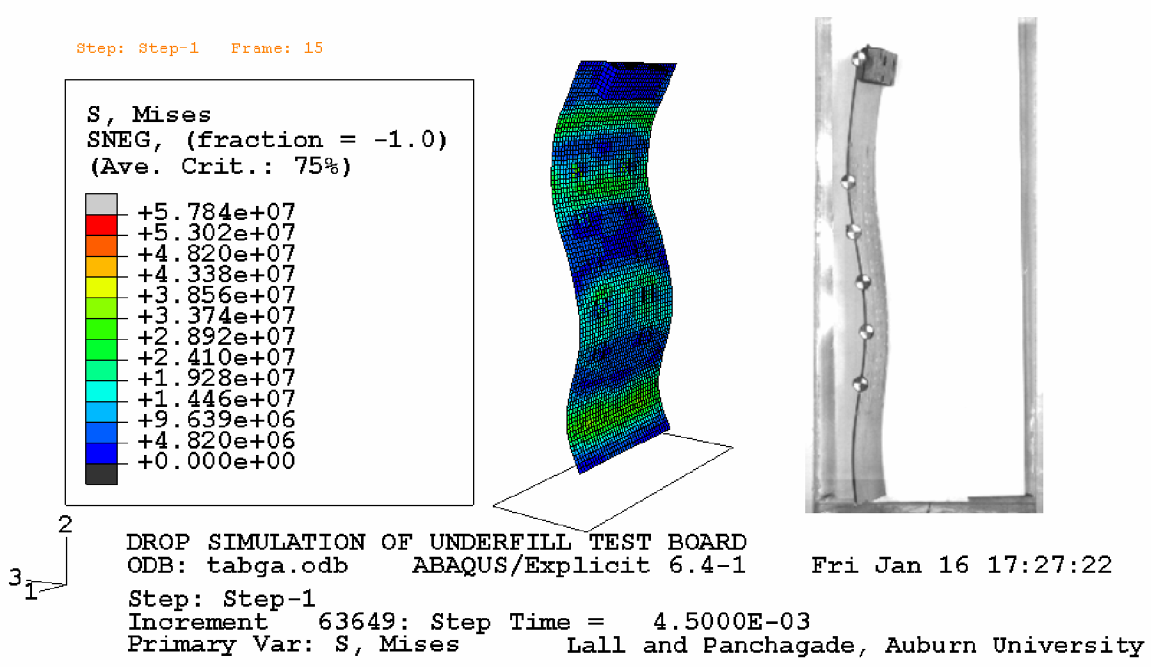
Table 3.5: Predicted Vs Experimental Peak Relative Displacement (6 ft Drop).

Component	Simulation (meter)		Expt. (meter)	Error (%)	
	Shell	Solid		Shell	Solid
8mm CSP	0.00379	0.00414	0.00416	8.8%	0.38%
15mm CSP	0.00109	0.00093	0.00122	10.65%	23.77%
16mm CSP	0.00108	0.00092	0.00123	12.19%	23.22%
27mm BGA	0.00229	0.00287	0.00289	20.76%	0.69%
PQFN	0.00217	0.00267	0.00289	24.91%	7.61%

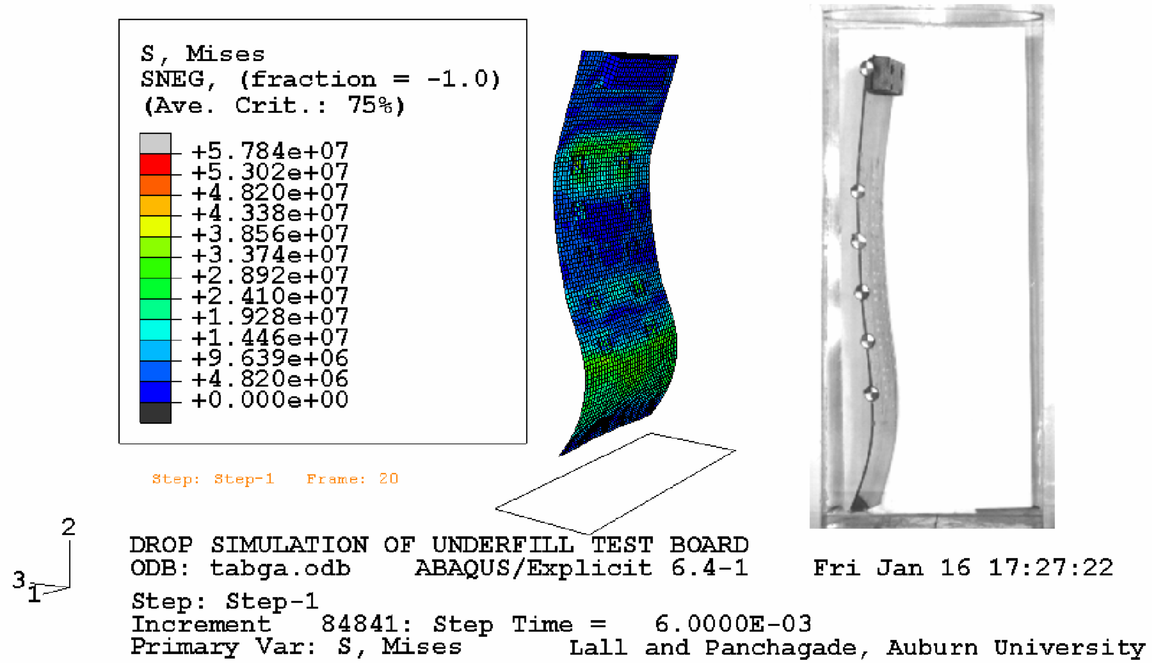
Correlation of peak strain value at component locations have also been compared with both the solid and shell model for a 3ft drop. The results from the solid and shell models correlate well with experimental data. Both models show errors in the neighborhood of 1% to 30% depending on component type (Table 3.6).



Time = 2.4 ms

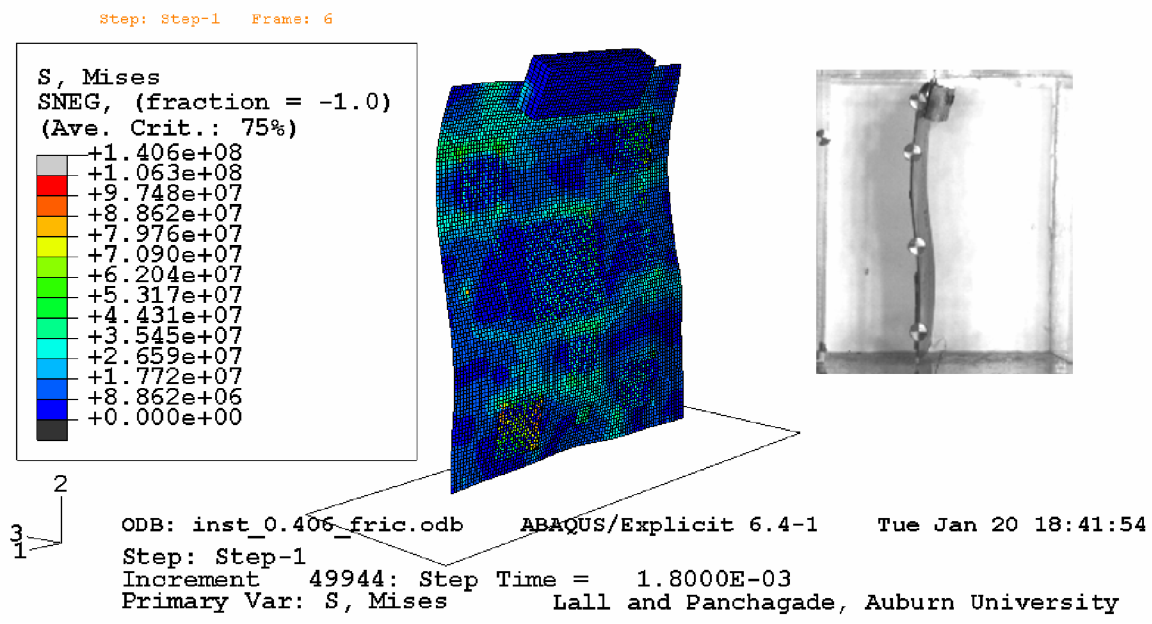


Time = 4.5 ms

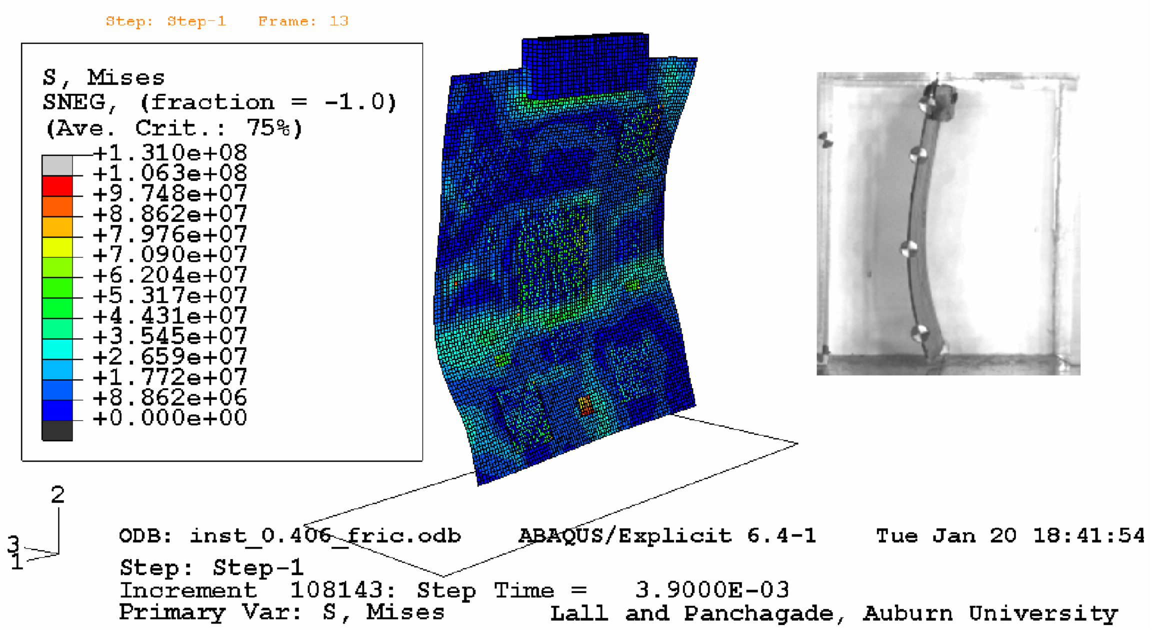


Time = 6 ms

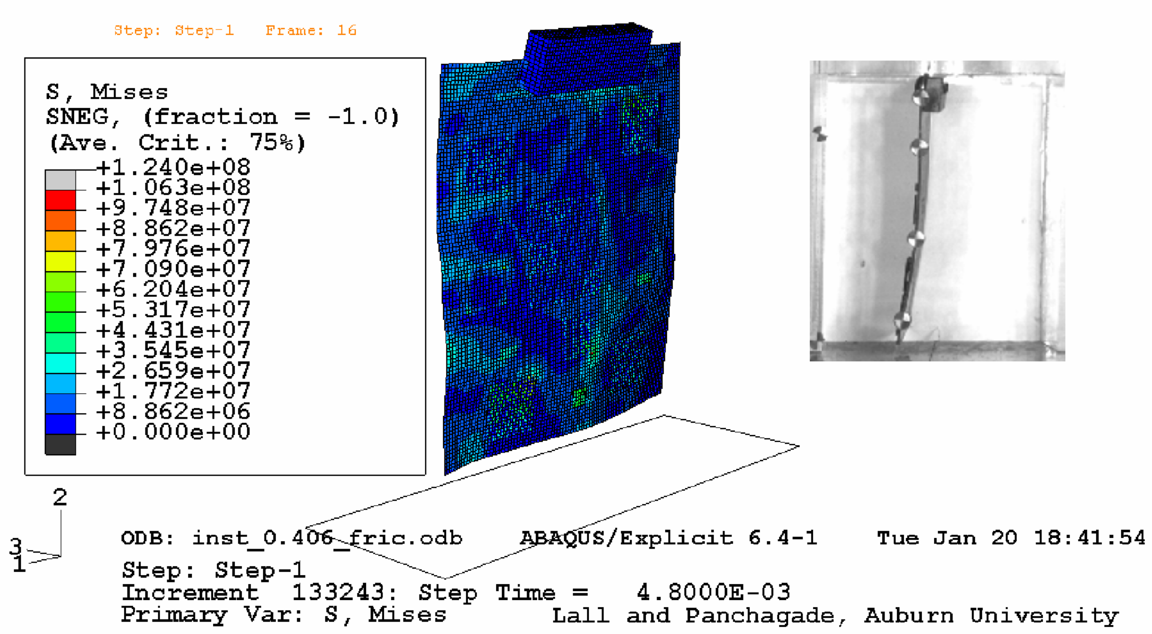
Figure 3.6: Correlation of Model Prediction versus Ultra-High-Speed Video for Test Board A.



Time = 1.8 ms



Time = 3.9 ms



Time = 4.8 ms

Figure 3.7: Correlation of Model Prediction v/s Ultra-High-Speed Video for Test Board B.

Table 3.6: Predicted Vs Experimental Strain (3 ft Drop).

Component	Simulation (εy)		Expt (εy)	Error (%)	
	Shell	Solid		Shell	Solid
8mm CSP	0.00186	0.0019	0.00257	27.6%	26.1%
15mm CSP	0.00182	0.00232	0.00263	30.7%	11.8%
16mm CSP	0.00211	0.00214	0.00275	1.4%	22.2%

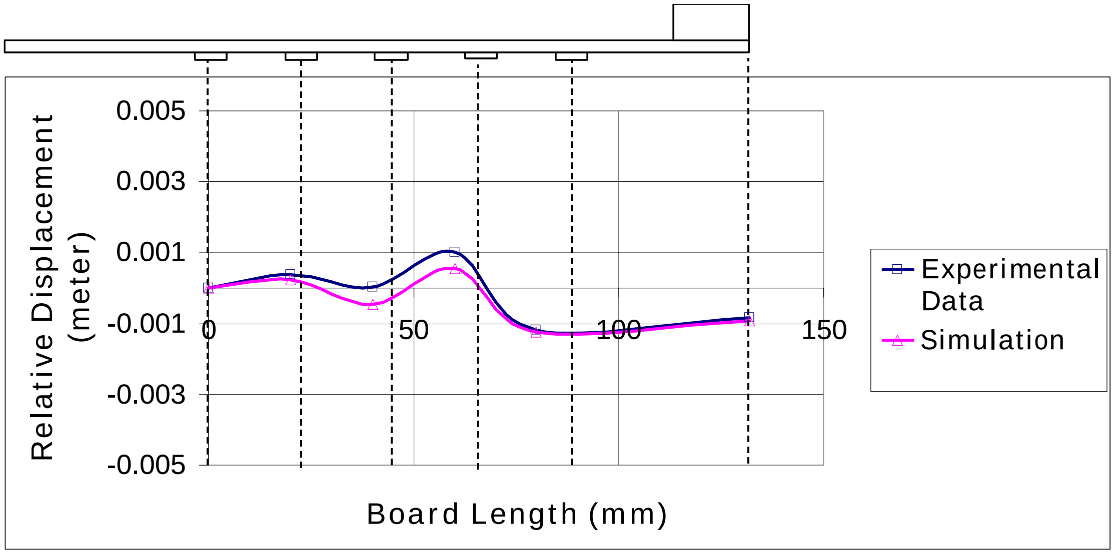


Figure 3.8: Relative Displacement of Test Board A versus Board Length at 2.4 ms.

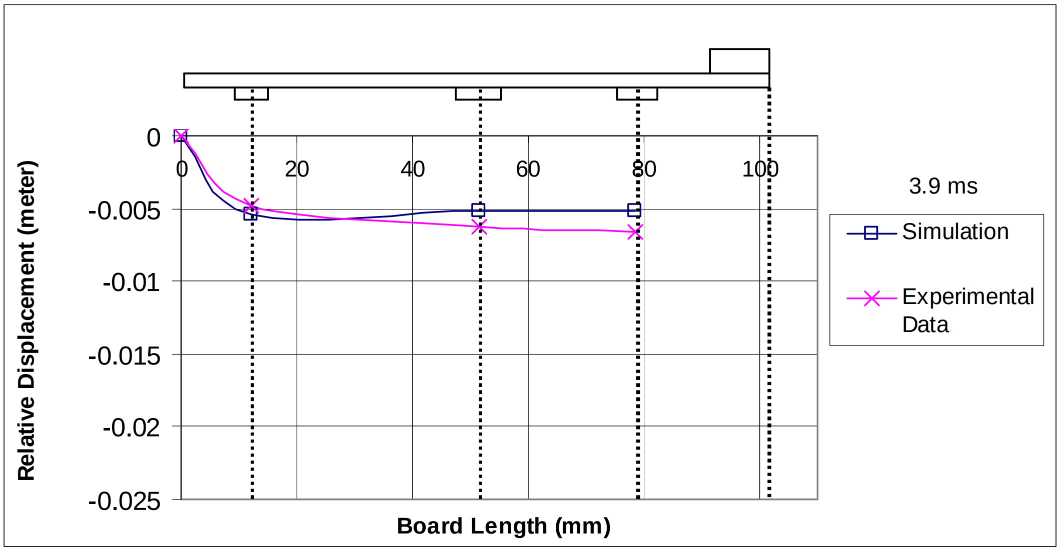


Figure 3.9: Relative Displacement of Test Board B versus Board Length at 1.3 ms.

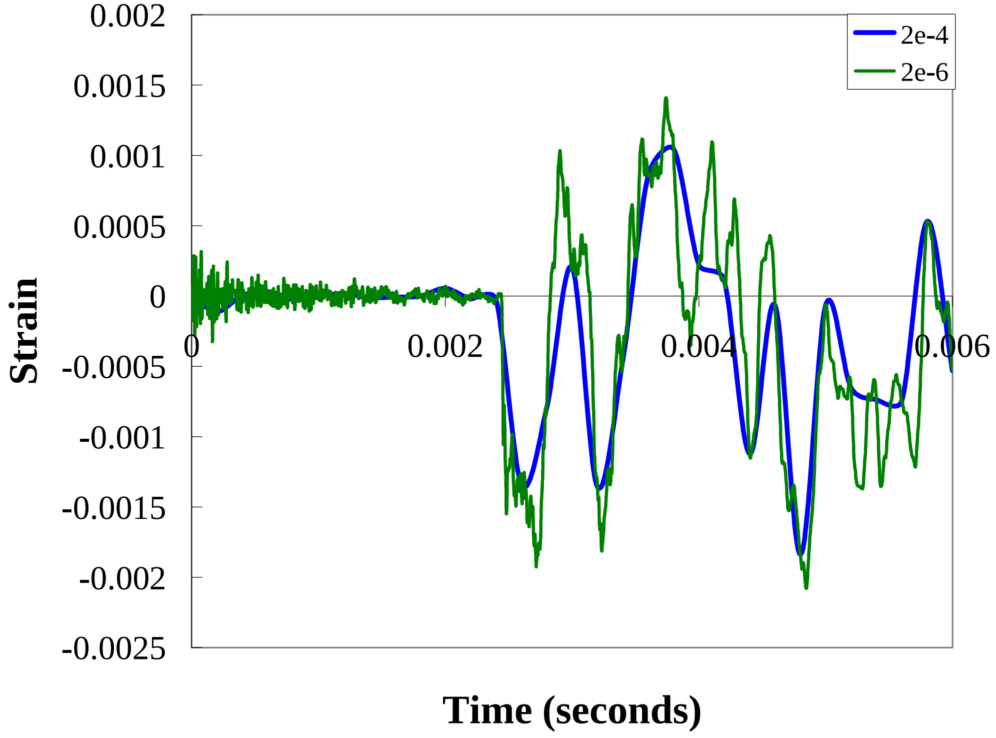


Figure 3.10: Aliasing of Output Data Based on Output Time Interval.

3.5 Summary and Conclusions

In this dissertation, a methodology for prediction of transient dynamic behavior of a board assembly during drop has been developed. It has been shown that a fairly accurate correlation of model prediction with experimental data on relative displacement and strain can be obtained using smeared property models. The methodology has been demonstrated for various component architectures including flex-substrate ball-grid arrays, plastic ball-grid arrays, thermally enhanced C2 ball-grid arrays and lead-frame chip-scale packages such as PQFN, variety of component I/O pitches ranging from 0.5 mm to 1 mm pitch, and variety of component I/O counts ranging from 132 I/O to 388 I/O.

Since smallest computational time step size in explicit dynamics is governed by the smallest element, there is limited freedom in inclusion of fine geometric features in the computational model. The smeared property models are advantageous, since they allow the adequate model accuracy while maintaining reasonable computational efficiency.

3.6 Discussion

Significant care needs to be exercised in studying transient-dynamic failure mechanisms such as drop in electronics. Several sources of error need to be carefully monitored before a robust correlation can be achieved.

A test set-up for producing repeatable orientation of drop is essential to study the transient dynamic response in any kind of detail. Portable electronic products dropped from 6ft may change orientation significantly during the drop. The final impact orientation may thus have no correlation with the initial angle at release from top of drop-height. Small changes in orientation may produce significant changes in the measured response of the product making it difficult to establish a valid baseline for development of finite-element models. Further, the most detrimental drop orientation may vary from product-to-product depending on design. Repeatability of drop orientation may help with the identification of most vulnerable drop configurations.

Significant error may be introduced because of aliasing of the experimental and computational data. Under-sampled experimental may miss peaks in strain or displacement. Further, error may be introduced because of under-sampled computational models.

Figure 3.10 shows the impact of aliasing in prediction of transient dynamic on-board strain. Model geometries need to be carefully developed. Individual material layers are often omitted, and detailed features of the metal traces are rarely incorporated. Smeared property model based on volume averaging may not capture structural degradation during successive drops produced due to possible progressive delamination in layers.

CHAPTER 4

MODELS FOR SHOCK AND VIBRATION SURVIVABILITY OF ELECTRONIC AND MEMS PACKAGING

4.1 Introduction

Electronic products may be subjected to drop and shock due to mishandling during transportation or during normal usage. Portable communication and computing products with fine-pitch ball-grid arrays, quad-flat no-lead packages are very susceptible to shock-related impact damage. Some of the products are repetitively subjected to shock in military operations such as artillery fire. Presently, product level assessment of drop and shock reliability relies heavily on experimental test methods. Product-level tests typically involve computing the number of drops-to-failure in addition to an assessment of the failure modes for the product. Factors such as drop height, mass of the product, impact orientation and the properties of the impacting surface affect the forces and the accelerations that are experienced by the product during impact. Design changes encompass an iterative process for improving the impact resistance of the electronic product.

Test methods for drop reliability can be broadly classified into constrained and unconstrained or free drop. Examples of constrained drop include the JEDEC test method. The JEDEC test standard [2003] is often used to evaluate and compare the drop performance of surface mount electronic components for handheld electronic product applications. This is a component level test. The primary intent is to standardize the test board and test methodology to provide a reproducible assessment of drop performance of surface mount electronics. However, the correlation between drop-performance in the test and that at the product-level is weak. Product-level failures are often influenced by housing design, in addition to drop-orientation, which may not always be perpendicular to the board surface. Previous researchers have investigated constrained drop techniques for edge-drop orientation of the test board and shown good repeatability. Testing methods for free drops have been proposed using high speed photography. However repeatability of these drops is difficult because of the phenomenon of ‘clattering’ in which one corner of the product touches the ground first and the other corner rebounds repeatedly.

Use of experimental approach to test out every possible design variation, and identify the one that gives the maximum design margin is often not feasible because of product development cycle time and cost constraints. There is a fundamental need for understanding and predicting the electronic failure mechanics in shock and drop-impact environment. To minimize development costs and maximize reliability performance, advanced analysis is a necessity during the design and development phase of a microelectronic package.

The analyst is typically interested in the cycles to failure that a package design configuration and cyclic loading condition will cause. This requires the utilization of a life prediction methodology in which a typical data provided can be translated into cycles to solder joint failure. Limited correlation has been achieved with acceleration, velocity and displacement time histories. Life prediction of electronics in shock-impact has been scarce. Use of the peak von-mises stresses and normal stresses with power-law relationships to predict drops to failure has been investigated.

Strain behavior of electronic assemblies is not elastic and the large transient deformation is often not accurately represented by the small strain theory. In addition, the final or the peak strain does not capture the final strain or damage state of the assembly. The rate-of-change of deformation and the latent damage in previous drops impacts the susceptibility to failure during successive drops.

Dynamic responses at board level at product level have been measured by previous researchers. Failure may not happen in the first drop, and damage may be cumulative. There is need for techniques and damage proxies which enable the determination of failure-envelopes and cumulative damage during overstress and repetitive loading for various packaging architectures. Presently, investigation of dynamic responses such as deflection, velocities, strains etc during the transient event gives us an insight about the failure mode and failure mechanism of solder joints. However, there are experimental limitations of measuring field-quantities and their derivatives at the board-solder joint interface, primarily because of the small size of interconnect in fine-pitch ball-grid array packages.

There is need for damage proxies to interrogate state of the material and determine cumulative damage at any instant of time. In this dissertation, a methodology has been developed to determine the damage progression versus number of drops by studying the transient strain history of the test boards. The damage proxies developed in this dissertation can be used on strain response from simulations or from experimental data in controlled drop or shock tests.

Damage proxies developed provide objective and quantitative failure definitions that allow for variation in orientation, component location, in addition to load history. Damage proxies also allow for determination of failure envelopes for component deployment in various product level applications.

4.2 Transient Damage and Resistance Measurement

Many sensors exhibit a change electrical resistance in response to the quantity that they are trying to measure. Some examples include force sensing resistors which decrease their resistance when a force is applied, thermistors which change resistance as a function of the temperature and carbon microphones which alter their resistance in response to changing acoustical pressure. In all these cases, one must be able to convert the resistance of the device into a usable voltage which can be read by the analog to digital converters. Following are some circuits which perform these measurements.

The voltage that appears across the sensor (or the reference resistor) is then buffered before being sent to the ADC. The output voltage is given by: [McLaren 1984]

$$V_{\text{out}} = \frac{R_m}{R_m + R_f} = \frac{1}{1 + \frac{R_f}{R_m}} \tag{4.1}$$

There are two ways to convert resistance of a sensor to a voltage. The first and simplest way is to apply a voltage to a resistor divider network composed of a reference resistor and the sensor as shown in Figure 4.1.

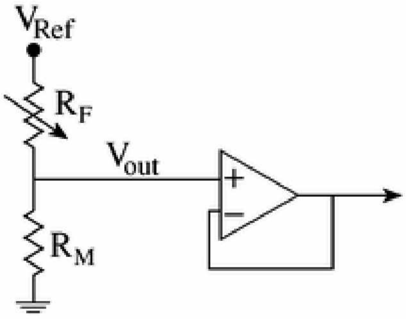
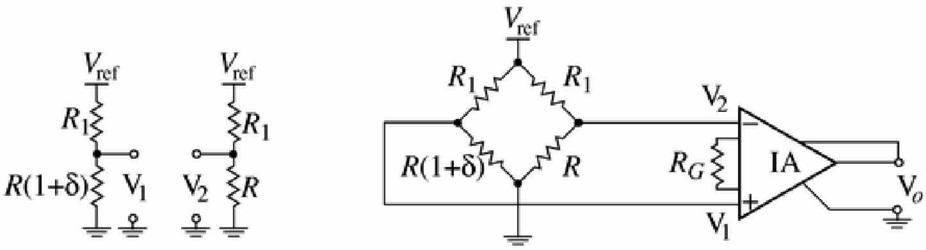


Figure 4.1: Resistance to Voltage Converter

The problem with this method of measuring resistance is that the amplifier is amplifying the entire voltage measured across the sensor. It would be much better to amplify only the change in the voltage due to a change in the resistance of the sensor. This can be accomplished using a bridge as shown in Figure 4.2.

$$V_o = A\frac{R}{R_1 + R} V_{ref} \frac{\delta}{1 + (R/R_1)(1 + \delta)}$$



(4.2)

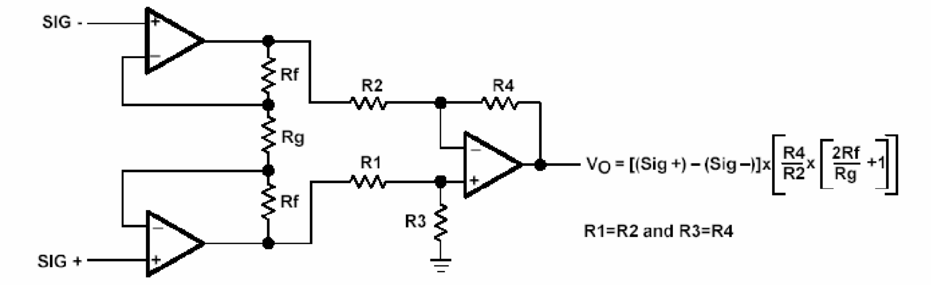
Figure 4.2: A Resistance Bridge Connected to an Instrumentation Amplifier (IA)

If R_1 is set equal to R, then the approximate output of this circuit is: $V_{out} = \frac{A}{4}V_{ref}\delta$ Where A is the gain of the IA and δ is the change in the resistance of the sensor corresponding to some physical action.

Notice in this equation that the gain can be set quite high because only the change in voltage caused by a change in the sensor resistance is being amplified.

4.2.1 Three Op Amp Instrumentation Amplifiers

The three op amp instrumentation amplifier, or in-amp, uses three op amps. The circuit, shown in Figure 4.3, has high input impedance, and source impedance does not play a role in calculation of gain. To achieve better CMRR performance, use a resistor pack for resistors R1–R4 and RF. Set the gain using Rg. [McLaren 1984]



(4.3)

Figure 4.3: Three Op Amp Instrumentation Amplifier

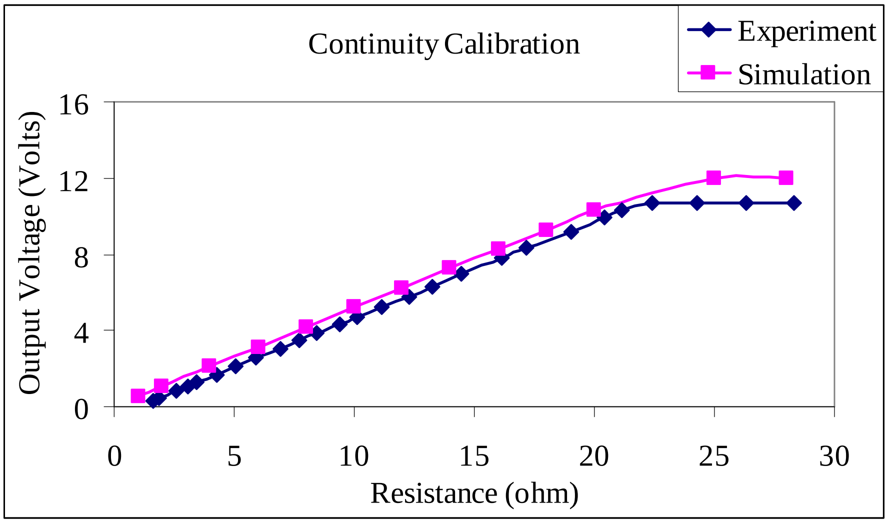


Figure 4.4: Comparison of simulation and test results

The error between simulation and test results (Figure 4.4) comes from two sources. First, voltage input of amplifier in simulation is V+=12v and V-= -12v, While the real voltage supply in test is not exactly 12v, V+=11.93v and V-= -11.05v. Secondly, the resistance of real resistors is not exactly the same as that in simulation (R=500 ohm).

4.3 Test Vehicle

Three test boards have been used to study the reliability of chip-scale packages and ball-grid arrays. Test board A has 10 mm ball-grid array, 0.8 mm pitch, 100 I/O. It has 10 components on one side of the board (Figure 4.5). Test board B includes 8mm flex-substrate chip scale packages, 0.5 mm pitch, 132 I/O (Table 4.1). The number of components varies from 6 to 10 on some of the boards. All the components are on one side of the board. For the 8 mm CSP, conventional eutectic solder, 63Sn/37Pb and lead-free solder balls 95.5Sn4.0Ag0.5Cu have been studied. Test boards A and B are made of FR-4. These test boards were based on standard PCB technology with no build-up or HDI layers. Test Board A and B was 2.95" by 7.24" by 0.042" thick.

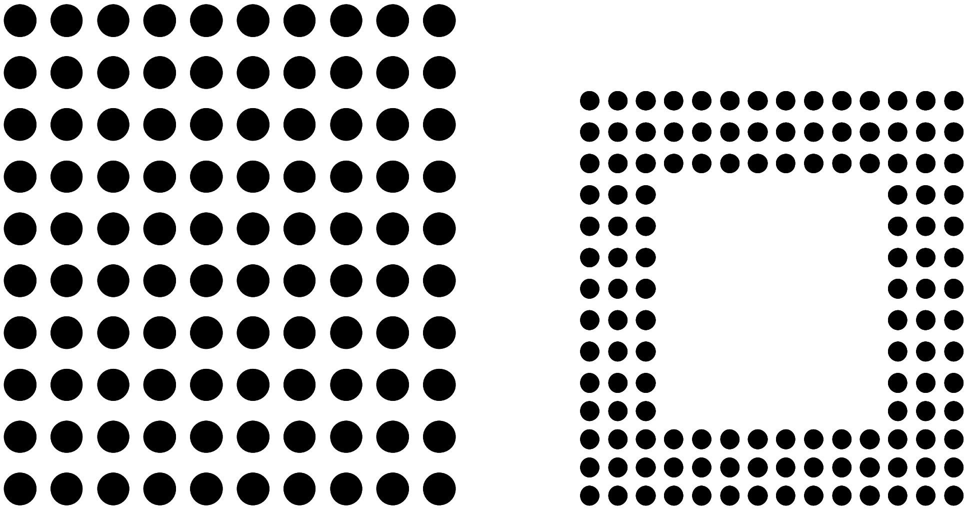


Figure 4.5: Interconnect array configuration for 95.5Sn4.0Ag0.5Cu and 63Sn37Pb Test Vehicles.

Table 4.1: Test Vehicles

	10mm 63Sn37Pb	8mm 62Sn36Pb2Ag	8mm 95.5Sn4.0Ag 0.5Cu
Ball Count	100	132	132
Ball Pitch	0.8 mm	0.5 mm	0.5 mm
Die Size	5 x 5	3.98 x 3.98	3.98 x 3.98
Substrate Thickness	0.5 mm	0.1 mm	0.1 mm
Substrate Pad Dia.	0.3 mm	0.28 mm	0.28 mm
Substrate Pad Type	SMD	Thru-Flex	Thru-Flex
Ball Dia.	0.46 mm	0.3 mm	0.3 mm

4.4 Damage Detection

Figure 4.6 shows the strain history during successive drops (drop 1 – drop 4) for a 8 mm 95.5Sn4Ag0.5Cu ball-grid array package. Failure in the device has been identified as an increase in voltage drop. Different locations on the test board exhibit different strain histories during same drop and different number of drops to failure. However, the strain histories are very consistent and repeatable at the same component location across various test boards.

4.5 Wavelet Analysis

Wavelets have been used in several areas including data and image processing, geophysics, power signal studies, meteorological studies, speech recognition, medicine, and motor vibration. However, the application of wavelets to analysis of transient-response of electronics under shock and vibration is new. In this dissertation, wavelets and wavelet transforms have been used to analyze transient signals acquired during drop-impact of printed circuit board assemblies (Figure 4.7).

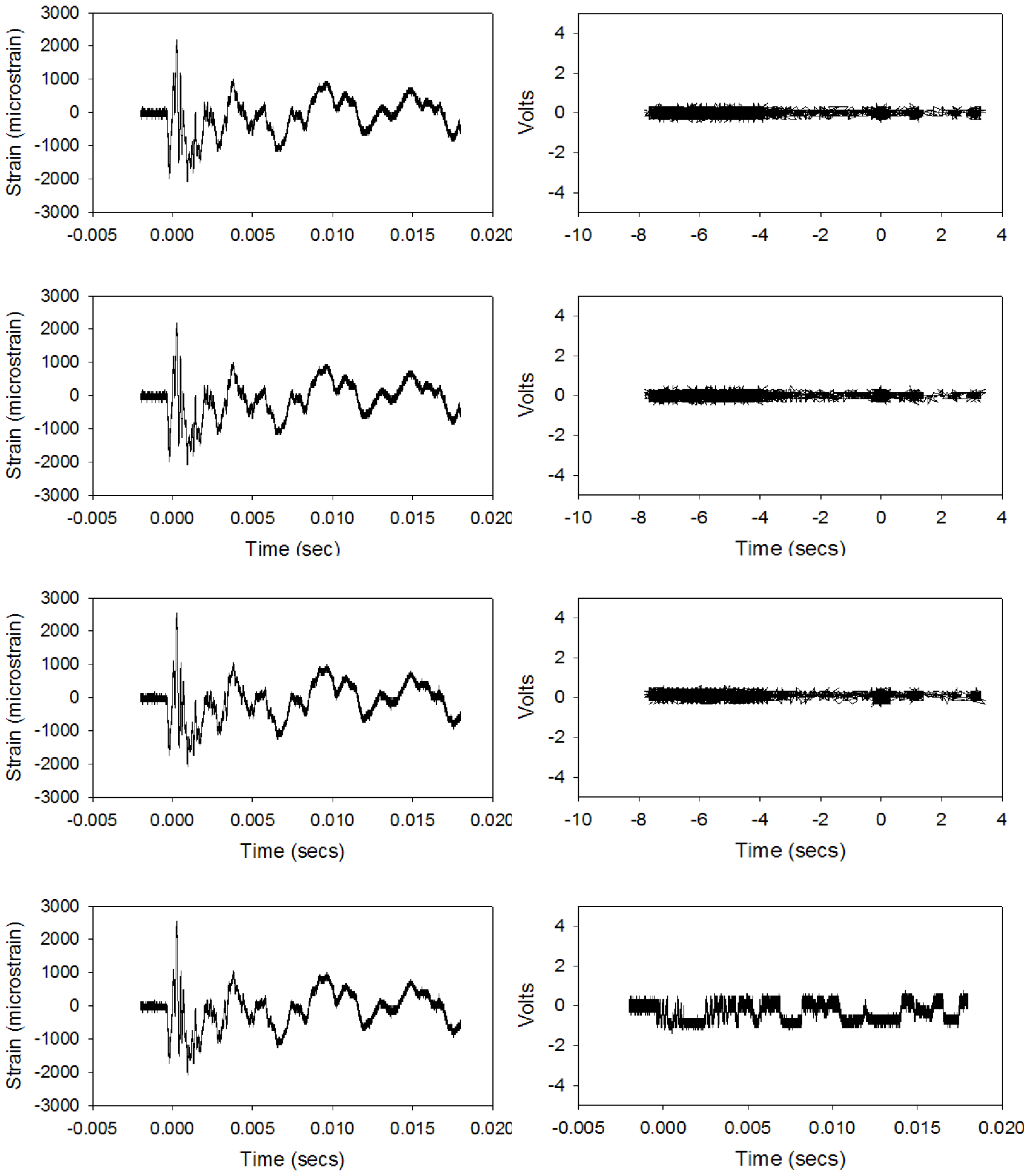


Figure 4.6: Strain and continuity transient history in successive drops, from 6ft for the 8mm, 95.5Sn4Ag0.5Cu ball-grid array. Note the solder joint failure in drop 4.

Wavelets based time-frequency analysis is specifically useful to analyze non-stationary signals. A time-frequency representation describes simultaneously when a signal component occurs and how its frequency spectrum develops with time, so as to extract the transients or sudden spikes in the signal. Wavelet transform is more suitable to determine the frequency spectrum of the transient strain, acceleration or displacement signals as the Fourier transform extracts frequency information for the complete duration of the stress signal, using sine and cosine functions that are uniform in time. The Fourier Transform does not contain any time dependence of the signal and therefore cannot provide any local information regarding time evolution of its spectral characteristics. Transient impulses often occur as discontinuities in the signal. Representation of the local characteristics of signal in Fourier Transform is very inefficient and requires large number of Fourier Components.

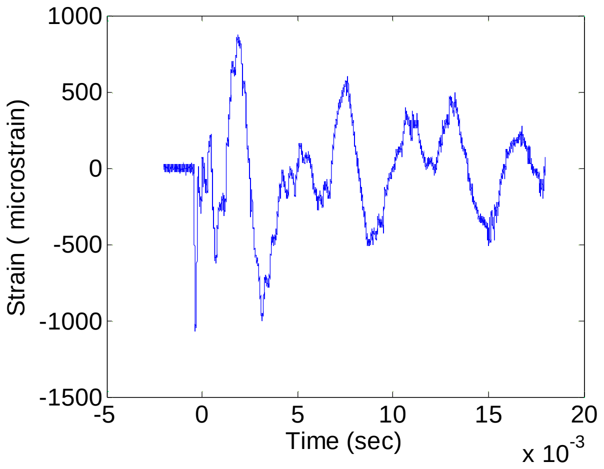


Figure 4.7: Transient Strain During Drop-Impact of Printed Circuit Assembly From 6ft.

One candidate for extracting the local frequency information from a transient strain signal could have been the Windowed Fourier Transform. However, in a

Windowed-Fourier Transform, a time series is examined under a fixed time-frequency window, i.e. the resolution or interval is constant in both time and frequency domains. In a transient dynamics, a wide range of frequencies are involved and a fixed time window of the Windowed-Fourier Transform tends to have a large number of high-frequency cycles and a few low-frequency cycles or parts of cycles. This causes over-representation of the high-frequency components and an under-representation of the low-frequency components. Therefore, different resolutions are required to analyze a variety of signal components of different duration. The accuracy of extracting frequency information is limited by the length of the window relative to the duration of the singularity in the signal.

The use of wavelet transforms in this thesis enables the examining of the transient signal, at different time windows and frequency bands, i.e. at different time resolutions and frequency resolutions, by controlling translation and dilation of wavelets and achieve optimal resolution with the least number of base functions. The size of the time window is controlled by the translation or positioning of the wavelet while the width of the frequency band is controlled by the dilations or scaling of the wavelet. In this case, wavelets therefore enable higher frequency-resolution and lower time-resolution in low frequency part, and at the same time enable lower frequency-resolution and higher time resolution in high frequency part. The wavelet transform is defined by

$$Wf(u,s) = \langle f, \psi_{u,s} \rangle = \frac{1}{\sqrt{s}} \int_{-\infty}^{+\infty} f(t)\, \psi^{*}\left(\frac{t-u}{s}\right) dt \tag{4.4}$$

where the base atom ψ^{*} is the complex conjugate of the wavelet function which is a zero average function, centered around zero with a finite energy. The function f(t) is decomposed into a set of basis functions called the wavelets with the variables s and u, representing the scale and translation factors respectively.

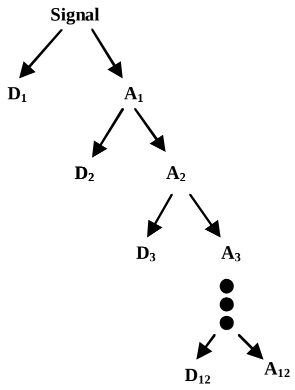


Figure 4.8: Twelve decompositions using the D_{10} Wavelet.

The transform has been used to analyze transient strains signals at different frequency bands with different resolutions by decomposing the transient signal into a coarse approximation and detail information (Figure 4.8). The signal is decimated into different frequency bands by successively filtering the time domain signal using low-pass and high-pass filters. The original stress signal is first passed through a half-band highpass filter g[n] and a lowpass filter h[n]. After the filtering, half of the samples are eliminated according to the Nyquist's rule, since the signal now has a highest frequency of p/2 radians instead of p. The signal is therefore sub-sampled by 2, simply by discarding every other sample. This constitutes one level of decomposition and can mathematically be expressed as follows:

$$\begin{aligned} y_{high}[k] &= \sum_{n} \mathrm{signal}[n] \cdot g[2k-n] \\ y_{low}[k] &= \sum_{n} \mathrm{signal}[n] \cdot h[2k-n] \end{aligned} \tag{4.5}$$

where $y_{high}[k]$ and $y_{low}[k]$ are the outputs of the highpass and lowpass filters, respectively, after sub-sampling by 2. However, the number of average number of data points out of the filter bank is the same as the number input, because the number is doubled by having two filters. Thus, no information is lost in the process and it is possible to completely recover the original signal. Aliasing occurring in one filter bank can be completely undone by using signal from the second bank. Further, the time resolution after the decomposition halves as the sub-sampling occurs. However this sub-sampling doubles the frequency resolution, as after decomposition the frequency band of the signal spans half the previous frequency band, effectively reducing the uncertainty in the frequency by half. At every level, the filtering and sub-sampling will result in half the number of samples (and hence half the time resolution) and half the frequency band spanned (and hence doubles the frequency resolution).The frequencies that are most prominent in the original signal will appear as high amplitudes in that region of the Wavelet transform signal that includes those particular frequencies. The time localization will have a resolution that depends on which level they appear.

4.5.1 Daubechies Wavelet

Daubechies wavelet has been chosen for analysis of transient dynamic signals mainly based on resemblance of the wavelet with the true signal. The Daubechies-wavelets are defined two functions, i.e. the scaling function $\phi(x)$, and the wavelet function $\psi(x)$. The Daubechies wavelet algorithm uses overlapping windows, so the high frequency spectrum reflects all changes in the time series. Daubechies wavelet shifts its window by two elements at each step.

However, the average and difference are calculated over four elements, so there are no "holes" unlike other wavelet transforms such as Haar transform, which use a window which is two elements wide. With a two element wide window, if a big change takes place from an even value to an odd value, the change will not be reflected in the high frequency coefficients.

The transient strain signal has been transformed at Level 12 using a Daubechies transform of order 10 i.e. a D_{10} transform. We have used the D_{10} transform at level 12 and filtered the signal using low and high pass filters repeatedly, to obtain 12 approximations and 12 details of the signal. The scaling function is the solution of the dilation equation,

$$\phi(t) = \sqrt{2}\sum_{u=0}^{L-1} h(u)\, \phi(2t-u) \tag{4.6}$$

where h(u) are a sequence of real or complex numbers called the scaling function coefficients, $\sqrt{2}$ represents the norm of scaling function with a scale of two, $\phi(t)$ is normalized $\int_{-\infty}^{\infty}\phi(t)dt = 1$. The wavelet $\psi(t)$ is defined in terms of the scaling function,

$$\psi(t) = \sqrt{2}\sum_{u=0}^{L-1} g(u)\, \phi(2t-u) \tag{4.7}$$

where the coefficients g(u) defines the scaling function. Building on the orthonormal basis from $\phi(t)$ and $\psi(t)$ by dilating and translating, the following functions are obtained,

$$\phi_u^s(t) = 2^{\frac{s}{2}}\phi(2^s t-u) \tag{4.8}$$

$$\psi_u^s(t) = 2^{\frac{s}{2}}\psi(2^s t - u)\,, \tag{4.9}$$

where s is the dilation parameter and u is the translation parameter.

The strain signal obtained from the impact drop test has a sampling time of 0.2 to 0.4 μs, i.e., a sampling frequency of 2.5 to 5 MHz. For the 2.5 MHz test data, in order to avoid aliasing during our analysis, we perform our transforms and calculations using the Nyquist frequency, which is half of the sampling frequency, i.e. 1.25 MHz. The Low-Pass and High-Pass filters used during the transform have a frequency response shown in Figure 4.9 and Figure 4.10. The approximations and details obtained from 12-level decomposition have been shown in Figure 4.11.

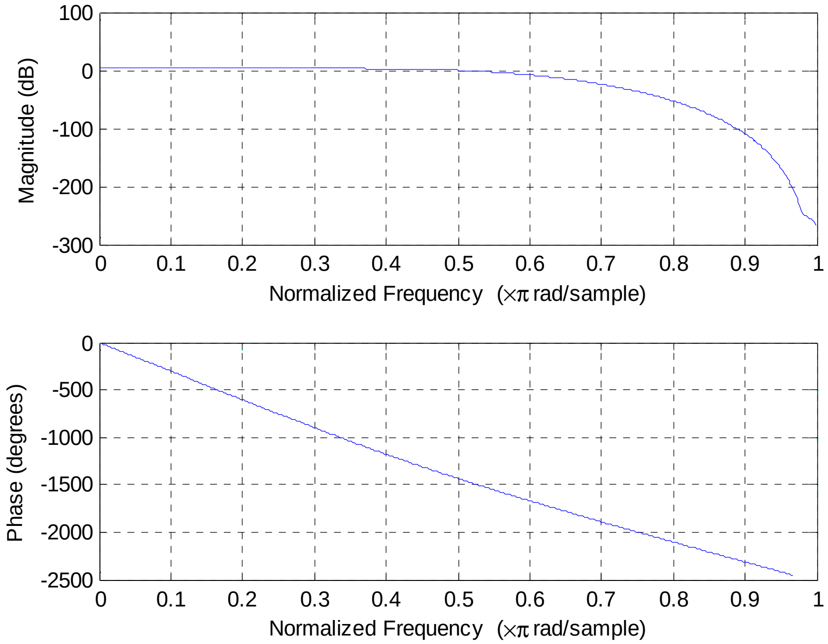


Figure 4.9: Frequency Response of the Low-Pass Filter.

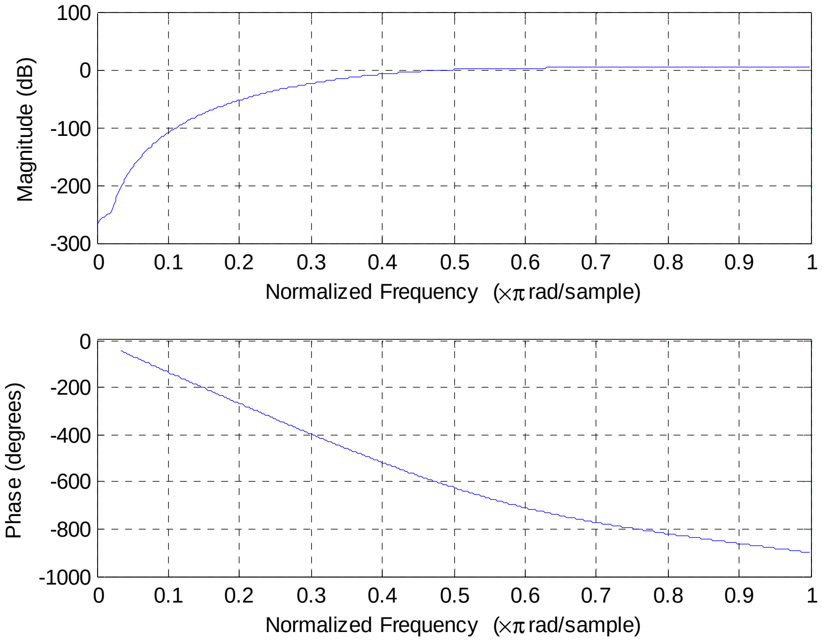


Figure 4.10: Frequency Response of High-Pass Filter.

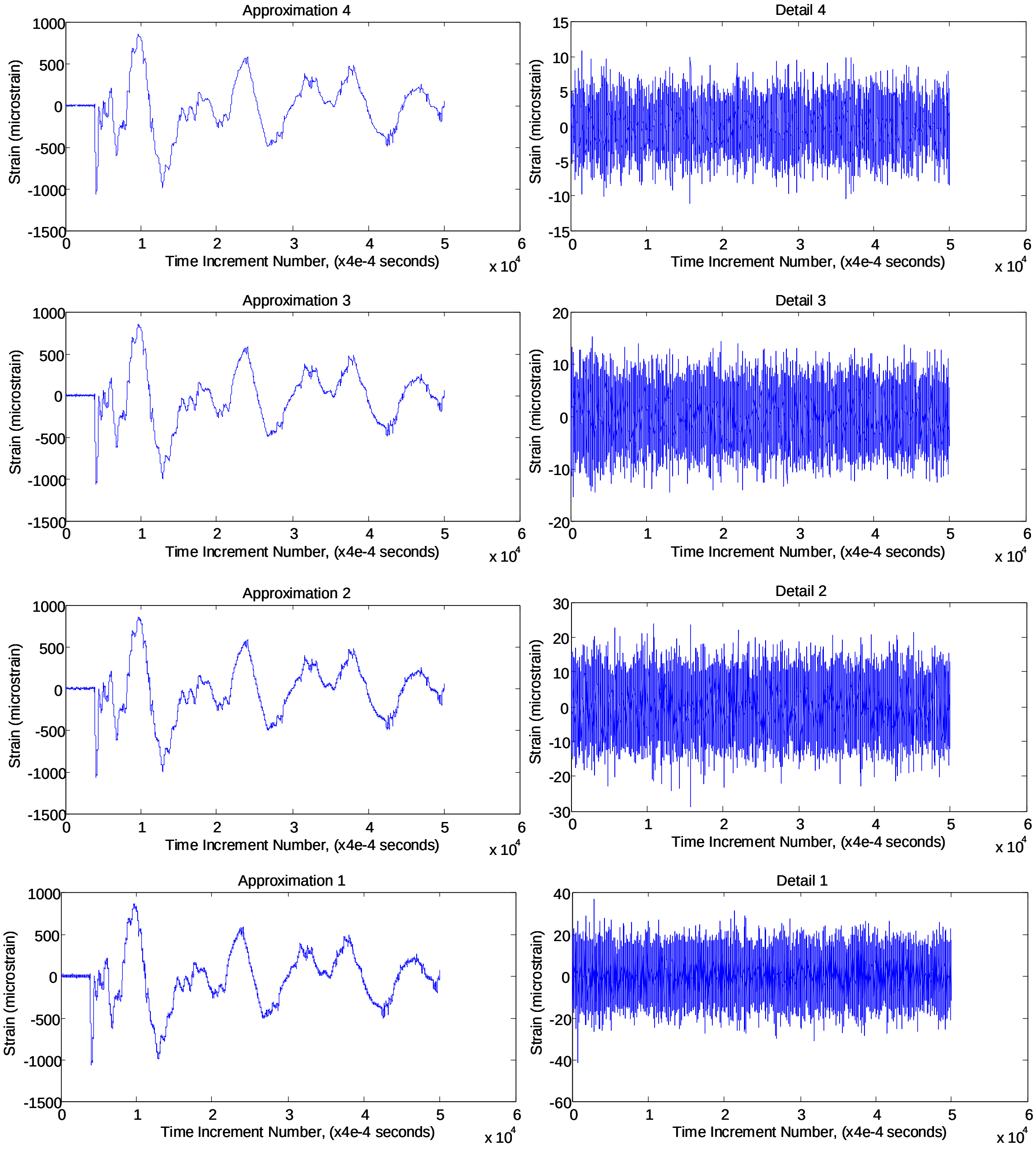


Figure 4.11: Approximation and Details 1-4 for a 12-Level Decomposition for Transient Strain Signal During Drop, Based on Daubechies 10 Wavelet.

4.6 Damage Prediction Models

In transient-shock and drop, the loads vary in both amplitude and frequency. Electronic structures very rarely experience constant amplitude loading. To analyze the structures in operating conditions strain measurements and relative displacement measurements have at specific points have been analyzed using Daubechies, D_{10} wavelet with 12-level decomposition.

For cycle-counting analysis the second approximation, A_2 has been used as input to the rainflow algorithms. In rainflow analysis, the strain time history data is drawn with time axis vertical with increasing time downwards. Rainflow cycles are then defined analogous to rain falling down the roof. Detailed rules for cycle counting are described in [ASME 1997, Bannantine 1990, and Downing 1982]. A flow of rain is begun at each strain reversal in the history and is allowed to continue to flow unless, (a) the rain began at a local maximum point (peak) and falls opposite a local maximum point greater than that from which it came. (b) The rain began at a local minimum point (valley) and falls opposite a local minimum point greater (in magnitude) than that from which it came. (c) it encounters a previous rainflow.

The transient-dynamic data in time-domain has been reduced into histograms of load cycle amplitudes and number of cycles. Number of cycles is calculated using cycle counting algorithm for the transient-strain history. Figure 4.12 is the histogram for one of the drops to failure showing the number of cycles for specific strain amplitude during the transient signal. The transient strain signal has a high number of very small strain amplitude cycles and very few number of large strain amplitude cycles.

Damage from both repeatable and non-repeatable drops has been analyzed. For repeatable drops, the strain histograms are very similar. Damage has been computed for each component, till failure.

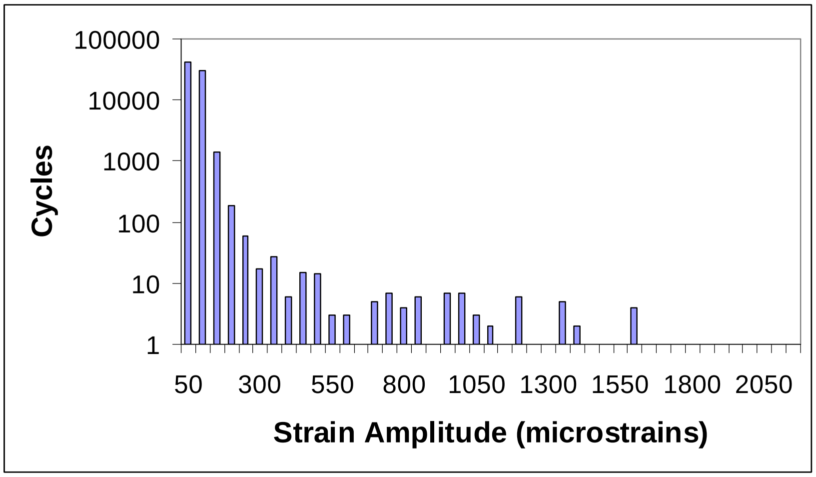


Figure 4.12: Cycles versus Strain Amplitude for Transient Strain History from Rainflow Algorithm. Histogram is for 95.5Sn4Ag0.5Cu Solder Joint Failures during the Drop for 132 I/O, 8 mm Ball Grid Array.

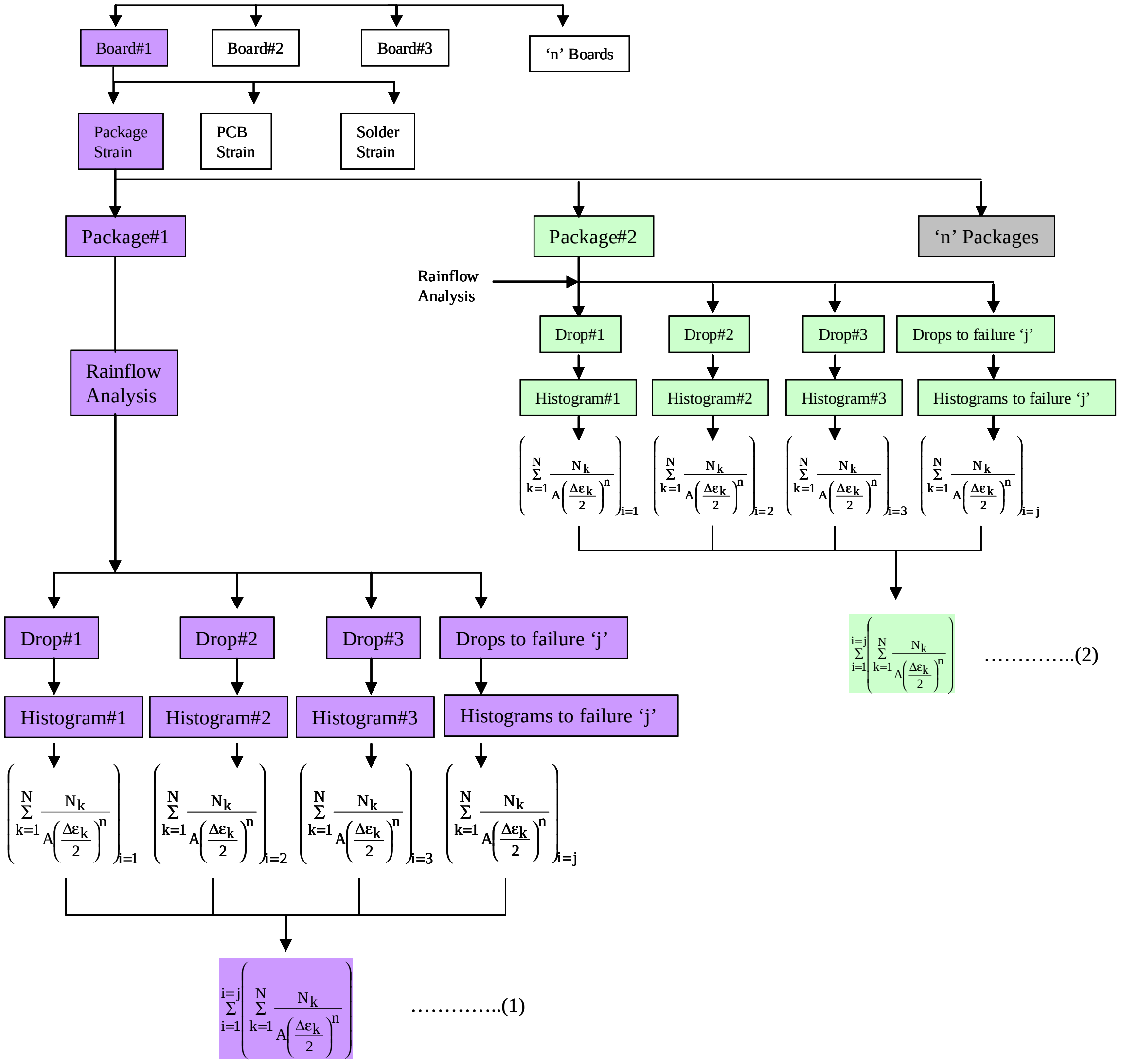


Figure 4.13: Flow Chart for Computing ‘A’ and ‘n’

Equation (1), (2),….. (n) in Figure 4.13 are solved simultaneously to calculate the unknowns ‘A’ and ‘n’.

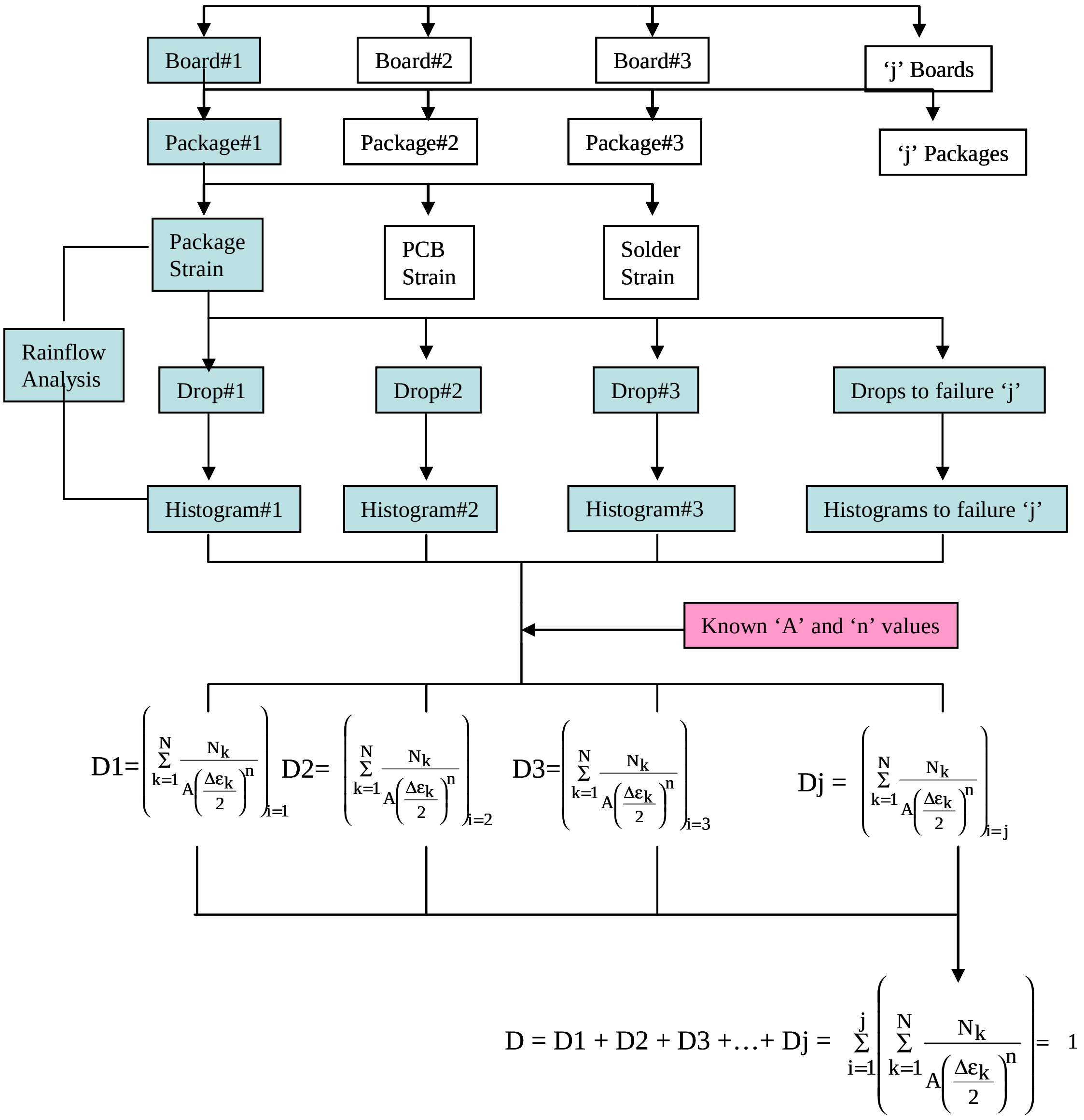


Figure 4.14 : Flow Chart for Damage Superposition

Figure 4.14 shows the flow chart for calculating the damage at each drop. The damage is summed for each drop and assumed to be equal to "1" at failure. Figure 4.15 shows the example of relative damage progression when the package fails at fifth drop.

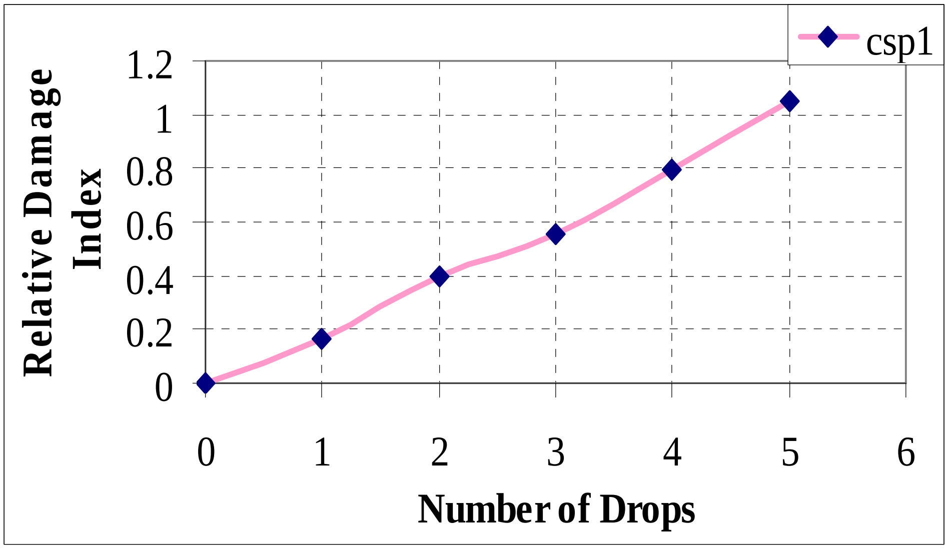


Figure 4.15: Relative Damage Index for Representative Drops to failure at location CSP1

All information about the sequence of the individual strain variation is lost during counting. The resulting cumulative frequency distribution histogram, gives the overall number of load cycles for each load amplitude. A relative damage index has been defined such that the damage magnitude at failure is “1”. Linear superposition of damage has been assumed in this study. The equation can be re-written as follows based on the assumed logarithmic relationship between strain and number of cycles (Coffin-Manson Relationship),

$$\sum_{k=1}^{M} \frac{D_k}{D} = 1 \tag{4.10a}$$

$$\sum_{k=1}^{M} \frac{N_k}{A\left(\frac{\Delta\varepsilon_k}{2}\right)^n} = 1 \tag{4.10b}$$

where, “k” is the bin-index for the histogram, $\Delta\varepsilon/2$ is the printed circuit board strain amplitude, M is the total number of bins in the histogram, N is the number of cycles subjected on the sample in the k^{th} histogram bin during all the drops until-failure of the device, and D is the damage index. Data from data sets has been solved as follows,

$$\left(\sum_{k=1}^{N}\frac{N_k}{A\left(\frac{\Delta\varepsilon_k}{2}\right)^n}\right)_i = 1, \quad \left(\sum_{k=1}^{N}\frac{N_k}{A\left(\frac{\Delta\varepsilon_k}{2}\right)^n}\right)_{i+1} = 1 \qquad (4.11a, b)$$

where the index “i” indicates the drop number. Each data-set includes test-vehicles which have been dropped-to-failure; therefore the cumulative relative damage index is 1. The load histories have been varied by varying the angle of impact by a small magnitude. Subtracting the two equations, we get,

$$\left(\sum_{k=1}^{N}\frac{N_k}{\left(\frac{\Delta\varepsilon_k}{2}\right)^n}\right)_i - \left(\sum_{k=1}^{N}\frac{N_k}{\left(\frac{\Delta\varepsilon_k}{2}\right)^n}\right)_{i+1} = 0 \qquad (4.12)$$

Average values of the exponent, “n” and coefficient “A’ has been computed over the complete data-set. Since, the values have been computed for board strain, they are specific to the test structure analyzed. The relative damage in any particular drop is computed based on total damage at failure (Figure 4.16). The advantage of the proposed approach is that it can be used to calculate damage in the test structures of interest, instead of an idealized test specimen.

The test samples were cross-sectioned after failure, and the test data was sorted based on failure modes. Solder joint failure were pre-dominant in the test samples examined in this study, however other failures modes including copper-trace cracking, and printed-circuit board resin cracks were also encountered. It is anticipated that the cumulative damage will be different for different failure modes. In this dissertation, only samples with solder joint failures have been examined.

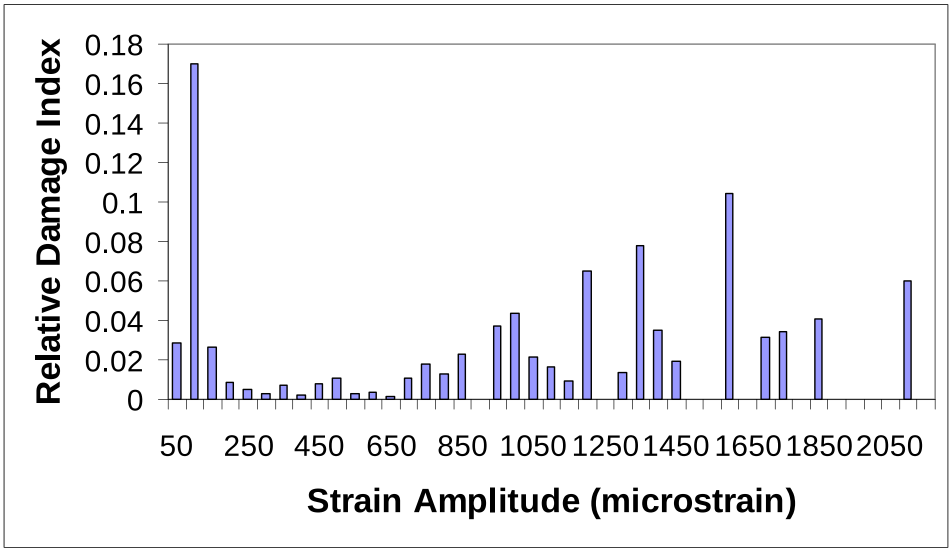


Figure 4.16: Damage for Various Strain Amplitudes during Transient Strain History of 8 mm, 95.5Sn4Ag0.5Cu, 132 I/O Ball Grid Array during impact.

It is observed that a significant amount of damage occurs at the very high strain amplitudes (Figure 4.16), even though the number of cycles is very low. Strain amplitudes less than 250 microstrains account for damage in the neighborhood of 20% even though they account for more than 90% of the total cycles in the transient strain history. Similar data has been acquired on all three packaging architectures including, 8mm, 0.5 mm pitch, 132 I/O ball-grid arrays with both 95.5Sn4Ag0.5Cu and 63Sn37Pb solder interconnects and 10 mm, 0.8 mm pitch, 100 I/O ball-grid arrays with 63Sn37Pb solder interconnects.

4.7 Failure Envelope and Model Correlation

The relative damage index has been used to predict the number of drops to failure for the 8 mm Ball Grid Array, 95.5Sn4Ag0.5Cu, 132 I/O. The location for the predictions is different from location at which the experimental data was acquired. Therefore, the transient-strain history and the damage progression is also different. Model prediction indicates 5 drops-to-failure and correlates well with the experimental data, which indicates that the ball-grid arrays at the location of measured transient strain failed after 6 drops. The present data-set is one has been chosen for correlation, because it is a representative average of the damage progression at this location. Number of drops-to-failure at this location ranged between 5-7 drops. The correlation is for a non-repeatable drop, indicated by the non-uniform damage progression in experimental data-set (Figure 4.17).

Model predictions and correlation with experimental data for the 63Sn37Pb, 8mm BGA is shown in Figure 4.18. The model predictions indicate failure after 9 drops-to-failure at the location of the transient strain trace. Representative average experimental data for the failure location exhibits failure after 10 drops.

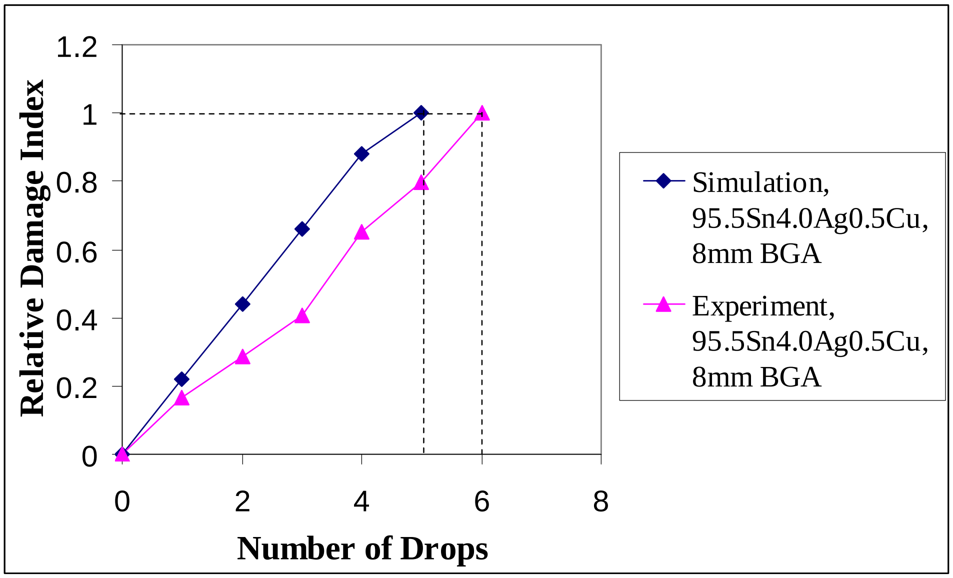


Figure 4.17: Correlation of Damage Progression and Number of Drops to Failure Between Experiment and Simulation for the 8 mm, 95.5Sn4Ag0.5Cu, 132 I/O Ball Grid Array.

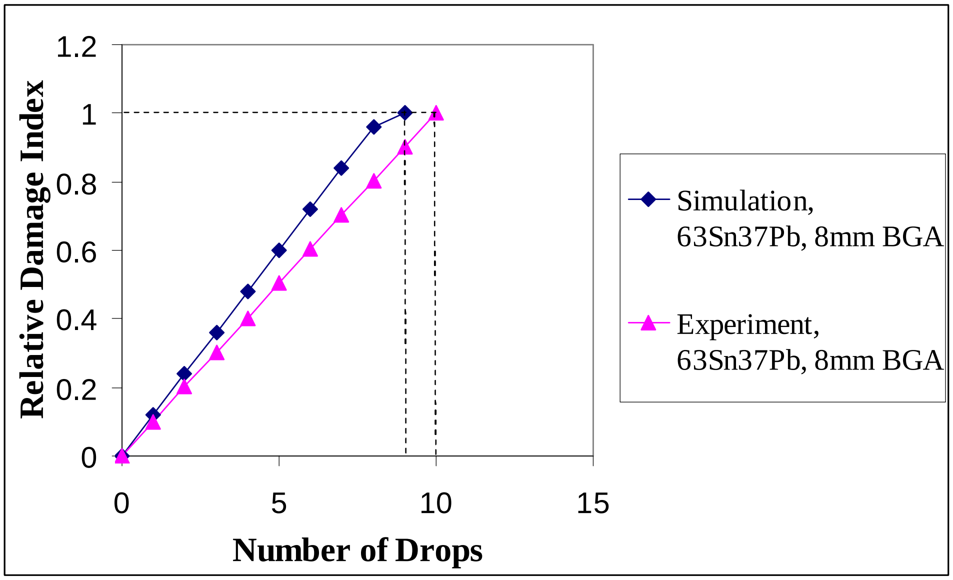


Figure 4.18: Correlation of Damage Progression and Number of Drops to Failure between Experiment and Simulation for the 8 mm, 63Sn37Pb, 132 I/O Ball Grid Array.

The relative damage index approach outlined in this dissertation provides a method to define the failure envelope for packaging architectures. The solder interconnect strain is not as easily measurable as board strain. The proposed methodology enables evaluation of the failure envelope in the application of interest and for the packaging architecture in question. Damage during the life of the product should not exceed “1” for the design to have good survivability in drop and shock applications. The constants used for damage progression are specific to the package architecture and boundary conditions. The proposed methodology is amenable to implementation not just at board-level but also at system-level.

4.8 Failure Analysis and Mechanisms

All the test specimen were cross-sectioned to determine the failure modes. Observed failure modes include, solder interconnect failures at the package and the board interface, copper-trace cracking, and printed circuit board resin cracks under the copper pads. In order to develop a consistent failure envelope on a failure mode specific basis, the failure modes have been sorted. The observed failures were predominantly in the solder interconnects for both the leaded and the lead-free packaging architectures (Figure 4.21, Figure 4.22,). The 95.5Sn4.0Ag0.5Cu solder interconnects were observed to have lower shock and vibration survivability compared to 63Sn37Pb interconnects (Figure 4.19, Figure 4.20). Both Weibull distributions exhibit similar slopes, in the neighborhood of β = 6-7 indicating the consistency in failure mechanism and mode.

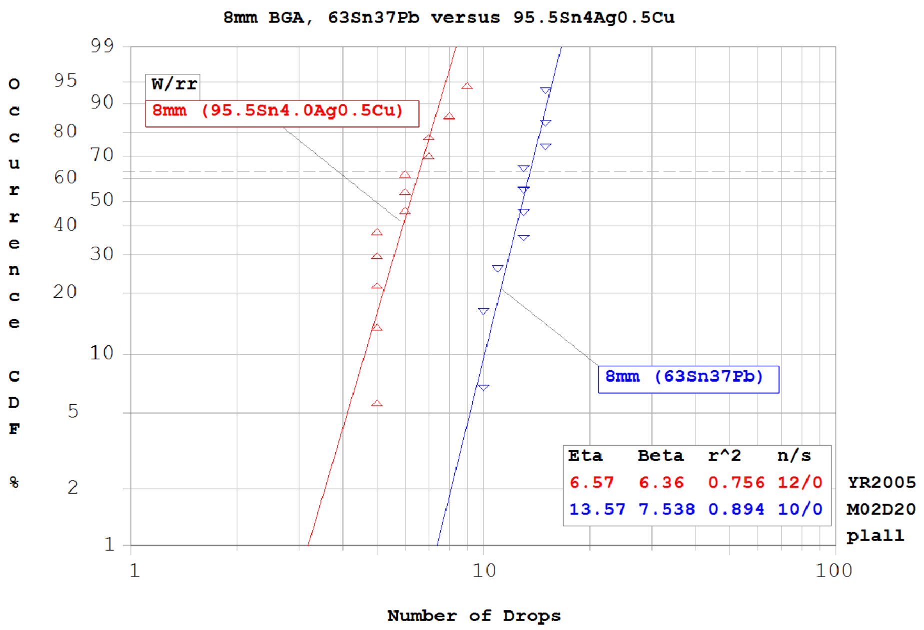


Figure 4.19: Weibull Data for Drops-to-Failure for 8mm Ball-Grid Arrays with 95.5Sn4.0Ag0.5Cu and 63Sn37Pb Solder Interconnects.

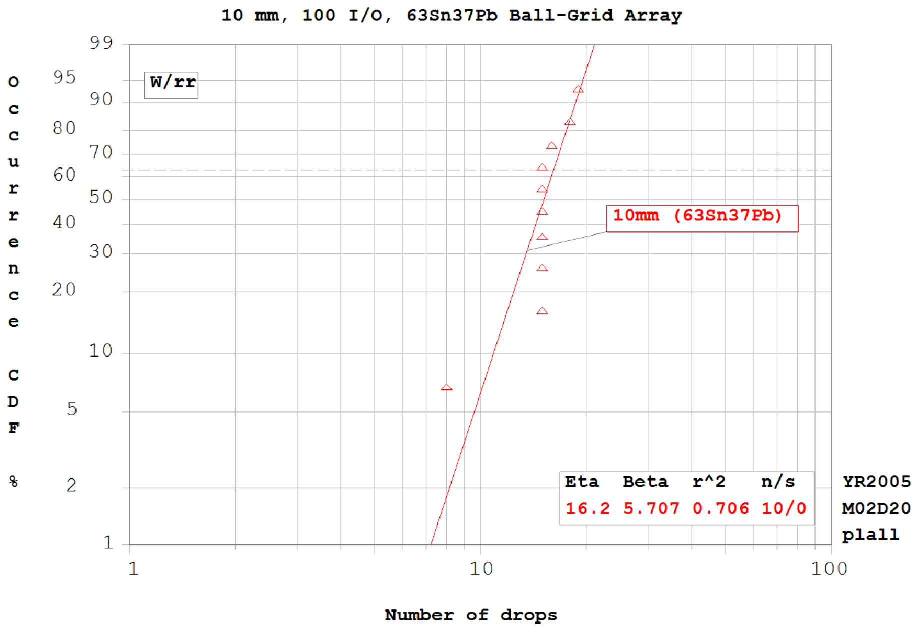


Figure 4.20: Weibull Data for Drops-to-Failure for 10mm Ball-Grid Arrays with 63Sn37Pb Solder Interconnects.

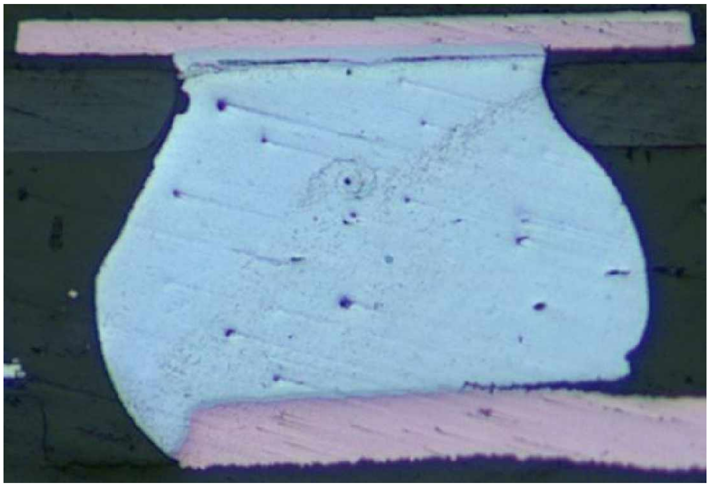


Figure 4.21: 95.5Sn4.0Ag0.5Cu Solder Interconnect failure at the package-to-solder interface and at the solder-to-board interface.

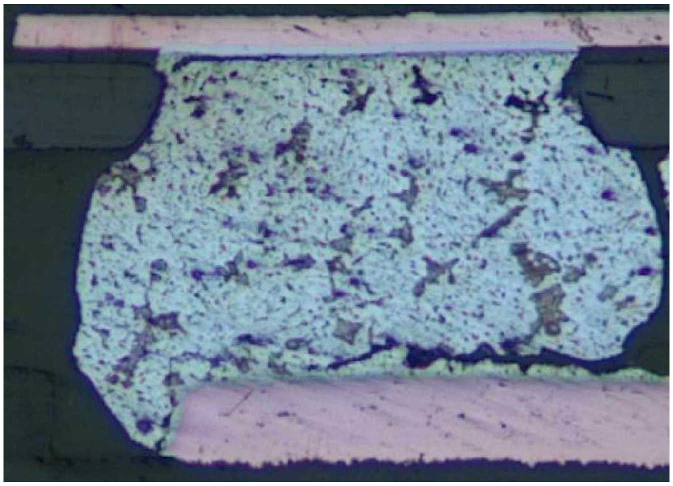


Figure 4.22: 63Sn37Pb Solder Interconnect Failure at the solder-to-board interface in 8mm, 132 I/O BGA.

4.9 Summary and Conclusions

In this dissertation, a methodology for development of the failure envelope for area-array packaging architectures has been developed. Wavelet transforms which have been used extensively in several areas including data and image processing, geophysics, power signal studies, meteorological studies, speech recognition, medicine, and motor vibration, have been applied to analysis of transient-response of electronics under shock and vibration. Wavelets have been used to avoid the problem of fixed time-frequency window with windowed Fourier transforms, which causes over-representation of the high-frequency components and an under-representation of the low-frequency components of a transient drop-impact signal. The need of different resolutions are required to analyze a variety of signal components of different duration has been addressed by using wavelet transforms. The Daubechies D_{10} wavelet with 12-level decomposition has been used to analyze non-stationary transient dynamic signals.

A relative damage index has been developed for prediction of the number of drops-to-failure under transient loads. The research presented attempts to address the need for techniques and damage proxies which enable the determination of failure-envelopes and cumulative damage during overstress and repetitive loading for various packaging architectures. The approach is based on assembly strains, since there are experimental limitations of measuring field-quantities and their derivatives at the board-solder joint interface, primarily because of the small size of interconnects in fine-pitch ball-grid array packages.

Explicit finite element models in conjunction with the proposed approach have been used to predict survivability of fine-pitch ball-grid arrays in transient-shock and vibration. The approach has been applied to both lead-free (95.5Sn4.0Ag0.5Cu) and leaded (63Sn37Pb) ball-grid array architectures. The validation has been presented for both repeatable and non-repeatable drops.

CHAPTER 5

LIFE PREDICTION AND DAMAGE EQUIVALENCY FOR SHOCK SURVIVABILITY OF ELECTRONIC COMPONENTS

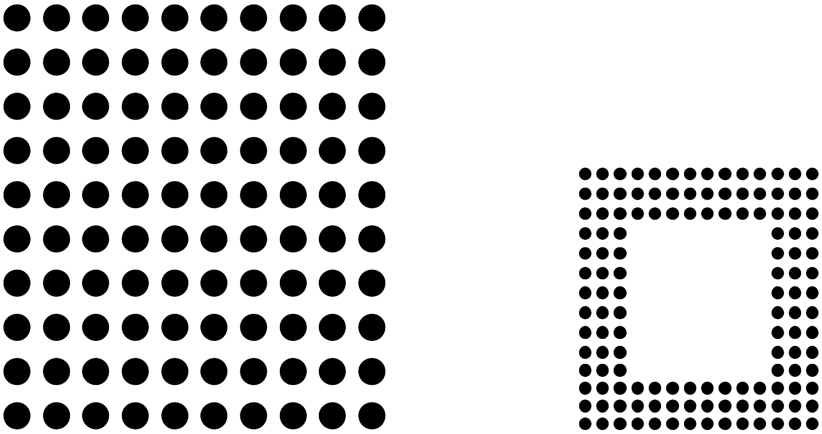
5.1 Introduction

Emerging trends of portable computing and communication applications towards smaller, lighter, form-factors have driven the need for robust-designs under overlapping environments of shock and vibration. Electronic products may be subjected to drop and shock due to mishandling during transportation or during normal usage. Test methods for drop reliability can be broadly classified into board-level and product-level tests, under constrained and unconstrained or free drop. Examples of board-level constrained drop include the JEDEC test method. The JEDEC test standard [2003] is often used to evaluate and compare the drop performance of surface mount electronic components for handheld electronic product applications. Correlation of the board-level tests to product-level performance is often challenging. Product-level failures are often influenced by housing design, in addition to drop-orientation, which may not always be perpendicular to the board surface [Lim 2002]. Factors such as drop height, mass of the product, impact orientation and the properties of the impacting surface affect the forces and the accelerations that are experienced by the product during impact. Design changes encompass an iterative process for improving the impact resistance of the electronic product. Use of experimental approach to test out every possible design variation, and identify the one that gives the maximum design margin is often not feasible because of product development cycle time and cost constraints.

5.2 Test Vehicle

Test vehicles A and B (Figure 5.1, Figure 5.2) were fabricated with various packaging architectures typical of fine-pitch electronic applications. Alloy compositions investigated include, 63Sn37Pb, and 95.5Sn4.0Ag 0.5Cu. Board finishes investigated include, immersion silver, ENIG, and HASL. Effect of capillary-underfilled and corner-bonded underfilled devices was also investigated.

Test board A includes, 10 mm ball-grid array, 0.8 mm pitch, 100 I/O and, 8mm flex-substrate chip scale packages, 0.5 mm pitch, 132 I/O. It has 10 components on one side of the board (Table 5.1). Test board B includes 27 mm, 1 mm pitch, 388 I/O ball-grid array packages, 16 mm, 0.8 mm pitch, 240 I/O ball-grid array packages, and 15 mm, 0.8 mm pitch, and 193 I/O ball-grid array packages (Table 5.2). The number of components varies from 6 to 10 on some of the boards. All the components are on one side of the board. For the several of the devices indicated in (Table 5.1, Table 5.2), conventional eutectic solder, 63Sn/37Pb and lead-free solder balls 95.5Sn4.0Ag0.5Cu have been studied. Test boards A and B are made of FR-4. These test boards were based on standard PCB technology with no build-up or HDI layers. Test Board A was 2.95" by 7.24" by 0.042" thick and Test Board B was 3.25" by 3.25" by 0.060" thick.

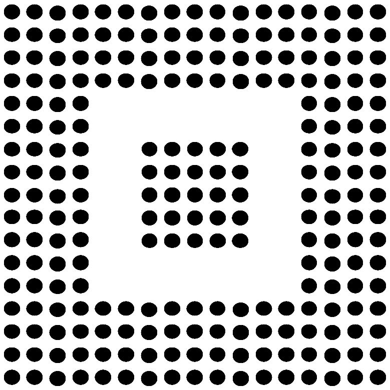

10 mm, 100 I/O BGA

8mm 132 I/O BGA

(a) Test Vehicle-A

Figure 5.1: Interconnect array configuration for 95.5Sn4.0Ag0.5Cu and 63Sn37Pb Test Vehicle-A.

27mm, 388 I/O BGA 16 mm, 240 I/O BGA



15 mm, 193 I/O BGA

(b) Test Vehicle-B

Figure 5.2: Interconnect-array Configuration for Ball-Grid Arrays, with 95.5Sn4.0Ag0.5Cu and 63Sn37Pb interconnects on Test Vehicle-B.

Table 5.1: Test Vehicle-A Configuration.

	10mm 100 I/O BGA	8mm 132 I/O BGA
Ball Count	100	132
Ball Pitch	0.8 mm	0.5 mm
Die Size	5 x 5	3.98 x 3.98
Substrate Thickness	0.5 mm	0.1 mm
Substrate Pad Dia.	0.3 mm	0.28 mm
Substrate Pad Type	SMD	Thru-Flex
Ball Dia.	0.46 mm	0.3 mm
Interconnect Alloy	63Sn37Pb	63Sn37Pb 95.5Sn4.0Ag 0.5Cu

Table 5.2: Test Vehicle-B Configuration.

	27 mm, 388 I/O BGA	16 mm, 240 I/O BGA	15 mm, 193 I/O BGA
Ball Count	388	240	193
Ball Pitch (mm)	1	0.8	0.8
Thermal Balls	36	Pad	25
Die Size (mm)	10 x 10	5 x 5	8.6 x 8.6
Substrate Thickness (mm)	0.56	0.56	0.56
Substrate Pad Diameter (mm)	0.5	0.45	0.4
Substrate Pad Type	SMD	SMD	SMD
Ball Diameter (mm)	0.6	0.53	0.6
Interconnect Alloy	63Sn37Pb 95.5Sn4.0Ag 0.5Cu		

5.3 Sequential Stresses

Test vehicles A and B have been exposed to sequential stresses of thermal aging followed by shock impact and, thermo-mechanical cycling followed by shock-impact. Thermal aging conditions include 125°C for 20 hours. Thermo-mechanical cycling included exposure to -40 to 125°C for 50 cycles (Figure 5.3). The thermal cycle duration is 90 minutes with 15 minutes ramps between temperature extremes and 30 minutes dwells at each temperature extreme (Table 5.3). No thermo-mechanical cracks were developed during the thermo-mechanical exposure, since the pre-conditioning is significantly smaller than the time to one-percent failure.

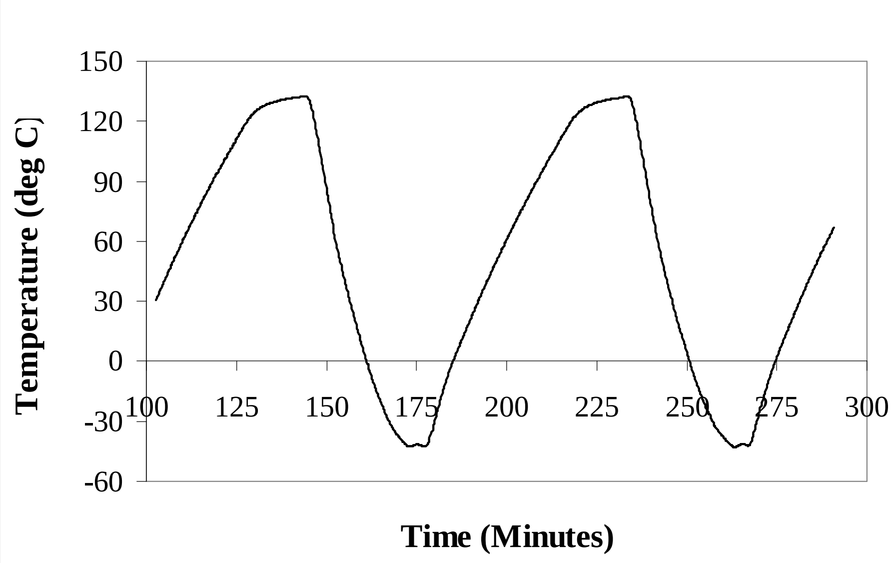


Figure 5.3: Thermal Cycling Profile.

Table 5.3: Profile for Temperature Cycle Chamber

Low Temp	High Temp	Ramp Up Time (sec)	Dwell Time High (sec)	Ramp Down Time (sec)	Dwell Time Low (sec)
-40	125	900	1800	900	1800

5.4 Finite Element Analysis

Previously, the JEDEC JESD22-B111 has been modeled has been modeled using the input-G method [Tee 2004]. In this dissertation, the use of explicit finite elements has been investigated (Figure 5.4). The use of explicit finite elements enables the calculation of response history using step-by-step integration in time without changing the form of dynamic equations as done in modal methods. The modeling effort has focused on prediction of transient dynamic drop response using explicit finite-element theory with reduced integration elements. An explicit algorithm uses a difference expression of the general form,

$$\{D\}_{n+1} = f\left[\{D\}_n, \{\dot{D}\}_n, \{\ddot{D}\}_n, \{D\}_{n-1}, \ldots.\right] \tag{5.1}$$

where {D} is the d.o.f. vector, the "." on top represents time integration, and subscript "n" represents the time-step. The equation contains only historical information on the right hand side. The difference expression is combined with the equation of motion at time step "n" for the simulation.

$$\begin{aligned} &\left(\frac{1}{\Delta t^2}[M] + \frac{1}{2\Delta t}[C]\right)\{D\}_{n+1} \\ &= \{R^{ext}\}_n - \{R^{int}\}_n + \frac{2}{\Delta t^2}[M]\{D\}_n - \left(\frac{1}{\Delta t^2}[M] - \frac{1}{2\Delta t}[C]\right)\{D\}_{n-1} \end{aligned} \tag{5.2}$$

The degree of freedom vector at the n-1 time-step is given by a Taylor series,

$$\begin{aligned} &\{D\}_{n-1} = \{D\}_n - \Delta t\{\dot{D}\}_n + \frac{\Delta t^2}{2}\{\ddot{D}\}_n - \frac{\Delta t^3}{6}\{\dddot{D}\}_n + \ldots \\ &\text{for } n = 0, \qquad \{D\}_{-1} = \{D\}_0 - \Delta t\{\dot{D}\}_0 + \frac{\Delta t^2}{2}\{\ddot{D}\}_0 \end{aligned} \tag{5.3}$$

The coefficient matrix of $\{D_{n+1}\}$ can be made diagonal using lumped mass-matrix or diagonalization of the consistent mass matrix, $[m] = \int \rho\, [N]^T [N]\, dV$ through techniques such as HRZ lumping. Therefore, $\{D_{n+1}\}$ can be cheaply calculated for each time step. Drop height required for a 1500 Gs, 0.5 millisecond duration, and half-sine input pulse has been determined. In addition, the free-drop of printed circuit assembly with weight attached on top has also been modeled. Transient Dynamic Behavior of a populated printed circuit board during drop using Abaqus™ Explicit. An initial velocity of $\{\dot{D}\}_0$, equivalent of the required drop has been assigned to the board, components and the weight at the top edge of the board (Equation 5.3). The printed circuit board and components have been modeled with reduced integration tetrahedral elements. The concrete floor has been modeled with rigid R3D4 elements. Reduced integration elements have been used for computational efficiency because evaluation of internal force vector, $\{r^{int}\}_n$ requires the same order of quadrature as element stiffness matrix [K].

A reference node has been placed behind the rigid wall for application of constraints. Contact has been monitored between any PCB surface, CSP surface or Weight surface and only on the positive side of the floor. Node to surface contact has been used. An event length of 20 ms after impact has been modeled. Time history has been monitored at a time period of 0.1 ms at the corner of all CSPs. The Gerschgorin Bound has been used to provide an estimate of highest natural frequency, ω_{max}, which is used for calculation of the critical time step size. For a lumped diagonal mass matrix, it may be stated as follows,

$$\omega_{max}^2 \le \max_i \left(\frac{1}{M_{ii}} \sum_{j=1}^{n} \left| K_{ij} \right| \right) \tag{5.4}$$

where, i = 1, 2, 3,….,n, and n is the matrix order of number of degrees of freedom, K and M are the stiffness and mass matrices respectively. Smeared properties and stiffnesses have been used for computational efficiency as described in [Lall 2004]

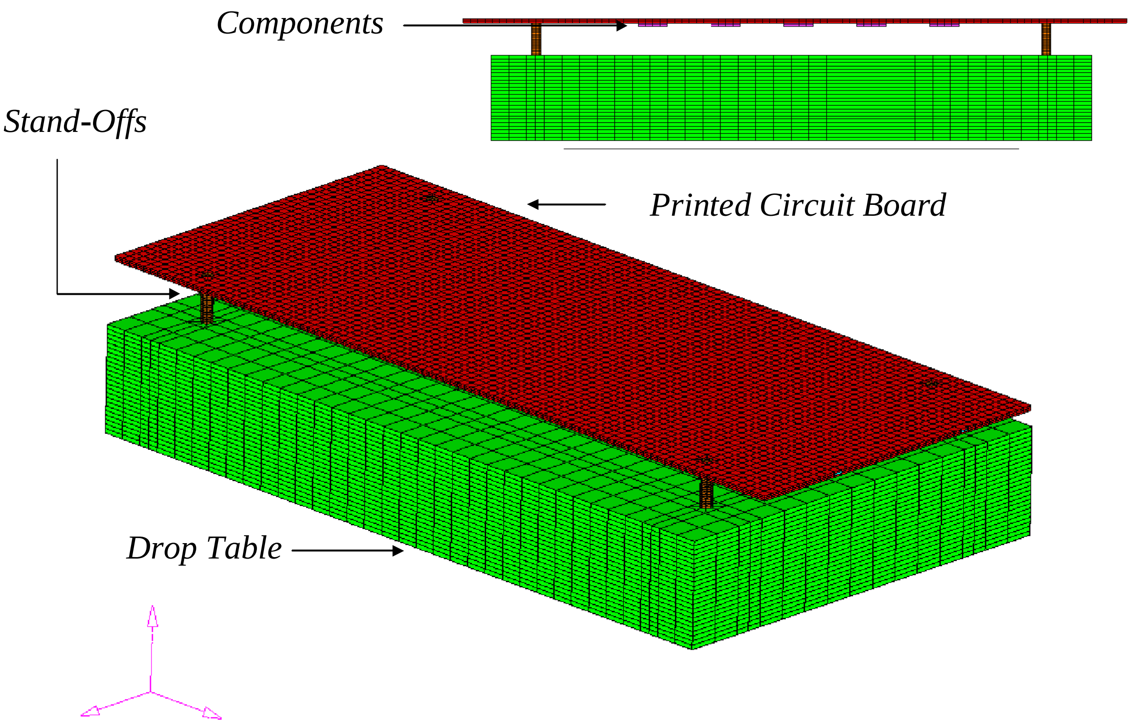
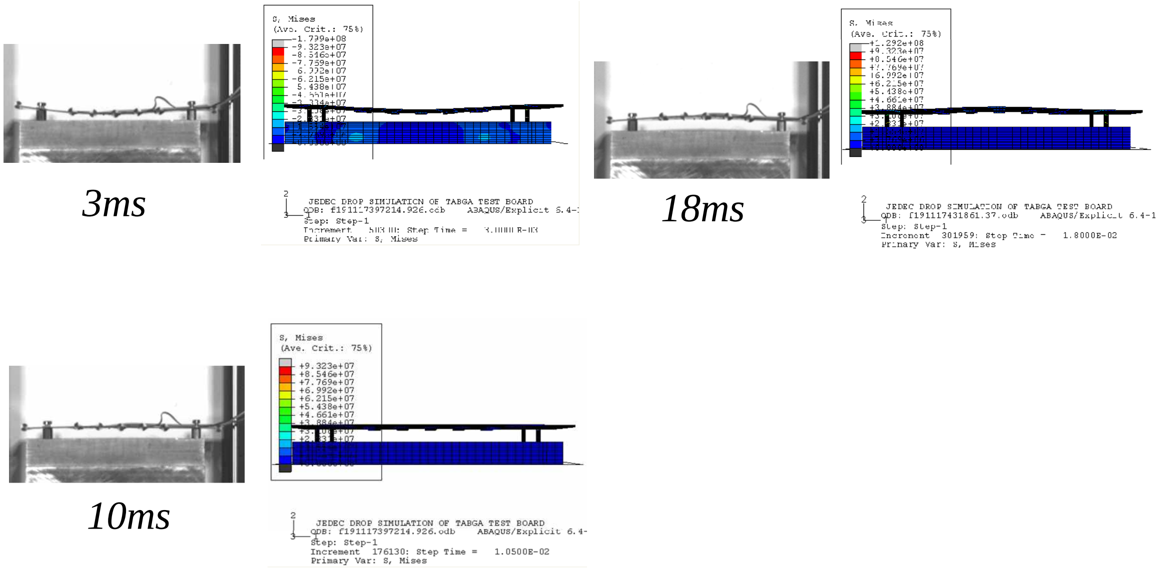


Figure 5.4: JEDEC Drop Test Model with Smeared Property Hexahedral Elements.

5.5 Model Correlation

Strain data has been acquired on the top surface of the components using high speed data-acquisition system simultaneously sampling at 5 MS/sec. The transient strain and displacement history has been predicted from explicit finite element simulations. Transient displacement of the printed circuit board has been correlated using high speed video imaging operating at 50,000 fps (Figure 5.5). The relative displacement history has been measured using high-speed image analysis systems (Figure 5.6).

Both relative displacement and transient package strain show good correlation. There is scope to improve the correlation of the experimental and finite element model in terms of relative displacement and strain results. Currently the finite element model assumes linear elastic material properties at low strain rate. Material properties at high strain rate events such as shock and drop needs to be characterized and implemented in the FEM models. Also it will be of interest to accurately model all the package details and the solder balls. This FEM model uses smeared property approach.


3ms

18ms

10ms

Figure 5.5: High-Speed Correlation of Transient Displacement.

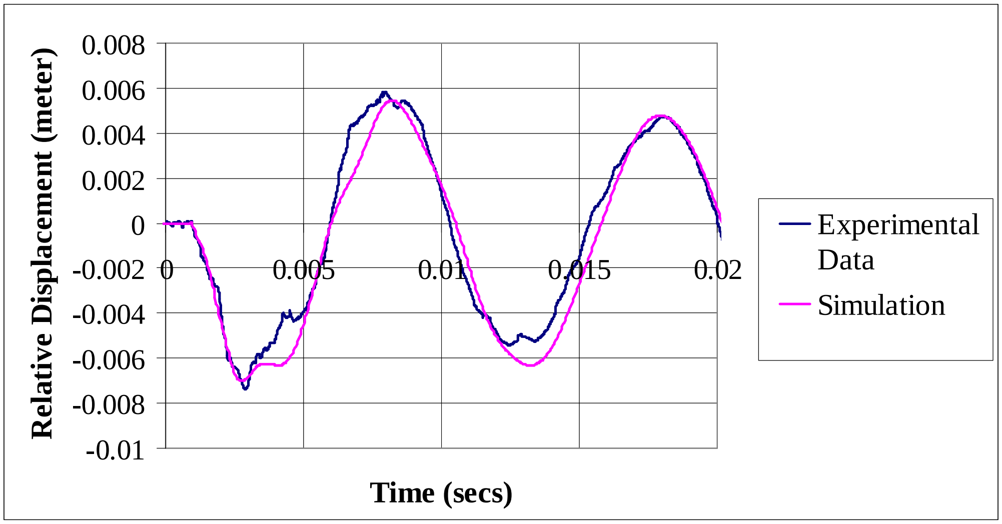


Figure 5.6: Correlation of Simulated Package Relative Displacement versus Experimental Measurements.

5.6 Modal Analysis

5.6.1 Introduction

Physical systems can vibrate. Natural frequencies of vibration and mode shapes are properties of the system and can be determined experimentally and analytically using Modal analysis. Inherent vibration modes can shorten equipment life and cause premature failure which may result in hazardous situation. Its main application is in mechanical and aeronautical engineering, but it is also gaining widespread use in civil and structural engineering, biomechanical problems, space structures, acoustic instruments and nuclear engineering.

Modal testing involves artificially exciting a structure through mechanical excitation, created either by vibrational or impact methods to measure its natural frequencies, mode shapes, damping properties and sometimes inertia properties. These dynamic characteristics are often measured by accelerometers or lasers. It is often undertaken to correlate finite element (FE) models either visually or using more rigorous techniques such as modal assurance criteria and orthogonality. Once the FE model has been proven to accurately represent the physical hardware, it can be used to predict a revised design or dynamic behavior under difficult to reproduce operating conditions. The mode shapes indicate the points of maximum deflection.

Application

- Damage Detection: Mode shapes have been used to identify local damages that caused curvature changes and e.g. the modal frequencies has been used to identify global damages.
- Vibration Level Documentation:

If the vibration level needs to be documented in locations where no measurements can be made, from the modal test you will obtain the modal coordinates or modal response at some measurable locations. These modal responses will then be extrapolated to other unmeasured locations through the mode shapes of the FE model, and by superposition the actual responses at the location is estimated. Even though the FE models only return normal modes this extrapolation will be good most structures.

5.6.2 Transfer Function

Frequency transfer functions measurements are made to define modal frequencies, damping values, modal vectors, modal mass, modal stiffness and modal damping of real life structures.

The transfer function representation of an undamped multiple degree of freedom system can be formulated from the differential equations of motion in terms of mass, stiffness and damping matrices. [Allemang 1999]

$$[M]\{\ddot{x}\}+[K]\{x\}=\{f\} \tag{5.5}$$

Taking Laplace Transform, assuming all initial conditions such as displacements and velocities are zero, yields:

$$[s^2[M]+[K]]\{X(s)\}=\{F(s)\} \tag{5.6}$$

Represent the first term as,

$$[B(s)]=[s^2[M]+[K]] \tag{5.7}$$

Then the equation becomes:

$$[B(s)]\{X(s)\}=\{F(s)\} \tag{5.8}$$

Where $[B(s)]$ is referred as the system impedance matrix or just the system matrix. Pre-Multiplying Equation by $[B(s)]^{-1}$ yields:

$$[B(s)]^{-1}\{F(s)\}=\{X(s)\} \tag{5.9}$$

Defining:

$$[H(s)]=[B(s)]^{-1} \tag{5.10}$$

Then:

$$[H(s)]\{F(s)\}=\{X(s)\} \tag{5.11}$$

Above equation relates the system response $\{X(s)\}$ to the system forcing function $\{F(s)\}$ through the matrix $[H(s)]$.

This matrix is generally referred to as the Transfer Function matrix. The above equation can be extended for MDOF.

$$\frac{X_p(s)}{F_q(s)} = H_{pq}(s) = \frac{\beta_n(s)^n + \beta_{n-1}(s)^{n-1} + \beta_{n-2}(s)^{n-2} + \cdots + \beta_1(s)^1 + \beta_0(s)^0}{\alpha_n(s)^n + \alpha_{n-1}(s)^{n-1} + \alpha_{n-2}(s)^{n-2} + \cdots + \alpha_1(s)^1 + \alpha_0(s)^0} \tag{5.12}$$

The roots of the denominator polynomial are the modal frequencies of the system and are considered as the global properties of the system the roosts of the numerator polynomial are the zeroes of the system and are local properties of the system that depend upon the specific input-output relationship of the transfer function. The above equation can be written in more concise form as:

$$\frac{X_p(s)}{F_q(s)} = \frac{\sum_{k=0}^{n} \beta_k (s)^k}{\sum_{k=0}^{m} \alpha_k (s)^k} \tag{5.13}$$

This model can be generalized to represent the general multiple input, multiple output case.

5.6.3 Excitation systems and Sensors

Any vibration test system requires a device to subject the test object to some vibration motion. Such device may be attached to the structure or not. The most classical set-up consists of one or more shakers standing on the ground (or fixed to some frame) and attached to the structure. Others are attached to the structure only. In these cases, the shaker affects to some extend the dynamic behavior of the structure. In other cases non-fixed excitation is used: no device is attached to the object. Hammer excitation is the best known example.

5.6.3.1 *Fixed-fixed excitation systems*

This type of shaker is mounted on the ground and attached to the structure. The most commonly used fixed-fixed exciters are hydraulically or electro dynamically driven. Where large displacement strokes are required, electro-hydraulic shaker are perfect. An electronic servo-control system allows the easy derivation and regulation of the vibration signal, while the hydraulic drive system can show long stroke and high force capabilities.

5.6.3.2 *Motion transducers*

The usual response in a modal analysis test of a mechanical structure is the motion of the object, expressed as displacement, velocity or acceleration. Theoretically it is irrelevant which of the three motion parameters is measured. Displacement measurements place more weight on the low frequencies. Acceleration measurements stress the higher frequencies. The RMS (root mean square) value of the velocity is considered to be a measure of the severity of the vibration, since the vibration velocity is in a simple way related to the vibration energy. This may be an important reason to measure velocity. However, as proven in ref b.1.7, displacement and velocity transducers tend to be relatively heavy. Most motion transducers are relatively simple mass-spring systems, showing resonance frequency. A displacement transducer generates a signal proportional to a displacement in a frequency band above its own resonance. This necessitates a low transducer resonance and hence, a relatively high mass. ($\omega_r^2 = k / m$). The opposite is true for an accelerometer. The lower mass of an accelerometer will have a much smaller influence when attached to the structure and therefore results in a more accurate measurement.

An additional factor that underlines the benefits of accelerometers is the fact that an acceleration signal can easily and validly be integrated electronically to obtain velocity and displacement. Electronic differentiation of velocity and displacement is more dubious.

5.6.3.3 Non-contact type motion transducers

For special applications specific motion transducers can be used. For very small, light weight structures non-contact measurements may be necessary. One possible way to measure displacements of surfaces of an electrically conductive material is based upon the inductive proximity principle. Laser vibrometers are another alternative for contact less motion measurements.

Principle: The signal beam is directed onto the vibrating surface and reflected. The reflected light is combined with the internal reference beam. When the surface moves, the path difference between reference and reflected signal beam varies. This results in an intensity modulation of the recombined beam due to interference phenomena. This can be seen as the effect of the recombination of a reference beam with a signal beam, the frequency of which is shifted by the Doppler Effect by an amount of $f_d = 2v/\lambda$ (with λ the wavelength of the laser and ‘v’ the velocity of the surface). Since one-to-one correspondence exists between the Doppler frequency f_d and the frequency of the intensity modulation, it contains the information about the surface velocity. More electronics allows determining the direction of the velocity and generates a voltage signal proportional to the surface velocity. Such device allows measurements from 0 to 50 kHz and from 0 to 100 mm/s.

Other non-contact motion measurement devices are based upon light beam sensors or speckle Interferometry.

5.6.3.4 Input Excitation evaluation Criteria

The selection of the excitation of the shaker depends on many factors: the availability and complexity of the equipment, the available time, the signal’s sensitivity for bias and variance errors, the (non-)linear behavior of the device under test, the controllability of the excitation signal, the required measurement accuracy, and so on.

5.6.3.5 Pure Random Signals

The pure random excitation signal is a non-periodic stochastic signal with a Gaussian probability distribution. It contains all frequencies in a specified frequency band. However, since the properties of the excitation frequency spectrum are only described in a stochastic way, averaging is essential when estimating this frequency spectrum. Due to its relatively low peak to RMS ratio (typically 3…4), pure random easily averages out non-coherent noise. Furthermore, pure random yields the best linear approximation of non-linear systems, since in each averaged time record the non-linear distortions will be different and tend to cancel with sufficient averaging. It also has good signal to noise ratio, and the easy control of the RMS level. The main problem of random signal is leakage. A minor drawback is that test time is relatively long due to a necessary number of averages.

5.6.4 Experimental Set-up

The responses are usually measured in frequency domain and are commonly called as Frequency Response functions or Transfer Function. The frequency response was measured on matrix of 4 X 10 grids as shown in Figure 5.7 on Test vehicle A with packages facing down. The test vehicle is mounted on rigid aluminum plate with four screws/standoffs. The rigid aluminum plate was mounted on the shaker and excited randomly (Figure 5.8). The electrodynamic shaker used for the experiment is LDS V408 which has a frequency range from 5 Hz - 9000 Hz. The response was measured using two laser vibrometers (Figure 5.9). One reference laser was always kept at grid number 9 and the second laser beam was scanned on all other grid points. The block diagram of the experimental modal testing is shown in Figure 5.10. Laser vibrometers measured the frequency response of the grid points relative to grid point number 9. Measured frequency domain was in the range of 100-900 Hz. Figure 5.11 shows a sample frequency response function at grid point 18. Four distinct modes were observed in this range.

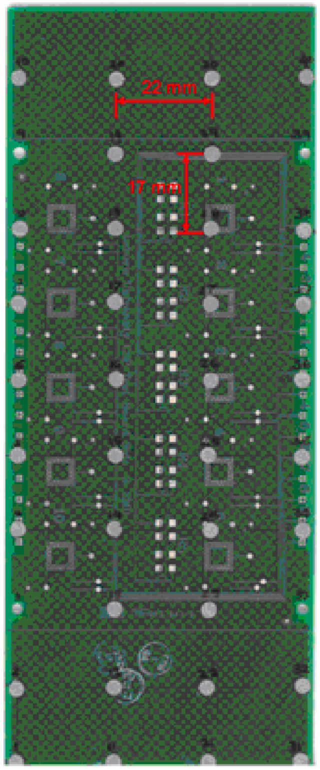


Figure 5.7: Grid points on TABGA board

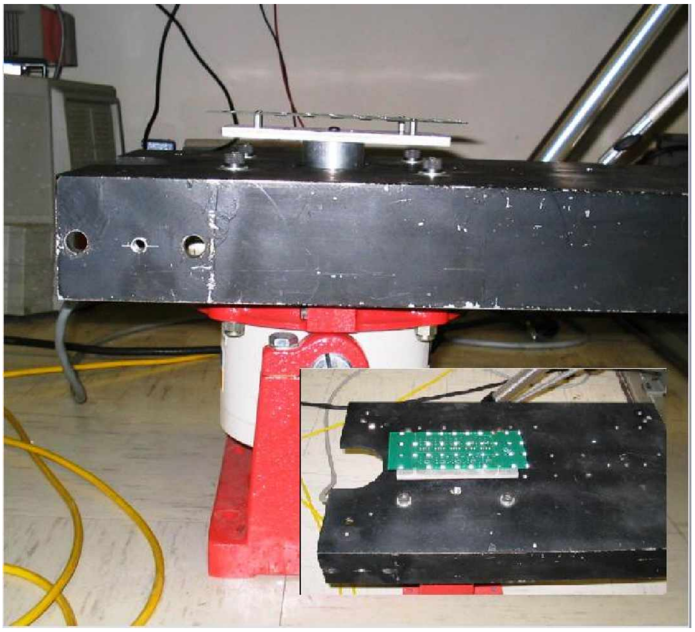


Figure 5.8: Specimen mounted on the shaker

Figure 5.9: Laser Vibrometers

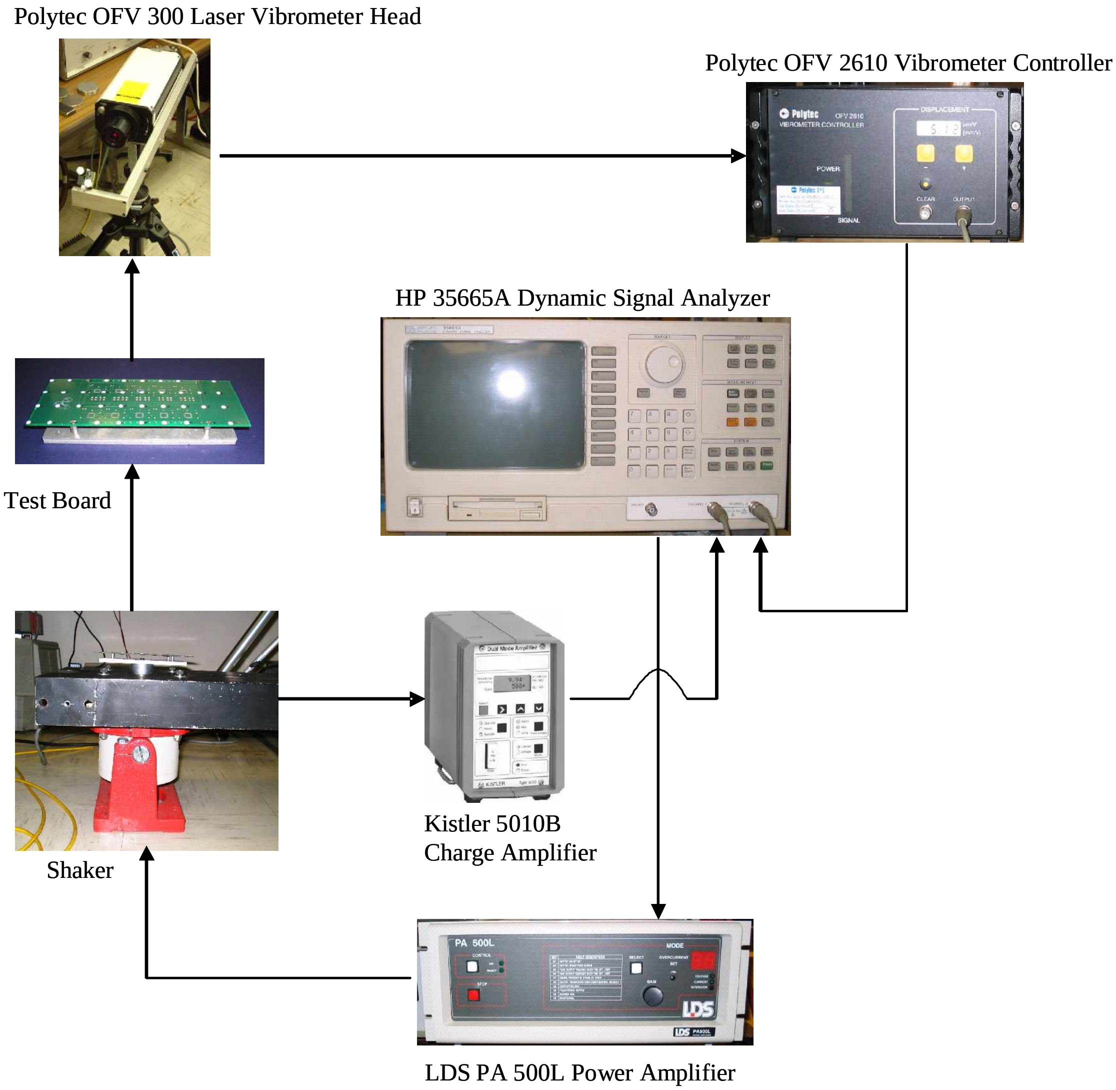


Figure 5.10: The whole experimental modal testing set-up

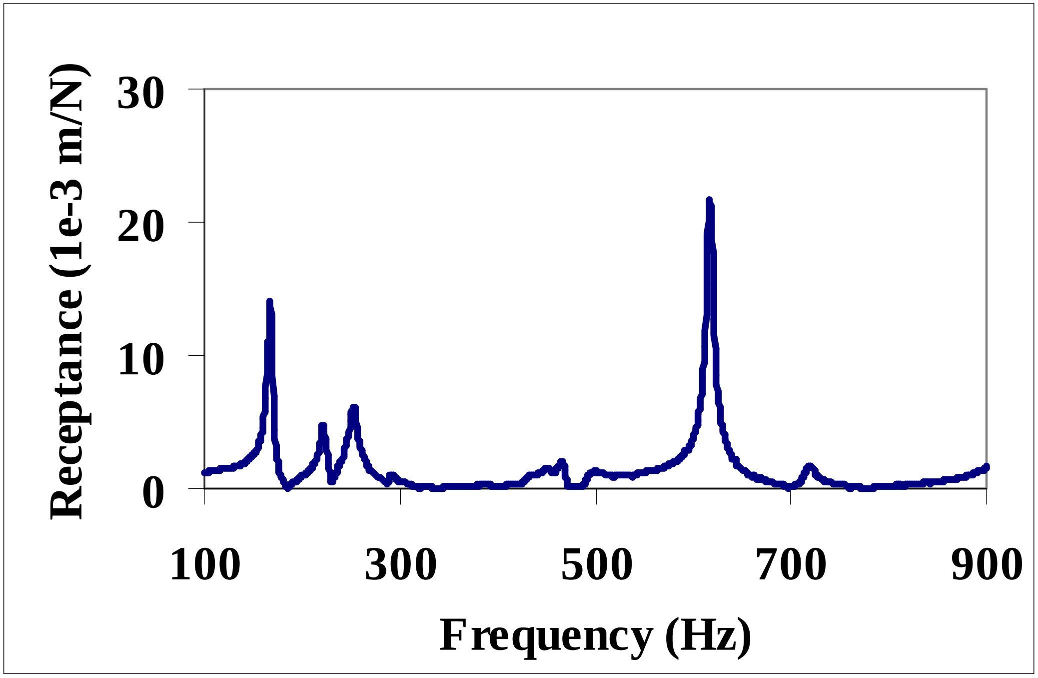


Figure 5.11: Transfer Function

5.6.5 Modal assurance criterion (MAC)

The modal assurance criterion has been used for determination of correlation between predicted and measured mode shapes. Theoretically, MAC value near one indicates a high degree of correlation or consistency between two mode shapes. Natural frequencies and mode shapes are extracted from FE model using Abaqus/Standard. Normalized nodal displacement at the corresponding grid locations (Table 5.5) is extracted from the FE model.

Modal Assurance Criteria is given as:

$$\mathrm{MAC(A, X)} = \frac{\left| \sum_{j=1}^{n} (\psi_X)(\psi_A)_j^* \right|^2}{\left(\sum_{j=1}^{n} (\psi_X)(\psi_X)_j^* \right) \cdot \left(\sum_{j=1}^{n} (\psi_A)(\psi_A)_j^* \right)} \tag{5.14}$$

where:
(ψ_X) = Experimentally measured mode shape
$(\psi_X)_j{}^*$ = Complex conjugate
(ψ_A) = Theoritically predicted or analytical mode shape

n = Number of degrees of freedom

This is a scalar quantity. The modal assurance criterion does not discriminate between random scatter. Thus, these parameters are useful means of quantifying the degree of correlation between two sets of mode shape data, but they do not present the whole picture and should preferably be considered in conjunction with the plots of coherence function. MAC value of one means the experimental and the predicted mode shape correlate exactly. MAC value less than unity may be because of non-linearities in the test structure, noise on the measured data, and poor modal analysis of measured data or inappropriate choice of DOFs included in the correlation.

Table 5.4: Modal Analysis of Test Vehicle A

	Simulation (Hz)	Experiment (Hz)	% Difference	MAC
Mode 1	153	168	-8.92	0.958

Table 5.5: Experimental and Analytical Correlation of the first four mode shapes of Test Vehicle A.

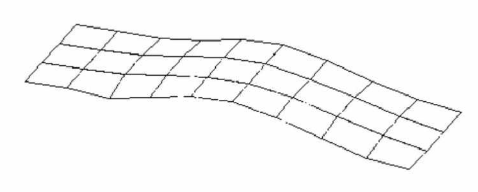
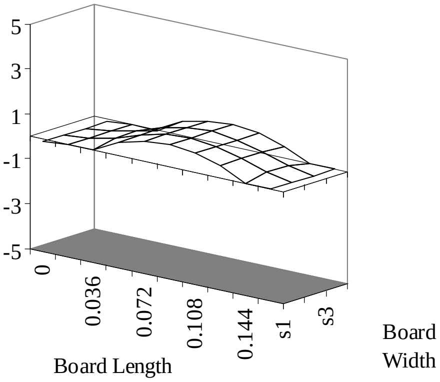
Experiment	**Simulation (Analytical)**
153 Hz	168 Hz
	
Error (%)	-8.92%
MAC	0.96

Table 5.4 shows the experimentally and analytically calculated and mode shapes. MAC of 0.96 for the first mode shows a good correlation of the mode shape. However for the subsequent mode shapes the MAC is below 0.9. This can be explained as experimental error. One needs to make sure the surface need to be perfectly flat so as to accurately measure the transfer function. Also approximations in the material property for Finite Element model can cause errors in measuring mode shapes. One of the reasons for the error can be seen from the coherence function plot in Figure 5.12

5.6.6 Coherence

Coherence at all the grid locations is recorded, since it is indicator of false data. Generally coherence value of 0.9 and above is good indicator that the displacement data is accepted. Coherence is the ratio of the input-output cross-spectrum to the product of the input and output auto spectrum. The magnitude squared coherence estimate is a function of frequency with values between 0 and 1 that indicates how well the input signal corresponds to the response output at each frequency and at each gird location. Mathematically, the coherence is a function of the power spectral density (Pxx and Pyy) of x and y and the cross power spectral density (Pxy) of x and y. x and y must be the same length. The coherence is given as follows:

$$C_{xy}(f) = \frac{\left|P_{xy}(f)\right|^2}{P_{xx}(f)P_{yy}(f)} \qquad (5.15)$$

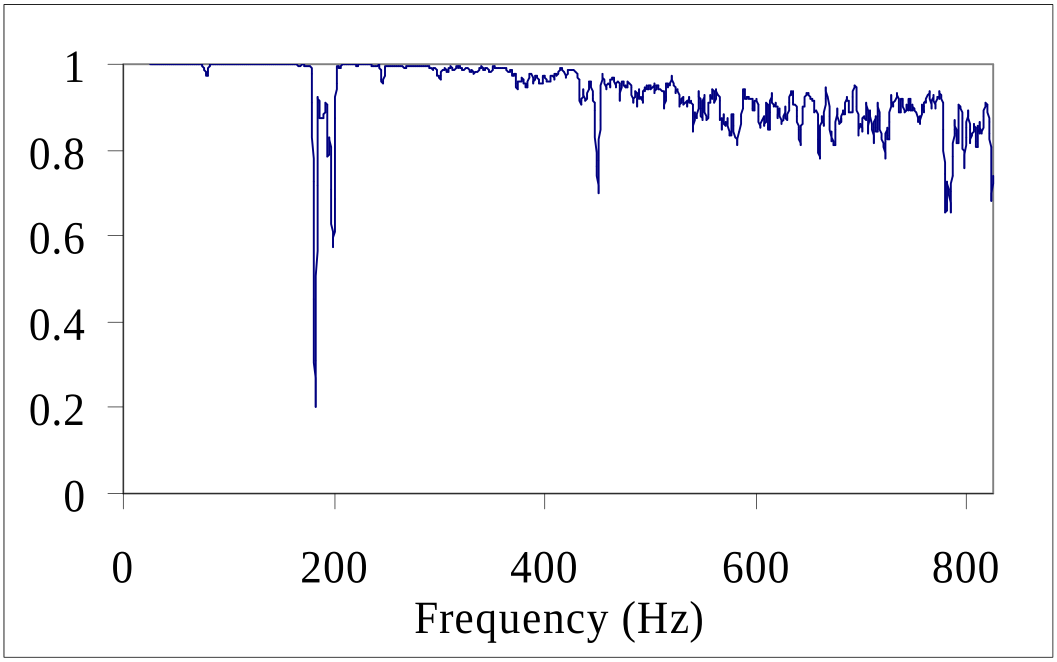


Figure 5.12: Coherence

5.6.7 Damping in PCB assemblies

The printed circuit board assembly is characterized by its mass, stiffness and damping matrices. The first two may be obtained from the geometry and material properties of the structure; however, damping for inclusion in the FE analysis has been determined through experiments. For purposes of this experiment it is assumed that the only damping present in the structure is due to viscous damping. Two commonly used methods to determine the damping in structure is the logarithmic decrement method and the half power bandwidth method. Later method is used in the study since logarithmic decrement technique is more effective for lightly damped systems. The total loss factor of a structure is a linear sum of the damping loss factor and the radiation damping loss factor of the structure [Norton 1989]. Current research concentrates on the damping loss factor only. The half power bandwidth method uses the transfer function of the structure to determine the amount of damping for each mode.

5.6.7.1 Half-Power Bandwidth method

The half power bandwidth method Figure 5.13 uses the transfer function plot to obtain the damping in the structure. The method consists of determining the frequencies at which the amplitude of the transfer function is $x_{max}/\sqrt{2}$ and x_{max}. The frequencies associated on either side of the peak ω_1 and ω_2 are obtained as shown in Figure 5.13. The damping ratio is obtained using following formula.

$$\frac{\omega_2 - \omega_1}{\omega_n} = 2\xi_n \tag{5.16}$$

The damping ratio can be obtained with each natural frequency using half power bandwidth method. Rayleigh Damping in the form of α and β is obtained using the equation, $[C] = \alpha[M] + \beta[K]$ where, 'α' and 'β' is obtained from the following equation.

$$\alpha + \beta\omega_i^2 = 2\omega_i\xi_i \tag{5.17}$$

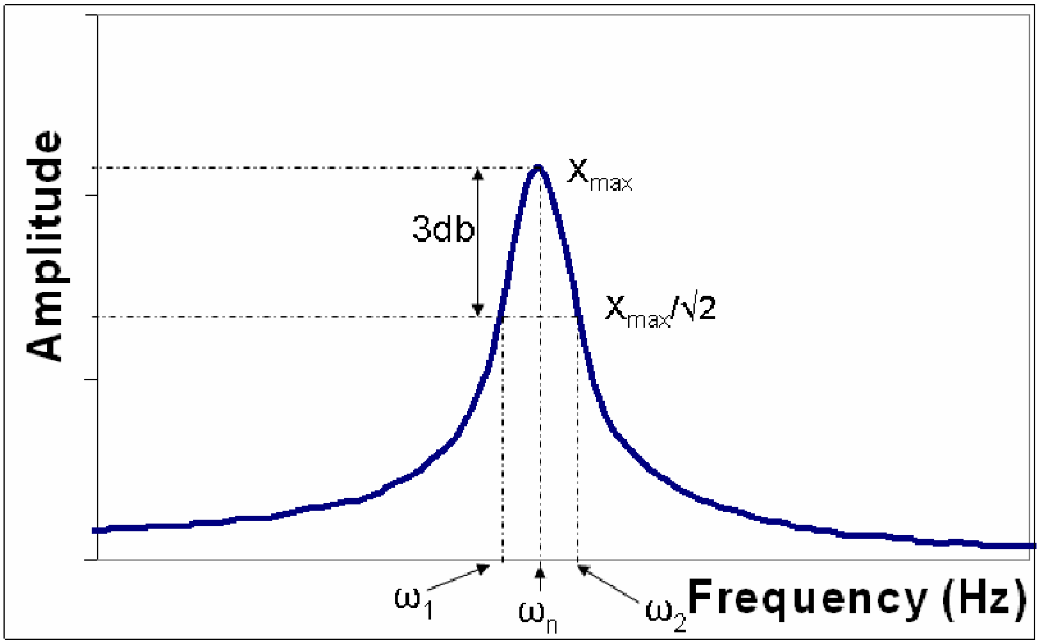


Figure 5.13: Half Power Bandwidth Method

Limitations of bandwidth method

- Actual peak in the transfer function is difficult to capture.
- Interpolation is required to estimate the half-power points.

5.6.7.2 Damping in Finite Element model

Due to the limitation in our knowledge about damping the most effective way to treat damping, within modal analysis framework is to treat the damping value as an equivalent Rayleigh Damping in the form of

$$[C] = \alpha[M] + \beta[K] \tag{5.18}$$

where, [C] = Damping matrix of the physical system, [M] = Mass matrix of the physical system, [K] = Stiffness matrix of the system, α, β = Pre-defined constants.

Advantage of converting the damping matrix into an equivalent Rayleigh damping lies in the fact that using orthogonal transformation a structure having n degrees of freedom can be reduced to n-number of uncoupled equations. However, for systems with large degrees of freedom, it is difficult to guess meaningful values of α and β at the start of the analysis.

A system having multi-degrees of freedom, the equation of motion for externally applied time dependent force is given by [Wilson 1972, Rao 2005]

$$[M]\{\ddot{X}\} + [C]\{\dot{X}\} + [K]\{X\} = \{P_t\} \tag{5.19}$$

in which $\{P_t\}$ force vector which is a function of time.

By orthogonal transformation, the above equation reduces to

$$\{\phi\}^T[M]\{\phi\}\{\ddot{\xi}\} + \{\phi\}^T[C]\{\phi\}\{\dot{\xi}\} + \{\phi\}^T[K]\{\phi\}\{\xi\} = \{\phi\}^T\{P_t\} \tag{5.20}$$

Above equation subsequently reduces to an n-uncoupled equation of the form

$$\{\ddot{\xi}_j\} + 2\,\zeta_j\,\omega_j\{\dot{\xi}_j\} + \omega_j^2\{\xi_j\} = \{P_j(t)\} \tag{5.21}$$

in which $\{\xi\}$ is displacement of the structure in the transformed co-ordinate, ζ = damping ratio in uncoupled mode, ω = natural frequency of the system, $\{P_t\}$ = modified force vector in transformed co-ordinate, $\{\phi\}$ = normalized Eigen vector of the system.

By orthogonal transformation the damping term in eqn. (3) reduces to

$$\{\phi\}^T[C]\{\phi\} = \begin{bmatrix} \alpha+\beta\omega_1^2 & 0 & . & 0 & 0 \\ 0 & \alpha+\beta\omega_2^2 & . & . & 0 \\ . & . & . & . & . \\ 0 & . & . & . & . \\ 0 & 0 & . & . & \alpha+\beta\omega_n^2 \end{bmatrix} \tag{5.22}$$

From symmetry, it can be inferred that

$$\begin{aligned} 2\zeta_1\omega_1 &= \alpha+\beta\omega_1^2 \\ 2\zeta_2\omega_2 &= \alpha+\beta\omega_2^2 \\ &\ldots\ldots\ldots\ldots\ldots\ldots\ldots \\ &\ldots\ldots\ldots\ldots\ldots\ldots\ldots \\ 2\zeta_n\omega_n &= \alpha+\beta\omega_n^2 \end{aligned} \tag{5.23}$$

When the system has two degrees of freedom eqn. (6) reduces to

$$\begin{aligned} 2\zeta_1\omega_1 &= \alpha+\beta\omega_1^2 \\ 2\zeta_2\omega_2 &= \alpha+\beta\omega_2^2 \end{aligned} \tag{5.24}$$

To find the values of α and β, one has to solve the eqn. (5.19). However, while solving a system having large degrees of freedom, the analyst is in some difficulty to arrive at the values of Rayleigh coefficients, which shall be valid for all the n degrees of equation or shall be valid for all significant modes. There is no straightforward solution to arrive at these values. An iterative solution is possible and this can be obtained possibly from best-fit values of α and β in a particular system.

5.7 Damage Prediction Models

The relative damage index has been used to predict the number of drops to failure for aged and pristine 8 mm Ball Grid Array, 95.5Sn4Ag0.5Cu, 132 I/O Packages. The location for the predictions is different from location at which the experimental data was acquired. Therefore, the transient-strain history and the damage progression are also different.

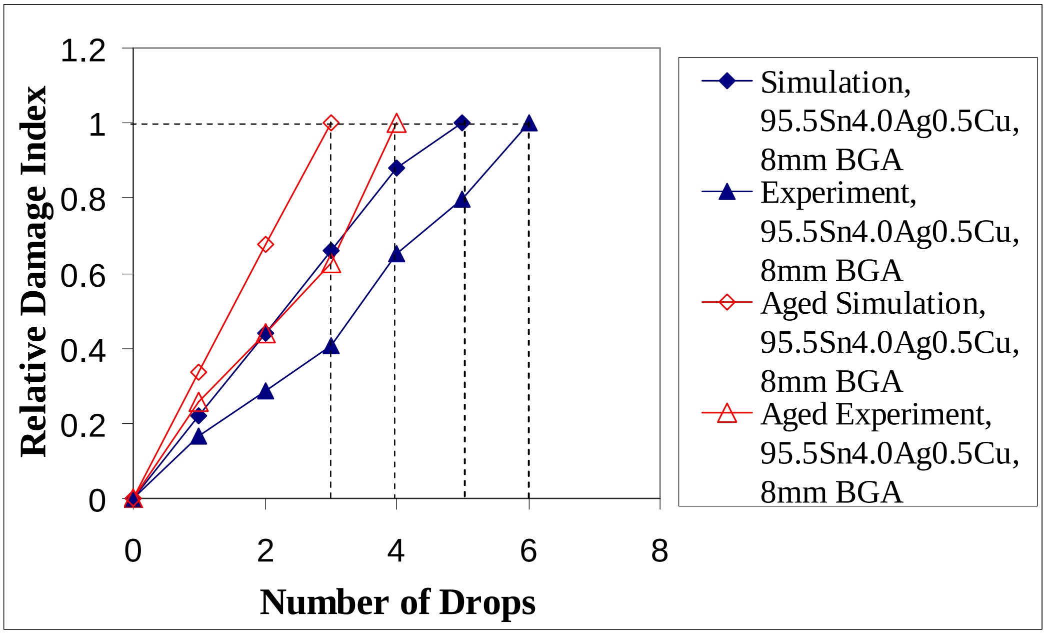


Figure 5.14: Correlation of Damage Progression and Number of Drops to Failure Between Experiment and Simulation for the 8 mm, 95.5Sn4Ag0.5Cu, 132 I/O Ball Grid Array.

Model prediction indicates 5 drops-to-failure and correlates well with the experimental data, which indicates that the ball-grid arrays at the location of measured transient strain failed after 6 drops. The present data-set is one has been chosen for correlation, because it is a representative average of the damage progression at this location. Number of drops-to-failure at this location ranged between 5-7 drops. The correlation is for non-repeatable vertical-drops, indicated by the non-uniform damage progression in experimental data-set (Figure 5.14). Exposure to thermal aging reduces the number of drops to failure for both experimental data and simulation.

The relative damage index approach outlined in this dissertation provides a method to define the damage equivalency for a variety of aging conditions for fine-pitch packaging architectures. The solder interconnect strain is not as easily measurable as board strain or package strain. The proposed methodology enables evaluation of the damage equivalency in the application of interest and for the packaging architecture in question. Damage during the life of the product should not exceed “1” for the design to have good survivability in drop and shock applications. The constants used for damage progression are specific to the package architecture and boundary conditions. The proposed methodology is amenable to implementation not just at board-level but also at system-level.

5.8 Failure Analysis and Mechanisms

All the test specimens were cross-sectioned to determine the failure modes. Observed failure modes include, solder interconnect failures at the package and the board interface, copper-trace cracking, and printed circuit board resin cracks under the copper pads. In order to develop a consistent damage equivalency on a failure mode specific basis, the failure modes have been sorted. The observed failures were predominantly in the solder interconnects for both the leaded and the lead-free packaging architectures.

The 95.5Sn4.0Ag0.5Cu solder interconnects were observed to have lower shock and vibration survivability when subjected to thermal aging and thermal cycling pre-conditioning (Figure 5.15, Figure 5.17). Figure 5.16 shows the intermetallic growth in 95.5Sn4Ag0.5Cu solder joints in the 27mm BGA after 50 cycles of -40 to 125C. Both Weibull distributions exhibit similar slopes, in the neighborhood of β = 2-3 indicating the consistency in failure mechanism and mode. The free drops are conducted with assemblies in vertical configuration. The zero-degree drops are JEDEC drops.

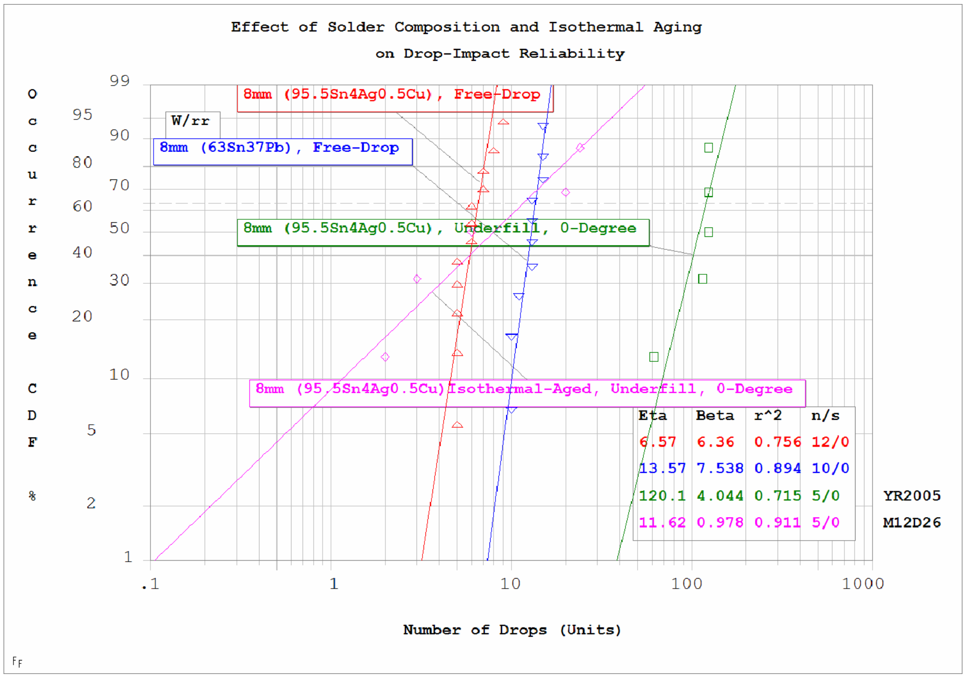


Figure 5.15: Weibull Data for zero-degree Drops-to-Failure for 8mm Ball-Grid Arrays with 95.5Sn4.0Ag0.5Cu and 63Sn37Pb Solder Interconnects with CAPILLARY UNDERFILLS.

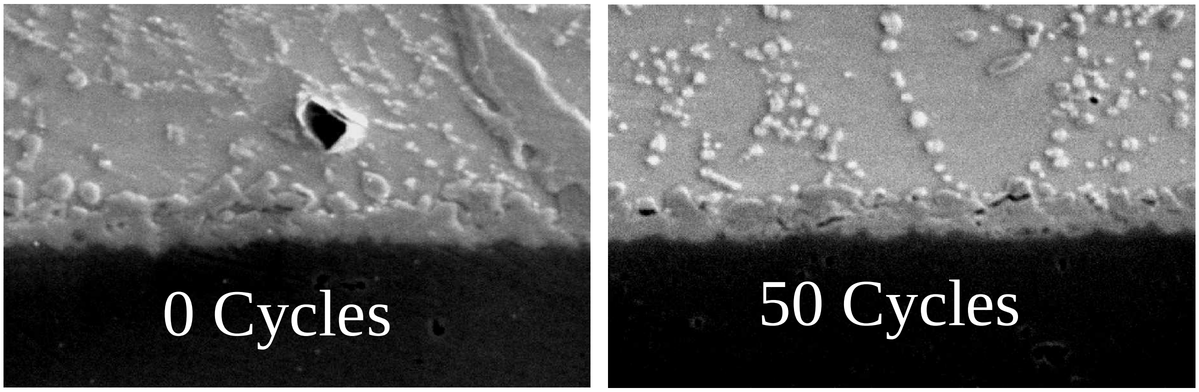


Figure 5.16: Intermetallic growth after 50 cycles, -40 to 125 C preconditioning in SAC405, 27 mm BGA, solder interconnects.

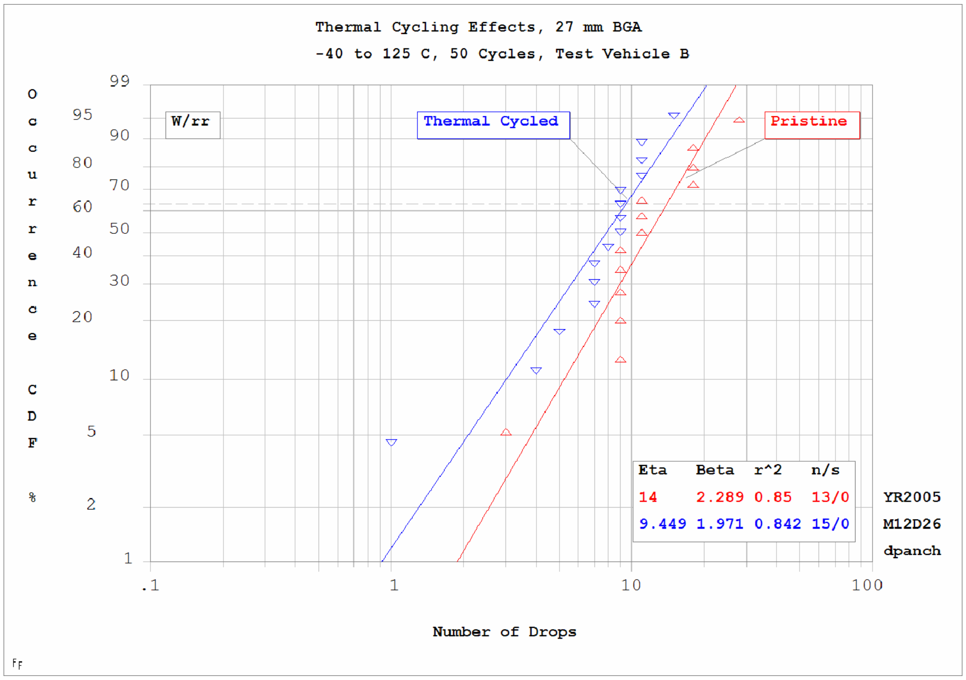


Figure 5.17: Weibull Data for Drops-to-Failure for 27mm Ball-Grid Arrays with 95.5Sn4.0Ag0.5Cu Solder Interconnects.

5.9 Summary and Conclusions

In this dissertation, a methodology for development of the damage equivalency for area-array packaging architectures exposed to single and sequential thermo-mechanical and transient shock stresses has been developed. Wavelet decomposition which have been used extensively in several areas including data and image processing, geophysics, power signal studies, meteorological studies, speech recognition, medicine, and motor vibration, have been applied to analysis of transient-response of electronics under shock and vibration. Wavelets have been used to avoid the problem of fixed time-frequency window with windowed Fourier transforms, which causes over-representation of the high-frequency components and an under-representation of the low-frequency components of a transient drop-impact signal. The need of different resolutions is required to analyze a variety of signal components of different duration has been addressed by using wavelet transforms. The Daubechies D_{10} wavelet with 12-level decomposition has been used to analyze non-stationary transient dynamic signals.

A relative damage index has been developed for prediction of the number of drops-to-failure under transient loads. The research presented attempts to address the need for techniques and damage proxies which enable the determination of damage equivalency and cumulative damage during overstress and repetitive loading for various packaging architectures. The approach is based on assembly strains, since there are experimental limitations of measuring field-quantities and their derivatives at the board-solder joint interface, primarily because of the small size of interconnects in fine-pitch ball-grid array packages.

Explicit finite element models in conjunction with the proposed approach have been used to predict survivability of fine-pitch ball-grid arrays in transient-shock and vibration. The approach has been applied to both lead-free (95.5Sn4.0Ag0.5Cu) and leaded (63Sn37Pb) ball-grid array architectures. The validation has been presented for both repeatable and non-repeatable drops.

CHAPTER 6

HIGH SPEED DIGITAL IMAGE CORRELATION FOR TRANSIENT-SHOCK RELIABILITY OF ELECTRONICS

6.1 Introduction

High speed photography has been used to measure deformation and strain in sheet metal forming analysis, automotive crash testing, rail vehicle safety [Kirpatrick 2001], air-plane safety [Marzougui 1999], modal analysis of blades, disks, shearography which involves laser NDT for rapid honeycomb delamination tests, dynamic fracture phenomenon, tire tests, rotating components, exhaust manifolds, split Hopkinson bar tests, package integrity or hermiticity (MIL-STD-883) tests. High-speed cameras measure impact speed, force, and deformation due to shock, and thermal loading. It is also used for quantitative evaluation of in-plane deformation characteristics of geo-materials [Watanabe 2005], and in medical fields to assess local failure of bone by implementing mechanical compression testing of bone samples [Thurner 2005].

Previously, the measurement of derivatives of field quantities, such as strains, was limited to a specific physical locations or discrete target points in an electronic structure. It was not feasible to extract data at a very large number of locations by using discrete targets because of the time-consuming process.

Techniques such as Moiré Interferometry is an option to get the overall deformation contour, but it is often time consuming and involves expensive grates. Digital Image Correlation (DIC) is the state-of-art technique which super-cedes the later as it is less time consuming. The sample preparation is simple and quick. The test specimens are speckle painted and transient deformation recorded with the help of high-speed cameras, to enable the measurement of full-field strains. Feasibility of this technique has been explored in this dissertation and has been experimented on electronic assemblies under free drop and constrained drop for the first time.

In electronics industry, digital image correlation has been used to study the stresses in solder interconnects of BGA packages under thermal loading [Zhou 2001, Yogel 2001, Rajendra 2002, Zhang 2004, Zhang 2005, Xu 2006, Bieler 2006, Sun 2006], material characterization under thermal loading [Srinivasan 2005, Gu 2006], parametric study of speckle size [Gu 2006], dynamic testing to study deformation for flexible bodies [Reu 2006], material characterization at high strain rate [Tiwari 2005], stresses and strain in flip-chip die under thermal loading [Kehoe 2006], fracture toughness of underfill/chip interface due to temperature and aging conditions [Song 2006]. In this dissertation, deformation kinematics has been measured with the help of ultra high-speed data acquisition and video systems. Various test board assemblies have been drop tested in 00 JEDEC and 900 vertical drop orientations. Continuity of the daisy chained packages is measured for all the packages during the transient event. Experimental data has been correlated to the finite element models. Explicit finite element models have been used to assess reliability and performance of the electronic boards. Failure modes have been studied for various packaging architectures including flex-BGA and Tarray BGA. Influence of thermal cycling, board surface finish (ImSn, ImAg, ENIG), and drop severity has been studied on the development of failure modes. Weibull plots are used for reliability prediction of the fine-pitch packages.

Statistical pattern recognition method (SPR) has been implemented to quantify the relative performance based on strain histories obtained from DIC technique. SPR has been used to study the effect of damage progression for various packaging architectures. SPR refers to the study of algorithms that recognize patterns in data and contains various sub-disciples like discriminant analysis, feature extraction, error estimation, and cluster analysis. Some important application areas are image analysis, character recognition and industrial inspection. Confidence value of the transient-strain response computed using Wavelet Packet Energy Decomposition and Mahalanobis distance approach have been investigated.

A methodology has been developed to identify the damage progression versus number of drops by studying the transient strain history of electronic assemblies from digital image correlation in conjunction with statistical pattern recognition. Manifestation of damage has been studied through analysis of failure modes and correlation with degradation in confidence value. The development of a statistical-pattern recognition based damage proxies has been investigated to establish a method for identification of impending failure. The damage proxies developed in this dissertation can be used on strain response from simulations or from experimental data in controlled drop or shock tests. Damage proxies developed provide relatively objective and quantitative failure definitions that allow for variation in orientation, component location, in addition to load history. Damage proxies are scalable and allow for identification of impending failure in product level applications. Digital image correlation technique has been used to investigate dynamic degradation due to drop, thermal aging, and thermal cycling. The damage accumulation due to progressive drop has been studied. In addition, the effect of thermal stresses has been studied by subjecting two sets of test boards to thermal cycling from -40°C to +125° C for 25 cycles, and thermal aging for 100 hrs at 125° C respectively.

6.2 Test Vehicle

The test vehicles used in the study includes, test board-A, B, C, D, and E. Test boards A, B and E have identical size: FR-4 with dimensions of 8" x 5.5" x 0.06" thick. Test board-E is populated with three different packages: 17mm, 256 I/O PBGA, 18mm, 192 I/O CABGA and 6 mm, 56 I/O CABGA. Test board-A is a bare board and Test board-B is populated with five packages which include, two 10mm, 144 I/O BGA, 16mm, two 16mm, 280 I/O BGA and one 6 mm, 56 I/O package on one side of the printed circuit board. Test board-D includes 8mm flex-substrate chip scale packages, 0.5mm pitch, 132 I/O. Each board has 10 CSP locations on one side of the board only. Test board-C includes, 15mm CSP, 16mm C2BGA, 27mm BGA, and PQFN. For test boards A, B and E, lead-free solder balls 95.5Sn4.0Ag0.5Cu have been studied (Table 6.1, Table 6.2, and Table 6.3).

Table 6.1: Package Architecture of 6mm, 10mm, 14 mm BGAs.

	6mm, 56 I/O CABGA	10 mm, 144 I/O BGA	14 mm, 192 I/O CABGA
Ball Count	56	144	192
Ball Pitch	0.5 mm	0.8 mm	0.8
Die Size	4 mm	7 mm	6.35 mm
Substrate Thickness	0.36 mm	0.36 mm	0.36 mm
Substrate Pad Dia.	0.28 mm	0.34 mm	0.34 mm
Substrate Pad Type	NSMD	NSMD	NSMD
Ball Diameter	0.32 mm	0.48 mm	0.48 mm

Table 6.2: Package Architecture of 16mm, 17 mm BGAs.

	16 mm, 280 I/O BGA	17 mm, 256 I/O PBGA
Ball Count	280	256
Ball Pitch	0.8 mm	1 mm
Die Size	10 mm	6.35 mm
Substrate Thickness	0.36 mm	0.36 mm
Substrate Pad Dia.	0.34 mm	0.34 mm
Substrate Pad Type	NSMD	NSMD
Ball Diameter	0.48 mm	0.5 mm

Table 6.3: Package Architecture of 32 I/O, 44 I/O MLFs.

	7 mm, 32 I/O MLF	7 mm, 44 I/O MLF
Lead Count	32	44
Pitch	0.5 mm	0.65 mm
Die Size	2.5 mm	3.25 mm
Substrate Thickness	0.9 mm	0.9 mm
Substrate Pad Thickness	0.1 mm	0.1 mm
Substrate Pad Type	NSMD	NSMD

Three different lead-free surface finishes were studied, viz. ImAg, ENIG and ImSn for test board-B. Strain gages were used to measure longitudinal strain. Gages were placed on the populated boards on the package side and on the board side and repeated readings were taken to determine repeatability of the controlled drop orientation. The 0-degree drop was done in the JEDEC configuration, involving a 1500g, 0.5 ms pulse. In addition, the drop height was varied to obtain shock pulses of various magnitudes, in addition to the 1500g, 0.5 millisecond duration, half-sine input pulse. The 90-degree drop was a free drop with a weight attached to the drop of the circuit-board assembly to simulate the weight of the battery and the components in a typical product board. Repeatability of drop orientation is critical to measuring a repeatable response. Small variations in the drop orientation can produce vastly varying transient-dynamic board responses. Repeatability of the test-set up was characterized (Figure 6.1).

All the packages used in the test configuration were daisy-chained. In all cases, multiple boards were tested in each test-configuration. Test boards were exposed to sequential stresses of thermal cycling followed by shock impact to determine the effect of cumulative damage on the interconnect reliability. Thermo-mechanical cycling included exposure to -40 to 125o C for 25 cycles. The thermal cycle duration is 90 minutes with 25 minutes ramps between temperature extremes and 45 minutes dwells at each temperature extreme.

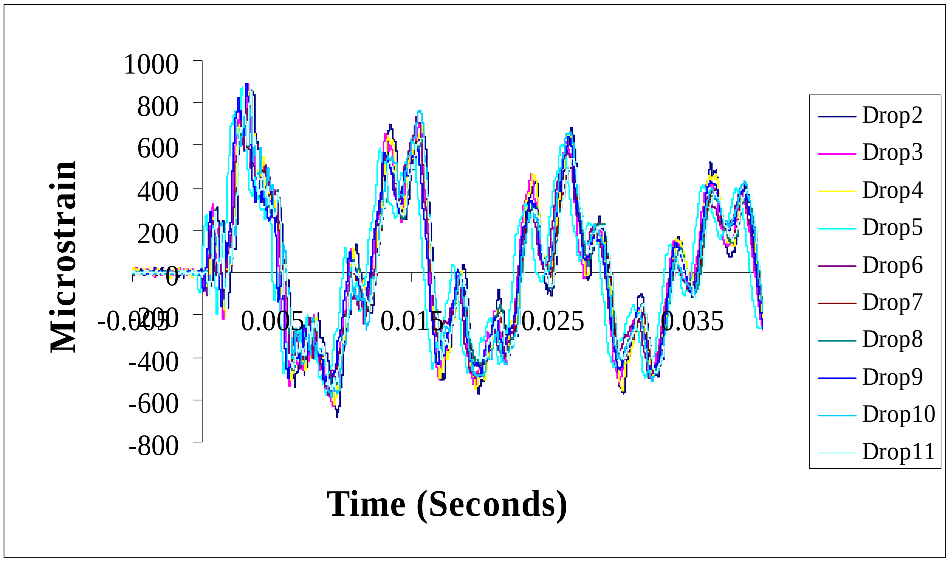


Figure 6.1: Strain Repeatability for Test-Board A.

6.3 Detection Of Damage Progression

The test boards were subjected to a controlled drop. Repeatability of drop orientation is critical to measuring a repeatable response. Small variations in the drop orientation can produce vastly varying transient-dynamic board responses. Significant effort was invested in developing a repeatable drop set-up. The drop height was varied to obtain shock pulses of various magnitudes, in addition to the 1500 Gs, 0.5 millisecond duration, half-sine input pulse. Component locations on the test boards were instrumented with strain sensors (Figure 6.3). Strain and continuity data was acquired during the drop event using a high-speed data acquisition system at 2.5 to 5 million samples per second.

The drop-event was simultaneously monitored with ultra high-speed video camera operating at 30,000 frames per second. Targets were mounted on the edge of the board to allow high-speed measurement of relative displacement during drop.

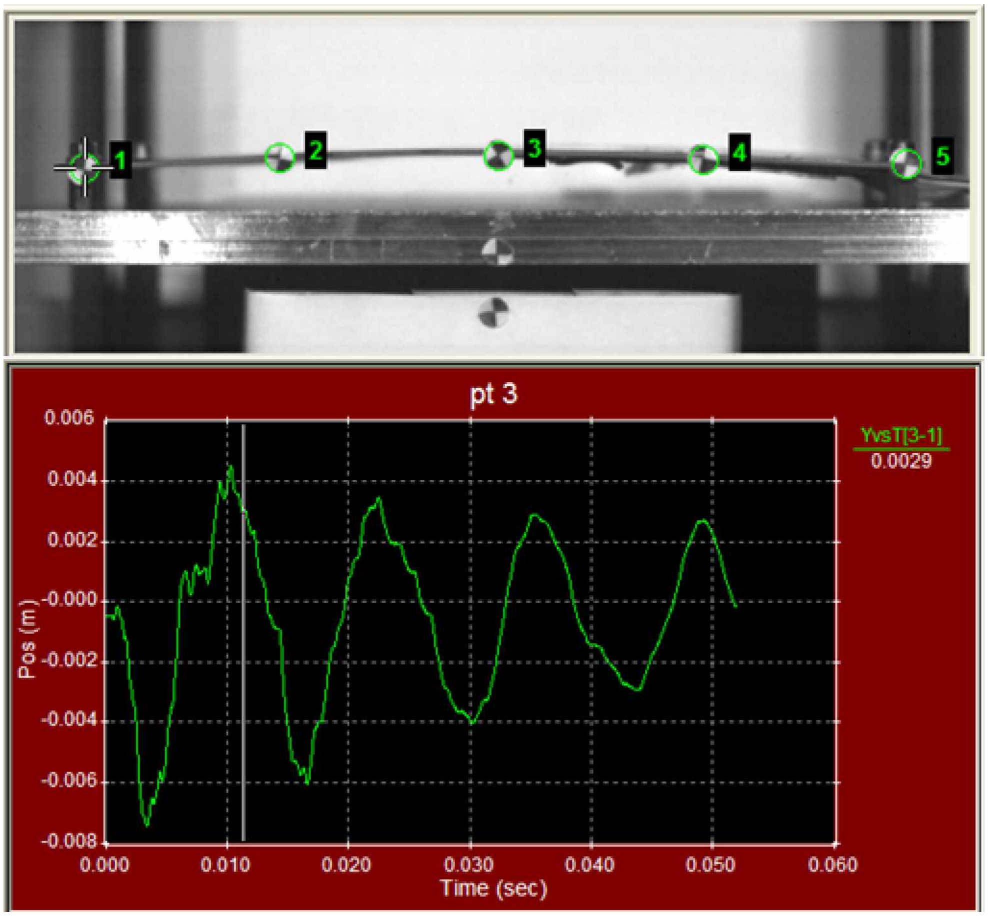


Figure 6.2: Relative Displacement of Test Board B (JEDEC Drop)

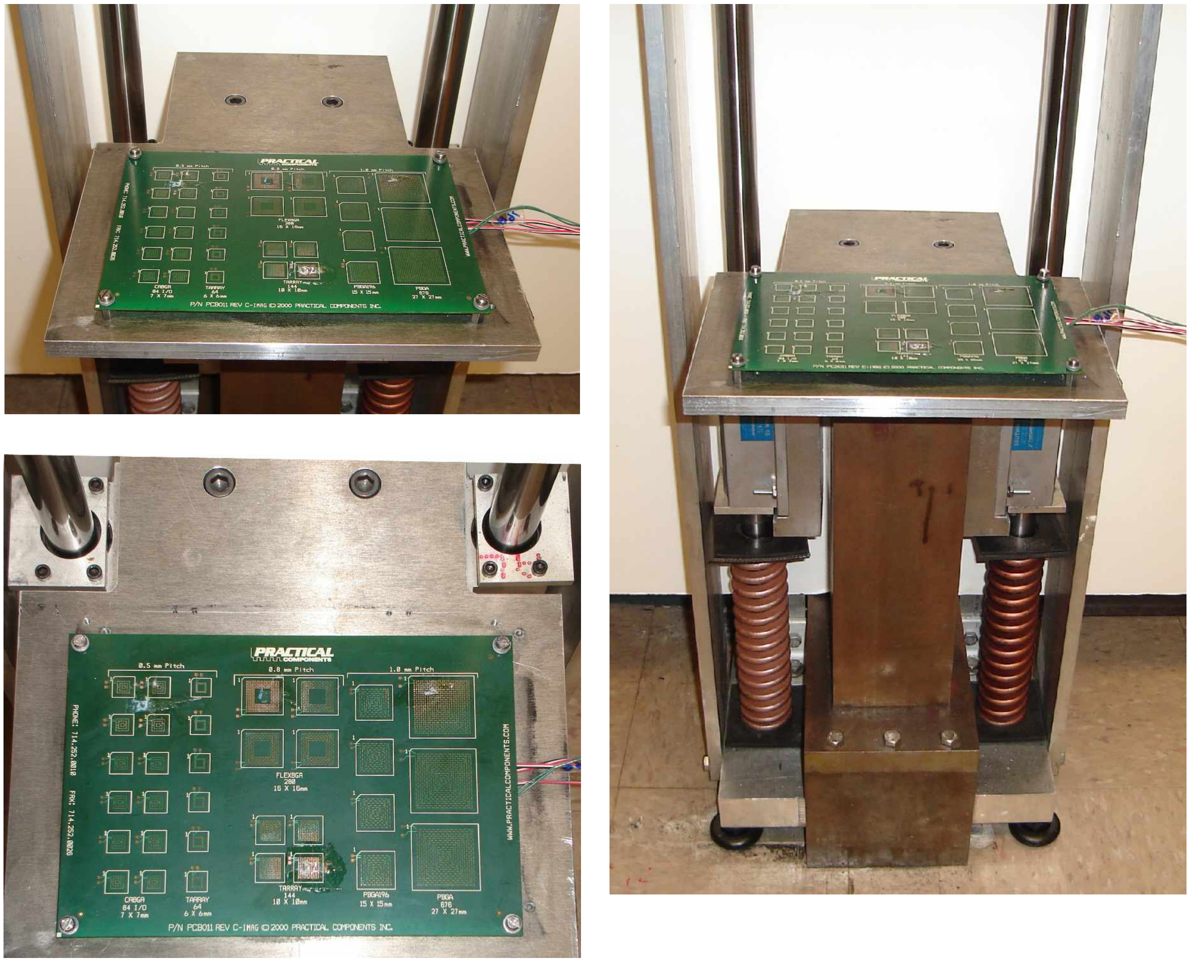


Figure 6.3: Experimental Set-up for Controlled Drop (Test board B).

Strain, displacement, orientation angle, velocity, acceleration, and continuity data has been acquired simultaneously. An image tracking software was used to quantitatively measure displacements during the drop event. Figure 6.2 shows a typical relative displacement plot measured during the drop event. The position of the vertical line in the plot represents the present location of the board (i.e. just prior to impact in this case) in the plot with “pos (m)” as the ordinate axis. The plot trace subsequent to the white scan is the relative displacement of the board targets w.r.t. to the specified reference. Figure 6.3 shows the board instrumentation for strain and relative displacement during horizontal JEDEC drop. In addition to relative displacement, velocity, and acceleration of the board prior to impact was measured. This additional step was necessary since, the boards were subjected to a controlled drop, in order to reduce variability in drop orientation.

Figure 6.4 shows the package-strain history during JEDEC drop-shock for 16mm, 280 I/O package on Test board B. Failure in the device has been identified as an increase in voltage drop. Different locations on the test board exhibit different strain histories during the same drop and different number of drops to failure. However, the strain histories are very consistent and repeatable at the same component location on the test board for various drops. The strain history is also very repeatable for the same component location across various test boards.

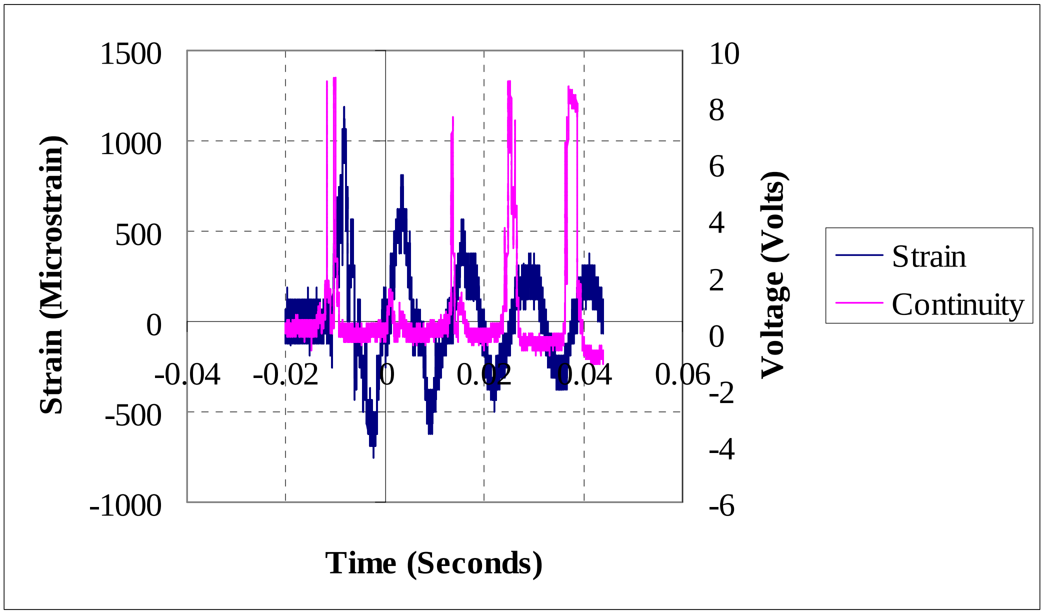


Figure 6.4: Package Strain and continuity transient history in JEDEC drop-shock, for Test board B

6.4 Digital Image Correlation

In electronics industry, digital image correlation has been used to study the stresses in solder interconnects of BGA packages under thermal loading [Zhou 2001, Yogel 2001, Rajendra 2002, Zhang 2004, Zhang 2005, Xu 2006, Bieler 2006, Sun 2006], material characterization under thermal loading [Srinivasan 2005, Gu 2006], parametric study of speckle size [Gu 2006], dynamic testing to study deformation for flexible bodies [Reu 2006], material characterization at high strain rate [Tiwari 2005], stresses and strain in flip-chip die under thermal loading [Kehoe 2006], fracture toughness of underfill/chip interface due to temperature and aging conditions [Song 2006]. However, the application of this technique to study deformation and strain for transient event such as shock and drop of the PCB assembly is largely unexplored.

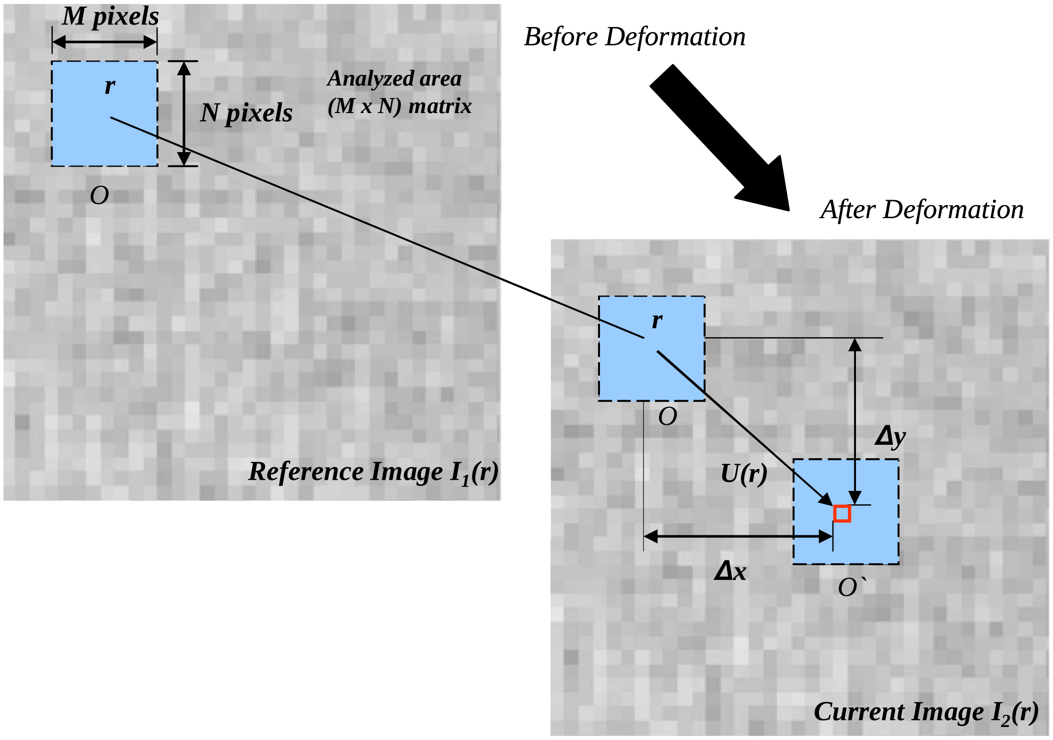


Figure 6.5: Digital Image Correlation Principle

Data is scarce for the behavior of the printed circuit board transient dynamics in shock, which is a major reliability issue to study the failures at the solder interconnects in portable electronics. Board-level reliability of the electronic assembly has never been studied using this technique when subjected to drop in vertical and JEDEC orientations. Tracking of a geometric point before and after deformation gives the displacement field [Zhou 2001, Amodio 2003, Srinivasan 2005, Kehoe 2006]. The tracking is achieved using image processing of speckle pattern on the specimen surface. Speckle pattern of the image before and after deformation are captured using high speed camera and digitized into digital images (Figure 6.5).

The two images are called reference image I1 (r) and the deformed image I2 (r) respectively, which are related as follows:

$$I_2(r) = I_1[r - U(r)] \tag{6.1}$$

$$I_1(r) = I_2[r + U(r)] \tag{6.2}$$

Where U(r) is the displacement vector at pixel r = (x, y)T . The difference of the positions of the current pixel and the reference pixel gives the in-plane displacement U(r) of this reference pixel. Full-field in-plane displacement can thus be found out by changing the reference pixel and following the same procedure described above. A subimage around a reference pixel O in the reference image is then compared with the subimages corresponding to different pixels in the current image using a predefined correlation function to describe the difference of the two digital subimages. Three typical correlation functions are defined as follows: [Zhou 2001]

Absolute difference:

$$C_A(r') = 1 - \frac{\iint_\Omega \left| I_2(r + r') - I_1(r) \right| dr}{\iint_\Omega I_1(r) dr} \tag{6.3}$$

Least square:

$$C_L(r') = 1 - \frac{\iint_\Omega [I_2(r + r') - I_1(r)]^2 dr}{\iint_\Omega I_1^{\ 2}(r) dr} \tag{6.4}$$

and Cross-Correlation:

$$C_C(r') = 1 - \frac{\iint_\Omega I_1(r) I_2(r + r') dr}{\left[\iint_\Omega I_1^{\ 2}(r) dr \iint_\Omega I_2^{\ 2}(r + r') dr\right]^{1/2}} \tag{6.5}$$

where Ω (M x N) is the area of the subimage around reference pixel r, r` is the current pixel, CA(r`) is the current absolute correlation function, CL(r`) is the current least square correlation function, and CC(r`) is the current cross-correlation function. The cross-correlation functions provide the correspondence between matching subsets in images of the undeformed and deformed states. It is an iterative spatial-domain cross-correlation method. This method maximizes the cross-correlation coefficient between a subset in the reference image I1 and the deformed image I2. In practice, the absolute and least square correlation functions require less computation. They assume constant brightness. In order to handle illumination changes, Normalized cross-correlation is used, which is more computationally demanding. Correlation functions determine the current pixel O' from the reference pixel O, by matching the two subimages.

6.5 Experimental Set-Up

Strains were measured using two techniques including digital image correlation in conjunction with ultra-high speed video and strain gages in conjunction with high-speed data-acquisition systems. Strain gages were mounted at different locations on the test board on both the package and the board side. Package continuity was monitored during the transient-dynamic shock event. Figure 6.6 shows the speckle pattern on the four boards. Effort has been made to get a close and consistent speckle patterns on all the test boards. It has been shown in the past that speckle size and distribution affects accuracy [Zhou 2001, Gu 2006]. The speckle pattern and strain gages are shown for the test boards A, B, C and D in the Figure 6.7.

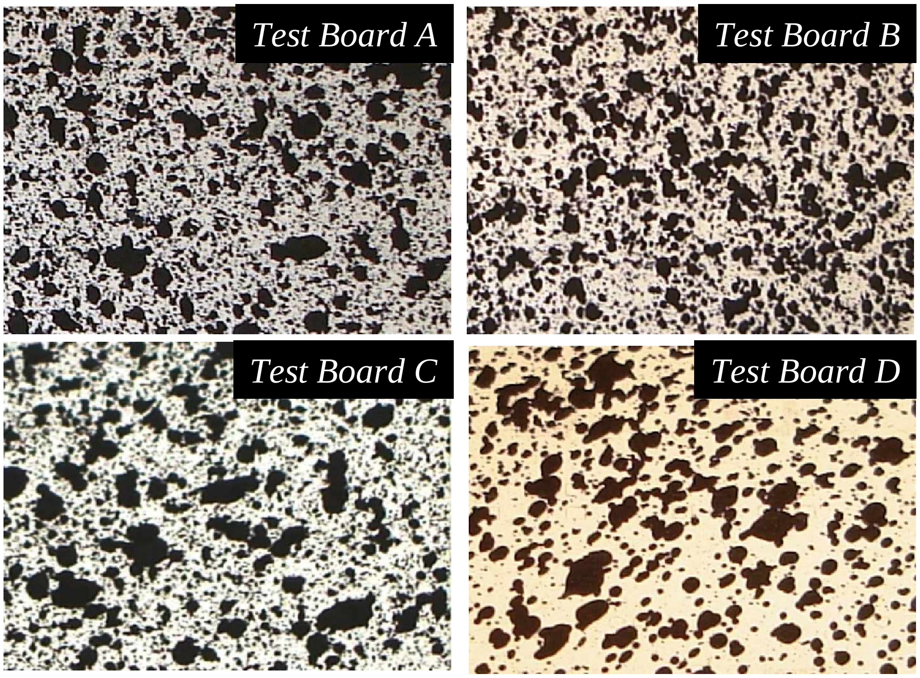


Figure 6.6: Speckle Pattern for various test boards

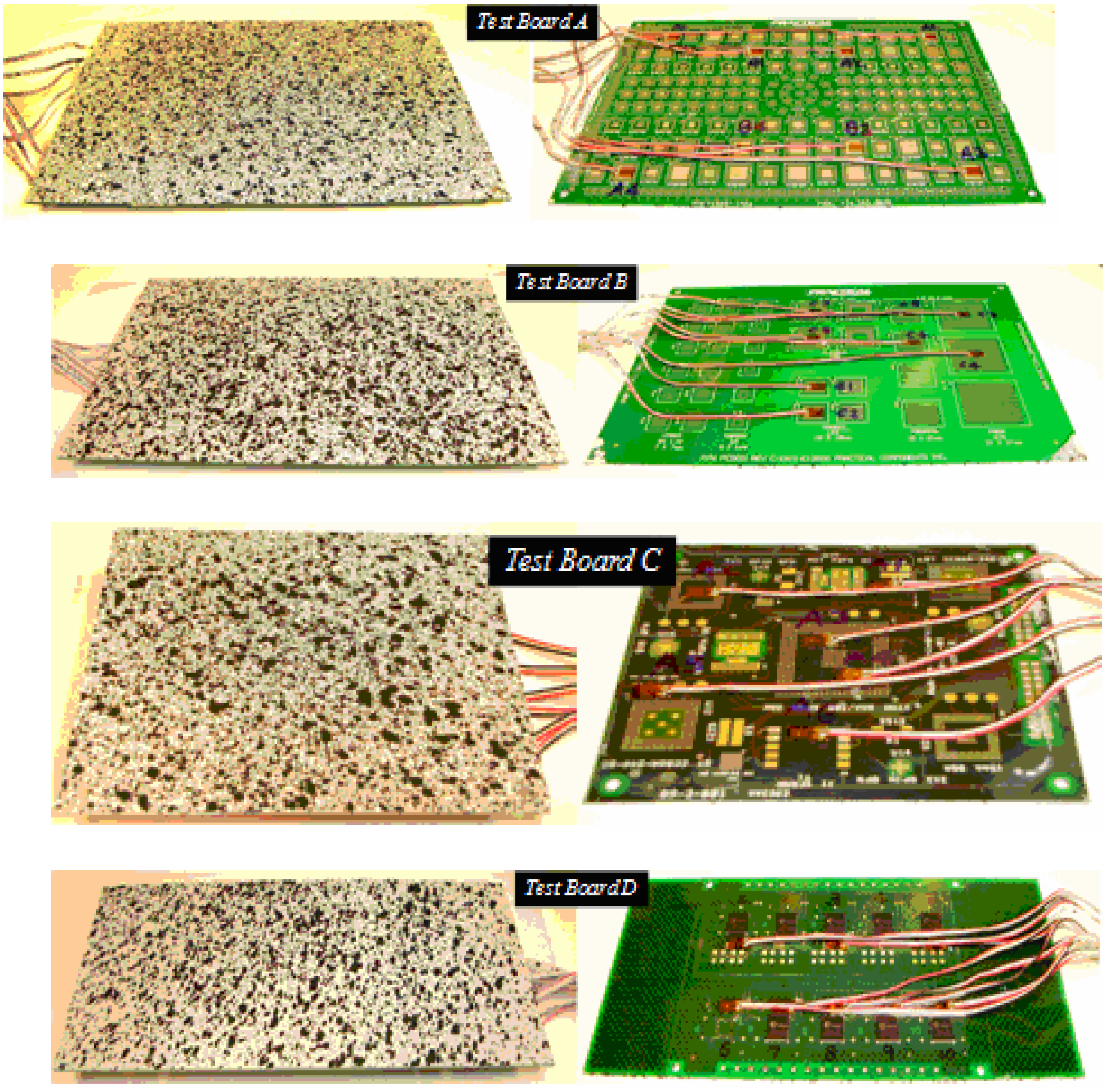


Figure 6.7: Speckle Pattern and Strain Gages for Test Boards A-D

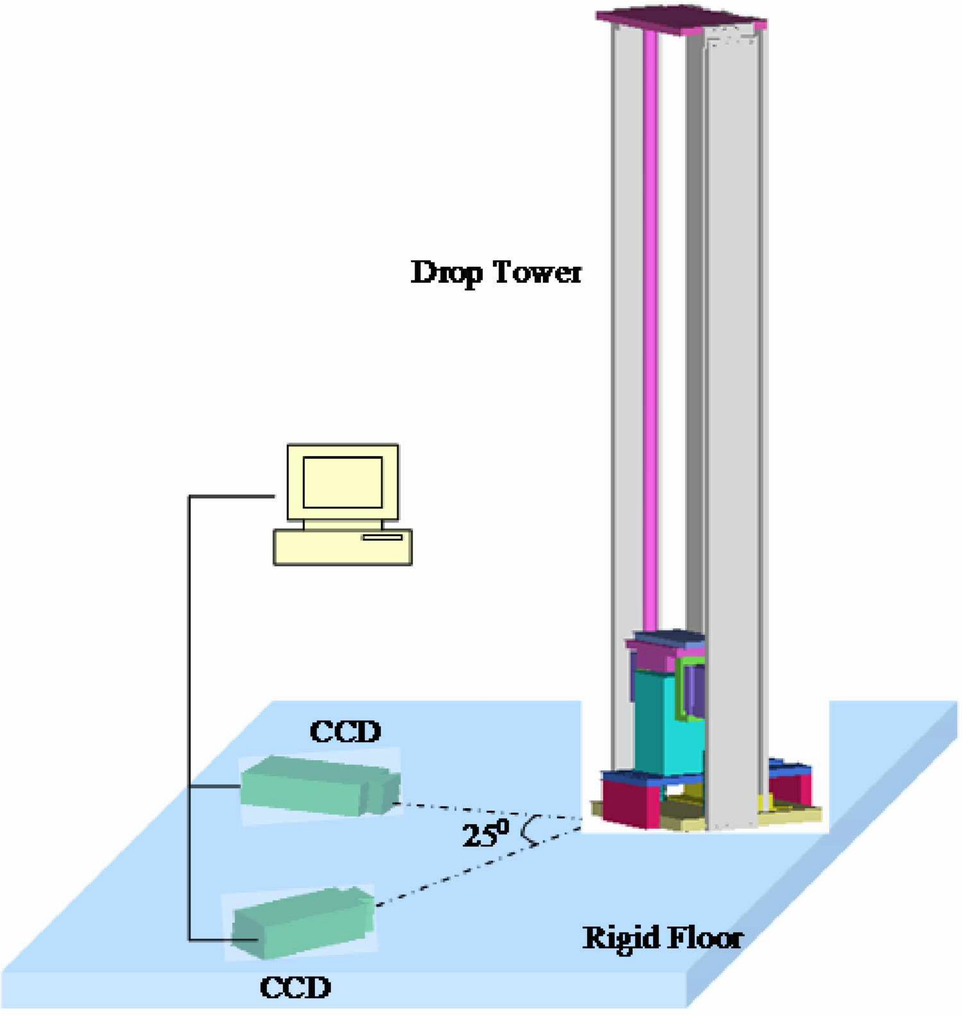


Figure 6.8: Vertical Drop Test Setup

The experimental setup consists of two cameras rested on the rigid floor as shown in Figure 6.8. The test boards are dropped from 3 ft height in vertical orientation. A mass of steel weighing 31.8 gms is attached on the top edge of the board to accelerate the experiment. The test board is attached to the fixture on the drop tower with the help of fishing lines. Test board falls freely from a predefined height and hits the rigid floor. This event is captured by two high speed cameras at 40,000 fps. The two cameras make an angle of 25 degrees with each other when facing the speckled test board. [Gu 2006] 200, [Helm 1996] 600. It was observed that an angle in the range of 20-40 degrees gave good results. The cameras are calibrated before the start of the experiment. Calibration involves positioning the two cameras at a certain angle in front of the calibration grid (target). Figure 6.9 shows the picture of the target at various positions during calibration. The images of the target are roughly centered in the field of view for each camera. Exposure from each camera is approximately kept same while capturing target images. Target consists of 9x9 grid points with 15 mm pitch. The two cameras are synced together with one camera as master and the other as slave. A series of images are taken from both the cameras. Approximately 15-20 images per camera are sufficient for calibration. Both the cameras are triggered simultaneously and the images are recorded and analyzed using software from Correlated Solutions, Inc.

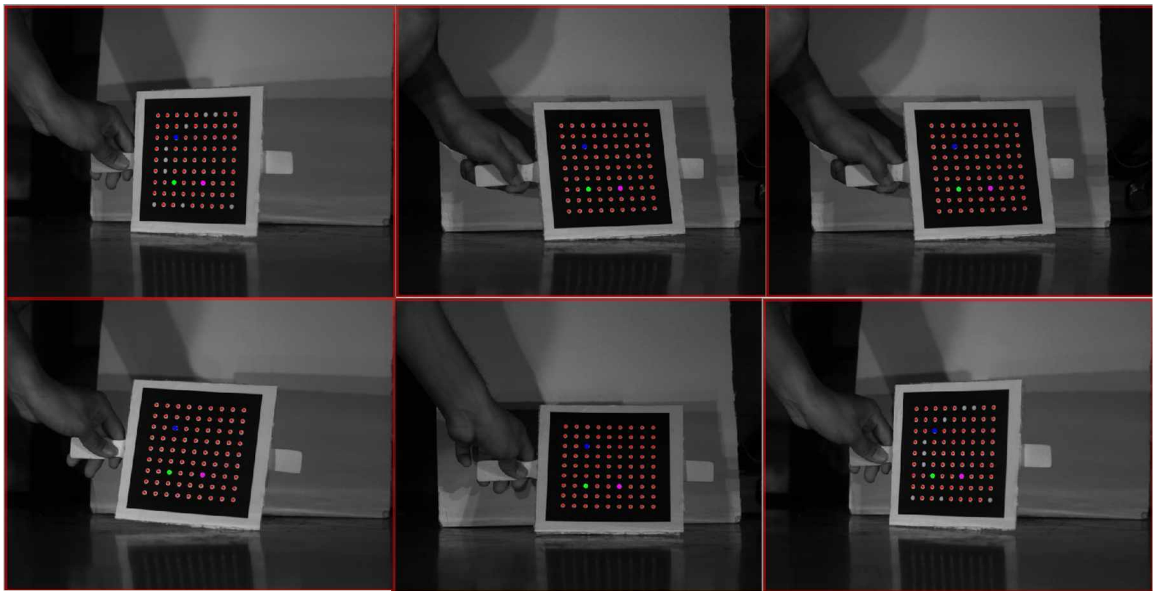
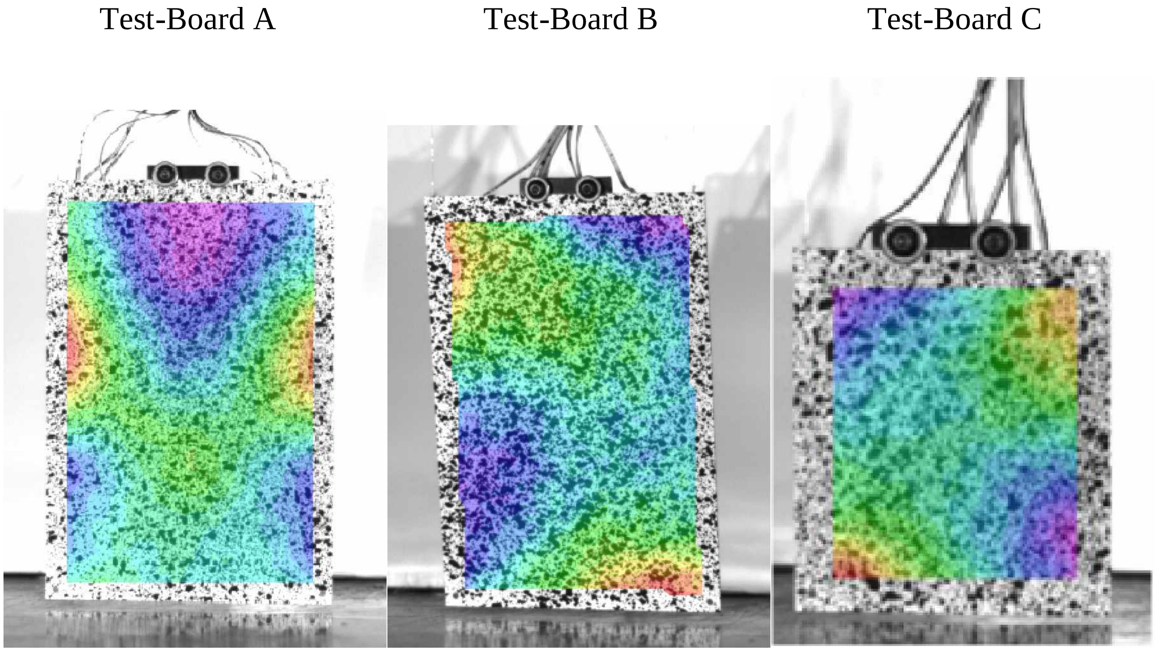


Figure 6.9: Calibration

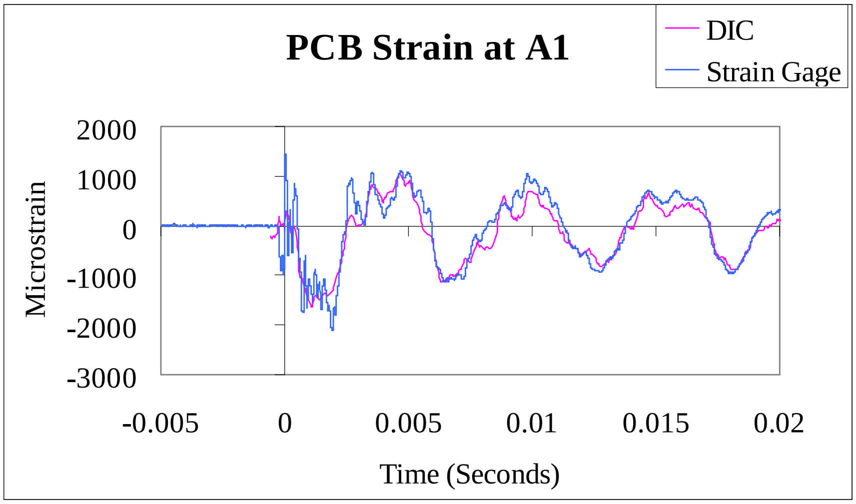


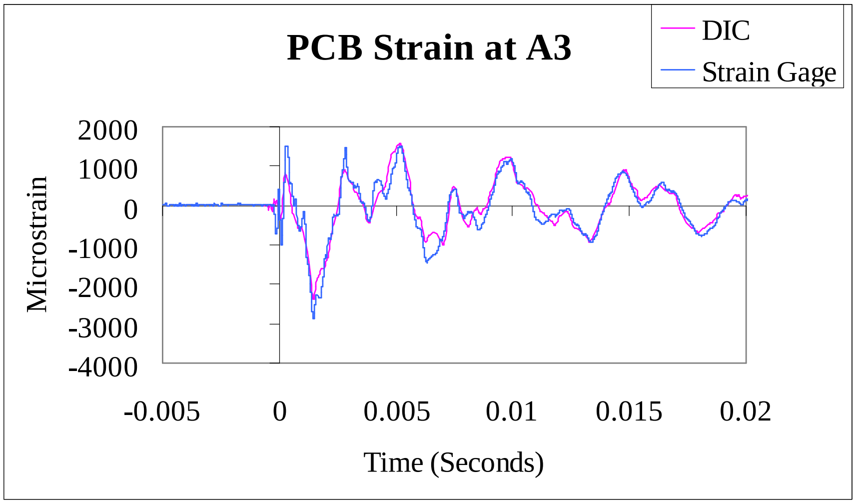
Test-Board A

Test-Board B

Test-Board C

Figure 6.10: 2-D Strain Contour.





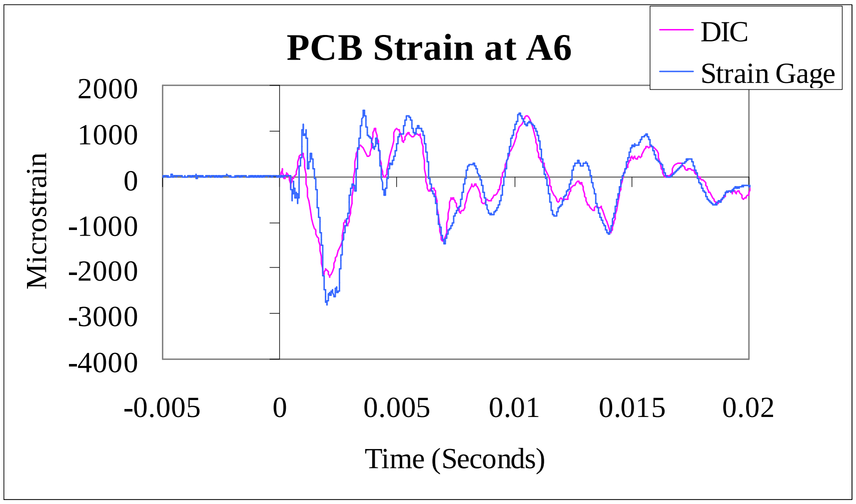


Figure 6.11: Test Board-C Strain Correlation (Vertical Drop)

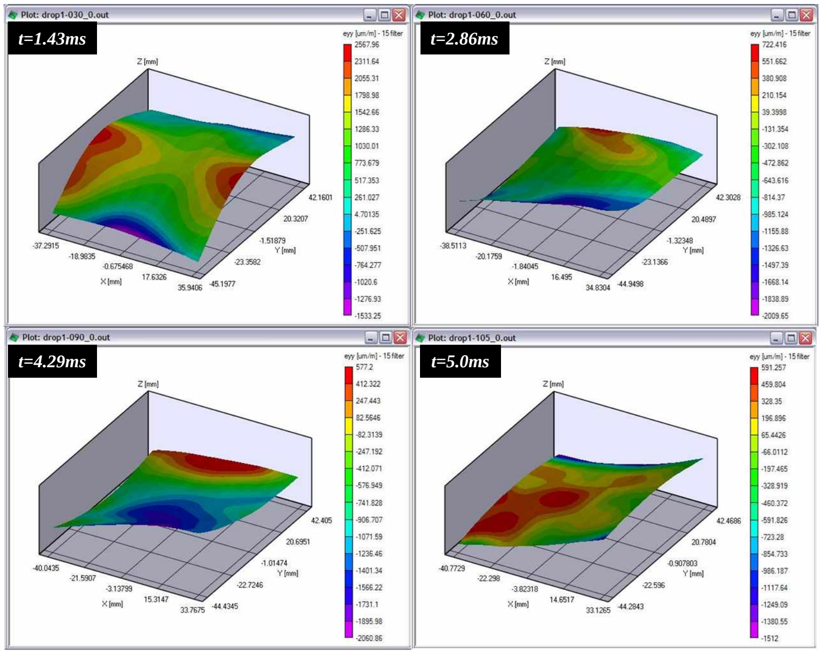


Figure 6.12: 3D contour of strain in the longitudinal direction from DIC for Test-Board C, 90-degree Vertical Drop.

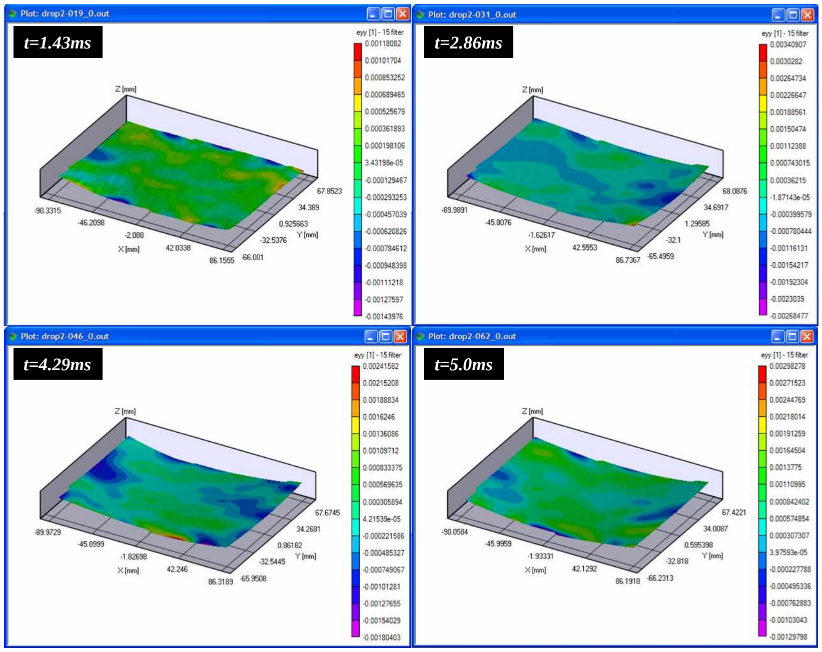


Figure 6.13: 3D contour of strain in the longitudinal direction from DIC for Test-Board A, 0-degree JEDEC Drop.

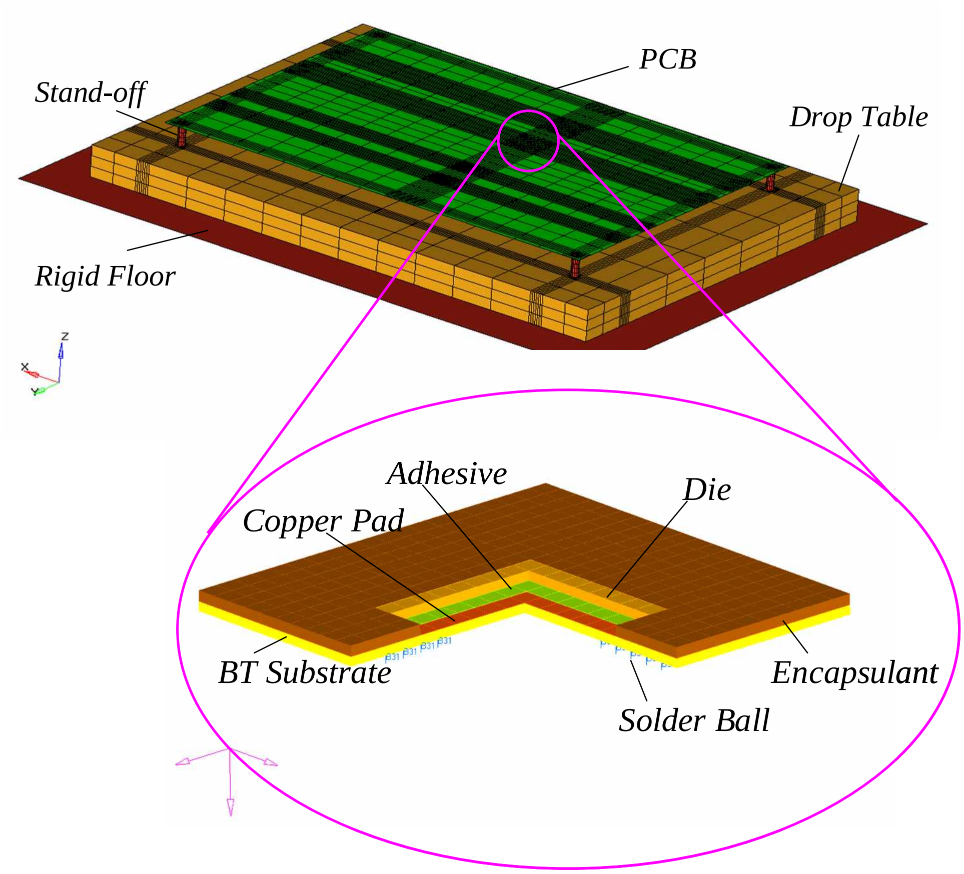
6.6 Correlation of Speckle Data with Strain Gage Data

Strain from DIC technique is correlated with the strain from strain gages at various locations on the test board C (Figure 6.11). Figure 6.10 shows the 2D strain contour of test boards A, B, C when dropped in vertical orientation. Drop results for vertical drop orientation from 3 ft height are shown in Figure 6.11. The strains are correlated from strain gage sensors and DIC at location A1, A3, and A6 on the Test Board-C. DIC results obtained were accurate and consistent with the strain gage sensors for vertical drop. Figure 6.12 and Figure 6.13 show the 3-D contour of strain in the longitudinal direction from DIC at different time instants for two-different test boards in 0-degree JEDEC configuration and 90-degree vertical configuration.

6.7 Explicit Finite Element Models

Transient dynamic deformation of the test boards was modeled using Explicit Finite Element Models. The effect of board drop orientation on global response of printed circuit assembly has been predicted and correlated with digital image correlation measurements.

Previously, the JEDEC JESD22-B111 has been modeled has been modeled using the input-G method [Tee 2004]. In this dissertation, the use of explicit finite elements has been investigated. The use of explicit finite elements enables the calculation of response history using step-by-step integration in time without changing the form of dynamic equations as done in modal methods. The modeling effort has focused on prediction of transient dynamic drop response using explicit finite-element theory with reduced



Test Board B (Zero-Degree Configuration)

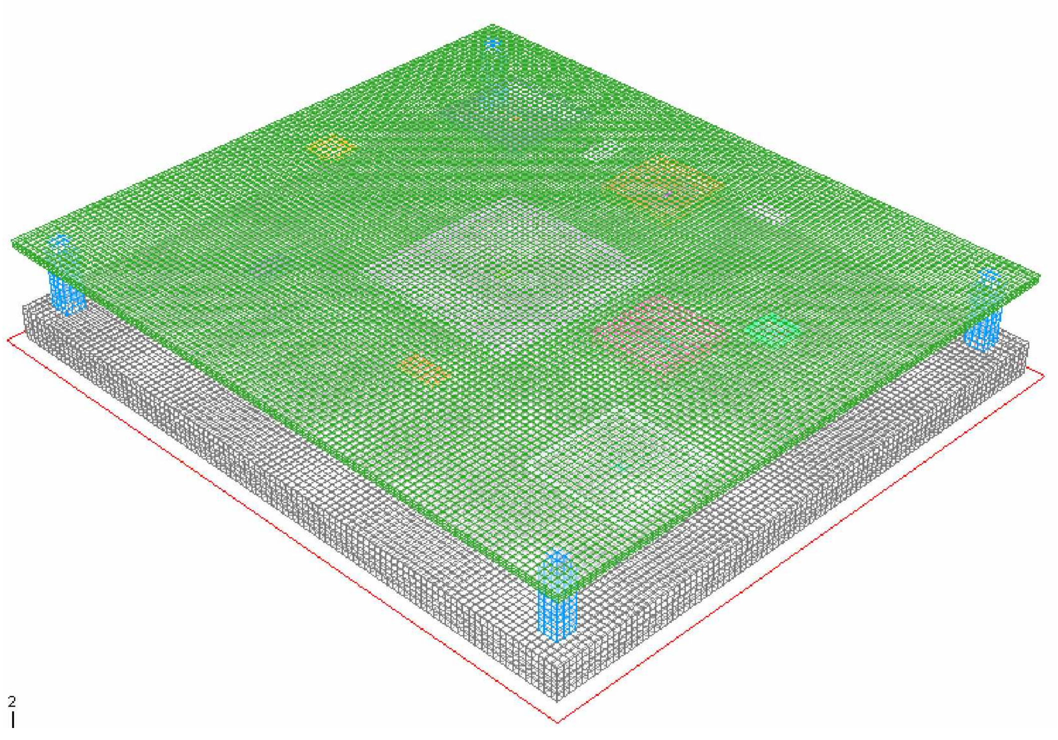
Figure 6.14: Explicit-Finite Element Model for Test Board-B in JEDEC Configuration.

integration elements. An explicit algorithm uses a difference expression of the general form, "n" represents the time-step. The equation contains only historical information on the right hand side. The difference expression is combined with the equation of motion at time step "n" for the simulation.

$$\{D\}_{n+1} = f\left[\{D\}_n, \{\dot{D}\}_n, \{\ddot{D}\}_n, \{D\}_{n-1}, \ldots.\right] \tag{6.6}$$

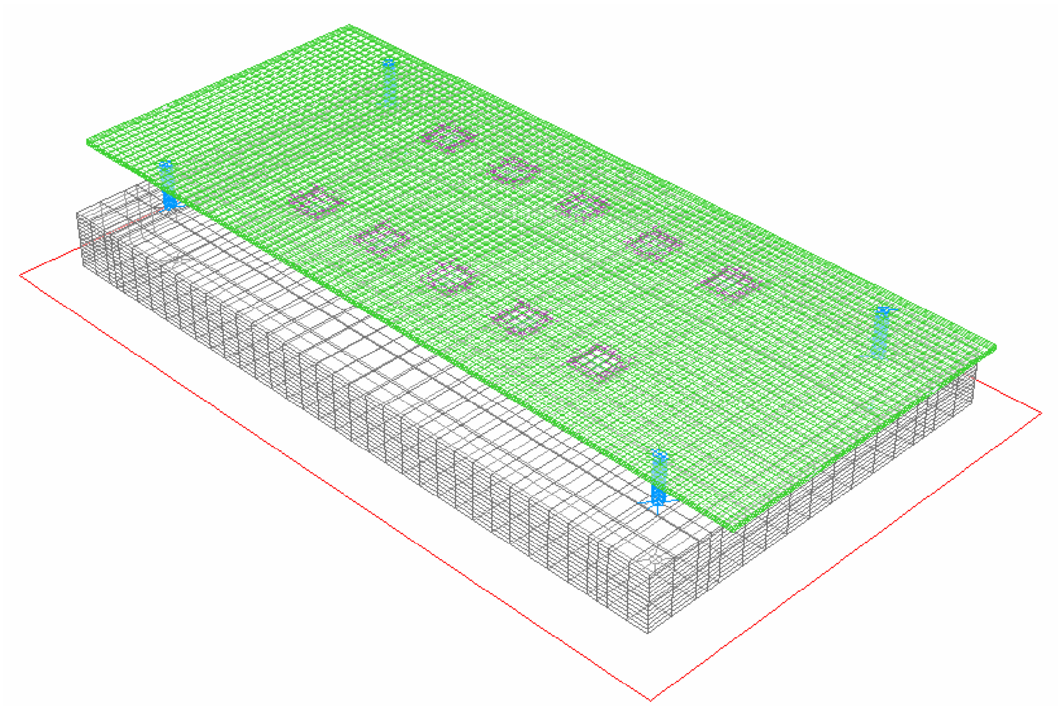
where {D} is the d.o.f. vector, the "." on top represents time differentiation, and subscript

$$\begin{aligned}&\left(\frac{1}{\Delta t^2}[M]+\frac{1}{2\Delta t}[C]\right)\{D\}_{n+1}\\&=\{R^{ext}\}_n-\{R^{int}\}_n+\frac{2}{\Delta t^2}[M]\{D\}_n-\left(\frac{1}{\Delta t^2}[M]-\frac{1}{2\Delta t}[C]\right)\{D\}_{n-1}\end{aligned} \tag{6.7}$$



Test Board C (Zero-Degree Configuration)

Figure 6.15: Explicit-Finite Element Model for Test Board-C in JEDEC Configuration



Test Board D (Zero-Degree Configuration)

Figure 6.16: Explicit-Finite Element Model for Test Board-D in JEDEC Configuration

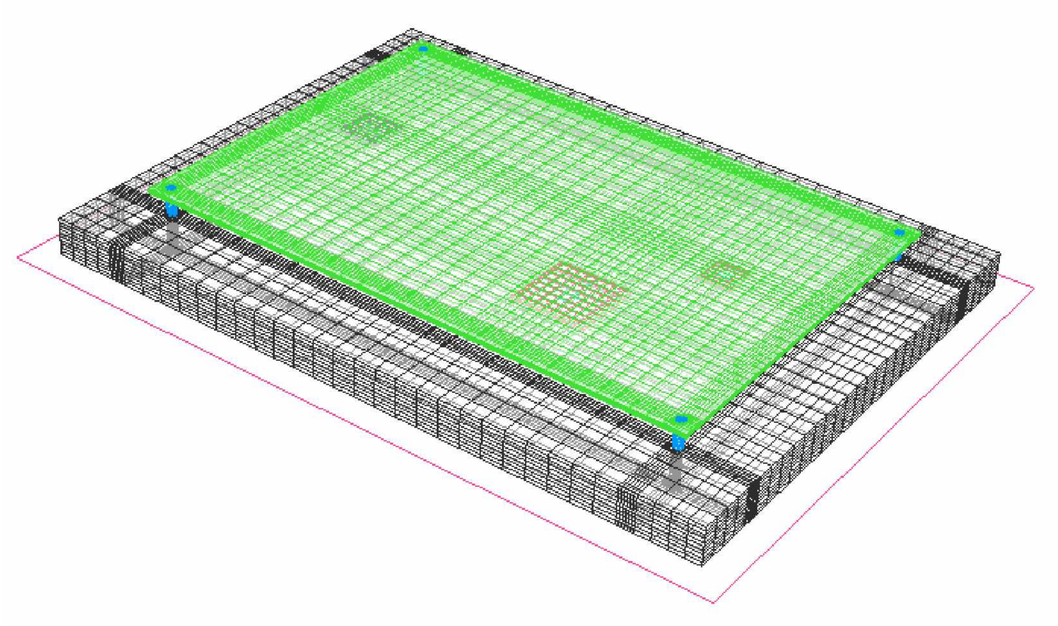
The degree of freedom vector at the n-1 time-step is given by a Taylor series,

$$\{D\}_{n-1} = \{D\}_n - \Delta t\{\dot{D}\}_n + \frac{\Delta t^2}{2}\{\ddot{D}\}_n - \frac{\Delta t^3}{6}\{\dddot{D}\}_n + \ldots$$

$$\text{for } n = 0, \qquad \{D\}_{-1} = \{D\}_0 - \Delta t\{\dot{D}\}_0 + \frac{\Delta t^2}{2}\{\ddot{D}\}_0 \qquad (6.8)$$

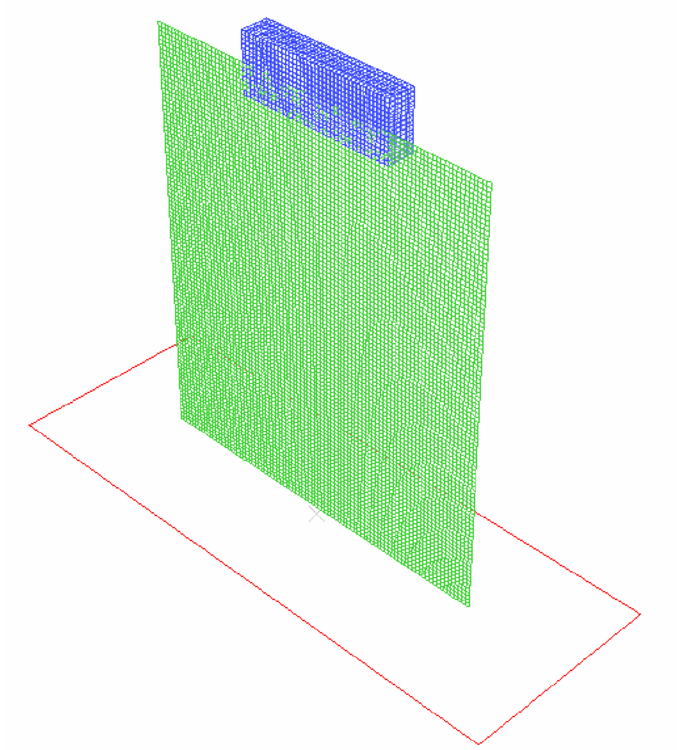
The coefficient matrix of {Dn+1} can be made diagonal using lumped mass-matrix or diagonalization of the consistent mass matrix, $[m] = \int \rho\, [N]^T [N]\, dV$ through techniques such as HRZ lumping. Therefore, {Dn+1} can be cheaply calculated for each time step.

Figure 6.14 to Figure 6.19 show the various explicit finite element models for Test Boards B, C, D, and E in both zero-degree JEDEC and 90-degree vertical drop configurations. Reduced integration elements have been used to formulate the transient event. Fewer integration points are used as compared to the implicit formulation hence it saves computational time. Shell-elements (S4R) are used to model the PCB which accounts for large strains [AbaqusTM 2006]. The solder interconnects has been modeled using three-dimensional, linear, Timoshenko-beam element (B31) elements. Three-dimensional beams have six degrees of freedom at each node including three translational and three rotational degrees of freedom. The rotational degrees-of-freedom has been constrained to model the interconnect behavior. The B31 elements allow for shear deformation. It is assumed that the strain in the beam is constant throughout the beam. Various component layers for the packages such as substrate die-adhesive, silicon die, encapsulant, copper pads have been modeled with C3D8R elements. The concrete floor has been modeled as rigid floor using R3D4 elements.



Test Board E (Zero-Degree Configuration)

Figure 6.17: Explicit-Finite Element Model for Test Board-E in JEDEC Configuration



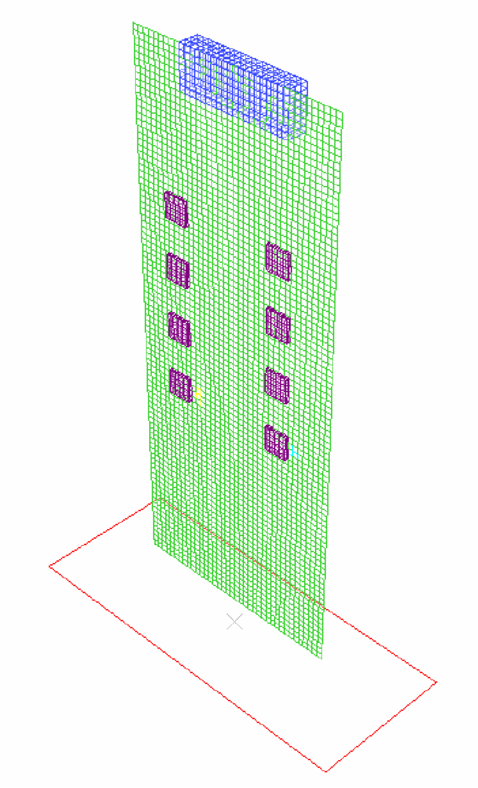
Test Board C (90° Vertical Drop)

Figure 6.18: Explicit-Finite Element Model for Test Board-C in 90-degree Vertical Drop Configuration

Reduced integration elements have been used for computational efficiency because evaluation of internal force vector, {rint}n requires the same order of quadrature as element stiffness matrix [K]. A reference node has been placed behind the rigid wall for application of constraints. Contact has been monitored between any PCB surface, CSP surface or Weight surface and only on the positive side of the floor. Node to surface contact has been used. The Gerschgorin Bound has been used to provide an estimate of highest natural frequency, ωmax, which is used for calculation of the critical time step size. For a lumped diagonal mass matrix, it may be stated as follows,

$$\omega_{\max}^{2} \leq \max_{i}\left(\frac{1}{M_{ii}}\sum_{j=1}^{n}\left|K_{ij}\right|\right) \tag{6.9}$$

where, i = 1, 2, 3,….,n, and n is the matrix order of number of degrees of freedom, K and M are the stiffness and mass matrices respectively. Node to surface contact has been employed between PCB and rigid floor. The drop orientation has been varied from 0° JEDEC drop to 90° free-drop. Linear elastic material properties were assumed for solder interconnects. Drop height required for an 1500 Gs, 0.5 millisecond duration, half-sine input pulse has been determined. An initial velocity of $\{\dot{D}\}_0$, equivalent of the required drop has been assigned to the board, components and the weight at the top edge of the board (Equation 3). The model was simulated between 6ms to 20 ms as the peak deformation and strain was observed during this period. Using beam elements for solder interconnects saved 10x of time as compared to conventional solid elements (C3D8R) for the solder balls.



Test Board D (90° Vertical Drop)

Figure 6.19: Explicit-Finite Element Model for Test Board-D in 90-degree Vertical Drop Configuration

6.8 Mass Scaling in Explicit Analysis

Dynamic formulation is based on the dynamic equilibrium equations in the current (deformed) configuration,

$$\frac{\partial \sigma_{ij}}{\partial x_j} - \rho \ddot{u}_i = 0 \qquad (6.10)$$

Where ρ is the density and $\ddot{\upsilon}_i$ is the acceleration of material particles. The Variational form resulting from the above equation can be written as,

$$\int_V \sigma_{ij}\delta\varepsilon_{ij}dV - \int_V \rho\ddot{\upsilon}_j\delta\upsilon_j dV - \int_{S_T} T_j\delta\upsilon_j dS = 0 \tag{6.11}$$

where $\delta\upsilon_j$ is the virtual displacement and T_j is the surface traction. The most significant difference of the dynamic formulation to alternative quasi-static formulations is due to the fact that it takes inertial effects into account by treating them as body forces $-\rho\ddot{\upsilon}$. The global mass matrix M is,

$$[M] = \sum_e m_e = \sum_e - \int_V \rho N^T = NdV \tag{6.12}$$

Where N are the element shape functions. The semi-discretization of Eq. (2) generally leads to,

$$[M]\ddot{\upsilon} + \{F_{int}\} = \{F_{ext}\} \tag{6.13}$$

This can be discretized in time through the utilization of finite difference formula for the acceleration,

$$\ddot{\upsilon}^i = \frac{\upsilon^{i+1} - 2\upsilon^i + \upsilon^{i-1}}{\Delta t^2} \tag{6.14}$$

In conjunction with an explicit time integration algorithm,

$$\frac{[M]}{\Delta t2}\upsilon^{n+1} = \{F^i_{ext}\} - \{F^i_{int}\} + \frac{[M]}{\Delta t2}\{2\upsilon^i - \upsilon^{i-1}\} \tag{6.15}$$

The stability of the numerical solution procedure of Eq. (6.6) requires the size of the time increment, Δt, to be less than a critical value based on the highest eigenvalue, λ_{max} in the model,

$$\Delta t \leq \frac{2}{\lambda_{max}} \approx \frac{L_e}{\sqrt{E/\rho}} \tag{6.16}$$

where ‘L_e’ characteristic length of the element and ‘E’ is the elasticity modulus of the material. A common rule to set-up the size of the time increment, Δt, is to consider the time it takes for a longitudinal wave to travel across the smallest element of the finite element mesh,

$$\Delta t \circledR \frac{L_e}{c_e} \tag{6.17}$$

Where ce is the current wave speed in element e. The above mentioned procedure gives rise to the utilization of very small time increments, Δt, in the numerical simulation. Thus, at each time step no iterations are needed to accomplish the overall solution procedure. The main advantage of the explicit dynamic formulation draws from the fact that the solution of nodal displacements can be accomplished very efficiently, without solving any equations, if the mass matrix M is diagonal. This hinges critically on the use of diagonal (lumped) mass matrices,

$$M_{ii} = \sum_j M_{jj} \tag{6.18}$$

Where all terms with $i \neq j$ is set equal to zero. This approach is widely used in sheet-metal forming analysis [Silva 2004] and transient dynamic analyses [Towashiraporn 2006]. The cost of a numerical simulation depends only on the size of the model and the number N of time increments that are required to perform the entire shock event.

Possible approaches to reduce the overall CPU time require either to increase the size of the time increments, Δt, or to reduce the total time t of the operation. The first approach known as mass scaling can be easily achieved by increasing the density of the material and thus artificially reducing the speed of the longitudinal wave. The second approach known as load factoring is generally accomplished by changing the rate of loading through an artificially increase in the velocity if the tooling as compared to the real process speed. This second approach is not allowed whenever the material is strain-rate sensitive or thermo-mechanical phenomenon are involved.

It is worth mentioning that the above-mentioned numerical strategies to reduce the CPU time must be judiciously utilized because they may cause the dynamic formulation to provide inaccurate solutions for the deformation as well as for the stress-strain distribution. It need to be ensured that parametrization by mass scaling or load factoring approaches should prevent the kinetic energy to rise above 5% if the total strain energy.

The mass of selected element sets or individual elements in Abaqus™ can be scaled that control the stable time increment. Because the explicit central difference method is used to integrate the equations in time, the discrete mass matrix used in the equilibrium equations plays a crucial role in both computational efficiency and accuracy for transient dynamic response problems. Anytime if we add non-physical mass to increase the time step in a dynamic analysis, $F = m * a$ relation gets affected. Sometimes the effect is insignificant and in those cases adding non-physical mass is justifiable to just a few small elements in non-critical areas. User defined scale factor was used to scale the mass. It was observed that mass scaling saved computational time by 2x to 4x with 1-5% change in accuracy.

Material deformation has been assumed to be linear elastic for FR4 PCB, SnAgCu solders, copper pad on package side, BT substrate, silicon die and encapsulant (Table 6.4).

Table 6.4: Material Property for Finite Element Simulation

	Elastic Modulus (GPa)	Poisson's Ratio	Density (Kg/m3)
62Sn36Pb2Ag	32	0.35	8400
Mold	23.5	0.25	1650
Die	162	0.28	2329
Die Attach	2.76	0.35	7800
Epoxy Film	0.649	0.35	2100
BT substrate	17.4	0.28	1800
Bare FR4	16.8	0.39	1800

6.9 Model Validation

Transient dynamic strains have been predicted for 0-degree JEDEC drop and 3ft, 0-degree vertical drop respectively and correlated with high-speed strain-gage measurements and digital-image correlation measurements. Figure 6.20 and Figure 6.21 shows the strain correlation for Test board C from simulation and strain gage sensors located on the packages and on the PCB respectively. During impact, the peak deformation occurs within 20 ms, and hence the correlation is shown for this time duration. The strains on the PCB-side and the package-side show good correlation with the experiment. Transient mode shapes at different time intervals has been shown Figure 6.22 for Test-Board C. Correlation is for the 90-degree vertical drop orientation.

However, the plot is shown with the board drop horizontally from left-to-right, with the ground shown on the right side of the plot for both high-speed digital image correlation and explicit finite elements. Transient mode shapes have been plotted at 1.4ms, 2.8ms.

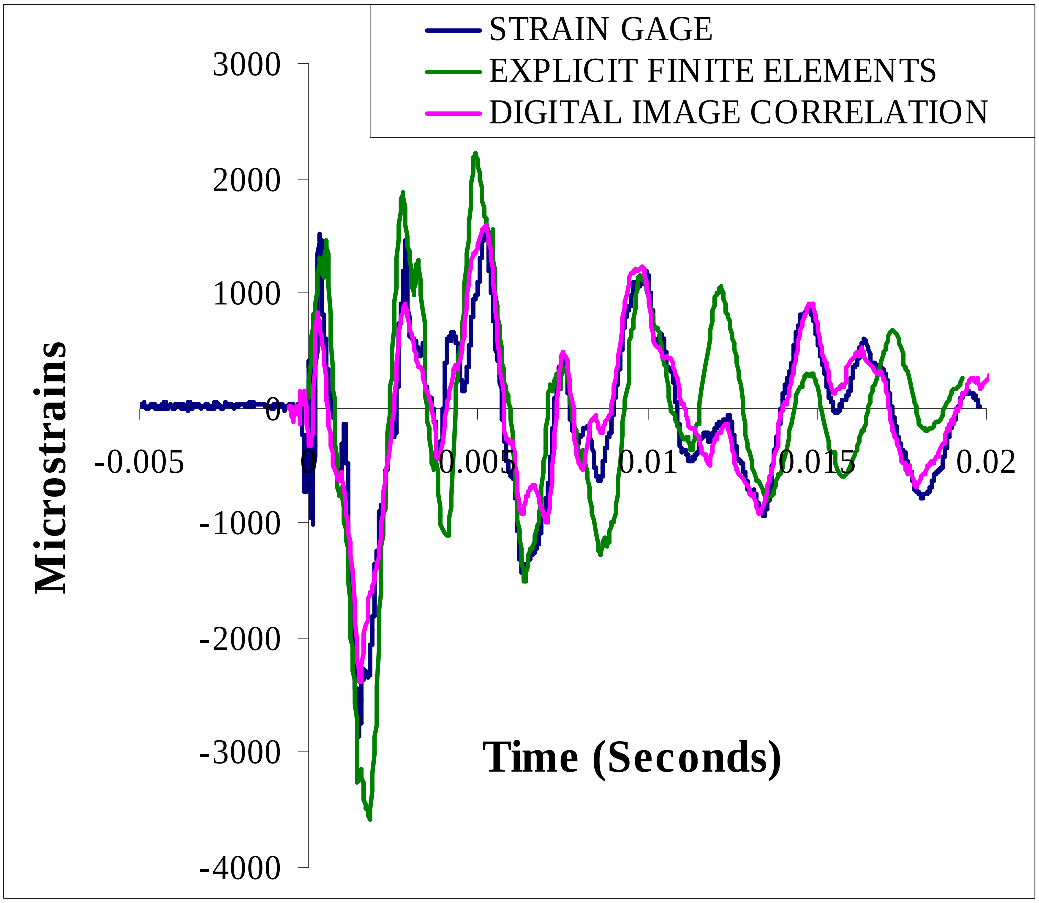


Figure 6.20: PCB Strain correlation between experiment and finite element model at location A3 on Test Board-C, during 3 ft Vertical Drop

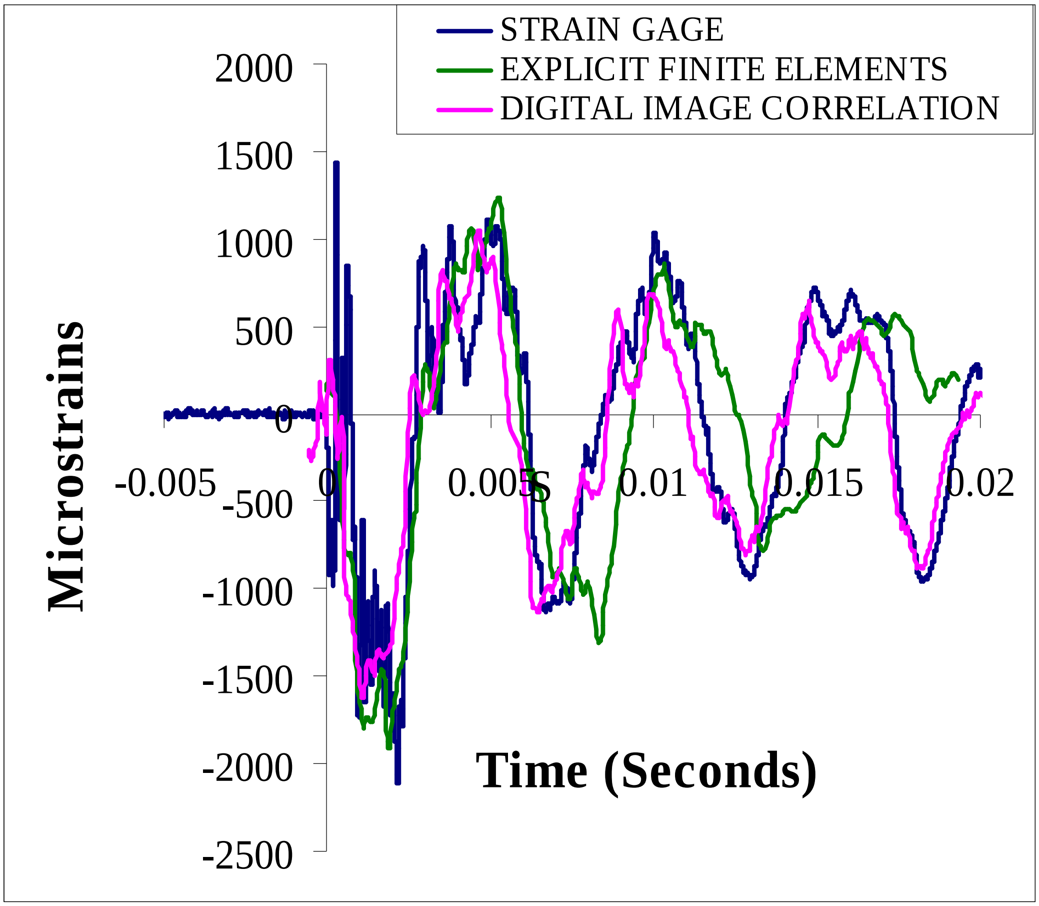
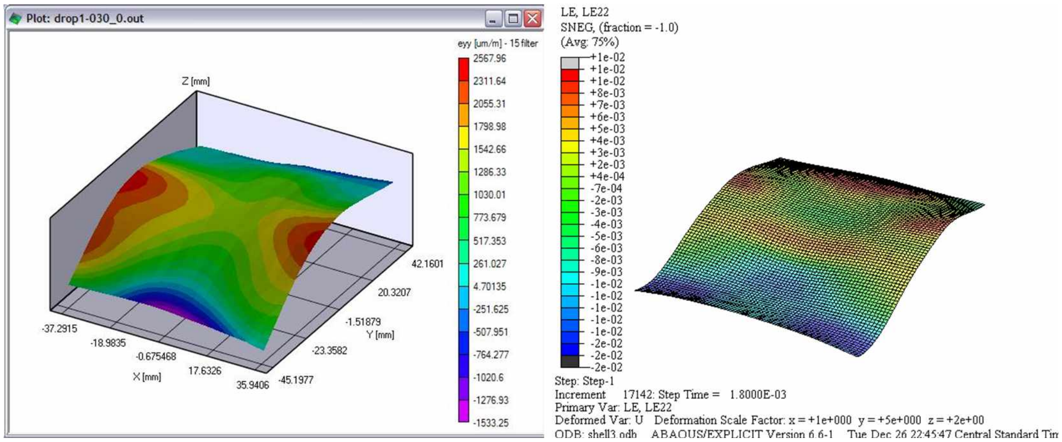
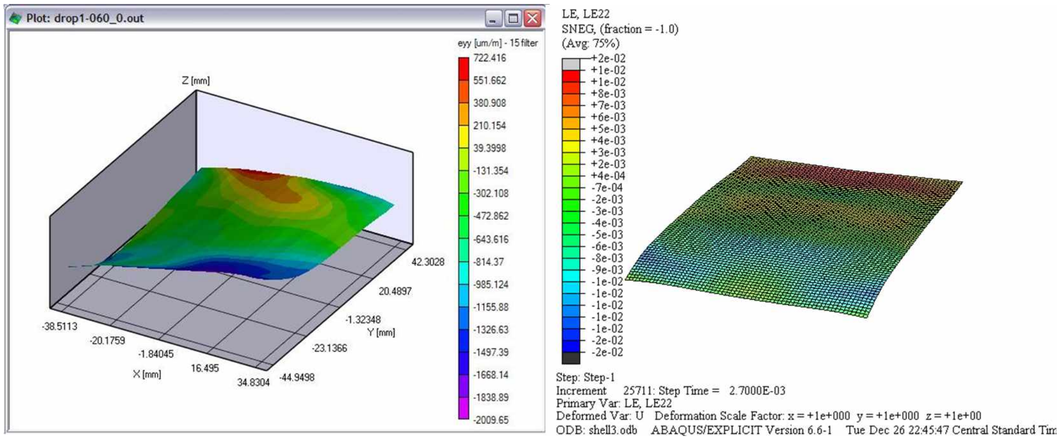


Figure 6.21: PCB Strain correlation between experiment and finite element model at location A1 on Test Board-C, during 3 ft Vertical Drop



```
Step: Step-1
Increment     17142: Step Time =    1.8000E-03
Primary Var: LE, LE22
Deformed Var: U    Deformation Scale Factor: x = +1e+000  y = +5e+000  z = +2e+00
ODB: shell3.odb    ABAQUS/EXPLICIT Version 6.6-1    Tue Dec 26 22:45:47 Central Standard Tim
```

t=1.4ms

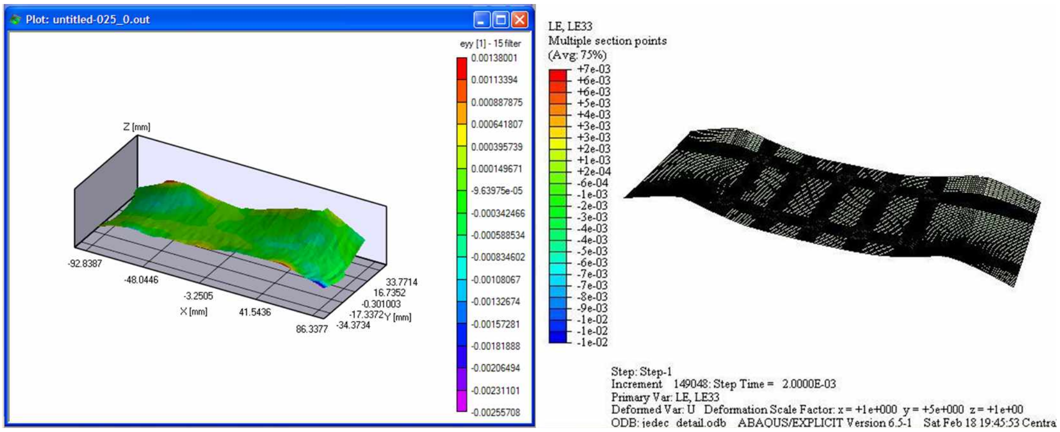


```
Step: Step-1
Increment     25711: Step Time =    2.7000E-03
Primary Var: LE, LE22
Deformed Var: U    Deformation Scale Factor: x = +1e+000  y = +1e+000  z = +1e+00
ODB: shell3.odb    ABAQUS/EXPLICIT Version 6.6-1    Tue Dec 26 22:45:47 Central Standard Tim
```

t=2.8ms

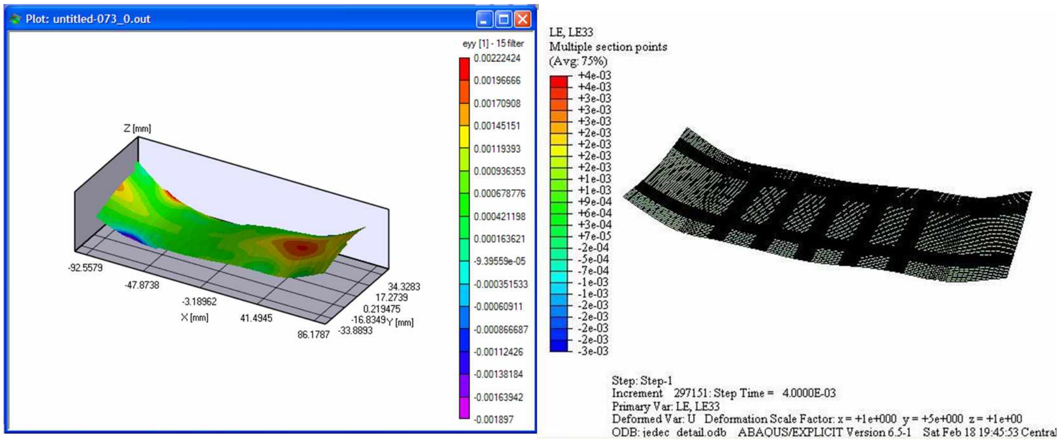
Figure 6.22: Correlation of DIC and FEM Full Field 3D Strain Contour of Test Board C

(vertical drop)



```
Step: Step-1
Increment    149048: Step Time =    2.0000E-03
Primary Var: LE, LE33
Deformed Var: U   Deformation Scale Factor: x = +1e+000  y = +5e+000  z = +1e+00
ODB: jedec  detail.odb    ABAQUS/EXPLICIT Version 6.5-1    Sat Feb 18 19:45:53 Centra
```

1.4 ms



```
Step: Step-1
Increment    297151: Step Time =    4.0000E-03
Primary Var: LE, LE33
Deformed Var: U   Deformation Scale Factor: x = +1e+000  y = +5e+000  z = +1e+00
ODB: jedec  detail.odb    ABAQUS/EXPLICIT Version 6.5-1    Sat Feb 18 19:45:53 Central
```

4.29 ms

Figure 6.23: Correlation of DIC and FEM Full Field 3D Strain Contour of Test Board D

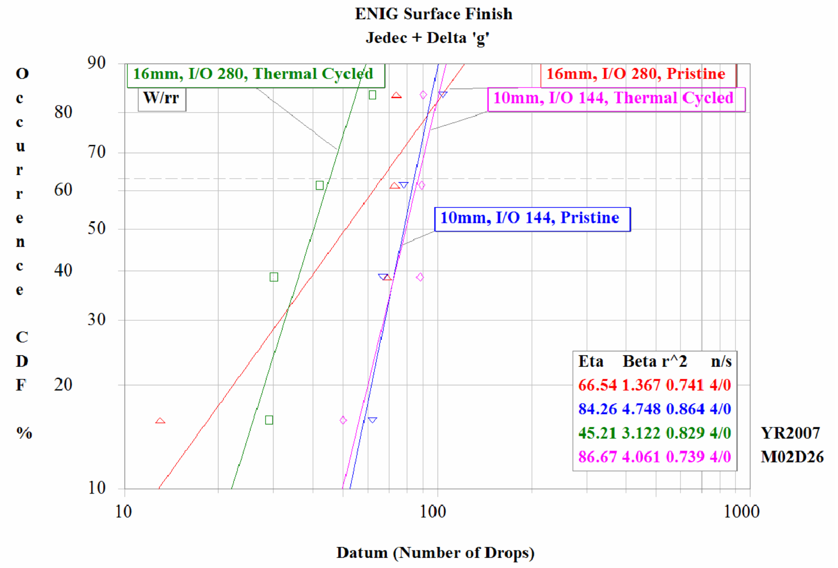
(0-degree JEDEC Drop)

The board has been dropped with a weight attached to the top end of the printed circuit board assembly, which is equivalent to the left-edge in the plotted orientation in Figure 6.22. The predicted mode shapes show good correlation with experimental data.

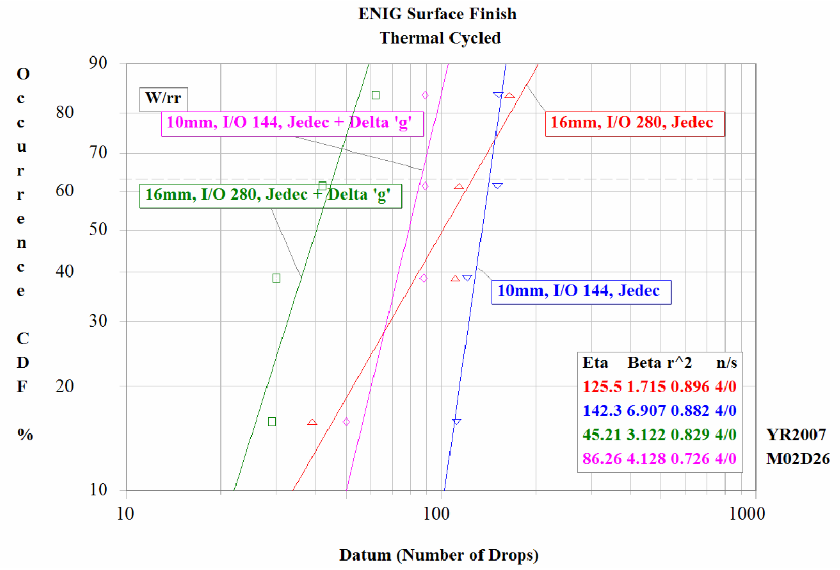
Transient mode shapes at different time intervals has been shown Figure 6.23 for Test-Board D. Correlation is for the 0-degree JEDEC configuration between high-speed digital image correlation and explicit finite elements. Transient mode shapes have been plotted at 1.4ms, 4.29ms. The predicted mode shapes show good correlation with experimental data.

6.10 Failure Modes

Previously, various pad finishes such as ENIG (Electroless Nickel Immersion Gold), Solder on Pad (SOP), Immersion Silver, Immersion Gold has been studied under high strain rate events such as cyclic bend tests, and vibrations caused due to drop impact. Performance of the Flip-Chip BGAs, CSPs are studied according to JEDEC standards [Jiang 2005], ball pull and shear tests [Bansal 2005, Song 2006], horizontal free drop of PCB assemblies in face-up and face-down position [Xie 2006]. Previous research involved comparative study of failure modes based on area percentage of solder remaining on the pad [Song 2006], crack progression based on cross-sectioned samples after failure. Relative drop performance has been quantified in terms of mean-drops-before-failure [Xie 2006]. Failure modes have been classified as ductile and brittle at the bulk solder and IMC interface on the package and the PCB side.



(a)



(b)

Figure 6.24: Weibull Distribution of 16 mm, 288 I/O and 10 mm, 144 I/O components (a) Comparison of Pristine and Thermal-Cycled Board Assembly Drop Performance in JEDEC+ΔG Configuration (b) Comparison of G-Loading on Drop Performance of Thermal Cycled Boards in 0-degree JEDEC Configuration.

It has been shown in the past that Flip-chip BGA substrates with SOP surface finish performs best compared to Electrolytic NiAu and ENIG under ball pull test [Bansal 2005]. Ni/Au performs better than OSP on board level drop tests [Jiang 2005]. ENIG was better than OSP and ImAg for bend test and drop test [Hossain 2006, Chong 2006], OSP pads generated more brittle failures in ball pull tests compared to ENIG [Song 2006], OSP enhanced drop performance compared to ENIG for PBGA packages subjected to ball pull tests [Chai 2005, Xie 2006].

The 0-degree drop was done in the JEDEC configuration, involving a 1500g, 0.5 ms pulse (labeled as JEDEC). In addition, the drop height was increased to obtain shock pulses of higher magnitude (labeled as JEDEC+ΔG). Current research, discusses the failure modes of BGA packages when the PCB assembly is subjected to drop tests according to JEDEC test standards. The packages are dropped until failure. Failure is monitored using continuity during the transient drop event. Figure 6.24 shows the comparison of pristine and thermal-cycled board assembly drop performance, and comparison of G-Loading on drop performance of thermal cycled boards in 0-degree JEDEC Configuration. For ENIG surface finish, it is seen (Figure 6.24) that 16mm I/O 280 package; drop reliability reduces against 10mm, I/O 144 irrespective of drop height, pristine or thermal cycled boards. There is marginal difference in characteristic life for overlapped stresses caused due to pristine and thermal cycling on 10mm package architecture. Shock severity reduces characteristic life irrespective of package size, surface finish and environmental conditions.

The samples are cross-sectioned and SEM images (Figure 6.25) are used to see the failure cites. ENIG surface exhibited the best drop performance among all the surface finishes (Figure 6.24). Based on the images, failures have been classified into five types as mode A, B, C, D and E (Figure 6.26). It is observed that ENIG surface finish performs better than ImAg and ImSn. The results are consistent with the published literature. It is observed that small packages in terms of body size and I/O count are stronger than the bigger packages. But as the drop severity is increased (drop height), body size does not matter. It is to be noted that these results are based on specific location of the packages and hence cannot be generalized. It will be of interest to study the influence of package location on the above observation. ImAg has better drop performance over ImSn with the pristine PCB assembly (Table 6.6). ImAg and ImSn perform equally better when the PCB assembly is subjected to thermal cycling (Table 6.7).

ENIG surface finish has good reliability as it forms protective Ni3Sn4 layer and hence there is no crack observed between copper pad and the board interface as against ImAg surface finish. PCB side resin crack failure (mode C) is the dominant failure under drop loading. Increase in shock severity induces solder-component and solder-board interface failures. Failure is observed on the solder-component interface for ImSn boards. High stresses tend to develop on the solder-component side as compared to solder/board side due to strain hardening effect of SAC alloys under repetitive loading.

Table 6.5: Percentage Difference in Drop-Performance due to Thermal Cycling of Pristine PCB Assemblies

	JEDEC Configuration		(JEDEC+ΔG)	
	280I/O FlexBGA	144 I/O TarrayBGA	280I/O FlexBGA	144 I/O TarrayBGA
ImAg	56	38	85	80
ENIG	1.37	12.67	28.5	78.75
ImSn	53.6	30	38.7	36.2

Table 6.6: Percentage Difference in Drop-Performance for ImAg, ImSn, Board Surface finish w.r.t. ENIG (PRISTINE Condition)

Pristine Board	JEDEC Configuration		(JEDEC+ΔG)	
Surface Finish	ImAg	ImSn	ImAg	ImSn
280I/O FlexBGA	69	77	-5	72.8
144 I/O TarrayBGA	67	84.8	30	63.6

Table 6.7 : Percentage Difference in Drop-Performance for ImAg, ImSn, Board Surface finish w.r.t. ENIG (Thermal Cycled Condition)

Thermal Cycled Boards	JEDEC Configuration		(JEDEC+ΔG)	
Surface Finish	ImAg	ImSn	ImAg	ImSn
280I/O FlexBGA	89	89.5	78	76.6
144 I/O TarrayBGA	77	88	86.6	77

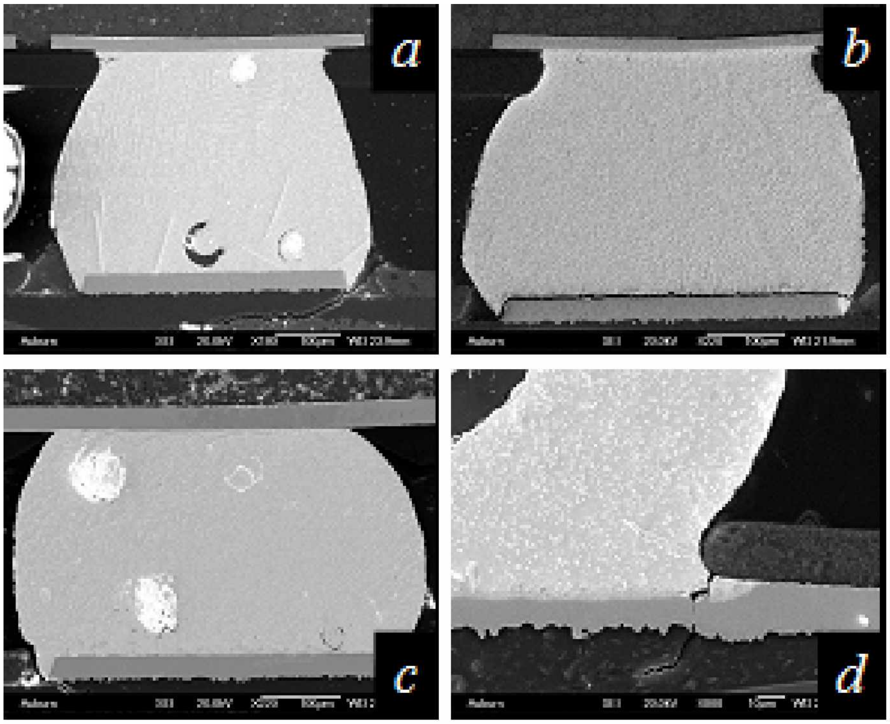


Figure 6.25: Failure modes, (a) Resin Crack (b) Solder-Copper pad on PCB-side(c) Solder-Copper pad on Package-side (d) Copper trace failure

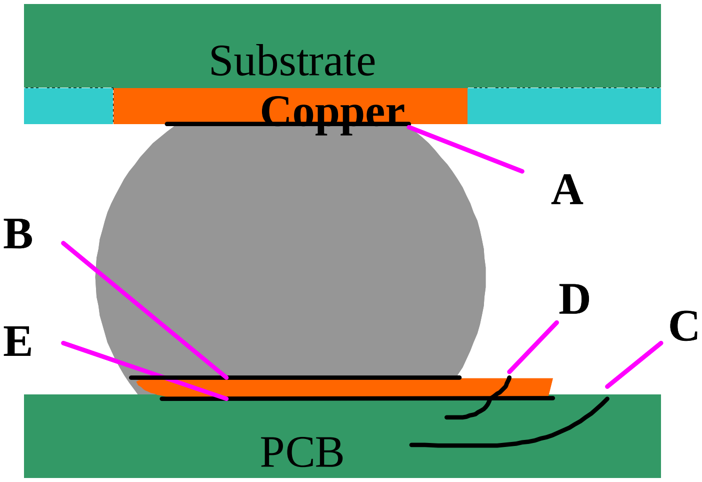


Figure 6.26: Failure Modes

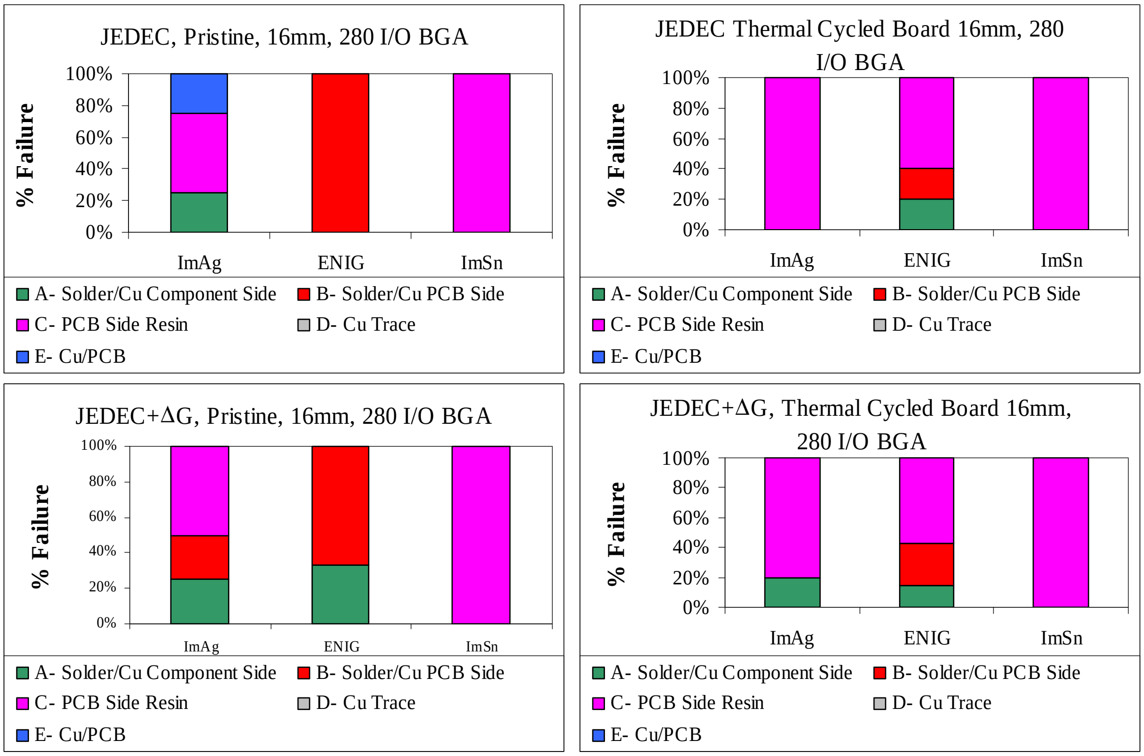


Figure 6.27: Failure Modes for16mm, 280 I/O BGA with SAC405 alloys on different surface finish

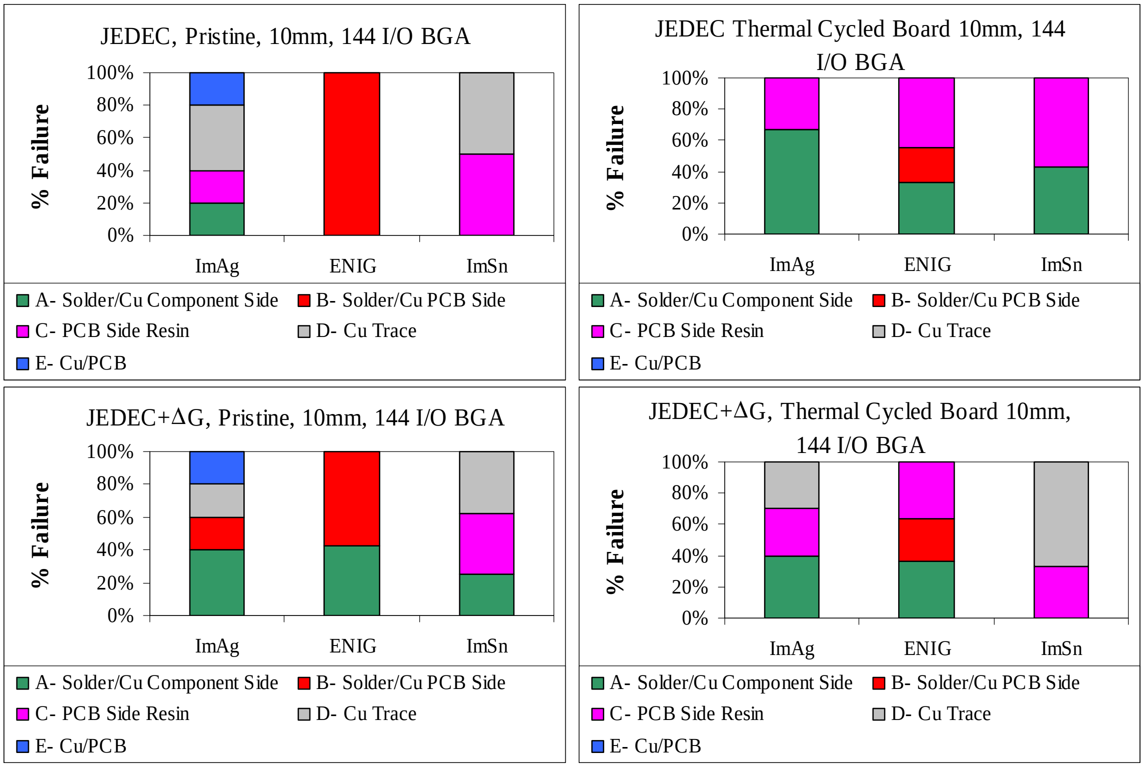


Figure 6.28: Failure Modes for10mm, 144 I/O BGA with SAC405 alloys on different surface finish

6.11 Transient Strain Signals from Digital Image Correlation for Health Monitoring

In this dissertation statistical pattern recognition is used to study the degradation of reliability in electronic assemblies, due to shock and drop. In the presence of multiple failure modes, discussed in the failure modes section of this dissertation, health monitoring of assemblies has been investigated by monitoring the confidence values computed by applying statistical pattern recognition techniques to the transient-strain response, transient displacement-response, vibration mode shapes and frequencies of the electronic assembly under shock and drop. Correlation of structural response, damage proxies and underlying damage has been accomplished with high-speed digital image correlation and high-speed data-acquisition. Here two statistical pattern recognition techniques, including the wavelet packet approach and the Mahalanobis distance approach have been investigated. Details of the analysis technique are discussed in [Lall 2006a]

6.11.1 Wavelet Packet Approach

Wavelets have been used in several areas including data and image processing [Martin 2001], geophysics [Kumar 1994], power signal studies [Santoso 1996], meteorological studies [Lau 1995], speech recognition [Favero 1994], medicine [Akay 1997], and motor vibration [Fu 2003, Yen 1999]. The wavelet transform is defined by

$$Wf(u,s) = \langle f, \psi_{u,s} \rangle = \frac{1}{\sqrt{s}} \int_{-\infty}^{+\infty} f(t)\ \psi^{*}\left(\frac{t-u}{s}\right) dt \tag{6.19}$$

where the base atom ψ^* is the complex conjugate of the wavelet function which is a zero average function, centered around zero with a finite energy. The function f(t) is decomposed into a set of basis functions called the wavelets with the variables s and u, representing the scale and translation factors respectively.

An entropy-based criterion is used to select the most suitable decomposition of a given signal. This implies that at each node of the decomposition tree, the information gained by performing a split is quantified. Simple and efficient algorithms exist for both wavelet packet decomposition and optimal decomposition selection. Adaptive filtering algorithms, allow the Wavelet Packet transform to include the "Best Level" and "Best Tree" features that optimize the decomposition both globally and with respect to each node. For obtaining the optimal tree, a node is split into two nodes, if and only if the sum of entropy of the two nodes is lower than the sum of entropy of the initial node. After the wavelet packet transform, the wavelet packet energy is calculated at each node of the decomposition tree. An energy signature E_n for each sequence of wavelet packet coefficients $C^{p}_{n,k}$, for $n = 0,1,2.......4^{p-1}$ can be computed by using the formula

$$E_n = \frac{1}{N^2}\sum_{k=1}^{N}\left|C^{p}_{n}\right|^2 \tag{6.20}$$

where N is the total number of points in the signal at a given node in the wavelet packet tree, p is the decomposition depth, and Ci is the wavelet packet coefficients obtained during the wavelet packet transform at the particular node where energy is being calculated. The feature vector of length 4^{p-1}, is formed for the signal.

The packet energies obtained from the wavelet packet decomposition of the various mode shapes and frequencies of vibration of the electronic assembly are the basis for the computation of confidence values for health monitoring.

6.11.2 Mahalanobis Distance Approach

The Mahalanobis Distance classification is similar to the Maximum Likelihood classification except for the class covariances which are all assumed to be equal, hence the method is more efficient. It is based on correlations between variables by which different patterns can be identified and analyzed. It is a useful way of determining similarity of an unknown sample set to a known one. It differs from Euclidean distance in that it takes into account the correlations of the data set. The Mahalanobis distance from a group of values with mean $\mu = (\mu_1, \mu_2, \mu_3, \mu_4 \ldots, \mu_n)$ and covariance matrix Σ for a multivariate vector $x = (x_1, x_2, x_3, x_4 \ldots, x_n)$ is,

$$D_M(x) = \sqrt{(x-\mu)^T \Sigma^{-1} (x-\mu)} \tag{6.21}$$

Mahalanobis distance can also be defined as dissimilarity measure between two random vectors x and y of the same distribution with the covariance matrix Σ,

$$d(\mathring{x}, \mathring{y}) = \sqrt{(\mathring{x}-\mathring{y})^T \Sigma^{-1} (\mathring{x}-\mathring{y})} \tag{6.22}$$

The Mahalanobis distance approach has been chosen over other classification approaches as it considers the variance and covariance of the variables as opposed to only the average value. The distance measure is taken as a basis for the calculation of the confidence values for prognostics.

Figure 6.29 demonstrates the relative confidence value degradation in the transient strain feature vector calculated from Mahalanobis distance and the Wavelet Packet Energy feature vectors for pristine, thermally-aged, and thermally-cycled assemblies after the 1st shock-impact. Figure 6.30 shows the relative confidence value of the transient strain feature vector for pristine, thermally-aged and the thermally cycled electronic assemblies after 50 shock-impacts.

A different training-signal has been selected for each relative CV calculation, as appropriate, in Figure 6.29 to Figure 6.32. For example, in Figure 6.30, the pristine assemblies subjected to 50 shock-impacts have been taken as the training signal for the analysis. Figure 6.31 and Figure 6.32 demonstrate the confidence value degradation in the transient strain feature vector calculated from Mahalanobis distance and the Wavelet Packet Energy feature vectors versus number of drops for thermally aged and thermally-cycled assemblies respectively, after 1, 25, and 50 drops. The transient strain feature vector shows a significant degradation in the feature vector at 25 drops. The graphs demonstrate that the transient strain signal feature vector constructed from full-field DIC measurements have the ability to identify the onset of degradation in the presence of multiple failure modes.

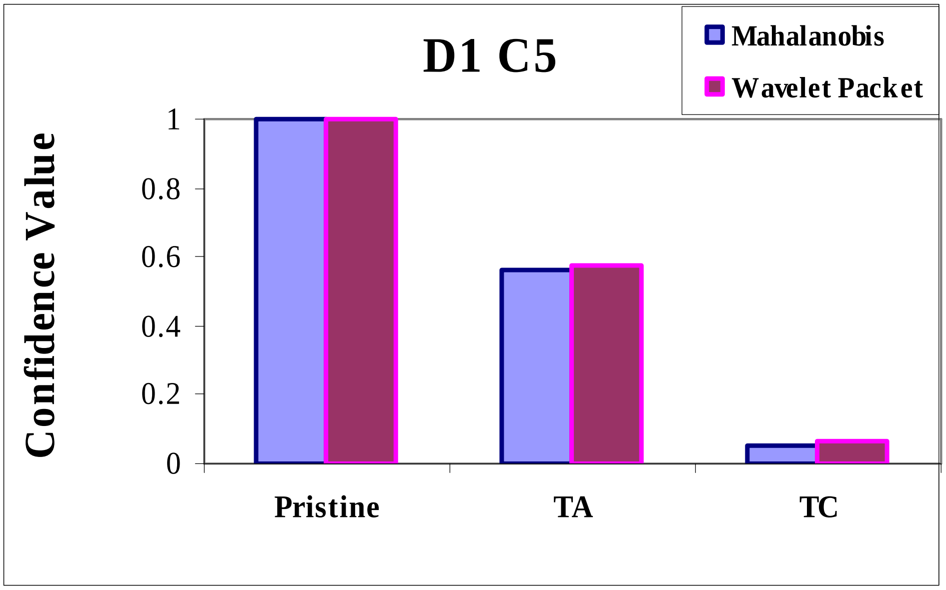


Figure 6.29: Relative Confidence Value Degradation for pristine, thermally-aged and thermally-cycled Assemblies after first shock-impact.

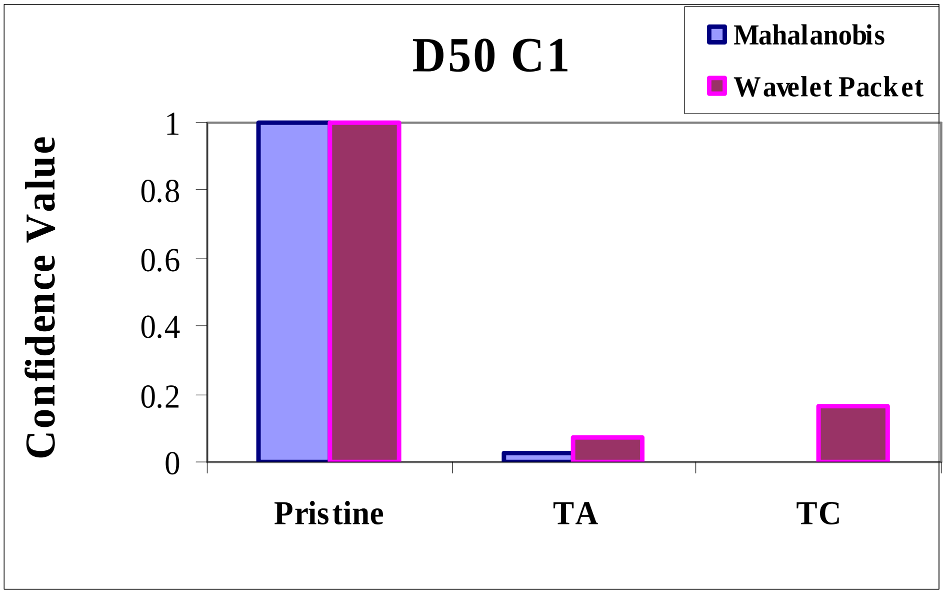


Figure 6.30: Relative Confidence Value of the Pristine, Thermally Aged and Thermally-Cycled Assemblies after 50-Shock-Impacts.

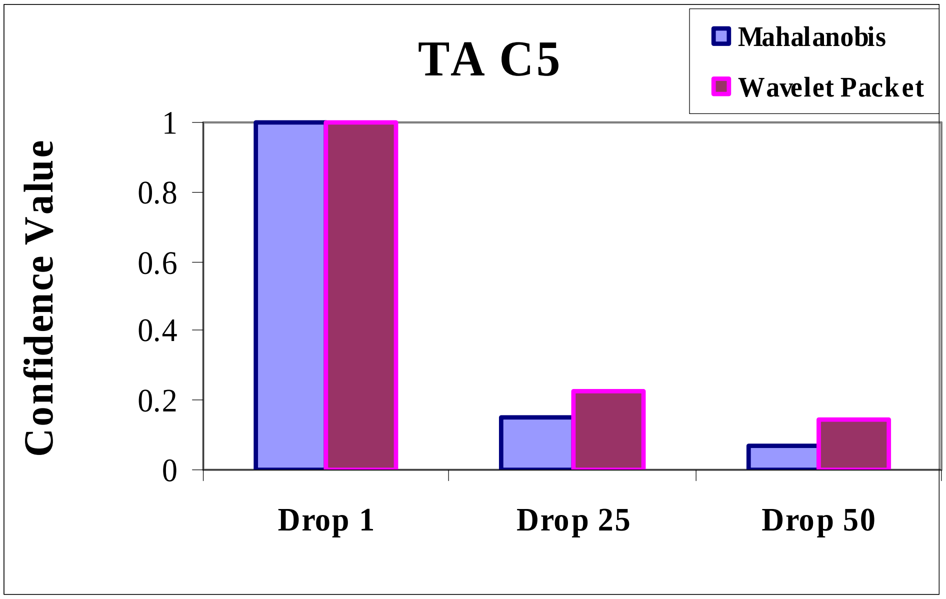


Figure 6.31: Confidence Value Degradation for THERMALLY AGED Assemblies versus Number of Drops.

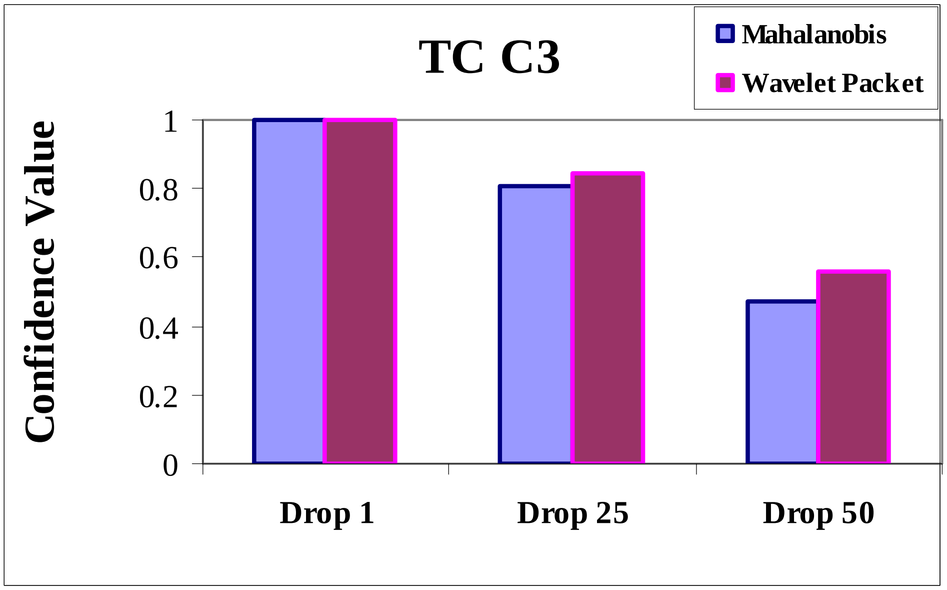


Figure 6.32: Confidence Value Degradation for THERMALLY CYCLED Assemblies versus Number of Drops.

6.12 Summary and Conclusions

In this dissertation, full-field strain measurement using digital image correlation (DIC) has been investigated for shock and vibration of electronic assemblies. It has been shown that accurate full-field measurements can be made using DIC in conjunction with high-speed imaging for 5-electronic assemblies (labeled Test Board-A to Test Board-E) with various packaging architectures. Transient impact strain histories have been measured in two orientation including 0-degree JEDEC shock and the 90-degree Vertical drop. Full-field strain data from DIC has been correlated with high-speed strain measurements at discrete electronic assembly locations. Explicit finite element models have been constructed for all the electronic assemblies to simulate transient-impact. Model predictions have shown to have good correlation with experimental data. All the samples in the study have been cross-sectioned and the failure modes quantified for the three finishes studied including, ENIG, ImAg, and ImSn. The transient strain measurements have been analyzed using statistical pattern recognition and the ability to monitoring in-situ health of the electronic assemblies studied. Results show that the confidence value degradation of the transient strains feature vector from DIC can be used as leading indicator of failure.

CHAPTER 7

SUMMARY AND CONCLUSIONS

The following advancements in transient dynamics measurement and predictive techniques have been presented in this dissertation.

Prediction of Transient Deformation during Free drop of leaded and Eutectic BGAs

A methodology for prediction of transient dynamic behavior of a board assembly during drop has been developed. An 8-feet drop tower and various fixtures were designed in-house to drop test electronic products according to industry test standards [JEDEC 2003]. Strain gage sensors were mounted on the printed circuit board and the data was acquired using high-speed DAQ system. The electrical resistance of all the packages was measured during the transient drop event. Simultaneously high-speed video was acquired at 50,000 fps to study the deformation kinematics. Portable electronic products dropped from 6ft may change orientation significantly during the drop. Small changes in orientation may produce significant changes in the measured response of the product making it difficult to establish a valid baseline for development of finite-element models. Repeatability of drop orientation may help with the identification of most vulnerable drop configurations.

It has been shown that a fairly accurate correlation of model prediction with experimental data on relative displacement and strain can be obtained using smeared property models. The methodology has been demonstrated for various component architectures including flex-substrate ball-grid arrays, plastic ball-grid arrays, thermally enhanced C2 ball-grid arrays and lead-frame chip-scale packages such as PQFN. The smeared property models are advantageous, since they allow the adequate model accuracy while maintaining reasonable computational efficiency.

Prediction of Failure due to Cumulative Damage during Shock on Pristine and Aged assemblies

A methodology for development of the damage equivalency for area-array packaging architectures exposed to single and sequential thermo-mechanical and transient shock stresses has been developed. Wavelet transforms have been applied to analysis of transient-response of electronics under shock and vibration. Wavelets have been used to avoid the problem of fixed time-frequency window with windowed Fourier transforms, which causes over-representation of the high-frequency components and an under-representation of the low-frequency components of a transient drop-impact signal.

A relative damage index has been developed for prediction of the number of drops-to-failure under transient loads. The research presented attempts to address the need for techniques and damage proxies which enable the determination of failure-envelopes and cumulative damage during overstress and repetitive loading for various packaging architectures. The approach is based on assembly strains, since there are experimental limitations of measuring field-quantities and their derivatives at the board-solder joint interface, primarily because of the small size of interconnects in fine-pitch ball-grid array packages. The approach has been applied to both lead-free (95.5Sn4.0Ag0.5Cu) and leaded (63Sn37Pb) ball-grid array architectures.

Full-Field High-Speed Measurement of Board Assembly Deformation using Digital Image Correlation

Full-field strain measurement using digital image correlation (DIC) has been investigated for shock and vibration of electronic assemblies. It has been shown that accurate full-field measurements can be made using DIC in conjunction with high-speed imaging on different electronic assemblies with various packaging architectures. Transient impact strain histories have been measured in two orientation including 0-degree JEDEC shock and the 90-degree Vertical drop. Full-field strain data from DIC has been correlated with high-speed strain measurements at discrete electronic assembly locations. Explicit finite element models have been constructed for all the electronic assemblies to simulate transient-impact. Model predictions have shown to have good correlation with experimental data. All the samples in the study have been cross-sectioned and the failure modes quantified for the three finishes studied including, ENIG, ImAg, and ImSn. The transient strain measurements have been analyzed using statistical pattern recognition and the ability to monitoring in-situ health of the electronic assemblies studied. Results show that the confidence value degradation of the transient strains feature vector from DIC can be used as leading indicator of failure.

BIBLOGRAPHY

Abaqus Documentation, Finite Elements and Rigid Bodies, Getting Started with Abaqus Explicit: Keywords Version, Version6.5, Section 4.1, 2005.

Ahat, S, Sheng, M., Luo, L., “Microstructure And Shear Strength Evolution Of Sn/Ag/Cu Surface Solder Joint During Aging”, Journal of Electronic Mater., Vol. 30, No. 10, pp. 1317-1332, 2001.

Akay, M., “Wavelet Applications in Medicine”, IEEE Spectrum, Vol. 34, Issue 5, pp.50–56, 1997.

Alajoki, M., Nguyen, L., Kivilahti, J., “Drop Test Reliability of Wafer Level Chip Scale Packages”, Electronic Components and Technology Conference, pp. 637-644, 2005.

American Society of Mechanical Engineers (ASME), “Standard Practices for Cycle Counting in Fatigue Analysis”, ASTM E1049-85, 1997.

Amodio, D., Broggiato, G., Campana, F., Newaz, G., “Digital Speckle Correlation for Strain Measurement by Image Analysis, Society for Experimental Mechanics”, Vol. 43, No. 4, December 2003.

Bangs, E., Beal, R., Wel. J. Res. Supp., 54, p.377, 1978.

Bannantine, J. A., Comer, J.J., Handrock, J.L., “Fundamentals of Metal Fatigue Analysis”, Prentice Hall, 1990.

Bansal, A., Yoon, S., Xie, J., Li, Y., Mahadev, V., “Comparison of Substrate Finishes for Flip Chip Packages”, Electronic Components and Technology Conference, Vol. 1, pp. 30- 37, June, 2005.

Bieler, T., Jiang, H., “Influence of Sn Grain Size and Orientation on the Thermomechanical Response and Reliability of Pb-free Solder Joints”, Electronic Components and Technology Conference, pp. 1462-14671, May, 2006.

Chai T.C., Quek,S., Hnin W.Y., Wong E.H., Chia, J., Wang Y.Y., Tan Y.M., Lim C.T., “Board Level Drop Test Reliability of IC Packages”, Electronic Components and Technology Conference , Vol. 1 pp. 630- 636, June, 2005.

Che, F., Low, T., Pang, J., “Modeling Thermo-Mechanical Reliability of Bumpless Flip Chip Package”, Electronic Components and Technology Conference, pp. 421-426, 2004.

Che, F.X., Pang, H. L., “Modeling Board-Level Four-Point Bend Fatigue and Impact Drop Tests”, Proceedings of the 56th Electronic Components and Technology Conference, San Diego, CA, pp. 443-448, 2006.

Chong, D., Ng, K., Tan, J., Low, P., “Drop Test Reliability Assessment Of Leaded/Lead-Free Solder Joints For IC Packages”, Electronic Components and Technology Conference, pp. 210-217, 2004.

Chong, D. Y. R., Ng, K., Tan, J. Y. N., Low, P. T. H., Pang, J. H. L., Che, F. X., Xiong, B. S., Xu, L. “Drop Impact Reliability Testing for Lead Free and Leaded Soldered IC Packages”, Electronic Components and technology Conference, Orlando, Florida, pp. 622-629, May 31-June 3, 2005.

Chong, D., Che, F., Xu, L., Pang, J., Xiong, B., Lim, B., “Performance Assessment on Board-level Drop Reliability for Chip Scale Packages (Fine-pitch BGA), Electronic Components and Technology Conference”, pp. 356-363,May 2006.

Clech., J-P., “Solder Reliability Solutions: a PC-based Design-for-reliability Tool”, Proceedings of the Surface Mount International Conference, Sept. 8-12, San Jose, CA, Vol. I, pp. 136-151, 1996.

Clech., J-P., “Flip-chip /CSP Assembly Reliability and Solder Volume Effects”, Proceedings of the Surface Mount International Conference, San Jose, CA, August 25-27, pp. 315-324, 1998.

Chiu, T., Zeng, K., Stierman, R., Edwards, D., Ano, K., “Effect of Thermal Aging on Board level drop reliability for Pb-free BGA Packages”, Electronic Components and Technology Conference, pp. 1256-1262, June 2004.

Coffin, L., “A Study Of The Effect Of Cyclic Thermal Stresses On A Ductile Metal”, ASME Transactions, Vol. 76, pp. 931-950, 1954.

Darveaux, R., et al., “Reliability of Plastic Ball Grid Array Assembly”, Chapter 13, Ball Grid Array Technology, Ed. Lau, J.H. McGraw-Hill, 1995.

Date, M., Shoji, T., Fujiyoshi, M., Sato, K., Tu, K., “Impact Reliability Of Solder-Joints”, Electronic Components and Technology Conference, pp. 668-674, 2004.

Davis, C., Freeman, D., “Statistics Of Subpixel Registration Algorithms Based On Spatiotemporal Gradients Or Block Matching”, Optical Engineering, 37, pp. 1290-1298, 1998.

Downing, S. D., and Socie, D. F., “Simple Rainflow Counting Algorithms, International Journal of Fatigue”, Vol. 4, No. 1, pp. 31-40, 1982.

Dunford, S., Okura, J., “JEDEC Drop Test Preparations For Qualification of Ceramic LGAs”, Proceedings of the SMTA International, Chicago, IL, pp. 314-318, 2004.

Dutta, I., “A Constitutive Model for Creep of Lead-Free Solders Undergoing Strain-Enhanced Microstructural Coarsening: A First Report”, Journal of Electronic Materials, Vol 32, No. 4, pp. 201-207, 2003.

Dutta, I., “Impression Creep Testing and Micro-structurally Adaptive Creep Modeling of Lead Free Solder Interconnects”, TRC, October 25-27, 2004.

Dutta, I., Park, C., Choi, S., “Creep and Microstructural Evolution in Lead-Free Microelectronic Solder Joints”, Proceedings of InterPACK ’03, pp.1-6, July 6-11, 2003.

Ewins, D.J., “Modal Testing: Theory and Practice”, John Wiley and Sons, New York, 1984.

Favero, R.F., “Compound Wavelets: Wavelets For Speech Recognition, Proceedings of the IEEE-SP International Symposium on Time-Frequency and Time-Scale Analysis”, pp. 600 – 603, 1994.

Frear, D., “Microstructural Evolution During Thermomechanical Fatigue of 62Sn-36Pb-2Ag, and 60Sn-40Pb Solder Joints”, IEEE Transactions on Components Hybrids and Manufacturing Technology, Vol 13. No 4, pp. 718- 726, December 1990.

Fu, Y., Wen-Sheng Li, Guo-Hua Xu, “Wavelets And Singularities In Bearing Vibration Signals”, International Conference on Machine Learning and Cybernetics, Vol. 4, pp. 2433 - 2436, 2003.

Ghaffrian, R., Kim, N., “CSP Assembly Reliability And Effects Of Underfill And Double-Sided Population”, Electronic Components and Technology Conference, pp. 390-396, 2000.

Goyal, S. and Buratynski, E., “Methods For Realistic Drop Testing”, International Journal of Microcircuits And Electronic Packaging”, Vol. 23, No. 1, pp. 45-51, 2000.

Groothuis, S., Chen, C., Kovacevic, R., “Parametric Investigation of Dynamic Behavior of FBGA Solder Joints in Boar-Level Drop Simulation”, Electronic Components and Technology Conference, pp. 499-503, 2005.

Gu, J., Cooreman, S., et al., “Full-Field Optical Measurement For Material Parameter Identification With Inverse Methods”, WIT Transactions on The Built Environment, Vol. 85, 2006.

Gu, J., Cooreman, Steven., "Full-Field Optical Measurement For Material Parameter Identification With Inverse Methods", Proceedings of the 2006 SEM Annual Conference and Exposition on Experimental and Applied Mechanics, June 4-7, 2006.

Gupta,P., Doraiswami, R., Tummala, R., "Effect of Intermetallic Compounds on Reliability of Sn-Ag-Cu Flip Chip Solder Interconnects for Different Substrate Pad Finishes and Ni/Cu UBM", Electronic Components and Technology Conference, Vol. 1, pp. 68- 74, June, 2004.

Hannan, N., Viswanadham, P., Crane, L., et al., "Reworkable Underfill Materials for improved manufacturing and reliability of CSP assemblies", Proceedings of the 2001 APEX Conference, San Diego, Jan 14-18, pp. AT8-3 - 1AT8-3-10, 2001.

Hannan, N., Kujala, A., Mohan, V., Morganelli, P., Shah, J., "Investigation of Different Options of Pre-Applied CSP Underfill for Mechanical Reliability Enhancements in Mobile Phones", Electronic Components and technology Conference, Orlando, Florida, pp. 770-774, May 31-June 3, 2005

Helm, J., McNeill, S., Sutton, M., "Improved Three-Dimensional Image Correlation For Surface Displacement Measurement, Society of Photo-Optical Instrumentation Engineers", Vol. 35, No. 7, pp. 1911-1920, July 1996.

Henderson, D.W., Woods, J.J., Gosselin, T.A., Bartelo, J., King, D. E., Korhonen, T.M., Korhonen, M.A., Lehman, L.P., Cotts, E.J., Kang, S.K., Lauro, P., Shih, P., Goldsmith, C. and Puttliz, K., "The Microstructure of Sn in Near Eutectic Sn-Ag-Cu Alloy Solder Joints and its Role in Thermo-mechanical Fatigue", Journal of Materials Research, Volume 19, Number 6, , pp. 1608–1612, 2004.

Hossain, M., Zahedi, F., Agnafer, D., "Reliability of Lead (Pb) Free SAC Solder Interconnects With Different PWB Surface Finishes Under Mechanical Loading", Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronics Systems, pp. 1038-1048, May 2006.

Irving, S., Liu, Y., "Free Drop Test Simulation for Portable IC Package by Implicit Transient Dynamics FEM", 54th Electronic Components and Technology Conference, pp. 1062 – 1066, 2004.

JEDEC Solid State Technology Association, "Board-Level Drop Test Method of Components for Handheld Electronic Products", No. JESD22-B111, 2003.

Jiang, D., Hung, J., Wang, Y., Hsiao, C., "Effect of Solder Composition And Substrate Surface Finishes On Board Level Drop Test Reliability", InterPACK Conference Proceedings, July 17-22, San Francisco, 2005

Kehoe, L., Lynch, P., Guénebaut, V., “Measurement of Deformation and Strain in First Level C4 Interconnect and Stacked Die using Optical Digital Image Correlation”, Electronic Components and Technology Conference, pp. 1874-1881, May 2006.

Kim, J., Jo, I., Chung, Y., Lim, J., “Optimal Design of a Cellular Phone Using LS-OPT Considering the Phone Drop Test”, 7th International LS-DYNA Users Conference, Dearborn, MI, pp. 14/2-14/10, May 2001.

Kirkpatrick, S., Schroeder, M., Simons, J., “Evaluation of Passenger Rail Vehicle Crashworthiness, International Journal of Crashworthiness,” Vol. 6, No. 1, pp. 95-106, 2001.

Kivilahti, J. and Laurila, T., Laboratory of Electronics Production Technology, Helsinki University of Technology, Finland

Kumar, P, Georgiou, E. F., “Wavelets in Geophysics, Wavelets and its Applications”, Academia Press, 1994.

Lim, C.T. and Low, Y.J., “Investigating the Drop Impact of Portable Electronic Products”, 52nd Electronic Components and Technology Conference, pp. 1270-1274, 2002.

Lau, K.-M., and H.-Y. Weng, “Climate Signal Detection Using Wavelet Transform: How to Make a Time Series Sing”, Bulletin of the American Meteorological Society, No. 76, pp. 2391–2402, 1995.

Lall, P., Choudhary, P., Gupte, S., “Health Monitoring for Damage Initiation & Progression during Mechanical Shock in Electronic Assemblies”, Proceedings of the 56th IEEE Electronic Components and Technology Conference, San Diego, California, pp.85-94, May 30-June 2, 2006.

Lall, P., Gupte, S., Choudhary, P., Suhling, J., “Solder-Joint Reliability in Electronics Under Shock and Vibration using Explicit Finite-Element Sub-modeling”, Electronic Components and Technology Conference, pp. 428-435, 2006.

Lall, P., Hande, M., Bhat, C., Islam, N., Suhling, J., Lee, J., “Feature Extraction and Damage-Precursors for Prognostication of Lead-Free Electronics”, Electronic Components Technology Conference, pp. 10, May 2006.

Lall, P., Islam, N., Suhling, J., “Prognostication and Health Monitoring of Leaded and Lead Free Electronic and MEMS Packages in Harsh Environments”, Electronic Components and technology Conference, Orlando, Florida, pp. 1305-1313, May 31-June 3, 2005

Lall, P., Panchagade, D., Liu, Y., Johnson, W., Suhling, J., “Shock and Drop-Impact Reliability Prediction for Fine-Pitch BGAs and CSPs, Lall, P., Panchagade”, Proceedings of the International Military and Aerospace Avionics COTS conference, Seattle, WA, Paper No. 3.1, pp. 1-28, August 3-5, 2004.

Lall, P., Panchagade, D., Liu, Y., Johnson, W., Suhling, J., “Shock-Induced Failure Prediction Model for Fine-Pitch BGAs and CSPs”, Surface Mount Technology Association (SMTA), pp. 472-481, 2004.

Lall, P., Panchagade, D., Liu, Y., Johnson, W., Suhling, J., “Models for Reliability of Fine-Pitch BGAs and CSPs in Shock and Drop Impact”, Proceedings of the ASME International Mechanical Engineering Congress and Exposition, Anaheim, CA, Paper No. IMECE2004-62317, pp. 1-10, November 13-19, 2004.

Lall, P. Panchagade, D., Liu, Y., Johnson, W., Suhling, J., “Models for Transient Dynamic Reliability of Area-Array Packages”, Accepted for Publication in the ASME Journal of Electronic Packaging, October 2005.

Lall, P., Panchagade, D., Choudhary, P., Suhling, J., Gupte, S., “Shock and Vibration Survivability Prediction using Failure Envelopes for Electronic and MEMS Packaging”, Proceedings of the ASME International Mechanical Engineering Congress and Exposition, Orlando, Florida, Paper IMECE2005-82612, pp. 1-12, November 5-11, 2005.

Lall, P., Panchagade, D., Choudhary, P., Suhling, J., Gupte, S., “Development of Survivability-Envelopes for Electronic Components in Extreme Shock and Vibration Environments”, Proceedings of the International Military and Aerospace Avionics COTS conference, Portsmouth, Virginia, pp. 1-31, August 2-4, 2005.

Lall, P., Panchagade, D., Choudhary, P., Suhling, J., Gupte, S., “Failure-Envelope Approach to Modeling Shock and Vibration Survivability of Electronic and MEMS Packaging”, Proceedings of the 55th IEEE Electronic Components and Technology Conference, pp. 480-490, June 1-3, 2005.

Lall, P., Panchagade, D., Choudhary, P., Gupte, S., Suhling, J., “Failure-Envelope Approach to Modeling Shock and Vibration Survivability of Electronic and MEMS Packaging”, Accepted for Publication in the IEEE Transactions on Components and Packaging Technologies, pp. 1-29, Nov. 2005.

Lall, P., Panchagade, D., Iyengar, D., Suhling, J., “Life Prediction and Damage Equivalency for Shock Survivability of Electronic Components”, Proceedings of the ITherm 2006, May 30-June 2, 2006.

Lall, P., Panchagade, D., Iyengar, D., Suhling, J., “Drop-Impact Reliability Prediction Models for Shock-Tolerant Design of Electronic Assemblies”, Surface Mount Technology Association (SMTA), September 24-28, 2006.

Lall, P., Panchagade, D., Liu, Y., Johnson, W., Suhling, J., “Models for Reliability Prediction of Fine-Pitch BGAs and CSPs in Shock and Drop-Impact”, IEEE Transactions on Components and Packaging Technologies, Vol. 29, No. 3, pp. 464-474, Sept 2006.

Lall, P., Panchagade, D., Iyengar, D., Suhling, J., “High Speed Digital Image Correlation for Transient-Shock Reliability of Electronics”, To be published at the Proceedings of the 57th IEEE Electronic Components and Technology Conference, Reno, Nevada, May 29-June 1, 2007.

Lall, P., Panchagade, D., Liu, Y., Johnson, W., Suhling, J., “Smeared Property Models for Shock-Impact Reliability of Area-Array Packages”, Accepted for Publication in the ASME Journal of Electronic Packaging, Jan 2007.

Lauro, P., Kang, S.K., Choi, W. K. and Shih, D., “Effect of Mechanical Deformation and Annealing on the Microstructure and Hardness of Pb-free Solders”, Journal of Electronic Materials, Volume 32, Number 12, pp.1432–1440, 2003.

Lee, T., et al., “Board Level Drop Test and simulation of TFBGA Packages for Telecommunication Application”, 53rd Electronic Components and Technology Conference Conference Proceedings, New Orleans, May 2003.

Lee, W. W., et al., “Solder Joint Fatigue Models: Review And Applicability To Chip Scale Packages”, Microelectronics Reliability, Vol. 40, pp. 231-244, 2000.

Liang, F. Z., Williams, R. L., and Hsieh, G., “Board strain states method and FCBGA mechanical shock analysis”, Proc 1st International Conference and Exhibition on Device Packaging, Scottsdale, AZ, March 2005

Lim, C., Low, Y., “Investigating The Drop Impact Of Portable Electronic Products”, 52nd Electronics Components and Technology Conference, pp. 1270-1274, 2002.

Lim, C. T. and Low, Y. J., “Drop Impact Survey of Portable Electronic Conference”, pp. 113-120, 2003

Lim, J., Tay, A., “Simulation of Mechanical Response of Solder Joints under Drop Impact Using Equivalent Layer Models,” Electronic Components and Technology Conference, pp. 491-498, 2005.

Lin, Chen-Chi, “Finite-Element Analysis Of A Computer Hard-Disk Drive Under Shock”, Journal of Mechanical Design, Vol. 24, pp. 121- 125, 2002.

Liu, J., Johnson, W., Yaeger, E., Konarski, M., Crane, L., “CSP Underfill, Processing and Reliability”, Proceedings of the 2002 APEX Technical Program, pp. S16-1-1 to S16-1-7, Jan 19-24, 2002.

Luan, J., Tee, T., “Effect of Impact Pulse Parameters on Consistency of Board Level Drop Test and Dynamic Responses”, Electronic Components and Technology Conference, pp. 665-673, 2005.

Manson, S., “Fatigue: A Complex Subject – Some Simple Approximations”, Experimental Mechanics 5, No. 7, pp. 193-226, 1965.

Martin, M.B., Bell, A.E., “New Image Compression Techniques Using Multiwavelets and Multiwavelet Packets”, IEEE Transactions on Image Processing, Vol 10, Issue 4, Pp. 500 – 510, 2001

Marzougui, D., Eskandarian, A., Mechzkowski, L., “Analysis and Evaluation of a Redesigned 3” x 3” Slipbase Sign Support System Using Finite Element Simulations”, International Journal of Crashworthiness, Woodhead Publishing Ltd, Cambridge, Vol. 4, No. 1, 1999.

McLaren, P. G., “Elementary Electric Power and Machines”, Pearson Higher Education, 1984.

Mei, Z., Ahmad, M., Hu, M., Ramakrishna, G., “Kirkendall Voids at Cu/Solder Interface and their effects on solder joint reliability”, Electronic Components and Technology Conference, pp. 415-420, 2005.

Mishiro, K., “Effect of the Drop Impact on BGA/CSP Package Reliability”, Microelectronics Reliability Journal, Vol. 42 (1), pp. 77-82, 2002

Morganelli, P., Shah, J., Wheelock, B., Mohan, V., Laffey, M., “Partial Pre-Applied Underfill for Assembly and Reliability of Pb-Free CSPs”, Electronic Components and technology Conference, Orlando, Florida, pp. 223-227, May 31-June 3, 2005.

Morris, J., Tribula, D., Summers, T., Grivas, D., “The Role of Microstructure in Thermal Fatigue of Pb/Sn Solder Joints”, Solder Joint Reliability, pp. 225- 265, New York, 1991.

Newland, D.E., “An Introduction to Random Vibrations, Spectral & Wavelet Analysis”, 3rd Edition, Addison Wesley, 1996.

Newman, K., “BGA Brittle Fracture-Alternative Solder Joint Integrity Test Methods”, Electronic Components and Technology Conference 2005, pp. 1194-1201.

Ng, H., Tee, T., et al., “Absolute and Relative Fatigue Life Prediction Methodology for Virtual Qualification and Design Enhancement of Lead-free BGA”, Electronic Components and Technology Conference, pp. 1282-1291, 2005.

Ong, K., Tan, C., Lim, C., et al., “Dynamic Materials Testing and Modeling of Solder Interconnects”, Electronic Components and Technology Conference, pp. 1075-1079, 2004.

Ou, S, Xu, Y., Tu, K., “Micro-Impact Test on Lead-Free BGA Balls on Au/Electrolytic Ni/Cu Bond Pad”, Electronic Components and Technology Conference 2005, pp. 467-471.

Pang, J., Che, F., Low, T., “Vibration Fatigue Analysis For FCOB Solder Joints”, Electronic Components and Technology Conference, pp. 1055-1061, 2004.

Pang, J., Che, F., “Isothermal Cyclic Bend Fatigue Test Method For Lead Free Solder Joints”, Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronics Systems, pp. 1011-1017, 2006.

Peng, H., Johnson, W., Flowers, G., et al., “Underfilling Fine Pitch BGAs”, IEEE Transactions on Electronics Packaging Manufacturing, Vol. 24, No. 4, pp. 293-299, Oct 2001.

Perkins, A., Sitaraman, K., “Vibration-Induced Solder Joint Failure of a Ceramic Grid Array (CCGA) Package”, Electronic Components and Technology Conference, pp. 1271-12787, 2004.

Pittarresi, J., Di Edwardo, A., “Optimal Support Locations for Circuit Cards Populated with Modules”, ASME Winter Conference, pp. 91-WA-EEP-2, December 1991.

Pitarresi, J., Roggeman, B., Chaparala, S., “Mechanical Shock Testing and Modeling of PC Motherboards”, Electronic Components and Technology Conference, pp. 1047-1054, 2004.

Rajendra, Pendse, D., Zhou, P., “Methodology For Predicting Solder Joint Reliability In Semiconductor Packages”, Microelectronics Reliability, Vol. 42, pp. 301-305, 2002.

Ratchev, P., Vandervelde, B., Wolf, I., “Reliability And Failure Analysis Of Snagcu Solder Interconnections For PSGA Packages On Ni/Au Surface Finish”, IEEE Transactions on Device and Materials Reliability, Vol. 4, No. 1, March 2004.

Rao, S., “Mechanical Vibrations”, Fourth Edition, Pearson Education, 2005

Ren, W., Wang, J., Reinikainen, T., “Applications of ABAQUS/Explicit Submodeling Technique in Drop Simulation of System Assembly, Electronic Components and Technology Conference, pp. 541-546, 2004.

Reu, P., Miller, T., “High-Speed Multi-Camera DIC for Finite Element Model Validation, Part 1”, SEM Annual Conference and Exposition on Experimental and Applied Mechanics, June 4-7, 2006.

Saha, S., Mathew, S., Canumalla, S., “Effect Of Intermettalic Phases On Performance In A Mechanical Drop Environment: 96.5Sn3.5Ag Solder On Cu And Ni/Au Pad Finishes”, Electronic Components and Technology Conference, pp. 1288-1295, 2004.

Shah, K., Mello, M., “Ball Grid Array Solder Joint Failure Envelope Development for Dynamic Loading”, Electronic Components and technology Conference, Las Vegas, Nevada, pp. 1067-1074, June 1-4, 2004

Santoso, S., Powers, E.J., Grady, W.M., Hofmann, P., “Power quality assessment via Wavelet transform analysis”, IEEE Transactions on Power Delivery, Volume 11 , Issue 2, pp. 924 – 930, 1996.

Seah, S., Lim, C., et al., “Mechanical Response of PCBs in Portable Products During Drop Impact”, 4th Electronics Packaging Technology Conference, pp. 120-125, 2002.

Seah, S.K.W., Wong, E.H., Ranjan, R., Lim C.T., Mai, Y.-W., “Understanding and Testing For Drop Impact Failure”, ASME, pp. 1-6, 2005.

Seeling, K., Suraski, D., “The Status of Lead-Free Solder Alloys”, Electronic Components and Technology Conference, Las Vegas, 2000

Shah, K., Mello, M., “Ball Grid Array Solder Joint Failure Envelop Development for Dynamic Loading”, 54th Electronic Components and Technology Conference Proceedings, Las Vegas, May 2004.

Sharan, K., Lahoti, S., Zhou, J., “Dynamic Response of a Portable Electronic Product Subjected to an Impact Load”, Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronics Systems, pp. 1049-1055, 2006.

Shin, D., Lee, D., et al., “Development of Multi Stack Package with High Drop Reliability by Experimental and Numerical Methods”, Electronic Components and Technology Conference, pp. 377-382, 2006.

Siviour, C., Williamson, D., et al., “Dynamic Properties Of Solders And Solder Joints”, J. Phys, IV France, Vol. 110, pp. 477-482, 2003.

Sogo, T. and Hara, S., “Estimation of Fall Impact Strength for BGA Solder Joints”, ICEP Conference Proc., Japan, pp. 369-373, 2001.

Song, F., Lee, S., “Investigation of IMC Thickness Effect on the Lead-free Solder Ball Attachment Strength: Comparison between Ball Shear Test and Cold Bump Pull Test Results”, Electronic Components and Technology Conference, pp.1196-1203, May 2006

Song, G., Shi, X., Qin, F., He, C., “Effect Of Loading Mode, Temperature And Moisture On Interface Fracture Toughness Of Silicon/Underfill/Silicon Sandwitched System”, Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronics Systems, pp. 1147-1152, May 2006.

Srinivasan, V., Radhakrishnan, S., Zhang, X., Subbarayan, G., Baughn, T., Nguyen, L., “High Resolution Characterization of Materials Used In Packages Through Digital Image Correlation”, InterPACK Conference Proceedings, July 17-22, 2005.

Sun, Y., Pang, J., Shi, X., Tew, J., “Thermal Deformation Measurement by Digital Image Correlation Method”, Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronics Systems, pp. 921-927, May 2006.

Syed, A., “Accumulated Creep Strain and Energy Density Based Thermal Fatigue Life Prediction Models for SnAgCu Solder Joints”, Electronic Components and Technology Conference, pp. 737-746, 2004.

Syed, A., Kim, S. M., Lin, W., Khim, J.Y., Song, E.K., Shin, J.H., Panczak, T., “An Methodology for Drop Performance Prediction and Application for Design Optimization of Chip Scale Packages”, Electronic Components and technology Conference, Orlando, Florida, pp. 472-479, May 31-June 3, 2005.

Tee, T. Y., Luan, J., Pek, E., Lim, C. T., Zhing, Z., “Advanced Experimental and Simulation Techniques for Analysis of Dynamic Responses during Drop Impact”, Electronic Components and technology Conference, Las Vegas, Nevada, pp. 1088-1094, June 1-4, 2004.

Tee, T. Y. , Hun Shen Ng, Chwee Teck Lim, Eric Pek , Zhaowei Zhong , “Board Level Drop Test and Simulation of TFBGA Packages for Telecommunication Applications”, 53rd Electronic Components and Technology Conference, pp. 121-129, 2003.

Tan, L., Ang, C., Tan, V., Zhang, X., “Modal and Impact Analysis of Modern Portable Electronic Products”, Electronic Components and Technology Conference, pp. 645-653, 2005.

Tasooji, A., Ghaffarian, R., Rinaldi, A., “Design Parameters Influencing Reliability Of CCGA Assembly: A Sensitivity Analysis”, Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronics Systems, pp. 1056-1063, 2006.

Tee, T. Y. , Hun Shen Ng, Chwee Teck Lim, Eric Pek , Zhaowei Zhong , “Board Level Drop Test and Simulation of TFBGA Packages for Telecommunication Applications”, 53rd Electronic Components and Technology Conference, pp. 121-129, 2003.

Tee, T., Luan, J, et al., “Advanced Experimental and Simulation Techniques for Analysis of Dynamic Responses during Drop Impact”, Electronic Components and Technology Conference , pp. 1088-1094, 2004.

Terashima, S. and Tanaka, M., “Thermal Fatigue Properties of Sn-1.2Ag-0.5Cu- xNi Flip Chip Interconnects”, Materials Transactions, Volume 45, Number 3, pp. 681–688, 2004b.

Terashima, S., Takahama, K., Nozaki, M., and Tanaka, M., “Recrystallization of Sn Grains due to Thermal Strain in Sn-1.2Ag-0.5Cu-0.05Ni Solder”, Materials Transactions, Volume 45, Number 4, pp. 1383–1390, 2004a.

Thurner, P., Erickson, B., Schriock, Z., et al., “High-Speed Photography of Human Trabecular Bone during Compression”, Materials Research Society Symposium Proceedings, Vol 874, 2005.

Tian, G, Liu, Y., Lall, P., Johnson, W., et al., “Corner Bonding Of CSPs: Processing And Reliability”, Proceedings of the 2003, APEX Conference, Anaheim, CA,” March 31-April 2, pp. S02-1-1 to S02-1-8, 2003.

Tian, G., Liu, Y., Lall, P., Johnson, W., Suhling, “Drop-Impact Reliability of Chip-Scale Packages in Handheld Products”, ASME International Mechanical Engineering Congress and RD & D Exposition, Washington, D.C., November 15-21, 2003.

Tiwari, V., Williams, S., Sutton, M., McNeill, S., “Application of Digital Image Correlation in Impact Testing”, Proceedings of the 2005 SEM Annual Conference and Exposition on Experimental and Applied Mechanics, June 7-9, 2005.

Tribula, D., Grivas, D., Frear, D., Morris, J., Journal of Electronic Packaging, 1989, 111, pp. 83-89.

Wang, B., Yi, S., “Dynamic Plastic Behavior of 63wt% Sn37%Pb Eutectic Solder under High Strain Rates”, Journal of Materials Science Letters 21, pp. 697-698, 2002.

Wang, S., Liu, C., “Study Of Interaction Between Cu-Sn And Ni-Sn Interfacial Reactions By Ni-Sn3.5Ag-Cu Sandwich Structure”, Journal of Electronic Materials, Vol. 32, No. 11, pp. 1303-1309, 2003.

Wolverton, A., “Brazing and Soldering”, 13, pp. 33, 1987.

Watanabe, K., Koseki, J., Tateyama, M., “Application of High-Speed Digital CCD Cameras to Observe Static and Dynamic Deformation Characteristics of Sand”, Geotechnical Testing Journal, Vol. 28, No. 5, 2005.

Wilson, E.L., Penzien, J., “Evaluation of Orthogonal Damping Matrix, Int Jour. Num. Meth. in Engg, Vol. 4, pp. 5-10, 1972.

Wong, E. H., Lim, C. T., Field, J. E., Tan, V. B. C., Shim, V. P. M., Lim, K. T., Seah, S. K. W., “Tackling the Drop Impact Reliability of Electronic Packaging”, ASME International Electronic Packaging Technical Conference and Exhibition, July 6 -11, Maui, pp. 1 – 9, 2003.

Wong, T., Fenger, H., "Vibration and Thermo-Mechanical Durability Assessments in Advanced Electronic Package Interconnects", Electronic Components and Technology Conference, pp. 1080-1087, 2004.

Wu J., "Global and Local Coupling Analysis for Small Components in Drop Simulation", 6th International LSDYNA Users Conference, pp. 1117 - 1126, 2000.

Wu, Jason, Goushu Song, Chao-pin Yeh, Karl Wyatt, "Drop/Impact Simulation and Test Validation of Telecommunication Products", Intersociety Conference on Thermal Phenomena, pp. 330-336, 1998.

Xie, D., Minna Arra, Dongkai Shangkai, Hoang Phan, David Geiger and Sammy Yi, "Life Prediction of Lead free Solder Joints for Handheld Products", Presented and published at Telecom Hardware Solutions Conference, Doubletree Hotel, Plano, Texas, USA, May 15-16, 2002.

Xie, D., M. Arra, S. Yi and D. Rooney, "Solder Joint Behavior of Area Array Packages in Board Level Drop for Handheld Devices", Electronic Components & Technology Conference, pp. 130-135, 2003.

Xie, D., Rooney, D., Geiger, D., Shangguan, D., "A Comparative Study Of Drop Test Performance Of Fine Pitch BGA Assemblies Using Pb-Free And Tin-Lead Solders", Electronic Components and Technology Conference, pp. 865-874, May 2006.

Xu, L., Pang, H., "Combined Thermal and Electromigration Exposure Effect on SnAgCu BGA Solder Joint Reliability", Electronic Components and Technology Conference, pp. 1154-1159, May 2006.

Yaeger, E., "Technical Forum: Beyond Flip-Chip, Underfills Enhance CSP Reliability", Chip Scale Review, March 2001.

Yang, W., Messle, R., "Microstructure evolution of eutectic Sn-Ag solder joints", Journal of Electronic Materr., Vol. 23, No. 8, pp. 767-772, 1994.

Yen, G.Y., Kuo-Chung Lin, "Wavelet packet feature extraction for vibration monitoring", Proceedings of the IEEE International Conference on Control Applications, Vol.2, Pp. 1573 - 1578, 1999.
Yogel, D., Grosser, V., Schubert, A., Michel, B., "Micro-DAC Strain Measurement for Electronics Packaging Structures", Optics and Lasers in Engineering, Vol. 36, pp. 195-211, 2001.

Young, S., "Underfilling BGA and CSP for Harsh Environment Deployment", Proceedings of the 1999 International Conference on High Density Packaging and MCMs, Denver, CO., April 7-9, 1999.

Zhang, F., Li, M., Xiong, C., Fang, F., Yi, S., “Thermal Deformation Analysis of BGA Package by Digital Image Correlation Technique”, Microelectronics International, Vol. 22, No. 1, pp. 34-42, 2005.

Zhang, Y., Shi, X., Zhou, W., “Effect of Hygrothermal Aging on Interfacial Reliability of Flip Chip on Board (FCOB) Assembly”, Electronic Packaging Technology Conference, pp. 404-409, 2004.

Zhao, J., Garner, L., “Mechanical Modeling and Analysis of Board Level Drop Test of Electronic Package”, Electronic Components and Technology Conference, pp. 436-442, 2006.

Zhao, Y., Basaran, C., et al., “Thermo-Mechanical Behavior Of BGA Solder Joints Under Vibrations: An Experimental Observation”, Inter. Society Conference on Thermal Phenomena, pp. 349-355, 2000.

Zhou, P., Goodson, K. E., “Sub-pixel Displacement and Deformation Gradient Measurement Using Digital Image-Speckle Correlation (DISC)”, Optical Engineering, Vol. 40, No. 8, pp. 1613-1620, August 2001.

Zhu, L., “Submodeling Technique for BGA Reliability Analysis of CSP Packaging Subjected to an Impact Loading”, InterPACK Conference Proceedings, pp. 1401-1409, 2001.

Zhu, L., “Modeling Technique for Reliability Assessment of Portable Electronic Product Subjected to Drop Impact Loads”, 53rd Electronic Components and Technology Conference, pp. 100-104, 2003.

Zhu, L., Marcinkiewicz, W., “Drop Impact Reliabiltiy Analysis of CSP Packages at Board and Product System Levels through Modeling Approaches”, Proc of ITherm 2004, Las Vegas, pp. 296-303, June 2004.

Zhu, L., Williams, R., “Plastic Strain Based Criterion For Reliability Assessment of CSP Packages Subjected to Dynamic Shock Loads”, InterPACK Conference Proceedings, No. 73059, July 17-22, 2005.