Fabrication and Characterization of High Temperature P-channel 4H-SiC MOSFETs

by

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A dissertation submitted to the Graduate Faculty of
Auburn University
in partial fulfillment of the
requirements for the Degree of
Doctor of Philosophy

Auburn, Alabama
December 10, 2022

Keywords: MOSFETs, CMOS, Hall Measurements,
Interface trap, Sustainable annealing, Scattering

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Abstract

Power devices are of paramount relevance with the emergence of greener technology to utilize renewable energy sources. Conventional Si devices are reaching their performance limit due to Silicon's physical limitation of low band gap and low break down voltage. In this regard, wide band gap semiconductor mainly silicon carbide (4H-SiC) is most promising in producing high-performance power devices. 4H-SiC power MOSFETs and Schottky diodes are already commercialized due to their ability to withstand high voltage and lower power consumption. Additional to the vertical power MOSFETs and other discrete devices, high-performing integrated circuits (IC) made of 4H-SiC would be very useful in applications such as space exploration and electric vehicles. An IC uses complementary metal-oxide semiconductor technology (CMOS) that needs both n- and p-channel MOSFETs. The operation of a MOSFET largely depends on the oxide-semiconductor interface. Therefore, rigorous study of both n- and p-type 4H-SiC/SiO_2 interface is necessary to produce high-performing 4H-SiC ICs. The research on p-channel 4H-SiC MOSFETs is few compared to the rigorous study of n-channel 4H-SiC MOSFETs over the past decade. Because of this, the focus of this thesis has been to study the p-type 4H-SiC/SiO_2 interface and improve p-channel MOSFET channel conduction at high temperatures.

The performance of 4H-SiC MOSFETs is yet to reach its full potential. The operation is mainly limited by low channel mobility due to the presence of a large number of interface traps at the oxide semiconductor interface. Interfacial traps capture charge carriers and increase scattering at the channel, that intern lowers channel conductivity. In this thesis, several post-oxidations annealing treatments were incorporated to reduce a large number of interface traps and make highly conductive n- and p-channel MOSFETs, keeping the focus on the p-type interface mainly. After finding the best annealing method that is nitric oxide annealing (NO), the channel transport

properties of electrons and holes are studied by Hall measurements following the fabrication of NO annealed 4H-SiC n- and p-channel 4H-SiC MOSFETs. Furthermore, the principal channel scattering mechanisms are distinguished using the application of body bias and temperature-dependent Hall analysis. For both kinds of MOSFETs, Coulomb scattering is seen to be dominant in the weak inversion region. In the strong inversion region phonon and surface roughness scattering are prevailing for n-channel MOSFET, whereas for p-channel, surface roughness scattering plays a crucial role. The power law dependence of mobility on the transverse electric field for n- and p-channel 4H-SiC MOSFETs are found. The importance of body bias and temperature-dependent study that can predict the behavior of MOSFETs with different substrate doping is presented.

In the next phase of work, an alternative annealing treatment was tried to find out to replace toxic and expensive NO. For this purpose, several post oxidation nitrogen annealing treatments were carried out to observe their effect on device performance. N- and p-type 4H-SiC MOS capacitors are fabricated and characterized under temperature and bias. X-ray photoelectron spectroscopy is performed to quantify nitrogen at the interface. Additionally, the role of nitrogen at the interface is explained using density functional theory (DFT) calculation through collaboration with Auburn's theoretical condensed matter group.

The results presented here regarding electron and hole channel transport in n- and p-channel 4H-SiC MOSFETs play a crucial role in 4H-SiC IC fabrication as well as provide insights into improving oxide semiconductor interface in the fabrication of 4H-SiC power MOSFETs.

Acknowledgments

This thesis is based on the research I conducted under the guidance of Prof. Sarit Dhar at Auburn University. My time as a Ph.D. student was one of the most delightful and fulfilling experiences of my life. I still have the impression that I started my Ph.D. a few months ago. Time goes by so quickly! The amazing people that came into my life and assisted me in various ways are the sole reason for the excellent experience I've had over the last five years. It would have been difficult to finish this thesis without their affection and support. As a result, I'd like to use this time to express my gratitude to these wonderful people for their generosity, love, support, and encouragement.

Before all else, I want to express my profound gratitude to my advisor Prof. Sarit Dhar for his guidance, friendship, and excellent supervision. He has been incredibly generous to me. He was always willing to assist and advise me anytime I needed it. While doing research with him and attending his lectures, I was lucky to get a significant amount of knowledge and skills from him. Thank you, Dr. Dhar, for being so patient with me and patiently listening and answering all my stupid questions. Thank you for your encouragement and support in allowing me to travel, attend conferences and workshops, and connect with researchers and scientists.

Apart from my advisor, I owe a debt of gratitude to Dr. Ayayi C. Ahyi for his unending assistance and insightful talks during the study program. Mrs. Tamara Isaacs-Smith and Mr. Max Cichon deserve special gratitude for their tremendous support with experimental settings. It is hard to count how many times some instrument broke and I needed their help in fixing it. Thank you for all your help in training and for being patient with me.

I would like to express my profound gratitude to Prof. Leonard Feldman for his enormous help and support for my research. A special thanks to Prof. Minseo Park, Prof. Marcelo Kuroda, Prof. David Maurer, and Prof. Allen Landers for encouragement, support and always helping me with my academic and professional concerns.

Special gratitude to all my committee members Dr. Sarit Dhar (advisor), Dr. Marcelo A. Kuroda, Dr. Ayayi Ahyi, Dr. Ryan Comes, Dr. Laurent Guzzoto, and Dr. Willis Hames (university reader) for their valuable time and effort to assess my dissertation and participate in my defense.

I owe a debt of gratitude to the Physics department's staff members for patiently aiding me with a tremendous amount of paperwork and financial matters. Many thanks to Mrs. Freddie Killian, Mrs. Mary Prater, Mrs. Jennifer Morris, Mrs. Glenda Stroud, and Mr. David M. Patrick for always being willing to help me whenever I needed it, and for being so good to me.

I am enormously grateful to all my teachers who taught me at various stages of my life since my childhood. Without their help and care, I would never have made it this far.

I am very grateful to my friends and colleagues, Dr. Isanka Jayawardhena, Dr. Sunil Uprety, Dr. Asanka Jayawardena, Dr. Yongju Zheng, Mr. Arka Sardar, Dr. Hengei Gu, Dr. Suresh Thapa, Dr. Rajendra Poudel, Dr. Lu wang, Dr. Kosala Yapabandara, Dr. Min Prasad Khanal, and Dr. Vahid Mirkhani for their friendships and strong teamwork during my Ph.D. at Auburn University that helped me grow both personally and professionally.

I shall be eternally grateful to my wonderful parents and fabulous sister for having faith and trust in me and my dreams. Without their sacrifice, kindness, and unwavering love, I would be nothing. Thank you so much from the bottom of my heart, for always being at my side. I'd also like to thank my in-laws' parents for their unconditional support. Last but not least my gratitude

goes to Neha, my wonderful wife, for her continuous support and friendship during my doctoral studies and the production of this thesis. I would not have been able to do it without your unfailing love. Thank you.

This work has been financially supported by the US Army Research Laboratory (grant ARMY-W911NF-18-2-0160) and the US Department of Energy (subcontracted to National Renewable Energy Laboratory, grant NREL-AHL-9-92632-01). Additionally, I acknowledge the support from Auburn University for letting me use all the resources.

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Chapter 1

Introduction

1.1. Silicon Carbide in power electronics

In today's world with the rise of greenhouse gas emissions, it is critical to search out new energy-efficient technology that can minimize fossil fuel consumption and reduce global warming. Electrical transmission using conventional Silicon (Si) technology wastes a significant amount of power in the conversion from AC (alternating current) to DC (direct current) and vice versa. Si has been the most widely used semiconductor in electronic applications due to its abundance and accessibility for over a century. However, the performance of Si technology is reaching its potential limit due to the material properties of Si such as low band gap (1.1 eV) and low breakdown voltage.

To overcome the limitations of Si, wide band gap (WBG) semiconductors play a crucial role in power devices and technological applications. Among others (Gallium Nitride, Gallium oxide, etc.), silicon carbide (4H-SiC), [1], [2] is the most promising wide bandgap Semiconductors that have the potential to replace Si in high-power and high-temperature electronic application areas.

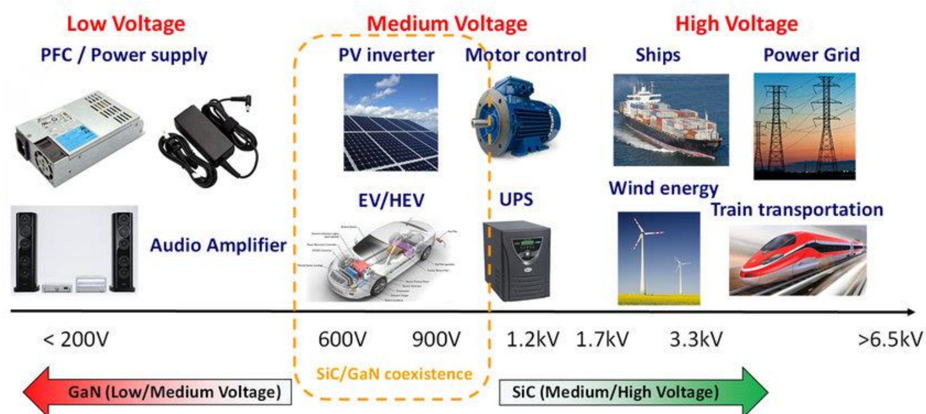

Figure 1.1: Application areas of WBG semiconductors plotted against voltage range and power ratings [3]

4H-SiC has a bandgap of 3.3 eV which is three times higher than Si and produces more energy-efficient devices for power transmission and storage. It is the only wide band gap semiconductor known to date where both n- and p-type doping modulation is possible through ion implantation or epitaxial doping. Other notable characteristics include the presence of a native oxide (SiO_2), several polytypes, and a high critical electric field. Due to its superior material qualities and availability 4H-SiC is employed in fundamental components in current electronic systems such as DC to AC inverters, AC to DC rectifiers, AC to AC, DC to DC converter circuits, etc. Furthermore, 4H-SiC is very promising in harsh environment application areas such as electric/hybrid vehicles, renewable energy sources, transportation, power supply, spacecraft, motor control, traction, electric power transmission, etc. as indicated in Figure 1.1.

1.2. 4H-SiC Power MOSFET

One of the most important applications of 4H-SiC, is its use in vertical power metal oxide semiconductor field effect transistors (MOSFETs), Insulated gate bipolar transistors (IGBTs), Schottky barrier diode (SBD), pin diode, etc. A vertical power MOSFET is highly desirable in high-power electronics due to its blocking capability of thousands of volts. An n-drift region is used for this purpose. Additionally, a power MOSFET is more favorable as it has significantly low power loss, smaller size, and faster switching applications compared to an IGBT. Two kinds of 4H-SiC vertical MOSFETs have been mainly studied that are a double diffused MOSFET or DMOSFET and a U-shaped MOSFET called UMOSFET or trench MOSFET.

Figure 1.2 (a) shows the structure of commercially available D-MOSFETs with a p-base region, n+ source and drain regions, and n-drift region. The channel here is defined as the junction difference between the n+ source and p-base region. The n- drift region is designed to block high voltages. The value of drift resistance R_D depends on the semiconductor material properties and

thickness. The electric field as shown here is triangular, which is maximum near the drift and substrate junction. The maximum blocking voltage is determined by the critical electric field (E_C) that relies on the maximum depletion width (W_D) and doping concentration (N_D) of the drift region.

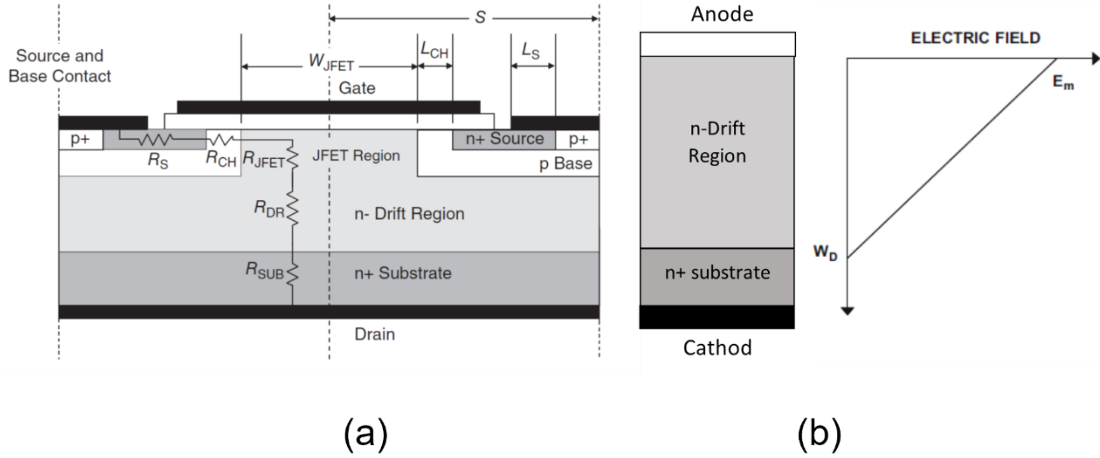

Figure 1.2: (a): Schematic diagram of D-MOSFET. The total ON resistance is a summation of the contact resistance R_S, channel resistance R_{CH}, JFET resistance R_{JFET}, Drift resistance R_{DR}, and substrate resistance R_{SUB}. (b) The drift region and the variation of the electric field are shown. The amount of blocking voltage depends on the thickness and doping concentration of this region [4].

The specific resistance of the ideal drift region is given by:

$$R_{on,sp} = \frac{W_D}{e\mu_n N_D} \tag{1.1}$$

The maximum depletion width (W_D) at the breakdown voltage (V_B) is given by,

$$W_D = \frac{2V_B}{E_C} \tag{1.2}$$

The breakdown voltage is related to the doping concentration of the drift layer [2],

$$N_D = \frac{\epsilon_S E_C^2}{2eV_B} \tag{1.3}$$

Substituting eq. 1.2 and 1.3 in eq. 1.1, the specific on-resistance can be expressed as,

$$R_{on,sp} = \frac{4V_B^2}{\epsilon_S \mu_n E_C^3} \tag{1.4}$$

Here, ϵ_S is the semiconductor dielectric constant, and e is the electron charge. E_c is the critical electric field at the onset of breakdown, and μ_n is the carrier mobility. $R_{on,sp}$ ultimately determines the energy loss in conduction. It can be reduced by increasing μ_n or E_C. However, it can be seen from eq. 1.4 that, $R_{on,sp}$ increases with the increase of V_B. A high breakdown voltage is desirable to obtain high blocking voltage capability in a semiconductor. On the other hand, a low $R_{on,sp}$ is needed for lower power loss. Therefore, there is a trade-off in $R_{on,sp}$ and V_B. The denominator in eq. 4 is known as Baliga's figure of merit (BFOM) which has the most significant contribution to determining the value of $R_{on,sp}$. Table 1.1 [1], [2] depicts the material properties

Materials parameters	Si	GaAs	4H-SiC	GaN	β-Ga_2O_3	Diamond
Bandgap (eV)	1.1	1.43	3.26	3.4	4.3-4.9	5.5
Dielectric constant, $\boldsymbol{\epsilon_s}$	11.8	12.9	9.7	9	10	5.5
Critical field, E_C (MV/cm)	0.3	0.4	2.5	3.3	8	10
Thermal conductivity (W/cm K)	1.5	0.5	4.9	2.3	0.1-0.3	20
Electron mobility, $\boldsymbol{\mu_n}$ (cm^2/V s)	1480	8400	1000	1250	300	2000
BFOM ($\boldsymbol{\epsilon_S \mu_n E_C^3}$) relative to Si	1	14.7	317	846	3214	24660

Table 1.1: Material properties of 4H-SiC [1], [2] in comparison with the most popular semiconductors such as Si, β-Ga_2O_3 [5], etc.

of 4H-SiC in comparison to other popular semiconductors. It can be noted that Wide band gap semiconductors have higher breakdown voltage, thermal conductivity, and BFOM, which makes them more suitable for power device applications. 4H-SiC is now the most technologically advanced WBG semiconductor, due to exceptional material characteristics and the availability of high-quality epitaxial wafers. Even though 4H-SiC MOSFETs have been successfully marketed in the power electronics market [6]–[8] their performance is limited by low channel mobility and

a high density of near-interface states at the SiO_2/4H-SiC interface. Figure 1.3 shows specific on-resistance versus breakdown voltage at 25 ºC for the most recent commercially available 4H-SIC MOSFETs. 4H-SiC has a higher breakdown voltage due to a high band gap which is highly desirable for power device applications and lower energy consumption.

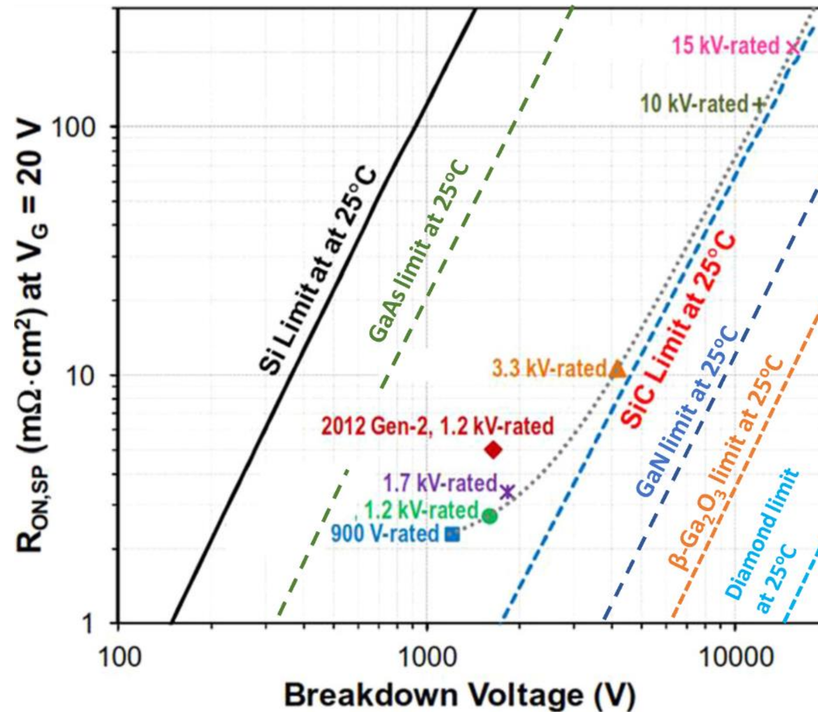

Figure 1.3: Comparison of Specific on-resistance with breakdown voltage for 4H-SiC with other popular semiconductors. Along with the ideal curves, actual 4H-SiC data points are shown for Gen 1, Gen 2, and Gen 3 4H-SiC MOSFETs fabricated by Wolfspeed Inc. [6].

1.3. Physical properties of 4H-SiC

The fast advancement in SiC growth and device technology increase the semiconductor market's expansion day by day. A tremendous amount of research on SiC is being carried out. The physical properties of SiC are essential academic topics as well as critical criteria for effective device simulation. In this section, the basic properties of SiC are discussed briefly.

1.3.1. Crystal structure of 4H-SiC

Silicon carbide (SiC) is an IV-IV compound having a rigid stoichiometry of 50% silicon (Si) and 50% carbon (C). Si ($3s^2 3p^2$) and C ($2s^2 2p^2$) atoms are both tetravalent, with four valence electrons in their outermost shells. To construct a SiC crystal, Si and C atoms are tetrahedrally bonded with covalent bonds with a very high Si–C bond energy (4.6 eV) by sharing the outermost electrons in their orbitals. A high chemical bond energy allows the SiC to present in different forms of polytypes through stacking sequences without changing the chemical composition. To represent polytypes, the number of Si-C bilayers and the type of crystal structure (C for cubic, H for hexagonal, and R for rhombohedral) are used. The most popular and extensively researched

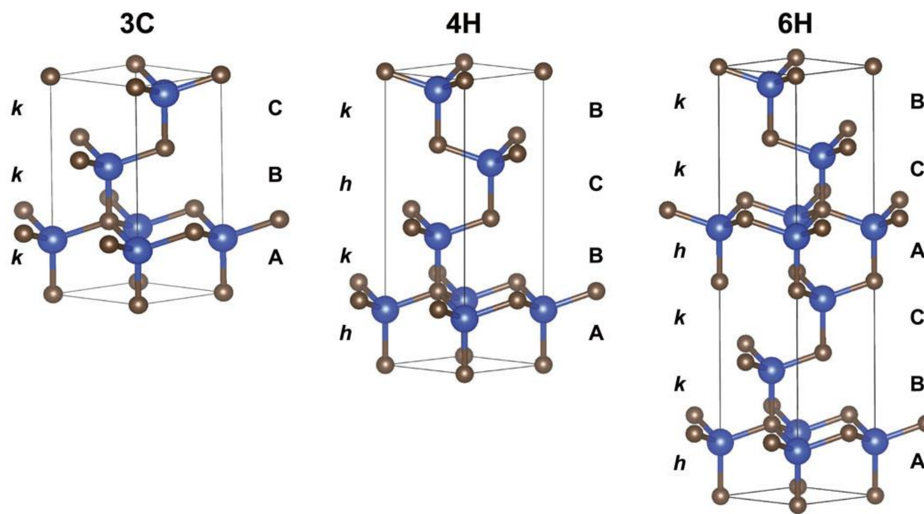

Figure 1.4: The most popular SiC polytypes are 3C-SiC, 4H-SiC, and 6H-SiC [9], blue balls represent Si and grey balls represent carbon atoms.

polytypes are 3C-SiC, 4H-SiC, and 6H-SiC, the unit cells of which are shown in Figure 1.4. Here, A, B, and C represent the potentially occupied sites in a hexagonal close-packed structure. Through these sites, 3C-SiC is described by the repeating sequence ABC, and 4H- and 6H-SiC can be described by ABCB (or ABAC) and ABCACB, respectively. The chemical and electronic properties of these polytypes vary significantly as listed in Table 1.2 [1].

Properties	3C-SiC	4H-SiC	6H-SiC
Bandgap (eV)	2.36	3.26	3.02
Dielectric constant, $\boldsymbol{\epsilon_s}$			
$\boldsymbol{\epsilon_s}$ ⊥ to c-axis	9.72	9.76	9.66
$\boldsymbol{\epsilon_s}$ ∥ to c-axis	9.72	10.32	10.03
Critical field, E_C (MV/cm)			
$\boldsymbol{E_C}$ ⊥ to c-axis	1.4	2.2	1.7
$\boldsymbol{E_C}$ ∥ to c-axis	1.4	2.8	3.0
Electron mobility, $\boldsymbol{\mu_n}$ (cm^2/V s)			
$\boldsymbol{\mu_n}$ ⊥ to c-axis	1000	1020	450
$\boldsymbol{\mu_n}$ ∥ to c-axis	1000	1200	100
Hole mobility, $\boldsymbol{\mu_p}$ (cm^2/V s)	100	120	100
BFOM ($\boldsymbol{\epsilon_S \mu_n E_C^3}$)			
n-type ∥ to c-axis	61	626	63
p-type ∥ to c-axis	2	25	19

Table 1.2: Physical properties of different polytypes of SiC relative to c-axis <0001> [2]

The quantity BFOM (Baliga's figure of Merit) correlates breakdown electric field (E_c) and mobility (μ_n) through factor $\epsilon_s \mu_n E_c^3$. Due to its higher bandgap, higher electron, and hole mobility, and higher BFOM, 4H-SiC is extensively employed in power electronics. Depending on the orientation of miller indices SiC may have different faces. Figure 1.5 shows a schematic diagram of bond configuration and major crystal planes. The "Si-face" is represented as the (0001) face as Si atoms are directed along the <0001> (c-axis). Whereas $(000\overline{1})$ is represented as "C-face" as C atoms are directed along <$000\overline{1}$> axis. The other faces are known as $(1\overline{1}00)$ face

called “m-face”, and $(11\bar{2}0)$ face or “a-face”. It can be noted from Table 1.2 that the electronic properties and surface energies vary substantially for different faces.

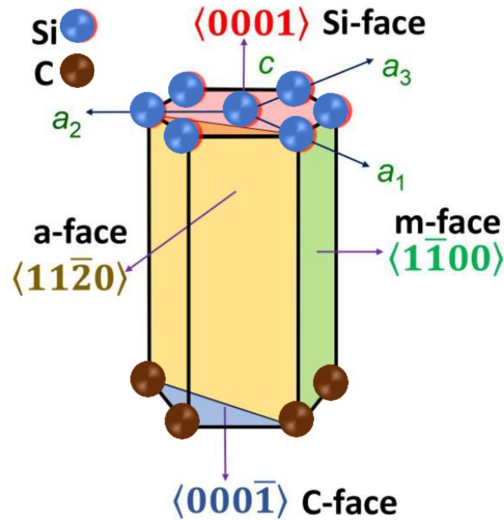

Figure 1.5: Different Crystal faces in 4H-SiC. (a) Si and C terminated surface. (b) The Si-face is terminated by Si atoms (blue balls) and the C-face by C atoms (gray balls). The other non-polar faces, e.g., a-face and m-face, have an equal number of Si and C atoms.

1.3.2. Band structure of 4H-SiC

Given the demands and popularity of 4H-SiC, the band structure is discussed below in Figure 1.6. All SiC polytypes have an indirect bandgap [1]. The conduction band minima are located at M point ant the valence band maxima appear at Γ point in the Brillouin zone. The total number of conduction band minima in the first Brillouin zone (Mc) for 4H-SiC is 3. The effective masses of electrons and holes depend on the curvature of conduction band minima and valence band maxima as listed in Table 1.3 [1].

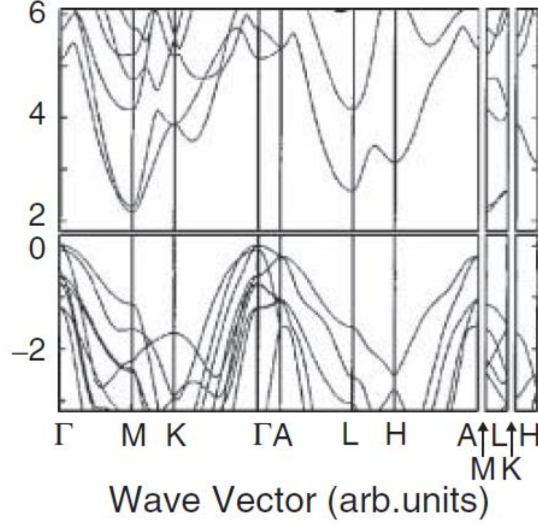

Figure 1.6: Electronic band structure of 4H-SiC [1]

Effective Masses		Experiment	Theory
Electron	$m_{\parallel}$	0.33	0.31
	$m_{\perp}$	0.42	0.40
Holes	$m_{\parallel}$	1.75	1.62
	$m_{\perp}$	0.66	0.61

Table 1.3: Effective masses of electrons and holes in 4H-SiC [1]

1.3.3. Doping and impurity

One of the major benefits of SiC is that it can be doped both n- and p-type through ion implantation or epitaxial doping. N-type doping can be performed by implanting a group V impurity such as nitrogen or phosphorus into pure SiC. An epitaxial n-type conductivity is obtained by introducing nitrogen gas into the growth ambient [1]. Similarly, p-type conductivity of SiC is

achieved by implanting Al or introducing Al impurity during the SiC growth process, through an aluminum-containing compound such as trimethylaluminum (TMA: $Al(CH_3)_3$) to the SiC source [1]

1.3.4. Bulk to channel Mobility for 4H-SiC

Depending on the type and amount of doping the mobilities (bulk and channel) can be different. In Table 1.4, the ratio of the channel to bulk mobilities is given for n- and p-channel MOSFETs fabricated on a moderately doped substrate. When compared to the bulk, channel mobilities are noticeably lower. As a result, there is a lot of room for device engineering to improve channel mobilities.

Carriers	Bulk Mobility (cm^2/vs)	Channel Mobility (cm^2/vs)	Channel/Bulk
Electrons (μ_e)	900 [1]	40 [1]	1/22
Holes (μ_h)	120 [1]	17 [10]	1/7

Table 1.4: The bulk and channel mobilities of 4H-SiC MOSFETs fabricated on moderately doped substrates ($6 \times 10^{15}\ cm^{-3}$) [1].

1.4. Motivation for studying p-channel MOSFET

As described above, the 4H polytype of SiC (4H-SiC) is a compound semiconductor with a wide band gap of 3.3 eV, a 10X higher breakdown electric field, and a 3X higher thermal conductivity than conventional Si. These properties make 4H-SiC very attractive for high power, high frequency, and high-temperature electronics. Vertical 4H-SiC power metal-oxide semiconductor-field-effect transistors (MOSFETs) are currently being widely adopted for high

voltage power conversion in hybrid/electric vehicles [11], solar and wind energy generation [12], and various high-temperature sensor applications [13]. While these devices are enabling significant advances for next-generation energy-efficient power systems, the development of an integrated circuit (IC) technology (as opposed to discreet) based on 4H-SiC is relatively immature. A high-performance 4H-SiC IC technology operating at temperatures >300 °C [14]–[16] is very attractive as it will enable various functions that are not accessible to conventional silicon or silicon on insulator (SOI) ICs [17], [18].

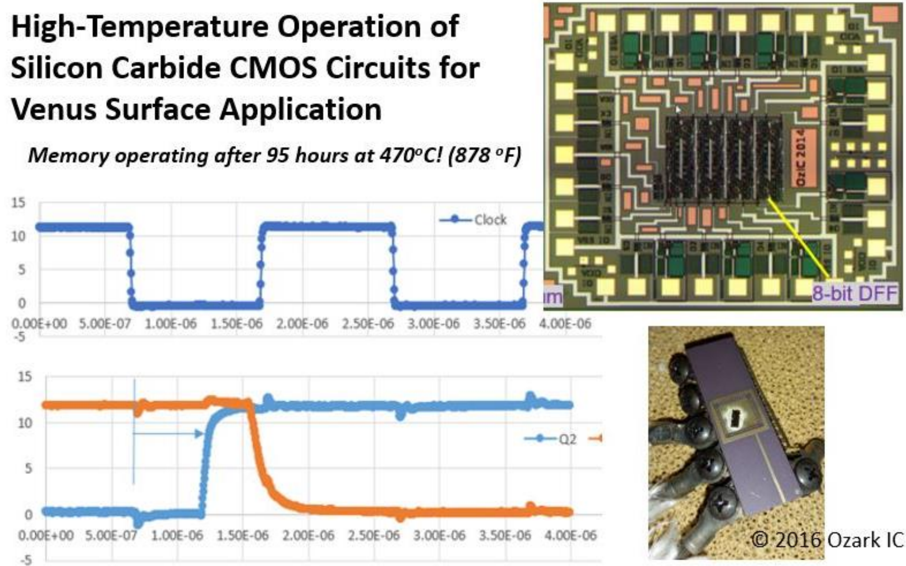

Figure 1.7: An example of the recent development of 4H-SiC IC technology demonstrates its ability to survive and perform in the extreme environment making it useful for harsh environment application areas such as space exploration, transportation, renewable energy sectors, etc. [15].

One of the many recent research demonstrates that 4H-SiC ICs can survive and operate at 470 °C as shown in Figure 1.7 [15]. In Si, complimentary-metal-oxide-semiconductor (CMOS) technology is the most widely used technology for very largescale integration (VLSI) due to high noise immunity and low static power consumption [19]. The formation of native oxide SiO_2 and the ability to be doped either *p*- or *n*-type also motivates a lateral CMOS IC technology

in 4H-SiC for harsh environments. The first commercial SiC CMOS process was announced by Raytheon Inc. [20]. In a CMOS inverter, the input voltage is connected to the common gate connection of NMOS and PMOS. When the input voltage is low, the PMOS transistor turns ON, whereas the NMOS remains off due to a lower gate voltage than the threshold. Similarly, when the input voltage is high, the NMOS turns on, and PMOS remains OFF. For high-temperature, low-power CMOS applications, the performance of both n- and p-channel 4H-SiC MOSFET is crucial.

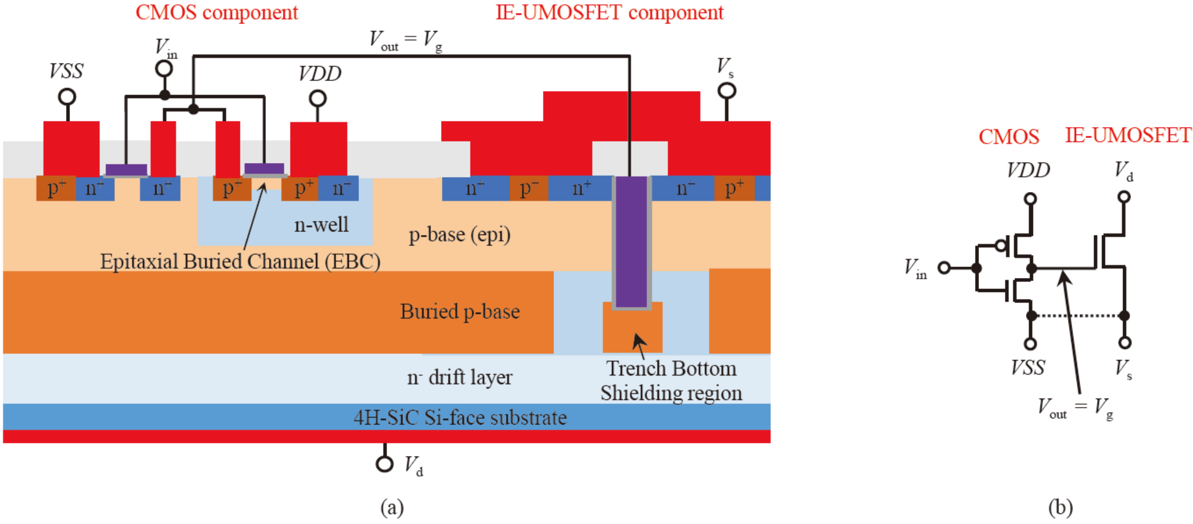

Figure 1.8: (a) Schematic cross-section of the monolithic 4H-SiC power IC (b) The analogous circuit [21].

In high power application areas such as gate drivers a low voltage CMOS device often needs to be integrated with a high voltage 4H-SiC power MOSFETs. This integration requires additional shielding circuitry for the well-being of the low-voltage device. On the other hand, monolithic integration of power MOSFETs' gate drivers on the same chip (Figure 1.8) [21], the so-called power integrated circuit (IC) can be very energy efficient that allows high-speed switching, smaller

device size, reduction of the parasitic effects in the interconnections, etc. Therefore, in addition to a highly performed n-channel MOSFET, its p- counterpart also needs to be significantly advanced.

Over the past decade, n-channel 4H-SiC transistors, with electrons as current carriers have been investigated extensively, but research on p-channel (where holes are the channel carriers) is relatively sparse [22], [23]. The heart of a MOSFET is the interface between the dielectric (oxide) and the semiconductor. As the channel forms within ~5 nm of the surface, the transport of carrier electrons or holes is very sensitive to defect states as well inhomogeneities such as different scattering centers. Therefore, control of the nano-scale chemical composition and structure is critical. For n-channel devices, it has been established that nitridation of the SiO_2/4H-SiC interface by processes such as post oxidation nitric oxide annealing (NO POA) is necessary for acceptable device performance. Nitridation lowers the interface state density (D_{it}) and improves channel conductivity yielding maximum field-effect electron mobilities of ~35-40 cm^2/Vs for n-channel 4H-SiC MOSFETs [24]. In contrast, the role of nitrogen in the p-channel is not well established. Additionally, only sparse data is available on the high-temperature characteristics, threshold voltage control, and bias-temperature instabilities of p-channel 4H-SiC MOSFETs. Consequently, the focus of this thesis has been on hole transport in 4H-SiC p-channel MOSFET alongside the process implication on electron transport in 4H-SiC n-channel MOSFET.

1.5. Challenges at p-type interface

1.5.1. Oxidation and interface trap density

In comparison to other wide bandgap materials, 4H-SiC has the distinct benefit of being the only compound semiconductor that can be thermally oxidized. A thermal oxidation yields high-quality SiO_2 to be used as the gate dielectric for device fabrication. However, the release of C

atoms that are present in 4H-SiC, degrades the oxide qualities. A thermal oxidation process can be expressed by a simple equation,

$$SiC + \frac{3}{2}O_2 \rightarrow SiO_2 + CO \quad (1.5)$$

Using the Si density in SiC, the amount consumed during thermal oxidation of SiC can be calculated to be 46%. Depending on the SiC faces (Si, C, a, m, and c) the oxidation rate varies [1]. Details on the oxidation process can be found in [25]. During thermal oxidation, most of the C atoms leave in the form of carbon monoxide (CO) gas.

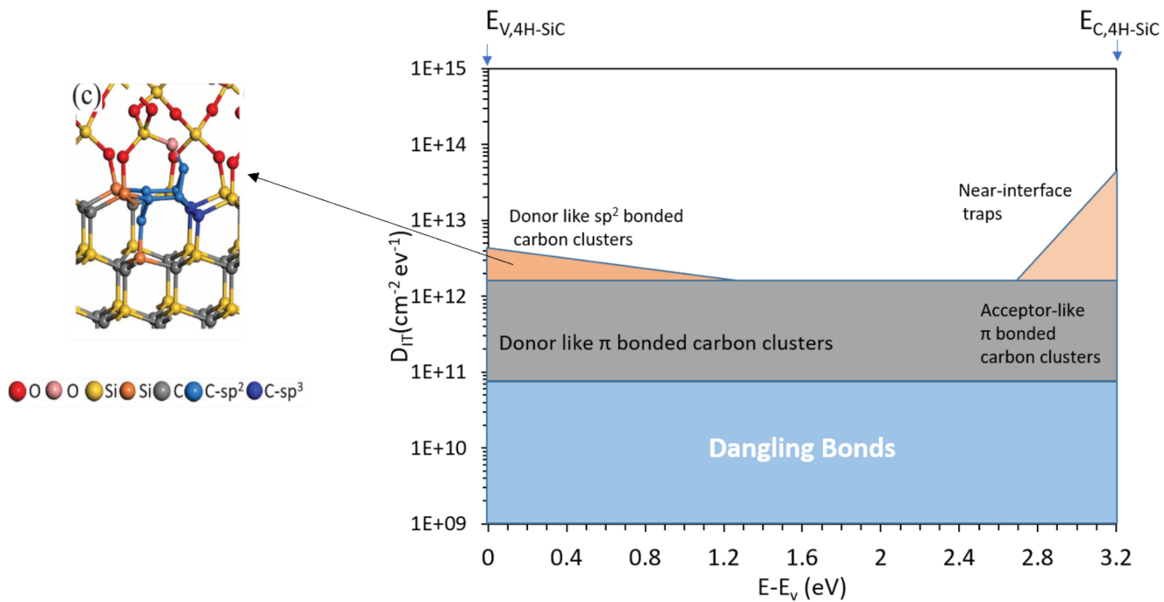

Figure 1.9: Schematic diagram [26] of interface trap distribution in the 4H-SiC band gap. E_C and E_V represent conduction and valence band edges. The different kinds of traps are π- bonded carbon clusters [27], Dangling bonds [28], and Sp^2-bonded carbon clusters [29] near the valence band edge that mostly affects pp-channel MOSFET operation.

However, a small amount of carbon diffuses into the bulk of SiC and some amount of carbon atoms remain at the oxide-semiconductor interface leading to near interface traps (D_{it}) that degrade device quality. In addition to the carbon atoms, different factors can contribute to the D_{it} as shown in Figure 1.9. Dangling bonds or unsatisfied carbon atoms create states that are present across the whole 4H-SiC bandgap. Next, π bonded carbon clusters play a major role in forming D_{it}. These

traps can be donor or acceptor-like depending on their position in the bandgap. The most important D_{it} that affects a MOSFET performance are the ones present near the conduction band edge (E_C) are called near interface traps which can be carbon dimers and carbon interstitials that degrade the performance of an n-channel MOSFET. Similarly for p-channel MOSFET, the donor-like sp^2 bonded carbon clusters present near the (E_V) play the most crucial role. Rigorous research has been carried out for passivating the traps near E_C. Relatively the research on D_{it} near E_V is less. There are several ways to measure interface trap densities using a capacitor or a transistor structure. Using a MOS capacitor structure interface trap densities can be found using methods such as simultaneous high frequency-low frequency CV (HI-LO CV), $C - \psi$ methods, photo-assisted CV, constant capacitance deep level transient spectroscopy (CCDLTS), etc. Details about these methods can be found in [30]. Similarly, using a MOSFET structure the number of interface traps can also be estimated by methods namely charge pumping [31], charge sheet model [32], etc.

1.5.2. Effect of nitridation on n-4H-SiC/SiO_2 interface

Since its discovery, nitric oxide (NO) annealing has been the most effective way to passivate interface traps in n-channel 4H-SiC MOSFETs. It has been shown that during NO annealing, nitrogen comes and sits at the oxide-semiconductor interface (Figure 1.10 (a).). With the increase of NO timing, the amount of nitrogen at the interface increases before it reaches saturation. A higher nitrogen concentration at the interface also increases the trap passivation that in turn increases the channel mobility that has been confirmed through SIMS [33], XPS [34], and CCDLTS [35] measurements. A maximum field effect mobility of 50 $cm^2/V\ s$ can be achieved with an n-channel MOSFET fabricated on a moderately doped p-well substrate as shown in Figure 1.10 (b). Below the effect of nitrogen at the interface for different processing is tabulated in Table 1.5.

Gate oxide	Orientation	Processing Temperature (°C)	μ ($cm^2 V^{-1} s^{-1}$)	D_{it} ($cm^{-2} eV^{-1}$)	N_A (cm^{-3})	References
Dry (As-Ox)	(0001)	1200	6–8	8×10^{12}	1×10^{16} epi	[37]
NO (POA)	(0001)	1175	35-50	4×10^{11}	6×10^{15} epi	[33], [38]
NO (POA)	$(000\bar{1})$	1175	65	8×10^{11}	5×10^{15} epi	[39]
NO (POA)	$(11\bar{2}0)$	1250	50	N.A.	5×10^{16} epi	[40]
NO (POA)	$(0\bar{3}3\bar{8})$	1250	100	N.A.	5×10^{15} epi	[40]
NO (PDA)	(0001)	1175	45	N.A.	1×10^{16} epi	[41]
NO (O)	(0001)	1175	N.A.	2×10^{11}	8×10^{15} epi	[42]
N_2O (POA)	(0001)	1175	49	3×10^{11}	N.A.	[33]
N_2O (PDA)	(0001)	1150	24-40	$4\text{-}8\times 10^{11}$	1×10^{17} imp	[41], [43]
N_2O (O)	(0001)	1410	N.A.	1×10^{12}	5×10^{15} epi	[44]

Table 1.5: Summary of interface nitridation processing and their effect on electron mobility and D_{it} in n-channel 4H-SiC MOSFET. Here POA represents post oxidation annealing, PDA is post deposition annealing, and (O) represents oxidation in NO or N_2O [36].

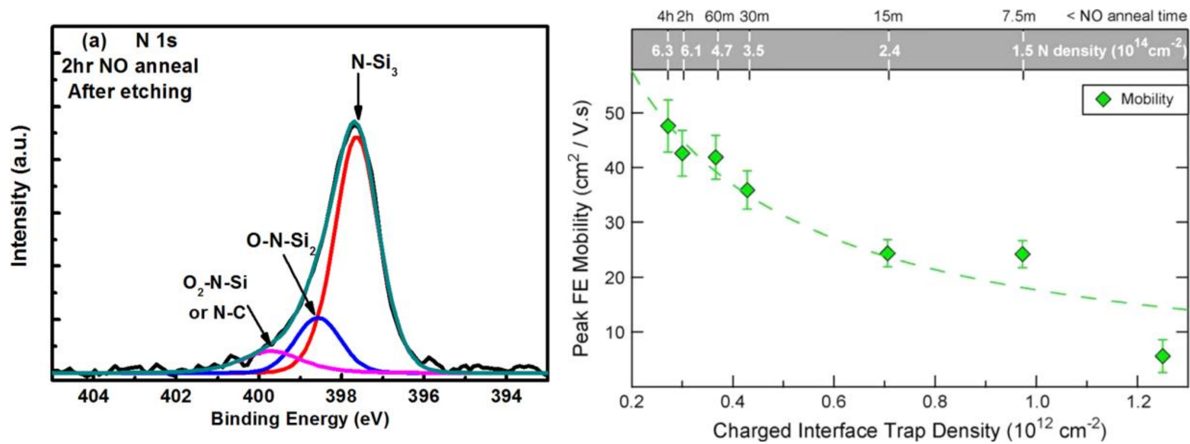

Figure 1.10: Figure 1.10: (a) N 1s spectra showing nitrogen incorporation at the interface through XPS measurements. [34] (b) Peak field-effect mobility versus various NO annealing times (upper horizontal axis), that produce distinct N densities (measured by SIMS) of charged interface states (lower axis) in the ON-state of the MOSFETs [33].

1.5.3. Alternate dielectric on n-4H-SiC/SiO_2 interface

In addition to POA, research has been conducted on n-channel MOSFET using alternate dielectric incorporating elements from groups II, III, V, and other elements of the periodic table such as (B, Ba, Ca, La, Sr, etc.) [45], [47], [48]. Some of these elements were very efficient in increasing channel mobility and reducing D_{it}. A summary of MOSFET characteristics made with these elements is shown in Table 1.6. A significant improvement in peak mobility can be observed by introducing metals at the interface [46]. Phosphorus can improve peak mobility; however, a large negative threshold voltage shift can be seen in these devices under positive bias temperature stressing at high temperatures [49]. A counter-doped antimony layer at the channel improves n-channel MOSFET mobility without much threshold voltage loss [24]. A low-temperature atomic layer deposited Al_2O_3 after surface treatment with nitrogen and hydrogen is also seen to increase mobility, although suffers from high gate leakage [51].

Gate oxide Interlayer element	Processing Temperature (°C)	μ ($cm^2 V^{-1} s^{-1}$)	D_{it} near E_C ($cm^{-2} eV^{-1}$)	Counter doping	References
Lanthanum	NA	133	N.A.	N.A.	[46]
Boron	950	100	9×10^{10}	No	[47], [48]
Phosphorus	1000	108	5×10^{11}	Yes	[49]
Antimony	1150	65-100	N.A.	Yes	[24]
Barium	950	85	3×10^{11}	No	[50]
Calcium	950	1-5	N.A.	No	[50]
Strontium	950	40	3×10^{11}	No	[50]
Aluminum	200	52	NA	No	[51]

Table 1.6: Summary of n-channel MOSFETs mobility and D_{it} made with gr. II, III, and V elements [45].

1.6. Recent developments of p-channel MOSFET

In search of the best oxidation method and post-oxidation annealing treatments, some encouraging research has been performed which is discussed below. The best results for p-channel MOSFET are high-temperature N_2 annealing and post oxidation NO annealing. The other notable research includes wet-oxidation/Re-oxidation, counter doping a thin p-layer at the channel, and N_2O-grown oxides.

1.6.1. Wet Oxidation/ Re-oxidation

Gate oxidation is performed using a pyrogenic method and in comparison, thermal dry oxidation is performed at 1200 ºC by *Okamoto et al* [52]. Additionally, a wet reoxidation is done on a sample that is thermally oxidized at 1200 ºC. The list of the samples is in below Table 1.7. It can be observed from figure 1.11 (a) that maximum passivation of D_{it} occurs with the wet oxidation method additionally it yields maximum fixed charge passivation that is visible from the lowest flat band voltage.

	Oxidation	POA	Reoxidation
(i)	Dry at 1200 °C	Ar POA at 1200 °C for 30 min	···
(ii)	Dry at 1200 °C	Ar POA at 1200 °C for 30 min	Wet at 950 °C for 180 min
(ii)	Wet at 1200 °C	Ar POA at 1200 °C for 30 min	···

Table 1.7: Wet oxidation processes incorporated in the study [52].

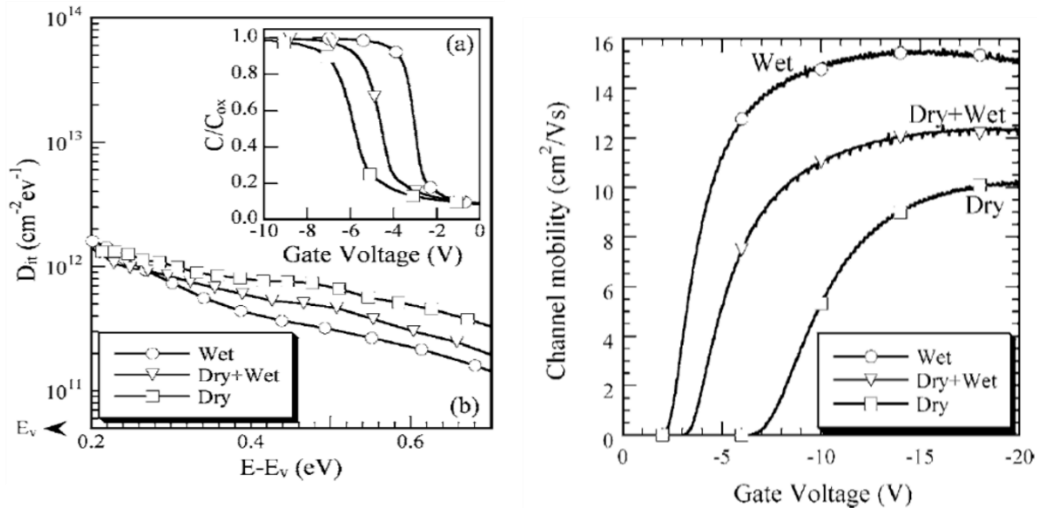

Figure 1.11: (a) D_{it} near the valence band edge for three incorporated processes. The inset figure shows the CV curves signifying the amount of fixed charge at the oxide semiconductor interface. (b) p-channel MOSFET mobility for three different processes [52].

Furthermore, Figure 1.11 (b) denotes the highest field effect mobility of 15.6 cm^2/V s is obtained due to this process. The wet reoxidation method is also seen to be passivating traps and increasing mobility over the dry oxide-only process. Instead of a significant improvement of the p-type interface through wet oxidation, it failed to produce competitive results for n-channel MOSFETs [53]. Therefore, from a CMOS standpoint, wet oxidation cannot be used for p-MOS processing.

1.6.2. Effect of nitridation on p-4H-SiC/SiO_2 interface

The recent best result in terms of p-channel MOSFET mobility is obtained by using high temperature (1400 ^oC-1600 ^oC) post oxidation N_2 annealing by *Tachiki and Kimoto* [10]. N_2 annealing efficiently reduces the D_{it} near E_v, and the field-effect mobility of p-channel MOSFETs reaches 17 cm^2/Vs, which is roughly 30% higher than the NO-annealed MOSFETs. However, NO is still the most efficient post oxidation annealing treatment to passivate traps near E_C. The Bias temperature instability of MOSFETs annealed in an N_2 environment is found to be comparable to the MOSFETs annealed in a NO. The effect of nitrogen at the interface due to different processes is tabulated below in Table 1.8.

Gate oxide	Orientation	Processing Temperature (^oC)	μ ($cm^2 V^{-1} s^{-1}$)	D_{it} ($cm^{-2} eV^{-1}$)	N_A (cm^{-3})	References
Dry (As-Ox)	(0001)	1200	3-6	5×10^{12}	6×10^{15} epi	[10], [33]
N_2 (POA)	(0001)	1400-1600	17	3×10^{11}	6×10^{15} epi	[10]

NO (POA)	(0001)	1175-1300	8-15	4×10^{11}	6×10^{15} epi	[33], [54], [55]
N_2O (PDA)	(0001)	1300	10	1×10^{12}	5×10^{15} epi	[22]
N_2O (PDA)	$(11\bar{2}0)$	1300	17	N.A.	5×10^{15} epi	[22]
N_2O (PDA)	$(03\bar{3}8)$	1300	13	N.A.	5×10^{15} epi	[22]
N_2O (O)	(0001)	1300	7	1×10^{12}	5×10^{15} epi	[22]
N_2O (O)	$(11\bar{2}0)$	1300	17	1×10^{12}	5×10^{15} epi	[22]
N_2O (O)	$(03\bar{3}8)$	1300	11	1×10^{12}	5×10^{15} epi	[22]

Table 1.8: Summary of p-channel MOSFETs mobility and D_{it} made with different POA conditions.

1.7. Mobility limiting mechanisms

Understanding the core fundamental principles is critical for overcoming channel mobility and device stability issues. The recent development with innovative interface engineering, high mobilities, and improved characterization techniques provides key insight that can be used to comprehend the mechanisms underlying mobility and device stability issues. The channel mobility of a MOSFET can be measured in several ways. The different mobilities depending on the

measurement techniques are (i) effective mobility (μ_{eff}) (ii) field effect mobility (μ_{FE}), and (iii) Hall mobility (μ_{Hall}). A detailed discussion about the measurements of these mobilities is done in *Chapter 2.*

An expression of μ_{eff} is obtained from source-drain conductance measurements as

$$\mu_{eff} = \frac{L/W}{C_{ox}(V_G - V_{th})}\left(\frac{dI_D}{dV_D}\right)_{V_D \to 0} \tag{1.6}$$

Here L and W are the length and width of the channel, C_{ox} is the gate capacitance per unit area, V_G and V_D are the gate and drain voltages with respect to source, V_{th} is threshold voltage and I_D is drain current.

The value of μ_{FE} is obtained from drain to gate transconductance measurements as

$$\mu_{FE} = \frac{L/W}{C_{ox}V_D}\left(\frac{dI_D}{dV_G}\right)_{V_D \to 0} \tag{1.7}$$

Even though μ_{eff} and μ_{FE} gives a good estimation of the channel mobility, they do not undertake the amounts of trapped charges. Whereas μ_{Hall} that is calculated from sheet resistance (r_s) and sheet charge density (n_s) gives the most accurate value of channel mobility. The expression of μ_{Hall} is given by,

$$\mu_{Hall} = \frac{1}{en_s r_s} \tag{1.8}$$

Here, e is the electron charge.

The channel mobility of a MOSFET not only gets hampered by a large amount of interface trap densities but also gets affected due to different several mechanisms that take place at the channel as shown in figure 1.15. The three main scattering mechanisms that affect the channel mobilities are (i) Coulomb scattering (ii) phonon scattering, and (iii) surface roughness scattering [56]–[58]. The resulting hole mobility due to these three scattering is given by Matthiesen's rule [59]:

$$\frac{1}{\mu_{Hall}} = \frac{1}{\mu_C} + \frac{1}{\mu_{Ph}} + \frac{1}{\mu_{SR}} \tag{1.9}$$

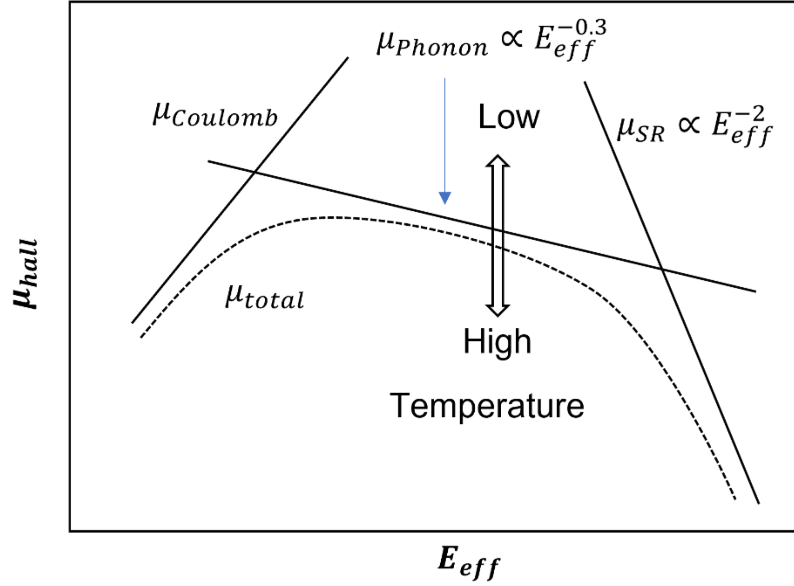

Figure 1.12: Hall mobility versus effective electric field at the different regimes of scattering. (i) $\boldsymbol{\mu_C}$ depends on E_{eff} through a constant $\boldsymbol{\gamma}$ that depends on MOSFET substrate doping. $\boldsymbol{\mu_{Ph}}$ is the phonon scattering limited mobility and $\boldsymbol{\mu_{SR}}$ the surface roughness scattering limited mobility [60].

Here, μ_C, μ_P, and μ_{SR} are the Coulomb, phonon, and surface roughness scattering limited mobilities, respectively. A brief discussion about the scattering mechanisms is done below. Earlier studies on Si n- and p-channel MOSFETs [61], [62] and 4H-SiC n-channel MOSFET [60], [63], [64] suggest that the dominant scattering mechanisms largely depend on E_{eff}. The magnitude of E_{eff} can be obtained [61] as,

$$E_{eff} = \frac{1}{\epsilon_{SiC}}\left(Q_{dep} + \eta Q_{inv}\right) \tag{1.10}$$

The first term in Eq. 1.7 represents depletion space charge, and the second term stands for the inversion layer charge and excludes trapped charges. Here, η is a constant with a value of 0.33, considering the same value as in Si p-channel MOSFET at $27\ ^{o}$C [62], [65] and ϵ_{SiC} is the dielectric constant of 4H-SiC.

The channel scattering mechanisms for Si and n-channel 4H-SiC MOSFETs were well understood as explained above. However, data on p-channel MOSFET related to Hall measurements and channel scattering mechanisms are relatively insignificant. That is why in this thesis the focus has been on the channel transport properties of holes in 4H-SiC MOSFETs using Hall measurements and scattering mechanisms that affect the channel mobility.

1.7.1. Coulomb scattering

Coulomb scattering occurs due to the interaction of the inversion layer carriers (electrons or holes) with the interface traps present at the oxide-semiconductor interface. This type of scattering decrease with increasing temperature, and as a result Coulomb mobility (μ_C) increases. Relation between temperature and μ_C can be obtained in terms of scattering rate, distance from the interface (z), and occupied trap density (N_{it}) as [66],

$$\frac{1}{\mu_C(T,z)} = \frac{m^* e^3 N_{it}}{16\pi\bar{\epsilon}^2 \hbar k_B T} \times F \tag{1.11}$$

Here F is an integrating factor that incorporates the effect of the distance between the interface and the mobile charges [67], [68],

$$F(z) = \int_{\alpha=0}^{\pi/2} \left(1 - \frac{q_{sc}^2}{\frac{8m^* k_B T}{\hbar^2} sin^2\alpha + q_{sc}^2}\right) exp\left[-2\sqrt{\left(\frac{8m^* k_B T}{\hbar^2} sin^2\alpha + q_{sc}^2\right) \times z}\right] d\alpha \tag{1.12}$$

Here, e is the electron charge, m^* is the effective mass, $\hbar$ is the Planck's constant, k_B is the Boltzmann's constant, $\bar{\epsilon}$ is the average permittivity of SiO_2 and 4H-SiC. q_{sc} is the screening wave vector, and α is the scattering angle.

It can be seen from eq. 1.11, that Coulomb mobility is inversely proportional to the occupied interface trap density and directly proportional to temperature. As the temperature increase, N_{it} decreases, and therefore μ_C increase.

1.7.2. Phonon scattering

Phonon scattering originates from the interaction of the channel carriers with the phonon vibration on the bulk and surface of the semiconductor. This scattering increases with the rise of temperature. As a result, the phonon limited mobility (μ_{ph}) decreases as temperature (T) goes up. A relation between μ_{ph}, T and the transverse electric field (E_{eff}) can be obtained [68], [69],

$$\mu_{ph} = \frac{A}{E_{eff}} + \frac{B}{TE_{eff}^{1/3}} \tag{1.13}$$

Here A and B are parameters that are extracted using theoretical or experimental data. For n-channel MOSFETs fabricated on a lightly doped substrate ($3 \times 10^{14}\ cm^{-3}$) phonon scattering is seen to be the sole dominant scattering mechanism at the channel at room temperature [60]. For moderate to highly doped substrate it arises at higher temperatures and high gate bias [70].

1.7.3. Surface roughness scattering

Surface roughness scattering originates from the interaction of the mobile carriers in the channel with the rough semiconductor surface. 4H-SiC substrates are grown with a 4° or 8° off-axis alignment. Because of this off-axis aligning (miscut), some nano-level steps arise on the surface as shown in Figure 1.13 called step bunching. These steps are ~ 1 nm high and come at a

regular interval of 7 nm. Sometimes these step bunching can be 3-5 nm in height and 30-70 nm in length at the 4H-SiC/SiO_2 interface [71], [72]. These surface imperfections give rise to a perturbation potential that can be written as [66],

$$V_{perturb}(r) = \delta(r).\frac{\partial V}{\partial z} \tag{1.14}$$

Here $\delta(r)$ is the fluctuation in the step bunching that is a function of position r. and $\frac{\partial V}{\partial z}$ is the electric field at the semiconductor surface/oxide-semiconductor interface. A typical model that is taken for $S(q)$ [equals the square of the Fourier transform of $\delta(r)$], called the power spectrum in surface roughness scattering calculations [66] is shown in Figure 1.13 (right). q is the scattering wave vector here.

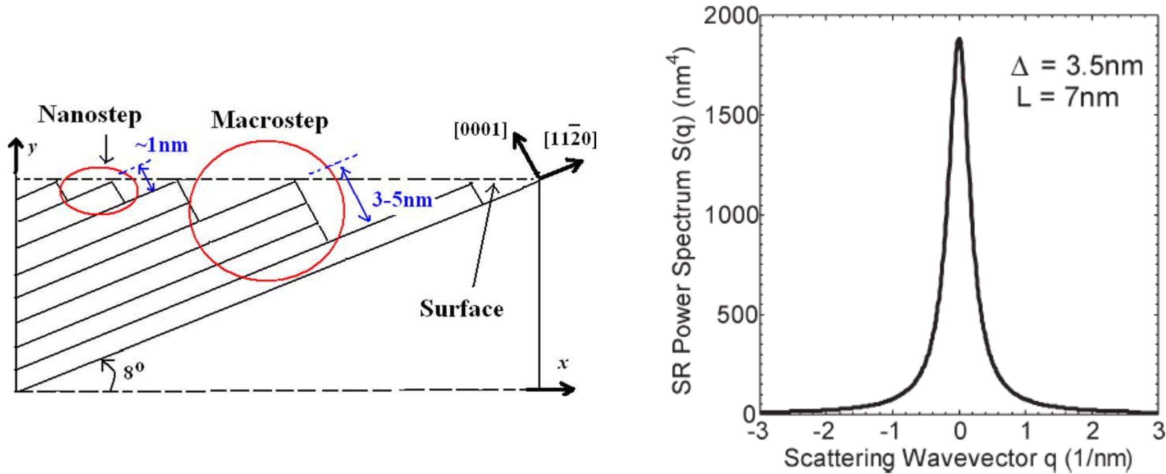

Figure 1.13: (left) Step bunching on a 4H-SiC surface grown at 8° off-axis. Typical power spectrum considered in the calculation to model surface roughness scattering [68]

Now, the scattering matrix element for an electron that is at z distance from the interface with wave vectors k and k' before and after scattering can be written as,

$$|H_{kk'}|^2 = \langle \vec{k}|\delta(r)\frac{\partial V}{\partial z}|\vec{k}'\rangle^2 = e^2E_{eff}^2S(q) \tag{1.15}$$

From this above matrix element, the scattering probability can be determined as,

$$S_{kk'}(z) = \frac{2\pi}{\hbar}|H_{kk'}|^2\delta(\vec{k}-\vec{k}') = \frac{2\pi}{\hbar}e^2E_{eff}^2S(q)\delta(\vec{k}-\vec{k}') \tag{1.16}$$

For an average step height of Δ and average repetition factor L, the value of $S(q)$ can be determined as [66],

$$S(q) = \frac{\pi\Delta^2L^2}{\left[1+\frac{q^2L^2}{2}\right]} \tag{1.17}$$

Putting $S(q)$ in eq. 1.16, the value of the scattering probability $S_{kk'}(z)$ is given by,

$$S_{kk'}(z) = \frac{2\pi^2\Delta^2L^2}{\hbar\left[1+\frac{q^2L^2}{2}\right]}e^2E_{eff}^2\delta(\vec{k}-\vec{k}') \tag{1.18}$$

The average scattering rate can be obtained from eq. 1.18, considering the effect of screening as [73],

$$\langle\frac{1}{\tau_{sr}(z)}\rangle = \int_{\theta=0}^{2\pi}\int_{k'=0}^{k} S_{kk'}(z)\,(\frac{q}{q+q_{sc}})(1-cos\theta)d\theta\,k'dk' \tag{1.19}$$

Here q_{sc} is the screening wave vector that depends on the inversion layer charge density. The surface roughness mobility is related to the mean free scattering time $\tau_{sr}(z)$ as,

$$\frac{1}{\mu_{sr}} = \frac{m_c}{e}\langle\frac{1}{\tau_{sr}(z)}\rangle \tag{1.20}$$

m_c is the conductivity effective mass. Therefore, μ_{sr} can be expressed as

$$\mu_{sr} = \frac{\Gamma}{E_{eff}^2} \tag{1.21}$$

Γ is the constant resulting from the eq. 1.19, i.e.

$$\Gamma = \frac{1}{\frac{m_c e 2\pi^2 \Delta^2 L^2}{\hbar\left[1+\frac{q^2 L^2}{2}\right]} \int_{\theta=0}^{2\pi} \int_{k'=0}^{k} S_{kk'}(z) \left(\frac{q}{q+q_{sc}}\right)(1-cos\theta) d\theta \, \delta(\vec{k}-\vec{k}') k' dk'} \quad (1.22)$$

It depends on the device processing and quality of the oxide-semiconductor interface. Theoretically, μ_{sr} depends on E_{eff} as $\frac{1}{E_{eff}^2}$ as explained above. For Si, experimental values match closely with the theoretical expression. In this thesis, the power law dependence of μ_{sr} on E_{eff} for 4H-SiC n- and p-channel MOSFETs are experimentally determined.

1.8. Transverse Electric field (E_{eff})

As seen above, the transverse electric field (E_{eff}) is an important parameter, that determines most of the scattering mechanisms. E_{eff} originates from the charges present at the channel that are depletion charges (Q_{dep}) and inversion charges (Q_{inv}). The peak field at the channel can be written from Gauss' law,

$$E = \frac{1}{\epsilon}\left(Q_{dep} + Q_{inv}\right) \quad (1.23)$$

However, the carriers present at the channel do not encounter the total field. Electrons being quantum particles are distributed in the channel in a Gaussian profile with the peak inside the Si surface [61], which makes the effective field to be different than the total field. For instance, two different doping concentrations with the same *E* are shown in Figure 1.14. Although they have the same *E,* the average field inside the two-inversion layer can be significantly different. If $n(x)$ is the carrier concentration at a location x in the channel, and x_i being the total length of the channel, the effective electric field at the inversion layer becomes [61],

$$E_{eff,\,inv} = \frac{\int_0^{x_i} n(x)E(x)dx}{\int_0^{x_i} n(x)dx} = \eta\left(\frac{Q_{inv}}{\epsilon}\right) \tag{1.24}$$

Here η is a constant equal to 0.5 and 0.33 for electrons and holes respectively originating from the above integration [61]. Therefore, the effective electric field becomes,

$$E_{eff} = \frac{1}{\epsilon}\left(Q_{dep} + \eta Q_{inv}\right) \tag{1.25}$$

Q_{dep} is a function of the substrate doping concentration (N_A) and bulk potential (ϕ_B) whereas Q_{inv} depends on the carrier concentration (n_s) at the channel. E_{eff} can be rewritten as [61],

$$E_{eff} = \frac{1}{\epsilon}\left(\sqrt{2N_A q\epsilon.\,2\phi_B} + \eta e n_s\right) \tag{1.25}$$

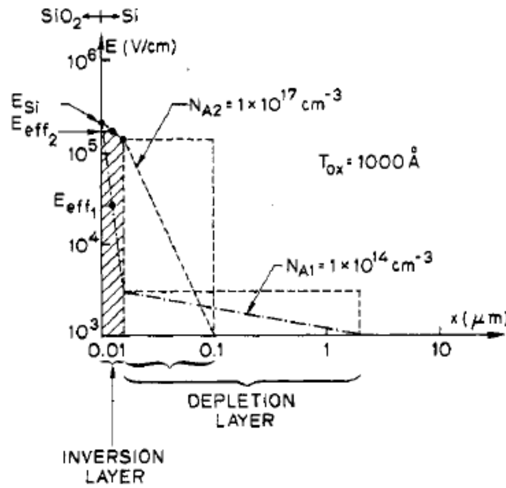

Figure 1.14: Total electric field (E) and effective electric field at the inversion layer for two different substrate doping $N_{A1} = 1 \times 10^{14}\ cm^{-3}$ and $N_{A2} = 1 \times 10^{17}\ cm^{-3}$ [61].

1.9. Thesis Outline

A brief description of the chapters in this thesis is described below:

Chapter 2 discusses the device fabrication and measurement methods used in this thesis. First, the fundamentals of MOS physics through energy band diagrams of different operation regions are explained. The process to determine interface traps at the oxide-semiconductor interface are enlightened. Furthermore, the basics of MOSFET characteristics and fabrication procedures are explained using process flow diagrams. Measurements procedure of field effect and Hall mobilities are illustrated.

Chapter 3 introduces different post oxidation annealing (POA) treatments consisting of hydrogen (H_2) and nitric oxide (NO) annealing, motivated by past research on p-channel MOSFETs. The effect of these annealing methods on the p-4H-SiC/SiO_2 interface is found and compared using the simultaneous high frequency-low frequency CV (hi-lo CV) method. Moreover, oxide thicknesses are varied to find the optimum thickness and POA conditions for p-channel MOSFET fabrication that has been studied in later chapters.

Chapter 4 introduces nitric oxide (NO) annealing as a suitable interface trap passivation method near the valence and conduction band edge of 4H-SiC. Using high temperature simultaneous High-Low frequency methods, trap density is calculated in the whole band gap of 4H-SiC. Later p-channel Hall bar MOSFETs are fabricated with NO annealing. High-temperature Hall measurements are carried out to study the transport of channel holes in 4H-SiC p-channel MOSFETs. Additionally, device reliability studies have been conducted using bias temperature instability (BTI).

Chapter 5 discusses the dominant scattering mechanisms at the channel of NO annealed 4H-SiC p-channel MOSFETs. The scattering mechanisms are distinguished using Hall measurements. With the application of body bias and temperature, the relationship between mobility and the transverse electric field at the channel is determined. Additionally, the effect of substrate doping concentration on channel conduction is discussed. It is also described how to transit from one scattering mechanism to another with a single device using body bias and temperature-dependent study that serves as a prediction of hole transport for MOSFETs with different substrate doping.

The research in *Chapter 6* focuses on finding a sustainable alternative annealing method for 4H-SiC p-channel MOSFETs that can replace NO. High-temperature N_2 annealing is found to be the best environment-friendly annealing method to reduce traps near the valence band edge. A variation of temperature and time-dependent study of N_2 annealing is performed. The electrical analysis is conducted through fabrication and characterization of n- and p-type MOS capacitors and p-channel MOSFETs. Furthermore, X-ray photoelectron spectroscopy data are used to investigate the chemical alteration at the oxide-semiconductor interface caused by N_2 annealing in comparison with NO. Finally, the effect of nitrogen at the interface is addressed theoretically in collaboration with the theoretical condensed matter Physics group.

Chapter 7 summarizes the research that has been discussed in the early chapters. It also gives some insight into the future work that can be performed on 4H-SiC p-channel MOSFETs.

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Chapter 2

Fabrication and characterization techniques

One of the most common semiconductor architectures used in electronic applications is the Metal–Oxide–Semiconductor Field-Effect Transistor (MOSFET). MOSFET is widely utilized in digital circuit applications, where millions of devices can be produced in a single integrated circuit because of scalability. The first ever Si-based MOSFET was demonstrated by Kahng and Atalla [1]. Two types of complementary configurations of MOS transistors can be available depending on carrier types such as n-channel (electron as carriers) and p-channel MOSFET (holes as carriers). When both sorts of devices are employed in the same circuit, called Complementary MOS (CMOS) circuits [2]–[4], electronic circuit design becomes incredibly adaptable. In this chapter, the physics related to the basics of the MOS interface and measurement methods are discussed.

2.1. MOS Fundamentals

The heart of a MOSFET is a parallel plate capacitor where the dielectric layer (SiO_2 or any other oxide layer) is sandwiched between the gate metal and semiconductor forming a metal-oxide-semiconductor structure as shown in Figure 2.1 (a). The oxide layer can be thermally grown at high temperatures or deposited onto the semiconductor. The gate metal is deposited on top of the oxide which can be Aluminum, Molybdenum, etc. A backside contact is created for electrical connection by attaching the MOS structure with a copper plate through conductive epoxy/silver paste. The equivalent capacitance (Figure 2.1 (b)) of the system is a series of the oxide capacitance (C_{ox}) and a variable semiconductor capacitance (C_S).

2.1.1. Thermal Equilibrium

The mechanism in a MOS capacitor can be explained using an energy band diagram. Figure 2.2 (a) shows the energy band diagrams for the metal, oxide, and semiconductor before forming

any junction. When they are brought together to form a MOS system the fermi level in all three components tries to align at the same level [5]–[7].

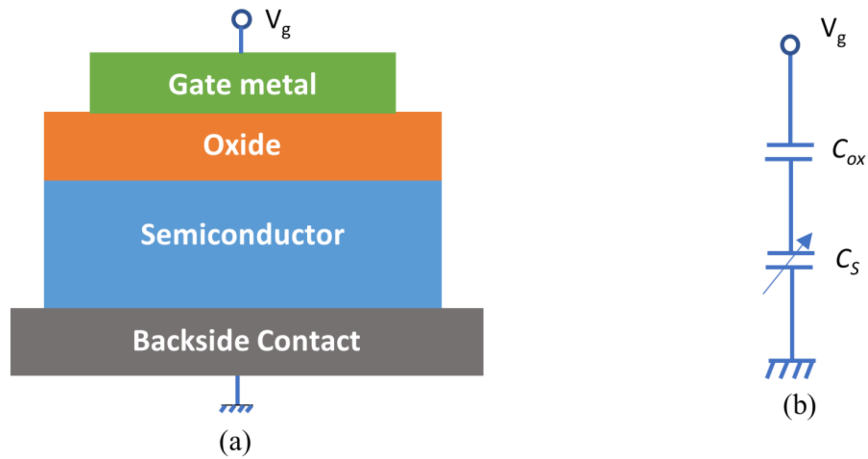


Figure 2.1: (a) Schematic diagram of the metal-oxide-semiconductor (MOS) capacitor. (b) Equivalent circuit of the capacitance system

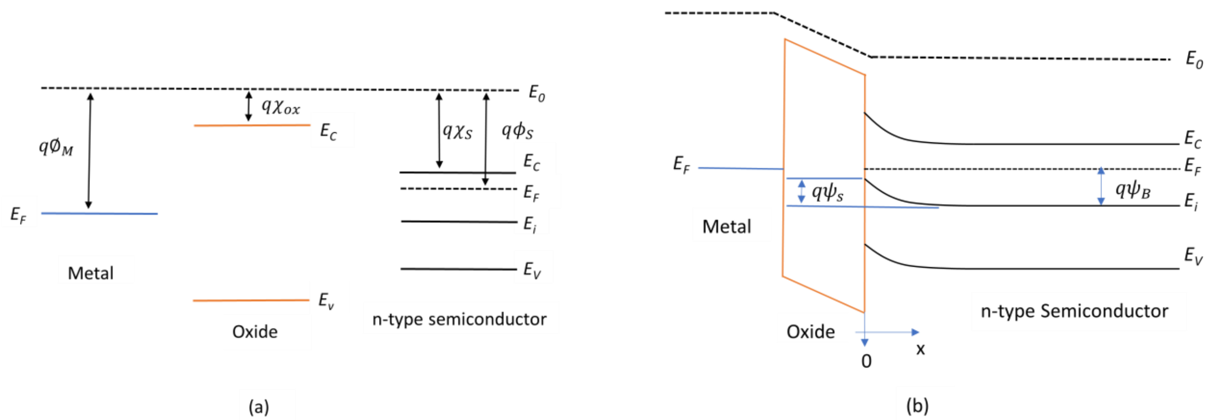


Figure 2.2 : (a) Energy levels for metal, oxide, and semiconductor before forming MOS system. (b) Real MOS system showing band bending due to the difference in Fermi level at equilibrium.

Due to the difference in work function between metal and semiconductor the band bends at the interface of oxide and semiconductor as shown in Figure 2.2 (b) as ψ_s called the surface potential. Additionally, the negative charges from metal to semiconductor gather at the metal surface

forming a thin sheet of charge. To balance out the total charge to be zero from Gauss's law an equal amount of charge sheet forms by the positive donor atoms that extend from the interface into the semiconductor.

2.1.2. Surface potential versus space charge density

The application of gate voltage allows for a change in the surface potential (ψ_s) and the space charge density in the semiconductor. Band bending ψ at any point x can be expressed in terms of the intrinsic Fermi level (E_i) difference at any interfacial point from its bulk counterpart [6].

$$\psi(x) = \frac{1}{q}[E_i(bulk) - E_i(x)] \tag{2.1}$$

Here, $\psi(x = 0) = \psi_s$. The career concentrations n_s and $p_s$can be written in terms of ψ as follows [6],

$$n_s(x) = n_0 \exp[\beta\, \psi(x)] \tag{2.2}$$

$$p_s(x) = p_0 \exp[-\beta\, \psi(x)] \tag{2.3}$$

Here $\beta = \frac{1}{KT}$, K is the Boltzmann constant, and T is the absolute temperature. n_0 and p_0 are the electrons and hole concentrations at equilibrium and can be expressed in terms of the bulk potential ψ_B and intrinsic carrier concentrations n_i and p_i as follows [6],

$$n_0 = n_i \exp[\beta\, \psi_B] \approx N_D \text{ for n-type semiconductor and,} \tag{2.4}$$

$$p_0 = p_i \exp[\beta\, \psi_B] \approx N_A \text{ for p-type semiconductor} \tag{2.5}$$

Here N_D is the donor doping concentration and N_A is the acceptor doping concentration for n- and p-type semiconductors respectively.

The surface potential can be solved in terms of surface charge density ρ by applying Poisson's equation,

$$\frac{d^2\psi(x)}{dx^2} = -\frac{\rho(x)}{\epsilon_s} \tag{2.6}$$

Where $\rho(x)$ is total space charge density and ϵ_s is the dielectric constant of the semiconductor. Using the above equations, the surface potential $\psi(x)$ can be obtained, and thereafter the electric field at the surface $E_S = -\frac{d\psi}{dx}$ can be obtained as [6],

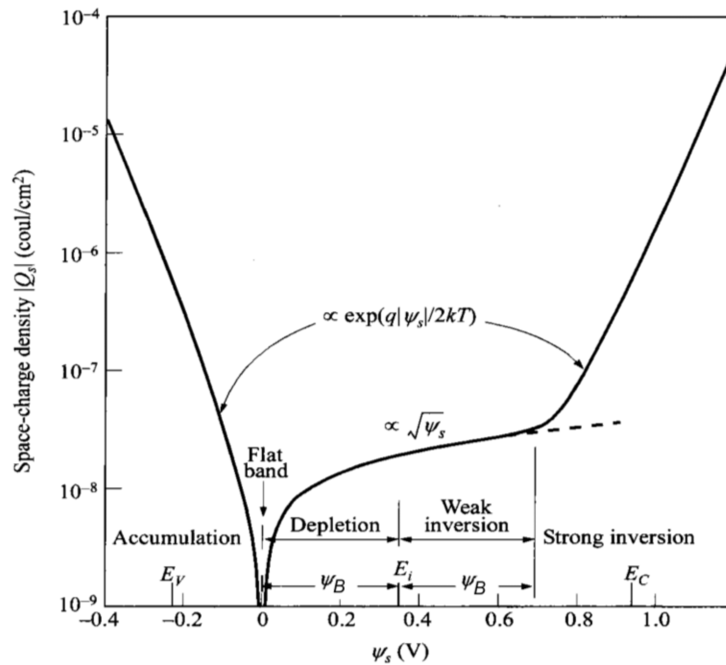


Figure 2.3: Space charge density versus the surface potential for p-type Si of doping concentration $N_A = 4 \times 10^{15}\ cm^{-3}$ at room temperature [6].

$$E_S = \pm sqrt[\ (\frac{2qn_0}{\epsilon_s\beta})\{(\exp(\beta\,\psi) - \beta\,\psi - 1) + \frac{p_0}{n_0}(\exp(-\beta\,\psi) + \beta\,\psi - 1)\}] \tag{2.7}$$

Now, from Gauss's law the space charge density Q_S can be extracted as $Q_S = \epsilon_s\ E_S$,

$$Q_S = \pm sqrt[\ (\frac{2\epsilon_s q n_0}{\beta})\{(\exp(\beta\,\psi) - \beta\,\psi - 1) + \frac{p_0}{n_0}(\exp(-\beta\,\psi) + \beta\,\psi - 1)\}] \quad (2.8)$$

The variation of surface charge density with the surface potential can be seen in Figure 2.3. The semiconductor capacitance C_S can also be extracted from $C_S = \frac{dQ_s}{d\psi_s}$ as [6],

$$C_S = \sqrt{\frac{\epsilon_s q n_0 \beta}{2}} \frac{[1-\exp(-\beta\,\psi)+(\exp(-2\beta\,\psi)(\exp(\beta\,\psi)-1)]}{[(\exp(-\beta\,\psi)+\beta\,\psi-1)+(\exp(-2\beta\,\psi)(\exp(\beta\,\psi)-\beta\,\psi-1)]^{1/2}}] \quad (2.9)$$

Depending on the applied gate voltage, a MOS capacitor may have 3 different stages as discussed below.

2.1.3. Flatband condition

When the applied gate voltage compensates for the work function difference between the semiconductor and the metal, called built-in potential, the band looks flat as shown in Figure 2.4. In this case the value of $\psi_s = 0$, makes the stored charge in the zero as shown in Figure 2.4 (b).

Hence the semiconductor capacitance C_s can be written as [6],

$$C_s = \frac{\epsilon_s}{L_{Dn}} \quad (2.10)$$

Here, L_{Dn} is the Debye length for an n-type semiconductor as given by,

$$L_{Dn} = \sqrt{\frac{\epsilon_s}{q N_A \beta}} \quad (2.11)$$

Therefore the flat band capacitance is given by,

$$C_{FB} = \frac{\epsilon_{ox}}{t_{ox} + (\frac{\epsilon_{ox}}{\epsilon_s})L_{Dn}} \quad (2.12)$$

Here ϵ_{ox} and ϵ_s are the permittivity of the oxide and semiconductor respectively.

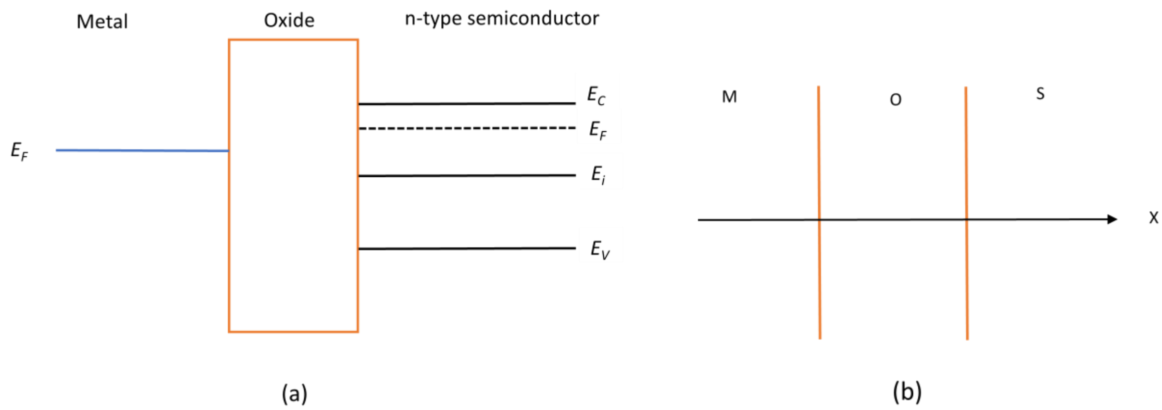


Figure 2.4: (a) Energy band diagram of the MOS system at flat band condition. (b) Block diagram of charge states of metal, oxide, and semiconductor.

2.1.4. Accumulation

For an n-type capacitor, the gate voltage beyond the flat band makes $\psi_s > 0$ as shown in Figure 2.5 (a). This makes the positive charges accumulate on the metal surface. To compensate for charge neutrality the same amount of negatively charged electrons moves toward the interface

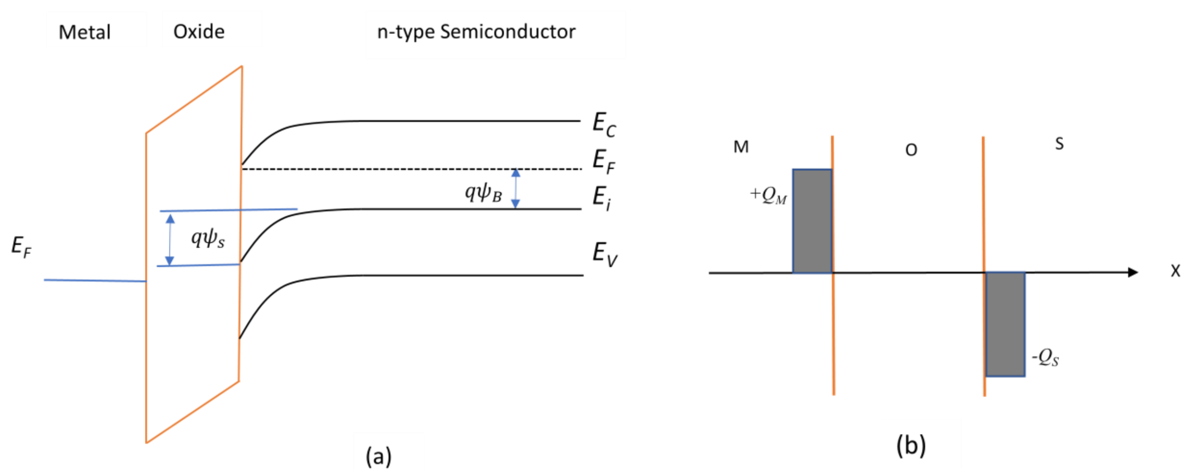


Figure 2.5: (a) Energy band diagram of the MOS system at Accumulation (b) Block diagram of charge states of metal, oxide, and semiconductor at accumulation.

and accumulate there as shown in Figure 2.5 (b). In this case, the total capacitance becomes approximately equal to the oxide capacitance,

$$C_{accumulation} = \frac{\epsilon_{ox}}{t_{ox}} \tag{2.13}$$

Here t_{ox} is the oxide thickness that can be measured from the value of C_{ox}.

2.1.5. Depletion

If the applied gate voltage becomes less than the flat band voltage, the band will bend downward for an n-type semiconductor as shown in Figure 2.6 (a). In this case, negatively charged electrons accumulate on the metal surface, and to compensate for the negative charges, the positively charged donor atoms (N_D) gather at the interface as shown in Figure 2.6 (b).

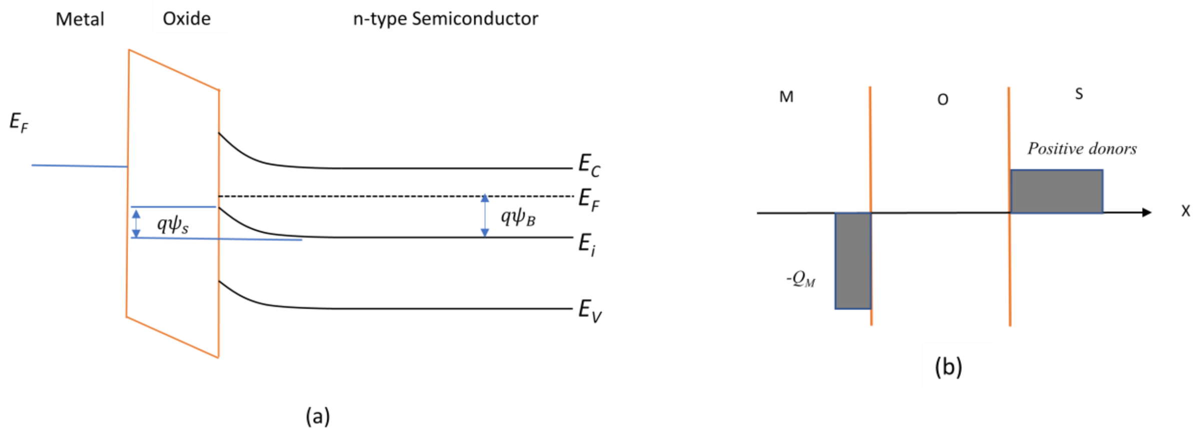


Figure 2.6: (a) Energy band diagram of the MOS system at depletion (b) Block diagram of charge states of metal, oxide, and semiconductor at depletion.

The depletion width is given by,

$$W_D = \sqrt{\frac{2\epsilon_s|\psi_s|}{qN_D}} \tag{2.14}$$

And the capacitance becomes,

$$C_S = \frac{\epsilon_s}{W_D} \tag{2.15}$$

At deep depletion, CV measurements can be used to find the doping concentration of the semiconductor using [5], [6], [8],

$$\frac{d(1/C^2)}{dV} = \frac{2}{q\epsilon_s N_D} \tag{2.16}$$

2.1.6. Inversion

For an n-type capacitor when the negative voltage is high enough the band bending happens in such a way that it crosses the intrinsic fermi level E_i. In this case, the valence band is nearer to the fermi level than the conduction band as shown in Figure 2.7 (a), which means that the surface has more hole concentration than the electron. In other words, the interface gets inverted, and the bias region is called inversion.

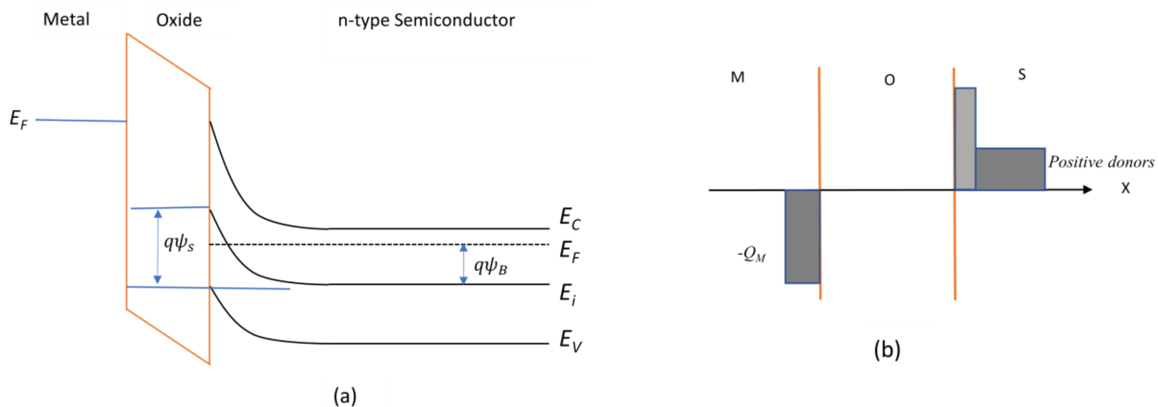


Figure 2.7: (a) Energy band diagram of the MOS system at inversion for an n-type capacitor (b) Block diagram of charge states of metal, oxide, and semiconductor at inversion.

At a voltage when maximum band bending happens ψ_s becomes equal to twice the bulk potential and the number of minority carriers becomes equal to the number of dopants. This region at $\psi_s = 2\psi_B$ is called strong inversion. The depletion width becomes maximum here [5], [8],

$$W_{D,max} = \sqrt{\frac{4\epsilon_s \psi_B}{qN_D}}$$

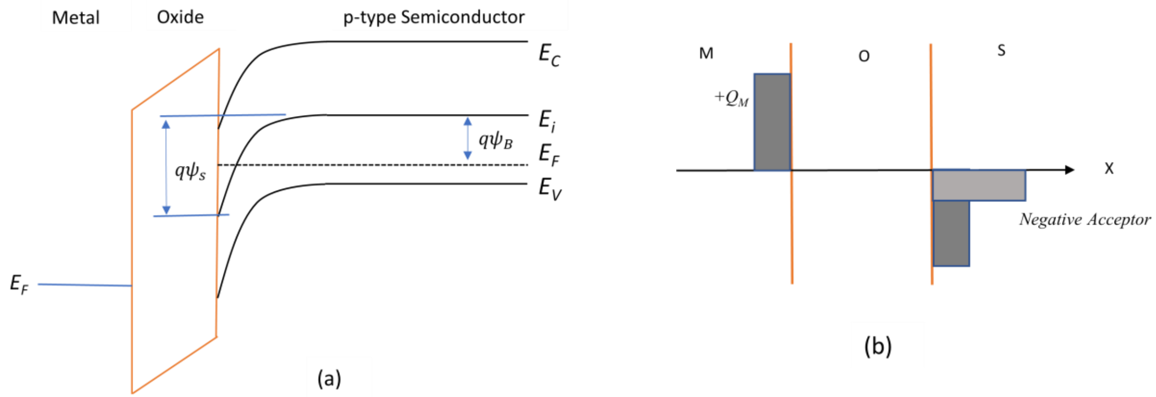


Figure 2.8: (a) Energy band diagram of the MOS system at inversion for a p-type capacitor (b) Block diagram of charge states of metal, oxide, and semiconductor at inversion.

Operation region	Value of $\boldsymbol{\psi_s}$ for n-type	Value of $\boldsymbol{\psi_s}$ for p-type
Accumulation	$\psi_s > 0$	$\psi_s < 0$
Flat band	$\psi_s = 0$	$\psi_s = 0$
Depletion	$\psi_B < \psi_s < 0$	$\psi_B > \psi_s > 0$
Strong Inversion	$\psi_S = 2\psi_B$	$\psi_S = 2\psi_B$

Table 2.1: Regions of operation for n- and p-type capacitors.

Figure 2.8 (a) and (b) show the band bending scenario under inversion condition for p-type capacitors. The different regions of operation for n- and p-type capacitors are tabulated below. Downward and upward bending is considered *positive* ($\psi_s > 0$) and *negative* ($\psi_s < 0$) band bending respectively.

2.2. Interface traps and fixed charges

The operation of a MOS capacitor and MOSFET is highly impacted by some undesired energy states or carrier traps. Based on their function and impact on the device they can have different names as discussed below.

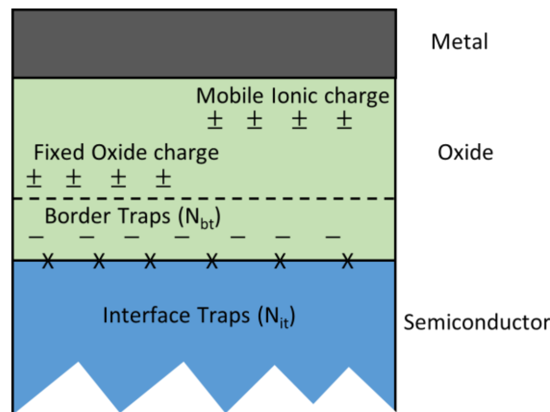


Figure 2.9: Distribution of different kinds of traps at the oxide semiconductor interface and in the oxide.

Interface traps or interface states are the energy states that are present in the bandgap of the semiconductor. Traps can be created because of processing stages at high temperatures or due to the abruptness of the junction between the crystalized semiconductor and the amorphous oxide layer. The states which are near to the conduction or valence band edge are called shallow states and the ones that are present deeper in the bandgap are called deep traps [5], [6], [8]. The interface traps that are below the intrinsic Fermi level are donor-like traps, that become positive when

releasing an electron. On the other hand, acceptor-like traps are present above the intrinsic Fermi level, which becomes negative when accepting an electron.

Border Traps are presents near the oxide semiconductor interface that frequently interact with the semiconductor via tunneling to and from the states in the conduction band, leading to longer capture and emission time constants depending on their energy level [9].

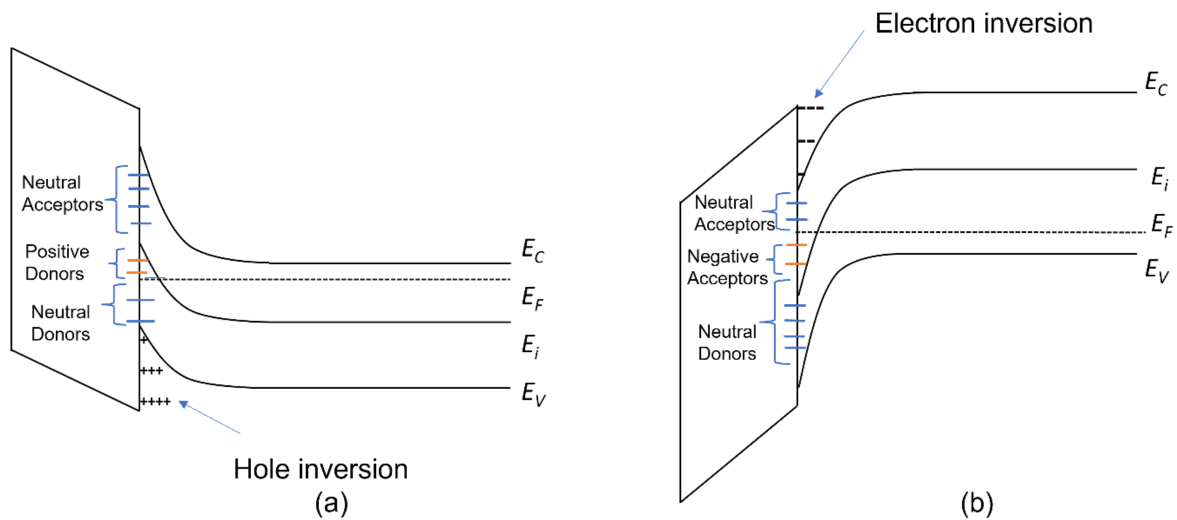


Figure 2.10: Charge states of different types of interface traps (a) for n-type capacitors at inversion and (b) for p-type capacitors at inversion.

Fixed oxide charges come in the oxide due to the poor quality of oxide processing. Depending on the charge states they can give rise to higher or lower flat band voltage in MOS capacitors [5], [6], [8].

Mobile ionic charges generate in the oxide due to metallic contamination during device processing such as Na^+ or Li^+. An unstable flat band and the threshold voltage can result due to the presence of these charge states [8].

2.3. Simultaneous high frequency (100 kHz)- low-frequency CV measurements

One of the most common methods to find interface trap density (D_{it}) in MOS interface is Simultaneous high frequency (100 kHz)- low frequency CV measurements [7], [10]. Here D_{it} is measured by observing the band bending in the semiconductor with the application of gate voltage. For this purpose, a small (15 mV) AC high-frequency signal (100 kHz or 1 MHz) is applied on top of a DC gate voltage supply. The capacitances due to the interface traps (C_{it}) do not respond to the high frequency due to their large emission rate [7], [11]. The equivalent capacitance [Figure 2.11 (a)] at high frequency (C_{HF}) comes due to the series combination of oxide (C_{ox}) and semiconductor capacitances (C_s) given by,

$$\frac{1}{C_{HF}} = \frac{1}{C_{Ox}} + \frac{1}{C_S} \tag{2.17}$$

However, at low-frequency interface traps respond and C_{it} comes in parallel with C_s. The equivalent capacitance [Figure 2.11 (b)] at low frequency (C_{LF}) is given by,

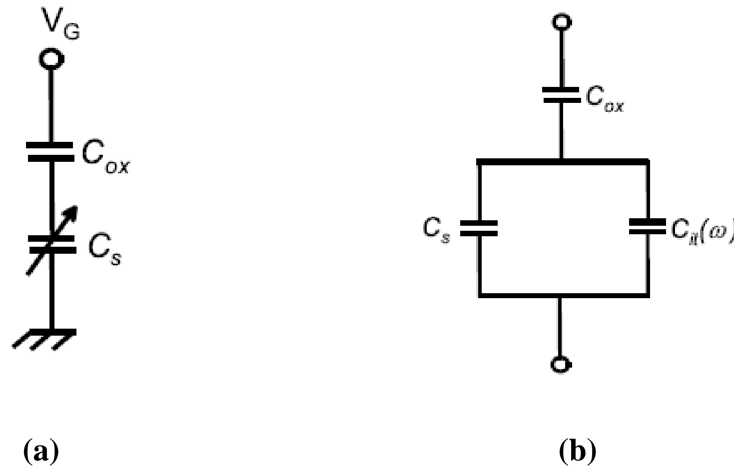


Figure 2.11: Equivalent capacitance circuit diagram at (a) high frequency (b) quasistatic or low frequency.

$$\frac{1}{C_{LF}} = \frac{1}{C_{Ox}} + \frac{1}{C_S + C_{it}} \tag{2.18}$$

Using eq. (2.1) and eq. (2.2), the interface trap capacitance can be found as follows *[6], [7]*,

$$C_{it} = \left(\frac{1}{C_{LF}} - \frac{1}{C_{Ox}}\right)^{-1} - \left(\frac{1}{C_{HF}} - \frac{1}{C_{Ox}}\right)^{-1} \tag{2.19}$$

The interface trap density D_{it} can be calculated from C_{it} from, $D_{it} = \frac{C_{it}}{e^2}$ [6], [7], here e is the charge of electrons. Therefore,

$$D_{it} = \frac{C_{ox}}{e^2}\left(\frac{C_{LF}/C_{Ox}}{1 - C_{LF}/C_{Ox}} - \frac{C_{HF}/C_{Ox}}{1 - C_{HF}/C_{Ox}}\right) \tag{2.20}$$

Eq. 2.4 gives an expression of D_{it}, in terms of applied gate voltage, however D_{it} can be represented in terms of energy by observing the band bending in the oxide semiconductor interface due to the application of gate bias. In this regard, the change in surface potential $\psi_s(V_G)$ for the application of a gate voltage V_G from its flat band point $\psi_s(V_{FB})$ can be calculated using Berglund's integral [7],

$$\psi_s(V_G) - \psi_s(V_{FB}) = \int_{V_G}^{V_{FB}} [1 - C_{LF}/C_{Ox}]\, dV \tag{2.21}$$

Finally, the energy position can be extracted from,

$$E_C - E_T = \frac{E_g}{2} + \psi_s - \psi_B \tag{2.22}$$

$$E_T - E_V = \frac{E_g}{2} - \psi_s + \psi_B \tag{2.23}$$

2.5

Here, E_g represents semiconductor bandgap, and ϕ_B is the bulk potential. A typical simultaneous hi-lo cv curve is shown in Figure 2.12 (a) and the D_{it} extracted from it is shown in Figure 2.12 (b).

While measuring the D_{it} profile, the energy levels depend on the response times of interface states. The time constant for electron emission from an interface state to the conduction band in an n-type semiconductor can be written as [7], [11]

$$\tau_n(E) = \frac{1}{\sigma_n v_T N_C} \exp\left(\frac{E_C - E_T}{kT}\right) \quad (2.24)$$

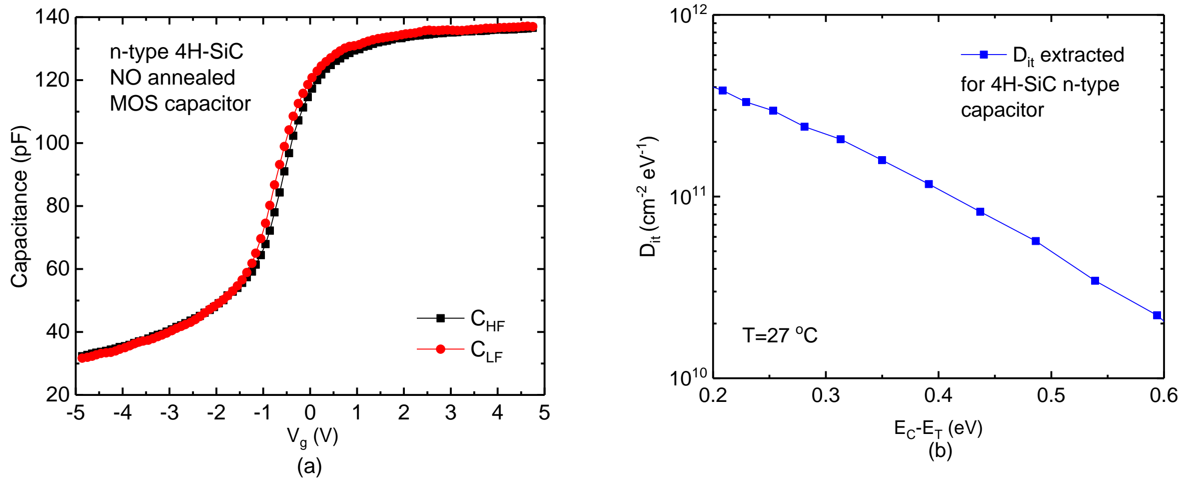


Figure 2.12: (a) Typical high frequency and low-frequency capacitance versus gate voltage for an n-type NO annealed 4H-SiC MOS capacitor. (b) The value of the D_{it} versus energy curve was extracted from the simultaneous Hi-Lo CV measurements.

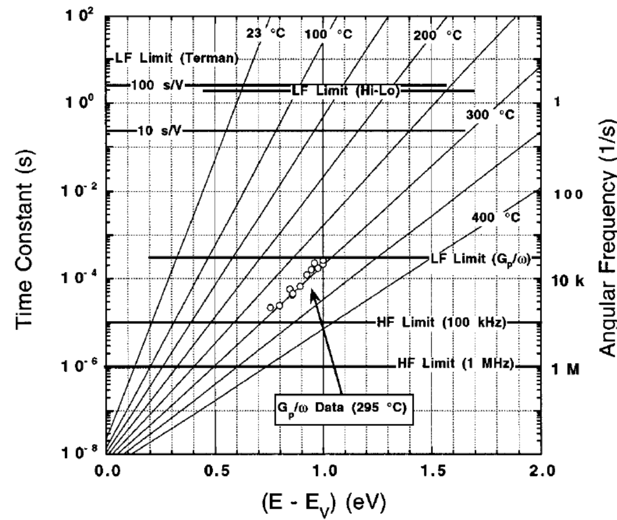


Figure 2.13: Example of hole emission time constant from an interface state to valence band [11].

Similarly for holes in a p-type semiconductor,

$$\tau_p(E) = \frac{1}{\sigma_p v_T N_V} \exp\left(\frac{E_T - E_V}{kT}\right) \tag{2.25}$$

The energy ranges to find D_{it}, change with the temperature of the capacitor. Figure 2.13 shows hole emission the time constant versus energy ranges at different temperatures with an interface trap cross-section of 10^{-15} cm^2. From this plot, the energy ranges for room temperature D_{it} measurements are valid from 0.2 to 0.6 eV from near the conduction band or valence band for electrons and holes respectively.

2.4. Photo CV

To measure interface traps and border traps present deeper in the band gap photo-assisted CV measurements can be used [11]–[13]. First, a capacitor is illuminated with UV lights while biased at deep depletion. UV illumination creates an inversion layer at the interface. For a p-type capacitor, the positively charged deep donor-like states capture electrons and become neutral at

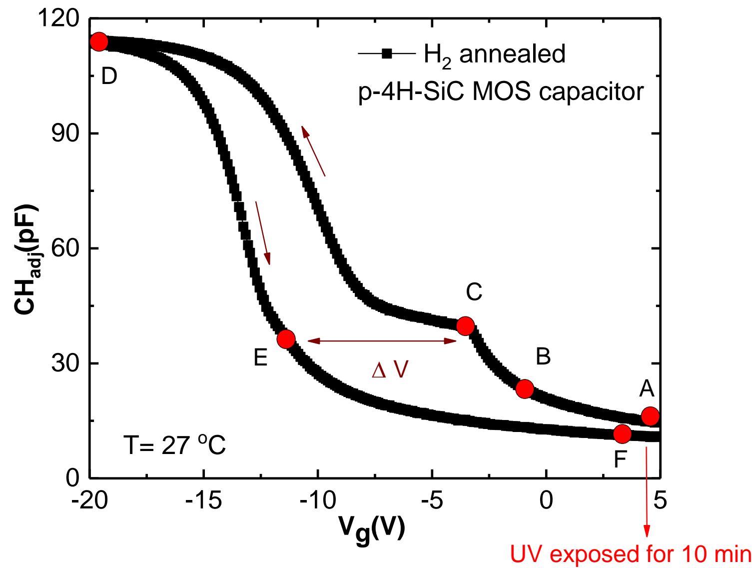


Figure 2.14: Photo CV measurements on a p-type 4H-SiC capacitor. The gate oxide is formed by thermal oxidation and post oxidation H_2 annealing at 1000 °C for 30 minutes. The UV wavelength used is 254 nm.

point A of Figure 2.14. From A to B the inversion layer is maintained at the interface that makes

the capacitance constant. At point B the capacitance increases due to the decrease of the depletion layer width. at point, C holes come near the neutrally charged deep states. At this stage, the deep-states start to capture holes and become positively charged. Due to the change in charge states of these deep traps, “a constant capacitance ledge” [14] is visible at point C, offering a sign of the presence of deep states.

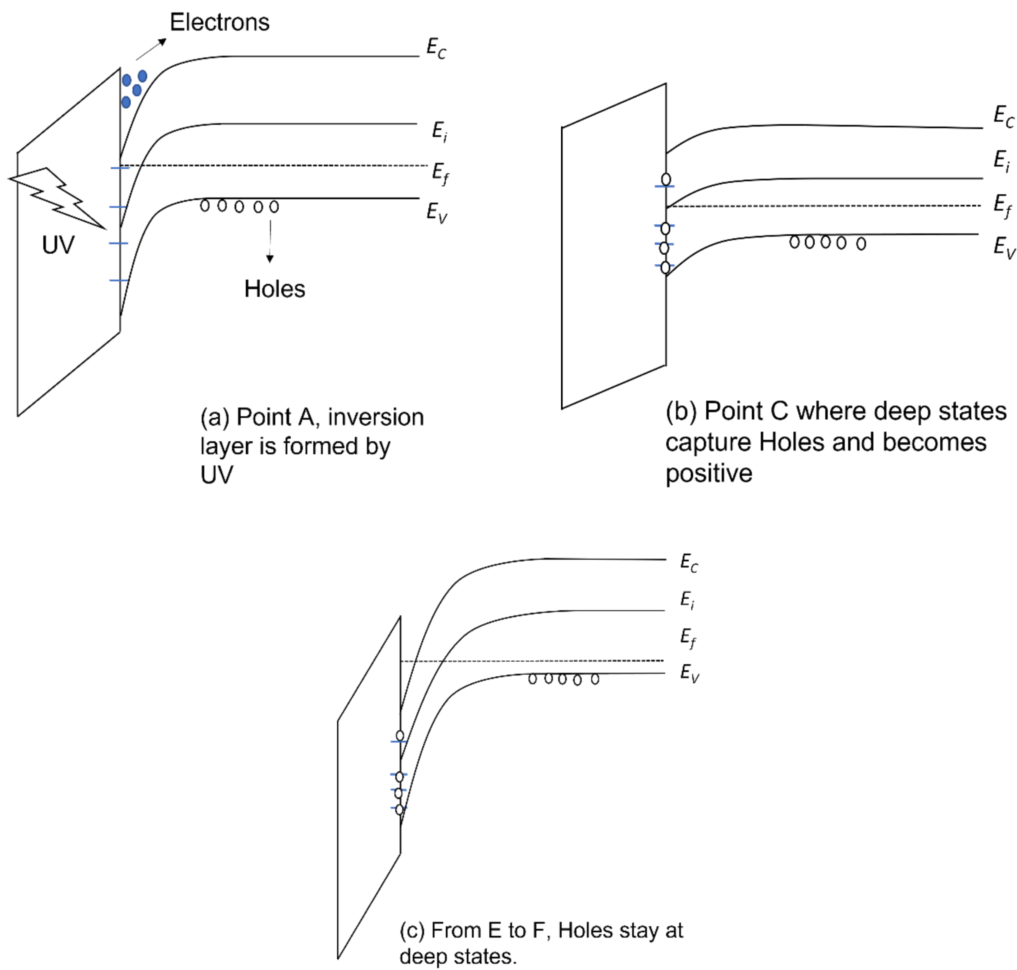


Figure 2.15: Energy band diagram [13] of p-type capacitor explained in Figure 2.14 (a) represents point A when the UV light is exposed for 10 minutes and an inversion layer is formed. (b) Denotes point C when the neutral deep traps accept holes and becomes positively charged. (c) Explains E to F when the trapped holes cannot go back to E_V due to the long emission time constant.

Once the holes are captured at the deep states, they cannot return to the valence band through thermionic emission due to the long emission time constant. At point D all the states are filled with holes and the states remain positive during the returning sweep from D to E to F. From the voltage difference ΔV_{deep} at this ledge, deep states ($N_{it,deep}$) are calculated as [7], [11], [13],

$$N_{it,deep} = \frac{C_{ox}\Delta V_{deep}}{Ae} \tag{2.26}$$

2.5. MOSFET

MOSFETs are the building block of integrated circuits. Based on the carrier types (electrons or holes) they can be classified into n-channel and p-channel MOSFET. Additionally, they can also be categorized according to the modes of operation as depletion mode which is normally on at zero gate bias, and enhancement mode, or normally off MOSFETs at zero gate bias. As this thesis mostly focuses on p-channel MOSFET, the structure of an enhancement mode p-channel lateral MOSFET is shown below, and its basic operation is discussed. In Figure 2.16 p+ regions are called source (S) and drain (D) that are heavily doped (~10^{20} cm^{-3}) layers with acceptor-like dopants. Similarly, the body terminal (B) is heavily doped with donor-like dopants that are kept grounded under normal operation. The dielectric layer is formed in between the source and drains. The gate connection (G) is formed by putting metal on top of it. Note that together the gate connection, dielectric, and semiconductor form an n-type capacitor. In the enhancement mode MOSFET, the application of voltage to the drain terminal with respect to the source simply does not turn on if the gate voltage is zero. At this condition, if the gate voltage (V_g) is increased and passed a certain voltage called threshold voltage (V_{th}) then an inversion layer is formed between the source and drain. In the case of p-channel MOSFET, an increase of negative gate voltage forms

an inversion layer of holes just below the oxide as shown by the red layer and holes start to flow from source to drain giving rise to a drain current (I_D).

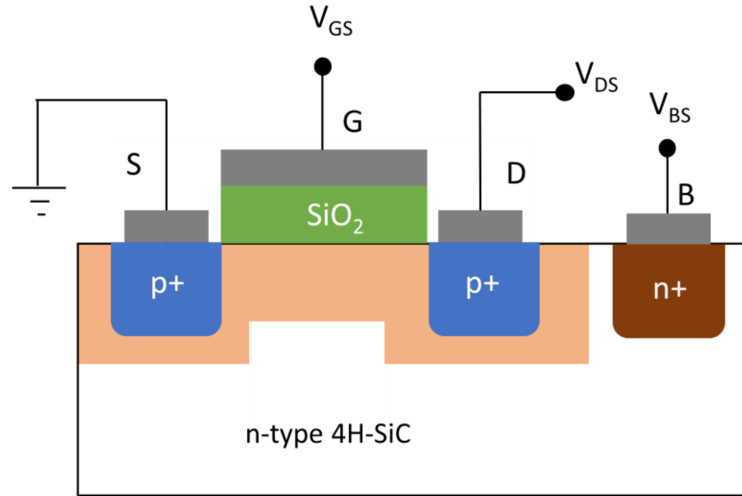


Figure 2.16: Schematic diagram of lateral p-channel MOSFET. S, D, G, and B represents the source, drain, gate, and body connections respectively.

At $|V_g| > V_{th}$, when the inversion layer forms the band bends as shown in Figure 2.7 (a). The value of V_{th} can be determined [6] in terms of the bulk potential ψ_B, flatband voltage V_{FB},

$$V_{th} = V_{FB} + 2\psi_B + \frac{\sqrt{2\epsilon_s e N_D (2\psi_B)}}{C_{ox}} \tag{2.27}$$

Here N_D is the substrate doping concentration, e is the electron/or hole charge C_{ox} is the oxide capacitance, and ϵ_s is the semiconductor capacitance.

2.5.1. Current-voltage relationship

Let's consider a gate voltage $|V_g| > V_{th}$ is applied to a MOSFET with channel length L and width W when a small V_{DS} is applied (linear region). Considering a continuous channel forms along the x-axis or in the linear operation region, the drain current can be represented in terms of the inversion charge Q'_p forms at the channel due to the electric field E_x as [5],

$$I_x = W\mu_p Q_p' E_x \tag{2.28}$$

Applying Gauss' law, the total inversion charge can be calculated [5] as,

$$Q_p' = C_{ox}(V_g - V_{th} - V_x) \tag{2.29}$$

Therefore, the total drain current can be written as,

$$I_D = \int_0^L I_x dx = \int_0^L W\mu_p Q_p' E_x dx \tag{2.30}$$

$$I_D = \int_0^L W\mu_p C_{ox}\left(V_g - V_{th} - V_x\right) E_x dx \tag{2.31}$$

$$I_D = \frac{W\mu_p C_{ox}}{L}\int_0^{V_D}\left(V_g - V_{th} - V_x\right) dV_x \tag{2.32}$$

Solving the above equation I_D becomes,

$$I_D = \frac{W\mu_p C_{ox}}{L}[(V_g - V_{th})V_D - V_D^2] \tag{2.33}$$

In the calculation of field effect mobility $\mu_{p,FE}$ transfer characteristic curves (I_D-V_g) at linear region ($V_D \rightarrow 0$) are used. An important parameter transconductance [$g_m = (\frac{dI_D}{dV_g})_{V_D \rightarrow 0}$] can be used to find $\mu_{p,FE}$.

From Eq. 2.33,

$$\mu_{p,FE} = \frac{L}{W C_{ox} V_D}(\frac{dI_D}{dV_g})_{V_D \rightarrow 0} \tag{2.34}$$

Field effect mobility is a very useful parameter that gives an overall picture of channel conductance. However, the calculation of field effect mobility gets hampered by trapped carriers at the channel due to interface states [8], [10]. A more rigorous and accurate calculation of mobility can be done by using MOS Hall measurements. The basics of Hall measurements and their application to find Hall mobility are discussed later.

2.5.2. Substrate/body bias effect on MOSFET

The fourth terminal of a MOSFET in Figure 2.16 is the body terminal that acts as a knob to control the biasing condition of the substrate with respect to the source. This terminal could be an important parameter to study channel scattering processes and carrier transport [15]–[17]. Here, the effect of body/substrate bias effect on a p-channel MOSFET is discussed. For n-channel MOSFET it works similarly, only the polarity reverses.

In the discussion of the previous section, the body connection was at the same ground potential as the source. When V_{BS}=0 the inversion happens at $\psi_s = 2\psi_B$ as discussed earlier. Now if a positive V_{BS} is applied, the surface will try to make an equilibrium at $\psi_s = 2\psi_B + V_{BS}$ as shown in Figure 2.17 [5], [8]. Here E_{fn} represents the Fermi level from n-well to the source through the reverse biased body-source junction. A positive V_{BS} makes the body-to-source junction reverse biased. This increases the positive space charge near the body region. To compensate for this extra positive space charge, the negative charge on top of the gate metal should increase. In other words, a more negative gate voltage is needed to turn on the MOSFET when $V_{BS} > 0$. Therefore, the threshold voltage increases. On the other hand when $V_{BS} < 0$, depletion width decreases and threshold voltage also drops. The change in threshold voltage (ΔV_{th}) in an ideal condition due to the application of V_{BS} can be derived by monitoring the change in space charge density upon application of V_{BS} [5], [8] as,

$$\Delta V_{th} = \frac{\sqrt{2q\epsilon_s N_D}}{C_{ox}}[\sqrt{2\psi_B + V_{BS}} - \sqrt{2\psi_B}] \quad (2.35)$$

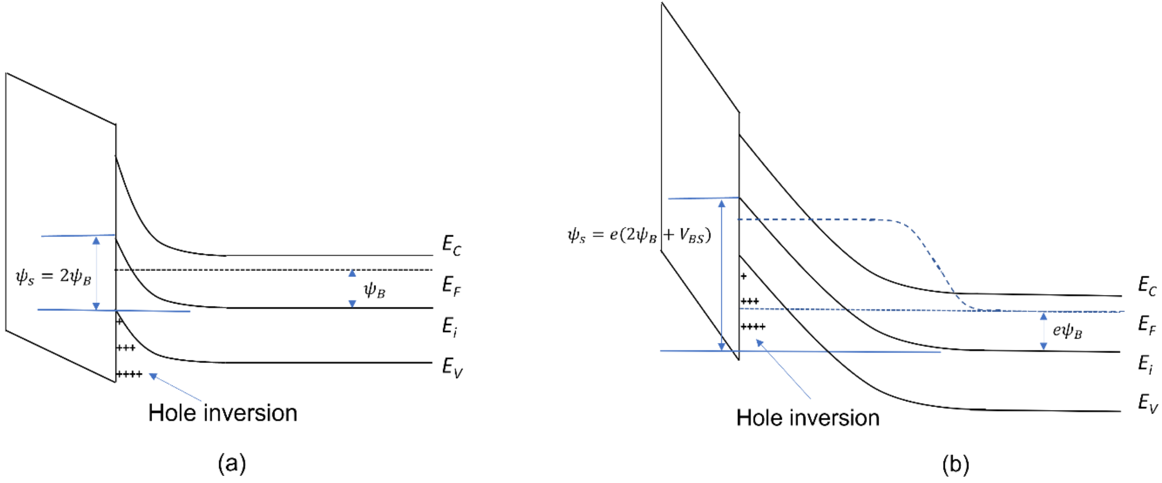


Figure 2.17: Energy band diagram for p-channel MOSFET with (a) zero body bias. (b) when a reverse body bias V_{BS} is applied.

2.6. Hall measurements

2.6.1. Theory

The mobility of a MOSFET can be measured using several methods. The most comprehensive technique to detect channel carrier concentration and MOSFET mobility is Hall analysis as used in different chapters of this thesis [18]. Therefore, the basics of Hall analysis and the measurement methods used here are discussed below.

As shown in Figure 2.18 that when a semiconductor carrying a current I_x is placed in a perpendicular magnetic field B_z to the current, the charge carriers namely electrons and holes flowing with velocity v_x in the semiconductor experiences a force called Lorenz's force. Due to this force electrons and holes are pushed towards the edges and develop a voltage called Hall voltage (V_H). At equilibrium, the magnetic and the developed electric field balance each other,

$$F = e(E + v \times B) = 0 \quad (2.36)$$

This gives,

$$E_H = v_x B_z \tag{2.37}$$

Here, E_H is the associated electric field due to charge separation.

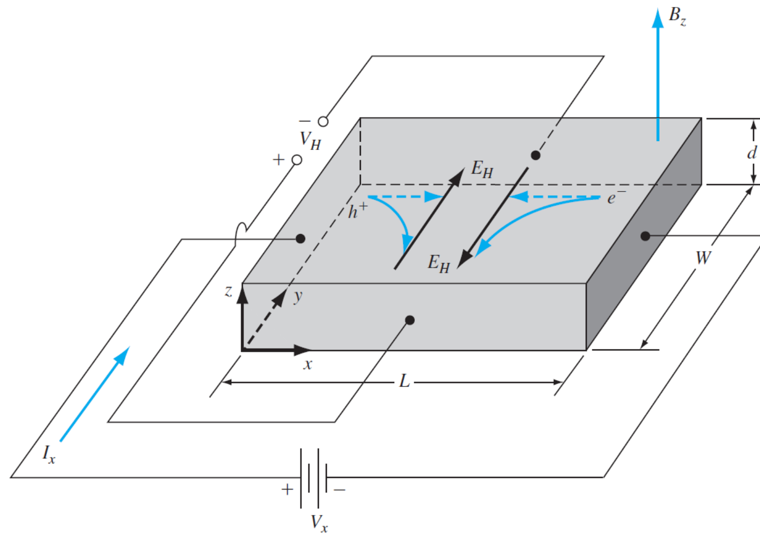


Figure 2.18.: Hall measurement setup. A current (I_x) carrying semiconductor is placed under a perpendicular magnetic field B_z where the deflected carriers due to Lorentz force develop Hall voltage V_H. L, W, and d are the length, width, and depth respectively of the semiconductor [5].

If W is the width of the semiconductor,

$$V_H = W E_H \tag{2.38}$$

Putting eq. (2.37) into eq. (2.38),

$$V_H = W v_x B_z \tag{2.39}$$

For a p-type semiconductor where holes are the majority carriers,

$$v_x = \frac{J_x}{e p_s} = \frac{I_x}{e d W p_s} \tag{2.40}$$

Now using eq. (2.39) and (2.40), p_s can be estimated as,

$$p_s = \frac{I_x B_z}{e d V_H} \tag{2.41}$$

Similarly, for an n-type semiconductor, the absolute value of the carrier concentration is given by,

$$n_s = \frac{I_x B_z}{e d V_H} \tag{2.42}$$

The hole mobility μ_p is related to the current density J_x as,

$$J_x = e p_s \mu_p E_H \tag{2.43}$$

Therefore, μ_p can be calculated from eq. (2.41) and (2.43),

$$\mu_p = \frac{I_x L}{e p_s V_H W d} \tag{2.44}$$

Similarly, the electron mobility is given by,

$$\mu_n = \frac{I_x L}{e n_s V_H W d} \tag{2.45}$$

2.6.2. MOS Hall measurement structure

To find out carrier concentration and channel mobility in a metal oxide semiconductor, the following Hall bar MOSFET structure is fabricated as shown in Figure 2.19. Here S, D, B, and G represent the source, drain, body, and gate contacts respectively. The hall voltage terminals are represented by Vh1, Vh2, Vh3, and Vh4. The MOSFET structure is placed under a perpendicular magnetic field of 0.6 T. The electrons and holes are separated due to Lorentz's force and create a voltage difference V_H. The resistivities are calculated from the Hall voltage difference measured from the hall contacts as follows [8],

$$\rho_x = \frac{(Vh1 - Vh4)}{I_D}\frac{W}{L'} \tag{2.46}$$

$$\rho_y = \frac{(Vh1 - Vh2)}{I_D}\frac{W}{L'} \tag{2.47}$$

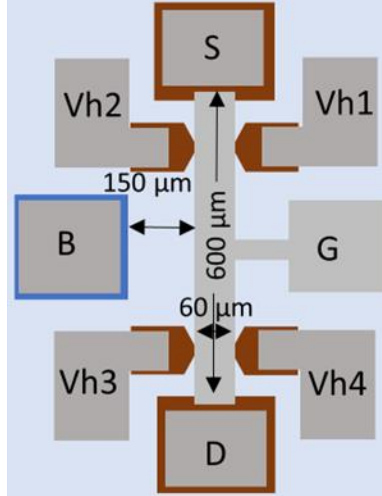


Figure 2.19.: Top view of fabricated MOS Hall bar with gate width 60 µm and gate length 600 µm.

Now from two equations, the carrier concentration can be obtained as [8],

$$n_s = \left(e\frac{d\rho_y}{dB}\right)^{-1} = \frac{I_d/e}{dV_H/dB} \tag{2.48}$$

The electron Hall mobility for an n-channel MOSFET can thus be determined as [8],

$$\mu_{H,n} = \frac{\sigma_0}{en_s} \tag{2.49}$$

Similarly for p-channel MOSFET, the hole Hall mobility is given by,

$$\mu_{H,p} = \frac{\sigma_0}{ep_s} \tag{2.50}$$

Here σ_0 represents the channel conductivity of the MOSFET.

2.6.3. Hall bar MOSFET Fabrication Steps

Figure *2.20* shows the major steps of p-channel MOSFET fabrication. It is fabricated on a 4° off-axis (0001) Si-face oriented 4H-SiC substrate having an n-type epilayer (N_D-N_A= 6.2 $\times 10^{15}$ cm^{-3}). The source/drain p^+ regions were formed by Al implantation using multiple ion energies at 700 °C with an average concentration of 6×10^{19} cm^{-3} to form a nominally uniform Al profile to a depth of 0.6 μm. Body contact regions were formed by Nitrogen implantation. The implanted dopants were activated by annealing at 1650 °C for 30 minutes in flowing Ar with a graphitic cap to protect the surface. A thick oxide layer (500 nm) is deposited using the low-pressure chemical vapor deposition (LPCVD) method to form field oxide (FOX). This layer prevents cross-talk

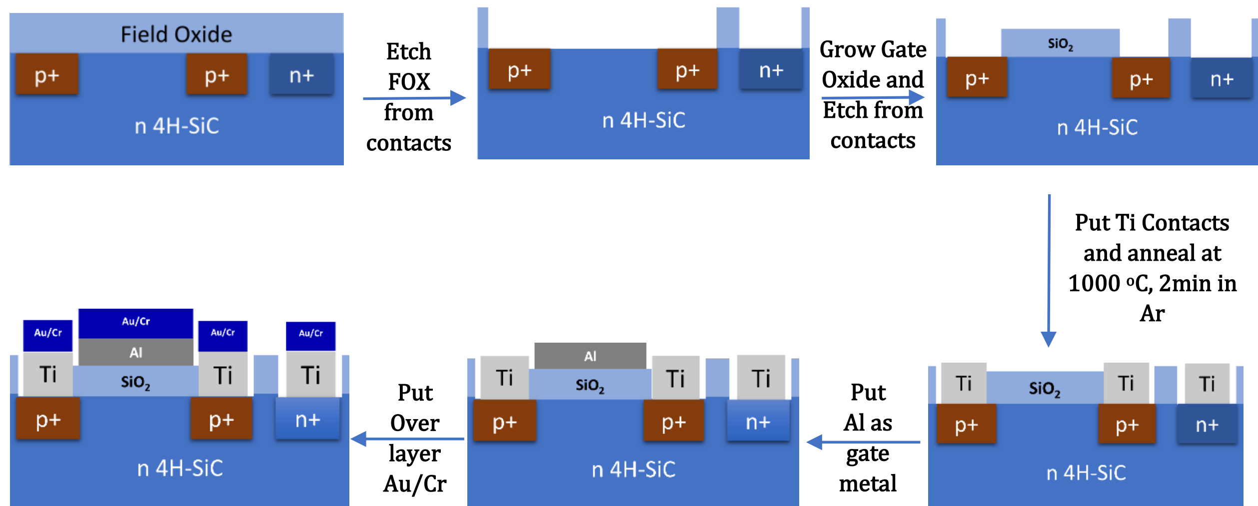


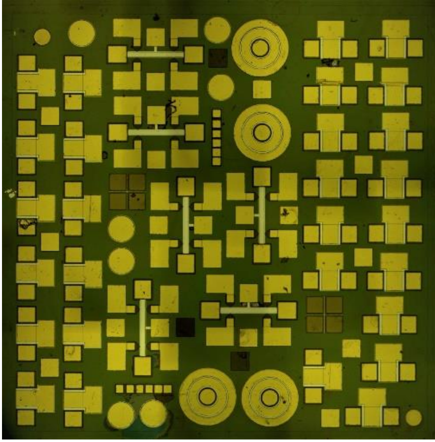
Figure 2.20: p-channel MOSFET fabrication process flow. Any post oxidation annealing (N_2 or NO) is performed immediately after the gate oxide is grown.

between devices on the same chip. The FOX is then etched from the contacts and gate regions using the reactive ion etching (RIE) method. The gate oxide is grown at 1150 °C for 10 hours

followed by post oxidation annealing (POA) at 1175 °C in a quartz tube furnace. Any kind of post oxidation annealing was done at this stage immediately after the gate oxidation. Later using contact photolithography and reactive ion etching (RIE) the oxide from the source/drain/body (S/D/B) regions and Hall voltage (V_h) terminals are removed. Afterward, Ti was sputtered and lifted-off to define the S/D/B/V_h contacts that were then annealed at 1000 °C for 2 minutes in Ar to make them ohmic. Afterward, aluminum (55 nm) was thermally evaporated for the gate metal and patterned using lift-off. Later, an overlayer of Au/Cr was sputtered on all the contacts for better connection. Here the T-shaped p-channel MOSFETs have a width × length of 200 μm × 200 μm and p- channel MOS Hall bars are 60 μm × 600 μm.

2.6.4. Hall measurements system

A fabricated Hall bar MOSFET looks as shown in Figure 2.21 (a). Following fabrication of the Hall bar MOSFET, it is attached with a thermally conductive epoxy to a gold platted ceramic chip shown in Figure 2.21 (b). For better attachment of the device to the ceramic chip, the system is baked at 120 °C for 4 hours. Later, to make the connection between the gold platted chips and the device, gold wires are bonded using the wedge wire bonding method [19]. Wire bonding is conducted in the Department of Electrical Engineering at Auburn University. Followed by wire bonding, the device with the ceramic chip is mounted on the sample holder of the Hall system shown in Figure 2.22 (a). The connection pins make contact with the gold plates of the ceramic chip. Afterward, the sample holder is inserted into the Hall system in between two electromagnets as shown in Figure 2.22 (b). Next, the system is closed, and the vacuum is pulled for Hall measurements under a perpendicular magnetic field of 0.6 T.



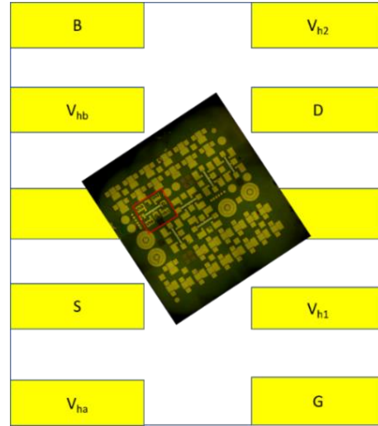
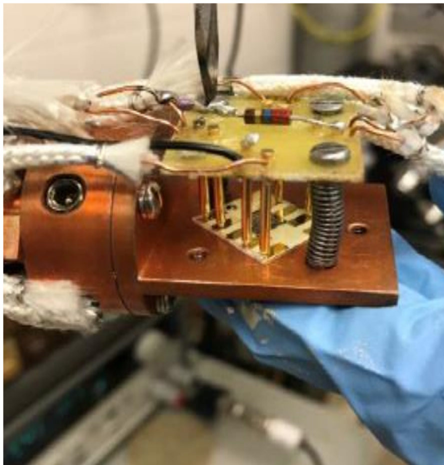


Figure 2.21: (a) Fabricated MOSFET. (b) MOSFET is attached to the gold platted ceramic chip with epoxy.



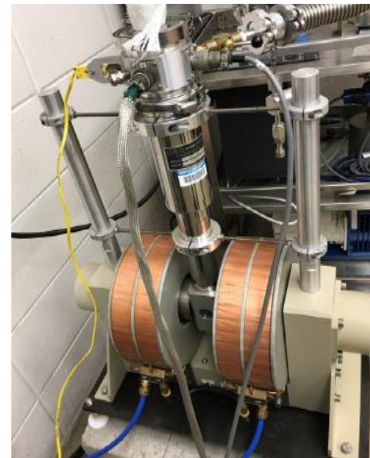


Figure 2.22: (a) Ceramic chip with MOSFET is mounted on the Hall system sample Holder for connection with the system. (b) Electromagnets where the sample is inserted in between.

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Chapter 3

Interface states passivation for p-channel 4H-SiC MOS devices

Part of this chapter is published in 2021 ECS, *Meet. Abstr.* MA2021-02 993

3.1. Abstract

Several post oxidations annealing treatments are used to passivate interface states in p-type 4H-SiC MOS devices. Among others, nitric oxide (NO) and hydrogen (H_2) post oxidation annealing were the most effective in reducing interface traps and positive fixed charges in SiO_2/4H-SiC interface for p-type semiconductors. NO annealing reduces maximum shallow traps, while the effect of H_2 is more obvious in passivating deep traps evident from photo-assisted CV measurements. Overall, NO annealing turns out to be the best passivation method among the annealing treatments used. Later, a thickness-dependent study using NO annealing is conducted, that reveals different oxidation rates of n- and p-type 4H-SiC. Furthermore, oxide thickness is optimized for MOSFET fabrication using NO annealing for a later stage.

3.2. Introduction

Impressive material properties such as wide band gap, high breakdown electric field, and thermal conductivity make silicon carbide (4H-SiC) an attractive semiconductor for high-power and high-temperature electronics [1]–[3]. Applications include, but are not limited to, power and control systems in hybrid and electric vehicles, space crafts, and renewable energy sources [4], [5]. In addition to discrete power components, an advanced 4H-SiC complementary metal-oxide-semiconductor (CMOS) integrated circuit technology has the potential to revolutionize high-temperature electronics, for operational temperatures greater than 200 ºC [6]–[8], where Si is not efficient or usable. CMOS requires both n-channel (electron) and p-channel (hole) metal-oxide-

semiconductor field effect transistors (MOSFETs) and it is critical for both polarities to have adequate performance.

In n-channel 4H-SiC devices, nitrogen incorporation at the SiO_2/4H-SiC interface reduces interface state density (D_{it}) energetically located in the upper half of the 4H-SiC band gap and near the conduction band-edge [9]–[11]. Research on the p-channel is less extensive, but prior research uses wet oxidation [12] that motivates hydrogen and more recent studies suggest nitridation [11], [13] as effective passivation agents for donor-like traps in the lower half of the 4H-SiC band gap.

Here we investigated several post-oxidation annealing (POA) processes involving NO and H_2 for D_{it} passivation in p- and n-type MOS capacitors. The results show that NO and H_2 both reduce D_{it} in the upper and lower half of the 4H-SiC band gap, with NO having a much larger effect. The reduction of positive trapped charge lowers the flat band voltage for p-type 4H-SiC MOS capacitors with different degrees of passivation. The D_{it} profile near the band-edges, extracted from simultaneous high (100 kHz) - low-frequency CV (quasistatic) at room temperature, highlights the large reduction associated with NO. The effect of hydrogen is primarily in the reduction of energetically deep interface traps. To measure the density of the deep traps ($N_{it, deep}$), photo-assisted CV measurements were carried out, from which $N_{it, deep}$ was calculated. Overall, the results confirmed that 2 h NO annealing at 1175 °C results in the lowest D_{it} in the lower half of the band gap, and the same is true for 4 h NO annealing in the upper half.

3.3. Device Fabrication

In this work, metal-oxide-semiconductor (MOS) capacitors were fabricated on p-type (N_A-N_D= 6.2×10^{15} cm^{-3}) and n-type (N_D-N_A= 2.0×10^{16} cm^{-3}) epitaxial layers on 4° off-axis (0001) Si-face oriented substrate. All samples were oxidized at 1150 °C for 10 h to grow an oxide film and some samples were subjected to post oxidation annealing (POA) for comparative studies of D_{it}.

The thicknesses of the gate oxides for the n- and p-type capacitors were found to be ~55 nm and ~65 nm respectively, by the capacitance-voltage (CV) method. The various samples are labeled according to the process as follows. 'As-Ox' represents a sample without any POA. The samples called 'NO_2' and 'NO_4' are annealed in nitric oxide (NO) at 1175 °C for 2 and 4 h, respectively (flow rate). The 'H_2' sample is annealed at 1000 °C for 30 min in flowing hydrogen gas (flow rate). 'NO+H_2' represents samples that went through 2 h NO annealing at 1175 °C and 30 min H_2 annealing at 1000 °C consecutively.

3.4. Results

3.4.1. Capacitance voltage measurements

Figure 3.1 shows high-frequency CV curves comparison for the different processes for p-type MOS capacitors. As-Ox sample has the highest negative flat band voltage due to high D_{it} and positive fixed charge, $(N_{eff} \rightarrow D_{it} + Fixed\ charge)$. Samples H_2, NO+H_2, and NO_4 reduces

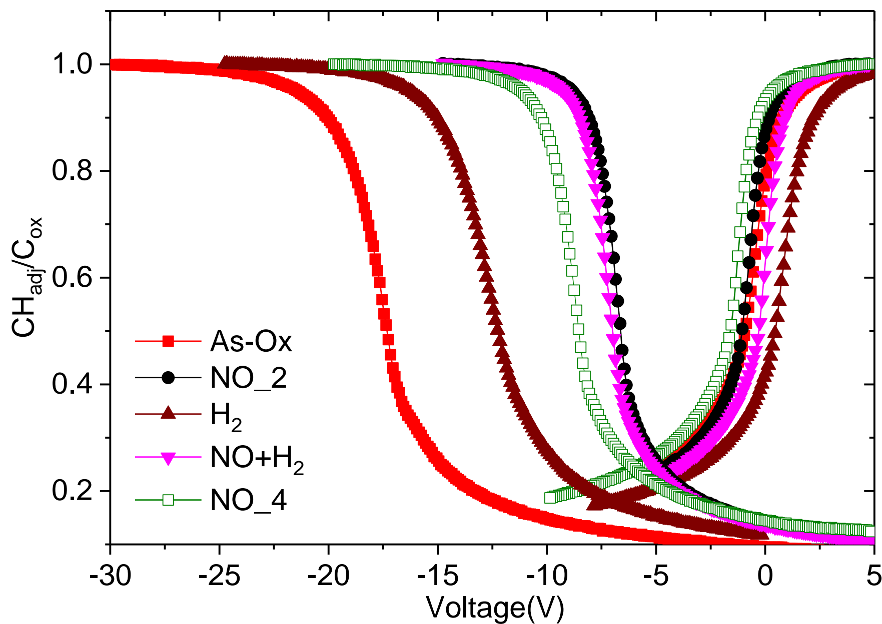

Figure 3.1: High frequency (100 kHz) capacitance-voltage (CV) characteristics of n- and p-type 4H-SiC capacitors at room temperature (27 ºC) fabricated using different POAs.

The flat band voltage V_{fb} to different degrees, where NO was the most effective with the minimum value of V_{fb}. On the other hand, the flat band voltages for the n-type capacitors were within 0.5 V but there were significant differences in shallow D_{it} for the n-type capacitors for the different processes are shown in Figure 3.2. Next, simultaneous Hi-Lo CV was employed to compare the D_{it} near the valence (E_v) and conduction band (E_C) edges as shown in Figure 3.2. NO_2 was the most successful annealing for p-type capacitors (i.e. close to Ev) whereas NO_4 was slightly better for n-type. Hydrogen annealing does not result in passivation near E_v and E_C. This is consistent with [15] where Pt gates are used to crack H_2 catalytically to enhance hydrogen uptake and reduce

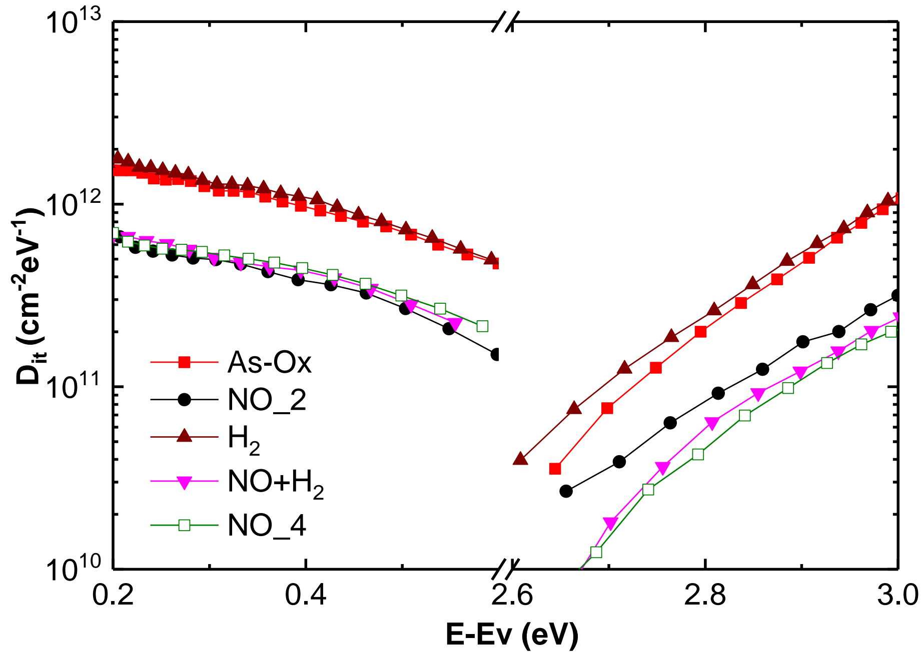

Figure 3.2. Density of shallow interface trap (D_{it}) distribution near the valence and conduction band edge for various p-type 4H-SiC capacitors fabricated using different POAs. Data are extracted from simultaneous high (100 kHz) - low-frequency CV characteristics at room temperature (27 °C).

shallow trap densities. These experiments prove that post-oxidation annealing in H2 only passivates traps deeper in the band gap, as described later. As a consequence, the NO+H_2 process results in the shallow Dit as the NO_2 for both n- and p-type capacitors.

3.4.2. Deep trap ($N_{it,\ deep}$) analysis

In standard room temperature Hi-Lo CV measurements, the value of carrier capture cross-section allows for inspecting the energy range from 0.2 to 0.6 eV [16]. To study deep interface trap passivation, photo-assisted CV measurement can be performed [16]. For this purpose, a capacitor is illuminated by ultraviolet (UV) light of frequency 254 nm for 10 min while biased at deep

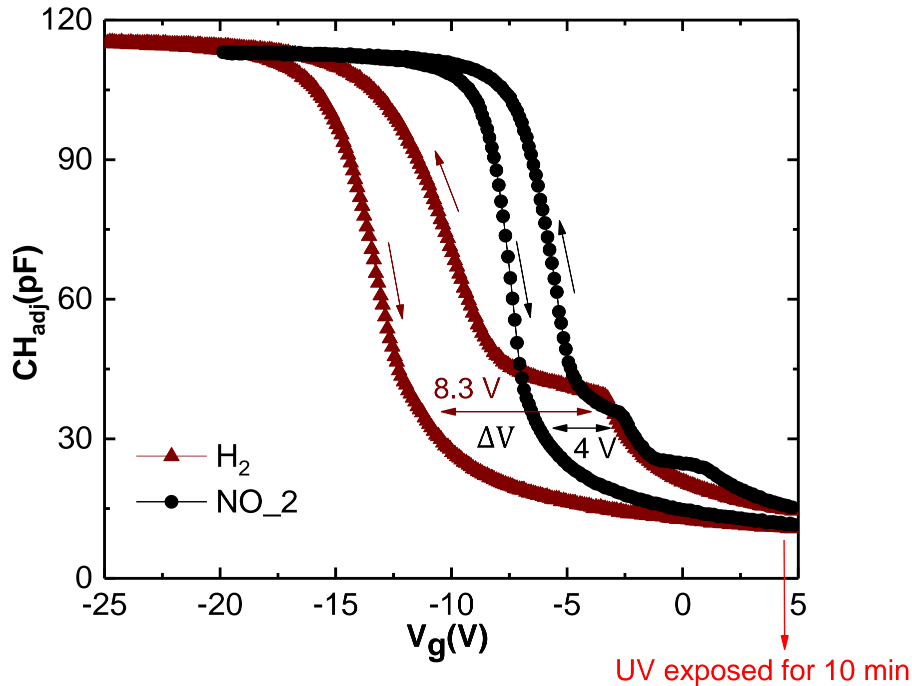

Figure 3.3. Typical photo CV for NO and H_2 annealed samples. Biased in deep depletion, the sample is exposed to 254 nm UV light to generate an electron inversion layer. The electrons recombine with deep interface traps and change their charge state. After turning off the UV, the voltage is swept from depletion to accumulation filling the traps with holes. This change in the trap occupancy creates a voltage shift ΔV_{ds} as shown. The $N_{it,\ deep}$ is calculated using $N_{it,\ deep} = \Delta V_{ds} * C_{ox} /A$ and summarized in Table 1.

depletion (+5 V). After turning off the UV, the gate voltage is swept from depletion to accumulation and then brought back to deep depletion again. UV illumination generates electron-hole pairs at the SiC surface. While the capacitor goes from depletion to accumulation, the holes are trapped in the states present at the interface but cannot relax at the return sweep due to the long

emission times associated with the energetically deep traps. This creates a constant capacitance ledge [16] in the CV curve as shown in Figure 3.3. From the associated voltage difference ΔV at this ledge deep states ($N_{it,\,deep}$) are calculated.

$$N_{it,deep} = \frac{C_{ox}\Delta V}{Ae}$$

3.4.3. $N_{it,\,deep}$ comparison between processes

A comparative analysis presented in Table 3.1 shows that among all the processes studied, 1175 °C, 2 h NO annealing has the lowest amount of $N_{it,\,deep}$, and, therefore, was most successful in trap passivation in p-type capacitors. These results also show a reduction of 40 % of total trapped charges by H_2 compared to As-Ox. This suggests that H_2 POA passivates states in the large mid-gap range consistent with [17], related to dangling bonds small C clusters [18] but is not as effective as using catalytic Pt post metallization annealing [15], [17].

Sample ID	Post oxidation annealing conditions	Thickness (nm)	$N_{it,\,deep}$ (10^{12} cm^{-2})
As-Ox	-	60.5 ± 1.0	4.6 ± 0.1
NO_2	2 hr. NO at 1175 °C	61.6 ± 0.8	1.3 ± 0.1
H_2	30 min H_2 at 1000 °C	61.5 ± 0.8	2.9 ± 0.3
NO + H_2	2 hr. NO at 1175 °C+ 30 min H_2 at 1000 °C	56.6 ± 0.7	1.5 ± 0.1
NO_4	4 hr. NO at 1175 °C	62.6 ± 1.1	1.7 ± 0.2

Table 3.1: Post oxidation annealing conditions and quantitative comparison of deep interface trap ($N_{it,\,deep}$) obtained from photo CV measurements on the respective p-type MOS capacitor.

This is also distinct from wet-oxidation /or wet-reox [12]. As observed in the above analysis from Figure 3.2 and Table 3.1 that, 2 h NO produces n- and p-type MOS capacitors with the least amount of D_{it}, and $N_{it,\ deep.}$ Therefore, a thickness-dependent study has been conducted using 2 h NO annealing to find the oxidation rate and total effective charge for different duration of oxidation. For this purpose, n- and p-type 4H-SiC samples are oxidized for 3, 6, and 10 h to obtain different oxidation thicknesses for comparison. Later these samples are annealed in NO for 2 h. An Al gate is put on top to make MOS capacitors for comparison using simultaneous Hi-Lo CV.

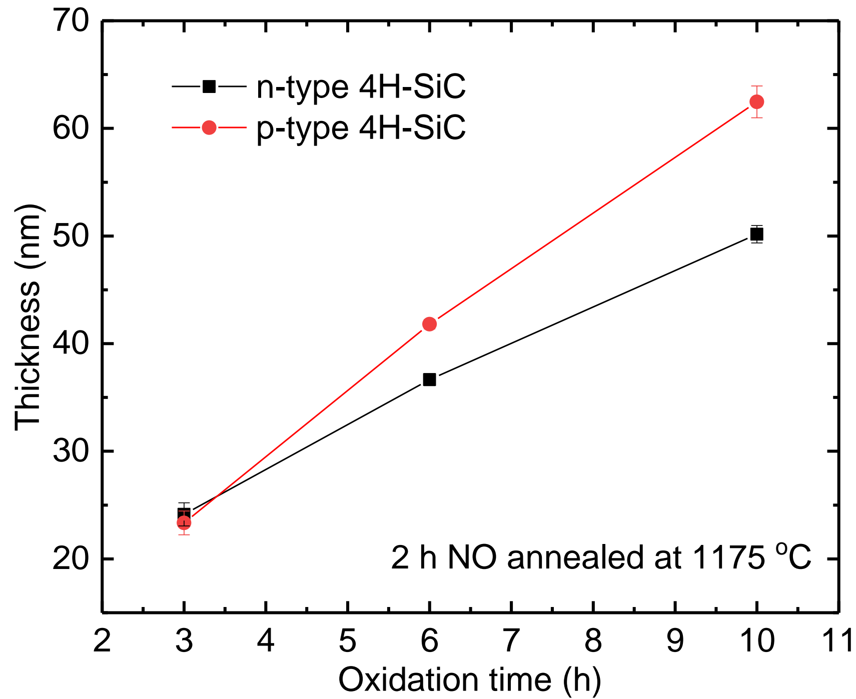

Figure 3.4: Thickness versus oxidation time for NO annealed 4H-SiC capacitors. Thicknesses are measured using Hi-Lo CV. The diameter of the capacitors is 500 μm with an Al gate on top.

Figure 3.4 shows n- and p-type capacitors fabricated using different oxidation thicknesses. It can be observed that the oxidation rate for the p-type capacitor is a little higher for the larger oxidation

durations than compared to its n-counterpart. The difference in oxidation rates can be attributed to the types and amount of dopant used for n-(nitrogen) and p- (Aluminum) type 4H-SiC.

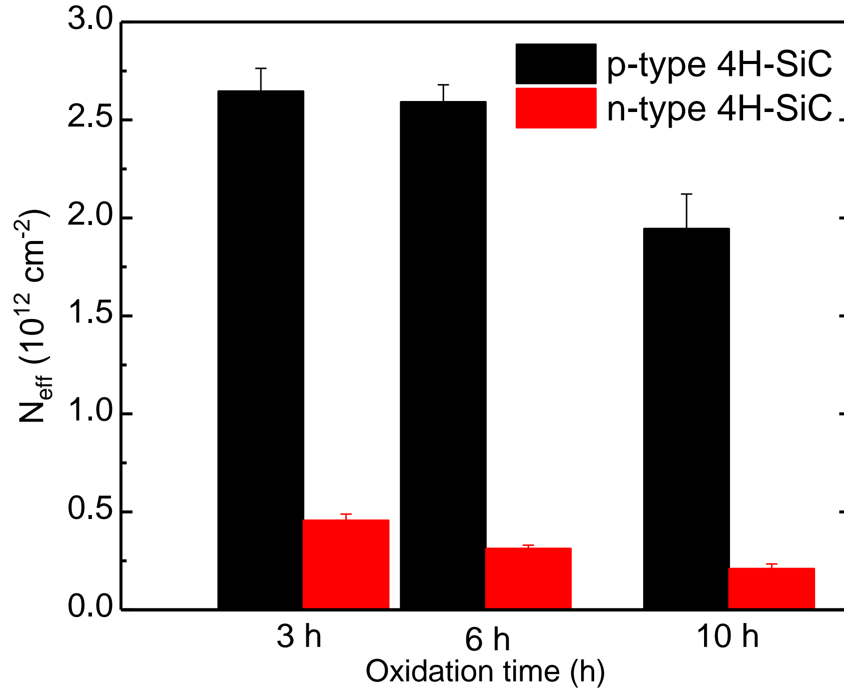

Figure 3.5: Effective charge (N_{eff}) versus oxidation time for n-and p-type capacitors fabricated using 2 h NO POA. N_{eff} is measured using simultaneous Hi-Lo CV. The diameter of the capacitors is 500 μm with an Al gate on top. Note that the oxide thicknesses are different for n- and p-type MOS capacitors for the same oxidation times.

Next, the total effective charges at the interfaces are calculated for these fabricated capacitors using simultaneous Hi-Lo CV analysis as shown in Figure 3.5. The total effective charge consists of the sum of fixed charge and interface traps. It is evident that with the increase of oxidation time, the value of N_{eff} decrease. Therefore, for the fabrication of 4H-SiC p-channel MOSFET, 10 h oxidation with 2 h post oxidation NO annealing should be used.

3.5. Summary

In conclusion, various post-oxidations annealing treatments are incorporated to reduce interface traps and fixed charges in the p-type SiO_2/4H-SiC interface. High-frequency CV curves are

compared to find degrees of passivation in fixed charges between processes. Using Hi-Lo CV D_{it} is extracted also to compare the effectiveness of these methods. Out of the annealing treatments, NO annealing seemed to passivate the maximum number of shallow traps near E_{V}. The effect of H_2 annealing is more evident from the deep passivation as apparent from the photo-assisted CV measurements. Overall, NO annealing surpasses all treatments in passivating both shallow and deep traps. Later, a thickness-dependent study using NO annealing reveals different oxidation rates for n- and p-type 4H-SiC. Furthermore, 10 h oxidation plus 2 h NO POA generates the least amount of effective charges at the interface, indicating the most effective combination of p-channel MOSFET fabrication. Based on these findings p-channel 4H-SiC MOSFET is fabricated which is discussed in the next chapter.

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Chapter 4

High-temperature characteristics of nitric oxide annealed p-channel 4H-SiC MOSFETs

Part of this chapter is published in special issues of the *Journal of Applied Physics (2021)*

4.1. Abstract

In this work, p-channel 4H-SiC MOSFETs were fabricated and analyzed at high temperatures. It is demonstrated that nitridation of the gate oxide enables enhancement mode operation in these devices. Nitrogen incorporation at the 4H-SiC/ SiO_2 interface by nitric oxide annealing reduces the interface trap density energetically located in the lower half of the 4H-SiC bandgap, resulting in viable high-temperature p-channel devices. In the 27 °C to 300 °C temperature range, the threshold voltage decreases with increasing temperature, consistent with the reduction of occupied interface traps at higher temperatures. The hole channel mobility is weakly temperature dependent under strong inversion conditions. Hall measurements support that above the threshold voltage, the mobility is limited by surface roughness scattering. In the weaker inversion, the channel conductivity is limited by interface hole trapping and Coulomb scattering. In addition, high-temperature bias stress measurements confirm a temperature-activated hole trapping under negative gate bias which requires further investigations.

4.2. Introduction

The development of high-quality large area wafers, in conjunction with a wide band gap (3.2 eV) and high thermal conductivity, makes 4H-SiC one of the most advanced semiconductors for high-temperature electronics [1], [2]. Additionally, the availability of both p- and n-type conduction places 4H-SiC as the state-of-the-art for high-temperature complementary metal-oxide semiconductor (CMOS) technology [3–6]. Motivated by high voltage power electronics, transport

and bias instability in 4H-SiC n-channel metal-oxide-semiconductor field-effect transistors (MOSFETs) have been widely studied. In contrast, significantly fewer investigations [7–10] have been reported on transport in p-channel devices. Earlier work showed that wet oxidation and/or wet re-oxidation may yield high mobility and low threshold voltage for p-channel MOSFET [11]. However, for CMOS applications, such processes would not be preferable as they do not yield adequate channel mobility for the n-channel counterpart [12]. Therefore, the study of p-channel devices fabricated using nitrided or nitric oxide (NO) annealed SiO_2 is of considerable importance.

Nitrogen incorporation at the 4H-SiC/SiO_2 interface [13], [14] decreases the interface trap density (D_{it}) in the upper half of the 4H-SiC bandgap, especially near the conduction band. After nitridation, peak field-effect channel mobility (μ_{fe}) of ~35-40 cm^2/Vs for electrons can be obtained for light p-body doping of ~10^{15} cm^{-3} [15]. In the case of hole transport, the role of nitridation is yet to be elucidated. Early work reported that hole channel μ_{fe} was poor for nitridation by N_2O annealing [16]. Nonetheless, a recent study by *Tachiki et al*. [17] demonstrates higher hole μ_{fe} with 1250 °C NO (~14 cm^2/Vs at 27 °C) and 1400 °C N_2 post oxidation (~17 cm^2/Vs at 27 °C) annealing [17].

In this study, we carry out capacitance and transport measurements on 4H-SiC/SiO_2 devices to show that NO annealing also reduces D_{it} in the lower half of the 4H-SiC bandgap over non-nitrided devices and enables high-temperature operation. We then extend the high-temperature characterization of NO annealed p-channel FETs to 300 °C. To gain insights into the temperature and density dependence of hole mobility, Hall measurements were also performed. Results show that the channel conductivity is limited by interface trapping for low carrier concentration (p_s), where hall mobility (μ_{hall}) increases with temperature. Under strong inversion, μ_{hall} is weakly dependent on temperature due to surface roughness scattering and matches that of

the field-effect mobility. In addition, the measured high-temperature bias instability of the devices is analyzed in terms of temperature-dependent oxide hole trapping.

4.3. Experimental Details

In this work capacitors were fabricated on p-type (N_a-N_d= 6.2×10^{15} cm^{-3}) and n-type (N_d-N_a= 2.0×10^{16} cm^{-3}) epitaxial layers on 4° off-axis (0001) Si-face oriented substrate. The p-channel MOSFETs (W/L=200 µm/200 µm) and MOS Hall bars (W/L= 60 µm /600 µm) were fabricated using an n-type epilayer with doping (N_d-N_a) of 6.0×10^{15} cm^{-3}. The schematic cross-section of the devices is shown in Figure 4.1 (a) and the top view of the hall bar MOSFET is shown in Figure 4.1 (b).

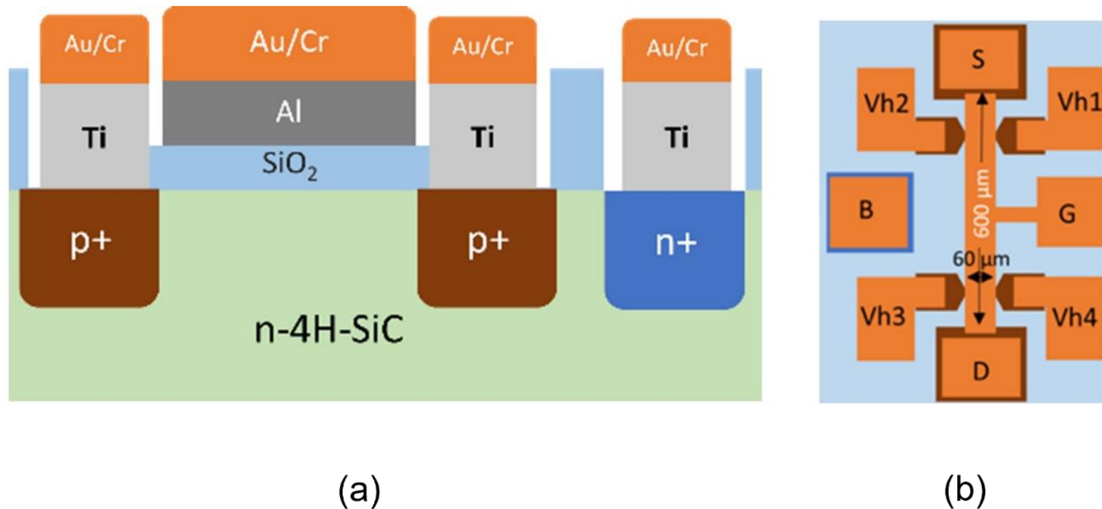

Figure 4.1:(a) Schematic diagram of the fabricated p-channel MOSFET cross-section. The layer thicknesses and dimensions are described in the text. (b) Top view of the Hall bar MOSFET with a channel length of 600 µm and channel width of 60 µm. S, B, D, and G represent source, body drain, and gate contacts, respectively. Vhs denote the four Hall voltage terminals.

The source/drain p$^+$ regions were formed by Al implantation using multiple ion energies at 700 °C with an average concentration of 6×10^{19} cm^{-3} to form a nominally uniform Al profile to a depth of

0.6 μm. Body contact regions were formed by Nitrogen implantation. Dopants were activated by annealing at 1650 °C for 30 minutes in flowing Ar with a graphitic cap to protect the surface. After the removal of the cap, a thick (500 nm) field oxide was deposited to prevent cross-talk between devices. Next, the field oxide is selectively removed from the contact and gate areas using reactive ion etching (RIE) and followed by a buffered oxide etch. Then, dry oxidation was carried out at 1150 °C for 10 hours followed by post oxidation annealing (POA) at 1175 °C for 2 hours in flowing nitric oxide (NO), in a quartz tube furnace. Control samples were also included which did not receive POA. The thicknesses of the gate oxides were ~55 nm and ~65 nm on the n- and p-type respectively, as measured by the capacitance-voltage (CV) method. The amount of interfacial nitrogen was ~ 4.2×10^{14} cm^{-2} as measured by x-ray photoemission spectroscopy (XPS) in agreement with previous reports [18]. Contact photolithography and RIE were done to remove the oxide from the source, drain, body regions, and Hall voltage terminals. Next, Ti (200 nm) was sputtered and lifted off to define these contacts. The contacts were then annealed at 1000 °C for 2 minutes in Ar to form ohmic contacts. Following this, aluminum (55 nm) was thermally evaporated for the gate metal and patterned using lift-off. Subsequently, an overlayer of Au/Cr was sputtered on all the contacts.

4.4. Results and Discussions

4.4.1. Characteristics of MOS capacitors and interface trap density

Figure 4.2 shows typical 100 kHz CV characteristics for p-type capacitors at room temperature. The p-type device without NO annealing has a very large negative flat band voltage (V_{fb}) of -18.6 V. Upon NO annealing, the V_{fb} reduces to -7.5 V. Using the difference in V_{fb} the total reduction of effective positive charge at the interface was calculated to be ~ 3.7×10^{12} cm^{-2}. This suggests that nitridation effectively removes interface traps in the lower half of the bandgap.

To obtain D_{it} profiles as a function of energy in the bandgap, simultaneous high (100 kHz)-low frequency (quasistatic) CV measurements [19], [20] were performed at room temperature (27 °C), 150 °C, and 300 °C. In Figure. 4.3 the D_{it} for both p- and n-type devices are plotted from the flat band energy at a given temperature to that of the next higher temperature. The trap energies are calculated from the gate bias dependence of surface potential and the quasistatic capacitance [21]. At 300 °C the measurable energy range is up to the mid-gap as estimated using the time constants for hole emission from interface states to E_v [22]. The change of bandgap with temperature has not been included in the analysis.

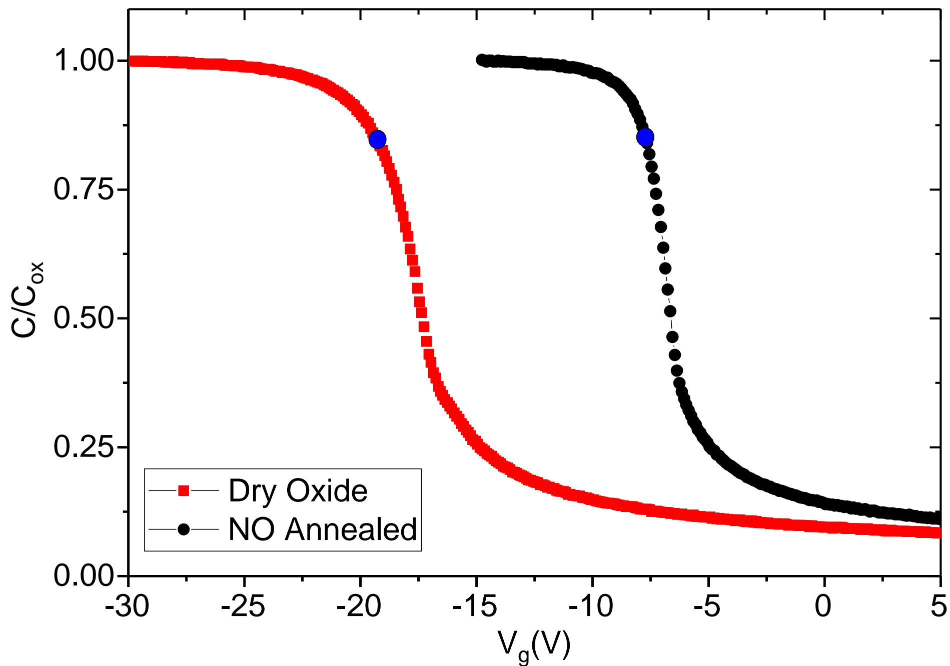

Figure 4.2: Room temperature capacitance-voltage (CV) characteristics of p-type dry oxidized and NO annealed capacitors at high frequency (100 kHz). The corresponding flat band voltages are marked with dots on each graph.

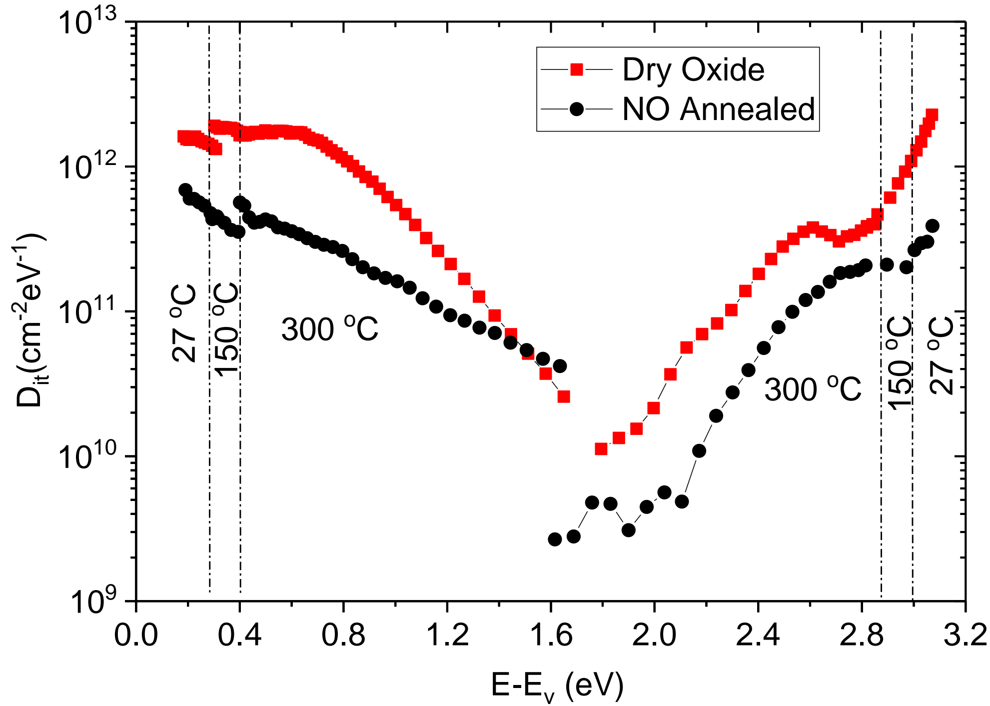

Figure 4.3: Typical D_{it} profiles for dry oxidized (red) and NO annealed (black) 4H-SiC MOS capacitors obtained by simultaneous high (100 kHz)-low-frequency CV measurements at 27 °C, 150 °C, and 300 °C. Data for energy levels below and above mid-gap are from measurements on p- and n-type capacitors respectively.

The reduction of D_{it} by NO annealing is clearly observed both near the valence and conduction band edges as well as for energies deeper in the gap. Integration of the D_{it} profiles gives a total interface trap density (N_{it}) of 1.3×10^{12} cm^{-2} and 3.3×10^{11} cm^{-2} in the lower half of the bandgap, for the dry oxide and NO annealed samples, respectively. The difference between these values is lower than the effective charge reduction calculated from the V_{fb} shift. This can be attributed to the reduction of additional positive fixed oxide charges by NO annealing. In addition, the underestimation of D_{it} using the simultaneous high-low frequency CV method near the band edges [23], could also contribute to this difference.

4.4.2. High-temperature characterization of NO annealed p-channel MOSFET

Transfer characteristics of the fabricated lateral p-channel MOSFETs were measured as a function of temperature from room temperature to 300 °C and the hole field-effect mobility (μ_{fe}) was extracted as shown in Figure 4.4. Under strong inversion, the μ_{fe} in the NO annealed MOSFET was measured to be about 8 cm^2/Vs at room temperature.

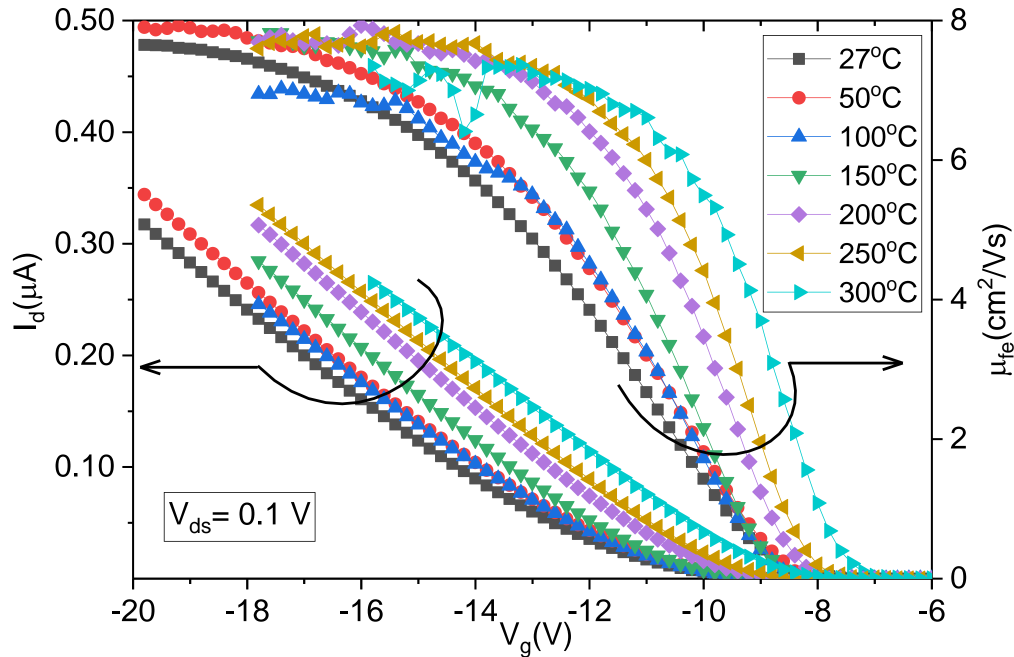

Figure 4.4: Drain current I_d and field effect mobility μ_{fe} as a function of the gate voltage V_g with the drain to source voltage V_{ds}= 0.1 V at different temperatures for NO annealed p-channel 4H-SiC MOSFET with an oxide thickness 55 nm and channel width/length equal to 200 µm/200 µm.

In contrast, it was difficult to obtain reliable data for p-channel MOSFETs fabricated without nitridation because they turned on at very large negative voltages and exhibited high gate leakage.

The improvement in the transconductance after NO annealing is consistent with the reduction of positive donor-like traps observed in CV measurements. Therefore, NO annealing not only reduces V_{th} but also provides a more operation-friendly gate voltage range for high-temperature 4H-SiC CMOS. However, the V_{th} is still quite high consistent with the large negative V_{fb} in NO annealed

p-type capacitors (Figure 4.1), which highlights the need for further reduction of positive trapped charge. The value of μ_{fe} obtained here is lower than that reported with NO annealing at 1250 °C [17] and can be ascribed to a higher D_{it} in the devices reported here. This difference is likely due to the lower NO annealing temperature employed here, and could also be attributed to the variations in the oxide thickness and ohmic contact annealing processes. A summary of the temperature dependence of V_{th} and μ_{fe} is shown in Figure 4.5. The V_{th} is extracted as the gate voltage for 1 nA current (J ~2.5 μA/cm^2) and μ_{fe} is the value at a gate voltage of -16 V (E_{ox} ~1.5 MV/cm at room temperature). As temperature increases from room temperature to 300 °C a right shift is observed in the transfer characteristics indicative of a V_{th} reduction.

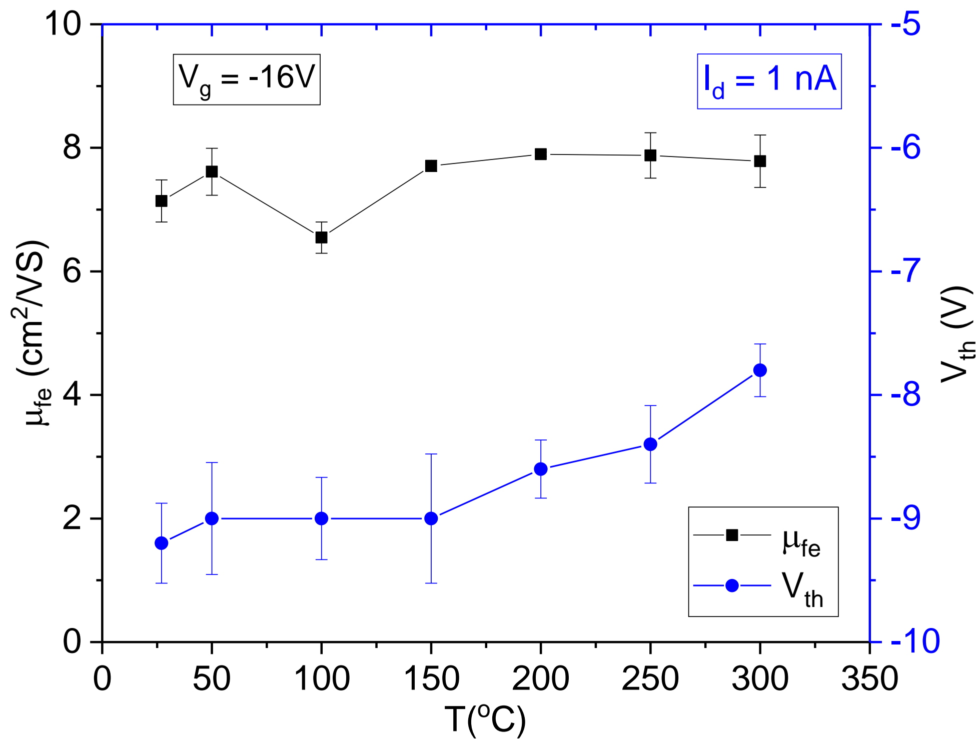

Figure 4.5: Temperature dependence of field effect mobility (μ_{fe}) and threshold voltage (V_{th}) for NO annealed p-channel 4H-SiC MOSFET. The V_{th} is extracted at 1 nA drain current and the μ_{fe} is plotted for a gate voltage of -16 V at all temperatures. The error bars signify the standard deviation of each measurement for 3 devices.

This is due to the decrease of total occupied D_{it} at higher temperatures. The μ_{fe} shows a weak temperature dependence when plotted at the fixed gate voltage. To explain the possible transport mechanisms occurring in the channel which keeps μ_{fe} nearly constant under strong inversion conditions, temperature-dependent Hall measurements were performed as discussed below.

4.4.3. MOS Hall measurements

Hall measurements were performed on fabricated Hall bar MOSFETs under a perpendicular magnetic field of 0.6 T and bias (V_{ds}) of 0.75 V. The Hall voltages are measured from four Hall terminals present perpendicular to the channel region (Figure 4.1). Devices were wire bonded to a gold-coated alumina ceramic chip carrier and placed in a temperature-controlled sample holder to

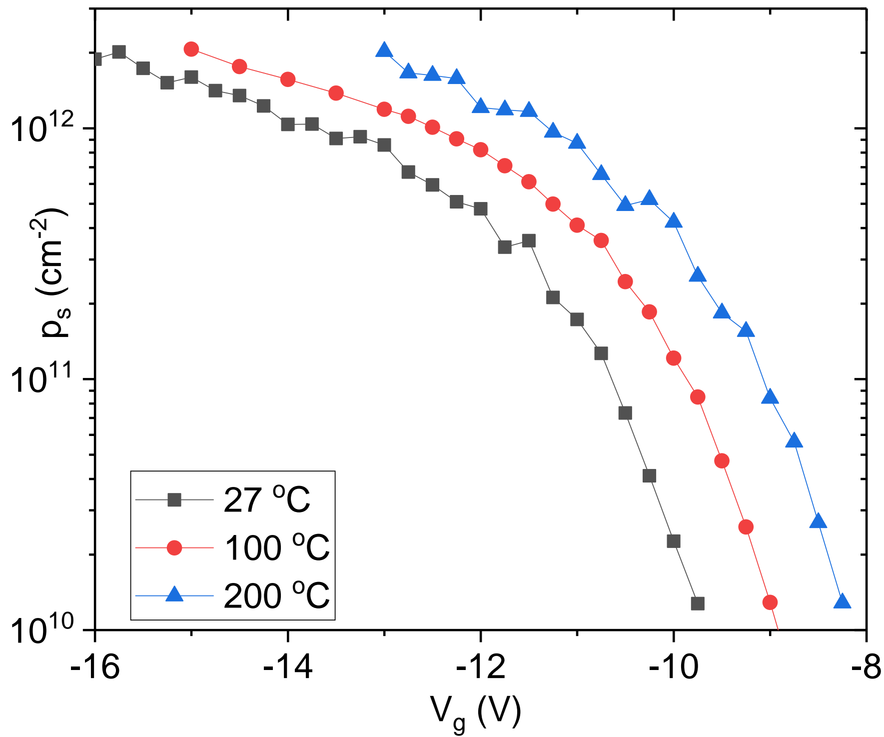

Figure 4.6: Channel hole concentration (p_s) as a function of gate voltage (V_g) at different temperatures for NO annealed 4H-SiC MOS Hall bars. Hall measurements were taken at V_{ds} = 0.75 V and under a perpendicular magnetic field of 0.6 T. Hall voltages are averaged out for the forward and reverse directional magnetic field. Device dimension: channel length/width is 600 μm/60 μm.

vary the temperature between 27 °C to 200 °C. The hole channel carrier concentration (p_s) at different temperatures as a function of gate voltage (V_g) is shown in Figure 4.6. At any temperature, as V_g is swept from depletion to inversion, i.e., towards more negative voltage, the surface Fermi level gets closer to E_v, and neutral donor-like interface traps capture channel holes. This results in a lower than ideal free hole concentration and a poor p_s-V_g slope. Once strong inversion is reached (V_g <-12 V), p_s increases much more rapidly with increasing V_g with a slope close to the ideal value of C_{ox}/e (not shown) [24]. As temperature rises, strong inversion is achieved with smaller band-bending, and the surface Fermi level at the inversion point moves closer to the mid-gap away from the valence band. This also lowers total occupied N_{it} at higher temperatures, resulting in a less negative V_{th}.

Next, the Hall mobility (μ_{hall}) was extracted using p_s and sheet resistance and plotted as a function of p_s and temperature as shown in Figure 4.7. The μ_{hall} increases with temperature in the low p_s region (< 5 x 10^{11} cm^{-2}), which can be attributed to a Coulomb scattering limited mobility. At higher p_s (> 5 x 10^{11} cm^{-2}), the temperature dependence of μ_{hall} weakens, and at even higher p_s

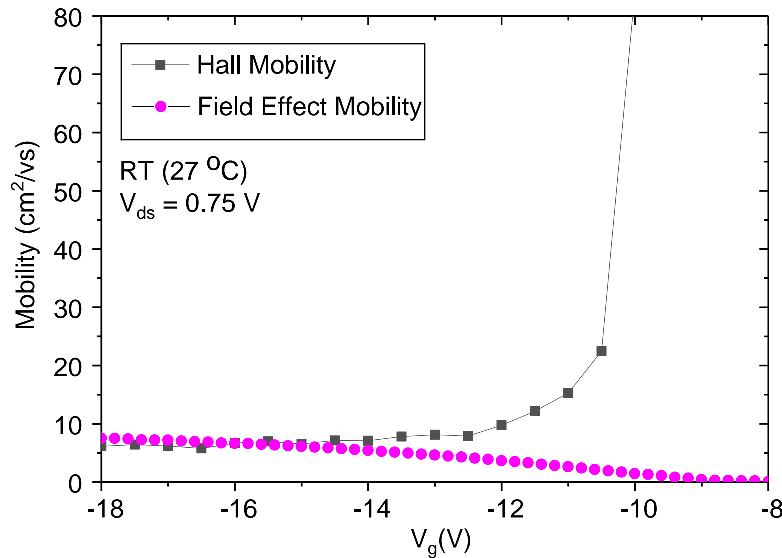

Figure 4.7: Field effect and Hall mobility for fabricated p-channel MOSFET

(2×10^{12} cm^{-2}), becomes temperature independent. Temperature-independent mobility can be explained by taking surface roughness scattering limited mobility into account. In this regime, the μ_{hall} closely matches with μ_{fe} as shown in Figure 4.7.

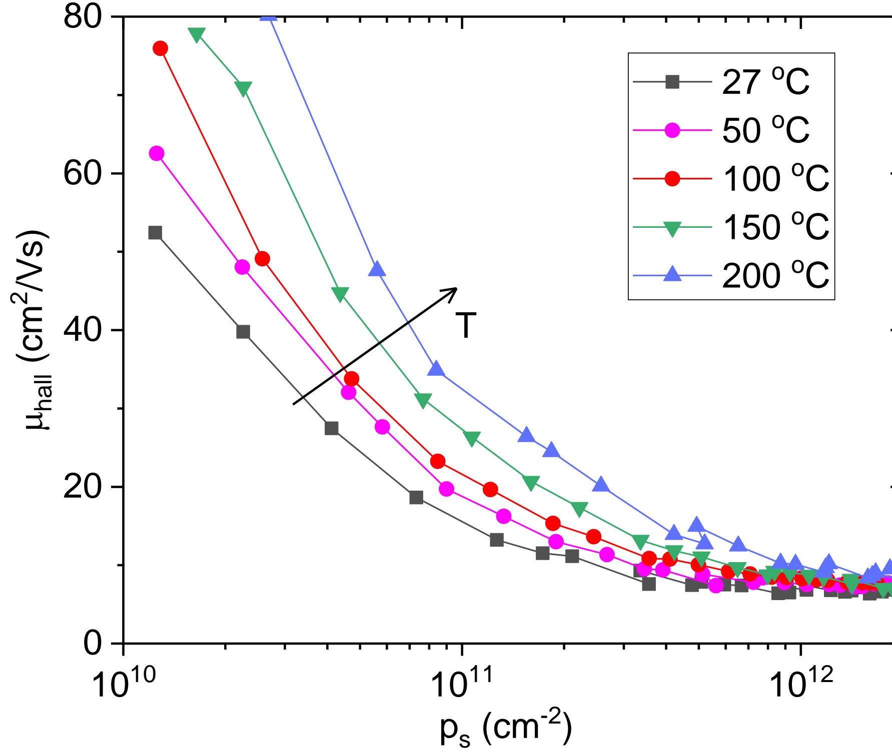

Figure 4.8: Hole mobility (μ_{hall}) in NO annealed 4H-SiC p-MOS Hall bars as a function of channel carrier concentration (p_s) at different temperatures ranging from 27 °C to 200 °C. Measurements were made with V_{ds} = 0.75 V and a perpendicular magnetic field of 0.6 T. Device channel length/width is 600 µm/60 µm.

In the measured temperature range no signature of phonon limited scattering, i.e., decreasing mobility with increasing temperature, was observed. This can be attributed to the moderate value of doping concentration (6×10^{15} cm^{-3}) of the n -base epi-layer. Earlier Hall measurements [25] on 4H-SiC n-channel MOSFET suggest that, at such doping concentrations, the phonon-limited electron mobility is not dominant. For low electron concentration, the mobility is coulomb

scattering limited, and as concentration increases surface roughness scattering dominates. Presumably, a similar mechanism is in place for holes as well, based on these results.

4.4.4. Hole trapping under negative bias and temperature stress

While NO annealing realizes high-temperature operation, the negative bias temperature instability could be a shortcoming. To study charge trapping under high temperature and gate voltage stress in NO annealed p-type capacitors, the following protocol was used. After

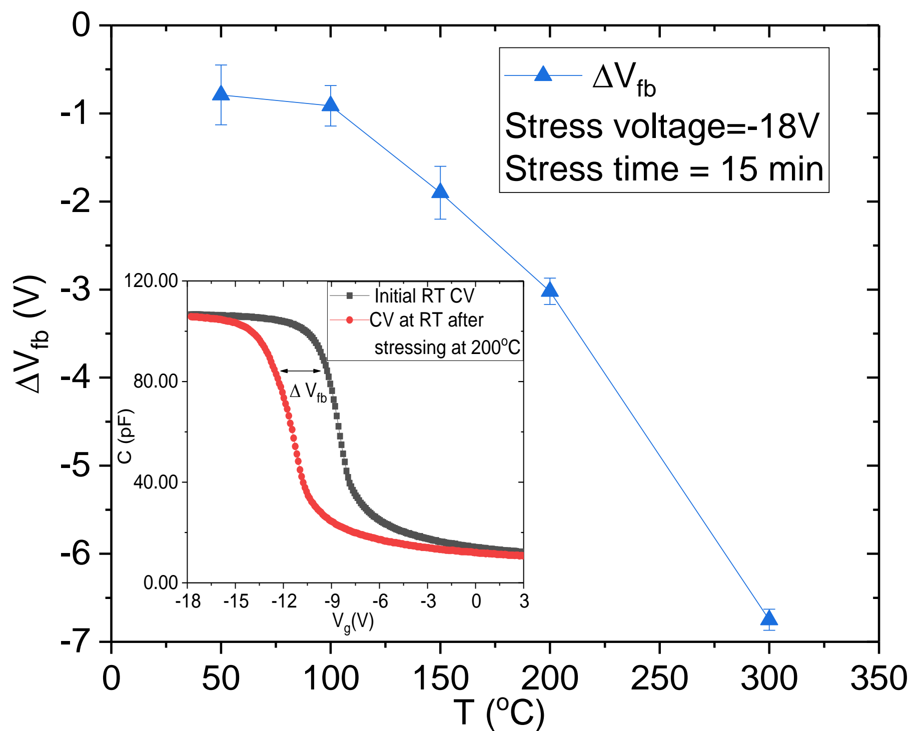

Figure 4.9: Change of flat band voltage ΔV_{fb} under constant negative bias stress in p-type NO annealed 4H-SiC MOS capacitors. A fixed negative bias -18 V is applied at the stress temperature and CV is measured at room temperature before and after the stress.

bidirectional room temperature CV sweeps, the devices were raised to the desired stress temperature and biased at -18 V (E_{ox} ~ 2 MV/cm using $E_{ox}= (V_g-V_{fb})/t_{ox}$) for 15 minutes. Subsequently, the capacitors were cooled to room temperature under bias and post-stress CV measurements were conducted to measure the flat band voltage shift (ΔV_{fb}) from the initial room

temperature sweep. With the increase in stress temperature, the V_{fb} becomes more negative as shown in Figure 4.8. This indicates positive charge/hole trapping in the near interfacial oxide under strong accumulation conditions.

Effective activation energy associated with the hole trapping of $0.21 \pm 0.01\ eV$ is obtained using an Arrhenius plot for ΔV_{fb} for the stress temperature range of 100 °C to 300 °C, as shown in Figure 4.9. This value matches closely that of a prior report on NO-annealed p-type MOS capacitors [26]. This temperature-activated hole trapping could be caused by nitrogen-related defects in the near-interfacial oxide [27]. Additionally, the capture of holes could also stem from

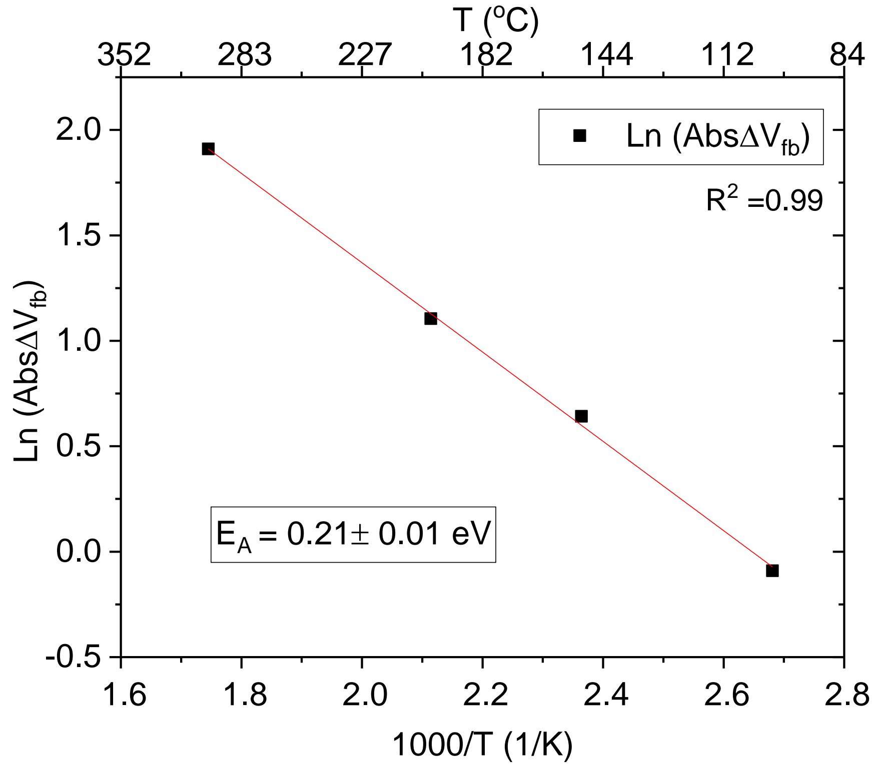

Figure 4.10: Arrhenius plot of average flat-band voltage shifts as a function of stress temperatures (lower axis: 1000/T, upper axis: T) in the 100 °C to 300 °C temperature range for NO annealed p-type 4H-SiC MOS capacitors. The capacitors are stressed at -18 V for 15 minutes at each temperature. Activation energy is calculated from the slope of the Arrhenius plot to be 0.21 eV for holes with a fitting error of 0.01 eV.

oxygen vacancies present at the 4H-SiC/SiO_2 interface transforming from a dimer to a puckered configuration [26].

The oxide hole trapping in capacitors under bias and temperature stress can be qualitatively correlated with hysteresis observed in the I_d-V_g of MOSFETs for bidirectional gate voltage sweeps at high temperatures. The direction of the hysteresis is consistent with hole trapping and the amount of hysteresis increases with temperature. This problem needs to be further mitigated, perhaps by using polysilicon gates and further D_{it} passivation.

4.5. Conclusions

In conclusion, nitridation of the 4H-SiC/SiO_2 interface realizes high temperature (300 °C) p-channel MOSFETs. Electrical characterization of MOS devices revealed that reduction of D_{it} in the lower half of the wide 4H-SiC bandgap by NO annealing enables enhancement mode operation. The hole field effect mobility in strong inversion is found to be weakly temperature dependent. Hall measurements confirm that a dominant surface roughness scattering is responsible for the weak temperature dependence. In weak inversion, transport is limited by hole trapping in interface traps and Coulomb scattering. At high temperatures, the total occupied D_{it} reduces and results in a smaller negative threshold voltage. Constant negative gate bias stress tests identify a temperature-activated oxide hole trapping mechanism that could be related to the interfacial nitrogen. The role of nitrogen and device instability at high temperatures requires further investigation.

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Chapter 5

Mobility limiting mechanisms in 4H-SiC MOSFETs using Hall Analysis

Part of this chapter is published in the special issue of the journal *Materials (2022)*

5.1. Abstract

The channel conduction in 4H-SiC MOSFETs is highly impacted by charge trapping as well as scattering at the interface. Even though nitridation reduces the interface trap density, scattering still plays a crucial role in increasing the channel resistance in these transistors. In this work, the dominant scattering mechanisms namely Coulomb, phonon, and surface roughness scattering are distinguished for inversion layer electrons and holes using temperature and body-bias dependent Hall measurements on nitrided n- and p-channel lateral 4H-SiC MOSFETs. Moreover, the effect of the transverse electric field (E_{eff}) on carrier mobility is analyzed under strong inversion conditions where surface roughness scattering becomes prevalent. The application of a body bias reveals a power law dependence of the electron and hole Hall mobility for surface roughness scattering to be $E_{eff}^{-1.8}$ and $E_{eff}^{-2.4}$ respectively analogous to that of silicon MOSFETs. For n-channel MOSFETs, phonon scattering dominates at zero body bias whereas in p-channel MOSFETs are observed only under negative body biases. Along with the identification of regimes governed by different scattering mechanisms, these results highlight the importance of the selection of substrate doping and of E_{eff} in controlling the value of channel mobility in 4H-SiC MOSFETs.

5.2. Introduction

Silicon carbide (4H-SiC) is one of the primary wide band gap semiconductors for high power and harsh environment applications because of its physical properties such as a high critical

electric field and high thermal conductivity [1]. Discrete 4H-SiC diodes and metal-oxide semiconductor-field-effect transistors (MOSFETs) are being widely adopted for high voltage power conversion in hybrid/electric vehicles [2], solar and wind energy generation [3], and various high-temperature applications [4], enabling significant advances for next-generation energy-efficient power systems. Moreover, 4H-SiC is a unique candidate for the development of an integrated circuit (IC) technology that is still in its infancy. 4H-SiC IC technology operating at very high temperatures >300 °C [5], [6] is very attractive as enables operation environments and ambiances that are not accessible to conventional silicon or silicon on insulator (SOI) platforms [7], [8]. A lateral complementary-metal-oxide-semiconductor (CMOS) IC technology in 4H-SiC is desirable for the fabrication of large-scale integration devices due to its high noise immunity and low static power consumption [9]. To materialize, such technology demands both n- and p-channel MOSFETs capable of operating at high temperatures. While n-channel MOSFETs have reached a suitable degree of maturity through the nitridation of the SiO_2/4H-SiC interface [10]–[12], mechanisms governing electrical transport in their p-channel counterparts must be investigated to reach comparable levels of development in terms of channel conductivity and device stability.

Recent studies [10], [13] on 4H-SiC MOSFETs use field-effect mobility models to analyze channel transport. Additionally, research by *Mikami et al.* [13] explores the importance of body bias and explains how body bias experiments can be a prediction of transistor characteristics for MOSFETs made on higher or lower substrate doping using field-effect mobility on the weak inversion region. However, the channel scattering mechanisms for p-channel 4H-SiC MOSFET remain unexplored using Hall analysis. Hall mobility is more accurate than field effect mobility as the carrier concentration is measured independently and does not get affected by trapped charges.

A comprehensive study for both kinds of carriers will enable control of the operation region and the preferable substrate doping concentrations for high temperature IC design. To this end, the channel mobility of nitric oxide (NO) annealed n- and p-channel 4H-SiC MOSFETs in the strong inversion regime is characterized using Hall measurements. Measurements are performed using body bias technique which allows variation of the effective electric field (E_{eff}) in the channel [13], [14]. This approach allows for differentiating and establishing the dominant scattering mechanisms limiting carrier transport, in different carrier density and substrate doping regimes. The power law that governs the relationship between μ_{Hall} and E_{eff} is determined for both electrons and holes in the surface roughness scattering dominant regime. In addition, it is demonstrated that combination of temperature and body bias enables observation of the dominant mechanisms transitioning from surface roughness to phonon scattering.

5.3. Fundamentals on channel transverse electric field and mobility

The channel resistance depends on the channel inversion carrier concentration and its mobility (μ_{Hall}) which are related to the atomic-scale composition, structure, and defects at the SiO_2/4H-SiC interface. The mobile carrier concentration is reduced by traps at electrically active defect sites while the channel mobility is degraded by interfacial scattering processes. When the FET is on, the dominant scattering mechanisms at a SiO_2/4H-SiC interface that limits μ_{Hall} are (i) Coulomb scattering occurring due to trapped charges present at or near the interface oxide as well as from ionized impurities in the depletion region close to the channel; (ii) phonon scattering occurring due to the interaction of the carriers with lattice vibration in the channel and the surface; and (iii) surface roughness due to imperfections of the 4H-SiC interface [15]–[17]. The resulting carrier mobility is given by Matthiesen's rule [18],

$$\frac{1}{\mu_{Hall}} = \frac{1}{\mu_C} + \frac{1}{\mu_{ph}} + \frac{1}{\mu_{SR}} \tag{5.1}$$

Here, μ_C, μ_{ph}, and μ_{SR} are the Coulomb, phonon, and surface roughness scattering limited mobilities, respectively.

On Si MOSFETs [19], [20] earlier studies suggest that the transverse electric field E_{eff} is an important parameter in influencing scattering in the channel. The magnitude of E_{eff} can be obtained as [19],

$$E_{eff} = \frac{1}{\epsilon}\left(\sqrt{2N_A e\epsilon.(2\phi_B \pm V_{BS})} + \eta q n_s\right) \tag{5.2}$$

The first term in Equation (5.2) represents the amount of depletion space charge, and the second term stands for the induced inversion layer charge excluding trapped charges. Here the '+' sign is applicable for n-channel and the '−' sign is for p-channel MOSFETs, respectively. A schematic diagram of these two charge distributions is shown in the left panel of Figure 5.1. In Equation (5.2), η is a constant with a value of 0.5 for n-channel and 0.33 for p-channel Si MOSFETs at

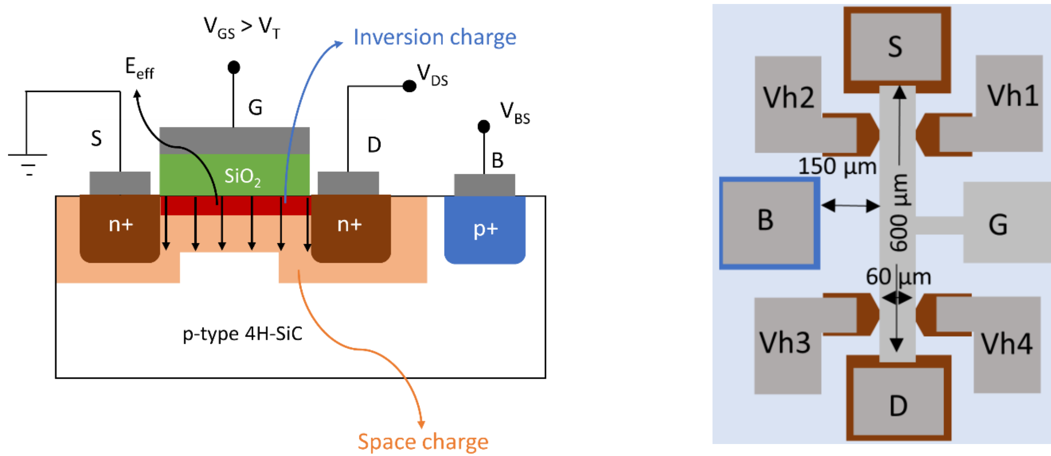

Figure 5.1: (left) Schematic diagram of lateral n-channel Hall MOSFET with the transverse electric field E_eff shown, which depends on space charge and inversion charge in the channel at a gate voltage higher than the threshold voltage. (right) Top view of a schematic of the fabricated Hall bar MOSFET. Vh1, Vh2, Vh3, and Vh4 represent the Hall voltage terminals.

$27\ ^{o}\mathrm{C}$ [20], [21] that is considered same for 4H-SiC. ϵ is the dielectric constant, e is the electron charge, n_s is the free carrier concentration, and N_A is the p-well substrate doping concentration for n-channel MOSFETs. V_{BS} is the substrate or body-to-source bias. $\phi_B = \frac{KT}{q} \ln \frac{N_A}{n_i}$ is the bulk potential. K is the Boltzmann constant and n_i denotes the temperature dependent intrinsic carrier concentration. Note, for p-channel MOSFET the n-well substrate doping concentration is denoted by N_D.

5.4. Experimental Methods

Hall bar MOSFETs with a channel length of 600 µm and channel width of 60 µm were fabricated on a 4° off-axis (0001) Si-face oriented 4H-SiC substrate having a p-type epilayer (N_A-N_D=6×10^{15} cm^{-3}) for n-channel, and n-type epilayer (N_D-N_A=6.2×10^{15} cm^{-3}) for p-channel MOSFET respectively. Additional to the Hall bar MOSFETs, T gated MOSFETs were also present in the chip with a 200 µm × 200 µm channel (width, length). The cross-sectional schematic of the Hall bar device is shown in Figure 5.1 (left). A nominally uniform doping profile was created using nitrogen and aluminum ion implantations at 700 °C to form n+ and p+ layers on the MOSFETs respectively to form source, drain, and body contacts. The implanted layers were then activated by annealing at 1650 °C for 30 min in flowing Ar with a graphitic cap to protect the surface. After removal of the cap, gate oxidation was carried out at 1150 °C for 10 h followed by post oxidation annealing at 1175 °C for 2 h in NO. The thickness of the gate oxide was measured to be about ~ 60 nm and 55 nm by capacitance-voltage method (CV) for n- and p-channel MOSFETs respectively. Contact photolithography and reactive ion etching were carried out to remove the oxide from the source/drain/body (S/D/B) regions and Hall voltage (V_h) terminals. For n-channel MOSFET, Al was evaporated for all the contacts and annealed at 800 °C for 30 minutes in flowing Ar. On the other hand, for p-channel MOSFET, Ti was sputtered and lifted off to define

the S/D/B/V_h contacts as shown in Figure 5.1 (right), following which annealing at 1000 °C for 2 min was performed in flowing Ar to form ohmic contacts. Subsequently, aluminum (55 nm) was thermally evaporated as the gate metal and patterned using lift-off. An overlayer of Au/Cr was sputtered on all the contacts of both kinds of MOSFETs. Finally, the Hall bar MOSFET was mounted on a ceramic chip with epoxy and wire bonded to gold pads on the chip.

5.5. Results and discussions

5.5.1. Classification of the dominant scattering mechanisms

After fabrication of the 4H-SiC MOSFETs, transfer characteristics were obtained at various temperatures. Temperature for the n-channel MOSFET is varied from 77 K to 373 K. For the p-channel MOSFET on the other hand the temperature is raised above room temperature (300 K) and went to 573 K. The absolute value of threshold voltage becomes smaller at higher temperatures as shown in Figure 5.2. This is associated with the reduction of occupied interface trap densities (D_{it}) at higher temperatures [22].

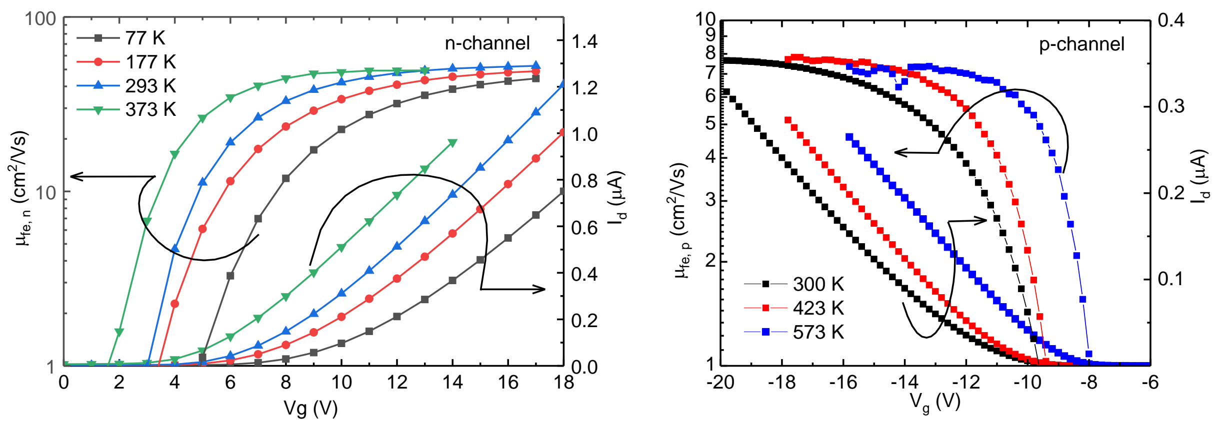

Figure 5.2: Field effect mobility of electrons and holes versus gate voltage at different temperatures for n- (left) and p-channel (right) 4H-SiC MOSFETs. For n-channel MOSFETs channel width/length is 60 µm/600 µm, oxide thickness is 60 nm, V_{ds} is set to 0.4 V and temperature is varied from 77 K to 373 K. For p-channel MOSFET channel width/length is 200 µm/200 µm, oxide thickness is 55 nm, V_{ds} is set to 0.1 V and temperature is varied from 300 K to 573 K.

In addition, the field effect mobility of electrons ($\mu_{fe,n}$) is observed to increase from 77 K to 296 K at high gate bias. Whereas, for p-channel MOSFET, the field effect mobility of holes is observed to be constant at varying temperatures. To confirm the dominant scattering mechanisms in these devices, Hall measurements were carried out under a perpendicular magnetic field of strength of 0.6 T. Figure 5.3 shows μ_{Hall} versus carrier concentration curves at different temperatures and at zero body bias for electrons and holes in n- and p-channel 4H-SiC MOSFETs. To obtain μ_{Hall} versus carrier concentration plot, the gate to source voltage V_{GS} is varied from +2 to +10 V for n-channel and -6 V to -20 V for p-channel MOSFETs at the constant drain to source voltage $V_{DS} =$ 0.75 V.

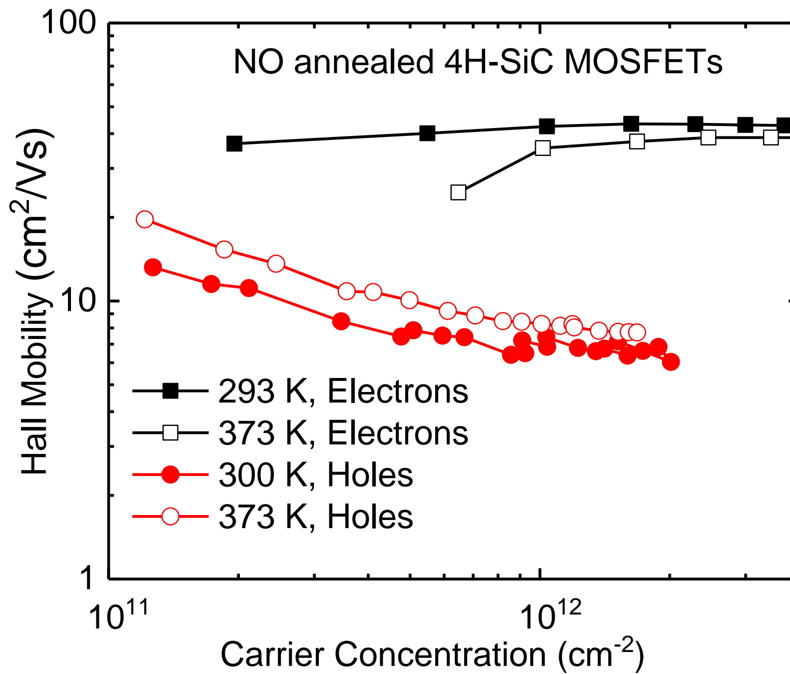

Figure 5.3: Hall mobility as a function of carrier concentration at different temperatures for n- and p-channel MOSFETs with channel width 60 µm and channel length 600 µm for both kinds of Hall bar MOSFETs, and V_{ds} is set to 0.75 V.

The threshold voltage is found to be +3 V electrons (at 293 K) and -8 V for holes (300 K), based on linear extrapolation of the I_D-V_G characteristics (Figure 5.2). For n-channel MOSFET, Hall

mobility above room temperature drops. An increase in mobility from 77 K to 293 K is a signature of prevalent Coulomb scattering whereas above 296 K mobility decreases with increasing temperature when phonon scattering is dominant. Therefore, electron transport is limited by Coulomb and phonon scattering. A presence of surface roughness scattering at higher concentrations can also be observed in earlier reports [14]. Conversely, for holes in p-channel MOSFET, Hall mobility is seen to increase at lower carrier concentration (for approximately $p_s < 6 \times 10^{11}\ cm^{-2}$ at 300 K) signifying dominant Coulomb scattering and becomes independent of temperature at approximately $p_s = \ 10^{12}\ cm^{-2}$ as shown in Figure 5.4. Temperature-independent mobility is a sign of surface roughness scattering. Therefore, hole mobility in 4H-SiC p-channel MOSFET is limited by Coulomb scattering at weak inversion and dominant surface roughness scattering at strong inversion.

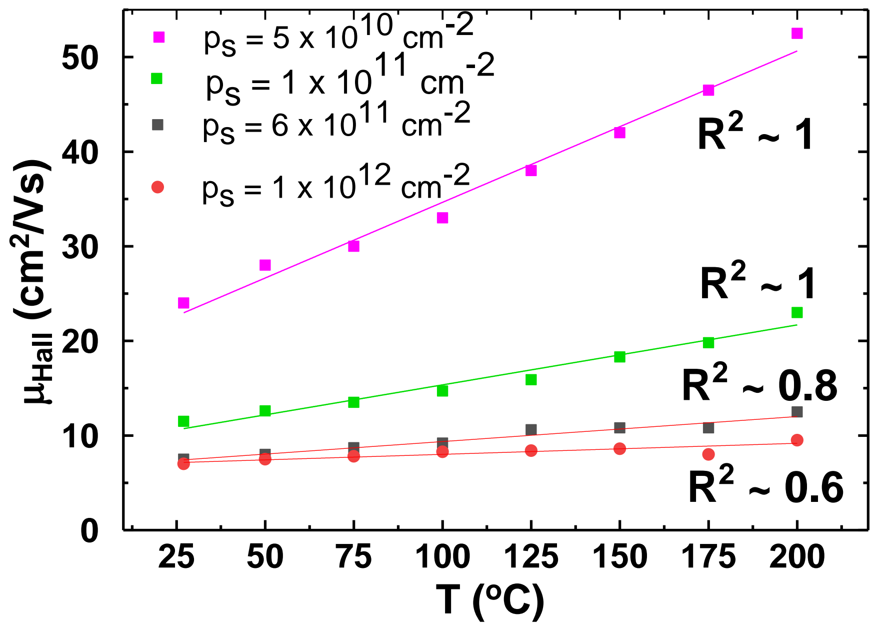

Figure 5.4: Temperature dependence of the Hall mobility for p-channel MOSFET at different carrier concentrations. At $p_s = 1x12\ cm^{-2}$, the fitting parameter R^2 can be seen to deviate from 1, showing a surface roughness scattering regime.

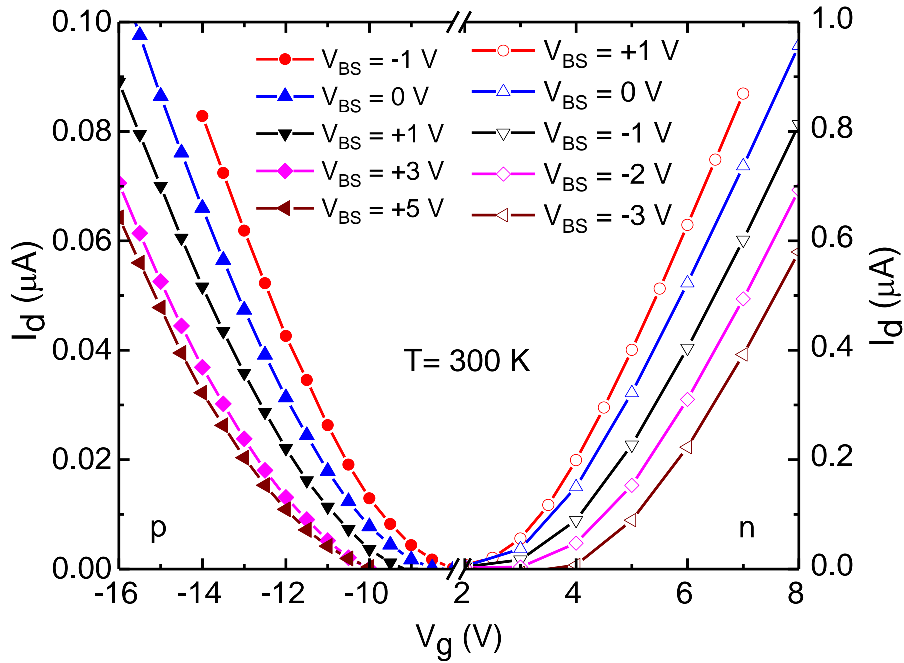

Figure 5.5: Transfer characteristics at room temperature (300 K) for different body biases (V_{BS}) for n- and p-channel MOSFETs. Id -Vg sweeps are taken at a constant drain to source (0.75 V) voltage. A change in V_{th} can be observed due to the modulation of the depletion layer width at the body to source junction with the application of body bias. Note that the y-axis scales are different for two kinds of MOSFETs.

After distinguishing the dominant scattering mechanisms in these devices, Hall measurements were carried out under the effect of body bias (V_{BS}) so that the Hall mobility (μ_{Hall}) can be studied as a function of transverse electric field (E_{eff}) in the strong inversion regime. Recent research [13], [14] observed the effect of transverse electric field on mobility in the strong inversion regime maintaining a fixed carrier concentration. A constant carrier concentration realizes fixed screening from scattering centers and enables the assessment of the sole effect of surface roughness scattering on mobility.

5.6. Analysis of surface roughness scattering using body bias measurements

The plot of μ_{Hall} as a function of carrier concentration in the strong inversion region for different body biases is shown in Figure *5.6*. An increase in reverse body bias increases the magnitude of the transverse electric field (Equation 5.2) and pushes the carriers closer to the surface making the

channel width thinner (~1 nm) at strong inversion. Hence, at high gate voltage, when mobile holes are closer to the surface, surface roughness scattering becomes even more prevalent through the influence of the varying perturbed potential energy [15].

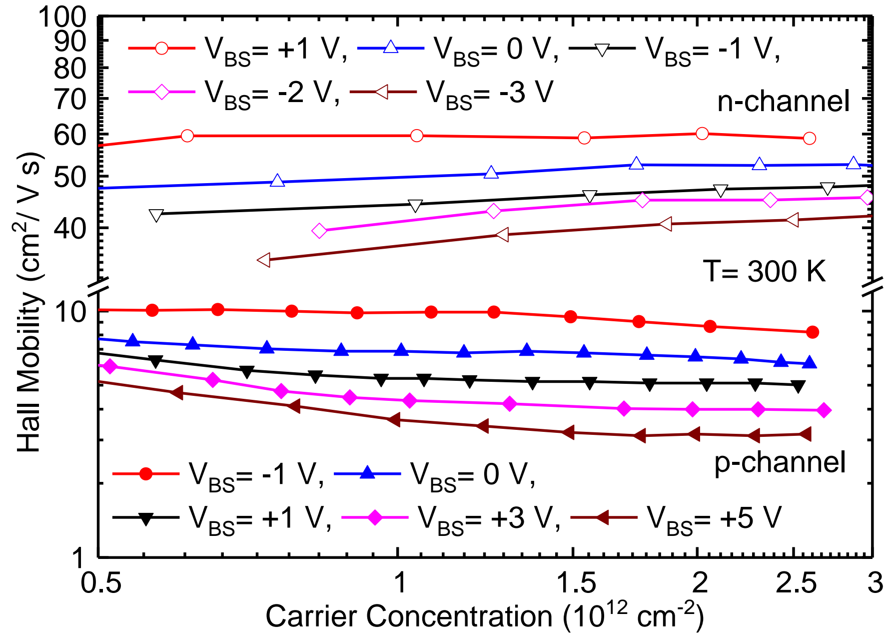

Figure 5.6: Hall mobility as a function of channel carrier concentration at different body biases at 27 °C. The body bias is varied from +1 to -3 V for n-channel and -1 to +5 V; the gate bias V_{GS} is swept to modulate the carrier concentrations under a fixed body bias. A forward body bias value decreases the depletion layer width between source and body, increasing mobility and at reverse body bias, E_{eff} increases due to expansion of the depletion layer which in turn decreases the channel mobility.

This is attributed to charge carrier wave functions becoming more susceptible to the fluctuating perturbation near the interface stemming from the crystal miscut (4° off-axis substrate) and nano-steps/roughness. As a result, an increased E_{eff} lowers the value of μ_{Hall}. Conversely, a negative body bias decreases the value of E_{eff}, which widens the channel region and lessens the impact of the surface roughness scattering.

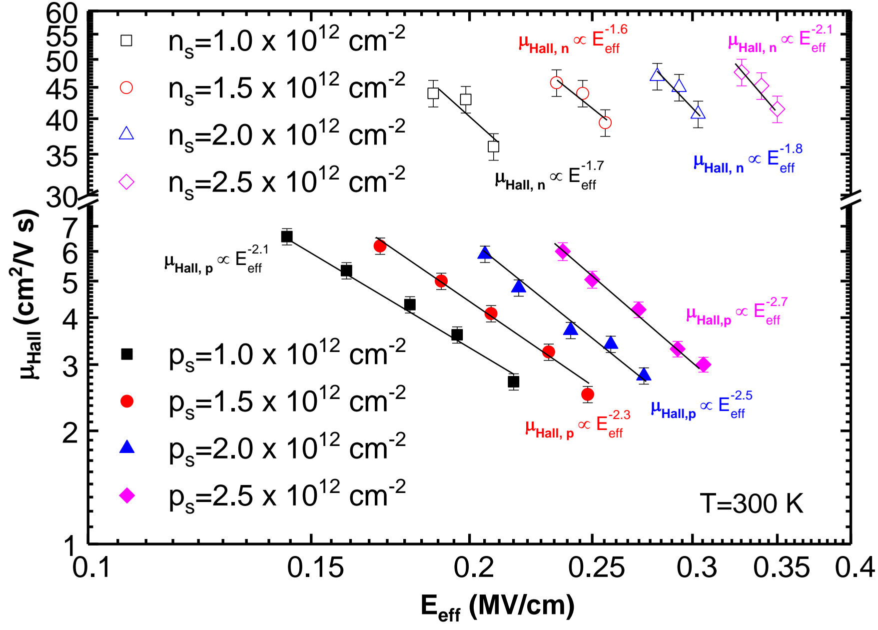

Figure 5.7: Transverse electric field (E_{eff}) dependence of Hall mobility (μ_{Hall}) at different body biases (-1, -2, and -3 V for n -channel and 0, +1, +3, +5, and +7 V for p -channel) at room temperature (27 °C) for different carrier concentrations ($1.0 \times 10^{12}, 1.5 \times 10^{12}, 2.0 \times 10^{12}$, and 2.5×10^{12} cm^{-2}), in log–log scale. The different E_{eff} points for a particular curve were obtained from different body biases at a fixed carrier concentration from Figure 5.6. The average power law that μ_{Hall} follows on E_{eff} is (-1.8 ± 0.2) for n -channel MOSFETs and (-2.4 ± 0.3) for p -channel MOSFETs, providing the power of E_{eff} for surface roughness scattering for electrons and holes in 4H-SiC MOSFETs. Error bars signify ~5% error estimated based on variation in at least 3 measurements.

These results were used to extract the functional dependence of μ_{Hall} at a fixed carrier concentration to analyze surface roughness scattering under *constant screening*. For this purpose, using Equation (5.2), n_s *and* p_s are converted to E_{eff} for each V_{BS} above 0 V in the strong inversion regime. Next, μ_{Hall} is extracted at fixed carrier concentrations ($1.0 \times 10^{12}, 1.5 \times 10^{12}$, and 2.0×10^{12} cm^{-2}) and plotted against E_{eff} as shown in Figure 5.7. The curves have been fit using a power law function of E_{eff}, yielding an exponent of (-1.8 ± 0.2) and (-2.4 ± 0.3) for channel electrons and holes in 4H-SiC n- and p-channel MOSFETs respectively. These values are close to those found earlier for surface roughness scattering in Si MOSFETs [20], suggesting

that at high E_{eff}, surface imperfections have a similar effect on channel carriers in 4H-SiC as in Si MOSFETs. However, different from Si where μ_{Hall} versus E_{eff} curves merge with each other when surface roughness scattering becomes dominant regime, this universal behavior is not visible for 4H-SiC in Figure 5.7. This is consistent with earlier researches on 4H-SiC n-channel MOSFETs [14], [23], [24]. Perhaps for a single 4H-SiC MOSFET, the measurable range of E_{eff} is not large enough before the breakdown of gate dielectric to observe the merging of μ_{Hall} at higher E_{eff} and a larger range of measurements using devices with different substrate doping is necessary as reported in [24].

5.6.1. Phonon scattering limited mobility

For n-channel MOSFET, dropping mobility is observed above room temperature at zero body bias which signifies the dominance of phonon scattering limited mobility as seen in Figure *5.9*. This fact is consistent with recent work [23] which reported that phonon scattering limited mobility can be observed for n-channel MOSFETs fabricated on lightly doped ($\lesssim 5 \times 10^{15}$ cm^{-3}) p-type epitaxial layers. However, for p-channel MOSFET phonon scattering, limited mobility is absent at zero body bias at the measured temperature range. In this case, phonon scattering is visible only when the source to body junction is kept at a forward bias ($V_{BS} < 0$). Here the power law-dependence of the μ_{Hall} on E_{eff} is observed to give an exponent of -0.32 as shown in Figure 5.8. A power law of $E_{eff}^{-1/3}$ is an indication of phonon scattering [20], [23].

In our study, a negative body bias is used to replicate a lightly doped n-type substrate through the 'effective doping concentration' [14] of the n-well $N_{D,eff}$, given by:

$$N_{D,eff} = N_D(1 + \frac{V_{BS}}{2\phi_B}). \tag{5.3}$$

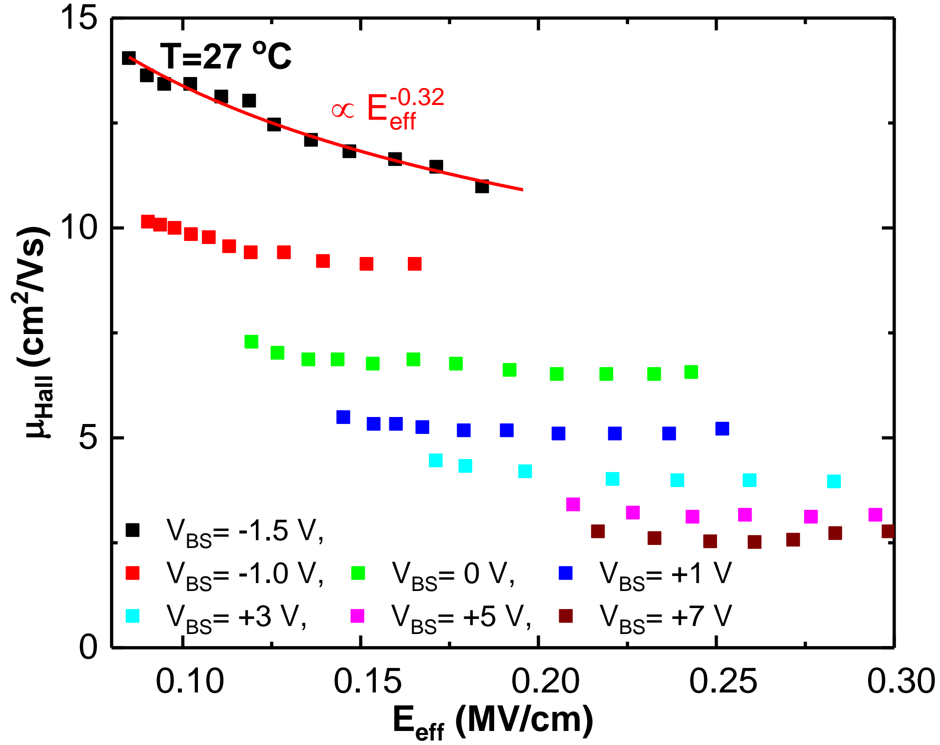

Figure 5.8: Hole mobility versus transverse electric field for different body biases at room temperature. The curve for V_{BS} =-1.5 V shows a dependence of $E_{eff}^{-1/3}$ which is an indication of phonon scattering.

At a body bias $V_{BS} = -1.3\,V$ and a fixed $p_s = 10^{12}$cm^{-2}, a low value of $N_{D,eff}$ (approximately 3×10^{15} cm^{-3}) can be maintained in the 300 to 498 K (27 °C to 225 °C) temperature range. Figure 5.9 shows that μ_{Hall} increases from room temperature to 398 K due to Coulomb scattering, after which it decreases owing to the dominance of phonon scattering following a power law of $T^{-0.9}$. Under negative V_{BS}, the channel is thick enough to interact with the n-well lattice vibrations at T > 398 K, and the hole mobility is limited by phonon scattering. This is consistent with n-channel 4H-SiC MOSFETs fabricated on lightly doped substrates where a phonon scattering limited mobility at low E_{eff} or $N_{D,eff}$ is observed [23]. Conversely for $V_{BS} = 0$ V, channel thickness is comparatively thinner than at $V_{BS} = -1.3\,V$. In this case no phonon limited scattering is

observable, but μ_{Hall} is limited by the cumulative effect of Coulomb and surface roughness scattering. As a result, μ_{Hall} increases slightly at higher temperatures.

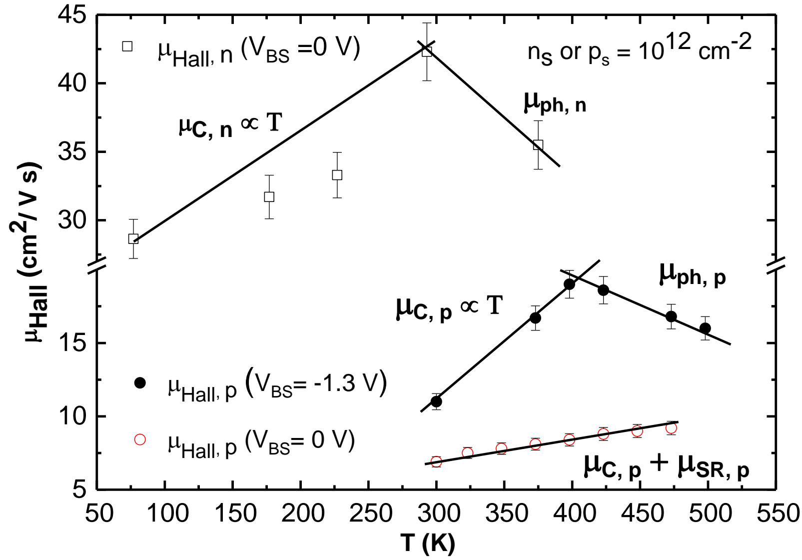

Figure 5.9: Hall mobility (μ_{Hall}) versus temperature T for different body biases is plotted for a fixed n_s /or $p_s = 10^{12}$cm^{-2}. For n-channel MOSFET, Coulomb scattering is dominant below RT, above it, phonon scattering is observed at zero body bias. However, for p-channel MOSFETs μ_{Hall} is limited by a combined effect of Coulomb and surface roughness scattering V_{BS}= 0 V. For V_{BS}= -1.3 V, μ_{Hall} increases linearly until 398 K (125 °C) due to Coulomb scattering. At higher temperatures, phonon scattering dominates and μ_{Hall} decreases with temperature as $T^{-0.9}$.

5.7. Summary

In conclusion, the dominant scattering mechanisms in n- and p- 4H-SiC MOSFET channels are distinguished using Hall measurements. Electron mobility in n-channel MOSFET is limited by Coulomb scattering in weak inversion and a combination of phonon and surface roughness scattering in the strong inversion region. On the other hand, hole mobility in p-channel MOSFET is limited primarily by Coulomb and surface roughness scattering. Body bias and temperature-dependent Hall measurements are performed and analyzed under strong inversion to study mobility in terms of effective transverse electric field (E_{eff}). As body bias is increased, a higher value of E_{eff} confines the mobile carriers near the 4H-SiC/SiO_2 interface resulting in a surface

roughness scattering limited mobility. A changing body bias is applied to determine the power law dependence of channel electron and hole mobility on the E_{eff} for surface roughness scattering in 4H-SiC as $E_{eff}^{-1.8}$ and $E_{eff}^{-2.4}$ respectively. Furthermore, with the application of negative V_{BS}, the depletion layer between the source and body contact decreases, and the resulting low E_{eff} leads to higher mobility at a given gate bias. For p-channel MOSFET, at a forward V_{BS} (-1.3 V at 398 K), the channel is thick enough to interact with the n-well lattice vibration, giving rise to a phonon scattering limited hole mobility. Therefore, at low negative V_{BS}, the channel conduction behaves like a MOSFET with a lightly doped substrate. These new findings emphasize the significance of substrate doping selection for 4H-SiC MOSFETs. Additionally, for the development of highly efficient 4H-SiC CMOS devices for high-temperature operation, the three types of scattering processes identified here must be considered depending on the value of the transverse electric field in the channel and the operating temperature.

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Chapter 6

Nitrogen annealing as a sustainable method for interface trap passivation in 4H-SiC MOSFETs

Part of this chapter is an under-preparation manuscript and will be submitted soon

6.1. Abstract

In search of a sustainable annealing treatment to passivate interface traps (D_{it}) in n- and p-type 4H-SiC, high temperature (1400 °C-1500 °C) N_2 post oxidation annealing is employed. With the potential to replace hazardous and expensive NO, N_2 post oxidation annealing reduces Dit in both the upper and lower halves of the 4H-SiC band gap, with a greater impact at the valence band edge. Among several conditions, 1500 °C N_2 annealing is observed to be more effective in passivating traps and positive fixed charges than NO annealing for p-type devices. D_{it} is measured as a function of the nitrogen areal densities in the near interfacial regions for the different processes. The breakdown voltages for these devices are found to be comparable to that of NO annealed samples. D_{it} versus nitrogen concentration at the interface measured by X-ray photoelectron spectroscopy is analyzed. Furthermore, theoretical analysis through density functional theory (DFT) calculations provides insights into the role of nitrogen near the SiO2/SiC interface.

6.2. Introduction

Silicon Carbide (4H-SiC) has emerged as a leading wide band gap semiconductor for high-power, high-temperature applications [1]. 4H-SiC metal-oxide semiconductor-field-effect transistors (MOSFETs) have much lower power dissipation compared to silicon, allowing for low-noise and high-efficiency all-electric vehicle drives, fast-charging stations, solar inverters, and much more. While these devices provide substantial advancements for next-generation energy-

efficient power systems, 4H-SiC also provides additional functionality in the form of integrated circuits (ICs) at high temperatures (>300 °C). Because of its high noise immunity and low static power consumption, lateral complementary-metal-oxide-semiconductor (CMOS) IC technology in 4H-SiC is widely desirable for large-scale integration [2]. This technology necessitates the use of both n- and p-channel MOSFETs that can operate at high temperatures. Despite the substantial advance of 4H-SiC MOSFETs, the high density of interface states (D_{it}) at the 4H-SiC/SiO_2 interface prevents reaching full potential by resulting in high channel resistance and low mobility.

Extensive gate passivation research has been conducted over the last decade to reduce D_{it} in 4H-SiC [3]–[12]. Some passivation methods such as wet oxidations [13] were only helpful in reducing traps near the valence band edge (E_V), but not so efficient in lowering traps near the conduction band edge (E_C). Out of all passivation methods, post oxidation annealing in nitric oxide (NO) at high temperature turned out to be the most successful and the standard process for reducing D_{it} both near E_C and E_V [12], [14]. However, it is impossible to ignore the negative effects of NO annealing on the economy and the environment. Furthermore, NO is known to cause threshold voltage instability [15] and create oxide hole trapping [6] in 4H-SiC MOSFETs. To find alternative solutions for toxic and expensive NO, some earlier research [5], and more recently *Tachiki and Kimoto* [16], demonstrated that high temperature (1400 °C-1600 °C) annealing in flowing nitrogen gas produces promising results for 4H-SiC MOSFET processing.

In this work, post oxidation annealing at high temperatures (1400 °C-1500 °C) in flowing N_2 gas is conducted to study trap characteristics at 4H-SiC/SiO_2 interface. The values of D_{it} obtained here from MOS capacitors are consistent with [16] and attempt to correlate the nitrogen areal densities of the near interfacial regions with the D_{it} for high-temperature N_2 annealing compared to NO. Nitrogen annealing is found to be more effective in reducing D_{it} near the valence

band than NO annealing, while the opposite is true close to the conduction band-edge. It also decreases the positive fixed charges at the interface of p-type 4H-SiC and SiO_2, as evidenced by the flat band voltage comparison between processes. This work tries to answer the reason for the N_2 annealing to be effective for p-type, however not so viable for n-type capacitors. The oxide breakdown voltages for the devices made with 1500 °C N_2 annealing, were similar to that of NO annealed devices. To find the areal density of N_2 at the interface, X-ray photoelectron spectroscopy (XPS) is performed. Additionally, for the theoretical perspective of the nitrided interface, DFT calculation is carried out.

6.3. Experiments and Methods

In this work, metal-oxide-semiconductor (MOS) capacitors were fabricated on p-type (N_A-N_D= 6.2×10^{15} cm^{-3}) and n-type (N_D-N_A= 2.0×10^{16} cm^{-3}) epitaxial layers on a 4° off-axis (0001) Si-face oriented substrate. All samples were oxidized at 1150 °C and some samples were subjected to post oxidation annealing (POA) for comparative studies of D_{it}. The thicknesses of the gate oxides for the n- and p-type capacitors were found to be ~ 55 nm and ~ 65 nm respectively, by the capacitance-voltage (CV) method. The various samples are labeled according to the process as follows. 'As-Ox' represents a sample without any POA. The samples called 'NO_2' is annealed in nitric oxide (NO) at 1175 °C for 2 h with a flow rate of 500 sccm. Selected oxidized samples are annealed in flowing N_2 at high temperatures (1400 °C, 1 hour; 1450 °C, 1 hour; and 1500 °C, 30 minutes or 1 hour) at a flow rate of 3000 sccm. After POA, ~ 50 nm thick Aluminum (Al) was evaporated on top of the samples to form gate metal on all the capacitors. Simultaneous high frequency (100 kHz)- low-frequency CV (HI-LO CV) measurement was performed to extract interface trap densities (D_{it}) for each process and compared at room temperature (27 °C) with reference to 1175 °C, 2 h NO annealing.

XPS measurements were conducted using a monochromatic Al Kα X-ray source (K-Alpha, Thermo Scientific Inc.) with a flood gun for charge compensation. To prepare the samples for measurements, the SiO_2 dielectric layer was removed using buffered oxide etchant (BOE) etchant 6:1 (6 parts by volume of 40% ammonium fluoride and 1 part by volume of 49% hydrofluoric acid, Sigma-Aldrich). Calibration was done against the C1s spectra from 4H-SiC (283.4 eV). During the measurements, X-rays with a spot size of 200 μm were focused on each sample and the normal direction of the sample surfaces was pointed to the analyzer.

6.4. Results and Discussion

6.4.1. MOS capacitor measurements

To characterize electrically, high frequency (100 kHz) CV curves are obtained for capacitors made using different methods. Figure 6.1 shows the same for n- and p-type capacitors under different N_2 annealing conditions, compared with 'As-ox' and 'NO_2'. For p-type capacitors, the CV curves clearly move to the right with the increase of N_2 annealing temperature, reducing the flat band voltage due to the passivation of deep interface states and fixed charges. For 1500 °C annealing the flat band voltage for p-type becomes less than NO annealing, which is definitely advantageous. On the other hand, with the increase in annealing temperature, CV curves in n-type devices move slightly left and the 1500 °C process yields a similar flat band as NO.

Next, from simultaneous Hi-Lo CV, shallow D_{it} profiles were extracted for states near the valence (E_v) and conduction band (E_C) edges as shown in Figure 6.2. For p-type capacitors, a consecutive reduction of D_{it} is visible with the increase of N_2 annealing temperature, consistent with the decrease of V_{fb}. Among all the processes, 1500 °C, 30 min N_2 yielded the minimum D_{it} close to Ev. A lower D_{it} using N_2 annealing could be a combined effect of higher temperature and less nitrogen concentration at the p-type interface. However, for n-type capacitors, D_{it} near Ec

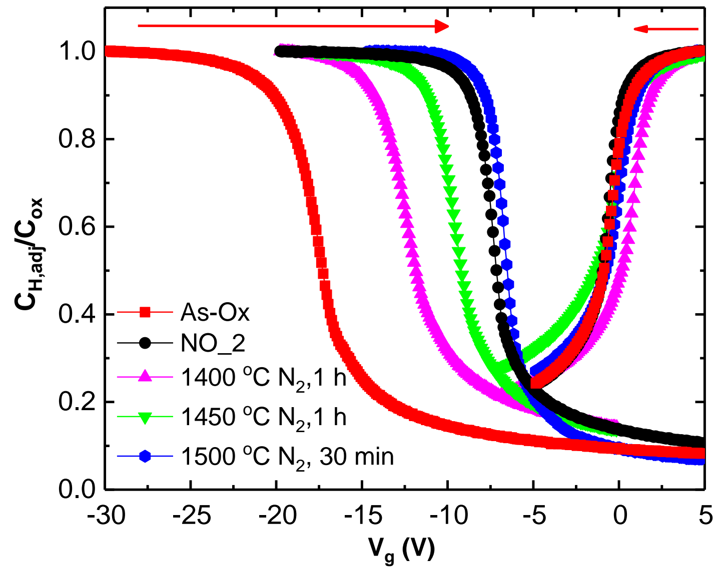

Figure 6.1. High frequency CV curves for p- and n-type MOS capacitors for different processes. Interface state passivation and fixed charge reduction is associated with N_2 annealing for both p- and n-type capacitors, lowering the flat band voltages as a result. The oxide thickness ranges from ~ 65-70 nm and for p-type 4H-SiC and ~ 55-60 nm and for n type 4H-SiC. The capacitors have circular shape with a diameter of 500 µm.

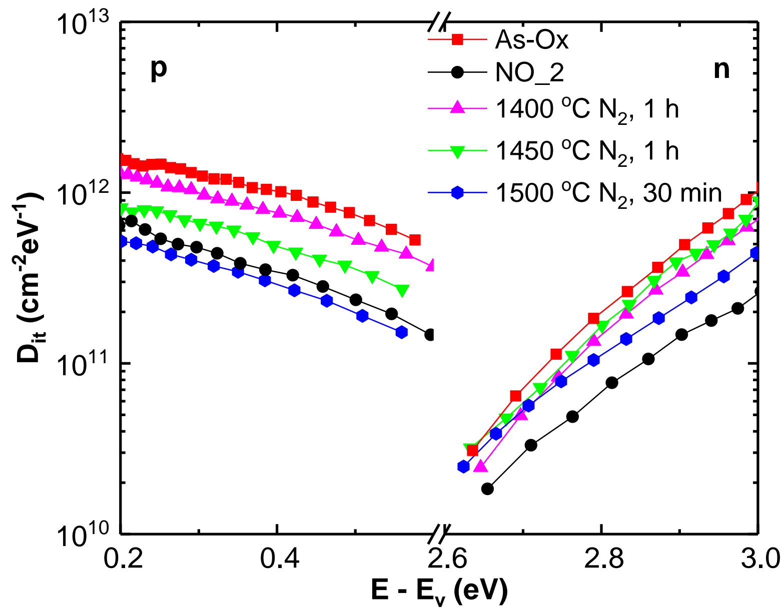

Figure 6.2. Shallow D_{it} profiles of p and n-type MOS capacitors extracted from simultaneous high frequency (100 kHz)-low-frequency CV measurements. As-Ox represents oxidation at 1150 °C without any POA, NO_2 represents oxidation at 1150 °C, and POA at 1175 °C NO for 2 h. 1500 °C, 30 min N_2 POA passivates more traps near the valence band edge (E_V) than NO annealed devices. The opposite is true near the conduction band edge (E_C).

was lower for NO annealing compared to N_2, consistent with [16]. To find the breakdown voltage of the capacitors fabricated with 1500 °C, 30 min N_2 annealing, current-voltage (I-V) characteristics were obtained and compared with the 2 h NO annealed samples as shown in Figure 6.3. Both for n- and p-type capacitors the breakdown voltage was found to be slightly lower than the NO annealed samples. The slightly lower breakdown and sharpness in the N_2 curves might be due to the annealing at a higher temperature compared to NO annealing.

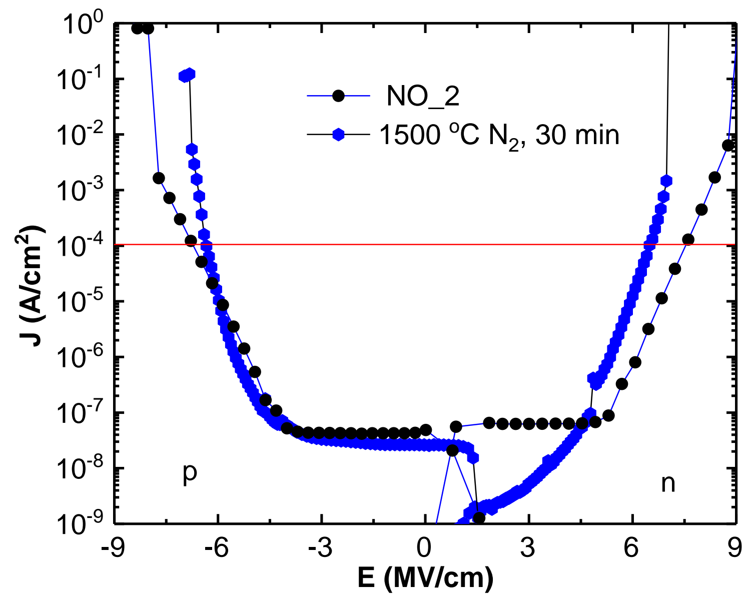

Figure 6.3. Current density (J)- Electric Field (E) characteristics of the devices made with 1500 °C, 30 min N_2 POA and compared to 1175 °C, 2 h NO annealed devices. The horizontal red line denotes the breakdown current. Both p- and n-type capacitors have a comparable breakdown field with NO annealed devices. The thickness for p-types capacitors is ranging from ~ 65-70 nm and that for n-types is ~ 55-60 nm and with a circular gate diameter of 500 µm.

6.4.2. XPS analysis

To understand the surface chemistry of the high-temperature N_2 annealed samples, X-ray photoelectron spectroscopy (XPS) was performed and compared with NO annealed samples in collaboration with *Dr. Hengfei Gu (Rutgers University)*. Nitrogen incorporation is confirmed through the N1s XPS spectra of Figure 6.4. The corresponding N areal density calculated using

the method in [17] as shown in Table 6.1. Silicon nitride ($N\text{-}Si_3$ configuration) as indicated by N1s peaks at 398.2 eV (blue peaks) are observed to present in both NO POA at 1175 °C and N_2 POA at 1500 °C. Moreover, NO POA also resulted in the formation of silicon oxynitride ($N\text{-}Si_2O$ configuration) as indicated by the N1s peak at 399.7 eV (orange peak) [18]. The total N area density due to NO POA is calculated to be 4.7×10^{14} cm^{-2}, which is consistent with [17]. The maximum N areal density achieved through N_2 POA at 1500 °C, 1 h is 2.8×10^{14} cm^{-2}, which is ~40% lower than that resulting from NO POA. Combined with the D_{it} results in Figure 6.5, we

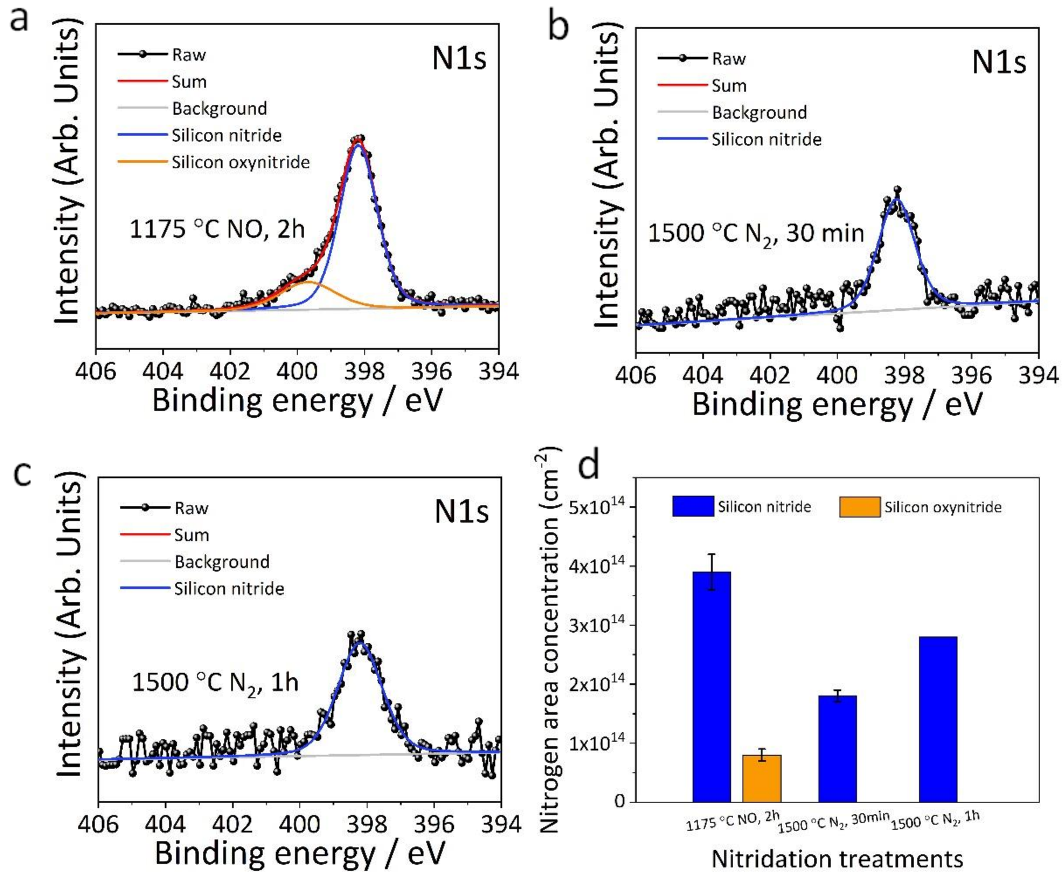

Figure 6.4. (a)-(c) N1s spectra of BOE-etched SiO_2/SiC MOS structures after nitridation treatments including 1175 °C, 2 h NO POA, 1500 °C, 30 min N_2 POA and 1500 °C, 1 h N_2 POA, respectively, and (d) the corresponding nitrogen area concentrations.

conclude that N-update effectively reduces the interface trap density for both n-type and p-type SiO_2/SiC devices. However, when the N areal density $\geq 1.8\times10^{14}$ cm^{-2} there can be negative correlations between N-uptake and the interface trap density for p-type devices that is explained later.

Nitridation conditions	N1s binding energy of silicon nitride (eV)	N1s binding energy of carbon nitride (eV)	N area concentration of silicon nitride (10^{14} cm^{-2})	N area concentration of silicon oxynitride (10^{14} cm^{-2})
1175 °C, 2 h NO	398.2	399.7	3.9±0.3	0.8±0.1
1500 °C, 30 min N_2	398.2	-	1.8±0.1	-
1500 °C, 1 h N_2	398.2	-	2.8 (Error < detection limit)	-

Table 6.1: XPS measurement data showing the amount of nitrogen at the interface for different processes.

6.4.3. D_{it} versus nitrogen at the interface

The values of D_{it} near the E_C (at 3.0 eV) and E_V (at 0.2 eV) are plotted with respect to the nitrogen amount at the oxide-semiconductor interface as shown in Figure 6.5. Here the 1400 °C N_2 annealed sample is assumed to be the zero-nitrogen point because the concentration of nitrogen at the interface for this sample is well below the XPS detection limit. It can be noted that with the

increase of nitrogen amount, the value of D_{it} near E_C reduces continuously. However, for the p-type interface, the value of D_{it} near E_V lowers up to a particular amount but does not reduce further. For p-type, D_{it} due to NO annealing increased. The reason of higher D_{it} with NO annealing compared to N_2, might be due to the effect of lower temperature annealing or associated with additional states generation near the valence band edge that has been explained later using theoretical calculations.

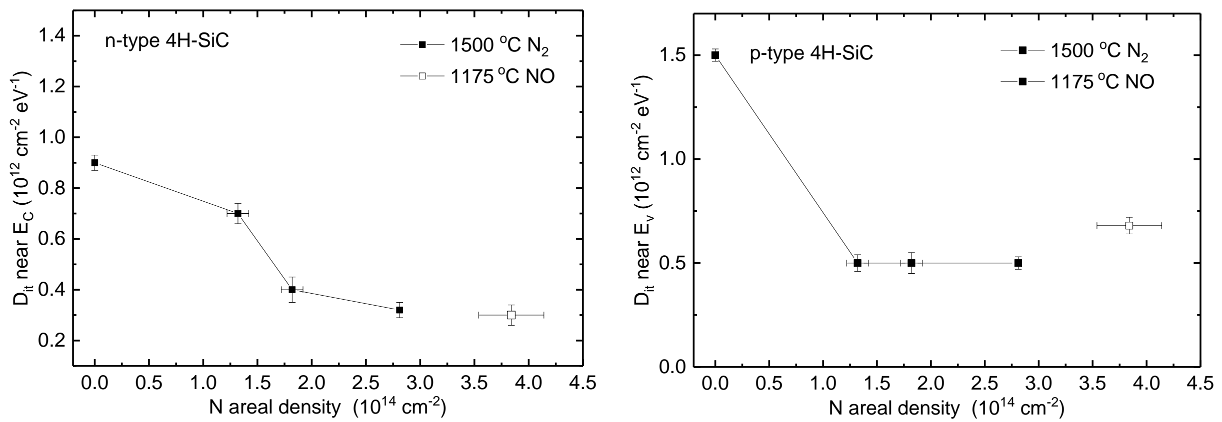

Figure 6.5. D_{it} near the conduction (left) valence (right) band edge versus nitrogen concentration at the interface. Here the zero N point is taken as the 1400 °C N_2 annealed sample because the N_2 amount in this sample was found to be lower than the XPS detection level. X-axis error bar signifies XPS measurement error of nitrogen areal density. Y-axis error bars are the standard deviation of measurement of D_{it} over 5 devices.

6.4.4. Theoretical analysis (*by Dr. Marcelo Kuroda and Dr. Lu wang*)

To gain insights into the nitrided SiO_2/4H-SiC interface at the atomistic scale, the electronic properties of model interfaces are computed using first-principles calculations within the density functional theory (DFT) using the Quantum Espresso software [20]. Computational descriptions of these interfaces employed 3×3-unit cells of the 4H-SiC (0001) with different atomic arrangements near the interface, as illustrated in Figure 6.6.

Atomic cores are described with projector augmented wave (PAW) pseudopotentials and exchange-correlation energy is parameterized by the Perdew-Burke-Ernzerhorf (PBE) functional. The self-consistent field was obtained through integration over the Brillouin zone in a 6×6×1 Monkhorst-Pack k-point grid [21] as well as energy cutoffs set to 60 and 500 Ry for wave functions and charge density, respectively. Atomic positions in the model interface supercells were determined through a structural relaxation until forces were lower than 0.01 eV/Å. Different degrees of nitridation (1.3×10^{14}, 2.7×10^{14}, and 4.0×10^{14} cm^{-2}) were analyzed assuming the N-Si_3 configuration (where N binds to 3 Si atoms) previously found as prevalent in these systems [22].

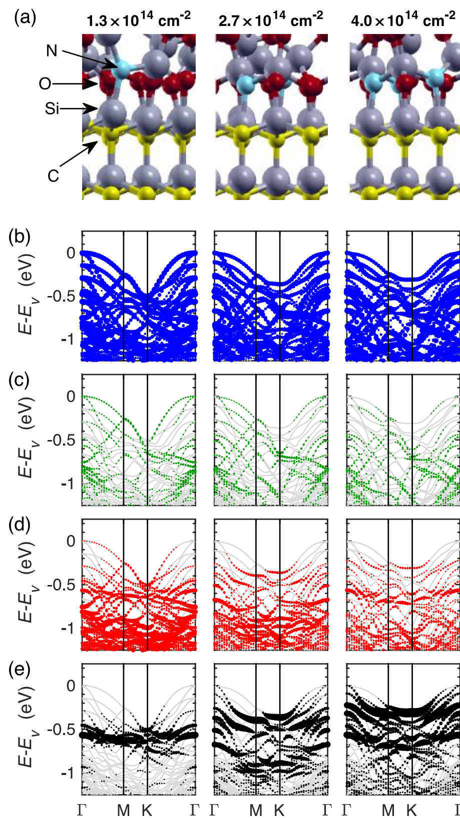

Figure 6.6: Geometric and electronic structure of 4H-SiC/SiO_2 model interfaces with different nitrogen areal density. (a) Geometric configuration of the different interfaces. Corresponding band structures where the projections onto localized atomic orbitals and denoted in color for the atoms near the interface: (b) carbon layer (blue); (c) top silicon layer in SiC (green); (d) oxygen states (red); and (e) nitrogen states (black) adjacent to the interface. Different columns denote the cases with different N areal density (from left to right): 1.3×10^{14} cm^{-2}, 2.7×10^{14} cm^{-2}, and 4.0×10^{14} cm^{-2}.

Figure 6.6 shows the band structures for the interfaces with different nitrogen areal densities. To facilitate the comparison, Bloch states are projected onto localized orbitals corresponding to atoms

(C, Si, O, and N) residing near the interface. Results show that as nitridation level increases the energy position of interfacial Bloch states containing nitrogen gets closer to the valence band edge. This is attributed to the lower electronegativity of nitrogen which in turn decreases the barrier height for holes in the semiconductor. As found in previous work [23], nitridation of the SiO_2/4H-SiC interface removes interfacial traps by compensating for the silicon mismatch between the oxide and alleviating strain. However, the addition of nitrogen forms interfacial states that reside closer to the valence band edge as its areal density increases. These results could provide a qualitative explanation of the D_{it} uptick observed in Figure 6.5 and suggest a weaker hole carrier confinement which may require further studies in p-channel transistor devices.

6.4.5. MOSFET measurements

As N_2 annealing produces a p-type capacitor with the least amount of D_{it} near E_V, p-channel MOSFET is fabricated with a POA of 1500 ^oC N_2. The transfer characteristics of the fabricated MOSFET are plotted in comparison with the As-Ox and NO_2 samples as shown in Figure 6.7. Increased mobility can be observed in N_2 annealed MOSFET compared to 2 h NO annealed one. As D_{it} near E_V reduces, the mobility for p-channel MOSFET is increased.

Later, high-temperature characteristics of the N_2 annealed MOSFET are obtained as shown in Figure 6.8. At higher temperatures, the peak mobility increases when the MOSFET is on. A rise in mobility can be explained due to heightened Coulomb scattering at the channel. Although the D_{it} near E_V is reduced for N_2 processes, the number of deep traps is enhanced due to additional processing related to MOSFET fabrication, as seen from photo CV measurements in Figure 6.9. In this case, at the constant capacitance ledge the value of ΔV becomes ~ 9 V whereas for NO annealed capacitor it is only ~ 4 V. The process of photo CV measurements using UV illumination

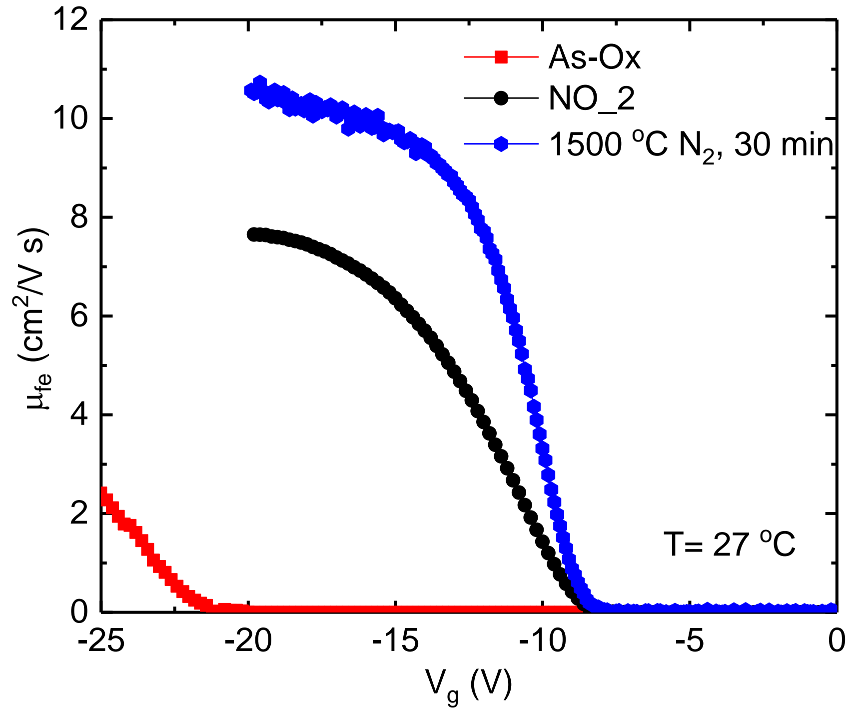

Figure 6.7: Field effect mobility versus gate voltage for p-channel N_2 annealed MOSFET compared with NO annealed and as oxidized MOSFET at RT with MOSFET dimension 200 µm × 200 µm (gate length/ gate width).

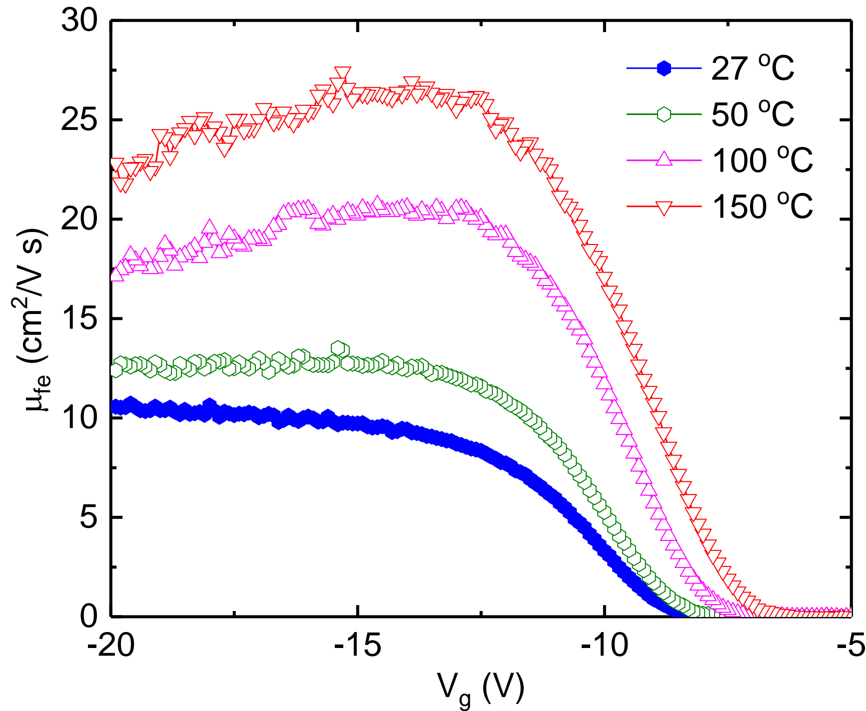

Figure 6.8: High-temperature characteristics of p-channel N_2 annealed MOSFET at V_{ds}=0.1 V.

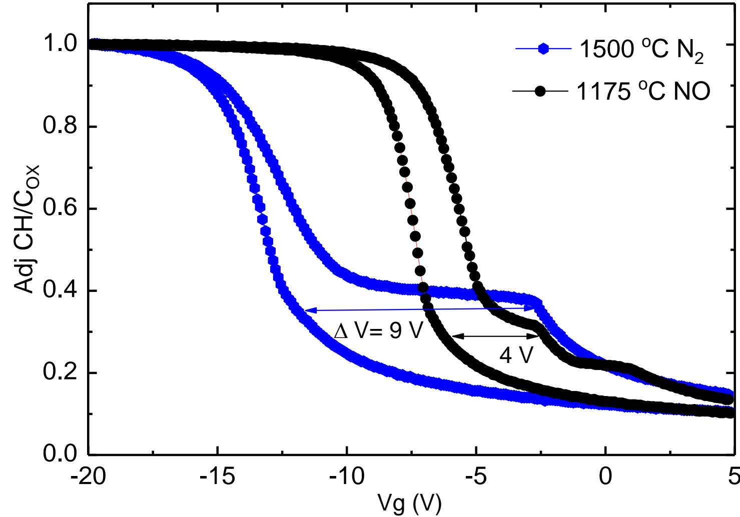

Figure 6.9: Photo CV measurements of 1500 °C N_2 annealed p-type capacitor in comparison with 1175 °C 2 h NO annealed p-type capacitor. ΔV is seen to increase here for N_2 annealed capacitor due to increased deep states.

is discussed in chapter 2. At higher gate voltage the MOSFET mobilities tend to merge due to dominant surface roughness scattering.

6.5. Summary

In conclusion, the effect of high-temperature N_2 post oxidation annealing in 4H-SiC n- and p-type MOS interface is discussed. Among several methods, 1500 °C N_2 annealing is observed to passivate the maximum positive fixed charge and interface traps near the valence band edge. The amount of trap passivation here is greater than that for NO annealed samples. However, for the n-type counterpart, the opposite is true. To quantify the nitrogen areal densities at the interface, X-ray photo electron spectroscopy has been performed and compared with NO annealed samples. For p-type material, D_{it} versus areal nitrogen density curves shows a very small amount of nitrogen is needed for passivation. Furthermore, higher nitrogen concentration may lead to increased trap density. For n-type capacitors, a subsequent decrease of D_{it} is visible with the increase of nitrogen. Finally, theoretical calculation using DFT analysis shows additional nitrogen intake can create

states near E_V explaining the D_{it} increase due to increased nitrogen concentration at the p-4H-SiC/SiO_2 interface. P-channel MOSFET fabricated using N_2 annealing shows higher field-effect mobility due to reduction in D_{it} near E_V. However, because of increased deep traps due to additional processing in MOSFET fabrication, mobility increases at a higher temperature. These results are crucial in finding successful alternative annealing treatment for 4H-SiC MOSFETs that can potentially replace NO for good.

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Chapter 7

Conclusion and future work

7.1. Conclusion

In conclusion, wide band gap semiconductors are the present and future of high-power and high-temperature electronics, and 4H-SiC plays the leading role in it. In the wake of green technology, in application areas where Si fails to produce energy-efficient devices, 4H-SiC simply outperforms and achieves higher expectations in terms of device operation. However, the performance and reliability of the 4H-SiC devices can yet be improved significantly. Moreover, to produce the most energy-efficient devices both n- and p-channel MOSFETs are necessary. At the starting of this thesis, the research on p-channel MOSFET was quite sparse compared to n-channel. Therefore, the focus of this thesis has been to find solutions to improve p-type conduction alongside the effect of the implementations on its n-type counterparts. Here, the chapter-wise findings are summarized below.

Chapter 3

- In an attempt to improve p-channel conduction, several post oxidations annealing (POA) treatments such as NO, H_2, and NO+H_2 were first used for different durations to passivate interface traps and fixed charges in p-type 4H-SiC/SiO_2 interface as shown in *chapter 3*.
- Simultaneous Hi-Lo CV is used to extract D_{it} near valence and conduction band edges, for different processes and compared to determine the most effective POA for MOSFET fabrication. Additionally, high frequency (100 kHz) CV curves are compared to find degrees of passivation in fixed charges between processes. Among these different processes, NO POA passivated the maximum number of shallow traps near E_C and E_V and lessens the number of fixed charges at the interface.

- To find the interface traps deeper in the bandgap, photo-assisted CV measurements are conducted using UV light and compared between processes. Although NO POA was the most efficient, the effect of H_2 POA in reducing deep traps can clearly be observed from these measurements. NO+H_2 is also seen to passivate a comparable number of deep traps as NO.
- From these observations, NO annealing surpasses all POA treatments in reducing both shallow and deep traps at the interface. Therefore, to find the optimum conditions for p-channel MOSFET fabrication a thickness-dependent study using NO POA is conducted. This experiment reveals that the oxidation rates for n- and p-type 4H-SiC are different. In addition, a combination of 10 h oxidation and 2 h NO POA contains the least number of traps and fixed charges at the interface, indicating the most effective combination for p-channel MOSFET fabrication that has been discussed in the later chapters.

Chapter 4

- Started with NO annealed MOS capacitors to determine the total reduction of traps in the whole 4H-SiC bandgap through high-temperature simultaneous Hi-Lo CV measurements. Later, NO annealed p-channel Hall bar MOSFET is fabricated that enables enhancement mode MOSFET operation at high temperature (300 °C).
- High-temperature transfer characteristics show a reduction in threshold voltage with the increasing temperature that indicates the reduction of occupied D_{it} with rising temperature. Additionally, field effect mobility is seen to be independent of temperature at strong inversion.
- High-temperature Hall measurements are conducted to study hole channel transport in NO annealed 4H-SiC MOSFETs. Hall measurements confirm that the dominant surface

roughness scattering is responsible for the weak temperature dependence in the strong inversion region. A rigorous analysis of the strong inversion region is conducted in the next chapter. On the other hand, in weak inversion, transport is observed to be limited by hole trapping in interface traps and Coulomb scattering.

- Furthermore, a device reliability study is conducted using constant negative gate bias stress tests (NBTI) on NO annealed p-type MOS capacitor. NBTI detects a temperature-activated oxide hole trapping mechanism is present in the device that could be related to the interfacial nitrogen creating additional states or oxygen vacancies present at the 4H-SiC/SiO_2 interface.

<u>*Chapter 5*</u>

- A comprehensive analysis is performed on the strong inversion region of NO annealed p-channel 4H-SiC MOSFETs and compared with fabricated n-channel 4H-SiC MOSFETs. For this purpose, a body bias and temperature-dependent Hall measurements on nitrided n- and p-channel 4H-SiC MOSFET are carried out and analyzed with respect to the transverse electric field (E_{eff}) present at the channel. This helped to study the scattering mechanisms present at the channel of 4H-SiC MOSFETs more rigorously.
- Hall measurements are conducted at different body biases to find the power law dependence of channel electron and hole mobility μ_{Hall} on the E_{eff} for surface roughness scattering at a constant screening is determined. μ_{Hall} is observed to depend on E_{eff} as $E_{eff}^{-1.7}$ and $E_{eff}^{-2.3}$ for n- and p-channel MOSFETs respectively.
- Condition for observing phonon scattering limited mobility for p-channel MOSFET is explored. The application of forward body bias allows for imitating the characterization of a MOSFET made on a lightly doped substrate. In this case, the channel is thick enough to

interact with the substrate lattice vibration showing phonon scattering and limited hole mobility. Overall, this chapter signifies the importance of 3 types of scattering mechanisms at the channel and the substrate doping concentration of a 4H-SiC MOSFET.

Chapter 6

- Alternating annealing treatment for p-channel 4H-SiC MOSFET to replace toxic and expensive NO is found. High temperature (1500 °C) N_2 post oxidation annealing passivates more interface traps compared to standard NO annealing near the valence band edge. Moreover, this method also passivates maximum positive fixed charges for p-type capacitors observed through High-frequency CV measurements. Whereas for the n-type counterpart NO annealing is still found to be the most effective annealing treatment.
- Working with Rutger's University, X-ray photo electron spectroscopy (XPS) has been conducted to find nitrogen areal densities at the interface due to N_2 annealing and compared with NO annealed samples.
- D_{it} versus nitrogen areal density curves for p-type 4H-SiC indicates that the areal density of nitrogen at the interface over a certain amount can have an adverse effect on passivating D_{it}, later that has been explained through theoretical analysis that shows the creation of additional states near E_V due to further nitridation on p-4H-SiC/SiO_2 interface.
- P-channel MOSFET is fabricated using N_2 annealing and characterized at high temperatures. N_2 annealed MOSFET produces higher mobility than NO annealed p-channel MOSFET.
- As temperature increases, the threshold voltage reduces due to the lowering of occupied interface trap density. The field effect mobility is seen to increase with rising temperatures because of increased deep traps due to additional MOSFET processing steps.

7.2. Future work

During the production of this thesis, while working on different projects, experimental methods are incorporated relying on the availability of the instruments and standardized methods. To produce better-performing p-channel MOSFETs, processes can be optimized at different stages of fabrication. Additionally, some unexplored methods related to 4H-SiC p-channel MOSFET fabrication can be implemented for producing better channel conduction and device stability that are listed below.

- In this thesis, Titanium is used as the source-drain (SD) contacts for p-channel MOSFETs fabrication. Ti needed to be annealed at 1000 ^{o}C to make the contacts Ohmic. Due to this process, the gate oxide is exposed to a high-temperature annealing environment where it might have unfavorable consequences such as a device with leaky gates, an increase in D_{it}, and mobile ion effects. The SD contacts could be optimized with other metals or highly doped semiconductors that need less annealing temperature to form ohmic contacts.
- Bias temperature instability measurements on NO annealed p-type capacitors show significant temperature-activated hole trapping that causes the flat band voltage to increase more. This effect could be because nitrogen or oxide related as theorized earlier. Therefore, more studies on reducing the temperature-activated traps and the role of nitrogen at the interface are required.
- The effect of deposited oxide on p-channel MOSFETs can further be explored. Oxide deposited on p-type capacitors using low-pressure chemical vapor deposition (LPCVD) is seen to be creating more interface traps. However, oxide deposited by other methods

such as atomic layer deposition (ALD), and plasma-enhanced chemical vapor deposition (PECVD) are yet to be explored on p-channel 4H-SiC MOSFETs.

- Recent studies show that H_2 etching prior to oxidation can lead to a cleaner 4H-SiC surface and a less trappy oxide semiconductor interface. For deposited oxide, this process step could be vital in reducing interface traps and fixed charges.
- Field effect mobility of N_2 annealed MOSFET is used here to study temperature and bias effect on these MOSFETs. For an elaborated study of channel scattering mechanisms, Hall bar MOSFETs using N_2 annealing can be used. Hall measurements were unsuccessful in the limited number of trials to fabricate Hall bar MOSFET using the N_2 annealing method. Therefore, more process optimization is needed for successful Hall bar MOSFET fabrication and measurements using N_2 annealing methods.
- The effect of high k dielectric on p-channel MOSFETs is still unexplored. A combination of these dielectric and optimized N_2 annealing treatments may produce effective results in producing higher mobility p-channel MOSFETs with lower $D_{it.}$
- p-channel MOSFETs fabricated on different faces of 4H-SiC are still unchartered. Hole transport on the MOSFETs fabricated on faces such as a-face, m-face, and c-face of 4H-SiC could be an interesting study to observe how analogous they are to electron transport on these faces.

Appendix A

Sample cleaning procedures

Ground yourself first to avoid charge injection.

1. Rub the surface of 4H-SiC samples with a cotton swab and acetone to remove sticky layer.
2. Next put the samples 5 minutes in an ultrasonic shaker on each of the chemical subsequently
   (a) Acetone
   (b) Trichloroethylene (TCE)
   (c) Acetone
   (d) Methanol
   (e) Methanol
   (f) Deionized (DI) Water
3. Remove the samples and put it for 5 minutes in a buffered oxide etch (BOE) solution.
4. Next, 5 minutes in a DI water ultrasonic shaker
5. Later, put the samples for 15 minutes in 1:1 H_2SO_4:H_2O_2 solution. Following that rinse in DI water for 30 sec, BOE for 1 m, and DI water for 30 sec again.
6. Next, put the samples in 3:1:1 DI H_2O:H_2O_2:NH_4OH for15 minutes at 100-115 ^oC temperature. Followed by rinsing in DI water for 30 sec, BOE for 1 minute, and DI water for 30 sec again.
7. Clean with H_2O_2:HCl for 15 minutes at 100-115 ^oC. Later clean with 30 sec DI water, BOE for 1 minute, and DI water for 30 sec again.

Appendix B

Thermal oxidation procedures

Ground yourself first to avoid charge injection.

1. Check if the exhaust is closed.
2. Open the vacuum valve of the oxidation furnace tube and lower pressure to ~ 200 mTorr.
3. Vent the furnace with oxygen flowrate 500 sccm and let it flow 10-15 min.
4. Load the samples by pulling the glass handle into the furnace.
5. Pull vacuum again by opening vacuum valve and reduce pressure.
6. Vent the furnace with oxygen again and let it flow 10-15 min to remove residual gases.
7. Ramp up the furnace temperature to 1150 ^{o}C and at a rate of 5 ^{o}C/ min at flowing oxygen.
8. At 1150 ^{o}C, Start the timer for desired oxidation time.
9. After the oxidation is finished, begin argon, and stop oxygen.
10. Let the samples anneal in Ar for 30 min.
11. Ramp down the furnace temperature to 900 ^{o}C at a ramp rate of 10 ^{o}C/min in flowing Ar.
12. Ground yourself by putting on grounding strap to avoid static charge injection into oxide.
13. Remove samples from oxidation chamber 900 ^{o}C.
14. After sample removal, vacuum the furnace tube and back fill with Ar and close the exhaust.

Appendix C

NO annealing procedures

Ground yourself first to avoid charge injection.

1. Check if the exhaust is closed.
2. Open the vacuum valve of the oxidation furnace tube and lower pressure to ~ 200 mTorr.
3. Vent the furnace with Ar with a flowrate 500 sccm and let it flow 10-15 min.
4. Load the samples by pulling the glass handle into the furnace.
5. Pull vacuum again by opening vacuum valve and reduce pressure.
6. Vent the furnace with Ar again and let it flow 10-15 min to remove residual gases.
7. Ramp up the furnace temperature to 1175 ^{o}C and at a rate of 5 ^{o}C/min at flowing Ar.
8. At 1175 ^{o}C, begin NO (at 575 sccm) for desired annealing time and turn off argon flow.
9. Keep the NO regulator to 15 psi.
10. After NO annealing is done, close the tank top.
11. Flow Ar to the chamber through the NO lines as to clear out NO because it is toxic.
12. Ramp down the furnace temperature to 900 ^{o}C at a ramp rate of 10 ^{o}C/min in flowing Ar.
13. Ground yourself by putting on grounding strap to avoid static charge injection into oxide.
14. Remove samples from oxidation chamber at 900 ^{o}C.
15. After sample removal, vacuum the furnace tube and back fill with Ar and close the exhaust.

Appendix D

N_2 annealing procedures

Ground yourself first to avoid charge injection.

1. Connect the exhaust pipe.
2. Flow N_2 in the furnace at a rate of 3 L/min for 10-15 min to remove residual gases.
3. Slowly drag out the boat from inside the furnace.
4. Load samples, push the boat at the hot zone, and close the furnace.
5. Ramp up the furnace temperature to 1500 ^oC and at a rate of 5 ^oC/min at flowing N_2.
6. At 1500 ^oC, start timer for desired annealing time.
7. After annealing is done ramp down the temperature at a rate of 10 ^oC/min at flowing N_2.
8. Ground yourself by putting on grounding strap to avoid static charge injection into oxide.
9. Remove samples from oxidation chamber at 900 ^oC, close the furnace and the N_2 cylinder.

Appendix E

Hydrogen Anneal Procedure

1. **Step 1**

To check if enough Ar is there and if the lines are clear (Cause purging will be needed at the end of the process)

- **Flow Ar through the H_2 lines to the furnace**
  - Open the Argon cylinder and set the output at 20psi
  - Open the PGI valve at the hydrogen station
  - Open the HPI valve at the hydrogen station
  - Open the black hydrogen knob close to the furnace
  - Switch on the 2 on MKS(mass flow meter) and set Ar flow to 500sccm
  - Open the exhaust of the furnace.

Once the flow is good

2. **Step 2**

Vaccuum the chember and the lines

- Close the the two valves at hydrogen cylinder station PGI and HPI
- Close the exhaust at the furnace and close the hydrogen black knob (near to the furnace) and close the MKS # 2
- Open the green valve for vaccuming the furnace.
- Check the HPV is closed
- Open the overhead green valve near to the hydrogen clylinders.

- Now open the knobs HPI and HPV and set the regulator to maximum by turning full clockwise.
- Wait until the pressure at the right gauze reaches around 150 mT which shows pressure for the hydrogen lines.
- Close the overhead green valve near the hydrogen cylinder(don’t close the furnace vacuum knob yet).
- Close HPI and HPV valve at hydrogen station
- Turn the regulator anticlockwise full to zero.

3. **Step 3**

Fill hydrogen lines with Hydrogen (Hydrogen knob near the furnace and the MKS #2 is closed)

- Open HPI knob
- Open hydrogen cylinder
- Set the regulator to 10-12 psi and leave it like that.

4. **Step 4**

Back fill the furnace with Ar (Flow Ar to the furnace through it’s own line MKS #3)

- Close the vaccum green valve near the furnace
- Switch on # 3 in the MKS and open Ar knob near the furnace and continue the flow at 500 Sccm.
- When pressure at the left pressure gauze reaches at 760 T, Open the exhaust of the furnace

- Load the samples at 800 C (putting ground strap on).

5. **Step 5**

Vaccum the furnace 2nd time and back fill with Ar

- Close the exhaust
- Close the MKS no.3
- Open the green vaccum knob near the furnace
- Check for a pressure drop of 0.6 T at the left pressure gauze.
- Close the green vacuum knob near the furnace.
- Open Ar at the MKS no.3 and back fill the furnace
- At 760 Torr. Open the exhaust and keep the Ar flowing.
- Set the temperature to 1000 ^{o}C at a ramp rate of 5C/min and keep Ar flowing.

6. **Step 6**

Flowing H_2 at 1000 ^{o}C

- Once 1000 ^{o}C is reached open the hydrogen black knob near the furnace.
- Open #2 at the MKS.
- At #2 of the MKS when 500 sccm H2 is flowing then close no. 3 (Argon)
- Set the timer to 30 min.

7. **Step 7**

Purging Ar and ramping down

- Once 30 min is over open the Ar at MKS no.3 and keep the Ar flowing throgh it's own line.
- Close the hydrogen at it's cylinder but keep the HPI valve open

- Open the PGI valve to purge Ar through the H_2 line.(When you see a output pressure drop from 10 towards 0 at the H_2 regulator)
- Keep the Ar flow throgh both #2 and #3 line (may need to set the H_2 regulator to make 500 sccm Ar flow at MKS #2).
- Turn the temp. down to 800 ^oC at a rate of 10C /min

8. **Step 8**

Closing of H_2

- At 800 C take samples out(put the ground strap on)
- Turn hydrogen regulator to zero.
- When the flow comes to zero at MKS no.2 then close all the valve(PGI,HPI,HPV) at the hydrogen station(in a way we kept the line of H_2 filled up with Ar).
- Switch off #2 in MKS

9. **Step 9**

Vaccuming the furnace and closing the process

- Close the exhaust of the furnace
- Close Ar at the MKS no. 3
- Vaccum the furnace by openning the green vaccum knob near to the furnace.
- Back fill with Ar at 0.6 Torr.
- When pressure reaches to 760 Tor then close the Ar flow both at MKS no.3 and in the Ar cylinder.
- Check all the valves are closed and exhausts are closed.

Appendix F

Al evaporation procedure

Ground yourself first to avoid charge injection.

1. Turn OFF the Ion Gauge.
2. Close the high vacuum valve.
3. Open the Nitrogen (N_2) gas cylinder and vent the chamber.
4. Load Al pallets in the tungsten basket.
5. Load the samples facing down either with shadow mask or patterned through lithography.
6. Open the roughing pump slowly.
7. At 50 mTorr, close the rouging valve, and open the fore-line valve.
8. Slowly open high vacuum valve to the chamber, and let it pump minimum 4-5 hours.
9. At pressure ~ 10^{-7} Torr, turn on the DC power supply and Ammeter.
10. Turn on the variac power to 60 % slowly.
11. Pre deposit Al for 15-20 seconds.
12. Remove the shutter and deposit Al on samples for 3-4 minutes.
13. Then, turn the variac back to 0%, turn off the voltage supply, and the ammeter.
14. Turn off Ion gauze and close high vacuum valve
15. Back fill with N_2
16. Remove samples
17. Repeat step 6 to 8 and return the system to stand-by mode.

Appendix G

Photo Lithography procedure

Ground yourself to avoid charge injection.

1. Put a small amount of 5214E photoresist and attach sample.
2. Attached extra dummy samples at the edge to avoid edge beads.
3. Bake for 15 minutes in oven at 105 ^{o}C.
4. Spin coat with AZNLOF 2070 (negative) or 5214 (positive) photoresists at 4000 rpm for 30 sec.
5. Perform a soft bake for 90 sec 105 ^{o}C. 12.
6. Remove the dummy edge samples.
7. In the mask aligner put the mask using vacuum suction.
8. Aligning the mask with the sample
9. Expose UV for 30 sec and 1 minute for 5214 and 2070 photoresists, respectively.
10. If 2070 used, post bake 90 seconds followed by the UV expose.
11. Develop in AZ 726 MIF developer.
12. Rinse in DI water and dry with nitrogen.

Appendix H

DC sputtering procedures

Ground yourself to avoid charge injection.

1. Turn off the ion gauge.
2. Close the High vacuum valve.
3. Fill with house nitrogen. (Open wall valve and air inlet at the chamber)
4. At atmospheric pressure (~790 torr) close nitrogen valve and air inlet valve.
5. Open the chamber and place the samples underneath the big circular disc.
6. Put desired target, chimney, and corresponding power outlet.
7. Close the chamber.
8. Open the roughing pump slowly.
9. When presser gets less than 40 mTorr, close the roughing valve.
10. Open the fore-line valve and slowly open high vacuum valve.
11. At around 10^{-7} Torr, turn off ion the gauge.
12. Close partial high vacuum valve underneath.
13. Open Ar (80 sccm, 18 mTorr) wall knob and knob near the chamber.
14. Check for correct power line for target and if the cooling water valve is open.
15. Turn on the circuit breaker and increase voltage up to plasma ignition.
16. Once plasma ON, maintain the current (Mo=0.4 A, Ti=0.4 A, Ni=0.2 A etc) by using the voltage knob.
17. Pre sputter for 2 minutes and sputter on the samples for desired time.
18. Turn down the voltage and power off the circuit breaker.
19. Close Ar wall knob and the other knob.

20. Close high vacuum valve and open nitrogen.

21. Take the samples out.

22. Clean the sputtering chamber by vacuum cleaner.

23. Pump down the chamber to standby mode.

Appendix I

Reactive Ion Etch procedure (RIE)

1. Attach sample to 2-inch Si wafer and do the required lithography pattering.
2. In RIE chamber, open the glass window.
3. Place wafer on the electrode center.
4. Flow N_2 and close the glass window and tighten until snug.
5. Open the vacuum valve and keep vacuuming until system reaches ~ 15 mTorr.
6. Open all the valves to clear gas line and turn on the appropriate switch on the flow controller.
7. After base pressure is reached, flush the gas line for 5 minutes.
8. Turn on the RF power supply switches.
9. Adjust the flow rate of the etchant gas (NF_3, or SF_6) and power.
10. Set the desired time of etching and turn ON RF power.
11. Adjust the shunt and reflected power knob to make the reflected power zero.
12. After the desired etch time, turn off the RF power.
13. Turn off the etchant gas valves and power knob and allow system to vacuum to its lower base pressure.
14. Before opening chamber, fill the chamber with nitrogen for 1 minute and vacuum again.
15. Repeat step 14 for at least three times to get rid of any toxic etch gas.
16. Close the vacuum valve and fill the chamber with N_2 to reach atmospheric pressure.
17. Remove the sample.
18. Fill the chamber with N_2 for 1 minute and close all the gas tanks.
19. Vacuum the chamber.

20. Close the vacuum valve and turn off the vacuum pump.

Appendix J

Ohmic anneal furnace procedure

1. Close ion gauze and close the high vacuum valve.
2. Flow Ar through Ohmic anneal furnace for 5 min at 12 LPM once atmospheric pressure is reached reduce the flow rate 4 LPM.
3. Once the paddle reaches at 50 ºC, close Ar, open loading area and load samples.
4. Close the loading area.
5. Put the paddle at a desired length.
6. Flush with Argon for 5 min.
7. Ramp up the temperature to 1000 ºC at a rate 5 ºC/min.
8. Stop Ar and vacuum the furnace tube until 10^{-7} Torr is reached.
9. Turn the ion gauze off and close the high vacuum valve.
10. Flush the system with Ar for 5 min at 12 LPM.
11. Insert the samples into furnace and start timing for 2 min once sample temperature reaches 975 °C.
12. After 2 min annealing is finished, transfer samples from hot to cooler zone.
13. When the paddle temperature is reached to 50 °C, close Ar flow.
14. Drag the paddle in the loading zone and remove samples from system.
15. Close furnace, flow Ar for 5 min
16. Close Ar and vacuum the furnace and return Ohmic anneal system to stand-by mode.

Appendix K

Carbon cap anneal

1. Stick the sample with a little bit of water-soluble wax on a Si wafer.
2. Spin on 5214 photo resists at 4000 rpm for 30 sec.
3. Remove the sample from Si wafer and put it in water.
4. Bake the sample with photo resist for 15 minutes at 115 ^{o}C.
5. Put the sample now in the carbon cap designated box facing up.
6. Put the box with the sample in the high temperature annealing furnace.
7. Vacuum the system to a pressure of ~ 10^{-7} Torr.
8. Fill the chamber with Ar and keep a flow rate of 8 psi.
9. Turn on the circuit breaker and keep increasing the variac.
10. First increase the variac to 10 % and wait for 10 minutes.
11. Then keep increasing 5 % in every two minutes up to ~ 28 %.
12. Try to hold the temperature at about 600 ± 5 ^{o}C for 30 minutes by adjusting variac.
13. After 30 minutes, turn down the variac, and turn off the circuit breaker.
14. When temperature reaches less than 50 ^{o}C, stop the Ar flow.
15. Open chamber and get the samples out.
16. Put the carbon cap box to its designated place.
17. Vacuum the chamber and leave it in standby mode.

Appendix L

4H-SiC dopant activation procedures

1. Complete carbon cap process first.
2. Place the sample, with carbon cap facing down, in designated carbon box for activation anneal.
3. Close ion gauze and high vacuum valve.
4. Fill the system with argon, and then load the sample, make sure the thermocouple touches the anneal box.
5. Vacuum the system until pressure is ~3×10^{-7} Torr.
6. Turn off ion gauze and close High vacuum
7. Fill with argon to atmospheric pressure and keep a flow rate of 12 psi.
8. Increase variac power 1% every ten seconds until variac reaches at ~ 55%.
9. Adjust variac to keep temperature stabilized at 1650 °C ±5°C for 30 min.
10. After 30 min, turn down the variac to zero.
11. When temperature is less than 50°C, stop Ar flow and open the chamber.
12. Carefully remove sample and put the carbon cap box back to its storage container.
13. Vacuum the system to leave it at standby mode.

Appendix M

LPCVD oxide deposition process

1. **Step 1**

- **Inside Clean room**
- Set the TEOS heater to 3.5 in the Down chamber
- Check the Vacuum pump is ON below the keyboard
- wait 1hr until the Temp comes around 50 ^{o}C
- Check "TEOS Channel Temp" is set to 2
- (Any type of samples cleaning can be done this time if needed)

2. **Step 2**

- **After 1 h of temp. gain to 50C**
- Outside the clean room
- open 3 types of Nitrogen chamber (around ~2000 psi)
  i. Ultra-purified
  ii. Industrial
  iii. House Nitrogen
- switch ON 24V
- Switch ON Cross Purge

3. **Step 3**

- **Inside Clean room**
- On the back wall behind the LPCVD
- open the UHP N2 knob
- check if the water supply there is opened

- House N_2 is opened
- Inside LPCVD chamber
- open the right knob out of two knobs written as UHP N_2 (Up chamber)
- Vacuuming- Open two Black knob at the down chamber
- In the program close open #10 and watch the pressure in #14 to drop to 0
- Close the #10 valve again

4. **Step 4**

- **In Down chamber open two knobs of TEOS bottle**
- In the program open file named "TEOS 650N2 in H2"
- At the recipe Change the deposition time accordingly at stage #8
- open the program and click on RUN
- At the 2nd stage when the pressure goes up to 760 T then we can load samples
- After stage 3 look for closing valve 4 by itself
- After stage 4 valve 10 open by itself
- After 5th stage we need to do TEOS Switching

5. **Step 5**

- **TEOS Switching**
- Open knob on the right wall of LPCVD chamber to TEOS
- close the right valve at the down chamber
- At the half of stage 7 close the left valve and open the right valve at the down chamber
- Deposition will start at #8 stage
- After 5 min of deposition look for the TEOS pressure at the valve #14 in the program and write on the logbook.

6. **Step 6**

- After stage 8 when the deposition is done close the wall knob for TEOS
- open the left valve so that both valves are open in the down chamber
- 1min before the finishing of stage 10 take sample out slowly as the tube is hot

7. **Step 7**

- **Closing**
- Hit STOP
- Hit Close
- Close UHP H_2 knob in up glass chamber
- close two valve in the down chamber
- close two valve in TEOS bottle in the down chamber
- Switch off heating
- Close UHP N_2 on the wall
- Don't close cooling
- Outside the clean room
- Turn Off Cross Purge
- Turn Off 24 V
- Close UHP N_2 chamber
- Close industrial N_2 chamber

Appendix N

Additional gate passivation trials

A1. Gate oxide deposition by low pressure chemical vapor deposition (LPCVD)

In addition to the gate passivation processes described in the thesis, some additional gate passivation methods are also carried out. However, unfortunately they did not produce desired outcomes. Low pressure chemical vapor deposition (LPCVD) is used to deposit oxide on top of n- and p-type 4H-SiC. The oxides were then densified in flowing oxygen at 700 ^{o}C. The CV and D_{it} figures in comparison with other processes are shown in Fig. A1 (left and right). For n-type capacitor, LPCVD deposited oxide is seen to contain more negative fixed charge and increasing D_{it} at the interface compared to As-ox (thermal dry ox).

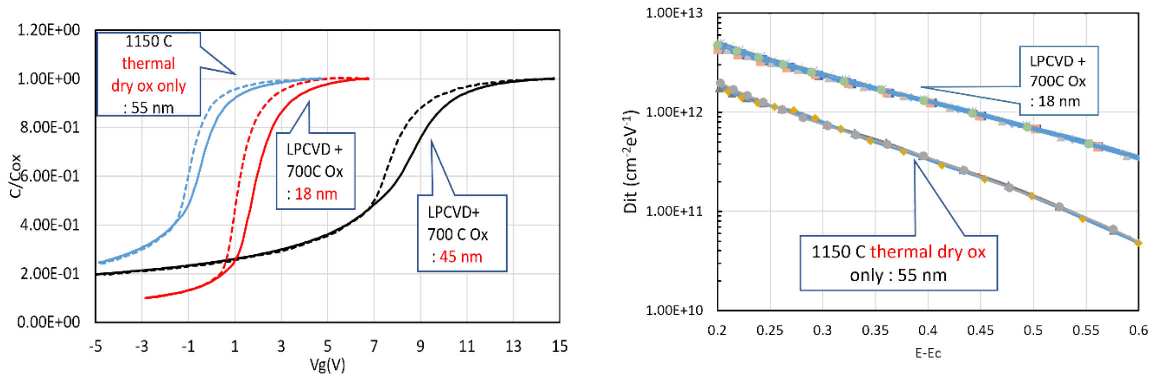

Figure A1: (left) CV curves for LPCVD deposited oxide on n-type 4H-SiC. (Right) D_{it} curves near E_C compared to dry-oxide only samples.

For p-type 4H-SiC the oxide quality produced was very poor using LPCVD deposited oxide. The MOS capacitors fabricated using this method were not reaching into accumulation due to gate oxide break down. The D_{it} near E_V also increased compared to the As-Ox (dry ox) samples as shown in Fig. A2 (left and right).

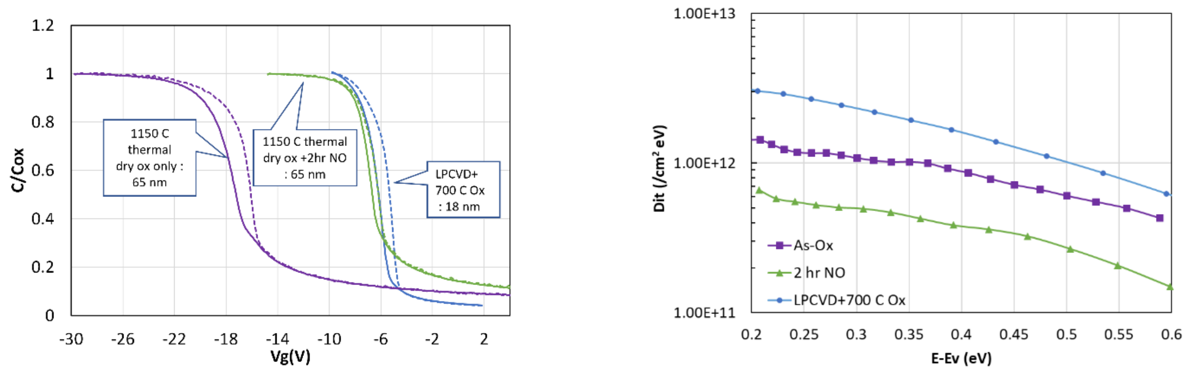

Figure A2: (left) CV curves for LPCVD deposited oxide on p-type 4H-SiC. (Right) D_{it} curves near E_V compared to dry-oxide only samples.

A2. Pre oxidation annealing treatments

In an attempt to incorporate nitrogen at the interface on deposited oxide, pre oxidation annealing treatments were conducted using nitrogen plasma annealing at 1160 ^oC and separately on a different furnace high temperature N_2 annealing at 1400 ^oC and 1600 ^oC before depositing oxide using LPCVD. Although nitrogen was incorporated at the interface successfully, as confirmed from XPS measurements, the electrical results were not satisfactory. The results of these methods are discussed below.

A.2.1. N_2 plasma pre oxidation annealing

In introducing high temperature N_2 plasma annealing, the negative fixed charge at for n-type capacitor is reduced (Fig. A3 left). Also, the D_{it} near E_c is decreased from unannealed sample as shown in Fig. A1 (right) and Fig. A3 (right). However, for p-type capacitors the results are disappointing. Due to introduction of large number of positive charges at the interface the CV curves moved left and they were unable to reach accumulation due to bad quality of oxide (Fig. A4). As a result, D_{it} near E_V could not be extracted.

To check break down voltage on these devices, current -voltage curves (I-V) are obtained as shown in Fig. A4 (right). The n-type capacitors are seen to have a similar break electric field ('E' at $J=10^{-4}$ A/cm^2) compared to thermally grown oxide. However, for p-type capacitors, the break don voltage is very low due to weak gate oxide.

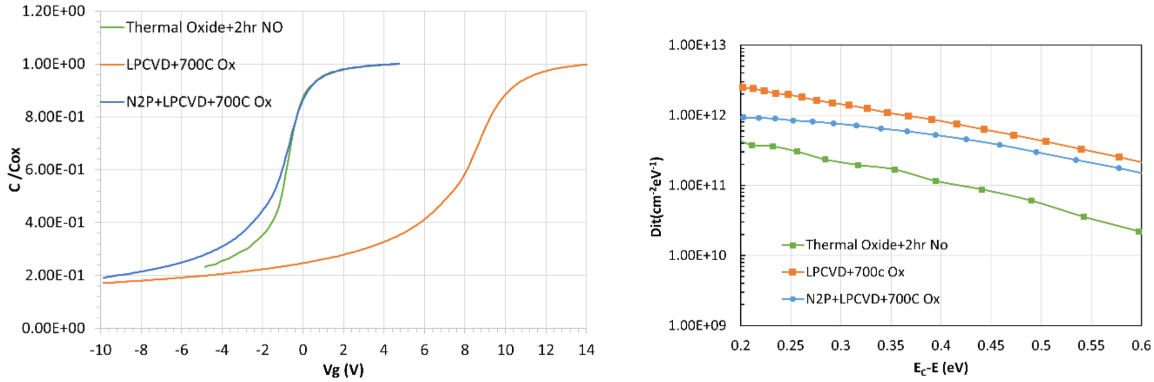

Figure A3: (left) CV curves for nitrogen plasma annealed followed by LPCVD deposited oxide on n-type 4H-SiC. (Right) D_{it} curves near E_C compared to dry-oxide only samples.

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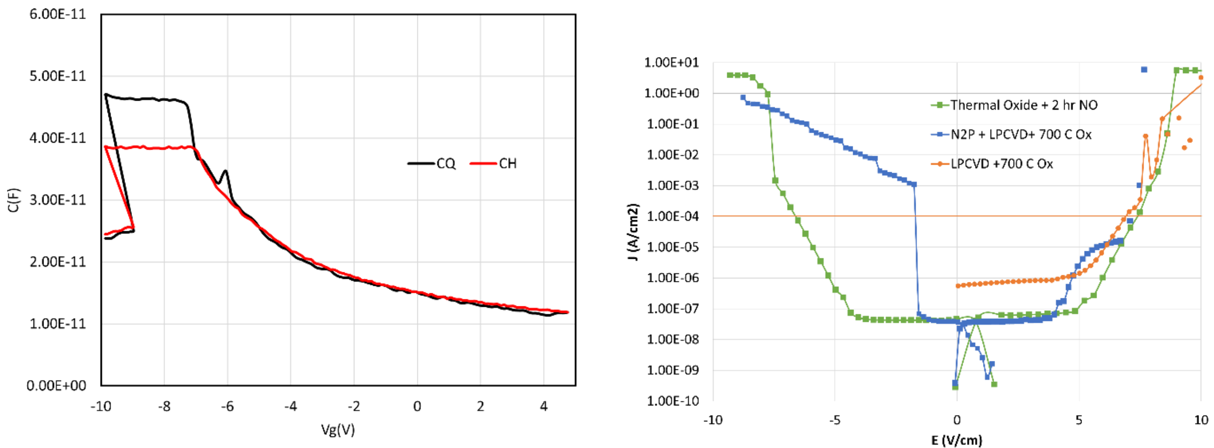

Figure A4: (left) CV curves for nitrogen plasma annealed followed by LPCVD deposited oxide on p-type 4H-SiC. (Right) D_{it} curves near E_C compared to dry-oxide only samples.

A.2.2. High temperature pre oxidation N_2 annealing

N_2 annealing at 1400 °C and 1600 °C are conducted on 4H-SiC prir to depositing LPCVD oxides on n- and p-type 4H-SiC. As shown in Fig. A5 left and right, the CV curves does not reach into accumulation before gate oxide break down in either case due to poor oxide quality. Therefore, this process could not be explored further.

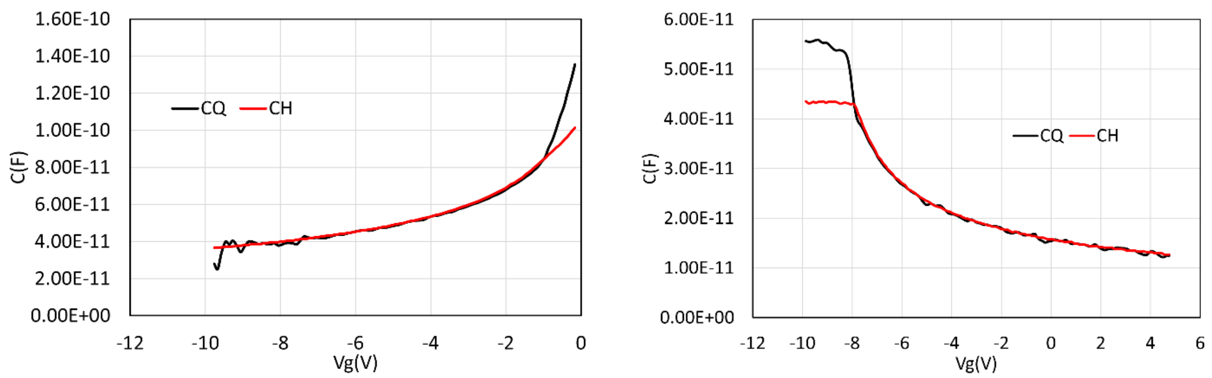

Figure A5: (left) Typical CV curves for high temperature (1400 °C) nitrogen annealed followed by LPCVD deposited oxide on n-type 4H-SiC. (Right) Typical CV curves for high temperature (1400 °C) nitrogen annealed followed by LPCVD deposited oxide on p-type 4H-SiC.