The Effects of High Temperature Ion Implantation in β-Ga_2O_3

by

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Abstract

Doping electronic oxides is often challenging due to issues like self-compensation, limited solubility, and defect formation. Additionally, there is typically an imbalance in favor of one type of conductivity, most commonly n-type. Another key factor is the impact of post-growth annealing, used for forming contacts or activating dopants, on material conductivity, which depends on the annealing environment. Ion implantation is an appealing technique for device processing because it enables precise control over dopant concentration and spatial distribution, allowing selective doping of specific regions within a material. While the effectiveness of high-temperature ion implantation in SiC is well-documented, this work focuses on investigating its influence on the conductivity and crystal structure of β-Ga_2O_3.

This study highlights the benefits of performing silicon ion (Si^+) implantation at elevated temperatures to achieve controlled, heavily doped regions in gallium oxide. Silicon implants were introduced into MBE-grown (010) β-Ga_2O_3 films at both room temperature (RT, 25 °C) and high temperature (HT, 600 °C) to form approximately 350 nm deep Si-doped layers with average concentrations of around 1.2×10^{20} cm^{-3}. While the RT samples were too resistive to measure, the HT samples demonstrated remarkable results, achieving a Si dopant activation efficiency of 82.1%. They also exhibited a high sheet electron concentration of 3.3×10^{15} cm^{-2} and excellent mobility of 92.8 cm^2/V·s at room temperature. Additionally, X-ray diffraction analysis revealed that high-temperature implantation minimized the formation of secondary Ga_2O_3 phases and reduced structural defects and lattice damage. These findings underscore the potential of high-temperature ion implantation for fabricating ultra-low-resistance, heavily doped Ga_2O_3 layers.

In this study, Fe-doped β-Ga_2O_3 substrates were implanted with Si^+ ions at 275 and 425 keV to create a 300 nm thick doping profile, verified by SRIM simulations. Post-implantation

annealing was performed at 970 °C and 1050 °C to activate the samples. Ohmic contacts were fabricated using a Ti/Au metal stack, with a 60 nm Ti layer followed by 150 nm Au, and post-deposition annealing was conducted in a high-vacuum chamber at 450 °C for 1 minute. Samples annealed at 970 °C exhibited a linear I-V response between -0.2 V and +0.2 V, confirming the formation of ohmic contacts, while samples annealed at 1050 °C appeared more resistive. Schottky barrier diodes were also fabricated on in-situ Si-doped samples, showing a rectification ratio of 10^5 and a turn-on voltage near 1 V. C-V measurements indicated a carrier concentration of 1.9×10^{17} cm^{-3}, closely aligning with the target doping level of 2×10^{17} cm^{-3}.

This study investigates high-temperature (HT) Germanium (Ge) ion implantation to understand its impact on the structural morphology of β-Ga_2O_3. While prior work on Si ion implantation at 600 °C showed reduced lattice deformation compared to room temperature implantation, the influence of implantation-induced defects on material conductivity remains underexplored. Ge was implanted into Fe-doped β-Ga_2O_3 substrates with (010) orientation at room temperature and 600 °C using a dose of 1.5×10^{15} ions/cm^2. HRXRD analysis revealed that HT implantation resulted in less crystal deformation than room-temperature implantation. STEM analysis further identified dislocations at the interface of the MBE-grown β-Ga_2O_3 film and substrate, as well as within the film itself. Additional studies are necessary to fully characterize these dislocations and their effects on material properties.

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Chapter 1

Introduction

1.1 Wide Band Gap Semiconductor

Power electronics play a crucial role in all aspects of electrical energy, including electricity generation, storage, transmission, conversion, and consumption. Their influence spans daily life, powering devices ranging from mobile phones to high-speed computing and renewable energy systems. Current semiconductor research focuses on developing new materials and device designs to support high-power and high-speed electronics, which operate across a broad range of voltages and currents (see Fig. 1). Consumer electronics, such as mobile phones, laptop chargers and lighting typically operate at low voltages (<650 V). Mid-voltage devices (650–1700 V) are used in applications like electric vehicles, robotics, and motor drives, while high-voltage devices (>1700 V) power electric trains, and renewable energy grids, including photovoltaic inverters and wind turbines ([8],[1]).

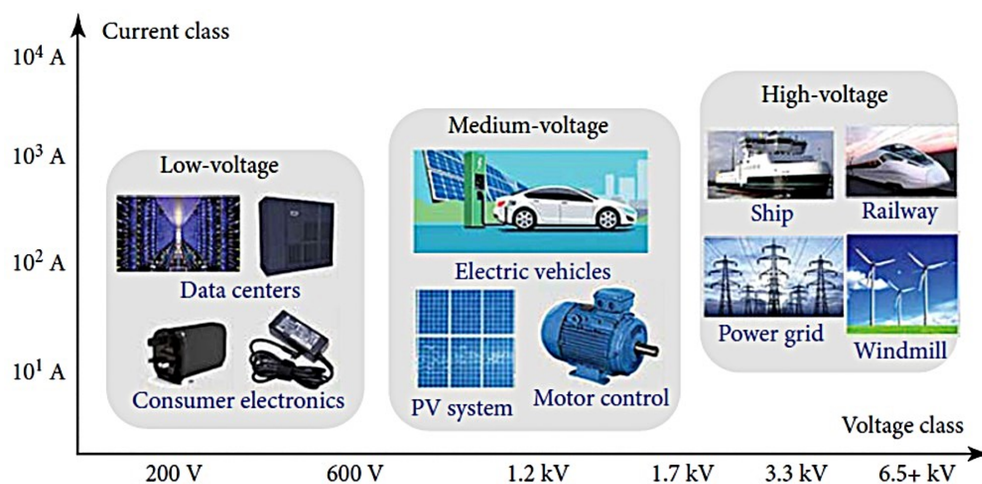


Figure 1.1: Power electronics applications at different current and voltage ranges [1].

High-power electronics today predominantly rely on silicon (Si), which experiences significant energy loss in high-voltage applications. To enhance power device performance and efficiency, researchers are exploring alternative materials to replace silicon. Wide-bandgap (WBG) and ultrawide-bandgap (UWBG) semiconductors have gained sustained interest, particularly for mid- to high-voltage applications, where silicon falls short due to its inherent material limitations. An ideal power device should make a transition instantly between the on-state and off-state with no power dissipation or switching time, as illustrated in Figure 2(a) ([9]). In practical power switches, however, a finite conduction loss occurs due to the voltage drop V_{ON} when the device is on. From the specific on-state resistance (R_{ON-SP}) the resistive loss in the on state can be obtained. The voltage at which the device undergoes catastrophic failure is referred to as the breakdown voltage (V_B) (Figure 2(b)).

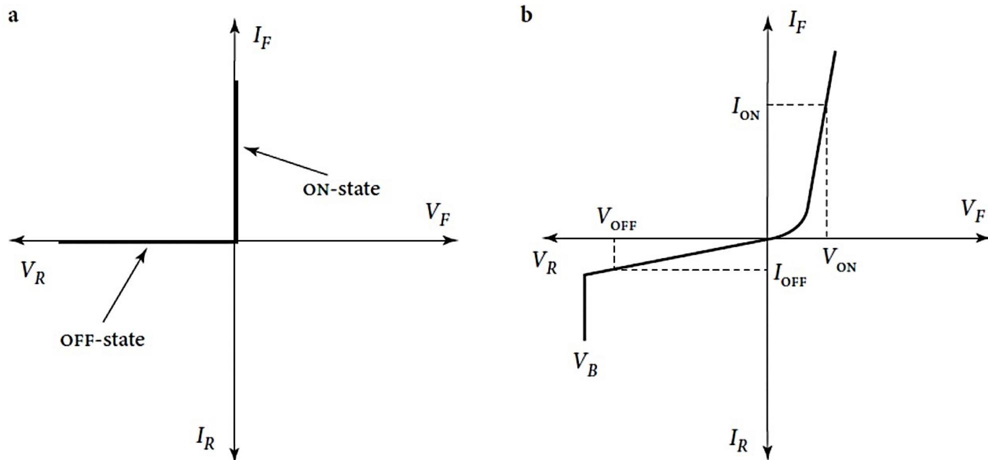


Figure 1.2: Current-voltage characteristics of (a) ideal and (b) practical power diodes [3].

Over the last two decades, significant developments have been made by WBG semiconductors, particularly silicon carbide (SiC) and gallium nitride (GaN), in the power electronics applications owing to their better electrical and thermal properties than Si([1],[8]). Recently, researchers are working on UWBG semiconductors in order to improve power electronics that can perform beyond the performance limit of GaN and SiC. The breakdown field of a semiconductor scales approximately as,

$$E_B \propto E_g^{3/2} \tag{1.1}$$

and the Baliga's figure-of-merit (BFoM), which is also known as power electronic figure-of-merit, indicates a semiconductor's potential for use in power electronics applications. The BFoM scales as the third power of the breakdown field ([1],[9]).Therefore, UWBG semiconductors are required to realize high power and high voltage devices that go beyond the capabilities of GaN and SiC-based devices.

1.2 Gallium Oxide (β-Ga_2O_3) Physical Properties

Beta Gallium Oxide (β-Ga_2O_3) is emerging as a promising wide bandgap semiconductor material and is attracting significant attention from the research community for power electronic applications ([10],[11],[12]). It has five different polymorphs i.e. α (corundum), β (monoclinic), γ (defective spinel), δ (orthorhombic), ϵ (hexagonal), among which β is the most stable polymorph upto it's melting point 1800 °C. Other polymorphs are metastable and transform into most stable β phase within 950 °C, so melt growth methods for these phases are difficult ([1]). The material has robust chemical resistance and radiation hardness, making it attractive for the devices operating in harsh environments ([13]).

Despite some advancements, the development of β-Ga_2O_3 and its devices significantly lags those based on SiC and GaN. Achieving successful engineering of β-Ga_2O_3 devices requires a comprehensive understanding and precise control of defects and doping in the material. Intrinsic and extrinsic defects are present in all materials, irrespective of the growth method employed. To modulate electrical properties, dopants and impurities are introduced, although the defects can sometimes negatively impact device performance. For instance, recombination centers formed by defects can limit doping levels by reducing carrier concentrations. Deep-level defects that are not thermally ionizable to generate free carriers often function as recombination centers. Such defects, however, are beneficial for creating semi-insulating materials, which are valuable for device fabrication.

1.2.1 Crystal Structure

The unit cell of β-Ga_2O_3, illustrated in Figure 1.8, features a base-centered monoclinic crystal structure with space group 12 (C2/m) and lattice parameters a = 12.23 Å, b = 3.04 Å, c = 5.8 Å, $\alpha = \gamma = 90°$and $\beta = 103.7°$[14]. It consists of two types of gallium ions: Ga(1) in tetrahedral geometry and Ga(2) in octahedral geometry, along with three types of oxygen ions with O(1) and O(2) being threefold coordinated, while O(3) is fourfold coordinated ([14],[15]). Research and development efforts employ β-Ga_2O_3 crystals or wafers with orientations such as ($\bar{2}01$), (010), and (001); however, commercially available wafers are limited to (010) and ($\bar{2}01$). The crystal planes of β-Ga_2O_3 are regarded as non-polar surfaces, though the presence of two distinct gallium ions and three oxygen ions can lead to different types of non-polar terminations, resulting in varied physical, optical, and electrical properties ([11],[16],[17]). For example, the thermal conductivity of β-Ga_2O_3 exhibits strong anisotropy, with the (010) direction reaching a maximum value of 29 W/$(m.k)$, approximately 2.5 times higher than the 13 W/$(m.k)$ measured in the [100] direction ([18],[19]). Both theoretical and experimental studies suggest minimal anisotropy in electron effective mass, yet dopants like Sn and Fe reduce thermal conductivity compared to undoped samples due to enhanced phonon-impurity scattering [11].

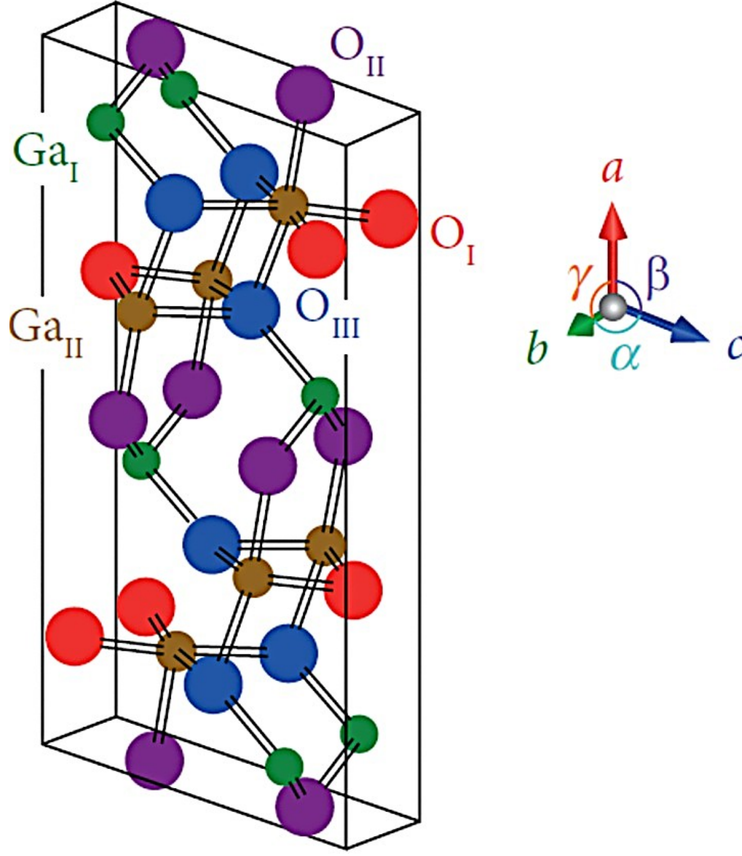


Figure 1.3: Unit cell structure of β-Ga_2O_3 with two types of gallium ions (Ga(1) and Ga(2)) and three types of oxygen ions (O(1), O(2), O(3)) ([2]).

1.2.2 Band Structure

Fig. 2 shows the band structure calculated from Density Functional Theory (DFT). The band structure of β-Ga_2O_3 shows the conduction band minimum (CBM) located at the Γ point, while the valence band maximum (VBM) is nearly at the same energy at both the Γ and M points, with the M point being marginally higher in energy by approximately 0.03–0.04 eV ([15],[20]). The conduction band of β-Ga_2O_3 originates predominantly from Ga 4s orbitals, with the conduction band minimum at the Γ point exhibiting a nearly parabolic shape. The electron effective mass, based on density of states (DOS) calculations, lies between $0.28m_0$ [3] and $0.34m_0$ [14]. In contrast, the valence band is primarily derived from localized O 2p orbitals, characterized by minimal dispersion and a substantial hole

effective mass, calculated as $40m_0$ [3] based on DOS. This high hole effective mass leads to limited hole mobility and supports the formation of localized holes, or small polarons, due to local lattice distortions, presenting a major challenge for achieving p-type doping in Ga_2O_3 ([21],[22]). The valence band maximum (VBM) is located just off the M point, 0.04 eV higher than at Γ [3]. The direct bandgap at the Γ point is 4.87 eV, only slightly larger than the indirect bandgap of 4.83 eV, making β-Ga_2O_3 effectively a direct bandgap material due to the significantly stronger dipole-allowed transitions at the Γ point [3]. Consequently, the Γ point is often referred to as the VBM [23].

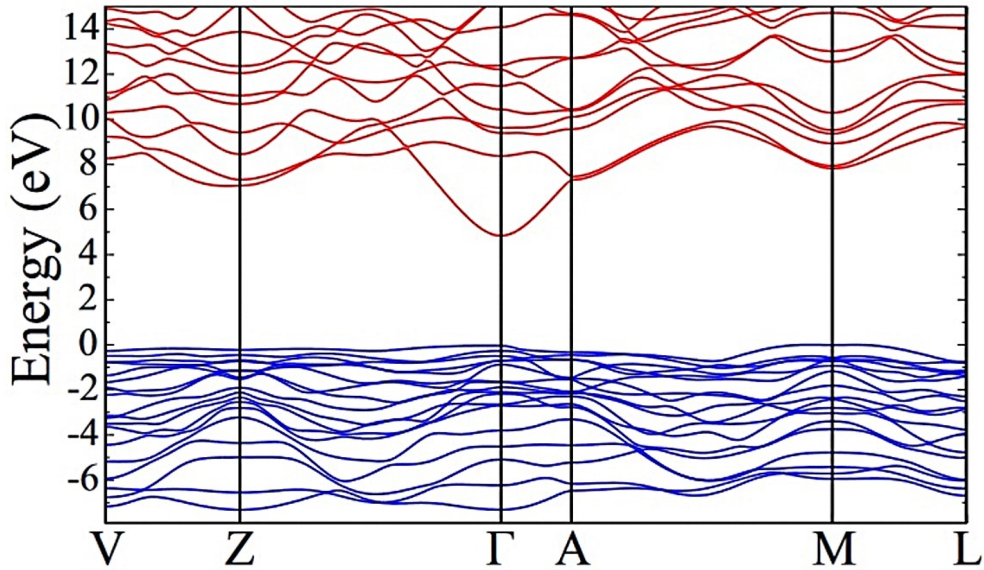


Figure 1.4: Band structure of β-Ga_2O_3 ([3]).

1.3 Bulk Growth of β-Ga_2O_3

The accessibility of affordable native wafers manufactured from melt-grown bulk single crystals provides β-Ga_2O_3 a significant advantage over SiC and GaN in terms of wafer size, crystal quality, and production cost. SiC bulk crystals are primarily grown by physical vapor transport at high temperatures (>2000 °C) with very low growth rates, while GaN bulk crystals are grown using expensive and low-yield methods like hydride vapor phase epitaxy

(HVPE), the sodium flux method etc. On the other hand, β-Ga_2O_3 can be grown from liquid-phase by common techniques, such as floating-zone (FZ) [24], Czochralski (CZ) method ([25],[26]), Bridgman method [27] and an edge defined film-fed (EFG) method ([24],[28]) that results in high-quality, yielding large-size, and potentially cost effective crystals. Some of the methods like the CZ, FZ, and EFG methods are discussed below in brief.

1.3.1 Floating Zone Method

The FZ growth process is known for its crucible free technique. The schematic diagram of this methos is shown in fig. 3. A seed crystal rod made of β-Ga_2O_3 single crystal is prepared and set in the lower part of the growth chamber, while the feed rod is suspended from the upper part using a platinum wire. Both rods are counter-rotated, with speeds up to 20 rpm, and enclosed in a cylindrical quartz tube. Infrared light or heating coils focus heat on the tip of the feed rod to melt it, and the melted tip is brought into contact with the seed crystal. Crystal growth occurs as the melting region is moved by adjusting the focal point or heating zone. The growth rate typically ranges from 5 to 10 mm/h, with a gas mixture of O_2 and N_2 used as the growth environment [4]. Impurities are swept to the end of the crystal during the process, making this method suitable for purification as well.

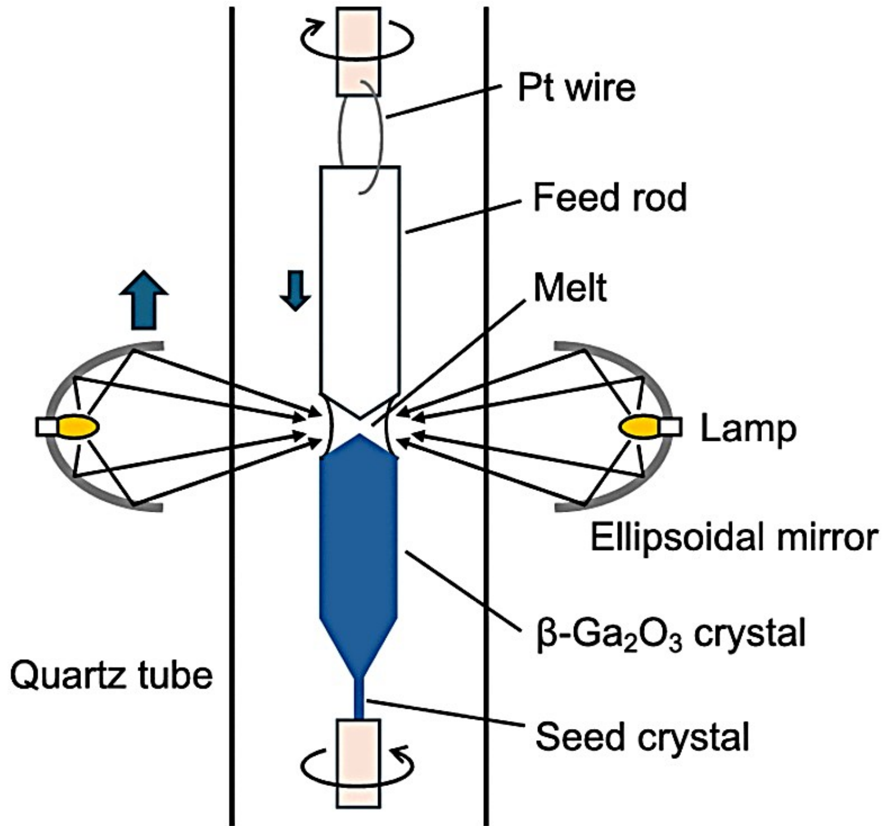


Figure 1.5: Schematic of FZ method ([4]).

1.3.2 Czochralski Method

The CZ method is highly appealing due to its demonstrated ability to produce high-quality, large-diameter single crystals. Figure 4 illustrates a schematic of the Czochralski (Cz) method, a fast growth technique for semiconductors commonly used in optoelectronic applications. In the Cz method, a rotating crystal, typically spinning at 5–20 rpm, is slowly pulled upward at a rate of 1–3 mm/h from the melt surface contained within a metal crucible [29]. For β-Ga_2O_3, an iridium (Ir) crucible is used due to the high melting point (1800 °C). The raw material, or charge, is placed in the Ir crucible and heated above its melting point using an RF coil arranged around the crucible. A seed crystal with the desired orientation is attached to the end of a spinning rod and lowered to contact the melt surface. As the seed crystal begins to melt, it is gradually pulled upward, allowing the crystal to grow [4]. The

desired diameter is achieved by carefully adjusting the melt temperature. Once the crystal reaches the intended size, the boule is either cut off or the melt temperature is increased to reduce the diameter to zero. However, the use of an Ir crucible may lead to the unintentional incorporation of Ir impurities into the crystal.

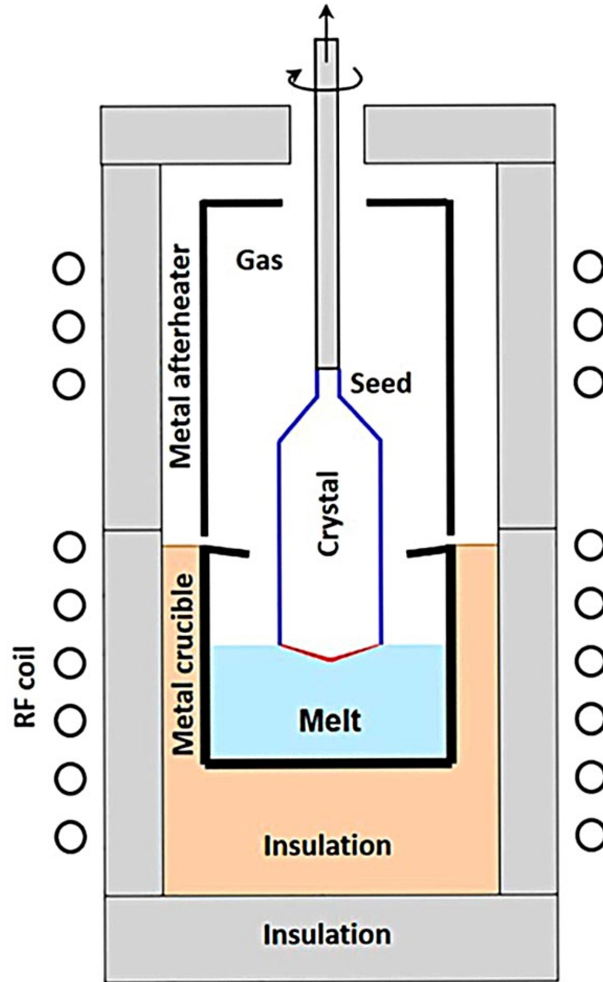


Figure 1.6: Schematic of CZ method [4].

1.3.3 Edge-Defined Film-Fed Growth Method

Among the other growth methods EFG by far is the most prominent and well-established melt growth technique utilized by current commercial suppliers of β-Ga_2O_3 single crystals. In this method, the source powder is placed in an Ir crucible along with an Ir die, and the growth process occurs at atmospheric pressure in a gas mixture of 98% nitrogen and 2%

oxygen. Heating is performed using a radio-frequency (RF) induction coil, and when the temperature reaches the melting point of β-Ga_2O_3, the melt rises through a slit in the Ir die via capillary action, reaching the die's top surface [24]. Crystal growth begins by placing a β-Ga_2O_3 seed crystal in contact with the melt on the die's top surface, where the crystal subsequently grows. To minimize evaporation effects from the melt, an Ir lid covers the melt around the die. The typical growth rate for this process is 10–15 mm/h ([24],[28]).

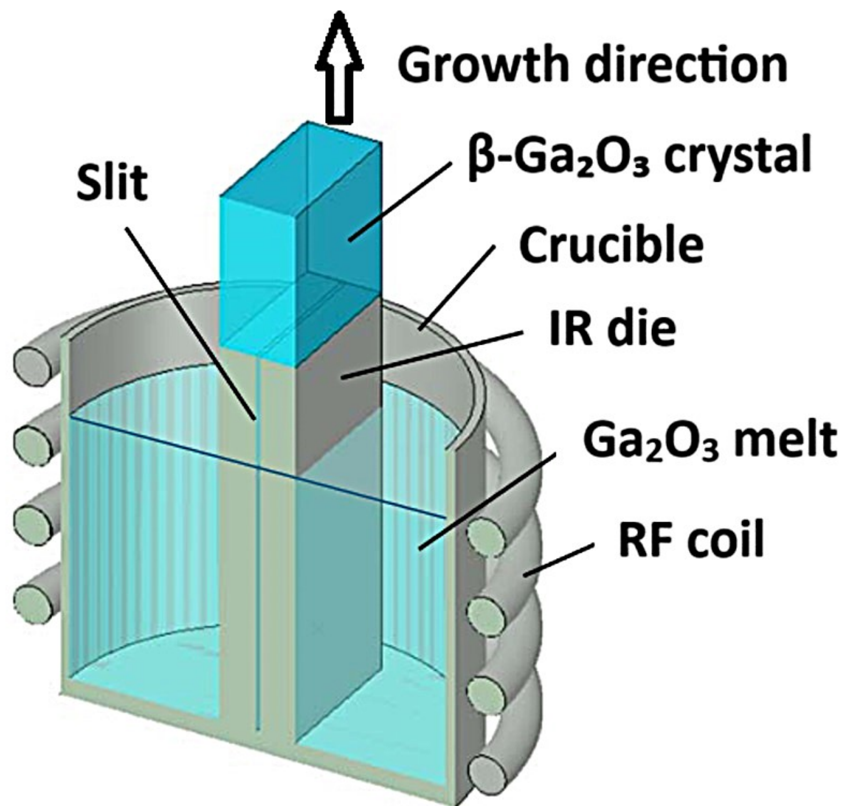


Figure 1.7: Schematic of EFG growth method.

1.4 Molecular Beam Epitaxy (MBE)

For producing materials with exceptional structural, optical, and electrical characteristics, Molecular Beam Epitaxy (MBE) has proved to be one of the most effective methods. Due to the remarkable ability to create extremely pure and defect-free epilayers, this technique has been extensively researched and potentially commercialized for depositing β-Ga_2O_3

thin films. According to the procedure two key reactions happen during the process. Initially, gallium atoms at the surface undergo oxidation, forming volatile gallium suboxides (Ga_2O). the process is followed by these suboxides either removing from the surface through evaporation or undergoing further oxidation to form Ga_2O_3, contributing to the development of the growing oxide layer. Different factors that play a crucial role in the process are O/Ga flux ratio, substrate orientation, and growth temperature. Using MBE-grown Ga_2O_3 film, researchers fabricated different types of devices like photodetectors, Schottky diodes, and MOSFETs. Ozone-assisted molecular beam epitaxy (ozone MBE) enables the investigation of how surface orientation influences film quality while also providing flexibility in exploring different doping strategies.

Different growth conditions affects the properties of the β-Ga_2O_3 film: morphology, growth temperature, growth rate and thermal conductivity. Morphology plays an important role in device fabrication. Morphology was affected by many growth parameters, and lots of work has been performed to investigate by changing different parameters. Growth temperature has a crucial role to play in the growth process in attaining the preferred crystalline quality and structural integrity. Trong et al. investigated the effects of growth conditions on the growth behavior and crystal properties of Ga_2O_3 films [30]. The root mean square (RMS) roughness of the Ga_2O_3 films increased with substrate temperature up to 650 °C. However, as the temperature continued to rise beyond this point, the RMS roughness decreased. This trend indicates a strong dependence of both surface morphology and roughness on the growth temperature.

The morphology of the final film is controlled by Ga flux which in turn affects the growth rate of the film. The flux can be controlled by providing various Ga-effusion cell temperatures. Takeki et al. studied the dependence of the growth rate on Ga flux and from the study two distinct growth regimes were observed: a Ga-flux-dependent linear increase in growth rate under O-rich conditions, followed by a saturation plateau at higher Ga flux levels [31]. The low thermal conductivity of Ga_2O_3, i.e. 26 W/(m·K) along the (010) direction,

limits its performance in power applications [19], prompting efforts to grow it on high-conductivity substrates like 4H-SiC [32]. MBE-grown β-Ga_2O_3 films on SiC showed slightly improved thermal conductivity compared to those on sapphire, with values influenced by growth methods due to defect-related phonon scattering. A polycrystalline SiO_x interfacial layer was also observed at the Ga_2O_3/SiC interface, unlike in Ga_2O_3/sapphire [33].

1.5 Doping

Successful implementation of β-Ga_2O_3 in power devices requires precise control over doping to achieve the target performance. Dopant incorporation during growth of the materials is known as in-situ doping which has been demonstrated using various growth techniques like Molecular Beam Epitaxy (MBE) ([2],[13],[34]) , Metal-Organic Vapor Phase epitaxy (MOVPE) [35], Pulsed Laser Deposition (PLD) [36] etc. Ion implantation is another powerful, well-established method for device processing since it offers a way to selectively dope different regions of a material with precise control of dose and doping profile. When energetic ions penetrate through a substance, the energy gets transferred to electrons and nuclei of the target. When the transferred energy from the incident ions to atomic nucleus exceeds the threshold value it creates a recoil atom and a vacancy which in turn can produce additional recoils and vacancies [8]. These collisions induce defects and structural damage are the concern for the practicality of ion implantation. Previous studies have shown that even after thermal annealing the damage was not recovered completely ([35],[37],[38]). Further study needed to understand implantation-induced damage and remaining defects after thermal annealing for better optimization of ion implantation to achieve desired electrical properties, it is crucial to have fundamental understanding of the defects and structural damage caused by ion implantation.

Structural damage and recovery due to Sn ion implantation in β-Ga_2O_3 films were investigated using Scanning Transmission Electron Microscopy (STEM) and X-ray Diffraction (XRD) by Yoo et al. [38]. High density of the defect phase and phase change from β to

γ was observed due to implantation. Increased XRD rocking curve full-width half maxima were another indication of deterioration of the crystal quality. Although high-temperature rapid thermal annealing showed partial recovery of β from γ phase, the presence of nano-sized voids depicts the presence of remaining structural defects at different locations in the material [31]. On the other hand, Ge implantation results in β phase to change into κ phase has been reported by Anber et al. [35], although the samples in ref. 31 had different plane orientations compared to ref. 28. Complete recovery of the crystal structure was not obtained in both cases. Another study by Tadjer et al. showed similar results about structural damage and remanent strain in β-Ga_2O_3 due to room temperature ion implantation of Sn and Si [37]. The presence of damage even after high temperature annealing was observed by XRD and TEM. The effect of annealing temperature was extensively studied by different groups. Sharma et al. have observed significant dopant diffusion (Si, Ge, Sn) in β-Ga_2O_3 when the post-implantation anneals were performed in O_2 atmosphere, in contrary to anneal the samples in N_2 ambient [39] where dopant diffusion was suppressed. This suppression can be attributed to the influence of Ga vacancies [38].

Wong et al. [40] investigated the diffusion characteristics of implanted acceptor impurities, specifically nitrogen (N_2) and magnesium (Mg). In their study, the peak concentration of Mg in the implanted samples reached approximately 10^{19} cm^{-3}, while N_2 was around 10^{18} cm^{-3}. Following implantation, annealing was performed, revealing that Mg redistribution began at an annealing temperature of 900 °C. In contrast, significant N_2 redistribution was only observed at a much higher of 1100 °C. This finding is noteworthy because it indicates that, for N_2 doping, the annealing temperature can be raised to enhance dopant activation.

In another study, Tetzner et al. [41] implanted nitrogen ions into epitaxial β-Ga_2O_3 layers to generate a boxlike profile with a concentration of 10^{21} cm^{-3}. From Hall effect measurement, the formation of the semi-insulating layer was observed, and the resistivity remained unchanged up to 600 °C annealing temperature. An increase in temperature to

800 °C caused the recovery of conductivity almost to its original level which indicates the compensation of conductivity was caused by the radiation defects.

The implantation of rare earth elements (Eu, Er, Gd) and transition metals has been primarily investigated for their luminescence properties. The study by Peres et al. [42] examined how implantation and post-implantation annealing temperatures influence the Eu^{3+} charge state and cathodoluminescence properties in β-Ga_2O_3. The findings emphasized that radiation-induced defects significantly affect both the luminescence characteristics and the stability of the Eu^{3+} charge state. Raman scattering and cathodoluminescence of β-Ga_2O_3 nanowires and bulk crystals implanted with Cr^+ and Mn^+ (E = 150 keV, D = 10^{15} cm^{-2}) were analyzed, revealing structural improvement during rapid thermal annealing between 700 °C and 1000 °C. Cr-related cathodoluminescence correlated with structural improvement in both nanowires and bulk samples, while Mn^+ implantation exhibited different behavior, with the underlying physical reasons still unclear [43].

Another category of implanted impurities are light gas ions, among which hydrogen (H) is the most important one. Interest in hydrogen impurities grew after a report claimed successful fabrication of low-resistive p-type β-Ga_2O_3 through diffusion [44]. Deuterium, an isotope of hydrogen, is preferred for studying H diffusion due to its easier detectability. The diffusion of implanted deuterium in β-Ga_2O_3 ($\bar{2}01$) was analyzed using SIMS before and after isochronous annealing (5 min) at 450–650 °C. Comparing this with plasma doping revealed the role of radiation defects, such as vacancies, in trapping hydrogen during diffusion [45]. The formation of bubbles in β-Ga_2O_3 (010) due to He^+ ion implantation (E = 160 keV, D = 5×10^{16} cm^{-2}), followed by annealing at 200 °C and 500 °C, was investigated using XRD, TEM, and AFM. Blistering and crack formation were identified as key processes leading to the exfoliation of the implanted Ga_2O_3 layer [46].

Although significant improvement has been made, further investigation is needed to fully understand the mechanism behind doping with ion implantation in β-Ga_2O_3. A key area of focus could be the interaction between implanted impurities and native defects,

and their impact on electrical and optical properties. Additionally, to optimizing material performance in practical applications systematic studies on the influence of growth techniques on implantation outcomes will be essential.

Chapter 2

Experimental Techniques

2.1 Standard device fabrication procedure

The β-Ga_2O_3 (010) and β-Ga_2O_3 ($\bar{2}01$) wafers used in this study for ion implantation, Hall measurements, and TLM fabrication were sourced from the Air Force Research Laboratory (AFRL) and Tamura Corporation, respectively. The β-Ga_2O_3 (010) wafers obtained from AFRL featured a molecular beam epitaxy (MBE)-grown thin film layer deposited on a β-Ga_2O_3 substrate, both having the same crystallographic orientation. The thin film layer was doped with silicon (Si) to achieve a carrier concentration of approximately 2×10^{16} cm^{-3}, which was significantly lower—by nearly four orders of magnitude—than the ion implant concentration employed in this work. In contrast, the β-Ga_2O_3 (-201) wafers obtained from Tamura Corporation consisted of a substrate doped with tin (Sn) to achieve a doping concentration of approximately 5.9×10^{18} cm^{-3}. These wafers provided the required material properties for TLM fabrication. Both types of wafers initially came in 2-inch diameters but were diced into smaller 5 mm $\times$ 5 mm pieces to facilitate device fabrication and subsequent processing. These diced samples served as the building block for implementing the designed experiments and fabricating the semiconductor devices explored in this study.

2.1.1 Standard sample cleaning and capping layer removal procedures

Prior to annealing after implantation and before undergoing device fabrication the samples were subjected to both organic and Piranha cleaning procedures. Organic cleaning was performed to eliminate any organic contaminants from the sample surfaces, while Piranha cleaning effectively removed ionic and heavy metallic impurities. Prior to depositing the capping layer Molybdenum/Aluminum Oxide (Mo/Al_2O_3) used during the ion implantation

process, the samples were first treated with organic cleaning to ensure a pristine surface. After implantation, the capping layer was carefully removed using specific cleaning methods before proceeding with annealing. The detailed steps involved in organic cleaning, Piranha cleaning, and the removal of capping layers are outlined below.

Organic Cleaning:

1. Immersed in acetone and sonicated in an ultrasonic bath for 5 minutes.
2. Immersed in trichloroethylene (TCE) and sonicated in an ultrasonic bath for 5 minutes.
3. Immersed in acetone and sonicated in an ultrasonic bath for 5 minutes.
4. Immersed in methanol and sonicated in an ultrasonic bath for 5 minutes.
5. Immersed in fresh methanol and sonicated in an ultrasonic bath for 5 minutes.
6. Rinsed in de-ionized water (DI water) for 5 minutes.
7. Dried with N_2 gas.

Piranha Cleaning:

1. After completing the organic cleaning process, the samples were immersed in a Piranha solution. The Piranha solution consisted of a 1:1 mixture of sulfuric acid (H_2O_4) and hydrogen peroxide (H_2O_2).
2. The samples were soaked in the solution for 15 minutes and then rinsed with deionized (DI) water for 5 minutes.
3. Dried with N_2 gas.

Capping layer (Mo/Al_2O_3) removal:

1. Immersed in H_2O_2 for 5 minutes to remove Mo from the top of the surface.
2. Rinsed in de-ionized water (DI water) for 5 minutes.

3. Immersed in buffer oxide etch (BOE) for 10 minutes to remove Al_2O_3 layer.

4. Rinsed in de-ionized water (DI water) for 5 minutes.

5. Dried with N_2 gas.

After capping layers removal the samples went through organic clean and Piranha cleaning in order to get rid of any excess residue of the surface. These cleaning steps were essential to prepare the samples for subsequent annealing and device fabrication processes, ensuring optimal surface quality and minimizing the risk of defects during further processing.

2.2 Ion Implantation

To form low resistance regions such as source/drain contacts, emitters, and buried collectors, the samples were implanted at room temperature and high temperature (600 °C) using Auburn University 6SDH-2 Pelletron tandem accelerator shown in Fig. which provides with a wide energy range from 100 keV to 12 MeV. In this process ionized impurity atoms accelerated through an electrostatic field strike the surface of the wafer. Heavier ions like Silicon (Si), Germanium (Ge), Nitrogen (N), Aluminum (Al) are available from SNICS II (Source of Negative Ions by Cesium Sputtering). The accelerator is used for different analysis such as heavy ion implantation (HII), Rutherford backscattering spectroscopy (RBS), light ion channeling (LIC) etc.

Prior to ion implantation, a 20-30 nm thick Al_2O_3 layer was grown using Atomic Layer Deposition (ALD) method. A comparatively thicker layer of Mo was sputtered deposited on top of the oxide layer. The thickness of both oxide and Mo layer was determined by running Stopping and Range of Ions in Matter (SRIM) ([47]) simulation and was considered as capping layer. The capping layers were removed after implantation and prior to activation annealing to activate the implanted ions. H_2O_2 and Buffered oxide etch (BOE) were used to remove Mo and Al_2O_3 respectively. The capping layers served two purposes simultaneously, 1. to lower the speed of the implanted ions and keep the dopants close to the surface of

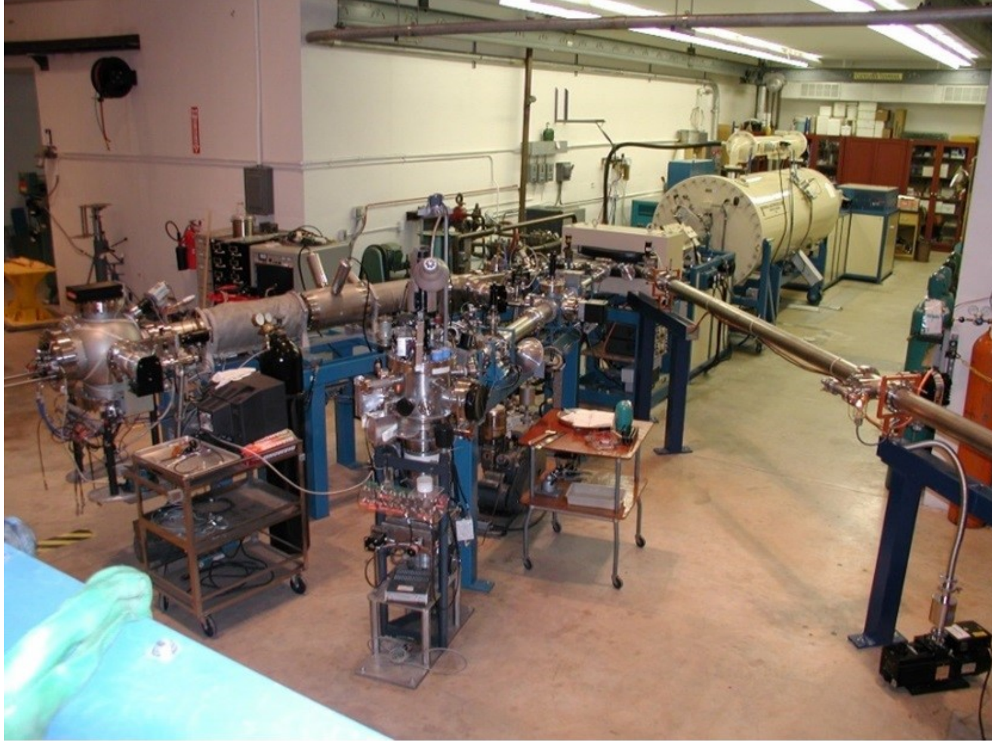


Figure 2.1: 6SDH-2 Pelletron tandem accelerator.

β-Ga_2O_3 and 2. to prevent any Mo knock-ons into β-Ga_2O_3. At the end both organic and piranha cleaning were performed on all the samples before further processing. A schematic of the ion implantation process flow has been shown in Figure 2.2.

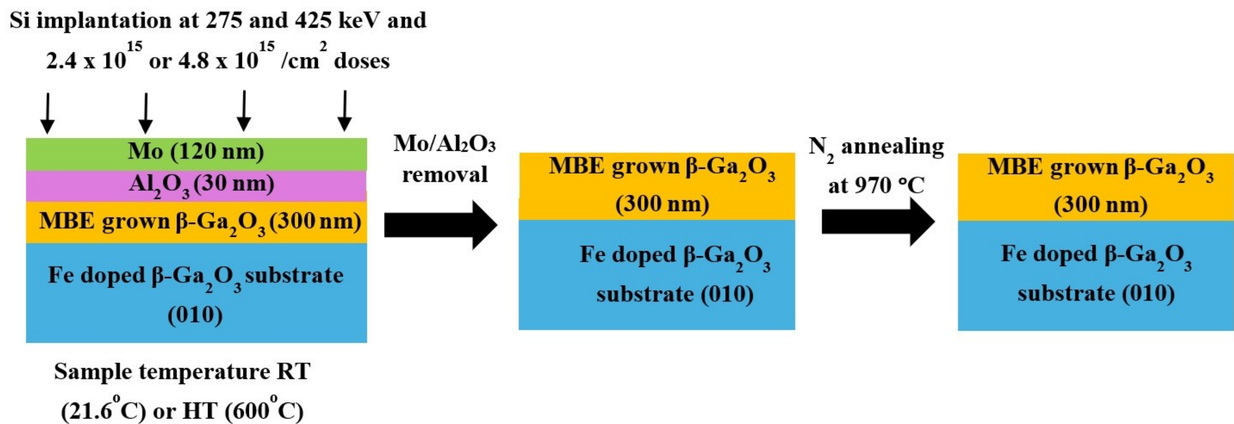


Figure 2.2: Schematic of ion implantation process flow.

Si and Ge were implanted at different energies and temperatures into 300 nm thick, unintentionally doped β-Ga_2O_3 films grown by molecular beam epitaxy (MBE) on top of

the Fe doped semi-insulating β-Ga_2O_3 substrate. For Si ion implantation, 275 and 425 keV energies were used with a targeted 300 nm box profile and total doses of 2.4x10^{15} or 4.8x10^{15} cm^{-2}. In case of Ge ion implantation the target dose and box profile were 1.5x10^{15} cm^{-2} and 350 nm. The implantation dose depends on the desired doping concentrations. The SRIM profile for both Si and Ge implantation has been shown in the figure.

2.3 Optical Photolithography

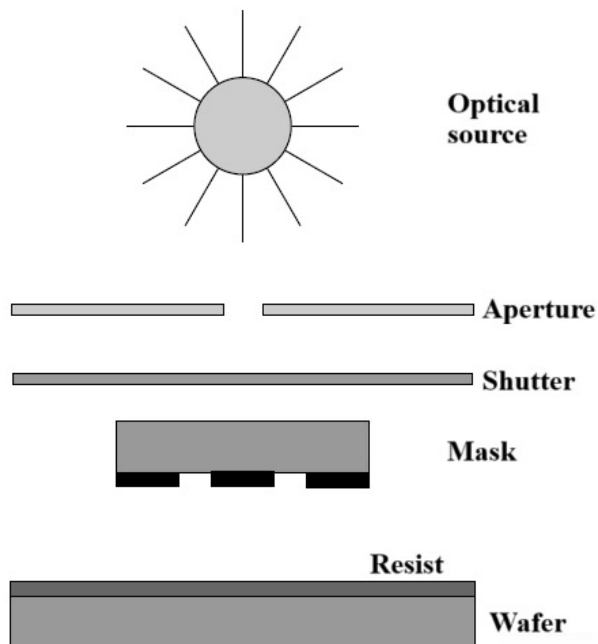


Figure 2.3: Schematic of lithographic exposure system.

In mainstream microelectronic fabrication optical photolithography is the most expensive complicated process [48]. An optical source positioned above directs light through the mask. This light creates a projection of the mask's image onto the wafer's surface, which is coated with a thin, photosensitive layer called photoresist. Optical photolithography consists of two primary components. The first involves the design and functionality of the exposure tool, which forms the photomask image on the wafer surface. The second aspect focuses on the chemical reactions triggered after the image's radiation is absorbed by the photoresist, leading to pattern development. A ray diagram of photolithography exposure system has

been shown in Figure 2.3. The requirement for an exceptionally clean environment and a highly flat surface are among the key limitations of this process.

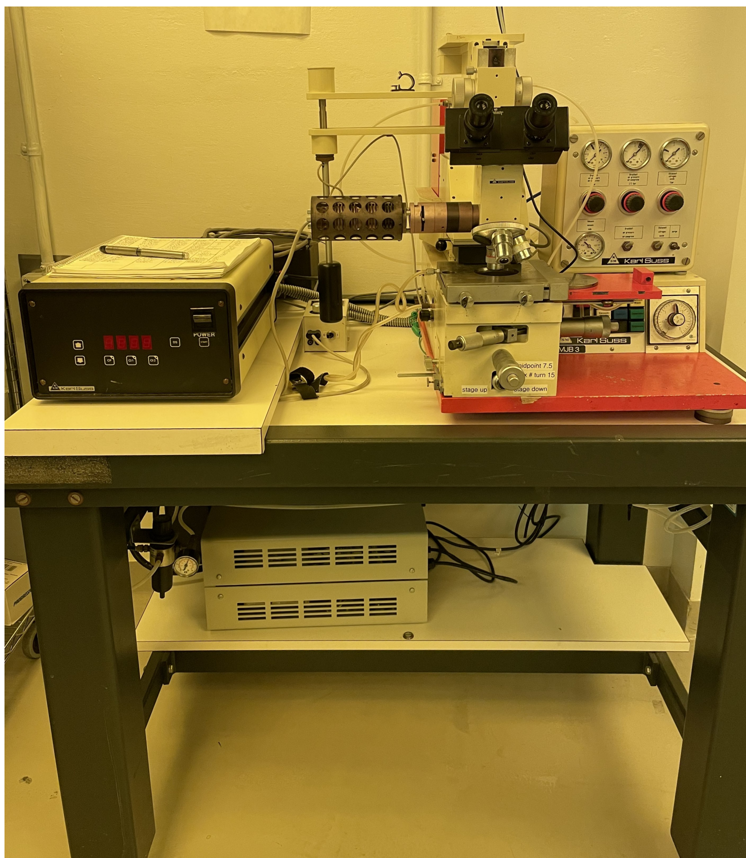


Figure 2.4: Karl Suss MJB3 UV400 mask aligner with an optical microscope.

A Karl Suss MJB3 UV400 mask aligner was used to make TLM, Van der Pauw Hall patterns and Schottky Barrier Diode (SBD). The aligner consists of an optical microscope having magnifications of 5, 10 and 20, and a UV light source having an output power of 160W. The performance of a mask aligner depends on three primary performance parameters, 1. resolution, defined as the minimum feature size that can be exposed (2-3 µm for this system); 2. registration, a measure of the overlay accuracy from layer to layer; and 3. throughput. The sample is held at the center of a 3 inch silicon wafer which is then covered with 2070 photo-resist by spin coating for 30s at a rotor speed of 7000 rpm., resulting a 1.5 µm thick photoresist on the sample. The photoresist-coated wafer is soft-baked for 90 sec at 110 °C in the oven, which dries the photoresist causing it to be more sensitive to UV light.

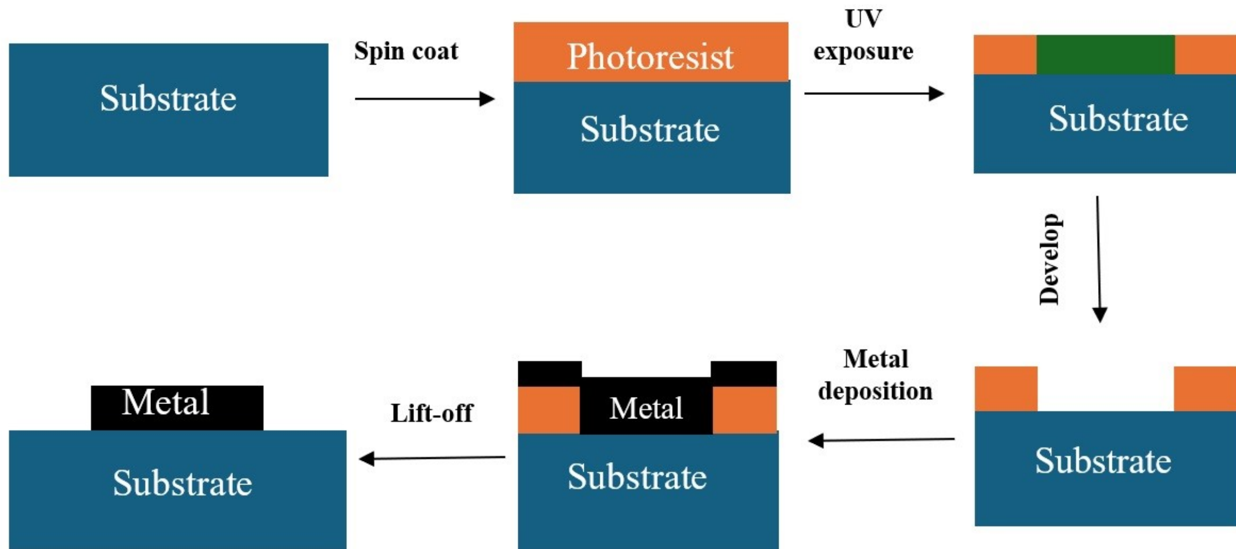


Figure 2.5: Flow diagram of the photolithography and Lift-off process.

The wafer was secured onto the mask aligner and positioned accurately with the sample holder by fine-tuning the X, Y, and θ coordinates. The samples underwent UV light exposure for 60 seconds, followed by a soft bake at 110 °C for 90 seconds in the oven. Maintaining proper baking conditions is critical to preserving the photoresist's sensitivity, as deviations can impair its performance. Baking initiates a cross-linking process in the photoresist, facilitating its dissolution during development. Following the soft bake, the samples were submerged in AZ 726 MIF developer for 45–50 seconds and then rinsed with deionized water for 1 minute. It is essential to employ the rinsing immediately after development to avoid overdeveloped patterns. The regions where the mask blocked UV light during exposure retained the photoresist, while the exposed areas were dissolved. If the pattern edges appear insufficiently sharp, additional development for a few more seconds may be performed.

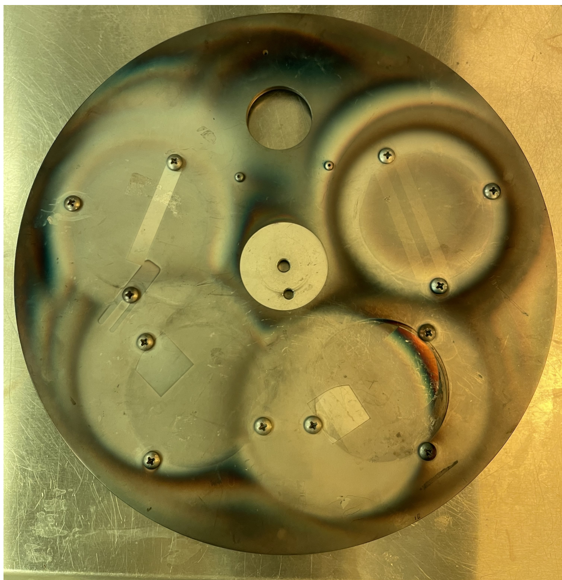
2.4 Metal Sputter deposition

In a sputtering system, most of the voltage drop occurs at the target electrode, but the substrate electrode bias causes ion bombardment on the wafer. This bombardment removes material from the wafer surface and can be regulated by adjusting the electrode's bias relative

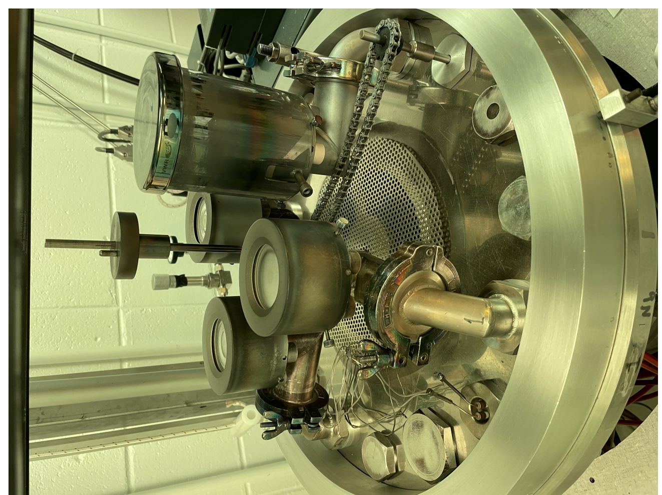
to the plasma [2]. In an inert gas such as Argon (Ar) atmosphere, plasma is created by the application of DC voltage between the two electrodes cathode, and anode in the sputter system. Positively charged ions (Ar^+) of the inert gas (Ar) are accelerated towards the target which is in a negative potential with respect to the plasma. Sputtering is typically performed in a vacuum or at low pressure to minimize gas-phase collisions between the target and substrate. In a magnetron setup, a magnet under the target generates a magnetic field parallel to its surface, increasing plasma intensity near the surface. This design allows DC magnetron sputtering to achieve a higher sputtering rate than conventional DC sputtering with parallel electrodes.

There are two types of available magnetron sputtering systems, 1. DC sputtering and 2. RF sputtering. The deposition rate is high in DC sputtering compared to the RF system. In DC sputtering electrically conductive materials are preferred where as in RF sputtering system has a variety of applications and is effective for both conductive and non-conductive materials. metal contact deposition was performed using a DC magnetron sputtering system with a maximum power capacity of 1000W. The system includes a vacuum chamber capable of reaching a high vacuum of 3×10^{-7} Torr, supported by a roughing pump and a turbopump, which can further achieve a vacuum of 10^{-8} Torr. It features four 2-inch diameter water-cooled magnetron sputtering guns with a cathode potential range of 200–1500V. These guns allow consecutive sputtering of different targets without breaking vacuum. Cylindrical glass chimneys are fitted on each gun to focus material deposition onto the substrate while minimizing cross-contamination.

(a)



(b)



(c)

Figure 2.6: (a) Sputter deposition system; (b) Sample holder disc; (c) Vacuum chamber.

The detailed process flow for sputtering is given below:

1. Turn off the ion gauge and close the high vacuum valve. Ensure the high vacuum partial valve is open.

2. Open the nitrogen gas valve on the wall and the gas intake on the vacuum system. Fill the chamber until the pressure reaches 790 Torr, then close the nitrogen gas supply.

3. Open the chamber, place photolithographically patterned samples on the sample holder, and replace the target and chimney as needed.

4. Close the chamber and slowly start the roughing pump until the pressure drops to 30 mTorr. Stop the roughing pump, open the fore-line valve, and gradually open the high vacuum valve.

5. Pump down the chamber to approximately 3×10^{-7} Torr, then turn off the ion gauge and close the turbo pump's partial valve.

6. Open the argon gas flow at 95 sccm to maintain a chamber pressure of 17 mTorr. Allow the turbo pump to stabilize and confirm the power and cool water supply for the target.

7. Turn on the power and gradually increase the voltage until plasma ignition occurs.

8. Adjust the voltage knob to sustain the desired current for different materials (e.g., Mo = 0.4 A, Ti = 0.25 A, Ni = 0.2 A).

9. Perform pre-sputtering for 2 minutes before proceeding with the actual sputtering process for the required duration.

10. Reduce the voltage, power off the system, and close the argon flow. Vent the chamber with N_2, remove the sample, clean the sputtering chamber, and pump it down to stabilize the system.

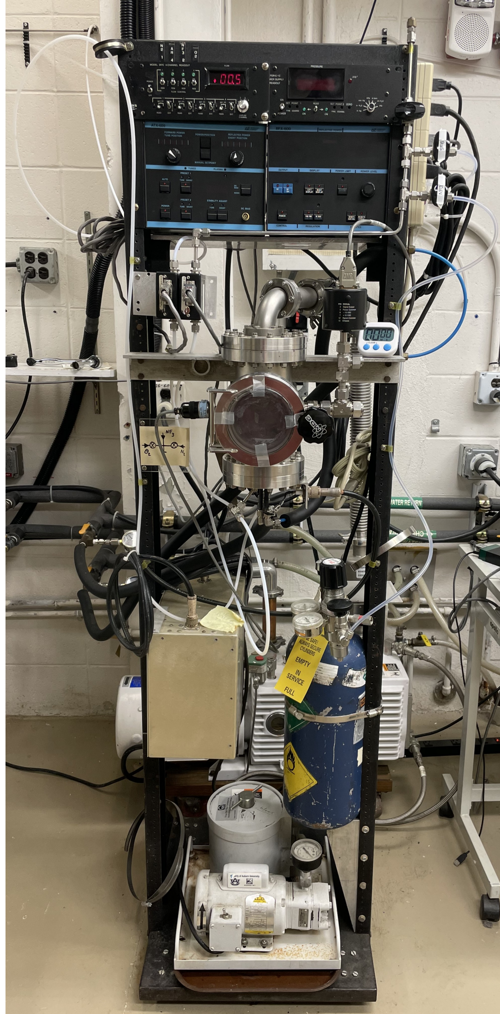
The sample holder plate, located about 15 cm above the sputter targets, could be mechanically rotated to enable sequential deposition of up to four different metals without venting the vacuum. Sputtering time was controlled based on the sputtering rate and the desired metal film thickness.

2.5 Lift-off

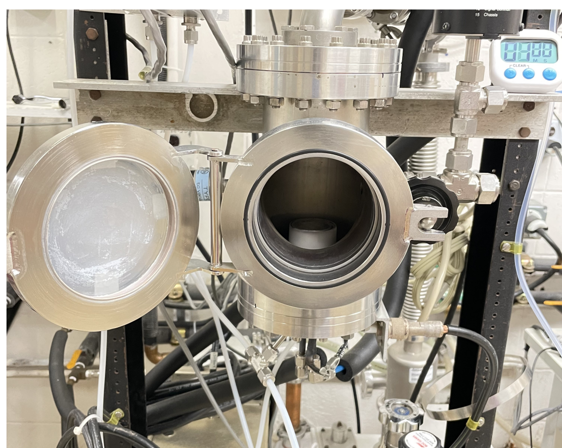
Lift-off is a crucial step in semiconductor device processing used to remove unwanted metal deposited on the substrate. The lift-off duration depends upon different factors such as, type of photoresist, prebake/post-bake time, UV exposure dose, and developer solvent. This process involves stripping the underlying photoresist, causing the deposited metal to detach when the resist dissolves in a solvent. In this research, wet chemical lift-off was carried out using acetone, followed by methanol and deionized water rinsing, effectively dissolving the photoresist and removing excess metal to create patterned metal contacts on the substrate. The lift-off process has been shown in the flow diagram of figure 2.4.

2.6 Reactive Ion Etching

The RIE system, depicted in Fig. 2.7(a), was utilized for defining Hall patterns and TLM strips in this study. The sample was mounted on a 2-inch silicon wafer, and placed on the cathode inside the vacuum chamber, as shown in Figure 2.7(b). The chamber maintains a base pressure of 9–12 mTorr, while the working pressure with plasma is 34–38 mTorr when nitrogen trifluoride (NF_3) gas is supplied. For β-Ga_2O_3, the etching rate is between 20-25 nm/min with a forward power of 60W and a reflected power of 2W. Nitrogen gas was used to vent the chamber.



(a)



(b)

Figure 2.7: (a) View of overall RIE system; (b) Vacuum chamber inside the RIE system.

The detailed process flow for RIE is given below:

1. 5 mm x 5 mm samples were attached to a 2-inch graphite plate using photoresist applied at the interface between the back of the sample and the plate.
2. The assembled samples were soft baked in an oven at 100°C for 5 minutes to secure attachment.
3. Open the glass window of the etcher system.
4. Position the wafer on the electrode, center it, and press it down gently with tweezers to ensure it is firmly in place. Close and seal the chamber.
5. Flow N_2 gas into the chamber for 1 minute to purge contaminants.
6. Start the vacuum pump and evacuate the chamber for 1 hour until the base pressure reaches approximately 10 mTorr.
7. Activate all valves connected to the etch gas line and switch on the flow controller. Adjust flow rates if necessary.
8. Allow the gas lines to flush for 5 minutes to clear out any residual gases.
9. Switch on the RF power supply unit and adjust the forward power to about 3 watts above the desired setting.
10. Turn on the RF power to initiate plasma generation.
11. Fine-tune the power setting and adjust the matching network to minimize reflected power.
12. Allow the etching process to run for the desired time duration.
13. Turn off the RF power and close the etchant gas supply. Pump down the chamber to return to base pressure.

14. Fill the chamber with nitrogen for 1 minute, then evacuate it. Repeat this step at least twice to remove any toxic residual gases.

15. Bring the chamber to atmospheric pressure using nitrogen, remove the wafer, perform a final nitrogen purge, and close all gas tanks. Turn off the vacuum pump if no further etching is required.

2.7 Annealing

The annealing system used for both high temperature implant activation and contact anneal has been shown in the figure 2.8(a). It was heated in a high temperature furnace where the temperature can go upto 1700 °C temperature. A thermocouple was used to monitor the temperature of the sample when it is heated in an Argon (Ar) or N_2 environment and the sample surface was faced upward. The sample was positioned on a glass paddle, and the paddle temperature, monitored by the thermocouple, was treated as the sample temperature. For implant activation annealing, the temperature ranged from 955–975 °C, while contact annealing was conducted between at 450 °C. The system achieved a vacuum pressure of 10^{-7} Torr after two hours of pumping.

In this work, Si and Ge implanted samples were activated at 970 °C temperature to activate the implanted dopants. All samples were activated with for 30 min in an ultra-high purity (UHP) N_2 atmosphere. For Si implantation, the samples were positioned on a silicon wafer placed on the glass paddle with the implanted surface facing upward during annealing. In contrast, Ge-implanted samples were directly placed on the glass paddle with the implanted surface facing upward. The glass paddle was connected to a thermocouple to monitor the temperature throughout the annealing process. After placing the samples, the chamber was vacuumed to a level of approximately 10^{-7} Torr. Following this, the pump was turned off, and UHP N_2 gas was introduced into the chamber. It took around 2 minutes for the paddle temperature to reach 950 °C, after which the timer was initiated. The paddle

(a)

(b)

Figure 2.8: (a) Annealing chamber; (b) Sample stage made of glass and thermocouple.

temperature varies between 950-975 °C. The samples were maintained at this temperature for 30 minutes to activate the dopants.

For contact activation annealing, samples with Titanium/Gold (Ti/Au) contacts were positioned inside the annealing chamber, and UHP N_2 was introduced for 1 minute at 450 °C. During annealing, the samples were placed on the glass paddle with the contacts facing

upward. The paddle temperature reached 450 °C in approximately 1 minute, after which the timer was started. The temperature was held at 450 °C for 1 minute.

2.8 Transfer Length Method (TLM) contacts

TLM patterns were fabricated on the samples through photolithography using TLM masks, as illustrated in figure 2.9. The process began with the preparation of the samples, followed by the deposition of metal contacts through DC magnetron sputtering. To begin the process, a photoresist layer was spin-coated onto the sample surface, and a mesa etch mask was applied to define the regions for etching. Following this, molybdenum (Mo) and nickel vanadium (NiV) layers were deposited using a sputtering system. These layers served as protective masks to shield the β-Ga_2O_3 surface areas intended for contact with the metal electrodes.

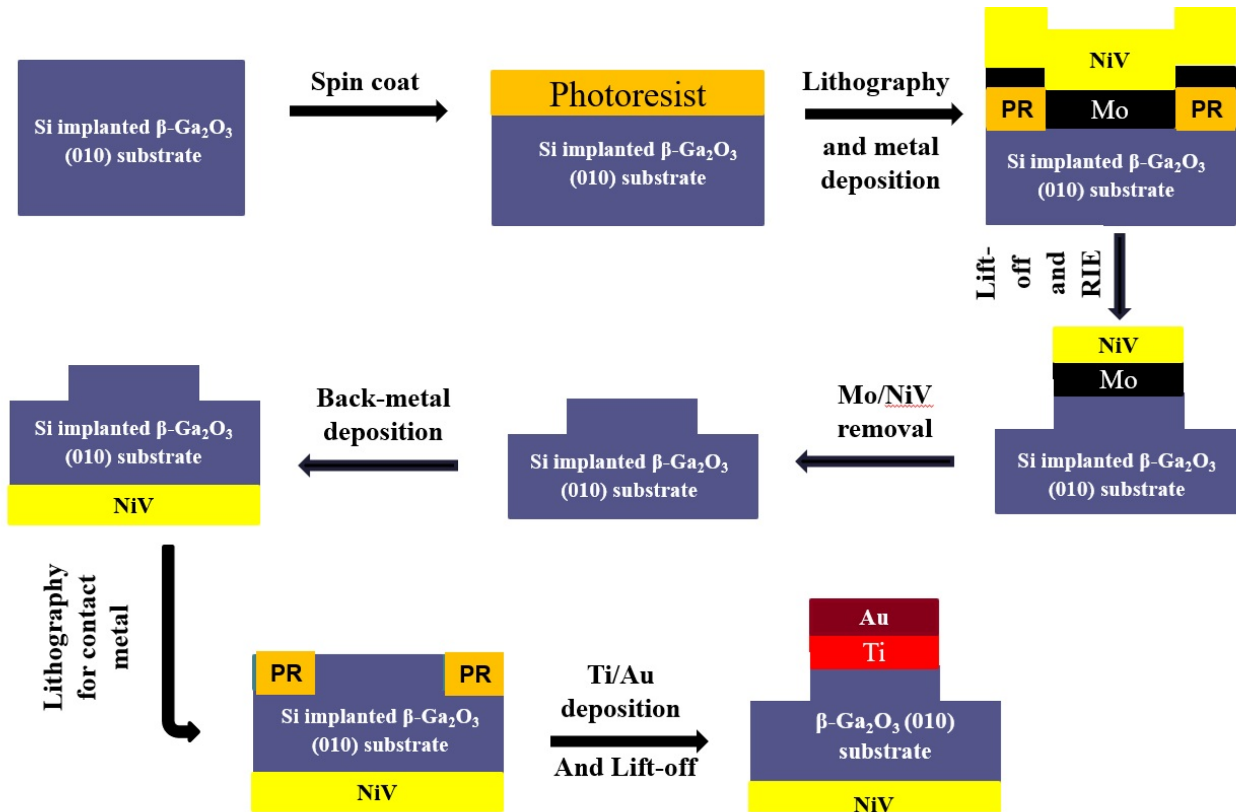


Figure 2.9: Flow diagram of TLM fabrication steps.

A lift-off process was then performed to remove excess material, ensuring precise patterning of the protective layers. In this experiment, titanium (Ti) and gold (Au) were selected as the contact metals due to their desirable electrical and adhesion properties. After the deposition of Mo and NiV, the samples were transferred to the RIE chamber for dry etching. The etching was carried out in a NF_3 plasma environment for 20 minutes, achieving an etch rate of approximately 20 nm/min, effectively removing around 400 nm of the β-Ga_2O_3 substrate. Once the etching process was complete, the Mo and NiV layers were stripped away using chemical treatments. First, the samples were immersed in a nickel etchant for 5 minutes to dissolve the NiV layer. Subsequently, they were treated with hydrogen peroxide H_2O_2 for an additional 5 minutes to remove the Mo layer. This sequence ensured complete removal of the protective masks, leaving the desired regions of the β-Ga_2O_3 surface exposed for further processing.

(a) (b)

Figure 2.10: (a) Mesa etch mask, (b) TLM mask.

A Ti layer approximately 60 nm thick was deposited to serve as an adhesion layer, ensuring strong bonding between the film and the subsequent metal layer. This was followed by the deposition of a 150 nm Au layer, which acted as the primary conductive material

for the contacts. After the metal deposition, the samples underwent an annealing process to improve the contact quality and activate the interfaces. Figure 7 showed the mesa etch and TLM mask used in the fabrication. The annealing was conducted in a high-vacuum chamber with a pressure of 10^{-7} Torr, filled with ultra-high purity (UHP) N_2 gas. The chamber temperature was ramped up to 450 °C, which was achieved within approximately one minute, and this temperature was maintained for an additional minute to complete the annealing process. This step ensured optimal electrical contact properties for the TLM patterns. The detailed sequence of the TLM fabrication steps is presented in figure 2.9.

2.9 Schottky Barrier Diode (SBD) fabrication

Schottky Barrier Diode (SBD) contacts were fabricated on the samples using photolithography with predefined masks, the process flow is illustrated in Figure 2.11. The fabrication process began with meticulous sample preparation to ensure a clean and uniform surface. Following the preparation, metal contacts were deposited through DC magnetron sputtering. To initiate the process, a negative photoresist was spin-coated onto a lightly silicon-doped β-Ga_2O_3 substrate, where the silicon doping concentration was approximately 2×10^{17} cm^{-3}. The coated samples then underwent photolithography to define the desired structures on the substrate surface.

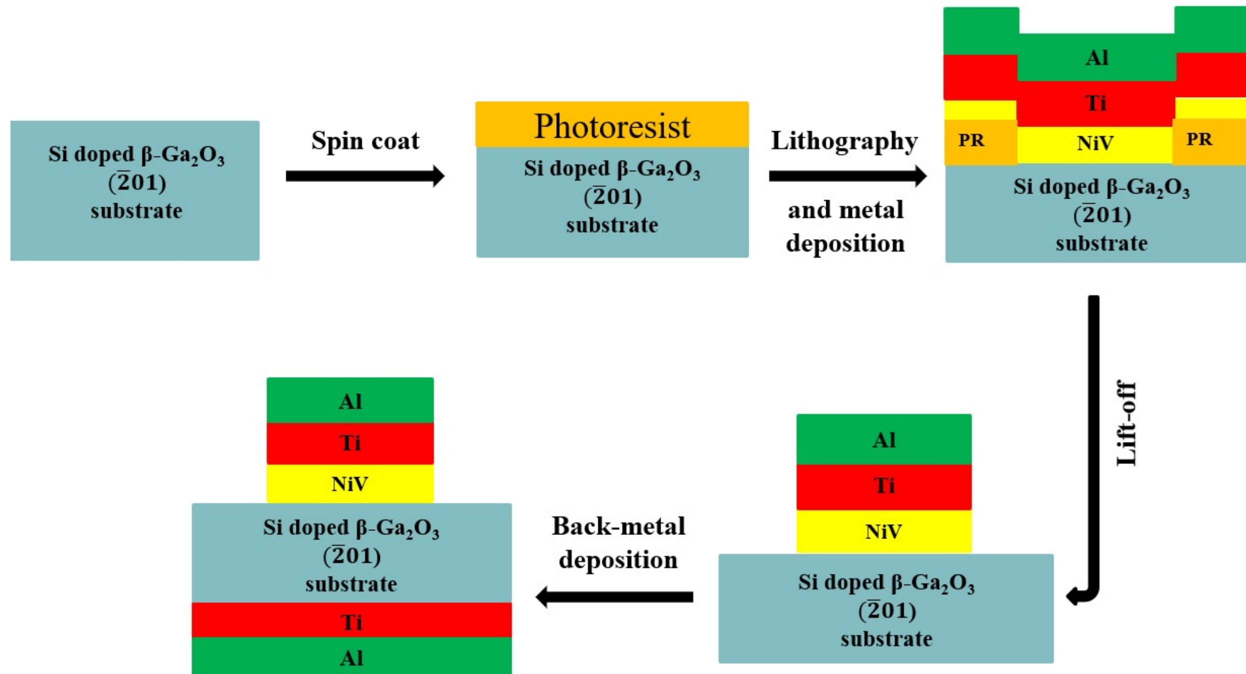


Figure 2.11: Flow diagram of SBD contact fabrication steps.

After patterning, the samples were transferred into the sputtering chamber for metal deposition. Without breaking the vacuum, a multilayer stack of NiV, Ti, and Al metals was sputtered onto the samples. Maintaining the vacuum throughout the deposition process minimized contamination and ensured high-quality metal films. Once the deposition was complete, a lift-off process was performed to strip away any excess metal and reveal the patterned structures. The photomask used for this process contained circular patterns with three different diameters to create contacts of varying sizes. The largest circular structures had a diameter of 350 µm, while the smallest measured 80 µm. For electrical characterization, including current-voltage (I-V) and capacitance-voltage (C-V) measurements, the largest diameter contacts were utilized due to their larger surface area, which facilitated accurate testing. An image of SBD mask has been shown in figure 2.12.

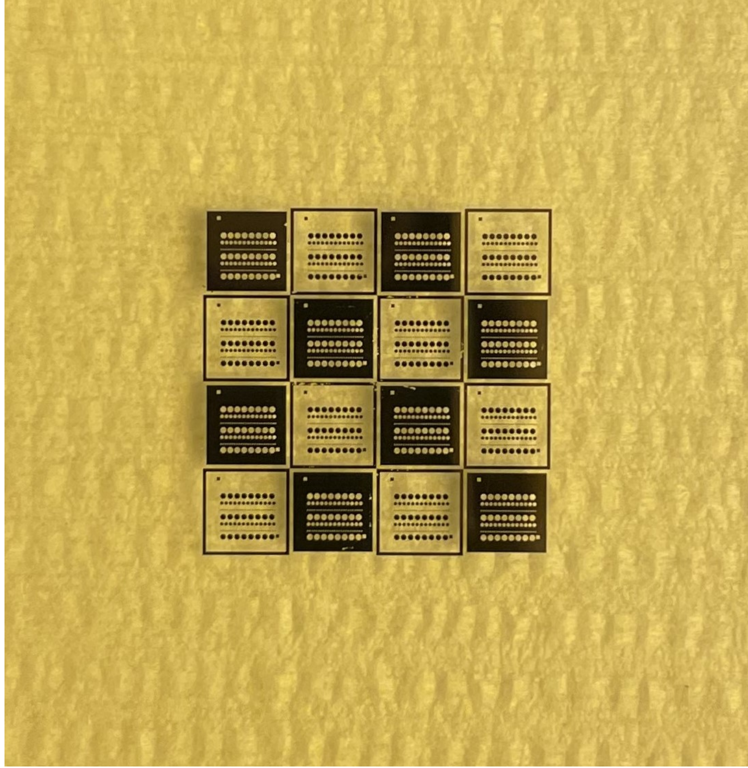


Figure 2.12: Schottky Barrier Diode mask for photolithography.

To form ohmic contacts on the backside of the samples, Ti and Al were deposited. Titanium was specifically chosen for the back contact due to its relatively low work function of 4.33 eV, which promotes effective electron injection [49]. The selection of Ti was further supported by prior studies reported in the literature, demonstrating its suitability as an ohmic contact material for β-Ga_2O_3. This comprehensive process ensured the fabrication of high-quality SBD devices suitable for subsequent electrical testing and characterization.

Chapter 3

Experimental Techniques

3.1 X-Ray Diffraction analysis

X-ray diffraction (XRD) is a bulk-sensitive analytical technique that relies on the constructive interference of elastically scattered X-rays from atoms within a crystal lattice. X-rays are generated when high-energy electrons interact with the anode material of an X-ray tube. Two processes occur: (i) electrons decelerated by the atomic core produce a continuous X-ray spectrum, and (ii) high-energy electrons displace core electrons, leading to characteristic X-ray emission from electron transitions to fill the vacancy. Crystals, composed of regularly spaced atoms, typically have interatomic spacings of a few angstroms, making X-rays with wavelengths between 0.5 Å and 5 Å suitable for diffraction studies. A commonly used X-ray source for such measurements is Cu Kα radiation, which consists of Kα_1 and Kα_2 components and has a wavelength of approximately 1.54 Å. However, high-resolution XRD filters out Kα_2, utilizing only the Kα_1 line by diffracting X-rays through two Ge crystals aligned to satisfy Bragg's condition for Kα_1. All measurements in this dissertation were performed using Cu Kα_1 radiation (1.54 Å). When X-rays interact with solids, they generate photoelectrons, fluorescent X-rays, and scattered X-rays. XRD specifically analyzes coherently scattered X-rays that satisfy Bragg's condition, producing diffraction patterns used to extract detailed structural information [50].

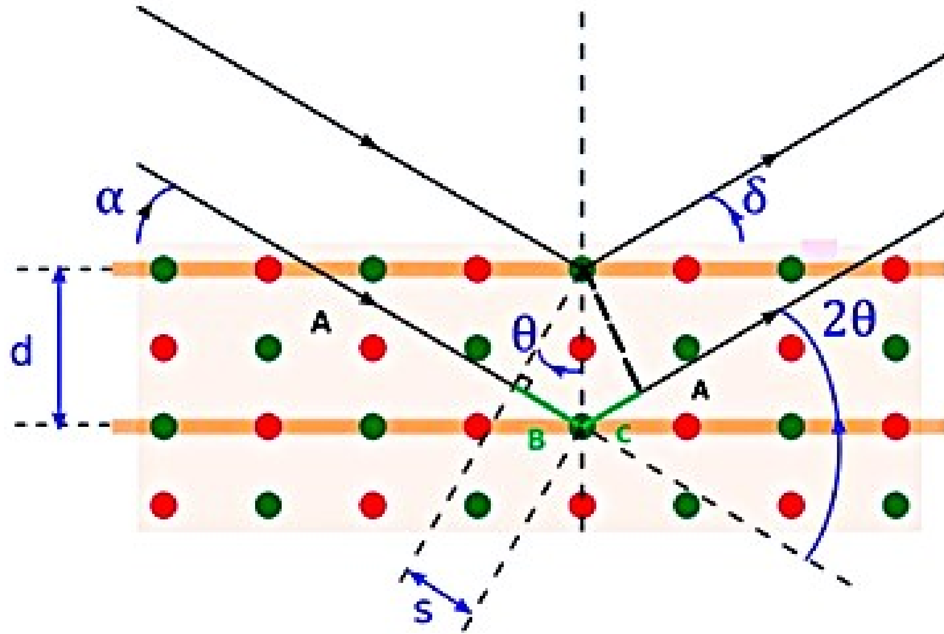


Figure 3.1: Ray diagram of XRD following Bragg's law. A, B, C are the path lengths and d is the plane spacing.

XRD provides structural information about materials by analyzing the size and orientation of their unit cells. This is based on Bragg's law, which describes constructive interference occurring when the path difference between scattered X-rays, is an integer multiple of the wavelength (λ).

$$2d_{hkl}\sin\theta = n\lambda \tag{3.1}$$

where θ is angle of incidence and λ is the wavelength of the X-ray. In a cubic crystal with lattice constant 'a', (hkl) atomic planes are separated by a distance,

$$d_{hkl} = \frac{a}{\sqrt{h^2 + k^2 + l^2}} \tag{3.2}$$

The diffraction pattern obtained enables the determination of lattice parameters, texture, grain size, and microstrain. In this study, high-resolution X-ray diffraction (HRXRD) has been employed to assess the crystallinity of implanted samples.

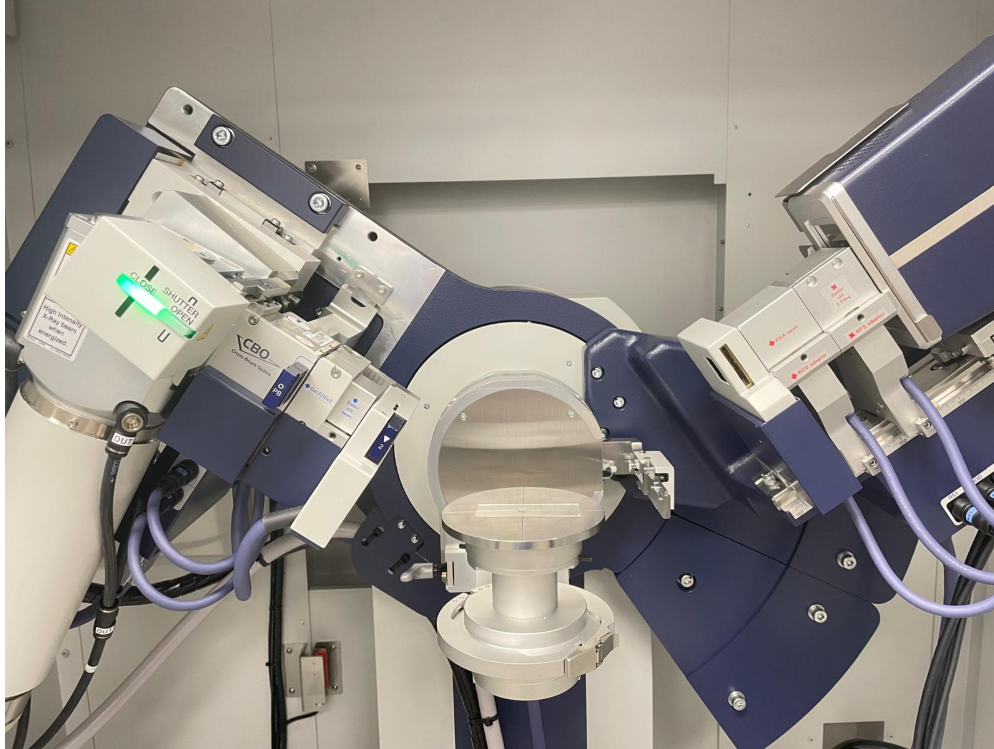


Figure 3.2: The Rigaku SmartLab X-Ray diffraction machine.

3.1.1 High Resolution X-Ray Diffraction analysis

High-resolution X-ray diffraction (HRXRD) encompasses a series of advanced, non-destructive analytical techniques specifically designed for characterizing crystalline materials with highly ordered structures. These materials often include epitaxial thin films, heterostructures, and superlattices, where precise knowledge of structural properties is essential for their effective implementation in devices and applications. HRXRD techniques provide detailed insights into crystallographic parameters such as lattice constants, strain, composition, interface quality, and layer thickness. The ability to accurately evaluate these properties is critical for optimizing material performance in electronic and optoelectronic applications.

A key requirement for HRXRD experiments is a monochromatic X-ray beam with minimal angular divergence and a well-defined wavelength spread. This ensures high precision in

measurements by eliminating distortions caused by unwanted wavelengths and angular variations. Unlike conventional X-ray diffraction (XRD), HRXRD systems are equipped with monochromators capable of selectively filtering out Cu Kα_2 radiation and other undesirable spectral components. This filtering process prevents improper constructive interference, which can arise from the presence of multiple wavelengths in the X-ray source, thus improving resolution and accuracy. Among the various scan modes available, out-of-plane XRD scanning is widely employed in HRXRD for analyzing thin-film single crystals, as it offers detailed information about structural parameters such as crystal orientation, strain, and layer thickness. The Rigaku SmartLab system used in this study is equipped with a Cu Kα_1 source optimized for thin-film samples. It employs a parabolic mirror and a double-bounce Ge (220) monochromator to refine the X-ray beam, ensuring high resolution and reliability in the characterization of epitaxial layers and heterostructures.

3.2 Secondary Ion Mass Spectroscopy (SIMS) analysis

Secondary ion mass spectrometry (SIMS) is recognized as one of the most powerful and versatile analytical techniques for detecting impurities in solid materials [51]. Originally developed by Castaing and Slodzian, as well as Herzog and collaborators [52], SIMS operates by sputtering material from a solid surface and analyzing the ionized species ejected during the process. While the majority of sputtered particles are neutral atoms that cannot be analyzed, only the ionized species are filtered based on energy and passed through a mass spectrometer for analysis. This method can detect all elements and is regarded as the most sensitive among beam-based techniques, with detection limits reaching 10^{14} to 10^{15} atoms cm^{-3} in cases where background interference signals are minimal. SIMS enables simultaneous detection of multiple elements, offers excellent depth resolution ranging from 1 to 5 nm, and provides lateral surface characterization over several microns. Despite its high sensitivity and precision, SIMS is a destructive technique, as the sputtering process leaves a visible crater on the sample surface due to material removal.

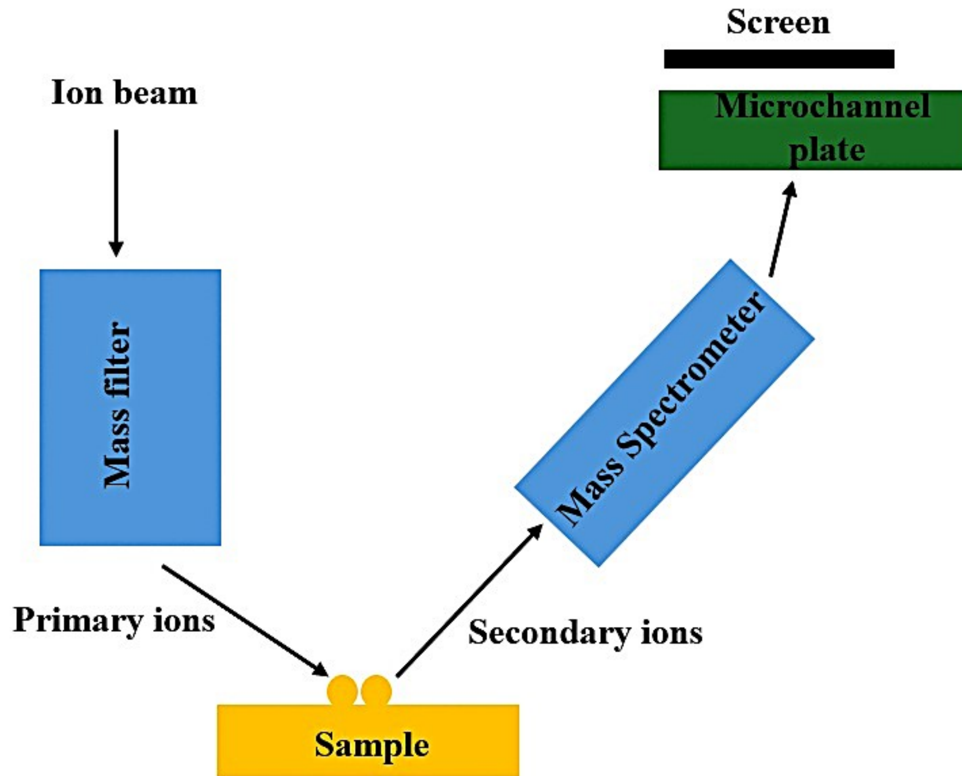


Figure 3.3: Ray diagram of SIMS.

SIMS operates by sputtering material from a sample surface and analyzing the ejected particles using a mass analyzer. A schematic representation of this process is provided in Figure 3.3. In this technique, a primary ion beam bombards the sample, causing atoms to be dislodged or sputtered from the surface. While most of these ejected atoms are neutral and cannot be detected directly by conventional SIMS, a small fraction becomes ionized, either positively or negatively. This ionized fraction, although relatively low, is sufficient for effective analysis [53]. The mass/charge ratio of the ionized particles is measured and recorded as a mass spectrum, displayed either as a count or visualized on a fluorescent screen. However, challenges arise due to the presence of light elements such as hydrogen (H), carbon (C), oxygen (O), and nitrogen (N) within the SIMS vacuum environment. These elements can interfere with accurate identification, as the mass spectrometer relies solely on the mass/charge ratio, which can occasionally lead to misidentification of ions with similar values.

SIMS employs two primary instrumentation methods: (i) the ion microprobe and (ii) the ion microscope [54]. The ion microprobe functions similarly to an electron microprobe, where a finely focused primary ion beam scans, or rasters, across the sample surface. The resulting secondary ions are mass-analyzed, and the output from the mass spectrometer is displayed on a CRT screen, synchronized with the primary beam, to create a detailed map of secondary ion intensity over the sample surface. The mass spectrometer used in this method incorporates both electrostatic and magnetic sector analyzers in series [55]. Within the electrostatic analyzer, ions travel between two parallel plates separated by a distance d and follow a curved trajectory with a radius of curvature r_V. A potential difference V is applied across the plates, allowing only ions with a specific energy E to pass through without colliding with the plates, ensuring accurate mass and energy analysis [7]. The energy can be expressed as,

$$E = \frac{qVr_V}{2d} \tag{3.3}$$

A magnetic field B curves the ion of mass m, charge q, and energy E into a path of radius r_B according to,

$$\frac{m}{q} = \frac{qB^2r_B^2}{2E} \tag{3.4}$$

combining above two equations mass/charge ratio can be expressed as,

$$\frac{m}{q} = \frac{dB^2r_B^2}{Vr_V} \tag{3.5}$$

The ion microscope functions as a direct imaging tool, similar to an optical microscope or TEM. It uses a broad primary ion beam to uniformly illuminate the sample, while secondary ions are collected across the entire imaged area. The spatial arrangement of these ions is maintained as they pass through a combination of electrostatic and magnetic analyzers. The signal is then amplified using a microchannel plate and visualized on a fluorescent screen.

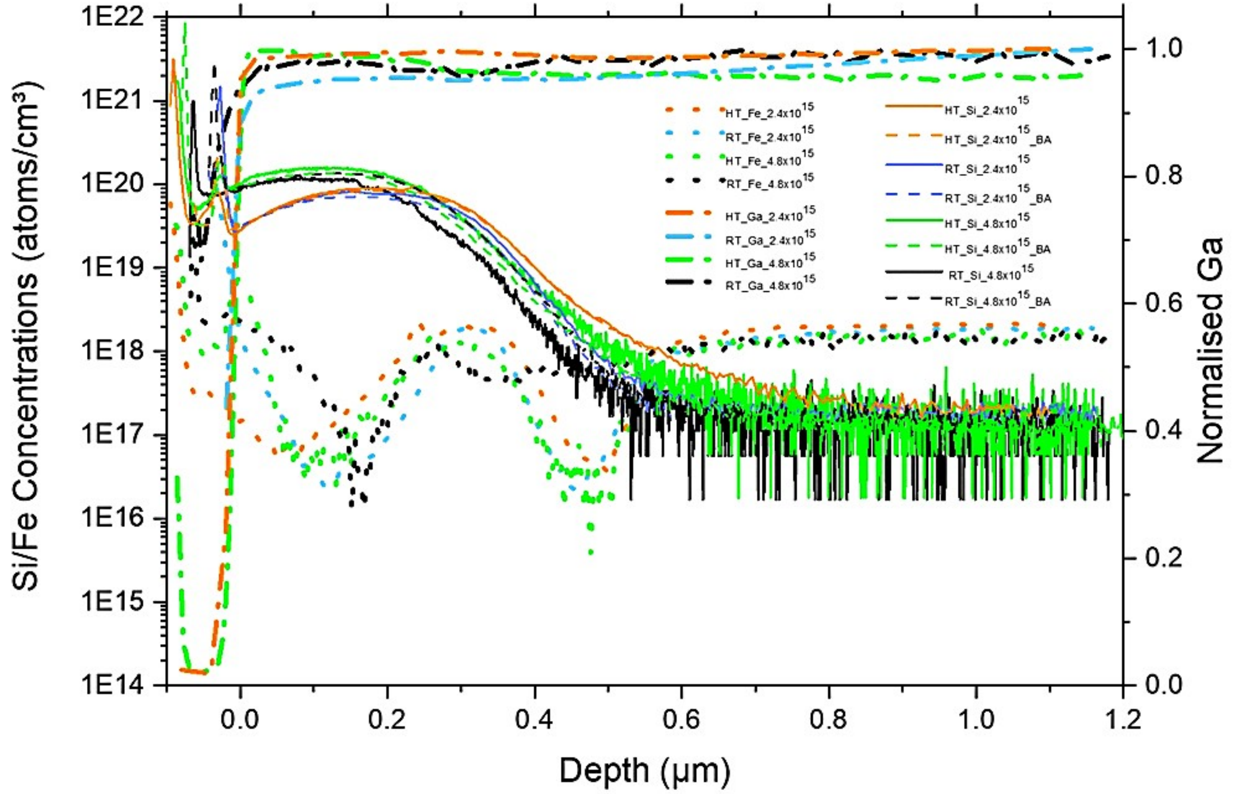


Figure 3.4: SIMS profile of Si, Fe and Ga for different implant temperatures and doses.

SIMS measurements are well suited for semiconductor applications, because matrix effects are minor and ion yields can be assumed to be linearly proportional to densities. Furthermore, the substrate sputters very uniformly, at least for Si. An example profile has been shown in figure 3.4 where silicon (Si), iron (Fe) and gallium (Ga) can be determined in a single measurement. This sample was formed by implanting Si in the β-Ga_2O_3 substrate. The plot showed profile of different elements at different implant temperature and doses.

Several factors must be considered during data analysis in SIMS measurements to ensure accuracy and reliability. These include artifacts such as crater wall effects, ion knock-on, atomic mixing, diffusion, preferential sputtering, and surface roughening. While some of these issues stem from instrument-related limitations and can be partially mitigated through optimized settings, others are inherently linked to the sputtering process itself and may require careful interpretation of results to minimize errors.

3.3 Scanning Transmission Electron Microscopy

Scanning transmission electron microscopy (STEM) is a high-resolution imaging technique used to analyze materials at the atomic scale. It operates by focusing a finely tuned electron beam, approximately 1Å in size, into a point probe, which is sufficient to resolve interatomic distances in most crystal structures. This highly focused electron beam is scanned across a thin cross-section of the sample to generate detailed images. Since STEM relies on transmitted electrons to create these images, the sample must be extremely thin—typically less than 100 nm—to ensure adequate electron penetration. The transmitted electrons interact with the atoms in the material, scattering in different directions. Various detectors then capture these scattered electrons, allowing for the reconstruction of a high-resolution cross-sectional image that reveals crucial structural details about the material, particularly in thin film samples.

STEM sample preparation involves an intricate process to obtain a thin cross-sectional slice, known as a lamella, which is necessary for successful imaging. This process begins with a technique called lift-out, where a focused ion beam (FIB) is used to selectively mill away material surrounding the region of interest. Once the lamella is isolated, the FIB is further employed to thin it down to the required thickness of approximately 100 nm or less, ensuring that the electron beam can effectively pass through the sample. After the thinning process is complete, the prepared lamella is carefully positioned in the STEM system, ensuring that the electron beam is oriented normal to its surface. This meticulous preparation allows STEM to capture atomic-scale details of thin films, providing critical insights into the structural properties of the material.

3.4 Van der Pauw Hall measurement

The van der Pauw method is a widely used technique for determining the resistivity and Hall coefficient of materials [56]. This method is particularly useful for samples of

arbitrary shapes, provided they are two-dimensional and free of holes. The van der Pauw method utilizes a four-point probe configuration around the sample's edges to calculate a sheet resistance (R_{sh}), offering a more comprehensive assessment of the material's electrical properties. The resistivity of a sample with thickness t can be expressed as follows,

$$\rho = R_{\text{sh}} t \tag{3.6}$$

A standard Hall effect measurement setup includes current source, voltmeter, and magnet. Given the significance of resistivity and Hall coefficient measurements across varying temperatures in semiconductor research, these systems are often integrated with precise heating and cooling mechanisms. This configuration enables measurements over a broad temperature range, facilitating comprehensive analysis of the material's electrical properties.

3.4.1 Sample preparation

In order to measure hall effect, four ohmic contacts need to be fabricated on the four corners of the sample. For accurate measurements using the Hall effect method, specific sample requirements must be met. The sample thickness should be significantly smaller than its width and length, and a symmetrical shape is preferred to minimize calculation errors. Ideally, the contact regions should be much smaller compared to the overall sample dimensions. The sample surface must be smooth and free of isolated holes to ensure uniform current distribution. Additionally, the contacts and their connecting leads should be made from the same material to reduce thermoelectric effects and maintain symmetry during measurements.

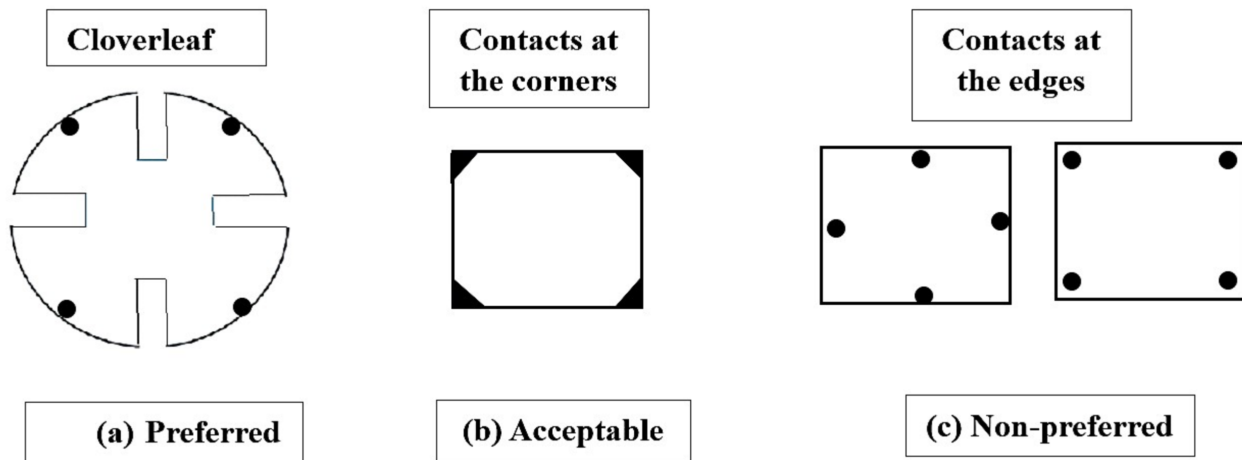


Figure 3.5: Van der Pauw sample patterns according to preferences.

3.4.2 Resistivity Measurement

To perform a measurement, a current is applied along one edge of the sample (I_{12}), while the voltage is measured across the opposite edge (V_{12}). This setup, illustrated in Figure 3.6, enables the calculation of resistance by applying Ohm's law,

$$R_{12,34} = \frac{V_{34}}{r_{12}} \tag{3.7}$$

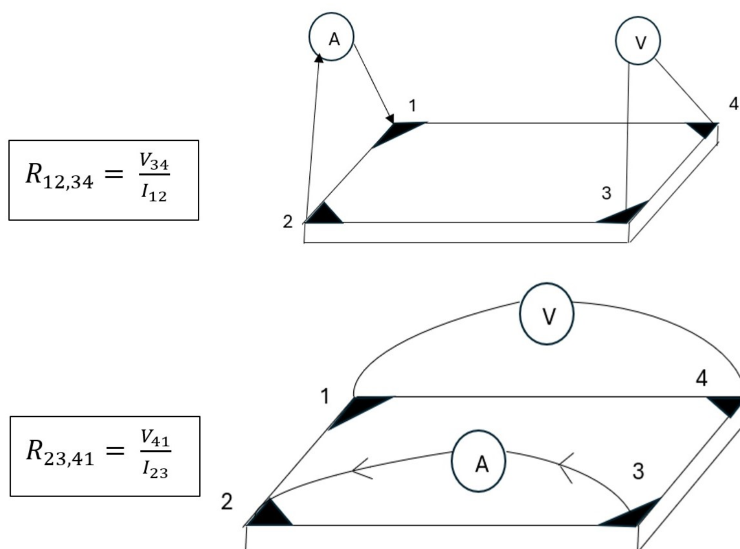


Figure 3.6: Measurement of $R_{12,34}$ and $R_{23,41}$.

Van der Pauw established that the sheet resistance of a sample, regardless of its geometric shape, can be accurately calculated using resistance measurements taken along two distinct orientations. One measurement is obtained along a vertical edge, denoted as $R_{12,34}$, while the other is recorded along a horizontal edge, referred to as $R_{23,41}$. The actual sheet resistance R_s can be expressed using the following formula,

$$e^{-\frac{\pi R_{12,34}}{R_s}} + e^{-\frac{\pi R_{23,41}}{R_s}} = 1 \tag{3.8}$$

3.4.3 Reciprocal Measurement

According to reciprocity theorem, we have assumed $R_{AB,CD} = R_{CD,AB}$ in equation 3.6. However, due to non-identical shapes of ohmic contacts $R_{AB,CD}$ is not equal to $R_{CD,AB}$. So to obtain more accurate value for the resistances an average of resistances $R_{12,34}$ and $R_{23,41}$ with their reciprocal values $R_{34,12}$ and $R_{41,23}$ need to be obtained. We can define the vertical and horizontal values as follows,

$$R_{\text{vertical}} = \frac{R_{12,34} + R_{34,12}}{2} \tag{3.9}$$

$$R_{\text{horizontal}} = \frac{R_{23,41} + R_{41,23}}{2} \tag{3.10}$$

By replacing above two equations in equation 3.6 van der Pauw formula can be expressed as,

$$e^{-\frac{\pi R_{vertical}}{R_s}} + e^{-\frac{\pi R_{horizontal}}{R_s}} = 1 \tag{3.11}$$

3.4.4 Reverse Polarity Measurement

The precision of resistance measurements can be enhanced by eliminating offset voltages, such as thermoelectric potentials caused by the Seebeck effect. This can be achieved by performing resistance measurements twice—once with the standard polarity and then with

reversed polarities for both the current source and the voltage meter. Since these measurements correspond to the same region of the sample but in opposite directions, the vertical ($R_{vertical}$) and horizontal ($R_{horizontal}$) resistances can be accurately determined by averaging the results obtained from the standard and reversed polarity measurements. This approach minimizes errors and ensures more reliable calculations of sheet resistance. Both resistances can be expressed as follows,

$$R_{\text{vertical}} = \frac{R_{12,34} + R_{34,12} + R_{21,43} + R_{43,21}}{2} \tag{3.12}$$

$$R_{\text{horizontal}} = \frac{R_{23,41} + R_{41,23} + R_{32,14} + R_{14,32}}{2} \tag{3.13}$$

3.4.5 Hall Measurement

If a steady state current is flowing into the semiconductor sample the velocity (v) of electrons can be expressed as,

$$v = \frac{I}{nAq} \tag{3.14}$$

where I is the current, n is the electron density, A is the cross-sectional area of the sample and q is the charge.

Lorentz force will be exerted on the electrons due to the motion of electrons if the semiconductor material is placed in an external magnetic field. The Lorentz force can be expressed as,

$$\vec{F} = q(\vec{v} \times \vec{B}) \tag{3.15}$$

where q is the charge on the particle, v is the traveling velocity in magnetic field, and B is the strength of the magnetic field. The Lorentz force is stronger if the direction of motion is perpendicular to the magnetic field.

When a magnetic field is applied perpendicular to the direction of current flow in a semiconductor bar, it exerts a force on the moving electrons. This force, known as the Lorentz force, drives the electrons toward one side of the bar. As electrons accumulate, they

generate an electric field that opposes further charge separation. Eventually, equilibrium is established when the electric force created by this field counterbalances the Lorentz force. This phenomenon gives rise to a measurable potential difference across the bar, referred to as the Hall voltage (V_H). By analyzing the governing equations and recognizing that q represents the electron charge, an expression for the Lorentz force acting on the electrons can be derived.

When a magnetic field is applied perpendicular to the direction of current flow in a semiconductor bar, it induces a Lorentz force that pushes the electrons toward one side of the material. This movement causes a buildup of charge, resulting in the formation of an electric field. The process continues until the electric force generated by this field counteracts the Lorentz force, establishing equilibrium. As a result, a voltage difference, known as the Hall voltage (V_H), develops across the semiconductor. By relating equations 3.12 and 3.13, an expression for the Lorentz force acting on the electrons can be derived as follows,

$$F = \frac{IB}{nA} \tag{3.16}$$

since under equilibrium condition F is equivalent to Eq, electric field can be expressed as,

$$E = \frac{IB}{nAq} \tag{3.17}$$

And the hall voltage can be written as,

$$V_H = WE = \frac{WIB}{nAq} = \frac{IB}{n_s q} \tag{3.18}$$

where W is the width of the sample, d is the thickness of the sample. A schematic of Hall measurement has been shown in figure 3.7.

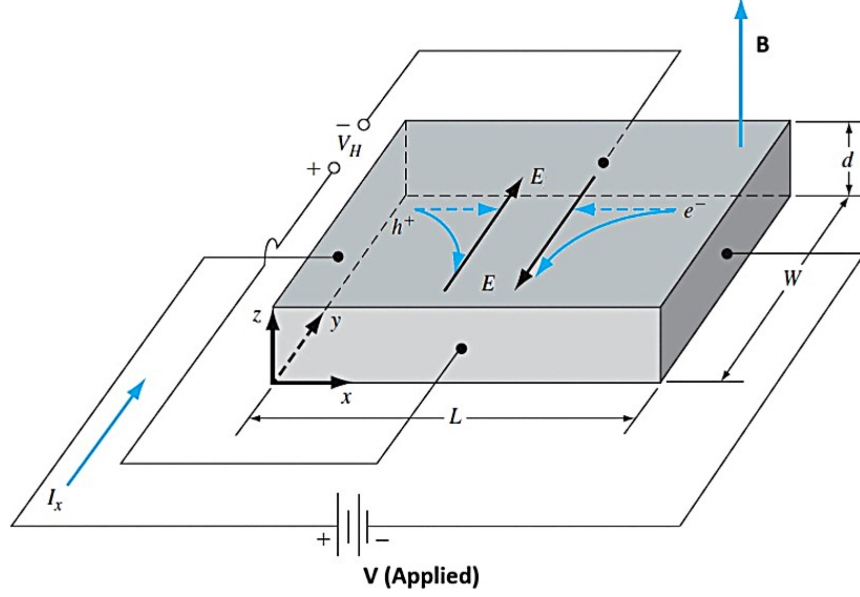


Figure 3.7: Hall effect measurement configuration [5]

3.4.6 Hall Voltage Calculation

If we consider the difference of the voltages for positive and negative magnetic fields the overall Hall voltage can be expressed as,

$$V_{\mathrm{H}} = \frac{V_{13} + V_{31} + V_{24} + V_{42}}{8} \tag{3.19}$$

where,

$$V_{13} = V_{13,P} - V_{13,N}$$

$$V_{31} = V_{31,P} - V_{31,N}$$

$$V_{24} = V_{24,P} - V_{24,N}$$

$$V_{42} = V_{42,P} - V_{42,N}$$

The type of the semiconductor material can be found out from the polarity of the Hall voltage. For is p-type material for $V_{\mathrm{H}}>0$ and the material is n-type if $V_{\mathrm{H}}<0$. The sheet

density can be expressed as follows,

$$n_s = \frac{IB}{qV_H} \tag{3.20}$$

It is important to ensure that the magnetic field strength, B, is expressed in units of Wb/cm^2 when n_s is given in cm^{-2}.

3.4.7 Mobility Calculation

The resistivity of a semiconductor material can be expressed as,

$$\rho = \frac{1}{n\mu_n q + p\mu_p q} \tag{3.21}$$

where μ_n and μ_p are the carrier mobilities of electrons and holes, and n and p denote concentration of electrons and holes respectively [57]. In most cases, the material is heavily doped, resulting in a significant disparity, often several orders of magnitude, between the concentrations of the two carrier types. Similarly, the doping concentration in the epitaxial layer is typically much higher than that in the substrate. This substantial difference allows the equation to be simplified for practical analysis.

$$\rho = \frac{1}{n_m \mu_m q} \tag{3.22}$$

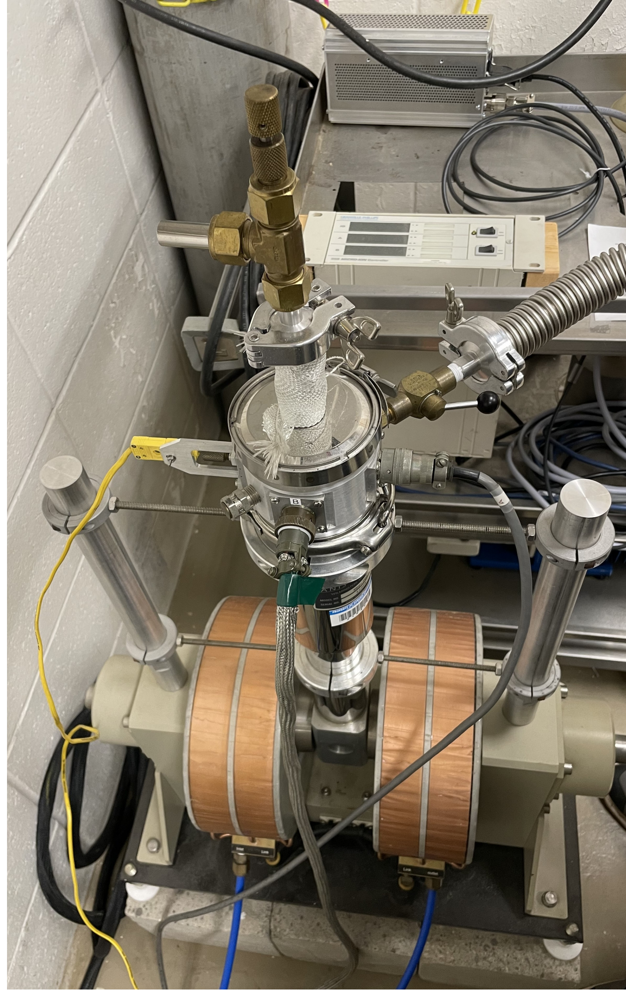
where n_m and μ_m represents doping level and mobility of the majority carriers respectively. Replacing $\rho = R_{sh}t$ and $n_s = n_m d$ in equation 3.20 and rearranging, the majority carrier mobility can be expressed as,

$$\mu_m = \frac{1}{n_s R_{sh} q} \tag{3.23}$$

3.4.8 Hall Effect Measurement

The Hall measurement system depicted in Figure 3.8 consists of several key components, including a liquid nitrogen VPF-700 cryostat, a GMW Model 5403 electromagnet, a

KEPCO power supply, and a KEITHLEY 7001 switch system. Additionally, it includes a KEITHLEY 6514 system electrometer, a KEITHLEY 6220 precision current source, and a temperature controller. The system operates across a temperature range of 77K to 700K and can supply a maximum current of 100 mA. The water-cooled electromagnet generates a maximum magnetic field of 0.6 T, ensuring stable operation during measurements.



(a)

(b)

Figure 3.8: (a) Hall measurement setup with magnets; (b) Sample holder inside the cryostat.

Hall measurements are conducted within a temperature range of 70K to 500K for Si-implanted samples. As illustrated in Figure 3.8, the sample is mounted on a holder with four wires connected—two for current sourcing and two for voltage measurement. The sample holder is then placed inside the cryostat. To prevent thermal effects and ensure accurate results, the sourcing current is maintained below 10 mA, as excessive current may heat the sample and distort measurements. The magnetic field strength varies between 0.1 T and 0.6 T during the experiments.

3.5 Transfer Length Method (TLM)

3.5.1 Specific Contact Resistance Measurement

Metal-semiconductor contacts can be broadly classified into two types based on the direction of current flow, either vertical or horizontal relative to the contact. In the analysis of ohmic contacts to semiconductors, greater emphasis is placed on the specific contact resistance (r_c) measured in Ω-cm^2 rather than the overall contact resistance (R_c). The contact resistance represents the total electrical resistance at the interface between the metal and semiconductor, which is influenced by the contact area and geometry. In contrast, specific contact resistance characterizes the intrinsic properties of the interface that affect R_c and can be expressed as,

$$R_c = \frac{r_c}{A} \tag{3.24}$$

where A is the surface area of the contact. Since it is independent of the contact area, r_c serves as a reliable parameter for comparing contacts of different sizes. In terms of the current density J (units of A/cm^2), the specific contact resistance can be written as [58],

$$r_c = \lim_{V \to 0} \left(\frac{dJ}{dV} \right)^{-1} \tag{3.25}$$

Techniques for measuring contact resistance are generally categorized into four types: two-contact two-terminal, multiple-contact two-terminal, four-terminal, and six-terminal methods. In the following section, we will focus on the multiple-contact two-terminal measurement technique.

3.5.2 Transmission Line Model analysis

The Transmission Line Model (TLM), originally introduced by Murrmann and Widmann, is a widely used method for evaluating contact resistance and sheet resistance. This model accommodates both linear and concentric test structures for analysis [59]. Berger later extended the TLM framework by accounting for nonzero values of both contact resistance and sheet resistance while assuming a negligible semiconductor sheet thickness [60]. Based on this model, contact resistance can be determined using the following expression,

$$R_c = \sqrt{R_{sh} \cdot \rho_c} \coth\left(\frac{L}{L_T}\right) \tag{3.26}$$

where R_{sh} is sheet resistance, ρ_c is specific contact resistivity, L is the length of the contacts and L_T is the transfer length.

$$L_T = \sqrt{\frac{\rho_c}{R_{sh}}} \tag{3.27}$$

For $L \leq 0.5\ L_T$, equation 3.26 can be solved as,

$$R_c = \frac{\rho_c}{L \cdot Z} \tag{3.28}$$

For $L \geq 0.5\ L_T$, equation 3.26 can be solved as,

$$R_c = \frac{\rho_c}{L_T \cdot Z} \tag{3.29}$$

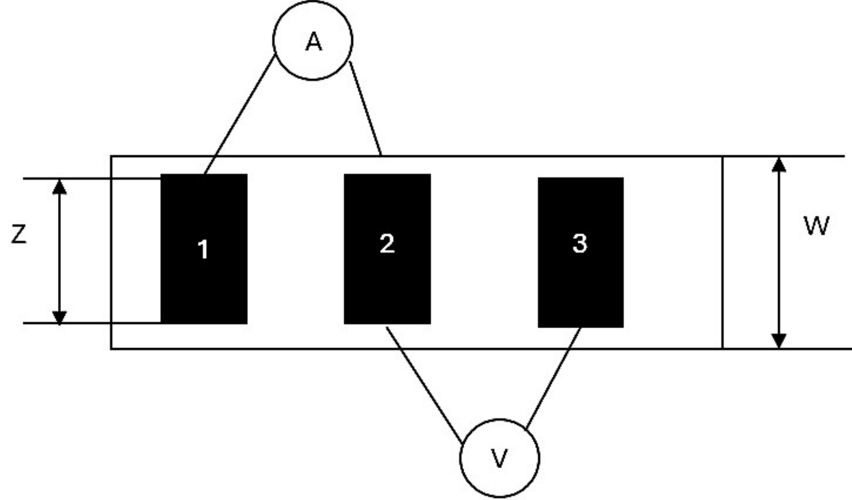


Figure 3.9: Test structure for end resistance measurement using Transmission Line Model.

Contact end resistance can be achieved (Figure 3.9) by applying current in from 2 to 1 and measuring voltage between contacts 2 and 3 [7]. The contact end resistance can be written as,

$$R_c = \sqrt{R_{sh} \cdot \rho_c}\,\frac{1}{\sinh\left(\frac{L}{L_T}\right)} \tag{3.30}$$

However, accurately measuring the end resistance poses a challenge when the contact size is extremely small. This limitation restricts the applicability of the transmission line method.

3.5.3 Transfer Length Method Analysis

The Transfer Length Method (TLM), initially introduced by Shockley, was developed to address the limitations and inaccuracies associated with the Transmission Line Method. While both methods share the same abbreviation, TLM, a key distinction lies in the number of contacts they accommodate. The Transmission Line Method is restricted to three contacts, whereas the Transfer Length Method supports more than three contacts. The test structure utilized for the Transfer Length Method is illustrated in Figure 3.10.

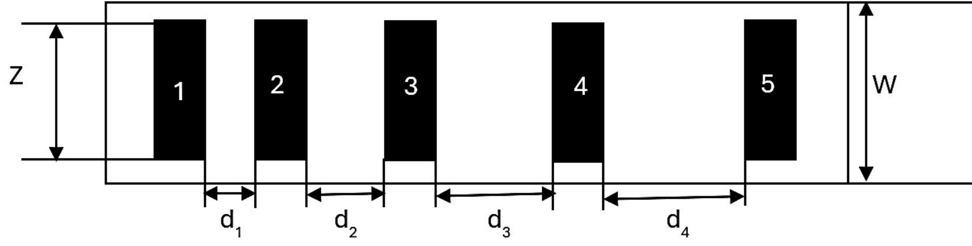


Figure 3.10: Transfer Length Method test structure.

The total resistance from two adjacent pad can be written as,

$$R_T = 2R_c + R_s \tag{3.31}$$

where R_c is the contact resistance, R_s is the resistance from the semiconductor between two pads. R_s can be expressed as,

$$R_s = \frac{R_{sh} \cdot d}{Z} \tag{3.32}$$

where Z is the contact width, d is the distance between two consecutive contacts. Replacing 3.32, equation 3.31 can be rewritten as [7],

$$R_T = 2R_c + \frac{R_{sh} \cdot d}{Z} \tag{3.33}$$

In terms of transfer L_T, we can write 3.33 as,

$$R_T \approx \frac{R_{sh}}{Z} \left(2L_T + d\right) \tag{3.34}$$

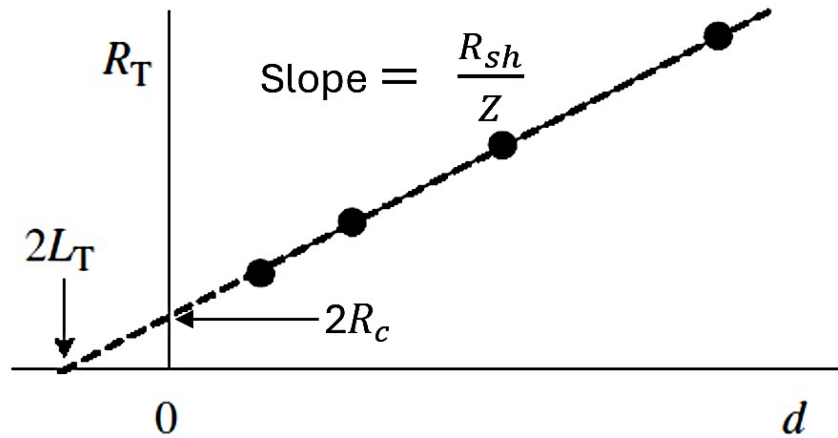


Figure 3.11: Linear plot of total resistance vs contact spacing [8].

The total resistance is measured for different contact spacings and plotted against d, as shown in Figure 3.11. From this plot, three key parameters can be determined. The slope of the plot, R_{sh}/Z, provides the sheet resistance, where Z represents the contact width, measured independently. The y-intercept at d = 0 corresponds to $R_T = 2R_c$, from which the contact resistance can be calculated. Additionally, the x-intercept at $R_T = 0$ yields $-d = 2L_T$, allowing for the determination of the specific contact resistivity, provided the sheet resistance (R_{sh}) is known from the slope. The transfer length method thus offers a comprehensive characterization of the contact, including the sheet resistance, contact resistance, and specific contact resistivity.

3.6 Schottky Barrier Diode

The band diagram of a Schottky barrier diode on an n-type and p-type substrate is shown in Figure 3.12.

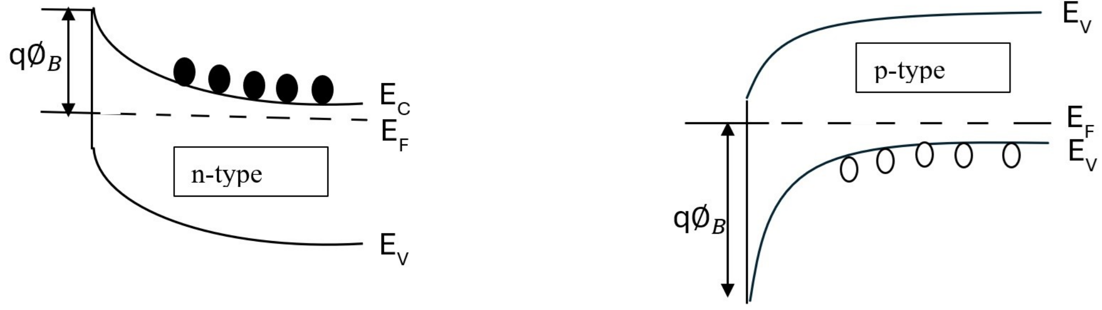


Figure 3.12: Band diagram of a Schottky barrier diode on an n-type and p-type substrate.

Here ϕ_{B} is the barrier height which can be written as ([61],[62]),

$$\phi_B = \phi_M - \chi \tag{3.35}$$

where ϕ_{M} is the metal work function and χ is electron affinity of the semiconductor. χ can be defined as the potential difference between the bottom of the conduction band and the vacuum level at the semiconductor surface. In Schottky theory, the barrier height is determined solely by the metal's work function and the semiconductor's electron affinity, with no dependence on the doping density of the semiconductor. The thermionic current-voltage relationship for a Schottky barrier diode can be described by the corresponding equation,

$$I = AA^*T^2 e^{\frac{q\phi_B}{kT}} \left(e^{\frac{qV}{nkT}} - 1 \right) = I_s \left(e^{\frac{qV}{nkT}} - 1 \right) \tag{3.36}$$

where $\mathrm{I_s}$ is the saturation current, A the diode area, A* is Richardson's constant, and n the ideality factor. The ideality factor accounts for various factors that deviate from ideal behavior. In practice, a Schottky diode often exhibits non-uniformity across its surface. Variations in barrier height, known as patchiness, contribute n > 1 and explain phenomena such as a decrease in n with increasing temperature or reverse bias [63]. To determine n, it is common practice to use that range of the log(I)–V plot where series resistance is negligible.

Under this restriction equation 3.36 can also be expressed as,

$$I = I_s e^{\frac{qV}{nkT}} \left(1 - e^{\frac{-qV}{kT}}\right) \tag{3.37}$$

3.6.1 Barrier Height Measurement Methods

3.6.1.1 Current-Voltage Method

In current-voltage measurement techniques, the barrier height is typically determined using the saturation current (I_s), which is obtained by extrapolating the semilogarithmic plot of I versus V to V=0.

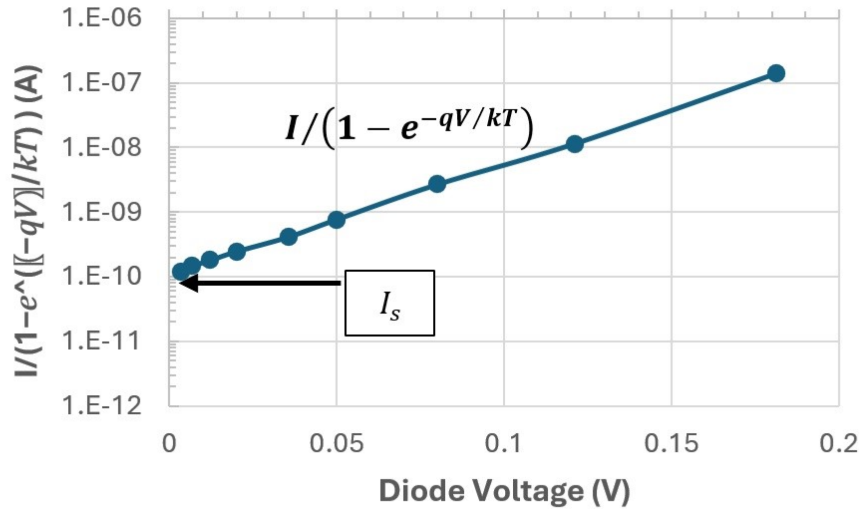


Figure 3.13: Current-Voltage plot for n-type Al/GaAs Schottky barrier diode [6].

The barrier height ϕ_B is then calculated from I_s using the expression provided in Eq. (3.36) as follows,

$$\phi_B = \frac{kT}{q} \ln\left(\frac{AA^*T^2}{I_s}\right) \tag{3.38}$$

The accuracy of ϕ_B the calculation in Eq. (3.38) is limited by the uncertainty in A^*. However, since A^* appears in the logarithmic term, its impact on ϕ_B is relatively small, causing only minor errors.

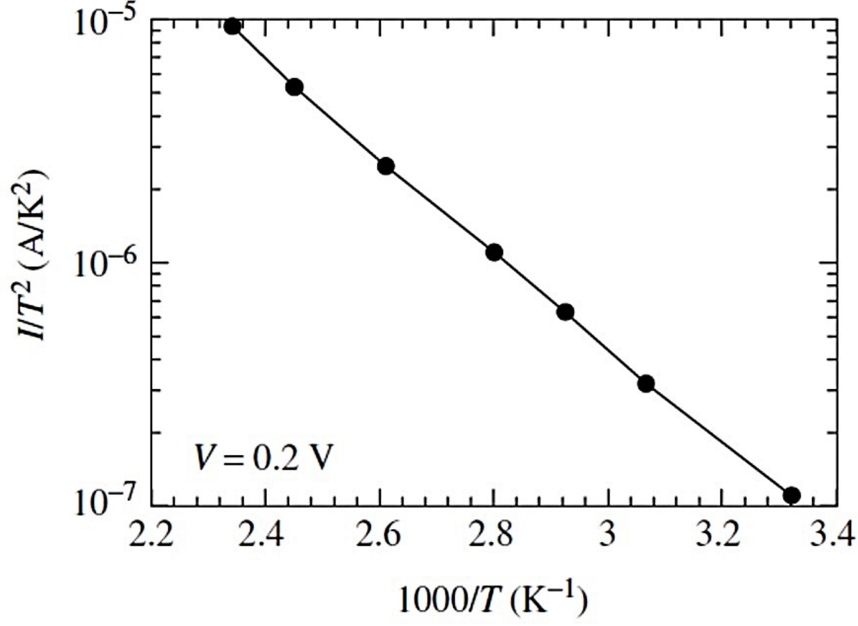


Figure 3.14: Richardson plot of Schottky Barrier Diode measured at 0.2 V [7].

3.6.1.2 Current-Temperature Method

Using the condition V >> kT, equation 3.36 can be expressed as,

$$\ln\left(\frac{1}{T^2}\right) = \ln(AA^*) - \frac{q\left(\phi_B - \frac{V_1}{n}\right)}{kT} \tag{3.39}$$

A Richardson plot, which is a graph of $\ln(1/T^2)$ versus 1/T at a constant forward bias voltage $V = V_1$, has a slope of $q(\phi_B - V_1/n)/kT$ and a vertical-axis intercept of ln (AA*), as illustrated in Figure 3.14. While the slope is typically well-defined, determining A* from the intercept is susceptible to errors. The barrier height can be written as,

$$\phi_B = \frac{V_1}{n} - \frac{k}{q}\frac{d\left(\ln\left(\frac{I}{T^2}\right)\right)}{d\left(\ln\left(\frac{1}{T}\right)\right)} \tag{3.40}$$

Richardson plots can exhibit non-linear behavior at low temperatures, often caused by additional current mechanisms beyond thermionic emission. Such non-linearity may also occur when the barrier height and ideality factor vary with temperature [64].

3.6.1.3 Capacitance-Voltage Method

According to Goodman et. al., capacitance per unit area of a Schottky Barrier Diode can be written as [65],

$$\frac{C}{A} = \sqrt{\frac{\pm qK_s\epsilon_0(N_A - N_D)}{2(\pm V_{bi} \pm V - \frac{kT}{q})}} \tag{3.41}$$

where N_A is the acceptor concentration and ND is the donor concentration. The sign is positive when $N_A > N_D$ and the substrate is p-type and the sign is negative when $N_D > N_A$ and the substrate is n-type. For n-type substrates, both the built-in potential (V_{bi}) and the applied voltage (V) are negative under reverse bias. Conversely, for p-type substrates where V_{bi} and V are positive under reverse bias conditions. The relationship between built-in potential and barrier height is,

$$\phi_B = V_{bi} + V_0 \tag{3.42}$$

and V_0 can be expressed as,

$$V_0 = \frac{kT}{q} \ln\left(\frac{N_C}{N_D}\right) \tag{3.43}$$

where N_A is the effective density of states. In terms of intercept voltage (V_i) barrier height can be determined as,

$$\phi_B = -V_i + V_0 + \frac{kT}{q} \tag{3.44}$$

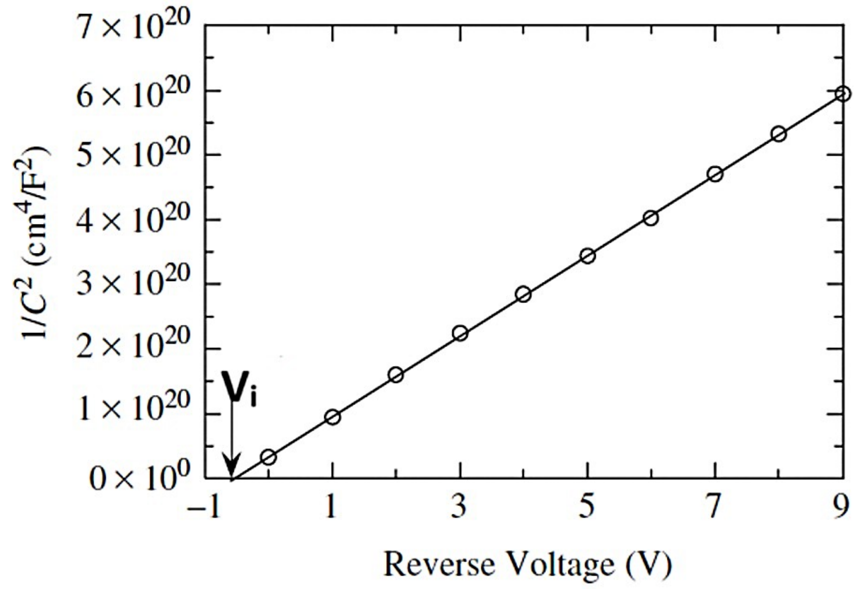


Figure 3.15: Room temperature measurement of reverse-bias $1/C^2$ versus voltage plot.

From the slope of $1/C^2$ versus V graph N_A can be determined. Additionally, the interception of the graph provides the value of V_i. These parameters are then used to determine ϕ_B.

Chapter 4

High conductivity β-Ga_2O_3 formed by hot Si ion implantation

Arka Sardar

This work is based on a collaborative research project with the Air Force Research Laboratory, under the guidance of Dr. Sarit Dhar, who served as the principal investigator. I would like to express my sincere gratitude to my co-authors—Mrs. Tamara Isaacs Smith, Dr. Neil Merrett, Dr. Ryan Comes, Mr. Jacob Lawson, and Dr. Thaddeus Asel—for their valuable contributions and support throughout the course of this work and during the publication process. The major content of this chapter is based on my previously published work[66].

4.1 Abstract

This work demonstrates the advantage of carrying out silicon ion (Si+) implantation at high temperature for forming controlled heavily doped regions in gallium oxide. Room temperature (RT, 25 °C) and high temperature (HT, 600 °C) Si implants were carried out into MBE grown (010) β-Ga_2O_3 films to form 350 nm deep Si-doped layers with average concentrations up to 1.2 x 10^{20} cm^{-3}. For such high concentration, the RT sample was too resistive for measurement, but the HT samples had 82.1% Si dopant activation efficiency, with a high sheet electron concentration of 3.3 x 10^{15} cm^{-2} and excellent mobility of 92.8 $cm^2/V.s$ at room temperature. X-ray diffraction measurements indicate that HT implantation prevents the formation of other Ga_2O_3 phases and results in reduced structural defects and lattice damage. These results are highly encouraging for achieving ultra-low resistance heavily doped Ga_2O_3 layers using ion implantation.

4.2 Introduction

Ga_2O_3 is emerging as a promising wide bandgap semiconductor material and is attracting significant attention from the research community for power electronic applications ([10],[11],[12]). Among the different phases, the monoclinic β phase is thermally the most stable, with a reported bandgap of 4.6-4.9 eV 4,and a breakdown electric field of 8 MeV/cm 5, which is much higher compared to SiC and GaN. β-Ga_2O_3 has robust chemical resistance and radiation hardness, which are attractive for devices operating in harsh environments [37]. In addition, the prospect of low-cost mass production due to floating zone (FZ)[28] and edge-defined film-fed (EFG)[28] growth method is also a key advantage for this material.

Ion implantation is attractive for device processing as it offers a way to selectively dope different regions of a material with precise control of dopant concentration and profile [13]. Sasaki et al. [67] performed Si implantation into β-Ga_2O_3 (010) at room temperature with concentrations ranging from 10^{19} to 10^{20} cm^{-3} followed by anneals ranging from 700 to 1100 °C. The highest carrier concentration and lowest resistivity was achieved for samples implanted with 5 x 10^{19} cm^{-3} and annealed at 1000 °C. The ratio of the free electron concentration to the total amount of Si in Ga_2O_3 (activation efficiency, η was found to be 63% for 5 x 10^{19} cm^{-3} implant concentration. However, for concentration of 10^{20} cm^{-3}, a severe drop of η to 6% was reported, which resulted in a resistivity even higher than samples with the lowest implanted concentration of 1 x 10^{19} cm^{-3}. These experiments seemed to define a maximum effective implanted concentration of 5 x 10^{19} cm^{-3} for room temperature implanted Si into β-Ga_2O_3. In the case of 4H-SiC, high-temperature Al^+ implantation results in a dramatic improvement of activation efficiency and conductivity over room temperature implantation due to lower defect densities and better recrystallization after annealing [68]. Also, improvement in electrical activation by high temperature ion implantation in Si is a well-established phenomenon [69]. In this work, it is demonstrated that ion implantation at elevated temperature can be used to efficiently dope β-Ga_2O_3 as well.

4.3 Experimental Procedure

To this end, 300 nm thick, unintentionally doped β-Ga_2O_3 films grown by AFRL on top of Fe doped semi-insulating substrate using a Veeco GEN Xcel plasma-assisted MBE (PAMBE) system equipped with a standard effusion cell for Ga and a UNI-Bulb RF plasma source for oxygen angled at the substrate at 45°relative to the substrate. The substrates were solvent cleaned prior to being inserted into the chamber. An O plasma clean was performed in the chamber prior to growth. The films were grown with a substrate temperature of 650 °C, a Ga beam equivalent pressure (BEP) of 8.0×10^{-8} Torr was used as it was calibrated to be near the stoichiometric conditions in our chamber, and an oxygen plasma produced with 1.55 sccm of oxygen flow and 250 W of RF power. The films were grown targeting a thickness of 300 nm with no intentional doping. Based on previous MBE runs, the doping and mobility of the film are estimated to be 2 x10^{16} cm^{-3} and 100 $cm^2/(V\text{-}s)$, respectively, giving an approximate sheet resistance of 1 x 10^5 $(\Omega)/\square$. Samples were implanted with 275 and 425 keV Si^+ ions targeting a box profile approximately 300 nm thick as shown in the SRIM profile in Fig.1. The SRIM [47] simulated profile for Si is shown in Fig. 1 that gave idea about two energies of implantation based on the targeted implant profile. The ion flux for the lower and higher energy was 4.61 x 10^{11} and 6.46 x 10^{11} $ions/cm^2/s$ respectively, maintaining identical beam current (1µA for both energies, with a chamber pressure of 3.0 x 10^{-6} Torr) for all the implants with total fluence of 2.4 x 10^{15} or 4.8 x 10^{15} cm^{-2}. To overcome the limitation of the lowest available Si+ beam energy in the pelletron accelerator that was used (lowest possible energy is 100 KeV), 110 nm of Mo was used as an energy reducing layer to enable doping of the film with the target SRIM profile. A 30 nm thick Al_2O_3 layer was used between Mo and β-Ga_2O_3 to prevent any Mo knock-ons into the β-Ga_2O_3. However, Al atoms get recoiled into the MBE film. Based on SRIM simulation this Al containing surface layer is 15 nm and likely to be thinner due to wet etching of the Al_2O_3 prior to annealing. Therefore, this layer is not likely to significantly impact the bulk electron transport results of the much thicker Si doped region. The implants were done with the sample holder at

21.6 °C (RT implants) and at 600 °C (HT implants). The temperature was measured at the back of the sample holder using a thermocouple. After implantation, the Mo and Al_2O_3 were removed by etching in hydrogen peroxide and a commercial (1:7) buffered oxide etch respectively. This was followed by annealing in flowing nitrogen at 970 °C for 30 minutes to anneal the implant damage and activate the dopants. Optical and Atomic Force Microscopy was performed after implantation and annealing. The RMS roughness, (R_q) was less than 1 nm for all samples. However, the higher fluence RT sample had long (mm) line-like features throughout the surface after annealing possibly due to surface reconstruction (see AFM and optical micrographs in the supplemental information) that require further investigation.

4.4 Result Discussion

Secondary ion mass spectrometry (SIMS) profiles of Si in samples implanted with a fluence of 4.8 x 10^{15} cm^{-2} at HT and RT before and after activation annealing are shown in Fig.1. The SIMS profiles are deeper than the simulated profile possibly due to partial channeling of the ions into the crystal lattice since the samples were not tilted during implantation. The RT implanted sample prior to annealing had a similar Si ion distribution to that of the as implanted HT sample. After annealing, however, Si concentration increased in HT, whereas it decreased for RT. More measurements are required to determine the reason for this or whether it is a real effect. Previously, it has been reported that ion-induced damage at the film/substrate interface results in enhanced out-diffusion of Fe from the substrate into the film [70]. This is observed here as well, but the Fe profiles are comparable for the RT and HT implantation after activation, as shown in Fig.1. The thickness of the conducting layer was considered as the depth at which the Si concentration falls to 10^{19} cm^{-3}, where compensation effects of Fe would not affect the conductivity. The dip of Fe profile in the MBE layer is likely due to the interplay between damage and diffusion [70] during annealing, but further investigation is needed for more evidence.

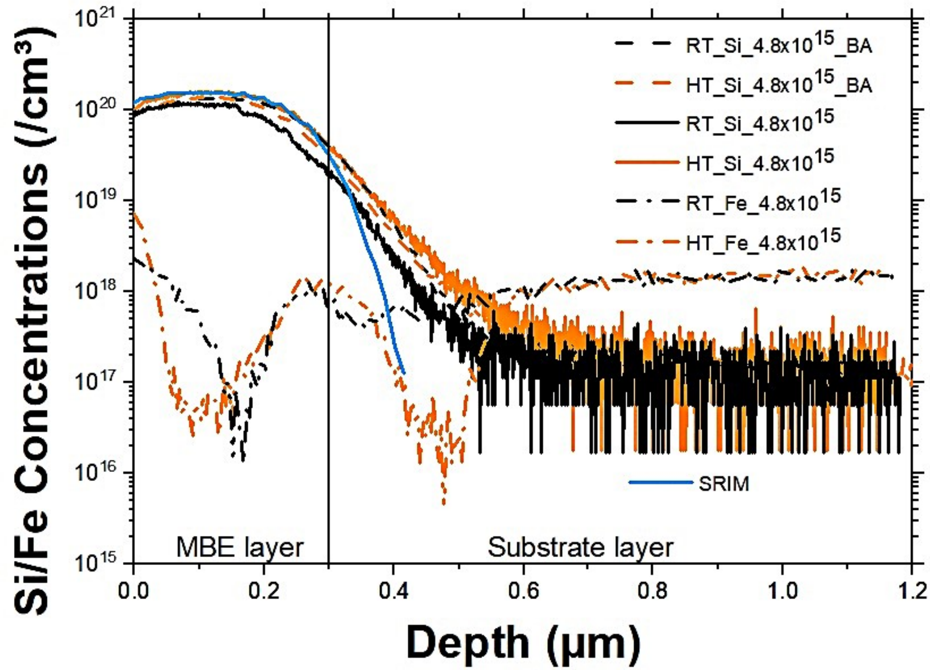


Figure 4.1: SIMS profiles of Si^+ in β-Ga_2O_3 implanted with 275 and 425 keV Si^+ ions with total fluence of 4.8 x 10^{15} cm^{-2} for RT and HT implanted samples before and after annealing. The Si SRIM simulated profile and SIMS of Fe after annealing for RT and HT implanted samples are also shown.

Figure 2 gave idea about two energies of implantation based on the targeted implant profile. Implantation through the Al_2O_3 overlayer causes Al ions to recoil into the Ga_2O_3 film possibly affecting the conductivity of the top 15 nm and likely to be thinner due to wet etching of the Al_2O_3 prior to annealing. As the MBE films are 300 nm thick and the Si doping concentration is $> 10^{20} cm^{-3}$, the Al containing surface layer is not likely to significantly impact the bulk electron transport results reported here, but we need further study to understand the effect of Al.

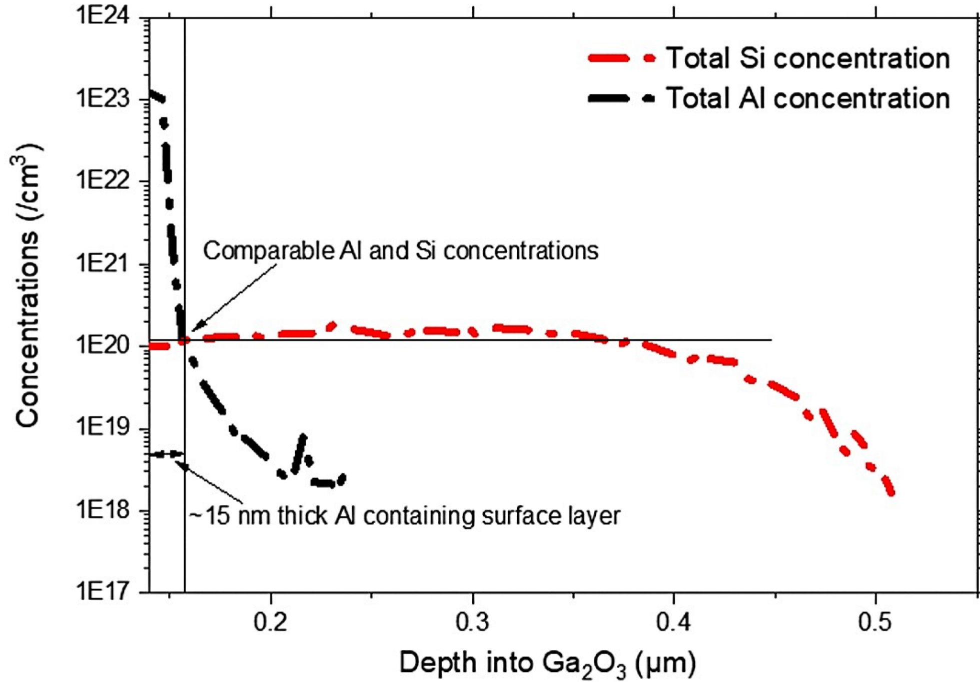


Figure 4.2: Concentrations of Al recoils and implanted Si profiles obtained from SRIM with a 30 nm layer of Al_2O_3 on top of Ga_2O_3 MBE film followed by 110 nm thick Mo layer as shown in the figure. Si ions were implanted at energies 275 and 425 keV with a total fluence of 4.8 x 10^{15} cm^{-2}.

Hall measurement was performed in the Van-der-Pauw configuration in the temperature range of 27 to 325 °C. The contacts were made by depositing Ti/Au at four corners of the nominally square sample followed by annealing in an argon (Ar) atmosphere at 550 °C for 5 minutes. Multiple measurements were made, and the average values are reported here with the error bars representing the standard deviation of the measurements. Figure 3 shows that the sample implanted at high temperature with the higher fluence has the lowest sheet resistance of 20.8±0.68 (Ω)/□ at 27 °C. On the other hand, the higher fluence RT implanted sample was too resistive for measurement. For the lower fluence, the HT and RT samples had sheet resistances of 41.4±8.24 and 51.3±1.4 respectively, at 27 °C. At higher temperature, overall resistance increased for all samples, but the HT implanted samples-maintained advantage even at 325 °C.

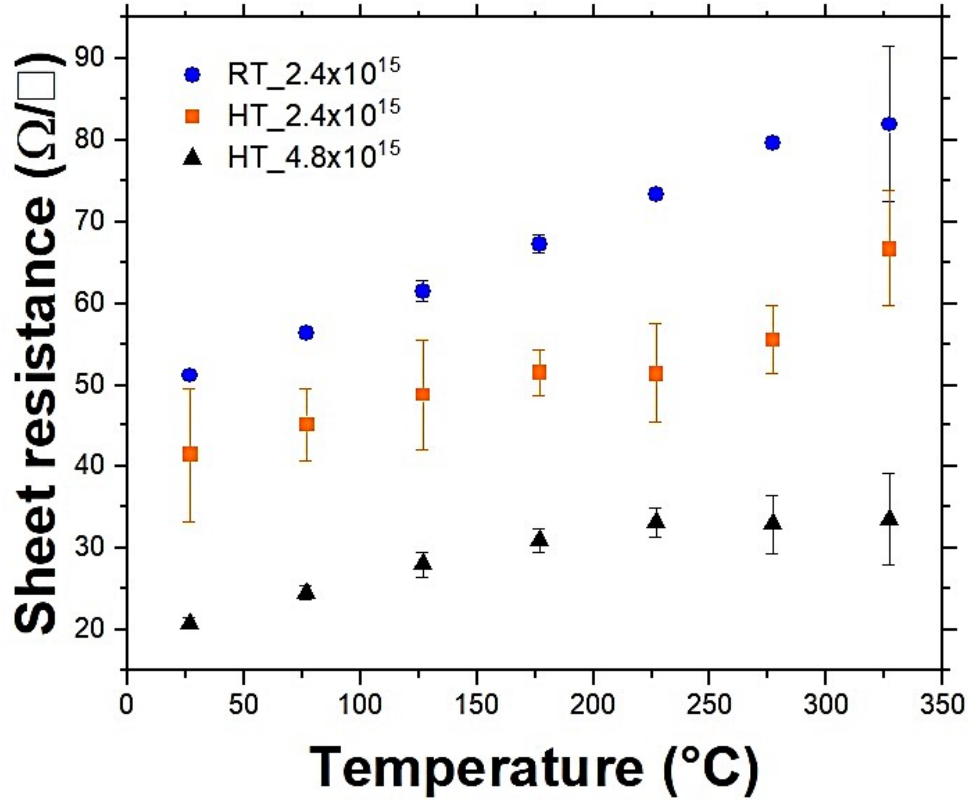


Figure 4.3: Sheet resistance versus temperature for samples implanted at HT and RT with total Si^+ fluences of 2.4 x 10^{15} and 4.8 x 10^{15} cm^{-2}. Error bars represent variation over four measurements.

The average sheet electron concentrations (n_s) are shown in Figure 4. In Table 1, the activation efficiencies η for all the samples are listed. Here, η was determined as the ratio of n_s and the total amount of Si obtained by integrating the SIMS profiles. For the lower fluence, RT and HT implanted samples, η is equal to about 68.2% and 76.3%, respectively, a modest advantage in favor of HT sample. Remarkably, for the higher fluence HT sample, η The likely reason for maintaining the high η is the reduction of ion induced compensating defects such as vacancies, interstitials, and/or their complexes by high temperature implantation.

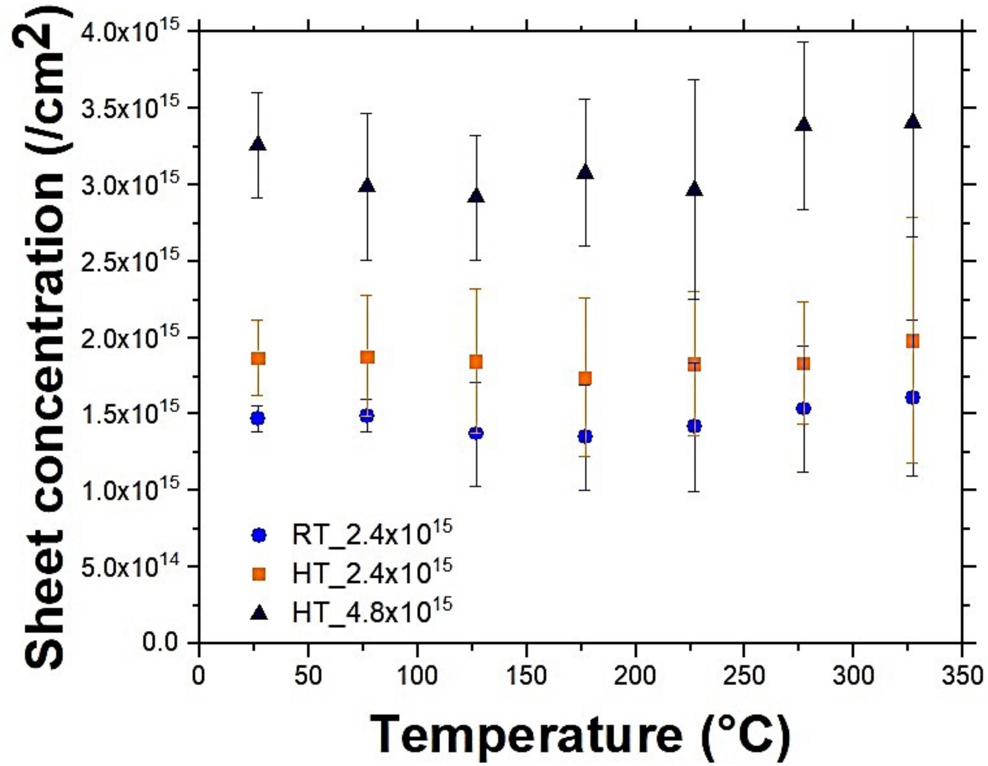


Figure 4.4: Sheet charge concentration versus temperature for samples implanted at HT and RT with total Si^+ fluences of 2.4 x 10^{15} and 4.8 x 10^{15} cm^{-2}. Error bars represent variation over four measurements.

Figure 5 shows the electron Hall mobility as a function of temperature. For the lower fluence, mobility of HT and RT samples are 80.2±1.1 and 82.8±2.14 $cm^2/V.s$ respectively at 27 °C. For the higher fluence, the mobility increases to 92.8±5.64 $cm^2/V.s$ (at 27 °C). This unusual trend of mobility increasing with higher electron concentration could be due to enhanced screening of the electron phonon-scattering by the increased carrier density[71] and requires further investigation.

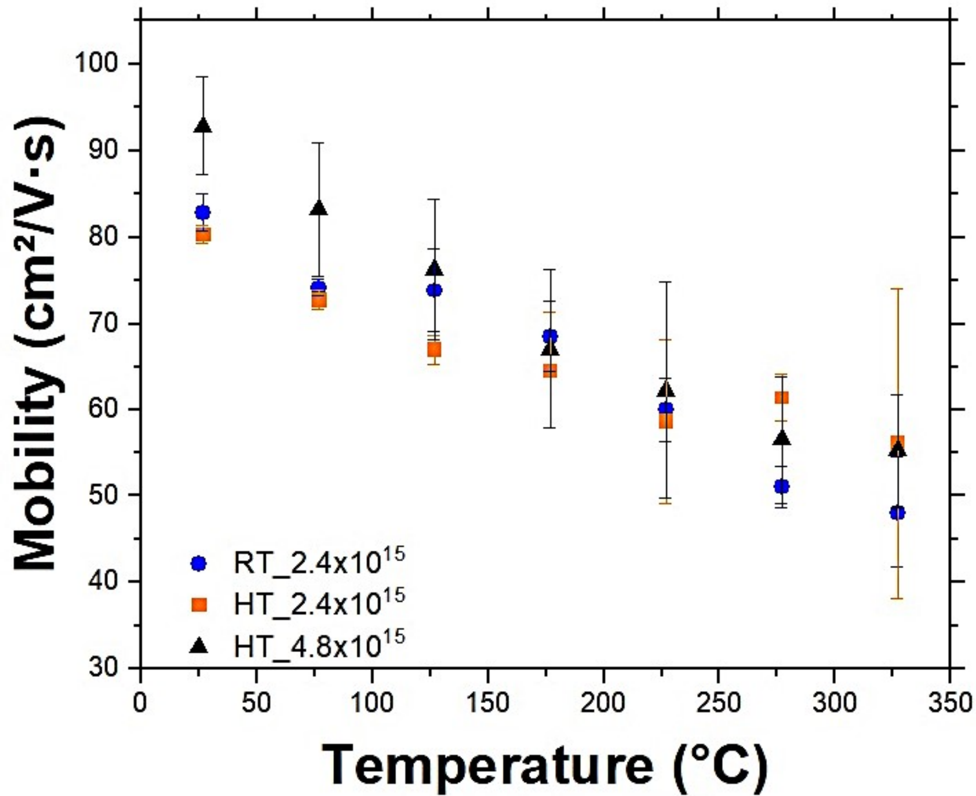
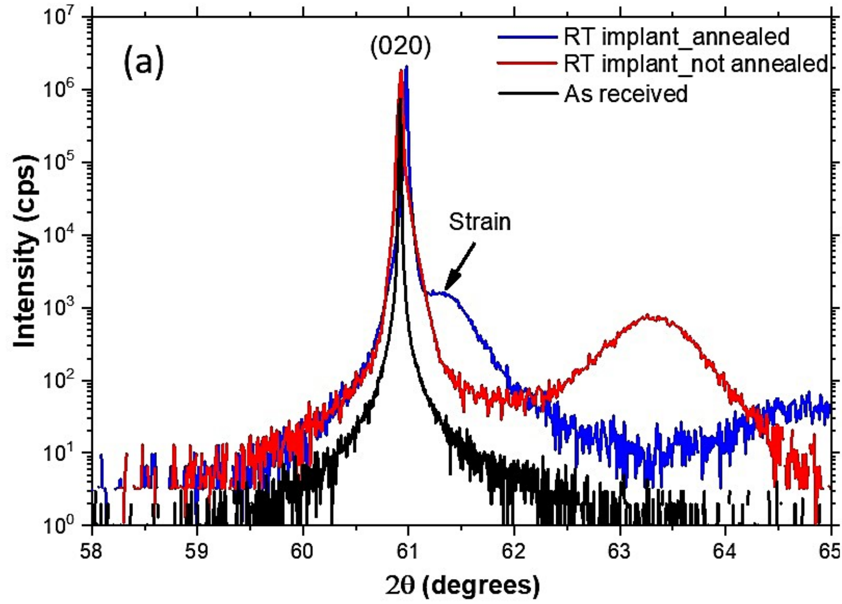
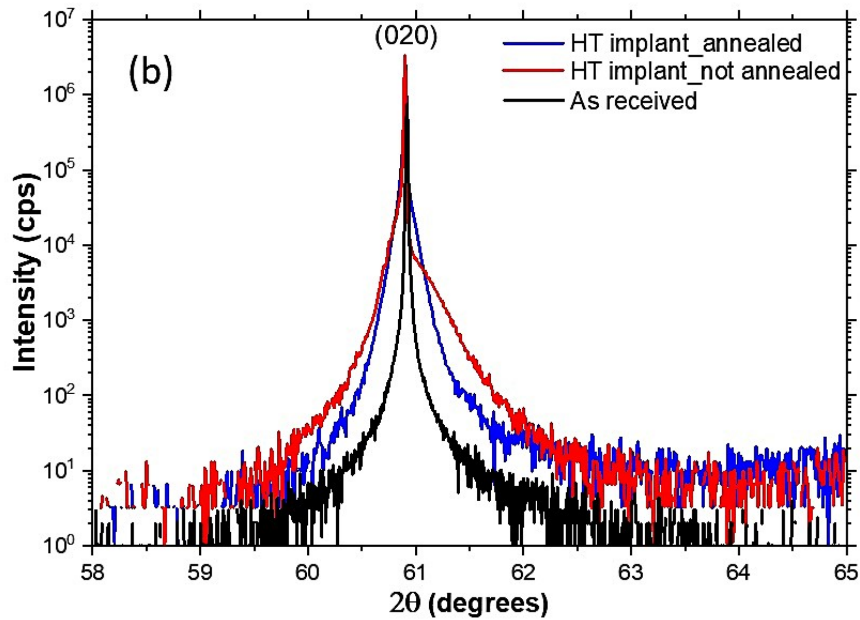


Figure 4.5: Electron mobility versus temperature for HT and RT implanted samples total fluences of Si^+ ions of 2.4 x 10^{15} and 4.8 x 10^{15} cm^{-2}. Error bars represent variation over four measurements.

To study the crystal quality and strain, x-ray diffraction was performed using a Rigaku SmartLab XRD system using a Ge (220)x2 monochromator. Figure 6 shows HRXRD data for the higher fluence samples at the three different stages: as received, after Si implantation and after the activation annealing. The excellent crystal quality of the as received homoepitaxial samples is evident in the FWHM value of 52.5 arc sec corresponding to the (020) peak. After RT Si implantation (red in Fig.5a), the FWHM increased to 122 arc sec consistent with ion implantation induced defect creation and strain. An additional broader peak with a FWHM 196.5 arc sec also appeared centered at 63.3°which indicates the formation of a different phase; identified in the literature as κ-Ga_2O_3([72],[73]) or γ-Ga_2O_3[74]. On the other hand, no additional phase is observed for HT implantation (red in Fig.5b) but broadening and distortion of the (020) peak is evident.



(a)



(b)

Figure 4.6: HRXRD data for Ga_2O_3 implanted with 4.8 x 10^{15} cm^{-2} Si^+ at (a) RT and (b) HT before and after annealing compared to the as-received MBE sample spectrum.

After the annealing at 970 °C the broader peak in RT samples (blue in Fig. 5 a) disappears, but an additional side shoulder appears at an angle higher than the original peak

position, along with a shift of the (020) peak, which can be attributed to the accretion of compressive strain in previous studies([72],[75],[76],[77]), although due to the strong anisotropy of Ga_2O_3 it does not necessarily hold for other orientations. The strain peak is significantly smaller in the HT samples after annealing (blue in Fig. 5b). However, the ion damage is not completely recovered, possibly due to the residual strain[41] suggesting optimization of the process is further needed. For the lower dose samples, similar effects were observed, and the results are included in the supplementary material.

In conclusion, we have demonstrated the advantage of HT ion implantation for forming heavily doped ($> 10^{20} cm^{-3}$) n-type regions in β-Ga_2O_3 devices and resistivity as low as 0.68 mΩ·cm. Using Si^+ as the dopant, we observe a substantial increase in sheet electron concentration and consequently a significantly lower sheet resistance compared to room temperature implantation. In addition, HRXRD shows that HT implantation causes reduced structural defects and strain in the implanted layer by preventing formation of any other phase. Being able to maintain the high mobility for carrier concentration above 10^{20} cm^{-3} due to the impressive dopant activation efficiency, makes it pertinent to further investigate the limits of high temperature ion implantation in β-Ga_2O_3.

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Chapter 5

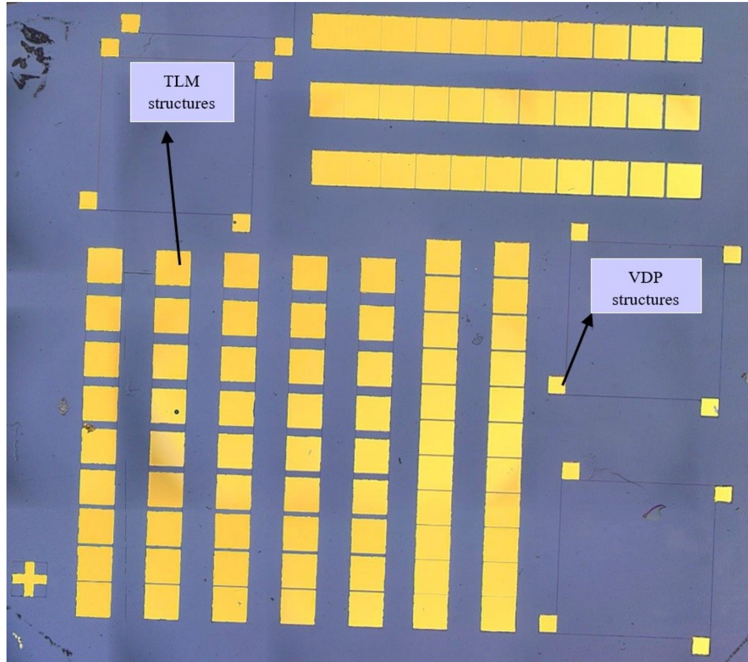
Transfer Length Method and Schottky Barrier Diode fabrication

5.1 TLM contact formation on Si implanted samples

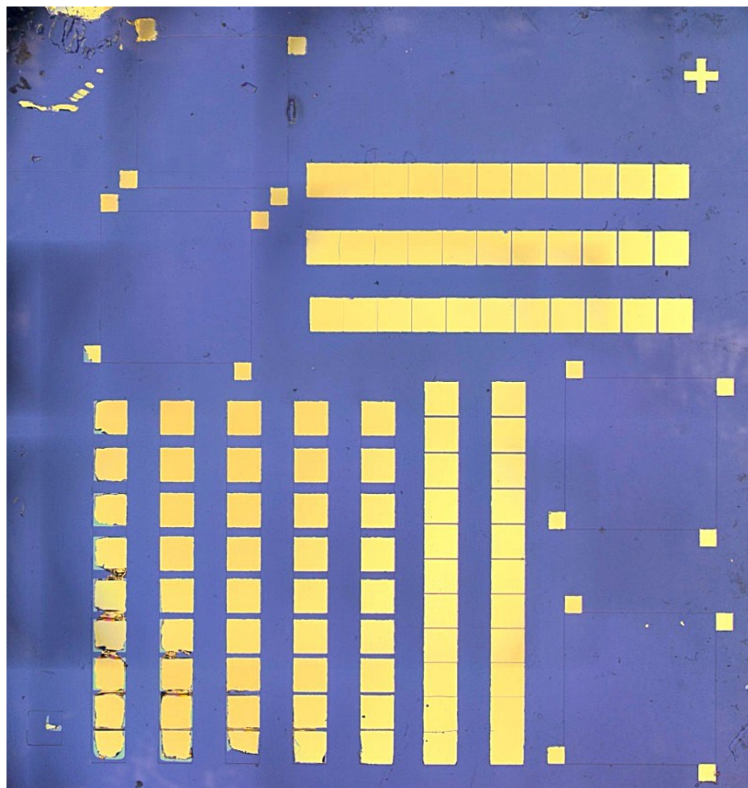
For this experiment Fe doped β-Ga_2O_3 substrate was used. The samples were implanted with Si^+ ions at energies of 275 and 425 keV to achieve a target doping profile approximately 300 nm thick, as confirmed by SRIM simulations. Implantations were performed with ion fluxes of 4.61×10^{11} and 6.46×10^{11} ions/cm^2/s, using a beam current of 1 μA at a chamber pressure of 3.0×10^{-6} Torr. The total fluence was 4.8×10^{15} ions/cm^2. A 110 nm Mo energy-reducing layer was added, along with a 30 nm Al_2O_3 buffer layer to prevent Mo contamination of the β-Ga_2O_3 film. Implantations were carried out at elevated temperature (600 °C), with temperatures monitored via a thermocouple. Post-implantation processing involved removing Mo and Al_2O_3 layers with hydrogen peroxide and buffered oxide etch, followed by a nitrogen anneal at 970 °C and 1050 °C for 30 minutes to repair implant damage and activate dopants.

Following activation annealing, ohmic contacts were fabricated on the samples and Ti/Au contacts were used in this process. A photoresist layer was spin-coated onto the sample surface to define regions for etching through a mesa etch mask. Protective molybdenum (Mo) and nickel vanadium (NiV) layers were sputtered onto the surface to shield the β-Ga_2O_3 regions designated for metal contact. After deposition, a lift-off process was employed to remove excess material, ensuring precise patterning. The samples underwent reactive ion etching (RIE) in a nitrogen trifluoride (NF_3) plasma for 20 minutes, achieving an etch depth of approximately 400 nm. Following the etching, the protective Mo and NiV layers were removed using sequential chemical treatments with nickel etchant and hydrogen peroxide. This process exposed the intended β-Ga_2O_3 regions for further metal deposition.

To create robust electrical contacts, a 60 nm Ti layer was deposited, followed by a 150 nm Au layer for conductivity. After metal deposition, the samples underwent annealing in a high-vacuum chamber at 10^{-7} Torr with ultra-high purity nitrogen gas. The temperature was ramped to 450 °C within one minute and held for another minute to optimize the electrical contact properties. This annealing process enhanced the quality of the contacts and activated the interfaces, crucial for the TLM patterns. After fabrication, the final image of the devices has been shown in figure 5.1. Only TLM patterns were used to measure I-V characteristics, we didn't measure the VDP structures on the devices.



(a)



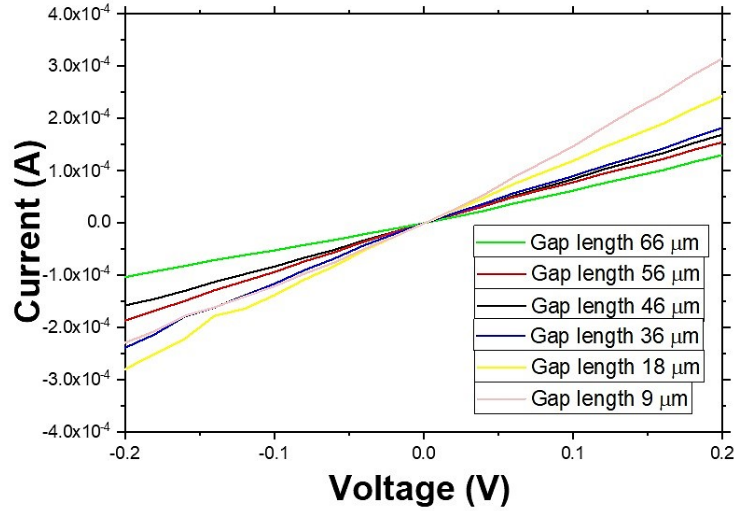
(b)

Figure 5.1: TLM and Van der Pauw (VDP) structure after Ti/Au metal deposition for the sample annealed at (a) 970 °C and (b) 1050 °C.

5.1.1 I-V result analysis

5.1.1.1 Sample annealed at 970 °C

Figure 5.2(a) presents the I-V characteristics of one of the fabricated TLM strip, measured across various TLM pads. A subset of these results is shown to highlight the electrical behavior of the sample. The sample annealed at 970 °C prior to TLM fabrication exhibited a linear I-V response between -0.2 V and +0.2 V, confirming that the Ti/Au electrodes form ohmic contacts. This linearity indicates efficient charge carrier transport at the metal-semiconductor interface, a critical requirement for accurate TLM analysis. The total resistance between adjacent electrodes was extracted from the I-V plots to further analyze the sample's electrical properties.



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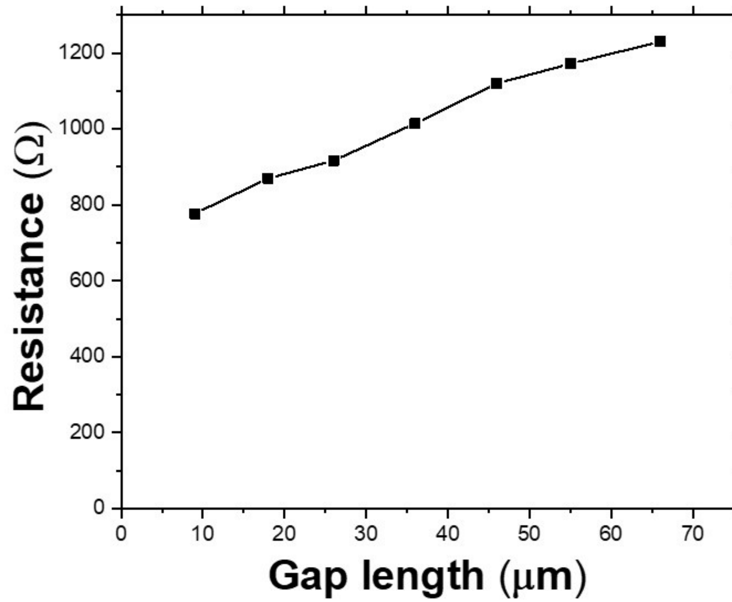
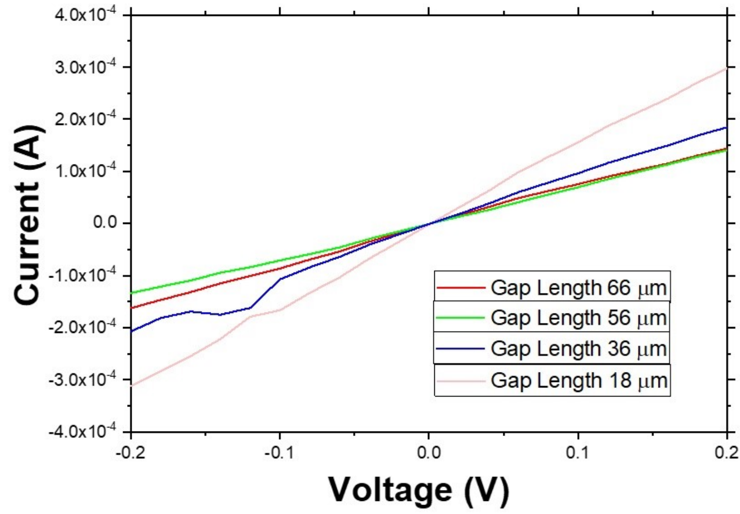


(b)

Figure 5.2: (a) I-V measurement data and (b) resistance versus gap length for Si implanted sample with concentration of 1 x 10^{20} /cm^3 and annealed at 970 °C temperature. Ti/Au contacts were annealed at 450 °C for 1 minute.

Figure 5.2(b) shows the total resistance as a function of electrode spacing for the sample, enabling the determination of key parameters such as sheet resistance (R_{sh}), contact resistance (R_c), and specific contact resistivity. Based on the slope of the resistance vs. spacing plot, the sheet resistance was calculated to be 1629.7 Ω/□. The y-intercept of the plot at

zero spacing provided the contact resistance value of 359.5 Ω. Additionally, the transfer length (L_T), a measure of the distance over which current transfers from the metal to the semiconductor, was determined to be 45 μm. The specific contact resistivity, a parameter indicating the quality of the contact interface, was calculated to be 3.3×10^{-2} Ω·cm^2.



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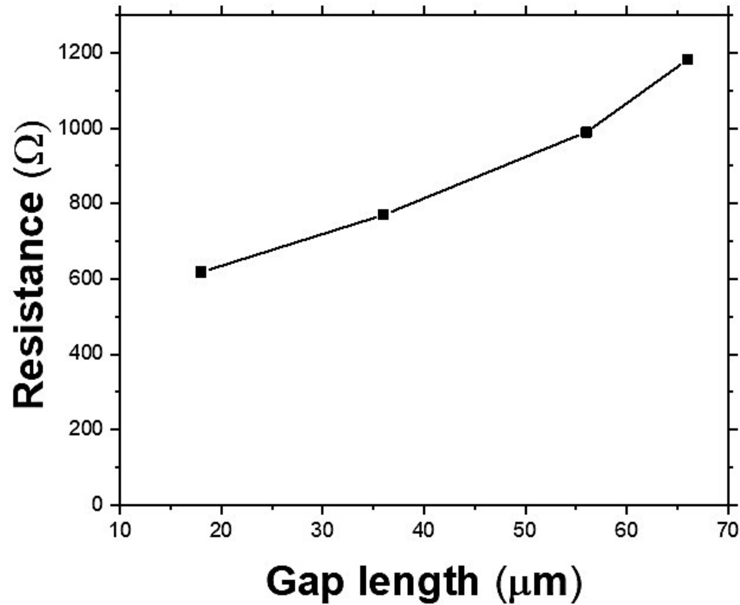


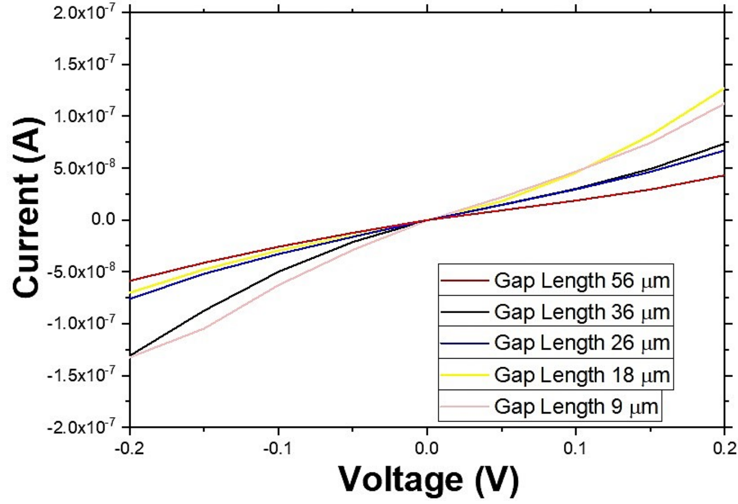
(b)

Figure 5.3: (a) I-V measurement data and (b) resistance versus gap length for Si implanted sample.

These findings show the effectiveness of the annealing process and the Ti/Au contacts in achieving desirable electrical properties for the fabricated TLM structure. I-V measurement from another TLM strip and corresponding resistance versus gap length plot has been shown in figure 5.3(b) which is consistent with the result shown in figure 5.2(b).

5.1.1.2 Sample annealed at 1050 °C

Figure 5.4 illustrates the I-V characteristics of a fabricated TLM strip, measured across multiple TLM pads. The linear I-V response observed within the voltage range of -0.2 V to +0.2 V for the sample annealed at 1050 °C prior to TLM fabrication confirms the formation of ohmic contacts by the Ti/Au electrodes. But compared to the sample annealed at 970 °C, the samples look more resistive. The possible reason could be the 'Over Annealing' of the sample. Previous studies have indicated that excessive annealing in implanted samples can lead to a reduction in active carrier concentration and a corresponding decline in mobility[78]. Jacobs et al. reported the importance of annealing temperature and its effect for Aluminum Gallium Oxide, which is similar to β-Ga_2O_3[79].



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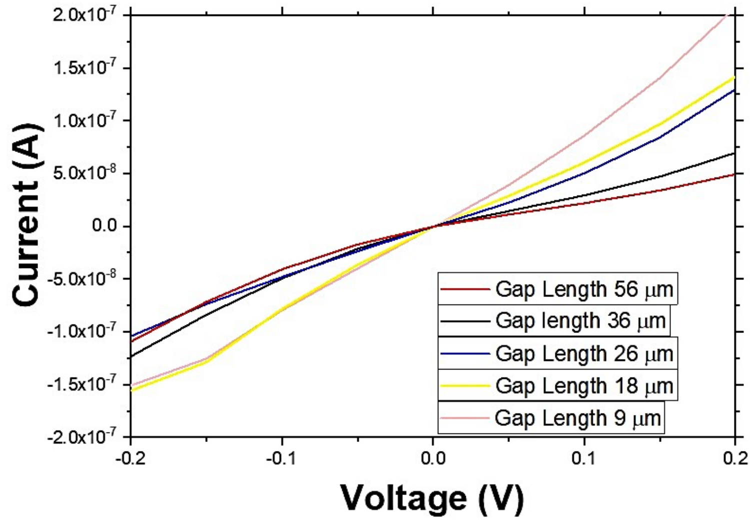


(b)

Figure 5.4: I-V measurement data for Si implanted sample with concentration of 1 x $10^{20}/cm^3$ and annealed at 1050 °C temperature. Ti/Au contacts were annealed at 450 °C for 1 minute.

5.2 Schottky Barrier Diode fabrication on Si doped β-Ga_2O_3 sample

The sample used in this study was a square piece (5 mm × 5 mm) diced from a 2-inch diameter, 680 μm thick, n-type β-Ga_2O_3 single crystal wafer doped with Si (2.8 × 10^{17} cm^{-3}), grown using the EFG method and sourced from Tamura Corporation, Japan [3]. The plane orientation of the sample was ($\bar{2}01$). Initial cleaning was performed using acetone, methanol, and deionized (DI) water, followed by a 15-minute Piranha etch (H_2SO_4 and H_2O_2 in a 1:1

ratio) and a 1-minute dip in buffered oxide etchant (BOE). The sample was then rinsed with DI water and dried with N_2 gas before proceeding to photolithography. Circular patterns with a diameter of 80, 210 and 350 μm were transferred onto the substrate using AZ 5214 E photoresist, a chrome photomask, and a MJB3 Karl Suss mask aligner. The exposed photoresist was developed with AZ 726 MIF, followed by DI water rinsing and nitrogen drying. For the measurement only patterns with bigger diameters were used. A picture of the SBD is shown in figure 5.5.

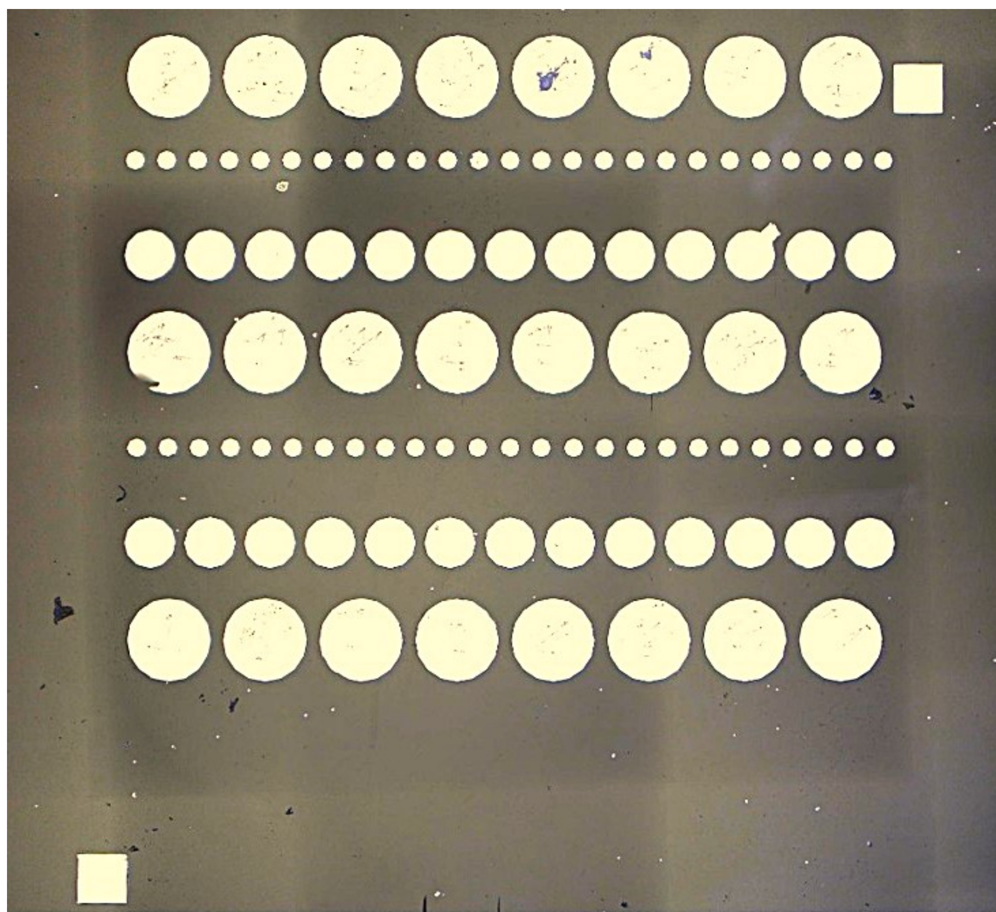
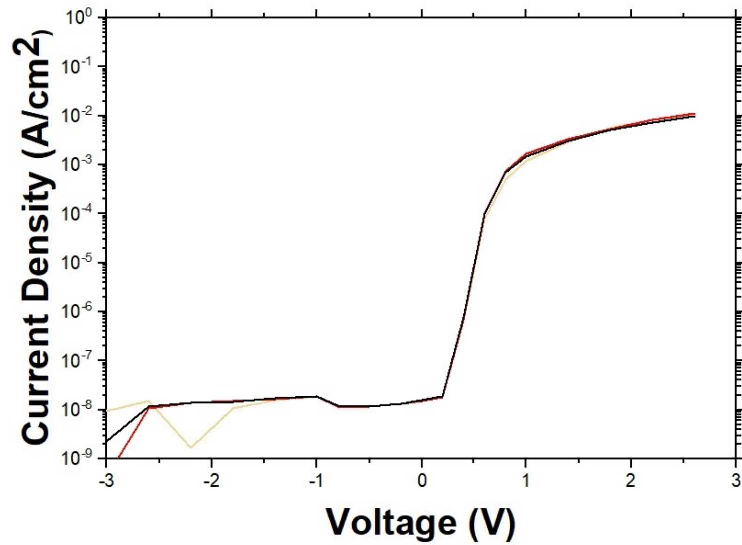


Figure 5.5: Schottky Barrier Diodes structures on (-201) β-Ga_2O_3 substrate with Al/Ti/NiV contact on top and Ti/Al ohmic metal at the back.

An Al/Ti/NiV (150 nm/40 nm/40 nm) film was deposited by DC magnetron sputtering at a low pressure of 3.0×10^{-7} Torr to form Schottky contacts. The lift-off process, performed by dipping and sonicating the sample inside acetone, resulted in well-defined circular Ni

contacts. For the ohmic contact, a Ti/Al layer was deposited on the backside of the sample. The sample was then mounted on a gold-plated ceramic plate using conductive silver paint for electrical measurements. Current-voltage (I-V) measurements were conducted from room temperature to 373 K using a Current-voltage (I-V) measurements were conducted from room temperature to 373 K using a Keithley 6517 electrometer/high resistance system, while capacitance-voltage (C-V) characteristics were measured at room temperature using a Keithley 590 CV analyzer.



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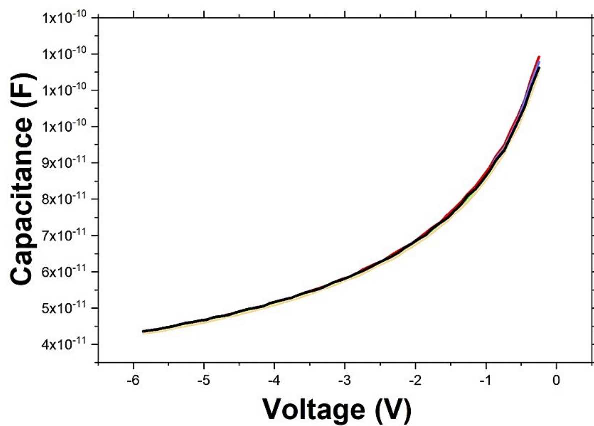

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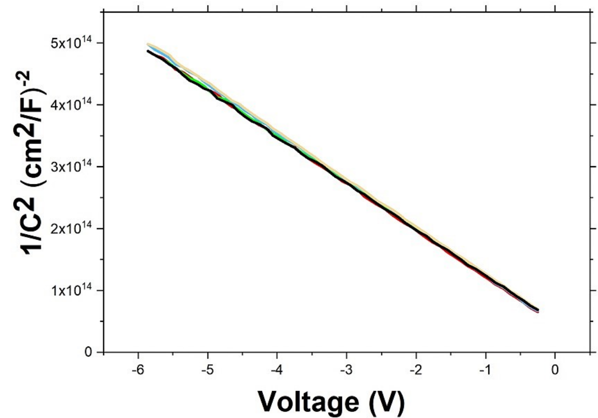


(c)

Figure 5.6: (a) I-V trace; (b) room temperature C-V characteristics; (c) room temperature $1/C^2$ versus V plot of Al/Ti/NiV Schottky diode.

Figure 5.6(a) depicts the current-voltage (I-V) characteristics of the fabricated Schottky barrier diode (SBD) devices. The I-V traces demonstrate excellent rectifying behavior, with a rectification ratio of 10^5, indicating a high level of diode efficiency. Additionally, the turn-on voltage was observed to be close to 1 V. These results highlight the quality of the metal-semiconductor interface and the effectiveness of the fabrication process in achieving desirable electrical characteristics.

Capacitance-voltage (C-V) measurements were also performed to assess the carrier concentration, yielding a value of 1.9×10^{17} cm^{-3}. This calculated carrier density closely matches the intended doping level of silicon in the sample, reported as 2×10^{17} cm^{-3}. The agreement between the measured and nominal carrier concentrations confirms the uniform incorporation of Si dopants during crystal growth. These findings validate both the material quality and the reliability of the measurement techniques used. Overall, the combination of excellent rectification, appropriate turn-on voltage, and accurate doping concentration indicates that the fabricated SBD devices are well-suited for potential applications requiring efficient and reliable rectifying behavior.

Chapter 6

High Temperature Ge Ion Implantation in β-Ga_2O_3

This project was performed in collaboration with University of California, Santa Barbara (UCSB), National Renewable Energy Laboratory (NREL), University of Delaware (UD). We received the samples from UCSB, NREL helped us with STEM measurement and we used the SIMS facility at UD. The ion implantation was performed at Auburn University by Mrs. Tamara Isaacs-Smith and Mr. Max Cichon and we used XRD facility at Auburn university to run XRD analysis.

6.1 Introduction

Ion implantation has been demonstrated as an effective method to enhance the performance of β-Ga_2O_3 devices, particularly by reducing contact resistance. Studies have investigated doping with Si and Sn ions [80], while Wong et al. ([81],[40]) utilized deep-level impurities such as nitrogen (N) and magnesium (Mg) for current blocking in vertical MOSFETs. However, complete recovery of implantation-induced structural damage remains uncertain even after annealing at temperatures ranging from 900 to 1150 °C. Wendler et al. [82] reported the formation of point defects and non-amorphous defect clusters in β-Ga_2O_3 following P, Ar, and Sn implantation, indicating the potential formation of a new Ga_2O_3 phase.

Additionally, Wong et al. [70] observed that implantation damage increased the diffusivity of Fe in adjacent layers due to defect migration during annealing. Sharma et al. [83] highlighted the significant influence of annealing ambient on the diffusivity of implanted Sn and Ge in β-Ga_2O_3, with O_2 ambients promoting redistribution and N_2 ambients suppressing it. These findings underscore the importance of understanding implantation-induced

damage and defect behavior in β-Ga_2O_3, as compensating defects like gallium vacancies can significantly affect material properties.

Tetzner et al. demonstrated that nitrogen ion implantation into epitaxial β-Ga_2O_3 layers with an initial electron concentration of 2×10^{18} cm^{-3} forms a semi-insulating layer due to radiation defects. Conductivity nearly returned to its original level after higher-temperature annealing, confirming that radiation-induced defects were responsible for conductivity compensation [41]. Furthermore, nitrogen implantation reduces electron concentration in β-Ga_2O_3, but low nitrogen activation at 900 °C suggests the need for higher annealing temperatures, with compensation dependent on both implantation dose and annealing conditions [84].

In this study, unintentionally doped (010) β-Ga_2O_3 Molecular Beam Epitaxy (MBE) grown films were implanted with Ge ions at multiple energies to achieve a peak dopant concentration of approximately 10^{19} cm^{-3}. To repair implantation-induced damage and activate the dopants on substitutional lattice sites, the samples underwent annealing at 970 °C for 30 minutes in an N_2 ambient. Post-implantation and annealing, the samples were analyzed using secondary ion mass spectrometry (SIMS), high-resolution X-ray diffraction (HRXRD), and cross-sectional transmission electron microscopy (TEM). Electron Paramagnetic Resonance (EPR) at University of Alabama, Burmingham and optical ellipsometry at Pacific Northwest National Laboratory (PNNL) were performed to understand the defect and doping characteristics further, but no conclusive results were obtained from those measurements.

6.2 Experimental Procedure

To this end, 350 nm thick, unintentionally doped β-Ga_2O_3 films grown on top of Fe doped semi-insulating substrate using plasma-assisted MBE system at the University of California Santa Barbara. The films were grown with a substrate temperature of 700 °C. The films were grown targeting a thickness of 350 nm with no intentional doping. Prior to growth, samples were implanted with 325 and 675 keV Ge ions targeting a box profile

approximately 350 nm thick. To overcome the limitation of the lowest available Ge beam energy in the pelletron accelerator that was used (lowest possible energy is 100 KeV), 110 nm of Mo was used as an energy-reducing layer to enable doping of the film with the target SRIM profile. A 30 nm thick Al_2O_3 layer was used between Mo and β-Ga_2O_3 to prevent any Mo knock-ons into the β-Ga_2O_3. However, Al atoms get recoiled into the MBE film. As observed in SIMS analysis. The implants were done with the sample holder at 21.6 °C (RT implants) and 600 °C (HT implants). The temperature was measured at the back of the sample holder using a thermocouple. After implantation, the Mo and Al_2O_3 were removed by etching in hydrogen peroxide and a commercial (1:7) buffered oxide etch respectively. This was followed by annealing in flowing nitrogen at 970 °C for 30 minutes to anneal the implant damage and activate the dopants.

6.3 Results and Discussions

6.3.1 SIMS analysis

Figure 1 presents the secondary ion mass spectrometry (SIMS) depth profiles of Ge in the sample implanted at high temperature (HT) with a fluence of 1.5×10^{15} cm^{-2}, following activation annealing. The measured SIMS profiles extend deeper into the substrate compared to the simulated profiles. A previous study attributed this discrepancy to partial ion channeling within the crystal lattice, as the samples were not tilted during implantation [66]. This phenomenon allows implanted ions to penetrate deeper than expected.

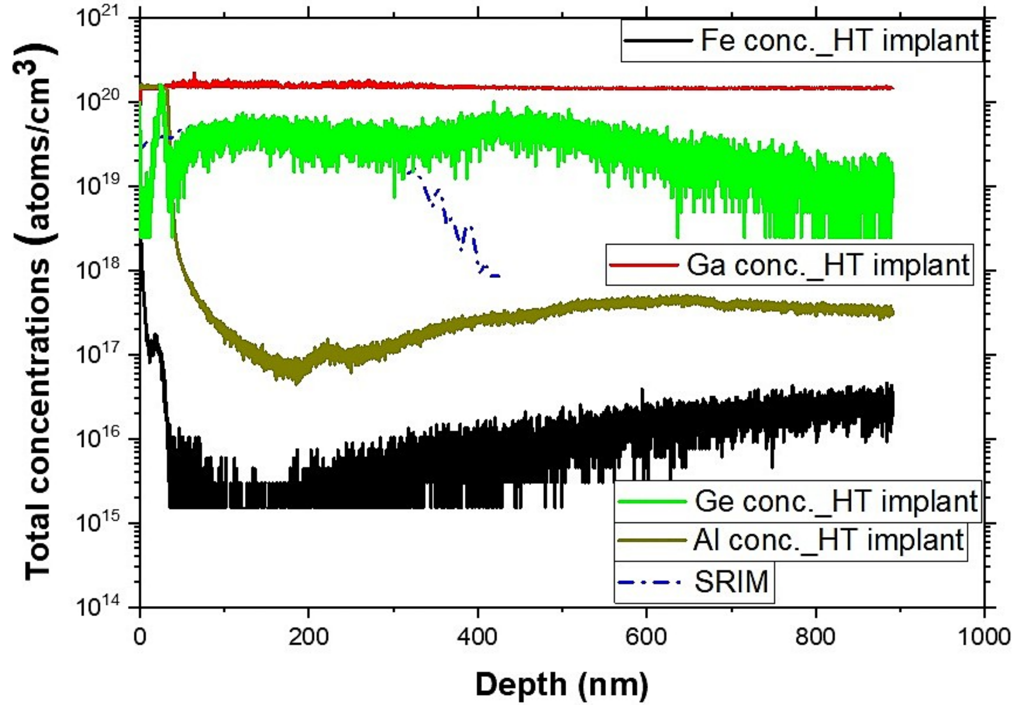


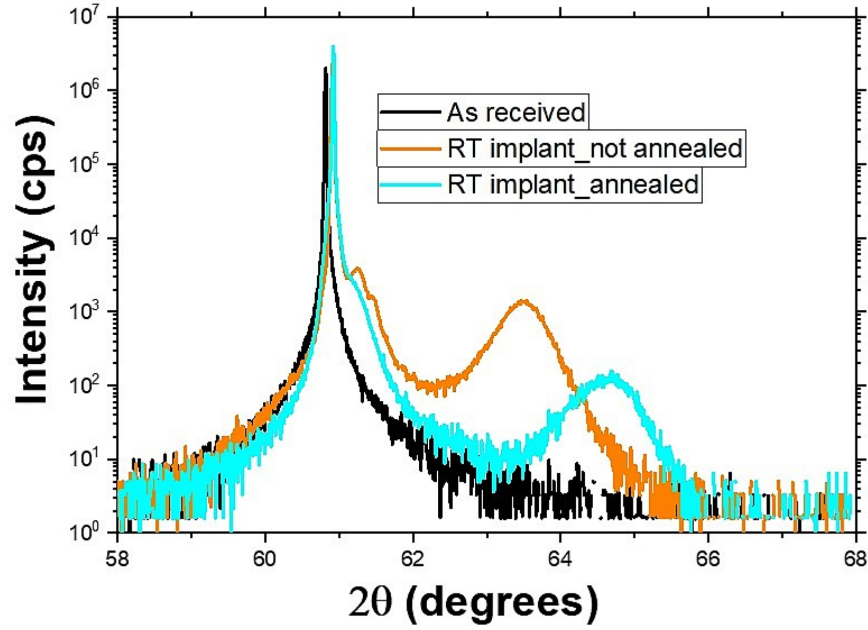
Figure 6.1: SIMS profiles of Ge in β-Ga_2O_3 implanted with 325 and 675 keV with total fluence of 1.5 x 10^{15} cm^{-2} for HT implanted sample after annealing. The Si SRIM simulated profile and SIMS of Fe, Al, and Ga after annealing HT implanted samples are also shown.

Additionally, prior research has indicated that implantation-induced damage at the film/substrate interface can facilitate the out-diffusion of Fe from the substrate into the film ([70],[85]). A similar effect is observed in this study, where Fe migration into the implanted layer is evident. Furthermore, Al incorporation is detected within the top 30 nm of the surface. In our earlier study, we found that ion implantation through an Al_2O_3 overlayer can lead to Al ions recoiling into the β-Ga_2O_3 film, potentially influencing the electrical properties of the top layer.

To assess the impact of implantation on conductivity, Hall measurements were attempted; however, the sample exhibited high resistivity, preventing accurate conductivity measurements. A likely explanation for this increased resistivity is the unintentional incorporation of Al into the film. However, further investigation is required to fully understand the underlying mechanisms affecting the electrical properties of the implanted layer.

6.3.2 XRD analysis

X-ray diffraction (XRD) analysis was performed using a Rigaku SmartLab XRD system with a Ge (220)×2 monochromator to assess the crystal quality and strain in the samples. Figure 1 displays the XRD rocking curve measurements for three different stages: the as-received sample, post-Ge implantation, and after-activation annealing. The as-received homoepitaxial β-Ga_2O_3 sample exhibited exceptional crystal quality, as evidenced by a full width at half maximum (FWHM) of 30.1 arcseconds in the rocking curve measurement. However, after room-temperature (RT) Ge implantation, the FWHM increased to 31.8 arcseconds, suggesting the introduction of implantation-induced defects and strain. Interestingly, post-implantation annealing did not lead to a reduction in the FWHM, indicating that the defects were not fully recovered. In contrast, samples subjected to high-temperature (HT) implantation displayed less peak broadening, with the FWHM decreasing to 29 arcseconds. This suggests that HT implantation may mitigate defect formation and strain accumulation, potentially preserving better crystal quality compared to RT implantation.



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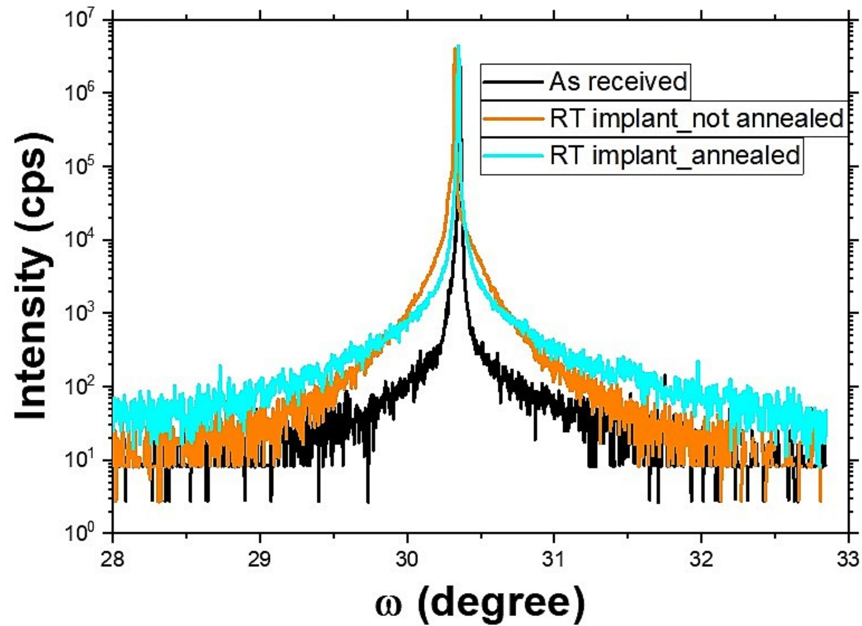
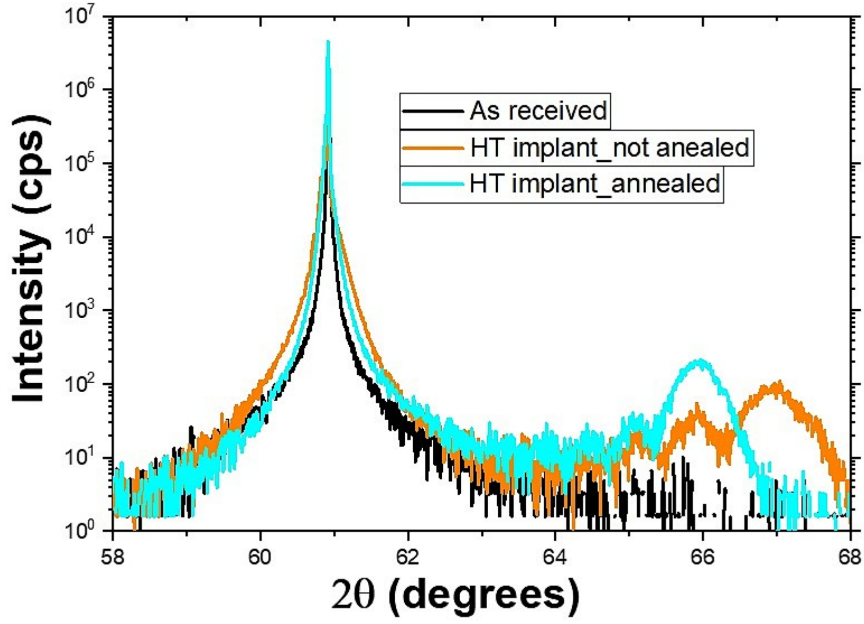


(b)

Figure 6.2: (a) HRXRD and (b) rocking curve data for Ge implanted β-Ga_2O_3 at RT, both before and after annealing, compared to the as-received MBE film.

HRXRD analysis identified an additional broad peak centered at 64.5°, suggesting the emergence of a secondary phase. Following annealing, this peak shifted to a higher diffraction angle but remained visible, accompanied by the appearance of a side shoulder. In the case

of high-temperature (HT) implantation, an extra peak was detected at 67°, which shifted to a lower angle after annealing. Although no side shoulder was observed for the HT-implanted sample, new diffraction peaks emerged between 64°and 66°in both implanted and annealed states. Further investigation is necessary to clarify the origin of these additional peaks. The side shoulder observed in the RT-implanted sample, along with the shift in the (020) peak, could be indicative of compressive strain accumulation, as suggested by previous studies. However, due to the pronounced anisotropy of β-Ga_2O_3, strain effects may vary depending on the crystal orientation.



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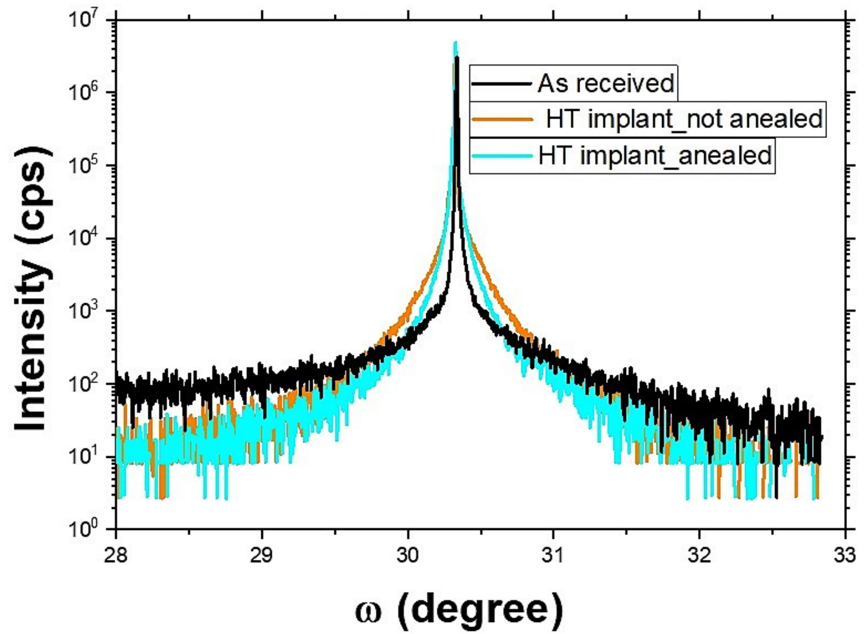


(b)

Figure 6.3: (a) HRXRD and (b) rocking curve data for Ge implanted β-Ga_2O_3 at HT, both before and after annealing, compared to the as received MBE film.

6.3.3 STEM analysis

Figure 2 presents the cross-sectional transmission electron microscopy (TEM) image of the high-temperature (HT) implanted β-Ga_2O_3 sample prior to annealing. The capping layers remained intact following implantation, allowing for a clear examination of the interface morphology. The image distinctly reveals the layered structure, including Mo, Al_2O_3, molecular beam epitaxy (MBE) β-Ga_2O_3, and the β-Ga_2O_3 substrate. Notably, the interface between Al_2O_3 and MBE β-Ga_2O_3 appears rough, which may be attributed to the incorporation of aluminum into the film during implantation. Previous secondary ion mass spectrometry (SIMS) analysis confirmed the presence of Al incorporation, supporting this observation.

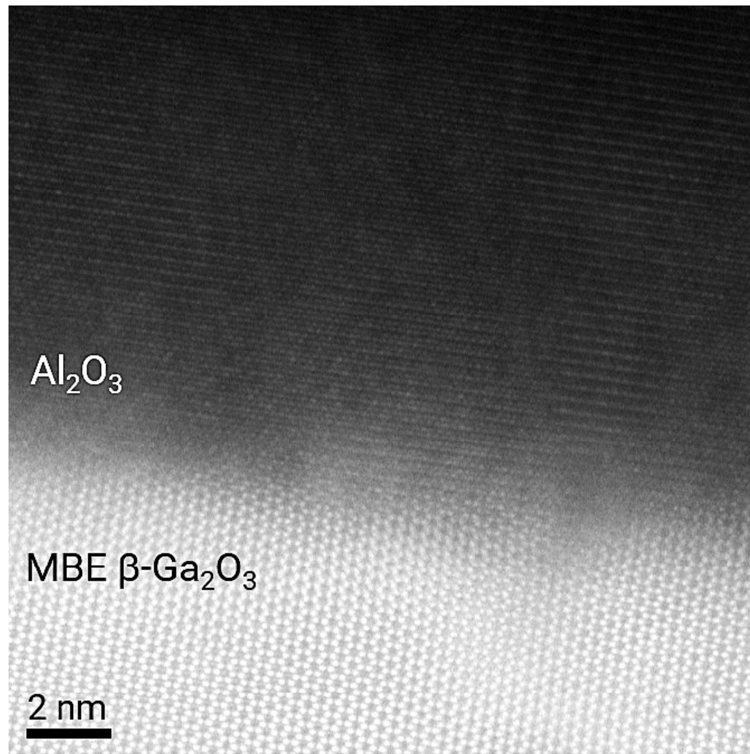
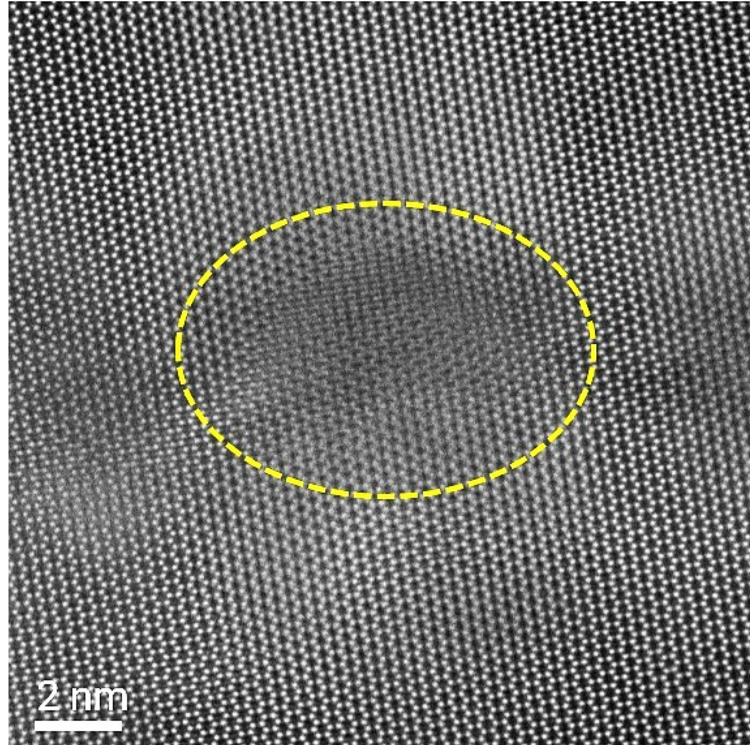


Figure 6.4: STEM image of the capping layer and MBE β-Ga_2O_3 film interface.

Localized dark spots, observed in the TEM image, are distributed on the nanometer scale and are primarily present within the MBE-grown film and at the interface between the film and the substrate. Within the regions highlighted by the yellow dashed circles,

the β-Ga_2O_3 structure appears relatively intact. However, in other sections—particularly at the center of the dark spots—atomic positions exhibit noticeable distortions. Additionally, intensities from extra atomic columns suggest the presence of lattice irregularities. These structural modifications imply a displacement of atomic columns from their original positions, potentially indicative of defect formation due to ion implantation.

Similar defect structures have been previously reported. Huang et al. investigated Si-implanted β-Ga_2O_3 and observed dislocations, which they identified as screw dislocations propagating along the (010) crystallographic direction [86]. Previous research also supports the defect-reducing effects of annealing. Anber et al. [35] reported a significant reduction in implantation-induced defects in Ge-implanted β-Ga_2O_3 following thermal treatment. Similarly, Tajder et al. [77] demonstrated that Sn implantation at room temperature resulted in notable improvements in crystalline quality after annealing at 1150 °C. Given these findings, further annealing studies within the scope of this research are essential to assess potential improvements in crystal quality and defect recovery in the implanted β-Ga_2O_3 samples.



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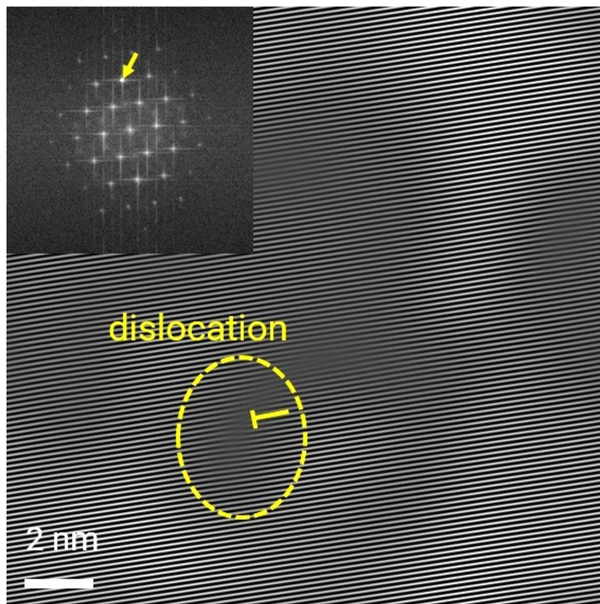

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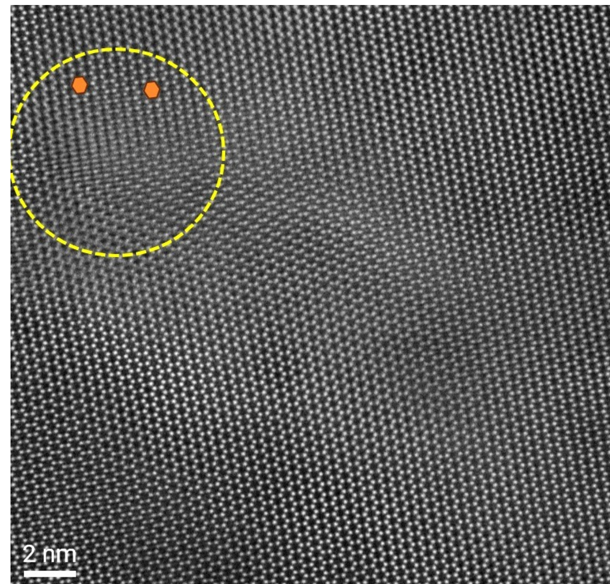

(c)

Figure 6.5: STEM images of (a) MBE film and substrate interface, (b)dislocation at the interface, (c) dislocation in the MBE film.

In an earlier study, post-annealing analysis demonstrated a reduction in crystal defects, suggesting that thermal treatment may mitigate implantation-induced damage [66]. However, in the current study, the STEM analysis of the annealed sample has yet to be conducted, and further investigation is necessary to determine the extent to which annealing can alleviate dislocation defects.

6.4 Conclusion

Here we implanted Ge at both RT and HT with a fluence of 1.5×10^{15} cm^{-2}. HRXRD analysis revealed the formation of additional phases in Ge-implanted β-Ga_2O_3, with broad peaks appearing at 64.5°and 67°, shifting after annealing. The presence of a side shoulder and peak shifts in RT-implanted samples suggests compressive strain accumulation, while further investigation is needed to understand the nature of the observed structural changes. STEM analysis performed on HT implanted not annealed sample revealed the formation of screw dislocation, additional studies on annealed samples are necessary to determine whether annealing can mitigate or eliminate these dislocations.

Chapter 7

Conclusion and Future work

7.1 Conclusion

In summary, wide bandgap (WBG) semiconductors represent the present and future of high-power and high-temperature electronic applications, with β-Ga_2O_3 emerging as a frontrunner in this field. As the demand for green technology grows, β-Ga_2O_3 outperforms materials like Si, SiC, and GaN in applications requiring energy-efficient devices, meeting higher operational expectations. However, the absence of a reliable p-type material limits its performance and reliability, leaving significant room for improvement. Technological advancements in this area can impact the WBG semiconductor surface and introduce interface defects, making the electronic characterization of these interfaces crucial. Additionally, understanding both inherent and extrinsic bulk defects is vital for further progress. This thesis focuses on investigating the influence of high-temperature ion implantation on the crystal defects and conductivity of β-Ga_2O_3. The key findings of this work are summarized as follows,

- In chapter 4, high-temperature ion implantation in β-Ga_2O_3 enables heavily doped n-type regions ($>10^{20}$ cm^{-3}) with low resistivity (0.68 mΩ·cm) and enhanced sheet electron concentration. Compared to room-temperature implantation, it reduces structural defects and strain, as confirmed by HRXRD, while maintaining high carrier mobility due to efficient dopant activation. This highlights its potential for further advancements in β-Ga_2O_3 device fabrication.

- In Chapter 5, Si implantation in β-Ga_2O_3 was utilized to fabricate ohmic electrodes. Samples annealed at 970 °C showed lower resistivity compared to those annealed at

1050 °C, with both displaying ohmic behavior between -0.2 V and +0.2 V. Schottky diodes on in-situ Si-doped samples achieved a rectification ratio of 10^5 and a turn-on voltage near 1 V. C-V measurements confirmed a carrier concentration of 1.9×10^{17} cm^{-3}, matching the target doping level.

- This study examines high-temperature Germanium ion implantation in Fe-doped β-Ga_2O_3 to assess its impact on structural morphology. Compared to room-temperature implantation, high-temperature implantation at 600 °C, with a dose of 1.5×10^{15} ions/cm^2, resulted in reduced crystal deformation, as confirmed by HRXRD. STEM analysis identified dislocations both at the interface and within the MBE-grown β-Ga_2O_3 film in the sample implanted at 600 °C. Further STEM analysis is required for the room-temperature implanted sample in future studies.

7.2 Future work

- In chapter 4, The highest ion implantation temperature explored in this study was 600 °C. While the results demonstrated significant advantages in terms of reduced lattice deformation and improved material properties, investigating even higher implantation temperatures could provide further insights into the effectiveness of high-temperature ion implantation in -GaO. Such studies could potentially reveal critical thresholds where structural or electrical properties reach optimal levels.

  Additionally, the annealing temperature used throughout this work was 950 °C. A future area of research could involve implanting ions directly at this annealing temperature to evaluate whether the activation process can be bypassed entirely. If successful, this approach could streamline the fabrication process by eliminating the need for a separate activation annealing step, reducing processing time and cost while potentially enhancing material performance.

- In chapter 5, Transmission Line Method (TLM) structures were fabricated on samples implanted at 600 °C. However, earlier studies revealed that the AlO capping layer used during implantation led to unintended aluminum incorporation into the MBE-grown -GaO film. This incorporation could be responsible for the observed higher contact resistance at the electrode interface. SRIM simulations suggest that the first 15 nm of the film's surface might be affected by aluminum diffusion. However, further experimental studies are necessary to understand the extent and impact of aluminum incorporation on the material's electrical and structural properties.

  To mitigate the effects of aluminum incorporation and reduce contact resistance, a practical solution would be to remove approximately 20 nm of the surface layer using reactive ion etching (RIE) prior to contact fabrication. This approach could ensure a cleaner interface, leading to improved contact properties. Future investigations should focus on optimizing this surface removal technique and analyzing its impact on the overall device performance.

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