# LEAD-FREE ASSEMBLY AND RELIABILITY OF CHIP SCALE PACKAGES AND 01005 COMPONENTS

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# LEAD-FREE ASSEMBLY AND RELIABILITY OF CHIP SCALE PACKAGES AND 01005 COMPONENTS

Except where reference is made to the work of others, the work described in this dissertation is my own or was done in collaboration with my advisory committee. This dissertation does not include proprietary or classified information.

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Yueli Liu, daughter of Shixun Liu and Yulian Yang, was born Sept. 15, 1973, in Shihezi, China. She entered Nanchang Institute of Aeronautical Technology in September, 1991, and graduated with a Bachelor of Science degree in Material Engineering in July 1995. She then entered Graduate School, Tianjin University, in September 1995. She received the degree of Ph. D. in Material Engineering in February 2000. She married Dong Wei, son of Qinghe Wei and Heai Wang, in November 2003. She worked at the Motorola Advanced Technology Center - Asia, China, as a Research & Development Engineer from Feb. 2000 until Aug. 2001. In Aug. 2002, she joined the Electrical and Computer Engineering Department's Ph.D. program at Auburn University.

# DISSERTATION ABSTRACT

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Chip Scale Packages (CSPs) are widely used in portable and hand-held electronic devices due to their small size and availability. Consumers expect portable products to survive being dropped repeatedly, and drop testing is now common in the reliability evaluation of portable product designs. Lead-free assembly is another trend in electronics industries because of legislation and market factors.

Underfill materials are often used to improve the reliability of a variety of electronic components. In this research, the assembly processes for three underfill options (capillary underfill, fluxing underfill and corner bond underfill) compatible with lead-free assembly have been developed and evaluated. CSPs with eutectic SnPb and without underfill were compared with lead-free and underfilled CSPs. Drop tests were carried out to evaluate the drop reliability of the CSPs as a function of assembly materials. Failure analysis was performed to reveal the typical failure modes for different underfills.

The mechanical shock reliability over the life of the product is very important to the customer. The effects of different surface finishes (Immersion Sn and Immersion Ag), reflow profiles (two cooling rates) and thermal aging on the drop reliability of lead-free CSPs were investigated. Drop test results for assemblies as-built and as a function of aging at 125°C were correlated with cross sectional analyses of the solder joints. Microstructural and failure analyses were also conducted to study IMC evolution and the formation of Kirkendall void and the effect of these changes on drop reliability.

Reducing the size of the passive components and the spacing between them increases the package density and is an efficient way to miniaturize many electronic products. To satisfy this demand, 01005 chip components are now commercially available. However the implementation of such tiny components in new products presents some novel design and assembly process issues. A 01005 test vehicle was designed to investigate the effect of PCB pad design on assembly yield. Process capability of 01005 test board manufacturing was evaluated. A Design of Experiment (DOE) was used to optimize the solder paste printing based on 3D solder paste inspection. Lead-free solder was used for all assembly trials. Several tests were performed to explore the influence of process parameters on placement accuracy and reflow defects. As a results of this analyses of experimental results and a post-reflow inspection for assembly defects, recommendations for PCB design and assembly processes are made.

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I would like to recognize the help of several key members of the technical staff, industrial partners and fellow graduate students. Special thanks are due to Guoyun Tian, Mike Palmer and John Marcell for their assistance throughout the process of this research.

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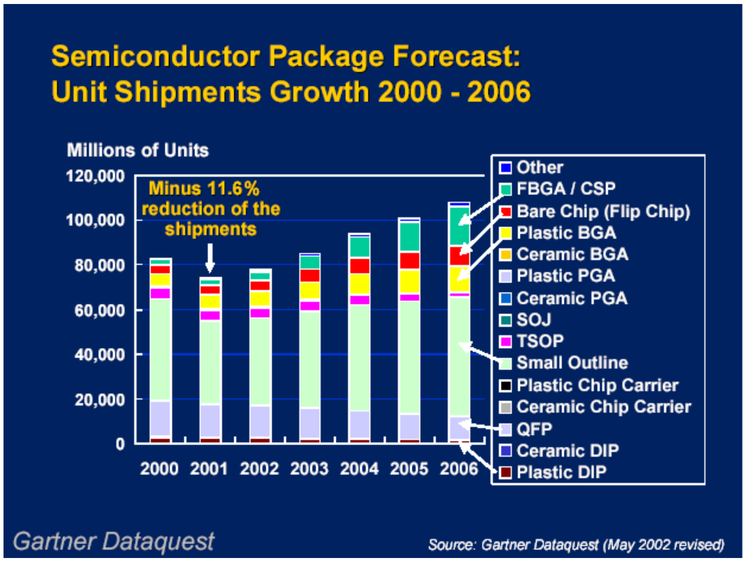
# CHAPTER 1

# INTRODUCTION

## 1.1 Integrated Circuit (IC) Package Trends

The electronics industry is mainly driven by the demand for “smaller, lighter, faster, higher complexity, lower power consumption, and cheaper technology” [1]. Miniaturization continues to accelerate for portable consumer electronics, particularly for consumer electronic products like cell phones, personal data assistants (PDA), camcorders, laptops, cameras and MP3 players. In fact, another driving force in product miniaturization is the increasing complexity of features and functions, accompanied by a lower cost. This market dynamic has accelerated the development and use of finer pitch and smaller components with higher density, both in design and manufacturing technologies.

Chip Scale Packages (CSPs) and Fine-Pitch Ball Grid Array Packages (FBGAs) are the two package types that are most prevalent in portable hand held consumer electronics today [2]. If the area required by the die is more than 80% of the total package area, the industry typically refers to this as a CSP. FBGAs on the other hand are typically defined by their ball pitch, i.e. 1.0mm and below. As shown in Figure 1.1, over the next few years, it is likely that CSPs/FBGAs will experience the largest growth within mainstream IC packages. Much of the this growth will come by way of new product introductions, although some of the growth will be due to Plastic Ball Grid Array (PBGA) and Quad Flat Package (QFP) migration. Figure 2 shows how a CSP/FBGA can significantly reduce the package area for roughly the same ball/lead count [2].



Source: Gartner Dataquest (May 2002 revised)

Figure 1.1 Unit Shipments Growth YR2000 through YR2006 [2]

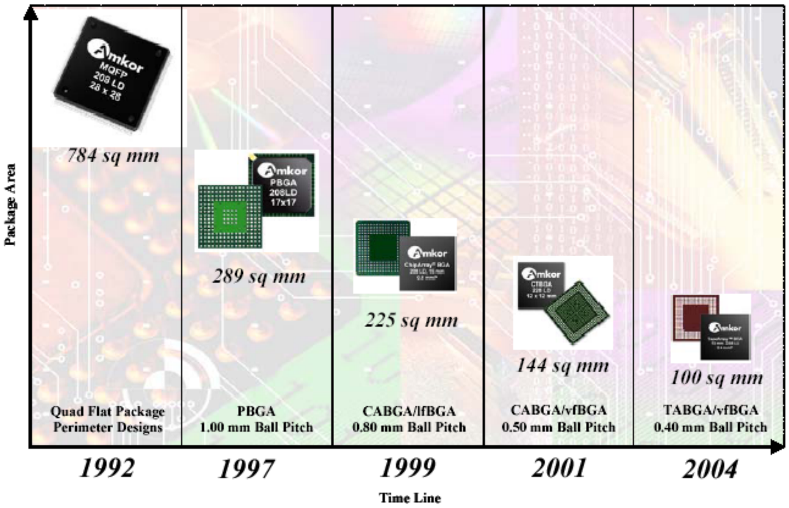


Figure 1.2 IC Package Evolution and the area reductions achieved with CSPs/FBGAs [2]

Passive components occupy a significant area on the printed circuit board (PCB), especially for analog and mix-signal applications, which use a larger number of passives compared to a typical digital system [3]. Reducing the size of the passive components and the spacing between them would increase the package density, and is an efficient way to miniaturize many electronic products.

Figure 1.3 shows the dimensions of dominant passive components. An example of the size evolution of multi-layer ceramic chip capacitors is given in Figure 1.4 [4]. The chip size of the most commonly used passive components gradually decreased from 0805 chip in 1995, to 0603 (1.6-0.8mm) in 1998. With the increasing adoption of ultra-small capacitors for mobile phones, digital cameras and digital camcorders and other compact portable products, set makers have begun to adopt 0402 (1.0-0.5mm), format products as general-purpose capacitors, so 0402 was projected to be the most popular size in 2003. 0201 (0.5-0.25mm) emerged in 1998 and is rapidly gaining market acceptance. Set makers are now demanding that monolithic ceramic capacitors be downsized still further to 01005 (0.4-0.2mm) size, and products of this size are expected to be used in 2004 for modular products that contain capacitors.

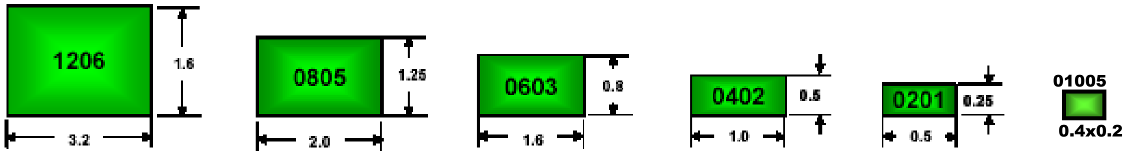


Figure 1.3 Dominant Passive Component Dimensions (mm) [2]

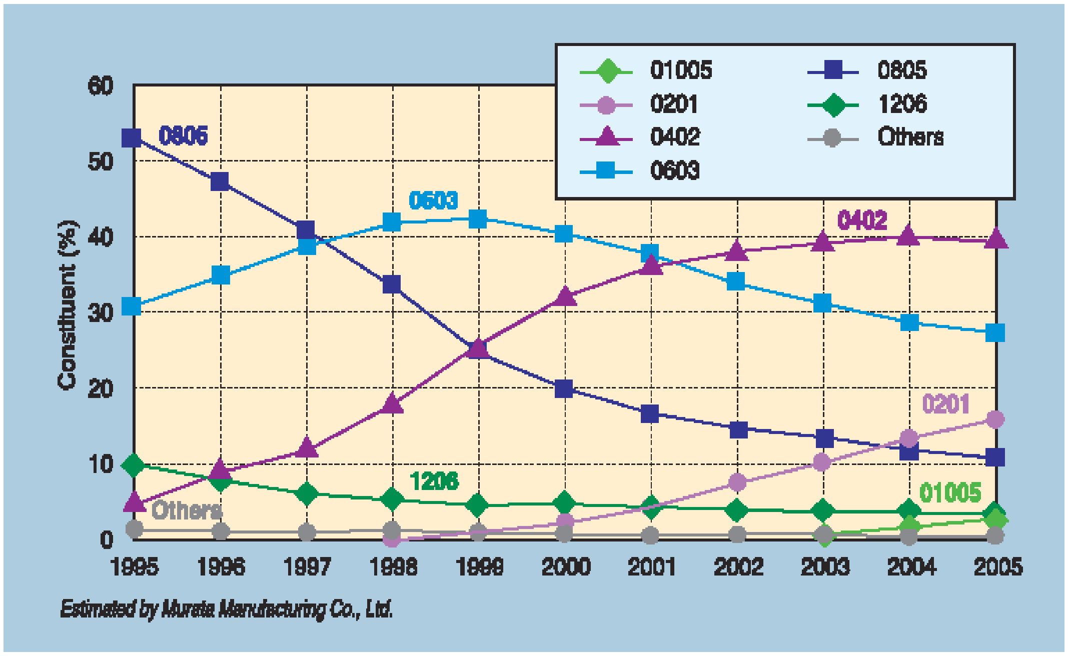


Figure 1.4 Trends in Size of Monolithic Ceramic Capacitors [4]

## 1.2 Chip Scale Package (CSP)

### 1.2.1 Advantages of CSPs

Chip Scale Packages combine the best of flip chip assembly and surface mount technology. It gives almost the same size and performance benefits as a bare die chip assembly, while offering the advantages of an encapsulated package. In comparison to standard surface mount technology, CSPs have the following advantages [5]:

- Reduced package footprint
- Thin profile and reduced weight

- Better electrical performance
- Area array distribution of connections (for most CSPs)

In comparison to standard flip chip technology assembly, CSPs have the following advantages:

- Encapsulated packages
- Easily testable with fast testing for known good dies
- Mountable using a conventional assembly line
- Accommodates die shrink without changing package footprint
- Reworkable
- Some CSPs do not require underfill when mounted on organic substrates

### 1.2.2 Types and Application of CSPs

The package may use an interposer/carrier, and the interposer may be ceramic, polymer, or flex-film. Depending on the CSP design, the interconnection [7] between the IC and the carrier may be wire bonding, TAB, Au stud, soldering, or conductive adhesives. CSPs are generally classified into four major types based on their structure: flex circuit interposer, rigid substrate interposer, custom lead frame, and wafer-level assembly. Examples of packages of these types are shown in Figure 1.5 [6].

Reduction of size and weight are the most important factors during initial adoption of CSP technology. Consequently, consumer products such as camcorders, mobile phones, and laptops are among the products that have been first to use CSPs.

The electrical improvement and high-speed architecture development for memory also make them attractive for DRAM applications.

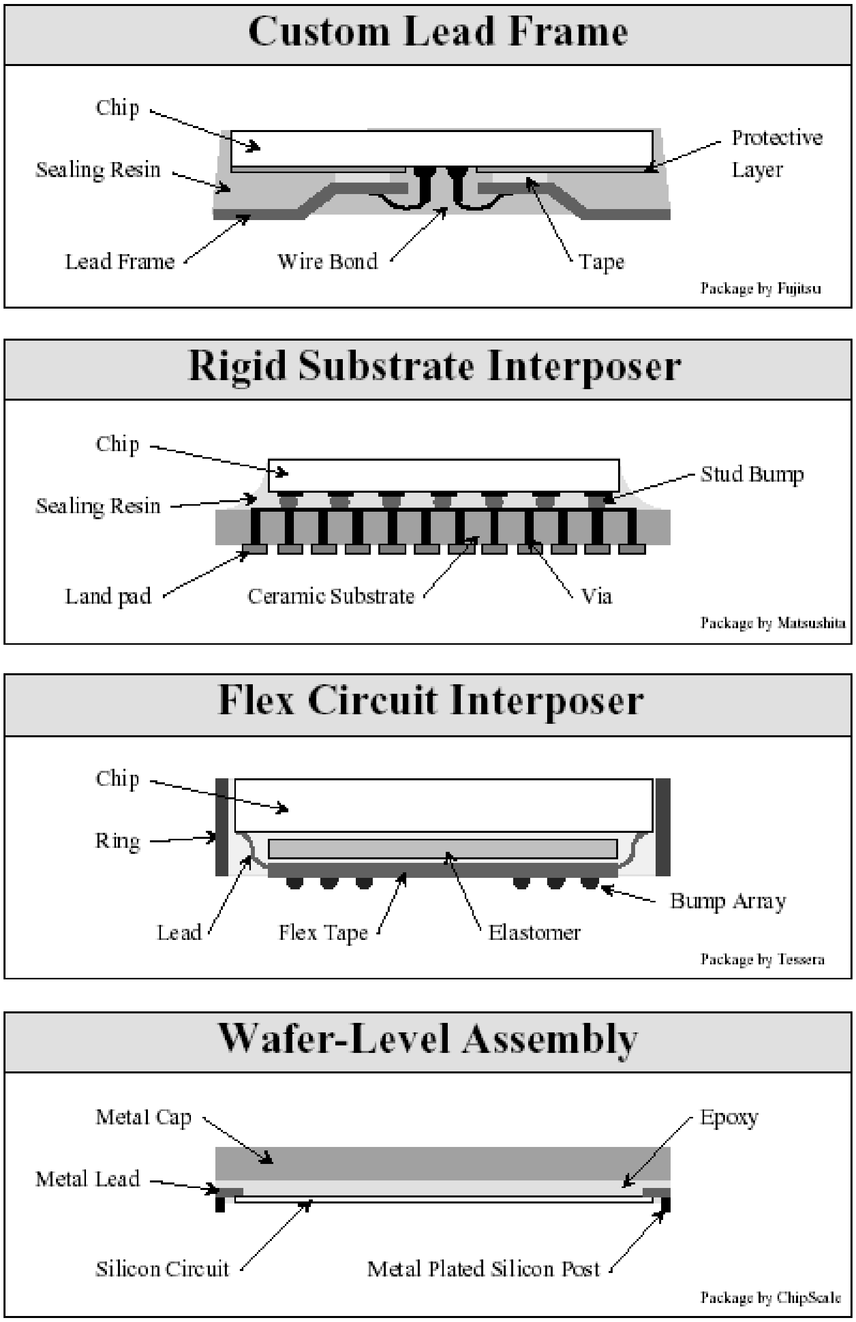


Figure 1.5 Main CSP Types [6]

## 1.3 Lead-free Technology

### 1.3.1 Driving Forces for Lead-free Technology

Electronic products currently contain lead (Pb) in their components, printed circuit boards (PCBs) and solder joints. The eutectic tin-lead alloy (63%Sn37%Pb, wt%) has been practically the only alloy used for soldering purposes in electronics. Although electronics manufacturing accounts for less than 0.6% of lead consumption in the world [8], electronic products often end up in landfills after their disposal, and lead can potentially leach out from the landfills into water supplies. In the USA, the regulatory limit for lead in drinking water is set at 0.015 mg/l, as per EPA40 CFR141. The limit is set at 5 mg/l if the test follows the Toxicity Characteristics Leaching Procedure (TCLP), as per EPA40 CFR261 [9]. A recent study [10] demonstrates that the lead that leaches out from solder can be several hundred times higher than these limits.

Lead is dangerous to human health. The most common types of lead poisoning are classified as alimentary, neuromotor, and encephalic [11]. Lead poisoning often occurs following a prolonged exposure to lead or lead-containing materials [12]. Therefore, the risk of lead leaching from landfills into water supplies must be eliminated.

There are several forces driving the movement toward the elimination of Pb. The initial driving force is the fear of legislation, for example, the proposal of (RoHS) and WEEE directives in Europe to restrict the sale of lead-bearing electronic products, effective July 1, 2006; recycling laws in Japan; and pending regulations in both China and California. However, recently other forces such as the market-driven commercial advantages associated with environmental-friendly electronics have raised a great deal of interest in the industry and have accelerated this process. “Green electronics” is gaining greater appreciation from consumers [13]; so green marketing is now rapidly being viewed as a powerful and effective marketing tool.

### 1.3.2 Lead-free Solder Alloy

The criteria for screening candidate lead-free alloys can be summarized as follows:

- Nontoxic
- Available and affordable in sufficient quantities
- Exhibit sufficient electrical and thermal conductivity
- Possess adequate mechanical properties: strength, toughness, fatigue and creep resistance
- Compatible with typical terminal metallizations (eg. Cu, Ni, Ag, Au, Sn, etc.)
- Have acceptable melt and process temperatures

Several review papers have been published on the development of lead-free solders. [13-19]. Vincent and Humpston summarized their research on electronic assembly using binary lead-free solder. The factors they considered were economic and supply limitations, as well as the technical questions such as solderability and reliability [19]. Hwang systematically illustrated important solder properties for practical applications, especially those properties that are important to ensure solder joint integrity in surface mount technology. The comparisons between lead-free alternatives and conventional Sn-Pb or Sn-Pb-Ag eutectic solders were emphasized [17]. Glazer reviewed the physical metallurgy aspects, including the physical properties and microstructure, mechanical properties, and oxidation and corrosion behavior of binary lead-free solders [15]. This database was later updated and expanded to include the Sn-Ag-, Sn-Zn-, and Sn-Bi-based ternary solders. The manufacturability issues for applications of these lead-free solders in low-cost electronic assembly were also presented [16]. Abtew and Slvaduray discussed the properties of the binary lead-free solders and technical issues of solder joints [14]. Suganuma reviewed recent developments in ternary lead-free solders and the interaction of these solders with metallization [18].

A great deal of effort has been directed to the development of a eutectic Sn-Ag-Cu solder. Based on the above criteria, eutectic Sn-Ag-Cu alloy is considered to be the most promising candidate for replacing eutectic Sn/Pb systems. Cu is added to Sn/Ag in order to lower the melting temperature, and improve the wettability, creep and thermal fatigue characteristics. The ternary eutectic temperature is at 217°C. Its thermo-mechanical properties are also better than those of the conventional Sn-Pb solder [20]. In 2000, NEMI recommended the use of eutectic Sn-Ag-Cu alloy (Sn3.9 Ag0.6Cu) to replace eutectic Sn-Pb alloy in reflow processing and eutectic Sn0.7Cu alloy in wave soldering [21]. These alloys have already been used successfully in production and have demonstrated exceptional reliability in thermal cycling compared to eutectic Sn-Pb.

### 1.3.3. Issues in Implementing Lead-free Technology

The impact of using lead-free technology for SMT assembly is shown in Figure 1.6 [22]. There are several important issues that arise as a consequence of switching from eutectic Sn-Pb to a lead-free solder technology for microelectronic chips, packages, and assemblies. The key issues are discussed in this section.

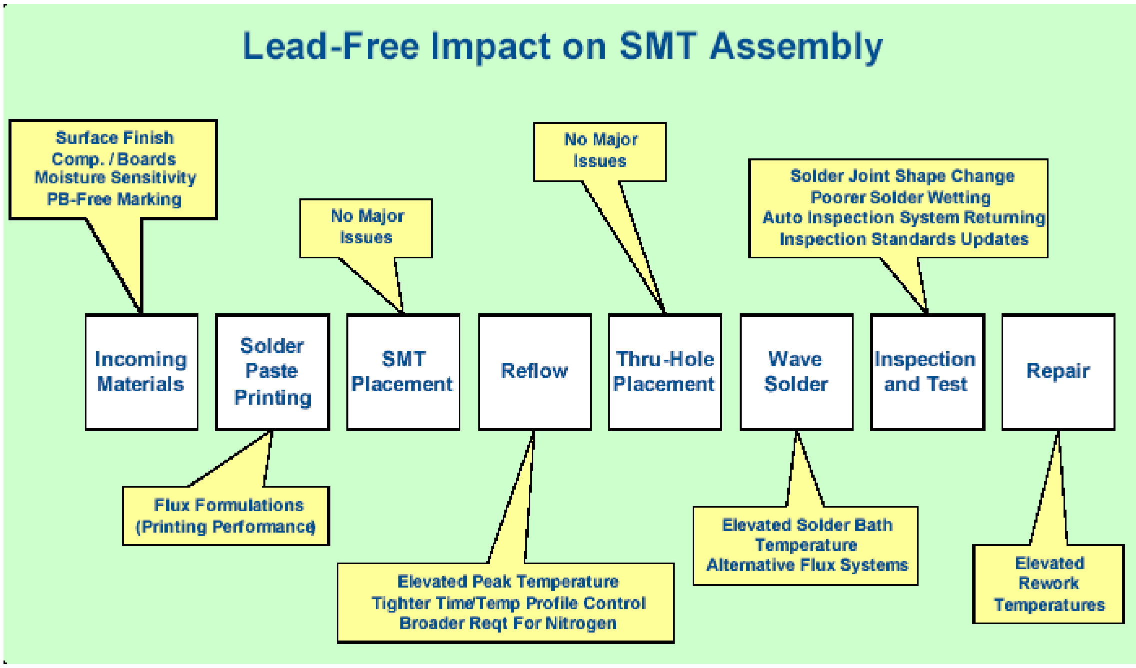


Figure 1.6 Lead-free Impact on SMT Assembly [22]

#### 1.3.3.1 Higher Process Temperatures

Most lead-free alloys of interest have a melting temperature that is 35-40°C higher than eutectic Sn-Pb (Melting Point = 183°C), which often has a drastic effect on the integrity, reliability, and functionality of printed wiring boards, components, and other attachments [23]. The bulk of lead-free research has focused on identifying suitable solder candidate alloys to replace eutectic Sn-Pb. The effects of higher process temperatures on various microelectronic board assemblies when utilizing most lead-free solders are listed in Table 1.1 [41], and other issues related to higher process temperature will be discussed in the following section.

TABLE 1.1 Effect of Higher Process Temperatures on Various Microelectronic Board Assembly [41]

| Board assembly items | Effects |
|---|---|
| *Components* | |
| Ceramic chip carriers | Little to none |
| Organic chip carriers | Degradation can be substantial, depends on $T_g$ of material<br>Increased moisture sensitivity level |
| Specials: electrolytic capacitors, wound components, etc. | Susceptible to damage, typically designed for 230° maximum temperature, some up to 260°C |
| *Printed circuit board material* | Standard FR-4, $T_g$ ~140°C<br>Subject to degradation<br>Higher $T_g$ materials<br>Will survive proposed ~ 240°C<br>Typically will not survive ≥ 260°C |
| *Plastic overmold material* | Thermal plastics may undergo shrinking or warping or cause critical features to move (creep)<br>Thermal setting compounds, typically not affected by MSL-related effects |
| *Fluxes* | Must be formulated to be active near and at the alloy melt point temperature<br>Must not create charred masses that hinder soldering, or allow surface reoxidation |

Higher reflow temperatures increase dissolution rates, which may result in an increased concentration of termination pads and surface finish elements in solder joints.

Copper is the main circuit material utilized for PCBs and also some component lead frames (e.g., small outline—SO; quad flat pack—QFP; plastic leaded chip carrier—PLCC) owing to its good electrical conductivity and solder wetting properties. Tin has a high affinity for copper, so the high tin composition of many lead-free solders and their high melt temperatures lead to a much increased tendency to dissolve copper termination pads compare to eutectic Sn-Pb. The lead-free alloys have significantly greater Sn contents and melting points than eutectic Sn-Pb, which both serve to boost the Cu dissolution rate to between two and seven times faster compared to 60Sn-40Pb [100]. Excessive intermetallic compound formation ($Cu_6Sn_5$) can also adversely affect the solder joint reliability due to the brittle nature of this compound, particularly under impulsive load conditions [24].

Nickel/gold is another popular board finish. However, care must be exercised to not exceed the rule-of-thumb Au threshold concentration in a solder joint, which is approximately 3% [25].

#### 1.3.3.2 Component Finishes

Lead-free manufacturing not only pertains to solder pastes and solder bars for wave soldering, but also as a substitute for the lead-bearing finishes used for component leads and solder bumps. In general, the change to lead-free finishes for components is expected to be a substantial part of the conversion of electronic assemblies to lead-free manufacturing, and may well be the most difficult to implement. Component manufacturers have reliability concerns related to both the impact of devising suitable processes to provide consistent, high-quality finishes with new materials, and also the effects these finishes will have on the integrity of solder joints. As noted earlier, there is also some concern about the possible effects that increased process temperatures will have on the components themselves [26].

Many peripherally leaded components utilize Sn-Pb finishes for the leads. In general, it is relatively easy to eliminate lead from surface finishes on the leads of components. Examples of alternatives include Pd/Ni, Sn, Au, Ag, Ni/Au, Ag/Pt, Ag/Pd, Pt/Pd/Ag, Pd, and Ni. These finishes have all been used in the past and are likely to be key contenders for use in completely lead-free systems [27]. Ni/Pd finished terminations have previously been evaluated with several lead-free solders and found to provide solderability comparable to eutectic Sn-Pb [28]. Sn-Bi-based finishes have also been utilized with component lead frames for some time. These finishes exhibit excellent mechanical properties when used with Sn-Ag-Bi solders. [29]. Several plated, tin-based lead-free finishes, such as Sn, Sn-Bi and Sn-Cu among others have been found to be suitable for component terminations (i.e., lead frames) [30].

Area array components (i.e., Ball Grid Arrays) typically consist of eutectic Sn-Pb or Sn-Pb-2%Ag solder ball terminations. It appears that the major lead-free solder candidates are also suitable as BGA solder ball materials. However, if the melting temperature for the later interconnections is set around 220°C, then the first level interconnection needs to have a melting point of at least above 260-270°C in order to avoid remelting during subsequent reflow processes. A suitable high melt, lead-free alloy that meets the condition of low cost and whose melting point is within the range of

250-300°C has not yet been identified. The only well-established lead-free alloy in this temperature range is 80Au-20Sn, which is too expensive to be utilized for this application [31]. There are also concerns with lead-free terminated BGA components, among which are their wetting and self-centering characteristics, both of which impact placement accuracy requirements and manufacturing yields [32].

Some lead-free component finishes are eutectic Sn-Cu or pure Sn. Sn whiskers readily grow on high Sn content finishes under certain condition, which may cause shorts, so Sn whiskers are major concern for components with high Sn finishes.

#### 1.3.3.3 Board Surface Finishes

The PCB industry currently produces a number of lead-free finishes including electroless nickel/immersion gold (ENIG), Immersion Ag (Im Ag), Sn, Ni/Pd, and organic solderability protectants (OSPs).

*a. Hot Air Solder Leveling (HASL)*. It is a physical deposition process using bulk liquid metal into which the board is dipped to apply coatings. A secondary step (hot air blow) is used to level or reduce the amount of material retained on the surface [31]. Hot air solder leveling accounts for over 60% of the surface finishes on printed circuit assemblies. The PCB industry has been exploring alternatives to HASL that eliminate thermal shock for boards, which is further aggravated by the increased process temperature required by most lead-free alloys.

b. *Plated Finishes.* The trend here is to provide thinner, more uniform, and planar finishes that facilitate fine-pitch assembly. These conditions are more easily achieved by utilizing plated finish solutions:

1. Electroless Nickel/Immersion gold—The Interconnection Technology Research Institute (ITRI) and others have investigated the failure of SMT parts, particularly eutectic Sn-Pb BGA component solder joint failures associated with electroless Ni/Immersion Au metallization on board pads [37]. These failures general occur under mechanical shock test conditions. Given the root cause theory of this type of failure, it is anticipated that lead-free solders will experience the same failure mechanism. Nickel/gold finishes are often utilized for higher temperatures and multi-soldering purposes. The cost of Ni/Au is about 25% higher than for OSP finishes [26].

2. Electroplated tin—Electroplated Sn exhibits excellent solderability and corrosion resistance, but is prone to Sn whisker growth. Thin, hair-like whiskers grow from the surface and pose a potential reliability problem due to the electrical shorts they may cause in the field [38-40]. Heat fusing or reflow is used to eliminate tin whiskers [26].

c. *Organic Solderability Protection (OSP).* OSP is an anti-tarnish coating of an organic compound over a copper surface to prevent oxidation. It is a water-based organic compound that selectively bonds with copper to provide an organometallic layer that protects the copper. OSP keeps the copper surface solderable and flat, and it is lead-free and hence may be considered more environmentally friendly [31].

*Effects of Higher Process Temperatures.* The higher process temperatures typical of lead-free solders may cause some lead-free surface finishes to react more rapidly compared to eutectic Sn-Pb conditions. If the board finish is Sn finish, it can be consumed in Cu-Sn intermetallics and then lose solderability with multiple high temperature reflows.

Oxidation problems with OSPs can result upon exposure to several soldering processes, particularly at elevated lead-free soldering temperature conditions. Utilizing an inert atmosphere and reformulating OSPs to withstand higher process temperatures will reduce this risk [26].

Another area of concern is the reaction rate between lead-free solders and terminal metallurgy systems. The formation of Ni-Sn IMCs at the interface is considerably slower than the formation of Cu-Sn IMCs. This is an important aspect that must be taken into consideration because the Sn content and process temperature are both significantly higher for lead-free solders compared to eutectic Sn-Pb, so the reaction rates are quicker. The formulation of excessively thick IMC layers should be avoided to prevent weak solder joints. However, even with a reduced formation rate, a thicker Ni layer is required than for eutectic Sn-Pb solders [28].

#### 1.3.3.4 Process Challenges

As noted previously, the preliminary challenge that lead-free solders present for IC and component manufacturers, and electronic assemblers is the higher process temperatures typically required of lead-free solders. The generally accepted limit that

IC packages can withstand is approximately 240°C, and the lower limit to reliably reflow eutectic Sn-Pb solders is about 205°C. This provides approximately a 35°C process window, which is sufficient in a properly monitored line to produce a low-defect-rate, high-yield product with a low risk of creating process drift-related defects. However, with lead-free assemblies, the process window shrinks dramatically, as illustrated in Figure 1.7 [22]. For Sn-Ag-Cu alloys, whose liquidus is 217°C, the process window is reduced to only 10°C. Given that assemblers, prefer to remain within 5°C of their control limits, the actual process window is therefore very small. However, it has been determined that the soldering process can be significantly improved by obtaining and analyzing data on a real-time basis in a reflow oven. Process control can be aided by utilizing prediction software that customizes the profile for a specific solder paste, product type, and user-defined input process limit [33].

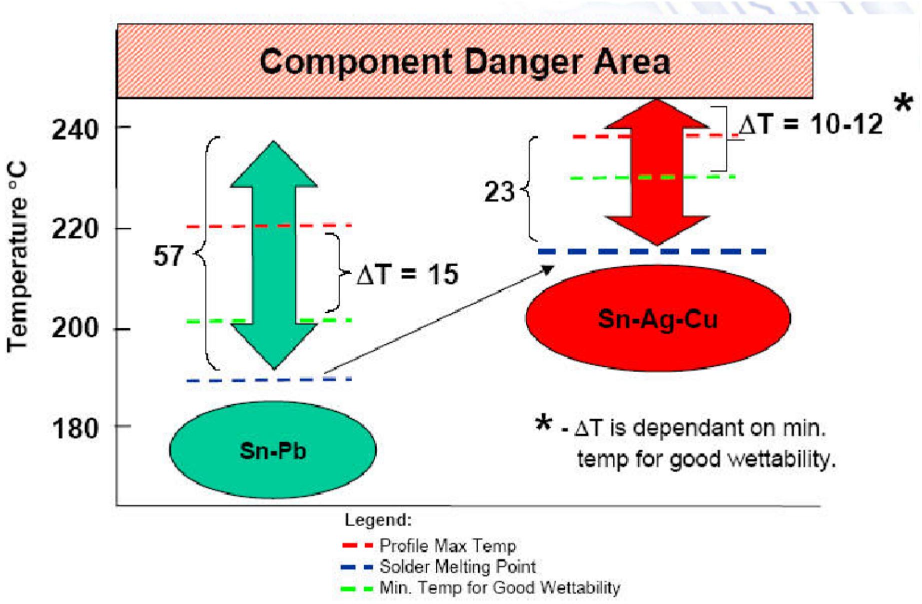


Figure 1.7 Lead-free Tighter Process Window [22]

#### 1.3.3.5 Rework

Rework is the term in the electronics industry that pertains to removing and subsequently replacing one or more of the components or other attachments on a PWB. The procedure typically consists of locally heating the solder joints of the component. When the solder joints melt, the component is lifted away from the board either by mechanical means or by a vacuum-activated device. A replacement component is locally reflowed to the same site. Typically the board is also heated from the underside to lower the thermal gradient and to reduce warping.

Rework is an important aspect of manufacturing that helps meet required yields to achieve economic viability—another aspect that is expected to be substantially affected by the change to lead-free technology. Rework operators will require additional training, and further development work will be necessary because the properties and melting points of the solders can be significantly altered from component to component across an assembly because of elemental additions introduced to the solder from the PWB and terminal pad metallization systems.

Several studies focusing on rework practices for solders have been reported [34, 35, 36, 44]. The rework of lead-free solder joints has been shown to be technically feasible. Concerns associated with locally heating printing circuit boards or attachments at high temperatures are mostly associated with the need to reflow heavy and complex components such as BGAs that require a high level of heat to effectively achieve removal and reflow. With careful optimization, it appears that rework can be accomplished without damaging temperature-sensitive parts with minimal board warpage. The same issues apply to rework of general assembly operations, soldering temperatures and other parameters must be tightly controlled.

## 1.4 Board Level Reliability of Lead-free Solders

### 1.4.1 Limited Database

Long-term reliability remains a major unknown, since there is currently only a limited database for lead-free solders. Even with accelerated testing, it will take years to generate an understanding equivalent to that presently available for eutectic Sn-Pb. The need for this level of understanding is admittedly less critical for relatively short-lived consumer electronics applications such as games, mobile telephones, or other handheld telecommunication devices, but for applications whose service lifetimes are expected to span from a few years to a decade or more, this lack of information is a real concern. Numerous studies have indicated that, in general, lead-free alloys including Sn-Ag-Cu exhibit a level of reliability under accelerated testing conditions that is at least equivalent to that of eutectic Sn-Pb solder joints, and in many cases is substantially better [41]. The field data for the lead-free solders utilized in several niche products such as phones (Nortel), minidisc players (Panasonic), laptop and tabletop personal computers available from several manufacturer have not indicated any major reliability problems [41]. However, more accelerated laboratory tests and field data are necessary before drawing conclusions about the long-term reliability of these solder materials, as they have so far been used in a limited number of solder joint configurations and field conditions [41-43].

### 1.4.2 Drop Reliability of Lead-free Components

Two of the main failure modes for packages to board solder joint interconnects are low cycle solder fatigue due to thermal excursions and brittle fracture caused by static and dynamic loads such as impact shock, vibration, and bending. Traditionally, the critical failure mode of interest has been solder fatigue, which is driven by the coefficient of thermal expansion (CTE) mismatch between the component and motherboard. However, due to the continuous push for device miniaturization and new applications in portable electronics, which are subjected to human clumsiness, solder joint failure under drop or shock conditions has now become a critical reliability issue. Instead of ductile fatigue cracking through the bulk solder that is typically observed in thermal cycle loading, the typical failure mode for a solder joint under drop impact is brittle fracture of the intermetallic compound (IMC) between the board pad and bulk solder joint [69].

Researchers are now starting to pay more attention to drop test studies and analyses due to urgent industrial demands to understand the failure mechanisms involved [45-50]. A new JEDEC standard for board level drop tests of handheld electronic products has just been released that specifies the drop test procedure and conditions that should be used for such tests [51-53].

New reliability concerns are also arising due to the increasing complexity of solder metallurgies, since as a result of the new environmental requirements novel combinations of solder paste, printed circuited boards (PCB) surface finishes and component terminal metallizations are being employed. Therefore, it is important to have a systematic study of the metallurgical reactions and the evolution of the related microstructures of solder interconnections, as well as their impact on reliability, especially when soldered assemblies are tested under mechanical shock loading conditions.

#### 1.4.2.1 Effect of the Surface Finish on Drop Reliability

The compatibility of PWB surface finishes with solder compositions is an important factor governing the reliability of solder joints. Extensive work has been conducted to study the effect of PCB surface finish on the thermal fatigue reliability performance of lead-free solder joints and their underlying failure mechanism. However, very few papers have been published on the board level reliability under drop conditions [55-61]. The influence of surface finish on drop impact reliability has not been comprehensively documented and the failure mechanism not yet well understood.

Samhit et al. [54] discussed the reliability implications of the incompatibility between 96.5Sn3.5Ag solder and two PWB surface finishes (Electroless Ni/Immersion Au and pre-tinned Cu) for the case of a Cu terminated component. Their work illustrates how surface finish combinations involving Cu and Electroless Ni/Immersion Au on the component and board, respectively or vice versa, can present reliability risks in thin (30-100*um*) solder joint assemblies in portable electronic products that are subjected to mechanical drop environments.

Chong et al. [55] studied the effects of drop impact on the reliability of solder interconnects of leaded (36Pb62Sn2Ag) and lead-free (Sn4Ag0.5Cu) compositions. The influence of different package types and the impact of PCB surface finishes of OSP and ENIG (electroless Ni/Immersion Au) were also examined. The drop test results showed that lead-free solder joints on the ENIG finish have weaker drop reliability performance compared to the leaded and lead-free solders on an OSP finish.

Mikko et al. [60] investigate two different types of wafer level chip scale package (WL-CSP) components with eutectic Sn3.8Ag0.7Cu and eutectic SnPb solder paste on Ni (P)/Au and OSP surface finishes under standard drop test. The failure analyses revealed that the primary failure mode in the component side was the cracking of interconnections along a brittle NiSnP layer between the electroless Ni(P) of high P-content and the solder alloy, while components with (Al)Ni(V)/Cu UBM failed by cracking along the $[Cu, Ni]_6Sn_5$ intermetallic layer. On the board side the cracking occurred in the porous NiSnP layer formed between the electroless Ni(P) metallization and the $(Cu, Ni)_6Sn_5$ intermetallic layer. The fact that the cracking occurred predominantly on the component side reaction layer was though to be due to three factors: higher normal stresses on the component side, brittleness of the reaction layer(s) and the strain-rate hardening of the bulk solder interconnections.

Jiang et al. [61] compared the reliability of two solder compositions (Sn-Pb and Sn-Ag-Cu) and two surface finishes (Ni/Au and OSP). The results indicated Sn-Ag-Cu solder showed lower fracture toughness then SnPb solder during drop impact. The crack path in the SnPb solder joint almost always went through bulk solder near the substrate side. However, IMC interfacial failure near the substrate side was found in the Sn-Ag-Cu solder. The Ni/Au surface finish showed a better drop performance than OSP in both Sn-Pb and Sn-Ag-Cu solder joints.

#### 1.4.2.2 Effect of Underfill on Drop Reliability

Underfill materials are often used to enhance the reliability of a variety of component types, including flip-chips, chip scale packages (CSPs), and ball grid arrays (BGAs) [62-67]. Most manufacturers that use flip-chips on boards (FCOB) or a flip-chip in a package (e.g. FC-BGA) underfill them due to the large CTE mismatch between the silicon die and the substrates. The other packages may only be underfilled if there is either a perceived risk to the products (e.g. a cell phone may undergo frequent drops) or for a high reliability application (e.g. avionics). The CTE matching of the underfill materials is typically achieved through the addition of silica-based fillers. This addition lowers the CTE and thus provides a gradient between the silicon chip and the substrate.

Liu et al. [65] examined the assembly process with capillary and fluxing underfills. Issues of solder paste versus flux only, solder flux residue cleaning and reworkability were investigated for the capillary flow underfills. Drop tests were performed to evaluate the relative performance of the underfills, and the results indicated that all of the underfills significantly (5-6x) improved the reliability in the drop test compared to nonunderfilled parts. Test vehicles were also subjected to liquid-to-liquid thermal shock testing. The use of underfill improved the thermal shock performance by 5x.

Ghaffrian et al. [67] studied the effect of underfill on CSP reliability. Three package structures were tested: leadless CSP, flex-on-chip CSP and TAB CSP. The results showed that underfill improved the reliability of leadless packages, had a minimal impact on flex-on-chip CSPs, and was negative for TAB CSP reliability.

The most common reason to underfill CSPs is to improve their shock and vibration reliability (drop testing). However, their widespread use has been limited due to complex application requirements that restrict the integration of underfills into SMT assemblies, and also complicate repair and rework [68]. New developments in underfill materials that can be pre-applied to the CSP prior to board-level assembly will eliminate the uncertainties and imprecision of liquid underfill dispensing, a concept that is most often associated with wafer-level package.

#### 1.4.2.3 Effects of Thermal Aging and Kirkendall Void on Drop Reliability

Drop tests are typically performed on as-built samples. However, customers expect their portable products to survive dropping after some use time in the field, so portable electronic products such as cellular phone should undergo thermal aging prior to the drop and bend tests.

Chiu et al. [69] conducted drop tests and shear tests of ball grid arrays (BGAs) with Sn-Ag-Cu solder balls on Cu pads after thermal aging at 100°C, 125°C, 150°C, 175°C for 3, 10, 20, 40 and 80 days. Kirkendall voids were observed at the Cu to $Cu_3Sn$ interface. Voids occupied 25% of pad/solder interface after only 3 days of 125°C aging, and the void density increased with the aging time and temperature. The drop performance degraded 80% from time 0 to 10 days at 125°C.

Date et al. [70] performed miniature Charpy tests on solder balls of eutectic Sn-Pb and Sn-Ag-Cu bonded to Cu, which were subsequently aged at 150°C for up to 1000hrs. A large number of voids were observed in the $Cu_3Sn$ phase after 500hrs aging at the interface between solder and Cu. A ductile to brittle transition associated with the fracture inside the solder to within the interfacial intermetallic compound (IMC) phase was seen as the aging time increased.

The formation of Kirkendall voids at the solder/Cu interface had been reported by earlier researcher. In 1994, Yang and Mussel [71] reported observation of voids at the interface between a eutectic Sn-Ag solder joint and electroplated Cu after aging at 190°C for 3 days. It is interesting that they also aged the same solder on rolled Cu at 190°C for 12 days. Although the $Cu_3Sn$ phase existed, no voids were found in either the $Cu_3Sn$ phase or the $Cu_6Sn_5$ phase. Their explanation was that during the formation of the $Cu_3Sn$ phase, the mass imbalance due to the different diffusion rates of Sn and Cu induced the formation of vacancies or fine Kirkendall voids, which may be accelerated by the hydrogen introduced during the electroplating process.

Ahat et al. [72] reported a study of interface microstructure and shear strength of 96.5Sn3.5Ag and 62Sn36Pb2Ag on Cu after aging at 250°C for 0, 50, 250, 500, and 1000 hrs. As the aging time increased, more voids formed in the $Cu_3Sn$ phase. The shear strength of both the Sn-Ag and Sn-Pb-Ag decreased with aging time, and the fracture mode changed from mixture of solder and IMC at zero aging time, to a complete fracture of the IMC layer after1000 hrs aging.

Mei et al. [73] carried out a study that focused on two issues: the conditions for void formation, and the effect of voids on solder joint reliability. There were a total of 9 cases studied based on the different combinations of components, component finish, solder and board surface finish. Voids were seen in high, low, and zero densities in samples under different conditions, after aging either for 20 days at 125°C or for 5 days at 145°C. For Case 4, leaded component (10 μm electroplated SnPb over lead-frame of 97Cu2.5Ni0.5Si aged 5 days at 145°C), very few voids were seen and the $Cu_3Sn$ phase was not visible. For case 7, leaded component with 10 μm electroplated matt Sn over Cu-3Ni lead-frame, attached onto the motherboard with OSP Cu pads, -40°C-125°C 2000 cycles, there were few voids at the interface between the solder and the mother board; no voids were visible at the interface between the solder and component lead. It seems that the Cu plating process and the small concentration of Ni in either the solder or substrate influenced the void density and distribution. Voids were seen in the thermal cycled assemblies. Drop tests showed that aged BGAs did not fail at the voided interface; rather the failures occurred inside the solder joint or PCB laminate. The shock strength at 400G of BGAs packages aged for 20 days at 125°C did not degrade.

## 1.5 Research Objectives

The main objective of this research was to develop and optimize the assembly processes for chip scale packages (SnPb/lead-free) and very tiny 01005 components (lead-free), and to evaluate the drop reliability of CSPs. Four projects were conducted and are presented in the following chapters.

Chapter 2 examines the SnPb CSP assembly processes with corner bonding underfill including underfill dispensing, CSP placement and reflow. SnPb CSPs were used as a baseline to compare with lead-free CSPs in the latter chapters. Drop tests were carried out to evaluate the drop reliability of CSPs with corner bonding underfill and the results compared with those obtained with conventional capillary underfill and non-underfilled CSPs. Failure analysis was performed to find the typical failure modes and the location of solder joint cracks for different underfill processes using cross-sectioning and SEM technologies.

The assembly processes for three underfill options (capillary underfill, fluxing underfill and corner bond underfill) compatible with lead-free assembly were developed and are discussed in Chapter 3. CSPs with eutectic SnPb were compared with lead-free CSPs. Drop tests and failure analyses are also included.

Chapter 4 investigates the effects of surface finishes (Immersion Sn and Immersion Ag), reflow profiles (two cooling rates) and thermal aging on the drop reliability of lead-free CSPs. The test vehicles were assembled and then subjected to thermal aging to simulate IMC growth under application conditions. Drop test results for assemblies as-built and as a function of aging at 125$^{o}$C were correlated with cross sectional analyses of the solder joints. Microstructural and failure analysis were also conducted to study IMC evolution and the formation of Kirkendall voids, as well as the effect of those changes on drop reliability.

Chapter 5 describes a test vehicle designed to investigate the effect of PCB pad design on 01005 chip resistor assembly yield. The process capability for 01005 test board manufacturing was evaluated. A Design of Experiment (DOE) was used to optimize the solder paste printing based on 3D solder paste inspection. Lead-free solder was used for all assembly trials. Several tests were performed to explore the influences of process parameters on placement accuracy and reflow defects. As a result of a through analyses of the experimental results and post-reflow inspection for assembly defects, recommendations for PCB design and assembly processes are provided.

Chapter 6 concludes the dissertation results and findings and discusses the topics for future work.

# CHAPTER 2

# PROCESSING AND RELIABILITY OF CORNER BONDING CHIP SCALE PACKAGES

## 2.1 Introduction

Chip scale packages (CSPs) are now widely used for many electronic applications, especially in portable products. Usually CSP designs are expected to meet the necessary thermal cycle or thermal shock reliability requirements for those applications. However, with decreasing pad sizes and solder joint volumes, the mechanical shock (drop) and bending resulting from mishandling during transportation or customer usage, may cause solder joint failure, which eventually leads to product malfunctions. Therefore, board level solder reliability during drop impact is a great concern to semiconductor and electronic product manufacturers, especially for handheld or portable telecommunication devices such as mobile phones and PDAs.

The use of underfills is known to increase the mechanical strength of CSP-to-board connections [62-67]. The most common underfills used in the electronics industry today are capillary underfills with low viscosity, which are developed to flow underneath a component by capillary action after reflow, and are then cured at elevated temperatures to form a bond with high adhesion to both the component and the substrate. If moisture is present in the PCB, a dehydration bake is required prior to underfilling to eliminate voids in the underfill [74]. Since capillary underfills need additional board dehydration, underfill dispensing, flow and cure steps and the associated equipment for the assembly process, this process increases the cost of materials, capital equipment, and process time. Consequently, manufacturers of portable electronics are looking for other solutions that would not only improve drop performance but also reduce cost.

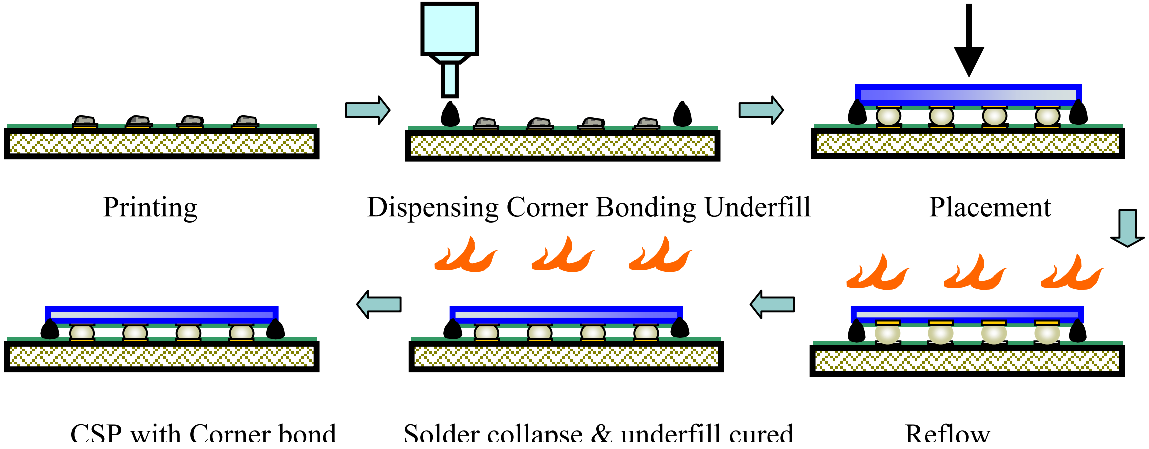


Figure 2.1 Corner Bonding Underfill Process

Corner bonding underfill offer an alternate approach, as shown in Figure 2.1. In this approach a high-viscosity underfill is dispensed at the four corners of the CSP site after solder paste printing, just prior to CSP placement. The CSP is then placed and reflowed. During the reflow cycle the solder balls collapse and the underfill cures, providing reinforcement at the four corners of the CSP. Since the underfill dots are relatively small, a dehydration bake is not required. With a smaller contact area compared to full capillary underfill, the assembled CSPs can be removed using a standard hot air rework station, so this process is reworkable. The whole assembly cycle time is reduced due to no post-reflow dispensing and a cure step.

In this chapter, the SnPb assembly processes for corner bonding including underfill dispensing, CSP placement and reflow are examined. Drop tests were carried out to evaluate the drop reliability of CSPs with corner bonding underfill and compared with conventional capillary underfill and non-underfilled CSPs. Failure analysis was performed to find the typical failure modes and the locations of solder joint cracks for different underfill processes using cross-sectioning and SEM technologies.

## 2.2 Assembly Process of Corner Bonding CSPs

### 2.2.1 Test Vehicle

A test vehicle designed at Auburn University was used in this study, as shown in Figure 2.2. The test board dimensions were 2.95" by 7.24" by 0.042" thick, with a four-layer construction of FR-4 epoxy with glass fiber reinforcement. Each side had 10 CSPs attachment sites with one side for 12mm CSPs and another side for 8mm CSPs. Only the 8mm CSPs were used in this study. Standard technology was used for board fabrication, with no build-up or HDI layers. Drill holes (0.013” drill) under the 12mm CSP were plugged and tented to prevent underfill from flowing through the hole during dispensing. The pads were 0.010” in diameter, NSMD (non-solder mask defined) with an electroless nickel/immersion gold finish. Initial drop testing experiments yielded inconsistent results. Failure analysis revealed failure at the interface between the nickel and the intermetallic layer (Figure 2.3), which is indicative of black pad associated with electroless nickel/immersion gold [75]. Boards were therefore obtained from a second supplier with an immersion silver finish and used for the remaining experiments.

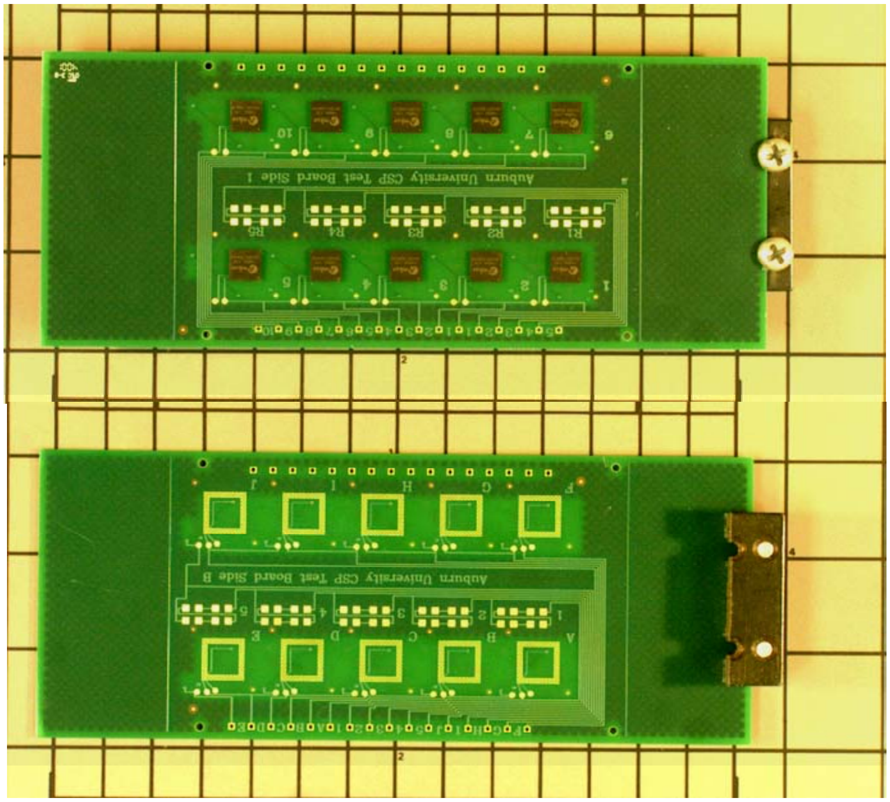
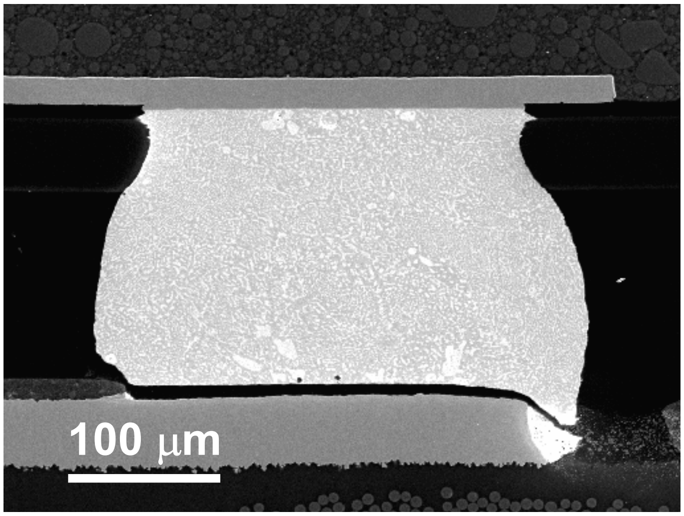
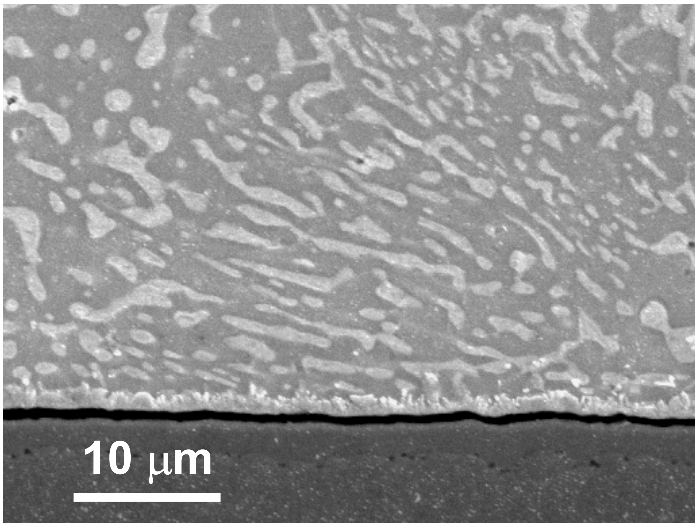


Figure 2.2 Photographs of Test Board (front and back) with Weight (31.8g) Attached to Backside (non-CSP side) for Drop Test.

The CSP, manufactured by Amkor Technology, was an 8mm, 0.5mm pitch, 132 I/O TapeArray and was purchased from Practical Components (A-TArray132-.5mm-8mm-DC). The I/O was on a 14 x 14 array with only the outer three rows populated. The CSP was a daisy chain test part for continuity measurements. The silicon die was 3.98mm x 3.98mm.



(a)



(b)

Figure 2.3 Cross Section (a) and Close-up (b) of Failed Solder Joint after Drop Test Using Printed Wiring Board with Electroless Ni/Immersion Au Finish.

### 2.2.2 Process Issues of Corner Bonding Underfill

Before board assembly, several issues had to be considered and then the corresponding processes had to be optimized to obtain the optimum process parameters. One of the issues is the limited space between the comer solder bump and the edge of the package for the underfill material. In general, most of the packages have full array or perimeter solder ball patterns, so the available space between the package edge and the first solder ball was quite small.

Another concern was to determine the appropriate placement force, since the underfill dot diameter would increase after placement. In this case, the dispensed underfill dot may contact the solder paste in the corner CSP site, which would eventually lead to a bad solder joint shape or a solder joint failure after reflow, as shown in Figures 2.4, 2.5 and 2.6. In order to avoid any contamination of the solder paste deposits with underfill material, it was extremely important to apply an appropriate and consistent underfill volume (diameter and height) for a particular package, which would depend on the gap between the substrate and package and the available space between the package outside edge and the closest of the solder balls. In this study, the optimized placement force was 9N, and the underfill volume was determined to be 0.64 $\mu l$.

The typical underfill dot geometry was peaked (like a Hershey kiss). Trial and error revealed that if the center of the adhesive dot was located at the edge of the package, then there was minimal interference with the corner bump solder joint formation. This position also allowed for a fillet to be formed with the corner of the package.

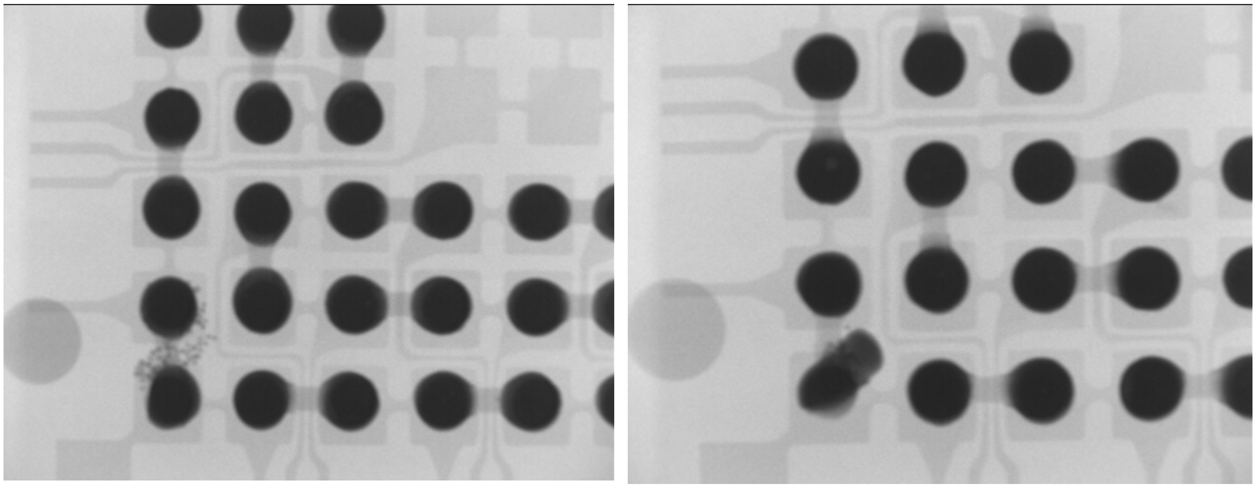


Figure 2.4 X-ray Pictures of Underfill Contacting the Solder Paste

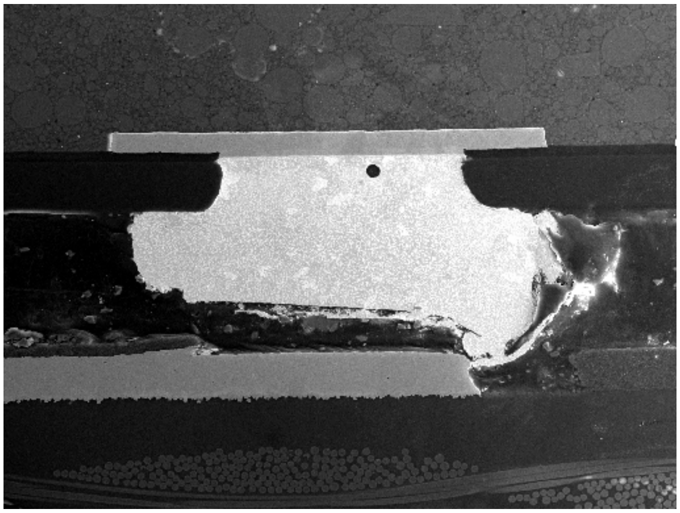


Figure 2.5  Underfill was Pushed into the Solder Paste, Causing Solder Joint Failure

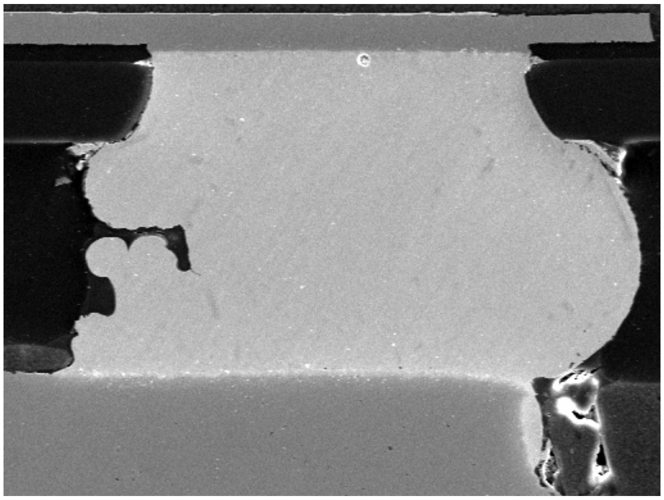


Figure 2.6 Underfill Touching Solder Paste, Causing a Bad Solder Joint Shape

### 2.2.3 Effect of Dispensing Pressure on Underfill Volume Consistency

The test vehicles were assembled on an automated SMT line at Auburn University. No-clean solder paste was printed with an MPM AP25 stencil printer using a 4 mil thick, laser cut, electro-polished, nickel plated stencil. The solder paste print was then inspected. For those CSPs assembled with corner bond underfill (Loctite 3515), the underfill was dispensed with a Camalot 3700 dispensing system after the solder paste printing.

Dispensing was conducted using a rotary pump dispensing system. Four dots were dispensed at the four corners of the CSP site (Figure 2.7). No board heat was used. The dot was positioned so that the corner of the CSP was in the center of the dispensed dot (Figure 2.8).

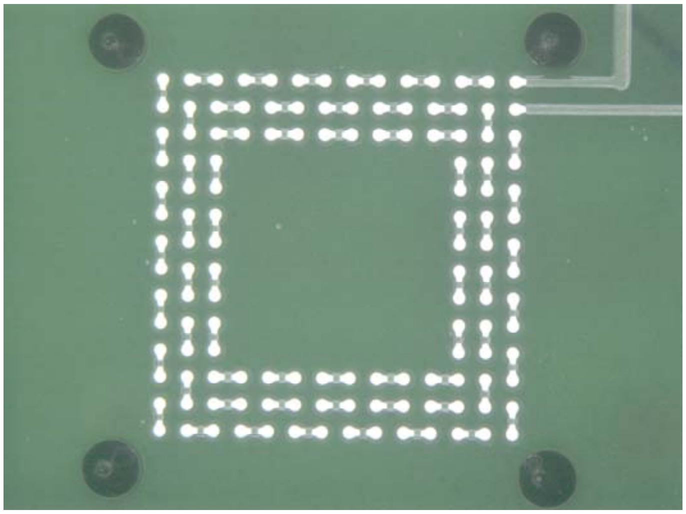


Figure 2.7 Corner Dot Dispensing Pattern.

Figure 2.8 CSP Placed into Corner Dot Underfill.

Dispensng experiments were performed to optimize the dispensing process. Since the viscosity of the underfill was higher than that of traditional capillary flow underfills, the effect of fluid pressure on dot volume consistency was measured using the volumetric measuring system on the dispensing system. The dispensing time was varied to maintain the same volume of 0.64 $\mu l$ at the two fluid pressures. For the high pressure 1.2 bar, shot time was 270 msec, and for the low pressure 0.6 bar, the shot time was 370 msec. The distance between the needle and board surface was 0.028 in for both pressures.

The control chart and the results of the process capability under high pressure and low pressure are shown in Figures 2.9 to 2.12. It can be seen from Figure 2.9 that there are three points that fall outside the LSL (Low Specification Limit) for the low pressure 0.6 bar process, and this process is therefore out of control. Figure 2.10 shows a frequency histogram of an observed data sample, together with the best-fitting normal distribution for the low pressure process. It can be seen that the process mean (0.6353 $\mu l$) of low pressure dispensing falls short of the target (0.64 $\mu l$ ), and the left and right tail of the distribution fall outside the lower specification limit (LSL) and upper specification limit (USL), respectively. For the high pressure 1.2 bar process, all of the data points fall within the specification limits as shown in control chart Figure 2.11. The process mean of the high pressure dispensing (0.64 $\mu l$) matches the target (0.64 $\mu l$), and all of the distributions fall inside the lower specification limit (LSL) and upper specification limit (USL), which indicates that the process is statistically in control.

$C_{pk}$ is an index that measures how close a process is to the target and how consistent the process is around the average performance [76]. A process may be running with minimum variation, but it can drift away from the target towards one of the specification limits, which indicates lower $C_{pk}$, whereas $C_p$ will be high. On the other hand, a process may be on average exactly at the target, even if the variation in performance is high (as long as it is lower than the tolerance band (i.e. specification interval). In such cases $C_{pk}$ will be lower, and $C_p$ will be high. $C_{pk}$ will be higher only when the process is meeting the target consistently with minimum variation. The general rule of thumb states that if a $C_{pk}$ value of a process is less than 1.33, then the process is incapable of producing a repeatable part.

The $C_{pk}$ index indicates whether the process will produce units within the tolerance limits. The $C_{pk}$ index for the low pressure 0.6 bar process was only 0.38, indicating that the process is out of control and some process parameters need to be optimized to reduce variability and center the process on the target. The $C_{pk}$ index for the high pressure 1.2 bar was 1.86 > 1.33, indicating that process is capable and under control.

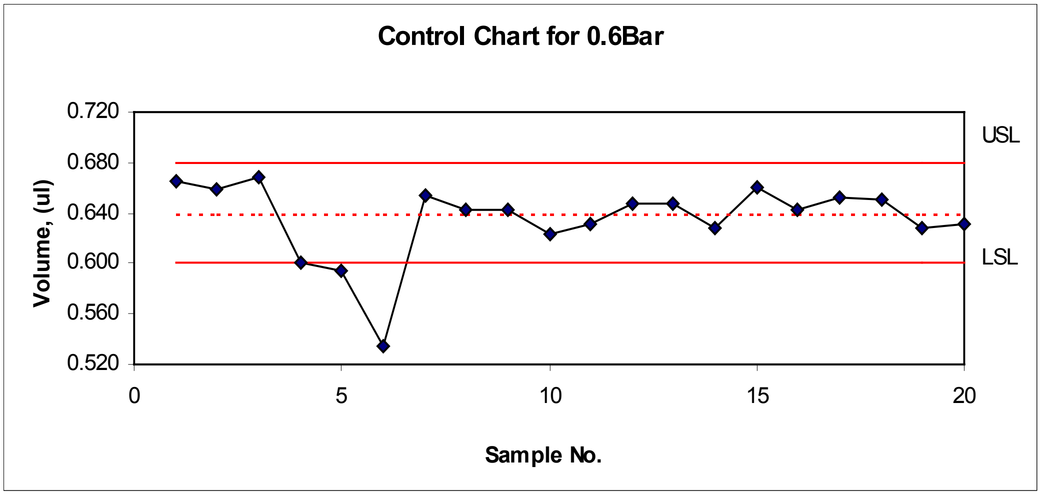
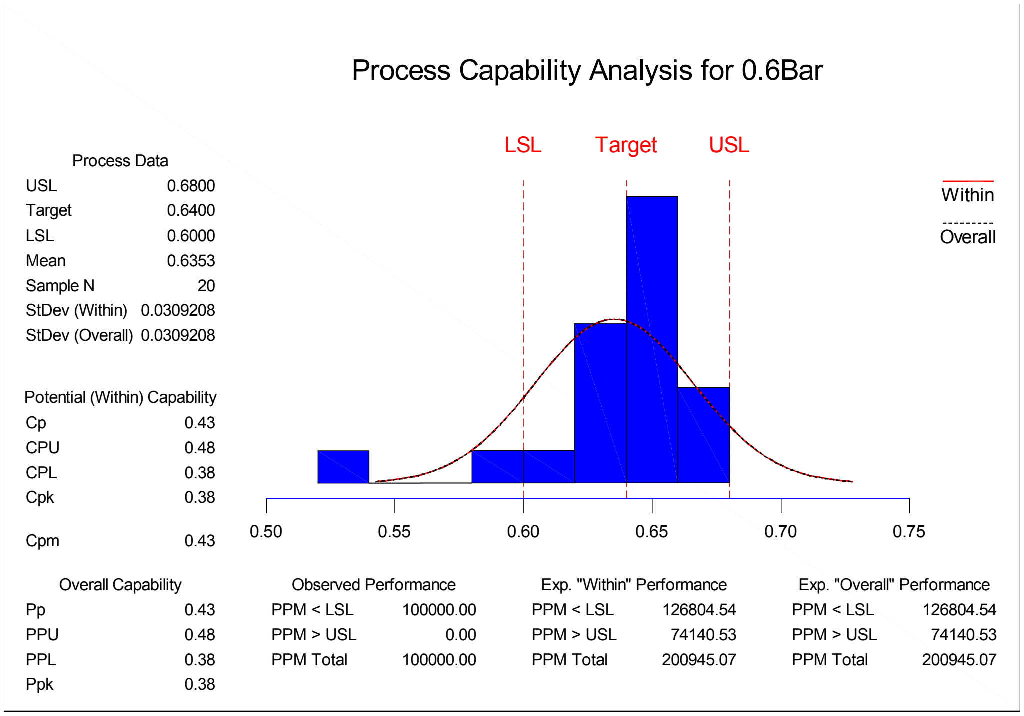


Figure 2.9 Control Chart of Underfill Volume at 0.6 Bar



| Process Data | |
|---|---|
| USL | 0.6800 |
| Target | 0.6400 |
| LSL | 0.6000 |
| Mean | 0.6353 |
| Sample N | 20 |
| StDev (Within) | 0.0309208 |
| StDev (Overall) | 0.0309208 |

| Potential (Within) Capability | |
|---|---|
| Cp | 0.43 |
| CPU | 0.48 |
| CPL | 0.38 |
| Cpk | 0.38 |
| Cpm | 0.43 |

| Overall Capability | |
|---|---|
| Pp | 0.43 |
| PPU | 0.48 |
| PPL | 0.38 |
| Ppk | 0.38 |

| Observed Performance | | Exp. "Within" Performance | | Exp. "Overall" Performance | |
|---|---|---|---|---|---|
| PPM < LSL | 100000.00 | PPM < LSL | 126804.54 | PPM < LSL | 126804.54 |
| PPM > USL | 0.00 | PPM > USL | 74140.53 | PPM > USL | 74140.53 |
| PPM Total | 100000.00 | PPM Total | 200945.07 | PPM Total | 200945.07 |

Figure 2.10 Process Capability Analysis of Underfill Volume at 0.6 Bar

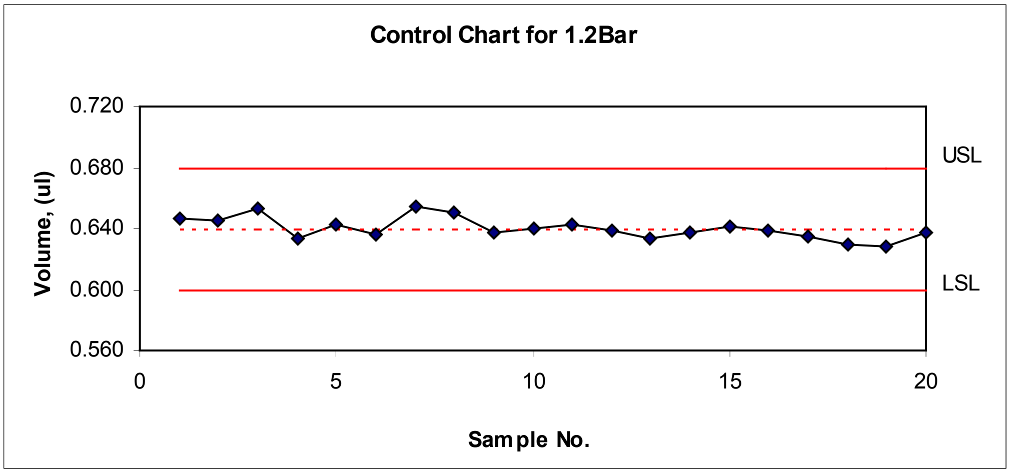


Figure 2.11 Control Chart of Underfill Volume at 1.2 Bar

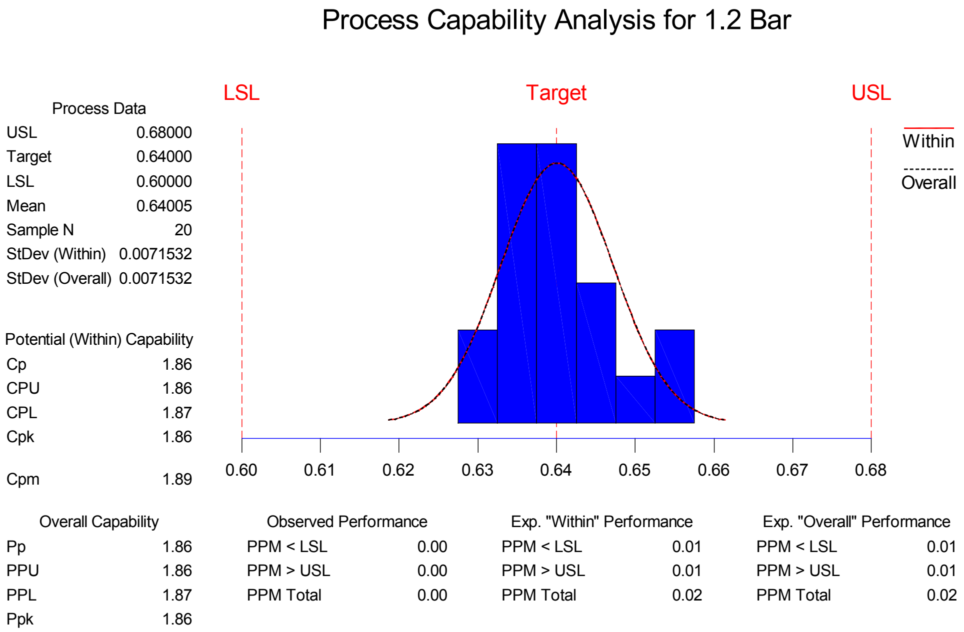
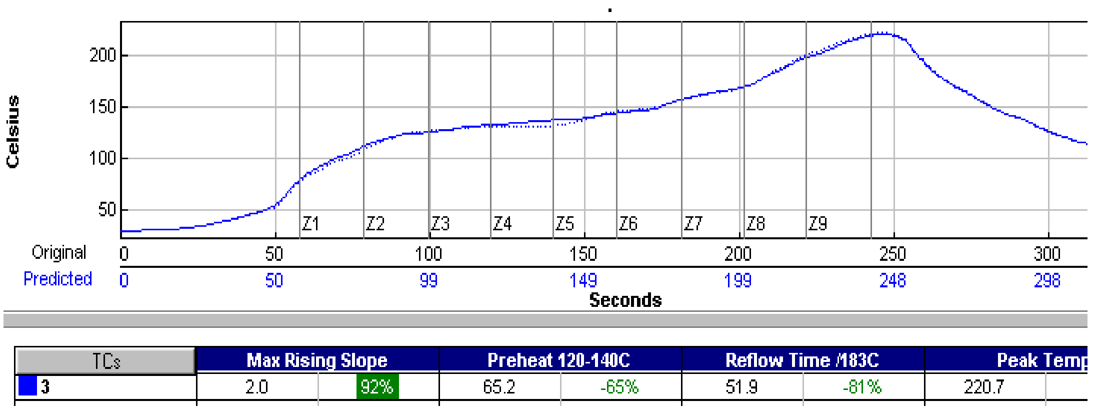


Figure 2.12 Process Capability Analysis of Underfill Volume at 1.2 Bar

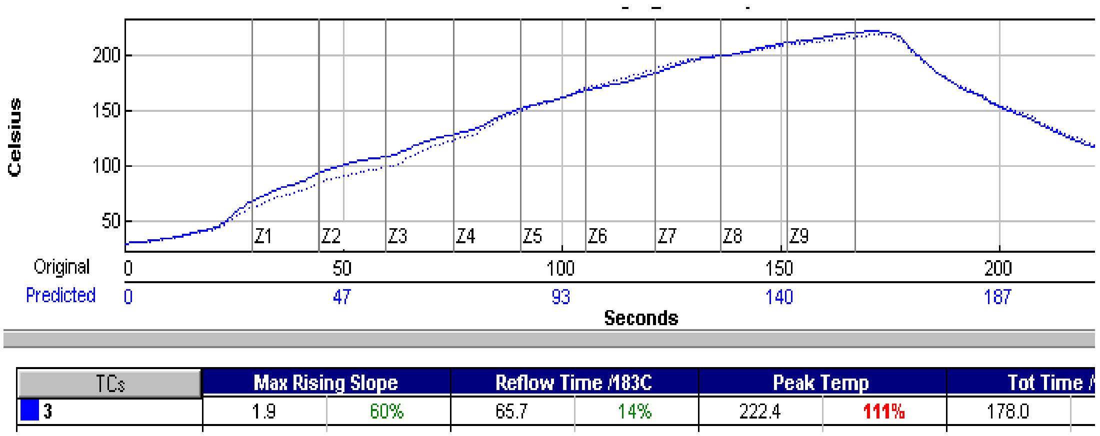
### 2.2.4 Reflow Profile and Underfill Cure

The CSPs were placed with a Siemens F5 machine using a placement force of nine Newtons. The boards were then reflowed in a Heller 1800 EXL furnace in air. Two profiles were evaluated. Figure 2.13 shows a conventional profile with a soak prior to reflow. For low mass, high volume portable product boards, ramp profiles (Figure 2.14) are generally used to reduce the total time in the furnace, increasing throughput.



| TCs | Max Rising Slope | | Preheat 120-140C | | Reflow Time /183C | | Peak Temp | |
|---|---|---|---|---|---|---|---|---|
| 🟦 3 | 2.0 | 92% | 65.2 | -65% | 51.9 | -81% | 220.7 | |

Figure 2.13 Conventional Soak Reflow Profile.



| TCs | Max Rising Slope | | Reflow Time /183C | | Peak Temp | | Tot Time / | |
|---|---|---|---|---|---|---|---|---|
| 🟦 3 | 1.9 | 60% | 65.7 | 14% | 222.4 | 111% | 178.0 | |

Figure 2.14 Ramp Reflow Profile.

Differential scanning calorimetry (DSC) was used to evaluate the underfill cure with each of the two profiles. For comparison, a sample was cured for 45 minutes at 150°C in a box oven. A DSC plot of an uncured sample is also plotted. As shown in

Figure 2.15, there is no exotherm associated with either reflow profile, indicating a high degree of cure. Figures 2.16 and 2.17 show cross sections of the solder joints for both profiles and indicate good wetting and collapse, where the underfill does not become too viscous before the solder collapses. For the subsequent experimental work, the ramp profile was used.

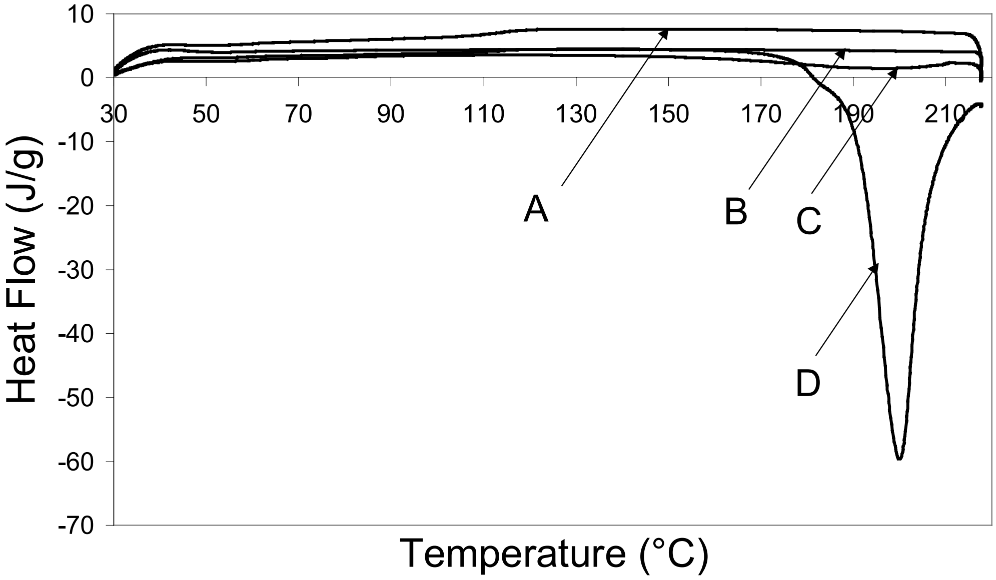


Figure 2.15 DSC of Loctite 3515 (A- Soak, B - Ramp, C - Box Oven, D - Uncured);

(Heating rate = 20°C/min., Purge gas = Nitrogen (50 ml/min).

Instrument Model - TA Instruments DSC2920 Modulated DSC.

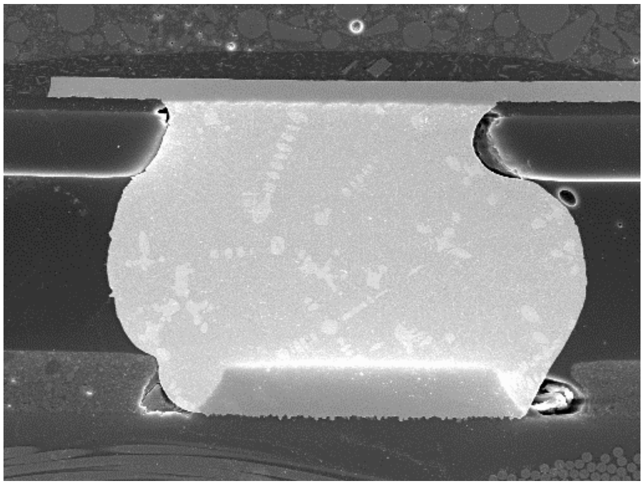


Figure 2.16 Cross Section of Solder Joint Showing Excellent Wetting with Soak Profile.

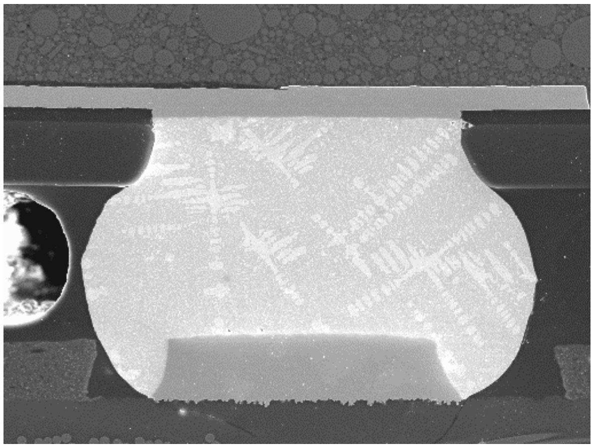


Figure 2.17 Cross Section of Solder Joint Showing Excellent Wetting with Ramp Profile.

### 2.2.5 Self-alignment Capability of Corner Bonding CSPs

In order to check the self-alignment capability of corner bonding underfilled CSPs a corner underfill dot was dispensed at each corner of the CSP site on the board, and then a CSP was intentionally placed with 50% offset (5mil off center) in the x-direction to simulate the worst mis-alignment case, in which the solder ball center was placed on the pad edge, an X-ray image of a CSP with a 50% offset is shown in Figure 2.18, After reflow, the CSP had self-centered (Figure 2.19) indicating no influence of the underfill dots on self-centering.

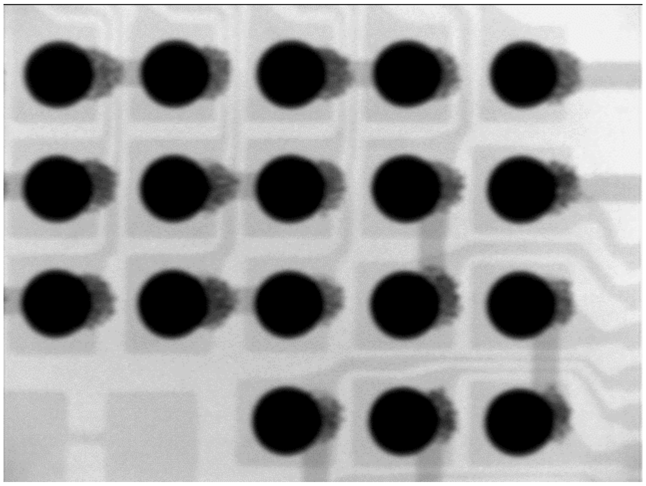


Figure 2.18 X-ray Image of a CSP Intentionally Placed with a 5 mil (50%) Offset.

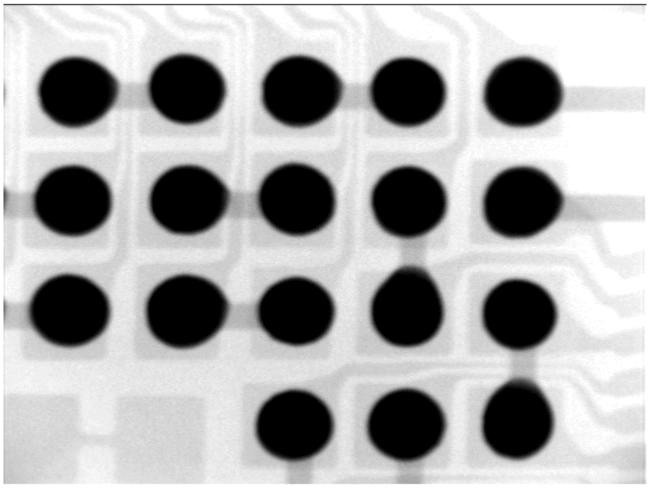


Figure 2.19 X-ray of CSP after Reflow.

For comparison, CSPs with no underfill and with capillary flow underfill (Loctite 3593) were also built using the ramp reflow profile. For the capillary flow underfill, the boards were dehydrated at 125°C for fifteen hours prior to underfill dispensing. The dehydration bake was necessary to remove moisture absorbed by the board during the time between reflow and the underfill dispensing [74]. An ‘L’ shaped dispensing pattern was used. The underfill was cured in a box oven at 165°C for five minutes. Samples were flat sectioned to verify a complete underfill with no voids. As has been previously shown, there were pockets of trapped flux residue around the base of the solder balls [65, 74].

### 2.2.6 Rework of Corner Bonding CSPs

Although defects are never planned, they do occur on occasion even in controlled processes. The ability to rework an underfilled device is an advantage, which can substantially reduce scrap costs. Since the corner bond material does not completely underfill the CSP, the reworkability of the underfill was investigated.

As shown in Figure 2.20, the shear strength of corner bond underfill dots decreases dramatically above 100°C [77]. At rework temperatures, the mechanical strength is less than 20% of its room temperature value. This allows removal of the CSP for rework. Using an Air-Vac DRS 24C rework station, CSPs were removed at a temperature of 220°C using a small tool to apply a very low amount of force to the corner bonds.

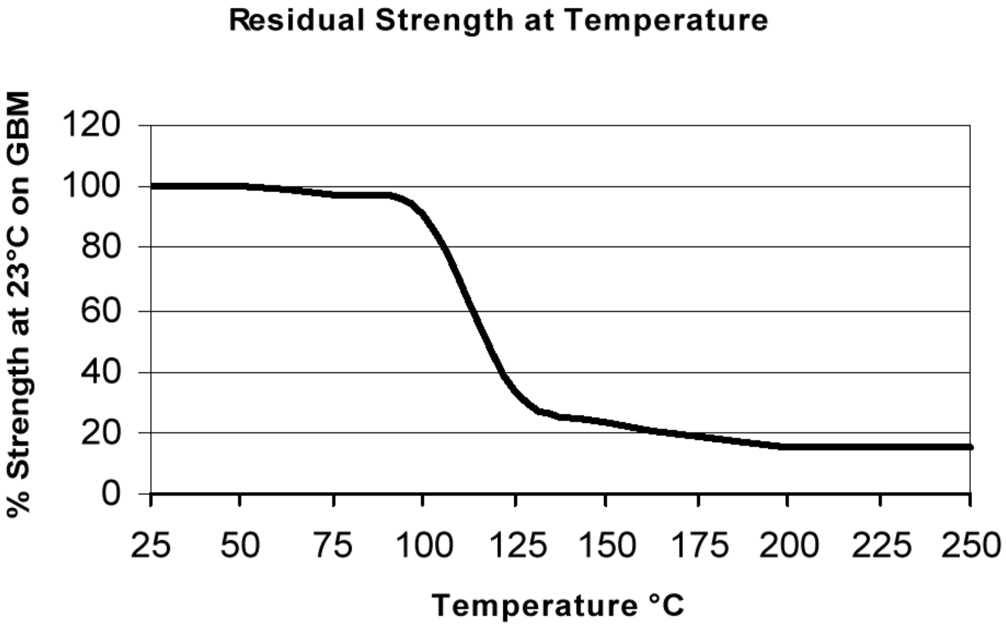


Figure 2.20 Shear Strength of Corner Bond Underfill Dots as a Function of Temperature [77].

The board was heated from the bottom (with IR) and from the top (with hot air) to remove the soldered and underfilled package. The next step was to remove the cured underfill residues from the solder mask layer (on the board). The board was again heated from the bottom (measured board temperature: 90°C) and the top (measured board temperature: 140°C).

As shown in Figure 2.21, the CSP can be removed with no damage to the board. There is corner bond underfill residue remaining. Using the dressing tool on the rework station, most of the underfill can be removed (Figure 2.22).

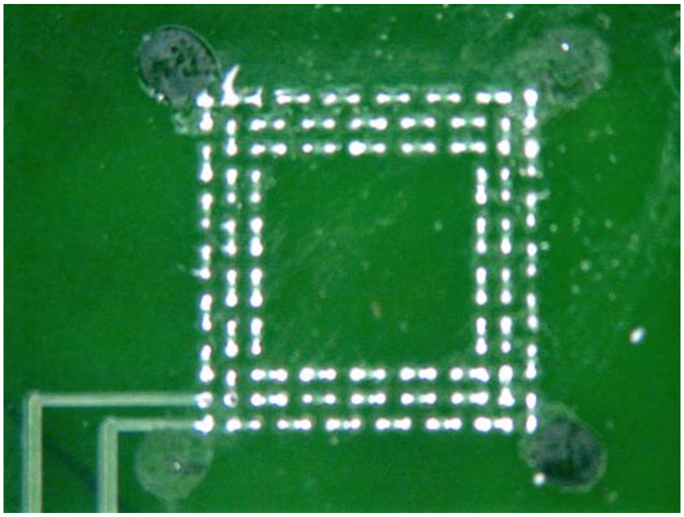


Figure 2.21 CSP Site after CSP Removal.

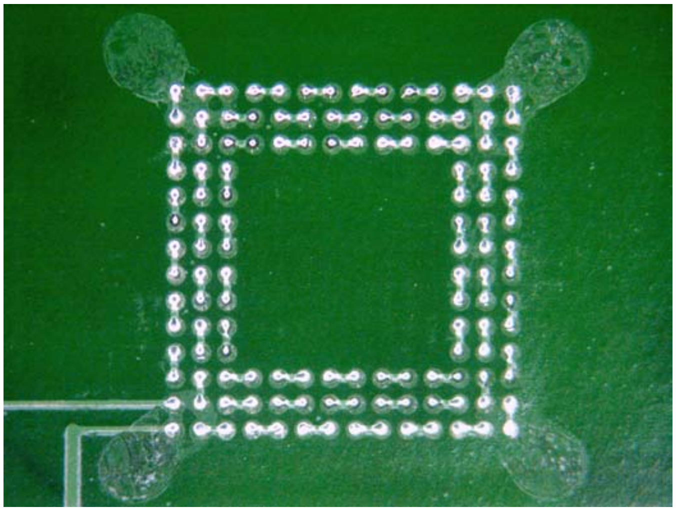


Figure 2.22 CSP Site after Dressing.

It is not necessary to remove all the residue, since there is no degradation of the underfill during rework. To verify this, underfill dots were dispensed and reflow cured. Then the bulk of the dot was removed using the rework station dressing tool. A second underfill dot was dispensed over the residue and reflow cured. The second dot was shear tested with a Dage 2400 shear tester. In all cases, the failure mode was cohesive failure in the PCB laminate - chunks of laminate were pulled out, exposing the glass fiber bundles.

For reassembly, a flux dip, underfill dispense, place and reflow process was used. The drop test and liquid-to-liquid thermal shock performance of flux-only assembly has been shown to be comparable to using solder paste and is suitable for repair [78].

### 2.3 Drop Test

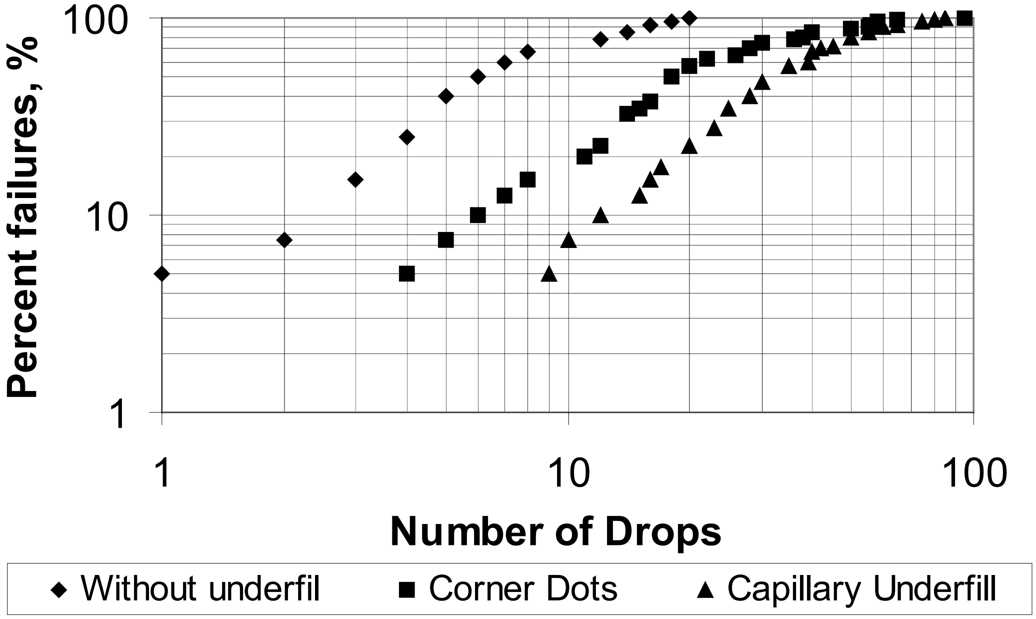


Figure 2.23 Drop Test Results.

For mechanical shock testing, a 31.8 gram weight was attached to one end of the board as shown in Figure 2.2 to accelerate failure and simulate product weight. The board was then dropped through a six foot long, three inch diameter tube onto a concrete floor. The daisy chain resistance of each CSP was measured and a 10% increase in resistance was recorded as a failure.

Four boards (40 CSPs) were tested for each assembly type and the results are shown in Figure 2.23. As can be seen in the plot, capillary underfill provides the most reliable assembly, with the corner dots providing approximately a 3-4x improvement compared to no underfill.

## 2.4 Failure Analysis

*No Underfill:* Cross sections were made of failed CSPs after drop testing. Figure 2.24 shows failure in the solder on the package side with no underfill.

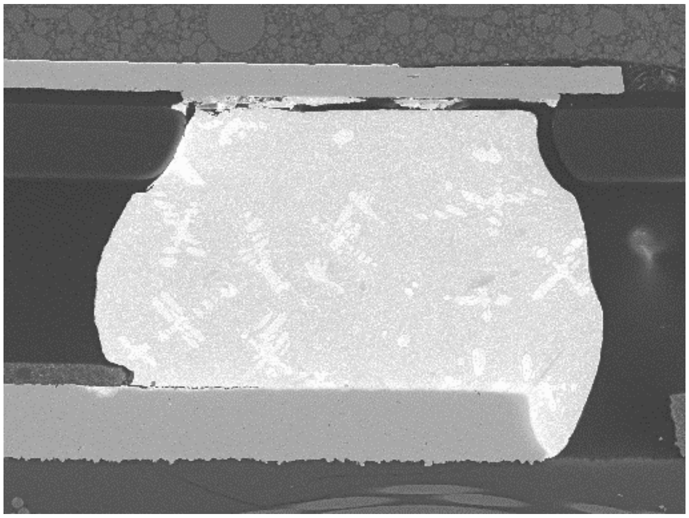


Figure 2.24 Cross Section of Failed Solder Joint (No Underfill).

Figure 2.25 shows a cracking in the printed circuit board under the solder pad. In some cases, the entire CSP came away from the board due to cohesive failure in the laminate material. The copper pads and chunks of laminate were removed, leaving exposed glass fiber bundles. In some cases, the part had been electrically good on the drop just before the drop in which the CSP came off the board, thus a massive failure.

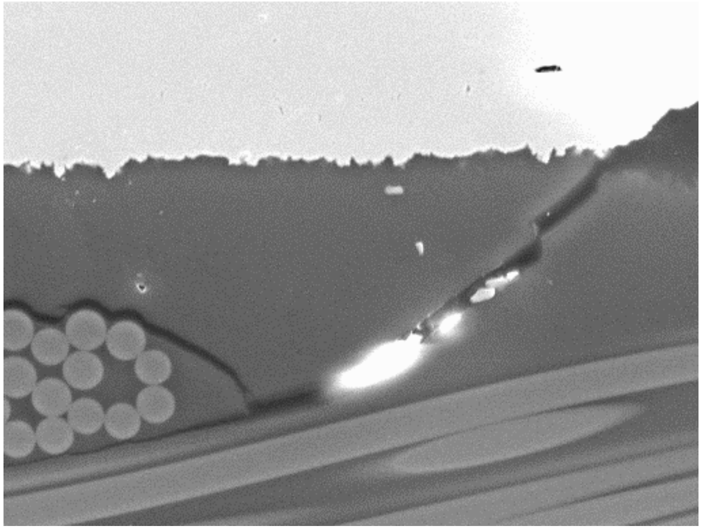


Figure 2.25 Crack in Laminate under Solder Pad (No Underfill).

*Corner Bond:* Figure 2.26 shows cracking of the corner bond underfill after drop testing. At the end of the drop test (a total of 80 drops) there was cracking of at least one dot of the corner bond material on each CSP. Figure 2.27 shows cracking of the copper and laminate after drop testing. Although not as common, some CSPs from corner bonded samples came completely off the board during drop testing. In most case, electrical failure had already occurred.

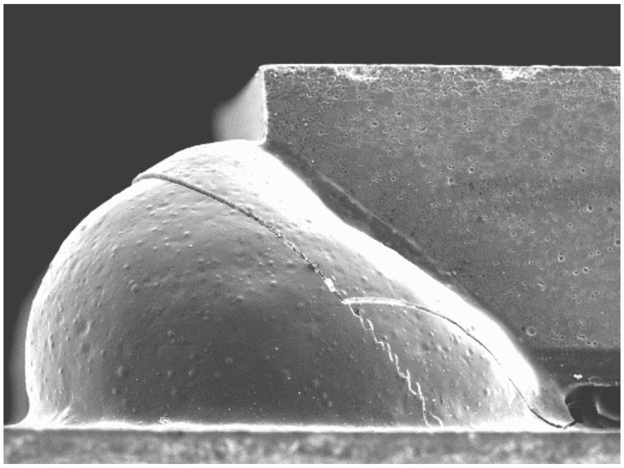


Figure 2.26 Photograph of Cracked Corner Bond Underfill after Drop Testing.

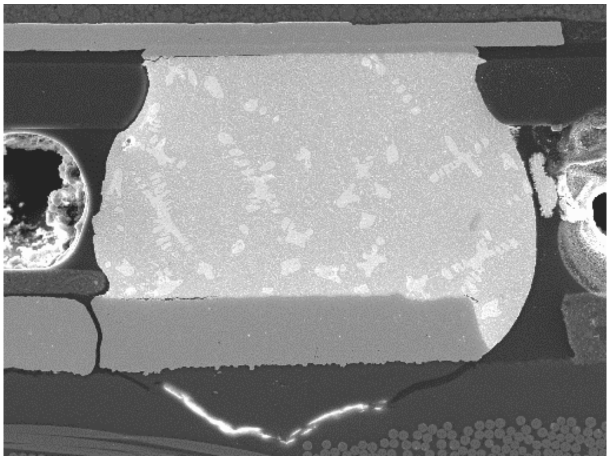
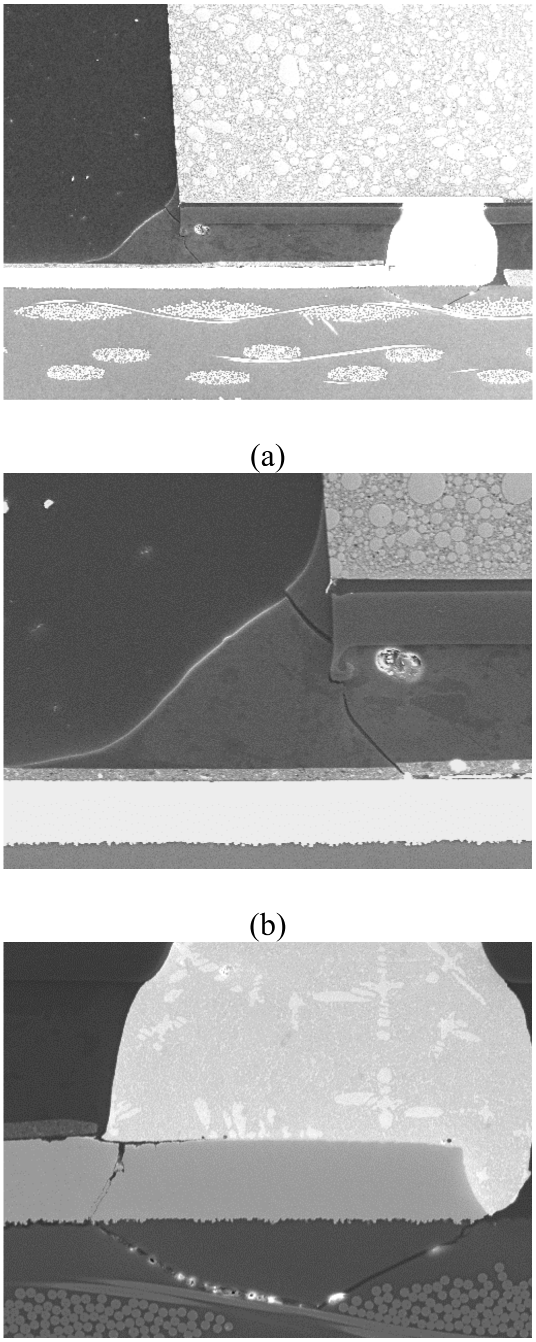


Figure 2.27 Cracking of Copper and Laminate after Drop Testing. Sample was Corner Bonded.

Figure 2.28 shows a failure with the capillary underfill. The crack had propagated from the underfill fillet, along the solder mask-copper interface, then through the copper trace and into the laminate. Again, there were a few instances in which the CSP came off the board during the drop test (100 total drops per board).



(a)

(b)

(c)

Figure 2.28 Cross Section of Crack in Capillary Underfilled CSP after Drop Test (a - low magnification). (b) Close-up of Crack in Underfill Fillet. (c) Close-up of Crack in Copper and Laminate.

### 2.5 Summary

Corner bonded underfill provides a simplified manufacturing process for CSPs that require underfill, eliminating the dehydration bake, capillary flow time and cure. Dispensing guidelines have also been provided for applying the material in a way that will not interfere with the soldering process. The material has also been shown to have only a minimal impact on the process, curing during the solder reflow, and allowing the parts to self-align. While the drop test reliability is not as high as with a complete capillary underfill, corner bonded underfill provides a 3-4 x improvement compared to no underfill. Corner bonding underfill is a viable, cost-effective approach for many portable product applications.

# CHAPTER 3

# LEAD-FREE ASSEMBLY AND DROP RELIABILITY OF CHIP SCALE PACKAGES

## 3.1 Introduction

Portable products face the challenges of ever increasing functional density, shorter product cycles, and pressure to reduce costs. Increasing functional density has led to an explosive growth in chip scale package (CSP) usage.

The expected product life for a portable product is typically short compared to many other product categories; however, portable products must be able to survive multiple drops. The decreasing I/O pitch of CSPs and the resulting smaller pads and solder joints, make the drop requirement more challenging. There are two approaches to improving drop reliability. The first is enhancing the mechanical design of the product to minimize the shock and flexing of the printed circuit board that occurs when the product is dropped. However, this approach places pressure on the time-to-market constraint. The second approach is to use underfills to mechanically reinforce the CSP solder joints [65-66]. This adds cost and cycle time to the manufacturing process.

With the proliferation of portable products and their short product life, there is growing concern over the resulting waste stream. Whether through legislative activity in

Europe or global market pressure, a growing percentage of portable electronics are lead-free.

In this chapter, three underfill options compatible with lead-free assembly have been evaluated: capillary underfill, fluxing underfill and corner bond underfill. CSPs with eutectic Sn/Pb solder were used for control samples. The effect of aging on the drop test results with lead-free solder and either no underfill or corner bond underfill was also studied. Thermal aging was used to simulate drop performance after the product had been placed in service for some period of time. The assembly processes, drop test results and failure analysis are presented.

## 3.2 Test Vehicle

The test vehicle was a four-layer test board with ten CSP attachment sites per side. In these experiments, CSPs were only assembled on one side of the board. Standard technology (FR4) was used for board fabrication, with no build-up or HDI layers. The board was 2.95" by 7.24" by 0.042" thick. The pads were 0.010” in diameter, non-solder mask defined with an immersion silver finish.

The CSP was a 8mm, 0.5mm pitch, 132 I/O TapeArray manufactured by Amkor Technology and purchased from Practical Components (A-TArray132-.5mm-8mm-DC-LF). The I/Os were on a 14 x 14 array with only the outer three rows populated. The lead-free solder ball composition was 95.5%Sn/4.0%Ag/0.5%Cu. CSPs with eutectic 63%Sn/37%Pb solder balls were used for comparison. The CSP was a daisy chain test part for continuity measurements. The silicon die was 3.98mm x 3.98mm.

Multicore LF300 lead-free solder paste (type 3, 95.5%Sn/3.8% Ag/0.7%Cu) was used for the lead-free assemblies. Multicore MP200 63Sn/37Pb, type 3 solder paste was used for the Sn/Pb assemblies. Table 3.1 lists the properties of the underfills investigated. The table also indicates which materials were used for Sn/Ag/Cu and/or eutectic Sn/Pb assembly.

Table 3.1 The Properties of the Underfill Investigated

| Material | 3593 | FP6101 | CNB933-25 | 3515 | CNB951-01 |
|---|---|---|---|---|---|
| Underfill Type | Capillary - A | Capillary - B | Fluxing | Corner Bond | Corner Bond |
| Solder Alloy | Sn/Ag/Cu<br>& Sn/Pb | Sn/Ag/Cu<br>& Sn/Pb | Sn/Ag/Cu | Sn/Pb | Sn/Ag/Cu |
| $T_g$ (°C) | 110 | 10 | 83 | 122 | 150 |
| CTE Below $T_g$ (ppm/°C) | 50 | 83 | 77 | 47 | 60 |
| CTE Above $T_g$ (ppm/°C) | 160 | 211 | 190 | 165 | 155 |
| Modulus (MPa) | 2069 | 50 | 2600 | 2297 | 3800 |

## 3.3 Assembly Process

### 3.3.1 No-Underfill

Figure 3.1 schematically illustrates the common steps of the conventional no-underfill process. The test vehicles were assembled on an automated SMT line at

Auburn University. The solder paste was printed with an MPM AP25 stencil printer using a 4 mil thick, laser cut, electro-polished, nickel plated stencil. The aperture opening was a 10 mil square. The solder paste print was inspected with an MVT 3-D solder paste inspection system. Assembly was performed with a Siemens F5 pick & place system.

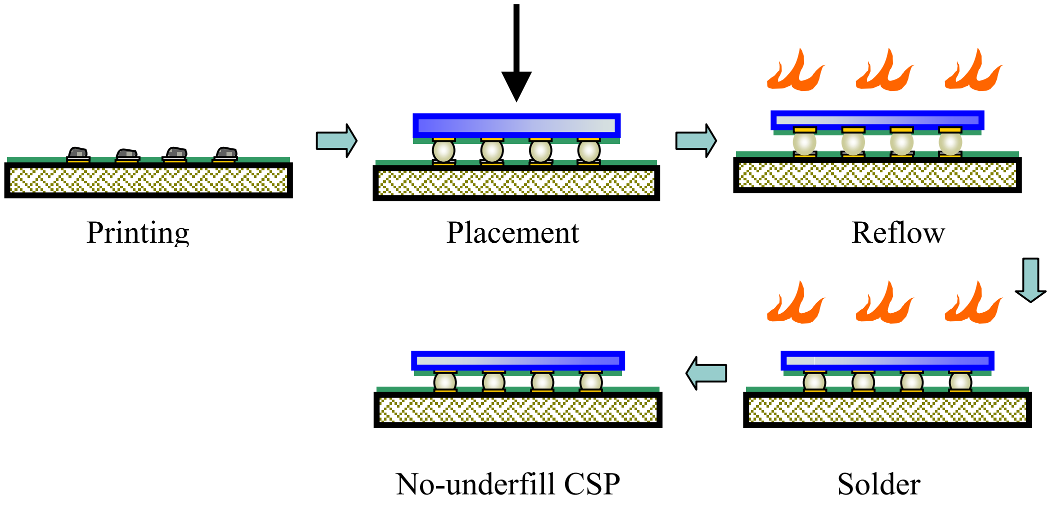
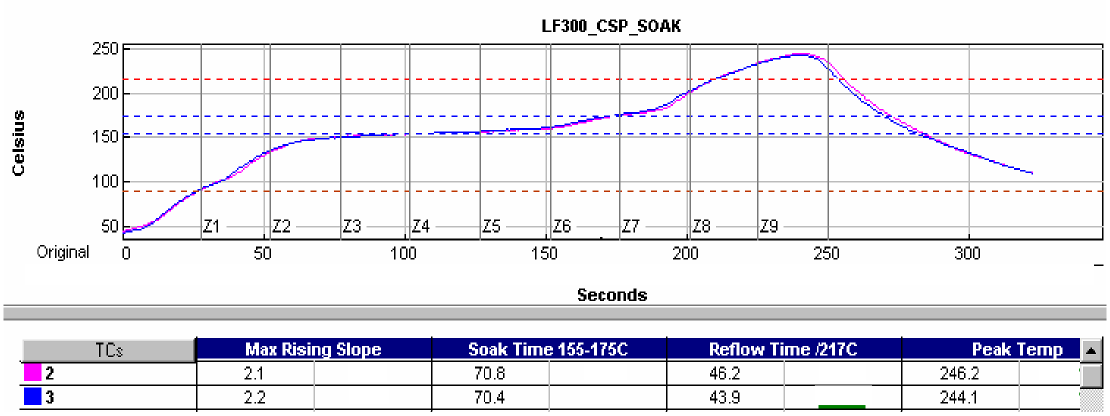


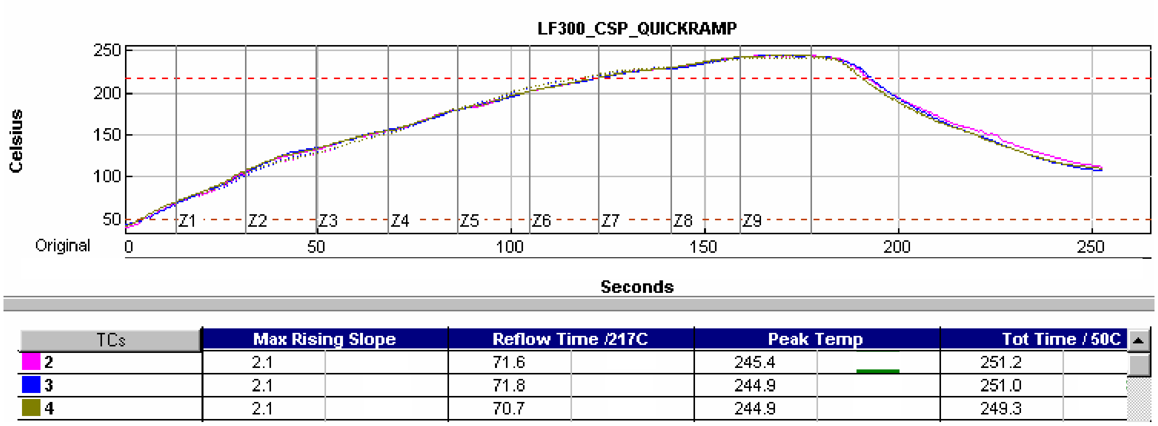
Figure 3.1 No-Underfill Process

A Heller 1800 reflow furnace was used to evaluate two reflow profiles for the lead-free assembly. The first profile, shown in Figure 3.2, is a ‘traditional soak’ profile. Figure 3.3 is a straight ramp-to-peak profile, often used in portable electronics assembly since the overall reflow time is shorter. CSPs assembled with both profiles were examined with a Phoenix X-ray system. While there was some minor voiding in the solder joints (Figure 3.4), there was no significant difference in voiding between the two reflow profiles. Figure 3.5 shows cross sections of solder joints for both profiles and indicate good wetting and collapse. The ramp-to-peak profile was used for all subsequent lead-free assemblies. A ramp profile with a peak temperature of 221°C was used for the eutectic Sn/Pb assembly (Figure 3.6).



| TCs | Max Rising Slope | Soak Time 155-175C | Reflow Time /217C | Peak Temp |
|---|---|---|---|---|
| 🟪 2 | 2.1 | 70.8 | 46.2 | 246.2 |
| 🟦 3 | 2.2 | 70.4 | 43.9 | 244.1 |

Figure 3.2 ‘Soak’ Reflow Profile for Lead-free Assembly.



| TCs | Max Rising Slope | Reflow Time /217C | Peak Temp | Tot Time / 50C |
|---|---|---|---|---|
| 🟪 2 | 2.1 | 71.6 | 245.4 | 251.2 |
| 🟦 3 | 2.1 | 71.8 | 244.9 | 251.0 |
| 🟫 4 | 2.1 | 70.7 | 244.9 | 249.3 |

Figure 3.3 Ramp-to-Peak Lead-free Reflow Profile.

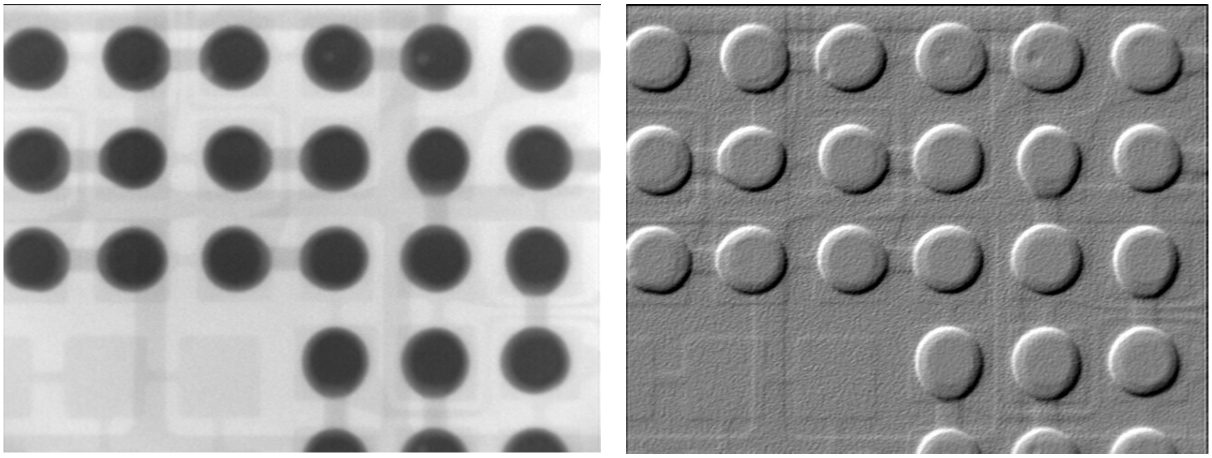
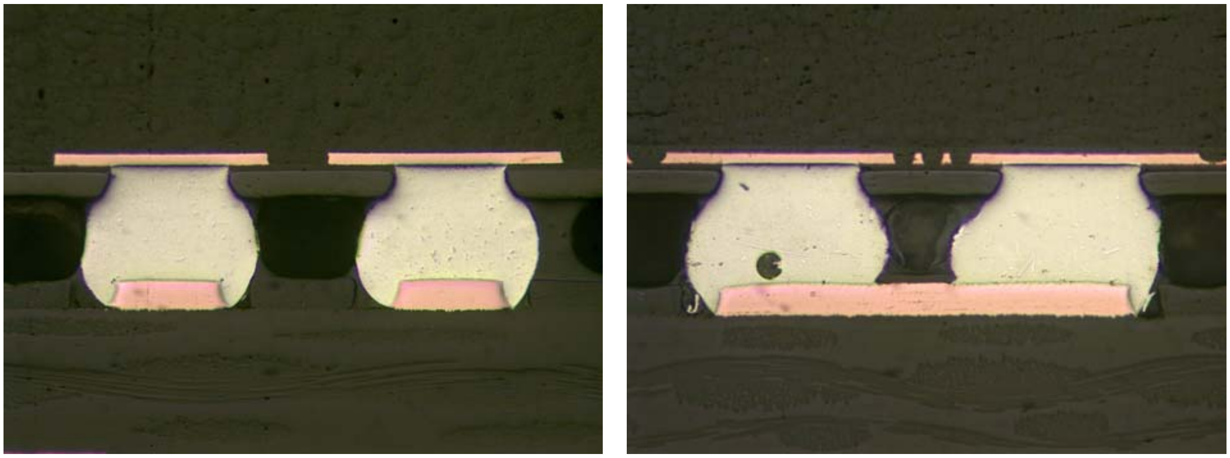


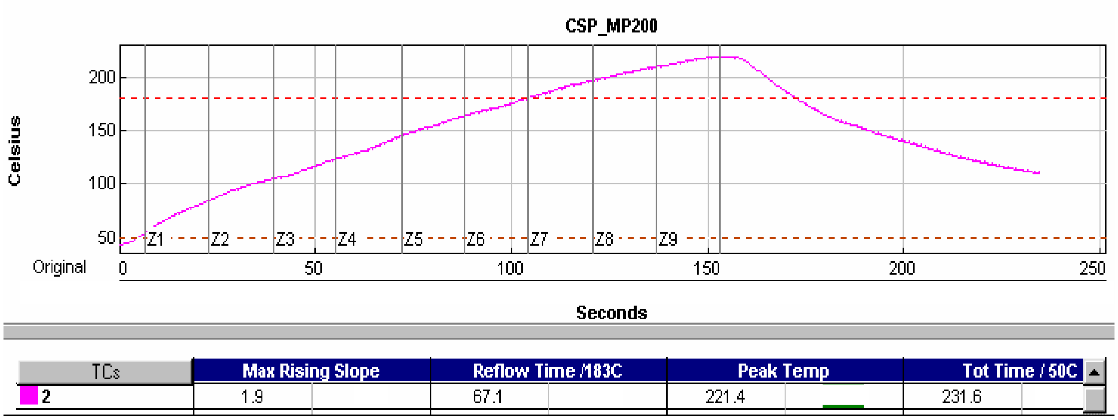
Figure 3.4 X-Ray Image of Lead-free Solder Joints (Ramp-to-Peak Profile).



(a) Ramp Profile

(b) Soak Profile

Figure 3.5 Cross Section of Solder Joint Showing Excellent Wetting with Ramp Profile and Soak Profile



| TCs | Max Rising Slope | Reflow Time /183C | Peak Temp | Tot Time / 50C |
|---|---|---|---|---|
| 2 | 1.9 | 67.1 | 221.4 | 231.6 |

Figure 3.6 Eutectic Sn/Pb Reflow Profile.

The wetting characteristics of Sn/Ag/Cu solders are typically not as good as for Sn/Pb solder. To evaluate the self-centering capability of the Sn/Ag/Cu alloy, CSPs were intentionally placed 50% off-pad (5 mils) in both the X and Y directions, as shown in Figure 3.7. After reflow the CSP had self-centered, as shown in Figure 3.8.

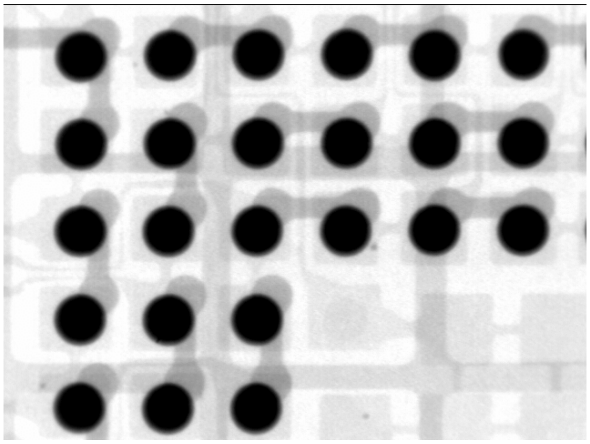


Figure 3.7 X-Ray Image of CSP Intentionally Placed 50% Off-pad in Both the X and Y Directions.

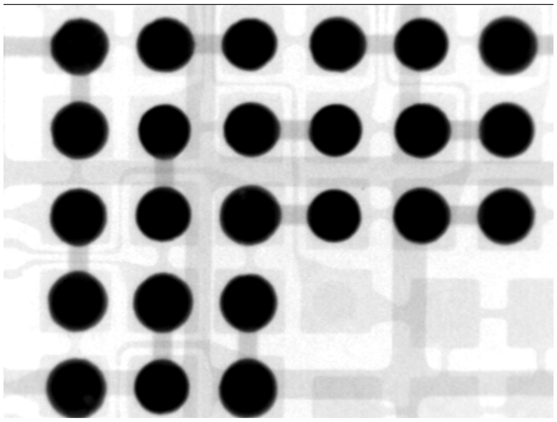


Figure 3.8 X-Ray Image after Reflow

### 3.3.2 Capillary Underfill

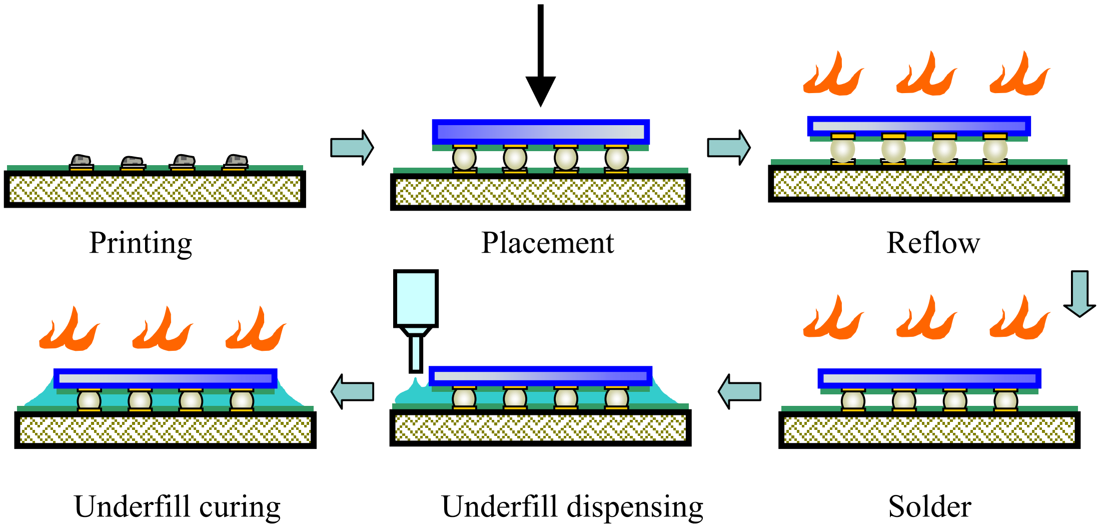


Figure 3.9 Capillary Underfill Process

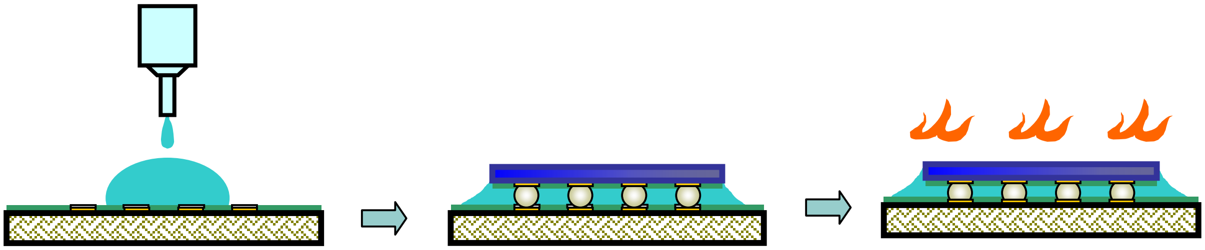
The capillary underfill process has been extensively studied since the extension of flip chip technology onto printed wiring boards (PWBs). As shown in Figure 3.9, the process follows the same assembly process as the no-underfill process up through the reflow step. After reflow, capillary flow underfill is dispensed and then cured in a box oven or an in-line oven. Capillary underfill has been commonly used in CSP assembly with eutectic Sn/Pb solder for portable electronics products.

For the capillary flow underfill, following reflow, the boards were dehydrated at 125°C for 12 hours prior to underfill dispensing. The dehydration bake was necessary to remove moisture absorbed by the board during the time between reflow and the underfill dispensing. In a continuous assembly process, this dehydration step may not be necessary since most of the moisture absorbed by the PCB would have been removed during the reflow cycle. However, in this experiment, there was a significant lag time between reflow and underfill, so a dehydration bake was required. Both eutectic Sn/Pb and lead-free assembles were made.

The capillary underfills were dispensed with a Camalot 3700 dispensing system. An 'L' shaped dispensing pattern was used. The FP6101 and 3593 underfills were cured for 5 minutes at 165$^{o}$C in a box oven. In-line conveyor ovens have also been used in the past. Samples were flat sectioned to verify a complete underfill with no voids.

### 3.3.3 Fluxing Underfill

As shown in Figure 3.10, the fluxing underfill process begins with dispensing a controlled amount of fluxing underfill at the CSP site on the board prior to CSP placement. No solder paste is printed at the site. The CSP is then placed onto the substrate with a pick and placement machine. During this step, the components squeeze the liquid underfill out until the solder balls contact the substrate pads. With a sufficient quantity of underfill, an underfill fillet can be also formed in this step. Finally the board is sent through a reflow oven to form the solder interconnects and cure the underfill simultaneously. In this study, a new fluxing underfill developed for compatibility with the higher lead-free solder reflow profiles was investigated.



Dispensing underfill Chip Placement Reflow and underfill cure

Figure 3.10 Fluxing Underfill Process

Compared to the capillary underfill process, this fluxing underfill process uses the fluxing underfill dispense to replace the solder paste printing and underfill flow steps, and integrates the solder reflow and underfill curing into a single step. Because there are no separate underfill dispensing and curing steps required, the fluxing process needs less equipment, speeding up the whole assembly process, and has a higher assembly throughput than the conventional capillary underfill process.

Although the fluxing underfill has the above advantages, in order to realize the process, the fluxing underfill must have the following two properties different from the traditional underfill [79]:

1. The fluxing underfill must provide fluxing capability to remove the surface oxide from the solder and the substrate metallization to promote solder wetting.
2. The underfill should remain flowable and have a reasonable low viscosity until the completion of solder wetting.

A successful fluxing underfill is also expected to fully cure in a single reflow cycle with a reflow profile similar to a typical SMT reflow profile. This will enable a mixture of other SMT components on the board to be reflowed at the same time, make the fluxing underfill process compatible with the SMT process.

Several issues and concerns with fluxing underfill are listed as follows.

1. Requires substrate bake out prior to assembly.
    a. The PCBs must be dehydrated to remove absorbed moisture.
    b. Complete the curing of undercured solder mask
2. Placement voids
3. Reflow profile sensitivity
4. Not reworkable
5. Little or no filler
    a. Filler particles impact assembly yield
    b. Higher CTE may impact thermal cycle reliability

#### 3.3.3.1 Fluxing Underfill Process Optimization

There are a number of factors related to the assembly process, such as the test vehicle, process variables and underfill materials. The process variables include dispensing stage temperature, placement force, placement velocity, placement dwell time, reflow profile and underfill volume. A better assembly result can be obtained through process optimization based on the design of experiments (DOE).

Only lead-free assemblies were built with fluxing underfill. Eutectic Sn/Pb CSP assembly with fluxing underfill has previous been studied [65]. Figure 3.11 shows a flat section (the CSP has been polished away) of an initial assembly after reflow. Significant placement voids were observed. Voids may be caused by air entrapped during placement, or moisture and volatiles in the PCB, or organic volatiles in the underfill. Voiding has been noted with fluxing underfills for eutectic Sn/Pb CSPs [65]. In that study, the voids did not degrade drop or liquid-to-liquid thermal shock performance. A DOE was performed to optimize the placement parameters for minimizing placement voids.

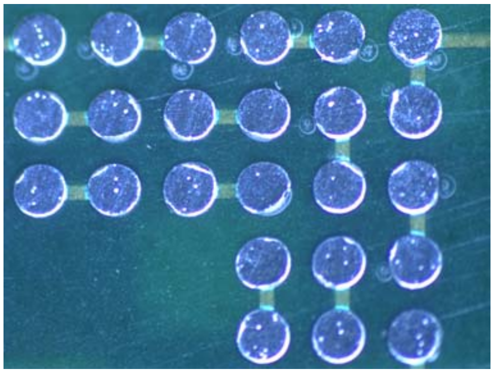


Figure 3.11 Flat Section (CSP Polished Away) of Fluxing Underfill Showing Voiding Before Placement Optimization.

The DOE used Taguchi's L9 ($3^4$) design. Four controllable factors: dispensing stage temperature, placement acceleration, placement force and placement dwell time were studied. Each of these controllable factors has three levels, as shown in Table 3.2. Taguchi's L9 test matrix is shown in Table 3.3.

Table 3.2 Controllable Factors

| Controllable Factors | Level 1 | Level 2 | Level 3 |
|---|---|---|---|
| A: Dispensing stage temperature, (°C) | 25 | 60 | 120 |
| B: Placement acceleration, (g) | 0.1 | 2.6 | 5.3 |
| C: Placement force, (N) | 1 | 5 | 10 |
| D: Placement dwell time, (s) | 0 | 1.5 | 3.0 |

Table 3.3 Taguchi L9 Test Matrix

| Run No. | DOE Controllable Factors | | | |
|---|---|---|---|---|
| | A: Stage temp. | B: Acceleration | C: Force | D: Dwell time |
| 1 | 25°C | 0.1g | 1N | 0s |
| 2 | 25°C | 2.6g | 5N | 1.5s |
| 3 | 25°C | 5.3g | 10N | 3s |
| 4 | 60°C | 0.1g | 5N | 3s |
| 5 | 60°C | 2.6g | 10N | 0s |
| 6 | 60°C | 5.3g | 1N | 1.5s |
| 7 | 120°C | 0.1g | 10N | 1.5s |
| 8 | 120°C | 2.6g | 1N | 3s |
| 9 | 120°C | 5.3g | 5N | 0s |

Since the voids were usually near the edge of a solder ball, as shown in Figure 3.12, flat–sectioning (polishing the CSP away) provided a better method for identifying and counting voids. Because less underfill voiding is desired, the design type is smaller-the-better (STB). Minitab 13.0 statistical analysis software was employed to analyze the data.

The response table for means is given in Table 3.4. And Figure 3.12 shows the main effects for means. The response tables show the average of the selected characteristic for each level of the factors. The response tables include ranks based on Delta statistics, which compare the relative magnitude of effects. The Delta statistic is the highest average for each factor minus the lowest average for each factor. Ranks are assigned based on Delta values; rank 1 is assigned to the highest Delta value, rank 2 to the second highest Delta value, and so on. The main effects plot provides a graph of the averages in the response table.

Table 3.4 Response Table for Means

| Level | Dispensing stage temp. | Acceleration | Force | Dwell Time |
|---|---|---|---|---|
| 1 | 110.33 | 116.89 | 108.00 | 128.11 |
| 2 | 124.22 | 122.00 | 134.667 | 122.00 |
| 3 | 152.44 | 148.11 | 144.33 | 136.89 |
| Delta | 42.11 | 31.22 | 36.33 | 14.89 |
| Rank | 1 | 3 | 2 | 4 |

From Table 3.4 and Figure 3.12, the response table and main effects plots for means both show that the factor with the greatest effect on the mean is factor A, dispensing stage temperature (Delta = 42.11, Rank = 1). When dispensing at a high stage temperature, a dome shape is difficult to form, and a relatively flat underfill surface tends to trap voids when placing. Factor C (placement force) and factor B (placement acceleration) are also strong factors, which have an obvious effect on the placement voids, while factor D (placement dwell time) has an intermediate effect on placement voids.

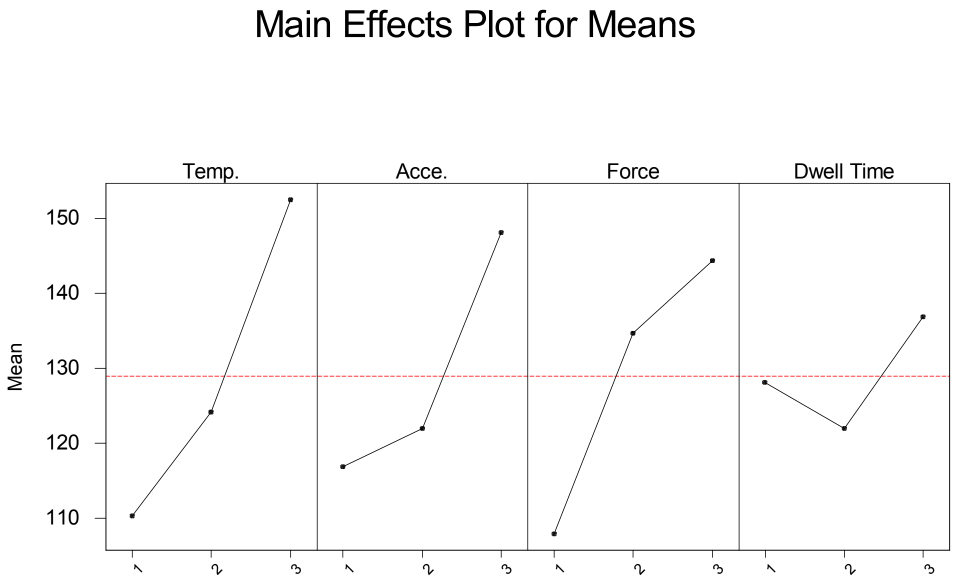


Figure 3.12 Main Effects Plot for Means

The response table for S/N (Signal to Noise) ratio and the main effect plots for S/N ratios are given in Table 3.5 and Figure 3.13. Two-step optimization, an important part of robust parameter design, involves first reducing variation and then adjusting the mean on target. Based on the two-step optimization, the optimal processing condition for void minimization is $A_1B_1C_1D_2$. In other words, the optimal combination is to set the dispensing stage temperature at level 1 (25°C, room temperature), the placement acceleration at level 1 (0.1g), the placement force at level 1 (1N), and the dwell time at level 2 (1.5s).

Table 3.5 Response Table for S/N

| Level | Dispensing stage temp. | Acceleration | Force | Dwell Time |
|---|---|---|---|---|
| 1 | -40.5321 | -41.0445 | -40.4531 | -41.6767 |
| 2 | -41.8956 | -41.7050 | -42.3948 | -41.6488 |
| 3 | -43.6114 | -43.2897 | -43.1913 | -42.7136 |
| Delta | 3.0793 | 2.2451 | 2.7381 | 1.0648 |
| Rank | 1 | 3 | 2 | 4 |

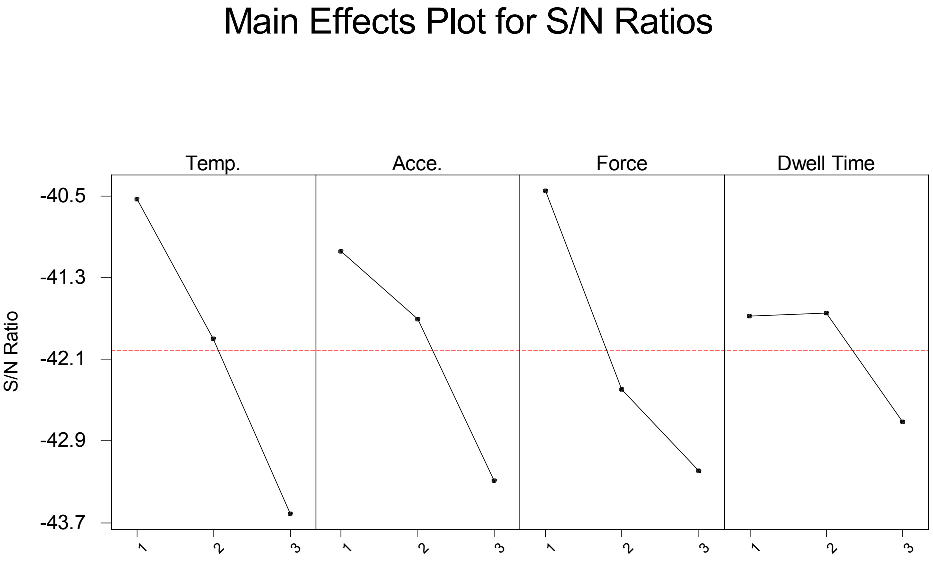


Figure 3.13 Main Effects Plot For S/N Ratios

After determining the optimal parameter combination, experiments were conducted to verify the best conditions. As shown in Figure 3.14, voiding was not totally eliminated, but it was significantly reduced.

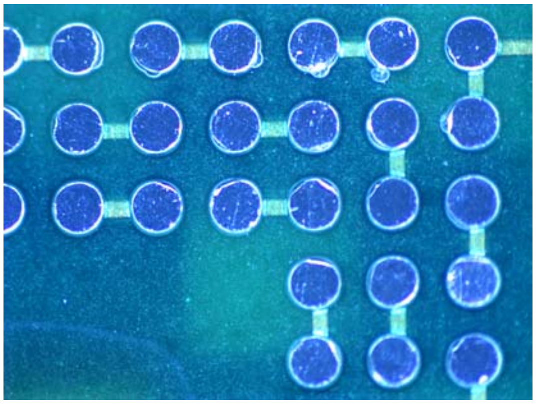


Figure 3.14 Flat Section of Fluxing Underfill Showing Reduced Voiding After Placement Optimization.

After reflow, the fluxing undefill is expected to be fully cured in a single reflow cycle. Differential scanning calorimetry (DSC) was used to evaluate the underfill cure with the lead-free ramp-to-peak profile. A DSC plot of an uncured sample was also made. As shown in Figure 3.15, there was no exotherm associated with the reflow cured sample, indicating that the fluxing underfill had a high degree of cure.

Self-centering with the fluxing underfill was also studied. CSPs that were intentionally placed offset by 50% in both the X and Y directions self-centered during reflow.

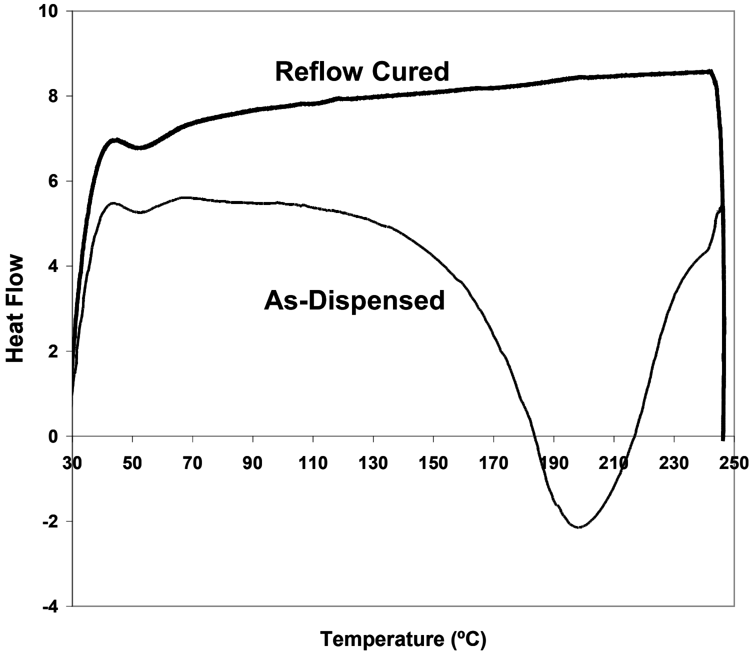


Figure 3.15 DSC Curves for Uncured and Reflow Cured Fluxing Underfill.

### 3.3.4 Corner Bond Underfill

The corner bond underfill process was described in detail in Chapter 2. The corner bond underfill was dispensed as four dots corresponding to the four corners of the CSP after solder paste print, but before CSP placement. The corner bond material cured during the reflow cycle. This is a simpler process compared to capillary or fluxing underfill.

Two different corner bond materials, one for each solder alloy, were required due to the different reflow profiles used. During reflow, the underfill cannot be allowed to cure before the alloy melts, to allow collapse. However, the underfill must cure during the final stages of the reflow profile. DSC was used to verify that the underfill for lead-free assembly cured during the ramp-to-peak reflow profile. Cross sections verified good collapse and solder wetting. The reflow profile for the eutectic Sn/Pb assembly had previously been verified [66].

Self-centering of the CSPs with corner bond underfill was studied. CSPs that were intentionally offset by 50% in either the X or the Y direction self-centered during reflow. However, a 50% offset in both the X and Y directions resulted in the corner solder ball contacting the dispensed underfill. As shown in Figure 3.16, this resulted in a deformed solder joint (lower left corner), although this CSP still self-centered. The alignment tolerance for solder balls contacting the dispensed underfill is a function of the CSP ball pattern design and the dispense volume.

If corner bonded CSPs are to be assembled on both sides of a board, the corner bond material on the first side assembled will be subjected to a second reflow cycle. To evaluate the effect of this, boards with corner bonded CSPs were inverted and passed thorough the reflow oven a second time. No CSPs were actually assembled on the second side, as this would have changed the mechanical structure of the assembly. During drop testing, this change in mechanical structure would be a second variable and would not allow direct observation of the effect due to the two reflow passes. CSPs assembled with no underfill were also subjected to a second, inverted, reflow cycle for comparison.

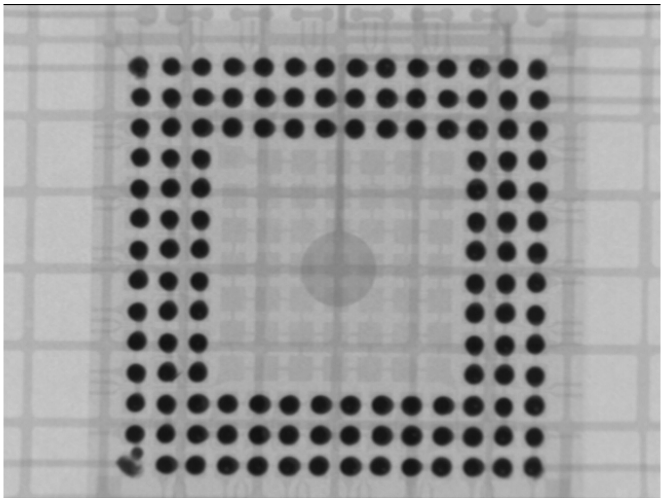


Figure 3.16 X-Ray Image After Reflow for CSP Intentionally Mis-placed by 50% in Both the X and Y Directions with Corner Bond Underfill.

### 3.4 Drop Test Results

For drop testing, a 31.8 gram weight was attached to one end of the board to accelerate failure and simulate product weight. The board was then dropped through a six foot long, three inch diameter tube onto a concrete floor. The daisy chain resistance of each CSP was measured and a 10% increase in resistance was recorded as a failure.

Before making a final reflow profile selection, four Sn/Ag/Cu boards without underfill were assembled with each reflow profile and dropped. The results are shown in Figure 3.17. Based on these results, the ramp-to-peak profile was chosen for all subsequent test vehicles built.

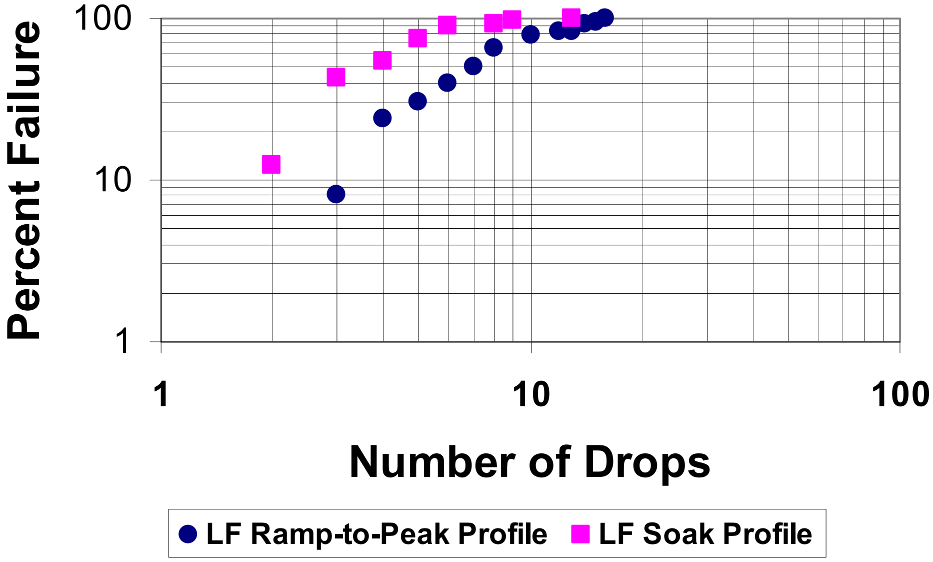


Figure 3.17 Drop Test Results for Non-Underfilled Sn/Ag/Cu CSPs with Two Reflow Profiles.

Figure 3.18 shows the drop test results for each solder alloy and underfill combination tested. With the exception of the Sn/Pb corner bond test vehicle, five boards (50 CSPs) were dropped for each test combination. Four Sn/Pb corner bond boards were dropped.

The earliest group to fail was the samples with no underfill. There was no significant difference between the Sn/Pb and the Sn/Ag/Cu CSPs. The second group to fail was the corner bonded CSPs with a 3x improvement over the no underfill samples. This is consistent with earlier results with Sn/Pb and corner bond underfill [66]. Again, there was no significant difference between Sn/Pb and Sn/Ag/Cu. The next group to fail was the capillary flow samples. For this group of samples, capillary underfill B performed better than capillary underfill A and Sn/Ag/Cu out performed Sn/Pb. The combination of Sn/Ag/Cu and capillary underfill B had only 2 CSPs failures out of 50 CSPs after 100 drops. The best drop test results were obtained with the Sn/Ag/Cu alloy and the fluxing underfill – No failures (0/50) after 150 drops. The presence of voids in the underfill did not degrade the drop test performance of the fluxing underfill.

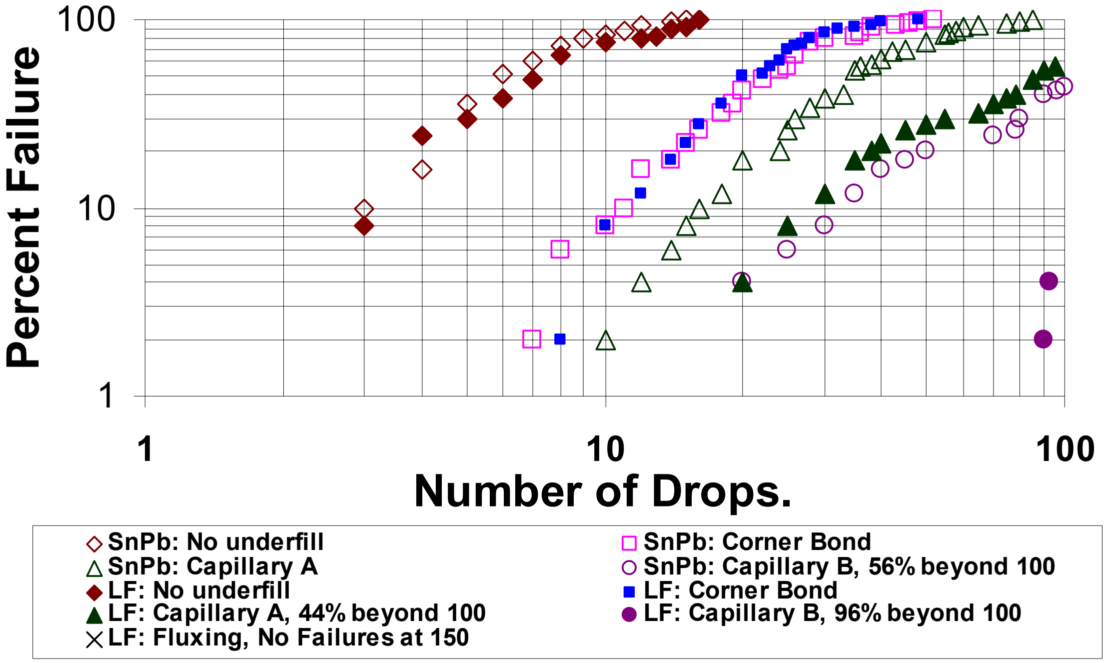


Figure 3.18 Drop Test Results for Sn/Pb and Sn/Ag/Cu Solders and Different Underfills.

Figure 3.19 shows the drop test results for the double reflow samples, where the board was inverted for the second reflow cycle with no underfill and with the corner bond underfill. There was some decrease in drop test performance of the corner bond samples with the second reflow cycle, as well as earlier failures in the non-underfilled samples with two reflow cycles.

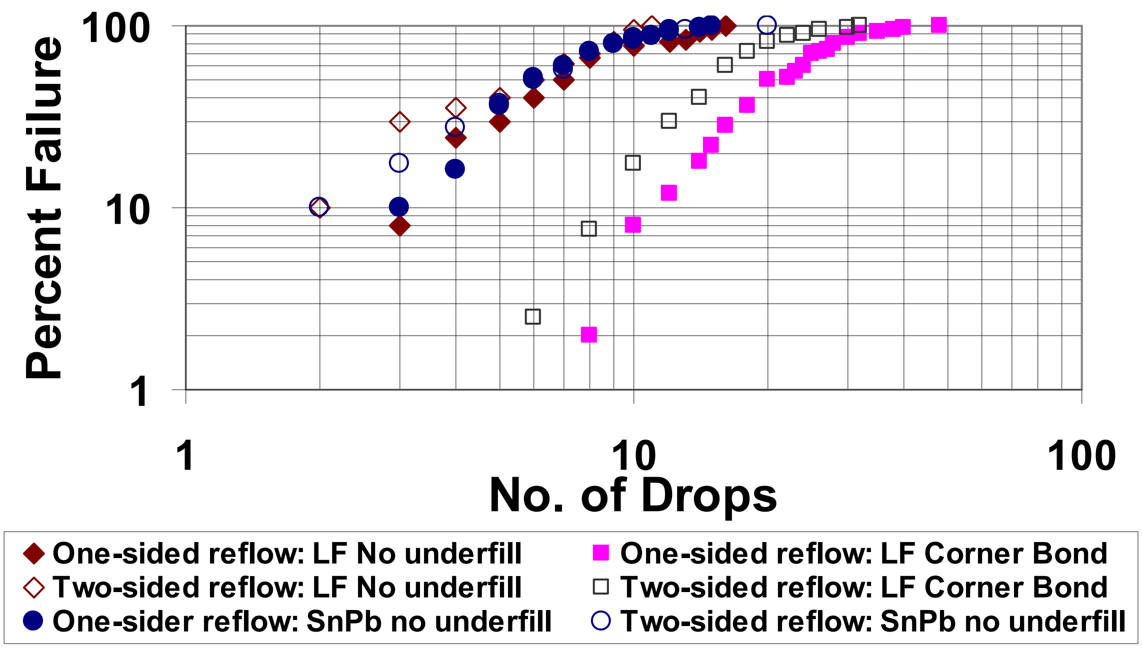


Figure 3.19 Drop Test Results for Single and Double Reflow Cycles.

Drop tests are typically performed on as-built samples. However, customers expect their portable products to survive being dropped even after some use time in the field. To begin to explore the effect of aging on drop test performance, Sn/Ag/Cu CSPs, with no underfill and with corner bond underfill was studied. Samples were aged at 125°C for 100 hours and 250 hours, and then drop tested. The results are shown in Figure 3.20. There was a significant decrease in drop test performance after 100 hours at 125°C. After 250 hours at 125°C, the drop test results for the corner bonded CSPs are approximately equal to the unaged, non-underfilled Sn/Ag/Cu samples. The decline in non-underfilled performance seems to stabilize after 100 hours.

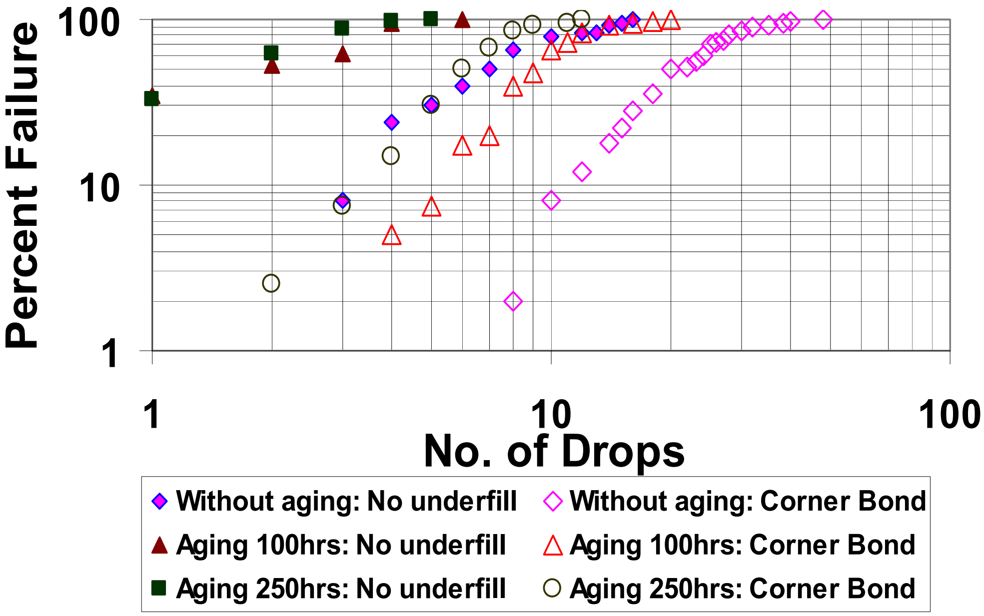


Figure 3.20 Drop Test Results for Sn/Ag/Cu Solder With No Underfill and With Corner Bond Underfill After 0, 100 and 250 Hours of Aging at 125°C Prior to Dropping.

Figure 3.21 compare the effect of thermal aging on drop reliability between Sn/Pb and Sn/Ag/Cu CSPs, the drop test reliability of lead-free CSP assemblies decreases more rapidly with high temperature aging compared to Sn/Pb CSPs.

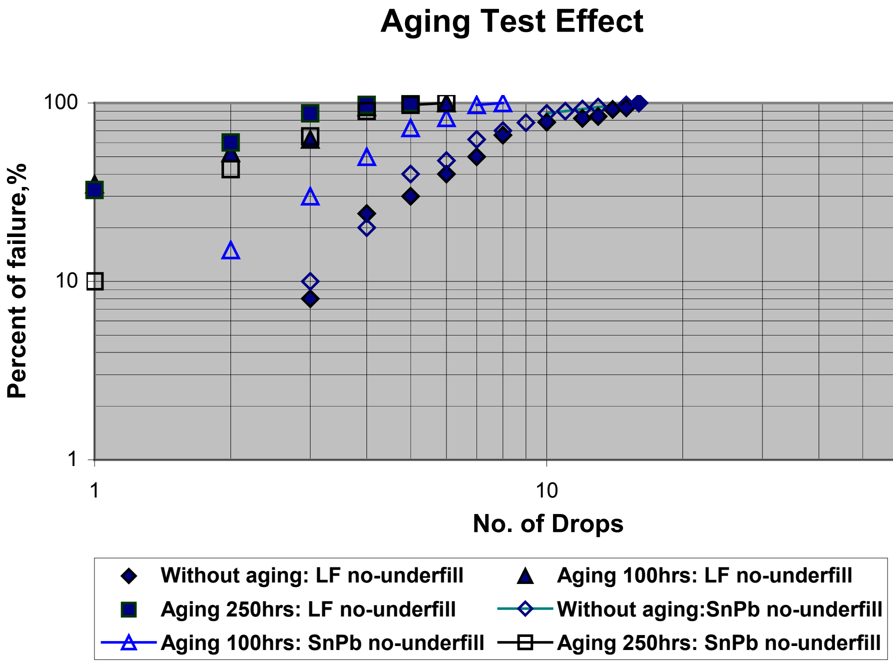


Figure 3.21 Drop Test Results for Sn/Pb and Sn/Ag/Cu Solder with No Underfill After 0, 100 and 250 Hours Aging at 125°C Prior to Dropping

### 3.5 Failure Analysis

Figures 3.22 and 3.23 show typical failures modes for the 'ramp-to-peak' and 'soak' lead-free profiles, respectively. The predominant failure mode for the ramp-to-peak profile is in the solder near either the package or substrate interface. With the longer soak profile, the typical failure mode was fracture of the laminate under the pad with corresponding fracture of the copper trace. The drop test results for the soak profile were not quite as good as the results for the ramp-to-peak reflow profile (Figure 3.17), corresponding to the change in failure mode.

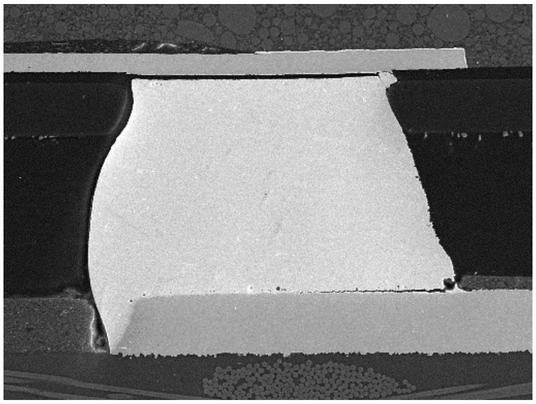


Figure 3.22 Cross Section of a Typical Drop Test Failure of a Sn/Ag/Cu Solder Joint (no Underfill) Reflowed With the Ramp-to-Peak Profile.

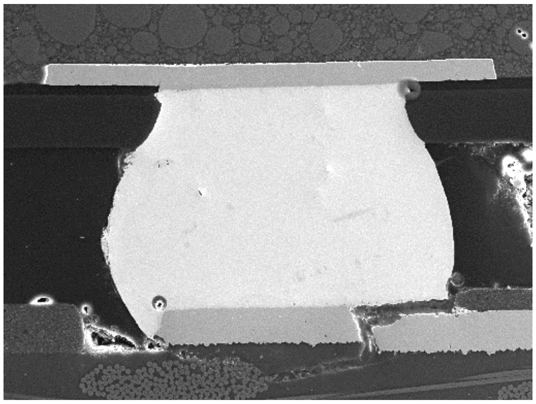


Figure 3.23 Cross Section of a Typical Drop Test Failure of a Sn/Ag/Cu Solder Joint (no Underfill) Reflowed With the Soak Profile.

The corner bond underfilled Sn/Ag/Cu and Sn/Pb CSPs both failed by cracking of the corner bond adhesive and failure of the solder joint at the package or substrate interface. This is similar to the results previously reported for corner bonded Sn/Pb CSPs [66].

Figures 3.24 and 3.25 show cross sections of Sn/Ag/Cu CSP failures with capillary underfills A and B, respectively. Capillary underfill A has a higher modulus, strongly coupling the CSP to the PCB. Thus, the PCB is rigidized at the CSP locations. Flexing of the PCB during drop testing results in fracture of the underfill fillet. This crack propagates into the outer row of solder balls and then through the copper trace into the laminate. This failure mode has been reported previously for Sn/Pb CSPs [66].

The modulus of capillary underfill B is significantly lower, allowing more relative movement between the PCB and the CSP. This places more stress on the solder joint, leading to failure in the solder. From the drop test results, the lower modulus underfill is better for both Sn/Pb and Sn/Ag/Cu CSPs.

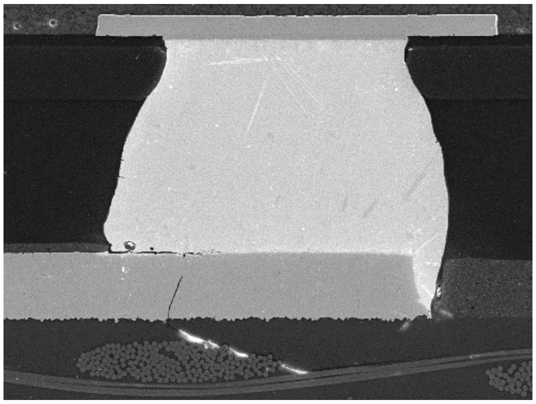


Figure 3.24 Cross Section of Sn/Ag/Cu Failure with Capillary Underfill A.

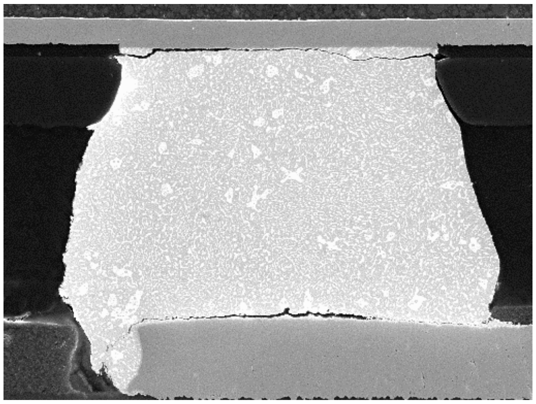


Figure 3.25 Cross Section of Sn/Ag/Cu Failure with Capillary Underfill B.

Figure 3.26 shows a cross section of Sn/Ag/Cu CSP failure (no underfill, two reflow cycles). The two reflow cycles were both ramp-to-peak. The exposure of the PCB to two lead-free reflow cycles resulted in a change in failure mode compared to that shown in Figure 3.22. This is consistent with the failure mode resulting from the longer soak profile.

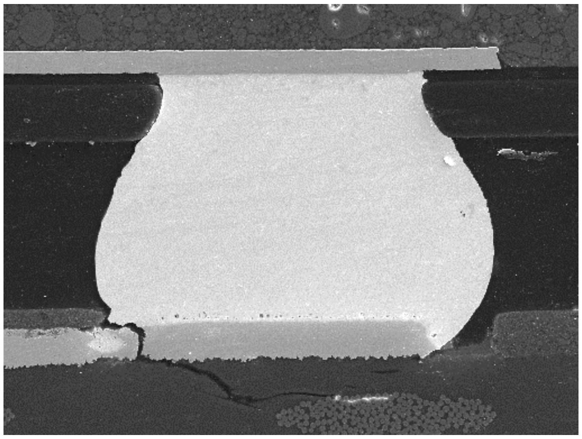


Figure 3.26 Cross Section of Sn/Ag/Cu CSP (No-Underfill) Failure Assembled With Two Reflow Cycles.

Figure 3.27 shows the failure mode for the Sn/Ag/Cu CSP (no underfill) when aged at 125°C for 250 hours before dropping. While the drop test performance was significantly degraded with aging, there was no change in the failure mode (compare this to Figure 3.16). This indicates the degradation mechanism is controlled by changes in the solder and/or intermetallic with aging.

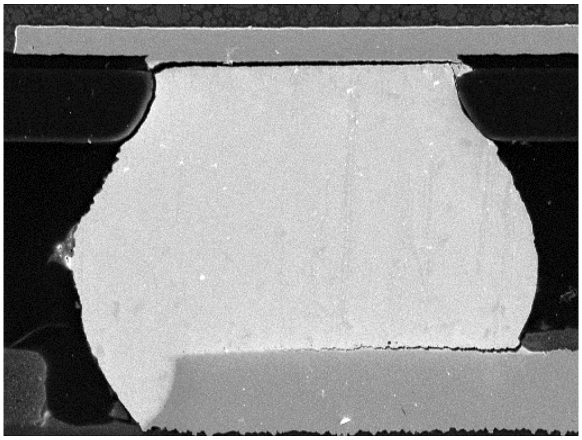


Figure 3.27 Cross Section of Sn/Ag/Cu CSP Failure After 250 Hours at 125°C Storage Prior to Drop Testing.

### 3.6 Summary

Three underfill options, all of which are compatible with lead-free assembly, have been evaluated: capillary underfill, fluxing underfill and corner bond underfill. CSPs with eutectic Sn/Pb solder were used as control samples.

The reflow profile affected the drop test performance and failure mode with the Sn/Ag/Cu CSPs. The longer soak profile resulted in poorer drop test performance, with the failure occurring in the laminate. The shorter, ramp-to-peak profile was used for all subsequent test vehicle builds.

Without underfill, lead-free and Sn/Pb eutectic drop results were comparable. With capillary flow underfill, the drop test results were significantly better with lead-free solder assembly than with Sn/Pb eutectic. The lower modulus capillary underfill performed better with both Sn/Pb and Sn/Ag/Cu CSPs in the drop test.

The fluxing underfill with lead-free solder yielded the best drop test results. There were no failures after 150 drops. The drop test results with corner bond were intermediate between no underfill and capillary underfill and were similar for both lead-free and Sn/Pb eutectic solder assembly. There was some degradation in the drop test results after 100 and 250 hours of storage at 125°C prior to the drop test.

The use of underfill improved the drop test performance of the CSPs evaluated in this series of experiments. The different underfill types provide assembly process options, which must be weighed against the difference in drop test performance.

# CHAPTER 4

# EFFECT OF SURFACE FINISH, REFLOW PROFILE AND THERMAL AGING ON DROP RELIABILITY OF LEAD-FREE CSPS

## 4.1 Introduction

Single and multi-die CSPs are increasingly used in portable products and are migrating to other product segments due to their small size and availability. Consumers expect portable products to survive being dropped repeatedly, and drop testing is now common in the reliability evaluation of portable product designs. In some cases underfill is used to improve the drop test performance [63-66], while in others underfill is not used, lowering manufacturing costs and facilitating rework. The switch to lead-free assembly has required the electronics industry to generate new reliability data.

Most drop test reliability data reported for CSPs are for the as-built condition. However, the mechanical shock reliability over the life of the product is equally important to the customer. As previously discussed in Chapter 3, the drop test reliability of lead-free CSP assemblies decreases more rapidly with high temperature aging compared to Sn/Pb CSPs. Chui, et al. has reported similar results and attributed the failures to voids forming at the copper-copper intermetallic interface during accelerated aging [69]. The objective of this work was to provide a systematic study of surface finish (Immersion Sn and Immersion Ag), reflow profile (cool down rate) and thermal aging on the drop test reliability of CSP assemblies, and to further characterize this decrease in drop test reliability with elevated temperature aging.

## 4.2 Test Vehicle

The test vehicle, shown in Figure 4.1, was a four-layer test board with ten CSP attachment sites on one side and four BGA sites on the other. In these experiments, only the CSP side of the board was assembled. Standard technology (FR4) was used for board fabrication, with no build-up or HDI layers. The board was 2.95" by 7.24" by 0.040" thick. The pads were 0.012” in diameter, non-solder mask defined.

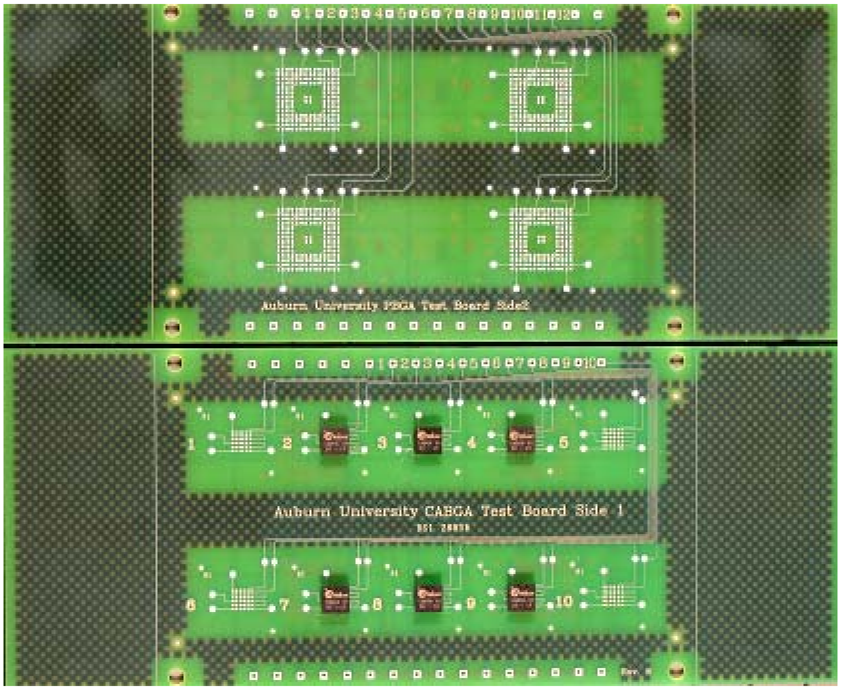


Figure 4.1 Test Vehicle

Immersion Ag and immersion Sn finishes were used as the board surface finishes. The Sn finish provides an initial Cu-Sn intermetallic layer, while the Ag finish allows the formation of the initial Cu-Sn intermetallic during the reflow cycle. Figure 4.2 shows the cross sections of the as received Sn finished pads. There is an initial Cu-Sn intermetallic layer formed on the immersion Sn finished pads. One objective of this experiment was to determine if the formation of this initial Cu-Sn intermetallic prior to solder assembly had any impact on drop test reliability.

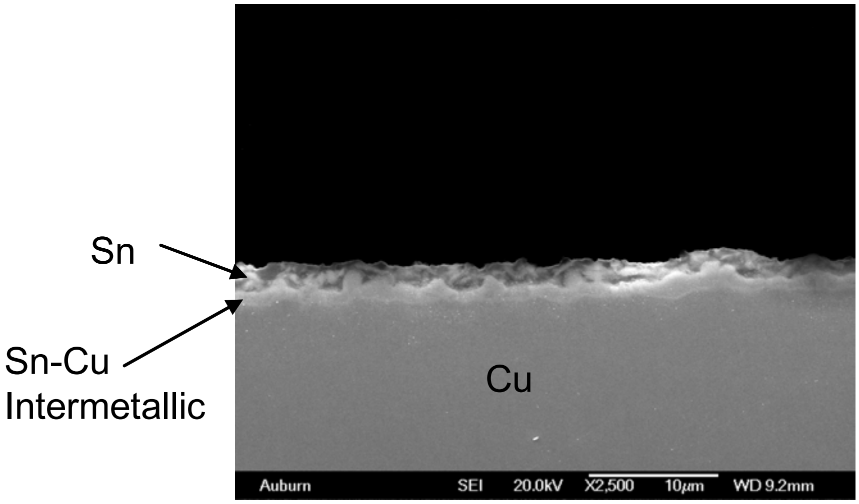


Figure 4.2 Cross Section of As-Received Sn Finish.

The CSP was a 6mm daisy chain part manufactured by Amkor and purchased from Practical Components (A-CABGA36-.8mm-6mm-DC-LF). The part had a full area array of 36 solder balls on 0.8mm pitch. The solder balls were 96.5Sn/4.0Ag/0.5Cu and 0.46mm in diameter. The pads on the CSP were solder mask defined and had a Ni/Au finish.

### 4.3 Assembly Process

Table 4.1 lists the factors and levels investigated in this design of experiment (DOE), the corresponding full factorial DOE matrix is shown in Table 4.2. Three boards with 10 CSPs each were built for each test run.

Table 4.1 Factors and levels investigated in this DOE

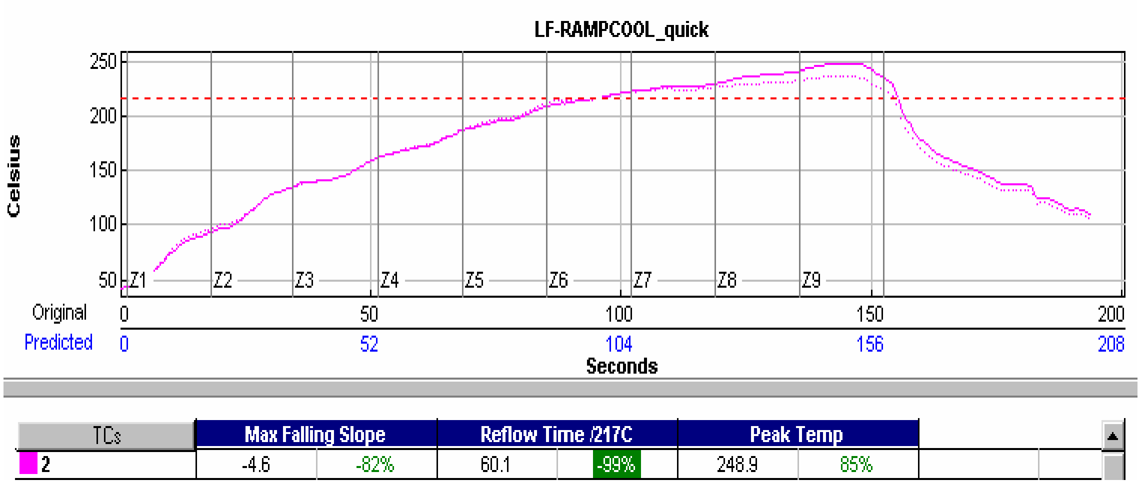
| Factors | Level 1 | Level 2 | Level 3 | Level 4 |
|---|---|---|---|---|
| A: Surface Finish | Immersion Sn | Immersion Ag | | |
| B: Reflow Profile | Medium Cooling rate | Quick cooling rate | | |
| C: Aging Time, (hrs) | 0 (As-built) | 50 | 240 | 480 |

Table 4.2 Full Factorial DOE for $2^2 1^4$

| Run No | A | B | C | Run No | A | B | C |
|---|---|---|---|---|---|---|---|
| 1 | 2 | 1 | 3 | 9 | 2 | 2 | 4 |
| 2 | 1 | 2 | 1 | 10 | 2 | 2 | 2 |
| 3 | 2 | 1 | 1 | 11 | 2 | 1 | 4 |
| 4 | 1 | 2 | 4 | 12 | 1 | 1 | 1 |
| 5 | 2 | 2 | 1 | 13 | 1 | 1 | 4 |
| 6 | 2 | 2 | 3 | 14 | 1 | 2 | 2 |
| 7 | 1 | 1 | 3 | 15 | 1 | 2 | 3 |
| 8 | 2 | 1 | 2 | 16 | 1 | 1 | 2 |

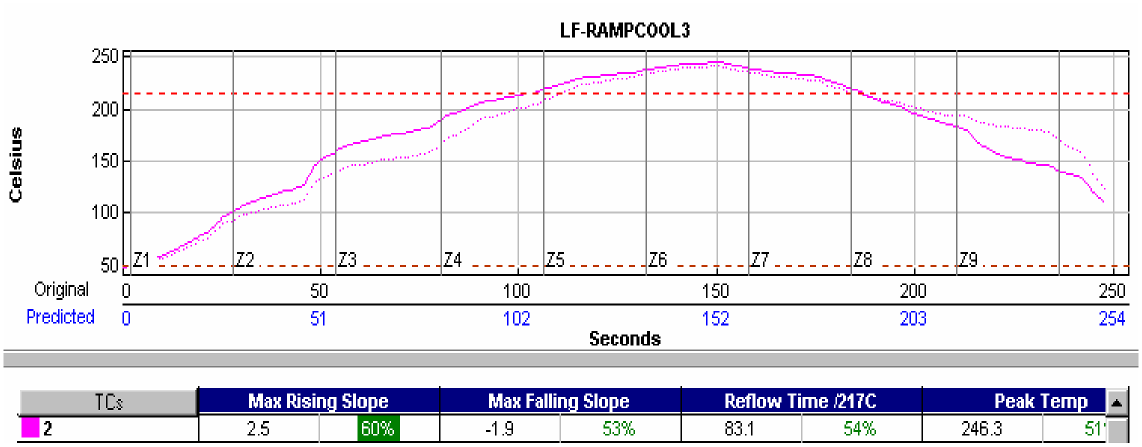
The assemblies were built on a high volume, automated SMT line at Auburn University. Kester EM907 no clean lead-free solder paste SAC305 (96.5Sn3Ag0.5Cu) solder paste was printed with an MPM AP25 stencil printer using a 4mil thick, laser cut, electro-polished, nickel plated stencil. Assembly was performed with ACM Micro pick and placement system and Heller 1800 reflow furnace.

Two reflow profiles were used, as shown in Figures 4.3 and 4.4. The slower cool down profile produced a coarse microstructure compared to the quick cool down profile shown in Figure 4.5. The objective of this variable was to study the effect of solder microstructure and grain size on the drop test performance.



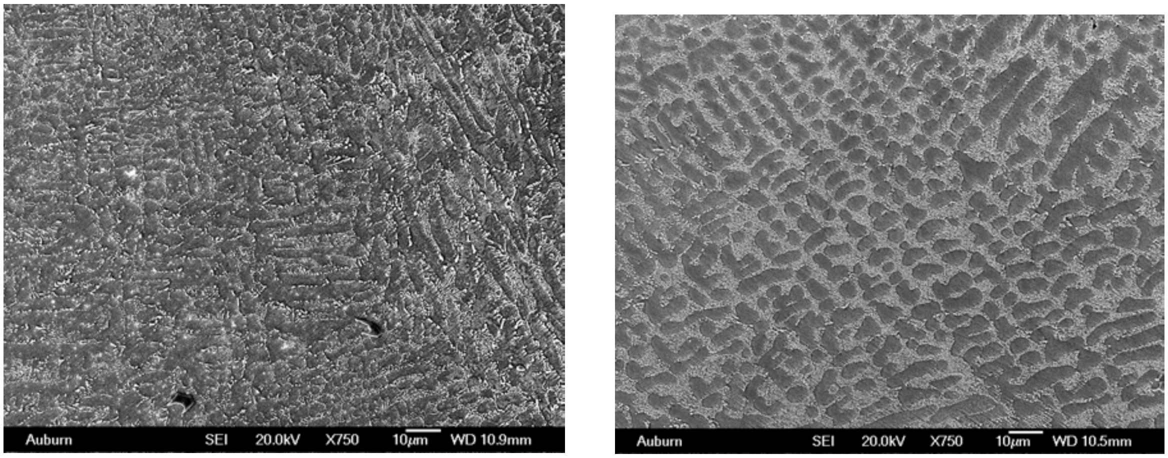
| TCs | Max Falling Slope | | Reflow Time /217C | | Peak Temp | | | |
|---|---|---|---|---|---|---|---|---|
| 🟪 2 | -4.6 | -82% | 60.1 | -99% | 248.9 | 85% | | |

Figure 4.3. ‘Quick’ Cool Down Reflow Profile.



| TCs | Max Rising Slope | | Max Falling Slope | | Reflow Time /217C | | Peak Temp | |
|---|---|---|---|---|---|---|---|---|
| 🟪 2 | 2.5 | 60% | -1.9 | 53% | 83.1 | 54% | 246.3 | 51' |

Figure 4.4 ‘Moderate’ Cool Down Reflow Profile.

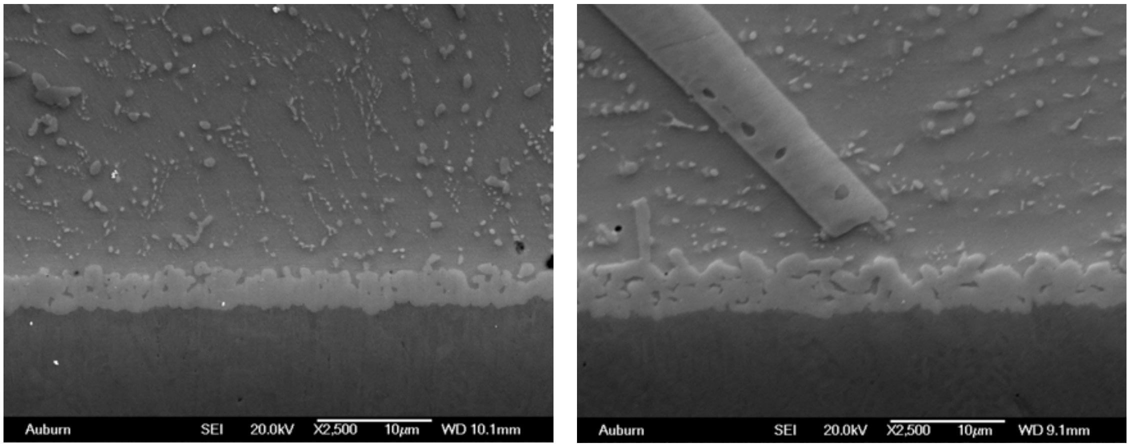


(a) Quick Cool Down Profile

(b) Moderate Cool Down Profile

Figure 4.5 Scanning Electron Micrographs for the “Quick” and “Moderate” Cool Down Profiles for Solder Joints on the Sn Surface Finish.

Figure 4.6 shows the intermetallic structure for the Ag and Sn finishes as-built (Moderate Profile). There was no significant difference in the intermetallic structures between the two reflow profiles. The intermetallic layer was slightly thicker for the Sn finish since there was an initial intermetallic layer. There were also occasional small voids at the intermetallic-to-solder interface with both surface finishes. There was no indication of voids at the Cu-to-intermetallic interface.



(a) Ag (b) Sn

Figure 4.6 As-built Intermetallic Structure for Ag and Sn Finishes, Moderate Reflow Profile.

Parts were dropped as-built and after 50, 240 and 480 hours of storage at 125°C. For drop testing, weights totaling 23.0 grams were attached to both faces of one end of the board to accelerate failure and simulate product weight. The board was then dropped through a six-foot long, three inch diameter tube onto a concrete floor with the weighted end up. The daisy chain resistance of each CSP was measured and a 10% increase in resistance was recorded as a failure.

## 4.4 Drop Test Results

Wiebull plots of the drop test data were generated using Minitab 13.0. An example is shown in Figure 4.7.

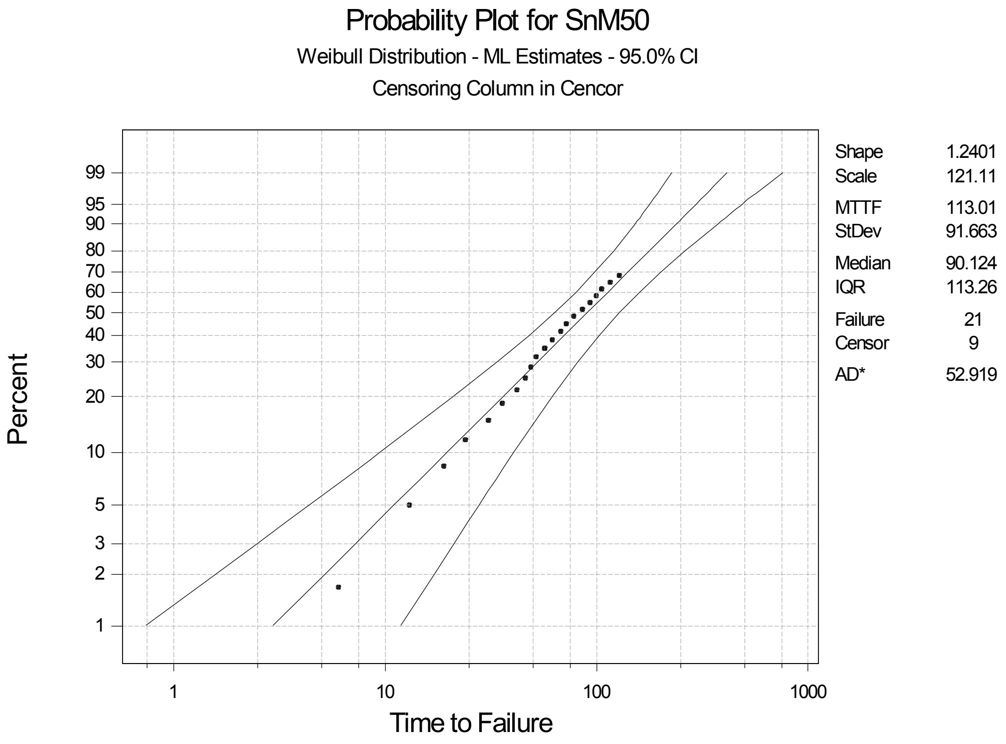


Figure 4.7 Weibull Plot for Sn Surface Finish, Moderate Cooling, Aging 50hrs.

From these plots, the mean number of drops to failure (MDTF) as a function of surface finish, reflow profile and aging at 125$^{o}$C were plotted in Figure 4.8. In the legend, "Q" refers to the quick cool down profile and 'M' refers to the moderate cool down profile. The Ag finish only slightly out performed the Sn finish, and there was no difference due to reflow profile. The data demonstrates a steady decrease in MDTF as a function of aging at 125$^{o}$C.

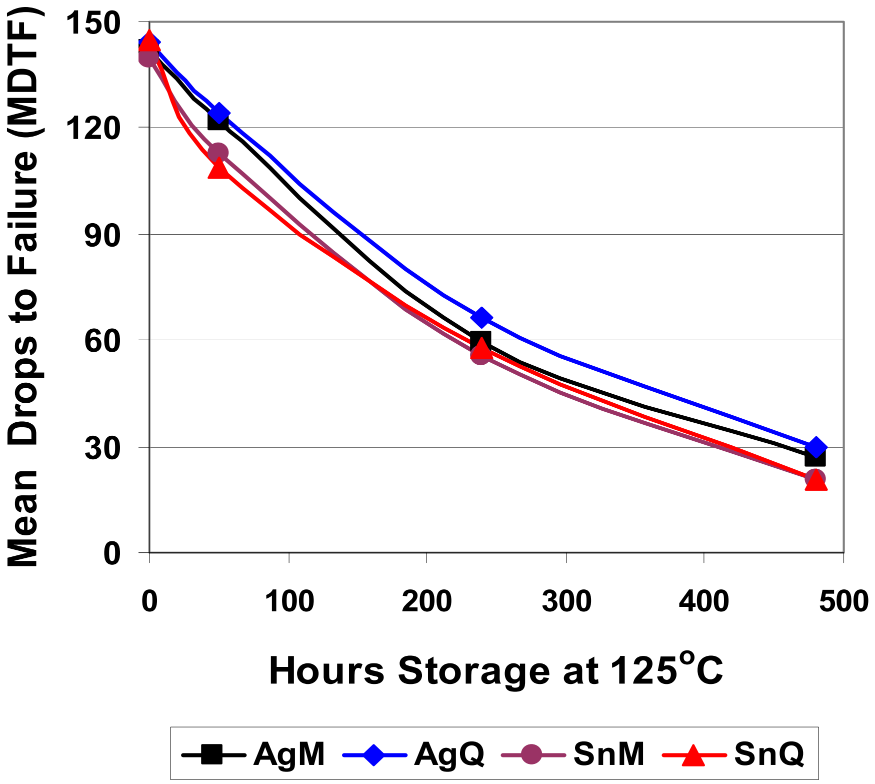


Figure 4.8 Mean Number of Drops to Failure as a Function of Aging at 125$^{o}$C, Surface Finish and Reflow Profile.

## 4.5 Kirkendall Voids Formation with Aging Time

Figure 4.9 shows a schematic representation depicting the formation of Kirkendall voids during the reaction of Cu with Sn to form intermetallic compounds [98]. In a reactive system such as Cu-Sn, the reactants are initially separated by an interface, which is on the order of a few atomic distances, as shown in Figure 4.9. When the reaction is initiated, the reactants become separated by a layer of reaction product. Further reaction requires that reactants diffuse through the reaction product, $Cu_3Sn$ in this example. The initial reaction kinetics are interface-controlled and the growth of the layer is linear with time, as shown in Figure 4.10 [99]. The interface reaction is one in which a Cu atom, for example, jumps from the Cu to the $Cu_3Sn$ crystal lattice structure. When the reaction product reaches a critical crossover thickness, on the order of 100nm, the kinetics become diffusion-controlled and growth proceeds as time to the one-half power. The crossover thickness is equal to the parabolic rate constant divided by the linear rate constant. In this example, further growth of $Cu_3Sn$ proceeds as the Cu diffuses through the $Cu_3Sn$ to react with Sn at the $Cu_3Sn$-Solder interface. At the same time, Sn diffuses in the opposite direction through $Cu_3Sn$ to react with Cu at the Cu-$Cu_3Sn$ interface. However, the rates at which Cu and Sn diffuse through $Cu_3Sn$ are not equal. For this system, Cu diffuses more quickly than Sn and the result is that atomic-size vacancies are generated in the Cu to preserve the mass balance. As the reaction proceeds, the vacancy concentration increases until super-saturation occurs, resulting in nucleation and the growth of voids.

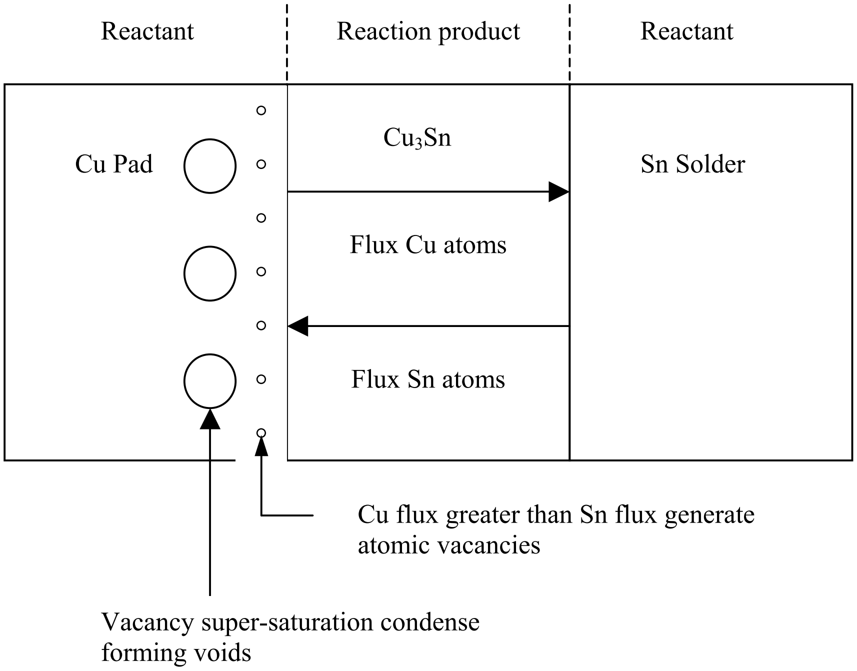


Figure 4.9 Schematic Representation Depicting the Formation of Kirkendall Voids During the Reaction of Cu with Sn to Form Intermetallic Compounds.

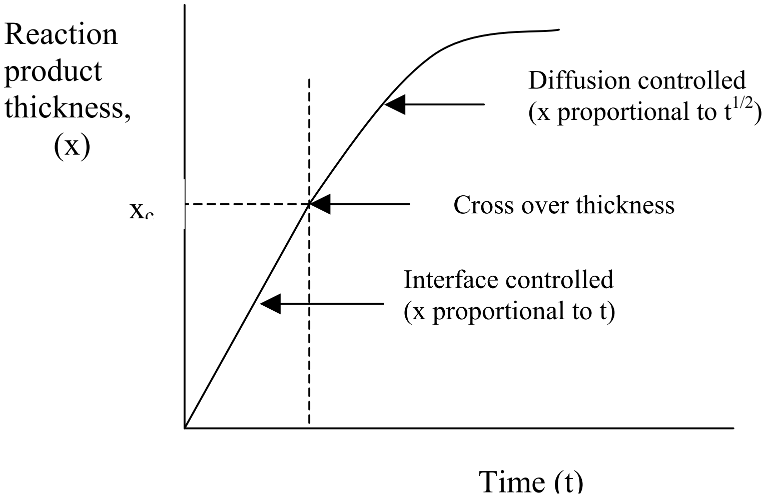
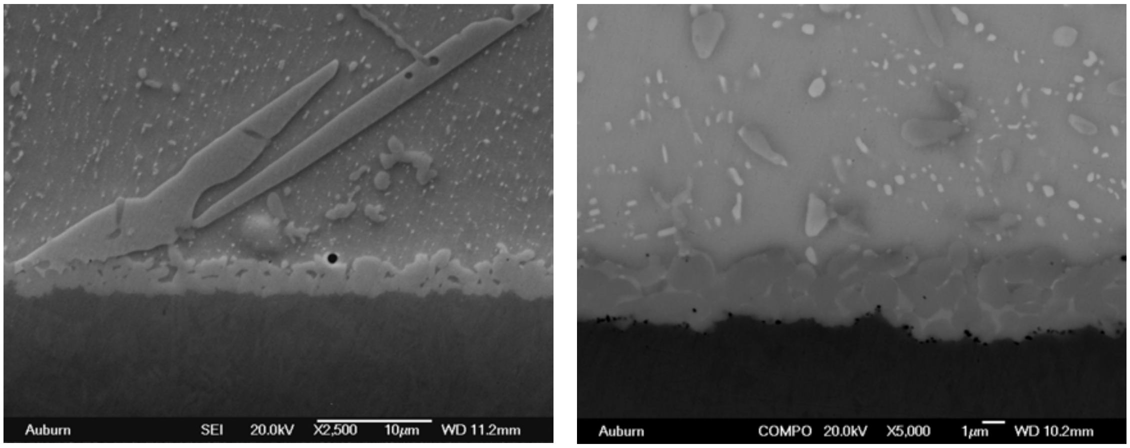
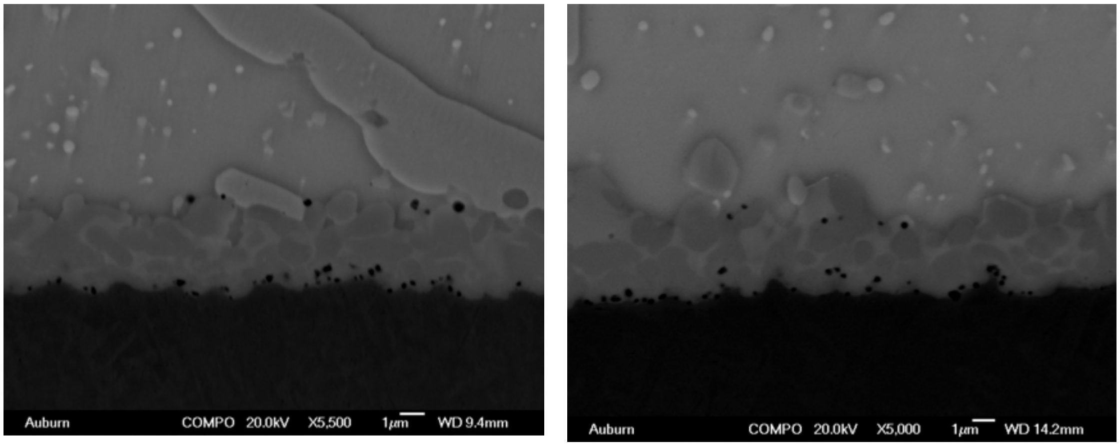


Figure 4.10 Graphic Representation of Change in Reaction Kinetics with Reaction Product Thickness.

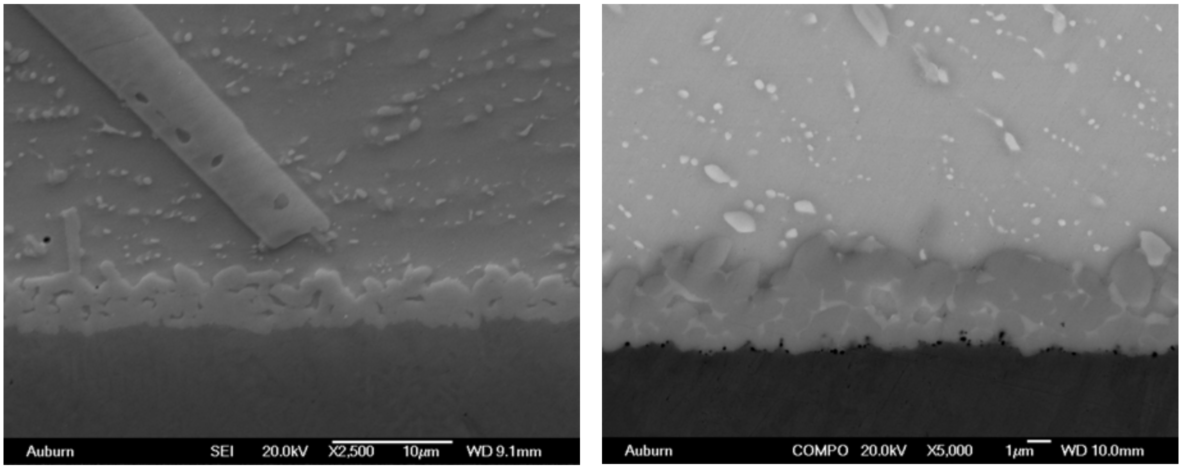


(a) Ag as-received (b) Ag aging 50 hrs

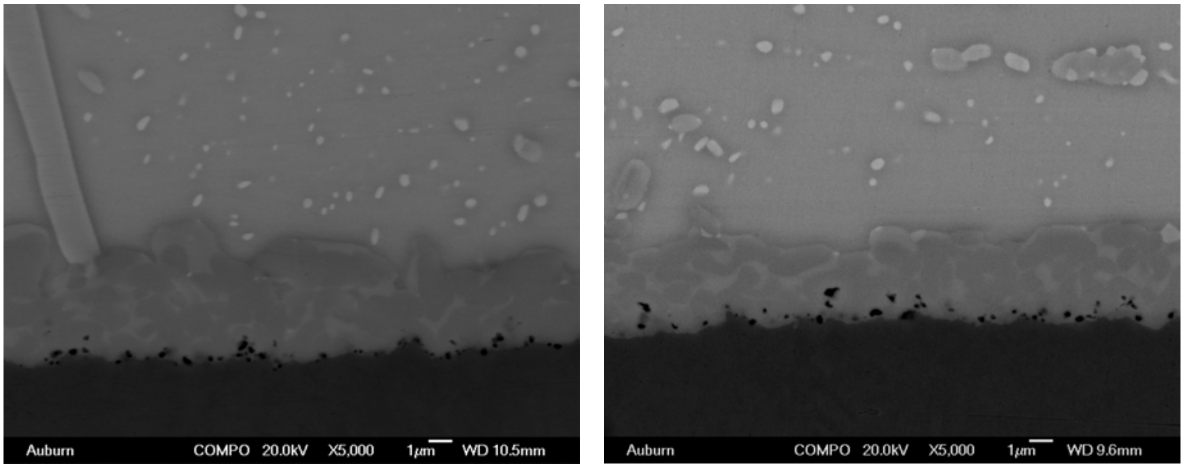


(c) Ag aging 240 hrs (d) Ag aging 480 hrs

Figure 4.11 Kirkendall Void Formation and Increasing as Aging Time Increases at 125°C, Ag Finish, Quick Profile.



(a) Sn as-received (b) Sn aging 50hrs



(c ) Sn aging 240hrs (d) Sn aging 480hrs

Figure 4.12 Kirkendall Void Formation and Increasing as Aging Time Increases at 125$^o$C, Sn Finish, Quick Profile.

Figures 4.11 and 4.12 show the formation of Kirkendall voids and their increase as aging time increases at 125$^{o}$C for the Ag finish and the Sn finish, both quick profile, respectively. There was no difference in the void formation between finishes or reflow profiles. The voids are not all at the exact interface between Cu and Cu-Sn intermetallic (IMC); rather most of them are inside the Cu-Sn IMC phase. This observation is consistent with that reported by Yang and Messle [71] and Mei et al [73], but different from that found by Chiu et al [69], where most voids were located and aligned at the $Cu_3Sn$ and Cu interface. The aligned voids provide an easier path than distributed voids for crack extension.

In Chiu et al's paper [69], voids at the interface reached 70% of the joint interface area after 20 days at 125C. The voided area in this study under the same aging conditions composed less than 40% of solder joint interface, which is consistent with Mei et al's study [73].

### 4.6 Failure Analysis

Failure analysis was preformed on the drop tested CSPs. Two failure modes were identified in the as-built samples: failure in the Cu-Sn intermetallic (substrate side), and fracture of the Cu trace. Crack examples are shown in Figures 4.13-4.16. Cracks that had not completely propagated through the joint causing failure were selected for publication, because they better illustrate the crack propagation paths. Fracture in the intermetallic layer during a drop test is expected, as the intermetallic layer is the most brittle part of the structure.

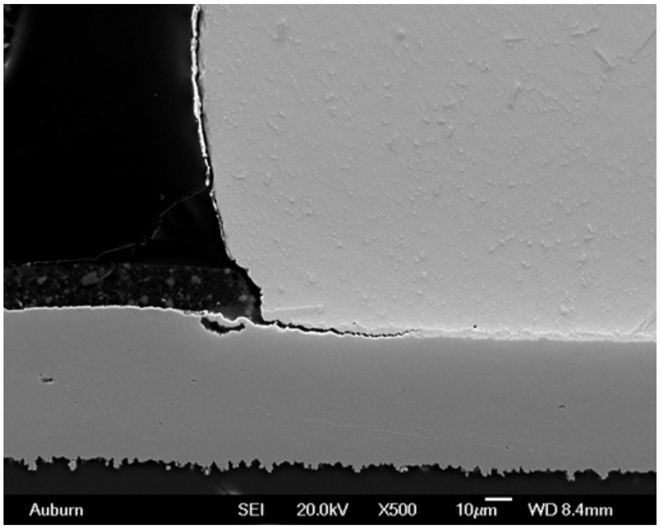


Figure 4.13 Typical Crack Propagating Through the Cu-Sn Intermetallic (No Aging, Sn Finish, Quick Profile

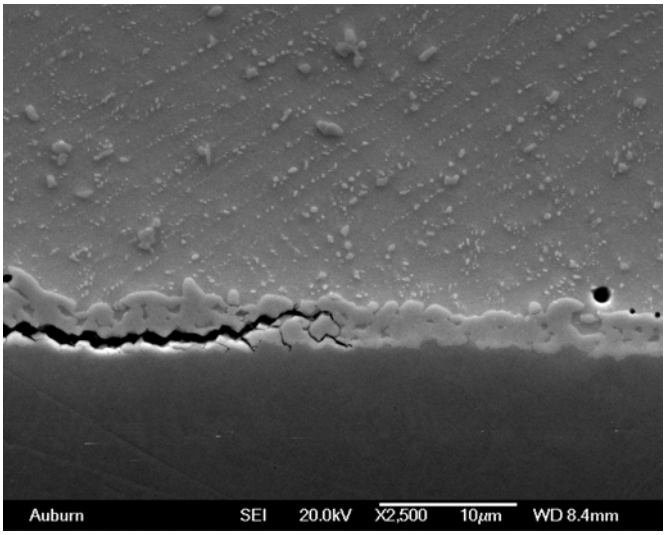


Figure 4.14 Close-up of Crack in Figure 4.13

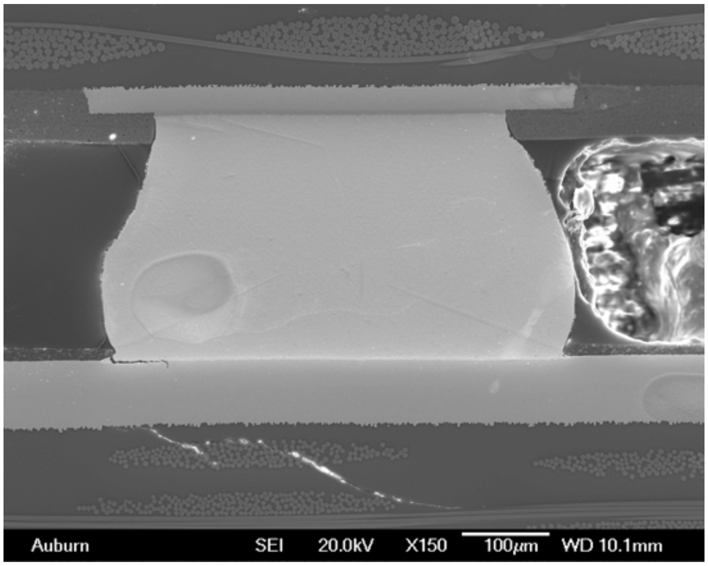


Figure 4.15 Typical Crack Propagating Through the Cu-Sn Intermetallic, then Turning into Cu (No Aging, Ag Finish, Moderate Profile).

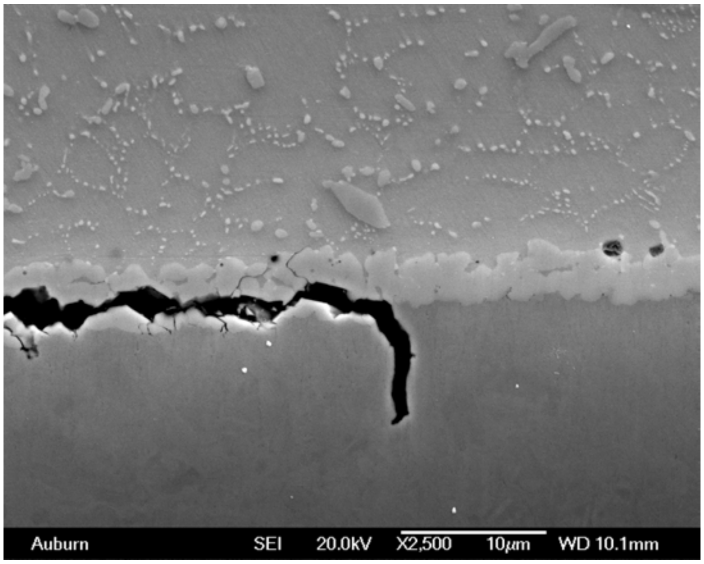


Figure 4.16. Close-up of Crack in Figure 4.15.

After 50 hours of aging at 125°C, voids are present. However, the voids are not in the crack path, as shown in Figures 4.17 and 4.18. In some cross sections, the voids appear to terminate one branch of the propagating crack. Thus, formation of the voids cannot explain the initial decrease in drop test performance with aging at 125°C.

After 240 hours of 125°C aging, the number of voids increased, but the crack path remained in the intermetallic layer and did not travel from void-to-void (Figure 4.19). The cross sections after 480 hours at 125°C were similar with an increasing number of voids (Figure 4.20). After aging, failures due to crack propagation through the Cu-Sn intermetallic, turning into the Cu layer were still observed (Figure 4.21). There were also a very few failures after aging due to fracture of the Ni-Sn intermetallic on the CSP side of the solder joint (Figure 4.22).

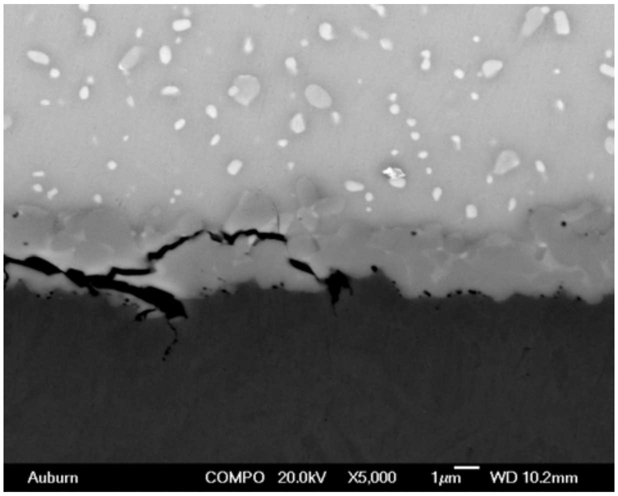


Figure 4.17 Example of Crack Propagation With the Ag Finish, Quick Reflow Profile after 50 hours at 125°C.

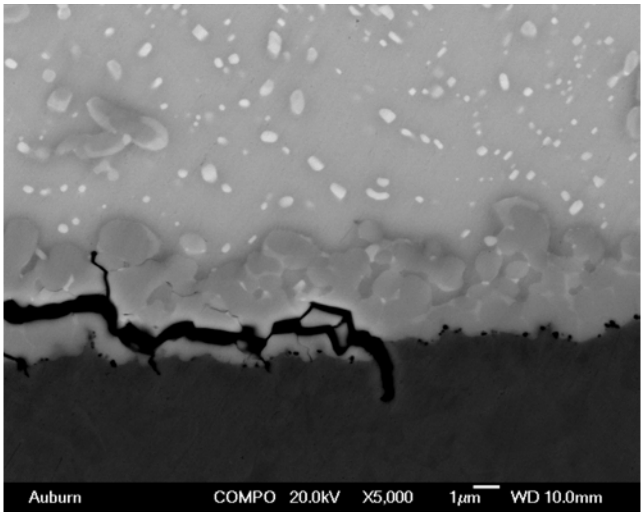


Figure 4.18 Example of Crack Propagation With the Sn Finish, Quick Reflow Profile after 50 hours at 125$^{o}$C.

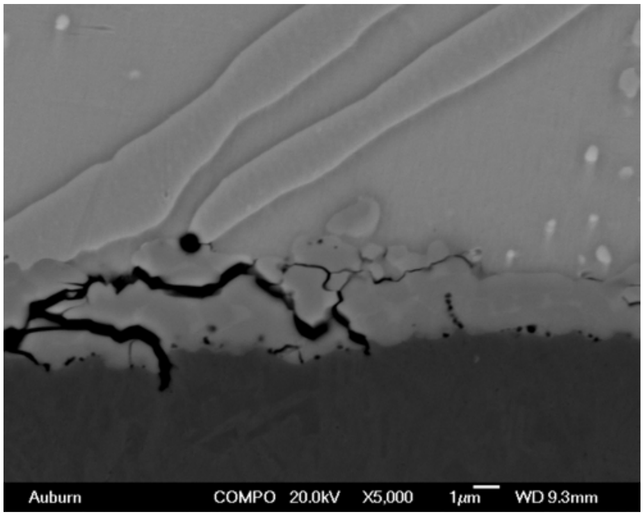


Figure 4.19 Example of Crack Propagation in the Intermetallic Layer With the Ag Finish, Quick Reflow Profile after 240 hours at 125$^{o}$C.

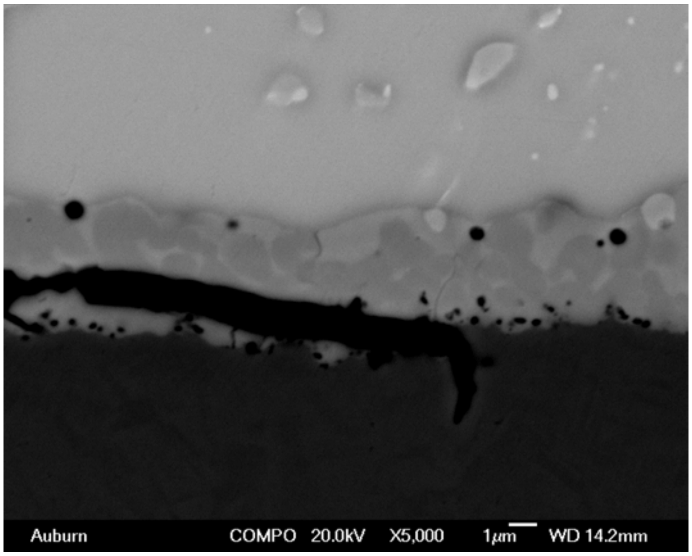


Figure 4.20 Example of Crack Propagation in the Intermetallic Layer With the Ag Finish, Quick Reflow Profile after 480 hours at 125$^{o}$C.

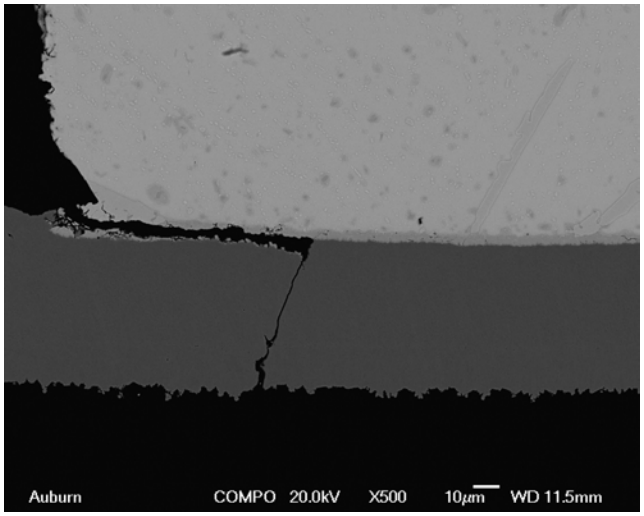


Figure 4.21 Example of Crack Propagation in the Intermetallic Layer Turning into the Cu With the Ag Finish, Moderate Reflow Profile after 480 hours at 125$^{o}$C.

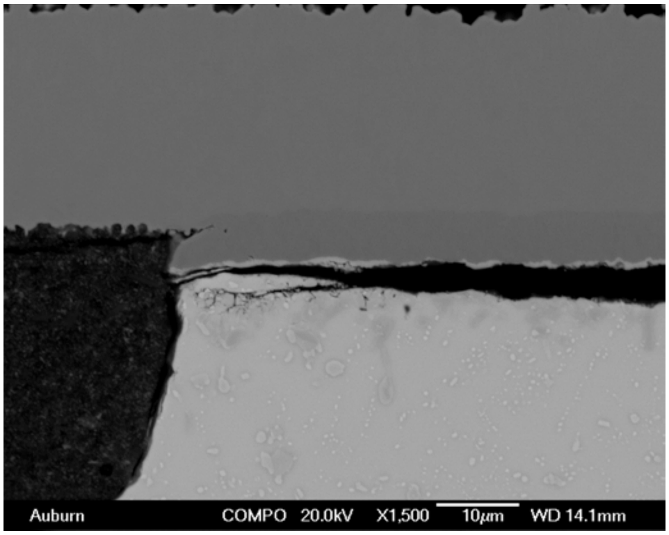


Figure 4.22 Example of Crack Propagation in the Ni-Sn Intermetallic Layer on the CSP Side of the Solder Joint With the Ag Finish, Quick Reflow Profile after 480 hours at 125$^{o}$C.

### 4.7 Summary

As previously reported, the mean number of drops to failure (MDTF) for lead-free CSP assemblies decreases with aging time at 125$^{o}$C. The results obtained in this study show that surface finish and reflow profile have little or no impact on this phenomenon.

Kirkendall voiding does occur with aging at 125$^{o}$C due to the more rapid diffusion of Cu into Sn, than Sn into Cu. The voids are not all at the exact interface between the Cu and Cu-Sn intermetallic (IMC); rather most of them are inside the Cn-Sn IMC phase. Through 480 hours of aging at 125$^{o}$C, the crack propagation path does not travel between voids. In fact, the voids appear in some cases to terminate the propagation of cracks. Thus, the decrease in MDTF must be related to changes in the mechanical properties of the intermetallic layer. Further analysis is necessary to explore this conclusion.

# CHAPTER 5

# PCB DESIGN AND ASSEMBLY PROCESS DEVELOPMENT OF 01005 COMPONENTS WITH LEAD-FREE SOLDER

## 5.1 Introduction

The continuing demand for smaller, lighter multifunctional portable electronic products has driven the use of miniature components. To satisfy this demand, 01005 chip components are now commercially available. However the incorporation of such tiny components into new products presents some novel design and assembly process issues. In this study, a test vehicle was designed to investigate the effect of PCB pad design on assembly yield. The process capability of 01005 test board manufacturing was evaluated. A Design of Experiment (DOE) was used to optimize solder paste printing based on 3D solder paste inspection. Lead-free solder was used for all assembly trials. Several tests were performed to explore the influences of process parameters on placement accuracy and reflow defects. Based on the analysis of experimental results and post-reflow inspection for assembly defects, recommendations for PCB design and assembly processes are made.

Due to the desire to make electronic products smaller and lighter, miniaturization and reducing spacing between components is a general trend in the electronics industry, particularly for handheld electronic products such as camcorders, cameras, cell phones and laptops. Another driving force for smaller components is the increasing complexity of features and functions. Passive components occupy a significant area on the PCB, especially for analog and mix-signal applications that use a larger number of passives compared to a typical digital system [83]. Reducing the size of the passive components and the spacing between them would increase the packaging density, and is an efficient way to miniaturize many electronic products.

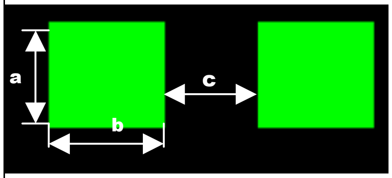
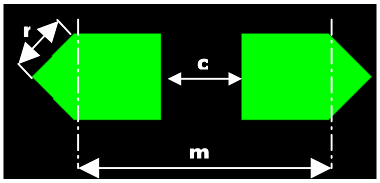
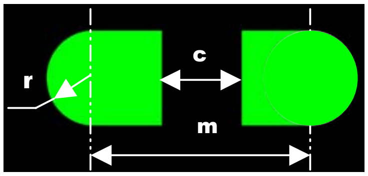
The second trend impacting the electronics industry is the switch to lead-free solder in response to the RoHS and WEEE Directives in Europe, recycling laws in Japan and pending regulations in China and California. The wetting characteristics of lead-free solders are different from eutectic Sn/Pb [84], and higher reflow temperatures are required.

Recently, 0201 components have been implemented in very high density applications such as mobile phones, blue tooth modules, and wireless LANs after extensive process optimization [85-92]. Resistors and capacitors are now being produced in the extremely miniaturized 01005 size (0.4mm×0.2mm). However, the use of such tiny components poses challenges for SMT assembly. The main factors affecting the 01005 assembly process can be divided into the following categories: PCB design, components, stencil, solder paste, PCB handling, printing, pick and placement, reflow and inspection [93, 94]. In order to investigate the effect of PCB design on assembly yield, a 01005 test vehicle was designed with different pad sizes, resistor-to-resistor spacing, shapes and orientations. Experiments were performed to optimize and characterize the solder paste printing, component placement and reflow processes.

## 5.2 Test Vehicle Design

In order to optimize pad designs and evaluate assembly processes for 01005 components, a test vehicle was designed. The pad dimensions are shown in Table 5.1. Pad Size Type 1 is considered ‘nominal’. The pads were non-solder mask defined (NSMD). The other variables in the PCB design included: one laser drilled via in one of the two pads; a laser drilled via in both of the pads; no via in either pad; different orientations ($0^o$, $45^o$ and $90^o$); resistor-to-resistor spacing; and intentional solder mask misalignment.

Table 5.1 Pad Dimensions (unit: mil).

| Pad size No. | Pad Type | a | b | c | r | m | Stencil Area Ratio | |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | 3mil | 4 mil |
| Pad size 1, 100% | Rectangular | 8.0 | 8.7 | 7.0 | | | 0.624 | 0.468 |
| Pad size 2, 90% | Rectangular | 7.2 | 7.8 | 7.0 | | | 0.695 | 0.521 |
| Pad size 3, 110% | Rectangular | 8.8 | 9.5 | 7.0 | | | 0.761 | 0.571 |
| Pad size 4, 120% | Rectangular | 9.6 | 10.4 | 7.0 | | | 0.832 | 0.624 |
| Pad size 5, 130% | Rectangular | 10.4 | 11.3 | 7.0 | | | 0.903 | 0.677 |
| Pad size 6, | Home base 1 | | | 7.0 | 5.6 | 23.0 | 0.755 | 0.566 |
| Pad size 7, | Home base 2 | | | 7.0 | 4.0 | 19.0 | 0.748 | 0.561 |
|  Rectangular | |  Home base 1 | | | | |  Home base 2 | |

The test vehicle, shown in Figure 5.1, was a single-sided 4-layer, high $T_g$ ($T_g$>170°C) FR-4 board with 9600 resistor sites, 8 CSP sites and 1 BGA site on one side. The pads had an immersion silver finish. The test board was 8.0" by 6.0" by 0.042" thick and replicated the basic test pattern in a 2 x 2 array. There were a total of 20 design groups located in each quadrant of the board: nine groups with 90° orientation; nine groups with 0° orientation; one group with 45° orientation; and one group with 0° orientation, with the solder mask intentionally shifted along the length of the resistor. The individual design groups were the different pad sizes and shapes, as well as via-in-one-pad and via-in-two-pad designs. Within each design group, the resistor-to-resistor spacing was systematically varied. Round global and local (a set for each quadrant) fiducials were also included in the design.

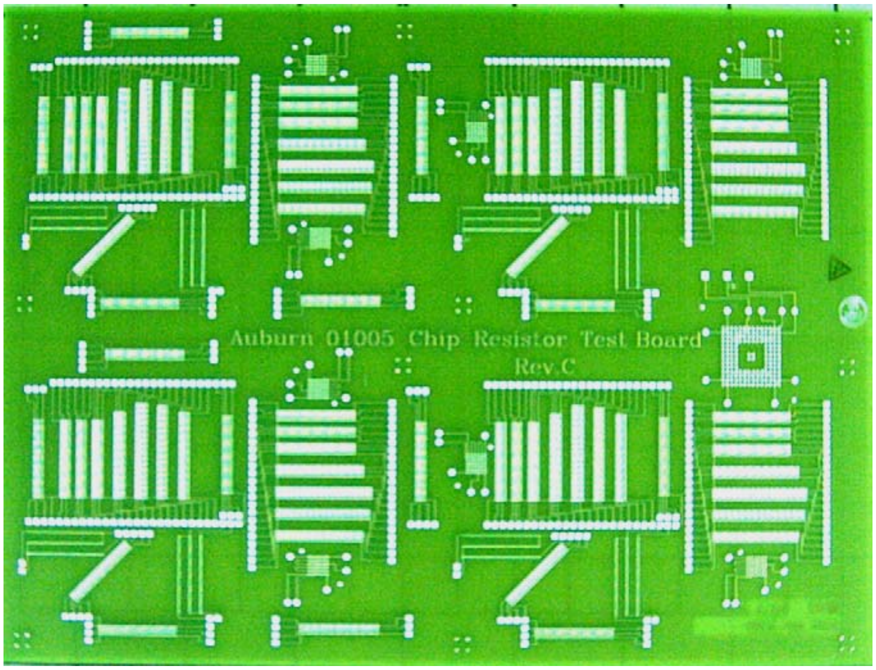


Figure 5.1 01005 Test Vehicle.

## 5.3 Process Capability Evaluation of Board Manufacturing

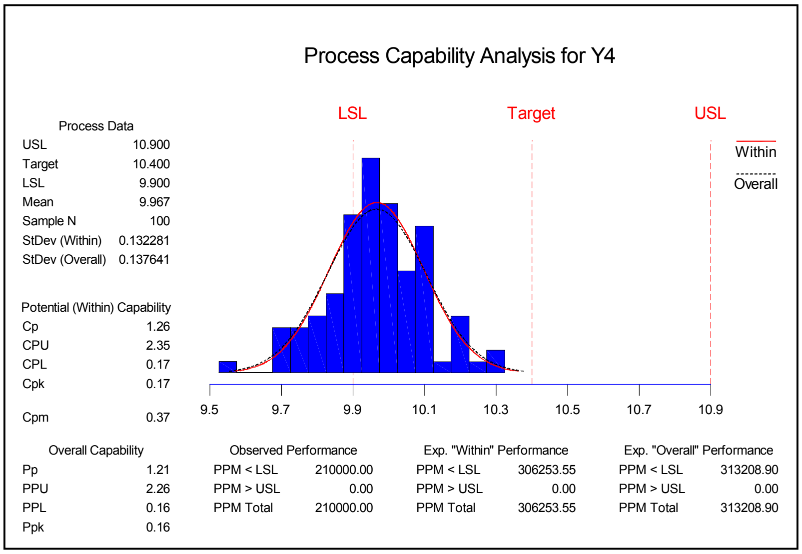
The board quality is important for reliable and consistent SMT assembly. To determine if the board manufacturing was capable, and if the boards met the specification limits, capability analysis was performed on the incoming boards. Five rectangular pad size designs and five different spacing designs were chosen for measurement. Fifty samples per board were measured for two boards. Based on the design specifications, the pad width and spacing tolerance was ±0.5mil.

Process capability analysis for normal distribution samples was conducted using Minitab 13.0. In this analysis, the process variation was measured by 6 standard deviations (+/-3$\sigma$ on each side of the mean). For the pad dimension, the process capability statistics are summarized in Table 5.2, and one of corresponding capability histograms of the individual measurements overlaid with a normal curve based on the process mean and standard deviation is shown in Figure 5.2. Similarly, for the pad spacing, the process capability statistics are summarized in Table 5.3, and the corresponding capability histogram of the individual measurements is shown in Figure 5.3.

From the statistical results in Table 5.2 and Figure 5.2, it is clear that the process for pad size is non-centered on the target, most of pads are smaller than the target, and the whole normal distribution is shifted to the LSL (Lower Specification Limit). Nominally, the pads are ~0.5mil smaller than the design value.

Table 5.2 Process Capability Statistics of the Pad Dimensions (unit: mil).

| | X1 | Y1 | X2 | Y2 | X3 | Y3 | X4 | Y4 | X5 | Y5 |
|---|---|---|---|---|---|---|---|---|---|---|
| Ave. | 7.48 | 8.25 | 6.70 | 7.39 | 8.29 | 9.09 | 8.97 | 9.97 | 9.95 | 10.73 |
| Std. Dev. | 0.19 | 0.19 | 0.20 | 0.17 | 0.20 | 0.15 | 0.13 | 0.14 | 0.27 | 0.24 |
| Target | 8.00 | 8.70 | 7.2 | 7.8 | 8.80 | 9.50 | 9.60 | 10.40 | 10.40 | 11.30 |
| USL | 8.50 | 9.20 | 7.70 | 8.30 | 9.30 | 10.00 | 10.10 | 10.90 | 10.90 | 11.80 |
| LSL | 7.50 | 8.20 | 6.70 | 7.30 | 8.30 | 9.00 | 9.10 | 9.90 | 9.90 | 10.80 |
| $C_p$ | 0.89 | 0.89 | 0.85 | 0.99 | 0.85 | 1.12 | 1.27 | 1.21 | 0.63 | 0.69 |
| $C_{pU}$ | 1.82 | 1.70 | 1.71 | 1.81 | 1.73 | 2.05 | 2.87 | 2.27 | 1.19 | 1.46 |
| $C_{pL}$ | -0.04 | 0.08 | -0.01 | 0.18 | -0.02 | 0.20 | -0.33 | 0.16 | 0.07 | -0.09 |
| K | 1.05 | 0.90 | 1.01 | 0.82 | 1.02 | 0.82 | 1.26 | 0.87 | 0.89 | 1.13 |
| $C_{pK}$ | -0.04 | 0.08 | -0.01 | 0.18 | -0.02 | 0.20 | -0.33 | 0.16 | 0.07 | -0.09 |



| Process Data | |
|---|---|
| USL | 10.900 |
| Target | 10.400 |
| LSL | 9.900 |
| Mean | 9.967 |
| Sample N | 100 |
| StDev (Within) | 0.132281 |
| StDev (Overall) | 0.137641 |

| Potential (Within) Capability | |
|---|---|
| Cp | 1.26 |
| CPU | 2.35 |
| CPL | 0.17 |
| Cpk | 0.17 |
| Cpm | 0.37 |

| Overall Capability | |
|---|---|
| Pp | 1.21 |
| PPU | 2.26 |
| PPL | 0.16 |
| Ppk | 0.16 |

| Observed Performance | |
|---|---|
| PPM < LSL | 210000.00 |
| PPM > USL | 0.00 |
| PPM Total | 210000.00 |

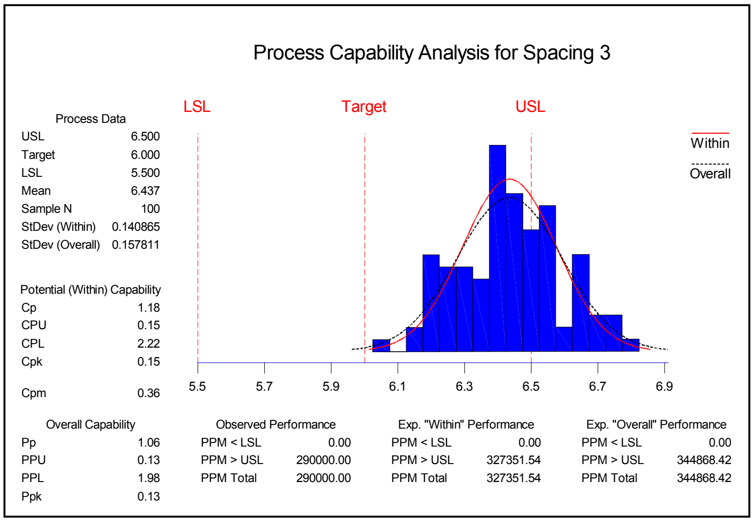
| Exp. "Within" Performance | |
|---|---|
| PPM < LSL | 306253.55 |
| PPM > USL | 0.00 |
| PPM Total | 306253.55 |

| Exp. "Overall" Performance | |
|---|---|
| PPM < LSL | 313208.90 |
| PPM > USL | 0.00 |
| PPM Total | 313208.90 |

Figure 5.2 Capability Histogram for Y4 (Pad Size 4).

Table 5.3 Process Capability Statistics of the Pad Spacings (unit: mil).

| | Spacing 1 | Spacing 2 | Spacing 3 | Spacing 4 | Spacing 5 |
|---|---|---|---|---|---|
| Ave. | 4.32 | 5.36 | 6.44 | 8.51 | 15.61 |
| Std. Dev. | 0.18 | 0.19 | 0.16 | 0.22 | 0.19 |
| Target | 4.00 | 5.00 | 6.00 | 8.00 | 15.00 |
| USL | 4.50 | 5.50 | 6.50 | 8.50 | 15.50 |
| LSL | 3.50 | 4.50 | 5.50 | 7.50 | 14.50 |
| $C_p$ | 0.92 | 0.88 | 1.06 | 0.77 | 0.89 |
| $C_{pU}$ | 0.33 | 0.24 | 0.13 | -0.02 | -0.19 |
| $C_{pL}$ | 1.50 | 1.51 | 1.98 | 1.56 | 1.97 |
| K | 0.64 | 0.73 | 0.87 | 1.03 | 1.22 |
| $C_{pK}$ | 0.33 | 0.24 | 0.13 | -0.02 | -0.19 |



```
Process Data
USL               6.500
Target            6.000
LSL               5.500
Mean              6.437
Sample N            100
StDev (Within)  0.140865
StDev (Overall) 0.157811

Potential (Within) Capability
Cp                 1.18
CPU                0.15
CPL                2.22
Cpk                0.15

Cpm                0.36

Overall Capability
Pp                 1.06
PPU                0.13
PPL                1.98
Ppk                0.13

Observed Performance
PPM < LSL          0.00
PPM > USL     290000.00
PPM Total     290000.00

Exp. "Within" Performance
PPM < LSL          0.00
PPM > USL     327351.54
PPM Total     327351.54

Exp. "Overall" Performance
PPM < LSL          0.00
PPM > USL     344868.42
PPM Total     344868.42
```

Figure 5.3 Capability Histogram for Pad-to-Pad Spacing 3.

From the statistical results in Table 5.4 and Figure 5.3, it can be seen that the process for spacing is non-centered on the target. Most of the spacings are larger than the target, and the whole normal distribution is shifted to the USL (Upper Specification Limit). For both pad size and spacing, $C_{pk} << 1$, indicating the process capability did not meet the desired process specifications. A compensation factor was used in plotting the imaging artwork to address processing factors by the board manufacturer. However, due to the small spacing designed into the test vehicle, the amount of compensation that could be used was limited. In the subsequent discussions of assembly process optimization, the design value (not the actual value) of the pad and space will be used to describe the pads and spacings.

Direct laser imaging was used to define the solder mask. As shown in Figure 5.4, the solder mask could not be designed between the pads with spacings of 4mil and 5mil given a $\underline{+}$2mil solder mask alignment tolerance specification.

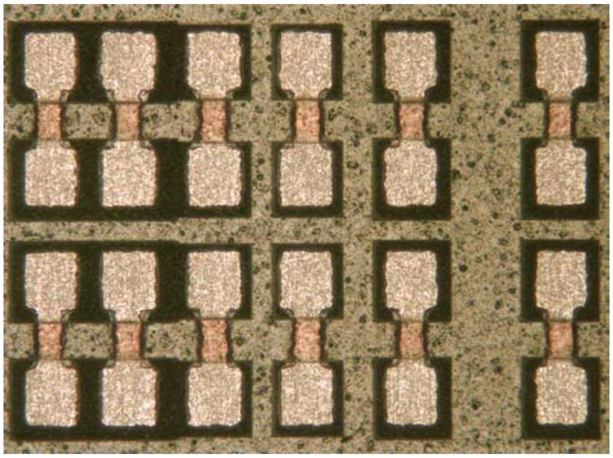


Figure 5.4. Photograph of Pads and Solder Mask Showing Lack of Solder Mask between Pads with 4mil and 5 mil spacing. The other pad spacings are 6mil, 8mil and 15mil.

## 5.4 Printing Optimization

Solder paste printing is a critical step in the SMT process, with the majority of SMT assembly defects related to this process step. In this project, four main factors were investigated: stencil thickness, squeegee pressure, squeegee speed and stencil-board separation speed. The factors and levels are shown in Table 5.4, with the corresponding Taguchi's L8 OA shown in Table 5.5. For each DOE run, 3 boards were printed with a fully automated MPM AP printer and then inspected with a 3D solder paste inspection system (MVT SP-1). The solder paste height and volume data of 20 reference designators for pad size 5 (130%) were collected for analysis.

The solder paste used in this test was Kester EM907 SAC305 (96.5%Sn/3% Ag/0.5%Cu) lead-free solder paste with 88.5% metal content and Mesh 400. Two electroformed stencils with 3mil and 4mil thickness were tested in this experiment. The aperture shape was the same as the pad shape, and the ratio of aperture to pad size was 100%. The area ratio (AR), defined as the ratio of the opening area of the aperture to the wall area of the aperture, were calculated and are given in Table 5.1.

Table 5.4 Factors and Levels for 01005 Printing DOE.

| Factors | Level 1 | Level 2 |
|---|---|---|
| A: stencil thickness | 3mil | 4mil |
| B: Printing Speed | 1in/sec | 2in/sec |
| C: Squeegee Pressure | 10lb | 14lb |
| D: Separate speed | 0.01in/sec | 0.025inch/sec |

Table 5.5 Taguchi's L8 OA for Printing DOE.

| Run No. | A | B | C | D |
|---|---|---|---|---|
| | Stencil thickness | Printing speed | Squeegee pressure | Separate speed |
| 1 | 1 | 1 | 1 | 1 |
| 2 | 1 | 1 | 2 | 2 |
| 3 | 1 | 2 | 1 | 2 |
| 4 | 1 | 2 | 2 | 1 |
| 5 | 2 | 1 | 1 | 1 |
| 6 | 2 | 1 | 2 | 2 |
| 7 | 2 | 2 | 1 | 2 |
| 8 | 2 | 2 | 2 | 1 |

Before running the tests, the 3D solder paste inspection system was calibrated, and the 3D solder paste inspection results after calibration are shown in Figure 5.5. A Gage R & R (Gage Repeatability & Reproducibility) study was conducted. Variability of reproducibility is due to differences between more than one gage/operator combination. Variability of repeatability is due to differences in successive readings by a single gage/operator combination. The Gage R&R results are shown in Figure 5.6 based on solder paste Height and Volume response. Since there was only one gauge/operator combination, the variability of reproducibility is 0. It can be seen that most of the variation is due to differences between parts. The Gage R & R result based on height response is 7.5% and the Gage R & R result based on volume response is

9.83%; both measurement errors of the gage are less than 10% of the measurements of the product characteristic, which indicates this inspection machine is capable and appropriate for 3D solder paste inspection.

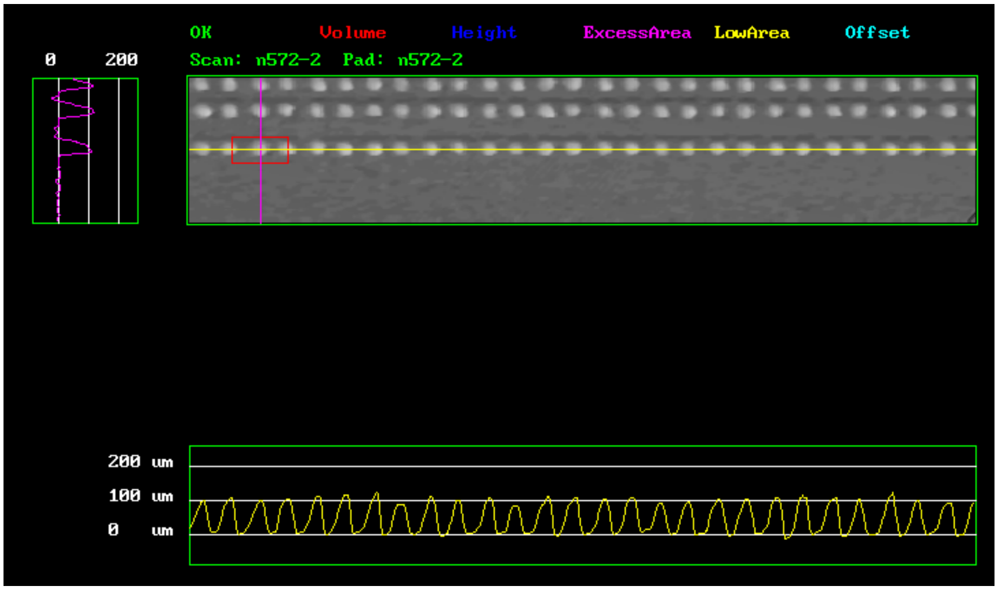


Figure 5.5 3D Solder Paste Inspection Using the MVT SP-1 after Calibration.

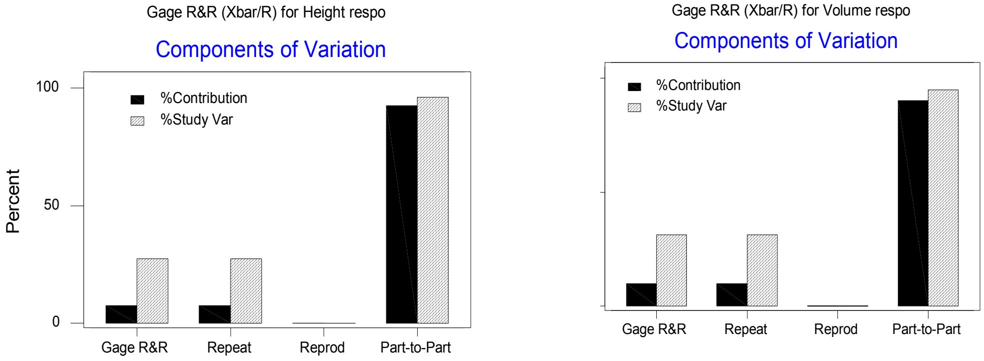


Figure 5.6 Gage R&R for Height and Volume Response.

Figures 5.7 and 5.8 show the Taguchi DOE analysis results. Figure 5.7 is the main effect plot for means based on solder paste volume transfer efficiency. Volume transfer efficiency (volume of solder paste transferred/volume of stencil aperture) was used to normalize the difference in solder paste volume due to stencil thickness. From Figure 5.7, only the stencil thickness had an obvious effect on volume transfer efficiency. The stencil with 3 mil thickness had a better transfer efficiency (more than 95%) than the stencil with 4 mil thickness (72%), which correlated with the area ratio, since the area ratio has the biggest impact on transfer efficiency and repeatability of the solder paste deposits [94]. The 3mil stencil with a pad size 5 had a higher area ratio (0.903) than the 4mil stencil (0.677). Usually an area ratio of $\geq 0.66$ is considered acceptable in the industry [95]. The separation speed had a slight effect; quicker separation contributed to higher transfer efficiency. Printing speed also had a minor effect, while squeegee pressure had an insignificant effect on transfer efficiency.

Further examination of the DOE results by analysis of variance on the S/N ratio is shown in Figure 5.8. Here, the experiment was conducted with “nominal is the best” quality characteristic. A higher S/N ratio is preferred because a high value of S/N implies that the signal is much higher than the uncontrollable noise factors. The optimal print parameters can be identified based on the S/N ratio plot. The optimal print parameters were: stencil thickness 3mil, printing speed: 2 in/sec, squeegee pressure: 14lb, separate speed: 0.01in/sec. Figure 5.9 shows the printing performance using the optimized print parameter settings.

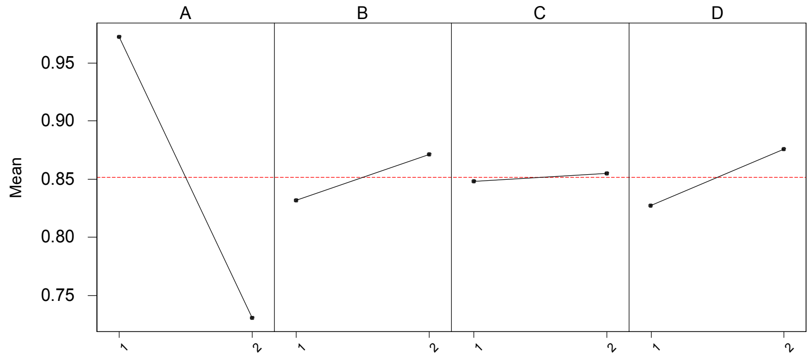


Figure 5.7 Main Effects Plot for Means Based on Volume Transfer Efficiency.

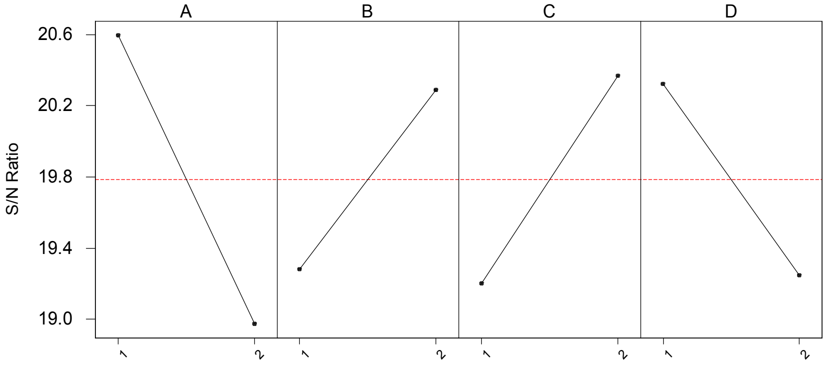


Figure 5.8 Main Effects for S/N Ratio Based on Volume Transfer Efficiency.

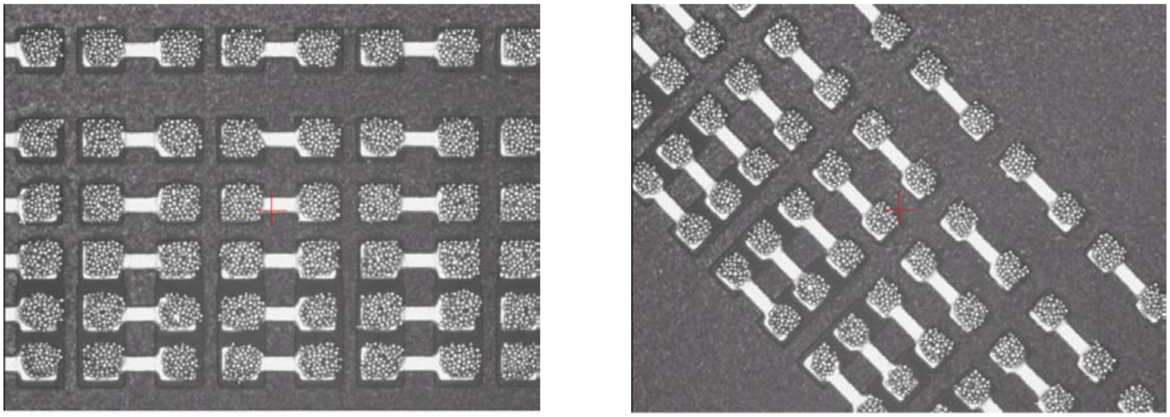


Figure 5.9 Printing Performance Using Optimized Print Settings.

Figure 5.10 shows the process capability index ($C_p$) comparison of solder paste height for different pad size types using the two stencils based on the optimal print settings. The upper and lower specification limit is set to ±5% mean value. For each stencil, the volume for fifty reference designators was collected for data analysis. The 3mil stencil was more process capable and robust than the 4mil stencil, which confirmed the above DOE results. Similarly, the bigger pad size types with higher area ratio had larger process capability indices. The 3 mil thick stencil was used for all subsequent assembly experiments.

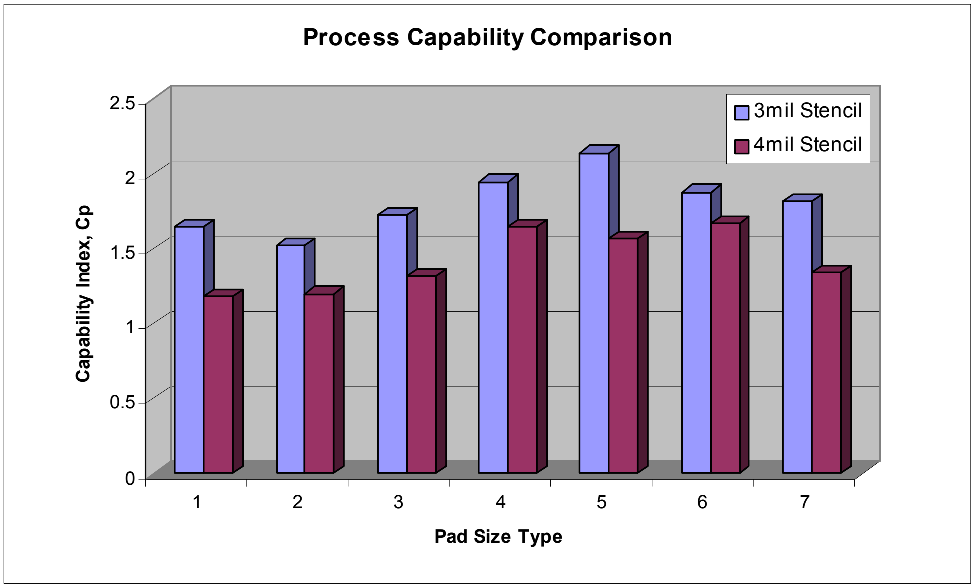


Figure 5.10 Process Capability Comparison for Two Stencils and Pad Size Types.

## 5.5 Placement Accuracy Evaluation

The typical size of the 01005 resistor was 0.38mm x 0.18mm, with a termination width of 0.08mm. 01005 components are supplied in a regular 8mm tape and reel with a

2mm pitch between pockets. There were two common orientation defects in as-received components in the tape & reel, as shown in Figure 5.11: edge-standing and upside-down components. Sometimes edge-standing components damaged the nozzle tip during pick and place of the component. Edge-standing components may also be placed since the width and thickness of these tiny components are similar and the difference may not be readily discerned by the pick and place vision system. Upside-down components have the appropriate length and width dimensions and will typically not be rejected by the pick and place vision system.

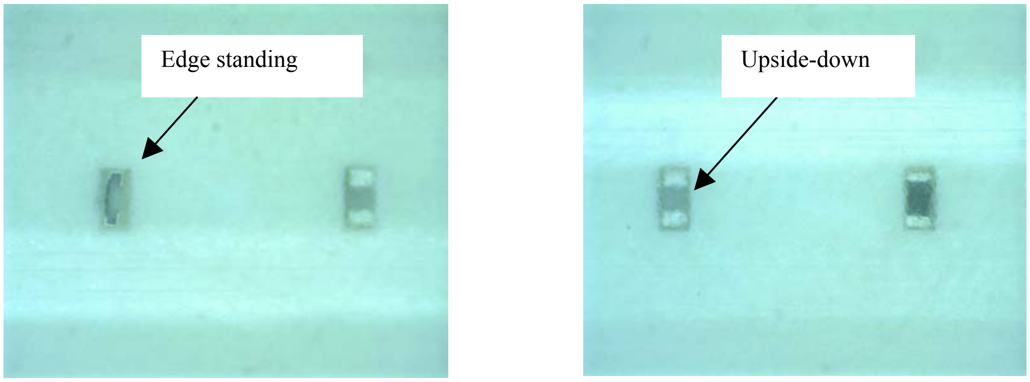


Figure 5.11 Two Common Orientation Defects in As-received 01005 Components in Carrier Tape.

The 01005 components were placed with an Assembleon ACM Micro pick and placement machine. A new nozzle body and tip were specially designed for 01005 placement. The diameter of the nozzle tip was 0.38mm and the opening of the tip was 0.14mm. The maintenance of such a tiny and precise tip is very important. Once the tip becomes worn or is no longer flat enough, it will have an obvious effect on the placement performance. Feeder precision is sensitive for consistent pick performance.

The objective of the placement tests was to compare the placement accuracy when using 2 or 3, local or global fiducials. Four tests were performed based on: 2 round global fiducials, 3 round global fiducials, 2 round local fiducials and 3 round local fiducials. The distances X1, Y1, X2 and Y2, shown in Figure 5.12, were measured to calculate the component's centroid offset and rotation. Two boards were run for each test and 25 components were randomly select for measurement. The calculated offset and rotation data were analyzed using the statistics software Minitab 13.0. Table 5.6 lists the mean and $C_{PK}$ for all combinations. The Centroid Offset (CO) is calculated as:

$$CO = \sqrt{(\Delta x)^2 + (\Delta y)^2}$$

From these data, it can be seen that using 3 local fiducials results in the best placement accuracy. The subsequent assembly used 3 local fiducials for placement.

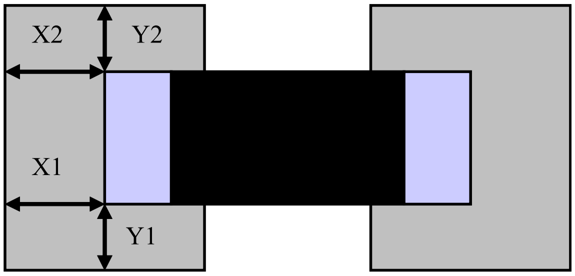


Figure 5.12 Schematic of Distances X1, Y1, X2 and Y2.

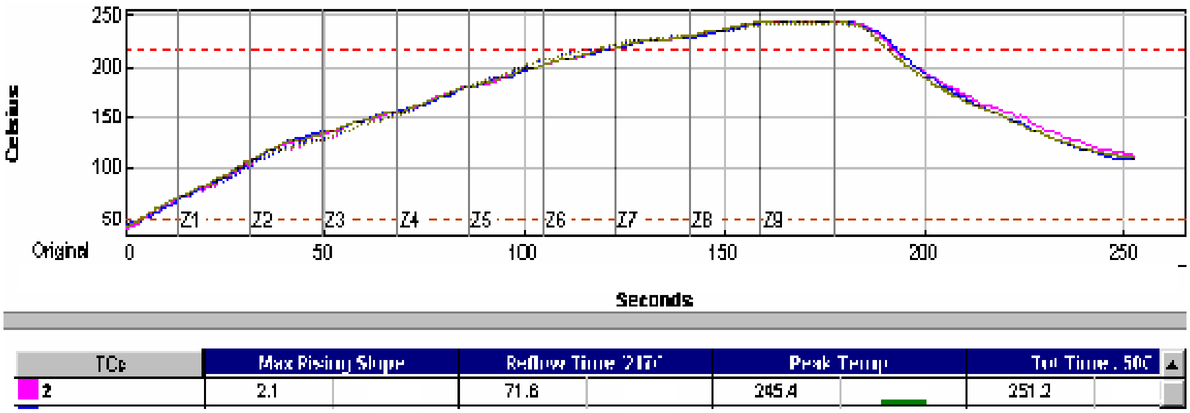
Table 5.6 The Means and $C_{PK}$ for Placement Accuracy Evaluation.

| Fiducial | Centroid Offset, (mm) | | | Rotation, (Degree) | | |
|---|---|---|---|---|---|---|
| | Orientation | 0 | 90 | Orientation | 0 | 90 |
| 2 Global Fiducial | Mean | 0.024 | 0.023 | Mean | -0.90 | 0.55 |
| | $C_{pk}$ | 0.93 | 1.45 | $C_{pk}$ | 1.03 | 1.21 |
| 3 Global Fiducial | Mean | 0.026 | 0.022 | Mean | -1.052 | -0.206 |
| | $C_{pk}$ | 0.98 | 1.54 | $C_{pk}$ | 1.41 | 2.25 |
| 2 Local Fiducial | Mean | 0.011 | 0.026 | Mean | -1.129 | 0.34 |
| | $C_{pk}$ | 2.18 | 1.87 | $C_{pk}$ | 1.81 | 2.13 |
| **3 Local Fiducial** | Mean | 0.014 | 0.018 | Mean | 0.643 | 0.521 |
| | **$C_{pk}$** | **2.21** | **2.32** | **$C_{pk}$** | **2.08** | **3.12** |

### 5.6 Reflow

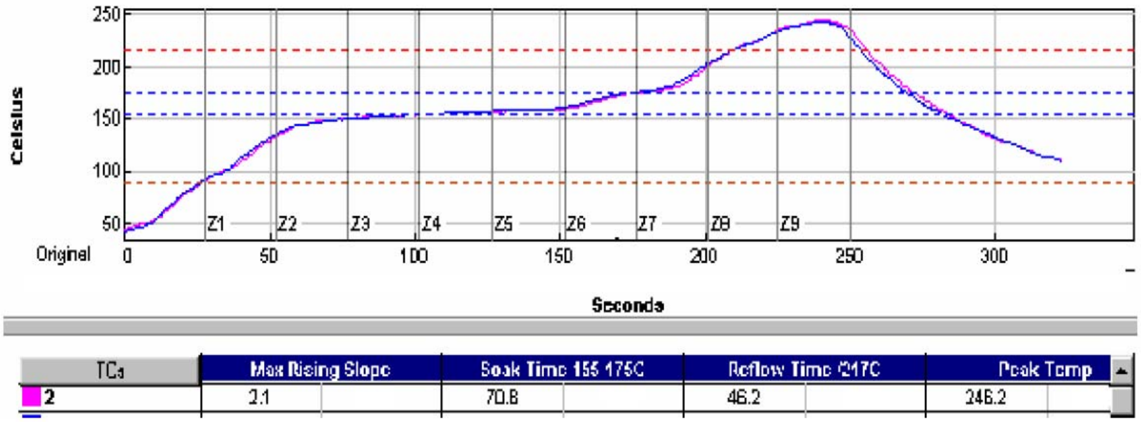
Reflow was carried out in a Heller 1800 reflow oven. Two reflow profiles, a quick-ramp and a soak profile shown in Figures 5.13 and 5.14, were used for lead-free soldering. Initially, one board was reflowed in air; however, the wetting was not satisfactory, and individual solder spheres could be seen under the microscope.

The 01005 solder paste deposits were so small that most of the solder alloy was exposed to the reflow atmosphere, which could lead to surface oxidation in an air environment. Subsequently, nitrogen was used for reflow and good wetting was observed. Figure 5.15 shows a comparison of the wetting performance in air and nitrogen reflow atmospheres. Solder joints reflowed using the two reflow profiles were x-rayed. Figure 5.16 shows typical x-ray images. Both profiles resulted in some voiding, primarily in the fillet, but also under the resistor terminals.



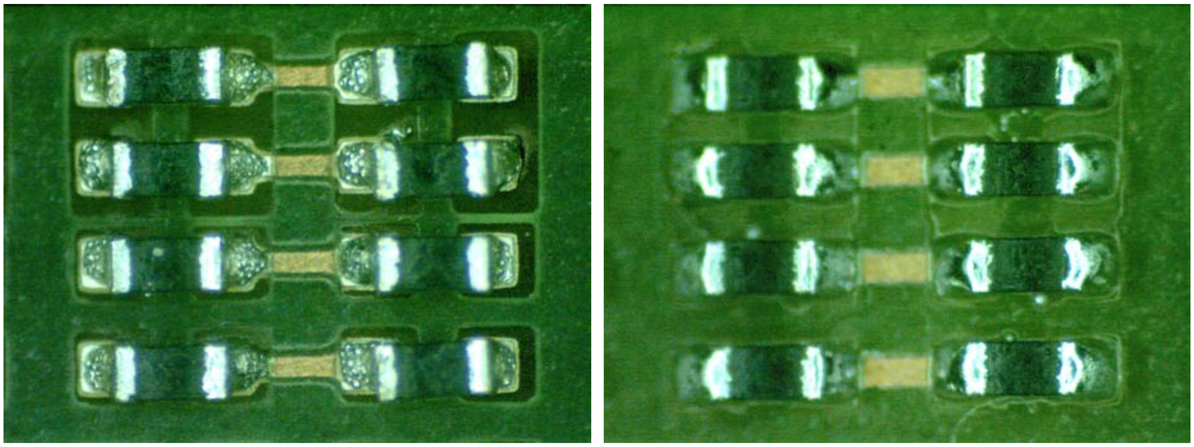
| TCs | Max Rising Slope | Reflow Time 217C | Peak Temp | Tot Time . 50C |
|---|---|---|---|---|
| 2 | 2.1 | 71.8 | 245.4 | 251.2 |

Figure 5.13 Lead-free Quick-ramp Reflow Profile.



| TCs | Max Rising Slope | Soak Time 155 175C | Reflow Time 217C | Peak Temp |
|---|---|---|---|---|
| 2 | 2.1 | 70.8 | 46.2 | 246.2 |

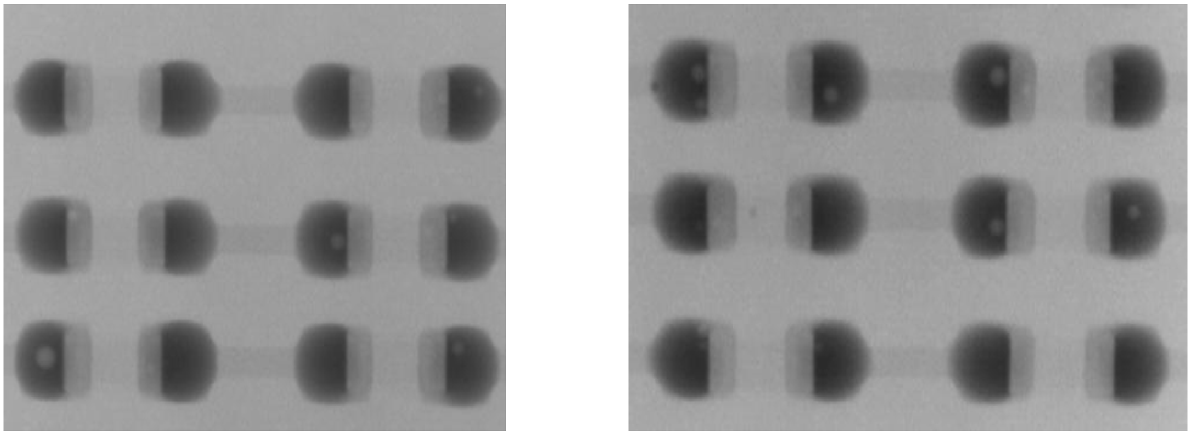
Figure 5.14 Lead-free Soak Reflow Profile.



(a) Reflow in air

(b) Reflow in nitrogen

Figure 5.15 Wetting Comparison in Air (a) or Nitrogen (b).



(a) Ramp Profile

(b) Soak Profile

Figure 5.16 X-ray of Solder Joints for Ramp (a) and Soak (b) Profiles in Nitrogen.

## 5.7 Post Reflow Inspection

After reflow, all of the boards were inspected using a VISCOM PCB automated optical inspection machine, and the number of defects was collected. Defects observed after reflow included bridging, tombstone, edge-standing parts, missing parts and upside-down parts. There were a total of 2,296 defects out of 28,920 resistor placements, i.e. a 7.94% defect rate. This includes all combinations of pads, spacings, reflow profiles, orientations, and via-in-pad. Table 5.7 lists the defect distribution in all samples. Figure 5.17 shows a pie chart of the defect distribution for all defects. Bridging and tombstones are the primary defects (68%). Figure 5.18 illustrates the common defects.

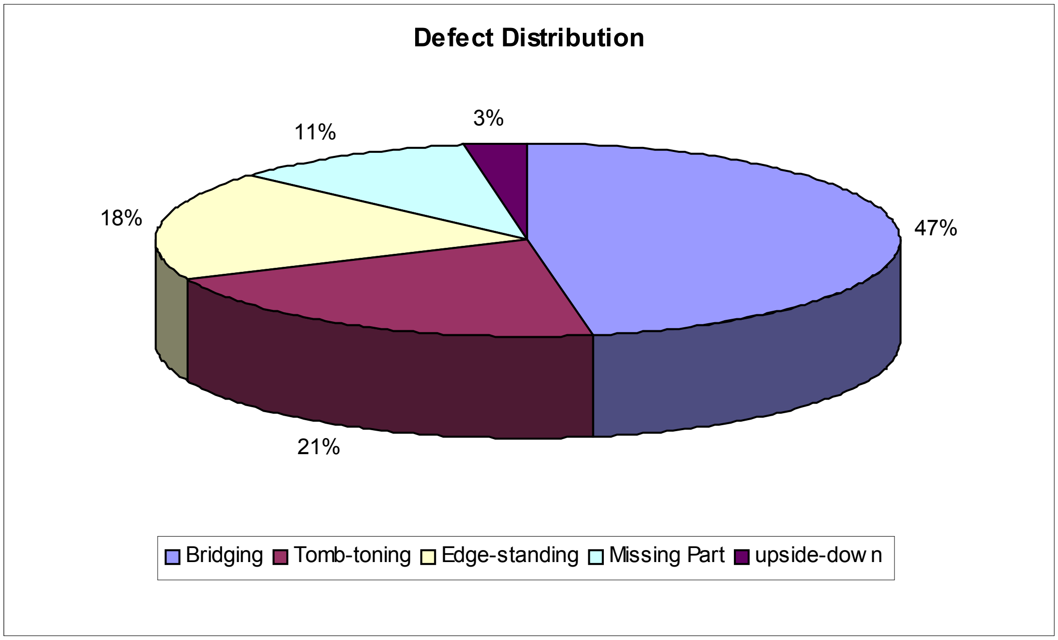
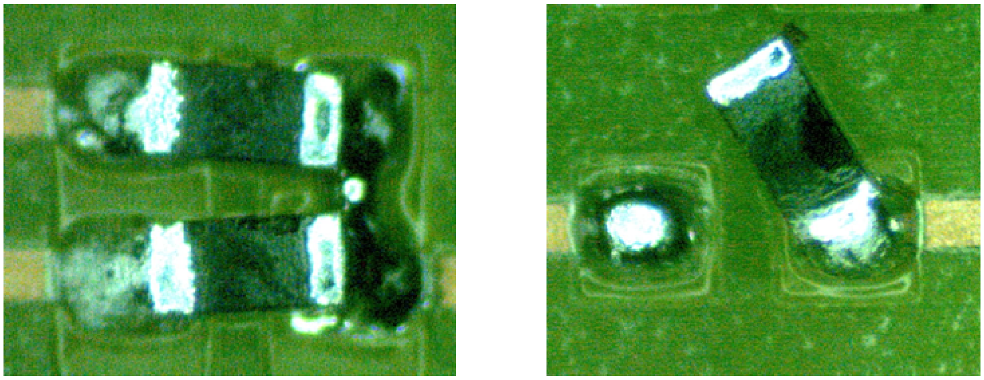


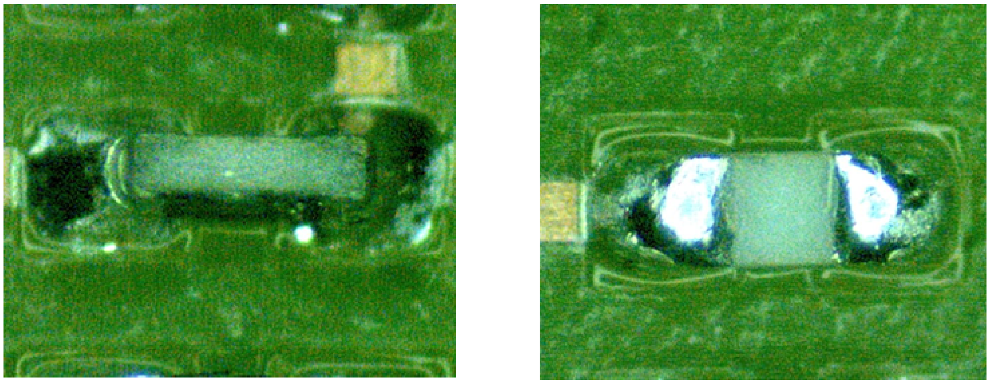
Figure 5.17. Defect Distribution in for all Build Combinations.

Table 5.7 Defect Distribution in All Samples.

| Defect | Bridging | Tombstone | Edge-standing | Missing Part | Upside-down | Sum |
|---|---|---|---|---|---|---|
| Sum | 1086 | 485 | 416 | 245 | 64 | 2296 |
| Percentage | 3.75% | 1.68% | 1.44% | 0.85% | 0.22% | 7.94% |



Bridging Tombstone



Edge-standing Upside-down

Figure 5.18 Example of Different Defects.

### 5.7.1 Bridging

90.3% of the bridging occurred in the Space 1 (4mil pad-to-pad) group and 9.7% of the bridging was in the Space 2 (5mil pad-to-pad) group. As previously noted in Figure 5.4, there was no solder mask patterned between the pads at these tight spacings. There were no bridges for pad-to-pad spacing of 6mil or greater. Figure 5.19 shows the bridging defect rate comparison for different pad size types. It can be seen that larger pad sizes resulted in more bridging for rectangular pads and the home base design had more tendency for solder bridging than the rectangular pads. A minimum of 6mil pad-to-pad spacing for parallel resistors is therefore recommended for 01005 chip resistors.

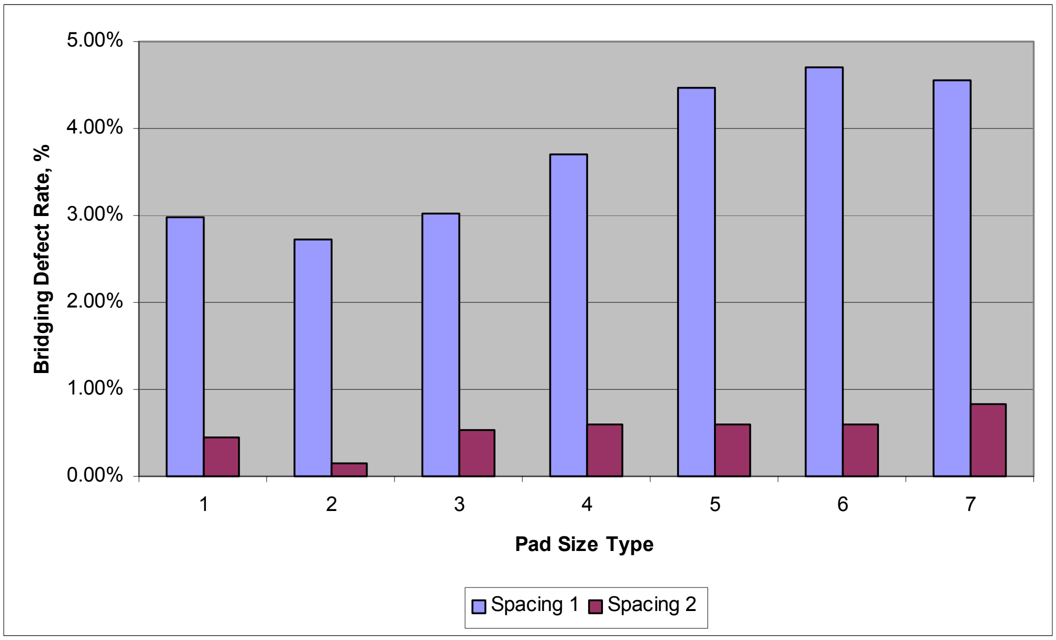


Figure 5.19 Bridging Defect Rate Comparison for Different Pad Size Types.

### 5.7.2 Tombstones

Figure 5.20 shows the influence of pad-in-via design on tombstones for Pad Size Type 1 (100%) pads. As expected, via-in-pad design significantly increases the likelihood of tombstones, with a via in only one of the two pads being slightly worse.

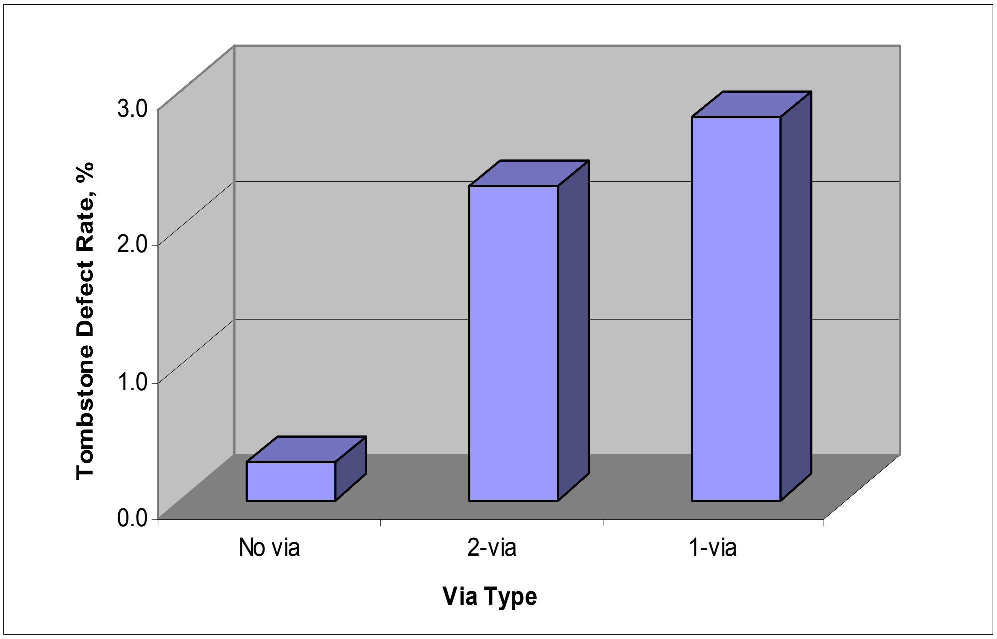


Figure 5.20 Tombstone Defect Rate Comparison for Pad Size Type 1 with and without Via-in-pad.

Figure 5.21 plots the effect of the reflow profiles on tombstone defect rates. The data includes all pad size types and resistor orientations. The direct ramp-to-peak profile is significantly better than the soak profile.

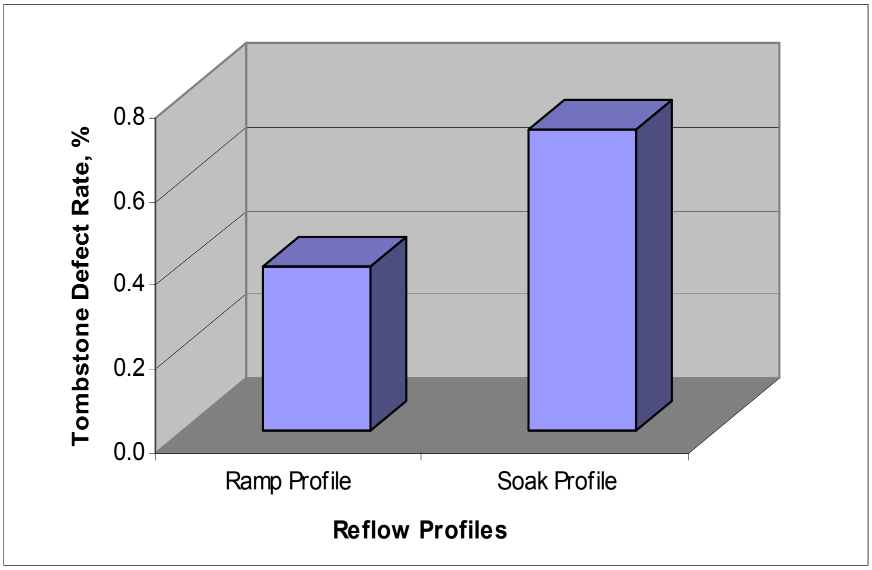


Figure 5.21 Tombstone Defect Rate as a Function of Reflow Profile.

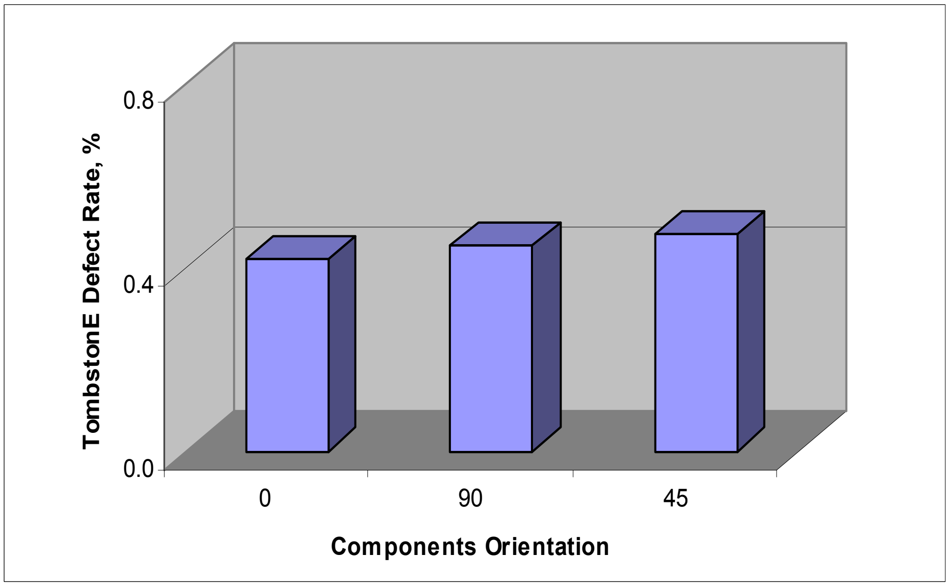


Figure 5.22 Tombstone Defect Rate as a Function of Resistor Orientation for Type 1 Size Pads.

Figure 5.22 plots the tombstone defect rate as a function of resistor orientation for Type 1 Size Pads (100%). It includes data for both reflow profiles. Resistor orientation was found to have little effect on tombstones.

Figure 5.23 plots the effect of pad size type on tombstone defect rates. The data includes both $0^o$ and $90^o$ orientations and both reflow profiles. Increasing the pad size (and volume of solder) had a significant impact on the tombstone defect rate. With the ramp profile, rectangular pads with no via-in-pad and designed at 90% of the nominal pad size (Pad Size Type 2) produced 5 tombstones in 6960 placements, independent of $0^o$ or $90^o$ resistor orientation, for a tombstone rate of 718ppm. One of tombstones was also edge-standing.

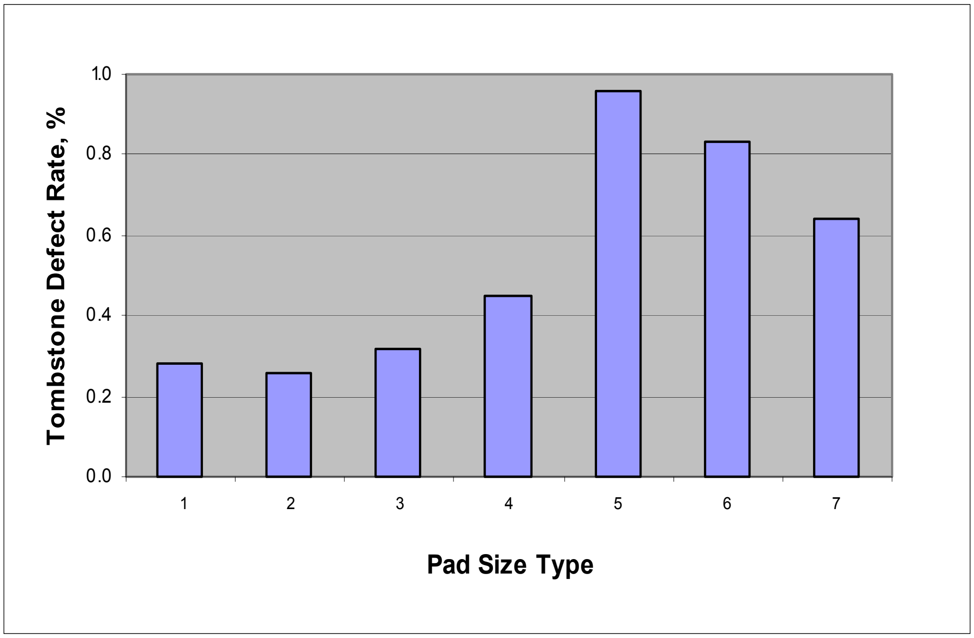


Figure 5.23 Tombstone Defect Rate as a Function of Pad Size Type.

Figure 5.24 compares the tombstone defect rate for pad size Type 1, no via pads, with an intentional solder mask shift of 2mil in the resistor length direction. ±2mil was the solder mask design tolerance. Shifting the solder mask unbalanced the area of exposed copper; the pad only on one end and the pad plus 4mil of trace on the other. Solder mask misalignment also increased the tombstone defect rate.

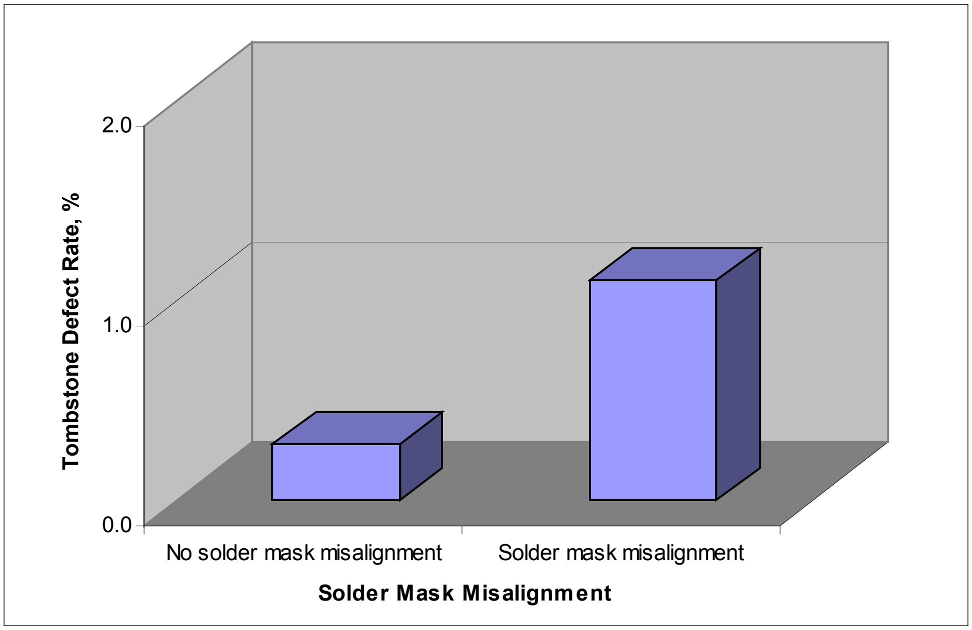


Figure 5.24 Tombstone Defect Rate as a Function of Solder Mask Misalignment for Pad Size Type 1.

### 5.7.3 Missing Parts

Due to the small size of the nozzle tip opening and the component, vacuum sensing could not be used to verify part pick-up. After the nozzle became worn, the surface of the tip became shiny and the vision system would occasionally recognize the shiny tip as the small 01005 component. Tip wear must therefore be carefully monitored in order to avoid missing parts.

### 5.7.4 Edge-standing and Upside-down Components

As mentioned in the placement section, upside-down and edge-standing defects were caused by part orientation in the as-received tape. Given the symmetry of the part, the vision system could not consistently detect edge-standing components and could not detect upside-down components. Upside-down components are not likely to be an issue, as bulk feeding is often used for larger chip components and up or down orientation is not a concern. Edge-standing parts should be addressed in the taping system.

## 5.8 Summary

The placement of 01005 chip resistors has been studied. The board manufacturer did not maintain the design tolerance of ±0.5mil, and the pads were all approximately 0.5mil below design dimensions. An electroformed, 3mil stencil yielded a robust paste printing process and higher $C_p$ indices compared to a 4mil stencil. Nitrogen reflow was required to achieve good solder wetting due to the high surface-to-volume ratio of the solder deposits. With regard to bridging defects, no defects were observed if the pad-to-pad spacing for parallel resistors was 6mil or larger.

Rectangular pads with no via-in-pad and designed at 90% of the nominal pad size (Pad Size Type 2) produced 5 tombstones in 6960 placements with the ramp profile, independent of $0^o$ or $90^o$ resistor orientation, for a tombstone rate of 718ppm. One of tombstones was also edge-standing. Given the undersized pads on the actual board, the 90% pad average width was 6.7mil (versus a design value of 7.2mil) and the measured width of the 01005 chip resistor was 7.1mil. Thus, the pads were slightly smaller in width than the chip resistor.

# CHAPTER 6

# CONCLUSIONS

## 6.1 Processing and Drop Reliability of Corner Bond Chip Scale Packages

The use of CSPs is widespread, particularly in portable electronic products. Many CSP designs already meet the thermal cycle or thermal shock requirements for these applications. However, mechanical shock (drop) and bending requirements often necessitate the use of underfills to increase the mechanical strength of the CSP-to-board connection. Capillary flow underfills processed after reflow provide the most common solution to improving mechanical reliability. However, the use of capillary underfill adds board dehydration, underfill dispensing, flow and cure steps and the associated equipment to the assembly process.

Corner bonded underfill provides a simplified manufacturing process for CSPs that require underfill, eliminating the dehydration bake, capillary flow time and cure. While the drop test reliability is not as high as with complete capillary underfill, corner bond underfill provides a 3-4x improvement compared to no underfill. Corner bond underfill offers a viable, cost-effective approach for many portable product applications. The application and reliability of a corner bond underfill has been demonstrated. Dispensing guidelines have also been provided to apply the material in a way that will not interfere with the soldering process. The material has also been shown to have a minimal impact on the process, curing during the solder reflow, and allowing the parts to self-align.

## 6.2 Lead-free Assembly and Drop Reliability of Chip Scale Packages

The second trend impacting the electronics industry is the switch to lead-free solder in response to the RoHS and WEEE Directives in Europe, recycling laws in Japan and pending regulations in China and California. Three underfill options that are compatible with lead-free assembly have been evaluated in this study: capillary underfill, fluxing underfill and corner bond underfill. CSPs with eutectic Sn/Pb solder were used for control samples. The reflow profile affected the drop test performance and failure mode with the Sn/Ag/Cu CSPs. The longer soak profile resulted in poorer drop test performance with failure occurring in the laminate. The shorter, ramp-to-peak profile was used for all subsequent test vehicle builds.

Without underfill, the lead-free and Sn/Pb eutectic drop results were comparable. With capillary flow underfill, the drop test results were significantly better with lead-free solder assembly than with Sn/Pb eutectic. The lower modulus capillary underfill performed better with both Sn/Pb and Sn/Ag/Cu CSPs in the drop test, while the fluxing underfill with lead-free solder yielded the best drop test results, with no failures after 150 drops. The drop test results with corner bond were intermediate between no underfill and capillary underfill and similar for both lead-free and Sn/Pb eutectic solder assembly.

There was degradation in the drop test results after 100 and 250 hours of storage at 125°C prior to the drop test. Underfill improved the drop test performance of the CSP evaluated in this series of experiments. The different underfill types provide assembly process options, which must be weighed against the difference in drop test performance.

## 6.3 Effect of Surface Finish, Reflow Profile and High Temperature Aging on Drop Test Reliability of Lead-free CSPs

Most drop test reliability data reported for CSPs are for the as-built condition. However, the mechanical shock reliability over the life of the product is equally important. This study provided a systematic study of surface finish (Immersion Sn and Immersion Ag) and reflow profile (cool down rate) on the drop test reliability of CSP assemblies.

As previously reported, the mean number of drops to failure (MDTF) for lead-free CSP assemblies decreased with aging time at 125°C. The results obtained in this study show that surface finish and reflow profile have little or no impact on this phenomenon. Kirkendall voiding does occur at the Cu-to-intermetallic interface with aging at 125°C due to the more rapid diffusion of Cu into Sn than Sn into Cu. However, even after 480 hours of aging at 125°C, the crack propagation path did not travel between voids. In fact, the voids appear in some cases to terminate the propagation of cracks. Thus, the decrease in MDTF must be related to changes in the mechanical properties of the intermetallic layer.

## 6.4 PCB Design and Assembly Process Development of 01005 Components with Lead-free Solder

The continuing demand for smaller, lighter multifunctional portable electronic products has driven the use of miniature components. To satisfy this demand, 01005 chip components are now commercially available. However the application for such tiny components into new products presents some new design and assembly process issues. In this study, a test vehicle was designed to investigate the effect of PCB pad design on assembly yield. The process capability of 01005 test board manufacturing was evaluated. Assembly processes were developed and optimized based on a Design of Experiment (DOE).

The board manufacturer did not maintain the design tolerance of ±0.5 mil, the pads were all approximately 0.5 mil below design dimensions. An electroformed, 3mil stencil yielded a robust paste printing process and higher $C_p$ indices compared to a 4mil stencil. Nitrogen reflow was required to achieve good solder wetting due to the high surface-to-volume ratio of the solder deposits. With regard to bridging defects, no defects were observed if the pad-to-pad spacing for parallel resistors was 6mil or larger. Rectangular pads with no via-in-pad and designed at 90% of the nominal pad size (Pad Size Type 2) produced 5 tombstones in 6960 placements with the ramp profile, independent of $0^o$ or $90^o$ resistor orientation, yielding a tombstone rate of 718ppm. One of tombstones was also edge-standing. Given the undersized pads on the actual board, the 90% pad average width was 6.7mil (versus a design value of 7.2mil) and the measured width of the 01005 chip resistor was 7.1mil. Thus, the pads were slightly smaller in width than the chip resistor.

### 6.5 Recommendations for Future Work

A continuous effort to develop more suitable underfill materials is needed in the future. This includes developing materials that can be pre-applied to packages and then testing the material in a lead-free solder process, such that the package can be supplied with the underfill already attached. The use of pre-applied underfill on components prior to board-level assembly will eliminate many of the uncertainties and problems associated with liquid underfill dispensing.

More tests and SEM/EDS analysis are needed to explore the effect of the OSP and Ni/Au surface finishes on drop reliability, and to examine the degradation mechanism of thermal aging on drop performance.

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