BULK GALLIUM NITRIDE BASED ELECTRONIC DEVICES: SCHOTTKY DIODES, SCHOTTKY-TYPE ULTRAVIOLET PHOTODETECTORS AND METAL-OXIDE-SEMICONDUCTOR CAPACITORS

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DISSERTATION ABSTRACT

BULK GALLIUM NITRIDE BASED ELECTRONIC DEVICES: SCHOTTKY DIODES, SCHOTTKY-TYPE ULTRAVIOLET PHOTODETECTORS AND METAL-OXIDE-SEMICONDUCTOR CAPACITORS

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Gallium Nitride (GaN) is one of most promising semiconductor materials for high power, high temperature and high frequency applications. Due to the lack of native substrates for homoepitaxial growth, GaN electronic devices have been conventionally fabricated on epitaxial GaN layers grown on foreign substrates, mostly sapphire. This scheme complicates the fabrication process and compromises the device performance due to the large amount of native defects within the heteroepitaxial layer. In order to fabricate devices with improved performance and simplified fabrication processes, it is desirable to utilize high quality bulk GaN substrates. Recent developments in Hydride Vapor Phase Epitaxy (HVPE) technology have enabled the successful growth of free-standing GaN wafers with very low dislocation densities. This dissertation reports some developments in the device fabrication, performance and simulation based on bulk GaN substrates.

We have fabricated vertical geometry Schottky diodes with a full backside ohmic contact using a bulk GaN substrate. The absence of the sapphire substrate, improved ohmic contact scheme and the vertical transport mode greatly enhance the forward current conduction of the bulk GaN Schottky diode. The device also displays a high reverse breakdown voltage and ultrafast reverse recovery characteristics.

The low dislocation density of the substrate allows the fabrication of Schottky-type ultraviolet photodetectors with ultralow dark currents. The large band gap of GaN provides the intrinsic “visible blindness” of the UV photodetector. The device displays a reasonably high responsivity and a good linearity of photocurrent with UV irradiance.

We have also fabricated MOS capacitors using a thermally oxidized bulk GaN substrate. The thermal gallium oxide is characterized and its oxidation mechanism and etching process are explored. The thermal grown Ga_2O_3/GaN interface displays a relatively lower interface density of state as compared to the deposited insulator/GaN interfaces.

Schottky diode device simulation has been carried out using Medici software. The simulation shows the utilization of a SiO2 field plate can effectively mitigate the field crowding at the Schottky contact edge and increase the device breakdown voltages.

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CHAPTER 1

INTRODUCTION

Recent developments have allowed Silicon-based semiconductor technology to approach to the theoretical performance limits of this material. However, to date, Si-based devices have not met all the desired requirements for ideal power electronics applications, such as high blocking voltages, low on-state voltage drop, low conduction and switching losses, high switching frequencies and high temperature or harsh environment operation. The wide band gap semiconductor family, which includes Silicon Carbide (SiC), Gallium Nitride (GaN) and diamond, have long demonstrated their potential to replace Si in power electronics applications because of their superior material and electrical properties.

GaN has mostly been aimed at optoelectronics applications, predominantly owing to its large direct band gap.[1] The recent commercialization of GaN light-emitting diodes (LEDs) in the blue and UV wavelengths has fueled interests in this semiconductor. More recently, GaN has also been viewed as a high-power, high-temperature material with its electrical properties potentially even superior to SiC.[2]

The potential of GaN for power electronics stems from its unique material and electrical properties, which include a large band gap (3.4 eV), a high electrical breakdown field (4 MV/cm) and a high electron saturation velocity (3×10^{7} cm/s). A large band gap results in a low intrinsic carrier concentration. For GaN, the intrinsic carrier concentration is 2×10^{-10} cm^{-3} at room temperature, compared to 1×10^{10} cm^{-3} for Si and 2.1×10^{6} cm^{-3} for GaAs. The unmanageable thermal generation of intrinsic carriers occurs at around 150C for Si, while for wide band gap semiconductors, the intrinsic temperature could be as high as 900C. This means that GaN devices can operate at a much higher ambient temperature, at which Si devices can not be used. High temperature operation of power electronic devices is crucial not only for elevated ambient temperatures, but also for the reliability issue caused by device self-heating during high power operation. For Si-based power devices, in order to avoid device failure due to hot-spot formation, complicated cooling systems are designed to maximize the heat extraction. By using GaN devices, a significant reduction in cooling requirements, size and cost can be achieved. The wide band gap also offers high radiation hardness, which allows for less radiation shielding and provides mass and volume advantages in aerospace applications.

The critical electric field for GaN is estimated to be 4 MV/cm, which is over ten times larger than Si. The higher electric field strength in GaN results in a higher breakdown voltage for power devices, which is a crucial attribute for high power requirements. With a higher critical field, higher doping levels and thinner drift regions can be used for the same breakdown voltage, which results in a lower on-state resistance. One of the key factors that limit the use of Si-based unipolar device in power electronics is the high drift region resistance due to the low doping level and thick drift region required to achieve the desired high breakdown voltage. A numerical computation of specific resistance for Schottky diodes designed with n-type Si, GaAs, GaP, 6H-SiC and GaN for various breakdown voltages has shown that the GaN Schottky diode stands out and demonstrates the best performance by having the highest breakdown voltage for a given drift region specific resistance, and lowest resistance for a given breakdown voltage.[3]

A high electron drift velocity is also favorable in high frequency applications. The electron saturation velocity of GaN is as high as 3×10^7 cm/s, which is 3 times higher than that of Si. A higher electron drift velocity allows for a faster removal of charges in the depletion region of a diode, which results in a shorter reverse recovery time. The high frequency capability of GaN is expected to be much better than Si, and also better than SiC at elevated temperatures.[4]

In addition to the key properties discussed above, GaN also has a good electron mobility which is comparable to that of Si. The thermal conductivity of GaN is considerably lower than that of SiC. However, it should be noted that the commonly cited value of 1.3 W/cm•K is almost certainly a lower limit. Witek derived a simple expression for predicting the thermal conductivity of defect-free crystals.[5] Using this expression, he predicted the thermal conductivity of GaN at room temperature to be as high as 4.1 W/cm•K. The discrepancy between his calculation and experimental observation was attributed to the native defects in the GaN. Therefore, the thermal conductivity of GaN is expected to increase with the perfection of material growth techniques. Recently, a higher thermal conductivity of 2.3 W/cm•K was experimentally measured on a high quality bulk GaN substrate with a low dislocation density.[6]

Basic material properties and figure-of-merits (FOM) for several semiconductors are summarized in Table 1.1.[7] The Johnson figure-of-merit (JFOM) is calculated based on the critical electric field and saturation electron drift velocity in defining a measure of the high-frequency capability of a material.[8] For GaN, the JFOM is more than 1000 times that of Si and 4 times that of SiC. The Baliga figure of merit (BFOM) takes into account dielectric constant, carrier mobility and critical electric field to define a measure of minimizing conduction losses in power field effect transistors (FETs).[9] The BFOM for GaN is more than 1000 times that of Si and almost 3 times that of SiC. The combined figure of merit (CFOM) is a comprehensive measure of the high power, high temperature and high frequency capability of a material. GaN has the highest CFOM of all the materials listed in Table 1.1. It is obvious that for high power, high frequency and high temperature applications, GaN offers far better performance than Si or GaAs. Again, the large bandgap, high breakdown field and high electron saturation velocity of GaN make this performance possible.

Table 1.1. Comparison of semiconductor material properties at room temperature

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Property	**Si**	**GaAs**	**4H-SiC**	**GaN**
Bandgap, E_g (eV)	**1.12**	**1.42**	**3.25**	**3.4**
Dielectric constant, ε	**11.8**	**12.8**	**9.7**	**9**
Breakdown field, E_c (MV/cm)	**0.3**	**0.4**	**3**	**4**
Electron mobility, μ ($cm^2/V \cdot s$)	**1500**	**8500**	**1000**	**1250**
Maximum velocity, V_s (10^7cm/s)	**1**	**1**	**2**	**3**
Thermal conductivity, λ ($W/cm \cdot K$)	**1.5**	**0.5**	**4.9**	**2.3**
JFOM[a] = $E_c^2 V_s^2 / 4\pi^2$ (relative to Si)	**1**	**1.8**	**400**	**1600**
BFOM[b] = $\varepsilon \mu E_c^3$ (relative to Si)	**1**	**14.6**	**548**	**1507**
CFOM[c] = $\lambda \varepsilon \mu V_s E_c^2 / (\lambda \varepsilon \mu V_s E_c^2)_{si}$	**1**	**3.6**	**358**	**520**

[a] JFOM: Johnson's figure of merit, a measure of the ultimate high-frequency capability of the material.

[b] BFOM: Baliga's figure of merit, a measure of minimizing conduction losses in power FET's

[c] CFOM: Combined figure of merit for high temperature/high power/high frequency applications

Another advantage of GaN for power electronics is the easy realization of good ohmic contacts to n-GaN. Compared to a large number of other semiconductors, including Si, GaAs and SiC, the GaN surface Fermi energy is unpinned as indicated by the dependence of Schottky barrier height on the metallic work function. This is due to the ionic nature of GaN.[10] An unpinned surface Fermi energy facilitates the development of suitable ohmic contacts. Initial investigations of ohmic contacts to n-GaN were carried out by Foresi and Moustakas.[11] Contact resistances in the range of 10^{-4} to 10^{-3} Ω•cm^2 were achieved using a single metallization layer of Al or Au. Later, it was found that the addition of a Ti layer can significantly reduce the contact resistance. A low contact resistance value of 8×10^{-6} Ω•cm^2 was obtained by using a Ti/Al bi-layer contact annealed at 900C for 30 s.[12] The improvement with the additional Ti layer has been attributed to the N out-diffusion from the GaN lattice to form a TiN layer.[13] Since the N vacancies in GaN act as donors, the accumulation of N vacancies would create a heavily doped region near the contact layer-semiconductor junction, which facilitates electron tunneling. However, other researchers proposed that ohmic contact formation for Ti/Al contacts is not a result of the chemical reaction between GaN and Ti. Instead, these authors suggest that contact formation is due to the reduction of native gallium oxide formation by the presence of Ti and the diffusion of Al through the Ti to form a low work function Al-Ti intermetallic phase at the GaN surface.[14] In either case, the Ti/Al based metallization is by far the most widely used ohmic contact to n-GaN. Pre-metallization schemes can be employed to further reduce the ohmic contact resistance. Fan *et al*.[15] utilized reactive ion etching (RIE) treatment and multi-layer (Ti/Al/Ni/Au) metallization to achieve a very low contact resistance of 8.9×10^{-8} Ω•cm^2. The RIE treatment is believed to reduce the contact resistance by removing the surface oxide layer, roughening the GaN surface and creating more N vacancies to form a highly doped region at the GaN surface. Burm *et al.*[16] realized an ultra-low specific contact resistance of $3.6\times10^{-8}\ \Omega\bullet\text{cm}^2$ by implanting a high dose of Si ions followed by an activation anneal at 1150C for 30s before Ti/Au metallization. The ohmic contacts of such low specific resistances pave the way for developing power electronics devices based on n-GaN.

In spite of the encouraging material characteristics and the ease of forming n-ohmic contacts, the development of GaN power electronics lags behind Si and SiC. The primary reason is that a native substrate for device-quality material growth was not available, thus requiring heteroepitaxial growth on lattice mismatched substrates which naturally results in a substantial concentration of defects and a high unintentional n-type background doping level.[17]

The ideal solution to this issue will be the utilization of native bulk GaN substrates with low defect densities. Recent developments in Hydride Vapor Phase Epitaxy (HVPE) process have enabled the realization of bulk GaN substrates with defect densities over three orders of magnitude lower than the conventional GaN epilayer grown on sapphire substrates. The electronic devices fabricated with the low-defect-density bulk GaN substrate is believed to have improved performance over the conventional ones fabricated on GaN epilayer/sapphire structure. The low-defect-density bulk material also allows more accurate determination of some fundamental material properties.

In this dissertation, electronic devices, such as Schottky diodes, Schottky-type ultraviolet photodetectors and Metal-Oxide-Semiconductor capacitors, have been fabricated with the bulk GaN substrates and their electrical performance have been studied. Fundamental material property, such as Richardson constant, has been extracted based on a temperature-dependent Current-Voltage (I-V) measurement on Schottky diodes. The structure of this dissertation is outlined as follow.

A literature review on the problems associated with conventional Schottky diodes fabricated on GaN epilayer/Sapphire structure is presented in Chapter 2. The development of bulk GaN substrate and its superior material properties as compared to GaN epilayer grown on sapphire substrates are also introduced in this chapter.

The fabrication process and electrical characteristics of Schottky diodes fabricated on bulk GaN substrates are described in Chapter 3. The absence of the sapphire substrate allows the fabrication of vertical geometry devices with simplified processes. The devices exhibited excellent forward current conduction characteristics, high reverse breakdown voltages and ultrafast reverse recovery characteristics. The temperature-dependent I-V measurements were performed to extract the Richardson constant of GaN.

In Chapter 4, MEDICI simulation of a bulk GaN Schottky diode with a SiO_2 field plate edge termination scheme is presented. The purpose of this study is to predict the optimal edge termination parameters in order to reduce the field crowding at the Schottky contact edge and improve the reverse breakdown voltage of the bulk GaN Schottky diode.

Parameters, such as field plate thickness, Schottky metal overlap distances and oxide fixed charge density at the interface, are explored for optimal values.

Schottky-type ultraviolet photodetectors fabricated on a bulk GaN substrate is reported in Chapter 5. The wide band gap (3.4 eV) of GaN provides an intrinsic “Visible-blindness” for this ultraviolet photodetector. The low dislocation density of the bulk GaN substrate allows the fabrication of Schottky-type ultraviolet photodetector with extremely low dark currents and high UV/Visible rejection ratio. The photodetector also displayed a reasonably high responsivity and a good linearity of photocurrent with irradiance power density.

In Chapter 6, a systematic study of thermal oxidation of a bulk GaN substrate for Metal-Oxide-Semiconductor Capacitor fabrication is presented. Studies include oxidation rates and mechanism under different temperatures, material characterization and surface analysis, oxide etching process and electrical characterization of the MOS Capacitor using the thermally grown gallium oxide as an insulator. Despite a poor insulating nature of the thermal oxide, the thermal oxide/GaN interface displays a relatively low interface density of state compared to the deposited insulator/GaN interfaces reported in the literature.

A summary of this research is presented in Chapter 7. The future research direction is also pointed out in this chapter.

CHAPTER 2

LITERATURE REVIEW

Conventionally, GaN-based Schottky diodes have been fabricated on GaN thin films grown on foreign substrates, mostly sapphire or SiC, using hydride vapor phase epitaxy (HVPE)[18] or metal organic chemical vapor deposition (MOCVD).[19, 20] A very high reverse breakdown voltage (V_B) of 6350 V was achieved with Schottky diodes fabricated on resistive GaN films, which is a record for GaN Schottky diode.[21] However, the forward turn-on voltage (V_F) and on-state resistance (R_{on}) were as high as 15 V and 0.15 Ω•cm^2, respectively, which limited the forward current conduction. Schottky diodes fabricated on conducting GaN films typically have a V_B in the range of 280-550 V, a V_F in the range of 3-5 V at the current density of 100 A/cm^2, and an R_{on} of around 6-23 mΩ•cm^2. These results demonstrate the potential of GaN Schottky diodes for high power applications.

However, there are several drawbacks for heteroepitaxial GaN Schottky diodes. First, due to the large lattice mismatch (~13%) and thermal expansion coefficient mismatch (~34%), GaN films grown on sapphire substrates contain high dislocation densities, typically in the range of 10^8-10^{10} cm^{-2}.[22] SiC has smaller lattice and thermal expansion coefficient mismatch with GaN, however, heteroepitaxial growth of GaN on SiC is less studied due to the high cost of the SiC bulk substrates and the fact that only a limited reduction in dislocation density relative to sapphire is achievable. It is well-known that dislocations behave as non-radiative recombination centers in GaAs, GaP and ZnSe based semiconductors. Even a moderate dislocation density can diminish the bulk luminescent efficiency in GaAs or GaP LEDs.[23, 24] Nevertheless, GaN LEDs with high efficiency have been fabricated despite a high dislocation density.[25] The exact reason why such a high dislocation density is tolerated in GaN-based optoelectronic devices is still unclear. Early work to explain to this phenomenon suggested that the threading dislocations in GaN do not have electronic states in the band gap. Theoretical calculations by Elsner *et al.*[26] proposed that screw dislocations with open cores and edge dislocation with filled cores are energetically preferable and both dislocations are electrically inactive with a band gap free of deep levels. Recently however, direct observation through transmission electron microscopy (TEM) has revealed filled cores for screw dislocations.[27] A subsequent calculation based on a Ga-filled core for screw dislocations pointed to the existence of electronic states in the band gap. Therefore, screw dislocations are expected to be centers for nonradiative recombination and pathways for current leakage.[28] Indeed, numerous experimental studies have revealed a strong correlation between reverse leakage current and the density of pure screw dislocations.[29-32] Even though pure edge dislocations do not seem to form leakage paths in GaN-based Schottky diodes,[33] they do, however, have a major impact on the electron mobility in GaN. Weimann *et al.*[34] proposed that threading edge dislocations introduce acceptor centers along the dislocation line. These centers capture electrons, and the negatively charged dislocation lines scatter other electrons traveling across them and thus reduce the mobility. This dislocation-related scattering mechanism becomes dominant at low carrier concentrations. In the case of high carrier concentration, its effect is screened by free carriers, and scattering by ionized impurities becomes dominant. The validity of this model was supported by an investigation of the temperature dependence of the n-GaN film's transport coefficients.[35] Later, a more rigorous model was proposed, showing that threading edge dislocations in GaN can indeed directly affect the electron mobility.[36] These models are supported by a scanning capacitance microscopy study which showed evidence for the presence of negative charges in the vicinity of dislocations.[37] Dislocation-related mobility reduction and localized current blocking were also observed experimentally.[38, 39] Additionally, threading dislocations in GaN have been identified as non-radiative recombination centers based on a cathodoluminescence measurement.[40] Therefore, dislocations in GaN are indeed electrically active and play a detrimental role for the reverse leakage current and electron mobility in GaN Schottky diodes. It is very unlikely that the promise of GaN for power electronics can be realized without a significant reduction in dislocation densities.

The lateral epitaxial overgrowth (LEO) technique was developed with the goal of improving the quality of the heteroepitaxially grown GaN films by enforcing lateral growth of GaN films over the masked area with reduced dislocation density.[41] However, this method requires multi-step processes and is not suitable for large area growth.

Secondly, with the GaN/sapphire structure, fabrication of vertical Schottky diodes is difficult due to the insulating nature of sapphire. Vertical devices are preferred because the vertical geometry can provide a more uniform electric field distribution and higher electron mobility. In the dislocation-related scattering model proposed by Weimann *et al.*[34], electron scattering by dislocation lines depends critically on the angle between the direction of the electron transport and the orientation of the dislocation lines. Vertical devices are expected to be less affected by the scattering of electrons at threading dislocation lines since the current conduction is parallel to the line direction. Indeed, Misra *et al.*[42] has shown that vertical mobility in GaN Schottky diodes is about 6 times higher than the lateral mobility, which was attributed to the reduction in scattering by charged dislocations. Katz *et al.*[43] recently observed a lower noise level for a vertical GaN Schottky UV photodetector, which is also attributed to the reduced effect of dislocations on carrier transport. An ideal vertical device should have a full area ohmic contact on one side of the substrate and Schottky contacts on the other side. Using this structure, device processing, cleavage and packaging are greatly simplified. Quasi-vertical Schottky diodes can be fabricated on GaN/sapphire structures using mesa etching technique. However, this complicates the fabrication process, and defects induced by etching process often lead to surface leakage currents.

Finally, the forward current conduction of a Schottky diode is significantly limited due to the low thermal conductivity (0.5 W/cm•K) of the sapphire substrates. It is well-known that efficient dissipation of heat is essential to the performance of high power electronic devices.

The drawbacks discussed above for heteroepitaxial diodes point to the necessity for vertical geometry devices fabricated with high quality films grown, preferably on bulk native substrates with low dislocation densities. Bulk GaN crystals have been successfully synthesized by a high pressure, high temperature process proposed by Porowski *et al.*[44] Even though the crystals were reported to be practically free of extended defects, the limitations of small area and the long growth time will likely inhibit commercialization of this process.

Recently, another process, hydride vapor phase epitaxy (HVPE) has received much attention. High growth rates (~1 μm/min) and the near-equilibrium nature of this process facilitate the growth of thick GaN layers with low defect densities, which can be processed to produce a bulk GaN substrate for homoepitaxial growth and device fabrication.[45] The current HVPE growth of GaN films is generally carried out on sapphire substrates with ZnO or GaCl pre-growth treatments.[46, 47] Even though a highly dislocated thin layer is still generated at the layer/substrate interface due to the large lattice mismatch between GaN and sapphire substrate,[48] the film quality improves significantly as it grows thicker, possibly due to defect interaction and subsequent dislocation annihilation.[49] Reynolds *et al*.[50] has reported a reduction of surface strain with increasing GaN film thickness, and the authors estimated that the surface strain would be fully relaxed at the thickness near 75 µm. The types and concentrations of deep levels, as well as the dislocation density, were found to decrease significantly with the increasing film thickness.[51] The reduction of the threading dislocation with film thickness also leads to a higher electron mobility and longer carrier diffusion length at the uppermost GaN film.[52, 53] Thus, the successful growth of thick, high quality GaN films using the HVPE process offers the possibility of freestanding GaN substrates for homoepitaxial growth and subsequent device fabrication.

Following the growth of thick GaN films (typically ~300 µm) using the HVPE process, the removal of the sapphire substrate is necessary in order to obtain freestanding GaN wafers. Several techniques of separating GaN film from the sapphire substrate have been reported. Nakamura *et al*.[54] obtained freestanding GaN wafers by mechanically polishing the sapphire substrate away. Kelly *et al*.[55] used a laser-induced liftoff technique to separate thick GaN films from the sapphire substrates. This technique takes advantage of the fact that the interface between the GaN film and the sapphire can be thermally decomposed with illumination from an intense laser pulse of the correct wavelength. Using this approach, large area freestanding GaN wafers can be separated from sapphire substrates without the need for mechanical polishing. Oshima *et al*.[56] developed a wafer separation technique with the aid of a thin TiN film formed on top of the growth template. As the sample cools after HVPE growth, the thick GaN layer can be easily separated from the sapphire substrate through the assistance of many voids generated around the TiN film.

A freestanding wafer will normally have its N-terminated face in contact with the sapphire substrate side, as indicated by the convergent beam electron diffraction (CBED) analysis.[57] Both the Ga and N-terminated faces can be mechanically polished. The Ga-face can be further chemical-mechanical polished (CMP) or dry etched to remove the mechanical polishing-induced surface damage, in order to obtain an epi-ready surface for homoepitaxy or bulk device fabrication. Owing to the continuous optimization in material growth conditions, freestanding GaN substrates have demonstrated excellent material quality in terms of electrical, optical and structural properties. Numbers of the improvements in the material properties of the freestanding GaN wafers over conventional thin heteroepilayers are listed in Table 2.1. Many of the parameters listed are from references.[58-65] The significant reduction in dislocation density (over three orders of magnitude) leads to a remarkable increase in electron mobility, which is a great in power electronic applications. Such a low dislocation density ($<5\times10^{6}$ cm^{-2}) is also desirable in order to achieve low reverse leakage currents in Schottky diodes. Electronic devices fabricated on the low-defect-density bulk GaN substrates are expected to have a much simpler fabrication process and to demonstrate improved performance over those on conventional GaN epilayer/Sapphire structure. However, so far, little research has been done on the electronic devices fabricated with bulk GaN substrates yet.

Table 2.1. Material properties comparison of unintentionally-doped bulk GaN wafer and thin GaN epilayer

	bulk GaN wafer	**thin GaN epilayer**
Dislocation density (cm^{-2})	**5×10^5-5×10^6**	**10^8-10^{10}**
Compensation ratio (N_A/N_D)	**0.14-0.23**	**0.3**
300K Electron mobility ($cm^2/V\cdot s$)	**1100-1245**	**300-1191**
Peak Electron mobility ($cm^2/V\cdot s$)	**8000**	**3000**

CHAPTER 3

SCHOTTKY DIODE FABRICATED ON A BULK GALLIUM NITRIDE SUBSTRATE

3.1 Introduction

Gallium nitride (GaN) is one of the most promising materials for the fabrication of high power, high frequency and high temperature devices due to its superior characteristics such as a large bandgap (3.4 eV), a high electron saturation velocity (3×10^7 cm/s) and a high breakdown field (4 MV/cm). Both Schottky diodes and p-n junction diodes can be employed in power rectifier applications. In the case of the bipolar p-n junction diode, minority carriers can be stored when the diode is forward biased, and a large transient reverse current is required to extract these carriers when the device is switched. Due to its unipolar nature, a Schottky diode does not exhibit the minority carrier storage effect, and thus shows a negligible reverse current transient. Therefore, faster switching can be achieved with Schottky diodes compared to p-n junction diodes. As a majority carrier device, GaN Schottky rectifier is expected to have a high switching speed and a low reverse recovery current as well as remaining a high reverse blocking voltage.

Due to the poor availability of bulk GaN substrates, GaN-based Schottky rectifiers have been fabricated using GaN films epitaxially grown on foreign substrates such as sapphire. Zhang *et al.*[21] has reported a record V_B value of 6350 V for Schottky rectifiers fabricated laterally on resistive GaN epitaxial layer grown on sapphire. The figure-of-merit $(V_B)^2/R_{on}$ of these devices are as high as 268 MW•cm^{-2}, which is a record for GaN Schottky rectifiers. Although an excellent reverse breakdown voltage has been achieved, its application is limited due to some inevitable drawbacks as pointed out in Chapter 2. In order to achieve higher currents without compromising the reverse breakdown voltages, vertical geometry Schottky diodes fabricated on conducting GaN films with a low density of defects are desirable. The ideal solution to this scheme is to utilize a low-defect-density bulk GaN substrate. Thanks to the recent development in the Hydride Vapor Phase Epitaxy (HVPE) process, bulk GaN substrates with a low dislocation density ($<5\times10^6$ cm^{-2}) start to come into commercialization. Recently, there have been few initial reports on the fabrication and operation of vertical geometry Schottky diodes utilizing bulk GaN substrates.[66-68] In all cases, ohmic contacts are formed by depositing broad area Ti/Al on the N-face of the substrate with subsequent annealing in N_2 at around 800 C for a short time (~30 seconds). Metals with high work functions (Pt, Au and Ni) are frequently deposited as Schottky contacts on the Ga-face.

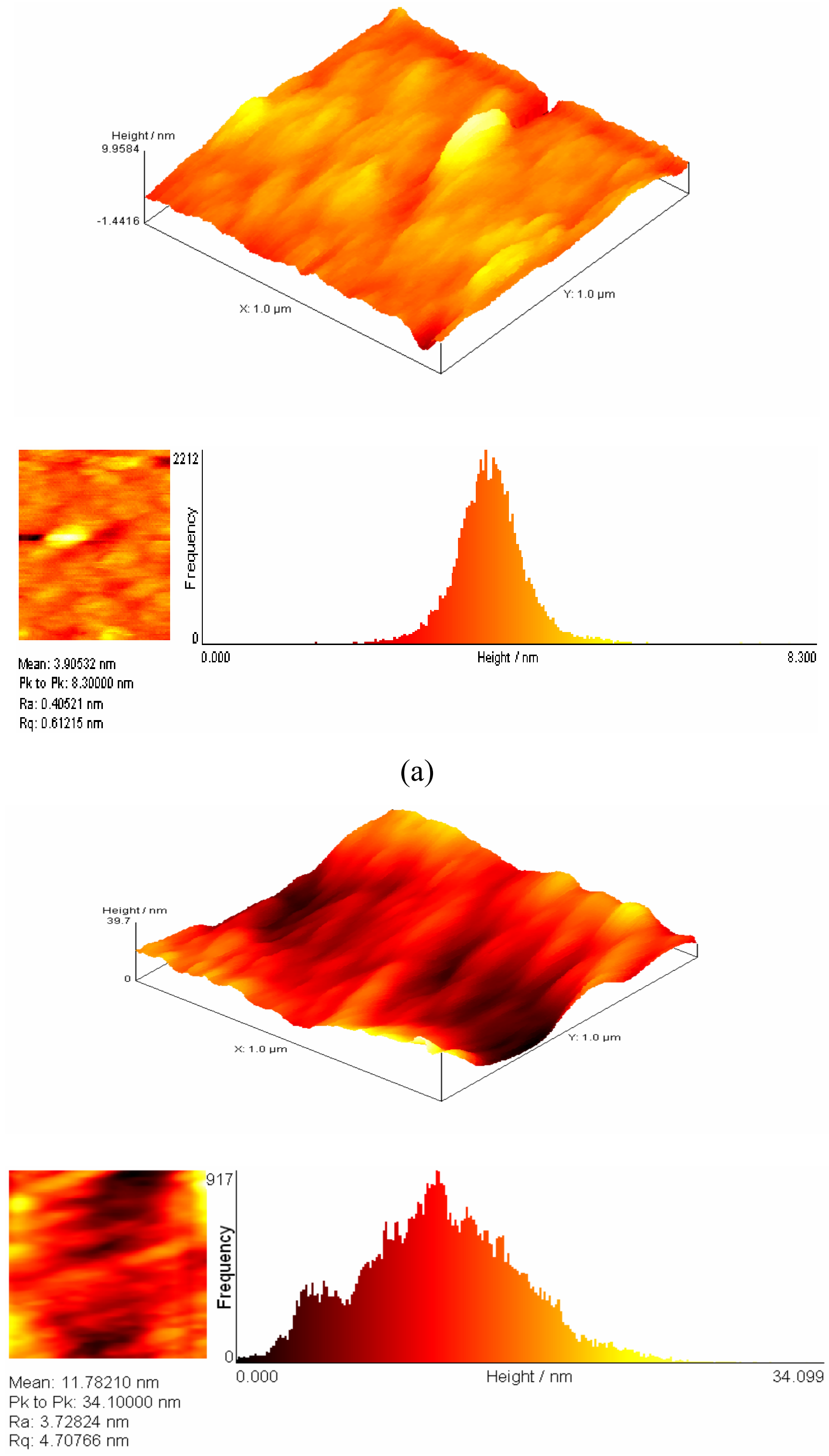
The N-face of the substrate is preferred for ohmic contact formation for the following reasons. First, the highly defective layer at the surface of the substrate provides electron tunneling paths to achieve better ohmicity. Second, the Schottky barrier height formed on the N-face is much lower than that formed on Ga-face.[69] Third, the N-face is more chemically active than the Ga-face, which facilitates N gettering by the Ti layer and the formation of a highly conductive region to promote electron tunneling. The full area ohmic contact on the backside (i.e., N-terminated) surface also eliminates the photolithography steps that are required for ohmic contacts on GaN/sapphire structure.

The improved ohmic contact scheme and the absence of the sapphire substrate have enhanced the high current capabilities of the vertical geometry Schottky diodes fabricated on freestanding GaN substrates. Ip *et al.*[70] have reported a record high forward current value of 1.72 A at 6.28 V under pulsed conditions for a 7 mm diameter rectifier fabricated on a freestanding GaN substrate. Even though the reverse breakdown voltage for this device is low, the ability of GaN Schottky diodes to conduct high current has been demonstrated for the first time. By interconnecting the output of many smaller rectifiers, the forward current as high as 161 A has been achieved while maintaining the reverse breakdown voltage.[71] The high current conduction achieved with the bulk GaN substrate represents an important step towards the realization of diodes for high power switching applications.

In this work, we have successfully fabricated vertical geometry Schottky diodes on a bulk GaN substrate with a record low on-state resistance (0.88 m$\Omega \bullet cm^2$) and a record short reverse recovery time (<20 ns). Without any edge termination schemes and subsequent epilayer growth on bulk GaN substrates, high reverse breakdown voltages (>600 V) have been achieved and high current conduction capability has been demonstrated. The excellent device performance was mainly attributed to the high material quality of the bulk substrate. A temperature-dependent I-V measurement was performed to extract the Richardson constant of GaN.

3.2 Bulk GaN substrate characterization

Figure 3.1 shows the Atomic-Force-Microscopy (AFM) images of (a) Ga-face and (b) N-face of the bulk GaN substrate, respectively. The AFM images were taken by Dr. Dake Wang. The Ga-face of the substrate was polished and the root-mean-square roughness was determined to be 0.61 nm. The N-face was not polished, and the root-mean-square roughness was 4.7 nm.



(a)

(b)

Figure 3.1: AFM images of Ga-face (a) and N-face (b) of the bulk GaN substrate.

The x-ray rocking curves from (a) (002) (b) (102) planes of the bulk GaN substrate are taken by Kyma Technologies, Inc and shown in Figure 3.2. The typical values for the Full-Width-at-Half-Maximum (FWHM) of the (002) rocking curves for thin GaN films grown on sapphire substrates via HVPE process have been reported in the range of 200-600 arcsec.[72-74] The FWHM value of the (002) rocking curves for the bulk GaN substrate was determined to be 90 arcsec, indicating the state-of-the-art quality of the material. It was found that lattice distortion from screw type dislocations would contribute to the broadening of the (002) x-ray rocking curve peak and distortion from edge dislocation would contribute to broadening of the (102) peak.[75] Some groups have reported the (002) rocking curves as narrow as 30-40 arcsec for GaN films grown by MOCVD process.[75-77] This is possibly due to the fact that most of the threading dislocations in the GaN film grown by MOCVD process are pure edge dislocations and these edge dislocations do not contribute to the broadening of the (002) rocking curve. Indeed, the FWHM value of the (102) rocking curve for these samples can be as high as 740 arcsec, indicating the presence of a high density of edge dislocations.[75] The FWHM value of the (102) rocking curve for the bulk GaN substrate is as low as 118 arcsec. The narrower x-ray rocking curve linewidths of the bulk GaN substrate are attributed to the overall lower dislocation density of the substrate.

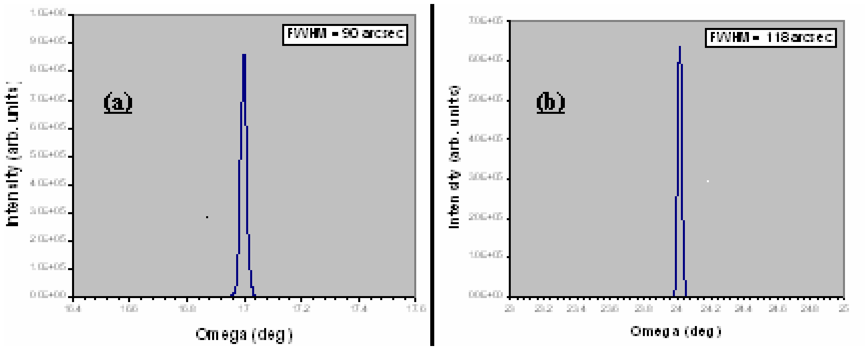


Figure 3.2: x-ray rocking curves for (a) (002) and (b) (102) planes of the bulk GaN substrate.

Figure 3.3 shows the Raman spectrum of the bulk GaN substrate. The Raman spectroscopy was carried out at room temperature using a backscattering geometry. The wavelength of 441.6 nm line of the Kimmon Electric’s He-Cd laser was used as an excitation. The Jobin-Yvon’s spectrometer with a thermoelectrically-cooled charge coupled device (CCD) detector was used to collect the Stokes’ and anti-Stokes’ Raman spectra. The group theory predicts two A_1, two E_1, two E_2 and two B_1 modes for GaN with a hexagonal wurtzite structure.[78] Among them, one A_1, one E_1 and two E_2 modes are Raman active. According to the Raman selection rules, only the E_2 and A_1(longitudinal optical) modes can be observed with the z(-,-)$\underline{z}$ scattering geometry. Our experimental data agrees well with the theoretical prediction, with only E_2 and A_1(LO) modes visible. The peak position and the FWHM of the E_2 mode were determined to be 568.2 cm^{-1} and 5.09 cm^{-1}, respectively, by fitting the Raman peak with Lorentzian functions. The position of E_2 mode was found to be closely related to the biaxial stress in the GaN, with an up-shift corresponding to the compressive stress and a down-shift corresponding to the tensile stress.[79] The bulk GaN substrates are frequently used as a stress-free reference to other GaN films or nanorods.[80] The line shape analysis of the A_1(LO) peak based on the LO phonon-plasmon coupling phenomenon are often employed to extract the free electron concentration and electron mobility of the GaN.[81, 82] This technique is unique and attractive because of its non-contact, non-destructive nature. However, the lowest free electron concentration which can be accurately determined by this method is 3×10^{16} cm^{-3}.[83] The A_1(LO) peak was found to shift towards the high frequency side and broaden with increasing carrier concentration.[78] Our bulk GaN substrate has a low free electron concentration ($<3\times10^{16}$ cm^{-3}) as evidenced by the position (735.6 cm^{-1}) and FWHM (8.25 cm^{-1}) of the A_1(LO) peak.

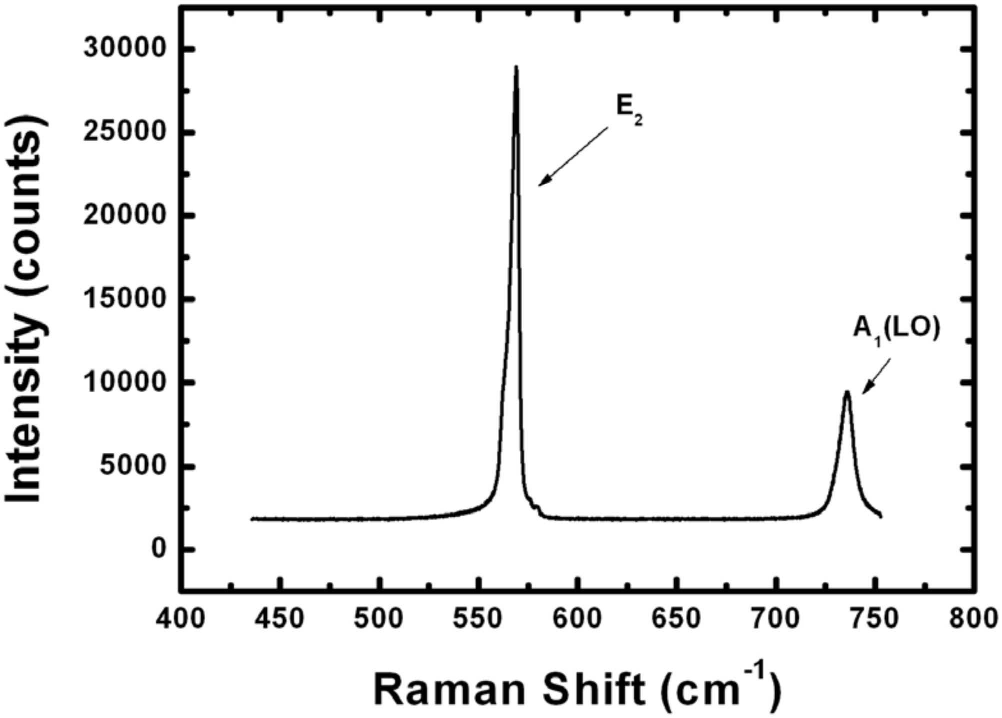


Figure 3.3: Raman spectrum of the bulk GaN substrate.

Figure 3.4 shows the photoluminescence (PL) spectrum of the bulk GaN substrate. The spectrum was collected by Dr. Dake Wang. The experiment was performed at room temperature on the Ga-face of the substrate using a 325 nm line of the He-Cd laser as an excitation. The spectrum was collected using a Jobin-Yvon's spectrometer equipped with a thermoelectrically cooled CCD. The full-width-at-half-maximum (FWHM) of the near band-edge PL peak is ~80 meV, which is indicative of high quality material.[77] A broad yellow-green luminescence centered around 2.3-2.4 eV is observed. This defect-related luminescence appears to be a universal feature for both bulk GaN crystallites and GaN epitaxial layers, regardless of growth techniques.[84] The origin of this luminescence has brought up a hot debate. Now most investigators agree that it is caused by transition from the conduction band or a shallow donor to a deep acceptor, which is most probably a gallium vacancy or a gallium vacancy-oxygen complex.[85-87]

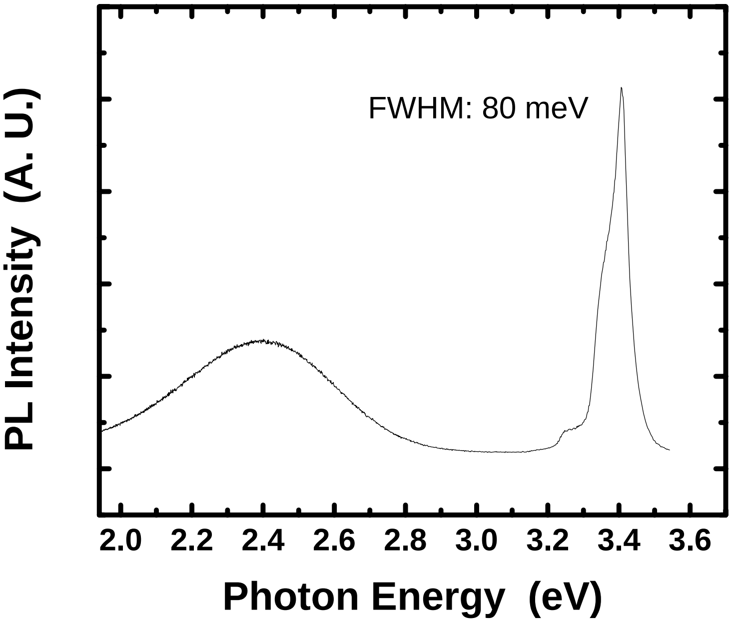


Figure 3.4: Photoluminescence spectrum of the bulk GaN wafer

3.3 Experiment

The bulk GaN substrates were provided by Kyma Technology, Inc. The as-received samples were 10×10 mm^2 in dimension and ~460 μm thick. The capacitance-voltage (C-V) measurements showed unintentional n-doping levels range from 5×10^{15} cm^{-3} to 2×10^{16} cm^{-3} for different samples. The Ga- side (front side) of the substrate was polished, while the N- side (back side) had a rough surface. The 10×10 mm^2 samples were further cut into smaller pieces (typically 3×3 mm^2) using a diamond scribe for device fabrication and characterization.

The basic fabrication processes are described as follows. Before metallization, the substrates were ultrasonically cleaned sequentially in acetone, trichloroethylene, acetone, and methanol for 5 minutes each, followed by immersion in a heated HCl: H_2O (1:1) (~100 °C) for 10 minutes, rinsing well in deionized water and blowing dry using N_2. After cleaning, a full backside ohmic contact of Ti (50 nm)/Al (100 nm) was deposited by a direct-current (DC) magnetron sputtering in Ar ambient followed by rapid thermal annealing at ~850 °C in N_2 atmosphere for ~ 1 minute. Then, the Pt (250 nm) Schottky contacts with different diameters were deposited on the Ga- side of the substrate by DC magnetron sputtering, patterned by standard photolithography liftoff and then annealed in N_2 atmosphere at ~500 °C for 30 seconds to improve adhesion between Pt film and the GaN substrate. The schematics of the device are depicted in Figure 3.5.

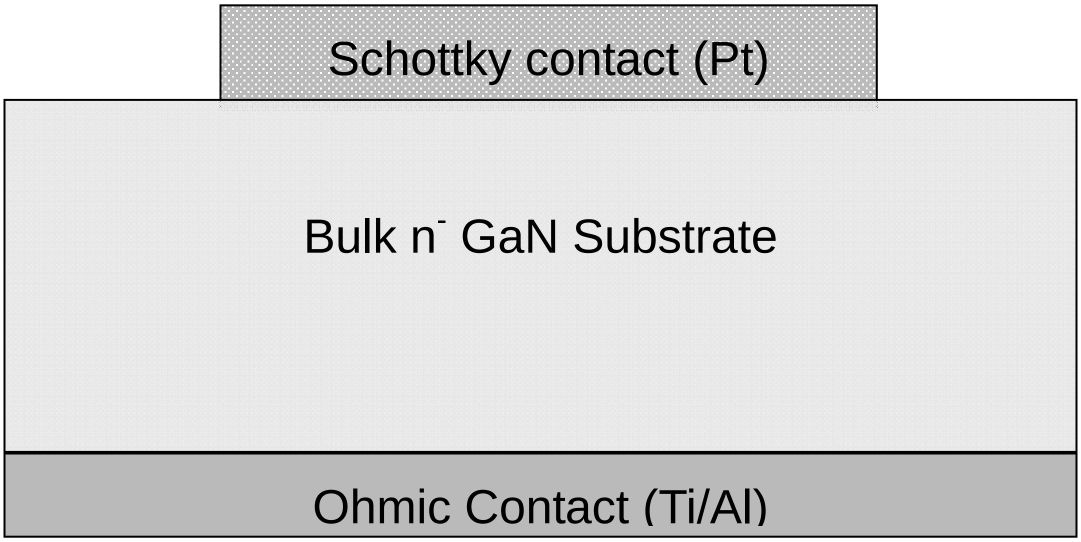


Figure 3.5: Schematics of the GaN Schottky diode fabricated.

The Low-field I-V measurements were performed using a Keithley 6487 picoammeter or a Keithley 6517 electrometer with its built-in power supply. High-field I-V measurements were carried out using a Tektronix 471 curve-tracer. Capacitance-voltage (CV) measurements were performed at 100 kHz using a Keithley simultaneous hi-lo C-V system. Reverse recovery characteristics were studied using an Astable switching circuit that applied voltages from 9 to -9 V with a maximum current of 50 mA to the device. A 50 Ω resistor was used to measure the current and terminate the 50 Ω coaxial line in the measurement system.

3.4 Result and discussion

Figure 3.6 shows a typical room temperature low field I-V characteristics of a 50 μm diameter Schottky diode fabricated on a bulk GaN substrate with a unintentional n-doping level of 2×10^{16} cm^{-3}. By fitting the curve into the thermionic emission over a barrier,

$$J_F = J_s \cdot \exp(\frac{eV}{nkT}); \tag{3.1}$$

$$J_s = A^* \cdot T^2 \cdot \exp(-\frac{\Phi_b}{kT}); \tag{3.2}$$

where J_F is the forward current density, J_s is the saturation current density, e is electron charge, V is the applied voltage, n is the ideality factor, k is the Boltzman constant, T is the temperature, A^* is the Richardson constant for n-GaN (assumed to be 26.4 Acm^{-2}K^{-2}), and Φ_b is the barrier height, the Schottky barrier height was found to be 1.0 eV with an ideality factor of 1.06, indicating a very good Schottky contact. The reverse leakage current was below 1 pA up to -30 V bias. Defining V_F as the bias voltage at which the forward current density is 100 A/cm^2, a typical V_F was found to be 1 V for the 50 μm diameter rectifiers with the on-state resistance (R_{on}) to be 1.84 mΩ•cm^2. The low forward turn-on voltage and on-state resistance are attributed to the unique ohmic contact scheme compatible with the bulk GaN substrate and the higher electron mobility in vertical transport mode due to the reduction of scattering by dislocations.

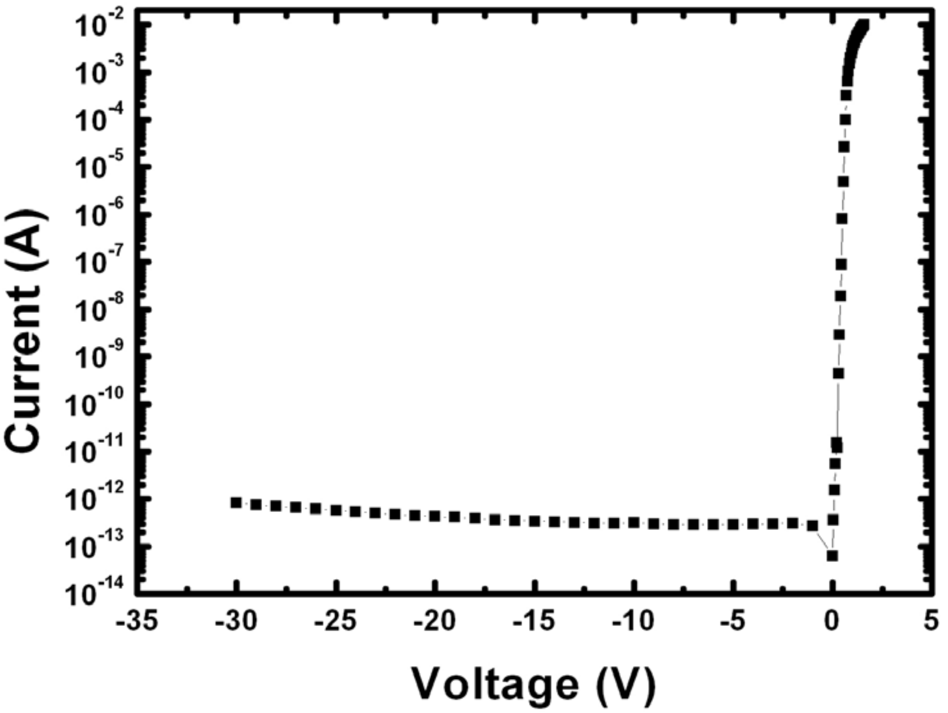


Figure 3.6: Low field I-V characteristics of a 50 μm diameter Schottky diode fabricated on a bulk GaN substrate with an unintentional n-doping of 2×10^{16} cm^{-3}.

Even though the forward turn-on voltage and on-state resistance of bulk GaN Schottky diodes are already significantly lower than those fabricated on GaN epilayer on Sapphire substrates, it will be interesting to apply the ohmic contact enhancement schemes such as Reactive Ion Etching (RIE) and Si implant, which have been conventionally employed in the Schottky diode fabrication on GaN epilayer/Sapphire structure, to bulk GaN Schottky diodes to see whether there is any further improvement in forward current conduction. Therefore, another two samples were cut from the same substrate and Schottky diodes were prepared using different ohmic contact enhancement schemes. Before ohmic contact deposition, one sample was implanted with a high dose of Si ions on the whole area of the N-face side followed by activation at 1000 C in N_2 atmosphere for 2 minutes; the other sample was treated with Reactive Ion Etching (RIE) on the N-face side using Cl_2/Ar discharge. The Si implants profile was simulated using SRIM software, as shown in Figure 3.7. The implantation was carried out at three different implantation energies (100 keV, 200 keV and 360 keV) with different doses (2×10^{14} cm^{-2}, 4×10^{14} cm^{-2} and 8×10^{14} cm^{-2}), aiming to produce a box profile with the Si concentration of ~4×10^{19} cm^{-3} and a depth of ~0.3 μm into the backside of the substrate. In order to bring the implants peak position to the substrate surface, a Molybdenum layer (100 nm) was deposited at the backside as the implantation mask. This layer was removed after implantation using H_2O_2. RIE was performed using a homebuilt plasma processing system, equipped with a 13.65 MHz RF power supply RFX-600 (Advanced Energy) and an impedance matching unit ATX-600 (Advanced Energy). The plasma chemistry used was Cl_2/Ar mixture with a ratio of 1:2. The etch pressure was ~80 mTorr and the etch power was 50 W. The sample's backside was etched for 5 minutes.

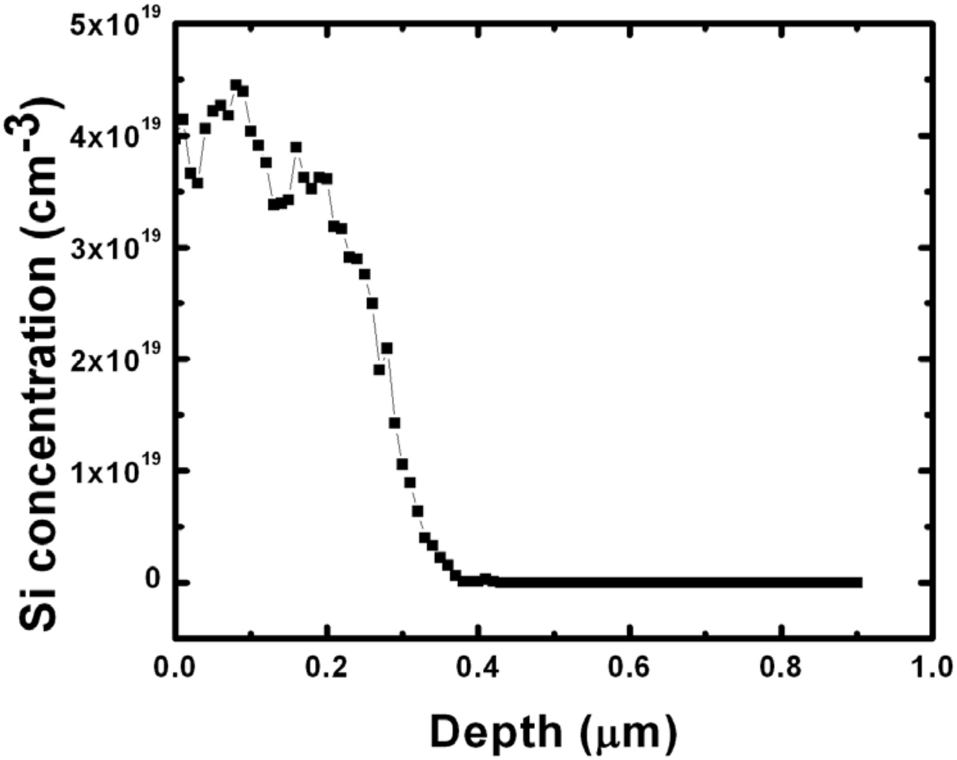


Figure 3.7: Si implants profile simulated by SRIM software

Figure 3.8 shows the forward Current-Voltage characteristics of the vertical geometry Schottky diodes fabricated on bulk GaN substrates with or without ohmic contact enhancement schemes. High dose Si implants creates a highly conductive layer at the surface of the substrate. And this layer can facilitate electron tunneling to achieve better ohmicity. Schottky diode fabricated with this ohmic contact enhancement scheme has a lower forward turn-on voltage of 0.85 V and on-state resistance of 0.88 mΩ•cm^2. To our best knowledge, this is the lowest reported on-state resistance value for GaN Schottky diodes. However, the Schottky diode with RIE treatment on the N-side has an even higher on-state resistance than that without any ohmic contact enhancement scheme. The reason is that instead of generating a more conductive region by creating more N vacancies, the RIE process etched away the highly defective layer at the surface of the N-side of the substrate. And this highly defective layer is essential to the ohmic contact formation for vertical Schottky diodes on bulk GaN substrates. Therefore, RIE ohmic contact enhancement scheme is not applicable to Schottky diodes fabricated on bulk GaN substrate due to the unique structure of the substrate.

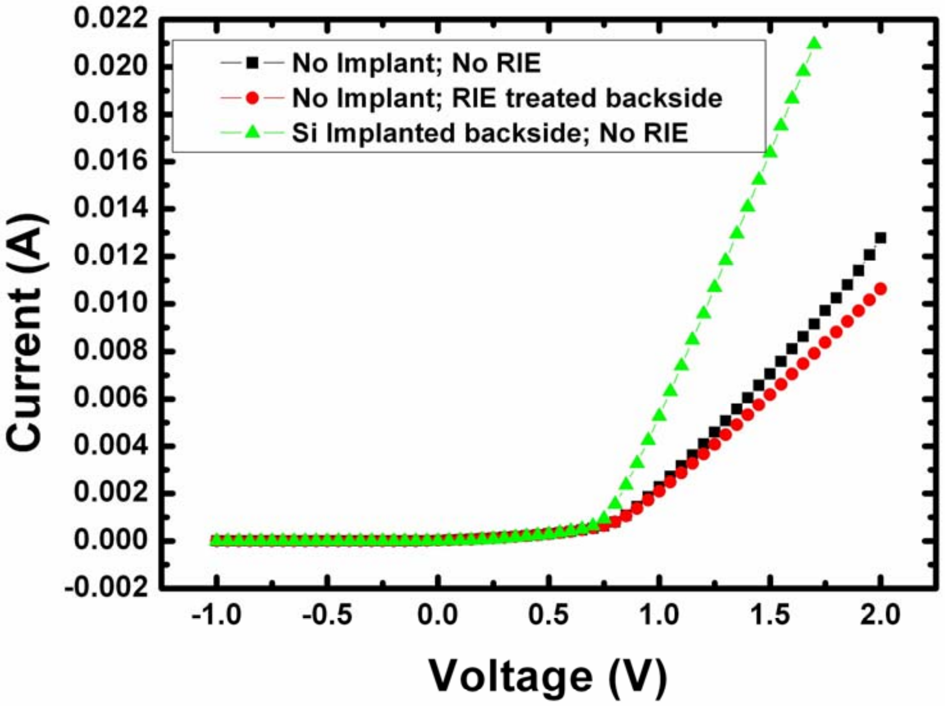


Figure 3.8: Forward I-V characteristics of vertical bulk GaN Schottky diodes with or without ohmic contact enhancement schemes.

Care must be taken as for the activation temperature following the Si implantation. It is well-known that GaN is thermally unstable at temperature above 1000 °C.[88] Dissociation of nitrogen from the GaN surface is found to occur at high temperatures. In our experiment trials, after an activation annealing at 1150 C for 2 minutes, the GaN showed severe surface pitting due to the nitrogen loss. The nitrogen loss is expected to create an n^+ region at the GaN surface which accounts for the high leakage currents and low reverse breakdown voltages of the Schottky diodes fabricated on it. For samples annealed at 1000 C for 2 minutes, the surface is still mirror-like and the reverse I-V characteristics were the same as samples without annealing, which means rapid thermal annealing at 1000 C is a safe processing procedure for Schottky diodes fabricated with our bulk GaN substrate.

The reverse breakdown voltage of the bulk GaN Schottky diodes differs from sample to sample. Our best result is shown in Figure 3.9. These devices were fabricated on a bulk GaN substrate with an unintentionally n-doping level of 7×10^{15} cm^{-3}. The V_B was arbitrarily defined as the voltage at which the reverse current reached 1 mA. High reverse breakdown voltages were achieved with small diameter rectifiers, including a V_B of 630 V for 50 μm diameter rectifiers and 600 V for 150 μm diameter rectifiers. For larger diameter (300 μm) rectifiers, the good device yield dropped significantly, and the V_B decreased to 260 V. Up to date, all reported GaN Schottky diodes displayed premature breakdown characteristics which are attributed to the defects within the device active area, especially at the contact periphery.[68] So one would expect a decrease of V_B with increasing device diameter. Our experimental data comply with this general trend, however a linear relation was not found possibly due to a non-uniform distribution of defects. The >600 V reverse breakdown voltage is among the highest reported value for Schottky diodes fabricated on conducting GaN films. We achieved such a high breakdown voltage without any epitaxial films or edge termination schemes, indicating a very good material quality of the bulk GaN substrate.

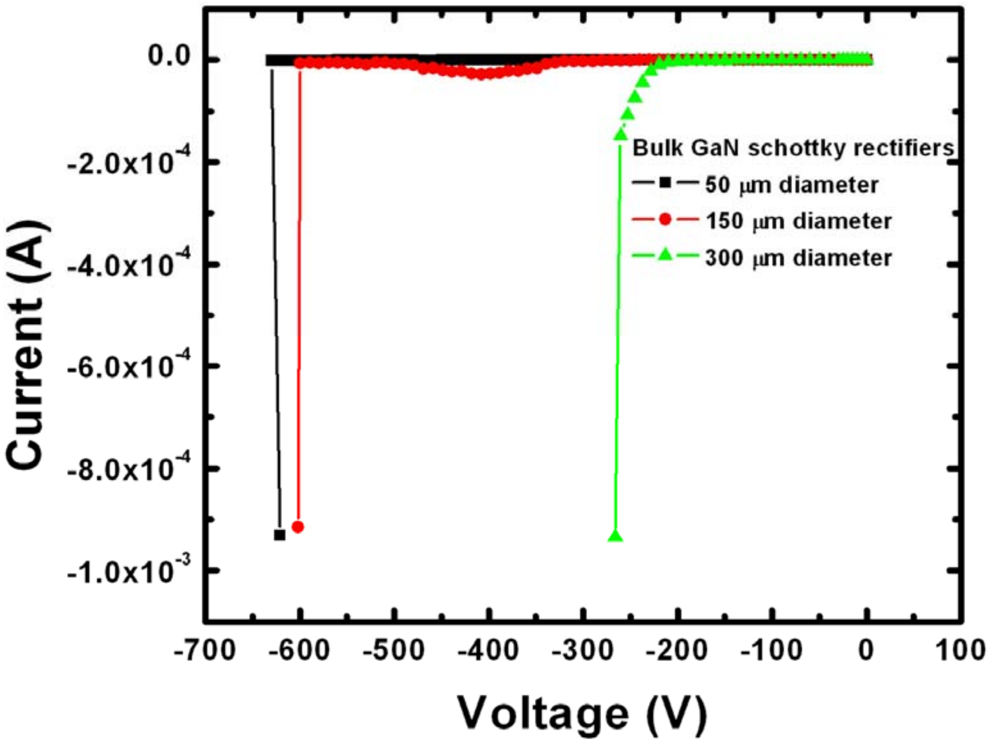


Figure 3.9: Reverse breakdown voltages for bulk GaN rectifiers of different diameters

Figure 3.10 shows the room temperature high field I-V characteristics of the 150 μm and 300 μm diameter Schottky diodes described above. At the bias of 10V, the forward currents reached 0.5 A and 0.8 A for 150 μm and 300 μm diameter rectifiers, corresponding to a current density of 2830 A/cm^2 and 1130 A/cm^2, respectively. The measurements were repeated several times and no device degradation was found, which means the GaN bulk substrate can effectively dissipate heat to avoid over self-heating at such high current density levels. There are a number of reports of mesa and lateral GaN Schottky rectifiers fabricated on heteroepitaxial layers on sapphire substrates. Compared to bulk GaN substrates, the major disadvantage of the sapphire substrates is the poor thermal conductivity (0.5 W/cm•K) which restricts the high current conduction. The typically cited value (1.3 W/cm•K) of the thermal conductivity for GaN is actually a lower limit. Recent experimental study has shown that a higher thermal conductivity of 2.3 W/cm•K was measured on a high quality, low dislocation density bulk GaN substrate.[6] And this value is expected to increase with the perfection of material growth technique. The elimination of the sapphire substrate and the improved thermal conductivity of the low-defect-density bulk GaN substrate, together with the vertical device geometry, essentially enable much higher current conduction than lateral geometry diodes fabricated on insulating substrates.

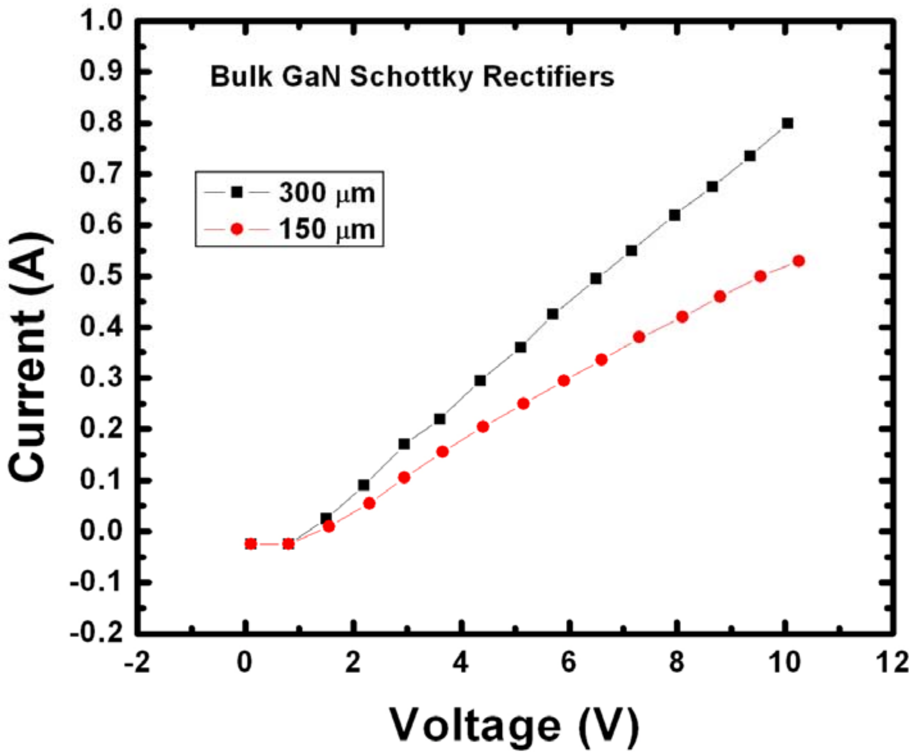


Figure 3.10: High field I-V characteristics of the 150 µm and 300 µm diameter bulk GaN Schottky diodes

The reverse recovery characteristics of a 50 µm diameter bulk GaN Schottky diode is shown in Figure 3.11. The device exhibited ultrafast reverse recovery characteristics, with the reverse recovery time shorter than 20 ns when switching from forward bias to reverse bias. Similar reverse recovery characteristics were also found for 150 µm and 300 µm diameter diodes. To our best knowledge, this is the shortest reverse recovery time reported for GaN Schottky diodes. A reverse recovery time of ~ 200 ns was reported for GaN Schottky diodes fabricated on GaN epilayer/sapphire structure.[19] The ultrafast reverse recovery characteristics are mainly attributed to the low dislocation density of the bulk GaN substrate, which effectively reduces the electron scattering at the dislocation lines. And this device looks very promising for high frequency applications.

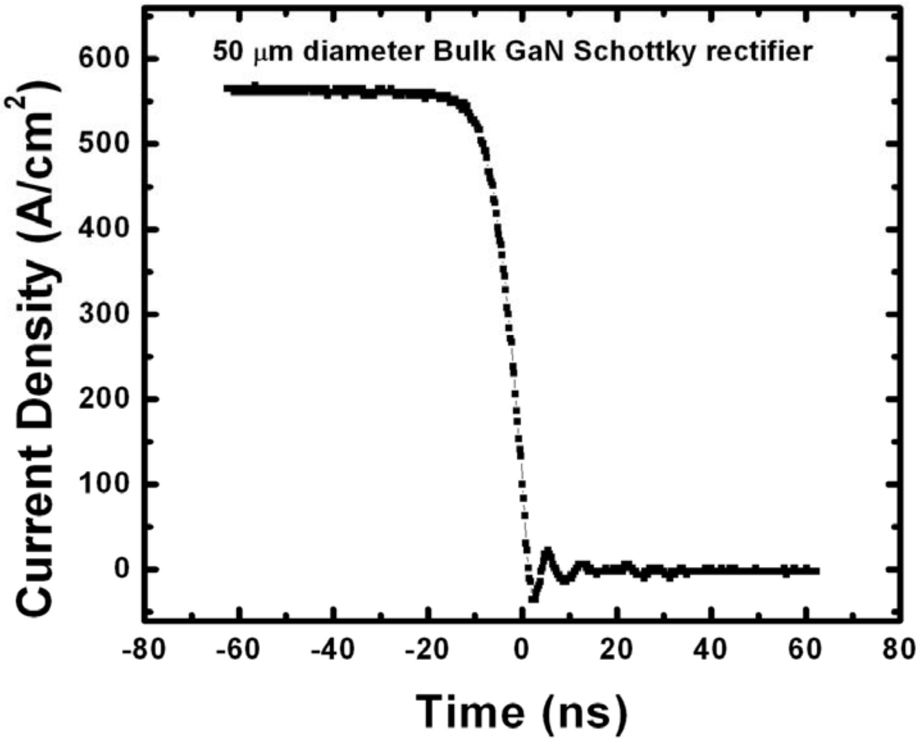


Figure 3.11: Reverse recovery characteristics of a 50 µm diameter bulk GaN rectifier

3.5 Temperature-dependent characteristics

It's of great importance to study the temperature-dependent electrical characteristics of the bulk GaN Schottky diodes since they are also aimed for applications at elevated temperatures. Some fundamental material properties, such as Richardson constant, can be extracted based on temperature-dependent I-V data. The accurate determination of these properties depends largely on the material quality, since the defects within the material can significantly change the electrical characteristics of the device fabricated on it. So another motivation for this study is to experimentally determine the Richardson constant of GaN using our low-defect-density bulk GaN substrate.

The Schottky diodes under this study were fabricated on a bulk GaN substrate with an unintentionally n-doping level of 7×10^{15} cm^{-3}. A SiO_2 field plate (~1 μm thick) was deposited on the front side of the substrate by radio frequency (RF) sputtering using a SiO_2 sputter target with 25 sccm Ar flow. Buffered Oxide Etch (BOE) was used to open windows on the SiO_2 for 50 μm diameter Schottky contacts. Ohmic contact and Schottky contact metallization were the same as described in Section 3.3 except the Schottky metal is 1.2 μm in thickness and with 25 μm overlap on the SiO_2 field plate. The utilization of the SiO_2 field plate was aimed to relieve the electric field crowding at the Schottky contact edge so as to increase the reverse breakdown voltage of the Schottky diodes. A detailed device simulation using MEDICI software will be given in Chapter 4. However, due to the poor material quality of the sputtered SiO_2 and a possible high density of fixed oxide charge at the SiO_2/GaN interface, there is no obvious improvement in the reverse breakdown voltage of the bulk GaN Schottky diode with the presence of the sputtered SiO_2 field plate. Nevertheless, the Schottky diode exhibited excellent I-V characteristics at room temperature, with a reverse leakage current of ~0.5 pA at -30 V and reverse breakdown voltage of 560 V. The I-V and C-V characteristics of the bulk GaN Schottky rectifiers were studied in the temperature range of 298K-473K in the dark by using a Thermcraft temperature-controlled chuck with a sensitivity of ± 1K.

The forward I-V characteristics of the bulk GaN Schottky rectifiers at different temperatures are shown in Figure. 3.12. There are two regions where the temperature-dependent I-V behaves differently. At low current levels, the thermionic emission current is the dominant current conduction mechanism. As the temperature increases, the barrier heights are lowered due to the increase in electron thermal energy.[89] So at the same forward bias, the current increases with temperature. However, at higher current levels, the voltage drop is mainly attributed to the series resistance (R_s) of the diode. A decrease in current with increasing temperature is mainly due to the decrease in electron mobility which causes an increase in R_s. Defining the forward turn-on voltage (V_F) to be the forward bias voltage at which the current density reaches 100 A/cm^2, the typical V_F for our Schottky diode is ~1.3 V at room temperature and it is found to increase slightly with temperature, with V_F of ~1.7 V at 200°C. It indicates that the series resistance effect takes over the barrier lowering effect before the current density reaches 100 A/cm^2, which is possibly caused by the low n-doping of our bulk substrate. V_F was also found to be almost independent of temperature[90] or decreases with temperature[91] by other researchers, which may be caused by the compensation of these two opposite effects or dominance of barrier lowering.

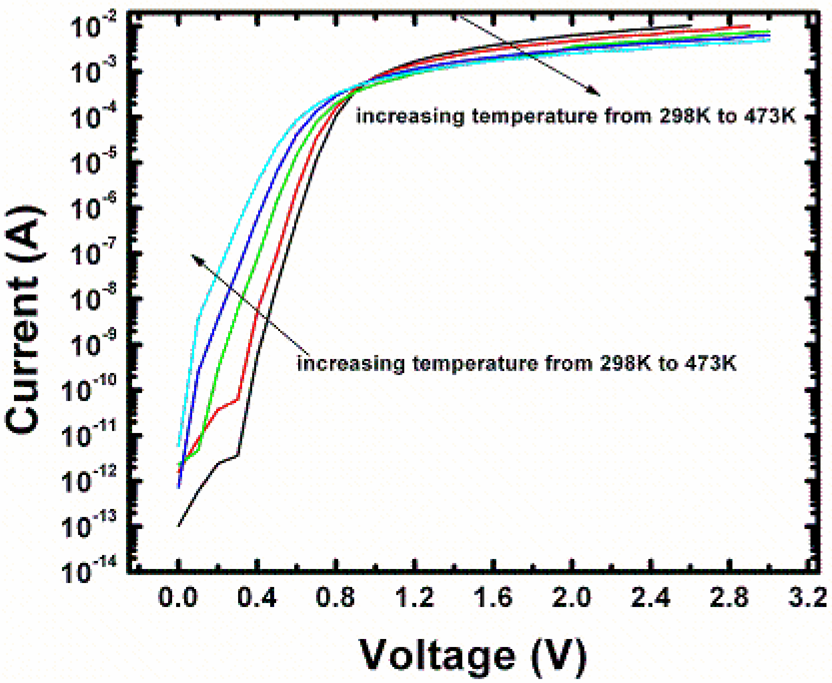


Figure 3.12: Forward I-V of 50μm diameter bulk GaN Schottky diodes at different temperatures.

The I-V relation for a Schottky diode based on thermionic emission theory is given by:[92]

$$I = I_0 \exp(qV / nkT)[1 - \exp(-qV / kT)] \tag{3.3}$$

$$I_0 = AA^* T^2 \exp(-q\Phi_b / kT) \tag{3.4}$$

where I_0 is the saturation current, n is the ideality factor, V is the forward bias voltage, T is the absolute temperature, q is the electron charge, k is the Boltzmann constant, Φ_b is the apparent Schottky barrier height, A is the effective diode area and A^* is the effective Richardson constant for n-GaN, assumed to be 26.4 Acm^{-2}K^{-2}. Under forward bias ($qV >$

3*kT*), Eq. (3.3) reduces to:

$$I = I_0 \exp(qV / nkT) \tag{3.5}$$

A linear region can be found by plotting log *I vs. V*, where the intercept at *V*=0 is I_0 and the slope is *q/nkT*. However, the above equations are based on the neglect of the series resistance of the diode. For diodes with a high series resistance, especially at high temperature where the series resistance increases significantly due to reduction of mobility, the forward current is limited and departs from linearity for much of the forward region. Thus, the accurate determination of I_0 and *n* is not reliable.[93] Therefore, the correct voltage across the junction should be $V\text{-}IR_s$, and Eq. (3.5) now becomes:

$$I = I_0 \exp[q(V - IR_s) / nkT] \tag{3.6}$$

The Φ_b^{I-V} (Schottky barrier height evaluated from I-V measurement) and *n* are then evaluated from the semilog plot of *I vs.* $V\text{-}IR_s$. The R_s is determined using a method proposed by Cibils.[94] One can also obtain the series resistance of a Schottky diode using approaches described by Norde[95], Bohlin[96], Cheung[97], Sato[98] or Lee[99]. For our diode, the values of R_s are found to be 180Ω, 240Ω, 390Ω, 430Ω, and 600Ω at 298K, 323K, 373K, 423K, and 473K, respectively.

C-V measurements were performed at a frequency of 100 KHz. The C-V relation for a Schottky barrier is given by:[92]

$$(1/C)^2 = (2/\varepsilon qNA^2)(V_{bi} - V - kT/q) \tag{3.7}$$

where *C* is the capacitance, ε is the permittivity (for GaN $\varepsilon = 9\varepsilon_0$), *N* is the n-type doping concentration of the substrate (7×10^{15} cm^{-3} was used) and V_{bi} is the built-in potential. The Φ_b^{C-V} (Schottky barrier height evaluated from C-V measurement) is related to V_{bi} by the relation:

$$\Phi_b^{C-V} = V_{bi} + V_0 \tag{3.8}$$

$$V_0 = (kT/q)\ln(N_c/N) \tag{3.9}$$

where N_c is the effective conduction band density of states. N_c=2.3×10^{18} cm^{-3} for GaN at room temperature and has a temperature dependence of $N_c \propto T^{\frac{3}{2}}$.

Figure. 3.13. shows the temperature dependence characteristics of Φ_b^{I-V}, ideality factor *n* and Φ_b^{C-V}. Interestingly, the Φ_b^{I-V} was found to increase with temperature while Φ_b^{C-V} remain almost the same or slightly decrease with temperature. Ideality factor n was found to decrease with temperature. Similar phenomenon was also found in silicon-based Schottky diodes.[100, 101] The existence of Schottky barrier height inhomogeneity was often used to explain such a temperature dependence of Φ_b^{I-V} and *n*. Assuming a diode consists of parallel segments of different barrier heights and each contributes to the current independently (parallel conduction model), the current of the diode will preferentially flow through the lower barriers. As a result, the current conduction is dominated by patches of lower barrier height with larger ideality factor at lower temperatures. However, as the temperature increases, patches with higher barrier heights take effect due to the fact that electrons gain sufficient thermal energy to surmount them.[102] A Gaussian distribution of the barrier heights based on thermionic emission (TE) mechanism has been widely accepted and utilized to explain the nature of this temperature dependence by some studies.[100-102] However, in order to apply this model, more information is needed in the lower temperature range where the deviation from TE is severe. On the other hand, Φ_b^{C-V} is more likely an average measurement of the Schottky barrier height within the device active area. Therefore, it is less dependent on the temperature.

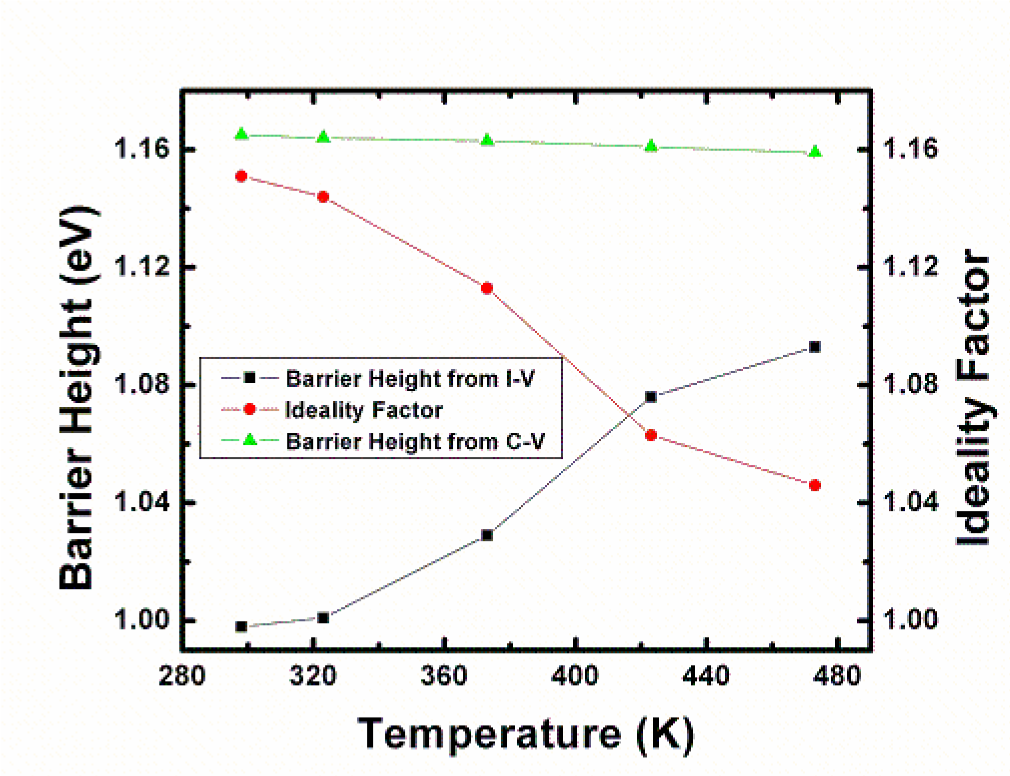


Figure 3.13: Temperature dependent Schottky barrier heights and ideality factor of 50 μm diameter bulk GaN Schottky diodes derived from I-V and C-V data

The Richardson constant is usually determined from the ln(J_0 / T^2) *vs.* 1/*T* plot, where J_0 is the saturation current density. Figure. 3.14(a) shows the conventional

Richardson plot, which yields an effective value of A^* to be 0.029 Acm^{-2}K^{-2}. The A^* extrapolated from conventional Richardson plot is typically much smaller than the theoretical value of 26.4 Acm^{-2}K^{-2}.[103-105] Hacke *et al.* suggested that it was caused by the presence of a barrier through which the electron must tunnel.[103] Guo *et al.* suggested the decrease of effective contact area may also cause the low value of A^*.[104] The conventional Richardson plot is based on the assumption that both Schottky barrier height and ideality factor are independent of temperature. However, according to our experimental data, such an assumption is not validated. Otterloo *et al.*[106] have shown that C-V method is most accurate in determining Schottky barrier height compared to I-V and photoemission methods. If we take Φ_b^{C-V} as the real Schottky barrier height, the temperature dependence of barrier height is rather small and thus could be neglected. The temperature dependent ideality factor *n(T)* was proposed to be included in the expression of saturation current by Hackam *et al*;[107] thus,

$$I_0 = AA^*T^2 \exp(-q\Phi_b / n(T)kT) \qquad (3.10),$$

so the modified Richardson plot should be $\ln(J_0/T^2)$ *vs.* $1/nT$ as shown in Fig. 14(b). The linearity of this plot is much better and the A^* extrapolated is 35 Acm^{-2}K^{-2}, which is much closer to the theoretical value of 26.4 Acm^{-2}K^{-2}.

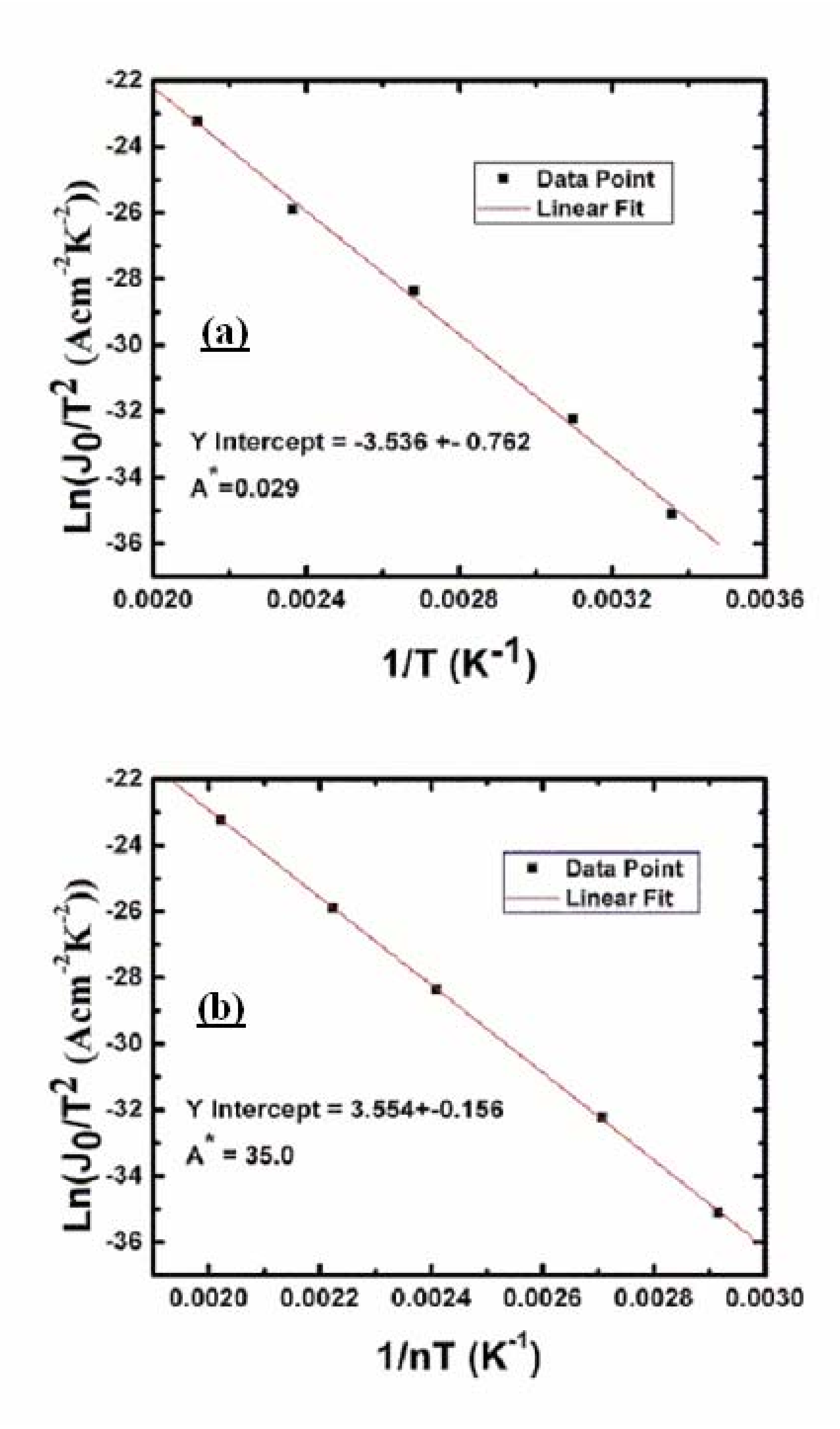


Figure 3.14: (a) A conventional Richardson plot of ln(J_0 / T^2) *vs.* 1/*T* and (b) a modified Richardson plot of ln(J_0 / T^2) *vs.* 1/*nT* for bulk GaN Schottky diodes.

Figure 3.15 shows the temperature dependent reverse leakage current of the 50 μm diameter Schottky diode. A very low reverse leakage current of ~0.5 pA at -30V at room temperature was observed. However, it increases significantly as the temperature exceeds 50°C, which is possibly caused by defect-assisted tunneling through surface or defects states.[91]

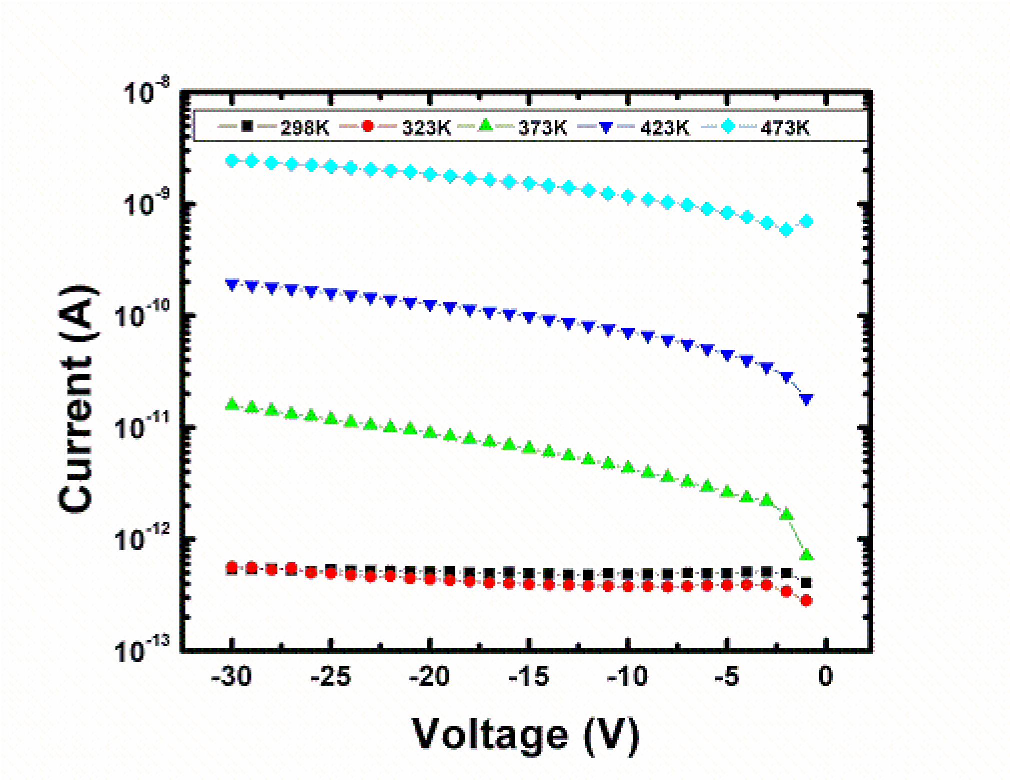


Figure 3.15: Temperature dependent reverse current of 50μm diameter bulk GaN Schottky diodes.

Figure 3.16 shows the typical temperature-dependent breakdown voltage of these diodes. Clearly, the reverse breakdown voltage has a negative temperature coefficient. Furthermore, the V_b decreases more rapidly in the temperature range of 25°C-100°C, with a coefficient of -3.5 VK^{-1}, and much less in the temperature range of 100°C-200°C, with a coefficient of -1.1 VK^{-1}. A positive temperature coefficient of V_b has been observed in 4H-SiC rectifiers with junction area small enough to avoid dislocations and other crystal imperfections.[108] The negative temperature coefficient of our bulk GaN Schottky rectifiers suggests that defect-assisted breakdown is a dominant breakdown mechanism for these rectifiers.

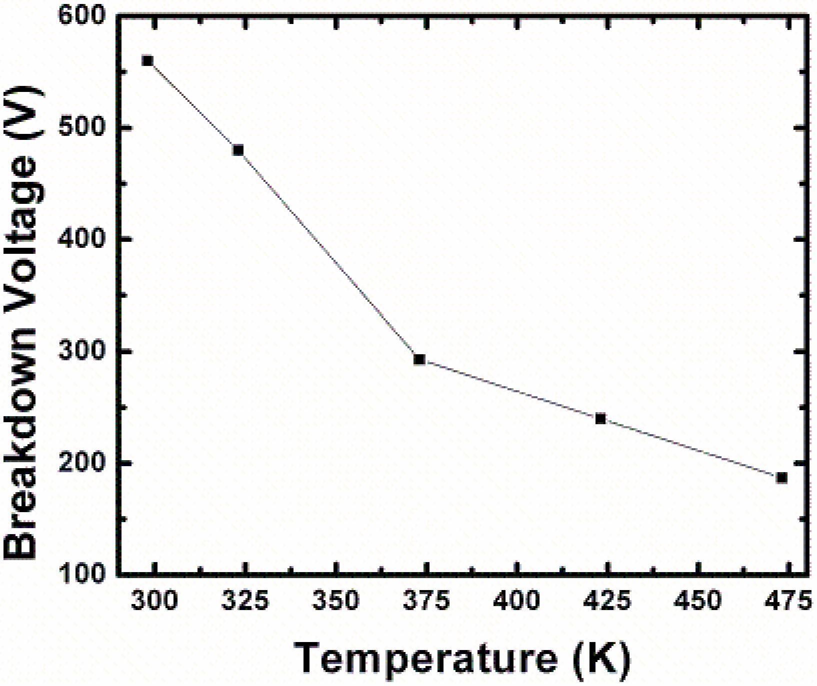


Figure 3.16: Reverse breakdown voltage as a function of temperature for 50μm diameter bulk GaN Schottky diodes.

3.6 Conclusion

The low-defect-density bulk GaN substrate enables the fabrication of high performance Schottky diode with a much simplified process. The unique ohmic contact scheme, improved thermal conductivity of the substrate and the vertical device geometry facilitate the forward current conduction with a much lower on-state resistance and at a much higher current density level. The high material quality of the bulk substrate also allows for the low reverse leakage current, high reverse breakdown voltage and ultrafast reverse recovery characteristics of the Schottky diode fabricated directly on it. Some electrical characteristics of Schottky diodes fabricated on bulk GaN substrates are summarized in Table 3.1 and compared with those fabricated on conventional unintentionally doped GaN epilayer/Sapphire structure. The improvements in device characteristics of Schottky diodes fabricated on bulk GaN substrates are obvious and the potential of GaN Schottky diode for high power application is further demonstrated.

Table 3.1. Comparison of Schottky diodes characteristics fabricated on unintentionally doped bulk GaN substrate and GaN epilayer/Sapphire structure

	On bulk GaN	On GaN epi/Sapphire
Forward turn-on voltage V_F (V)	0.85-1.3	3 - 5
On-State Resistance R_{ON} (mΩ•cm^2)	0.88-3.3	6 - 23
Reverse breakdown voltage V_B (V)	630	280 - 550
Reverse recovery time (ns)	<20	<200
High current density capability	Yes	No
Best Figure of Merit V_B^2/R_{ON} (MW/cm^2)	180	48

However, despite the recent encouraging result, one should note that the remarkable improvements in electrical characteristics are mainly achieved with small -area diodes. Large-area diodes are preferred in order to conduct high current for practical high power application. However, for the current defect density level of the bulk GaN substrate (typically ~5×10^6 cm^{-2}), even a 50 μm diameter diode would contain ~ 100 dislocations within the device active area. The reverse breakdown voltage for a large-area diode would be compromised due to the huge amount of defects within its active area.

Strong dependence of reverse leakage current and breakdown voltage on diode size is observed for all the reported Schottky diodes fabricated on bulk GaN substrates. Indeed, the temperature dependent studies of reverse breakdown voltage of Schottky diodes fabricated on bulk GaN substrates revealed a negative temperature coefficient, which is indicative of a defect-assisted breakdown mechanism. The positive temperature coefficient of breakdown voltage has not yet been achieved with the bulk GaN substrate. However, it is anticipated that with the continuous perfection in crystal growth with the aid of bulk GaN substrate, large-area Schottky diodes with high breakdown voltage and positive temperature coefficient for practical high power electronic application will eventually come to reality. The Richardson constant extracted from the modified Richardson plot is 35 $Acm^{-2}K^{-2}$, which is reasonably close to the theoretical value of 26.4 $Acm^{-2}K^{-2}$.

CHAPTER 4

MEDICI SIMULATIONS OF REVERSE BREAKDOWN VOLTAGES OF BULK GAN SCHOTTKY DIODES WITH FIELD PLATES EDGE TERMINATION

4.1 Introduction

Device simulation is an important step for industry-standard fabrication processes. Simulation can help analyze the device performance without having to manufacture and test the actual device. It allows device designs to be optimized for the best performance without fabrication, eliminating the need for costly experiments and offering guidance for the real fabrication process.

Taurus-Medici is a Synopsys industry-standard device simulation software that can be used to predict the electrical, thermal and optical characteristics of semiconductor devices, such as MOSFETs, BJTs, HBTs, power devices, IGBTs, HEMTs, CCDs, photo detectors and LEDs.[109] Medici models the two-dimensional (2D) distributions of potential and carrier concentrations in a device and can be used to analyze the device under arbitrary bias conditions by solving Poisson’s equation and the electron and hole current continuity equations. For accurate simulations, Medici incorporates a number of physics models, including models for recombination, photogeneration, impact ionization, band-gap narrowing, band-to-band tunneling, mobility, lifetime, Fermi-Dirac and Boltzman statistics.[110] A nonuniform triangular simulation grid is used to model arbitrary device geometries. The simulation grid can also be refined automatically during the solution process. Material regions, impurity concentrations and electrodes can be defined by the user for a specific device structure and simulation process.

The semiconductor materials that have pre-defined material parameters in Medici include Si, Ge, GaAs, SiGe, AlGaAs, HgCdTe, InP, InGaAs, InAs, Diamond, ZnSe, ZnTe, AlInAs, GaAsP, InGaP, InAsP and SiC. Unfortunately, GaN is not one of them. However, Medici allows users to arbitrarily define new materials or change default parameters for pre-defined materials. So there are two ways to define GaN material properties for the simulation of GaN-based devices. One way is to use the MATERIAL statement to define a new material named “GaN” by inputting all the necessary material parameters into the program. The other way is to use one of the pre-defined materials, such as Si, and then use the MATERIAL statement to change the Si’s default properties to GaN’s. We choose the second method, that is, we use Si for GaN regions and then change the Si default parameters to GaN’s. The material parameters we have changed are listed in Appendix A.

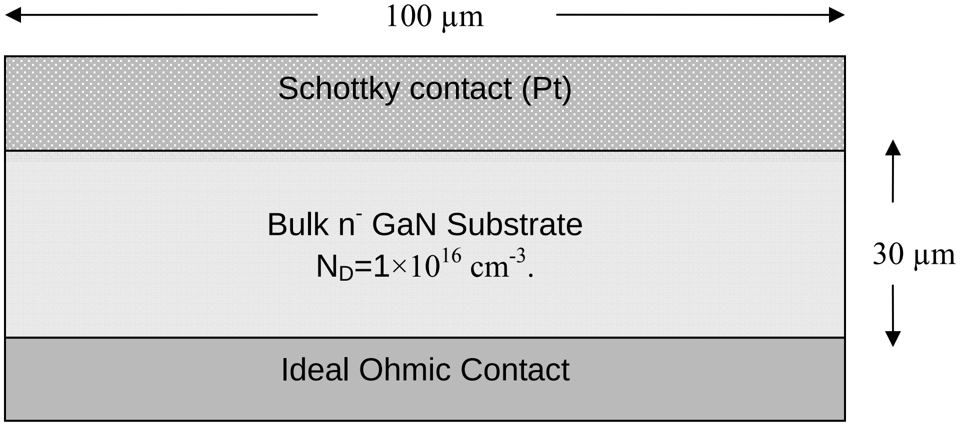
The purpose of this study is to simulate the reverse breakdown characteristics of the bulk GaN Schottky diodes with a field plate edge termination scheme, and to find the optimal field plate parameters for alleviating the electric field crowding at the Schottky contact edge so as to increase the reverse breakdown voltages. It is well-known that field crowding at the Schottky contact edge can cause avalanche breakdown of the devices at much lower voltages than expected from an ideal parallel-plate device. Edge termination schemes, such as field plates,[111] p-type guard rings,[112] floating metal rings,[113] and highly resistive surface regions formed by implantation,[114-116] have been shown to effectively mitigate the field crowding at the contact edge, resulting in higher breakdown voltages for SiC Schottky diodes.

Even though the field plate edge termination may not be able to achieve the same level of reverse breakdown voltages as other edge termination schemes mentioned above, it is still widely used due to its process simplicity and the fact that it requires no ion implantation and subsequent high temperature activation. This advantage is even more obvious for GaN devices, because p-type doping for GaN by ion implantation still remains a challenge,[117] and GaN is thermally unstable at high temperatures which are necessary to activate the implants.

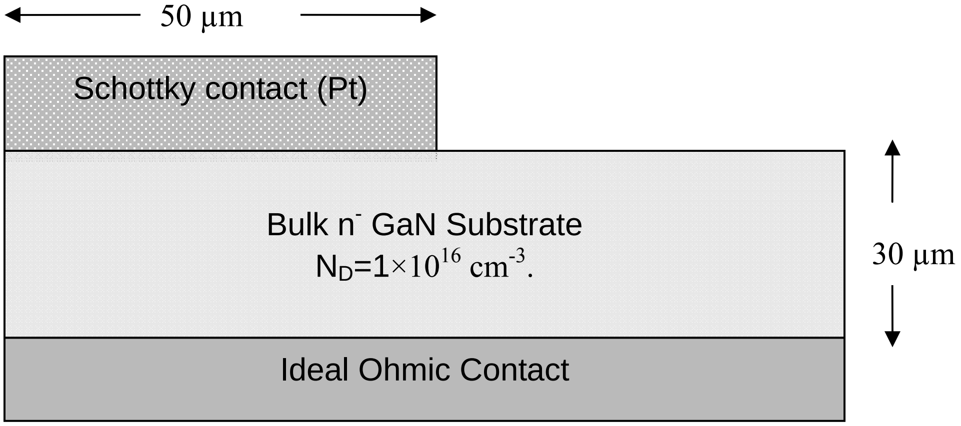
We choose SiO_2 as the field plate dielectric since it’s one of the most commonly used materials for field plate termination schemes for Si and SiC Schottky diodes. The parameters we have investigated include the extent of metal electrode overlap, dielectric thickness and fixed oxide charge density at the SiO_2/GaN interface.

4.2 Device structure and simulation setup

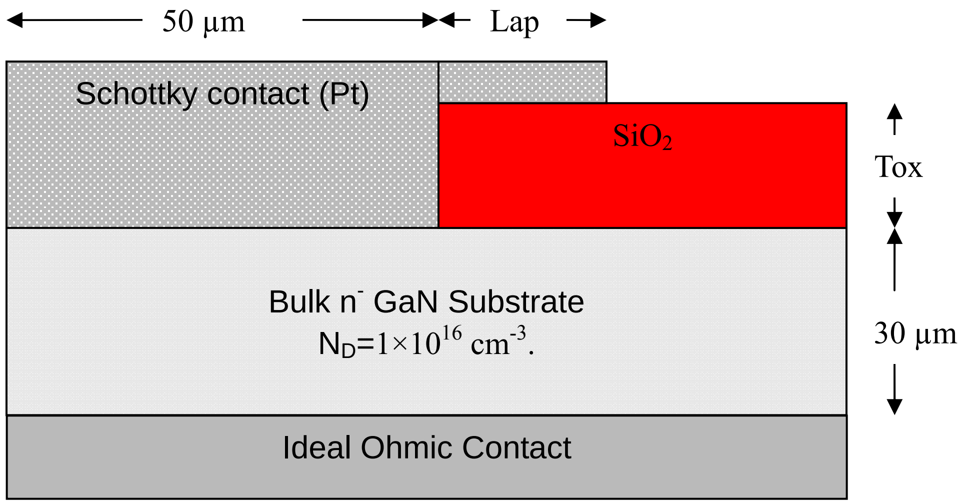
The structures of ideal parallel-plate, unterminated, and field plate edge terminated bulk GaN Schottky diodes are shown in Figure 4.1(a), (b) and (c), respectively.



(a)



(b)



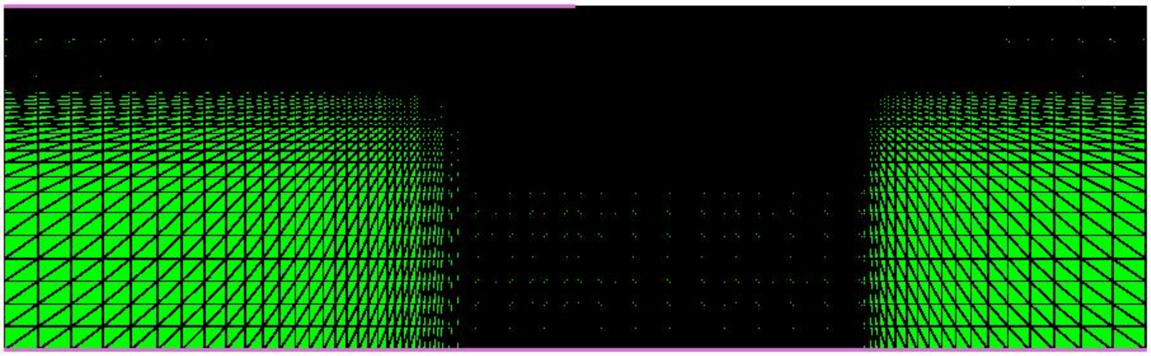
(c)

Figure 4.1: Device structures of (a) ideal parallel plate, (b) unterminated, (c) field plate edge terminated bulk GaN Schottky diodes

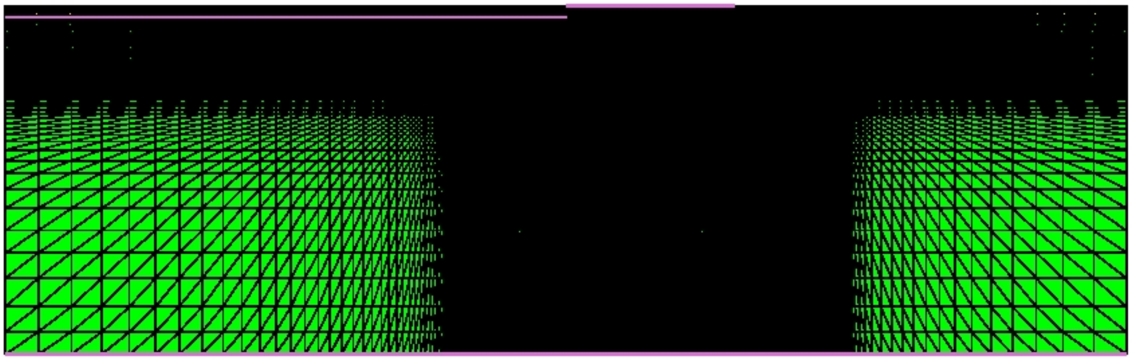
The actual thickness of the bulk GaN substrate is ~460 μm. However, since the depletion depth is limited by the background doping level, we used a thickness of 30 μm in this simulation, which is thick enough to prevent full depletion of the n^- GaN layer. The n-doping concentration of the bulk GaN substrate is set to be 1×10^{16} cm^{-3}. Ideal ohmic contact (zero contact resistance) is assumed on the full backside of the GaN, and the Pt Schottky contact is defined on the front side by setting the work function of the Schottky contact (5.65 eV for Pt) in the CONTACT statement. For devices with field plate edge termination, the SiO_2 layer thickness (Tox) and the Schottky metal overlap

(Lap) are defined as variables in order to find the optimal values.

After designing the device structures, device grids are created to allow the solutions of the transport equations to be obtained. Device gridding is found to play a significant role in convergence stability as well as the simulation results. Correct meshing for a specific device structure is often gained heuristically through trial and error.[118] From the efficiency point of view, and to save simulation time, it is desirable to use more mesh nodes at critical regions of interests, such as the Schottky contact edge where field crowding occurs, and fewer mesh nodes in regions where there is much less electric field, such as regions far away from the Schottky contact edge or deep inside the bulk GaN. The typical meshing griddings for our unterminated and field plate edge terminated devices are shown in Figure 4.2(a) and (b), respectively.



(a)



(b)

Figure 4.2: Mesh griddings for (a) unterminated Schottky diode and (b) field plate terminated Schottky diode

Since the device gridding can significantly affect the simulation result, it is very important to keep the gridding as intact as possible for each simulation. This is to ensure that the differences in simulation results are caused by the change of input variables, not by the change of device griddings.

We performed quasi-3D simulations in cylindrical symmetry to account accurately for the effects of three-dimensional field crowding.[119] The physical models we have incorporated in the simulations include Shockley-Read-Hall and Auger recombination, impact ionization, Fermi-Dirac statistics, analytical and field-dependent mobility models.

Device failure occurs when either one of the following condition is met. The first condition is semiconductor breakdown due to impact ionization, which is defined when the ionization integral for electrons (4.1) or for holes (4.2) reaches one:[120]

$$\int_0^W \alpha_n(x)\exp\left(-\int_0^x (\alpha_n(\Delta)-\alpha_p(\Delta))d\Delta\right)dx = 1 \tag{4.1}$$

$$\int_0^W \alpha_p(x)\exp\left(\int_0^x (\alpha_n(\Delta)-\alpha_p(\Delta))d\Delta\right)dx = 1 \tag{4.2}$$

where W is the depletion width at breakdown, α_n and α_p are electron and hole ionization coefficients, respectively, which are given by:[120]

$$\alpha_{n,p} = a_{n,p}\exp\left(\frac{-b_{n,p}}{|E|}\right) \qquad (4.3).$$

Here E is the electric field component in the direction of current flow, a_n, b_n, a_p, b_p are constants. For GaN, a_n = a_p = 8.85 $\times 10^6$ cm^{-1} and b_n = b_p = 2.6 $\times 10^7$ Vcm^{-1}.[3]

The second condition is oxide breakdown, which occurs when the maximum electric field inside the SiO$_2$ field plate region exceeds the SiO$_2$ breakdown field strength (10 MV/cm). This consideration is essential for the SiO$_2$ field plate because it usually suffers from a high electric field and premature breakdown due to its relatively low relative dielectric constant of $\varepsilon = 3.9$.[121]

The simulation stops when either one of the above conditions is met. A sample simulation program is given in Appendix B.

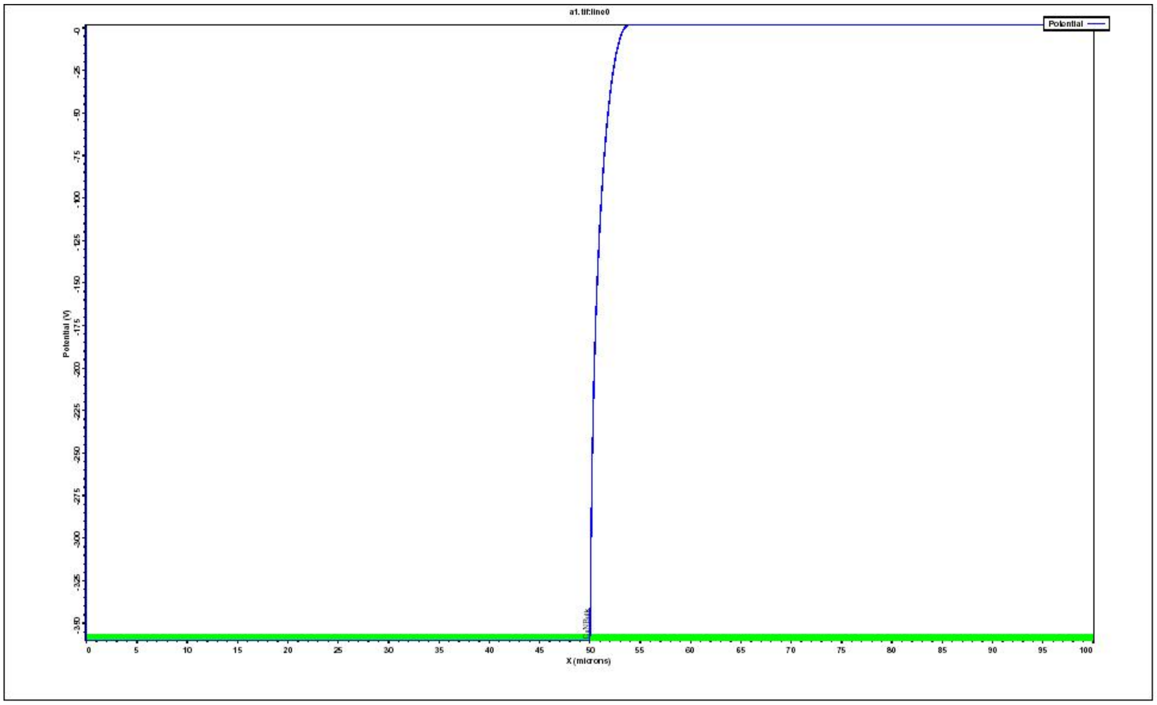
4.3 Result and discussion

The breakdown voltage of the parallel plate bulk GaN Schottky diode shown in Fig 4.1(a) is simulated to be 3060 V at a critical breakdown field of 3.5 MV/cm. According to the theoretical predictions[122]

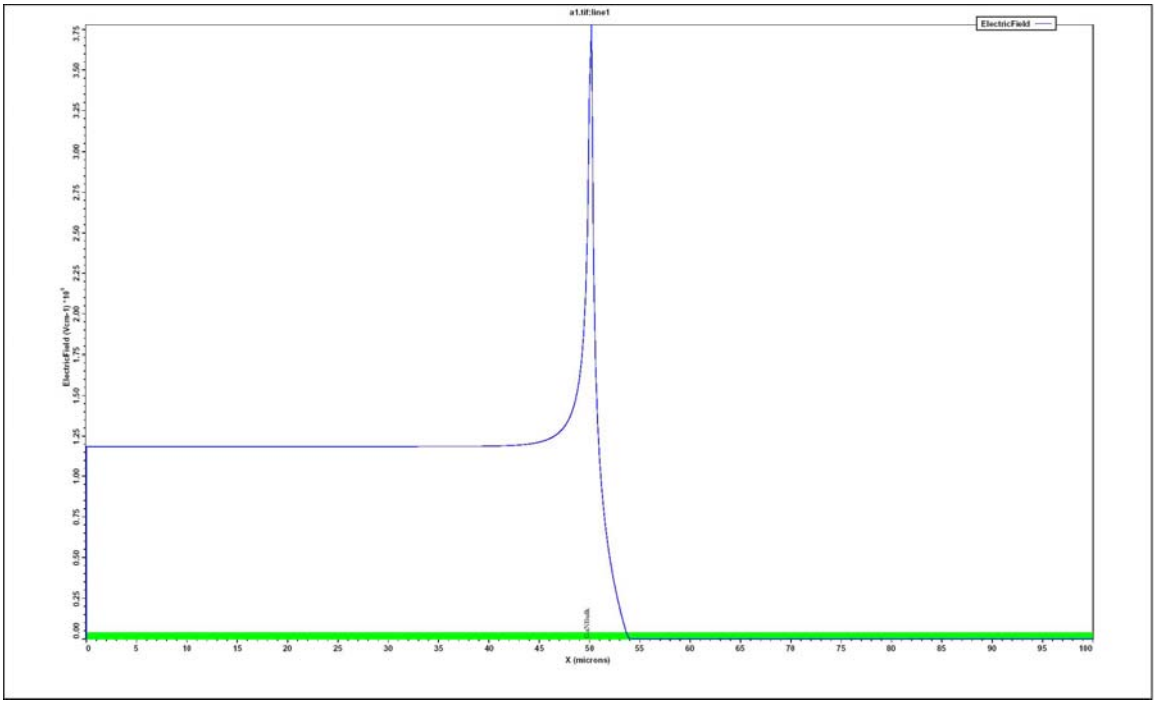
$$V_b = \frac{\varepsilon_0 \varepsilon E_c^2}{2qN_d} \tag{4.4}$$

where V_b is the breakdown voltage, ε_0 is the vacuum permittivity, ε is the relative semiconductor dielectric constant, E_c is the semiconductor critical field, q is the electron charge and N_d is the doping concentration. In our case, $\varepsilon = 9$ for GaN and $N_d = 1 \times 10^{16} cm^{-3}$, the V_b is then calculated to be around 3050 V if a E_c of 3.5 MV/cm is used. This value is very close to our simulation result of 3060 V, indicating the simulation is in good shape. This breakdown voltage is the ideal maximum value achievable irrespective of the kind of edge termination scheme used.

In comparison, the V_b for the unterminated structure shown in Fig 4.1(b) is only around 360 V, which is less than 12% of the ideal value. Figures 4.3(a) and (b) show the potential and electric field distribution of this device at breakdown. It can be clearly seen that the device has undergone a corner breakdown due to the electric field crowding at the Schottky contact edge, where the peak electric field in GaN is as much as 3.75 MV/cm, which is more than 3 times the field under the center of the contact. A critical design need therefore is to mitigate the electric field crowding at the Schottky contact periphery.



(a)



(b)

Figure 4.3: The (a) potential and (b) electric field distribution of the unterminated Schottky diode at breakdown

Figure 4.4 shows the electric field distribution of a SiO_2 field plate terminated structure as shown in Fig 4.1(c) at the reverse bias of 360 V, which is the breakdown voltage of the unterminated device. The SiO_2 field plate is 1 μm thick, and the Schottky metal overlap is 15 μm. The electric field under the Schottky contact edge is reduced from 3.75 MV/cm to 2.2 MV/cm due to the presence of the field plate. As a result, the breakdown voltage for this device has increased to 970 V, which is 2.7 times that of unterminated devices and 32% of the parallel plate devices.

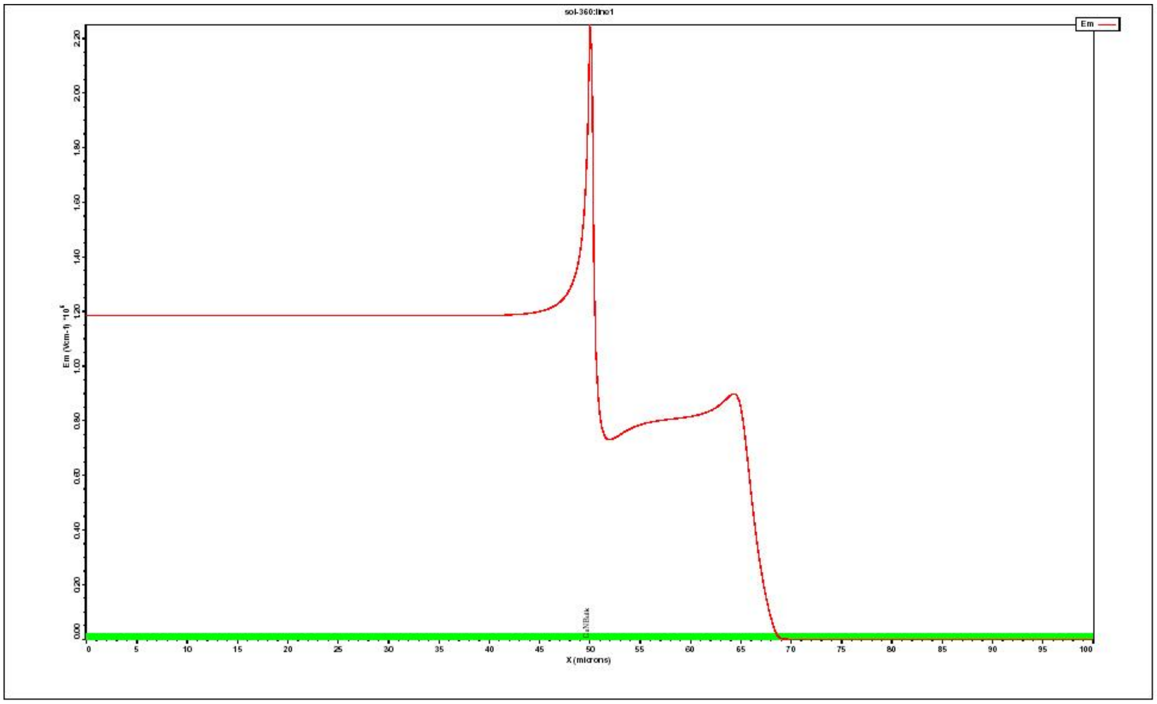


Figure 4.4: The electric field distribution of a SiO_2 field plate terminated Schottky diode at -360 V bias

It is obvious that the utilization of a SiO_2 field plate can effectively mitigate the field crowding at the Schottky contact edge and increase the device breakdown voltage. However, the selection of the SiO_2 field plate thickness plays a crucial role in fulfilling this task. Figure 4.5 shows the peak electric fields within the SiO_2 field plate and the GaN substrate at the reverse bias of 600 V, as a function of the SiO_2 field plate thickness. It can be seen that the peak electric field within the SiO_2 field plate decreases with field plate thickness, while the peak electric field within the GaN decreases, reaches a minimum value, and then increases with the field plate thickness.

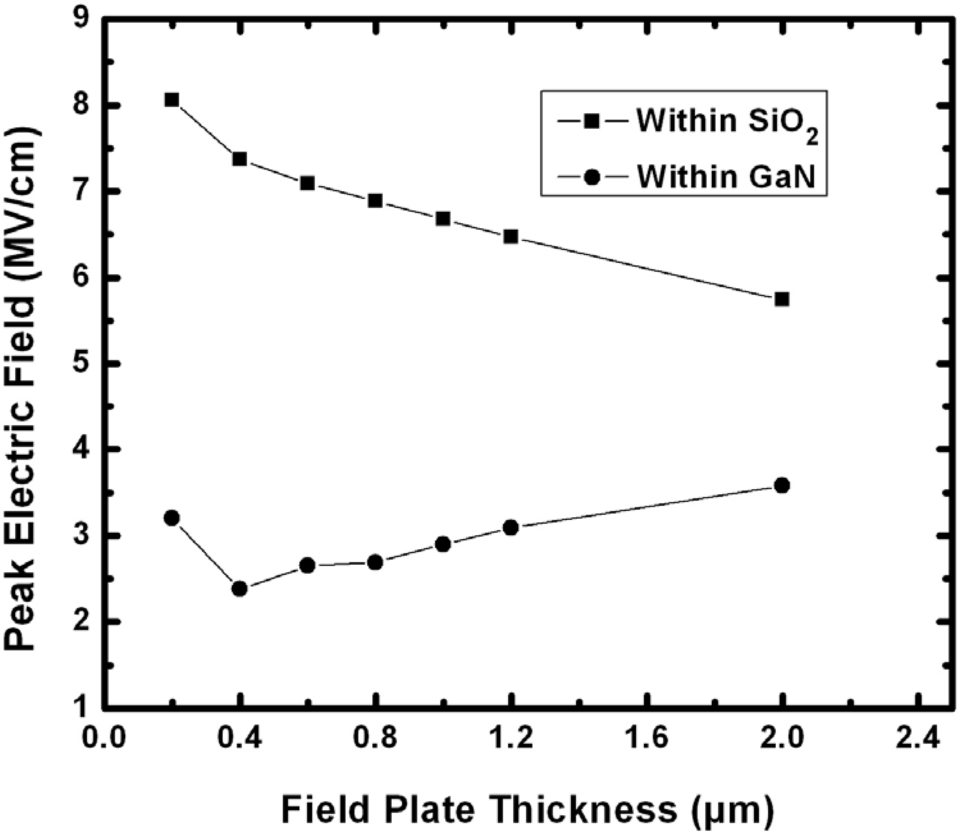


Figure 4.5: Peak electric fields within the SiO_2 field plate and GaN as a function of the field plate thickness at the reverse bias of 600 V

Figure 4.6 shows the electric field distribution of a terminated device with 0.2 μm thick field plate and 15 μm Schottky metal overlap at device breakdown. It should be noted that when using a field plate which is too thin, the peak electric field (4 MV/cm) within the GaN occurs at the Schottky metal overlap corner instead of the Schottky contact edge. This shift is caused by the fact that the Schottky metal overlap corner is so close to the semiconductor that it strongly influences the electric field there and creates a second high field region inside the semiconductor. So the utilization of a field plate which is too thin is not desirable since it creates high electric fields both within the dielectric and the semiconductor.

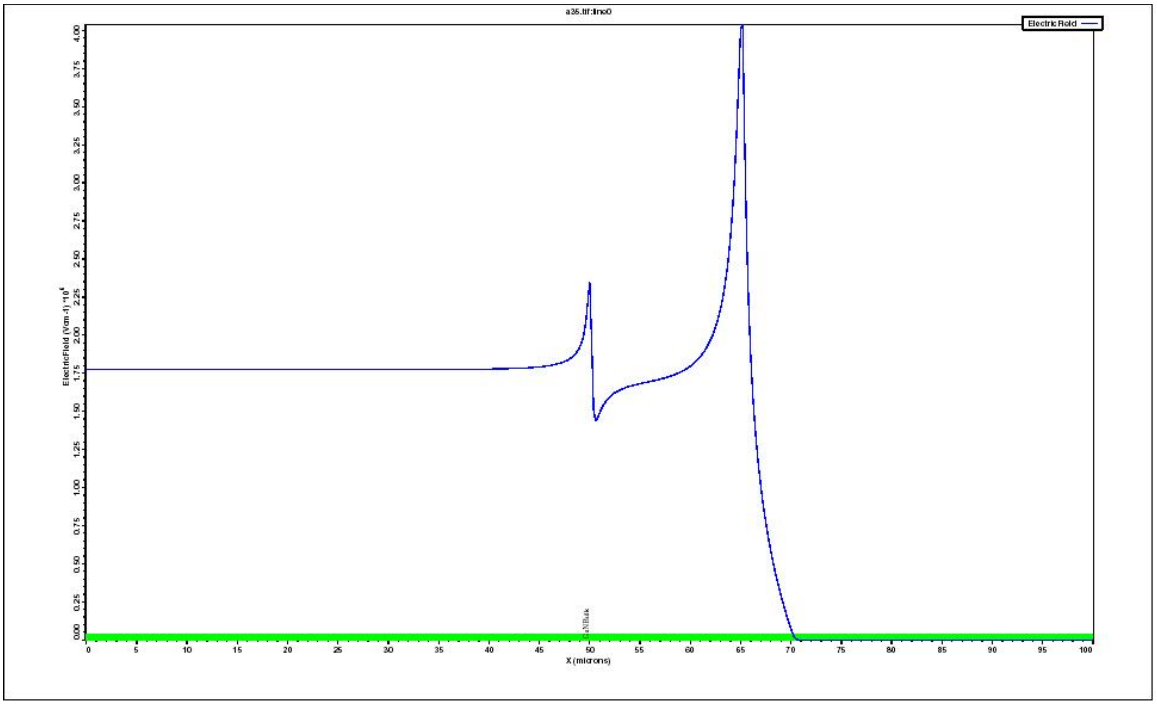


Figure 4.6: the electric field distribution of a terminated Schottky diode with 0.2 μm thick field plate and 15 μm Schottky metal overlap at device breakdown

As the field plate thickness increases, the peak electric field within both SiO_2 and GaN decreases, and the peak position within GaN shifts back to the Schottky contact edge. At the thickness of 0.4 μm, the peak electric field within GaN decreases to a minimum value and starts to increase with further increasing of the field plate thickness.

The increasing trend of the electric field within GaN with the field plate thickness is due to the fact that the Schottky metal overlap is so far away from the semiconductor that it does not have much influence on the electric field distribution. So the utilization of a field plate which is too thick is not desirable either.

Therefore, an optimized field plate should be sufficiently thick to prevent the breakdown of the dielectric and sufficiently thin to influence the electric field distribution within the semiconductor and provide sufficient field relief at the Schottky contact corner.[123]

Figure 4.7 shows the breakdown voltage as a function of field plate thickness, where the optimum thickness is found to be 1 μm, giving a maximum breakdown voltage of 970 V. The Schottky metal overlaps are kept as 15 μm for all cases. For field plate thickness thinner than 1 μm, dielectric breakdown occurs before the semiconductor breakdown. When field plate thickness exceeds 1 μm, semiconductor corner breakdown dominates. However, since the effect of electric field relief decreases with further increasing field plate thickness, the breakdown voltage decreases when thickness exceeds 1 μm.

Also in Figure 4.7 shows the breakdown voltage as a function of field plate thickness when only considering the GaN breakdown. The neglect of oxide breakdown leads to an optimum oxide thickness of 0.6 μm with a maximum breakdown voltage of 1330 V. This optimum oxide thickness is very close to the value of 0.7 μm from a similar study by Baik *et al*,[124] in which they only considered the GaN breakdown. However, this result could be misleading due to the fact that when the oxide field plate is too thin, intensive electric field within the SiO_2 field plate will leads to the device breakdown before the impact ionization integrals for electrons or holes in GaN reach one.

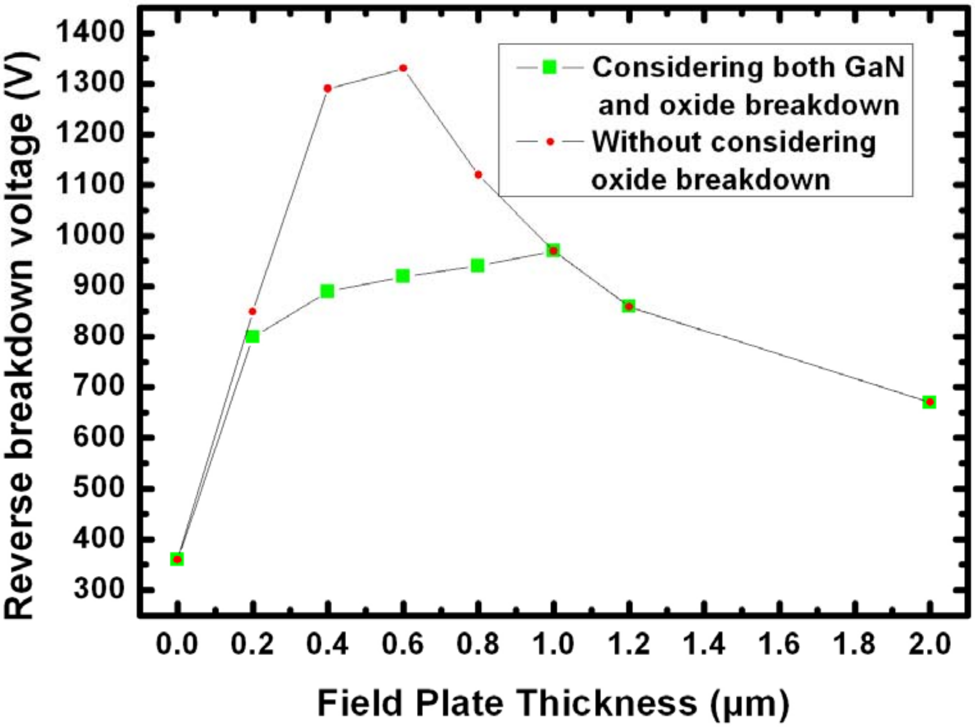


Figure 4.7: Reverse breakdown voltage as a function of field plate thickness with the same Schottky metal overlap of 15 μm.

The Schottky metal overlap distance also plays an important role in field relief. Figure 4.8 shows the reverse breakdown voltages as a function of Schottky metal overlap on a SiO_2 field plate of 1 µm thick. The breakdown voltage increases rapidly for overlaps up to 15 µm, beyond which, there is almost no further improvement. Considering the fact that the lateral spread of the depletion region is comparable to the depth of vertical depletion region, which is around 10 to 15 µm, extending the field plate into the undepleted region (>15 µm) does not result in any significant field relief effect.[123]

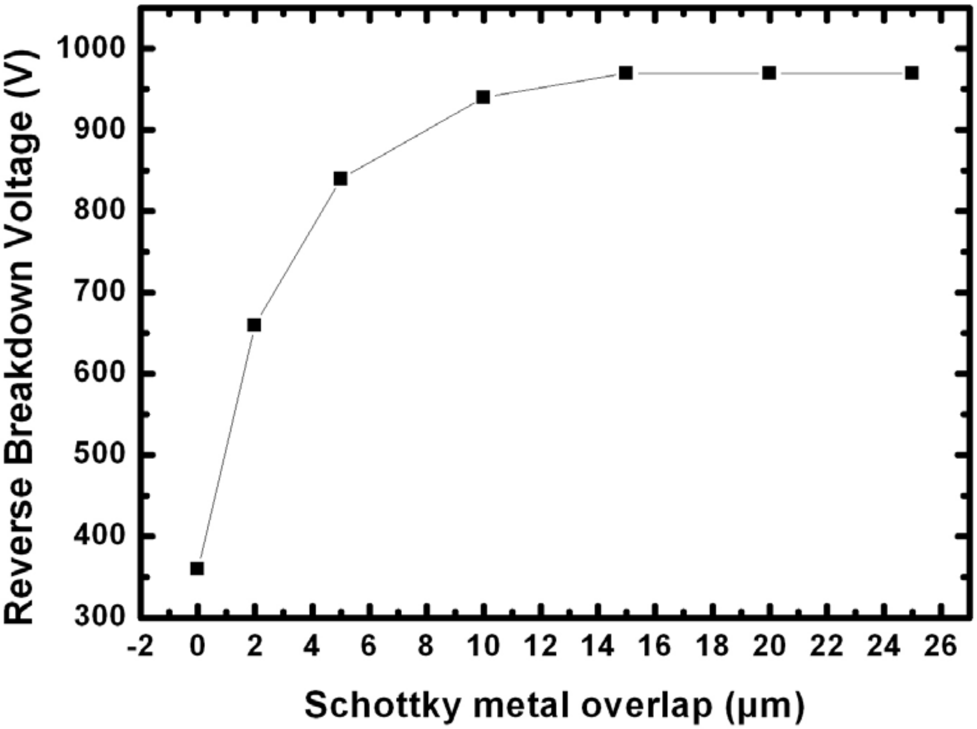


Figure 4.8: The reverse breakdown voltages as a function of Schottky metal overlap on a SiO_2 field plate of 1 µm thick

The above simulation results are based on the assumption that there are no interface charges at the SiO_2/GaN interface. However, this is not realistic, especially for the SiO_2/GaN interface, which can not be realized by thermal oxidation. The deposition of a SiO_2 layer on GaN typically results in an interfacial fixed oxide charge density at the level of high 10^{11} cm^{-3} or higher.[125] The fixed oxide charge density was found to play a detrimental role in the breakdown characteristics of SiC MOS capacitors[126] and Si detector diodes.[127]

The peak electric fields within the dielectric and semiconductor as a function of the fixed oxide charge density at the interface for an edge terminated device with 1 μm thick SiO_2 field plate and 15 μm Schottky metal overlap at the reverse bias of 200 V are shown in Figure 4.9.

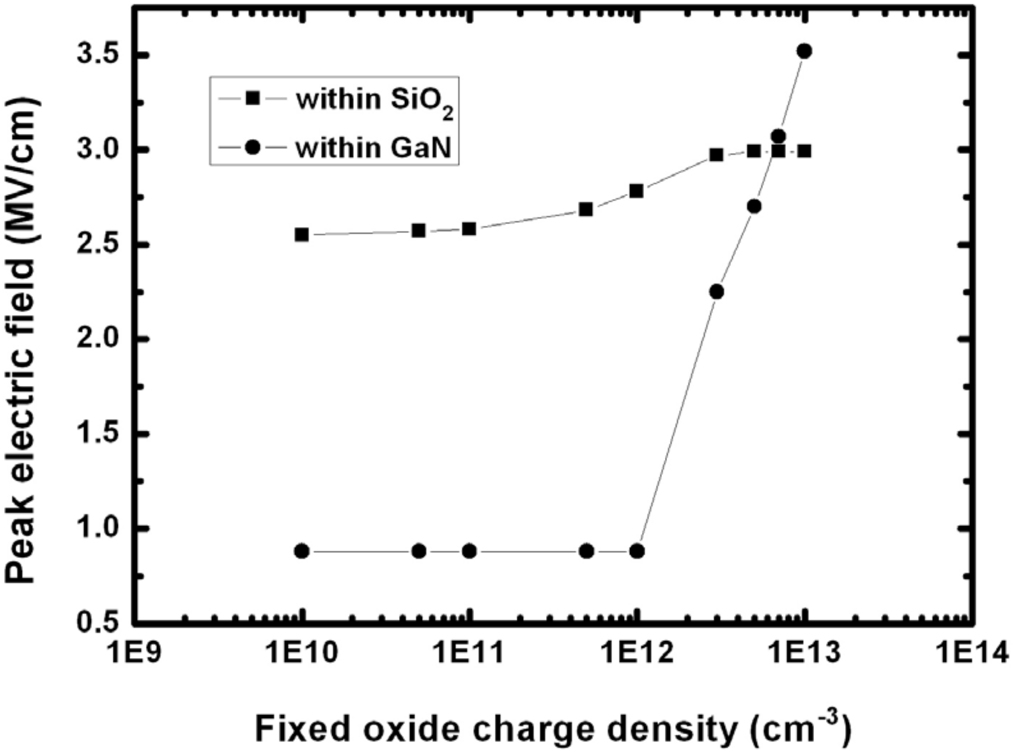


Figure 4.9: The peak electric fields within SiO_2 and GaN as a function of the fixed oxide charge density at the interface

Both electric fields show increasing trends with the density of fixed oxide charge at the interface. The increase of the peak electric field within GaN is negligible when the fixed oxide charge densities are lower than 10^{12} cm^{-3}. However, it increases dramatically when the fixed oxide charge exceeds 10^{12} cm^{-3}.

As a result, the reverse breakdown voltage decreases with fixed oxide charge density as shown in Figure 4.10. It should be noted that when the fixed oxide charge density exceeds 7×10^{12} cm^{-3}, the reverse breakdown voltages of the field plate terminated Schottky diodes are even lower than the unterminated devices. This is caused by the high electric field within the GaN due to the presence of large amount of fixed oxide charge at the interface.

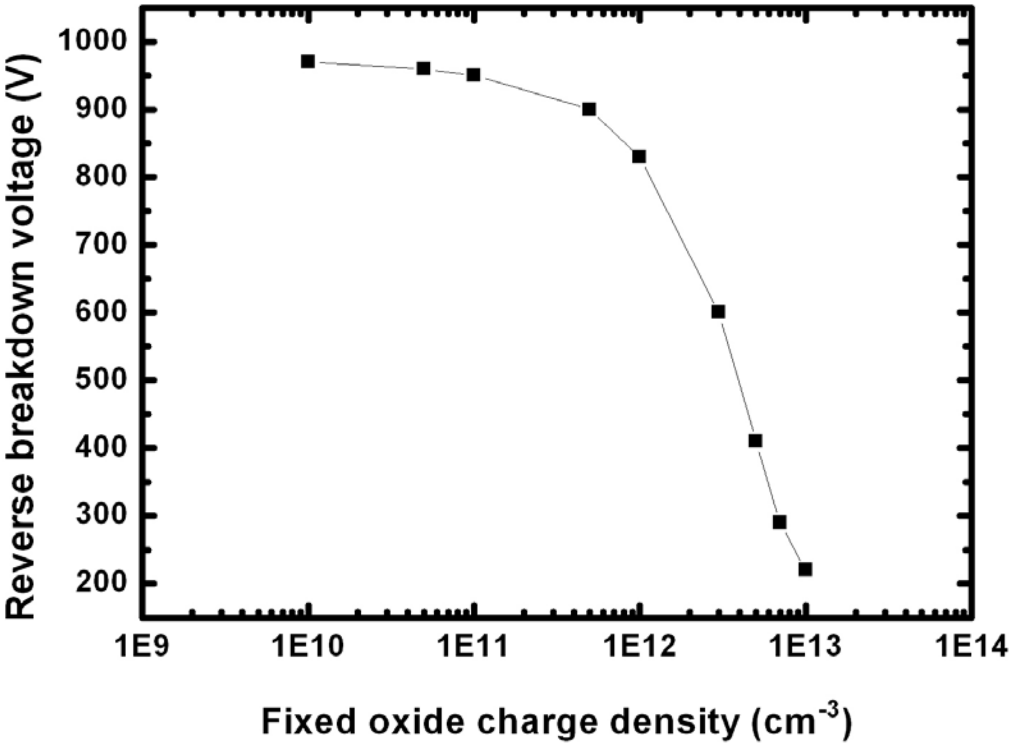


Figure 4.10: The reverse breakdown voltage as a function of fixed oxide charge density

4.4 Conclusion

We have carried out quasi-3D simulations on the reverse breakdown characteristics of a bulk GaN Schottky diode with a SiO_2 field plate using Medici software. The utilization of a SiO_2 field plate on bulk GaN Schottky diodes can effectively relieve the electric field crowding at the Schottky contact edge so as to increase the reverse breakdown voltage of the device. The optimum field plate thickness was found to be 1 μm, below which, oxide breakdown occurs before breakdown in the semiconductor. The effect of Schottky metal overlap on field relief saturated when extended into the undepleted region. The fixed oxide charge at the SiO_2/GaN interface was found to play a detrimental role in the reverse breakdown characteristics of the device, especially for charge densities above 10^{12} cm^{-3}.

CHAPTER 5

SCHOTTKY-TYPE ULTRAVIOLET PHOTODETECTOR FABRICATED ON A BULK GAN SUBSTRATE

5.1 Introduction

Gallium nitride (GaN) is one of the most promising materials for the realization of visible-blind Ultraviolet photodetector due to its large direct bandgap. Recently, various types of UV photodetectors such as p-n junction photodiodes,[128] p-i-n photodiode,[129] p-π-n photodetectors,[130] metal-semiconductor-metal (MSM) photodetectors[131-133] and Schottky barrier type photodiodes,[134-136] have been fabricated using GaN.

Compared to p-n junction photodiodes, MSM and Schottky barrier photodetectors are attractive because of their fabrication simplicity and high response speed. However, Schottky barrier type photodiodes typically suffer from an excess reverse leakage current compared to p-n junction diode or MSM photodetectors. Recently, extremely low dark currents have been achieved with MSM[137] and p-i-n photodetectors.[138]

Therefore, in the case of Schottky-type photodetectors, reducing the leakage current is of great technological importance. The leakage current characteristics can be influenced by many factors. Among these factors, formation of a Schottky contact with a high barrier height is one of the most important factors. Since it is also important to consider the transparency of the contact, semitransparent metals and transparent conducting oxide[139] with high work functions have been widely used for Schottky contacts in order to achieve high Schottky barrier heights with improved transparency of the contact. In addition to the choice of Schottky contact material, the leakage current of Schottky barrier photodetectors also depends strongly on the semiconductor material crystal quality, especially that of the topmost layer.[140] Due to the lack of native substrates, GaN films have been grown epitaxially on mismatched substrates, which results in a high density of dislocations traversing vertically from the epilayer/substrate interface to the film surface. The typical dislocation density of epitaxially grown GaN film is 10^8-10^{10} cm^{-2}. It has been shown that the threading screw dislocations of high concentration are the dominant source of high leakage current in GaN Schottky contacts at room temperature.[28, 31, 141] Therefore, reducing the dislocation density is essential for reducing the leakage current of GaN Schottky barrier photodetectors. Recently, we have synthesized bulk GaN substrates with dislocation density lower than 5×10^6 cm^{-2}, and we have also demonstrated fabrication of high quality Schottky rectifiers with a simplified processing step.[142] Therefore, by using the bulk GaN substrate with low dislocation density, we can also expect the improvement of the performance of GaN photodetector. Post-deposition annealing of the contact is also effective in reducing the leakage current of Schottky diodes with certain Schottky metals.[143, 144] The formation of interfacial compounds after annealing often leads to an increase in Schottky barrier height, which significantly reduces the leakage current.

Up to date, most of the GaN photodetectors fabricated are of lateral geometry. It was suggested that scattering by charged dislocations is the dominant scattering mechanism at low carrier concentration ($n<5\times10^{17}$ cm^{-3}) while impurity scattering becomes significant at high carrier concentration due to the screening of the dislocation charges by electrons.[34, 35] In this model, it was also suggested that the degree of scattering depends on the angle between the dislocation line and the direction of the current flow. Therefore, we can expect that the vertical transport is relatively immune to scattering by dislocations since the electron transport is parallel to the dislocation line. Indeed, Misra *et al*. has shown a significant increase in mobility for vertical transport due to the reduction in scattering by charged dislocations.[42] Katz *et al*. recently showed a lower noise level for vertical GaN Schottky UV photodetector, which is also attributed to the reduced effect of dislocations on the carrier transport.[43] As one may expect, the use of the bulk GaN substrate is the ideal solution to realize vertical geometry device. Utilization of the backside ohmic contact will eliminate the need for mesa etching which is frequently employed in the fabrication of vertical devices on conventional structure such as GaN epilayer on sapphire substrates. In this letter, we report on the fabrication process and device characteristics of vertical-geometry Schottky-type UV photodetectors based on a bulk n^- GaN substrate with low dislocation density ($<5\times10^6$ cm^{-2}). The devices showed an extremely low dark current and high UV/Visible rejection ratio.

5.2 Experiment

The free-standing GaN substrates were synthesized by a hydride vapor phase epitaxy process. They are 10×10 mm^2 in dimension and ~460 μm thick. The capacitance-voltage (C-V) measurements showed an unintentional n-doping level of $\sim7\times10^{15}$ cm^{-3}. The Ga-face (front side) was polished and a typical dislocation density measured by etch-pit method is $<5\times10^6$ cm^{-2}. A full area ohmic contact of Ti (50 nm)/Al (100 nm) was sputtered on the backside and subsequently annealed at 750 °C in N_2 atmosphere for 30 s. The circular semi-transparent Schottky contacts with 150 μm in diameter and 20 nm thick Ni (with 7% Vanadium) layer were deposited on the front side by DC magnetron sputtering. After Schottky contact deposition, some samples are annealed at 300 °C, 500 °C or 700 °C in N_2 atmosphere for 30 s.

The spectral responsivity measurements were performed with a 150 W Xe arc lamp and a monochromator. A 325 nm line from a He-Cd laser (Kimmon Electric) was used to study the power-dependent photocurrent measurement. The incident power was calibrated by a UV-enhanced Si photodetector. Photocurrent and dark current were measured using Keithley 6487 picoammeter and Keithley 6517 electrometer, respectively. A broadband UV light from the deuterium/tungsten combo light source (DT 1000CE, Analytical Instruments, Inc.) was used for photocurrent measurement.

5.3 Results and discussion

The dark current-voltage (I-V) characteristics for Ni/GaN Schottky photodetectors with as-deposited and annealed Schottky contacts are shown in Figure 5.1.

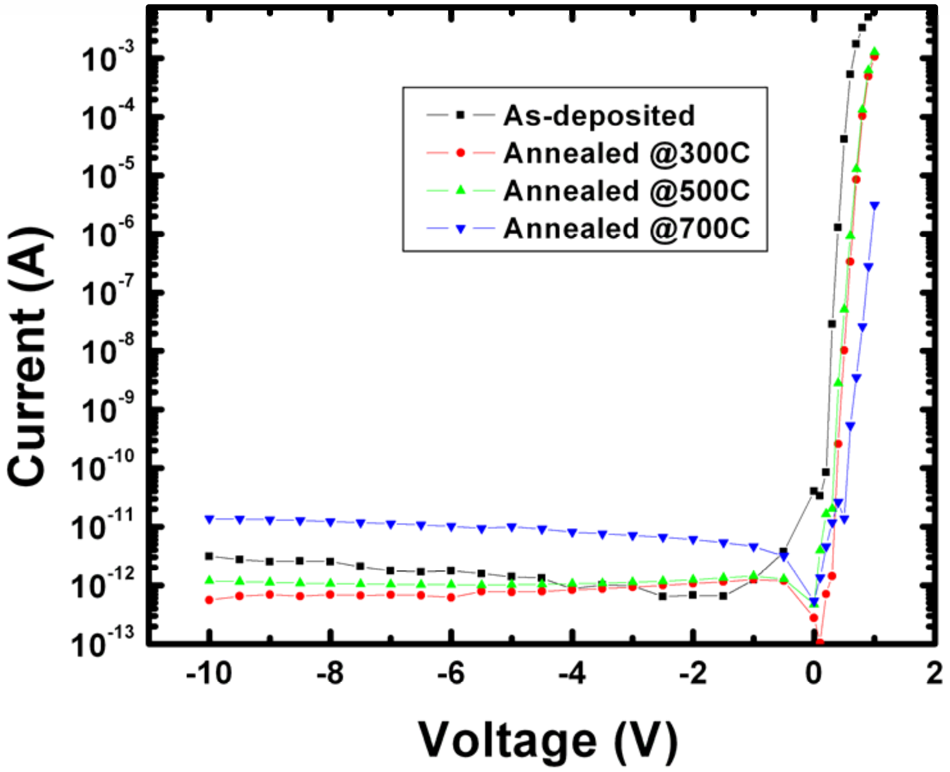


Figure 5.1: The dark current-voltage (I-V) characteristics for Ni/GaN Schottky photodetectors with as-deposited and annealed Schottky contacts

According to thermionic emission theory, the I-V relation for a Schottky diode for forward bias $V>3kT/q$ can be expressed as

$$I = I_0 \exp(qV / nkT) \tag{5.1}$$

where I_0 is the saturation current given by

$$I_0 = AA^*T^2 \exp(-q\Phi_b / kT) \tag{5.2}$$

and n is the ideality factor, V is the forward bias voltage, T is the absolute temperature, q is the electron charge, k is the Boltzmann constant, Φ_b is the effective Schottky barrier height, A is the diode area, and A^* is the effective Richardson constant for n-GaN. In our analysis, we have assumed that A^* is 26.4 $\mathrm{Acm^{-2}K^{-2}}$. The Φ_b for the unannealed device is 0.89 eV, but increased to 1.09 eV, 0.97 eV and 1.02 eV for the device annealed at 300 °C, 500 °C and 700 °C, respectively. Guo *et al.* has attributed the increase in Φ_b for annealed Schottky contact to the formation of nickel nitrides such as Ni_3N and Ni_4N at the interface between Ni and GaN.[145] Judging from the forward conduction characteristics observed, it is conjectured that the formation of such interfacial compounds may also increase the resistance of the Ni film.

The dark current measured at -10 V is 3.12 pA for the device with as-deposited Schottky contacts. In the case of the device with the Schottky contacts annealed at 300 °C, the dark current measured at -10 V reduced to 0.56 pA, which is the lowest value reported for GaN-based Schottky-type photodetectors. We ascribe such a low dark current to the low dislocation density of the substrate and an optimized Ni/GaN Schottky contact characteristics through low temperature annealing. However, for the devices with Schottky contacts annealed at 700 °C, the dark current measured at -10 V increased to 13.7 pA, indicating a degradation of the Schottky contact. These devices exhibit an ideality factor of ~2, which indicates a severe deviation from thermionic emission model after high temperature annealing.

The devices annealed at 300 °C were used for further analysis. Figure 5.2 shows the spectral response of these devices. In order to avoid the generation of internal gain, the measurements were conducted at zero bias.[146] The incident power density was set at ~80 mW/m^2 for each monochromatic light.

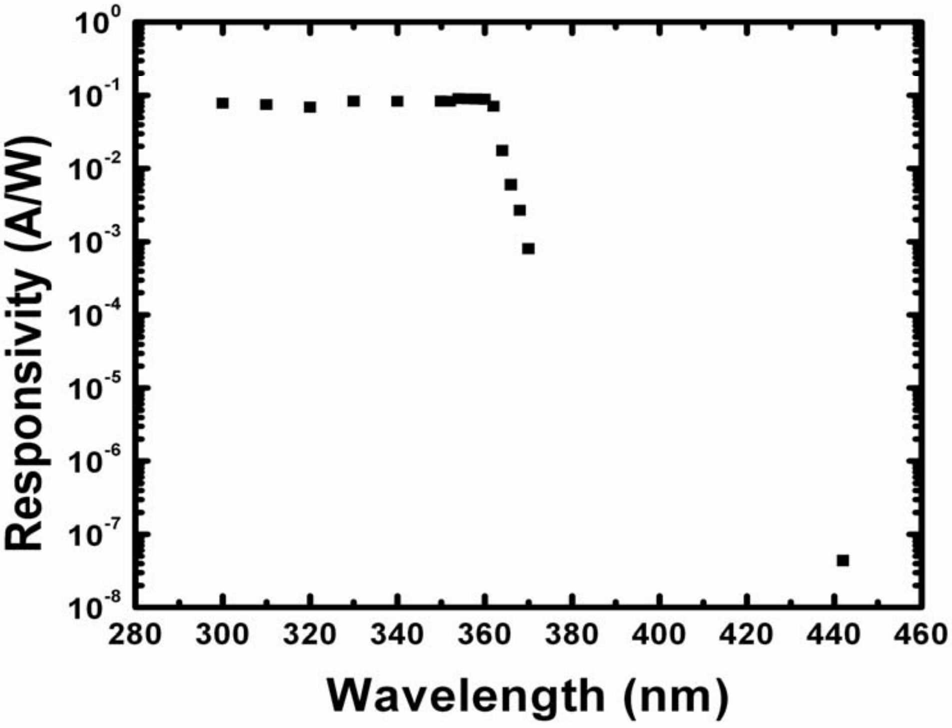


Figure 5.2: The spectral response as a function of wavelength.

Upon illumination of light with energies higher than the band gap of GaN, a fairly flat responsivity with a value of ~0.09 A/W was observed. A sharp cutoff occurs at around 362 nm, which corresponds to the band gap. Due to the relatively low irradiance for the Xe lamp, it is not possible to detect any photoresponse for wavelength above 370 nm. Therefore, He-Cd laser (442 nm) was used for illumination to obtain the photoresponse in the visible spectral region. Under the irradiance of ~2.24 kW/m^2, the responsivity at 442 nm was found to be 4.37×10^{-8} A/W. By taking the ratio of responsivity at 360 nm to that at 442 nm, an UV/Visible contrast of 2×10^6 was obtained, which is among the highest reported value for GaN UV photodetectors. It is well known that crystal defects or impurities can create energy levels within the bandgap, which will reduce the visible-blindness for UV photodetectors. The excellent visible-blindness of our photodetector was mainly attributed to the reduced concentration of defects and impurities in the bulk GaN substrate.

In order to study the incident optical power dependent photoresponse, the optical power from a He-Cd laser (325 nm) was controlled using sets of neutral density filters. Again the photocurrent was measured at zero bias to avoid internal gain. Figure 5.3 shows the plot of photocurrent *vs.* optical power density. As shown in the figure, the photocurrent increases linearly with incident power in the range measured (50 mW/m^2-2.2 kW/m^2), indicating an independence of responsivity on optical power.

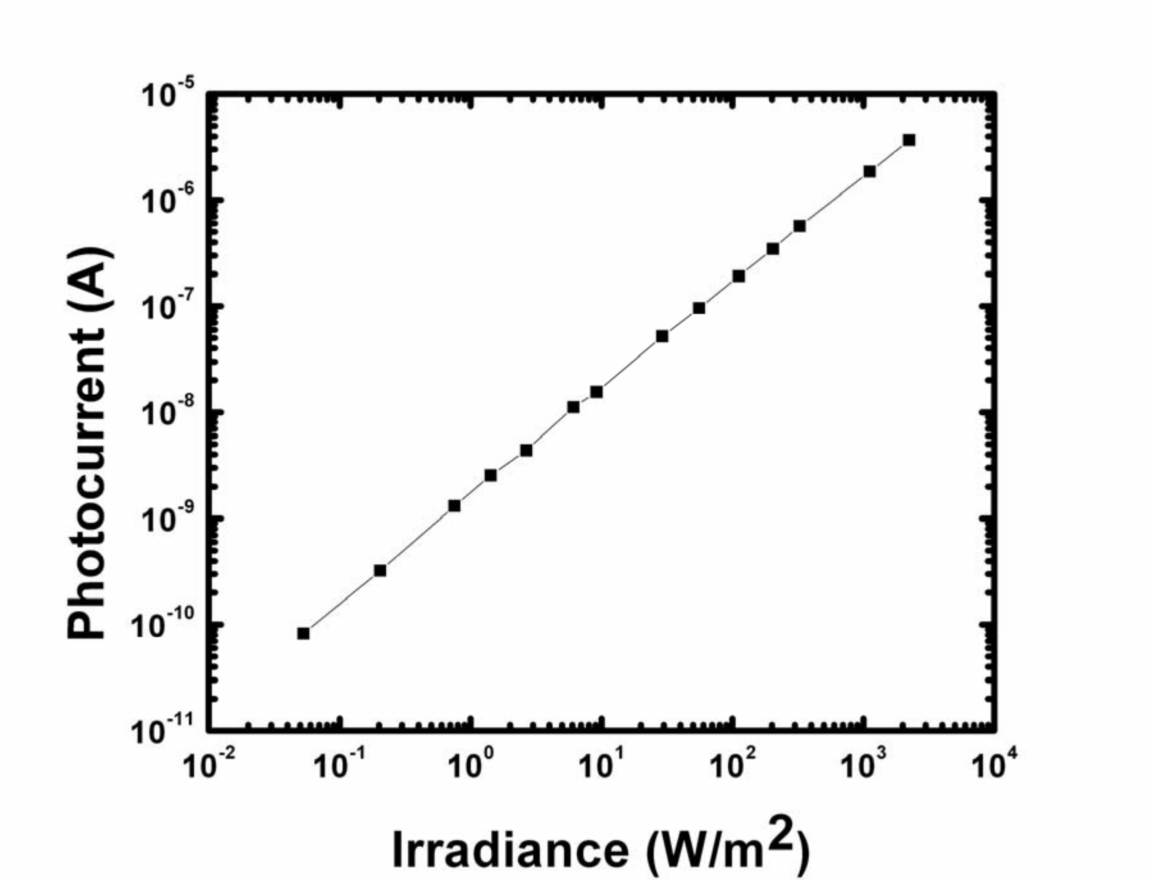


Figure 5.3: The plot of photocurrent *vs*. optical power density.

Figure 5.4, shows the I-V characteristics for dark current and photocurrent under broadband UV illumination. An open-circuit voltage determined from the plot is 0.3 V, and this device may find application in UV photovoltaics (solar cells).

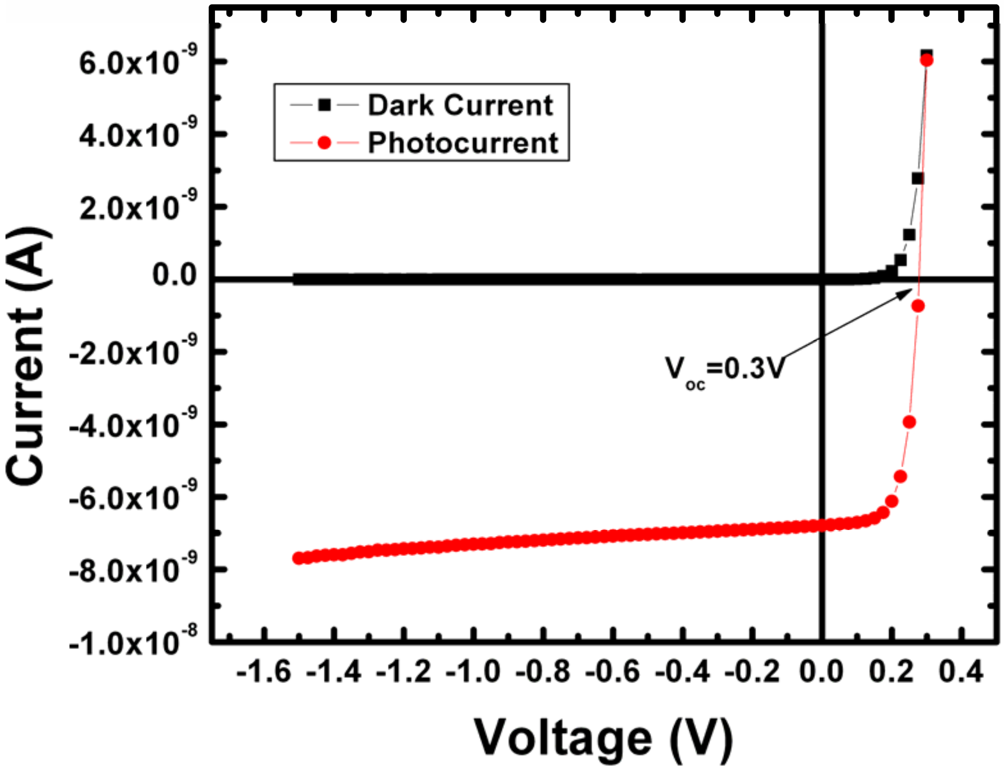


Figure 5.4: The I-V characteristics for dark current measurement and photocurrent measurement under broadband UV illumination.

5.4 Conclusion

In summary, we have fabricated vertical-geometry Schottky-type UV photodetectors based on a bulk GaN substrate, and have investigated the device characteristics. The device exhibits an ultralow dark current of 0.56 pA at -10 V, which was attributed to the low dislocation density of the substrate and an optimized Ni/GaN Schottky contact through low temperature annealing. The spectral responsivity measurement showed a high UV/Visible rejection ratio of 2×10^6. The responsivity was found to be independent of incident power in the range measured (50 mW/m^2-2.2 kW/m^2). An open circuit voltage of 0.3 V was obtained under a broadband UV illumination.

CHAPTER 6

METAL-OXIDE-SEMICONDUCTOR CAPACITORS FABRICATED ON A BULK GAN SUBSTRATE USING THERMALLY GROWN OXIDE

6.1 Introduction

GaN has received much attention recently in the area of optoelectronics, especially in the fabrication of high-efficiency blue/green and ultraviolet (UV) light-emitting diodes (LEDs). Its fundamental physical properties, such as a large band gap (3.4 eV), high breakdown field (4 MV/cm) and high electron saturation velocity (3×10^7 cm/s), also make it promising for high power, high temperature applications. GaN metal-semiconductor field effect transistors (MESFETs) and GaN/AlGaN heterostructure field effect transistors (HFETs) with promising device characteristics have been fabricated and their potential for high power, high temperature application have been demonstrated.[147-149] However, one of the major factors that limit the performance and reliability of these devices for high power application is their relatively high gate leakage. The gate leakage problem for Schottky contacts is further deteriorated at high temperature.

To avoid this problem, significant progresses have been made on the metal-oxide-semiconductor (MOS) or metal-insulator-semiconductor (MIS) structure. The use of an insulated gate is expected to reduce the gate leakage and power consumption. Ren *et al.*[150] reported the fabrication and electrical characteristics of the first GaN-based metal-oxide-semiconductor field effect transistor (MOSFET) using a gate dielectric comprised of deposited $Ga_2O_3(Gd_2O_3)$. Since then, several approaches have been employed to develop GaN-based MOS or MIS system using deposited insulators, such as SiO_2,[151, 152] Si_3N_4,[153] MgO,[154] Sc_2O_3,[155] Ta_2O_5,[156] and Al_2O_3.[157] One of the bottlenecks of these structures for MOSFET application is the relatively high interface trap density at the insulator/GaN interface, typically in the order of mid 10^{11} eV^{-1} cm^{-2} to 10^{12} eV^{-1} cm^{-2}.

Thermal oxidation has been the most useful method for oxide growth as a gate dielectric in Si-based MOS technology due to its advantages such as low interface trap density and fabrication simplicity. Despite a relatively higher interface trap density than SiO_2/Si interface, thermal oxidation is still the preferred method for SiC-based MOS technology. However, for some compound semiconductors, thermal oxidation is much more complicated than that of Si. For example, the growth of high quality thermal oxides for GaAs is hindered by the competing formation of Ga_2O_3 and As_2O_3 as well as by the presence of excess elemental As at the oxide/GaAs interface, which results in a poor property of the native thermal oxides and interfaces.[158] Fortunately, for GaN, nitrogen and corresponding oxides are volatile and only Ga-oxide will be formed. However, care must be taken as for the oxidation temperature. No or minimal oxide growth is observed for temperature below 750 °C.[159] On the other hand, GaN is thermally unstable at temperature above 1000 °C.[88]

Recently, there have been few initial reports of GaN MOS structure based on a thermally oxidized GaN epitaxy layer on a sapphire substrate.[160, 161] The thermally grown β-Ga_2O_3/GaN interface indeed displayed a lower interface trap density than other deposited insulator/GaN interfaces by more than one order of magnitude. It looks promising for GaN-based MOSFET application.

Recent development in Hydride Vapor Phase Epitaxy (HVPE) technology has enabled the success of growing free-standing GaN wafers with a very low dislocation density ($<5\times10^6$ cm^{-2}). MOS capacitors fabricated on a bulk GaN substrate using thermally grown gallium oxide has not yet been reported. Therefore, in this paper, we report a comprehensive investigation of the oxidation kinematics, material characterization, surface analysis, wet or dry etching as well as electrical characterization of thermally grown Ga_2O_3 on a bulk GaN substrate.

6.2 Thermal oxidation of bulk GaN substrates

The free-standing GaN substrates used in this study were synthesized by a hydride vapor phase epitaxy (HVPE) process. The substrates are 10×10 mm^2 in dimension and

~265 μm thick. The C-V measurement showed an unintentional n-doping level of ~5.5×10^{16} cm^{-3}. The Ga- side (front side) was polished with a typical dislocation density of 5×10^{6} cm^{-2}.

Prior to oxidation, the samples were ultrasonically cleaned sequentially in trichloroethylene (TCE), acetone, and methanol for 5 minutes each, then dipped into a heated HCl: H_2O (1:1) (~100 °C) for 10 minutes, and then rinsed in deionized water and blown dry using N_2.

Before loading the samples into the horizontal quartz tube furnace, the furnace temperature was stabilized at 300 degree below the designed oxidation temperature and the system was purged with dry O_2 for 15 minutes. Then the samples were placed in a quartz boat and transferred into the center of the quartz tube. They were kept there for 15 to 20 minutes to allow the sample temperature to equilibrate with the ambient. Then the furnace temperature was increased to the designed temperature at a rate of 5 °C /min. The oxidation was performed at 850 °C, 900 °C, 950 °C and 1000 °C with varying oxidation time (4-12 hours). Since the oxidation rate is negligible when below 750 °C, the temperature rising time was not counted in oxidation duration. The O_2 gas flow rate was maintained at 500 sccm for the entire process. After oxidation was completed, the samples were taken out from the tube and cooled to room temperature in air.

The oxidation rates at different temperatures are shown in Figure 6.1(a). The method used to determine the oxide thickness will be discussed in Section 6.3. The equations for the oxide growth on GaN powder have been described by Wolter *et al* as:[162]

$$\boldsymbol{I^n = k \cdot t} \tag{6.1}$$

$$\boldsymbol{n \cdot \ln I = \ln k + \ln t} \tag{6.2}$$

where *n* is the reaction order, *k* is the reaction rate constant, *t* is the oxidation time and *I* is the intensity of X-ray diffraction peak, which is related to the oxide volume formed. If *n* equals 1, the oxidation is under interfacial reaction-controlled mechanism. If *n* equals 2, the oxidation is under diffusion-controlled mechanism. Unlike GaN powder, the oxide thickness formed on bulk GaN substrate can be easily determined. Therefore, a direct measurement of oxide thickness *T* is used to replace the diffraction intensity *I* in the above equations.

Figure 6.1(b) displayed a plot of *ln(T) vs. ln(t)* to determine the reaction order *n*. Single linear region was found for samples oxidized at 850 °C or 900 °C. However, the reaction orders, which equal the inverse of the slope, differ from each other. The value of *n* increases from 0.9 at 850 °C to 1.3 at 900 °C, which indicates dominance of interfacial reaction-controlled oxidation mechanism at 850 °C and a combination effect of interfacial reaction-controlled and diffusion-controlled mechanism at 900 °C during the time scale measured. The combination effect is even more obvious for oxidation at 950 °C, where there is a clear transition from interfacial reaction-controlled (*n*=1.1) to diffusion-controlled mechanism (*n*=2.8).

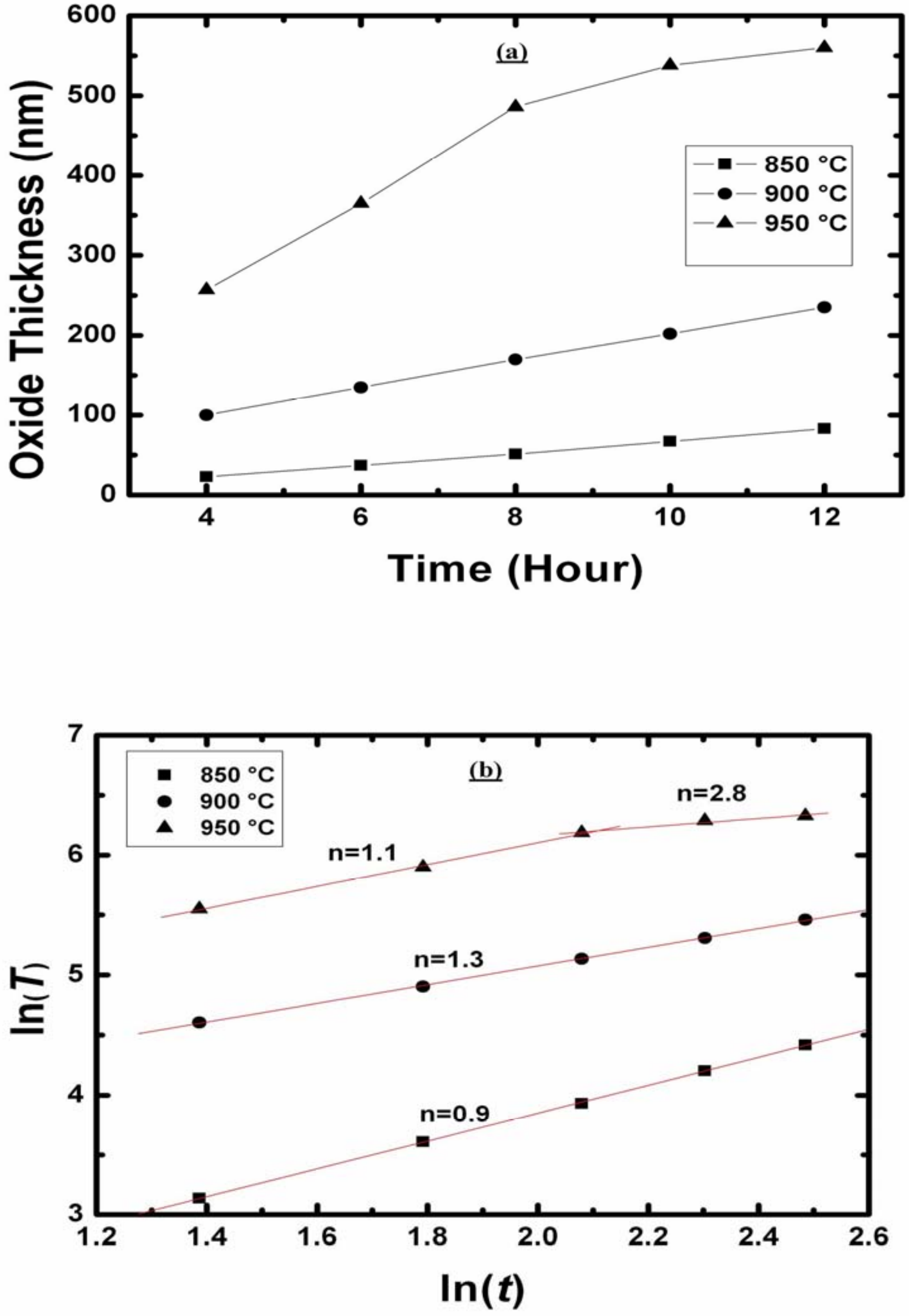


Figure 6.1: (a) The oxidation rates at different oxidation temperatures. (b) A plot of ln(T) *vs* ln(t) from Figure 6.1(a) to determine the reaction order *n* in equation (6.2).

The structural and chemical properties of the oxidized samples were analyzed by X-ray diffraction (XRD), Auger electron spectroscopy (AES), X-ray photoelectron spectroscopy (XPS) and Scanning electron microscopy (SEM) measurements.

Figure 6.2 shows the XRD pattern (θ-2θ scan) for the oxide which was grown on bulk GaN at 900 °C for 10 hours. In addition to the characteristic diffraction peaks for GaN (002) and (004), additional peaks that are associated with the thermally grown oxide were observed. Among them, the strongest two peaks were identified as the monoclinic β-Ga_2O_3 (-1 1 3) and (-3 0 6) by comparing with *Powder diffraction file*, **11-370**. Similar peak positions were also observed on samples oxidized at 850 °C for 12 hours or 950 °C for 4 hours. β-Ga_2O_3 is believed to be the most thermodynamically stable phase of all possible allotropes.[163] Instead of showing all peaks representative of β-Ga_2O_3, the peaks present and their intensities were indicative of a preferential orientation along some particular crystallographic directions. Our result is in agreement with a previous observation on thermally oxidized GaN epilayer in dry oxygen.[164]

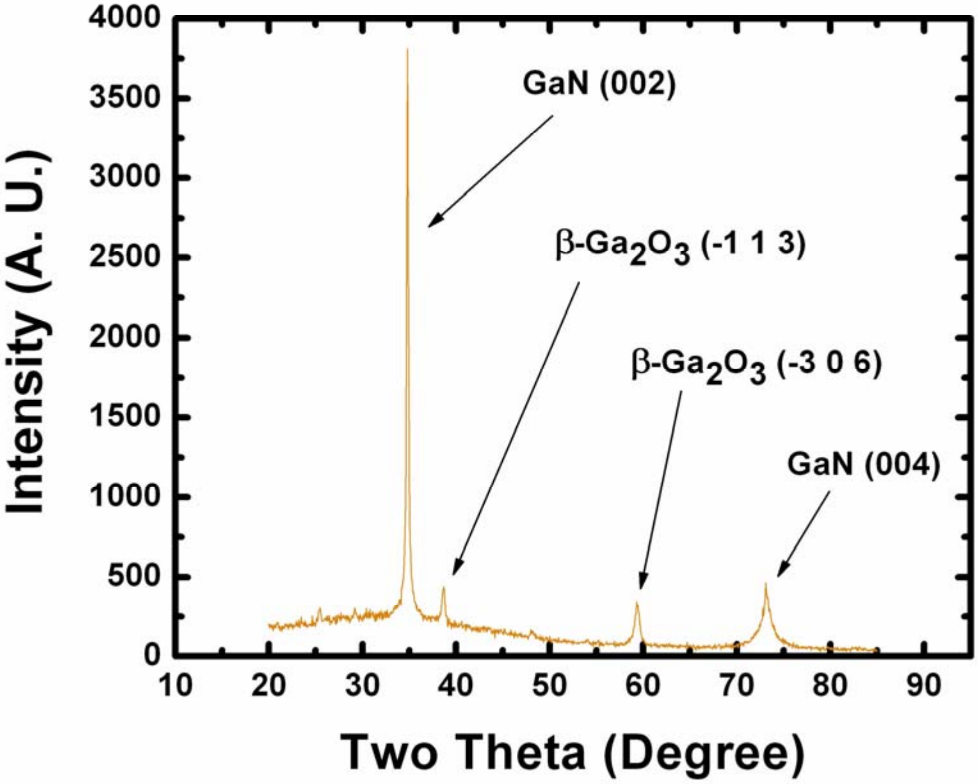


Figure 6.2: The XRD spectrum of the β-Ga_2O_3 formed on a bulk GaN substrate after oxidized at 900 °C for 10 hours.

Figure 6.3 shows the AES and XPS spectra of the same sample used for XRD. The AES and XPS measurements were performed in a load-locked Kratos XSAM 800 surface analysis system equipped with a standard Mg *Ka* x-ray source and a hemispherical energy analyzer. The base pressure of the analysis chamber was approximately 1×10^{-10} Torr. Prior to analysis, the sample surface was cleaned by light 3 keV Ar^+ ion sputtering which removed the adventitious adsorbed C, O, and N atoms present on all surfaces exposed to atmosphere. According to the AES spectra in Fig 6.3(a), there is no measurable N on the surface; the surface consists entirely of Ga and O atoms. In order to determine the specific Ga-O surface compound present, a high-resolution XPS spectrum was recorded over the Ga $2p_{3/2}$ feature. As shown in Fig 6.3(b), the measured Ga $2p_{3/2}$ binding energy was measured to be 1118.1 eV, which is in excellent agreement with previous photoemission studies on a standard specimen of Ga_2O_3.[165] The best peak fit deconvolution of the Ga $2p_{3/2}$ peak indicated the presence of a single elemental peak. The absence of peak shoulders indicated that the surface was totally Ga_2O_3 and not a combination with Ga (elemental) and other types of gallium oxide. The lack of N signal in both AES and XPS spectra preclude the existence of surface GaN.

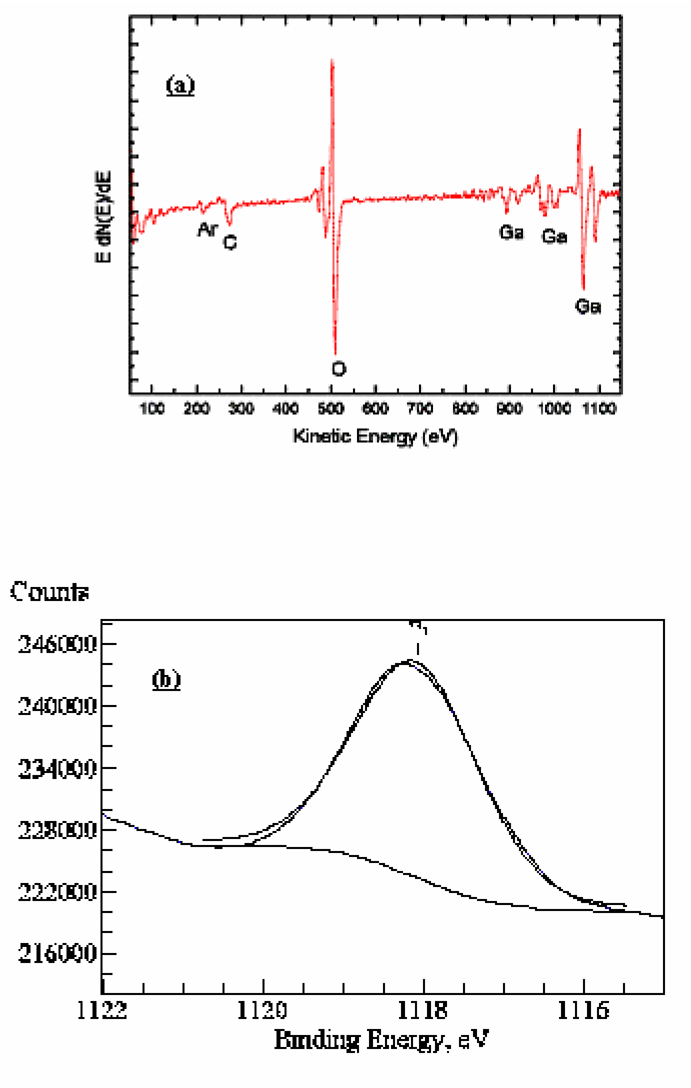


Figure 6.3: (a) AES spectra of the gallium oxide surface after 3.0 keV sputter cleaning. (b) High-resolution XPS spectra of the gallium oxide surface over the Ga $2p_{3/2}$ peak showing the raw photoemission data (black) and best-fit deconvolution (blue).

Figure 6.4 shows the SEM images of the as-grown Ga_2O_3 surfaces oxidized at different temperatures. The samples used in this measurement were oxidized at 850 °C, 900 °C, 950 °C or 1000 °C for 6 hours respectively. The oxide surface roughnesses were found to increase with oxidation temperatures. In particular, a much higher degree of roughness of the oxide formed at 1000 °C could be attributed to the decomposition of GaN.

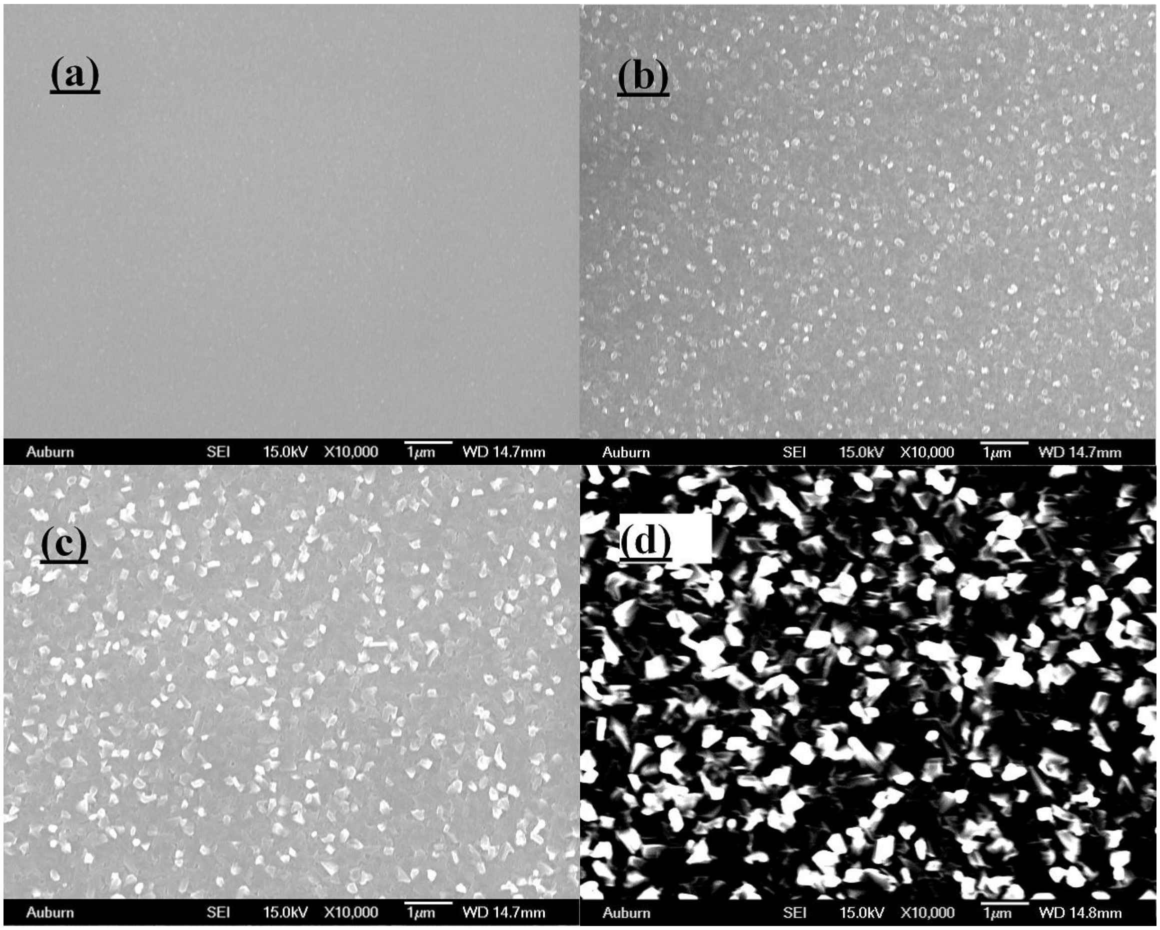


Figure 6.4: The SEM images of the β-Ga_2O_3 surfaces formed at the oxidation temperatures of (a) 850 °C, (b) 900 °C, (c) 950 °C and (d) 1000 °C.

After the oxide surface images were taken, the samples were soaked in a HCl:H_2O (1:1) solution at 250 °C for 15 minutes to remove the top oxide layer. Then the SEM images of the GaN surfaces were taken, as shown in Figure 6.5. Similar features were found for samples that had been oxidized at 850 °C or 900 °C. Except for some pitted area, which is caused by the preferential oxidation at dislocations, most of the GaN surfaces are smooth. However, for samples had been oxidized at 950 °C or 1000 °C, the GaN surfaces appear to be covered by many bubble-like small domains, resulting in very rough surfaces. These bubble-like domains seem not to be dislocation-related according to the relative positions of dislocations (the black dots) on the image, which means they are probably caused by the decomposition of GaN during the oxidation.

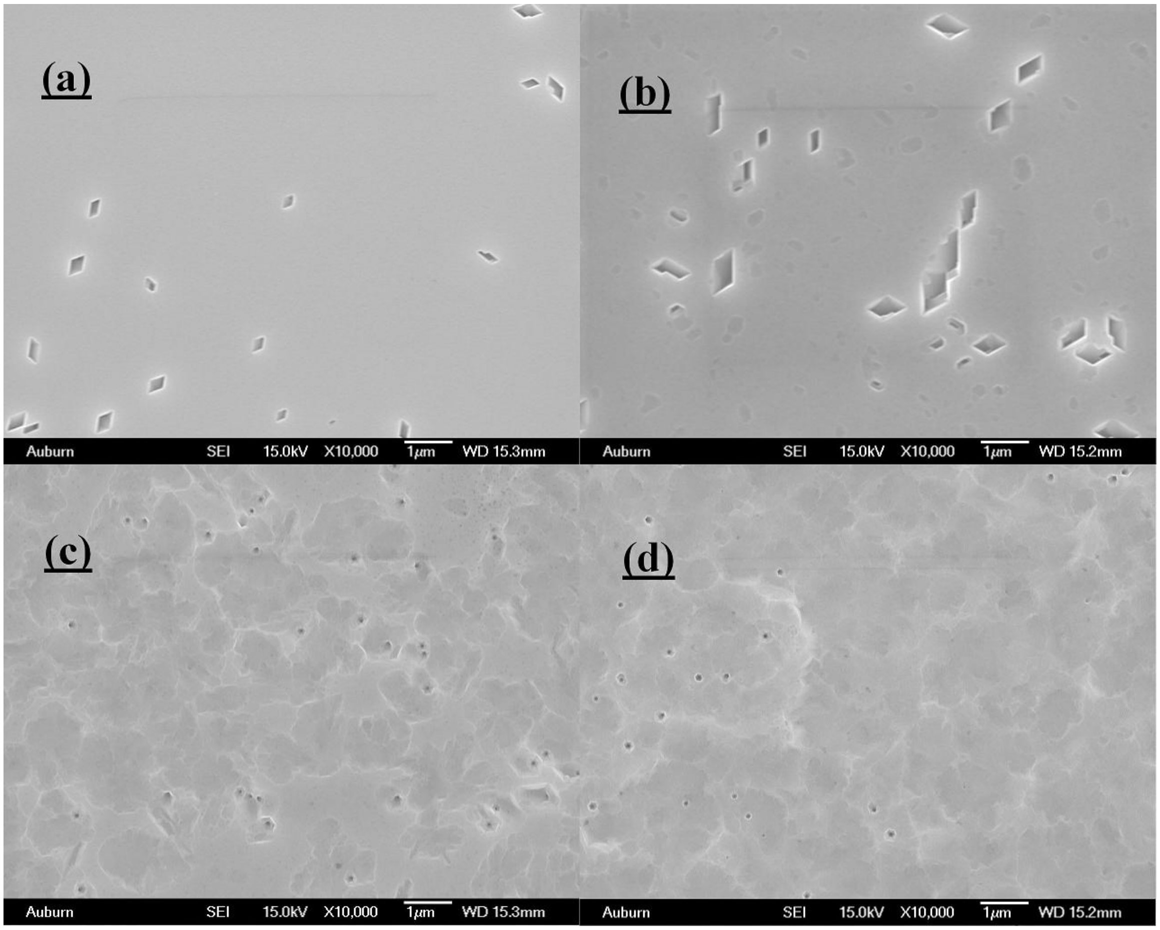


Figure 6.5: The SEM images of the GaN surfaces in Figure 5 after removing the top oxide layer which had been oxidized at (a) 850 °C, (b) 900 °C, (c) 950 °C and (d) 1000 °C.

In order to further examine the quality of the GaN surfaces after oxidation, Schottky diodes were fabricated on these bulk GaN substrates following our previously reported procedure.[142] As shown in Figure 6.6, the reverse leakage currents for Schottky diodes fabricated on samples that had been oxidized at 850 °C or 900 °C are as low as those fabricated on GaN substrates that have not been oxidized. However, much higher leakage currents were found for Schottky diodes fabricated on samples that had been oxidized at 950 °C or 1000 °C, indicating significant degradation of the GaN surfaces.

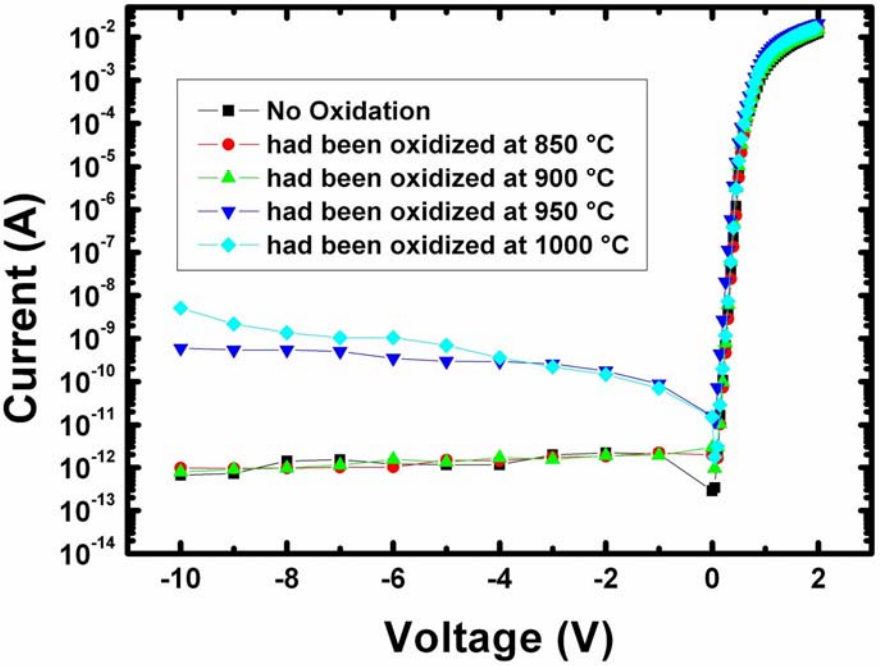


Figure 6.6: The I-V characteristics of the Schottky diodes fabricated on GaN surfaces in Figure 6.5

6.3 Wet-chemical and Reactive Ion etching of thermally grown Gallium Oxide

HCl-based solution is found to be effective removing native surface oxides on GaN layers.[166] It can also be used as wet chemical etchant for deposited $Ga_2O_3(Gd_2O_3)$ film on GaAs substrate.[167] So in this study, HCl:H_2O (1:1) solution was explored as a wet chemical etchant for thermally grown Ga_2O_3. However, there is no appreciable etch rate at room temperature. The etch rate was found to be too low to be used for device fabrication when the temperature was below 100 °C. Unfortunately, the conventional etch mask, such as photoresist, is not stable at temperatures above 100 °C, which makes the controlled etching at high temperature unfeasible. Significantly higher etch rate was found at 250 °C, but more research needs to be done to find a stable etch mask at this temperature.

RIE was performed using a home-built plasma processing system, equipped with a 13.65 MHz RF power supply RFX-600 (Advanced Energy) and an impedance matching unit ATX-600 (Advanced Energy). The plasma chemistries explored were 9 sccm NF_3 or 9 sccm Cl_2/Ar (1:2). The process pressure was ~60 mTorr for NF_3 and ~80 mTorr for Cl_2/Ar. Patterned Mo/Ni layer was used as the etch mask for NF_3 due to the fact that photoresist AZ5214E lacks of resistance to NF_3 discharges. Photoresist AZ5214E was used as etch mask for Cl_2/Ar after baking at 100 °C for 10 minutes following developing. The etch rates were determined from the depth of etched features measured by an Alpha-step profiler after removing the etch mask Mo/Ni using H_2O_2 or photoresist using acetone.

Figure 6.7 shows the etch rates as a function of RF power in the range of 20 W to 50 W.

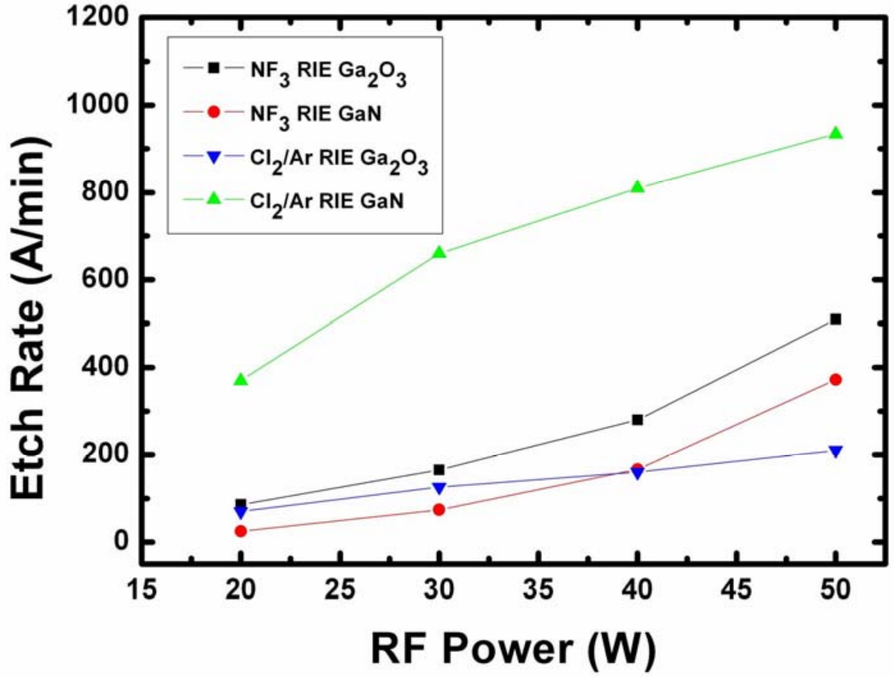


Figure 6.7: The RIE rates of GaN and β-Ga_2O_3 as a function of RF power by using NF_3 or Cl_2/Ar based discharges.

Cl_2-based discharge is commonly used to etch GaN.[168] However, the etch rate of Cl_2/Ar on Ga_2O_3 is much slower than that on GaN at the same etch condition. Therefore, there is no selectivity to remove Ga_2O_3 and stop on GaN by using Cl_2/Ar. Our result shows a much slower etch rate of NF_3 on GaN than that of Cl_2/Ar, probably due to the lower vapor pressure of the corresponding fluorides. However, NF_3 does show a higher etch rate on Ga_2O_3. The selectivity over GaN is ~3.5 at 20 W, but decreases with RF power.

To find out the optimal etching process, we used the following method to find the oxide thickness formed on GaN. First, patterned Mo/Ni layer was deposited as an etch mask. Then NF_3 was used to RIE the sample long enough so that it etches through the oxide and into the GaN. After dry etching, the Mo/Ni mask was removed and the depth of the etched feature, including the thickness of the oxide and GaN mesa, was measured using the Alpha-step profiler and recorded as T_1. Then the sample was soaked in an HCl:H_2O (1:1) solution at 250 °C long enough so that all the oxide was etched away. Finally, the GaN mesa depth was measured and recorded as T_2. The oxide thickness was calculated as $T=T_1-T_2$. The validity of this method to determine oxide thickness is confirmed by the cross-sectional SEM images (not shown) of the sample.

6.4 Electrical characteristics of the bulk GaN MOS capacitor

Some thermally oxidized samples were used to fabricate MOS capacitors. The fabrication processes are described as follows. First, the oxide grown on the backside was removed by RIE. Then a full backside ohmic contact of Ti (50 nm)/Al (100 nm) was deposited by sputtering, followed by rapid thermal annealing at 850 °C in N_2 atmosphere for 1 minute. Finally, circular contacts of Mo (100 nm thick) with 210 μm in diameter were sputtered onto the front oxide as gate electrodes. I-V measurements were performed using a Keithley 6487 picoammeter. The C-V measurements were performed at 1 MHz using a Keithley simultaneous hi-lo C-V system.

Three samples were used for this study. Sample A was oxidized at 900 °C for 6 hours, resulting in an oxide layer of 130 nm. Sample B was oxidized at 900 °C for 10 hours with an oxide layer of 200 nm. Sample C was oxidized at 950 °C for 4 hours with an oxide layer of 250 nm.

Figure 6.8 shows the I-V characteristics of MOS devices fabricated on sample A. The reverse current was as low as 1.5 pA at -10 V, which is due to the formation of space charge region in the GaN. The forward breakdown voltage was found to be 8.4 V, corresponding to a breakdown field of only 0.65 MV/cm. The relatively low oxide breakdown field and high gate leakage current is indicative of a poor insulating quality of β-Ga_2O_3 and a small conduction band offset between GaN and β-Ga_2O_3.[169]

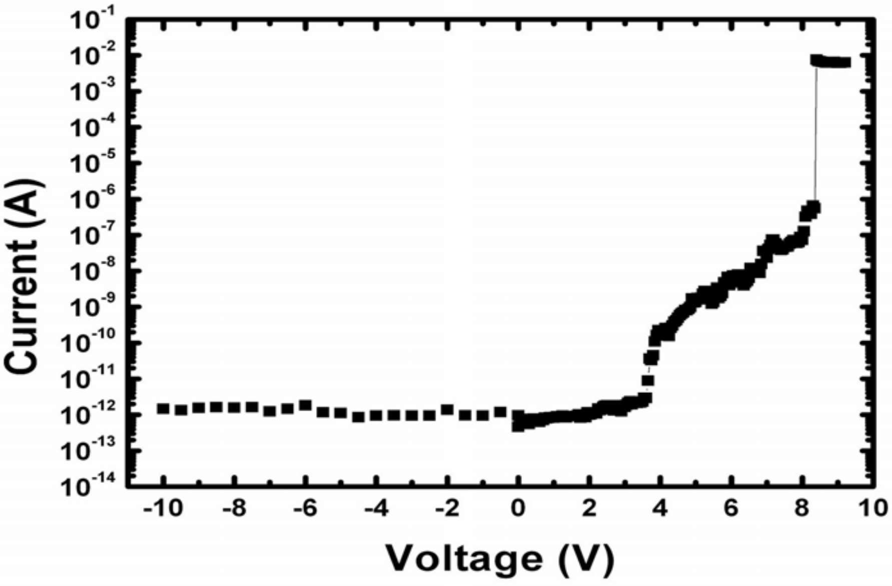
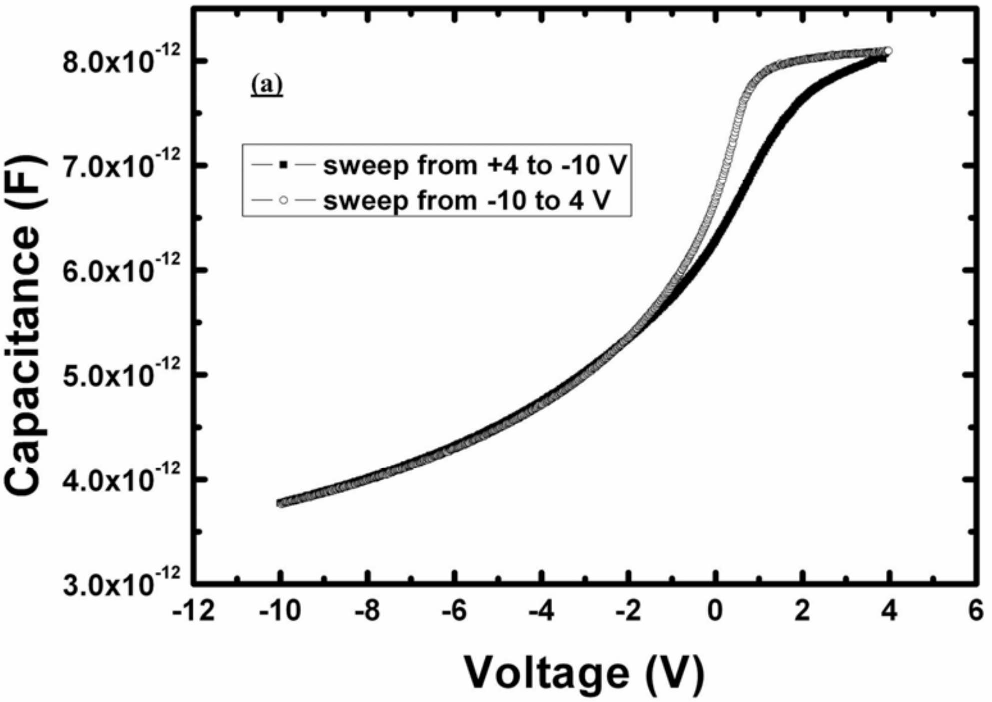


Figure 6.8: The I-V characteristics of a MOS capacitor with a 130-nm-thick thermally grown β-Ga_2O_3 at 900 °C.

Figure 6.9(a) shows the C-V characteristics of a MOS device fabricated on sample B under different sweep directions. A deep depletion behavior under reverse bias is clearly observed.


(a)
sweep from +4 to -10 V
sweep from -10 to 4 V
Capacitance (F)
8.0x10^{-12}
7.0x10^{-12}
6.0x10^{-12}
5.0x10^{-12}
4.0x10^{-12}
3.0x10^{-12}
-12
-10
-8
-6
-4
-2
0
2
4
6
Voltage (V)

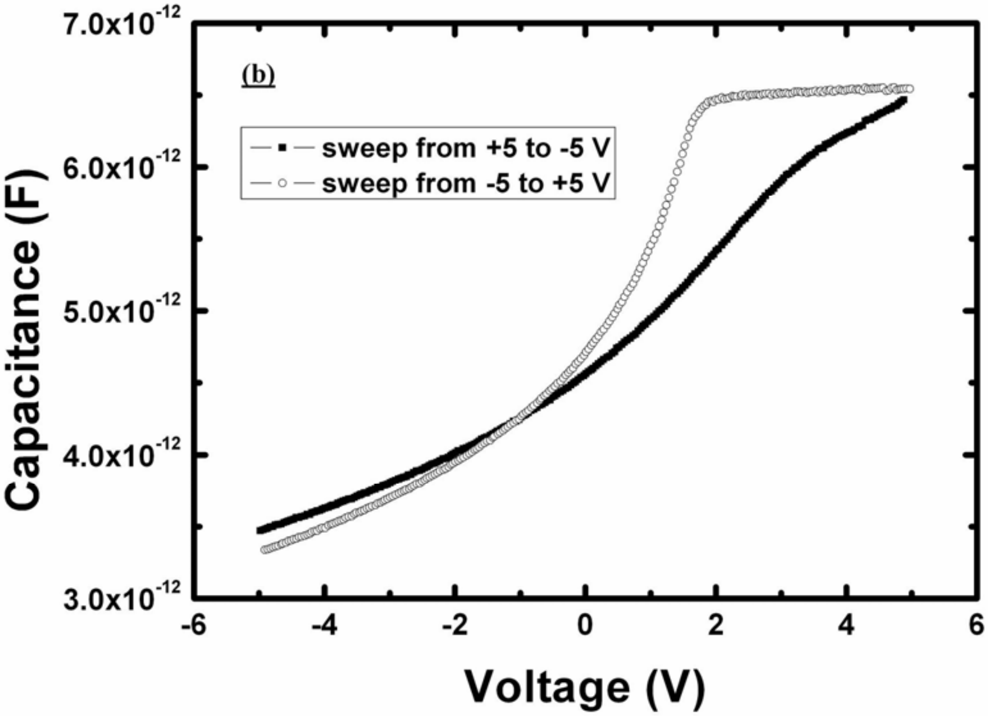

(b)
sweep from +5 to -5 V
sweep from -5 to +5 V
Capacitance (F)
7.0x10^{-12}
6.0x10^{-12}
5.0x10^{-12}
4.0x10^{-12}
3.0x10^{-12}
-6
-4
-2
0
2
4
6
Voltage (V)

Figure 6.9: (a) The C-V characteristics of a MOS capacitor with a 200-nm-thick thermally grown β-Ga_2O_3 at 900 °C under different sweep directions. (b) The C-V characteristics of a MOS capacitor with a 250-nm-thick thermally grown β-Ga_2O_3 at 950 °C under different sweep directions.

For GaN, the generation rate of minority carriers is extremely low at room temperature, which is due to its wide band gap of $E_g = 3.4\ eV$. According to the relation of $C_{ox} = A(\varepsilon_0 \varepsilon_{ox}) / T_{ox}$ where ε_0 is the permittivity in vacuum, ε_{ox} is the dielectric constant of the oxide, C_{ox} is the oxide capacitance, A is the area of the gate contact and T_{ox} is the oxide thickness, the calculated effective oxide thickness would be ~ 386 nm by using a tabulated ε_{ox} value of 10.2,[170] which is considerably thicker than the actual oxide layer of 200 nm. Nakano *et al.*[171] have found a broad intermediate Ga oxynitride layer with graded composition at the β-Ga_2O_3/GaN interface. According to our result, this Ga oxynitride layer may serve as an additional insulator layer in the MOS capacitor.

The effective oxide charge density ($Q_{eff} = Q_f + Q_{ot} + Q_m$) can be determined by the flatband voltage shift from the theoretical value, where Q_f is the fixed oxide charge density, Q_{ot} is the oxide trapped charge density at the oxide/GaN interface and Q_m is the mobile ionic charge density at the oxide/GaN interface.

To determine the experimental flatband voltage (V_{FB}), it is necessary to calculate the flatband capacitance (C_{FB}) by using equations:

$$C_{FB} = C_{FBs} \cdot C_{ox} /(C_{FBs} + C_{ox}) \tag{6.3}$$

$$C_{FBs} = \varepsilon_{GaN} \varepsilon_0 A / \lambda \tag{6.4}$$

$$\lambda = \sqrt{\varepsilon_{GaN} \varepsilon_0 kT / q^2 N_D} \tag{6.5}$$

where C_{FBs} is the flatband capacitance of GaN, $\varepsilon_{GaN} = 9$ is the dielectric constant of GaN, λ is the Debye length of the n-type GaN, k is the Boltzmann constant, T is the absolute temperature, q is the electron charge and $N_D = 5.5 \times 10^{16}\ cm^{-3}$ is the free electron concentration of the n-type bulk GaN substrate.

The calculated flatband capacitance (C_{FB}) is 7.66 pF, corresponding to a flatband voltage V_{FB}^{d} of 0.7 V when sweeping from deep depletion to accumulation and V_{FB}^{a} of 2 V when sweeping from accumulation to deep depletion. The theoretical flatband voltage (V_{FB}^{0}) is given by:

$$V_{FB}^{0} = \phi_{MS} / q \tag{6.6}$$

$$\phi_{MS} = \phi_M - [\chi + E_g / 2 - (kT / q)\ln(N_D / n_i)] \tag{6.7}$$

where ϕ_{MS} is work function difference between metal and semiconductor, $\phi_M = 4.53\ eV$ is the metal work function for the metal (Mo), $\chi = 4.1\ eV$ is the electron affinity of GaN and $n_i = 2 \times 10^{-10}\ cm^{-3}$ is the intrinsic carrier concentration of GaN. The calculated theoretical flatband voltage (V_{FB}^{0}) is 0.31 V. Then the effective oxide charge density (Q_{eff}) was calculated to be a negative value of 9.1×10^{-9} C/cm^2 by using the following expression:

$$\boldsymbol{Q_{eff} = (V_{FB}^{0} - V_{FB}^{d})C_{ox} / A} \qquad (6.8),$$

which gives an effective oxide charge number density ($\boldsymbol{N_{eff} = Q_{eff} / q}$) of 5.7×10^{10} cm^{-2}. Here we used the experimental flatband voltage when sweeping from deep depletion to accumulation in order to minimize the effect of the charged interface traps when in accumulation. By definition, the fixed oxide charge density ($\boldsymbol{Q_f}$) should be positive. The negative value of the effective oxide charge density ($\boldsymbol{Q_{eff}}$) indicates the presence of a higher density of interface states and border oxide traps ($\boldsymbol{Q_{ot}}$) which are occupied by electrons.[172]

The sweeping direction induced hysteresis, according to the hysteresis loop direction, could be caused by charge injection into the oxide instead of by the displacement of mobile ions.[173] Similar hysteresis was also found in high frequency C-V measurements on SiO_2/GaN MOS capacitors and Chen *et al.*[152] have ascribed this hysteresis to the charging and discharging of electrons from the relatively shallow interfacial electron traps. The interfacial electron trap number density ($\boldsymbol{N_{it}}$) can be estimated by using the equation:[174]

$$\boldsymbol{N_{it} = |V_{FB}^{a} - V_{FB}^{d}| C_{ox} / qA} \qquad (6.9).$$

A low $\boldsymbol{N_{it}}$ value of 1.9×10^{11} cm^{-2} was obtained for our device.

However, care must be taken when interpreting this result. The above equation is based on the assumption that the trapped electron can be emitted to the conduction band when in deep depletion. However, the emission time constant for the interface states increases exponentially with the energy from the band edge. For a wide band gap semiconductor such as GaN, the emission time constants of deep interface states can be so long that almost no electrons can be emitted at room temperature. So this $\boldsymbol{N_{it}}$ value is only an estimation of the interfacial electron trap number density near the conduction band. And this $\boldsymbol{N_{it}}$ should also be differentiated from the commonly termed interface state density ($\boldsymbol{D_{it}}$) in the unit of eV^{-1}cm^{-2}.

Figure 6.9(b) shows the C-V characteristics of a MOS device fabricated on sample C. This device has a much higher effective oxide charge number density ($\boldsymbol{N_{eff}}$) of 1.61×10^{11} cm^{-2} and a higher near-conduction-band-edge interfacial electron trap number density ($\boldsymbol{N_{it}}$) of 4.08×10^{11} eV^{-1}cm^{-2} than those determined from the sample B, which is possibly caused by the degradation of the GaN surface at 950 °C.

In order to further study the interface state density ($\boldsymbol{D_{it}}$) of the Ga_2O_3/GaN MOS capacitors, we calculated the $\boldsymbol{D_{it}}$ using the Terman method.[175]

The Terman method was one of the first methods for determining $\boldsymbol{D_{it}}$. This method extracts $\boldsymbol{D_{it}}$ information by comparing the experimental high frequency C-V curve to the theoretical curve of an ideal MOS capacitor which is assumed to contain no interface traps. The validity of Terman method is based on the facts that the interface states do not respond to the high frequency (1 MHz) measurement signal but do follow the DC bias sweep quasi-statically. Therefore, the interface traps do not contribute any capacitance to the high frequency C-V curve, but they do cause the high frequency curve to stretch out along the gate bias axis. And this distortion in the shape of the high frequency C-V curve contains the information of interface state densities.

At high frequencies, the total capacitance is given by:

$$\boldsymbol{C_{HF} = \frac{C_s C_{ox}}{C_s + C_{ox}}} \qquad (6.10),$$

where $\boldsymbol{C_s}$ is the semiconductor surface capacitance and $\boldsymbol{C_{ox}}$ is the oxide capacitance. The equivalent circuit is a serial combination of $\boldsymbol{C_s}$ and $\boldsymbol{C_{ox}}$. The theoretical value of $\boldsymbol{C_s}$ for an n-type semiconductor of a known doping concentration is a function of the non-dimensional band bending $\boldsymbol{V_s}$, which is given by:[175]

$$\boldsymbol{C_s = \frac{C_{FBs}}{\sqrt{2}} \cdot Sgn(V_s) \cdot \frac{\exp(V_s) - 1}{[-(V_s + 1) + \exp(V_s)]^{\frac{1}{2}}}} \qquad (6.11).$$

Here the function $\boldsymbol{Sgn(V_s)}$ equals +1 if $\boldsymbol{V_s}$ is positive and it equals -1 if $\boldsymbol{V_s}$ is negative. The non-dimensional band bending $\boldsymbol{V_s}$ is related to the band bending $\boldsymbol{\psi_s}$ in electron volts by:

$$\boldsymbol{V_s = \frac{q\psi_s}{kT}} \qquad (6.12).$$

Therefore, a theoretical curve can be constructed with the high frequency capacitance $\boldsymbol{C_{HF}}$ as a function of the band bending $\boldsymbol{\psi_s}$. However, the experimentally measured high frequency capacitance $\boldsymbol{C_{HF}}$ is a function of gate bias $\boldsymbol{V_G}$. Thus, a $\boldsymbol{\psi_s}$ versus $\boldsymbol{V_G}$ relation can be obtained and this relationship contains all the information about the interface trap density in high frequency C-V measurements.

To construct this relationship, select an arbitrary V_G value from the experimental C-V curve, find the corresponding C_{HF}, then place this C_{HF} value on the theoretical curve and find the corresponding ψ_s. By repeating doing so, a full curve of V_G versus ψ_s can be constructed. Then the interface state density D_{it} can be determined by:[175]

$$D_{it} = \frac{C_{ox}}{q}[(\frac{d\psi_s}{dV_G})^{-1} - 1] - \frac{C_s}{q} \qquad (6.13).$$

For wide band gap semiconductors, the emission time for the interface traps deep inside the band gap can be so long that it does not follow the DC bias sweep quasi-statically. Therefore, the Terman method can only be applied to extract D_{it} near the conduction band edge.

The D_{it} near the conduction band edge was shown in Figure 6.10.

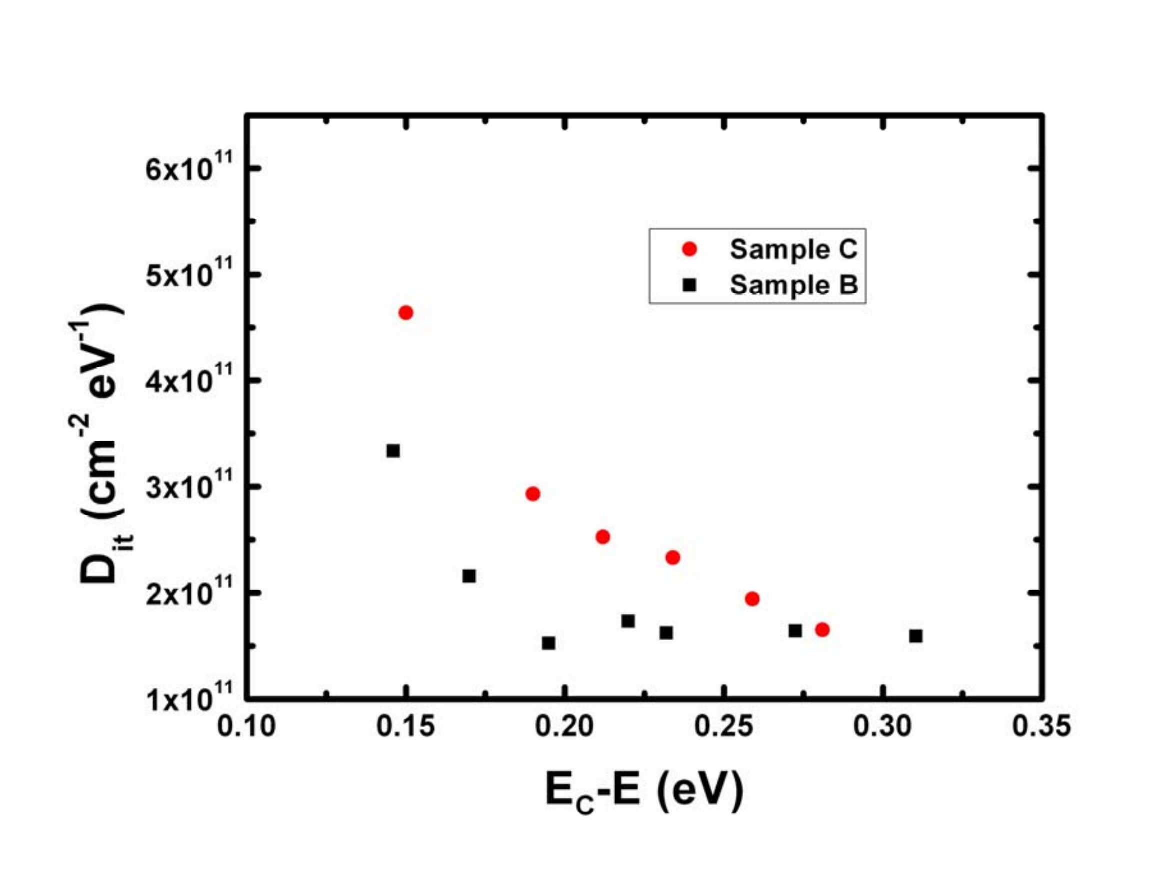


Figure 6.10: D_{it} determined by Terman method.

The D_{it} values are indeed in the low 10^{11} eV^{-1}cm^{-2} range for sample B. Sample C displayed a higher D_{it} value, which could be attributed to the degraded GaN surface at 950 °C. Further research needs to be done in order to examine the D_{it} value deep inside the band gap. However, compared to the reported D_{it} value obtained from the same methods as above,[154] the thermally grown Ga_2O_3 on bulk GaN does form an interface with lower interface state density than deposited insulator/GaN interfaces.

6.5 Conclusion

In summary, the oxidation of bulk GaN substrates in dry oxygen has been investigated. Based on XRD, AES and XPS measurements, the formation of a monoclinic β-Ga_2O_3 is confirmed. The dominant oxidation mechanism was interfacial reaction-controlled for oxidation at 850 °C during the time scale measured (4-12 hours). A combination effect of interfacial reaction-controlled and diffusion-controlled mechanism was found for oxidation at 900 °C and 950 °C. Appreciable etch rate of β-Ga_2O_3 in an HCl-based solution can only be achieved at high temperatures (>100 °C). Both NF_3 and Cl_2/Ar discharges can be used to etch β-Ga_2O_3 or GaN. NF_3 has a higher selectivity over β-Ga_2O_3 at lower RF power. The SEM images suggested a possible surface decomposition at oxidation temperatures of 950 °C and 1000 °C. Moreover, it is supported by the excess leakage currents of Schottky diodes fabricated on these surfaces. Despite a poor insulating property, the thermally grown β-Ga_2O_3 at 900 °C does form a high quality interface with GaN. The interface state density near the conduction band edge was estimated to be in the low 10^{11} $eV^{-1}cm^{-2}$ range However, higher oxidation temperature results in a higher interface state density, which might be caused by the GaN surface degradation. The thermally grown β-Ga_2O_3 displayed a low breakdown field of 0.65 MV/cm. Therefore, we suggest the use of gate stack (deposited oxide plus thermal oxide) for the fabrication of GaN-based MOS-type devices.

CHAPTER 7

SUMMARY AND FUTURE DIRECTION

In summary, we have fabricated high performance Schottky diodes using low-defect-density bulk GaN substrates. The bulk GaN substrate facilitates the fabrication of vertical geometry devices with a much simplified process. The full backside ohmic contact scheme, the higher electron mobility in vertical transport mode and the absence of the sapphire substrate greatly improve the forward current conduction of the bulk GaN Schottky diode. A high dose of Si implant on the backside can further reduce the ohmic contact resistance by forming a highly doped region at the GaN surface to facilitate electron tunneling. However, RIE treatment was not suitable for ohmic contact enhancement due to the fact that the highly defective thin layer at the backside of the substrate was etched away and this layer is essential to the ohmic contact formation for bulk GaN Schottky diodes.

Without any edge termination scheme or epilayer, high breakdown voltages have been achieved with small-size Schottky diodes. The devices also exhibited ultrafast reverse recovery characteristics. The temperature-dependent I-V measurements indicated a defect-assisted breakdown mechanism. Richardson constant was determined to be 35 $Acm^{-2}K^{-2}$ by using a modified Richardson plot.

A simulation of the breakdown characteristics of bulk GaN Schottky diodes have been carried out using MEDICI software. The simulation indicated a severe electric field crowding at the Schottky contact edge for unterminated devices. The field crowding at the Schottky contact edge led to a much lower breakdown voltage than that of the parallel plate device. SiO_2 field plates were found to be effective for reducing the field crowding at the Schottky contact edge, which resulted in a higher breakdown voltage of the device. The edge termination scheme parameters, such as oxide thickness and Schottky metal overlap, have been explored for optimal values. The fixed oxide charge at the oxide/GaN interface was found to play a detrimental role for breakdown voltages when its density exceeds 10^{12} cm^{-2}.

We have also demonstrated the fabrication and operation of Schottky-type ultraviolet photodetector using bulk GaN substrates. Extremely low dark currents have been achieved, which was attributed to the low dislocation density of the substrate and an optimized Ni/GaN Schottky contact by using rapid thermal annealing. The device displayed a reasonably good responsivity at zero bias, a good linearity of photocurrent with optical power density and a very high UV/Visible rejection ratio.

Thermal oxidation of bulk GaN was carried out at different temperatures for different oxidation times. The thermal oxide was identified to be β-Ga_2O_3 by XRD and

XPS studies. Oxidation rates and mechanism for different temperatures were analyzed. Wet chemical and reactive ion etching were explored under different etching conditions. SEM images indicated a possible surface decomposition for oxidation at 950 C or 1000 C. The MOS capacitors were fabricated using the thermally oxidized bulk GaN substrates. A low breakdown field was revealed by the I-V measurement, which was caused by the poor insulating nature of the β-Ga_2O_3 and a low conduction band offset between β-Ga_2O_3 and GaN. However, the C-V measurements indicated a reasonably good interface with a low effective oxide charge density and interface state density near the conduction band, as compared to those of deposited insulator/GaN interfaces.

Future work on bulk GaN Schottky diodes is needed in order to achieve high currents, without compromising the reverse breakdown voltages, for practical high power applications. As indicated by the strong dependence of reverse breakdown voltage on diode size and a negative temperature coefficient of breakdown voltage, current defect density level of the bulk GaN substrate still have significant impacts on the device performance. The device performance of large-size diode is significantly compromised due to the large number of defects within the device active area. So one of the efforts should be placed on further improving the GaN material quality, either by improving the bulk GaN substrate quality through HVPE process or growing high quality epitaxial layer on the bulk GaN substrate using MOCVD. Another effort could be placed on applying edge termination schemes, such as field plates. However, our work has shown that a high quality field plate is needed in order to accomplish the task. The sputtered SiO_2 field plates did not bring improvements to the reverse breakdown voltage due to the poor material quality. The desired deposition method should be CVD process. P-type floating guard rings and junction termination extension are supposed to be able to provide higher blocking voltage than field plates. However, much work is needed to achieve controllable p-type doing through implantation. MEDICI simulations on P-type floating guard rings and junction termination extension can be carried out to provide guidance to experimental work.

We have demonstrated that the thermally grown β-Ga_2O_3 can form a good interface with GaN, as compared to the deposited insulator/GaN interfaces. However the thermal gallium oxide was found to be leaky due to the poor insulating nature and a low conduction band offset with GaN. To overcome this problem, the stacked gate dielectric scheme can be employed. That is, to deposit an insulator layer on a thin thermal oxide layer to form a gate stack. The thermal oxide layer provides a good interface with GaN, and the insulator layer prevents the gate leakage. Once this scheme is implemented successfully, depletion mode metal oxide semiconductor field effect transistor (MOSFET) can be approached since the n^+ doping via Si implantation is proven to be feasible. Enhancement mode MOSFET or vertical MOSFET can also be approached once the p-type doping via implantation is achieved successfully.

BIBLIOGRAPHY

[1] S. N. Mohammad, A. A. Salvador and H. Morkoc, Proc. IEEE. **83**, 1306 (1995).

[2] H. Morkoc, S. Strite, G. B. Gao, M. E. Lin, B. Sverdlov and M. Burns, J. Appl. Phys. **76**, 1363 (1994).

[3] M. Trivedi and K. Shenai, J. Appl. Phys. **85**, 6889 (1999).

[4] M. Trivedi and K. Shenai, Proceeding of 33rd IEEE IAS Annual Meeting. **2**, 959 (1998).

[5] A. Witek, Diamond. Relat. Mater. **7**, 962 (1998).

[6] C. Mion, J. F. Muth, E. A. Preble and D. Hanser, Mater. Res. Soc. Symp. Proc. **892**, 0892-FF29-05.1.

[7] Y. Zhou, D. Wang, C. Ahyi, C. -C. Tin, J. Williams, M. Park, N. M. Williams and A. Hanser, Solid-State Electron. **50**, 1744 (2006).

[8] E. O. Johnson, IRE International Convention Record **13**, 27 (1965).

[9] B. J. Baliga, IEEE. Electron. Dev. Lett. **10**, 455 (1989).

[10] S. Kurtin, T. C. McGill and C. A. Mead, Phys. Rev. Lett. **22**, 1433 (1969).

[11] J. S. Foresi and T. D. Moustakes, Appl. Phys. Lett. **82**, 2859 (1993).

[12] M. E. Lin, Z. Ma, F. Y. Huang, Z. F. Fan, L. H. Allen and H. Morkoc, Appl. Phys. Lett. **64**, 1003 (1994).

[13] S. Ruvimov, Z. Liliental-Weber, J. Washburn, K. J. Duxstad, E. E. Haller, Z. -F. Fan, S. N. Mohammad, W. Kim, A. E. Botchkarev and H. Morkoc, Appl. Phys. Lett. **69**, 1556 (1996).

[14] B. P. Luther, S. E. Mohney, T. N. Jackson, M. Asif Khan, Q. Chen and J. W. Yang, Appl. Phys. Lett. **70**, 57 (1997).

[15] Z. Fan, S. N. Mohammad, W. Kim, O. Aktas, A. E. Botchkarev and H. Morkoc, Appl. Phys. Lett. **68**, 1672 (1996).

[16] J. Burm, K. Chu, W. A. Davis, W. J. Schaff, L. F. Eastman and T. J. Eustis, Appl. Phys. Lett. **70**, 464 (1997).

[17] S. J. Pearton, F. Ren, A. P. Zhang and K. P. Lee, Mater. Sci. Engi. **R30**, 55 (2000).

[18] Z. Z. Bandic, P. M. Bridger, E. C. Piquette, T. C. McGill, R. P. Vaudo, V. M. Phanse and J. M. Redwing, Appl. Phys. Lett. **74**, 1266 (1999).

[19] G. T. Dang, A. P. Zhang, F. Ren, X.. A. Cao, S. J. Pearton, H. Cho, J. Han, J. -I. Chyi, C. -M. Lee, C. -C. Chuo, S. N. George Chu and R. G. Wilson, IEEE. Trans. Electron. Devices. **47**, 692 (2000).

[20] T. G. Zhu, J. H. Lambert, B. S. Shelton, M. M. Wong, U. Chowdhury and R. D. Dupuis, Appl. Phys. Lett. **77**, 2918 (2000).

[21] A. P. Zhang, J. W. Johnson, F. Ren, J. Han, A. Y. Polyakov, N. B. Smirnov, A. V. Govorkov, J. M. Redwing, K. P. Lee and S. J. Pearton, Appl. Phys. Lett. **78**, 823 (2001).

[22] D. Kapolnek, X. H. Wu, B. Heying, S. Keller, B. P. Keller, U. K. Mishra, S. P.

DenBaars, and J. S. Speck, Appl. Phys. Lett. **67**, 1541 (1995).

[23] R. J. Roedel, A. R. von Neida, R. Causo and L. R. Dawson, J. Electrochem. Soc. **126**, 637 (1979).

[24] T. Suzuki and Y. Matsumoto, Appl. Phys. Lett. **26**, 431 (1975).

[25] S. D. Lester, F. A. Ponce, M. G. Craford and D. A. Steigerwald, Appl. Phys. Lett. **66**, 1249 (1995).

[26] J. Elsner, R. Jones, P. K. Sitch, V. D. Porezag, M. Elstner, Th. Frauenheim, M. I. Heggie, S. Oberg and P. R. Briddon, Phys. Rev. Lett. **79**, 3672 (1997).

[27] Y. Xin, S. J. Pennycook, N. D. Browning, P. D. Nellist, S. Sivanathan, F. Omnes, B. Beaumont, J. P. Faurie and P. Gibart, Appl. Phys. Lett. **72**, 2680 (1998).

[28] J. E. Northrup, Appl. Phys. Lett. **78**, 2288 (2001).

[29] E. G. Brazel, M. A. Chin and V. Narayanamurti, Appl. Phys. Lett. **74**, 2367 (1999).

[30] J. W. P. Hsu, M. J. Manfra, D. V. Lang, S. Richter, S. N. G. Chu, A. M. Sergent, R. N. Kleiman, L. N. Pfeiffer and R. J. Molnar, Appl. Phys. Lett. **78**, 1685 (2001).

[31] J. W. P. Hsu, M. J. Manfra, R. J. Molnar, B. Heying and J. S. Speck, Appl. Phys. Lett. **81**, 79 (2002).

[32] Y. Huang, X. D. Chen, S. Fung, C. D. Beling and C. C. Ling, J. Appl. Phys. **94**, 5771 (2003).

[33] K. Shiojima, T. Suemitsu and M. Ogura, Appl. Phys. Lett. **78**, 3636 (2001).

[34] N. G. Weimann, L. F. Eastman, D. Doppalapudi, H. M. Ng and T. D. Moustakes, J.

Appl. Phys. **83**, 3656 (1998).

[35] H. M. Ng, D. Doppalapudi, T. D. Moustakas, N. G. Weimann and L. F. Eastman, Appl. Phys. Lett. **73**, 821 (1998).

[36] D. C. Look and J. R. Sizelove, Phys. Rev. Lett. **82**, 1237 (1999).

[37] P. J. Hansen, Y. E. Strausser, A. N. Erickson, E. J. Tarsa, P. Kozodoy, E. G. Brazel, J. P. Ibbetson, U. Mishra, V. Narayanamurti, S. P. DenBaars and J. S. Speck, Appl. Phys. Lett. **72**, 2247 (1998).

[38] S. Keller, B. P. Keller, Y. -F. Wu, B. Heying, D. Kapolnek, J. S. Speck, U. K. Mishra and S. P. DenBaars, Appl. Phys. Lett. **68**, 1525 (1996).

[39] A. R. Arehart, B. Moran, J. S. Speck, U. K. Mishra, S. P. DenBaars and S. A. Ringel, J. Appl. Phys. **100**, 023709 (2006).

[40] S. J. Rosner, E. C. Carr, M. J. Ludowise, G. Girolami, and H. I. Erikson, Appl. Phys. Lett. **70,** 420 (1997).

[41] Y. Kato, S. Kitamura, K. Hiramatsu and N. Sawaki, J. Cryst. Growth. **144**, 133 (1994).

[42] M. Misra, A. V. Sampath, and T. D. Moustakas, Appl. Phys. Lett. **76**, 1045 (2000).

[43] O. Katz, V. Garber, B. Meyler, G. Bahir and J. Salzman, Appl. Phys. Lett. **80**, 347 (2002).

[44] Porowski, S. and I. Grzegory, *Growth of GaN single crystals under high nitrogen pressure*. Optoelectron. Prop. Semicond. Superlattices, **2**(GaN and Related Materials), p. 295-313. (1997).

[45] R. J. Molnar, W. Gotz, L. T. Romano and N. M. Johnson, J. Cryst. Growth. **178**, 147 (1997).

[46] T. Detchprohm, K. Hiramatsu, H. Amano and I. Akasaki, Appl. Phys. Lett. **61**, 2688 (1992).

[47] K. Naniwae, S. Itoh, H. Amano, K. Itoh, K. Hiramatsu and I. Akasaki, J. Cryst. Growth. **99**, 381 (1990).

[48] D. C. Look and R. J. Molnar, Appl. Phys. Lett. **70**, 3377 (1997).

[49] S. K. Mathis, A. E. Romanov, L. F. Chen, G. E. Beltz, W. Pompe and J. S. Speck, Phys. Stat. Sol. (a) **179**, 125 (2000).

[50] D. C. Reynolds, D. C. Look, B. Jogai, J. E. Hoelscher, R. E. Sherriff and R. J. Molnar, J. Appl. Phys. **88**, 1460 (2000).

[51] Z. -Q. Fang, D. C. Look, J. Jasinski, M. Benamara, Z. Liliental-Weber and R. J. Molnar, Appl. Phys. Lett. **78**, 332 (2001).

[52] W. Gotz, L. T. Romano, J. Walker, N. M. Johnson and R. J. Molnar, Appl. Phys. Lett. **72**, 1214 (1998).

[53] L. Chernyak, A. Osinsky, G. Nootz, A. Schulte, J. Jasinski, M. Benamara, Z. Liliental-Weber, D. C. Look and R. J. Molnar, Appl. Phys. Lett. **77**, 2695 (2000).

[54] S. Nakamura, M. Senoh, S. -I. Nagahama, N. Iwasa, T. Yamada, T. Matsushita, H. Kiyoku, Y. Sugimoto, T. Kozaki, H. Umemoto, M. Sano and K. Chocho, Appl. Phys. Lett. **73**, 832 (1998).

[55] M. K. Kelly, R. P. Vaudo, V. M. Phanse, L. Gorgens, O. Ambacher and M. Stutzmann, Jpn. J. Appl. Phys. **38**, L217 (1999).

[56] Y. Oshima, T. Eri, M. Shibata, H. Sunakawa, K. Kobayashi, T. Ichinashi and A. Usui, Jpn. J. Appl. Phys. **42**, L1 (2003).

[57] J. Jasinski, W. Swider, Z. Liliental-Weber, P. Visconti, K. M. Jones, M. A. Reshchikov, F. Yun, H. Morkoc, S. S. Park and K. Y. Lee, Appl. Phys. Lett. **78**, 2297(2001).

[58] P. Visconti, K. M. Jones, M. A. Reshchikov, F. Yun, R. Cingolani, H. Morkoc, S. S. Park and K. Y. Lee, Appl. Phys. Lett. **77**, 3743 (2000).

[59] F. Yun, M. A. Reshchikov, K. Jones, P. Visconti, H. Morkoc, S. S. Park and K. Y. Lee, Solid-State Electron. **44**, 2225 (2000).

[60] D. C. Look and J. R. Sizelove, Appl. Phys. Lett. **79**, 1133 (2001).

[61] M. A. Reshchikov, H. Morkoc, S. S. Park and K. Y. Lee, Appl. Phys. Lett. **78**, 3041 (2001).

[62] D. Huang, F. Yun, M. A. Reshchikov, D. Wang, H. Morkoc, D. L. Rode, L. A. Farina, C. Kurdak, K. T. Tsen, S. S. Park and K. Y. Lee, Solid-State Electron. **45**, 711 (2001).

[63] A. Saxler, D. C. Look, S. Elhamri, J. Sizelove, W. C. Mitchel, C. M. Sung, S. S. Park and K. Y. Lee, Appl. Phys. Lett. **78**, 1873 (2001).

[64] S. Nakamura, T. Mukai and M. Senoh, J. Appl. Phys. **71**, 5543 (1992).

[65] B. Heying, I. Smorchkova, C. Poblenz, C. Elsass, P. Fini, S. Den Baars, U. Mishra and J. S. Speck, Appl. Phys. Lett. **77**, 2885 (2000).

[66] J. W. Johnson, J. R. LaRoch, F. Ren, B. P. Gila, M. E. Overberg, C. R. Abernathy, J. -I. Chyi, C. C. Chuo, T. E. Nee, C. M. Lee, K. P. Lee, S. S. Park, Y. J. Park and S. J. Pearton, Solid-State Electron. **45**, 405 (2001).

[67] A. P. Zhang, J. W. Johnson, B. Luo, F. Ren, S. J. Pearton, S. S. Park, Y. J. Park and J. -I. Chyi, Appl. Phys. Lett. **79**, 1555 (2001).

[68] J. W. Johnson, A. P. Zhang, W. -B. Luo, F. Ren, S. J. Pearton, S. S. Park, Y. J. Park and J. -I. Chyi, IEEE. Tran. Electron. Dev. **49**, 32 (2002).

[69] Z. -Q. Fang, D. C. Look, P. Visconti, D. -F. Wang, C. -Z. Lu, F. Yun, H. Morkoc, S. S. Park and K. Y. Lee, Appl. Phys. Lett. **78**, 2178(2001).

[70] K. Ip, K. H. Baik, B. Luo, F. Ren, S. J. Pearton, S. S. Park, Y. J. Park and A. P. Zhang, Solid-State Electron. **46**, 2169 (2002).

[71] K. H. Baik, Y. Irokawa, J. Kim, J. R. LaRoche, F. Ren, S. S. Park, Y. J. Park and S. J. Pearton, Appl. Phys. Lett. **83**, 3192 (2003).

[72] Y. C. Chang, A. L. Cai, J. F. Muth, R. M. Kolbas, M. Park, J. J. Cuomo, A. Hanser and J. Bumgarner, J. Vac. Sci. Technol. A. **21**, 701 (2003).

[73] L. T. Romano, B. S. Krusor and R. J. Molnar, Appl. Phys. Lett. **71**, 2283 (1997).

[74] E. Valcheva, T. Paskova, P. O. A. Persson, L. Hultman and B. Monemar, Appl. Phys. Lett. **80**, 1550 (2002).

[75] B. Heying, X. H. Wu, S. Keller, Y. Li, D. Kapolnek, B. P. Keller, S. P. DenBaars and J. S. Speck, Appl. Phys. Lett. **68**, 643 (1996).

[76] K. G. Fertitta, A. L. Holmes, J. G. Neff, F. J. Ciuba and R. D. Dupuis, Appl. Phys. Lett. **65**, 1823 (1994).

[77] P. Kung, A. Saxler, X. Zhang, D. Walker, T. C. Wang, I. Ferguson and M. Razeghi, Appl. Phys. Lett. **66**, 2958 (1995).

[78] T. Kozawa, T. Kachi, H. Kano, Y. Taga, M. Hashimoto, N. Koide and K. Manabe, J. Appl. Phys. **75**, 1098 (1994).

[79] C. Kisielowski, J. Kruger, S. Ruvimov, T. Suski, J. W. Ager III, E. Jones, Z. Liliental-Weber, M. Rubin, E. R. Weber, M. D. Bremser and R. F. Davis, Phys. Rev. B. **54**, 17745 (1996).

[80] D. Wang, C. -C. Tin, J. R. Williams, M. Park, Y. S. Park, C. M. Park, T. W. Kang and W. -C. Yang, Appl. Phys. Lett. **87**, 242105 (2005).

[81] P. Perlin, J. Camassel, W. Knap, T. Taliercio, J. C. Chervin, T. Suski, I. Grzegory and S. Porowski, Appl. Phys. Lett. **67**, 2524 (1995).

[82] M. Park, J. J. Cuomo, B. J. Rodriguez, W. -C. Yang, R. J. Nemanich and O. Ambacher, J. Appl. Phys. **93**, 9542 (2003).

[83] M. Park, J. -P. Maria, J. J. Cuomo, Y. C. Chang, J. F. Muth, R. M. Kolbas, R. J. Nemanich, E. Carlson and J. Bumgarner, Appl. Phys. Lett. **81**, 1797 (2002).

[84] J. Neugebauer and C. G. Van de Walle, Appl. Phys. Lett. **69**, 503 (1996).

[85] T. Suski, P. Perlin, H. Teisseyre, M. Leszczynski, I. Grzegory, J. Jun, M. Bockowski, S. Porowski and T. D. Moustakas, Appl. Phys. Lett. **67**, 2188 (1995).

[86] T. Mattila and R. M. Nieminen, Phys. Rev. B. **55**, 9571 (1997).

[87] M. A. Reshchikov, H. Morkoc, S. S. Park and K. Y. Lee, Appl. Phys. Lett. **81**, 4970 (2002).

[88] C. B. Vartuli, S. J. Pearton, C. R. Abernathy, J. D. MacKenzie, E. S. Lambers and J. C. Zolper, J. Vac. Sci. Technol. B. **14**, 3523 (1996).

[89] A. R. Hefner, R. Singh, J. Lai, D. W. Berning, S. Bouche and C. Chapuy, IEEE. Trans. Power. Electron. **16**, 273 (2001).

[90] M. Bhatnagar, P. K. McLarty and B. J. Baliga, IEEE. Trans. Electron. Dev. Lett. **13**, 510 (1992).

[91] J. I. Chyi, C. M. Lee, C. C. Chuo, X. A. Cao, G.. T. Dang, A. P. Zhang, F. Ren, S. J. Pearton, S. N. G. Chu and R. G. Wilson, Solid-State Electron. **44**, 613 (2000).

[92] E. H. Rhoderick and R. H William, Metal-Semiconductor Contacts. Oxford 1988.

[93] W.P. Kang, J.L. Davidson, Y. Gurbuz and D.V. Kerns, J. Appl. Phys. **78**, 1101 (1995).

[94] R. M. Cibils and R. H. Buitrago, J. Appl. Phys. **58**, 1075 (1985).

[95] H. Norde, J. Appl. Phys. **50**, 5052 (1979).

[96] K. E. Bohlin, J. Appl. Phys. **60**, 1223 (1986).

[97] S. K. Cheung and N. W. Cheung, Appl. Phys. Lett. **49**, 85 (1986).

[98] K. Sato and Y. Yasumura, J. Appl. Phys. **58**, 3655 (1985).

[99] T. C. Lee, S. Fung, C. D. Beling and H. L. Au, J. Appl. Phys. **72**, 4739 (1992).

[100] S. Chand and J. Kumar, J. Appl. Phys. **80**, 288 (1996).

[101] S. Zhu, R. L. Van Meirhaeghe, C. Detavernier, F. Cardon, G.. P. Ru, X. P. Qu and B. Z. Li, Solid-State Electron **44**, 663 (2000).

[102] S. Karadeniz, M. Sahin, N. Tugluoglu and H. Safak, Semicond. Sci. Technol. **19**, 1098 (2004).

[103] P. Hacke, T. Detchprohm, K. Hiramatsu and N. Sawaki, Appl. Phys. Lett. **63**, 2676 (1993).

[104] J. D. Guo, M. S. Feng, R. J. Guo, F. M. Pan and C. Y. Chang, Appl. Phys. Lett. **67**, 2657 (1995).

[105] L. Wang, M. I. Nathan, T. H. Lim, M. A. Khan and Q. Chen, Appl. Phys. Lett. **68**, 1267 (1996).

[106] J. D. Otterloo and L. J. Gerritsen, J. Appl. Phys. **49**, 723 (1978).

[107] R. Hackam and P. Harrop, IEEE. Trans. Electron. Dev. **19**, 1231 (1972).

[108] P. G. Neudeck and C. Fazi, IEEE. Electron. Dev. Lett. **18**, 96 (1997).

[109] Synopsys (formerly ISE AG), Mountain View, California, Taurus-MEDICI: Industry-Standard Device Simulation Tool. http://www.synopsys.com/products/mixedsignal/taurus/device_sim_ds.html.

[110] Synopsys, Fremont, USA, MEDICI User's Manual, 2003.

[111] V. Saxena, J. N. Su, A. J. Steckl, IEEE. Trans. Electron. Devices. **46**, 456 (1999).

[112] K. Ueno, T. Urushidani, K. Hashimoto and Y. Seki, IEEE. Electron. Dev. Lett. **16**, 331 (1995).

[113] M. Bhatnagar, H. Nakanishi, S. Bothra, P. K. McLarty and B. J. Baliga, 5th Int. Symp.

Power. Semiconductor Devices and IC's, pp 89-94 (1993).

[114] D. Alok, B. J. Baliga and P. K. McLarty, IEEE. Electron. Dev. Lett. **15**, 394 (1995).

[115] A.Itoh, T.Kimoto, and H.Matsunami, IEEE. Electron. Dev. Lett. **17**, 139 (1996).

[116] K. J. Schoen, J. M. Woodall, J. A. Cooper and M. R. Melloch, IEEE. Trans. Electron. Dev. **45**, 1595 (1998).

[117] J. C. Zolper, J. Crys. Growth. **178**, 157 (1997).

[118] D. C. Sheridan, G. Niu, J. Neil Merrett, J. D. Cressler, C. Ellis and C. -C. Tin, Solid-State Electron. **44**, 1367 (2000).

[119] T. S. Ma and W. B. Grabowski, Solid-State. Electron. **35**, 201 (1992).

[120] M. Ruff, H. Mitlehner and R. Helbig, IEEE. Trans. Electron. Dev. **41**, 1040 (1994).

[121] A. Kumta, Rusli, C. -C. Tin, J. Ahn, Microelectron. Reliability. **46**, 1295 (2006).

[122] B. J. Baliga, *Power Semiconductor Devices*. PWS. Boston, MA. (1996)

[123] M. C. Tarplee, V. P. Madangarli, Q. Zhang and T. S. Sudarshan, IEEE. Trans. Electron. Dev. **48**, 2659 (2001).

[124] K. H. Baik, Y. Irokawa, F. Ren, S. J. Pearton, S. S. Park and S. K. Lee, J. Vac. Sci. Technol. B. **20**, 2169 (2002).

[125] H. C. Casey, G. G. Fountain, R. G. Alley, B. P. Keller and S. P. DenBaars, Appl. Phys. Lett. **68**, 1850 (1996).

[126] Q. Zhang, S. Soloview, V. Madangarli, I. Khlebnikov and T. S. Sudarshan, Proc. Mater. Res. Soc. Symp. **572**, 75 (1999).

[127] G. A. Beck, A. A. Carter, J. R. Carter, N. M. Greenwood, A. D. Lucas, D. J. Munday, T. W. Pritchard, D. Robinson, C. D. Wilburn and K. H. Wyllie, Solid-State Electron. **45**, 183 (2001).

[128] E. Monroy, E. Munoz, F. J. Sanchez, F. Calle, E. Calleja, B. Beaumont, P. Gibart, J. A. Munoz and F. Cusso, Semicond. Sci. Technol. **43**, 1042 (1998).

[129] D. Walker, A. Saxier, P. Kung, X. Zhang, M. Hamilton, J. Diaz and M. Razeghi, Appl. Phys. Lett. **72**, 3303 (1998).

[130] A. Osinsky, S. Gangopadhyay, R. Gaska, B. Williams, M. A. Khan, D. Kukenkov and H. Temkin, Appl. Phys. Lett. **71**, 2334 (1997).

[131] D. Walker, E. Monroy, P. Kung, J. Wu, M. Hamilton, F. J. Sanchez, J. Diaz and M. Razeghi, Appl. Phys. Lett. **74**, 762 (1999).

[132] J. C. Carrano, T. Li, P. A. Grudowski, C. J. Eiting, R. D. Dupuis and J. C. Campbell, J. Appl. Phys. **83**, 6148 (1998).

[133] Y. Chiou, J. Electrochem. Society **152 (8)**, G639 (2005).

[134] E. Monroy, F. Calle, E. Munoz, F. Omnes, P. Gibart and J. A. Munoz, Appl. Phys. Lett. **73**, 2146 (1998).

[135] M. L. Lee, J. K. Sheu, W. C. Lai, S. J. Chang, Y. K. Su, M. G. Chen, C. J. Kao, G. C. Chi and J. M. Tsai, Appl. Phys. Lett. **82**, 2913 (2003).

[136] O. Katz, G. Bahir and J. Salzman, Appl. Phys. Lett. **84**, 4092 (2004).

[137] S. Butun, M. Gokkavas, H. Yu and E. Ozbay, Appl. Phys. Lett. **89**, 073503 (2006).

[138] J. B. Limb, D. Yoo, J. H. Ryou, W. Lee, S. C. Shen, R. D. Dupuis, M. L. Reed, C. J. Collins, M. Wraback, D. Hanser, E. Preble, N. M. Williams and K. Evans, Appl. Phys. Lett. **89**, 011112 (2006).

[139] J. K. Kim, H. W. Jang, C. M. Jeon and J. Lee, Appl. Phys. Lett. **81**, 4655 (2002).

[140] M. L. Lee, J. K. Sheu, W. C. Lai, Y. K. Su, S. J. Chang, C. J. Kao, C. J. Tun, M. G. Chen, W. H. Chang, G. C. Chi and J. M. Tsai, J. Appl. Phys. **94**, 1753 (2003).

[141] H. Zhang, E. J. Miller and E. T. Yu, J. Appl. Phys. **99**, 023703 (2006).

[142] Y. Zhou, M. Li, D. Wang, C. Ahyi, C. -C. Tin, J. Williams, M. Park, N. M. Williams and A. Hanser, Appl. Phys. Lett. **88**, 113509 (2006).

[143] T. Sawada, Y. Ito, K. Imai, K. Suzuki, H. Tomozawa and S. Sakai, Appl. Surf. Sci. **159/160**, 449 (2000).

[144] D. J. As, S. Potthast, J. Fernandez, J. Schormann, K. Lischka, H. Nagasawa and M. Abe, Appl. Phys. Lett. **88**, 152112 (2006).

[145] J. D. Guo, F. M. Pan, M. S. Feng, R. J. Guo, P. F. Chou and C. Y. Chang, J. Appl. Phys. **80**, 1623 (1996).

[146] O. Katz, V. Garber, B. Meyler, G. Bahir and J. Salzman, Appl. Phys. Lett. **79**, 1417 (2001).

[147] S. C. Binari, W. Kruppa, H. B. Dietrich, G. Kelner, A. E. Wickenden and J. A. Freitas JR, Solid-State electron. **41**, 1549 (1997).

[148] R. Gaska, Q. Chen, J. Yang, A. Osinsky, M. Asif Khan and M. S. Shur, IEEE Electron Device Lett. **18**, 492 (1997).

[149] G. J. Sullivan, M. Y. Chen, J. A. Higgins, J. W. Yang, Q. Chen, R. L. Pierson and B. T. McDermott, IEEE Electron Device Lett. **19**, 198 (1998).

[150] F. Ren, M. Hong, S. N. G. Chu, M. A. Marcus, A. Baca, S. J. Pearton and C. R. Abernathy, Appl. Phys. Lett. **73**, 3893 (1998).

[151] Y. Nakano and T. Jimbo, Appl. Phys. Lett. **80**, 4756 (2002).

[152] P. Chen, W. Wang, S. J. Chua and Y. D. Zheng, Appl. Phys. Lett. **79**, 3530 (2001).

[153] S. Arulkumaran, T. Egawa, H. Ishikawa, T. Jimbo and M. Umeno, Appl. Phys. Lett. **73**, 809 (1998).

[154] J. Kim, B. Gila, R. Mehandru, J. W. Johnson, J. H. Shin, K. P. Lee, B. Luo, A. Onstine, C. R. Abernathy, S. J. Pearton and F. Ren, J. Electrochem. Soc. **149**, G482 (2002).

[155] J. Kim, R. Mehandru, B. Luo, F. Ren, B. P. Gila, A. H. Onstine, C. R. Abernathy, S. J. Pearton and Y. Irokawa, Appl. Phys. Lett. **81**, 373 (2002).

[156] L. W. Tu, W. C. Kuo, K. H. Lee, P. H. Tsao, C. M. Lai, A. K. Chu and J. K. Sheu, Appl. Phys. Lett. **77**, 3788 (2000).

[157] P. D. Ye, B. Yang, K. K. Ng, J. Bude, G. D. Wilk, S. Halder and J. C. M. Hwang, Appl. Phy. Lett. **86**, 063501 (2005).

[158] D. W. Langer, F. L. Schuermeyer, R. L. Johnson, H. P. Singh, C. W. Litton and H. L. Hartnagel, J. Vac. Sci. Technol. **17**, 964 (1980).

[159] S. D. Wolter, B. P. Luther, D. L. Waltemyer, C. Onneby, S. E. Mohney and R. J. Molnar, Appl. Phys. Lett. **70**, 2156 (1997).

[160] H. Kim, S. Park and H. Hwang, J. Vac. Sci. Technol. B. **19**, 579 (2001).

[161] Y. Nakano, T. Kachi and T. Jimbo, J. Vac. Sci. Technol. B. **21**, 2220 (2003).

[162] S. D. Wolter, S. E. Mohney, H. Venugopalan, A. E. Wickenden and D. D. Koleske, J. Electrochem. Soc. **145**, 629 (1998).

[163] R. Roy, V. G. Hill and E. F. Osborn, J. Am. Chem. Soc. **74**, 719 (1952).

[164] P. Chen, R. Zhang, X. F. Xu, Z. Z. Chen, Y. G. Zhou, S. Y. Xie, Y. Shi, B. Shen, S. L. Gu, Z. C. Huang, J. Hu and Y. D. Zheng, Mater. Res. Soc. Symp. Proc. **W11.71** (1999).

[165] G. Schon, J. Electron. Spectrosc. Relat. Phenom. **2**, 75 (1973).

[166] S. W. King, J. P. Barnak, M. D. Bremser, K. M. Tracy, C. Ronning, R. F. Davis and R. J. Nemanich, J. Appl. Phys. **84**, 5248 (1998).

[167] F. Ren, M. Hong, J. P. Mannaerts, J. R. Lothian and A. Y. Cho, J. Electrochem. Soc.

144, L239 (1997).

[168] C. B. Vartuli, J. D. MacKenzie, J. W. Lee, C. R. Abernathy, S. J. Pearton and R. J. Shul, J. Appl. Phys. **80**, 3705 (1996).

[169] T. S. Lay, M. Hong, J. Kwo, J. P. Mannaerts, W. H. Hung and D. J. Huang, Solid-State Electron. **45**, 1679 (2001).

[170] G. V. Samsonov, *The Oxide Handbook*, 2nd ed. IFI/Plenum, New York, 1982.

[171] Y. Nakano and T. Jimbo, Appl. Phys. Lett. **82**, 218 (2003).

[172] J. A. Cooper, Jr, Phys. Stat. Sol. (a). **162**, 305 (1997).

[173] D. K. Schroder, *Semiconductor Material and Device Characterization*, 2nd ed. (Wiley, New York, 1998).

[174] Y. Nakano, T. Kachi and T. Jimbo, Appl. Phys. Lett. **83**, 4336 (2003).

[175] E. H. Nicollian and J. R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology* (Wiley, New York, 1986).

APPENDIX A

Material parameters of GaN defined in Medici to replace Si's default values

Parameter	Units	Silicon	GaN
PERMITTI		11.8	9
AFFINITY	V	4.17	4.1
EG300	eV	1.08	3.39
EGALPH	eV/K	4.73e-4	-10.8e-4
EGBETA	K	636	745
EGALX	eV/K	4.73e-4	0
EGBEX	K	636	0
NC300	cm^{-3}	2.8e19	2.3e18
NV300	cm^{-3}	1.04e19	4.6e19
EDB	eV	0.044	0.062
EAB	eV	0.045	0.15
TAUN0	s	1e-7	1e-9
TAUP0	s	1e-7	1e-9
AUGN	cm^6/s	2.8e-31	1E-30
AUGP	cm^6/s	9.9e-32	1E-31

ARICHN	A/(K-cm)^2	110	26.4
ARICHP	A/(K-cm)^2	30	103.8
N.IONIZA	cm^{-1}	7.03e5	8.85e6
ECN.II	V/cm	1.231e6	2.6e7
P.IONIZA	cm^{-1}	1.528e6	8.85e6
ECP.II	V/cm	2.036e6	2.6e7
ME.SBT	cm	0.22	0.222
MH.SBT	cm	0.35	1
DENSITY	kg/cm^3	2.32e-3	6.15e-3
A.SP.HEA	J/kg/K	850.9	494.4
B.SP.HEA	J/kg/K^2	152.2e-3	108.9e-3
D.SP.HEA	J-K/kg	-158.2e5	-114.4e5
A.TH.CON	cm-K/W	0.03	0.435
B.TH.CON	cm/W	1.56e-3	0
C.TH.CON	cm/W/K	1.65e-6	0
OP.PH.EN	eV	0.063	0.0912
LAN300	cm	10.4542e-7	1e-5
LAP300	cm	6.32079e-7	1e-5
EL.EMAS		0.31	0.222
HO.EMAS		0.5	1
MUN0	cm^2/V-s	1000	1250
MUP0	cm^2/V-s	500	100

MUN.MIN	cm^2/V-s	55.24	55
MUN.MAX	cm^2/V-s	1429.23	1000
NREFN	#/cm^3	1.07e17	2e17
NUN		-2.3	-2
ALPHAN		0.733	1
MUP.MIN	cm^2/V-s	49.705	3
MUP.MAX	cm^2/V-s	479.37	170
NREFP	#/cm^3	1.61e17	3e17
NUP		-2.2	-5
ALPHAP		0.7	2
VSATN	cm/s	1.035e7	3e7
VSATP	cm/s	1.035e7	4.8e6

APPENDIX B

Sample Medici simulation program for reverse breakdown characteristics of bulk GaN Schottky diode with a SiO_2 field plate

```
Title      GaN Schottky Diode 30um bulk 1E16 n-doping, 1um thick SiO2 edge
termination, 15um Schottky metal overlap


comment      lateral dimension
assign name=Lschottk    n.value=50
assign name=Lw    n.value=100
assign name=Lap n.value=15
comment        vertical dimension
assign name=Toxide    n.value=1
assign name=Tbulk      n.value=30
assign name=Tbulkm    n.value=20


mesh            cylindri SMOOTH=1    out.file=G38.msh


comment      mesh initialization
```

```
x.mesh      x.min=0   x.max=@Lschottk-20   h1=3 h2=1

x.mesh      x.min=@Lschottk-20 x.max=@Lschottk-10   h1=1 h2=0.2

x.mesh      x.min=@Lschottk-10 x.max=@Lschottk+25   h1=0.2 h2=0.2

x.mesh      x.min=@Lschottk+25 x.max=@Lschottk+30 h1=0.2 h2=1

x.mesh      x.min=@Lschottk+30 x.max=@Lw h1=1 h2=3

y.mesh      depth=8 h1=0.2 h2=0.2

y.mesh      depth=3 h1=0.2 h2=0.5

y.mesh      depth=@Tbulkm-11 h1=0.5 h2=2

y.mesh      depth=@Tbulk-@Tbulkm+@Toxide   h1=2 h2=2


comment     specify materials and contact position. use silicon as GaN, but properties

will be changed to GaN later.


region      Name=fieldp oxide y.min=0 y.max=@Toxide

region      Name=GaNBulk silicon y.min=@Toxide y.max=@Toxide+@Tbulk


ELECTR          Name=Anode interfac x.min=0 x.max=@Lschottk

ELECTR          Name=Anode x.min=@Lschottk x.max=@Lschottk+@Lap y.min=0

+y.max=0

ELECTR          Name=Cathode bottom


comment         Doping Profile

Profile     N-Type N.Peak=1E16 uniform y.min=@Toxide
```

```
comment        change default Silicon Material parameters to GaN
Material     Silicon   PERMITTI=9   AFFINITY=4.1   EG300=3.39
+EGALPH=-10.8E-4   EGBETA=745   EGALX=0   EGBEX=0   NC300=2.3E18
+NV300=4.6E19   EDB=0.062   EAB=0.15   TAUN0=1E-9   TAUP0=1E-9
+AUGN=1E-30   AUGP=1E-31   ARICHN=26.4   ARICHP=103.8 N.IONIZA=8.85E6
+ECN.II=2.6E7   P.IONIZA=8.85E6   ECP.II=2.6E7   ME.SBT=0.222   MH.SBT=1
+DENSITY=6.15E-3   A.SP.HEA=494.4   B.SP.HEA=108.9E-3   D.SP.HEA=-114.4E5
+A.TH.CON=0.435   B.TH.CON=0   C.TH.CON=0 OP.PH.EN=0.0912
+LAN300=1E-5   LAP300=1E-5   EL.EMAS=0.222   HO.EMAS=1

comment        change default Silicon Mobility parameters to GaN
Mobility       Silicon   MUN0=1250   MUP0=100   MUN.MIN=55
+MUN.MAX=1000   NREFN=2E17   NUN=-2   XIN=-3.8   ALPHAN=1
+MUP.MIN=3   MUP.MAX=170   NREFP=3E17   NUP=-5   XIP=-3.7
+ALPHAP=2 VSATN=3E7   VSATP=4.8E6

comment        specify schottky contact on electro name=Anode and schottky metal to
be Pt with a work function 5.65ev
Contact      Name=Anode    WORKFUNC=5.65   SURF.REC   VSURFN=1E3
+VSURFP=1E3

Regrid       doping log ratio=1
```

```
PLOT.2D        GRID TITLE="Grid Setup" FILL bound junc SCALE
mesh    in.fil=G38.msh

comment    repeat to change default Silicon Material parameters to GaN because it's not
saved in mesh file

Material     Silicon   PERMITTI=9   AFFINITY=4.1   EG300=3.39
+EGALPH=-10.8E-4   EGBETA=745   EGALX=0   EGBEX=0   NC300=2.3E18
+NV300=4.6E19   EDB=0.062   EAB=0.15   TAUN0=1E-9   TAUP0=1E-9
+AUGN=1E-30   AUGP=1E-31   ARICHN=26.4   ARICHP=103.8 N.IONIZA=8.85E6
+ECN.II=2.6E7   P.IONIZA=8.85E6   ECP.II=2.6E7   ME.SBT=0.222   MH.SBT=1
+DENSITY=6.15E-3   A.SP.HEA=494.4   B.SP.HEA=108.9E-3   D.SP.HEA=-114.4E5
+A.TH.CON=0.435   B.TH.CON=0   C.TH.CON=0 OP.PH.EN=0.0912
+LAN300=1E-5   LAP300=1E-5   EL.EMAS=0.222   HO.EMAS=1

comment    repeat to change default Silicon Mobility parameters to GaN because it's not
saved in mesh file

Mobility       Silicon   MUN0=1250   MUP0=100   MUN.MIN=55
+MUN.MAX=1000   NREFN=2E17   NUN=-2   XIN=-3.8   ALPHAN=1
+MUP.MIN=3   MUP.MAX=170   NREFP=3E17   NUP=-5   XIP=-3.7
+ALPHAP=2 VSATN=3E7   VSATP=4.8E6
```

```
comment     repeat contact information because it's not save by mesh file
Contact Name=Anode     WORKFUNC=5.65    SURF.REC     VSURFN=1E3
VSURFP=1E3

symbo   newton    carriers=0
solve     v(anode)=0

models  srh auger analytic fermidir fldmob    impact.i

comment     nint=electron ionization integral
comment     pint=hole ionization integral
comment     VStep=anode volatge step size
comment     eb=breakdown field of the oxide

assign    name=nint n.val=1
assign    name=pint n.val=1
assign    name=eb      n.val=1E7
assign    name=VSt    n.val=0
assign    name=VStep1 n.val=-20
assign    name=VStep2 n.val=-10
assign    name=Va n.val=@VSt
```

```
symbo   newton   carriers=2
models  srh auger analytic fermidir fldmob   impact.i
solve   V(anode)=@Va   out.file="sol"@Va save.bia

log     out.file=G38iv.out

solve       v(anode)=-0.1
solve       v(anode)=-0.2
solve       v(anode)=-0.5
solve       v(anode)=-1
solve       v(anode)=-2
solve       v(anode)=-4
solve       v(anode)=-8
solve       v(anode)=-16

assign  name=Va n.val=-20

comment print material parameters
material print

loop    steps=400
    extract name=iinint expressi="min(4e34;@ii.n.int)" print
    extract name=iipint expressi="min(4e34;@ii.p.int)" print
```

```
    extract expressi="max(@emax;@em)" cond="@x>50&@y<1"    name=emax
initial=0    print
    assign name=nbd l.val=(@iinint>=@nint)
    assign name=pbd l.val=(@iipint>=@pint)
    assign name=obr l.val=(@emax>=@eb)
    if cond=(@nbd|@pbd|@obr)
          l.modify    break
    else
          solve    V(anode)=@Va    out.file="sol"@Va save.bia
              SAVE TIF OUT.FILE=a38.tif ALL
          assign name=nearbd l.val=(@Va<=-200)
               if cond=(@nearbd)
             assign name=Va    n.val=@Va+@VStep2
               else
        assign name=Va      n.val=@Va+@VStep1
               if.end
    if.end
l.end
```