A Low Power, Low Noise Phase Locked Loop MMIC for Ku− and X−Band Applications

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Mark E. Ray

Certificate of Approval:

Stuart Wentworth
Associate Professor
Electrical and Computer Engineering

Fa Dai, Chair
Professor
Electrical and Computer Engineering

Robert Dean
Assistant Professor
Electrical and Computer Engineering

Mark Nelms
Department Head
Electrical and Computer Engineering

George T. Flowers
Dean
Graduate School

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Mark E. Ray

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Mark E. Ray

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Signature of Author

_____

Date of Graduation

Vita

Mark Edward Ray, son of Roger and Lois (Battles) Ray, was born February 12, 1985, in Birmingham, Alabama. He graduated from Trinity Christian Academy, Oxford, Alabama, as co-Valedictorian in 2003. During his Junior and Senior years, he attended Gadsden State Community College in Gadsden, Alabama, becoming the first dual-enrollment student at Trinity Christian Academy. He entered Auburn University as a Sophomore in August, 2003, and he entered the co-operative education program in May, 2004. Mr. Ray worked for the U.S. Army Space and Missile Defense Command on alternating semesters and graduated cum laude with a Bachelor of Electrical Engineering in December, 2007. He entered Graduate School, Auburn University, in January, 2008. He is a Research Assistant for Dr. F. Dai in the field of Integrated Circuit (IC) design. He is married to Christina (Pizano) Ray and has a daughter Kaylee and son Andrew.

Thesis Abstract

A Low Power, Low Noise Phase Locked Loop MMIC for Ku− and X−Band Applications

Mark E. Ray

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This paper presents the analysis, design, simulation, and test results for a Fractional−N PLL frequency synthesizer. The synthesizer is designed to cover multiple frequency bands, require low power, and have low noise. Detailed analysis is presented on loop dynamics, stability, and noise. All components in the circuit are designed for low noise and low power. For example, The Multi−Modulus Divider (MMD) is implemented such that it has the minimum number of gates and the lowest power consumption. The division ratios can be programmed from 128 to 159 and consumes 11mA under a 2.2V power supply, which corresponds to 59.2% power reduction compared to the prior art.

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Chapter 1

Introduction

1.1 Purpose Statement

The purpose of this thesis is to develop a frequency synthesizer that addresses the need for flexibility to be able to operate in multiple frequency bands. This is accomplished through fractional−N synthesizer design with a Multi−Modulus Divider. The PLL Frequency synthesizer design can synthesize channels in Ku− and X− bands. The designer seeks to minimize noise through methodical analysis of noise sources and careful design of circuits. For further reduction in noise a $\Sigma\Delta$ modulator can be employed.

The trend for wireless transceivers is to offer the ability to operate in different frequency bands. To be competitive, a frequency synthesizer must exhibit low noise and be able to synthesize channels in multiple frequency bands. This means that there must be an emphasis on divider design. Another challenge in frequency synthesizer design is the demand for fast switching and high operating frequency. These demands push the limits of the current technology.

This design of a fractional−N frequency synthesizer seeks to obtain the capability of synthesizing channels in multiple frequency bands. For the purpose of a single chip system, the designer must seek to cut power consumption. All circuits presented here are designed for low power applications.

1.2 Technology Overview

1.2.1 SiGe HBTs

There are many benefits to SiGe over Silicon, GaAs and other technologies. Utilizing a process where Heterojunction Bipolar Transistors (HBT)s and Complimentary MOS

Parameter	CMOS	Si BJT	SiGe BJT
f_T	High	High	High
f_{MAX}	High	High	High
Linearity	Best	Good	Better
Vbe (or V_T)*tracking*	Poor	Good	Good
1/f noise	Poor	Good	Good
Broadband noise	Poor	Good	Good
Early Voltage	Poor	OK	Good
Transconductance	Poor	Good	Good

Table 1.1: Technology Comparison[1]

Transistors can be combined gives the designer the opportunity to exploit the best of both worlds. SiGe provides just such an opportunity. Heterojunction bipolar transistors have lower current consumption and better high frequency performance than traditional homojuntion bipolar transistors because they have higher forward gain and lower reverse gain[1]. Table 1.1 shows how the different technologies compare.

Frequency synthesizers are a prime example of mixed signal circuits. The charge pump, VCO, and loop filter are analog circuits, while the divider and phase detector are usually digital blocks. HBT technology has several features that are good for frequency synthesizer application, which needs both digital and analog circuits [2]. For digital applications, f_T must be at least twice the highest flip-flop toggling rate [3]. f_T higher than 210 GHz has been obtained for HBT technology. The high transconductance of the HBT allows a digital circuit to respond to small signal swings, and to drive large output capacitances in short times. For analog circuit applications, high power gain is required in addition to high f_T . An HBT has low base resistance and low extrinsic base-collector capacitance; f_{MAX} as high as 285 GHz has been observed for HBTs in current technologies. An HBT is a vertical structure device that has much lower l/f noise than a MESFET. 1/f noise is a heavy contributor to phase noise. In turn, the phase noise of the VCO is the key characteristic for frequency synthesizer application.

1.2.2 CMOS Logic and Bipolar Current Mode Logic

HBT technology discussed in the previous section lends itself easily to Current Mode Logic (CML) circuits. CMOS circuits dissipate energy during switching, thus for low frequency operation it is intuitive that CMOS would have lower power consumption. Conversely, for high frequency operation such as the frequency of the synthesizer, CMOS has high power consumption. The advantage of Bipolar CML over CMOS is in high frequency operation. CML, which has high current consumption at low frequency, has a more shallow increase in current versus frequency than does CMOS.

Bipolar CML also has better noise performance and power supply rejection than rail−to−rail CMOS. CML is inherently differential allowing for common mode noise to be rejected. CML has a very small signal swing compared to CMOS which swings rail−to−rail introducing power supply noise. Dc current is constant in CML, making switching noise smaller. With the ability to operate at much higher maximum speed and lower power dissipation, CML is the clear choice for high speed synthesizer design.

1.3 Thesis Organization

The body of this document is divided into ten chapters. The first chapter gives a summary of the current technology. The benefits of SiGe over Si and GaAs are discussed. In this chapter the question of why CML is used instead of high speed CMOS logic is answered.

Next, the PLL system level analysis is performed. Continuous time and discrete time models are derived and expressions are evaluated for system parameters. The different behaviors of acquisition mode and phase lock mode are analyzed. PLL component values are determined through specific example. Other analyses performed include: stability, noise, step response and frequency response.

The next chapters cover the design of the PFD, charge pump, loop filter, and VCO. Included in these chapters is an interesting possibility for a future design to make the loop

filter programmable. A brief analysis of the $-$gm oscillator is performed and K_{VCO} and phase noise are simulated.

A more in$-$depth chapter covers the design of the divider. Different architectures are compared and the analysis is performed to minimize the number of cells for a MMD. The MMD current is reduced further by reducing the current at each stage at the expense of modularity (but not area). The noise in the loop is further reduced if a $\Sigma\Delta$ modulator is added to toggle the MMD bits.

Chapter 9 delves into the circuits designed for low voltage applications. Chapter 10 covers the testing and measurement results of the PLL frequency synthesizer.

Chapter 2

PLL System Analysis

2.1 Introduction

To understand the performance of the Phase Locked Loop frequency synthesizer it is necessary to look at the loop from a control system perspective[1]. In normal operation, the PLL is a Linear Time−Invariant System, but in acquisition it must be treated as a nonlinear system. In sections 2.2−2.5 in−depth analysis is performed to determine the loop transfer function, frequency and step response, loop filter component values, damping constant, natural frequency, stability and phase margin. In section 2.6, the noise sources in individual blocks are modeled.

2.2 Continuous−Time Analysis

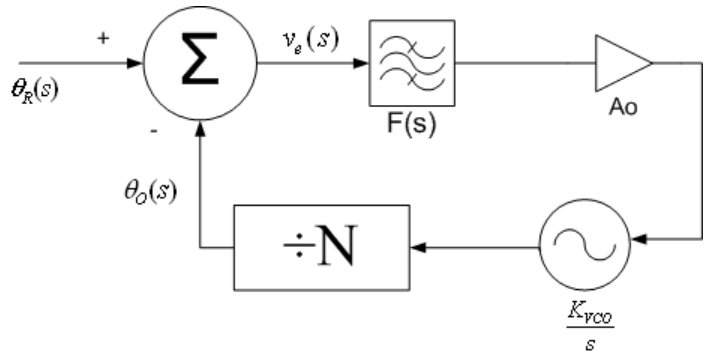

Figure 2.1: Complete loop in the frequency domain

[1]PLL system analysis has been outlined in several texts [4], [18]. Except where stated, the author follows the analysis performed in [4]. Examples make use of the author's specific design requirements and figures are generated by the author with code listed in Appendix A.

In general, the PLL is broken down in the s domain in the following way. In the frequency domain the complete loop is shown in Figure 2.1. The simplified loop equation is

$$\frac{\theta_o}{\theta_R} = \frac{\frac{A_o K_{phase} F(s)}{N} \cdot \frac{K_{vco}}{s}}{1 + \frac{A_o K_{phase} F(s)}{N} \cdot \frac{K_{vco}}{s}} = \frac{KF(s)}{s + KF(s)} \tag{2.1}$$

For a second order PLL (1^{st} *order loop filter*) the transfer function becomes

$$\frac{\theta_o}{\theta_R} = \frac{\frac{IK_{vco}}{2\pi \cdot NC_1}(RC_1 s + 1)}{s^2 + \frac{IK_{vco}}{2\pi \cdot N} Rs + \frac{IK_{vco}}{2\pi \cdot NC_1}} \tag{2.2}$$

From control theory, the purpose of R can be seen. If R were not included then the poles of the equation would sit on the jω axis and the loop would become unstable. From Equation 2.2 several key expressions for loop dynamics can be determined. The natural frequency is given by

$$\omega_n = \sqrt{\frac{IK_{vco}}{2\pi \cdot NC_1}} \tag{2.3}$$

The damping constant is

$$\zeta = \frac{R}{2}\sqrt{\frac{IK_{vco}C_1}{2\pi \cdot N}} \tag{2.4}$$

Usually, natural frequency and damping constant are chosen for desired loop performance. If natural frequency and damping constant are specified then the equations can be rearranged to solve for R and C_1.

$$C_1 = \frac{IK_{vco}}{2\pi \cdot N\omega_n^2} \tag{2.5}$$

$$R = 2\zeta\sqrt{\frac{2\pi \cdot N}{IK_{vco}C_1}} \tag{2.6}$$

The PLL frequency response for differing values of ζ is shown in Figure 2.2. We can see that the 3$-$dB bandwidth is dependent on ζ and the equation is provided here

$$\omega_{3dB} = \omega_n\sqrt{1 + 2\zeta^2 + \sqrt{4\zeta^4 + 4\zeta^2 + 2}} \tag{2.7}$$

It will be shown later that we should choose ζ greater than 1.5. Therefore, the bandwidth can be approximated as

$$\omega_{3dB} \approx 2\zeta\omega_n \tag{2.8}$$

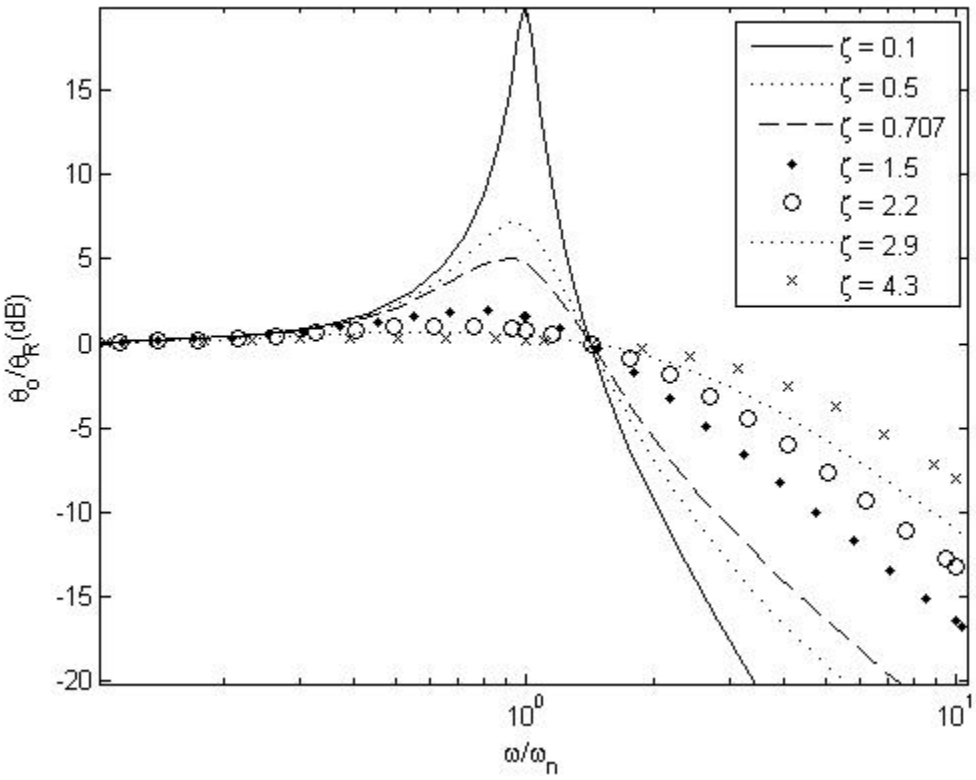

Figure 2.2: 2^{nd} Order PLL frequency response for different values of ζ

For the 3^{rd} order loop that includes a second capacitor (C_2) a high frequency pole is added. The function of this pole is to further reduce high frequency ripple on the control line. The value of C_2 is usually chosen to be 1/10 of C_1. For the 3^{rd} order loop the transfer function becomes

$$\frac{\theta_o}{\theta_R} = \frac{K_{vco}K_{phase}\left(1+sC_1R\right)}{s^2N\left(C_1+C_2\right)\left(1+sC_sR\right)+K_{vco}K_{phase}\left(1+sC_1R\right)} \tag{2.9}$$

2.3 Discrete Time Analysis for PLL

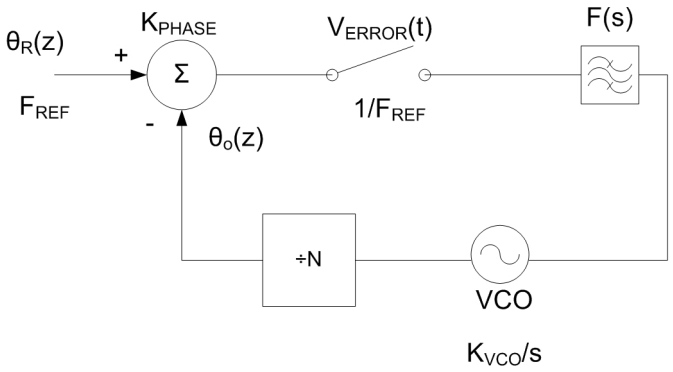

Figure 2.3: Discrete time equivalent of PLL

If the loop bandwidth is a significant fraction of the reference frequency the previous approach becomes inaccurate. Therefore we treat it as a discrete−time control system. In this case we treat the PFD as a sampling element. The loop filter performs a hold function. We now have a sampled system and can convert from the s domain to the z domain. The discrete time equivalent of the PLL system is shown in Figure 2.3. The factored open loop transfer function is shown here without derivation.

$$G_{OL}(z) = k\left[\frac{z-\alpha}{(z-1)^2}\right] \tag{2.10}$$

where the open-loop zero α is dependent on the reference frequency and is given by

$$\alpha = \frac{4\zeta - \omega_n T}{4\zeta + \omega_n T} \tag{2.11}$$

and the open loop gain is

$$K = \frac{\omega_n^2 T^2}{2}\left(1 + \frac{4\zeta}{\omega_n T}\right) \tag{2.12}$$

Some important equations for the purpose of root locus analysis will be given here and the concepts will be illustrated in a specific example in a later section. The poles of 2.12

are given by

$$Poles = 1 - \frac{k}{2} + \frac{1}{2}\sqrt{(k-2)^2 - 4(1-\alpha K)} \tag{2.13}$$

The large positive pole will never leave the unit circle, but we need to determine the point of instability that occurs when

$$1 - \frac{K}{2} - \frac{1}{2}\sqrt{(K-2)^2 - 4(1-\alpha K)} = -1 \tag{2.14}$$

or when

$$K(1+\alpha) = 4 \tag{2.15}$$

This leads to the critical period T_{US} where the loop goes unstable.

$$T_{US} = \frac{1}{\omega_n \zeta} = \frac{2\pi}{\omega_{ref_crt}} \tag{2.16}$$

where ω_{ref_crt} is the reference frequency at which the loop goes unstable. ω_{ref_crt} can be determined by rearranging Equation 2.16.

$$\omega_{ref_crt} = 2\pi\zeta\omega_n \tag{2.17}$$

Therefore,

$$\frac{\omega_{ref}}{\omega_n} \geq 2\pi\zeta \tag{2.18}$$

So, if we choose $\zeta = .707$ the ratio of reference to natural frequency must be greater than 4.4. Therefore, for a reference frequency of 40 MHz, if the loop natural frequency is set any higher than 9.1 MHz, the loop will go unstable. A rule of thumb is to make the reference frequency to natural frequency ratio about 10:1[6], [26].

2.4 Transient Behavior of PLLs

The analyses of the previous two sections do not determine what happens before the loop starts to track the phase of the input. If the phase error exceeds 2π then the loop will experience what is known as cycle slipping. In extreme cases if the VCO is forced beyond its linear range of operation the loop may lose lock indefinitely.

2.4.1 Linear Transient Behavior

For transient analysis, we desire to find the phase error. The transer function of phase error for a 3^{rd} order PLL is derived as follows:

$$\frac{\theta_e}{\theta_R} = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{2.19}$$

Normally, for transient analysis we desire to apply a frequency step $\Delta\omega$. To find phase error we take the phase equivalent of a frequency step. The phase equivalent of a frequency step is a phase ramp. So the input signal is described by

$$\theta_R = \frac{\Delta\omega}{s^2} \tag{2.20}$$

This phase ramp multiplied with the transfer function in Equation 2.19 results in

$$\theta_e = \frac{\Delta\omega}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{2.21}$$

Taking the inverse Laplace transform yields the following results

$$\theta_e(t) = \frac{\Delta\omega}{\omega_n}\left[\frac{\sinh\omega_n\sqrt{\zeta^2-1}t}{\sqrt{1-\zeta^2}}\right], \zeta > 1 \tag{2.22}$$

$$\theta_e(t) = \frac{\Delta\omega}{\omega_n}\omega_n t \cdot e^{-\omega_n t}, \zeta = 1 \tag{2.23}$$

$$\theta_e(t) = \frac{\Delta\omega}{\omega_n}\left[\frac{\sin\omega_n\sqrt{1-\zeta^2}t}{\sqrt{1-\zeta^2}}\right], \zeta < 1 \tag{2.24}$$

From Figure 2.4 it is seen that a damping constant of 0.707 to 1 yields the fastest settling time. Settling time corresponds to how fast the phase error settles to zero. From Figure 2.4 it is seen that the settling is better than 99% complete when $\omega_n t = 7$ for $\zeta = 0.707$.

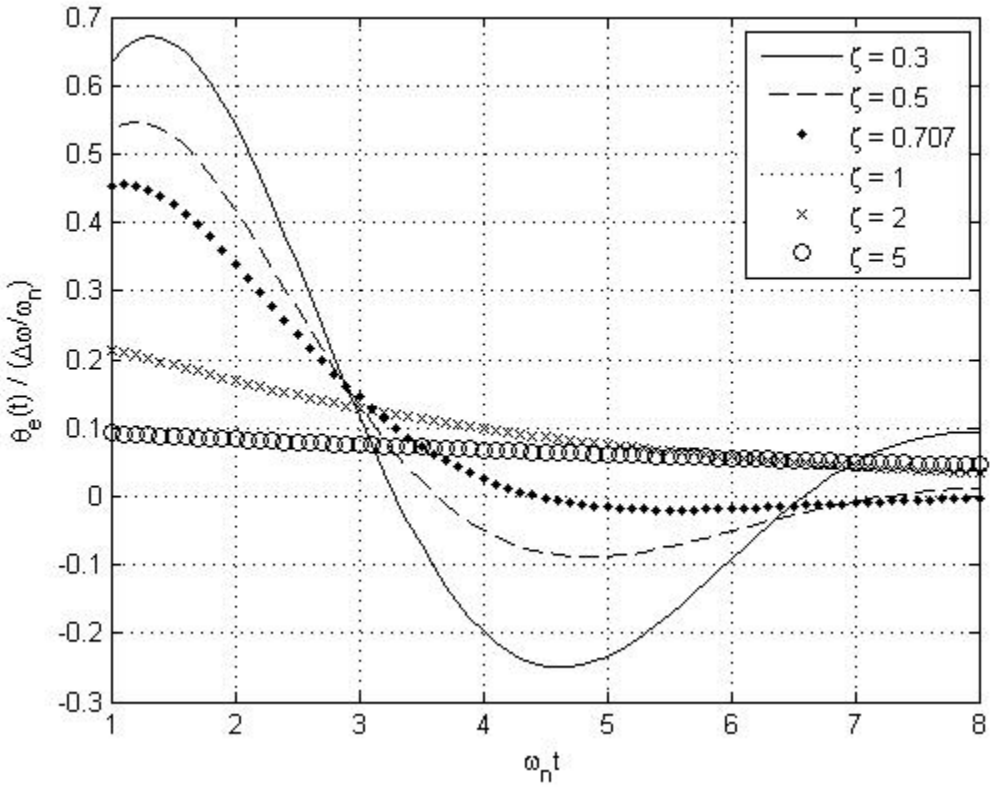

Figure 2.4: 2^{nd} Order PLL step response for different values of ζ

2.4.2 *Example: Settling Time of Synthesizer*

The 2^{nd} order PLL synthesizer designed with a charge pump, PFD, and loop filter as discussed earlier in this chapter is assumed here. It is assumed that the loop filter is designed to have a damping constant $\zeta = 0.707$ and a bandwidth of 110 kHz. What is the maximum frequency step that the synthesizer can handle?

Solution: First, compute the natural frequency of the loop from 2.7:

$$\omega_n \approx \frac{\omega_{3dB}}{\left(1+\zeta\sqrt{2}\right)} = \frac{2\pi \cdot 110kHz}{2} = 2\pi \cdot 55kHz \tag{2.25}$$

From Figure 2.4, the maximum phase error from a frequency step is about 0.46 for $\zeta = 0.707$. So, the maximum phase error is

$$\theta_{e_max} = 0.46\frac{\Delta\omega}{\omega_n} \tag{2.26}$$

With the tristate phase detector the maximum phase error that can be handled is 2π. This means that the largest frequency step that the system can handle is

$$\Delta\omega_{max} = 4.72Mrad/sec \Rightarrow 751.25kHz \tag{2.27}$$

For a frequency step $> \Delta\omega_{max}$ then cycle slip occurs. Knowing that the step response settles to within 99% of its value at $\omega_n t = 7$. So the transient settles in about $t = 20.25\mu$s.

2.4.3 *Example: Design of Integer-N Synthesizer for Specified Settling Time*

Design an integer-N synthesizer to operate from 11.5−14.31 GHz (13.84 GHz is the operating frequency of the PLL frequency synthesizer). The synthesizer must be able to settle from a frequency step in 200μs. The channel spacing and the the reference frequency are 40 MHz. Assume that the damping constant $\zeta = 0.707$ and $\omega_n t = 7$. Therefore, $\omega_n = 35krad/s \Rightarrow 5.57kHz$. The bandwidth is calculated as $BW = (1+\zeta\sqrt{2})\omega_n = 11.139kHz$.

To continue this analysis we must find the loop gain K, and the divider ratio (N). If the reference frequency is 40MHz, then the divider ratio (N) must be from 256 to 318. The VCO tuning range is 223.2MHz. To allow for 10% process variation we will extend the tuning range to 250MHz. Assuming a 2V supply, K_{vco} becomes 250MHz/V.

Charge pump current I, and loop filter component values C_1 and R can now be calculated. The ratio of loop filter capacitance and charge pump current can be calculated

first.

$$\frac{C_1}{I} = \frac{K_{vco}}{2\pi\omega_n^2} = \frac{2\pi \cdot 250MHz}{2\pi \cdot 256 \cdot 35^2\,[krad/s]^2} = 4.4 \times 10^{-3} \tag{2.28}$$

Choosing $C_1 = 5nF$ yields charge pump current $I = 11.33\mu$A. The loop filter resistance can now be calculated.

$$R = 2\zeta\sqrt{\frac{2\pi \cdot N}{IK_{vco}C_1}} = 19k\Omega \tag{2.29}$$

2.4.4 Nonlinear Transient Behavior

As discussed in the previous section, for large frequency step inputs the linear transient behavior model does not apply. We must use the nonlinear model. We know that any frequency step will generate some nonzero phase error. If the loop experiences a transient frequency step, how long does it take the loop to reacquire lock? The output of the PFD will look like the simulation in figure 2.5 and the charge pump will output current pulses. These current pulses vary between close to zero and the reference period. Then the average current produced by the charge pump is I/2. We assume that the current flows onto the capacitor C_1 and the change in voltage across the capacitor as a function of time is

$$\frac{\Delta v_C}{\Delta t} = \frac{I}{2C_1} \tag{2.30}$$

Therefore, the settling time will be

$$T_s = \frac{2\Delta v_C C_1}{I} \tag{2.31}$$

Using the relationship $\omega_{vco} = K_{vco}v_c$ the settling time as a function of input frequency change $\Delta\omega$ is written as

$$T_s = \frac{2C_1\Delta\omega N}{IK_{vco}} = \frac{\Delta\omega}{\pi\omega_n^2} \tag{2.32}$$

For 3^{rd} order loop the capacitor C_2 can be included. The function of C_2 is to further filter the high frequency ripple caused by the turning on and off of the control current. For this reason C_2 tends to smooth ripple on control voltage.

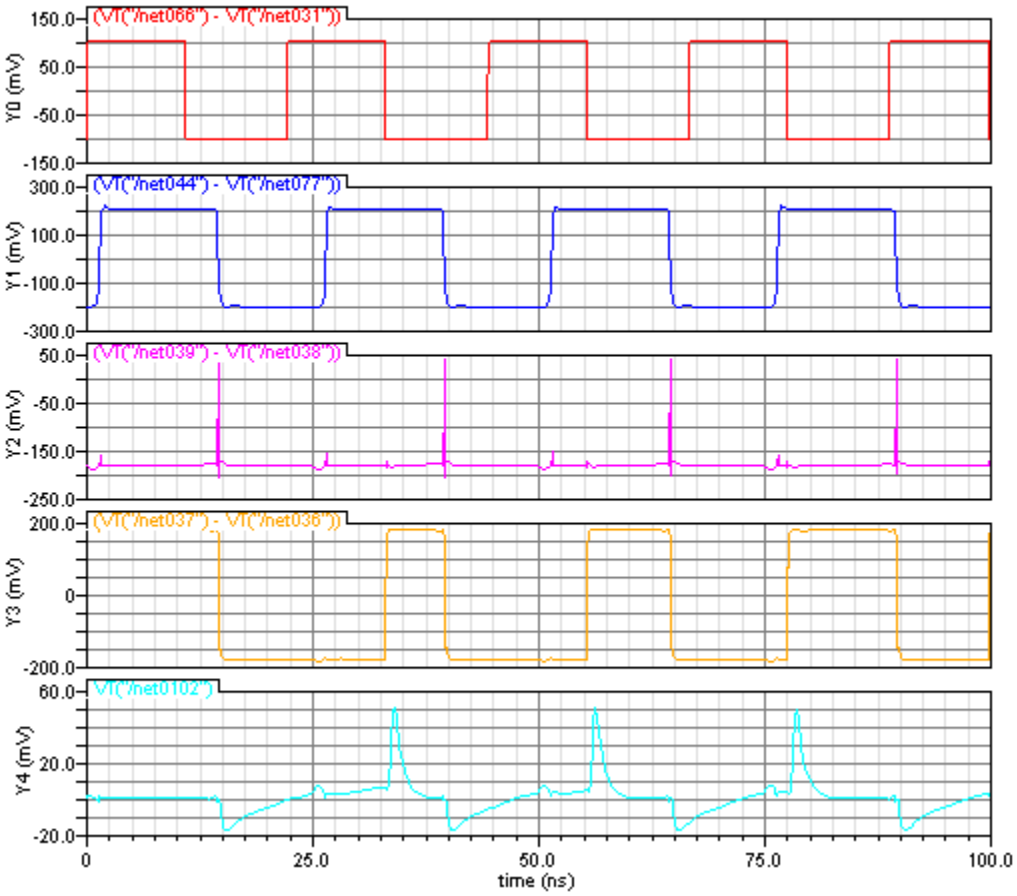

Figure 2.5: PFD simulation signals from top to bottom are: Reference, Divider, UP, DOWN, Charge Pump Output

2.4.5 *Example: Estimation of Loop Settling Times*

Using the same PLL synthesizer from the previous example, estimate settling time for output frequency steps of 50MHz and 500MHz. This results in reference frequencies of 224kHz and 2.24MHz respectively. The loop from the previous example has a loop bandwidth of 110kHz and a charge pump current of 11.33μA.

We learned previously that the maximum step that the system can handle is 750kHz. Since the first frequency step is smaller than this value the frequency step will be a linear one and easily handled. From $\omega_n t = 7$ and for a $\omega_n = 2\pi \cdot 55kHz$ the loop will settle in 20.25μs.

For the frequency step of 500MHz, we must include cycle slipping. The acquisition time is estimated using Equation 2.32 to be 3.75μs. Therefore, the complete settling time for the loop is 3.75μs for frequency acquisition + 20.25μs for phase lock.

In reality the loop should settle somewhat faster than this. The loop starts phase lock just before frequency acquisition is finished.

2.5 Stability Analysis

A root locus analysis is performed to determine when the system is stable. For a z domain analysis, the root locus is stable if the poles are inside the unit circle. From the root locus analysis we can determine at what frequency the loop becomes unstable.

For this analysis we choose $\zeta = 0.707$, and a reference period of 1/40MHz. Using the open loop transfer function in Equation 2.12 for $\omega_n = 55kHz$ the open loop zero is:

$$\alpha = \frac{4\zeta - \omega_n T}{4\zeta + \omega_n T} = 0.9939 \tag{2.33}$$

and the open loop gain is

$$K = \frac{\omega_n^2 T^2}{2}\left(1 + \frac{4\zeta}{\omega_n T}\right) = 0.0123 \tag{2.34}$$

Using the code in Appendix A.3 the root locus plot is generated. From Figure 2.6 we see that the system is stable to 2.51×10^8rad/s or 15.7GHz.

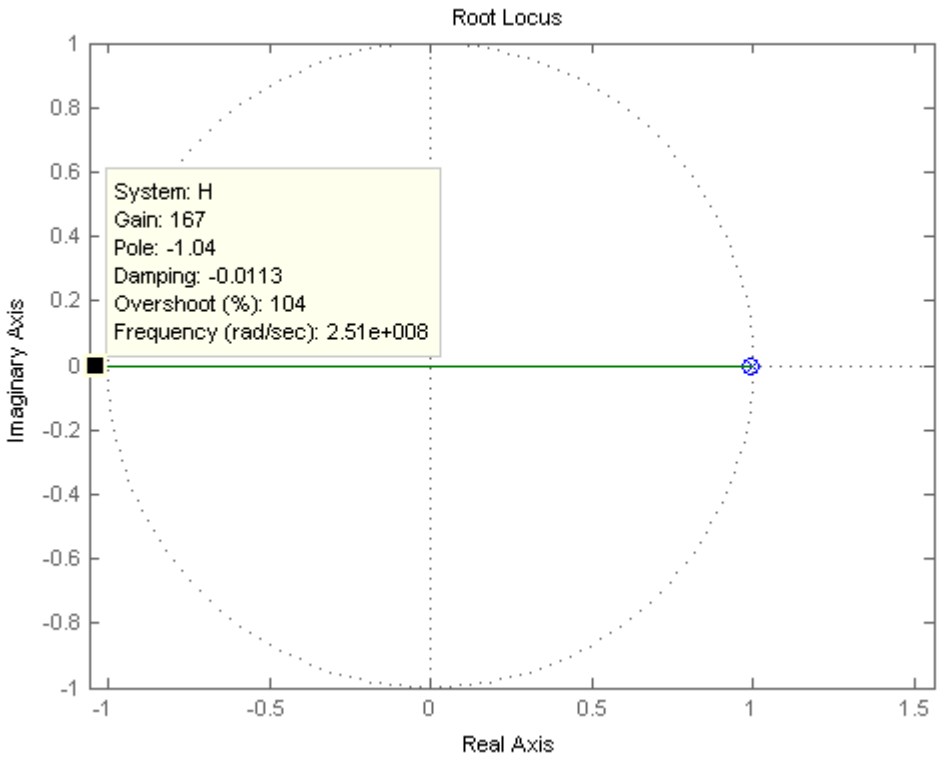

Figure 2.6: Root locus analysis

In an expanded view in Figure 2.7, the analysis is confirmed. one pole will pair with the zero and the other will tend to $-\infty$ as the frequency is increased.

2.5.1 Gain and Phase Margin

Another measure of stability for a control system are the gain and phase margins. Gain margin is defined as the difference in dB between unity gain and the gain at the point where the phase is -180 degrees. Phase margin is defined as the difference between the phase at unity gain and -180 degrees. The target phase margin of 60 degrees is usually accepted as a tradeoff between loop stability and settling time[8]. Gain margin is the minimum gain for

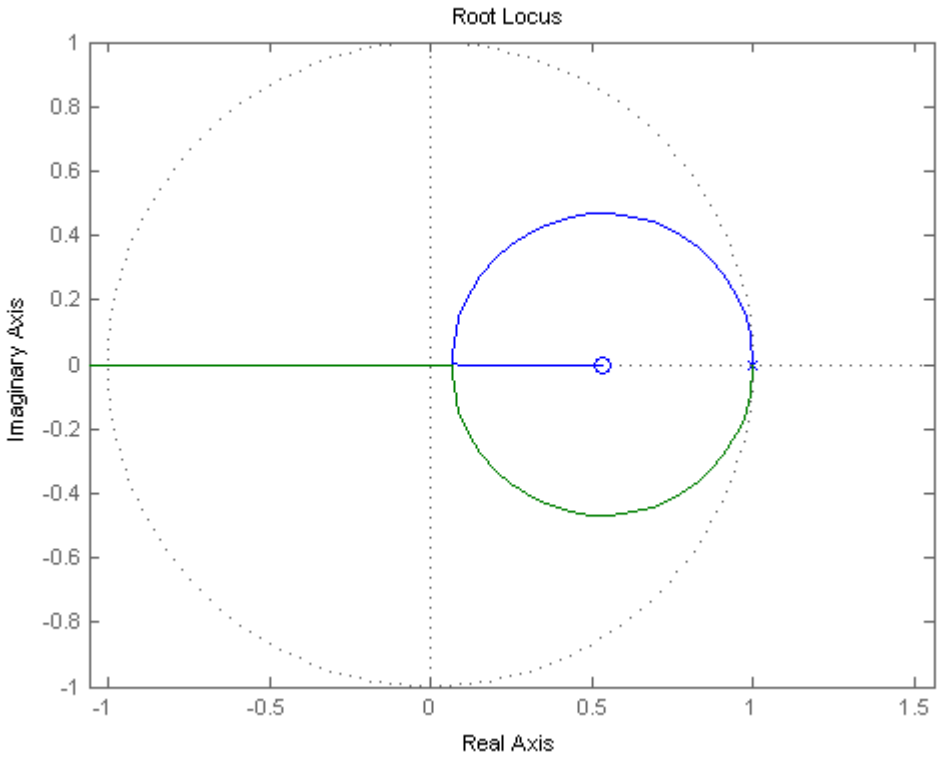

Figure 2.7: Root locus analysis (Expanded View)

the loop to remain stable. Figure 2.8 shows the gain and phase margins for the 2^{nd} order phase locked loop frequency synthesizer with component values from the previous example.

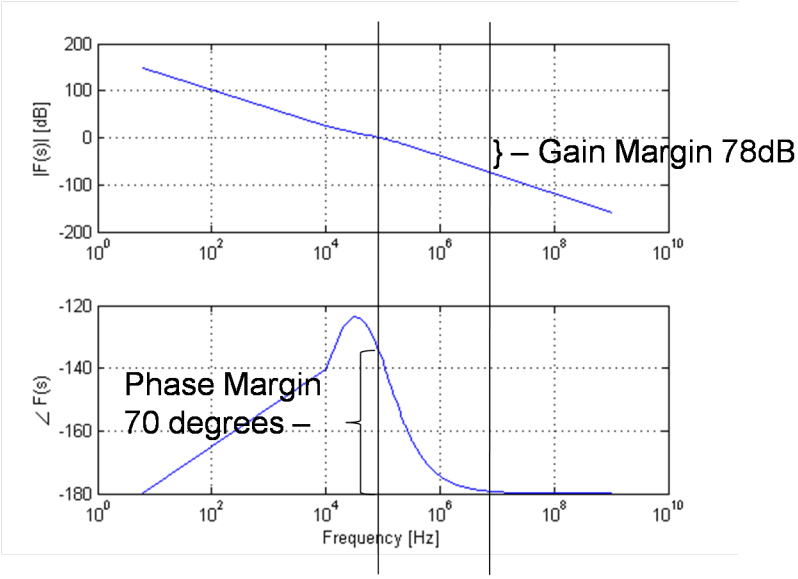

Figure 2.8: Gain and Phase Margins

2.6 Phase Noise in PLL

A major effort in synthesizer design is mitigating noise. It has been stated previously that phase noise of the VCO is the most important specification for the PLL. Noise sources for the loop include thermal noise, transistor noise, timing jitter from the divider and phase detector and reference feedthrough in the charge pump. The noise is further subdivided into in−band and out of band noise. This section introduces the noise sources, classifies them as in−band or out of band noise, and explains how to minimize their impact.

2.6.1 Noise Sources

The first noise source to consider is thermal noise or white noise [19]. Thermal noise is caused by thermal energy causing electron motion in random directions. The noise in a

resistor is

$$v_n^2 = 4kTR \tag{2.35}$$

where T is temperature in degrees Kelvin, k is Boltzmann's constant and R is the value of the resistor.

Shot noise is another white noise source. Shot noise describes the noise of charge carriers when they pass through a barrier like the pn junction. Shot noise from Equation 2.36 is proportional to the current flowing through the junction.

$$i_{n_shot} = \sqrt{2qI} \tag{2.36}$$

Flicker noise or 1/f noise is a noise source that is dominant in−band. The power spectral density of 1/f noise is inversely proportional to frequency[5]. Flicker noise is more of a factor in MOS transistors than in BJTs. It is seen that 1/f noise for the MOS transistor is modeled as a noise voltage and is inversely proportional to area.

$$\overline{v_{nf}^2} = \frac{K_f}{WLC_{OX}f^{\alpha}} \tag{2.37}$$

where α is a process constant and ranges from 2−3. For the BJT it is modeled as a noise current injected at the base.

For a more complete explanation of noise sources see [5]

2.6.2 In−Band vs. Out of Band Noise

All of the noise generated by the PFD, charge pump, divider, and loop filter are considered in−band noise sources. These noise sources are referred to the input. When the noise source frequency is less than the loop bandwidth, the crystal, divider and charge pump dominate the noise[18]. The charge pump being the main culprit for phase noise.

The total Power Spectral Density (PSD) of the crystal oscillator is found by using Leeson's equation[10]. PSD is in units of [rad^2/Hz] or more commonly converted to [dBc/Hz].

Since the Q is very high for crystal oscillators, it only affects the very close in phase noise.

$$\varphi^2_{XTAL}(\Delta\omega) = 10^{-16^{+}_{-1}} \cdot \left[1 + \left(\frac{\omega_0}{2\Delta\omega \cdot Q_L}\right)^2\right]\left(1 + \frac{\omega_c}{\Delta\omega}\right) \tag{2.38}$$

The divider can be considered to be composed of digital switching circuits that are susceptible to timing jitter. Timing jitter occurs when spurious signals, thermal noise, or 1/f noise distort the rising or falling edges of the clock. The divider phase noise is modeled by[12]

$$\varphi^2_{Div_Added}(\Delta\omega) = \frac{10^{-14^{+}_{-1}} + 10^{-27^{+}_{-1}}\omega^2_{do}}{2\pi \cdot \Delta\omega} + 10^{-16^{+}_{-1}} + \frac{10^{-22^{+}_{-1}}\omega_{do}}{2\pi} \tag{2.39}$$

Phase detectors generate 1/f and thermal noise. The dead zone of the PFD must also be minimized because it contributes to the close in phase noise. The dead zone is discussed in Chapter 3.

$$\varphi^2_{PD}(\Delta\omega) = \frac{2\pi \cdot 10^{-14^{+}_{-1}}}{\Delta\omega} + 10^{-16^{+}_{-1}} \tag{2.40}$$

Charge pump noise is generated from mismatch in transistors. Careful matching of the NMOS and PMOS transistors alleviates much of the problem with charge pump noise. This subject is handled more in−depth in Chapter 4.

For the 2^{nd} order passive loop filter, the only noise source is the thermal noise of the resistor. The noise current in the filter is modeled by the transfer function in Equation 2.41. From the transfer function we see that the noise current has a high pass characteristic.

$$i_{n_LPF} = \frac{1}{R} \cdot \frac{v_n s}{s + \frac{C_1+C_2}{C_1C_2R}} \approx \frac{1}{R} \cdot \frac{v_n s}{s + \frac{1}{C_2R}} \tag{2.41}$$

All of the noise sources to this point have affected the in− band phase noise. Conversely, the noise from the VCO is referred to the output. It can be shown that the noise for the VCO has a high pass characteristic. Therefore, for frequencies outside the loop bandwidth, the VCO is the dominant factor.

VCO phase noise is described by [9] as:

$$\varphi^2_{VCO}(\Delta\omega) = \frac{C}{\Delta\omega^2} + D \tag{2.42}$$

where $\Delta\omega$ is the offset frequency from the carrier and C and D are constants of proportionality.

2.7 Conclusion

Analysis has been performed to determine loop characteristics during phase lock and acquisition mode. Stability analysis shows that for the given loop dynamics the system is stable to $>$ 15GHz. Phase noise can be mitigated by following good circuit design practices.

Chapter 3

Phase Frequency Detector

3.1 Introduction

In general, the Phase Frequency Detector (PFD) is implemented as a digital block. The simplest implementation of a PFD is the XOR gate. Next in complexity is the tristate PFD. More complex phase detectors include the five state PFD and the Hogge phase detector and variations of these. This chapter will deal exclusively with the tristate phase detector which is implemented in the fabricated design.

3.2 Tristate PFD

The tristate PFD can be implemented using well known digital blocks. Figure 3.1 shows the tristate PFD implemented with two D−Latches and an AND gate. The divider output and the reference signal are fed into the clock inputs of the two latches respectively. The D−input is tied to to the V_{DD} line in each latch. In the fabricated design the D−Latch has been modified to eliminate the need to tie the D input to V_{DD} and is shown in Figure 3.2.

The PFD operation will be explored next. On the rising edge of either latch the output goes high corresponding to the divider output or the reference signal. When the other latch output goes high the AND gate produces a pulse that resets the latches. The Cadence simulation in Figure 3.3 is included to visualize the functionality of the PFD. When the reference leads the divider it is easily seen that the DOWN pulse (Falling edge triggered) is set high on the falling edge of the reference and is set low on the falling edge of the divider. The UP pulse is a very tiny pulse in this case. It is just wide enough to reset the latches.

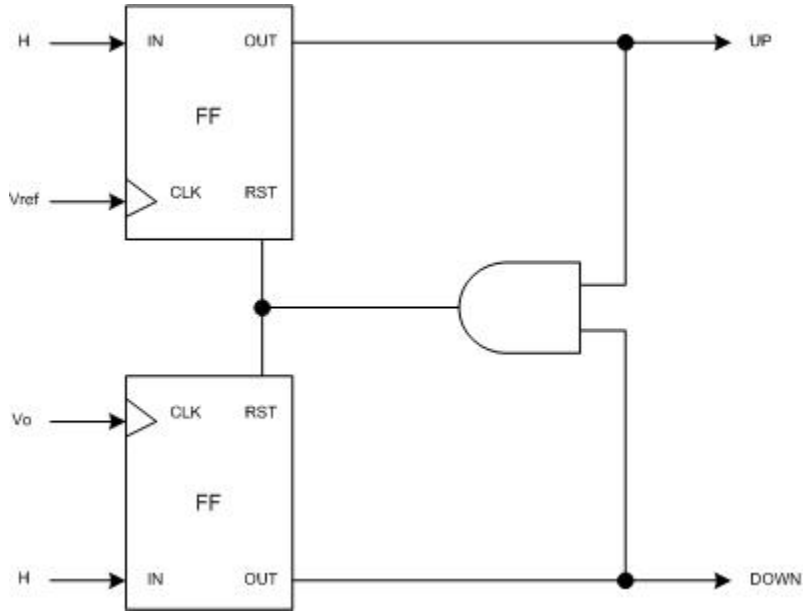

Figure 3.1: Tristate PFD

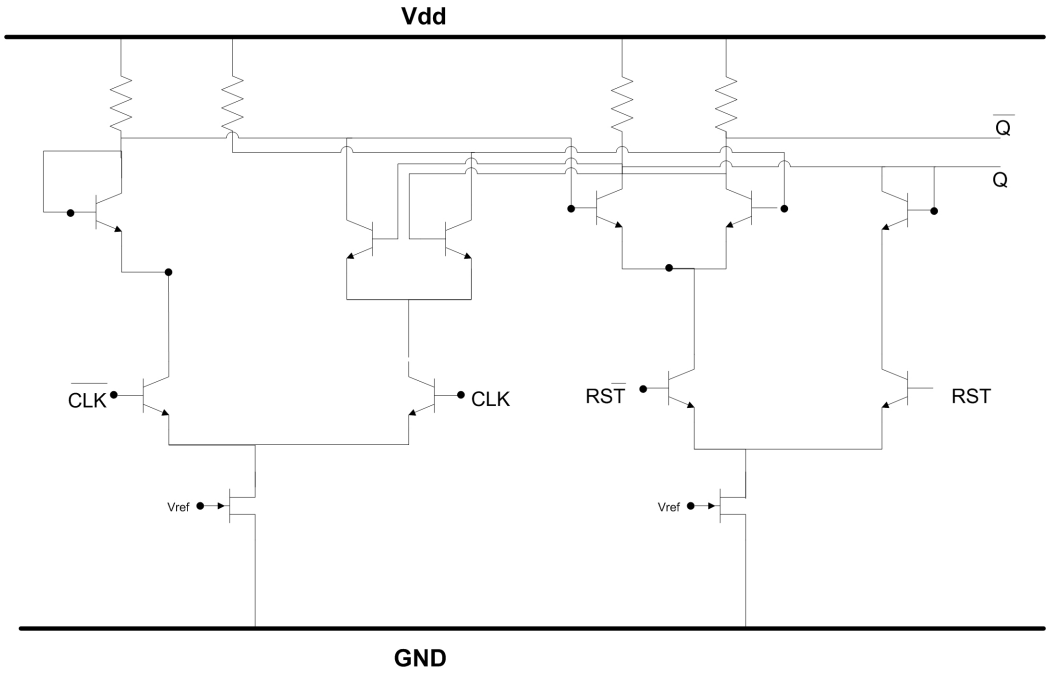

Figure 3.2: Modified folded D−Latch with Reset

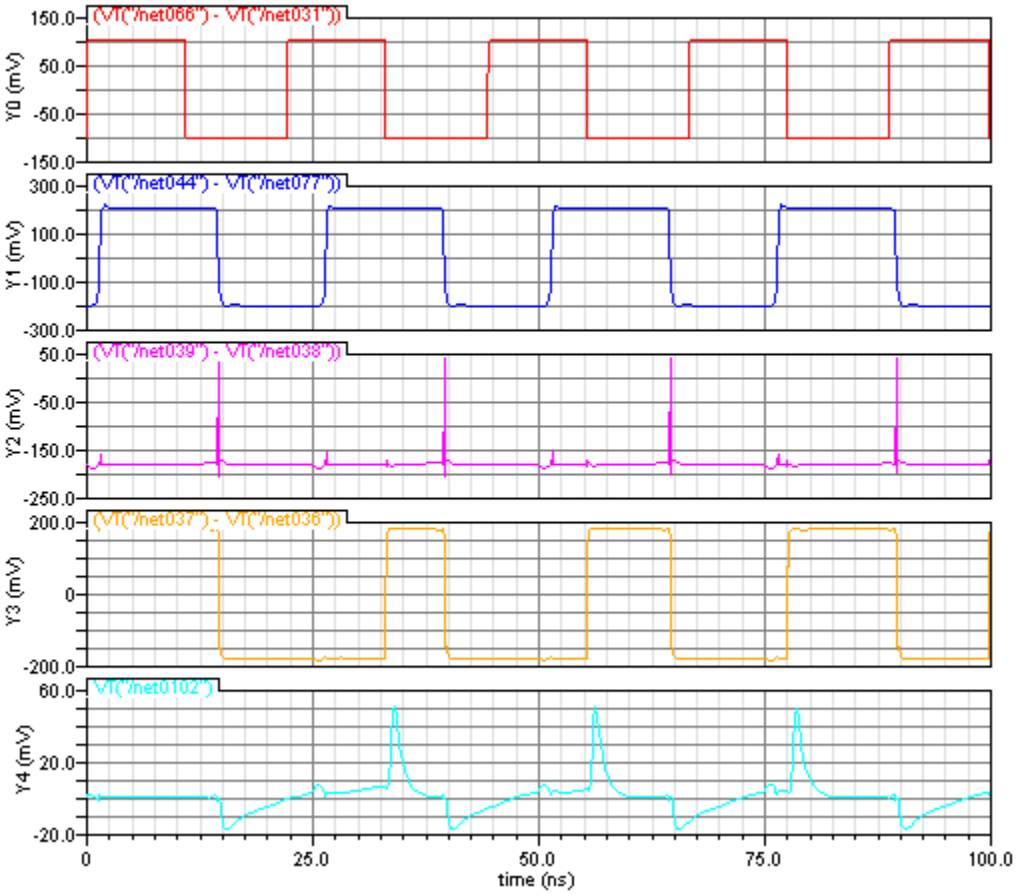

Figure 3.3: PFD simulation signals from top to bottom are: Reference, Divider, UP, DOWN, Charge Pump Output

3.3 PFD Dead Zone

When the phase difference of the input signals becomes small, the correction pulses to the charge pump become small. Finite rise and fall times of the circuit cause narrow pulses that cannot activate the charge pump. If this is the case, the charge pump can no longer follow the input phase for small phase errors. This region is known as the dead zone. This dead zone can be mitigated by adding a delay to the reset line to force the pulses to become wider. The tradeoff is that this widened pulse can cause reference spurs if it becomes too wide.

3.4 Conclusion

A tristate phase−frequency detector has been designed with minimum gate count. The latches have been modified to reduce the number of transistors while still functioning in the same capacity. The circuit delay must be as uniform as possible to reduce the dead zone.

Chapter 4

Charge Pump

4.1 Introduction

The charge pump has a very important function in the loop. It takes the digital pulses from the phase detector and converts them to an analog current to drive the VCO. The charge pump must be carefully designed to mitigate reference feedthrough and phase noise. The Charge pump offers the circuit designer many opportunities to modify or improve performance. In spite of alterations, most charge pumps consist of two current sources and two switches. The main focus of this section will be the differential charge pump because it integrates nicely with the CML phase detector.

4.2 Circuit Design Considerations

4.2.1 Saturation Voltage of MOS Transistors

To utilize the full range of the VCO, it is important to design the current mirror transistors with a small saturation voltage ($v_{DSSat} = v_{GS} - v_T$). This can be accomplished by making the W/L ratio large and the drain current small. This allows the VCO to operate close to the supply rails.

4.2.2 Current Source Matching

Current matching between PMOS and NMOS transistors is a challenge in charge pump design. To minimize current mismatches, it is desirable to keep output resistance high. Note that the output resistance for a MOS transistor is given by

$$r_{DS} = \frac{1}{\lambda I_{DS}} \propto \frac{L}{I_{DS}} \tag{4.1}$$

From Equation 4.1 we see that for purposes of current matching it is good to have a long device. Bipolar transistors have even higher output resistances, but it can be harder to match npn and pnp transistors.

There are ways to increase output resistance in the MOS current source. Resistive degeneration can be added or a cascode transistor can be inserted. For low voltage circuits these techniques must be thought about carefully because they increase headroom. None of these techniques to increase output resistance have been employed for the charge pump in this paper because of the lack of headroom.

4.2.3 Reference Feedthrough

Reference feedthrough occurs when the upper and lower current sources are mismatched. When the phase difference of the input signals to the charge pump is zero, both upper and lower current sources are on for an instant while the Phase-Frequency Detector (PFD) resets itself. If the current sources are mismatched, then there will be a current pulse sent to the VCO that will need to be corrected on the next cycle.

4.2.4 Current Source Matching

To mitigate reference feedthrough the current sources should be matches as closely as possible. This means that the transconductance of the devices should be matched, where transconductance is defined by

$$g_m = \sqrt{2\mu C_{ox}(\frac{W}{L})I_{DS}} \tag{4.2}$$

The mobility of the transistor μ is $2-3$ times larger for the NMOS transistor than for a PMOS transistor. The W/L ratio of the PMOS must be scaled by the same amount to match the NMOS transistors. There are several ways to increase W/L.

1. If the W/L ratio is to be adjusted then the L for the NMOS and PMOS transistors should be the same.

2. The number of fingers can be scaled. If this is the case, then the number of fingers should be odd for matching reasons.

3. It is best to scale the number of transistors and, if possible, use a common centroid layout.

The speed of the circuit is also important. If the circuit cannot respond fast enough, then the charge pump will cause a reduction in gain at low phase differences. This results in a dead zone even if the PFD is designed to be dead zone free.

4.3 Differential Charge Pump

The charge pump shown in Figure 4.2 is a differential charge pump for a BiCMOS process. The input transistors are Bipolar for ease of switching, while the charge pump itself is CMOS.

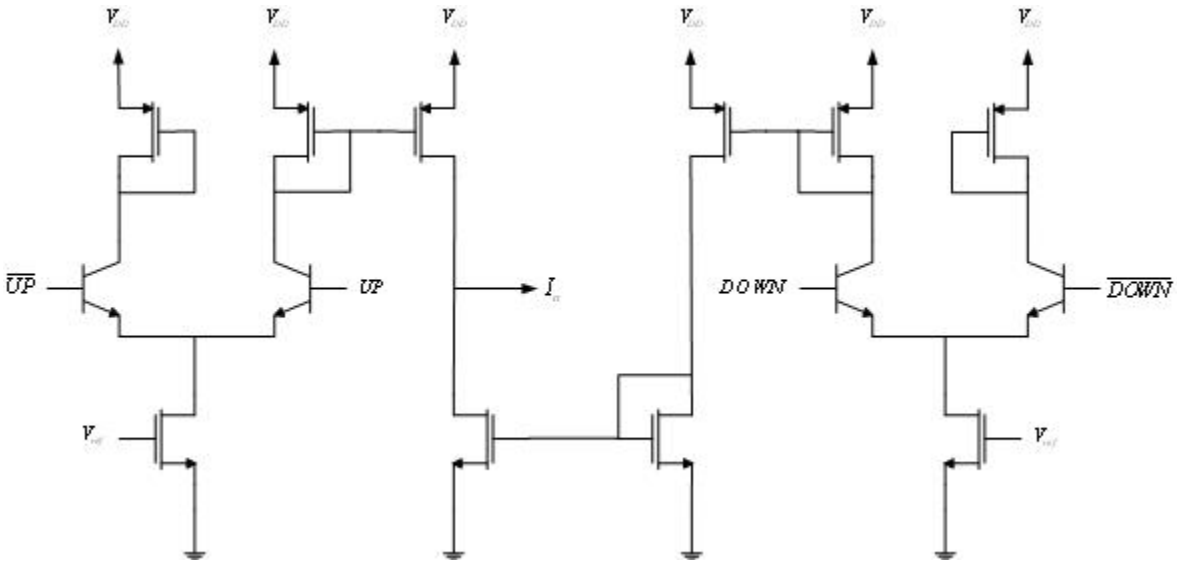

Figure 4.1: Differential BiCMOS Charge Pump

This charge pump has good current matching because the UP and DOWN input stages are very symmetric. By virtue of being a differential charge pump, this circuit has good common mode rejection.

4.4 Tunable Current Source

A tunable current source can be made simply by taking the reference current produced by the bandgap and then scaling it up. Programming in binary steps is achieved by placing swiches in series with the current mirrors. The current is programmed in binary steps as given by

$$I_{ref} = (8b_3 + 4b_2 + 2b_1 + b_0)I_{bias} \tag{4.3}$$

The tunable current source can be implemented to adjust the current flowing in the charge pump for one of a couple of reasons. Because of the uncertainty of the fabrication process it might be desirable to tune the current for optimal noise performance. The bandwidth of the loop can be changed by the charge pump, so tuning the charge pump current could be instrumental in setting the loop dynamics.

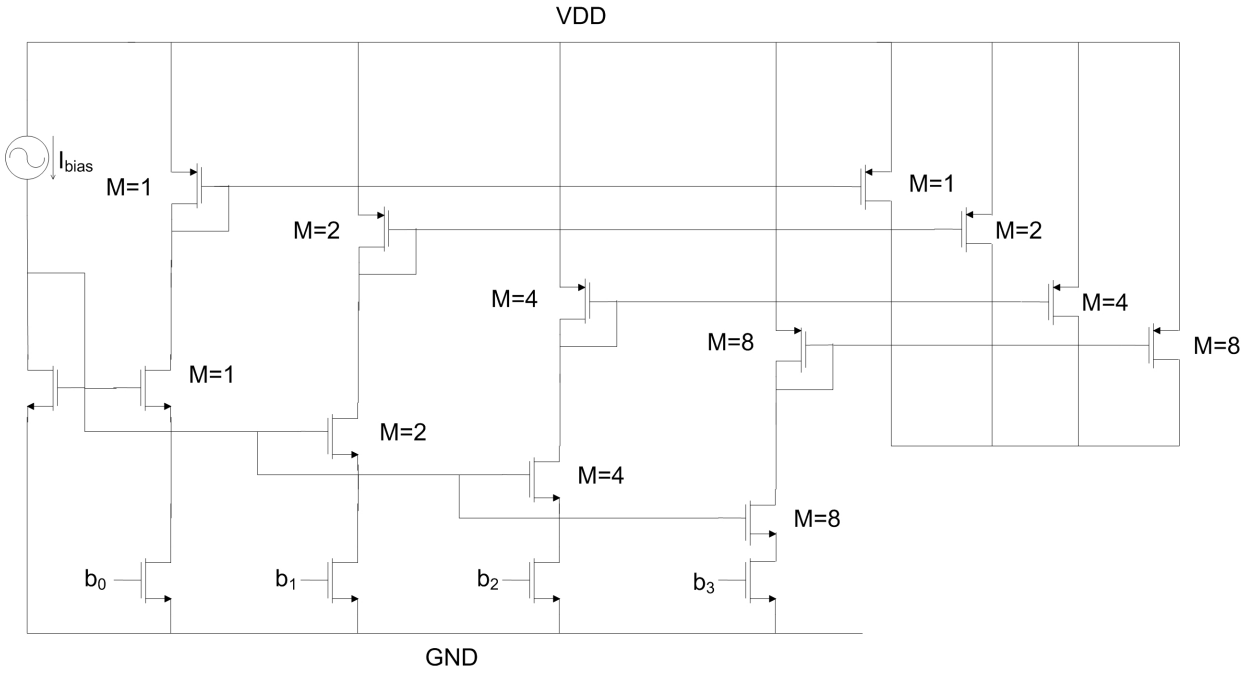

Figure 4.2: Tunable current source

4.5 Conclusion

Proper sizing of the transistors in the charge pump can mitigate reference feedthrough and close in spurs in the output spectrum of the VCO. Although not implemented in the author's fabricated design, the tunable current source is very useful in optimizing noise performance. The tunable current source can be used for tuning bandwidth and settling time. This function is covered because it could be useful to implement in a future design.

Chapter 5

Loop Filter

5.1 Introduction

Because the VCO is controlled by voltage and the output of the charge pump is a current, a function of the loop filter is to convert from current to voltage. The loop filter low pass filters the tune line to the VCO reducing the ripples that would otherwise cause undesired effects in the VCO. In addition, the loop filter adds a loop stabilizing zero as can be seen in the system level analysis.

Active loop filters use transistor amplifiers to implement the low pass filter [30], [31]. This can be done easily, but it is important that the loop filter does not introduce noise to the tune line. Active loop filters introduce power supply noise, and transistor noise. For this reason, active loop filters are not desired.

Passive filtering is the most widely used choice for loop filter. If the loop filter could be integrated on chip, the only noise that would be added to the system is the thermal noise in the resistor. Because the loop filter capacitances must be large it is not easy to integrate the loop filter on chip. Parasitic inductances from bonding wires and PCB level coupling of noise sources make the tune line very susceptible to noise.

A third option is presented in [27]. Although this paper turns out to be falsified, the concept has been verified in [28], [29], and others. This method of implementing the loop filter offers promising results for integrating the loop filter on chip without increasing noise.

5.2 Passive Loop Filter

The second order loop filter is shown in Figure 5.1. The second order passive loop filter yields a straight forward analysis. Figure 5.2 shows the transfer function of the second

order passive loop filter. The transfer function of the second order loop filter is of the form

$$F(s) = \frac{v_c}{I_{cp}} = \frac{1 + sC_1R}{s(C_1 + C_2)(1 + sC_sR)} \tag{5.1}$$

where

$$C_s = \frac{C_1C_2}{C_1 + C_2} \tag{5.2}$$

It should be noted that the filter transfer function is a transimpedance function.

A magnitude plot of the second order loop filter is shown in Figure 5.2. Component values for this loop filter are: $R = 20k\Omega$, $C_1 = 5nF$, and $C_2 = 500pF$. This transfer function is verified with a Cadence simulation in Figure 5.3.

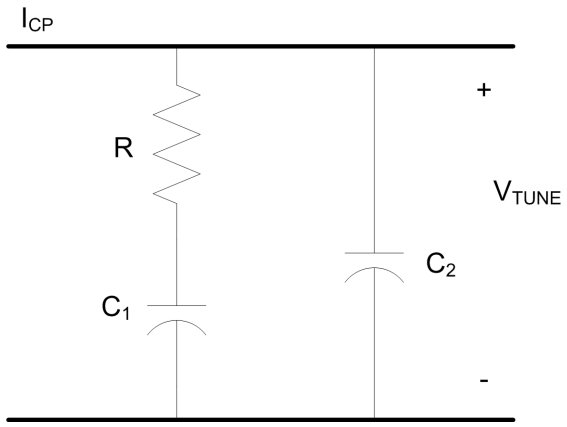

Figure 5.1: 2^{nd} order loop filter

From either of these plots it is seen that there is a pole at DC. The slope continues at $-20dB/dec$ until the zero at $s = \frac{1}{RC_1}$ where the slope levels off. The slope is zero until the high frequency pole is reached and then the curve resumes its $-20dB/dec$ descent.

For higher order loop filter transfer functions the reader is referred to [24].

5.3 Dual Path Loop Filter

The dual path loop filter presented in [27] is a promising prospect in integrating the loop filter on chip. Simply put, the dual path loop filter uses two charge pumps that are

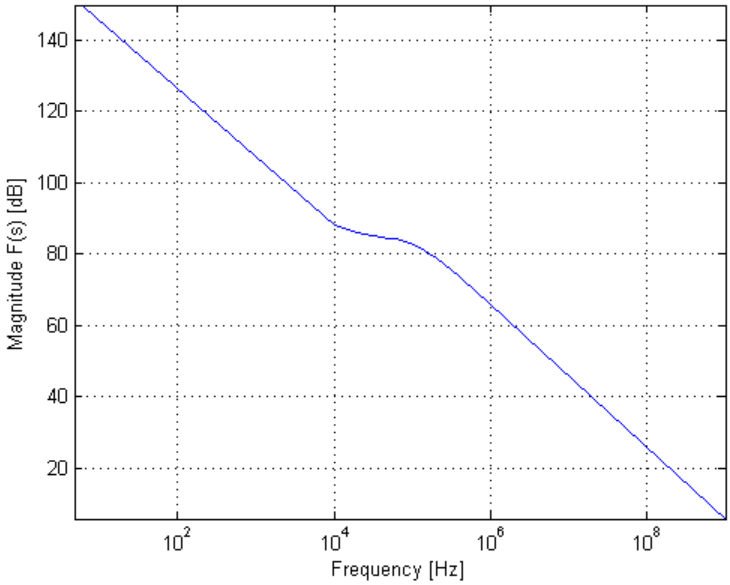

Figure 5.2: 2^{nd} order loop filter transfer function simulated with Matlab

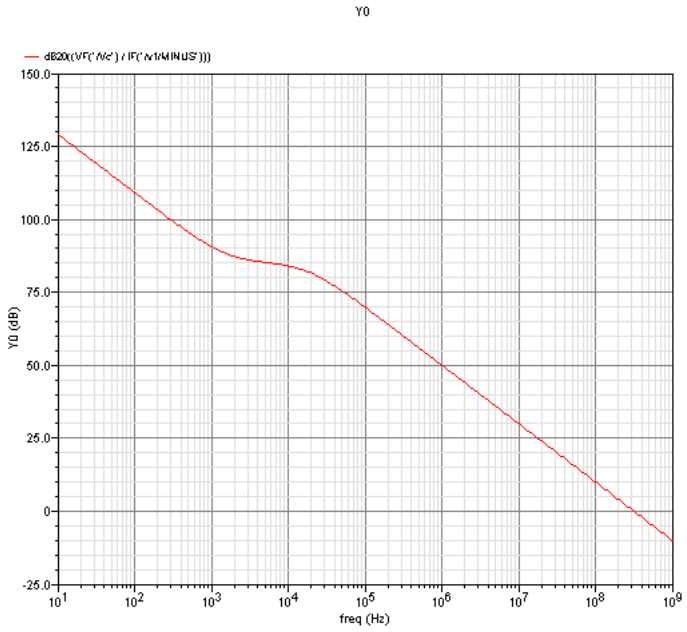

Figure 5.3: 2^{nd} order loop filter transfer function simulated with Cadence

equal in phase but differ in magnitude. The charge pumps interact with the loop filter as shown in Figure 5.4.

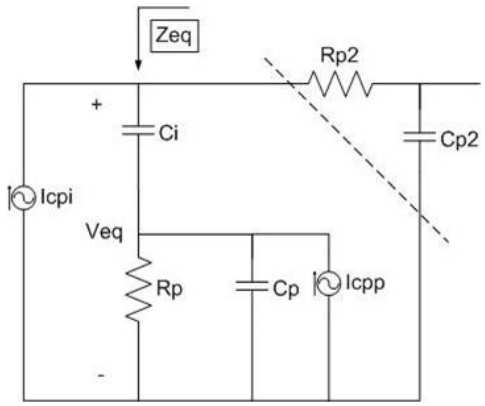

Figure 5.4: Dual path loop filter circuit diagram

Neglecting the higher order components R_{P2} and C_{P2} we can find the transimpedance transfer function of this loop filter. The transimpedance transfer function is defined as

$$Z_{eq} = \frac{v_{eq}}{I_{CPI}} \tag{5.3}$$

where v_{eq} is the voltage from C_I to ground and is found analytically as

$$v_{eq} = Z_{C_I} I_{CPI} + R_P \left(I_{CPI} + I_{CPP} \right) \tag{5.4}$$

So the transimpedance transfer function is

$$Z_{eq} = \frac{v_{eq}}{I_{CPI}} = Z_{C_I} + R_P \cdot (1 + \frac{I_{CPP}}{I_{CPI}}) \tag{5.5}$$

We see that the resistance is effectively multiplied by the ratio of the charge pumps. The benefit of this structure is that the capacitor can now be reduced in size and the same $1/RC$ time constant can be achieved. Figure 5.5 shows that for a charge pump ratio of 10:1 the zero in the transfer function can be reduced by a frequency decade.

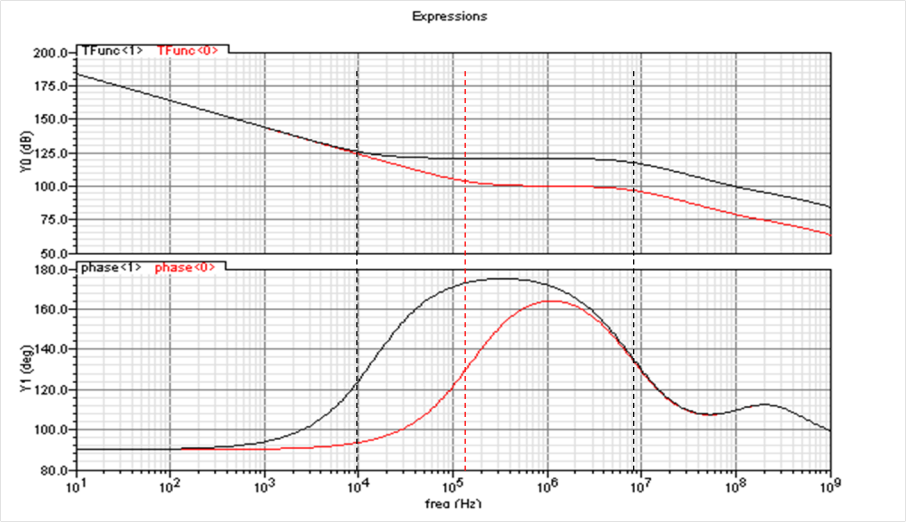

Figure 5.5: Dual path loop filter compared to traditional 2^{nd} order loop filter

The effective multiplication of the resistance is sometimes called "'Noiseless Resistor Multiplication[27]"' because the extra charge pump is not connected directly to the tune line and does not directly add any noise to the tune line.

5.4 Simplification of Dual Path Loop Filter Structure

The structure put forth by A. Maxim calls for two charge pumps. We propose a simplification to Maxim's structure. Obtaining the ratio of the two charge pumps as described earlier is as simple as adding a CMOS current mirror as shown in Figure 5.8. For a current mirror ratio of 10:1 the same loop filter magnification can be achieved without the need for two distinct charge pumps.

5.5 Tunable Loop Filter

The ability to electronically shift the poles and zeros of the loop filter is an entertaining concept. With this ability it might be feasible to design a frequency synthesizer with one loop filter specification for frequency acquisition (wider bandwidth) and one specification for phase lock (Faster settling time).

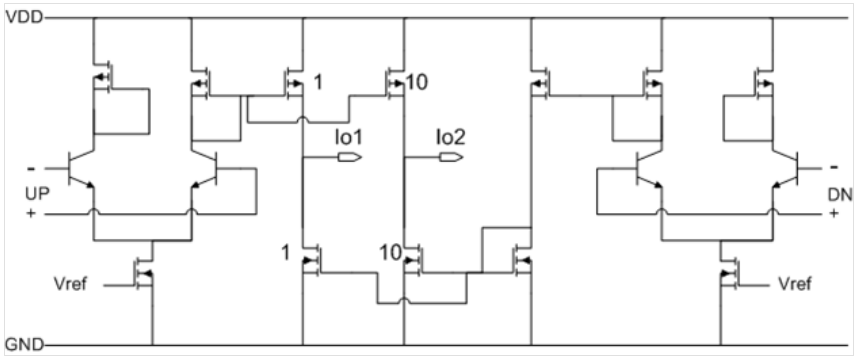

Figure 5.6: Proposed tunable loop filter

One possibility is to use a tunable current source. A binary weighted current source has been suggested for the purpose of adjusting charge pump current for optimum noise performance[6]. A four bit programmable current source like the one in Figure 5.7 allows for current tuning from $I_{bias} - 15I_{bias}$. We propose the use of the tunable current source for an adjustable loop filter. Diagram for the proposed loop filter is shown in Figure 5.8.

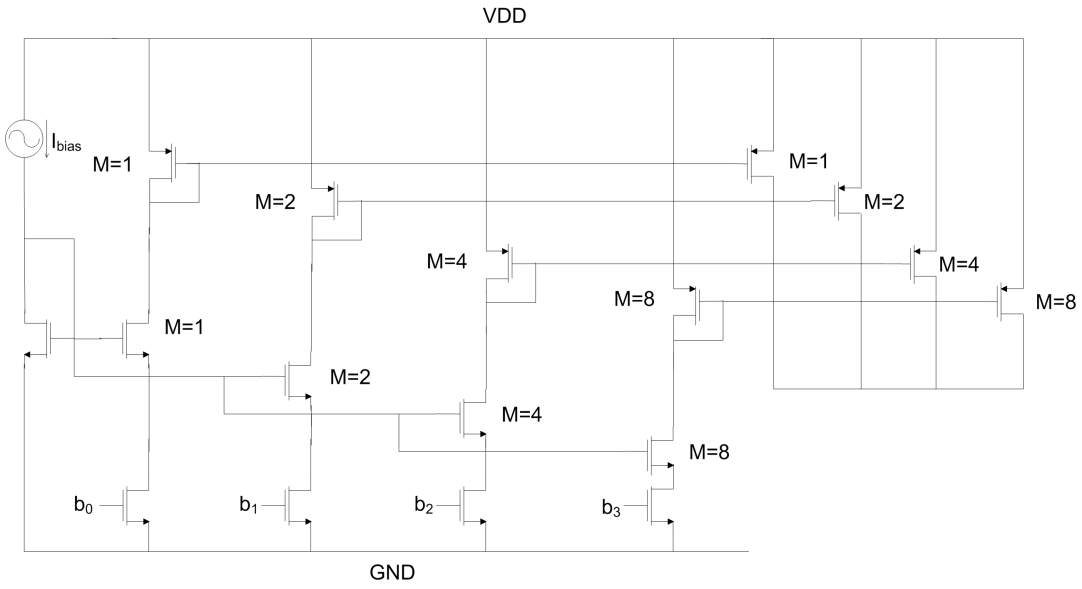

Figure 5.7: Tunable current source

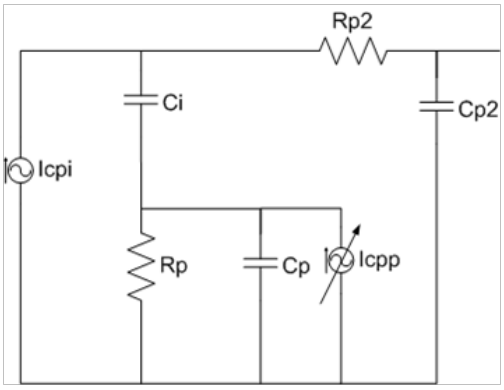

Figure 5.8: Proposed tunable loop filter

5.6 Conclusion

The simplest and most direct loop filter is the passive loop filter. This filter is the most commonly used. Indeed, the second order passive loop filter is the one chosen by the author to implement filtering for the fabricated design.

The dual path loop filter seems promising for future designs. One problem with this architecture is that it seems to move the zero but not the pole of the loop filter. It is of most interest to shift the pole of the system, moving the corner lower in frequency.

Chapter 6

Voltage Controlled Oscillator

6.1 Introduction

This chapter will briefly discuss the voltage controlled oscillator design. The −gm cell has been designed for the fabricated PLL. Please note that a thorough discussion of VCO design is omitted. The design effort for the VCO has been a part of the research effort by another student. The full analysis will be presented in a thesis by William Souder.

6.2 Negative Gm Oscillator

The negative transconductance oscillator is so called because the effective resistance seen at the output is negative. Looking at Figure 6.1 we immediately see that $v_{be1} = -v_{be2}$ and from that $v_x = v_{be2} - v_{be1}$. So then $v_x = -v_{be2} - v_{be2} = -2v_{be2}$. The collector current can be expressed as $i_c = gm \cdot v_{be}$. From here we see that the output resistance is

$$\frac{v_x}{i_c} = -\frac{2}{gm} \tag{6.1}$$

and does in fact appear negative to the output. This negative resistance is important to grow oscillations.

The full circuit for the −gm oscillator is shown in Figure 6.2. Oscillation occurs when the imaginary impedances cancel and the negative resistance is grown to be larger than the positive output resistance.

Figure 6.3 shows a K_{vco} of 1GHz/V. The charge pump of this PLL must be designed with care to prevent pulses from occuring on the tune line. Tail current for this design is 8mA to provide adequate drive strength for the divider.

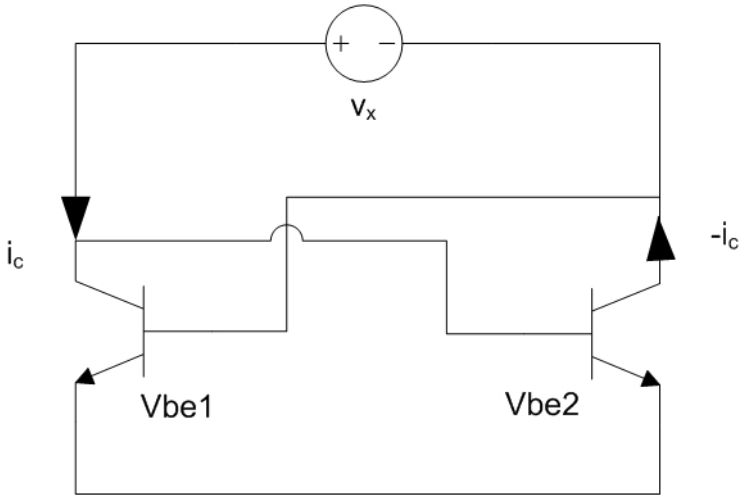

Figure 6.1: AC model of negative gm oscillator analysis

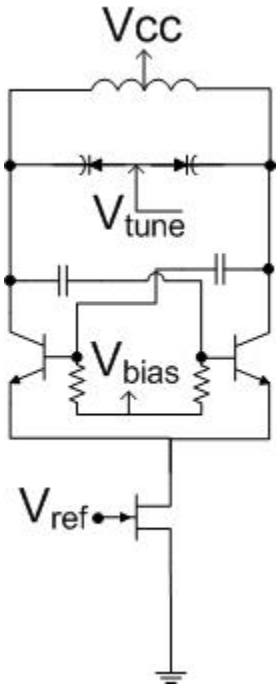

Figure 6.2: Negative gm oscillator with varactor tuning

Figure 6.4 shows that, in simulation, the VCO has a phase noise of −95dBc/Hz at a 1MHz offset from the carrier. The phase noise has a −20dB/dec slope to greater than 100MHz offset from the carrier.

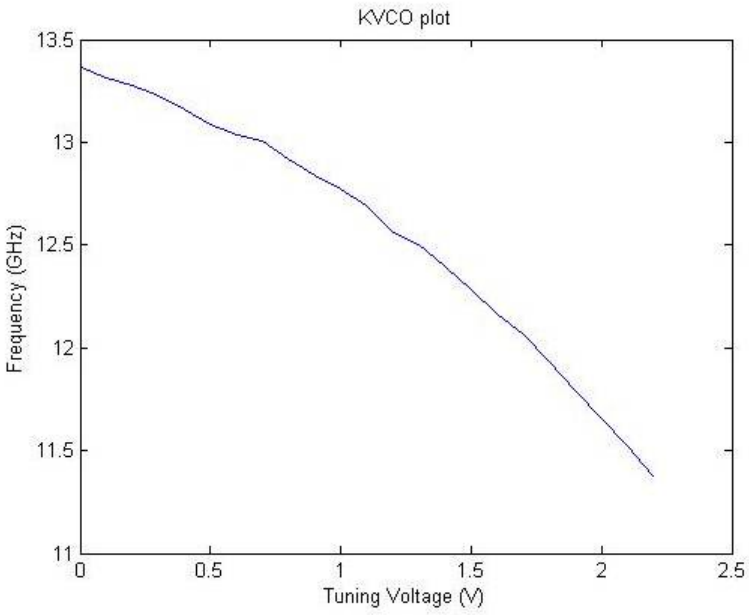

Figure 6.3: Simulated K_{VCO}

6.3 Conclusion

The theory of operation of the −gm oscillator has been presented in this chapter. The fabricated VCO has been carefully designed to provide enough drive strength for the divider. Phase noise has been simulated and the parameter K_{VCO} has been determined graphically.

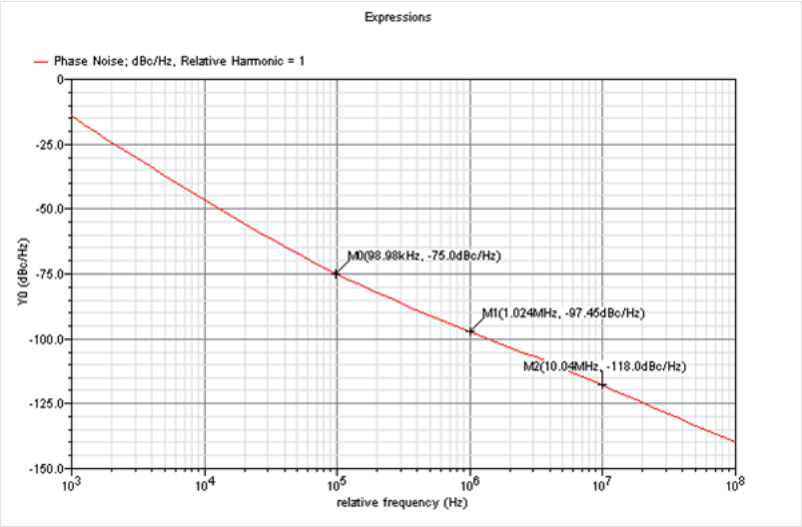

Figure 6.4: Simulated VCO phase noise

Chapter 7

Divider Circuit Design

7.1 Introduction

The design of the divider in the frequency synthesizer is a matter for careful consideration. The divider contributes to the close in phase noise, controls the channel spacing and step size, and is a large contributing factor in total loop power consumption.

There are several options for divider design. Pulse swallow counters are one of the most common divider implementations, but often they cannot program all frequencies in a required band. The circuit with all two/three cells is a truly modular option, but does not always present the lowest power consumption. This chapter presents a third alternative, the Multi−Modulus Divider (MMD). The MMD architecture is similar to the architecture with all two/three cells. It differs in the fact that the last stage of the MMD is a divide by P/P+1 stage.

A generic algorithm [22] is presented to determine the minimum number of cells. A specific example is included to illustrate the differences between the architectures.

Lastly, the approach to minimizing the current in each individual cell is presented. Simulated results of the MMD designed for 13GHz, implemented in 0.13μm SiGe BiCMOS technology are presented in the final section.

7.2 Design Challenges

Divider design is one of the most important challenges in designing a frequency synthesizer. The first stage of the divider must operate at the highest frequency in the loop. The divider must be carefully designed to have minimum current consumption, but must still switch fast enough to handle the highest frequencies in the loop.

The divider contributes to the close in phase noise of the loop. Therefore, the output of the divider must be clean to reduce jitter and spurs. Properly sizing the transistors and bias current help reduce jitter.

7.3 Divider Architectures

7.3.1 Dual Modulus Prescaler with Pulse Swallow Counter

The pulse swallow counter is a commonly used divider architecture. It consists of a dual modulus prescaler, programmable frequency divider M, and down counter A as shown in Figure 7.1. The programmable counter is a frequency divider with programmable division ratio M. The pulse−swallow divider operation is described in [6] and is reiterated here.

1. The M divider divides the output frequency of the dual−modulus prescaler by M.
2. The A down counter is loaded with an initial value of A at the rising edge of the M divider output and is clocked by the input signal of the M divider.
3. The A down counter value is reduced by one at every rising edge of its value reaches zero, it will remain zero unless the next load signal loads a start value to the counter
4. The A down counter output is high when the counter value is nonzero, which toggles the dual−modulus divider to divide by P + 1, and its output is low when the counter value is zero, which toggles the dual−modulus divider to divide by P.
5. The hold input to the down counter can be connected to a fractional accumulator's carry out to achieve a fractional division ratio

The average division ratio of the pulse−swallow divider is

$$Div = (P+1)A + (M-A)P = PM + A \tag{7.1}$$

Under some conditions it is not possible to synthesize all channels with this counter. The programmable blocks must be designed carefully to aleviate this problem. For normal

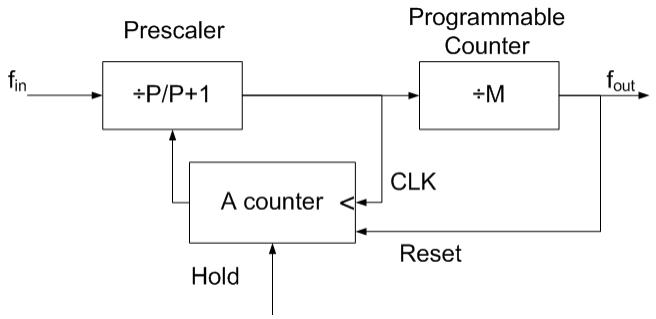

Figure 7.1: Pulse Swallow Divider

operation $M, A = 0 - \min\{P-1, M\}$. The condition so that no channels are skipped is $M > P-2$. No channels are overlapped when $A < P$ and the minimum ratio for continuous programming is P(P-1).

The architecture for the pulse swallow divider is easily designed but implementing this divider presents several design challenges. Firstly, the architecture requires three different blocks. Design time and the layout effort are greatly increased because the design is not modular. Power dissipation is increased because the counters present a substantial load at the output of the prescaler[20]. Another drawback of this architecture is that a $\Sigma\Delta$ modulator cannot be implemented.

7.3.2 Vaucher's Structure

A very elegant and modular divider design is the one developed by C. Vaucher[20]. The design is modular because the divider can be scaled by cascading 2/3 cells as shown in Figure 7.2. Design time and layout time are significantly decreased. The period of a chain of 2/3 cells is

$$N = \left(2^n + 2^{n-1}p_{n-1} + 2^{n-2}p_{n-2} + ... + 2^1 p_1 + p_0\right) \tag{7.2}$$

The 2/3 cell in Figure 7.3 is the backbone of Vaucher's architecture. The 2/3 cell can be thought of as a digital block as it is comprised of latches and AND gates. The function

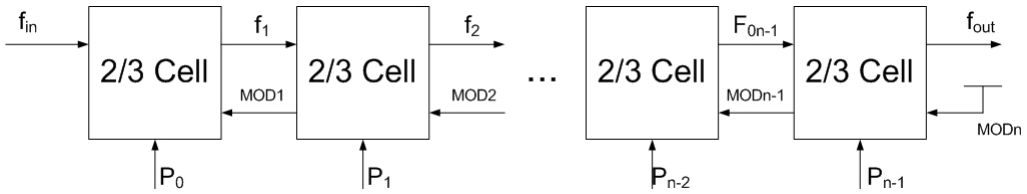

Figure 7.2: Divider with all Two/Three Cells

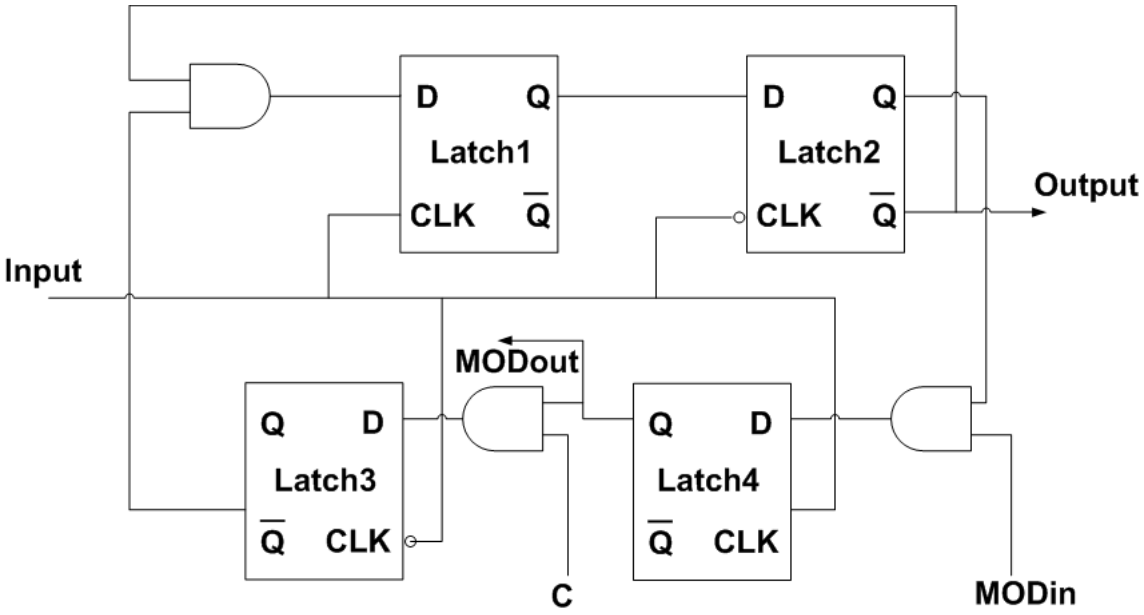

Figure 7.3: Two/Three Cell

of the 2/3 cell can be easily recognized if we begin by looking at the divide by two circuit in Figure 7.4. It is easily seen that if the modulus input (MOD_{in}) and control bit (C) are logic zero, AND gate 1 can be ignored and the resulting circuit is just a divide by two circuit. In fact, the only case where the circuit performs differently is when both MOD_{in} and C are logic 1. When this occurs the feedback path becomes active and Latch3 and Latch4 "swallow" a pulse. This functionality is demonstrated in a Cadence simulation in Figure 7.5.

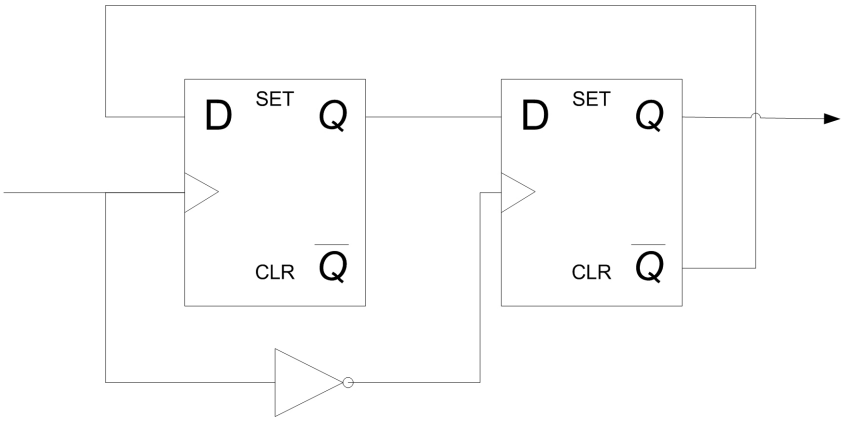

Figure 7.4: Divide by Two

7.3.3 Designing P/P+1 Cells

The design of a 2/3 cell can be extended to any P/P+1 division ratio easily if P is chosen to be even. If P is chosen to be an even number then the example of the divide by two circuit can be reused here. The divide by two circuit can be cascaded to develop the P division ratio. Then just as in the divide by 2/3 cell, two latches can be placed in the feedback path to "Swallow" an extra pulse yielding the P+1 ratio.

For example: In the case of the divide by 8/9 cell, four flip−flops are cascaded to give the divide by eight. Then two latches are placed in the feedback path to yield the divide by nine case. Figure 7.7 shows the output of an 8/9 cell, input signal, and control bit value simulated in cadence.

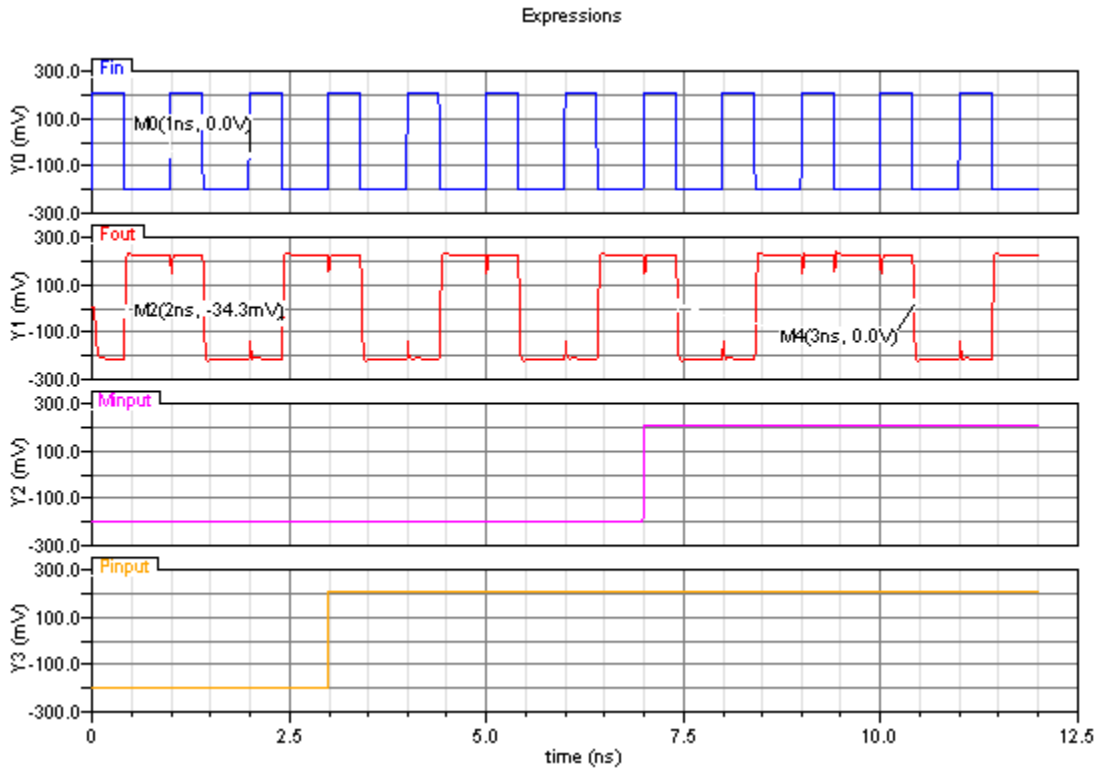

Figure 7.5: Divide by Two/Three with signals from top to bottom: $\mathrm{F}_{in}, F_{out}, Modin, P$

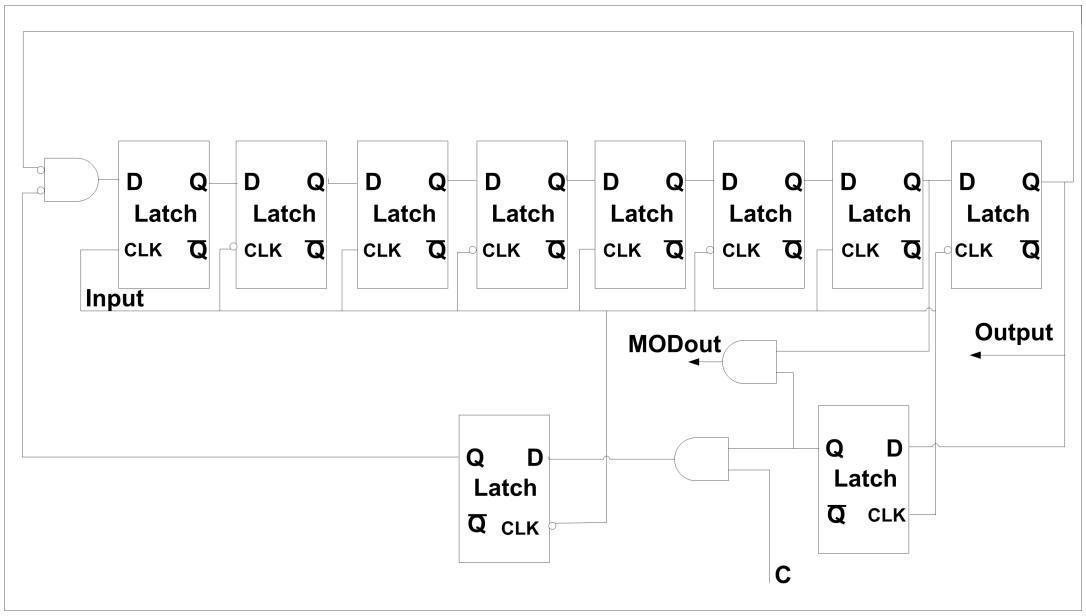

Figure 7.6: Divide by 8/9 Cell

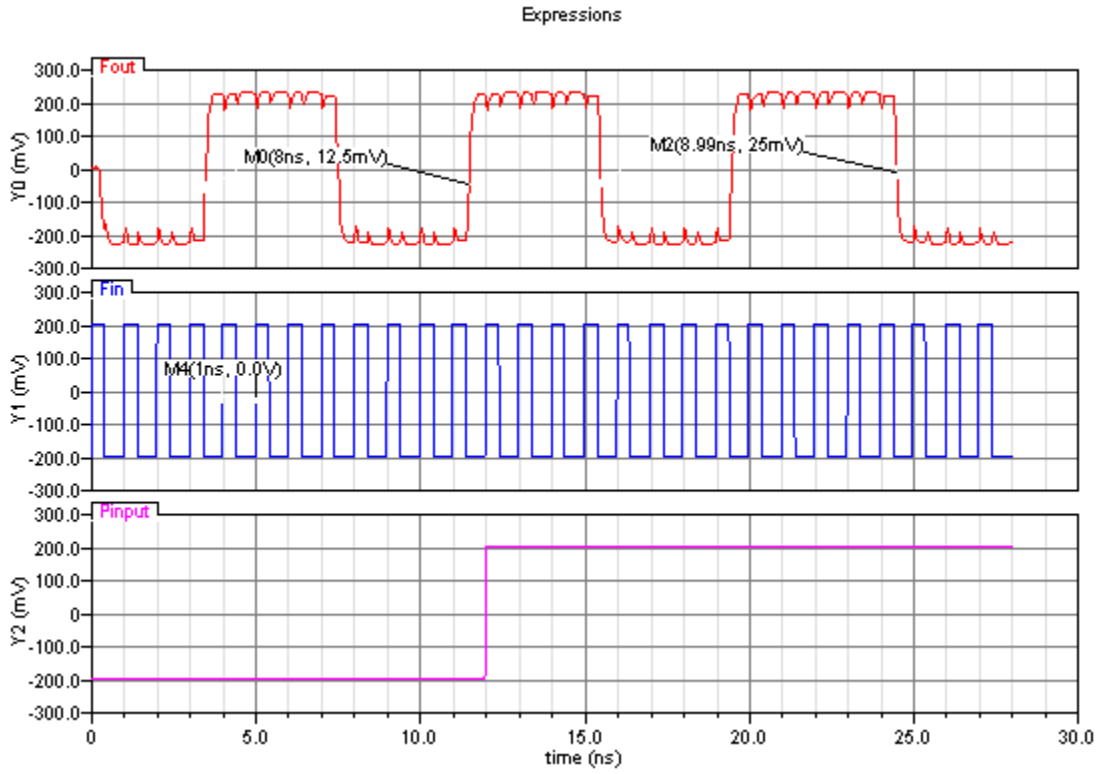

Figure 7.7: Cadence Simulation of 8/9 Cell

7.3.4 Multi−Modulus Divider

The divider architecture with all 2/3 cells may not necessarily end up with the minimum gate count and power consumption [23]. We therefore introduce a modification to the structure with all 2/3 cells, where the minimum division ratio is increased by the P/P+1 cell.

The MMD can easily synthesize all frequencies in the band of interest. It has another advantage over other architectures. A $\Sigma\Delta$ modulator can be included to reduce the in−band noise. Therefore, an MMD is highly desired in delta-sigma fractional-N frequency synthesis [32].

7.4 Generic MMD Architecture

A generic algorithm to determine the minimum number of cells has been developed in [22]−[23] and will be presented here for completeness.

The generic MMD architecture includes cascaded 2/3 cells with a dual modulus prescaler (P/P+1) cell at the end. This is done so that a unit step increment of one can be preserved. If a step size other than one is preferred, then a fixed ratio divide by S cell is added to the front of the divider. For this architecture shown in 7.8 the division ratio is shown as

$$N = \left(2^{n-1} \cdot P + 2^{n-1}C_{n-1} + 2^{n-2}C_{n-2} + ... + 2^1 C_1 + C_0\right) \cdot S \tag{7.3}$$

From this equation it is seen that the division ratio is programmable with a unit step increment and the minimum division ratio is increased.

1. Assume that the required division ratios are from D_{min} to D_{max}; then, the number of divisor steps is given by

$$Number\ of\ divisor\ steps\ = (D_{max} - D_{min} + 1) \tag{7.4}$$

2. If the required range is greater than the minimum division ratio, D_{min}, the MMD should be constructed using an architecture with all divide−by−2/3 cells.

3. The implemented MMD range, defined from M to N, may be larger than the required range D_{min} to D_{max}. Initially, however, the minimum implemented division ratio M is set to D_{min}.

4. Now the number of cells required becomes

$$n = \lceil \log_2 (D_{max} - M + 1) \rceil \tag{7.5}$$

where the function $\lceil\ a\ \rceil$ denotes rounding the number a to the nearest integer larger than a.

5. The division ratio for the last cell can be found from

$$P = \left\lfloor M/2^{n-1} \right\rfloor \tag{7.6}$$

where the function $\lfloor\ a\ \rfloor$ denotes rounding the number a to the nearest integer less than a.

6. if $M/2^{n-1}$ is not an integer, then reset $M = P \cdot 2^{n-1}$, and go to step 4.

7. If $M/2^{n-1}$ is an integer, it is necessary to evaluate whether using a single $P/P+1$ cell or using any combination of cascaded cells, such as $2/3 \rightarrow \lfloor P/2 \rfloor / (\lfloor P/2 \rfloor + 1)$, or $2/3 \rightarrow 2/3 \rightarrow \lfloor P/4 \rfloor / (\lfloor P/4 \rfloor + 1), ...,$ or using all 2/3 cells will achieve lower current consumption and smaller die size.

8. The final MMD architecture is thus a combination of stages, as shown in Figure 7.8. If only 2/3 cells are used, then the total number of cells required is

$$n_{2/3} = \lceil \log_2 (\, D_{max} + 1\,) \rceil - 1 \tag{7.7}$$

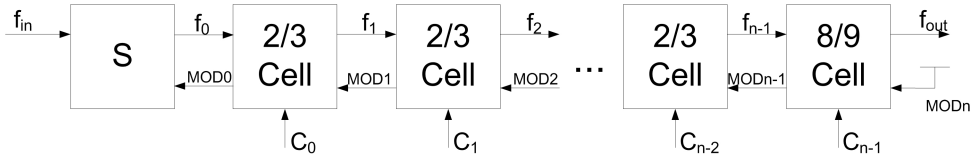

Figure 7.8: Generic Architecture for Multi−Modulus Divider

7.4.1 *Example: Design MMD for X-band Radar*

For a 13 GHz PLL used in X-band radar transceivers, the MMD is required to cover the division range from 131 to 154 with a unit increment. Following the generic algorithm the MMD architecture presented in the previous section, we obtain:

1. *Number of divisor steps* $= (D_{max} - D_{min} + 1) = 154\text{-}131\text{+}1 = 24$

   The required division range is not greater than the minimum division ratio. Therefore, we continue the algorithm.

2. The implemented MMD range, defined from M to N, may be larger than the required range D_{min} to D_{max}. Initially, however, the minimum implemented division ratio M is set to D_{min}.

3. Now the number of cells required becomes

$$n = \lceil \log_2 (D_{max} - M + 1) \rceil = \lceil \log_2 (154 - 128 + 1) \rceil = 5 \tag{7.8}$$

4. The division ratio for the last cell can be found from

$$P = \left\lfloor M/2^{n-1} \right\rfloor = \left\lfloor 128/2^{5-1} \right\rfloor = 8 \tag{7.9}$$

5. The final MMD architecture is thus a combination of stages, as shown in Figure 7.8. If only 2/3 cells are used, then the total number of cells required is

$$n_{2/3} = \lceil \log_2 (D_{max} + 1) \rceil - 1 = \lceil \log_2 (154 + 1) \rceil - 1 = 8 \tag{7.10}$$

So the optimum architecture in this case is $2/3 \rightarrow 2/3 \rightarrow 2/3 \rightarrow 2/3 \rightarrow 8/9$ as shown in Figure 7.12.

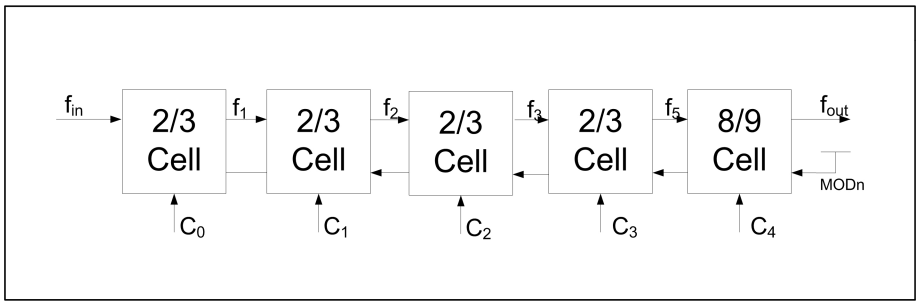

Figure 7.9: Multi−Modulus Divider

7.4.2 Design Simulation of MMD in Cadence

Extensive simulation has been performed to ensure the correct functionality of the MMD. Circuit level simulation has been performed using the Cadence's Spectre.

The output of the divider is shown for two cases: divide by 128 and divide by 159 in Figures 7.10 and 7.11 respectively. Often it is desired to take the output at the modulus output because it has a sharper edge instead of the 50% duty cycle output. Figure 7.12 shows the output of the divider with the modulus outputs of each stage.

7.5 Minimizing Current

The MMD from the previous example has been determined to have the minimum number of cells. Power consumption can be further reduced if the specific current consumption in each cell is examined.

We know that faster switching is obtained, to a point, by driving the devices with higher current. The first stage must handle an input of 13GHz and therefore, must have the highest current. As the frequency is reduced in each stage, the current can be reduced.

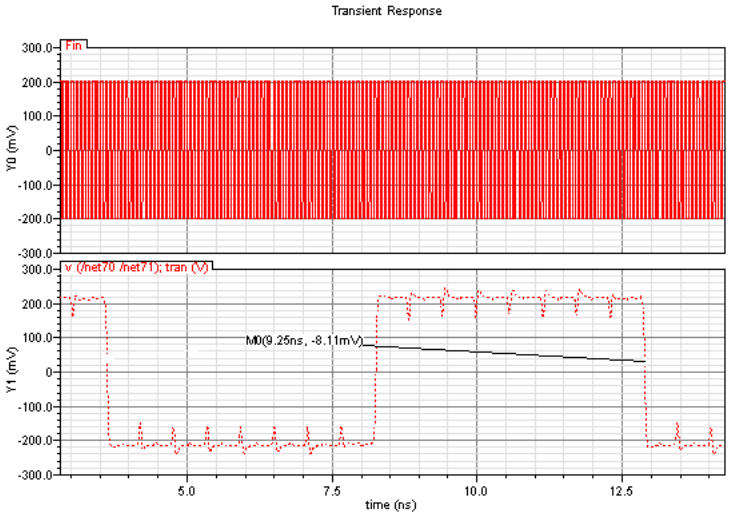

Figure 7.10: MMD Output for the Divide by 128 Case with $f_{in} = 13.84GHz$

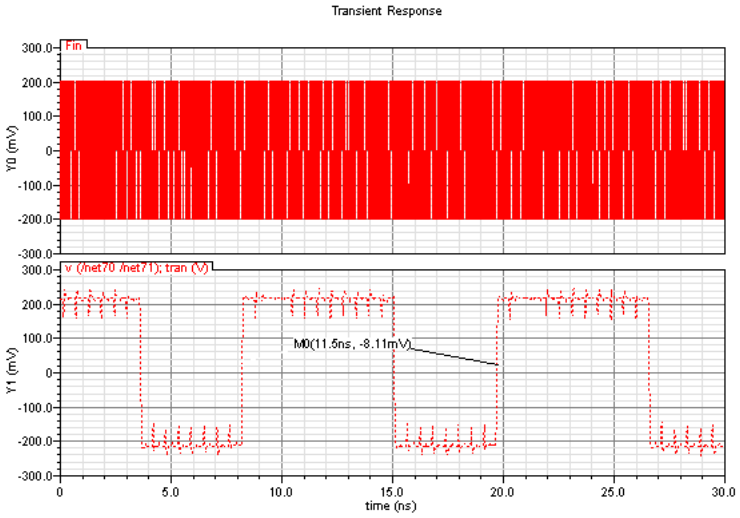

Figure 7.11: MMD Output for the Divide by 159 Case with $f_{in} = 13.84GHz$

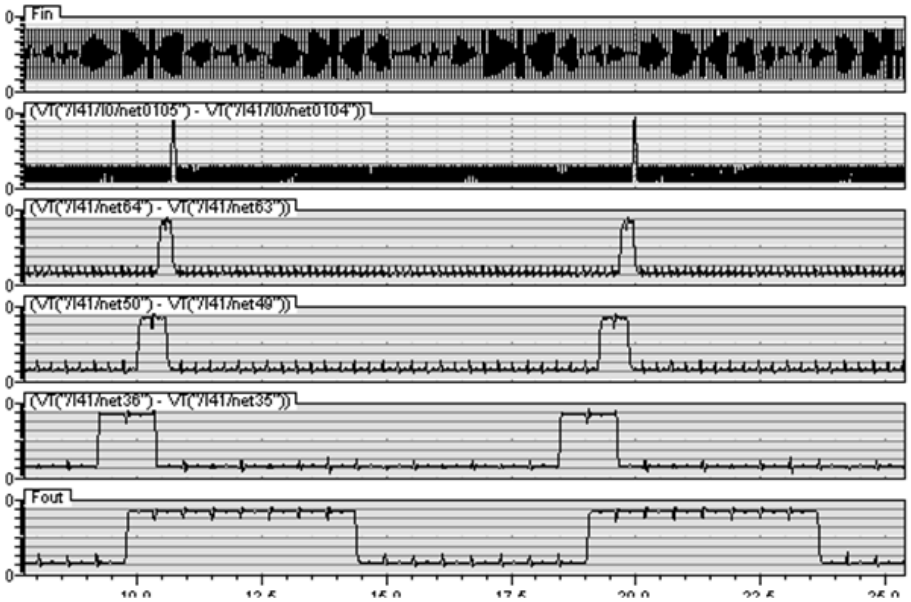

Figure 7.12: MMD Modulus Outputs and 50% Duty Cycle Output for the Divide by 159 Case with $f_{in} = 13.84GHz$

For the MMD implemented in 0.13μm SiGe BiCMOS technology the currents are chosen as shown in Figure 7.13. Because of the drive strength needed we were unable to scale the final three stages under 125μA of current.

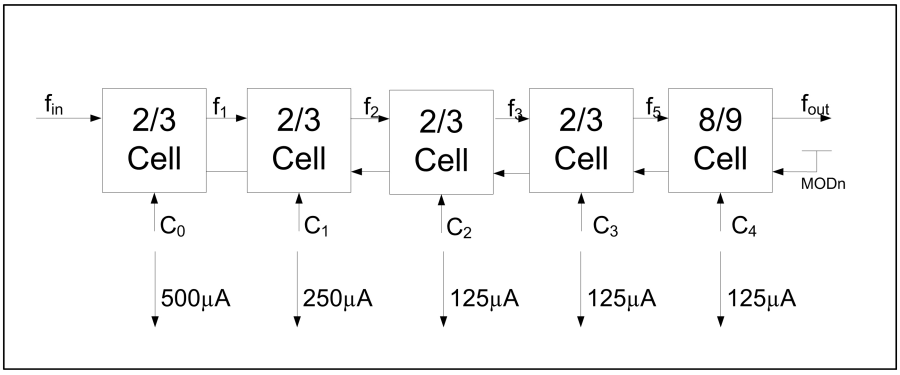

Figure 7.13: Multi−Modulus Divider Designed for Minimum Current

Design	#Stages /Control Bits	# of Latch /Gate	Transistor area (Relative to this work)	Current Consumption (Relative to this work)
This work	5/5	36/15	3219(1)	11mA(1)
[20]	7/7	42/21	4272(1.33)	26.95mA(2.45)
[21]	7/7	56/21	5567(1.73)	30.65mA(2.79)

Table 7.1: Comparison of Previous MMD Architectures

7.6 Conclusion

To avoid the reference frequency and step size problems associated with Integer−N frequency synthesizers, a Fractional−N frequency synthesizer with a MMD is designed.

Power consumption is minimized by designing a MMD with minimum gate count and optimizing the current in each individual cell. The design offers minimum die size and power consumption compared to other designs. Comparison is made between this design and previous MMD architectures in Table 7.1.

Chapter 8

ΣΔ Modulation

8.1 Introduction

ΣΔ modulation has been well developed for analog to digital and digital to analog converters. The noise shaping characteristics of the modulator can be utilized in synthesizer design. The ΣΔ modulator can be used to toggle the control bits of the divider and shape the noise. Thus, the converter appears as a high pass filter for the noise spectrum and a low pass filter for the input signal.

In this chapter we will review basic sampling theory and quantization noise theory. Then the ΣΔ modulator for the PLL frequency synthesizer will be introduced.

8.2 Sampling and Quantization Noise

The Nyquist Theorem states that to reconstruct a sampled signal, the signal must be sampled at greater than two times the highest frequency input signal. If this condition is violated then aliasing occurs and the reconstructed signal will be distorted. The ratio of the sampling frequency f_s to the Nyquist frequency $2f_O$ is defined as the *oversampling ratio* (OSR) and is defined as

$$OSR = \frac{f_s}{2f_O} \tag{8.1}$$

For an N−bit system the quantizer has 2^N levels with equal spacing Δ. The peak−to−peak amplitude is given by

$$v_{max} = (2^N - 1) \cdot \Delta \tag{8.2}$$

If the signal is sinusoidal, the signal power is

$$p = \frac{1}{8}(2^N - 1)^2 \cdot \Delta^2 \tag{8.3}$$

The signal to noise ratio due to quantization noise power that ends up in the signal band is

$$SNR = 10log\left(\frac{\frac{1}{8}(2^N - 1)^2 \cdot \Delta^2}{n_O^2}\right) \approx 10log\left(\frac{3 \cdot 2^{2N} OSR}{2}\right) \tag{8.4}$$

Simplified, the equation becomes

$$SNR \approx 6.02 \cdot N + 3 \cdot log_2(OSR) + 1.76 \tag{8.5}$$

We see that for each addition of a bit, the SNR improves by 6dB. Every doubling of the sampling frequency results in a reduction of in−band quantization noise by 3dB**??**.

8.3 Noise Shaping

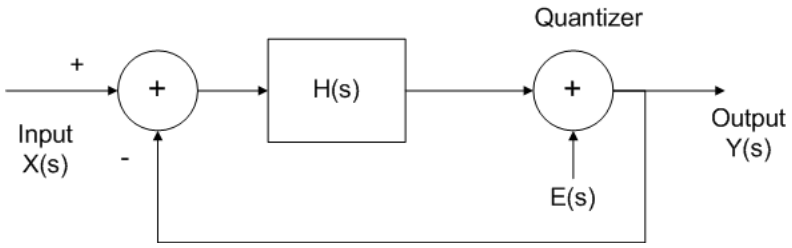

Figure 8.1: Feedback model of noise−shaping system

Another useful trick in reducing the in−band noise is to use a feedback system. If the feedback system is designed as shown in Figure 8.1 from control theory the output is described by

$$Y(s) = \frac{H(s)}{1 + H(s)}X(s) + \frac{1}{1 + H(s)}E(s) \tag{8.6}$$

If we assume that $|H(s)| \gg 1$, which is the case when an integrator is included and only the low frequency components are considered. The output is approximated by $Y(s) \approx X(s)$ and the output noise transfer function (NTF) is approximated by $NTF(s) \approx 0$. So we see that the signal has a low pass transfer function and the noise is passed through a high pass transfer function. Although the total noise is the same, the in−band noise is reduced and the out of band noise can be easily filtered.

8.4 ΣΔ Modulator

8.4.1 First−Order ΣΔ Modulators

The first order ΣΔ modulator is shown as an equivalent circuit in Figure 8.2. The derivation for this modulator is presented in [33]. The noise magnitude is given by

$$n_0 = e_{rms}\frac{\pi}{\sqrt{3}}(2f_0T)^{3/2} = e_{rms}\frac{\pi}{\sqrt{3}}(OSR)^{-3/2} \tag{8.7}$$

So we see that with each doubling of the oversampling ratio reduces the quantization noise by 9dB and increases the number of effective bits by 1.5. This is a significant increase from the system that just uses oversampling!

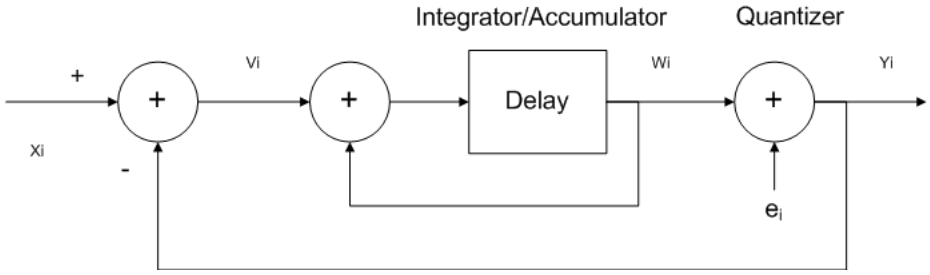

Figure 8.2: $1^{st}Order\Sigma\Delta$ Modulator

8.4.2 Second−Order ΣΔ Modulators

Similarly the second order ΣΔ modulator has the noise magnitude of

$$n_O = e_{rms}\frac{\pi^2}{\sqrt{5}}(OSR)^{-5/2} \tag{8.8}$$

From Equation 8.8 we see that the noise is now lowered by 15 dB when the oversampling ratio is doubled and 2.5 bits of resolution is added.

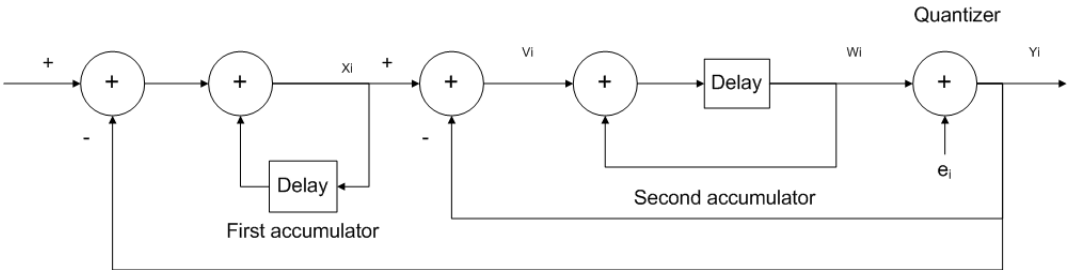

Figure 8.3: $2^{nd}Order\Sigma\Delta$ Modulator

8.5 ΣΔ Modulation for Fractional−N PLL

For the Fractional−N PLL synthesizer, the fractional division ratio is generated by toggling the divider controll bits to generate an average fractional division ratio. This switching division ratios causes phase jitter or spurs near the desired carrier frequency. Utilizing the ΣΔ modulator high pass characteristic for the noise these spurs can be shifted to a higher frequency and removed by the loop filter.

Typically, the modulator implemented in fractional−N synthesizers is a "MASH ΣΔ" Modulator. Since the control bits are digital, the modulator can be designed in a field programmable gate array (FPGA). For a more in−depth look at MASH ΣΔ modulators see reference [33].

8.6 Conclusion

This chapter has given a cursory look at using $\Sigma\Delta$ modulator. $\Sigma\Delta$ modulators offer many advantages in Fractional$-$N synthesizers. In$-$band noise can be reduced substantially. The design of these modulators are generally digital designs that can be implemented off chip in FPGAs and do not necessarily have to be part of the IC design flow.

Chapter 9

Circuit Designs for Low Voltage Applications

9.1 Introduction

The demand for low power drives circuits to lower voltages. Headroom is a critical concern for the circuit designer working with power supplies at 3.3V, 2.2V and lower. The designs in this section are focused on low power versions of blocks that are necessary for the design of the divider.

9.2 Large Signal Behavior of Bipolar Differential Pairs

Before the circuit designs are introduced, the function of the differential pairs should be discussed. The differential pairs are easily interfaced with other circuits including the analog parts. It is important for the pairs to be fully switched. A large enough differential voltage must be applied to the inputs for the the transistors to fully switch. For the bipolar differential pair the tail current is:

$$I_{EE} = i_{C1} + i_{C2} \tag{9.1}$$

and the differential input voltage is:

$$v_1 = v_{BE1} - v_{BE2} \tag{9.2}$$

Using these equations and the relationships:

$$i_C = I_S e^{\frac{v_{BE}}{v_T}} \tag{9.3}$$

and

$$v_{BE} = v_T \ln \frac{i_C}{I_S} \tag{9.4}$$

after some manipulation the resulting equations are:

$$i_{C1} = I_{EE} \left(\frac{e^{\frac{v_1}{v_T}}}{1 + e^{\frac{v_1}{v_T}}} \right) \tag{9.5}$$

$$i_{C2} = I_{EE} \left(\frac{e^{\frac{-v_1}{v_T}}}{1 + e^{\frac{-v_1}{v_T}}} \right) \tag{9.6}$$

This result indicates that the bipolar differential pair is completely switched when v_1 is approximately $4 \times v_T$ (Approximately 100mV) or larger, regardless of the size of the transistor or the current. All circuits in this design are designed to have a swing of 200mVpp, thus ensuring that the transistors are fully switched.

9.3 CML D−Latch

Several versions of the CML D−Latch are commonly used in practice. For 3.3V applications and lower a three level D−latch in Figure 9.1 with reset can be used. This latch has active low reset, D input and a clock input. Variations of this circuit are used in the fabricated design. The latch can be implemented without the reset signal and the latch will only have one current tail, or as in the case of the PFD, the D input is always tied to Vcc.

The D−Latch in Figure 9.2 is the essential building block of the divider designed by the author and presented in [32]. The design excludes the reset signal as it is not necessary in this application. Note that this latch only needs one current tail. For optimal performance the higher speed signal is fed to the lower set of transistors Q5 and Q6. The current tail transistor M1 and the resistors R1 and R2 are designed to provide a swing of 200mV.

9.4 CML AND Gate

The CML AND gate for low voltage applications is shown in Figure 9.3.

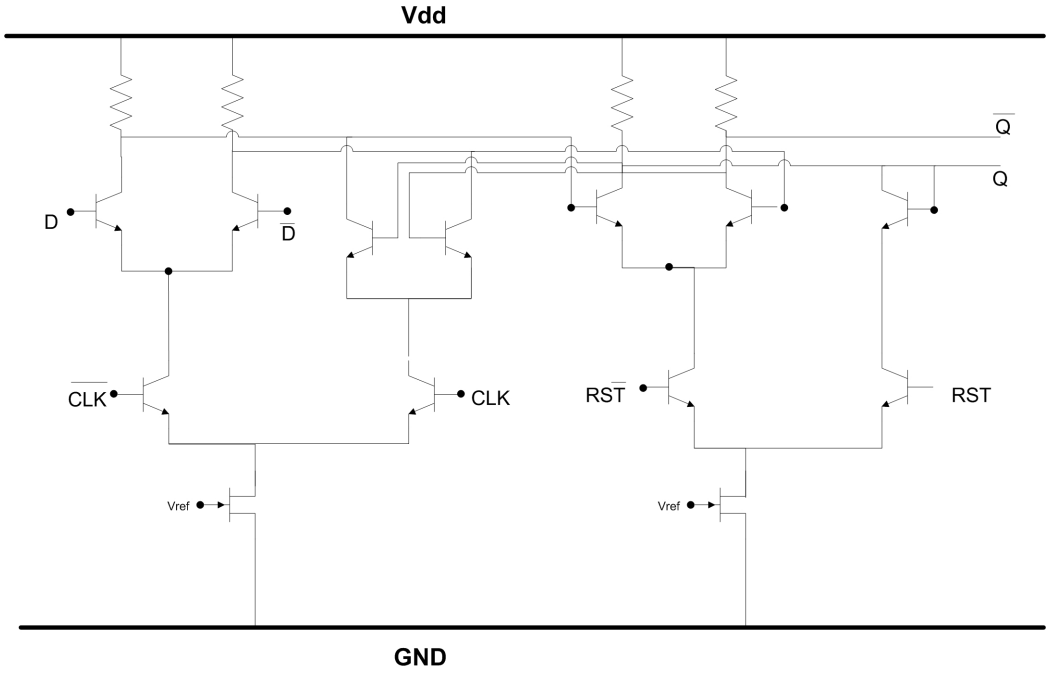

Figure 9.1: CML D−Latch for Low Voltage Applications

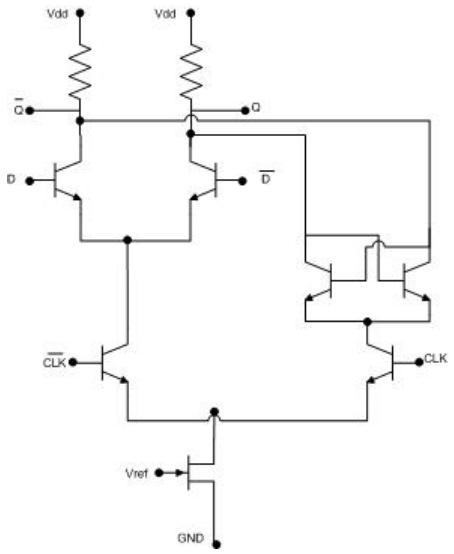

Figure 9.2: CML D−Latch with a Single Current Tail

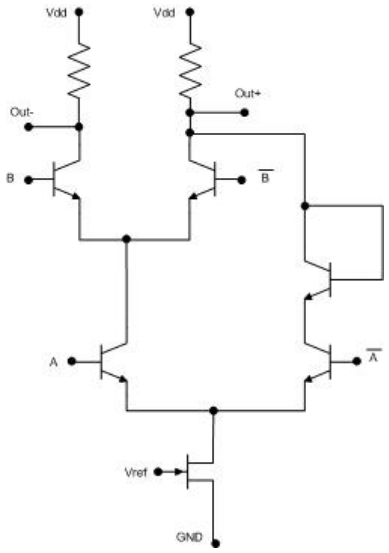

Figure 9.3: CML AND Gate

9.5 Buffer

The CML buffer is a simple circuit to analyze after the previous circuits. It is simply a differential pair with resistors and current tail designed for the specified swing. A schematic view of the buffer is in Figure 9.4. In our case the swing is 200mV. If the buffer is to service the top level transistors then a transistor is added between the pair and the current tail with base tied to collector. This transistor operates in soft saturation as a diode providing proper biasing. Likewise, if the buffer should service the bottom level transistors, the diode drop should be above the resistors and tied to Vcc.

9.6 Level Shifter

The level shifter is the simplest of circuits to be implemented. The input comes in on the base of a set of transistors with the collectors tied to Vcc (no resistors) and the output taken on the emitter as shown in Figure 9.5. Also strung to the emitter is another transistor with the base tied ot collector to act as a diode drop. Lastly, a current tail is needed for each input.

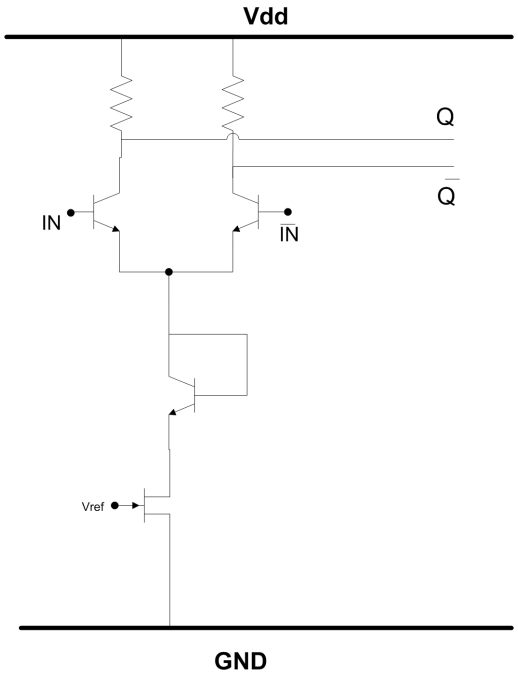

Figure 9.4: CML Buffer

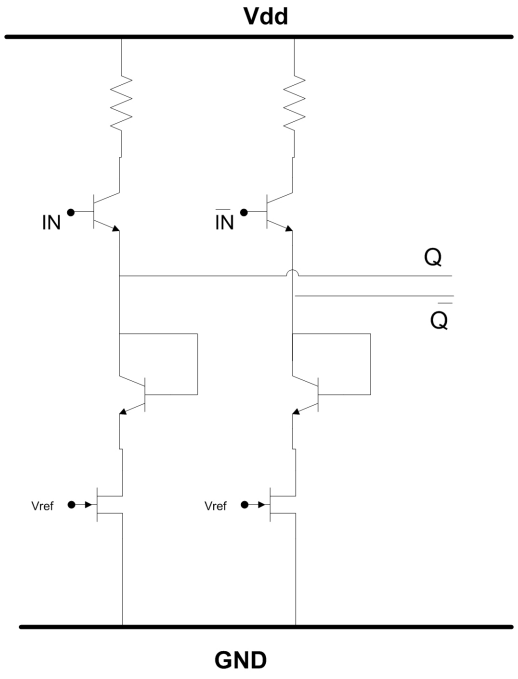

Figure 9.5: CML Level Shifter

9.7 Conclusion

The circuits shown in this chapter are useful for the implementation of the reference buffer, divider and phase detector specifically. Each is designed to have a swing of 200mV for a specified current.

Chapter 10

Fabricated Design

10.1 Introduction

The 13GHz PLL MMIC is implemented in 0.13μm SiGe BiCMOS technology. The chip micrograph in Figure 10.1 shows the PLL MMIC. The total die area is $2.4x1mm^2$. The PLL operates at a maximum of 13GHz with a supply voltage of 2.2V. The total power consumption of the PLL RFIC with supporting circuitry is 95mA.All measurements were done using CLLC packaged prototypes.

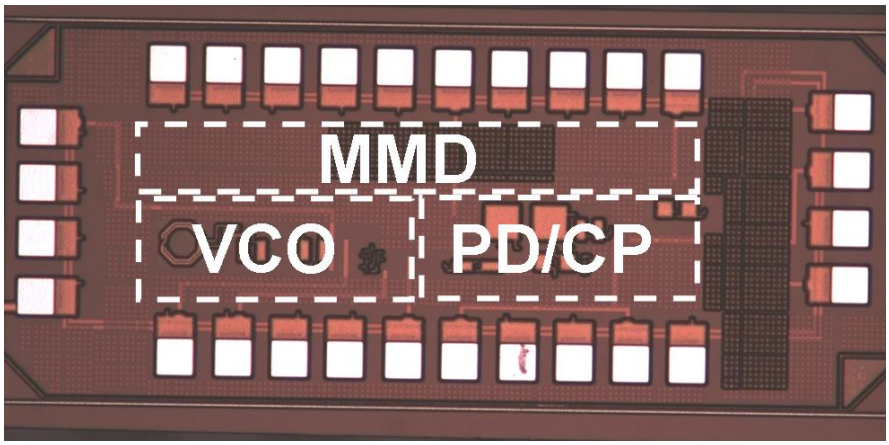

Figure 10.1: PLL RFIC implemented in 0.13μ technology

10.2 Test Setup

The printed circuit board developed for testing is shown in 10.2. The VCO and MMD outputs are differential. The VCO outputs are fed through a differential balun and viewed with a spectrum analyzer. The MMD outputs are at a low enough frequency to be fed

to the channels of an oscilliscope and processed internally. The complete test setup with spectrum analyzer, oscilliscope, test board, and power supplies is shown in Figure 10.3.

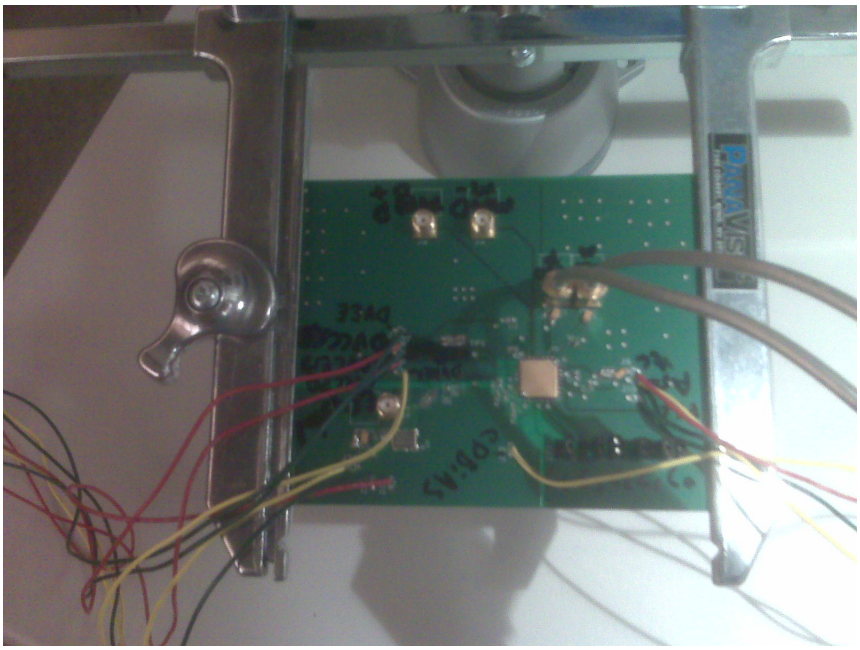

Figure 10.2: Printed circuit board developed for PLL testing

10.3 Multi−Modulus Divider

The MMD circuit occupies .88 x .10 mm^2 die area. Operating at maximum 13GHz input frequency with a single 2.2 V power supply, the total power consumption of the MMD RFIC is 24.2 mW. Figure 10.4 gives the measured MMD output waveform at 7 MHz.

10.4 Voltage Controlled Oscillator

The VCO has a measured K_{VCO} of approximately 867MHz/V which is in agreement with the simulated result in Figure 10.5.

Phase noise for the *loop* is measured at −102dBc/Hz at an offset of 1MHz from the carrier.

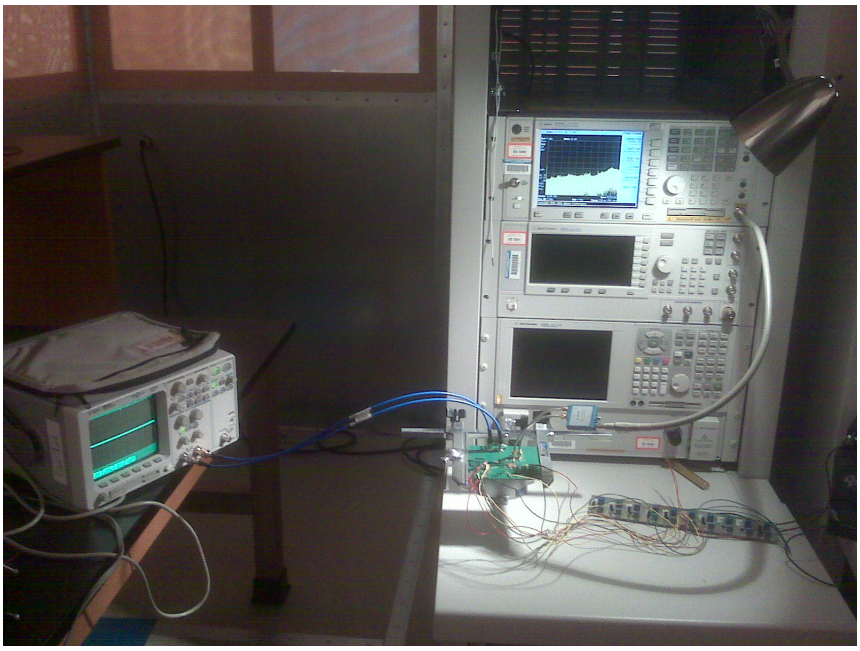

Figure 10.3: Test Setup for PLL Testing

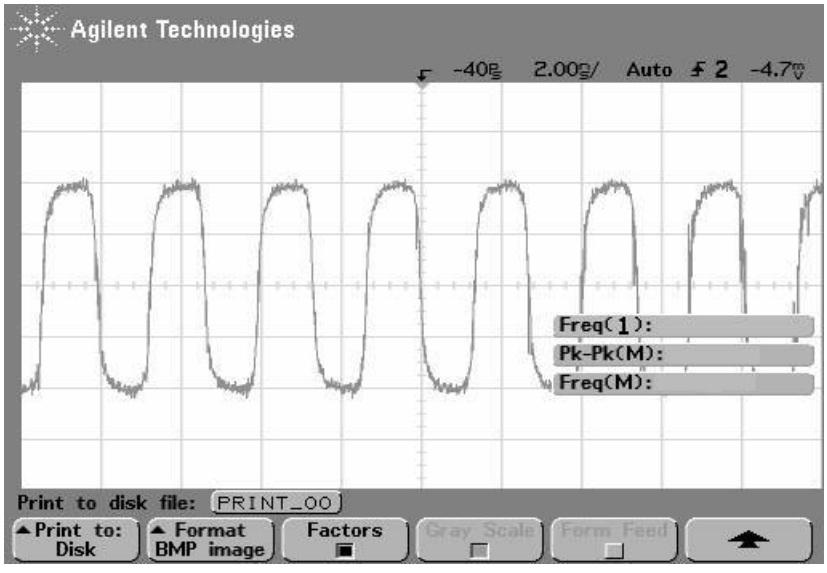

Figure 10.4: MMD output of 86MHz with input frequency of 11GHz

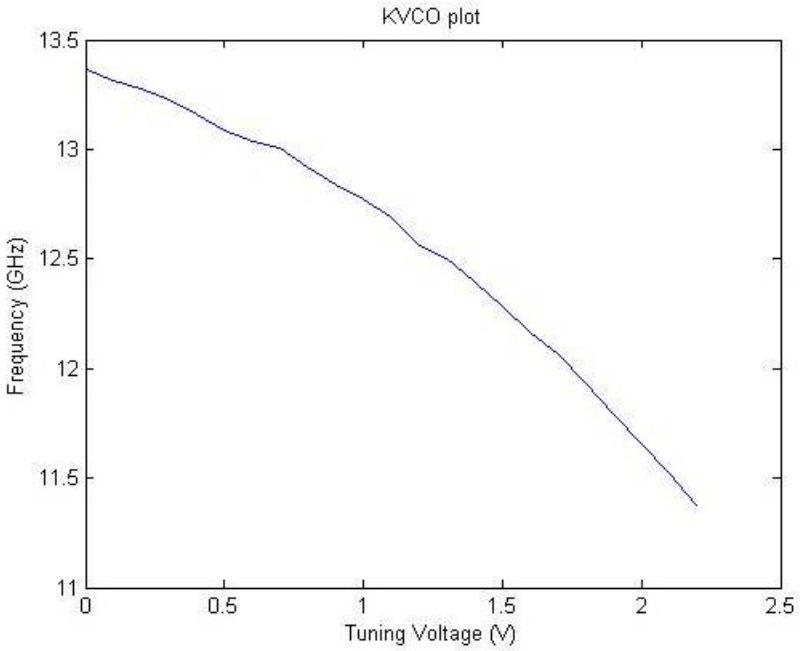

Figure 10.5: Simulated K_{VCO}

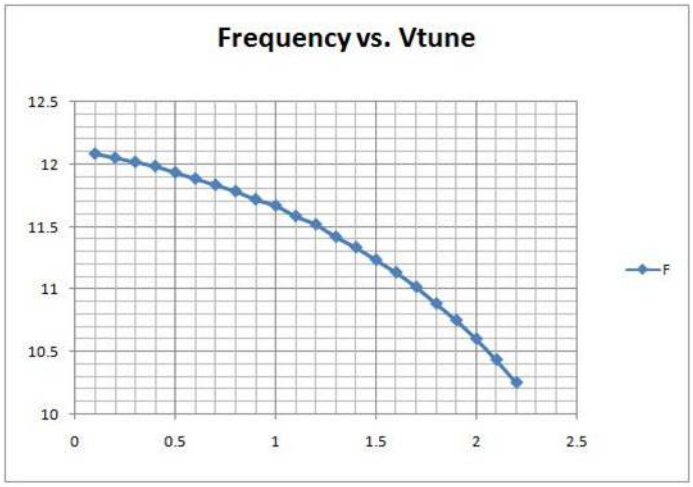

Figure 10.6: Measured K_{VCO}

Total Area	$2.4\times1mm^2$
−MMD Area	$0.88\times0.1mm^2$
−VCO Area	$0.476\times0.119mm^2$
−PFD Area	$0.213\times0.09mm^2$
−Charge Pump Area	$0.125\times0.073mm^2$
Total Power	95mA
−MMD core	11mA
−VCO core	8mA
−PFD core	7mA
−Charge Pump	3mA
VCO Tuning Range	10.25 - 12.075 GHz
Phase Noise @1MHz	-102 dBc/Hz
MMD Division Ratio	128-159

Table 10.1: Performance Summary

10.5 Conclusion

The performance of the packaged RFIC has been summarized in Table 10.1. The PLL has minimal area, low power, and moderate phase noise under a low voltage supply. All testing has been performed with packaged prototypes.

Chapter 11

Conclusions

A frequency synthesizer has been designed that addresses the need for flexibility to be able to operate in multiple frequency bands. This requirement is accomplished through the design of a fractional−N synthesizer with a Multi−Modulus Divider. The PLL Frequency synthesizer design can synthesize channels in Ku and X bands. The design minimizes noise through methodical analysis of noise sources and careful design of circuits. The analysis of a $\Sigma\Delta$ modulator shows that if $\Sigma\Delta$ modulation techniques are employed the noise can be reduced substantially in the band of interest.

The fabricated design has low power consumption, low noise, and can synthesize all required frequencies in the Ku and X bands.

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Appendices

Appendix A

Matlab M−Files

A.1 PLL Frequency Response

```
y = .1
z = tf([y, 1], [1,y,1]);
[mag,phase,w] = bode(z);mag1 = mag(1,:);semilogx(w,20*log10(mag1),'k');
xlabel(['\omega','/','\omega_n']);ylabel(['\theta_o','/','\theta_R', '(dB)']);
hold on
y = .5
z = tf([y, 1], [1,y,1]);
[mag,phase,w] = bode(z);mag1 = mag(1,:);semilogx(w,20*log10(mag1),'k:');
xlabel(['\omega','/','\omega_n']);ylabel(['\theta_o','/','\theta_R', '(dB)']);
hold on
y = .707
z = tf([y, 1], [1,y,1]);
[mag,phase,w] = bode(z);mag1 = mag(1,:);semilogx(w,20*log10(mag1),'k--');
xlabel(['\omega','/','\omega_n']);ylabel(['\theta_o','/','\theta_R', '(dB)']);
hold on
y = 1.5
z = tf([y, 1], [1,y,1]);
[mag,phase,w] = bode(z);mag1 = mag(1,:);semilogx(w,20*log10(mag1),'k.');
xlabel(['\omega','/','\omega_n']);ylabel(['\theta_o','/','\theta_R', '(dB)']);
hold on
y = 2.2
```

```
z = tf([y, 1], [1,y,1]);
[mag,phase,w] = bode(z);mag1 = mag(1,:);semilogx(w,20*log10(mag1),'ko');
xlabel(['\omega','/','\omega_n']);ylabel(['\theta_o','/','\theta_R', '(dB)']);
hold on
y = 2.9
z = tf([y, 1], [1,y,1]);
[mag,phase,w] = bode(z);mag1 = mag(1,:);semilogx(w,20*log10(mag1),'k:');
xlabel(['\omega','/','\omega_n']);ylabel(['\theta_o','/','\theta_R', '(dB)']);
hold on
y = 4.3
z = tf([y, 1], [1,y,1]);
[mag,phase,w] = bode(z);mag1 = mag(1,:);semilogx(w,20*log10(mag1),'kx');
xlabel(['\omega','/','\omega_n']);ylabel(['\theta_o','/','\theta_R', '(dB)']);
hold on
y = 5

legend(['\zeta = ',num2str(.1)],['\zeta = ',num2str(.5)],...
['\zeta = ',num2str(.707)],['\zeta = ',num2str(1.5)]...
    ,['\zeta = ',num2str(2.2)],['\zeta = ',num2str(2.9)]...
    ,['\zeta = ',num2str(4.3)])
```

A.2 PLL Step Response

```
zeta = [0.3,0.5,0.707, 1, 2, 5];
delomega = 1;
natfreq = 1;
t = 1:.1:8;

theta = (delomega/natfreq)*(sinh(natfreq*sqrt(zeta(1)^2-1)*t)...
```

```
/sqrt(zeta(1)^2-1)).*exp(-zeta(1)*natfreq.*t);
plot(t,theta,'k');hold on
theta = (delomega/natfreq)*(sinh(natfreq*sqrt(zeta(2)^2-1)*t)...
/sqrt(zeta(2)^2-1)).*exp(-zeta(2)*natfreq.*t);
plot(t,theta,'k--');hold on
theta = (delomega/natfreq)*(sinh(natfreq*sqrt(zeta(3)^2-1)*t)...
/sqrt(zeta(3)^2-1)).*exp(-zeta(3)*natfreq.*t);
plot(t,theta,'k.');hold on
theta = (delomega/natfreq)*(sinh(natfreq*sqrt(zeta(4)^2-1)*t)...
/sqrt(zeta(4)^2-1)).*exp(-zeta(4)*natfreq.*t);
plot(t,theta,'k:');hold on
theta = (delomega/natfreq)*(sinh(natfreq*sqrt(zeta(5)^2-1)*t)...
/sqrt(zeta(5)^2-1)).*exp(-zeta(5)*natfreq.*t);
plot(t,theta,'kx');hold on
theta = (delomega/natfreq)*(sinh(natfreq*sqrt(zeta(6)^2-1)*t)...
/sqrt(zeta(6)^2-1)).*exp(-zeta(6)*natfreq.*t);
plot(t,theta,'ko');hold on;grid on;
xlabel('\omega_nt');ylabel(['\theta_e(t) / (\Delta\omega/\omega_n)'])
legend(['\zeta = ',num2str(.3)],['\zeta = ',num2str(.5)],...
['\zeta = ',num2str(.707)],['\zeta = ',num2str(1.0)]...
    ,['\zeta = ',num2str(2.0)],['\zeta = ',num2str(5.0)])
```

A.3 Root Locus Analysis

```
dampingConst = 0.707;
naturalFrequency = 2*pi*55000;
T = 1/40e6;%period of reference
Ts = 1/(2*40e6);Sampling time
alpha = (4*dampingConst - naturalFrequency*T)/...
```

```
(4*dampingConst + naturalFrequency*T);%open loop zero
K = naturalFrequency^2*T^2*(1+4*dampingConst/(naturalFrequency*T))...
/2;%Open loop Gain
z = tf('z',Ts);  H = K*(z-alpha)/((z-1)^2);%Transfer function
rlocus(H);axis equal;
```