A TUNABLE COPLANAR PATCH ANTENNA, A POLYMER MEMS BASED TUNABLE BANDPASS FILTER, AND A CHIP-IN-POLYMER PACKAGING TECHNOLOGY

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A TUNABLE COPLANAR PATCH ANTENNA, A POLYMER MEMS BASED TUNABLE BANDPASS FILTER, AND A CHIP-IN-POLYMER PACKAGING TECHNOLOGY

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Brian Russell Holland was born to Earl Houston and Susan (Kinch) Holland on the 22nd of March, 1982 in Loma Linda, CA. He graduated from Rosemont Christian School in Dothan, AL in May of 2000. After attending Troy State University at Dothan for one academic year he entered Auburn University in August of 2001. He graduated magna cum laude in May of 2005 with a Bachelor of Wireless Engineering degree. In that very month he entered graduate school to pursue a Master of Science degree in Electrical Engineering with research in MEMS Antennas and Technology while working as a Teaching Assistant as well as a Research Assistant.

THESIS ABSTRACT

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Brian Russell Holland

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This thesis presents a tunable coplanar patch antenna, a Polymer MEMS-based tunable bandpass filter, and a chip-in-polymer packaging technology. First, a Coplanar Waveguide (CPW) based patch antenna is integrated with a prepackaged diode. This diode functions as a variable capacitor (Varactor), which is used to adjust the effective length of the open-end resonator in the Coplanar Patch Antenna (CPA). An increase in the effective length decreases the resonant frequency of the CPA and vice versa. Thus, the resonant frequency of the antenna is tuned by changing the capacitance of the varactor through an applied bias voltage.

Second, two Polymer MEMS varactors are integrated with an embedded bandpass filter to yield a tunable filter. In this project, each MEMS varactor is an electro-static parallel plate actuator. The capacitance of the parallel plate actuator is varied by controlling the DC voltage applied between the plates. Two MEMS varactors are

integrated with the two cascaded LC tank circuits to adjust the resonant frequency of each tank circuit independently and/or simultaneously to realize a tunable bandpass filter. The capacitance is varied by a DC bias voltage that is placed between the plate itself and the center and ground conductors of a CPW segment over which the plate hangs. When this voltage reaches the "pull-down voltage" of the parallel plate actuator, the plate will snap down to contact the dielectric and the capacitance will increase thereby effectively lowering the resonant frequency of the tank circuit as well as the filter's overall corner frequency. The filter assembly consists of two main layers that are bonded together via a thermal compression bonding film. The lower substrate of the filter assembly consists of a lumped-element filter fabricated using embedded passives technology in Liquid Crystal Polymer (LCP) and the upper part of the filter assembly consists of MEMS varactors. The substrate was fabricated at the Georgia Institute of Technology and the MEMS layer was fabricated in the Alabama Microelectronics Science and Technology Center.

Lastly, a "chip-in-polymer" packaging technology is presented that is being developed for the National Aeronautics and Space Administration's (NASA) Jet Propulsion Laboratories (JPL). This approach is intended to yield two silicon die thinned down to be embedded in a flexible polymer film. In this process, a handle wafer has adhesion promoter spun on around the periphery of the wafer before a layer of PI2611 is spun on. After the initial layer is cured, several other layers, including the thinned die, are spun on and deposited using various methods. Once the device is complete, the handle wafer and the attached devices are diced, however the adhesion in the bulk of the center of the handle wafer between the wafer and the device is such that the device detaches from the handle wafer as desired. Experimental results are presented.

ACKOWLEDGEMENTS

The author would like to thank Dr. Ramadoss for his unending patience and understanding in walking through this process as well as Dr. Stuart Wentworth for his Teaching Assistantships that kept the author housed and well-fed. Also, this project would not have been possible were it not for Ananth Sundaram in the development of the MEMS Varactor used for his prior project. Thanks also go to Amit Bavisi and everyone else at Georgia Tech who contributed to the design and fabrication of the PCB portion of the filter. In addition, thanks go to all family members, friends, roommates, officemates and professors who contributed with their love and support.

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TABLE OF CONTENTS

LIST OF FIGURES

CHAPTER 1: INTRODUCTION

In recent years, much emphasis in the development of new technology has been placed not only on increased functionality, but also on miniaturization. The mobile phone industry's massive demand for cheaper, smaller and better performance RF-components has ignited research activities related to Radio Frequency Micro-Electromechanical Systems (RF-MEMS) in many places worldwide [1]. With an increasing interest in the RF MEMS area, and with such a high demand for smaller devices, it would be attractive to redesign conventional tunable RF components (such as antennas and filters) using MEMS technology for not only better performance, but also for smaller size.

Micro-Electromechanical Systems (MEMS) offer a reliable, easy to manufacture, low-loss, low-cost replacement option for many classically large components. If, using MEMS technology, bulky capacitors, relays, switches, or other typically large components can be replaced, the overall size of electrical circuits such as filters and phase shifters can be significantly reduced.

In this thesis, Printed Circuit Board (PCB) process compatible Polymer MEMS varactors are monolithically integrated with a band pass filter fabricated using conventional PCB technology. If a traditionally packaged diode were to be incorporated into a PCB application, it must be packaged separately and integrated into the circuit by conventional packaging techniques such as wire bonding and/or soldering. Such a packaging requirement can increase the overall size of a circuit very quickly, as well as add time, complexity, and cost to manufacturing. If instead a PCB compatible MEMS varactor were to be incorporated into that same type of application, there would be a dramatic decrease in size with no loss in functionality. Instead of adding the entire thickness of the diode's separate packaging which might be on the order of 1-3 mm, only one thickness of a MEMS device would be added which is typically less than 200 microns.

In the first project, an ordinary varactor diode was integrated with a Coplanar Patch Antenna for implementation of a tunable antenna suitable for multi-band wireless communication systems. This antenna was previously designed, manufactured, and tested at Auburn University. This experiment was conducted as a precursor to a project that would fabricate an antenna specifically designed for the MEMS varactor as well as the MEMS devices associated with it. However, the portion of the project pertaining to this thesis was merely to test and demonstrate tunability using an ordinary varactor diode. Since this particular antenna has already been characterized in absence of the varactor, after integration of the varactor, it can be shown that the varactor's presence adds to the functionality of the device without disrupting it.

In the second project, a MEMS tunable filter was demonstrated by integrating two Polymer MEMS varactors with a bandpass filter. The filter was designed by Bavisi et al. [2] at the Georgia Institute of Technology. The filter was adapted to accommodate a MEMS varactor design and later fabricated on site at GA Tech. The filter design with the MEMS varactor integrated is such that the lower half of the entire device can function as a filter with or without the MEMS device attached. The MEMS layer was fabricated by the author in the Alabama Microelectronics Science and Technology Center.

Finally, the author is involved in the development of a Chip-in-Polymer packaging technology with potential applications for miniaturization. Auburn University is currently developing a thinned, flexible die technology that could be adapted for Jet Propulsion Laboratories' (JPL) space-based radar systems and other novel utilizations of such technologies. JPL supplied 10 die for use in production once a final process was developed and approved for embedding the JPL die. A wafer of repeated instances of a test pattern called PB6 was acquired to obtain thinned die with which to test processes. The final goal being to hone a process in which die were thinned and embedded into a polymer substrate called polyimide. These thinned die were to be embedded not only in such a way that they would be totally sealed inside the substrate, and so they could be accessed from the outside environment, but that they would also be interconnected together via intermediate layers within the substrate itself.

In conclusion, three separate projects from three different sections of the Research and Development process promoted the author's understanding of design, simulation, fabrication, and testing through his time at Auburn. These three projects while completely independent were similar in content and conduction.

CHAPTER 2: ANTENNA WITH VARACTOR DIODE

2.1 Introduction

Coplanar Patch Antennas (CPAs) are based on the concept of open-ended Coplanar Waveguide (CPW) resonators [3]. CPAs, due to their single-plane configuration, easily accommodate integration of shunt and series mounting of active and passive components. CPAs offer several advantages such as wider bandwidth and lower cross-polarization radiation, as compared to microstrip patch antennas [4], [5]. In this example, a CPA is fed by a Coplanar Waveguide (CPW) at the radiating edge as pictured in Figure 1.

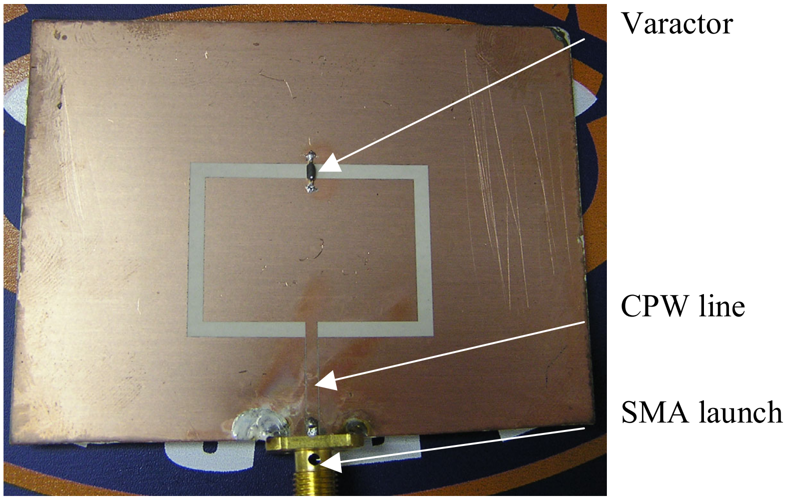

Figure 1 Photograph of the CPA with a varactor diode.

In a CPA, the resonant frequency of the antenna is determined mainly by the effective length of the antenna along the non-radiating edge. The frequency of operation of the antenna can be changed by changing the effective length of the antenna via using a variable capacitor load at the radiating edge. Here, a diode-based variable capacitor is used as a shunt terminating element on the CPA yielding an adjustable effective length. It is located at the radiating edge opposite the feed point, as pictured in Figure 1.

A varactor diode, if forward biased, functions as a normal diode. However, if it is reverse biased, inside the diode there forms a depletion region between the p-type silicon and the n-type silicon, forming a capacitance across the p/n junction. If the reverse biasing voltage is increased, the width of the depletion region between the two types of silicon increases. The behavior of the diode can be utilized as a variable capacitor in a circuit. If the reverse biasing voltage is increased, the depletion region increases, thereby decreasing the capacitance. This variable capacitance, if implemented correctly, can be used to vary the effective length of an open-ended transmission line segment. The varactor diode MA46H200 (available from MACOM) was chosen for this particular application because of its specific range of capacitance values, its voltage range, and its packaging available suitable for installation on a CPA. This varactor's capacitance ranges between 1.4 pF and 0.15 pF corresponding to reverse bias voltages of 0.5 V and 20 V, respectively.

2.2 Design and Simulation

A transmission line model for the antenna with the varactor at the end is shown below in Figure 2. The resonating frequency will depend heavily on the effective length of the antenna. This effective length will be comprised of the electrical length of the physical portion of the antenna, plus the effective electrical length added by the varactor's capacitance. By varying the capacitance of the varactor to change the effective electrical length of the varactor, the effective electrical length of the entire antenna can be tuned.

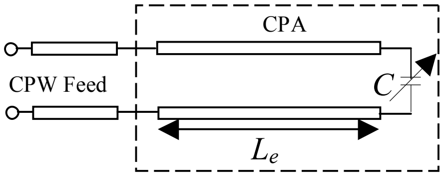

Figure 2 Transmission Line model of CPA

Typical performance parameters of interest for an antenna include return loss (i.e., the reflection coefficient looking into the feed of the antenna) and the radiation patterns in both the E-plane and H-plane. Figure 3 shows the simulated and measured return losses of the antenna before mounting the varactor.

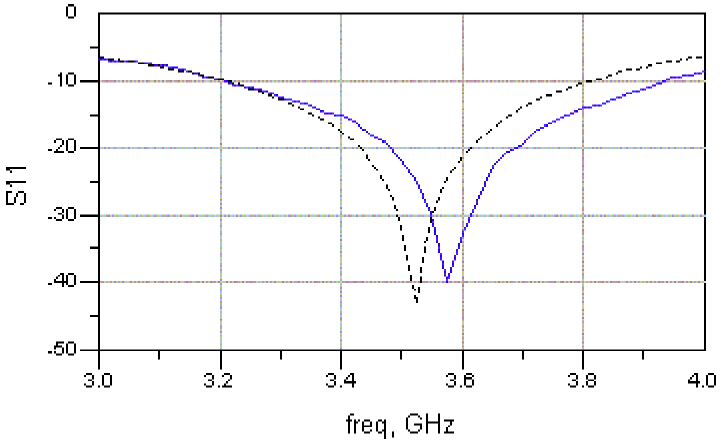

Figure 3 Simulated (dashed) and measured (solid) S_{11} of CPA with varactor

2.3 Experimental Results

This specific antenna in this specific configuration can be tuned from 4.92 GHz at 0 V to 5.40 GHz at 19.5 V with a return loss of greater than 14 dB. Moreover, the antenna provides a return loss better than 32 dB in the tunable frequency range of 5.16 to

5.40 GHz [6]. The measured return loss of the antenna after mounting the varactor diode is shown in Figure 4for various bias voltages.

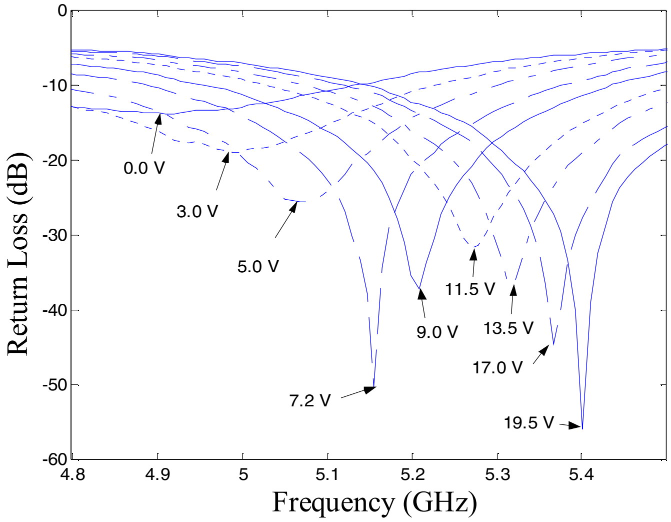

Figure 4 Measured return loss results of the coplanar patch antenna for various bias voltages applied to the varactor diode.

It should be noted that in order to apply a DC bias to the diode, a “bias tee” must be used to protect the Vector Network Analyzer (VNA) from high DC voltages as well as prevent interference between the instrument and the power supply. A bias tee is a simple two-element circuit designed to allow the DC biasing of RF circuits without interfering with the RF portion of the circuit as illustrated in Figure 5.

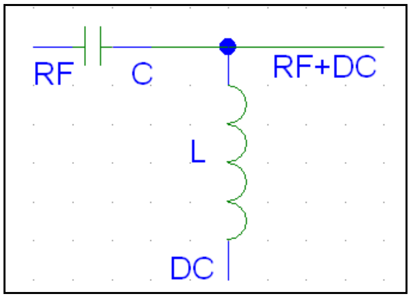

Figure 5 Schematic diagram of a Bias Tee

The VNA used for the measurement, the Agilent 8510C, was calibrated by connecting the standard 2.4mm open-short-load standards at the reference plane between the bias tee and the antenna.

It should be pointed out that the radiation pattern of the CPA was not measured before mounting the diode, so comparison of radiation patterns before and after mounting the diode is not discussed. It should also be noted that since an attempt at adding a tuning functionality to the antenna is being made, the radiation pattern must be measured throughout the entire proposed range of tuning to ensure that it is acceptable over the tuning range. Measured E-plane (E_θ in yz-plane) and H-plane (E_ϕ in xz-plane) radiation patterns of the coplanar patch antenna for various bias voltages are shown in Figure 6.

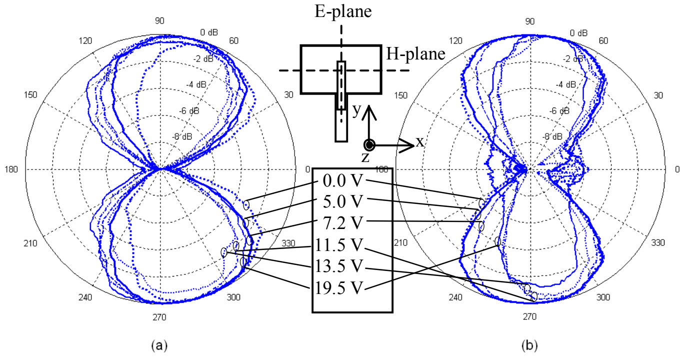

Figure 6 Measured radiation patterns of the coplanar patch antenna for various bias voltages applied to the varactor diode a) E-plane (E_θ in *yz*-plane), and b) H-plane (E_ϕ in x*z*-plane).

As observed in Figure 6 it is clear that the tuning of the CPA via the varactor diode has no detrimental effects on the radiation pattern. The only noticeable effect is the slight leaning of the E-plane radiation pattern towards one direction. Due to the capacitive loading effect introduced by the varactor at the top radiating edge, the phase of the fields radiated from the top radiating edge lag behind that of the fields radiated from the bottom radiating edge. As a result, the E-plane patterns are slightly tilted towards the top radiating edge.

2.4 Conclusion

A varactor tuned coplanar patch antenna capable of operation in the frequency range of 4.92 GHz to 5.4 GHz was presented. These types of tunable antennas will find potential applications in next generation multi-standard wireless communication systems.

Another application of this tunability is using one single tunable antenna when normally either an RF adjustment would have to be made to accommodate a low bandwidth antenna, or possibly even multiple antennas would have to be used. The main purpose of this project specifically was to attempt to determine if a MEMS varactor could be used to do the same function as demonstrated here. The monolithic integration of a MEMS varactor with a CPA has been recently demonstrated by Maddella et al. [7].

CHAPTER 3: TUNABLE BANDPASS FILTER

A bandpass filter can be formed by cascading two parallel LC tank circuits with series coupling with capacitors. The bandpass filter can be made tunable by using variable capacitors in the LC tank circuits. A schematic circuit diagram of the tunable bandpass filter architecture described above is shown in Figure 7.

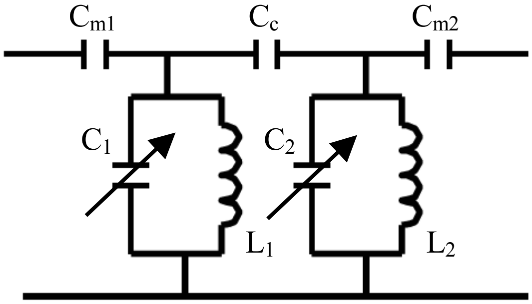

Figure 7 Schematic of a two pole tunable bandpass filter

3.1 Introduction

This configuration is a second order capacitively-coupled Chebyshev filter [8]. Bavisi et al. at Georgia Tech designed, fabricated, and tested one such filter including the coupling capacitors, the inductors and all interconnections (excluding the varactors) using a Liquid Crystal Polymer (LCP) based embedded passives (EPs) printed circuit fabrication technology [2]. The thickness of the entire fabricated device excluding varactors was 0.7 mm and the traditionally packaged varactors were also 0.7 mm, doubling the thickness of the total assembled device. Such increases in size are quite typical in the assembly of large-level design implementations and often prevent more compact end-user packaging as well. In addition since there is an overall shift in the electronics market to a tendency to try to bring all aspects of a system onto one single chip using System on Chip (SoC) architectures, or to instead merge entire systems into one package using System on Package (SoP) architectures, it would be worthwhile to investigate the feasibility of implementing MEMS varactors on this filter.

3.2 Tunable Filter Using Varactors

The tunable filter designed by Bavisi et al. in [2] was mainly designed to demonstrate the capabilities of a new LCP based EPs fabrication procedure to achieve more metallization layers per unit of thickness. Figure 8 shows an X-ray photograph of the fabricated filter including the varactor diodes and biasing and ground wires.

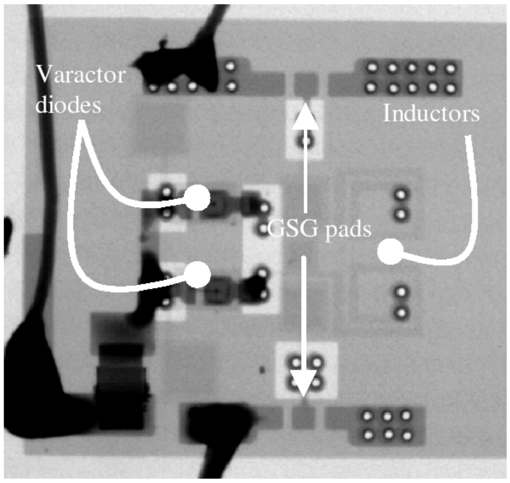

Figure 8 X-ray photograph of final fabricated and assembled filter by Bavisi et al. [2]

Figure 9 compares the measured results (square marker) of the fixed frequency version (i.e., instead of varactors, fixed embedded capacitors were used) of the filter with the results obtained from Sonnet software (solid line). The measured result of a similar filter (‘x’ marker) with the exception that the capacitors C1 (1.1 pF) and C2 (1.1 pF) are replaced with silicon varactor diodes from Skyworks Inc. (model SMV 1405).

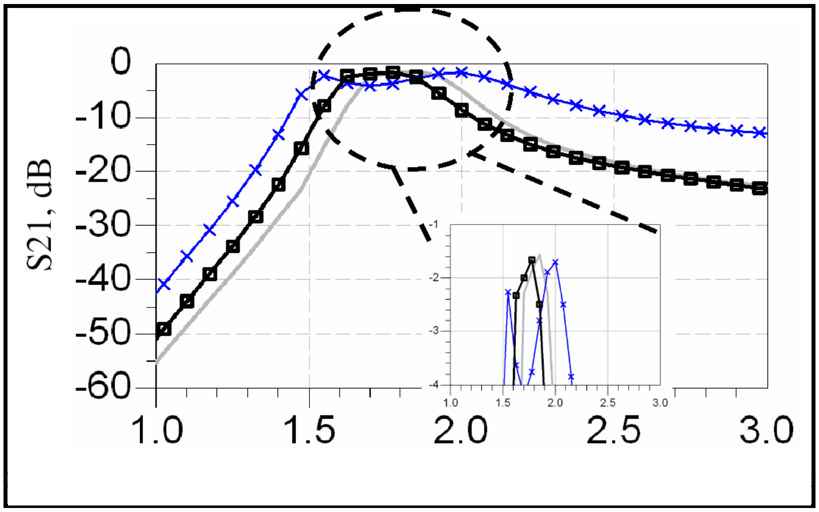

Figure 9 Comparison of filter responses: both tunable and fixed frequency. Insertion loss is also shown in the inset [2]

Each abrupt-junction type diode can provide a capacitance of 2.7 pF to 0.6 pF over a reverse junction voltage of 0 V to 30 V. The data of the tunable filter in Figure 9 is at a tuning voltage of 6 V where the varactors give 1.05 pF of capacitance and hence, comparable to the results of the fixed frequency filter [2].

3.3 Tunable Filter Using MEMS Varactors

In collaboration with Bavisi et al at Georgia Tech, polymer MEMS varactors were integrated with the filter discussed earlier. The original substrate (shown in Figure 8) was therefore redesigned to accommodate MEMS varactors designed by our group [9], [10]. In this design, a Parallel Plate Actuator type MEMS varactor is suspended above the center conductor of a CPW line as shown in Figure 10. This forms an effective RF capacitance ($C_M = 2C_1C_2/(C_1+2C_2)$) between the ground planes and center conductor and the MEMS Varactor plate that can be varied by changing the DC bias voltage between the MEMS Varactor plate and the CPW metallization (i.e., the ground plane and center conductor). In order to incorporate this CPW based MEMS varactor design, the configuration of the original filter was modified to include very short 50Ω CPW line sections. The signal transmits through the center conductor of the section of the CPW line to the ground plane as displacement current through the capacitances C_1 and C_2. There is an intrinsic capacitance that is formed between the center conductor and the ground plane. This capacitance is accounted into the 50Ω characteristic impedance of the transmission line segment. When the MEMS Varactors are integrated, an additional effective RF capacitance (C_M) between the center conductor and ground planes is formed. The capacitance C_M due to the MEMS Varactor can be adjusted by electrostatically controlling the height of the MEMS Varactor plate above the CPW. This additional variable capacitance C_M has been utilized to change the resonant frequency of each LC tank circuit in the filter.

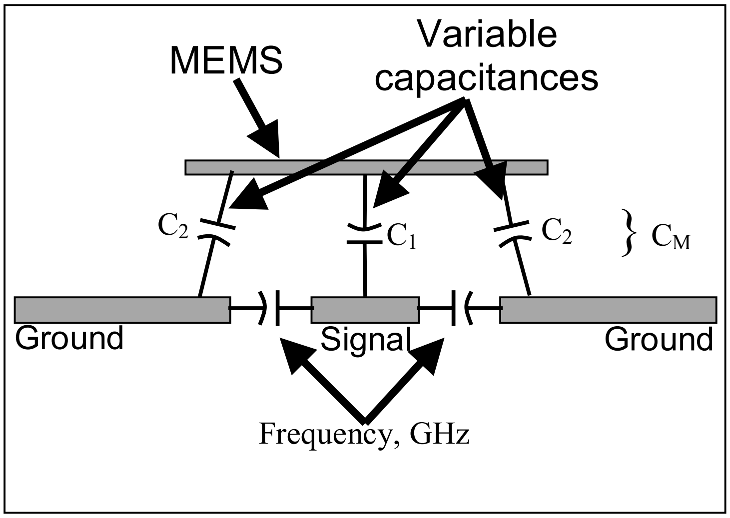

Figure 10 Illustration of capacitances present between the MEMS Varactor plate and CPW

However, the mere presence of an increased capacitance will not yield tunability, nor will it be practical, or even successful, to test the value of this capacitance to determine if the MEMS layer is functioning. In order to check functionality of the implementation of the MEMS varactors the shift in the signal, not just the shape and location, must be observed in correlation to the changing height of the MEMS plate. The effects of the attempts at utilizing MEMS on this device will be observed in a later section.

3.4 MEMS Varactor Operation

As stated earlier, the MEMS varactor utilized in this project is a standard parallel plate type electrostatic actuator. Such an actuator is designed around the balancing of an electro-static force against a spring tension created by that force. As displayed in Figure 11, where z_o is the initial height of the plate at rest, z is the current height of the plate, k is the spring constant of the plate's suspension structure, and the electrostatic force is generated by a bias voltage *V*.

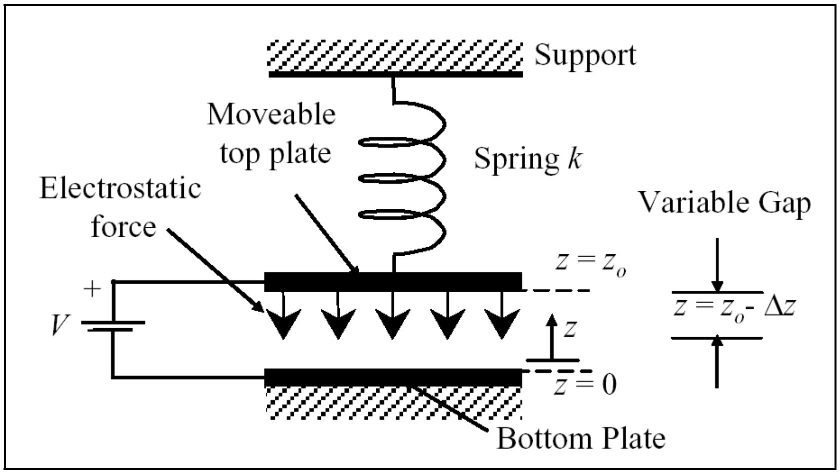

Figure 11 Lumped element model of Parallel Plate Actuator [11]

If a non-zero voltage is applied it will generate a downward electrostatic force between the top and bottom plate and is balanced by a resisting upward mechanical force by the spring. These mechanical and electrostatic forces are given by Equations (1) and (2) respectively [11].

$$F_M = k(z_o - z) \tag{1}$$

$$F_E = -\frac{1}{2}\frac{\varepsilon_o A V^2}{z^2} \tag{2}$$

Equating these two forces and solving for V yields Equation (3).

$$V = z\sqrt{\frac{2k(z_o - z)}{\varepsilon_o A}} \tag{3}$$

However, a quadratic equation yielding two answers such as the one above typically has one stable answer and another unstable answer. If the displacement as a function of voltage is plotted, the instability point can be visually observed. Figure 12 below shows the plate's displacement as a function of applied bias voltage. The upper region of the graph corresponds to the "stable region" and conversely the lower half corresponds to the "unstable region". Simply put, driving the bias voltage higher than the pull-down voltage

(V_p) will result in the system reaching a point at which the mechanical force can no longer balance the system and an effect called "Pull-down" occurs, after which the top plate collapses onto the bottom plate.

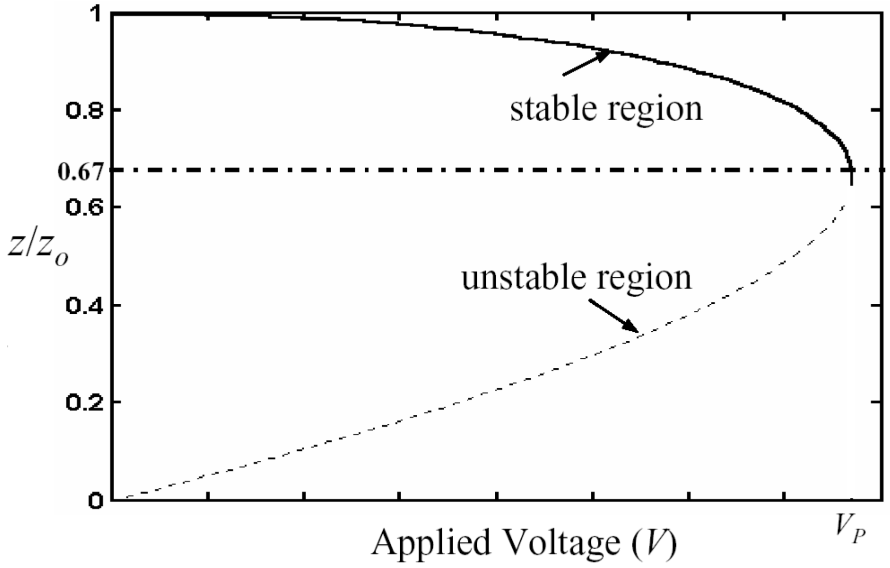

Figure 12 Normalized displacement of MEMS plate versus applied bias voltage [11]

The voltage at which this occurs is appropriately called the "Pull-Down Voltage". Solving Equation (3) for where $\partial V/\partial z = 0$ we obtain the displacement at which pull-down occurs: $z = \frac{2}{3} z_o$ (as indicated by dashed horizontal line). Substituting this back into Equation (3) we can determine the pull-down voltage.

$$V = \sqrt{\frac{2kz_o^3}{27\varepsilon_o A}} \tag{4}$$

In the event of pull-down, there would normally be catastrophic failure unless there was something to insulate the top plate from the bottom plate, or some physical stopper to keep them from coming in contact. If there were a dielectric layer that was thinner than $z = \frac{2}{3} z_o$, the plate would press up against this layer after pull-down occurs, preventing a bias voltage short. Another benefit of having a dielectric layer is having a set value of capacitance for the down state of the MEMS Varactor. Instead of a linear voltage input and output relation, the varactor would essentially be discretely controllable between the two values of capacitance. The two values would be the value when the plate is at rest and the value when the plate is pressed against the dielectric. However, care must be taken when selecting the material for, and thickness of, the dielectric layer. If the dielectric layer's thickness is designed to be less than that of the material's dielectric breakdown voltage, failure will likely occur even with the layer in place. Other issues that might introduce a breakdown are pinholes and other in consistencies in the dielectric layer and voltage spikes.

Although the varactor can switch between these two values of capacitance readily, it is not just a simple matter of increasing or decreasing a voltage above or below any one given level. Once pull-down occurs, if the voltage were dropped back down below the pull-down voltage there would be virtually no change in the plate's displacement. This is due to the proximity of the MEMS plate to the ground plane making the voltage required to maintain a down state much lower than the original pull-down voltage. In other words, in addition to a "Pull-down voltage" there is also the concept of a "Release Voltage," i.e. the voltage at which the plate is released from the down state and allowed to return to the stable region. This influence of the system's history on how it behaves in the present is called "hysteresis" and a graph of the hysteresis of a similar MEMS device from [10] is shown in Figure 13.

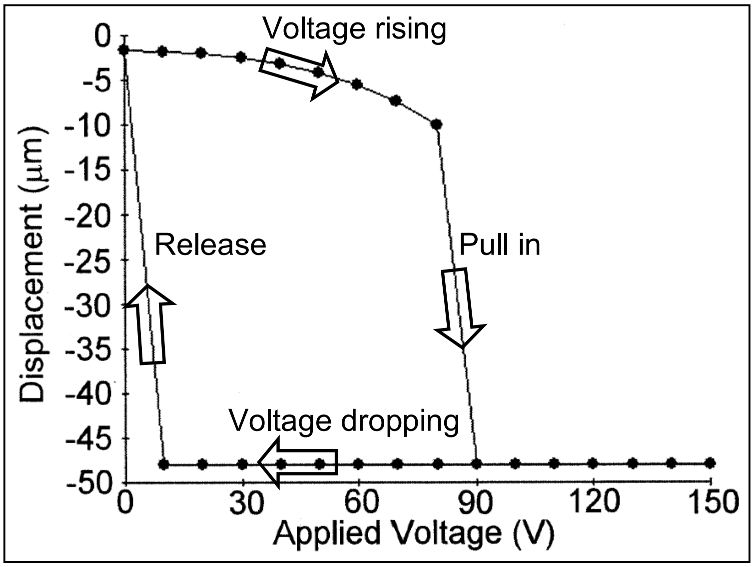

Figure 13 A sample gap-height versus applied voltage hysteresis cycle for the parallel plate electrostatic actuator [10]

3.5 Integration of MEMS Varactors with the Filter

The final step in implementing tuning on this varactor-based design, was deducing how specifically to integrate the MEMS varactor design. Essentially, the MEMS varactor only needs a small section of CPW line on the top layer of LCP in order to function. The majority of this design will still suffice as it is, merely the top layer needs to have the CPW sections inserted and rearranged, and any subsequent adaptations made in the underlying layers. Ensuring a good, uniform, and complete ground plane is also essential in getting a good passage of the signal through the CPW line. This is accomplished by several vias along the CPW ground that penetrate the entire design through to the ground plane on the back of the filter. The overall footprint of the newly designed circuit covers a slightly larger area, but once the MEMS varactors are in place the device will still be less than 1 mm thick (excluding biasing inductors).

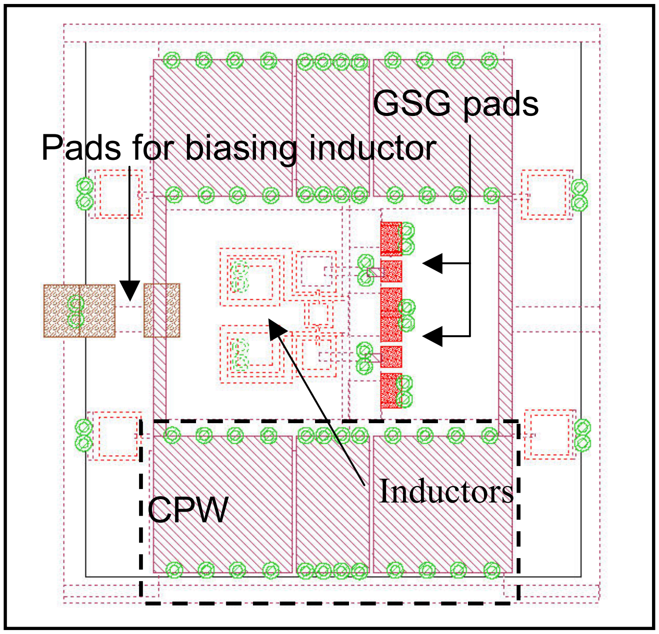

Figure 14 Final design layout of the MEMS varactor based filter

One slightly more difficult problem to overcome, however, is the fact that the MEMS plate suspended over this center section of CPW can cause interference with the rest of the circuit. The signal could quite easily be picked up by the plate and be transmitted through to some other part of the circuit. So it is advisable to maintain necessary spacing between the MEMS Varactors and neighboring circuits. The biasing line that runs along each of the suspension springs attached to the plate must exhibit a large enough resistance to attenuate any RF signal that might bleed through from the MEMS Varactor plate to the DC power supply. If this line were to short out and provide a low-impedance link back through the DC power supply to the rest of the circuit, there would be a significant degradation in the overall circuit performance. On the other hand, if this line were to break or crack somehow, then the MEMS Varactor plate would not only be physically floating, but it would be electrically floating as well, leaving the

MEMS varactor non-functional for tuning purposes. The bias line is an important aspect in getting a functional MEMS Varactor.

The equivalent circuit model for the final MEMS based filter is shown in Figure 15. L_1, L_2, C_4 and C_5 represent the LC tank circuit components. C_1, C_2, and C_3 represent the series coupling capacitors. The bias inductor (L_3) connects C_4 and C_5 to the RF ground of the filter. Resistors R1 and R2 are bias resistances present between the MEMS Varactor plate and the anchors.

Notice that bias line resistances R1 and R2 are not physically connected to the tank circuits, but are merely floating attachments to the MEMS Varactor plates that are in proximity to the CPW lines. Note also the location of the biasing inductor L_3. The biasing of the MEMS Varactors is accomplished by connecting a DC power supply between the bias inductor (L_3) and bias resistances (R1 and R2).

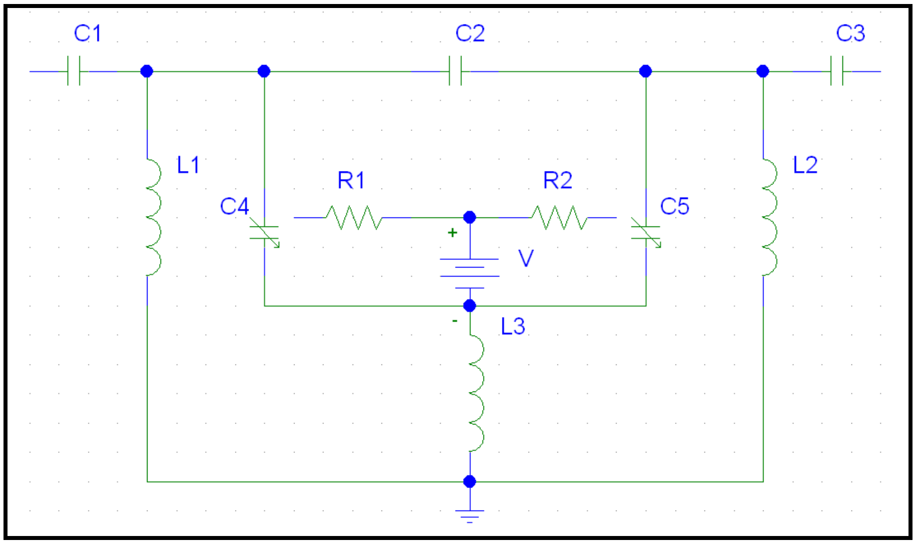

Figure 15 Schematic lumped element model of filter including MEMS elements

The final design and layering of the MEMS parallel plate Varactor is illustrated in Figure 16 and the top view of the MEMS Varactor is shown in Figure 17.

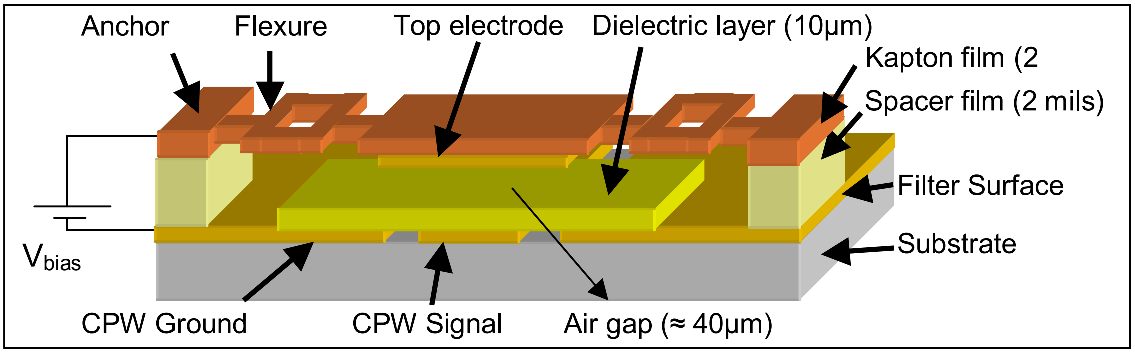

Figure 16 Layered schematic of the MEMS varactor

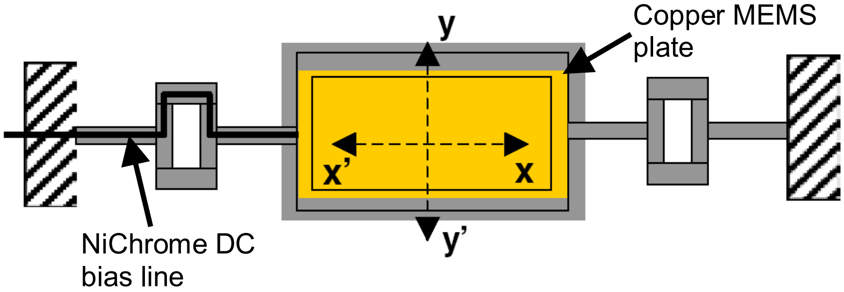

Figure 17 Top view of the MEMS Varactor

3.6 Fabrication

As stated earlier, the lower LCP portion of the filter was fabricated at Georgia Tech; however, the upper MEMS portion was fabricated in the Alabama Microelectronics Science and Technology Center (AMSTC). Detailed fabrication procedures are attached in Appendix A. In this section various processing steps are briefly discussed.

Beginning from the lower portion of the filter acquired from Georgia Tech, the substrate, a layer of photosensitive BenzoCycloButene (BCB) was spin-coated onto the substrate and patterned to form the dielectric layer. This layer was then cured for several hours in a vacuum oven. Figure 18 shows a photograph of the filter substrate with the BCB dielectric layer fully cured on the surface. The thickness of the layer is determined mainly be spin speed, but if the liquid BCB is diluted with solvent, ultra-thin layers can be obtained. However, the uniformity of the layer can be detrimentally affected if care is not taken to ensure a homogeneous mixture at the time of spin-coating.

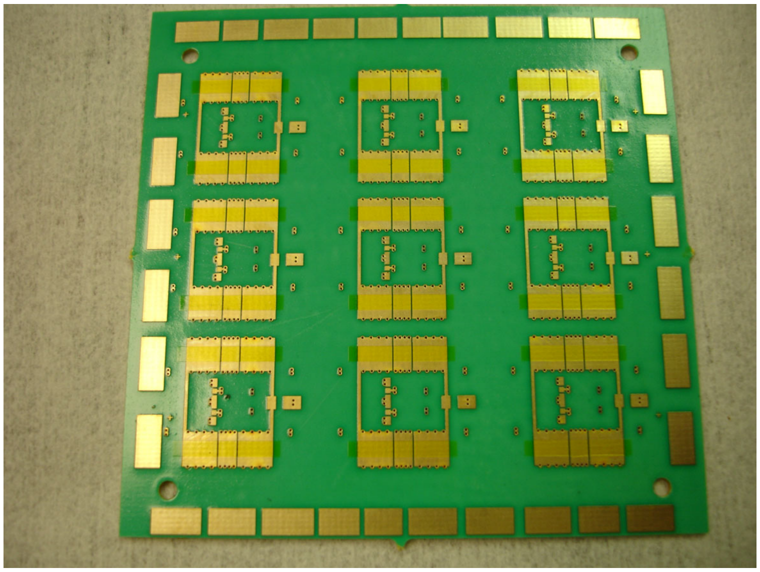

Figure 18 Photograph of the filter substrate with the BCB dielectric layer fully cured on the surface

The spacer layer provides the required spacing between the substrate and the polyimide layer. Hence, the thickness of the spacer film determines the up-position gap height z_o. A 2 mils thick polyflon bonding film is used as the spacer film. This film is machined using a milling machine to create openings for the contact pads and the MEMS varactor in the polyimide film. A photograph of the final machined spacer layer is shown in Figure 19.

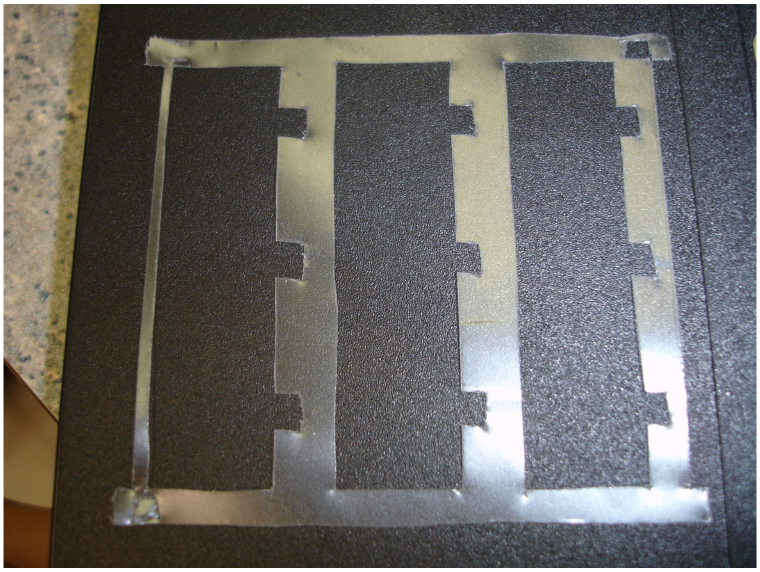

Figure 19 Photograph of the final machined spacer layer

A 2 mils thick flexible Kapton E polyimide film ($\varepsilon_r = 3.1$) with 100–150 Å NiChrome seed layer and 3 µm thick copper cladding is used. The Kapton polyimide film layer is used as the MEMS structural layer because of its ability to withstand millions of mechanical flexing cycles. First, the electrode is defined on the 3 µm thick copper cladding on the Kapton film by photolithography and etching processes. Then, the film is machined using deep reactive ion etching (DRIE) to create slot openings required for the formation of a movable membrane. These flexures separate the membrane from its adjacent area and thus reduce the stiffness of the movable membrane. The equipment used for the DRIE process is an STS AOE (Advanced Oxide Etcher). The configuration of the gases used for this etch in our facility is 8 sccm CF4 and 35 sccm Oxygen with 500 W of RF power. These processing parameters take about 70 min to etch a 2 mils thick Kapton layer. Finally, the resistive bias lines are defined in the NiChrome seed layer by removing the copper cladding to expose the underlying NiChrome. A photograph of the final fabricated Kapton layer is shown in Figure 20.

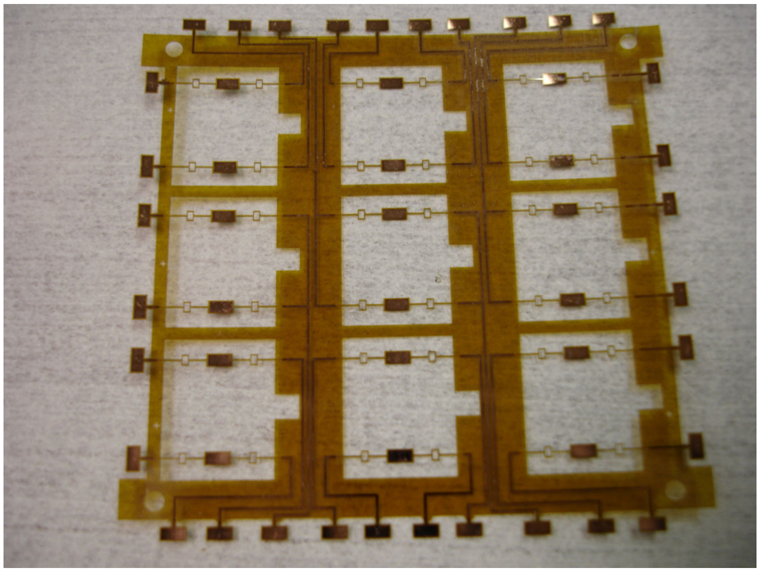

Figure 20 Photograph of the final fabricated Kapton layer of the MEMS Varactor

Thermo-compression bonding is performed using a Carver press consisting of two platens. The platens are heated using heaters, which are controlled by a thermocouple. The fixture consists of two steel plates with alignment holes at four corners. The substrate forms the bottom most layer, the spacer is the middle layer, and the Kapton film forms the topmost layer in this structure. The different layers are aligned by aligning the marks created on the three layers during the fabrication process described earlier. This unit is now placed between the press platens. The bonding is performed at a pressure of 65 psi (a load of 165 lbs) and a temperature of 130° C. Both pressure and temperature are maintained for 5 min during bonding. Before pressure is released, the assembly is cooled down to room temperature. A photograph of the final assembled MEMS based filter prototype, including biasing inductors, as well as grounding and biasing wires is shown in Figure 21.

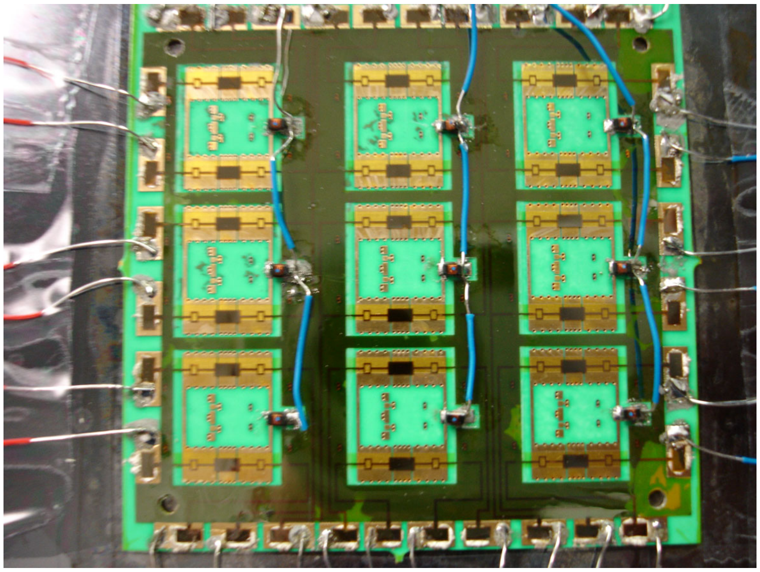

Figure 21 Photograph of the 2” X 2” assembled prototype with 9 MEMS based filters

Due to the small size of the filter design, it was possible to accommodate 9 copies of the final design on a 2” X 2” substrate. Pictured below in Figure 22 is a single copy of the filter, along with some labels of the individual filters parts.

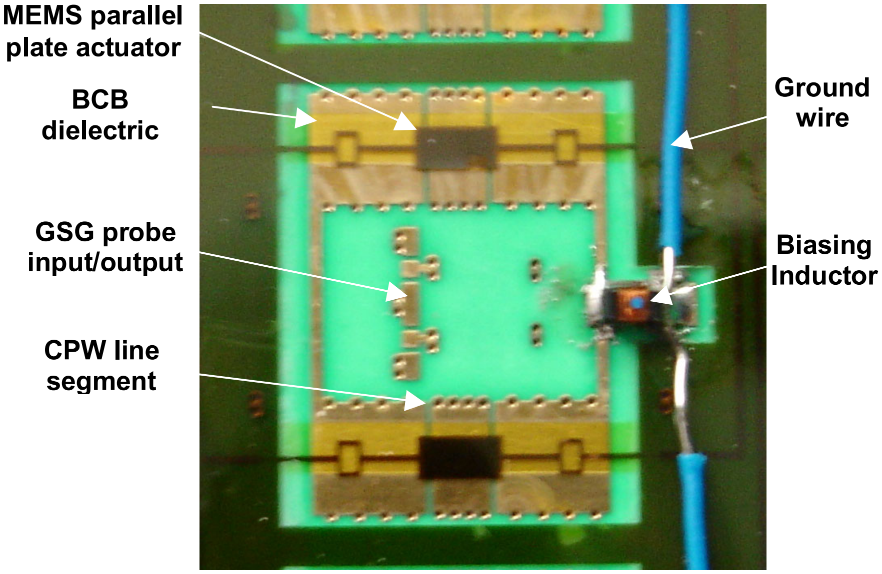

Figure 22 Photograph of individual filter with labels

3.7 Experimental Results

The RF testing of the final assembled filter was performed on the HP 8510C network analyzer in the High Frequency Testing lab at Auburn University. The original filter design, as well as the redesigned filter with the MEMS devices, was setup to measure the input and output signal on Ground-Signal-Ground Coplanar probes. In this situation since the bias voltage is to be applied between two locations on the substrate (namely, the bias inductor and the NiChrome bias line), a bias tee is not necessary. The DC voltage terminal is connected to the bias pad connecting through the bias line resistance to the MEMS Varactor plate and the DC ground is connected to the MEMS inductor as illustrated in Figure 23.

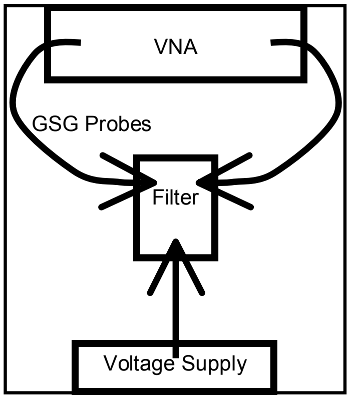

Figure 23 Block diagram of measurement setup

The measurements were taken with DC bias voltages applied ranging from 0-250V, increasing the voltage with each measurement by 5 or 10 volts. Figure 24 shows plots of the measured insertion loss (S_{21}) for the filter at various biasing voltages, and Figure 25 shows a more detailed plot of the peak of Figure 24. The measured center frequency of the MEMS filters is 1.714 GHz and 1.650GHz for 0V and 250V, respectively. These results demonstrate the feasibility of monolithic integration of polymer MEMS Varactors with lumped element filters and embedded passives using PCB processing techniques.

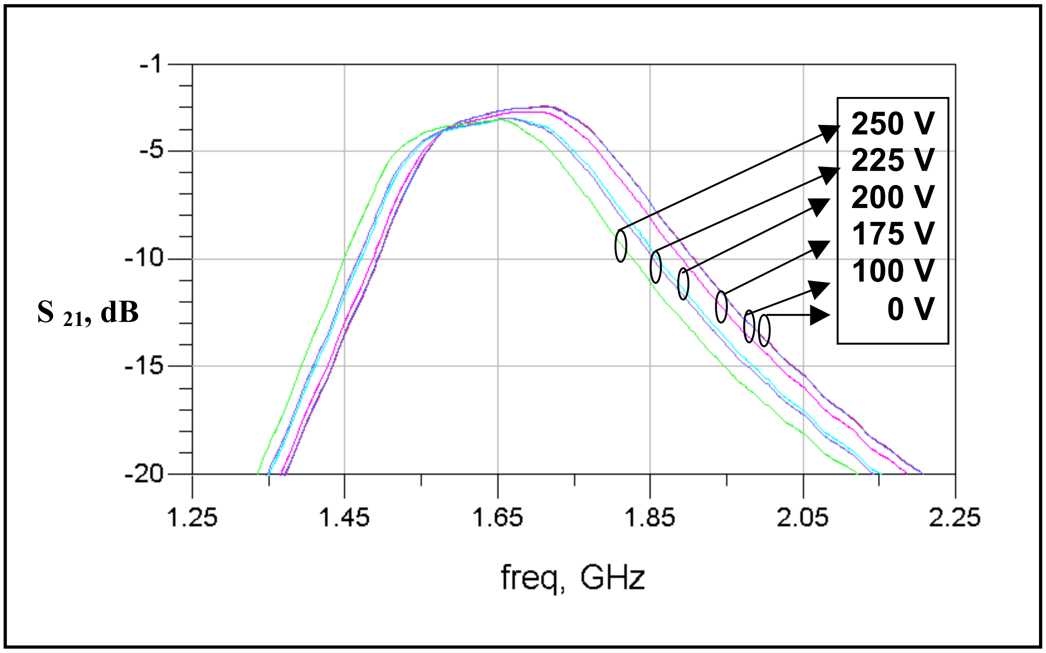

Figure 24 Insertion Loss of the MEMS filter for various applied bias voltages

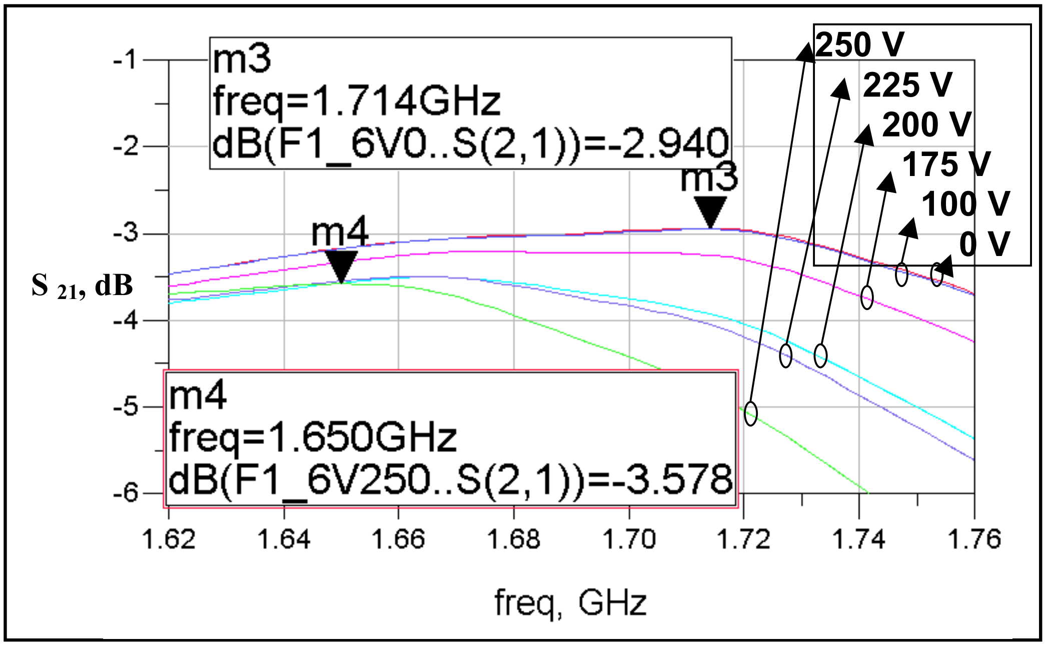

Figure 25 Detailed Insertion Loss results for the same filter as **Figure 24**

3.8 Problems and Future Work

In the current design, the bias inductor appears in series with MEMS Varactors in the LC tank circuit. This could be attributing to the high insertion loss. The filter performance can be improved by modifying the biasing arrangement. Also, biasing voltage can be reduced by decreasing the initial gap height between the MEMS Varactor plate and the CPW and/or by reducing the spring constant of the suspension flexures of the MEMS Varactors.

The bulk of the problems that occurred were with reference to the bias line resistance. Some times the NiChrome would be removed completely. Other times the Copper cladding would not be etched quite enough. Still other times the NiChrome would crack or erode beyond DC conductance. Getting a MEMS layer with Copper electrodes and all the right shapes is relatively easy compared to getting bias lines with the right amount of resistance. This difficulty was the biggest of the obstacles in achieving a functioning device. Experimenting to determine where in the fabrication process this step most consistently worked only revealed that the NiChrome seed layer is extremely fragile. It was found that the NiChrome layer cracks during the DRIE process step due to the thermal expansion mismatch between Kapton and NiChrome. Short DRIE etching steps (roughly 5 minutes each) followed by a cooling step (roughly 10 minutes) seems to alleviate this cracking problem.

The processing step that etched the Kapton film is called Deep Reactive Ion Etching (DRIE). In order to use this type of step in a process, more often than not, a mask that is more resilient than typical photoresist has to be used. For this process, Aluminum was chosen for its ease of deposition, and many other reasons. Once the Aluminum is deposited, the shape of the MEMS layer is etched into the Aluminum to protect the Kapton in the same shape. During DRIE, the Aluminum protects the Kapton from the plasma that etches it. Once the etching is completed, the Aluminum is removed with an Aluminum etchant. One of the bigger obstacles was that most Aluminum etchants also etch Copper and hence would not only remove the Aluminum DRIE protective mask, but would remove the all-important electrode from underneath. Finally, after much searching, experimentation, and frustration, Sodium Hydroxide (NaOH) was used.

During the final step of the final assembly, thermo-compression bonding, a problem was encountered with the MEMS layer. The two platens that pressed against either side of the device layers would press hard enough on the floating MEMS plate that it would actually lightly adhere to the dielectric layer; effectively immobilizing the plate. This problem was alleviated by putting a dummy piece of Kapton in between each floating MEMS plate and the dielectric layer and removing it after bonding.

Another problem encountered during the final bonding and assembly process pertains to the bonding film. During the heating phase of the bonding process, the spacer layer film actually changes to a semi-liquid state and can flow out from underneath the MEMS layer. This is not generally a problem in the open spaces of the filter, but the two main locations where problems arose were around the MEMS plates themselves, but much more so in the small space in which the biasing inductor was to be soldered. A simple yet extremely tedious remedy was to physically remove this excess manually.

While effective on a small, prototyping scale, this would need to be worked out in any implemented manufactured design.

Overall, in the future, it might actually be simpler to start with plain, unclad Kapton and deposit the metal layers as needed. This would alleviate most of the chemical incompatibilities as well as the need for etching Copper and NiChrome off the back side of the material. There also may be some interesting experimentation in packaging once a definite, more reliable process was developed.

CHAPTER 4: CHIP-IN-POLYMER PACKAGING TECHNOLOGY

4.1 Introduction[1]

Another aspect of miniaturizing components is in the area of electronics packaging. Long ago, in the earliest days of experimentation with electricity, electronic devices were so bulky, dangerous, and fragile that there was simply no other packaging to be done than that which kept the part safe and operational. In today's ever-shrinking world it is most profoundly not so. At the very instant the first silicon chip was put into a sealed package, an entirely new realm of electronics development and manufacturing was born.

The problem with the bulkiness of most packaging comes from the material used with which to encapsulate the device. More often than not this package is of a very box-like form, constructed from a rigid material, and without space efficiency in mind. With the advent of robotic soldering and solder re-flow ovens that do not require the human element to enter the picture, surface-mount packaging stepped in and took the packaging industry down by almost an order of magnitude. Assuming the principles of packaging remain the same, the size of a device's packaging will get ever larger with respect to the size of the device itself. However, there is a new concept in the packaging world: embedding a chip inside a substrate all its own (usually a polymer) that is sealed and

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[1] The discussion in this chapter is based heavily on the currently unpublished work [12]

ready to be used. The idea behind packaging a silicon die inside a polymer substrate is to eliminate the need for traditional packaging altogether. The purposes of packaging are to prevent damage to the device, to allow easy electronic access to the fabricated silicon devices, and to physically mount the device to something larger for stable, steady, and continued use. So any packaging that were attempting to replace traditional packaging would have to accomplish these goals, if not exceed them.

Ultra-thin, flexible electronics are advantageous for integration into space-based radar, biomedical sensors, wearable electronics, multifunction surfaces and low profile applications. Although flexible interconnects have been successfully demonstrated for these applications [13], the embedding of thinned, flexible semiconductor die will greatly enhance the application of this technology. Die thinning, thin multilayer substrates, and the elimination of solder joints are required to meet the thickness targets for these applications. A process sequence has been developed to achieve final thicknesses of 50-75mm.

4.2 Previous Efforts

The simplest way to cut off a chip from exposure to the outside world is to coat it with something, in a sense just basically encapsulate it in a sealant. This is, however, completely impractical in that the device is no longer electrically accessible to the outside world. Although, if a silicon die were sandwiched between two layers of a polymer film with metal traces leading outward, most of the desired effects would be accomplished.

Zhenwei Hou developed a process that did just that [14]. This project was more oriented towards the actual physical connection between the chip itself and its LCP substrate as well as the effects of physical flexing of the circuit on the circuit's electrical performance. This was accomplished by attaching a thinned die to a holder die, preparing a substrate of LCP, bonding them together via thermal compression bonding, and sealing the back side with another layer of LCP. Figure 26 below shows a diagram of this process flow.

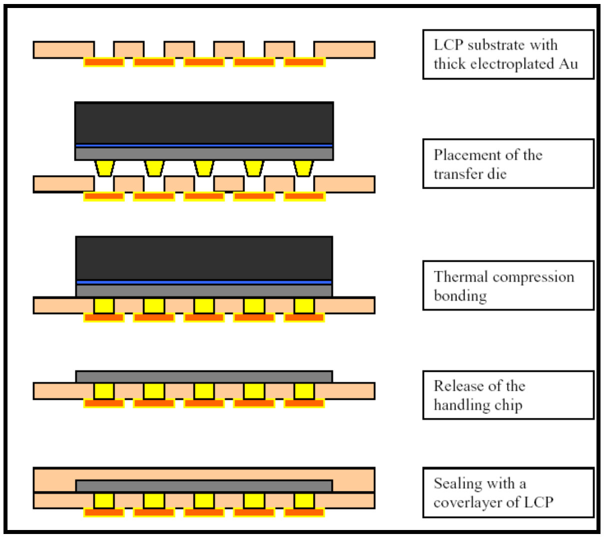

Figure 26 Assembly process for Hou's work with LCP

However, this project is interested in developing a process with which Flexible Printed Circuit Board (PCB) processing techniques and photolithography processing can be combined to integrate a chip into a polymer substrate. Meyer et al. also worked with integrating polymer interconnects with silicon chips, but this process also was not based on PCB technology processing, nor on a flip chip bonding, but on a wire bonding technique. While yet another group utilized the same substance as the dielectric layer in Chapter 3 of this work, BenzoCycloButene, as an adhesive to secure the die during processing [15]. Figure 27 below summarizes their process flow.

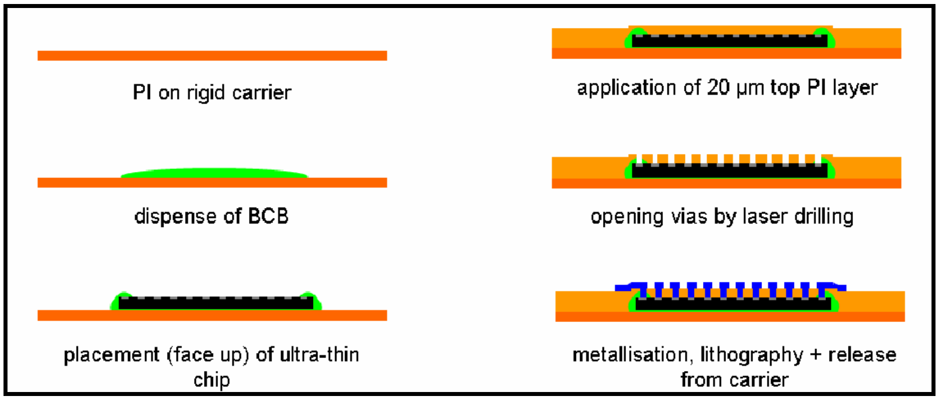

Figure 27 Assembly process for Christiaens' et al. process

4.3 Die Thinning

Multi level 3-D flexible assemblies have been demonstrated with die that were thinned to around 50µm [16]. However, if the die can be further thinned to around 10µm, the resulting 3-D assemblies can be far more flexible. Therefore the fabrication sequence begins with die thinning. Wafers are pre-sawn to a depth of 75µm and then mechanically thinned to 50µm, resulting in individual die. The die are then mounted face down onto handle die (500µm thick Si die diced to the dimensions of the thinned die) using a thin adhesive layer. Using Deep Reactive Ion Etching, the 50µm die are then further thinned to 8-10µm. The handle die keeps the thinned die planar, protects the face during processing and aids in handling.

4.4 Fabrication and Assembly

Polyimide layers have been utilized in the realization of complex 3-D interconnect layers because the material can be deposited as a thin insulating layer; it can be micromachined to realize very small vias; it adheres well to Si, deposited metal traces and previously deposited polyimide layers; and it has a high moisture resistance [17].

Therefore HD Microsystems polyimide product PI-2611 was selected as the substrate material in this application. The substrate fabrication begins with patterning of alignment marks in a thin film metal layer deposited on a Si wafer. After spinning the corresponding Adhesion Promoter VM651 around the periphery of the Si wafer, a layer of PI-2611 polyimide is then applied by spin coating and is fully cured. Then a layer of HD Microsystems polyimide product PI 2556 is spin coated on top of this cured layer to serve as an adhesive for the thinned die. The thinned die with the handle die still attached are then placed onto this adhesive layer using the alignment marks for placement reference. The polyimide is then cured using a slow curing profile to allow volatiles to escape out from under the die. Once the polyimide is fully cured, the handle die is removed by soaking in a solvent solution to dissolve the die bonding adhesive. A second layer of PI-2611 is spin coated and cured over the die, and contact holes to the wire bonding pads on the thinned die are created with reactive ion etching. A short Ar ion cleaning step is then used to remove oxide from the surface of the exposed die wire bonding pads. A thin film Ti/Cu seed layer is then vacuum-deposited. A photoresist layer is patterned and Cu is electroplated onto the seed layer to realize electrical traces connected to the thinned die wire bonding pads. The photoresist and exposed Ti/Cu seed layer are then removed with a wet etching step. The polyimide/Cu process is repeated to create the required interconnect structure to form an electrically accessible chip embedded inside the polyimide-based substrate. The completed multichip circuits are then released from the silicon wafer, creating an ultra-thin, flexible circuit.

4.5 Problems and Future Work

The results obtained thus far in the project have been very encouraging. The main concerns of the process were getting strong enough adhesion of the die to the polyimide and the ability to handle die of the thicknesses discussed. These have proven attainable, but only under strict process restrictions and with certain process steps in place. A Dehydration Bake is absolutely necessary due to uncured polyimide being strongly hydrophilic. If there is any moisture present when the substance is cured it will evaporate from within the layer and form pockets and voids in the layer. Also, a simple plasma etch (can be either Oxygen, or Nitrogen) for a minute or so is necessary to roughen up the surface of cured polyimide to attain good adhesion of any additional layers desired on top of the cured layer. This serves the same purpose as the Adhesion Promoter which only works between polyimide and silicon or silicon dioxide.

By far the most difficult issue in the process is the two die alignment problem. Normally once a process is developed, Pick-and-Place machines would do the work of aligning the thinned die to their destinations. However in such a prototyping stage as the project is in, the use of such a machine is neither practical nor affordable. With the human element forced into the picture, aligning a die to within 2-3µm of where it is intended to be becomes a non-trivial issue. This creates an even larger problem when there are multiple die in one design. For example, if the die can be placed by hand within 5% of their destination, and the patterning can only afford 10% misalignment error, placing a mere 2 die by hand pushes the error to the allowable 10%.

Future research in this area might include investigating different methods to overcoming the two die alignment problem. Being such a process-oriented problem it seems there should be a way to build a self-aligning pattern in which the alignment of the die has a much higher alignment tolerance than the rest of the process masks. Another issue that might reduce fabrication costs in the future is finding a reusable substrate. The process of fabricating the device requires it to be on a rigid substrate during fabrication, however in order to remove the finished device from the substrate, the device (and hence the substrate) is usually diced or scored to remove the device. If the substrate could be recycled to serve again through another process it would reduce production cost.

CHAPTER 5: CONCLUDING REMARKS AND FUTURE WORK

In this thesis, a CPA tunable from 4.92 GHz at 0V to 5.40 GHz at 19.5V with a return loss of greater than 14dB has been discussed. The antenna provides a return loss better than 32dB in the tunable frequency range of 5.16 to 5.40GHz. These types of tunable antenna will find potential use in next generation multi-standard wireless communication systems. For the future work in the area of CPA tunable antennas, it would be worth investigation to see if there would be any benefit to compressing the size of the antenna iself in addition to adding tuning. An interesting field of study in antennas right now is fractal antennas, typically sought after to accomplish multiple operating ranges. If a fractal antenna could be fabricated in such a way as to facilitate tuning of both regions of operation simultaneously or otherwise it would be a revolution in miniaturizing the RF front end of a system.

Polymer MEMS Varactors have been monolithically integrated with an LCP based lumped element bandpass filter by low coast PCB processing techniques. The measured center frequency of the MEMS filter is 1.714GHz and 1.650GHz for 0V and 250V respectively. These results demonstrate the feasibility of integrating of polymer MEMS devices with embedded passives technologies.

The chip-in-polymer technology is still in the early stages and there is a considerable commercial interest on this topic in the packaging community. Smartcards, organic LEDs, and flexible circuits, are only the beginning of a practically untapped wealth of applications of new technologies. Tying this together with the Radio Frequency Identification industry will spawn an entirely new generation of practically invisible technology that will revolutionize our world.

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APPENDIX A

A.1 Detailed Fabrication Procedures (MEMS layer)

A.1.1 Kapton film cleaning

Step 1 Acetone/Methanol Cleaning

Cleaner	First Acetone then Methanol
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until film is completely dry

Step 2 Oxidation Removal

Remover	250 ml DI water + 2 drops of H_2SO_4 using a pipette
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until film is completely dry

Step 3 Acetone/Methanol Cleaning

Cleaner	First Acetone then Methanol
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until film is completely dry

A.1.2 Etching the backside of the Kapton film

Step 1 Copper Etching

Etchant	CE-200
Time	8 secs
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until film is completely dry

Step 2 Nichrome Etching

Etchant	250 ml DI water + 10 gm $KMnO_4$ + 5 gm NaOH
Time	60 secs
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until film is completely dry

Step 3 Acetone/Methanol Cleaning

Cleaner	First Acetone then Methanol
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until film is completely dry

A.1.3 Sticking the film on a wafer

Step 1 4" Wafergrip application

Peel wafergrip and put it on a clean and smooth wafer

Step 2 Heat wafer on hot plate

Temperature	110 ^{0}C
Time	till wafergrip melts and sticks to the wafer

Step 3 Stick film on wafer

While the wafer gel is still in molten state, stick the kapton film starting with one edge and smoothing the entire film on the gel without any unevenness

A.1.4 Defining the electrode

Step 1 Photoresist application

Photoresist	S1813
Spin Speed	2500 rpm
Spin Ramp	500 rpm
Spin Time	30 secs

Step 2 Soft bake

Temperature	110 ^{0}C
Time	60 secs

Step 3 Photoresist Exposure

Mask used	ELECTRODE_50_um _AU_GT
Exposure Time	15 secs

Step 4 Photoresist Develop

Developer	CD-30
Time	45 secs
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until film is completely dry

Step 5 Post Develop Bake

Temperature	110 ^{0}C
Time	60 secs

Step 6 Copper Etching

Etchant	CE-200
Time	8 secs
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until film is completely dry

Step 7 Photoresist Removal

Photoresist Remover	First Acetone then Methanol
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until film is completely dry

Step 8 Nichrome Etching

Etchant	250 ml DI water + 10 gm $KMnO_4$ + 5 gm NaOH
Time	60 secs
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until film is completely dry

Step 9 Acetone/Methanol Cleaning

Cleaner	First Acetone then Methanol
DI Rinse	30 secs in a bowl of slightly agitated DI water

N_2 dry	until film is completely dry

A.1.5 Aluminum deposition

Step 1 Oxidation Removal

Remover	250 ml DI water + 2 drops of H_2SO_4 using a pipette
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until film is completely dry

Step 2 Acetone/Methanol Cleaning

Cleaner	First Acetone then Methanol
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until film is completely dry

Step 3 Aluminum deposition

Process	E-beam
Thickness	5000 ^{0}A

Step 4 Acetone/Methanol Cleaning

Cleaner	First Acetone then Methanol
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until film is completely dry

A.1.6 Patterning film for DRIE

Step 1 Photoresist application

Photoresist	S1813
Spin Speed	2500 rpm
Spin Ramp	500 rpm
Spin Time	30 secs

Step 2 Soft bake

Temperature	110 ^{0}C
Time	60 secs

Step 3 Photoresist Exposure

Mask used	Kapton_AU_GT
Exposure Time	15 secs

Step 4 Photoresist Develop

Developer	CD-30
Time	45 secs
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until film is completely dry

Step 5 Post Develop Bake

Temperature	110 ^{0}C
Time	60 secs

Step 6 Aluminum Etching

Etchant	PAE
Time	15 mins

A.1.7 DRIE and subsequent Aluminum Etching

(a) Multi-Step DRIE

Step 1 DRIE

Time	25 mins
Cycles	3

Step 2 Aluminum Etching

Etchant	6 gm NaOH + 200 ml DI water
Time	3 mins

Step 3 Acetone/Methanol Cleaning

Cleaner	First Acetone then Methanol
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until film is completely dry

(b) Single Step DRIE

Step 1 DRIE

Time	75 mins
Cycles	1

Step 2 Aluminum Etching

Etchant	6 gm NaOH + 200 ml DI water
Time	3 mins

Step 3 Acetone/Methanol Cleaning

Cleaner	First Acetone then Methanol
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until film is completely dry

A.1.8 Defining the bias lines

Step 1 Photoresist application

Photoresist	S1813
Spin Speed	2500 rpm
Spin Ramp	500 rpm
Spin Time	30 secs

Step 2 Soft bake

Temperature	110 ^{0}C
Time	60 secs

Step 3 Photoresist Exposure

Mask used	BIAS_LINES_AU_GT
Exposure Time	60 secs

Step 4 Photoresist Develop

Developer	CD-30
Time	45 secs
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until film is completely dry

Step 5 Post Develop Bake

Temperature	110 ^{0}C
Time	60 secs

Step 6 Copper Etching

Etchant	CE-200
Time	8 secs
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until film is completely dry

Step 7 Photoresist Removal

Photoresist Remover	First Acetone then Methanol
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until film is completely dry

A.1.9 Final film cleaning

Step 1 Wafer gel Cleaning

Cleaner	Amyl Acetate
Temperature	150 ^{0}C
Time	until film lifts off the wafer with no residual wafer gel on it

Step 2 Acetone/Methanol Cleaning

Cleaner	First Acetone then Methanol
DI Rinse	30 secs in a bowl of slightly agitated DI water

N_2 dry until film is completely dry

A.2 Chemical Incompatibilities

- Copper etchant, CE-200 removes Aluminum faster than it removes copper.
- Photoresist Developer, CD-30, attacks Nichrome while H_2SO_4 does not.
- Nichrome etchant reacts with photoresist, S1813.
- Aluminum etchant, NaOH, reacts with photoresist, S1813.
- Photoresist Developer AZ 400K attacks NiChrome.

A.3 BCB Dielectric Layer Deposition

These steps are for approximately 1um final thickness, mixed 2:1 (BCB: T1100)

1) Put BCB/T1100 mixture on stirrer for about half and hour to ensure good solution

2) Adhesion Promoter AP3000:
    a. Spin 3000rpm, 30 sec
    b. Bake 120C, 30 sec

3) BCB:
    a. Pout BCB/T1100 mixture onto the wafer, let sit for about 1min.
    b. Spin 500rpm, 5 sec -> 2000rpm, 30sec
    c. Bake 95C, 90 sec
    d. Expose 10 sec

4) Develop (on the spinner)
    a. Pour DS2100 onto the wafer and let sit for about 15 sec.
       -continue pouring DS2100 onto the wafer every 15 sec. for 60 sec.
    b. Spin 1000rpm 5 sec (keep pouring DS2100) -> 2500rpm, 30 sec (drying)
    c. Bake 75C, 60 sec

Notes:
-DO NOT clean wafer with acetone/methanol after BCB is deposited.
-DO NOT use a film mask to expose, you must use a glass mask.