IMPACT OF CHARGE COLLECTION MECHANISMS ON SINGLE EVENT EFFECTS IN SIGE HBT CIRCUITS AND HARDENING IMPLICATIONS

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A Thesis

Submitted to

the Graduate Faculty of

Auburn University

in Partial Fulfillment of the

Requirements for the

Degree of

Master of Science

Auburn, Alabama
August 10, 2009

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THESIS ABSTRACT

IMPACT OF CHARGE COLLECTION MECHANISMS ON SINGLE EVENT EFFECTS IN SIGE HBT CIRCUITS AND HARDENING IMPLICATIONS

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Master of Science, August 10, 2009
(B.S., Huazhong University of Science and Technology, 2000)

94 Typed Pages

Directed by Guofu Niu

Investigations into single event effect (SEE) induced charge collection in Silicon Germanium (SiGe) heterojunction bipolar transistors (HBT) are made through three-dimensional (3-D) device simulation. The transistor is constructed based on actual device. The results indicate that collector-substrate (CS) junction plays an important role due to the reverse biased CS junction. Therefore by adding a dummy collector to the HBTs, a recently published radiation hardening by design (RHBD) technique, the total collector collected charge can be reduced due to reduction of the diffusion charge collection at the intrinsic CS junction.

At present, the single event upset (SEU) sensitivity is primarily characterized using the total amount of collector charge collected during an ion strike. This, however, may not be accurate, as the contributions of different charge collection processes are greatly influenced by external loading and the circuit topology. The individual impact of drift and diffusion charge collection at the collector-base (CB) and CS junctions on SiGe HBT current mode logic (CML) circuit SEU is examined. The CS junction diffusion charge collection has negligible impact on circuit SEU, despite its large charge collection magnitude. The CB drift charge collection is as important as the CS drift charge

collection, even though its charge magnitude is much less, because the resulting current excitation appears between collector and base nodes, and hence is amplified. Using selective ion track placement in 3-D simulations, we further find that an ion track passing through the physical CS junction is much more effective in causing SEU than an ion track not passing through the CS junction. This is attributed to potential funneling and consequent large induced drift current magnitude, which is necessary for SEU of CML circuit.

For emitter followers, the conventional hardening approach to minimize SEE is using a higher emitter biasing current as the emitter current determines output. This, however, is shown to not work at all with 3-D mixed mode simulations. Instead, it is the CB junction charge collection that dominates emitter output SEE, because CB junction charge collection determines the base voltage deviation, and the emitter output follows the base deviation. Therefore, the impedance and the electric field across the CB junction are the most important factors affecting emitter follower SEE. From the simulation results, the product of SEE induced base current and the base biasing impedance determines the amount of base voltage upset or deviation. For base biasing impedance values found in practical circuits, a smaller base biasing impedance should be used to reduce emitter output voltage SEE, as the emitter voltage upset tracks the base voltage upset.

ACKNOWLEDGMENTS

I am deeply indebted to Dr. Guofu Niu for his technical, educational and moral support throughout my Master program. I am deeply influenced by his research and teaching philosophy which made my graduate work an educational and professionally enriching experience. I would also like to thank Dr. Fa Foster Dai and Dr. Vishwani Agrawal for their encouragement and for being my committee.

I would like to thank Muthubalan Varadharajaperumal and Lan Luo for their help on the software. I would like to thank my wife, Xiaoyun Wei for her great support to my research work as well as my life. Also, I would like to thank my family and friends for their encouragement and support all through my research.

This work was supported by NASA-GSFC under NASA Electronic Parts, Packaging Program and DTRA under the Radiation Hardened Microelectronics Program, and the NASA ETDP Program under Contract NNL06AA29C. I would like to thank K. A. LaBel, NASA-GSFC, P. W. Marshall, consultant to NASA-GSFC, J. D. Cressler of Georgia Institute of Technology, R. A. Reed of Vandabilt University, and Alvin Joseph of IBM Microelectronics, for their contributions and support.

Style manual or journal used Journal of Approximation Theory (together with the style known as “aums“). Bibliography follows van Leunen’s *A Handbook for Scholars*.

Computer software used The document preparation package TEX (specifically LATEX) together with the departmental style-file `aums.sty`.

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CHAPTER 1

INTRODUCTION

1.1 Motivation

Electronics in spacecrafts and satellites can be degraded significantly by the natural space radiation environment mainly through three manners, total dose ionizing radiation damage, single event related soft and hard errors, and displacement damage [1] [2]. This work will deal with single event effect (SEE) in Silicon-Germanium (SiGe) Heterojunction Bipolar Transistor (HBT) electronics that is being actively investigated for space applications.

SiGe HBT has generated considerable interest in the space community due to its robustness to total ionizing dose radiation (TID) without any additional hardening [3] [4]. But, recently, high speed SiGe HBT digital logic circuits were found to be vulnerable to single event upset (SEU) [5] [6]. Hence it is important to study the SEE on SiGe HBT circuits.

SEE is defined as deleterious effects in the devices caused by the deposition of energy within electronic devices by a single energetic particle. The major types of SEE namely are SEU, single event latchup (SEL), single event snapback (SESB), and single event transient (SET), etc [7] [2]. This work focuses on SEU in current mode logic (CML) circuits and SET in emitter followers.

1.1.1 Single Event Upset in CML Circuit

It is difficult to evaluate circuit SEU sensitivity experimentally. A convenient approach is to study the charge collection characteristics of the struck device, and compare the collected charge to some critical charge to upset. Critical charge is primarily characterized using the total amount of collector charge collected during an ion strike [8] [9]. However, the usefulness of this approach is extremely limited, since the critical charge itself may be ill-defined, and dependent on external loading and specific circuit designs [10] [11] [12] [13]. Nevertheless, unloaded device simulation has been useful for studying the basic physical properties of charge collection, and for studying circuits where loading effects are not as prevalent and critical charge is well-defined [14].

Drift and diffusion charge collections at different junctions have different impact on circuit SEU. To find out the most dominate factors responsible for CML circuit SEU, different charge collection processes need to be examined individually. By this way, the mechanisms behind different phenomena observed in CML circuits SEU can be better understood, and the guidelines for transistor- and circuit- level hardening techniques can be provided.

1.1.2 Single Event Transient in Emitter Followers

Investigations into charge collection in SiGe HBTs indicate that collector charge collection, particularly through the reverse biased collector-substrate (CS) junction, is the dominant path for ion-induced charge to be collected. Therefore, the resulting hardening techniques focus on collector charge collection, and apply to circuits in which the collector current determines circuit output, such as emitter coupled logic (ECL) circuits. Such techniques, however, do not apply to circuits where the emitter current determines circuit output. An example is emitter follower, which is widely used as output buffer, unity voltage gain amplifier, dc power regulator in analog circuits, as well as level shifter in ECL circuits. SET simulations using three-dimensional (3-D) mixed mode simulation in SiGe HBT emitter followers are demanded.

To improve SEE immunity in emitter followers, conventional wisdom of designers tends to use a higher biasing emitter current, as the emitter current determines output. However, our simulations show this intuitive approach is completely incorrect, as it does not consider the complex operation of the circuit during SET. Parametric analysis of emitter followers is performed to find out the design parameters that are essential to emitter follower SET. Guidelines on how to improve emitter follower SET can then be provided.

1.2 Silicon Germanium HBT

The basic formulation and operational theory of the HBT was in place by Kroemer in as early as 1957 [15] [16]. Research and development activity in SiGe devices, circuits, and technologies in both industry and at universities worldwide has grown rapidly since the first demonstration of a functional SiGe HBT in 1987 [17] [18]. Commercial SiGe HBT technologies now exist in companies around the world, including: IBM, Philips, Infineon, IHP, etc. In recent years, a variety of papers demonstrating impressive digital, analog, RF, and microwave circuit results for wireless and wireline communications applications were published.

Fig. 1.1 shows the 2-D cross section of a typical SiGe HBT. A small amount of Germanium is introduced into the base of a silicon (Si) bipolar junction transistor (BJT). As a consequence, the Ge-gradient-induced drift field across the neutral base is aligned in a direction from collector to emitter such that it will accelerate the injected minority electrons across the base and thereby reduce the base transit time. Because the base transit time typically limited the frequency response of a Si BJT, the operating speed can be improved by a factor of 2-3 over conventional BJT. In addition, the Ge-induced band offset at the emitter-base (EB) junction exponentially enhances the collector current density (and thus β) of a SiGe HBT compared to a comparably constructed Si BJT.

Experimental results suggest that SiGe HBTs have much better TID tolerance than conventional diffused or even ion-implanted Si BJT technologies (even radiation-hardened ones) [18]. This observed radiation hardness is attributed to the unique and inherent structural features of the SiGe

HBT itself through careful comparisons between identically fabricated SiGe HBTs and Si BJTs (same device geometry and wafer lot, but without Ge in the base for the epitaxial-base Si BJT) [18].

Note that these SiGe HBTs compare very favorably in both performance and radiation hardness with (more expensive) GaAs HBT technologies that are often employed in space applications requiring both very high speed and an extreme level of radiation immunity [19]. Furthermore, SiGe's fabrication compatibility with conventional Si CMOS processing ensures that both high-speed SiGe HBTs and aggressively scaled CMOS devices can be co-integrated on the same Si wafer, making it possible to combine analog, RF/microwave, and digital functions on a single chip.

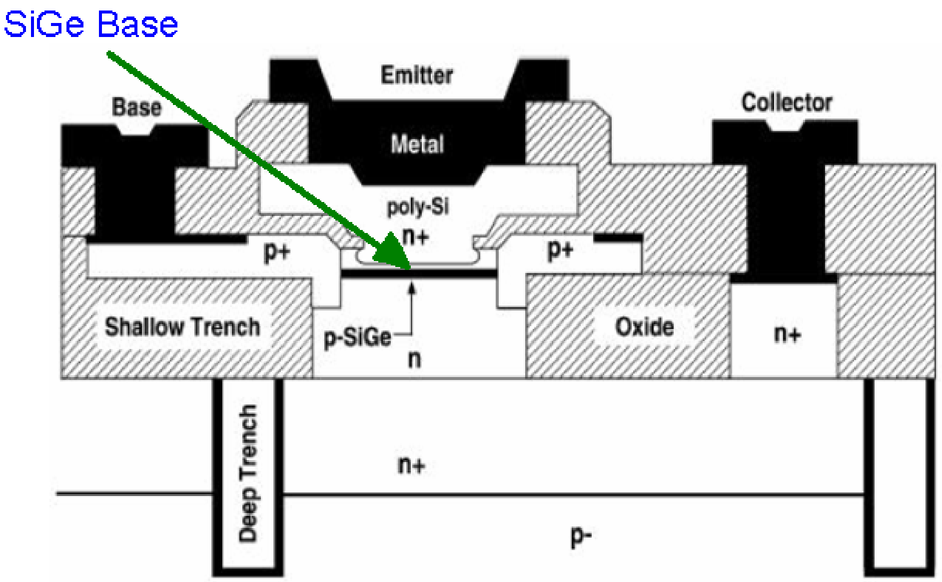


Figure 1.1: 2-D cross section of a typical SiGe HBT used in simulation.

1.3 Single Event Effect and Single Event Transient

Space is full of highly energetic particles. As they pass through the semiconductor material, the ions strip electrons from atoms, leaving behind a track of unbound electrons and holes. When the track passing through or near a region with an electric field, such as exists in a semiconductor *pn* junction, the free electrons and holes are separated and collected at electric contacts, giving rise to an electric current at each contact. It is the electric current that causes all SEEs [2]. In a word, the mechanisms contributing to SEE are charge generation, charge collection and circuit response.

Fig. 1.2 shows the electron and hole pairs generated along ion strike path in a *pn* junction [4]. The electrostatic potential is disturbed in the junction and this disturbed field extends deep to the substrate. The disturbed field collects charge deposited deep in the substrate.

SEE can be classified into two categories, destructive SEE and non-destructive SEE. SET and SEU in logic or memory circuits are examples of non-destructive SEE. An SET is defined as a momentary voltage excursion (voltage spike) at a node in an integrated circuit [2]. Under certain conditions, the voltage spike can propagate away from where it was generated and eventually appear at the circuit's output. When an SET is captured, e.g. by a latch, it becomes an SEU. Up to date, the studies of SET in digital logic circuits are relatively less than those of SEU. Significant increase in error rate due to SET is observed in very fast logic circuits [20] [21] [22]. Besides, SET is also observed in analog (linear) circuits and opto-electronic circuits in space [23] [24]. Therefore, SET simulation becomes indispensable in space applications.

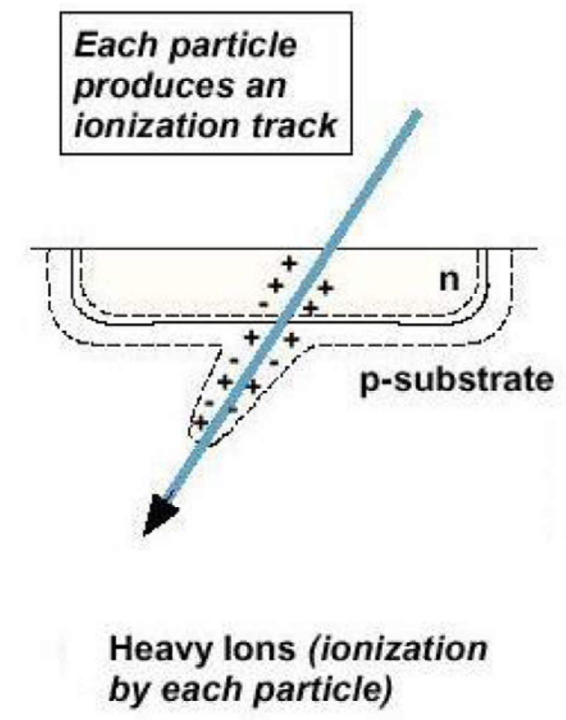


Figure 1.2: Illustration of a heavy ion passing through a *pn* junction.

1.4 3-D Device Simulation

The inherently 3-D nature of an ion passing through a microelectronic device needs advanced 3-D modeling tools. The most commonly used formalism for device simulation is that of driftijdiffusion models. There are three equations to be solved, the Poisson equation and the current continuity equations, together with the constitutive relationships for current density (the actual driftijdiffusion equations) [25]. These equations are discretized and solved at each mesh point. A typical SEE simulation of single device is performed in three steps, which will be detailed in Chapter 2. First, a stand alone device is built using MESH. The boundaries of all the device regions are constructed using layers of cuboidal blocks, which is a simplified strategy compared to using polyhedrons. Second, the device is doped according to the secondary ion mass spectrometry (SIMS) data and meshed. Finally, an SEE transient simulation is executed in 3-D device simulator, e.g. DESSIS.

There are mainly two issues central to any device simulation. One is the ion strike track structure, the other is that of gridding, or mesh generation. Experimental results have highlighted the need to include realistic charge generation profiles in SEE simulations [26] [27]. The variation of charge density along the path and around the path of an incident particle both need to be correctly modeled. Gaussian function is available and prevalent in most device simulators. Dense mesh points are necessary at sensitive regions for both correct device electrical characteristics and SEE results, e.g. at *pn* junctions, along the ion track path.

1.5 Circuit Simulation

Unloaded device simulation has been useful for studying the basic physical properties of charge collection and for studying circuits where loading effects are not that important. However, the impacts of SEE induced charge collection are greatly influenced by external loading and the feedback mechanism in lots of circuits, e.g. D-flip flop (DFF) in Chapter 4 and emitter follower in Chapter 5 [11]. The coupling of device and circuit response to incident ionizing radiation can be predicted through two mixed mode approaches as below.

The first approach models the single event induced transient currents as current sources at the struck nodes and calculates the effects on circuit outputs with a circuit simulator such as Cadence Spectre [13] [28] [29]. This approach can handle large scale circuits efficiently. A drawback is the accuracy of the transient currents used as the input stimulus as the transient currents are normally from 3-D device simulation of a struck unloaded device. The circuit result inherits the inaccuracy of the improperly loaded device simulation. Still, this approach has provided considerable insight into circuit SEU and has resulted in improvements to hardening techniques for a variety of circuits [30] [31] [32].

The second approach finds the concurrent solution of device and circuit equations. The struck device is modeled in the "device domain" (e.g. using 3-D device simulation) while the rest of the circuit is represented by SPICE-like compact circuit models [11]. The two domains are tied together by the boundary conditions at contacts, and the solution to both sets of equations is rolled into one matrix solution [33] [34]. This approach reduces simulation times and greatly increases the complexity of the external circuitry that can be modeled since the circuit consists of computationally efficient SPICE models except only the struck device. This kind of mixed mode simulation has been incorporated into most of the commercially available 3-D device simulators [35] [36] [37].

The drawback of these two mixed mode methods is that coupling effects between adjacent transistors cannot be taken into account, which have been shown to exist at the device level using 2-D simulations [38]. To address this difficulty, it is necessary to simulate the entire circuit in the 3-D device domain, namely full-cell device simulation [39] [40]. As inter-device spacing decreases with increasing integration levels, coupling effects can be expected to become more important, and simulating the entire circuit in the device domain may become routinely necessary [39]. However, mixed mode simulation is still useful for in-depth studies of SEU in specific circuits for given ion strikes. Both mixed mode approaches will be detailed in Chapter 3, and applied on circuit simulations in Chapter 4 and 5.

1.6 Thesis Contributions

The 3-D structure of a regular 0.5μm SiGe HBT is detailed and the SET simulation results are shown in Chapter 2. Based on charge collection mechanisms of this single device, a four-current-source model and a simplified two-current-source model are detailed, which provide a practical approach to include SEE in circuit simulators. A hardened HBT with a dummy collector is examined to reduce the CS junction diffusion charge collection effectively. However, this technique does not improve certain circuits' SEU immunity as detailed in Chapter 4 and Chapter 5.

Advantages and disadvantages of true and combined mixed mode simulations are discussed in Chapter 3. Taking DFF as an example, combined mixed mode provides similar SEU results to true mixed mode, but with high computational efficiency and large scale circuit capability. Therefore, combined mixed mode is still favorable for circuit SEU simulations where loading effects are not that prevalent.

Chapter 4 presents combined mixed mode simulation results for a DFF circuit. The impacts of different charge collection mechanisms are examined by manually separating collector charge collection to collector-base (CB) and CS junction drift and diffusion charge collection. The charge collection processes that dominate the storage cell upset in a DFF are investigated. Regional analysis in device domain is performed to further verify the conclusions. The implications on different ion strike location and hardening techniques are discussed.

Chapter 5 presents true mixed mode transient simulation results for a typical emitter follower topology. Parametric analysis is performed to figure out the factors that are responsible for emitter voltage upset. Guidelines to reduce emitter voltage upset in real circuit designs are then provided.

CHAPTER 2

CHARGE COLLECTION

To understand circuit SEE, it is important to first understand the physical mechanisms responsible for SEE in a single transistor [41]. At device level, the SEE induced transient currents are obtained using 3-D device simulation. The 3-D transistor is constructed based on the actual device layout and the SIMS data from the IBM SiGe HBT technology. All of the regions of the device must be accounted for, including the deep and shallow trench isolation (DT and STI). A top substrate contact and a sufficiently large simulation area are necessary to keep simulation conditions consistent with physical reality. The 3-D device structure and simulation conditions will be detailed in Section 2.1.2 and Section 2.1.3.

SEE is caused by the collection of charge deposited along the ion strike path at the sensitive regions of a microelectronic device or circuit. Charge generation depends on the incident ionÐs mass and energy and on the properties of the material through which it passes. Therefore, the same charge generation mechanism will apply to all devices and circuits manufactured in silicon. A uniform linear energy transfer (LET) function with a Gaussian radius is used to model the heavy ion strike in this work. Charge collection depends on electrical parameters such as biasing voltage and doping levels in the semiconductor. For single device simulation, the emitter, collector, and base terminals are unloaded and grounded. The substrate is biased at a negative potential, which is always the lowest potential in a practical circuit. The reverse biased CS junction collects most of the deposited charge as shown in Section 2.1.3. Based on charge collection analysis, transistor-level hardening techniques have been developed to improve the SEU immunity. A recently published dummy-collector hardening technique can effectively reduce CS diffusion charge collection by adding a dummy CS junction outside DT. The technique will be detailed and verified in Section 2.2.2, which is later used as the hardening technique in Chapter 4.

2.1 Regular SiGe HBT Device

2.1.1 Basic Device Structure

Fig. 2.1 shows the top view of a regular SiGe HBT. DT is used to isolate the transistor from the other adjacent devices. NS layer is a heavily doped n^+ buried layer for low resistance collector contact. The length and width of the transistor are noted as W_E and L_E, which are much smaller than the dimensions of the silicon region inside DT.

Fig. 2.2 illustrates the 2-D cross section of the SiGe HBT along the Y-cut in Fig. 2.1. The transistor is built on a lightly doped p-type silicon substrate. SUB is the top substrate contact. The intrinsic transistor contains an n^+ emitter, a p-type SiGe base, an n-type collector, and an n^+ buried layer. With Ge in the base, it makes two heterojunctions, EB junction and CB junction.

2.1.2 Device Construction in MESH

Fig. 2.3 shows the 3-D structure built using MESH for the HBT device illustrated in Fig. 2.1 and Fig. 2.2. The construction starts with a large piece of silicon substrate of an area of 28 μm × 25 μm and a depth of 25 μm, as well as a top substrate contact is used to minimize simulation errors associated with charge collection [42]. Doping of the substrate is boron, $10^{15} cm^{-3}$. The whole surface is covered by silicon oxide except the openings for the transistor, and the contacts for collector and substrate.

Fig. 2.4 shows the 2-D cross section with gridding of the 3-D structure at y=0. The transistor is only several microns thick on the top of the silicon substrate surface. The vertical structure consists

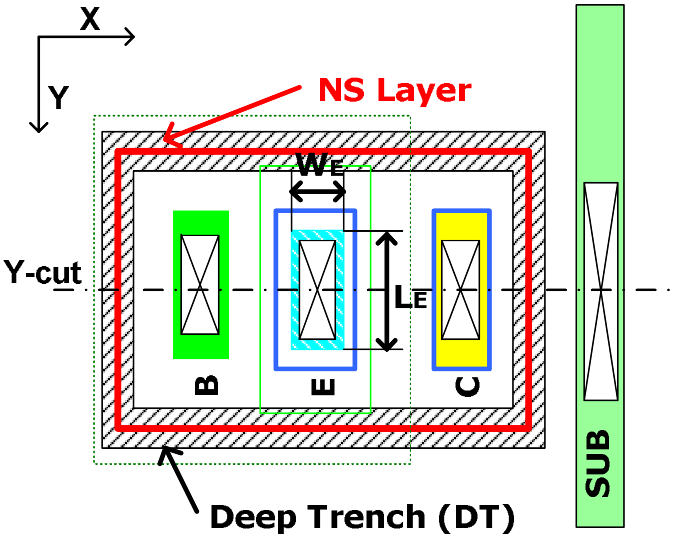


Figure 2.1: Top view of a regular bipolar transistor

of an n^+ polysilicon emitter, a *p*-type epitaxial base, an *n*-type collector, an n^+ buried layer, and a lightly doped *p*-type substrate [43]. A gradient Ge profile is added to the base. The equations for potential, electric field, electron concentration, and hole concentration are solved at each node of the mesh grid. Fine meshes are used along the path of the ion strike and at the *pn* junction interfaces as shown in Fig. 2.4. The average number of nodes is approximately 10^4 for each simulation.

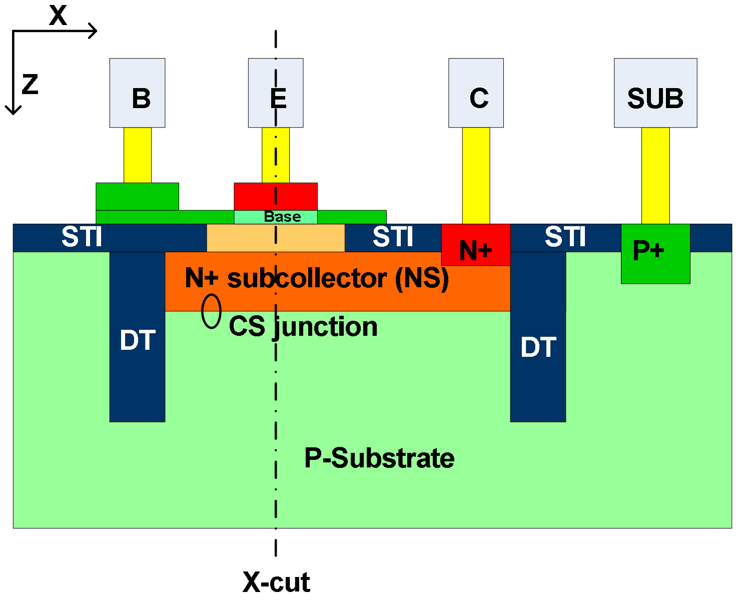


Figure 2.2: 2-D cross section of a regular bipolar transistor

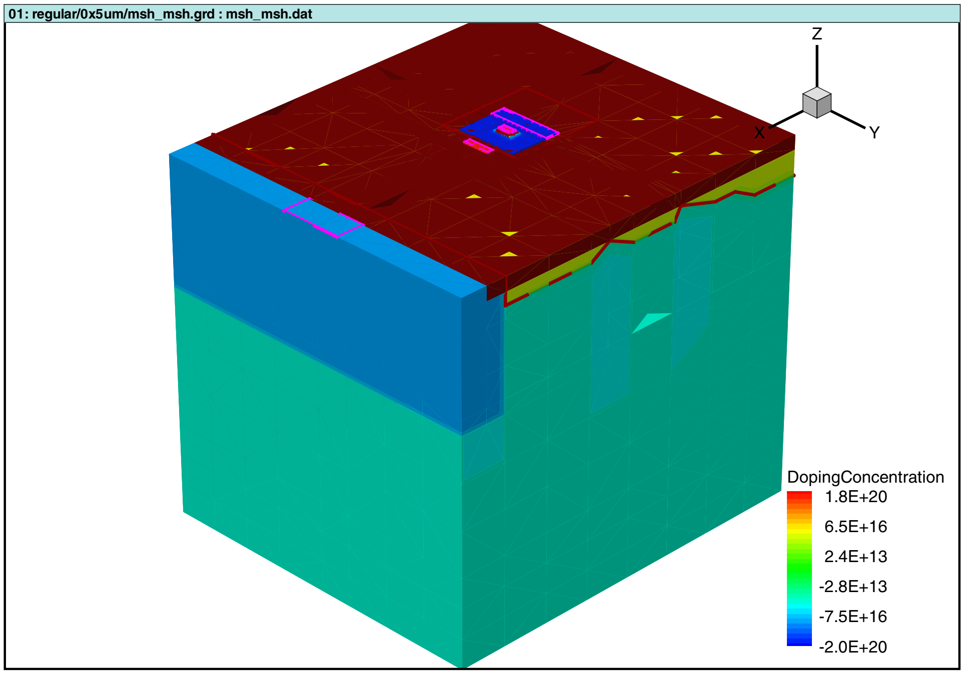


Figure 2.3: A 3-D HBT device constructed using MESH.

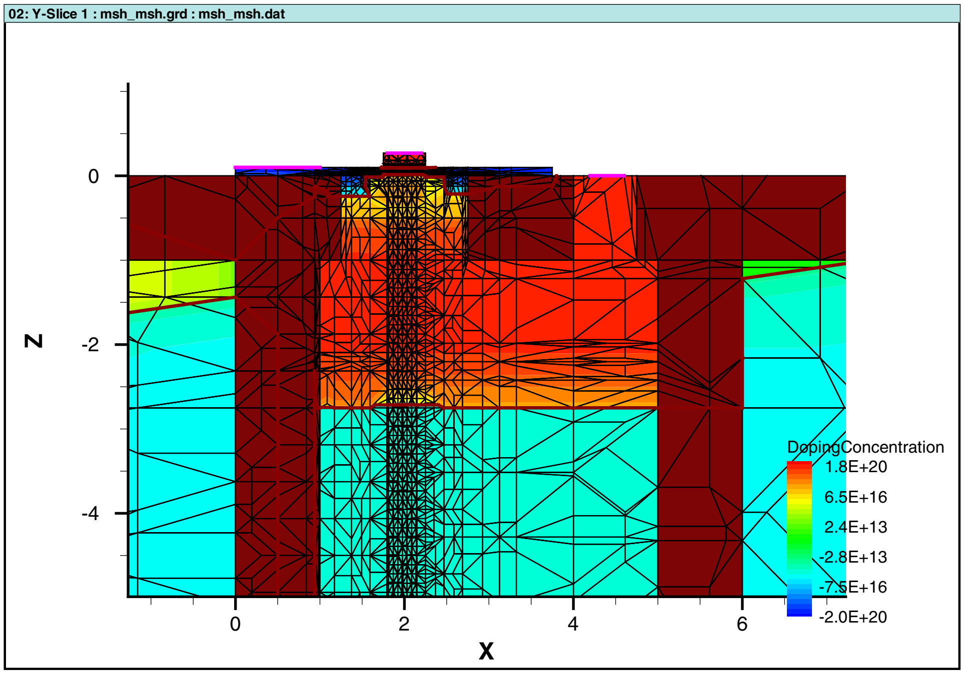


Figure 2.4: 2-D Cross section of the meshed HBT device for emitter center ion strike SET simulation.

2.1.3 Charge Collection Mechanisms

Device-level SEE simulation is significantly more complicated than dc or ac simulation, since the *n-p-n-p* multi-layer structure makes the charge collection more complicated than in a *n-p-n* bipolar structure. The charge track is generated using a Gaussian waveform, with an $1/e$ characteristic time scale of 2 picosecond and an $1/e$ characteristic radius of 0.1 μm. The peak of the Gaussian occurs at 6 picoseconds [18] [3]. For deep ion strike simulation, the depth of the charge track is 25 μm, with a uniform LET value along the charge track. Unless specified, the charge track is located at the emitter center, with a uniform LET=0.037 pC/μm (3.6 MeV·cm^2/mg). Physical TCAD models including the Philips unified mobility model, the Slotboom bandgap narrowing model, the high field velocity saturation model, and the Shockley-Read-Hall (SRH) and Auger recombination models, are activated for these DESSIS 3-D simulations [43].

The SiGe HBT is unloaded, with zero biasing voltages at collector, emitter, and base. The CS junction is reverse biased at -4 V. Fig. 2.5 and Fig. 2.6 show the transient currents and the integral charge collected at each terminal versus time in log and linear scale. Note that the linear plots are just for the first 5 nanoseconds, which is the time period when drift charge collection dominates as detailed below. The positive direction of currents is defined as entering the terminals. The positive emitter and collector currents indicate that during the SET process the collector and emitter collect electrons, while the negative base and substrate currents indicates that the base and substrate collect holes.

The deposited charge is initially collected from the depletion layer mainly through drift over a very short time span (hundreds of picoseconds), causing a pulse like shape for currents at the four terminals, as shown in Fig. 2.5 (a). Therefore, significant drift charge collection occurs in reverse-biased junctions, e.g. CS junction, due to the high electric field [40]. Fig. 2.5 (b) indicates that CS junction collects 0.5 pC drift charge, while the other junctions collect less than 0.1 pC drift charge. Charge deposited deep in the substrate diffuses towards the CS space charge region (SCR). Those that encounter the electric field are collected via drift, and generate currents on the collector and substrate contacts. This diffusion process lasts for several microseconds, with very low charge collection rate. The peak collector drift current is around 1.8 mA, while the collector diffusion current is less than 0.5μA.

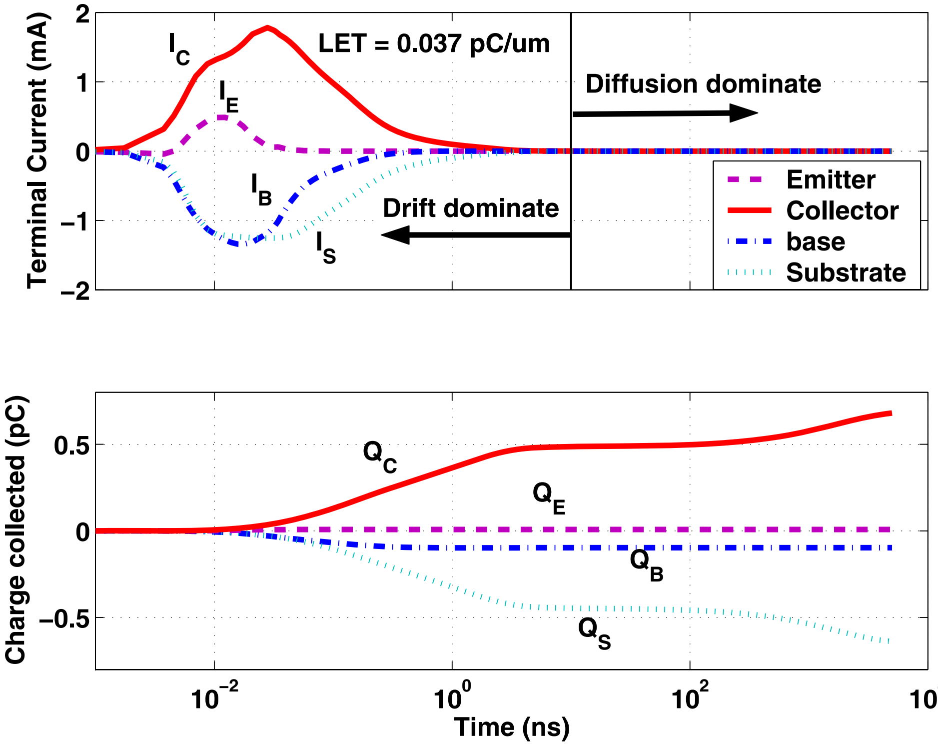


Figure 2.5: Terminal currents and integrated charges from DESSIS SET simulation.

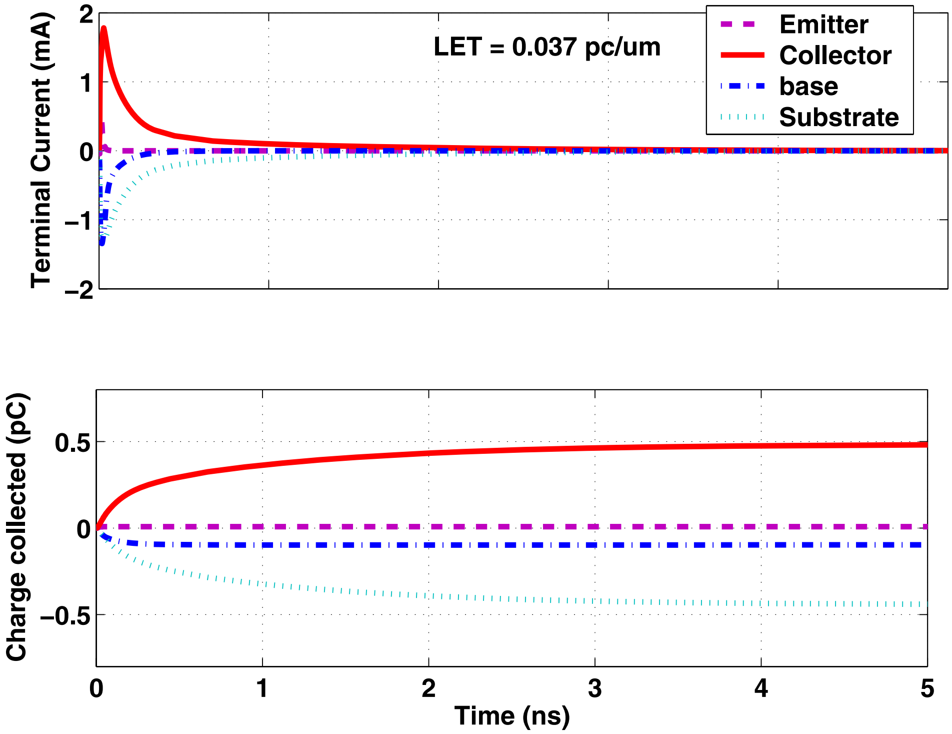


Figure 2.6: Terminal Current and charge from DESSIS transient simulation in linear scale.

To reduce the SEE introduced charge collection, transistor-level hardening techniques have been developed. These device hardening techniques focus on reducing CS junction charge collection, such as back junction [44], dummy collector [3], silicon-on-insulator (SOI) technology [45]. The actual effect of the dummy collector on charge collection will be examined in Section 2.2.2

2.1.4 SEE Current Modeling

Under certain conditions, the ion-induced transient currents can propagate away from the struck device and cause SEU at the circuit output. To study the impact of the transient currents in a circuit, these currents are frequently modeled as current sources at the struck transistor [46] [47] [48] [49].

Fig. 2.7 (a) shows the four-current-source model that includes all possible charge collection processes in a SiGe HBT. i_{eb} is the SEE induced EB junction charge collection current. i_{cb} is the SEE induced CB junction charge collection current. Compared with i_{cb}, i_{eb} is small due to the thin EB depletion layer thickness. The base terminal current is mainly i_{cb}. i_{cs} represents the SEE induced CS junction charge collection current. The substrate current is mainly i_{cs}, which is the most significant part among all ion-induced currents based on the reason introduced in Section 2.1.3. i_{ce} comes from ion track shunt effect, which will lead to negative emitter current if it dominates. The positive emitter current in Fig. 2.5 suggests that i_{ce} is negligible compared to the other three current sources in this work [47] [50]. The collector current is thus the sum of i_{cb} and i_{cs}, while the emitter current is mainly i_{eb}. Comparison of base and collector collected charge in Fig. 2.5 (b) suggests that much less charge is collected through base than collector. However, this small amount of charge can produce circuit SEU effectively, as will be shown in Section 4.3.

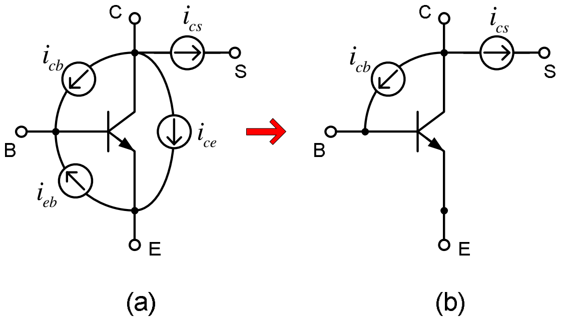


Figure 2.7: Illustration of ion-induced current sources in a SiGe HBT and a simplified model used for circuit simulations.

Fig. 2.7 (b) shows the simplified two-current-source model. i_{eb} and i_{ce} are removed due to their small current level and the small amount of charge collected. The simplified model makes it easier to determine the value of the current sources. From Fig. 2.7 (b), i_{cb} is equal to the simulated base current, and i_{cs} is calculated as the difference of simulated collector and base currents. Our simulation results indicate that with only i_{cb} and i_{cs}, it is sufficient to investigate the influence of ion-induced currents on circuit response. i_{cb} and i_{cs} include both drift and diffusion currents. i_{cb} is primarily drift dominated, while i_{cs} has a diffusion component for a typical deep strike.

2.2 Transistor-level Hardening

2.2.1 Hardening Techniques

There are approaches for mitigating the effects of radiation at all levels of hierarchy from the fabrication process and circuit design, to the system configuration and software levels. Various radiation hardening by design (RHBD) techniques have been published recently, including transistor-level hardening [44] [51] [3] [9], and circuit-level hardening [52] [53].

Transistor-level hardening approaches mainly focus on reducing CS junction charge collection through different techniques, such as a back junction, an SOI process or a dummy collector. A back junction approach is realized by adding another n^+ layer below the *p*-type substrate, which shares part of CS junction charge collection [44]. SOI technology removes the CS junction by fabricating a buried oxide to insulate n^+ buried layer and *p*-type substrate [45]. However, both of the two techniques require process changes, which may lead to extra cost in fabrication. The dummy collector is built by extending the n^+ buried layer (NS layer) outside the DT. This added *pn* junction is more reverse biased than the intrinsic CS *pn* junction, and can effectively reduce

CS diffusion charge collection without any process modification [3]. Simulation results of dummy collector hardened HBT will be shown in the following section.

2.2.2 Dummy Collector Hardening

Fig. 2.8 and Fig. 2.9 show the top view and 2-D cross section view of a dummy collector hardened SiGe HBT. Compared with the regular SiGe HBT in Fig. 2.1 and Fig. 2.2, the dummy collector hardened HBT simply extends the NS layer outside the DT. Fig. 2.10 shows the 3-D structure of the hardened HBT using MESH, while Fig. 2.11 shows the 2-D cross section at y=0. The dummy collector is biased at +3 V unless specified. The area of the added PN junction is much larger than the CS junction, and the junction is more reverse biased than the CS junction. As a consequence, the added *pn* junction should be able to collect deposited charge easier and faster.

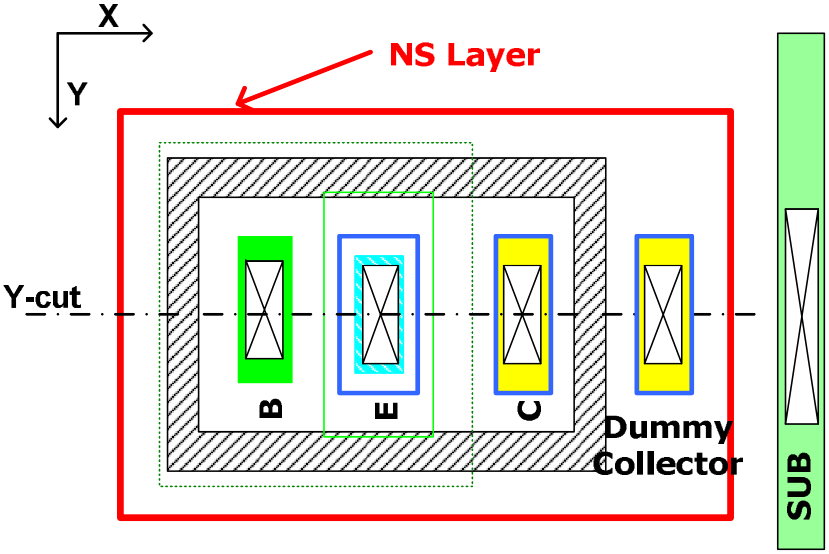


Figure 2.8: Top view for a dummy collector hardened HBT device

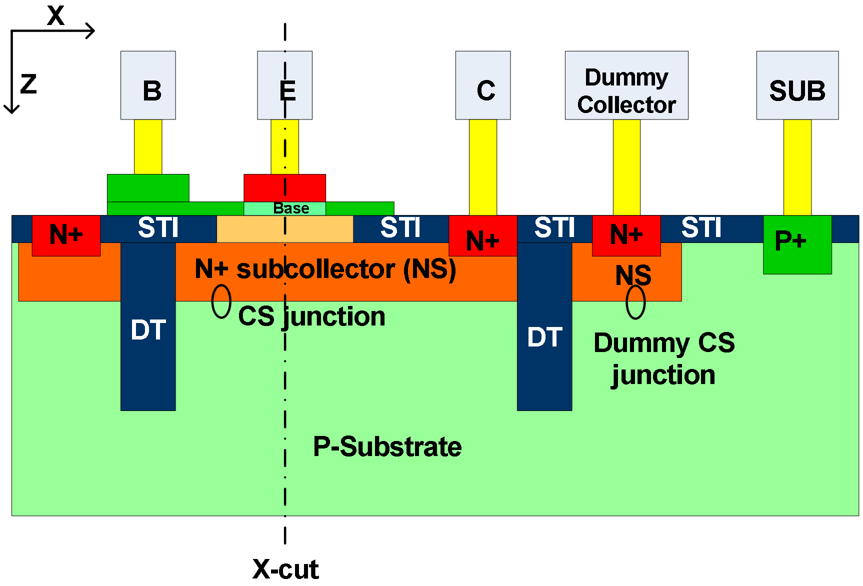


Figure 2.9: 2-D Cross section for a dummy collector hardened HBT device

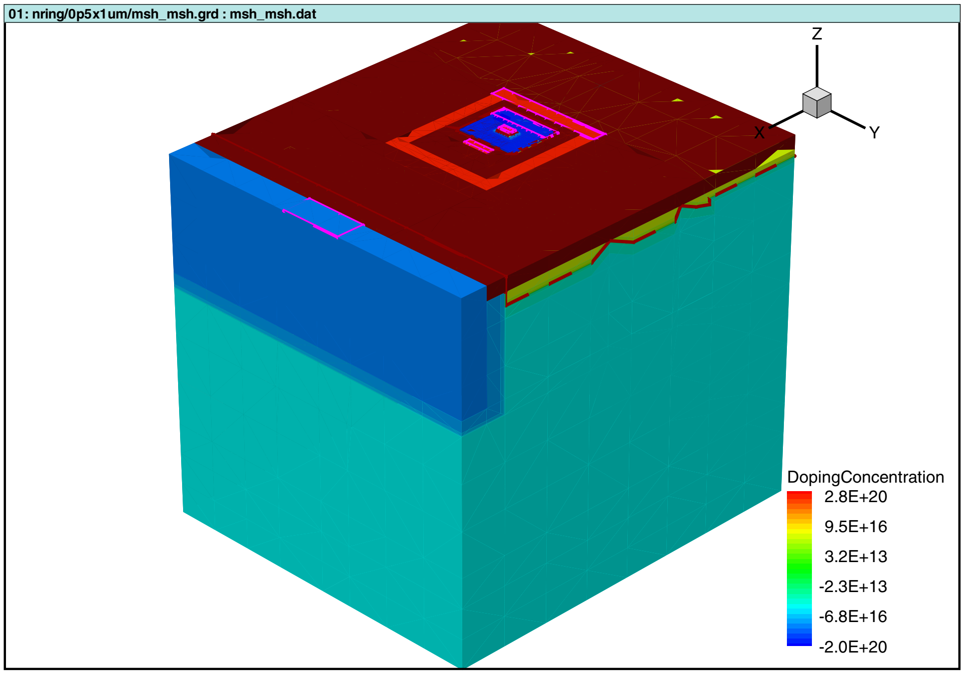


Figure 2.10: A HBT hardened device with dummy collector constructed using MESH .

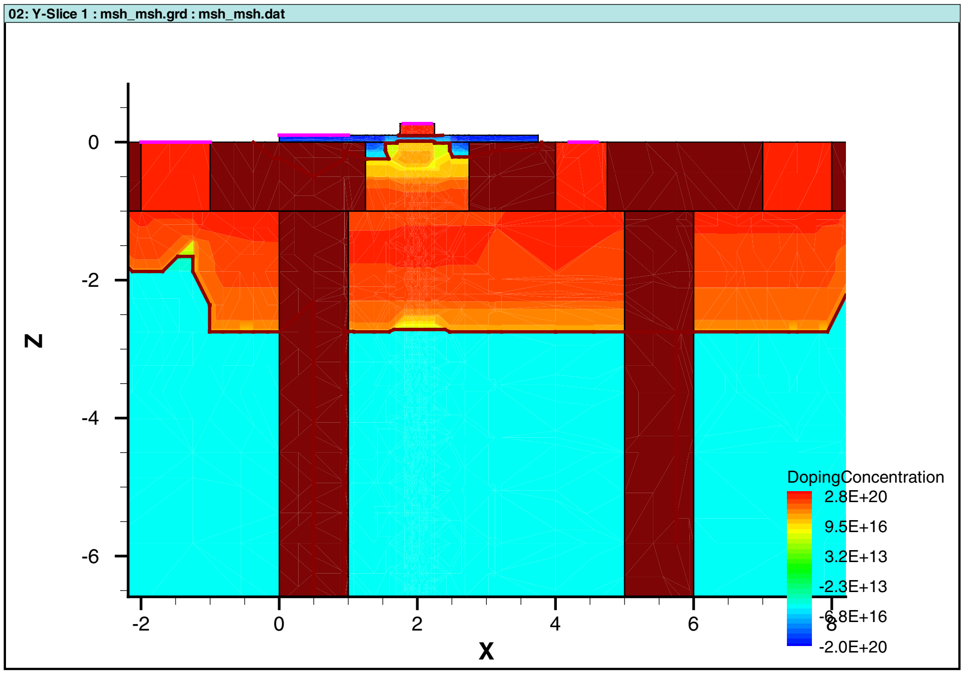


Figure 2.11: 2-D cross section of a HBT hardened device.

Fig. 2.12 shows the terminals currents and the integral charges versus time in log scale. The two devices are constructed with identical geometries and doping profiles, except the area of NS layer, and simulated under the same conditions, including charge track properties, biasing voltages, etc. For emitter center deep strike, the deposited charge is isolated from the added *pn* junction by DT. Therefore, drift charge collections are approximately the same for regular and hardened HBTs. After drift charge saturates, the charges left in the substrate start to diffuse outward towards the added *pn* junction instead of the intrinsic CS junction, which significantly reduces CS junction diffusion charge collection.

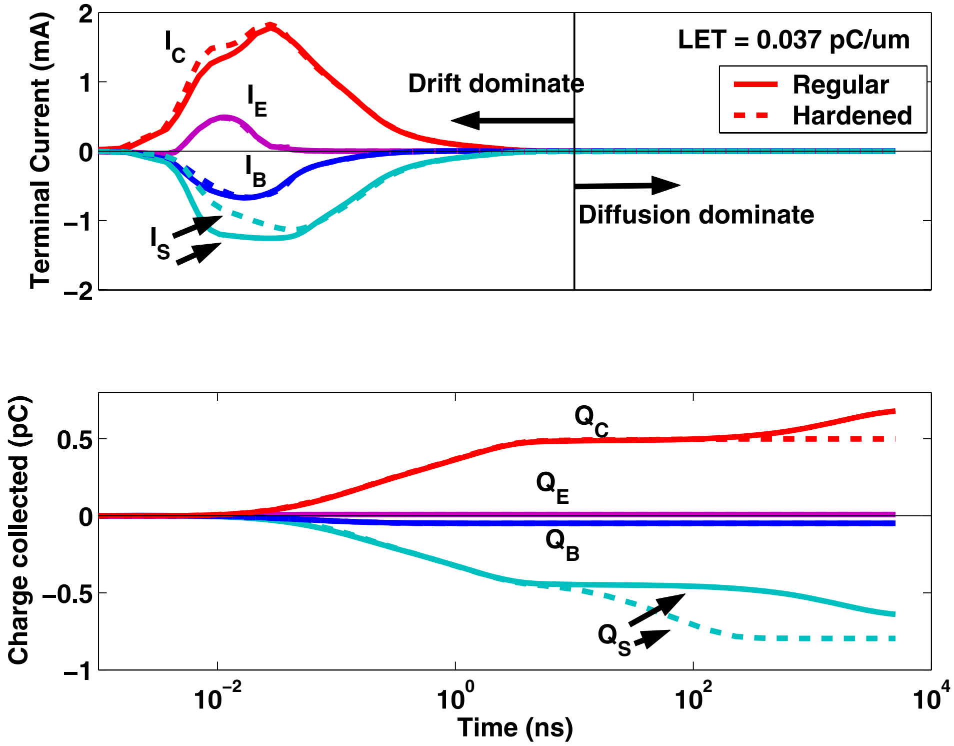


Figure 2.12: The terminal Currents and the integral charges versus time in log scale for regular and dummy collector hardened HBT.

Fabrication of dummy collector is done with a few layout changes. Devices are apart by several microns due to design rules, density requirement and other practical reasons. The unused silicon between the neighbouring devices can be utilized to create the dummy collector. Since multiple HBTs in a circuit can share the same dummy collector, the added dummy collector does not really suffer area penalty. Although the dummy collector can effectively reduce total collector charge collected, its impact on circuit SEU needs further investigation. Chapter 4 examines the impact of dummy collector hardening on DFF circuit. Note that the results cannot be generalized to all circuits as the tight coupling between device and circuit determines the circuit response to ion strike on a single device.

2.3 Conclusion

A regular SiGe HBT is constructed and simulated under an emitter center deep ion strike. The deposited charges are collected through drift and diffusion. Drift charge collection is fast and dominates at the first several nanoseconds, while diffusion charge collection is much slower and lasts for several microseconds. The total amount of diffusion charge is comparable to that of drift charge. The reverse biased CS junction collects most of the charges. Dummy collector hardening technique is shown to be effective in reducing total collector charge by reducing diffusion charge collection.

CHAPTER 3

CIRCUIT SEU SIMULATION APPROACHES

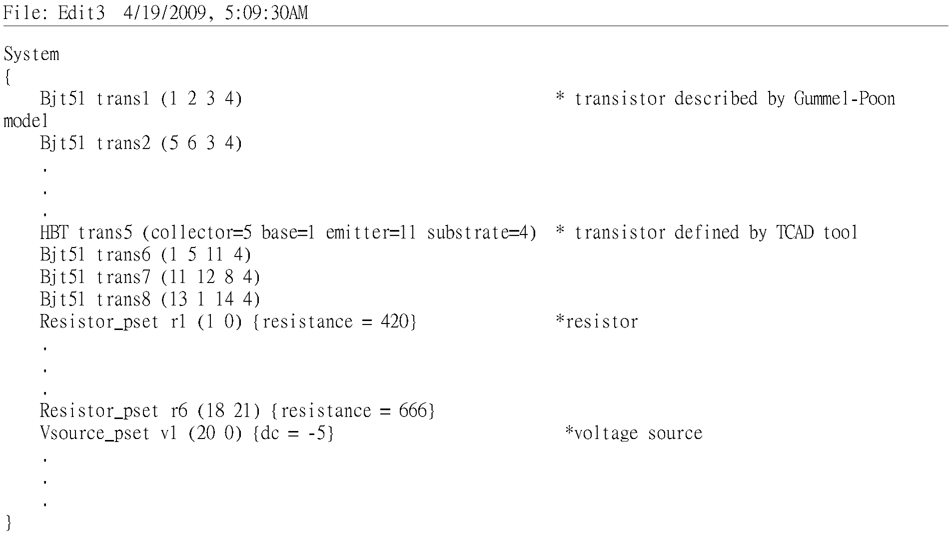
Fabricated SiGe HBTs are inherently robust to various types of ionizing radiation, in terms of both their dc and ac electrical characteristics [18]. However, high-speed SiGe HBT digital logic circuits were found to be vulnerable to SEU at even low LET values recently [5] [54]. In addition, successfully employed III-V HBT circuit-level hardening schemes were found to be ineffective for these SiGe HBT logic circuits. To help understanding these SEU results, and to aid in the search for effective SEU mitigation approaches, mixed mode circuit simulations are required. Two kinds of circuit simulation approaches are normally used. One is done in DESSIS, namely true mixed mode. The other combines device simulation in DESSIS and circuit simulation in Cadence, namely combined mixed mode. Both of the approaches are detailed below, and the simulated results are compared.

This chapter compares the results obtained from a combined mixed mode simulation and a true mixed mode simulation for a master-slave DFF. True mixed mode simulations are performed on analog emitter follower circuits, as will be shown in Chapter 5. In the analog emitter follower circuit the collector is at the supply potential while the emitter is at a lower potential. There is a shunt of the collector and the emitter terminal. The collector to emitter shunt current is complex due to the device/circuit interactions. Mixed mode simulations can capture the device/circuit interactions better. The mixed mode simulation neglects charge sharing when multiple devices are present.

3.1 True Mixed Mode Simulation

DESSIS mixed mode simulation describes the struck transistor using 3-D device model, while the rest of the transistors using SPICE like compact models. The device and circuit equations are solved simultaneously with continuous boundary conditions at the contacts.

The code in Fig. 3.1 shows an example circuit system with one 3-D HBT and several elements using compact models. The codes in the brackets after keyword "system" are used to describe the circuit elements and connection. The transistors defined by "BJT51" are described using Gummel-Poon (GP) model. The parameters for the GP model are transformed from the VBIC model in Cadence with corresponding design kit. The transistor defined by "HBT" is the 3-D HBT device constructed using MESH in Section 2.1.2. The numbers that follow the elements are node numbers, which represent the electric connection of the circuit.



```
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System
{
    Bjt51 trans1 (1 2 3 4)                               * transistor described by Gummel-Poon 
model
    Bjt51 trans2 (5 6 3 4)
    .
    .
    .
    HBT trans5 (collector=5 base=1 emitter=11 substrate=4)  * transistor defined by TCAD tool
    Bjt51 trans6 (1 5 11 4)
    Bjt51 trans7 (11 12 8 4)
    Bjt51 trans8 (13 1 14 4)
    Resistor_pset r1 (1 0) {resistance = 420}            *resistor
    .
    .
    .
    Resistor_pset r6 (18 21) {resistance = 666}
    Vsource_pset v1 (20 0) {dc = -5}                      *voltage source
    .
    .
    .
}
```

Figure 3.1: Example codes in DESSIS for mixed mode simulation.

Since all of the circuit elements are involved self consistently, the true mixed mode simulation is more accurate than the combined mixed mode. However, it is extremely time consuming. If there are a bunch of such simulations that need to be run, resource availability is a challenge. Furthermore, DESSIS supports only netlist description of circuit, making it difficult to describe large scale circuits. Circuit connection errors, which may lead to unphysical results, are hard to diagnose. Based on the reasons described above, in many cases, the combined mixed mode simulation is favorable, as described below.

3.2 Combined Mixed Mode Simulation

Although the true mixed mode in DESSIS provides accurate SEU prediction, advanced transistor models used by circuit designers are not supported by DESSIS currently, making true mixed mode simulation less attractive in practice. An alternative and popular methodology, namely combined mixed mode, is to simulate the SEE induced transient terminal currents using DESSIS, and then use the equivalent circuit in Section 2.1.4 in a conventional circuit simulator with advanced transistor model capability, e.g. Cadence Spectre in this work [42]. One strength of this approach is the large scale of the circuit that can be modeled. Another is its computational efficiency.

In principle, any transistor in the modeled circuit can be hit by a heavy ion. The biasing and loading conditions of the transistors are quite different from each other. If the transient currents are based on device simulations of a struck unloaded device, the circuit simulation inherits the inaccuracy of device simulation. In practice, however, it is generally easy to identify the sensitive transistors and concentrate the analysis on those devices.

Fig. 3.2 shows an example for loading the transient currents into Cadence. Transistor Q3 is chosen as the struck transistor and I_{CB}, I_{CS} are the two current sources representing charge collection currents at CB and CS junctions. The current sources use the data files extracted from DESSIS 3-D device simulation as input files.

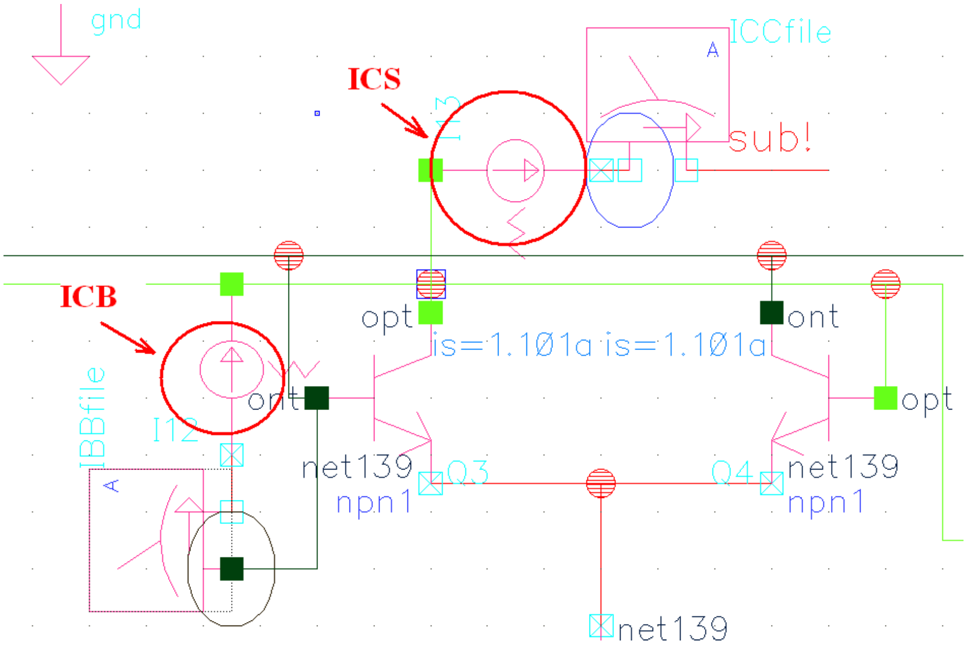

Figure 3.2: An example of load SEE current source into circuit.

Another advantage of combined mixed mode simulation is that I_{CB} and I_{CS} can be manually scaled to examine the LET dependence of circuit SEU qualitatively. Also, the sensitive transistor can be easily determined by simply applying I_{CB} and I_{CS} to different transistors. In qualitative analysis, I_{CB} and I_{CS} can be modified manually. Meanwhile by varying the turn on time of I_{CB} and I_{CS}, the clock and data point dependence of digital circuit SEU can be explored. For any of the strategy above, it takes only a few seconds in Cadence. Compared to each simulation taking one or two weeks in DESSIS, it is more convenient and computationally efficient. A natural question of practical importance is how the simulation results from true mixed mode and combined mixed mode compare with each other, which we address next in Section 3.3 for a CML circuit, a DFF.

3.3 Simulation Results

Fig. 4.1 shows the schematic of a master-slave DFF. Simulations using true mixed mode and combined mixed mode simulation are compared. In principle, any of the transistors can be struck at any time. The two simulations compared here have Q3 struck at 3 nanosecond, which is a representative worst case as detailed in Section 4.1 In true mixed mode, Q3 is modeled in 3-D device domain, and the other transistors are modeled using GP model, e.g. "HBT" and "BJT51" in Fig. 3.1 respectively. The ion strike hits Q3 at 3 nanosecond. In combined mixed mode, current sources are added to the terminals of Q3 as shown in Fig. 3.2. The values of the current sources are calculated from base and collector transient currents using 3-D device simulation. These current sources are turned on at 3 nanosecond.

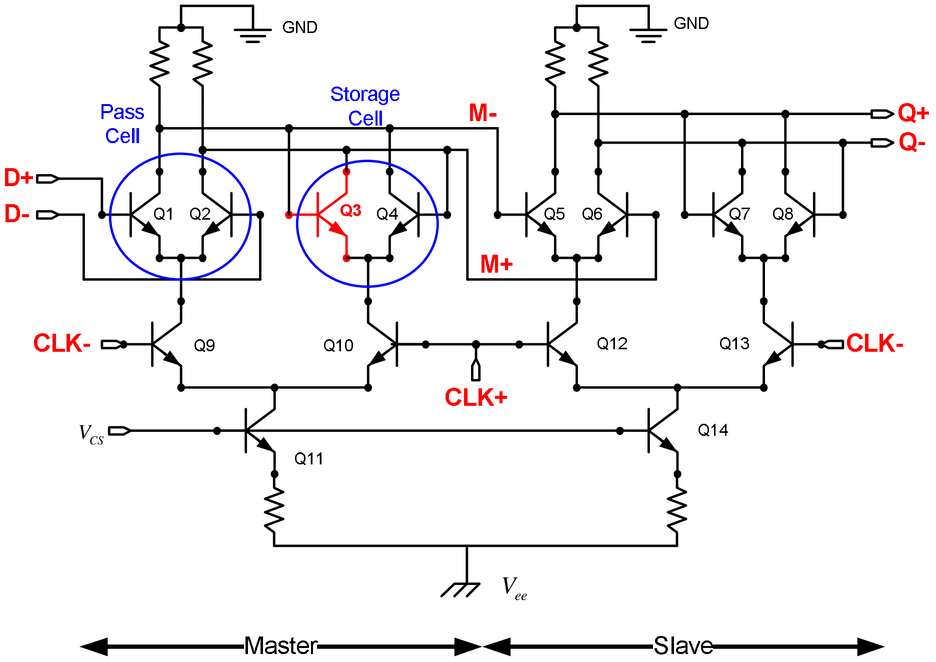

Figure 3.3: Schematic of a master-slave DFF.

Fig. 3.4 compares the circuit outputs from true mixed mode simulation and combined mixed mode simulation for the circuit. Waveform Q+ represents the circuit positive output and $\Delta M = (M+)-(M-)$ represents the differential voltage on the storage stage. The two types of simulations produce similar output waveforms. That is, for certain circuit SEU analysis, e.g. DFF, combined mixed mode simulation is sufficient, which will be applied on mechanism and regional analysis of DFF circuit SEU analysis in Chapter 4.

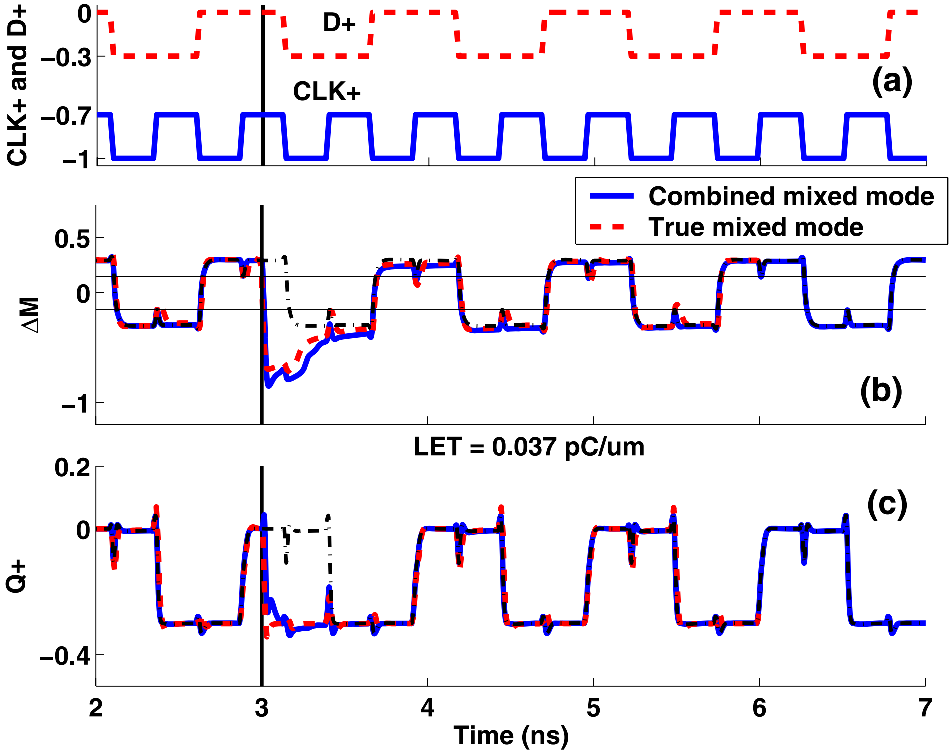

Figure 3.4: Comparison between true mixed mode output and combined mixed mode output for a DFF.

3.4 Conclusion

The advantages and disadvantages of two types of mixed mode simulation are introduced and discussed. The true mixed mode simulation using DESSIS solves device and circuit equations simultaneously, which considers the interaction between the struck device and the left of the circuit naturally. This type of mixed mode simulation is accurate but time consuming as well as difficult to realize. The combined mixed mode simulation models SEE of the struck device using current sources, which can be easily applied on large scale circuits, and provides qualitatively accurate simulation results. The simulation results from the two types of mixed mode simulations are compared for an example circuit, a master-slave DFF. For the circuit examined, combined mixed mode is sufficient for circuit SEU analysis.

CHAPTER 4

MECHANISMS OF SINGLE EVENT UPSET IN DFF

SiGe HBTs are robust to various types of ionizing radiation, but can be susceptible to SEU [55] [49]. At present, the SEU sensitivity is primarily attributed to the high resistivity or lightly doped substrate, and the associated large amount of both drift and diffusion charge collected by the collector through the reverse biased CS junction [46]. As a result, transistor-level hardening has focused on reducing CS junction charge collection, including the use of a dummy collector placed outside the DT isolation [3] [9], or removal of the CS junction using an SOI substrate [45]. Experimentally, transistor-level SEU sensitivity has been primarily characterized using the total amount of collector charge collected during an ion strike as a figure-of-merit [8] [9]. This, however, may not be accurate, as the CB junction charge collection current has recently been shown to dominate SEU in emitter followers via circuit action, despite the small collected charge involved [50].

The purpose of this chapter is to examine the difference in SEU of CML circuit, a master-slave DFF here, caused by CB and CS charge collection, respectively. For CS charge collection, we examine the difference in SEU impact between drift and diffusion charge collection. The CS junction diffusion charge is shown to have negligible impact on CML circuit SEU, despite the large amount of charge collected. The CB drift charge collection is shown to be relevant and impose the level of mitigation possible in transistor-level RHBD, (e.g, even in the extreme case of using SOI substrate) despite its small amount of charge collected. An ion track passing through the physical CS junction is found to be more effective in causing SEU than an ion track passing through only CS SCR but not intersecting the junction interface, because of the funneling-induced large current amplitude.

Implications on threshold LET, cross section, angular strike, and device hardening techniques are discussed.

4.1 Technical Approach

The same CML master-slave DFF used in [56] is simulated here. Fig. 4.1 shows the circuit schematic. The switching current is 0.6 mA, and the voltage swing is 300 mV. The input data alternates between '1' and '0' bits at 2 Gbit/s unless otherwise specified.

The simulations are first run using the combined mixed mode simulation in Section 3.2, then verified using the DESSIS mixed mode simulation in Section 3.1 that the conclusions are still valid .

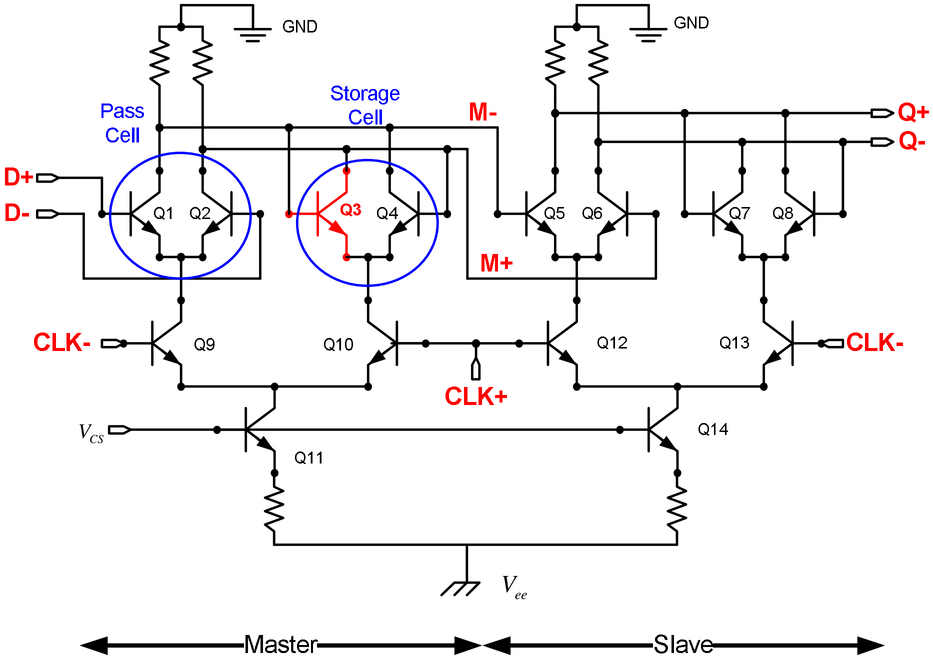

Figure 4.1: Schematic of a master-slave DFF.

The 3-D transistor using in this work is shown as in Chapter 2. In device simulation, the collector, base, and emitter nodes are grounded, and the substrate is held at -4 V. The simulated emitter current is negligible, as EB junction drift charge collection is small due to the narrow depletion layer. The base current is then mainly the CB drift current. The collector current is the sum of CB drift current, CS drift current and CS diffusion current.

To mimic an ion strike, two current sources, I_{CB} and I_{CS}, were placed on the struck transistor, as shown in Fig. 4.2 [46] [47] [48] [49]. Here, I_{CB} and I_{CS} represent the ion strike induced charge collection currents at the CB and CS junctions, including both drift and diffusion currents. I_{CB} is primarily drift dominated, while I_{CS} has a diffusion component for a typical deep strike. I_{CB} is approximately equal to the ion-induced base current from 3-D device simulation. I_{CS} is then determined from the difference of simulated collector and base currents.

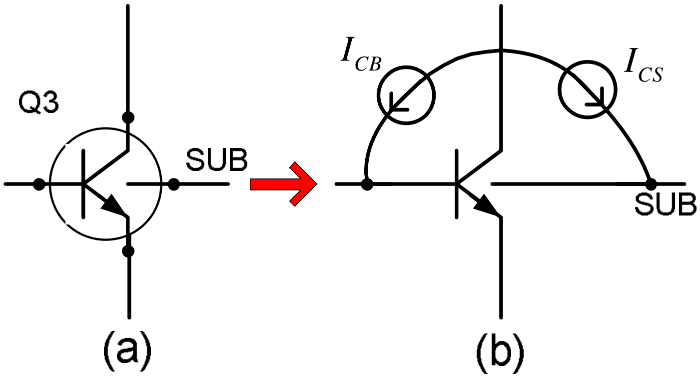

Figure 4.2: The equivalent circuit model used for including the charge collection currents in circuit simulation.

Fig. 4.3 (a) shows a typical I_{CB} and I_{CS} response versus time. Fig. 4.3 (b) shows the corresponding integral charges Q_{CB} and Q_{CS} vs. time curves. Note that the final Q_{CB} is only 0.05 pC, much smaller than 0.6 pC Q_{CS}. However, as we will show below, I_{CB} is important for circuit SEU, despite the small Q_{CB}.

I_{CS} is further separated into a drift and a diffusion component, $I_{\mathrm{CS,drift}}$ and $I_{\mathrm{CS,diff}}$, at the point in time of drift charge saturation, as shown in Fig. 4.3 (a). CS diffusion charge is about 25% of total CS charge collection as $Q_{\mathrm{CS,drift}} = 0.45$ pC, $Q_{\mathrm{CS,diff}} = 0.15$ pC in Fig. 4.3 (b). Observe that $I_{\mathrm{CS,diff}}$ is less than 0.004 mA, despite the large final charge $Q_{\mathrm{CS,diff}}$. This $I_{\mathrm{CS,diff}}$ is much less than typical biasing currents used in CML gates (e.g., 0.6 mA in this work), and thus is not capable of producing circuit upset, as detailed below, even though it may last for several microseconds.

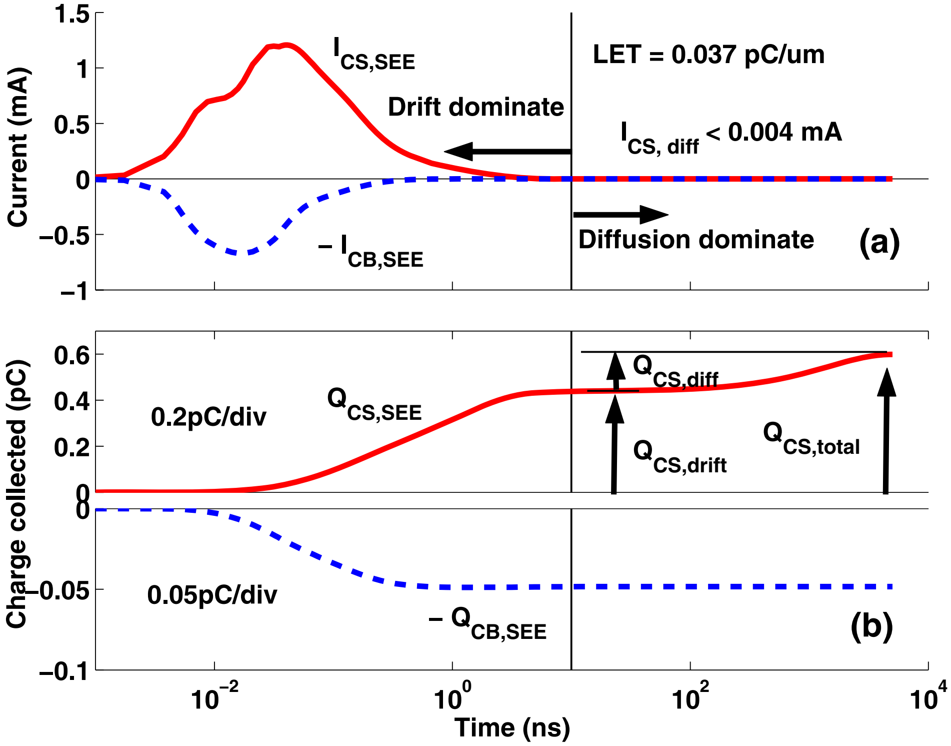

Figure 4.3: The SEE induced CB and CS charge collection currents and the integral charges.

Simulations show that all eight transistors, Q1 to Q8 in Fig. 4.1, are SEU sensitive. Q12, Q13 and Q14 show less SEU sensitivity or higher threshold LET, while Q9, Q10 and Q11 show the least SEU sensitivity. For the discussions below, we will strike Q3 as an example. The excitations are turned on when Q3 is holding a "1" logic state, unless specified, as this represents a worst case for producing SEU.

Fig. 4.4 shows the DFF output waveforms with I_{CS} and I_{CB} added to Q3 and turned on at 3 nanosecond, which is 100 picoseconds after the rising clock edge. Fig. 4.4 (a) shows $\Delta M = (M+) - (M-)$, which is the differential input signal to the slave stage. $Q+$ in Fig. 4.4 (b) is the positive output. Upset is observed at the output.

An upset is also observed when the strike occurs on Q3 when Q3 holds a "0" logic state; that is, when Q3 is turned on. At the ion strike, the collector voltage becomes lower than its normal low, causing its CB junction to be forward-biased and driving the transistor into saturation. When the next "1" bit comes, if Q3 is not able to recover from saturation, the output will continue to show a "0" rather than "1", effectively causing an upset.

4.2 Drift vs. Diffusion Charge Collection

To better evaluate the individual impact of various charge collections mechanisms, different current excitations representing different components of collector charge collection were simulated. Three cases were compared:

1. only drift currents, with I_{CB} and $I_{\text{CS,drift}}$ turned on. Note that I_{CB} is purely drift in origin.
2. with only diffusion current $I_{\text{CS,diff}}$ turned on.
3. both drift and diffusion currents turned on.

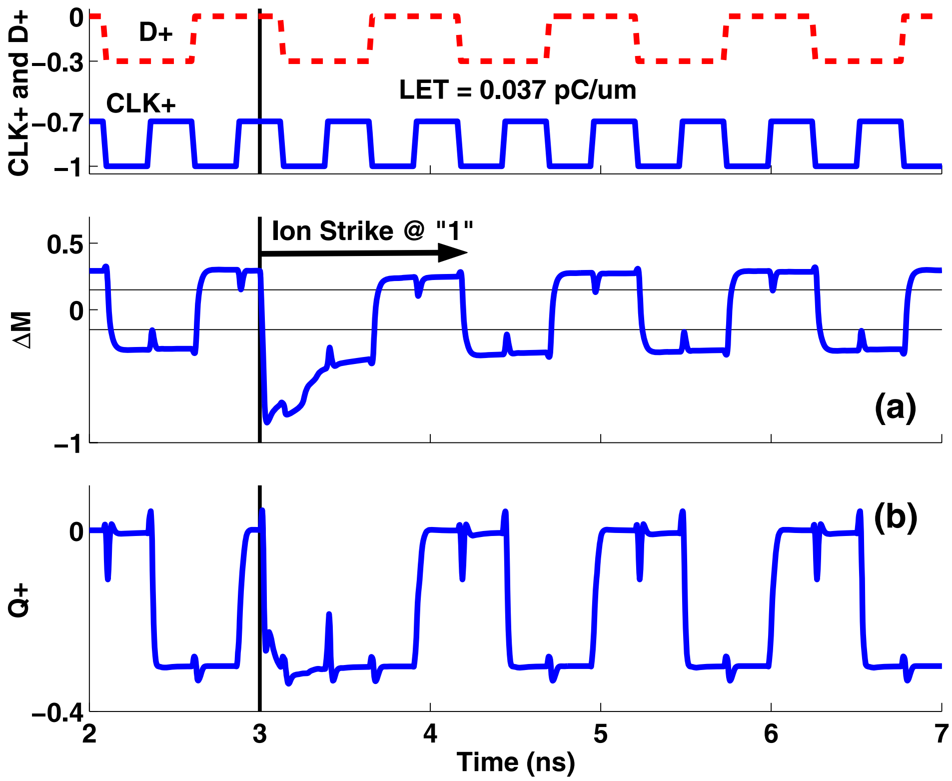

Figure 4.4: Output waveform from transient simulation result for the DFF.

In all cases, the time axis of the original current sources obtained from device simulation was shifted to excite the circuit at the same starting time. The results are shown in Fig. 4.5.

The $Q+$ with all currents is identical to the $Q+$ with drift currents alone, both showing upsets, while the $Q+$ with only diffusion current shows no upset. The actual simulation was performed for tens of microseconds, much longer than the diffusion charge collection time, and no upset was observed. To account for the slow nature of diffusion collection, simulations were also performed with a static clock, which holds the data in the storage cell indefinitely, as in an SRAM. The results are shown in Fig. 4.6. Still, no upset is observed for the $I_{\mathrm{CS,diff}}$ only case. This is attributed to the

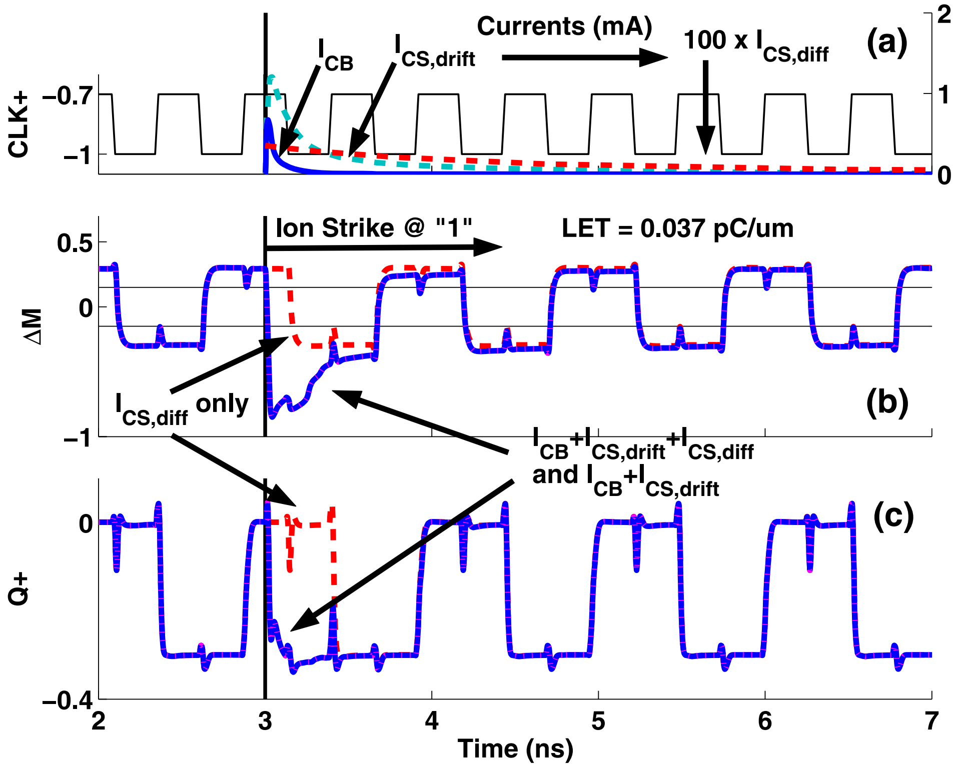

Figure 4.5: Comparison of the simulated ΔM and $Q+$, with drift and diffusion currents activated individually.

current mode operational nature of CML circuits, and the small magnitude of $I_{\mathrm{CS,diff}}$ (.004 mA). Since $I_{\mathrm{CS,diff}}$ is much less than the biasing current, $\Delta V = I_{\mathrm{CS,diff}} R_{\mathrm{C,load}}$ is on the order of 2 mV, much less than the voltage swing. Here $R_{\mathrm{C,load}}$ is the load resistor at the collector of Q3. This small ΔV variation is restored by the circuit itself through cross-coupling between Q3 and Q4, and no upset is produced.

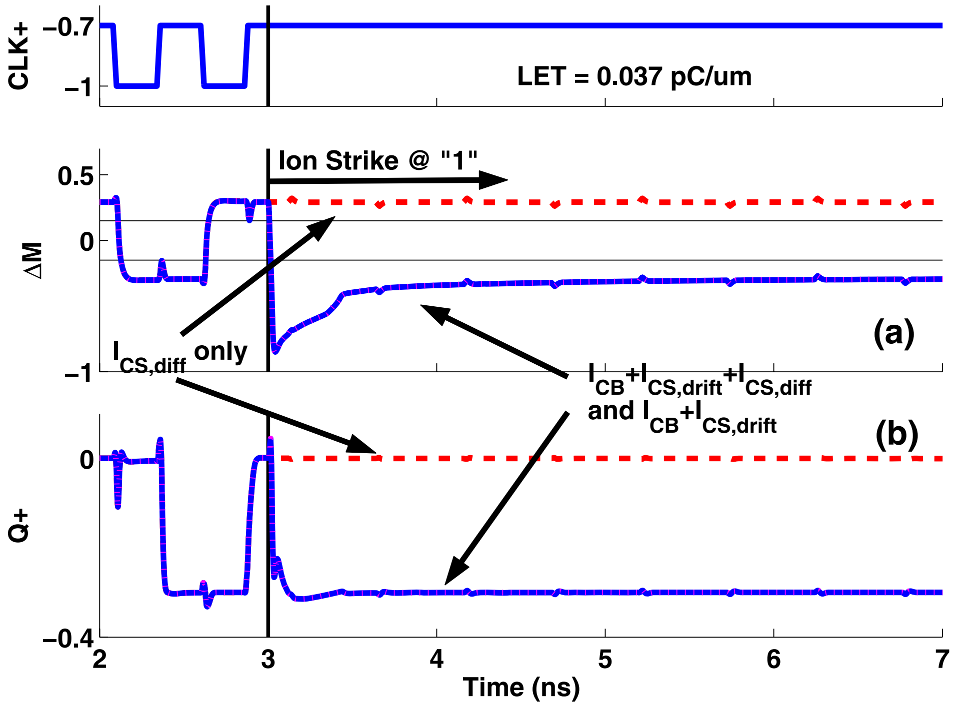

Figure 4.6: Comparison of the simulated ΔM and $Q+$ with drift and diffusion currents activated individually, for a static clock.

4.3 CB Drift Charge vs. CS Drift Charge

For the LET used, Q_{CB} is about one tenth of $Q_{CS,drift}$. However, its impact on circuit SEU is much stronger than the charge magnitude might suggest, because I_{CB} appears in the feedback path between collector and base, where it is amplified by the transistor. This directly raises the base voltage and indirectly increases the collector current, which exponentially depends on base-emitter voltage. The process is further enhanced by the cross-coupling of Q3 and Q4. Fig. 4.7 (b) and (c) compare ΔM and $Q+$ from simulations with I_{CB} and $I_{\text{CS,drift}}$ activated individually. Both I_{CB} and $I_{\text{CS,drift}}$ cause circuit upset. I_{CB} is actually "more effective" than I_{CS}, since only very little Q_{CB} is necessary to produce SEU.

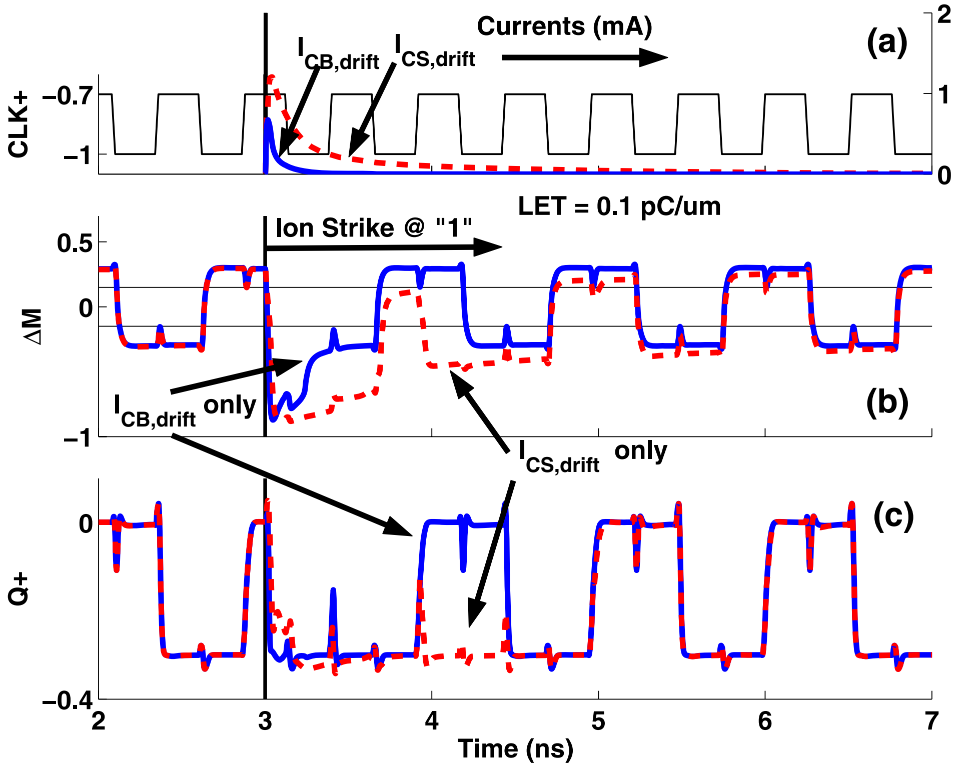

Figure 4.7: Comparison of the simulated ΔM and $Q+$ with CB and CS drift currents activated individually.

4.4 Regional Charge Collection Analysis

A more elaborate approach to study the different charge collection mechanisms is by using selective ion track placement in different regions of the SiGe HBT. Simulations were performed for the following ion track placement:

1. Ion track is placed only in the EB and CB junctions. This should produce primarily CB drift current.

2. Ion track is placed only in the CS junction. This should produce CS drift and diffusion currents.
3. Ion track is placed below the CS junction, but through part of its SCR. This should produce CS drift and diffusion currents. The difference from the previous case, however, is that the ion track does *not* pass through the junction interface.
4. Ion track is placed well below the CS SCR. This should produce only CS diffusion current.

All of these cases are compared with placing the ion track through the whole device. A schematic illustration is given in Fig. 4.8.

Fig. 4.9 (a) and (b) show the simulated I_{CB}, I_{CS} and the corresponding integral charge versus time, respectively. The results are close to our expectations. I_{CB} is produced only in the two placements that traverse the CB junction, and I_{CB} is primarily caused by drift. The ion track that passes the CS junction only produces only CS drift and diffusion charge collection. The ion track passing through part of CS SCR produces less drift current and charge, but about the same total collected charge. The ion track placed below the CS SCR causes only CS diffusion charge collection, and no drift charge collection, as expected.

Fig. 4.10 compares the circuit output waveforms. There is no upset when the ion track passes part of CS SCR or below CS SCR. In all other cases, upset is observed. It is worth noting that the ion strike passing part of CS SCR produces 0.25 pC of drift charge, which is significant. However, the overall current magnitude is much less compared to the strike passing through CS junction, as can be seen from Fig. 4.9. The I_{CS} peak is above 1 mA when the ion track passes through CS junction, and below 0.2 mA when the ion track does not pass through the junction. This current difference, rather than the drift charge difference, is the reason why upset is not observed with a 0.25 pC drift charge, and originates from the fact that the ion track does not pass through the CS junction interface. We will further discuss this in detail below. We will see that a smaller 0.22 pC CS drift charge can actually produce upset when the ion strike passes through the CS junction.

4.5 Threshold LET and the SOI Limit

Fig. 4.11 plots the CS, CB and the total drift charge versus LET for a deep strike at emitter center. When the LET is below 0.02 pC/μm, the relationship between Q_{drift} and LET is linear. The drift current itself is also approximately linear with LET. This provides an excellent way of speeding up the process of determining threshold LET, as one can take 3-D simulation results at one LET and scale the currents continuously with LET so that threshold LET can be determined by only re-running circuit simulation (not device TCAD). The process can be automated through a parametric sweep in circuit simulators. At higher LET, the linear relationship becomes less valid.

Also shown in Fig. 4.11 are the threshold LET, defined as the LET at which upset starts to be observed, and the corresponding drift charge for three cases: 1) $I_{\text{CB,drift}}$ only, $Q_{\text{drift}} = 0.025$ pC, $LET_{\text{threshold}} = 0.02$ pC/μm. 2) $I_{\text{CS,drift}}$ only, $Q_{\text{drift}} = 0.22$ pC, $LET_{\text{threshold}} = 0.02$ pC/μm. 3) $I_{\text{CB,drift}}$ and $I_{\text{CS,drift}}$, $Q_{\text{drift}} = 0.0074$ pC, $LET_{\text{threshold}} = 0.008$ pC/μm, that is, 0.8 MeV$\cdot$cm^2/mg. This is consistent with the experimental result of [5] at a similar data rate. In [5], cross sections were appreciable at LET of 1.4 MeV$\cdot$cm^2/mg with C-12. Note that even though $I_{\text{CS,drift}}$ and $I_{\text{CB,drift}}$ give the same threshold LET in Fig. 4.11, this should not be generalized to all technologies.

The I_{CB} only case corresponds to the use of SOI substrate, which eliminates the CS junction. Although SOI can decrease total collector charge by 10 times, the threshold LET, however, shows much less improvement since CB charge collection is more effective. This suggests that the CB charge collection poses a limit to achievable device-level hardening.

4.6 Importance of Junction Passing and Potential Funneling

Note that the CS junction drift charge at a threshold LET of 0.02 pC/μm is 0.22 pC in Fig. 4.11 for the CS drift charge only case. Recall that in the partial passing through the CS SCR case of Fig. 4.9, LET = 0.037 pC/μm, the drift charge is a higher 0.25 pC, but no upset is produced in that case. The main difference is that the overall current is much higher when the ion passes though the CS junction, due to potential funneling.

This result suggests that the drift charge number alone cannot be used as an indicator for CML circuit upset. Whether a strike passes through the junction interface is also very important, as the current magnitude is much larger for junction passing strikes due to potential funneling. Observe that for the junction passing case, LET = 0.02 pC/μm, while for the passing CS SCR case, LET = 0.037 pC/μm. The induced I_{CS} is much larger in the junction passing case, despite a smaller LET. The importance of potential funneling therefore not only lies in the amount of drift charge collected, which is well known, but more importantly, the high rate of charge collection or high drift current. This is particularly the case for CML circuits.

For angular strikes, particularly those at a large angle, some of the ion tracks may not pass the whole CS junction, but only part of CS SCR. An extreme case would be horizontal (parallel to the surface) ion tracks below the CS junction interface. This will certainly reduce the CS drift current compared to a vertical strike.

For smaller angles, the ion track still intersects with the junction, but will suffer from limited potential funneling because of the presence of the DT, and hence reduced drift current magnitude. This should make angular strikes produce less circuit SEU than predictions from traditional sensitive volume theory that only considers charge deposition in a sensitive volume, which could potentially explain the angular dependence data in [5].

4.7 Error Cross Section

From an error cross section standpoint, for a given transistor in the circuit, the sensitive area for a given LET should be a function of both the CB and CS sensitive areas. Fig. 4.12 shows the sensitive areas for CB and CS junction charge collection. The CB junction area is defined by the active area between STIs. The CS junction area is defined by the silicon area enclosed by the DT ring, which is typically over 10 times larger than the CB junction area. The cross section for an LET larger than the threshold LET of $I_{\text{CB,drift}}$ and $I_{\text{CS,drift}}$ case is determined by CB junction area, while the cross section for an LET larger than the threshold LET $I_{\text{CS,drift}}$ only case is determined by CS junction area. The error cross section can thus be reduced by using an SOI substrate, as the ion strike sensitive area is limited to CB junction area. Given the different threshold LET of different transistors, the overall circuit SEU cross section should increase with increasing LET.

4.8 Outside DT Charge Deposition

Experimentally, outside DT deep strikes were shown to produce significant amounts of charge, and were suspected to cause digital circuit SEU [3]. The underlying physical mechanism, however, is the diffusion of charge deposited deep in the substrate. This will only contribute to $I_{\text{CS,diff}}$, but not I_{CB} or $I_{\text{CS,drift}}$, as further verified by selective ion track placement simulations.

According to the new simulation results above, outside DT strikes should not produce SEU in CML circuits. Additional device simulations for outside DT strikes were performed, and the corresponding circuit simulations indeed show no circuit level upset, despite the appreciable amount of final charge collection. This observation significantly affects how SEU sensitive area or cross section should be calculated. The same argument applies to charges deposited outside the DT by angular ion strikes.

4.9 Dummy Collector Hardened SiGe HBT

A dummy collector was proved to be effective in reducing CS junction diffusion charge collection using both device simulation and microbeam testing [3] [9]. As drift charge collection is responsible for SEU, we expect such hardening to be ineffective for CML circuits. Fig. 4.13 (a) and (b) compare I_{CB}, I_{CS}, Q_{CB}, and Q_{CS} for the regular and the hardened HBT. The dummy collector is biased at +3 V. Fig. 4.14 compares ΔM and $Q+$ for circuits using a hardened HBT and regular HBT. No SEU improvement is observed, as expected.

Even though dummy collector does not improve CML circuit SEU, the removal of diffusion current on the order of μA for tens of microseconds can be significant for many analog, mixed-signal and RF circuits. Circuit topology clearly matters.

4.10 Conclusion

The individual contributions of charge collection in the CB and CS junctions to SEU in SiGe HBT CML digital circuits are examined. The voltage change introduced by CS junction diffusion charge collection is negligible compared with the signal voltage swing. Such voltage change is restored through circuit operation, and no SEU is produced. The CS and CB drift charge collections are primarily responsible for CML SEU. The CB drift charge collection is shown to be more effective than CS drift charge collection in producing circuit SEU, and will ultimately set the threshold LET in an SOI process. The dummy collector hardening technique shows no SEU improvement in CML circuits, as it reduces only diffusion charge collection. Using selective ion track placement, we showed that for the same amount of CS drift charge, the ion track that passes through the physical junction is much more effective in causing SEU, due to potential funneling and the resulting high current magnitude. Implications to outside DT charge deposition, angular strike, and dummy collector hardening are discussed.

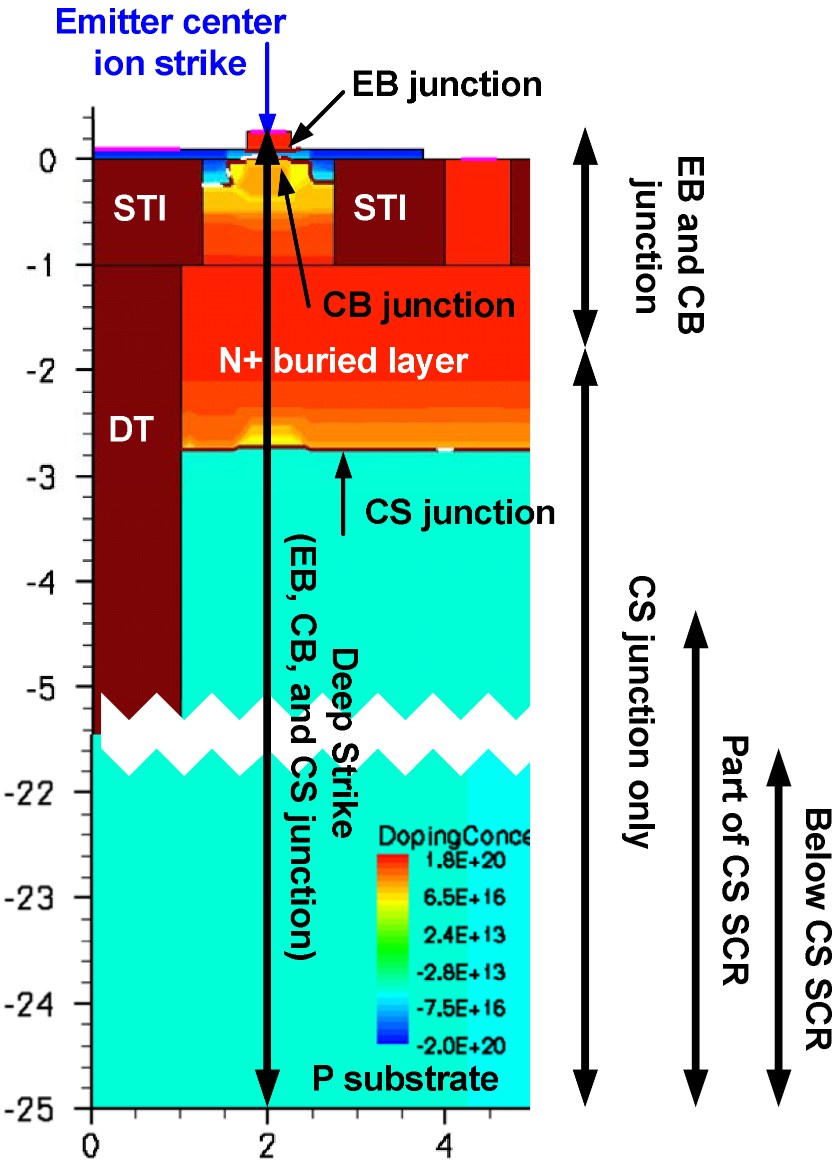

Figure 4.8: Illustration for regional charge collection analysis.

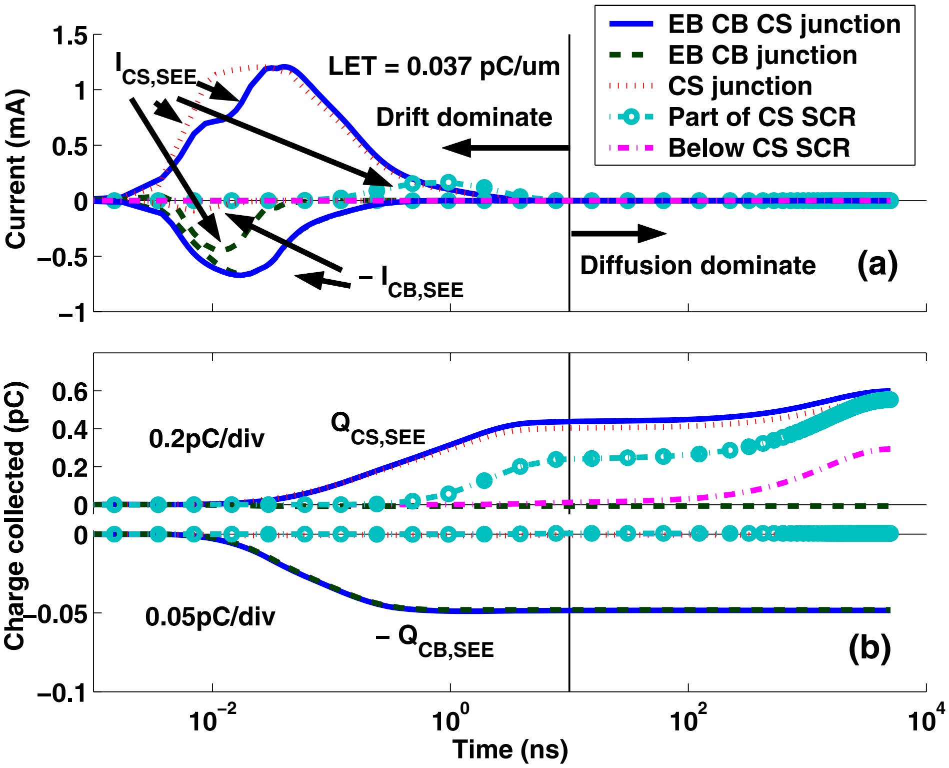

Figure 4.9: Terminal currents and charge for regional charge collection analysis.

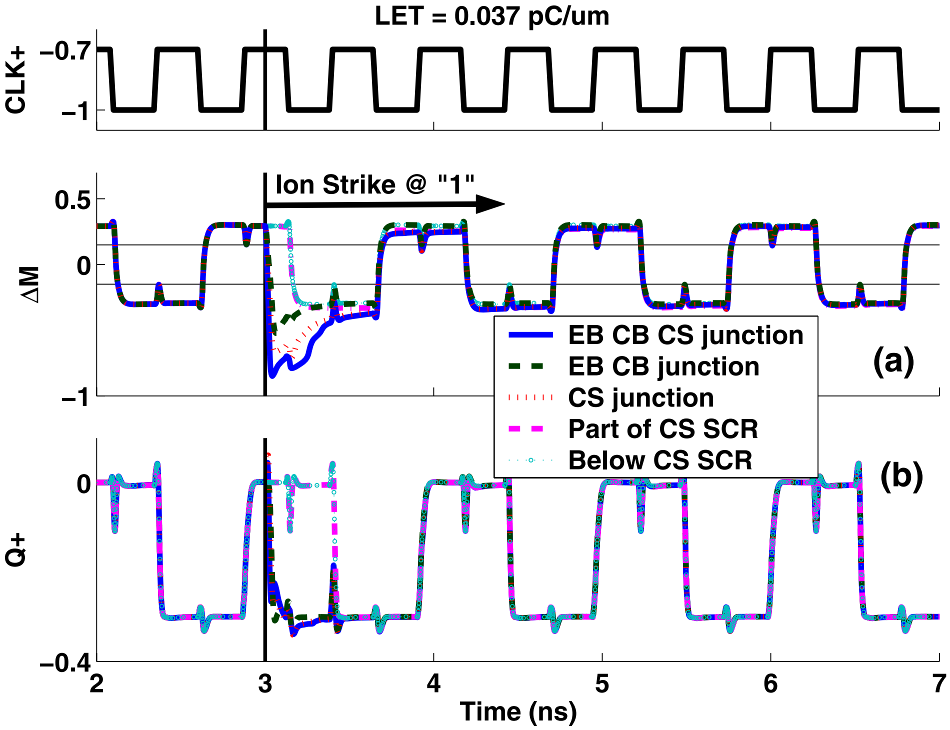

Figure 4.10: Circuit output comparison for regional charge collection analysis.

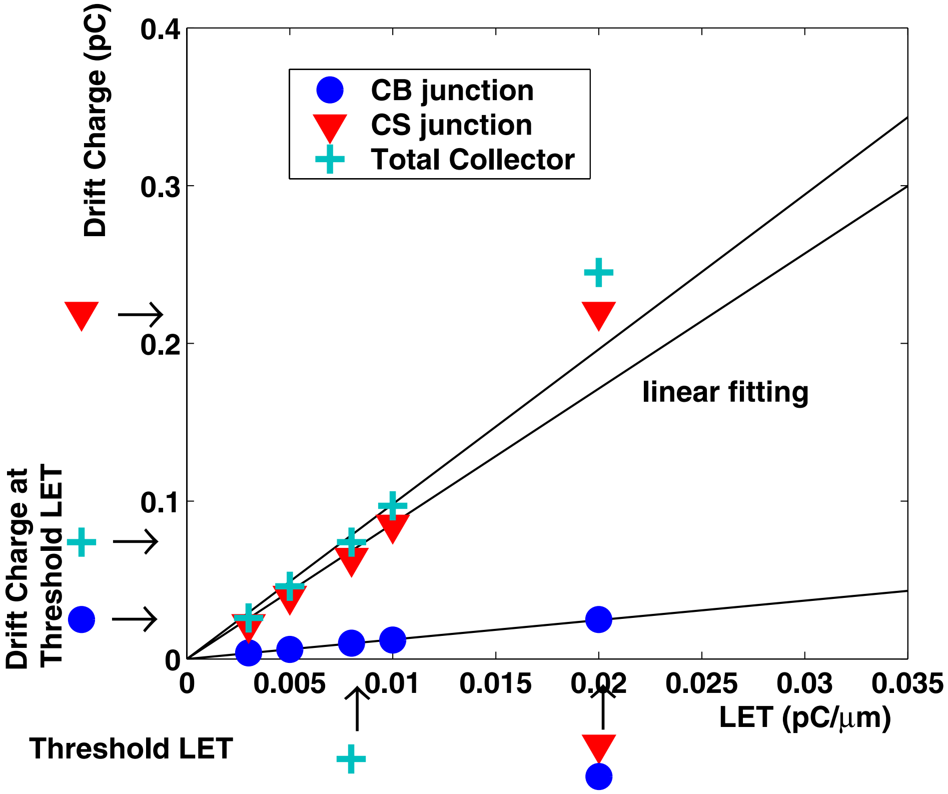

Figure 4.11: The drift charge collected at CB and CS junctions, individually, and the total collector drift charge versus LET.

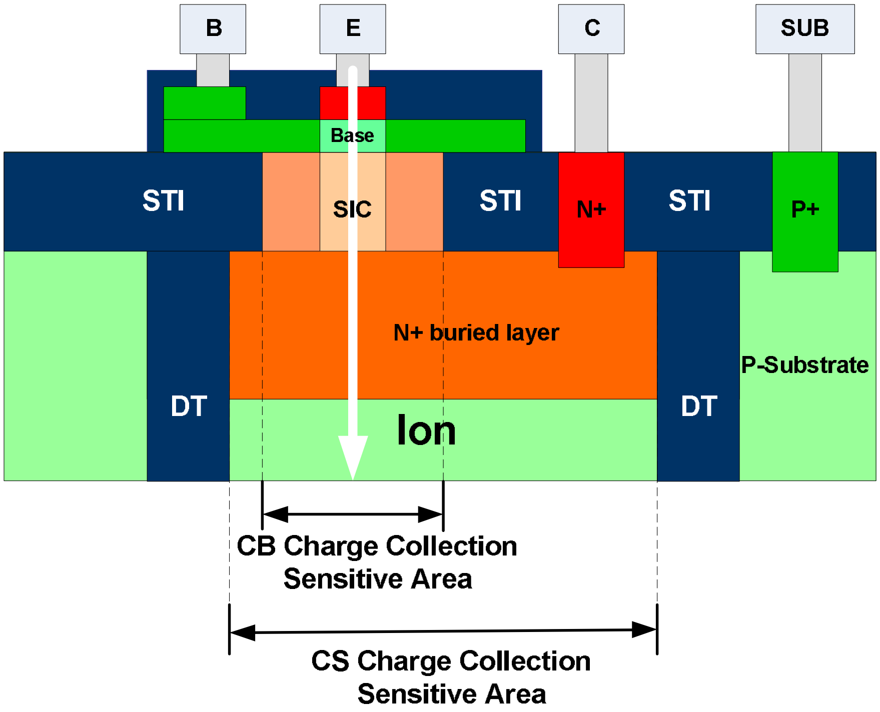

Figure 4.12: Sensitive areas for CB and CS junction charge collection in 2-D cross section illustration.

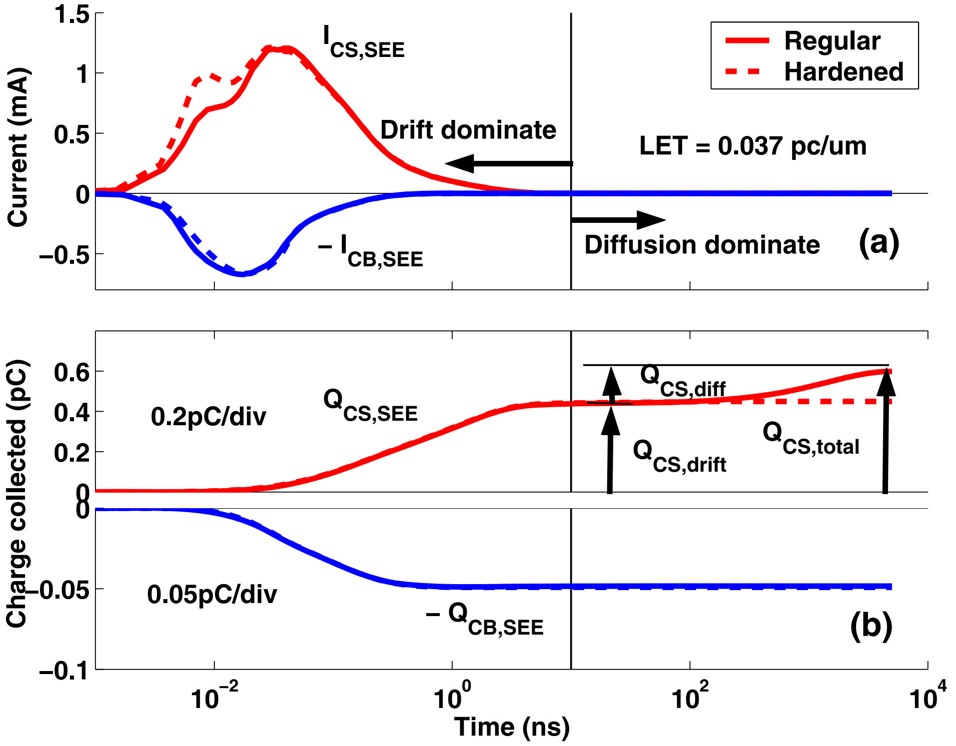

Figure 4.13: The SEE induced CB and CS charge collection currents and the integral charges for regular and hardened SiGe HBTs.

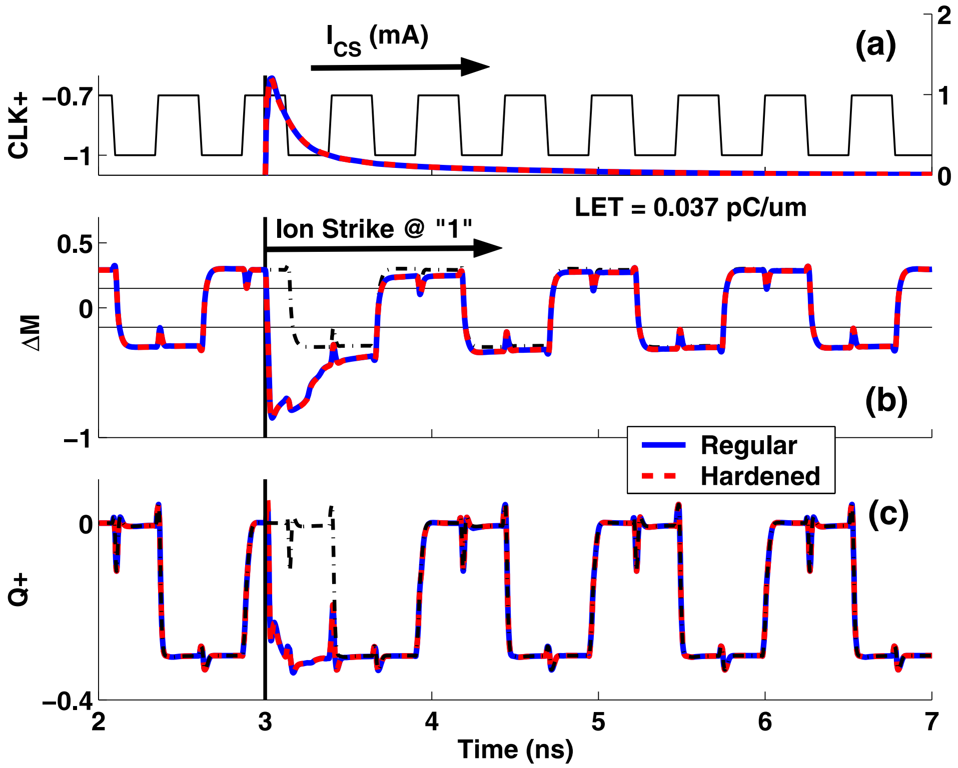

Figure 4.14: Comparison of the simulated ΔM and $Q+$ with CB and CS currents from regular and hardened SiGe HBTs.

CHAPTER 5

SINGLE EVENT TRANSIENTS IN EMITTER FOLLOWERS

This work is started to answer circuit designer's questions on how to optimize circuit design to minimize SET in emitter followers. As the emitter current determines output, using a higher biasing emitter current seems to be a logical hardening approach. The basic idea is to make SEE induced transient emitter current smaller than the biasing emitter current. This is in fact what designers first proposed. However, our simulations show this intuitive approach is completely incorrect, as it does not consider the complex operation of the circuit during SET.

Various RHBD techniques at both device and circuit levels have been developed to improve SEE [45] [44] [3] [9]. These techniques focus on collector charge collection, particularly through the reverse biased CS junction, the dominant path, and therefore apply to circuits in which the collector current determines circuit output, such as ECL circuits. However, such techniques do not apply to circuits where the emitter current determines circuit output. An example is emitter follower, which is widely used as output buffer, unity voltage gain amplifier, dc power regulator in analog circuits, as well as level shifter in ECL circuits. This chapter investigates SET in SiGe HBT emitter followers using true mixed mode simulation, and provides hardening guidelines.

This chapter is organized as follows. In Section 5.1, the 3-D simulation details and circuit topology of an emitter follower are described. Section 5.2 describes the SET simulation results in three typical emitter followers. Section 5.4 to 5.8 further examines the impact of biasing current and biasing resistance on SET individually by varying only the design parameter in question while keeping everything else the same. A critical result is that the emitter voltage SET follows the base voltage SET by the very nature of circuit operation of an emitter follower, which in turn is determined by base charge collection. Section 5.9 examines the impact of ion strike position, depth, and LET. Section 5.10 examines the optimization of base biasing resistance for reduced emitter voltage SET.

5.1 Simulation Details and Circuit Topology

The 3-D transistor used in this work is from the IBM 8HP SiGe HBT technology, which is from a more advanced technology compared with the device used in Chapter 2 and 4. The *n-p-n-p* structure is the same, but the layout of the contacts and the doping profile are different. Fig. 5.1 shows the 2-D cross section of this advanced transistor. The transient simulation conditions are also a little different from simulations in Chapter 2 and 4. The silicon substrate has an area of $25\mu m \times 25\mu m$ and a depth of $35\mu m$. The normal deep ion strike through the emitter center has a uniform LET of 0.1pC/μm ($10 MeV\text{-}cm^2/mg$). The charge track was generated using a Gaussian waveform, with an $1/e$ characteristic time scale of 2 picosecond and an $1/e$ characteristic radius of 0.2 μm. The peak of the Gaussian occurs at 6 picoseconds.

Fig. 5.2 shows the circuit topology of a typical emitter follower. Unless specified, the dc power supply V_{CC} is 3.3V. The base biasing resistance R_{BB}, base biasing current I_{BB}, emitter biasing resistance R_{EE}, and emitter biasing current I_{EF} are the design parameters. Emitter followers with multiple R_{BB}, I_{BB}, R_{EE}, and I_{EF} combinations are carefully designed and simulated to find out how to minimize duration and magnitude of emitter voltage SET.

5.2 SET in Typical Emitter Followers

We first consider three emitter followers with design parameters shown in Table 5.1. I_{EF}, R_{EE}, I_{BB}, and R_{BB} are chosen such that the quiescent emitter voltage $V_{E,Q}$ is 2.24V for a V_{CC} of

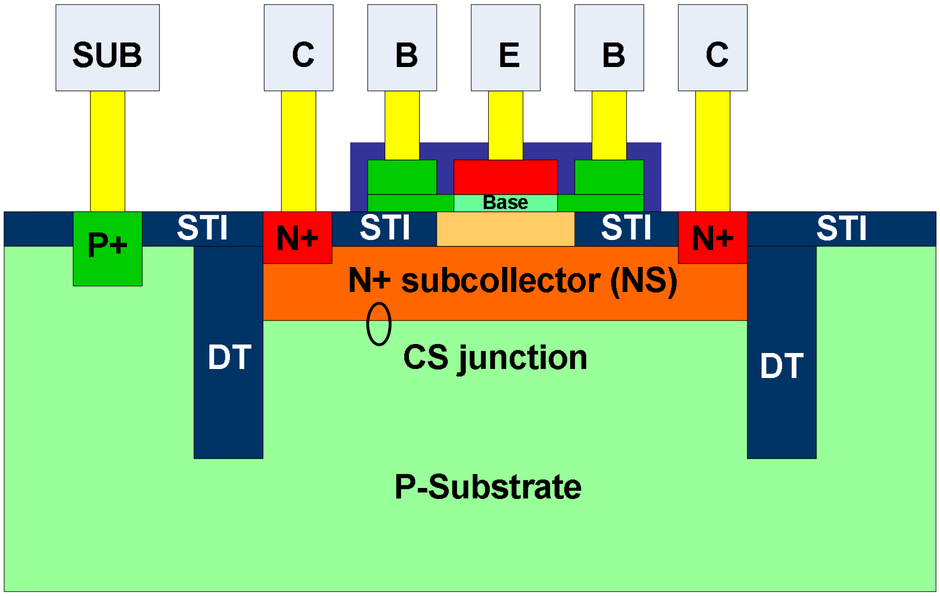

Figure 5.1: 2-D cross section of an 8HP regular HBT.

Table 5.1: Design parameters for three typical emitter followers.

Name	$R_{EE}(\Omega)$	$R_{BB}(\Omega)$	$I_{BB}(\mu\text{A})$	$I_{EF}(\mu\text{A})$
EF1	5000	200	1300	450
EF2	2000	200	1100	1120
EF3	1000	1600	140	2200

3.3V. The base quiescent voltage $V_{B,Q}$ is only slightly different among the three emitter followers, as I_E exponentially depends on V_{BE}.

Fig. 5.3 (a) compares the output emitter voltage of the three emitter followers. The peak V_E deviation is relatively close for the three designs. However, the design with highest I_{EF} shows the longest (worst) duration. The results at least suggest that a high I_{EF} does not guarantee reduced

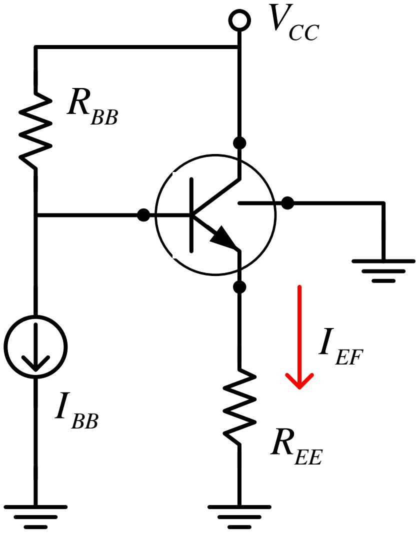

Figure 5.2: The circuit topology of a typical emitter follower.

emitter voltage SET. To further clarify the impact of I_{EF}, we will vary only I_{EF} while keeping everything else the same in Section 5.4 to 5.8.

Fig. 5.3 (b) compares the SEE induced emitter current $I_{E,SEE}$ for the three circuits. $I_{E,SEE}$ is defined as $I_{E,SEE} = -(I_E - I_{E,Q})$. I_E and $I_{E,Q}$ are the transient and quiescent current flowing out of the emitter. $I_{E,Q} = I_{EF}$. The positive direction of $I_{E,SEE}$ is defined as entering the emitter. $I_{E,SEE}$ is not dominated by EB junction charge collection, which would give a positive $I_{E,SEE}$, while the simulated $I_{E,SEE}$ is negative in all cases. It is not dominated by ion track shunt effect [47] either, even though the resulting $I_{E,SEE}$ would be negative, because V_{CE} is the lowest for the highest $I_{E,SEE}$, as shown in Fig. 5.3 (c). Instead, $I_{E,SEE}$ follows V_E through

$$I_{E,SEE} = -(V_E/R_{EE} - I_{EF}). \tag{5.1}$$

The impact of ion track shunt effect will be further investigated using an off-center ion strike in Section 5.9.1.

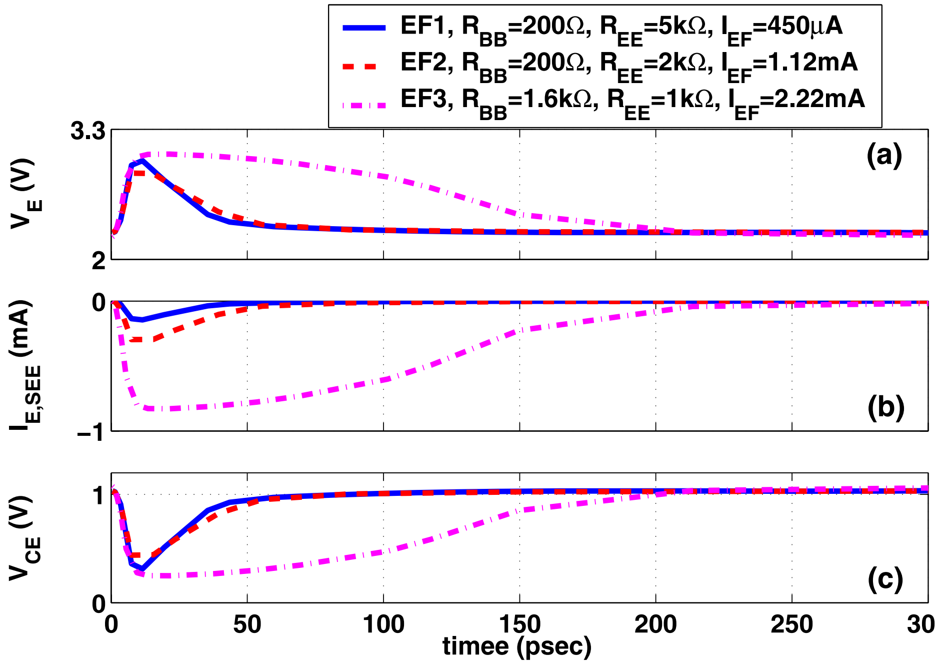

Figure 5.3: SET on three typical emitter followers. (a) V_E, (b) $I_{E,SEE}$, and (c) V_{CE} versus time.

Now we have established that $I_{E,SEE}$ is not a result of the normal *pn* junction and ion track shunt charge collection. The only next possibility is that it is a result of interaction between circuit and charge collection. Fig. 5.4 (a) and (b) show the base voltage V_B and the SEE induced base current, $I_{B,SEE} = I_B - I_{B,Q}$. Again, $I_{B,SEE}$ flowing into the base is defined as positive. V_B can be determined from $I_{B,SEE}$ as

$$V_B = V_{B,Q} - I_{B,SEE} R_{BB}. \tag{5.2}$$

Observe that the V_E SET waveform closely follows the V_B SET waveform, which is a result of the emitter voltage following base voltage nature of the emitter follower circuit operation, despite the ion strike. During the following process, V_E is limited by V_{CC}. V_B follows $I_{B,SEE}$ according to (5.2). $I_{E,SEE}$ actually originated from $I_{B,SEE}$ and hence base charge collection.

V_E upset is thus mainly a result of V_B upset, which then depends on $I_{B,SEE}R_{BB}$ product. $I_{B,SEE}$ lasts longer for design EF3, because of the largest R_{BB} in the path of CB junction charge collection. The EB junction total volume is very small compared to the CB junction volume, thus the base charge collection observed is dominated by CB junction collection. Here the collector is *ac* grounded, while the base node sees R_{BB}. Fig. 5.4 (c) shows the base collected charge $Q_{B,SEE}$ obtained from integration of $I_{B,SEE}$ vs time data [42]. The final total amount of charge collected is about the same for all 3 designs, as expected.

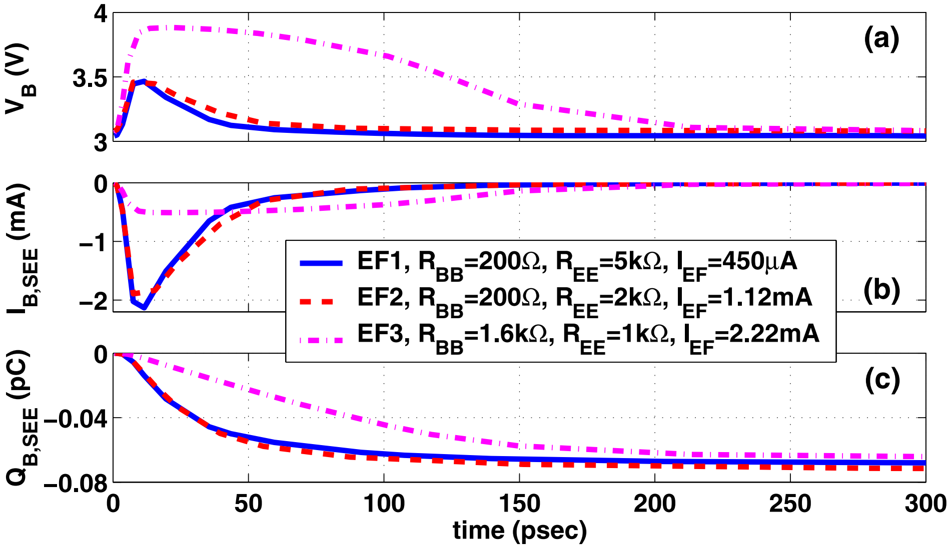

Figure 5.4: SET on three typical emitter followers. (a) V_B, (b) $I_{B,SEE}$, and (c) $Q_{B,SEE}$ versus time.

The above analysis concludes that R_{BB} *is what determines the emitter voltage SET waveform.* EF1 and EF2 have identical R_{BB} and thus the same V_E SET waveforms. EF3 has a larger R_{BB}.

The higher impedance slows down base charge collection, leading to the longest V_E SET. V_E cannot exceed V_{CC} in this process. More mixed mode DESSIS simulations are done to examine the individual impact of design parameters in Section 5.4 to 5.8 .

5.3 Biasing Current and Resistance Dependence

To examine the impact of the four design parameters, I_{EF}, R_{EE}, I_{BB}, and R_{BB} separately, the circuit topology in Fig. 5.2 must be modified slightly. For example, to investigate the impact of I_{EF} individually, emitter followers with different I_{EF} but the same I_{BB}, R_{BB}, and R_{EE} must be simulated. $V_{B,Q}$ are the same for the three circuits since I_{BB}, and R_{BB} are the same. Then, there will be a voltage shift at $V_{E,Q}$, since $V_{E,Q} = I_{EF}R_{EE}$. This, however, will cause an additional exponential change of I_{EF} as V_{BE} varies. An independent dc voltage source V_{EE}, as shown in Fig. 5.5 (a), must be added to compensate the shift of $V_{E,Q}$. For smaller I_{EF}, V_{EE} is positive, and for larger I_{EF}, V_{EE} is negative, since now we have $V_{E,Q} = V_{EE} + I_{EF}R_{EE}$. The same schematic can be used for designs with different R_{EE}. Similarly, an independent voltage source has to be used to compensate the voltage shift at $V_{B,Q}$ when examining the impact of I_{BB} and R_{BB} in singles. Fig. 5.5 (b) gives the schematic for simulations with varying I_{BB} or R_{BB}. A separate voltage source V_{BB} is added. With V_{BB}, the base biasing voltage is calculated as $V_{B,Q} = V_{BB} - \left(I_{BB} + I_{B,Q}\right) R_{BB}$.

5.4 Emitter Biasing Current Dependence

As mentioned before, one intuitive approach to reduce emitter voltage SET is to increase the emitter biasing current I_{EF} so that the SEE induced emitter current can be made less significant, as $\left(I_{EF} + I_{E,SEE}\right) R_{EE}$ determines V_E. We have however shown earlier using the three typical

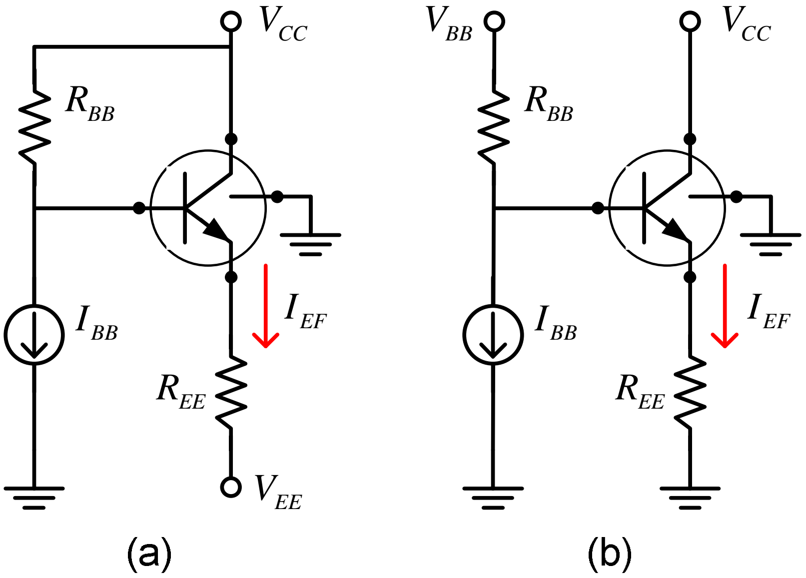

Figure 5.5: The schematic of emitter followers used to examine the impact of (a) I_{EF} and R_{EE}, and (b) I_{BB} and R_{BB}, on emitter voltage SET individually.

designs that a larger I_{EF} does not guarantee reduced V_E SET. In those designs, all design parameters are varied inevitably due to circuit constraints.

We now vary I_{EF} only using the circuit shown in Fig. 5.5 (a). Three emitter followers with different I_{EF} are designed and simulated. One of them is EF2 with I_{EF}=1.12mA. The other two emitter followers have I_{EF}=480μA and I_{EF}=2.2mA. V_{EE}=1.34V for I_{EF}=480μA, and V_{EE}=-2.16V for I_{EF}=2.2mA. The three circuits have the same R_{BB}, I_{BB}, R_{EE} as EF2, but a sightly different $V_{E,Q}$ to allow the shift in V_{BE} and then I_{EF}.

The simulation results are shown in Fig. 5.6. First, the rate, duration, and total amount of base charge collection are approximately the same for the three circuits with varying I_{EF}, as shown in Fig. 5.6 (a) and (b). The three circuits have practically identical V_E SET output as expected, which follow V_B SET very well, as shown in Fig. 5.6 (c) and (d). Since R_{EE} are the same for the three circuits, $I_{E,SEE}$ are approximately the same, and thus are not shown here. This further confirms our earlier analysis that I_{EF} can barely affect SET of emitter follower.

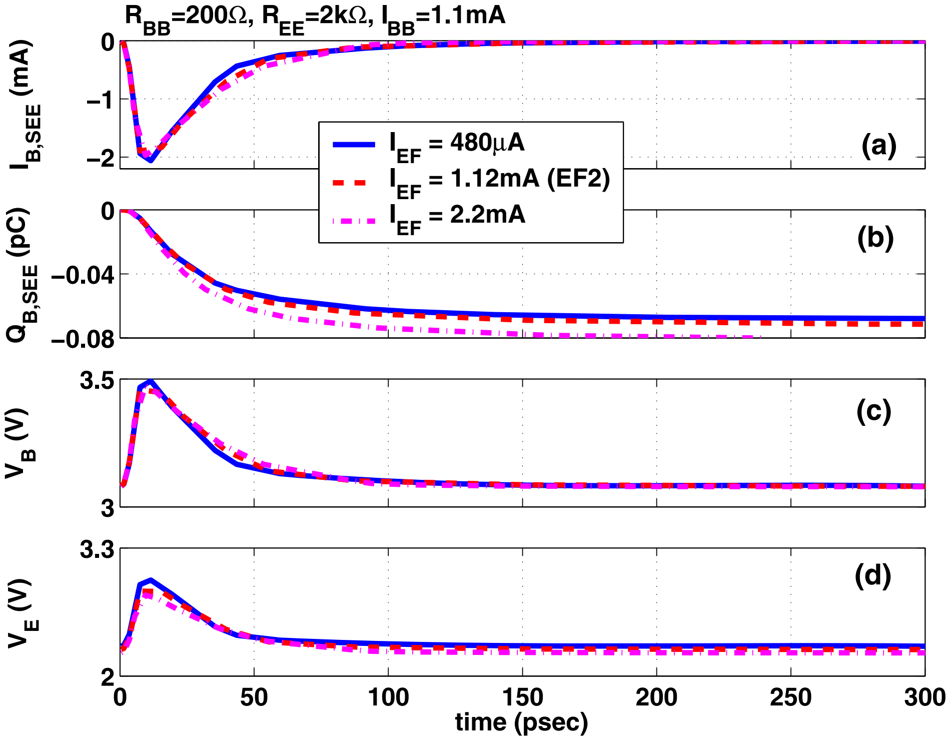

Figure 5.6: SET on emitter followers with different emitter biasing current. (a) $I_{B,SEE}$, (b) $Q_{B,SEE}$, (c) V_B, and (d) V_E versus time.

5.5 Emitter Biasing Resistance Dependence

Again, for further verification of the impact of R_{EE}, two emitter followers with the same I_{EF}, I_{BB} and R_{BB}, but different R_{EE} are compared with EF2. Here we choose to use R_{EE}=1kΩ and R_{EE}=5kΩ. The other design parameters are chosen to be the same as in EF2, that is, I_{EF}=1.12mA, I_{BB}=1.1mA, R_{BB}=200Ω, $V_{B,Q}$=3.08V, and $V_{E,Q}$=2.24V. Recall that $R_{EE} = 2k\Omega$ and $V_{EE} = 0$V in EF2. To achieve the same $V_{E,Q}$ with multiple R_{EE}, we use V_{EE}=1.1V for R_{EE}=1kΩ and V_{EE}=-3.3V for R_{EE}=5kΩ in the schematic of Fig. 5.5 (a).

Fig. 5.7 (a) and (b) show SEE induced base current and base collected charge versus time. Neither the base current transient nor the base charge collected is dependent on R_{EE}. Fig. 5.7 (c) shows that V_E from the three circuits are practically identical. A larger R_{EE} does lead to a lower $I_{E,SEE}$, as shown in Fig. 5.7 (d), since

$$I_{E,SEE} = -\left(\left(V_E - V_{EE}\right)/R_{EE} - I_{EF}\right). \tag{5.3}$$

Thus, R_{EE} has negligible effects on emitter voltage SET, despite its large impact on the emitter current SET.

5.6 Base Biasing Current Dependence

To examine the impact of I_{BB} on V_E SET, two emitter followers with I_{BB}=140μA and 2.2mA are simulated and compared with EF2 (I_{BB}=1.1mA). The schematic in Fig. 5.5 (b) is used to achieve the same $V_{B,Q}$. V_{BB}=3.11V for I_{BB}=140μA, and V_{BB}=3.52V for I_{BB}=2.2mA. I_{EF}=1.12mA, R_{BB}=200Ω, R_{EE}=2kΩ, and V_{CC}=3.3V for all three circuits. As long as $V_{B,Q}$ is fixed, the value of I_{BB} should have no effects on base charge collection and emitter voltage upset. $I_{B,SEE}$ and $Q_{B,SEE}$ in Fig. 5.8 (a) and (b) are identical for the three circuits as expected. Fig. 5.8 (c) and (d) show that the V_E SET from three circuits are identical, and follow the V_B SET exactly. This concludes that I_{BB} has no effects on base charge collection, and then does not affect emitter voltage SET at all.

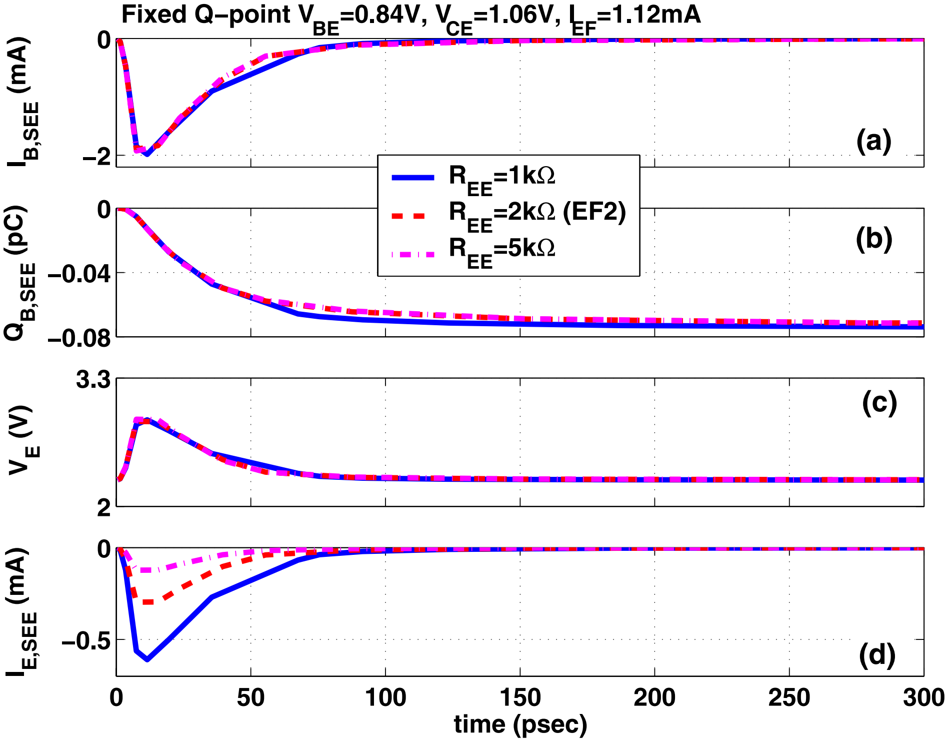

Figure 5.7: SET on emitter followers with different emitter biasing resistance. (a) $I_{B,SEE}$, (b) $Q_{B,SEE}$, (c) V_E, and (d) $I_{E,SEE}$ versus time.

5.7 Base Biasing Resistance Dependence

For further verification and better insight into R_{BB}'s effect, we vary R_{BB} in Fig. 5.5 (b), while keeping I_{EF}, R_{EE}, $V_{B,Q}$, $V_{E,Q}$, and V_{CC} the same as in EF2. V_{BB}=3.3V. To keep $V_{B,Q}$ the same, we choose I_{BB}=1.1mA, 140μA, 70μA for R_{BB}= 200Ω, 1.6kΩ, and 3.2kΩ, since $V_{B,Q} = V_{BB} - (I_{BB} + I_{B,Q})R_{BB}$. The difference in I_{BB} will not affect SET, as we have shown in Section 5.6.

Fig. 5.9 (a) compares $I_{B,SEE}$ for different R_{BB}. A larger R_{BB} reduces the charge collection speed, which leads to a lower charge collection current, and a longer SET duration. However, the total amount of charge collected by the base are approximately the same for different R_{BB}, as shown

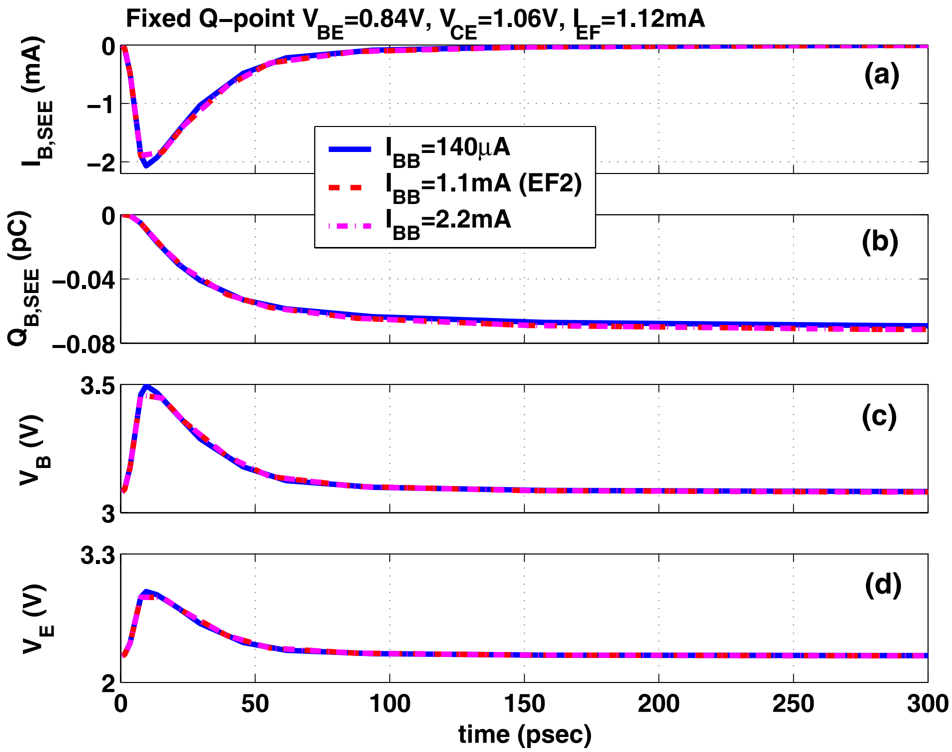

Figure 5.8: SET on emitter followers with different base biasing current. (a) $I_{B,SEE}$, (b) $Q_{B,SEE}$, (c) V_B, (d) V_E versus time.

in Fig. 5.9 (b) and expected from CB junction charge collection mechanism. The peak $I_{B,SEE}$ decreases as R_{BB} increases. As R_{BB} increases from 200Ω to 1.6kΩ, by a factor of 8, the peak $I_{B,SEE}$ decreases by only 4×. The SEE induced voltage change on R_{BB} is doubled. Since $I_{B,SEE}$ is negative, V_B for higher R_{BB} is higher from (5.2). Fig. 5.9 (c) compares V_B for different R_{BB}. The peak V_B SET increases as R_{BB} increases, until it reaches a limit of 4V. The duration increases significantly as R_{BB} increases after V_B reaches 4V. The relationship between SET duration and R_{BB} will be further discussed in Section 5.10. The V_E SET waveforms in Fig. 5.9 (d) clearly show that V_E is highly R_{BB} dependent and follows V_B SET as expected. As R_{BB} increases, the level and duration of V_E upset increase. The peak value of V_E is limited by V_{CC}=3.3V. V_E upset and $I_{E,SEE}$ are not dominated by SEE induced charge collection at the emitter. Instead, V_E upset simply follows the V_B upset for reasons discussed above.

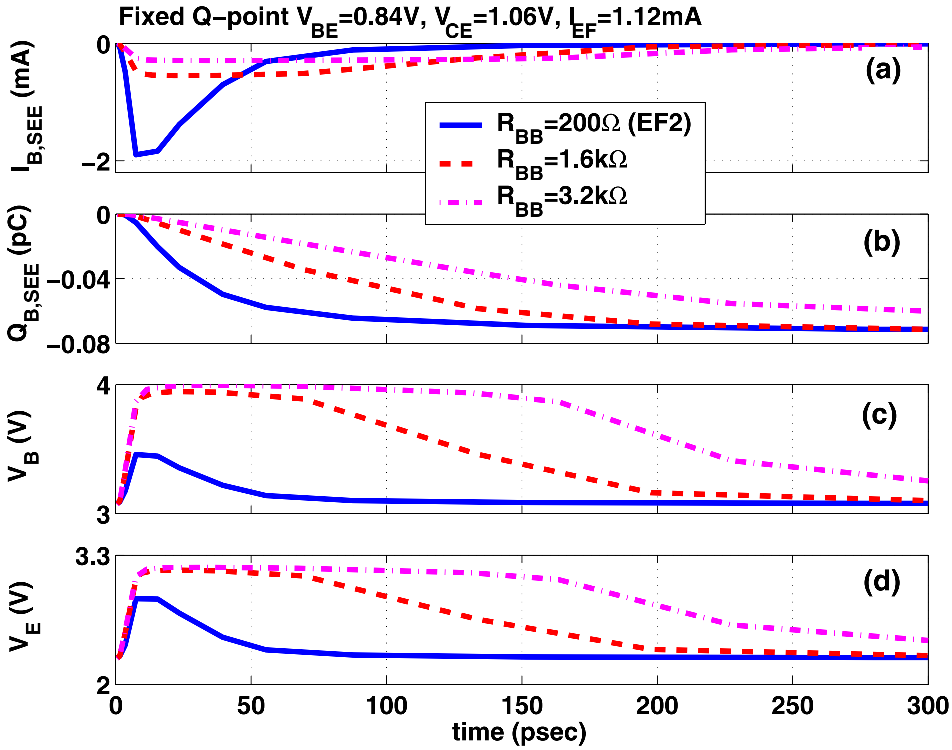

Figure 5.9: SET on emitter followers with different base biasing resistance. (a) $I_{B,SEE}$, (b) $Q_{B,SEE}$, (c) V_B, and (d) V_E versus time.

5.8 CB Voltage Dependence

From previous analysis, V_E SET is determined by base charge collection. R_{BB} is the most important design parameter for optimizing emitter follower SET, because R_{BB} is the impedance on base charge collection path. The higher the impedance, the lower the base charge collection rate, the longer the base charge collection time. V_{CB} is another dominant factor that affects base charge collection. To examine the effects of V_{CB}, Two emitter followers with V_{CB}=-0.5V and 1V are compared with EF2 (V_{CB}=0.22V). The schematic in Fig. 5.5 (b) is used here. I_{EF}=1.12mA, V_{BB}=3.3V, R_{BB}=200Ω, R_{EE}=2kΩ for the three circuits. The other design parameters for the three circuits are:

1. I_{BB}=1.075mA, V_{CC}=2.58V.
2. I_{BB}=1.1mA, V_{CC}=3.3V (EF2).
3. I_{BB}=1.13mA, V_{CC}=4.08V.

As V_{CB} increases, the CB junction field increases, which should lead to a faster base charge collection. The total amount of charge collected should not change much. With increasing V_{CB}, we observe a higher peak value and a shorter duration of $I_{B,SEE}$ in Fig. 5.10 (a) and the same total amount of charge collected by base in Fig. 5.10 (b), as expected.

Fig. 5.10 (c) compares V_B for different V_{CB}. As a consequence of the faster base charge collection at higher V_{CB}, V_B determined by $I_{B,SEE}$ from (5.2) has a higher peak value and a shorter duration. V_E in Fig. 5.10 (d) follows V_B. However, the peak of V_E is still limited by V_{CC}. It does not exceed V_{CC} for all cases.

5.9 Ion Strike Dependence

5.9.1 Position and Depth Dependence

In Section 5.2, we have shown that the ion track shunt effect is not important for $I_{E,SEE}$, and $I_{E,SEE}$ is mainly a result of V_E following V_B. Furthermore, V_B SET is primarily determined by base charge collection through the CB junction.

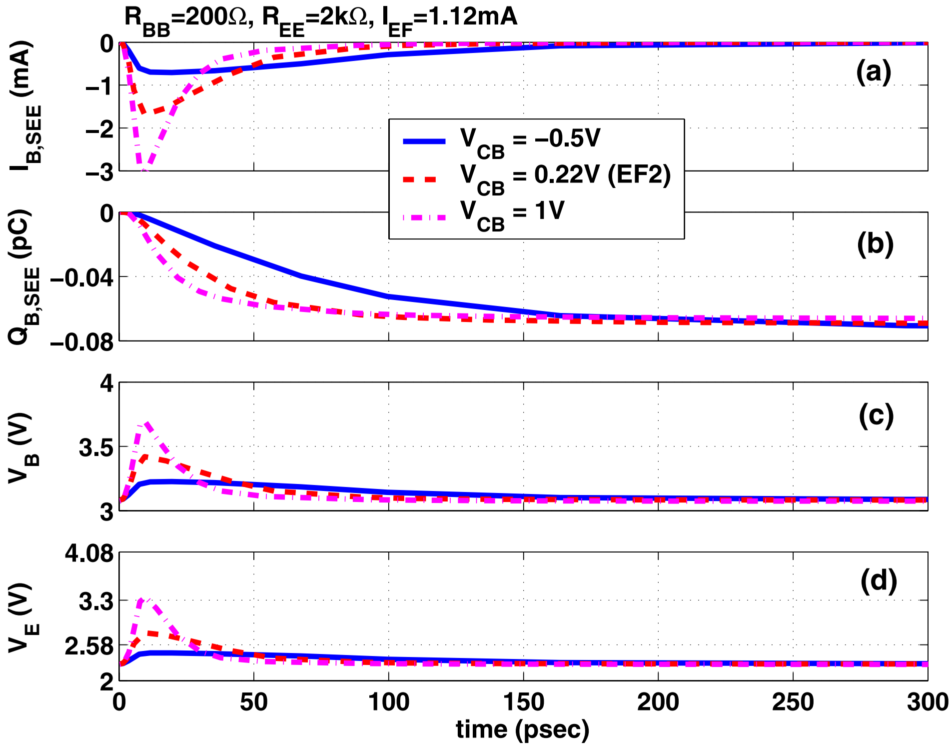

Figure 5.10: SET on emitter followers with different CB voltage. (a) $I_{B,SEE}$, (b) $Q_{B,SEE}$, (c) V_B, and (d) V_E versus time.

These results can be further verified by varying the position and depth of ion strike. We choose two ion strike positions, one at the emitter center, and the other in the middle of the extrinsic base. This is illustrated in a 2-D cross section in Fig. 5.11. The ion track for the center strike, ION$_1$, shunts the emitter and collector, while the off center strike track, ION$_2$, does not. A comparison of the two strikes would directly show any ion track shunt effect on the circuit. We also reduce the depth of the ion strike for the off center strike such that charge deposition occurs only above the n^+ buried layer. As this strike does not go through the EB junction or the CS junction, the only junction involved is the CB junction. This off center shallow strike allows us to examine if CB junction is indeed the dominant charge collection path responsible for SET in emitter followers.

The simulation results for EF2 are shown in Fig. 5.12 for the above three ion strikes. $I_{B,SEE}$, $Q_{B,SEE}$, $I_{E,SEE}$ and V_E are approximately identical for all three ion strikes. This provides additional verification to our conclusion that the emitter voltage SET primarily originates from CB junction charge collection.

From a cross section standpoint, we expect an improvement over circuits in which collector current determines output. In that case, the CS junction is the dominant charge collection path, and the area enclosed inside the DT isolation around the HBT approximately defines the area for maximum collector charge collection [43]. For emitter followers, we are concerned with the area for maximum base charge collection, which is defined by the STI [43]. This is illustrated in Fig. 5.11. When the ion strike is in between the STIs, base charge collection maximizes, and the resulting emitter voltage SET is the same.

5.9.2 LET Dependence

The EF2 circuit, which shows best SET tolerance, is simulated for different LETs. Fig. 5.13 (a) indicates that the higher LET, the longer it takes for the charge to be collected, even though the charge collection is faster. The total amount of charge collected increases accordingly as shown in Fig. 5.13 (b). Since base charge collection rate and time determine base voltage upset, a higher LET further leads to a worse V_B upset. With increasing LET, a larger and longer V_B upset is observed in Fig. 5.13 (c). Fig. 5.13 (d) compares V_E under three LETs. V_E follows V_B, but is limited by V_{CC}, and thus its magnitude will saturate as LET increases. Note that there is a small V_{CE} saturation voltage difference between V_{CC} and V_E.

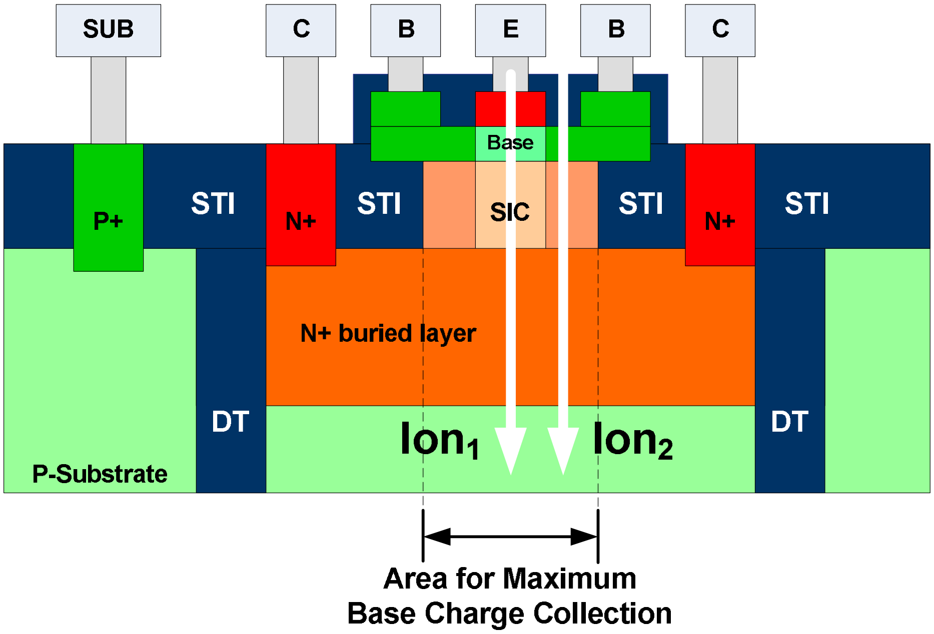

Figure 5.11: Illustration of the ion tracks for a center strike and an off center strike.

5.10 Hardening Implications

From previous analysis, the impedance and electric field across the CB junction dominate V_E SET of an emitter follower. Therefore, R_{BB} and V_{CB} are the most important factors for emitter follower SET. V_{CB} is normally limited by the supply voltage and headroom considerations. This leaves R_{BB} the only variable to be optimized for reducing SET.

To identify the relationship between R_{BB} and V_E SET, more emitter followers with R_{BB} ranging from 5Ω to 3.2kΩ are designed and simulated. We note that 5Ω represents a low extreme, and in practice R_{BB} is much higher. Fig. 5.14 (a) compares V_E for six R_{BB}. As R_{BB} decreases, V_E SET is first reduced dramatically, especially the duration of V_E SET. When R_{BB} is below 50Ω, further decrease of R_{BB} does not help reducing V_E SET. Instead, V_E SET reaches a low limit with

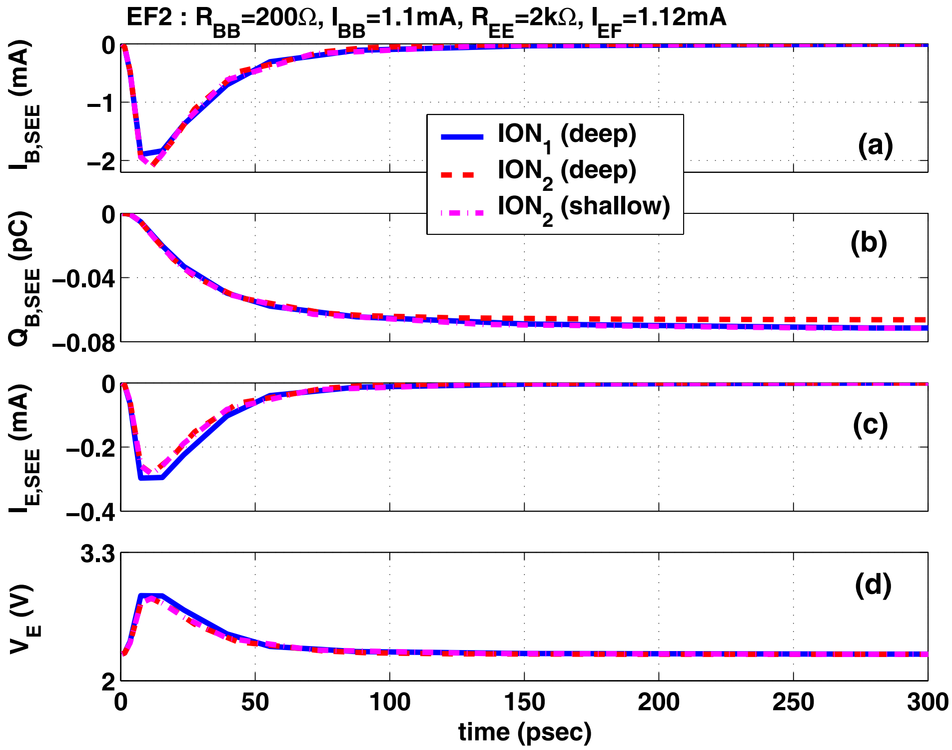

Figure 5.12: SET on emitter followers under ion strikes at different position and with different depth. (a) $I_{E,SEE}$, (b) V_E versus time.

very short duration. However, the peak and duration of V_B SET continue to decrease as shown in Fig. 5.14 (b). This indicates that V_E no longer follows V_B for extremely small R_{BB}. Fig. 5.14 (c) shows that base charge collection for R_{BB} below 50Ω are practically identical. V_B SET reduces to a negligible short pulse because the voltage drop on R_{BB} is very small.

For comparison, we define SET duration as the time it takes for V_E to drop back to a reference value $V_{E,REF}$. For the waveforms shown in Fig. 5.14, a $V_{E,REF}$ of 2.3V is used for a $V_{E,Q}$ of 2.24V. Fig. 5.15 (a) shows SET duration versus R_{BB}. Fig. 5.15 (b) shows SET duration versus $1/R_{BB}$. As R_{BB} decreases, the duration of V_E SET first decreases linearly until it reaches 44 picoseconds.

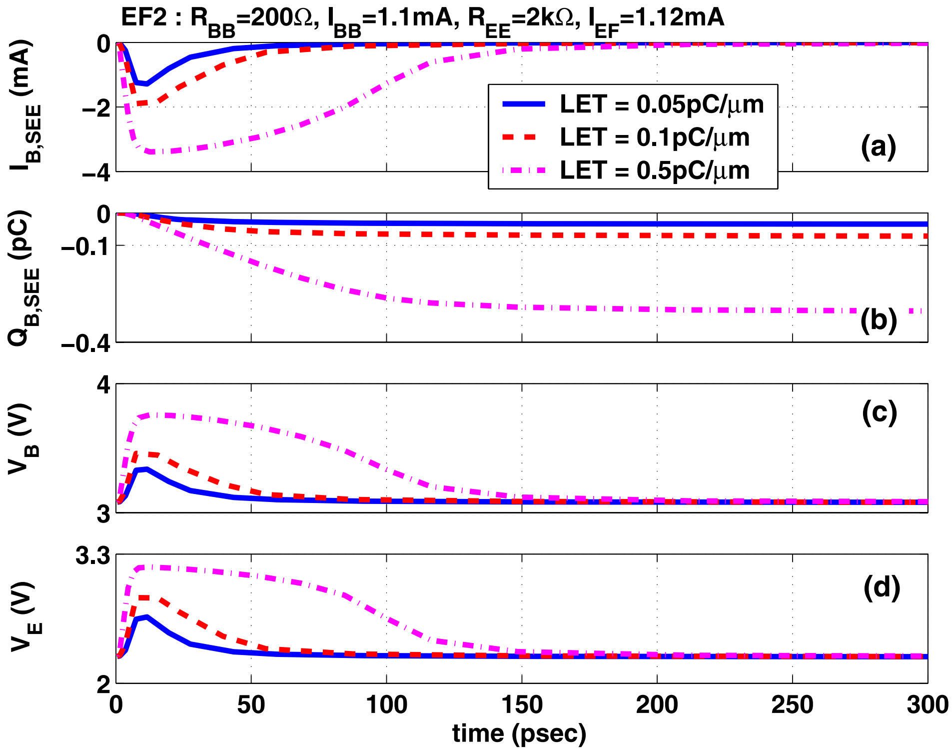

Figure 5.13: SET on emitter followers under ion strikes with different LET. (a) $I_{B,SEE}$, (b) $Q_{B,SEE}$, (c) V_B, and (d) V_E versus time.

Approximately, the duration limit is reached at R_{BB}=50Ω. We believe that the V_E SET duration's low limit is R_{EE} dependent. No further simulation is done as this occurs only for extremely small R_{BB}, that are not used in practical designs.

Device level hardening is not effective for emitter followers as base charge collection is the dominant origin for typical circuits. Existing device level SiGe HBT hardening techniques focus on reducing charge collection in the CS junction by collecting part of the deposited charge in the substrate through an added back junction or a dummy CS junction [44] [3] [9]. SOI technology even completely eliminates the CS junction [45]. However, the heavily doped n^+ buried layer

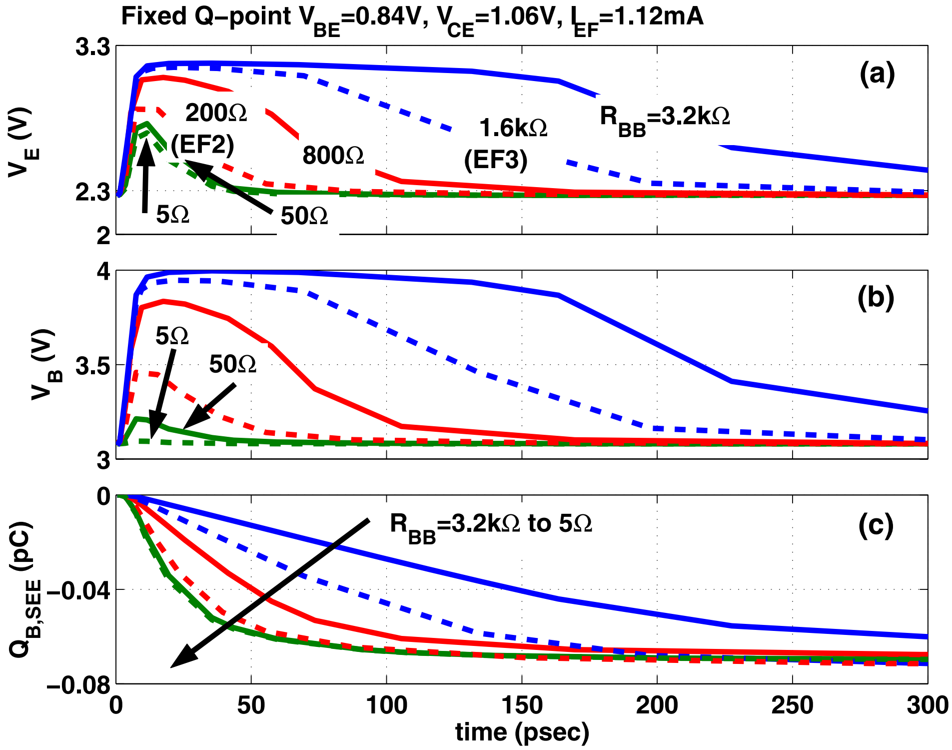

Figure 5.14: SET on emitter followers with different R_{BB}. (a) V_E, (b) $Q_{B,SEE}$ versus time.

decouples the charge collection in the intrinsic emitter, base from those in the CS junction. The charge collected by base and emitter is nearly identical for SOI and bulk SiGe HBTs [45]. The same situation exists for SiGe HBTs hardened using back junction or dummy collector methods. This indicates that all of these device-level or technology-level hardening techniques are not effective for reducing SET in emitter followers and other circuits in which the emitter current is of interest.

5.11 Conclusion

This chapter presents true mixed mode simulation results for multiple emitter follower designs, as well as parametric analysis. In contrast to conventional wisdom, using a higher emitter current

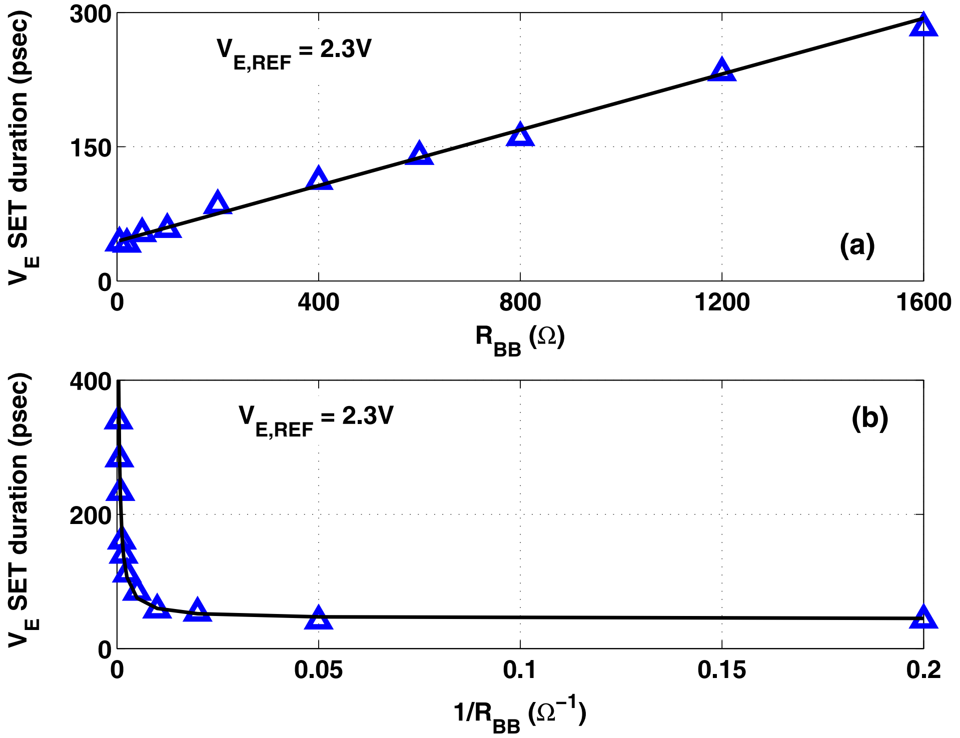

Figure 5.15: SET duration on emitter followers with different base biasing resistance. (a) SET duration versus R_{BB}, (b) SET duration versus R_{BB}^{-1}

does not help reducing emitter voltage SET at all. Detailed analysis shows that the emitter voltage upset originates from base charge collection. The parametric analysis shows that R_{BB} is the key parameter that affects V_E SET in emitter followers. The product of SEE induced base current and base biasing resistance R_{BB} determines the amount of base voltage upset or deviation, which is shown to decrease with decreasing R_{BB}. For R_{BB} values found in practical circuits, a smaller R_{BB} should be used to reduce emitter output voltage SET, as the emitter voltage upset tracks the base voltage upset.

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