Design and Implementation of RF Receiver Front-end and Tunable Filter

by

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Abstract

The rapidly growing wireless communication market is creating a high demand for low-cost, low power, highly-integrated radio frequency (RF) transceivers. This dissertation focuses on techniques to realize fully-integrated, wireless RF receivers incorporating all passive components.

In this work, several novel topologies for RF receivers, like reconfigurable wideband low noise amplifier (LNA), mixers with gain reuse, high resolution digitally controlled oscillator and the low power wideband receiver are investigated. The work uses both standard silicon CMOS and SiGe BiCMOS technology to demonstrate operations of those building blocks and the whole receiver. First, a LNA MMIC with notch filter implemented in a 0.13um SiGe BiCMOS technology is introduced. The LNA utilizes Q-enhanced techniques to achieve high gain and high image rejection ratio (IRR) simultaneously. With Q-enhanced techniques, 70dB image rejection ratio is achieved in the LNA. Next, the design of a wide-band LNA for self-healing application is demonstrated. With the self-healing technology, the peak gain frequency and the input matching frequency can be adjusted to the operating frequency simultaneously. Meanwhile, the gain of proposed LNA is also adjustable for self-healing purpose. In order to implement a digital phase locked loop (DPLL), a 12 bits digitally controlled oscillator implemented in 0.18um CMOS technology is also investigated in the following chapter.

After introducing the building blocks, this dissertation presents an 8-18GHz wideband receiver with super-heterodyne topology. Multi-feedback technology, which provides more

freedom in input matching, was utilized in the LNA design for the input matching over the X- and Ku-band frequency range. In order to save power, both the RF and IF signals share the tunable transconductance stage. The IF output of the first mixer is fed back into the tunable input stage for IF amplification in a recursive manner, which significantly enhances the gain tuning without increasing the power.

In the second part of the dissertation, tunable filter technologies are discussed. Two different tunable filter architectures are discussed and implemented. One is the 6^{th} order Butterworth switched capacitor (SC) low pass filter while another is low pass filter based on the tunable active CMOS resistor. The SC filter is capable of operating over an ultra-wide temperature (UWT) range from -180℃ to 120℃ and under high-energy particle radiation environment on the lunar surface. The later tunable filter is based on a novel tunable CMOS resistor. The resistance is inversely proportional to bias current, to provide the resistor with a wider tuning range. And transistors, which compose the active resistor, operate at saturation region to achieve very large resistance within a small area.

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List of Abbreviations

RF	Radio frequency
LNA	Low noise amplifier
DCO	Digitally controlled oscillator
VGA	Variable gain amplifier
RFID	Radio frequency certification
GPS	Global positioning system
WLAN	Wireless local area network
NF	Noise figure
IIP3	Input third-order intercept point
OIP3	Output third-order intercept point
P1dB	Input 1dB compression point
OP1dB	Output 1dB compression point
SiGe	Silicon-germanium
HBT	Heterojunction bipolar transistor
IR	Image rejection
SAW	Surface-acoustic wave
SC	Switching capacitor
UWT	Ultra wide temperature
RHBD	Radiation hardened by design

Chapter 1 INTRODUCTION

1.1 RFIC design

The wireless communication market has been growing explosively in last decade due to the emerging applications and dropping prices. The rapidly growing market is creating an increasing demand for the high performance radio frequency (RF) transceivers. The RFIC technology is widely used in various systems, such as: cell phones, radio frequency identification (RFID), global positioning system (GPS), wireless local area network (WLAN), HyperLAN, Bluetooth, ultra wideband (UWB) and so on. A summary of several RF wireless systems is given in Table 1.1. In addition, since the RFIC technology has the inherent advantage of small size, low power consumption and low cost, traditional systems relying on separate components are being replaced. In the design of RFIC, expertise in many different areas such as microwaves, communications and integrated circuit design is required. How to combine the required knowledge is a real challenge.

The commercial process for RFIC design mainly includes GaAs, CMOS and BiCMOS processes. Among the above processes, GaAs technology can achieve the best performance at high operating frequency up to 60GHz. The outstanding feature of GaAs technology comes at the expense of a relatively high price and high power consumption. Although CMOS technology can achieve high integration, low power and small size, it is hard to achieve high performance at high operating frequency, especially at the frequency beyond the X-band. Recently, silicon-germanium (SiGe) heterojunction bipolar transistor (HBT) technology, which utilizes bandgap

engineering to improve transistor performance while maintaining compatibility with low cost, high integration CMOS manufacturing, attracts more and more attention in IC design. This technology enjoys the quality of a high performance compared to CMOS at a relatively low price compared to GaAs. This dissertation takes the advantage of recent developments in CMOS and SiGe BiCMOS technologies to demonstrate the operations of RFIC designs and two tunable filters.

Table 1.1 Characteristics of some wireless systems

Characteristics	UWB	802.11a	802.11b	802.11g	Bluetooth
Frequency	3.1 ~ 10.6 GHz	5.150 ~ 5.250 GHz	2.41 ~ 2.462 GHz	2.4 GHz	2.4 GHz
Channel bandwidth	>500 MHz	20 MHz	25 MHz	25 MHz	1 MHz
Number of channels	1 ~ 15	127	127	3	79
Modulation type	BPSK/QPSK	OFDM: QPSK, QAM OFDM: BPSK OFDM: 16 QAM OFDM: 64 QAM	FHSS: GFSX DSSS:DBPSK DQPSK CCK:QPSK	OFDM+CCK	GFSK
Date rate	>100 Mbit/S	5.5 ~ 54 Mbit/S	1, 2, or 11 Mbit/S	54 Mbit/S	1 Mbit/S
Sensitivity	-	-87 dBm	-86 dBm	-76 dBm	-70 dBm

1.2 Dissertation organization

The following presents the organization of the dissertation and the contributions made by author throughout his Ph.D. research.

Chapter 2: Low noise amplifier (LNA), which is the most critical block in the RF receiver, is introduced in this chapter. Two LNA design examples are explained, designed and hardware verified in this chapter. First, a Q-enhanced LNA implemented in a 0.13um SiGe BiCMOS technology is introduced. The LNA/filter combination utilizes Q-enhanced techniques to achieve high gain and high image rejection ratio (IRR), simultaneously. The Q-enhanced LNA operates at 7.27GHz and achieves 22.5dB gain with an image rejection of 70dB IRR. The noise figure of the LNA is less than 5.1dB and the IIP3 is -13dBm. The LNA dissipates 21mW power with a 1.7V supply. Next, the design of a wideband LNA with self-healing technology is presented. With the self-healing technology, the peak gain frequency and the input matching frequency can be adjusted to the operating frequency simultaneously. Meanwhile, the gain of the LNA is also adjustable for self-healing purpose. The self-healing LNA is implemented in a 0.13um SiGe BiCMOS technology. The operating frequency of the proposed LNA can be adjusted from 4.5GHz to 7.8GHz. The self-healing LNA achieves typical gain of 19dB with 14dB continuous tuning range. The measured input matching is below -12dB over the entire frequency band. The measured noise figure of the LNA is 4.2dB at 7.8GHz and the output 1dB compression point is -9dBm.

Chapter 3: A 12-bit LC based digitally controlled oscillator (DCO) in a 0.13um CMOS technology is introduced in this chapter. The DCO is based on a negative gm architecture with banks of digitally controlled capacitors. The DCO oscillation frequency can be tuned from 3.36 GHz to 3.77 GHz with a tuning range of 11.5% and an average frequency resolution of 0.1MHz/bit. The measured DCO phase noise at 1MHz offset is -111 dBc/Hz. The DCO core consumes 8mA from a 1.5V supply.

Chapter 4: Wideband receiver design is discussed in this chapter. As an example, an 8-18GHz wideband receiver with super-heterodyne topology is introduced. Multi-feedback technology, which provides more freedom in input matching, was utilized in the LNA design for the input matching over the X- and Ku-band frequency range. In order to save power, both the RF and IF signals share the tunable transconductance stage. The IF output of the first mixer is fed back into the tunable input stage for IF amplification in a recursive manner, which significantly enhances the gain tuning without increasing the power. The wideband receiver MMIC is implemented in a 0.13um SiGe BiCMOS technology and achieves a 6.7-7.8dB noise figure (NF). The average voltage gain of the receiver is measured as 53dB maximum gain with 20dB continual tuning and 36dB discrete tuning. The average output P1dB, is measured as -10dBm at maximum gain. The receiver dissipates 180mW with a 2.2V power supply.

Chapter 5: Two filter designs are introduced in this chapter. First, a six order Butterworth switched capacitor (SC) low pass filter for NASA application is introduced. Implemented in a 0.5μm SiGe BiCMOS technology, this cryogenic SC filter is capable of operating over an ultra-wide temperature (UWT) range from -180℃ to 120℃ and under high-energy particle radiation environment on the lunar surface. The measured results show that the filter approximates a sixth order Butterworth filter response in range of -180℃ to 120℃. The clock-to-cutoff frequency ratio is 100:1. The clock feedthrough is less than $10uV_{RMS}$ with single 3.3V supply. It consumes only 640uA at 200 kHz clock frequency current and occupies only 0.4x1.4 mm^2. Secondly, a new tunable CMOS resistor is proposed. The resistance is inversely proportional to bias current, to provide the resistor with a wider tuning range. And transistors, which form the active resistor, work at saturation region to achieve very large resistance within a small area. Then, a low pass RC filter using tunable CMOS resistor realized in 0.5-μm CMOS technology is reported. The

measured result shows that the cutoff frequency of low pass filter can be widely tuned from 5 kHz to 1.9 MHz. The total harmonic distortion (THD) stays lower than -40 dB for an input signal up to 100mV Vp-p at 500-kHz input frequency. The die area of the low-pass filter is 0.25×0.13 mm2 and the maximum power consumption (at fc=1.9 MHZ) is 5.7mW with single 3.3-V power supply.

Chapter 6: The dissertation concludes in Chapter 6 with future research topics suggested.

Chapter 2 LOW NOISE AMPLIFIER DESIGN

2.1 Introduction

In modern integrated RF receivers, the low noise amplifier (LNA) is one of the most critical building blocks. There are several design goals for the LNA design including low noise figure, reasonable gain, high linearity, a stable input impedance matching, and low power consumption for portable devices. Satisfying all of the design goals is particularly difficult. For different systems and different architectures, the performance requirement for the LNA is different. In this chapter, two novel LNA designs are introduced: one is Q-enhanced LNA for the applications which require high image rejection ratio, while another is a tunable wideband LNA for self-healing application, which solves the problems introduced by process variations and different environment.

2.2 Q-enhanced LNA design

2.2.1 Introduction

In modern integrated wireless and radar receiver designs, super-heterodyne architecture is one of the most commonly used front-end architectures, since it is capable of providing high performance with superior out-of-band rejection in wireless and radar networks. For super-heterodyne receivers, the problem of images has to be carefully addressed. Since each wireless standard only imposes constraints upon the interested signal, the power of image signals or interferers may be much higher than that of the desired signal, as shown in Figure 2.1. In

addition, for radar applications that experience large jamming signals close to the desired signal, a band-pass filter is usually needed before the LNA to remove those unwanted signals. Due to the low quality of on-chip inductors, pre-filtering is generally done using external passive components such as surface-acoustic wave (SAW) filters. These external filters are large and expensive, and often have high losses. To remove these external components, recent research has focused on the development of monolithic image rejection (IR) using notch filters [1][2]. In this technique, a notch located at the image frequency is used to reject image signals rather than simply relying on bandpass filtering. Unfortunately, the notch filter depth is always limited by the low Q of on-chip inductors, and it is therefore hard to meet the system requirements for image rejection ratio (IRR). Therefore, Q-enhancement technique was developed to provide high IRR with on-chip inductors [3][4].

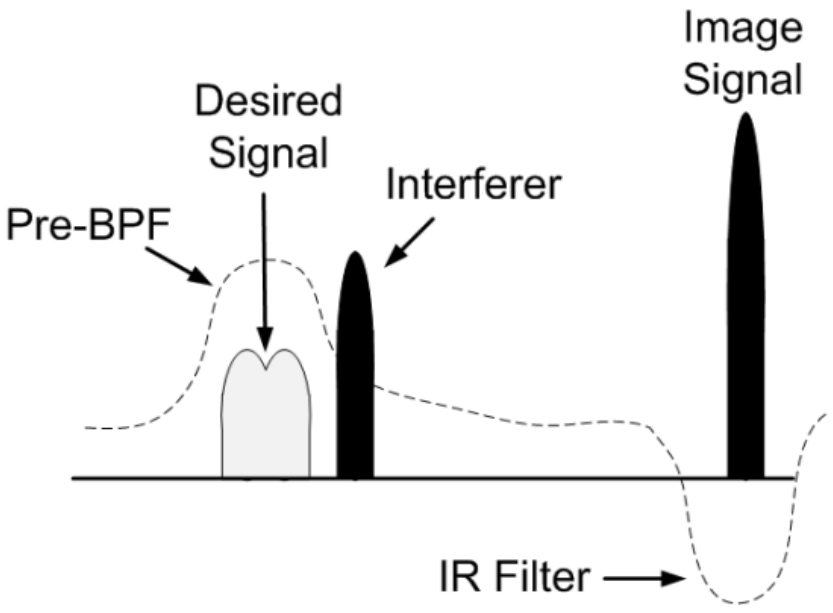


Figure 2.1 Problem of image signals and interferences existing in a super-heterodyne receiver.

In this section, a combination design of the LNA and the notch filter with Q-enhanced technique is presented. As shown in Figure 2.2, the proposed LNA can replace the traditional three stage front-end, providing similar gain, equivalent noise and high IRR. The proposed image rejection LNA is optimized for super-heterodyne applications operating at 7.27GHz with image signal located at 10.96GHz. With the use of an on-chip inductor, the image rejection LNA can achieve power gain larger than 22.5dB, noise figure (NF) lower than 5.1dB and IRR larger than 70dB without any external components. Measured linearity results show -13dBm of the input-referred third-order intercept point (IIP3) and -25dB input-referred 1dB compression point. The circuits dissipate a dc current of 12mA with a supply voltage of 1.7 V.

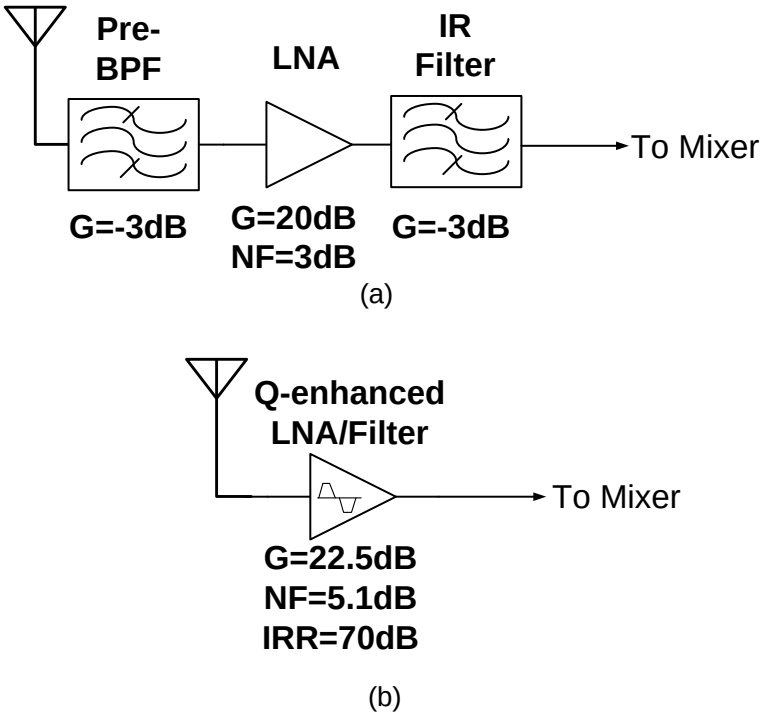


Figure 2.2 Receiver front-end design: (a) Conventional three stage architecture (b) Proposed Q-enhanced LNA/filter.

2.2.2 Q-enhanced LNA and filter deign

The basic idea of the Q-enhancement technique is to utilize a negative gm cell to compensate for the loss of the LC tank and then boost the Q in the lossy tank. Figure 2.3 shows a simplified diagram of the Q-enhancement technique, where Rp represents equivalent parallel loss resistance due to the finite Q of the inductor. With the help of negative gm, the effective Q can be enhanced as

$$Q_{eff} = Q_0 \frac{1}{1 - g_m R_p} \tag{2.1}$$

where Q_0 is the quality factor of on-chip inductor.

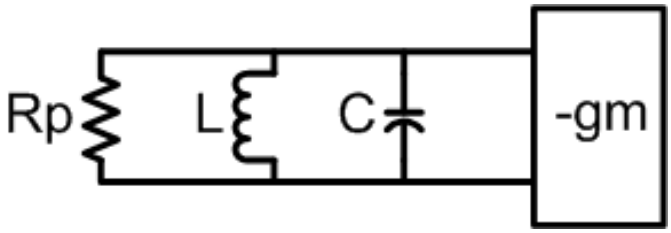


Figure 2.3 Simplified diagram of Q-enhancement technique.

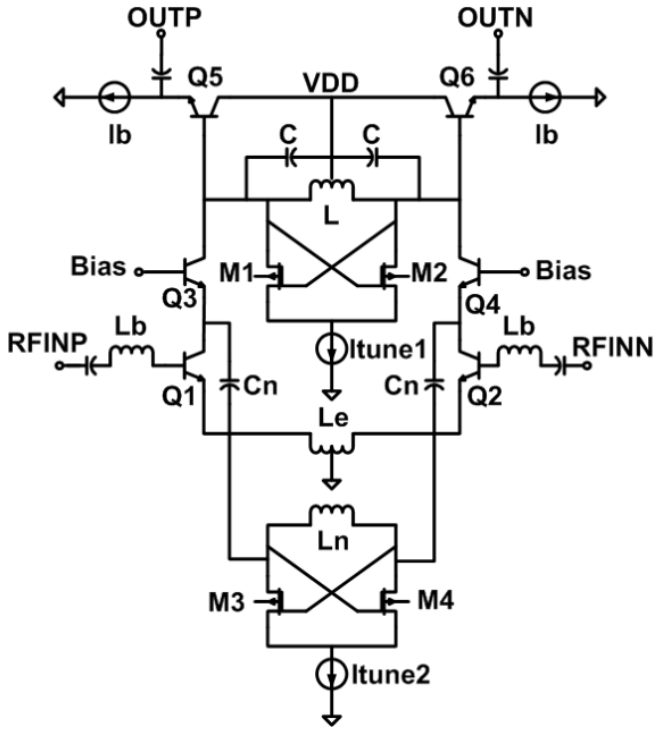


Figure 2.4 Simplified schematic of Q-enhanced LNA/filter.

The proposed Q-enhanced LNA provides the notch effect in a conventional cascode structure with Q-enhancement technique applied to both load tank and notch filter, as shown in Figure 2.4. In the proposed approach, a notch filter was applied to the collector of the driving transistors Q1 and Q2. The notch filtering is realized by capacitors Cn and inductor Ln. The LC circuit resonates at the image frequency and therefore presents very low impedance to the collectors of differential driving transistors. Since the load and the notch filter are in parallel, most of the ac current is steering away from the load path at the image frequency and thus dramatically reduces the gain at that frequency. Unfortunately, there are losses associated with the LC resonator, which greatly affects the notch depth. And the loss of the load tank will limit the bandwidth of the amplifier. Thus, two negative gm cells were applied to the load inductor L and notch filter inductor Ln separately, which can compensate the losses of the resonator and boost the Q. The negative gm cell is formed by a pair of transistors in a cross-coupled configuration. The values of the negative transconductance are designed to be adjusting by means of the control currents I_{tune1} and $I_{tune2.}$

In this design, two input inductors Lb and differential inductor Le are used to provide simultaneous power and noise matching at the operation frequency. The output buffer was added to drive the measurement equipment. The emitter followers Q5 and Q6 form the buffer.

2.2.3 Stability analysis

The stability issue is always a concern for filter design with high Q resonators. Theoretical analysis is derived to examine the margin between current for boosting Q and oscillating. Taking the notch filter as an example, negative resistance is tuned to be equal to the resonator losses,

which is dominated by the loss of inductor. Then the losses can be compensated and a perfect notch filter is achieved. Thus, the control current I_{tune2} can be derived as follows:

$$I_{tune2\_filter} = \frac{2V_T}{R_P} \tag{2.2}$$

where R_p represents the equivalent parallel loss of the notch resonator and V_T is the thermal voltage.

Once the negative resistance cancels all resistance around it, then the circuit will start oscillating. That means the negative resistance must be equal to the combination of resonator's loss and the loading due to the emitters of transistors Q3 and Q4 to start an oscillation [4]. Thus, the current to start an oscillation is given by

$$I_{tune2\_osc} = \frac{V_T}{R_P}(g_{m3}R_P + 2) \tag{2.3}$$

where g_{m3} represents the transconductance of transistor Q3 and is equal to that of transistor Q4. Therefore, the ratio between these two currents is given by

$$\frac{I_{tune2\_osc}}{I_{tune2\_filter}} = 1 + \frac{g_{m3}R_P}{2} \tag{2.4}$$

From Eq. (2.4), it can be seen that there is still a safe margin for the tuning current between Q-enhancement and oscillation. Similar derivation for the Q-enhancement technique can be performed at the load resonator. Thus, both load and notch resonators can be safely tuned to a much high Q avoiding oscillation.

2.2.4 Noise analysis

Using a Q-enhanced LNA to replace the discrete pre-select band pass filter, LNA and image rejection filter simultaneously, noise figure needs to be carefully addressed.

The voltage gain of the amplifier is given by

$$A_v = g_m \cdot R_L \tag{2.5}$$

where g_m is the half-circuit transconductance of the driving transistors while R_L represents the equivalent parallel loss resistance of the load resonator, which is enhanced by the negative g_m cell.

For simplicity, only three major noise sources are considered in our derivation: base shot noise, collector shot noise and the thermal noise from base resistance of the driving transistors Q1 and Q2. In the analysis, the noise due to the notch filter is neglected since it only significantly affects the gain at the image frequency. In another word, it degrades the signal to noise ratio and therefore the noise figure only at the image frequency and doesn't contribute much to the in-band noise.

The following equations present the differential output noise contributed by the source resistance R_S, the base resistance r_b, collector current I_C, base current I_B and the output current from the negative g_m cell, respectively

$$V_{n\_R_S} = \sqrt{4kTR_S} \cdot A_v \cdot \sqrt{2} \tag{2.6}$$

$$V_{n\_r_b} = \sqrt{4kTr_b} \cdot A_v \cdot \sqrt{2} \tag{2.7}$$

$$V_{n\_I_C} = \sqrt{2qI_C} \cdot R_L \cdot \sqrt{2} \tag{2.8}$$

$$V_{n\_I_B} = \sqrt{\frac{2qI_C}{\beta} Z_{eq}} \cdot A_v \cdot \sqrt{2} \tag{2.9}$$

$$V_{n\_I_{tune1}} = \sqrt{2qI_{tune1}} \cdot R_L \tag{2.10}$$

In Eq. (2.9), Z_{eq} is the impedance seen from the input of driving transistor. Eq. (2.10) assumes that the noise produced by the load resonator is dominated by the collector shot noise in the case of negative g_m applied to the resonator.

Then the overall output noise can be expressed as:

$$V_n^2 = V_{n\_R_S}^2 + V_{n\_r_b}^2 + V_{n\_I_C}^2 + V_{n\_I_B}^2 + V_{n\_I_{tune1}}^2 \tag{2.11}$$

Substituting (2.5) – (2.10) into (2.11), and then dividing by the source noise $V_{n\_R_S}^2$ yields the noise factor of the proposed Q-enhanced LNA as

$$F = 1 + \frac{r_b}{R_S} + \frac{1}{2R_S g_m} + \frac{g_m Z_{eq}^2}{2\beta R_S} + \frac{I_{tune1}}{4V_T R_S g_m^2} \tag{2.12}$$

In comparison to a stand-alone LNA, the noise factor of the LNA/filter circuit increases slightly due to the Q-enhanced technology, as shown by the last term of Eq. (2.12). However, it is still acceptable compared to conventional three stages RF front-end architecture.

2.2.5 Experimental results

In this design, a center-tapped symmetrical spiral inductor is used. This geometry provides symmetrical inductors in a single coil. With the differential inductor, the layout becomes more symmetrical and compact in comparison to the two inductors configuration. In order to reduce substrate loss, a ground shield in deep trench is formed underneath the inductor. The ground shield also helps isolate the noise from the substrate.

The wideband LNA was implemented in a commercially-available 0.13μm 200-GHz SiGe HBT BiCMOS technology with a core size of 0.3mm^2. The LNA characteristics were measured

on wafer using SUSS wafer probes. The probes were connected to an Agilent E8364B network analyzer and an N8975A NF analyzer to measure the small signal S-parameters and NF. The measured total DC power consumption is 21mW with 1.7V voltage supply. S-parameters are tested to verify the gain and input matching. As shown in Figure 2.5, the S21 at operating frequency 7.27GHz is 22.58dB. Figure 2.5 also shows a good attenuation of -47dB at the image frequency 10.96GHz. Thus 70dB IRR is achieved in the proposed LNA/filter design without any external components. The measured input reflection coefficient S11 is shown in Figure 2.6. Although there is a slight shift for the input matching, it is still well-matched to be less than -17dB at the operation frequency of 7.27GHz. Measured noise figure of the proposed LNA with notch filter is 5.1dB at 7.27GHz. This noise figure is still small compared to total NF obtained using the traditional three stages architecture, as shown in Figure 2.2. Two tone measurements are performed at the operation frequency to measure the linearity of the IR-LNA. Two tones were applied with equal power levels at 7.265GHz and 7.27GHz. The output power against the input power for both fundamental signals and third order products are shown in Figure 2.7. The measured results indicate -13dBm IIP3 and -25dBm input compression point (P1dB). The performance of the proposed IR-LNA is summarized in Table 2.1 and compared with the state-of-art LNA designs with notch filters. The die photograph of the proposed LNA is shown in Figure 2.8. As shown, the total chip area is 1 mm^2 and the core size is only 0.3 mm^2.

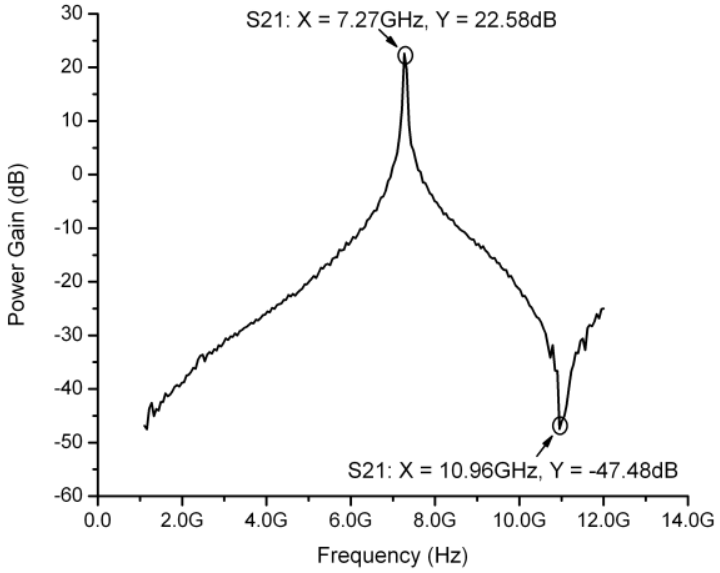


Figure 2.5 Measured S21 of the proposed LNA/filter.

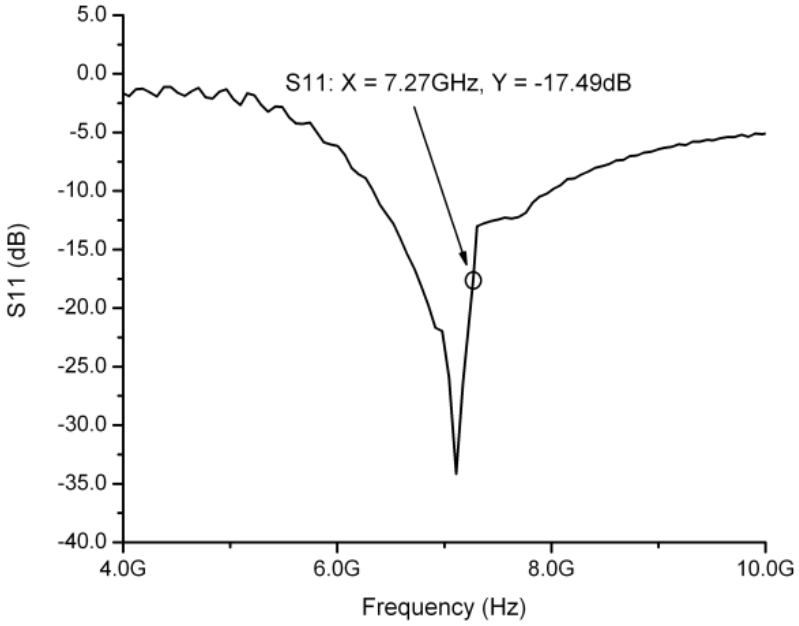


Figure 2.6 Measured S11 of the proposed LNA/filter.

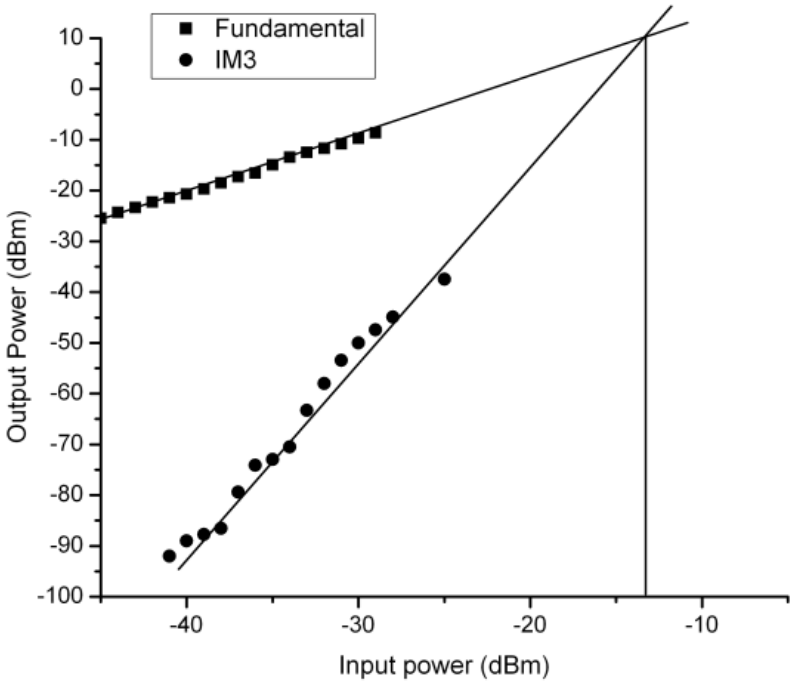


Figure 2.7 Measured IIP3 of the proposed LNA/filter.

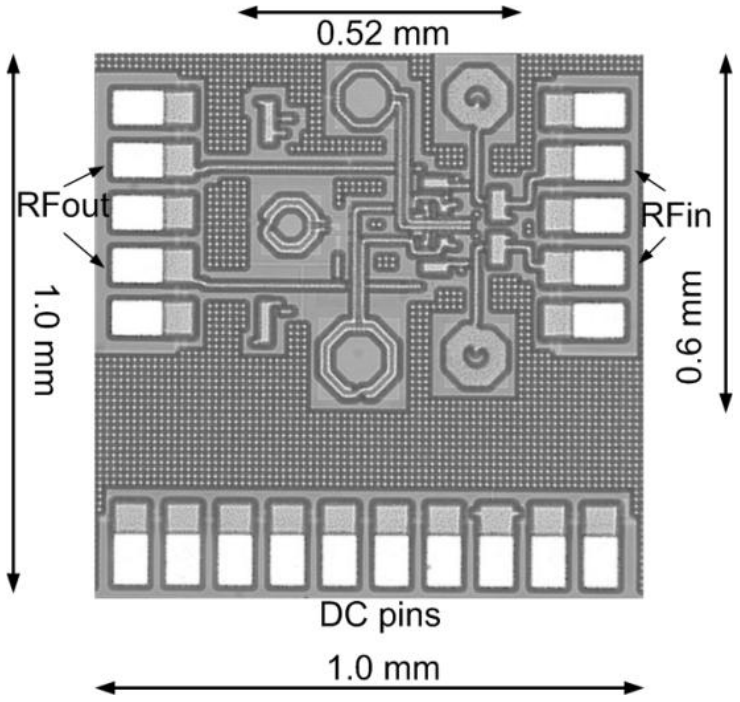


Figure 2.8 Die micrograph of the proposed LNA/filter.

Table 2.1 PERFORMANCE COMPARISON WITH Q-ENHANCED LNA

	Freq (GHz)	S11 (dB)	S21 (dB)	IIP3 (dBm)	IRR (dB)	Technology
[1]	5.0	-12	18	-	12	0.24μm CMOS
[2]	0.947	-10	22	-17	50	0.5μm CMOS
[3]	5.0	-7.5	14	-6	70	50GHz SiGe
This work	7.27	-17.5	22.5	-13	70	0.13μm SiGe

2.2.6 Summary

The prototype design described in this section implements a Q-enhanced 7.27GHz LNA with high image rejection notch filter in a 0.13μm SiGe BiCMOS process. With the help of Q-enhanced technology, the LNA provides good gain of 22dB and an excellent IRR of 70dB without any external components. The proposed LNA RFIC is suitable for the wireless and radar applications where a high degree of integration and high image rejection are desirable.

2.3 A reconfigurable wideband LNA for self-healing application

2.3.1 Introduction

Development of integrated circuit technology, which shows the advantages of increased speed and higher device density, has enabled integration of multiple RF, analog and digital functions in a single chip. However, the scaling-down of technology brings some negative aspects such as the increase of process variations that will directly impact the circuit performance, especially for RF circuits. The changes in environment will also impact the circuit performance. In order to guarantee a sufficient post-fabrication performance yield, designers have to relax the design goals. Although several calibration methods have been proposed in [5][6], they all used extra internal or external tuning circuits, which make the amplifier complicated, bulky and noisy.

On the other hand, for the systems, like software defined radios and UWB which cover multiple standards, the performance requirements for different standards remains significant. Although traditional wideband LNA technology can operate over a wideband frequency range, it is very difficult to meet all the requirements of different standards simultaneously. Moreover, since there is no interference filtering realized in the traditional wideband LNAs, the linearity requirement for those wideband LNAs is extremely difficult [7][8][9].

In this section, a wideband LNA for self-healing application is demonstrated. The tuning of operating frequency is achieved by means of voltage-voltage feedback [10]. A current steering gain tuning approach is applied to the second stage to realize the self-healing of gain. As measured, the proposed LNA covers the entire 4.5GHz to 7.8GHz frequency band with coarse and fine tuning. The proposed LNA achieves a typical power gain of 19dB with 14dB continuous tuning range. The measured input matching is better than -12dB over the entire frequency range. The measured noise figure of the LNA is 4.2dB at 7.8GHz and the output 1dB compression point is -9dBm. The LNA dissipates 52mW power.

2.3.2 Design of a wideband LNA with self-healing

A simplified schematic of proposed self-healing LNA, which consists of two stages, is shown in Figure 2.9. The input stage of the LNA is a common base amplifier with feedback network from the load to the input. Noise matching and input matching are achieved simultaneously in this stage. In addition, self-healing of the operating frequency is realized through the feedback network in this stage. Current steering technology is employed in the second stage to realize self-healing of the gain and achieve higher dynamic range.

Conventional LNAs are usually configured as common emitter topology, which tends to minimize the noise figure (NF). However, since the input impedance of the amplifier is dominated by the parasitic capacitor between base and emitter, the input matching is only achieved in a narrow frequency band with help of the matching network. Previous calibration methods, which focus on tuning of the input matching, are based on this type of architecture[5][6]. The tuning of input matching in their work relies on switching the elements at the input of LNA, which would impact the noise figure. In our design, a feedback solution is utilized to achieve wideband frequency range and self-healing.

Referring to Figure 2.9, the load inductor L_{load}, four-bit switchable capacitor bank including C_a, C_b, C_c, C_d and two identical tunable varactors Var1 and Var2 form the tunable load tank. The tunable load impedance is fed back to the input through a feedback network realized by a capacitor divider. Then the feedback factor is determined by the ratio of $C1/(C1+C2)$. Using feedback theory, the input impedance of proposed LNA can be expressed as:

$$\begin{aligned} Z_{in,loop}(j\omega) &= \left(\frac{1}{g_{m1,2}+\frac{1}{Z_{\pi 1,2}}}\right)\times\left(1+\frac{r_{b1,2}}{Z_{\pi 1,2}}\right) \\ &\quad\times\left(1+\frac{C1}{C1+C2}\times\frac{g_{m1,2}}{1+\frac{r_{b1,2}}{Z_{\pi 1,2}}}\times Z_{load}(j\omega)\right) \\ &\approx \frac{1}{g_{m1,2}}+\frac{C1}{C1+C2}\times Z_{load}(j\omega) \end{aligned} \tag{2.13}$$

where $g_{m1,2}$ and $r_{b1,2}$represent the transconductance and base resistance of input transistors Q1 and Q2 respectively, while $Z_{\pi 1,2}$ represent the impedance between base and emitter nodes. $Z_{load}\,(j\omega)$ is the load impedance and is pure resistance at resonance.

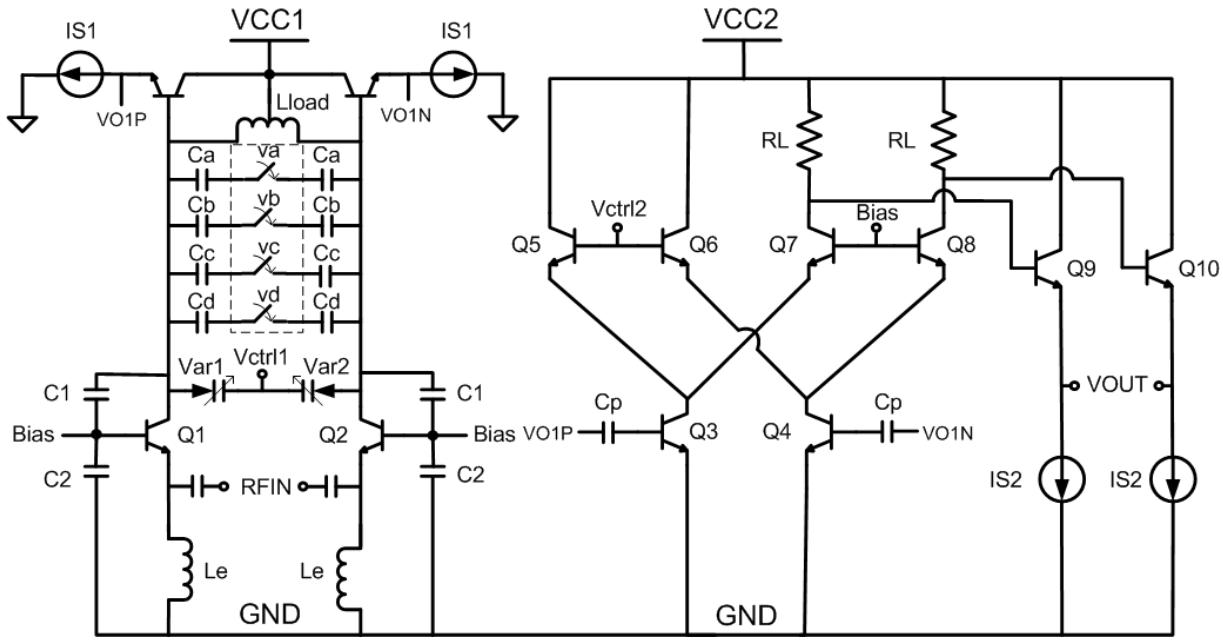


Figure 2.9 Simplified schematic of proposed wideband LNA with self-healing.

Referring to Eq. (2.13), the input impedance consists of two parts: the open loop input impedance of the input transistors $1/g_{m1,2}$ and the feedback impedance, which varies with the resonance frequency of the load tank. In our design, the input transistors were biased at the minimum noise point. The transconductance $g_{m1,2}$is then fixed. By choosing the proper values of feedback capacitors C1 and C2, we are able to match the input impedance $Z_{in,loop}\,(j\omega)$ at the resonance frequency of the load tank. As the load tank is tunable, the peak gain frequency and input matching frequency can be tuned to any interested frequency band.

There are two tuning methods of the operating frequency: coarse tuning and fine tuning. Coarse tuning is realized by the digitally controlled and binary weighted capacitor bank. The

purpose of coarse tuning is to achieve a wideband operating frequency range. Four bit digital control words set the capacitor bank to the desired value. To reduce the influence of parasitic parameters and temperature, MIM capacitors with minimum value of 100fF were used to implement the capacitor bank. To prevent degrading the quality factor of the load tank, the on-resistance of switches must be as low as possible. Thus, switches in our design are realized by large NMOS transistors (130μm/0.13μm) to reduce the on-resistance. In addition, the NMOS switches are configured in differential manner, which reduces the on-resistance of the switches by a factor of 2, as shown in Figure 2.10. However, a large NMOS switch will introduce large parasitic capacitance at the drain and source of the switch. The parasitic capacitance, when the switch is off, will limit the tuning range of the coarse tuning. The two inverters pull the drain and source to a high voltage level when the switch is off. The junction diodes are reverse biased and parasitic capacitance is dramatically reduced.

Through coarse tuning, the input matching frequency and peak gain frequency are adjusted to the operating frequency band simultaneously, based on the application. However, due to the process variation or the environment influence, it is hard to guarantee the operating frequency is tuned to the desired point. Fine tuning, realized by two varactors under the control of signal Vctrl1, adjusts the operating frequency to the desired frequency band. Thus, self-healing of the operating frequency is realized. Careful consideration of the varactors' value is essential to ensure every frequency point in the frequency band is covered. A buffer, formed by emitter followers Q3 and Q4, is added to prevent decreasing the quality factor of the load tank in the first stage.

The second stage of the self-healing LNA is a differential cascode amplifier with current steering technology applied to the upper cascode transistors. Current steering transistors Q7 and

Q8, under the control of signal Vctrl2, control the current flowing to the load. Then the gain of the LNA can be continuously adjusted to generate a stable output. Since the linearity requirement for the second stage is more challenging than the first stage, a higher power supply VCC2 (2.2V) is applied to the second stage and the output buffer, as shown in Figure 2.9.

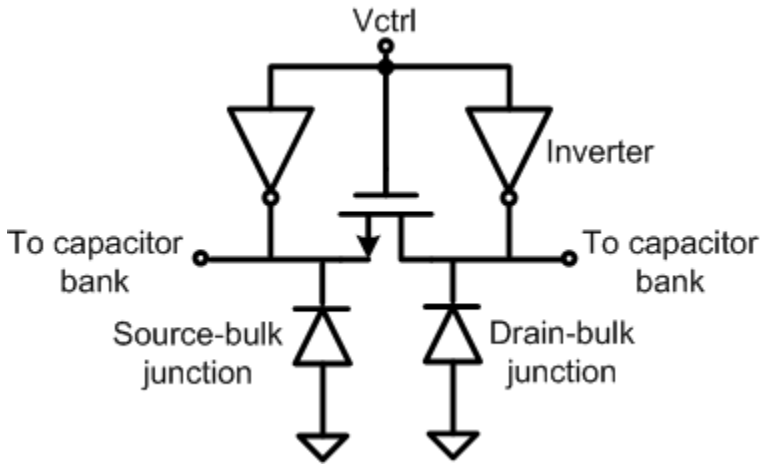


Figure 2.10 Simplified schematic of the switch used in self-healing LNA.

2.3.3 Experimental results

The proposed self-healing LNA was fabricated in a commercial 0.13μm SiGe HBT BiCMOS technology with a peak cutoff frequency (f_T) of 200GHz and a maximum oscillation frequency (f_{MAX}) of 250GHz. The chip consumes an area of 1.1 × 1.24 mm^2 which is limited by pads. The core size is only 0.334 mm^2, as shown in Figure 2.11. The chip was packaged in a 24 pin QFN package and soldered on double-sided FR4 boards. External 180° hybrid couplers are used at the RF input to transform the single ended signal to differential. All strip lines are optimized by means of EM simulation. In the design, a center-tapped symmetrical spiral inductor is used to implement the load inductor of the first stage. This geometry provides symmetrical inductors in a single coil. With the differential inductor, the layout becomes more symmetrical and compact in comparison to a two inductor configuration. To reduce substrate loss, a patterned ground shield is

formed underneath the inductor. The ground shield also helps further isolate the noise from the substrate. Moreover, banks of on-chip decoupling capacitors were located at the termination of DC bias and power to filter out the noise from the reference as shown in Figure 2.11. The measured result shows that the DC power consumption is 52mW with separate 1.5V and 2.2V supplies.

Figure 2.12 shows the measured power gain under different control words. To simplify the test, only reverse thermometer code control words were applied to examine the coarse tuning. As shown, the measured peak frequency of power gain can be adjusted from 4.5GHz to 7.8GHz with coarse tuning. The measured power gain is 19dB, as shown in Figure 2.12. Moreover, the measured adjustment of gain with fine tuning at high frequency band is shown in Figure 2.13. As shown, an approximately 1GHz frequency tuning range is achieved with fine tuning. Measured tuning results of the frequency show that the entire 4.6GHz to 7.8GHz frequency band is covered by coarse tuning and fine tuning together.

In addition to adjustment of operating frequency, the gain tuning is also measured under the control code of 0000. As shown in Figure 2.14, 14dB continuous tuning of gain is achieved by directly changing the control voltage Vctrl2. Input reflection coefficient is measured with Agilent E8364B network analyzer to verify the input matching. Figure 2.15 shows the measured results of S11 with coarse tuning. As shown, S11 is better than -12 dB at all frequency bands, showing good input matching in all interested frequency bands.

Figure 2.16 shows a comparison of the measured and simulated NF of proposed self-healing LNA. The measured minimum noise figure 4.2dB occurs in the high frequency band and increases up to 5.8dB at low frequency. The increase of the NF is because the more capacitors are connected to the load inductor as more switches turn on, which degrade the quality factor of load

tank. The measured NF is about 1.8dB off from the simulation results after parasitic extraction, which is due to the lossy FR4 PCB.

Two tone measurements, under different control words, are performed to examine the linearity of the LNA. The frequency spacing of two tones is 50MHz. As shown in Figure 2.17, the typical output P1dB is -9dBm and the average output IP3 is 4dBm. Since the interference signals can be filter out by the self-healing architecture, the linearity requirement for the LNA is relaxed. Thus, measured linearity will satisfy most of systems' linearity requirement. The performance comparison with other wideband LNAs is summarized in Table 2.2.

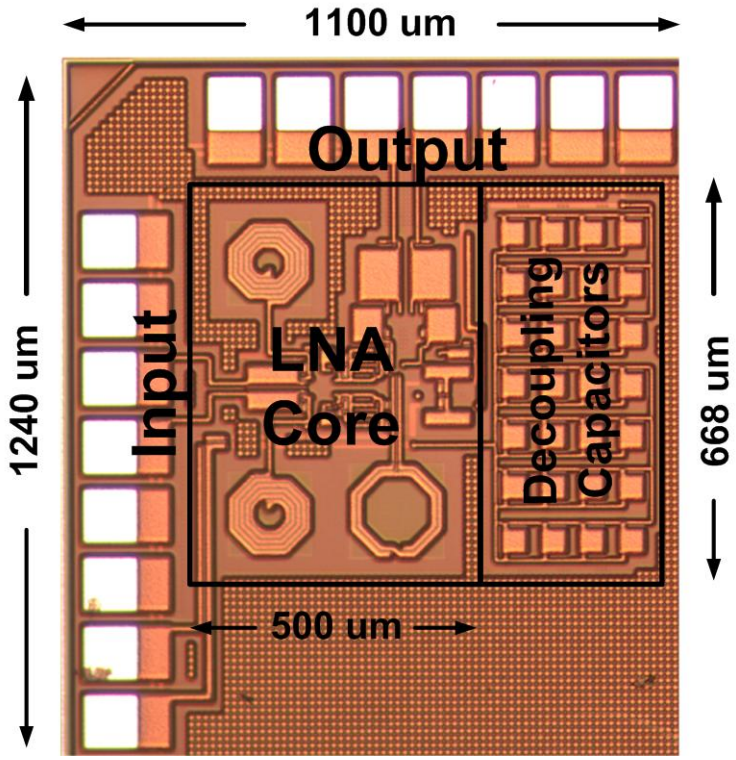


Figure 2.11 Die photography of the proposed self-healing LNA.

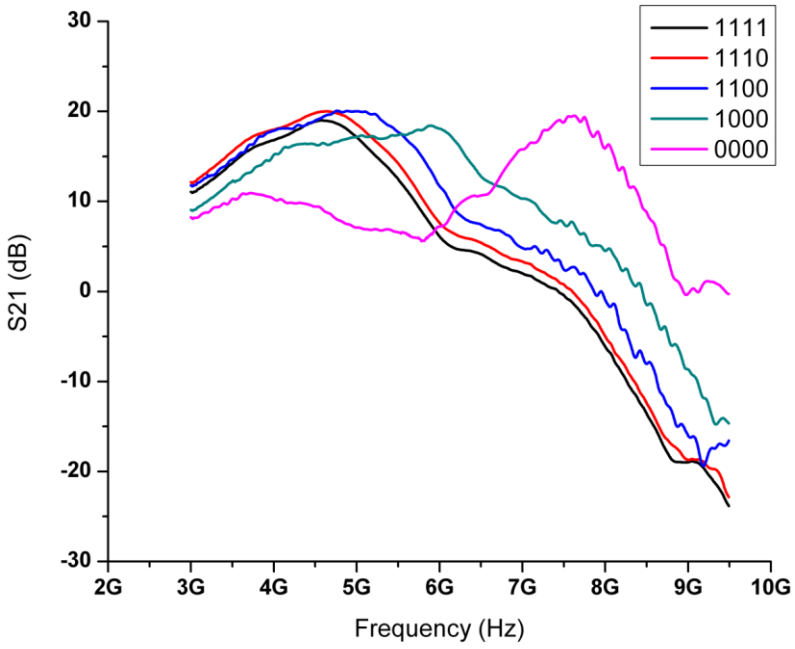


Figure 2.12 Measured S21 of proposed self-healing LNA with coarse tuning of frequency bands.

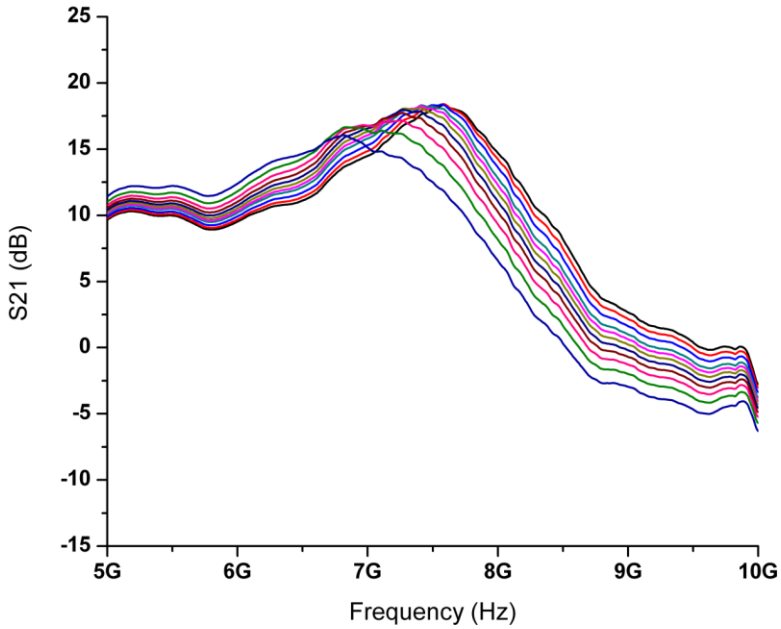


Figure 2.13 Measured S21 of proposed self-healing LNA with fine tuning of frequency bands.

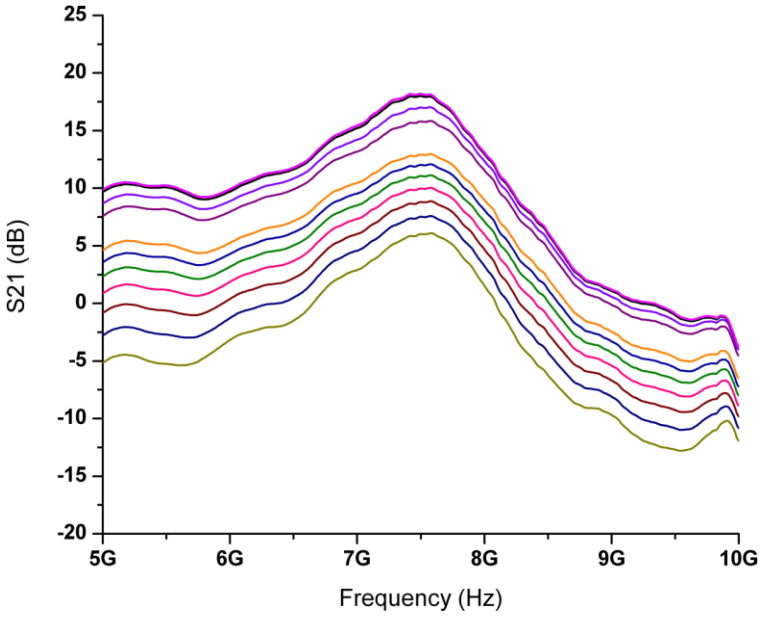


Figure 2.14 Measured gain tuning of proposed self-healing LNA at high frequency band under code 0000.

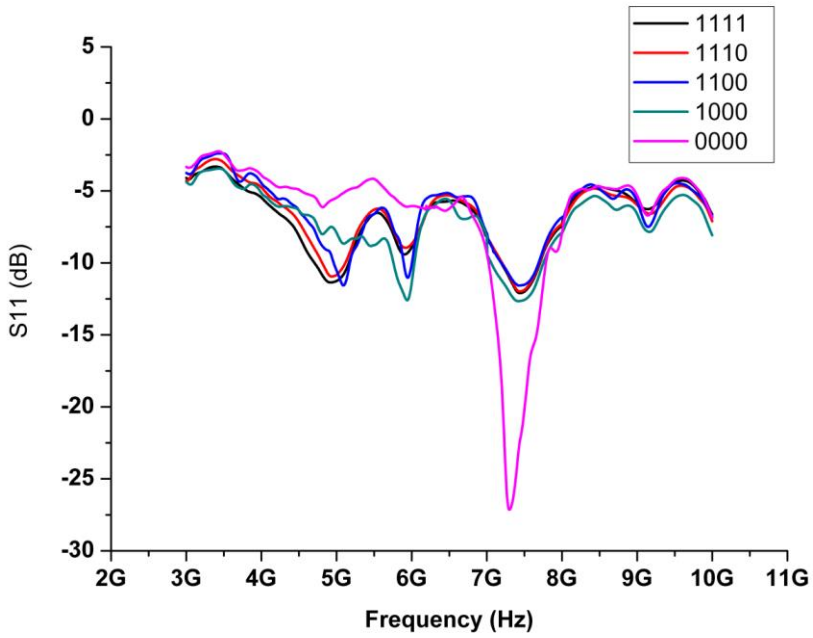


Figure 2.15 Measured S11 of proposed self-healing LNA with coarse tuning of frequency bands.

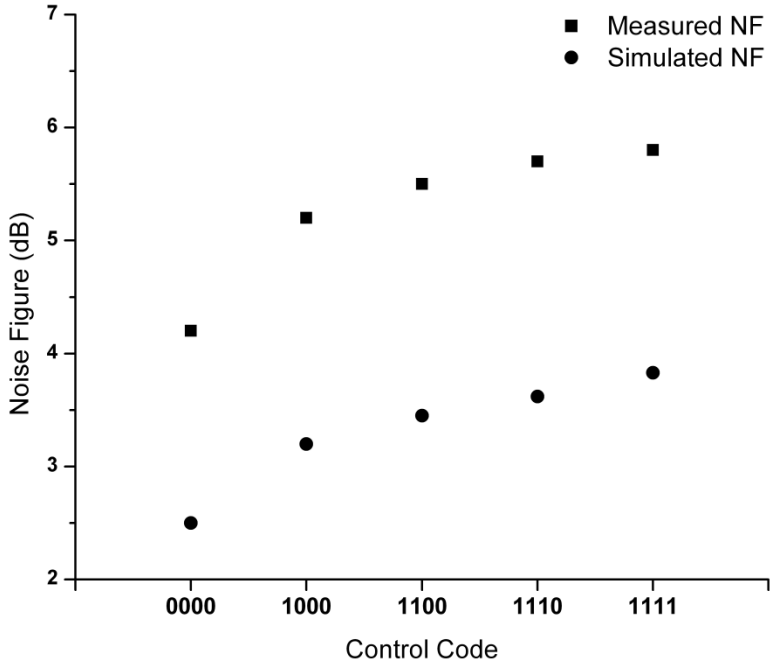


Figure 2.16 Measured NF of proposed self-healing LNA at different frequency bands.

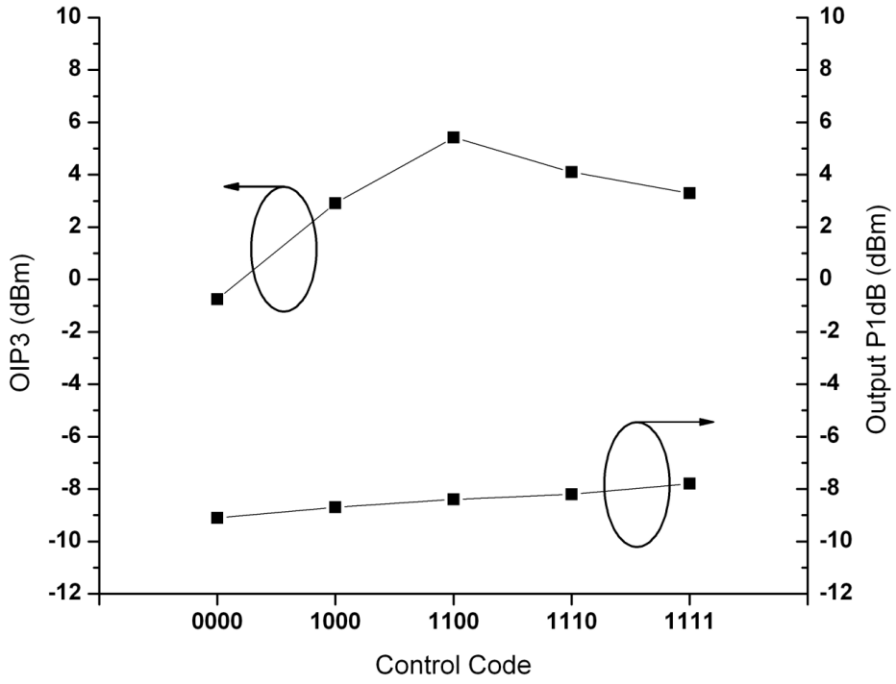


Figure 2.17 Measured linearity of proposed self-healing LNA at different frequency bands.

Table 2.2 Performance summary and comparison with published LNA

	[7]	[8]	[9]	This work
Frequency /GHz	0.8-10.6	2-10	3.1-14.5	4.5-7.8
S11/dB	-12	-10	-1	-12
Gain/dB	16	21	22	19
NF/dB@7.8GHz	4.1	3.3	3	4.2
IIP3/dBm	1.6	-5.5	-32.5	-15
Supply voltage/V	1.5	2.7	3	1.5/2.2
Self-healing	No	No	No	Yes
Process	0.13μm CMOS	0.18μm BiCMOS	0.25μm BiCMOS	0.13μm BiCMOS

2.3.4 Summary

A fully integrated wideband LNA with self-healing technology is designed and fabricated in a commercial SiGe BiCMOS technology. With self-healing, the peak gain frequency and input matching frequency can simultaneously be adjusted to operating frequency. In addition, the gain of proposed self-healing LNA is also adjustable. The proposed seal-healing circuits will allow the LNA to be more robust and make it possible to resemble living organisms in their ability to self-heal and adjust to changes in the environment. Moreover, the proposed self-healing wideband LNA based on feedback technology seems attractive for software defined radio technology, which consists of several frequency bands for different standards. The measured performance of the wideband LNA shows that operating frequency can be adjusted from 4.5GHz to 7.8GHz with 14dB continuous gain tuning. The measured performance of proposed self-healing LNA is comparable to the best reported wideband LNA in a similar operating frequency, giving it a decided advantage for future wideband systems.

2.4 Conclusion

In this chapter two LNAs are presented showing evolutionary design for different applications. Here, certain techniques were required to enhance some performance, like quality factor and self-healing, etc. Both the LNAs are hardware verified and the measured performance is comparable to the best reported LNAs in a similar operating frequency, giving it a decided advantage for future RF receivers and systems.

Chapter 3 DIGITALLY CONTROLLED OSCILLATOR

3.1 Introduction

Recently, digitally controlled oscillators that deliberately avoid any analog tuning control attracted more and more attention for RF wireless applications. This enables a fully digital implementation of the loop control circuitry, such as a phase-domain digital phase-locked loop (DPLL). A DCO which avoids any analog tuning voltage control is presented in this chapter.

3.2 A 12 bits 3.6GHz digitally controlled oscillator

3.2.1 Digitally switched capacitor bank

It is difficult to implement a high resolution DCO due to the limitation of the minimum capacitor size. Recently, there are several DCO designs published, in which weighted binary varactors, which could be switched into a high-capacitance mode or a low-capacitance mode, were used as a switchable device. However, MOS varactors are very susceptible to process, voltage and temperature (PVT) variations.

Compared to MOS varactors, metal-insulator-metal (MIM) capacitors are more accurate and reliable with higher quality factor. However, an accurate MIM capacitor below 100fF is difficult to realize, since the parasitic capacitance is comparable at this capacitance range. This makes the method of switching a MIM capacitor bank seldom used in high resolution DCO design. In the proposed DCO design, the MIM capacitors in a series configuration were utilized to realize the small capacitance.

A simplified diagram of the capacitor array is shown in Figure 3.1. As shown, the oscillating frequency of a DCO is tuned with a coarse, medium, and fine-tuning capacitor bank C_H, C_M, and C_L. The equivalent capacitance of the lower bits is determined by the capacitors (constant capacitor $C_{1,2}$ and tunable capacitor $C_{M,L}$) connected in series. By choosing the proper value of capacitor $C_{1,2}$, a very small capacitance step size can be achieved with reasonable minimum capacitor value of 100fF. High resolution is then achieved. The value of the switching capacitors is pre-distorted to get equal step size.

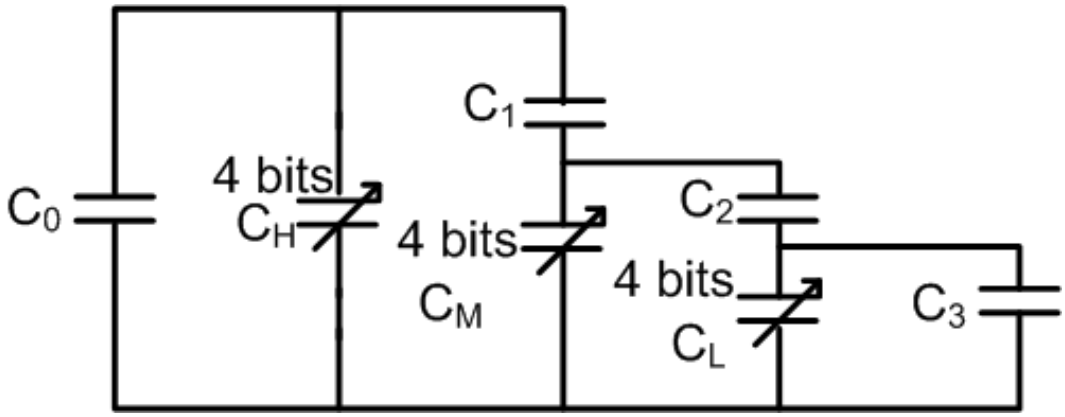


Figure 3.1 Simplified diagram of the switched capacitor bank.

3.2.2 Circuit implementation

Figure 3.2 shows the schematic diagram of the proposed DCO circuit. The DCO configuration consists of NMOS and PMOS cross coupled pairs that provide a negative resistance of $-1/g_m$ to overcome the loss due to the parasitic tank resistance. The transistors are sized such that each pair provides half the transconductance required to overcome the tank loss. The combination of NMOS and PMOS will reduce the power consumption required to achieve the same negative resistance as compared to NMOS or PMOS only topologies.

A digitally controlled oscillating frequency is realized by means of an inductor in parallel with the SC bank. As is well known, the switches used in the SC bank will affect performance of the

oscillator. The on-resistance of the switch must be minized to avoid degradation of the resonator quality factor. In order to get low turn-on resistance, we should make the switching MOS device as large as possible. However, a large device means large drain/source to substrate parasitic capacitance, which determines the minimum capacitance and limits the tuning range of the oscillator. For traditional MOS switches, it is very hard to overcome the tradeoff between on-resistance and drain/source to substrate parasitic. In our design, two additional inverters were added to the switching transistor, as shown in Figure 3.3. With the two additional inverters, we are still able to choose a large MOS transistor as a switch to realize a low turn-on resistance. When the switch is off, two inverters will provide a path to the Vctrl, which is a high voltage. Thus, the drain/source to substrate diode capacitance will be dramatically reduced due to the large reverse voltage, and the capacitance will be dramatically reduced due to the large reverse voltage. A wide tuning range is then achieved.

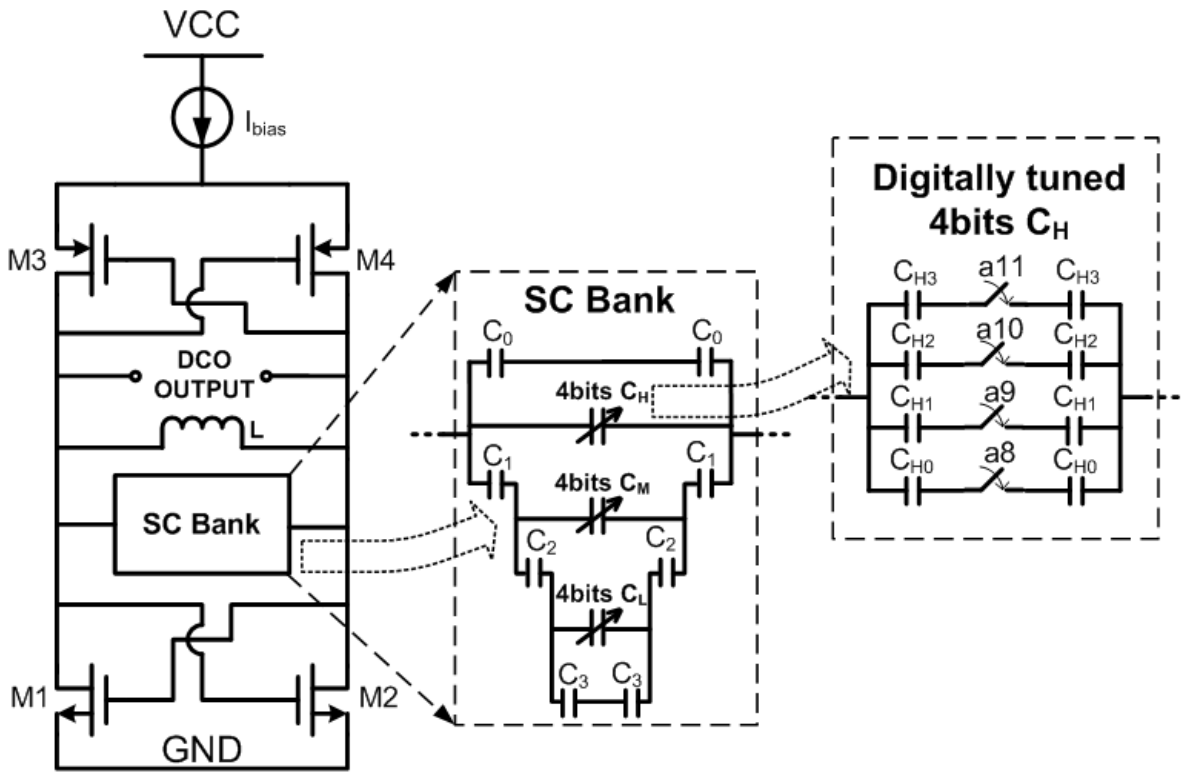


Figure 3.2 Simplified schematic of the DCO.

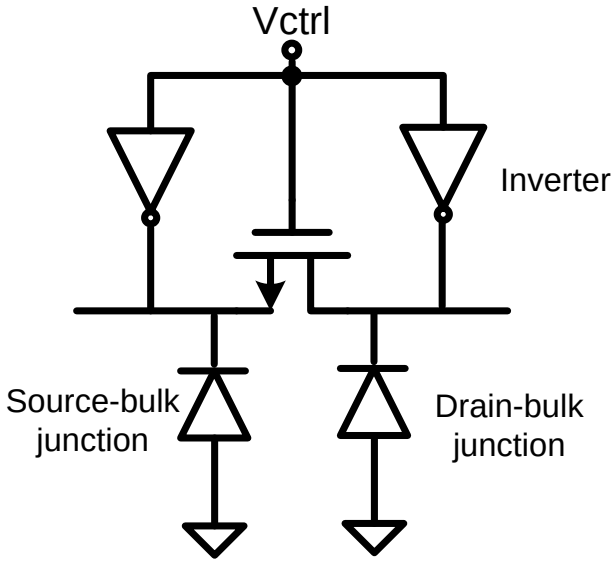


Figure 3.3 Simplified schematic of the switch.

3.2.3 Chip fabrication and experimental results

The proposed DCO chip was designed and fabricated in a 0.18μm CMOS process. Figure 3.4 shows a die microphotograph of the RF DCO within a fully integrated DPLL. As shown, The DCO occupies an area of 0.26×0.46 mm^2. The chip was packaged in a 48-pin QFN package and soldered on double-sided FR4 boards. The strip lines, which connect the DCO output and the SMA connectors, are optimized by means of EM simulation, and banks of on-chip and on-board decoupling capacitors were located at the termination of DC bias and power to filter out the noise from the reference. The measured result shows that the current consumption is 8mA with a 1.5V supply voltage. Figure 3.5 shows frequency tuning of the DCO with variation of 4 bits of high control bits, which control the capacitor bank C_H. As shown in Figure 3.5, the DCO can be tuned from 3.36GHz to 3.77GHz. The frequency tuning with middle band control words is shown Figure 3.6. Figure 3.7 shows the measured results of phase noise of the DCO. The DCO exhibits phase noise of -111dBc/Hz at 1MHz offset. The performance of the proposed DCO is summarized in Table.1.

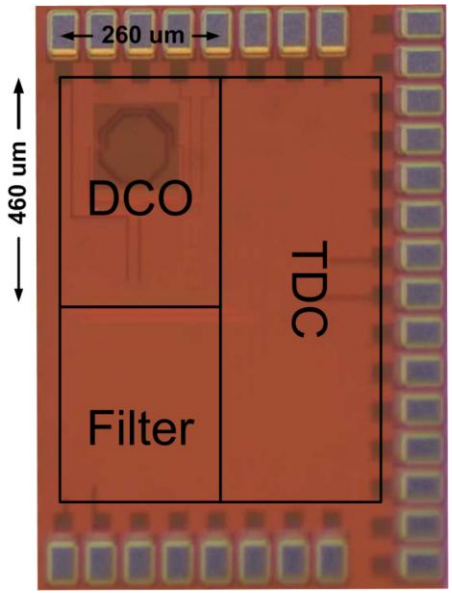


Figure 3.4 Die micrograph of the DCO embedded in DPLL

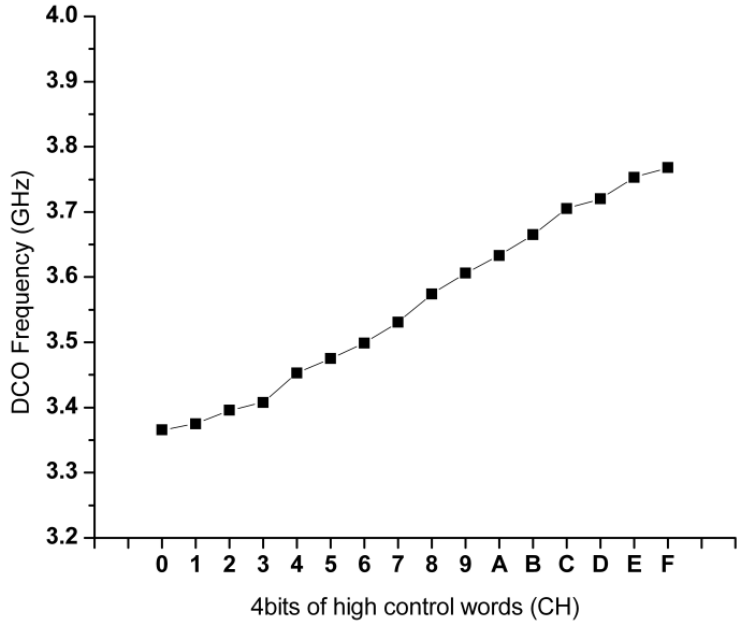


Figure 3.5 Measured DCO oscillating frequency versus 4bits of high tuning code. (4bits of high control bits is tuning while rest 8bits keep zeros)

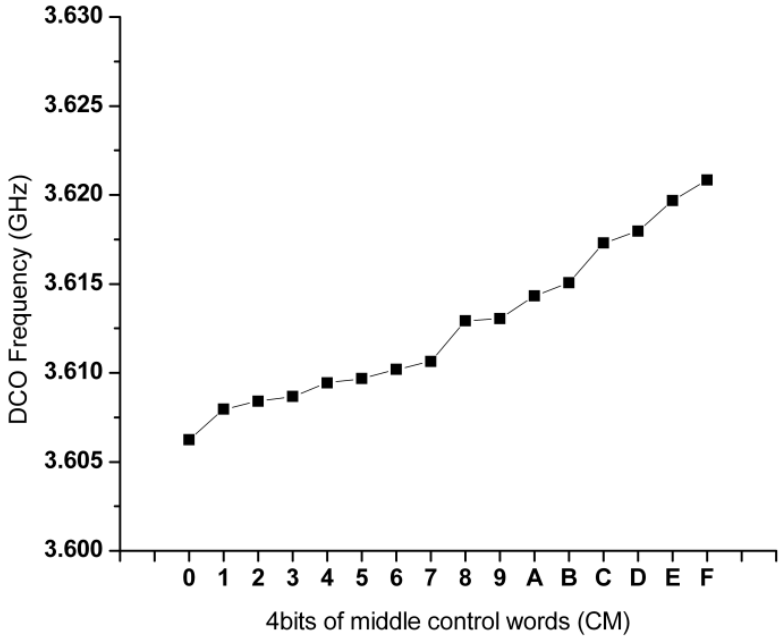


Figure 3.6 Measured DCO oscillating frequency versus 4bits of high tuning code. (4bits of middle control bits is tuning while 4 high bits are 1001 and 4 low bits are 0000).

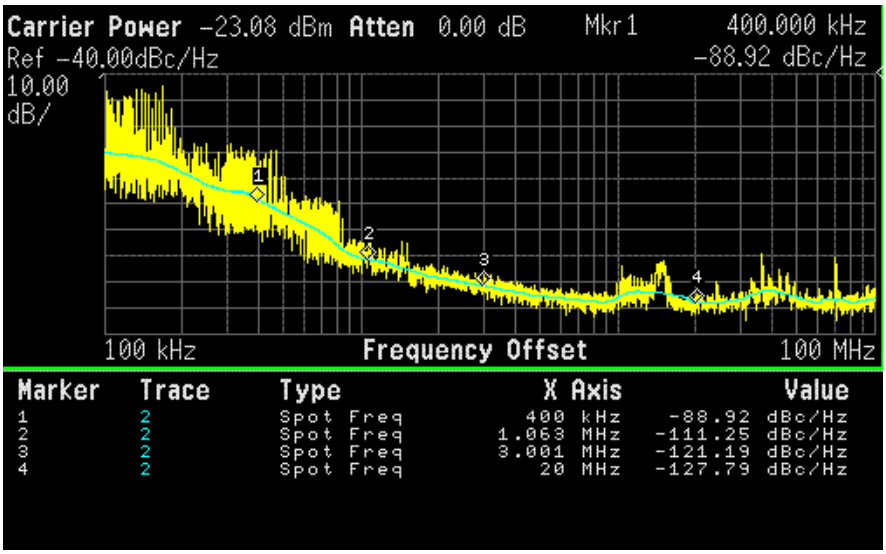


Figure 3.7 Measure phase noise of proposed DCO.

Table 3.1 Measured results of proposed DCO

	DCO
Power Supply	1.5V
Phase Noise	-111 dBc/Hz
Frequency Range	3.36 – 3.77 GHz
Chip Area	0.26 x 0.46 mm^2
Current Consumption	8mA
Technology	0.18um CMOS

3.3 Conclusion

In this chapter, a 3.6GHz 12-bit digitally controlled oscillator fabricated in a 0.13um CMOS technology is presented. The oscillation frequency can be tuned from 3.36 to 3.77GHz with an average frequency resolution of around 0.1MHz/bit. The DCO exhibits phase noise of -111dBc/Hz at the 1MHz offset. The DCO provides a critical building block for future digital implementation of DPLL.

Chapter 4 WIDEBAND RECURSIVE RECEIVER WITH GAIN-REUSE

4.1 Introduction

The development of modern radar and wireless applications require next generation receivers to have wideband frequency range and low power consumption. The 8-to-18GHz frequency band is used by many radar and commercial communication systems, such as X-band and Ku-band radars, as well as ultra-wide-band (UWB) [11] and software-defined radios [12]. The aim of this work is to produce a compact, low power and inexpensive wideband receiver for portable digital wideband radars and other wireless applications. Wideband receiver MMICs with coverage of the entire X-band and Ku-band have been published recently [13][14]. However, their commercial applications are limited due to their high cost, high power consumption and large size. These limitations result from the use of expensive III-V technologies that are not compatible with silicon-based baseband developments. Therefore, the integration of wideband RF blocks with baseband processors on a commercial silicon technology will dramatically reduce the cost of the overall system. The Silicon-germanium (SiGe) Heterojunction Bipolar Transistor (HBT) BiCMOS technology is an excellent candidate that utilizes bandgap engineering to improve transistor performance while maintaining compatibility with low cost CMOS baseband implantation [15]. The receiver presented in this chapter is implemented in a commercial SiGe HBT BiCMOS technology featuring a 0.12 μm lithography, a peak cutoff frequency (f_T) of 200 GHz and a maximum oscillation frequency ($f_{\max}$) of 250 GHz.

In the proposed receiver design, a multi-feedback topology in conjunction with inductive compensation is applied to the LNA design to achieve wideband operation. For the super-heterodyne mixing stages, the gain reuse topology [16], that employs recursive signal amplification through the same transconductance (Gm) stage, is chosen. In addition, a current steering gain adjustment approach is applied to the Gm stage[17]. Thus, the Gm stage is not only operating as an input stage for two mixers, but also as a variable gain amplifier (VGA). The VGA simultaneously adjusts the RF and IF signals utilizing the wide bandwidth of the Gm stage and sufficient separation between RF and IF frequencies. Multi-functions are realized in a single block. With recursive gain adjustment, the proposed super-heterodyne receiver achieves significant tunability enhancement and power savings simultaneously.

The phase-array receiver based on SiGe BiCMOS technology in [18] shows an excellent performance in X- and Ku-band frequency range. However, there is no frequency translation and gain tuning realized in their receiver. In this chapter, the wideband receiver MMIC is implemented in a 0.13μm SiGe BiCMOS technology and achieves a 6.7-7.8dB noise figure in the 8-18GHz frequency band that covers the entire X- and Ku- bands. The maximum voltage gain of the receiver is measured as 53dB. The average output, P1dB, is about -10dBm at maximum gain over the entire operational frequency range. The receiver MMIC occupies 1.81 mm^2 and dissipates 180mW with a 2.2V power supply in maximum gain mode.

4.2 Receiver architecture design

In modern wireless receiver design, there are three common architectures: direct conversion, super-heterodyne and low intermediate frequency (low IF), as shown in Figure 4.1. The direct conversion architecture is widely used in many state-to-art receivers for its simple architecture

[19] [20]. This type of architecture requires only one mixer and lends itself well to compact implementation. However, its classic drawbacks are large flicker noise, large DC-offset and the need for high quadrature matching, which makes the achievement of high performance more challenging.

For applications with high performance requirements, the super-heterodyne architecture is normally the first choice due to the attendant low design risk [21] [22]. However, the main disadvantage of this architecture is the high cost and high power consumption. Since this architecture requires more than one mixer and usually multiple VGAs, it consumes more power when compared with other receivers. This effect makes the super-heterodyne architecture unsuitable for low power applications. Another issue introduced by the super-heterodyne architecture is the image signal, which must be removed in order to prevent degrading the sensitivity of the receiver.

As a compromise between above two architectures, the low-IF receiver topology was developed. This architecture has many of the desirable properties of the direct conversion architecture, but avoids the DC offset and flicker noise problems [23]. Nevertheless, the use of a non-zero IF re-introduces the image issue. The image signal in low-IF architecture is very close to the desired signal and is more difficult to remove, especially at high operating frequency. Moreover, in comparison to a super-heterodyne, the low-IF topology usually requires a high dynamic range, high linearity analog-to-digital converter (ADC) to process the IF signal, which limits its utilization [24]. In order to achieve good performance at a high operating frequency and relax the requirement for the ADC, the super-heterodyne architecture is chosen in the proposed receiver. In addition, some particular techniques, like wideband LNA and recursive gain re-use

topology, are applied to the receiver circuit design. Then the natural drawbacks of the super-heterodyne receiver can be overcome.

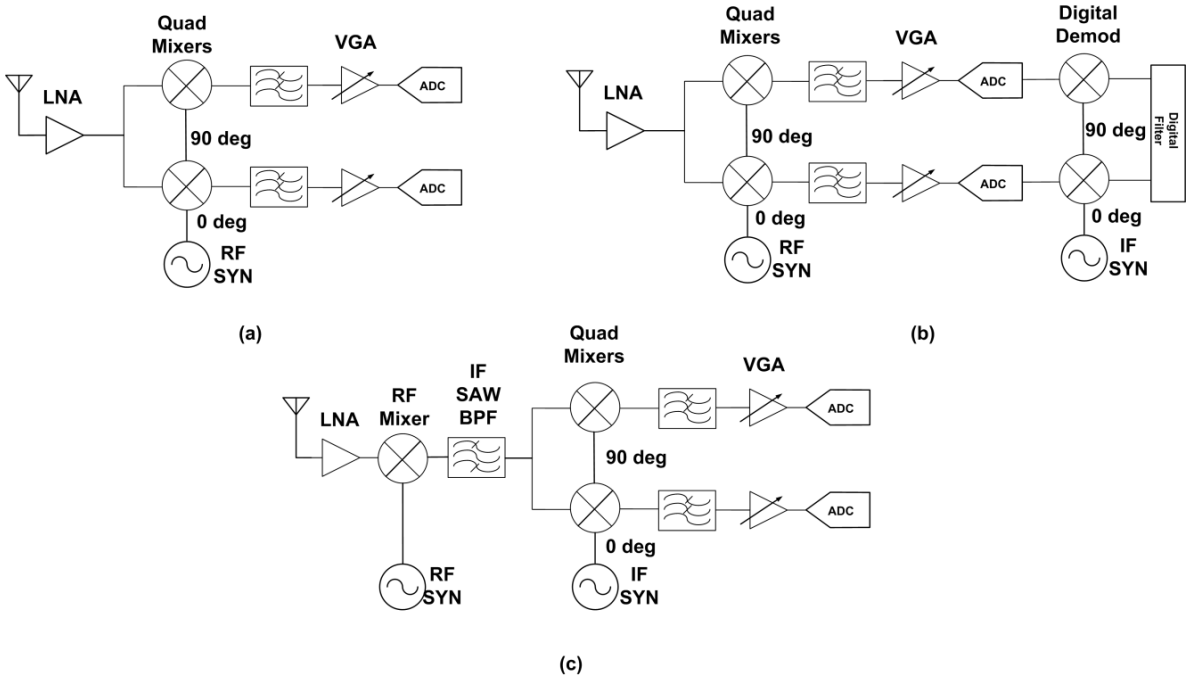


Figure 4.1 Basic receiver architectures: (a) Direct conversion receiver. (b) Low-IF receiver. (c) Super-heterodyne receiver.

Figure 4.2 illustrates the system block diagram of the proposed wideband recursive receiver, which consists of a wideband LNA, two mixers, some internal and external filters and a baseband VGA. The input X-band and Ku-band RF signal is amplified by a wideband LNA. The amplified RF signal is adjusted in the Gm/VGA cell and then down converted to the first IF (IF1). The first IF output is fed back to the input of the same Gm stage through an external SAW filter. Thanks to the high performance of the SiGe HBT technology, a very wide gain bandwidth can be easily achieved in Gm/VGA stage. Figure 4.3 shows the simulated frequency response of the tunable Gm stage at different gain settings. As shown, the gain bandwidth of the Gm stage is approximately 83GHz at different gain modes. This gain bandwidth is wide enough to easily

adjust both RF and IF1 signals. Then both input RF and feedback IF1 signals can share the unique gain stage. After re-amplifying, the first IF signal is down converted again to the second IF (IF2), which is adjusted in the baseband VGA and then quantized by the ADC.

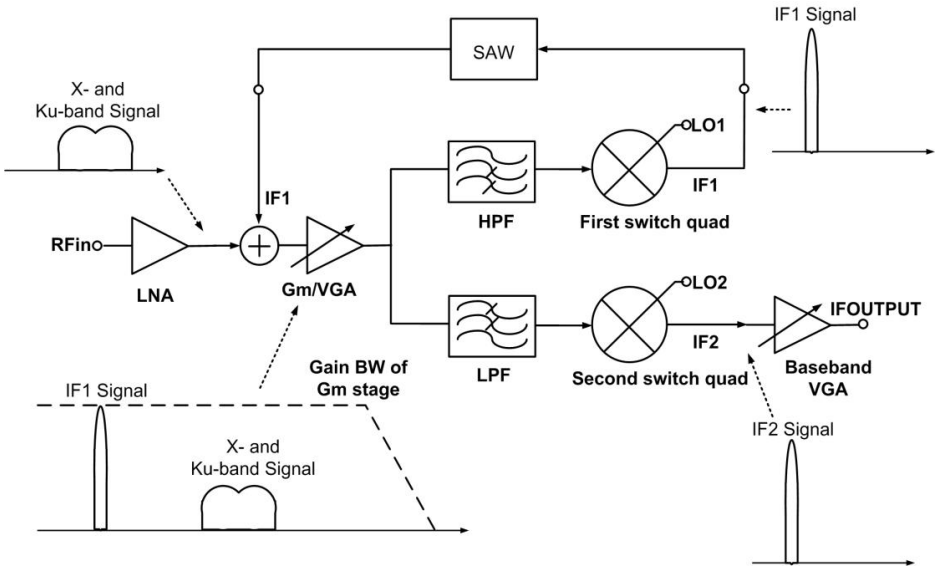


Figure 4.2 Block diagram of the wideband recursive receiver.

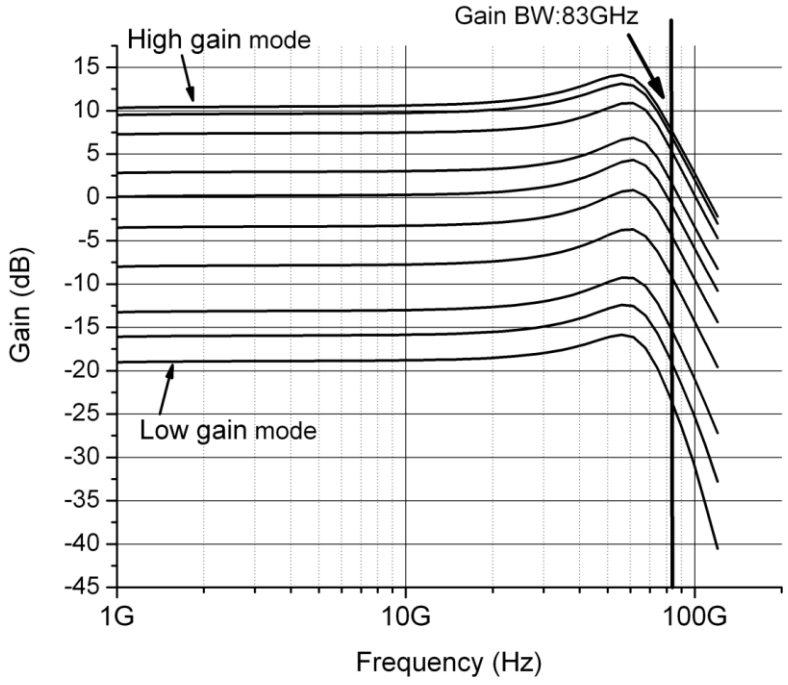


Figure 4.3 Simulated frequency response of tunable Gm stage.

In order to overcome the disadvantages of a super-heterodyne architecture, the following design issues are addressed:

1) To save cost, the proposed receiver, especially the input LNA, can operate over a wide frequency range without splitting the frequency band into a number of sub-bands. This leads to a compact and power-saving implementation.
2) The issue of high power consumption is addressed by the gain re-use topology, which is applied to the super-heterodyne mixing stages. The recursive gain re-use topology makes it possible to achieve multiple functions in a unique stage for power and cost saving purposes.
3) The image signal is removed by employing an external surface acoustic wave (SAW) filter in the feedback loop. For some applications that experience large jamming signals, especially for radar, it's often difficult to remove the image and jamming signals using an on-chip filter due to the poor quality factor of the inductor. For additional image-rejection and channel filtering, the receiver chip provides an option of routing the signal through an off-chip filter which also provides access to the RF and IF signals for separate testing purposes.
4) The issue of local oscillator (LO) leakage is eliminated by using cascode LNA and Gm/VGA circuits that provide high isolation between input and output. In addition, deep trench (DT) isolation rings were located around each cell and critical transistors to suppress substrate crosstalk.
5) A double-balanced configuration is chosen in the mixer design to eliminate even-order distortion, thus relaxing the half-IF issue in the receiver [24]. In addition, careful layout including symmetric tracing of differential signals, also helps suppress the even-order distortion.

4.3 Receiver circuit design

4.3.1 LNA design

In the design of wideband LNAs in modern receivers, there are several considerations that include a low NF, flat gain over the operating frequency range, stable input impedance matching, sufficient linearity and low power consumption for portable systems. Satisfying all of the design goals for the LNA over X- and Ku-bands is particularly difficult, because of the high operating frequency and the broad bandwidth compared to conventional LNAs. A few existing topologies that can provide flat gain over a wide frequency band include LNAs using LC-ladder matching network [8] [25], distributed amplifiers [26][27][28], common-base LNAs [9][7] and an LNA with reactive feedback [29]. However, all of these technologies have some drawbacks when they are operating at X- and Ku-band frequency range. The LC-ladder matching technology occupies large area, and the noise figure is also large due to bulky and lossy on-chip inductors. Although the distributed amplifier can achieve the widest bandwidth, the inherent poor noise performance and large power consumption limit its application. The noise figure of common-base LNAs decreases quickly with frequency, which makes it unsuitable for X- and Ku-band application.

In comparison with above LNA topologies, the shunt feedback topology is a good candidate because wideband input matching is easy, chip size is small, and there is low sensitivity to process variations with the use of precision resistors [28][30][31][32][33][34]. However, feedback can degrade the noise figure for input matching and consume large amounts of current in order to achieve the desired gain, especially in CMOS technology. The SiGe HBT technology offers the advantages of excellent noise performance and an improved transconductance over CMOS devices [15]. These major advantages can be employed to overcome the limitations of the shunt feedback topology. In addition, the multi-feedback topology, in conjunction with inductive compensation, is chosen in the LNA design to achieve wideband input impedance matching with

low NF.

A simplified schematic of the proposed wideband LNA, which consists of three stages, is shown in Figure 4.4. The input stage of the LNA is a single-ended cascode amplifier which achieves simultaneous power and noise matching over the wide bandwidth. Although a differential architecture provides high linearity and common-mode rejection, a differential input makes the testing very difficult when the network analyzer only supports a single-ended port. Thus, in our design, a single-ended input and differential output architecture is chosen. Besides improving reverse isolation, the cascode architecture reduces the Miller capacitance of input transistor, which degrades the wideband impedance matching. Three different feedback paths are provided in this design to achieve the input matching: emitter degeneration feedback R_{e1}, local shunt feedback R_{f1} and global shunt feedback R_{f2}, as shown in Figure 4.4. Among these feedback resistors, feedback resistor R_{f2} is the main component that not only determines the input impedance but also affects the overall noise figure of the amplifier.

The feedback resistor directly contributes noise to the amplifier and the noise design needs to carefully address mitigatation of the noise contribution of the feedback resistor and reduce the overall noise figure of the LNA.

As we know, the noise factor of an N-stage system is given as: [35]

$$F = F_1 + \frac{F_2 - 1}{A_1} + \frac{F_3 - 1}{A_1 A_2} + \cdots + \frac{F_N - 1}{A_1 A_2 \cdots A_{N-1}} \tag{4.1}$$

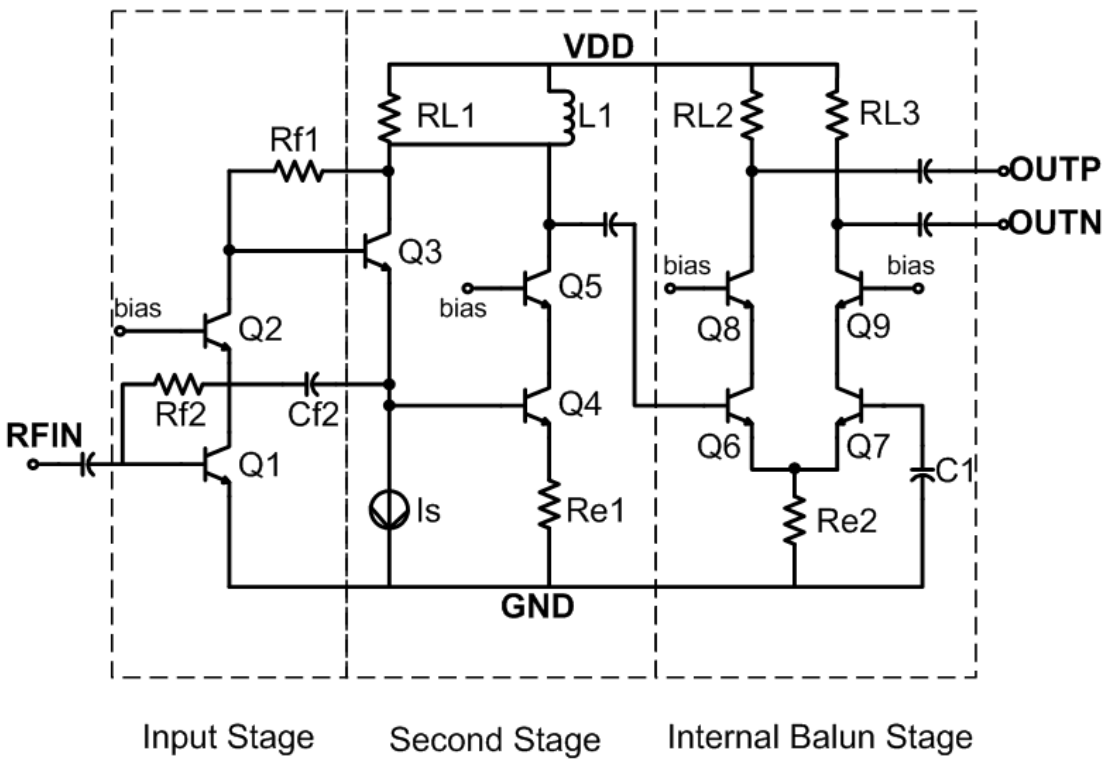


Figure 4.4 Simplified schematic of the wideband LNA.

Based on the above equation, it is clearly necessary to reduce the noise of the input stage, which is the dominant factor of the noise figure for the whole amplifier, even the whole receiver. Thus, in the following noise analysis, the noise performance of the input stage is first analyzed and then combined with noise theory of shunt feedback to evaluate the overall noise figure of the LNA.

The input referred noise voltage $\overline{V_{Q1}^2}$ and noise current $\overline{I_{Q1}^2}$ are used to characterize the noise figure of input transistor Q1. The equivalent input noise voltage and current of the input transistor are given by: (neglecting the noise contribution from cascode transistor Q2)

$$\overline{V_{Q1}^2} \approx 4kT(r_{b1} + \frac{1}{2g_{m1}})\Delta f \tag{4.2}$$

$$\overline{I_{Q1}^2} = \left(2qI_{B1} + \frac{2qI_{C1} + \dfrac{4kT}{\left(R_{f1} + R_{L1}\right)}}{\left|\beta(jf)^2\right|} \right) \Delta f \tag{4.3}$$

Where r_{b1} and g_{m1} represent the base resistance and transconductance of the transistor Q1, respectively. Then the noise figure of Q1 without shunt feedback can be written as: [36]

$$NF_{Q1} = 1 + \frac{\overline{V_{Q1}^2}}{4kTR_S\Delta f} + \frac{\overline{I_{Q1}^2}}{4kT\dfrac{1}{R_S}\Delta f} \tag{4.4}$$

where R_S represents the source impedance.

In order to minimize the noise figure, there is no degeneration resistor located at the emitter of the input transistor Q1. On the other hand, the shunt feedback resistor R_{f2} senses the current and feeds it to the input. Thus, R_{f2} only affects the input referred noise current without disturbing the input referred noise voltage. Then the total input referred noise current can be given as:

$$\overline{I_{total}^2} = \overline{I_{Q1}^2} + \frac{\overline{V_{Q1}^2}}{R_{f2}^2} + 4kT\frac{1}{R_{f2}}\Delta f \tag{4.5}$$

With both input referred noise current and voltage, the overall noise figure of the amplifier can be derived as follow: (the noise contribution of following stages is neglected)

$$
\begin{aligned}
NF_{total} &= 1 + \frac{\overline{V_{Q1}^2}}{4kTR_S\Delta f} + \frac{R_S\overline{I_{Q1}^2}}{4kT\Delta f} + \frac{\overline{V_{Q1}^2}R_S}{4kTR_{f2}^2\Delta f} + \frac{R_S}{R_{f2}} \\
&= 1 + (r_{b1} + \frac{1}{2g_{m1}}) \cdot \left(\frac{1}{R_S} + \frac{R_S}{R_{f2}^2} \right) \\
&\quad + \frac{R_S}{4kT} \left(2qI_B + \frac{2qI_{C1} + \frac{4kT}{\left(R_{f1} + R_{L1}\right)}}{\left|\beta(jf)^2\right|} + \frac{4kT}{R_{f2}} \right)
\end{aligned}
\tag{4.6}
$$

From Eq. (4.6), feedback resistor R_{f2} is limited to large value in order to avoid degrading overall noise figure. On the other hand, the input transistor Q1 must be sized at which minimum noise figure is achieved. Referring to the Eq. (4.6), if we further neglect the noise contribution of the current noise contribution from the base and collector of Q1, the overall noise figure can be simplified as:

$$
NF = 1 + \frac{R_{EQ1}}{R_S} + \frac{R_S \times R_{EQ1}}{R_{f2}^2} \tag{4.7}
$$

Where

$$
R_{EQ1} = r_{b1} + \frac{1}{2g_{m1}} \tag{4.8}
$$

From the simplified expression of overall noise figure, we can see that the overall noise figure is dominated by the base resistance and bias current of Q1.

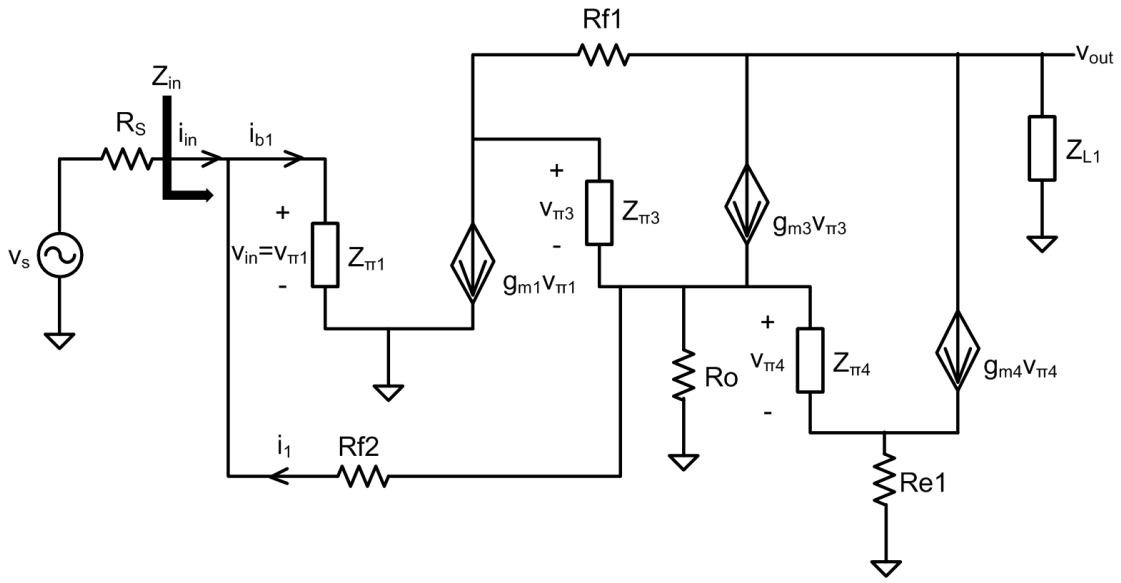


Figure 4.5 Equivalent small signal model of first two stages of the wideband LNA. In the model, the cascode transistors were replaced with single common emitter transistor for simplicity.

With this type of amplifier, it is advantageous to feedback to the input from the emitter of Q3 instead of the collector of Q2. This choice will provide some inductance at the input, which tends to make for a better match. Since there are several feedback paths in our design, it is very hard to derive the input impedance through general feedback theory. Therefore, direct derivation of the input impedance based on the equivalent small-signal model is performed to examine the input impedance of the wideband LNA. Figure 4.5 shows the equivalent small signal model of the first two stages of the wideband LNA, which are associated with input impedance. In the equivalent model, cascode transistors are replaced with single common emitter transistor to simplify the derivation. Using the small-signal model shown in Figure 4.5, the input impedance of the amplifier can be written as:

$$Z_{in} \approx \frac{R_{f2}}{1+\frac{R_{f2}}{Z_{\pi 1}}+g_{m1}\left(R_{e1}+r_{e4}\right)\left(1+\frac{R_{f1}}{Z_{L1}}\right)} \tag{4.9}$$

where Z_{L1} represents the parallel combination of R_{L1} and load inductor L1. Compared to the total impedance of R_{f1}, the variation of Z_{L1} with frequency is very small. g_{m1} represents the transconductance of the input transistor Q1 while r_{e4} is the equivalent small-signal emitter resistor of transistor Q4. As Eq. (4.9) indicates, feedback transistors R_{e1}, R_{f1} and R_{f2} all play important roles in the input impedance. So input matching can be achieved by carefully choosing the value of these feedback resistors. Compared to a traditional shunt feedback architecture in which the input matching is only determined by the shunt feedback resistor and the gain of the amplifier, the proposed wideband LNA design provides more control parameters to adjust the input impedance, which means more freedom of achieving input matching. It helps break the trade-off between input matching and noise minimization.

In order to cover the entire X-band and Ku-band frequency range, the overall gain should be flat over the entire operating frequency range. However, the collector current from the transistor rolls off inversely with frequency. The inductive load can help equalize the voltage gain over the wide bandwidth. Then the bandwidth at high frequency can be widened. In addition, the load inductor also provides more headroom to achieve higher linearity.

The second stage of the LNA is a combination of a common-collector amplifier and a cascode amplifier, which operates similarly to the common-collector-common-emitter (CC-CE) configuration. The only difference to CC-CE is that the collector of Q3 is connected to the output of second stage instead of the power supply, which will reduce a little effective output resistance of the second stage because of the feedback through Q3. With this implementation, the effective current gain of the basic transistor is increased. Referring to Eq. (4.6), the collector shot noise is directly related to the current gain and the collector shot noise of the second stage can be dramatically reduced with boosted current gain. The overall noise figure of the wideband LNA is

further improved. Meanwhile, the noise term corresponding to the collector shot noise is frequency dependent. Thereby, the noise contribution of second stage at high frequency is also reduced. Furthermore, degeneration resistor R_{e1} was added to the second stage to improve the linearity performance, in addition to input matching.

The differential cascode architecture in the output stage transforms the single-ended signal to a differential output. Compared to an external balun, the internal single-ended to differential transformation makes the receiver more compact with lower noise figure. Since the unbalanced to differential transformation in our design is performed at the output of the amplifier, it contributes much less noise to the overall LNA, compared to the architecture where transformation occurs at the input of the amplifier [18].

In this stage, resistor R_{e2} was utilized to reject the common-mode signal, then ac current is forced to flow through Q6 and also Q7, thereby creating an approximate 180^{o} phase shift in differential paths. Although a tail current source realized by nMOS transistor can save some headroom requirement, the capacitance of the tail current transistor will cause common-mode capacitive degeneration. This capacitive degeneration, through impedance transformation performed by the transistors Q6 and Q7, can easily trigger the common-mode oscillation at high operating frequency. The equivalent output impedance of tail current is comparable to degeneration resistor at X- and Ku-band frequency range. Thus, degeneration resistor R_{e2} was chosen in our design, instead of a tail current source. As the two branches are under the same bias conditions, roughly identical output amplitudes will be achieved.

In the circuit implementation, the parasitic influence around the inductor was minimized to ensure self resonance occurs beyond the operating frequency and banks of decoupling capacitors

were located at the termination points of the DC bias and power supply in order to filter out the noise from the reference.

4.3.2 Mixers with gain reuse

The dual-conversion gain-reuse mixers are based upon a folded mixer architecture, and are composed of the Gm stage, two switching quads and some internal and external filters, as shown in Fig. 4.6. The folded approach is chosen for operation at low supply voltage to reduce the power consumption of the whole receiver. Moreover, the folded topology offers the advantage of permitting independent settings of the Gm stage and the switching quads to optimize the performance of each. In addition, a current steering gain tuning approach is applied to the transconductance stage to adjust the input signal level. The gain control voltage *Vctrl* that is

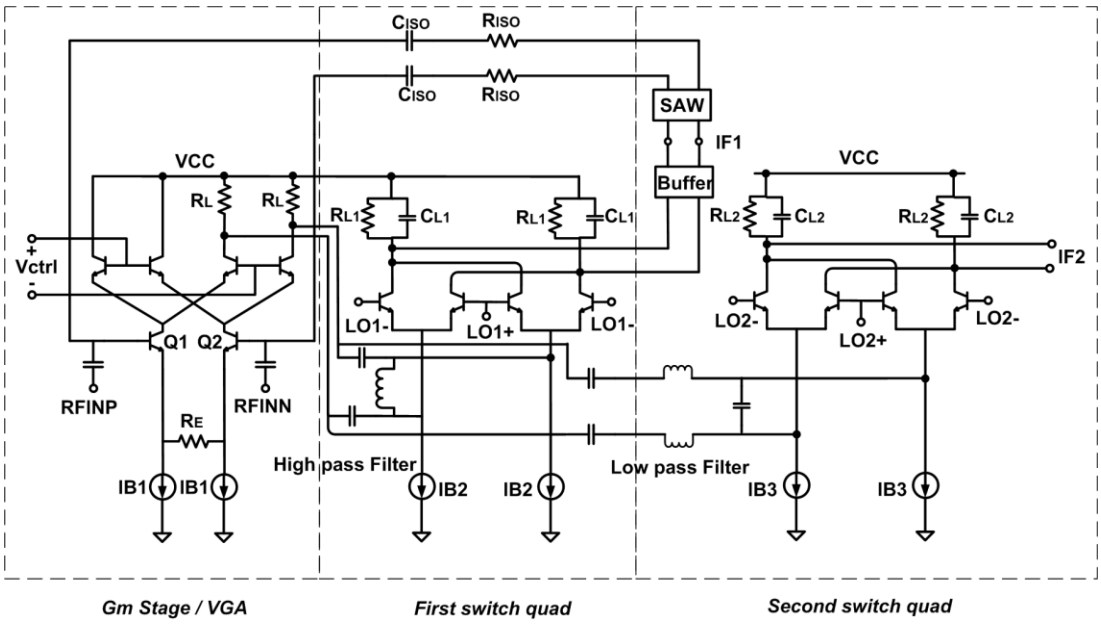


Fig. 4.6 Simplified schematic of the mixers with gain-reuse topology.

applied to the base of the upper multiplier in the Gm/VGA cell, is used to adjust the gain. With the control of *Vctrl* , the conversion gain from the input of the transconductance stage to the

output of the first switching quad is related to the control voltage as follows (assuming ideal square wave switching is applied to the switching transistors):

$$A_{v,IF1} \cong \frac{2}{\pi} \cdot \frac{1}{1+\exp\left(\frac{Vctrl}{V_T}\right)} \cdot \frac{R_{L1}}{r_e + R_E} \tag{4.10}$$

where V_T is the thermal voltage of the bipolar transistor, and r_e represents the equivalent emitter resistance of Q1 and Q2. A degeneration resistor R_E is used to increase the linearity since the mixer requires relatively high linear performance. As mentioned above, the first IF signal at the output of the first switching quad is re-applied to the input through the SAW filter. Hence, both the RF signal and the first IF signal are separately adjusted in the unique Gm stage before they are coupled into switch quads for the frequency-translation. Consequently, the tunability of the proposed super-heterodyne mixers' gain can be improved as indicated by Eq. (4.11) (neglecting the loss in the feedback loop)

$$A_{v,total} \cong \frac{4}{\pi^2} \cdot \frac{1}{\left[1+\exp\left(\frac{Vctrl}{V_T}\right)\right]^2} \cdot \frac{R_{L1}R_{L2}}{\left(r_e + R_E\right)^2} \tag{4.11}$$

The tunability of the gain is enhanced by the term of $\left[1+\exp\left(Vctrl/V_T\right)\right]$ compared to traditional multi-stage mixers without increasing the current consumption. Furthermore, since both RF and IF signals are adjusted in the unique Gm stage simultaneously, the power consumption of the two VGAs is further reduced with the same gain setting. Based on system requirements, a 20dB tuning range is finally determined as the continual tuning range. Although the continual gain tuning range can be further increased until IF2 output reaches the noise floor, the noise figure of the receiver will dramatically decrease. Meanwhile, spurs will increase due to

reduced linearity of the Gm/VGA stage. This is because the linearity of cascode transistors will be affected if too much current is steered away. In addition to the super-heterodyne receiver, the gain-reuse topology also shows good gain enhancement and power saving performance in the direct conversion receiver [16].

For noise considerations, the amplifier transistor in the Gm stage is carefully chosen to operate at the current density required for minimum noise figure. The minimum noise performance of the mixer also relies upon fast switching of the transistors in the switching quads, since fast switching will minimize the time in which the switching transistors stay in the active region. Thus, fast switching will dramatically reduce the noise passing on to the output. Therefore, the switching transistors are sized to the proper value, where their current density is close to that corresponding to the peak f_T .

In the circuit implementation of the proposed current reuse topology shown in Fig. 4.6, the outputs of the Gm stage are ac-coupled to the inputs of the switching quads of the mixers through a filter network. Both high-pass and a low-pass networks are needed in front of the switching quads to separate the RF and IF signals and avoid generating unwanted signals through the mixers. Load resistors for the tunable transconductance stage provide high impedance such that most of the small signal current flows into the switch quad. The isolation resistors R_{ISO} are used to prevent the RF signals from being loaded by small impedance, and the isolation capacitors C_{ISO} are used to isolate the DC bias.

The differential LO signals are generated by external signal generators. The signals, which are adjusted by the current mode logic (CML) inverter-type LO buffers with low-power and good slew-rate performance, drive the switching quad in Fig. 4.7. Each LO buffer, as shown in Fig. 4.7, consists of a CML inverter and emitter follower. Through use of an external balun, the

single-ended LO signal is transferred to differential mode and the LO voltage swing applied to the switching transistor is about 0.6 Vp-p to achieve the desired noise figure and gain.

With the option of routing the IF signal off-chip, the first IF signal is fed back to the inputs of the Gm stage through an external SAW filter that removes unwanted signals, such as image signals, LO leakages and their harmonics, before being reapplied to the input stage. Furthermore, leakage of first IF signal will generate an up-converted RF signal at the output of the first switching quad. This interference signal, along with the leakage of the RF signal, would lead to instability if they were fed back to the input of the Gm stage [16]. The bandpass SAW filter in the feedback loop will help remove these interference signals and keep the system stable. Since the second mixer requires higher linearity than the first, load resistor RL2 and bias current of the second mixer are chosen properly to give sufficient headroom for linearity.

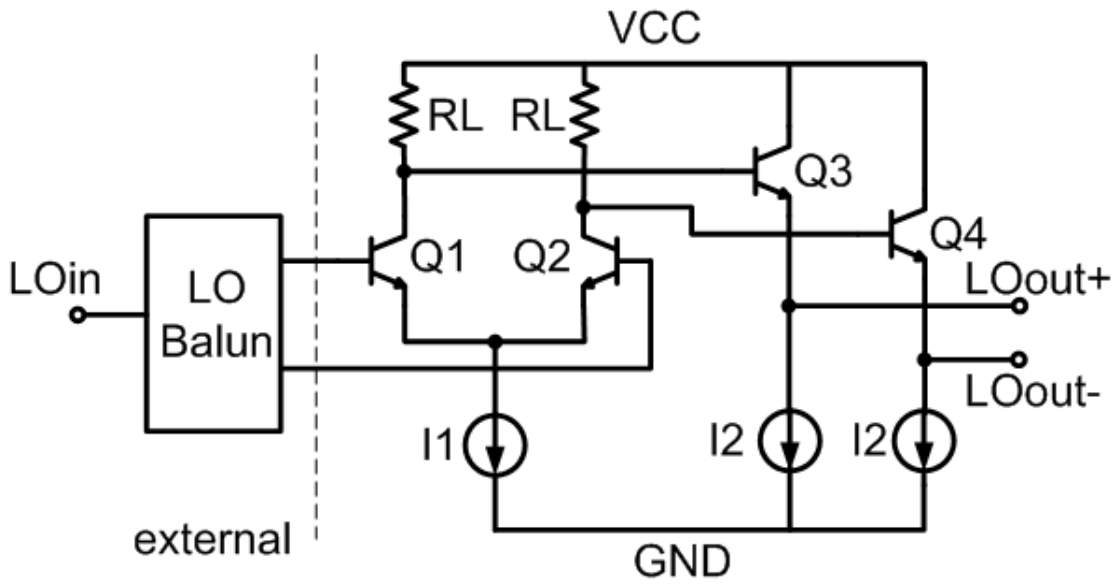


Fig. 4.7 Simplified schematic of the LO buffer.

4.3.3 Baseband VGA design

The baseband VGA, used in this design, has 8 gain settings. It has three cascade amplifiers

that each consists of two differential pairs with their collectors tied together. The core cells of each amplifier are similar, as shown in Figure 4.8. The only difference is the value of the load resistors and degeneration resistors in each stage. All tail current sources are controlled by 6 bit digital control signals. These digital control signals, which are translated from a 3 bit external control signal through a decoder, control which of the differential pairs in each stage will be on. Then current flows through one differential pair, but never both. The gain of each stage is approximately equal to the ratio of the load resistance to the degeneration resistance. In order to drive the output pad, two output buffers are included in the final stage. The VGA can be discretely tuned from -4dB to +32dB.

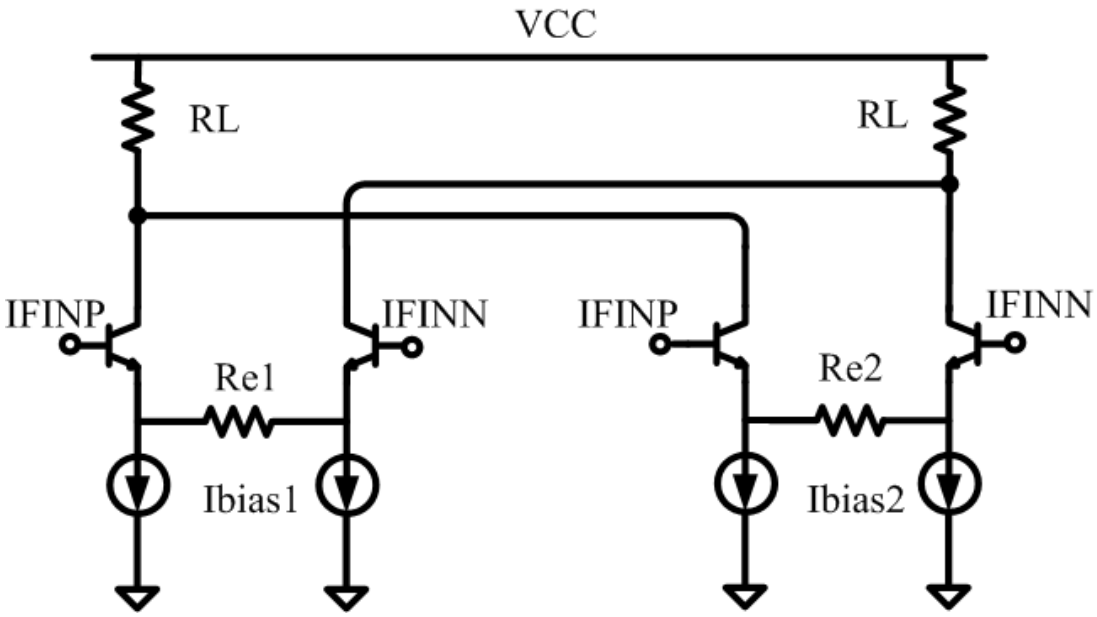


Figure 4.8 Simplified core cell of each stage of baseband VGA.

4.4 Experimental results

The wideband receiver MMIC is implemented in a 0.13μm SiGe BiCMOS process with a f_T of about 200GHz [17]. It occupies a total silicon area of 1.46 x 1.24 mm^2 and is packaged in a

48-pin QFN package. To obtain accurate RF measurements, a wafer probe was used for RF inputs while all other pads were wire-bonded to the package. Figure 4.9 shows the RF input return loss of the receiver. As shown, the input is well-matched to achieve smaller than -8.5 dB return loss over both the X- (8 – 12 GHz) and Ku-bands (12 – 18 GHz). In order to evaluate the performance of the receiver from 8 GHz to 12-GHz, the LO1 frequency was varied to follow the frequency change of the RF input to achieve a fixed IF2 signal at 150 MHz. The noise performance of the wideband receiver at maximum gain is shown in Figure 4.10. The double-sideband (DSB) noise figure was measured between 6.7 and 7.8dB from 8 – 18GHz with the minimum NF achieved at 11GHz. In order to examine the continuous tuning range of the receiver, the base-band VGA is set at high gain mode with a fixed gain of 32dB. The average maximum conversion gain of the wideband receiver is measured at 53 dB, as shown in Figure 4.11, and the tuning range resulting from tuning the Gm stage is also shown in this figure. The gain range between the minimum conversion gain (CG) and its maximum can be easily achieved by simply tuning the mixers of the Gm stage, and measured results show that a 20dB continuous tuning-range can be achieved. In the case of the gain-reuse design, the output in-band 1 dB gain compression point, measured at maximum gain, is nearly identical at different input frequencies. The measured average output compression point (OP1dB) is about -10 dBm, as shown in Figure 4.11. The measured performance and a comparison with previous work are summarized in Table I, and the die photo of the receiver MMIC is given in Figure 4.12. Compared to previous work [13], this design consumes much less power and occupies a smaller area. It also achieves much larger gain and higher dynamic range.

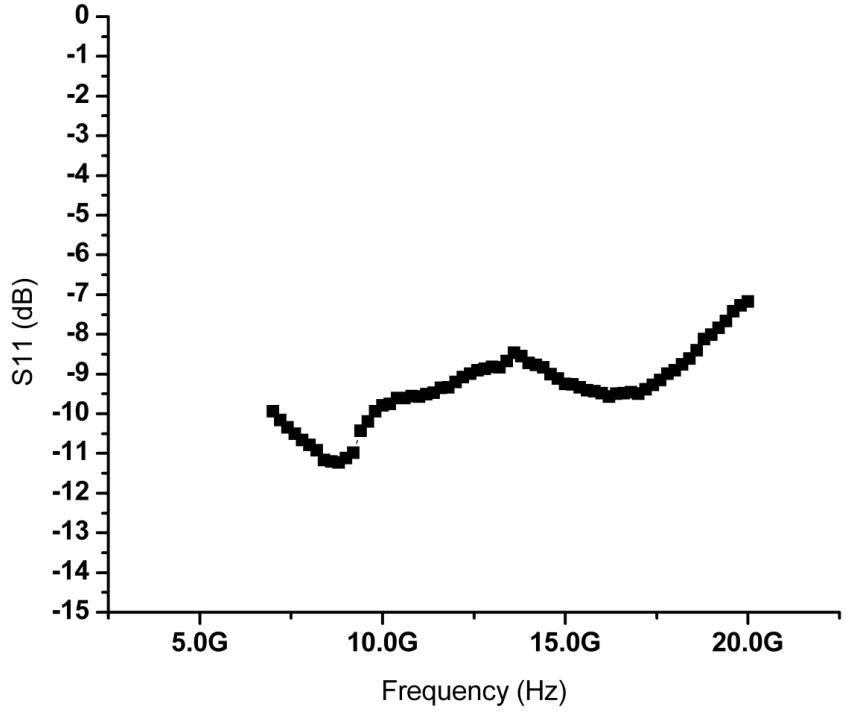


Figure 4.9 Measured S11 of wideband receiver versus frequency.

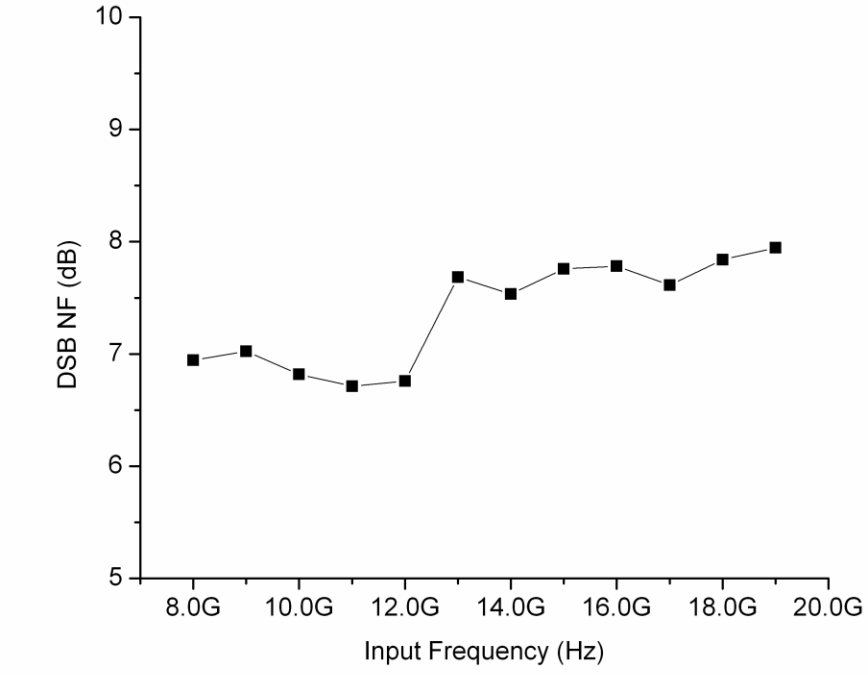


Figure 4.10 Measured NF of the wideband receiver.

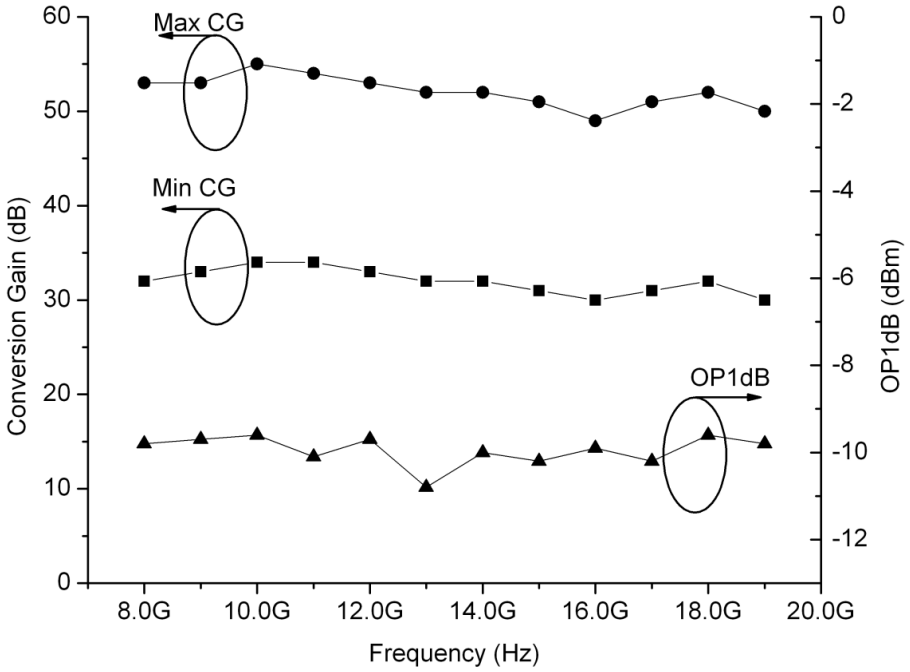


Figure 4.11 Measured conversion gain and the linearity performance of the wideband receiver when the baseband VGA is set at fixed gain.

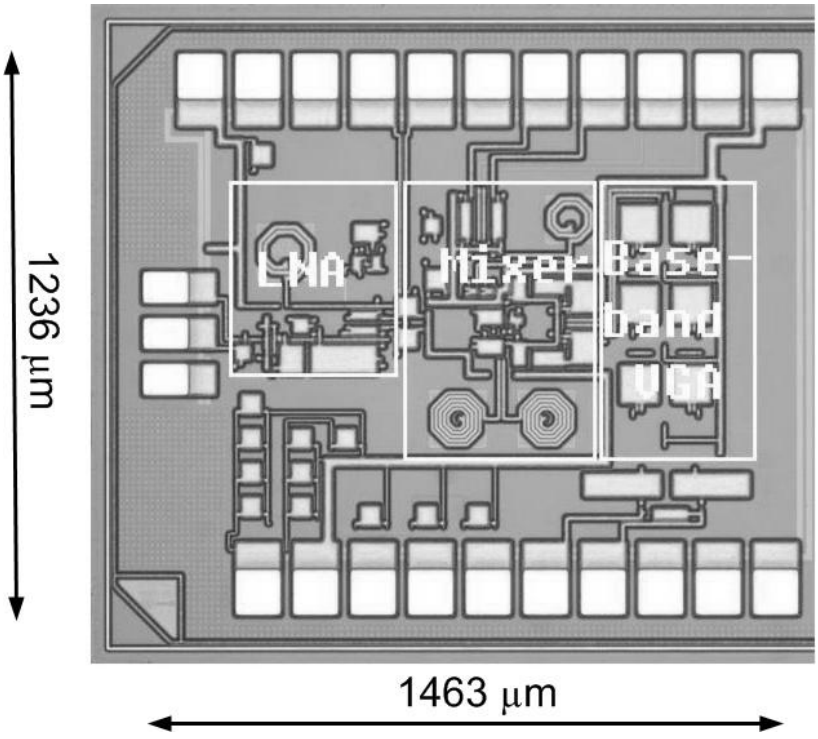


Figure 4.12 Die micrograph of the SiGe wideband receiver.

Table 4.1 PERFORMANCE COMPARISON WITH PUBLISHED WIDEBAND RECEIVER

	This Work	REF [3]
Technology	0.13 μ m SiGe BiCMOS	0.25 μ m GaAs pHEMT
Supply Voltage	2.2V	5V
Supported Band	X band (8 – 12 GHz) Ku band (12 – 18 GHz)	S band and C band (2 -8 GHz) X band (8 – 12 GHz) Ku band (12 – 18 GHz)
Voltage Gain	53dB (21dB from front end)	7.8dB
Tuning Range	56dB (20dB from front end)	0dB
Noise Figure	6.7 – 7.8dB @ Max gain	7dB
Input Return Loss	<-8.5dB @ 8 – 18GHz	<-10dB @ 2 – 18GHz
OP1dB @Max gain	-10dBm	--
Power Consumption	180mW **(**Maximum**)**	1.3W
Die Area	1.46x 1.24mm^2	5.7 x 4.2mm^2

4.5 Conclusion

A fully integrated, compact and power saving wideband receiver, which covers the entire X- and Ku- bands, without an external balun and matching network, is designed and fabricated in a commercial SiGe BiCMOS technology. Multi-feedback technology in conjunction with inductive compensation is applied to the input LNA design to achieve wideband operation. The design also utilizes a recursive gain reuse topology to save power with increased dynamic range. The receiver provides a flexible architecture with the option to use an external SAW for image rejection and anti-jamming. This work represents the demonstration of a fully integrated single-chip wideband receiver MMIC, fabricated on a commercially available SiGe process, that is capable of operating over the entire X- and Ku-bands. The MMIC represents a key component

for next generation wideband radar and wireless communication applications.

4.6 Appendix

Referring to Figure 4.5, performing KVL along the path which is from degeneration resistor R_{e1} to the input point v_{in}, the $v_{\pi 4}$ can be expressed as follow:

$$v_{\pi 4} = \frac{i_{b1} Z_{\pi 1} + i_1 R_{f2}}{1 + g_{m4} R_{e1}} \tag{4.12}$$

where i_1 is the feedback current and g_{m4} is the transconductance of transistor Q4.

Performing KVL along the path which starts from the degeneration resistor R_{e1} to the output point v_{out} instead of the input point, then $v_{\pi 3}$ is given as:

$$\begin{aligned} \left(1 + g_{m3} Z_{L1}\right) v_{\pi 3} \approx & -g_{m1} v_{\pi 1} \left(Z_{L1} + R_{f1}\right) \\ & - \left(i_{b1} Z_{\pi 1} + i_1 R_{f2}\right) \left(1 + \frac{g_{m4} Z_{L1}}{1 + g_{m4} R_{e1}}\right) \end{aligned} \tag{4.13}$$

where we have substituted $v_{\pi 4}$.

In the next step, performing KCL law on both sides the feedback resistor R_{f2}, we can get the relationship between i_1 and i_{b1}. From this relationship, Eq. (4.9) follows.

Chapter 5 TUNABLE FILTER DESIGN

5.1 Introduction

Despite the effort to build all circuits in the digital domain[37][38], analog filtering is still a hot topic in both academic and industry research due to its low power consumption, high speed and simplicity [39][40][41]. Tunable filtering is one of the challenges where tunable components, just like tunable resistors and capacitors, are very hard to be integrated. Recently, tunable filter IC with integrated tunable active devices attracts more and more attention owing to its lower cost, smaller size and higher level of integration [42][43][44][45][46][47][48].

Frequency characteristics of analog filters are usually based on RC or LC products, or on C/gm ratios, depending on the application and implementation. There are two widely used analog filtering methods: switched-capacitor filters(SC filters) and continuous-time technology. Typical applications for these filters are in video applications, RF front-end and baseband processing applications [49][50][51][52].

The switched-capacitor filters (SC filters) present some advantages, just like precisely defined bandpass characteristics, the ability of shifting cut-off frequency by just changing the clock frequency and easy programmability. However, the SC filter usually needs pre-filters and post-filters. To reduce the clock feedthrough, the clock frequency is much higher than the cut-off frequency of the filter. This limits the SC filter's application. The SC filters is usually used in the applications where programmability is important or high precision is required.

Continuous-time filters are often preferred for megahertz or gigahertz range applications, especially when only moderate precision is required. The two widely used technologies of

continuous-time analog filters are the MOSFET-C filters and the transconductance-C filters (G_m-C filters). However, the primary drawback in each is subtle: For MOSFET resistor, the transistor works at triode region, it is very hard to achieve large resistance in the commercial technologies. It is also difficult to compensate the nonlinear in the native characteristic of transistor working in this range[53][54][55]. For Gm-C filter, due to the reason that Gm is proportional to square root of bias current, it has a limited tuning range[56]. Typically, the tuning range is lower than tens times. This drawback makes it unsuitable for applications where wide tuning range is needed.

In this chapter, a SC filter for extreme environment application and a second order low pass filter with novel tunable CMOS resistor are presented.

5.2 Six order Butterworth SC low pass filter design

5.2.1 Introduction

With the development of aerospace exploration, considerations of extreme environments have been included more comprehensively into most IC designs related to aerospace engineering. The extreme environments, such as temperature, radiation, pressure, vibration, will easily preclude the use of conventional terrestrial IC designs for operation, actuation and movement under ambient conditions. Although the Moon is relatively close to the earth and the radiation level there is not too high, the extreme temperature conditions ($+120^{o}$C at lunar day and -180^{o}C at lunar night) on the lunar surface can still invalidate conventional electronic components and systems for control, sensing, and communication. This is problematic, since the development of modular, expandable, and reconfigurable human and robotics systems for lunar missions clearly requires electronic components and integrated packaged electronics modules which can operate

robustly without external thermal control. Designing robust electronic systems for over 300^{o}C (cyclic) temperature variations has never been attempted, until now.

Used on the NASA Lunar-Mars series of missions, the remote electronic unit sensors interface (RSI) ASIC is being developed. The RSI ASIC is the mixed signal ASIC that interfaces to the sensor and translates the analog sensor data to digital form for back end processing. The RSI ASIC includes 16 channels, partitioned as follows: 12 slow speed "Universal" channels, 2 high speed channels, and 2 charge amplifier channels. The extreme space environment of those projects gives tough challenges to the circuit design technologies. The chosen SiGe BiCMOS technology for this design inherently provides both novel bipolar devices (SiGe HBTs) and Si CMOS. Unlike conventional Si transistors, SiGe HBTs are very well suited for operation in the lunar environment [15]. The addition of Ge allows tailoring of the device bandgap which can be used to optimize device behavior as a function of temperature. SiGe BiCMOS offers unparalleled low temperature performance, wide temperature capability, and optimal mixed-signal design flexibility at the monolithic level by offering power efficient, high speed SiGe HBTs and high density Si CMOS [15][57].

The sixth order Butterworth low pass switched capacitor filter proposed in this section is a key part of the RSI ASIC. It is located before the analog to digital converter to help the system get accurate information from the sensor. The switched-capacitor (SC) technique is a widespread analog approach for the implementation of high-accuracy filtering functions in commercial integrated circuits (ICs). A very popular method for designing high-order or/and high-selectivity (high-Q) SC filters consists of transforming the desired transfer function into the cascade of first- and second-order structures. This approach reduces the frequency response sensitivity of the

filter to the quantization of its coefficients and provides good phase response robustness. However, each low-order section is specifically designed for realizing the necessary transfer function. Moreover, both extreme temperature and radiation environments were considered in filter design. Some topologies were utilized in our design to make the Butterworth filter work well under extreme environments. For example, the bandgap and opamp in our filter utilized temperature compensating architecture to achieve ultra-wide temperature (UWT) operation range. And also, an UWT band gap reference with a constant current output is used. The post simulation result shows that the temperature coefficient is less than 40ppm from -180^{o} C to 120^{o} C with full swing output.

The measured results show that the filter approximates a 6th order Butterworth filter response in range of -180^{o} C to 120^{o} C. The clock-to-cutoff frequency ratio is 100:1. The clock feedthrough is less than 10uV_{RMS} with single 3.3V supply. It consumes only 640uA current at clock frequency of 200 kHz and occupies only 0.4x1.4 mm^2.

5.2.2 Building blocks

5.2.2.1 SC integrator

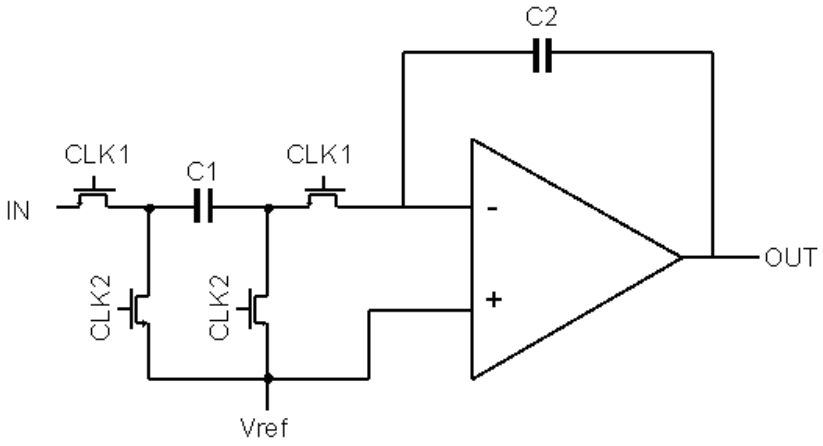
Figure 5.1 shows the two SC integrators used in our design. Referring to the schematics, assuming input signal is zero (virtual ground), the output voltage will be the virtual ground (Vref). Then these integrator can be directly cascaded. When switches are in CLK1 phase, charge on C_1 equals to$Q = C_1V_{in}$. Since the opamp input is open, the current to charge C_1 will flow to the right through C_2 where it changes the charge on C_2. When the switches are in CLK2 phase, C_2 discharges completely and C_1 retains its charge until next CLK1 phase. Then the transfer function of Figure 5.1(a) can be derived, which is an inverting integrator:

$$\frac{V_{out}}{V_{in}} = -\frac{f_c C_1}{j\omega C_2} \tag{5.1}$$

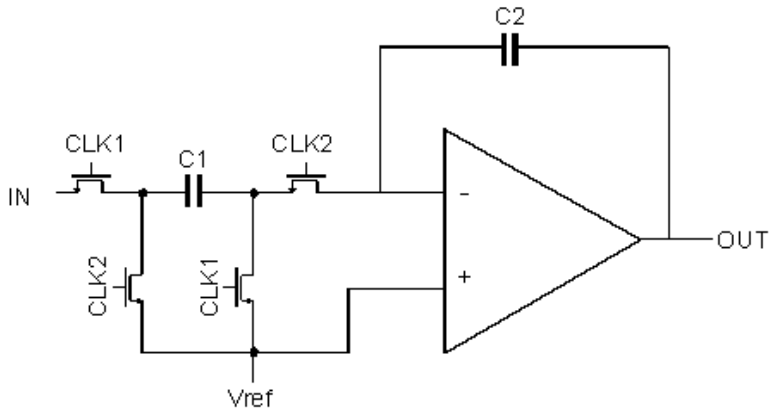
where f_c is the clock frequency,

Transfer function of Figure 5.1(b) shows a noninverting integrator :

$$\frac{V_{out}}{V_{in}} = \frac{f_c C_1}{j\omega C_2} \tag{5.2}$$



(a)



(b)

Figure 5.1 SC integrators: (a) inverting SC integrator; (b)noninverting SC integrator.

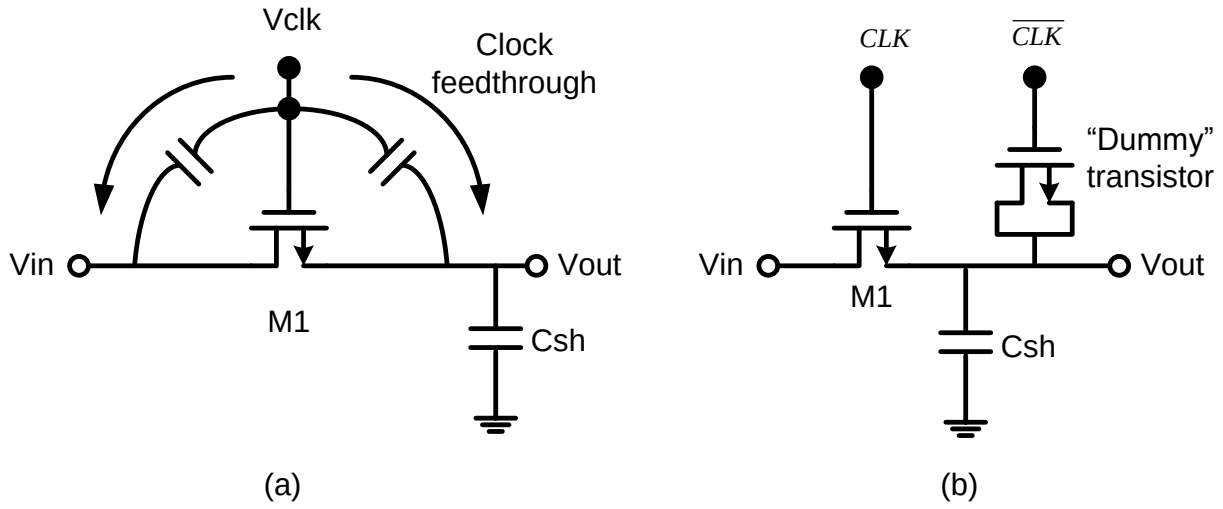


Figure 5.2 (a) Clock feedtrough in a sampling circuit. (b)Addition of dummy device to reduce clock feedthrough.

In our design, NMOS transistors were chosen to realize the filter switches. A MOS switch will couple the clock transitions to the sampling capacitor through the parasitic capacitors, as shown in Figure 5.2 (a). A "Dummy" switch, driven by opposite clock of M1, can be used to remove the clock feedthrough as shown in Figure 5.2 (b), After M1 turns off and the "dummy" transistor turns on, the channel charge deposited by the former on Csh is absorbed by the "dummy" transistor [58].

5.2.2.2 Operational amplifier (Opamp)

For extreme application, it is quite important that the amplifiers are stable and keep same performance in a very wide temperature range. This is particularly true in the amplifier of SC filters, since the amplifier is repeated a large number of times in the chip. Figure 5.3 shows the schematic of the opamp used in our design. It is made up of two stages: an n-channel input pair

followed by a common source amplifier with “nulling resistor” compensation, which makes the filter stable over wide temperature range.

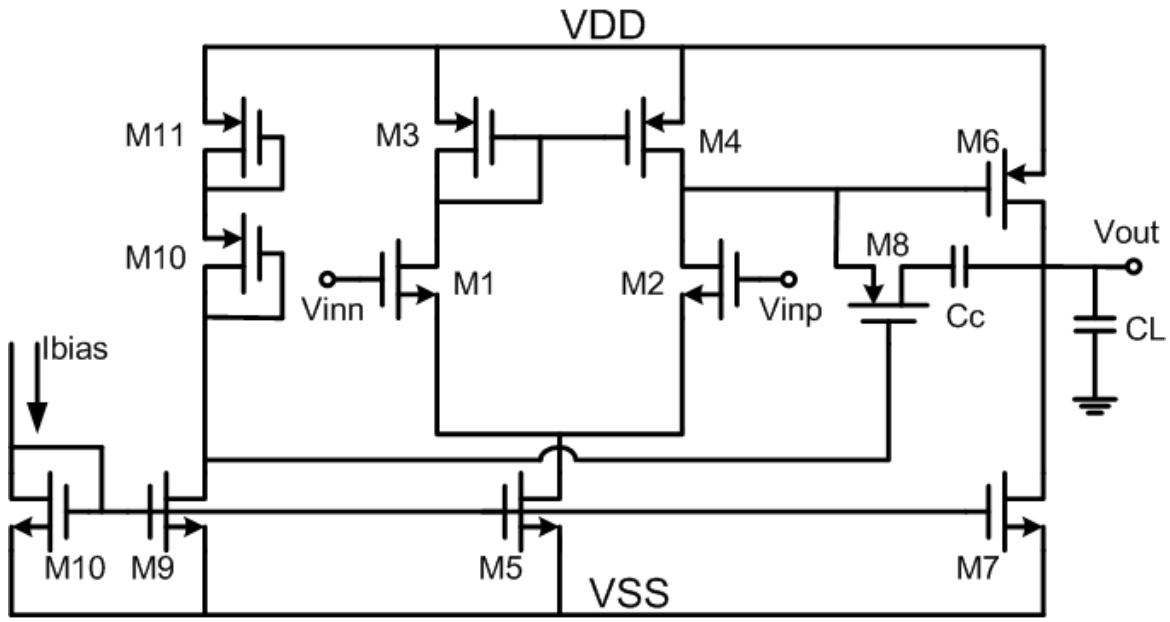


Figure 5.3 Simplified schematic of the operational amplifier

A common problem in MOS amplifiers is the presence of a low-frequency right half-plane zero. There are two traditional methods to eliminate the effect of this zero. One is to drive the compensation capacitor with a voltage follower [59], while another is to insert a resistor in series with the compensation capacitor [60]. Since there is no temperature consideration in both of the methods above, they are not suitable for the systems operating at extreme low temperature. The amplifier in our design utilized the UWT compensation method, which uses transistor M8 as a resistor, as shown in Figure 5.3. [61] The total gain is shown:

$$A_v = \frac{2g_{m2}g_{m6}}{I_5(\lambda_2+\lambda_4)I_6(\lambda_6+\lambda_7)} \tag{5.3}$$

With the addition of the transistor in the compensation, the resulting poles and zeros are: [61]

$$P_1 = -\frac{g_{m2}}{A_v C_c} = -\frac{g_{m1}}{A_v C_c} \tag{5.4}$$

$$P_2 = -\frac{g_{m6}}{C_L} \tag{5.5}$$

$$P_3 = -\frac{1}{R_z C_I} \tag{5.6}$$

$$Z_1 = \frac{-1}{R_z C_c - C_c / g_{m6}} \tag{5.7}$$

where C_I represents the total capacitance between gate and source while C_L represents the load capacitance. The resistor R_z is realized by the transistor M8, which is operating in the active region because the dc current through it is zero. By choosing the proper transistor M8's size and bias conditions, the zero can be easily placed on top of the highest nondominant pole (P2). Then the right half-plane zero is moved to the left half-plane and compensation is achieved. Using a simple MOS model, it is easy to get the size of the compensation transistor M8:

$$\left(\frac{W}{L}\right)_8 = \left(\frac{C_c}{C_c + C_L}\right)\sqrt{\left(\frac{W}{L}\right)_{10} \times \left(\frac{W}{L}\right)_6 \times \frac{I_6}{I_{10}}} \tag{5.8}$$

As shown in Eq. (5.8), the compensation is independent of temperature. It is only a function of relative device sizes, which can be well-matched and easily specified [61]. The use of this technique allows the amplifier to be stable and keep the same performance for cryogenic applications from -180^{o} C to 120^{o} C.

5.2.2.3 Ultra wide temperature (UWT) bandgap reference

Key to the success of developing a system at an extreme temperature range is to realize a robust and precise current reference. For a SC filter, the opamp's performance is sensitive to the accuracy and stability of the on-chip current reference. Therefore, it's rather critical to build a stable and temperature-independent bandgap reference capable of operating over the UWT range from -180 ℃ to +120 ℃. The bandgap reference circuit for UWT application is shown in Figure 5.4. Reference [62] shows the advantage of using SiGe technology in extreme environments. So our design utilizes the SiGe transistors to generate the temperature independent current sources. As shown in Figure 5.4, the bandgap consists of three stages: (1) PTAT stage: transistors M1-M6 and Q1-Q2, along with the resistor R1, generate the proportional to the absolute temperature (PTAT) bias current. (2) Compensating stage: transistors M7-M11 and Q3, along with the resistor R3, generate compensating current with a negative temperature coefficient (TC). (3) Summing stage: transistors M12-M17 combine the current from the PTAT stage and the compensating stage to generate a stable current in a wideband temperature range.

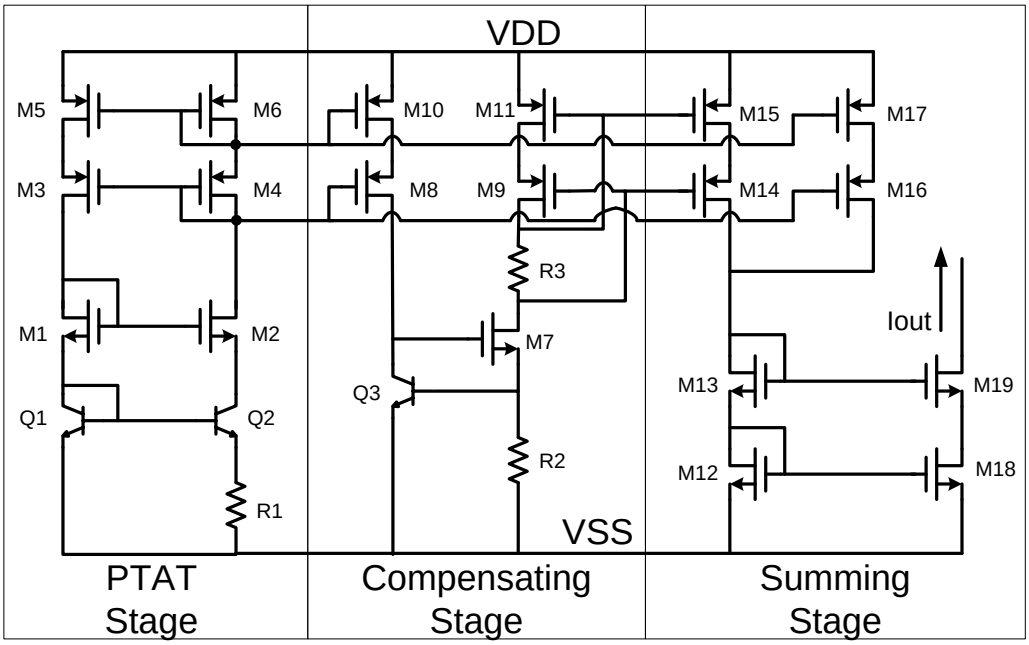


Figure 5.4 Schematic of UWT bandgap reference

In the PTAT stage, the voltage adding on resistor R1 is the difference between the base-emitter voltages of transistors Q1 and Q2. It generates a PTAT current, which has a positive temperature coefficient. The current through R1 and its TC can be expressed as follows : [36] [62]

$$I_{R1} = \frac{V_{BE,Q1} - V_{BE,Q1}}{R1} = \frac{kT}{qR1} \ln\left(\frac{I_{S2}}{I_{S1}}\right) \tag{5.9}$$

$$TC_1 = \frac{1}{I_{OUT}} \frac{\partial I_{OUT}}{\partial T} = \frac{1}{T} - \frac{1}{R1} \frac{\partial R1}{\partial T} \tag{5.10}$$

where T is the absolute temperature, I_{S1} and I_{S2} are saturation currents of Q1 and Q2. A large value was chosen for R1 to make TC of PTAT current positive.

Meanwhile, the output current in the compensating stage is determined by R2 and the voltage $V_{BE,Q3}$. The TC of current created by the compensating stage is:

$$TC_2 = \frac{1}{V_{BE,Q3}} \frac{\partial V_{BE,Q3}}{\partial T} - \frac{1}{R2} \frac{\partial R2}{\partial T} \tag{5.11}$$

Since both terms in (11) are negative, the TC of the second stage's current is negative, which can be used to compensate the positive temperature coefficient of PTAT current. PTAT current and compensating current are summed in the last stage, then UWT current source is achieved. And careful layout techniques were employed to reduce mismatch effects. The simulation result shows that the temperature coefficient of the current source is less than 80 ppm/℃ from -180 ℃ to 120 ℃.

5.2.2.4 Clock generator

The clock phase is an important issue in the switched capacitor filter design. The traditional two clock phases are used as the nonoverlapped clock phases for the SC filter[63]. Consequently, the two phases are generated starting from a master clock signal. Considering the "dummy" switches used to cancel the clock feedthough, complementary clocks of the above nonoverlapped clock are needed. The schematic of clock generator and nonoverlapped phases are shown in Figure 5.5. As shown, CLK1 and CLK2 are the nonoverlapped clock signal and CLK1P and CLK2P are complementary clocks. In our design, the nonoverlap is created by the delay through the inverter delay chain. Although the inverter delay would decrease as temperature drops, sufficient inverter delay inserted in the circuit can make sure two phases are nonoverlapped even at extreme low temperature -180 ℃.

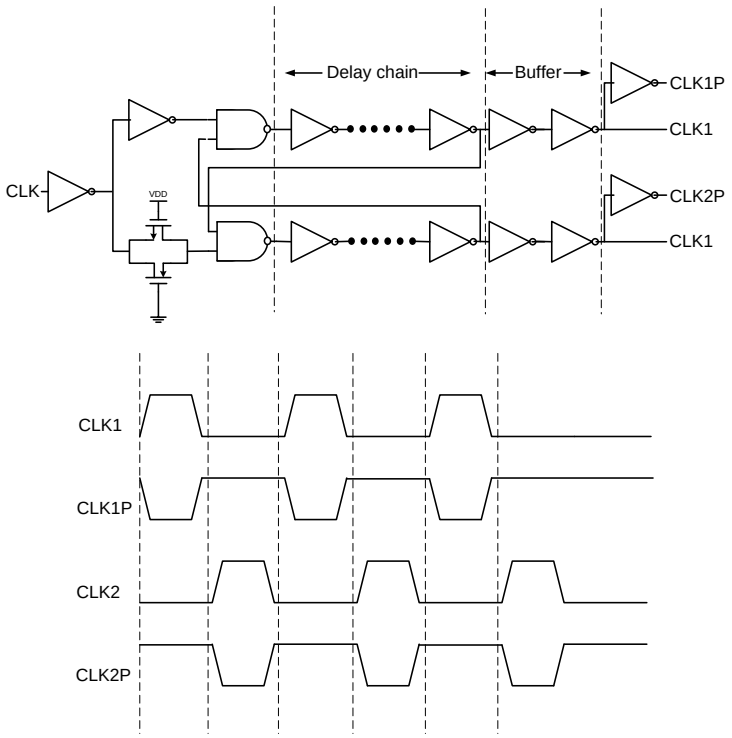


Figure 5.5 Schematic of clock generator and the nonoverlapped phases for switched capacitor filter.

5.2.3 SC filter design

The SC filter is used in both the charge amplifier channel and the high speed channel to filter out unwanted signals. The proposed filter design needs to meet some tough requirements given by RSI system, especially in extreme cryogenic condition. The requirements for the filter are: (1) stable sixth order Butterworth response with tunable cutoff frequency, which is proportional to the control clock; (2) low power consumption to reduce the system's power cost; (3) UWT operation range; (4) small clock feedthough; (5) radiation hardened by design.

By using the building blocks proposed above, a sixth-order Butterworth SC low pass filter was designed as shown in Figure 5.6. With proper architectures and suitable topologies utilized in the

design, the SC filter meets all requirements: (1) The Butterworth SC filter architecture was chosen, and then the first requirement is met by the nature of SC filter. The clock to cutoff frequency ratio was designed at 100:1. (2) To save power, the power killing block (opamp) was designed as simple as possible and a minimum number of opamps were used. Each opamp only draws 50uA current, and the total SC filter only consumes 640uA current at 200 kHz-clock frequency. (3) Each block in the SC filter was designed with temperature compensation, which makes the SC filter work over the UWT range. (4) "Dummy" transistors were added at the sampling capacitor to reduce the clock feedthrough, and also a post active filter with two fixed high frequency poles was placed after the SC filter core to remove the clock feedthrough. The block diagram of the proposed SC filter is shown in Figure 5.6. (5) Some special radiation hardening by design (RHBD) layout rules are applied in this design to improve the robustness in the radiation environment, which will be discussed in section 5.2.4.

Figure 5.7 shows the simplified core cell of the sixth order Butterworh SC filter. As shown, the SC filter is realized by cascading three biquads, each of them is a second order filter. While implementing the circuit, the switches are replaced by NMOS switches. Some of them perform the same function and can be shared to get a simpler circuitry. Considering the parasitic influence, a 500fF capacitor was chosen as the minimum switch capacitor.

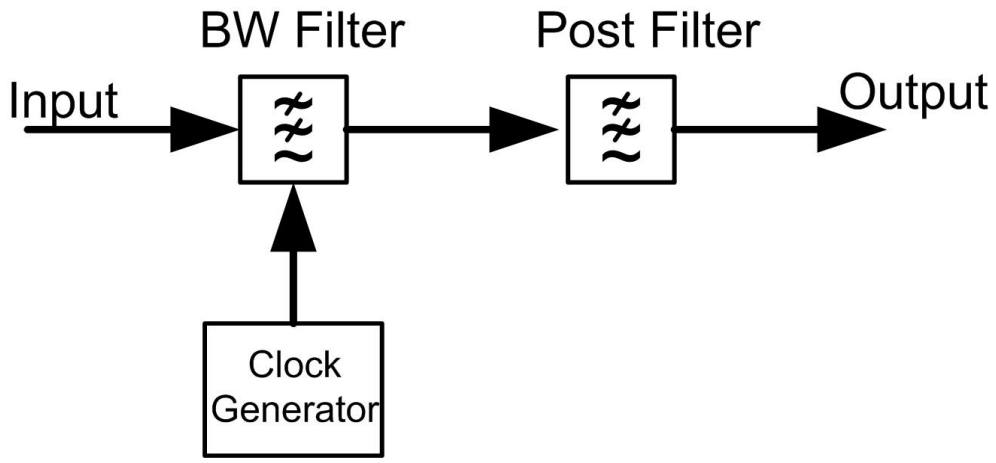


Figure 5.6 Block diagram of proposed SC filter

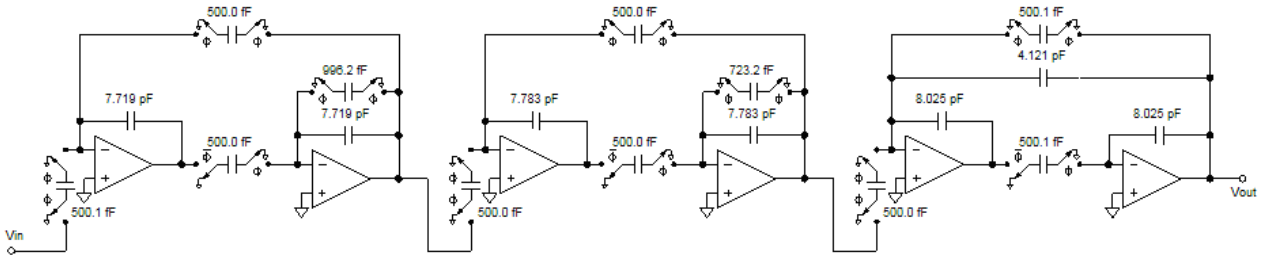


Figure 5.7 Proposed sixth order Butterworth switched capacitor low pass filter

5.2.4 Radiation hardening by design

Due to the lack of atmosphere on the moon, the semiconductor devices working on the lunar surface need to sustain high-energy radiation as well as extreme temperature environments. High-energy radiation will dramatically impair the performance of devices and even cause destruction of the devices [64]. To improve the robustness in the radiation environment: the minimal transistor width is chosen as 1μm other than the default 0.5μm. And to prevent the single event latch-up caused by the positive feedback formed in the parasitic transistors, some special RHBD layout rules are applied in this design to reduce the well/substrate parasitic

resistance and reduce the gain product of the parasitic NPN/PNP pairs. The RHBD rules include: active N+ (P+) guard rings are added around PMOS (NMOS); n-well and p-sub contacts are generously and frequently used; deep trench rings are added for isolation between PMOSs and NMOSs; keep n-well and n+ source/drain further apart if possible [65].

An example cell of RHBD layout in this design is shown in Figure 5.8. The die size of this design is enlarged by several times compared with the normal layout without RHBD consideration. This design still results in relatively small area compared with similar works by choosing the suitable circuit architecture and good layout floor plan.

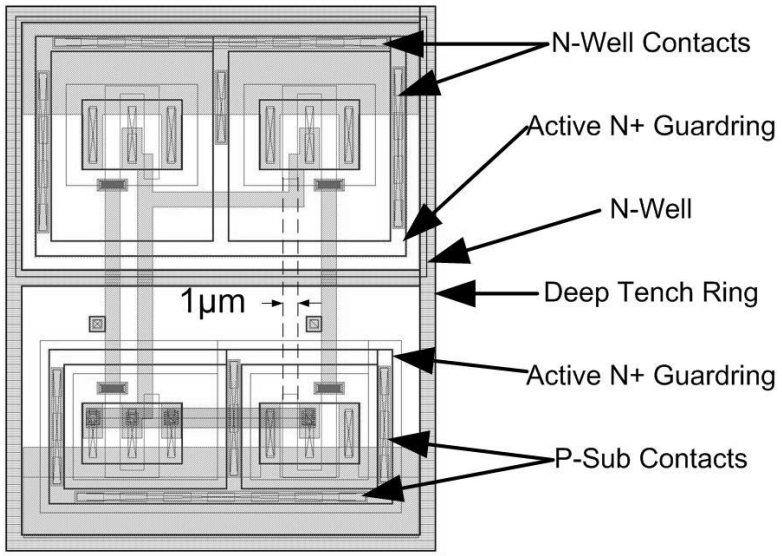


Figure 5.8 NAND gate by RHBD layout rules

5.2.5 Experimental results

The proposed cryogenic SC filter has been implemented in a 0.5μm SiGe BiCMOS technology. The micrograph photo of the filter chip is shown in Figure 5.9. The whole filter occupies an area of 0.08 mm^2 with a unit capacitor of 0.5 pF. In addition to RHBD layout rules,

some special layout techniques were also applied. To reduce the radiation effect, dummy transistors and duplicate cells are required to provide radiation protection for crucial circuit blocks. With the large W/L transistors and the protection cells, the area for crucial circuit blocks is enlarged so that the capability of resisting the radiation effects is improved. For increased transconductance and freeze-out effect at very low temperatures, the interconnection metals with larger width were used to provide margin for larger current conduction such that a sudden current increase will not damage the interconnection wires and invalidate the filter operation.

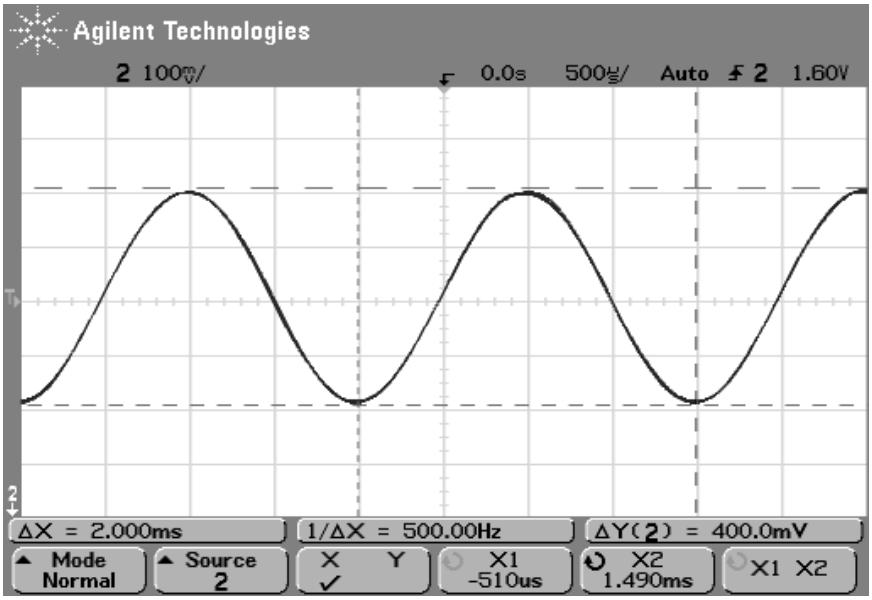
Figure 5.9 Die photo of the SC low pass filter

To test the cryogenic filter, an chamber with electrical heating and liquid Nitrogen cooling is used. The temperature inside the chamber can be controlled from -180℃ to 120℃. The inputs and outputs of the filter placed in the chamber are connected to the equipment outside of the chamber with SMA cables.

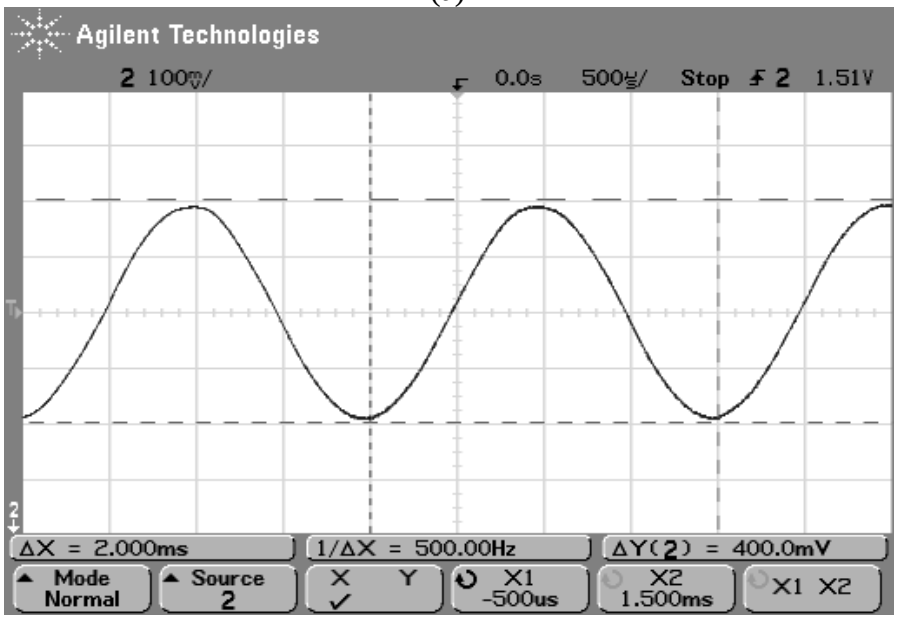
The measured transient responses for the output of the SC filter with a 500Hz 0.4-Vpp in-band input and 2 kHz clock frequency at room temperature, 120℃ and -180℃ are shown in Figure 5.10, respectively. From the above waveforms, it is evident that the proposed SC filter keeps the same performance over UWT range. It can be observed that the only difference as temperature changed is slight DC variation of output signal. That is due to the nature of the post active filter and small variation of bandgap reference. This DC variation can be easily calibrated by the DC

offset calibration circuit in each channel, together with DC offset of the whole channel as temperature changed.

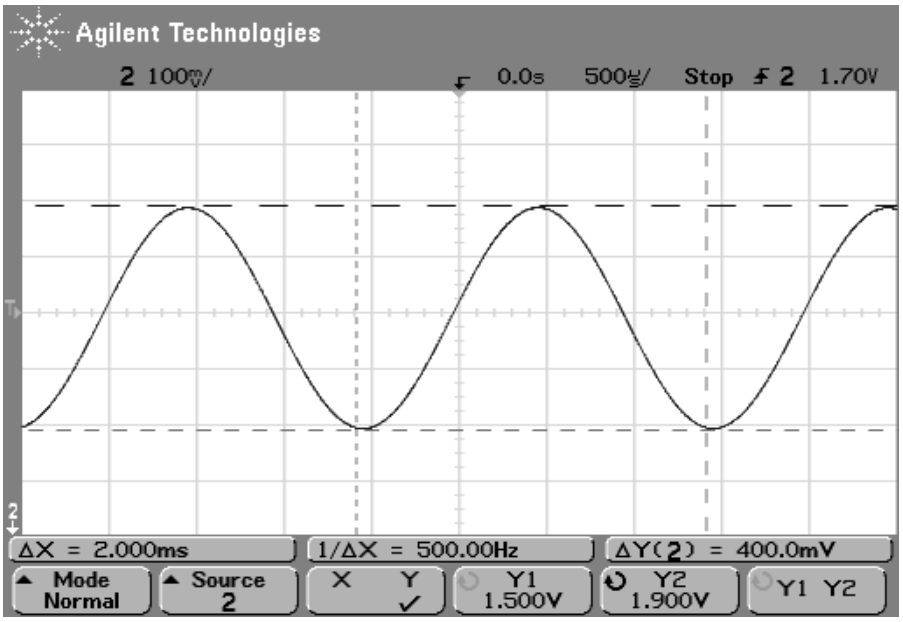
Measured results show that the filter achieves a stable sixth-order Butterworth low pass response, which is constant from -180 ℃ to 120 ℃, as shown in Figure 5.11. As mentioned above, the ratio of cut-off frequency to clock frequency is 1:100. The measured cut-off frequency in Figure 5.11 is 2 kHz, which is one hundredth of control clock frequency 200 kHz.



(a)



(b)



(c)

Figure 5.10 (a) Output transient response with a 500Hz 0.4-VPP input signal and 200 kHz clock frequency at room temperature. (b) Output transient response with a 500Hz 0.4-VPP input signal and 200 kHz clock frequency at 120 ℃. (c) Output transient response with a 500Hz 0.4-VPP input signal and 200 kHz clock frequency at -180 ℃.

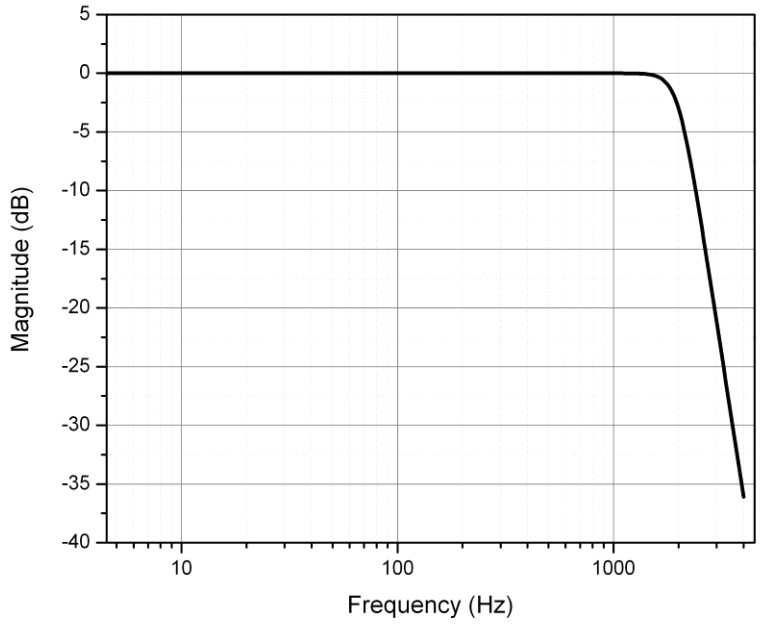


Figure 5.11 Frequency response of proposed SC filter, which keeps the same from -180 ℃ to 120 ℃.

A summary of the measured performance of the proposed SC filter is shown in Table 5.1. The maximum clock frequency is 12 MHz which means the maximum cut-off frequency of the SC filter is 120 kHz. Measured third-harmonic distortion (THD) is also given in Table 5.1. The input signal frequency is set at 500 Hz when cutoff frequency is at 2 kHz. The THD of proposed filter is -54dB when input amplitude is 0.4-V_{PP}. The clock feedthrough of proposed SC filter is only 10μV_{PP}, which is a simulation result. That's because the clock feedthrough is too small to be observed in real measurement.

Table 5.1 Summary of measured SC filter performance

Parameters	Performance
Technology	0.5μm SiGe BiCMOS
Temperature Range	-180 ℃ ~ 120 ℃
Cutoff Frequency	Fcutoff/Fclk=1/100
Maximum Clock	12 MHz
THD	-54 dB @ 400 mV_{PP}
Power Supply	3.3 V
Power Dissipation	640uA @ 200 kHz clock frequency
Clock Feedthrough	10 μV_{PP}*
Die Size	0.4×1.4 mm^2

* 10μV_{PP} is a simulated result. In real measurement, the clock feedthrough can not be observed, which confirmed simulation result.

5.2.6 Summary

In this section, a sixth order Butterworth SC low pass filter for aerospace extreme environment applications was implemented in 0.5μm SiGe BiCMOS technology. The measurement results

showed that the proposed SC filter is capable of operating over the ultra-wide temperature range from -180℃ to +120℃. Meanwhile, for the aerospace radiation environment, the SC filter was designed with good radiation-tolerance and robustness. In order to achieve temperature-independence, each block in the SC filter was designed for the UWT operation range. Design considerations for both extreme temperature and aerospace radiation environments have also been discussed. The chip die area is 0.56 mm^2 and the total current is only 640 μA at a clock frequency of 200 kHz with a 3.3 V power supply. Although no radiation performance was discussed in the dissertation, radiation testing with high energy proton dose to mimic the radiation environments is in progress.

5.3 Second order low pass filter with tunable resistor

5.3.1 Introduction

In this section, an improved tunable CMOS resistor with large resistance is presented [66]. In our design, a cascade differential pair of CMOS transistors is utilized in combination with a feedback circuit to generate an active tunable resistor. The resistance is inversely proportional to bias current instead of square root of the bias current. Thus, the tuning range of cutoff frequency is much wider than Gm cell in Gm-C filter. As an example, a second-order low pass RC filter using tunable CMOS resistor is proposed. The cutoff frequency can be widely tuned in the range of 5 kHz to 1.9MHz. The THD for a 500-kHz input signal is lower than -40dB up to 100mVpp input signal amplitude.

5.3.2 Operation of the tunable resistor

Active tunable resistors are used in a lot of applications such as voltage controlled amplifiers, automatic gain control systems and tunable filters. Many different techniques have been

proposed for implementing tunable resistors [54][55][67][68]. However, none of the above techniques can achieve large resistance and wide tuning range simultaneously.

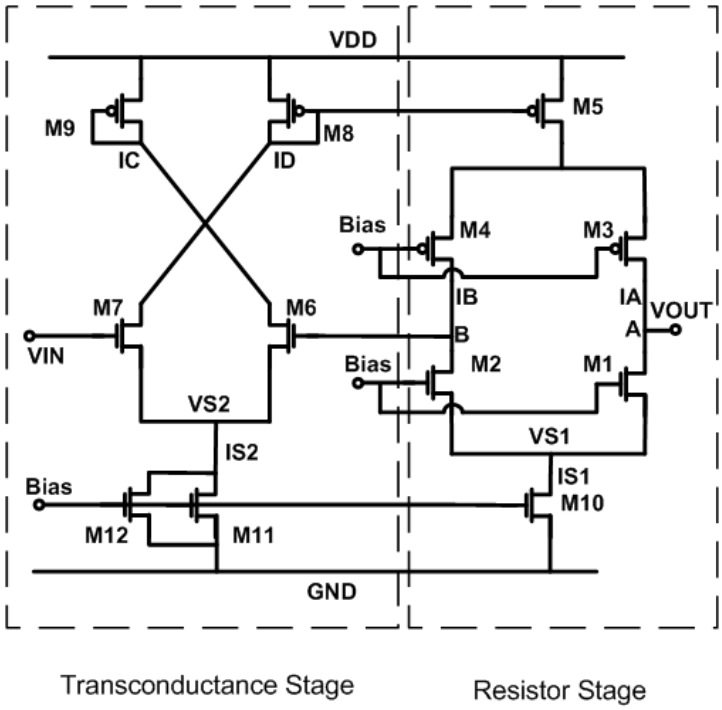


Figure 5.12 Simplified schematic of tunable resistor

Figure 5.12 shows the conceptual schematic of a presented tunable CMOS resistor. The tunable CMOS resistor can be seen as two parts: transconductance amplifier stage and resistor stage. Differential pair M6 and M7, together with current mirror transistors M9, M8, M5, and M10~12, constitute a transcondutance amplifier. This transconductance amplifier is loaded with internal cascade transistors. The gain can be described as follow:

$$A_V = \frac{r_{o4}\left(1+r_{o5}\times g_{m4}\right) \| \, r_{o2}\left(1+r_{o10}\times g_{m2}\right)}{\frac{1}{g_{m7}}+\frac{1}{g_{m6}}} \tag{5.12}$$

where $r_{o2,4,5,10}$ are the output resistances of transistors M2, M4, M5 and M10. $g_{m2,4,6,7}$ are the equivalent transconductances of transistor M2,M4, M6 and M7. As shown in Eq. (5.12), the

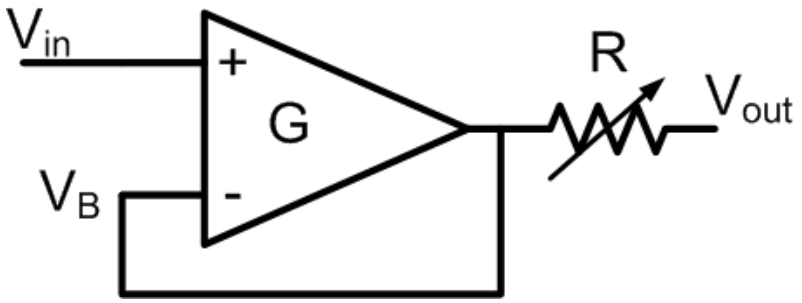


Figure 5.13 Equivalent symbol of the tunable resistor

voltage gain of this amplifier is very large. By connecting one input of the amplifier (gate of transistor M6) with its output (drain of transistor M4), it acts like a voltage follower. In this way, the voltage on B will follow input voltage. Then the desired tunable resistance from VIN to output A is equal to resistance between point A and B. The equivalent symbol of the tunable resistor is shown in Figure 5.13. As shown, the gain of the input amplifier is given as:

$$G = \frac{\left(g_{m6} \parallel g_{m7}\right)}{2} \tag{5.13}$$

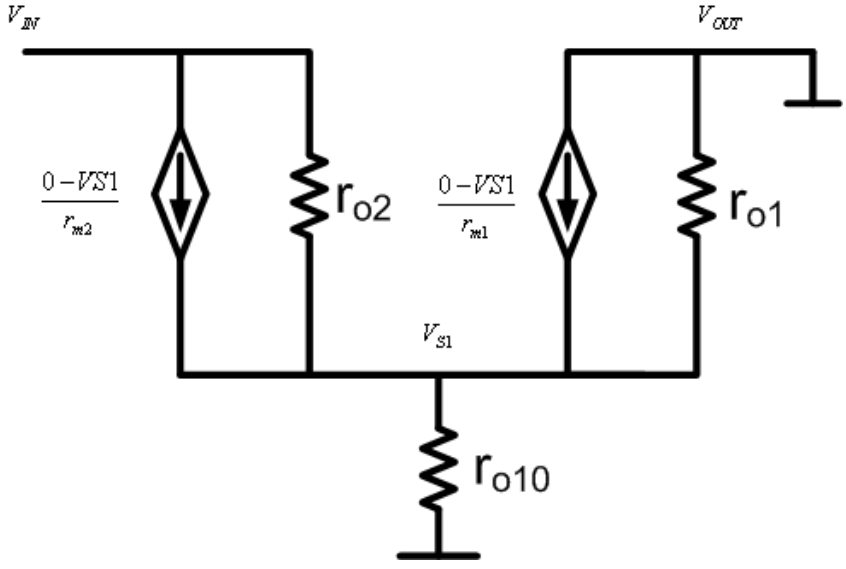


Figure 5.14 Small signal model of the tunable resistor

Figure 5.14 shows the small signal model of a half circuit of the tunable resistor, in which only nMOS transistors are considered. Assuming $V_{OUT} = 0$ and the output resistance ro are the same, we are able to derive the equivalent resistance between point A and Vin. Performing KCL at node VS1, we have:

$$V_{S1} = \frac{V_{IN}}{2\left(\frac{r_o}{r_m} + \frac{3}{2}\right)} \tag{5.14}$$

Where r_m represents reciprocal of $g_{m6,7}$ and r_o represent the output resistance of transistor $M_{1,2,10}$, which are unique. With the relationship between V_{S1} and V_{IN}, we can derive the equation for input current as follows:

$$\begin{aligned} I_{IN} &= \frac{-V_{S1}}{r_m} + \frac{V_{IN}}{r_o} \\ &= \frac{V_{IN}}{2r_o} \end{aligned} \tag{5.15}$$

Then the half circuit, which is shown in Figure 5.14, has the resistance of $2r_o$. And the overall tunable resistor has the equivalent resistance of $2r_{op}||r_{on}$. In order to provide large resistance, transistors M1, M2, M3 and M4 operate in the saturation region for our design. Then the resistance between point A and B is given as follow:

$$\begin{aligned} R &= \left(r_{o3} + r_{o4}\right) || \left(r_{o1} + r_{o2}\right) \\ &= \frac{1}{I_{eff}\left(\lambda_n + \lambda_p\right)} \end{aligned} \tag{5.16}$$

where $r_{o1,2,3,4}$ is the output resistance of transistors M1, M2, M3 and M4. λ_n and λ_p are channel length modulation parameters . And I_{eff} can be expressed as:

$$I_{eff} = \frac{I_A \times I_B}{I_A + I_B} \tag{5.17}$$

Due to symmetric design for the resistor stage, I_A and I_B are identical. Then the tunable CMOS resistor is achieved, with resistance equal to:

$$R = \frac{1}{I_{S1}\left(\frac{\lambda_n + \lambda_p}{2}\right)} \tag{5.18}$$

As derived in Eq. (5.18), the resistance is inversely proportional to bias current I_{S1}. It can be easily adjusted via changing the transistor's bias current I_{S1} and I_{S2}.

Above derivation is based on the assumption that voltage on node B is exactly as same as the input voltage. However, there is an offset between those two voltages. Next , more accurate results are derived. Still assuming the output voltage equals to zero, then referring to Figure 5.13, we can write the equation for node B, as follows:

$$\frac{V_B - 0}{R} - G \cdot \left(V_{IN} - V_B\right) = 0 \tag{5.19}$$

Voltage on node B is then given as:

$$V_B = \frac{V_{IN}}{1 + \frac{4 \cdot r_{m6,7}}{r_{op} \parallel r_{on}}} \tag{5.20}$$

With equation (5.20), the correction of tunable resistor's resistance is given as:

$$R_{corr} = R \cdot \left(1 + \frac{4 \cdot r_{m6,7}}{r_{op} \parallel r_{on}}\right) \tag{5.21}$$

Equation (5.21) is a correction result for the resistance of the proposed tunable resistor. However, for a transistor working at saturation range, the output resistance is usually much

larger than the reciprocal of the trancoductance. Equation (5.18) is still a simple and accurate expression for the resistance of the tunable resistor.

Sweeps of tunable resistance are shown in Figure 5.15. Here, V_T (x-axis) is the voltage adding on the tunable resistor, where VIN is the input point and the point A is the output point of the tunable resistor. And Iout (y-axis) is the current flow out from the tunable resistor. The bias current I_{S1} is shown on the top of Figure 5.15. As shown, the resistor behavior is obvious by the linear relation between Iout and V_T. The simulation result also validates that the tunable resistance is inversely proportional to bias current. Figure 5.16 shows the resistance variation as bias current changes. In Figure 5.16, both resistance and bias current I_{S1} are in logarithm scale. As shown, the resistance can be tuned from 90K ohm to 40M ohm by directly changing the bias current. Compared to traditional Gm cell, in which the tuning range is determined by square root of the bias current, and MOSFET working in triode region to act as a resistor, the CMOS resistor in our design has much wider resistance tuning range and larger resistance. In the implementation of tunable CMOS resistor, both current I_{S1} and I_{S2} are controlled by external voltage Vcurrent. Vcurrent can be tuned from 0.75V to 0.95V with step size of 0.05V, which results in the bias current I_{S1} tuned in range of 3uA to 50uA.

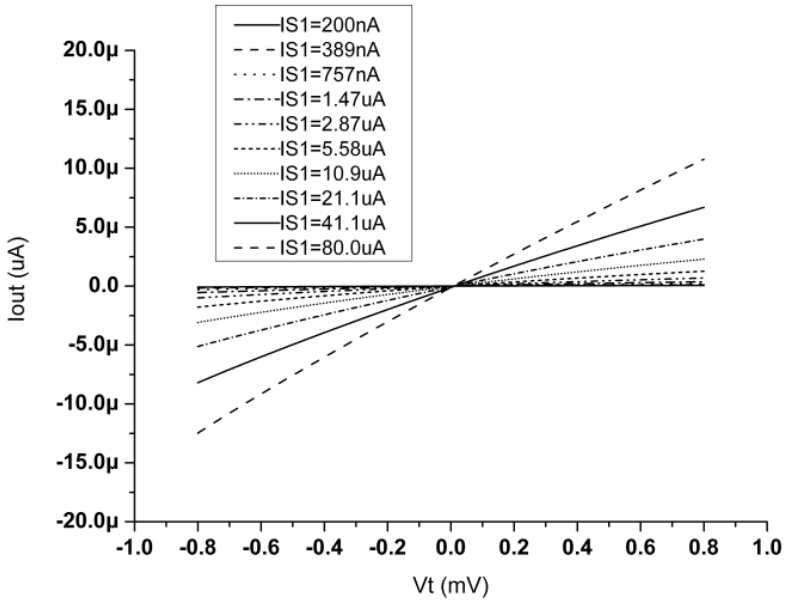


Figure 5.15 Simulation result of sweeps of resistance

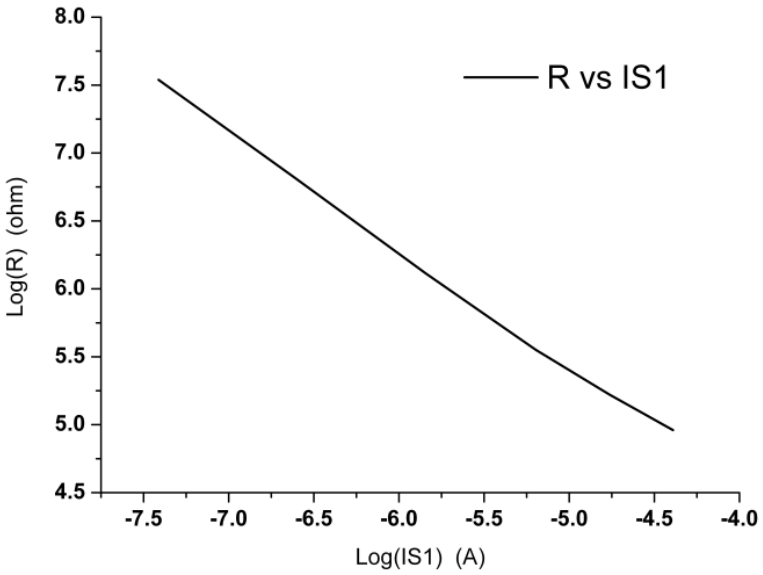


Figure 5.16 Resistance variation as current changes (resistance and current are both in logarithm scale)

For active components, power supply rejection ratio (PSRR) is an important parameter, which will directly affect the performance of the circuit. By using differential feedback architecture, the equivalent resistance of proposed tunable CMOS resistor exhibits a small change as power

supply shifts. Figure 5.17 shows simulation result of resistance's variation as power supply shifts, where Vcurrent is set to 0.9V. As shown in Figure 5.17, the resistance variation is less than ±5.6% as power supply voltage shifts from 3.1V to 3.5V.

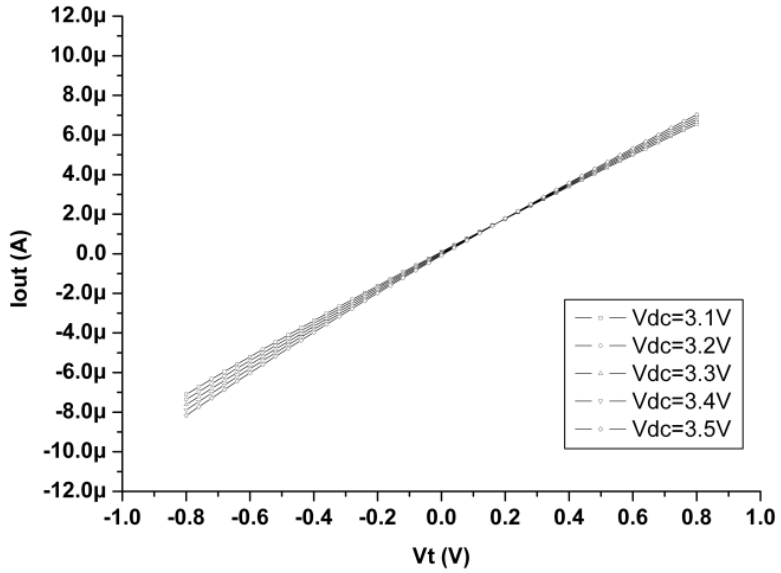
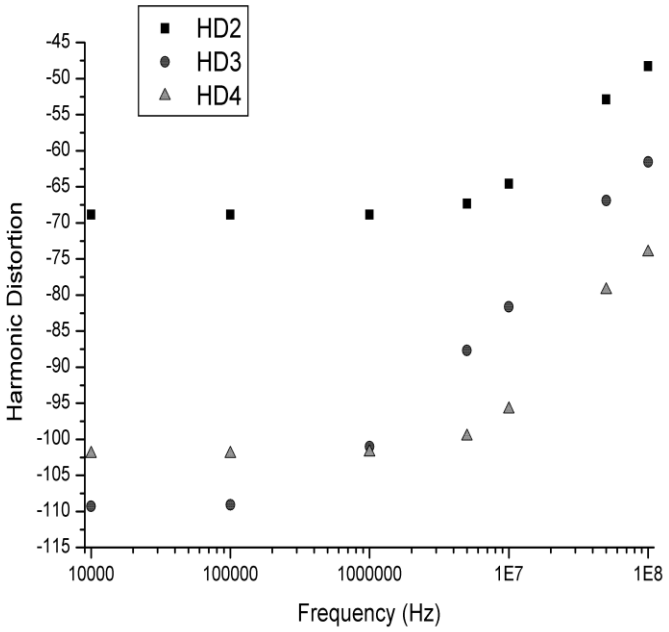
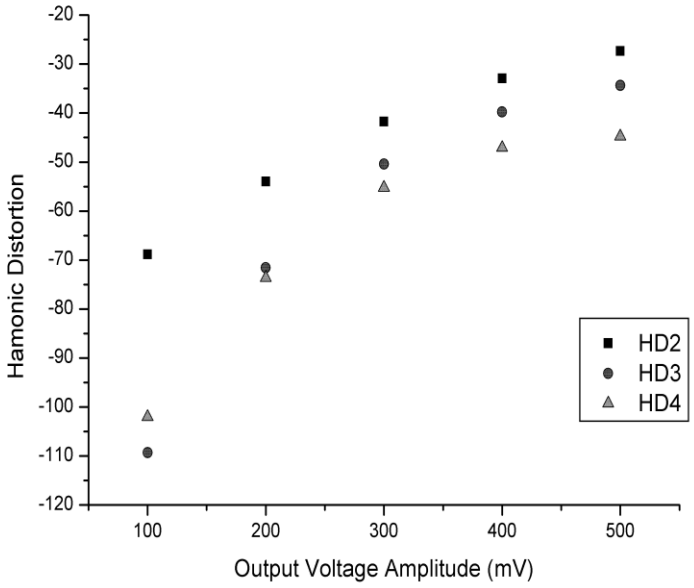


Figure 5.17 Voltage-current sweeps of the tunable resistor for different power supply voltage

Linearity performance of the tunable resistor at different conditions is also simulated. Figure 5.18 shows the simulated linearity performance of tunable resistor. Figure 5.18 (a) illustrates the harmonic distortion of the tunable resistor for different frequency when output signal amplitude is held at 100mV. As shown, the second harmonic distortion determines the THD, which is below -48dB when frequency is lower than 50MHz. Figure 5.18 (b) shows the harmonic distortion of the tunable resistor as signal amplitude is swept. The frequency of the input signal is kept at 500 kHz. Both (a) and (b) show that second order harmonic distortion is the dominated nonlinearity factor. Thus, reduction of distortion can be obtained by using the tunable resistor in balanced structures.



(a)

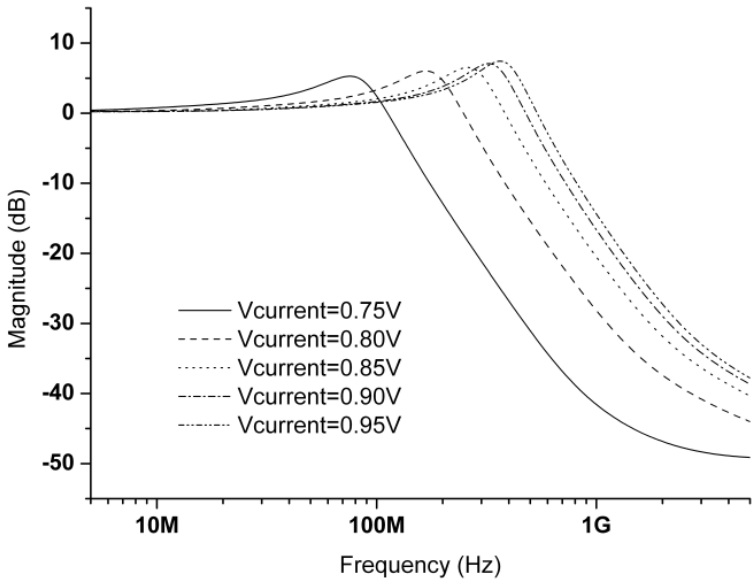


(b)

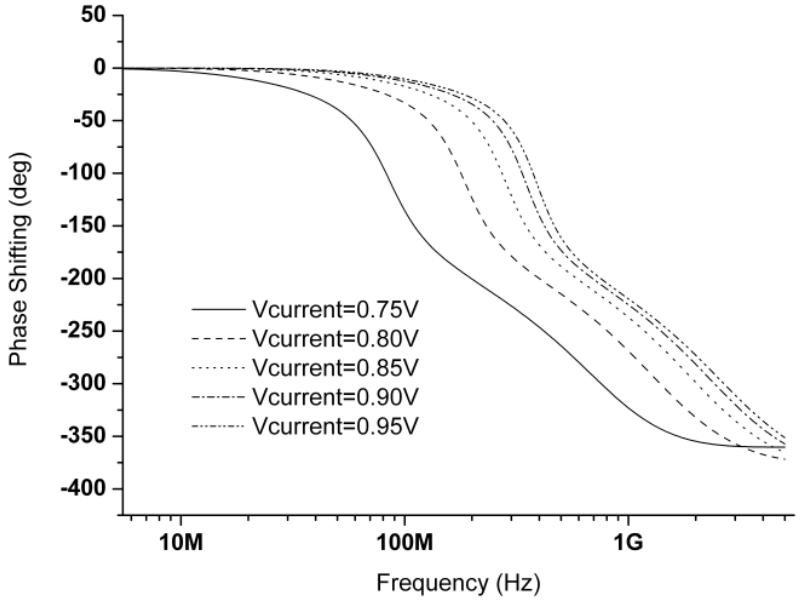
Figure 5.18 Experimental linearity results of the tunable resistor for different frequency and different output power. (a) Harmonic distortion for different input signal frequency. (b) Harmonic distortion for different output signal amplitude.

Figure 5.19 shows the simulation result for tunable resistor's amplitude response and phase shifting, which verifies our derivation. In our application, where Vcurrent is tuned from 0.75V to 0.95V, the cut-off frequency of the tunable resistor itself is from 130MHz to 670MHz. The cut-off frequency is far beyond operating frequency of the low pass filter, which is only several megahertz. Then the poles of the resistor itself can be neglected in the filter analysis.

The noise performance of the tunable CMOS resistor is also evaluated. Simulated performance of the equivalent output noise is shown in Figure 5.20. The noise spectrum is scanned from 1KHz to 100KHz at different current control voltages. The maximum output noise is $23nV/\sqrt{Hz}$ at 1KHz when Vcurrent is set at 0.95V. The output noise decreases as bias current I_{S1} and I_{S2} increase. As shown in Figure 5.20, output noise at low frequency is higher than that at high frequency due to 1/f noise from MOSFET transistors. The output noise of the proposed tunable CMOS resistor is much smaller than other active tunable resistors [68].



(a)



(b)

Figure 5.19 Simulation result of tunable resistor's frequency response: (a) magnitude response of the tunable resistor. (b) phase response of the tunable resistor.

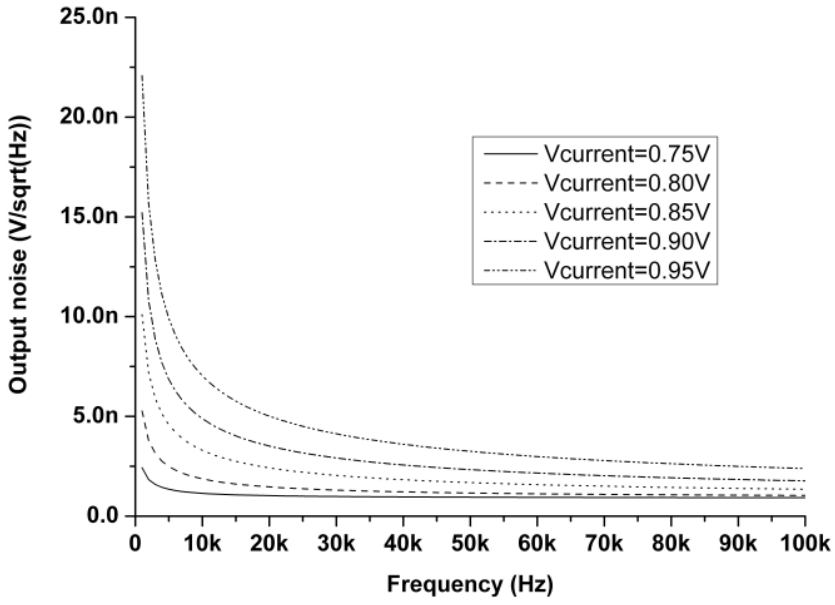


Figure 5.20 Equivalent output noise of the tunable resistor

5.3.3 Low pass filter

The quiescent value of the tunable resistor's output voltage is always very close to the DC level of its input voltage. On the other hand, compared to a real resistor, the proposed tunable resistor's input capacitance C_{gs} is only several femtofarads, which can be seen as infinity in the megahertz frequency range. Then two tunable resistors can be directly cascaded without considering the influence of input and output impedances between two blocks. A simple way to implement a second-order low-pass RC filter with proposed tunable resistor is shown in Figure 5.21. As shown, tunable resistors and capacitors are simply connected to compose a low-pass filter.

The transfer function of the two cascaded RC sections is the product of each transfer function (two tunable resistors are under same control voltage for bias current):

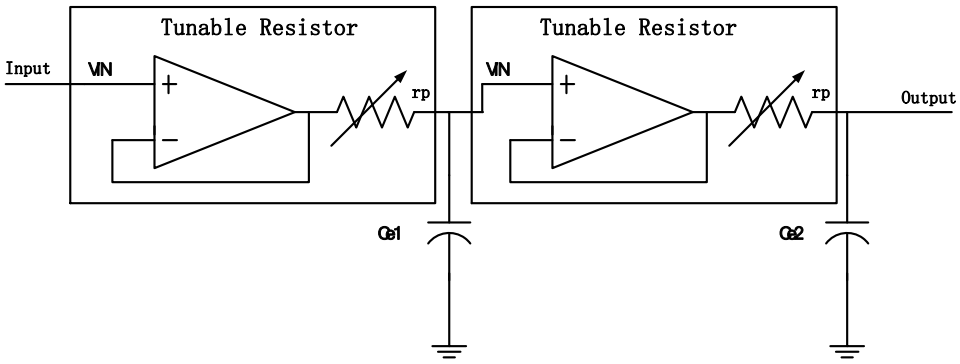


Figure 5.21 Simplify schematic of second-order low pass filter based on tunable resistor

$$\begin{aligned} T(s) &= T_1(S) \times T_2(s) = \frac{1}{sCR+1} \times \frac{1}{sCR+1} \\ &= \frac{1}{(sCR)^2 + 2sCR + 1} \\ &= \frac{1}{\left(sC \times \frac{1}{\alpha I_{S1}}\right)^2 + 2sC \times \frac{1}{\alpha I_{S1}} + 1} \end{aligned} \tag{5.22}$$

Since tunable resistor's pole frequency is far away from the filter's pole frequency, as shown in last section, its influence on low frequency pole can be neglected. The proposed second order low-pass RC filter has a single pole located at:

$$p = -\omega_c = -\frac{1}{RC} = -\frac{I_{S1}\left(\frac{\lambda_n + \lambda_p}{2}\right)}{C} \tag{5.23}$$

As shown in Eq. (5.23), the cut-off frequency can be tuned via directly changing bias current.

As an example, a second-order tunable low pass filter using the CMOS resistor as discussed above is implemented in 0.5-μm CMOS technology. The total filter block occupies $0.25 \times 0.13 mm^2$ as shown in Figure 5.22. Figure 5.22 (a) shows the layout of the second-order tunable low pass filter. As shown, the chip size is limited by the pads. Due to the density requirement, the whole chip was filled with a lot of small top layer metal cells. Then the chip detail is covered by the top layer metal in the die micro-photography, as shown in Figure 5.22 (b). The tunable resistor block is the same as shown in Figure 5.12. The two tunable resistors in the filter are identical; but differences will occur due to manufacturing tolerances. Therefore separate external tuning may be necessary.

Referring to Eq. (5.23), the frequency response of the filter is also related to the value of the on-chip capacitors besides bias current. But capacitances, such as Ce1 and Ce2, normally can only be changed at the design stage and cannot be tuned in operation. To reduce influence of parasitic parameters, metal isolator metal (MIM) is chosen to implement the capacitors Ce1 and Ce2. In advanced technologies, the capacitance can be further reduced to achieve high operating frequency.

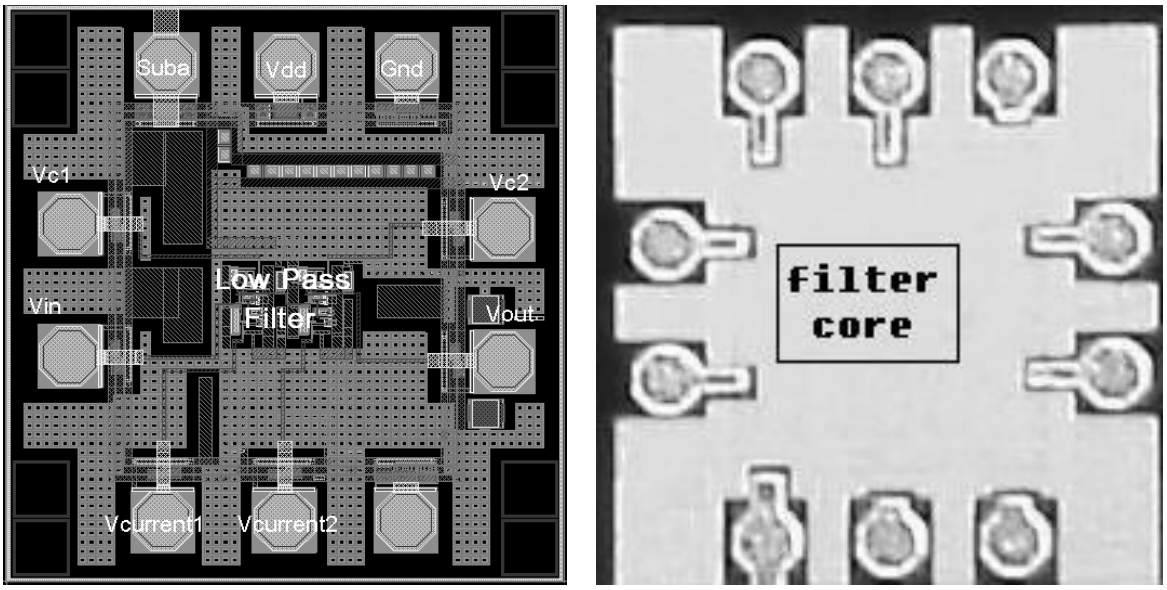
Careful consideration during layout is important to ensure the minimum parasitic influence

through the low pass filter. Banks of decoupling capacitors were located at the power supply and bias point to filter out noise coming from the external test equipment. Symmetrical layout is performed to the proposed resistor to ensure each branch in the differential pair has the same value and performance.

5.3.4 Experimental results

The filter was packaged in 2mm×2mm QFN package. Figure 5.23 shows the measured amplitude response of the filter when input signal level is 300mV_{p-p}. As shown, the cutoff frequency can be widely tuned from 5 kHz to 1.9 MHz as current control voltage changes from 0.75V to 0.95V. The cutoff frequency is a little bit lower than the simulation result due to the influence from parasitic capacitance of package and PCB board.

The linearity performance of the low pass filter is shown in Figure 5.24. The input signal frequency is set at 500 kHz when cutoff frequency is at 1.5MHz. The THD of the tunable filter is -40dB when input amplitude is 100mV_{p-p} and -34dB when input amplitude is 200mV_{p-p}. A summary of the measured performance of the proposed filter is shown in Table 5.2. The tuning range of the proposed filter, which is defined as the ratio of the maximum cut-off frequency to the minimum frequency, is much wider than previous work with smaller power consumption and area cost.



(a) (b)

Figure 5.22 Layout (left) and the die micro-photography (right) of the tunable low pass filter.

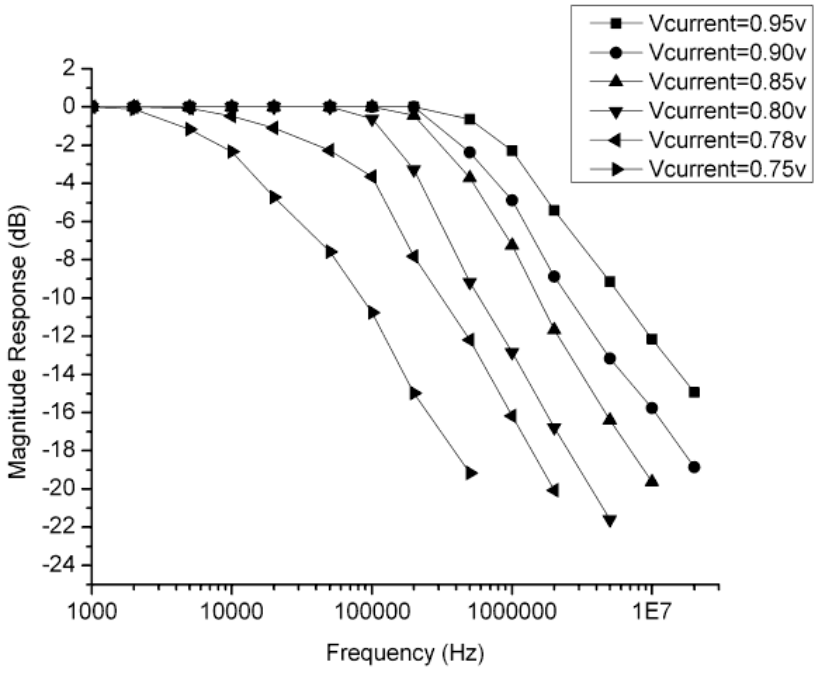
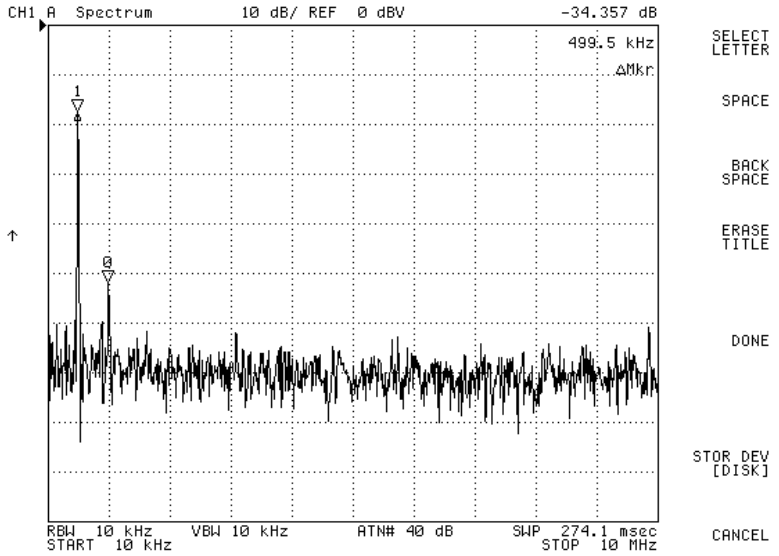
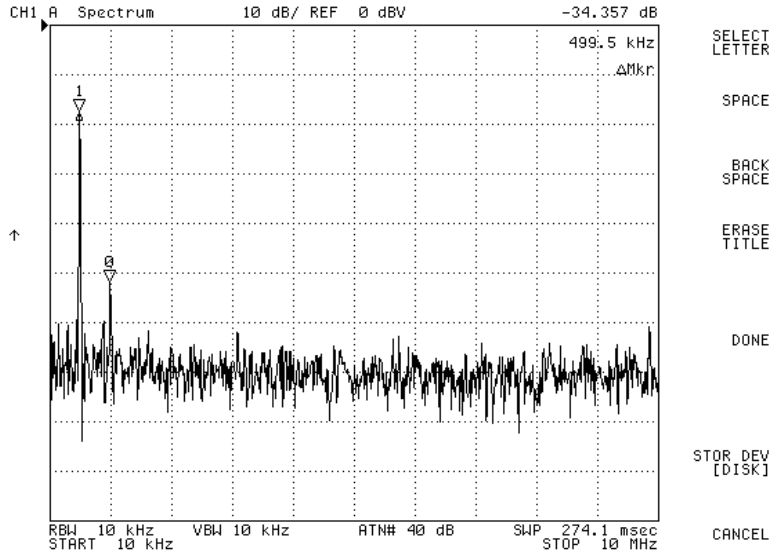


Figure 5.23 Measured amplitude response of tunable low pass filter.



(a)



(b)

Figure 5.24 Measured output spectrum of the second-order low pass filter at: (a) input signal level of 100mV Vp-p (b) input signal level of 200mV Vp-p

Table 5.2 Summary of measured performance of the proposed low pass filter

	Ref [43]	This work
Technology	0.18-μm CMOS	0.5-μm CMOS
Power Supply Voltage	1.8V	3.3V
Cutoff frequency range	0.5M - 12M Hz	5kHz - 1.9MHz
Frequency tuning range	24	380
Power Consumption (maximum/minimum)	4.7mW/1.1mW	5.7mW/2.8mW
THD (100mV V_{P-P} @ 0.5MHz)	--	-40dB
Core Size	0.125 mm^2	0.0325mm^2

5.3.5 Summary

In this section, a novel all-transistors CMOS tunable resistor has been designed and analyzed. Its main characteristics are: wide frequency tuning range, low power consumption, and small die size. The resistance can be tuned by directly changing a bias current. The frequency response of a tunable resistor is derived. The derivation and simulation results show the tunable resistor itself operates as a low-pass filter in the hundred megahertz range. Its tuning range is from 130MHz to 670MHz. The equivalent output noise of the proposed resistor is below $23nV/\sqrt{Hz}$; THD is -48dB at an output signal level of 100mV. The performance of the proposed tunable resistor has been demonstrated realizing a second-order low-pass RC filter in 0.5-μm CMOS technology. The measured result shows that the cutoff frequency can be tuned from 5 kHz to 1.9 MHz. The THD is -40dB at an input signal level of 100mV.

5.4 Conclusion

In this chapter, two tunable filters implementation are addressed. First, a six order SC filter for cryogenic application is introduced. The SC filter operates in the digital domain. This integrated filter has been proven very successful at low to medium frequencies range in cryogenic practice. And the analysis and design entail a new and different mathematical treatment. Secondly, a novel tunable CMOS resistor, where the transistors operate at saturation region, is presented. With the novel tunable CMOS resistor, large tuning range and large resistance are achieved. As an example, a low pass filter based on the CMOS resistor is develop, which show a excellent performance.

Chapter 6 Conclusion

6.1 Summary of original work

Due to emergence of next-generation wireless communications, system requirements and multimedia standards have placed increasing demands for high performance RFIC designs and analog circuits. The high performance challenges the designer to build novel RF transceivers with high performance.

In this dissertation the methods necessary for RFIC design and tunable filter design are explored, with distinctions drawn between them and conventional designs. In chapter 2, two novel LNAs are developed. The Q-enhanced LNA uses a negative gm cell to cancel the loss in the tank, which achieves 70dB IRR. With Q-enhanced technology, the cost and power are dramatically reduced. In the following section of chapter 2, the design of a wideband LNA is introduced. With the self-healing technology, the peak gain frequency and the input matching frequency can be adjusted to the operating frequency simultaneously. Meanwhile, the gain of the LNA is also adjustable for the self-healing purpose.

An LC based digitally controlled oscillator (DCO) is introduced in chapter 3. The capacitor switching bank in series is used to increase the resolution bits. With this configuration, the average frequency resolution is 0.1MHz/bit.

After introduced building block design, an wideband RF receiver design is discussed in chapter 4. As an example, an 8-18GHz wideband receiver with super-heterodyne topology is introduced. Multi-feedback technology, which provides more freedom in input matching, was

utilized in the LNA design for the input matching over the X- and Ku-band frequency range. In order to save power, both the RF and IF signals share the tunable transconductance stage. The IF output of the first mixer is fed back into the tunable input stage for IF amplification in a recursive manner, which significantly enhances the gain tuning without increasing the power.

In the final chapter, research on tunable filters is addressed. The discussion is divided into two parts, an SC filter and a low pass filter based on novel tunable resistor. The SC filter is for cryogenic application. Some particular technologies, like UWT opamp circuit, UWT bandgap circuit and radiation hardening by design, are addressed in the SC filter design. The measured results show that the filter approximates a sixth order Butterworth filter response in range of -180 ℃ to 120 ℃. Secondly, a new tunable CMOS resistor is proposed. The resistance is inversely proportional to bias current, to provide the resistor with a wider tuning range. And also transistors, composing the active resistor, work in the saturation region to achieve very large resistance within a small area. As a example, a low pass RC filter using the proposed tunable CMOS resistor realized in 0.5-μm CMOS technology is reported. The measured result shows that the cutoff frequency of the low pass filter can be widely tuned from 5 kHz to 1.9 MHz, whose tuning ratio is 380.

6.2 Possible future works

In this dissertation, several novel RFIC designs and analog circuits are implemented and hardware verified. Furthermore, there are still some works which needs to be carefully analyzed to further improve their performance in the future:

1) For the Q-enhanced LNA design, adjustment of operating frequency and image filtering frequency is possible by making load tank and filtering tank tunable.

2) For the wideband LNA with self-healing, only the self-tuning of operating frequency and gain is achieved. Self-healing of linearity is possible by tuning the bias current of major transistors.
3) For the digitally controlled oscillator, the load tank could be shared by two or three negative gm cells to broaden the frequency range.
4) For the six order Butterworth SC filter, the radiation verification will be performed in the near future to exam the RHBD performance of the filter.

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