Thick Film Packaging Techniques for 300°C Operation

by

Rui Zhang

A dissertation submitted to the Graduate Faculty of
Auburn University
in partial fulfillment of the
requirements for the Degree of
Doctor of Philosophy

Auburn, Alabama
December 12, 2011

Keywords: thick film, Silicon Carbide, die attach,
high temperature packaging

Copyright 2011 by Rui Zhang

Approved by

Robert W Johnson, Chair, Professor of Electrical & Computer Engineering
Robert N Dean, Assistant Professor of Electrical & Computer Engineering
Guofu Niu, Professor of Electrical & Computer Engineering
John Evans, Professor of Industrial and Systems Engineering

Abstract

Geothermal well logging and instrumentation applications require electronics capable of 300°C operation. SiC device technology enables the design and fabrication of analog circuits that can operate at these temperatures. However, to build functional systems operating at high temperatures, an interconnection and packaging technology must be developed to provide interconnectivity between different SiC devices and passive components. Key elements of a high temperature packaging technology include the interconnection substrate, die attach and wire bonding. New developments in each of these areas for high temperature operation are discussed in this work.

Thick film technology based on ceramics and metals has potential for higher operating temperatures. In this work, the effect of 300°C storage on the adhesion of different thick film conductors and multilayer dielectrics has been studied. In addition, the electrical properties of the dielectric, including leakage current, capacitance, and dissipation factor, have been studied as a function of temperature and of high temperature aging. The leakage current was also investigated as a function of high temperature aging under DC bias voltage.

Eutectic AuSn die attach was used with a Ti/TiW/Au backside die metallization for 300°C operation. Liquid Phase Transient (LPT) die attach process was developed. Results of die attach reliability based on shear strength were discussed after thermal

storage and thermal cycling tests. Investigation of Au wire bonding on different SiC die metallization was reported. Failure analysis after reliability testing was also performed.

Passive components were selected for this high temperature application and an attach process was developed. After an initial test, one resistor and one capacitor were selected for reliability testing after 300°C storage and thermal cycling tests. External lead attach was also investigated for next level device connection.

Before building the final amplifier module, a SiC die was attached in a ceramic DIP package and tested functional at 300°C. An amplifier module was fabricated on a multilayer thick film ceramic substrate. Passive components and the SiC chip were then assembled. The amplifier was tested as-built and after high temperature storage.

Acknowledgments

First and foremost, I would like to express my sincere gratitude to my advisor, Dr. R. Wayne Johnson. He has been a constant source of inspiration and ideas, given me great challenges and been very supportive with all kinds of help. His advice and research attitude have provided me with a model for my future career. I would also like to thank my advisory committee members, Dr. Robert Dean, Dr. Guofu Niu and Dr. John Evans for their support.

Appreciation is also expressed to cooperative support and continual assistance from Dr. Michael Bozack, Michael J. Palmer, John Marcell, Ping Zheng, Huihua Shu, Kun Fang, and ZhenZhen Shen throughout the course of this research. The support for this research provided by GE Global Research is also acknowledged.

This material is based upon work supported by the Department of Energy's Geothermal Technologies Program, under Award DE-FC36-08GO18181.

Finally, I would like to thank my parents for their continuous encouragement and support throughout my life.

Table of Contents

Abstract ii

Acknowledgments iv

List of Tables ix

List of Figures x

Chapter 1 Introduction 1

1.1 High Temperature Electronics (HTE) 1

1.2 Applications of High Temperature Electronics 1

1.3 High Temperature Electronics in Enhanced Geothermal Systems 3

1.4 High Temperature Electronics Packaging 4

1.4.1 SiC Device 5

1.4.2 Substrate Materials 8

1.4.3 Thick Film Metallization 9

1.4.4 Die Metallization 10

1.4.5 Die Attach and Wire Bonding 11

1.4.6 Passive Components Attach 13

1.5 Research Outline 13

Chapter 2 Thick Film Paste Selection 15

2.1 Introduction to Thick Film Technology 15

2.2 Thick Film Conductor Paste 16

2.3 Thick Film Dielectric Paste 18

2.4 Adhesion Test 18

2.5 Electrical Testing 33

2.5.1 Leak Current Measurement 34

2.5.2 Dissipation Factor and Capacitance Measurement 40

2.5.3 Biased Measurement 42

2.6 Summary 46

Chapter 3 High Temperature Die Attach and Wirebonding of Silicon Carbide Devices 48

3.1 Introduction 48

3.2 SiC Die Metallization 48

3.3 Off-eutectic AuSn Liquid Phase Transient (LPT) Die Attach 50

3.3.1 Liquid Phase Transient Bonding 51

3.3.2 Die Attach with Eutectic AuSn Paste 54

3.3.3 Die Attach with Eutectic AuSn Preform 55

3.4 Die Attach Reliability Test 57

3.4.1 High Temperature Thermal Aging Test 57

3.4.2 Thermal Cycling Test 63

3.5 Wire Bonding 64

3.5.1 Wire Bond Pad Metallurgy 64

3.5.2 Wire Bond Pull Test 65

3.5.3 Wire Bond Ball Shear Test 66

3.5.4 Daisy Chain Electrical Resistance 68

3.5.5 New Metallization Evaluation 69

3.6 Summary 72
Chapter 4 Passive Components Attach 73
4.1 Introduction 73
4.2 Passive Components Selection 73
4.3 Resistor and Capacitor Attach 76
4.3.1 Process Development 77
4.3.2 High Temperature Thermal Aging Test 79
4.3.3 Thermal Cycling Test 85
4.4 External Lead Attach 88
4.4.1 Background 88
4.4.2 Moly Tab Attach 89
4.4.3 External Lead Attach 90
4.5 Summary 91
Chapter 5 High Temperature Electronics Packaging 92
5.1 Single Chip DIP Packaging 92
5.2 Amplifier Module 94
5.2.1 Substrate Fabrication 94
5.2.2 Passive Components Attach 96
5.2.3 Die Attach and Wire Bonding 96
5.2.4 AmplifierTesting 97
Chapter 6 Conclusion and Future Work Recommendation 98
6.1 Thick Film Technology for 300°C Applications 98
6.2 Packaging for High Temperature SiC Based Devices 98

6.3 Passive Components for 300°C Applications 98

6.4 Recommendations for Future Work 99

References 100

List of Tables

Table 1.1 Application Area and Parameters for High Temperature Electronics 1

Table 1.2 Physical Properties of Semiconductor Materials 6

Table 1.3 Physical Properties of Semiconductor and Substrates Materials 9

Table 2.1 Properties of Selected Thick Film Conductors 19

Table 2.2 Properties of Selected Thick Film Dielectric..19

Table 2.3 Test Pattern for Electrical Test Vehicle 34

Table 2.4 Measured Line Width and Spacing on Comb Pattern.......................................38

Table 3.1 High Temperature Solder and Braze Alloys...50

Table 3.2 EDS Analysis on the Initial Bonding Layer 57

Table 3.3 EDS Analysis on the 320°C Aged Bonding Layer 60

Table 3.4 Average Daisy Chain Resistance (Ω) 69

List of Figures

Figure 1.1 Diagram of an Enhanced Geothermal System..4

Figure 1.2 Intrinsic Carrier Density Versus Temperature
for Si, GaAs, GaN, and SiC 7

Figure 1.3 Metallization Scheme for Semiconductor in HTE 10

Figure 2.1 Basic Screen Printing Process 16

Figure 2.2 Adhesion Test Vehicle 20

Figure 2.3 Standard 850°C Firing Profile 21

Figure 2.4 Illustration of Pull Test...22

Figure 2.5 Ceramic Surface after Pull Test...22

Figure 2.6 SEM Photos of DuraStrate Substrate in
Comparison with Standard Al_2O_3 23

Figure 2.7 Metal Surface after 500 hours Aging at 320°C 23

Figure 2.8 Auger Analysis on Samples as Build and
after 500 hours Aging at 320°C 24

Figure 2.9 Pull Strength as a Function of Aging (320°C) for
Conductor C101 and Dielectric D1 Fired at 850°C 25

Figure 2.10 Pull Strength as a Function of Aging (320°C) for
Conductor C101 and Dielectric D1 with Co-fire Process 26

Figure 2.11 Pull Strength as a Function of Aging (320°C) for
Conductor C101 and Dielectric D1 Fired at 980°C 27

Figure 2.12 Pull Strength as a Function of Aging (320°C) for
Conductor C105 and Dielectric D1 fired at 850°C..28

Figure 2.13 Pull Strength as a Function of Aging (320°C) for

Conductor C110, C101 and Dielectric D1, D4 fired at 850°C 29

Figure 2.14 Pull Strength as a Function of Aging (320°C) for
Conductor C109 and Dielectric D1 fired at 850°C....30

Figure 2.15 Pull Strength as a Function of Aging (320°C) for
Conductor C109 on Ceramic fired at Different Conditions....31

Figure 2.16 Pull Strength as a Function of Aging (320°C) for
Conductor C109 on Dielectric D1 fired at Different Conditions....32

Figure 2.17 Conductor C109 Pulled off from Ceramic
and Dielectric D1 fired at 980°C 32

Figure 2.18 Electrical Test Vehicle 34

Figure 2.19 Capacitor Leakage Current Density at
100V Bias as a Function of Storage Time at 320°C....35

Figure 2.20 Capacitor Leakage Current Density at 100V Bias
as a Function of Temperature (Test Vehicle Fired at 980°C)....36

Figure 2.21 Designed Comb Test Pattern....38

Figure 2.22 Initial Leakage Current at 100V Bias as a
Function of Temperature (Test Vehicle Fired at 980°C)....39

Figure 2.23 Test Fixture for Capacitance and Dissipation Factor Measurement 40

Figure 2.24 Initial Capacitance as a Function of Frequency
and Temperature (Test Vehicle Fired at 980°C)....41

Figure 2.25 Initial Dissipation Factor as a Function of Frequency
and Temperature (Test Vehicle Fired at 980°C)....42

Figure 2.26 Test Pattern for Leakage Current under Bias 42

Figure 2.27 Wires Held on Test Vehicle 43

Figure 2.28 Stacked Test Fixtures 43

Figure 2.29 Leakage Current as a Function of Aging Time 44

Figure 2.30 Comb Pattern after 1000 hours Biased Aging....45

Figure 2.31 Corner of Capacitor after 1000 hours Biased Aging....45

Figure 2.32 Leakage Current as a Function of Aging Time for 300 Minutes 46

Figure 3.1 SiC Test Die with Daisy Chain Pattern 49

Figure 3.2 Au-Sn Phase Diagram 52

Figure 3.3 Wire bonding and Die Shear Test Vehicle 53

Figure 3.4 Typical X-Ray Result for SiC Die Attach with AuSn Paste 55

Figure 3.5 X-Ray Result for SiC Die Attach with AuSn Preform....................................56

Figure 3.6 Cross-section Micrograph of Initial Die Attach with AuSn Preform...............57

Figure 3.7 Failure Mode on Substrate after Shear Test 58

Figure 3.8 Shear Strength as a Function of Aging (320°C) with C101 on Al_2O_3.............59

Figure 3.9 Wirebonded Sample After 2000 hour Aging at 320°C 59

Figure 3.10 Cross-section Micrograph of 320°C Aged
Die Attach with AuSn Preform..60

Figure 3.11 Shear Strength as a Function of Aging (320°C) with C109 and D1 61

Figure 3.12 Failure Mode for Die Shear as Built and after Aging 62

Figure 3.13 Thermal Cycle Profile 63

Figure 3.14 Schematic Sequence of Ball-Stitch Wire Bonding..64

Figure 3.15 Wire Pull Strength as a Function of Aging (320°C) 66

Figure 3.16 Ball Shear Strength as a Function of Aging (320°C) 67

Figure 3.17 Wire Bonding Pad after Ball Shear Test on Sample
after 1000 Hours Aging at 320°C 68

Figure 3.18 Auger Test Result for 0 hour Sample
and 500 hour Aged Sample (320°C)...68

Figure 3.19 Test Vehicle for Daisy Chain Resistance Measurement 69

Figure 3.20 Wire Pull Strength as a Function of Aging (320°C)
with New Metallization...70

Figure 3.21 Ball Shear Strength as a Function of Aging (320°C)
with New Metallization....71

Figure 3.22 Average Daisy Chain Resistance (Ω) as
Function of Aging (320°C) with New Metallization....72

Figure 4.1 Vishay WSC4527 Resistor....74

Figure 4.2 Capacitance and Dielectric Loss for
TRS High Temperature Capacitor....75

Figure 4.3 Passive Component Attach Test Vehicle....77

Figure 4.4 X-Ray Result of Passive Component Attach with AuSn Paste....77

Figure 4.5 X-Ray Result of Passive Component Attach with AuSn Preform....78

Figure 4.6 Side View of KEMET Capacitor after Bonding....79

Figure 4.7 Test Vehicle for Mini-Systems Resistor and KEMET Capacitor....81

Figure 4.8 Shear Strength of Passive Component after Aging at 320°C....82

Figure 4.9 Failure Mode on the Thick Film Metallization
after (a) 500 (b) 1000 (c) 2000 Hours Aging at 320°C....82

Figure 4.10 Failure Mode on Resistor after 2000 Hours Aging at 320°C....83

Figure 4.11 Resistor Solder Joint (a) As Built (b) After 2000 Hours Aging at 320°C....83

Figure 4.12 Initial Failure Mode for KEMET Capacitor
on (a) Thick Film Metallization (b) Capacitor Body....84

Figure 4.13 KEMET Capacitor Failure Mode on the Thick Film Metallization
after (a) 500 (b) 1000 (c) 2000 Hours Aging at 320°C....84

Figure 4.14 KEMET Capacitor Sheared after 2000 Hours
Aging at 320°C (a) Top View (b) Side View....85

Figure 4.15 Shear Strength of Passive Component after Thermal Cycles....86

Figure 4.16 Failure Mode on the Thick Film Metallization
after (a) 200 (b) 1000 Thermal Cycles....86

Figure 4.17 Mini-System Resistor Sheared after 500 Thermal Cycles....87

Figure 4.18 Mini-System Resistor Sheared after 1000 Thermal Cycles 87

Figure 4.19 Failure Mode on the Thick Film Metallization after 100 cycles 88

Figure 4.20 Failure Mode on the Thick Film Metallization after 500 cycles 88

Figure 4.21 Failure Mode on the Thick Film Metallization after 1000 cycles 88

Figure 4.22 Configuration of Wire Welding Substrate...90

Figure 4.23 Wire Welding Substrates with Peripheral Moly Tabs Attached 90

Figure 5.1 16-Pin Ceramic DIP Package 92

Figure 5.2 X-Ray on Amplifier Attached to DIP Package 93

Figure 5.3 Amplifier Attached and Wirebonded to DIP Package 93

Figure 5.4 Designed Amplifier Test Board...94

Figure 5.5 Substrate Fabrication Process..95

Figure 5.6 Fabricated Substrate 96

Figure 5.7 Resistor Attachment Process 96

Figure 5.8 Die Attach and Wirebonding Process..97

Figure 5.9 Assembled Test Board...97

CHAPTER 1 INTRODUCTION

1.1 High Temperature Electronics (HTE)

The term "high temperature electronics" (HTE) is defined in various ways in the literature, depending on the areas of application. For this thesis, HTE is taken to mean "electronic operation at temperatures in excess of those normally encountered by conventional, silicon-based semiconductors [1]". This temperature limit has been set by convention at 75°C, with some military systems being operated at a maximum temperature of 125°C. However, there are growing demands for electronics that must operate at a much higher temperature.

1.2 Application of High Temperature Electronics

Interest in the area of high temperature electronics has increased dramatically in recent years. The primary applications for high temperature electronics include automotive, well logging, power grid, nuclear reactors, aircraft, and space exploration. For example, the temperature of the instrumentation of combustion engine environments is typically greater than 300°C [2]; Measurement-While-Drilling (MWD) tools for oil, natural gas, and geothermal wells have to withstand reservoir ambient temperatures up to 350°C; Applications for Venus planetary exploration require electronics operating at 500°C. Table 1.1 lists a number of high temperature applications and summarizes their temperature, operating times, and other requirements [3].

Table 1.1 Application Area and Parameters for High Temperature Electronics. [3]

Application	Temperature (°C)	Minimum Duration	Duty	Other Environmental Factors
Well-logging-gas & oil (down-hole) instrumentation	150 to 300	Few hours-years	Intermittent/cyclical, or continuous	Temperature cycling, chemicals, pressure, mechanical stress, possibly radiation
Well-logging-geothermal	150 to 400	Few-100 hours	Intermittent/cyclical	Temperature cycling chemicals, pressure, mechanical stress
Aircraft systems-on engines & smart transducers	300 to 500	1000 hours	Intermittent/cyclical	Temperature cycling,vibration, stress, fuel/oil/chemicals
Aircraft engine R & D	500 to 600	100 hours	Intermittent/cyclical (one-shot acceptable)	Temperature cycling,shock/vibration
Automobiles	150 to 250 (700)	8000 operating hours, 10 years "shelf"	Intermittent/cyclical	Temperature cycling,vibration, fuel/oil/chemicals, rough handling
Fossil-fuel energy plants	400 to 500	Months-years	Continuous	Radiation
Nuclear reactors	200 to 450	Months-years	Continuous	Radiation
Space Exploration	125 to 485	Month - years	Intermittent/cyclical, or continuous	Temperature cycling chemicals, pressure, Radiation

The elevated temperature may be a result of high environment temperature or it may develop due to high power dissipation and difficulties of effective heat removal. Heat buildup in dense electronics and the concept of un-cooled high power electronics have been an attractive research topic over the years. Operating electronic devices at higher temperature could eliminate or reduce the need for bulky heat transfer hardware and cooling systems. For example, in the aircraft industry, where weight reduction is a major cost driver, elimination of the heavy hydraulic cooling systems for lighter electrical systems is always desired [2].

There is a growing body of evidence that high temperature electronics have greatly improved operating lifetimes at lower temperatures. Honeywell HT SOI electronics rated for 5 years at 225ºC have a potential for 10 years at 200ºC and 20 years at 150ºC [4]. The

improvement of electronics reliability at high temperature can be of substantial benefit to the reliability and lifetime of electronics used at conventional temperatures. High temperature exposure and operation has also been an important part of the reliability evaluation and improvement for conventional temperature electronics.

1.3 High Temperature Electronics in Enhanced Geothermal Systems

Until recently, geothermal systems have only exploited resources where naturally existing hot fluid and rock permeability is sufficient to allow heat extraction from production wells. However, the vast majority of geothermal energy within reach of conventional techniques is in dry and non-permeable rock [5].

A DOE sponsored study by MIT concluded that geothermal energy could provide 100,000 MWe or more in 50 years by using advanced technology known as Enhanced Geothermal Systems (EGS) [6][7]. EGS reservoirs are made by drilling wells into hot but dry rock and fracturing the rock sufficiently to enable a fluid (water) to flow between the wells. The fluid circulates along permeable pathways, picking up in situ heat, and is then pumped to the surface through the production wells. At the surface, the hot fluid passes through a power plant where electricity is generated. The fluid is recycled into the reservoir through the injection well to complete the circulation, as shown in Figure 1.1 [6]. EGS may be expanded by adding additional production and injection wells, which could allow heat harvesting from large areas and increase power generation capacities. EGS in multiple geological environments at various depths will enable geothermal energy to increase in scale and be an important contributor to the U.S. energy portfolio as a source of clean and renewable energy. [8].

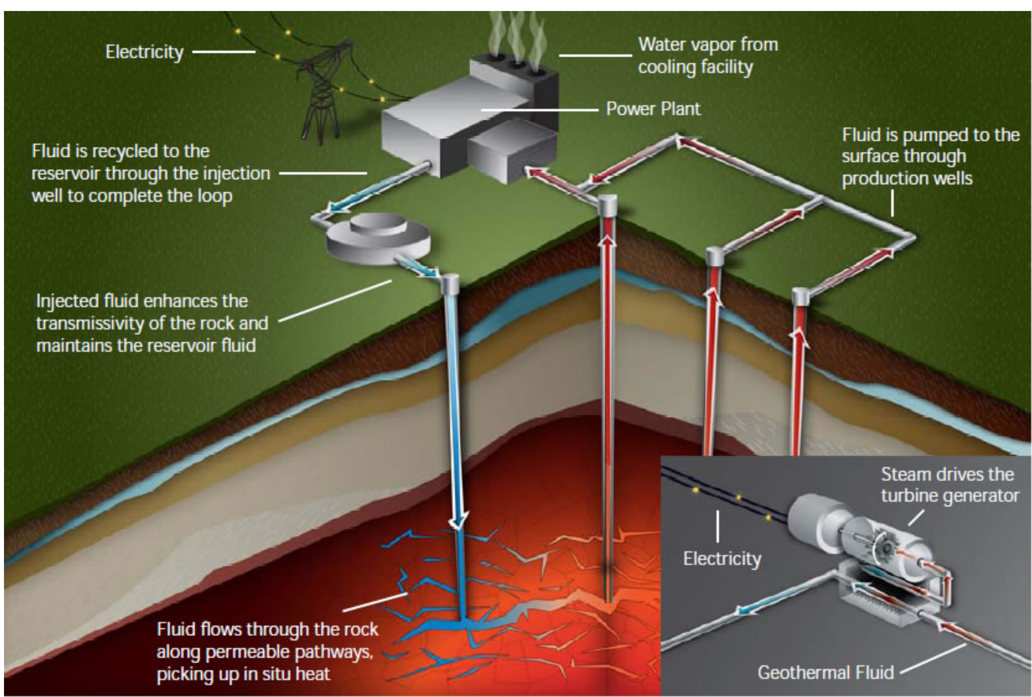


Figure 1.1 Diagram of an Enhanced Geothermal System [6]

In EGS, typical measurements made by a measurement-while-drilling (MWD) tool include: azimuth, inclination, temperature, pressure, and strain. For maintenance and monitoring purpose, fluid flow, data logging, and data transmission are also required. The control of these parameters enables the productivity of the EGS to be optimized.

The MIT study indicates that high temperature instrumentation for geothermal is a key technology deficiency [6][7]. Today most geothermal tools use conventional oil patch electronics operating in a heat shield or dewar flask [9]. The heat shields used in geothermal tools are highly specialized and relatively large and expensive. Shielded or flasked devices do not provide for long term operation and there are also many sensors that cannot be flasked. Logging and well monitoring instruments capable of operation at high temperatures for days or even years remain commercially unavailable.

1.4 High Temperature Electronics

The keys to successful high temperature circuits are the availability of stable high

temperature electronic components (integrated circuits, resistors, capacitors, etc.) and the packaging of these components using the proper materials [2]. In the following sections the semiconductor, packaging materials and processes, and passive components for high temperature electronics are discussed.

1.4.1 SiC Device

Silicon has been the dominant semiconductor material over the last 50 years. However, the long term operating temperature for devices made with Si is not more than 150°C. Beyond this temperature, Si-based devices are not able to function efficiently, especially when the high temperature is combined with a high power, high frequency and high radiation environment [10]. Silicon on insulator (SOI) technology extends the performance of electronics toward higher temperature up to 300°C. Beyond 300°C, SOI devices would not be applicable.

To solve this problem, a semiconductor with a wider band gap is a better choice to fabricate devices for high temperature applications. The band gap energy, Eg, is a measure of the amount of thermal energy needed to ionize the particular semiconductor material. Wide band gap (WBG) semiconductors offer various advantages over traditional Si-based devices, including high thermal conductivity, high breakdown voltage, high temperature stability, and low chemical reaction rates. Examples of WBG semiconductors are silicon carbide (SiC), gallium nitride (GaN), gallium phosphide (GaP) and diamond. Table 1.2 summarizes some of the physical properties of these materials in comparison with traditional semiconductors [11] [12] [13]. Due to the dependence of the physical properties on the doping level, impurities, temperature, and structural defects, these values can be different from other published literature.

Table 1.2 Physical Properties of Semiconductor Materials [11] [12] [13]

	Silicon	GaAs	AlGaAs	GaN	SiC	Diamond
Band Gap (eV)	1.1	1.3	1.9	3.39	2.9	5.5
Breakdown Field (kV/cm)	250	300	500	3300	2500	10000
Thermal Conductivity (W/cm/K)	1.5	0.5	0.1	1.3	4.9	20
Electron Mobility (RT) cm^2/v-s	1400	4000	3000	1250	250	2200
Hole Mobility (RT) cm^2/v-s	600	400		250	50	1600
Electron Sat Velocity (10^7 cm/s)	1.0	1.0	1.0	2.7	2.0	2.7
Dislocation Energy (eV)	13	9	9	\	22	\
Melting Point (ºC)	1412	1238	1304	1800	2700	>3300

The intrinsic carrier density n_i is the most important physical property that increases exponentially with temperature, which leads to increased leakage current and finally the failure of the junction once the density of intrinsic carrier exceeds the doping density. The intrinsic carrier density n_i of a semiconductor depends on temperature and the band gap energy of the semiconductor [11],

$$n_i = \left(\frac{2\pi kT}{h^2}\right)^{3/2} (m_{dh} m_{de})^{3/4} e^{-E_g/2kT}$$

where k and h are Planck's and Boltzmann's constants, T is the absolute temperature, m_{de} and m_{dh} are the electron and hole effective masses, and E_g is the band gap energy. The intrinsic carrier density is plotted in Fig 1.1 for Si, GaAs, GaN, and SiC, showing an exponentially increase with temperature and decrease with band gap. As an example, a carrier density of $10^{14}cm^{-3}$ is reached at 200°C for Si but not until 900°C for SiC.

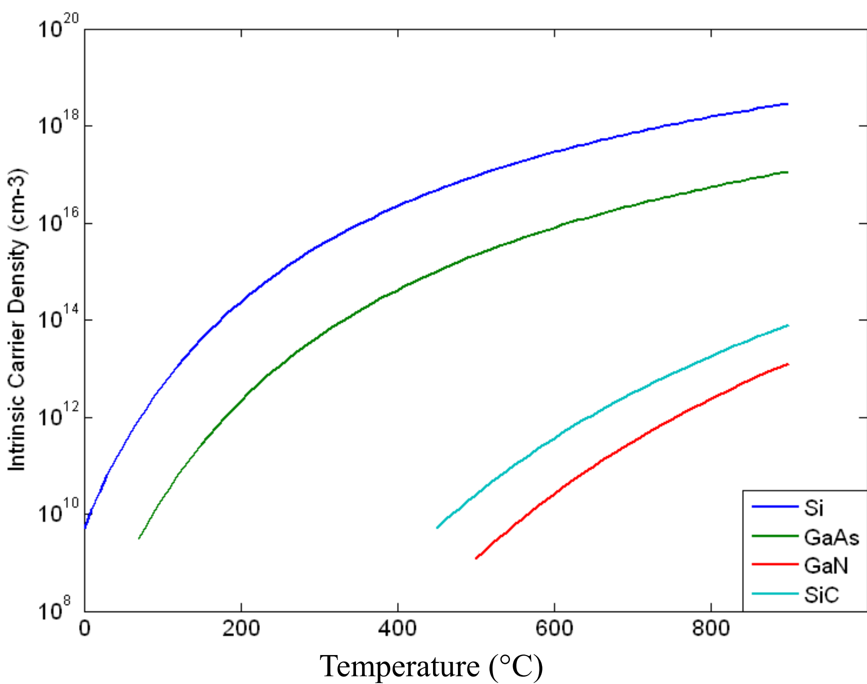


Figure 1.2 Intrinsic Carrier Density Versus Temperature for Si, GaAs, GaN, and SiC

Among all the candidates, SiC is by far the most developed wide band-gap semiconductor due to the commercial availability of high quality SiC bulk wafers, known device processing techniques, and the ability to grow thermal oxides. Various SiC semiconductor devices have recently been demonstrated to be functional at temperatures as high as 600°C [14] [15]. The most beneficial properties that make SiC an attractive semiconductor material are [16] [17]:

- Wide band gap energy: SiC based electronic devices can operate at extremely high temperatures without suffering from intrinsic conduction effects because of the wide band gap energy. The much smaller intrinsic carrier concentration of SiC theoretically permits device operation at temperatures exceeding 800°C. Also, this property allows SiC to emit and detect short wavelength light which makes the fabrication of blue light emitting diodes and ultraviolet detectors possible.

- High breakdown electric field: SiC can withstand a voltage gradient over eight

times greater than Si or GaAs without undergoing avalanche breakdown. This property enables the fabrication of very high-voltage, high-power devices such as diodes, power transistors, power thyristors and surge suppressors, as well as high power microwave devices. Additionally, it enables the blocking voltage region of a power device to be roughly 10 times thinner and 10 times more heavily doped, permitting roughly a 100-fold decrease in the blocking region resistance. It allows the devices to be placed very close together, providing high density packing for integrated circuits.

- High thermal conductivity: SiC is an excellent thermal conductor. Heat will flow more readily through SiC than other semiconductor materials. This property enables SiC devices to operate at extremely high power levels and still dissipate the large amounts of excess heat generated. SiC power devices can be made smaller and require less cooling, which lead to extremely high power densities and efficiencies.

- High saturated electron drift velocity: SiC devices can operate at high frequencies (RF and microwave) because of the high saturated electron drift velocity of SiC.

- High bonding energy between Si and C: This property gives SiC high mechanical strength, chemical inertness, and radiation resistance.

These properties allow SiC devices to offer tremendous benefits over other available semiconductor devices in a large number of industrial and military applications and make SiC the leading candidate for high power, high temperature electronics.

1.4.2 Substrate Materials

Organic based substrates have a glass transition temperature (T_g) in the 125°C to 200°C range. Above this temperature there is a significant increase in CTE and a decrease in mechanical properties. For high temperature applications, ceramic based technologies

must be considered. Table 1.3 [2] presents the properties of Si and SiC materials along with aluminum oxide (Al_2O_3) and aluminum nitride (AlN) ceramic substrates. It suggests that AlN is an ideal candidate for packaging SiC devices for high temperature applications, since its coefficient of thermal expansion (CTE) is closely matched to SiC. This matched CTE will provide excellent reliability for high temperature application that requires a large number of thermal cycles.

Al_2O_3 is the most widely used ceramic substrate and a wide variety of Al_2O_3 packages are commercially available. The CTE of Al_2O_3 is relatively high compared to that of SiC, which will limit the number of thermal cycles to failure. However, for applications that do not require large numbers of thermal cycles, Al_2O_3 could be a better choice considering the mature metallization technology on Al_2O_3 and the high cost of AlN.

Table 1.3 Physical Properties of Semiconductor and Substrates Materials [2]

	Si	SiC	Al_2O_3	AlN
Density, g/cm^3	2.3	3.21	3.75	3.31
Hardness, GPa	11.5	24.0	19.0	12.0
Strength, MPa	250	450	350-400	350-400
Elastic modulus, GPa	130	470	397	320
Thermal conductivity, W/mK	150	300	25	200
Thermal expansion coefficient, ppm/°C	3.5	3.7	7.2	4.1
Dielectric constant (@1MHz)	11.0	42	9.4	8.9
Dissipation Factor(@1MHz)	0.09	0.05	0.0004	0.0005

1.4.3 Thick Film Metallization

The term "thick film" is derived from the fact that the fired film is fairly thick, varying from 0.2 mil (5.08μm) to 2 mils (50.8 μm) [18]. In the thick film process, the individual layer is deposited by screen printing. The thick film material to be printed is

referred to as an ink or paste. The ink contains three components [19]: a functional phase which defines the electrical properties of the fired film (e.g.: conductor, dielectric, resistor), a binder which provides adhesion between the fired film and the substrate, and the vehicle which established the printing characteristics. More details about thick film technology will be given in Chapter 2.1.

Thick film metallization that is intended for high temperature operation must resist surface oxidation and migration while maintaining good adhesion to the substrate. Gold-based thick film materials were preferred for electrical interconnections and conductive die attach for high temperature applications.

1.4.4 Die Metallization

The semiconductor must be connected to the substrate with other components to provide a functional system. The temperature limit for devices is imposed by the die metallization rather than the semiconductor's inherent capability. A typical metallization scheme for a semiconductor used in high temperature application consists of a contact layer, a diffusion barrier layer, and a cap layer, as sketched in Figure 1.3.

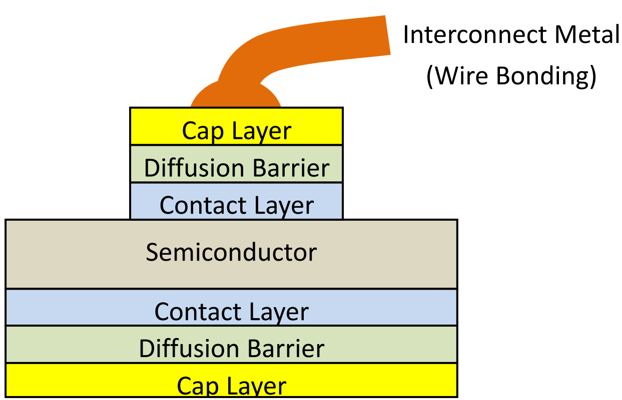


Figure 1.3 Metallization Scheme for Semiconductor in HTE.

Metals with high electrical conductivity needed for interconnections often do not

form chemically stable semiconductor interfaces [11]. The solution is to separate the two functions of making a contact and interconnecting devices by inserting a diffusion barrier and a cap layer. The contact is made with a material that is thermodynamically stable in contact with the semiconductor, providing good adhesion, high environmental resistance, as well as high electrical conductivity. The diffusion barrier must be inert to the contact and the cap layer. The cap layer must have good wettability with the die attach material, or, in the case of die surface metallization, must have good wire bonding properties or solder ball attach properties (for flip chip). For example, in this proposed research, Ti/TiW/Au is selected as the backside metallization. The Ti is used as a contact layer that provides strong adhesion to the semiconductor, and the TiW layer is used as the diffusion barrier.

To develop such a multilayer structure, it is not only the choice of materials that is important but also the way in which they are prepared [11]. The micro-fabrication techniques used affect the metallurgical properties of the layers, which may further affect diffusion rates or intermetallic formation. Developing a suitable metallization stack compatible with high temperature operation is difficult, and a great deal remains to be done.

1.4.5 Die Attach and Wire Bonding

Die attach (also known as die mount or die bond) is the process of attaching the chip to the substrate or the semiconductor package. The die attach material must be compatible with the substrate and die backside metallization, have a sufficiently high melting point after die attach, and not form intermetallics which degrade the bond strength with time at temperature [20]. Furthermore, thermal cycling must also be

considered depending on the application. Although in some applications the device might require only a few temperature cycles (such as in well logging, power plant monitoring, and space exploration), in other applications they may face many cycles (such as in automobiles and aircraft). Temperature cycling can be a more severe issue than continuous operation at an elevated temperature, due to the strain from thermal expansion differences [3].

For high temperature applications, Au based eutectic alloys have been proposed as promising die attach materials because of their good compatibility with the die and substrate metallization, excellent electrical conductivity, thermal conductivity and corrosion resistance [10][20]. The die attach material used in this research was eutectic AuSn. A eutectic alloy is an alloy with the lowest melting point possible for the metals combined in the alloy. The idea is to dissolve Au from both the substrate and die into the molten eutectic AuSn perform, increasing the Au concentration and thus increasing the melting point.

Wire bonding is the process of providing electrical interconnection between the semiconductor I/O pads and the corresponding substrate pads using very fine wires. This is accomplished using a combination of heat, pressure and/or ultrasonic energy. Once the surfaces are in intimate contact, electron sharing or interdiffusion of atoms takes place, resulting in the formation of a metallurgical bond. [21]

The wire used in wirebonding is usually made of gold (Au), aluminum (Al), and sometimes copper (Cu) and platinum (Pt). In general, it is desirable that the bonding pad and wire be of the same material because intermetallic growth due to interdiffusion and interface corrosion can occur between dissimilar metals at high temperatures [22]. For

example, Al wire cannot be used on a Au pad in high temperature applications due to diffusion, formation of brittle Au-Al intermetallics, as well as Kirkendall voiding, which can lower the physical and mechanical properties of the bond [20]. Au possesses higher strength at high temperature than Al, and Au ball bonding on gold pad provides a more reliable option for devices operated at high temperature.

1.4.6 Passive Components Attach

Passive components are a necessary part in most electronic systems. Although modern semiconductor technology can build on-chip resistors and capacitors, those passive component usually have a loose tolerance and only very small capacitors can be fabricated on chip. This on-chip fabrication process becomes much more difficult for passive component that need to work at high temperature, due to the very limited choice of dielectric materials. Passive components have received relatively little attention compared to semiconductor materials and processing techniques. As a result, capacitors are often the weakest point in designing electronics for high temperature applications.

The passive components selection, termination material selection, and reliability assessment for this research was done by GE Global Research [23] at Niskayuna, NY. Here the focus is on the component attachment process. AuSn was used for passive attach.

1.5 Research Outline

The goal of the project was to identify and develop packaging materials and processes for high-temperature electronics that can be used to monitor wellbore conditions in enhanced geothermal systems. The environmental conditions of temperature (300°C) and depth (10 km) pose significant challenges to the sensor and electronic

systems necessary to monitor wellbore conditions.

In Chapter 2, thick film technology is briefly discussed. The adhesion of several thick film conductor and dielectric pastes on Al_2O_3 substrates and on each other were tested. The adhesion as a function of aging at 300°C was also investigated. The dielectric properties: leakage current, capacitance and dissipation factor as a function of temperature as-built and after aging is also reported.

Chapter 3 describes the die attach and wire bonding of SiC test die. Off-eutectic AuSn solder was used for die attach and the results of die shear strength are discussed after 300°C storage and thermal cycling tests. Investigation of Au wire bonding on different SiC die metallization is also reported. Failure analysis after reliability testing was also performed.

Chapter 4 discusses the passive component attach process. Four components from various vendors were tested initially and two of them were selected for reliability test after 300°C storage and thermal cycling tests. External lead attach were also investigated for next level device connection.

Chapter 5 reports the SiC die attach in a ceramic DIP package. Then an amplifier module was fabricated on a multilayer thick film ceramic substrate. The substrate metallization was selected based on the results from Chapter 2. Passive components and the SiC chip were then assembled. The amplifier was tested as-built and after high temperature storage.

Chapter 6 summarizes the conclusion from this work and proposed ideas for future work.

CHAPTER 2 THICK FILM PASTE SELECTION

2.1 Introduction to Thick Film Technology

The technology used to manufacture thick film hybrid microelectronic circuits was introduced in the 1950s [24]. At that time it was considered an alternative approach to printed circuit boards (PCBs). With years of research and advances in materials technology, the current thick film technology is favored for high reliability, high power, and high temperature application.

In the thick film process, the individual layer is deposited by screen printing, which deposits a viscous ink (or paste) on to a base material (substrate) through a woven screen with a photo defined polymer pattern of the desired geometry. Figure 2.1[25] illustrates the process for screen printing. The substrate is usually held by vacuum and its position can be finely adjusted to ensure good alignment between consecutive layers. The ink is applied to the surface of the screen and the flexible squeegee travels across the screen, pushing the ink through the open areas of the screen mesh. At a point immediately behind the squeegee, the screen peels away from the substrate and, due to the surface tension between the ink and the substrate, leaves a deposit of paste in the desired pattern on the substrate [24].

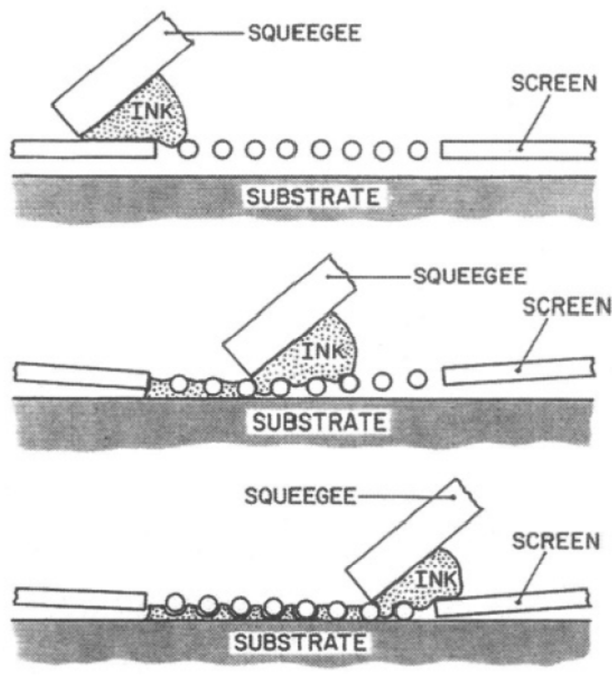


Figure 2.1 Basic Screen Printing Process [25]

After printing, the pastes are usually dried at 150°C for 15 minutes to remove the organic solvents. Then the films proceed to the firing stage. In some circumstances, however, they may be overprinted with another thick film paste, dried, and fired together, known as a co-fire process. The firing temperature profile typically includes 10 min at a peak temperature of 850°C and an overall firing cycle time of 30 to 60 minutes.

At the initial firing stage, the remaining organic carrier is removed from the film. At a temperature between 300°C and 500°C, the nonvolatile resin portion of the vehicle is pyrolyzed [19]. In the temperature range 600°C to 850°C, the glass flows, sintering of particles occurs, and chemical reactions take place to form the final film and to provide adhesion to the substrate. Precious metal conductors are fired in air while copper conductors require firing in an inert atmosphere such as nitrogen. The print, dry and fire steps are repeated to fabricate the interconnection structure.

2.2 Thick Film Conductor Paste

Thick film conductors provide interconnection between the components, attachment pads for passive components as well as bare die, wirebonding pads and terminations for thick film resistors. The three main components in a thick film paste are: a functional phase which defines the electrical properties of the fired film (e.g.: conductor, dielectric, resistor), a binder which provides adhesion between the fired film and the substrate, and the organic vehicle which established the printing characteristics.

For conductors, the functional phase may be gold, silver, copper, palladium-silver, platinum-silver, palladium-gold, or platinum-gold [19]. The metallurgy chosen depends on a number of engineering factors including wire bondability, solderability, environmental requirements, electrical conductivity, and cost.

The binder systems for thick film conductors are usually composed of glass compositions and oxide additives. Numerous oxides such as copper oxide and cadmium oxide promote adhesion to alumina substrates by formation of spinel compounds such as copper aluminate ($CuAl_2O_4$) [26]. This type of bonding mechanism is a chemical or reactive bond, which generally requires firing temperatures of 900°C or higher for the chemical reaction [19]. However, the detailed composition used in any commercial thick film ink, especially the binder system, is never published for proprietary reasons.

Thick film metallization that is intended for high temperature operation must resist surface oxidation and migration while maintaining good adhesion to the substrate. Silver based thick film conductor has poor solder leach resistance and has an inherent tendency to migrate in the presence of an electric field. Gold based thick film conductors exhibit high conductivity, excellent resistance to oxidation, corrosion and migration. It also has excellent wire bondability with Au wire and the ability to be die attached with Au based

die attach materials. Additions of platinum to Au conductor formulations can result in materials with excellent solderability and leach resistance at the expense of conductivity. [27]

2.3 Thick Film Dielectric Paste

Dielectrics serve three primary roles in thick film hybrid circuit applications: cross-over insulation between conductor layers, formation of capacitors, and encapsulation of the hybrid substrate.

Screen printed parallel plate capacitors are not widely used due to a low capacitance density compared to chip capacitors. It is also difficult to achieve the designed capacitance value. The trimming process can help but the cost is too high.

Thick film dielectric encapsulations are mainly used to protect resistors during trimming and the circuit from harsh environmental condition during operation. Encapsulant dielectrics are formulated with low melting point glasses to allow a reduced firing temperature (500°C) since it is usually the last layer to be processed.

For this research, the main function of the dielectric was to provide cross-over insulation between two conductive layers. Cross-over dielectrics are comprised of a ceramic material, a glass serving as the binder, and an organic vehicle. These films are required to have a low dielectric constant, low dissipation factor (low electrical loss), high breakdown voltage, high insulation resistance, a CTE matched to the substrate, and a smooth, pinhole-free surface finish [19].

2.4 Adhesion Test

A multilayer thick film circuit built with conductors and dielectrics for high temperature operation must maintain good adhesion to the substrate and to each other

after high temperature exposure. To achieve this requirement, several thick film conductor and dielectric inks that contain different binding systems were evaluated for use in high temperature applications. Their properties were summarized in Table 2.1 and Table 2.2. Some of them have previously been demonstrated for 500°C use on Al_2O_3 substrates [28], the others are recommended by the vendors.

Table 2.1 Properties of Selected Thick Film Conductors

Ink No.	Property	Fired thickness	Lin Resolution (Lines/Spaces)	Resistivity (m Ω /sq)	Viscosity (Pa.S)*
C101	Cd free, Au wire bondable	6-9μm	125/125μm	≤7.0 (@10μm fired thickness)	350-500
C105	Mixed bonded Au and Al wire bondable	8-11μm	125/125μm	≤7.0 (@10μm fired thickness)	240-260
C110	High density. Fine printing, ultra fine line etching.	5μm	75/75μm	≤5.0 (@10μm fired thickness)	240-360
C109	Pb, Cd, Ni free.	12-16μm	200μm	≤9.5 (@12μm fired thickness)	200-280

* Brookfield 2xHA, UC&SP, SC4-14/6r, 10rpm, 25°C

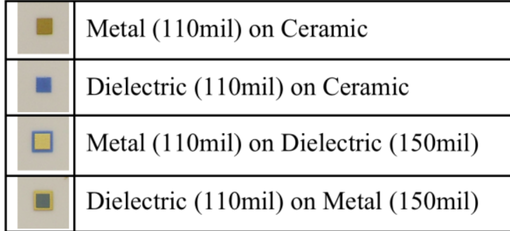
Table 2.2 Properties of Selected Thick Film Dielectric

Ink No.	D1	D4
Fired thickness (μm)	40-60 (3 fired layers)	45-50 (3 fired layers)
Breakdown voltage (Vdc/mil)	>700 (minimum)	>400
Dielectric Constant	6-10	8-10
Dissipation Factor (%)	≤0.5	<0.5
Insulation Resistance (Ω @100Vdc)	$>10^{11}$	$>10^{12}$
Viscosity (Pa.S)*	220-295	150-250

*Brookfield HBT, UC&SP, 10rpm, 25°C

An adhesion test vehicle was designed and fabricated to characterize the adhesion of thick film materials on a 2” by 2” alumina substrate. The three-layer test vehicle provided adhesion testing of metal to ceramic, metal to dielectric, dielectric to ceramic, and dielectric to metal. A test vehicle sample along with pad dimensions is shown in Figure

2.2. Each layer was printed, and then fired. Two dielectric layers were sequentially printed and fired as is common in multilayer thick film processing to eliminate pinholes. The inks were printed and dried at 150°C for 15 minutes. The standard firing profile was a 60-minutes profile with an 850°C peak temperature held for 10 minutes. The actual profile used here was recorded with a thermocouple and plotted in Figure 2.3.



	Metal (110mil) on Ceramic
	Dielectric (110mil) on Ceramic
	Metal (110mil) on Dielectric (150mil)
	Dielectric (110mil) on Metal (150mil)

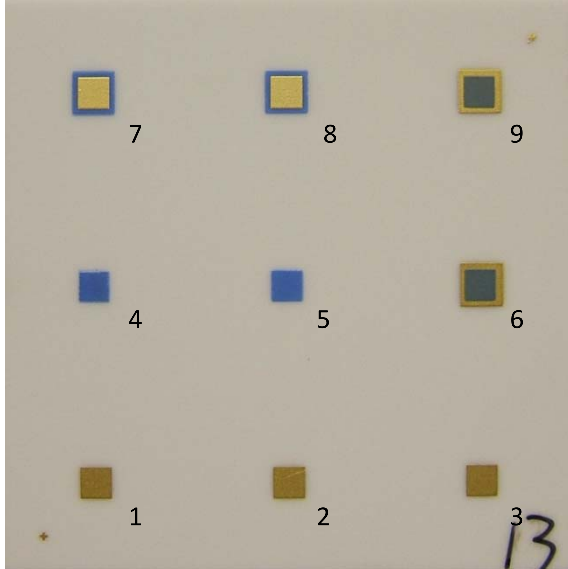


Figure 2.2 Adhesion Test Vehicle

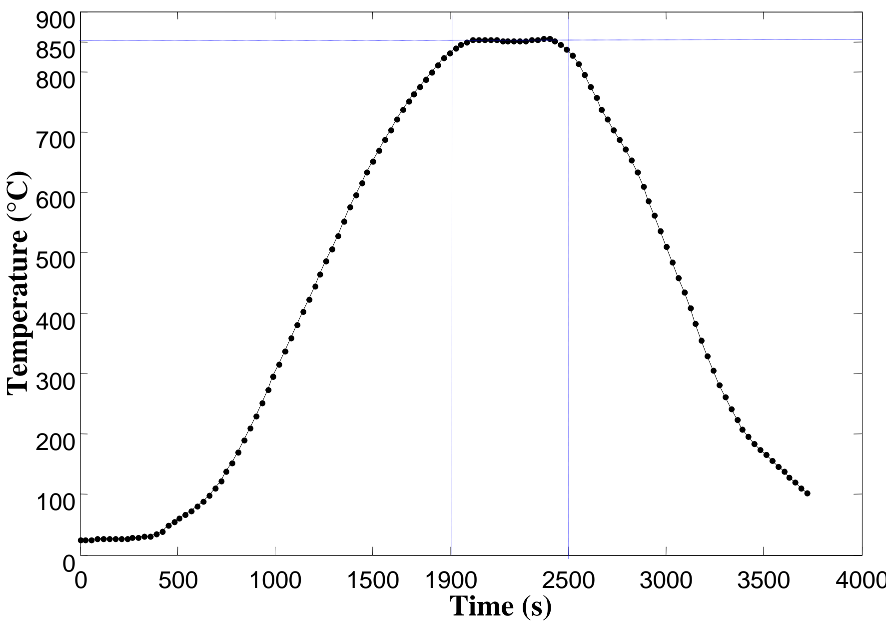


Figure 2.3 Standard 850°C Firing Profile

Then the substrate was diced into 9 pieces (0.67” by 0.67”). To evaluate the adhesion of the thick film inks, aluminum studs with epoxy coated ends from Quad Group were cured to the thick film pad and the bottom substrate was attached and cured to a ceramic plate coated with epoxy to reinforce the substrate. The pull stud end had a diameter of 106 mils and the epoxy coated on it had a tensile strength of 10,000 to 13,000 psi. Based on the pull stud diameter and epoxy tensile strength, the epoxy will start to fail when the pull strength reaches 88.2lb to 114.7lb. A clamp was used to clamp the part and the ceramic plate together during epoxy cure at 150°C for an hour. The pull test was conducted on a Sabastian-V Mechanical tester and this process is illustrated in Figure 2.4. The most severe tests that ultimately limit the number of applications for the thick film conductors are aging tests, including storage at elevated temperatures [26]. The pull test was conducted on samples as built and samples after aging at 320°C for 500, 1000, 1500 and 2000 hours. All of the pull tests were performed at room temperature.

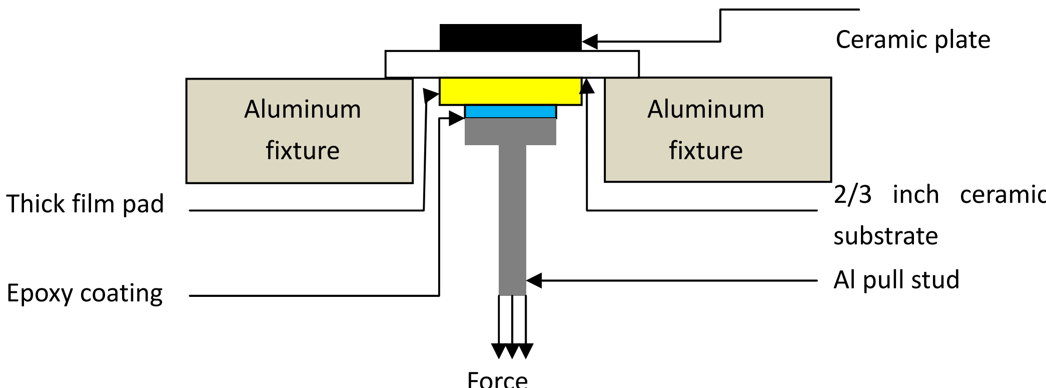


Figure 2.4 Illustration of Pull Test

In the initial test, conductor C101 with dielectric D1 was investigated (fired at 850°C). The initial failure was all in the epoxy for all four combinations. However, after 500 hours aging at 320°C, chunks of substrate were pulled off during the pull test, as shown in Figure 2.5. These failures were not expected since 320°C aging should not affect the strength of the ceramic substrate. To better evaluate the thick film adhesion, DuraStrate Thick-Film Substrates from CoorsTEK were selected for future adhesion tests. The fine-grained DuraStrate offers a 20% increase in strength and superior reliability over traditional Al_2O_3 [29]. Figure 2.6 are the SEM photos showing the difference of the DuraStrate Substrate in comparison with standard Al_2O_3.

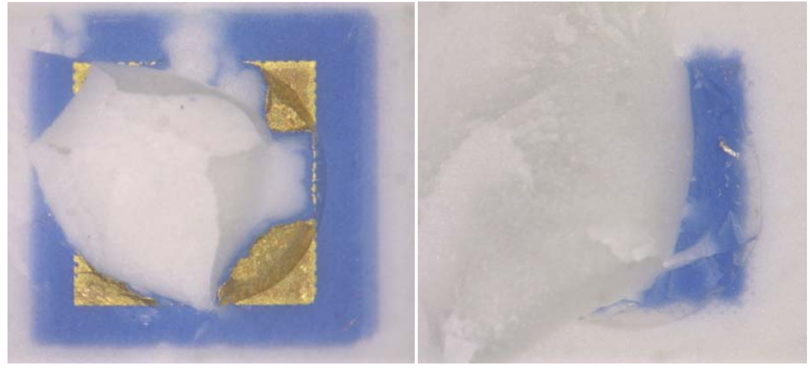


Figure 2.5 Ceramic Surface after Pull Test

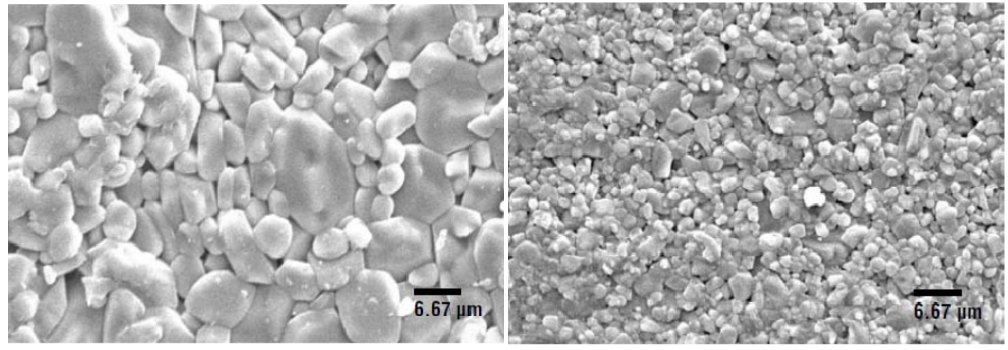


Figure 2.6 SEM Photos of DuraStrate Substrate
in Comparison with Standard Al_2O_3 [29]

For metal on ceramic, our initial pull test on 500 hours aged sample have low pull strength, with the failure still in the epoxy. A dark layer was observed on the metal surface, as shown in Figure 2.7. To identify the dark layer, Auger test is done on 0 hour and 500 hours sample. Five minutes of Ar sputtering was used, which corresponds to about 150 Å of the surface removed. Carbon was found on the aged sample, which explains the lower pull strength. Cu was also observed, likely from the copper oxide used in the reactive binding system. The results are shown in Figure 2.8. The pull test was repeated for metal on ceramic after cleaning the metal surface with carbon eraser.

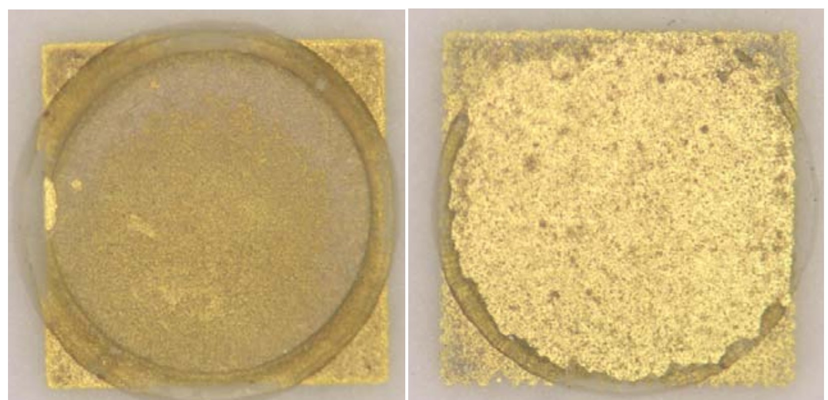


Figure 2.7 Metal Surface after 500 hours Aging at 320°C

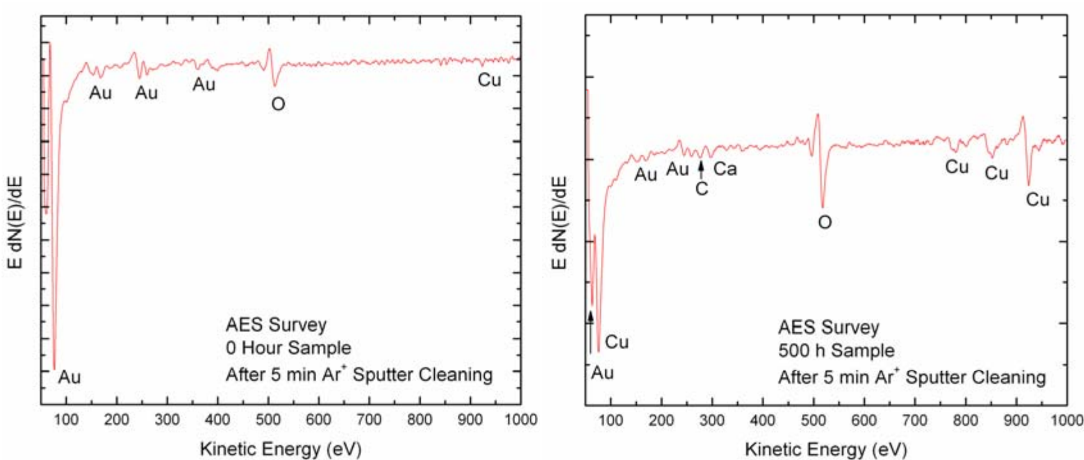


Figure 2.8 Auger Analysis on Samples as Build and after 500 hours Aging at 320°C

The investigation was continued with conductor C101 and dielectric D1 (fired at 850°C). The results are shown in Figure 2.9. All initial failures were in the epoxy layer. There was a significant drop in pull strength for conductor C101 on dielectric D1 after 1000 hours at 320°C and the failure mode shifted to metal-to-dielectric failure. There were also smaller decreases in pull strength for C101 on ceramic and D1 on C101 after aging.

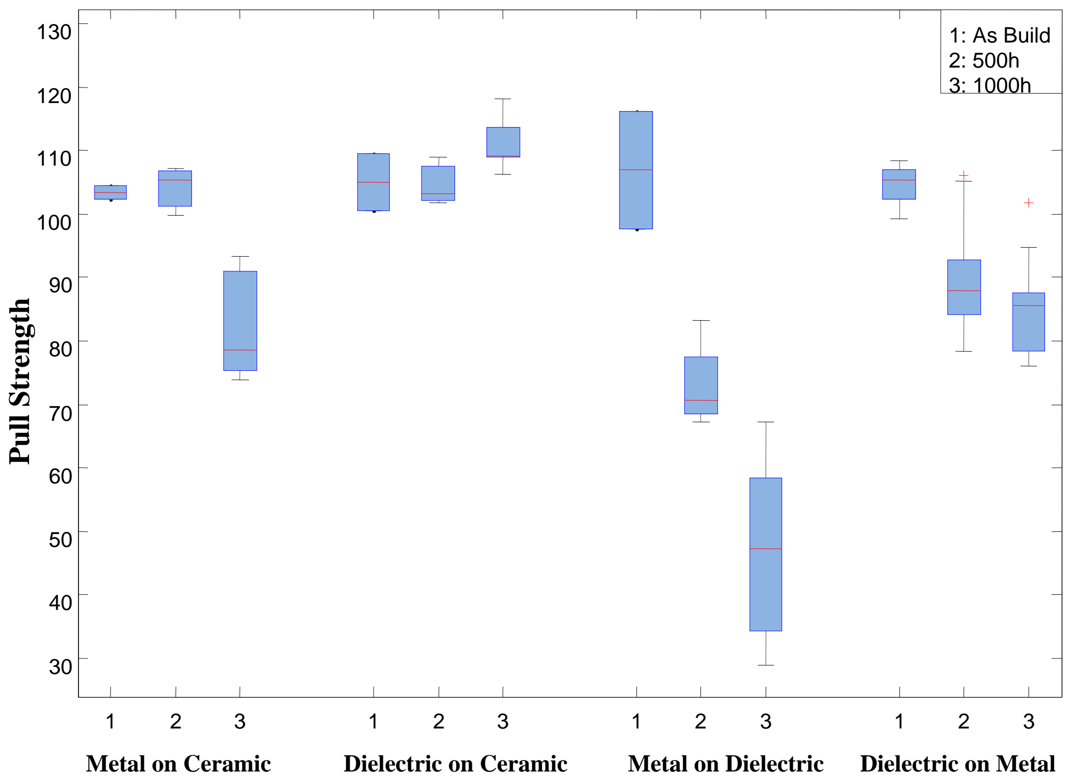


Figure 2.9 Pull Strength as a Function of Aging (320°C) for Conductor C101 and Dielectric D1 Fired at 850°C

Alternate processing of C101 and D1 was then evaluated. Two layers of D1 dielectric were printed and fired (the standard process), then a third layer of D1 was printed and dried, but not fired. The layer of C101 conductor was printed over the dried D1 and the two layers were co-fired. The adhesion was good after 500 hours aging, but after 1000 hours the metal adhesion degraded significantly. The test results are presented in Figure 2.10.

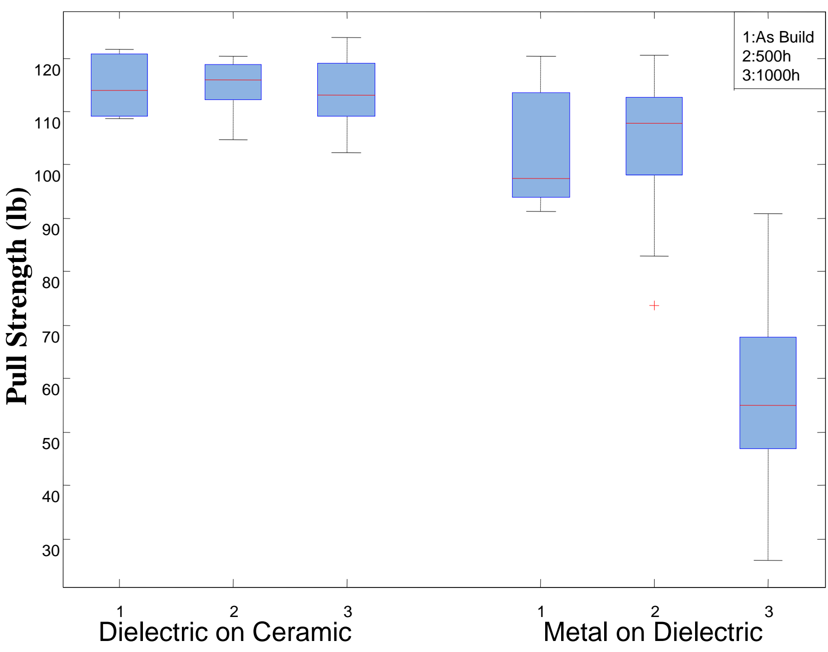


Figure 2.10 Pull Strength as a Function of Aging (320°C) for Conductor C101 and Dielectric D1 with Co-fire Process

Conductor C101 is a mixed bonded (both glass and reactive bonding) conductor ink. At 850°C, only the glass contributes to the bonding process. A higher firing temperature is required for the reactive bonding to occur. Thus a firing profile with a 980°C peak temperature was evaluated with conductor C101. The pull test results as a function of aging at 320°C are plotted in Figure 2.11. There was no degradation after 1000 hours at 320°C – all failures were in the epoxy layer. After 1500 hours, there were some samples with very small areas of dielectric that pulled off from the metal during pull testing, but the pull strength remained high. After 2000 hours the pull strength remained high. Again, there were some samples with very small areas of dielectric that pulled off from the metal during pull testing. In addition, a few samples exhibited a small amount of metal pulling off from the dielectric during pull testing. The results indicate that firing C101 and D1 at 980°C is the preferred profile for high temperature application.

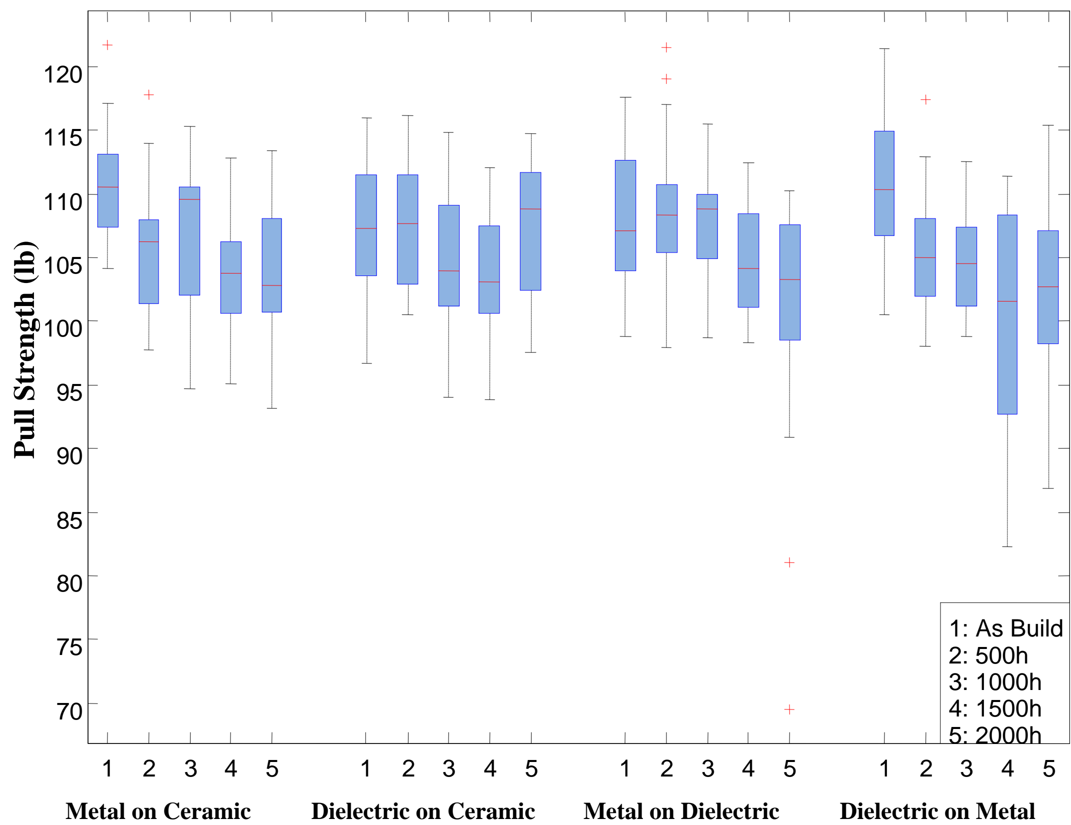


Figure 2.11 Pull Strength as a Function of Aging (320°C) for Conductor C101 and Dielectric D1 Fired at 980°C

Conductor C105 with dielectric D1 was also evaluated (fired at 850°C). The pull test results as a function of aging at 320°C are plotted in Figure 2.12. The initial pull test failures were all within the epoxy used to adhere the aluminum pull stud to the test pad. After 500 hours aging, all the metal has been pulled off from the ceramic and from the dielectric with low strength. The dielectric on ceramic showed no degradation after 1500 hour aging, confirming the dielectric results from the previous test with C101. However, low pull strength of the dielectric on metal after 500 hour aging was observed, with all the dielectric D1 pulling off from the C105 metal.

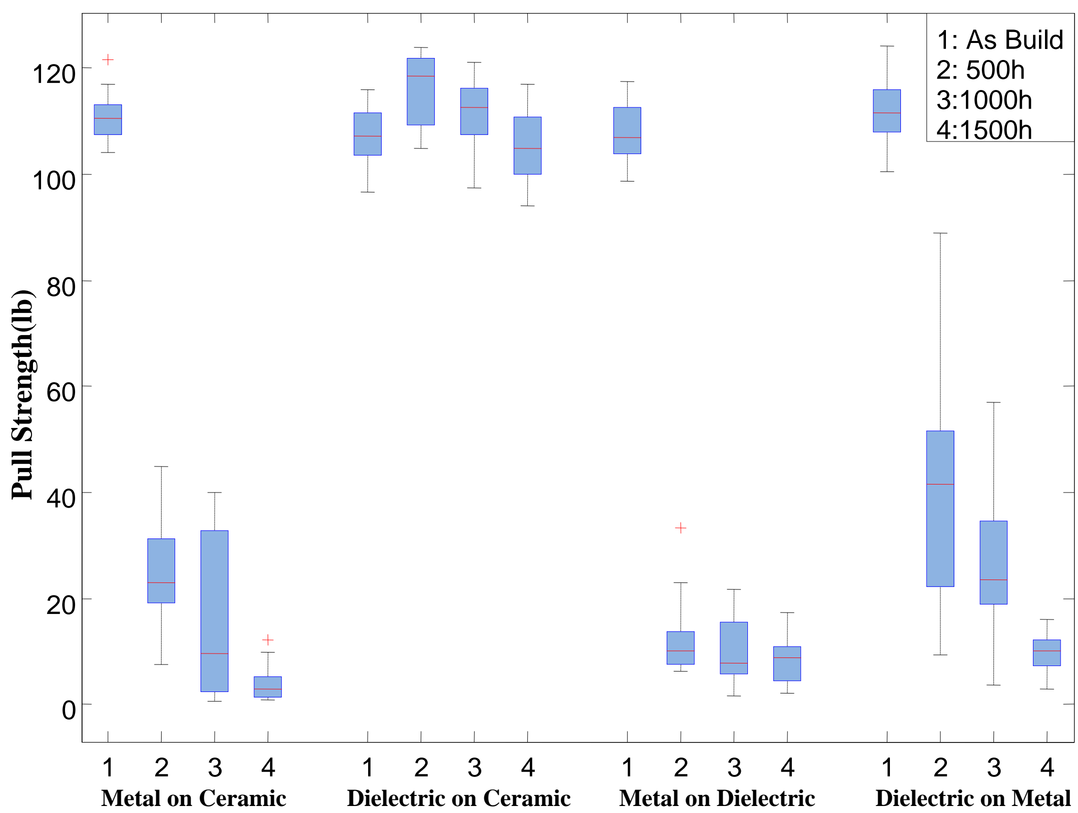


Figure 2.12 Pull Strength as a Function of Aging (320°C) for Conductor C105 and Dielectric D1 fired at 850°C

While improving adhesion with different process parameters, new materials were also evaluated. Au conductor C110 and dielectric D4 were tested with standard processes. C110 was printed on ceramic, on new dielectric D4, and on previously tested dielectric D1. New dielectric D4 was also tested with conductor C101 printed on it. The test results are shown in Figure 2.13. The initial pull test failures were all within the epoxy. After 500 hour aging, both C110 and C111 on dielectric D4 show degradation. The conductor C110 on ceramic did not degrade after 2000 hours aging and C110 on dielectric D1 also shows good adhesion after 2000 hour aging.

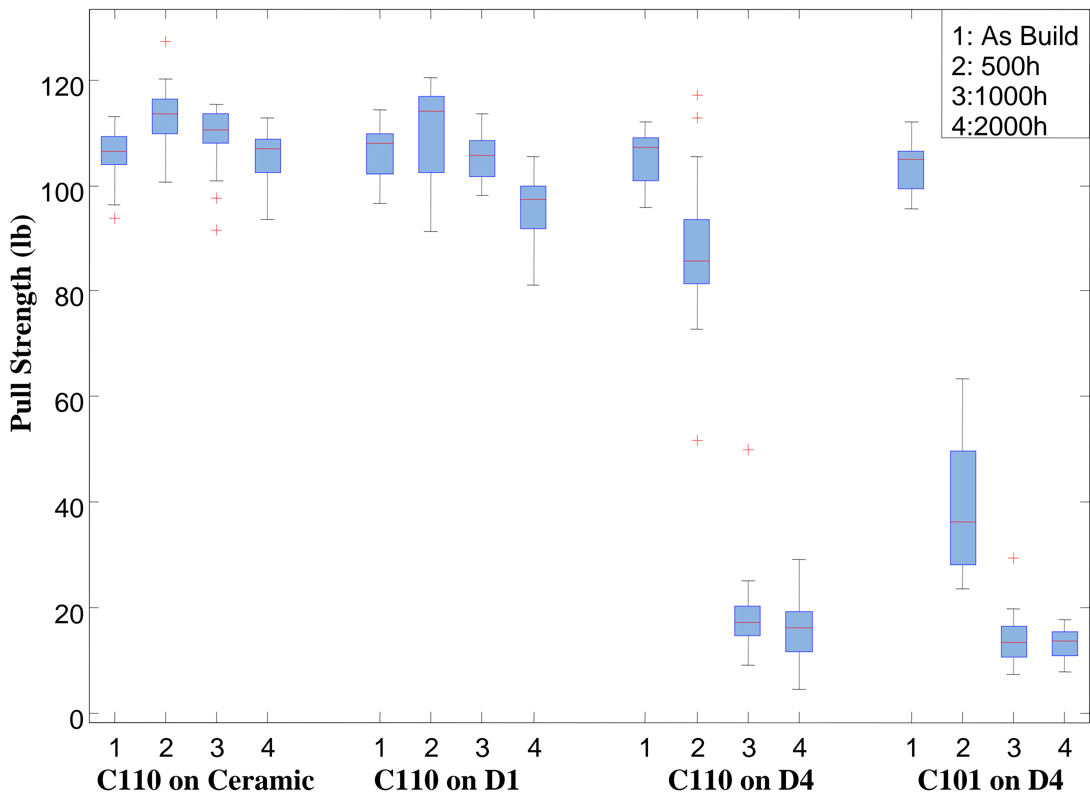


Figure 2.13 Pull Strength as a Function of Aging (320°C) for Conductor C110, C101 and Dielectric D1, D4 fired at 850°C

C109 Au/Pt/Pd conductor was tested with standard processes on ceramic and on dielectric D1. The test results are shown in Figure 2.14. The results show an improved adhesion after aging, with all failure in the epoxy after 2000 hours aging. Initially nearly half the samples had a small area of metal and dielectric pulled off. After 1000 hours aging, the failures were all within the epoxy. This failure mode remained the same after 2000 hours aging. This indicates that if fired at a higher temperature, the initial adhesion might be improved and all the failure would be in the epoxy.

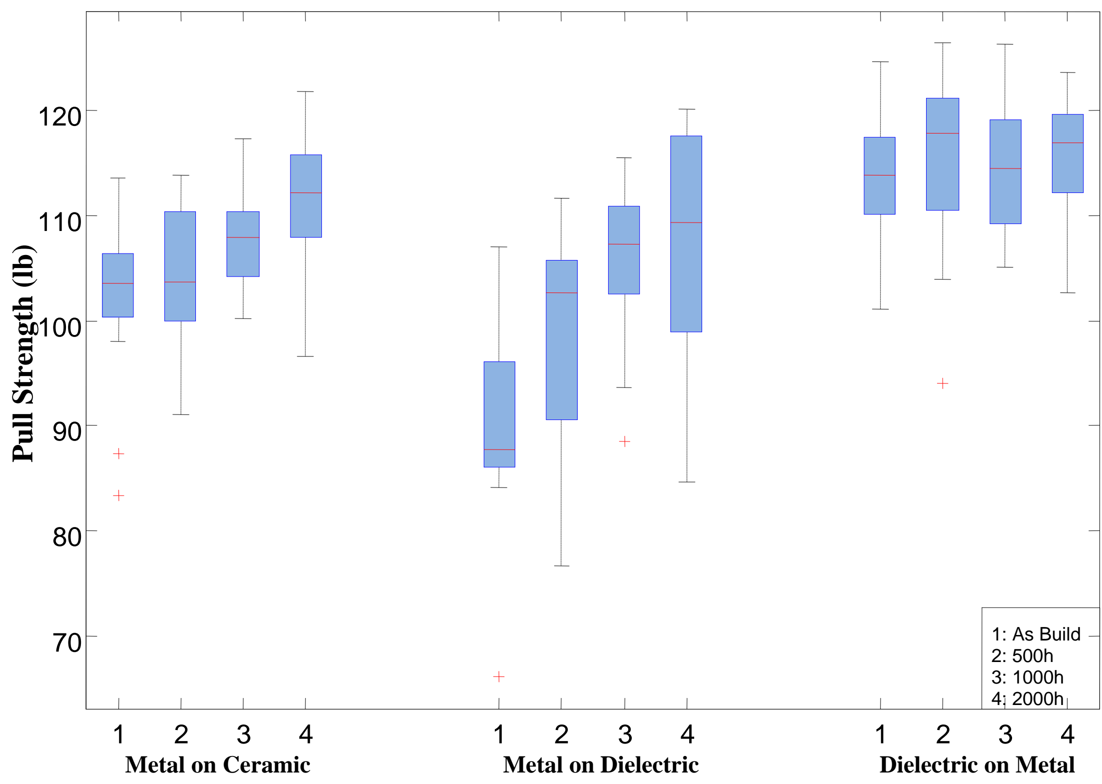


Figure 2.14 Pull Strength as a Function of Aging (320°C) for Conductor C109 and Dielectric D1 fired at 850°C

Conductor C109 on ceramic and on dielectric D1 with a firing profile with a 980°C peak temperature was evaluated. Also a group of samples were fired twice with the original 850°C profile. The test results are shown in Figure 2.15 (on ceramic) and Figure 2.16 (on dielectric D1). The second firing at 850°C does not improve the adhesion for C109 on ceramic or on dielectric D1. For conductor C109 fired with a 980°C peak temperature, although the initial pull strength was increased on both ceramic and dielectric D1, there were large areas of metal and dielectric pulled off during the pull test, as shown in Figure 2.17. A closer examination of the failure surface indicates that it was not just the metal that pulled off, but also ceramic and dielectric were found on the pulled conductor C109. It is suspected that a firing profile with 980°C peak temperature may cause excessive Pt diffusion into the ceramic and dielectric, which caused the above

failure. Since the detailed conductor composition remain proprietary, the exact reason is not clear.

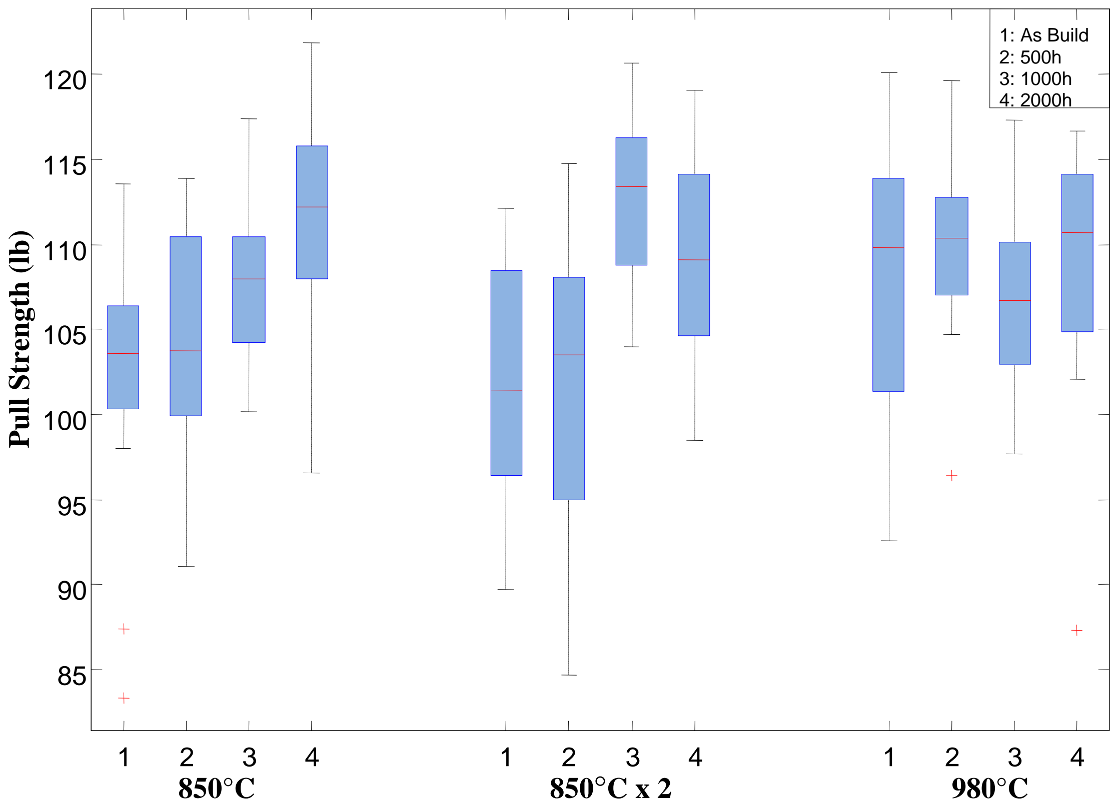


Figure 2.15 Pull Strength as a Function of Aging (320°C) for Conductor C109 on Ceramic fired at Different Conditions

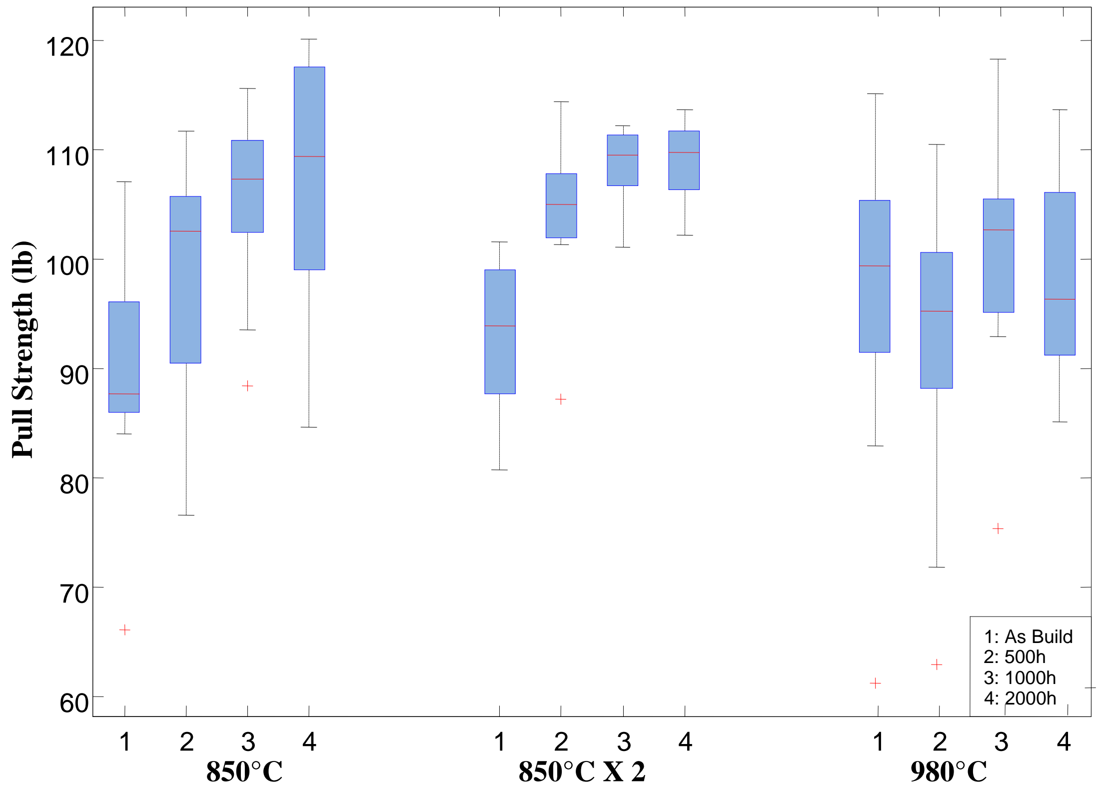


Figure 2.16 Pull Strength as a Function of Aging (320°C) for Conductor C109 on Dielectric D1 fired at Different Conditions

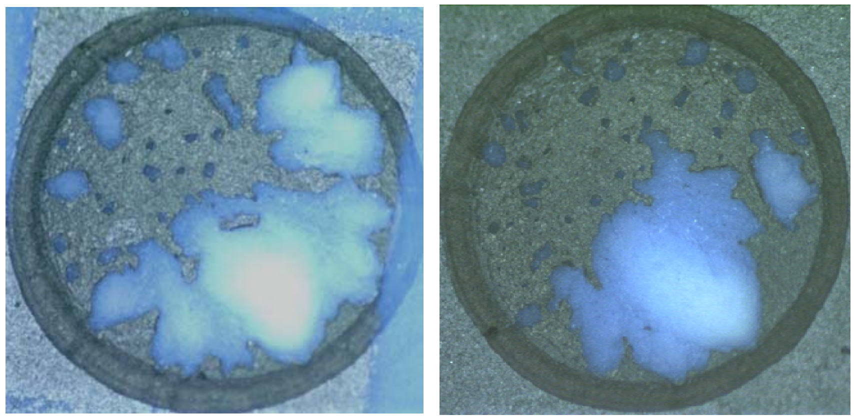


Figure 2.17 Conductor C109 Pulled off from Ceramic and Dielectric D1 fired at 980°C

From the adhesion perspective, the combination of C101/D1 fired at 980°C, C110/D1 fired at 850°C show satisfactory adhesion and should be used as our metal and dielectric for the multilayer thick film metallization. However, after the study of die attach, it was found that the Au based conductor C101 is not compatible with the die attach material

selected for high temperature application (details will be given in Chapter 3).

The combination of conductor C109 and dielectric D1 fired at 850°C provided satisfactory adhesion after 2000 hours aging at 320°C. Thus, C101 with C109 was selected for use on the die attach pads and the passive components attach pads. Since conductor C101 had good wire bonding results and lower resistivity than C109, it was used for wire bonding pads and interconnections.

2.5 Electrical Testing

The electrical properties and reliability of the dielectric at 300°C is important for circuit design and performance. To characterize dielectric properties of the thick film materials, an electrical test vehicle was designed and fabricated on 2” by 2” alumina substrates. Gold conductor C101 and dielectric D1 were evaluated. A bottom conductor layer, two dielectric layers, and a top conductor layer were printed, dried, and fired separately. Initial test vehicles were fired at 850°C. Based on the adhesion test results, subsequent test vehicles were fired at 980°C.

This three-layer test vehicle provided electrical test structures for leakage current, capacitance, dissipation factor, and a metal electromigration tests. The test pattern is shown in Figure 2.18. On the test vehicle there are 7 capacitors, 6 comb patterns, and 3 migration test lines. These structures are labeled in Figure 2.18 and their properties are summarized in Table 2.3. The metal migration patterns were 1730 mils long, but were not evaluated in this test as the anticipated application current levels were low and metal electromigration was not anticipated.

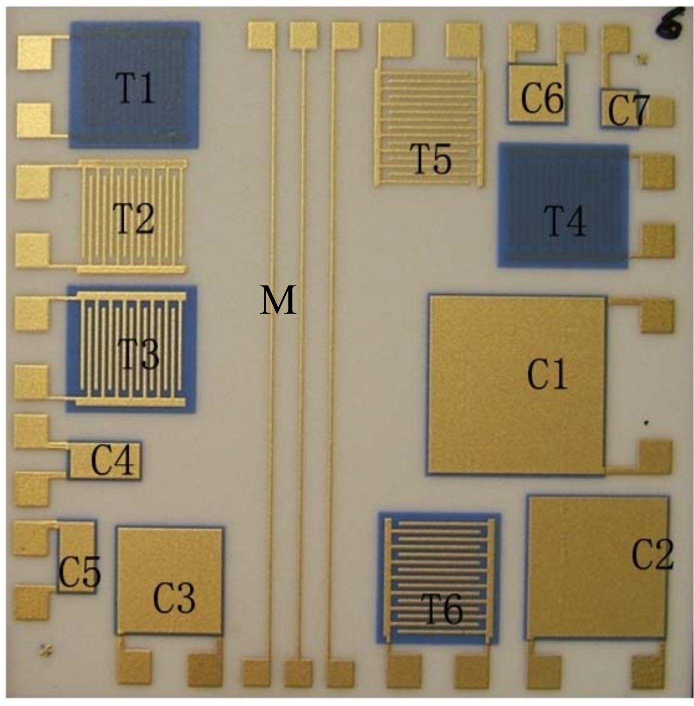


Figure 2.18 Electrical Test Vehicle

Table 2.3 Test Pattern for Electrical Test Vehicle

Capacitor	size (mil)	Comb Pattern (line width 10mil)	
C1	500 by 500	T1	10mil space; under dielectric
C2	400 by 400	T2	10mil space; no dielectric
C3	300 by 300	T3	10mil space; on dielectric
C4	100 by 200	T4	12mil space; under dielectric
C5	200 by 100	T5	12mil space; no dielectric
C6	160 by 160	T6	12mil space; on dielectric
C7	100 by 100		

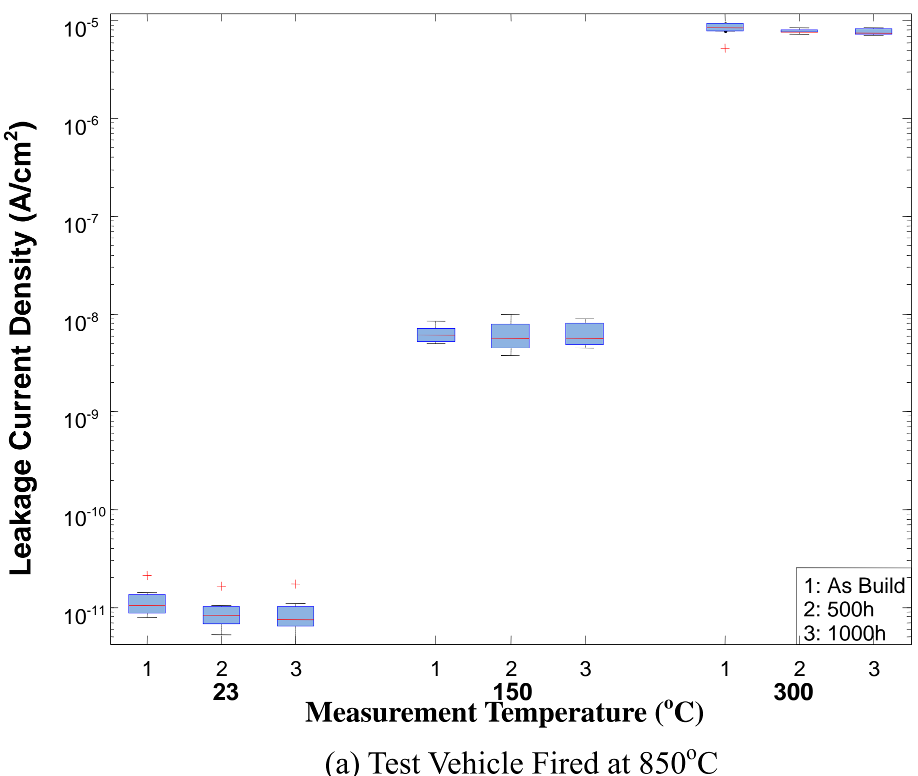
2.5.1 Leak Current Measurement

Leakage currents were measured on the various sized capacitors and comb patterns with a bias voltage up to 100V at different temperatures. An HP 4145 Semiconductor Parameter Analyzer was used. The measurement current includes two components: the transient capacitor charging current, and the steady state leakage current. The voltage was increased from 0V to 100V, in 5V steps. To reduce the error due to the charging current,

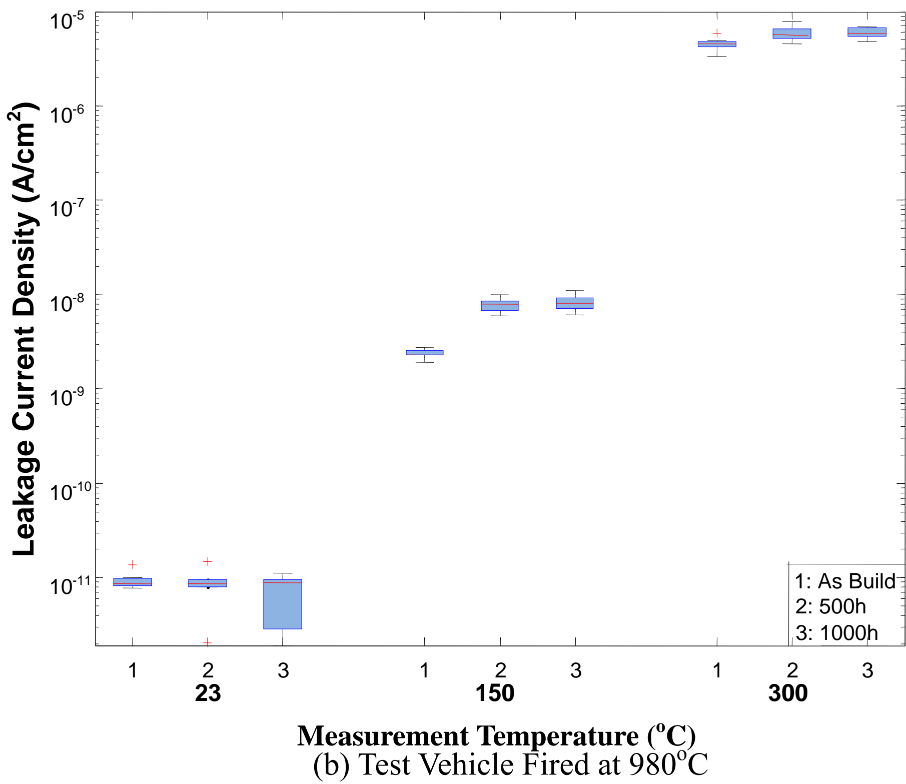
the leakage current was measured at each step after the voltage had been applied for 20 seconds.

Aging data up to 1000 hours has been collected for test vehicles fired with a peak temperature of 850°C and test vehicles fired with a peak temperature of 980°C. Figure 2.19 plots the results of 100V bias capacitor leakage current density (leakage current/capacitor area) measurements initially and after 500 and 1000 hours of unbiased aging at 320°C. No significant change was found with aging.

Figure 2.20 plots capacitor leakage current density as a function of temperature measured at 100V bias with test vehicles fired at a peak of 980°C, with samples as-built (a) and after 1000 hours aging (b). No significant change was found with aging, and compared with Figure 2.19, firing at 980°C does not change the electrical properties.

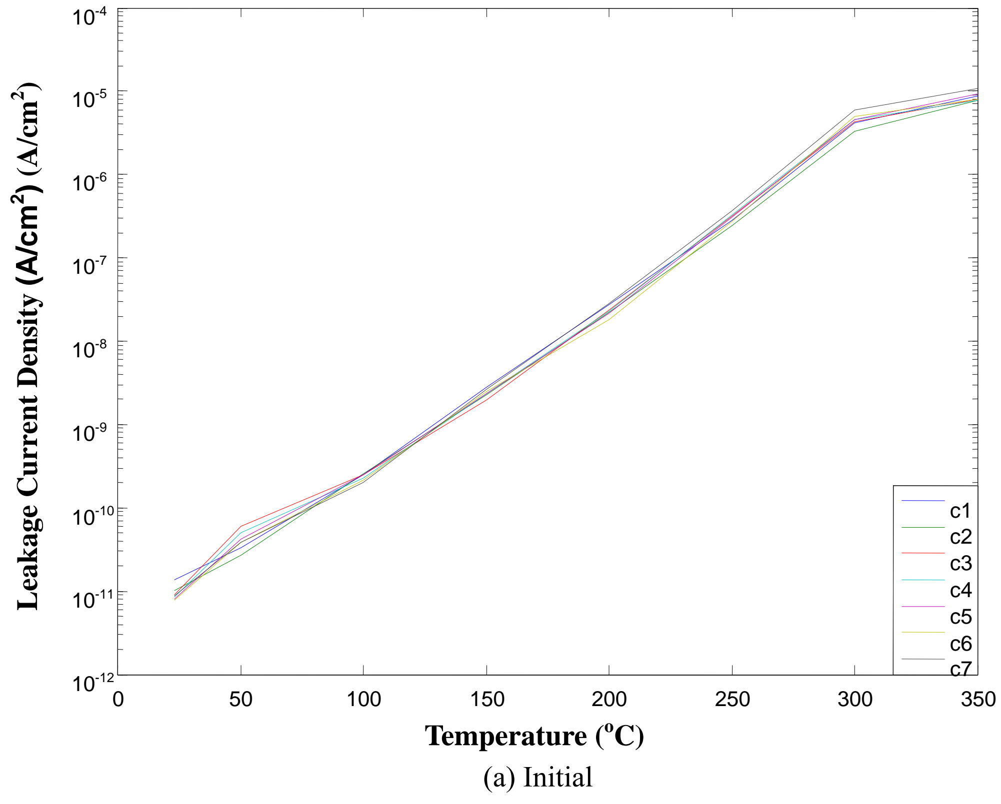


(a) Test Vehicle Fired at 850°C

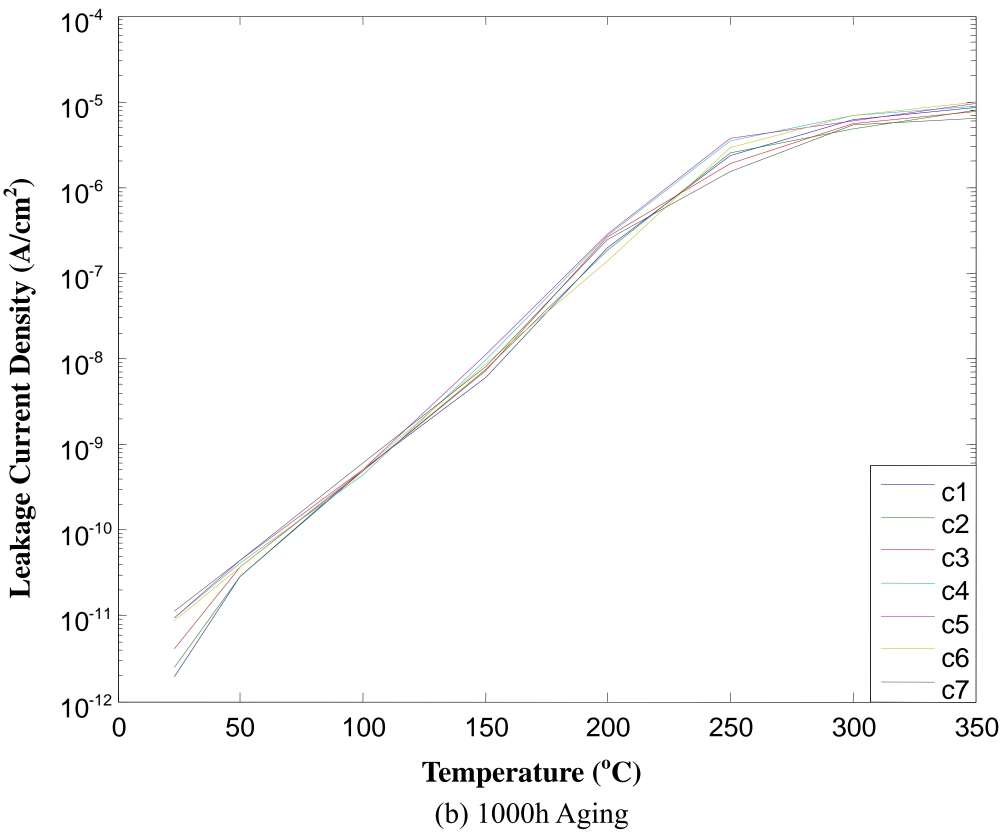


(b) Test Vehicle Fired at 980°C

Figure 2.19 Capacitor Leakage Current Density at 100V Bias as a Function of Storage Time at 320°C (a) Test Vehicle Fired at 850°C (b) Test Vehicle Fired at 980°C



(a) Initial



(b) 1000h Aging

Figure 2.20 Capacitor Leakage Current Density at 100V Bias as a Function of Temperature (Test Vehicle Fired at 980°C)

The comb pattern was designed to have 8 lines on one comb and 7 lines on the other. Each line was 10mil wide, with a 10 mil space for T1, T2, and T3, and 12 mil space for T4, T5, and T6. Each line had a length of 250 mil, with 225 mil overlapped to the next line, as shown in Figure 2.21. Each comb pattern had 225x14 = 3150 mil of overlapped length. For comb pattern T2 and T5, lines were printed onto the ceramic; for pattern T1 and T4, a dielectric layer was printed on top of the lines; for comb pattern T3 and T6, lines were printed on top of a dielectric layer. Table 2.1 shows the measured line width and spacing compared to the designed value, which indicates that after firing the conductor shrank on ceramic and expanded on dielectric.

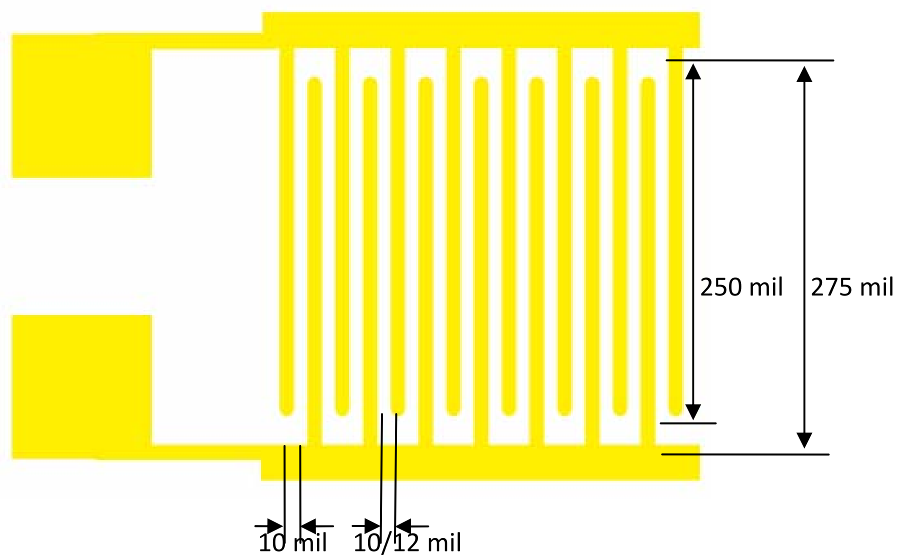
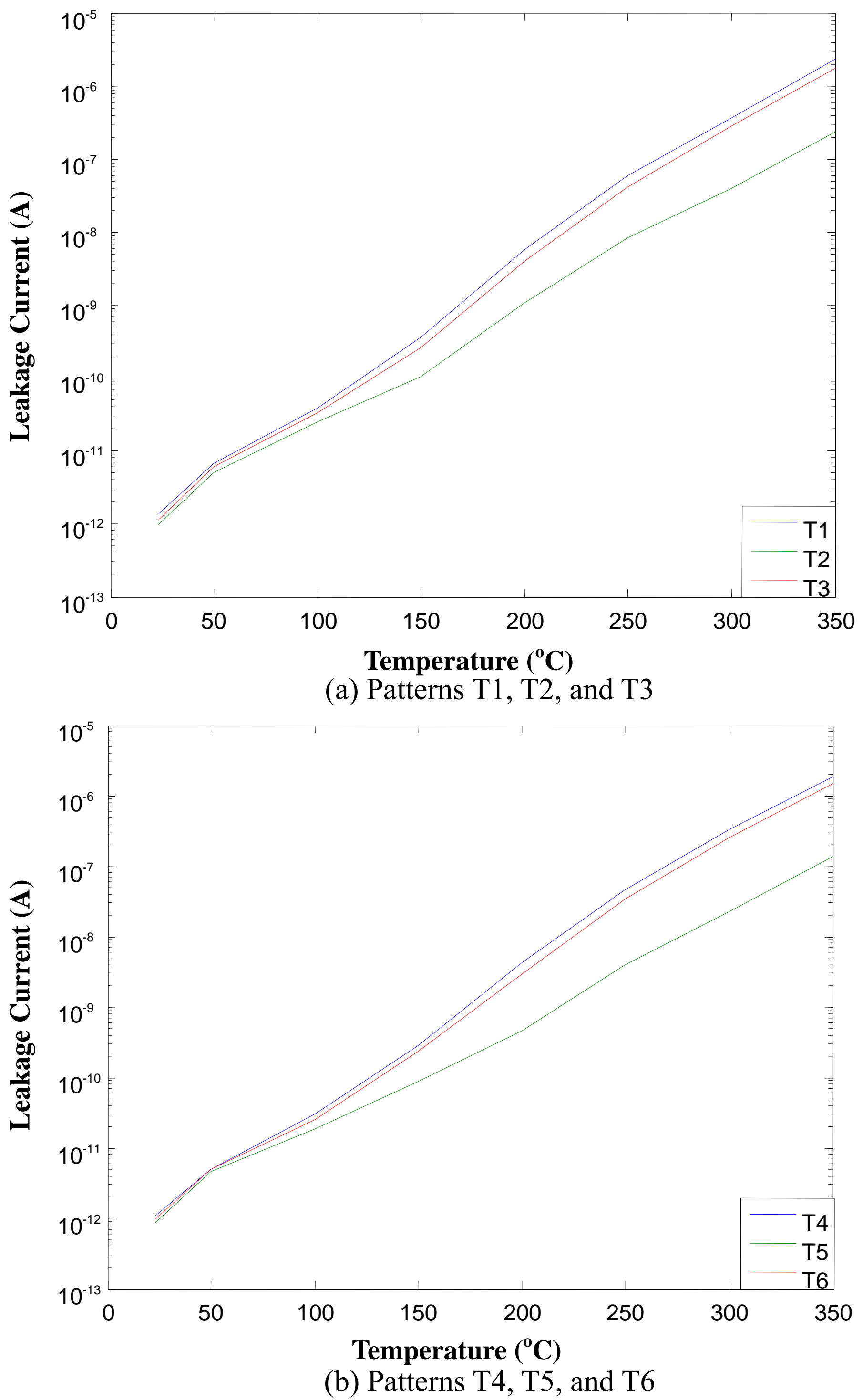


Figure 2.21 Designed Comb Test Pattern

Table 2.4 Measured Line Width and Spacing on Comb Pattern

Designed Line/Spacing (mil)	Measured Line/Spacing (mil)	
	On Ceramic	On Dielectric
10/12	9.70/12.6	10.65/11.2
10/10	9.65/10.7	10.15/9.8

Figure 2.22 plots the initial result of the leakage current measurements at 100V bias. The results are the average of seven test vehicles fired with a peak temperature of 980°C. The results indicate that comb patterns printed in contact with the dielectric D1 had slightly higher leakage currents at elevated temperatures.



(a) Patterns T1, T2, and T3

(b) Patterns T4, T5, and T6

Figure 2.22 Initial Leakage Current at 100V Bias as a Function of Temperature (Test Vehicle Fired at 980°C)

The comb pattern leakage current has also been measured on samples fired with a peak temperature of 850°C. The results were similar to the samples fired with peak

temperature of 980°C. There was no change in leakage current for both the 850°C fired and 980°C fired samples after 1000 hours unbiased aging at 320°C.

2.5.2 Dissipation Factor and Capacitance Measurement

For capacitance and dissipation factor measurements, a test fixture was designed to hold the sample and provide stable contact to the coax cable, as shown in Figure 2.23. Four 1-meter (electrical length) coax cables were connected to the capacitor through a glass ceramic (Macor). A contact screw was fixed on each cable to prevent twisting. Another screw was used to provide pressure on the spring (inconel) through an insulator ball (silicon nitride). The sample was held on an aluminum substrate and the substrate was attached to the glass ceramic by screws (not shown in the illustration). Due to the design complexity and space limitation, only capacitor C1 (500 mil by 500 mil) was measured.

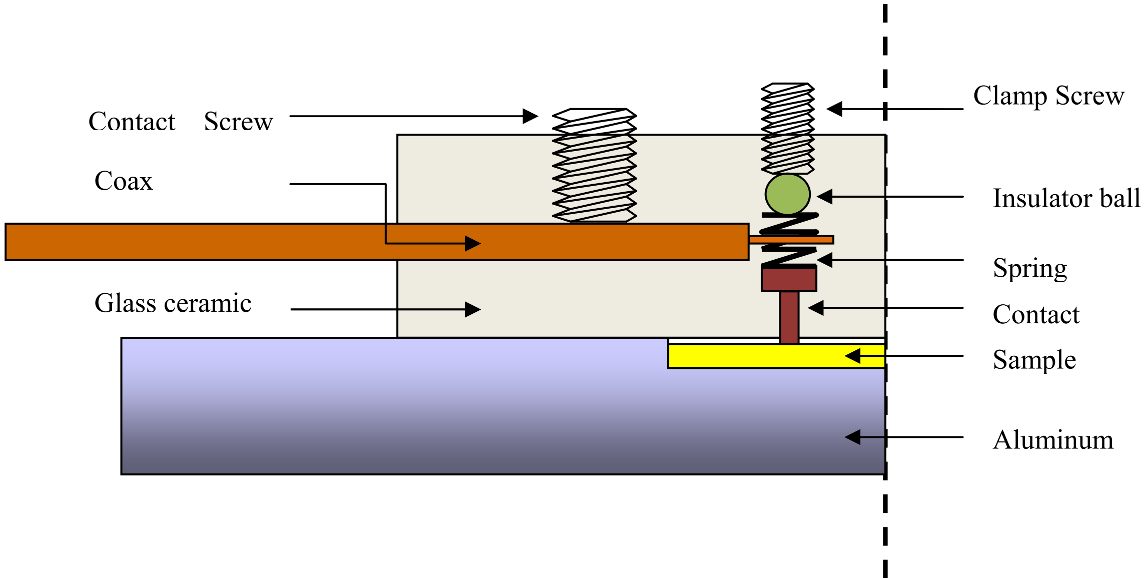


Figure 2.23 Test Fixture for Capacitance and Dissipation Factor Measurement

The fixture was placed inside a Delta Design 9023 oven. Dissipation factor and capacitance were measured with an Agilent 4192A LF Impedance Analyzer as the

temperature was stepped from room temperature to 350°C. The initial results for 980°C fired test vehicles are shown in Figures 2.24 and 2.25, which is the average value from six test vehicles. The capacitance and dissipation factor has also been measured on test vehicles fired with peak temperature of 850°C. The results were similar to the samples fired with peak temperature of 980°C. There was no significant change in capacitance or dissipation factor for both the 850°C fired and 980°C fired samples after 1000 hours unbiased aging at 320°C.

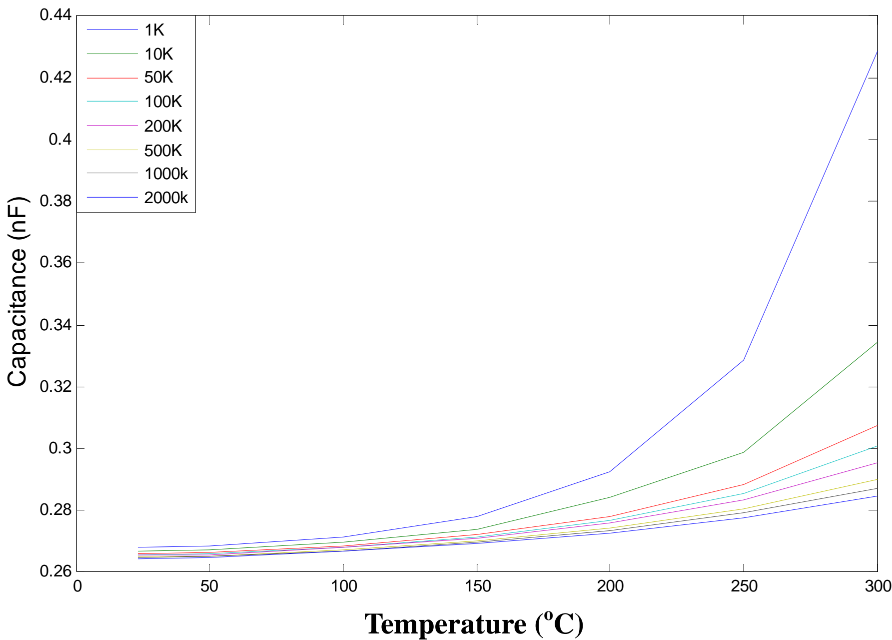
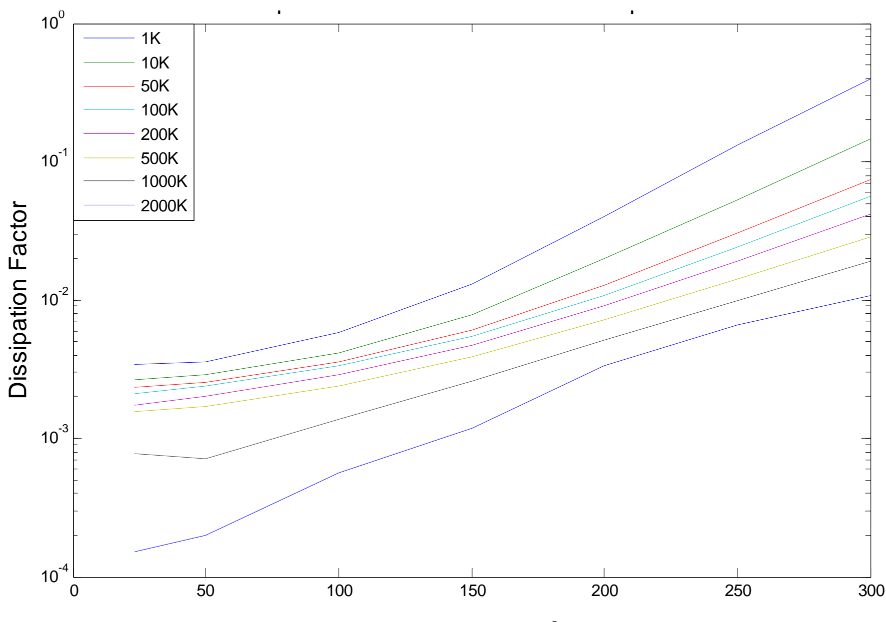


Figure 2.24 Initial Capacitance as a Function of Frequency and Temperature (Test Vehicle Fired at 980°C)



Temperature (°C)

Figure 2.25 Initial Dissipation Factor as a Function of Frequency and Temperature (Test Vehicle Fired at 980°C)

2.5.3 Biased Measurement

To further investigate the dielectric properties after high temperature storage, the leakage current test was repeated with a modified test pattern, and aging test was conducted under 100V DC and 60V DC bias voltage. Two capacitors (400mil square) and one comb pattern (10mil line/space) under dielectric were fabricated on 2" by 2" alumina substrates, as shown in Figure 2.26.

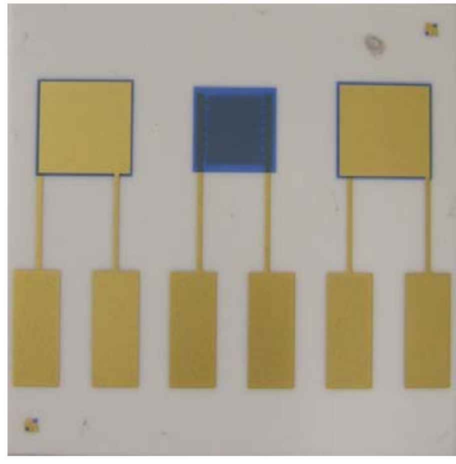


Figure 2.26 Test Pattern for Leakage Current under Bias

Au conductor C101, Au/Pt/Pd conductor C109, and dielectric D1 were evaluated. A bottom conductor layer, two dielectric layers, and a top conductor layer were printed, dried, and fired separately. The bottom and top conductor layer used the same conductor paste, either Au or Au/Pt/Pd. The test vehicles includes four groups: Au conductor under 100V bias voltage, Au conductor under 60V bias voltage, Au/Pt/Pd conductor under 100V bias voltage, and Au/Pt/Pd conductor under 60V bias voltage. Each group has eight substrates, which include 16 capacitor patterns and 8 comb patterns.

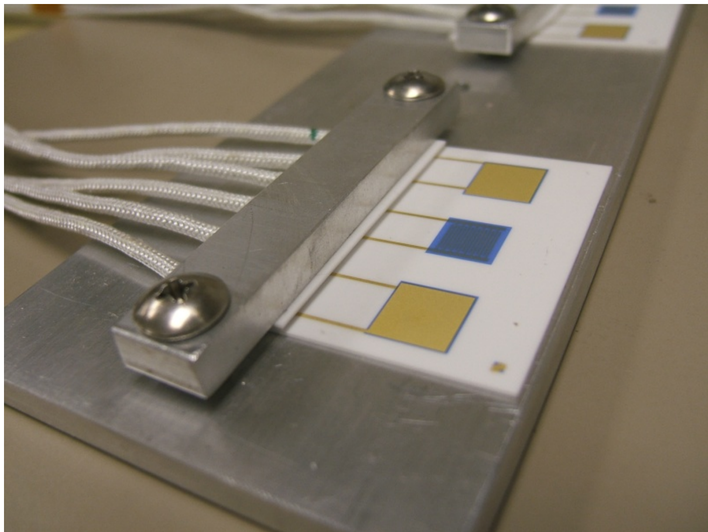


Figure 2.27 Wires Held on Test Vehicle

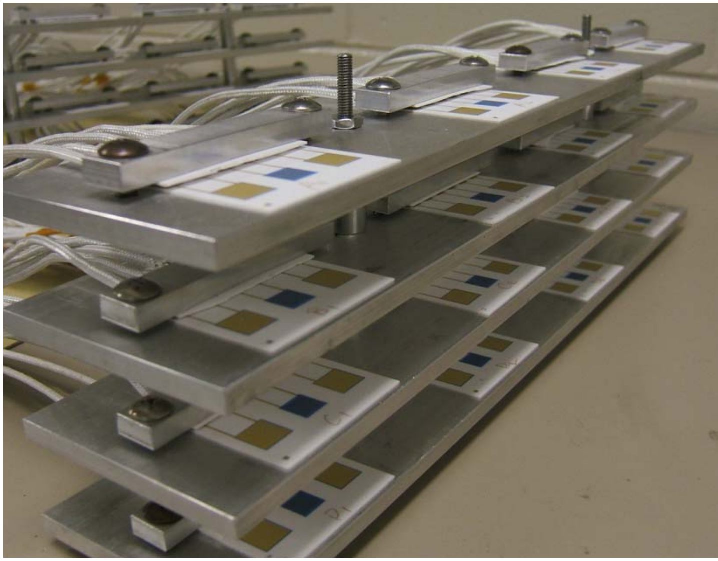


Figure 2.28 Stacked Test Fixtures

To measure leakage current with bias voltage on multiple test patterns, a 100kΩ resistor was connected in series with each test pattern. Leakage current was calculated from the voltage measurement across this resistor. High temperature wires were held by crimps and pushed into tight contact with the test pattern by an aluminum bar, as shown in Figure 2.27. A ceramic substrate was used between the aluminum bar and the wires to prevent electrical shorting. Four substrates were placed on a large aluminum fixture, and four of these fixtures were stacked together, as shown in Figure 2.28. The wires were connected to the resistors and power supplies on a breadboard outside the aging oven.

The test vehicles were placed in a 300°C oven, with 100V and 60V power supplied continuously. Leakage current was calculated from voltage measurements initially, after 100, 200, 500, and 1000 hours aging. The results were plotted in Figure 2.29.

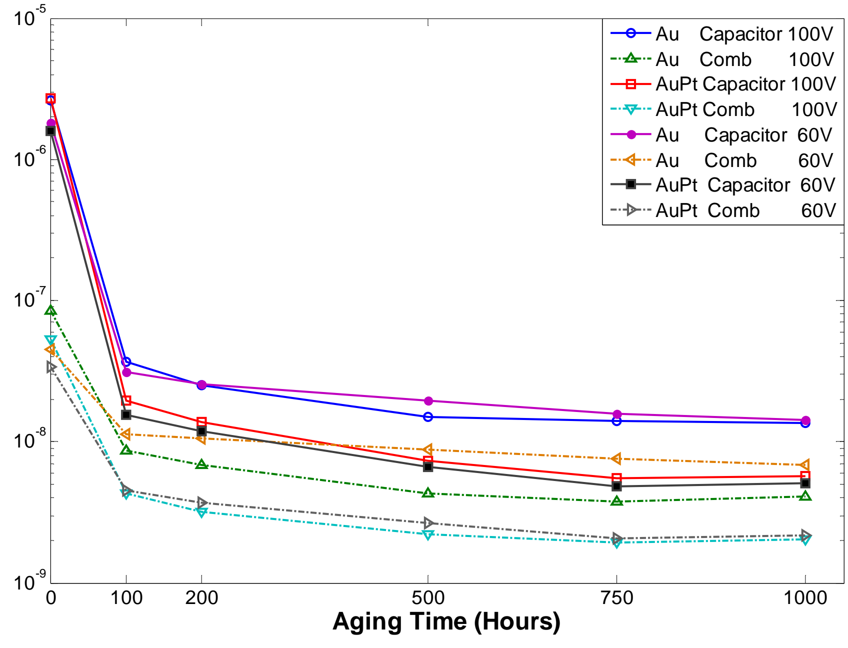


Figure 2.29 Leakage Current as a Function of Aging Time

After 100 hours aging at 300°C, the leakage current exhibited a significant decrease on all the test patterns, and a slow decrease continued through 750 hours. Test vehicles

were removed from the oven after 1000 hours aging at 300°C. On the comb pattern from all four groups, discoloration of the ground connected comb fingers was observed, as shown in Figure 2.30. There was no difference with bias voltage (100V/60V). Samples will be cross-sectioned for SEM/EDS analysis. The similar discoloration was found on the corner of the capacitor, as shown in Figure 2.31.

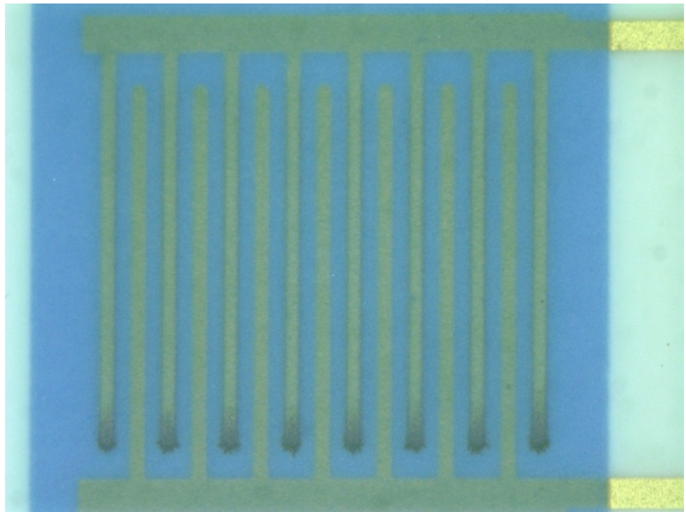


Figure 2.30 Comb Pattern after 1000 hours Biased Aging

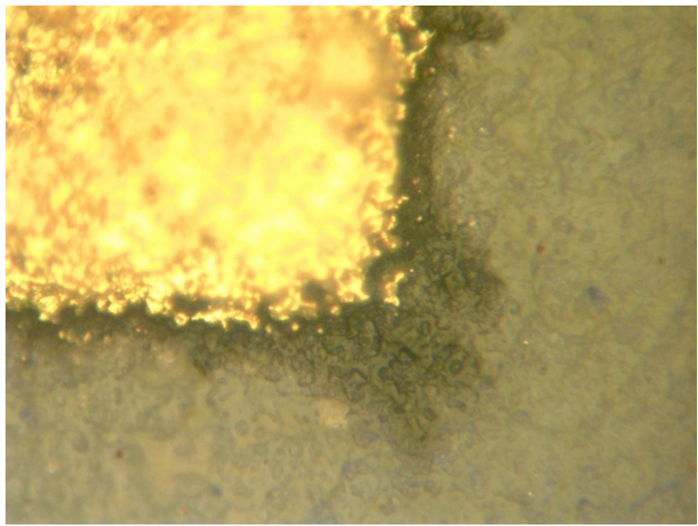


Figure 2.31 Corner of Capacitor after 1000 hours Biased Aging

The significant leakage current decreasing was not expected. To understand the mechanism, two aged samples (with 100V bias voltage) and two unaged samples were

wired onto the same test fixture. Since the thick film metal conductor did not show a large difference from Figure 2.29, the samples fabricated with Au conductor C101 were tested. 100V DC bias voltage was applied to the samples after the oven had reached 300°C for 20 minutes. The leakage current was then measured immediately. The initial leakage current from the unaged sample was higher than we measured in the initial test. This was because in the previous test, the initial leakage current was measured after applying bias voltage for some time, which is not an accurate initial value. The test result shows that 1000h bias aged samples have a relatively constant leakage current during the 300 minutes test time, while the unaged samples show a rapid decreasing leakage current, as shown in Figure 2.32. This test continued for 24 hours and no discoloration was found on the samples.

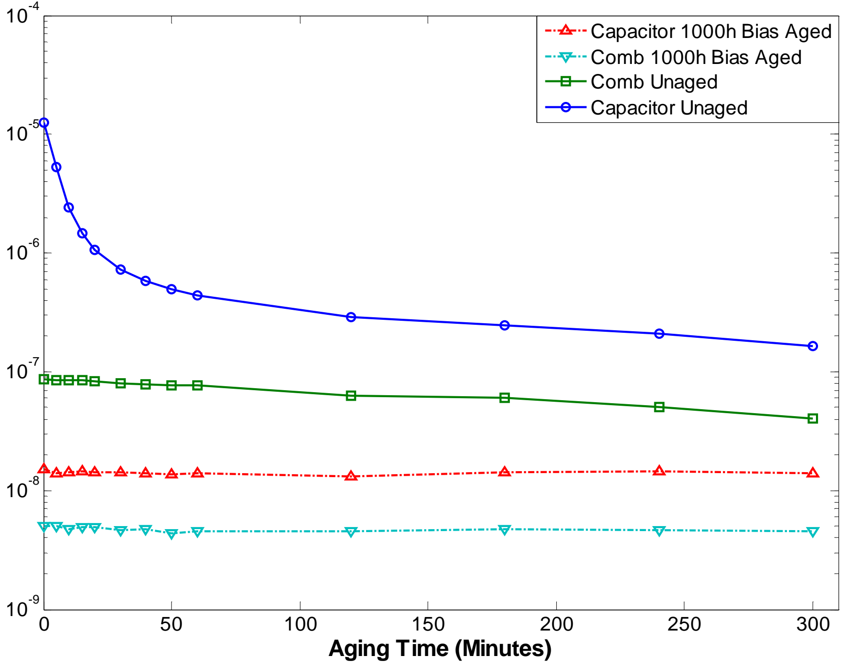


Figure 2.32 Leakage Current as a Function of Aging Time for 300 Minutes

2.6 Summary

Several conductor and dielectric inks were investigated for application at 300°C. For

some conductor and dielectric combination, the adhesion on ceramic and on each other can be improved with a higher firing temperature. The selected thick film combination shows excellent adhesion after 2000 hours aging at 320°C.

Dielectric D1 provides excellent insulation at 300°C. Its electrical performance is stable as a function of high temperature exposure and meets the requirements for this application. The increased firing temperature does not affect the performance. Dielectric D1 will be used to provide cross-over insulation between two conductive layers in our multilayer thick film hybrid circuit.

Decreasing leakage current was found in biased aging. The exact reason is unclear and need further investigation. Further analysis of the discoloration is also required.

CHAPTER 3 HIGH TEMPERATURE DIE ATTACH AND WIREBONDING OF SILICION CARBIDE DEVICES

3.1 Introduction

To realize SiC devices for high temperature applications, reliable packaging and interconnection technology must be developed. Die attachment of the SiC die to a metallized substrate or package is the first-level interconnection process and a fundamental element of any packaging approach. The selection of chip metallization, substrate metallization, and die attach material are critical to a successful package design that can survive high temperature excursions. This chapter examines eutectic AuSn as the die attach solder with two different thick film metallizations on Al_2O_3 substrates. Die shear tests were performed after aging at 320°C and after thermal cycling. The shear test results and failure analysis are discussed. Wirebonding was investigated for electrically connecting the I/O pads on the SiC die to the corresponding pads on the substrate. Small diameter (1 mil) gold wire was used for thermosonic wirebonding. Test vehicles were assembled for wire pull tests, ball shear tests and daisy chain electrical resistance measurement.

3.2 SiC Die Metallization

The temperature limit for devices is imposed by the die metallization rather than the semiconductor's inherent capability. Diffusion, intermetallic compound formation, and Kirkendall voiding will accelerate at elevated temperatures and interfaces are subject to

stress and strain due to differences in thermal expansion between the joined materials, which is aggravated by the wider thermal excursions in high temperature electronics and the general increase of CTE with temperature.[30]. A reliable metallization stack must be identified to work with the die attach material, substrate metallization, as well as the wirebonding.

Die backside metallization previously investigated at Auburn University include Cr/Cr-Ni/Au, Ti/$TaSi_2$/Pt [31], and Ti/TiW/Au [20][32]. Other metallization stacks for high temperature operation include Ti/TiN/Pt/Au [33], Ni/Cr/W [34], and Cr/Mo/W [35]. In this research, the SiC test die were fabricated by GE Global Research and had a backside metallization of 2kÅ Ni/NiSi2, 2kÅ TiW and 10μm Au. The SiC test die had no functional circuit but did contain a daisy chain metal pattern on the topside. The topside metallization for the pad and interconnection was: 1μm Au, 2kÅ Ti, 500Å NiSi, and 500Å Ni. For die shear testing the die were cut into 2.25mm x 2.25mm, while for the wire bond and thermal cycling tests the die were cut into 4.5mm x 4.5mm. Smaller die were used for the die shear test so the die shear strength would not exceed the 100kg maximum shear force limit of the Dage PC2400 die shear tester. Figure 3.1 shows the 4.5mm x 4.5mm die with the daisy chain pattern.

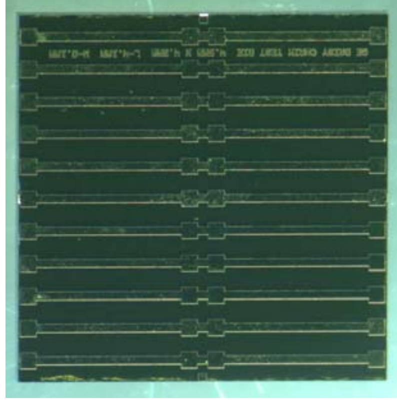


Figure 3.1 SiC Test Die with Daisy Chain Pattern

3.3 Off-eutectic AuSn Liquid Phase Transient (LPT) Die Attach

Attachment of the die to the substrate with epoxy adhesives followed by wirebonding is a commonly used method of bare die assembly for conventional temperature ranges. However, die attach epoxies are typically limited to a maximum continuous operation temperature of 150°C to 200°C [36]. For higher operating temperature ranges, a number of solder and braze die attach materials are available, as shown in Table 3.1. [30]

Table 3.1 High Temperature Solder and Braze Alloys [30]

Composition (wt. %)	Solidus (°C)	Liquidus (°C)
80Au/20Sn	278 (Eutectic)	
92.5Pb/5Sn/2.5Ag	280 (Eutectic)	
92Pb/5In/3Ag	300	310
90Pb/10Sn	275	302
97.5Pb/2.5Ag	303 (Eutectic)	
97.5Pb/1Sn/1.5Ag	309 (Eutectic)	
95Pb/5Sn	310	314
88Au/12Ge	356 (Eutectic)	
96.76Au/3.24Si	363 (Eutectic)	
82Au/18In	451	485
45Ag/38Au/17Ge	525 (Eutectic)	
50Ag/18Cd/16.5Zn/15.5Cu	625	635
72Ag/28Cu	780 (Eutectic)	
82Au/18Ni	980 (Eutectic)	

High-lead-content solders such as 95Pb/5Sn and 90Pb/10Sn are used for bare die attachment for applications to 200°C ~225°C. Au based alloys such as Au/Sn, Au/Ge, and Au/Si are used for higher temperature requirements [30].

Certain pairs of elements, determined by their crystalline structure, will undergo a eutectic transition at some specific composition and temperature (defined as the eutectic point on a phase diagram). A eutectic transition occurs at a critical temperature where two metals in proper proportions pass directly from solid to liquid (or vice-versa) phases

without passing through an intermediate solid plus liquid phase [37]. Common eutectic alloys for packaging applications include AuSn, AuGe, and AuSi. Eutectic AuGe has been successfully demonstrated with Si die and thick film Au metallization at Auburn University [38]. However, AuGe should not be used with Ni containing metallizations due to Ni-Ge intermetallic formation.

In this work, the off-eutectic AuSn transient liquid phase die attach process was used. This method has been previously demonstrated for SiC power devices on electrolytic Ni/Au plated direct bond copper substrates [20]. The resulting off-eutectic solder joint will have a melting point much higher than the eutectic point due to the interdiffusion of Au from die backside metallization and substrate metallization. This permits a high melting point solder joint to be created at a much lower processing temperature. Also the secondary reflow of passive components attachment can be performed at the same temperature without damaging the die attach solder joint.

3.3.1 Liquid Phase Transient Bonding

Liquid Phase Transient (LPT) bonding is a diffusional bonding process derived from high-temperature fluxless vacuum brazing [39]. An interlayer is placed between the two metallic surfaces to be bonded. Upon heating and maintaining the tri-layer at a sufficiently elevated temperature, the interlayer melts and then solidifies as a result of interdiffusion with the base material [40]. Liquid formation depends upon an eutectic reaction, either within the diffusion, or between the interlayer and the substrate metallizations. Diffusion of interlayer material into the substrate and/or vice-versa induces compositional changes that result in isothermal solidification at the bonding temperature. Upon cooling there remains no trace of the liquid phase, and ideally the joint

becomes indistinguishable from other grain boundaries. The major advantage of TLP bonding is that it is an isothermal process, the thermal stresses formed between the die and substrate are minimal [41]. When LPT bonding is possible, it generally produces joints of excellent strength and high reliability.

Eutectic alloy, AuSn (80 wt.% Au and 20 wt.% Sn) was evaluated for die attach using the liquid phase transient bonding process. The melting point of AuSn eutectic is 278°C, as the Au-Sn phase diagram shown in Figure 3.2 [42]. To increase the melting point of the alloy, Au must be dissolved into the joint from the backside of the SiC die and from the substrate metallization. This shifts the alloy composition to the left (Au rich) side of the phase diagram, increasing the solidus temperature. This approach has been used successfully in the past with SiC power die on direct bond copper substrates [18]. Control of initial AuSn volume and the reflow profile are important to achieve a high temperature die attach with 'off-eutectic' AuSn.

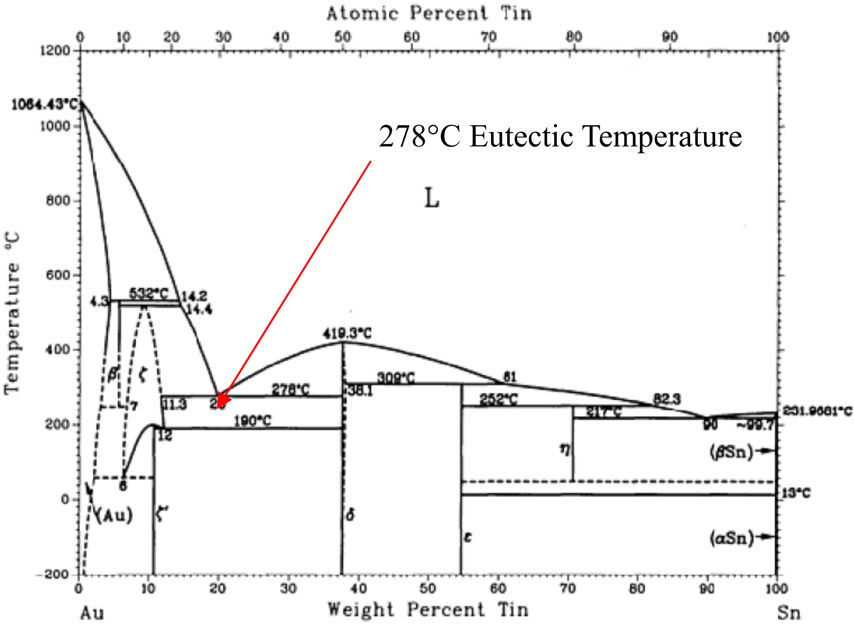


Figure 3.2 Au-Sn Phase Diagram [42]

Test vehicles fabricated for die shear and wirebonding evaluation were a two layer test vehicle with conductor on ceramic and conductor on dielectric. Five die attach and wire bonding patterns were printed on the ceramic substrate directly; the others were printed on the dielectric layer. Die attach pads and wire bonding pads were designed on this test vehicle for the 4.5mm by 4.5mm SiC test die for wire bonding. The printed substrate is shown in Figure 3.3.

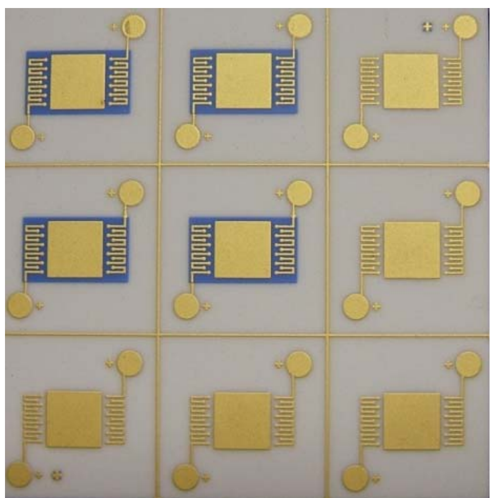


Figure 3.3 Wire bonding and Die Shear Test Vehicle

The first set of test vehicles was fabricated with conductor C101 and dielectric D1. A first metal layer for the wire bonding and die attach pattern was printed and fired on ceramic and on dielectric. On the die attach area, another conductor layer of DuPont 5063 (pure Au) was printed and fired over the previously printed and fired C101 to increase the die attach pad thickness and to increase wetting of the die attach braze. Since the solder is liquid during the die attach process, it dissolves Au from the die attach pad. If the pad is too thin, the pad can be completely dissolved during the die attach process resulting in very low adhesion. Increasing the die attach pad thickness increases the processing margin during die attach. Also, DuPont 5063 does not contain any binders and has better wetting characteristics, improving the die attach process. Based on the die shear result,

the second set of test vehicles were built with the first metal layer replaced by Au/Pt/Pd conductor C109 on the die attach pad. The wirebonding pad remained conductor C101.

3.3.2 Die Attach with Eutectic AuSn Paste

Solder paste is a viscous blended paste that consists of a flux medium containing solder powder particles. This viscous nature of the paste gives it excellent printing and reflow characteristics, thus enabling high volume production. For this research AuSn paste purchased form Indium Corporation was investigated first. Paste is preferred for assembling multiple components (actives and passives) onto a substrate since a fixture is required with preforms. Just prior to assembly, an argon plasma cleaning system was used to sputter clean both the substrate and the die. A small amount of the AuSn paste was manually dispensed on the die attach pad with a syringe, and the SiC die was carefully placed. The test vehicle was then placed inside a custom designed vacuum chamber. The reflow profile was 2 minutes at 330°C, followed by 1 hour at 280°C. The average initial die shear strength was 9.2kg/mm^2, with the die attach pad sheared off the ceramic substrate.

Different process parameters have been examined to reduce the voids under the SiC die, including applying the paste by printing, providing weight during reflow, supplying forming gas during reflow, applying vacuum during reflow, automated SiC die placement, and dispensing paste with different patterns. There are many factors that can influence void generation. A void-free die attach could be achieved with a large volume of paste, but not with the limited paste quantity required to raise the solidus temperature. Figure 3.4 is an X-ray photo showing the voids under the SiC die.

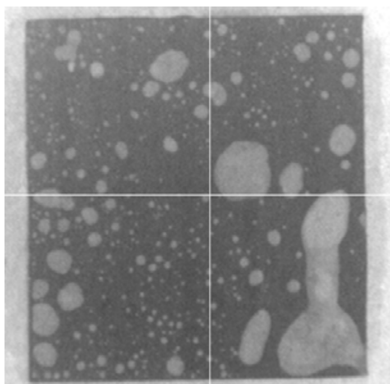


Figure 3.4 Typical X-Ray Result for SiC Die Attach with AuSn Paste

3.3.3 Die Attach with Eutectic AuSn Preform

Die attach with AuSn (80wt.%Au/20wt.%Sn) preforms has also been investigated. The preforms (25.4μm thick) were purchased from Williams Advanced Materials. An argon plasma cleaning system was used to sputter clean both the substrate and the die before assembly. To control the amount of Sn involved, the preform was cut into a 1mm by 1mm piece for use with a 2.25mm by 2.25mm SiC die. A 500 gram weight was used on top of the die-AuSn preform-substrate structure, helping the AuSn flow and cover the entire die attach area.

A profile with 3.5 minutes at 330°C followed by 30 minutes soak at 280°C was developed using an SST 3150 vacuum furnace. During the die attach process, the AuSn preform liquefied, rapidly dissolving the Au. As the Au dissolved, the melting point of the liquid increased. Once the liquid layers solidified, solid state Sn diffusion continued during the 280°C soak time. The long soak time allowed sufficient Sn diffusion into the thick film layers, lowering the Sn concentration throughout the die attach layer, thus raising the melting point of the die attach above 400°C. The Sn will continue to diffuse toward the equilibrium concentration during the high temperature service life. A void free die attach was achieved, as shown in Figure 3.5.

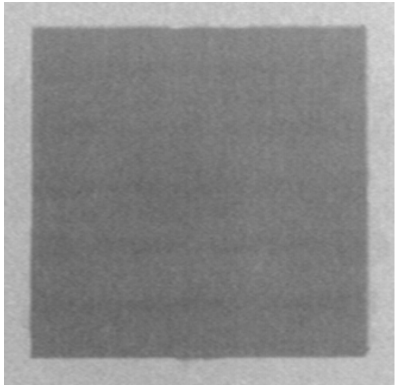


Figure 3.5 X-Ray Result for SiC Die Attach with AuSn Preform

To verify the composition of the Au/Sn after reflow, the cross-section microstructure of the die attach was examined with a JEOL-JSM-7000F Scanning Electron Microscope (SEM). Energy Dispersive Spectroscopy (EDS) was used to analyze the composition of the bonding layer, as shown in Figure 3.6 and Table 3.1. The resulting low percentage (<10wt.%) of Sn is desired to increase the solidus point. Assembled test vehicles were placed onto a hot plate and heated to 400°C. The die could not be sheared with a hand tool, indicating the die attach remained solid at 400°C. The average initial die shear strength was 10.9 kg/mm^2 at room temperature with the thick film Au lifted off from the substrate. This shear strength is comparable to that obtained with the AuSn paste, both limited by the strength of the thick film adhesion. Thus, for low power applications such as the one planned in this thesis, die attach voiding may not be an issue.

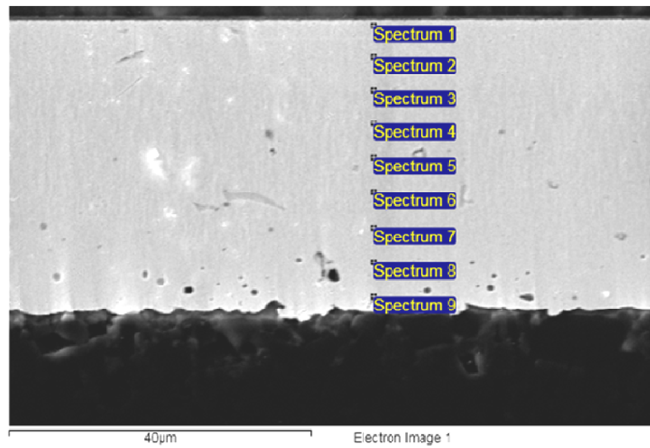


Figure 3.6 Cross-section Micrograph of Initial Die Attach with AuSn Preform.

Table 3.2 EDS Analysis on the Initial Bonding Layer

Specimen Location	W Wt%	Sn Wt%	Au Wt%	Total Wt%
1	3.67		96.33	100
2		0.89	99.11	100
3		7.16	92.84	100
4		8.67	91.33	100
5		9.02	90.98	100
6		9.59	90.41	100
7		8.52	91.48	100
8			100	100
9			100	100

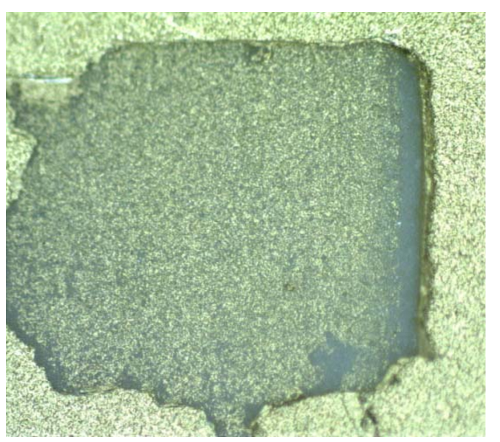
3.4 Die Attach Reliability Test

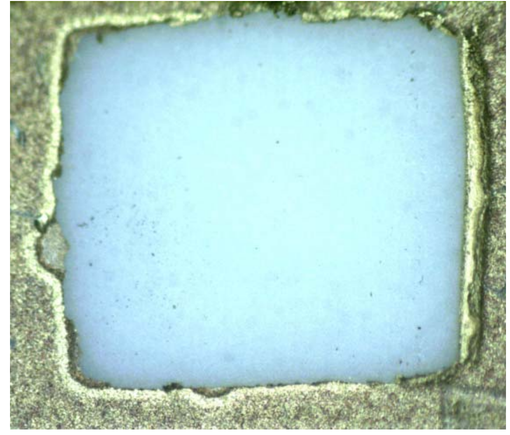
3.4.1 High Temperature Thermal Aging Test

Assembled parts were aged at 320°C in air and the die shear tests were performed at time intervals using a Dage 2400PC shear tester with a 100kg load cartridge. During high temperature aging of solder, microstructural changes can occur such as grain coarsening which changes the properties of the solder. Also, intermetallic formation occurs between the solder constituents, or between the solder and the surfaces being soldered, which can alter the mechanical properties of the solder [30].

The average initial die shear strength (kg of shear force divided by the die area) on

Al_2O_3 substrates was 10.9 kg/mm^2 at room temperature with the thick film Au lifted off from the substrate. After 500 hours aging at 320°C, the average shear strength decreased to 3.7kg/mm^2 with the thick film Au lifted off from the substrate. The shear strength continued to decrease after 1000 hour aging with the same failure mode. Figure 3.7 compares the failure mode on the substrate side after shear test, for samples as built and after 1000 hours aging. Although the failure mode remained the thick film Au lifted from the substrate, for die shear on sample as built, there was a thin layer of Au left on the ceramic; whereas for die shear on sample after 1000 hour aging, all of the thick film Au was lifted from the ceramic substrate. The shear test results as a function of storage time at 320°C are plotted in Figure 3.8.





(a) As Built (b) 1000 Hours Aged

Figure 3.7 Failure Mode on Substrate after Shear Test

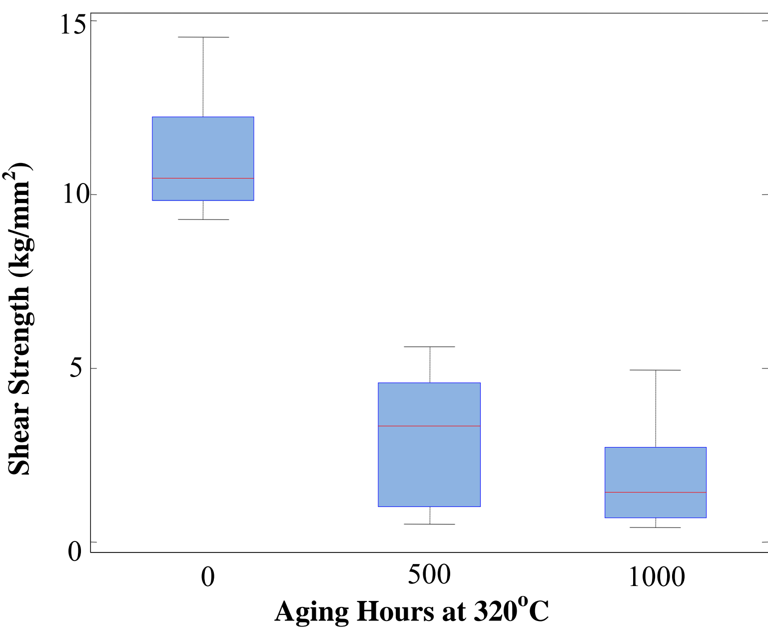


Figure 3.8 Shear Strength as a Function of Aging (320°C) with C101 on Al_2O_3

It is suspected the continued Sn diffusion caused the adhesion decrease of the thick film Au. Sn diffusion into Au is accelerated at elevated temperature. Figure 3.9 shows a wirebonded die after 2000 hours aging at 320°C, where horizontal Sn diffusion can be easily identified.

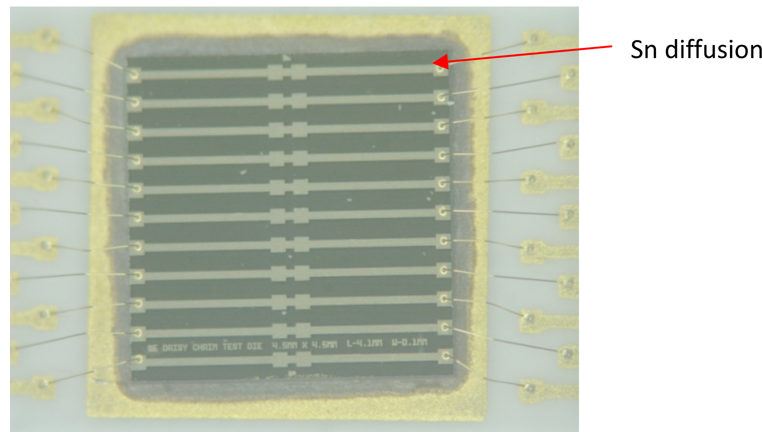
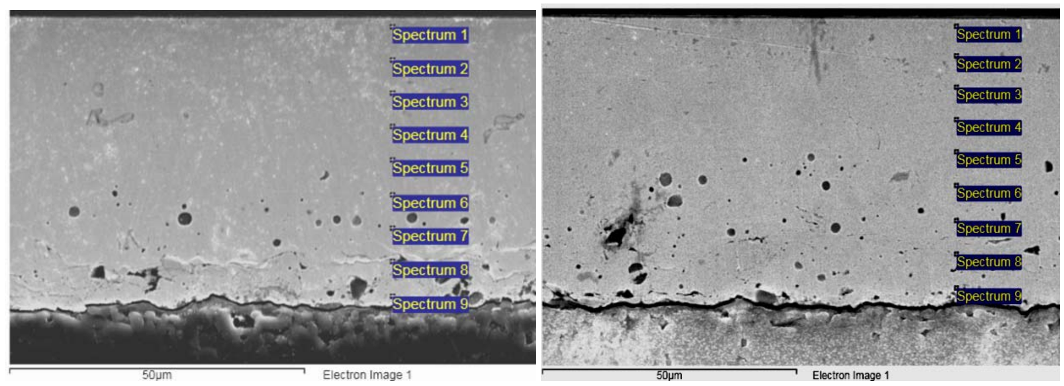


Figure 3.9 Wirebonded Sample After 2000 hour Aging at 320°C

The cross-section microstructure was examined with the SEM, and EDS was used to analyze the composition of the bonding layer on samples after 500 and 1000 hours aging. The result is summarized in Figure 3.10 and Table 3.2. The Sn percentage is much lower

compared with the as-built sample (Table 3.1). However, with 320°C aging, Sn will continue to diffuse and finally reach the ceramic substrate, resulting in adhesion loss of thick film Au.



(a) 500h Aged Sample (b) 1000h Aged Sample

Figure 3.10 Cross-section Micrograph of 320°C Aged Die Attach with AuSn Preform.

Table 3.3 EDS Analysis on the 320°C Aged Bonding Layer

	500h Aged			1000h Aged		
Specimen Location	Sn Wt%	Au Wt%	Total Wt%	Sn Wt%	Au Wt%	Total Wt%
1	3.01	96.99	100	2.44	97.56	100
2	4.60	95.40	100	2.96	97.04	100
3	3.62	96.38	100	2.23	97.77	100
4	3.14	96.86	100	2.38	97.62	100
5	2.90	97.10	100	1.58	98.42	100
6	2.95	97.05	100	1.88	98.12	100
7	2.34	97.66	100	2.18	97.82	100
8	2.33	97.67	100	3.29	96.71	100
9	2.83	97.17	100	3.71	96.29	100

To investigate this further, thick film conductor C101 (Au) was replaced by thick film conductor C109 (Au/Pt/Pd). It is known that Sn and Pt will form an intermetallic, consuming Sn. New test vehicles were built with conductor C109, dielectric D1, and thick film gold 5063. The die attach used the same AuSn preform and all the die attach process parameters remained the same. The shear test was performed on the substrates with thick film metallization on ceramic and substrate with thick film metallization

printed on the thick film dielectric C109 on top of ceramic. The shear test results as a function of aging at 320°C are plotted in Figure 3.11.

For shear test performed on substrates with thick film metallization on ceramic, the average initial die shear strength was 10.1kg/mm^2 with failure inside the thick film metallization. After 500 hours aging at 320°C, the average shear strength decreased to 9.3kg/mm^2 with the same failure mode. The average shear strength increased to 10.8 kg/mm^2 after 1000 hours aging and decreased to 8.0kg/mm^2 after 2000 hours aging at 320°C with the same failure mode. T-test was performed on the shear test data and result shows there was no statistical difference for shear strength on sample as built, sample after 500 hours, 1000 hours, and 2000 hours aging.

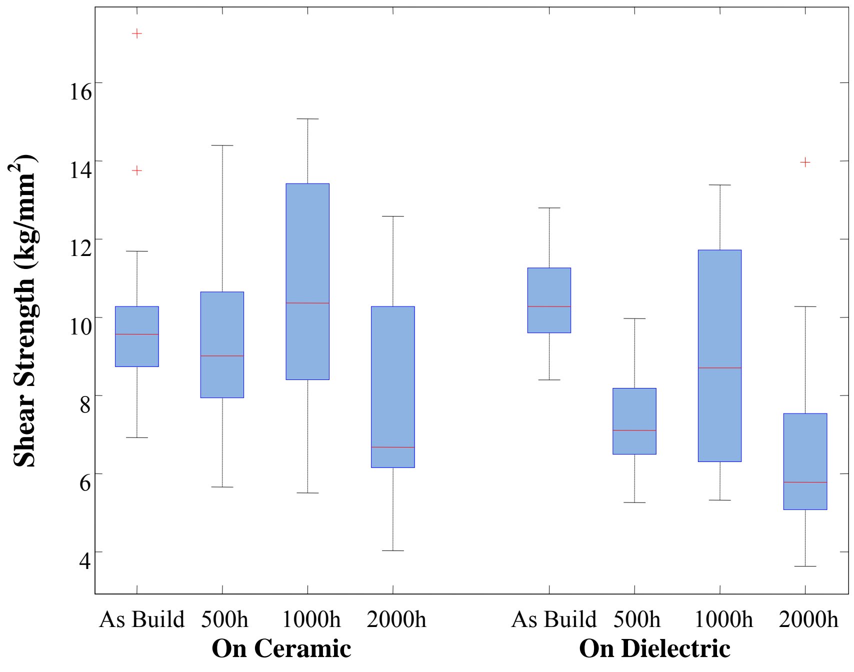
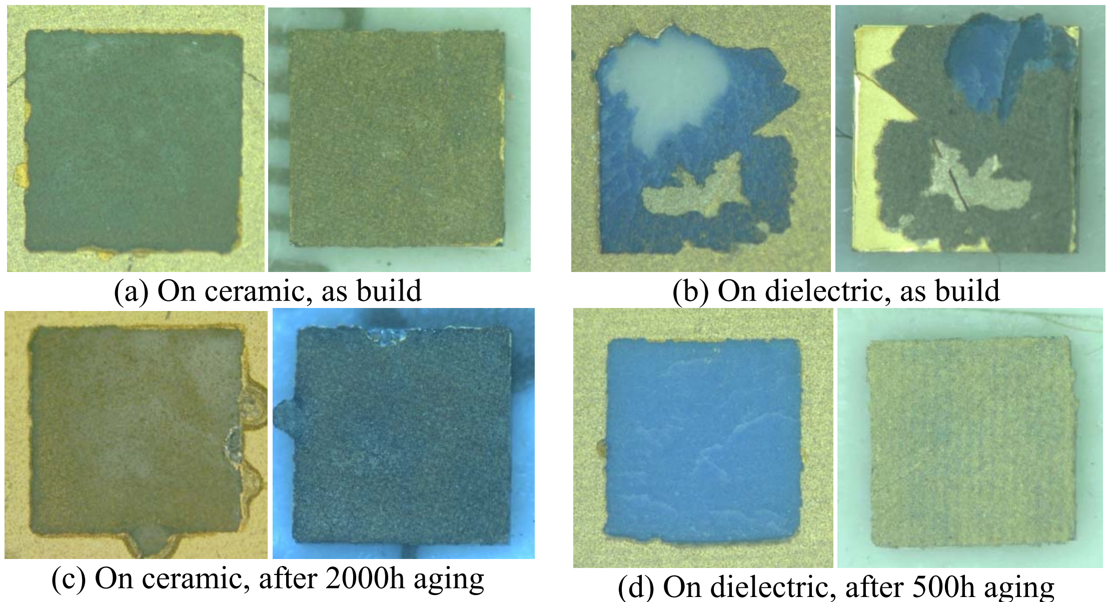


Figure 3.11 Shear Strength as a Function of Aging (320°C) with C109 and D1

For shear test performed on substrate with thick film metallization on dielectric D1, the average initial die shear strength was 10.7kg/mm^2 with the dielectric lifted off from the substrate and thick film metallization lifted off from the dielectric. After 500 hours

aging at 320°C, the average shear strength decreased to 7.4kg/mm^2 with the thick film metallization lifted off from the dielectric. The average shear strength increased to 8.9 kg/mm^2 after 1000 hours aging and decreased to 6.9kg/mm^2 after 2000 hours aging at 320°C with the failure mode between the thick film metallization and the dielectric. This decreasing may due to the decreased conductor to dielectric adhesion after aging. T-test was performed on the shear test data and results show there was no statistical difference for shear strength on sample as built, sample after 500 hours, and 1000 hours aging. Shear strength after 2000 hours aging does have a statistical difference than data from other groups. Although the shear strength decreased for both die shear on ceramic and on dielectric after 2000 hours aging, it was still very high with respect to 2.5kg minimum shear strength specified in Mil-Std-883 [43].

Figure 3.12 shows the initial failure mode for the die attached on ceramic (a) and on dielectric (b). The failure mode remains the same for die attach on ceramic after 2000 hours aging (c). For die attach on dielectric, the failure mode changed to failure between metal to dielectric after 500 hours aging (d).



(a) On ceramic, as build
(b) On dielectric, as build
(c) On ceramic, after 2000h aging
(d) On dielectric, after 500h aging

Figure 3.12 Failure Mode for Die Shear as Built and after Aging

3.4.2 Thermal Cycling Test

Thermal cycle testing was used to determine the ability of the package to withstand the stresses from cyclical exposure to those temperature extremes. Temperature cycling primarily accelerates the fatigue failures that result from cyclical thermomechanical loading. The thermal cycle test samples were assembled with larger die (4.5mm x 4.5mm) and preform (2mm x 2mm). A larger die size was selected to increase the die attach stresses during thermal cycling. Test substrates were built with conductor C109 and thick film gold 5063. The thermal cycle profile was from 25°C to 320°C in air, as shown in Figure 3.13, which consisted of 20 minutes ramp from 25°C to 320°C, 10 minutes soak at 320°C, 20 minutes cool down from 320°C to 25°C, and 10 minutes soak at 25°C

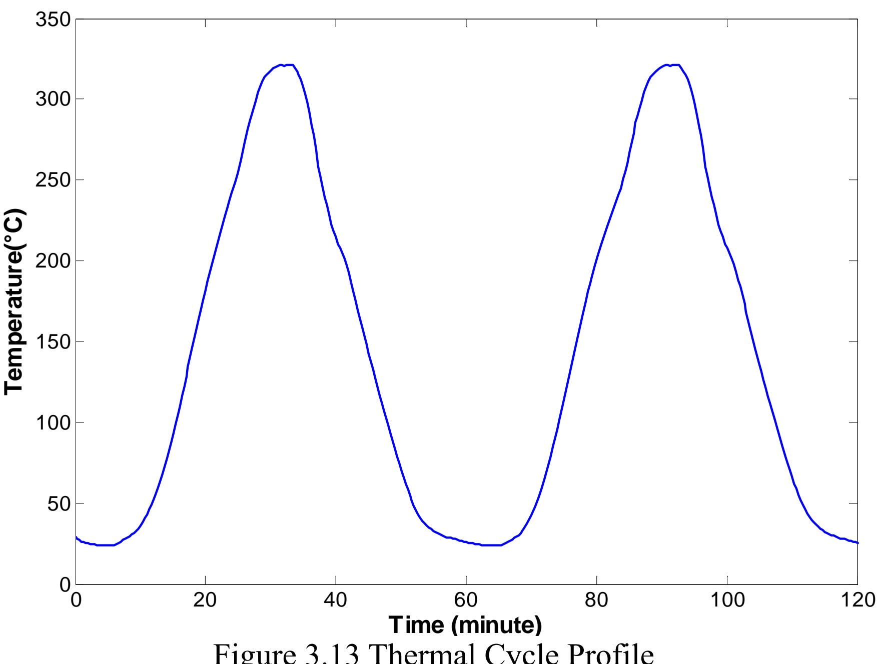


Figure 3.13 Thermal Cycle Profile

Die shear tests were performed on assembled die as built and after 1000 cycles with a group sample size of 10. All the test samples (10 samples as built and 10 samples after 1000 cycles) did not shear at the maximum shear force of the load cell (100kg).

3.5 Wire Bonding

There are two common wirebonding processes: ball bonding and wedge bonding.

In ball bonding, a capacitive discharge spark melts the tip of the wire and the surface tension of the molten gold forms the ball. This is called the “flame-off” process [44]. The ball is placed at the target bond pad with pressure and heat, and ultrasonic forces are applied for a specific amount of time, forming a metallurgical bond between the ball and pad. The capillary is then moved to the corresponding lead finger or substrate pad, rests against the pad surface and ultrasonic energy with heat and pressure forms the stitch and cuts the wire. The entire sequence of ball-stitch bonding is shown in Figure 3.14. [45]

In wedge bonding, a stub of wire is pressed against the bond pad by the foot of the bonding tool, applying ultrasonic energy to form the bond between the wire and pad. The capillary is then moved to the second bond location and the process is repeated. Once the second bond is completed, the wire is clamped and snapped above the second bond [44].

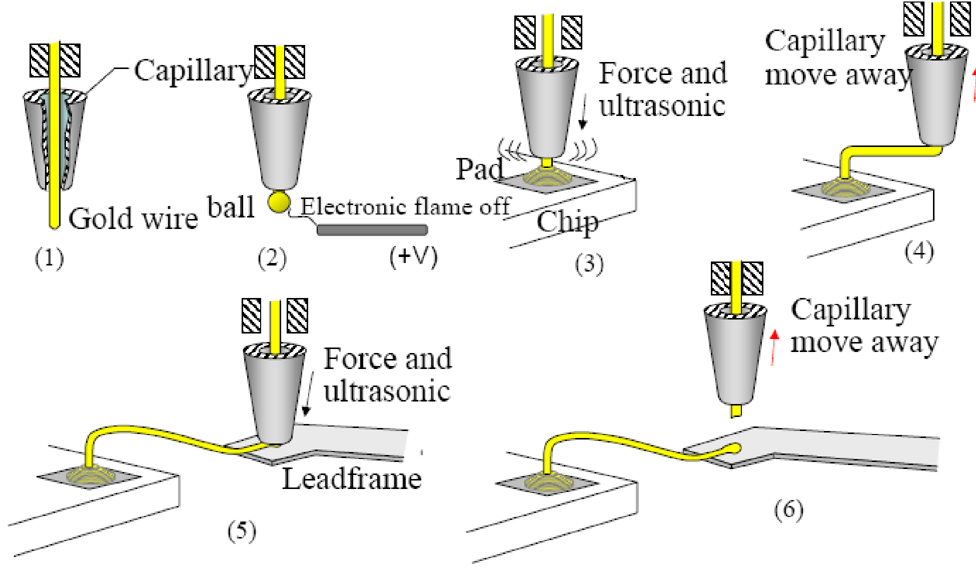


Figure 3.14 Schematic Sequence of Ball-Stitch Wire Bonding [45]

3.5.1 Wire Bond Pad Metallurgy

Gold thermosonic wire bonding provides a monometallic interconnect system between the die and the substrate pads. Small diameter (1 mil) gold wire was bonded with a Palomar 2460-V thermosonic wire bonder. The wire was purchased from Custom Chip Connections with 2~6% elongation and a minimum tensile strength of 9 grams. The first bond was placed on the SiC die and the second bond was placed on the alumina substrate with C101 thick film gold pads. Bonding force, time, temperature and capillary were optimized to improve the bonding strength. The initial die topside metallization for the pad and interconnection was: 1μm Au, 2kÅ Ti, 500Å NiSi, and 500Å Ni.

3.5.2 Wire Bond Pull Test

The wire pull test was performed using a Dage PC2400. The initial average pull strength was 9.19 grams with failure in the wire. After 500 and 1000 hours aging at 320°C, the pull strength decreased with all the failure still in the wire. This is due to the annealing of the gold wire that occurs at elevated temperature. This decrease was expected and was not large enough to cause reliability problems in high temperature application. After 1500 hours aging, about half the wires still failed in the wire, with an average pull strength of 6.60 grams, and the other half failed due to the pad on the SiC die lifting, with an average pull strength of 3.51 grams. This divergence continued after 2000 hours aging. The wire pull strength as a function of aging time at 320°C is plotted in Figure 3.15. Each data point represents the average of 32 measurements.

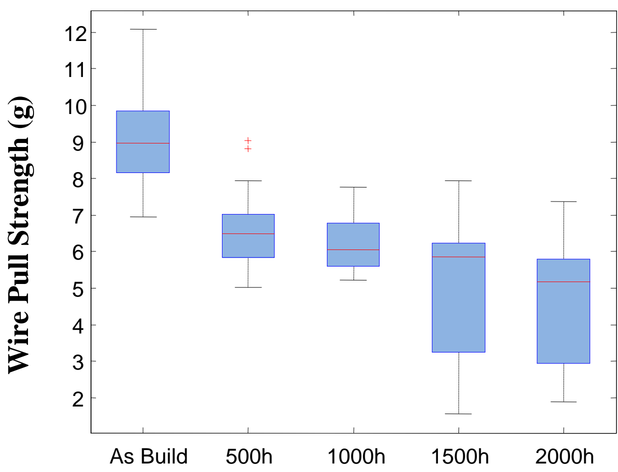


Figure 3.15 Wire Pull Strength as a Function of Aging (320°C)

3.5.3 Wire Bond Ball Shear Test

The ball shear test results are plotted in Figure 3.16. Each data point represents the average of 32 measurements. The initial average ball shear strength was 63.5 grams, with failure in the Au ball. After 500 hours aging at 320°C, the average ball shear force increased to 70.4 grams. All but one failure was still in the Au ball. In one test, the wire bond pad on the SiC die partially sheared off with the Au ball. After 1000 hours of aging, the average ball shear strength decreased to 51.1 grams, with more pads found partially lifted with the Au ball. The shear strength began to diverge, depending on the lifted pad area. Figure 3.17 shows two SEM photos of pads after shear testing, with shear strengths of 65.8 grams (a), and 34.9 grams (b). All of the SEM photos indicate that the shear strength was inversely proportional to the area of pad lifting.

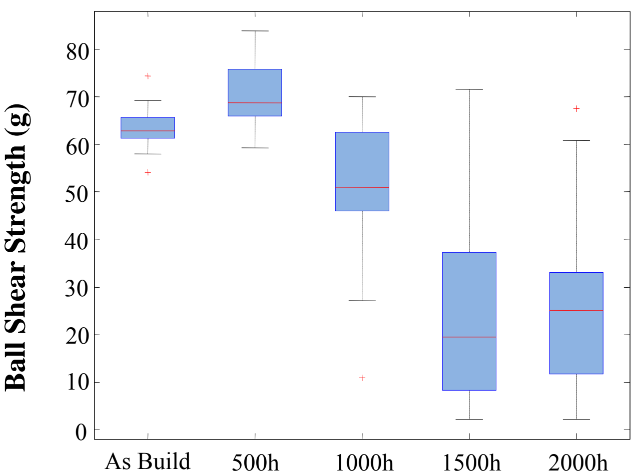
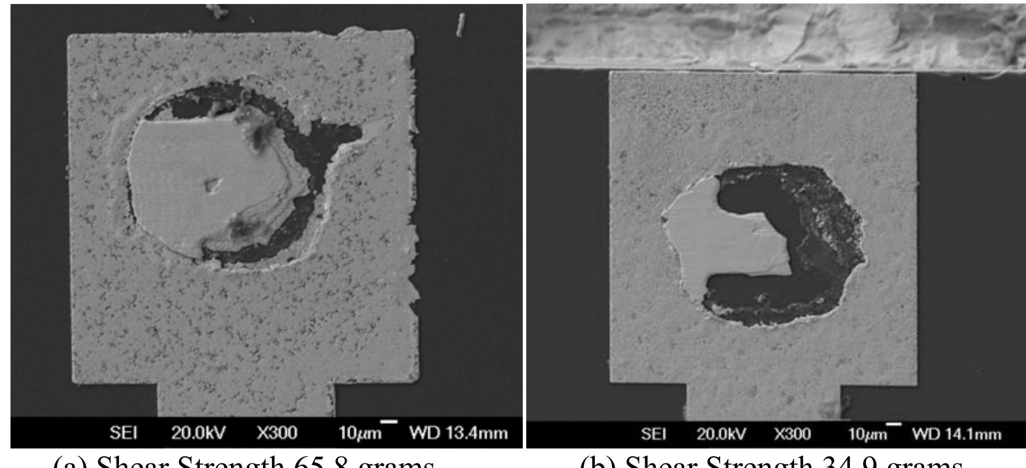


Figure 3.16 Ball Shear Strength as a Function of Aging (320°C)

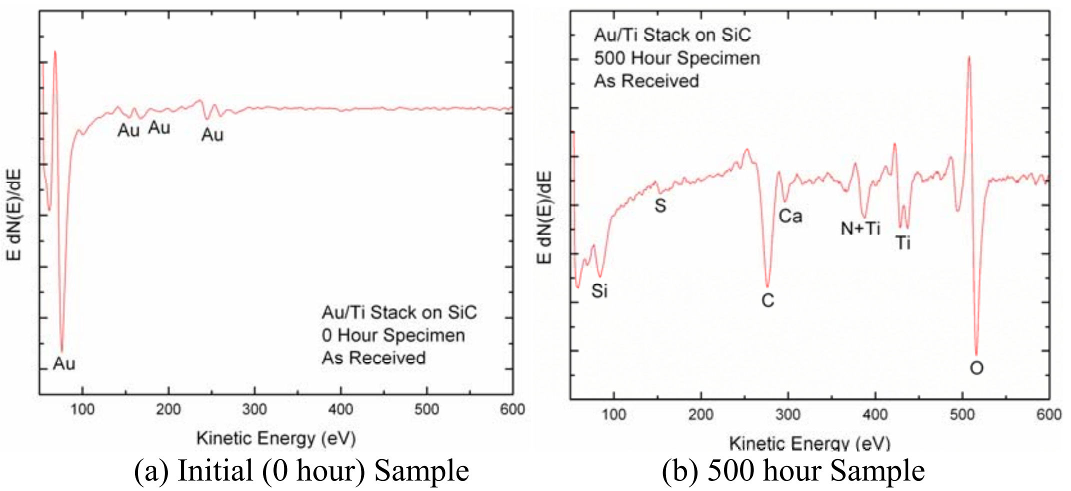
The shear strength continued to diverge after 1500 hours aging. Approximately 60% of the samples had entire pads lifted during shear test, with an average shear strength of 13.4 grams. The remaining samples all had pads partially lifted, with an average shear strength of 50.1 grams. The results after aging for 2000 hours were similar.

It was suspected that the Ti diffused into Au, causing the loss of pad adhesion. Surface analysis was done using a Kratos XSAM 800 surface analytical system with Auger electron spectroscopy (AES). Figure 3.18 shows the test result on the 0 hour (a) and the 500 hours (b) aged samples. No Ti was found on the pad surface of a 0 hour sample, but a significant amount of Ti was observed on the surface of 500 hours and 1000 hours aged samples. For high temperature application, a diffusion barrier is required between the Ti and Au layers.



(a) Shear Strength 65.8 grams (b) Shear Strength 34.9 grams

Figure 3.17 Wire Bonding Pad after Ball Shear Test on Sample after 1000 Hours Aging at 320°C



(a) Initial (0 hour) Sample (b) 500 hour Sample

Figure 3.18 Auger Test Result for 0 hour Sample and 500 hour Aged Sample (320°C)

3.5.4 Daisy Chain Electrical Resistance

Daisy chain resistance was measured on the wirebond test vehicle. The daisy chain included 22 Au wires, the metallization traces on the die and the thick film Au on the Al_2O_3 substrate, as shown in Figure 3.19. Each resistance data point through 2000 hours of storage represents the average of 18 daisy chain resistance measurements. The initial average resistance based on 18 test samples was 13.0Ω, as shown in Table 3.3. After 500 hour aging at 320°C, the average resistance increased to 33.2 Ω. This number decreased to 24.6 Ω after 1000 hour aging and to 21.9 Ω after 1500 hour and finally to 20.8 Ω after

2000 hour aging at 320°C. The resistance was measured at room temperature. This shift was not expected and but is consistent with Ti diffusing into Au layer, raising the resistance of the on-die traces.

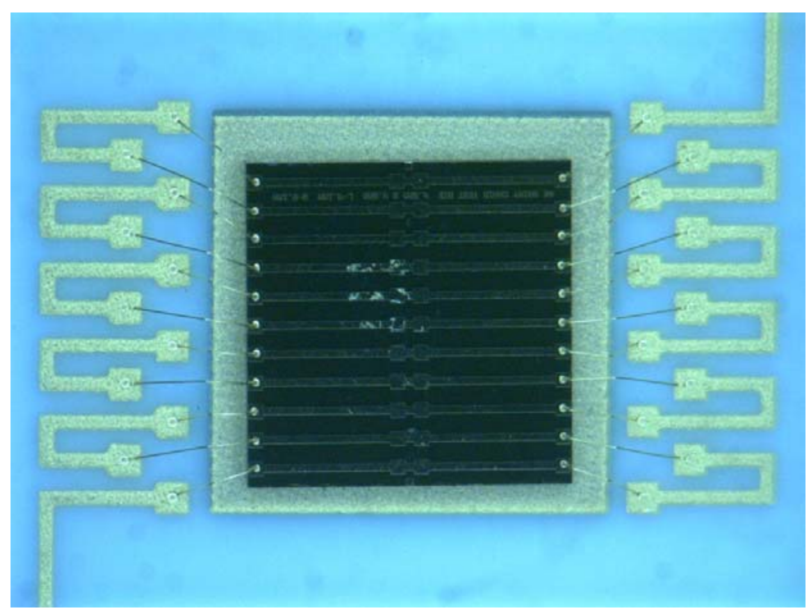


Figure 3.19 Test Vehicle for Daisy Chain Resistance Measurement

Table 3.4 Average Daisy Chain Resistance (Ω)

Aging Time	0h	500h	1000h	1500h	2000h
Avg. Daisy Chain Resistance (Ω)	13.0	33.2	24.6	21.9	20.8

3.5.5 New Metallization Evaluation

Several SiC wafers were fabricated using a different topside metallization, with the same test pattern. Those wafers were fabricated to test the topside metallization reliability in high temperature and did not have a backside metallization. Thus both the first and second bonds were placed on the wafer. Bonding locations were carefully selected so the daisy chain resistance could be measured on the wafer. Test vehicles were assembled for wire pull tests, ball shear tests and daisy chain electrical resistance measurement. For proprietary reason, those metallization were labeled as 5B, 10D, and 10C.

The wire pull strength as a function of aging time at 320°C is plotted in Figure 3.20.

Wirebonding on metallization 5B and 10D had stabilized wire pull strength after 500 hours aging, with the failure mode in the wire after 1500 hours aging. Pull strength on metallization 10C decreased rapidly after 500h aging, with the pad metallization pulled off from the SiC die.

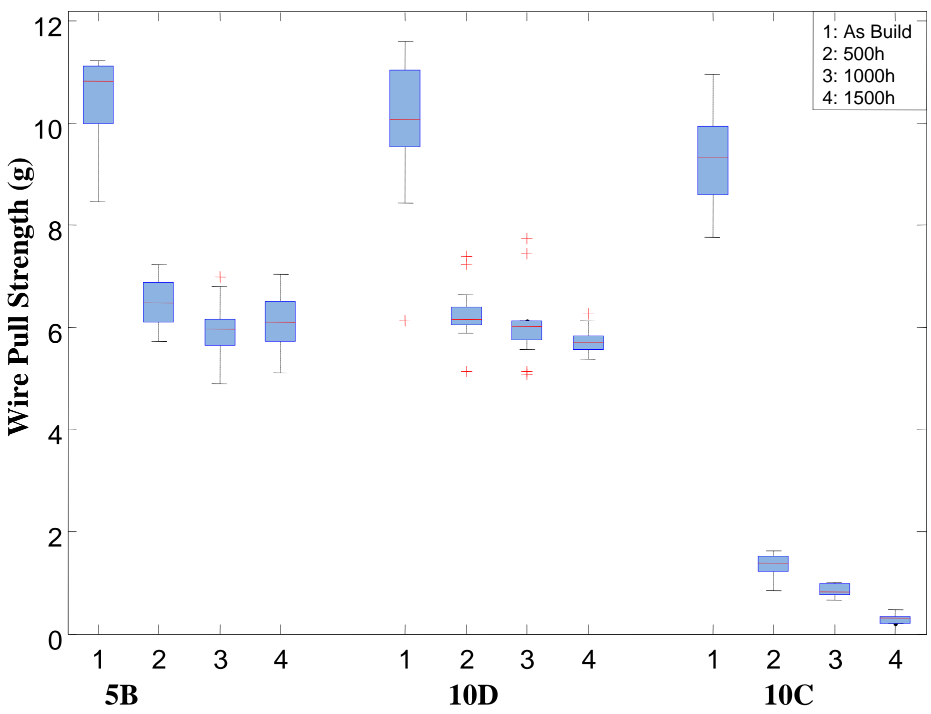


Figure 3.20 Wire Pull Strength as a Function of Aging (320°C) with New Metallization

The ball shear strength as a function of aging time at 320°C is plotted in Figure 3.21. The ball shear strength with metallization 5B decreased with aging time, but had a sudden increase after 1500 hours aging, with all the failures in the ball. This could indicate intermetallic formation. For metallization 10D, the ball shear strength had a small decrease after 500 hours aging and remained relatively costant, with all of the failures in the gold ball. For metallization 10C, the initial ball shear strength is high, with the failure in the ball. But after 500 hours aging, the shear strength decreased significantly with all of the bonding pad pulled off from the SiC die.

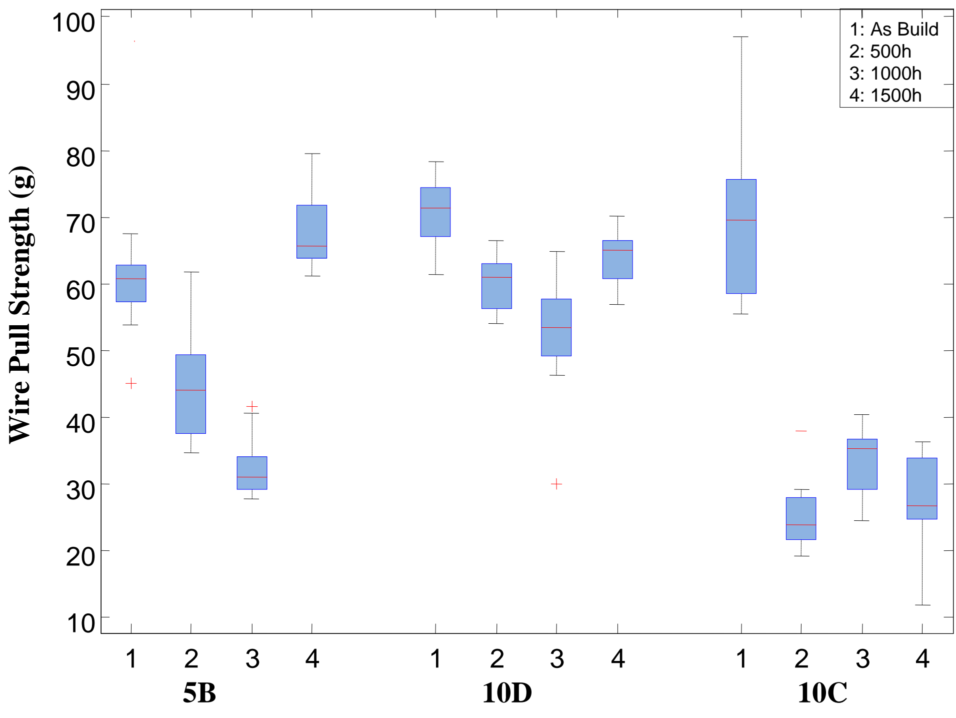


Figure 3.21 Ball Shear Strength as a Function of Aging (320°C) with New Metallization

Daisy chain resistance was also measured on the test vehicle with new metallization stack 5B, 10D, and 10C. Their daisy chain resistance as a function of aging time at 320°C is plotted in Figure 3.22. The daisy chain resistance from metallization 10C increased significantly after 500 hours aging, which is consistent with the wire pull and ball shear result. For metallization 5B, the daisy chain resistance increased approximately 50% and stabilized after 500 hours aging. For metallization 10D, the daisy chain resistance had a very small increase after 1000 hours aging and remained the same after 1500 hours aging.

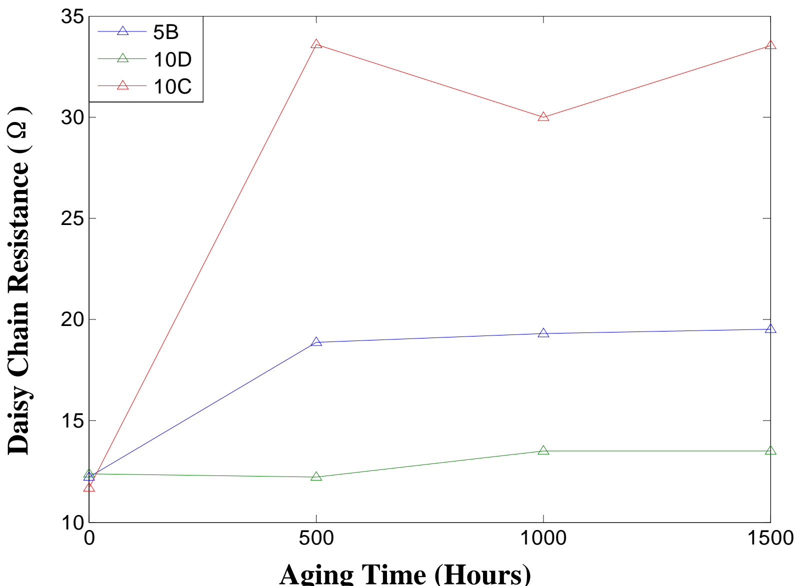


Figure 3.22 Average Daisy Chain Resistance (Ω) as Function of Aging (320°C) with New Metallization

3.6 Summary

Die attach and wirebonding that can withstand operation temperature up to 300°C has been demonstrated with SiC die on thick film metalized Al_2O_3 substrates. Different thick film metallization has been investigated with eutectic AuSn solder. With thick film conductor C109 on ceramic and on dielectric D1, the die shear strength after 2000 hours storage at 320°C was high with respect to minimum shear strength specified in Mil-Std-883. The large die used for thermal cycle testing did not shear with 100kg load after 1000 cycles.

Different die topside metallizations have also been investigated. The metallization 10D showed the best overall results after 1500 hours aging at 320°C. The 10C metallization performed worst with pad lifts during pull test, ball shear and an increase in resistance with 320°C aging. The 5B wafer had good mechanical test results, but an increase in electrical resistance of ~50% was observed after 500 hours at 320°C.

CHAPTER 4 PASSIVE COMPONENTS ATTACH

4.1 Introduction

Although semiconductor devices are key elements in electronics, passive components are a necessary ingredient in any practical system. Availability of certain passive components with adequate high temperature ability is a major obstacle for high temperature electronics. To meet the high temperature requirement, most users have had to indentify existing conventional temperature components that could be used beyond their rated temperature.

This chapter examines several resistors and capacitors that have the potential to work at 300°C. After initial testing, a thick film resistor and a multilayer ceramic chip capacitor (MLCC) were selected for further thermal aging and thermal cycling tests to access attachment reliability. The shear test results and failure modes are discussed. Attachment of Molybdenum (Moly) tabs to the substrate metallization was also investigated as external lead/wire attachment points.

4.2 Passive Components Selection

Thick film resistors generally have good stability for high temperature operation, partly because of their initial processing temperature, which is about 500°C~1000°C [46]. Thick film resistors are typically rated over the military temperature range of -65°C to +150°C [47]. Some ruthenium based resistor inks that use a higher softening point glass are suitable for higher temperature applications [46]. The conduction mechanism for

thick film resistors is not well understood and the materials are proprietary compositions.

Wirewound resistors made from heat-resistant wire and ceramic are also well suited for high temperatures. Powered and unpowered aging to 300°C has shown reasonable stability, and some commercial versions are capable of 500°C operation [46].

Organic dielectrics generally can be used to about 200°C. Inorganic dielectrics are required for higher temperatures [46]. Ceramic based thick film capacitors have been proved to work at 300°C to 500°C [47].

For our study, four passive components were selected for initial test. They were Vishay Wirewound resistor, Mini-Systems thick film resistor, TRS high temperature capacitor, and KEMET ceramic capacitor.

The Vishay WSC4527 wire wound resistor features thermoplastic encapsulation, high power rating (2.0W at 70°C), and wraparound terminations, with an operating temperature range from -65°C to 275°C. The temperature coefficient is ±20 ppm/°C for resistance larger than 10Ω. The reliability test from the manufacture shows stable result, after 1000 hours at 275°C [48]. The wire wound resistor comes with a CuSn termination. The Sn was etched and Ni/Au was plated by GE Global Research Center. However, the thermoplastic encapsulation will melt at 300°C, before reaching the attachment temperature. A photo of a Vishay WSC 4572 resistor is shown in Figure 4.1.

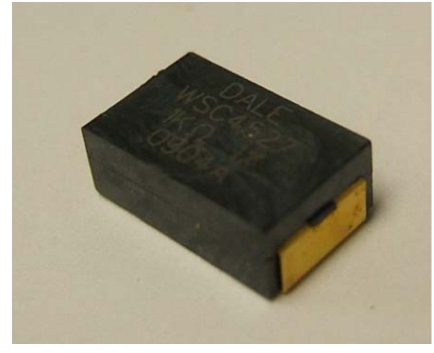
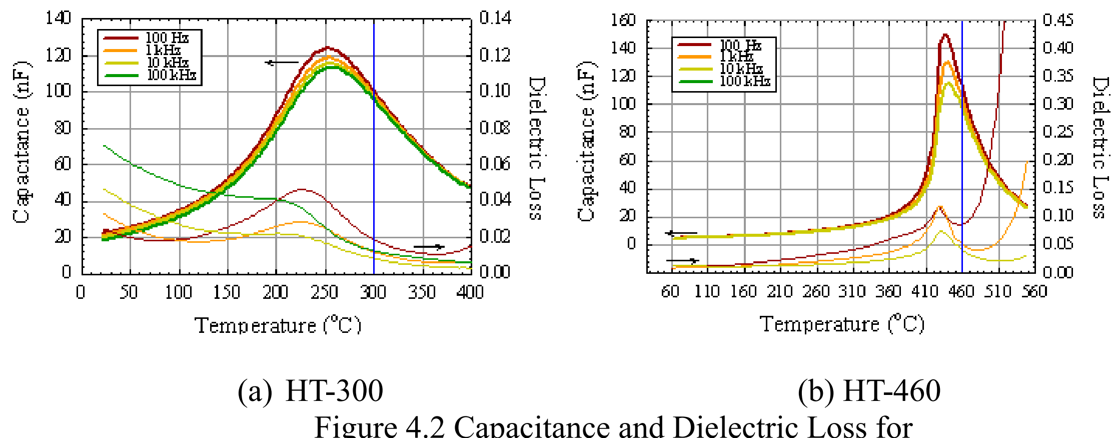


Figure 4.1 Vishay WSC4527 Resistor

The Mini-Systems QPL thick film resistors are printed and fired on 96% alumina. The case size selected was 1206, with 0.25W/100V power rating. The resistors had wrap around (5 sided) Pt-Au terminations. The resistors passed reliability test at 70°C for 10,000 hrs and exceed the qualification requirements of MIL-PRF-55342. The operating temperature specified in the datasheet is from -55°C to 150°C [49].

TRS high temperature capacitors are based on a unique relaxor ferroelectric with high volumetric efficiency. The temperature characteristics of the dielectric was engineered to provide high dielectric constant (K) performance centered around operating temperatures of 300°C (HT-300) and 450°C (HT-460) [50]. The performance characteristics of HT-300 and HT-460 are shown in Figure 4.2. Near the operating temperature, HT-300 capacitors are designed with a 4X voltage safety margin, a RC constant of 11Ω-F, about 30% change in capacitance at the rated voltage, and limited frequency dependence. The TRS high temperature capacitor came with a thick film Au termination.



(a) HT-300 (b) HT-460
Figure 4.2 Capacitance and Dielectric Loss for
TRS High Temperature Capacitor [50]

KEMET's high temperature surface mount C0G multilayer ceramic capacitors

(MLCCs) feature a robust, proprietary base metal dielectric system that offers significant reliability and performance advantages over traditional MLCC's for extreme temperature applications up to 260ºC [51]. The Electronics Components, Assemblies & Materials Association (EIA) characterizes C0G dielectric as a Class I material. Components of this classification are temperature compensating. C0G exhibits no change in capacitance with respect to time and voltage and boasts a negligible change in capacitance with reference to ambient temperature. Capacitance change is limited to ±30ppm/ºC from -55°C to +200°C. It has high thermal stability, high ripple current capability, and extremely low equivalent series resistance (ESR) and equivalent series inductance (ESL). The performance and reliability test passed MIL-STD-202/JESD22 with high temperature storage at 200ºC for 2000 hours under rated voltage. The KEMET ceramic capacitor comes with a CuNiSn termination. For compatibility with 300°C operation, the Sn was etched and Au was plated at GE Global Research Center. The detail of the Sn-stripping and Au-plating process can be found in [21].

4.3 Resistor and Capacitor Attach

The test vehicle fabricated for the passive component attach process development and evaluation was a two layer test vehicle. The bottom layer was thick film conductor C109, and the top layer was thick film conductor DuPont 5063. The bottom conductor provided adhesion to the ceramic substrate. The top conductor increased the pad thickness and increased the wetting of the component attach metallurgy, as described in Chapter 3.1.1. Four test patterns were designed on this test vehicle, corresponding to the four components discussed above, as shown in Figure 4.3. The test substrates were diced into four smaller pieces for bonding different components.

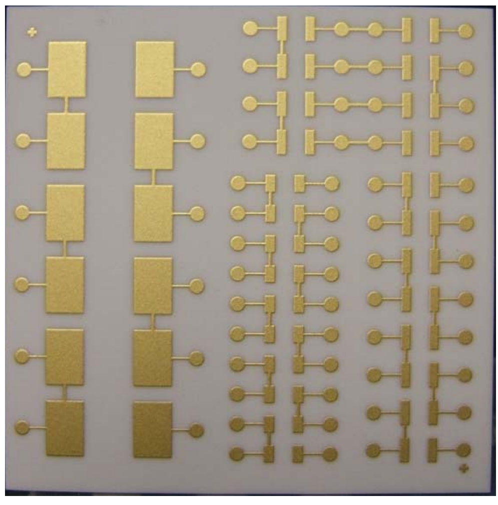


Figure 4.3 Passive Component Attach Test Vehicle

4.3.1 Process Development

AuSn paste purchased from Indium Corporation was investigated first since paste is preferred for assembling multiple components. A small amount of AuSn paste was manually dispensed on the pad with a syringe, and the passive component was carefully placed. The test vehicle was then placed inside a custom designed vacuum chamber. The reflow profile was 2 minutes at 330°C, followed by 10 minutes at 280°C. The initial shear strength was low, with a lot of voids found inside the solder joint. Figure 4.4 is an X-ray photo showing the voids under one termination of the component.

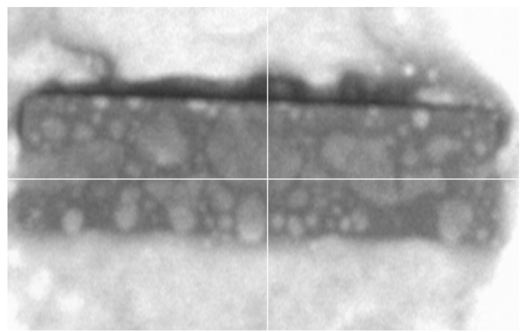


Figure 4.4 X-Ray Result of Passive Component Attach with AuSn Paste

As described in the die attach process, the quantity of AuSn solder dispensed must be

controlled carefully to achieve a high-temperature stable solder joint. With limited AuSn paste, there is not enough wetting between the solder paste and component termination. Unlike the traditional passive component soldering, where a solder fillet is formed to increase contact area and increase mechanical strength, in this process only the bottom component termination is in contact with the solder paste. Thus a void free solder joint is desired to increase the mechanical strength with limited contact area.

Passive component attach with AuSn (80wt.%Au/20wt.%Sn) preforms was investigated next. The preforms (25.4μm thick) were purchased from Williams Advanced Materials. To control the amount of Sn involved, the preform was cut to approximately 30% of the component termination area. The preforms were carefully placed on the pad, and the component was manually placed on the substrate. The preforms and component placement was done under the microscope, since the preforms were very small and high accuracy was required. This component-preforms-substrate structure was then placed on the chuck of FC150 Flip Chip bonder. The initial bonding profile uses 4kg forces with 4 minutes at 360°C followed by 2 minutes soak at 280°C. A void free solder joint can be achieved, as shown in Figure 4.5.

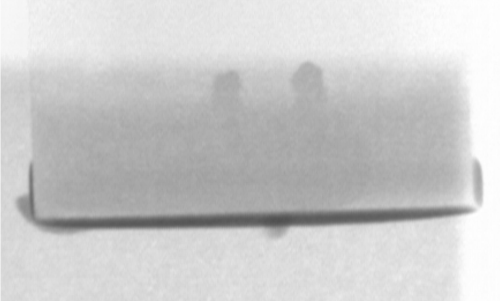


Figure 4.5 X-Ray Result of Passive Component Attach with AuSn Preform

During the bonding process, applied force will squeeze out excessive AuSn solder, making a uniform and thin solder joint layer, as shown in Figure 4.6. The X-Ray result in

Figure 4.5 also shows the solder being squeezed out. Au was dissolved into the molten AuSn from the component termination and from the substrate metallization. This shifts the alloy composition to the left (Au rich) side of the phase diagram, increasing the solidus temperature. To verify the process, assembled test vehicles were transferred onto a hotplate and heated to 350°C. Bonded components retained high mechanical strength at this temperature and cannot be removed with tweezers, indicating the solder joint remained solid at 350°C

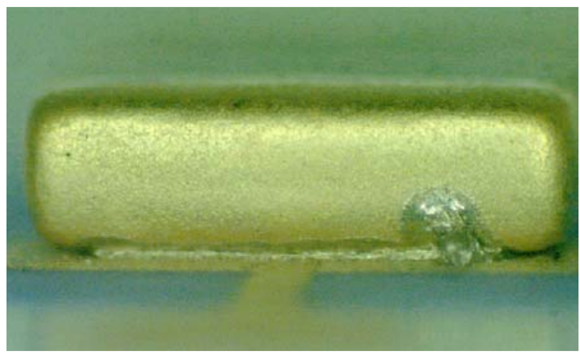


Figure 4.6 Side View of KEMET Capacitor after Bonding

A few Mini-Systems resistors, TRS capacitors, and KEMET capacitors were attached on the test substrate for initial process optimization. Vishay Wirewound resistor was not investigated due to the encapsulation melting at 300°C. It was found that the 4kg bonding force can cause cracking on resistor and capacitor body. Subsequent assembly used a bonding force of 1.5kg for resistors and 1.2kg for capacitors, to reduce the potential damage on the passive component body.

4.3.2 High Temperature Thermal Aging Test

After initial evaluation, Mini-Systems resistors and KEMET capacitors were selected for further reliability tests. The TRS high temperature capacitor was desired for bonding on Au thick film metallization since they come with a thick film Au termination.

However, the dielectric used in the TRS capacitor was specially engineered to reach the designed value only at target temperature. In other words, electronic devices built with those capacitors may not work at room temperature, which creates challenges in initial testing and verification. Furthermore, although the goal of this project is to develop functional electronics that can be used to monitor wellbore conditions at 300°C, the developed device must also work at a lower temperature.

Changes in resistance and capacitance with high temperature storage can result from a combination of mechanisms including annealing of the glass, diffusion with the resistor/capacitor matrix, diffusion between the resistor/capacitor and the termination metallization, and micro crack growth [47]. The important parameters for resistors and capacitors include temperature coefficient of resistance (TCR), temperature coefficient of capacitance (TCC), breakdown voltage, leakage resistance, and dissipation factor. This part of the evaluation was done by GE Global Research and had been well documented in the publications [21] [52]. Here the focus was on the bonding strength with high temperature storage and thermal cycling.

A new passive component attach test vehicle was designed based on the previous version, to provide test patterns for the Mini-Systems resistors and KEMET capacitors, as shown in Figure 4.7. Each test substrate provided 20 attachment sites for resistors and 20 attachment sites for capacitors. 160 Mini-system resistors and 160 KEMET capacitors were attached using FC150 flip chip bonder with the pre-described bonding profile. Their shear strength was recorded initially, after 500, 1000, and 2000 hours aging at 320°C.

Figure 4.7 Test Vehicle for Mini-Systems Resistor and KEMET Capacitor

The results are summarized in Figure 4.8. Each data point represents the average of 20 test samples. The initial average shear strength for the Mini-System resistor was 9.8kg, with failure half in the component termination metallization and half in the thick film metallization on the substrate. This failure mode was expected since the component termination was AuPt and the substrate metallization was thick film Au on thick film AuPt. The average shear strength decreased to 9.0kg, 8.3kg, and finally 7.4kg after 500 hours, 1000 hours, and 2000 hours aging at 320°C, with the failure mode remaining the same, as shown in Figure 4.9 and Figure 4.10. For shear test after 1000 hours and 2000 hours aging, 10% of the samples had small pieces of ceramic from the resistor body left on the substrate after shear test.

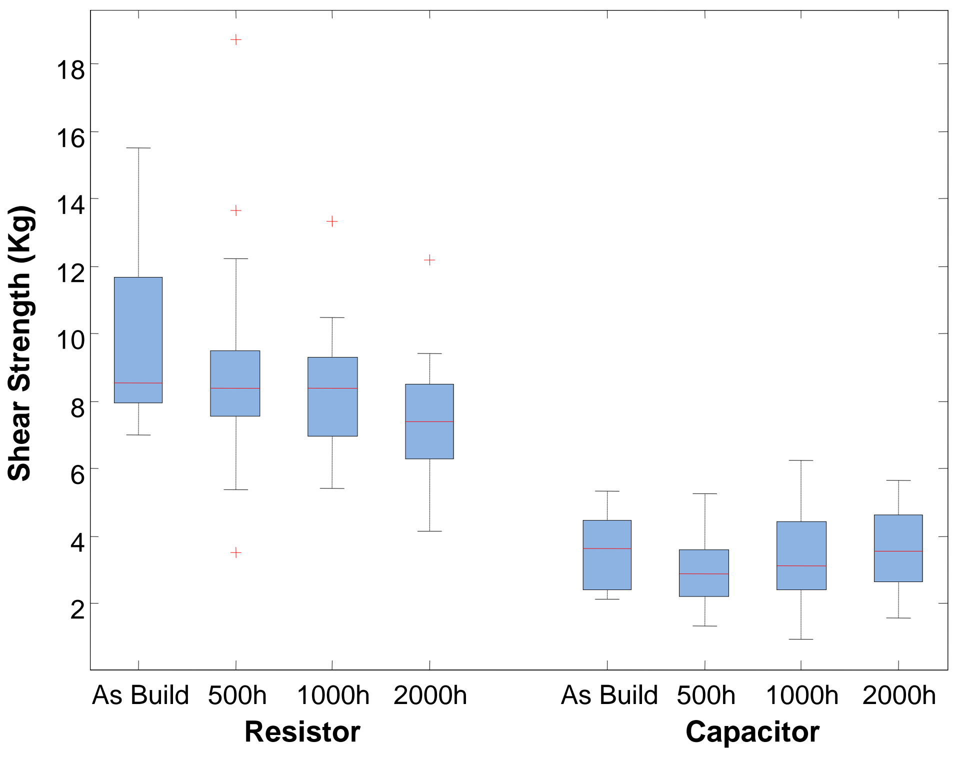
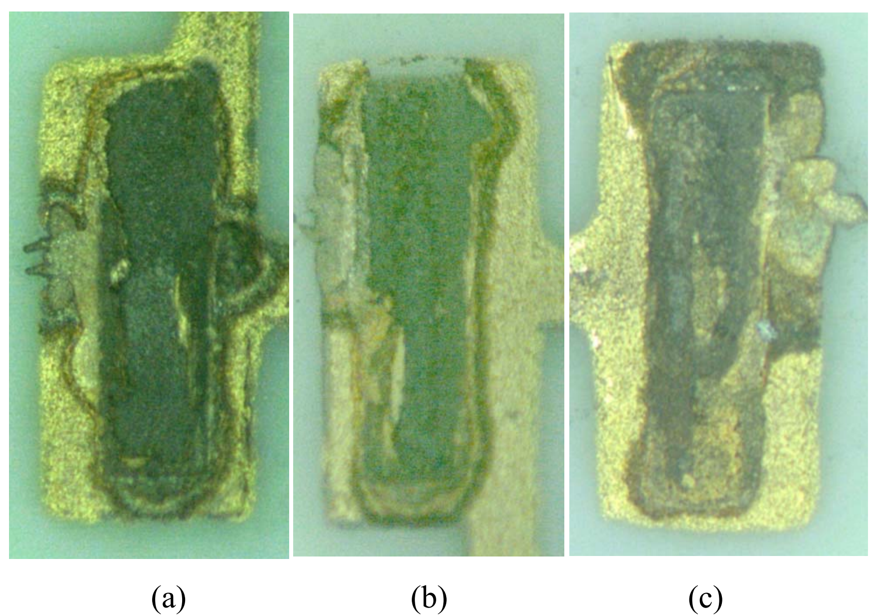


Figure 4.8 Shear Strength of Passive Component after Aging at 320°C



(a) (b) (c)

Figure 4.9 Failure Mode on the Thick Film Metallization after (a) 500 (b) 1000 (c) 2000 Hours Aging at 320°C

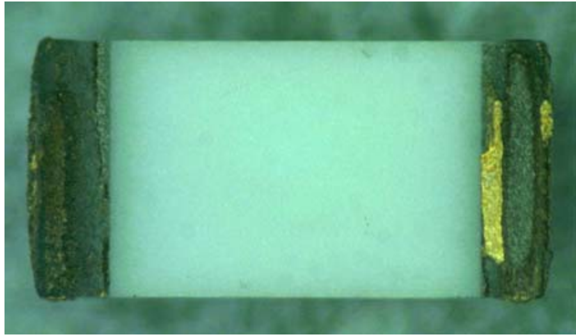
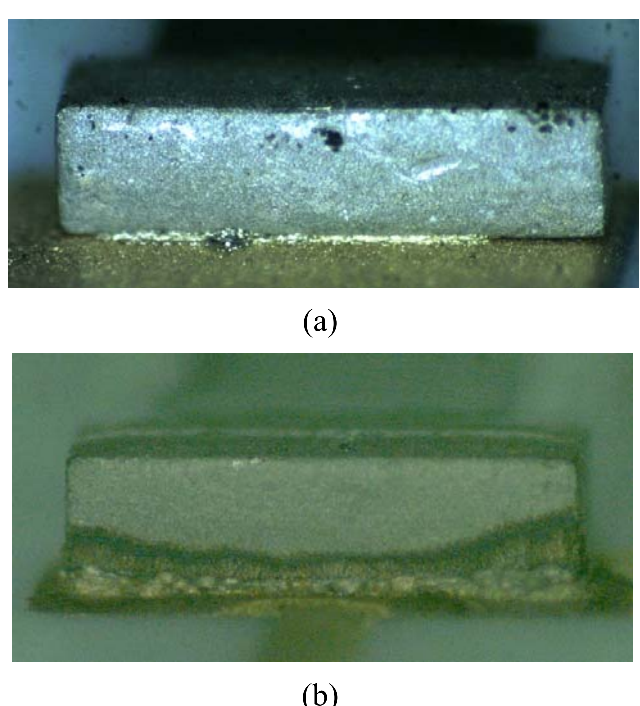


Figure 4.10 Failure Mode on Resistor after 2000 Hours Aging at 320°C

Figure 4.11 shows the solder joint on samples as built and after 2000 hours aging at 320°C, where Sn diffusion can be found from the bonding layer. This diffusion is expected and does not bring reliability issues as the shear strength was not decreasing significantly.



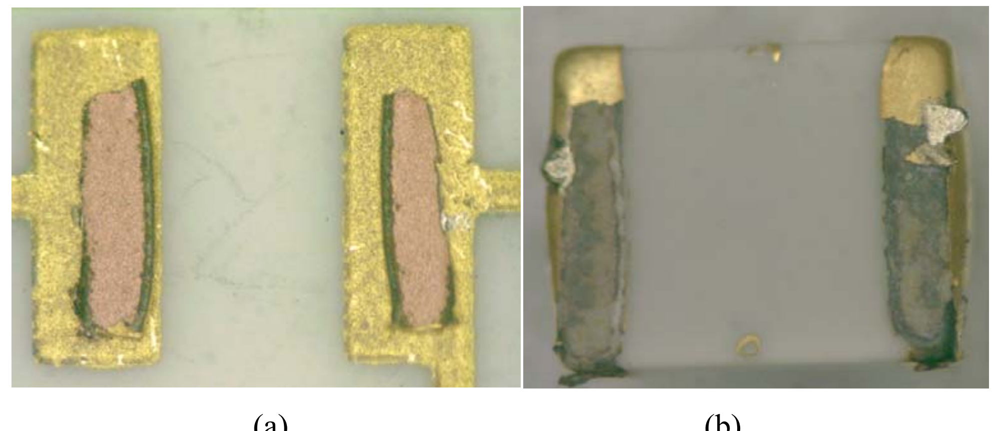
(a)

(b)

Figure 4.11 Resistor Solder Joint
(a) As Built (b) After 2000 Hours Aging at 320°C

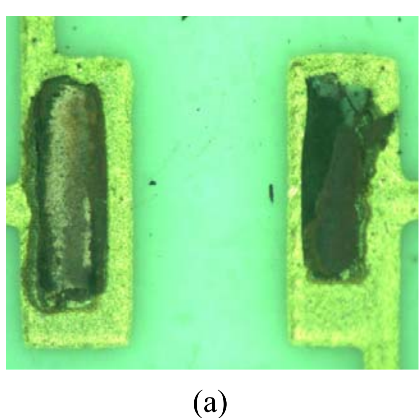
The initial average shear strength for the KEMET capacitor was 3.6kg, with failure in the termination metallization to the capacitor body, as shown in Figure 4.12. The shear

strength remained relatively constant, with the failure mode remaining the same. For shear test after 500 hours, 1000 hours and 2000 hours aging, 30% of the samples had small pieces of ceramic from the capacitor body left on the substrate after shear testing, as shown in Figure 4.13. Figure 4.14 shows the capacitor sheared after 2000 hours aging at 320°C. The multilayer ceramic was cracked during the shear test.

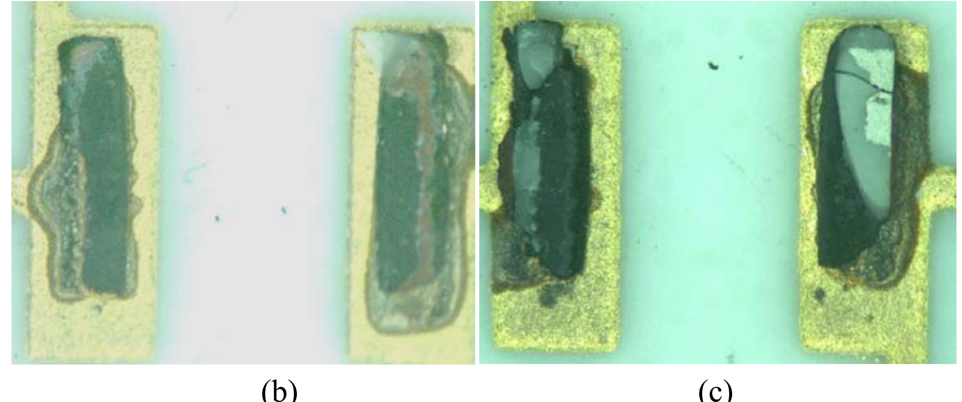


(a) (b)

Figure 4.12 Initial Failure Mode for KEMET Capacitor on (a) Thick Film Metallization (b) Capacitor Body

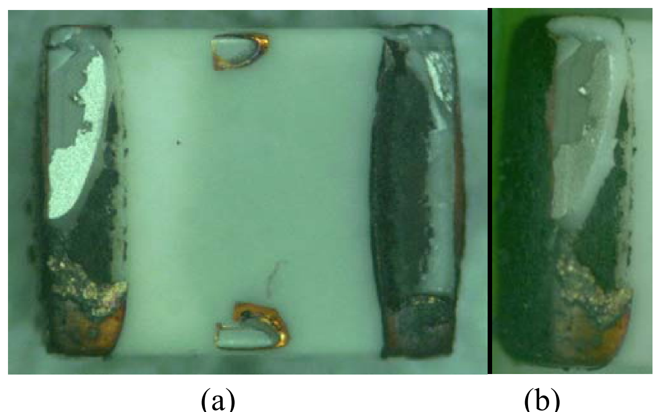


(a)



(b) (c)

Figure 4.13 KEMET Capacitor Failure Mode on the Thick Film Metallization after (a) 500 (b) 1000 (c) 2000 Hours Aging at 320°C



(a) (b)

Figure 4.14 KEMET Capacitor Sheared after 2000 Hours Aging at 320°C (a) Top View (b) Side View

4.3.3 Thermal Cycling Test

The shear strength was also recorded after 0, 100, 200, 500 and 1000 thermal cycles. The thermal cycle profile was a one hour profile with 10 minutes soak at 35°C, 20 minutes ramp to 320°C, 10 minutes soak at 320°C, followed by 20 minutes cool down from 320°C to 25°C, which is the same as described in Chapter 3, Figure 3.13.

The results are summarized in Figure 4.15. Each data point represents the average of 20 test samples. The initial average shear strength for the Mini-System resistor was 9.8kg, with failure half in the component termination metallization and half in the thick film substrate. After 100, 200, 500, and 1000 thermal cycles, the average shear strength were

10.1kg, 10.2kg, 8.8kg, and finally 8.3kg, with the same failure mode, as shown in Figure 4.16.

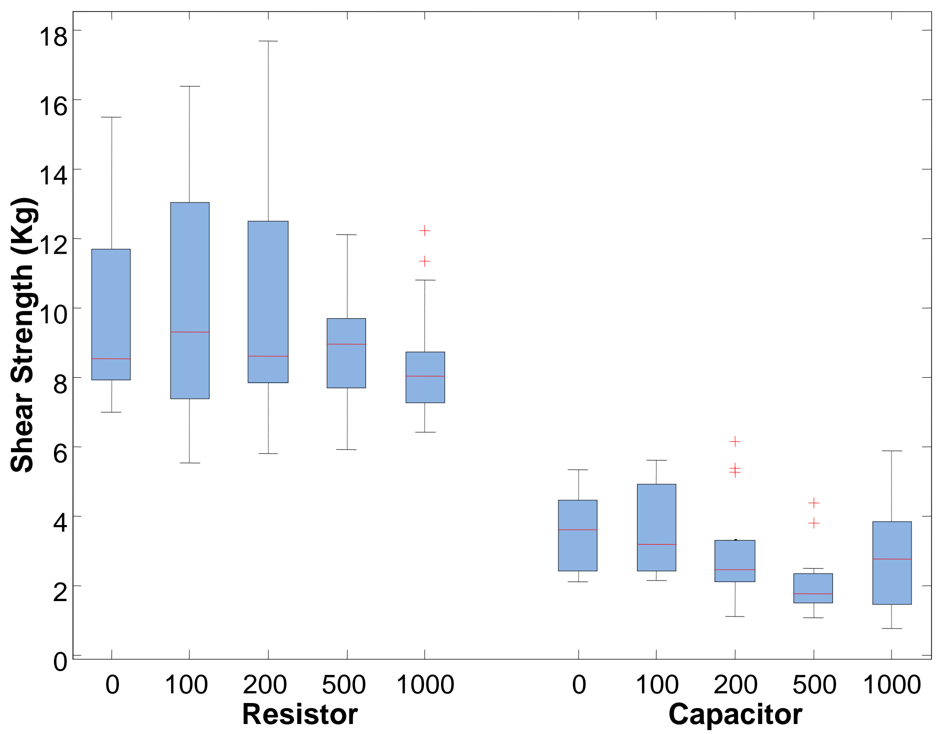
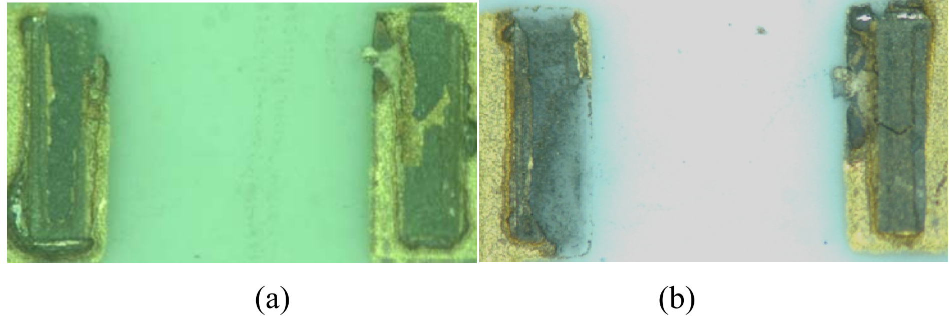


Figure 4.15 Shear Strength of Passive Component after Thermal Cycles

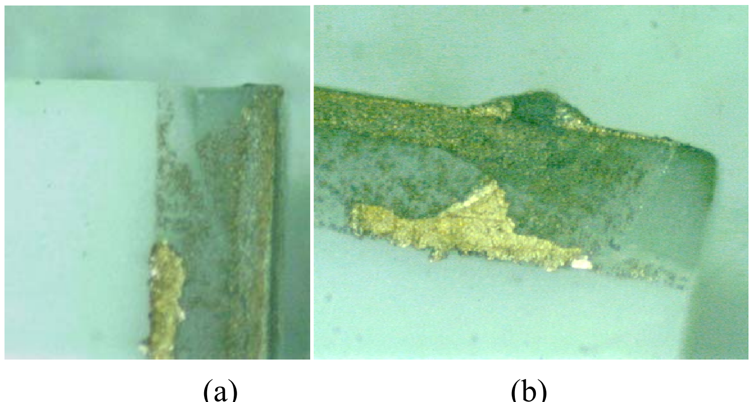


(a) (b)

Figure 4.16 Failure Mode on the Thick Film Metallization after (a) 200 (b) 1000 Thermal Cycles

For shear test after 500 thermal cycles, half of the samples had small pieces of ceramic cracked at the component corner after shear test, as shown in Figure 4.17. For shear test after 1000 thermal cycles, the number of samples that had small pieces of

ceramic cracked remained the same, but the cracking area was increased. Large ceramic pieces were found cracked from the resistor body, as shown in Figure 4.18.



(a) (b)

Figure 4.17 Mini-System Resistor Sheared after 500 Thermal Cycles
(a) Sample 1 (b) Sample 2

Figure 4.18 Mini-System Resistor Sheared after 1000 Thermal Cycles

The initial average shear strength for the KEMET capacitor was 3.6kg, with failure in the termination metallization to capacitor body After 100, 200, 500, and 1000 thermal cycles, the average shear strength were 3.6kg, 3.0kg, 3.2kg, and finally 2.8kg, with the same failure mode, as shown in Figure 4.19, Figure 4.20, and Figure 4.21. For shear tests after 500 and 1000 thermal cycles, 25% of the samples had small pieces of ceramic left on the substrate after shear testing.

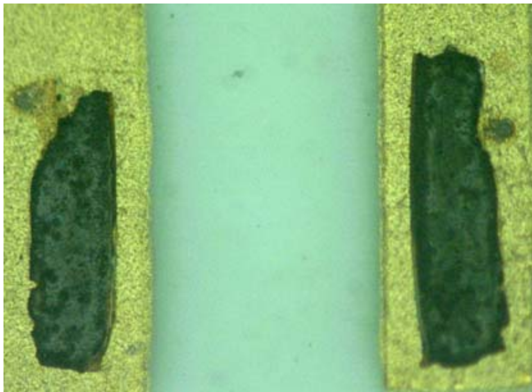


Figure 4.19 Failure Mode on the Thick Film Metallization after 100 cycles

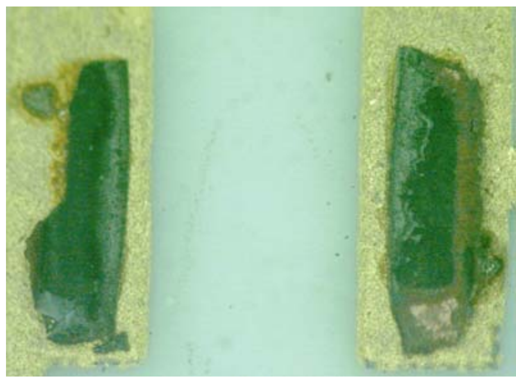


Figure 4.20 Failure Mode on the Thick Film Metallization after 500 cycles

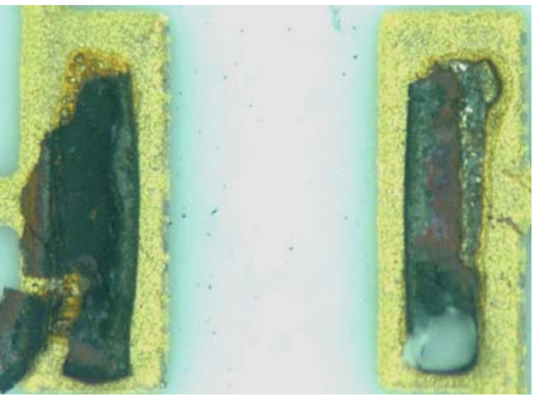


Figure 4.21 Failure Mode on the Thick Film Metallization after 1000 cycles

4.4 External Lead Attach

4.4.1 Background

A high temperature electronic device needs to be connected with other devices to

transfer signals, data, and power. Traditional connectors made with Nylon, Polyester, or Thermoplastic cannot work at 300°C. Wire welding was considered instead of using a connector. Molybdenum (Moly) tabs were selected as the wire attachment points. The ability of molybdenum to withstand extreme temperatures without significantly expanding or softening makes it useful in wire welding. Previous research at Auburn University used Moly tab as a CTE buffer between SiC die and copper foil [53]. The Moly tabs were purchased from Williams Advanced Materials (now Materion), with 0.5 mil gold plating over nickel plated Moly. The Moly tabs are 140mil by 140mil square, with 20 mil thickness.

4.4.2 Moly Tab Attach

A test vehicle for external lead (wire) attachment experiments was designed with Moly tabs to serve as the lead attachment points. The substrate was fabricated with C109 thick film conductor. In the Moly tab attach area, DuPont 5063 was printed and fired over the previous printed/fired C109. This was the same as the die attach pad structure previously described. The Moly tabs were attached with eutectic AuSn preform (80wt.%Au/20wt.%Sn). The preform was cut to about 30% of the Moly tab area to control the Sn involved. The configuration and substrate with Moly tabs is shown in Figures 4.22 and 4.23.

A thermal compression profile was developed on the FC150 Flip Chip bonder. The bonding profile used 5kg forces with 4 minutes at 360°C followed by 2 minutes soak at 280°C.

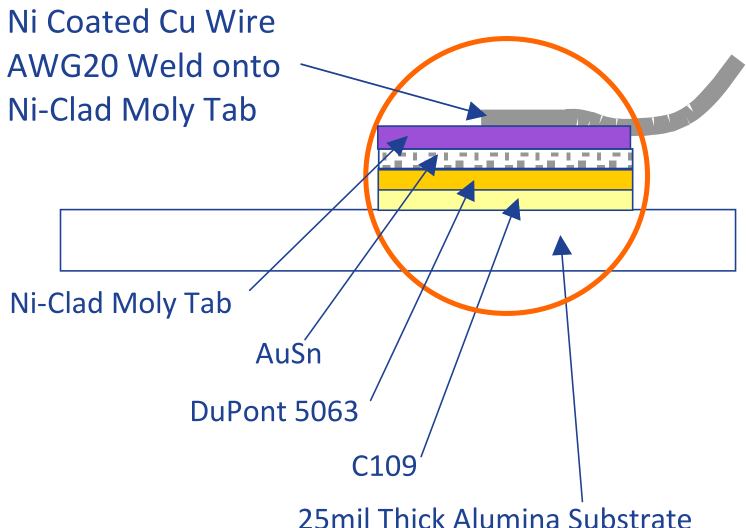


Figure 4.22 Configuration of Wire Welding Substrate

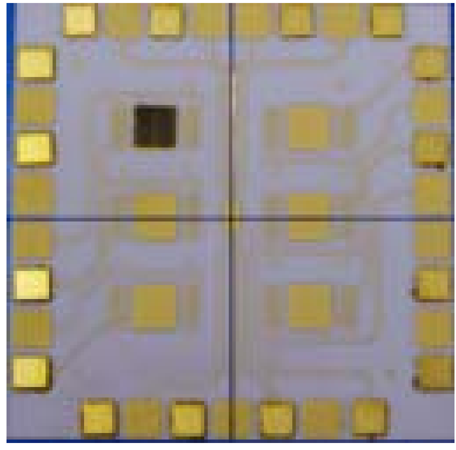


Figure 4.23 Wire Welding Substrates with Peripheral Moly Tabs Attached

4.4.3 External Lead Attach

Before attaching wires to the Moly tab on ceramic substrate, the wire to standalone Moly tab attachment process was evaluated using laser welding and ultrasonic welding. The laser welding attempts used a 1064um fiber laser system at the GE Research Center. The AWG20 nickel-coated-copper wire balling and wire-to-tab attaching process were tested by adjusting process parameters, including power, time, and focal position. The detailed test result was presented in the publication [21].

The ultrasonic welding was performed by Stapla Ultrasonics Corporation. AWG20 nickel-copper wire was attached to the moly tab that was mounted on the substrates. The wire could be bonded to the Moly tabs, but the substrates cracked during the process. Stiffness of the nickel and ultrasonic energy dissipated between the strands during bonding were identified as the two potential causes for the substrate cracking. Work is continuing at GE Global Research Center to explore the availability of single solid nickel coated copper wire, stainless steel wire and platinum wire.

4.5 Summary

The resistor from Mini-System and capacitor from KEMET were selected for reliability test and showed good mechanical strength with the thick film metallization. The shear strength remained high after 2000 hours storage at 320°C and 1000 thermal cycles from 25°C to 320°C, with the failure mode unchanged. Moly tabs were selected as the wire welding attachment points and welding process has been developed. Amplifier modules were built with those passive components.

CHAPTER 5 HIGH TEMPERATURE ELECTRONICS PACKAGING

5.1 Single Chip DIP Packaging

Before building the amplifier module, functional die need to be attached, wirebonded, and tested at 300°C. A 16-pin ceramic DIP package was selected for this purpose, as shown in Figure 5.1.

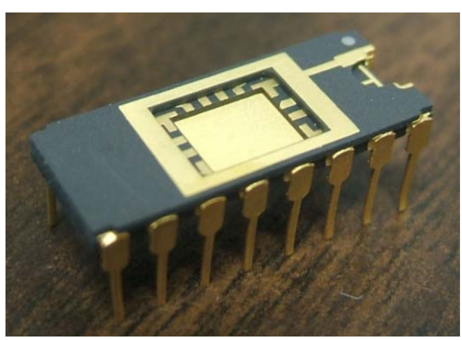


Figure 5.1 16-Pin Ceramic DIP Package

This DIP package was intended for conventional temperature range applications. To be compatible with the AuSn die attach process at high temperature, a thick Au layer on the cavity was electroplated using gold solution HS 434, supplied by Technic Inc. In the plating process, a platinum mesh was used as the anode with the electrolyte solution acting as the source of gold. The pin that connected to the cavity Au layer was connected through a multi-meter to the power supply. Thus only the cavity area was plated with Au. The current during plating was carefully monitored to ensure a smooth and accurate plating of Au.

A graphite fixture was designed to hold the DIP package in the SST 3150 vacuum

furnace and to support a deadweight on the chip. The profile was the same as used in the die attach process, with 3.5 minutes at 350°C followed by 30 minutes soak at 280°C. A weight of 500 grams was applied to the die using a special designed collet to apply the bonding force to the perimeter of the die rather than the die surface to prevent damage to the active die area. To control the Sn involved in the die attach process, the preform was cut to about 30% of the die area. Figure 5.2 shows an X-Ray photo of an attached amplifier, with no voids found in the solder joint. After die attach, wirebonding was used to make electrical connections from the chip pads to the DIP pads. The assembled amplifier is shown in Figure 5.3. The assembled amplifiers were sent to GE Global Research and tested functional at 300°C.

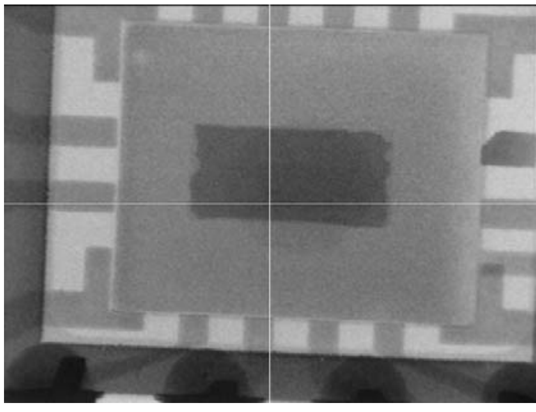


Figure 5.2 X-Ray on Amplifier Attached to DIP Package

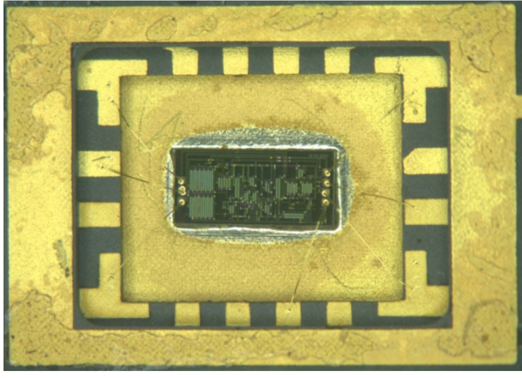


Figure 5.3 Amplifier Attached and Wirebonded to DIP Package

5.2 Amplifier Module

A circuit pattern for the thick film ceramic substrate was designed based on the circuit schematic developed by GE Global Research Center. Since this down hole application has a width limitation of 1 inch, the substrate size was selected to be 1 by 4 inches. The designed test board is shown in Figure 5.4. The substrate fabrication and devices assembly process will be discussed in the following sections.

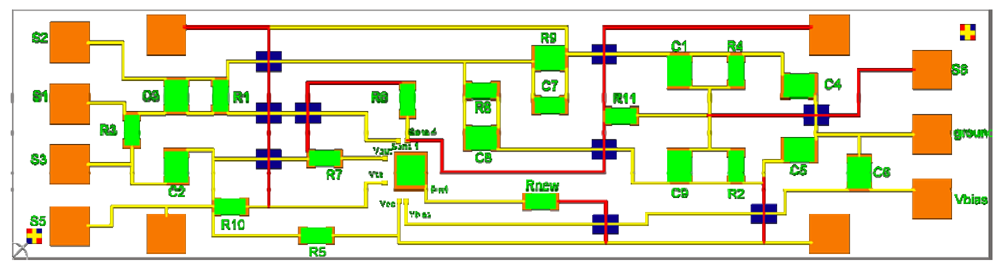


Figure 5.4 Designed Amplifier Test Board

5.2.1 Substrate Fabrication

The substrate metallization used the thick film conductor C101, C109, DuPont 5063, and dielectric D1, since their properties proved reliable at 300°C, as described in Chapter 2 and Chapter 3.

The bottom interconnect layer used thick film conductor C101. C101 has been proved to have good wirebondability with Au wire. This Au based conductor also has lower resistivity than thick film conductor C109, which is AuPt based. C101 was used for wirebonding pad and interconnect. A firing profile with a 980°C peak temperature was used to promote the adhesion of the C101 to the ceramic.

Two dielectric layers with dielectric paste D1were sequentially printed, dried, and fired to eliminate pinholes. A firing profile with 980°C peak temperature was used.

The third layer also used thick film conductor C101, to provide interconnects over

the dielectric. A firing profile with 980°C peak temperature was used here to promote the adhesion of C101 to the dielectric and ceramic.

The fourth layer used thick film conductor C109 for die and passive component attach pads. A firing profile with 850°C peak temperature was used.

The last layer was the pad thickness addition layer with DuPont 5063 Gold conductor. This layer increases the Au thickness on the die and passive component pads for the liquid transient phase bonding process with the AuSn preform.

This process is illustrated in Figure 5.5 and the fabricated substrate is shown in Figure 5.6. The larger pads around the substrate perimeter are for the Moly tab attach and the center pad is for SiC die attach. The blue box is the dielectric layer providing insulation for cross-over interconnects.

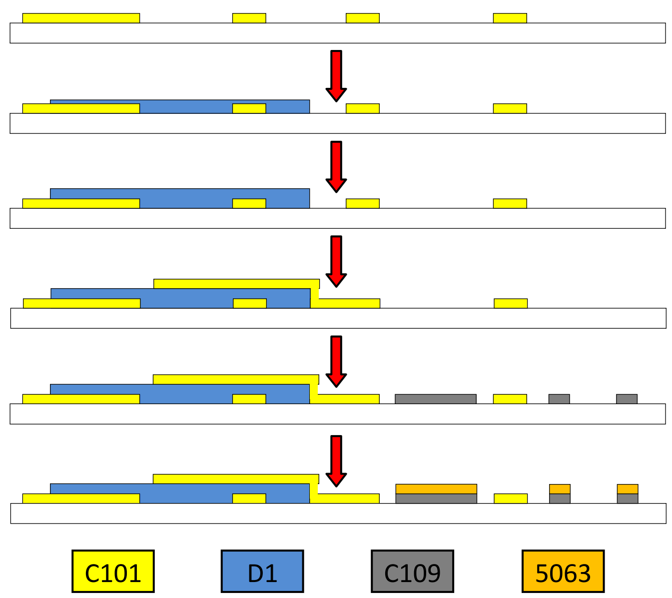


Figure 5.5 Substrate Fabrication Process

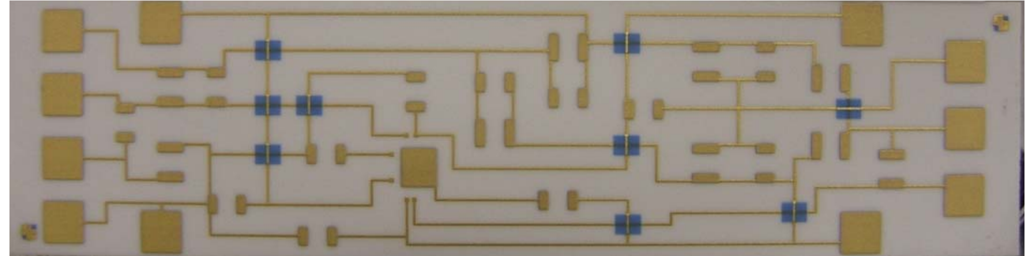


Figure 5.6 Fabricated Substrate

5.2.2 Passive Components Attach

AuSn (80wt.%Au/20wt.%Sn) preforms were used for passive component attach. The FC150 Flip Chip bonder was used to provide a thermal compression profile. Moly tabs were attached to the substrate first. The bonding profile used 5kg force with 4 minutes at 360°C followed by 2 minutes soak at 280°C. Here only a short soak time was required at 280°C since the subsequent die attach process had a 30 minutes soak at 280°C.

Resistors were attached before capacitors since resistors have a lower profile. The profile used was 4 minutes at 360°C followed by 2 minutes soak at 280°C, with 1.5kg force applied on the resistors and 1kg force applied on capacitors. Figure 5.7 illustrated the process of resistor attachment.

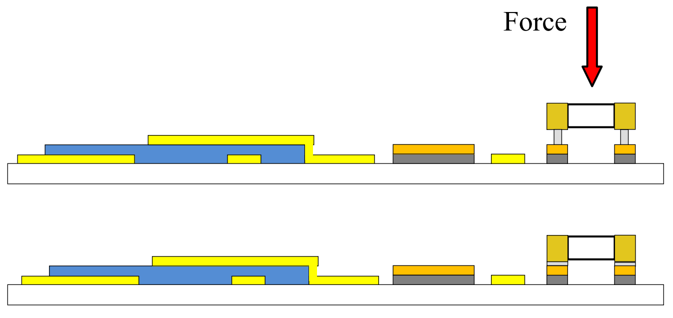


Figure 5.7 Resistor Attachment Process

5.2.3 Die Attach and Wire Bonding

A graphite fixture was designed to hold the 1 by 4 inch substrate in the SST 3150 vacuum furnace and to support the deadweight on the die. A weight of 500 grams was

applied to the die using a special designed collet to apply the bonding force to the perimeter of the die rather than the die surface to prevent damage to the active die area. The die attach pad was designed for a die size of 3.2 mm by 2.9 mm, but only half part of the designed die was used in this system. The actual die size was about 3.2 mm by 1.5 mm and the AuSn preform was cut to 2.0 mm by 0.7 mm to control the amount of Sn available. After die attach, 1 mil gold wire was used to wirebond the die to the substrate. The die attach and wirebonding process is shown in Figure 5.8.

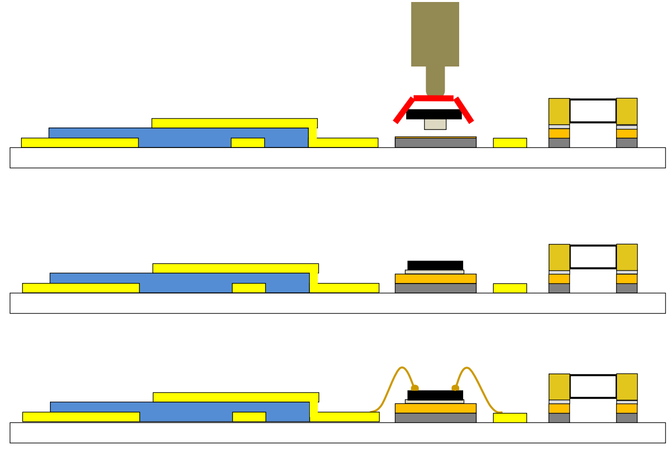


Figure 5.8 Die Attach and Wirebonding Process

5.2.4 Amplifier Testing

The assembled board is shown in Figure 5.9. The assembled amplifiers were sent to GE Global Research and tested functional at 300°C.

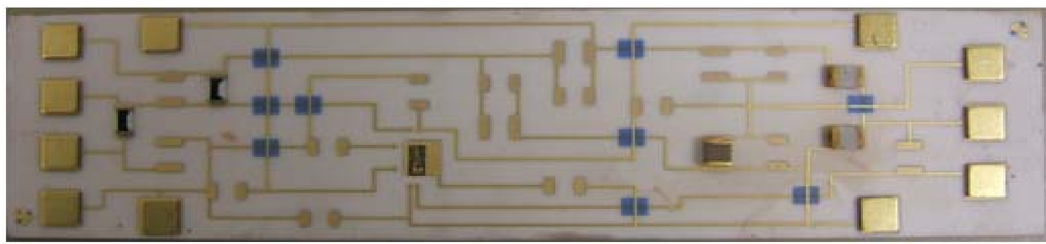


Figure 5.9 Assembled Test Board

CHAPTER 6 CONCLUSION AND FUTURE WORK RECOMMENDATION

6.1 Thick Film Technology for 300°C Applications

Thick film technology for fabrication of multichip modules capable of 300°C operation was explored. A thick film conductor and dielectric with corresponding processing conditions had been identified for 300°C applications. The selected thick film combination showed excellent adhesion after 2000 hours aging at 320°C. The electrical properties of the dielectric were acceptable at 300°C and stable as a function of high temperature exposure. Compatible thick film metallurgy for die attach had also been demonstrated.

6.2 Packaging for High Temperature SiC Based Devices

Die attach and wirebonding that can withstand operation temperature up to 300°C had been demonstrated with SiC die on thick film metalized Al_2O_3 substrates. Liquid phase transient bonding process using limited volume eutectic AuSn preform was developed. The die shear strength after 2000 hours storage at 320°C remained high. Au wire bonding on different SiC die metallization was explored and one metallization stack showed good results after 1500 hours aging at 320°C.

6.3 Passive Components for 300°C Applications

The resistor from Mini-System and capacitor from KEMET were identified for this high temperature application. Eutectic AuSn preform was used to attach passive components. Reliability testing showed good mechanical strength after 2000 hours

storage at 320°C and 1000 thermal cycles from 25°C to 320°C. Moly tabs were selected as the wire welding attachment points and a welding process has been developed.

6.4 Recommendations for Future Work

Based on the results presented in this dissertation, some recommendations for future work are as follows:

- Decreasing leakage current and discoloration on dielectric were found in biased aging test. The exact reason is unclear and needs further investigation. This discoloration may hurt the adhesion of metal on dielectric and more investigation is needed.

- For high temperature SiC die attach process, other die attach material could be considered rather than AuSn preform. Paste is preferred for assembling multiple chips and passive components. The current method has a tight limit on the volume of Sn involved and thus doesn't allow the use of AuSn paste.

REFERENCES

1. F. P. McCluskey, R. Grzybowsky, and T. Podlesak, “High Temperature Electronics”, CRC-Press, February 1, 1997

2. E. Savrun, “Packaging considerations for very high temperature Microsystems”, Proceedings of IEEE Sensors, 2002, vol.2, pp 1139 - 1143.

3. R. Kirschman, “High Temperature Electonics”, Wiley-IEEE Press, August 18, 1998.

4. R. Normann, “First High-Temperature Electronis Products Survey 2005”, Sandia National Laboratories.

5. D. Duchane, and D.Brown, “Hot Dry Rock (HDR) Geothermal Energy Research and Development at Fenton Hill, New Mexico", Geo-Heat Centre Quarterly Bulletin 23 (4): 13–19, ISSN 0276-1084

6. U.S. Department of Energy, Geothermal Technologies Program, “An Evaluation of Enhanced Geothermal Systems Technology”, 2008

7. Massachusetts Institute of Technology , “The Future of Geothermal Energy: Impact of Enhanced Geothermal Systems (EGS) on the United States in the 21st Century”, 2006.

8. US Department of Energy, “Geothermal Technologies Program Fact Sheet”.

9. R. Ásmundsson, R. Normann, H. Lubotzki,and B. Livesay, “High Temperature Downhole Tools-Recommendations for Enhanced and Supercritical Geothermal Systems”, IPGT High Temperature Tools Working Group, January 2011.

10. J. B. Casady and R. W. Johnson, “Status of silicon carbide (SiC) as a wide-bandgap semiconductor for high-temperature applications: A review”, Solid-State Electronics Vol.39, pp. 1409-1422, 1996

11. P. L. Dreike, D. M. Fleetwood, D. B. King, D.C. Sprauer, and T.E. Zipperian, “An overview of high-temperature electronic device technologies and potential applications”, IEEE Transactions on Components, Packaging, and Manufacturing Technology, Part A, Vol 17: 594-609, December 1994.

12. J. Camassel, S. Contreras, and J.-L. Robert, “SiC materials: a semiconductor family for the next century”, Comptes Rendus de l'Acade´mie des Sciences - Series IV - Physics 1: 5-21, 2000.

13. M. R. Werner, and W. R. Fahrner, "Review on materials, microsensors, systems and devices for high-temperature and harsh-environment applications", IEEE Transactions on Industrial Electronics, Vol 48, pp. 249-257,2001

14. G.W. Hunter, P.G. Neudeck, G.C. Fralick et al, "SiC-Based Gas Sensors Development", Proceedings of International Conference on SiC and Related Materials. Raleigh, North Carolina, Oct. 10-15, 1999.

15. P. G. Neudeck, G. M. Beheim, and C. Salupo, "600°C Logic Gates Using Silicon Carbide JFET's", 2000 Government Microcircuit Applications Conference,March 20-23, Anaheim, CA

16. http://www.cree.com/products/sic_sub_prop.asp "SiC Physical & Electronic Properties"

17. P .G. Neudeck, "Silicon Carbide Electronic Devices", Encyclopedia of Materials: Science and Technology, pp. 8508-8519

18. M. L. Topfer, "Thick-Film Microelectronic Fabrication Design and Application", Van Nostrand Reinhold, New York, 1971

19. R.W. Johnson, "Hybrid Microelectronics Handbook", Chapter 1, McGraw-Hill, 1995

20. R.W. Johnson, C. Wang, Y.Liu, and J.D.Scofield, "Power Device Packaging Technologies for Extreme Enviroments", IEEE Transactions on Electronics Packaging Manufacturing, Vol.30, No.3, July 2007, pp. 182-191

21. Wire Bonding http://extra.ivf.se/ngl/A-WireBonding/ChapterA1.htm#A1.1

22. L. Coppola, D. Huff, F. Wang, R. Burgos, and D. Boroyevich, "Survey on High-Temperature Packaging Materials for SiC-Based Power Electronics Modules", IEEE Power Electronics Specialists Conference, 2007.

23. D. Shaddock, V. Tilak, T. Zhang, R. Zhang, and R.W. Johnson, "Reliability Assessment of Passives for 300°C using HALT", International Conference on High Temperature Electronics (HiTEC 2010), May 11-13, 2010, Albuquerque, NM.

24. S. Kasap, and P. Capper, "Springer Handbook of Electronic and Photonic Materials", Springer, October 19, 2006

25. J.Savage, "Handbook of Thick Film Technology", Chap 3, Electrochemical Publications Ltd., Ayr, Scotland, 1976

26. D.L.Hankey, A.S Shaikh, S.Vasudevan, and C.S. Khadilkar, "Hybrid Microelectronics Handbook", Chapter 3, McGraw-Hill, 1995

27. J.C.Fu, “ A Study of Structure of Gold-Platinum in Thick Film Conductors,” Precious Metal, E.D.Zysk and J.A.Bonucci (eds.), pp.469-483, 1985

28. J. S. Salmon, R. W. Johnson, and M. Palmer, “Thick Film Hybrid Packaging Techniques for 500°C Operation,” Proceedings of 4th International High Temperature Electronics Conference, held in Albuquerque, NM, June 1998

29. http://www.coorstek.com/

30. R.W. Johnson, “Hybrid Materials, Assembly, and Packaging”, High Temperature Electonics, Wiley-IEEE Press, August 18, 1998.

31. P.Zheng, P.Henson, R.W. Johnson, and L.Chen, “Metallurgy for SiC Die Attach for Operation at 500°C”, International Conference on High Temperature Electronics (HiTEC 2010), May 11-13, 2010, Albuquerque, NM.

32. P.Zheng, A. Wiggins, and R.W. Johnson, “Die Attach for High Temperature Electronics Packaging”,International Conference on High Temperature Electronics (HiTEC 2008),Albuquerque, New Mexico USA May 12-15, 2008

33. J.S.Shor, R.A.Weber, L.G.Provost, D.Goldstein, and A.D.Kurtz, “High temperature ohmic contacts for n-type β–SiC sensors”, Wide Band Gap Semiconductors Symposium, Boston, Massachusetts, 2-6 Dec. 1991

34. S.Liu, K.Reinhardt, J.Scofield, and C.Severt, “High temperature Ni/Cr/W ohmic contact metallization on n-type SiC semiconductor”, Proc.-Workshop on High Te,perature Power Electronics for Vehicles, Fort Monmouth, New Jersey, 26-27 Apt. 1995, pp85-87

35 S.Liu, K.Reinhardt, C.Severt, and J.Scofield, “Thermally stable ohmic contacts on n-type 6H- and 4H-SiC based on silicide and carbide”, Proc. 6th International Conference-Silicon Carbide and Related Materials 1995, Kyoto, Japan, 18-21 Sept.1995

36. F.P. McCluskey, L. Condra, T. Torri, and J. Fink, “Packaging Reliability for High Temperature Electronics: A Materials Focus”, Microelectronics International, No. 41, pp. 23-26, September 1996.

37. “Eutectic Wafer Bonding for Hermetic Seals”, http://www.flipchips.com/tutorial92.html

38. M.J. Palmer and R.W.Johnson, “Thick Film Modules for 300°C Applications,” Proceedings of the International High Temperature Electronics Conference, Santa Fe, NM, May 16-18, 2006, pp. 118-124.

39. W.F.Gale, V.G.Krishnardula, R.Love, N.Sofyan, and R.Aluru, "Transient Liquid

Phase Bonding of Ferritic Oxide Dispersion Strengthened Alloys", Final Report, June 26, 2006

40. R.Venkatraman, J.R.Wilcox and S.R.Cain, "Experimental study of the kinetics of transient liquid phase solidification reaction in electroplated gold-tin layers on copper", Metallurgical and Materials Transactions A,Volume 28, Number 3, 699-706,

41. P.Zheng, “High Temperature Electronics Packaging Processes and Materials Development”, Ph.D dissertation, Auburn University, AL.

42. ASM International, “ASM Metals HandBook Volume 3 - Alloy Phase Diagrams”, 1992

43 Department of Defense Test Method Standard: Microcircuits. MIL-STD-883H, METHOD 2019.8 DIE SHEAR STRENGTH

44. V. Dixit, H.Davis, and M.Clark, “Wire Bonding Considerations”, Advanced Packaging, 2006

45. http://www.me.ccu.edu.tw/labs/mtlab/MtLab_Hp/

46. R.K.Kirschman, “Passive Components,” High Temperature Electonics, Wiley-IEEE Press, August 18, 1998.

47. J.E.Naefe, R.W. Johnson, and R.R.Grzybowski, “High-Temperature Storage and Thermal Cycling Studies of Thick Film and Wirewound Resistors,” IEEE Transactions on Components and Packaging Technology, Vol. 25, No. 1, March 2002, pp. 45-52.

48. Document Number 91000, http://www.vishay.com

49. http://www.Mini-SystemsInc.com

50. http://www.trstechnologies.com

51. http://www.kemet.com

52. D. Shaddock, V. Tilak, and T. Zhang, “Reliability Assessment of Passives for 300°C and 350°C”, International Conference and Exhibition on High Temperature Electronics Network (HiTEN), July 18-20, 2011, Oxford, United Kingdom

53 V. Bondarenko , P. Martin , M. S. Mazzola , R. Kelley , J. Casady , C. Wang , Y. L. S. Gale and R. W. Johnson, "Characterization and packaging of SiC JFET power modules for extreme environmant motor drives", Proc. 2006 Int. High Temp. Electron. Conf., p.488, 2006.