Architecture Analysis and Block Design in Modern Communication Radio Transceivers

by

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Abstract

With the rapid growth of consumer electronics market and the increasing demand for low power, wide bandwidth communication devices, the RF transceiver on chip implemented utilizing modern CMOS or SiGe BiCMOS technology achieves wide applications. Therefore it has been attracting attention in academia. This dissertation will present the research on transceiver architecture, and the design implementations of independent building blocks.

First the performance degradation of Multiple-Input-Multiple-Output (MIMO) communication systems is analyzed which is due to MIMO wireless transceiver radio frequency integrated circuits (RFIC) imperfections. The effects of signal coupling in RF front-end, frequency synthesizer phase noise and the gain imbalance between different radio paths are investigated. These issues are explored by analytical derivations and results are verified by Monte-Carlo simulations. The analytical model achieves good agreement with the simulation results. The conclusion can serve as a useful reference for MIMO RFIC designers. Then a comprehensive radar transceiver architecture with stretch processing is presented. The radar system on chip (RoC) is a promising topic. RoC with stretch processing was rarely implemented before. The dissertation demonstrates the detail of a practical transceiver. In additional, a power amplifier (PA) driver operating at 10GHz is designed and introduced as a critical block to the whole system. The PA driver delivers +5dBm power and 10dB power gain.

A power-saving RF front-end is indispensible to the radio receiver. This dissertation presents a novel RF receiver front-end using only one shared tail current for low power application. The 5GHz receiver front-end RFIC includes a voltage controlled oscillator (VCO), a double balanced

mixer and a low noise amplifier (LNA) in a cascoded topology. The receiver RFIC was implemented in a 0.5um SiGe BiCMOS technology. The VCO phase noise was measured around -105dBc/Hz at 1MHz frequency offset. Intermediate frequency (IF) output is centered at frequency of 600MHz using a low-IF architecture and the conversion gain is measured more than 15dB. The front-end core consumes 3.3mA current from a 3.3V power supply and occupies 1.4mm^2 area.

Harmonic rejection is an important characteristic for the systems in strong interference environment. Due to the time-variant property of mixers, the out-of-band interference will be folded back to in-band by the virtue of high order harmonics. This dissertation presents a novel mixer architecture suppressing 3rd and 5th order harmonics more than 30dB lower. Meanwhile it achieves higher dynamic range with affordable noise figure (NF).

Finally a wideband digitally controlled oscillator (DCO) for all digital phase-locked loop (ADPLL) application is presented in this dissertation. The DCO has an 8th order resonator composed of coupled inductors and MOS varactors. By the inductor coupling, the tuning range contains four bands and is extended from 1.4GHz to 3.86GHz. The power consumption for the DCO core is 6.5mW with a 1.5V power supply. The measured phase noise at 1MHz frequency offset from 3GHz output is around −110dBc/Hz.

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Chapter 1 Introduction

1.1 Motivation

The ever-increasing demand of the wideband communication market leads to application of innovative technologies, such as multiple-input-multiple-output (MIMO), orthogonal frequency division multiplexing (OFDM), beamforming, etc. Meanwhile the advance in semiconductor fabrication technique makes the realization of these technologies feasible and cost effective. Therefore more and more new standards including the new technologies are proposed to address the high speed, low cost and low power communication market, e.g., WiFi (IEEE802.11a/b/g/n), WiMAX, Bluetooth, WiGig, LTE. Both academic and industry have been focusing more effort on designs of high speed transceiver [1-6]. Despite the numerous implementations, there are still questions and challengers when one strives for higher reliability, lower cost and lower energy. MIMO transceiver integrates multiple RF chains into one single chip, hence it unavoidably meets the problem of mutual coupling and mismatch. How these impairments influence the system specification is an open question. In this thesis, this question will be addressed.

Radar system is still attracting attention though it has been a long time since radar was invented in World War II. The modern trend of radar system design requires high level of integration attributed to advanced and economic IC technology [7-11]. The traditional radar usually occupying large area is being replaced with radar on chip (RoC), even phase array radar has been integrated. Radar transceiver with stretch processing technique was proposed for a while but remains few employed in IC implementation. This thesis proposes an X band radar transceiver IC with stretch processing.

In additional to system design and analysis, building blocks are also critical for successful implementation. With the IC technology scales down to sub-micron meter range, the operation voltage scales down respectively. New design challengers such as linearity and distortion become more apparent. Lower power consumption is the crucial factor of commercial consumer electronics product because more battery powered applications come into market. Reducing area and cost of transceiver IC and maintaining wideband operation is the requirement of multi-mode devices. Innovative designs for important RF blocks, e.g., RF front-end, mixer and oscillator are included in this thesis as an effort to solve the above modern IC design challengers.

1.2 Dissertation organization

This dissertation is organized as following:

Chapter 2 addresses the performance degradation of Multiple-Input-Multiple-Output (MIMO) communication systems due to MIMO wireless transceiver radio frequency integrated circuits (RFIC) imperfections. The effects of signal coupling in RF front-end, frequency synthesizer phase noise and the gain imbalance between different radio paths are investigated. These issues are explored by analytical derivations and results are verified by Monte-Carlo simulations. The analytical model achieves good agreement with the simulation results. The conclusion can serve as a useful reference for MIMO RFIC designers.

Chapter 3 proposes and analyzes a X band UAV radar with stretch processing technique. The basic ideas of radar system are introduced. Stretch processing technique is analyzed and the corresponding specifications are derived. A PA driver at 10GHz operation frequency is designed as a part of radar transceiver, which is able to deliver 5dBm output power.

Chapter 4 presents a novel LNA-Mixer-VCO (LMV) cell front-end which addresses the low power RFIC requirement. The receiver RFIC was implemented in a 0.5um SiGe BiCMOS

technology. The VCO oscillation frequency is around 5GHz, targeting at the WLAN 802.11a application. Intermediate frequency (IF) output is centered at frequency of 600MHz using a low-IF architecture and the conversion gain is measured more than 15dB. The 1dB gain compression point and sensitivity of the front-end is measured greater than -14dBm and smaller than -60dBm respectively. The front-end core consumes 3.3mA current from a 3.3V power supply and occupies 1.4mm^2 area.

Chapter 5 presents a harmonic rejection mixer (HRM) which eliminating the higher order harmonic distortion. The HRM was fabricated in 0.13um CMOS technology and consumes negligible power consumption because it is a passive mixer basically. The 3rd and 5th order harmonics are attenuated more than 30dB. Meanwhile in-band P1dB is higher than 12dBm. The HRM can operate up to 1GHz frequency and serves a good candidate in low power and high linear applications.

Chapter 6 demonstrates a digital controlled oscillator (DCO) with coupled inductors layout. The DCO has an 8th order resonator composed of coupled inductors and MOS varactors. The tuning range contains four bands and covers from 1.4GHz to 3.86GHz. The DCO radio frequency integrated circuit (RFIC) was implemented in 0.13μm CMOS technology and occupies an area of 0.75x0.75 mm^2 including output buffer and bias circuitry. The power consumption for the DCO core is 6.5mW with a 1.5V power supply. The measured phase noise at 1MHz frequency offset from 3GHz output is around −110dBc/Hz.

Chapter 7 will draw the conclusion and propose the future research directions.

Chapter 2 Impact of Transceiver RFIC Impairments on MIMO System Performance

2.1 Introduction

Traditional wireless communication transceiver employs a single transmitter antenna and a single receiver antenna to form a single-input-single-output (SISO) system. However SISO system cannot meet the ever-increasing demanding of high data rate and reliability in future wireless communication systems. In recent years, digital communication systems using multiple-input-multiple-output (MIMO) have been developed to achieve better performance without additional costs of bandwidth and transmission power. This technology has been rapidly adopted by modern commercial communication standards such as wireless local area network (WLAN) standard IEEE802.11n and beyond third generation (B3G) mobile communication systems. The underlying principle of MIMO is to exploit the rich spatial dimensions and turn the multiple-path wireless link into two types of benefits: diversity gain or throughput increase. According to [12][13], these two benefits actually can be traded off to make MIMO flexible enough to fit into different communication standards. With the advance of MIMO technique, the MIMO transceiver RFIC design has been attracting more attentions recently [2-4][14-16]. Ref [14] demonstrated the first RFIC implementation for a 2×2 MIMO WLAN system. Despite the fast development of MIMO systems, there is a big gap between MIMO theory and its practical RFIC implementation. In the design given in [14], two duplicate RF receivers were integrated into a single chip that results in new challenges for RFIC designs such as inter-chain coupling and gain imbalance, which never exists in SISO RFICs. In [17] the receiver inter-chain coupling effect on space-timeblock code (STBC) MIMO system performance was analyzed. But it did not analyze

the transmitter side coupling, which contributes to the major part of signal coupling in a MIMO RFIC due to the on-chip power amplifier (PA). Compared to transmitter circuits, receiver circuits normally generate much less coupling energy. Gain imbalance among different RF paths is another concern that could greatly affect the MIMO system performance and has not been fully investigated so far. Similar to the SISO system, the phase noise of the frequency synthesizer directly affects system performance. But so far there are only numerical results that address this problem [18], which does not provide a clear and thorough explanation about the relationship between phase noise and MIMO performance.

In this chapter, a 2×2 MIMO system model is used to investigate the RF impairments. The Alamouti code [19] is employed to demonstrate MIMO diversity ability and RF effects. Quadrature phase-shift keying (QPSK) symbols are transmitted for its convenience to calculate BER performance and to be generalized to higher order modulation schemes. Regardless of the choice of modulations, the signal-to-noise ratio (SNR) degradation analysis is general and is not dependant on modulation schemes. Three RFIC imperfections: transmitter signal coupling, frequency synthesizer output phase noise and gain imbalance, are the major concerns of this chapter. The closed-form analytical expression of the SNR degradation caused by every imperfection is derived. The system BER performance can be directly obtained from their SNR assessments. There is no baseband correction algorithms used to combat the RF impairments because different algorithms have different improvements. Our goal is to get the performance lower bounds that the system might suffer.

This chapter is organized as follows. Section 2.2 develops the MIMO system model considering the signal coupling, phase noise and gain imbalance effects. Section 2.3 derives the

analytical expression of SNR loss due to RF impairments. Section 2.4 provides the Monte-Carlo simulation results to verify the theoretical analysis. Finally, conclusions are drawn in section 2.5.

2.2 System Model

2.2.1 MIMO System Model

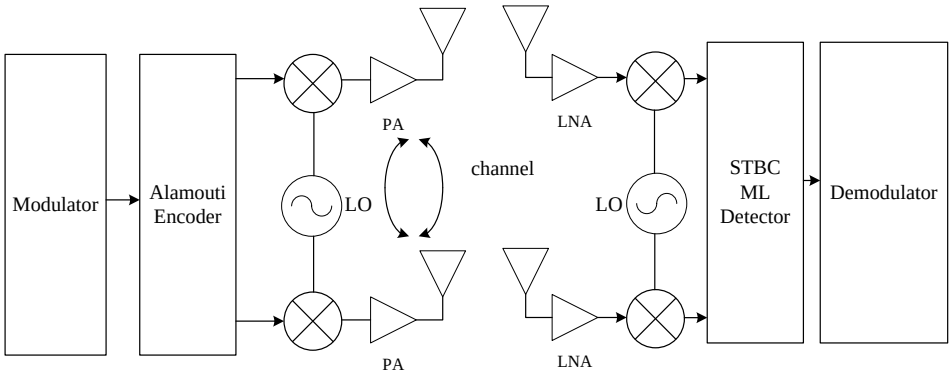


Fig. 2.1 Overview of MIMO communication system.

The MIMO communication system under consideration is modeled in Fig. 2.1. At the transmitter side, the binary data stream is first mapped into complex modulation symbols (e.g. QPSK). Then the symbols are fed into STBC encoder to produce separate symbol streams (2 streams in this analysis). In this chapter, a 2×2 antenna array was established to provide total 4 spatial dimensions, which can be used either for spatial diversity or for spatial multiplexing. Spatial diversity provides more transmission reliability over the wireless channel at no cost of more power or spectrum. However it needs space-time codes (STC) to fully exploit the diversity gain (4 in this analysis) provided by a 2×2 channel environment. Spatial multiplexing supplies more freedom to transmit data simultaneously. In a $M \times N$ MIMO system, the data rate is improved by a factor of min(M,N) times comparing to a SISO system [12] (M and N are numbers of transmitter and receiver's antennas). Since spatial diversity MIMO scheme is more frequently

adopted in the modern communication systems, for example: IEEE802.11n and 3G, this chapter focuses on STC MIMO analysis.

Alamouti [19] proposed a famous STC block coding scheme for transmission using two antennas. This scheme only needs linear processing and is easy to demonstrate the basic effect of RF impairments. Hence Alamouti code is adopted in this chapter. Let's assume that s_1, s_2, s_3, s_4, etc are consecutive symbols generated from QPSK modulator. Alamouti suggested that we group the symbols into groups of two. In the first time slot, send $s_1$and s_2 from the first and second antenna. In second time slot, send $-s_2^*$ and s_1^* from the first and second antenna. Alamouti block code matrix is given by:

$$\mathrm{S} = \begin{bmatrix} s_1 & -s_2^* \\ s_2 & s_1^* \end{bmatrix} \tag{2-1}$$

where vector $[s_1 \quad -s_2^*]$ is the signal sent to the first antenna and vector $[s_2 \quad s_1^*]$ represents the signal sent to the second antenna.

The channel matrix can be expressed as

$$\mathrm{H} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \tag{2-2}$$

where h_{ij} is the complex channel gain from transmitter antenna j to receiver antenna i and modeled as independent Gaussian variables with variance of 0.5 per real dimension.

The additive noise matrix is given by

$$\mathrm{N} = \begin{bmatrix} n_{11} & n_{12} \\ n_{21} & n_{22} \end{bmatrix} \tag{2-3}$$

where n_{ij} is noise received at *i*th antenna of *j*th symbol with variance of σ_n^2, assuming that n_{ij} has Gaussian distribution and is independent of each other. Thus, the received signal matrix can be found as

$$\mathrm{R} = \begin{bmatrix} r_{11} & r_{12} \\ r_{21} & r_{22} \end{bmatrix} = \mathrm{HS} + \mathrm{N} \tag{2-4}$$

The maximum likelihood (ML) estimation of Alamouti code with PSK modulation is given by [19]

$$\hat{s}_1 = h_{11}^* r_{11} + h_{21}^* r_{21} + h_{12} r_{12}^* + h_{22} r_{22}^* \tag{2-5}$$

$$\hat{s}_2 = h_{12}^* r_{11} + h_{22}^* r_{21} - h_{11} r_{12}^* - h_{21} r_{22}^* \tag{2-6}$$

where $*$ denotes the conjugate operation.

2.2.2 Signal Coupling Model

In order to reduce the cost of the MIMO transceiver RFIC, it is desirable to integrate multiple RF transceivers onto a single substrate. Thus the coupling may occur between different RF chains close to each other and cause signal cross-talk. The coupling will increase the correlation between different independent spatial links and degrade system performance. Relative to transmitter coupling, the MIMO system is not very sensitive to receiver coupling, because white noise is added to signal before receiver coupling happens. When MIMO system tries to equalize the receiver coupling, it will not amplify the white noise [20]. In addition, transmitter block has higher power level, so coupling between transmitters is the major concern of this chapter.

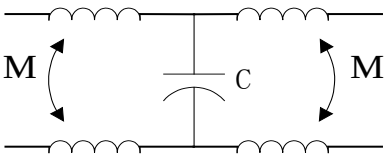


Fig. 2.2 Signal Coupling Model.

Usually the transmitter (TX) and receiver (RX) modules of a full duplex communication system work at different frequencies, namely in a frequency division duplex (FDD) manner. A half duplex system alternates operational period to avoid collision. In either case, the amplified signal in transmitter circuits will not interfere with the receiver chains through coupling and we will not consider this effect in our analysis. Fig. 2.2 illustrates one of the coupling equivalent circuit models. There are two chains interacting with each other by mutual inductance and capacitance cross-talk. These interactions might occur on chip or even between signal traces on printed circuit boards (PCBs) [21]. For MIMO systems, every transceiver occupies relatively large die area and the distance between each other is large enough that coupling capacitance and mutual inductance are small. Most of signal leakage is through the substrate, which can be modeled as resistance. The normal resistivity of silicon substrate is 11-16Ω•cm. Therefore there is considerable substrate loss which cannot be missed. It is assumed that the coupling network has all ports impedance matched. Let α be the voltage transmission coefficient or transmission efficiency defined as

$$|\alpha| = \sqrt{\frac{\text{signal power absorbed by load}}{\text{signal power input to one chain}}} \tag{2-7}$$

Let β be the voltage coupling coefficient defined by

$$|\beta| = \sqrt{\frac{\text{signal power coupled to adjacent load}}{\text{signal power input to one chain}}} \tag{2-8}$$

For most of the applications, the transmitting signal should be much stronger than the coupling signal, namely,

$$|\alpha| \gg |\beta| \tag{2-9}$$

Conservation of energy dictates that

$$|\alpha|^2 + |\beta|^2 \leq 1 \tag{2-10}$$

where $|\alpha|^2 + |\beta|^2 < 1$ happens when energy is lost through resistive coupling. Furthermore an assumption can be made that coupling network has symmetrical property between two RF transmitter chains. Therefore, for one Alamouti block code, corresponding coupling matrix is defined as:

$$\mathrm{C} = \begin{bmatrix} \alpha & \beta \\ \beta & \alpha \end{bmatrix} \tag{2-11}$$

This matrix can be inserted into Eq. (2-4) to generate new received signal matrix with signal coupling impairment

$$\mathrm{R} = \begin{bmatrix} r_{11} & r_{12} \\ r_{21} & r_{22} \end{bmatrix} = \mathrm{HCS} + \mathrm{N} \tag{2-12}$$

2.2.3 Phase Noise Model

Phase noise of voltage controlled oscillator (VCO) has been the topics of numerous studies [22-24]. Used in the local oscillator, VCO provides a sinusoidal wave for the purpose of frequency conversion at the up/down mixers. The VCO output can be expressed as

$$v(t) = A(t)\cos[\omega t + \phi(t)] \tag{2-13}$$

where ω is the angular frequency of oscillator. $A(t)$ and $\phi(t)$are amplitude and phase fluctuations respectively. Since the top–quad transistors in a Gilbert mixer are normally operated in fully switching mode, the LO amplitude modulation can be ignored. Only the phase noise contributes to the single sideband noise spectral density of $v(t)$. The phase noise in a free running VCO is usually treated as non-stationary Brownian motion process. Actually in most RF transceivers, phase-locked loop (PLL) is employed as a frequency synthesizer to provide more stable output. The closed loop PLL output has different phase noise behavior from the free running VCO output. In [25], it is shown that PLL output's power spectral density (PSD) follows the reference signal spectrum for very small frequency offset. Equivalently the PSD's main lobe is narrower than free running VCO. More importantly, the output of the PLL in locked condition is asymptotically wide-sense stationary with zero mean value and little variation, which justifies the assumption below:

$$|\phi(t)| \ll 1 \tag{2-14}$$

Based on Wiener-Khintchine Theorem, narrower PSD main lobe can be translated into longer coherence time. The theoretical prediction and empirical measurement both indicate that the PSD of phase noise falls below -100dBc/Hz beyond ten kHz away from the carrier frequency ω. Most of the modern communication systems occupy at least a few MHz bandwidth in order to support Msps symbol rate, which is much larger than the phase noise fluctuation rate. Hence the phase noises of two consecutive symbols, such as the case of Alamouti code, are strongly positive correlated. (as detailed in Appendix I)

$$\rho = \frac{E\phi(t)\phi(t+T)}{\sigma_\phi^2} \approx 1 \tag{2-15}$$

where T is the symbol duration and σ_ϕ^2 is the variance of phase noise.

2.2.4 Gain Imbalance Model

The MIMO transceiver RFIC integrates multiple RF chains into a single chip. The gain imbalance between different RF chains (transmitters or receivers) is caused by unavoidable device mismatch and process variation that degrades MIMO performance. Let a_1 and a_2 be the voltage gain coefficients of two RF chains at transmitter. The conservation of energy leads to the following normalized equation:

$$|a_1|^2 + |a_2|^2 = 2 \tag{2-16}$$

The same principle also applies to receiver side gain coefficients b_1 and b_2. By inserting matrix $\mathrm{A} = \begin{bmatrix} \mathrm{a}_1 & 0 \\ 0 & \mathrm{a}_2 \end{bmatrix}$ and $\mathrm{B} = \begin{bmatrix} \mathrm{b}_1 & 0 \\ 0 & \mathrm{b}_2 \end{bmatrix}$ into Eq. (2-4), the received signal is rewritten as

$$\mathrm{R} = \begin{bmatrix} r_{11} & r_{12} \\ r_{21} & r_{22} \end{bmatrix} = \mathrm{B}(\mathrm{HAS} + \mathrm{N}) \tag{2-17}$$

Additive noise **N** is also affected by the receiver gain imbalance.

2.3 Performance Degradation Analysis

2.3.1 Signal Coupling Effect

From this section we will start to evaluate the performance degradation caused by RF imperfections. According to Eq. (2-12), **HC** can be considered as a new channel matrix G

$$\mathrm{G} = \mathrm{HC} = \begin{bmatrix} \mathrm{g}_{11} & \mathrm{g}_{12} \\ \mathrm{g}_{21} & \mathrm{g}_{22} \end{bmatrix} \tag{2-18}$$

Assuming perfect channel estimation, the ML estimation of s_1 actually becomes

$$\hat{s}_1 = g_{11}^* r_{11} + g_{21}^* r_{21} + g_{12} r_{12}^* + g_{22} r_{22}^* = (|g_{11}|^2+|g_{21}|^2 + |g_{12}|^2+|g_{22}|^2)s_1 + g_{11}^* n_{11} + g_{21}^* n_{21} + g_{12} n_{12}^* + g_{22} n_{22}^* \quad (2\text{-}19)$$

The noise term still complies with the Gaussian distribution and has the variance $(|g_{11}|^2+|g_{21}|^2 + |g_{12}|^2+|g_{22}|^2)\sigma_n^2$, where σ_n^2 is variance of additive noise of one symbol at antenna. Frobenius norm leads to

$$\|\mathrm{G}\|_F^2 = \mathrm{Tr}(\mathrm{G}^{\mathrm{H}}\mathrm{G}) = |g_{11}|^2+|g_{21}|^2 + |g_{12}|^2+|g_{22}|^2 \quad (2\text{-}20)$$

where superscript **H** represents Hermitian transpose. **Tr** denotes trace of matrix. Hence SNR after ML estimator becomes

$$SNR = \|\mathrm{G}\|_F^2 \frac{\sigma_s^2}{\sigma_n^2} \quad (2\text{-}21)$$

σ_s^2 is transmission power of one symbol. SNR loss due to RF imperfection is defined by SNR without impairment over SNR with impairment. In this case, SNR loss is given by

$$SNR_{loss} = \frac{\|\mathrm{H}\|_F^2 \sigma_s^2/\sigma_n^2}{\|\mathrm{G}\|_F^2 \sigma_s^2/\sigma_n^2} = \frac{\|\mathrm{H}\|_F^2}{\|\mathrm{G}\|_F^2} \quad (2\text{-}22)$$

If no coupling exists, the channel matrix G will degenerate to H. Then SNR loss is 0 dB. According to Eq. (2-18),

$$\|\mathrm{G}\|_F^2 = \|\mathrm{H}\|_F^2(|\alpha|^2 + |\beta|^2) + 4\big(\mathrm{Re}(h_{11}h_{12}^*) + \mathrm{Re}(h_{21}h_{22}^*)\big)\mathrm{Re}(\alpha\beta^*) \quad (2\text{-}23)$$

Therefore the closed-form expression of SNR loss due to transmitter signal coupling can be expressed as:

$$SNR_{loss} = \frac{1}{|\alpha|^2 + |\beta|^2 + \frac{2\mathrm{Re}(h_{11}h_{12}^* + h_{21}h_{22}^*)}{\|\mathrm{H}\|_F^2} 2\mathrm{Re}(\alpha\beta^*)}$$

(2-24)

where $2\mathrm{Re}(h_{11}h_{12}^* + h_{21}h_{22}^*)/\|\mathrm{H}\|_F^2$ is defined as channel characteristic value. For some special cases, SNR loss can reduce to a simpler form. If h_{11}=h_{12}=h_{21}=h_{22}=1 holds as shown in Fig. 2.3, the SNR loss degenerates to Eq. (2-25).

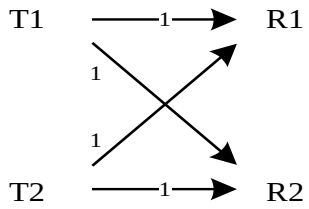


Fig. 2.3 Channel model h11 =h12 =h21 =h22 =1.

$$SNR_{loss} = \frac{1}{|\alpha|^2 + |\beta|^2 + 2\mathrm{Re}(\alpha\beta^*)} = \frac{1}{|\alpha + \beta|^2}$$

(2-25)

As an example, if there is -23dB coupling$(\beta = -0.07)$, 0.35dB attenuation $(\alpha = 0.96)$, the SNR loss is calculated about 1dB. If there are two parallel independent SISO channels, i.e. h_{12}=h_{21}=0 as shown in Fig. 2.4, the SNR loss would degenerate to Eq. (2-26).

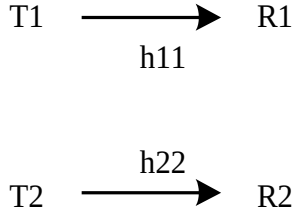


Fig. 2.4 Channel model h12 =h21 =0.

$$SNR_{loss} = \frac{1}{|\alpha|^2 + |\beta|^2} \tag{2-26}$$

As an exmaple, if there is 1.11dB signal strength attenuation and -20dB signal coupling to the other RF chain, which leads to about 1dB SNR loss. As known from Eq. (2-10), $|\alpha|^2+|\beta|^2$ represents total energy minus energy consumed in any resistive coupling. Hence it means SNR loss is only caused by energy loss, not by energy coupling in this case. In general, a MIMO system cares more about how much energy is leaked regardless of whether it is consumed in resistivity substrate or coupled to adjacent chain. If -20dB energy coupling is acceptable, the signal isolation between two chains should be no less than -20dB. This result becomes clearer in the SNR plot given in next section.

For QPSK modulation, BER is given by [26]

$$Q\left(\sqrt{SNR/2}\right)\left[1 - \frac{1}{2}Q\left(\sqrt{SNR/2}\right)\right] \tag{2-27}$$

where

$$Q(x) = \frac{1}{\sqrt{2\pi}}\int_x^\infty e^{-t^2/2}dt\,, x \geq 0 \tag{2-28}$$

There will be approximate 10^{-4} BER increase corresponding to 1dB SNR loss.

2.3.2 Phase Noise Effect

Modern communication systems have adopted a variety of phase noise tracking algorithms in baseband to compensate the phase noise impact on SNR degradation. Different algorithms can improve performance to different extents. Hence it is practical for us to leave these baseband algorithms out of analysis so that we can derive a generic performance lower bound. If MIMO radio can meet the lower bound requirement, the real system performance can only be better when considering advanced phase noise cancellation algorithms.

The phase noise of both the transmitter and the receiver should be simultaneously considered. For the sake of cost reduction and carrier synchronization, different RF chains in one MIMO transceiver usually share one frequency synthesizer. The only difference is that the routes from local oscillator (LO) output to different mixers may have different delays. However this time delay can be incorporated into channel coefficients under fixed carrier frequency ω, which will be estimated and compensated by the baseband channel estimation. Therefore this effect is not considered and the strict synchronization between LO signal routes is unnecessary as well. Let us assume at the transmitter side, there is one LO source with frequency ω and phase noise $\phi 1(t)$. The MIMO transmission matrix **S** can be rewritten as

$$e^{j(\omega t+\phi 1(t))}\begin{bmatrix}\sum s_{1k}a(t-2kT) & -\sum s_{2k}^{*}a(t-2kT-T)\\ \sum s_{2k}a(t-2kT) & \sum s_{1k}^{*}a(t-2kT-T)\end{bmatrix} \tag{2-29}$$

where $a(t)$ is the real shaping filter impulse response; S_{1k} is the first symbol in the kth Alamouti block and S_{2k} is the second one where subscript k is time index or block index. At the receiver side, it is reasonable to assume carrier frequency is captured and LO is locked to ω. Let $\phi 2(t)$ be

the phase noise of receiver synthesizer. Defining $s_1(t)=\sum s_{1k}\cdot a(t-2kT)$ and $s_2(t)=\sum s_{2k}\cdot a(t-2kT)$, the received signal after the quadrature demodulator is expressed as

$$e^{j(\phi 1(t)-\phi 2(t))}\mathrm{H}\begin{bmatrix} s_1(t) & -s_2^*(t-T) \\ s_2(t) & s_1^*(t-T) \end{bmatrix} \tag{2-30}$$

Let $\phi \triangleq \phi 1 - \phi 2$ and assume $\phi 1$ and $\phi 2$ are independent and identically-distributed (i.i.d.) stochastic process. Equation (2-30) can be further simplified to

$$e^{j\phi}\begin{bmatrix} h_{11}s_1(t)+h_{12}s_2(t) & -h_{11}s_2^*(t-T)+h_{12}s_1^*(t-T) \\ h_{21}s_1(t)+h_{22}s_2(t) & -h_{21}s_2^*(t-T)+h_{22}s_1^*(t-T) \end{bmatrix} \tag{2-31}$$

After the match filter, the first term of (2-31) becomes

$$\int h_{11}e^{j\phi(t)}\sum s_{1k}a(t-2kT)a^*(t-2nT)\,dt$$

$$+\int h_{12}e^{j\phi(t)}\sum s_{2k}a(t-2kT)a^*(t-2nT)\,dt$$

$$=(h_{11}s_{1n}+h_{12}s_{2n})\int e^{j\phi(t)}|a(t-2nT)|^2dt \tag{2-32}$$

Again according to Eq. (2-15), the above formula equals to

$$\approx (h_{11}s_{1n}+h_{12}s_{2n})e^{j\phi(2nT)}\int |a(t-2nT)|^2dt$$

$$=(h_{11}s_{1n}+h_{12}s_{2n})e^{j\phi(2nT)} \tag{2-33}$$

Similar process is applied to other three elements of Eq. (2-31). If we define $e^{j\phi_n}=e^{j\phi(2nT)}\approx e^{j\phi(2nT+T)}$, the received signal matrix after match filter is

$$e^{j\phi_n}\begin{bmatrix} h_{11}s_{1n}+h_{12}s_{2n} & -h_{11}s_{2n}^*+h_{12}s_{1n}^* \\ h_{21}s_{1n}+h_{22}s_{2n} & -h_{21}s_{2n}^*+h_{22}s_{1n}^* \end{bmatrix} \tag{2-34}$$

From Eq. (2-5), the ML estimation of s_{1n} leads to

$$\hat{s}_{1n} = \|H\|_F^2 s_{1n} + \left[(|h_{11}|^2 + |h_{21}|^2)\left(e^{j\phi_n} - 1\right) + (|h_{12}|^2 + |h_{22}|^2)\left(e^{-j\phi_n} - 1\right)\right]s_{1n} + (h_{12}h_{11}^* + h_{22}h_{21}^*)\left(e^{j\phi_n} - e^{-j\phi_n}\right)s_{2n} \tag{2-35}$$

From Eq. (2-14), a simplification can be made as

$$e^{j\phi_n} \approx 1 + j\phi_n \tag{2-36}$$

As a result, Eq. (2-35) reduces to

$$\hat{s}_{1n} = \|H\|_F^2 s_{1n} + (|h_{11}|^2 + |h_{21}|^2 - |h_{12}|^2 - |h_{22}|^2)j\phi_n s_{1n} + 2(h_{11}^* h_{12} + h_{21}^* h_{22})j\phi_n s_{2n} \tag{2-37}$$

Similar to the previous discussion on coupling effect, the additive noise whose power is $\|\mathrm{H}\|_F^2\sigma_n^2$ should be included. Frequency down conversion in receiver does not change the probability distribution and correlation of additive noise. Under the condition of PSK modulation, all possible constellations of a symbol have constant amplitude, thus $D(\varphi s)=D(\varphi)|s|^2$, where D denotes variance. The second term in Eq. (2-37) is actually uncorrelated to signal s_{1n} with variance $(|h_{11}|^2+|h_{21}|^2-|h_{12}|^2-|h_{22}|^2)^2\sigma_s^2\sigma_\phi^2$, where $\sigma_\phi^2 = D(\phi)$. The third term in (2-37) has a variance of $4|h_{11}^* h_{12} + h_{21}^* h_{22}|^2\sigma_s^2\sigma_\phi^2$. The two terms are also uncorrelated to each other and have zero mean values. Thus total energy of interference can be found out as

$$\{(|h_{11}|^2 + |h_{21}|^2 - |h_{12}|^2 - |h_{22}|^2)^2 + 4|h_{12}h_{11}^* + h_{22}h_{21}^*|^2\}\sigma_s^2\sigma_\phi^2 + \|H\|_F^2\sigma_n^2 \tag{2-38}$$

The SNR loss due to phase noise in a 2×2 Alamouti STBC is given by

$$SNR_{loss} = 1 + \frac{\left\{\left(|h_{11}|^2+|h_{21}|^2-|h_{12}|^2-|h_{22}|^2\right)^2+4|h_{12}h_{11}^*+h_{22}h_{21}^*|^2\right\}\sigma_s^2\sigma_\phi^2}{\|H\|_F^2\sigma_n^2} \tag{2-39}$$

Obviously if phase noise power is zero, SNR loss is 0dB. If additive noise is large, SNR loss due to phase noise will be small. Same thing happens to SISO channels. As known, SNR loss depends not only on phase noise power but also on signal power. Larger signal power also causes larger error vector magnitude (EVM) under same phase rotation. Eq. (2-39) confirms this property.

Those two interference terms in Eq. (2-37) do not comply with Gaussian distribution and the performance degradation caused by phase noise naturally cannot be calculated analytically using Eq. (2-27). Instead, Monte-Carlo simulation will be used to evaluate the BER performance and demonstrate the validity of Eq. (2-39). But an interesting observation is that when h_{12}=h_{21}=0 and $|h_{11}|$=$|h_{22}|$, or vice versa, which implies no link is established between different antenna indices or same indices, there is no performance degradation however large phase noise power is (if only $|\varphi_n|$<<1). The reason is that the second independent antenna provides diversity (another copy of phase noise) to cancel phase noise effect of first antenna. However this does not hold for all channel conditions.

Although direct application of Eq. (2-27) is impossible, there is other numerical solution of BER calculation. First assume $s_{1n} = (1 + j)\sigma_s/\sqrt{2}$ is transmitted (QPSK modulation), which means the constellation is in the first quadrant, and phase noise ϕ_n is of normal distribution which is a good approximation to real situations. Hence the second and third term interferences in Eq. (2-37) are both of normal distribution with zero mean values under the condition that s_{2n} is also specified. Defining

$$A = \mathrm{Re}\left\{(|h_{11}|^2+|h_{21}|^2-|h_{12}|^2-|h_{22}|^2)j\frac{1+j}{\sqrt{2}}\sigma_s + 2(h_{11}^*h_{12} + h_{21}^*h_{22})js_{2n}\right\}$$

$$B = \mathrm{Im}\left\{(|h_{11}|^2+|h_{21}|^2-|h_{12}|^2-|h_{22}|^2)j\frac{1+j}{\sqrt{2}}\sigma_s + 2(h_{11}^* h_{12} + h_{21}^* h_{22})js_{2n}\right\} \tag{2-40}$$

Because sum of normal distributed variables is still normal distributed, the vector of the real part and imaginary part of the interference plus additive noise has a covariance matrix expressed as:

$$\mathrm{C}=\begin{bmatrix} A^2 & AB \\ BA & B^2 \end{bmatrix}\sigma_\phi^2 + \begin{bmatrix} \|H\|_F^2\sigma_n^2 & \\ & \|H\|_F^2\sigma_n^2 \end{bmatrix}$$

$$= \begin{bmatrix} A^2\sigma_\phi^2 + \|H\|_F^2\sigma_n^2 & AB\sigma_\phi^2 \\ BA\sigma_\phi^2 & B^2\sigma_\phi^2 + \|H\|_F^2\sigma_n^2 \end{bmatrix} \tag{2-41}$$

The distribution of $\hat{s}_{1n}$ is given by

$$f_{s_{1n}=\frac{(1+j)\sigma_s}{\sqrt{2}},s_{2n}}(x,y)$$

$$= \frac{\exp\left\{-\frac{1}{2}\begin{bmatrix} x-\|H\|_F^2\sigma_s/\sqrt{2} \\ y-\|H\|_F^2\sigma_s/\sqrt{2} \end{bmatrix}^T \mathrm{C}^{-1}\begin{bmatrix} x-\|H\|_F^2\sigma_s/\sqrt{2} \\ y-\|H\|_F^2\sigma_s/\sqrt{2} \end{bmatrix}\right\}}{2\pi|\mathrm{C}|^{1/2}} \tag{2-42}$$

where x and y are real part and imaginary part of $\hat{s}_{1n}$ respectively. Thus the probability of correct decision is

$$P_c = \iint_{\text{first quadrant}} f_{s_{1n}=\frac{(1+j)\sigma_s}{\sqrt{2}},s_{2n}}(x,y)\,dx\,dy \tag{2-43}$$

The error probability is 1-P_c. So the error probability when $s_{1n} = (1+j)\sigma_s/\sqrt{2}$ is the expectation value of 1-P_c respective to s_{2n}:

$$P_e = \frac{1}{4}\sum_{i=0}^{3}(1-P_c)|_{s_{2n}=s_i} \tag{2-44}$$

where s_i is one of four possible QPSK symbols. Due to the symmetrical property of QPSK modulation, the average symbol error rate equals to that of $s_{1n} = (1+j)\sigma_s/\sqrt{2}$. The BER is nearly half of P_e because of Gray encoding.

2.3.3 Gain Imbalance Effect

Define $\mathrm{G} = \mathrm{BHA} = \begin{bmatrix} a_1 b_1 h_{11} & a_2 b_1 h_{12} \\ a_1 b_2 h_{21} & a_2 b_2 h_{22} \end{bmatrix}$. After some straightforward calculation,

$$\|\mathrm{G}\|_F^2 = |a_1|^2|b_1|^2(|h_{11}|^2 - |h_{12}|^2 - |h_{21}|^2 + |h_{22}|^2) + 2|a_1|^2(|h_{21}|^2 - |h_{22}|^2) + 2|b_1|^2(|h_{12}|^2 - |h_{22}|^2) + 4|h_{22}|^2 \tag{2-45}$$

Because the additive noise is also influenced by receiver gain imbalance, the variance of noise after ML estimator is given by

$$\begin{aligned}&(|g_{11}b_1|^2 + |g_{21}b_2|^2 + |g_{12}b_1|^2 + |g_{22}b_2|^2)\sigma_n^2 \\ &= \{|b_1|^4[|a_1|^2(|h_{11}|^2 + |h_{21}|^2) + |a_2|^2(|h_{12}|^2 + |h_{22}|^2)] \\ &\quad + 4(1-|b_1|^2)(|a_1|^2|h_{12}|^2 + |a_2|^2|h_{22}|^2)\}\sigma_n^2\end{aligned} \tag{2-46}$$

The signal power is the same as previous discussion, i.e., $\|\mathrm{G}\|_F^4\sigma_s^2$. Thus SNR after ML estimator becomes

$$SNR = \frac{\sigma_s^2\|\mathrm{G}\|_F^4}{\{|b_1|^4[|a_1|^2(|h_{11}|^2 + |h_{21}|^2) + |a_2|^2(|h_{12}|^2 + |h_{22}|^2)] + 4(1-|b_1|^2)(|a_1|^2|h_{12}|^2 + |a_2|^2|h_{22}|^2)\}\sigma_n^2} \tag{2-47}$$

SNR loss compared with balanced gain is

$$SNR_{loss} = \frac{\|\mathrm{H}\|_F^2}{\|\mathrm{G}\|_F^4}\{|b_1|^4[|a_1|^2(|h_{11}|^2 + |h_{21}|^2) + |a_2|^2(|h_{12}|^2 + |h_{22}|^2)]$$

$$+ 4(1 - |b_1|^2)(|a_1|^2|h_{12}|^2 + |a_2|^2|h_{22}|^2)\} \tag{2-48}$$

It can be noticed that SNR loss is independent of signal to noise ratio. For some special cases such as channel $|h_{11}|=|h_{12}|=|h_{21}|=|h_{22}|=1$, the SNR loss can be simplified to $(|b_1|^2\text{-}1)^2+1$, which indicates that the performance degradation does not depend on transmitter's gain imbalance. Furthermore, maximum SNR loss is 3dB. When $|b_1|=0.7$ or $|b_1|=1.23$ (4.88dB gain imbalance), there is 1dB SNR loss and 10^{-4} BER increase respectively for QPSK modulation. For channel $|h_{12}|=|h_{21}|=0$ and $|h_{11}|=|h_{22}|=1$,

$$SNR_{loss} = \frac{2[1+(|a_1|^2-1)(|b_1|^2-1)]-|b_1|^2|b_2|^2}{[1+(|a_1|^2-1)(|b_1|^2-1)]^2} \tag{2-49}$$

Thus in this case if the receiver has balanced gain, SNR loss will not occur no matter how large transmitter imbalance is. Both cases imply that gain balance of receivers, not transmitters, is more important for good performance, which is reasonable because receiver gain imbalance will magnify the additive noise**.**

2.4 Simulation Results

In the above section, the closed-form analysis of performance based on equivalent SNR loss measurement is presented. In this section these results will be verified by the Monte-Carlo simulation. Although all results were derived independent of channel types, it is necessary to choose a few typical channel types for the Monte-Carlo simulation. BER performance is adopted as the criterion. QPSK is the modulation method in simulation while analytical results are modulation independent**.** Performance is calculated based on different E_b/N_0 conditions, which represents energy of one bit over single side band PSD of white additive noise. Furthermore the

analytical expression of SNR loss under different RF impairments conditions is plotted for the purpose of visualization and comparison with Monte-Carlo simulations**.** The arithmetic average of SNR loss respective to channel **H** is evaluated to approach statistical average. Channel **H** follows the normal distribution and independent fading.

2.4.1 Signal Coupling Effect

Fig. 2.5 illustrates 3-D diagram of SNR loss due to the signal coupling at transmitter side. The two parameters which SNR loss depends on are $1\text{-}|\alpha|^2$ and $|\beta|^2$. α and β are both real numbers. Parameter $1\text{-}|\alpha|^2$ ranges from -30dB to -20dB, and parameter $|\beta|^2$ varies from -60dB to -40dB. The corresponding contour is also presented in Fig. 2.5. The results show that in simulated region, coupling coefficient $|\beta|^2$ has ignorable impact on the performance loss. All degradations are dominated by $1\text{-}|\alpha|^2$ as stated before. But when $|\beta|^2$ increases further with the constant power absorption coefficient $|\alpha|^2$, larger coupling coefficient $|\beta|^2$ leads to less performance degradation. It implies if power mismatch is constant, energy cross coupling

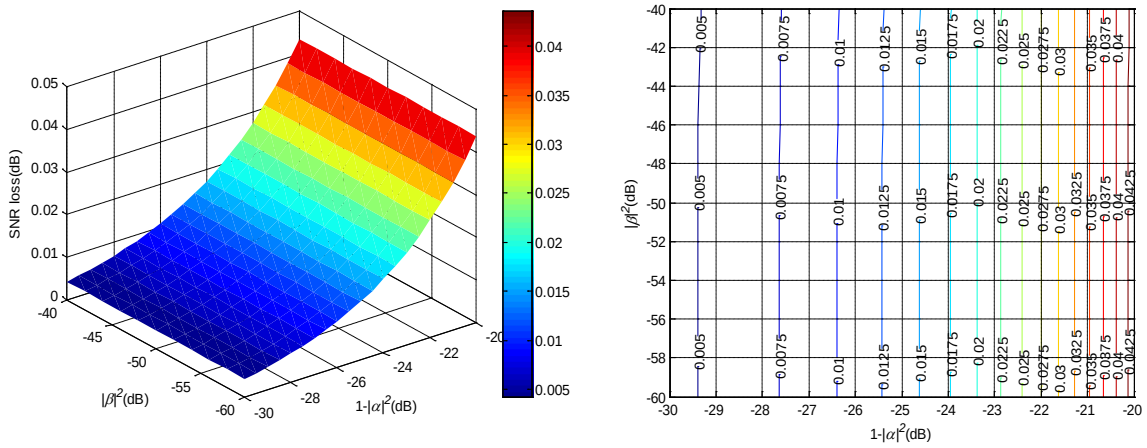


Fig. 2.5 3-D diagram and 2-D contour of SNR loss from the signal coupling in transmitter.

to adjacent branch is better than energy consumption in resistive substrate. Energy loss cannot be recovered by MIMO STBC code. As shown in Fig. 2.5, when power mismatch $1\text{-}|\alpha|^2$ is less than

-20dB, the SNR loss is less than 0.04dB, which is negligible. This gives us an upper bound about how large the signal coupling is affordable**.**

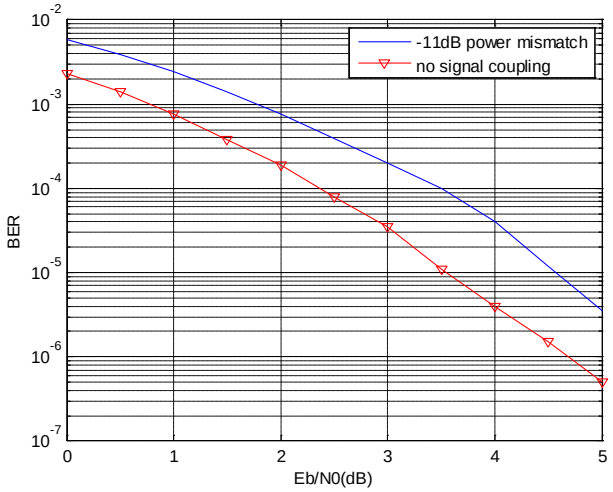


Fig. 2.6 BER loss from signal coupling in channel $\boldsymbol{h_{11} = h_{22} = h_{12} = h_{21} = 1}$.

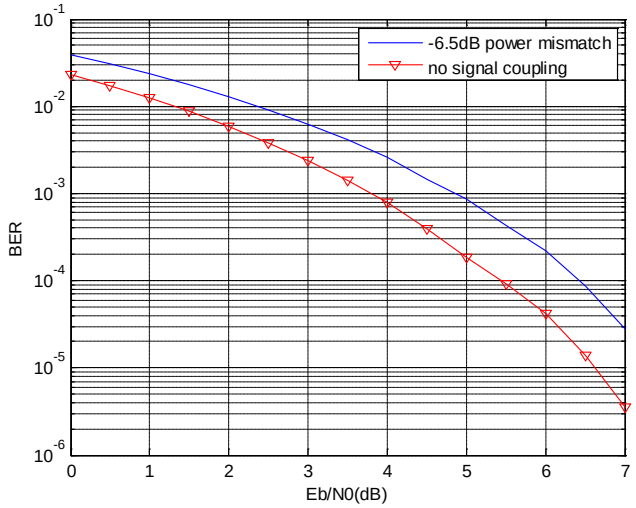


Fig. 2.7 BER loss from signal coupling in channel $\boldsymbol{h_{11} = h_{22} = 1, h_{12} = h_{21} = 0}$.

From Eq. (2-25), it is predicted that if there is -23dB signal coupling (β=−0.07), −11dB power mismatch (α=0.96), the SNR loss will be about 1dB. This channel situation is simulated by Monte-Carlo method and presented in Fig. 2.6. It is clearly shown that there is 1dB SNR loss

between two curves, which exactly matches the theoretical analysis. Another situation where channel coefficients h_{12}=h_{21}=0 and h_{11}=h_{22}=1 and α=0.88 (-6.5dB power mismatch), β=−0.1 (-20dB cross talking), is simulated. The performance loss is anticipated to be 1dB too and shown in Fig. 2.7. Furthermore, what most interests us is to know the limit of coupling which system can tolerate. For this purpose, RF chain coupling effect: α=0.99, β=−0.01, that is -17dB power mismatch and -40dB coupling coefficient, is simulated. In a channel environment: h_{11}=h_{12}=h_{21}=h_{22}=1, BER performance is shown in Fig. 2.8. The performance difference is about 0.1 dB. The channel environment h_{12}=h_{21}=0 and h_{11}=h_{22}=1 is simulated and shown in Fig. 2.9 and the performance loss is even less than 0.1dB. Therefore power mismatch less than -17dB is the reasonable requirement for negligible performance degradation of QPSK modulation. If considering higher order modulation scheme, e.g. QAM, the requirement will become more restrictive accordingly. In general -20dB power mismatch gives us acceptable performance. This result agrees with the analysis from Fig. 2.5 and the conclusion from [20], which requires 20dB isolation for negligible MIMO performance degradation.

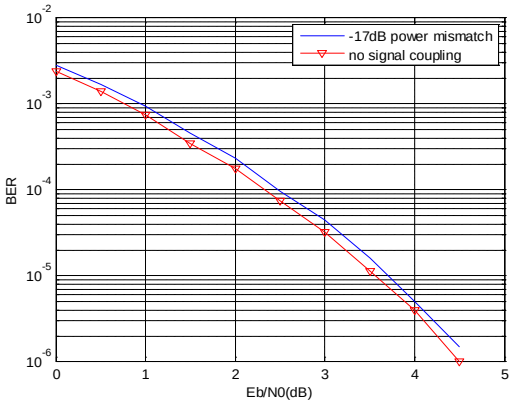


Fig. 2.8 BER loss from signal coupling in channel $\boldsymbol{h_{11} = h_{22} = h_{12} = h_{21} = 1}$.

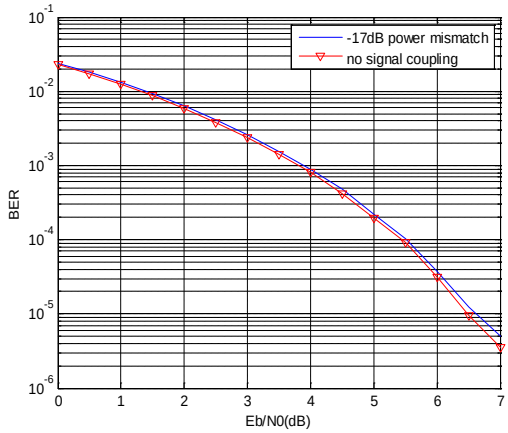


Fig. 2.9 BER loss from signal coupling in channel $\boldsymbol{h_{11} = h_{22} = 1, h_{12} = h_{21} = 0}$.

2.4.2 Phase Noise Effect

Fig. 2.10 illustrates a 3-D diagram of SNR loss due to the phase noise at both transmitter and receiver sides. The two parameters which the SNR loss depends on are signal-to-noise ratio σ_s^2/σ_n^2 displayed in decibel unit and one side (receiver or transmitter) phase noise root mean square (RMS) value $\sigma_\phi/\sqrt{2}$ in degree unit. The corresponding contour is presented in Fig. 2.10 too. As far as the region calculated (phase noise less than two degree), SNR loss is smaller than 0.1dB, small enough to be neglected**.**

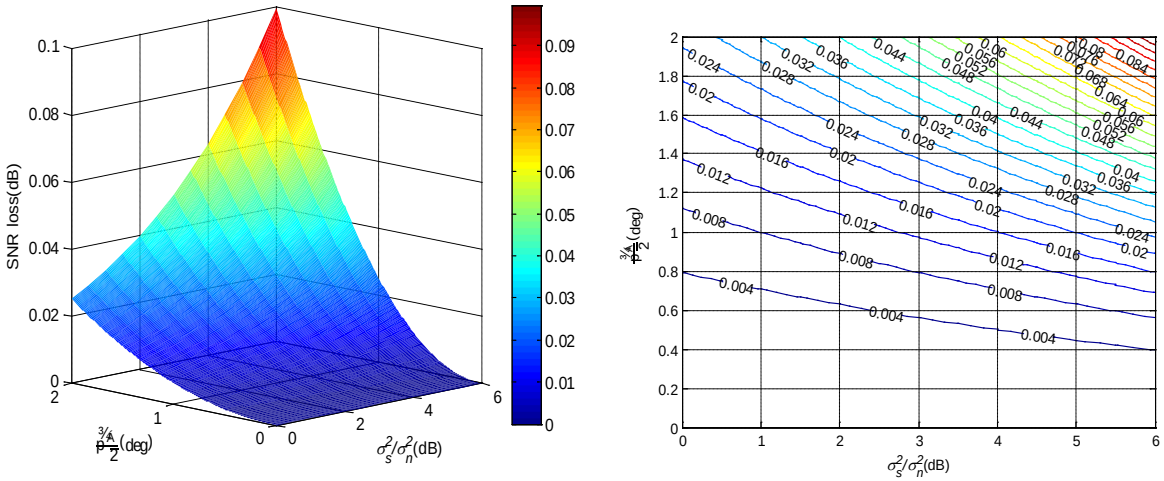


Fig. 2.10 3-D diagram and 2-D contour of SNR loss from phase noise.

Two figures, Fig. 2.11 and Fig. 2.12, show the Monte-Carlo simulation results of channel environment: h_{12}=h_{21}=0, h_{11}=h_{22}=1 and h_{12}=h_{21}=1, h_{11}=h_{22}=0 respectively. In the simulation we use phase noise with Gaussian distribution amplitude. It is assumed to have 0.05 radian RMS value at both transmitter and receiver sides, thus noise power is 0.0025 and $\sigma_{\phi}^{2} = 0.005$. We can find there is almost no performance degradation and this is the situation predicted by theoretical analysis. It should be pointed out that this phenomenon is not caused by small phase noise power, but by the specific channel condition and MIMO diversity, which makes MIMO system is more robust to phase noise than SISO system**.** When channel environment changes, performance degradation will emerge as shown in Fig. 2.13, where h_{11}=h_{12}=h_{21}=h_{22}=1. In this figure, the SNR loss is proportional to signal SNR itself. Due to 0.05 radian RMS value phase noise, there is 0.25dB SNR loss around BER=10^{-4} region. When SNR goes higher, performance loss also becomes higher, even more than 0.5dB at high SNR end. As for the requirement of phase noise tolerance, exact result should be obtained by numerical evaluation of Eq. (2-44). But Monte-Carlo simulation can give the approximate value. In Fig. 2.14, BER performance is

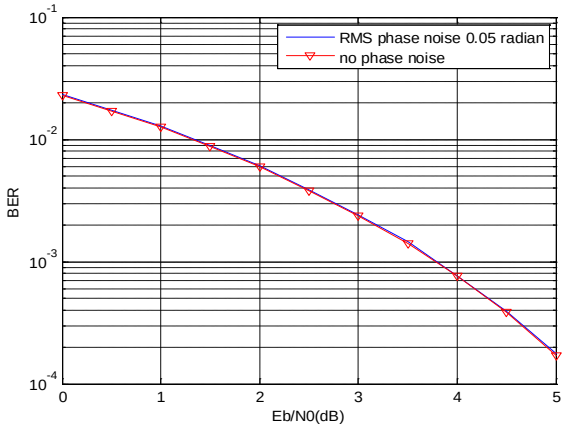


Fig. 2.11 BER loss from phase noise in channel $\boldsymbol{h_{11} = h_{22} = 1, h_{12} = h_{21} = 0}$.

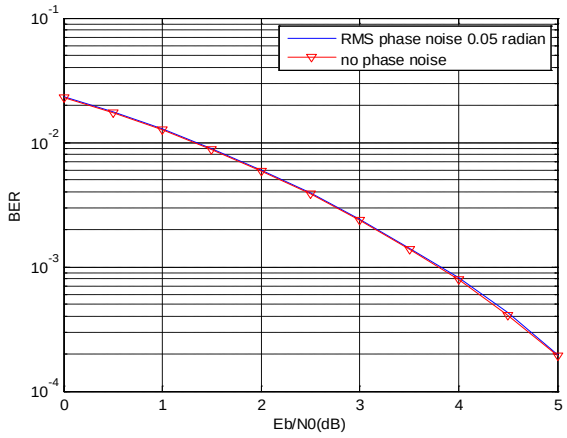


Fig. 2.12 BER loss from phase noise in channel $\boldsymbol{h_{11} = h_{22} = 0, h_{12} = h_{21} = 1}$.

simulated with 1 degree phase noise RMS value (0.0175 radian). Performance degradation is ignorable.

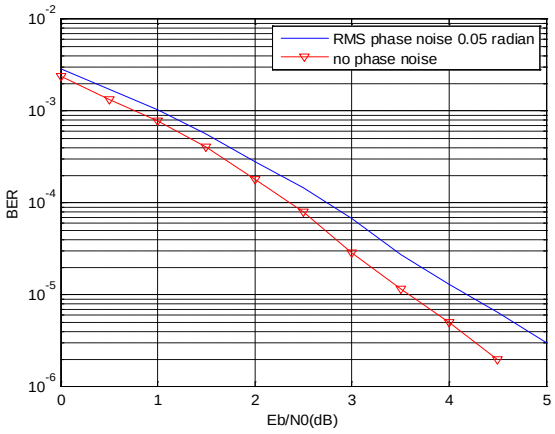


Fig. 2.13 BER loss from phase noise in channel $\boldsymbol{h_{11} = h_{22} = h_{12} = h_{21} = 1}$.

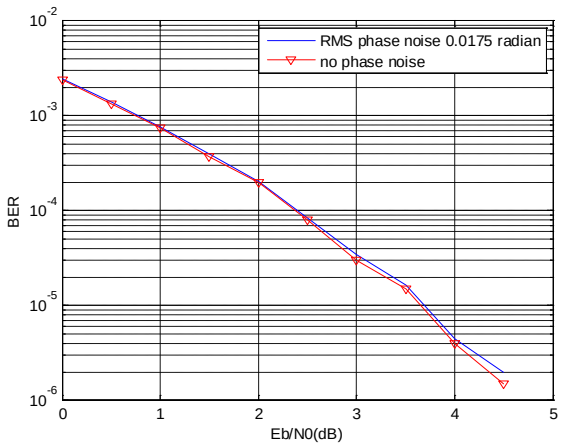


Fig. 2.14 BER loss from phase noise in channel $\boldsymbol{h_{11} = h_{22} = h_{12} = h_{21} = 1}$.

The simulations given above set up the upper limit of phase noise impact on MIMO system performance. Actually in modern communication systems lots of phase noise cancellation techniques are employed to reduce its impact thus the degradation will be less than our result.

2.4.3 Gain Imbalance Effect

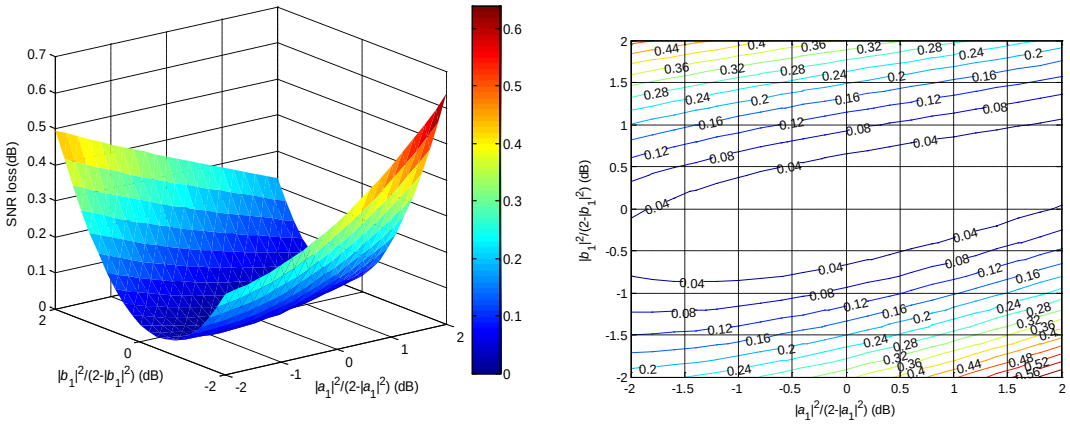


Fig. 2.15 3-D diagram and 2-D contour of SNR loss from transceiver gain imbalance.

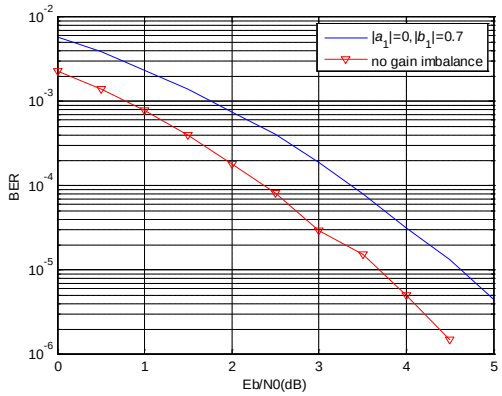


Fig. 2.16 BER loss from gain imbalance in channel $\boldsymbol{h_{11} = h_{22} = h_{12} = h_{21} = 1}$.

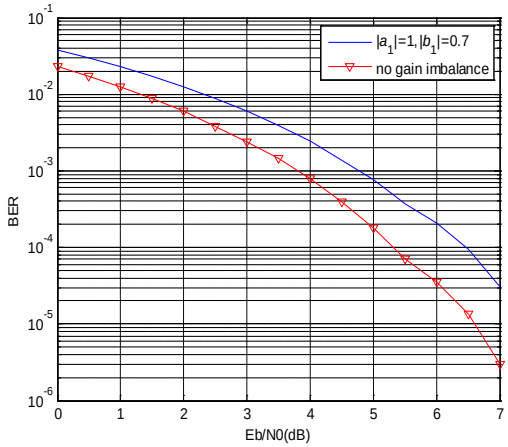


Fig. 2.17 BER loss from gain imbalance in channel $\boldsymbol{h_{11} = h_{22} = 1, h_{12} = h_{21} = 0}$.

Fig. 2.15 illustrates a 3-D diagram of SNR loss due to gain imbalance at both transmitter side and receiver side. The two parameters which SNR loss depends on are gain imbalance of transmitter: $|a_1|^2/(2-|a_1|^2)$ and that of receiver: $|b_1|^2/(2-|b_1|^2)$. The corresponding contour is also provided in Fig. 3.15. The figures demonstrate that SNR loss is not symmetrical around the center point $|a_1|^2=|a_2|^2=1$ or $|b_1|^2=|b_2|^2=1$, but it does have 0dB SNR loss at $|a_1|^2=|a_2|^2=1$ and $|b_1|^2=|b_2|^2=1$. Furthermore, it can be observed that SNR loss is more sensitive to the receiver gain imbalance $|b_1|^2$ than to the transmitter gain imbalance $|a_1|^2$ because the receiver gain imbalance affects additive noise. From Fig. 2.15, if 0.1dB SNR loss or less is the design requirement, the

receiver gain imbalance should be kept within ±1dB and transmitter gain should be within ±1.5dB.

The analytical results of RF chains' gain imbalance are also verified by BER simulation. First the channel environment $h_{11}= h_{12}=h_{21}=h_{22}=1$ with $b_1=0.7$ and $a_1=0$ was simulated and BER was plotted in Fig. 2.16. Despite the total imbalance in transmitter, the performance loss is mild and stays at 1dB. This result agrees with the previous analysis. Another channel environment $h_{12}=h_{21}=0$ and $h_{11}=h_{22}=1$ was simulated with $b_1=0.7$ and $a_1=1$ (no transmitter gain imbalance) and presented in Fig. 2.17. The curve matches the theoretical prediction exactly and exhibits 1dB SNR loss.

2.5 Conclusion

In this chapter, the MIMO RFIC imperfections including signal coupling, phase noise and gain imbalance among different RF paths are investigated. The rigorous analytical expressions of the performance degradation are derived. Results presented can be directly used as a basic reference for RFIC designers to evaluate the design specifications. It is shown that MIMO system has some interesting responses to RF impairments which do not happen in SISO environment. Monte-Carlo simulation is the part of this chapter's work which generates well matched results with theoretical analysis. In our analyzed scenario, less than -20dB transmitter power mismatch leads to negligible performance loss. That means more than -20dB coupling isolation is required. For the phase noise, less than two degree RMS value guarantees no more than 0.1dB SNR loss. In order to neglect the performance loss caused by RF chains' gain imbalance, the imbalance of transmitter and receiver had better to be kept under 1dB. Investigation on RF impairments has significant meanings in improving wireless communication systems performance, such as throughput, BER and quality of service (QoS) in cell phone and WLAN applications [27-29],

especially in continuously varying environment [30]. Other RF impairments which were not covered by this chapter include power amplifier nonlinear distortion [31], whose impact on MIMO system performance will be explored in future research.

Chapter 3 Radar Transceiver with Stretch Processing

3.1 Introduction

Radar is the acronym of radio detection and ranging. Radar systems use the electromagnetic waves to locate the objects, e.g., aircraft; ships, guided missiles and terrain, meantime determine the range, altitude, direction and speed information of objects. The radar system sends the electromagnetic wave which will bounce off the object, and the fraction of returned wave is sensed by the radar.

This chapter covers the materials from theoretical analysis of modern radar system, to advanced technique applied such as stretch processing. The whole radar transceiver specification is developed. Finally one of the critical design blocks, power amplifier (PA) driver is presented. The whole transceiver IC was fabricated in 0.13um BiCMOS technology.

3.1.1 Frequency band allocation

The international telecommunication union (ITU) designates the following radio bands for different applications.

Table 3-1 ITU Radio Bands

Band Number	Symbols	Frequency Range	Wavelength Range	Typical sources
1	ELF	3 to 30 Hz	10,000 to 100,000 km	deeply-submerged submarine communication

2	SLF	30 to 300 Hz	1000 to 10,000 km	submarine communication, ac power grids
3	ULF	300 to 3000 Hz	100 to 1000 km	earthquakes, earth mode communication
4	VLF	3 to 30 kHz	10 to 100 km	near-surface submarine communication,
5	LF	30 to 300 kHz	1 to 10 km	AM broadcasting, aircraft beacons
6	MF	300 to 3000 kHz	100 to 1000 m	AM broadcasting, aircraft beacons, amateur two-way radio
7	HF	3 to 30 MHz	10 to 100 m	Skywave long range radio communication: shortwave broadcasting, military, maritime, diplomatic, amateur two-way radio
8	VHF	30 to 300 MHz	1 to 10 m	FM radio broadcast, television broadcast, PMR, DVB-T, MRI
9	UHF	300 to 3000 MHz	10 to 100 cm	PMR, television broadcast, microwave oven, GPS, mobile phone communication (GSM, UMTS, 3G, HSDPA), cordless phones (DECT), WLAN (Wi-Fi 802.11 b/g/n), Bluetooth
10	SHF	3 to 30 GHz	1 to 10 cm	DBS satellite television broadcasting, WLAN (Wi-Fi 802.11 a/n), microwave relays, WiMAX, radars

11	EHF	30 to 300 GHz	1 to 10 mm	microwave relays, intersatellite links, WiMAX, high resolution radar, directed-energy weapon (Active Denial System), Security screening (Millimeter wave scanner)
12	THF	300 to 3000 GHz	0.1 to 1 mm	Terahertz radiation, submillimeter radiation, low Infrared

While at the same time IEEE has another set of frequency allocation and naming which is used frequently in radar application.

Table 3-2 IEEE Radio Bands

Band	**Frequency range**	**Origin of name**
HF band	3 to 30 MHz	**H**igh **F**requency
VHF band	30 to 300 MHz	**V**ery **H**igh **F**requency
UHF band	300 to 1000 MHz	**U**ltra **H**igh **F**requency
L band	1 to 2 GHz	**L**ong wave
S band	2 to 4 GHz	**S**hort wave
C band	4 to 8 GHz	**C**ompromise between S and X
X band	8 to 12 GHz	Used in WW II for fire control, X for cross (as in crosshair)
K_u band	12 to 18 GHz	**K**urz-**u**nder

K band	18 to 27 GHz	German **K**urz (short)
K_a band	27 to 40 GHz	**K**urz-**a**bove
V band	40 to 75 GHz	
W band	75 to 110 GHz	**W** follows V in the alphabet
mm band	110 to 300 GHz	

In general, higher frequency electromagnetic wave has high resolution due to its smaller wavelength, but shorter detection range due to its higher attenuation. In this unmanned aerial vehicle (UAV) radar, the X band which is around 10GHz fits the application well in terms of detection range and resolution.

3.1.2 Basic terminologies

The detection range of radar is calculated by travelling time of round trip

$$\boldsymbol{R = \frac{cT}{2}} \tag{3-1}$$

where c is light velocity, T is the radar wave travelling time, R is the range between radar and object.

The detection range resolution is defined as minimum range difference radar can distinguish. Obviously for conventional pulse radar which transmits the pulses with width τ, the range resolution is

$$\boldsymbol{\rho = \frac{c\tau}{2}} \tag{3-2}$$

Usually pulse bandwidth B is the reciprocal of τ, therefore Eq. (3-1) equals to

$$\boldsymbol{\rho = \frac{c}{2B}} \tag{3-3}$$

Eq. (3-3) is actually general expression of range resolution regardless of the modulation or pulse shape.

Doppler effect is the frequency changing phenomenon which happens when observer moves relative to wave source. In radar applications, either object/target is moving or radar is moving (UAV). Doppler effect is actually took advantage of in order to estimate the moving speed of target.

$$\boldsymbol{f = \left(\frac{c+v_r}{c+v_s}\right) f_0} \tag{3-4}$$

According to Eq. (3-4), the observed frequency of incoming signal changes with velocity of both observers and targets. v_r is the velocity of receiver relative to medium and v_s is the velocity of source (radar) relative to medium. Once the frequency is obtained, one can back calculate the moving velocity.

Another important specification in radar system analysis is radar cross section (RCS). RCS represents how much area a target from the point view of radar. By definition RCS is

$$\sigma = \lim_{R\to\infty} 4\pi R^2 \frac{|E_s|^2}{|E_0|^2} \tag{3-5}$$

E_0 is electrical field strength of incident wave on target; E_s is electrical field strength of scattered wave at the radar. RCS even varies with different incident wave angle. The following table shows the typical number of RCS at X band.

Table 3-3 Typical X band RCS

Targets	Typical RCS (m^2) @ X band
Bird	0.01

Man	1
Automobile	100
Truck	200

To establish radar equation, it is still necessary to know antenna gain. Antenna gain is the multiplication of antenna directivity and antenna efficiency. It measures the ability of an antenna to focus power in desired direction. According antenna theory, antenna gain is defined as

$$G = 4\pi \frac{U_{\max}}{P_{\mathrm{t}}} \tag{3-6}$$

where U_{max} is the maximum intensity of antenna, P_t is the transmitter power. 4π is solid angle of sphere. Table 3-4 gives an idea how large gain the common radar antenna has. The unit is dB, which is equivalent with dBi, i.e., compared with isotropic antenna radiation power.

Table 3-4 Typical radar antenna gain

Antennas	Typical gain (dB) @ 9GHz
Horn antenna	14
Circular parabolic reflector antenna	50
Monostatic radar	40

At this point, we can establish the radar equation based on the above parameters. Radar equation is actually the link budget analysis of radar system.

$$P_{\mathrm{r}} = \frac{P_{\mathrm{t}} G^2 \lambda^2 \sigma}{(4\pi)^3 R^4} \tag{3-7}$$

where P_t is transmitter power, P_r is receiver power, G is antenna gain because radar system has same transmitter and receiver antenna, λ is wavelength, σ is RCS, R is the range from radar to target. Eq. (3-7) is developed from Friis free space formula. Based on Eq. (3-7), let us assume P_t =2W, G=30dB which is reasonable for monostatic radar, λ=33.33mm@9GHz, σ=50m^2, R=5km, the minimum detectable signal (MDS) is -100dBm. Therefore radar system either transmits much higher power or needs sensitive receiver front-end in order for robust operation.

Traditional radar uses single beam to measure range. This kind of radar is called monopulse radar which was first introduced by Robert M. Page in 1943.

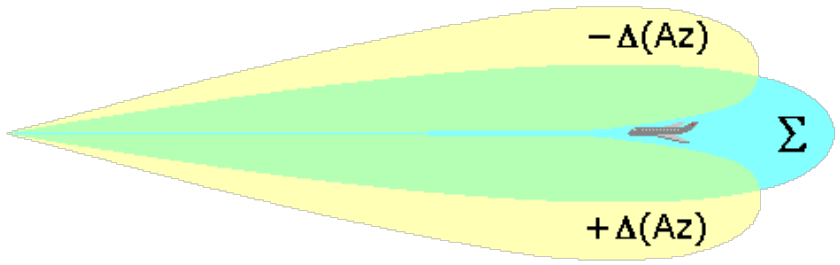


Fig. 3.1 Monopulse radar radiation pattern.

Monopulse radar transmits two separate beams through two different antennas to measure both range and direction of target. Therefore there are two antennas and two receivers. Every pulse is transmitted on both of antennas at the same time, hence, the name monopulse. The two pulses echo signal will be received by two receivers. They are separately amplified and combined. The sum pattern of two beams is used for range detection, and the difference pattern is used for angle detection. Two beams are separated further by orthogonal polarization. Because the polarization is hard to detect, the monopulse radar is hard to jam.

In this research what mostly interests us is UAV radar. UAV means unmanned aerial vehicle, usually there is no human on board. UAV radar is widely used for battle surveillance in that it is safe and convenient to operate, not dangerous to pilots. Hence UAV radar usually is deployed on

aircraft. The operation environment is at a few km elevation. The automobiles and humans on ground often serve as detection target.

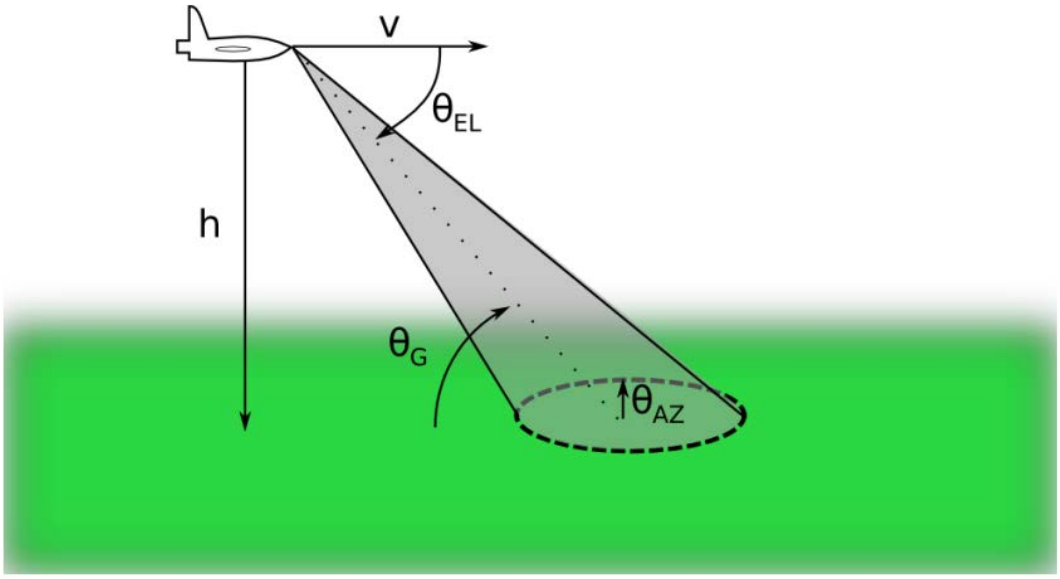


Fig. 3.2 UAV radar.

3.1.3 Pulse compression

Traditional pulse radar sends electromagnetic pulses to detect range and direction. According to Eq. (3-3), the range resolution is proportional to pulse bandwidth, inverse proportional to pulse width. Therefore in order to obtain enough bandwidth, it is required to send pulses as narrow as possible. While at the same time, the transmission energy needs to remain unchanged to combat in band noise. Then the peak power of pulses will become higher with shorter pulse width as shown in Fig. 3.3

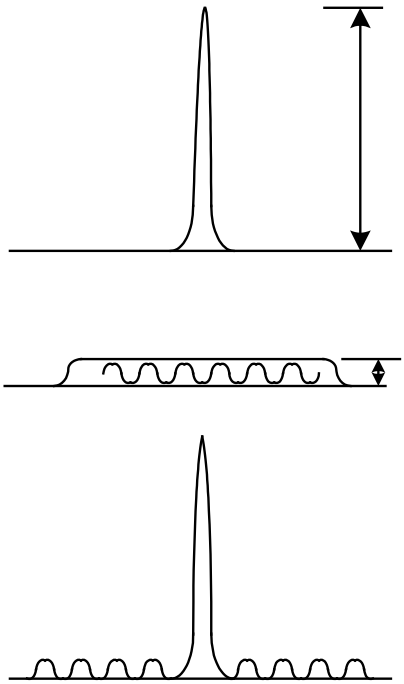


Fig. 3.3 Pulse compression.

Too high peak power imposes stringent requirement to power amplifier (PA) design, sometimes makes the design impossible. A technique called pulse compression was introduced to relieve the difficulty of PA. Pulse compression technique will transmit a wide pulse width signal which is modulated by some mechanism. Hence the bandwidth of signal is comparable to single narrow pulse. The range resolution will not be degraded as shown in middle of Fig. 3.3. After the radar receiver senses the echo signal, the wide pulse will be correlated with local pulse having same waveform. The sharp pulse is then recovered from widened pulse. Precise detection can be achieved through recovered pulses.

There are two classes of modulation techniques which implements the modulation function. One is binary phase coded modulation, the other is linear frequency modulation (LFM). A typical binary phase coded pulse compression uses Barker Code. Barker code has fixed 13 chips length as “1111100110101” as shown in Fig. 3.4.

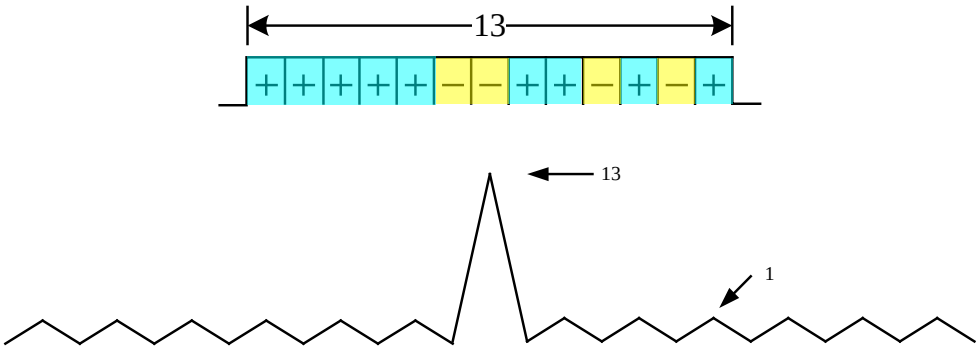


Fig. 3.4 Barker code.

Barker code is such a kind of code whose auto-correlation property exhibits a peak 13 when time difference between two codes is zero. And the other correlation value is 1 if the time lag is more than zero. If we transmit the Barker code as the original pulse, its bandwidth is determined by the chip rate which could be pretty high. After correlation with local another Barker code, the pulse is recovered to a narrow pulse and the range information can be read from the peak position. The peak power of Barker code is equivalent to its average power.

Another type of modulation applied in pulse compression is linear frequency modulation, which is usually called chirp modulation. Chirp modulation starts with a single tone sine wave, then increases the sine wave frequency linearly with time to achieve a wide bandwidth in frequency. Its waveform is shown in Fig. 3.5. From Fig. 3.5, it is shown that frequency of sine wave is linear with time.

The equation describing the modulation is shown in Eq. (3-8).

$$s(t) = A * \sin\left(\omega t + \pi \alpha t^2 + \phi\right) \tag{3-8}$$

Derivative to the term in bracket relative to time is the frequency of signal:

$$\boldsymbol{f = f_0 + \alpha t} \tag{3-9}$$

Obviously the bandwidth of chirp signal is proportional to transmission time.

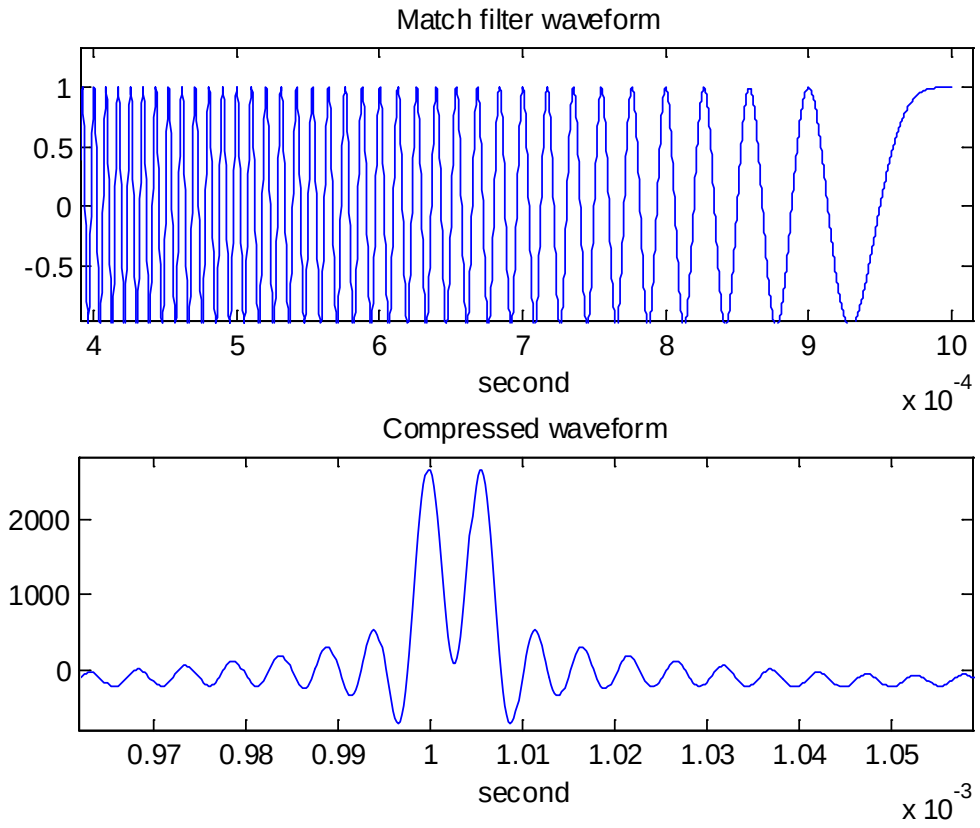


Fig. 3.5 Linear frequency modulation.

Applying the correlation operation at receiver leads to the same pulse compression mechanism as shown in Fig. 3.5. What shown in Fig. 3.5. is two peak detection which means there are two objects close to each other in range. As far as their range difference is larger than resolution, they can be distinguished. The next table summarizes the comparison between two modulation schemes.

Table 3-5 Comparison of linear FM and binary phase coded pulse

Property	Linear FM	Binary Phase Coded Pulse
Sidelobes	~30dB	1/2N

Doppler	Doppler tolerant	Requires filter bank
Pulse compression filter	Analog	Digital
Complexity	Less esp. when stretch	More complex
Application	High resolution	Long pulses
Other	Widely used	Bandwidth limited by A/D converter

Side lobe is generated during auto-correlation, whose strength will interfere with other peaks. Lower side lobe indicates higher sensitivity. From Table (3-5), the side lobe strength relative to main peak is constant for chirp signal, 30dB while it varies with code length for binary code modulation. Hence for short length modulation, chirp modulation can better performance than binary code. Chirp modulation is more tolerant to Doppler frequency effect. Furthermore chirp signal can be processed in analog domain while binary phase modulation is processed by digital signal processing in common cases. Therefore analog to digital (ADC) requirement can be relieved if we adopt some technique like stretch processing, but a high speed ADC must be in stage for binary code modulation. Based on these observations chirp signal achieves much wider application in radar and sonar system design. Besides chirp signal can be easily generated by direct digital synthesis (DDS) circuit. Therefore in this UAV radar, chirp modulation is specified.

3.1.4 Stretch processing

From the previous sections, it is known that the narrow pulse width will be recovered after pulse decompression in receiver. Narrow pulse width in time domain translates to wide

bandwidth in frequency domain. To facilitate the application of digital signal processing, a wide bandwidth ADC is required. Such high bandwidth imposes difficulty in implementing ADC. To make the pulse compression feasible, a technique called stretch processing can be used. Stretch processing multiplies the echo chirp signal with a local replica of chirp signal, instead of auto-correlation with the local chirp signal. [32]

Eq. (3-8) represents the transmitted chirp signal. The signal echo received by radar is

$$\boldsymbol{r(t) = A * sin[\omega(t-\tau) + \pi\alpha(t-\tau)^2 + \phi]} \tag{3-10}$$

The product of Eq. (3-8) and (3-10) is

$$\boldsymbol{r(t) = \frac{A^2}{2} * sin[\omega\tau + 2\pi\alpha t\tau + \varphi]} \tag{3-11}$$

where the high frequency component is filtered out. Eq. (3-10) shows a typical single tone sine wave whose frequency is related to time delay $\boldsymbol{\tau}$. Therefore the range information is stored in frequency offset. The wideband chirp signal is transformed into narrow band while maintains the range information in frequency domain.

The operation principle is visualized in the next diagrams.

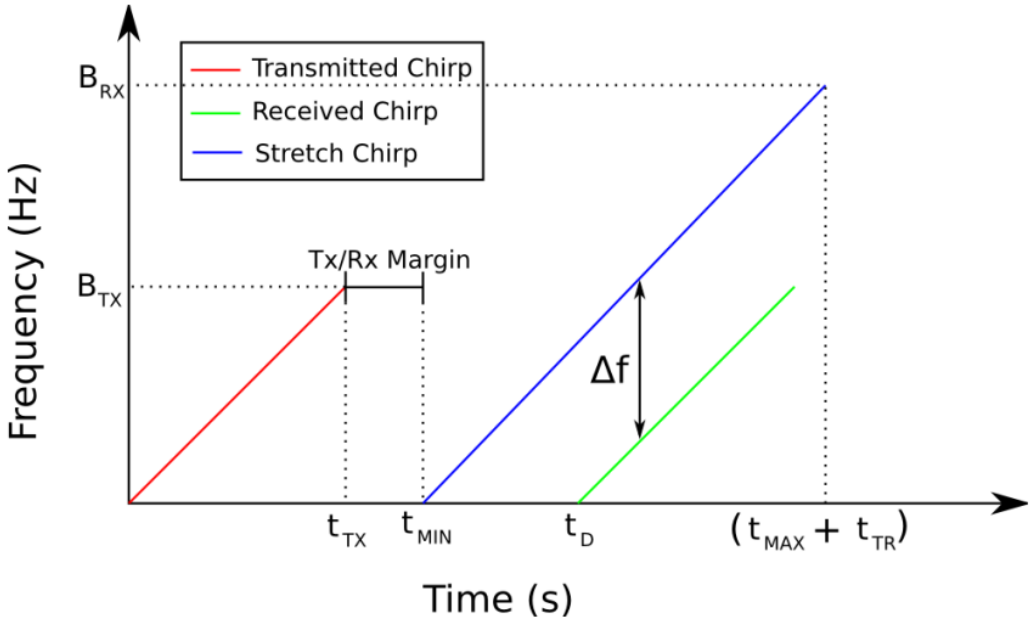


Fig. 3.6 Stretch processing.

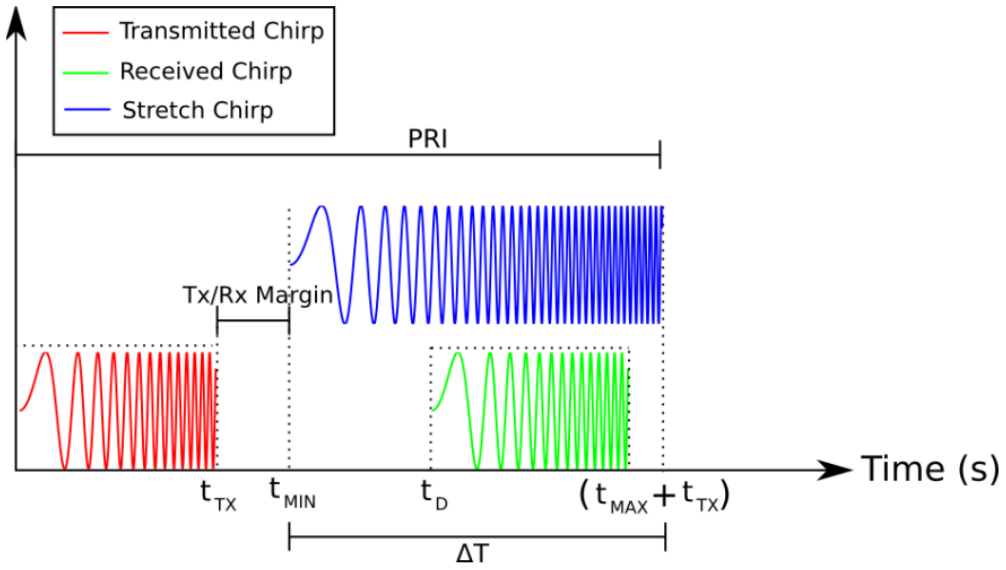


Fig. 3.7 Stretch processing waveform.

X axis represents the time index. From time zero to t_{TX} a linear frequency modulation signal is sent out from radar transmitter. The TX/RX margin is the time interval during which the closest target would reflect the chirp signal. From t_{MIN}, the local chirp modulator (e.g. DDS) generates a longer chirp pulse starting with zero frequency, which is labeled as blue color in diagrams. The green waveform is received chirp signal. Fig. 3.6 shows that larger t_D corresponds larger Δf. A simple stretch processor is shown Fig. 3.8.

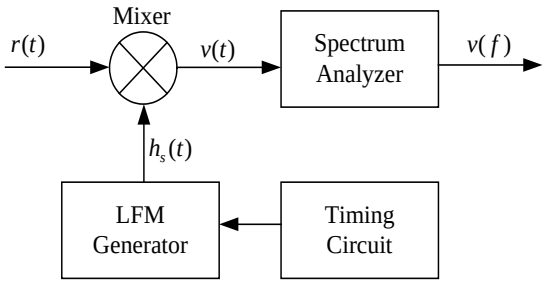


Fig. 3.8 Stretch processor.

The range resolution of stretch processing is

$$\frac{c}{2\alpha T} = \frac{c}{2B} \tag{3-12}$$

where T is chirp pulse width, B is the frequency bandwidth. The ADC must have a sampling rate higher than $2\alpha R\frac{2}{c}$, where R is the range interval defined as the desired detection range.

Although stretch processing alleviates the tradeoff between range resolution and ADC sampling rate, the range interval is limited by system bandwidth.

$$\boldsymbol{R = (T_{RE} - T_{TR})\frac{c}{2} = \frac{B_{RE} - B_{TR}}{\alpha}\frac{c}{2}} \tag{3-13}$$

B_{RE} is the chirp signal bandwidth used for stretch processing, B_{TR} is the transmitted chirp bandwidth. Since B_{TR} is limited by resolution requirement, the range interval is limited by local chirp signal bandwidth. The highest bandwidth chirp signal can reach is determined by generator, e.g., DDS in our research.

3.2 UAV radar transceiver architecture with stretch processing

3.2.1 UAV radar transceiver architecture

Fig. 3.9 shows the radar system architecture.

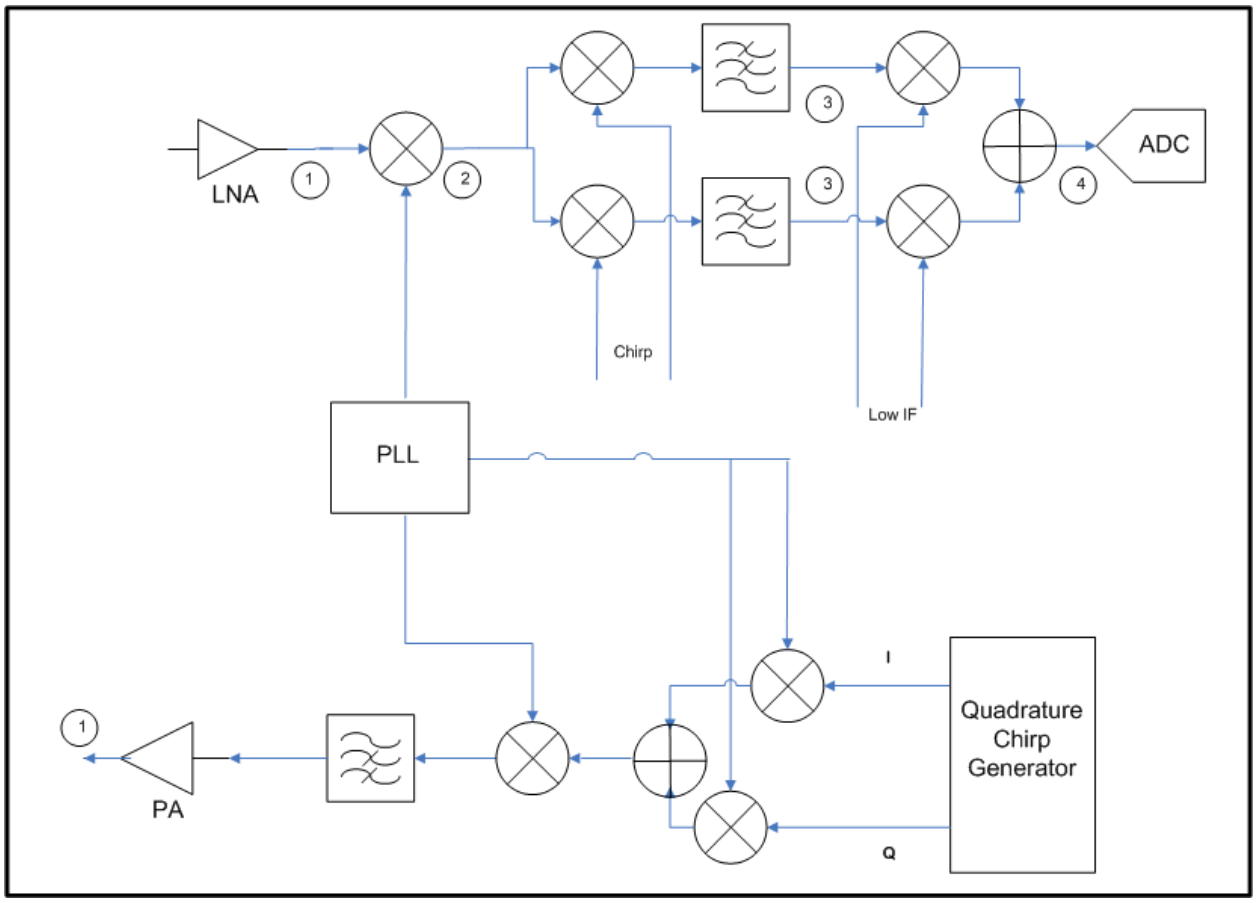


Fig. 3.9 Radar architecture with stretch processing.

The operation of stretch processing radar transceiver is much self-explained by the waveform equations at different nodes labeled in the above diagram. In this RoC transceiver, in-phase and quadrature chirp signals are generated by DDS and up-converted to 10GHz (X band) by two-stage super-heterodyne structure. Node 1 denotes the LNA stage which receives the target reflecting waveform as Eq. (3-14)

$$\cos(\omega_c t + \pi\alpha t^2 + \phi) = \cos(\omega_c t + \phi)\cos(\pi\alpha t^2) - \sin(\omega_c t + \phi)\sin(\pi\alpha t^2) \qquad (3\text{-}14)$$

Eq. (3-14) represents a SSB modulated chirp signal, where f_c is the carrier frequency, α is the chirp frequency modulation rate.

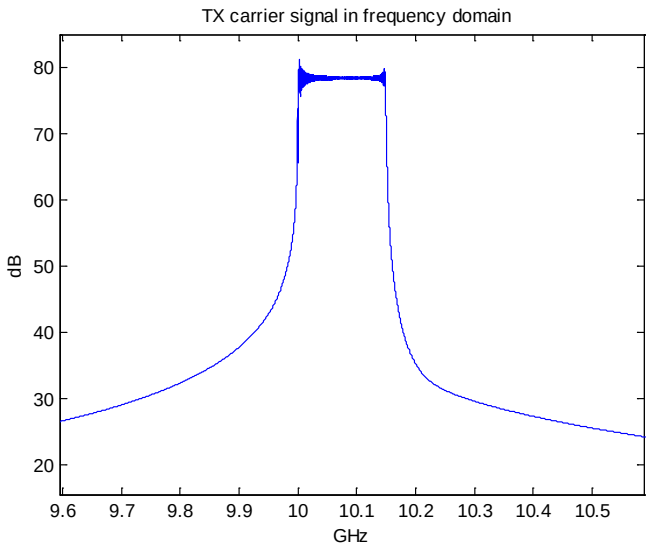


Fig. 3.10 Spectrum of modulated chirp signal.

Node 2 is the RF to intermediate frequency conversion. At node 3 the stretch processing is applied by a pair of quadrature mixers. At the same time the carrier frequency is converted to DC. The operation can be explained by the following mathematical derivation:

$$
\begin{aligned}
&\left[\cos(\omega_{IF}t+\phi)\cos(\pi\alpha t^2)-\sin(\omega_{IF}t+\phi)\sin(\pi\alpha t^2)\right]\times\cos(\pi\alpha(t+\tau)^2)\times e^{j\omega_{IF}t}\\
&=\cos(\omega_{IF}t+\phi)\left[\cos(2\pi\alpha\tau t+\theta)+\cos(2\pi\alpha t^2+2\pi\alpha\tau t+\theta)\right]\times e^{j\omega_{IF}t}\\
&+\sin(\omega_{IF}t+\phi)\left[\sin(2\pi\alpha\tau t+\theta)-\sin(2\pi\alpha t^2+2\pi\alpha\tau t+\theta)\right]\times e^{j\omega_{IF}t}\\
&=\cos(\phi)\left[\cos(2\pi\alpha\tau t+\theta)+\cos(2\pi\alpha t^2+2\pi\alpha\tau t+\theta)\right]+\sin(\phi)\left[\sin(2\pi\alpha\tau t+\theta)-\sin(2\pi\alpha t^2+2\pi\alpha\tau t+\theta)\right]\\
&-j\sin(\phi)\left[\cos(2\pi\alpha\tau t+\theta)+\cos(2\pi\alpha t^2+2\pi\alpha\tau t+\theta)\right]+j\cos(\phi)\left[\sin(2\pi\alpha\tau t+\theta)-\sin(2\pi\alpha t^2+2\pi\alpha\tau t+\theta)\right]\\
&\text{after lowpass filter}\\
&=\cos(2\pi\alpha\tau t+\theta-\phi)+j\sin(2\pi\alpha\tau t+\theta-\phi)+\cos(2\pi\alpha t^2+2\pi\alpha\tau t+\theta+\phi)-j\sin(2\pi\alpha t^2+2\pi\alpha\tau t+\theta+\phi)\\
&=e^{j(2\pi\alpha\tau t+\theta-\phi)}+e^{-j(2\pi\alpha t^2+2\pi\alpha\tau t+\theta+\phi)}
\end{aligned}
\tag{3-15}
$$

where τ is time interval between the beginning of the stretch processing chirp and the beginning of received chirp. Stretch processing chirp starts earlier to ensure the coverage of the received chirp pulse. f_{IF} is the intermediate frequency, ϕ: random phase of the transmitted carrier, θ: random phase introduced during stretch processing. The spectrum can be visualized in Fig. (3-11)

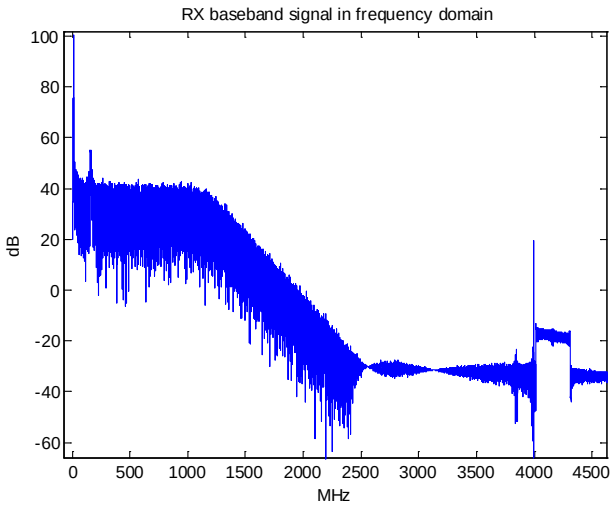


Fig. 3.11 Spectrum of stretch processing signal.

The desired echo appears at close DC band. From Fig. 3.11 it is clearly shown the wideband chirp signal in Fig. 3.10 is reduced to a single tone. In order to use only ADC, the baseband signal is up-converted again to low IF after baseband filtering. Node 4 denotes such an operation explained by Eq. (3-16)

$$\begin{aligned}
&\left[e^{j(2\pi\alpha\pi t+\theta-\phi)}+e^{-j(2\pi\alpha t^2+2\pi\alpha\pi t+\theta+\phi)}\right]\times e^{j\omega_{\text{offset}}t} \\
&=e^{j(2\pi\alpha\pi t+\theta-\phi+\omega_{\text{offset}}t)}+e^{-j(2\pi\alpha t^2+2\pi\alpha\pi t+\theta+\phi-\omega_{\text{offset}}t)} \\
&=\cos\left(2\pi\alpha\pi t+\theta-\phi+\omega_{\text{offset}}t\right)+\cos(2\pi\alpha t^2+2\pi\alpha\pi t+\theta+\phi-\omega_{\text{offset}}t) \quad \text{after output real part}
\end{aligned} \tag{3-16}$$

where first term is the desired tone plus offset frequency f_{offset} facilitating one ADC, the second term is the stretch image that has much lower energy.

3.2.2 Link budget analysis

Stretch processing owns huge processing gain in addition to the ability of reducing bandwidth. In some sense it is similar with pulse compression in frequency domain. The analytical derivation of processing gain can be found in Appendix II. Meanwhile the gain can be

evaluated by simulation. By simulation, we assume 1uW received signal power, 10uW noise power, the sampling rate is 10GHz. Then signal power P_s is 0dBu, noise power P_n is

$$P_n = 10\log 10 + 10\log(\frac{300M \times 2}{10G}) \tag{3-17}$$

300MHz here is the double side bandwidth (DSB) of chirp signal, 2 represents the DSB noise sources. Simulation result shows 20dB signal to noise ratio (SNR) as in Fig. 3.12.

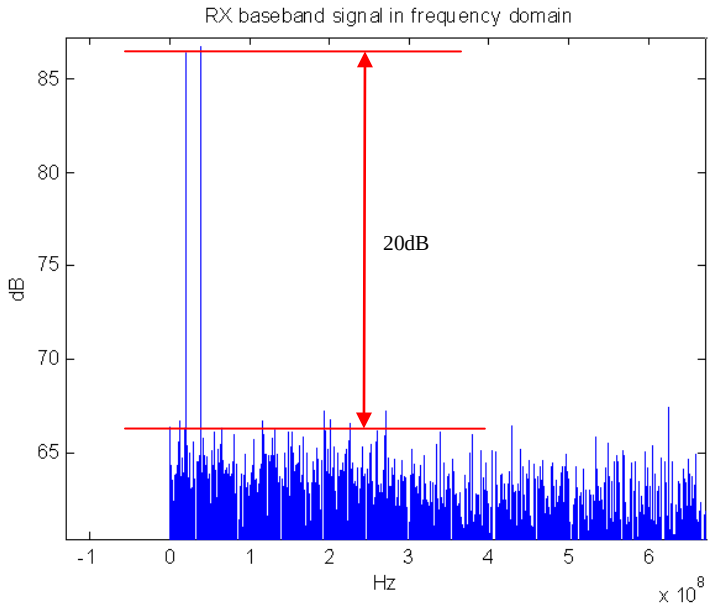


Fig. 3.12 SNR after stretch processing.

The stretch processing gain is

$$\boldsymbol{G = SNR + P_n - P_s} \tag{3-18}$$

Applying all the data above obtains the G=18dB which is pretty close to the theoretical prediction 20dB. The minimum detectable signal (MDS), i.e., sensitivity, is

$$\text{MDS} = -174\text{dBm} + \text{NF} + 10\log\text{BW} + \text{SNR}_{\min} - G \tag{3-19}$$

If we assume at least 4dB SNR can assure reliable single tone detection, the radio transceiver noise figure is 4dB, the MDS is

$$\text{MDS} = -174\text{dBm} + 4 + 10\log 3\times 10^{8} + 4 - 18 = -100\text{dBm} \tag{3-20}$$

3.2.3 Group delay analysis

Linear frequency modulation signal is sensitive to group delay it experiences. Hence the group delay analysis is important to feasibility of chirp radar.

Assuming the phase variation is represented by two order quadratic

$$\boldsymbol{\theta = a\omega^2 + b\omega + c} \tag{3-21}$$

where $\omega = 2\pi\alpha t$. The group delay should be:

$$\boldsymbol{GD = 2a\omega + b} \tag{3-22}$$

The resulting waveform after stretch processing is : $e^{j(2\pi\alpha\tau t+\theta)}$. The frequency of this waveform is:

$$\boldsymbol{\frac{1}{2\pi}\frac{d(2\pi\alpha\tau t+\theta)}{dt} = \alpha\tau + 4a\pi\alpha^2 t + b\alpha} \tag{3-23}$$

within which, $b\alpha$ is a constant shift, while $4a\pi\alpha^2 t$ will vary with time and extend the spectrum. Therefore the time resolution will be degraded to

$$\boldsymbol{\frac{\alpha\tau+4a\pi\alpha^2 t}{\alpha} = \tau + 4a\pi B} \tag{3-24}$$

where B is the chirp signal bandwidth. The range resolution will be degraded to

$$(\tau + 4a\pi B)\times\frac{c}{2} = \tau\frac{c}{2} + 2a\pi Bc \tag{3-25}$$

If the range resolution tolerance is 0.1m, $a = \frac{0.1}{2\pi Bc}$. Then GD variation is

$$GD_{variaion} = 2a\omega_B = \frac{0.1}{\pi Bc}\times 2\pi B = \frac{0.2}{c} \approx 666\text{ps} \tag{3-26}$$

One can apply the principle to different assumptions easily.

3.3 PA driver design for X band RoC application

3.3.1 PA driver circuit consideration

Power amplifier driver is the device which drives the power amplifier and acts as the inter-stage between transmitter circuit and power amplifier. For most applications, the linearity is critically concerned, so class A power amplifier is required. So does PA driver. The PA driver topology we designed is similar as following diagram depicted.

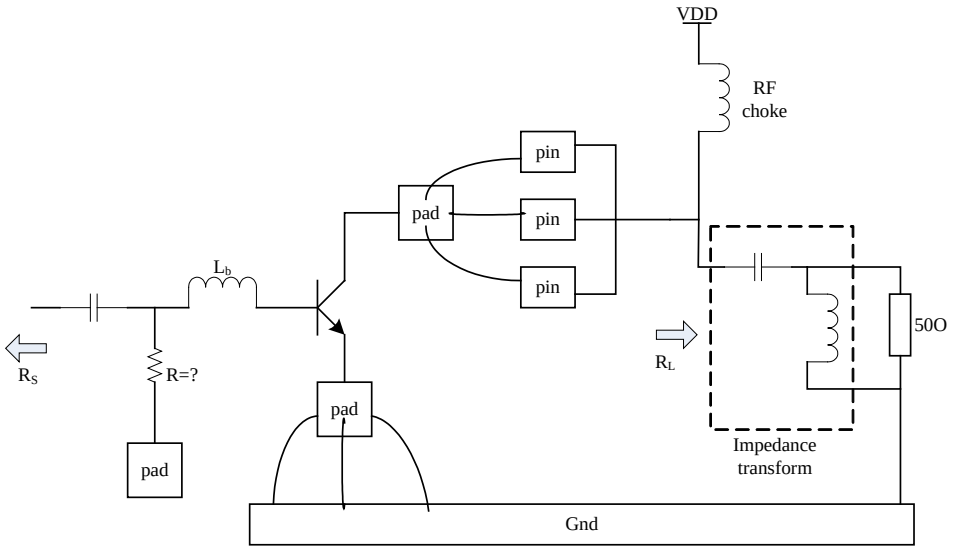


Fig. 3.13 PA driver topology.

Usually PA design follows the method of load line contrary to what is known as impedance conjugate match. Impedance conjugate match gives out the maximum output power with large voltage swing. The large swing will break down the transistors, especially in modern deep sub-micron technology. Load line is adopted to avoid device break down.

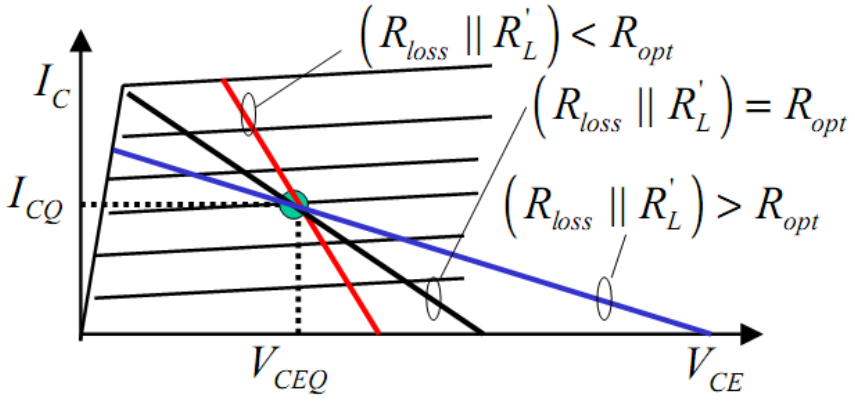


Fig. 3.14 I-V curve defining load line design.

In the above diagram, Icq is the quiescent current, Vceq is the DC bias voltage applied at collector/drain. The optimal load impedance is the ratio of the allowable voltage swing to Icq, which is visualized by the slope of black line in Fig. 3.14. If load impedance is smaller as red line, the current clipping will occur before voltage clipping; if load impedance is larger than optimal value as blue line, voltage clipping may occur and device suffers the possibility of beakdown.

The power is supplied from outside because the availability of high Q and large value inductance as RF choke. The gain for this amplifier can be expressed as below if input is matched

$$G = \frac{\omega_T^2 R_L}{\omega^2 R_S} \tag{3-27}$$

The first priority in designing PA or PA driver is to specify the current requirement and load impedance. Our target is to achieve larger than 0dBm output power to a standard 50Ω load. Since the power requirement is mild, we can consider avoid using impedance transform. Let's assume current is 16mA, the saturation power this driver can deliver is 8dBm which meets the requirement enough. In this case, the voltage swing at the output is $16mA \times 50\Omega = \pm 0.8V$. Plus

any power supply, this voltage will break down high f_t HBT transistor whose BVceo is 1.6V in the technology used. Hence the mixed cascode topology is adopted like shown in Fig. 3.15. [33]

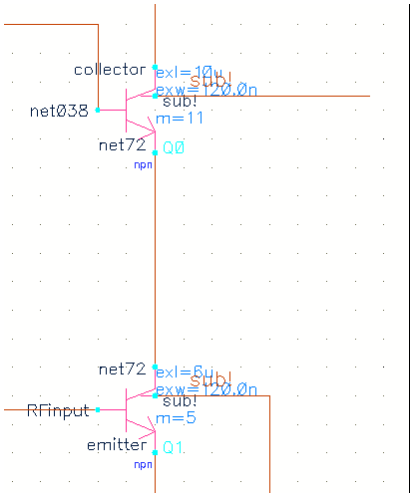


Fig. 3.15 Cascode topology of PA driver.

The upper transistor is high breakdown transistor since it does not provide gain while needs to sustain high voltage swing. The bottom transistor is high f_t transistor to implement amplifier function. In order to bias the transistor in its peak f_t current density, the bottom transistor is made to be wide, large enough to cover peak current when RF signal swings. In principle, the upper transistor should be 8 times of bottom since its peak ft current density is 8 times less. Hence it should be wider. But that wide transistor would incur oscillation under high current condition. As a result, a width which doesn't oscillate transistor is chosen though this size will push transistor to work over peak ft current region in big power. But for 2.2V power supply, voltage swing is $2.2 \pm 0.8 = 3$ or 1.2V, which is safe for high breakdown transistor.

In order to model real physical phenomenon as accurate as possible, a lumped element model of bonding wire is used in simulation as shown in Fig. 3.16. The critical inductance and resistance value are listed in Table 3-6. The inductance of bonding wire makes up a critical factor deteriorating the PA driver performance, especially make the bottom transistor easier to

break down because this PA driver works in 10GHz frequency. For this reason six downbonds are connected to emitter to reduce parasitic inductance, and three downbonds to short base of cascode transistor to ground, and three wirebonds as the collector output.

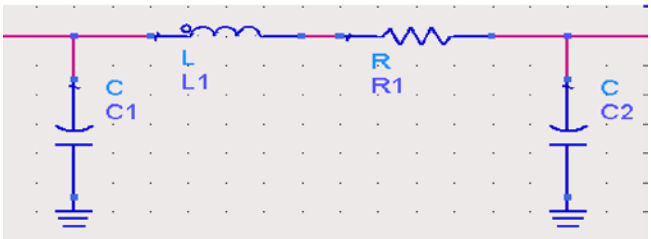


Fig. 3.16 Bonding wire model.

Table 3-6 Inductance and Resistance of bonding wire

Proj Length (um)	simulated Ind (nH)	Model Ind (nH)	%
300	0.6378	0.6382	0.1%
500	0.8039	0.7999	0.5%
700	0.9646	0.9771	1.3%
900	1.1460	1.1541	0.7%
1100	1.3000	1.3323	2.5%

Proj Length (um)	Simulated Res (Ohm)	Model Res (Ohm)	% model vs simulation
300	0.204	0.200	2%
500	0.229	0.224	2%
700	0.254	0.251	1%
900	0.276	0.279	-1%
1100	0.299	0.307	-3%

3.3.2 Simulation and measurement results

The simulation is carried out over extracted layout. Fig. 3.17 shows the group delay of S21, which is relatively flat around 10GHz band. Over 2GHz bandwidth the group delay only varies 20pS, much less than the requirement predicted by Eq. (3-26).

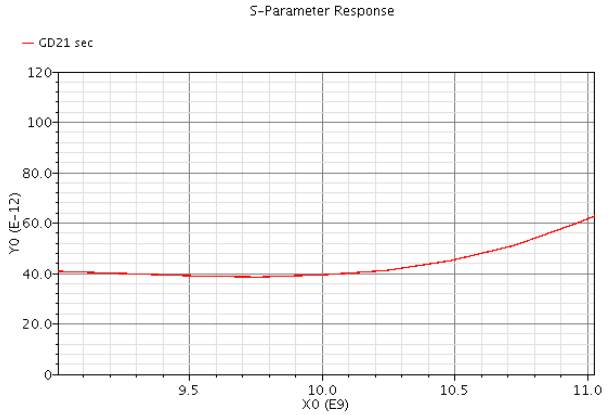


Fig. 3.17 Group delay.

Fig. 3.18 shows the P1dB point from PSS simulation. The input P1dB is almost -7.5dBm, output P1dB is at 8.79dBm. Fundamental gain is about 17dB. Both output power level and power gain meet the RoC requirement.

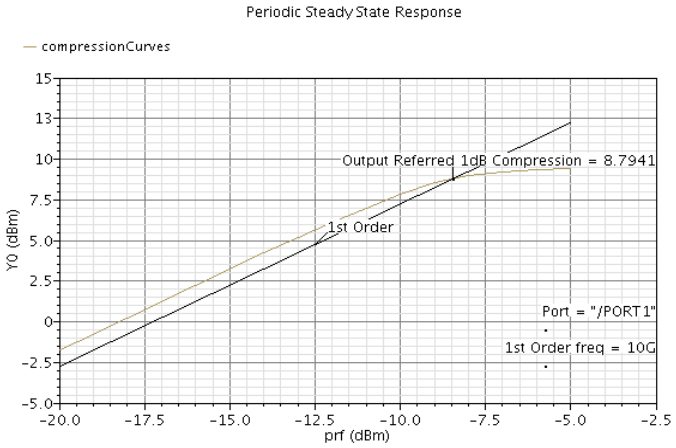


Fig. 3.18 P1dB of PA driver.

The simulated power added efficiency (PAE) is exhibited in Fig. 3.19. The PA driver maintains around 10% PAE with normal input power level, which is typical for class A amplifier. The simulated S parameters are shown in Fig. 3.19. Fig. 3.19(a) shows the S11 parameter is less than -7.5dB at 10GHz; Fig. 3.19(b) shows the S21 parameter is around 17dB at 10GHz.

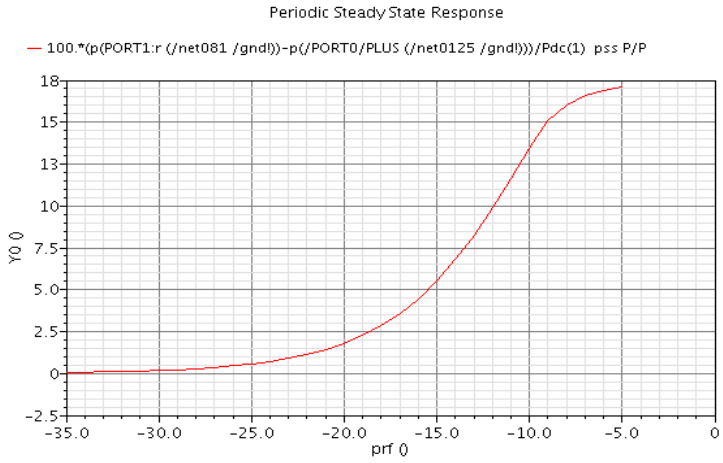
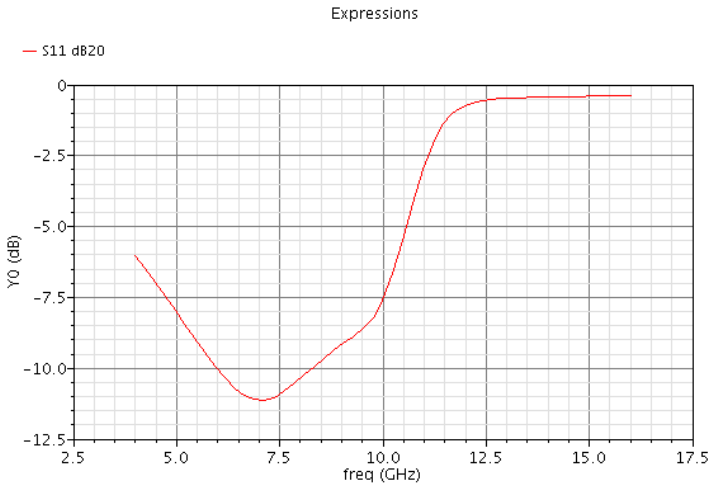
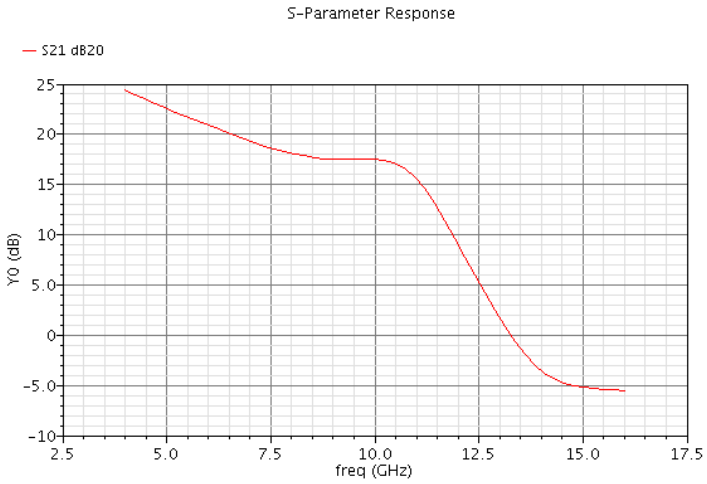


Fig. 3.19 PAE of PA driver.



(a)



(b)

Fig. 3.20 Simulated S11 and S21 of PA driver.

3.4 Conclusion

This chapter summarizes the theoretical work on radar on chip system bases on stretch processing. Simulation results are given out accompanying the theoretical analysis. Stretch processing radar is able to achieve lower bandwidth without sacrificing the range resolution. A 10GHz power amplifier driver is also presented and simulated results are approved to meet the X band RoC specifications.

Chapter 4 LMV cell Front-end

4.1 Introduction

This chapter presents a novel RF receiver front-end using only one shared tail current for low power application. The 5GHz receiver front-end RFIC includes a voltage controlled oscillator (VCO), a double balanced mixer and a low noise amplifier (LNA) in a cascoded topology. The receiver RFIC was implemented in a 0.5um SiGe BiCMOS technology. The VCO oscillation frequency is around 5GHz, targeting at the WLAN 802.11a application. The VCO phase noise was measured around -105dBc/Hz at 1MHz frequency offset. Intermediate frequency (IF) output is centered at frequency of 600MHz using a low-IF architecture and the conversion gain is measured more than 15dB. The 1dB gain compression point and sensitivity of the front-end is measured greater than -14dBm and smaller than -60dBm respectively. The front-end core consumes 3.3mA current from a 3.3V power supply and occupies 1.4mm^2 area.

An everlasting trend in modern RFIC design is to reduce power consumption and shrink die size without performance degradation. Especially the increased demand for wireless personal area network (WPAN) and wireless local area network (WLAN) application accelerates the need for power saving circuits because these applications are often battery-powered. Modern smart cell phone tends to integrate multiple standards, e.g., Bluetooth, WLAN, GPS etc into one system. All these applications are power hungry and supplied by battery. Low power design is becoming more important in modern RF IC design, even first priority in some scenarios. In additional, the low power design is small area design sometimes.

There are two methods to lower RF front-end power consumption: one is to lower power supply voltage, the other is to reduce current. For the former one, the supply voltage decreases with MOS transistor size scaling down naturally. According to Moore's law, the transistor size shrinks 30% for every generation of technology [34]; hence the supply voltage will reduces 30% to maintain the same electrical field.

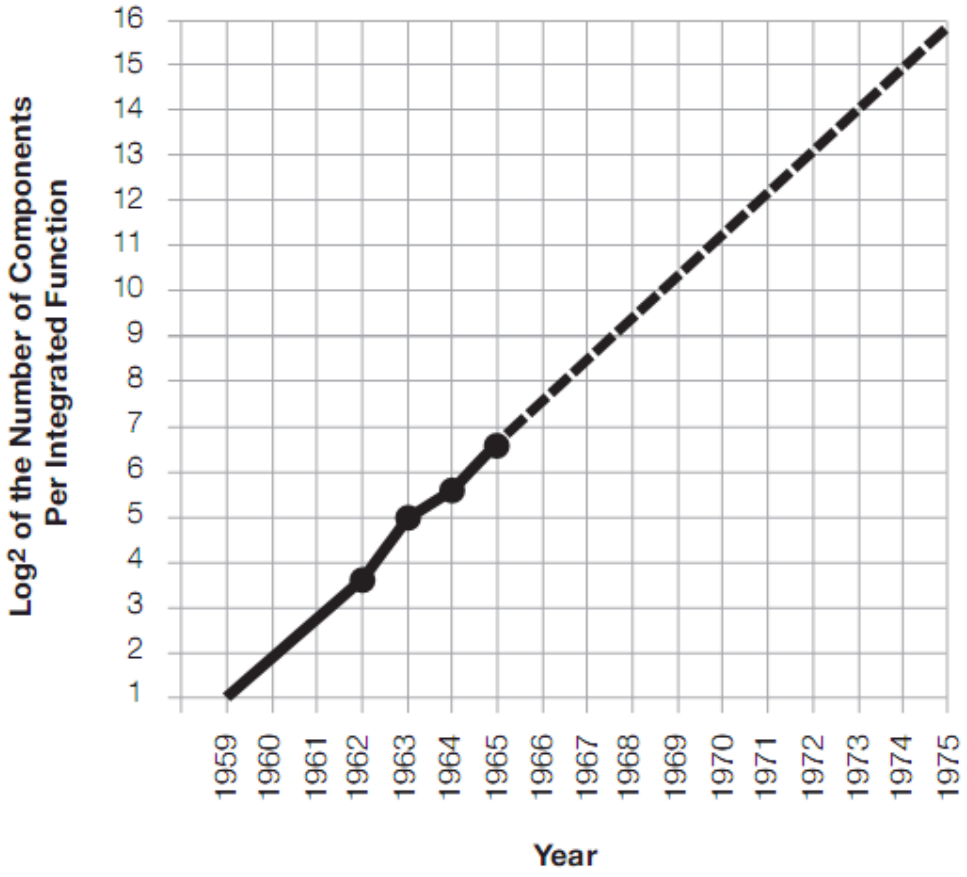


Fig. 4.1 Moore's Law.

To further reduce the power supply voltage, a folded topology is usually adopted in that it eliminates the load of a non-folded stage. However, this topology needs more tail currents and thus may not end up with lower power consumption. For the latter method, a popular method is

to stack different RF building blocks on top of each other and allow sharing of the bias current. Because of the current reuse, power consumption is greatly reduced.

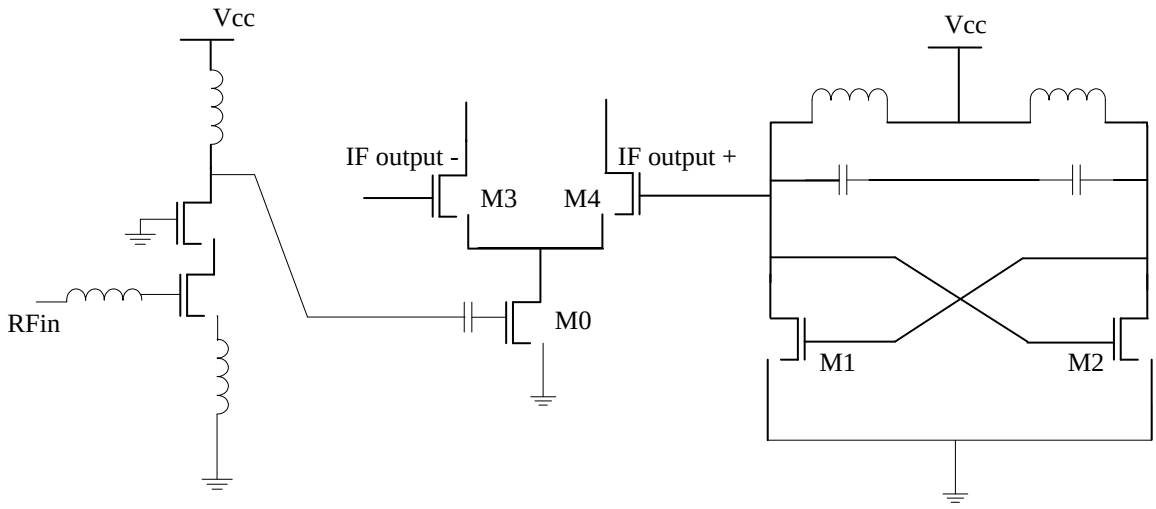


Fig. 4.2 Conventional RF Front-end.

Shown in Fig. 4.2 is the conventional RF receiver front-end circuit. The received RF signal applies the gate of LNA transistor and is transformed into current; then the RF current flows through the LNA load and exhibits itself as voltage swing; the voltage signal is sensed by transconductance transistor M0 of mixer and turned into current again. Besides the signal path, LO signal necessary for frequency conversion needs to be generated from a standalone oscillator. To fulfill the front-end functionality, there are at least three independent current tails used in Fig.4.2. The reason of high power consumption here is that this structure transforms signal between voltage domain and current domain back and forth frequently. If the signal can be confined in one domain during processing, the power dissipation could be lower.

Most examples of this structure are cascode low noise amplifier (LNA) combined with a mixer [35]. It was called current-mode cascade of LNA and mixer, or low-noise mixer in the sense that the Gm stage of the mixer is replaced with an LNA. Conventional RF front-end topology consists of back and forth current-to-voltage conversions, e.g., from LNA

transconductance to LNA load in voltage domain, and from mixer transconductance to mixer output in voltage domain. Compared with the conventional topology, the proposed one-tail topology in [35] does not convert signal back and forth from voltage domain to current domain and thus greatly saves power and area.

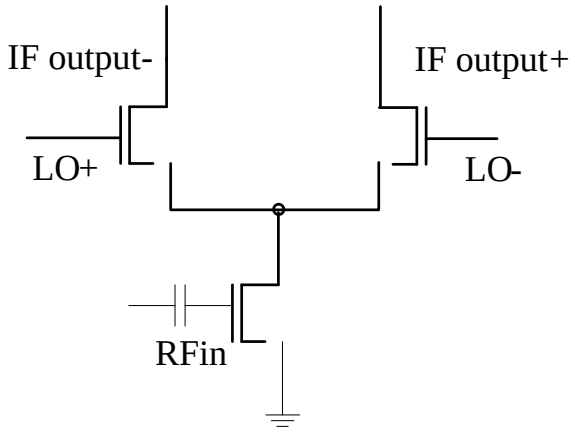


Fig. 4.3 Merged LNA and Mixer.

The current reuse circuit can also stack voltage controlled oscillator (VCO) and mixer [36]. The latest development is to merge LNA, Mixer, VCO in a single current stage that further enhances the current reuse [37-39]. It was called LMV (LNA, mixer and VCO) cell. This chapter proposes a novel structure based on LNA, mixer, VCO stacked topology.

In [38], the LMV cell shown in Fig. 4.5 evolves from self-oscillating mixer (SOM) [37] shown in Fig. 4.4.

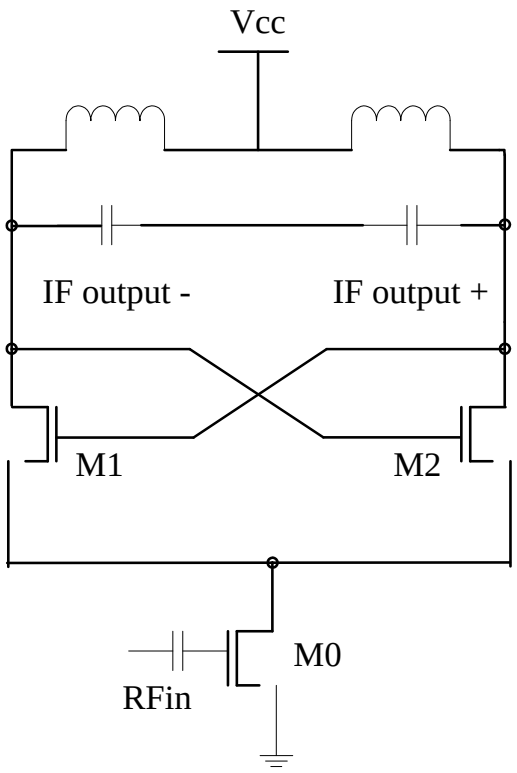


Fig. 4.4 Self-oscillating Mixer.

SOM uses only two transistors (M1 and M2) to fulfill the oscillation function and frequency conversion function when signal current is applied to source/emitter of the oscillator transistors. As shown in Fig. 4.4, the circuit topology looks exactly like a cross-coupled oscillator. Therefore it will generate the LO signal under appropriate bias conditions. On the other hand, if RF current is injected into the circuit from bottom M0 transistor, it will experience the commutating between M1 and M2. The output differential signal is actually frequency converted. Hence this simple topology implements all RF front-end functions and uses only one tail current simultaneously. The down converted signal is amplified on the same load of oscillator which should have maximum gain in LO band but low gain in IF band and even lowered gain in baseband, which results in the low conversion gain. This limitation brings the idea of sensing IF signal at the source/emitter. The topology shown in Fig. 4.5 adds a pair of transistors: M3 and

M4 under the VCO. They explicitly act as the single balanced mixer. The LO signal comes from above oscillator through two coupling capacitors. And IF load between mixer and VCO provides high gain for IF band and exhibits low gain for LO frequency. The tail transistor M0 provides biasing and transconductance for the RF signal. Although the IF load exhibits the low impedance for LO frequency, its resistive component degenerates the VCO. Furthermore it can be inferred that the IF load has capacitive component if its impedance decreases with frequency. Therefore the capacitive value will be seen across the VCO LC tank as parasitic capacitance, whose value will be attenuated by the cross-coupled transistors. Based on this observation, authors fabricated a very low resolution DCO with fine tuning steps [43]. On the other hand, the low input impedance from sources of M1/M2 transistors pair will steer away part of IF current from IF load, hence reduce the conversion gain. Drain of M1/M2 is coupled back to gate of M3/M4, thus making a feedback loop, which makes a potential unstable factor. To ensure the stability, careful parameter design is required.

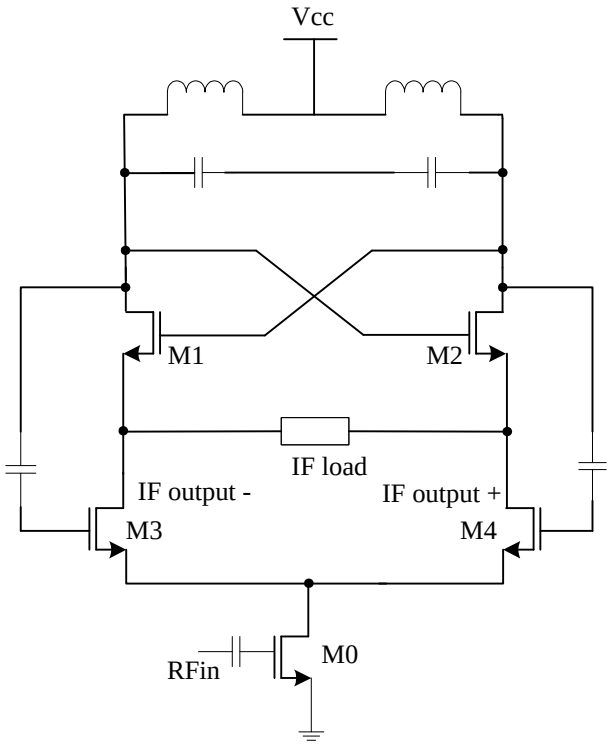


Fig. 4.5 Schematics of the LMV.

In this chapter we propose a double balanced mixer to replace the single balanced mixer and modify the interface between the VCO and mixer. The benefits achieved will be detailed in next section.

4.2 Proposed Single Current Topology

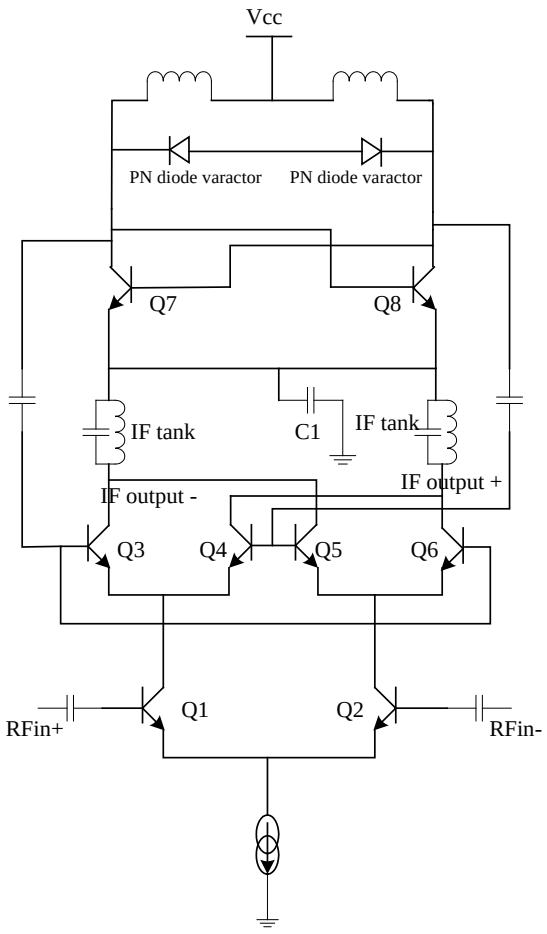


Fig. 4.6 Proposed stack topology of RF front-end.

Fig. 4.6 shows the proposed structure of a current reused RF front-end. On top of the stack is a classic LC tuned differential VCO. LC tank resonant frequency is tuned to 5GHz. Because there is no differential inductor in the chosen SiGe BiCMOS process, we used two single ended inductors here. Integrated inductors usually have much lower Q factor than capacitors, especially

at relatively low operation frequency band. Therefore they are first sized to have peak Q value close to the oscillation frequency. Then varactor size can be determined according to the oscillation frequency, namely Eq. (4-1)

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{4-1}$$

Similarly to the inductor, two varactors are serially connected since there is no differential varactor provided in this technology. The varactor is implemented using base-collector junction, i.e., the SiGe HBT base used as the anode and its collector as the cathode.

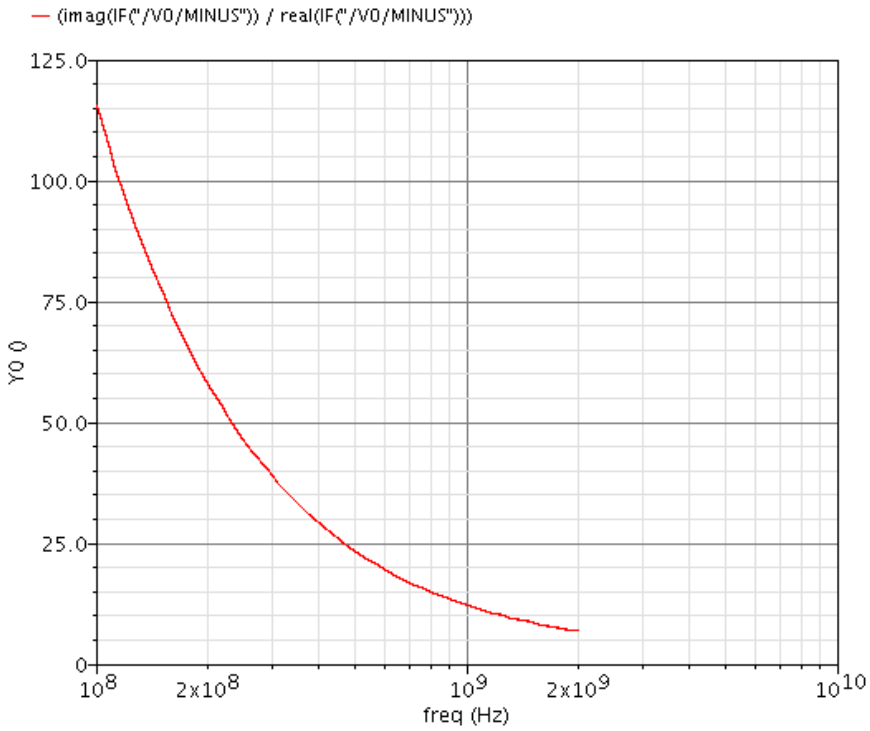


Fig. 4.7 Simulated Q factor of diode varactor.

In this technology, a MOS varactor is also provided, yet it has lower Q and the capacitance value falls quickly when the frequency goes beyond 2GHz. Transistors Q7 and Q8 form the positive feedback loop or –gm resistor to cancel the loss in LC tank. Although stacked on other RF blocks, the VCO is still relatively independent and can be easily incorporated into a phase-locked-loop

(PLL). It can also be built as quadrature VCO (QVCO), e.g. using parallel QVCO structure. Thus, the proposed topology is very flexible. Furthermore the emitters of Q7 and Q8 are shorted instead of an IF load as in Fig. 4.5. This modification returns VCO to its original form. Despite the low impedance exhibited at the LO frequency, the IF load can still degenerate the VCO and increase parasitic capacitance seen across the oscillator's LC tank. The output impedance of M3 and M4 will also influence the VCO. In additional to that, the down-converted IF signal will flow into VCO circuit. With emitter terminal shorted, the VCO operates independently from the other circuits. The transconductance loss and parasitic capacitance associated with IF load are eliminated in the new design. That's the first benefit of proposed topology.

As is known, a single balanced mixer has LO products feeding through to the mixer output. This will impose a stringent requirement on IF load design or the following filter design. Therefore, we replace it with a double balanced mixer with Q3~Q6, providing 40dB LO-IF isolation [40] without the need of a filter. In addition, the double balanced topology reduces clock feedthrough of the mixer. That comes from short connection of outputs of two alternate switching transistors: Q3 and Q5, or Q4 and Q6. Another modification is that the IF load is split into two parts. This improvement makes mixer differential output with a virtual ground at VCO-mixer interface. Hence the input impedance of VCO transistors (Q7 and Q8) has no influence on the mixer conversion gain. Because the IF load is cascode above the mixer and LNA, it will reduce the available voltage headroom. So a pair of LC tanks are substituted for RC tanks as the IF load. The resonant frequencies of the tanks are set to 600MHz. As we know, if the emitter connection of VCO transistors is floating, the voltage is a high frequency signal (usually it fluctuates at double of the oscillation frequency). This common mode voltage will squeeze the headroom of the cascode stages. To keep the VCO-mixer interface as a clean constant voltage, a

decouple capacitor (C1 in Fig. 4.6) is added to AC short the interface to ground. Furthermore any differential current is shorted before it reaches the VCO, then the capacitor feedback loop remains stable in differential mode. The decoupling capacitor C1 ensures that the loop is kept stable for any common mode feedback. Mixer transistors are sized to have maximum transition frequency at the given bias current.

The stage under the mixer is a differential LNA which is composed of Q1 and Q2 transistors. Differential topology can fit easily into a double balanced mixer. And the transistors are sized as 40um such that they have relatively small base resistance value for the purpose of minimum thermal noise. The input RF signal is AC coupled to base of Q1 and Q2. The input impedance matching is obtained on PCB board because of the unpredictable bonding wire inductance. The last stage is the reused current mirror. A bipolar current mirror is chosen here because it has the advantage of less flicker noise than the MOSFET counterparts.

4.3 Measured Results

The stacked 5GHz receiver front-end RFIC was implemented in a 0.5μm SiGe BiCMOS technology with four metal layers. The die microphoto is shown in Fig.4.8.with active area of 1.44mm^2. The top two inductors belong to the VCO LC tank. The tank uses a pair of inductors with 887pH having peak Q value of more than 10 at 4.7GHz. The corresponding varactor was implemented using a collector-base diode and has a Q value of above 60 at 5GHz. The VCO achieves lower than -100dBc/Hz measured phase noise performance at 1MHz frequency offset. The measured oscillation frequency versus the reverse biased tuning voltage is given in Fig. 4.9.

The IF tank inductor has 6.35nH inductance and occupies relatively large area. They have peak Q value at 1.1GHz. The measured differential IF output waveform is shown in Fig. 4.10, indicating a 600MHz IF frequency. The measured conversion gain is above 15dB around

600MHz. The 3dB gain bandwidth is measured across 150MHz band, as shown Fig. 4.11. Because LNA and mixer are cascode and share the same load, only the combined conversion gain can be measured. Basically there is only one gain stage due to LMV cell's cascode topology, hence the conversion gain is unavoidably low. The measured S11 of the LNA is shown in Fig. 4.12. The maximum match is achieved at 5.4GHz with -25dB return loss. Measured P1dB compression point is -14dBm given the high voltage supply. The receiver sensitivity is measured below -60dBm with sinusoid signal from signal generator. Overall performance of the receiver front-end RFIC is summarized and compared in Table. 4-1. Bear in mind that the entire front-end consumes only 3.3mA current under a 3.3V supply, leading to a low power consumption of only 11mW for a 5GHz receiver. Reducing supply voltage further is still possible considering the transistors are mostly HBT bipolar. If the commercial standard digital CMOS technology is used to replace bipolar, considerate power saving could be expected.

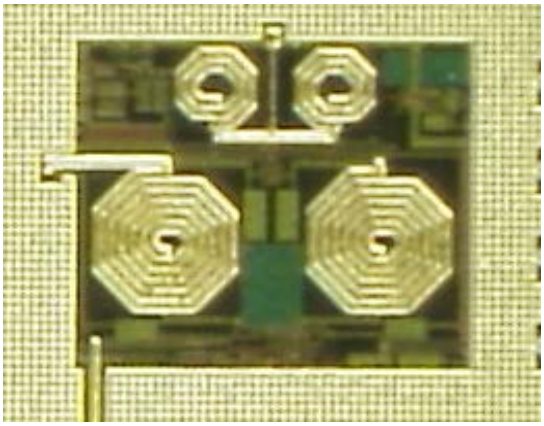


Fig. 4.8 Die photo of the 5GHz receiver front-end RFIC.

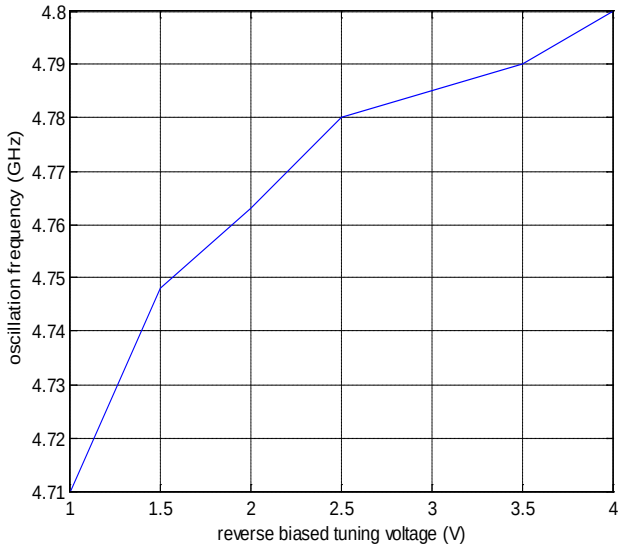


Fig. 4.9 Measured oscillation frequency versus the reverse biased tuning voltage across the varactor.

Fig. 4.10 600MHz IF output waveform under 5GHz LO and 5.6GHz RF input signal.

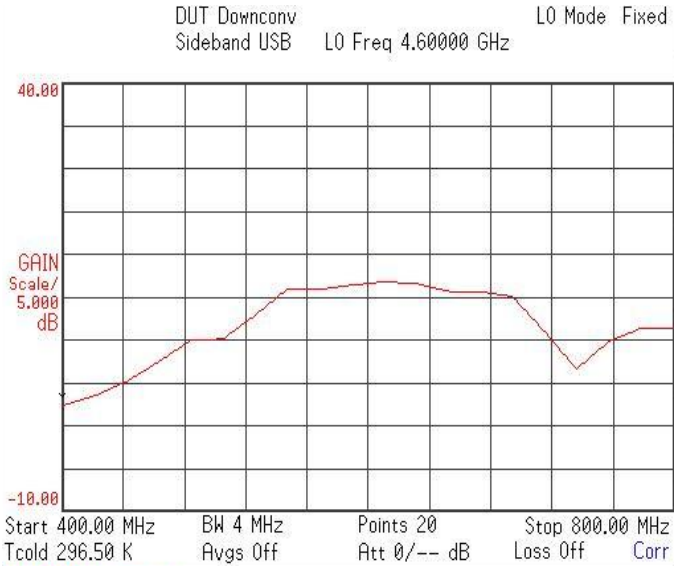


Fig. 4.11 Measured IF conversion gain centered at 600MHz.

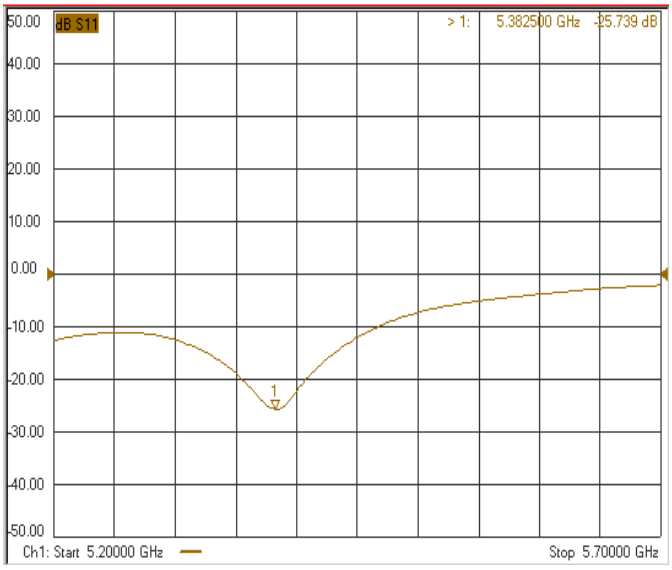


Fig. 4.12 Measured S11 of LNA input.

Table 4-1 Summary and Comparison of Front-End Performance

	[36]	[39]	[40]	**This Work**
Technology	0.13μm CMOS	0.8μm SiGe 50GHz f_T	0.13μm CMOS	0.5μm SiGe 50GHz f_T
RF frequency(GHz)	1.57	5	5	5
Phase noise@1MHz [dBc/Hz]	-104*	No VCO	-115*	<-100
Die size(core)[mm^2]	1.5	4**	6.7**	1.4
Conversion gain[dB]	36***	29/12***	33/N.A.***	>15
1dB compression point[dBm]	-31	-36/-17	-21/-4	-14
S11[dB]	N.A.	N.A.	N.A.	-25
Power dissipation[mW]	5.4	102/90	73.5	11

* PLL included ** dual band transceiver *** IF to baseband stage included

4.4 Conclusion

In this chapter we present a novel topology of stacked RF receiver front-end. The proposed low-power receiver front-end RFIC was fabricated in a 0.5μm SiGe BiCMOS technology. The proposed one-tail topology provides better isolations between the cascode mixer and VCO, and between LO signal domain and IF signal domain as well. The power consumption of the receiver RF core is measured as 3.3mA from a 3.3V supply. The proposed receiver topology with one-current tail provides a low-power solution for mobile networking and space applications.

4.5 Acknowledgement

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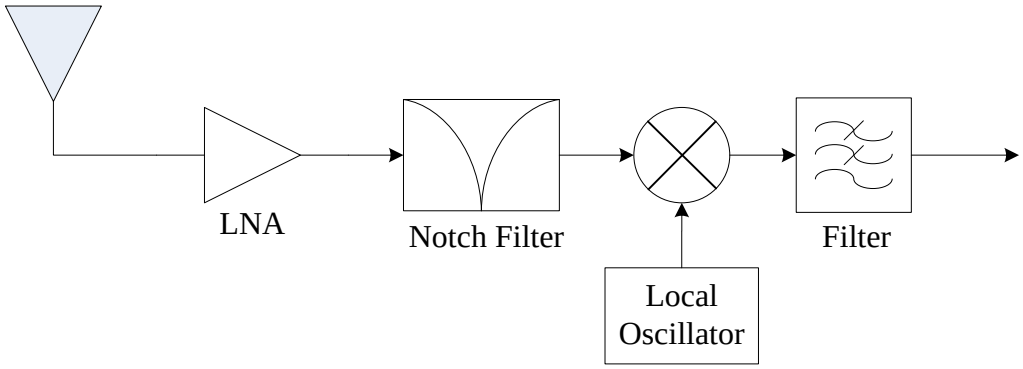
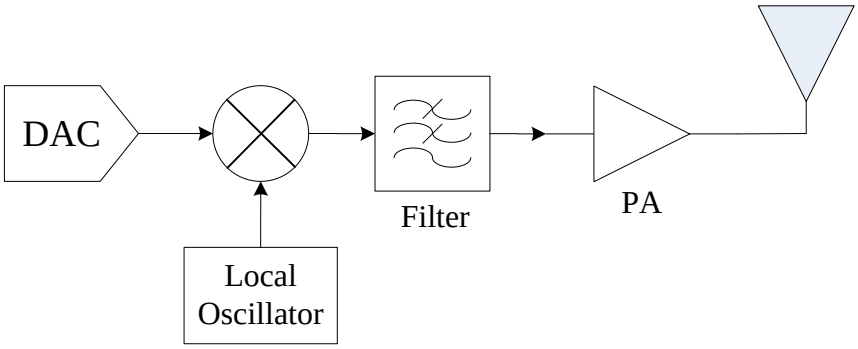
Chapter 5 Harmonic Rejection Mixer

5.1 Introduction

Mixer is an indispensible component in modern radio frequency (RF) systems. It down converts the high frequency modulated signal to baseband or low intermediate frequency in the receiver, and up converts the low frequency data back to RF carrier in the transmitter. As shown in Fig. 5.1, the mixer usually has two inputs: signal and local oscillator (LO) and one output whose frequency is the difference of two inputs. In most receivers, a low noise amplifier precedes the mixer followed by the filter. While in most transmitters the mixer is behind the digital to analog converter (DAC). The LO signal originates from the frequency synthesizer, e.g., phase locked loops in modern RF IC design. As we know, there are various architectures of RF receivers, among which super-heterodyne and homodyne are most popular. Different architectures may impose different requirements and specifications on mixer design.



(a)



(b)

Fig. 5.1 (a) Block diagram of receiver (b) block diagram of transmitter.

Same as other RF circuits, mixer has a few important characteristic. First one is conversion gain, where conversion means that the output and input are not in same frequency band. The gain is defined as the ratio of desired IF output tp RF input (considering receiver case). Active mixer can provide gain more than unity while passive mixer provides loss. The second parameter characterizing mixer is noise figure (NF). Noise figure in mixer usually brings a lot of confusion compared to other RF circuits because it is necessary to identify signal spectrum band when computing the noise figure. If the signal is considered double sideband, the noise figure calculated is double sideband (DSB) noise figure; if the signal is considered single sideband, the noise figure is calculated as single sideband (SSB) noise figure. In other words, one single mixer circuit can measure both SSB noise figure and DSB noise figure depending on the input signal spectrum. Since the output signal to noise ratio in DSB case is 3dB higher than SSB case, the DSB noise figure is 3dB lower than SSB case. The third characteristic of mixer is linearity, which can be quantified by compression point or third order intercept point (IP3). Third order inter-modulation component falls within signal bandwidth, therefore becomes most concern in typical mixer designs. Nevertheless for the mixer applied in homodyne (direct conversion) architecture, second order inter-modulation (IM2) is also a specification to be investigated

because the inter-modulation result of direct feedthrough in-band signal will fall in baseband around DC. Hence the IM2 product will interfere with down converted signal. The harmonics of LO signal also cause the spurious response in output spectrum, degrading the spurious free dynamic range.

5.2 Basic RF mixers

5.2.1 Mixer based on nonlinearity

Nonlinearity could generate new frequency component other than the input signal. There is a type of mixer depending on this nonlinearity of circuits to fulfill frequency conversion functions. More specifically the mixer utilizes the cross-modulation resulting from nonlinearity. This type of mixer usually has only one input port, hence the RF signal and LO signal must be added together before feeding to mixer. For example, if there is a second order circuit:

$$\boldsymbol{V_o = V_i^2} \tag{5-1}$$

and input signal is represented as

$$\boldsymbol{V_i = V_{RF}\cos(\omega_{RF}t) + V_{LO}\cos(\omega_{LO}t)} \tag{5-2}$$

Then the cross modulation component will generate the output as

$$\boldsymbol{V_o = V_{LO}V_{RF}[\cos(\omega_{RF} - \omega_{LO})t + \cos(\omega_{RF} + \omega_{LO})t]} \tag{5-3}$$

We can see to convert the frequency it is enough to have second order nonlinearity. Higher than second nonlinearity does not bring advantages but disadvantages because more harmonics would fold more noise back to desired output frequency and produce more out-of-band spurs. The second order nonlinearity can be implemented by long channel MOS FET whose transfer function follows the square law. Although the mechanism of this type of mixer is nonlinearity operation, the output signal is linear function of input signal in the sense of amplitude, as observed in Eq.(5.3). Another problem associated with nonlinear mixer is the isolation between

the RF signal and the LO signal. Since these two signals should be added together before mixer, the isolation between two signals is much less than the mixer topology with independent RF port and LO port. The RF signal leaked into LO circuit will injection pull the LO; at the same time LO signal leaked to RF part will radiate from antenna and interfere with other radio channels. Therefore the isolation between different mixer ports is important performance metrics.

5.2.2 Active multiplier based mixer

The nonlinearity based mixer depends on the implicit multiplication for frequency conversion. The problem with this method is that it is hard to control the degree of nonlinearity. Hence it is hard to achieve a clean spectrum without spurs. There is another class of mixers which employs explicit multiplication. In circuit diagram, it is usually labeled as a multiplier. Naturally the mixer has two input ports, corresponding to the RF input and LO input. This topology provides superior isolation performance over nonlinearity mixers. Multiplier mixer can be classified into two categories: active and passive. A typical active mixer is shown in Fig. 5.2.

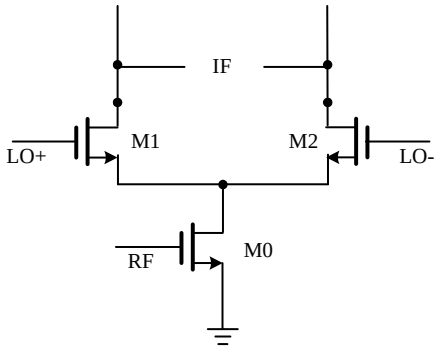


Fig. 5.2 Single balanced mixer.

The mixer is called Gilbert cell [44], and it is active because it has DC current and signal is amplified through the trans-conductance of M0 transistor. The LO signal commutates the current from M0 between M1 and M2 transistor. Equivalently seen from drains of M1 and M2, one can find the RF current is multiplied by a square wave with unity amplitude. Because the DC current

also experiences the current toggling, its frequency would be translated to LO frequency. The LO signal appearing at mixer output is called clock feedthrough and is especially detrimental in transmitters. The transistor M0 acts as an amplifier, therefore it should be optimized based on the criteria of amplifiers. The M1 and M2 will fully switch during operation. LO signal needs to be strong enough to switch them as quickly as possible. At any time there should be only one transistor turned on, thus only one transistor contributes noise at any time. However the sharp transition of LO signal contains plenty of high order harmonics, which is unnecessary for frequency translation. The conversion gain of single balanced mixer is:

$$\boldsymbol{G = \frac{2}{\pi} g_m} \tag{5-4}$$

where $g_m$is the transconductance of M0.

In order to cancel the LO feedthrough to the mixer output port, a double balanced mixer can be used as Fig. 5.3

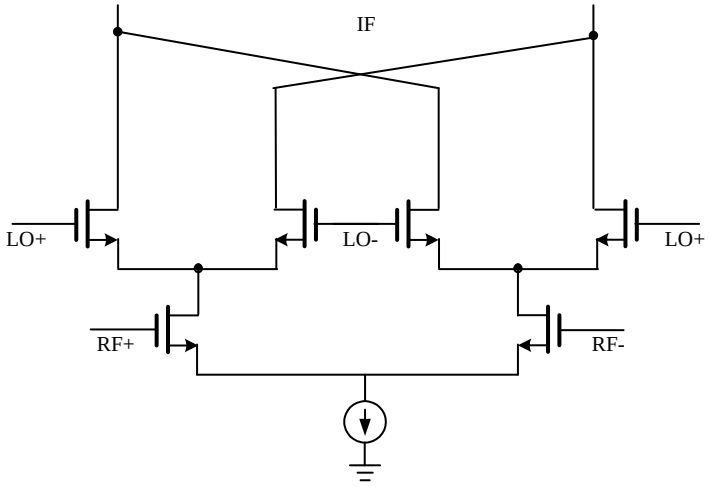


Fig. 5.3 Double balanced mixer.

In this circuit DC current is always split into two branches, therefore the difference current seen at IF port is zero. In practice, due to the mismatch of devices and layout, the double balanced mixer can provide up to 40~60 dB LO to IF isolation. The conversion gain is still

expressed as Eq. (5.4). The double balanced mixer has no even order harmonics of RF signal due to its differential RF input, and greatly helps its IP2 performance. This property is especially useful in homodyne (direct conversion) receivers. The noise of the Gilbert cell mixer firstly comes from amplifier transistors. Since the optimization criteria are similar with those of low noise amplifier (LNA), one can apply the ready procedure of optimizing LNA to mixers. For the switch quad, it is desired that switching time is as short as possible. When both of the switch transistors are turned on, they both contribute uncorrelated noise. Furthermore the low source impedance will enhance the noise contribution from the other transistor. Additionally, the AM noise of LO signal will feed through to IF port when the pair is not fully switched. Due to the frequency translation of mixer and multiple transistors in circuit, the mixer usually achieves much higher noise figure than LNA, typical SSB value varies between 10 to 15dB.

The linearity performance is one concern in mixer design as other circuit design. There are lots of ways of improving the linearity. Because the nonlinearity mainly happens at transconductance stage in Gilbert cell and switch quad plays the role of current unity gain amplifier, the optimization effort focused on the bottom transistors. Common source topology and common gate topology are both adopted in practical mixer designs. For common source circuit, the degeneration inductor is frequently used. For common gate amplify, the source impedance is made as small as possible, thus the linearity is determined by signal source. Another approach is called cross-quad as shown in Fig. 5.4

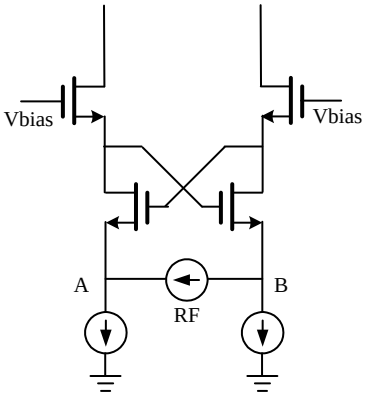


Fig. 5.4 Cross quad linear stage.

The RF signal source can be viewed as a voltage source with the output impedance. In either branch, the Vbe voltage of two cascode transistors will cancel each other's variation as far as the cross coupled pair is in saturation mode. Thus the node A voltage is kept unchanged with respect to RF source, so does node B. This means node A and node B are shorted in the sense of AC. Therefore the current is determined by external RF source and will be buffered to mixer's switch quad.

Schmook proposed a technique to linearize the input stage of operational amplifier (OPAMP). [45] as shown in Fig. 5.5.

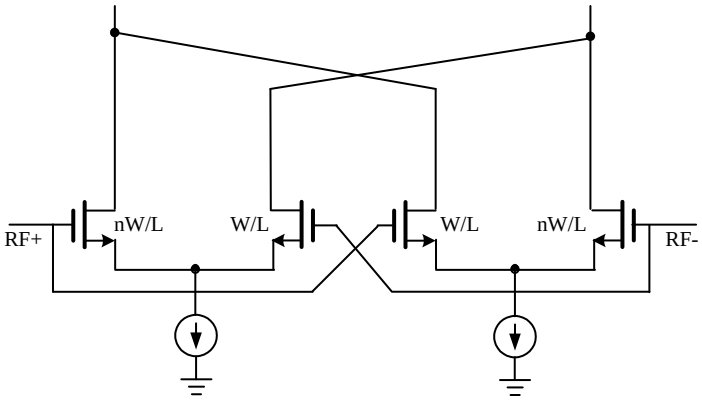


Fig. 5.5 Schmook's linearized pair.

The Schmook input stage is composed of two differential pairs. The left pair has a large transistor and a smaller one. The balanced point (which means balanced current flows through

two branches) is shifted from zero differential input voltage. Thus the maximum transconductance value also occurs at the shifted input voltage. The right side differential pair has opposite weighting factor, therefore its maximum Gm value is shifted to opposite direction. The combination of two Gm curves forms a flattened Gm curve, thus the transconductancec is linearized. Although it was proposed for OPAMP, the method can be applied in mixer input stages.

5.2.3 Passive multiplier based mixer

CMOS process has excellent performance in providing switches. Mixers can be constructed based on switches' on and off states to commutate the RF signals. This topology is called passive mixers because there is no stage to translate voltage signal to current signal through transconductance. The typical passive mixer is in the bridge form as shown in the following diagram:

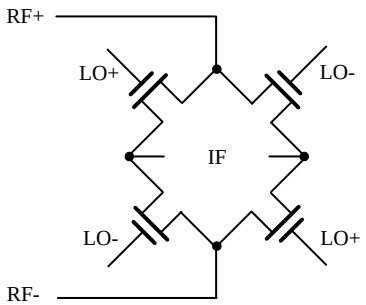


Fig. 5.6 Passive CMOS mixer.

The RF port can either supply voltage or current. Since there is no DC current, the passive mixer is suitable for low power application. And there is no voltage headroom needed, therefore it is also suitable for low voltage application. The circuit will only exhibit the on-resistance of MOS switch. Hence it can achieve quite high linearity. The linearity is mostly determined by external RF source impedance as far as the switch works in deep triode region. Therefore we would like to reduce on-resistance of MOS transistors. From the perspective of noise, the on-resistance

needs to be reduced as well. Another advantage with passive mixers is that it has no flicker noise in ideal cases since flicker noise is related with DC current. This is an attracting property in homodyne receiver design because the output of mixer will fall in DC and low frequency band. The passive mixer is even applied in software defined radio (SDR) front-end [46]. Nevertheless the flicker noise from LO port will appear at output port through limited LO to output isolation.

5.2.4 Sub-sampling mixer

A group of interesting mixers rely on sampling theory of RF signals [47-49]. Sampling of signal in time domain is equivalent with frequency shift of signal in frequency domain. Sub-sampling represents the sample frequency is a fraction of incoming RF signal. The sampled signal has multiple replicas of original input signal with frequency shift which equals to sampling frequency. The operational principle is shown in Fig. 5.7

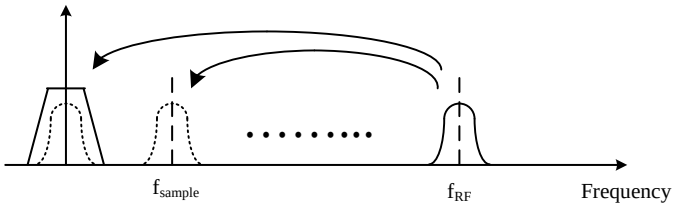


Fig. 5.7 Frequency conversion based on sampling.

A low pass filter is necessary to be cascaded after the sub-sampling mixer to attenuate all out of band signals but signal within Nyquist band. Therefore the baseband is picked up as the frequency converted version of RF signal. The advantage of sub-sampler mixer is the sampling frequency can be much lower than the RF frequency, only a fraction of f_{RF}. Very high operation frequency can be achieved without the use of state-of-art technology. The disadvantage with sub-sampling mixer is it will fold back more noise into baseband or low IF band. Hence a pre-filter is needed to lower out-of-band noise, otherwise the noise figure of sub-sampling mixer reaches more than 25dB (SSB NF) easily. The sub-sampling mixer can be implemented by switches and

capacitors, which makes it a passive mixer as well. Thus it has the typical advantage of passive mixers, e.g., high IP3 performance and low power consumption. The noise of a switch capacitor sampler is determined by the capacitor value.

$$V_{noise}^2 = \frac{kT}{C} \tag{5-5}$$

Bigger capacitance value exhibits less noise voltage, but reduces the speed of the sampler.

5.3 Harmonic rejection mixer

Most of the mixers discussed above share one common problem, i.e., that the harmonics will modulate each other resulting in inter-modulation products within interested frequency band. Both LO signal and RF signal can contribute harmonics. For current commutating mixers, the current switches abruptly between two branches indicating that LO signal applied on LO port has rectangular shape. The rectangular waveform with 50% duty cycle contains plenty of odd order harmonics. RF signal received at antenna usually exhibits less harmonics, but it has various kinds of interference, e.g., multiple channels in the nominal band. DVB-H standard occupies 470 to 862MHz. Interference also comes from out of band when the front end system does not give enough attenuation. GSM standard operates at both 900MHz and 1.8GHz. The inter-modulation products appear at nominal IF or baseband as spurs, and interfere with desired signal. Following table shows a simple example with 500MHz RF input and 400MHz LO, hence the IF is at 100MHz. Only up to 4th order harmonics are considered.

Table 5-1 Spurs of mixer inter-modulation

RF (GHz)	LO (GHz)	IF (MHz)
0.5	0.4	100
1	0.8	200
1.5	1.6	100

0.9	0.8	100
1.3	1.2	100

From the above table, 2nd harmonics of both RF and LO generate IF at 200MHz, which is 100MHz away from nominal IF. However third harmonic of RF signal and 4th harmonic of LO generate IF signal exactly at same frequency. Additionally if the interferences exist at 0.9GHz and 1.3GHz, they will generate the 100MHz IF spurs with 2nd and 3rd LO harmonics. Therefore in order to eliminate the spurs interference, it is necessary to adopt harmonic rejection mixer (HRM) which targets at LO harmonics. There is not much improvement to be done at RF port since it is hard to distinguish RF co channel signals with interference.

Furthermore the harmonic rejection mixer shows the reduction in LO pulling effect and LO feedthrough. The mechanism will be explained later.

Harmonic rejection mixer can be implemented in continuous time domain [50] as shown in the following diagram.

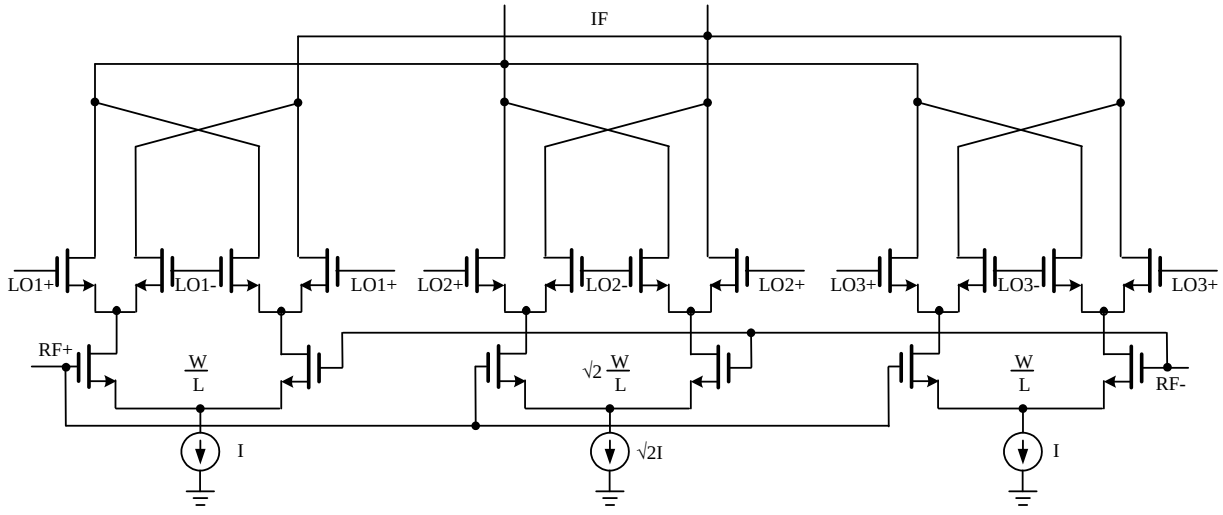


Fig. 5.8 Continuous time harmonic rejection mixer.

The circuit is composed of three active Gilbert switch mixers. They share same RF port but different LO port. The three different LO clocks have 50% duty cycle but with one eighth duty

cycle time lag. Additionally the center branch stage is biased to provide $\sqrt{2}$ times transconductance. Totally the combination of three branches generates an equivalent eight times sampled sinusoidal waveform as shown in the following diagram. From the knowledge of Fourier transformation, it has no 3rd and 5th order harmonics. The most troublesome harmonics are suppressed. 7th order harmonic still exists but the amplitude is smaller.

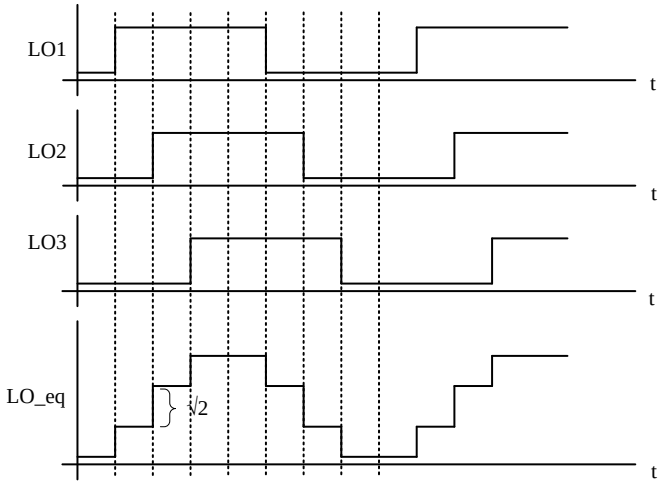


Fig. 5.9 Equivalent LO clock.

Evenly distributed sampling of sinusoidal waveform has phases at $\frac{\pi}{8}$, $\frac{3\pi}{8}$, …, etc. The second branch has $\sqrt{2}$ weighting factor instead of 1, therefore it represents the increment when phases jumps from $-\frac{\pi}{8}$ to $\frac{\pi}{8}$. The cost of this harmonic rejection mixer is it needs three clocks with different time delays. The time lag between two consecutive clocks is one eighth of LO period, thus a clock synthesizer with frequency higher than LO is indispensible. And the mixer LO signals will be generated by an extra clock circuits. Since the autonomous frequency synthesizer works at different speed from LO frequency (RF frequency in direct conversion receiver), the incoming RF signal has less effect on LO pulling.

Harmonic rejection mixer can be implemented in discrete time domain as well [51]. The mixer was based on weighted capacitors for superior matching properties. It was applied in wideband receivers.

In this chapter, a novel discrete time harmonic rejection mixer applied in transmitter is proposed. With the 3rd and 5th order harmonics suppressed, the quality requirement of following RF filter is relieved, which makes the HRM a good choice of on chip mixer in CMOS transmitter.

5.4 Schematic and operational principle

The harmonic rejection mixer based transmitter is shown below:

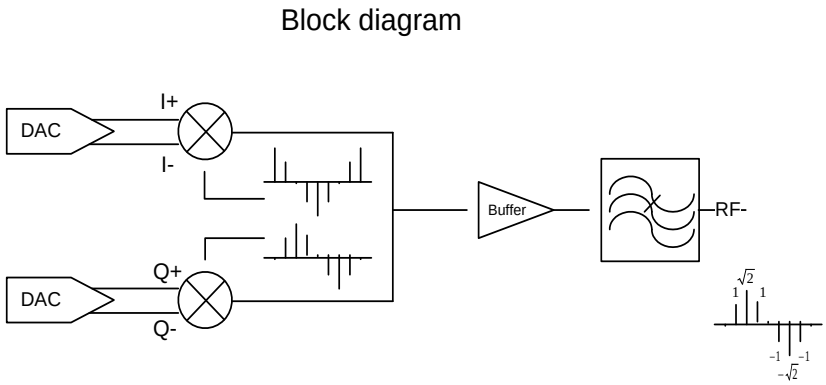


Fig. 5.10 Block diagram of HRM transmitter.

Two quadrature HRMs are cascaded after digital to analog converters (DAC). The quadrature LO clocks are generated by eight phase clock generator and the quadrature-phase is delayed by $\frac{\pi}{2}$ relative to in-phase. The LO clock is eight times sampled sinusoidal waveform with RF frequency. The eight sampling phases are $\left[0, \frac{\pi}{4}, \frac{\pi}{2}, \frac{3\pi}{4}, \pi, \frac{5\pi}{4}, \frac{3\pi}{2}, \frac{7\pi}{4}\right]$. As known, $\sin(0) = \sin(\pi) = 0$. Because of the quadrature property, when in-phase clock amplitude is at maximum value the quadrature LO amplitude is at its zero value, and vice versa. Either in phase HRM or quadrature HRM stops working. Therefore at these instances, $\left[0, \frac{\pi}{2}, \pi, \frac{3\pi}{2}\right]$, the computation load is cut greatly, which can be translated to chip area saving. While at the left

phases, $\left[\frac{\pi}{4}, \frac{3\pi}{4}, \frac{5\pi}{4}, \frac{7\pi}{4}\right]$, in phase clock has same amplitude value as quadrature clock. This property helps improve the match performance between I/Q paths. The digital Fourier transformation of eight times sampled LO is:

$$\mathbf{DFT} = \sum_{n=0}^{7} \boldsymbol{h(n)e^{-jn\Omega}} \tag{5-6}$$

, where $h(n)$=$\left[0, \frac{\sqrt{2}}{2}, 1, \frac{\sqrt{2}}{2}, 0, -\frac{\sqrt{2}}{2}, -1, -\frac{\sqrt{2}}{2}\right]$ is the sampled sinusoidal waveform**,** $\Omega \in [0, 2\pi)$ is the digital angular frequency. The fundamental tone is at $\Omega = \frac{\pi}{4}$; 3rd harmonic is at $\Omega = \frac{3\pi}{4}$; the 5th harmonic is at $\Omega = \frac{5\pi}{4}$; and 7th harmonic is at $\Omega = \frac{7\pi}{4}$. Eq. (2-6) is easily evaluated at these frequencies. The 3rd harmonic and 5th harmonic will disappear, while 7th harmonic has same amplitude as fundamental tone. In practice, sampling circuit will keep the electric charge over capacitors in holding period, thus make the effective LO waveform a step function between consecutive sampling points. The sampled sinusoidal waveform convolving with the step function will attenuate the 7th harmonic. The following diagram shows the frequency conversion and harmonics rejection of proposed HRM transmitter.

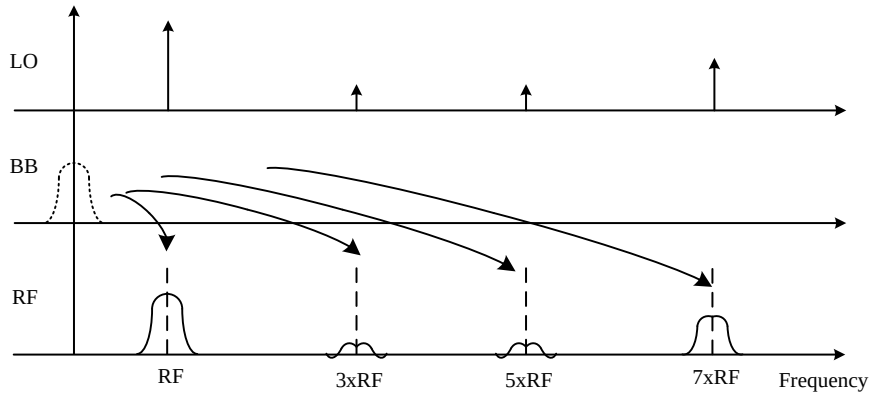
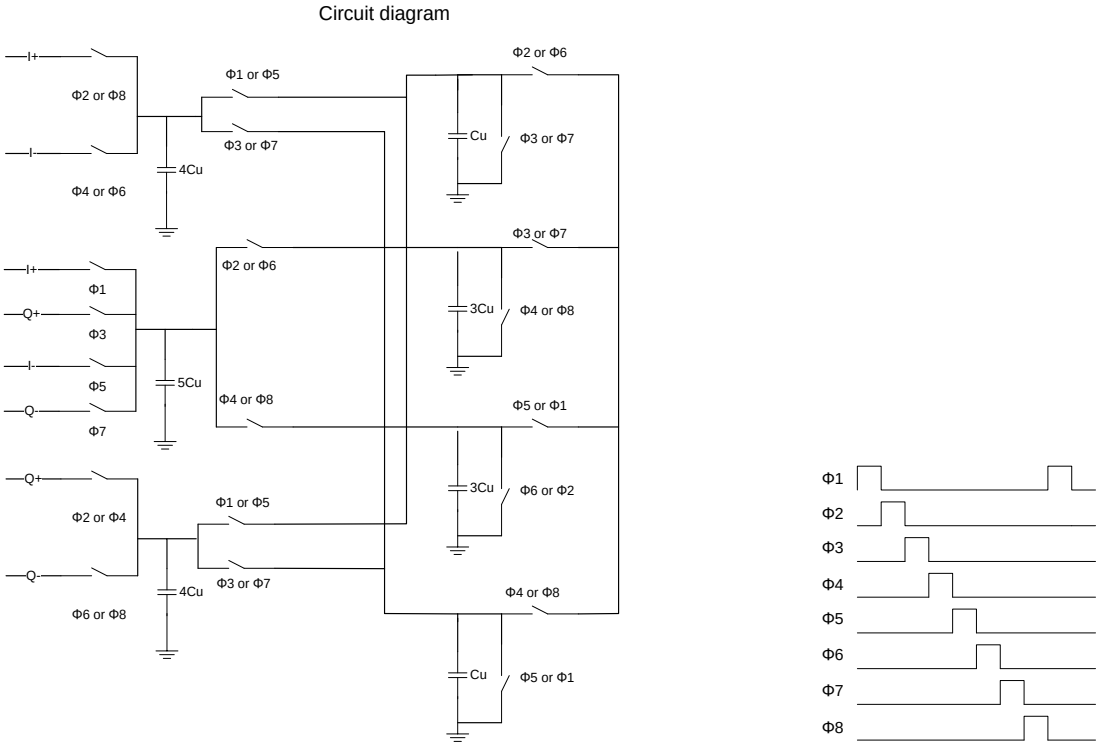


Fig. 5.11 Frequency up-conversion of HRM.

The 3rd and 5th order harmonics are attenuated and only 7th order harmonic remains. The filter requirement can be greatly relieved.

While in continuous time domain HRM can be implemented by active Gilbert switch mixers, in discrete time domain HRM can utilize the sample and hold circuit. The different LO amplitude multiplied with sampled signal is implemented by different capacitor value weighting. The capacitors have better match performance than current and transconductance used in active mixers. The circuit diagram of discrete time HRM is shown in the following,



(a) (b)

Fig. 5.12 (a) Schematic diagram of HRM, (b) Eight phase LO clocks.

The HRM has the differential outputs. For the sake of simplicity, only the positive output is plotted in the diagram. Every switch is turned on or off by the clock labeled next to the switch. Fig. 5.11(b) shows the eight LO clocks with one eighth duty cycle and different phases. They are generated from a master clock with frequency $4f_c$, where f_c is the carrier frequency. At clock phases $\left[0, \frac{\pi}{2}, \pi, \frac{3\pi}{2}\right]$ center branch charges the in-phase or quadrature signals alternatively onto

$5C_u$ (C_u is unity capacitor), then share the charge with second stage capacitor $3C_u$. The input voltage is multiplied by 5/8 weighting factor at output. At clock phases $\left[\frac{\pi}{4}, \frac{3\pi}{4}, \frac{5\pi}{4}, \frac{7\pi}{4}\right]$, top branch and bottom branch charge the inputs simultaneously onto $4C_u$ and then share them with each other plus a C_u capacitor. That makes the weighting factor 4/9. Hence the ratio of two factors is 1.4, an approximate value to $\sqrt{2}$.

The switches are implemented by double transmission gate with the circuit shown in the following diagram.

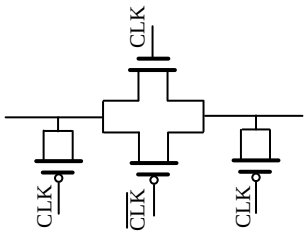


Fig. 5.13 Double transmission gate.

The NMOS/PMOS pair is adopted to reduce the on resistance dependence on input level, and to cancel the injected charge with each other. Two PMOS dummy cells are inserted before and after the gate to cancel the additional charge injection and clock feedthrough by PMOS transistor because PMOS usually is much larger than NMOS.

LO signal fully swings from 0V to 1.5V. The common mode voltage is biased at 0.75V. The simulated on resistance at 0.75V input is approximate 14Ω. It is postulated that source impedance is 50Ω for a standard RF interface. Therefore there is total 64Ω resistance and 460fF ($5C_u$) capacitance. The related time constant is calculated as 30pS. That means the step response will take 4.6x30=138pS to reach 99% of final steady value. Because the sampling frequency is eight times of RF frequency as shown in Fig. 5.12(b), the maximum operation frequency of this mixer is no more than 1GHz. This is the design target for this 0.13um CMOS technology. There

is always a tradeoff between speed, noise and charge injection. Reducing the capacitance further will increase the speed at the cost of bigger noise. Increasing the transmission gate also incurs the large charge injection.

The HRM is basically a passive mixer. Hence it shares the same properties of low power dissipation, high linearity and low flicker noise.

5.5 Simulation results

The HRM was implemented in 0.13um CMOS technology. Although the technology has the RF property, the HRM only used standard MOS transistors and capacitors, which makes it practical in digital CMOS process. The HRM core operates with a supply voltage of 1.5V and consumes no quiescent current. A clock circuit is designed to generate eight phase clocks.

Fig. 5.14 shows the simulated HRM output with 20MHz low IF input and 1GHz carrier frequency.

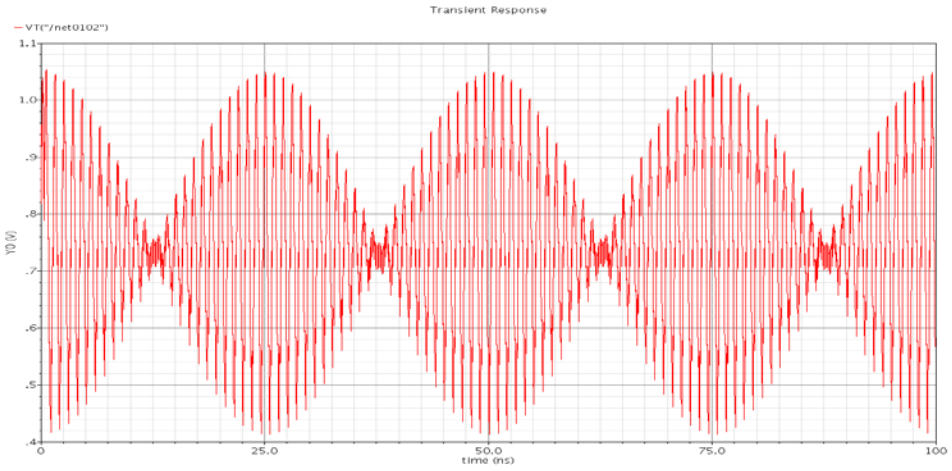


Fig. 5.14 HRM output with 20MHz input and 1GHz LO.

The simulated conversion gain relative to LO frequency is shown in the following diagram

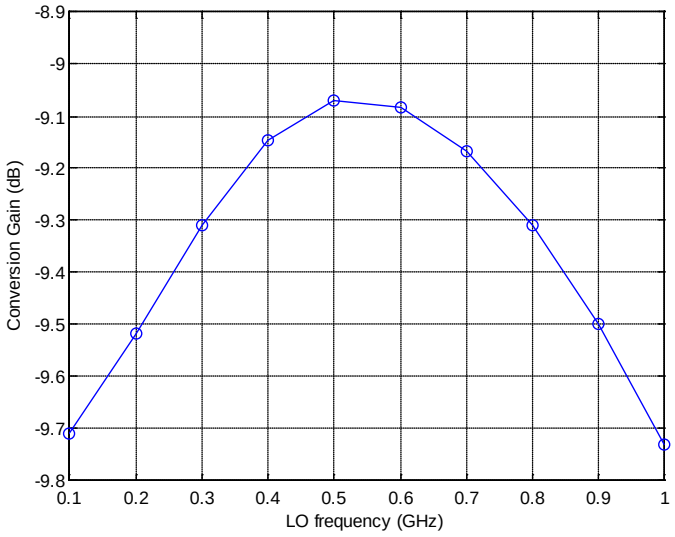


Fig. 5.15 Conversion gain with LO frequency.

From the diagram, it is observed that the conversion gain remains under -9dB regardless of frequency. Fig. 5.12(a) shows that the maximum weighting factor is 5/8. Therefore the frequency conversion can be expressed as

$$\mathbf{RF} = \frac{\mathbf{5}}{\mathbf{8}}\mathbf{cos}(\boldsymbol{\omega_c t}) \times \mathbf{cos}(\boldsymbol{\omega_L t})$$

$$= \frac{5}{16}\{\cos[(\omega_c - \omega_L)t] + \cos[(\omega_c + \omega_L)t]\} \quad (5\text{-}7)$$

,where $\boldsymbol{\omega_c}$ is LO angular frequency, $\boldsymbol{\omega_L}$ is angular frequency of baseband signal. The amplitude of modulated signal is 5/16, which approximates -10dB. The simulation result justifies the theoretical calculation. Because there is no active amplifying stage in this HRM, the conversion gain is low and might degrade the noise performance at following stages. This can be compensated by inserting an amplifying buffer behind or before the HRM.

The SSB NF of HRM with different LO frequency is simulated and results are shown in the following diagram:

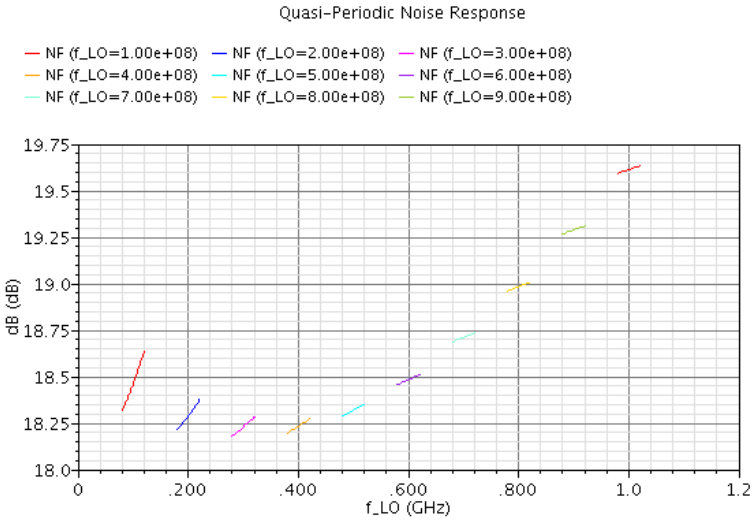


Fig. 5.16 SSB NF of HRM with frequency.

The noise figure varies from 18.25dB to maximum 19.7dB with LO frequencies ranging from 100MHz to 1GHz. This result is comparable with [51] which used 65nm CMOS. Furthermore the NF remains relatively stable over frequency unlike [51]. The NF rises at high frequency end which is a reasonable observation. This NF performance beats that of sub-sampling mixer of [48] and most of other passive mixers listed in [48].

The following figure shows the simulated 3rd order harmonic rejection ratio with LO frequency.

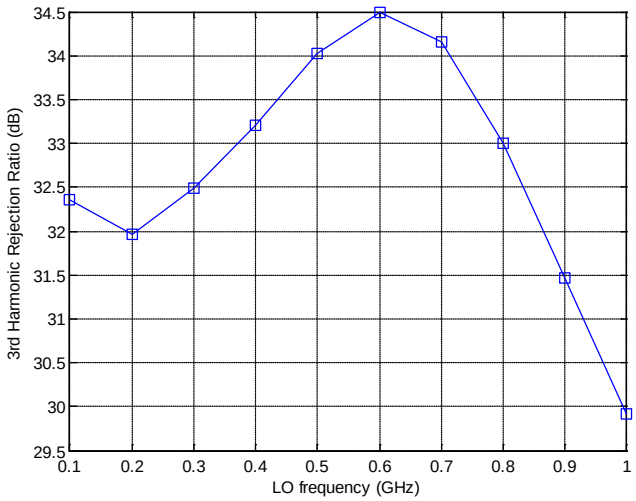


Fig. 5.17 3rd harmonic rejection ratio with LO.

The rejection ratio is more than 30dB, the maximum value reaches 35dB while the HR ration is 9dB in typical Gilbert switch mixers. The HR ratio will drop when frequency approaches 1GHz because the higher frequency makes the sampling circuit hard to complete sampling procedure. Therefore the weighting factors will deviate from their ideal values. Fig. 5.18 shows the 5th order harmonic rejection. 5th order HR ratio is higher than 3rd order.

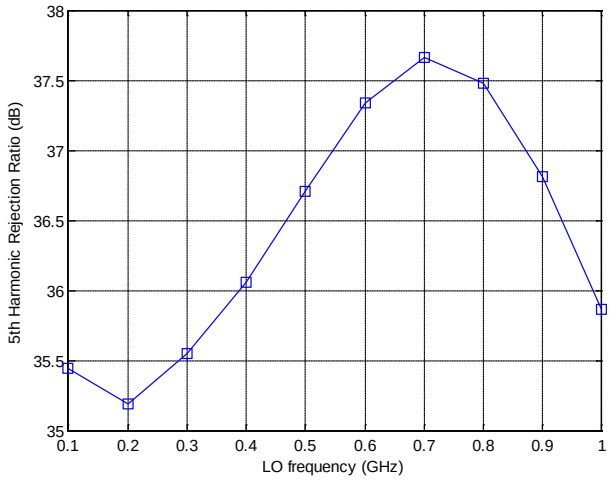


Fig. 5.18 5th harmonic rejection ratio with LO.

The above results in Fig. 5.17 and Fig. 5.18 demonstrate the validity and feasibility of HRM.

The HRM also possess the property of LO isolation. The HRM is different from the traditional mixer since it has more than one LO ports and LO clocks (eight in this design). Therefore it is hard to define the LO isolation. In this chapter, the LO attenuation is defined as LO signal amplitude relative to modulated signal amplitude in unit of dB at output port. The corresponding simulation is shown in the following figure.

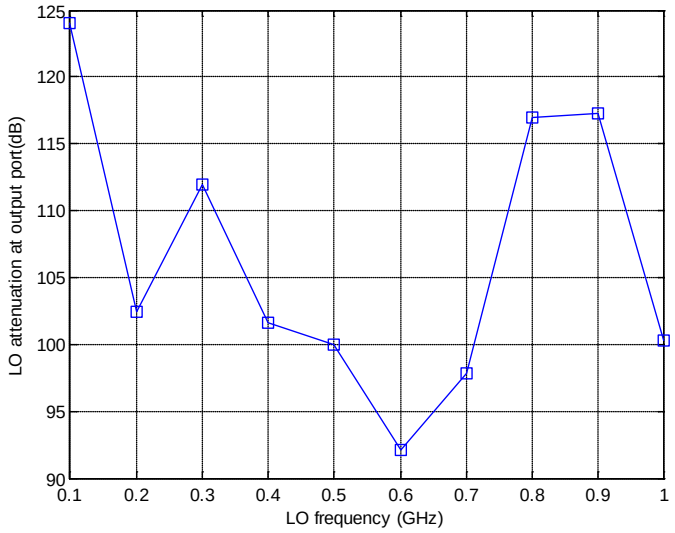


Fig. 5.19 LO attenuation at output port.

The LO attenuation is more than 100dB lower relative to the modulated signal, thus it will not influence the signal even if the signal has a bandwidth covering carrier frequency.

Due to the passive property of HRM, it possesses the characteristic of high linearity. The 1dB compression point is simulated and shown in Fig. 5.20.

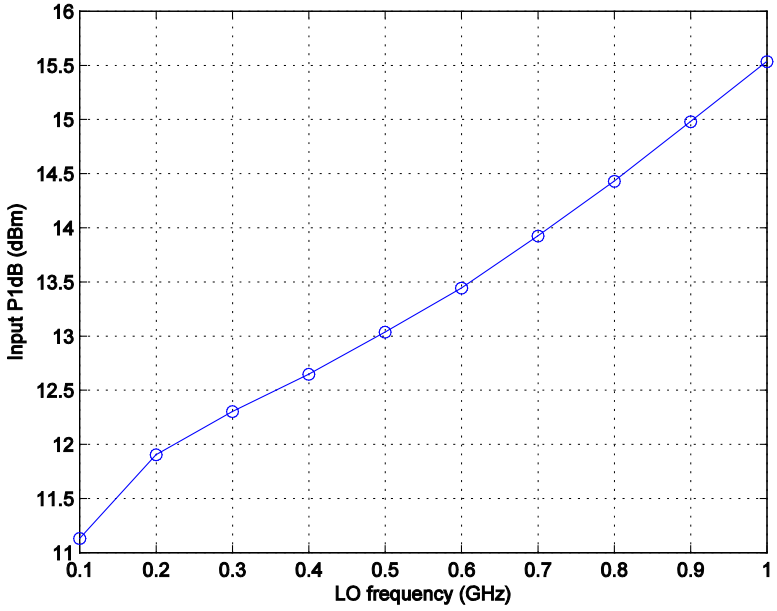


Fig. 5.20 IP1dB with LO frequency.

The input P1dB ranges from 11dBm to 15.5dBm over frequency of 100MHz to 1GHz. The linearity rises with frequency because gain falls at high frequency.

5.6 Conclusion

In this chapter, a novel HRM is presented and demonstrated. With the eight-phase LO clocks, the 3rd and 5th order harmonics are attenuated more than 30dB, which reduces the inter-modulation products and relieves the filter requirement. Good LO isolation and nonlinearity performance are achieved due to HRM passive property. Noise figure is comparable with other mixer designs. The HRM core circuit consumes negligible power which makes it a good candidate in low power application and digital CMOS technology.

Chapter 6 A 75% Tuning Range Digitally Controlled Oscillator

6.1 Introduction

A wideband digitally controlled oscillator (DCO) for all digital phase-locked loop (ADPLL) application is presented in this chapter. The DCO has an 8th order resonator composed of coupled inductors and MOS varactors. Layout of coupled inductors is in a concentric pattern that greatly saves die area while achieving wide tuning range and eliminating the use of MOS switches. The tuning range contains four bands and covers from 1.4GHz to 3.86GHz. The DCO radio frequency integrated circuit (RFIC) was implemented in 0.13μm CMOS technology and occupies an area of 0.75x0.75 mm^2 including output buffer and bias circuitry. The power consumption for the DCO core is 6.5mW with a 1.5V power supply. The measured phase noise at 1MHz frequency offset from 3GHz output is around −110dBc/Hz.

With the emergence of new wireless standards such as Bluetooth, Wireless LAN and Ultra Wideband (UWB), there has been an increasing demand for integrating multiple standards into one system for the purpose of saving power and cost. One of the main challenges to meet multiple standards in a single chip is the design of a wideband oscillator. Realization of wideband LC oscillators has been addressed in the literature for several years. LC DCO based on switched varactor bank is the most common choice [52][53].

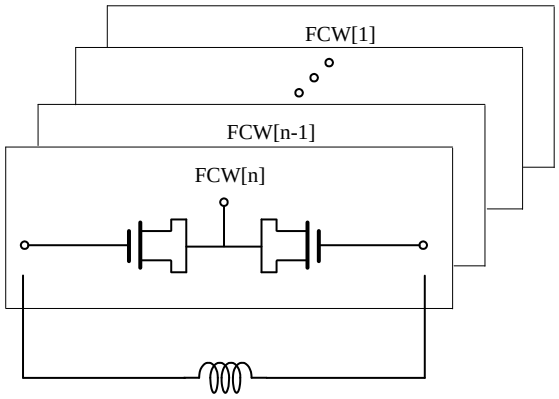


Fig. 6.1 Switched Varactor based LC tank.

The above diagram shows the basic LC tank applied in digitally controlled oscillator (DCO). The frequency control word (FCW) is used to tune the corresponding varactor tank. Different control bits have different weights of capacitance value. Inductor is usually parallel with the varactor banks. In switch capacitor topology, the varactor is replaced with capacitors and switches. Capacitors can be metal-insulator-metal capacitors in typical IC technology, which has higher Q factor than varactors. On the other hand, resistive loss associated with switches will limit the overall Q factor. Switched varactor oscillator has limited frequency tuning range due to the ratio of maximum to minimum capacitance obtained from the varactor. Using multiple LC tanks is the natural solution. A switched inductor resonator was reported in [54]. Up to four inductors are used in the design. Additional inductors can be selected by switches. But multiple separate inductors occupy large chip area, and the switches used can contribute noise and parasitic capacitance. In order to save area, a coupled inductor CMOS oscillator with switches was proposed in [55]. Three different inductors are placed together in an inter-wound manner, but switches are still used to select different frequency bands, therefore Q factor of the resonator is still degraded by switches. To eliminate the use of switches in resonators, various approaches have been proposed. In [56], a dual mode VCO built around two coupled inductors was reported.

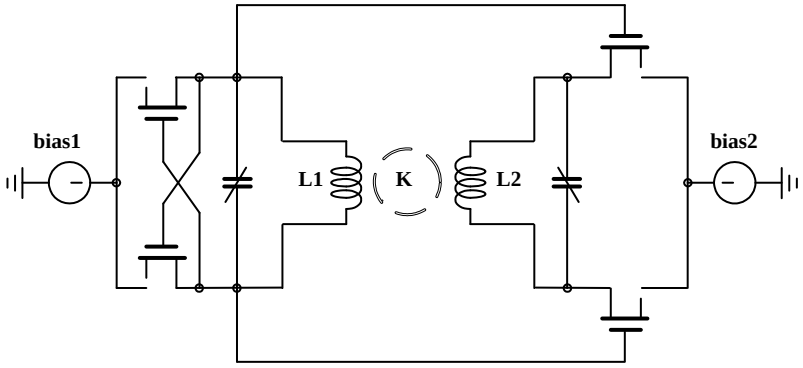


Fig. 6.2 Schematic of dual mode wideband VCO.

The VCO is built around a transformer based on two coupled inductors. Switching between two frequency bands is implemented by turning on or off corresponding tail currents. When bias2 is turned off, the wideband VCO degenerates to a traditional VCO with one LC tank. When bias2 is turned on, a pair of differential NMOS transistors acts as transconductance in a feedback loop. The feedback signal is magnetically coupled back to the L1 tank. Therefore the equivalent LC tank is the parallel of two tanks. The fine frequency tuning is obtained by varactor banks tuning. A wide tuning range is achieved while maintaining good phase noise. The feedback differential pair provides the transconductance instead of resistive loss as in switched VCO. In [57] and [58], a magnetically tuned oscillator based on transformers was proposed. The frequency tuning ability depends on current tuning which results in equivalent self-inductance variation. This type of resonator comprises only one LC tank and covers one frequency band (excluding the effect of varactor tuning). Since the inductance tuning range is limited, the frequency tuning range is limited as well. In [59] a VCO was designed based on concentric layout of the three inductors. These inductors work independently with small coupling. Every inductor is associated with a varactor and an active core, covers an independent frequency band respectively. When one of the three VCOs is turned on, the other two at the same time sense the oscillation signal through weak coupling. Totally three VCOs will cover a wide frequency band. In [60] the oscillator design

employed active inductors to achieve very wide tuning range in small area, but active inductors cannot provide low enough phase noise.

Most effort has been spent on wideband VCOs. In this chapter, a DCO built on an 8th order resonator is described and designed for use in an ADPLL. The inductor tanks are placed in a concentric layout and coupled to each other. Lossy switches are saved due to the coupling between inductors. The wideband VCO usually has the coarse tuning and fine tuning stages. In order to interface with the ADPLL smoothly, this DCO has only one group of digital controlled bits and one tuning stage. The organization of this chapter is as follows: In Section 6.2, the DCO architecture and circuit design will be discussed. In Section 6.3, the measurement results of the DCO chip will be given. Conclusions will be drawn in Section 6.4.

6.2 DCO Architecture and Circuit Design

The proposed DCO is built around coupled inductors as shown in Fig. 6.3. There are four inductors laid in the same area forming an 8th order resonator with capacitors. Because a single LC tank will generate a two order system, four LC tanks can only be represented by 8th order system. Each of the LC tanks is companied by an active circuit, corresponds to an operation mode and covers a separate frequency band. Four LC tanks are combined together by the magnetic coupling. The active circuit used to provide negative Gm has the complementary MOS topology for the purpose of saving power. The PMOS cross coupled pair shares the same current with NMOS cross coupled pair. To achieve the same transconductance, each pair needs to provide half of it. Because gm is square-root proportional to current,

$$\boldsymbol{gm = \sqrt{2\mu C_{ox}\frac{W}{L}I}} \tag{6-1}$$

the current is reduced to one fourth of the original value, where μ is electron mobility, C_{ox} is unity gate capacitance. Even though complementary topology requires higher voltage headroom,

the power consumption is still saved. There is no switch embedded in the circuit to turn on or off different modes. The switching is implemented by powering on the respective tail current. Due to the inductor coupling, any of the oscillation signals will be sensed by the other three tanks. Therefore any one of the four tanks could generate the output signal for the whole DCO. In this design, the tank of inductor L2 is chosen to generate the output signal and drive the output buffer because it has relatively stable coupling coefficients to other inductors. Thus it will not significantly degrade signal strength from any of the other three tanks.

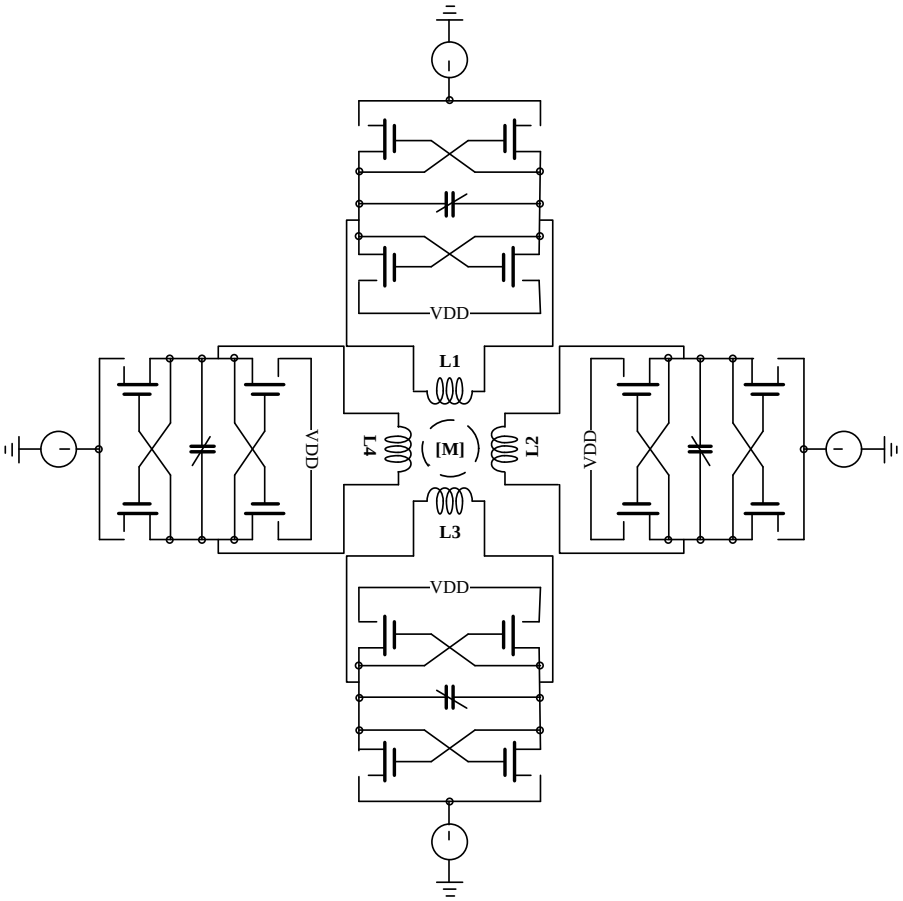


Fig. 6.3 Schematic of DCO based on 8th order resonator.

Four LC tanks will contribute to an 8th order transfer function and generate four second order stable solutions. It means four possible oscillation frequencies will exist at any port of the four-port resonator. When any one of the four active circuits is turned on, there is possible four

different frequency signals generated at most. But we only need one frequency to be sustained. Intuitively speaking, the impedance looking into any resonator port needs to be much bigger at the expected frequency than at other three frequencies. For port 1 (inductor L1) of the resonator, it is required that

$$\frac{\boldsymbol{Re\{Z(\omega_1)\}}}{\boldsymbol{Re\{Z(\omega_2)\}}} \gg \mathbf{1}, \frac{\boldsymbol{Re\{Z(\omega_1)\}}}{\boldsymbol{Re\{Z(\omega_3)\}}} \gg \mathbf{1}, \frac{\boldsymbol{Re\{Z(\omega_1)\}}}{\boldsymbol{Re\{Z(\omega_4)\}}} \gg \mathbf{1} \tag{6-2}$$

, where $Z(\cdot)$ is the impedance of port 1 and ω_1, ω_2, ω_3 and ω_4 are four resonate frequencies. At the same time, it is also required that the imaginary part of impedance is zero at resonation frequency,

$$\boldsymbol{Im\{Z(\omega_1)\} = 0} \tag{6-3}$$

which means the inductive part and capacitive part cancel each other at ω_1. For a fourth-order resonator composed of two LC tanks, the port impedance depends on both coupling coefficient *k* and the ratio of self-resonate frequencies $\gamma = (\omega_H/\omega_L)^2$ [56], where ω_H is the self-resonate frequency of one LC tank without mutual inductance, and ω_L is the frequency of another tank, $\omega_H > \omega_L$. To meet the requirement of large impedance ratio of (1), γ needs to be large while *k* needs to remain small [56]. If coupling factor is small, then one LC tank will exhibit its self resonation frequency impedance. If γ is large, the characteristic of two tanks differs with each other to a great extent, thus making the non-self-resonation frequency hard to survive at the other tank. But in order to achieve continuous frequency tuning range, γ cannot be large. Therefore one safe choice is $k \approx 0.2$ and inductance ratio is approximately 1.7 as in this design. Higher order resonators complicate the design choice, but since a low *k.* value is picked, the additional LC tanks do not influence the impedance too much.

Fig. 6.4 Stacked inductors layout

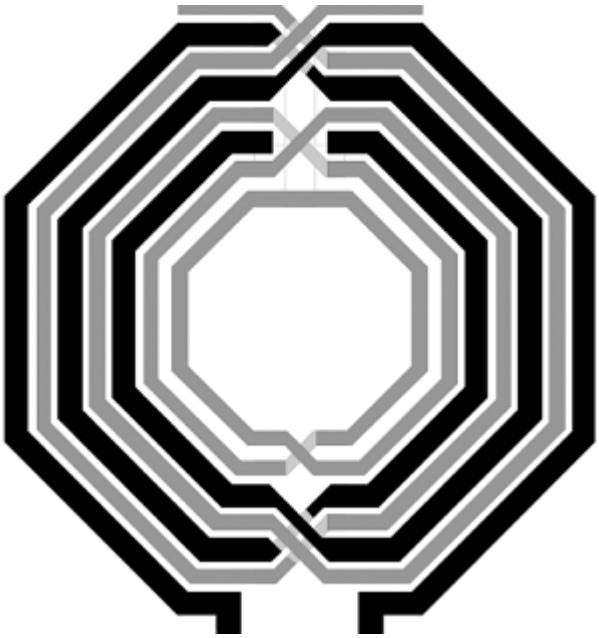
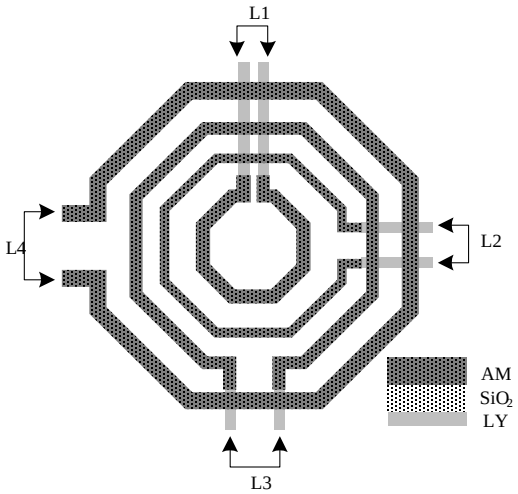
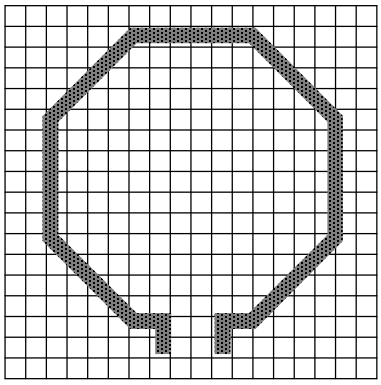


Fig. 6.5 Inter-wound inductors layout



(a)



(b)

Fig. 6.6 Diagram of (a) two-dimensional coupled inductors layout, and (b) two-dimensional inductor layout with deep trench lattice.

Usually there are three types of coupled inductor layouts: (1) stacked layout, (2) inter-wound layout and (3) concentric layout. The stacked inductors use top level analog metal and the second level metal. The top level analog metal owns low resistivity and thus low loss. The two inductors use different metal but share same area as shown in Fig. 6.4. As shown in Fig. 6.5., inter-wound layout uses one level metal (usually top level), the lower level metal is used for routing purpose (underpass path). Therefore the resistive loss is lower. But inter-wound layout occupies more area, thus it is hard to achieve large inductance value. The stacked inductor layout and inter-wound layout can both provide high coupling coefficient, which is not desired in this design. Furthermore these two structures have higher parasitic capacitance due to the close proximity of metals. Hence the operation frequency is limited by their low self-resonation frequency.

The concentric layout has low coupling and only uses a single layer of metal (excluding the underpass path). Therefore it can be built solely on the top level analog metal (AM) that provides low ohmic loss. Fig. 6.6(a) shows the inductors layout of the 8^{th} order resonator. The inductors use top level metal and underpass paths use next level metal. All inductors are placed on a layer of deep trench lattice embedded in silicon substrate in order to reduce parasitic capacitance from

inductor to substrate and reduce eddy current loss, as shown in Fig. 6.6(b). There are mainly three kinds of loss associated with on chip inductors, (1) ohmic loss, (2) displacement current loss, and (3) eddy current loss. The eddy current loss is shown in the following diagram.

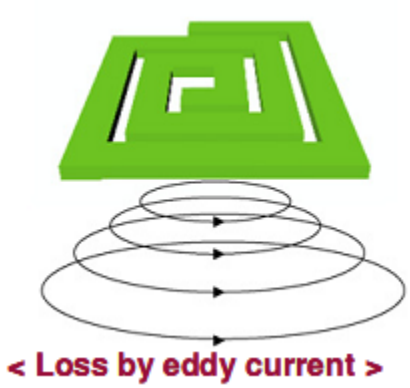


Fig. 6.7 Eddy current loss

It is induced by alternative magnetic field through resistive substrate. The substrate resistivity is 11-16 Ω·cm in this design. If a lattice of high resistance dielectric is embedded into substrate, the current loop will be broken resulting in low power loss and high Q factor. EM simulation has been carried out on coupled inductors using ADS Momentum. The inductor layout shown in Fig. 6.6(a) can either be drawn in ADS directly or drawn in Cadence VIRTUOSO layout and then streamed out to GDSII format. ADS layout can import the GDSII format. The import option can be accessed from ADS layout File menu.

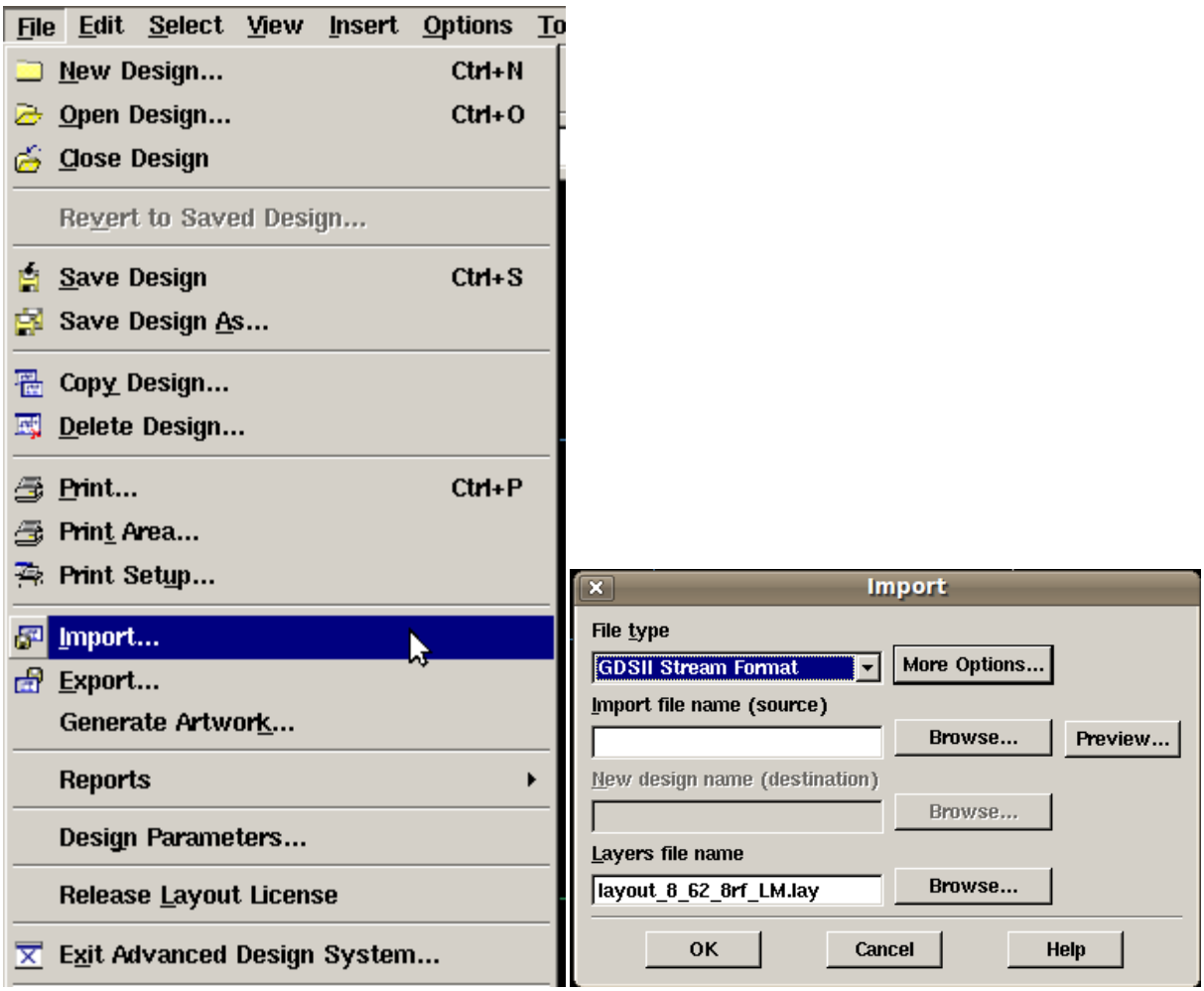


Fig. 6.8 ADS layout import menu

In next step it is necessary to define the substrate property, e.g., thickness and permittivity of dielectric, thickness and conductivity of metal layer, as shown in Fig. 6.9. The technology used in this design provides pre-defined substrate for ADS application. After loading the substrate, one should pre-compute the substrate and save the result for future application. The frequency range in substrate computation should cover the highest interested frequency band. Actually it is better to use four times highest frequency in order to interpolate the desired frequency response precisely.

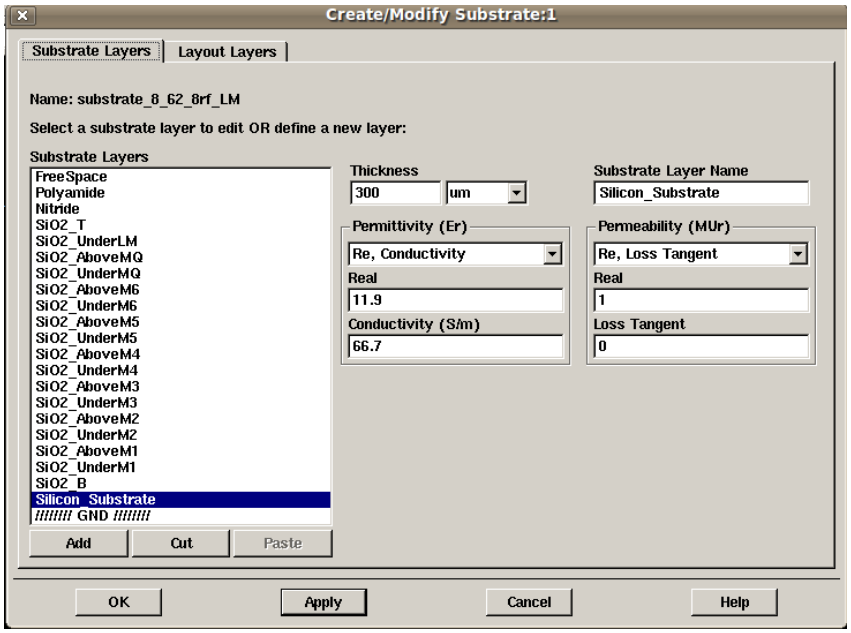


Fig. 6.9 ADS substrate creation

After setup of substrate, one needs to insert port and specify port property for every terminal. For example, one could use two ports for the positive terminal and negative terminal of an inductor. Totally eight ports were used in this 8th order resonator design. Therefore the simulated S parameters can only be represented by an eight port ‘nport’ cell. The fourth step is to mesh the object under simulation. Same principle is that mesh frequency needs to be much larger than desired operation frequency.

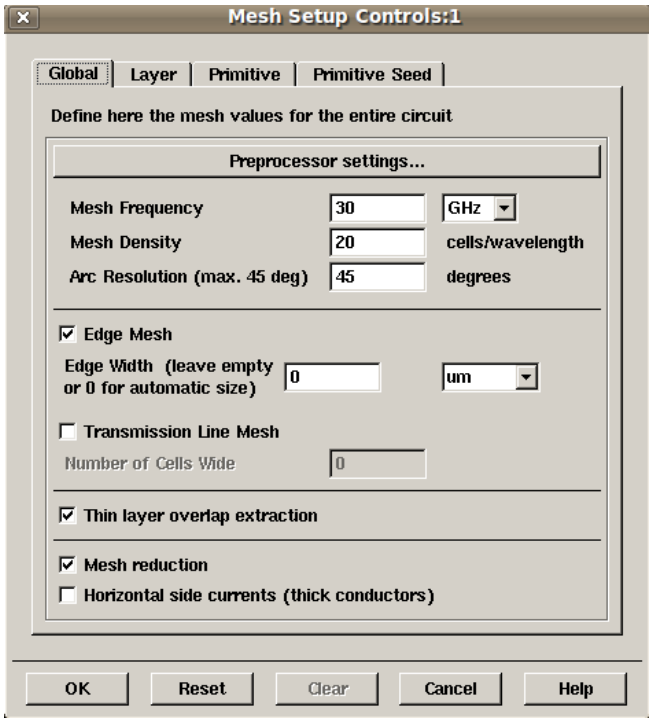


Fig. 6.10 ADS Momentum mesh option

The final step is to simulate the S parameter. All above actions can be accessed from ADS layout Momentum menu. The simulated S parameter can be exported into touchstone format which can be utilized by Cadence nport cell for circuit simulation. The lumped elements are extracted from S parameter file by MATLAB program as following equations:

$$\boldsymbol{L_n = \frac{imag(Z_{nn})}{2\pi f}} \tag{6-4}$$

$$\boldsymbol{Q_n = \frac{imag(Z_{nn})}{real(Z_{nn})}} \tag{6-5}$$

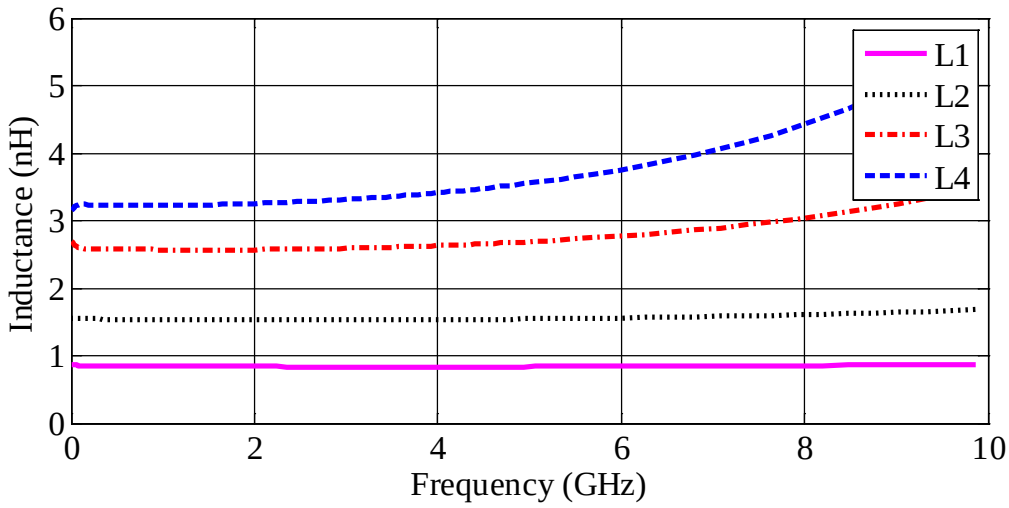
$$\boldsymbol{k_{mn} = \frac{imag(Z_{mn})}{2\pi f\sqrt{L_m L_n}}} \tag{6-6}$$

where Z stands for Z parameters, L is self inductance, Q is quality factor, k is the coupling factor. Z parameters can be converted from S parameters as:

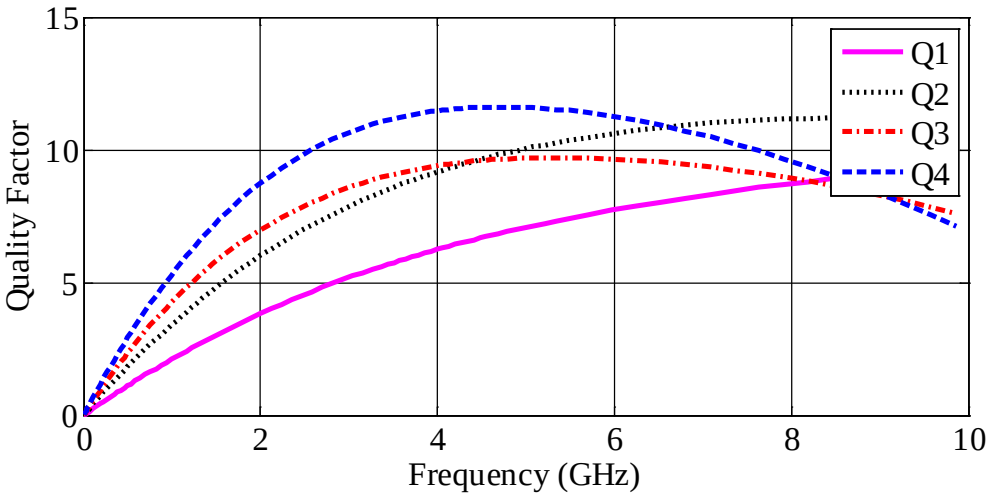
$$\boldsymbol{Z = Z0\frac{U+S}{U-S}} \tag{6-7}$$

where S stands for S parameter matrix, U represents identity matrix, Z0 is the characteristic impedance as reference.

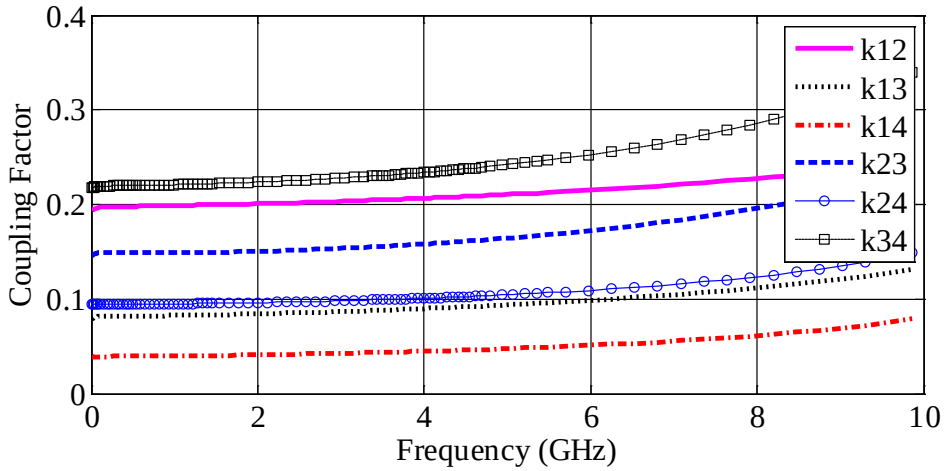
The extracted results of eight port transformer are shown in Fig. 6.11. Fig. 6.11(a) demonstrates the equivalent self-inductance of each port when other ports are left open. The inductance value is close to the original value without coupling and the ratio between adjacent inductance values is close to 1.7. Simulated Q factors in Fig. 6.11(b) are between 5 and 10 within the operational frequency band, which could be improved by increasing metal width or inserting parallel spiral beneath the top level. The peak Q frequencies are well above the operation band. The largest inductor (L4) reaches the maximum Q factor value first with frequency increases. Six coupling coefficients are shown in Fig. 6.11(c). They range from 0.05 to 0.22 and are close to the design choice. Coefficients *k*12, *k*23, *k*24 have the similar values, which means the signals from other three LC tanks couple to No.2 LC tank with approximately same amplitude. This observation justifies the design choice of port two as output port.



(a)



(b)



(c)

Fig. 6.11 Diagram of simulated (a) self inductance, and (b) Q factors, and (c) coupling coefficients of inductor bank.

The four varactor banks associated with inductors share the same nine control bits for frequency tuning. The accumulation type nMOS varactor used can provide maximum capacitance ratio of 2.6 (minimum channel length is selected for the tank Q factor). It indicates that the available frequency tuning range is no more than 48% for each operation band.

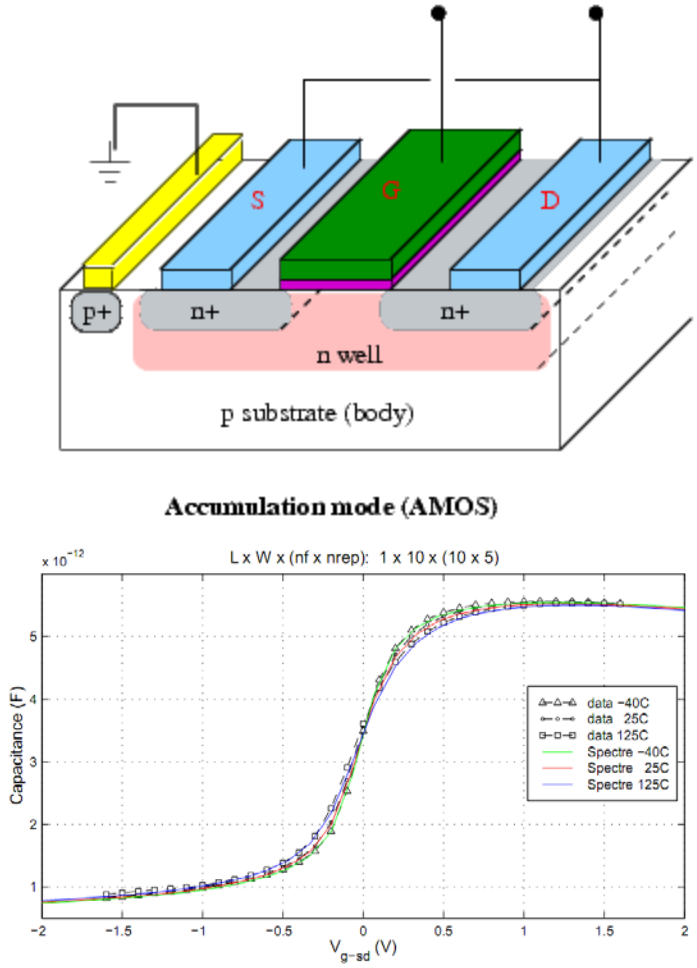


Fig. 6.12 Accumulation type MOS varactor

Fig 6.12 shows the capacitance value variation v.s. gate to source/drain voltage. In order to be applied in digitally controlled oscillator, the varactor C-V curve needs to provide stable tuning points to minimize the control line induced noise. From the above diagram, it is clearly shown that -0.5V and 1V gate voltage can be used. This choice makes the implementation of digital controlling feasible in 1.5V power supply.

6.3 Measurement Results

The DCO was fabricated in 0.13um CMOS technology. The DCO core circuit occupies 0.75x0.75 mm^2 and total area including pads is 1x1 mm^2 as shown in Fig. 6.13. The inductors are

placed in the center of layout while four varactor tanks are placed at the side of corresponding inductor. The DCO uses a supply voltage of 1.5V and consumes 4.3mA current for each independent active branch.

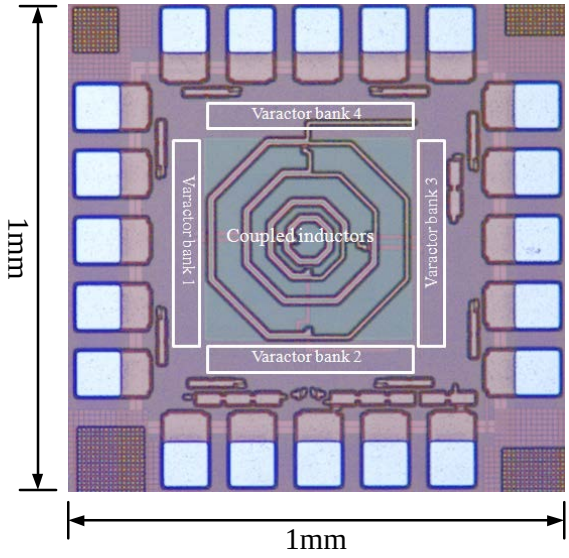


Fig. 6.13 Micrograph of DCO RFIC based on 8th order resonator.

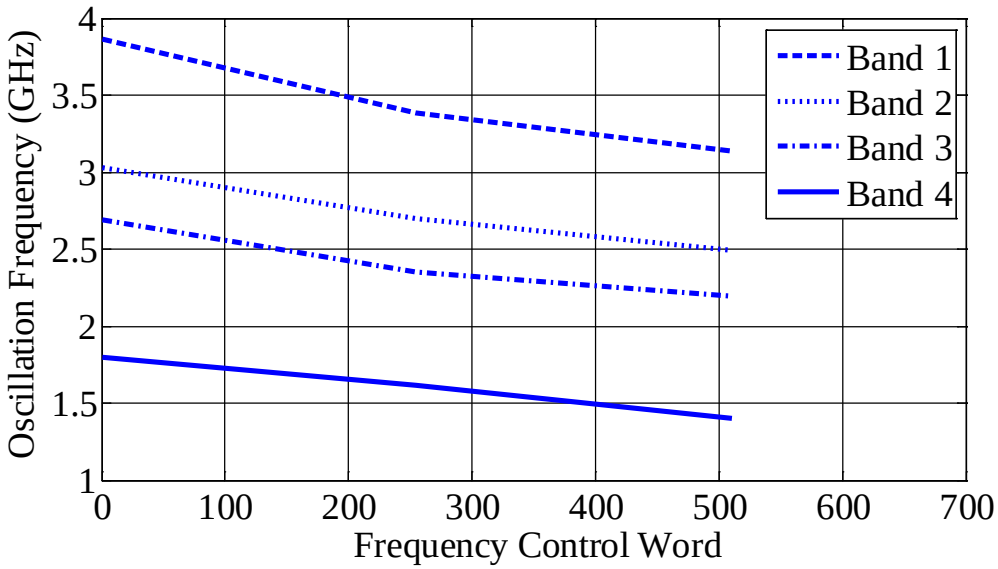
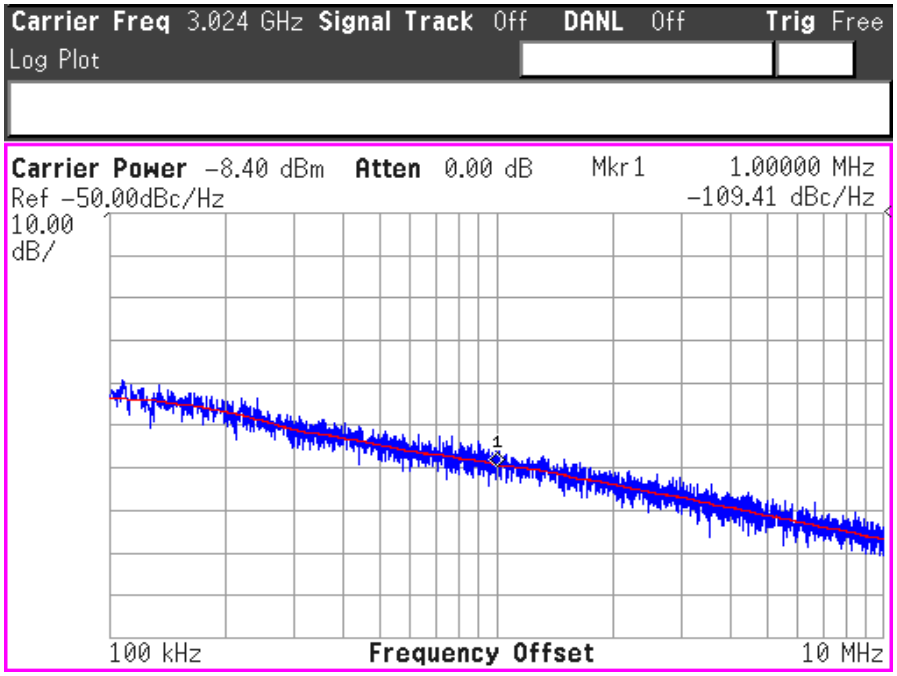


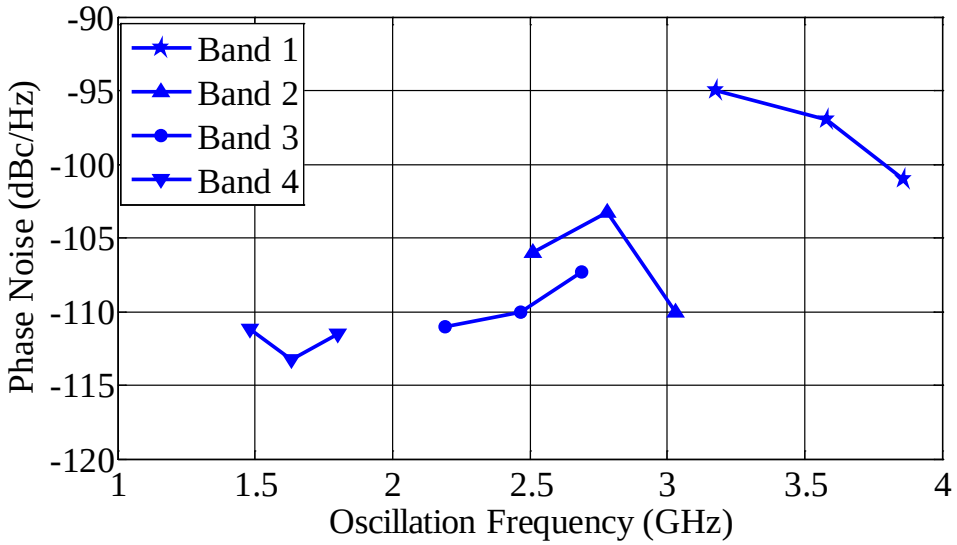
Fig. 6.14 Measured frequency tuning curves of DCO.

The measured frequency tuning range with respect to frequency control word is shown in Fig. 6.14. LC tank 1 covers the frequency band 3.14GHz-3.86GHz; tank 2 covers the 2.49GHz-

3.04GHz band; tank 3 covers 2.19GHz-2.69GHz, and tank 4 covers 1.4GHz-1.8GHz. There is a 390MHz frequency gap between band 3 and band 4 and a 100MHz gap between 1 and 2. This problem is due to the parasitic capacitance shifting the frequency band. It can be fixed by reducing CMOS transistor size or adding more varactors to shift frequency band 3 toward band 4. The frequency tuning range of each LC tank varies from 20% to 25%, reduced from 48% due to the parasitic capacitance. Although there is the frequency gap, the DCO covers a 75% tuning range (gap bandwidth subtracted) with the combination of four LC tanks according to Eq. (6-11). The frequency tuning step is approximately 1.1MHz/LSB.



(a)



(b)

Fig. 6.15 (a) Sample phase noise measurement at 3.024GHz, and (b) typical phase noise at 1MHz offset through the frequency bands.

A sample phase noise measurement is shown in Fig. 6.15(a) when the active circuit with port 2 is turned on. The oscillation frequency is 3.024GHz. Phase noise at 1MHz offset from carrier is approximately −109.4dBc/Hz. The phase noise curve follows a −20dB/decade slope predicted by Leeson's model. Since the output signal is picked up at port 2 of the 8th order resonator, the signal strength is measured as high as −8dBm. When the active circuits associated with other ports are turned on, the signal arrives at port 2 through weak coupling. The measured signal power falls between −20dBm and −30dBm. A group of sample phase noise has been measured across the whole frequency band and is shown in Fig. 6.15(b). In general, the average value of the phase noise increases with frequency, but the individual phase noise will vary in the opposite direction in frequency band 1 and 2. The phase noise is not only proportional to the square of the oscillation frequency but also inversely proportional to the square of the Q factor.

$$\boldsymbol{L(\Delta\omega)\sim\frac{k_BT}{P_{DC}}\left(\frac{\omega_0}{Q\Delta\omega}\right)^2} \tag{6-8}$$

k_B is the Boltzmann constant, T is the temperature in unit of Kelvins, P_{DC} is the DC power dissipated in the oscillator, and $\Delta\omega$ is the offset frequency from carrier ω_0. In the low frequency band, the tank Q is determined by the inductor, therefore changing the varactor has little effect. But in the high frequency band, turning the varactor on or off could affect resonator Q factor. Reducing varactor capacitance can tune the frequency higher and improve the tank Q factor simultaneously.

Table 6-1 Summary and Comparison of DCO Performance

	[52]	[53]	This Work
Technology	65nm CMOS	0.18μm CMOS	0.13μm CMOS
RF frequency[GHz]	10	5.8	1.4~3.86
Phase noise[dBc/Hz]	−102@1MHz	−118@1MHz	−95 ~ −114@1MHz
Die size(wo/pads)[mm^2]	0.025	0.48	0.56
Tuning range	10%	5%	75%
Power [mW]	10	9.2	6.5
Typical FOM[dBc/Hz]	−21	−16	−10, −4

The measured performance is summarized in Table 6-1. Comparison with other recent published DCOs is included as well. In order to evaluate the overall performance of the oscillator, power-frequency-tuning-normalized (PFTN) figure of merit (FOM) is widely used as comparison benchmark considering frequency tuning range, [10]

$$\boldsymbol{FOM = 10\log\left[\frac{k_B T}{P_{DC}}\left(\frac{\omega_{\max}-\omega_{\min}}{\Delta\omega}\right)^2\right] - L(\Delta\omega)} \tag{6-9}$$

$\omega_{\max}$ and $\omega_{\min}$ are the maximum and minimum oscillation frequency. Eq. (6-9) comes from

$$\boldsymbol{FOM = 10\log\left[\frac{k_B T}{P_{DC}}\left(\frac{\omega_0}{\Delta\omega}\right)^2\left(\frac{\omega_{max}-\omega_{min}}{\omega_0}\right)^2\right] - L(\Delta\omega)} \quad (6\text{-}10)$$

where ω_0 is the oscillation angular frequency. The frequency tuning range is defined as

$$\boldsymbol{R_{tune} = 2 \times \frac{\omega_{max}-\omega_{min}}{\omega_{max}+\omega_{min}} = \frac{\omega_{max}-\omega_{min}}{\omega_c}} \quad (6\text{-}11)$$

In which ω_c is the center frequency of the band. Substituting Eq. (6-11) into Eq. (6-10), the FOM can be expressed in terms of R_{tune}.

$$\boldsymbol{FOM = 10\log\left[\frac{k_B T}{P_{DC}}\left(\frac{\omega_0}{\Delta\omega}\right)^2 R_{tune}^2\right] - L(\Delta\omega)} \quad (6\text{-}12)$$

Eq. (6-12) is used to calculate the FOM in this chapter.

6.4 Conclusion

This chapter reports a wideband DCO applicable in all digital PLLs. The DCO is formed by an 8th order resonator composed of four coupled inductors and respective varactors. The operation band is selected by powering on or off the corresponding active circuits instead of switches. MOS switch loss and the parasitic capacitance is avoided. The output signal is sensed through mutual inductance coupling. The chip was fabricated in 0.13um CMOS. The DCO core occupies 0.56 mm^2 die size and draws 4.3mA current from a 1.5V power supply. Measured frequency band ranges from 1.4GHz to 3.86GHz. A 75% tuning range is covered, which is the largest result ever reported in DCO design to the best knowledge of authors.

Chapter 7 Conclusion

7.1 Summary of original work

This dissertation covers not only the theoretical analysis from modern communication system to X band radar system, but also the design details from PA driver to DCO and mixer. Analytical expression of system performance was derived to serve as design reference or specifications. At the same time, a wide range of simulations and experiments have been done to verify the implementation possibility.

Chapter 2 analyzes the RF transceiver impairments effect on MIMO system. The relevant results are presented with simulation verification. The good agreement is achieved. While the good agreement between analysis and experiment would be next goal to provide real guide for IC designer. The pioneer work can be found at [63]. Furthermore other impairment which may induce detrimental effects to MIMO such as PA nonlinearity can be included in future research.

In chapter 3, a radar transceiver architecture based on stretch processing is proposed and analyzed. The specifications of radar are described to meet the UAV radar requirement. And a PA driver delivering 5dBm at 10GHz band was designed and measured. Actually the first RoC chip is under test during the writing of this dissertation. The second phase of X band UAV RoC will adopt multiple antennas to form phase array. Phase array on chip has been attracting more attentions [62]. Applying stretch processing with phase array would be an interesting topic in UAV RoC design.

Chapter 4 presents a novel LMV cell implemented in SiGe bipolar technology. The significant power saving can be achieved if the bipolar technology is replaced by CMOS counterpart. Besides the CMOS implementation can reduce the chip cost as well.

Chapter 5 proposes a harmonic rejection mixer with eight times oversampling sine wave LO. The 3^{rd} order and 5^{th} order harmonics are greatly attenuated. The cost paid is an additional LO generator is necessary to obtain multi phase oversampling LO clocks. The extra overhead limits both the area and minimum power consumption. Due to mixer's passive property, most of energy is consumed on LO generation. A new circuit topology that uses less phase clocks is a good topic as the continuous time counterpart in [3]. Moreover, pushing the operation frequency to over 1GHz is another direction.

Chapter 6 exhibits a wideband DCO replying on multiple coupled inductors. The DCO covers a 70% tuning range. Nevertheless the range is reduced and moved by parasitic. The phase noise is worse than expected from simulation. These phenomena suggest the extracted transformer model might be inaccurate. Precise modeling of inductor and transformer is critical for the successful RFIC design, regardless of targeting blocks, LNA, VCO and PA. Modeling magnetic components on silicon substrate would be an interesting research direction. How to achieve wide bandwidth without suffering noise degradation is another promising topic in oscillator design.

7.2 Possible future works

Based on the above summary, there are still some interesting works to be future research topics.

1) Non-idealities such as nonlinearity of PA can result in MIMO system degradation. This effect needs to be addressed in future MIMO system analysis.

2) Extending the single antenna stretch processing RoC to phase array scenario can be an interesting topic.
3) Implementing the LMV cell in CMOS technology.
4) Building a wideband oscillator without suffering phase noise degradation.

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APPENDIX I

According to Wiener-Khintchine Theorem,

$$E\phi(t)\phi(t+T) = \int_{-\infty}^{\infty} P(\omega)e^{j\omega T}\,df$$

$P(\omega)$ is the power spectral density of phase noise. When PSD falls below -100dBc/Hz for example at 10kHz, the energy outside 10kHz (we call it main lobe) can be skipped. (100dB equals to 10^{10}) Hence

$$E\phi(t)\phi(t+T) \approx \int_{-10\mathrm{k}}^{10\mathrm{k}} P(\omega)e^{j\omega T}\,df$$

Let us assume T=1μS (which indicate 1Msps, a conservative transmission rate compared to modern communication systems). Within main lobe, we have

$$\omega T \leq \pi/50$$

Because of

$$e^{j\frac{\pi}{50}} \approx 0.998 + 0.0628j \approx 1$$

, the above equation becomes

$$E\phi(t)\phi(t+T) \approx \int_{-10\mathrm{k}}^{10\mathrm{k}} P(\omega)\,df$$

Again omit the energy outside of main lobe,

$$E\phi(t)\phi(t+T) \approx \int_{-\infty}^{\infty} P(\omega)\, df = \sigma_{\phi}^{2}$$

Thus Eq. (2-15) holds.

APPENDIX II

Transmitted chirp signal

$s(t) = \cos\left[\pi\alpha(t-\tau)^2\right], 0 \le \tau \le t \le \tau + T_1 \le T_2$, T_1 is transmitter chirp length, T_2 is receiver chirp length, α is chirp frequency modulation rate, τ is echo back chirp time delay relative to beginning of receiver chirp.

$$P_s = \frac{1}{T_1}\int_{\tau}^{\tau+T_1} s^2 dt = \frac{1}{2}$$

$P_n = N_0 \alpha T_1$, N_0 is one side power spectral density of noise, it is assumed noise has white power spectral density in $-\alpha T_1 \sim \alpha T_1$ frequency range.

$$SNR = \frac{1}{2N_0\alpha T_1}$$

Stretch processing is as following:

$$\left[s(t) + n(t)\right] * \cos\left(\pi\alpha t^2\right), 0 \le t \le T_2$$

Signal part is calculated as:

$$s(t) * \cos\left(\pi\alpha t^2\right) = \frac{\cos\left[\pi\alpha(t-\tau)^2 + \pi\alpha t^2\right] + \cos\left[\pi\alpha(t-\tau)^2 - \pi\alpha t^2\right]}{2}, \ \tau \le t \le \tau + T_1$$

The component we care is: $\frac{\cos\left[\pi\alpha(t-\tau)^2-\pi\alpha t^2\right]}{2}=\frac{\cos\left(\pi\alpha\tau^2-2\pi\alpha t\tau\right)}{2}$

Its Fourier transformation is:

$\int_{\tau}^{\tau+T_1}\frac{\cos\left(\pi\alpha\tau^2-2\pi\alpha t\tau\right)}{2}e^{-j\omega t}dt$, the peak value will be located at $\omega=2\pi\alpha\tau$

Hence $\int_{\tau}^{\tau+T_1}\frac{cos(\pi\alpha\tau^2-2\pi\alpha t\tau)}{2}e^{-2j\pi\alpha t\tau}dt=\frac{1}{4}\int_{\tau}^{\tau+T_1}\left[e^{j(\pi\alpha\tau^2-2\pi\alpha t\tau)}+e^{-j(\pi\alpha\tau^2-2\pi\alpha t\tau)}\right]e^{-2j\pi\alpha t\tau}dt$

$=\frac{1}{4}e^{j\pi\alpha\tau^2}\int_{\tau}^{\tau+T_1}e^{-j(2\pi\alpha t\tau+2\pi\alpha t\tau)}dt+\frac{1}{4}e^{-j\pi\alpha\tau^2}\int_{\tau}^{\tau+T_1}e^{j(2\pi\alpha t\tau-2\pi\alpha t\tau)}dt$

$=\frac{e^{j\pi\alpha\tau^2}}{-j16\pi\alpha\tau}e^{-j4\pi\alpha t\tau}\Big|_{\tau}^{\tau+T_1}+\frac{1}{4}e^{-j\pi\alpha\tau^2}T_1=\frac{e^{j\pi\alpha\tau^2}}{-j16\pi\alpha\tau}e^{-j4\pi\alpha\tau^2}\left(e^{-j4\pi\alpha\tau T_1}-1\right)+\frac{1}{4}e^{-j\pi\alpha\tau^2}T_1$

In our case, $\alpha\tau$ is very large, that leads to: Peak value $=\frac{1}{4}e^{-j\pi\alpha\tau^2}T_1$

Its energy is ${T_1}^2/16$.

Noise part:

For noise part, we also want to calculate energy, which is: $E\left|\int_0^{T_2}n(t)cos(\pi\alpha t^2)e^{-j\omega t}dt\right|^2$

$=E\left|\int_0^{T_2}n(t)c(t)e^{-j\omega t}dt\right|^2$, where $c(t)=\begin{cases}\cos\left(\pi\alpha t^2\right) & ,0\le t\le T_2\\ 0 & \text{others}\end{cases}$

$=E\iint n(t_1)c(t_1)e^{-j\omega t_1}n^*(t_2)c(t_2)e^{j\omega t_2}dt_1dt_2$, $c(t)$ is real function

$=\iint r(t_1-t_2)c(t_1)e^{-j\omega t_1}c(t_2)e^{j\omega t_2}dt_1dt_2, r(t_1-t_2)=En(t_1)n^*(t_2)$

As assumed, $r(t_1 - t_2) = \frac{1}{2\pi}\int R(j\omega)e^{j(t_1-t_2)\omega}d\omega,\ R(j\omega) = \begin{cases} N_0/2 & ,|\omega| \le 2\pi\alpha T_1 \\ 0 & ,\text{others} \end{cases}$

And it can be assumed $c(t) = \frac{1}{2\pi}\int C(j\omega)e^{jt\omega}d\omega$, hence the above expression becomes

=

$$\iint \frac{1}{2\pi}\int R(j\omega_1)e^{j(t_1-t_2)\omega_1}d\omega_1 \frac{1}{2\pi}\int C(j\omega_2)e^{jt_1\omega_2}d\omega_2 e^{-jt_1\omega}\frac{1}{2\pi}\int C(j\omega_3)e^{jt_2\omega_3}d\omega_3 e^{jt_2\omega}\,dt_1dt_2$$

$$=\frac{1}{8\pi^3}\iiint R(j\omega_1)C(j\omega_2)C(j\omega_3)d\omega_1d\omega_2d\omega_3 \iint e^{j(t_1-t_2)\omega_1}e^{jt_1\omega_2}e^{-jt_1\omega}e^{jt_2\omega_3}e^{jt_2\omega}\,dt_1dt_2$$

And $\iint e^{j(t_1-t_2)}e^{jt_1\omega_2}e^{-jt_1\omega}e^{jt_2\omega_3}e^{jt_2\omega}\,dt_1dt_2$

$$=2\pi\delta(\omega_1+\omega_2-\omega) * 2\pi\delta(\omega_1-\omega_3-\omega)$$

Again, the above expression is

$$\frac{1}{2\pi}\int R(j\omega_1)d\omega_1 \int C(j\omega_2)\delta(\omega_1+\omega_2-\omega)d\omega_2 \int C(j\omega_3)\delta(\omega_1-\omega_3-\omega)d\omega_3$$

$$=\frac{1}{2\pi}\int R(j\omega_1)C\big(j(\omega-\omega_1)\big)C\big(j(\omega_1-\omega)\big)d\omega_1=\frac{1}{2\pi}\int R(j\omega_1)\big|C\big(j(\omega-\omega_1)\big)\big|^2d\omega_1$$

$$=\frac{N_0}{4\pi}\int_{-2\pi\alpha T_1}^{2\pi\alpha T_1}\big|C\big(j(\omega-\omega_1)\big)\big|^2d\omega_1$$

Specifically we are interested in $\omega = 2\pi\alpha\tau$, which is very close to 0 frequency compared to integral range. And $C(j\omega)$ has relatively flat amplitude frequency response. Hence

$$\approx\frac{N_0}{4\pi}\int_{-2\pi\alpha T_1}^{2\pi\alpha T_1}|C(-j\omega_1)|^2d\omega_1=\frac{N_0}{4\pi}\int_{-2\pi\alpha T_1}^{2\pi\alpha T_1}|C(j\omega_1)|^2d\omega_1$$

If we consider $C(j\omega)$ as the Fourier transform of $C(t)$ from 0~T_1, then the frequency goes no more than $2\pi\alpha T_1$. Hence above expression is

$$\approx \frac{N_0}{4\pi}\int_{-\infty}^{\infty}|C(j\omega_1)|^2 d\omega_1 = \frac{N_0}{2}\int_{-\infty}^{\infty}|C(t)|^2 dt = \frac{N_0}{2}\int_0^{T_1}|C(t)|^2 dt = \frac{N_0}{2}\frac{T_1}{2}$$

$$\text{SNR} = \frac{{T_1}^2}{16} \Big/ \frac{N_0}{2}\frac{T_1}{2} = \frac{T_1}{4N_0}$$

The SNR improvement is $\frac{{T_1}^2}{4N_0} \Big/ \frac{1}{2N_0\alpha T_1} = \frac{\alpha {T_1}^2}{2}$