Drain Current Noise Spectrum Measurement in 0.18 μm MOSFET Using Integrated SiGe HBT Low-Noise Transimpedance Amplifier

by

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Abstract

We measured drain current noise power spectral density (PSD) in 0.18 μm metal oxide semiconductor field effect transistor (MOSFET) using integrated Silicon-Germanium (SiGe) Heterojunction Bipolar Transistor (HBT) low-noise transimpedance amplifier (TIA). This measurement system extends the noise-measuring capabilities beyond 2.5 GHz to detect the white noise component beyond the 1/f noise corner frequency. In this work, the corner frequency is approximately 2 GHz, which comes from radio frequency (RF) thermal noise measurement directly instead of the extension line of 1/f noise at low frequencies. PSD of drain current thermal noise is in the range from 1×10^{-22} A^2/Hz to 5×10^{-22} A^2/Hz for drain current from 1mA to 12 mA. S-parameters are measured to calculate the gain of device under test (DUT) and TIA system.

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List of Abbreviations

SiGe	Silicon-Germanium
HBT	Heterojunction Bipolar Transistor
TIA	Transimpedance Amplifier
DUT	Device Under Test
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
NMOS	N-Type Channel Metal–Oxide–Semiconductor
PSD	Power Spectral Density
RF	Radio Frequency
LNA	Low Noise Amplifier
SA	Spectrum Analyzer
VSD	Voltage Spectral Density
NF	Noise Figure

Chapter 1

Introduction

All semiconductor devices generate noise that can interfere with weak signals when used in circuits. Therefore, it is important to find ways to measure noise. There are several types of fundamental noise present in semiconductor device: thermal noise, flicker noise also called 1/f noise, shot noise, generation-recombination noise and burst noise. These noises vary with device structure and operating conditions. Thermal noise and flicker noise are two major types of noise in metal oxide semiconductor field effect transistor (MOSFET). The purpose of Chapter 1 is to introduce these different types of noise, especially the thermal noise in MOSFET.

A typical drain current noise PSD versus frequency plot is shown in Figure 1.1.Theoretically, a plot of drain current noise power-spectral density versus frequency in log-log axes is a straight line with the slope of approximately 1/f at low frequency and a horizontal line at high frequency. There is a corner at the intersection of these two lines which is valued from several hertz to several gigahertz depending on device geometry, construction, and bias. With the development of semiconductor technology, the corner frequency becomes higher and higher [1]. Usually, 1/f noise is measured using time domain equipment [2], such as dynamic signal analyzer. Since the drain current thermal noise is too weak to be measured directly, the main method for thermal noise measurement is based on measurement of noise parameters [3], such as noise figure (NF). Chapter 2 gives background material for thermal noise measurement method. The history of thermal noise measurement for MOSFET is introduced. Our noise measurement system and basic working theory are described. The algorithm used here is specific for our test system. The on-chip Silicon-Germanium (SiGe) Heterojunction Bipolar Transistor (HBT)

Transimpedance Amplifier (TIA) used to amplify drain current noise, is introduced. There are several requirements for TIA to meet to be able to measure MOSFET drain current noise.

Chapter 3 describes the process of noise measurement and analysis of experimental result. The power spectral density (PSD) of drain current noise S_{id} and thermal noise factor γ are extracted. We find that S_{id} increases with I_{DS} at fixed $V_{DS.}$ It also increases with V_{DS} at fixed V_{GS} as well as increases with V_{GS} at fixed V_{DS}. The values of noise factor γ from our extraction are consistent with reported values in literature for similar technologies.

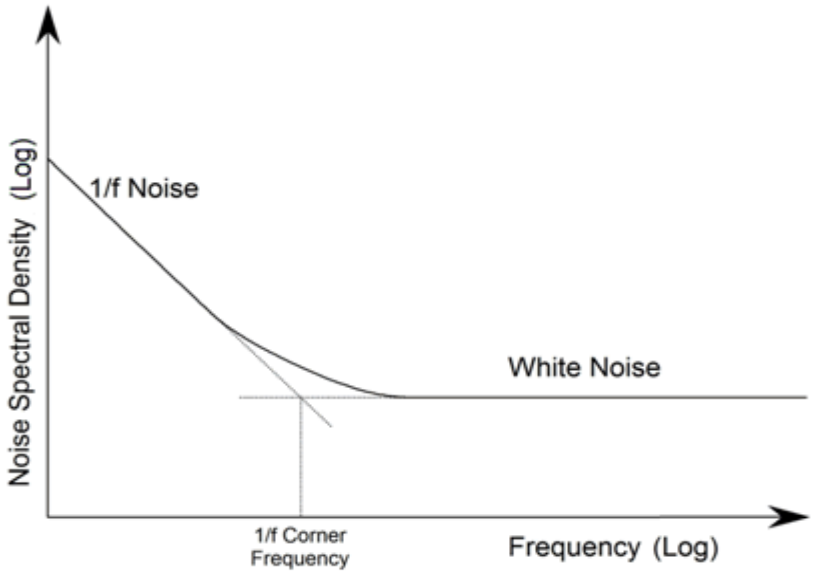

Figure 1.1 A typical plot of the drain current noise versus frequency in log-log axes.

Different types of fundamental noise are present in semiconductor devices: thermal noise, flicker noise (1/f noise), generation-recombination noise, shot noise and burst noise. Thermal noise and shot noise are white noise. 1/f noise origin remains a mystery. Thermal noise and 1/f noise are the two major concerns for drain current noise measurement.

With channel length scaling and the carrier mobility improvement, the cut-off frequency of MOSFET can go up to hundreds of gigahertz [4]. Hence, MOSFET are widely used in high

speed radio frequency RF integrated circuits. In these circuits, drain current noise becomes a critical issue.

1.1 Thermal Noise

Thermal noise is generated by random motion of free carriers in resistive materials. It is present in all circuit elements containing resistance regardless of any applied voltage. In 1928, J.B. Johnson was the first to prove that there is fluctuating movement of charges in thermal equilibrium [5]. In an ideal resistor, thermal noise is independent of frequency. In other words, the power spectral density is nearly constant throughout the frequency spectrum for a fixed bandwidth.

1.1.1 Drain Current Thermal Noise

Starting from van der Ziel (1962) [6], many drain current thermal noise models are developed. In 2002, Chen and Deen proposed their new model which considered the channel length modulation (CLM) effect [7]. In 2005, Paasschens, Scholten & van Langevelde provided channel thermal noise model which considered velocity saturation effect and separated the position and voltage dependence for the channel conductance [8]. The noise factor γ was discussed in both [7] and [8]. This noise factor was introduced in one of the most prevalent models for drain current noise PSD, $S_{id,}$ in long channel device at strong inversion region by van der Ziel [1]:

$$S_{id} = 4KT\gamma \cdot g_{ds0}, \tag{1.1}$$

where

$$g_{ds0} = \frac{\partial I_{DS}}{\partial V_{DS}} = \mu C'_{ox} \frac{W}{L}(V_{GS} - V_T), \tag{1.2}$$

$$\gamma = \frac{\int_0^{Vd} [g(V_0)/g_0]^2 dV_0}{\int_0^{Vd} [g(V_0)/g_0] dV_0}, \qquad (1.3)$$

K is Boltzmann constant, T is absolute temperature, γ is thermal noise factor, g_{ds0} is drain-source conductance evaluated at drain-source voltage V_{DS} = 0 V, W is channel width, L is channel length, μ is channel mobility, C'_{ox} is oxide capacitance per unit area, V_{GS} is gate-source voltage and V_T is threshold voltage, g(x) is the conductance per unit length, V_0(x) is the channel potential at the point, g_0 is conductance at V_0=0. The value of γ is 2/3 and 1 in the saturation and triode regions for long channel device, respectively.

With technology scaling, C'_{ox} is increased, μ is decreased while the product $\mu C'_{ox}$ is increased [4]. If $\frac{W}{L}$ and $V_{GS} - V_T$ are fixed, both g_{ds0} and S_{id} increase with reducing the physical size of devices. If L is fixed for a certain technology, increasing W can result in increasing S_{id}.

The parameter γ as a noise factor is defined [1] from equation (1.1) as

$$\gamma = \frac{S_{id}}{4KTg_{ds0}}. \qquad (1.4)$$

Later, the γ values are found higher than 2/3 in a short channel transistors working in the saturation region [7-10]. Actually, γ values are different with different semiconductor technologies [10]. γ is widely used in literatures to demonstrate the enhanced channel thermal noise in short channel transistors as shown in Figure 1.2. The γ range measured in our work is from 0.22 to 0.53 at bias sets V_{DS} from 0.18 V to 1 V and V_{GS} from 0.51 V to 0.64 V in 0.18 μm technology. The bias sets we used are in moderate region. The values of γ are from 1 to 2 at bias sets V_{DS} from 1.5V to 1.8V and V_{GS} from 1 to 1.8 in the same technology shown in Figure 1.2. More comparisons are discussed in section 3.2.

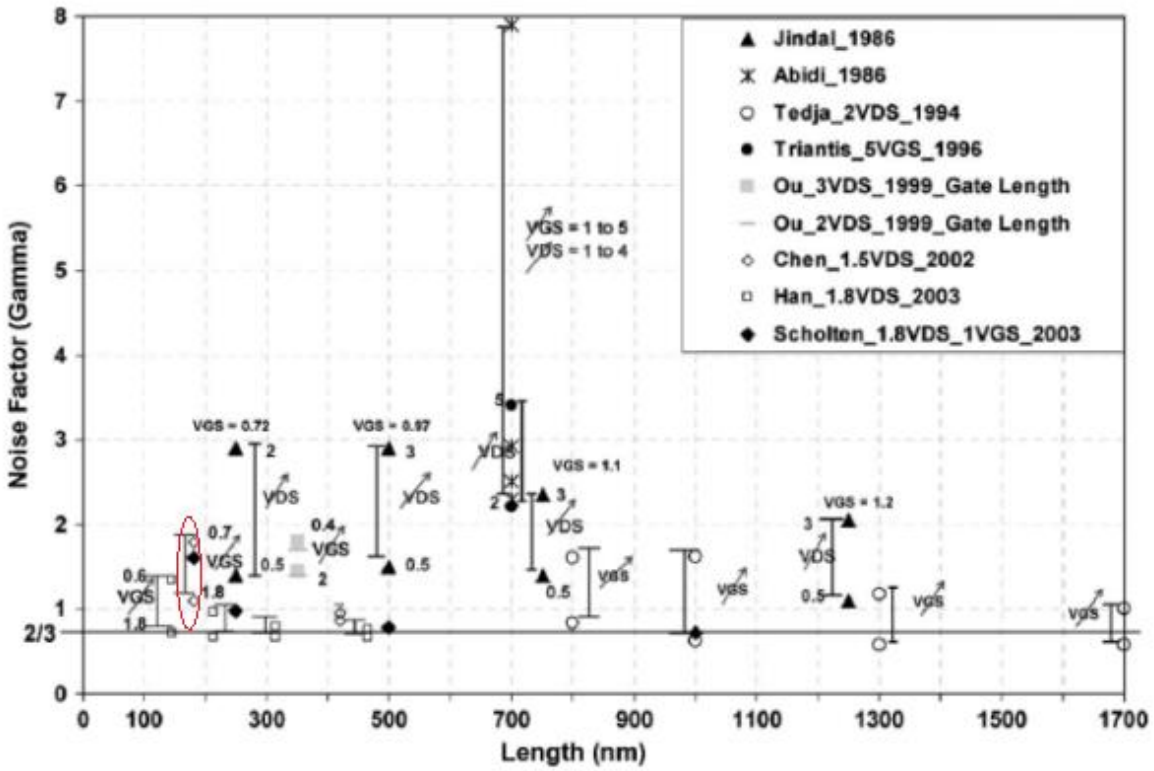

Figure 1.2 Measured γ values for different technologies reported in the literature [10].

1.1.2 Induced Gate Noise

Random fluctuations of the potential in the channel are coupled to the gate terminal through the oxide capacitance leading to induced potential fluctuations on the gate. Drain noise and gate noise are correlated in MOSFET with frequency dependence.

In van der Ziel model [1], PSD of gate current noise S_{ig} is given by:

$$S_{ig} = 4KT\beta g_G \tag{1.5}$$

where β = 4/3, and the saturation gate conductance g_G is:

$$g_G = \frac{4}{45}\frac{\omega^2 (C'_{ox} WL)^2}{g_m} \tag{1.6}$$

where g_m is transconductance.

In saturation, the cross-correlation of reduced gate current noise and drain current noise is given by [1],

$$\overline{i_g i_d^*} = i\omega \frac{C'_{ox} WL}{q} 4KT \tag{1.7}$$

where i is the imaginary unit. The correlation coefficient between gate and drain current fluctuations is i0.4 [1].

The gate-to-source capacitance decreases when the channel length decreases. Hence, both induced gate noise and its correlation with the channel thermal noise decrease [11]. The origin of this comparatively low coefficient is induced charge profile on the gate, and it will not occur in short channel MOSFET [12]. In 0.18 μm technology which is used in our project, PSDs of the channel noise (drain current noise), induced gate current noise, correlation of induced gate current noise and drain current noise, and cross-correlation coefficient are extracted [12] and shown in Figure 1.3.

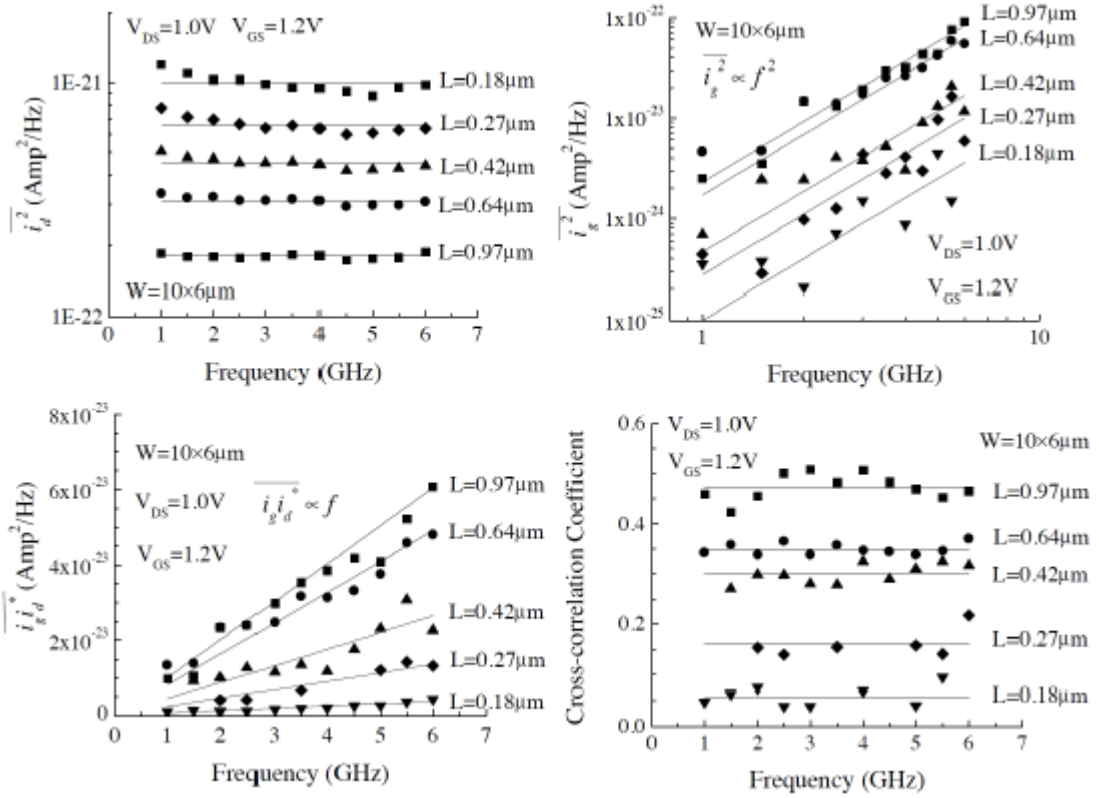

Figure 1.3 Channel noise, induced gate noise, correlation of these two noises, and cross-correlation coefficient as a function of frequencies for devices with different channel lengths [12].

1.2 Flicker Noise (1/f Noise)

Unlike other noises, there are many different explanations of the origin of flicker noise or 1/f noise. There are two major models and concepts for 1/f noise [13]. The first theory describes the origin of 1/f as the random fluctuation of the number of carriers in the channel because of the fluctuations in the surface potential [4]. PSD of the equivalent drain noise current S_{id} can be calculated by [4]

$$S_{id} = \frac{K_1}{C'^{2}_{ox}} \frac{1}{WL} \frac{1}{f^{c}} g_m^{2} \tag{1.8}$$

where $$g_m = \frac{W}{L}\mu C'_{ox}(V_{GS} - V_T) \tag{1.9}$$

in saturation region. K_1 is bias dependent quantity which increases with technology scaling, c is between 0.7~1.2 for n-channel device. This model obtains 1/f noise by superposing many different spectra of generation-recombination noise with a specific statistical distribution of [13]. Free carriers are randomly trapped and released by traps located near the silicon-oxide interface, causing noise in drop current.

At corner frequency, thermal noise S_{id} from equation (1.1) equals 1/f noise S_{id} from equation (1.8), so the corner frequency, f_{corner}, is calculated by

$$f_{corner} = \frac{1}{4KT\gamma g_{ds0}} \frac{K_1 g_m^2}{C'^2_{ox} WL} \tag{1.10}$$

Substituting equation (1.2) and (1.9) to (1.10), f_{corner} can be simplified to

$$f_{corner} = \frac{K_1 \mu (V_G - V_T)}{L^2 4KT\gamma}. \tag{1.11}$$

If (V_G-V_T) is fixed, f_{corner} increases with decreasing L. With technology scaling, f_{corner} becomes bigger and bigger.

The second theory attributes 1/f noise to the mobility [4]. Under this theory, PSD of the equivalent drain noise current is given by

$$S_{id} = \frac{K(V_{GS})}{C'_{ox}} \frac{1}{WL} \frac{1}{f} g_m^2 \tag{1.12}$$

where $K(V_{GS})$ is bias dependent quantity. In this model, both lattice scattering and impurity scattering are considered. It is assumed that only scattering on the silicon lattice generates 1/f noise. Similar to the first model, if V_G and V_T are fixed, f_{corner} increases with decreasing L.

In our work, DUT is a NMOS with channel width $W = 100 \times 3.2$ μm where100 is gate finger number, and channel length L = 0.18 μm. The reported noise factor γ for that technology is approximately in the range from 2/3 to 2 for several bias sets in [7], [12] and [14]. The corner frequency we measured is approximately 2 GHz.

Chapter 2

Drain Current Noise Measurement Methods

As mentioned in Chapter 1, the corner frequency becomes higher and higher with the development of semiconductor technology in MOSFET. To measure thermal noise which dominates after 1/f corner frequency, the noise measurement should be taken in very high frequency and it is up to several gigahertz for modern semiconductor technologies. Another difficulty is the thermal noise is too weak to be measured directly on noise measurement equipment. The main method for thermal noise measurement is based on measurement of noise parameters [3], F or NF. From 1986, TIA is used as a low noise amplifier (LNA) to boost the drain current noise and improve the measurement accuracy [8]. Approximately one decade later, TIA is integrated with DUT on chip for gallium arsenide GaAs metal-semiconductor field effect transistor MESFET[15] to reduce the parasitic capacitance and inductance. In our project, SiGe HBT TIA is integrated with a NMOS on chip to help with drain current noise measurement in 0.18 μm technology.

2.1 Noise-Parameters Measurement System

Different from the 1/f noise measurement, where the noise PSD can be directly measured using a dynamic signal analyzer, the main thermal noise measurement method is measuring the noise factor F (or noise figure NF in dB) and/or its well-known noise parameters developed by Haus et al. in [16], to evaluate the thermal noise characteristics. In [16], F (or NF) is presented as a mathematical equation

$$NF = NF_{min} + | Y_s - Y_{opt} |^2 \frac{R_n}{G_s} \tag{2.1}$$

where $Y_s = G_s + i B_s$ is the admittance of source, $Y_{opt} = G_{opt} + i B_{opt}$ is optimized source admittance, NF_{min} is minimum noise figure, R_n is equivalent noise resistance. This representation is based on a noisy two-port network expended from Rothe and Dahlke in [17]. Haus et al.'s impedance-based representation [16] demonstrates the dependence of noise factors on the source admittances attached to the input port of the noisy two-port network. In the measurement, NF is measured by Noise Figure Analyzer NFA for certain Y_s firstly, noise parameters NF_{min}, R_n and Y_{opt} can be calculated from equation (2.1). Then these noise parameters are expressed as functions of two-port network chain representation A, B, C and D [16]. Finally, drain current noise can be acquired [18-22]. Under the theory of this two-port noise representation [16], many noise measurement and extraction methods have been developed [18-22].

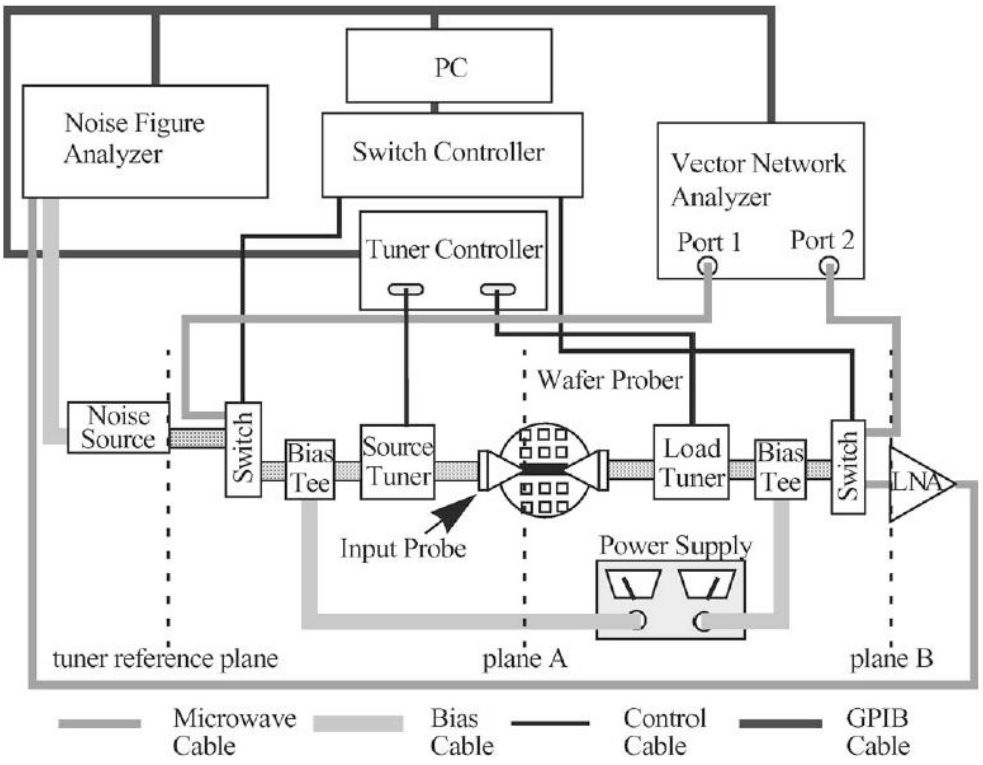

Figure 2.1 System configuration for radio frequency noise measurements [22].

Figure 2.1 is the system configuration for noise measurement in [22]. This system consists of a noise source, a noise figure analyzer (NFA), a vector network analyzer (VNA), low noise amplifier (LNA), microwave impedance tuners, power supply and other peripheral components, such as PC, switches and bias tees. In Y-factor or hot/cold-source technique [23], the calibrated noise source generates two noise outputs with different equivalent noise temperatures, hot temperature (T_{hot}) and cold temperature (T_{cold}). Under the theory of impedance-based two-port noise network [16], the impedance of the network should adjust. The source tuner and load tuner are used to provide different source admittances and to match the output of the DUT for a maximum power transfer, respectively [23]. These two tuners are controlled by tuner controller in this system. LNA is used to boost the weak noise signal to allow the noise signal been measured by NFA. PNA is to measure S-parameters of the impedance tuner S_T and receiver S_R which are defined in the following section and shown in Figure 2.2.

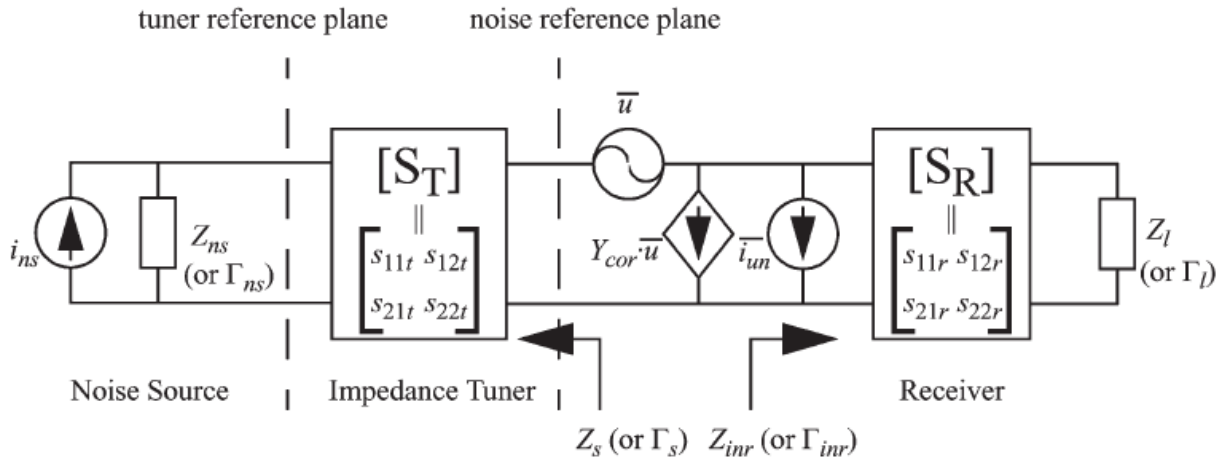

Figure 2.2 Schematic diagram for the measurement system shown in Figure 2.1[22].

Figure 2.2 is the schematic diagram for the measurement system shown in Figure 2.1. This measurement system contains three parts: noise source, an impedance tuner and a receiver. In the system calibration stage, a THRU line is placed between the input and output probes. Then,

noise reference plane in Figure 2.2 is corresponding to plane B in Figure 2.1. In other words, the impedance tuner in Figure 2.2 contains all the components from tuner reference plane to plane B in Figure 2.1, and the receiver in Figure 2.2 includes LNA, NFA and the cable between them in Figure 2.1. In the measurement stage, DUT takes the place of the THRU line. The noise reference plane in Figure 2.2 is moved to plane A in Figure 2.1. All the components between plane A and plane B in Figure 2.1 are included in receiver in Figure 2.2. Based on the noise reference plane in Figure 2.2, the noise power P_n detected by NFA is expressed by [22]

$$P_n = \frac{G_{tr}}{4R_s} \cdot [4KT_{sef} f\Delta fRs + |\overline{i_{un}}|^2 |Z_s|^2 + |\overline{u}|^2 \cdot (1 + |Y_{cor}|^2 |Z_s|^2 + 2G_{cor}R_s - 2B_{cor}X_s)] \qquad (2.2)$$

where Δf is noise bandwidth, R_s is source resistance, X_s is source reactance, Z_s is source impedance seen at the noise reference plane (= $R_s + i \cdot X_s$), $\bar{u}$ is input referred noise voltage [17], $\overline{i_{un}}$ is input referred noise current [17], G_{cor} is correlation conductance, B_{cor} is correlation susceptance, Y_{cor} is complex correlation admittance (= $G_{cor} + i \cdot B_{cor}$) [17], G_{tr} is transducer power gain of the receiver, T_{seff} is effective source temperature experienced at the noise reference plane. After conversions step by step in [22], noise parameters NF_{min}, R_n and Y_{opt} are expressed using the parameters shown in equation (2.2). Then NF_{min}, R_n and Y_{opt} are represent by chain parameters A, B, C and D. At last, the drain current noise can be calculated. As the main high frequency measurement method, the noise parameters measurement method is widely used and there are lots of relative literatures [18-23]. However, drain current noise cannot be measured directly using this method. Another method which can measured the drain current noise directly is described in section 2.2.

2.2 Noise PSD Measurement Using Discrete TIA

Another method of noise measurement is to amplify drain current noise using a low-noise transimpedance amplifier TIA [8,22,24]. Figure 2.3 shows the setup used by Tedja in measuring noise of spectrum of MOSFET from a 1.2 μm technology.

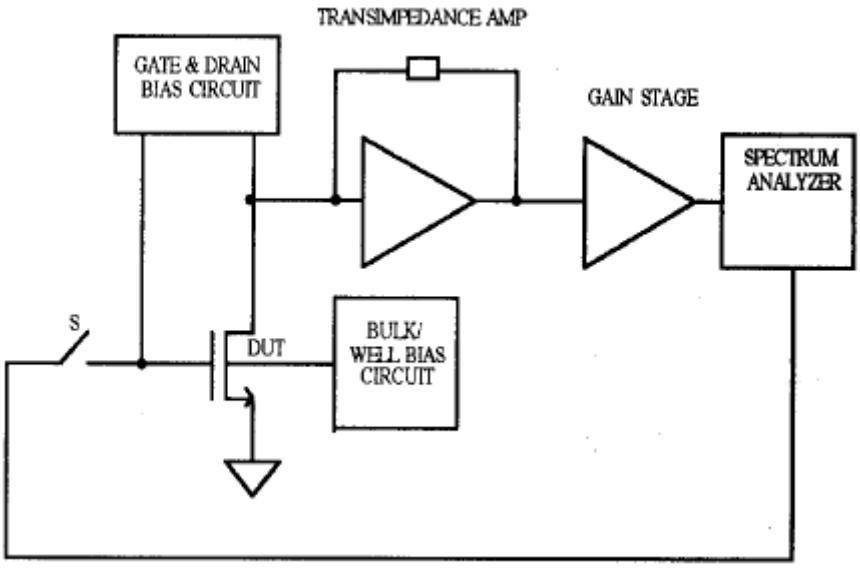

Figure 2.3 Block diagram of the noise PSD measurement set-up [24].

The noise current at the drain node of the DUT (or equivalently the input node of TIA) is dominated by the drain current noise. In the noise measurement stage, switch S is open and the drain current noise flows into a discrete TIA. Then the combined voltage from drain current noise and TIA noise at the output of the TIA is further amplified by a gain stage. At last, the resulting voltage was detected by SA. In [24], the measured result on SA is considered to be the drain current noise PSD multiplied by the gain of the amplifiers following the DUT if the TIA and the gain stage were noiseless. The extra noise in the measurement system, such as the noise from TIA, gain stage and biasing circuit, is re-measured when the DUT is turned off. In the system transfer function measurement stage, switch S is closed and a known signal from SA is fed into the DUT. After subtracting the extra noise from the output noise voltage spectral density

VSD, the output noise VSD is referred to the input of the DUT which is called input referred noise VSD (or called gate referred noise VSD in [25]) by dividing it by the overall gain or transfer function of the whole noise measurement system. A typical input noise voltage spectral density is shown in Figure 2.4

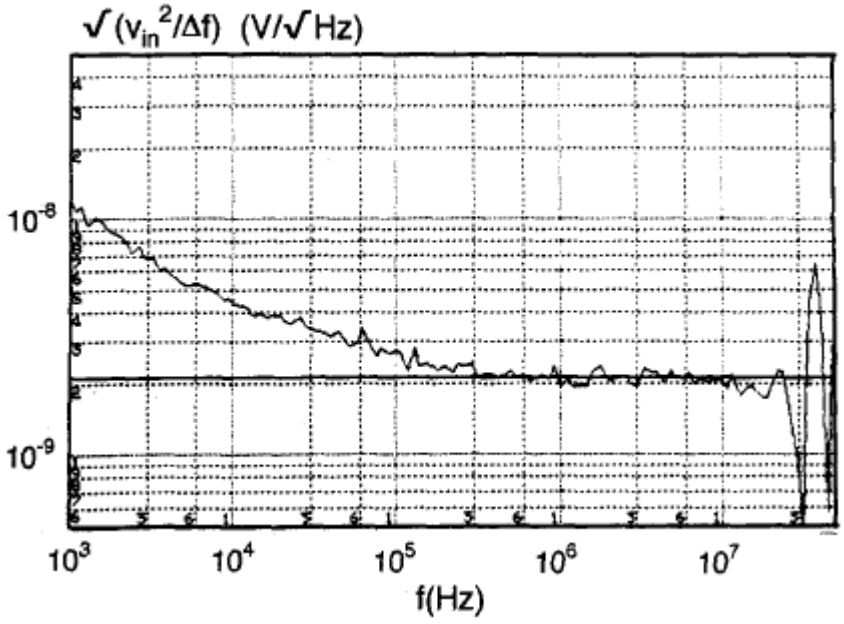

Figure 2.4 A typical equivalent input noise VSD [24].

The equivalent PSD of input voltage noise is given by [24]

$$\frac{\overline{V_{in}^{\,2}}}{\Delta f} = 4KT\varepsilon\frac{1}{g_m} + \frac{B}{f^{\alpha}} + 4KT(R_B' + R_G) \tag{2.2}$$

where $\varepsilon = \gamma\frac{g_{ds0}}{g_m}$, $R_B' = \frac{g_{mb}^{\,2}}{g_m^{\,2}}R_B$, B is the flicker noise coefficient, α is the power of the 1/f noise term (≈1), R_B' is the effective bulk noise resistance, R_B is the bulk resistance, R_G is the resistance of the poly-silicon gate and the gate interconnects. This equation also implies the gate is AC shorted to ground during noise measurement, which necessitates consideration of R_B and R_G noise as $4KT(R_B' + R_G)$. S_{id} can be calculated by multiplying $V_{in}^{\,2}$ by $g_m^{\,2}$.

One disadvantage of the noise measurement system in [24] is that the 50 Ω source resistance of SA is not considered in the measured overall gain or transfer function. At higher frequencies, the 50 Ω source resistance of SA cannot be neglected, as we will illustrate below in section 2.3. In our work, the overall gain portion is optimized by using S-parameters measurement instead of the transfer function measurement in [24].

2.3 Noise PSD Measurement System Using Integrated TIA on Chip

To reduce the parasitic capacitance and inductance, the noise PSD measurement system is optimized by integrating the TIA with DUT on chip [15]. In [15], both GaAs MESFET DUT and TIA are integrated on chip as shown in Figure 2.5. The frequency range for this system is up to 10 MHz and a sample measured result is shown in Figure 2.6. One contribution of our work is showing the measured data in much higher frequency up to approximate 2.5 GHz in 0.18 μm technology.

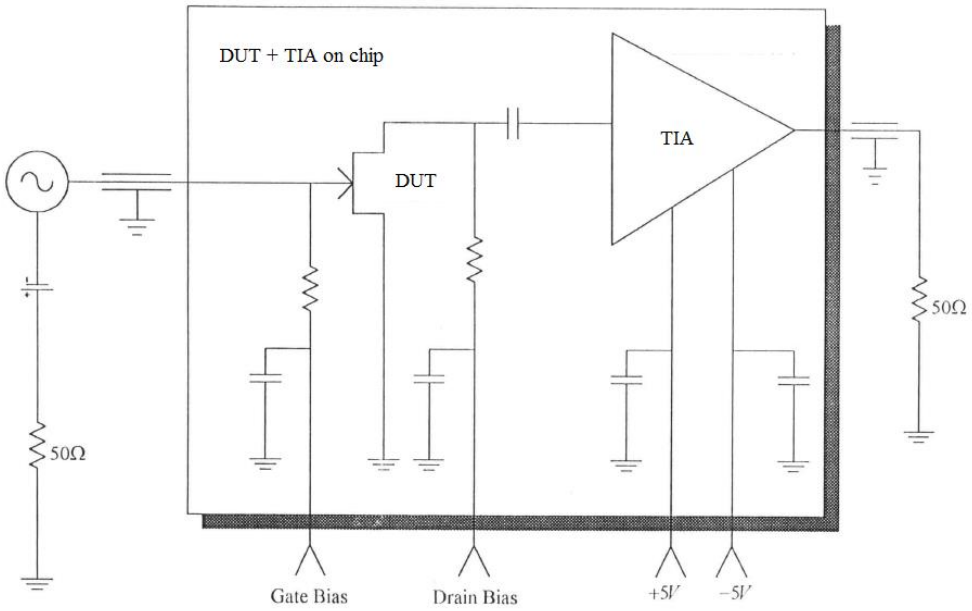

Figure 2.5 Noise measurement system using integrated TIA on chip.

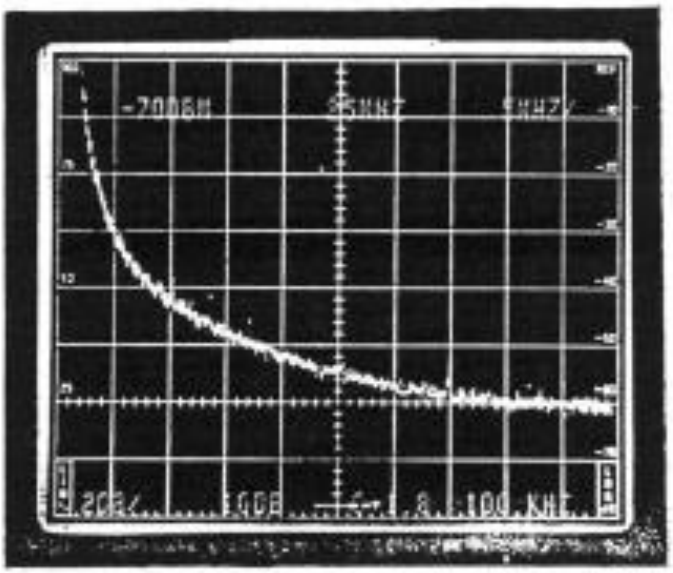

Figure 2.6 A sample noise power measured result [5].

2.3.1 Noise Measurement System in the Thesis

SiGe HBTs are widely used to design low noise amplifier [26]. In our project, we use a new TIA which has a bandwidth up to 2.5 GHz to allow us to detect the white noise component beyond the 1/f noise corner frequency. As shown in Figure 2.7, DUT and TIA are AC coupled and the output impedance of the DUT plus resistor on drain node is much larger than the equivalent input impedance of Cc plus TIA part, so that the drain current noise current i_d can flow into the TIA and be amplified there. A voltage buffer with an output impedance of 50 Ω is used to drive a 50 Ω spectrum analyzer.

The size of DUT is: W/L= 100 $\times$3.2 / 0.18 μm, where 100 is the number of gate figures, 3.2 μm is the gate finger width. As discussed in section 1.2, the chosen size of DUT affects noise measurement. With increasing the channel width, the thermal noise increases while 1/f noise

decreases. Hence the corner frequency decreases, making the thermal noise easier to measure. However, the channel width cannot go to infinity. One important reason is that the output impedance of DUT decreases with increasing the channel width.

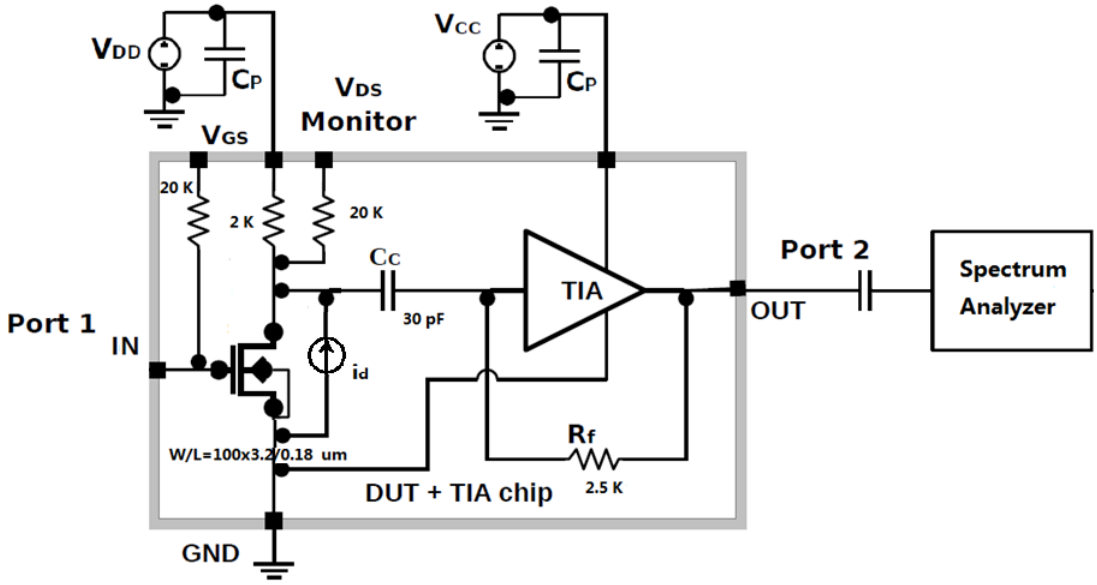

Figure 2.7 Noise measurement system using SiGe TIA on chip.

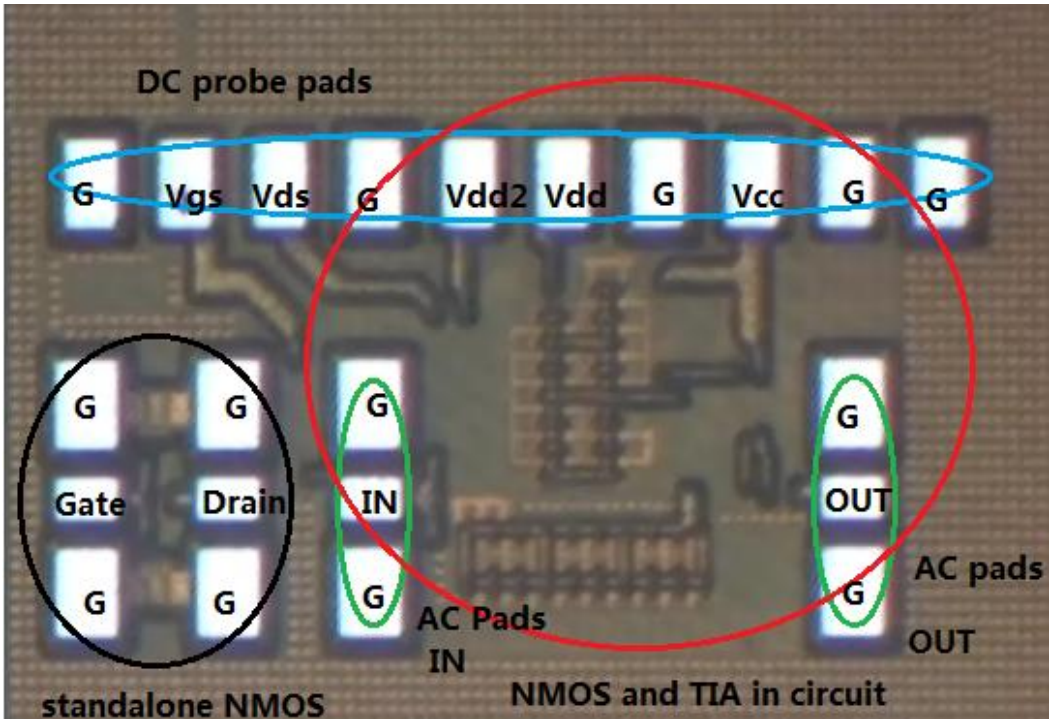

Figure 2.8 Die photo with DUT and TIA on chip.

Figure 2.8 shows one test die under microscope. The big circle on the right contains the DUT and TIA in circuit. The circle on the left contains the standalone NMOS which is designed to be the same structure as the NMOS in the circuit, and the size of the NMOS is the same as DUT in circuit. The standalone NMOS is used for DC and RF characteristics.

In Figure 2.7, DC pad V_{CC} is used to connect DC power supply for TIA. DC pad V_{DD} is used to connect DC power for drain terminal of the DUT. There is a resistor R_{DD} between V_{DD} and drain terminal to avoid drain current noise flow out from V_{DD} pad. Because that R_{DD} produces noise $i_{n,\ RDD} = \sqrt{4KT / R_{DD}}$, to ignore $i_{n,\ RDD}$ when measuring drain current noise id= $\sqrt{4KT\gamma g_{ds0}}$, $i_{n,\ RDD}$ should much less than id, which means $\frac{1}{R_{DD}} << \gamma g_{ds0}$. γ is around 1, so $R_{DD} >> \frac{1}{g_{ds0}}$. In our work, g_{ds0} is in the range of 30 mS to 80 mS, so $\frac{1}{g_{ds0}}$ is approximately from 10Ω to 30 Ω. Hence, 2 KΩ is a big enough value for R_{DD}. Since there is a resistor R_{DD} between V_{DD} and drain terminal, the value of V_{DD} is much higher than the voltage applied to drain terminal. If R_{DD} is too large, V_{DD} need to be very high to achieve a certain $V_{DS,}$ which may exceed the range of DC power supply. A tiny current source $i_{DS,}$ such as10 nA, is applied to DC pad V_{DS} to monitor the voltage actually applied to drain terminal V_{DS}. DC pad V_{GS} or AC pad IN is used to connect power supply for the gate. There is a 20 KΩ resistor $R_{g,bias}$ between V_{GS} pad and the gate terminal.

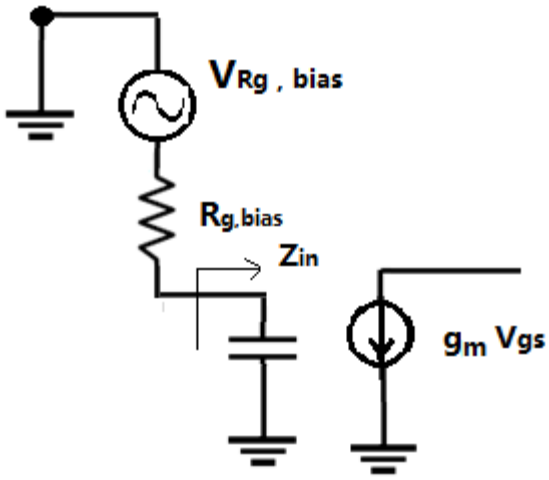

Figure 2.9 Simplified equivalent circuit for noise from $R_{g,bias}$.

Consider the noise from $R_{g,bias}$ as an equivalent voltage noise source $V_{Rg,bias}$ in Figure 2.9, the PSD of drain current noise from $R_{g,bias}$ $S_{id,Rgbias}$ can be calculated as

$$S_{id,Rgbias} = g_m^2 V_{Rg,bias}^2 \left(\frac{Z_{in}}{Z_{in} + R_{g,bias}} \right)^2 \approx g_m^2 V_{Rg,bias}^2 \left(\frac{Z_{in}}{R_{g,bias}} \right)^2 \tag{2.3}$$

where Z_{in} is equivalent input impedance approximately 100 Ω, g_m is the transconductance of the DUT, and the square of equivalent input voltage for $S_{id,Rg}$, $V_{in,Rgbias}^2$, is given by

$$V_{in,Rgbias}^2 = 4KTR_{g,bias} \left(\frac{Z_{in}}{R_{g,noise}} \right)^2 = 4KT \frac{Z_{in}^2}{R_{g,noise}} \tag{2.4}$$

To ignore $S_{id,Rgbias}$, $V_{in,Rgbias}^2$ in equation (2.4) should be much smaller than $4KT\gamma \frac{g_{ds0}}{g_m^2}$. $\frac{g_{ds0}}{g_m^2}$ and Z_{in} can be acquired by DC measurement and S-parameters measurement which are discussed in detail in Appendix A and B, respectively. So we can choose a large enough value for $R_{g,bias}$.

Hence, the output power show on SA is the amplified drain current noise plus noise power of TIA (TIA noise floor).

The TIA noise contribution to the output is first measured by turning the device off with V_{GS} and V_{DD} both set to 0 (never set V_{GS}=0 and use high V_{DD}, or device is damaged). V_{GS} and V_{DD} are ramped up gradually by monitoring V_{DS} and I_{DS} to desired value, noise measurement is made by SA. Subtracting the previously measured TIA noise contribution gives the desired output noise contributed by DUT. The output power data saved from SA is in dBm unit. To remove the TIA noise, all the measured powers which include TIA noise power and total output power data are convert to watt unit first, and then the TIA noise power is removed from all the total output power leaving the amplified device noise power. After subtracting the TIA noise, the output power is converted back to dBm unit. An example is shown for an active bias point of V_{GS} = 0.51V and V_{DS} = 1V in Figure 2.10.

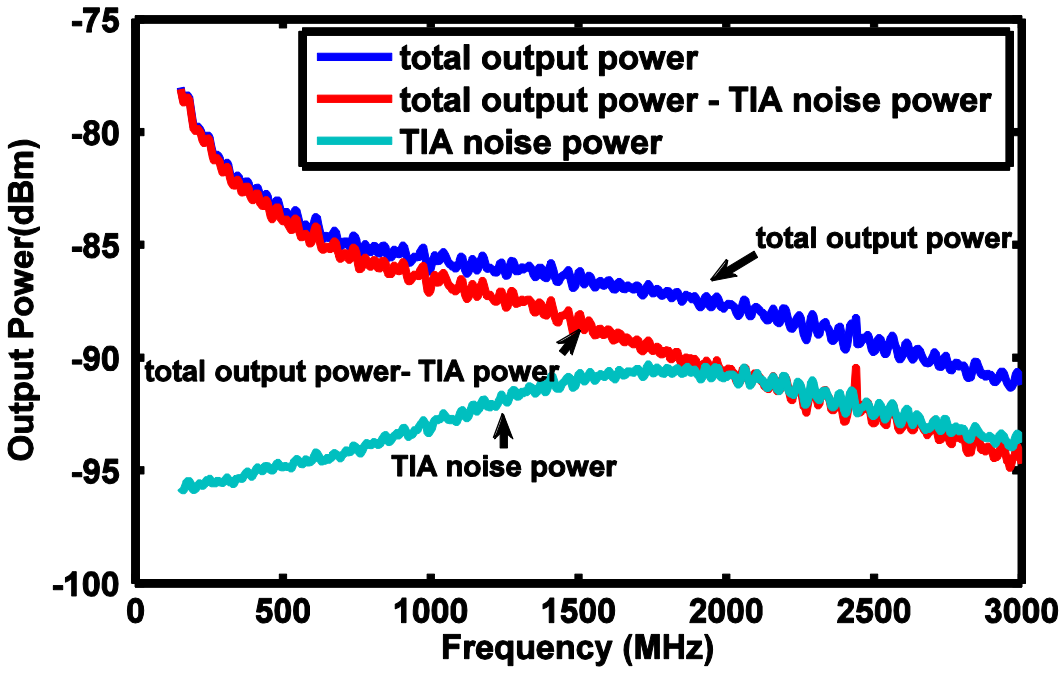

Figure 2.10 A typical output power of amplified noise.

The output power decreases from -78 dBm at 100 MHz to -92 dBm at 3 GHz. $N_{o,noise}$, PSD of the output power, is then calculated and expressed in unit of dBm/Hz as follows [27, 28]:

$$\mathrm{N}_{\mathrm{o,noise}} = 10\log_{10}\frac{\mathrm{P}}{1\mathrm{mW}\cdot\mathrm{BW}} = P_{out}\,|_{dBm} - 10\log_{10} BW \tag{2.5}$$

where BW is measurement bandwidth, and is determined by resolution bandwidth RBW in SA settings [29]. The voltage spectral density VSD of amplified drain current noise $V_{o,noise}$ $(\mathrm{V}/\sqrt{\mathrm{Hz}})$ by converting power to voltage which is given by

$$\mathrm{V}_{o,noise} = \sqrt{10^{\frac{No,noise}{10}-3}\cdot Z_o} \tag{2.6}$$

where Z_o = 50 Ω is the SA input impedance. Figure 2.11 and 2.12 are $N_{o,noise}$ and $V_{o,noise}$ for the same bias set V_{GS} = 0.51V and V_{DS} = 1V as Figure 2.10.

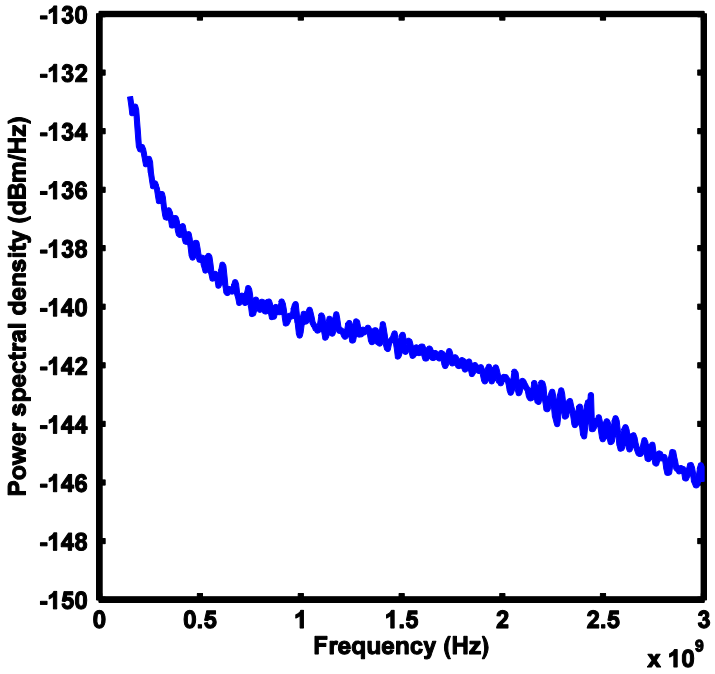

Figure 2.11 A typical output power spectral density of output power.

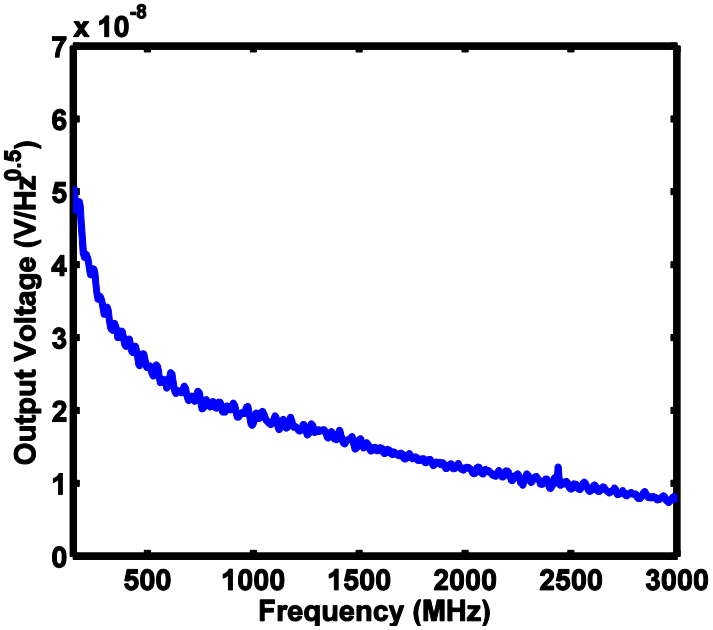

Figure 2.12 A typical output VSD.

Consider the noise measurement system in Figure 2.7 as an equivalent input referred noise voltage source $V_{in,noise}$ added to a noiseless circuit as shown in Figure 2.13. $V_{o,noise}$ has been acquired above. The drain current noise id related to $V_{o,noise}$ by

$$V_{o,noise} = id \cdot Z_{total} \tag{2.7}$$

where $Z_{total} = Z_{TIA} \cdot A_{buffer}$, Z_{TIA} is TIA gain, A_{buffer} is buffer voltage gain. To get Z_{total}, an input voltage signal V_{in} which is large enough to ignore id is added to input port of the network shown in Figure 2.13. The output voltage of the test signal V_{out} is given by

$$V_{out} = V_{in} \cdot g_m \cdot Z_{total}. \tag{2.8}$$

Using equivalent (2.7) and (2.8), an input referred noise voltage $V_{in,noise}$ can be defined as

$$V_{in,noise} = \frac{V_{o,noise}}{\frac{V_{out}}{V_{in}}}. \tag{2.9}$$

Such that $\mathrm{id} = g_m V_{in,noise}$. So the next question is to find $\frac{V_{out}}{V_{in}}$. In [24], a spectrum analyzer is used. This however cannot account for the 50 Ω source resistance, which is not negligible for high frequency, where Z_{in} is only 100 Ω in Figure B.17. We solve this problem using S-parameters measurement. The S-parameters can be converted to Y-parameters which we can use to find $\frac{V_{out}}{V_{in}}$ as below.

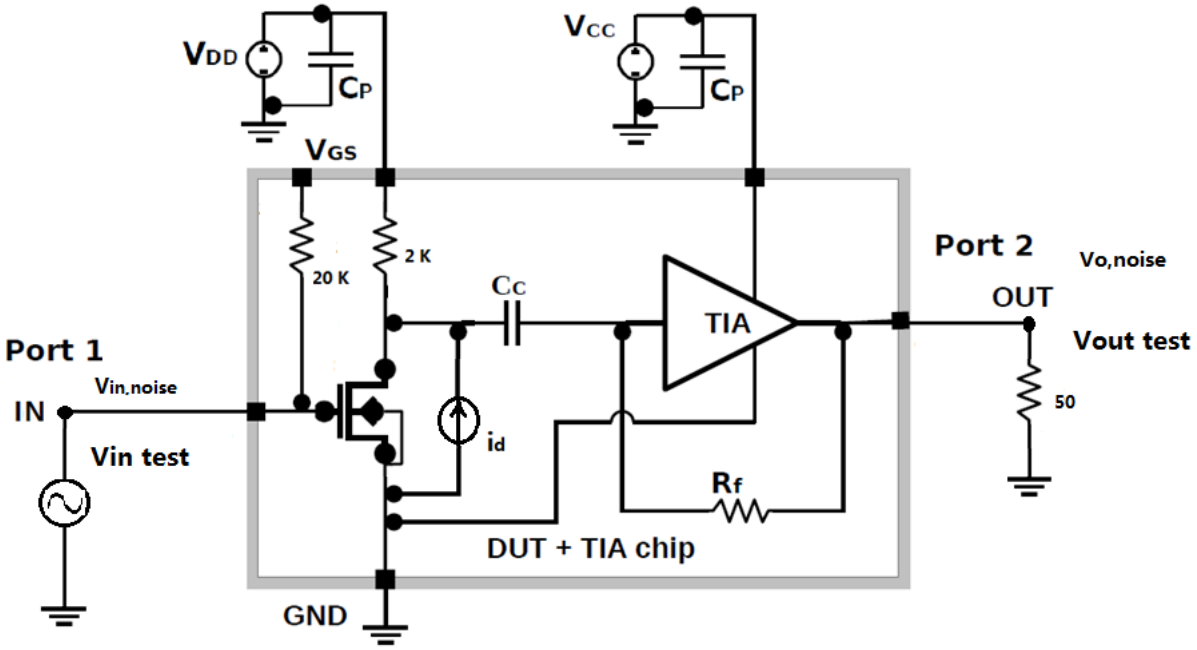

Figure 2.13 Noise measurement system equivalent circuit.

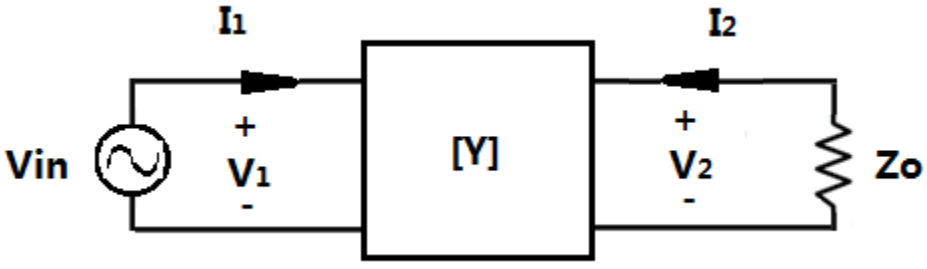

Figure 2.14 Equivalent two ports network.

Consider a two port network as shown in Figure 2.14, and apply an input test voltage V_{in} with a Z_o load, the current at port 2 I_2 is given by [30]

$$I_2 = Y_{22}V_2 + Y_{21}V_1 \tag{2.10}$$

where V_1 and V_2 are the voltages at port 1 and 2, respectively. Y-parameters Y_{21} and Y_{22} can be calculated from S-parameters by [27]

$$Y_{21} = \frac{1}{Z_o}\frac{-2S_{21}}{(1+S_{11})\quad(1+S_{22})-S_{12}S_{21}} \tag{2.11a}$$

$$Y_{22} = \frac{1}{Z_o}\frac{(1+S_{11})\quad(1-S_{22})+S_{12}S_{21}}{(1+S_{11})\quad(1+S_{22})-S_{12}S_{21}} \tag{2.11b}$$

Substituting $I_2 = -\frac{V_2}{Z_o}$, $V_{out} = V_2$ and $V_{in} = V_1$ into equation (2.10), $\frac{V_{out}}{V_{in}}$ is obtained as

$$\frac{V_{out}}{V_{in}} = \frac{V_2}{V_1} = -\frac{Y_{21}Z_o}{1+Y_{22}Z_o}. \tag{2.12}$$

Using equation (2.9) to (2.12), we can calculate $V_{in,noise}$ from $V_{o,noise}$ and S-parameters. $V_{o,noise}$ has been acquired from noise spectrum measurement discussed above and standard on-wafer S-parameters measurement is discussed in Appendix B. $V_{in,noise}(V/\sqrt{Hz})$ at bias V_{GS} = 0.51V and V_{DS} = 1V is plotted in Figure 2.15, $V_{in,noise}$ decreases from 100 MHz to 2 GHz, and then it becomes independent of frequency from 2 GHz to 3 GHz.

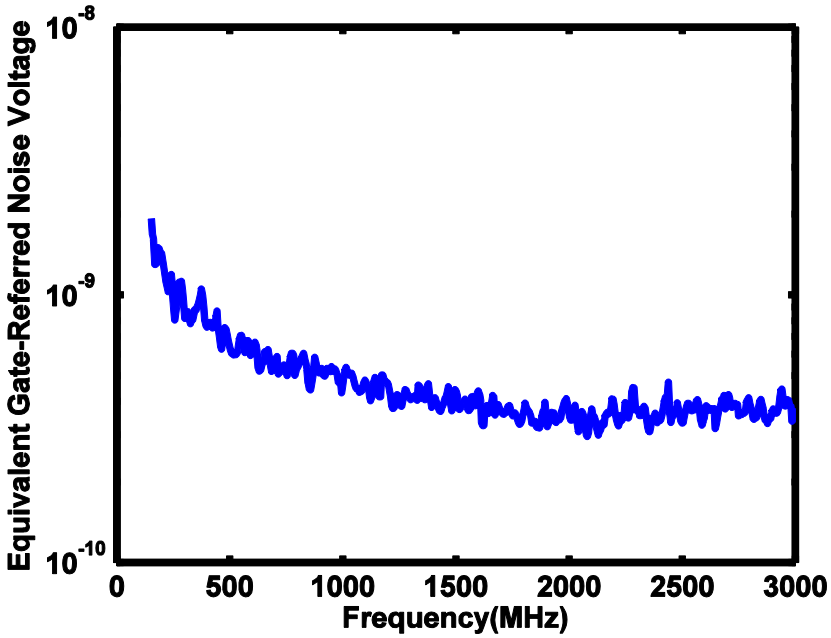

Figure 2.15 A typical $V_{in,noise}$(V/$\sqrt{\text{Hz}}$) vs frequency.

The drain current noise PSD S_{id} can now be calculated from gate-referred noise voltage $V_{in,noise}$ by

$$S_{id} = (g_m V_{in,noise})^2 . \tag{2.13}$$

S_{id} at V_{GS} = 0.51V and V_{DS} = 1V is shown in Figure 2.16.

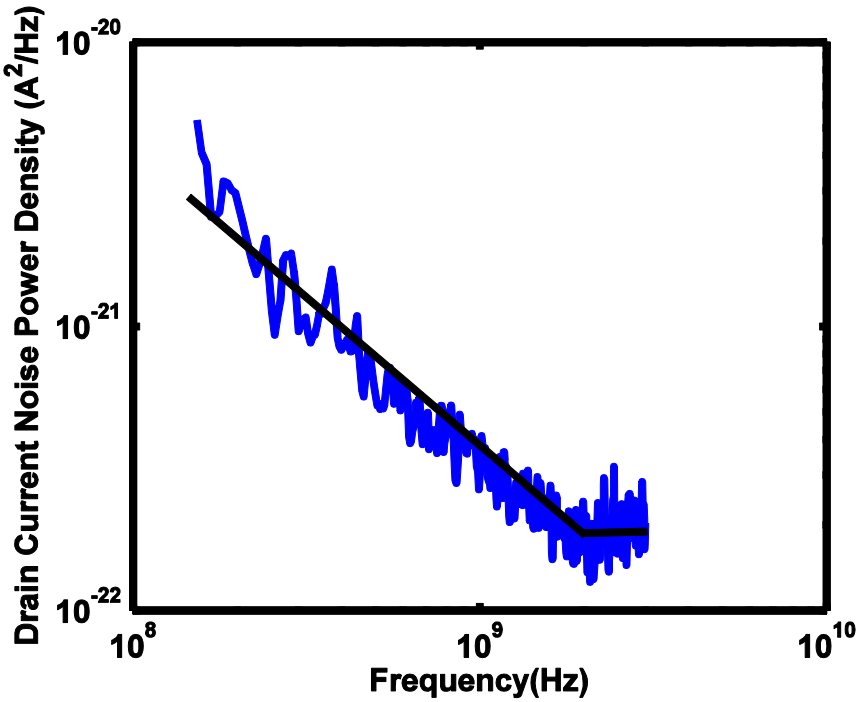

Figure 2.16 A typical S_{id} (A^2/Hz) vs freqency .

From Figure 2.16, we can see the corner frequency for our DUT is around 2 GHz. S_{id} at lower frequencies is nearly proportional to 1/f. S_{id} of the thermal noise component beyond 1/f corner frequency is 1.8×10^{-22} A^2/Hz. When frequency is higher than 2.5 GHz, S_{id} increases a little near 3 GHz. The possible reason is the poor performance of TIA in that frequency range which is discussed in section 3.2.2.

Since noise factor γ is widely used in literatures to demonstrate the enhanced channel thermal noise in short channel transistors. After extracting S_{id}, the noise factor γ is derived using equation (1.3). For bias set V_{GS} = 0.51V and V_{DS} = 1V, γ is shown in Figure 2.17.

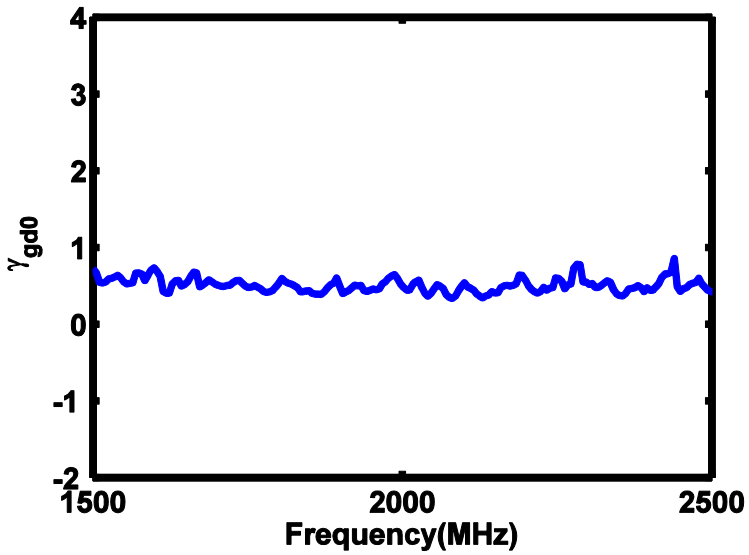

Figure 2.17 Noise factor γ versus frequency.

2.3.2 SiGe HBT TIA

To use TIA as the low noise amplifier, the system must satisfy two requirements to make sure the device noise can be resolved from other noise [8] because that the device noise is not the only noise source in the measurement system. The first requirement is that the amplified noise of the device must be greater than the input noise of the spectrum analyzer which is the SA noise floor. The second requirement is that the equivalent input noise of the amplifier which is the TIA noise floor must be less than the device noise.

In both triode and saturation regions of the MOSFET, the noise amplifier should be driven in a large resistances region presented by the DUT. In the saturation region of MOSFET, MOSFET works like a high resistance current source at output terminal. This phenomenon requires that the amplifier following the MOSFET has a low equivalent input current noise.

In our work, SA noise floor is the noise measurement result for only SA and the cable between output probe and SA. TIA noise floor is the noise measurement result when DUT turned off. NMOS device (DUT) amplified noise is measured when both DUT and TIA are biased.

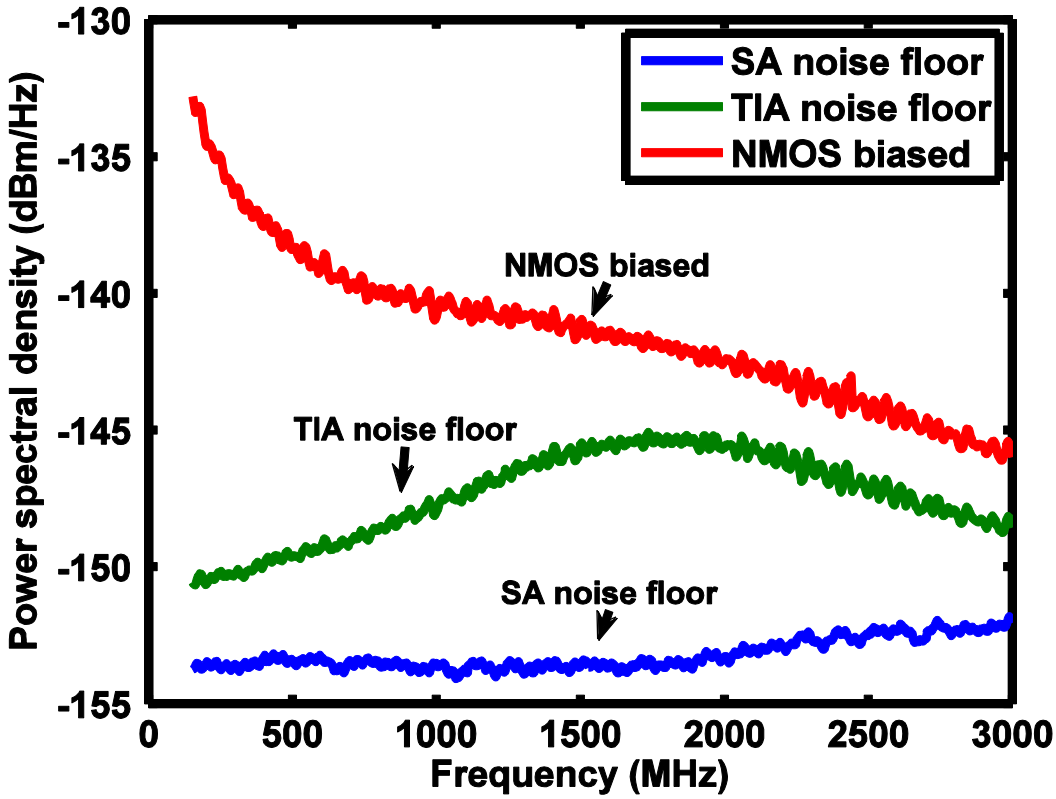

Figure 2.18 A typical output PSD of NMOS + TIA system, TIA noise floor and SA noise floor versus frequency

As shown in Figure 2.18, the TIA satisfies all the design requirements described above. Comparing the NMOS biased and SA noise floor curves, we see the amplified noise of the device is greater than SA noise floor. Comparing the NMOS biased and TIA noise floor curves, we know that the TIA noise floor is less than the amplified device noise.

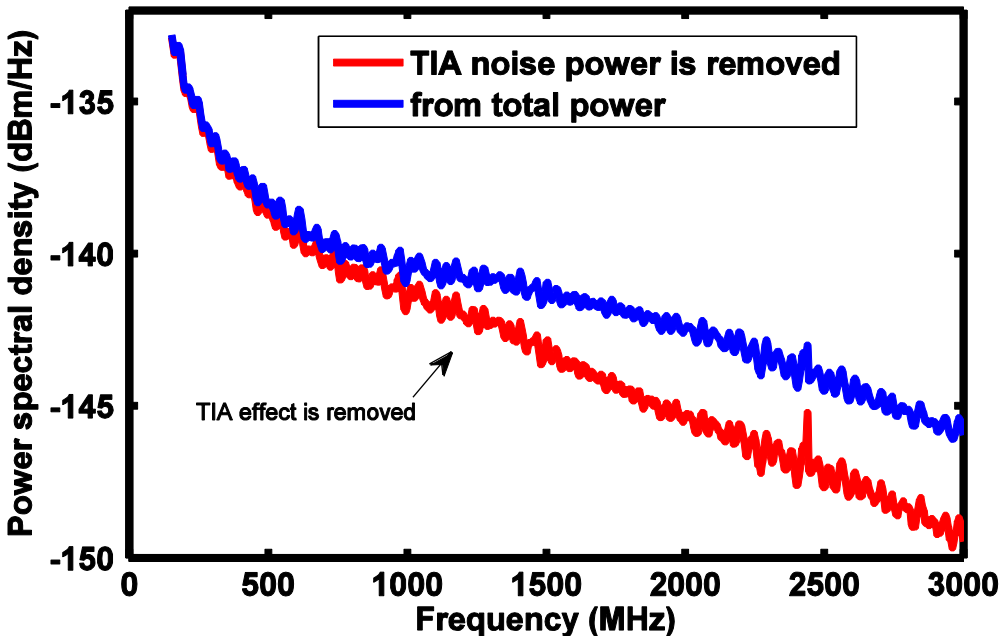

Figure 2.19 Power spectral density of output power with/without TIA noise effect.

Comparing PSD of output power with or without TIA noise effect in Figure 2.19, we can see the TIA noise has significant effect at higher frequencies. So the TIA noise power should be removed from the total output power to get accurate drain current noise power. Before measuring the drain noise characteristics, the I-V curve of this TIA shown in Figure 2.20 is measured when the DUT is turned off.

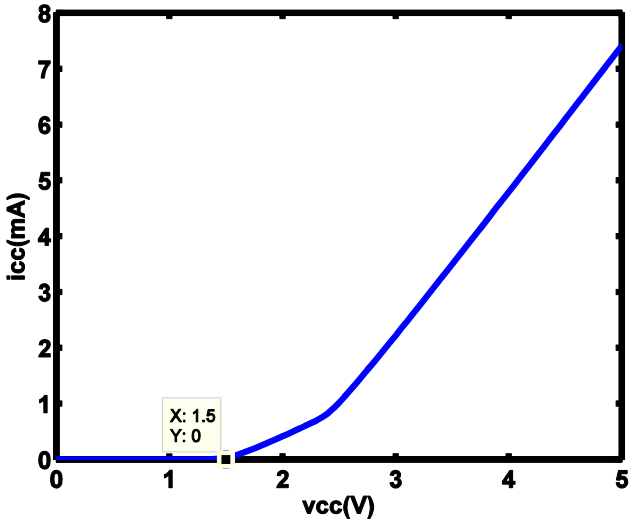

Figure 2.20 Measured I-V curve of TIA with DUT biased off

Figure 2.20 shows this TIA turns on at V_{CC} = 1.5V and the Icc-Vcc behaves like a resistor at V_{CC} > 2.5V. A Vcc = 4.25 V is used in this work.

From equation (2.8) Z_{total} can be calculated by

$$Z_{total} = \frac{V_{out}}{V_{in}} \frac{1}{g_m}. \tag{2.14}$$

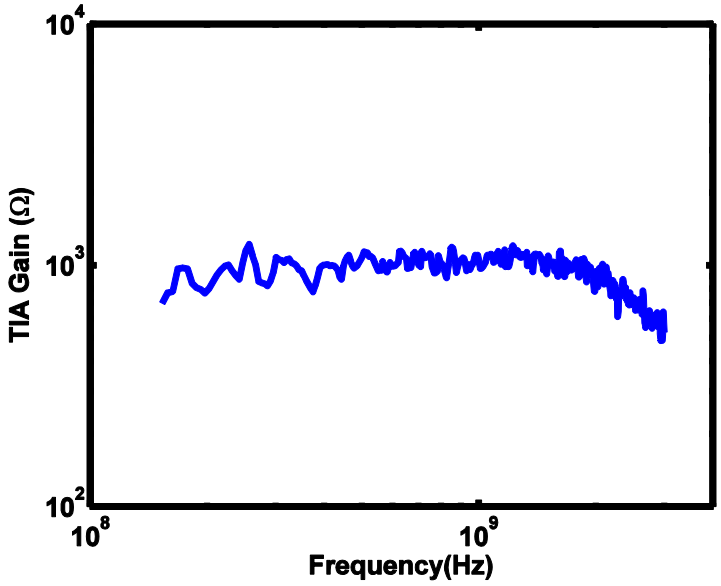

Figure 2.21 A typical Z_{total} vs frequency.

Figure 2.21 shows the total gain versus frequency at V_{GS} = 0.51V and V_{DS} = 1V. Gain is constant below 2 GHz, drops to half values at 3 GHz, indicating a 3 dB bandwidth of 2.6 GHz. The noiseness in the lower frequency range normally comes from S-parameters. From total gain and measured TIA and buffer noise voltage $V_{o,tia}$, PSD of the TIA and buffer current noise $i_{TIA,B}$, S_{tia}, is obtained as

$$S_{tia} = \overline{i_{TIA,B}^2} = \frac{V_{o,tia}^2}{Z_{total}^2} \tag{2.15}$$

For VGS=0.55V, VDS=1V, S_{tia} is shown in Figure 2.22. S_{tia} is 6×10^{-23} A^2/Hz for frequency lower than 1 GHz, and it increases to 2.5×10^{-22} A^2/Hz from 1 GHz to 3 GHz. Comparing Figure 2.22 and Figure 2.16, we can see that S_{id} is smaller than S_{tia} when frequency is higher than 2 GHz, which indicates the noise from TIA is not negligible at high frequencies in drain current noise measurement.

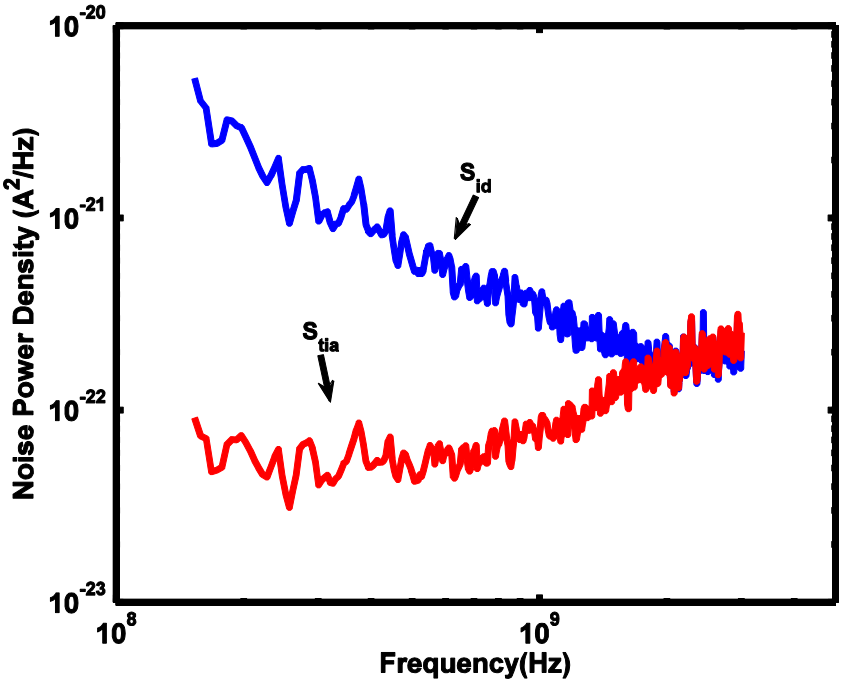

Figure 2.22 A typical S_{tia} and S_{id} vs frequency.

Chapter 3

Noise Measurement and Data Analysis

After boosting the noise though TIA, the output power of the noise can be measured by spectrum analyzer (SA). Drain current noise is extracted from the measured and calculated NMOS + TIA system parameters data. Noise factor γ is calculated from measured Sid in the white noise range of the measured drain current noise spectrum.

3.1 Noise Measurement

Figure 3.1a and Figure 3.1b show the noise measurement equipment setup used in our lab. On the left is a HP 4155 semiconductor analyzer, which we use to characterize DC I-V, transconductance g_m, output resistance R_{out}, as well as to supply power to both DUT terminals and V_{CC} of TIA. The metal box in front of the probe station adapts BNC connectors of the cables from the DC biasing probes to the special SMU cable connectors. The output power of amplified drain current noise is measured using a PSA series spectral analyzer, shown on the right. At the TIA output, a bias tee is used between the TIA output and SA to block DC and pass AC. As described in Appendix A and Appendix B, the measurement system needs to change during DC measurement and S-parameters measurement.

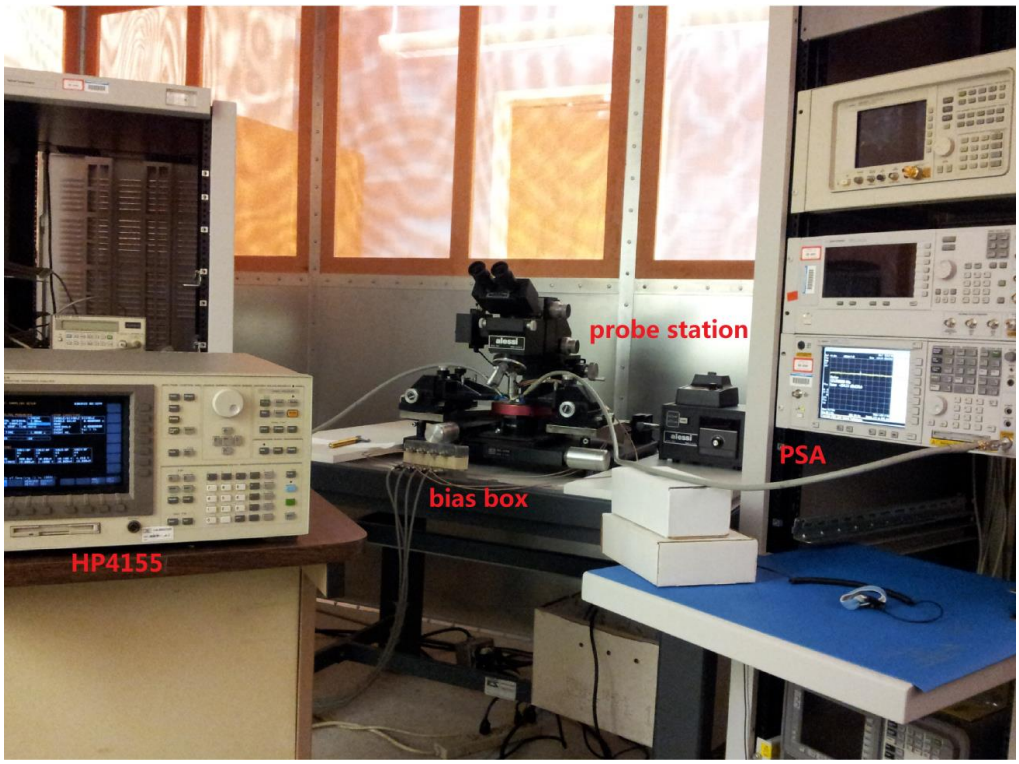

Figure 3.1a Drain current noise measurement system setup.

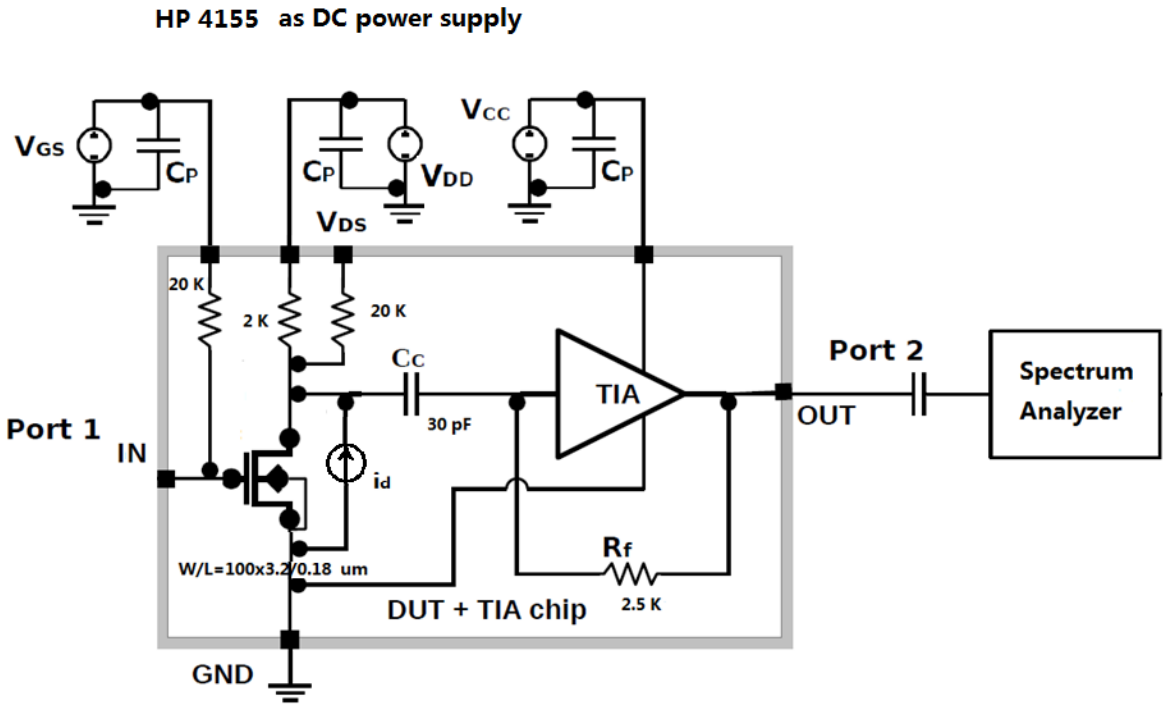

Figure 3.1b Drain current noise measurement system diagram.

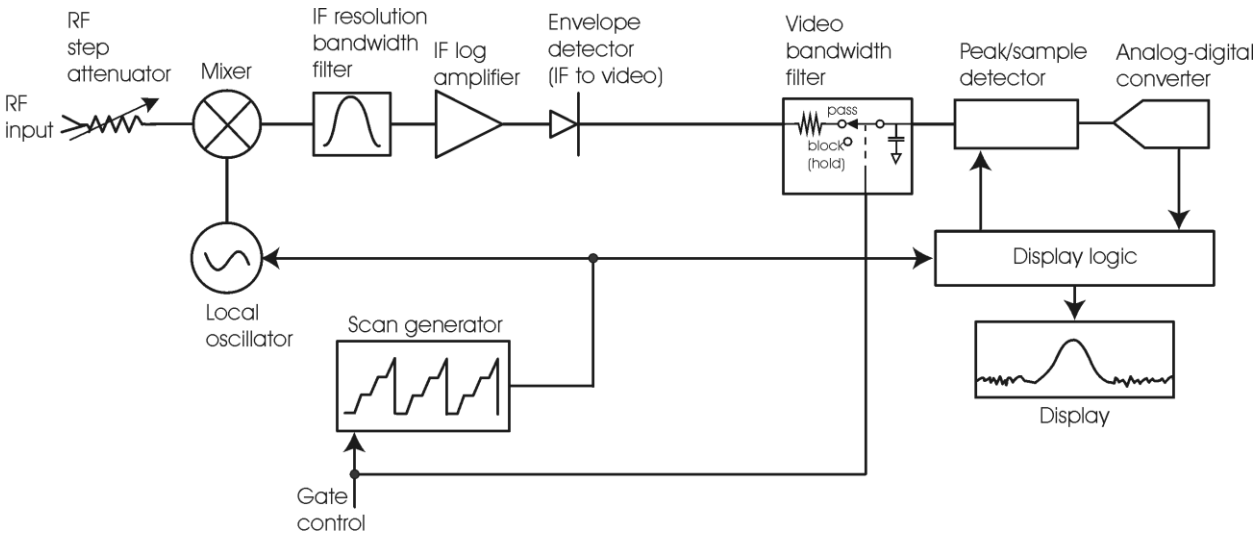

Figure 3.2 Block diagram of operation theory for spectrum analyzer [29].

Figure 3.2 shows block diagram of a spectrum analyzer. The input signal to be analyzed and the synchronous local oscillator signal which is generated by gate controlled scan generator are combined at the mixer. After passing the IF resolution bandwidth (RBW) filter, the filtered IF output goes through a log amplifier and is detected by an envelop detector. Then the signal passes through a video bandwidth filter which is used to decrease peal-to-peak variations of noise to a peak/sample detector. Then the signal passes through a video bandwidth filter which is used to decreasing the peal-to-peak variations of noise to a peak/sample detector. The display logic modify the horizontal (frequency) axes. The peak/sample detector detects and passes the signal to analog-digital converter to transfer the analog signal into digital signal to allow the spectrum analyzer to display the signal.

Considering the operation theory of SA [27-30], the following SA setting are used: Frequency range: 100 MHz ~ 3 GHz, Resolution Bandwidth (RBW on instrument panel) = 300 KHz, Video Bandwidth (VBW on instrument panel) = 3 KHz, Video Bandwidth/Resolution

Bandwidth = 0.01, Reference level = -60 dBm and Attenuation = 0dB. The default value of RBW is 3 MHz on SA we used. After changing it to 300 KHz, we compare these two measured results by overlay them in one figure and the figure shows taht these two curve are totally coincident. It demonstrates that both 3 MHz and 300 KHz work well for RBW setting in our work. The ratio of VBW/RBW is usually set to 0.1 or 0.01, which is small enough for accurate measurement result as described in [28].

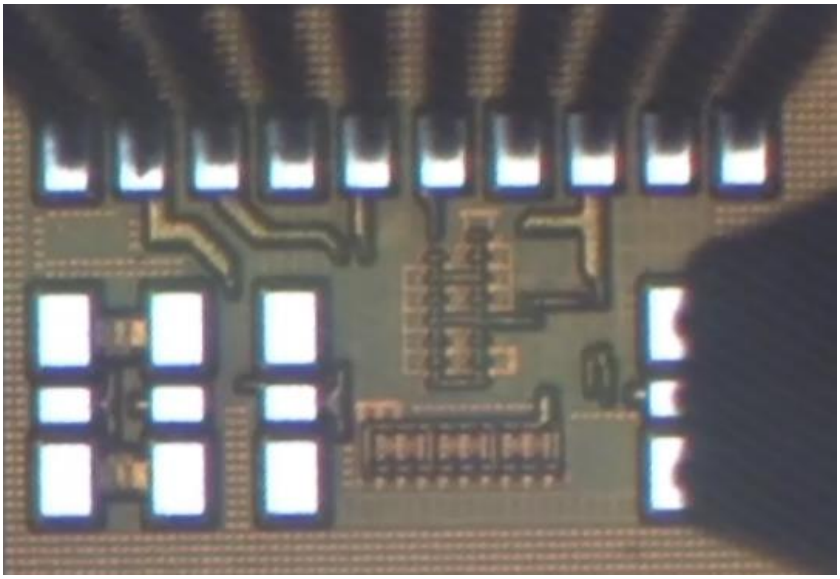

Figure 3.3 Die photo with right AC probe and DC probes on pads.

Figure 3.3 shows a photo of the die and probe configuration during noise power measurement. A Cascade Infinity GSG probe contacts the GSG pads at the TIA output, and connects the output to SA input. The Eye-Pass DC probe, shown in Figure 3.4, is used to contact all the DC pads and supply power to TIA through the V_{CC} pad, to DUT gate through the V_{GS} pad, and to DUT drain through the V_{DD} pad. The capacitance Cp in Figure 3.1b is 10 nF as shown in Figure 3.4 to keep AC ground from these pads. The ground tip showed in Figure 3.4 is contacted to our designed ground pad one to one.

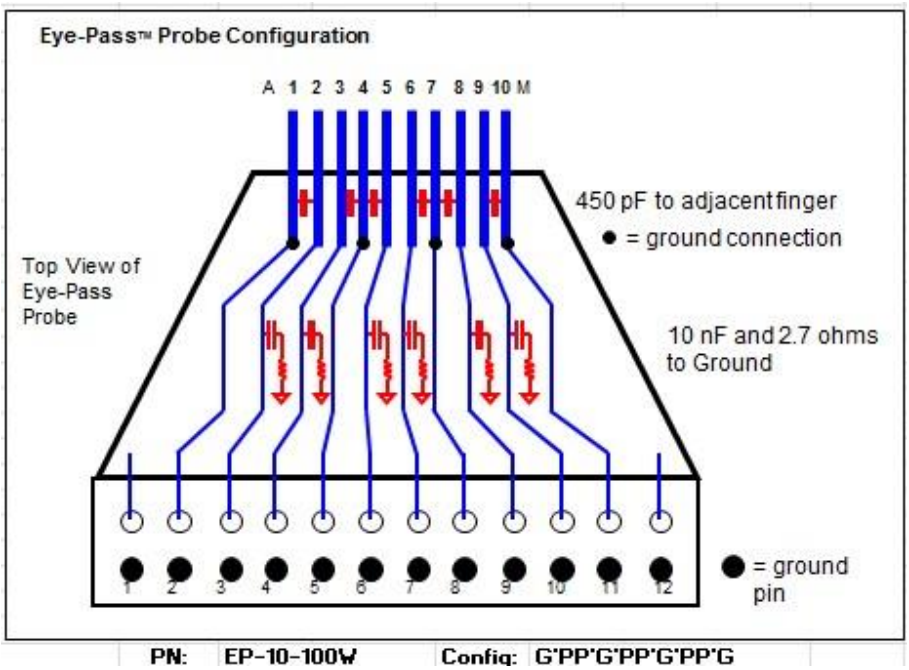

Figure 3.4 Configuration of Eye-Pass DC probes (Cascade Microtech Company).

3.2 Experimental Results Analysis

The drain current spectral density and noise factor from all the bias set we chose are shown in Figure 3.5. Figure 3.6 and Figure 3.8 demonstrate the voltage dependence of γ and S_{id} respectively.

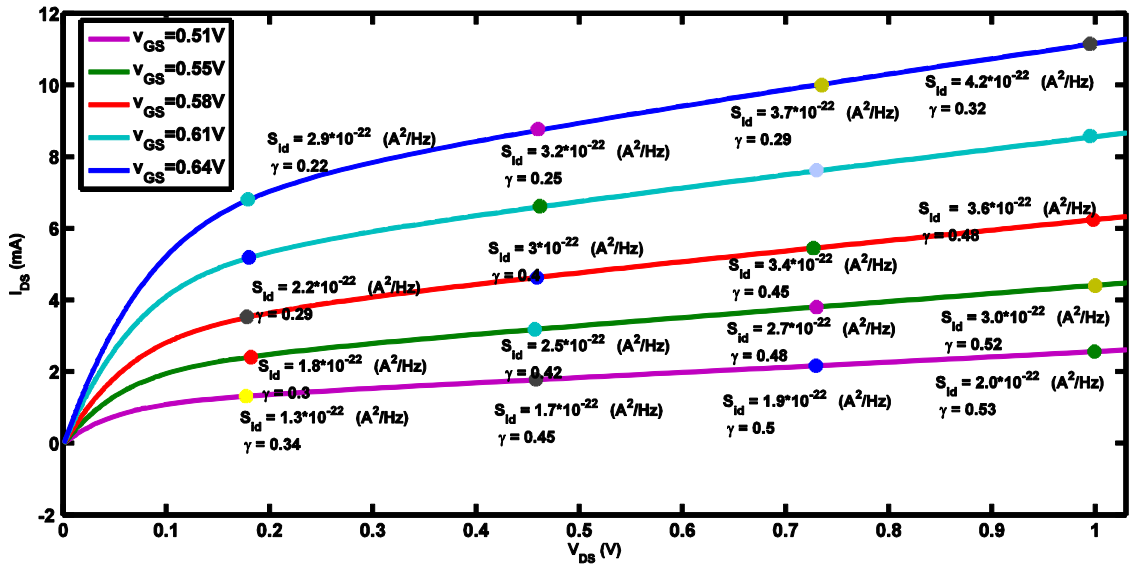

Figure 3.5 Drain current noise spectral density S_{id} and noise factor γ versus $V_{DS.}$

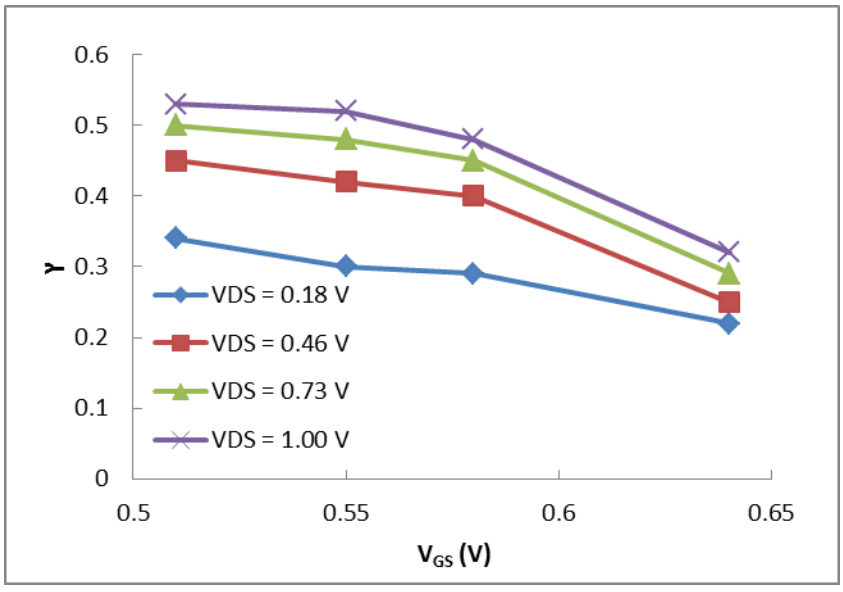

Figure 3.6 Noise factor γ with different biases.

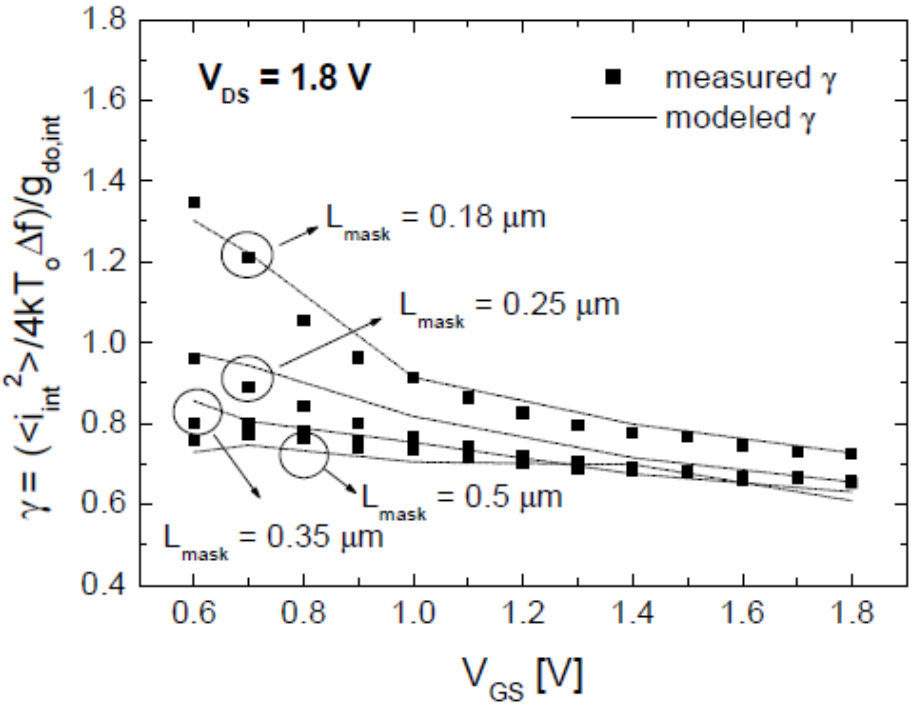

Figure 3.7 Extracted noise factor γ vs V_{GS} in 0.18 µm technology [14].

Same as plots in Figure 3.7, we can see that γ in Figure 3.6 decreases with increasing V_{GS} at fixed $V_{DS,}$ and it increases with increasing V_{DS} at fixed V_{GS}.

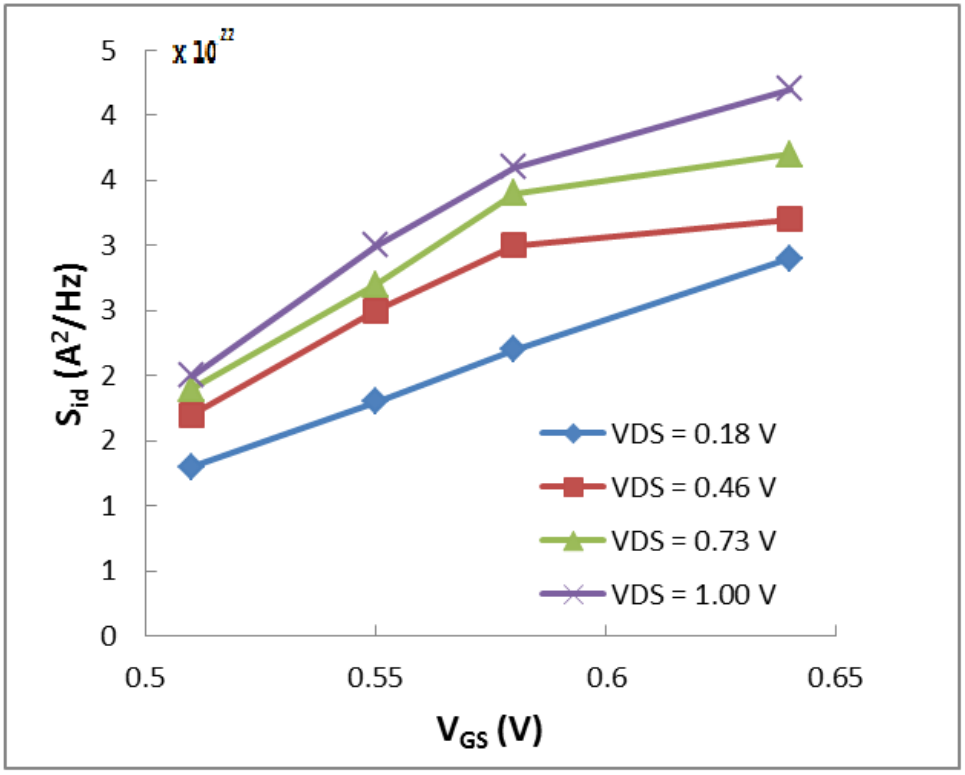

Figure 3.8 Drain current noise PSD S_{id} vs $V_{gs.}$

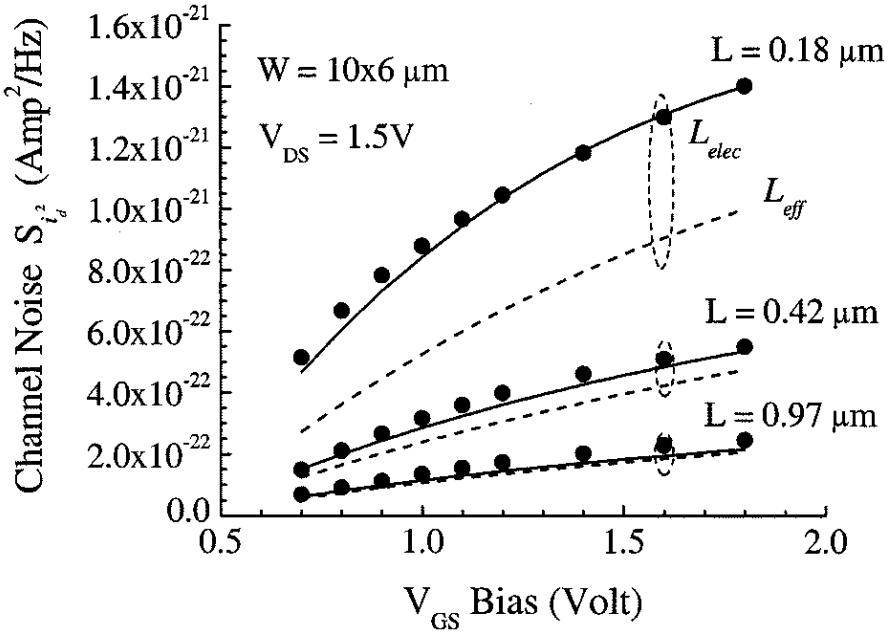

Figure 3.9 Drain current noise PSD S_{id} vs V_{gs} in 0.18 µm technology [6].

Same as plots in Figure 3.9, S_{id} in Figure 3.8 increases with raising V_{GS} at fixed V_{DS} and it also increases with increasing V_{DS} at fixed $V_{GS.}$ Figure 3.10 shows that S_{id} increases with I_{DS} at fixed $V_{DS.}$ This phenomenon is also shown in Figure 3.11 [31].

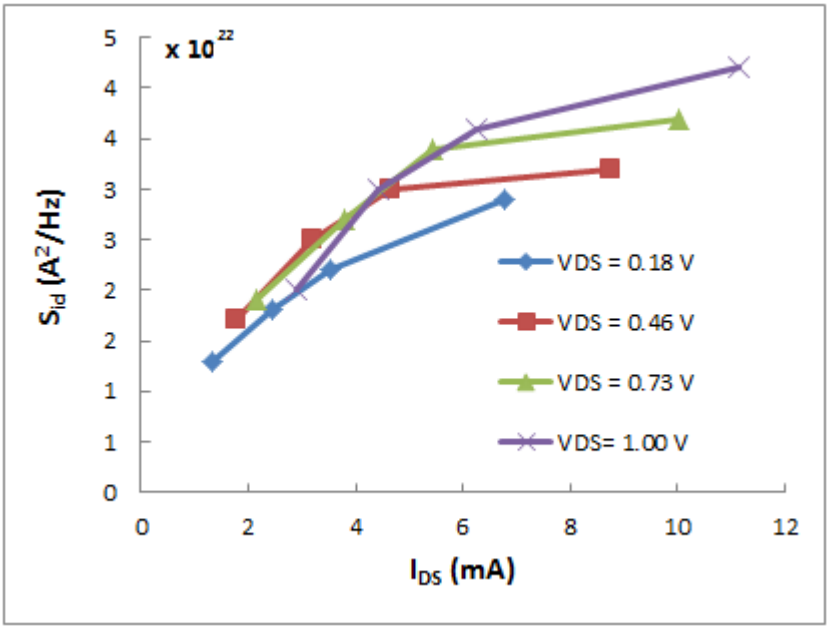

Figure 3.10 Drain current noise PSD S_{id} vs drain current $I_{DS.}$

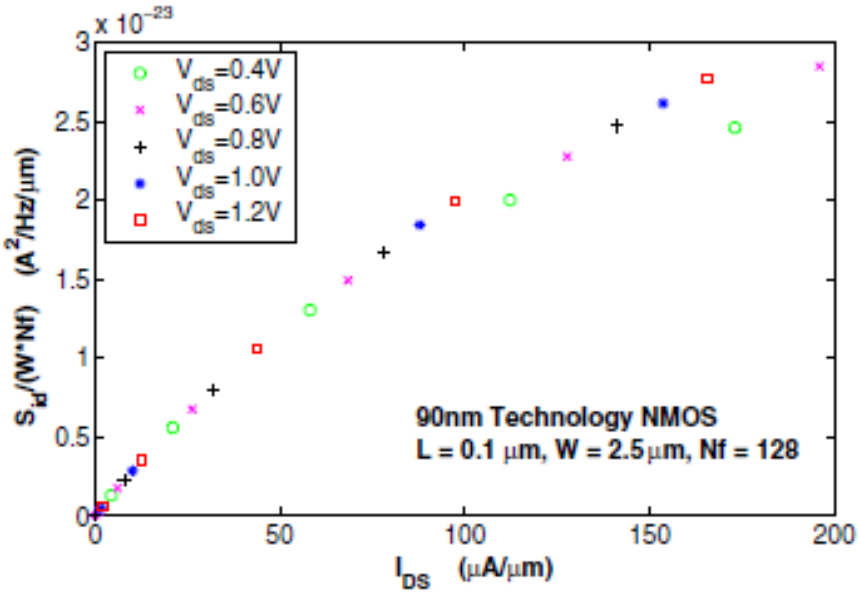

Figure 3.11 Drain current noise PSD S_{id} vs drain current I_{DS} in 90 nm technology [31].

As mentioned in Chapter 2, TIA is not noiseless and its noise power should be removed from the total measured noise power. Figure 2.15 shows us the noise floor of this SiGe TIA in green curve is only 3 or 4 dBm/Hz lower than the amplified noise power density in red curve when frequency is higher than 1.5 GHz. In other words, the noise of TIA is not negligible at higher frequency. To remove the TIA noise effect from measured drain current noise, we subtract TIA noise power from the total measured output power. And the result is shown in Figure 3.12.

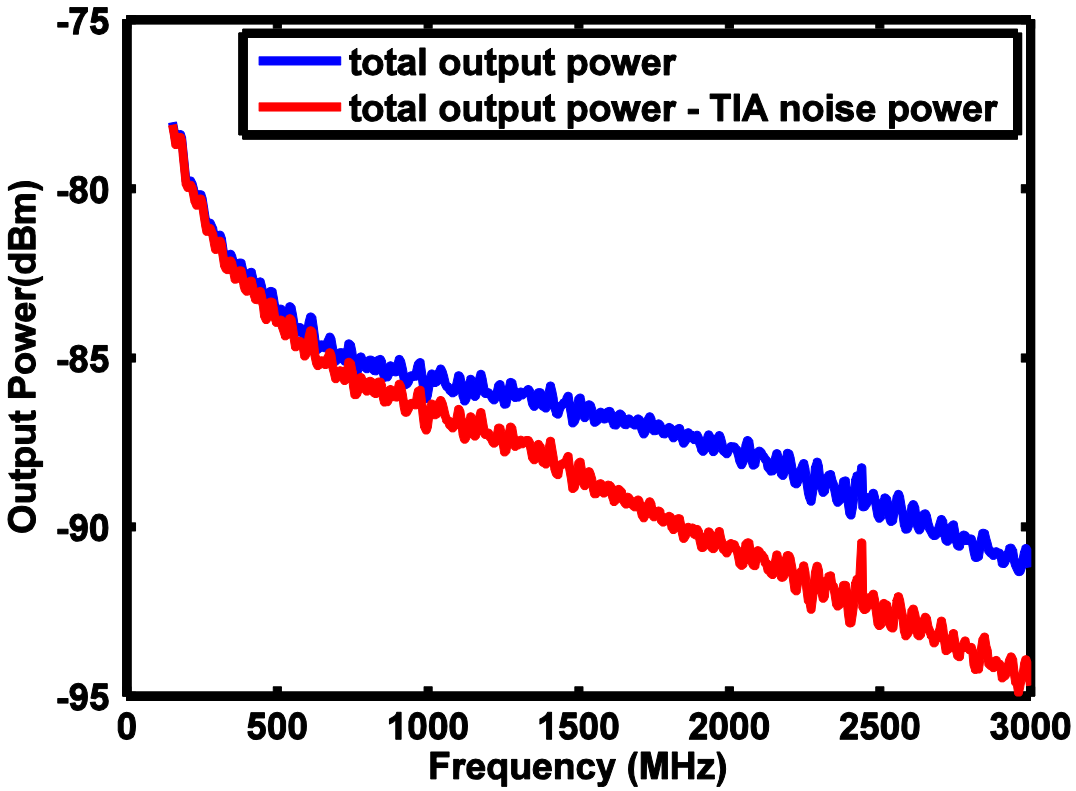

Figure 3.12 Comparison of output noise power

From Figure 3.12 we can see the measured output power without the effect of TIA which shown in red curve is lower than the total output power which contains the power of TIA noise. This phenomenon is obvious when frequency is higher than 1.5 GHz.

After subtracting the TIA noise power from the total measured power, the derived drain current noise PSD and noise factor are shown in Figure 3.13 and Figure 3.14.

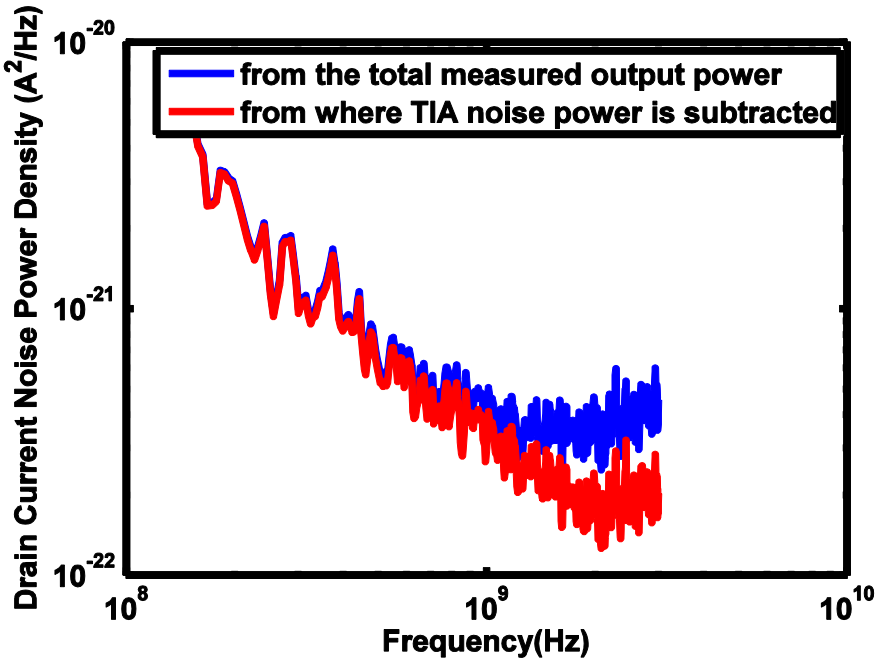

Figure 3.13 Comparison of S_{id}

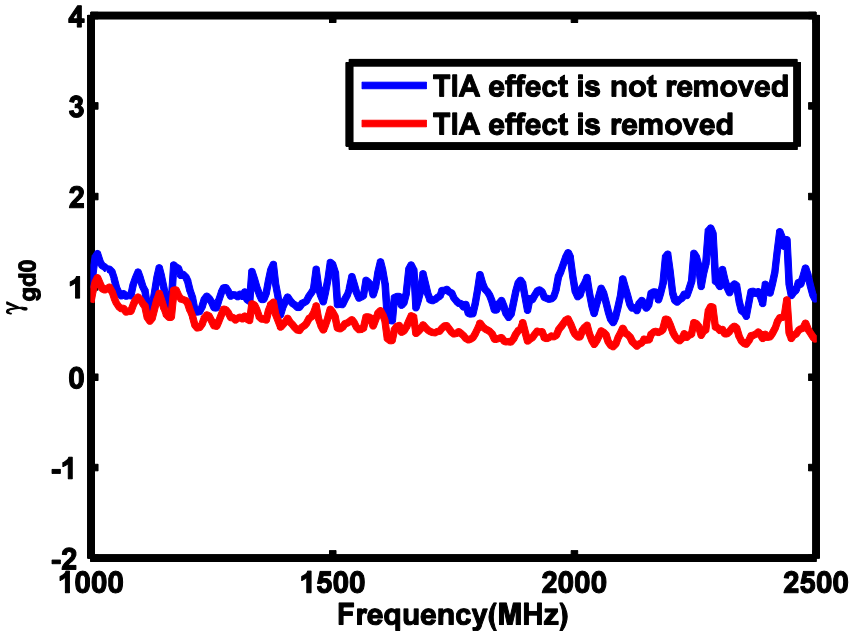

Figure 3.14 Comparing of γ

Actually, the TIA noise floor which shown in Figure 2.15 is not exactly the same as equivalent TIA noise when DUT is biased. Therefore, there is an approximation. A better way to remove the TIA noise effect from measured drain current noise is need to do as the future work. Moreover, the error bar of noise measurement on SA is approximately 1 dBm, which also affects the final experimental result.

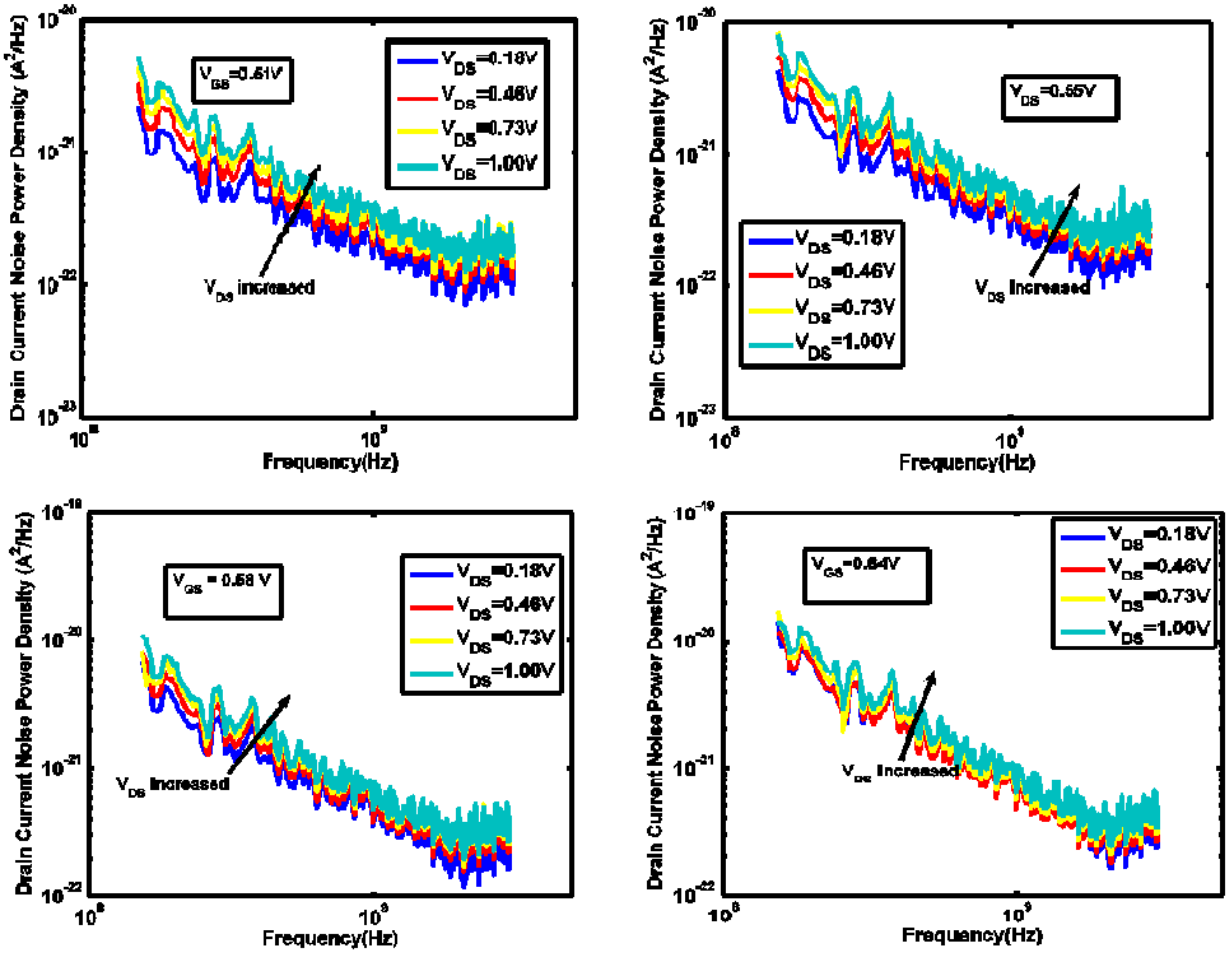

Figure 3.15 S_{id} vs frequency at fixed V_{GS}.

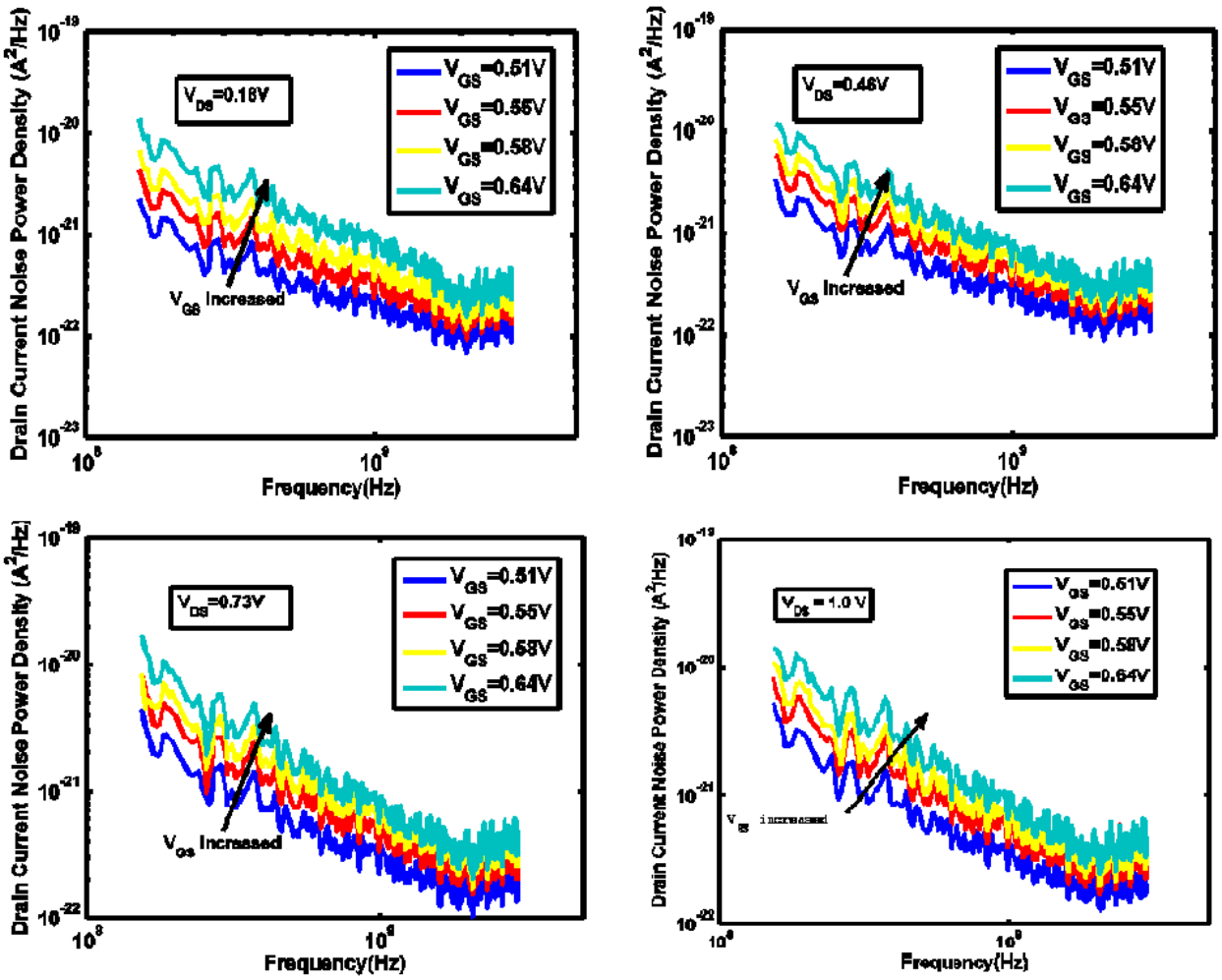

Figure 3.16 S_{id} vs frequency at fixed $V_{DS.}$

Figure 3.15 and Figure 3.16 show S_{id} versus frequency at fixed V_{GS} or fixed V_{DS}. For both 1/f noise component and thermal noise component, S_{id} increases with V_{DS} at fixed V_{GS} and S_{id} increases with V_{GS} at fixed $V_{DS.}$ The corner frequencies only change a little at these bias.

Appendix A

On-Wafer DC Measurements

A.1 Introduction

As mentioned in Chapter 1, to derive the drain current noise spectral density and noise factor, we need to measure transconductance (g_m) and drain-source conductance (g_{ds}). Hence, DC I-V measurements need to be done to acquire these parameters. Besides, we can see the mathematical relationship between the voltages and current at each terminal and know the operating limits of the transistor.

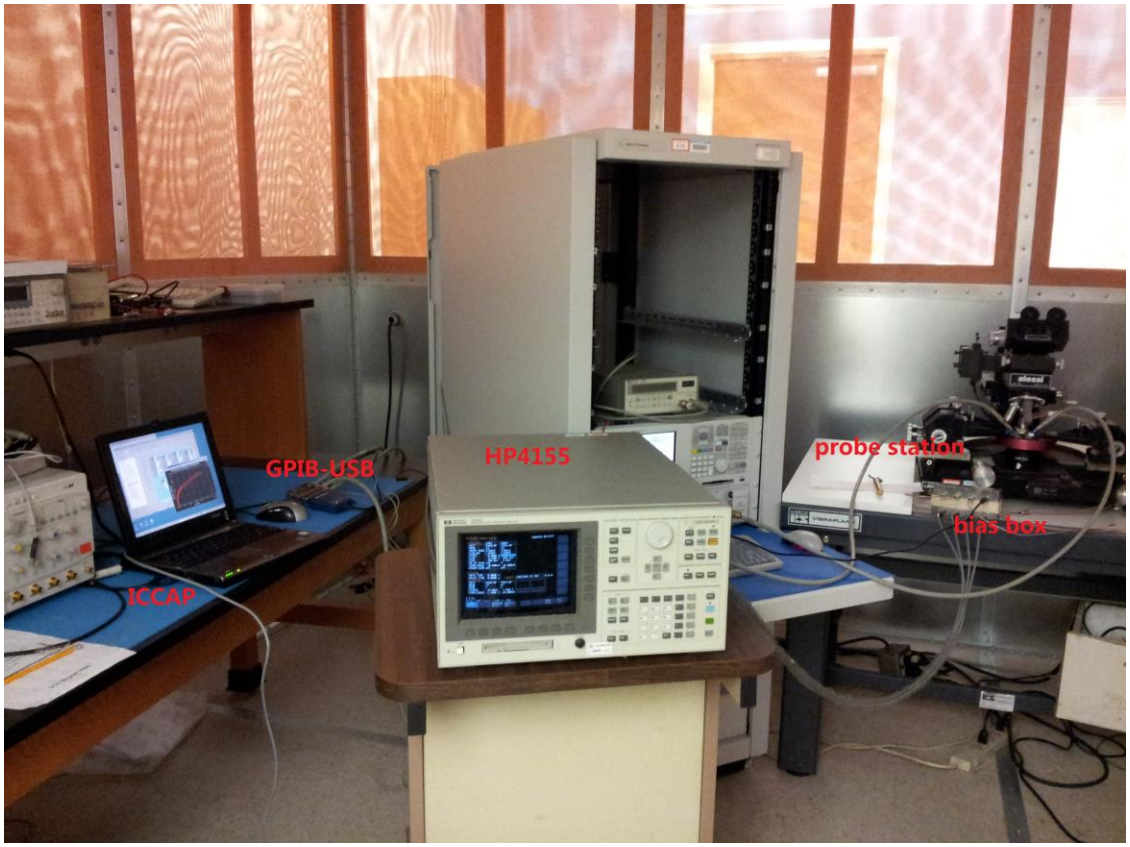

Figure A.1 DC measurement system setup

This measurement system was controlled by ICCAP software through GPIB-USB connected to probe station and HP4155 semiconductor parameter analyzer which was used to supply DC power through bias box.

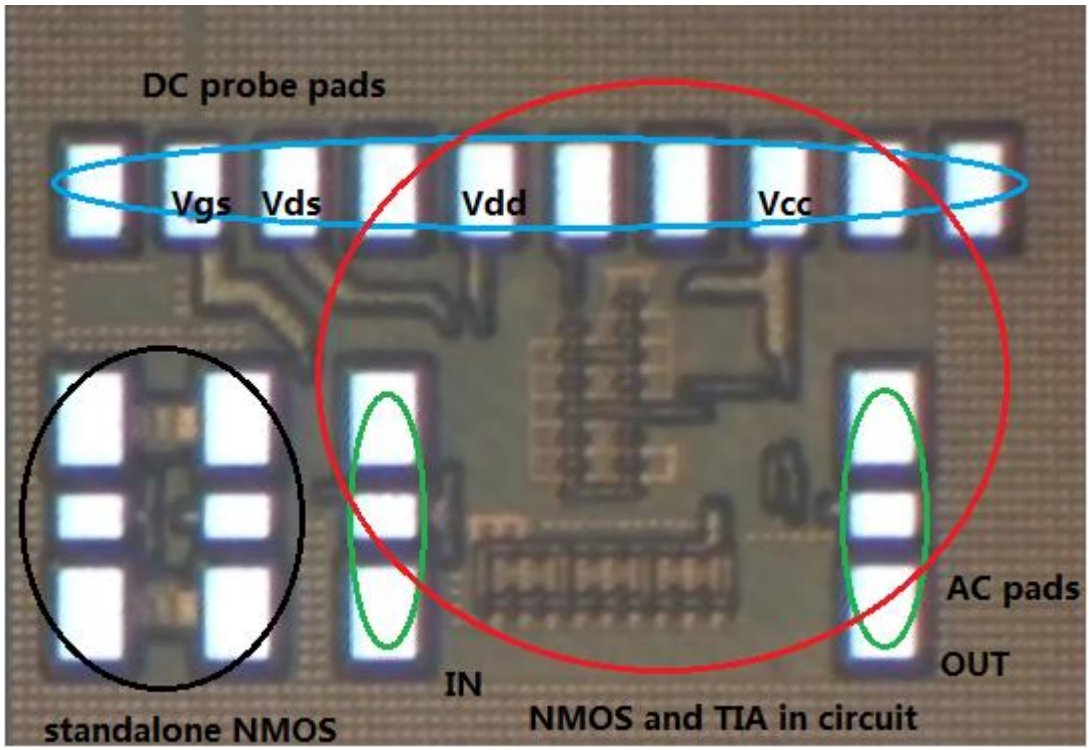

Figure A.2 Die photo with DUT and TIA on chip

One test die under microscope is shown in Figure A.2. The red circle contains the DUT and TIA in circuit. The blank circle contains the standalone NMOS which is designed to be the same structure as the NMOS in the circuit, and the size of the NMOS is the same as DUT in circuit. The reasons putting a standalone NMOS here are using the space on wafer efficiently and see some basic DC and RF characteristics.

A.2 DC Measurements for Standalone MOSFET

To know to basic characteristics of the transistor, DC measurements for standalone MOSFET was carried out at first. As shown in Figure A.3, two Ground-Signal-Ground AC probes was used to test the standalone NMOS.

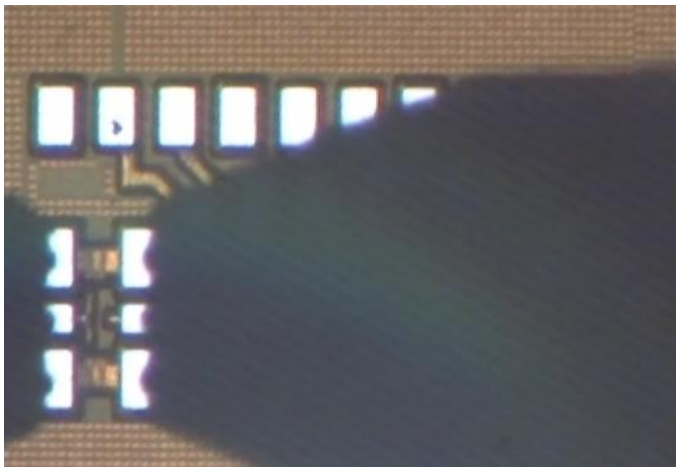

Figure A.3 Die photo with AC (G-S-G) probes on standalone NMOS pads

A.2.1 I_{DS}-V_{DS} and I_{DS}-V_{GS} Measurements

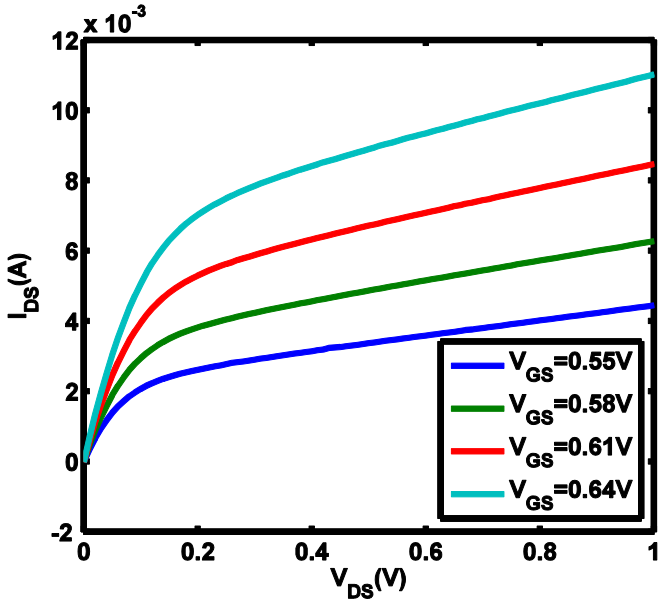

Figure A.4 Measured I_{DS}-V_{DS} for standalone NMOS

Considering the output characteristic of the transistor shown in Figure A.4, most of the drain biases we chosen, such as 0.46V, 0.73V and1V, are in the saturation regions. To compare the noise characteristics in saturation region which are interested in most cases, we also chose 0.18V in triode region as the drain bias.

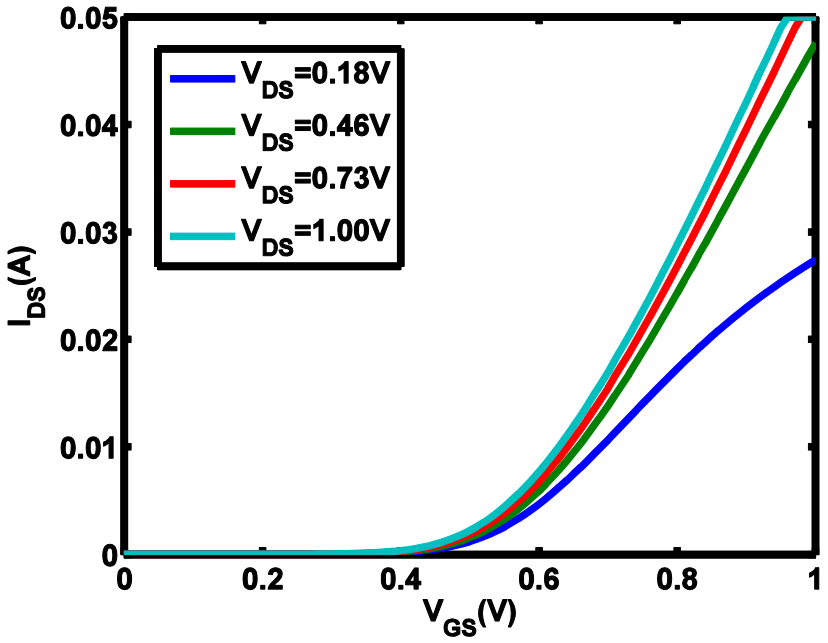

Figure A.5 Measured I_{DS}-V_{GS} for standalone NMOS

Considering the transfer characteristic of the transistor shown in Figure A.5, most of the gate biases we chosen, such as 0.55V, 0.58V, 0.61V and 0.64V, are in the moderate and strong inversion regions.

A.2.2 g_{ds} and g_m

In A.2.1, we got the measurement result for I_{DS}-V_{DS} and I_{DS}-V_{GS}. To acquire g_{ds} and g_m which are used for noise spectral density and noise factor extraction, equation (1.2) and (1.6) are used and the calculation results are shown in Figure A.6 and Figure A.7 separately.

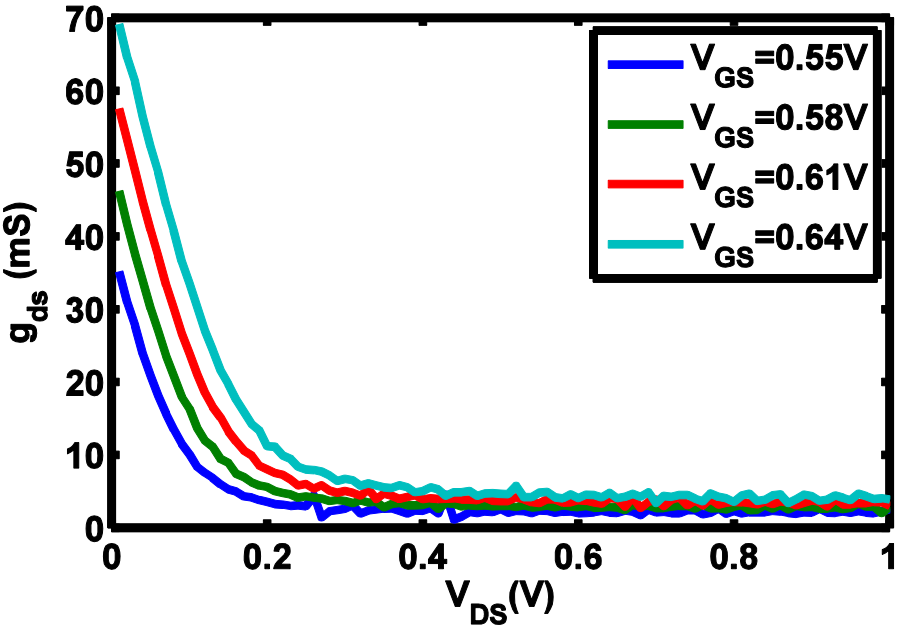

Figure A.6 Gate-source conductance g_{ds} vs V_{DS}

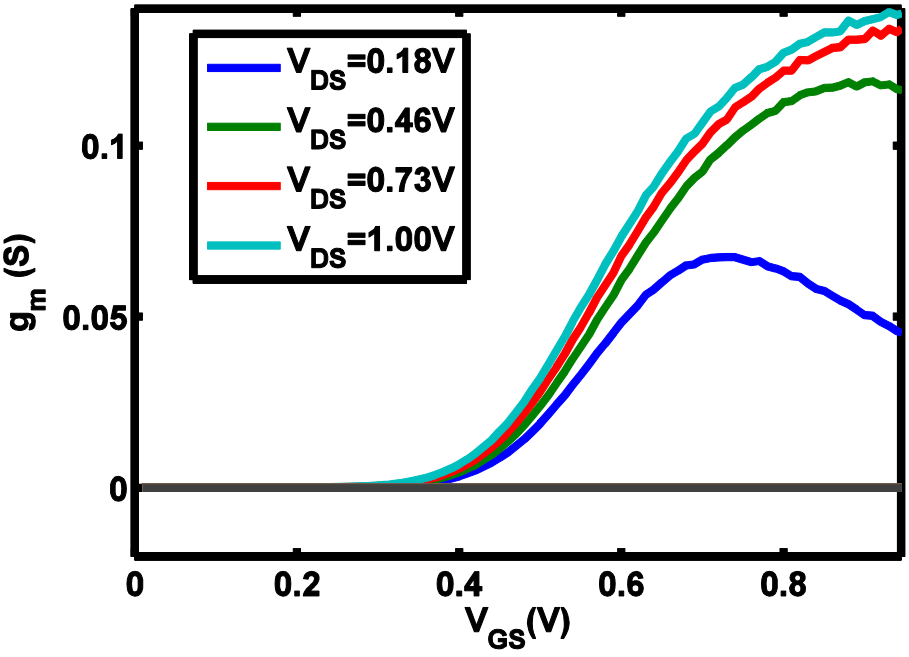

Figure A.7 Transconductance g_m vs V_{GS}

Also, we can check the output resistance of the transistor R_o from g_{ds}, which is shown in Figure A.8. The resistances are several hundreds of Ohms for these bias sets, which require the equivalent of input impedance of TIA part be less to allow drain current noise current flow into TIA.

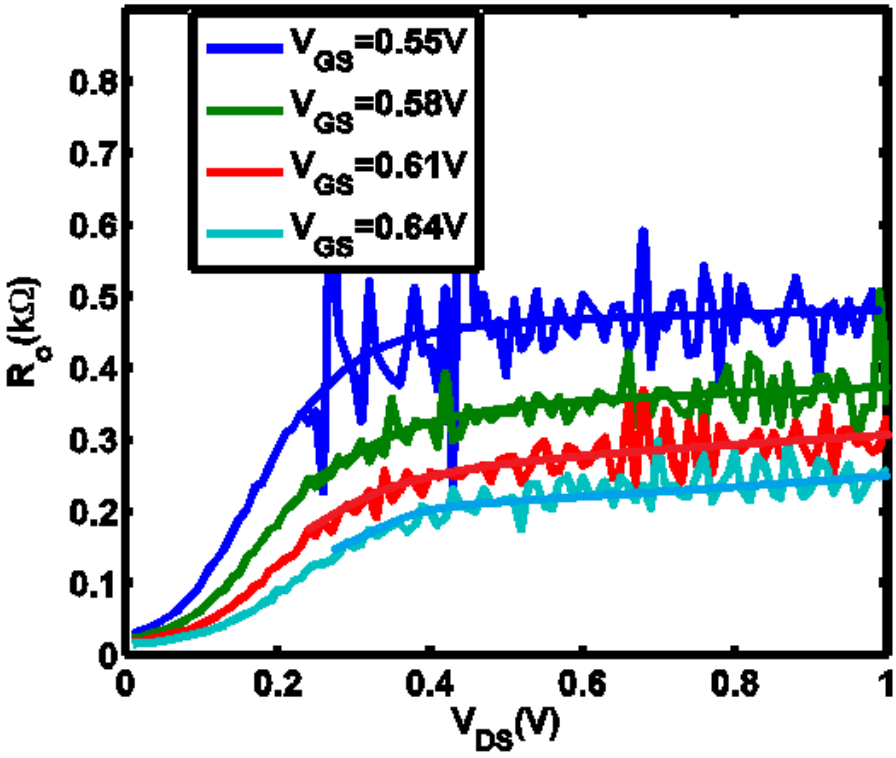

Figure A.8 Output resistance of the NMOS vs V_{DS}

A.3 DC measurements for Integrated DUT in Circuit

A.3.1 Measurement Equivalent Circuit

DC measurements for integrated MOSFET with TIA in circuit are more complex than DC measurements for standalone MOSFET since I_{DS}-V_{DS} and I_{DS}-V_{GS} measurements cannot be measured directly.

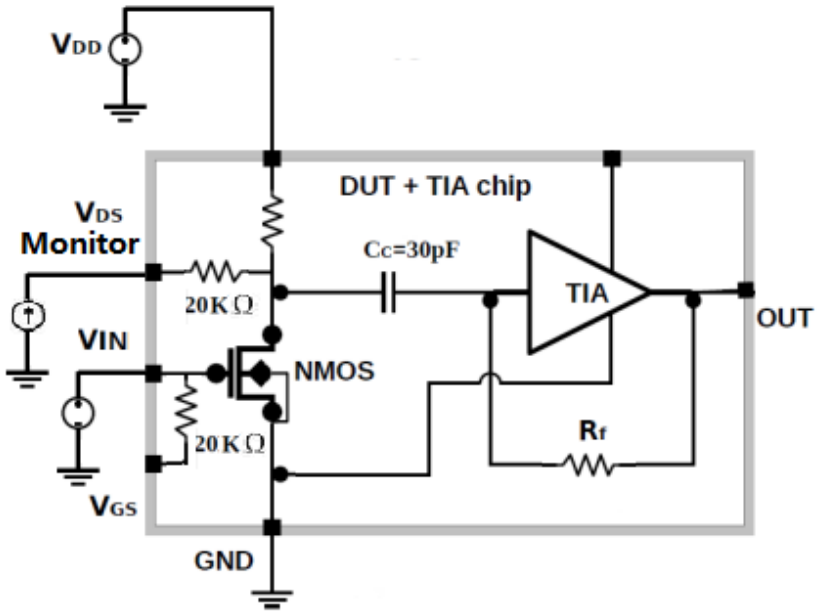

Figure A.9 DUT in circuit DC measurement circuit

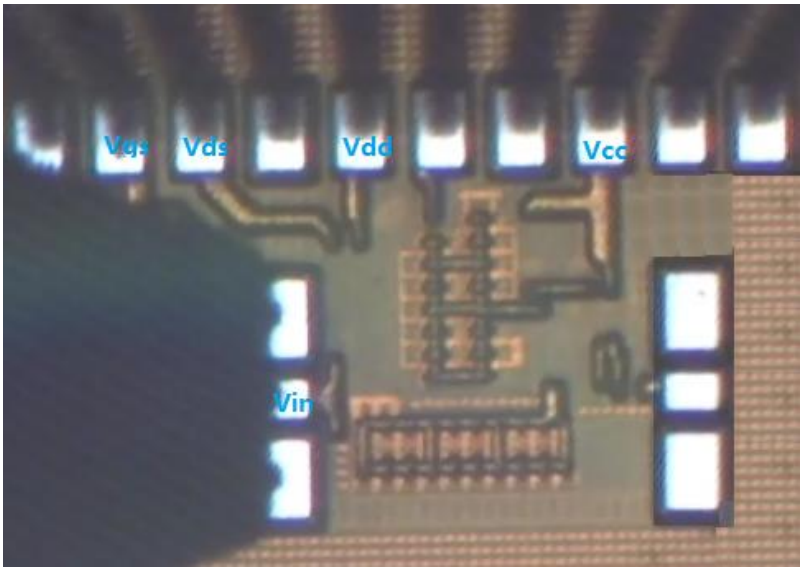

Figure A.10 Die photo with one AC probe and DC probes on pads for DC measurement

Figure A.9 shows the equivalent circuit for DUT DC measurement. V_{DD} and IN provide DC voltage for drain and gate separately. V_{DS} probe is used to monitor drain voltage by adding a tiny current source i_{DS} at V_{DS} pad, such as 10 nA. With this small current, the voltage drop can be ignored so that the tested voltage shown on V_{DS} is very close to drain voltage. Also, because there is a 2 KΩ resistor between V_{DD} pad and drain terminal, V_{DD} is not the voltage value we add to drain. In case of damaging the DUT, we have to estimate the V_{DD} using

$$V_{DD} = V_{GS} + I_{DS} \cdot R_{DD} \tag{A.1}$$

where V_{GS} is the operating voltage added to drain terminal, R_{DD} = 2 KΩ, measured current I_{DD} from V_{DD} pad is the drain current I_{DS} which should be similar value in standalone NMOS DC measurement result.

Compared with Figure A.9, Figure A.10 tells how the real probe pads matched the pins in the electrical circuit.

A.3.2 I_{DS}-V_{DS} measurement and g_m Extraction

Because I_{DS}-V_{DS} for the DUT cannot be measured directly, we need to do I_{DD}-V_{DD} and V_{DS}-V_{DD} measurement first, and then show the data using I_{DD}-V_{DS} axes. Attention is I_{DD} = I_{DS} as we talked before.

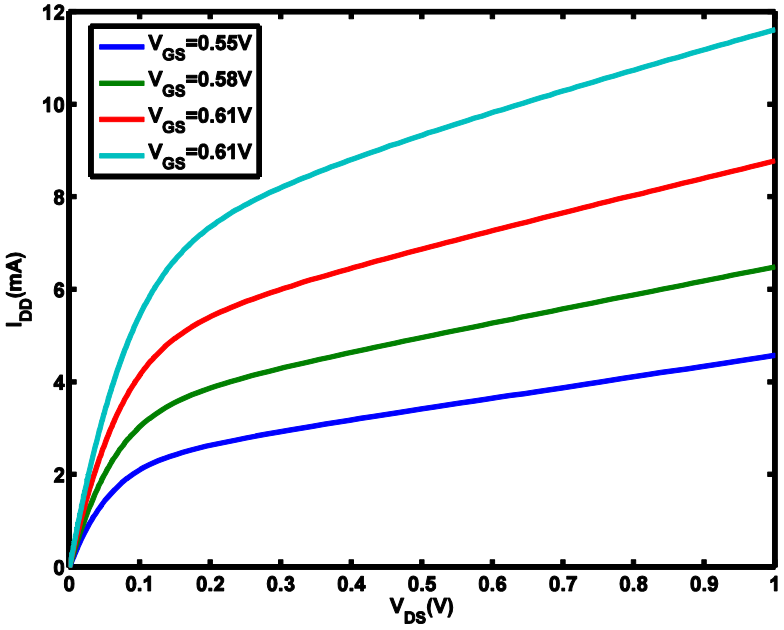

Figure A.11 Measured I_{DS}-V_{DS} for integrated DUT in circuit

Figure A.11 shows the output characteristic of the integrated DUT in circuit. To compare with the DC measurement result for standalone NMOS and integrated DUT in circuit, the I_{DS}-V_{DS} plots from Figure A.4 and Figure A.11 are overlay by Figure A.12.

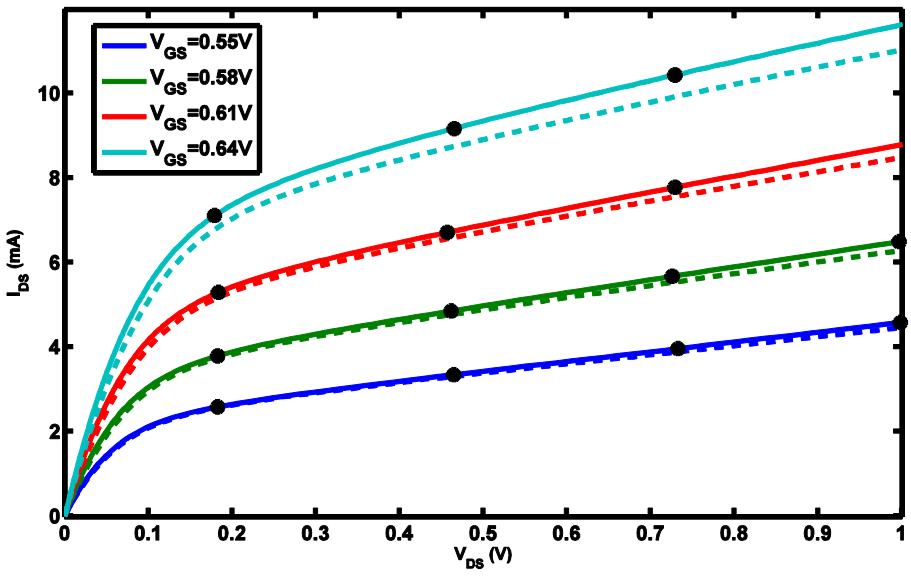

Figure A.12 Comparing I_{DS}-V_{DS} for both integrated DUT in circuit and standalone NMOS

For the manufacture reason, there are slight differences between the DC characteristics of standalone NMOS transistor and the integrated DUT in circuit. The drain current difference increases with raising gate voltage or drain voltage.

Similar to standalone NMOS DC measurement, using equation (1.2), g_{ds} could be derived from I_{DS}-V_{DS}. And g_{ds} of this DUT in circuit is shown in Figure A.13

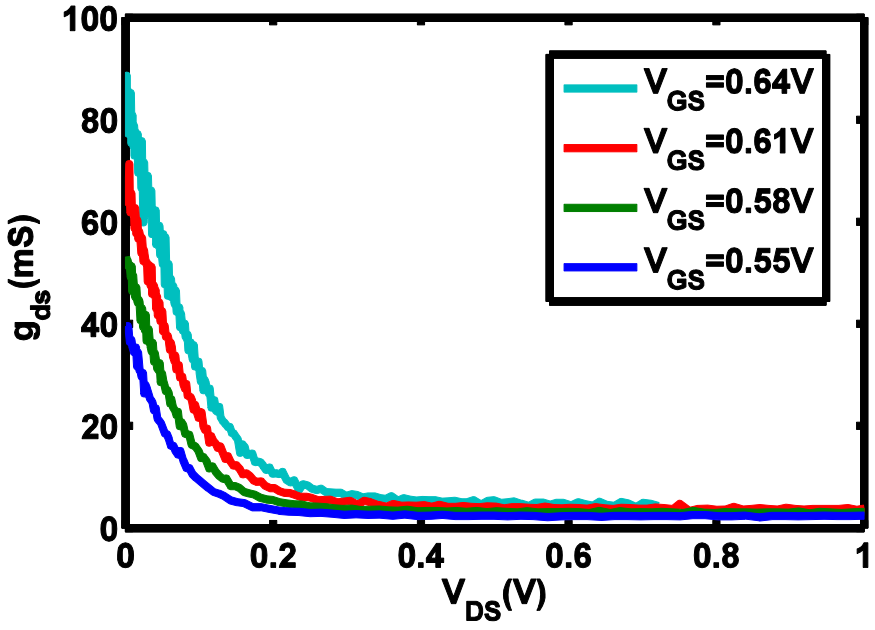

Figure A.13 g_{ds} of integrated DUT in circuit

To acquire g_m of integrated DUT, there are two methods. The first one is get g_m from g_m –V_{GS} measurement data for standalone NMOS. The second method shown in Figure A.14 is chosen very close to values of V_{GS}, using the difference of the nearby I_{DS} values as ∂I_{DS} and using the difference of the nearby V_{GS} as ∂V_{GS}. In this method, g_m is given by

$$g_m = \frac{I_{DS3} - I_{DS1}}{V_{GS3} - V_{GS1}} \tag{A.2}$$

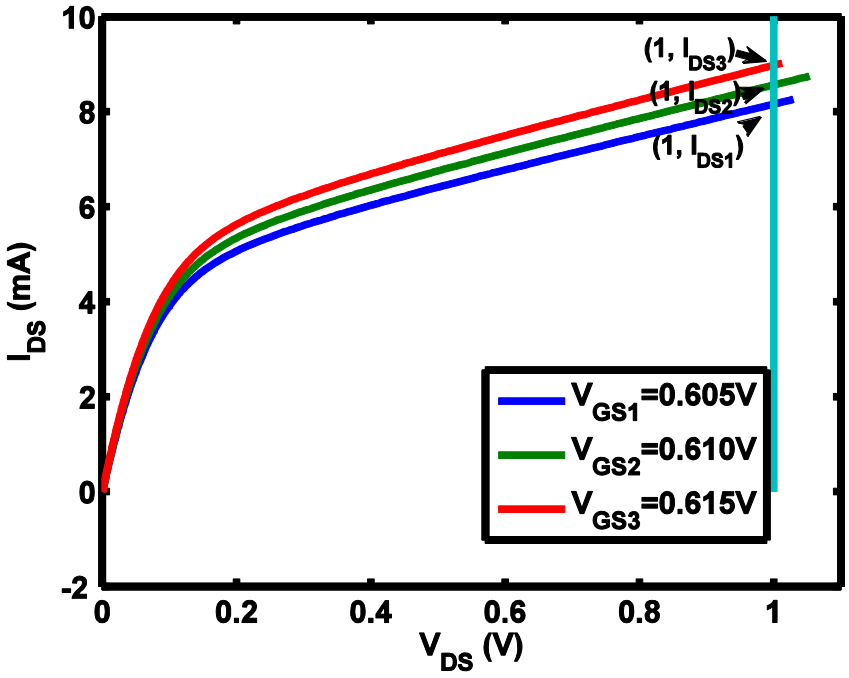

Figure A.14 I_{DS}-V_{DS} for nearby V_{GS}

Keep the Figure A.12 in mind; it is more appropriate to use the second method to derive g_m for higher biases set.

Appendix B

On-Wafer S-Parameters Measurement

B.1 Introduction

Scattering parameters (S-parameters) are power wave descriptors that used to define the input-output relations of a network, which is a two port network in our work, in terms of incident and reflected power waves.

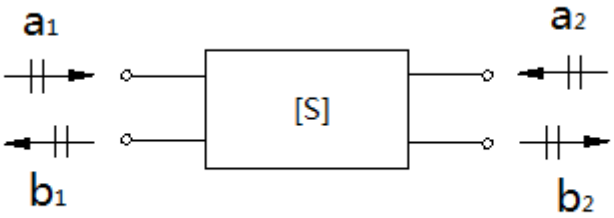

Figure B.1 Convention for defining S-parameters for two-port networks

Normalized incident power wave a_n and reflected power wave b_n are given by

$$a_n = \frac{1}{2\sqrt{Z_o}}(V_n + Z_o I_n) \tag{B.1a}$$

$$b_n = \frac{1}{2\sqrt{Z_o}}(V_n - Z_o I_n) \tag{B.1b}$$

where n is port number 1or 2, Z_o = 50 Ω is the characteristic impedance of the connecting lines on the input or output side of the network. V_n and I_n are input or output voltage and current. And based on Figure B.1, S-parameters are defined by

$$[b_n] = [S][a_n] \tag{B.2}$$

where S_{11} is the ratio of reflected to incident power wave at port 1; S_{22} is the ratio of reflected to incident power wave at port 2; S_{12} is the ratio of transmitted power wave at port 1 to incident power wave at power 2; S_{21} is the ratio of transmitted power wave at port 2 to incident power wave at power 1.

By matching on the input or output side, S-parameters can be determined. Figure B.2 shows the simple equivalent circuit of S_{11} and S_{21} measurement, where the line impedance Z_o is matched through a corresponding load impedance $Z_L = Z_o$ for $a_2 = 0$ at the output side.

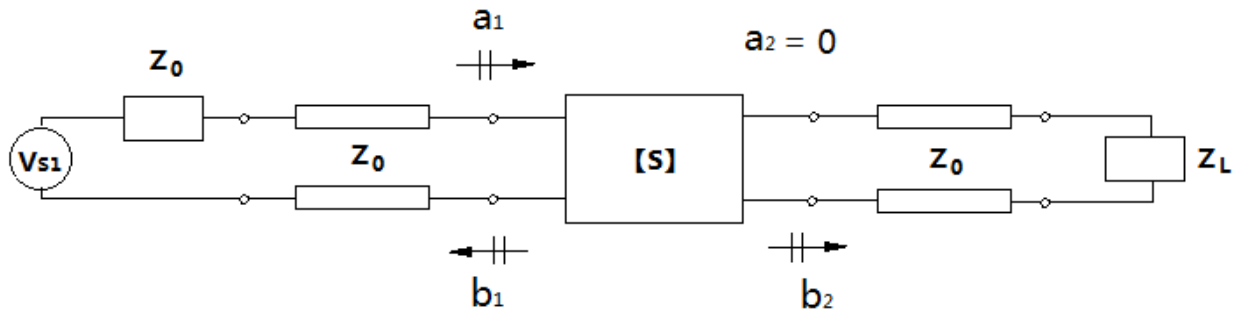

Figure B.2 Measurement of S_{11} and S_{21} by matching the line impedance Z_o at port 2 through a corresponding load impedance $Z_L = Z_o$

From Figure B.2, we can calculate S_{11} by the input reflection coefficient Γ_{in}:

$$S_{11} = \Gamma_{in} = \frac{Z_{in} - Z_o}{Z_{in} + Z_o} \tag{B.3}$$

On other hand, we can acquire Z_{in} from S_{11} by changing the form of equation B.3 to

$$Z_{in} = Z_o \frac{1 + S_{11}}{1 - S_{11}} \tag{B.4}$$

Besides, from equations B.1a, equation B.1b and Figure B.2, we can calculate S_{21} by

$$S_{21} = \frac{b_2}{a_1}\Big|_{a_2=0} = \frac{2V_2}{V_1 + Z_o I_1} \tag{B.5}$$

where $V_1 = V_{S1} - Z_o I_1$ and V_2 is the output voltage V_{out}. Hence, we can reform equation to

$$S_{21} = \frac{2V_{out}}{V_{s1}} \tag{B.6}$$

Since the voltage at port 2 is directly related the source voltage, available forward voltage gain can be get from S_{21} in dB unit by

$$G_{v,av} = 20\log|S_{21}| \tag{B.7}$$

Figure B.2 also represent that input voltage can be acquired by

$$V_{in} = V_s \frac{Z_{in}}{Z_o + Z_{in}} \tag{B.8}$$

Similar to measurement of S_{11} and S_{21} the measurement circuit (Figure B.3) of S_{22} and S_{12} can be considered as a reflection of Figure B.2 by matching the line impedance Z_o through a corresponding input impedance $Z_G = Z_o$

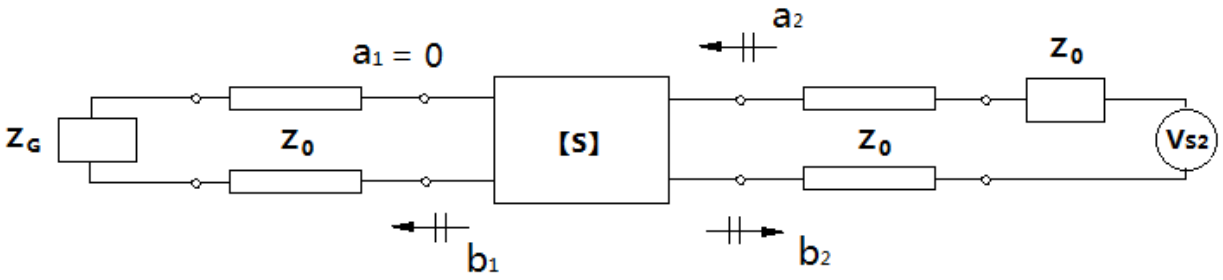

Figure B.3 Measurement of S_{22} and S_{12} by matching the line impedance Z_o at port 1 through a corresponding input impedance $Z_G = Z_o$

B.2 S-Parameters Measurement System

For S-parameters measurement system setup shown in Figure B.4, GPIB-USB was used to connect Agilent PNA E8464B network analyzer, HP4155 and a computer which offered ICCAP software. After setting up the measure/simulation and instrument option sections in ICCAP, HP4155 and PNA can be controlled automatically. HP4155 which works as DC power supply and PNA which works as AC power supply are connected to Probes through bias T. Power meter is connected to PNA by GPIB-USB to help with the power calibration portion during S-parameters measurement.

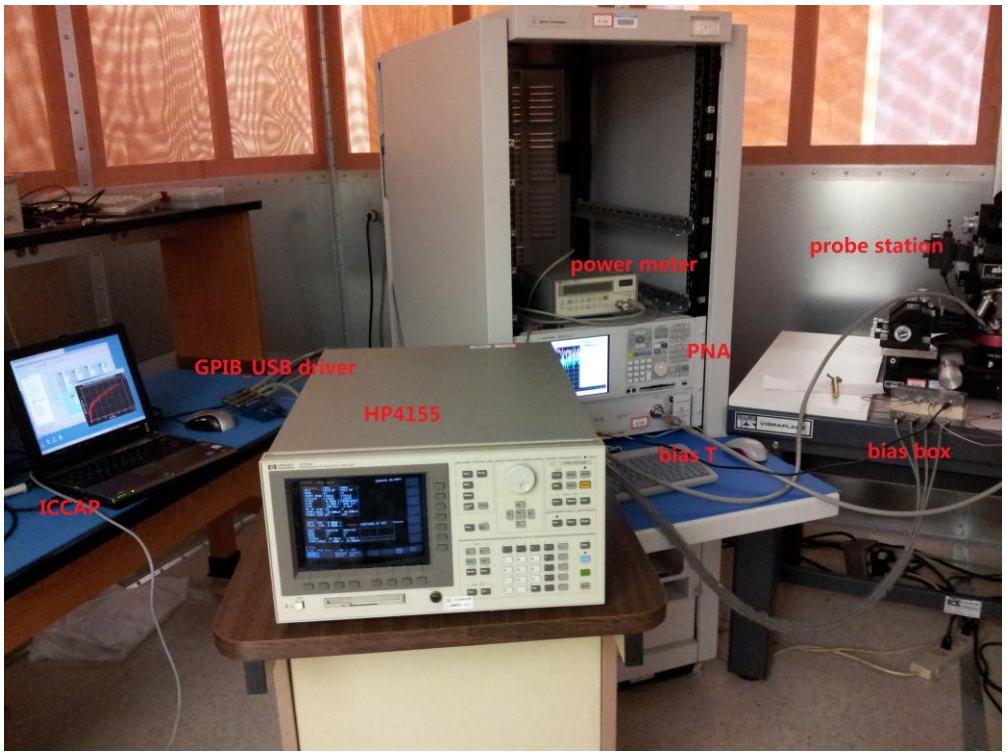

Figure B.4 S-parameters measurement system

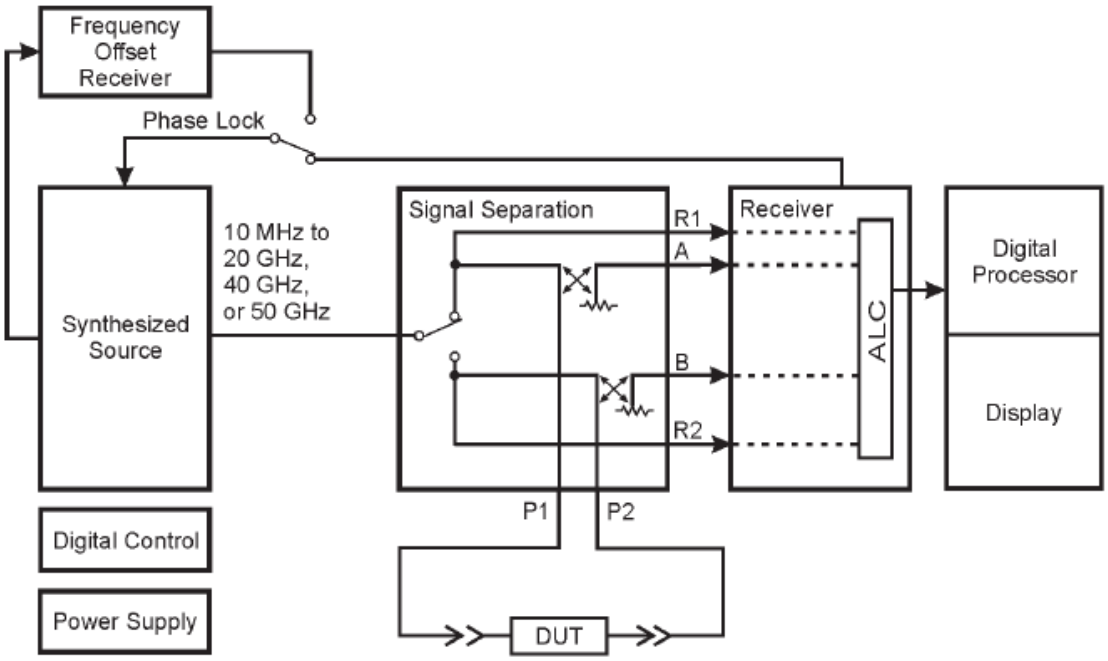

Figure B.5 Simplified block diagram of the PNA network analyzer system

As shown in Figure B.5, a phase-locked incident signal which includes both reference signal and test signal is generated from the synthesized source. Through the signal separation portion of the PNA, the reference signal was received by the receiver portion and the test signal is applied to the device under test (DUT) through port 1 and port 2. In this work, port 1 is selected as the source port as shown in Figure B.6.

In the test system, random and systematic measurement errors are involved in the S-parameters measurement. Although some random errors, such as thermal drift, cannot be removed systematically, the systematic error of the PNA network analyzer and the power loss of the cables can. In our work, the calibration standard technique short-open-load-through (SOLT) which uses testing and calculating short, load and through standard parameters to remove errors is used with Cascade impedance standard substrate ISS 101-190B which fit our AC probes and shown in Figure B.6.

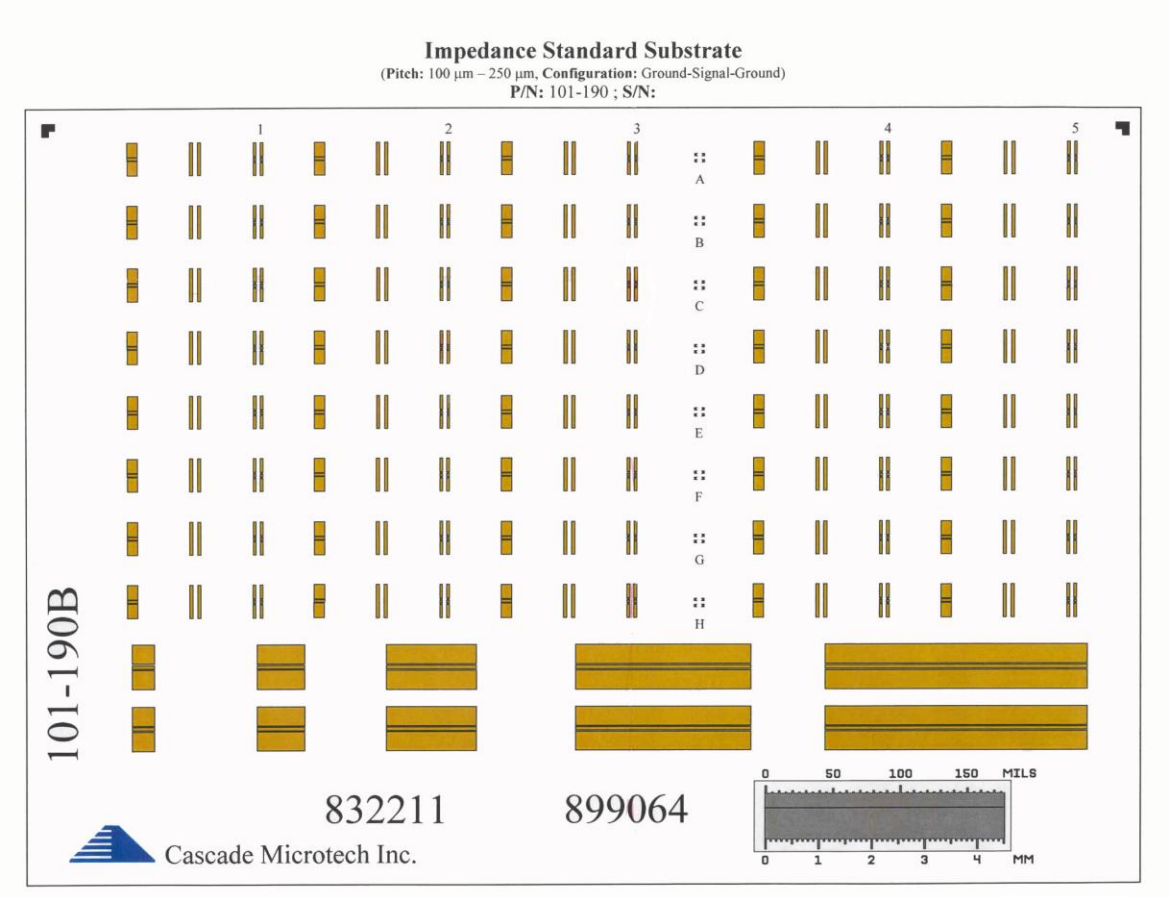

Figure B.6 Layout of Cascade impedance standard substrate 101-190B (Cascade Microtech Inc.)

B.3 S-Parameters Measurement for Standalone MOSFET

Similar to DC measurement, S-parameters measurement for standalone MOSFET was carried out first to check the setup of measurement system, the measurement method and RF performance of the transistor. The S-parameters measurement circuit is shown in Figure B.7. The DC power from HP4155 and AC power from PNA are combined in bias Ts and the output signals go into the NMOS through AC pads IN and OUT.

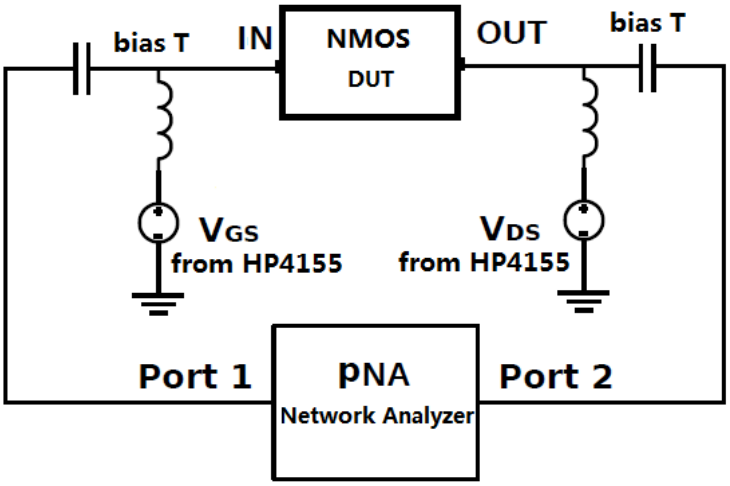

Figure B.7 Circuit of the S-parameter measurement system for standalone NMOS

Take biases set V_{GS} = 0.55V and V_{DS} = 1V (I_{DS} = 4.5 mA) for example, the measurement results is shown in Figure B.8:

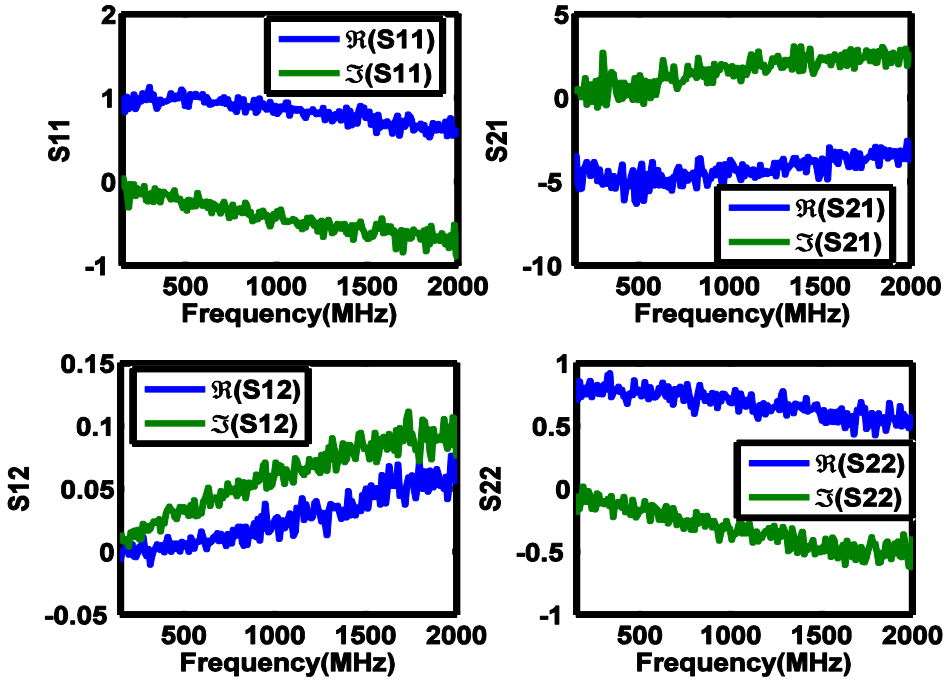

Figure B.8 Real and image parts of S-parameters versus frequency for standalone NMOS

Changing these data into dB unit by S_{dB} = 20 log |S|, we can see Figure B.9

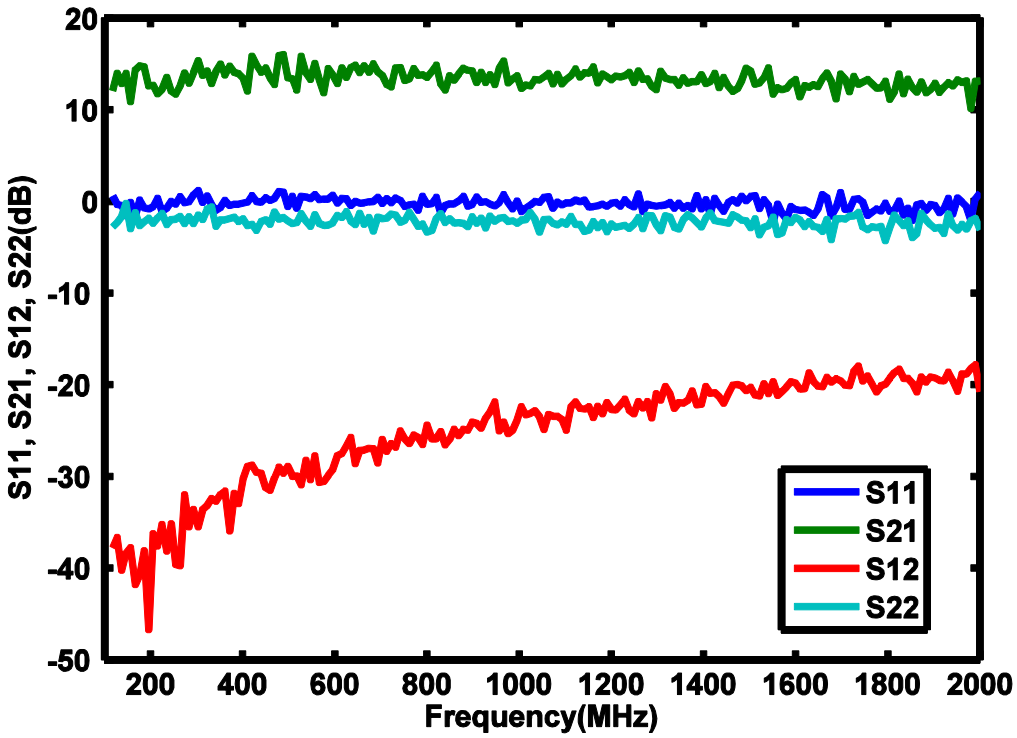

Figure B.9 S-parameters versus frequency for standalone NMOS in dB unit

As we mentioned in section B.1, S_{21} and S_{12} are the forward and reverse voltage gain separately. In Figure B.9, we can see the forward gain S_{21} is between 13dB to 14dB and it begins to drop a little at higher frequency. Reverse gain S_{12} is between -40dB to -20dB which is very small compared to other S-parameters. And it increases with rising frequency. Moreover, S_{11} and S_{22} is around 0 dB. These S-parameters represent that this NMOS transistor work well at the bias set V_{GS} = 0.55V and V_{DS} = 1V.

Besides S-parameters, the admittances Y-parameters are also common multi-port network parameters to check RF characteristics. Y-parameters of two-port network are usually defined by

$$[i_n] = [Y][V_n] \tag{B.9}$$

We can extract Y-parameters from S-parameters as described in by

$$Y_{11} = \frac{1}{Z_o} \frac{(1-S_{11})\quad(1+S_{22})+S_{12}S_{21}}{(1+S_{11})\quad(1+S_{22})-S_{12}S_{21}} \tag{B.10a}$$

$$Y_{12} = \frac{1}{Z_o} \frac{-2S_{12}}{(1+S_{11})\quad(1+S_{22})-S_{12}S_{21}} \tag{B.10b}$$

$$Y_{21} = \frac{1}{Z_o} \frac{-2S_{21}}{(1+S_{11})\quad(1+S_{22})-S_{12}S_{21}} \tag{B.10c}$$

$$Y_{22} = \frac{1}{Z_o} \frac{(1+S_{11})\quad(1-S_{22})+S_{12}S_{21}}{(1+S_{11})\quad(1+S_{22})-S_{12}S_{21}} \tag{B.10d}$$

And the calculation results is shown in Figure B.10

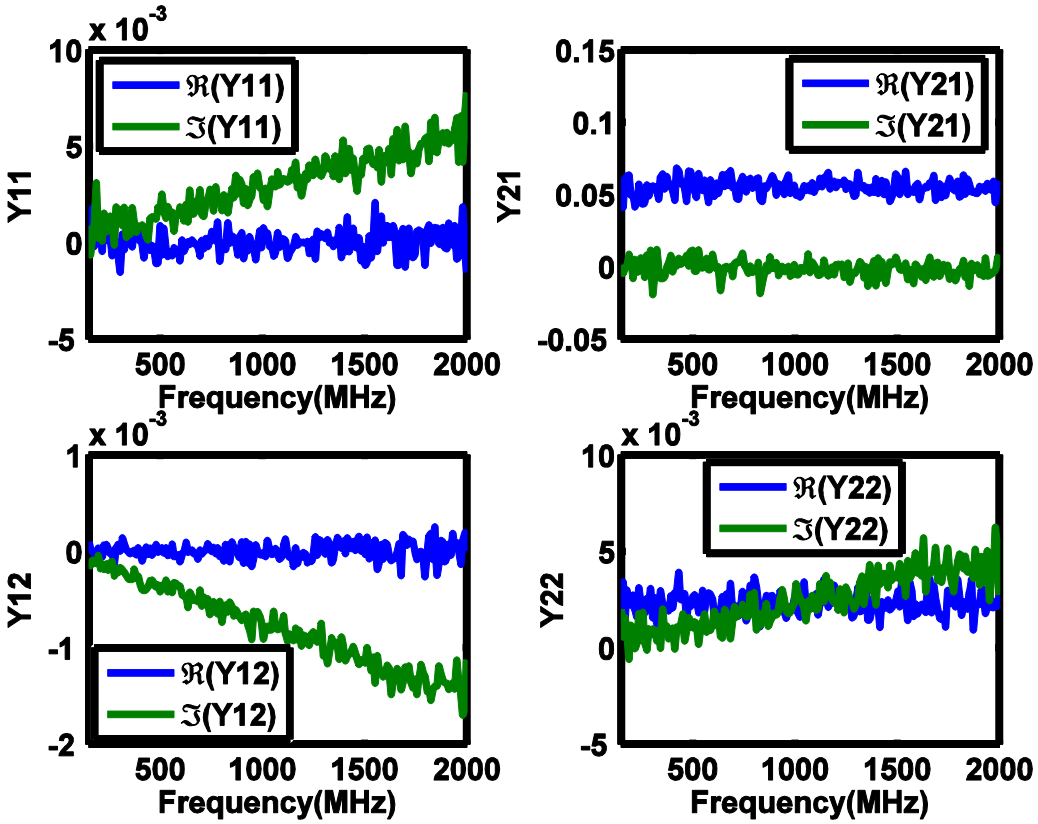

Figure B.10 Y-parameters versus frequency for standalone NMOS

B.4 S-Parameters Measurement for integrated DUT and TIA System

The electrical circuit for S-parameters measurement for DUT and TIA is shown in Figure B.11.

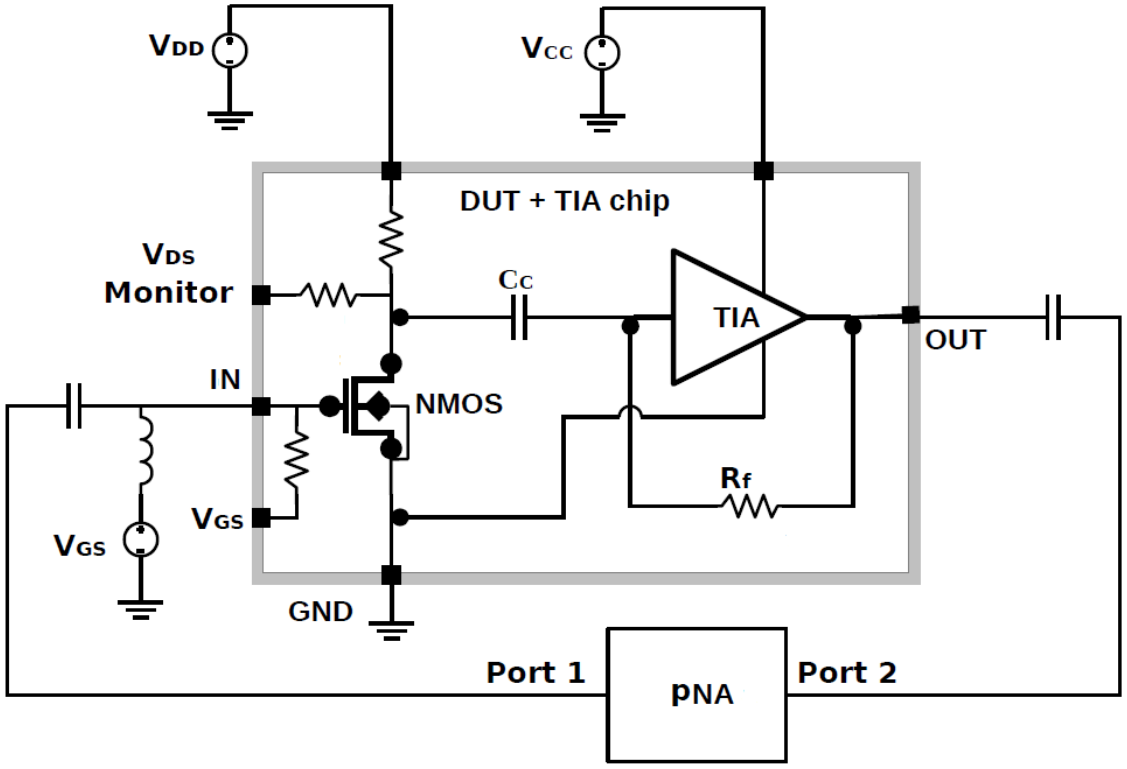

Figure B.11 S-parameters measurement system circuit

In this measurement system, the DUT and TIA are considered as a whole system. HP4155 is used to provide DC power for NMOS and TIA through RF pad IN, DC pads V_{DD} and V_{CC}. In this measurement, DC pads, RF pads IN and OUT all are connected to the probes like shown in Figure B.12.

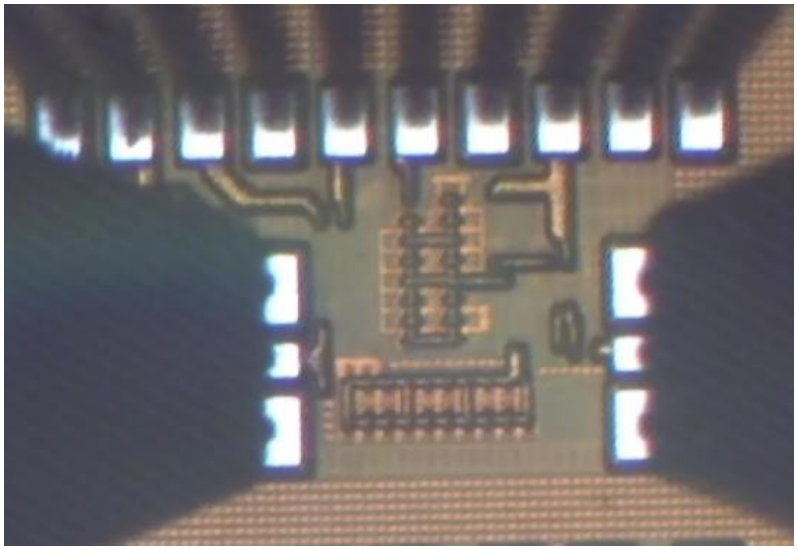

Figure B.12 Die photo with two AC probe and DC probes on pads for S-parameters measurement

One attention for S-parameters measurement is choosing the power value on PNA. When frequency = 1GHz, V_{ds} = 1 V and V_{gs} = 0.51 V, as shown in Figure B.13, the source power chosen for our work is -60 dBm which is small enough to neglect its effect on DC characteristics and also not too small to cause the RF characteristic distortion for our project.

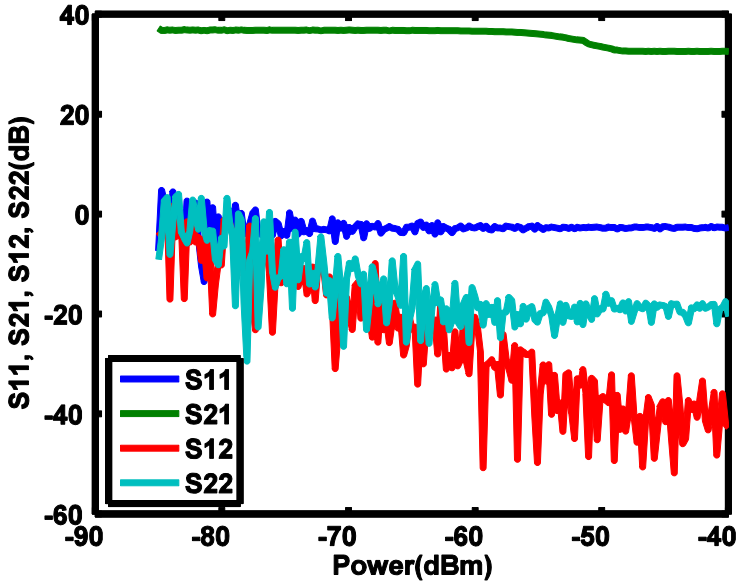

Figure B.13 Power sweep for S-parameters measurement

For an instance, the tested S-parameters for the DUT and TIA system at bias set V_{GS} = 0.51V, V_{DS} = 0.18V is shown in Figure B.13

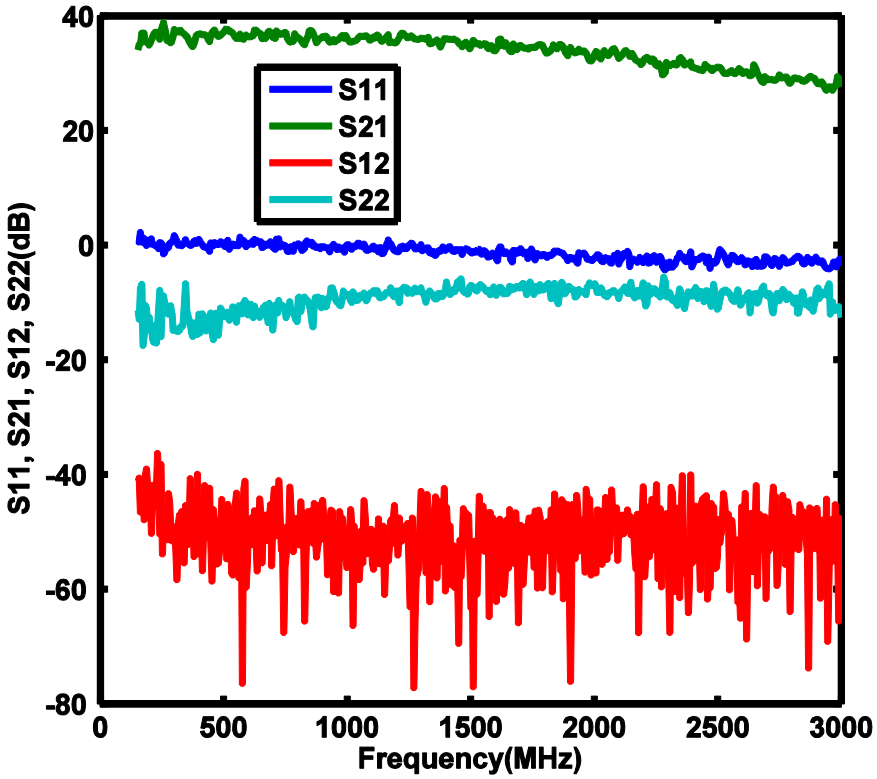

Figure B.14 S-parameters versus frequency for NMOS + TIA

In Figure B.14, S_{21} of the NMOS + TIA system keeps staying at 42 dB from 100 MHz to 1.50 GHz at 42 dB, and after 1.50 GHz, it drops from 28 dB to 23 dB. The reverse voltage gain S_{12} is between -60 dB to -40 dB. S_{11} keeps staying at 0 dB at lower frequency and it begins to drops approximately after 1.50 GHz. At 3 GHz, it drops to -3 dB. S_{22} decreases from -1 dB to -4 dB from 400 MHz to 3 GHz.

Besides, we can get equivalent input impedance of this NMOS + TIA system Z_{in} from S-parameters.

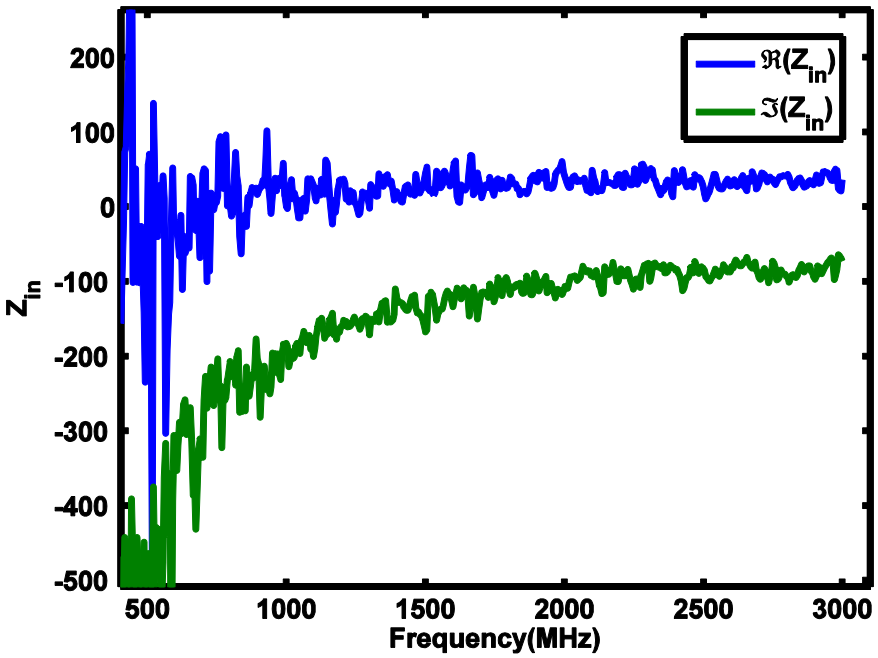

Figure B.15 Equivalent input impedance versus frequency for NMOS + TIA

Figure B.15 shows us that the real part of the equivalent of the input impedance seems like a resistor which values R = 36 Ω and is almost not changed with frequency after 500 MHz. Neglecting the effect of inductance, the image part of the input impedance $\Im(Z_{in})$ is given by

$$\Im(Z_{in}) = \frac{1}{i\omega C} \tag{B.111}$$

From equation B.13, we can derive equivalent input capacitance C to be

$$C = \frac{-1}{\omega \Im(Z_{in})} \tag{B.12}$$

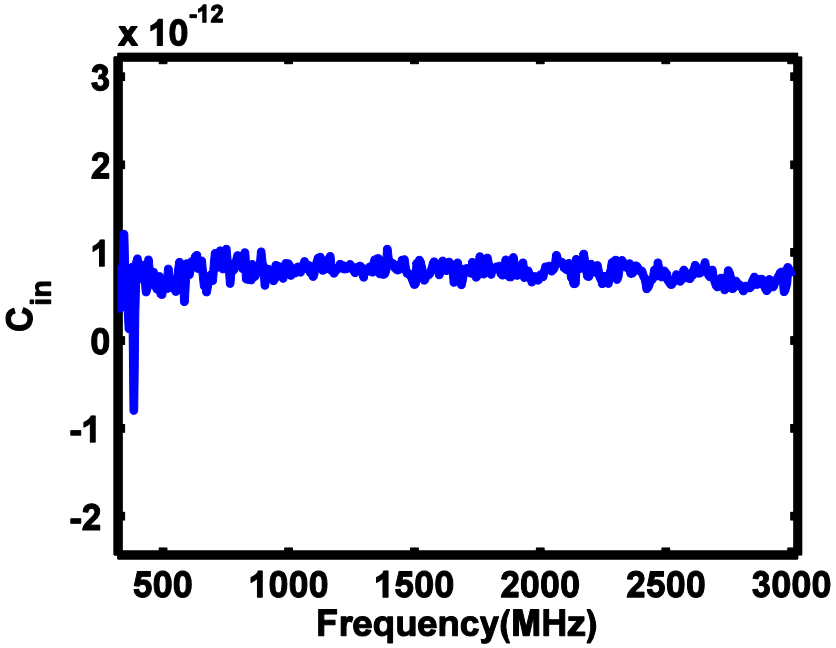

Figure B.16 Equivalent input capacitance versus frequency for NMOS + TIA

Equivalent input capacitance shown in Figure B.16 is around 0.8 pF. The equivalent input impedance can be considered as the resistor and capacitor in series. From Figure B.15 and Figure B.16, the magnitude of the equivalent input impedance can be calculated by

$$Z_{in} = R + \frac{1}{i\omega C}. \tag{B.13}$$

The magnitude of equivalent input impedance is shown in figure B.17.

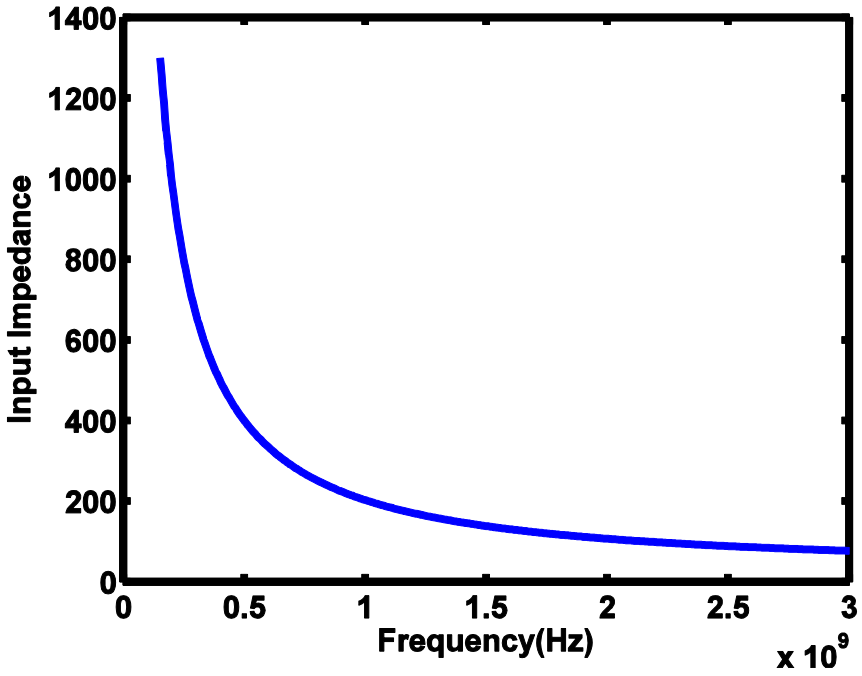

Figure B.17 Magnitude of equivalent input impedance for NMOS + TIA

Bibliography

[1] A. van der Ziel, "Noise in Solid-state Devices and Lasers," *proceeding of the IEEE*, vol. 58, No. 8, August 1970.

[2] Y. Nemirovsky, I. Brouk and C. G. Jakobson, "1/f Noise in CMOS Transistors for Analog Applications," *IEEE transactions on electron devices*, vol. 48, No. 5, May 2001.

[3] A. Hati, D. A. Howe, F. L. Walls and D. Walker, "Noise Figure vs. PM Noise Measurements: A Study at Microwave Frequencies," *IEEE International Frequency Control Symposium and PDA Exhibition*, 2003.

[4] Y. Tsividis, *Operation and Modeling of The MOS transistor*, McGraw-Hill Inc., 1999.

[5] J. B. Johnson,"Thermal Agitation of Electricity in Conductors," *Phys. Rev*. 32, 97–109, 1928.

[6] A. Van der Ziel, "Thermal Noise in Field-Effect Transistors", *Proc. of the IRE*, vol. 56, pp. 1808-1812, August 1962.

[7] C. Chen and M. J. Deen,"Channel Noise Modeling of Deep Submicron MOSFETs, "*IEEE IEEE transactions on electron devices*, vol. 49, No. 8, August 2002.

[8] J. C. J. Paasschens, A. J. Scholten, and R. van Langevelde, "Generalizations of the Klaassen-Prins equation for calculating the noise of semiconductor devices", *IEEE transactions on electron devices*, vol. 52, No. 11, November 2005.

[9] A. A. Abidi, "High-Frequency Noise Measurements on FET's with Small Dimensions," *IEEE transactions on electron devices*, vol. ED-33, No. 11, November 1986.

[10] S. Dronavalli and R. P. Jindal, "CMOS Device Noise Considerations for Terabit Lightwave Systems," *IEEE transactions on electron devices*, vol. 53, No. 4, April 2006.

[11] C. Chen, "Thermal Noise in Modern CMOS Technology," *Solid State Circuits Technologies*, InTech, 2010.

[12] C.Chen, M.J.Deen, M. Matloubian and Y. Cheng, "Extraction of the induced gate noise, channel thermal noise and their correlation in sub-micron MOSFETs from RF noise measurements," *Microelectronic Test Structures*, 2001. ICMTS 2001.

[13] B. M. Wilamoski and D. Irvin, *Fundamentals of Industrial Electronics*, Taylor & Francis Group, 2011

[14] K. Han, K. Lee and H. Shin, "Thermal Noise Modeling for Short-Channel MOSFET's," *Simulation of Semiconductor Processes and Devices*, SISPAD 2003.

[15] K. Yan, *Noise Measurements, Models and Analysis in GaAs MESFETs Circuit Design*, PHD dissertation, Oregon State University, 1996.

[16] H. A. Haus et al., "Representation of Noise in Linear Twoports", *Proc. IRE*, vol. 48, no. 1, pp. 69–74, Jan. 1960.

[17] H. Rothe and W. Dahlke, "Theory of noisy fourpoles," *Proceedings of the IRE*, Vol. 44, , pp. 811–818, June 1956.

[18] L., R. Q., "The determination of device noise parameters". *Proc. of the IEEE*, Vol. 57, No. 8, pp. 1461-1462, Aug. 1969,

[19] M. Mitama, and H. Katoh, "An improved computational method for noise parameter measurement," *IEEE Trans. Microwave Theory Tech*., Vol. MTT-27, No. 6, pp. 612-615, June 1979.

[20] G. I. Vasilescu, G. Alquie, and M. Krim, "Exact computation of two-port noise parameters," *Electron. Lett*. , pp. 292-293, Vol. 25, No. 4, Feb. 1988.

[21] O'Callaghan, J.M. and Mondal, J.P,"A vector approach for noise parameter fitting and selection of source admittances",*IEEE Trans. Microwave Theory Tech*., Vol. 28, No. 8, pp. 1376-1382. Aug.1991.

[22] C. H. Chen, et al., "Novel noise parameter determination for on-wafer microwave noise measurements". *IEEE Trans. Instrum. Meas*., Vol. 57, Issue 11, pp. 2462-2471, May 2007.

[23] L. F. Tiemeijer, R. Havens, R. Kort, and A. J. Scholten, "Improved Y-factor method for wide-band on-wafer noise parameter measurements," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 9, pp. 2917–2925, Sep. 2005.

[24] S. Tedja, H.H. Wiliams, J. van der Spiegel, F.M. Newcomer and R. Van Berg. "Noise Spectral Density Measurements of a Radiation Hardened CMOS Process in the Weak and Moderate Inversion," *IEEE Transactions on Nuclear Science*. Vol. 39(4). pp. 804-808, 1992.

[25] S. Tedja, "Analytical and Experimental Studies of Thermal Noise in MOSFET's", *IEEE transactions on electron devices*, vol. 41, No. I I , Novenber 1994.

[26] J. Cressler and G. Niu, *Silicon-Germanium Heterojunction Bipolar Transistors.* Boston, MA/USA: Artech House, INC., 2002.

[27] *Making RF Power and Frequency Measurements with Spectrum and Signal Analyzers*, Agilent Technologies, Inc. 2012

[28] *Agilent Technologies E8362B, E8363B and E8364B Option H85 User's and Service Guide Supplement*, Agilent Technologies, Inc. 2004, 2005, 2006.

[29] *Measurement Guide and Programing Examples PSA and ESA Series Spectrum Analyzers*, Agilent Technologies, Inc. 2004

[30] R.Ludwig, P.Bretchko, *RF Circuit Design: Theory and Applications*, Prentice Hall, New York, 2000

[31] X. Wei, G. Niu, Y. Li, et al., "Experimental characterization and simulation of RF intermodulation linearity in a 90 nm RF CMOS technology", *in Dig. of IEEE Radio Frequency Integrated Circuits Symp.*, pp. 251-254, 2008.