Design of Wide Band Transformer-Based Oscillator and Capacitive Coupled Multi-Phase VCO

by

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Abstract

Since globe wireless demand is increasing rapidly, more delicate and functional radio frequency (RF) devices are required. Software defined radio (SDR) has been introduced to address the challenges in this complicated wireless environment, which requires wireless systems to be compatible with various wireless standards and protocols. Voltage control oscillator (VCO) is a critical building block of wireless transceivers. For SDR applications, VCOs are required to have wide tuning range, low noise and low power in order to cover multiple frequency bands. In addition, multi-phase VCOs are often needed to generate multi-phase local oscillation (LO) signals for quadrature transceiver and phase array applications.

Two kinds of VCOs are proposed in this thesis for different applications. One is a quad-band transformer based VCO using four inductors and each inductor has its own independent cross-coupled core. The proposed VCO circuit contains two main cores and two auxiliary cores, and all cores are designed to have independent current sources for fully controlling the mutual inductance. This VCO circuit was fabricated in a 0.18 μm SiGe BiCMOS technology. The VCO prototypes cover most of the cellular bands.

Also presented is a 0.85 V eight-phase capacitive coupling voltage-controlled oscillator (CCVCO) with enhanced swing for low power supply applications. The CCVCO comprises novel multi-phase generation techniques, and employed not only for eight-phase generation, but also for phase noise reduction. The proposed coupling method applying to an 8-phase VCO design has intrinsic advantage of phase noise reduction comparing to its single-phase VCO counterpart.

Acknowledgments

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List of Abbreviations

VCO	Voltage control oscillator
SDR	Software defined radio
PLL	Phase lock loop
FoM	Figure of merit
ADC	Analog to digital convertor
CC	Capacitive coupling
ES	Enhanced swing
TR	Tuning range
LO	Local oscillator

Chapter 1

Introduction

1.1 Motivations

Since globe wireless demand is increasing rapidly, more delicate and functional RF devices are required. The term named SDR is presented with this worldwide trend, and this requires wireless system being more compatible with various protocols. VCO(voltage control oscillator), as one of essential parts in both receiver and transceiver, is closely related to the term SDR, due to it needs to provides not only large tunable frequency range, but also low phase noise for the wireless system. What's more, as interleaving strategy needs to meet higher processing speed and other wireless systems' purposes, multi-phase VCO with low phase noise is also required to be designed.

VCO in radio frequency is mainly composed of inductor, capacitor and active device, due to its much lower noise comparing to other oscillators which is without inductor and capacitor. However, in order to make VCO more functional with remaining its low phase noise, it requires to be designed carefully avoiding from parasitic components which would degrade the Q of LC tank. Since wide tuning range and multi-phase VCO are two major issue to meet nowadays' needs, and are always trend off with phase noise, the design of either wide tuning range or multi-phase VCO is biggest challenge of VCO design.

In this work, wideband transformer-based oscillator and capacitive coupled multi-phase VCOs are designed. The proposed designs are carefully make trend off among phase noise, wide tuning range and multi-phase in order to meet both function and quality needs.

1.2 Thesis Organization

The thesis has been organized to present VCO architecture as well as critical technology concerned design. Chapter 2 of the thesis summarizes previous presented VCO works with analyzing their characters. Chapter 3 presents the design of wide tuning range VCO based on transformer with its concept, topology, theoretical analysis and implementation. Chapter 4 presents the design of multi-phase VCO with low noise with its concept, topology and simulation analysis results. Chapter 5 draws conclusion of these design and shows future potential of this field.

Chapter 2

Summary of Previous work on VCO

2.1 VCO Performance Metrics

In the VCO design, there're three important parameters to judge the performance of VCO, The most important one is called phase noise which represents the amount of noise density in spectrum per Hz, and another is called tuning range which represents frequency range it can cover. The most comprehensive one is named figure of merit (FoM) which consider many parameters, i.e., phase noise, power consumption, even chip area, and so on.

First, phase noise is always specified in dBc/Hz, which means noise a 1-Hz bandwidth measured in decibels with respect to the carrier, and intended to be as small as possible. The most general form of phase noise is shown below:

$$L(\Delta\omega) = No/Pc \tag{2.1}$$

No is noise power in 1Hz bandwidth at $\omega + \Delta\omega$ and Pc is total carrier power. However, as the general form of it cannot provide any design guidance, more specific equation of phase noise was expressed by Leeson's equation [1] shown in (2.2):

$$L_{vco}(\Delta f) = 10\log\left\{\frac{FkT}{2P_s}\left[1 + \left(\frac{f_0}{2\Delta f Q_L}\right)^2\right]\left[1 + \frac{f_c}{|\Delta f|}\right]\right\} \tag{2.2}$$

where K is Boltzmann constant, T is absolute temperature, P is signal power, Q-tank is loaded quality factor, and F is fitting noise factor which related to both resistor noise and parasitic noise from active device. As shown in Leeson's equation, the phase noise is closely related to Q of LC tank, noise from both active and passive device. This gives us a guidance of how to trend-off among those parameters in VCO design, but if using this equation without consideration of other hidden parameters [2-3], it will lead to error.

Secondly, tuning range is defined as the tunable frequency range over the center frequency, namely,

$$\mathrm{TR} = \Delta\omega/\omega_c \tag{2.3}$$

Tuning range is intended to be as large as possible without considering other VCO parameters. However, in actual design, tuning range is often a trade-off with phase noise, power consumption, and so on, due to parasitic components added as range increasing. Thus, in order to enlarge tuning range, special techniques are needed, i.e., dual-band VCO.

Finally, FoM is the most general parameters than other two, due to it involves all the worthy testing and design parameters for more fair evaluation, and it is intended to be as large as possible in VCO design. However, FoM are differing from papers for different evaluation, and the most common one is shown in (2.4):

$$\mathrm{FoM} = 10\log\left(\left(\frac{\omega_0}{\Delta\omega}\right)^2 \frac{1\mathrm{mW}}{\mathrm{L}(\Delta\omega)\mathrm{P}}\right) \tag{2.4}$$

where ω_0 is oscillating frequency, $\Delta\omega$ is offset frequency from the oscillating one, $\mathrm{L}(\Delta\omega)$ is phase noise, and P is total power of VCO core. This parameter gives restriction on phase noise improvement, in order to show techniques other than purely increasing signal power. However, it also involves intrinsic phase noise degradation for higher oscillation frequencies. What's more, there's also another two FoM expressions, which is shown in (2.5):

$$\mathrm{FoM_A} = 10\log\left(\left(\frac{\omega_0}{\Delta\omega}\right)^2 \frac{1\mathrm{mW}}{\mathrm{L}(\Delta\omega)\mathrm{P}} \frac{1\mathrm{mm}^2}{\mathrm{A}}\right) \tag{2.5 (a)}$$

$$\mathrm{FoM_W} = 10\log\left(\left(\frac{\omega_0\omega_{\mathrm{tune}}}{\Delta\omega}\right)^2 \frac{1\mathrm{mW}}{\mathrm{L}(\Delta\omega)\mathrm{P}} \frac{1\mathrm{mm}^2}{\mathrm{A}}\right) \tag{2.5 (b)}$$

The $\mathrm{FoM_A}$ adds area into consideration, while $\mathrm{FOM_W}$ further adding tuning range into consideration. However, those expressions are intended for different applications and are not used as a common VCO performance metrics.

2.2 A Dual-band VCO

Since the term SDR was presented, multi-standard, multi-mode and multi-band wireless communication is heavily demanded than ever. This makes design of VCO a challenge, due to the trade-off between wide tuning range and acceptable phase noise, as reason of Q degradation and parasitic problems.

In general, the frequency tuning of the VCO is performed by varying the capacitor or inductor. Because the tuning range at high frequencies becomes narrow as the parasitic capacitance is increased, enlarging the tuning range cannot be done by independently varying either of capacitor. Employing capacitor switch array [4] is one way to increasing tuning range by turning switch on/off to control the number of capacitors in LC tank. However, increasing parasitic resistance [5] of the switch reduces the Q-factor of the resonators. In order to make frequency change large enough to be continuous, it requires C_{max}/C_{min} of varactor relatively large, and this is no doubt to make Q further degrade, due to adding parasitic resistance, and smaller inductor (shown in Fig. 2.1).

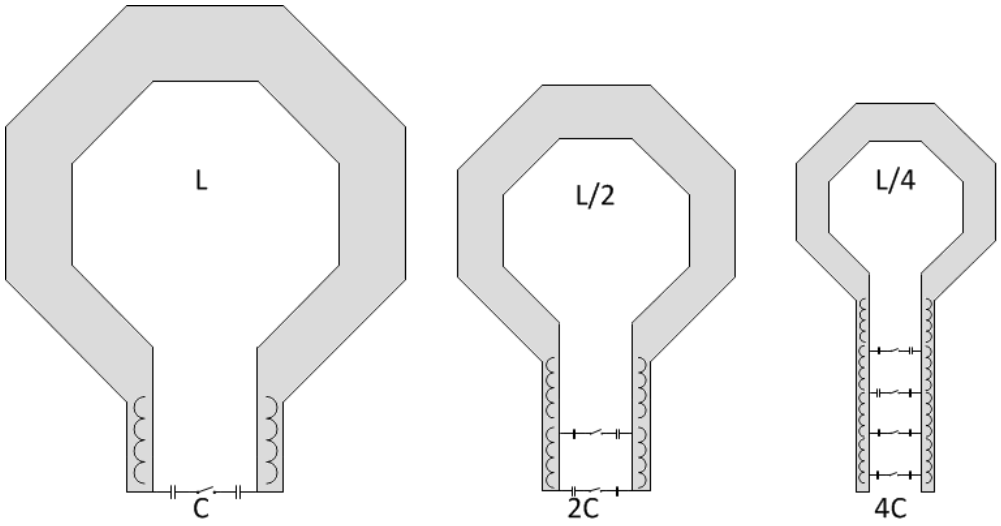


Fig. 2.1. Illustration of Q factor degradation.

As shown in Fig. 2.1, oscillation frequency should be kept constant, namely,

$$\omega = 1/\sqrt{L_{tot}C_{tot}} \tag{2.6}$$

where the L_{tot} includes the inductance from both tank and path, and C_{tot} includes the capacitance from array capacitors which are open, varactor capacitors and path parasitic components. Thus, the inductor of the tank needs to be relatively shrinking, while array capacitors are adding.

Alternatively, switched parallel VCOs can be used to form a dual-band VCO [6], and it has the advantage of better performance, due to inductor hasn't to be shrinking as single core does and capacitor array hasn't to be that much, which makes parasitic inductance from capacitor array fewer and the series resistor of inductor smaller, and phase noise is intrinsically improved due to higher Q factor. The topology of the dual-band VCO is shown in Fig. 2.2.

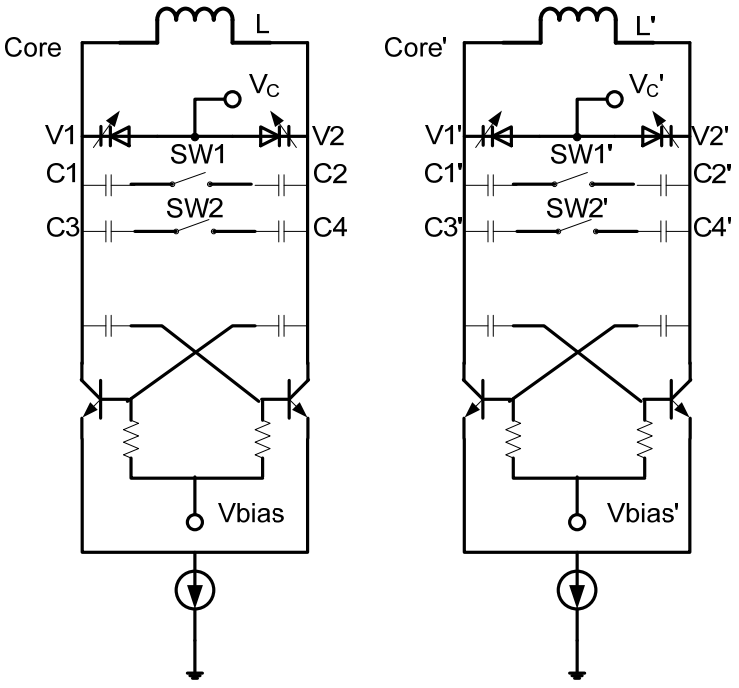


Fig. 2.2. Conventional dual-band VCO.

First, Core, in Fig. 2.2, at left side is taken to illustrate for why C_{max}/C_{min} of varactor should be large enough. Since the tuning technique of this core is implemented by turning switches on/off to change the capacitance in the tank, the varactors v1 and v2 need to make each of those array

change continuously in frequency, thus, C_{max} of varactor has to be large enough comparing to the sum of capacitance of all the capacitor array, in order to make fine tuning frequency. Meanwhile, C_{min} cannot be too large, or inductor would be over shirked, as center frequency is fixed. What's more, C_{max}/ C_{min} means large parasitic resistor in varactor and in smaller inductor, which mentioned above.

After analysis of a single core, it is clearer to see the advantages of this dual-band topology, intrinsically from releasing the pressure for a single pair varactor to two pairs of varactor and inductor. Here, it is worth noting that, although Core and Core' are the same structure, all the devices parameters are different, since they are serving for different center frequency. The most important issue of this dual-band topology is needed to make frequencies from both cores to be continuous, and this is shown in (2.7) (supposing that Core serving for higher frequency).

$$\omega = 1/\sqrt{L_{tank}(C_1(\text{or } C_2) + C_3(\text{or } C_4) + C_{max})} = 1/\sqrt{L'_{tank}C_{min}'} \tag{2.7}$$

where, C_{max} is largest capacitance of v1 or v2, and C_{min} is smallest capacitance of v1' or v2'.

2.3 Phase Noise Improvement of the Dual-band VCO

Since capacitor arrays would introduce noise to degrade phase noise which cannot be neglected, the new topology, which is named mode switching VCO (MSVCO) [7], was presented to cancel the noise from capacitor arrays. The main concept of switching VCO is based on dual-band LC oscillator, and using switching to control the coupling way of those two cores. The topology of this VCO is shown in Fig. 2.3.

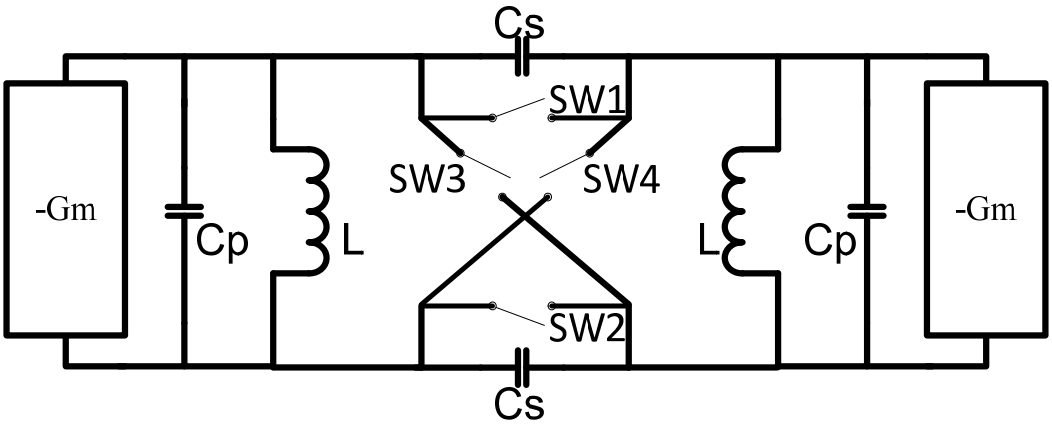


Fig. 2.3. Block diagram of the mode MSVCO.

The entire circuit mainly contains two cores and two LC tanks (L, Cp), and these two cores including tanks are designed to be symmetric for phase balance purpose. -Gm is provided by conventional cross couple CMOS which is the same as shown in Fig.2.2. What's more, there are four switches including SW1~SW4, together with Cs can achieve switch mode function. There're two modes by changing switches, and they are called even mode and odd mode.

The even mode is by turning SW1, SW2 on, and SW3, SW4 off. The equivalent circuit is shown is Fig. 2.4.

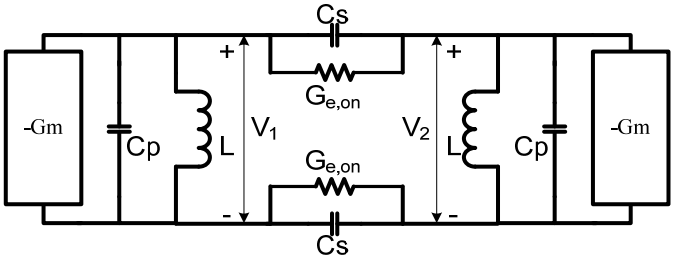


Fig. 2.4. Even mode operation of MSVCO.

Since both tanks have the same impedance network, the voltages V_1 and V_2 are in phase and equals to each other. Thus, there's no dc and ac current flowing through Cs and $G_{e,on}$, and the Fig. 2.4 can be further simplified as shown in Fig. 2.5.

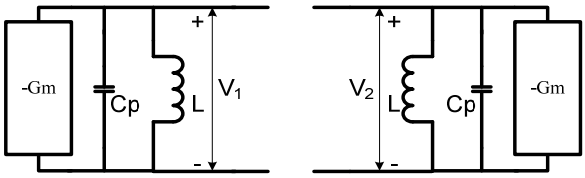


Fig. 2.5. Equivalent circuit of MSVCO even mode operation.

As shown in Fig. 2.5, both cores can be treat as independent cores, and the tank is consists of Cp and L. Thus, the oscillating frequency can be expressed as:

$$\omega_e = \frac{1}{\sqrt{LC_p}} \tag{2.8}$$

The odd mode is obtained by turning SW1, SW2 off, and SW3, SW4 on. The equivalent circuit is shown is Fig. 2.6.

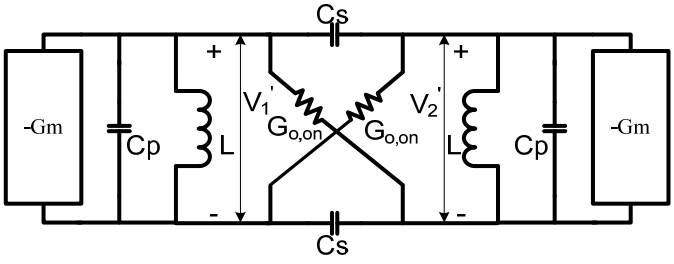


Fig. 2.6. Odd mode operation of MSVCO.

Since both tanks have the mirror impedance network, V_1' is equals to $-V_2'$, there's no dc and ac current flowing through $G_{o,on}$, and the middle of Cs can be treated as virtual ground. So, the block diagram, in Fig. 2.6., can be further simplified as shown in Fig. 2.7.

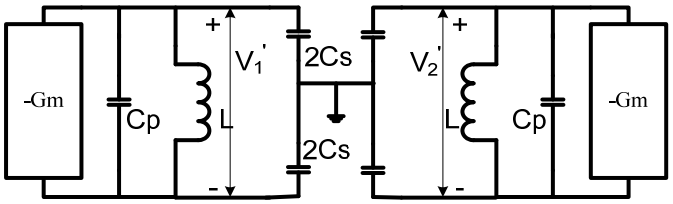


Fig. 2.7. Equivalent circuit of MSVCO odd mode operation.

As shown in. 2.7, both cores also can be treat as independent cores, but the tank is consists of Cp, L and Cs. Thus, the oscillating frequency can be express as:

$$\omega_o = \frac{1}{\sqrt{L(C_p+C_s)}} \tag{2.9}$$

By comparison two modes, there can be easily observed that odd mode serving for low center frequency and even mode serving for higher frequency. In this aspect, this structure is similar to dual-band VCO which has two cores and each of them serving for different frequency. However, this topology can achieve better phase noise than Dual-band VCO, due to its noise cancelling technique.

In order to give better explanation for noise cancelling from switches, firstly startup condition of those two modes are introduced. Since, the oscillation condition should be:

$$G_m > G_{tank} \tag{2.10}$$

Here should be noting that any parasitic conductance has been counted in G_{tank}. In the even mode, the startup condition is:

$$G_m > G_L + G_{o,off} \tag{2.11(a)}$$

where G_L is the conductance from the tank, $G_{o,off}$ is the conductance when SW3,SW4 are off. In

this topology, the other mode should also be damped, and satisfied following equation:

$$G_m < G_L + G_{e,on} \qquad (2.11(b))$$

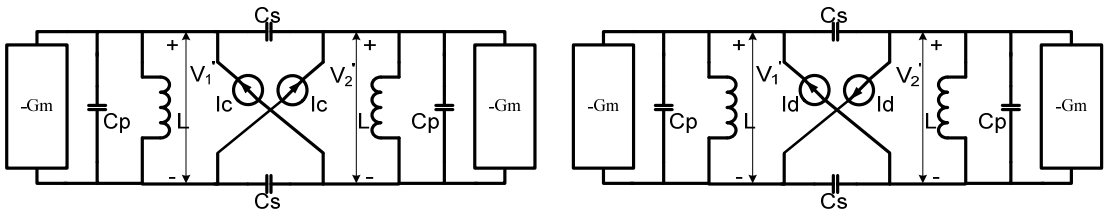
For the same reason, the odd mode should satisfy following equations:

$$G_m > G_L + G_{e,off} \qquad (2.12(a))$$

$$G_m < G_L + G_{o,on} \qquad (2.12(b))$$

If the switch is ideal one, (2.11(a)) and (2.12(a)) will no doubt be satisfied, since $G_{e,on} = G_{o,on}$ which equals to infinity and $G_{o,off} = G_{e,off}$ which equals to zero. Thus, for successfully switching to one mode and damping another one, therefore, turn-on resistor of those switches should be designed as small as possible, while turn-off resistor should be as large as possible, and this also gives a upper bound of G_m, which is shown in (2.11(b)) and (2.12(b)).

Supposing above condition are well designed, here will take odd mode of this topology to illustrate noise cancelling. The noise from $G_{o,on}$ can be separated into common noise part and differential noise part, which are shown in Fig. 2.8.



(a) Common noise cancelling (b) Differential noise cancelling

Fig. 2.8. Noise cancelling of odd mode.

The differential noise part flow either side of the same core, since $-G_m$ is generated by cross couple structure, it is differential circuit. Thus, Id following into left and right side will be treated as common mode signal and intrinsically cancelled. The common noise part of $G_{o,on}$ is treated as even mode signal to the circuit, and it is damped by odd mode working condition. That's also how

even mode resistor noise cancelled, but by reversed behavior. In sum, the resistor noise from switches will not add to the circuit by the differential structure and working mode. In order to show the noise cancelling effect, the phase noise of both dual-band VCO and switch mode VCO is shown in Fig. 2.9.

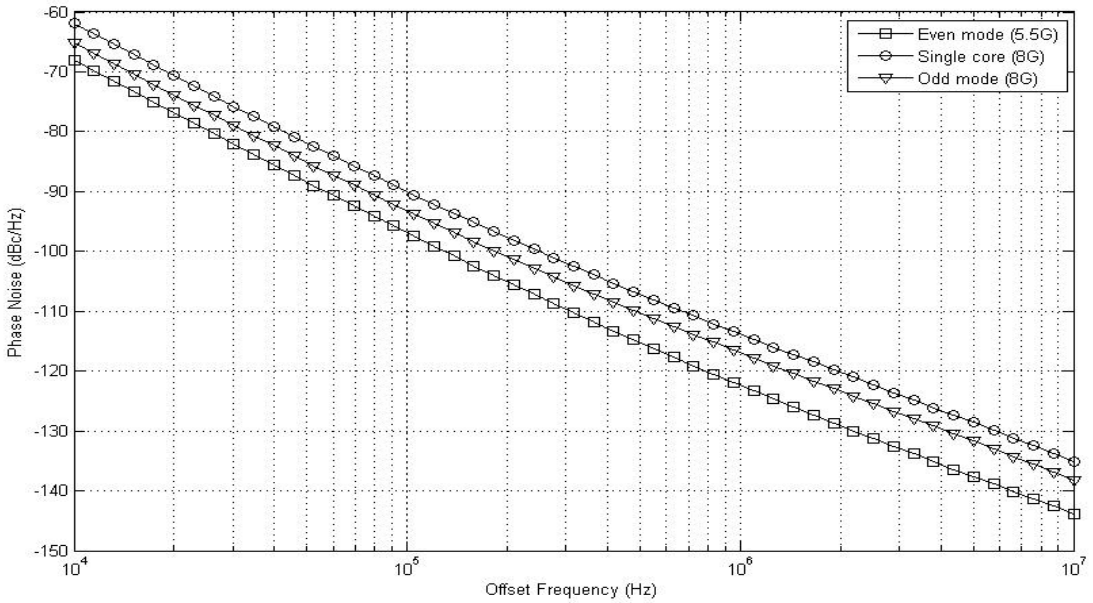


Fig. 2.9. Phase noise comparison.

where phase noise of single core (8G) is -113dBc/Hz@1MHz offset, odd mode (8G) is -117dBc/Hz@1MHz offset and even mode (5.5G) is -122dBc/Hz@1MHz offset. Since odd mode has the same frequency as single core has, their phase noise can be compared directly, and the improvement is about 4dB. As even mode is at lower frequency, 3.2 intrinsic phase noise improvement should not be counted, thus the improvement from even mode is about 5dB.

2.4 Impulse Sensitivity Function

Since ISF has close relationship with phase noise and it gives more effective guidance of how to improve phase noise than Leeson's equation in circuit structure level, especially for coupling VCO, whose active device noise is necessary to be analyzed, it is essential to give introduction of it for better illustration of following analysis.

ISF introduced by Hajimiri and Lee [8-9] models how system noise performance would be affected by analyzing noise injection through one oscillation cycle. The interpretation of ISF is derived from two kinds of impulse responses which are phase response $h_{\phi}(t,\tau)$ and amplitude impulse response$h_{A}(t,\tau)$. They together could explain how the impulse current from noise changes through those two transfer function and affect output signal, and the model of it is shown below:

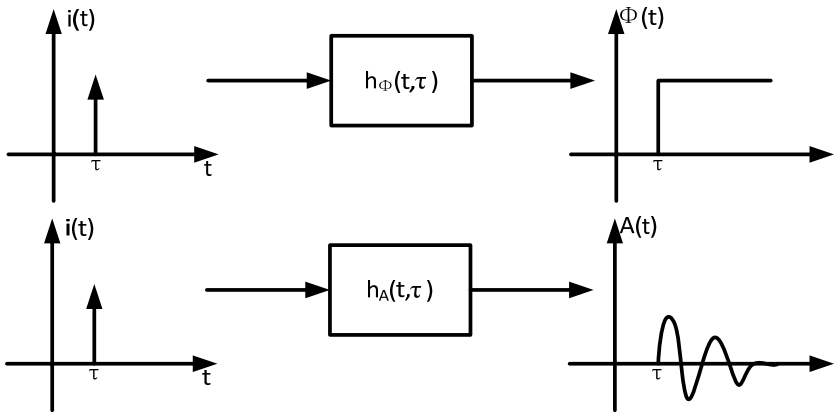


Fig. 2.10. Phase and amplitude impulse responses.

As shown in Fig. 2.10, the magnitude response would be diminished, and the VCO system can even damp this response by strong output signal and active device in real design. However, the system cannot recover output from phase response. Thus, in circuit design, phase response should be minimized by transfer it into magnitude response. For further illustrate how VCO output signal is affected, it is assumed as:

$$V = A_0(t)\cos\left(\omega t + \phi_0(t)\right) \tag{2.13}$$

When the noise impulse is injecting into maximum valve of output signal, since it has no phase component, the output signal is changed to V_1:

$$V_1 = \left(A_0(t) + A(t)\right)\cos\left(\omega t + \phi_0(t)\right) \tag{2.14}$$

By considering the model of A (t), the V_1 would be finally back to V expression, and its behavior is shown below:

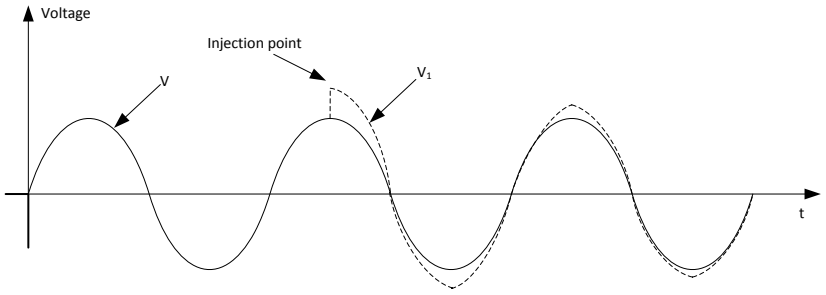


Fig. 2.11. Impulse injection at maximum voltage value.

When the noise impulse is injecting into zero crossing point of output signal, since it has no amplitude component, the output signal is changed to V_2:

$$V_1 = A_0(t)\cos\left(\omega t + \phi_0(t) + \phi(t)\right) \tag{2.15}$$

By considering the model of $\phi(t)$, the V_2 would be keeping its expression, and its behavior is shown below:

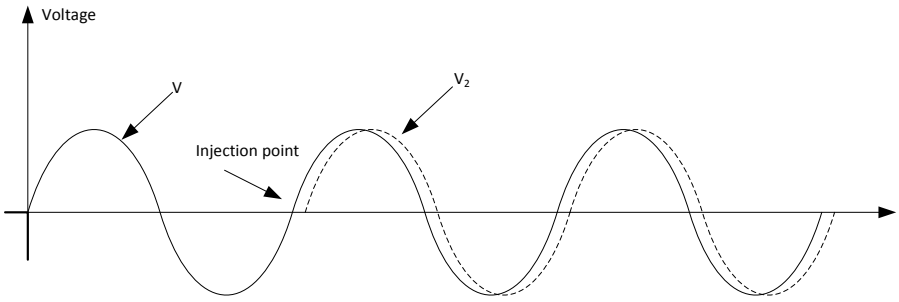


Fig. 2.12. Impulse injection at minimum voltage value.

Based on above introduction, the ISF can be defined as the noise effect accounting from each

point of a cycle with the same injection current. Normally, no matter what kind of oscillator is, the ISF has its max value at zero crossing point, which means the worst point for noise to come in. In other words, the point where has larger the ISF value would has worse phase noise by injection noise than point which has smaller ISF value. However, in analog circuit design, the zero crossing point are unable to avoid from noise injection, fortunately, the largest injection noise can be shifted from that point to lower ISF value point which usually be the maximum value of output voltage.

2.5 Coupling Techniques for Multi-Phase VCO

Since quadrature signals are essential part of RF front-end devices, like receiver and transceiver. The generation of quadrature signal is required high quality for phase accuracy and phase noise at high frequency, or the lack of phase accuracy would cause I,Q mismatch which would easily hurt both modulation and demodulation process. Additionally, noisy condition of the signal would easily cause error in sampling process. In order to ensure base band signal process, the high performance of quadrature signal design is necessary.

The most efficiency way to achieve quadrature phase signal is by coupling VCO, which not only provide accurate phase relationship, but also less noisy spectrum. One conventional way of coupling is to use transistors for coupling, and the concept of this structure is to add parallel branches of transistor with cross couple transistors. The schematic of it is shown in Fig. 2.13.

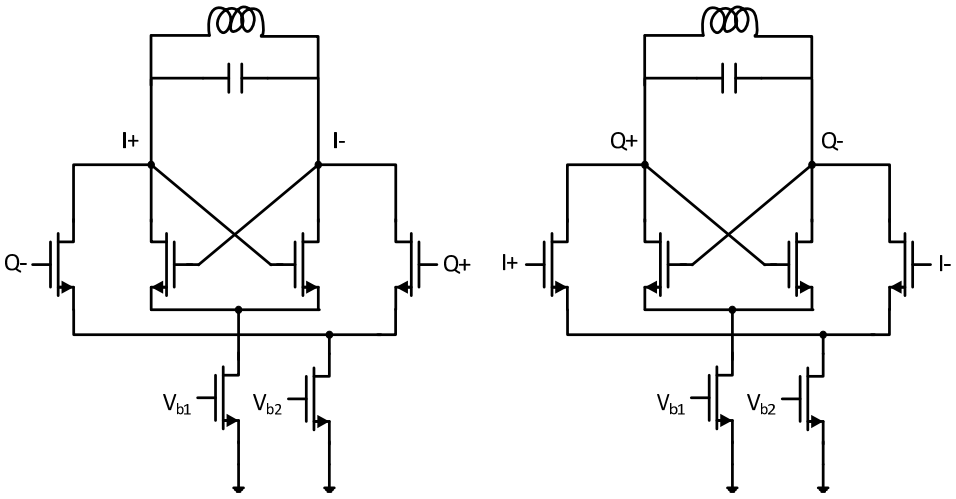


Fig. 2.13. Topology of conventional coupling VCO.

From Fig. 2.13, there can be observed that the quadrature signals are generated by coupling both outputs of a core and input of another core with transistor. The relationship between each output signal is shown below:

$$Q_+ = -Q_- \tag{2.16(a))}$$

$$I_+ = -I_- \tag{2.16(b))}$$

$$|I_+ - Q_+| = 90° \tag{2.16(c))}$$

Since their quadrature relationship, this structure is quite noisy, due to current impulse from coupling transistor happening at crossing zero part of output signal, and this is the worst point of current injection. For better illustration, here takes a pair of parallel transistors (Fig. 2.14) as an example.

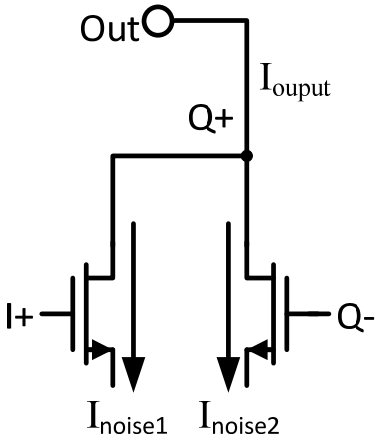


Fig. 2.14. Noise model of parallel transistors.

As shown Fig. 2.14, the output current I_{output} is conducting by the sum of I_{noise1} and I_{noise2}. From the CMOS current equation:

$$I \propto V_{GS}^2 \tag{2.17}$$

That's two say when I+ is at its maximum voltage the I_{noise1} is largest, unfortunately, due to 90 degree difference between I+ and Q+, when Q+ is at crossing zero point, I+ is at its maximum value, where the most of noise comes into the weakest point of output, according to ISF, and it is unavoidable for this case to shift it away from point, since it is coupled by transistor.

This conventional quadrature VCO is not only noisy, but also need more power consumption, as it needs extra transistors for coupling.

2.6 Phase Noise Improvement of Multi-Phase VCO

According to coupled oscillator theory [10], Coupling VCO itself will bring 1/N phase noise reduction, where N stands for the number of cores. However, due to noise comes from coupling device, this reduction is diminished. In order to avoid extra noise and power consumption by coupling device, the VCO with enhanced swing and capacitive coupling [11] was presented, and the structure is shown in Fig. 2.15.

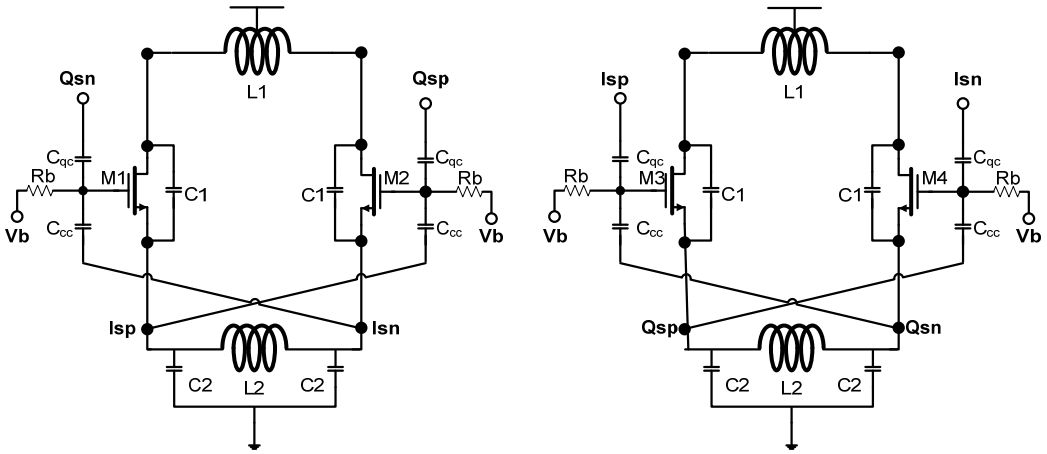


Fig. 2.15. Topology of improved VCO.

The chapter 4 would introduce similar single core design about the function of each component, here, in order to show coupling method improvement, just focus on the coupling part of this structure. Firstly, the coupling method was used is simply capacitive coupling, where use C_{qc} and C_{cc} to connect both output of two cores. One thing needs to be clear is that C_{cc} is also belonging to cross couple structure, and it is necessary for noise reduction. To make it clearer, coupling strength factor is defined as:

$$m = \frac{C_{qc}}{C_{qc}+C_{cc}} \tag{2.18}$$

The larger the coupling strength m is the more phase accuracy this circuit would be. However, m cannot be that large without restriction, since it is also related with noise reduction from coupling.

According to output quadrature relationship, V_{isn} and V_{qsn} should be difference by 90 degree. Thus, if assuming V_{isn} as:

$$V_{isn} = V_o \cos(\omega_o) \tag{2.19}$$

The V_{isp} would be:

$$V_{qsn} = V_o \sin(\omega_o) \tag{2.20}$$

Thus, there can get voltage for the gate of M_1:

$$V_{g,M1} = mV_{qsn}(t) + (1 - m)V_{isn}(t) \tag{2.21}$$

Since gate voltage can be adjusted by coupling strength factor, that's to say, there can make maximum $V_{g,M1}$ drift form zero crossing point of V_{isp}. That's because that C_{cc} breaks the quadrature relationship from gate to the corresponding output. If without C_{cc}, $V_{g,M1}$ is equals to V_{qsn} which is 270 degrees different from V_{isp}, thus it would no doubt introduce largest noise to the spectrum. For better illustration, the voltage shifting effect with different m is shown in Fig. 2.16.

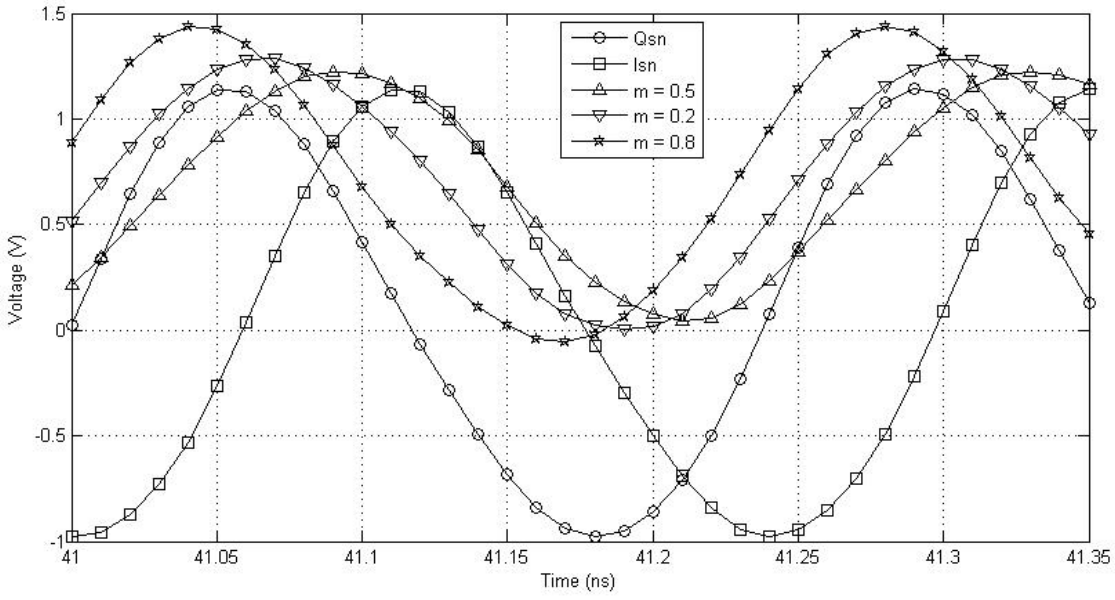


Fig. 2.16. Voltage shifting effect with different m.

From above analysis, the phase noise is intended to get improvement from both coupled oscillator

theory and drifting effect, and expected to be larger than 3 dB @1MHz offset. The simulation result of phase noise including both single and quadrature VCO structure at 4.8GHz are plotted in Fig. 2.17.

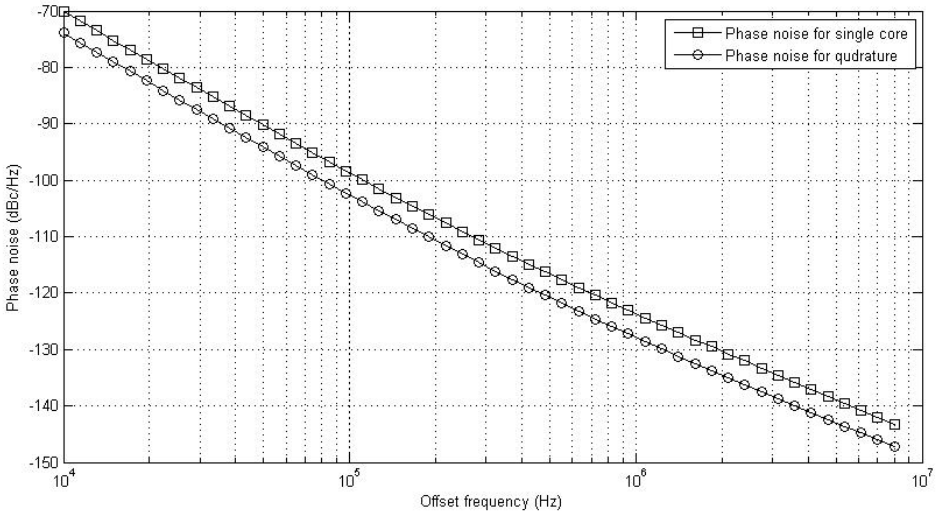


Fig. 2.17. Phase noise comparison.

From Fig. 2.17, there can be found that phase noise of single core is -123dBc/Hz@1MHz offset, and quadrature core is -127dBc/Hz@1MHz offset. Thus, simulation result quite meets the expectation which provides over 3 dB phase noise improvement.

Chapter 3

Design of A Transformer Based VCO

3.1 Architecture

After introduction of previous VCO work which are designed to achieve a certain tuning range in chapter 2, this chapter will propose a kind of transformer based VCO with Ultra wide tuning range, and resolve some problems which previous works have. Since multi band technique are utilized to achieve large tuning range, it requires large chip area for multi cores and tanks, and, among those devices, inductor is the largest device and always occupied most of the area within a layout. In additionally, even four-band VCO are not enough for tuning range purpose, thus adding more band to achieve wide tuning range is not acceptable. Based on above consideration, the proposed circuit uses transformer based technique, which can not only save area for tank inductors, but also can achieve ultra wide tuning range by its mutual inductance between each inductor.

The block diagram of the proposed VCO and is shown in Fig. 3.1, and it consists of four inductors and four cores which include varactors and capacitors.

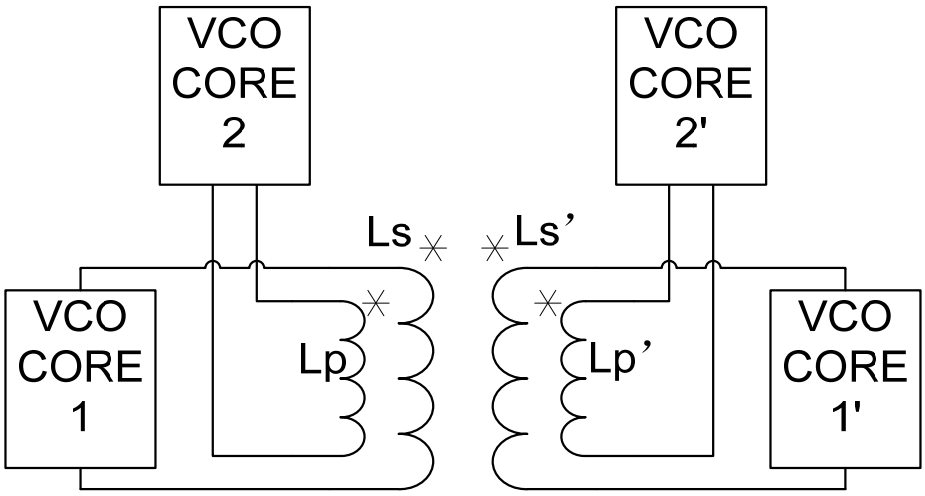


Fig. 3.1. Block diagram of proposed VCO.

Two inductors (Ls, Lp) are fabricated with top metal, and two other inductors (Ls', Lp') are on a

lower metal with same shape as upper ones. As inductance of round differential inductor [13] is known as:

$$L \propto \Delta R^2 D \tag{3.1}$$

where ΔR represents the difference between outer diameter and inner diameter, and D represents the depth of inductor layer. Due to (3.1), the lower layer inductor has smaller inductance. In addition, upper inductors and lower inductors are designed to be in the same vertical dimension, and small inductors (Lp, Lp') are inserted in the center of bigger ones (Ls, Ls'). The design details of this transformer will be introduced in next section, for now, the equivalent inductance from mutual and current effects will be discussed. By this structure, the mutual inductance is enhanced and core1' and core2' which are called auxiliary cores can switch their current to change the effect of mutual inductance. The mutual inductance controlled by current can be derived by:

$$\Psi = MI_1 + LI_2 \tag{3.2}$$

As $M = k\sqrt{L_1 L_2}$ and $\Psi = LI_1$, thus the relationship between equivalent inductance and current is given by:

$$L_m = L_1 + \frac{kI_2}{I_1}\sqrt{L_1 L_2} \tag{3.3}$$

Supposed L1 is Lp, L2 can be either inductor as Ls', Lp' or Ls, I_1 and I_2 are corresponding to the core current of L1 and L2. Due to each core is working separately, each of them can be turned on/off, therefore, L_m can reach large range of value without using small inductor which is unreliable to achieve certain frequency or work independently without further mutual effect. The behavior of this transformer focusing on equivalent inductance will be analyzed in section 3.3. Here, the circuit design will be further introduced.

The proposed circuit has two main cores (core1, core2) and two auxiliary cores (core1',

core2'), as shown in Fig. 3.1, core1' and core2' are designed to be the same as core1 and core2, and core1, core2 are built as similar structure as shown Fig. 3.2, what's more, they oscillate with L1 and L2 at 3Ghz and 6.8Ghz independently.

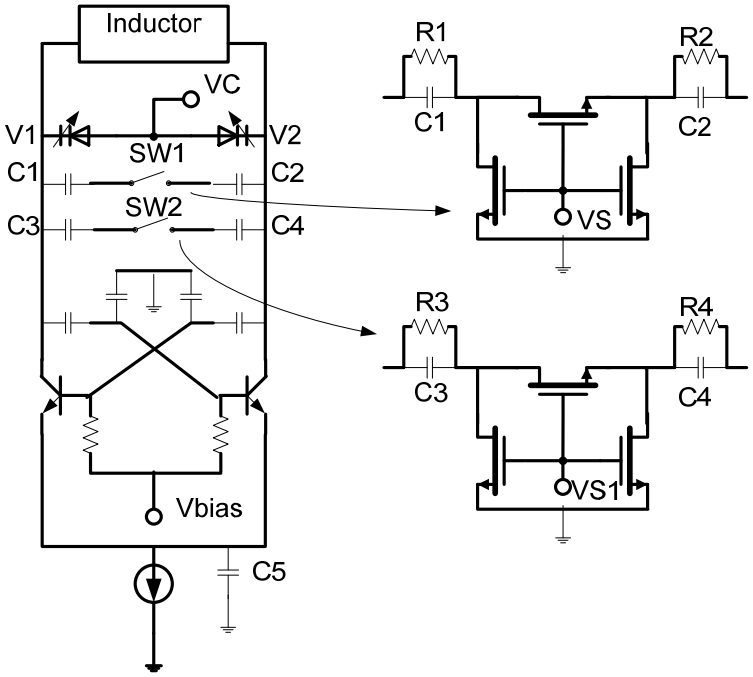


Fig. 3.2. Schematic of proposed VCO core and capacitor switch.

Differing from CMOS cross couple, this circuit chooses BJT instead, due to its lower noise and higher Gm efficiency. However, the Bias working condition of BJT is stricter than CMOS, so adjustable Vbias connected to base is chosen to ensure working condition, and capacitors which are connected to base are also used to constraint the voltage swing of base from getting into saturation state. C5 is capacitor to cancel the noise from current source which has similar function introduced in chapter 2, and it drift noise effects from zero crossing point of the output.

This proposed circuit can tune frequency by capacitor array (C1, C2 and C3, C4), and PN varactors v1 and v2. VC is bias voltage to adjust the capacitance of PN varactors and SW1 and SW2 are switches to control parallel capacitors of LC tank. In order to make switch more efficient,

this circuit choose three NMOS to increase on/off speed instead of one, and C1, C2, C3 and C4 are parallel with large impedance to make note voltage of switch from floating. Here needs to declare that although capacitor array brings parasitic problem, here it is acceptable to use two.

Except for core, each oscillator output is along with a buffer for overcoming 50 Ohms load and large capacitor, which will degrade Q the tank and change frequency, from output testing condition [15]. In order to drive this load and isolate outside interference, this proposed circuit, which is shown in Fig. 3.3, uses three-stage buffer to enhance the output voltage swing.

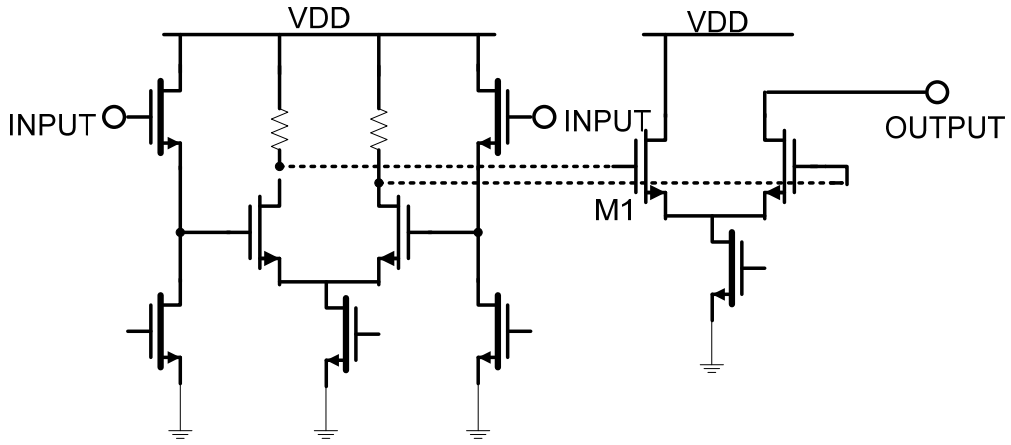


Fig. 3.3. Topology of output buffer.

The first stage uses source follower instead of AC couple, for higher Q purpose. Second stage uses differential pair, and last stage uses open drain structure to increase equivalent load. At the last stage, the inductor is off-chip one which is connected between output and VDD, what's more, this buffer is designed to be single output for testing purpose and in order to make last stage balance, thus the drain of M1 is directly connecting to the VDD.

3.2 Transformer Implementation

This proposed circuit implemented by using 6 layers metal BiCMOS technology, thus it allows that transformer design largely saves inductors area, by utilizing both vertical space and inner space of larger inductors. For better illustration, the concept architecture is shown in Fig. 3.4.

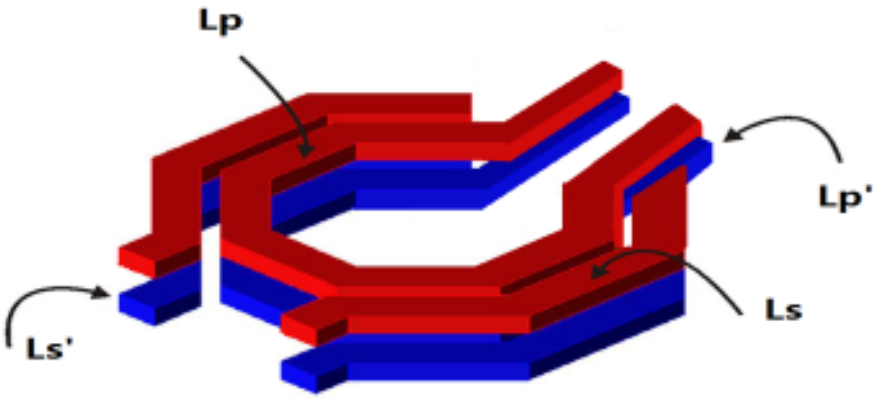
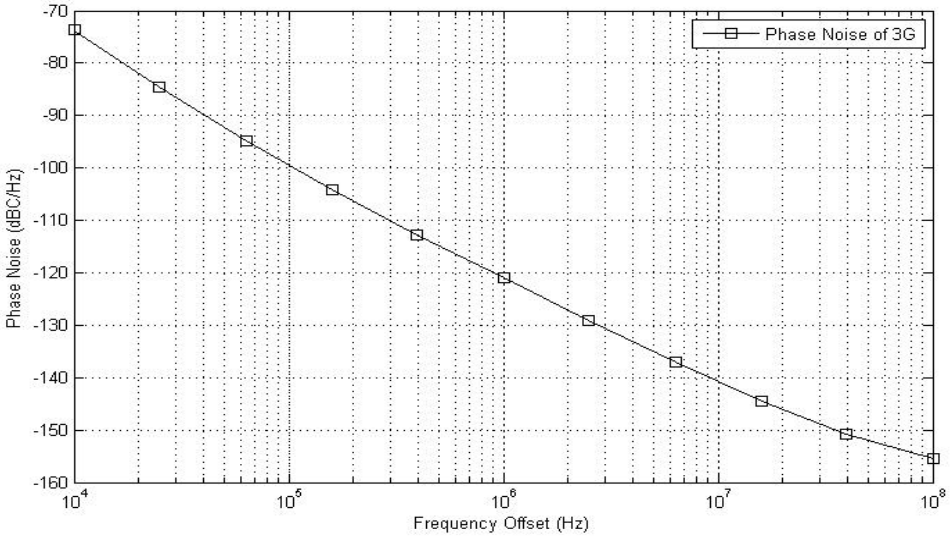


Fig. 3.4. Architecture of proposed transformer.

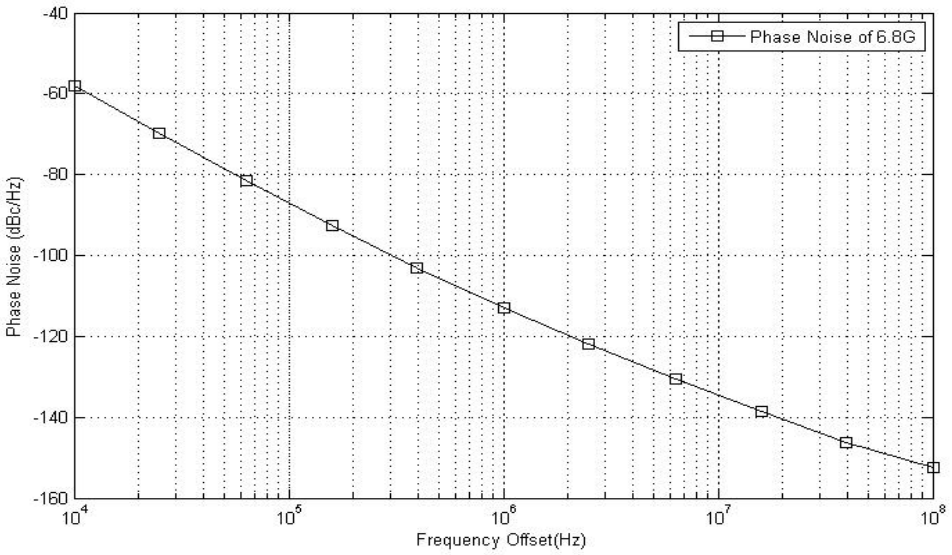
Firstly, the transformer is based on four differential inductors, and Lp are 3 turn coils ,while Ls is only one turn coil, additionally inductors in the same vertical dimension share with the same power tap. Upper inductor Ls, Lp are used by top metal layer (metal 6) which has thickness of 2.92 μm to built coil , and metal 5 is for crossing and under paths of upper inductors. Lower inductor Ls', Lp' are used by metal 3 which has thickness of 0.5μm to built the coil, and metal 2 is used for crossing while metal 4 for under paths. Due to (3.1), Ls' and Lp' have inductance which is six times smaller than Ls and Lp, and this can avoid from over using of mutual inductance, which cause large overlaps frequency. Besides, considering Q analysis based on mutual factors [15], oscillation frequency should be away from each other, thus Lp and Ls are designed to feed two center frequency, which are 3GHz and 6.8GHz.

3.3 Simulated Single Core Performance

The phase noise based on simulation result of core2 and core1's center frequencies are shown in Fig. 3.5(a) and Fig. 3.5(b).



(a)



(b)

Fig. 3.5. (a) Phase noise of the single core2; (b) Phase noise of the single core1.

As shown in simulated result, the phase noise of core1 achieves -113 dBc/Hz @ 1MHz offset, when the center frequency of core1 is 6.8GHz. While the center frequency of core2 is 3GHz, its

phase noise achieves -121 dBc/Hz @ 1MHz offset.

The function of the buffer which connected to the output of core2 was also simulated and shown in Fig. 3.6.

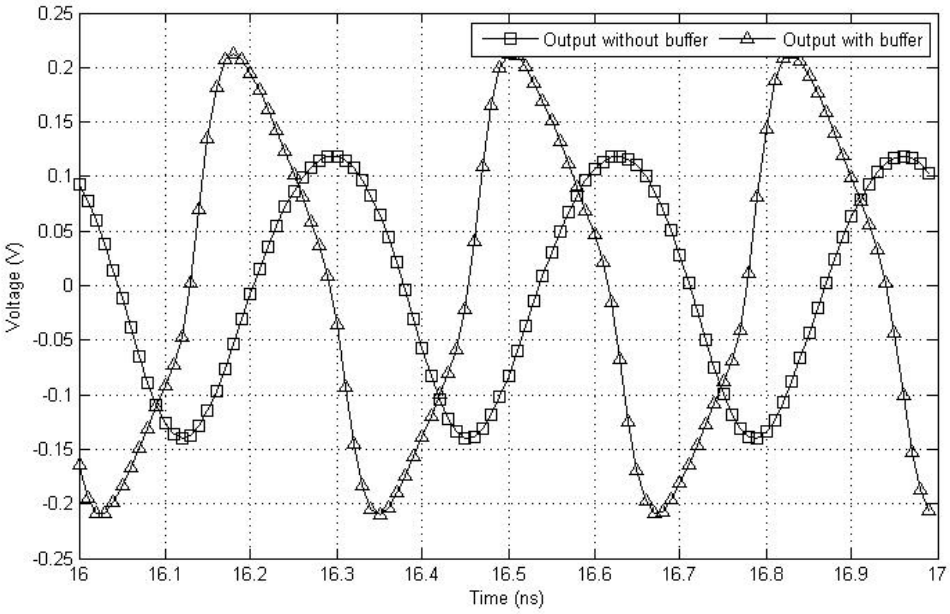


Fig. 3.6. Core2 output with and without output buffer.

From comparison of both waveforms, there can be found that the output signal with buffer have overcome 50 Ohms load and can achieve nearly twice larger voltage full swing than the one without buffer. That is matter because small voltage swing which is nearer to noise floor would affect measure accuracy, and especially for phase noise.

3.4 Frequency Analytical Estimation Based on Transformer

Due to mutual inductance accompanied by current control, this proposed circuit can provide different center frequencies from following status:

Output Core	Mode Condition	Equivalent Inductance
Core1	M Cores working $(M \geq 2)$	$L_{ms,M} = L_s + \sum_{n=0}^{M} \frac{kI_M}{I_s} \sqrt{L_s L_M}$
Core1	Single Core working	$L_{ms,S} = L_s + \sum_{n=0}^{3} \frac{kI_{M'}}{I_s} \sqrt{L_s L_M}$
Core2	M Cores working $(M \geq 2)$	$L_{ml,M} = L_p + \sum_{n=0}^{M} \frac{kI_M}{I_p} \sqrt{L_p L_M}$
Core2	Single Core working	$L_{ml,S} = L_p + \sum_{n=0}^{3} \frac{kI_{M'}}{I_p} \sqrt{L_p L_M}$

Table I. Equivalent inductance of different mode.

where, L_M are corresponding to those opening cores in Multi cores working mode, I_M is corresponding to working current of those cores, and $I_{M'}$ is each core's induced current. Noticing that we make an assumption here, when calculation multi cores equivalent inductance, and that is $I_M >> I_{M'}$. What's more, for more convenient behavior analysis, the product of k and $I_{M'}$ is reformed as $k'I_M$, and k is five times larger than k'.

For how frequencies spread in the spectrum, there plots it in Fig. 3.7 based on above equations. Here needs to be declaring that, the frequency variation plotted in Fig. 3.7 is without any capacitor array techniques, and that's just how center frequency changes with different working mode. For better evaluation, k was split into two value which are k_c=0.6 and k_f=0.5, and k_c represents closer inductor, while k_f represent farer inductors. Additionally, k' is equal to 1/5 k_f.

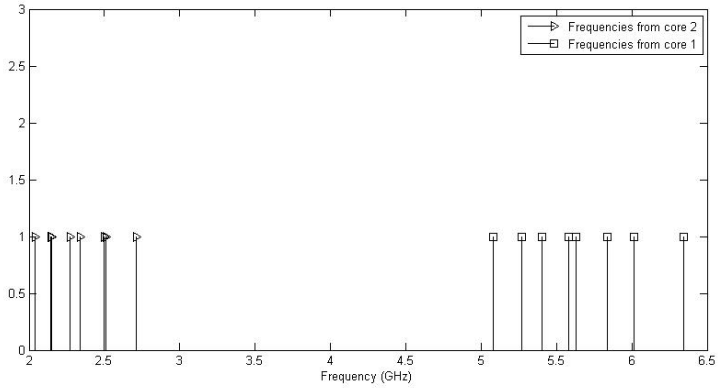


Fig. 3.7. Estimated resonant frequencies distribution under different mode conditions.

From Fig. 3.7, there can be observed that, although all the modes are available, not every mode is necessary, due to there are still some overlapping between frequencies under some mode condition. Thus, some modes are needed to be eliminated. After balancing those distances, the modes which are banned is shown in table II and new plot of frequencies distribution is shown in Fig. 3.8.

Output	Core1	Core2	Core1'	Core2'
Core1	On	Off	On	On
Core2	On	On	On	Off
Core2	On	On	Off	Off
Core2	On	On	Off	On

Table II Mode conditions corresponding to possible overlapped output frequencies.

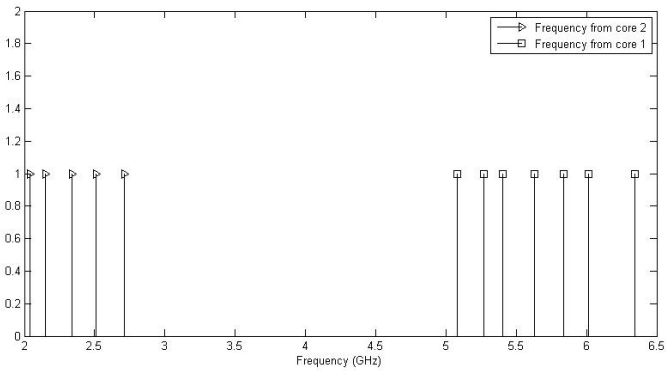


Fig. 3.8. Estimated resonant frequencies distribution without overlapping.

As shown in Fig. 3.8 without using capacitor array technique, there's still large gap between two cores. Fortunately, as considered this problem, this proposed circuit utilized only two set of capacitor array, and the result by using only one array from each core is shown in fig .3.9.

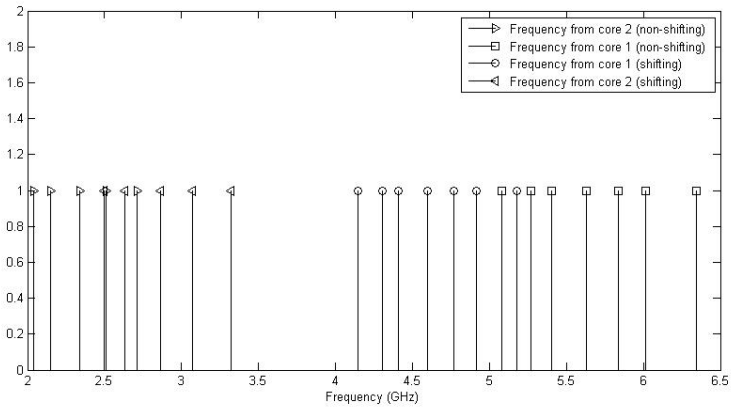


Fig. 3.9. Estimated resonant frequencies distribution by implemented capacitor array.

It is easily found that the gap are largely compensate by one step capacitor array, with further varactor tuning and second capacitor array, it can achieve tuning frequency from 900MHz to 5.6GHz.

3.5 Layout

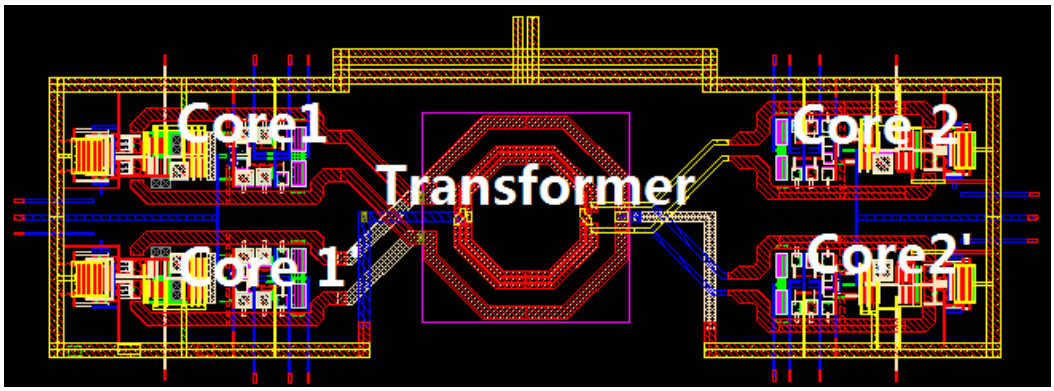


Fig. 3.10. Layout of the proposed VCO.

As shown in Fig 3.10, the whole layout occupied area as 1.875 x 0.665mm^2. Transformer consisted of four inductors is at the center position, and two inductors used top layer are overlapping with other two inductors used lower layers, thus there're only top two can be seen in Fig. 3.10. All the cores are designed in the symmetric structure and position for eliminating parasitic components as large as possible.

Chapter 4

Design of Low Noise Eight-Phase VCO

4.1 Motivation and Architecture

Chapter 2 has introduced some application of quadrature VCO and its requirement, and this chapter will further proposed a multi-phase VCO which is has wider application and more restrict requirement. Since multi-phase clock is increasing demand in RF field, such as, passive mixer in LNA, interleaving in ADC and the performance of VCO will directly affect these applications, to build a multi-phase VCO with low phase noise and high phase accuracy are still two essential specifications for multi-phase signal generation. Multi-phase signals with phase accuracy and no phase ambiguity are critical for passive mixer since they directly affect the turn-on resistance and noise of the complex mixers in LNA. What's more phase error existed in multi-phase signals will add to the error to sampling of ADC and deteriorate the bit error rate (BER) of a communication system. Thus, a high performance multi-phase signal generation technique with both low noise and decent phase accuracy is highly desirable for complex signal modulation and demodulation.

Several method can be applied to generate eight-phase signals, i.e., i) VCO with a eight times higher frequency followed by 6 divide-by-two circuits; ii) ring oscillator;. iii) coupling VCO. The first one is hard to implement, due to it requires high quality VCO with eight times higher frequency than desired one, what's more, those divider are supposed to handle higher frequency and add noise to spectrum. The second type, ring oscillaotr, has very poor phase noise, which can't be used in RF frequency. Comparing to first two, coupling VCO with four cores are easier to implement and has better phase noise. Since this paper used 4 cores to couple, according to coupled oscillator theory [10], VCO itself will bring 1/N phase noise reduction which is 6dB comparing to

single VCO, without considering the noise from coupling devices. One popular multi-phase VCO implementation is coupled with parallel transistors, which has been introduced in chapter 2, due to its simplicity and low cost of area. This coupling technique, however, suffers from a trade-off between phase noise and phase accuracy because the coupling needs to be strong enough to provide decent phase accuracy, which degrades the quality factor of LC tank and phase noise performance, additionally, more power consumption is also needed since large amount of current flowing through parallel transistors. Another implementation is coupled by transformer which can achieve less area and large tuning range, however, such technique is sensitive to the current flowing through inductor of each branch, and resulting large phase error and bad phase noise. What's more, in order to drive transformer, it would cost large amount of power in common case.

Based on above consideration, the single core of eight-phase capacitive coupled VCO (CC-VCO) is shown in Fig. 4.1. This structure is similar to quadrature VCO introduced in chapter 2; however, because that more phases are required and the performance is improved, parameters of those devices have different functions and needed to be redesigned.

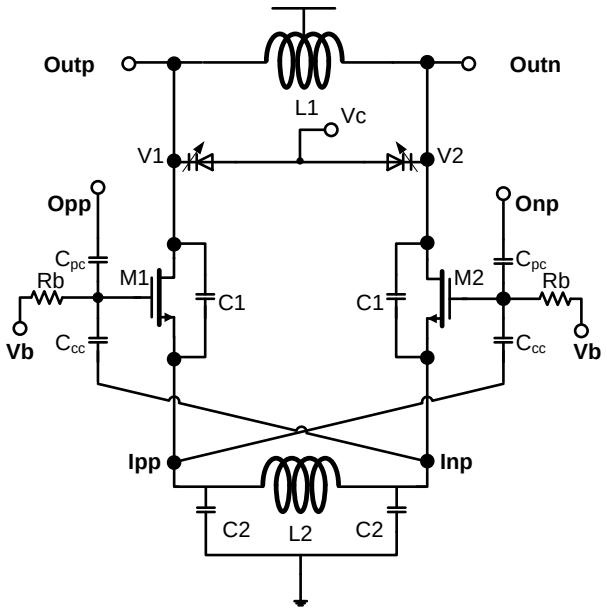


Fig. 4.1. Single Core of Proposed VCO.

As shown in Fig. 4.1, instead of using both noisy transistors and unstable transformer inductors for eight-phase signal coupling, capacitive coupling is employed to improve the phase noise performance of the VCO. In order to get large swing for better phase noise performance under low supply voltage, enhanced swing (ES) Colpitts VCO is employed. C1 and C2 formed Colpitts capacitors, while L2 is differential inductor for large voltage swing. Here needs to be noting that the tank formed by C2 and L2 should have much lower oscillating frequency than the system tank which formed by L1 and C_{tot} should have, due to stable purpose mentioned in [17]. Also, cross couple, which formed by Ccc, is employed to enlarge -Gm for lowering power consumption purpose. Opp and Onp are output coupling signals, and Ipp and Inp are input coupling signals. Their connection will be introduced together with coupling strategy in following section coupled. What's more, Cpc is phase coupling capacitor, which with Ccc defines coupling strength factor m as shown in (4.1), and this factor has the same expression as its in chapter 2, however, due to its different behavior, it is redefines here by using component in Fig. 4.1.

$$m = \frac{C_{pc}}{C_{pc}+C_{cc}} \tag{4.1}$$

4.2 Phase Noise Reduction Technique

Since phase noise reduction is mainly caused by phase shifting, the analysis of this effect will be introduced first. As shown in Fig. 4.1, assuming the transient voltage of coupling signals from one VCO core of four coupling cores as $V_{opp} = V_o \cos(\omega_o t)$ and $V_{inp} = V_o \cos(\omega_o t - 45°)$, the voltage signal at the gate of M1 is:

$$V_{g,M1} = mV_{opp}(t) + (1 - m)V_{inp}(t) \tag{4.2}$$

The voltage waveforms with different coupling-strength factor are illustrated in Fig. 4.2. As it can be seen from the figure, the smaller the coupling strength factor m is, the farther the peak of $V_{g,M1}$ deviate from the zero-crossing of V_{inp} or V_{opp}. Because drain and source voltage of one transistor have the same phase, if gate voltage is maximum during zero-crossing point of either V_{inp} or V_{opp} will cause large amplitude to phase noise conversion, since V_{opp} is also fed into V_{inp} of another coupling core. Thus, gate voltage should be away from both zero-crossing points of V_{inp} and V_{opp}. From (4.2), there can be observed that, if m=0, gate voltage is equals to V_{opp}; if m=1, gate voltage is equals to V_{inp}. Also, m represents coupling strength, there expects that m to be larger than certain level to ensure right phase coupling.

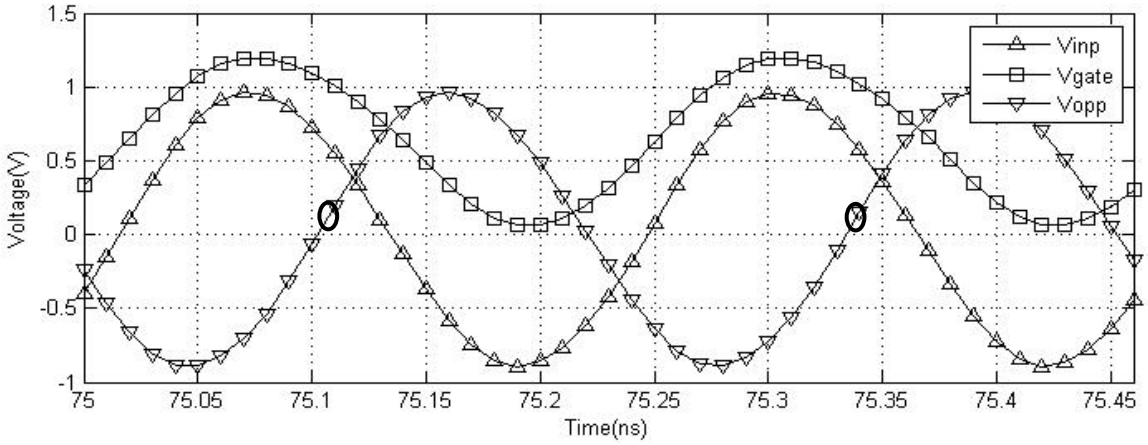


Fig.4.2. (a) Coupling signals for m=0.125.

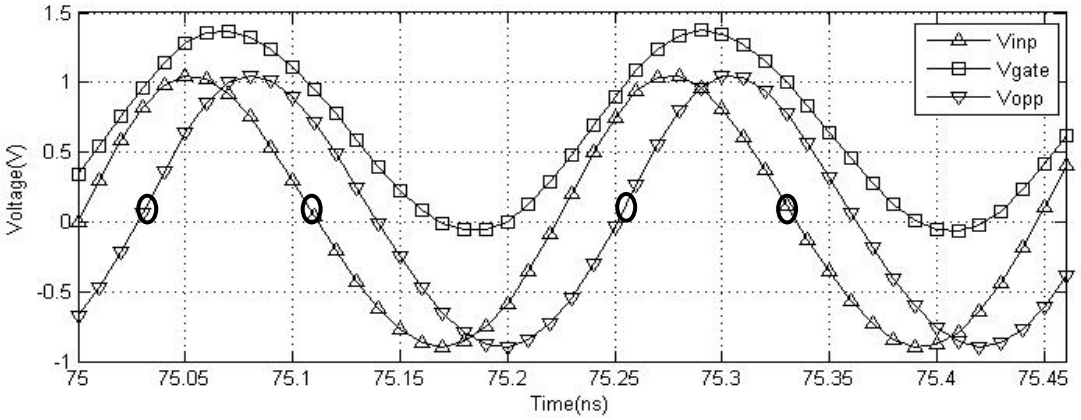


Fig.4.2. (b) Coupling signals for m=0.5.

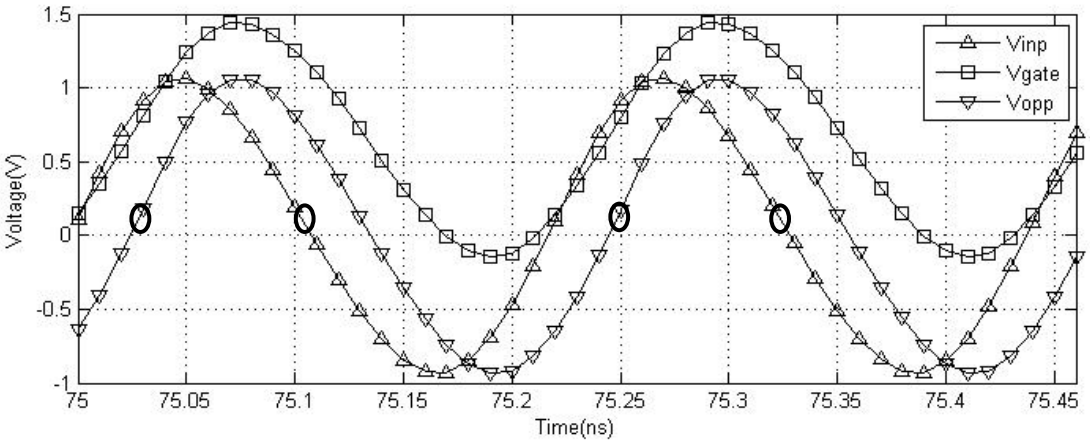


Fig.4.2. (c) Coupling signals for m=0.875.

As shown in Fig. 4.2(a), when m=0.125, the phase ambiguity happens, the coupling strength is weak. Fortunately, to ensure gate voltage deviating from both zero-crossing points, there's no necessary to make m to be that small. When m=0.5, there can get benefit from both coupling and phase noise. That's to say, if m is further approach to 1, the phase noise improvement will disappear. Moreover, eight phase coupling unlike quadrature coupling [11], it has intrinsic advantage in amplitude to phase noise conversion. Because, when gate voltage is in-phase of one coupling signal, it has to be maximum value at crossing point of another coupling signal, however, there's no necessary for eight phase coupling, if coupled in a right way. That's to say, eight phase coupling have larger benefit than quadrature coupling from both aspects of coupling strength and

phase noise. Since, according to ISF, $h_\phi(t,\tau)$ is reduced further under same coupling condition.

In order to predict phase noise improvement, firstly, there obtains noise power from both eight phase and single core transistors. It turns out that each transistor of eight phases contributes noise power of 1.8E-14 V2/Hz, while each transistor of single core contributes noise power of 2E-13 V2/Hz. Thus, there can roughly calculate the noise improvement as

$$C'_{\text{improve}}(\text{dB}) = 10\log\frac{2e^{-15}}{1.8e^{-15}} \approx 10.45 \tag{4.3}$$

In order to further verify phase noise improvement, the ISF of both eight phase and single core are plotted in Fig.3, by using direct measure of impulse response method in [10].

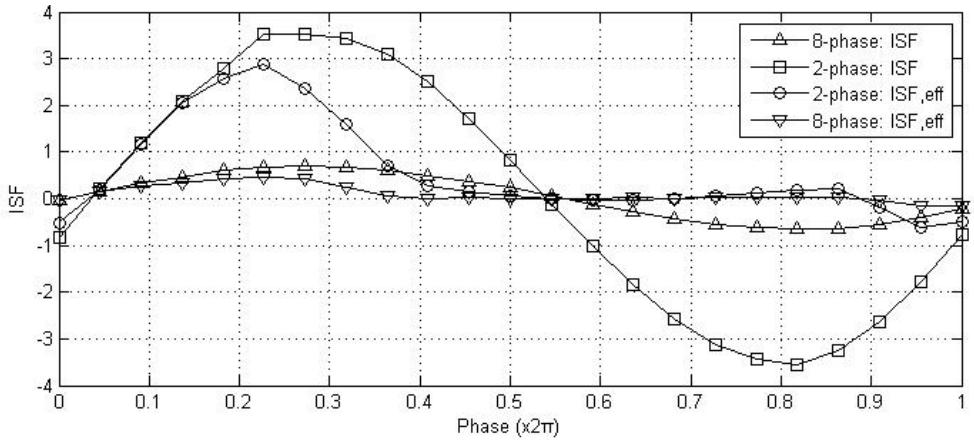


Fig. 4.3. ISF and ISF,eff for both 8-phase and 2-phase.

As it can be seen from Fig. 4.3, both ISF and ISF_{eff} of 8-phase are much smaller than those of 2-phase. By calculating the ratio of corresponding of C0, which is twice dc of ISF_{eff}, there can get phase noise improvement as

$$C_{0,\text{improve}}(\text{dB}) = 20\log 4 \approx 12.04 \tag{4.4}$$

Thus, the phase noise improvement counted from noise summary and ISF_{eff} are closed to each other, which together, proves that 8 phase VCO have better phase noise than single core VCO.

4.3 Multi-phase Generation

Since this capacitor coupling method is different from [11], which is coupled directly at output node, to ensure that eight phases can be right generated in sequence of proposed topology, the relationship between each core should be carefully arranged, or noise and phase ambiguity would be introduced into circuit. Since the relationship between V_{opp} and V_{onp} is 180 degree out phase, so does with V_{inp} and V_{ipp}, V_{opp} and V_{inp}, also with V_{onp} and V_{ipp}, should have 45 degree phase difference. The block diagram and whole circuit connection are shown in Fig. 4.4.

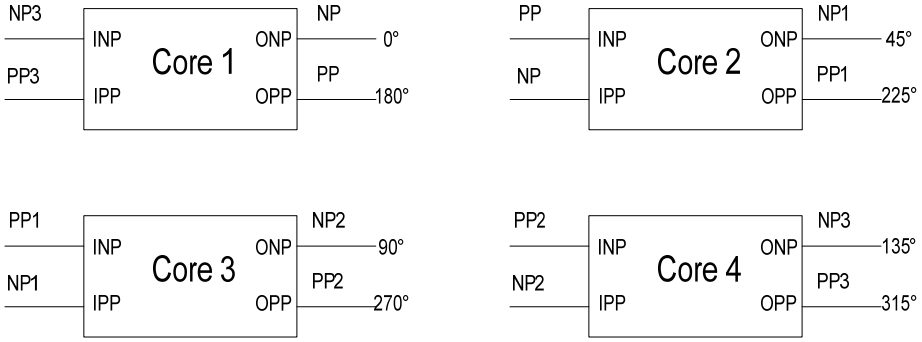


Fig. 4.4. (a) Block diagram of proposed VCO.

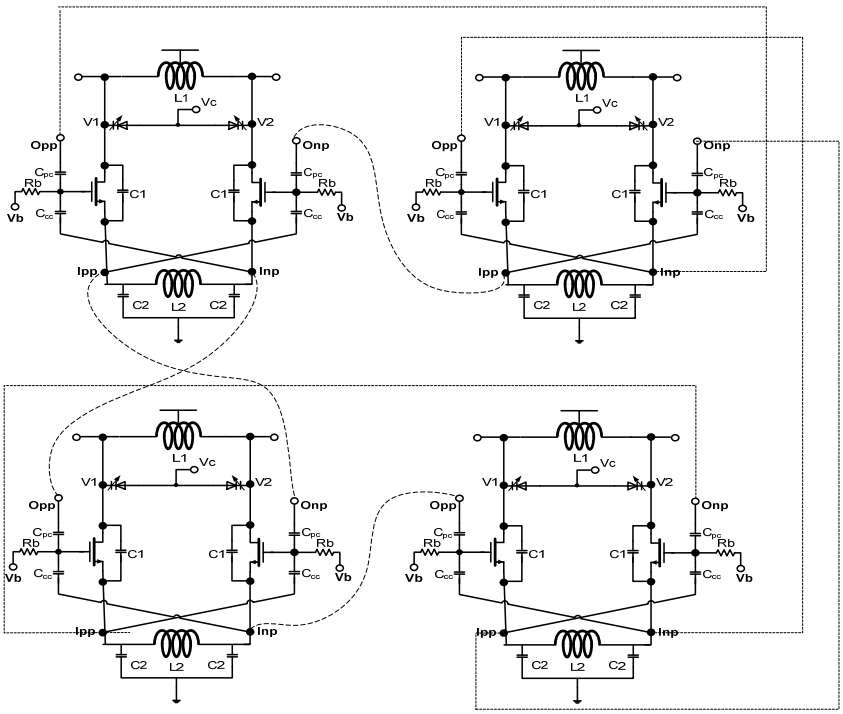


Fig. 4.4. (b) Entire circuit connection of proposed VCO.

Here, coupling strength factor m should be emphasized again, to illustrate how coupling behavior when m is small in Fig. 4.5.:

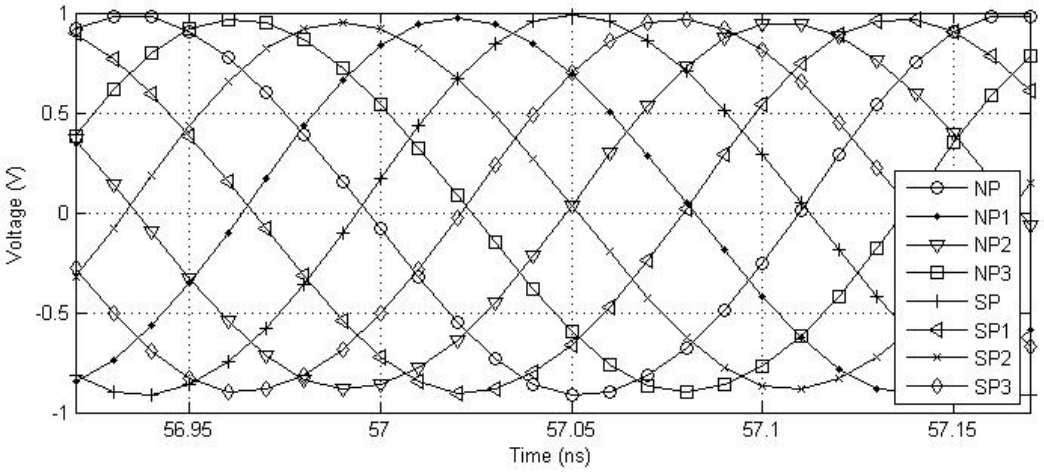


Fig. 4.5. Output signals (m=0.125).

In this case, when m is smaller than 0.2, it will get similar output in Fig. 4.5. As it can be observed that not only ambiguity happens, but also the amplitude of each phase is different from each other, by comparing it with the waveform (Fig. 4.6) whose m is equal to 0.5. Thus, without considering other factor, m should be larger than 2 at least, for coupling purpose.

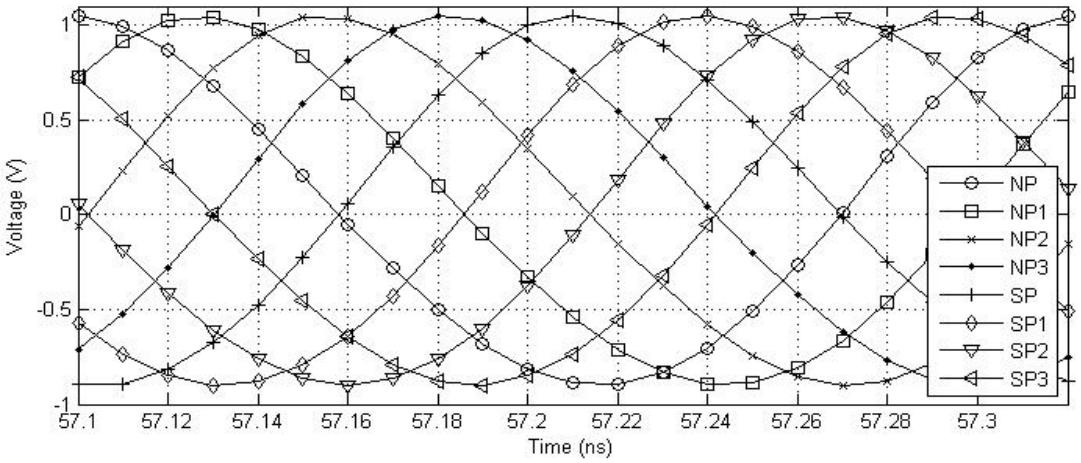


Fig. 4.6. Output signals (m=0.5).

4.4 Simulated Multi-Phase VCO Result

Previous sections have discuss some about coupling strength factor m, and this section will introduce how m affects phase noise, thus the best m factor can be figured out. As it can be seen from Fig. 4.7, phase noise reaches its peak when m equals to 0.5, and this can be explained as maximum voltage moving from zero crossing point of one signal to another zero crossing point, as m from 0 to 1. And, when m=0.5, maximum voltage is far away from both zero crossing point. One thing should be noting that phase improvement is not so obvious comparing to QCC-VCO [11], as m changing, in Fig. 8. This is because the phase different two coupling signals are not 90 degrees, but 45 degrees. That's to say the maximum gate voltage would cross neither of those two signals at zero point. Thus, this intrinsic advantage has already improved phase noise to a certain level. From this aspect, it allows m be little larger than optimum phase noise point for gaining less phase error, as phase noise is relatively stable as m changes. Finally, it provides less trade-off relationship between phase noise and phase error.

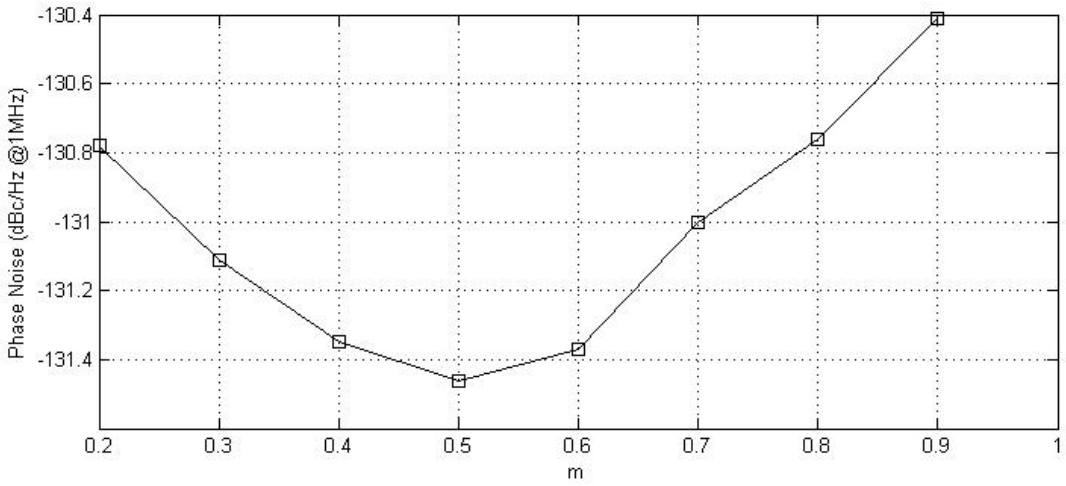


Fig. 4.7. Phase noise with different m.

According to the selection of m, here the simulation result of phase noise when m=0.5, is plotted and shown in Fig. 4.8., and it illustrates that phase noise, when frequency is 4.8GHz, is

-131.7 dBc/Hz @1MHz offset, while 8-phase noise is -122.3 dBc/Hz @1MHz offset, which is 9.4 dB phase noise improvement. This result quite fits the phase noise improvement of both noise summary and calculation from ISF_{eff} which have been analyzed in previous section. This states that 4 core accomplished 6dB phase noise improvement according to coupled oscillator theory [10], and the phase noise improvement beyond 6dB is caused by phase shifting which illustrated in IS_{Feff} in Fig. 4.3.

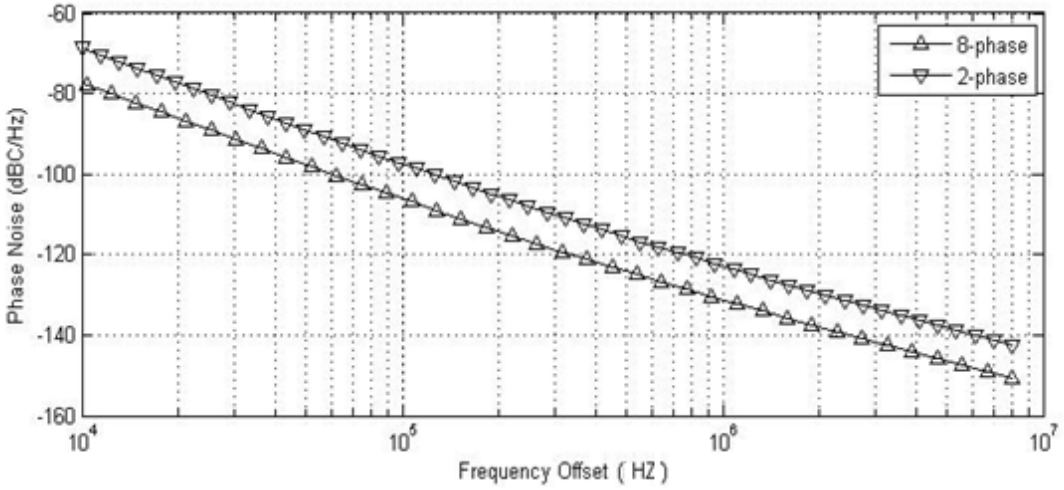


Fig. 4.8. Simulation result of phase noise.

Chapter 5

Conclusions

Two structures are proposed in this thesis for different application. Both circuits are implemented based on a 0.18 μm BiCMOS technology. The first transformer based quad-band VCO can generate two center frequencies as 3.1 GHz and 6.8 GHz with 30 percent tuning range. With mutual effect which is consists of four inductors and can be control by current of auxiliary cores, the tuning range will widely increase without introducing numbers of parasitic components and achieve better phase noise, and release the pressure from varactor.

The second 0.85-V eight-phase capacitive coupling voltage-controlled oscillator (CCVCO) with enhanced swing for low power supply applications can even achieve 9.4 dB lower phase noise than its single-phase counterpart at 1-MHz offset. Optimized capacitive coupling combined with source inductive enhance-swing technique enables low power and low phase noise simultaneously. The proposed VCO achieves a simulated phase noise of -131.7dBc/Hz @ 1-MHz offset with a center frequency of 4.8 GHz and consumes 80 mW from a 0.85-V supply. Also, based on simulation analysis, the proposed 8-phase VCO has intrinsic advantage for reducing ISF comparing to quadrature CC-VCO. This allows that proposed VCO can have better phase noise with larger coupling strength.

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