Design of Low-Voltage Broadband Folded Blixer for SDR Application

by

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Abstract

Recent years, a large number of researches have been made on the software-defined radio (SDR) architectures. SDR is radio communication systems where typical functions have been implemented in hardware (e.g. mixers, filters, amplifiers, modulators/demodulators, detectors, etc.) are replaced by processing of software on a computer or embedded system [1].

A basic SDR system will consists of an analog-to-digital converter, preceded by a so called RF (radio frequency) front end. Large amounts of signals will be processed by the software processor instead of being handled in special designed hardware. Such architectures raises requirement for a very broad bandwidth even UWB (ultra-wideband) processed by a single receiver front end, covering the frequency range from hundreds MHZ to several or even tens of GHz [2]-[4]. However, the demands for linearity, noise figure or voltage gain still exists, making the requirement of broadband an even challenging topic.

In this paper, a new structure for SDR front end application will be proposed. With balun LNA (low noise amplifier) combined with a folded mixer, the new structure will deal with a very wide input signal bandwidth ranging from 500 MHz to 6 GHZ and output directly at IF band from 5MHz to 300MHz. Design and topologies are chosen to best meet the input matching lower than -10 dB; overall font end noise figure lower than 8 dB; voltage gain as high as 25 dB.

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List of Abbreviations

SDR	Software Defined Radio
UWB	Ultra Wide Band
CE	Common Emitter
CB	Common Base
CS	Common Source
CG	Common Gate
LNA	Low Noise Amplifier
Blixer	Balun LNA with Mixer

Chapter 1 Introduction

1.1 Background and Motivation

Recent years, a large number of researches have been made on the SDR architectures. SDR is radio communication systems where typical functions have been implemented in hardware (e.g. mixers, filters, amplifiers, modulators/demodulators, detectors, etc.) are replaced by processing of software on a computer or embedded system [1].

A basic SDR system will consists of an analog-to-digital converter, preceded by a so called RF front end. Large amounts of signals will be processed by the software processor instead of being handled in special designed hardware. Such an architecture raises requirement for a very broad bandwidth even ultra-wideband processed by a single receiver front end, covering the frequency range from hundreds MHZ to several or even tens of GHz [2]-[4]. However, the demands for linearity, noise figure or voltage gain still exists, making the requirement of broadband an even challenging topic.

While broadband balun is one of the methods used for bandwidth extension, considering its huge losses, a single-ended RF input is more suitable for application which avoids using more switches between RF input and different RF filters or antenna networks.

In this paper, a new structure for SDR front end application will be proposed that has very low power consumption. With balun LNA combined with a folded mixer, the new structure deals with a very wide input signal bandwidth ranging from 500 MHz to 6 GHZ and output directly at IF band from 5MHz to 300MHz. Design and topologies are chosen to best meet the input matching lower than -10 dB; overall font end noise figure lower than 8 dB; voltage gain as high as 25 dB.

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1.2 Organization of the Thesis

The thesis has been organized to provide a complete discussion over the wideband RF front end techniques and architectures. Chapter 2 goes over basic and previous work on LNA and Mixer design. Different topology of RF front end has been compared with each other. Chapter 3 proposes the design of the low voltage merged RF front end with mathematical analysis and simulation results. Chapter 4 draws conclusion for the design.

Chapter 2 Previous Work on RF Front-end Design

2.1 Noise Analysis and Comparison of Basic Amplifier for LNA Design

2.1.1 Basic Bipolar Amplifiers

In the basic LNA design, there are three types of amplifier that can be used: CE (Common-Emitter) Amplifier, which is often used as a drive for an LNA for its high input impedance; CC (Common-collector) amplifier, with high input impedance and low output impedance, which can be used to make an excellent buffer between stages or before the output driver; CB (Common-base) amplifier, which is often used as a cascade in combination with the common-emitter to form a LNA stage with gain to high frequency.

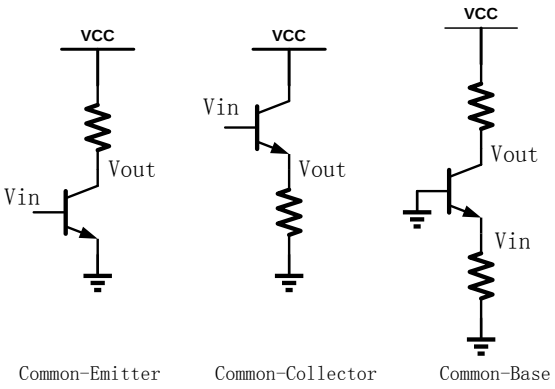

Figure. 2.1. Basic amplifiers in LNA design.

A. Common-Emitter Amplifier

1. Voltage Gain

The voltage gain of the CE amplifier can be calculated as:

$$A_{vo} = \frac{V_o}{V_i} = -\frac{r_\pi}{r_b + r_\pi} g_m Z_L \approx \frac{Z_L}{r_e} \tag{2.1}$$

Where $r_\pi = \beta r_e$, $r_e = \frac{1}{g_m}$ .For low frequencies, the parasitic capacitances can be ignored

and $r_b \ll r_\pi$. The input impedance at low frequencies can be expressed as:

$$Z_{in} = r_b + r_\pi \tag{2.2}$$

From equation 2.1 and 2.2, we can see that, by setting different load resistance, the CE amplifier can have a moderated gain with high input impedance at low frequency. However, the voltage gain performance under relatively high frequency will be affected by the Miller capacitor and drop as frequency increases.

2. High Frequency Response

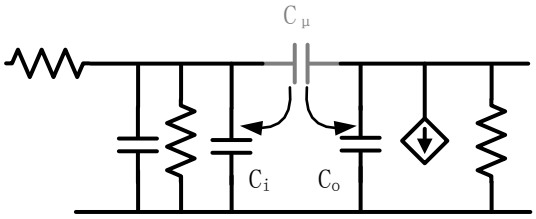

Figure. 2.2. The Miller capacitor equivalent circuit in bipolar transistor.

Figure 2.2 shows the Miller capacitor C_μ in the bipolar transistor. In order to study the effect of this capacitor in high frequency, we split C_μ into two separate capacitors at input C_i and at output C_o, where:

$$C_i = C_\mu\left(1 - \frac{V_o}{V_\pi}\right) = C_\mu(1 + g_m Z_L) \approx C_\mu g_m Z_L \tag{2.3}$$

$$C_o = C_\mu\left(1 - \frac{V_\pi}{V_o}\right) = C_\mu(1 + \frac{1}{g_m Z_L}) \approx C_u \tag{2.4}$$

Therefore, two poles can be observed at the high frequency response of the CE amplifier. The dominant pole is the one formed by C_A and C_π, and can be calculated as:

$$f_P = \frac{1}{2\pi[(r_b + R_s)]\cdot(C_\pi + C_i)} \tag{2.5}$$

This is pretty critical in Wideband LNA design because C_u is going to be directly multiple by

voltage gain when calculating C_i, this equation indicates the as the bandwidth of the amplifier becomes wider and wider, the voltage gain will drop as frequency goes higher as a result. There always exists tradeoff between bandwidth and high voltage gain.

3. Input Impedance and Noise Figure for Common-Emitter LNA

As LNA are typically designed to provide a 50 ohm input resistance and negligible reactance. This requirement limits the choice of LNA topologies. As we can see from equation 2.2, the CE amplifier is obviously not with 50 ohm pure resistance when at low frequency.

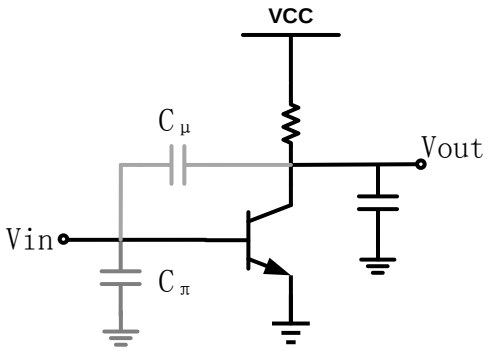

Figure. 2.3. Input impedance for CE Amplifier.

As depicted in figure 2.3, according to equation 2.2 and 2.3, the impedance in a CE amplifier can be expressed as:

$$Z_{in,CE} = r_\pi || C_\pi || C_i || + r_b$$

$$= r_\pi || C_\pi || C_\mu g_m Z_L || + r_b$$

$$= r_\pi || (C_\pi + C_\mu g_m Z_L) + r_b \quad (2.6)$$

As we can see from equation 2.6, the input impedance of the CE amplifier is an function of frequency. For input matching, we should make the real part to 50 ohm and cancel the imaginary part. For one way, we could put a resistor at the input of the gate and put another inductor to

cancel the imaginary impedance(figure 2.4).

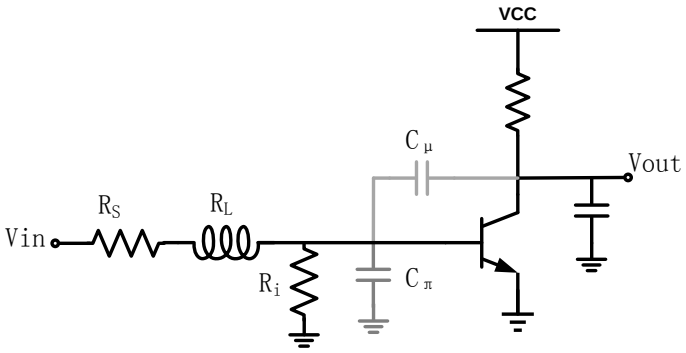

Figure. 2.4 Resistor and inductor input matching.

In order to deal with the capacitive part of the input impedance looking into the base, a series inductor has been connect to the input (like In figure 2.4) to offer a positive imaginary impedance under certain fixed frequency to cancel the negative imaginary part.

An paralleled resistor values around 50 ohm will also be added to the input, which will paralleled with big base impedance of the amplifier and make the total impedance around 50 ohm cause it is far smaller than the other component.

Assume under the input matching condition, the total output noise figure will be:

$$\overline{V_{n,out}^2} = 4kT(R_s||R_i)(g_m R_L)^2 + 2kTg_m R_L^2 + 4kTR_L \qquad (2.7)$$

Then the noise figure is given by:

$$NF = 1 + \frac{R_S}{R_i} + \frac{1}{2}\frac{R_s}{g_m(R_s||R_i)^2} + \frac{R_S}{g_m^2(R_S||R_i)^2 R_L} \qquad (2.8)$$

For input matching , the Ri should equle to Rs, therefore, the noise figure will 3 dB under ideal conditon.

Another method is to use the existence of C_μ , which will bring the characteristic of the load into the input and therefore it is possible to properly select the value of L and C so as to obtain 50

ohm input impedance.

All of the method, however, requires accurate value of LC and the matching condition and is only applicable under narrow band LNA design. This will limit the flexibility when one is going to change the gain or output matching. On other hand, the NF of this circuit will still be higher than 3 dB.

For avoiding repeat of the content, detailed noise analysis of an common-emitter bipolar amplifier will instead be decribed in chapter 3.

B. Common-base Amplifier

The most important advantage of the Common-Base amplifier over common-emitter amplifier is its low input impedance. As we know that, the input impedance seeing from the source of the amplifier is decided by $1/g_m$. Therefore, it will be very easy to do an input matching by setting proper g_m. Such a property makes it very suitable for wide band LNA application.

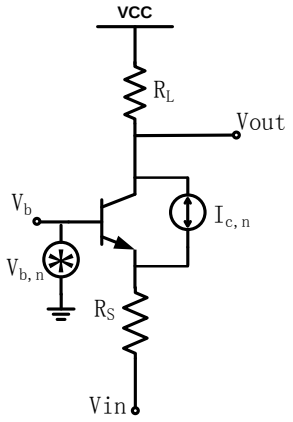

Figure. 2.5. Input impedance and noise for CB amplifier.

For input matching, we set $Rs=1/g_m$. The total noise at the output is given by:

$$\overline{V_{n,out}^2} = \left(\frac{2kT}{g_m} + 4kTr_b\right)\left(\frac{g_m R_L}{1+g_m R_s}\right)^2 + 4kTR_L$$

$$= \frac{1}{2}kT\frac{R_L^2}{R_S} + 2kTr_b R_L g_m + 4kTR_L \qquad (2.9)$$

Therefore, the noise figure can be calculated as:

$$F = 1 + \frac{1}{2g_m R_s} + \frac{R_S}{R_1} + \left(1 + \frac{1}{g_m R_S}\right)^2 + \frac{r_b}{R_s} = \frac{3}{2} + 4\frac{R_S}{R_L} + \frac{r_b}{R_s} \qquad (2.10)$$

Equation above indicates that it is still very difficult to make the NF reaches a level way than 3 dB .

2.2 Noise Cancellation Techonology for LNA Design

Based on all the analysis of basic LNA amplifier, we can find that no matter CE or CS amplifier we use, it is very difficult to meet the requirement for noise figure lower than 3 dB . Therefore, noise cancellation technology was proposed recent years to further improve the noise performance of LNA.

2.2.1 Cross-Coupled Noise Cancellation LNA Topology [3]

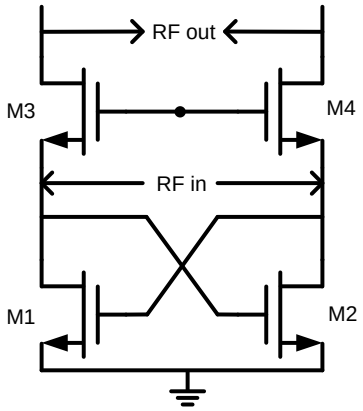

Figure. 2.6. Cross-Coupled LNA topology.

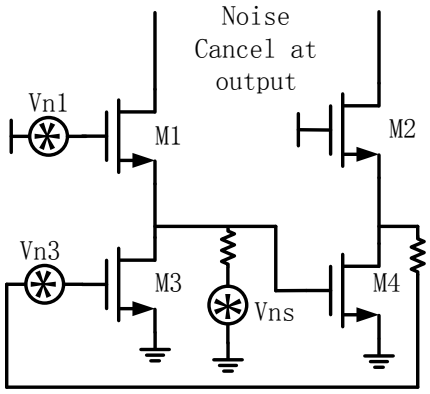

Figure. 2.7. The noise cancellation mechanism.

A. Input matching

Figure 2.7 shows the basic topology for cross couple LNA. The main transistor M3 and M4 will be used as signal amplifier with a differential (input) output while M1 and M2 serves as noise cancellation branch. The input impedance is given by:

$$R_{in} = \frac{2}{g_{m1} - g_{m3}} \tag{2.11}$$

The denominator is the transconductance of transistors M1 and M3. For input power matching condition:

$$R_s = \frac{R_{in}}{2} = \frac{1}{g_{m1} - g_{m3}} \tag{2.12}$$

B. Noise Cancellation

The noise cancellation mechanism can be analyzed by a simplified circuit in figure 9. For the left half part, assume three noise source is going to appear at the output:

$$v_{ns}^2 = 4KTR_S$$

$$v_{n1}^2 = \frac{4KT\gamma_1}{\alpha_1 g_{m1}}$$

$$v_{n3}^2 = \frac{4KT\gamma_3}{\partial_3 g_{m3}} \tag{2.13}$$

Among all the three noise sources, the noise coming from the source and M3 will be separately amplified through M1 and M2 and form a noise voltage at the load with opposite directions. While at the same time, the output noise coming from M1 can be treated as common-mode signals and therefore are cancelled partially with each other. Overall, the noise factor is given by:

$$F = 1 + \frac{\gamma}{\alpha}\left[\frac{(g_{m1}R_S - 2)^2}{g_{m1}R_S} + g_{m1}R_S - 1\right] \tag{2.14}$$

C. Limitation

One limitation of this system is that, only part of the noise coming from M1 and M2 can be cancelled, however, at the same time, M3, M4 will also introduce noise, being amplified as differential output which cannot be cancelled.

On the other hand, since input impedance only decided by the transconductance of M1 and M3, it can provide very wide band input matching at the cost of a super wide band balun for of its differential input. This is because practical input of an antenna in real life is all single-ended and there is no good wideband balun considering its loss and bandwidth.

2.2.2 Feed Forward Noise Cancellation Technology [5]

A. Common-Source Amplifier with Shunt Feedback

The feed forward noise techonology is based on an CS amplifier with shunt feedback. Let's first review the properpitis of an feedback amplifier.

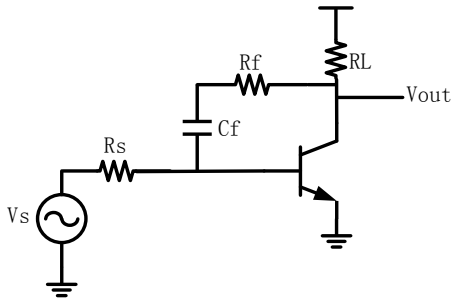

Figure. 2.8. Shunt feedback CS amplifier.

Figure 2.8 depicts the basic topology of a common-source amplifier. The capacitor C_f is used to isolate bias and will be set way larger over frequency of interest. If ignore C_μ , the gain is given by:

$$A_v = \frac{V_o}{V_i} = \frac{\frac{R_L}{R_f} - g_m R_L}{1+\frac{R_L}{R_f}} \approx \frac{-g_m R_L}{1+\frac{R_L}{R_f}} \tag{2.15}$$

The input impedance is equal to $R_f + R_L$ divided by the open loop gain:

$$Z_{in} = \frac{R_f+R_L}{A_{v,open}} \approx R_f || \frac{(R_f+R_L)}{g_m R_L} \approx \frac{(R_f+R_L)}{g_m R_L} \tag{2.16}$$

As we can see, the input impedance will be dominated by the feedback resistor therefore will be much better for wideband matching. However, like many other single stage amplifier, its noise figure is still higher than 3 dB.

B. Forward Noise Cancellation Technology

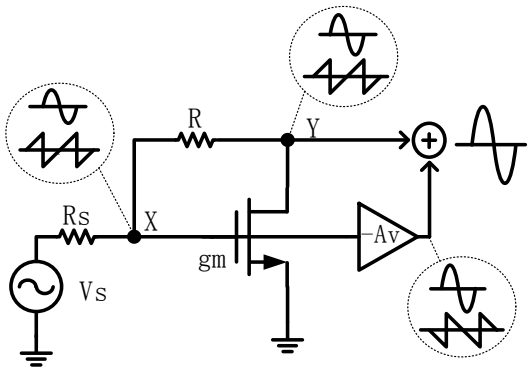

Figure. 2.9. Forward noise cancellation topology.

Figure 2.9 illustrate the basic idea of this noise canceling technology. Let us assume that the feedback resistor is way smaller than the load resistor. Therefore the input impedance from equation 2.16 will become $Z_{in} = 1/g_m$. The noise of the MOSFET can be expressed by a noise current I_n flow from its source to source. Depending on the relation between the input impedance and Rs, a certain ratio of I_n will flow out of the matching MOSFET through R and R_S, creating two noise voltage at nodes X and Y with equal sign and phase. On the other hand, the signal at node X and Y will have opposite sign for the amplifier's negative gain. By adding a new negative amplify branch from node X and sum it back to the original output, the noise of the MOSFET can be cancelled while on the other hand double the output. Under ideal condition, a proper scaling negative Av stage will produce exactly the same anti-phase noise and same phase of signal.

If under input matching condition and the noise of the main MOSFET can be cancelled, the noise at the output can be calculated as:

$$F_{min} = 1 + \frac{R_s}{R} + \frac{NEF}{g_{m2}}\left(\frac{1}{R_s} + \frac{3}{R} + \frac{2R_S}{R^2}\right) \qquad (2.17)$$

As we can see from the equation, proper value of R and g_{m2}will give a NF lower than 2dB.

C. Bandwidth Limitation

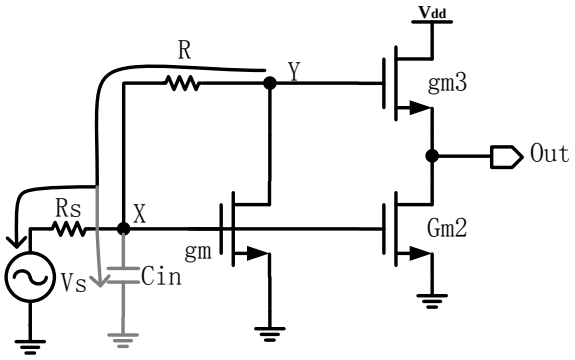

Figure. 2.10. Bandwidth affected by input capacitor.

As the noise voltage appear at node X is heavily depend on the relation between Z_{in} and R, as the frequency increases to a higher level , the impedance Z_{in} will no longer be $1/g_{m,}$ due to the input cap of MOSFET, Miller Effect and the changing of feedback property, the noise sensed at node X will varies from the original one. Since the voltage gain of cancellation stage is pre-decided and the gain of the cancellation stage decrease with frequency as well, the noise cancellation effect is going to degrade dramatically when the frequency is higher than 1 GHZ or 2GHZ. For a super wideband LNA, the bandwidth of this topology is not enough.

2.2.3 Single-End Balun-LNA Topology [6]

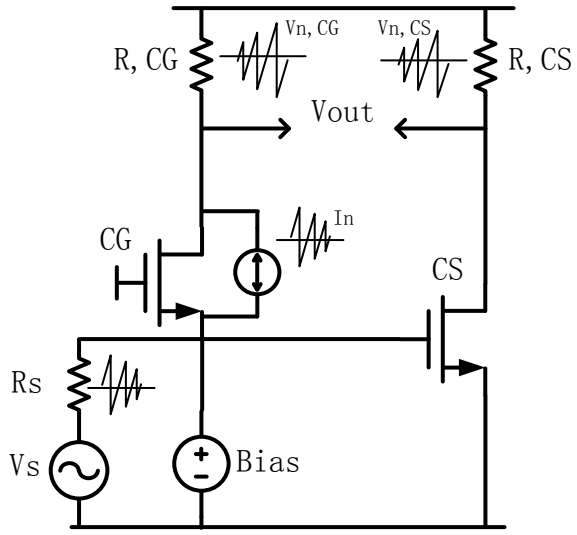

Figure. 2.11. The single-ended balun LNA topology.

Figure 2.11 is the basic topology of the Balun-LNA. The noise cancellation idea is very similar to the previously mentioned forward feedback LNA. The noise generated by the CG transistor can be represented by a noise current i_n. The current is going to flow toward the input through the CG transistor and R_S, generating a noise voltage $V_{n,in}$ at the input and an anti-phase noise voltage $V_{n,CG}$ at the load. The voltage appears at the input node will be sensed by a

common-source amplifier simultaneously and cancel at the differential output.

The noise voltage appears at the input is also depend on the ratio of $1/g_m$ and Rs. However, recall that the input impedance of the common-gate amplifier is decided by $1/g_m$, this property can be hold by a much wider frequency bandwidth than that of a shunt feedback CS stage since the f_T of the CG amplifier is normally much higher. In another words, the bandwidth of this topology is much wider than the shunt one. The NF of the system is given by:

$$F = 1 + \frac{\gamma g_{m,CG}\left(R_{CG} - R_S g_{m,cs} R_{CS}\right)^2}{R_S \cdot A_v^2}$$

$$+ \frac{\gamma g_{m,CG} R_{CS}^2 \left(1 + g_{m,CG} R_S\right)^2}{R_S \cdot A_v^2}$$

$$+ \frac{(R_{CG}+R_{CS})\cdot(1+g_{m,CG}R_S)^2}{R_S \cdot A_v^2} \qquad (2.18)$$

Under matching condition, assume the noise of the CG stage can be totally cancelled. The total output noise will be dominated by that of the CS stage. Therefore, the size of the common-gate transistor will be 3-4 times bigger than the CB one to minimize its noise contribution.

Though the noise cancellation effect will also degrade as the voltage gain of both CG and CS amplifier varies at high frequency, the balance is going to be hold for wide enough bandwidth for SDR application. This structure has been borrowed by the “Blixer” in this work. Detailed analysis will be in chapter 3.

2.3 Analysis of Passive and Active Mixer

Mixers can be generally categorized into ‘’passive” and “active” topoligies, as this topic is

going to merge the LNA with a mixer. It is necessary to go througn the basic two types of mixers.

2.3.1 Passive Mixer Analysis

Mixer is basicly an switch drived by the local ocilator signal (LO). The process that the input RF signal go through the switch can be treated as the mutilicity of two signals. The donimated two output signal will located at $|\omega_c \pm \omega_L|$. The chosen of low or high frequency output decided whether its an down-conversion or an up-conversion mixer.

A. Basic Topologies

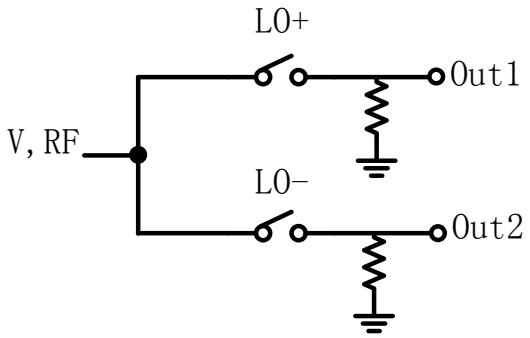

Figure. 2.12. Single balanced passive mixer.

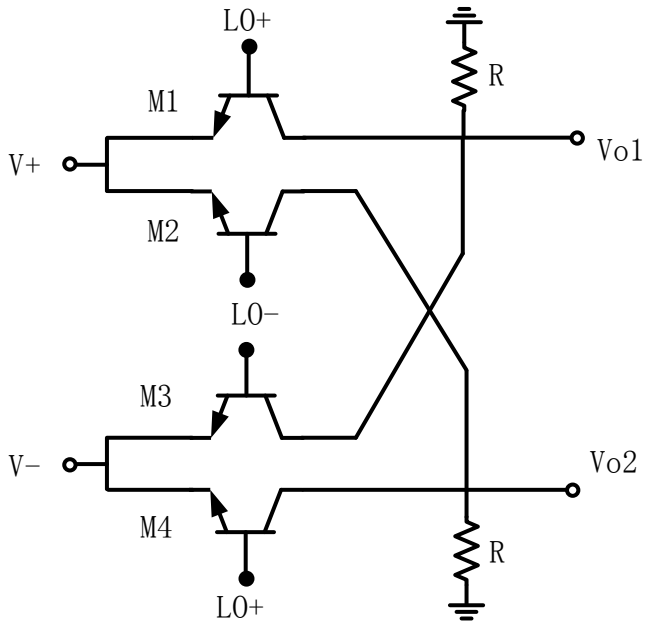

Figure. 2.13. Double balanced passive mixer.

Figure 2.12 and 2.13 shows the basic topology of a single and double balanced passive mixer. Such topology is called “passive” because their transistors do not operate as an amplifying device.

B. Properties of Passive Mixer

1. Conversion Gain

The output of a mixer waveform can be decomposed into two parts. One y1(t) is equal to the sampled signal when the switch in on while another y2(2), is equal to the voltage stored on the capacitor when switch is off. Assume the input can be represented as x(t), then y1(t) and y2(t) can be given by[8]:

$$Y_1(f) = \frac{X(f-f_{LO})}{j\pi} - \frac{X(f+f_{LO})}{j\pi} \tag{2.19}$$

$$Y_2(f) == \frac{-X(f-f_{LO})-X(f+f_{LO})}{2} \tag{2.20}$$

Therefore, the total output of the mixer is given by:

$$|Y_1(f) + Y_2(f)| = \sqrt{\frac{1}{\pi^2} + \frac{1}{4}}[X(f - f_{LO}) + X(f + f_{Lo})] \tag{2.21}$$

For a non-return to zero mixers, the ideal gain would be 1.48dB. However, since the leakage of stored voltage or parasitic caps of the switch, the gain is usually lower than this value, for many case it’s often lower than zero.

2. Noise

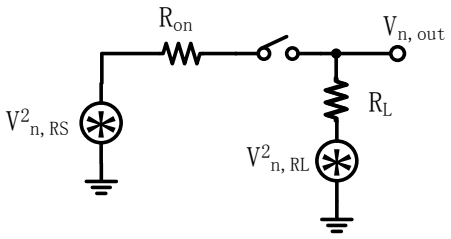

Figure. 2.14. Noise model for passive mixer.

As shown in figure 2.14, assume 50 duty cycle of the LO with half time of the switch being off, the noise at the output of the return-to-zero mixer can be given by:

$$\overline{V_{n,out}^2} = 2kT[(\frac{R_{on}R_L}{R_{on}+R_L}) + R_L] \tag{2.22}$$

We should note that, unlike the resistor noise at the output of a LNA, since there is no gain for the passive mixer, all of this noise will be added to the input without degrading. So the noise of a passive mixer is usually much higher than an active one.

2.3.2 Active Mixer Analysis

A. Basic Topologies

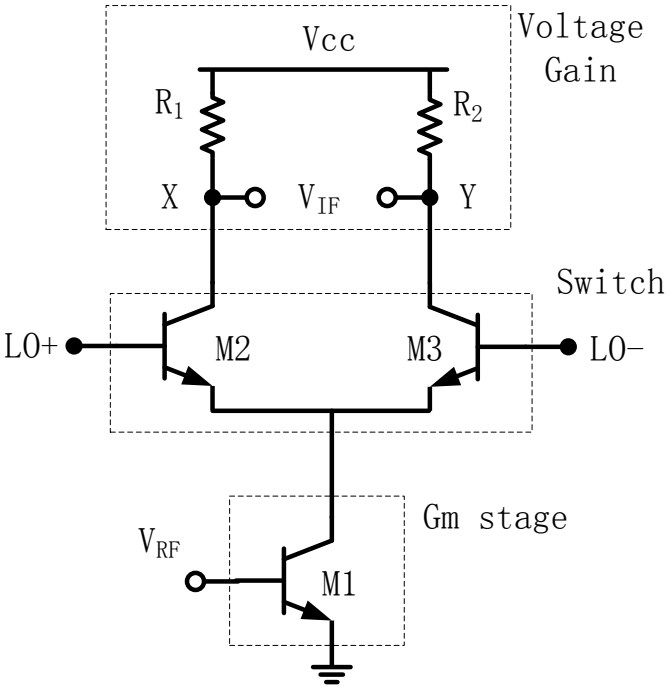

Figure. 2.15. Single balanced active mixers.

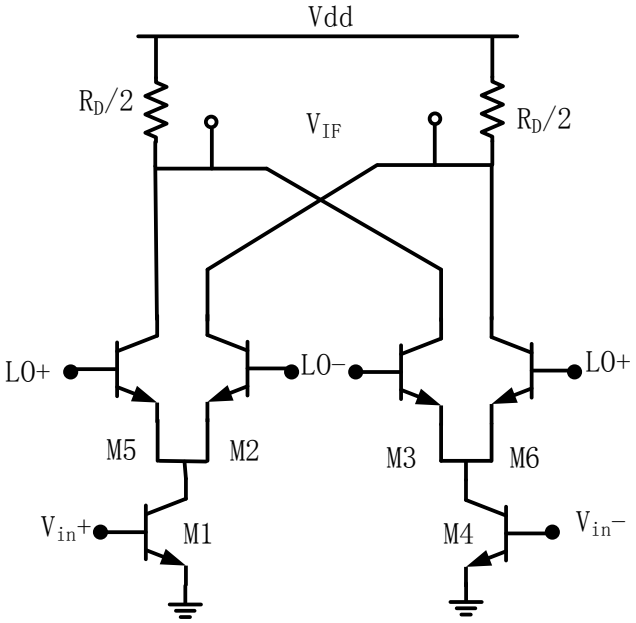

Figure. 2.16. Double balanced active mixers.

Figure 2.15 and 2.16 shows the basic topology for a single and double balanced Active Mixer. Instead of going through the switch stage (M2, M3, M5, and M6) directly, the input signal will be converted to amplified current by a transconductance stage (M1, M4). The switches than will steer the current and convert it into lower IF at the load band and thereby achieve gain.

B. Properties of Active Mixers

1. Conversion gain

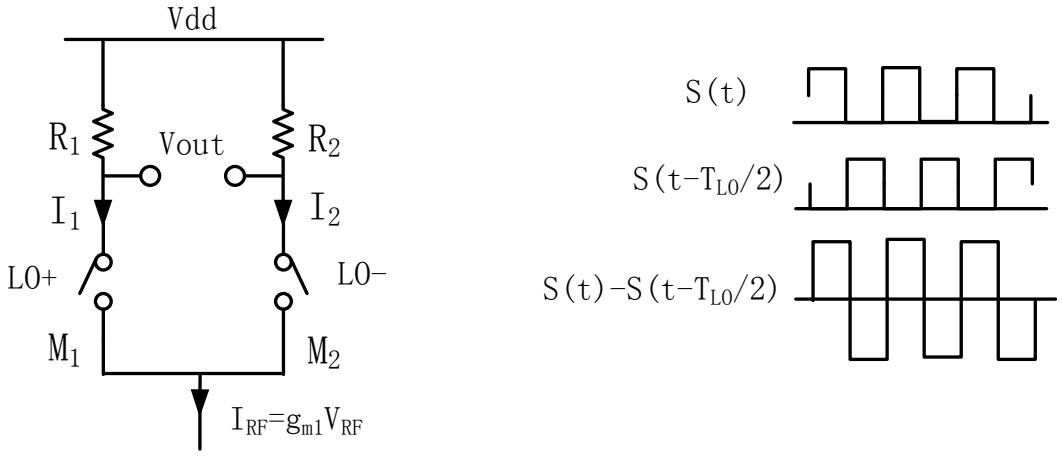

Figure. 2.17. Equivalent circuit of active mixer

Take the single balanced active mixer in figure 2.17 as an example, the transistor M1 will produce small signal current equal to $g_{m1}V_{Rf}$. The current of I1 and I2 is given by:

$$I_1 = I_{RF} \cdot S_{(t)} \tag{2.23}$$

$$I_2 = I_{Rf} \cdot S(t - \frac{T_{LO}}{2}) \tag{2.24}$$

At the output we get:

$$V_{out(t)} = I_{RF}R_D\left[s\left(t - \frac{T_{LO}}{2}\right) - S(t)\right]$$

$$= \frac{2}{\pi} g_{m1}R_D V_{RF} COS(\omega_{RF} - \omega_{LO})t \tag{2.25}$$

As shown in the equation, the active mixer has an ideal conversion gain of $\frac{2}{\pi}g_{m1}R_D$, which is much higher than that of the passive mixer.

2. DSB and SSB Noise

Unlike normal LNA noise, the noise of Mixer can be classified as double side band and single side band noise. Take a noiseless down-conversion mixer as an example. As we know the IF signal can be generated by both $|\omega_C - \omega_{LO}|$ and $|\omega_{img} - \omega_{LO}|$ where ω_{img} represents the image signal band. SSB noise represents the output noise figure when wanted signal only located on one side of the LO frequency. Since thermal noise exists equally in signal and image signal band, for DSB NF, where wanted signal located at either side of LO, the noise figure will be 3 dB lower.

2.3.3 Comparison of Active and Passive Mixer

Compared with a passive mixer, the gain of an active mixer will be much higher than that of a passive mixer. On the other hand, the passive mixer normally requires a large LO amplitude to minimize the noise contributed by its turn-on resistor which is more power consumption. Finally,

since the input impedance of passive mixer is a function of frequency, it will not be suitable for a design for wideband noise cancellation front-end.

A Gilbert double balanced mixer will be chosen in this design and detailed analysis will be presented in chapter 3.

2.4 Concept of "Blixer"

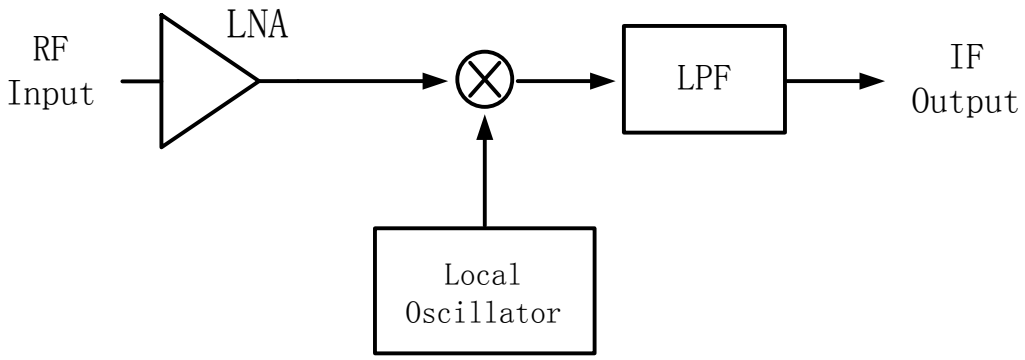

Figure. 2.18 Normal RF front-end architecture.

Figure 2.19 shows the traditional architecture of a RF receiver. The RF signal will process by an LNA and then goes into the Mixer for down-conversion. LNA and mixer are designed specifically for certain operation frequency. Also, normally there are several buffer stages between LNA and mixer to ensure better power transmission. In order to meet the requirement of SDR application, more and more wideband LNA have been proposed, which require the mixer also be wideband.

Recently an attractive structure called "Blixer" (Balun LNA merged with Mixer) has been proposed in order to meet the requirement of SDR. The basic idea is that the LNA and Mixer being combined together without any buffer stage, where both the LNA and Mixer stage are wideband. IF signal comes directly out the "Blixer" afterwards.

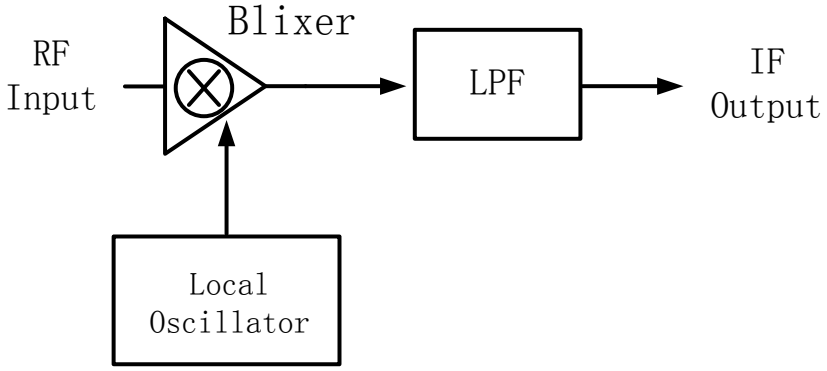

Figure. 2.19. Idea of Blixer topology.

Topic in this thesis will aims at building a wideband “Blixer” with noise cancellation technology. Detailed LNA and Mixer stage will be analyzed in chapter 3.

3.1 Balun LNA using BJT

3.1.1 Bipolar Balun-LNA Topology Synopsis

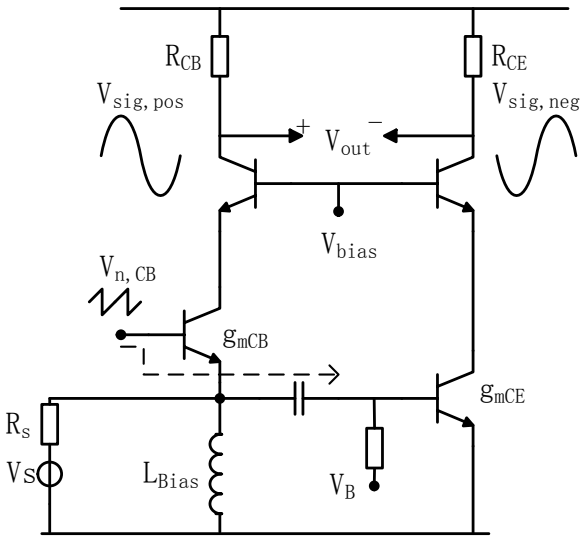

Figure. 3.1. Overall balun LNA topology using BJT.

Figure.3.1 shows the bipolar balun-LNA topology with one common base (CB) transistor paralleled by a common emitter (CE) transistor. The CB stage helps to achieve the wideband input matching with no extra matching network by its relatively stable input impedance matched to $R_s = \frac{1}{g_{m,CB}}$ and still provide enough gain. The CE stage is proposed for balun function by a negative phase output, while it simultaneously senses the noise flowing from the CB stage. Since the Bipolar transistor can achieve high g_m efficiency, this topology can reach good results in low noise, high linearity and achievable gain and detailed parameters and performance have been analyzed in following chapters.

The CB stage is biased by an off-chip inductor L_{Bias} to avoid extra noise elements and the inductor will occupy no DC voltage headroom. The inductor can be made to a suitable size in

order to match the requirement for certain bandwidth operation and serve as a RF band pre-filter, while in other way a relatively large inductor can make the circuit satisfied with a wideband input matching. As the inductor is an off-chip component, its quality factor is much higher than an on-chip one and it will be feasible enough to achieve different requirement especially for SDR.

3.1.2 Input Matching

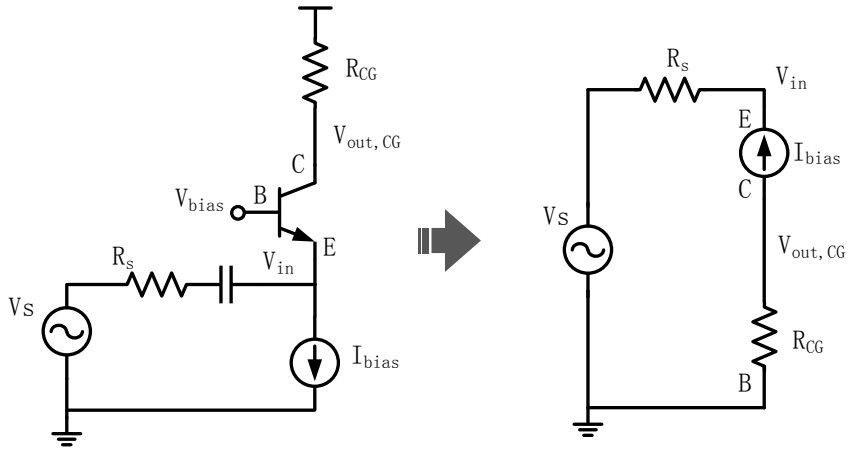

Figure. 3.2. Small signal equivalent of a CB-stage.

The common-base stage in Fig. 3.2 have an equivalent circuit where biased with a current by i_{ds} . As we can see, the current flows in and out through the transistor in a single path, making the current into the input equals to the current through the load resistor R_{CB}. The relation between its voltage gain and its input impedance can be calculated as:

$$i_{in} = i_{Rce} = \frac{V_{out,CB}}{R_{CB}} = \frac{V_{in} \cdot A_{v,CB}}{R_{CB}} \tag{3.1}$$

While the input impedance of the CB-stage can be expressed as:

$$R_{in,CB} = \frac{V_{in}}{i_{in}} = \frac{R_{CB}}{A_{v,CB}} \tag{3.2}$$

For an transistor having infinite output resistance paralleled with Load resistor, the voltage gain $A_{v,CB} = g_m R_{CB}$, results in an input impedance $R_{in} = \frac{V_{in}}{i_{in}} = \frac{1}{g_m}$.

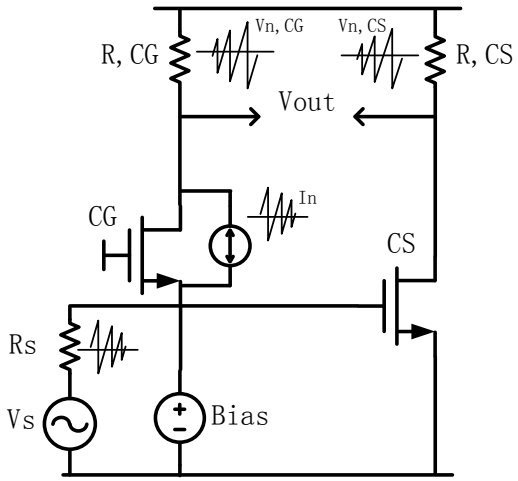

Figure. 3.3. Input equivalent circuit of the balun LNA.

Since another noise cancellation CE-stage that is being added to the CB-stage network, if Miller capacitor is ignored, the input of the CE stage can be calculated as:

$$Z_{CE} = r_b + r_\pi || C_\pi \tag{3.3}$$

Then the input impedance of the Balun LNA will be:

$$Z_{in,ToT} = Z_{in,CE} || Z_{in,CB} = \frac{1}{g_m} || (r_b + r_\pi || C_\pi) \tag{3.4}$$

As we can see from the equation, when the frequency of the input is relatively low, the impedance of CE stage will be way higher than the input impedance of CB stage ($\frac{1}{g_m}$). The input matching can be easily achieved by appropriate bias the CB stage and make $\frac{1}{g_m}$ equals 50 ohm.

Though the complex component (C_π) will add a pole to the impedance seeing from the input, degrading the real part of impedance of the CE stage and finally making the input impedance lower than 50ohm. The $\frac{1}{g_m}$ will still dominate the input impedance for a super wide bandwidth. The bandwidth (1GHz-7GHz) for 50ohm input matching is wide enough for SDR application. Smaller feature size of the transistor can further reduce the parasitic capacity and

extent the input matching bandwidth.

3.1.3 Wideband Voltage Gain Using Cascade

A. Gain Balance

For the CB stage of the balun-LNA, the input impedance can be written as $1/g_m$. The output voltage of the CB stage can be calculated as

$$V_{out,CB} = V_{in}A_{v,CB} = V_{in}g_{m,CB} \cdot R_{CB} \tag{3.5}$$

For an 50 Ω input impedance matching, $g_{m,CB}$ should be set to 20ms. A suitable load resistor R_{CB} such as 500Ω can make the idea voltage gain larger than 10.

In the CE stage, the voltage gain can be treated as the same as the CB stage, but have an opposite phase to form a balancing structure.

$$V_{out,CE} = V_{in}A_{v,CE} = -V_{in}g_{m,CE} \cdot R_{CE} \tag{3.6}$$

While in calculation the total voltage gain can be as large as 20, the actual gain after the input matching condition and many parasitism especially the Miller effect, will be dramatically affected. On the other hand, in practical using, as the input impedance of the buffer which is used between the output of the LNA and the input of the mixer stage is capacitive, the bandwidth will be further reduced.

B. Bandwidth

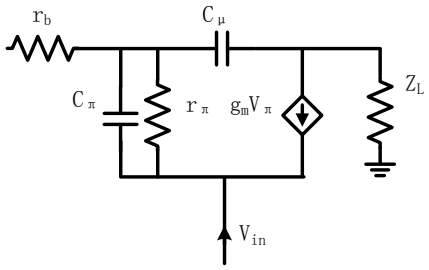

Figure.3.4. Pole in CB equivalent circuit.

Recall that in chapter 2, for both CE and CB amplifier, the gain bandwidth will be affected by the miller effect and other parasitic capacitor such as C_π. The pole of the CE and CB amplifier can be calculated as [7]:

$$f_{p,CE} = \frac{1}{r_\pi([C_\pi + C_\mu(1+g_m R_L)] + \frac{R_L}{r_\pi}[C_u + C_L])} \quad (3.7)$$

$$f_{p,CB} = \frac{1}{(\frac{1}{g_m}||R_E||R_I)C_\pi} \cong \frac{g_m}{C_\pi} \quad (3.8)$$

From the equation we can see that the input pole of the CB stage has no Miller components, and is dominate by the $\frac{1}{g_m}$ term, which is usually much smaller than the Load resistance of the CE stage. As a result, the input pole of the CB amplifier is typically a very higher frequency than CE. Such a property will result to gain and noise cancellation imbalance and heavily affect the LNA performance.

In order to extend the gain bandwidth of the CE stage for high frequency balance and noise cancellation. Two cascade stages have been added to the top of both CE and CB branch (figure 3.5). The load of the CE transistor now becomes $\frac{1}{g_{m,casd}}||R_{o,CE}$, which makes the multiplication component much smaller than before. At the same time, the same or even larger load resistor can be used after the cascade stage for keeping the voltage gain without hurting the bandwidth

[5].

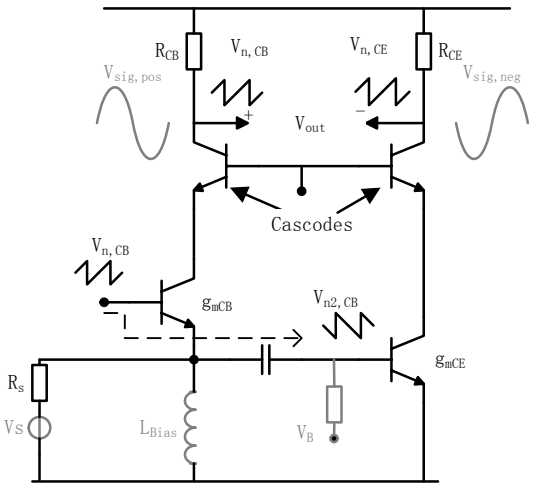

Figure. 3.5. The cascade balun LNA with noise cancellation.

3.1.4 Noise Cancellation Mechanism using BJT

A. Noise Cancellation

Recall the CE LNA analysis in chapter 2, in a simple CB stage, the noise of the CB transistor will dominate the noise figure. Additionally, as the g_m of the CB stage is fixed to 20ms, it is quite difficult to reach a NF under 3dB with achievable gain and bandwidth by changing the transistor size.

Like MOS transistor, Bipolar can also be chosen to form a noise cancellation structure. With its high current efficiency, the voltage gain can be as high as two times of MOS LNA. In another word, the power consumption can be lower to achieve same gain requirement by using BJT.

The mechanism for noise canceling BJT structure is very similar to the MOS one, but its noise analysis could be different. As in figure 3.5, the noise of CB can be treated as an voltage source $V_{n,CB}$ at the base of the transistor. This voltage will be sensed at the emitter of the CB or the base of the CE stage as $V_{n2,CB.}$ If we treated CB stage as an emitter follower, $V_{n2,CB}$ can be calculated as:

$$V_{n2,CB} = V_{n,CB}\frac{g_{m,CB}R_S}{1+g_{m,CB}R_S} \tag{3.9}$$

If α represent the input matching condition with a ratio of $\frac{R_S}{R_{in}}$, and we ignored the complex impedance provided by CE stage cause if very big, then the value of α is given by:

$$\alpha = \frac{R_S}{\frac{1}{g_{m,CB}}} = R_S g_{m,CB} \tag{3.10}$$

Then equation 3.9 becomes:

$$V_{n2,CB} = V_{n,CB}\frac{1}{1+\alpha} \tag{3.11}$$

This partial of noise of CB stage will be simultaneously amplified by CE stage as:

$$V_{o-,CB} = -V_{n,CB}\frac{1}{1+\alpha}A_{v,CE} = -V_{n,CB}\frac{1}{1+\alpha}g_{m,CE}R_{CE} \tag{3.12}$$

The noise voltage of CB will also be amplified by the CB transistor itself as:

$$V_{o+,CB} = V_{n,CB}A'_{v,CB} = -V_{n,CB}\frac{g_{m,CB}R_L}{1+g_{m,CB}R_S} = -V_{n,CB}\frac{g_{m,CB}R_{CB}}{1+\alpha} \tag{3.13}$$

The voltage gain in equation 3.13 is the gain from the base of the CB stage to the collector of the transistor.

Assume the voltage gain βA_v of CE stage is β times of that of the CB stage (A_v), the total output noise can be calculated as:

$$V_{no,TOT}^2 = V_{n,CB}^2 A_v\left(\frac{1-\beta}{1+\alpha}\right)^2 + V_{n,CE}^2 A_v\beta + 4kT(R_{CE}+R_{CB}) \tag{3.14}$$

In the equation, the first part of the noise is indicate the noise contributed by the CB transistor while the second terms indicate the noise resulted by the CE transistor. Since the overall voltage gain of the balun LNA is $A_v(1+\beta)\frac{1}{\alpha+1}$, the noise factor is the total output noise divided by the power gain and $4\mathrm{kT}R_S$:

$$F = 1 + \frac{V_{no,TOT}^2}{[A_v(1+\beta)\frac{1}{\alpha+1}]^2}$$

$$= V_{n,CB}^2 \frac{(1-\beta)^2}{4kTR_S(1+\beta)^2} + V_{n,CE}^2 \frac{(1+\alpha)^2}{4kTR_S} \frac{\beta^2}{(1+\beta)^2} + \frac{(R_{CB}+R_{CE})}{[A_v(1+\beta)\frac{1}{\alpha+1}]^2}$$

(3.15)

From the equation we can clearly see that the noise coming from the CB transistor can be completely cancelled once we keep the value of β equal to 1. This directly indicates that voltage gain of CB and CE stage should equal to each other. IN another words, the balance of the voltage gain also decide how well the noise of CB transistor can be cancelled.

Assume voltage gain is balance and under input matching condition, where α, β is 1, the main noise will be dominated by the CE stage instead of the CB stage. The noise figure can be approximately calculated as:

$$NF = 1 + \frac{R_S}{R_{CB}} + \frac{R_S R_{CE}}{R_{CB}^2} + \frac{V_{n,CE}^2}{4kTR_S} \quad (3.16)$$

By scaling the size of the CE transistor up by n times, the balanced bandwidth will not be heavily reduced and the noise will be scaled down as well. Normally the size of the CE stage should be 2~5 times larger than the CB stage. Unlike the MOS transistor, considering the input impedance of the CE stage is not purely capacitive, the size of the chosen bipolar transistor should not be overly scaled up so as its base resistor becomes close to 50 Ω. The load resistor of the CE stage should be relatively scaled down by n time in order to promise the output balance.

B. Analysis for Optimal Noise Figure of CE Transistor

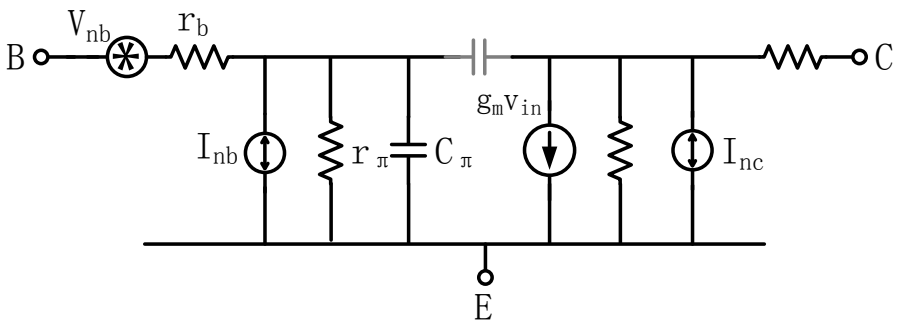

Figure. 3.6. Physical noise model for bipolar transistor.

Since the noise coming from the CB stage will been totally cancelled when the gain of two branches is properly set the, the total noise performance is going to be dominated by the CE transistor. The scaled size and the bias point of the CE stage directly determine the performance of the whole LNA. A detailed analysis of the noise performance of the CB amplifier has been made to optimize noise figure in this chapter.

As we can see from figure 3.6, the bipolar have basic three types of the noise source, including:

Base Resistor Noise: $$V_{nb}^2 = 4KTr_b \quad (3.17)$$

Base (Emitter) Shot Noise: $$i_{nb}^2 = 2qI_B \quad (3.18)$$

Collector Shot Noise: $$i_{nc}^2 = 2qI_C \quad (3.19)$$

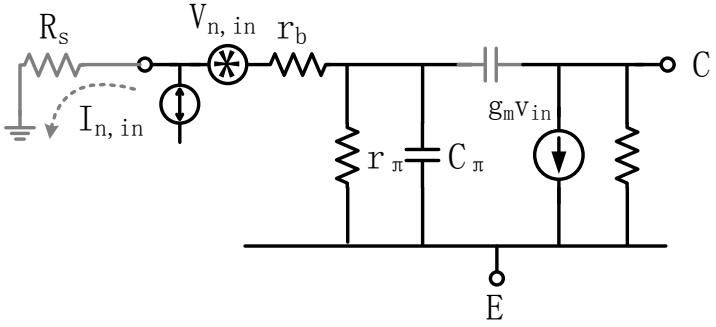

Figure. 3.7. Input referred noise model.

Both of those noise sources can be referred to input for noise figure calculation. First when we short the input, the referred input noise current flows into the ground and thus the input referred noise voltage V_n is the only noise source. Then we get:

$$\overline{i_{on\_tot}^2} = \overline{v_n^2} g_m^2 = \overline{v_{nb}^2} g_m^2 + \overline{i_{nc}^2} \tag{3.20}$$

$$\overline{v_n^2} = \frac{2qI_C}{g_m^2} + 4kTr_b \tag{3.21}$$

If the input is opened, the input referred current noise i_n is the only noise source. We get:

$$\overline{i_{on\_tot}^2} = \overline{i_n^2} Z_\pi^2 g_m^2 = \overline{i_{nb}^2} Z_\pi^2 g_m^2 + \overline{i_{nc}^2} \tag{3.22}$$

$$\overline{i_n^2} = 2qI_B + \frac{2qI_C}{g_m^2} Y_\pi^2 \tag{3.23}$$

where

$$Y_\pi \approx \frac{g_m}{\beta} \tag{3.24}$$

Finally, the total input referred noise (including noise from the input soucre) should be cacualted as the sum of the noise current(voltage format) and the noise voltage:

$$v_n^2 = \left[4kTr_b + \left(\frac{\sqrt{2qI_C}}{g_m}\right)^2\right] + R_s^2\left[\left(\frac{\sqrt{2qI_C}}{\beta}\right)^2 + \left(\sqrt{2qI_B}\right)^2\right] \tag{3.25}$$

There are four noise components in the equation for input referred noise. The terms that relate with I_c is the collector shot noise while the terms with I_b is base current shot noise. R_s represents the source noise resistrance and r_b is also one of the biggest dornor for noise.

According to equation 3.16 the NF of the bipolar balun LNA is given by:

$$NF = \frac{v_n^2}{4kTR_S} = 1 + \left(\frac{R_S}{R_{CB}} + \frac{R_S R_{CE}}{{R_{CB}}^2}\right) + \frac{r_b}{R_s} + \frac{1}{2g_{m,CE}R_s} + \frac{g_{m,CE}R_s}{2\beta_0} + \frac{g_{m,CE}R_s}{2|\beta|^2} \tag{3.26}$$

The equation 3.26 provides us with a clear guidance for the noise performance of the transistor. When the frequency is low, the relatively high β_0 will decrease the contribution of the $g_m R_S$ terms, which make the base resistance as well as the $\frac{1}{2g_m R_s}$ term dominate the noise figure. The NF is a strong function of emitter length (r_b) and I_C (g_m). NF_{min} can be obtained by proper bias current with proper scaled bigger emitter length. However, when the input frequency grows, as the decreasing of the current gain β, the NF will increase if we keep boosting the bias current for higher g_m. On the other hand, for high frequency operation, increase device size does reduce base resistance, yet capacitance also increase which reduce the gain. NF will degrade as frequency increases.

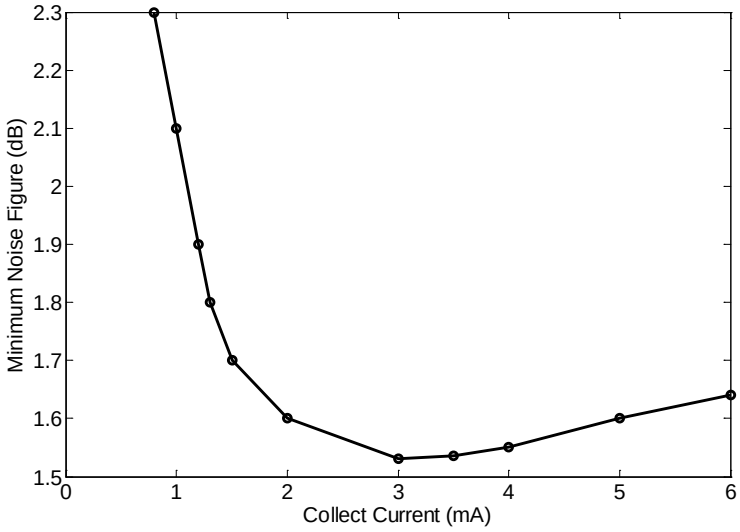

Figure. 3.8. Noise figure versus bias current.

Figure 3.8 shows the simulated relationship between the minimum NF we can obtain with the collector current for the 0.18um SiGe bipolar transistor that we are going to use. According to the simulation result, the CE stage of the balun LNA will be biased between 3mA to 3.5mA.

The size of the CE stage will be properly chosen with the tradeoff between noise and bandwidth. In this design, CE stage is 4 times of the CB stage.

3.2 Double Balanced Mixer stage

3.2.1 Double Balanced Gilbert Mixer Topology

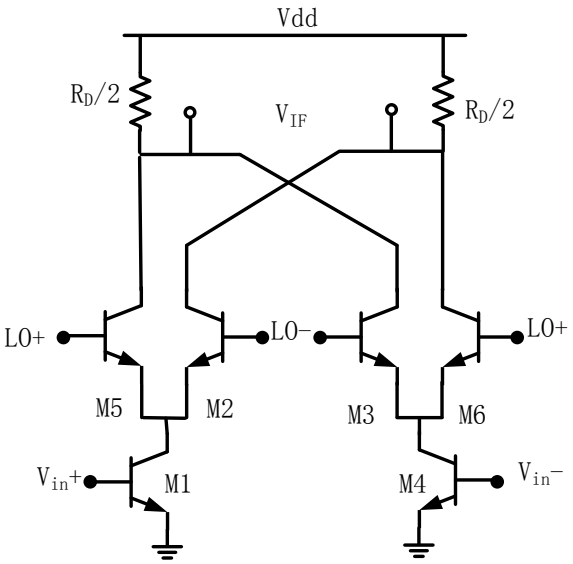

Figure. 3.9. Double balanced Gilbert mixer (BJT).

The mixer stage choice of this design in this thesis is the Gilbert Double Balanced stage. During the process of mixer, both input signal and LO signal will feed through into the output, contributing to noise and nonlinearity. Among all the mixer structure, Gilbert is a good solution to eliminate the problem.

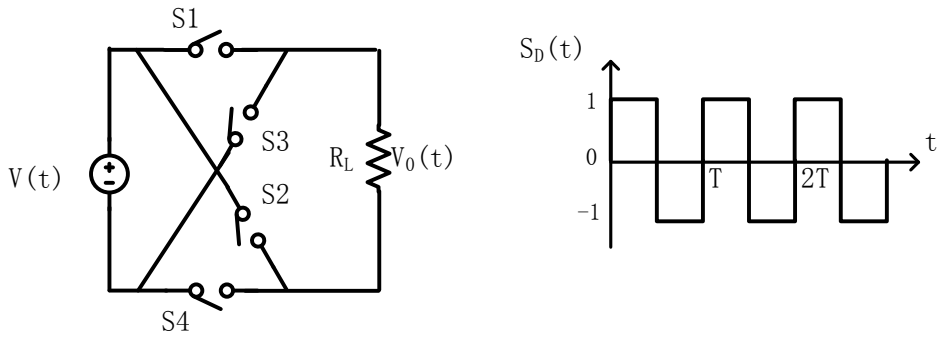

Figure. 3.10. Double balanced mixers equivalent circuit and switching waveform.

Double balanced Mixer uses four switches connected as figure 3.10. During the first half of the working circle, switch S_1 and switch S_4 are closed at the same time while the input source $V_1(t)$

is connected to the output load R_L. At the second working circle, when the switch S_1 and S_4 opened while switch S_2 and S_3 closed, the source is also directly connect with R_L but with reversing polarity. During the whole working circle when switch alternating between -1 and +1, the average DC will be zero at the output.

The Fourier series for the switching waveform is now [7]:

$$S_D(t) = \frac{4}{\pi}\sum_{n\ odd}\frac{1}{n}sinn\omega_2 t \qquad where \quad \omega_0 = \frac{2\pi}{T} \tag{3.27}$$

And the output will be [7]:

$$V_0(t) = \frac{2A}{\pi}\sum_{n\ odd}\frac{cos(n\omega_2-\omega_1)t-cos(n\omega_2+\omega_1)t}{n} \tag{3.28}$$

3.2.2 Analysis for Optimal Down Conversion [8]

A. Conversion Gain

We now consider the non-ideal conversion gain of an active mixer for latter optimization.

1. Gradual LO transition

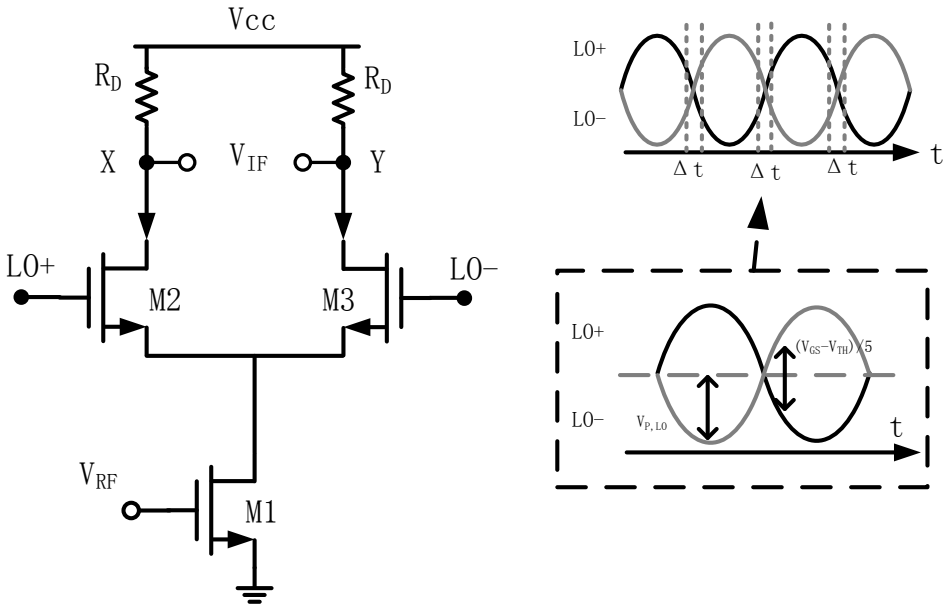

Figure. 3.11. Gain reduction of gradual LO transition.

In practical application, it is impossible to generate an ideal square wave for LO. Normally a sinusoidal waveform will be applied in replace of the square wave. As we can see from the figure 3.11, two anti-phase LO signal remains approximately equal within certain fraction of half cycle, ΔT. We assume both of the switch transistors M_2 and M_3 are equilibrium, during ΔT the current from M_1 will be separate equally to each branch, serving as a common mode input with very litter gain at the output. As a result, the conversion gain will degrade if the LO swing is lowered.

The differential pair has same overdrive voltage (VGS-VTH) and then differential input voltage generated from the input current is $\sqrt{2}(V_{GS} - V_{TH})$. We assume that the drain current are roughly equal for $\Delta V_{in} \leq (V_{GS} - V_{TH})/5$. If the peak amplitude of the LO waveform is $V_{p,LO}$, then $\overline{LO}\ and\ LO$ will different by (V_{GS}-V_{TH})/5 in $\frac{\Delta T}{2} = \frac{V_{GS}-V_{TH}}{5}/(2V_{P,LO}\omega_{LO})$seconds. This result will multiply by a factor of 4 for both rising and falling edges and normalizing to LO period, then the final conversion gain of the mixer can be calculated as [8]:

$$A_V = \frac{2}{\pi} g_{m1} R_D \left(1 - \frac{2\Delta T}{T_{LO}}\right) \tag{3.29}$$

$$= \frac{2}{\pi} g_{m1} R_D \left[1 - \frac{(V_{GS}-V_{TH})}{5\pi V_{P,LO}}\right] \tag{3.30}$$

Equation indicate that in order to minimize the effect of gradual LO, the amplitude of the LO should be relatively big.

2. Input Capacitor

Another component that can be related to conversion gain is the total capacitors seeing from the drain of input transistor.

As the capacitor is going to split the input current with the input impedance ($1/g_m$) of M_2,the conversion gain based on equation 3.22 can be changed to:

$$A_{v,cp} = \frac{2}{\pi} g_{m1} R_D \left[1 - \frac{2(V_{GS} - V_{TH})}{5\pi V_{P,LO}}\right] \frac{g_{m2}}{\sqrt{C_p^2 \omega^2 + g_{m2}^2}} \tag{3.31}$$

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd} + C_{gb})} \tag{3.32}$$

From the equation 3.24, we can see that the actual conversion gain is a function of C_p at the denominator. While at the same time, part of the Capacitors of C_p can be decided by f_T. This indicate that when the switch working frequency is way lower than the peak f_T， the effect of the input capacitor term can be minimized or even be ignored. Normally the f_T is a function of the transistor size and bias current which should be properly chosen.

B. Input Referred Noise

Both of the two switch transistor noise as well as the current noise injected by M1 will appear at the output. The total noise seeing at the output for one differential branch can be calculated as:

$$\overline{V_{no}^2} = \frac{1}{2}\left(\overline{I_{n,M1}^2} + \overline{V_{n,M2}^2} C_p^2 \omega^2\right) R_D^2 + 4kTR_D \tag{3.33}$$

Therefore the input referred noise is going to be:

$$\overline{V_{ni}^2} = \frac{\overline{V_{no}^2}}{Av} = \pi^2 \left(\frac{C_P^2 \omega^2}{g_{m2}^2} + 1\right) kT \left(\frac{\gamma}{g_{m1}} + \frac{\gamma C_P^2 \omega^2}{g_{m2} g_{m1}^2} + \frac{2}{g_{m1}^2 R_D}\right) \tag{3.34}$$

As we can observe that, at the output noise equation 3.34, there is also a component Cp that will affect the noise performance, which raise the importance of high f_T operation of the transistor.

On the other hand, unlike passive, the active mixer suffers from the flicker noise from the sub at the output. As mentioned at previously chapter, the noise can be calculated as:

$$V_{n,out}(f)||_{k=0} = \frac{I_{SS}R_D}{\pi V_{p,LO}} V_{n(f)} \tag{3.35}$$

As a sum up, order to reduce the flicker noise, it is important to scared down the $I_{SS}/V_{p,LO}$ term. Therefore it is necessary to minimize the bias current and improve the amplitude of the LO waveform.

3.3 The Folded Blixer Topology

3.3.1 The Folded Structure

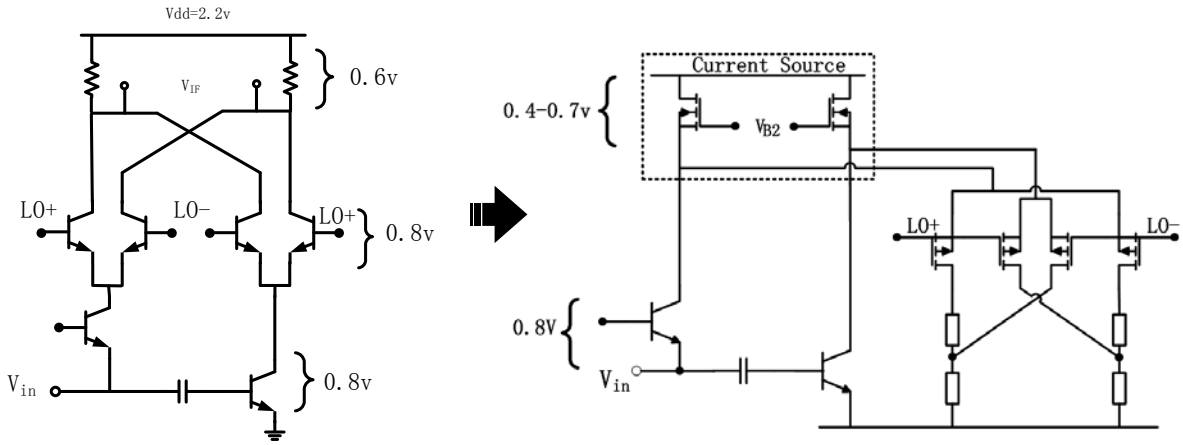

Figure. 3.12. Cascade mixer merged with LNA.

The goal of this topic is aims at merge the LNA noise cancellation technology with a gilbert mixer. A Usual way to do it is to cascade the mixer stage at the top of the LNA stage(figure 3.15). However, as we can obtain from previous analysis, the optimal working conditions for LNA and mixer stage are quite different, which raises the requirement for separate operation and this cannot be down with a same bias current just in one cascaded path. On the other hand, if we cascade several levels of transistors together, the voltage supply should be much higher in order to provide enough voltage headroom to each stage.

The folded structure(figure 3.17) is exactly an excellent method to solve this entire problem

at the same time. From the LNA side, proper bias current can be set to minimize the noise contribute by the CE stage. From the mixer stage, relatively low bias current should be used to minimize the flicker noise at the trade of high enough f_T。Also consider the power consumption; the supply voltage can be lowered from 2.2v to 1.5v or even 1.2v, with much lower current using at the mixer stage.

3.3.2 The Basic Folded Blixer Topology

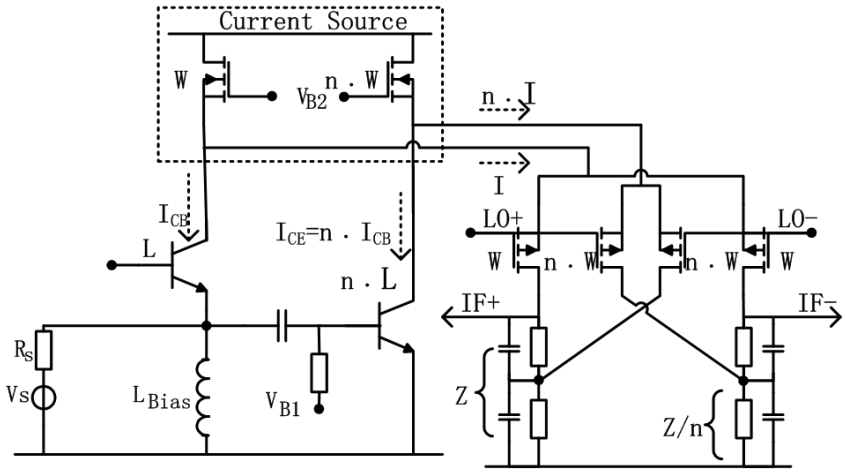

Figure. 3.13. The folded Mixer merged with balun LNA topology.

Figure 3.13 shows the basic topology of the folded balun-Blixer proposed in this thesis. The left side still holds like a basic balun-LNA topology, while the cascades stage now has been replaced by PMOS transistor and has been folded to another side to the ground. Two PMOS transistors at the top of the circuit form two current sources. As current in each side flows from top to bottom and sum together at the top, the circuit is folded which make the LNA and mixer stage paralleled to each other. The signal flows out of the LNA stage will still goes into the right side as it sees large impedance at the drain of the PMOS current source.

Each transistor in the balun-LNA stage will now have two cascades instead of one to form a

double balance gilbert mixer. The total four PMOS transistor on the right side will now also serve as switches, being turned on and off with two anti-phase LO signals bringing into its gate. In this topology, the LNA can be treated like a g_m stage of a mixer while the four switch stages become the cascades stage of the previously mentioned balun-LNA.

3.3.3 Noise Cancellation at IF Band

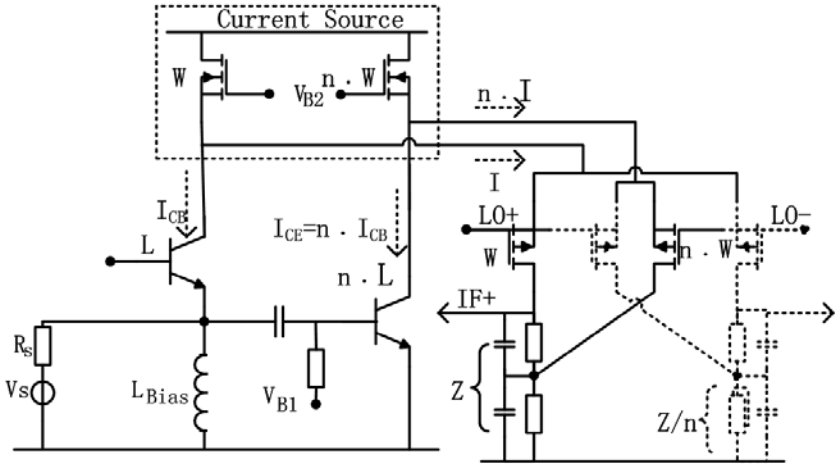

Figure. 3.14. The folded Blixer topology (half branch).

As we can see the half branch of the folded Blixer in figure 3.14, the basic topology is exactly the same as the balun-LNA except being folded and cascades being replaced with PMOS transistor. Unlike the balun-LNA, the output balance and noise cancellation in this topology occurs at one branch. As the two switches are driven by a couple of anti-phase LO signals, the signal at the IF node will have the same phase while noise of the CB stage will represents as anti-phases. At the switch stage, one capacity and one resistor forms the load. As we can see that the load impedance of CB stage is also n times than that of the CE stage which helps to form an output balance and noise cancellation.

Though appears the same property, gain balance for noise cancelation the IF node will be

quite better than that of the RF node. Signal that has been down converted with the same phase will be recombined to each other in a single path automatically without differential output. Unlike the Balun LNA, where differential output is with different bias current, the current through IF+ and IF- branch will have exactly the same bias. On the other hand, as the voltage gain generated at the IF band with much lower frequency, the variation of the load resistance due to parasitic capacitor will also be minimized.

3.3.4 Conversion Gain and Complex Load

A. Conversion Gain

As mention previously, the LNA stage can be treated as the g_m stage of the mixer, making the whole topology to a noise cancellation gilbert mixer. Since the voltage gain is obtained at the IF output after down conversion, the voltage conversion gain (CG) from the single-end of the LNA to the mixer output of the Blixer is calculated as follows:

$$CG_{Blixer} = \frac{2}{\pi}(g_{mCB} \cdot R_{CB} + g_{mCE} \cdot R_{CE}) \cdot 2 \cdot \frac{1}{2}$$

$$= \frac{2}{\pi} \cdot (g_{mCB} \cdot R_{CB} + g_{mCE} \cdot R_{CE}) \qquad (3.36)$$

In the equation, the second term comes from the balun LNA and the first term $2/\pi$ is the basic conversion loss of a double balanced gilbert mixer for 50% duty-cycle (LO)-signal waving from logic 0 to logic 1. Factor 2 indicates the differential output and factor 1/2 is because only lower frequency part of the down conversion result is being used.

Due to the nature of the frequency conversion, the gain have been inevitably scaled down by the factor $2/\pi$, contributing directly $20\log(2/\pi)$=3.91dB degrade of the noise figure

performance.

B. Complex Load

As the input matching of the LNA stage is super wideband, all kinds of signals as well as noises with frequency in the bandwidth will be treated indistinctively and will all be amplified. At the output of the LNA, however, there is impractical to design a filter to eliminate the unwanted signal and keep the wanted signal as the frequency remains very high.

In this design, a complex load has been used to replace the pure resistance load. Since the output frequency of the IF band is usually within hundreds MHz, it is much easier to add a pole to the voltage gain to filtered out high frequency noise as well as the image produce of the donw-converted signal. As we can see from figure 3.19, the capacity and the resistor together serves as filter that help to filter the majority of the high frequency signal or noise. The single pole formed by the RC can be calculated as:

$$f_{pole} = \frac{1}{2\pi RC} \tag{3.37}$$

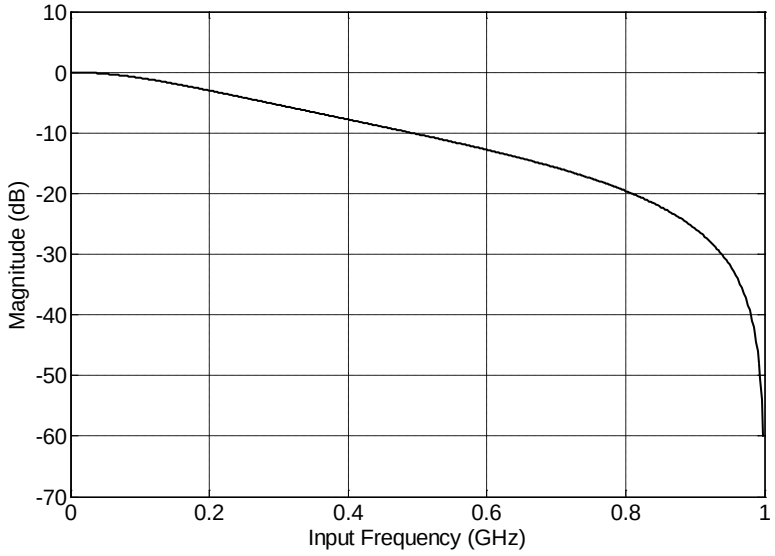

Figure. 3.15. Frequency response of complex load.

Higher order low pass load impedance can be designed to further reduce the noise of the system. However, the contribution will be far less important at the cost of extra inductor with huge size.

At the same time, the paralleled with the CE stage will also be n times bigger than the one paralleled with the CB stage. The total impedance seeing by the stage of CE will be keep 1/n times of the CB stage which maintained signal balance and noise canceling condition.

3.3.5 Allocation of Bias and Transistor Size

To the LNA stage, the current of the CB stage is set around 600uA so as to achieve input impedance (50 Ω). At the same time in order to provide the noise cancelation and have a low noise figure, the CE transistor's g_m is 5 times larger than the CB stage. As its size is far larger than the CB stage, its base resistor will be kept much lower.

While to the mixer stage, the bias current should be set to ensure the switch speed. With technique used in this research the PMOS devices with moderated W/L can relatively switches quickly enough to sense the signal from the LNA stage. In addition, the suitable LO amplitudes (500mVpp) is used to avoid gradual edge which may contribute to noise. When the speed of the device is ensured, the bias current of the switches (85uA and 445uA) should be minimized to suppress DC offset, thermal and 1/f noise. Moreover, as the bias current of the switches stage is relatively low, the load resistor can be further larger (200 Ω and 1k Ω) to boost the conversion gain.

4.1 Overview of the System

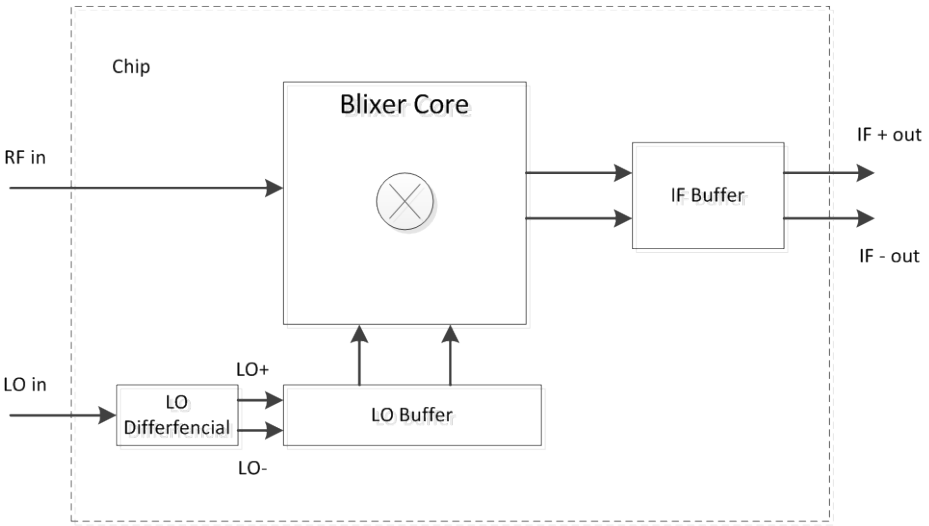

Figure. 4.1. Overview of the chip.

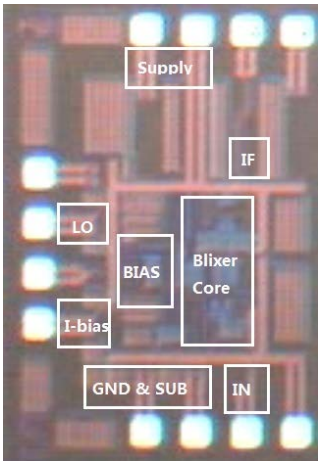

Figure. 4.2. Die photo of the Blixer front end.

The LO is derived from an external clock and go through a single-to-differential converter for differential output. Before entering the mixer it will pass several inverter and buffer stage to make it more like a square wave. RF input will go directly into the LNA stage and IF output signals will be buffered to the output.

4.2 Input Matching

As the CB stage with moderated g_m can provide a good input matching condition(real part of the total impedance is 50Ω) at low frequency. However, the LC (inductor and capacitor) property seeing from the input of the LNA stage will then gradually affect the match condition when frequency grows. That's another reason that the CB transistor size can't be overly large. The off-chip inductor and the input capacity of the CE stage together forms an LC tank and the S11 figure reaches a bottom value as the LC tank becomes resonate and cancel with each other. Figure below shows the S11 of the circuit. The total bandwidth (below -10dB) is from 500MHz to 6GHz and reaches the best value at 1.4G Hz.

Another observation is that, the down bond inductor and pad parasitic capacitor also contribute another LC which led to another zero in the figure. The most matching point in the figure (1.4G Hz) can be changed by varying the off-chip inductor for different application.

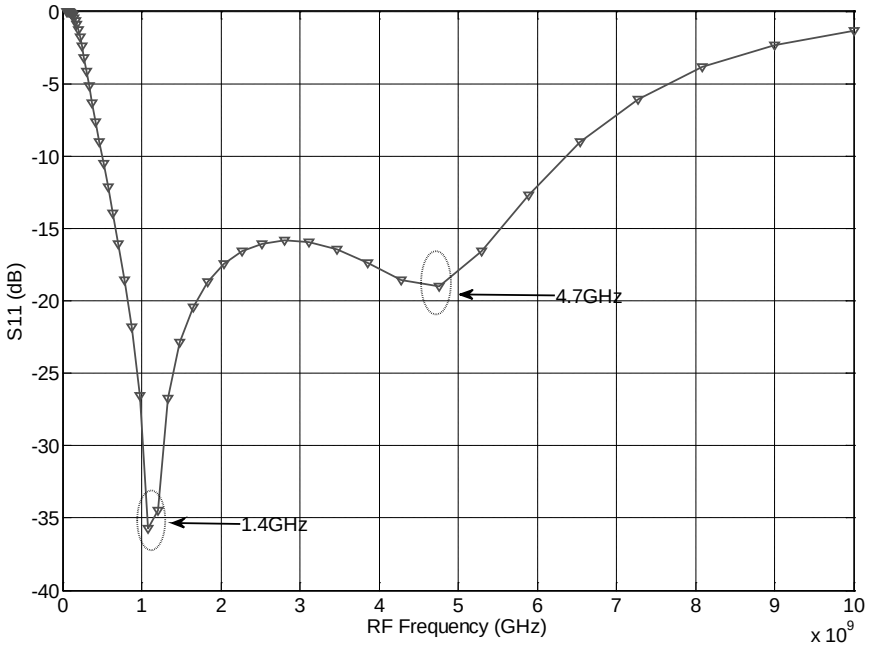

Figure. 4.3. S11 figure of the folded Blixer @RF frequency 0-6GHz.

4.3 Conversion Gain

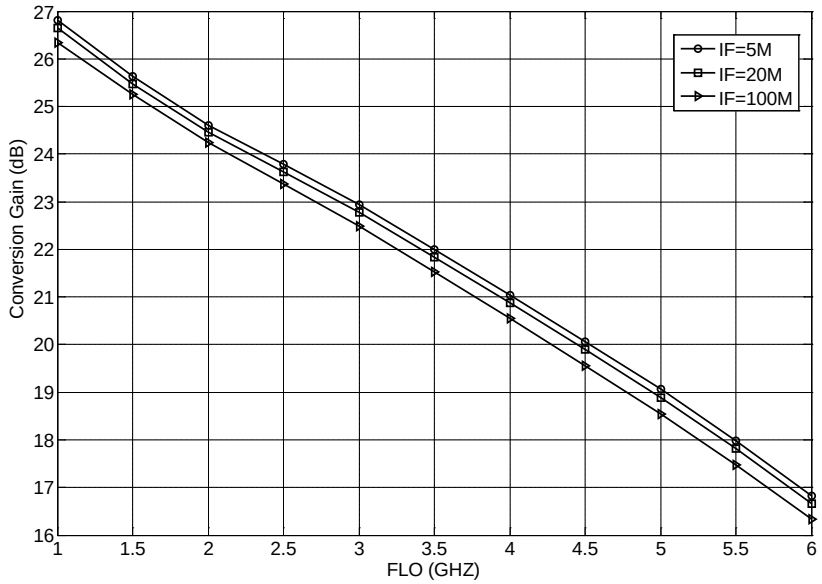

Figure. 4.4. Conversion gain of the Blixer @IF frequency 5MHz, 20MHz and 100MHz.

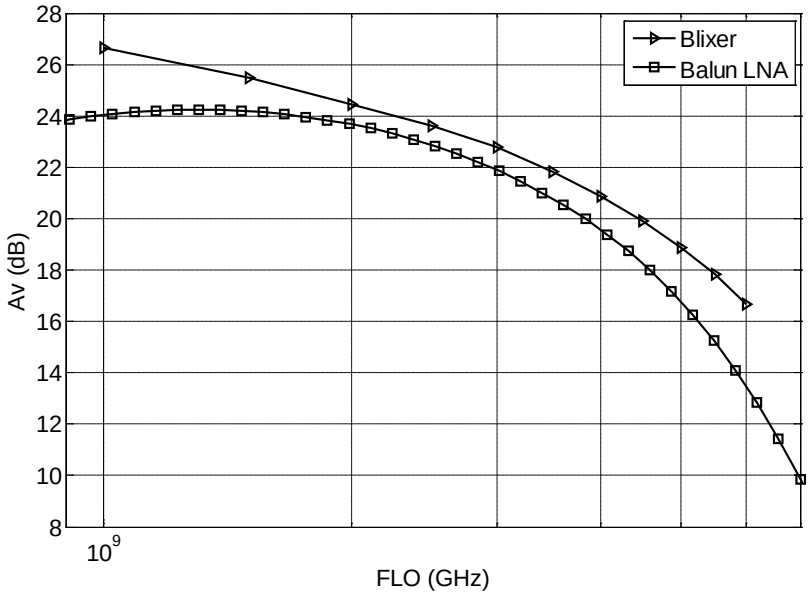

Figure. 4.5. Gain of balun LNA and Blixer @IF frequency 50MHz.

Figure 4.5 shows the IF conversion gain while LO frequency changes from 1GHz to 6GHz.As we can see , the conversion gain varies little around the IF frequency from 5MHZ to 100MHz, the overall conversion gain keeps larger than 16dB during 1-6GHz bandwidth of LO frequency.

4.4 Noise Figure

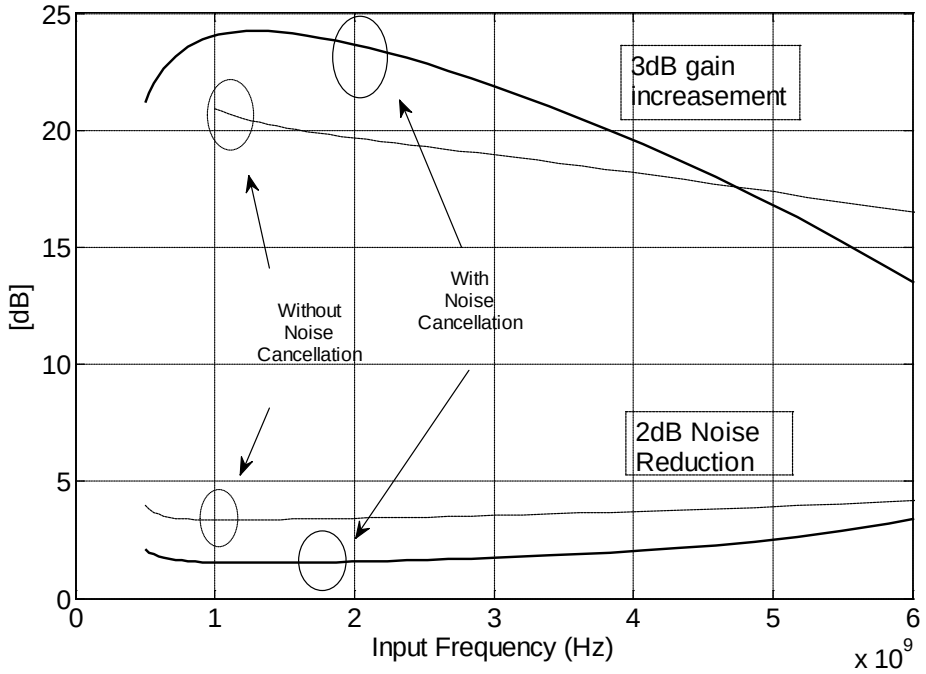

Figure. 4.6. Performance comparison between LNA with and without noise cancellation.

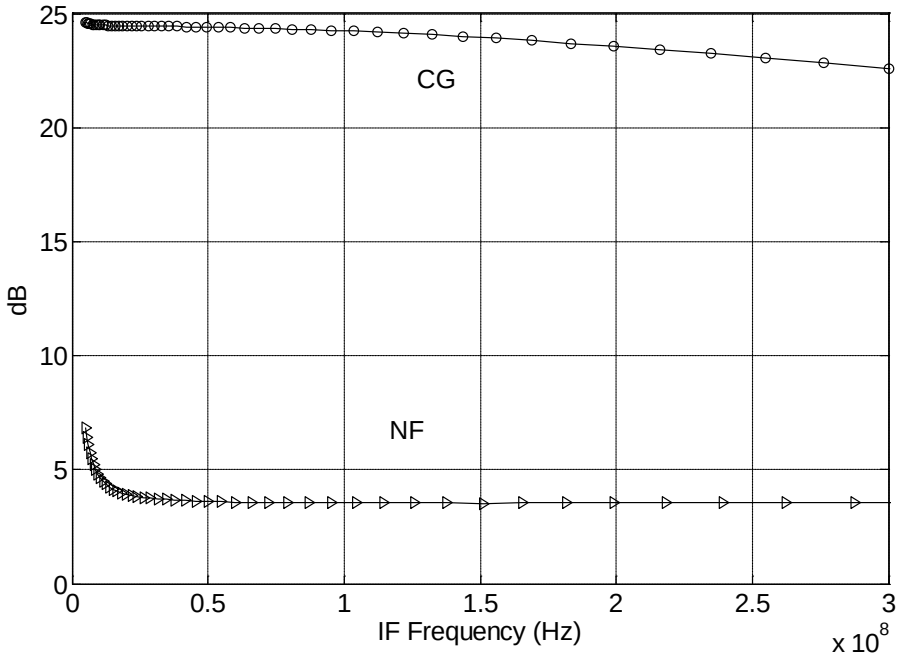

Figure. 4.7. Noise figure and conversion gain @input frequency of 2GHz.

Figure 4.6 shows the performance that improved by the noise cancellation technology of the

wideband LNA. Without cancellation, the noise figure is produced all by CB transistor. We can see, though it is relatively more wider-bandwidth, the noise figure is higher than 3dB. With noise cancellation, on the other hand, the LNA cancels the noise of CB with only 1.5dB noise coming from the scaled CE transistor. The voltage gain is also improved by 3 dB for its differential output.

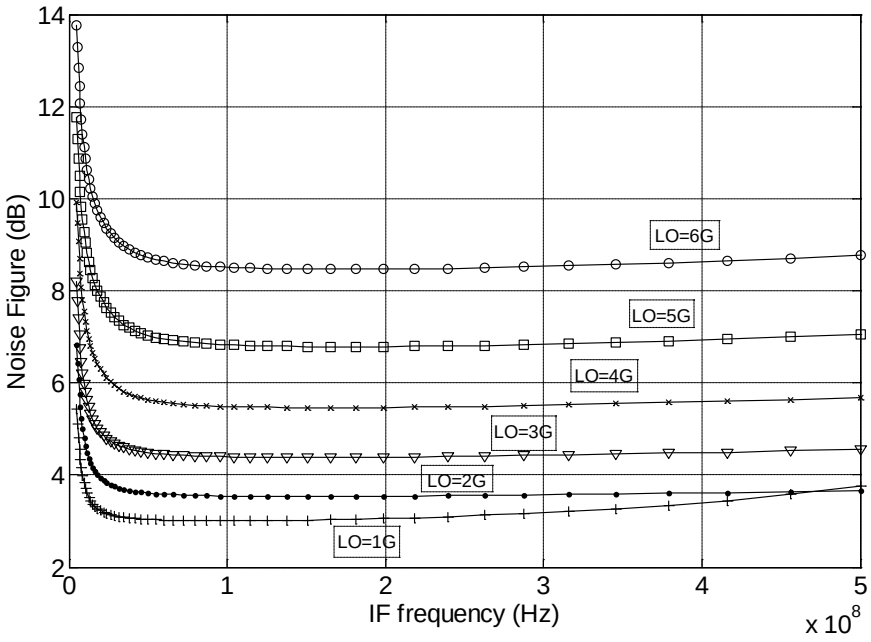

Figure. 4.8. Noise figure when IF bandwidth from 0 to 500 MHz while LO frequency from 1GHz to 6GHz.

Figure 4.7 and 4.8 shows the DSB noise figure of the IF frequency while LO frequency varies from 1GHz to 6GHz. Take LO=2GHz as an example, we can see that as the IF frequency grows, the 1/f noise dramatically decreases and the figure turns to be flat and reach 5.2dB over hundreds of MHz bandwidth (NF_{SSB} is calculated by adding N_{DSB} with 3 dB automatically). With the increasing of the signal frequency, performance of the switches and LNA stage has been scaled down for several degrees and so the overall noise level increases.

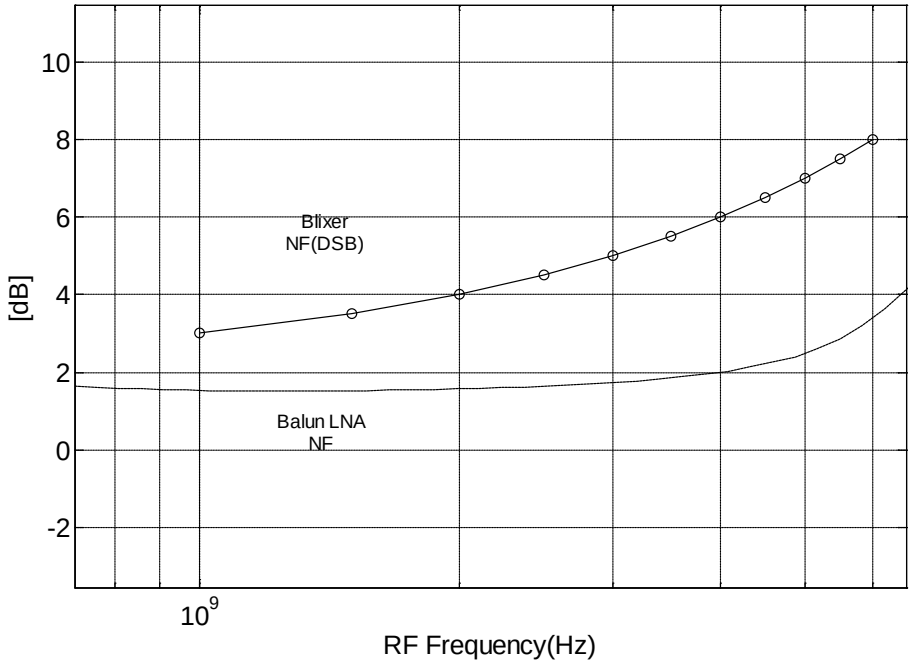

Figure. 4.9. Noise figure of balun LNA and folded Blixer versus input frequency

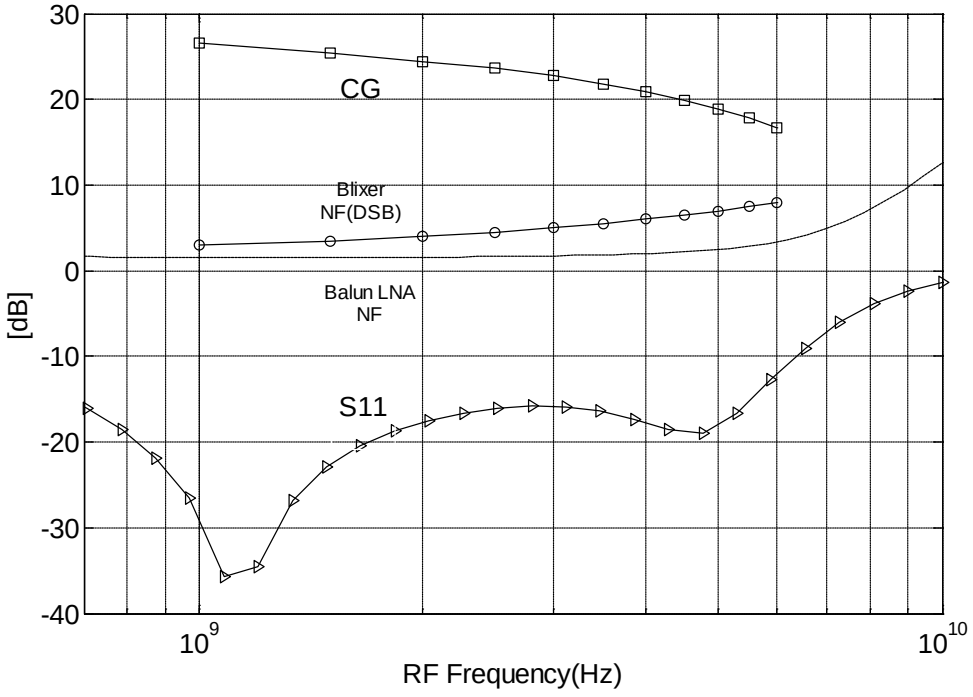

Figure. 4.10. S11, NF and CG performance @IF frequency 20MHz.

Figure 4.10 shows a complete picture about basic performance of the Blixer designed in this paper. Though its noise figure is larger than a single balun LNA for the added devices and

conversion loses, it's still comparable to other front-end's performance. As the bias current can be separately moderated, this topology is enough flexible to achieve different requirements.

4.5 Power Consumption of the Blixer

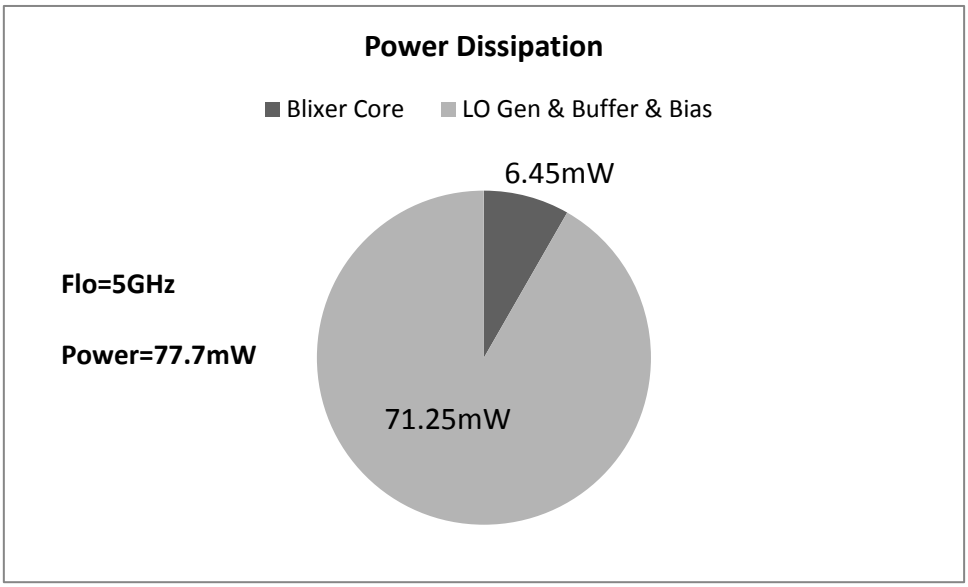

Figure. 4.11. Power consumption distribution.

4.6 Comparison of Wideband Down-Converters

Paremeter	This work	Craninckx Isscc'07[2]	Amer ISSC'07[3]	Cusmai ISCC'06[9]
RX Frequency[GHz]	1-5	1.8&5-6	0.1-3.85	3.4-7.6
Gain[dB]	16-25 Incl.IF-Amp	10-90 Incl.IF-Amp	20 Incl.IF-Amp	20-23
IIP3[dB]	-4	-9	-3.2	-3.5-3.3
NF[dB]	4.5-8.5 (SSB)	4-8	8.4-11.5 (SSB)	5.2-7.7
S_{11}[dB]	<-10	<-9	<-10	<-10
Power[mW]	6mW (only core)	34 WLAN setting	9.8 (only I -path)	18wm
Technology	0.18µm SiGe	0.13µm CMOS	90nm CMOS	0.18µm CMOS
VDD	1.5V	1.2v	1.2v	1.8v

Chapter 5 Conclusions

This thesis's topic is proposed to merge a Gilbert mixer topology with a noise-canceling Balun-LNA with folded structure. The voltage gain is created at the IF band out of the mixer instead of the RF band, thus the broad bandwidth is achieved using no inductor for bandwidth extension. The total circuit is based on 0.18-um SiGe technology. In order to realize a relative high voltage gain as well as less power consumption, bipolar is chosen at the LNA stage and MOS used at the mixer stage with a folded structure to lower down the power supply. The total LNA-Folded-Mixer achieves down conversion gain > 16dB, S11< 10dB and noise figure changes from 4.5dB to 8.5dB during RF bandwidth from 1GMHz to 5GHz, IIP3= -4dB. The total die area of the core is less than $2mm^2$ and the power supply is 1.5V with a power consumption of 6mW in 0.18um SiGe.

As the performance of the switches is mostly decided by the technology feature size, the overall noise figure can be further developed using less size PMOS transistors and the bandwidth can be even wider. The chip is under testing so all the figures are based on simulation.

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