Reliability of Lead-Free Electronic Package Interconnections Under Harsh Environmental Conditions

by

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Abstract

Lead (Pb)-free solder alloy technology has matured to the point where scientists and engineers are currently working out the fine points of Pb-free materials, particularly in regard to solder performance under harsh environmental conditions. The solder reliability is of special concern for Pb-free assemblies, especially those exposed to high temperature in a long period of time. In order to provide a better understanding of Pb-free solder joint behavior in harsh environments, this research addresses the isothermal aging of Sn-Ag-Cu (SAC105 and SAC305) alloys under elevated temperatures, with a point to examine the solder microstructural and thermal-mechanical properties. Our central goal is to discover the effect of isothermal aging on the reliability of Sn-Ag-Cu (SAC) assemblies. We have employed different surface finishes which have received increasing attention for both packaging and subtracted application—immersion Ag (ImAg), immersion Sn (ImSn), electroless Ni/immersion Au (ENIG), and electroless Ni/electroless Pd/immersion Au (ENEPIG). A full experiment matrix with varying aging temperatures and solder alloys was considered. Package sizes ranged from 19mm, 0.8mm pitch ball grid arrays (BGAs) to 5mm, 0.4mm pitch μBGAs and, in addition, 0.65mm MLF and 2512 resistors. Aging conditions included temperatures varying from 25°C, 55°C, 85°C, 100°C and 125°C over time periods of 0, 21 days, 6 months, 12 months and 24 months. After aging, the specimens were all subjected to thermally cycling from -40°C to 125°C with 15 min dwell times at the high and low peak temperature. This procedure enables the generation of experimental data to quantify the degradation of the characteristic lifetime of SAC alloys on ImAg and ImSn surface finish in elevated temperature environments.

Our results show a significant degradation in reliability for both SAC105 and SAC305 in 10mm packages on ImAg during elevated temperature isothermal aging. There were 9% and 50% reductions in characteristic lifetime for SAC105 and SAC305 after 24 months/85°C aging, respectively. After 2 years/125°C aging, the package lifetime decreased by 61% for SAC105 and

nearly 60% for SAC305. For passive 2512 resistors, the reliability performance was reduced by 25% and 35% after 24 months of aging at 85°C and 125°C respectively.

Long-term thermal aging results in significant reliability degradation for Sn-37Pb, SAC105, and SAC305 solder alloys on ENIG and ENEPIG. The reduction of reliability is observed throughout the aging period. There was a ~ 25% reduction in characteristic lifetime for SAC105 and SAC305 on ENIG during 12 month/85°C aging and ~ 35% degradation on ENEPIG. After 12 months/125°C aging, the package lifetime decreased ~ 40% for SAC105 and SAC305. Traditional Sn-37Pb solder outperformed the SAC alloys over long-term aging.

Failure analysis showed dramatic intermetallic binary Cu-Sn and ternary Ni-Cu-Sn film growth at the bottom of the solder joint interfaces for ImAg and ENIG/ENEPIG. For 125°C aged samples, the cracks appeared at the corners of both package and board sides of the solder ball and propagated along (near) the IMC location. For the case of aged fine-pitch packages, the failures tended to start at the component side solder ball corner and then propagate along an angled line downwards into the bulk solder.

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Table of Contents

Abstract ii
Acknowledgments iv
List of Table viii
List of Figure ix
Chapter 1 1
General Introduction 1
1.1 SMT components 1
1.1.1 QFP (Quad flat package) 2
1.1.2 QFN (Quad Flat No-lead Package) 3
1.1.3 PGA (Pin Grid Array) 5
1.1.4 BGA (Ball Grid Array) 6
1.2 Trends in Packaging Technology 9
1.3 Substrate 9
1.3.1 Thermal Performance 10
1.3.2 Reliability 11
1.4 Soldering Alloy 11
1.4.1 Tin-Lead solder 13
1.4.2 Lead-Free Solder 13
1.5 PCB Surface Finishes 15
1.6 SMT Assembly 16
1.6.1 Assembly process 16
1.6.2 Affective factors 19
1.7 Testing 21
1.8 Outline of the Dissertation 22
Chapter 2 23
Literature Review 23

2.1 Introduction 23
2.2 Effect on Solder Characteristic Life 25
2.3 The effect of thermal fatigue on solder joints 27
2.4 Microstructural change under thermal fatigue 30
Chapter 3 35
Experimental Approach 35
3.1 Introduction 35
3.2 Test Vehicle (TV7) Design and Assembly 37
3.2.1 Test Board Design 37
3.2.2 Components Selection 39
3.2.3 Solder Paste and Stencils 40
3.2.4 SMT Assembly Processes 40
3.2.5 Inspection Test Vehicle 43
3.3 Thermal Test 44
3.3.1 Test Matrix and Test Conditions 44
3.3.2 Data Acquisition System 46
3.4 Failure Analysis 47
Chapter 4 49
TV7-Phase I Reliability and Failure Analysis 49
4.1 Introduction 49
4.2 Reliability Data Analysis 49
4.2.1 10mm PBGA Package 49
4.2.2 15mm PBGA Package 54
4.2.3 2512 Resistor 58
4.3 Failure Analysis 61
4.4 Discussion and conclusion 69
Chapter 5 70
TV7-Phase II Reliability and Failure Analysis 70
5.1 Introduction 70
5.2 Reliability Data Analysis 70
5.2.1 10mm PBGA Package 70

5.2.2 15mm PBGA Package ... 79
5.2.3 2512 Resistors ... 86
5.3 Failure Analysis ... 92
5.3.1 Surface and Thin Film Analysis ... 92
5.3.2 IMC Analysis and Crack Propagation ... 97
5.4 Discussion and conclusion ... 102
Chapter 6 ... 103
TV-7 Plating Comparison Analysis ... 103
6.1 Introduction ... 103
6.2 Reliability Data Analysis ... 103
6.3 Failure Analysis ... 106
6.4 Discussion and conclusion ... 112
Chapter 7 ... 113
7.1 Literature Review ... 113
7.2 TV7-Phase I Reliability and Failure Analysis ... 113
7.3 TV7-Phase II Reliability and Failure Analysis ... 114
7.4 TV-7 Plating Comparison Analysis ... 114
7.5 Future Work ... 115
7.5.1 Continuous study on TV-7 ... 115
7.5.2 Doping project ... 116
References ... 117

List of Tables

Table 1.1 QFP thermal characteristics 3

Table 1.2 Thermal Performances 4

Table 1.3 Reliability Tests Result of P-PGAs 6

Table 1.4 PBGA Package Attributes [8] 7

Table 1.5 Properties of FR-4 Glass/Epoxy 10

Table 1.6 Properties of relevant materials 11

Table 1.7 Important Characteristics of Solders Alloys 12

Table 1.8 NEMI Users Group PCB Finish Rating [27] 16

Table 1.9 Lead-Free Temperature Profile for MSL Classification [32] 20

Table 2.1 Effects of Design Parameters on the Fatigue Life of BGA 24

Table 3.1 Component Matrix 39

Table 3.2 Pb-Free Solder Paste Parameters in TV7 40

Table 3.3 TV-7 Phase 1 Thermal Testing Plan 44

Table 3.4 TV7 Phase 2 Thermal Testing Plan 45

Table 4.1 Summary of Failure Data 61

Table 4.2 Board-Side, Sn-Cu IMC Layer Thickness vs. Aging Time 64

Table 5.1 Reliability Degradation Rate Summary 91

Table 5.2 SAC305 Board Side IMC Growth during 125°C Aging 98

Table 6.1 12-months aging characteristic lifetime 103

Table 6.2 12-month aging characteristic life degradation rate 105

Table 6.3 SAC305 board side IMC growth during 125°C aging. 108

List of Figures

Figure 1.1 Traditional DIP component 1

Figure 1.2 Plastic Quad Flatpack: PQFP 2

Figure 1.3 Individual Unit Design “Punch” MicroLeadFrame (MLF) 4

Figure 1.4 Thermal dissipation comparisons between QFN and ELP 5

Figure 1.5 Variation of junction temperature and PGA thermal resistance 6

Figure 1.6 Two types of die bonding in BGA packages 7

Figure 1.7 Comparison of BGA and QFP “Footprints” for the same product 8

Figure 1.8 I/O Count within Different Packages 8

Figure 1.9 Packaging Densities over Time 9

Figure 1.10 Survey of the solder market share 15

Figure 1.11 Standard SMT line process flow 17

Figure 1.12 Surface Mount Assembly 17

Figure 1.13 Air flow in a convection dominant system in different zones 18

Figure 1.14 X-ray and thermal Imaging 19

Figure 2.1 Typical fatigue curves 28

Figure 2.2 Typical creep curves 29

Figure 2.3 Typical Stress-Strain curves 30

Figure 2.4 Ag_3Sn Morphology [65] 32

Figure 2.5 Binary phase diagram: (a) Sn–Ag and (b) Sn–Cu 32

Figure 3.1 Package Height Comparisons 35

Figure 3.2 TV7 Design Layout 38

Figure 3.3 Assembled TV7 phase 1 (ImAg, ImSn)........ 38

Figure 3.4 Assembled TV7 phase 2 (ENIG, ENEPIG)........ 38

Figure 3.5 Continental Electronics Prototype Manufacturing Lab 41

Figure 3.6 Reflow Oven........ 42

Figure 3.7 (a) Lead-free Reflow Profile and (b) Tin-Lead Reflow 43

Figure 3.8 Skewed Pad on the left and solder bridging on the right........ 43

Figure 3.9 TCT Testing Profile: (a) -40 to 125℃ (b) -40 to 85℃ 46

Figure 3.10 Schematic design of the monitoring system........ 47

Figure 3.11 SEM schematic figure. 48

Figure 4.1 Weibull plots for Pb-free 10mm BGA packages........ 52

Figure 4.2 Degradation comparison of 10mm SAC105 and SAC305,........ 53

Figure 4.3 Degradation comparison of 10mm package SAC105 and SAC305, aging at 85°C. ... 53

Figure 4.4 Degradation comparison of 10mm package SAC105 and SAC305, aging at 125°C. . 54

Figure 4.5 Weibull plots for Pb-free 15mm BGA packages........ 57

Figure 4.6 Weibull plots and degradation bar charts for 2512 resistors. 59

Figure 4.7 Degradation comparison of 2512 resistors, aging at 85°C and 125°C 60

Figure 4.8 Backscattered electron image for the 0.8mm SAC 105 (a) and SAC305 (b). 62

Figure 4.9 Backscattered electron image for the 0.8mm SAC 105 63

Figure 4.10 Representative backscattered electron images for the 0.8mm pitch Packages. 63

Figure 4.11 Increase in board side 0.8 mm SAC IMC thickness vs. aging time 64

Figure 4.12 Ag_3Sn observations 65

Figure 4.13 EDX Line scan on 0.4mm pitch SAC105 package with 24 months 85°C aging....... 65

Figure 4.14 Low and High mag SEM image of 0.8mm pitch SAC105....................................... 66

Figure 4.15 Failure modes for 0.4 mm pitch SAC alloys. 68

Figure 4.16 Cracks in 2512 SAC305 chip resistor joints... 68

Figure 5.1 Weibull plost for 10mm BGA package subjected to 85°C aging:.............................. 73

Figure 5.2 Weibull plost for 10mm BGA package subjected to 125°C aging............................. 77

Figure 5.3 Summary of 10mm BGA reliability performance.. 78

Figure 5.4 Weibull plost for 15mm BGA package subjected to 85°C aging............................... 82

Figure 5.5 Weibull plost for 15mm BGA package subjected to 125°C aging............................. 85

Figure 5.6 Weibull plost for 2512 resistor package subjected to 85°C aging.............................. 88

Figure 5.7 Weibull plost for 2512 resistor package subjected to 125°C aging............................ 90

Figure 5.8 XPS surface analysis on No aging ENIG board... 92

Figure 5.9 RBS spectra for the starting ENIG (a) and ENEPIG (b) board finishes 93

Figure 5.10 Board-side EDX elemental line scan.. 95

Figure 5.11 Board-side EDX elemental map scan... 96

Figure 5.12 Board-side SAC305 IMC Thickness Growth on ENIG and ENEPIG 98

Figure 5.13 SAC305 (0.8mm pitch) solder joint on ENEPIG. 99

Figure 5.14 SAC305 (0.4mm pitch) solder joint on ENEPIG. 100

Figure 5.15 Representative crack propagation for SAC105 100

Figure 5.16 Representative crack propagation for SAC105. 101

Figure 5.17 Representative crack propagation for SAC305. 101

Figure 6.1 Characteristic lives for 15mm BGA subject to 125°C/12 months aging.................. 104

Figure 6.2 Characteristic life for 10mm BGA subject to 125°C/12 months aging.................... 104

Figure 6.3 Characteristic life for 2512 resistors vs. aging time for three surface finishes. 106

Figure 6.4 Observed cracks in chip resistor joints as a function of thermal cycles. 107

Figure 6.5 Board-side SAC305 IMC thickness on ImAg, ENIG, and ENEPIG. 108

Figure 6.6 Representative crack propagation for SAC105. 110

Figure 6.7 Representative crack propagation for SAC105 110

Figure 6.8 Kirkendall voids in 0.4mm pitch SAC305 solder on ENIG. 111

Chapter 1

General Introduction

1.1 SMT components

Surface mount technology (SMT) minimized the limitations of weight, volume, and reliability for electronic assemblies compared to conventional electronic manufacturing. SMA mounts electronic components on the surface of printed circuit boards (PCB) or substrates while conventional technology inserts components through holes in the PCB. Such deceptively simple differences change virtually every aspect of electronics design, process assembly, component packages, and substrates [1].

The component package, in addition to saving space and providing better electrical performance, serve many other functions. The packages protect the devices within them from the environment, provide communication links, remove heat, and offer a safe means for handling and testing. We illustrate several types of SMT components in the following. Figure 1.1 showed a DIP component.

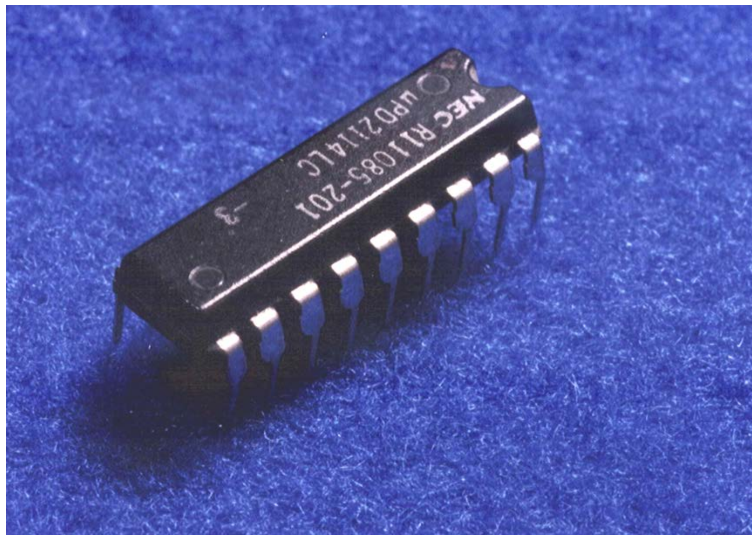


Figure 1.1 Traditional DIP component

1.1.1 QFP (Quad flat package)

QFP's are 4-side-pin flat packages. Substrates usually are ceramic or metal but plastic is used in package technology known as PQFP (plastic quad flat package). Typical pitch sizes are 1.0mm, 0.8mm, 0.65mm, 0.5mm, 0.4mm, 0.3mm. Up to 304 pins are attached with the 0.65mm specification. Some LSI manufacturers consider QFP-type or SQFP (small quad flat package) and VQFP (very small quad flat package) as fine pitch (< 0.5mm) but other vendors define SQFP packages as those having 0.65mm and 0.4mm pitches. Figure 1.2 showed a PQFP package. Because the structure of QFP requires a lead frame (L/F), the setup for electrical performance is minimally adjustable. Furthermore, with the higher lead density, the wiring density and series resistance (joule heating) during test are also increased significantly. In order to acquire high performance, heat sinks are generally necessary to improve the power dissipation.

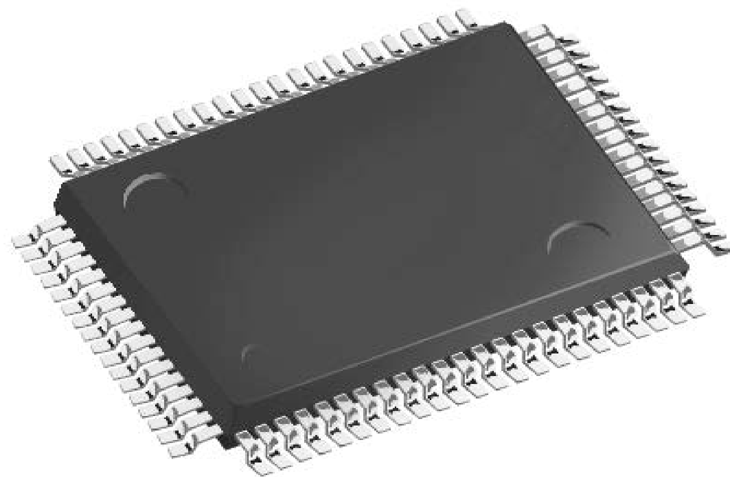


Figure 1.2 Plastic Quad Flatpack: PQFP

The testing of QFP packages is equally important before being put into production. During the test period, several kinds of tests are employed. One is termed the pull and drop test. During the pull test, the leads of the package are pulled up one-by-one until failure. In the drop test, continuous dropping movements are performed until certain components drop off the board [2]. Table 1.1 demonstrated a list of thermal characteristics.

Table 1.1 QFP thermal characteristics [1]

Type	Pin count	PKG size [mm]	Die size [mm]	Lead Frame material	Thermal Test Board Layers	0m/s		1m/s		2m/s	
						θja (°c/w)	Ψjt (°c/w)	θja (°c/w)	Ψjt (°c/w)	θja (°c/w)	Ψjt (°c/w)
QFP	208	28x28	5.5x5.5	Cu(t=0.150)	4	35	0.97	28	1.70	26	2.03
QFP	208	28x28	5.5x5.5	Cu(t=0.150)	2	39	0.99	30	1.74	27	2.09
QFP	208	28x28	6.6x6.6	Cu(t=0.150)	4	34	0.75	27	1.44	25	1.78
QFP	208	28x28	6.6x6.6	Cu(t=0.150)	2	38	0.77	29	1.50	26	1.84
QFP	208	28x28	7.7x7.7	Cu(t=0.150)	4	32	0.56	25	1.21	23	1.52
QFP	208	28x28	7.7x7.7	Cu(t=0.150)	2	36	0.59	27	1.27	24	1.58
QFP	208	28x28	7.71x7.71	Cu(t=0.150)	4	34	0.46	27	1.16	24	1.50
QFP	208	28x28	7.71x7.71	Cu(t=0.150)	2	38	0.48	29	1.22	26	1.56
QFP	208	28x28	8.8x8.8	Cu(t=0.150)	4	33	0.39	26	1.07	24	1.41
QFP	208	28x28	8.8x8.8	Cu(t=0.150)	2	37	0.41	28	1.13	25	1.47
QFP	208	28x28	9.7x9.7	Cu(t=0.150)	4	32	0.33	25	0.99	23	1.30
QFP	208	28x28	9.7x9.7	Cu(t=0.150)	2	36	0.35	27	1.05	24	1.37
QFP	208	28x28	9.71x9.71	Cu(t=0.150)	4	30	0.28	23	0.88	21	1.17
QFP	208	28x28	9.71x9.71	Cu(t=0.150)	2	34	0.30	25	0.94	22	1.24
QFP	208	28x28	10.7x10.7	Cu(t=0.150)	4	30	0.25	23	0.84	21	1.15
QFP	208	28x28	10.7x10.7	Cu(t=0.150)	2	34	0.27	25	0.90	22	1.19
QFP	208	28x28	11.7x11.7	Cu(t=0.150)	4	29	0.22	22	0.79	20	1.06
QFP	208	28x28	11.7x11.7	Cu(t=0.150)	2	33	0.23	24	0.85	21	1.12
QFP	208	28x28	11.71x11.71	Cu(t=0.150)	4	27	0.19	21	0.72	18	0.96
QFP	208	28x28	11.71x11.71	Cu(t=0.150)	2	31	0.21	22	0.78	20	1.02
QFP	208	28x28	12.7x12.7	Cu(t=0.150)	4	27	0.18	20	0.69	18	0.93
QFP	208	28x28	12.7x12.7	Cu(t=0.150)	2	31	0.19	22	0.75	19	0.99
QFP	208	28x28	13.7x13.7	Cu(t=0.150)	4	26	0.16	19	0.65	17	0.88
QFP	208	28x28	13.7x13.7	Cu(t=0.150)	2	30	0.17	21	0.71	18	0.94
QFP	208	28x28	13.71x13.71	Cu(t=0.150)	4	26	0.15	19	0.63	17	0.84
QFP	208	28x28	13.71x13.71	Cu(t=0.150)	2	30	0.16	21	0.69	18	0.90
QFP	208	28x28	14.7x14.7	Cu(t=0.150)	4	25	0.14	19	0.61	16	0.82
QFP	208	28x28	14.7x14.7	Cu(t=0.150)	2	29	0.15	20	0.67	18	0.88
QFP	208	28x28	15.7x15.7	Cu(t=0.150)	4	25	0.12	18	0.58	16	0.78
QFP	208	28x28	15.7x15.7	Cu(t=0.150)	2	29	0.14	20	0.64	17	0.84

1.1.2 QFN (Quad Flat No-lead Package)

QFN is a surface-mount chip package technology whose name derives from its small body and pad size, and by using plastic as encapsulation material. It usually is square or rectangular in shape, with an exposed thermal pad at the center of the package bottom which improves heat transfer out of the chip. Unlike the traditional SOIC and TSOP packages with gull-wing shaped leads, the QFP provides excellent electrical performance because of its reduced self-inductance and low wiring resistance, deriving from shorting the path between the internal pins and the pad. The exposed copper die-pad absorbs the excess heat from the thermal via in the PCB, which offers good thermal performance [3]. Figure 1.3 showed the structure of MLF package.

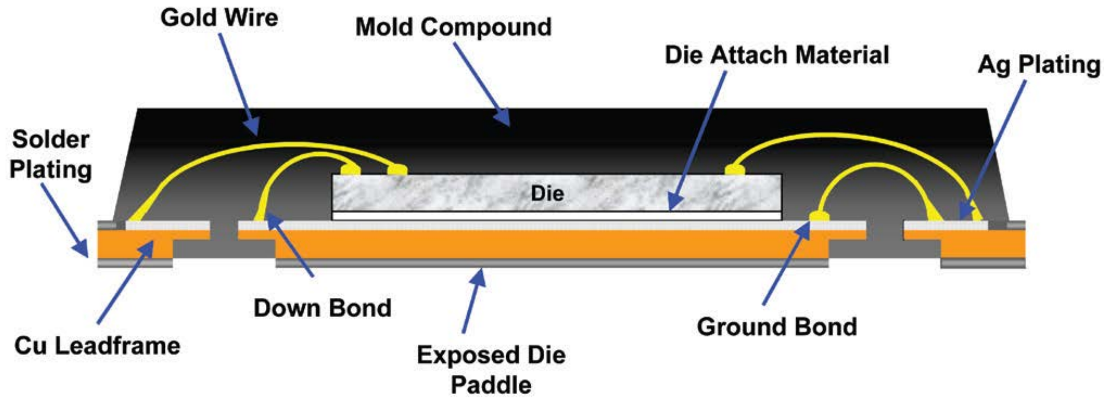


Figure 1.3 Individual Unit Design "Punch" MicroLeadFrame (MLF) [3]

Table 1.2 and Figure 1.4 gave the list of QFN thermal performance. From the reliability respective, QFN packaging offers several advantages. The CTE of the mold compound is a major factor which affects the board reliability. Pulling the leads back does not reduce the package reliability as the land length is the same. Environment and life testing studies demonstrate that QFN package technology survives in a variety of harsh environments [4].

Table 1.2 Thermal Performances [1]

THERMAL PERFORMANCE, θja (°C/W)

Package	Body Size (mm)	Pad Size (mm)	Die Size (mm)	*Thermal Performance θja(°C/W)	Thermal Vias (on test board)
48L UQFN	7 x 7 x 0.50	5.1 x 5.1	2.26 x 2.26	26.3	25
64L QFN	9 x 9 x 0.85	7.3 x 7.3	4.52 x 4.52	19.2	36
76L QFN-dr	8 x 8 x 0.85	5.28 x 5.28	4.52 x 4.52	26.6	16

Note: Simulation data for package mounted on 4 layer PCB (per JEDEC JESD51-7) under natural convection as defined in JESD51-2.

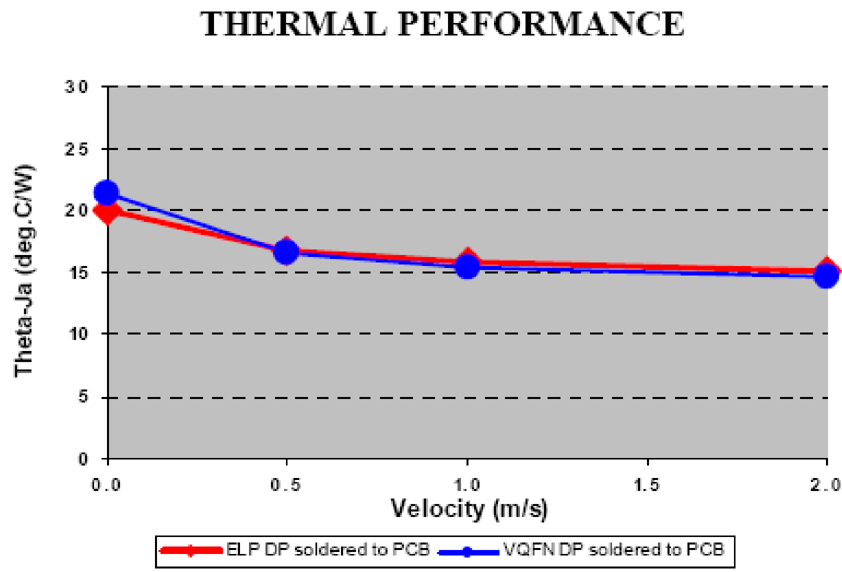


Figure 1.4 Thermal dissipation comparisons between QFN and ELP

1.1.3 PGA (Pin Grid Array)

Starting with the Intel 80286, most second through fifth generation processors used PGA packaging technology. PGA packages are usually square or rectangular and have two or more rows of pins numbering from 64 to 447 [5] with fine pitches (1.27mm and 2.45mm).

Thermal analysis of a pin grid array chip package is also crucial and heat sinks are necessary in most packaging applications. The thermal resistance of the package can be efficiently decreased by optimizing the PGA assembly. See Figure 1.5 and Table 1.3 for thermal performance of PGA packages. Reliability tests have been done for fine pitch P-PGAs. The tests are usually broken into two parts—one involving temperature cycling under high temperature/high humidity conditions and a second test for electromigration [6-7].

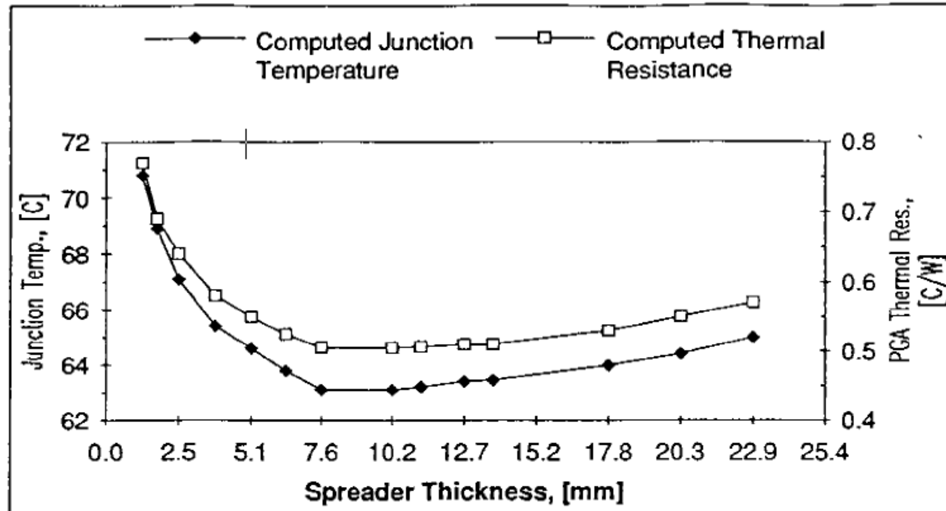


Figure 1.5 Variation of junction temperature and PGA thermal resistance with spreader thickness [6]

Table 1.3 Reliability Tests Result of P-PGAs [6]

	Temperature Cycle (-55℃ ◄—► 150℃)				High Temperature (125℃)		High Temperature/humidity (65℃/95%)	
	0	2000	3000	4000 cycles	0	2000 hours	0	2000 hours
Ni 3 μm	0/10 pkgs	0/10	3/10	10/10	0/9	0/9	0/8	0/8
5 μm	0/10	0/10	3/10	10/10	0/6	0/6	0/6	0/6
12 μm	0/10	0/10	4/10	10/10	0/9	0/9	0/9	0/9
*240pin P-PGA	0/9	5/9	9/9	-	-	-	-	-

1.1.4 BGA (Ball Grid Array)

In a BGA, I/O terminals are replaced by rows of solder balls distributed below the package. BGA packaging technology can be classified into five categories:

- PBGA (plastic BGA) substrate: Generally multilayer composed of 2-4 layers of organic materials. The Intel series Pentium II, III, IV processors all use this package. (See Figure 1.6)
- CBGA (ceramic BGA) substrate: Uses a ceramic substrate, with electrical connections between chip and substrate installed by flip-chip (FC). The Intel series Pentium I, II, Pentium Pro processors utilize CBGA technology.

- FCBGA (flip chip BGA) substrates: Uses a rigid multi-layer substrate.
- TBGA (tape BGA) substrates: Contains a substrate composed by 1-2 band-shape of soft-layer PCB.
- CDPBGA (cavity down PBGA) substrates: Refers to packaging with a concave area in the center.

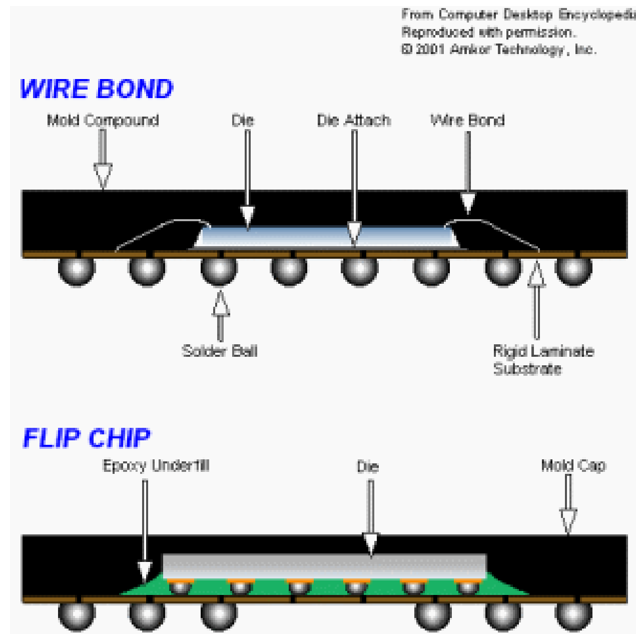


Figure 1.6 Two types of die bonding in BGA packages

Table 1.4 PBGA Package Attributes [8]

	PBGA										
Lead Count	196 (15mm)	208 (23mm)	241 (23mm)	256 (17mm)	256 (27mm)	304 (31mm)	324 (27mm)	421 (31mm)	468 (35mm)	492 (35mm)	544 (35mm)
Sq/Rect.	S	S	S	S	S	S	S	S	S	S	S
Pitch (mm)	1.0	1.27	1.27	1.0	1.27	1.27	1.27	1.27	1.27	1.27	1.27
Package Thickness (mm)	1.61	2.33	2.38	1.56	2.13	2.33	2.13	2.38	2.38	2.38	2.38
Weight (gm)	.67	1.56		.70		3.46	2.86	3.87	5.06		
Max. Footprint (mm)	15.20	23.20	23.20	17.20	27.20	31.20	27.20	31.20	35.20	35.20	35.20
Shipping Media:											
Tape & Reel	X	X	X				X	X	X	X	X
Trays	X	X	X	X	X	X	X	X	X	X	X
Desiccant Pack	X	X	X	X	X	X	X	X	X	X	X
Comments/ Footnotes											

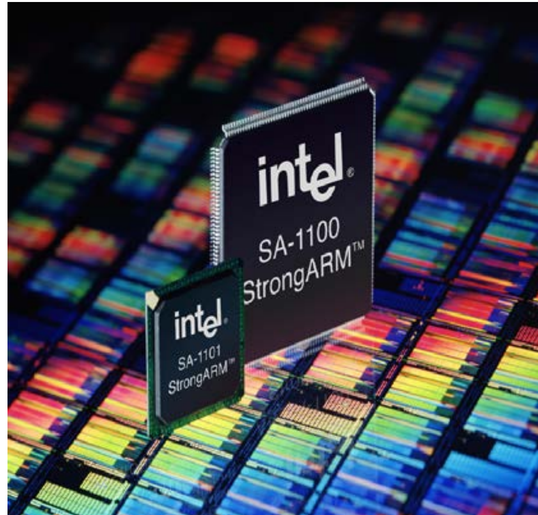


Figure 1.7 Comparison of BGA and QFP "Footprints" for the same product [8]

The Comparison of BGA and QFP was shown in Figure 1.7. In general, BGA technology provides an optimum solution to the manufacturing problem of packaging an integrated circuit with hundreds of pins. The electrical performance of BGAs is typically better than the pinned packages because of the lack of long pins and fine-line laminate base. The solder balls shorten the conducting plane/ground plane distance and reduce parasitic electrical signals. Figure 1.8 shows the I/O counts of packages.

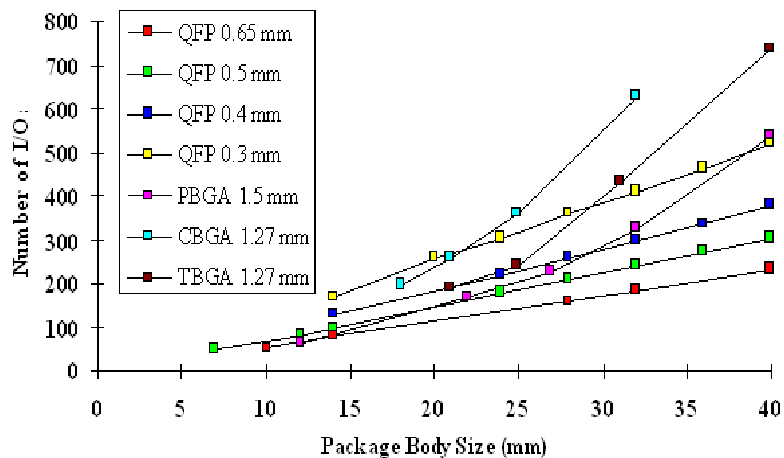


Figure 1.8 I/O Count within Different Packages [9]

1.2 **Trends in Packaging Technology**

Through-hole packaging was the mainstream technology during the early era of microelectronics in the 1970's. With the increasing chip integration required of modern circuitry, however, through-hole technology is at the edge of elimination. Surface mount technology (SMT) has rapidly developed as a replacement. The pin grid array (PGA) is playing a crucial role with its area array interconnections, as is the ball grid array (BGA) package, which came into prominence in the late 1980s and early 1990s.

Figure 1.9 introduced the Packaging Densities over Time. In the late 1990s, wafer level packaging was introduced, resulting in many revolutionary advances such as chip-on-board (COB), tape-automated bonding (TAB), and multichip modules (MCMs). These technologies represent the next step in the evolution of packaging [9].

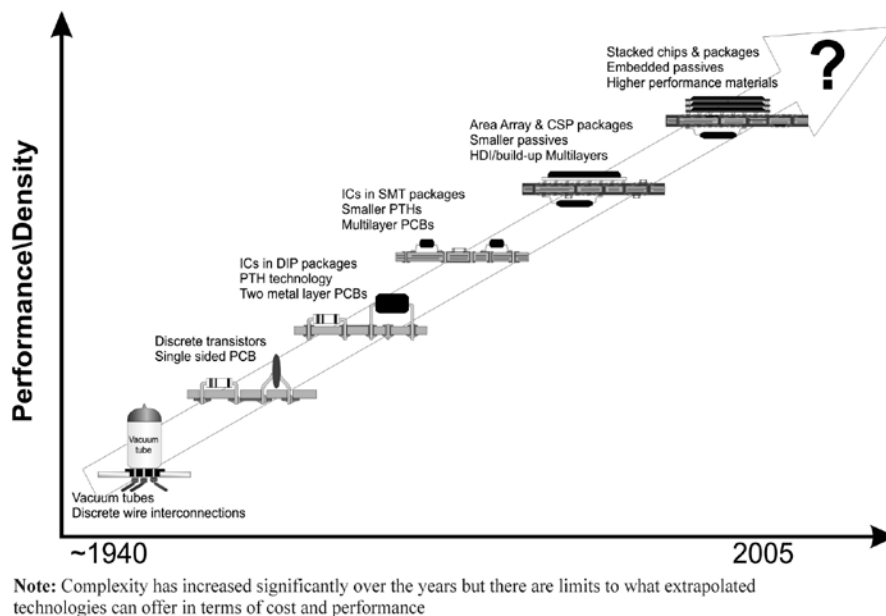


Figure 1.9 Packaging Densities over Time [9]

1.3 **Substrate**

Glass epoxy substrates have been widely used in single, double, and multilayer PCB for commercial and military applications. The substrate is composed of epoxy and glass fibers which provide the structural stability and ductility for the laminate.

FR-4 laminate is a composite of glass fabric impregnated with epoxy resin and copper foil.

"FR" stands for flame retardant and type "4" indicates woven glass reinforced epoxy resin. The FR-4 thickness is usually designated by "half-ounce" (~ 18 microns) or "one-ounce" (~ 35 microns). In general, the foil, formed by electrodeposition, has one surface electrochemically roughened to improve adhesion [10-12].

Table 1.5 Properties of FR-4 Glass/Epoxy [11]

Property	Units	FR-4 Glass/Epoxy
Physical		
Specific Gravity	-	1.80
Moisture Absorption (.062")	%	0.15
Mechanical		
Rockwell Hardness (.062")	M Scale	110
Flexural Strength (.062") LW CW	psi psi	70,000 60,000
Flexural Modulus (.062") LW CW	psi psi	2,700,000 2,400,000
Tensile Strength (.125") LW CW	psi psi	45,000 38,000
Izod Impact Strength E-48/50 (.500") LW CW	ft-lb/in ft-lb/in	14.0 12.0
Compressive Strength flatwise (.500")	psi	55,000
Bond Strength (.500")	lbs	2,200
Shear Strength (perpendicular) (.062")	psi	22,000
Thermal		
Maximum Operating Temperature	°F	284
Coefficient of Thermal Expansion (.062") X-axis Y-axis	in/in/°F in/in/°F	5.5 x 10^-6 6.6 x 10^-6
Flammability Rating - U. L. 94		V-0
Electrical		
Permittivity (.062") Condition D-24/23	-	4.80
Dissipation Factor (.062") Condition D-24/23	-	.025
Breakdown Voltage Condition - A (.062") D-48/50	V	65,000 54,000
Electric Strength Condition - A (.062") D-48/50	V/mil	800 750
Arc Resistance (.125") D-495	sec	100
Comparative Tracking Index (.125") D3638	-	150
Tg	°F	261

1.3.1 Thermal Performance

Studies show that the expansion coefficient of FR-4 laminate is about 16 ppm/^{o}C (copper 17-18ppm, glass fiber 5-7ppm, resin 40ppm). Depending on the resin chemistry, the glass transition temperature (Tg) of FR-4, where the resin changes from a glassy to a plastic state, is within a temperature range from 120°C to 180°C. Above Tg, the expansion coefficient of epoxy resin is roughly 330 ppm/^{o}C along the z axis (which is not reinforced). The continuous recommended operating temperature for FR4 is typically 130°C [13, 14]. Table 1.6 shows the properties of relevant materials.

Table 1.6 Properties of relevant materials [1]

Properties	Copper	Silver	Gold	Tin	96.5Sn3.5Ag
Melting point (°C)	1083	961	1063	231	221
Density (g/cc)	8.94	10.5	19.3	7.29	7.4
Thermal conductivity (W/cm K)	3.862	4.075	3.151	0.665	0.78
Electrical conductivity (/Ω cm)	5.88×10^5	6.25×10^5	4.17×10^5	0.87×10^5	0.812×10^5
Thermal expansion coefficient (/°C)	16.42×10^{-6}	18.6×10^{-6}	14.2×10^{-6}	22.2×10^{-6}	30.2×10^{-6}
Yield strength (psi)	10,000	1000	250	1300	3600
Ultimate tensile strength (psi)	32,000	21,000	17,000	2000	5000–7000
Young's modulus (psi)	1.92×10^7	1.18×10^7	1.12×10^7	6.89×10^6	7.8×10^6
Elongation at break (%)	51	50	50	50–80	37
Hardness (Brinell)	37	25	18.5	3.7	14.8

1.3.2 Reliability

Silver (Ag) bonding to copper (Cu) substrates is an important methodology in electronic packaging where Cu substrates/electrodes are used for bonding semiconductor device chips within the package. Ag/Cu bonding offers several advantages such as high strength, high electrical and thermal conductivity, adequate rigidity, ease in machining, and low cost. A downside is the significant coefficient of thermal expansion (CTE) mismatch between Cu and Si which causes bonding failure in temperature cycled applications. To remedy this, Ag, which is soft and ductile, functions as a strain buffer between the Cu substrate and the semiconductor chip; in addition, Ag is the highest electrical and thermal conductive material among all metals [15]. The solution involves choosing a material that has high thermal conductivity and also matches the CTE of silicon.

1.4 Soldering Alloy

Soldering is a metallurgical joining process in which two or more metals are permanently connected by melting a filler metal into the joint. The filler metal with melting point below 425℃ is called solder [16]. The solder used in electronic SMT assemblies serves to provide a robust electrical and mechanical connection [1]. There are two crucial selection criteria for solder—melting point and mechanical strength. The properties of the solder itself depend on the composition and microstructure of the specific alloy. When speaking of solder reliability, the fatigue resistance (mean cycles to failure) plays a central role. In fact, there are few significant differences between the tensile strengths of different solders. For a given solder, the shear strain,

stress/strain variation, and the temperature are the major factors which determine the fatigue resistance of a solder joint [17]. The important characteristics of solders both for manufacturing and reliability are summarized in Table 1.7.

Table 1.7 Important Characteristics of Solders Alloys [16]

Manufacturing	Reliability
Melting/liquidus temperature	Electrical conductivity
Wettabilitty (of copper)	Thermal conductivity
Cost	Coefficient of thermal expansion
Environmental friendliness	Shear properties
Availability and number of suppliers	Tensile properties
Manufacturability using current processes	Creep resistance
Ability to be made into balls	Fatigue properties
Copper pick-up rate	Corrosion and oxidation resistance
Recyclability	Intermetallic compound formation
Ability to be made into paste	

1.4.1 Tin-Lead solder

Historically, the most universal solder is eutectic solder with 63% tin and 37% lead (by weight) with a melting point of 183°C. The cost of eutectic (63Sn/37Pb) solder is more than 60Sn/40Pb solder because tin is more expensive than lead, but both solder stoichiometries have good performance in wave soldering applications. For SMT, eutectic solder is optimum since it is the lowest melting point combination of the alloying elements. Sn-Pb solders have the following advantageous properties [18, 19]:

- Pb is inexpensive and readily available. Sn-Pb alloys have relatively low melting temperatures which allow low reflow temperatures, which avoid exposing delicate boards and components to high temperatures.
- Pb improves the wetting ability by reducing the surface tension of pure tin.
- Pb prevents the transformation of β-tin to α-tin, which will cause a 26% volume increase and loss of structural integrity. Pb also lends ductility to Sn-Pb solder alloys.
- As a solvent metal, Pb helps tin and copper form intermetallic bonds by diffusion.

1.4.2 Lead-Free Solder

Despite the near-universal application of Sn-Pb solders historically, recent medical studies have shown that lead is a heavy metal toxin that can damage the kidneys, liver, blood, and central nervous system, and result in disorders of the nervous and reproductive systems and delayed neurological and physical development, particularly during the neurological development of youth. Less than one percent per year of the global lead consumption is used in solder alloys for electronic products but electronics and electrical systems make up an increasingly larger fraction of landfills [20]. International laws have recently been passed to limit or ban the use of lead in manufactured products. The most aggressive and well-known regulation is the European Union's Waste in Electrical and Electronic Equipment directive, which proposed a ban on lead in electronics by 2008. The Japanese Environmental Agency has directed that lead-containing scrap must be disposed of in sealed landfills to prevent lead leaching. The Japanese Ministry of International Trade and Industry and the Japan Automobile Industries Association called for a 50% reduction of lead in vehicles (excluding batteries) by 2001 and a 33.3% reduction by 2003 [21]. In the United States, the U.S. Environmental Protection Agency (EPA)

and IPC (Institute of Interconnecting and Packaging Electrical Circuits) proposed a roadmap for the lead-free movement in U.S. [22].

Because Sn-Pb solders are currently being phased out of consumption, it has been important to develop requirements for an alternative solder alloy [23]. The most important requirements are:

- Low Melting Point: The melting point should be low enough to avoid thermal damage to the assembly being soldered and high enough for the solder joint to bear the operating temperature. The solder should retain adequate mechanical properties at these temperatures.
- Wettability: The good metallurgical bond between the solder and the base metal is formed when the solder wets the base metal properly. A high Sn content insures this.
- Availability: There should be adequate worldwide supplies or reserves available of candidate metals. Sn, zinc (Zn), copper (Cu) and antimony (Sb) are available whereas there is a limited supply of indium (In), for example.
- Cost: Manufacturers of electronic systems are unlikely to change to an alternative solder with an increased cost unless it has demonstrated better properties or there is legislative pressure to do so.

In the quest for new lead-free solders with better properties, researchers frequently add trace amounts of elements into Sn-based solders (Ag, Cu, Zn, and a host of others currently being studied). Generally speaking, the elemental additives yield better solder performance when it comes to wettability, creep resistance, and tensile strength. Indeed, some doped alloys increase the creep resistance and rupture time by over 4 times for Sn–Ag and 7 times for Sn–Cu and Sn–Ag–Cu [24, 25]. Soldertec's [26] survey (below) shows that the most popular Sn-Ag-Cu (SAC) alloys which consist of 3.0–4.0% Ag and 0.5–1.0% Cu provide benefits deriving from their low melting temperatures and superior mechanical and solderability properties when compared to other Pb-free solders. Figure 1.10 clearly demonstrated market share of (a) different lead-free solders and different types of SAC alloys.

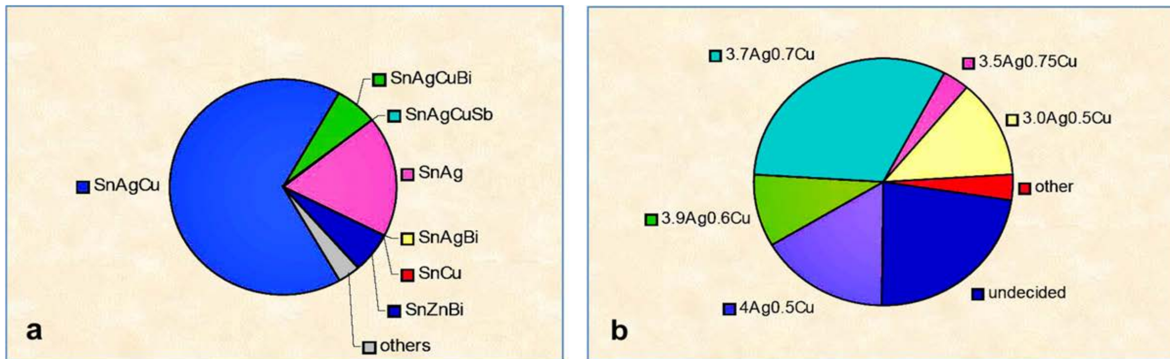


Figure 1.10 Survey of the market share of (a) different lead-free solders and (b) different types of SAC alloys

1.5 PCB Surface Finishes

Regulations established by RoHS required compliance of manufacturers to use Pb-free finishes. The leading finishes are hot air solder leveling (HASL), organic solderability preservative (OSP), immersion tin (ImSn), immersion silver (ImAg) and electroless-nickel immersion gold (ENIG). Table 1.8 illustrated the "pros and cons" of different platings.

- HASL has been the predominant surface finish for a long time. The process consists of dipping circuit boards in a molten tin/lead alloy bath followed by removal of the excess solder by blowing hot air across the board. It is the lowest cost finish, but lacks precise thickness control and the PCB receives a thermal shock during the dip.
- OSP is composed of a thin protective layer of organic (carbon) over copper. OSP finishes are inexpensive, provide good surface oxidation, coplanarity, and process control. The drawbacks are poor shelf life, rapid degradation with temperature, poor wettability, and very poor electrical testability.
- ImSn is another alternative Sn surface finish but has limited application due to its poor performance over reflow cycles.
- ImAg offers good wettability, good shelf life, and good coplanarity and is suitable for multi-process reflow, but suffers from slow adoption in the industry.
- The properties of ENIG are the best among lead-free board finishes. It has excellent wettability and coplanarity, excellent surface oxidation resistance, and good electrical testability. The disadvantage of ENIG is its higher cost and it can suffer "black pad" whereby the nickel layer breaks up during mechanical stress.

Table 1.8 NEMI Users Group PCB Finish Rating [27]

Finish	Recommend	Risky	Not Acceptable	No Vote
Immersion Ag	6	2	0	1
Immersion Sn	5	3	0	1
OSP	5	2	1	1
ENIG	4	2	2	1
HASL (SnCu)	2	4	0	3

1.6 SMT Assembly

1.6.1 Assembly process

The SMT manufacturing process is the central part of the entire SMT packaging technology. The standard process flow is shown in Figure 1.11 [28].

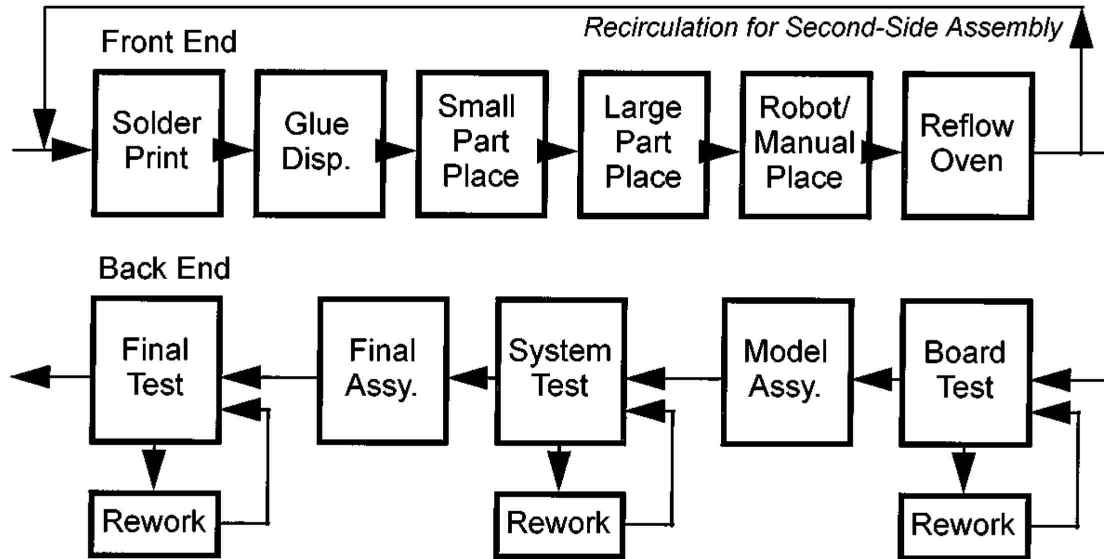


Figure 1.11 Standard SMT line process flow [1]

One can subdivide the process into two parts, front end and back end. In the front end, electronic components are assembled onto printed wiring boards (PWBs). Solder paste is printed and glue (required only for heavy parts on double-sided boards) dispensed onto the board, then the components are placed and the solder is reflowed to establish electrical and mechanical contact of the components and board. At the back end, the finished printed wiring board is assembled into a finished product like cellular phone or MP3 player.

Figure 1.12 Surface Mount Assembly

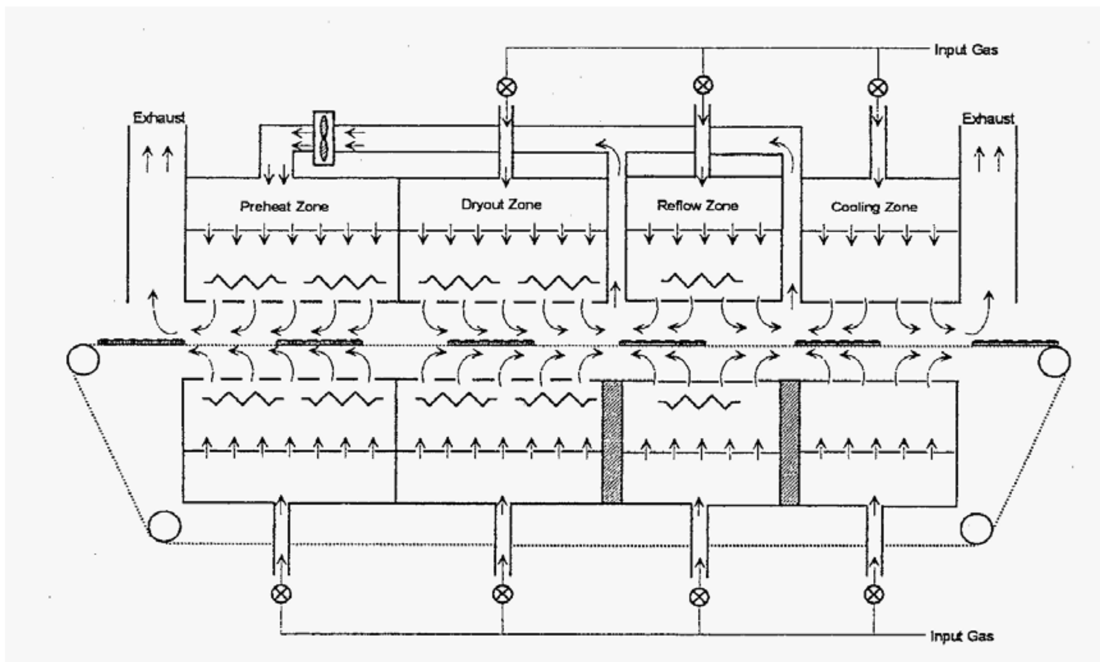


Figure 1.13 Air flow in a convection dominant system in different zones [1]

Figure 1.13 showed the reflow oven structure. The SMT packaging process can be achieved reliably if several process requirements are implemented carefully. Here is a summary of the key variables in the SMT process.

1. Low melting temperature of alloy
2. Flux chemistry - activation, temperature effects
3. Wetting and surface tension properties of the alloy
4. Solder balling and bridging potential increases
5. Component / board reliability
6. Compatible rework / repair
7. Compatible wave, selective soldering processes
8. Quality inspection criteria modifications
9. Cosmetic effects of flux at higher reflow temperatures
10. Nitrogen versus air reflows
11. Pin-testability of flux residues
12. Solder voids impact
13. Residue cleaning / removal process changes
14. Conformal coating and under fill compatibility

15. Oven maintenance, flux decomposition volumes

X-ray inspection (Figure 1.14) is now commonly used in the SMT production to check for process and solder related defects [29].

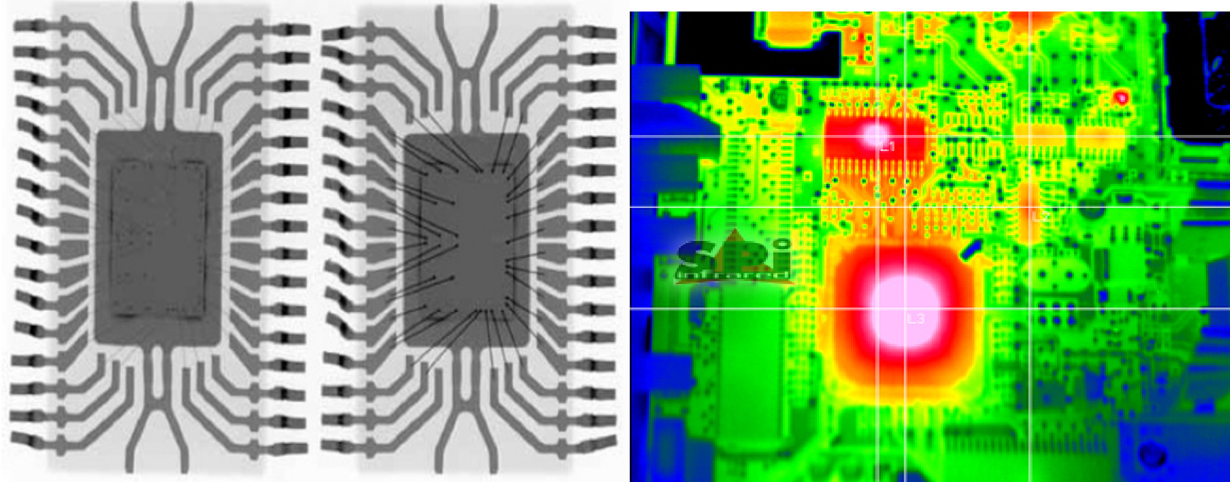


Figure 1.14 X-ray and thermal Imaging [29]

1.6.2 Affective factors

One goal of SMT process research is to determine the appropriate operating ranges for the equipment in an SMT line and to use board-to-board measurements of solder print quality, placement accuracy, and yield to determine the operational status of the equipment after the reflow process. Component, board, and equipment manufacturers are all impacted by research into improved manufacturing processes [30, 31]. Furthermore, selection of the optimum solder paste for specific SMT processes is critical. The properties below offer a guide to engineers to determine the best solder. It is important for the process engineer to determine which attribute is most critical in the process.

1. Print speed
2. Abandon time
3. Stencil life
4. Tack life
5. Solder ball potential
6. Slump, cold and hot

7. Spread on various metallization
8. Solderability on various finishes
9. Reflow window
10. Voiding potential
11. Double reflow window capability
12. Clean-ability, if water washable paste
13. Pin-testability, if no clean paste

Table 1.9 Lead-Free Temperature Profile for MSL Classification [32]

Thermal Profile Features	Small Devices	Large Devices	Very Large Devices
PREHEAT			
Ramp-up rate to 150℃	Minimum 3K/sec Average value over 10 sec		
Time From 190-200℃	Minimum 110 sec		
PEAK			
Ramp-up rate from 200℃ to Peak temp	0.5K/sec, average value over 10 sec		
Time above Liquidus. 217℃	Minimum 90 sec		
Peak Temperature	260℃`	250℃	245℃
Time above Peak temp	Minimum 40 sec	Minimum 30 sec	Minimum 30 sec
COOLING			
Ramp down from Solidus temp. 217℃	Minimum 6K/sec Average value over 10 sec		
GENERAL INFO.			
Time 25℃ to Peak temp	Minimum 300 sec		

The classification of non-hermetic solid-state SMD components may change when hotter preheats and higher peak temperatures are part of the process, and component reliability during reflow soldering can be affected by moisture. Delamination, cracks, bond-lifting, die lifting, and, in extreme cases, pop-corning effects can occur. Factors such as process speed, the equipment capacity and assembly accuracy significantly affect the throughput of a product. Table 1.9 provided the Lead-Free Temperature Profile for MSL Classification. [32]

1.7 Testing

The reliability and lifetime of different packages is one of the most important questions in SMT applications. The limited availability of reliability data of new component package styles and types has slowed widespread use of them. This is because few independent evaluations have been performed and because the reliability of FC, QFP, PGA, and CSP packages is much more complex than the reliability of conventional package types such as PLCCs and QFPs. To reduce the test time and cost it is necessary to accelerate the failure processes and determine mathematical and physical models for evaluating the test results [33]. Standard acceleration tests include:

- Temperature cycling: Accelerated thermal cycling is generally used to compare the performance of different packages. It is also used to detect any latent process defects that may be present in the first few cycles and to determine a wear-out (i.e., fatigue) failure distribution for the given device and environment. The test conditions are accelerated by using cycle times and temperatures over and above what the actual use requires.
- Thermal shock: Thermal shock testing can be divided into two main types. One type consists of an air chamber in which the specimen is alternately exposed to hot air and cold air. The other type consists of a liquid bath in which the specimen is alternately exposed to a hot liquid and a cold liquid.
- Drop: The drop test examines the mechanical integrity of the package and/or assembly under a mechanical shock. It uses machines to generate shock with such methods as free fall and elastic rebound. For special (military) purpose products, a common method is to perform MIL standards half sine shock testing.

- Vibration: Vibration testing shakes circuit boards by using sine wave testing to random wave testing and shock testing. This provides testing that more closely resembles the actual environment.

1.8 Outline of the Dissertation

This dissertation is divided into the following chapters:

- Chapter 1: Introduction to Surface Mount Technology, electronics packaging evolution, and SnPb/Pb-free soldering alloys, board finishes, and SMT process.
- Chapter 2: Literature review on the lead-free assembly process, microstructural changes of solder joints, and elevated thermal aging effects.
- Chapter 3: Description of the test vehicle, SMT assembly process, and experimental setup.
- Chapter 4: Effect of long term aging on the thermal reliability of TV-7 (Test Vehicle 7) phase 1 and microstructure evolution analysis.
- Chapter 5: Description of the data analysis and failure analysis of testing vehicle phase 2.
- Chapter 6: TV-7 Plating Comparison Analysis.
- Chapter 7: Summary and conclusions.

Chapter 2
Literature Review

2.1 Introduction

Flip chip technology gains its increasingly acceptance as an electronic packaging option in most industries is because it can handle sufficient amount of input/output interconnects in a small die footprint. The structural stability of solder joints in this package is critical. The solder joints provide mechanical support and electrical interconnection but are weak links in the overall package reliability under the combined application of mechanical, chemical, and electrical loads. In the past, eutectic or near eutectic Sn-37Pb solder has been commonly used due to its good solderability and reliability performance. The implementation of WEEE/ROHS legislation in Europe mandating a transition from conventional eutectic Sn-37Pb (Tm = 183°C) solder to Pb-free electronics, however, creates significant concerns for long term reliability.

In general, solder materials exposed to thermal-mechanical fatigue, such as temperature excursions, vibration, and shock during service causes the failure or function loss of the electronic hardware. Hundreds of studies addressing the thermal-mechanical properties of SAC alloy have been performed. Microstructure evolution and deformation caused by globally mismatched coefficients of thermal expansion (CTE) between components and printed circuit boards, and local CTE differences in various phases or grains in the solder [34] has been two of the primary factors which reduce the package reliability.

The studies largely focus on the mechanical property change and microstructural evolution of solder joints subjected to accelerated thermal mechanical test conditions. Only limited attention has been paid to the effect of package characteristic lifetime reliability under long term isothermal aging at elevated temperatures, which is the subject of this dissertation. Several challenges are involved with this type of experiment. First, it is difficult to obtain accurate mechanical properties of bulk solder, especially as a function of long times over high temperatures. Second, there are considerable variations in real electronics packages, with large deviations in experimental designs, die sizes, package sizes, ball counts, pitches, mold compounds, and substrate materials. Third, the effect of different environmental stress on the microstructure and thermal-mechanical reliability requires labor/equipment intensive experiment over months and years of time [35].

Table 2.1 Effects of Design Parameters on the Fatigue Life of BGA

No.	Design Parameters	Effects (Life Improvement)
1	Die size	Smaller (significant)
2	Die thickness	Thinner (little)
3	Ball standoff	Higher (significant)
4	Max. ball diameter	Smaller (significant)
5	Solder mask opening	Bigger (significant)
6	Board size	Smaller (little)
7	Board thickness	Thinner (significant)
8	Substrate thickness	Thicker (little)
9	Mold Compound thickness	Thinner (little)
10	Mold Compound modules	Lower (little)
11	Mold compound CTE	Higher (significant)

The industry interest in long-term reliability has motivated more researchers to develop long-term testing protocols, but the field is still in its infancy. Table 2.1 showed Design Parameters on the Fatigue Life of BGA. More accelerated tests and field data are necessary before drawing general conclusions about the long-term reliability of Pb-free solder materials and the effect of thermal aging on different package designs. In addition, it is useful to generate

reliable constitutive models for solder alloys in order to assess solder joint stress/strain effectiveness and predict solder joint life. Current finite element models do not account for aging effects; while solder joints show complicated creep-plasticity interactions and temperature-strain rate dependent material characteristics during aging.

2.2 Effect on Solder Characteristic Life

Qi, et al. [36] investigated different Pb-free package types under accelerated thermal testing and found that Pb-free solder joints lasted longer than the SnPb joints when the thermal cycle temperature (ΔT) range was narrow, but the reliability trend reversed when the cycling ΔT was wide. In contrast, Pb-free solder joints in PBGA test vehicles lasted longer than SnPb solder under both conditions. That the temperature range was a key factor affecting reliability was attributed to the greater effective stiffness of the resistor which results in larger thermal stresses and eventual failure. A small dummy die in the PBGA produced a relatively high compliance, which caused unexpectedly long thermal fatigue lives.

Shnawah, et al, [37] performed thermal and mechanical test on a series of SAC solders alloys. From thermal cycling test, he explained that significant performance improvement of SAC305 over SAC105 is attributed to three factors which are (1) the large number of Ag_3Sn disperse in the bulk solders, since they can improve the mechanical properties of the solder and suppress the recrystallization during thermal fatigue process, (2) the large number of single crystal-like and the fine grain type microstructures, because they decrease the thermal strain and retard the recrystallization, and (3) the high amount of coincidence site lattice (CSL) boundaries, as they suppress both inter-granular cracks and grain boundary sliding after recrystallization during thermal fatigue process. He's results shown that the best SAC composition for drop performance is not necessarily the best composition for optimum temperature cycles reliability, For example; SAC405 and SAC305 solder give good temperature cycling reliability which is desirable for high temperature electronic devices used in Aerospace, Military, and Automotive industry. However, SAC405 and SAC305 solder give poor drop shock performance, which is not preferable for portable and handheld electronic devices, such as cameras and cell phones.

When component assembles, the reflow process would impact the solder joint performance by its heating condition which needs to be considered as a pre-thermal treatment. Microstructural changes have certain initiation at this level. Qi, et al. [38] simulate this process with controls and

then did failure analysis on selected component samples. According to the result, the intermetallic layer thickness was sensitive to the reflow profiles employed. Furthermore, it is possible that the mechanical properties of the solder could be affected by microstructural changes, such as grain size and the creation of intermetallic particles. In addition, the solder joint with the highest cooling rate showed the worst reliability in terms of thermal fatigue. In general, the SAC solder joints demonstrated poorer wettability than the SnPb solder joint. Improving wettability of the SAC alloy during the reflow process will be beneficial to solder joint reliability. Similar result can be found in Kim's, et al. [39] study that slowly cooled joints (or alloys) exhibit a coarsened β-Sn dendrite structure with a lower micro-hardness value in comparison to fast cooled ones. When thermal fatigue would cause more time dependent deformation such as creep than pure mechanical deformation, the coarsened microstructure observed in slow cooled joints would exhibit a longer fatigue life. Since creep deformation is known to be operative dominantly on grain or crystal boundaries, a coarse dendrite structure of low Ag joints is expected to be more resistant to the creep component of thermal cycling tests than high-Ag joints. The thermal fatigue life of low-Ag solder joints is less dependent of the cooling rate during the assembly process in comparison to the high-Ag solder joints and longer fatigue life of low-Ag joints, possibly due to their greater ductility and lower hardness. Which were emphasized in by Kittidacha that the thermal cycling results and failure mode showed that the stiffness of the bulk solder contributed to its ability to resist shear force and creep propagation during test. But the Ag content in solder is still the most important factor to be optimized to improve thermal cycling performance [40]. Kim [39] also conclude, from his failure analysis, that Solder joint reliability at the given thermal cycling test condition is determined by the characteristics of crack growth at the given solder joints, which is determined by its characteristics of deformation. For eutectic SnPb solder joints, they showed a global and uniform deformation in the high temperature regime. In the low temperature regime, the deformation is localized only at chip side solder joint while maintaining the global deformed shape from the previous high temperature regime. This localized deformation at low temperature regime created a large shear dislocation at chip side solder joint, with the crack initiating at the outside corner of the solder joint and growing toward the inside of chip. Whereas for SAC alloy, the presence of a large Ag_3Sn plate can actually enhance fatigue life by blocking or arresting an advancing crack which is an agreement of Shnawah's study.

Coyle, et al. [41] agreed that Ag content has a strong positive influence on thermal fatigue

life. In his test, the best fatigue performance is recorded with higher Ag content SAC405 and SAC305 alloys. He gave an explanation that the fatigue life of SAC solders is dominated by the Ag content and the evolution of the Ag_3Sn intermetallic particle morphology during testing. The slower cooling rate results in a more elongated or lamellar intermetallic morphology which appears to be more resistant to coarsening. When change the testing temperature profile, he discovers a longer dwell time is more characteristic of service conditions. For resistors assembled with SAC405, SAC305, and SAC105 solders, a 60 minute dwell time reduced the characteristic life by approximately 20% below the value observed for a 10 minute dwell. The reduction in the characteristic life of the SnCu solder is over 30% with 60 minute dwell testing. Vandevelde, et al. [42] compared his analysis on SnPb and SAC solders, and then he stated that there is no general conclusion about the trend in life time from SnPb to SnAgCu. The main conclusion is probably that the trend is very dependent on the package type but also on the applied loading conditions (minimum temperature, maximum temperature, dwell and ramp-up time). Further, he mentioned that Lead-free solder materials are more creep resistant at high temperatures resulting in higher life time under similar stress conditions for the solder joint. However, the lead-free solder materials have a higher elastic modulus, which can result for certain packages in much higher stress conditions. Moreover, in some packages, the solder joints are subjected to deformations instead of forces (e.g. underfilled flip chip joints) which are often worse for the lead-free solders.

2.3 The effect of thermal fatigue on solder joints

In microelectronics packaging, complex stresses and strains are usually generated in the components due to the CTE mismatch of different materials. Solder interconnects are usually subjected to deformations that lead to three-dimensional stress and strain states. The solder material constitutive law is critical in the development of thermo-mechanical models for IC package assemblies. Matin, et al. [43] has discovered, in his paper, that the fatigue damage within solder initiates at grain boundaries (the intrinsic thermal fatigue contribution) and also takes the form of persistent slip bands (the mechanical fatigue contribution). In addition, the correlation between the observed damage and the calculated stress fields provides evidence that three crucial factors exist: thermal mismatch between Cu and solder, intrinsic thermal mismatches caused by Sn anisotropy and the mechanical constraints posed by the Cu on the soldered joint. So he stated that together these determine the location and severeness of fatigue

damage in solder joints. Some more publications helped to characterize the thermal-mechanical response and, hence, the failure mechanism of SAC solder interconnects, that is to understand the interaction between the grains of different orientations when the interconnection is thermal-mechanically stressed, and also the role of larger primary intermetallics in the failure of such interconnects. Park, et al. and Martin, et al. explained that strain within a solder interconnect varied significantly in different grains and at and around the intermetallics under a thermal-mechanical loading which resulted in plastic deformation (or strain accumulation) along the grain boundaries and near the primary intermetallic precipitates during thermal cycling. After thermal cycling, microstructural changes were noticed which were localized along a grain boundary or near grain boundaries. The micro-cracks were localized mainly along high angle grain boundaries. The location of the fatigue cracks was found to strongly correlate with regions the largest stresses were caused by the thermal anisotropy of Sn [44, 45]. As a result, fatigue life is usually plotted on a stress versus number of cycles to failure or S–N curve. A typical fatigue curve for solder is depicted in Figure 2.1. Figure 2.2 and Figure 2.3 illustrated typical creep and stress-strain curve.

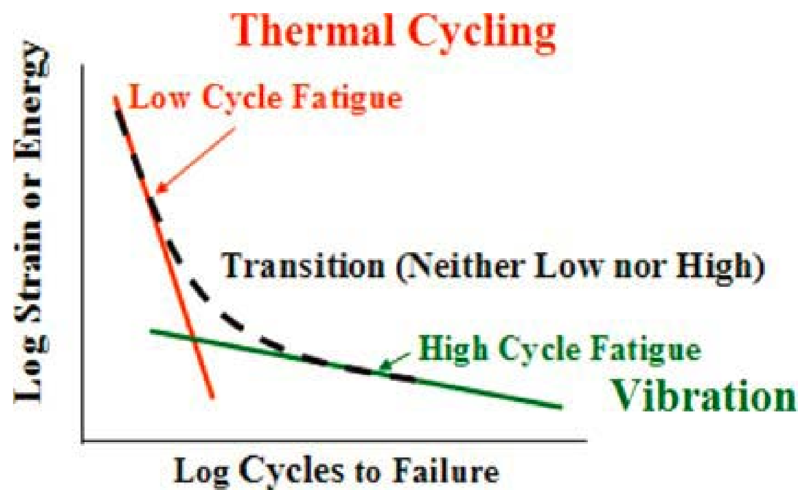


Figure 2.1 Typical fatigue curves

The creep properties are characterized by monitoring the strain history under the action of a constant mechanical stress. In general, the dwell time at the high temperature has been considered to influence fatigue life more than low temperature dwell. With evidence shown that SAC solder yields at a lower stress and has a higher creep resistance than Sn37Pb and the higher

creep resistance helps explain the generally observed longer fatigue life of SAC as compared with Sn37Pb under temperature cycle loading. So the proof has been delivers where SAC had a lower life than Sn37Pb [46]. Another finding has been that the reduction in fatigue life of SAC solder joints due to longer dwells (hold) times appears to be larger than the reduction observed with Sn37Pb solders [47]. That is obviously backing up Osterman's [46] point.

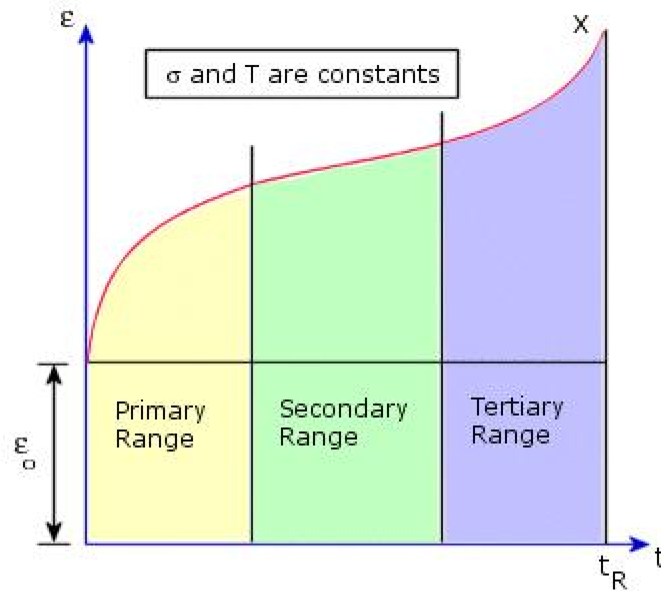


Figure 2.2 Typical creep curves

Xu, et al. [49] performed -40°C to125°C thermal cycling test on his test subject. He demonstrated the significant change of grain size during the thermal cycling test indicates that dynamic recrystallization occurred. It is well known that when alloy is subject to hot deformation (T> 0.5 Tm), the processes of strain-hardening and softening are concurrent. During the thermal cycling aging for solder alloy, thermal stress was induced by CTE mismatch in every temperature cycle and caused solder deformation. When the temperature ramp up from -40°C to125°C (for SAC, Tm is 217 C or 490K, 125 C=398K=0.8Tm), the dynamic recrystallization occurred, new grains formed and the stress is released. Then, the next temperature cycle came and new deformation was involved before the enlargement of the grains. On the other hand, he also characterized the isothermal effect on the solder that there is no stress or deformation developed. Long time high temperature aging, however, caused the significant

grain growth which provides a perspective need to be enhanced.

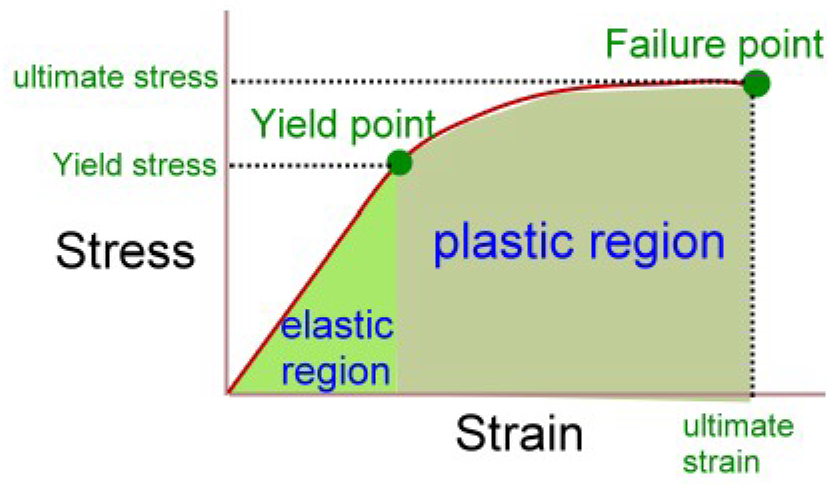


Figure 2.3 Typical Stress-Strain curves

From microstructural perspective, damage of solder interconnections is a result of the accumulation of internal energy in the form of increased dislocation densities in the plastically deformed regions of the solder interconnections. Arfaei, et al. [50] observed similarities in the failure mechanisms of a variety (BGA, CSP, QFN) of Pb free SAC solder joints which were subjected to one of a variety of thermal cycling regimes. Solder fatigue was observed in all of the samples, with evidence that crack propagation was along grain boundaries of recrystallized regions of the sample. He shown the evidence of prolific recrystallization was revealed in these samples. The presence of an interlaced Sn grain morphology was correlated with a delay in crack initiation. Meanwhile, Schubertt, et al. [51] had a test comparison between SnAgCu and SnPb(Ag) solder alloys. The data shown that the SnAgCu alloy considered here has resulted in higher acceleration factors compared to the SnPb alloy when comparing the different temperature cycling conditions and the results suggest that SnAgCu thermo-mechanical failure data may correlate to accumulated creep strains as in the case of eutectic SnPb(Ag) soldered assemblies which indicated that for the same strain level at higher strains, SnAgCu performs better, whereas for the same strain level at lower strains. SnPb(Ag) performs better.

2.4 Microstructural change under thermal fatigue

During service, electronic devices are exposed to high temperatures. Structure of the bulk

solder and interface will be changed by coarsening and inter-diffusion, resulting in different mechanical properties of the joints. Previous studies on the flip-chip packages with Sn-Pb solder bumps have shown that the creep strain plays a predominant role on the fatigue life of the flip-chip packages, while the formation of the continuous IMC layers, e.g., $(Au,Ni)Sn_4$, $(Ni, Cu)_6Sn_5$, Ni_3Sn_4, and Cu_6Sn_5, is the main cause for deterioration of the solder joint reliability [52]. Ma, et al. [53] discovered there are three possible intermetallic compounds that may be formed: Ag_3Sn forms due to the reaction between Sn and Ag as shown in Figure 2.5 (a) and Cu_6Sn_5 forms due to the Sn and Cu reaction as shown in Figure 2.5 (b), but Cu_3Sn will not form at the eutectic point unless the Cu content is high enough for the formation of Cu_3Sn at higher temperatures, so in bulk specimens Cu_3Sn is not present. A sequential of IMC formation is initiated at reflow process. During aging, two metallurgical processes occurred in the solder joints: (a) Kirkendall voiding in Cu_3Sn layer and (b) coarsening of the eutectic structure in the bulk solder. There should be another process going on, i.e., solid-state precipitation of finely dispersed Ag_3Sn and/or Cu_6Sn_5 particles from the Sn matrix. Precipitation of the dispersive IMC particles from the supersaturated Sn strengthened the bulk solder, decreasing the package reliability [54]. Large Ag_3Sn rods can also cause reliability concerns when they form in a high stress concentration area, such as the corner between solder bump and copper pad. Fatigue cracks can initiate and propagate along the interface between the Ag_3Sn and solder, leading to mechanical failure [55]. The morphology of Ag_3Sn compound formed in lead-free Sn-Ag solder matrix is greatly influenced by cooling rate during solidification process. Three types of Ag_3Sn IMC compound are possible: particle-like, needle-like, and plate-like as well. Cooling rate determined the size and morphology of Ag_3Sn compound. The sequential evolution or changing of Ag_3Sn compounds with decreasing cooling rate can be summarized as follows: particle-like → needle-like → plate-like. Figure 2.4 depict the different types of Ag_3Sn morphology: (a) particle-like, (b) needle-like, (c) plate-like.

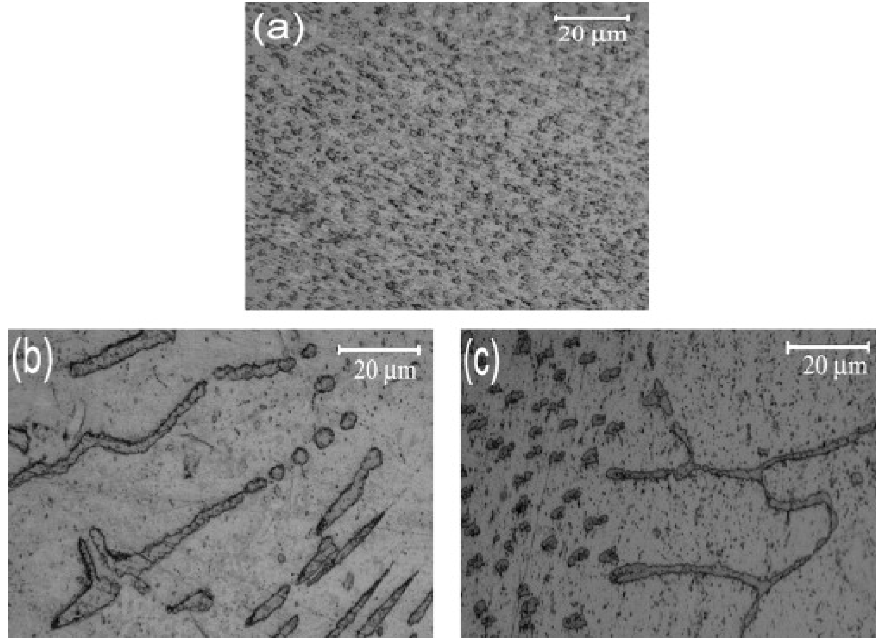


Figure 2.4 Ag_3Sn Morphology [65]

The extra-large plate-like Ag_3Sn compound can be formed in solder matrix adjacent to Cu_6Sn_5 interfacial layer in case of extremely slow cooling such as cooling in furnace. The formation of Cu_6Sn_5 interfacial layer causes the local concentration of Ag atoms to be enriched in solder matrix adjacent to interface and hence prompt to the growth of Ag_3Sn compound into large plate or pillar liked column [56].

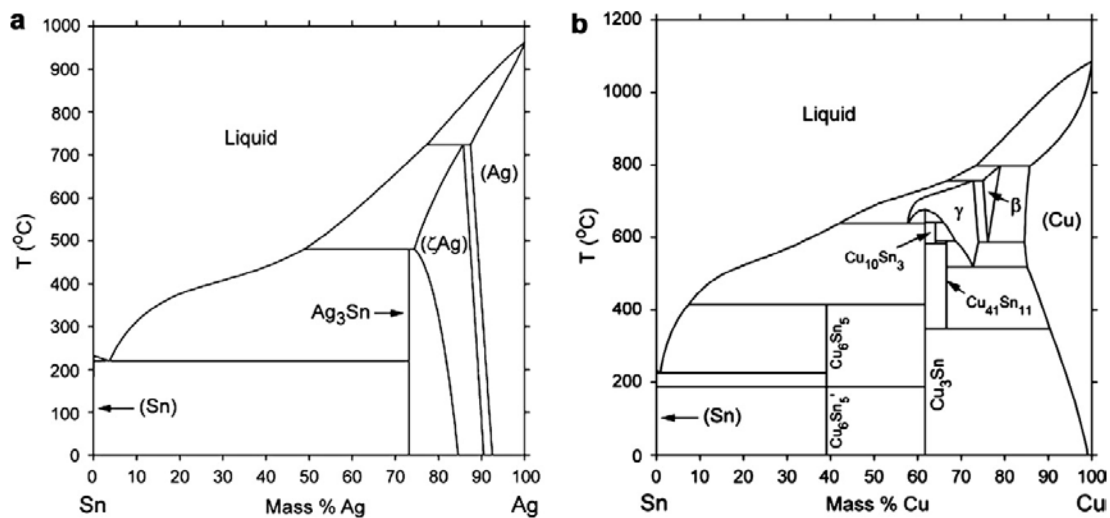


Figure 2.5 Binary phase diagram: (a) Sn–Ag and (b) Sn–Cu [53]

Xu, et al. [57, 58] observed the growth of Kirkendall voids at the interface between the intermetallic and Cu pad after thermal aging for the SAC/Cu-OSP soldered assemblies. The formation of the voids is due to the Cu diffusion is faster than the Sn diffusion during solid-state aging, resulting in a net vacancy flux of Cu at the interface of intermetallic compound or inside the Cu_3Sn.The void caused the crack path to change from the Cu_6Sn_5 layer to Cu_3Sn and the samples had significantly lower drop lifetimes than as-reflowed components. The void formation was always accompanied by an obvious morphological change, which results in the different diffusing rate of reactive species in different sublayers, and hence leads to the formation of voids at the interface between different morphological sublayers within the same IMC phase layer which lead to higher stress intensity factors than void-free structures [59]. The morphology and thickness of Cu-Sn IMC for the as-reflowed specimen were dependent on a number of factors, such as temperature/ time, volume of solder, property of solder alloy and morphology of the deposit [60]. Figure 2.5 demonstrated the phase diagram of Sn–Ag and Sn–Cu solder material.

When solder contact gold or nickel board finish, the IMC evolution mechanism shares some similarities with one on copper or copper based immersion metal plating. Davis, et al. [60] tried to isothermally age and temperature-cycle the SnPb/ENIG solder/surface finish system in his test. In the failure analysis process, he detected the intermetallic forms at both the board finish (bottom) and BGA side (top) of the solder joint for isothermally aged, temperature-cycled, and (aged cycled) joints. At low cycle numbers where high joint reliability is observed, the Au Ni Sn layer is broken, discontinuous, and not fully developed. At higher cycle numbers and longer aging times, the Au Ni Sn layer becomes continuous and encourages crack growth along the intermetallic interface and consequent lower reliability. When intermetallic compounds form smoothly at the solder interface, the mechanical properties are degraded (compared to a rough intermetallic) due to the decreased resistance to shear along the interface.

Islam, et al. [62] discovered sequential microstructural changes in solder-finish systems. During reflow, molten solder absorbs the entire Au layer into solution, allowing Sn, Ag and Cu from the solder to react with the Ni layer/NiP layer and Cu–Sn IMC form on the diffusion barrier layer. Later on the new fomed Cu–Sn IMC react with Ni and form Sn–Ni–Cu IMCs. After sufficient amount of Sn–Ni–Cu IMCs formation, Ni–Sn IMC also forms on the top of barrier layer due to limited supply of Cu from the solder. The IMCs of Electroless NiP/solder joints are

weaker and brittle than the electrolytic Ni IMCs due to the presence of dark P-rich Ni layer and P entrapment in the IMCs.

Copper or nickel based surface finish comparison always has been a research attractive subject. The nickel was chosen because it reacts slowly, compared to copper or gold, with tin-rich solders. In microstructural perspective, on copper, Sn-37Pb forms a two-phase intermetallic of Cu_6Sn_5 adjacent to the solder and Cu_3Sn adjacent to the copper. The Cu_3Sn is planar with a columnar grain structure and the Cu_6Sn_5 consists of elongated nodules. On nickel, eutectic tin-lead forms irregularly shaped Ni_3Sn_4. Ni_3Sn_4 intermetallic compound is known to form at the interface between Ni-metallized soldering pads and SnPb solder. However, when even a small amount of copper (more than about 0.3 wt.%) is present in the solder matrix, such as in the neareutectic SnAgCu solders, the formation of Cu_6Sn_5 is favored over the Ni_3Sn_4 at the Ni|solder interface. The structural defects such as the voids discovered in the reaction layer formed on the Ni(P)|Au metallized soldering pads can reduce the reliability performance of the solder interconnections. The solder interconnections on the Cu coated PWBs failed at the component side, where cracks propagated through the $(Cu, Ni)_6Sn_5$ or the Cu_6Sn_5 reaction layer depending on the component under bump Metallization (UBM): $(Cu, Ni)_6Sn_5$ on the Ni|Au metallization and Cu_6Sn_5 on the copper metallization. The reason for this failure mode is that, under fast deformation rates, the flow stress of the solder is increased and stresses concentrate at the corner regions of the interconnections where the fracture strength of the intermetallic reaction zone is exceeded. The recrystallization occurs first near the corner region of the interconnections, where the structure is the most heavily deformed plastically. The local recrystallization of solder interconnections enhances cracks to nucleate in and propagate through the recrystallized solder interconnections. The formation of a continuous network of high-angle (grain) boundaries enables intergranular fracture of interconnections. Meanwhile, the growth of interfacial intermetallics while the solder is in the solid-state is of concern for flip-chip interconnects. If the intermetallic layer coarsens significantly, it can consume the UBM and cause the joint to dewet at the layer beneath the UBM. Also, because the intermetallic is brittle, if it becomes a significant fraction of the solder joint, it can act as a site for crack initiation and propagation when the joint is deformed [63, 64].

Chapter 3
Experimental Approach

3.1 Introduction

Electronics assemblies containing solder joints are frequently exposed to harsh environments for prolonged periods of time. At the same time, electronic products continually trend toward smaller sizes with more complex functions, weight savings, and cost reduction. Board interconnect densities have been increasing for many years (~ 30-50% in six years) and, by the year 2014, the ball pitch of BGA for harsh environments are expected to be < 0.8 mm; high performance packaging pitches will reach 0.5 mm; and hand held devices will reach 0.4 mm [66]. The complexity of IC packages and the package integration are both rapidly increasing.

To add insult to injury, new legislation has been implemented to ban Pb in electronics globally. The transition to Pb-free technology is a demanding task for industries that assemble Pb-free components to Pb-free printed circuit boards using Pb-free solder alloys. The Pb-free challenge requires a combined effort from academic and industry researchers to select appropriate Pb-free solder alloys, to measure Pb-free solder alloy properties, and to characterize the solder behavior under various stress loading conditions. Last, efforts are necessary to specify efficient Pb-free manufacturing processes, determine logistics, handle intellectual property issues, and assess lead-free assembly reliability [67].

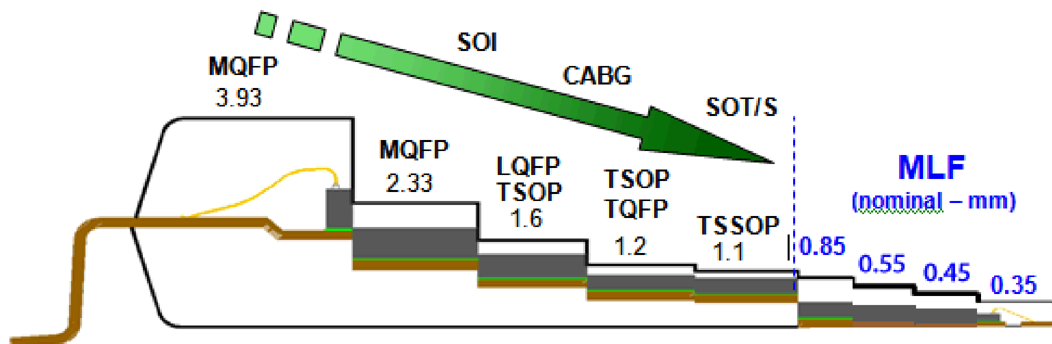


Figure 3.1 Package Height Comparisons

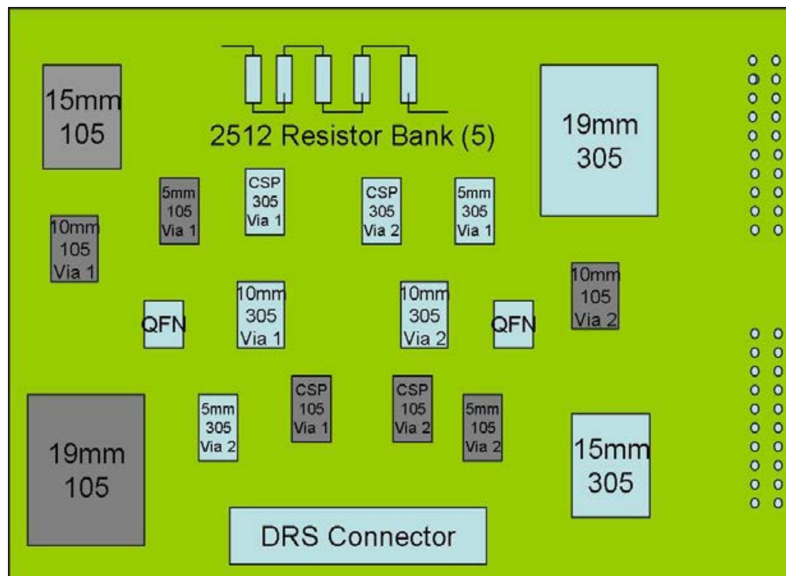
Industrial and military electronics demand long cycle, long-term reliability where products last years and even decades. But numerous studies [34-64] demonstrate that Pb-free solder reliability undergoes significant changes over time, which leads to our studies here of the effect of aging on Pb-free solder reliability. Figure 3.1 showed the height comparison of different packages. Isothermal aging effects on lead-free solders have been extensively investigated and showed aging effects significantly degrade the mechanical properties of lead-free solders. However, limited work has been done on the effects of aging on board-level thermal performance of lead-free solder, especially important for applications in harsh environment electronics such as high performance computing, automotive, aerospace and defense application; limited studies has been done on the different isothermal aging temperature for various durations, especially for room temperature and <100 ℃. Aging effect on different most popular SAC105 and SAC305 is still unknown; limited work were studied the reliability for long reliability >=6 months; limited work were studied to analysis the different acceleration factors of the reliability on aging effects and the trends of aging on different package designs. In order to break through those limitations, the TV-7 research project was introduced. In previous studies, Zhang, et al. [68-71] concluded that a direct and deleterious effect on packaging reliability results during long-term isothermal aging for fine-pitch ball grid array (BGA) packages with Sn-1.0Ag-0.5Cu (SAC105), Sn-3.0Ag-0.5Cu (SAC305), and Sn-37Pb solder ball interconnects. The trends were in the expected directions; namely, the reliability was reduced when using higher aging temperatures, smaller solder balls, and lower Ag content alloy since creep deformation is known to operate on grain or crystal boundaries. A coarse dendrite structure of low Ag joints is expected to be more resistant to the creep component of thermal cycling tests than high-Ag joints [72].

The purpose of this work is to discover the role of isothermal aging on the reliability of Sn-Ag-Cu (SAC) assemblies. Different surface finishes mixed with various types and sizes of packages were employed in our test vehicles. A full experiment matrix with varying aging temperatures and solder alloys was considered, followed by accelerated thermal cycling to generate Weibull plots showing how the package reliability depends on aging time and temperature. Our results will assist both academic and industrial researchers to select the best solder alloys, packages, and materials per the demanding environmental conditions of operation.

3.2 Test Vehicle (TV7) Design and Assembly

3.2.1 Test Board Design

The test vehicle was based on FR-406 glass epoxy four-circuit layer boards laminated with a glass transition temperature (T_g) of 170°C. The board had a reasonable copper distribution to provide optimum copper balance and CTE mismatch for thermal cycle testing. The dimensions of the board design were 100.076 x 67.056 mm with a thickness of 1.574 mm (measured laminate to laminate). Four types of surface finishes, Immersion Sliver (ImAg), Immersion Tin (ImSn) (TV7 phase 1), Electroless Nickel Immersion Gold (ENIG) and Electroless Nickel Electroless Palladium Immersion Gold (ENEPIG) (TV-7 phase 2) were in the experimental matrix. Some test vehicles were double-sided, built in TV-7 phase 1 to verify the difference in reliability between top and bottom components. The unpopulated layout of the TV 7 is shown Figure 3.2. Figure 3.3 and Figure 3.4 show populated assembled test vehicles for TV7 phase 1 and TV7 phase 2.



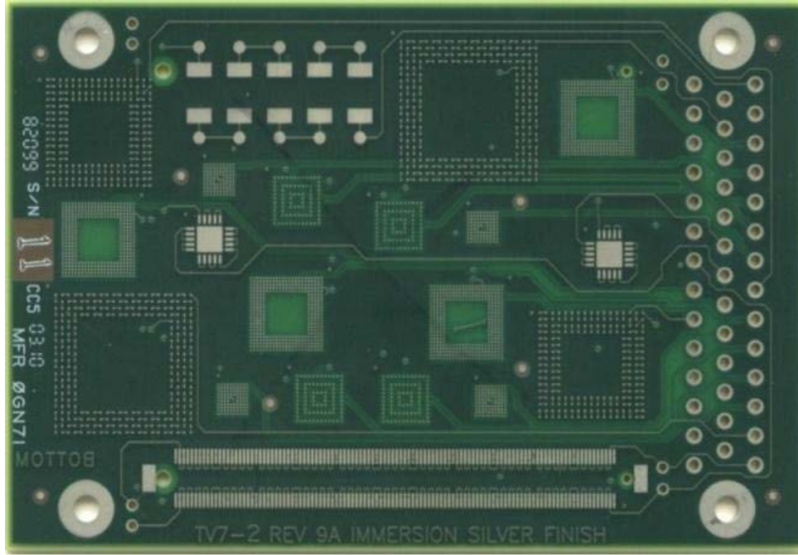


Figure 3.2 TV7 Design Layout

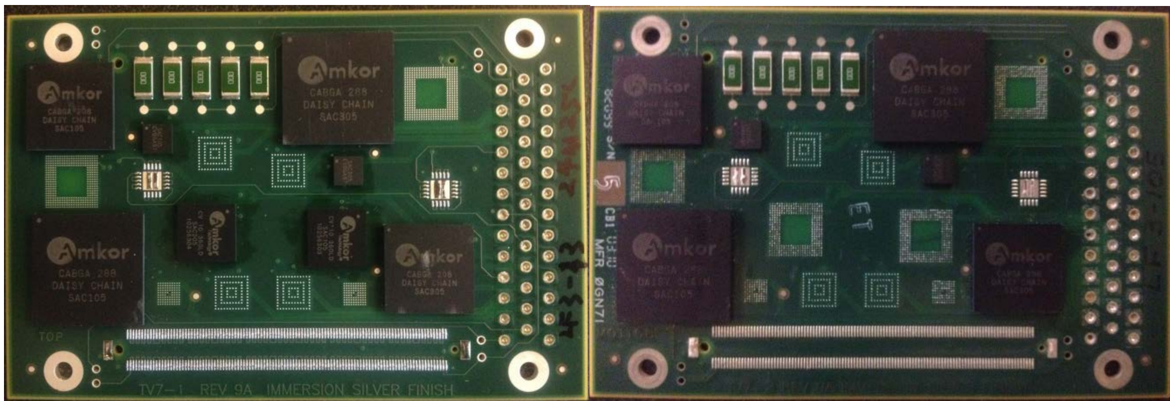


Figure 3.3 Assembled TV7 phase 1 (ImAg, ImSn)

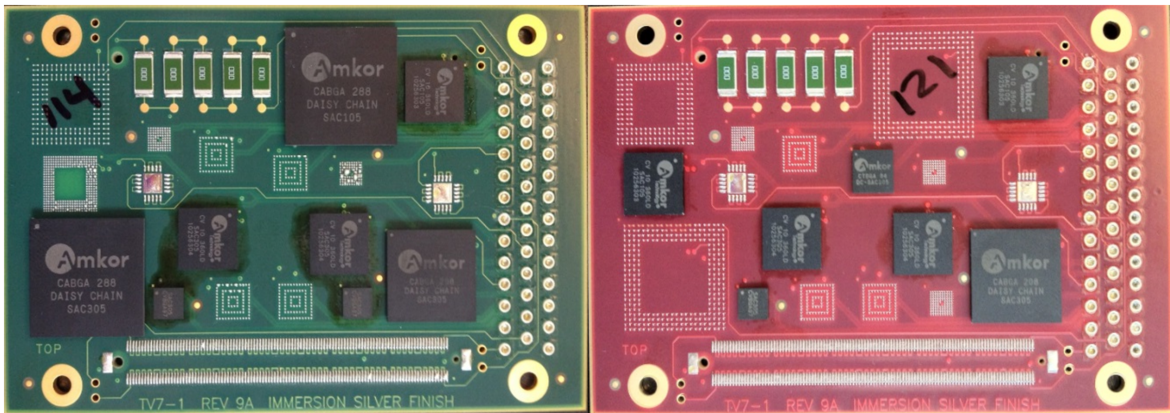


Figure 3.4 Assembled TV7 phase 2 (ENIG, ENEPIG)

3.2.2 Components Selection

TV7 was populated with both active and passive devices. The fine pitch PBGA packages measured 5x5mm, 10x10mm, 15mmx15mm, and 19mmx19mm and contained Sn-1Ag-0.5Cu (SAC105), Sn-3Ag-0.5Cu (SAC305) and Sn-37Pb (control) solder joints for each size. A 7×7 mm CSP, 5×5mm MLF with SAC305 solder paste was also included. The boards in the test used non solder mask design (NSMD) pads for easier analysis of aging on the reliability. The Sn termination resistors (passive devices) measured 6.3x3.2mm. Industry-standard naming conventions of resistor sizes describe the length and width of its body in hundredths of an inch. The resistors used in this research are thus referred to as 2512. Suhling [73] reported that chip resistors fabricated with 90Sn-10Pb solder terminations to match the Sn-Pb solder paste avoid fillet lifting. Pure Sn terminations were used as a part of the overall Pb-free initiative. 2512 resistors were selected due to their large body size, high rated power dissipation, and poor solder joint reliability. They were mounted in banks of five resistors placed in series. All test components provided by Practical Components were daisy chained for continuous sampling of component reliability through the accelerated life tests. The package matrix is shown in Table 3.1.

Table 3.1 Component Matrix

Type	Package Size (mm)	Die Size (mm)	Ball/Lead count	Pitch (mm)	Ball Alignment
BGA	19x19	12.0x12.0	288	0.8	Perimeter
BGA	15x15	12.7x12.7	208	0.8	Perimeter
BGA	10x10	5x5	360	0.4	Perimeter
BGA	5x5	3.2x3.2	97	0.4	Full Array
CSP	7x7	5.9x5.9	84	0.5	Perimeter
MLF	5x5	4.5x4.5	20	0.25	

3.2.3 **Solder Paste and Stencils**

No-clean-type 3-Kester 256 paste (Sn-37Pb) and SAC 305 solder paste were the two main solder pastes we selected for testing. For the lead-free test vehicle, the components were built onto the PCB with no clean Senju305 M31-GRN360-k1MK-V (Table 3.2).

Table 3.2 Pb-Free Solder Paste Parameters in TV7

Item	ECO M31-GRN360-K1MK-V Specification	Test method
Alloy Composition	Ag:3.5, Cu:0.75, Sn:Balance	J-STD-006
Powder Shape Powder Grain Size	Spherical Type 3 (25~45μm)	J-STD-005-3.3.3, STM-12, J-STD 005-3.3

We applied the E-FAB Electroform stencil for TV7, the thickness of which is 0.115 mm (0.0045 in). The solder paste print machine used was MPM UP2000 HiE.

3.2.4 **SMT Assembly Processes**

All the test vehicles TV7 were fabricated in Continental AG – Huntsville Electronics Division. Before assembly, there is a 12 hour "bake out" process in an oven at 150 ℃ to remove moisture and prevent damage to the components during reflow. The stencil and the PCB were positioned in the screen printer and the solder paste was pressed through the stencil with a rubber squeegee. The board was transferred out and inspected for correct alignment of the solder paste to the PCB pad sites.

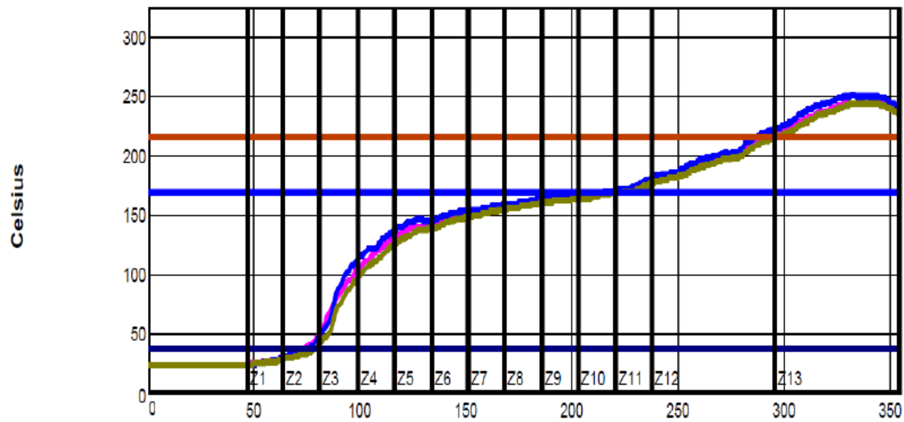
Next, the PCBs were put into two placement machines: Assembleon MG-1 and Universal GSM-1. MG-1 used a tape and real feeder to place small components: resistors, 5mmBGA, MLF, CSP and 10mmBGA; GSM-1 used a tray feeder to pick and place 15mm BGA and 19mm BGA components. Once the machine stared to receive boards, the programmed algorithm began and all the electronic components were picked and placed onto the test vehicle in order. The

board was then checked again in case of skewed package placement. Figure 3.5 shows the Continental Electronics prototype manufacturing lab.

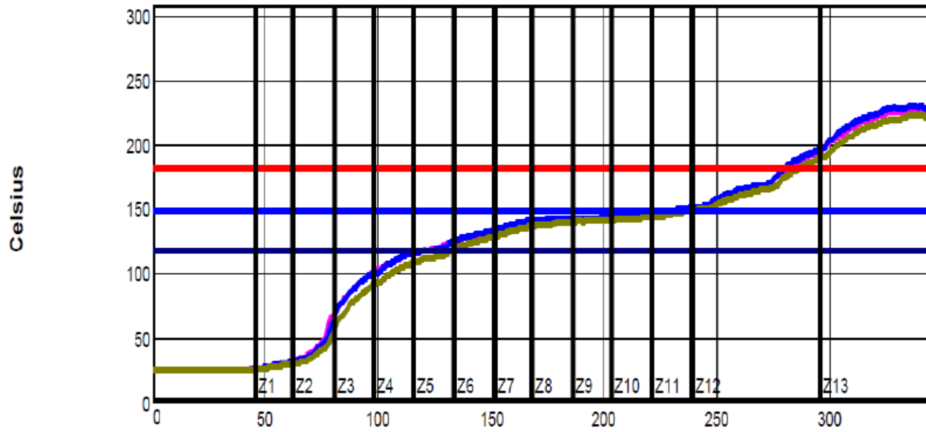
Figure 3.5 Continental Electronics Prototype Manufacturing Lab

Figure 3.6 shows the 13-zone Rehm V7 convection reflow oven used for reflow. The oven supplies a nitrogen gas environment during reflow and has a conveyor speed of 33.5 inch/min. The temperature was monitored and the SAC alloys melting temperature was ~ 217°C. The peak temperature was 245–247 °C for PBGAs and 252 ℃ for resistors. The time duration for PBGAs in the oven above the melting point was around 52 to 55 seconds, and 61 seconds for resistors. In the Sn-37Pb assemblies' thermal profile, the peak temperature of PBGAs was between 224 to 229°C. Resistors had a peak temperature of 231°C. The time duration for PBGAs in the oven above the melting point was around 60 to 65 seconds, and 67 seconds for resistors. By comparing two processes, there was a difference of 21°C in the peak temperature of PBGAs. The Pb-free-reflow and Pb-reflow profiles used for the assembly are shown in Figure 3.7.

Figure 3.6 Reflow Oven



(a)



(b)

Figure 3.7 (a) Lead-free Reflow Profile and (b) Tin-Lead Reflow

3.2.5 Inspection Test Vehicle

A transmission X-ray tomography system was used to inspect the quality of the solder joints in the assemblies. This type of system is good for detecting problems such as insufficient solder, solder ball bridging, pad skewing, and voids in joints. Figure 3.8 shows a couple of cases of pad skewing and solder bridging and how they would look in such a system. We found very few cases of misaligned assembly.

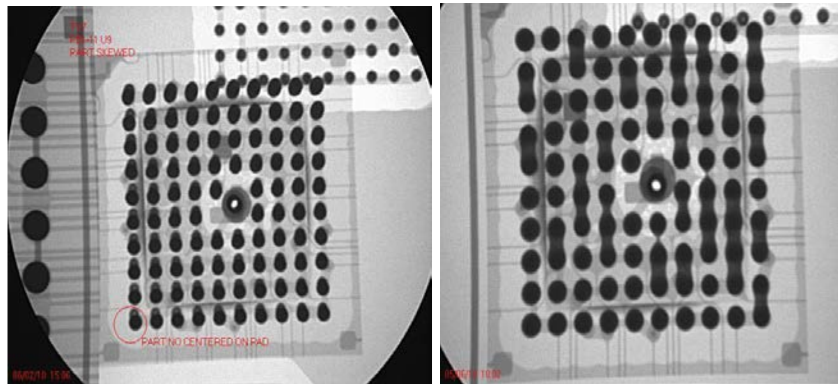


Figure 3.8 Skewed Pad on the left and solder bridging on the right

3.3 Thermal Test

3.3.1 Test Matrix and Test Conditions

In TV7 phase 1, all test specimens were subjected to aging at temperatures 25°C, 55°C, 85°C and 125°C with aging over time periods of 0, 6 months, 12 months and 24 months., In phase 2, the isothermal temperature conditions were 55°C, 85°C, 100°C and 125°C, with aging time periods of 0, 21 days, 6 months, and 12 months. The full matrix is shown in Tables 3.3-3.4.

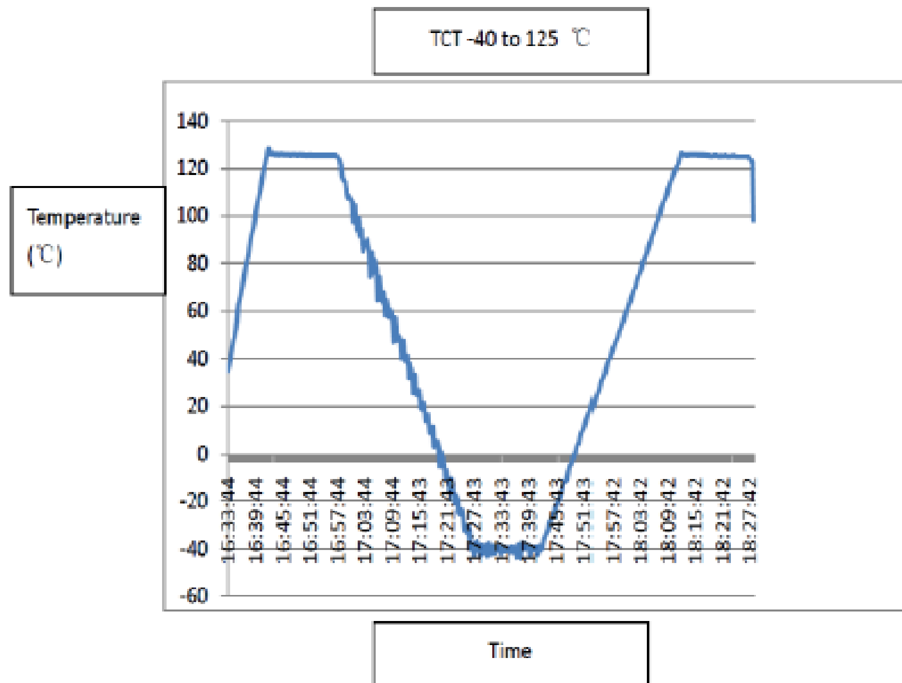
Our TV7 thermal testing design followed mainstream industry standards recommended by the Institute for Interconnecting and Packaging Electronic Circuits (IPC) and the Joint Electron Device Engineering Council (JEDEC). For the thermal cycling reliability test, thermal cycling (TCT) was carried out from -40°C to 125°C per JEDEC JESD22-A104B-Condition G, and from -40°C to 85°C per the JEDEC JESD22-A104B-Condition G-condition A. All tests were set for a 15 min dwell time and 30 min ramp time thermal profile, shown in Figure 3.9.

Table 3.3 TV-7 Phase 1 Thermal Testing Plan

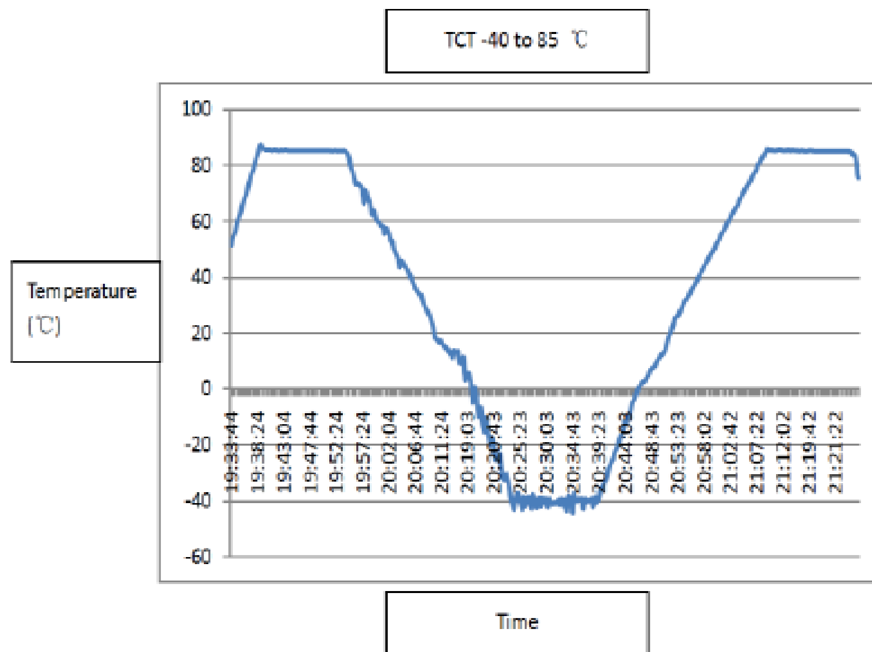
Thermal Test Plan												
	No aging			Aging 6 months			Aging 1 year			Aging 2 years		
	ImSn	ImAg	SnPb	ImSn	ImAg	SnPb	ImSn	ImAg	SnPb	ImSn	ImAg	SnPb
Thermal Cycle -40°C ~ +125°C	3:5 means 3(T/-) 5(-/B)	8	5	3:5(55°C) 3:5(85°C)	5(25°C) 5(55°C) 5(85°C) 5(125°C)	4(55°C) 4(85°C)	3:5(55°C) 3:5(85°C)	5(25°C) 5(55°C) 5(85°C) 5(125°C)	5(25°C) 5(55°C) 5(85°C) 5(125°C)	3:5(55°C) 3:5(85°C)	5(25°C) 5(55°C) 5(85°C) 5(125°C)	4(25°C) 5(55°C) 5(85°C) 5(125°C)
Thermal Cycle -40°C ~ +85°C	3:5	8	5	3:5(55°C)	5(25°C) 5(55°C) 5(85°C)	4(55°C) 4(85°C)	3:5(55°C)	5(25°C) 5(55°C) 5(85°C)	5(25°C) 5(55°C) 5(85°C)	3:5(55°C)	5(25°C) 5(55°C) 5(85°C)	4(25°C) 5(55°C) 5(85°C)
Thermal Shock -40°C ~ +85°C	3:5	9	5	3:5(55°C)	5(25°C) 5(55°C) 5(85°C)	4(85°C)	3:5(55°C)	5(25°C) 5(55°C) 5(85°C)	5(25°C) 5(55°C) 5(85°C)	3:5(55°C)	5(25°C) 5(55°C) 5(85°C)	4(25°C) 5(55°C) 5(85°C)
Subtotal	9:15 means 9(T/-) 15(-/B)	25	15	9:15 (55°C) 3:5(85°C)	15(25°C) 15(55°C) 15(85°C) 5(125°C)	8(55°C) 12(85°C)	9:15 (55°C) 3:5(85°C)	15(25°C) 15(55°C) 15(85°C) 5(125°C)	15(25°C) 15(55°C) 15(85°C) 5(125°C)	9:15 (55°C) 3:5(85°C)	15(25°C) 15(55°C) 15(85°C) 5(125°C)	12(25°C) 15(55°C) 15(85°C) 5(125°C)

Table 3.4 TV7 Phase 2 Thermal Testing Plan

	No Aging		**21 Days**		**6 Month**		**12 Month**	
Thermal Cycle -40°C~ +125°C	ENIG		ENIG		ENIG		ENIG	
	SnPb	SAC	SnPb	SAC	SnPb	SAC	SnPb	SAC
	10	5	25	14	15	15	10	10
	ENEPIG		ENEPIG		ENEPIG		ENEPIG	
	SnPb	SAC	SnPb	SAC	SnPb	SAC	SnPb	SAC
	5	5	25	14	15	15	10	10
	No Aging		21 Days		6 Month		12 Month	
Thermal Cycle -40°C~ +85°C	ENIG		ENIG		ENIG		ENIG	
	SnPb	SAC	SnPb	SAC	SnPb	SAC	SnPb	SAC
	10	5	0	20	0	15	0	10
	ENEPIG		ENEPIG		ENEPIG		ENEPIG	
	SnPb	SAC	SnPb	SAC	SnPb	SAC	SnPb	SAC
	5	5	0	20	0	15	0	10



(a)



(b)

Figure 3.9 TCT Testing Profile: (a) -40 to 125℃ (b) -40 to 85℃

3.3.2 Data Acquisition System

During testing, the boards were placed vertically in the thermal cycling chamber and wired through the access port to the CAVE-developed MarkDano data acquisition system. This system allows for continuous monitoring of the various daisy chain networks was throughout the cycling using a high accuracy digital multimeter coupled with a high performance switching system controlled by LabView software. Based on IPC-9701, the practical definition of solder joint failure is an interruption of electrical continuity > 1000 Ohms. In this study, failure was defined to be the point when the daisy chain resistance was > 300 Ohms for five repeated resistance measurements. Figure 3.10 shows the schematic design of the monitoring system.

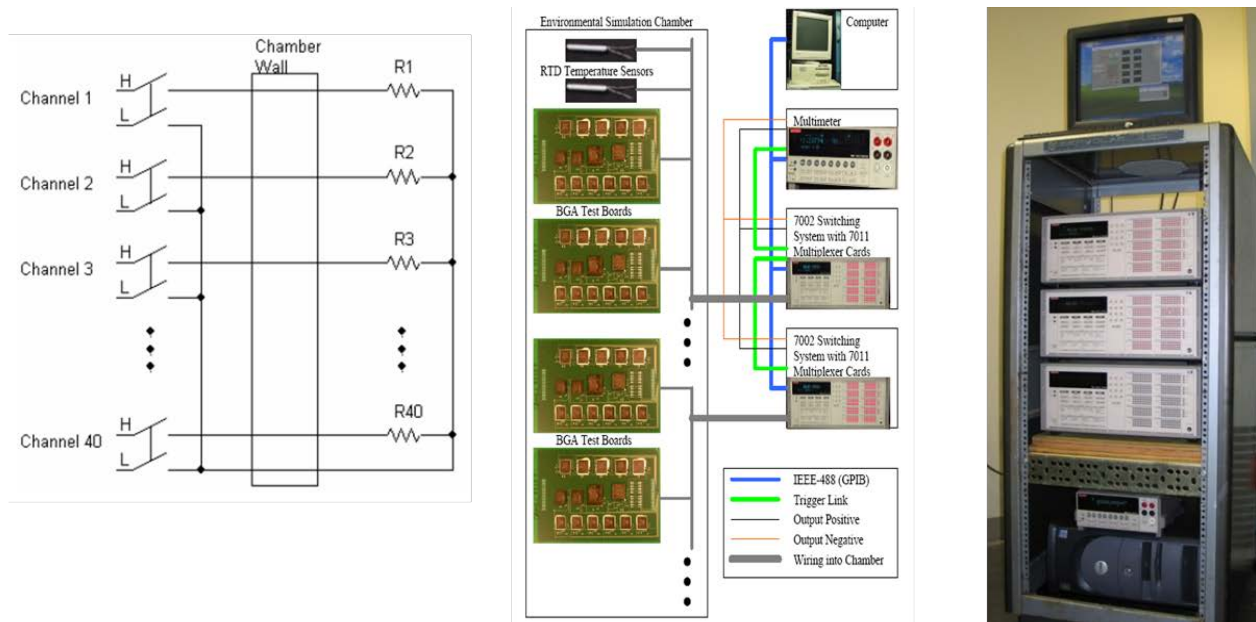


Figure 3.10 Schematic design of the monitoring system

3.4 Failure Analysis

Samples for microscopic examination were cross-sectioned and ground with SiC polishing paper (240, 320, 400, 600, 800, 1200 grit) followed by two steps of fine polishing with 3 micron diamond suspension. After polishing, a thin gold or carbon film was sputtered on the surface of samples for the prevention of electrical charging during SEM observation. SEM and energy-dispersive X-ray spectroscopy (EDX) was used to investigate the microstructure of the joints. The back-scattered electron (BE) imaging mode was used in most of the electron micrographs to highlight the various microstructural features in the solder joints. Figure 3.11 demonstrated the schematic explanation of SEM functions.

SEM uses a focused beam of high-energy electrons to generate a variety of signals at the surface. When the primary electron beam interacts with the specimen, the electrons lose energy within an absorption volume known as the interaction volume. Its size depends on the electron beam energy, the atomic number of the material, and the specimen density. The secondary electrons generated through the electron-surface interaction are collected by a scintillator, photomultiplier, and head amplifier detector system and directed to a cathode-ray tube monitor and/or digital image system.

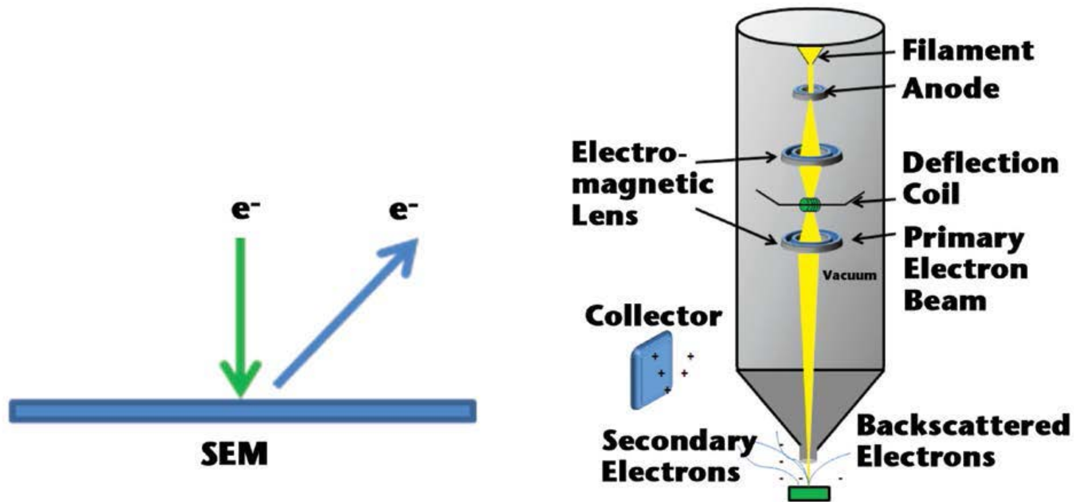


Figure 3.11 (a): SEM schematic showing the ion attack to release surface ions; (b): SEM schematic for beam signal.

EDX is used with the SEM to acquire the elemental composition of the thin film and/or solder material. EDX rests upon the fact that each element has a unique atomic structure which emits distinctive X-rays after electron irradiation. The primary electron beam possesses sufficient energy to ionize a core level of the target atom, which subsequently relaxes by an electron transition from an upper energy level to the vacated level. In the process, X-ray energy of a distinctive energy is emitted and detected by the X-ray detector in the SEM. Since each atom has a unique set of energy levels, the spectrum of X-ray energies allows determination of the elements in the absorption volume [75].

Chapter 4

TV7-Phase I Reliability and Failure Analysis

4.1 Introduction

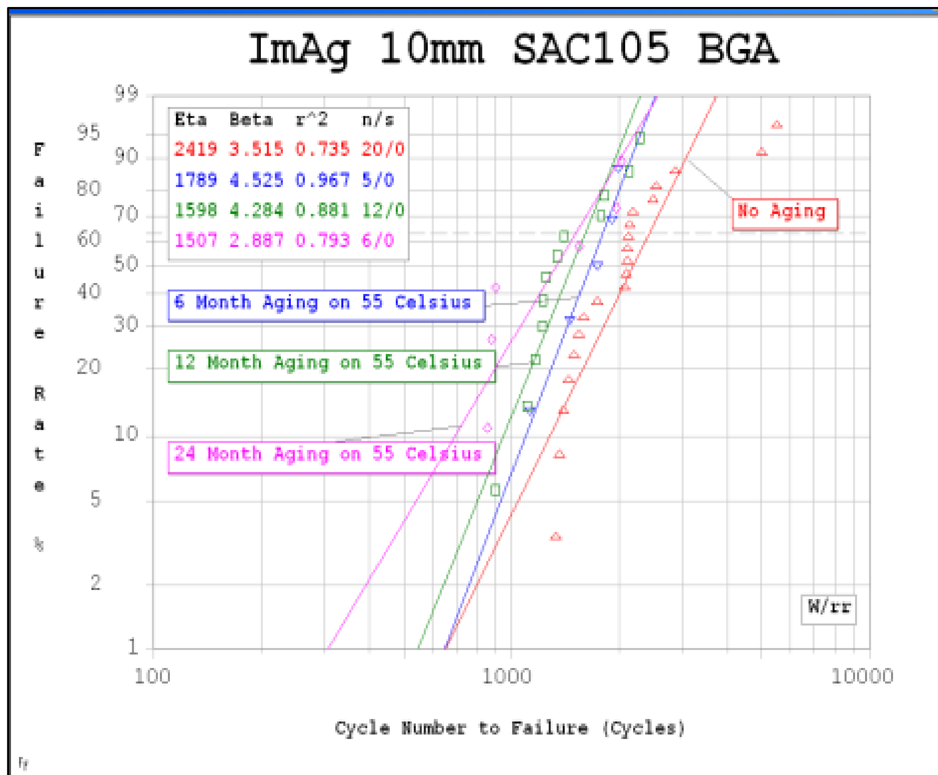
Solder materials exposed to temperature excursions, vibration, and shock during service suffer failure or function-loss by thermal-mechanical fatigue. The resulting microstructure evolution and/or deformation caused by globally mismatched coefficients of thermal expansion (CTE) between components, printed circuit boards, and the solder joint (as well as local CTE differences in phases or grains within the solder [34]) are the primary focus of concern.

This chapter presents basic reliability data gathered from two years of experiments using a number of SAC alloys, packages, and pitch sizes on two surface finishes, with isothermal aging at several temperatures (Table 3.3). At periodic time intervals, two-parameter Weibull plots were generated to yield a statistical picture of the package reliability. The failure life of electronic packages is characterized by a Weibull distribution. Plots of failure rate vs. cycle number to failure were generated for each tested package. The characteristic life (η) is defined as the point (i.e., number of cycles) at which 63.21% of the population is expected to fail. The slope (β) of the Weibull distribution distinguishes different failure modes. The experimental failure points are fitted with the least squares method to give the characteristic life and slope of the Weibull distribution. The r^2 value indicates the quality of the data fit. The TV7 test vehicles were air to air thermally cycled between -40℃ to 125℃ with a 90 minute cycle time.

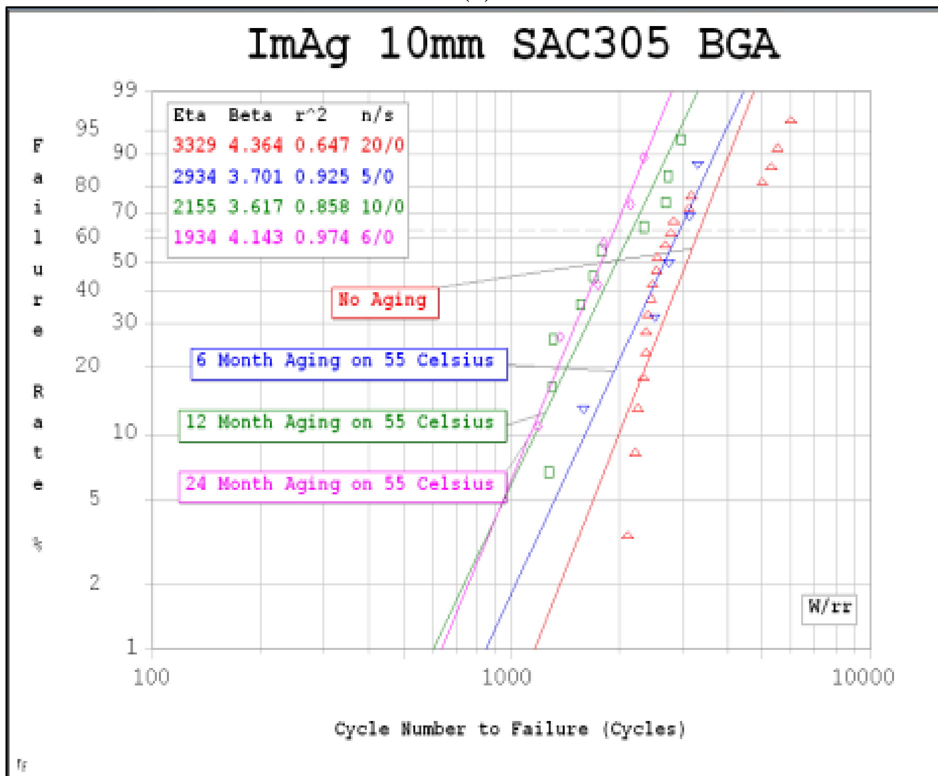
4.2 Reliability Data Analysis

4.2.1 10mm PBGA Package

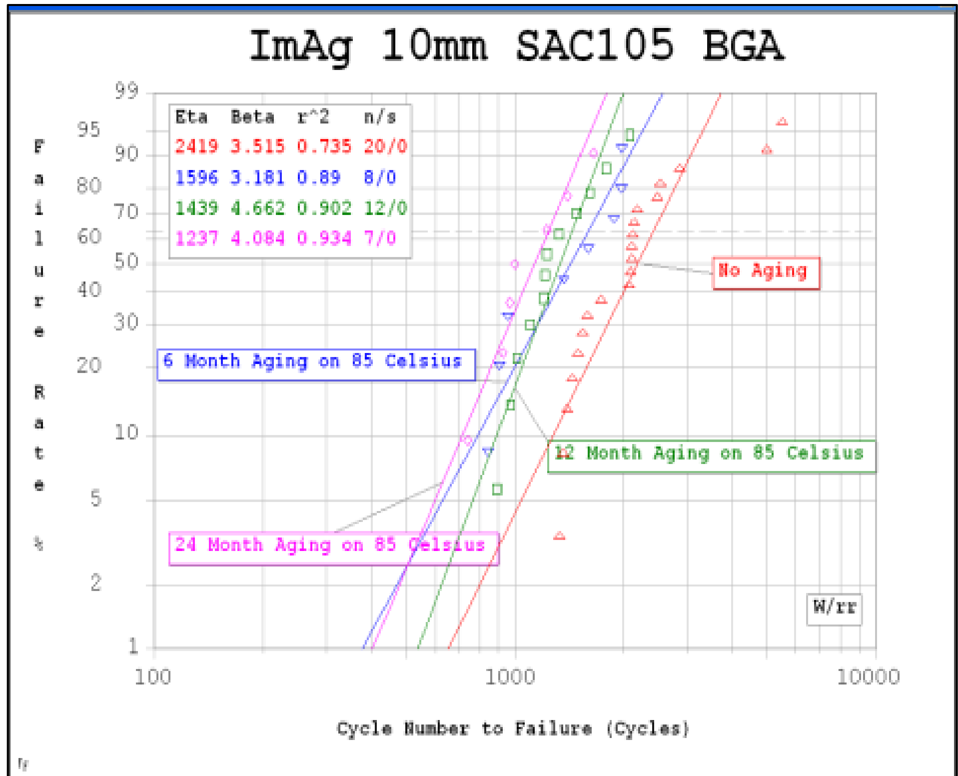
The list of Weibull plot below generally depicted the reliability degradation of 10mm BGA package subjected to several of aging preconditioning. Analysis follow on would show systematically reduction if more packages.



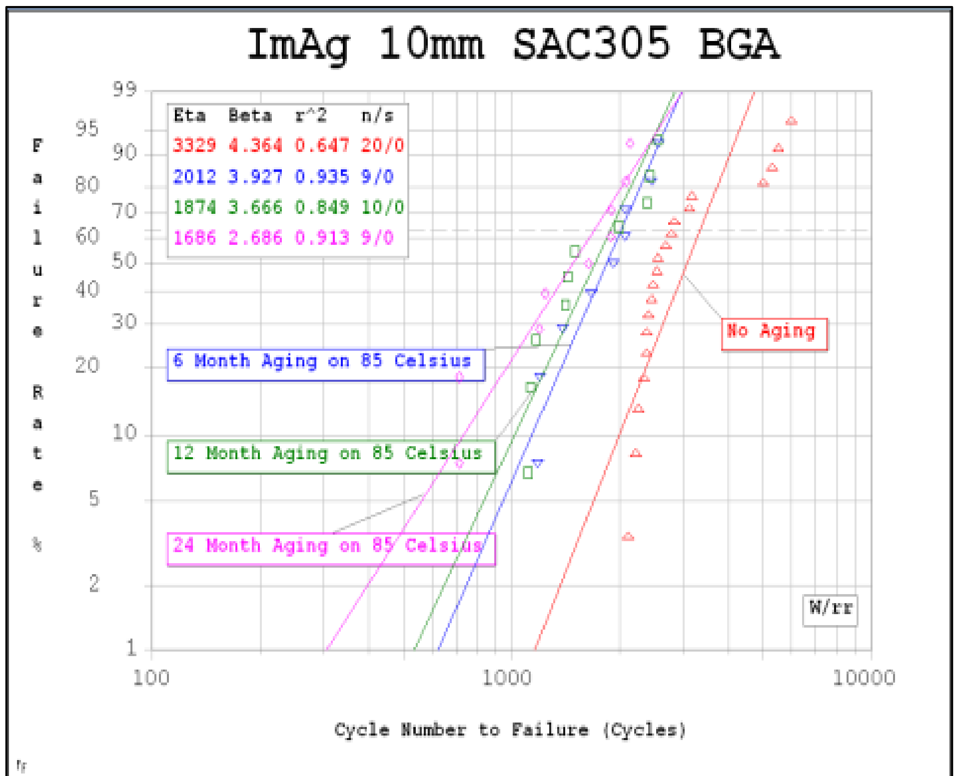
(a)



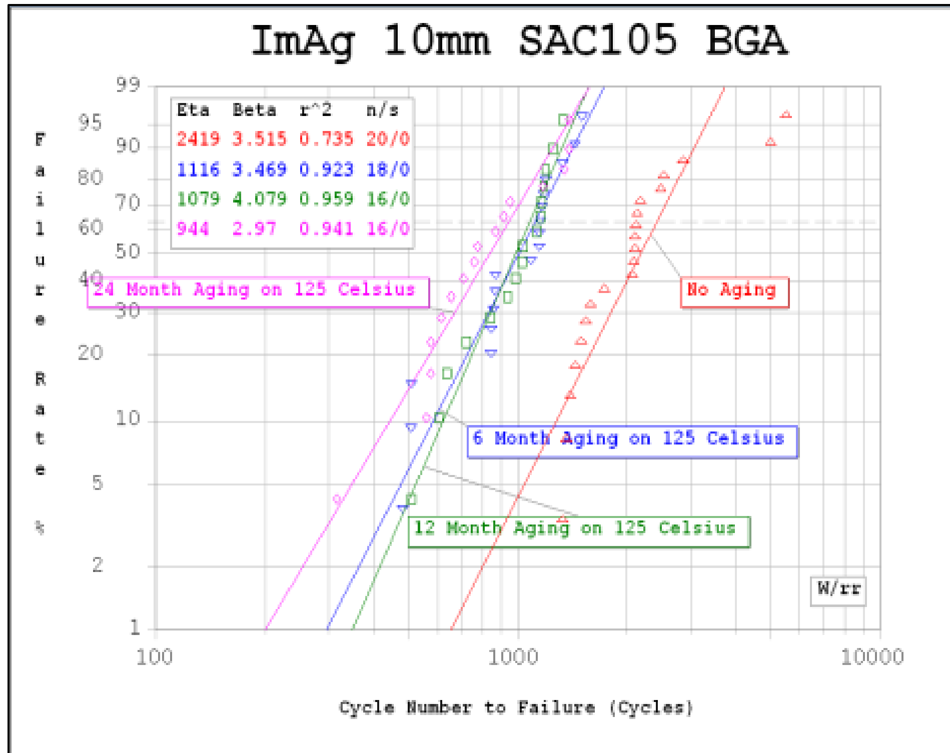
(b)



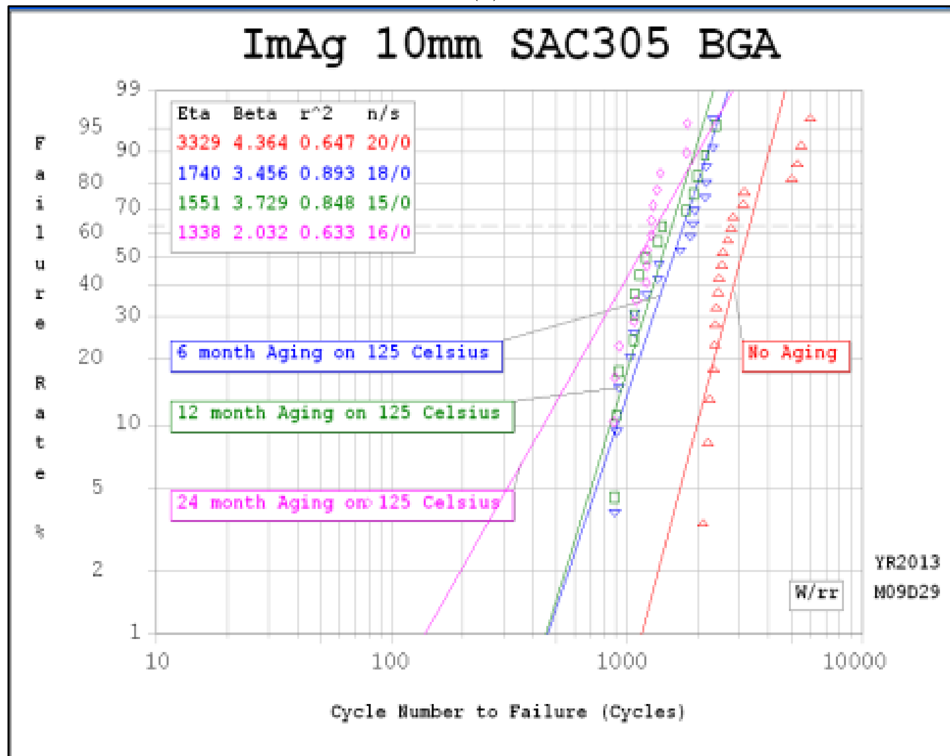
(c)



(d)



(e)



(f)

Figure 4.1 Weibull plots for Pb-free 10mm BGA packages on ImAg board plating after 2-year aging. SAC105 (a) 55°C; (c) 85°C; (e) 125°C aging. SAC305 (b) 55°C; (d) 85°C; (f) 125°C aging.

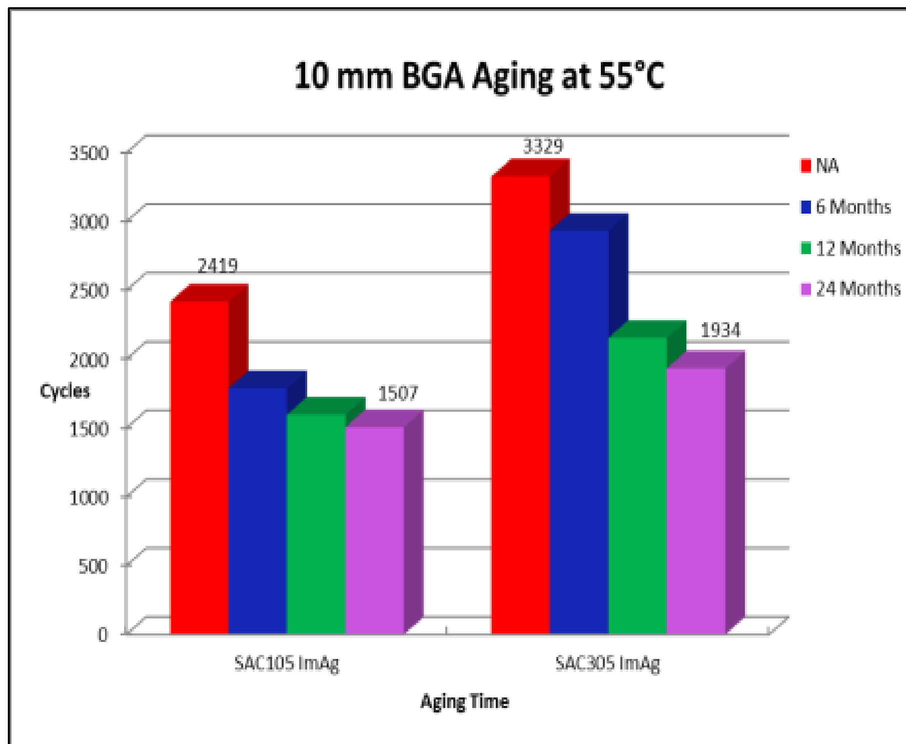


Figure 4.2 Degradation comparison of 10mm SAC105 and SAC305, aging at 55oC. NA in all degradation charts indicates "no aging."

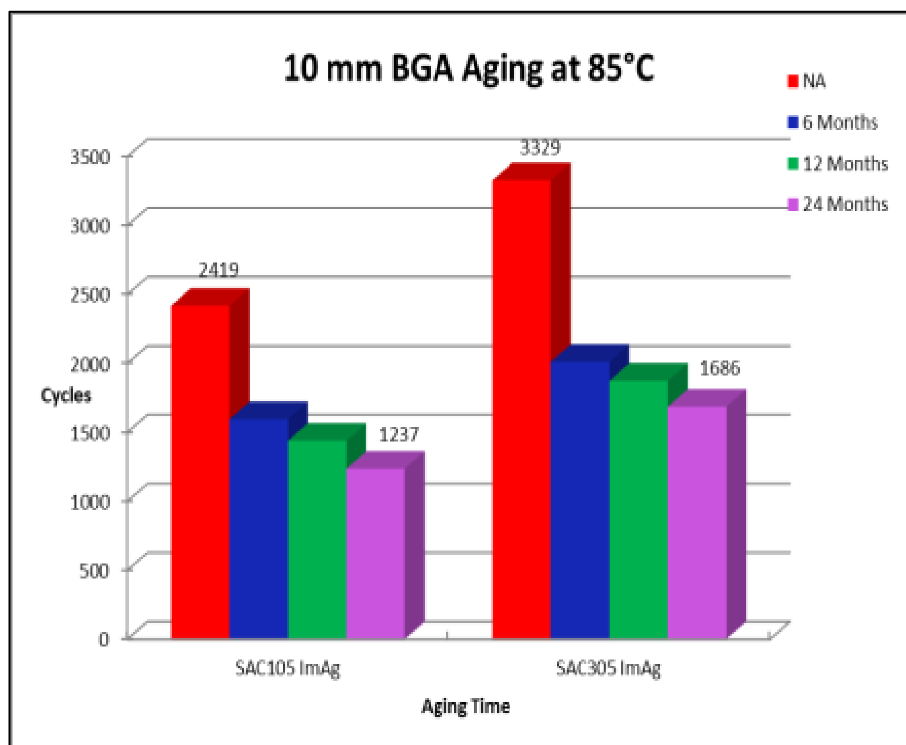


Figure 4.3 Degradation comparison of 10mm package SAC105 and SAC305, aging at 85°C.

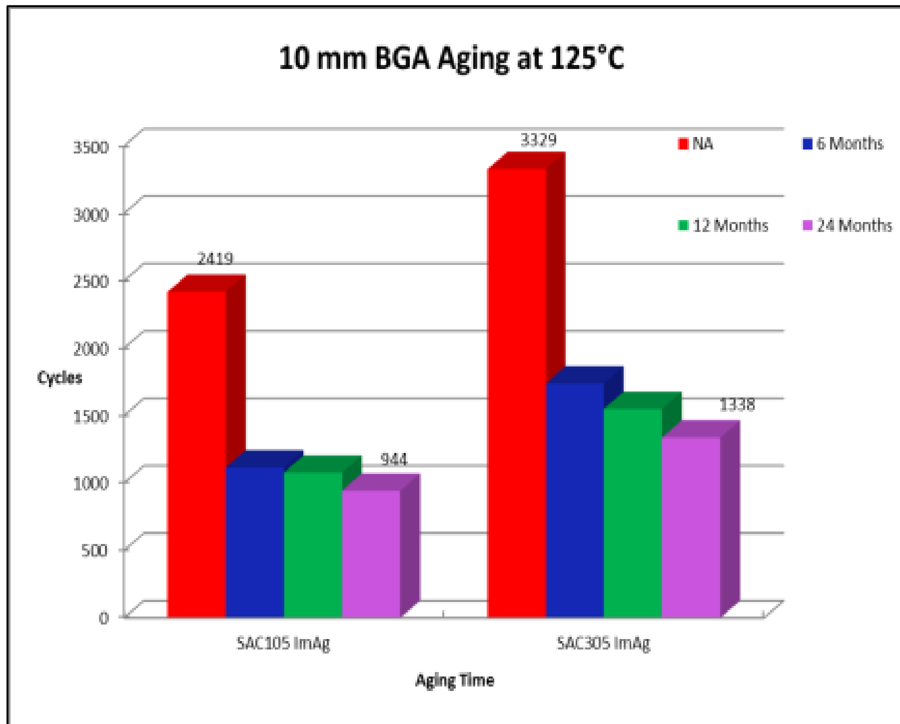
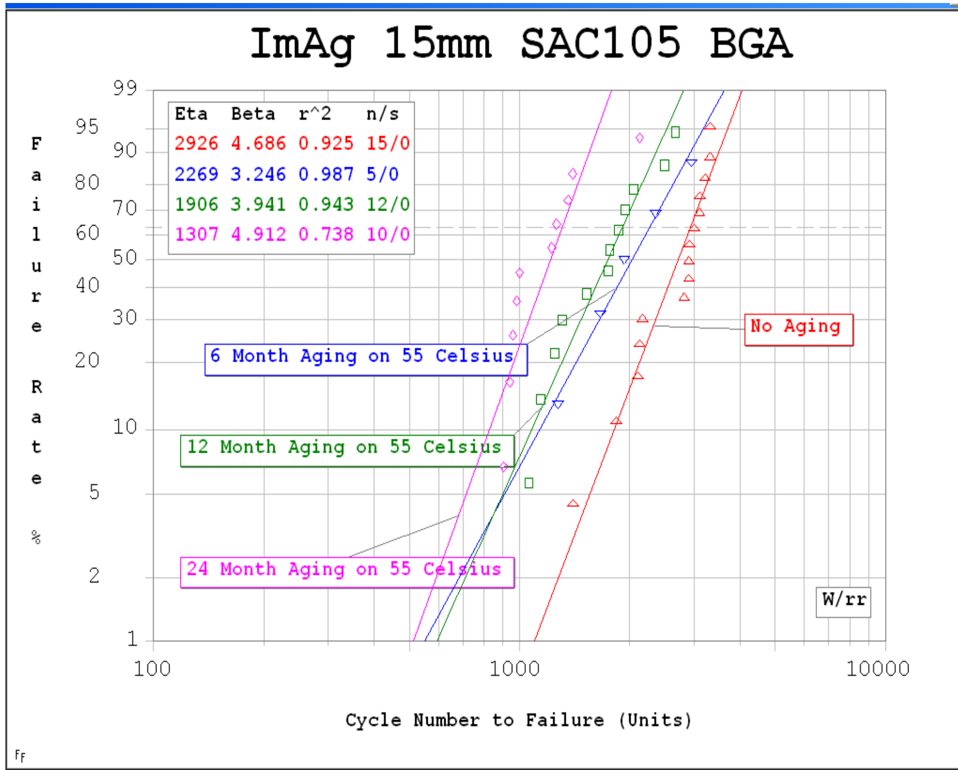


Figure 4.4 Degradation comparison of 10mm package SAC105 and SAC305, aging at 125°C.

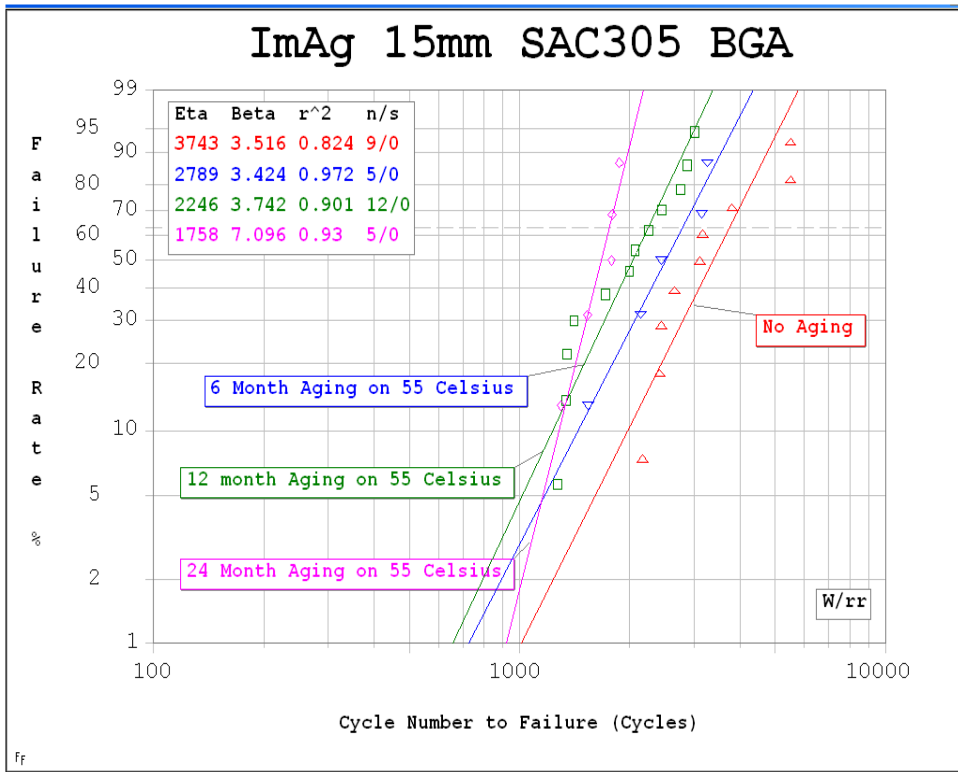
Figure 4.2 summarizes the characteristic life degradation of the 10mm package (0.4mm ball pitch) on immersion silver (ImAg) exposed to 55°C aging for up to 2 years. A continuous degradation in reliability is observed for both SAC alloys. The characteristic life for SAC105 was reduced from 2419 to 1507 cycles which is a 37.7% degradation when compared to the no aging case. For SAC305, the characteristic life was reduced from 3329 to 1934 cycles after aging at 55℃ for 24 months, which is a 41.9% characteristic life deterioration. Figure 4.3 shows the case for 24 month aging at 85°C for the 10mm package on ImAg. The degradation characteristic life is 48.9% for SAC105 and 49.4% for SAC305, respectively. Figure 4.4 shows that after 2 years of aging at 125°C, the characteristic life is degraded to 61% for SAC105 and nearly 60% for SAC305.

4.2.2 15mm PBGA Package

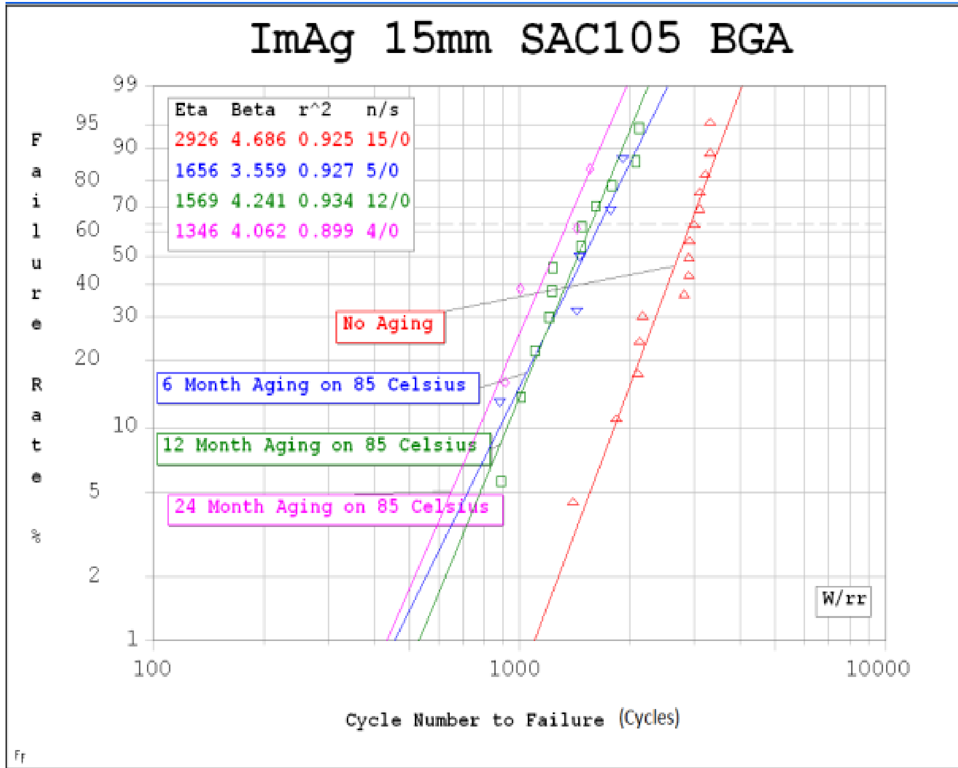
The list of Weibull plot below generally depicted the reliability degradation of 15mm BGA package subjected to several types of aging preconditioning.



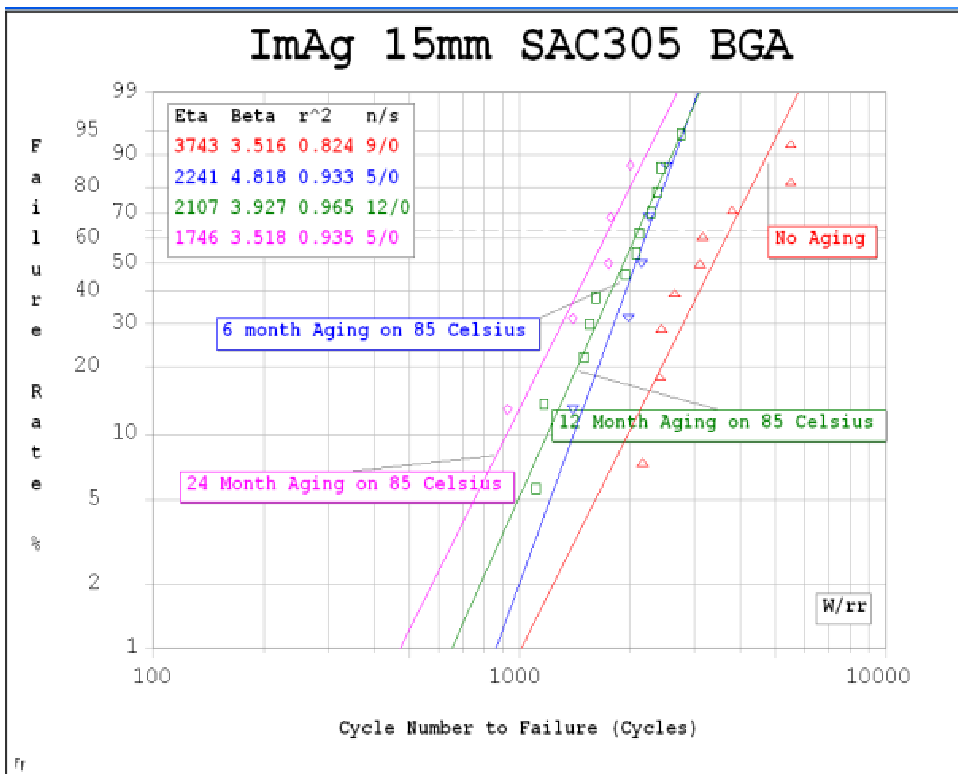
(a)



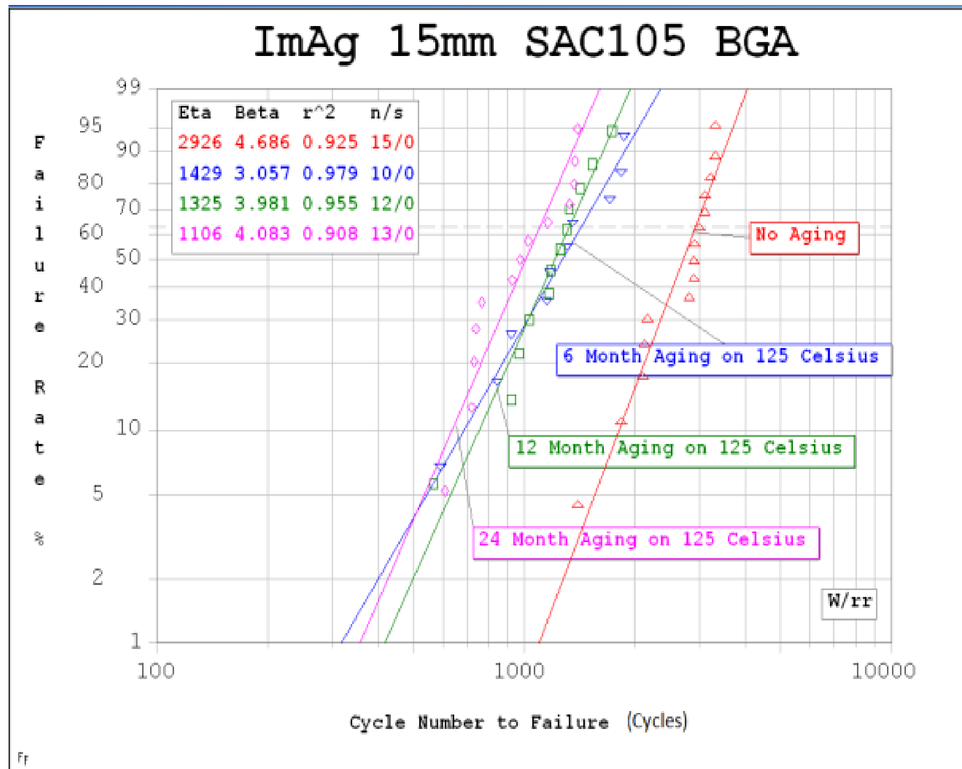
(b)



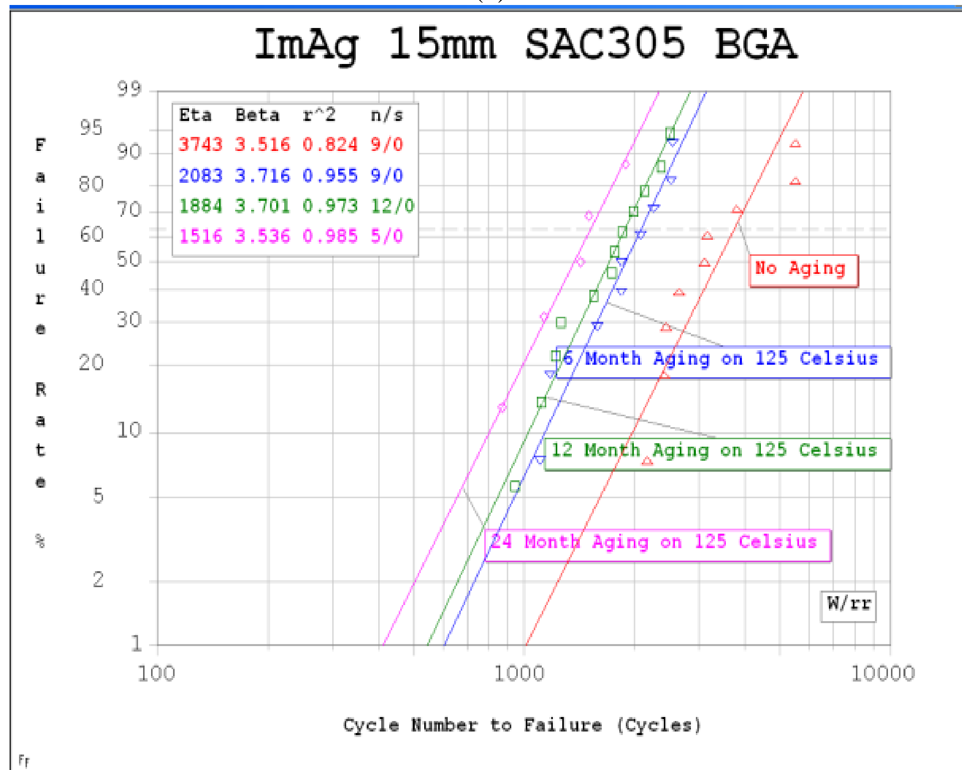
(c)



(d)



(e)



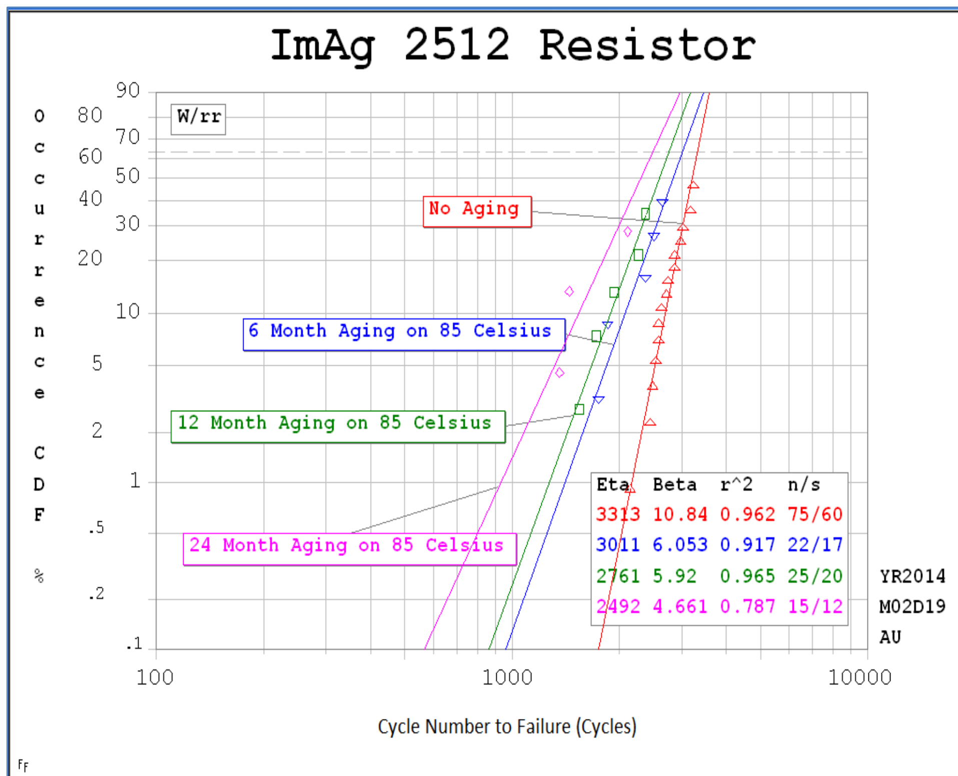
(f)

Figure 4.5 Weibull plots for Pb-free 15mm BGA packages on ImAg board plating after 2-year aging. SAC105 (a) 55°C; (c) 85°C; (e) 125°C aging. SAC305 (b) 55°C; (d) 85°C; (f) 125°C aging.

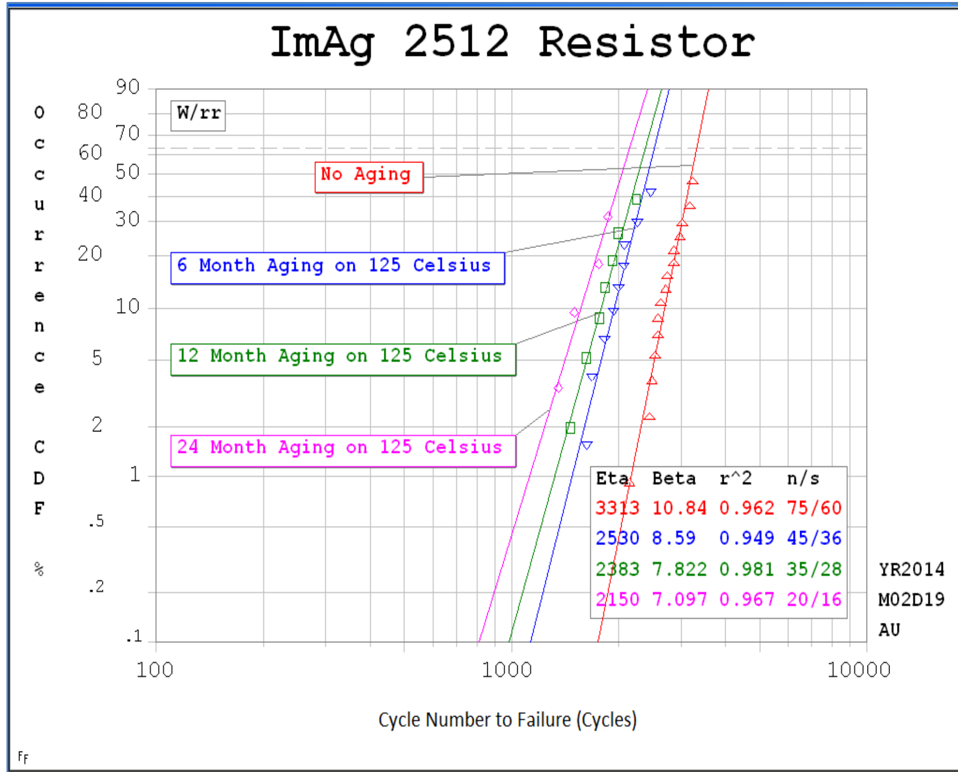
Summarizing, all Weibull plots in Figure 4.5 showed a clear life reduction with increasing aging time. In the cases of 15mm BGA package, after two year's aging at 85°C, the degradation rate of SAC105 and SAC305 were 54.0 and 53.4%, namely. At 125°C aging, the reduction rate for SAC105 and SAC305 were 62.2% and 59.5%, respectively. SAC105 joints have larger reduced reliability under aging than SAC305, showing that using SAC105 in long-term applications involving thermal fatigue is problematic.

4.2.3 2512 Resistor

The list of Weibull plot below generally depicted the reliability degradation of 2512 resistor package subjected to several of aging preconditioning. The result have certain similarity with BGA package.



(a)



(b)

Figure 4.6 Weibull plots and degradation bar charts for SAC305, 2512 resistors on ImAg after 2-years of aging: Weibull plots for (a) 85°C aging; (b) 125°C aging.

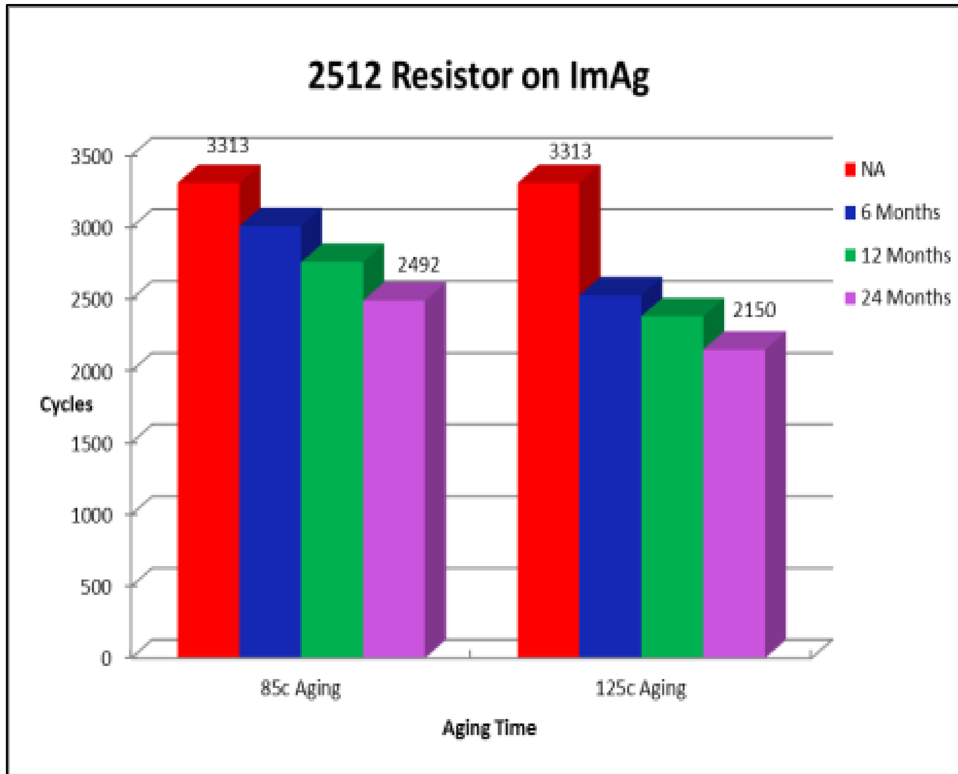


Figure 4.7 Degradation comparison of 2512 resistors, aging at 85°C and 125°C

Data shown in Figure 4.7 include the comparative failure data for the (SAC 305) 2512 resistors. The characteristic life of the resistors drops from 3313 cycles without aging to 2492 cycles after 2 years of aging at 85°C and from 3313 cycles to 2150 cycles at 125°C for 2 years. This corresponds to a 24.8% (85°C) and 35.1% (125°C) deterioration rate respectively. Table 4.1 provides the comparative characteristic life cycles and degradation for all three package types. Clearly, the 2512 resistor has higher reliability under isothermal aging and thermal cycling than the BGA due to its high stiffness body and relatively large area of contact with the metallization on both component and PWB sides of the solder joint. For BGA packages, the reliability performance were all reduced in half or even more when components subjected to high temperature isothermal aging, which brings a concern for applications on those packages with lead-free solder. In general, components subjected to higher aging temperatures over longer periods of time have larger degradation rates.

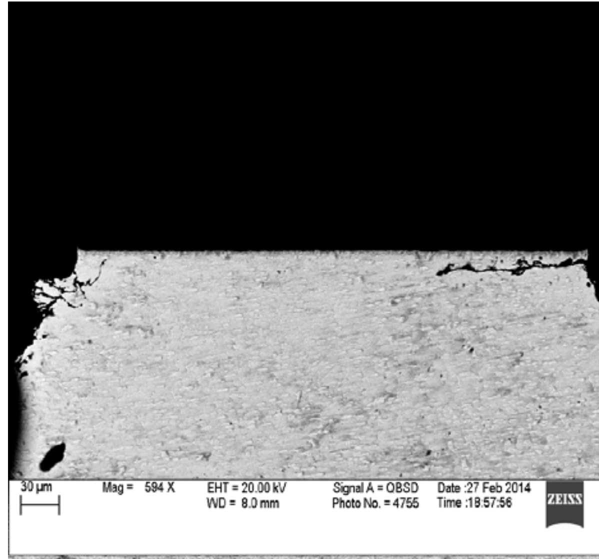
Table 4.1 Summary of Failure Data

		Characteristic Life η (cycles)				2-year Aging
		No Aging	6 Months	12 Months	24 Months	Degradation Rate
85℃	10mm SAC105	2419	1596	1439	1237	48.9%
	10mm SAC305	3329	2012	1874	1686	49.4%
	15mm SAC105	2926	1656	1596	1346	54.0%
	15mm SAC305	3743	2241	2107	1746	53.4%
	2512 Resistor	3313	3011	2761	2492	24.8%
125℃	10mm SAC105	2419	1116	1079	944	61.0%
	10mm SAC305	3329	1740	1551	1338	59.8%
	15mm SAC105	2926	1429	1325	1106	62.2%
	15mm SAC305	3743	2083	1884	1516	59.5%
	2512 Resistor	3313	2530	2383	2150	35.1%

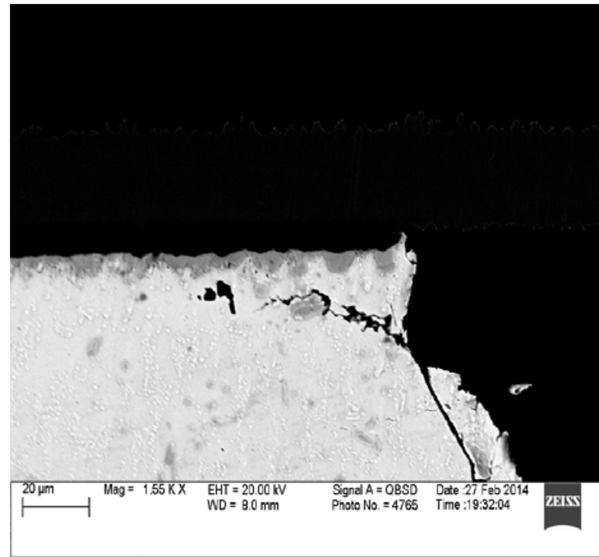
4.3 Failure Analysis

Since 1) intermetallic compound growth at both board and component sides of the solder joint; and, 2) grain coarsening during aging and thermal cycling are primary indicators of solder joint failure, we examined each factor by cross-sectioning several representative samples. Both 0.8mm and 0.4mm ball pitch solder joints after isothermal aging and thermal cycling were examined. Figure 4.8 shows typical backscattered electron images (BSE) for SAC105 and SAC305 0.8mm pitch BGA without aging and subsequent thermal cycling. Crack propagation for no aged samples usually at package side of the joint interface which is agreed by most current studies.

Figure 4.9 shows BSE image for SAC105 0.8mm pitch BGA joints after 12 months of aging at 125°C. For specimens aged at 125°C, the crack propagation path was typically on the PCB side of the solder joint along the Cu_6Sn_5 intermetallic layer. Figure 4.10 illustrates additional, representative SAC solder joints after aging at 125°C for two years. Cracks initially propagate at the corner of both component and board sides of the solder joints, and then proceed along the IMC layer.



(a)



(b)

Figure 4.8 Backscattered electron image for the No aging thermal cycled 0.8mm SAC 105 (a) and SAC305 (b).

Due to recrystallization during isothermal aging and thermal cycling, new grain boundaries are formed at the outer edge of a solder bump where the structure undergoes high plastic deformation [64] and encourages cracks. In some cases, we observe that the crack turns away from the IMC layer and enters the bulk solder.

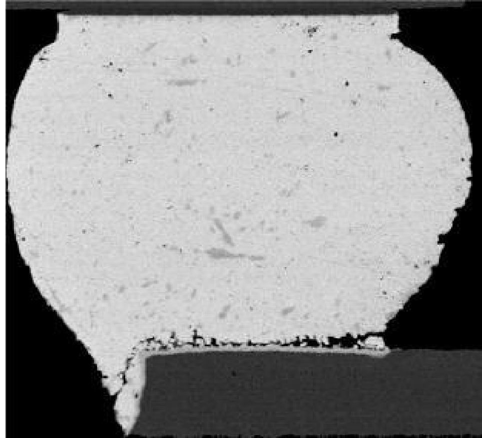
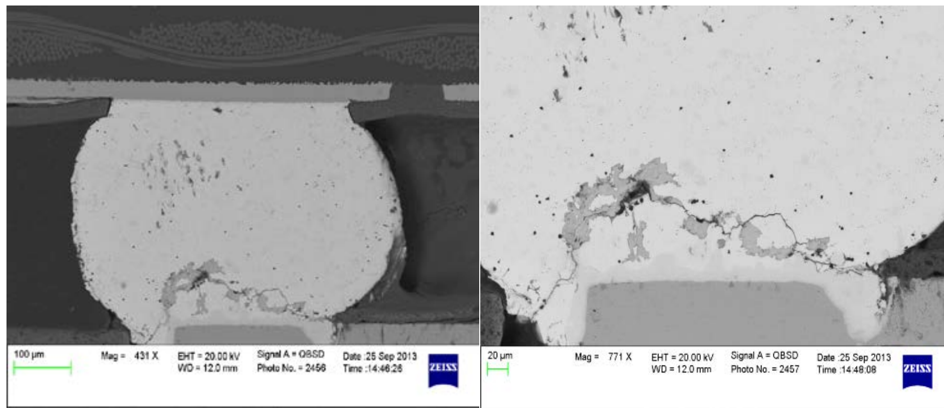
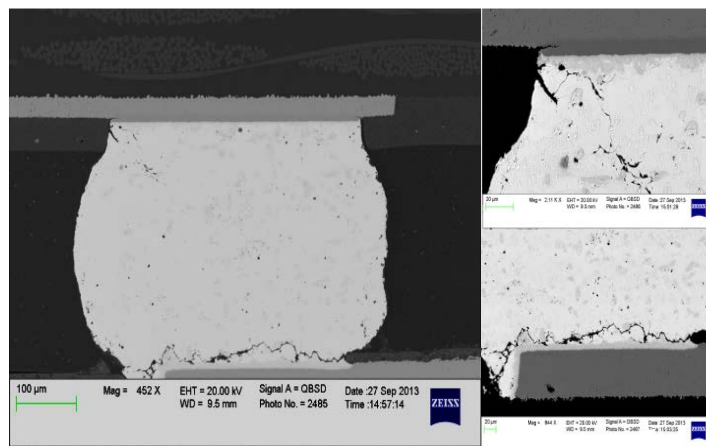


Figure 4.9 Backscattered electron image for the 0.8mm SAC 105 after 12 months of aging at 125°C



(a)



(b)

Figure 4.10 Representative backscattered electron images after 2-years of 125°C aging for the 0.8mm pitch (a) SAC105 package; (b) SAC305 package.

The bottom side Cu_6Sn_5 IMC adjacent to the copper layer initially forms during the reflow process by heterogeneous nucleation. Further reaction during aging and cycling forms a second, adjacent layer of Cu_3Sn between the copper pad and the Cu_6Sn_5 layer by solid state diffusion [69]. The intermetallic layers then grow over time and temperature, forming a brittle interface where failures typically occur.

Table IV and Figure 10 show that the thickness of the board side Cu-Sn IMC for both SAC alloys increases significantly during aging/cycling and is a primary reason for cracks along the board side during the long time, high temperature aged samples. Three thickness measurements were averaged along the intermetallic layer of three solder balls located at a left corner, center, and right corner line under a package.

Table 4.2 Board-Side, Sn-Cu IMC Layer Thickness vs. Aging Time

0.8mm pitch BGA SAC105/SAC305	No Aging (µm)	6 month 125°C Aging (µm)	12 month 125°C Aging (µm)	24 month 125°C Aging (µm)
SAC105	1.71	6.74	7.98	11.64
SAC305	1.83	6.45	9.04	13.90

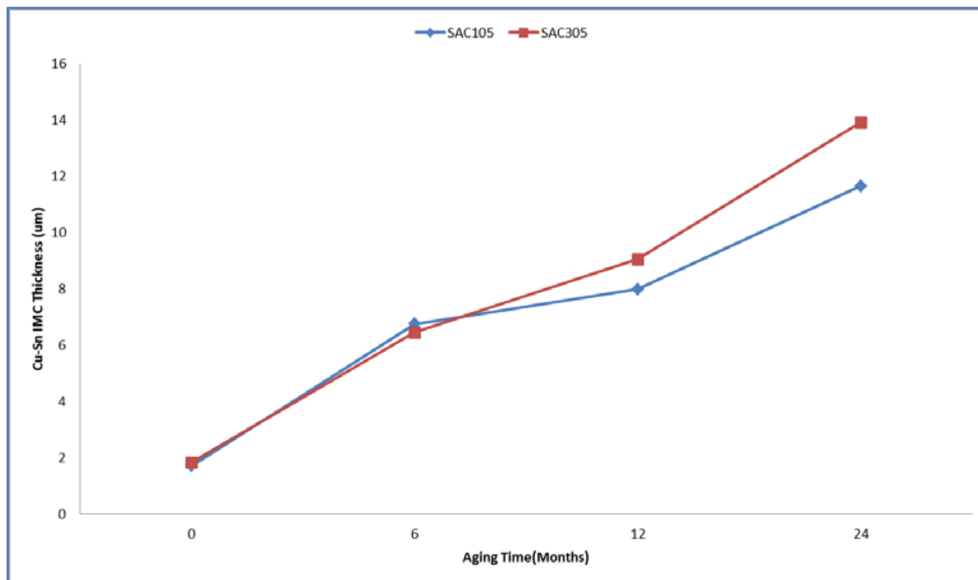


Figure 4.11 Increase in board side 0.8 mm SAC IMC thickness vs. aging time

The characteristic starting microstructure of SAC alloys contains Sn matrix with imbedded Ag_3Sn second phase particles. SAC alloys with greater Ag content have higher Ag_3Sn

particle densities. After aging at elevated temperatures, it is clear that the Ag_3Sn particles undergo coarsening caused by solid state diffusion [76]. The Ag_3Sn particles coarsen and block the crack paths, which in turn increase the joint structural stability and enhance grain gliding and dislocation movement, which affects creep deformation. Figure 4.12 showed a clear Ag_3Sn IMC particles reduction during high temperature aging. Figure 4.13 and Figure 4.14 verified the composition of SAC alloy joint PWB side IMC by applied the EDX line scan and point scan. Large Cu_6Sn_5 can also be found at bottom region of the joint.

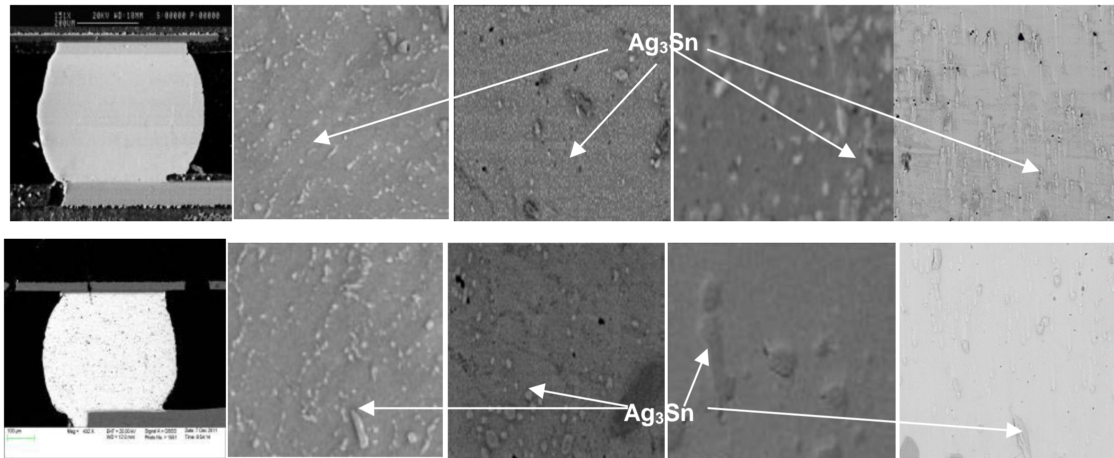


Figure 4.12 Ag_3Sn observations during aging time (No aging, 6 months, 12 months and 24 months) at 125°C for SAC105 (top) and SAC305 (bottom)

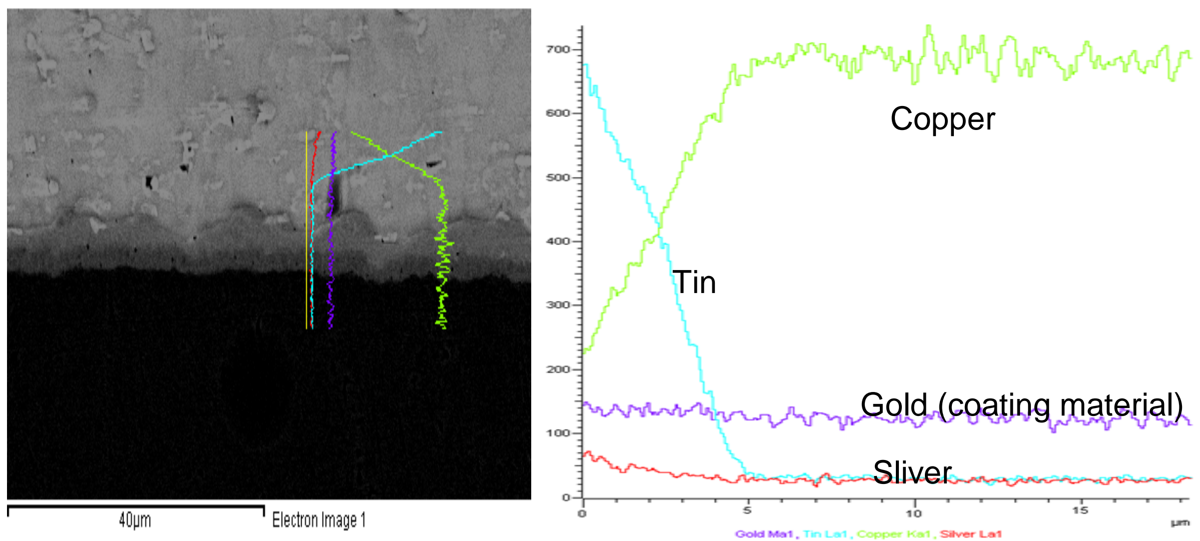


Figure 4.13 EDX Line scan on 0.4mm pitch SAC105 package with 24 months 85°C aging

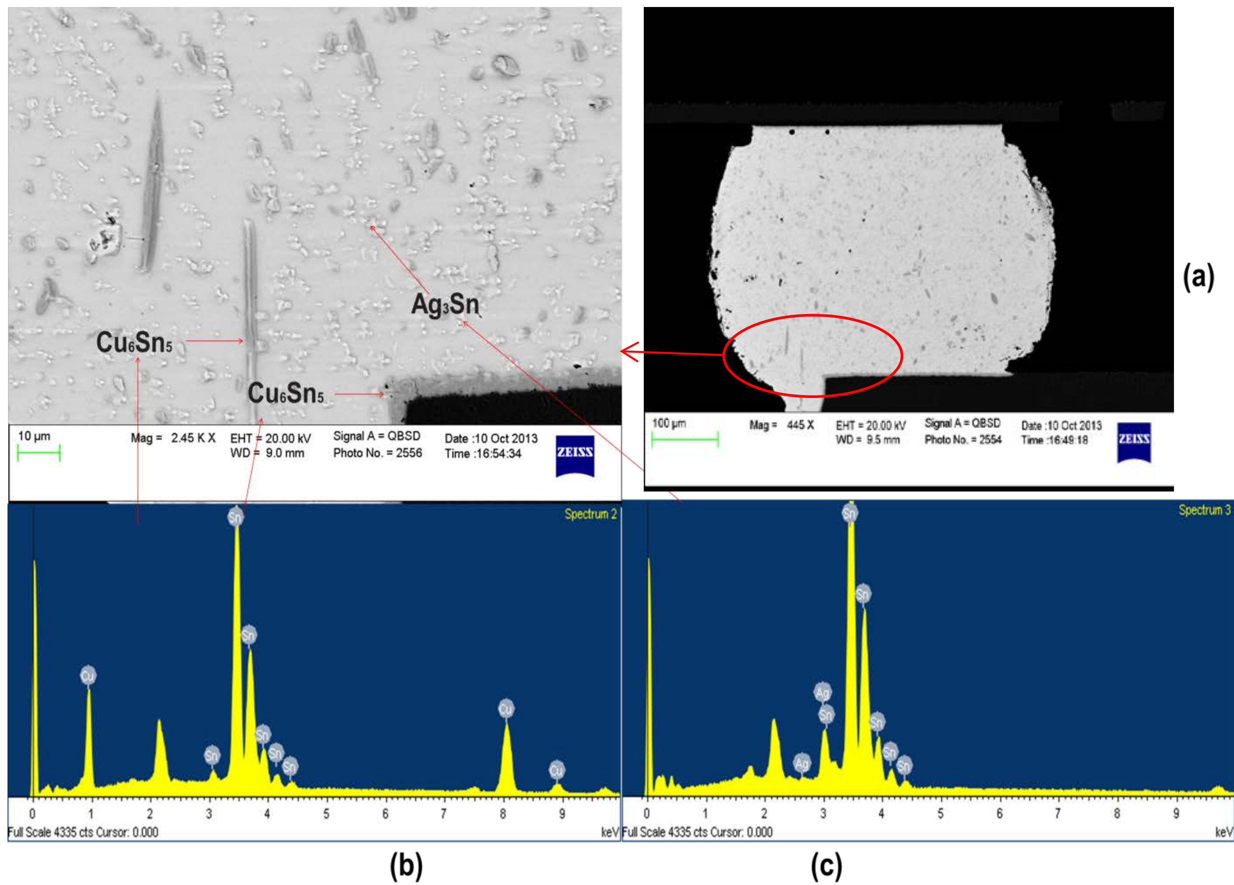
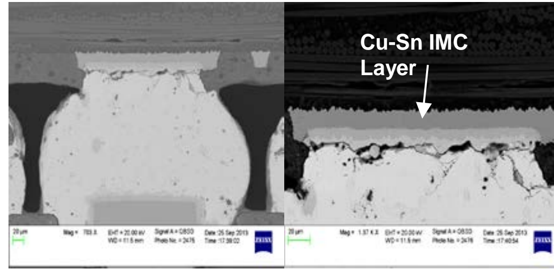
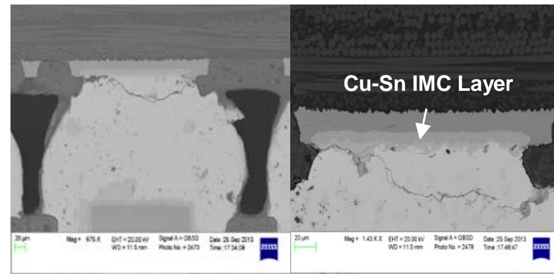


Figure 4.14 Low and High mag SEM image of 0.8mm pitch SAC105 after 24 month aging at 85°C (a); EDX Analysis of Cu_6Sn_5 IMC (b) and EDX Analysis of Ag_3Sn IMC (c).

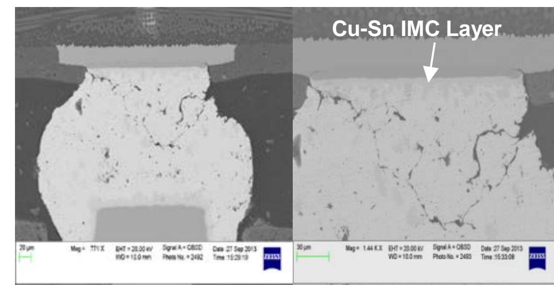
Different failure modes/crack propagation directions were observed in smaller pitch (0.4 mm) SAC balls after two years of aging, shown in Figure 4.15. Figure 4.15 (a) shows crack propagation along the package side IMC layer; Figure 4.15 (b) shows cracks which form initially at the package side IMC layer but then extend into the solder bulk; Figure 4.15 (c) shows cracks going directly through the solder bump; Figure 4.15 (d) shows the crack located at voids at the corner of board side; and Figure 4.15 (e) shows cracks propagating along the Cu_6Sn_5 IMC layer, through the solder bulk, but also along the plate-like Ag_3Sn IMC.



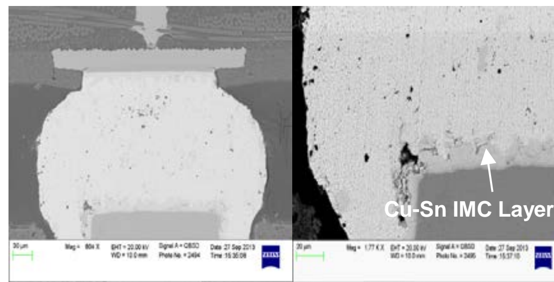
(a)



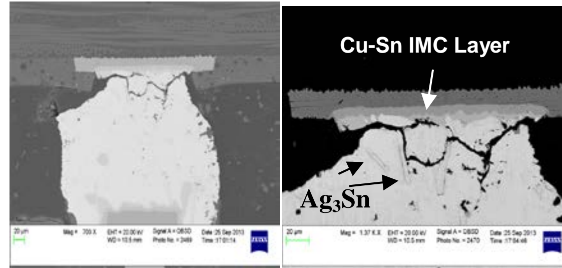
(b)



(c)



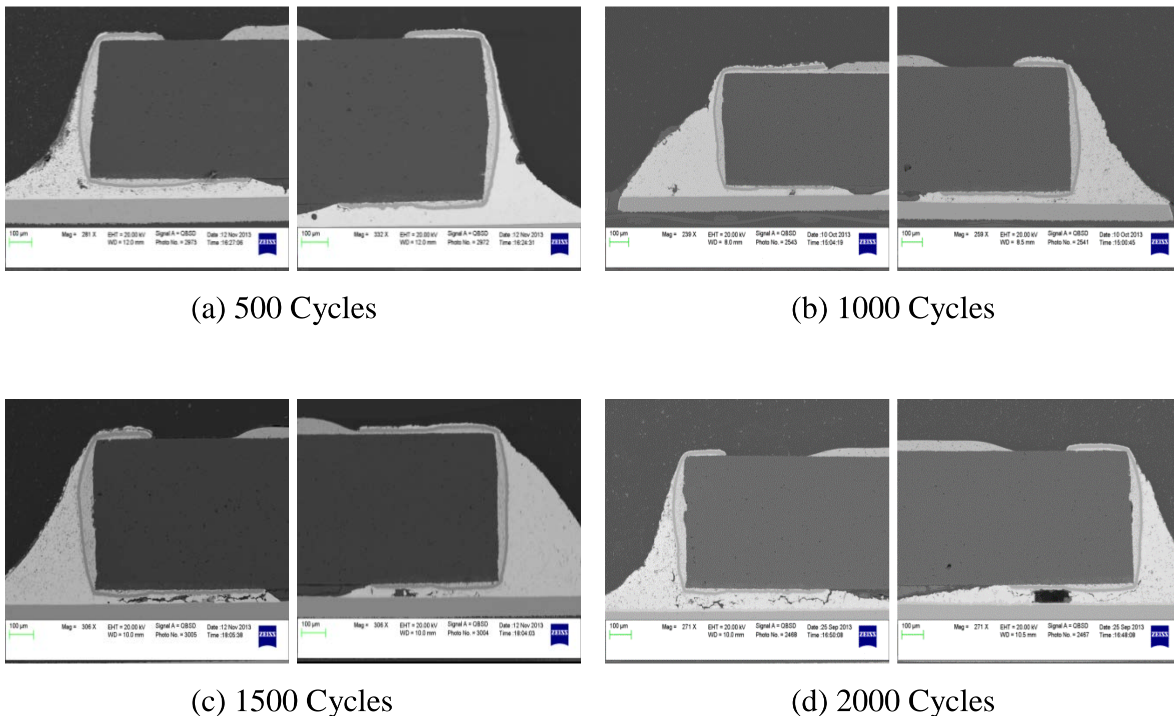
(d)



(e)

Figure 4.15 Failure modes for 0.4 mm pitch SAC alloys after 2 years, 125°C aging: (a, b) SAC105 and (c, d, e) SAC305 packages.

We expected extensive cracking in the 2512 resistors due to the high stiffness and large CTE mismatch with the substrate during large temperature swings. Further, according to Qi, et al. [36], which used finite-element modeling to predict resistor package failures in Pb-free alloys, crack initiation locations should correspond to the maximum strain and stress locations in the chip resistor package.



(a) 500 Cycles (b) 1000 Cycles

(c) 1500 Cycles (d) 2000 Cycles

Figure 4.16 Cracks in 2512 SAC305 chip resistor joints as a function of thermal cycle number

Figure 4.16 provided the observations in our experiment using SAC alloys, which shows representative SEM cross-sections vs. cycling time for SAC 305, 2512 resistors aged at 125°C for 12 months. After 1000 thermal cycles (Figure 4.16 (b)), large voids are observed underneath the resistor which seems to originate in the early stages of the fatigue life. In Figure 4.16 (c) and (d), the initiated crack propagated underneath the component and then extended along a path parallel to the resistor termination until an open circuit occurred.

4.4 Discussion and conclusion

A significant degradation in reliability has been observed for both SAC105 and SAC305 in 10mm packages on ImAg during elevated temperature isothermal aging. There were 49% and 50% reductions in characteristic lifetime for SAC105 and SAC305 after 24 months 85°C aging, respectively. After 2 years aging at 125°C, the package lifetime decreased by 61% for SAC105 and nearly 60% for SAC305. In case of 15mm BGA package, the degradation of reliability aging at 85°C of SAC105 and SAC305 were 54% and 53, namely. The reduction of life cycle aging at 125°C of SAC105 and SAC305 were 62% and 60%, respectively. Compare with previous results [68-71] which was one year aging reliability degradation rate ranging within 40% to 55%, the extra aging time continuously but not significantly affecting the joint reliability by 10% to 15%. For passive 2512 resistors, the reliability performance was reduced 25% and 35% after 24 months of aging at 85°C and 125°C respectively.

Failure analysis showed dramatic intermetallic Sn-Cu growth at the board-side solder joint interfaces over aging and cycling times which caused by Cu diffusion from bottom trace and newly formed a uniformed IMC layer (known as second-phase IMC, mainly Cu_3Sn_4 [79]). After 125°C aging, the cracks appeared at the lower corners at the board side interface and propagated along the Sn-Cu IMC. Different, new failure modes were discovered for fine-pitch packages which were also observed in our previous studies [70, 71]. Reduced Weibull lifetimes occur coincidently with increasing Sn-Cu layer growth at board and package sides of the solder joint. Resistor cross-sections revealed that cracks initiated at the ends beneath the resistor before propagating through the entire interconnection. In related work in our laboratory, Cai, et al. [77] has studied doped SAC-X alloys (X = 0.1% Bi) and finds similar joint degradation with aging for all aging temperatures (25, 50, 75, 100 and 125°C) in the experimental matrix. We are currently exploring the manufacturability of new doped alloys and board level reliability in our ongoing work.

Chapter 5

TV7-Phase II Reliability and Failure Analysis

5.1 Introduction

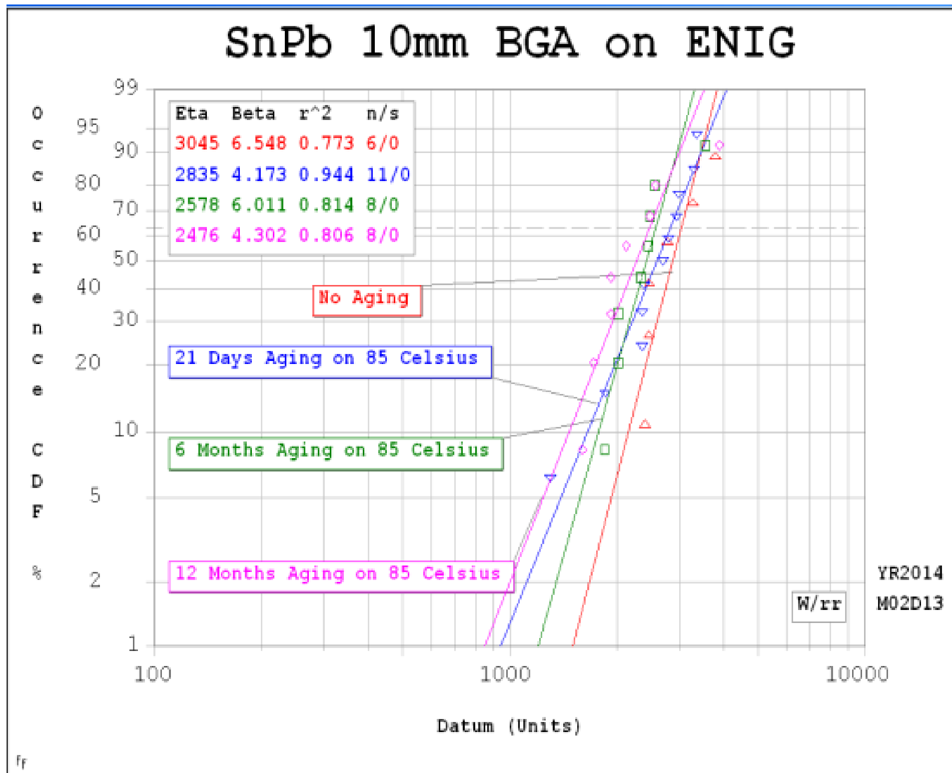
A familiar harsh environment is exposure to elevated temperatures for prolonged periods of time, commonly called aging. The purpose of the study is to determine the effect of isothermal aging on the reliability of Sn-Ag-Cu (SAC) assemblies. We employed two different board finishes which have received increased attention in packaging applications, (ENIG) electroless Ni/immersion Au and (ENEPIG) electroless Ni/ electroless Pd / immersion Au.

ENIG and ENEPIG surface finishes are outstanding due to their superior wettability and oxidation resistance, due to the inert Au layer between solder and pad. The Ni layer is employed as a diffusion barrier to prevent rapid Cu dissolution into the solder. The Pd layer in ENEPIG improves the wettability and acts as a diffusion barrier as well. The two board finishes were included in this test along with a mixed choice of SAC105, SAC305, and Sn-37Pb solders. The assembled test vehicle is shown in Figure 3.4. The daisy designed fine pitch PBGA packages measured 5x5m, 10x10mm, 15mmx15mm, and 7×7 mm CSP, 5×5 mm MLF and a series of 2512 resistors with SAC305 solder paste (Table 3.4).

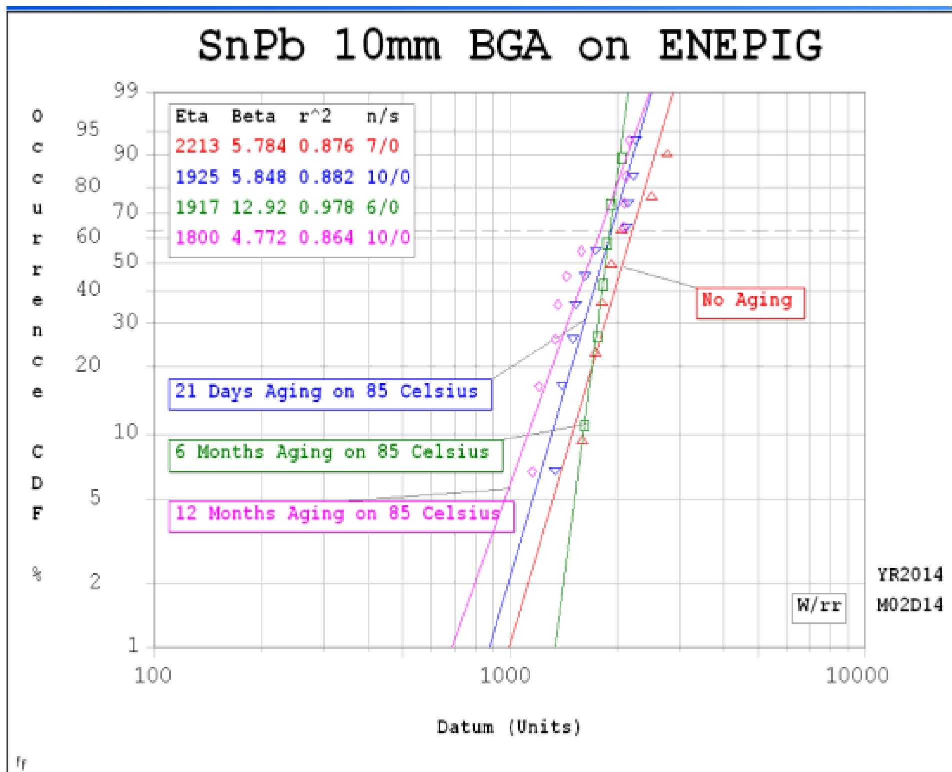
5.2 Reliability Data Analysis

5.2.1 10mm PBGA Package

Figure 5.1 illustrates the thermal cycling results on 85°C isothermally aged SnPb and Pb-free 10mm BGA packages on two surface finishes. The characteristic lifetime reduction can be observed clearly from the Weibull plots.



(a)



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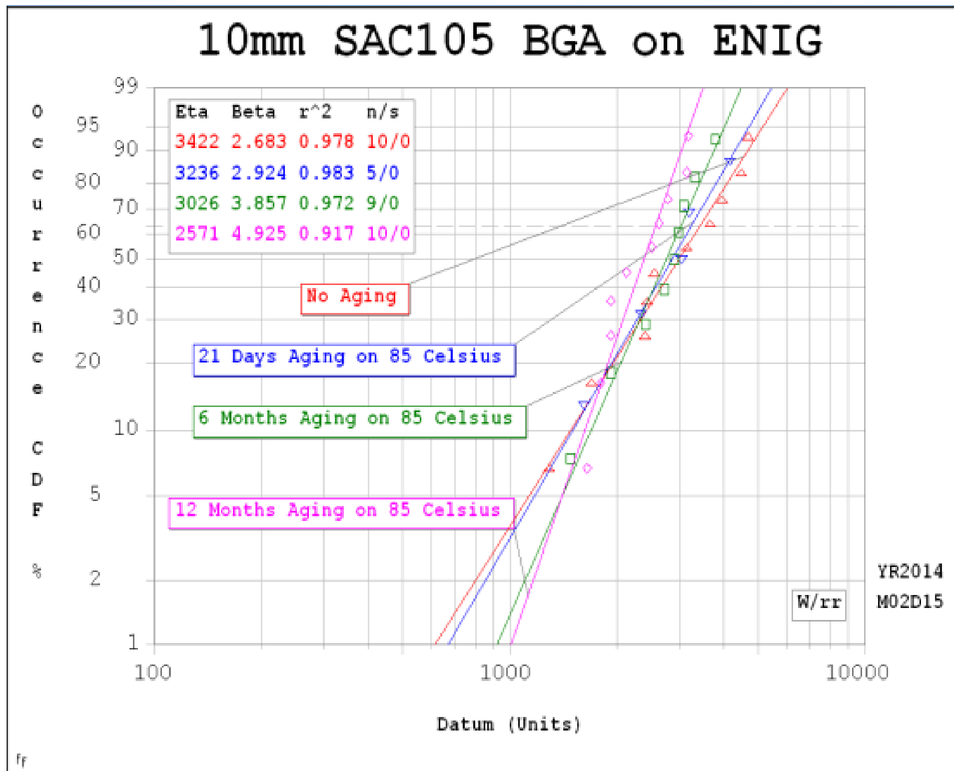

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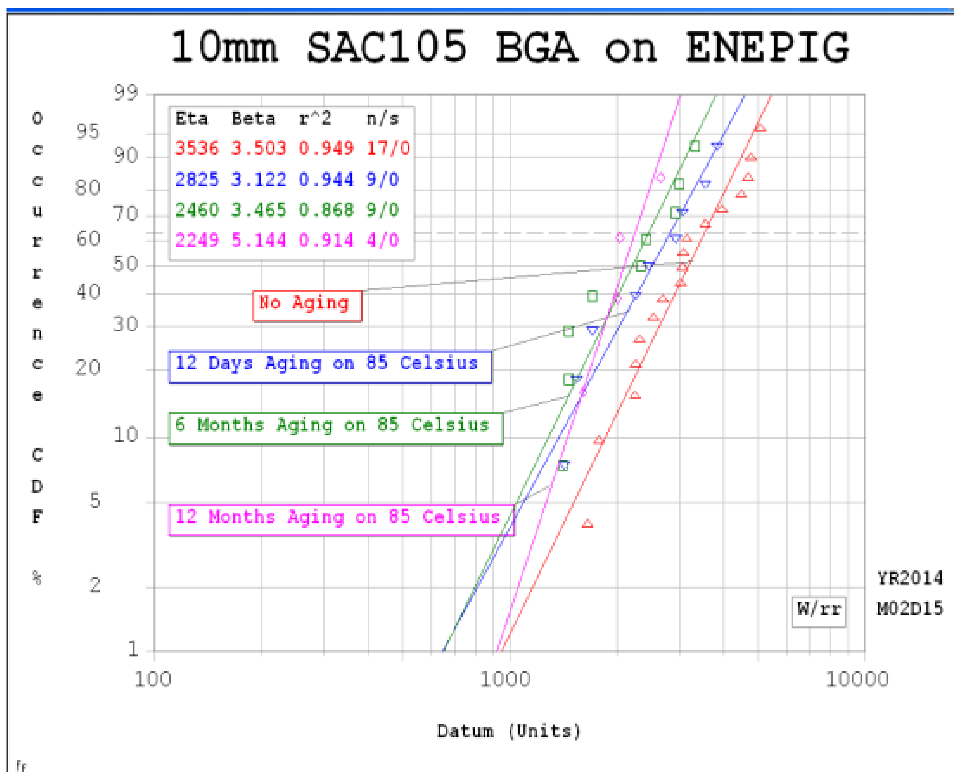

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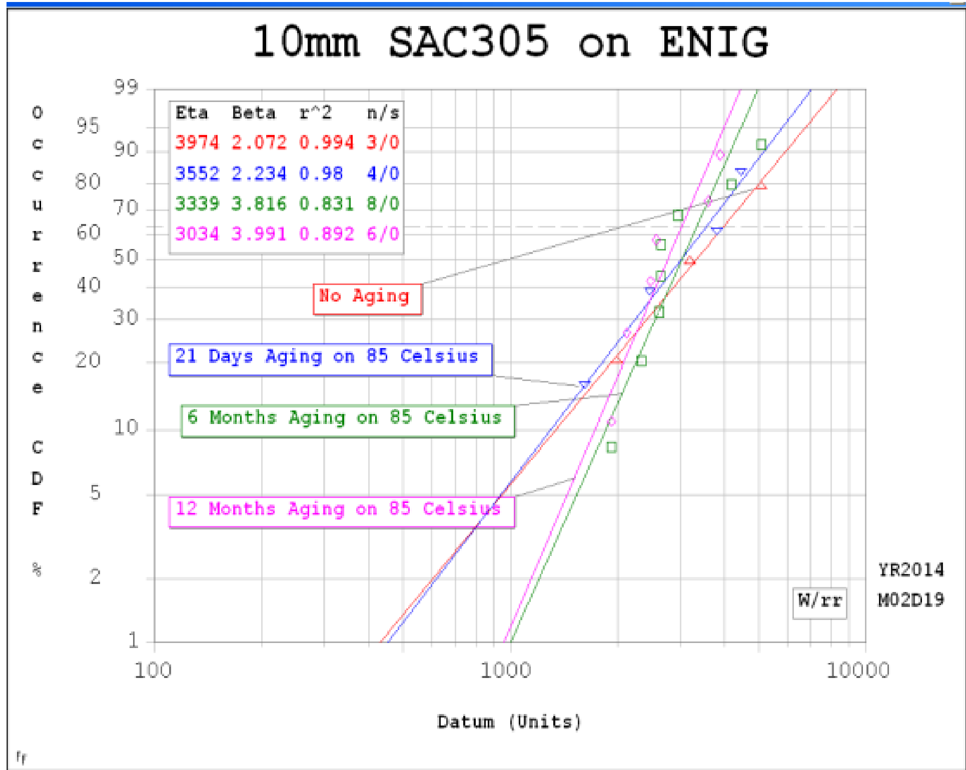

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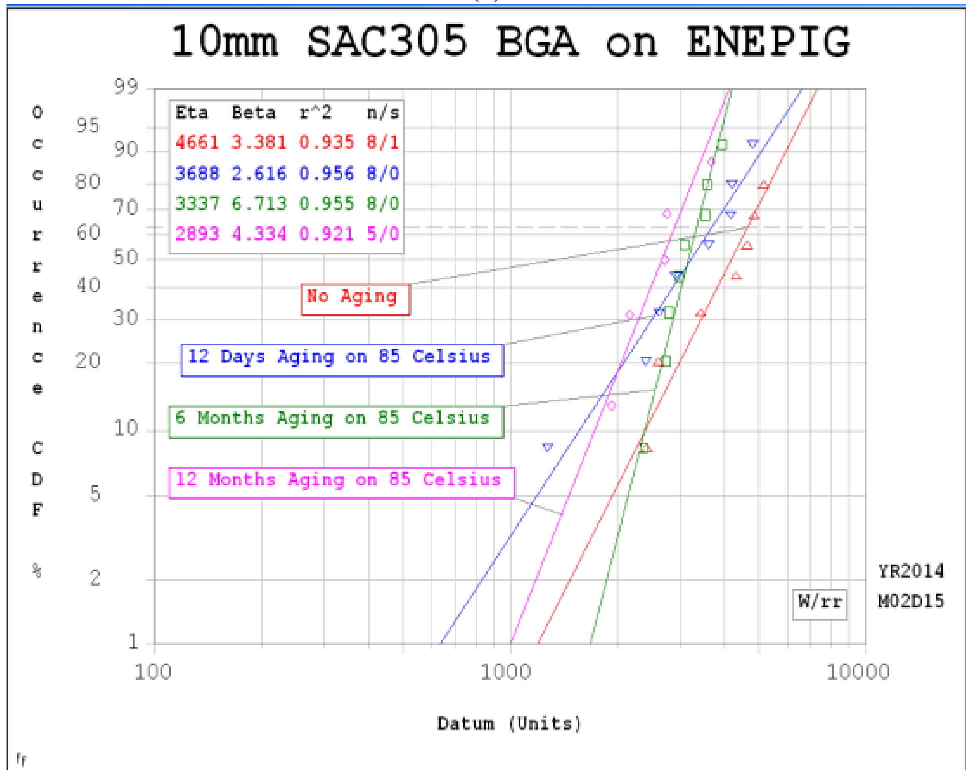
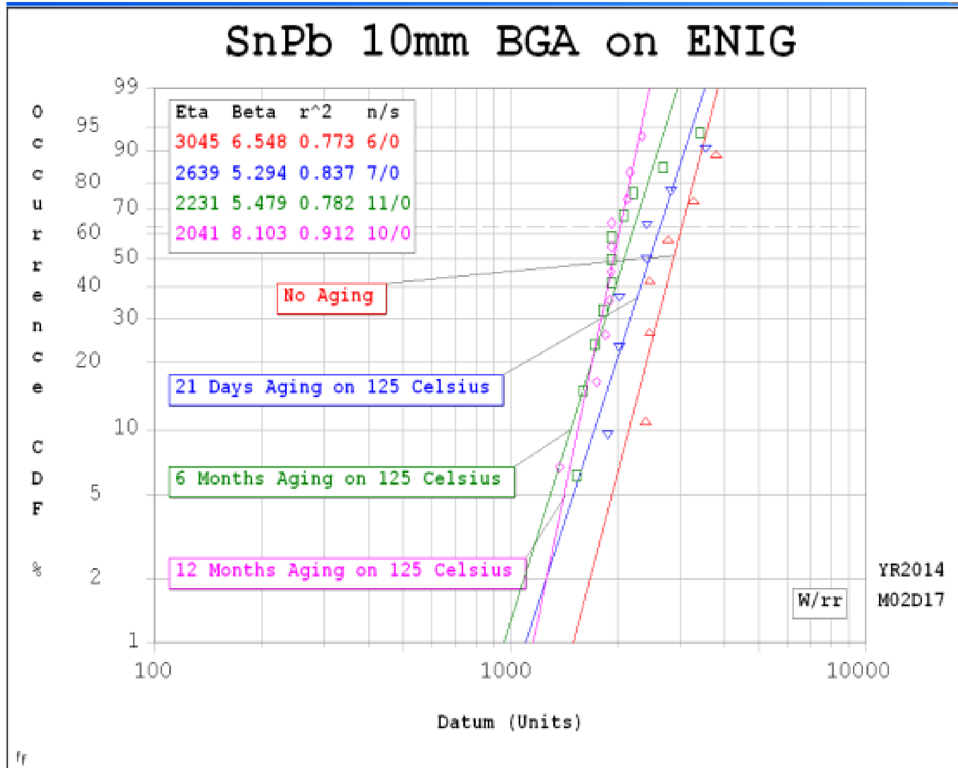


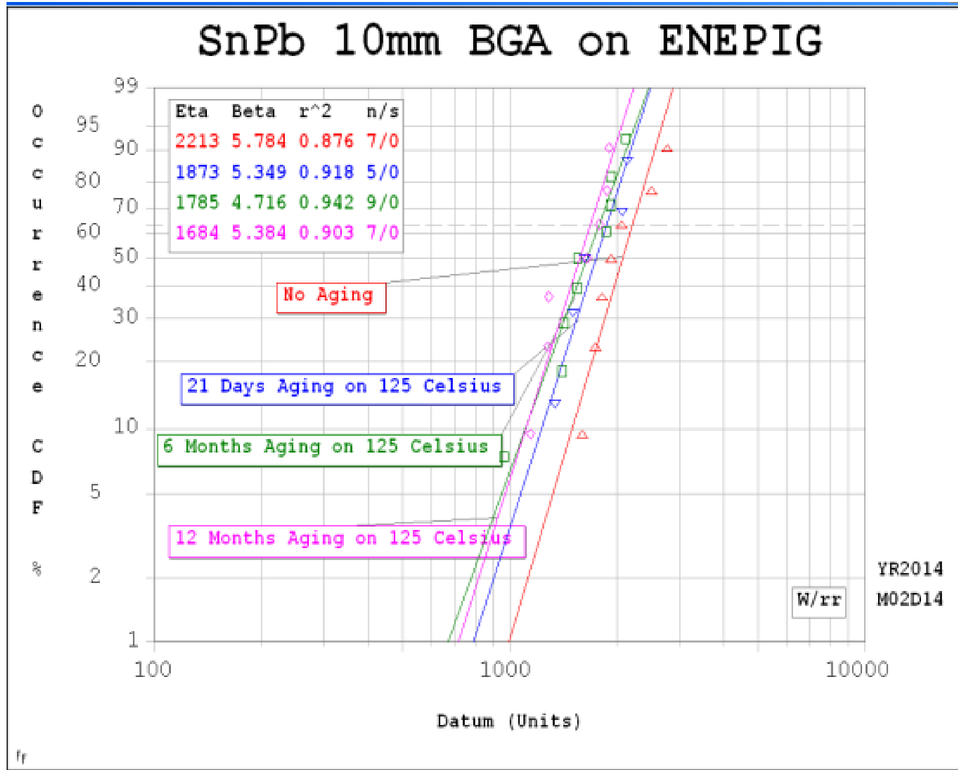
(f)

Figure 5.1 Weibull plost for 10mm BGA package subjected to 85°C aging: SnPb solder on ENIG (a), SnPb solder on ENEPIG (b), SAC105 solder on ENIG (c), SAC105 solder on ENEPIG (d), SAC305 solder on ENIG (e) and SAC305 solder on ENEPIG (f).

With increasing aging time, the reliability performance of the 10mm BGA continually reduces and this trend applies to all types of solder alloys. The comparison between various SAC alloys shows that SAC 305 has a longer characteristic lifetime than SAC105 on both surface finishes.



(a)



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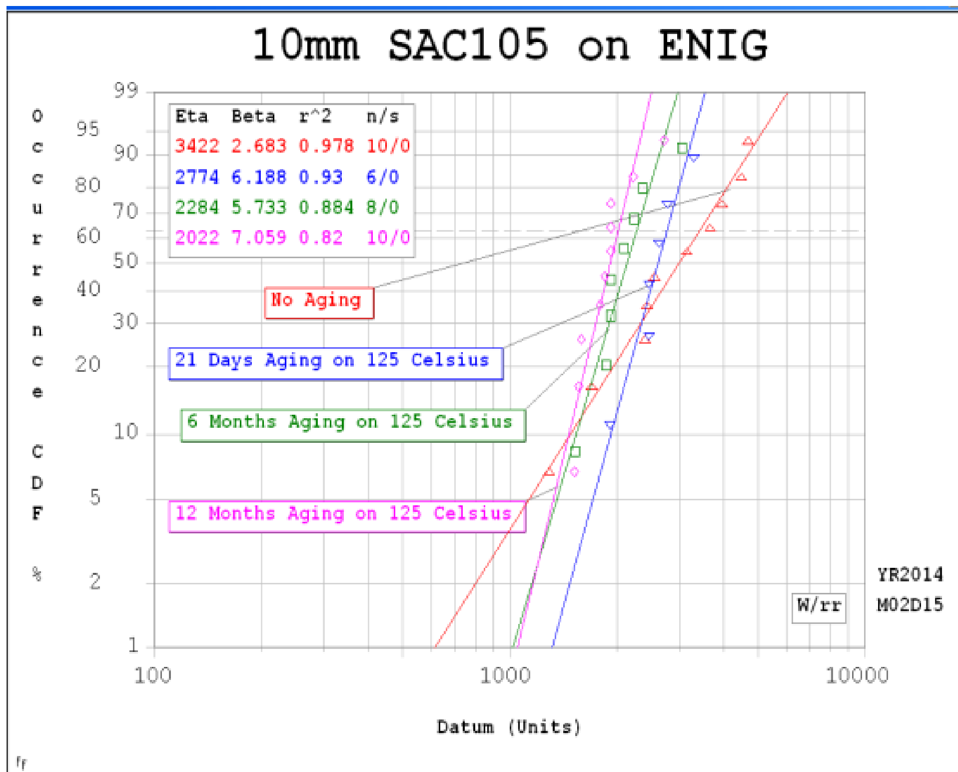

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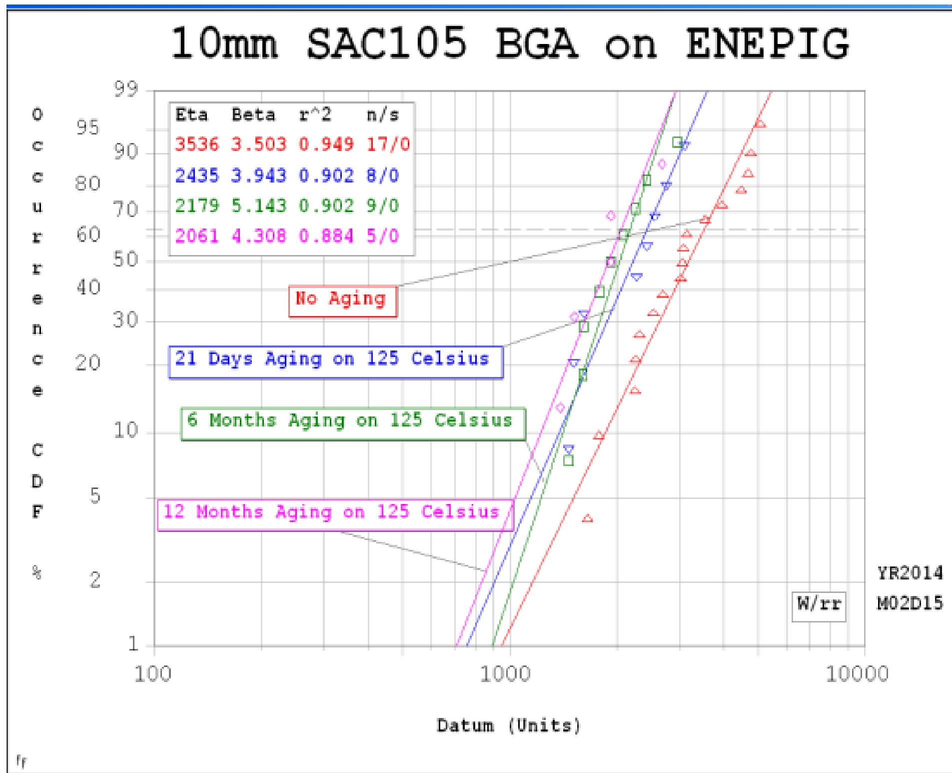

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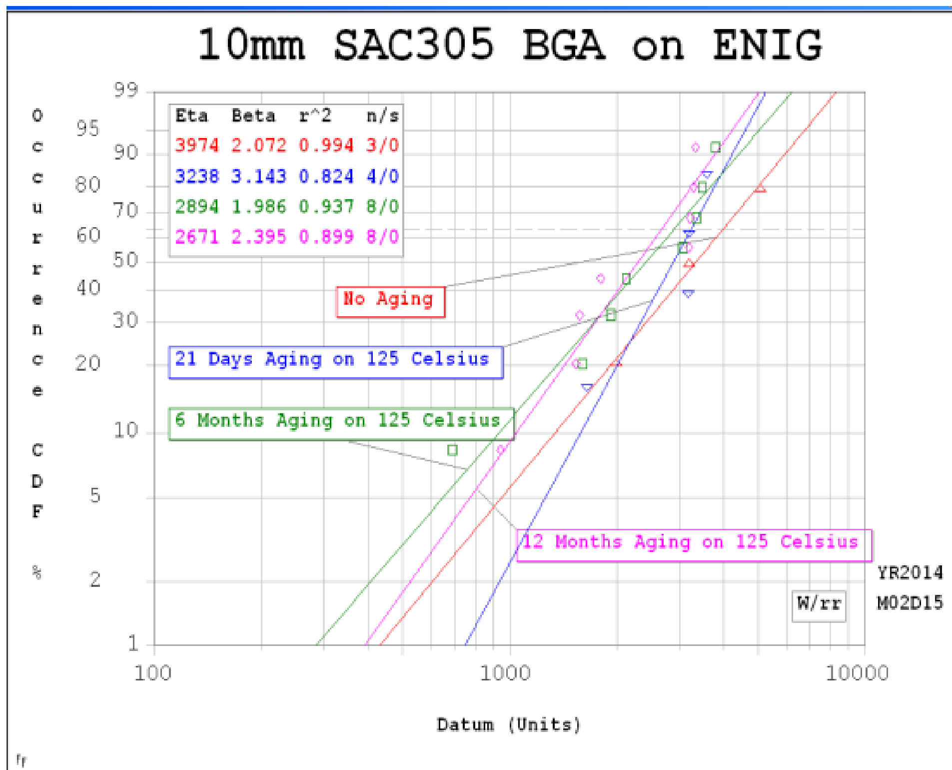

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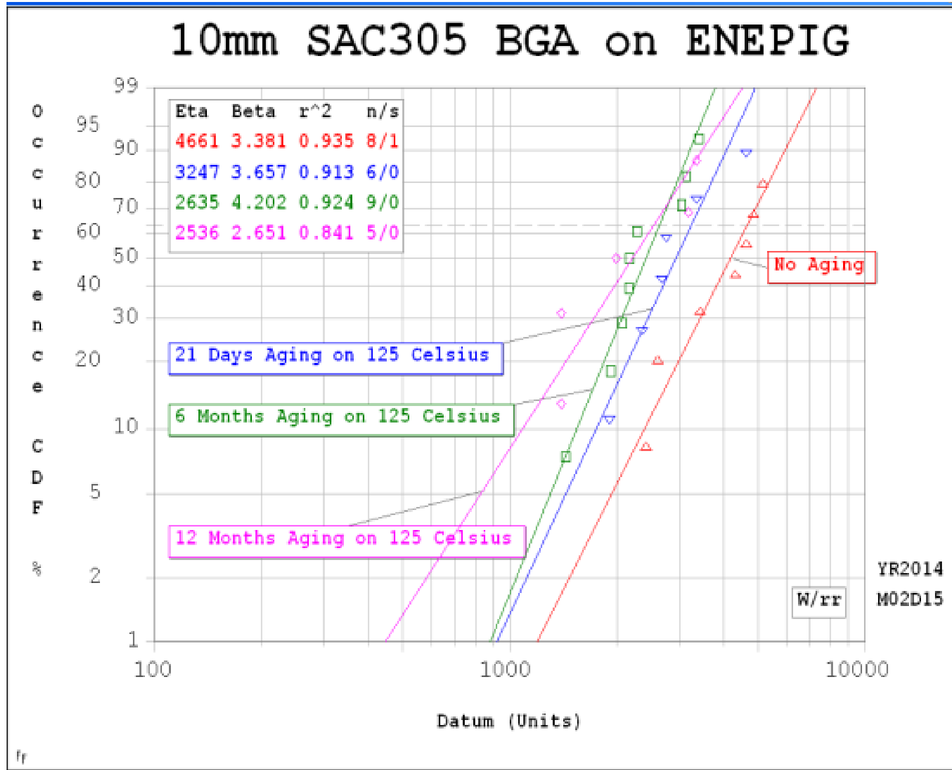


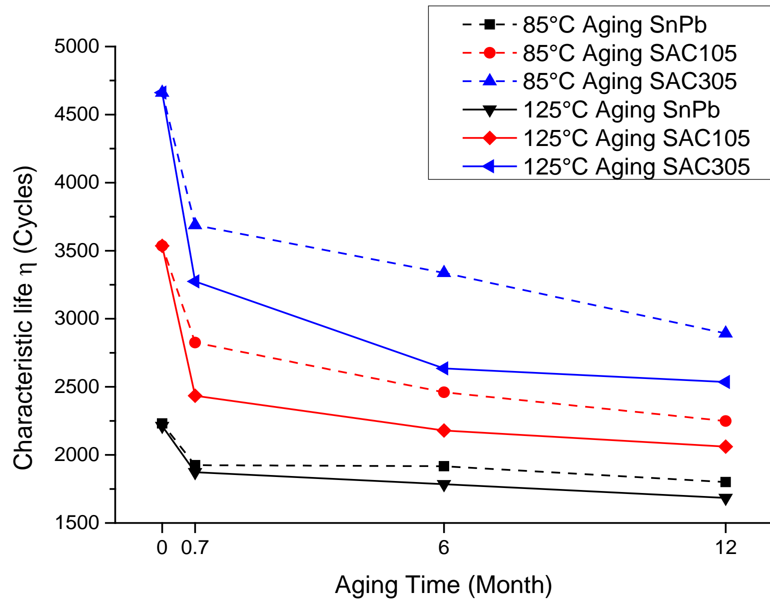
(f)

Figure 5.2 Weibull plost for 10mm BGA package subjected to 125°C aging: SnPb solder on ENIG (a), SnPb solder on ENEPIG (b), SAC105 solder on ENIG (c), SAC105 solder on ENEPIG (d), SAC305 solder on ENIG (e) and SAC305 solder on ENEPIG (f).

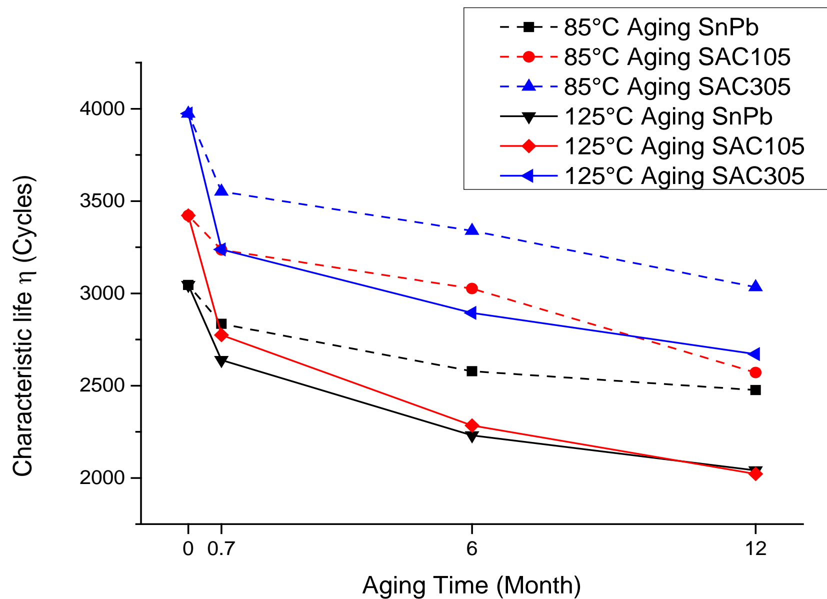
Figure 5.2 shows the 125°C aging data for the same test condition as the 10mm packages. A dramatic degradation in reliability is observed for both Sn-37Pb and SAC alloy solder joints. In Figure 5.2 (a), the characteristic lifetime for no aging Sn-37Pb 10mm package on ENIG was 3045 cycles; it dropped down to 2041 cycles after 12 months/125°C aging, which was a 33% degradation on reliability. In Figure 5.2 (b), same Sn-37Pb component under the same test conditions but on ENEPIG showed deterioration almost 24% from 2213 cycles to 1684 cycles after aging. The Weibull plots in Figure 5.3(a) and Figure 5.3(b) provide a clear baseline for Pb-free data comparisons.

Figure 5.2 (c) to (f) show data for SAC alloys. For SAC 105, the data deterioration was 40.9% on ENIG and 41.7% on ENEPIG. SAC305 generally has a better characteristic lifetime than SAC105 under 85°C aging. For no-aging data, SAC305 performed 500 cycles better on ENIG and over 1000 cycles more than SAC105 on ENEPIG. Even after 125°C aging, SAC305 still survives 500 and 600 cycles longer than SAC105 on ENIG and ENEPIG, respectively. If

one only considers SAC305 data in degradation; they still have a 32.8% and 45.6% reliability reduction on ENIG and ENEPIG, namely.



(a)



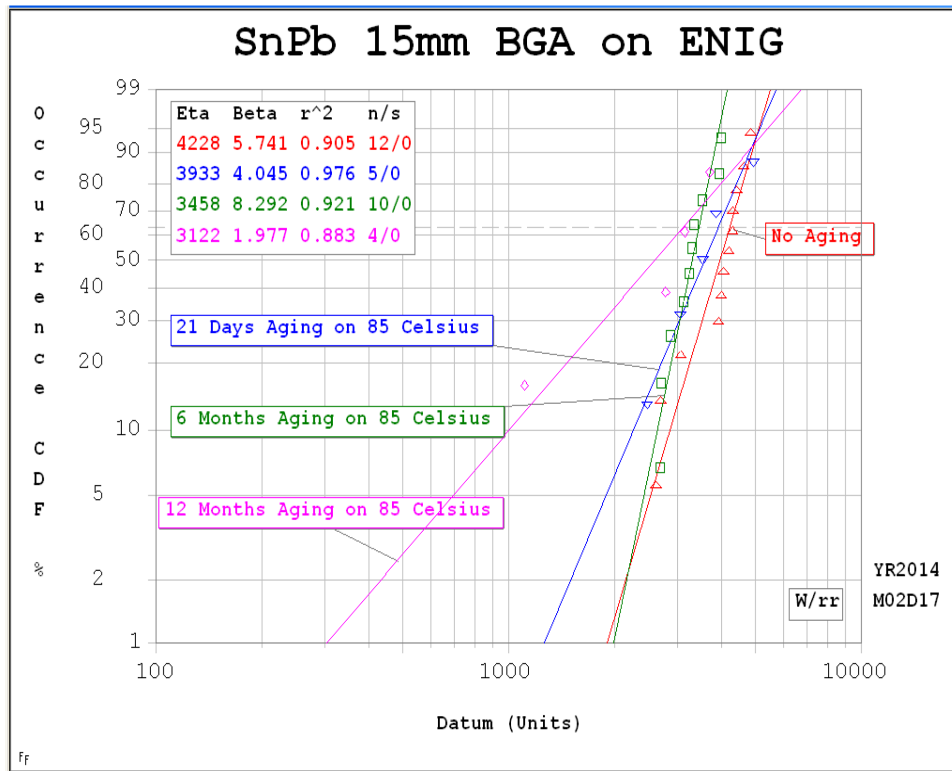
(b)

Figure 5.3 Summary of 10mm BGA reliability performance for ENIG (a) and ENEPIG (b) board finishes

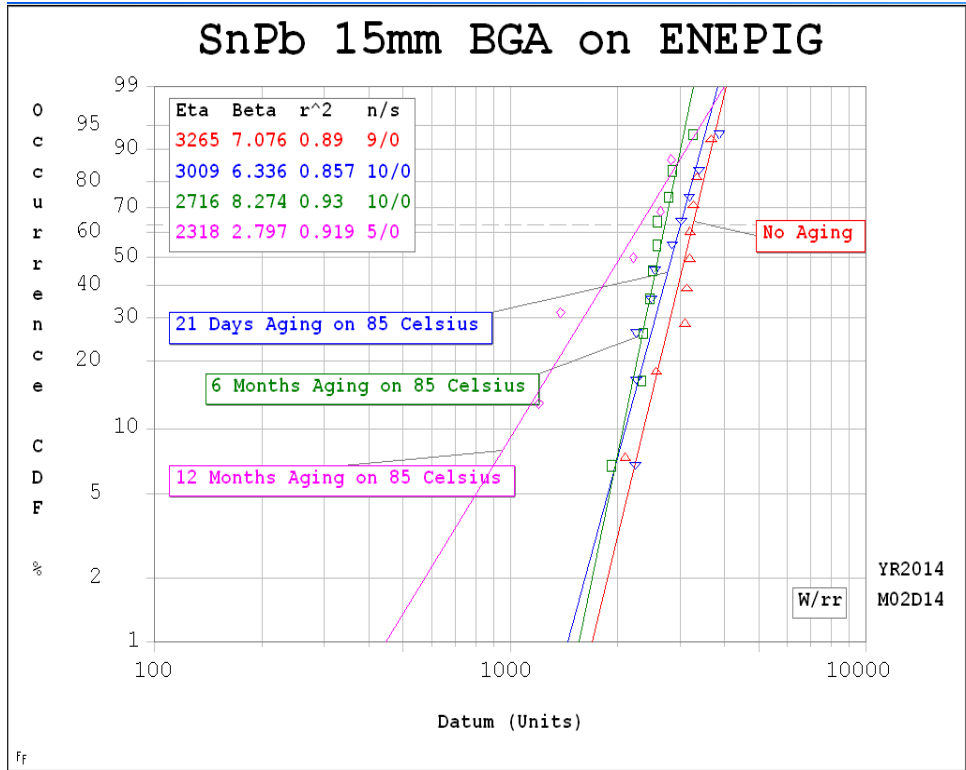
Figure 5.3 compares ENIG and ENEPIG reliability at both aging temperatures, showing how quickly the impact on reliability occurs. As early as 21 days into the aging, there is a significant drop in reliability for all packages at both 85°C and 125°C, indicated by dashed and solid lines, respectively.

5.2.2 **15mm PBGA Package**

The Weibull plot below demonstrated the thermal performance of 15mm BGA on different board plating.



(a)



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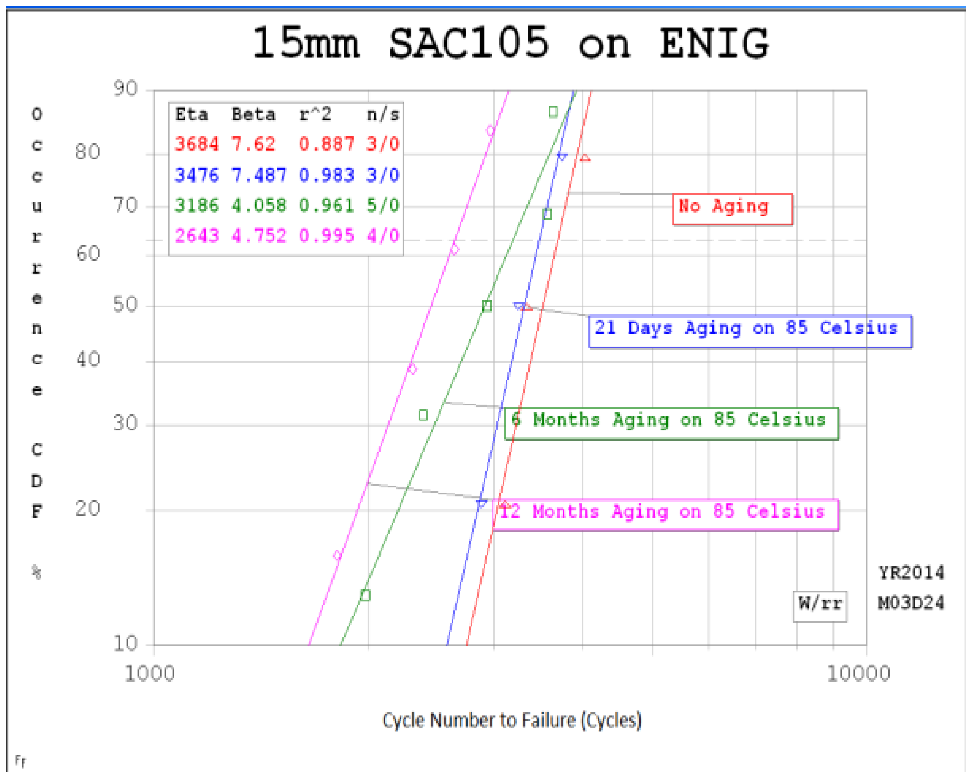

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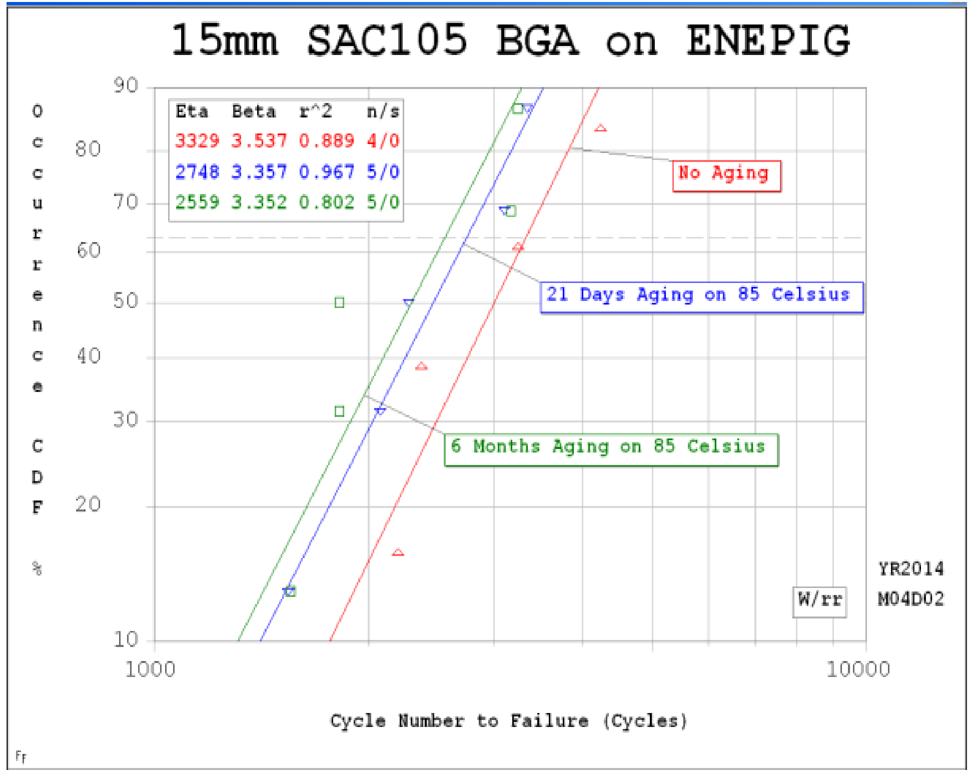

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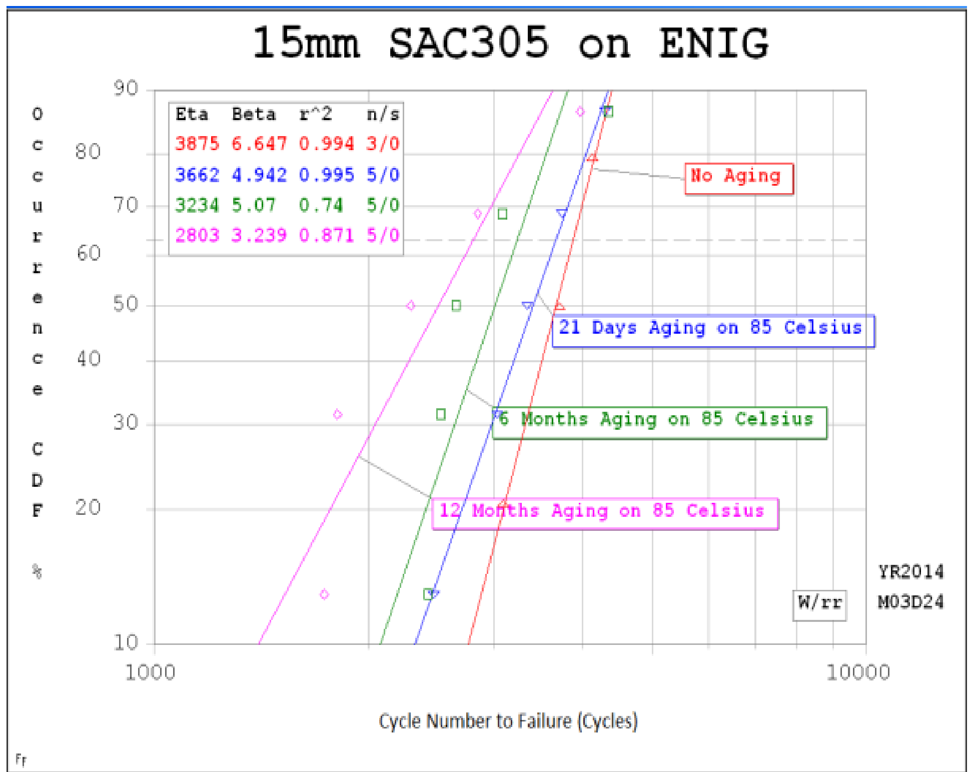

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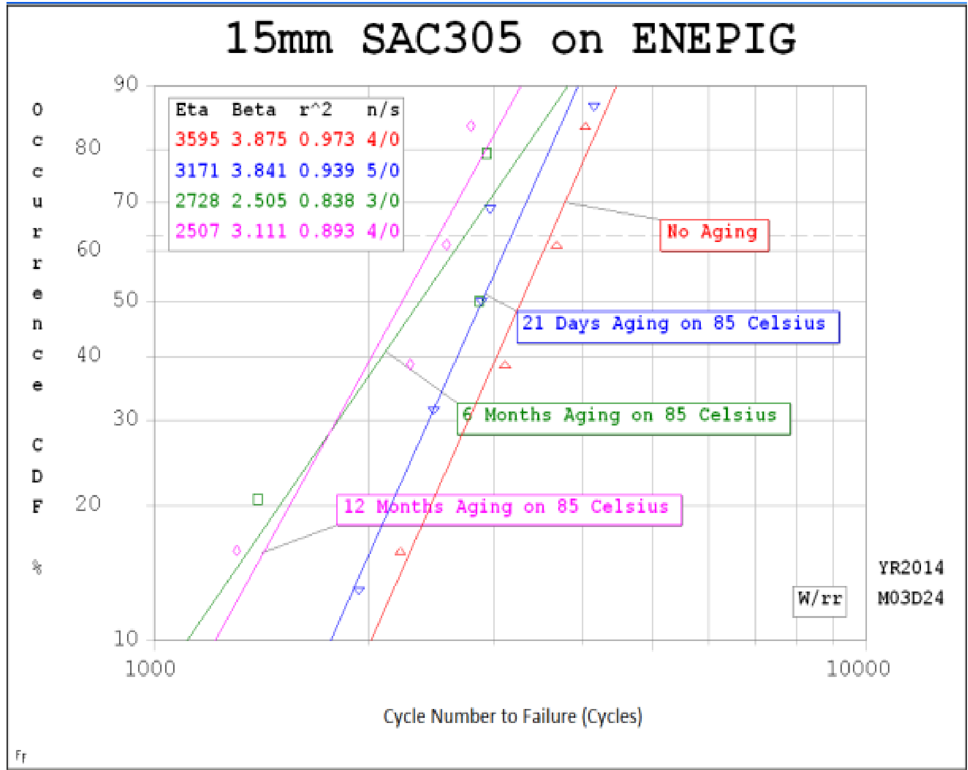
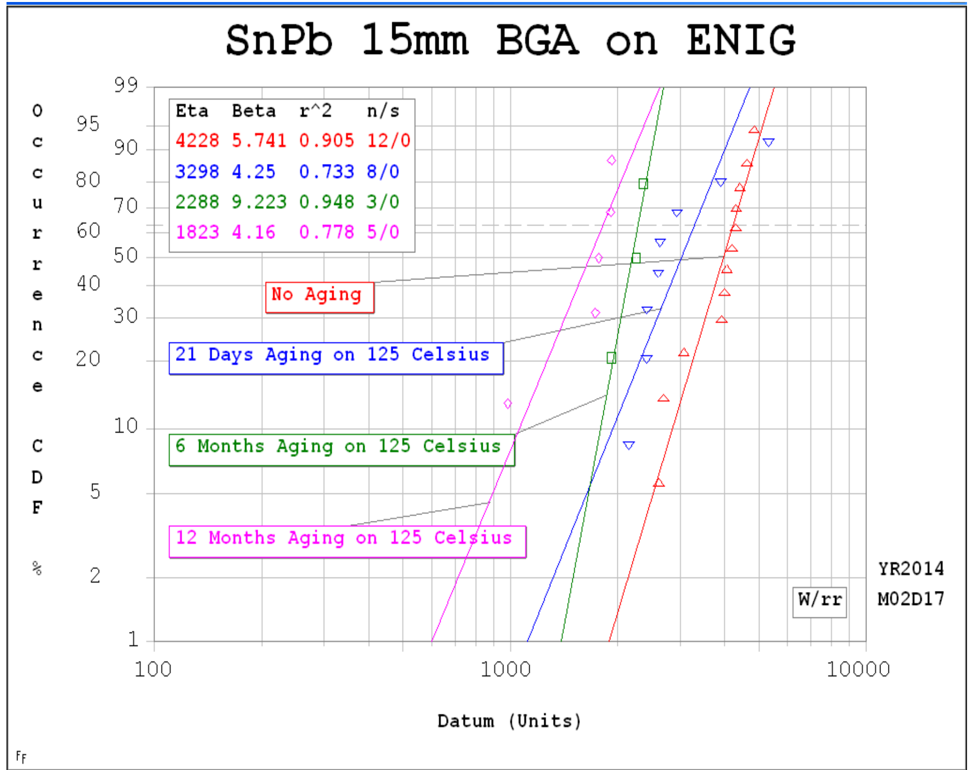
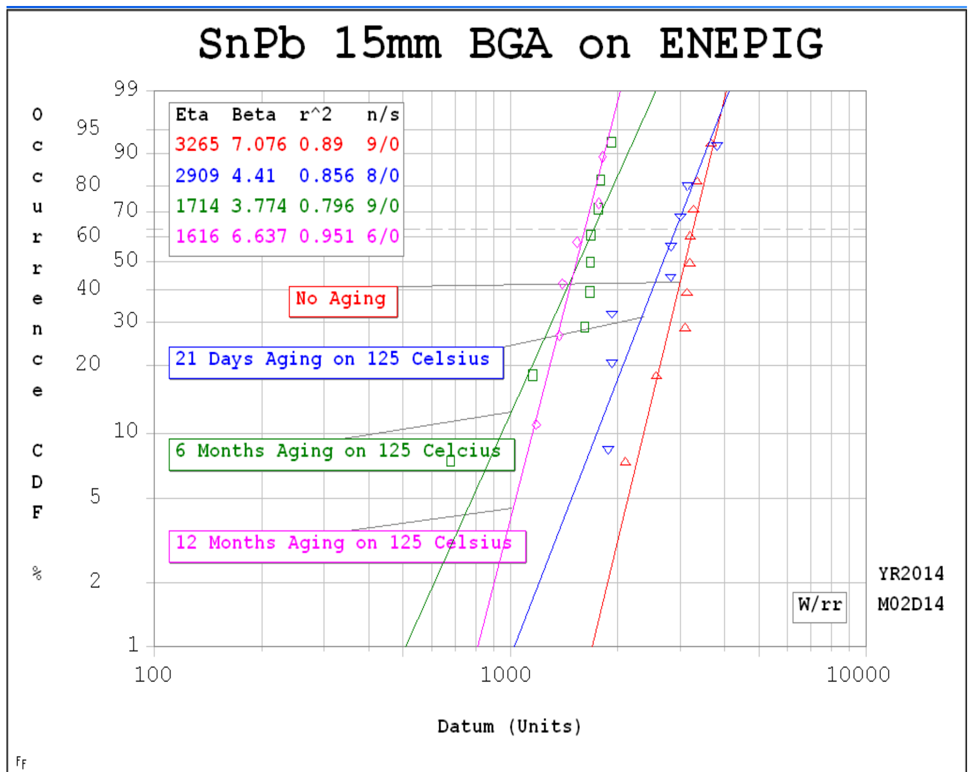


(f)

Figure 5.4 Weibull plost for 15mm BGA package subjected to 85°C aging: SnPb solder on ENIG (a), SnPb solder on ENEPIG (b), SAC105 solder on ENIG (c), SAC105 solder on ENEPIG (d), SAC305 solder on ENIG (e) and SAC305 solder on ENEPIG (f).



(a)



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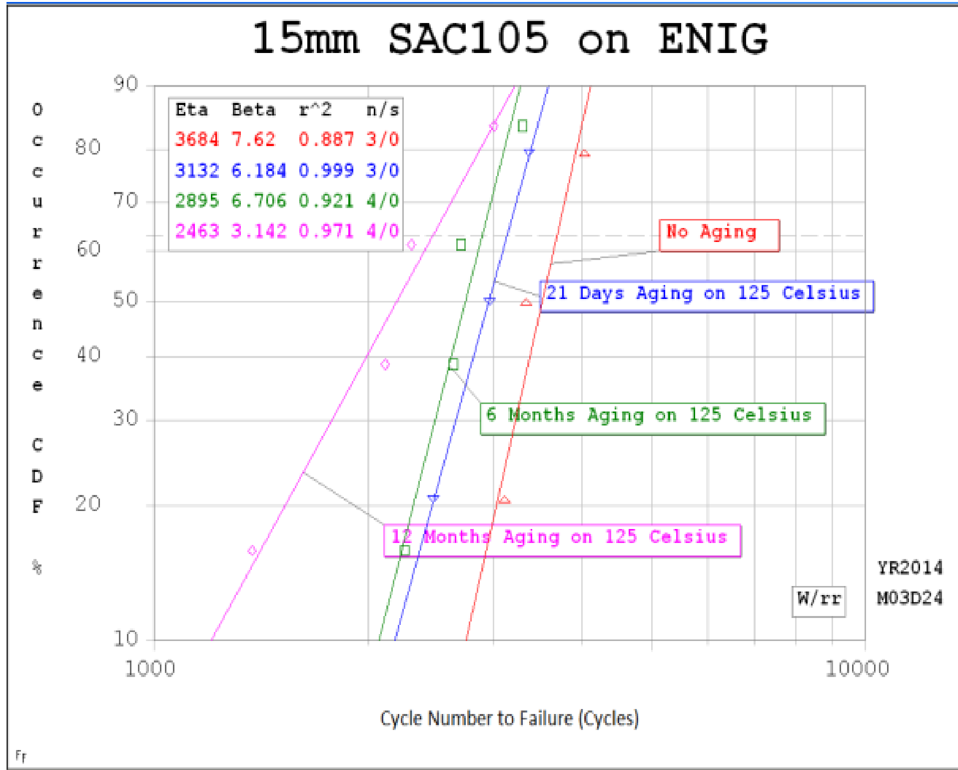

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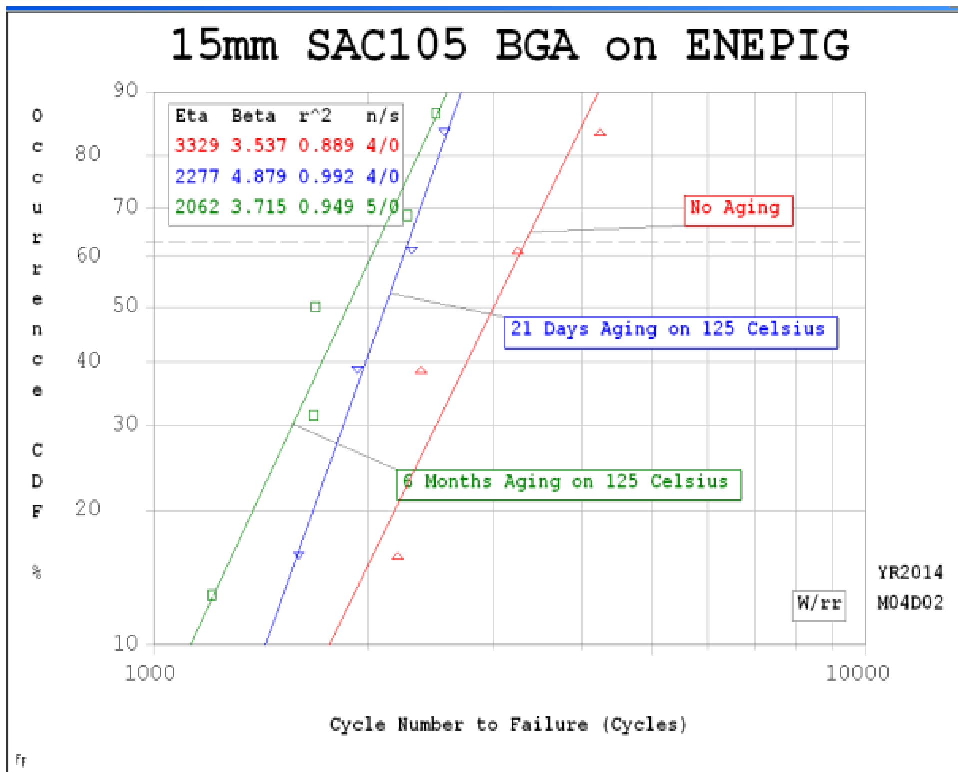

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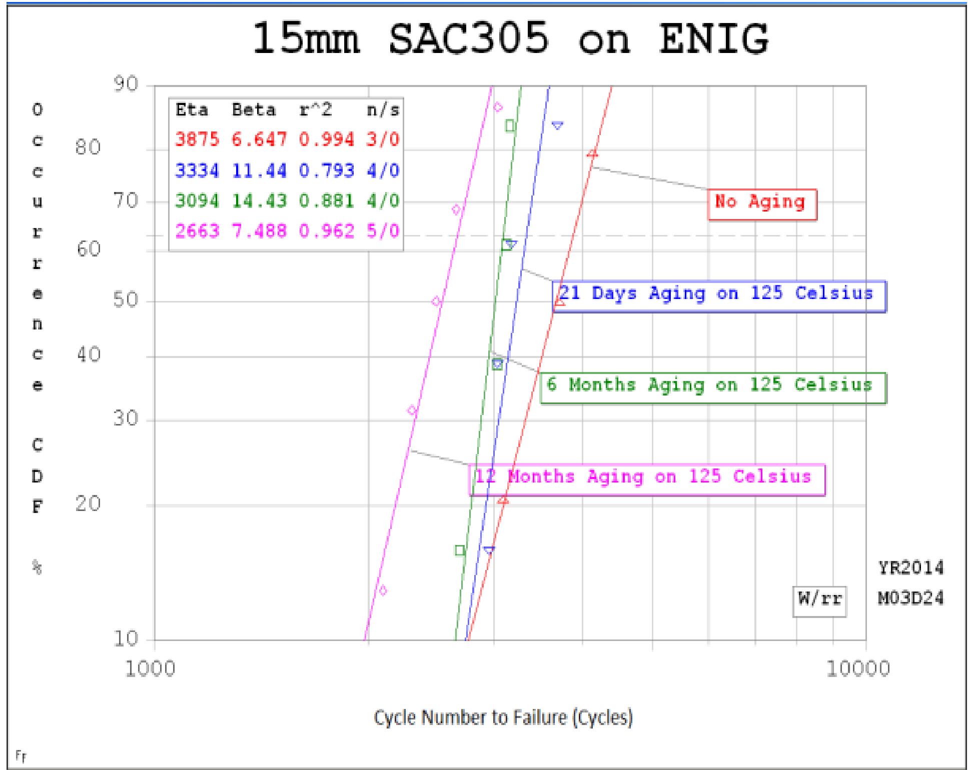

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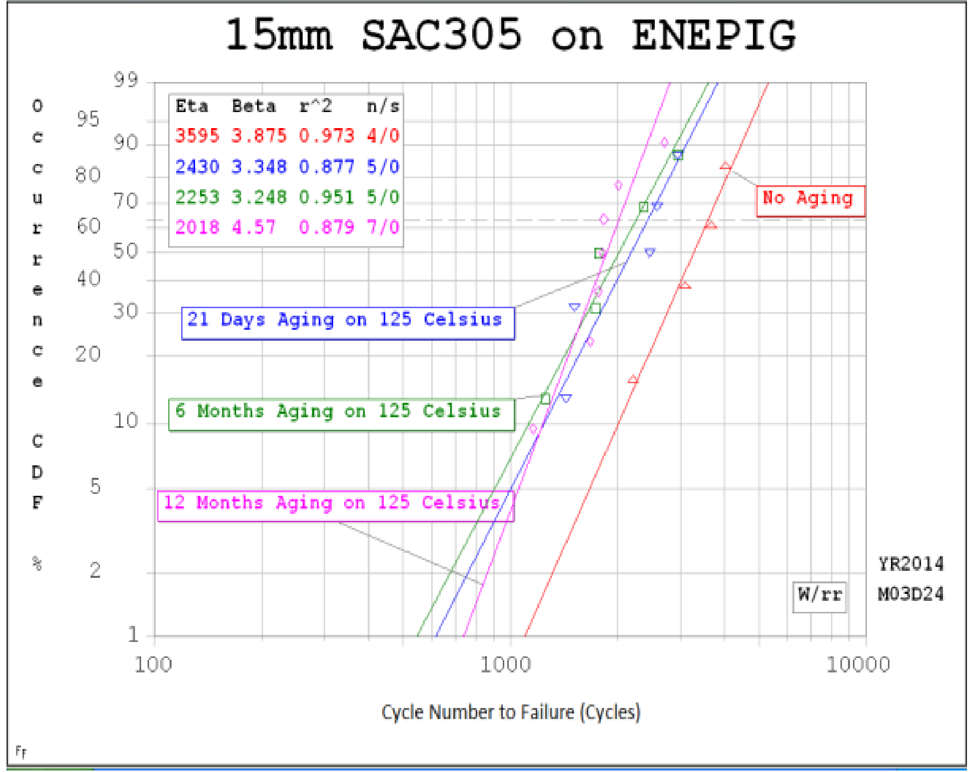


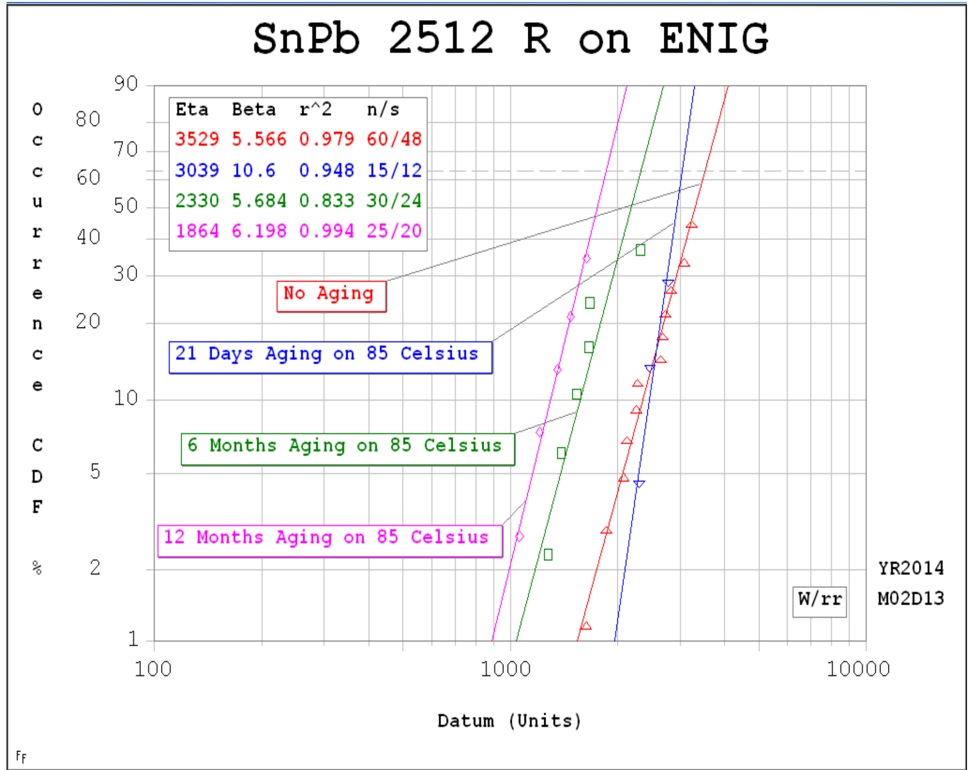
(f)

Figure 5.5 Weibull plost for 15mm BGA package subjected to 125°C aging: SnPb solder on ENIG (a), SnPb solder on ENEPIG (b), SAC105 solder on ENIG (c), SAC105 solder on ENEPIG (d), SAC305 solder on ENIG (e) and SAC305 solder on ENEPIG (f).

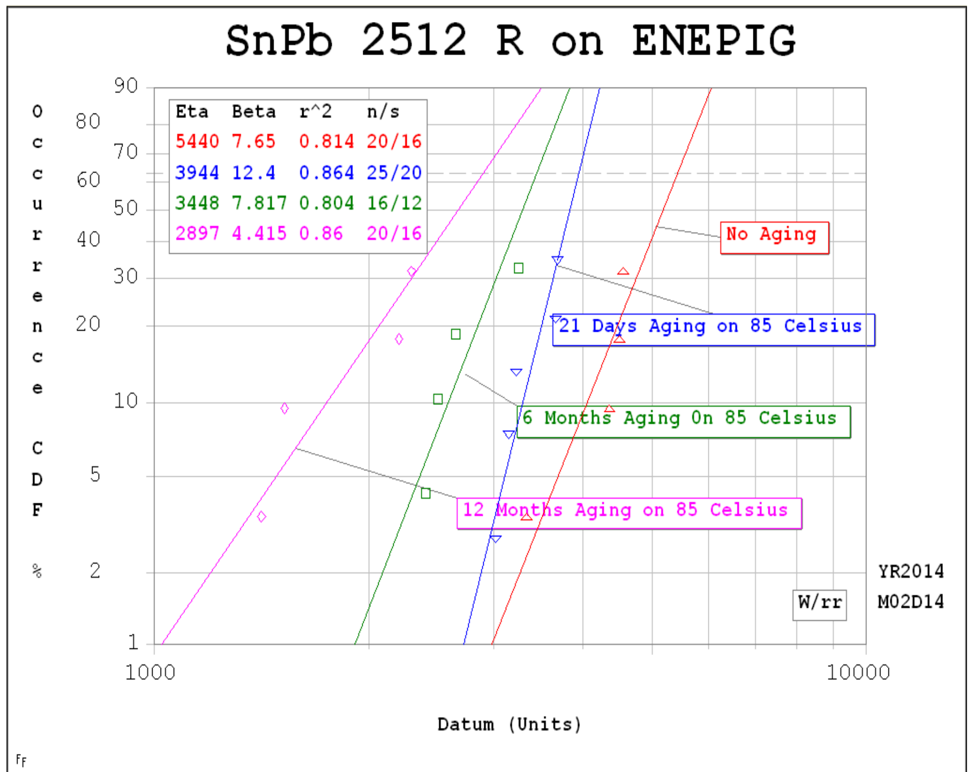
The Weibull plots in Figures. 5.4 and 5.5 show the thermal cycling results on isothermally aged ENIG and ENEPIG 15mm BGA samples (0.8mm ball pitch). For the Sn-37Pb case (Figure 5.4 (a), (b); Figure 5.5 (a), (b)), after 12 months of aging at 85°C and 125°C, the characteristic lifetime at both temperatures is reduced compared with no aging specimens. In contrast, the Sn-37Pb alloys have similar or greater lifetimes than as-assembled SAC, but also degrade considerably during aging. For example, Figure. 5.5 (a) showed that Sn-37Pb on ENIG has a characteristic lifetime of 1823 cycles after 12 months of aging at 125°C, which is 56.8% lower than the lifetime (4228 cycles) of no aging specimens. In Figure. 5.5 (c) and (e), the cycle lifetime of SAC105 and SAC305 is 33.1% and 31.3% lower than the lifetime (3684 and 3875 cycles) of no aging specimen, respectively. The results on ENEPIG have similar trends (Figure. 5.4 (d), (f); Figure. 5.5 (d), (f)).

5.2.3 2512 Resistors

The 2512 resistor banks consisted of five resistors placed in series. When one resistor failed, the other four resistors became censored data points. Figure. 5.6 and Figure.5.7 shows Weibull plots for the thermal cycling results on isothermally aged paste 2512 resistor with Sn-37Pb and SAC305 solder paste samples on ENIG and ENEPIG finishes. A measurable degradation in reliability is observed for both resistors on both finishes at elevated aging temperatures.



(a)



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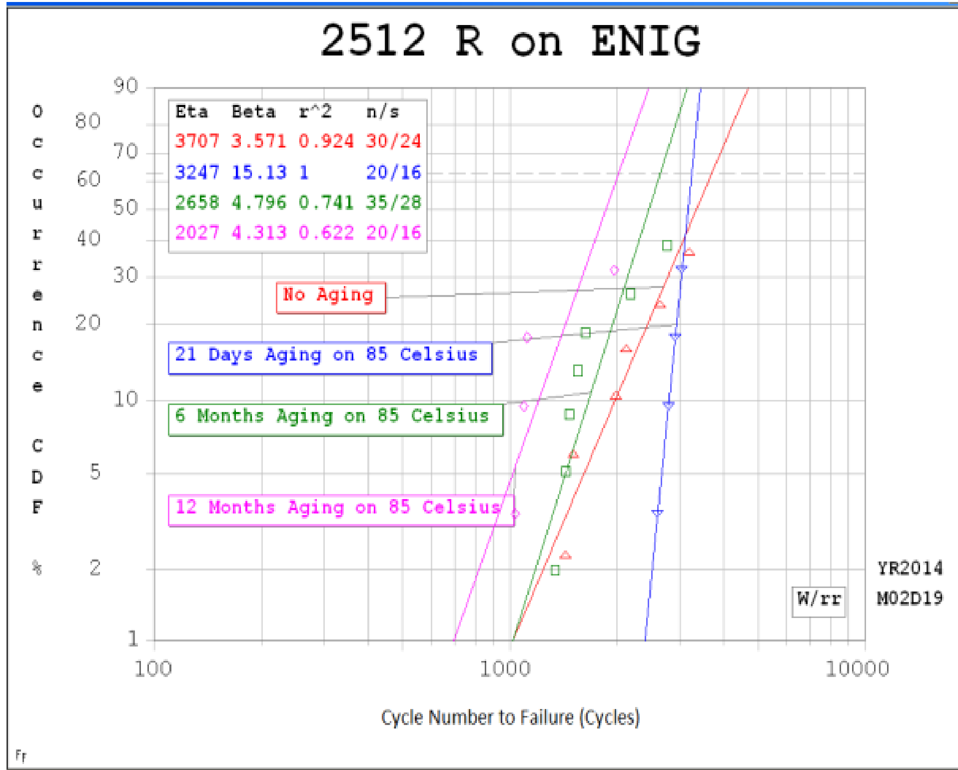

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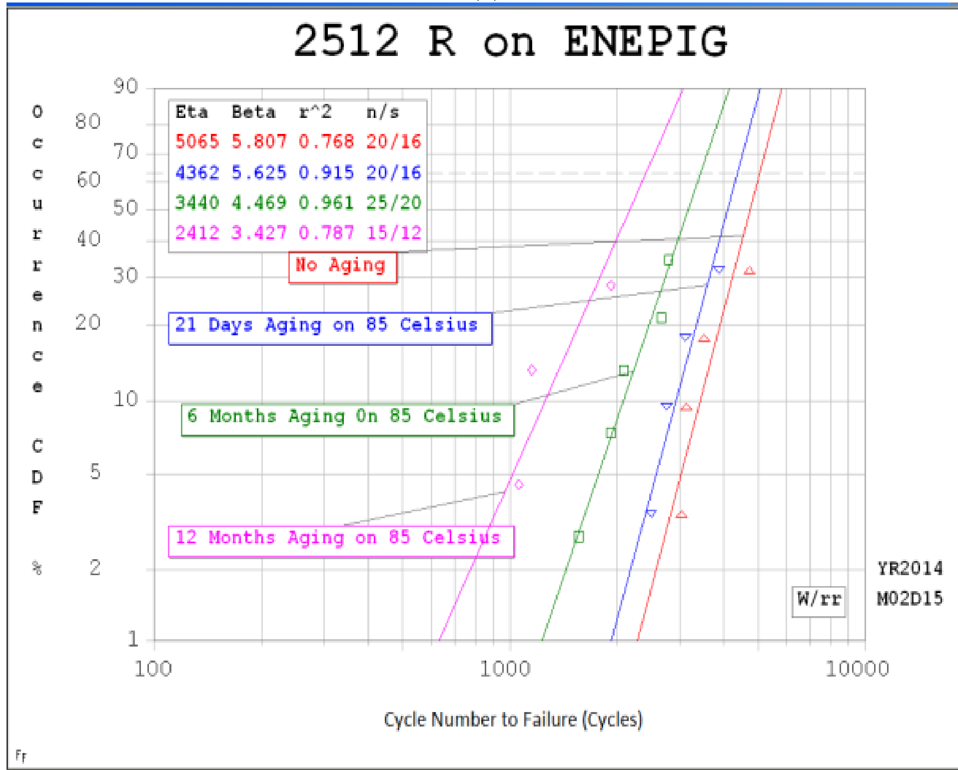
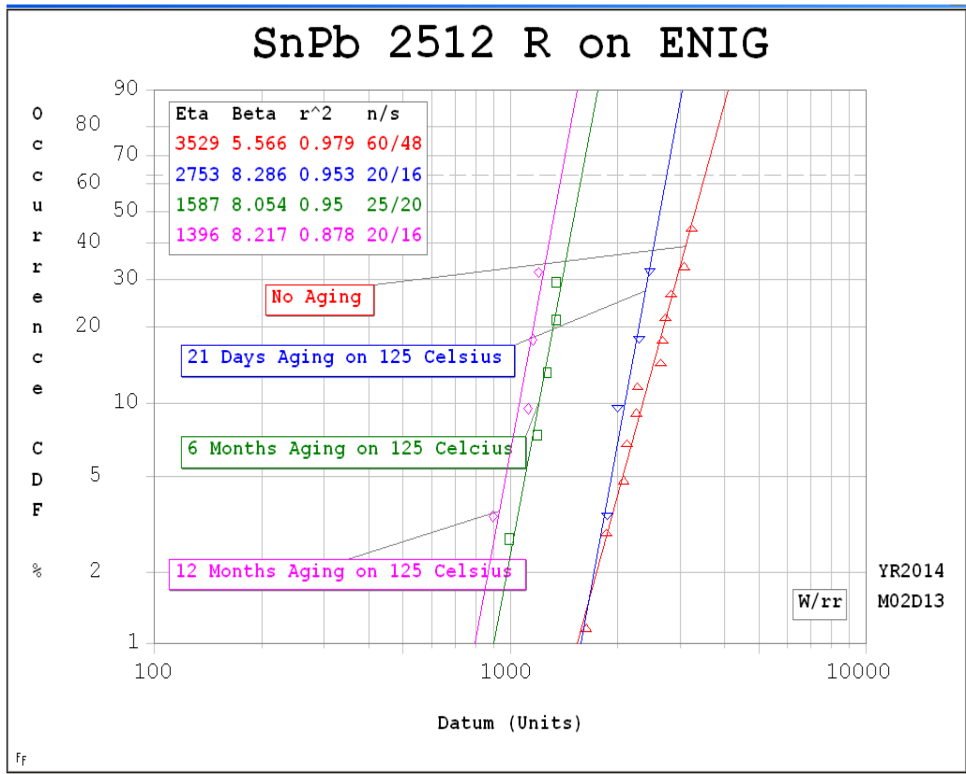
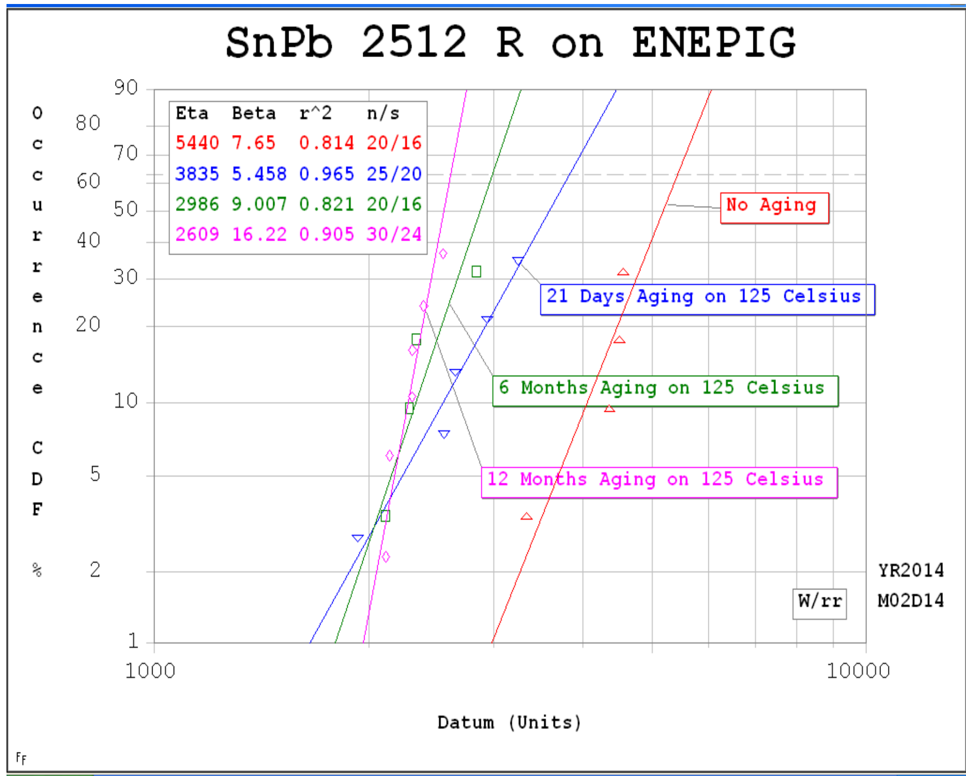


(d)

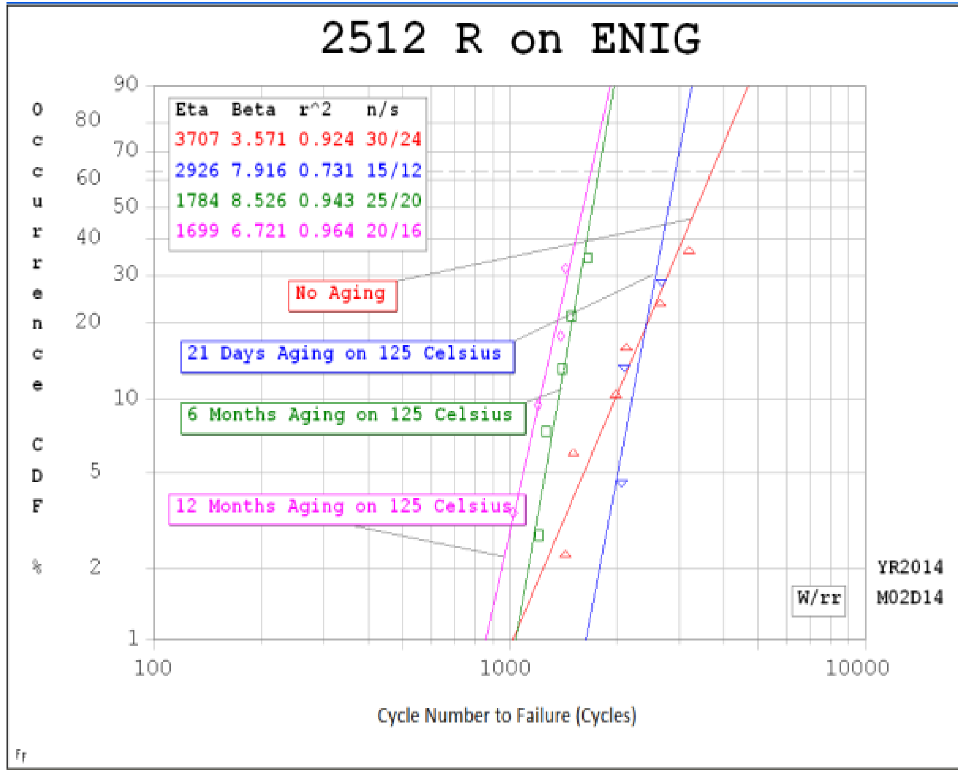
Figure 5.6 Weibull plost for SAC305 soldered 2512 resistor package subjected to 85°C aging: SnPb solder on ENIG (a), SnPb solder on ENEPIG (b), SAC305 solder on ENIG (c), SAC305 solder on ENEPIG (d).



(a)



(b)



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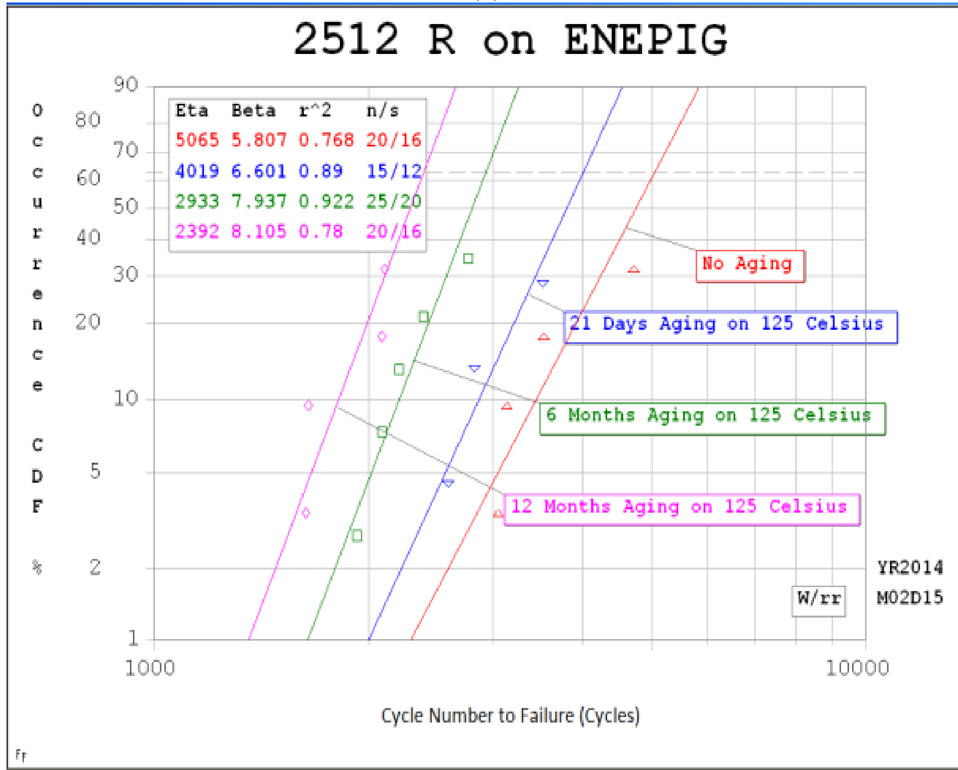


(d)

Figure 5.7 Weibull plost for SAC305 soldered 2512 resistor package subjected to 125°C aging: SnPb solder on ENIG (a), SnPb solder on ENEPIG (b), SAC305 solder on ENIG (c), SAC305 solder on ENEPIG (d).

In Figures. 5.6 and 5.7, the characteristic life reduction of 2512 resistors on ENIG and ENEPIG is shown. After aging, there is a significant drop in reliability for packages on ENIG and ENEPIG at both 85°C and 125°C aging, respectively. The two types of solder pastes performed similarly after 85°C aging for both finishes. At 125°C aging, SAC has a slightly lower reduction rate than Sn-37Pb solder on ENIG.

Table 5.1 Reliability Degradation Rate Summary

10mm BGA Package	12 Months Aging Degradation Rate		15mm BGA Package	12 Months Aging Degradation Rate		2512 Resistor	12 Months Aging Degradation Rate	
	85°C	125°C		85°C	125°C		85°C	125°C
Sn-37Pb on ENIG	18.7%	33.0%	Sn-37Pb on ENIG	26.2%	56.8%	Sn-37Pb on ENIG	47.2%	60.4%
SAC105 on ENIG	24.9%	40.9%	SAC105 on ENIG	28.3%	33.1%	SAC305 on ENIG	45.3%	54.2%
SAC305 on ENIG	23.7%	32.8%	SAC305 on ENIG	27.7%	31.3%	Sn-37Pb on ENEPIG	46.7%	52.0%
Sn-37Pb on ENEPIG	18.7%	23.9%	Sn-37Pb on ENEPIG	29.0%	50.5%	SAC305 on ENEPIG	52.4%	52.8%
SAC105 on ENEPIG	36.4%	41.7%	SAC105 on ENEPIG	X	X			
SAC305 on ENEPIG	37.9%	45.6%	SAC305 on ENEPIG	30.3%	43.9%			

Table 5.1 summarizes the Weibull reliability performance of the three alloys. It is clear that longer aging times and higher aging temperatures have a dramatic impact on solder interconnection reliability. SAC105 and SAC305 generally outperform Sn-37Pb solder in reliability under thermal fatigue. However, for 10mm BGA, when packages subject to aging, the SAC solder degraded worse than Sn-37Pb solder with only one exception (SAC 305/ENIG at 125°C). This finding indicated SAC solder alloy is more sensitive with thermal loading for finer pitch package (0.4mm ball pitch). Compare with BGA packages, resistor generally degrade worse subjected to isothermal aging. Another observation from Table 5.1 is that SAC alloys on ENIG show higher reliability than SAC on ENEPIG.

5.3 Failure Analysis

5.3.1 Surface and Thin Film Analysis

To gain an understanding of the starting ENIG/ENEPIG board finishes and to enable later comparisons to board finishes and solder joint morphology after high temperature, long time duration aging, a series of surface and thin film analysis were performed in order to guide our SEM/EDX analysis, showing the thicknesses of board finish layers expected during failure analysis.

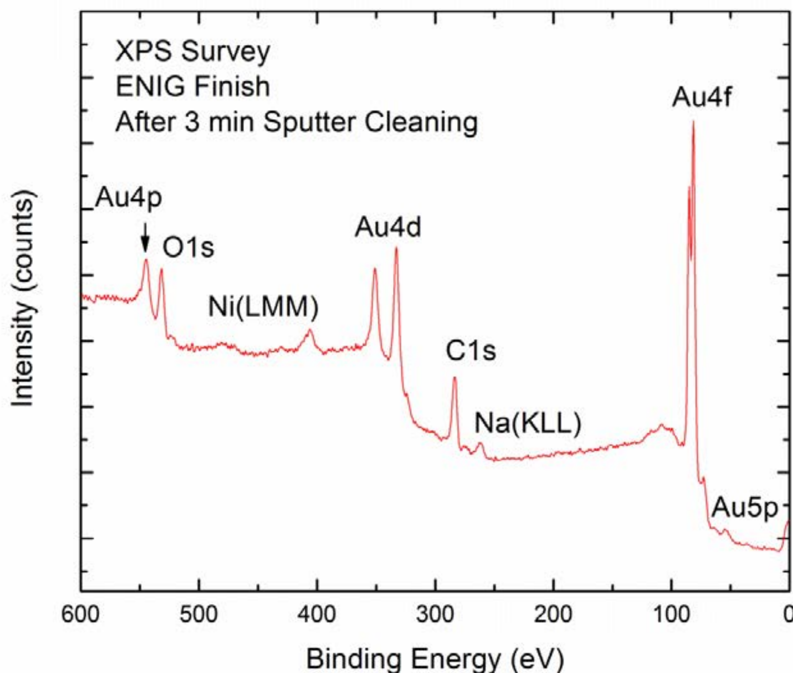


Figure 5.8 X-ray Photoelectron Spectroscopy (XPS) surface analysis on No aging ENIG board.

Figure 5.8 demonstrate one surface analysis (XPS) on a as received ENIG board. At a sputter rate of 25Å/min, three minutes of sputtering "drills" 75 Å under the "as received" surface. At this depth, the board finish remains mostly C. By comparison, for most "clean" metal surfaces (such as purchased from a metal supplier), the C would have been cleaned away at this depth. Similar results hold for the ENEPIG finish.

It is important to provide accurate baseline thicknesses of the Au, Ni, Pd layers in the

starting, “as supplied” ENIG/ENEPIG structures, for later comparison after high temperature, long time duration aging. The starting finish layers were evaluated nondestructively by Rutherford backscattering spectroscopy (RBS). RBS allows for quantitative analysis of layered structures, both in stoichiometry and thickness. The results are given in Figure 5.9.

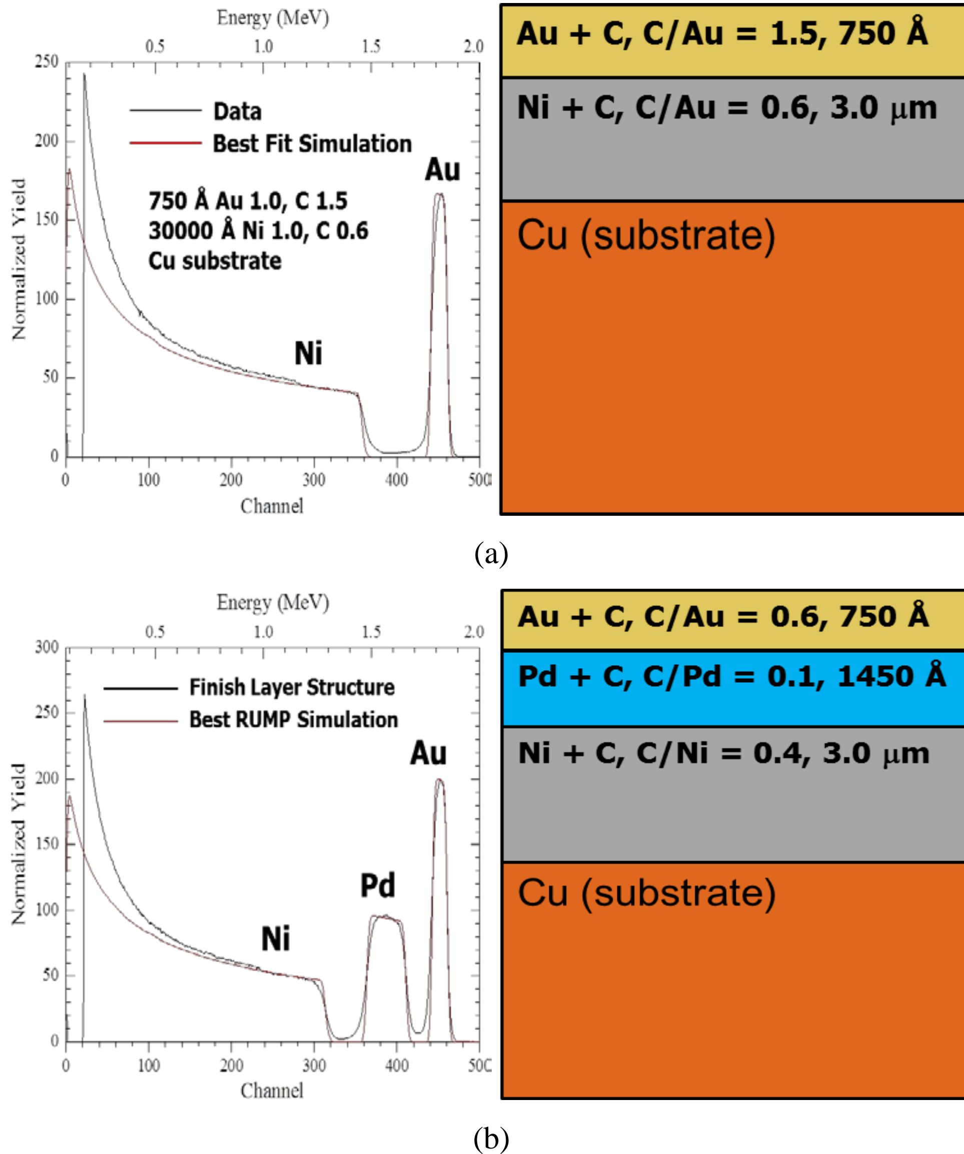
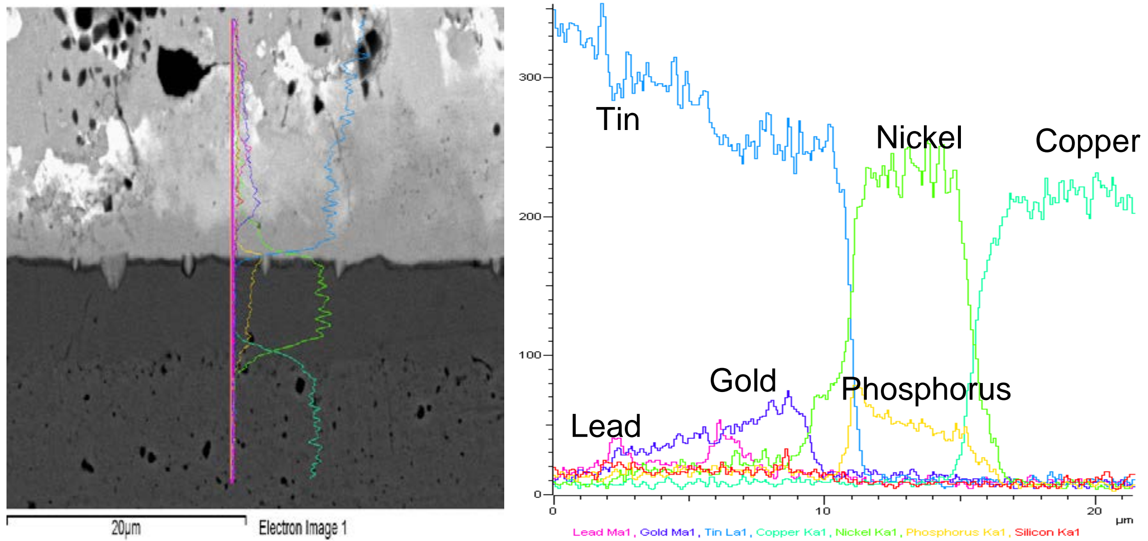


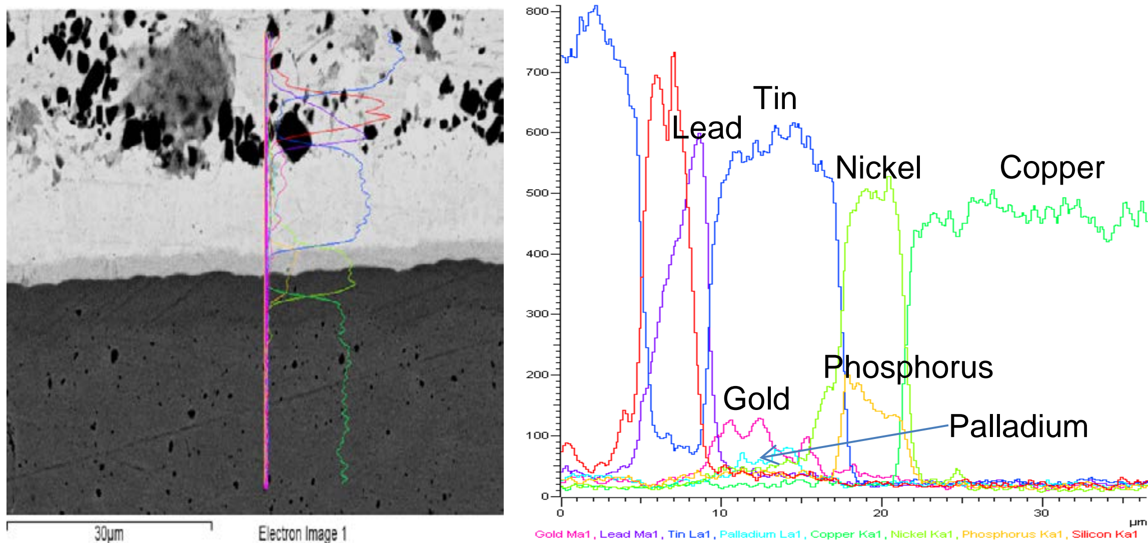
Figure 5.9 RBS spectra for the starting ENIG (a) and ENEPIG (b) board finishes

In Figure 5.9, the best RBS simulation for the ENIG finish board is 750 Å Au/3.0 μm Ni and for ENEPIG is 750 Å Au/1450 Å Pd/3.0 μm Ni. The results verified that the film thicknesses were within the range expected/quoted by suppliers. The RBS spectra shows that the starting

board finish layers are relatively sharp, although a slight “rounding” of the leading and trailing edges of the RBS peaks for the Au and Ni layers (compared to simulation) indicates interfacial roughness and/or slight inter-diffusion between the layers. These film thicknesses are within the range expected/quoted by suppliers of ENIG/ENEPIG. In addition, the starting board finish layer structure is relatively sharp, with little evidence for inter-diffusion between the layers.



(a)



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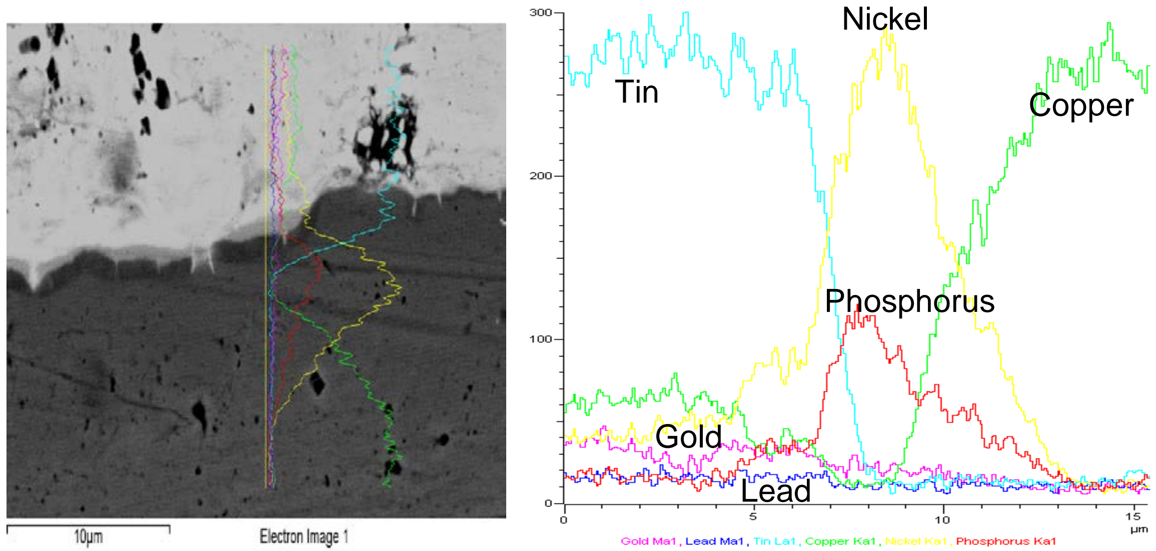

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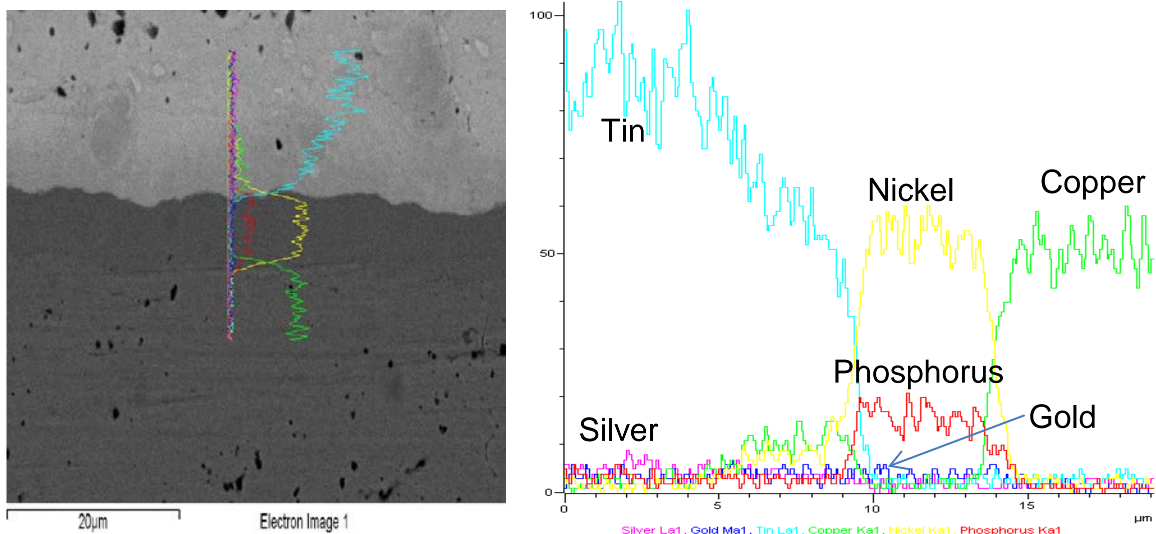


(d)

Figure 5.10 Board-side EDX elemental line scan for (a) Sn-37Pb on ENIG; (b) Sn-37Pb on ENEPIG; (c) SAC305 on ENIG; (d) SAC305 on ENEPIG after 6 months/125°C aging. The dark inclusions in the BSE images are due to imbedded polishing compound and can be ignored.

Figure. 5.10 show EDX line scans of board side Sn-37Pb and SAC305 solder on "as received" ENIG and ENEPIG finishes. All SEM images are generated in backscattered (BSE) mode, which allows for image contrast due to atomic number differences – heavier elements in the photograph "image" bright and light elements "image" dark, which is easily verified when

doing EDX line scans/maps. Example: Bright ("white") parts of the photograph are regions having high Pb concentration, shown by the line scan through the Pb-rich phase in the Sn-37Pb. Three quick observations are: 1) Au buildup at the Sn-Ni interface as was the case for Sn-37Pb; 2) the P buildup at the solder side of the Ni layer. 3) the P is distributed throughout the Ni layer and there is no evidence of Au rebuilding at the SAC-Ni interface.

A variety of failed solder joints was examined by SEM/EDX to determine how the open circuit failures occurred. EDX elemental maps for Sn-37Pb and SAC305 on ENIG and ENEPIG board side interfaces, after 6 months of aging (Fig. 5.11).

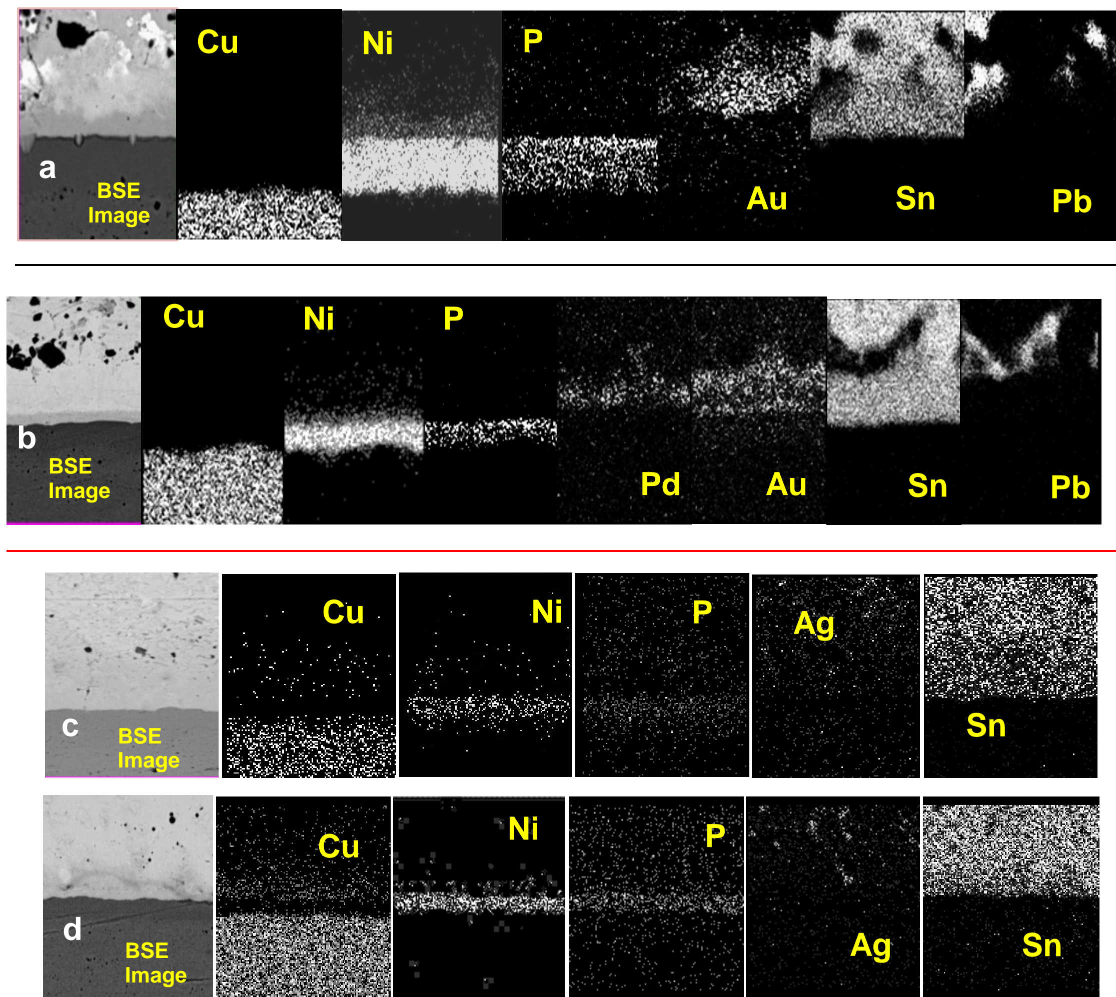


Figure 5.11 Board-side EDX elemental maps for (a) Sn-37Pb on ENIG; (b) Sn-37Pb on ENEPIG; (c) SAC305 on ENIG; (d) SAC305 on ENEPIG after 6 months/125°C aging. The dark inclusions in the BSE images are due to imbedded polishing compound.

The Ni layer functioned as an effective diffusion barrier in both finishes, as the Cu remains largely in the substrate and PCB interfacial layer. However, the Au which dissolves into the solder alloy during reflow "reforms" adjacent to Sn-Ni interface for both finishes after 6 months, which is consist with Erinc's observations on SAC alloys [78] and also observed during aging of Sn-37Pb alloys on ENIG [61]. The Au redistribution is of concern in solder reliability due to the development of a continuous interfacial $(Au,Ni)Sn_4$ over time, which adds to the IMC content at the interface and leads to brittle failure. The EDX maps for Sn-37Pb show that Pd in the ENEPIG finish also has begun to segregate to the solder side of the interface.

5.3.2 IMC Analysis and Crack Propagation

A second factor which strongly influences fatigue solder failures is the continuous growth of interfacial intermetallics during isothermal aging. When the intermetallic layer thickens, it consumes the substrate and can cause joint dewetting [63] [79]. Further, as the solder and IMC interconnection region encounter localized high strain due to CTE mismatches, the brittle intermetallic becomes a significant fraction of the solder joint and becomes a ready location for crack initiation and propagation when the joint is mechanically stressed. Figure. 5.12 and Table 5.2 illustrate the IMC thickness growth at the board side interface for both finishes.

Three thickness measurements were averaged along the intermetallic layer for three solder balls located at a left corner, center, and right corner line under a package. Studies by Yoon, et al. show that the IMC in SAC/ENIG/ENEPIG systems is the ternary compound $(Cu,Ni)_6Sn_5$ or second phase IMC $(Ni,Cu)_3Sn_4$ [80].

The data shows that ENIG has a greater average IMC thickness during short term aging than ENEPIG, which may be due to the absence of Pd in ENIG, presuming Pd provides an additional barrier to Cu diffusion. Eventually, as shown in Table III, the board side IMC for both finishes approaches a similar thickness; however, the fact that both ENIG and ENEPIG IMC thicknesses are increasing vs. aging time offer a partial explanation for the degraded reliability performance of SAC alloys on ENIG/ENEPIG over time and temperature.

Table 5.2 SAC305 Board Side IMC Growth during 125°C Aging

ENIG Plating PCB side IMC

ENEPIG Plating PCB side IMC

0.8mm pitch SAC305 BGA	No Aging (µm)	21 days 125°C Aging (µm)	6 month 125°C Aging (µm)	12 month 125°C Aging (µm)
ENIG	2.37	3.11	3.89	5.99
ENEPIG	1.55	1.77	4.43	5.70

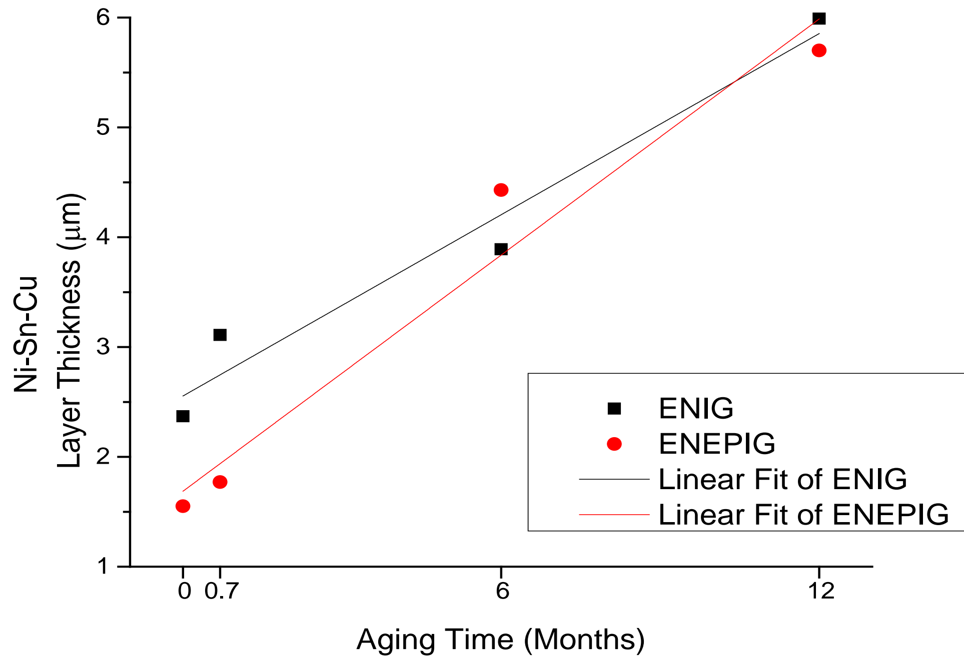


Figure 5.12 Board-side SAC305 IMC Thickness Growth on ENIG and ENEPIG

Large plate-like Ag_3Sn phases can be found regularly in SAC305 solder joints subject to isothermal aging alone, which is due to its higher Ag content (Figure. 5.13). During solid state diffusion, the Ag_3Sn particles coarsen and block the crack paths, which in turn increase the joint structural stability [69] [81].

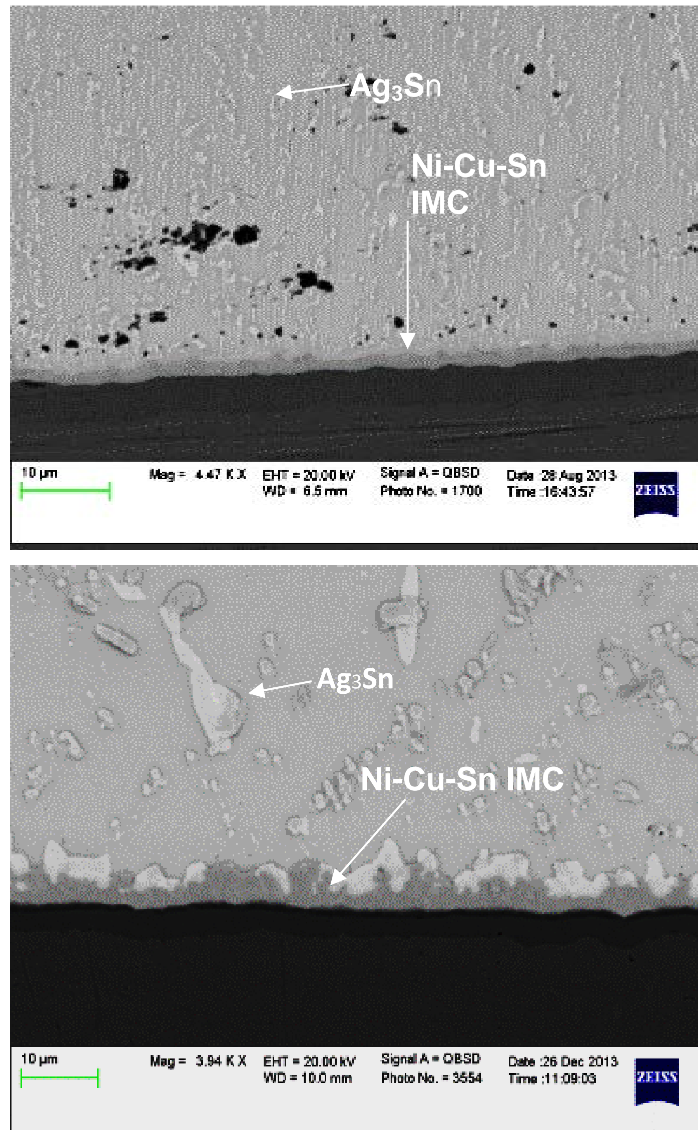


Figure 5.13 SAC305 (0.8mm pitch) solder joint on ENEPIG before thermal cycling: No aging (Top) and 12 months/125°C aging (Bottom). BSE imaging.

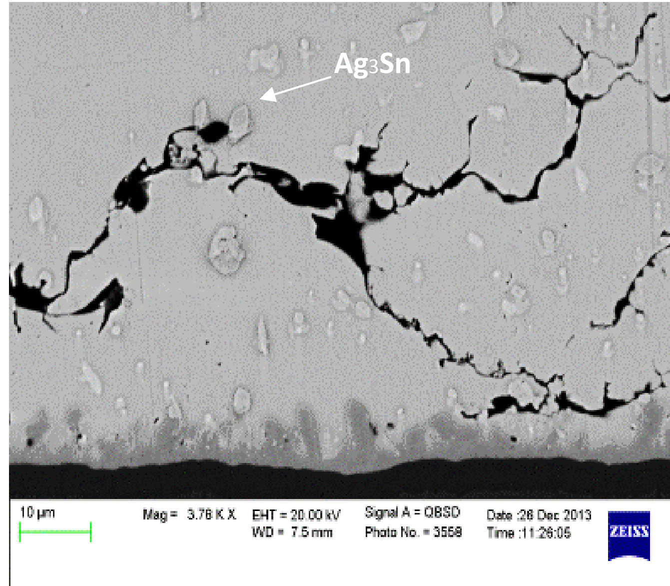


Figure 5.14 SAC305 (0.4mm pitch) solder joint on ENEPIG after 12 months/125°C aging and thermal cycling. BSE imaging.

In Figure. 9, one can clearly observe that coarsened Ag_3Sn IMC reduces/redirects the crack growth which results in enhanced joint structural strength. This helps to explain the superiority of high Ag content material to resist thermal fatigue. The shear stress created from the CTE mismatch at the both component and board-side solder/finish interface cause plastic deformation, which generates cracks and site at those areas.

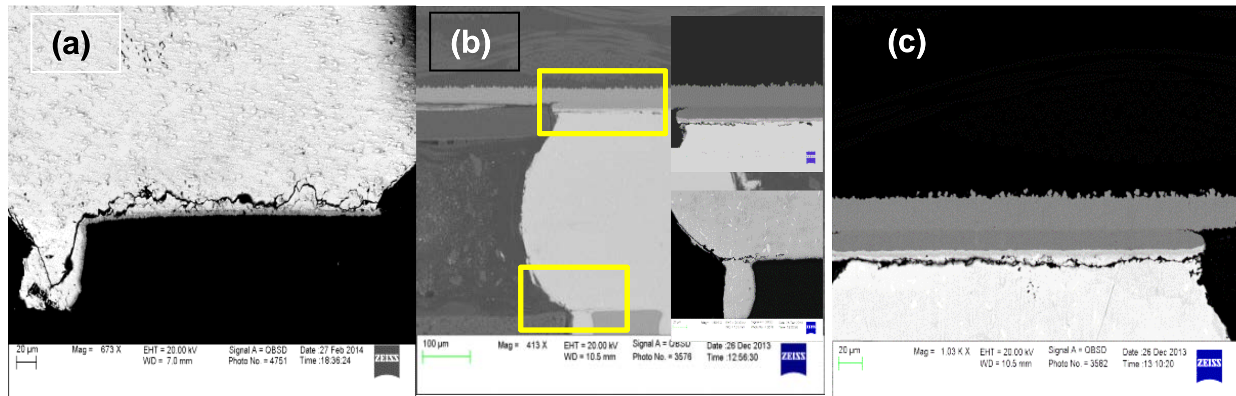


Figure 5.15 Representative crack propagation (BSE imaging) for SAC105 (0.8mm ball pitch) after 12 months/125°C aging on (a) ENIG, (b) and (c) ENEPIG

Figure. 5.15 show typical crack propagations for 0.8mm pitch solder joints after thermal aging and cycling for SAC 105 on ENIG and ENEPIG surface finishes. Cracks initially start from the corner of the interconnection and then proceed along the package/board interface and

often into the solder bulk. This failure mode has been observed in previous work and can be explained by fast deformation rates, where the stress concentrates at the corner regions of the interconnections and the fracture strength of the IMC reaction zone is eventually exceeded [64].

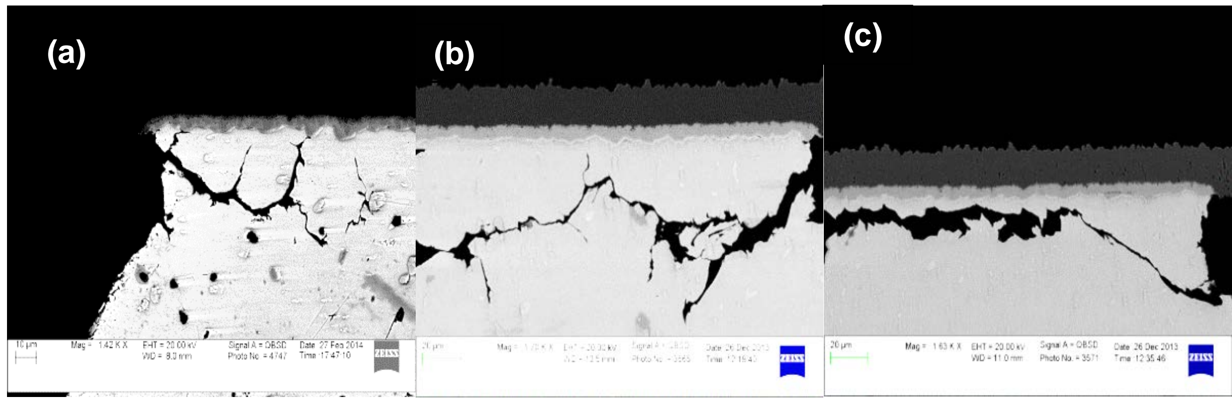


Figure 5.16 Representative crack propagation (BSE imaging) for SAC105 (0.4mm ball pitch) after 12 months/125°C aging on (a) ENIG, (b) and (c) ENEPIG.

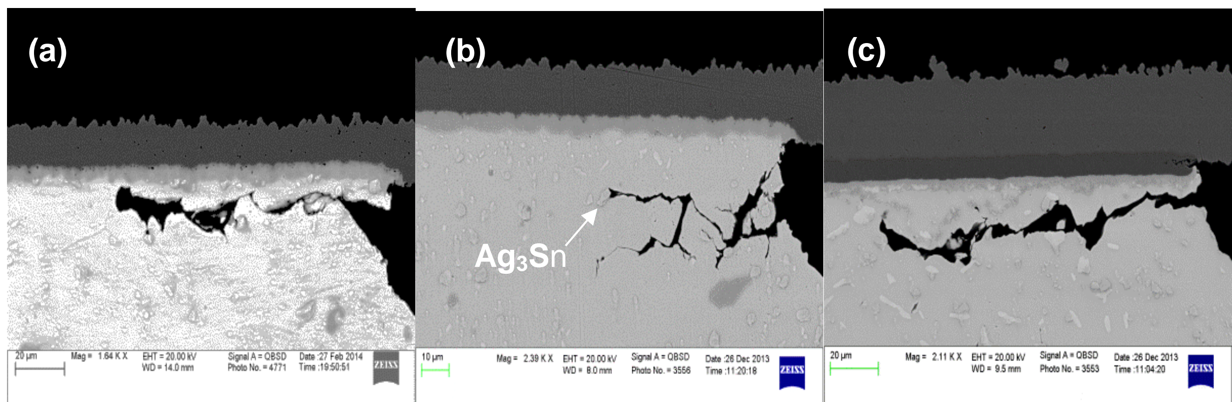


Figure 5.17 Representative crack propagation (BSE imaging) for SAC305 (0.4mm ball pitch) after 12 months/125°C aging on (a) ENIG; (b) and (c) ENEPIG.

For finer pitch solder interconnections (0.4mm), the microstructure deformation was more severe. Cracks were often found to propagate entirely through the bulk solder (Figure 5.16-5.17). The reason for the change in failure has to do with the thermal-mechanical stresses and the subsequent microstructural evolution produced during cycling. Finer pitch packages typically have less structural stability then larger pitch packages due to increased grain structure movement along the interfacial region for finer packages. The local CTE mismatch between adjoining grains rotates/slides and enlarges each grain during thermal cycling. The newly formed,

recrystallized networks of grain boundaries provide favorable sites for cracks to propagate [82], [49]. In addition, the subsequent grain boundary decrease begins to create micro-cracks within the recrystallized region. When the grain structure has been heavily deformed, the linkage of the micro-cracks generates a large crack which propagates along grain boundaries and eventually causes the electrical open of a component [45].

5.4 Discussion and conclusion

Long-term thermal aging results in significant reliability degradation for Sn-37Pb, SAC105, and SAC305 solder alloys on ENIG and ENEPIG. The reduction of reliability is observed throughout the aging period. There was ~ 25% reduction in characteristic lifetime for SAC105 and SAC305 on ENIG during 12 month/85°C aging and ~ 35% degradation on ENEPIG. After 12 months/125°C aging, the package lifetime decreased ~ 40% for SAC105 and SAC305. The reliability performance between those two board plating is not severe for most BGA packages. This finding is consistent with the result in TV-7 phase 1. Sn-37Pb solder outperformed the SAC alloys over long-term aging in deterioration rate. The performance of SAC105 is closing to SnPb solder material after aging at 125°C.

Failure analysis showed dramatic intermetallic Ni-Cu-Sn growth at the board-side solder joint interfaces. The root cause of the bottom side IMC changes is the diffusion of Ni, Cu or Au for some cases from bottom trace. However, there is no clear evidence shown that ENIG and ENEPIG has significant different diffusion rate. After 125°C aging, the cracks appeared at the lower corners at the board side interface and propagated near the Ni-Cu-Sn IMC region. Different new failure modes were discovered for fine-pitch packages. In that case, cracks not only propagate along the IMC region at both sides of the joint but proceed into the bulk solder. Ag-Sn IMC coarsening effectively pins the crack growth path for higher Ag content alloys such as SAC305.

Chapter 6

TV-7 Plating Comparison Analysis

6.1 Introduction

Pb-free solder joints exposed to elevated isothermal temperatures for prolonged periods of time undergo microstructural and mechanical evolution which degrades the joint electrical performance. We report the effect of isothermal aging on the reliability of Sn-Ag-Cu (SAC) assemblies on three different surface finishes (immersion Ag (ImAg), electroless Ni/immersion Au (ENIG) and electroless Ni/electroless Pd/immersion Au (ENEPIG)). This chapter presents information on the interaction between different types of packages with three board finishes tested in a 12-month isothermal aging period.

6.2 Reliability Data Analysis

Table 6.1 summarizes the characteristic life (η from Weibull plot) and provides a comparison between packages.

Table 6.1 12-months aging characteristic lifetime

		Characteristic Life η (cycles)								
		No Aging			6 Months			12 Months		
		ImAg	ENIG	ENEPIG	ImAg	ENIG	ENEPIG	ImAg	ENIG	ENEPIG
85°C	15mm SAC105	2926	3684	3329	1656	3186	2559	1569	2643	X
	15mm SAC305	3743	3875	3595	2241	3234	2728	2107	2803	2507
	10mm SAC105	2419	3422	3536	1596	3026	2460	1439	2571	2249
	10mm SAC305	3329	3974	4661	2012	3339	3337	1874	3034	2893
	2512 Resistor	3313	3707	5065	3011	2658	3440	2761	2027	2412
125°C	15mm SAC105	2926	3684	3329	1429	2895	2062	1325	2463	X
	15mm SAC305	3743	3875	3595	2083	3049	2253	1884	2663	2018
	10mm SAC105	2419	3422	3536	1116	2284	2179	1079	2022	2061
	10mm SAC305	3329	3974	4661	1740	2894	2635	1551	2671	2536
	2512 Resistor	3313	3707	5065	2530	1784	2933	2383	1699	2392

In general, Pb-free solder with ENIG and ENEPIG outperform ImAg under identical test conditions; in addition, SAC305 solder alloy performs better than SAC105 in all test groups,

which compares favorably with previous studies. The characteristic life for no aging 10mm SAC105 solder on ImAg, ENIG, and ENEPIG were 2419, 3422, and 3536 cycles, respectively. After aging at 85°C/12 months, the cycle life dropped to 1439, 2571, and 2249 and further reduced to 1079, 2022, and 2061 cycles after 125°C aging/12 months, respectively.

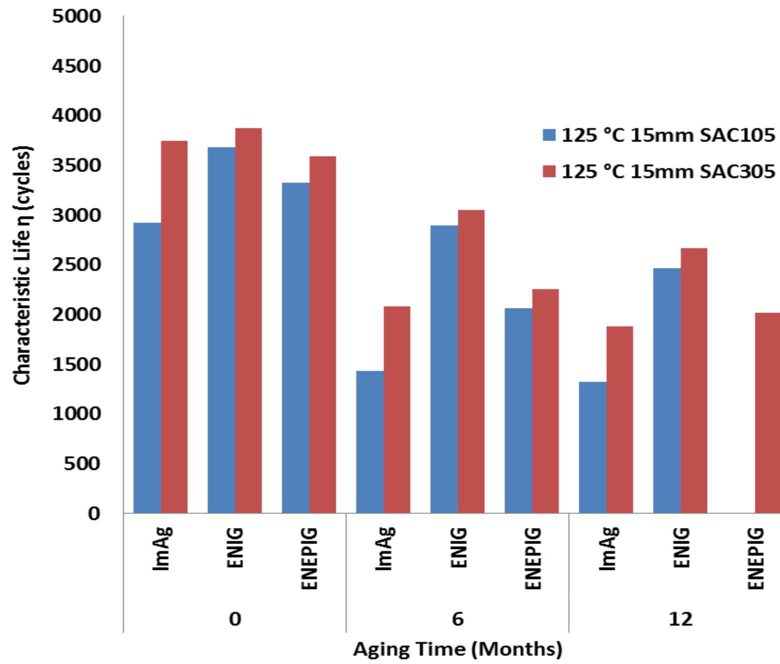


Figure 6.1 Characteristic lives for 15mm BGA subject to 125°C/12 months aging.

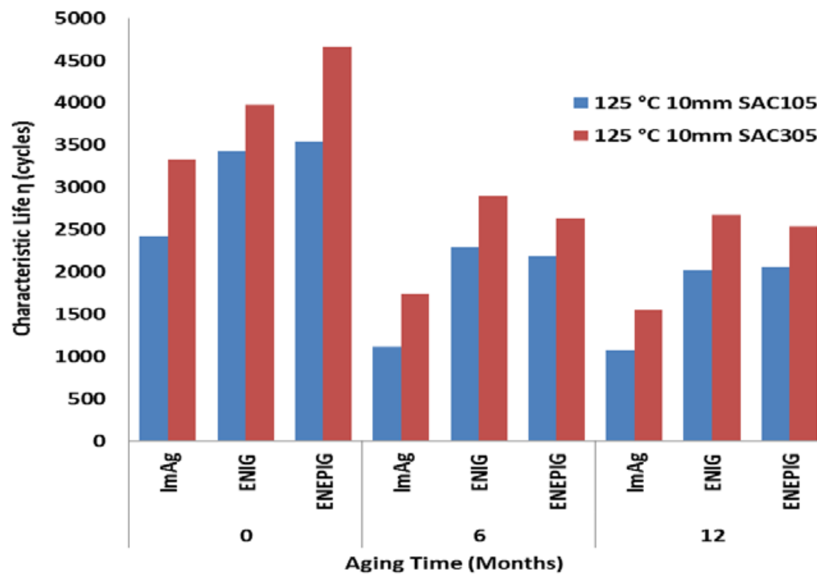


Figure 6.2 Characteristic life for 10mm BGA subject to 125°C/12 months aging.

Figure 6.1 and Figure 6.2 showed the difference in reliability performance between SAC105 and SAC305 for the 15mm package (0.8mm pitch) package and 10mm (0.4mm pitch) at 125°C aging. Both ENIG and ENEPIG outperform ImAg for 10mm SAC solder alloys before or after high temperature aging, but ENIG compared to ENEPIG had similar performance, with only one exception (no aged SAC305 on ENEPIG). However, for the 15mm package, the characteristic life was consistently in the order ENIG > ENEPIG > ImAg.

Table 6.2 12-month aging characteristic life degradation rate

		12-Month Aging Degradation Rate		
		ImAg	ENIG	ENEPIG
85℃	15mm SAC105	46.4%	28.3%	X*
	15mm SAC305	43.7%	27.7%	30.3%
	10mm SAC105	40.5%	24.9%	36.4%
	10mm SAC305	43.7%	23.7%	37.9%
	2512 Resistor	16.7%	45.3%	52.4%
125℃	15mm SAC105	54.7%	33.1%	X*
	15mm SAC305	49.7%	31.3%	43.9%
	10mm SAC105	55.4%	40.9%	41.7%
	10mm SAC305	53.4%	32.8%	45.6%
	2512 Resistor	28.1%	54.2%	52.8%

*Indicates no data point was available

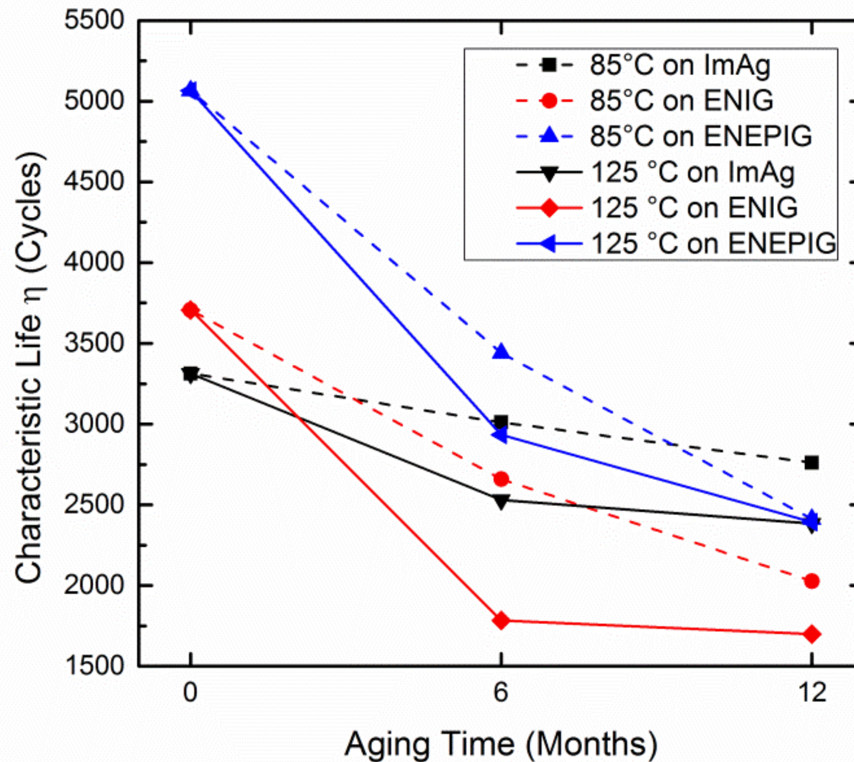


Figure 6.3 Characteristic life for 2512 resistors vs. aging time for three surface finishes.

Figure 6.3 showed the characteristic life reduction of 2512 resistors on ImAg, ENIG, and ENEPIG. After aging, there is a significant drop in reliability for packages on ENIG and ENEPIG at both 85°C and 125°C aging, indicated by dashed and solid lines, respectively. The resistors on ImAg degrade at a slower rate than the other two finishes under both 85°C and 125°C aging. Table 6.2 summarizes the degradation rate for all packages on three board finishes after 12 months of aging. For SAC alloy BGA packages, ImAg has the greatest reduction in reliability performance whereas the SAC/ENIG degraded least. For the 2512 resistor package, however, SAC/ImAg degraded less than other two finishes with thermal aging treatment.

6.3 Failure Analysis

The effect of isothermal aging and thermal cycling was studied by SEM/EDX techniques to determine how the open circuit failures occurred. The morphology of microstructure change is characterized by selected cross-sectioned samples.

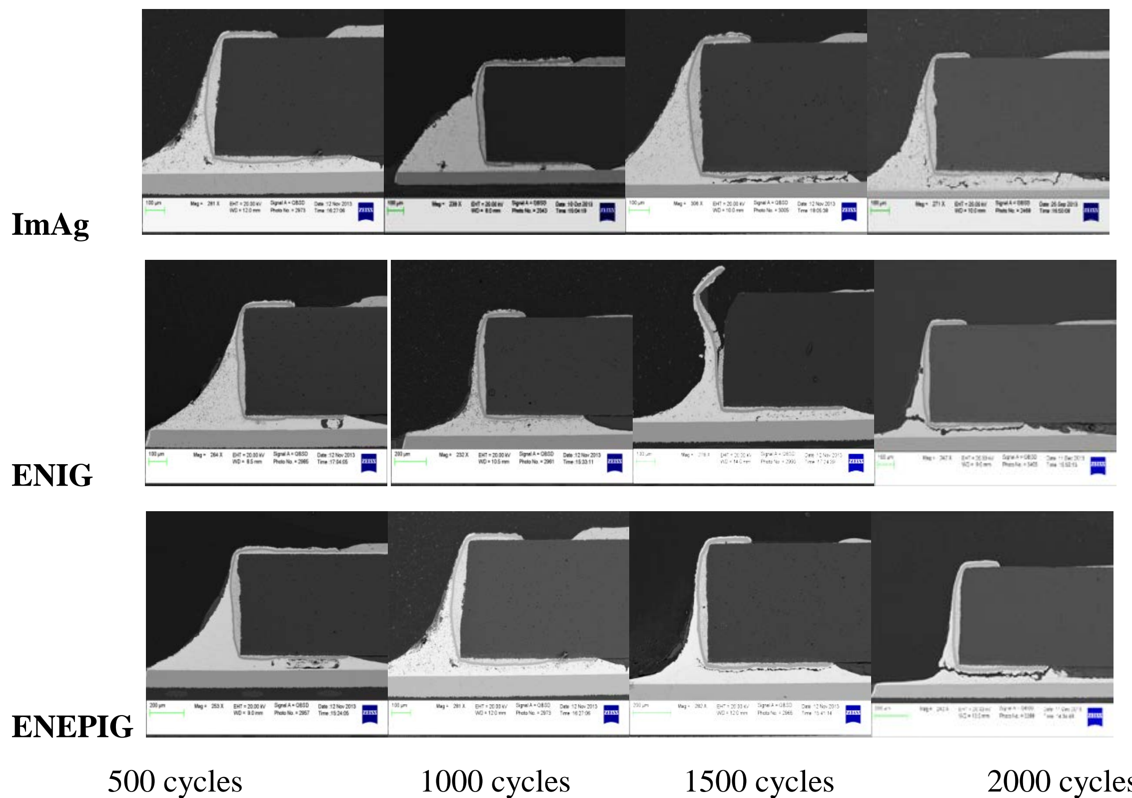


Figure 6.4 Observed cracks in chip resistor joints as a function of thermal cycles.

We expected extensive cracking in the 2512 resistors due to the high effective stiffness and large CTE mismatch with the resistor substrate which would result in larger thermal stresses during heating [36]. Figure. 8 shows representative SEM cross-sections vs. cycling time for SAC305, 2512 resistors aged at 125°C/12 months on three board finishes. Resistor cross sections showed that cracks initiated at the ends of the solder joints beneath the resistor or in the upper parts of the solder fillets, which appear to originate in the early stages of the fatigue life. After continuous cycling, the cracks then extended through the solder joint, usually along the periphery of the resistor lead to terminate as an electrical open. This finding was also reported by Qi, et al. [38] who used finite-element modeling to predict resistor package failures in Pb-free alloys, and showed that crack initiation locations correspond to maximum strain and stress locations in the chip resistor package.

The growing interfacial IMC during thermal aging strongly influences fatigue solder failures. For ImAg, a first layer Cu_6Sn_5 intermetallic is formed at the PCB/solder joint interface followed by a second layer of Cu_3Sn formed during aging. As the solder and IMC

interconnection region encounter localized high strain due to CTE mismatches, the brittle intermetallic provide a potential site for crack initiation and propagation when the joint is mechanically stressed. For ENIG/ENEPIG, the IMC layer is of Cu-Sn type with a small proportion of nickel, usually reported as $(Ni,Cu)_6Sn_5$ and $(Ni,Cu)_3Sn_4$. The nickel layer acts as a diffusion barrier inhibiting formation of the Cu_3Sn layer. Phosphorus is also present due to the process deposition of the nickel layer [83].

Table 6.3 SAC305 board side IMC growth during 125°C aging.

0.8mm pitch BGA on different Plating	No Aging (µm)	6 month 125°C Aging (µm)	12 month 125°C Aging (µm)
SAC305 on ImAg	1.83	6.45	9.04
SAC305 on ENIG	2.37	3.89	5.99
SAC305 on ENEPIG	1.55	4.43	5.70

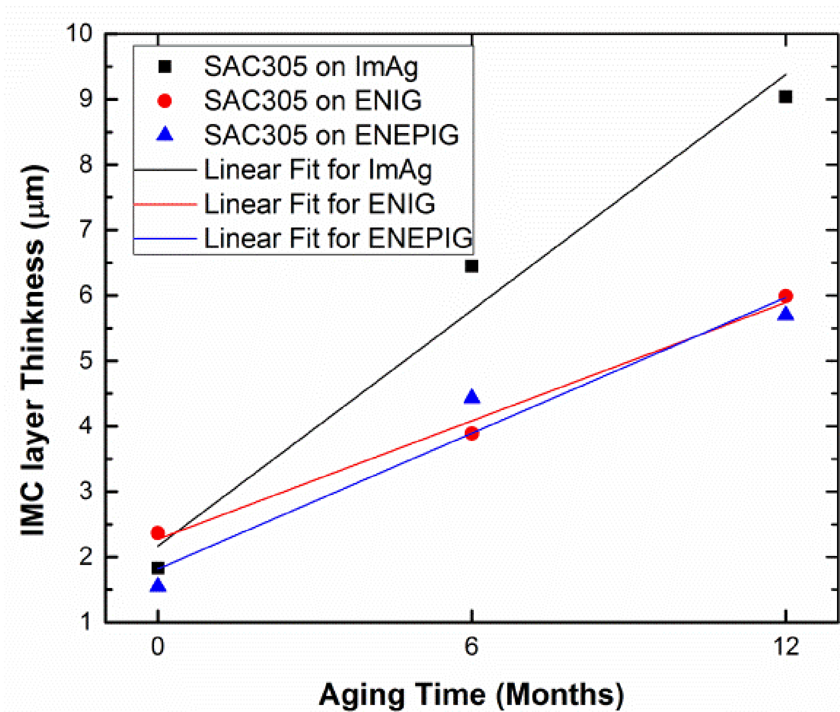
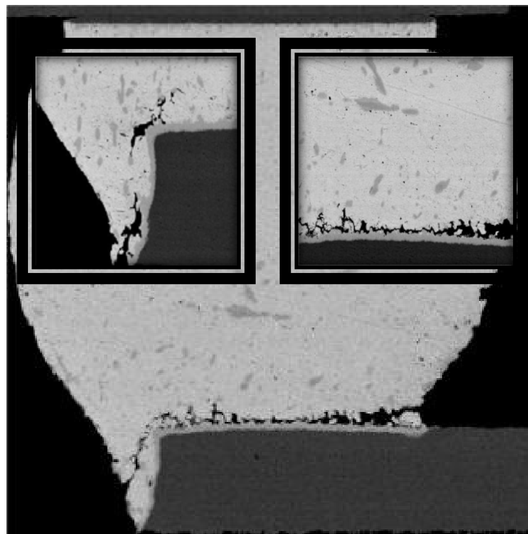


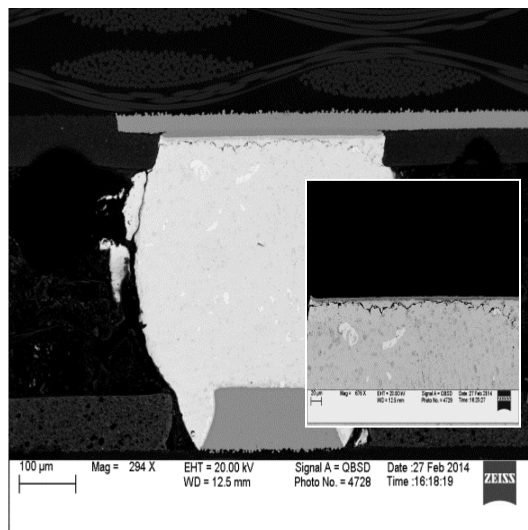
Figure 6.5 Board-side SAC305 IMC thickness on ImAg, ENIG, and ENEPIG.

Figure 6.5 and Table 6.3 illustrate the IMC thickness increase at the board side interface for ImAg, ENIG, and ENEPIG finishes. Three thickness measurements were averaged along the intermetallic layer for three solder balls located at a left corner, center, and right corner line

under a package. The data shows that ImAg has a greater average IMC thickness during thermal aging than ENIG/ENEPIG, which is probably due to the absence of Ni-P layer in ImAg, presuming Ni-P provides an additional barrier to Cu diffusion (in the case of the ENEPIG board, the Pd layer acts as a diffusion barrier to the interfacial growth of the IMC) [84]. That the board side IMC thicknesses for all finishes are increasing vs. aging time helps to explain the degraded reliability performance of SAC alloys on ImAg/ENIG/ENEPIG over time and temperature as the brittle interface assumes a larger fraction of the solder joint, precisely at the locations of high thermal stress in the joint.



(a)



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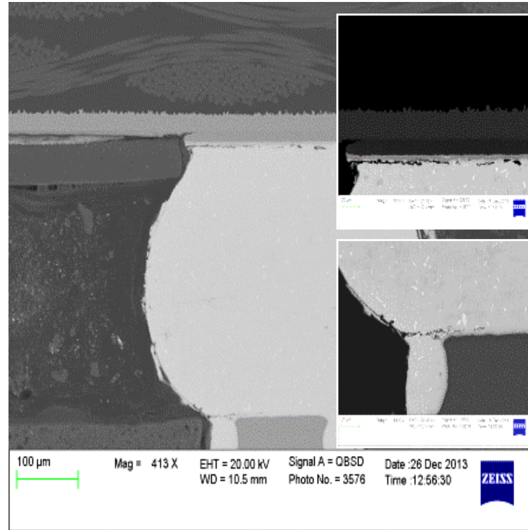
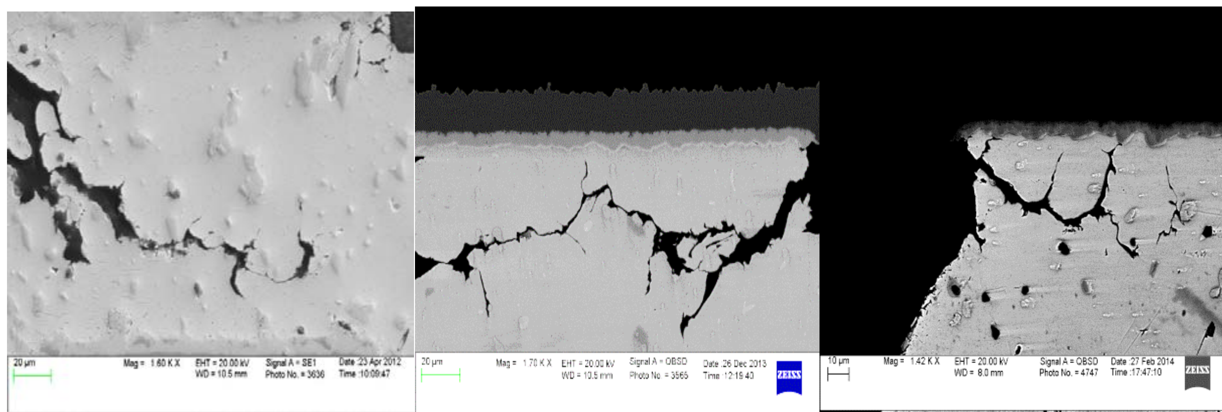


(c)

Figure 6.6 Representative crack propagation (BSE imaging) for SAC105 (0.8mm ball pitch) after 12 months/125°C aging on (a) ImAg, (b) ENIG, and (c) ENEPIG board finishes.

Figure 6.6 showed typical crack propagations for 0.8mm pitch solder joints after 125°C/12 months thermal aging and cycling for SAC 105 on ImAg, ENIG, and ENEPIG. The solder interconnections failed at both package and PCB sides of the joint, with cracks initially starting from the corner of the interconnection and proceeding along the package/board interface and often into the solder bulk.



(a) (b) (c)

Figure 6.7 Representative crack propagation (BSE imaging) for SAC105 (0.4mm ball pitch) after 12 months/125°C aging on (a) ImAg, (b) ENIG and (c) ENEPIG board finishes

The reason for this failure mode is that, under fast deformation rates, the flow stress of the solder increases and stresses concentrate at the corners of the interconnections where the fracture strength of the intermetallic reaction zone is exceeded. The recrystallization occurs first near the corner of the interconnections, where the structure is the most heavily deformed plastically [64].

For finer pitch solder interconnections (0.4mm) the microstructural deformation was more severe. Many joints showed a crack path starting near the alloy/package interface and then angling into the bulk solder rather than site along IMC interface after thermal aging at 125°C and cycling (Figure 6.7). This could be attributed to two factors. First, finer pitch packages generally have less structural stability than larger pitch packages, due to formation of a continuous network of high-angle (grain) boundaries by local recrystallization, typically at package joint region where the alloy microstructure undertaken higher stress than the IMC interface. There is heightened grain structure movement along the interfacial region, which encourages cracks to nucleate in and propagate through the recrystallized solder [64]. Second, the lower hardness and larger IMC precipitates as Ag_3Sn that cannot pining sites at the grain boundary and making it easier for the crack to propagate in the aged samples [85].

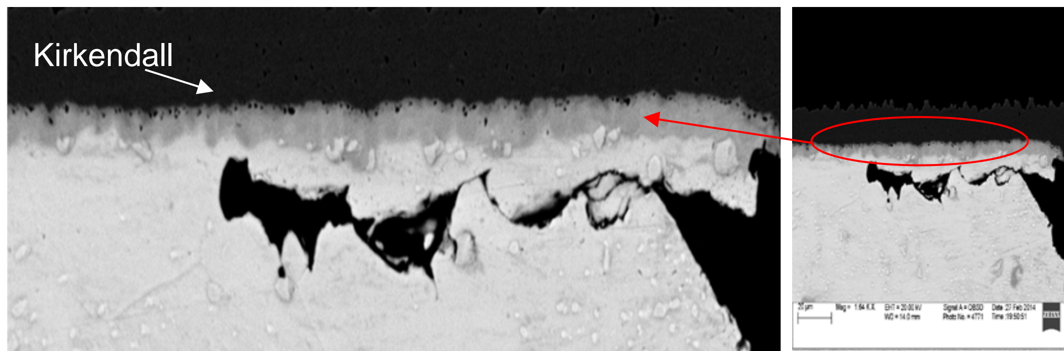


Figure 6.8 Kirkendall voids in 0.4mm pitch SAC305 solder on ENIG exposed to 12 months/125°C aging.

In Figure 6.8, growth of Kirkendall voids is shown at the interface between the intermetallic and Cu pad for cases of long-term, high temperature aged samples. Because of the unbalanced Cu-Sn interdiffusion through the interface, atomic-level vacancies left by migrating Cu atoms on the bare Cu side are not filled by Sn atoms. The vacancies coalesce into the so-called Kirkendall voids [57] [86]. The void formation weakens the interfacial structure and leads to high stress regions and crack development.

6.4 Discussion and conclusion

Significant reliability degradation was observed for SAC105 and SAC305 for the case of 15mm and 10mm packages on three board plating finishes during elevated temperature isothermal aging. SAC305 has better performance than SAC105 on all three board finishes with or without aging. After 12 months/85°C aging, the characteristic life for 10mm and 15mm SAC BGA packages on ImAg degraded ~ 40%, with ~ 50% reduction in characteristic life for 12 months/125°C aging. On ENIG or ENEPIG, the BGA package reliability reduced around 25% to 35% after aging at 85°C/125°C. BGA packages on ENIG and ENEPIG board finishes outperformed ImAg finish for any aging treatment. This is consistent with Yoon's study [80]. The For passive 2512 resistors on ImAg, the reliability performance reduced to 16.7% and 28% after 1-year aging at 85°C and 125°C, respectively. On ENIG and ENEPIG, however, the resistors degraded much faster (45% to 55% reduction rate). Resistor cross-sections revealed that cracks initiated at the ends beneath the component solder joints and then propagated through the entire interconnection.

Failure analysis showed dramatic intermetallic binary Cu-Sn and ternary Ni-Cu-Sn growth at the bottom solder joint interfaces for ImAg and ENIG/ENEPIG. The IMC thickness growth rate on ImAg suppress the rate on ENIG and ENEPIG after one year aging and this brittle IMC layer could be one of the root cause that ImAg board has less reliability performance than Gold based board plating. For 125°C aged samples, the cracks appeared at solder ball corners at both package and board side and propagated along (near) the interface IMC. For high temperature aged fine-pitch packages, the failures tended to propagate from the solder ball corner along a line downwards into the bulk solder. All cases that crack located not along the IMC layer but proceed into bulk solder indicated the recrystallization and grain structure changes significantly affect the joint structural stability during isothermal aging and thermal cycling test. Further microstructural observation need to be done carefully to provide more evidences to verify this assumption. Growth of Kirkendall voids is shown at the interface between the intermetallic and Cu pad for cases of long-term, high temperature aged samples. The void formation weakens the interfacial structure and leads to high stress regions and crack development.

Chapter 7

Summary and Conclusions

7.1 Literature Review

Isothermal aging has been found detrimental to the mechanical properties and the reliability of lead free solder materials. The dramatic changes in the material properties, constitutive and failure behavior of bulk solder materials as well as solder joints have been reported in the literature. However, traditional life prediction for solder joint reliability during thermal cycling accelerated life testing are based on solder constitutive equations and failure models that do not evolve with material aging. Thus, their validation of the data in real application under harsh environment is suspected. Previous studies in measured solder mechanical properties have been found and widely acknowledged due to the differences in the microstructures of the tested samples. This problem is exacerbated by the aging issue, as it is clear that the microstructure and material behavior of the samples change rapidly even at room temperature. For elevated temperature aging, this effect has been found to cause more dramatic change in the microstructure, material behavior and the reliability of lead free solder. Thus, the effects of aging on solder behavior must be better understood.

In the current study, a continuous aging at elevated temperature effect is considered during test. Test vehicles including several board surface finishes and two major solders were used on the various types of packages. The thermal fatigues on package size and ball pitch were also studied. Follow on; failure analysis and material analysis were performed to try to understand the microstructure evolving and failure mode changes throughout the entire test. Finally, good correlations have been found between the predictions of the constitutive and reliability models that include aging effects, and the experimental thermal cycling reliability data.

7.2 TV7-Phase I Reliability and Failure Analysis

After take the test vehicle aging for up 2 years and then subject to thermal cycling test and finalized the test result. A significant degradation in reliability has been observed for both SAC105 and SAC305 in 10mm packages on ImAg during elevated temperature isothermal aging. There were 9% and 50% reductions in characteristic lifetime for SAC105 and SAC305 after 24 months 85°C aging, respectively. After 2 years aging at 125°C, the package lifetime decreased by 61% for SAC105 and nearly 60% for SAC305. For passive 2512 resistors, the reliability

performance was reduced 25% and 35% after 24 months of aging at 85°C and 125°C respectively.

Failure analysis showed dramatic intermetallic Sn-Cu growth at the board-side solder joint interfaces over aging and cycling times. After 125°C aging, the cracks appeared at the lower corners at the board side interface and propagated along the Sn-Cu IMC. Different, new failure modes were discovered for fine-pitch packages which were also observed in our previous studies [70, 71]. Reduced Weibull lifetimes occur coincidently with increasing Sn-Cu layer growth at board and package sides of the solder joint. Resistor cross-sections revealed that cracks initiated at the ends beneath the resistor before propagating through the entire interconnection. We are currently exploring the manufacturability of new doped alloys and board level reliability in our ongoing work.

7.3 TV7-Phase II Reliability and Failure Analysis

For TV-7 phase II, we compared two Au based surface plating boards subjected to isothermal aging and thermal cycling test. The result has certain level of similarity with TV-7 phase I, that is, long-term thermal aging results in significant reliability degradation for Sn-37Pb, SAC105, and SAC305 solder alloys on ENIG and ENEPIG. The reduction of reliability is observed throughout the aging period. There was ~ 25% reduction in characteristic lifetime for SAC105 and SAC305 on ENIG during 12 month/85°C aging and ~ 35% degradation on ENEPIG. After 12 months/125°C aging, the package lifetime decreased ~ 40% for SAC105 and SAC305. Sn-37Pb solder outperformed the SAC alloys over long-term aging.

Failure analysis showed dramatic intermetallic Ni-Cu-Sn growth at the board-side solder joint interfaces. After 125°C aging, the cracks appeared at the lower corners at the board side interface and propagated near the Ni-Cu-Sn IMC region. Different new failure modes were discovered for fine-pitch packages. In that case, cracks not only propagate along the IMC region at both sides of the joint but proceed into the bulk solder. Ag-Sn IMC coarsening effectively pins the crack growth path for higher Ag content alloys such as SAC305.

7.4 TV-7 Plating Comparison Analysis

At last, we compared data through all board plating in phase I and phase II and try to discover the different thermal effect on various board finishes. The data revealed that significant reliability degradation was observed for SAC105 and SAC305 for the case of 15mm and 10mm packages on three board plating finishes during elevated temperature isothermal aging. SAC305

has better performance than SAC105 on all three board finishes with or without aging. After 12 months/85°C aging, the characteristic life for 10mm and 15mm SAC BGA packages on ImAg degraded ~ 40%, with ~ 50% reduction in characteristic life for 12 months/125°C aging. BGA packages on ENIG and ENEPIG board finishes outperformed ImAg finish for any aging treatment. For passive 2512 resistors on ImAg, the reliability performance reduced to 16.7% and 28.1% after 1-year aging at 85°C and 125°C, respectively. On ENIG and ENEPIG, however, the resistors degraded much faster (45% to 55% reduction rate).

Resistor cross-sections revealed that cracks initiated at the ends beneath the component solder joints and then propagated through the entire interconnection. Failure analysis showed dramatic intermetallic binary Cu-Sn and ternary Ni-Cu-Sn growth at the bottom solder joint interfaces for ImAg and ENIG/ENEPIG. For 125°C aged samples, the cracks appeared at solder ball corners at both package and board side and propagated along (near) the interface IMC. For high temperature aged fine-pitch packages, the failures tended to propagate from the solder ball corner along a line downwards into the bulk solder.

7.5 Future Work

7.5.1 Continuous study on TV-7

With more data coming out, the analysis would cover more package type as CSP and QFN. Data mining in depth would apply on current and future data in order to discover the characteristic lifetime variation of different package types. For instance, 2512 resistor package has significant reliability degradation on ENIG and ENEPIG board finishes (over 40% reduction) compare with ones on ImAg or ImSn finishes (around 20%) but sharing similar failure mode in cross section BSE images. Also for the case that how to interpret the characteristic life cycle into a real expecting failure cycle in field or in product's prototype can be further studied. Certain appropriate data analysis models to fit the current data can achieve the challenge. A compete data base would be generated with certain solder joint life prediction functions which can provide a full aspect on the current applied solder materials and board plating combinations for industries or academics. More options could be given to them and allow to have more detail research.

Finite element analysis would be used to construct to model of the solder joint and correlated with test result to have prediction of joint life in further. Detailed stress strain analysis can be achieved from the model to build up the joint thermal fatigue theory regarding long-term

aging effect. Microstructure analysis would be kept on to discover the root cause of different of failure mode. Morphology changes such as grain structure evolving and types of IMC growth at various geometric locations need to be carefully studied in order to understand the creep effect on joint reliability reduction. Also, better recording the microstructure changes need to be done in order to finalize more valuable aspect such as cracked join ratio of up or bottom areas. With higher standard in experimenting and recording that helps the researchers to construct more accurate and scientific studies.

7.5.2 **Doping project**

Auburn is currently engaged in a multi-million dollar Solder Doping (micro-alloying) study to find a solution for the harsh environment electronics industry. This program involves government, the vehicle community and most solder suppliers for the vehicle community.

The Primary Goal of this test is to find a manufactureable solder paste that will mitigate the effects of aging on lead free solder joints (both grid arrays and leadless packages). A secondary goal would be to find a paste for solder doping that could be used for individual package reliability enhancement and a solder for solder-sphere replacement to enhance the solder joint reliability. More than 10 types of different solder material would be applied with three board platings intent to find out the best major combination of solder/plating system. Also, double-side reflow boards would be manufactured and tested. LGA would also be concluded into test to bring more variety of the test matrix. For isothermal aging, only high temperature is considered (1-year 125°C aging) in testing. Same monitoring system and cycling profile would be kept in order to keep data consistency. The out coming data and further microstructure morphology study would be analyzed and compare with TV-7's result to construct a bigger blue print of lead-free solder joint reliability performance.

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