Die Attach for High Temperature Applications

by

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Abstract

The energy sector is seeing dynamic growth with advanced oil and gas recovery methods being deployed. Measure-while-drilling (MWD) and downhole production instrumentation is important to maximize production and safety. Well temperatures are moving past 175^{o}C therefore 200^{o}C instrumentation is increasingly in demand. Power electronics are required as part of the downhole measurement tools, geothermal and aerospace exploration instruments. Die attach materials and technology for high-temperature electronics that can be used in 200^{o}C, 300^{o}C and 500^{o}C applications were developed and evaluated with reliability tests.

Die attach using AuSn liquid phase transit (LPT) bonding for 500^{o}C applications was investigated. Both single and double prints of the PtPdAu thick film layers were evaluated. Both of the samples show good mechanical reliability for high temperature storage. The assembly process for two test circuit boards using AuSn liquid phase transit (LPT) bonding and thick film substrates for 300^{o}C application were developed. The dual in line package (DIP) socket board had contact stability beyond 3000 hours.

An innovative die attach method using Au sintering with patterned die and Au thick film paste was developed. The patterned gold die attach technology using micro-scale gold paste has been evaluated and showed the potential for applications at 500^{o}C. The patterns on both the thin film die backside metallization and thick film substrate has successfully created controlled voiding which allows the burnout gas to escape during the firing process. The shear strength after aging meets the MIL-STD-883 die attach requirement and this die attach method should be stable for use to 700^{o}C.

AgBiX solder has potential for 200oC applications. This alloy has been used to assemble SiC test die to ceramic substrates with direct bond copper (DBC), reactive brazed CuMo, thick film PtPdAu, thick film PdAg and thick film Ag. Surface mount chip resistors have also been attached to thick film metallized substrates. The assembly process and initial shear strength test results are presented. Assemblies have also been subjected to thermal cycling -55^{o}C to +195^{o}C) and high temperature (200^{o}C) storage. From the test results, the solder paste is compatible with all of the listed substrates above, except the thick film PtPdAu and thick film Au substrates. This solder paste is a promising lead-free solder paste for 200^{o}C applications.

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CHAPTER 1 INTRODUCTOIN

With the demand for increased energy supplies and more electric vehicles, many industries are calling for electronics that are able to work in harsh environments, such as extreme high temperature. High temperature electronics are playing a very important role nowadays and there is a continually growing demand for high temperature electronics in various fields. The traditional method is to rely on an additional active or passive cooling system when designing the electronic device. However, this approach may not be possible in some cases. It's more appealing for the electronic devices to operate hot to improve system reliability and reduce the cost. This choice leads us to the challenges on many aspects, especially the packaging techniques.

1.1 High Temperature Electronics (HTE)

The definition for "High Temperature Electronics" is electronics operating at temperatures in excess of those normally encountered by conventional, silicon-based semiconductor or their auxiliary components. Currently, there's different ranges cited by experts to define the realm of "High temperature" in the literatures. The operation temperature limits for conventional silicon device is set at 70^{o}C to 85^{o}C, with some special military application temperature up to 125^{o}C. Thus electronics operating at temperatures beyond 125^{o}C is taken to mean "High Temperature Electronics" [1]. However, in this dissertation, the electronics need to operate at a much higher temperature based on the application environment.

1.2 Applications of High Temperature Electronics

Commercial and military aircraft that can fly at greater than the speed of sound with improved safety, reliability and maintainability; automobiles with longer lifetimes and greater fuel economy, chemical processes with ultra-precise control and minimal waste--these are the applications that require high temperature electronics. For example, on-engine aircraft sensors and electronics can require operating temperatures of 500^{o}C and higher. Electronics for probing and analyzing the surface of Venus will also require an operation temperature of approximately 485^{o}C. Temperature for down hole oil and gas well logging systems range from 150^{o}C to 300^{o}C depending on the location and depth, while geothermal wells have an operation temperature of 250^{o}C to greater than 350^{o}C. Example applications and use temperature are listed in Table 1.1[2].

Table 1.1 Applications Area and Characteristics for High Temperature Electronics [2]

Application	Temperature(^{o}C)	Minimum Duration	Duty	Other Environmental Factors
Well-logging Gas&Oil instrumentation	150 to 300	Few hours- years	Intermittent/cyclical or continuous	Temperature cycling, chemical, pressure, vibration
Geothermal	150 to 400	Few - 100	Intermittent cyclical	Temperature cycling, chemicals, pressure, vibration
Aircraft systems On engine & smart transducers	300 to 500	100	Intermittent cyclical	Temperature cycling, vibration, stress, fuel/oil
Aircraft engine	500 to 600	100	Intermittent cyclical	Temperature cycling, vibration/shock

Automobiles	150 to 250	8000 operating, 10 years "shelf"	Intermittent cyclical	Temperature cycling, fuel/oil, rough handling
Nuclear Reactors	200 to 450	Months to years	Continuous	Radiation
Space exploration	125 to 485	Month to years	Intermittent/cyclical or continuous	Temperature cycling, chemical, pressure

1.3 Die Attach Technology

SiC is an ideal material for high power and high temperature electronics applications. It has a wide band-gap, high thermal conductivity and high breakdown electrical field strength. SiC devices and sensors have been demonstrated for extended operation at 500^{o}C and 600^{o}C [3]. However, there are many technical challenges involved in developing electronic systems that function at high temperature. These include proper IC design, the appropriate use of passives, and robust and reliable packaging that is capable to operate throughout its entire designed life. In order to build functional systems, multiple devices must be interconnected.

Electronics packaging provides protection for the semiconductor devices, a means of electrically interconnecting those devices along with passive and other components, and a path for heat removal.

Die attach is the joining of the die to the package or substrate, while substrate attach joins the substrate to the package. The first role of the attach material is to provide a mechanically joint. The attach material may also provide electrical connection and a thermal path for removing heat. Die and substrate attach is one of the most challenging aspects of high temperature packaging. The difference in coefficients of thermal expansion (CTE) between the die/package, die/substrate or substrate/package to be joined results in stresses on the attach material and the

die/package, die/substrate or substrate/package. High temperature applications result in wider temperature cycle ranges, and thus higher cyclic stresses leading to fatigue failure.

1.4 Die Attach Requirements

For most high-power semiconductor packaging configurations, the predominant heat dissipation path from the device is through the die attach material. Because the die attach layer is the first packaging layer in contact with the die, its thermal characteristics are the most critical. These characteristics include die attach layer thickness, thermal conductivity, and the thermal resistance at interfaces between the die attach, the device, and the package. Besides thermal dissipation, electrical conductivity is also a highly critical property for most high-power semiconductor applications. Electrical resistance between the die and the package results in joule heating, which is an energy-loss mechanism. Thus, the energy efficiency of the device is directly influenced by the electrical performance of the die attach layer, which is most critical for power semiconductors where the largest contribution to the critical RDS(ON) parameter is typically the die attach layer. In this case, reducing the resistance of the die attach will reduce the magnitude of RDS(ON) and improve the energy efficiency of the device.

The die attach layer is also the mechanical interface between the low thermal-expansion die (silicon carbide 4.2 ppm/℃) and the packaging material. For die bonded to a copper paddle, for example, the copper CTE is 17 ppm/℃. If the CTE induced stress is large, portions of the die can go into tension and die cracking can result. More importantly, thermal cycling can result in fatigue cracking of the die attach layer.

1.5 Die Attach Materials

Die and substrate attach materials fall into five categories: 1) polymer, 2) Ag-glass, 3) solders and brazes, 4) liquid phase transient bonding, and 5) sintered nano-particles. In this

dissertation, we are going to focus on die attach using liquid phase transient bonding, sintering, and solders.

1.5.1 Liquid Phase Transient (LPT) Bonding

Liquid phase transient (LPT) bonding is a joining process which has been widely used in many metallic systems for a long time. This bonding technique is derived from high temperature fluxless vacuum brazing [4, 5]. The process involves a low melting point element or alloy that forms intermetallics or diffuses into the materials to be joint, so that the solidification temperature of the joint changes with the composition of the liquid phase joint. The main advantage of liquid phase transient bonding is that it can obtain a bond with higher melting point than the bonding temperature. Thus the bonds can achieve a higher operation temperature than the process temperature. Silver-indium die attach material has been proposed [6, 7]. In order to provide better gap filling, In-Ag paste has been developed for die attach on Ag/Ni direct bond copper [8]. One concern with die attach using high Ag is Ag migration under bias at high temperature [9,10]. Gold based die attach using off eutectic Au-Sn has been demonstrate for high temperature die attach [11].

1.5.2 Sintering

While not on the nano-scale, Salmon, et al. [12] and Chen, et al. [13] have demonstrated die attach based on thick film Au conductor paste. The Au particles in this paste are on the μm-scale and a firing temperature of 600^{o}C was required. The challenge in the processing was void formation due to out gassing during burnout of the organic binder in the thick film paste.

1.5.3 Solder Paste

Historically, high lead content solders with solidus temperatures of 287^{o}C to 309^{o}C have been used for power die attach. However, due to international legislation, the use of lead in

solders has dramatically decreased. Due to the lack of suitable replacements for high lead solders in high temperature applications, high lead solders are exempt to Restriction on Hazardous Substances (RoHS) Directives. High lead solders are still widely used for power die attach [14, 15, 16], while alternatives are being sought. Sn/Sb (95/5) has been proposed with a solidus temperature of 243^{o}C, however, 200^{o}C data was not presented [17].

Lead-free Sn-Ag-Cu (SAC) solder alloys with melting points of 217-227^{o}C are marginal for use at 175^{o}C, limiting their applicability in these applications. Significant work has been published on AuSn [18, 19], AuGe [20] and AuSi [21, 22] as high temperature alloys for operation at 300^{o}C and higher. However, these are high cost alloys. For cost sensitive applications, alternate alloys are desired.

A AgBiX solder paste (AgBiX®, Indium Corporation) has been developed to provide a higher temperature, lead-free solder alternative [23, 24, 25]. In the AgBiX alloy, it is the 'X' component that forms the intermetallic. Ag does not form intermetallics with Bi, Cu or Ni. By limiting the amount of X, the amount of X-based intermetallic formed initially and with high temperature aging can be limited.

1.6 Substrate

There are different substrates options that can be used for high temperature electronics packaging: printed circuit boards, thick film, thin film, low temperature cofired ceramic (LTCC), high temperature cofired ceramic (HTCC) and copper foil on ceramic.

Thick film on Al_2O_3 has been examined by a number of researchers for use up to 500^{o}C [26, 27]. An example thick film circuit for 300^{o}C operation is shown in Figure 1. Riches, et al. has demonstrated thick film modules to 275^{o}C [28]. The metallization systems have been Au or

PtPdAu. Zhang, et al. has examined the compatibility of thick film conductors with dielectrics for 300^{o}C operation [29].

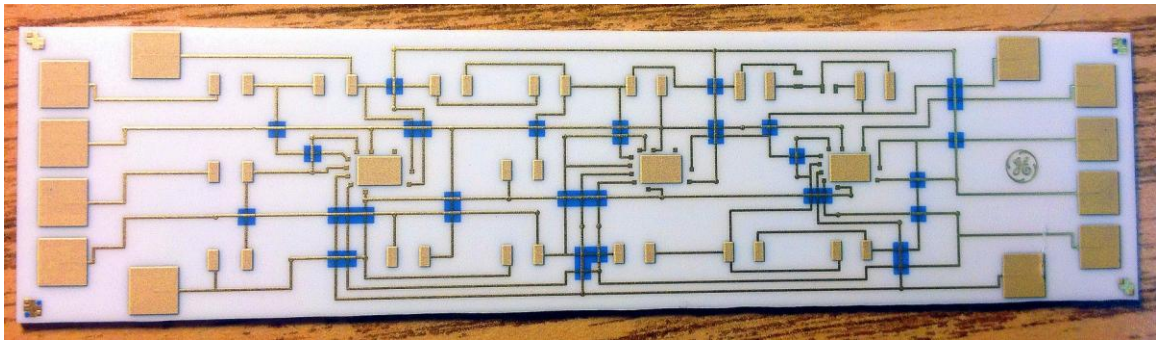


Figure 1.1 Pressure to Frequency Board Thick Film Substrate

For high current power applications, thick Cu foil on ceramic is used. A number of techniques are used to attach Cu to ceramics. Direct bond copper (DBC) on Al_2O_3 is the most common. At temperatures just below the melting point of Cu (m.p. 1083^{o}C) in a low partial pressure of oxygen, $CuAlO_2$ forms at the interface, creating a bond. Direct bonding can also be achieved with AlN substrates if a thin layer of Al_2O_3 is formed on the surface by thermal oxidation.

Johnson, et al. has demonstrated DBC on Al_2O_3 for static operation at 400^{o}C [30]. The modules assembled with Au-Sn LPT were reliable with a electrolytic Ni/Au surface finish, but failed with an electroless Ni:P/Au finish. A thick plated Au layer was used on the substrate to delay Ni reaching the outer Au surface.

1.7 Research Outline

The goal of the project was to evaluate and develop die attach materials and technology for high-temperature electronics that can be used in 200 ^{o}C, 300 ^{o}C and 500 ^{o}C applications. The environmental condition of the application involves continuous high temperature exposure and thermal cycles.

Chapter 2 describes an investigation of LPT AuSn die attach for 500^{o}C applications. This chapter includes substrate technology, die metallization, and die attach bonding process. Different thicknesses of PtPdAu thick film were used to metalize the substrate. Results of die attach reliability based on die shear strength after the high temperature storage test are discussed. The process of multi-chip-module assembly using LTP bonding was demonstrated. Two types of test boards were fabricated using thick film technology and LTP bonding.

Chapter 3 presents die attach using Au sintering for 500^{o}C applications. An innovative die attach method using patterned die and Au thick film paste were developed. The detailed procedure and high temperature storage test results are included in Chapter 3.

Chapter 4 reports the characterization of AgBiX solder paste on different die attach substrates for 200^{o}C applications. Die attach materials, assembly process development, reliability testing and failure analysis are included in this chapter. A discussion of the mechanisms behind the shear strength data is also presented.

Chapter 5 summarizes the conclusion of this work and proposed ideas for future work.

CHAPTER 2 DIE ATTACH USING AUSN LIQUID PHASE TRANSIENT BONDING

2.1 Introduction of Off-eutectic AuSn

There are several advantages of Au-Sn. AuSn is fluxless which does not require a chemical flux to remove oxides and prepare the surface. Eliminating flux and flux cleanup shortens the assembly process. The big advantage of fluxless soldering is the ability to get void-free die attach since there is no volatile materials in flux to get trapped under the die. AuSn solder readily wets bond pads for strong, uniform, void-free joints, a deficiency with some newer lead-free substitutes. What makes AuSn an attractive die attach material for high temperature is its excellent thermal properties. The high thermal conductivity of AuSn rapidly carries heat away without creating excessive stresses, a major concern in high-density packaging. In addition, the good electrical conductivity of AuSn provides low-resistance connections important for high power devices, as shown in Table 2.1 [31].

Properties	
Density	14.7 $g \cdot cm^{-3}$
Coefficient of thermal expansion*	16×10^{-6} /°C
Thermal conductivity	57 $W \cdot m^{-1} \cdot K^{-1}$
Tensile strength	275 MPa
Young's modulus	68 GPa
Shear modulus	25 GPa
Poisson's ration	0.405
Electrical resistivity	16.4×10^{-8} $\Omega \cdot m$
Elongation	2 %

Table 2.1 Physical properties of Au/Sn 20/80 wt% [31]

In this work, Au-Sn preforms have been used as the die attach material. With excess Au dissolved from the backside of the die and thick film metallization on the substrate, the wt% of Au in the die attach joint increases, and the solidus temperature of the Au-Sn joint increases (Figure 2.1).

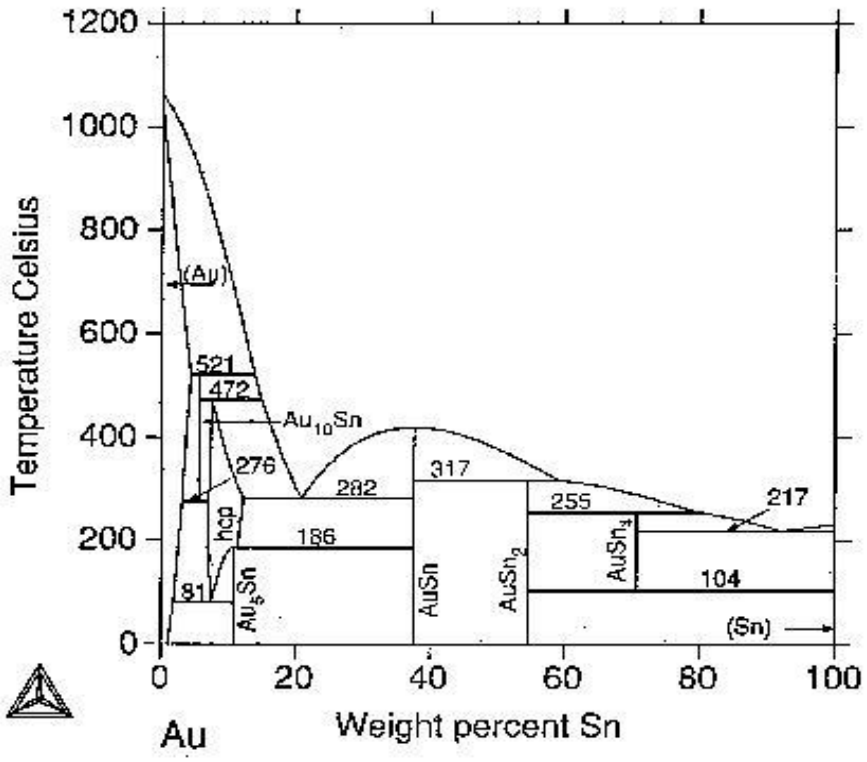


Figure 2.1 Au-Sn Phase Diagram [32]

2.2 Substrate Metallization and Fabrication

Alumina oxide (Al_2O_3) has a CTE of 7.2ppm/^oC, which is the most common substrate for thick film and has the largest selection of commercially available thick film paste. Also, it provides super abrasion, high temperature and chemical resistance, and excellent dielectric

properties from DC to GHz frequencies. For these reasons, alumina oxide was been selected for investigation for SiC high temperature electronics packaging.

For thick film processing, a PtPdAu thick film conductor paste, C6029 from Heraeus, was screen printed onto Al_2O_3 using a patterned 320 mesh screen. The patterned paste was dried in air at 150^{o}C for 15 minutes, then fired using an 850^{o}C (10 minutes) peak profile (Figure 2.2). A pure Au paste (no binder), 5063D from Dupont, was then printed, dried and fired over the fired PtAu thick film using the same process. The pure Au layer on the top was to provide additional Au for the off-eutectic AuSn die attach process. Pull testing of those inks has been previously done to demonstrated good adhesion to the Al_2O_3 substrate [33].

For the thick film metallization on Al_2O_3 substrate, both single and double prints of the PtPdAu thick film layers were evaluated. A double print increased the volume of Pt and Pd to react with the Sn from the AuSn preform.

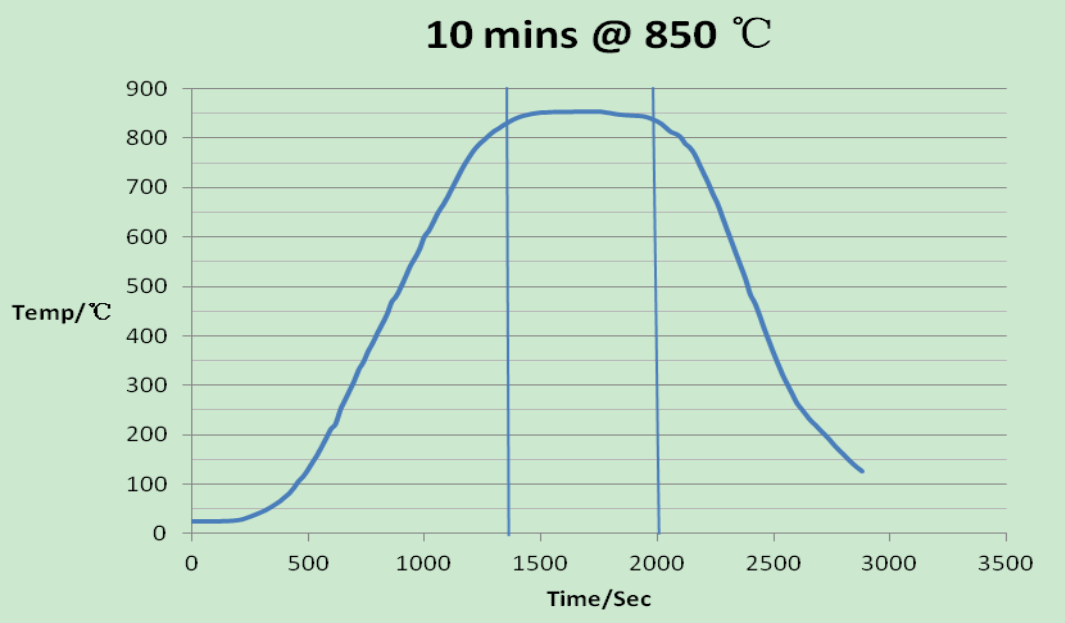


Figure 2.2 Thick Film Firing Profile with Peak temperature of 850^{o}C

2.3 SiC Die Metallization and Fabrication

Tested die were fabricated using SiC wafers. The wafers were cleaned with a full wet chemical cleaning process prior to thin film deposition. The cleaning process is list below:

- SiC wafer was immersed in the following solution for 5 minutes in ultrasonic: Acetone, TCE (Trichloroethylene), Acetone, Methanol, Methanol, De-ionized water (DI water)
- Then SiC wafer was immersed in sequences in the following solution for 5 minutes: BOE, DI water
- RCA (Radio Corporation of America) style cleaning was used to remove inorganic and organic contaminants on the SiC wafer. The SiC wafer was:

a) Immersed in a H_2SO_4: H_2O_2 (Vol. ratio 1:1) solution for 15 minutes. Then rinsing the wafer in DI water for 30 seconds, BOE for 1 minutes and DI water for 30 seconds.

b) Immersed in a DI H_2O: NH_4OH: H_2O_2 (Vol. ratio 3:1:1) solution heated on a hot plate to boil gently for 15 minutes. Then rinsing the wafer in DI water for 30 seconds, BOE for 1 minutes and DI water for 30 seconds.

c) Immersed in a HCL: H_2O_2: DI H_2O (Vol. ratio 1:1:3) solution heated on a hot plate to boil gently for 15 minutes. Then rinse the wafer in DI water for 30 seconds, BOE for 1 minutes and DI water for 30 seconds.

- Blow dry well with N_2 gas

The thin film layers were deposited on the carbon face of the wafer. After 3 minutes of in-situ ion milling, a three layer thin film stack of Ti/Ti:W/Au (8nm/62nm/100nm) was deposited by e-beam evaporation. A 3 minutes ion milling process was used prior to the deposition of each layer. After thin film deposition, additional Au was electroplated on the backside of the SiC

wafer to produce a final thickness of 4 μm. The wafers were diced into 2mm x 2mm die for the high temperature storage test vehicle assembly.

2.4 Die Attach with Eutectic AuSn Preform

The test vehicles were assembled with AuSn (80wt%Au/20wt.%Sn) preforms. The preforms (25.4μm thick) were purchased from Materion. Before assembly, both die and substrate were placed in an argon plasma cleaning system for sputter cleaning. The cleaning condition was 1 Torr Ar for 5 minutes at 300 watts. In order to control the amount of Sn available, the perform was cut to 0.67mm x 0.67mm for the assembly of a 2mm x 2mm SiC die. Figure 2.3 illustrates the substrate being assembled in the SST 3150 high vacuum furnace. 500 grams of weight was used on the top of the fixture to help the AuSn flow and spread over the entire die attach area during the brazing process.

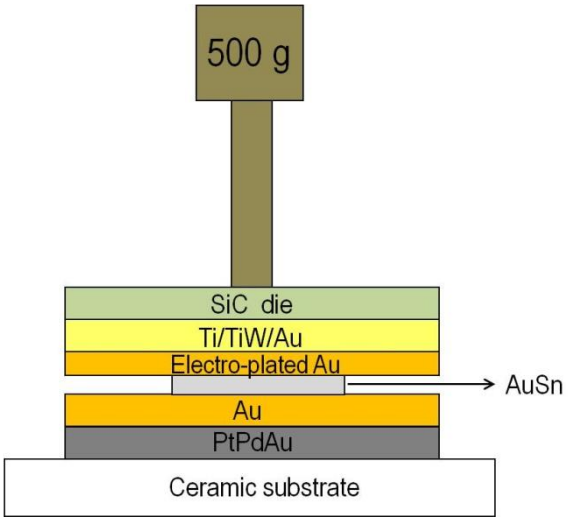


Figure 2.3 AuSn Die Attach Configration

The SST reflow profile (Figure 2.4) for the AuSn die attach was: peak temperature of 330^{o}C for 5 minutes followed by a soak at 280^{o}C for 20 minutes. During the reflow process, the

AuSn perform liquefied, rapidly dissolving Au from both the substrate side and the die side. The melting point of the joint increased as the Au dissolved. The 20 minutes soak time allowed Sn to continue to diffuse into the thick film layers, lowering the Sn concentration throughout the die attach layer. Therefore, after the reflow, the melting point of die attach joint was raised to over 500^{o}C. The Sn will continue to diffuse toward the equilibrium concentration in the high temperature working environment. A high temperature die attach was achieved using a low temperature reflow profile.

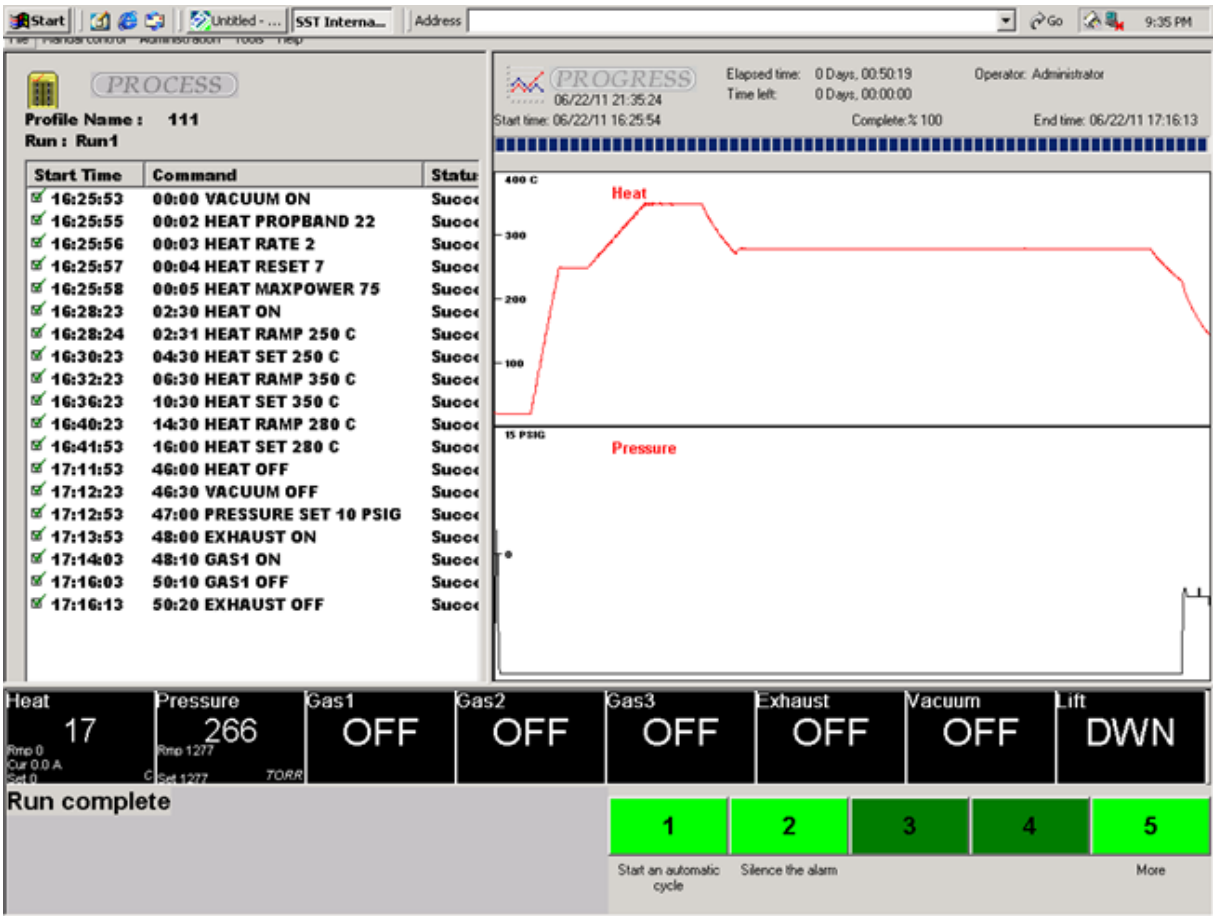


Figure 2.4 Off-eutectic AuSn SST Bonding Profile

After the assembly, the test vehicle was inspected under X-ray to check the voiding. As shown in Figure2.5, void-free die attach was achieved.

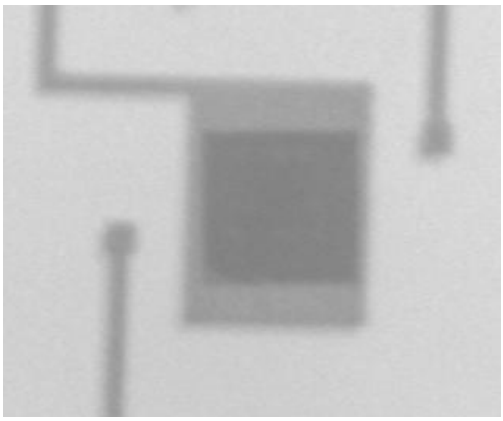


Figure 2.5 X-ray Results for SiC Die Attach with AuSn Preform

2.5 High Temperature Storage Test

Both single and double prints of the PtPdAu thick film metallized substrates were evaluated with AuSn die attach in the high temperature storage test. Assembled parts were stored in a Blue-MOV-10C high temperature chamber at 500^{o}C for long-term reliability tests. Die shear tests were performed at different time intervals to evaluate the mechanical reliability of the joint with aging. A Dage 2400PC shear tester with a 100Kg load cartridge was used to shear the samples. The die shear strength (shear force in Kg divided by die area in mm^2) as a function of storage time at 500^{o}C is shown in Figure 2.6. The columns on the left are data from die attach on single printed substrates, the columns on the right are the data from die attach on double printed substrates.

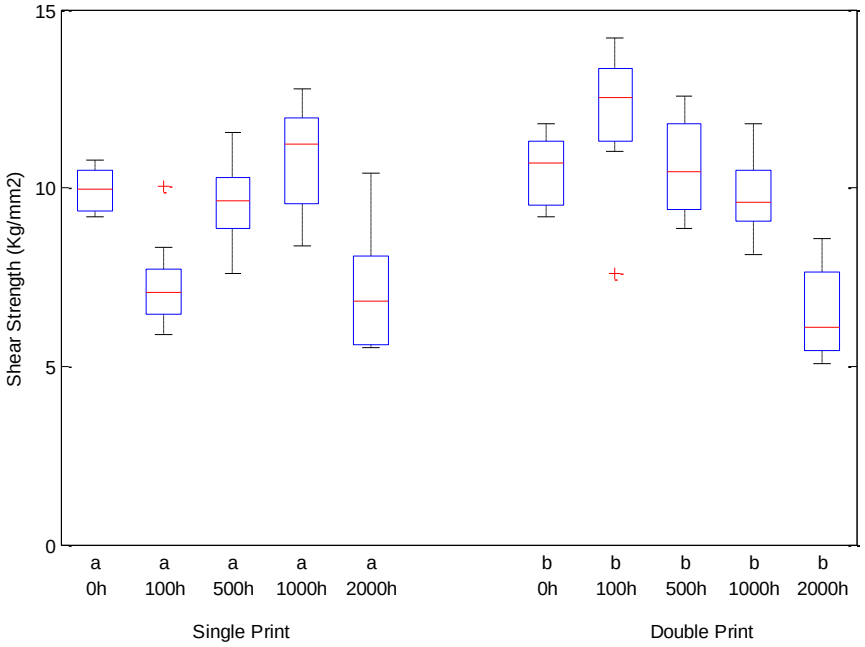


Figure 2.6 Die Shear Test Results for Single and Double PtPdAu Thick Film Substrates as a Function of Storage Time at 500^{o}C

For die attach on single PtPdAu printed substrates, the shear strength decreased during the first 100 hours, then increasing to 11.83kg/mm^2 after 1000 hours storage. While the sample with double printed substrates, the shear strength increased during the first 100 hours and then decreased to 9.79kg/mm^2 after 1000 hours storage. After 2000 hours storage at 500 ^{o}C, the shear strength of double printed and single printed samples were 6.583kg/mm^2 and 7.215kg/mm^2 respectively. For both the single printed and double printed samples, the failure mode was in the PtPdAu layer, near the substrate interface, as shown in Figure 2.7. The student T test was done to evaluate the statistics difference of both samples after 2000 hours of storage. The value of possibility is 0.50, which is greater than 0.05, so there is no significant difference on the shear strength of two samples after 2000 hours of aging.

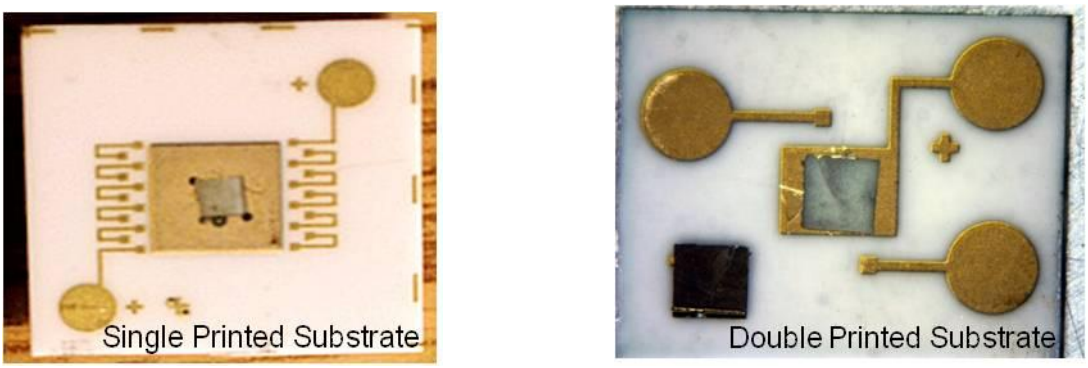


Figure 2.7 Fracture Surface of Single Printed Sample (left) and Double Printed Substrate (right) after 2000 hours storage at 500^{o}C

Energy-dispersive X-ray spectroscopy (EDX) analysis of the cross sections of both samples after 2000 hours was used to investigate Sn distribution in the die attach joints. For double printed AuSn die attach, EDX analysis shows a low Sn concentration near the die, low Sn concentration through the joint, then a higher Sn concentration in the PtPdAu layer (Figure 2.8). Plus, at some points, there's Pt, Pd and Sn. That indicates Sn reacts with Pt and Pd to form the intermetallics.

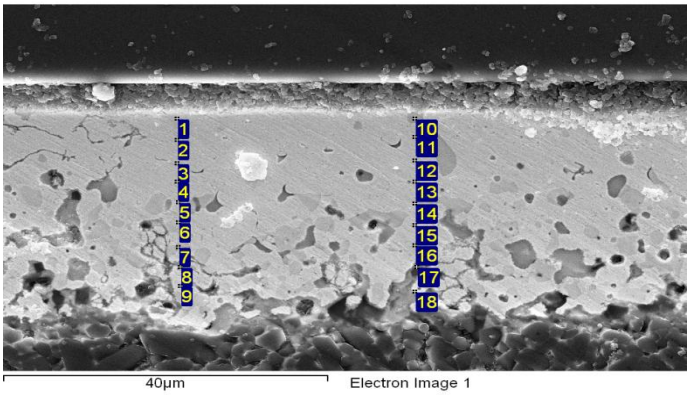


Figure 2.8 Elemental Analysis Across Die Attach Joint of 2000 Hours Aged Double Printed Samples (Part A)

Spectrum	Au	Sn	Pd	Pt	Bi	Si	Al
1	98.79	0	0	0	0	1.21	0
2	98.81	0	0	0	0	0.78	0.42
3	99.43	0	0	0	0	0.57	0
4	97.36	0	1.94	0	0	0.7	0
5	99.5	0	0	0	0	0.5	0
6	98.28	0	0	0	0	0.95	0.77
7	88.57	6.24	0	3.87	0	0.81	0.5
8	38.74	30.07	4.15	24.91	0	1.57	0.57
9	99.12	0	0	0	0	0.88	0

Spectrum	Au	Sn	Pd	Pt	Bi	Si	Al
10	27.94	28.78	35	7.53	0	0.75	0
11	99.2	0	0	0	0	0.8	0
12	99.48	0	0	0	0	0.52	0
13	96.88	1.82	0	0	0	0.78	0.52
14	99.41	0	0	0	0	0.59	0
15	99.42	0	0	0	0	0.58	0
16	99.58	0	0	0	0	0.42	0
17	55.1	11.75	0	18	3.02	0.51	11.62
18	71.07	8.1	0	1.87	7.57	0.35	11.04

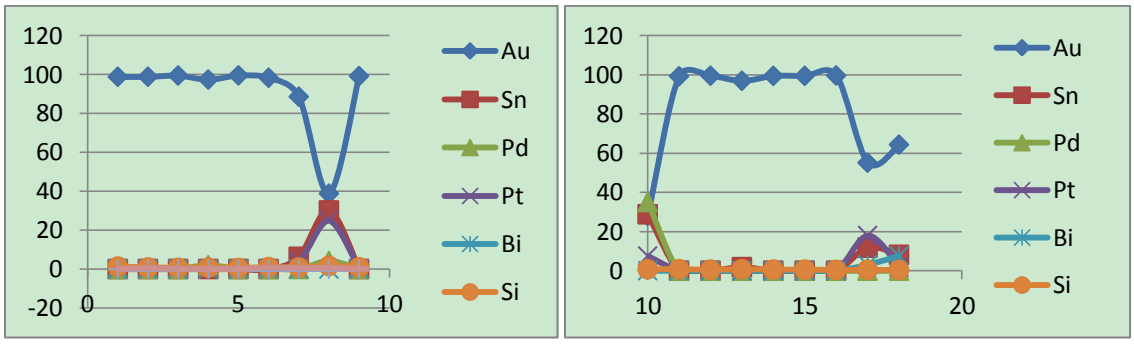
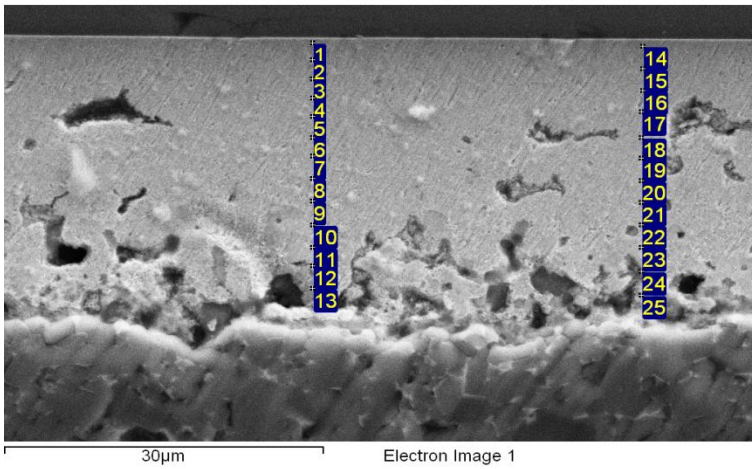


Figure 2.8. Elemental Analysis Across Die Attach Joint of 2000 Hours Aged Double Printed Samples (Part B)

For single printed samples, after 2000 hours aging at 500^{o}C EDX analysis indicate the same results, as shown in Figure 2.9. however the Sn extends toward the substrate beyond the Pt and Pd peaks. While Sn-Pd and Sn-Pt intermetallics formed, it is likely there is insufficient Pd and Pd to react with all of the Sn.



Spectrum	Au	Sn	Pd	Pt	Bi	Si	Al
1	98.18	0	0	0	0	0.95	0.88
2	98.32	0	0	0	0	0.71	0.98
3	99.05	0	0	0	0	0.46	0.49
4	100	0	0	0	0	0	0
5	99.39	0	0	0	0	0.61	0
6	99.56	0	0	0	0	0	0.44
7	100	0	0	0	0	0	0
8	99.48	0	0	0	0	0	0.52
9	99.39	0	0	0	0	0	0.61
10	99.47	0	0	0	0	0.53	0
11	99.18	0	0	0	0	0	0.82
12	93.99	4.77	0	0	0	0.51	0.74
13	92.7	4.89	0	0	0	0.72	1.69

Figure 2.9. Elemental Analysis across Die Attach Joint of 2000 Hours Aged Single Printed Samples (Part A)

Spectrum	Au	Sn	Pd	Pt	Bi	Si	Al
14	99	0	0	0	0	1	0
15	100	0	0	0	0	0	0
16	99.34	0	0	0	0	0.66	0
17	97.72	1.71	0	0	0	0.57	0
18	100	0	0	0	0	0	0
19	99.41	0	0	0	0	0.59	0
20	100	0	0	0	0	0	0
21	97.34	2.15	0	0	0	0.51	0
22	96.48	2.41	0	0	0	0.62	0.49
23	42.16	25.9	2.81	28.48	0	0.64	0
24	37.7	45.31	0	5.22	6.4	0.96	4.41
25	38.9	52.69	0	3.51	0	0.71	4.2

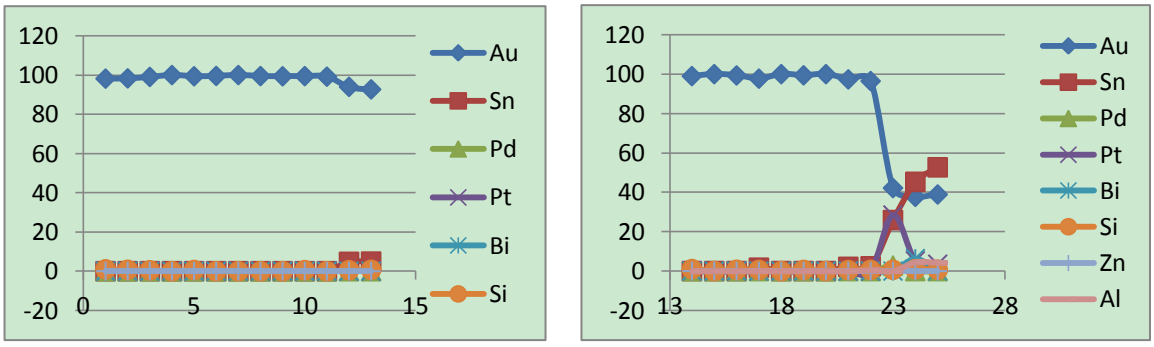


Figure 2.9. Elemental Analysis across Die Attach Joint of 2000 Hours Aged Single Printed Samples (Part B)

According to the EDX analysis of the cross section, there was a high concentration of Sn near the substrate, where it formed Pt-Sn and Pd-Sn intermetallic. EDX of the substrate fracture surface also detected rich Sn concentration and the glass from the thick film. But neither Pt nor Pd was detected. The hypothesis is: with 500^{o}C aging, Sn from AuSn perform diffused into the thick film layer and reacted with Pt and Pd to form Pt-Sn and Pd-Sn intermetiallics. But the Pt and Pd from the PtPdAu layer was not sufficient for all of the Sn to react. So the remaining Sn continued to diffuse into the glass layer as aging continued. Sn does not form intermetallics with

any elements in the glass. Thus, this Sn and glass region may be weak so we failed at this interface after 2000 hours aging. Also, the decrease in adhesion with aging at 500 ^{o}C may be related to Sn diffusion into glass in the thick film. Barry E. and John J. Felten had done some research that shows the interaction of Sn with the glass in the thick film [33].

LPT AuSn bonding provides a method to achieve die attach for applications up to 500 ^{o}C. The test results indicate that using a limited volume eutectic AuSn perform with excess Au provided by the die and the substrate can achieve high bonding reliability. Both double printed samples and single printed samples were assembled and tested, in the first 500 hours of aging, the double printed samples had a better performance than single printed samples. But after 2000 hours aging, there is not a significant difference in the shear strength.

2.6 Applications Using AuSn LPT bonding

Based on the liquid phase transient die attach technology with AuSn solder alloy on thick film metalized substrates, two test circuit boards for 300^{o}C applications were fabricated. A pressure to frequency test board used in a geothermal application to convert the pressure data into a frequency signal was assembled. A DIP socket test fixture to perform long term reliability testing of high temperature devices for long term at 300^{o}C was also fabricated.

2.6.1 Pressure to Frequency Test Board

The pressure to frequency circuit thick film ceramic substrate layout was designed based on the circuit schematic developed by GE Global Research Center. The alumina substrate size was 1 x 4 inch based on the application requirement. The designed test board is shown in Figure 2.10.

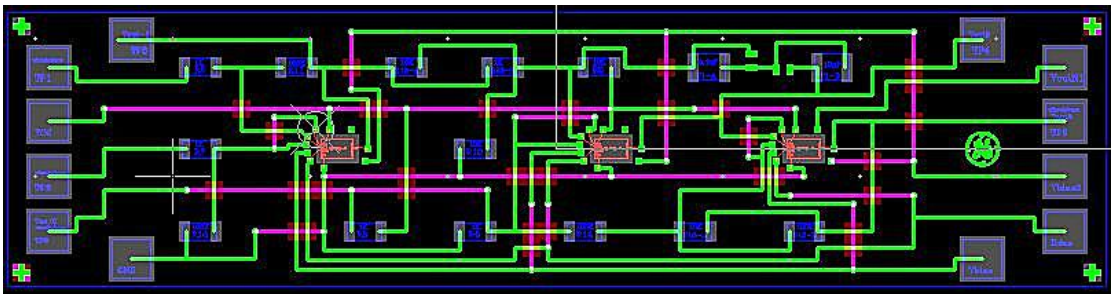


Figure 2.10 Layout of Pressure to Frequency Test Board

2.6.1.1 Substrate Fabrication

An MPM TF 100 screen printer was used to print the substrate automatically. The squeegee material was also from MPM, with a hardness of 60 durometern (Scale A). The thick film conductors (C6029, 5063D and 5729) and dielectric (QM44) were used to print the thick film pattern on the substrate. Their properties were proved reliable at 300^{o}C [34]. The blank substrate was cleaned with methanol and then blown dried with N_2 before the printing process.

The screen mesh and emulsion thickness provide the main control of the print thickness. The parameters of the screens were: 325 mesh, 0.9mil wire with 0.5 emulsion. Before the printing of each layer, there was a test printing to adjust the squeegee speed and pressure in order to get the correct thickness. The proper thickness value was determined from the datasheet of each paste. A surface profiler was used to measure the thickness of each layer after drying.

Au thick film conductor (5729) was used to print the bottom layer on the substrate. 5729 has good wirebondability with Au wire and it has very low resistivity. This layer was used to provide wire bonding pads and interconnect. A firing profile with 850^{o}C peak temperature was used.

Two dielectric layers (dielectric paste QM44) were sequentially printed, dried, and fired to eliminate pinholes. A firing profile of 850^{o}C peak temperature was used.

The third layer was also 5729 thick film conductor which provided interconnects over the dielectric layer. A 850^{o}C firing profile was used.

The fourth layer used Pt/Pd/Au thick film conductor C6029 for die, moly tab and passive component attach pads. This layer was also dried at 150^{o}C and fired at 850^{o}C.

A layer of DuPont 5063 gold conductor was printed on the pad layer (C6029 conductor layer). The gold thickness on the die, moly tab and passive component pads was increased to provide excess Au for the liquid phase transient bonding process with the AuSn perform.

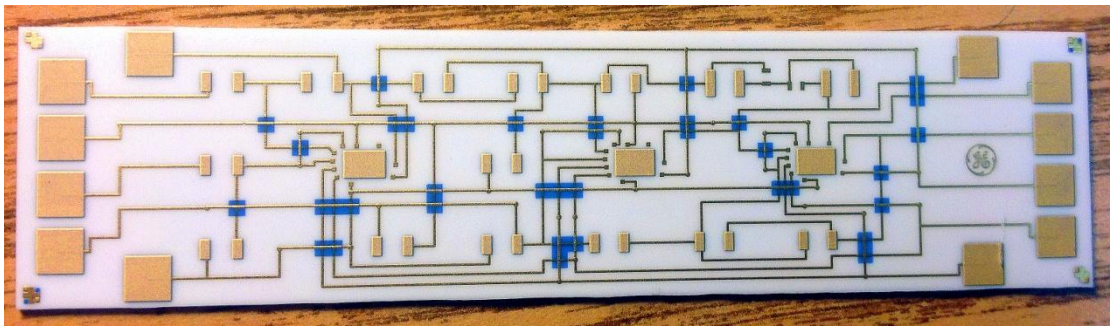


Figure 2.11 Thick Film Substrate before Assembly

2.6.1.2 Passive Components Attach

The FC150 thermal compression bonder was used for passive component and moly tab bonding. AuSn eutectic performs were used to attach the passive components and Moly tabs to the thick film pads. First, the moly tabs were attached to the substrate with a bonding profile of 330^{o}C for 2 minutes followed by 1 minute soak at 150^{o}C. 5kg bonding force was applied for 2 minutes during the bonding process.

Resistors were attached before capacitors since resistors have a lower height. The lower height created less interference with the placement of substrate components. The bonding profile was 2 minutes at 330^{o}C followed by 1 minute soak at 150^{o}C, with 2kg bonding force for resistors and 2.5kg bonding force for capacitors.

2.6.1.3 Die Attach and Wire Bonding

A graphite fixture was designed to hold the 4 x 1 in substrate in the SST 3150 vacuum furnace and to support the 500 grams dead weight on the SiC die. A special custom made collet was placed on the top of the SiC die in order to apply bonding force to the perimeter of the die without damaging the circuit on the front of the die. AuSn(80wt%Au/20wt.%Sn) performs were cut to small rectangular pieces which were approximately 1/3 of the die area. The SST profile for the die attach process was: peak temperature at 335^{o}C for 4 minutes, followed by the 20 minutes soak at 280C. After die attach, gold wire was used to wire bond the die to the substrate according to the wire bonding map. The assembled board (before wire bond) is shown as Figure 2.12.

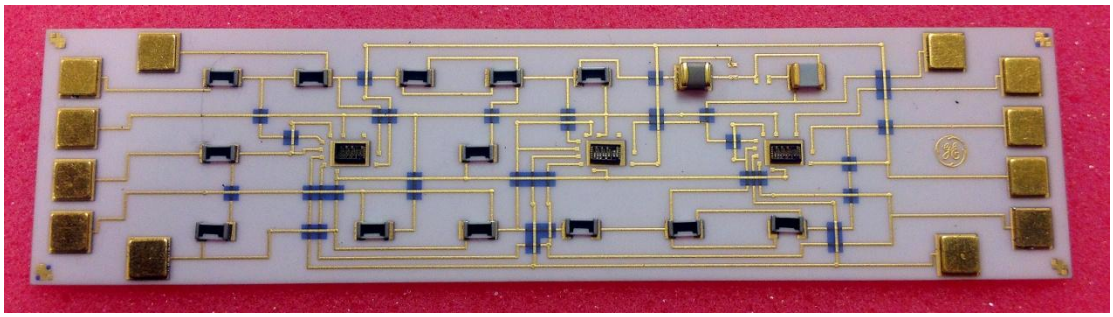


Figure 2.12 Assembled Test Board (Before Wire Bonding)

2.6.2 DIP Socket Test Board

Testing of SiC devices or prototype circuits for reliability at 300^{o}C requires that the test fixtures have better reliability. A prototype test fixture was fabricated using commercially

available BeNi contacts. The fabrication process and applications of the test board are presented below [35].

A test fixture was designed using the combined capability of Au thick film substrates and BeNi contacts. Materials and processes are commercial off-the-shelf (COTS). The design is illustrated in Figure 2.13.

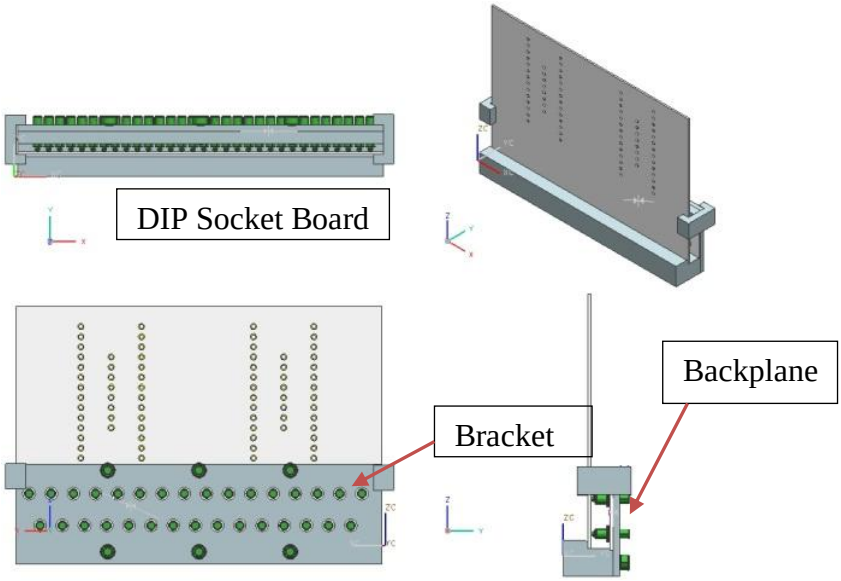


Figure 2.13 High Temperature DIP Socket Apparatus (Drawn by GE)

The Au thick film DIP socket board was fabricated with a 96% alumina, 25 mils thick substrate. The alumina substrate was laser drilled to accept the receptacles. The substrate was metalized with a combination of PtPdAu thick film conductor (C6029), Au thick film conductor (5729), pure Au thick film (5063) and thick film dielectric materials (QM44) selected from material testing reported in earlier publications at 300˚C [35]-[37]

The interconnect traces used thick film Au conductor since it has been shown to have good stability [38]. A firing profile with a 850˚C peak temperature was used. The receptacle and spring contact annular rings used PtPdAu thick film conductor plus an addition layer of pure

gold conductor printed on top of this to increases the Au thickness for the LPT bonding process with the AuSn performs. Two dielectric layers with dielectric paste were sequentially printed around the pad area to provide a solder mask. Figure 2.14 is the thick film substrate before connector assembly.

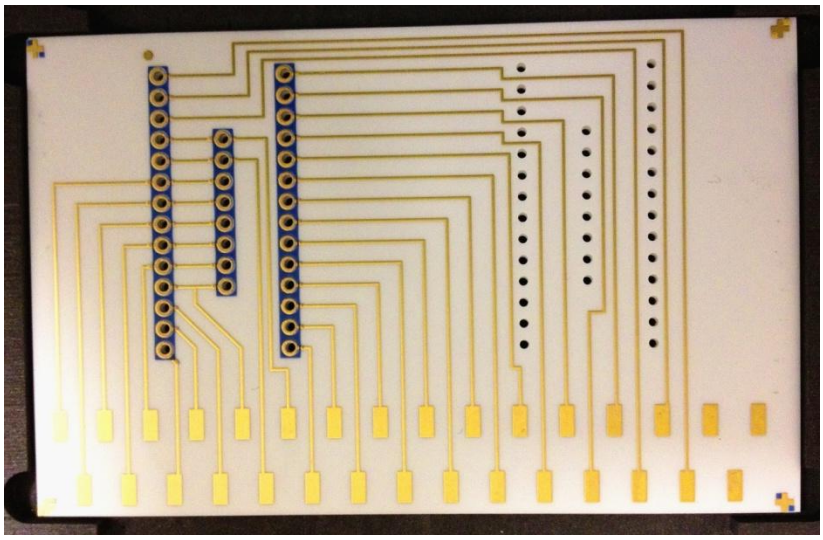


Figure 2.14 Printed DIP Socket Thick Film Substrate

AuSn (80wt%Au/20wt%Sn) washers were made for connection of the Au finished receptacles. A graphite fixture was designed to hold the substrate in the SST 3150 vacuum furnace and to support deadweight on the receptacles. Three weights of 500 grams were applied using a bare ceramic substrate to distribute bonding force to each connector.

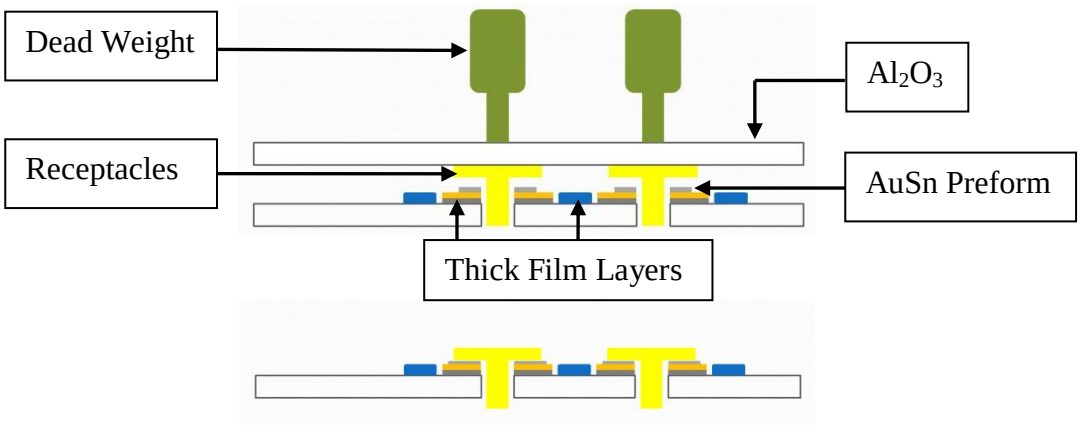


Figure 2.15 Receptacle Attach Process

The receptacle attach process is shown in 2.15. The reflow process was 4 minutes at 330˚C followed by 20 minutes soak at 280˚C. The finished assembly is shown in Figure 3.16. The assembly with an inserted DIP package is shown in Figure 2.17.

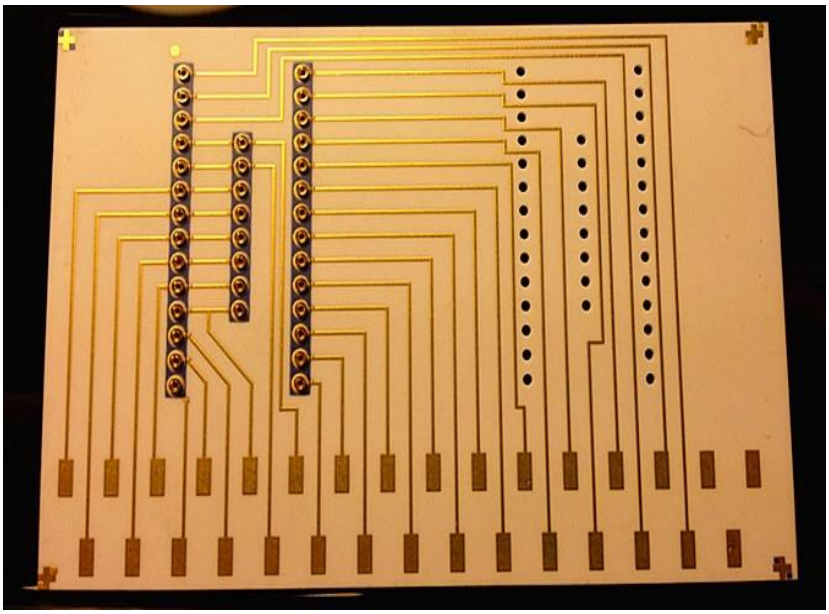


Figure 2.16 Assembled DIP Socket Board

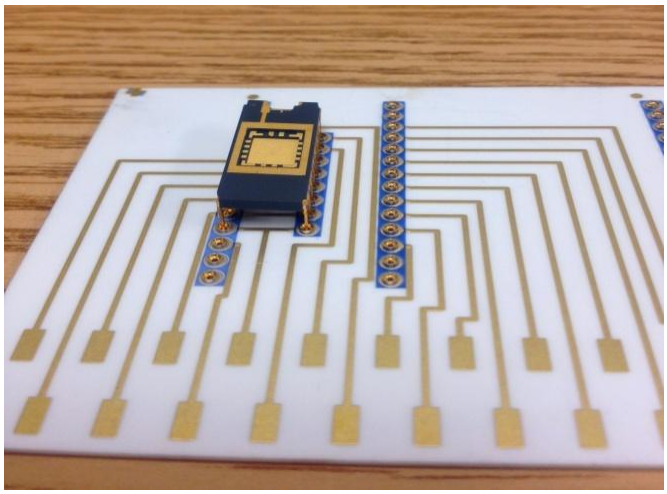


Figure 2.17 Assembled DIP Socket Board with Inserted DIP Package

The backplane board was fabricated in a similar manner. The board is shown in Figure 2.18. The alumina substrate was laser drilled with holes to accept the spring contacts. Thick film pads provide the attach pattern for the spring loaded contacts. PtPdAu was printed, dried and fired as the first layer followed by an additional layer of pure gold printed on the top for AuSn LPT assembly.

AuSn eutectic alloy was used to attach the spring loaded contacts to the thick film pads in the SST vacuum furnace. A special SST clamp fixture was made to apply force during the reflow process. The reflow profile was the same as the profile for the socket board.

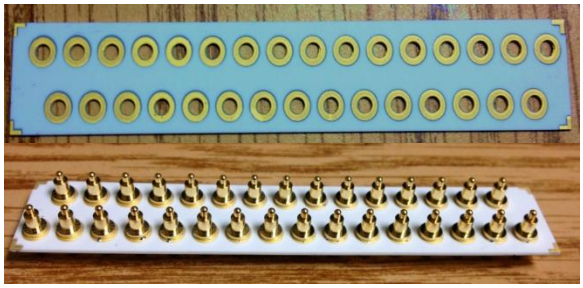


Figure 2.18 Backplane Board Substrate (Upper) and Assembled Back Plane Board (Lower)

The assembled boards were sent to GE Global Research Center for reliability testing. The DIP socket board was tested by making a daisy chain within a side brazed ceramic DIP and wire bonding traces on the socket board so that the resistance could be measured through multiple receptacles. The board was placed into a furnace at 300˚C and the daisy chain resistance was monitored at intervals using an Agilent 34970 data logger. The resistance remained steady for over 3000 hours, which indicates the fixture used AuSn LPT bonding can provided reliable conductivity [39].

2.7 Summery

Liquid phase transient bonding with AuSn preform is a reliable die attach method for high temperature applications up to 500^{o}C. Die attach with a AuSn preform and excess Au provided by the die and substrate metallization shows good mechanical reliability for high temperature applications. Both single and double prints of the PtPdAu thick film layers were evaluated. The shear test results after 2000 hours aging at 500^{o}C shows there is no significant difference between the single and double prints. Assembly processes for two test circuit boards using AuSn LPT bonding techniques for 300^{o}C application were developed. The DIP socket board had contact stability beyond 3000 hours.

CHAPTER 3 DIE ATTACH USING MICRO-SCALE PARTICAL Au SINTERING

3.1 Introduction

Traditional solders and eutectics will melt or become soft at lower temperatures which make them not suitable for high temperature operation. This lead to the exploration of using the interconnect metallization as a die attach material. The principle of the attach technique is based on the sinter process.

Jay S. Salmon et.al has evaluated circuit assembly using high temperature thick film conductor inks [40]. The evaluated processes include die attach, wire bonding, and passive component bonding on the ceramic substrate. The samples were aged at 500^{o}C. The experiment confirmed the operation of a SiC based circuit at 300^{o}C, and also proved the plausibility of future circuits operating in the 500^{o}C range. The paper also mentioned that the burn out gas from the conductor ink created voids/gaps under the die, resulting in the degradation of the shear strength in the aging test.

To address the voiding issue caused by the burn out gas during the firing process, a patterned die and die attach were designed. The patterns help volatile organics from the Au paste to escape during the firing process. The details are presented in the die attach process section.

3.2 Sintering Process

Sinter is a method for creating objects from powders. It is based on atomic diffusion. In most sintering processes, the powdered material is held in a mold and then heated to a temperature below the melting point. The atoms in the micro-scale particles diffuse across the

boundaries of the particles, fusing the particles together and creating one solid piece, illustrated in Figure 3.1.

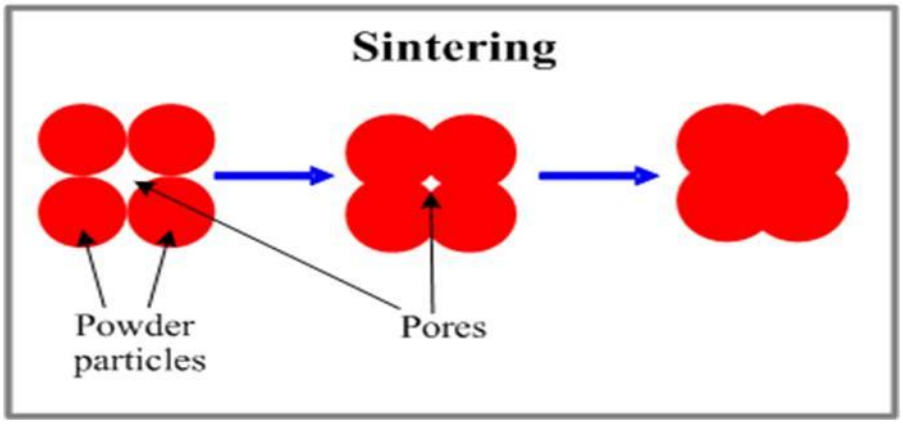


Figure 3.1 Sintering Process [41]

A sintered Au die attach was investigated. Since the die attach joint is just pure gold after sintering, the high electrical and thermal conductivity, and high melting point of gold can provide low electrical and thermal resistance and high temperature capable die attach.

3.3 Micro-scale Particle Gold Paste

DuPont gold conductor paste (5771) was chosen as the die attach material for the 500^{o}C aging test. Gold is a stable metal and has a very high melting temperature, which makes it a suitable material for high temperature application. The paste is screen printable and is widely used as a gold wire bondable conductor. Pull testing was done in the previous publication [42] to prove good adhesion of the paste to the alumina substrate.

3.4 Die Attach Process Using Micro-scale Particles Au Paste

SiC die with Ti/Ti:W/Au thin film metallization was used as the test die in the test vehicle. As described in the previous chapter, a three inch SiC wafer was fully cleaned using the

RCA cleaning process prior to thin film deposition. The thin film stack consisted of Ti/Ti:W/Au(8nm/62nm/100nm), Ti and Au were deposited by e-beam evaporation, and Ti:W was sputtered on the backside of the SiC. Then an array of 5um-6um height gold bumps (8um×8um in size) was electroplated on top of the thin film stack, as shown in Figure 3.2. Then the wafer was sawn into 5mm x 5mm die for assembly.

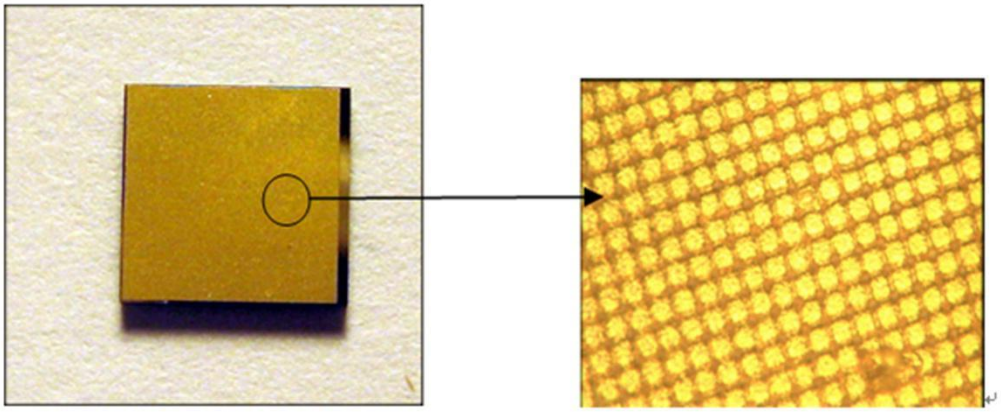


Figure 3.2 Image of Pattern Au Plating on SiC Die Backside

The alumina test substrate was metalized with PtPdAu thick film conductor. The DuPont 5771 paste was screen printed onto the metalized substrate pads in a line pattern (Figure 3.3). The pattern consists of 10 lines of 10mil×200mil rectangular. The line pattern was used to facilitate the escape of volatile organics from the Au paste during firing. The line pattern was double printed. The first printed layer was dried at 150^{o}C, followed by the second printed gold conductor paste. The second print was left wet. The die attach layer was approximately 20μm tall and strong enough to provide a uniform attach during the bonding process. An FC150 thermal compression bonder was used to place the die. The placement profile was 2Kg force for 2 minutes at room temperature. The assembly was 'fired' at 500^{o}C to sinter the Au paste.

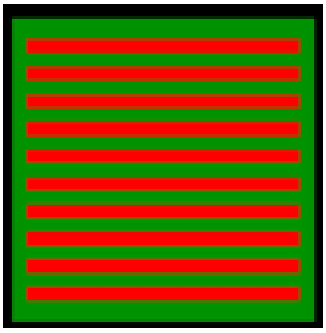


Figure 3.3 Illustration of Thick Film Au Die Attach Line Pattern Printed on the Die Attach Pad

3.5 High Temperature Storage Test

Test vehicles were assembled and placed in the oven for the 500^{o}C storage test. Shear tests were performed to evaluate the mechanical reliability at each time interval. A Dage 2400PC shear tester with a 100kg load cartridge was used to shear the samples. The die shear strength (shear force in kg divided by attach pattern area in mm^2) as a function of storage time at 500^{o}C is shown in Figure. 3.4. While the die shear strength is not as high with this process as with the AuSn LPT bonding, the shear strength increased with aging time through the first 500 hours and significantly exceeded the MIL-STD-883 requirement at all test times. The reduced bond area due to the line pattern can account for some of the reduced die shear strength. As the die attach is Au, this die attach approach has the potential for use to 750^{o}C and higher.

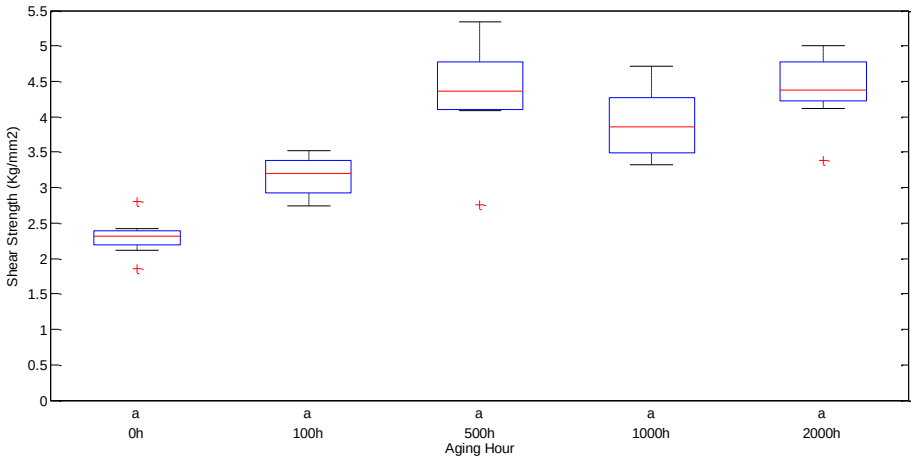


Figure 3.4. Die Shear Strength of Patterned Au Die Attach as a Function of Aging at 500^{o}C.

3.6 Summery

The patterned gold die attach technology using micro-scale gold paste has been evaluated and shows the potential for applications at 500^{o}C. The patterns on both thin film die and thick film substrate allows the burn out gas to escape during the firing process. The aging test results indicate after high temperature storage, the shear force with micro-scale Au die attach increased 90.41% compared to the initial shear force. Continued sintering of the Au atoms increased the strength of bonding during the 500^{o}C storage. While the die shear strength of the micro-scale particle Au die attach was less than with the AuSn LPT, it meets the MIL-STD-883 die attach requirement and should be stable for use to at 500^{o}C or higher.

CHAPTER 4 DIE ATTACH USING AgBiX SOLDER PASTE

4.1 Introduction

A AgBiX solder paste (AgBiX®, Indium Corporation) has been developed to provide a higher temperature, lead-free solder alternative [43-44]. During the soldering process, formation of an intermetallic at the interfaces assists wetting. In the AgBiX alloy, it is the 'X' component that forms the initial intermetallic. By limiting the amount of X, the amount of X-based intermetallic formed initially and with high temperature aging can be limited. In the case of SAC alloys, the Sn forms an intermetallic with Cu (Cu_6Sn_5 and Cu_3Sn), Ni (Ni_3Sn), Ag (Ag_3Sn) and Au ($AuSn_4$). Sn is a major component of SAC alloys and provides a readily available supply of Sn for the continued growth of Sn intermetallics (Cu_6Sn_5 and Cu_3Sn or Ni_3Sn) during operation at high temperature. Note that continued intermetallic growth can be detrimental to solder joint reliability.

This work examines the processing and reliability of the AgBiX solder paste for assembly of SiC die to multiple substrate materials. High temperature storage (200^{o}C) and thermal cycling (-55^{o}C to +195^{o}C) were used for reliability testing. Elemental analysis of cross sections and fracture surfaces after die shear along with micro X-ray diffraction of intermetallics were performed to assist in determination of failure mechanisms.

4.2 Solder Paste Characterization

The mixed alloy powder solder paste technology was invented to efficiently improve the interfacial reaction chemistry by Indium Corporation. The AgBiX solder paste is composed of the primary solder powder and the additive solder powder in the minority[46]. During the reflow process, the additive solder powder will react aggressively with various surface finish

materials, such as Cu, Ag, Ni, Au etc. When soldering, the additive solder powder will melt earlier than, or together with the primary solder powder, spread and react with the surface finish materials. In this process, the formation of the IMC layer is dominated by the additive solder in the solder paste. And the active elements in the additive solder will be completely converted into IMCs, including both the interfacial IMC layer and the IMC precipitates in the joint matrix. The non-active constituents will melt into the molten primary solder and solidified together to form a homogeneous solder joint [47].

4.2.1 Potential Intermetallic Formation

There are different elements from both the die side and the substrate side that might form intermetallics with Bi, Ag or Sn in the solder paste. Metallurgical phase diagram display the solubility limits of one metal into another, the melting temperature for metals and their alloys, and the intermetallics that can form. Phase diagrams are for equilibrium conditions and do not contain information about the rate of intermetallic formation, ie. rate kinetics. In the solder, there are Bi and Ag, and in the previous paper [47], we know that Sn is at least one element of the X. As shown in Figure 4.1 [48], Ag and Bi do not form intermetallics. There is negligible solubility of Ag in Bi and only slight solubility of Bi in Ag below 200^{o}C. Bi and Sn, also do not form intermetallics as shown in Figure 4.2 [49].

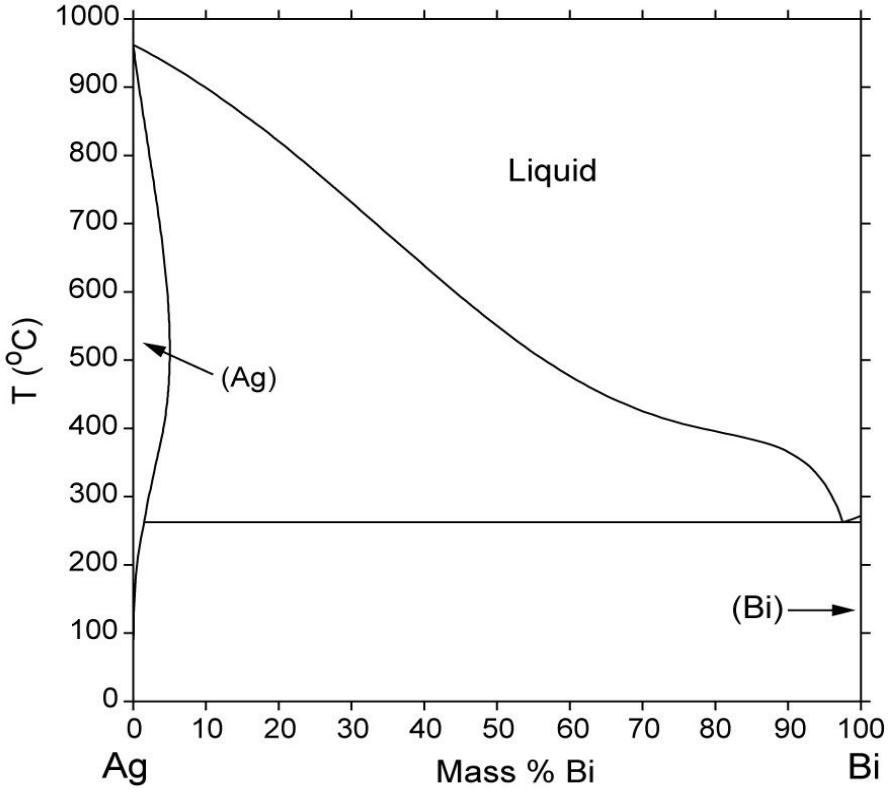


Figure 4.1 Ag-Bi Phase Diagram[48]

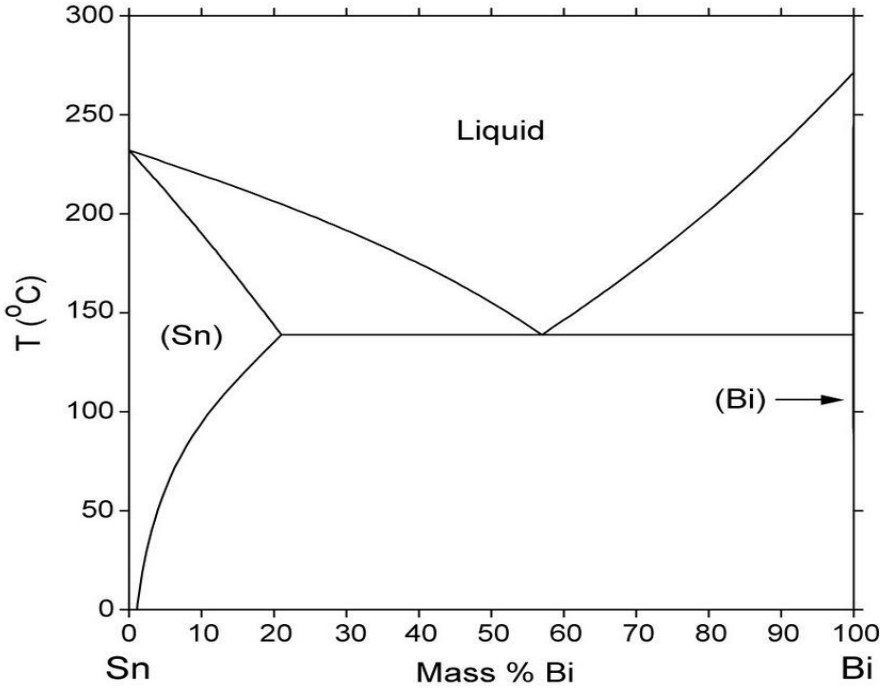


Figure 4.2 Sn-Bi Phase Diagram [49]

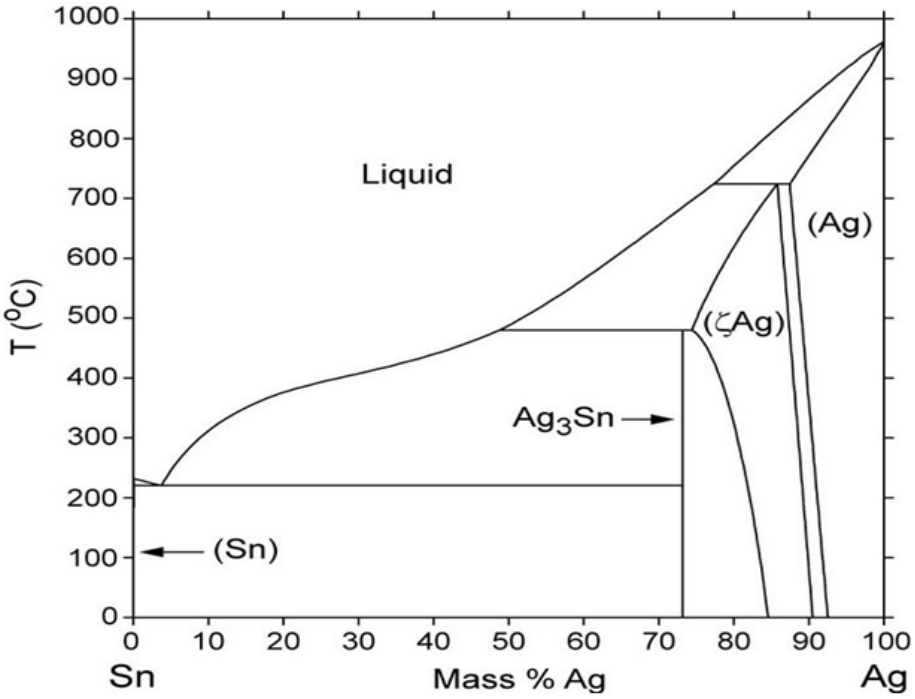


Figure 4.3 Sn-Ag Phase Diagram [50]

There is Sn and Ag in the solder, so there is a potential interaction of Sn and Ag. As shown in the phase diagram (Figure 4.3), there might be Ag_3Sn intermetallic formation, there is high solubility of Sn in Ag and a ζ phase with ~13 at% Sn.

From the die, there is Ni from the thin film layer on the SiC. And from the substrate side, there's Ni under Au, so this Ni may interact with Sn and Bi from the solder, to form Ni-Sn intermetallics and Bi-Ni intermetallics in the solder. As shown in Figure 4.4 and Figure 4.5.

From the substrate side, there is Cu in the DBC substrate. In the phase diagram of Bi-Cu, there is no intermetallic formation. In the phase diagram of Ag-Cu, it is shown that Ag and Cu didn't form any intermetallics.

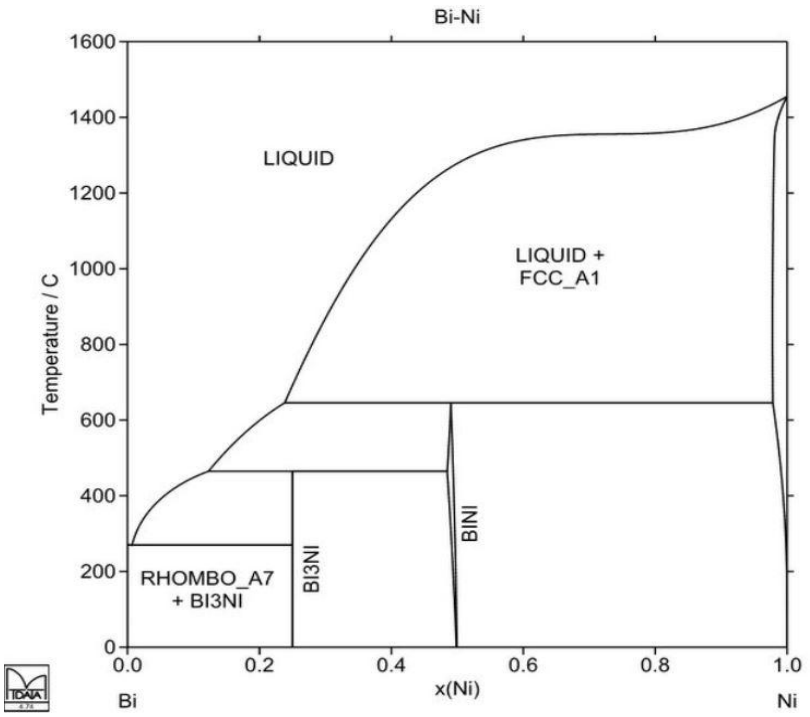


Figure 4.4 Bi-Ni Phase Diagram[51]

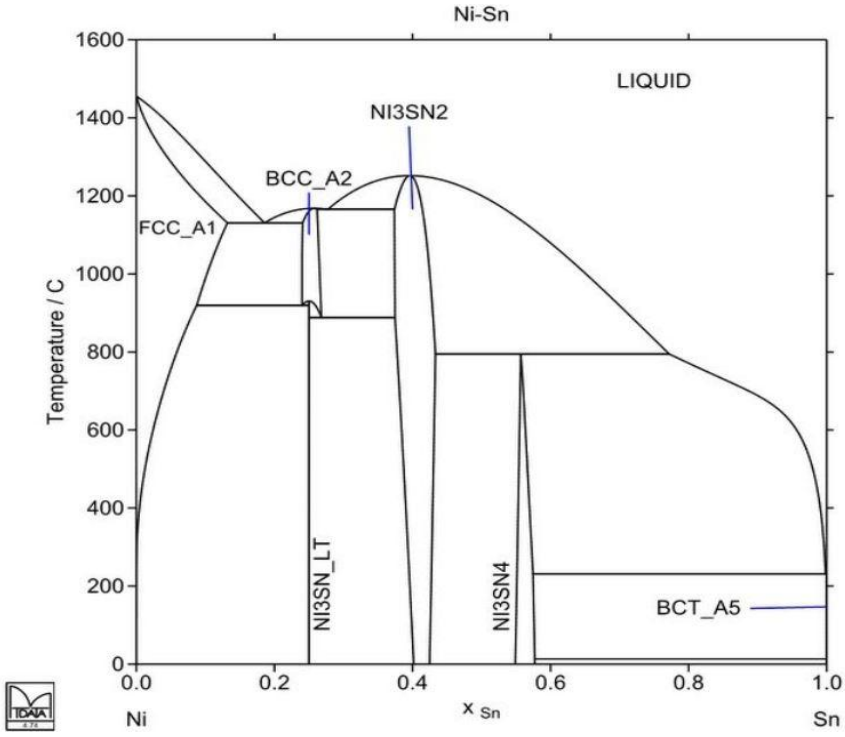


Figure 4.5 Ni-Sn Phase Diagram [52]

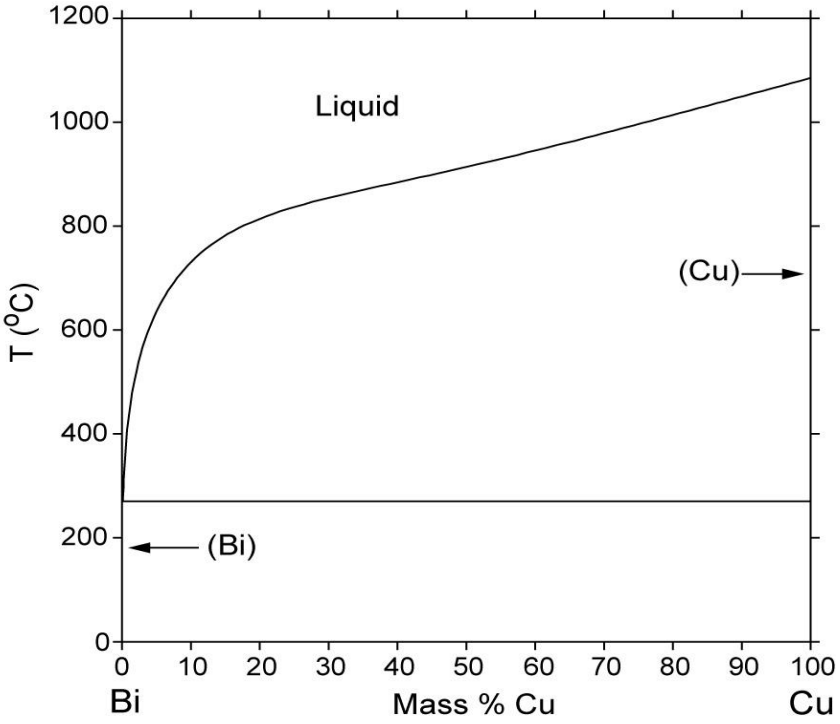


Figure 4.6 Bi-Cu Phase Diagram [53]

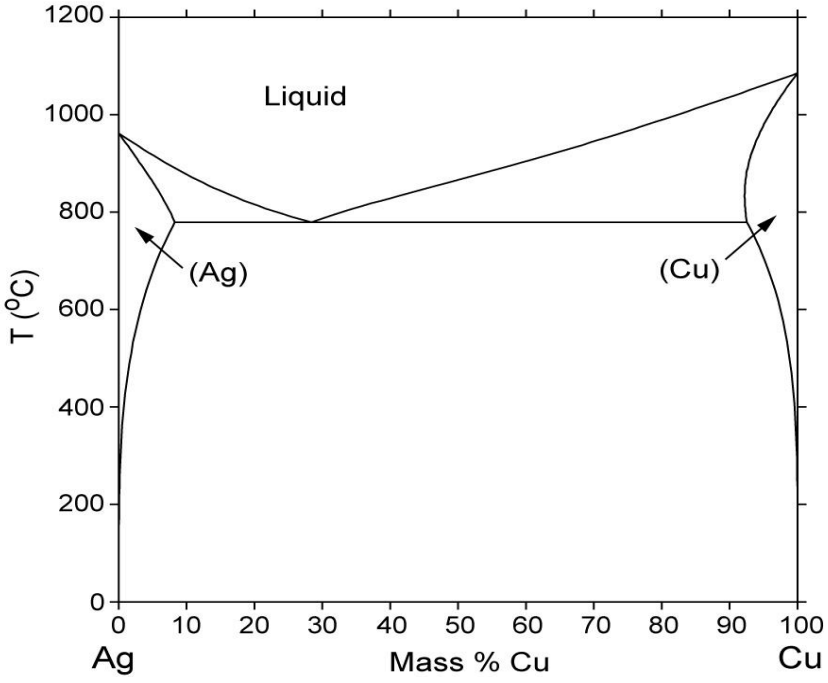


Figure 4.7 Ag-Cu Phase Diagram [54]

For solder and PdAg thick film substrate, the Pd from the substrate may react with Bi and Sn from the solder (Figure 4.8 and Figure 4.9). So there is a potential of forming the intermetallic compound of Bi_xPd_y and Pd_xSn_y. The eutectic temperature of Bi and Bi_2Pd is 256^oC.

For die attach on Au thick film substrate, the Bi from the solder may react with Au from the substrate. As shown in the Figure4.10, the eutectic temperature of Au-Bi is 241^oC. In Figure 4.11, the phase diagram of Pt-Sn shows the possible intermetallic formation of Pt_xSn_y.

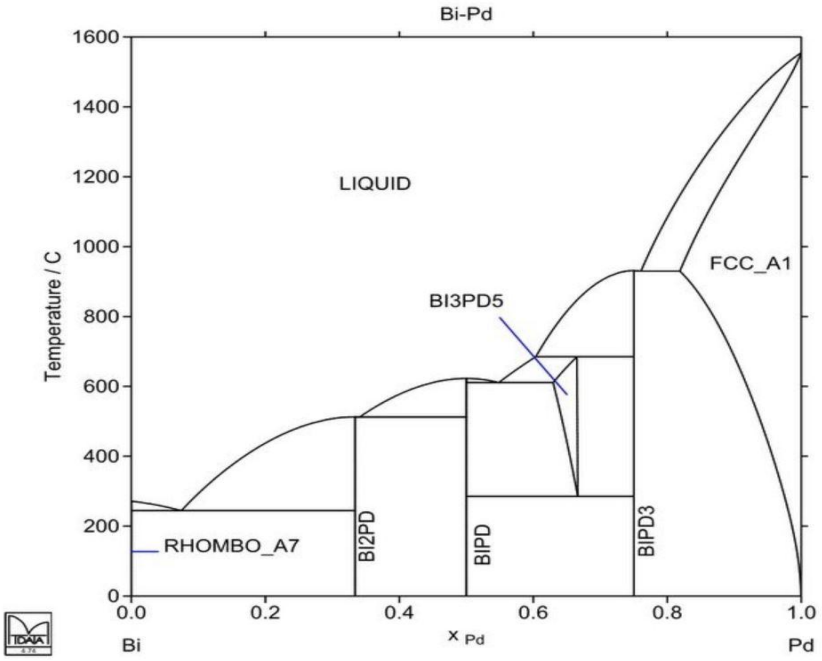


Figure 4.8 Bi-Pd Phase Diagram [55]

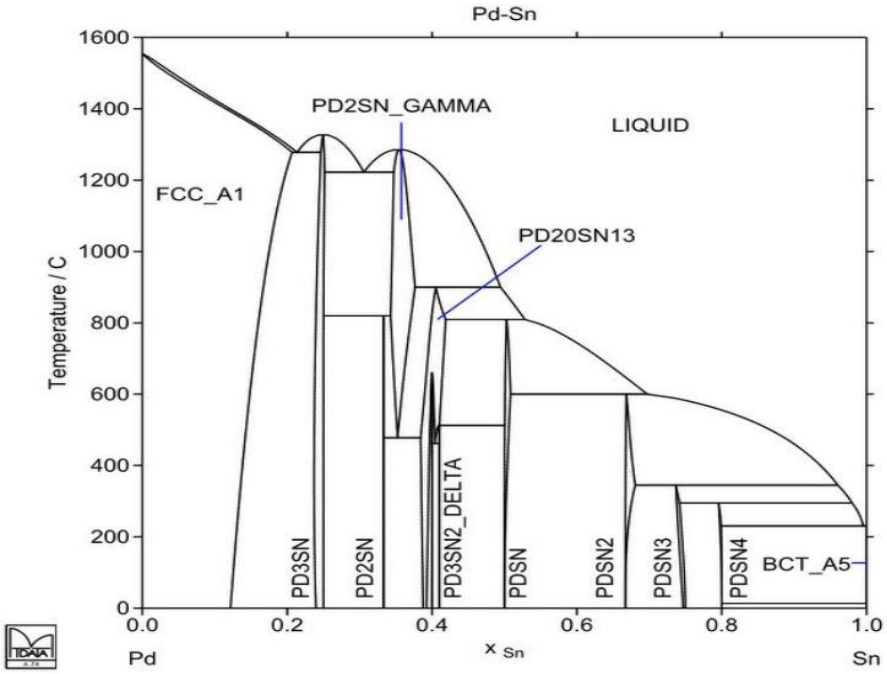


Figure 4.9 Pd-Sn Phase Diagram [56]

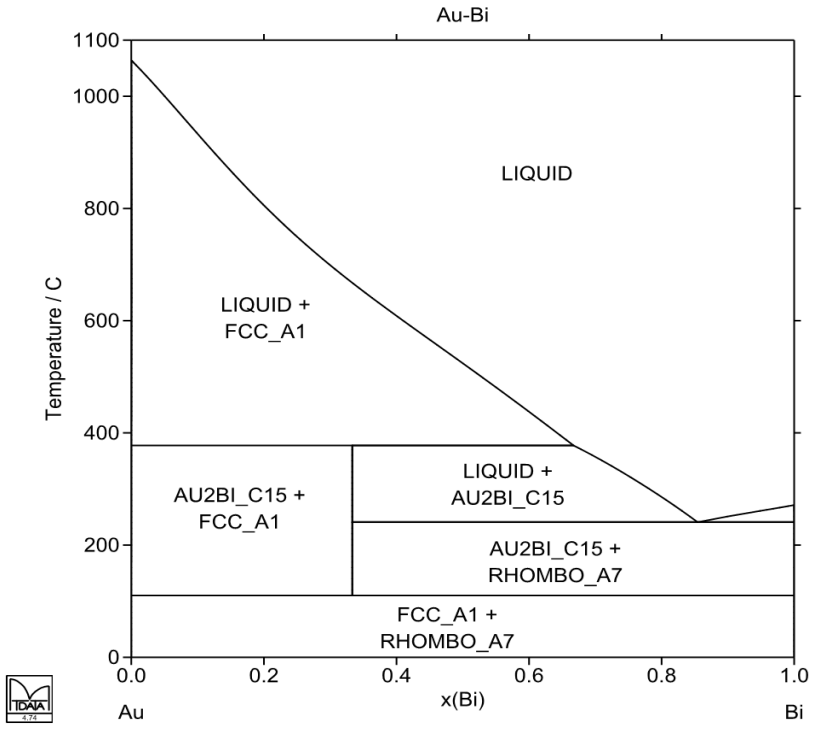


Figure 4.10 Au-Bi Phase Diagram [57]

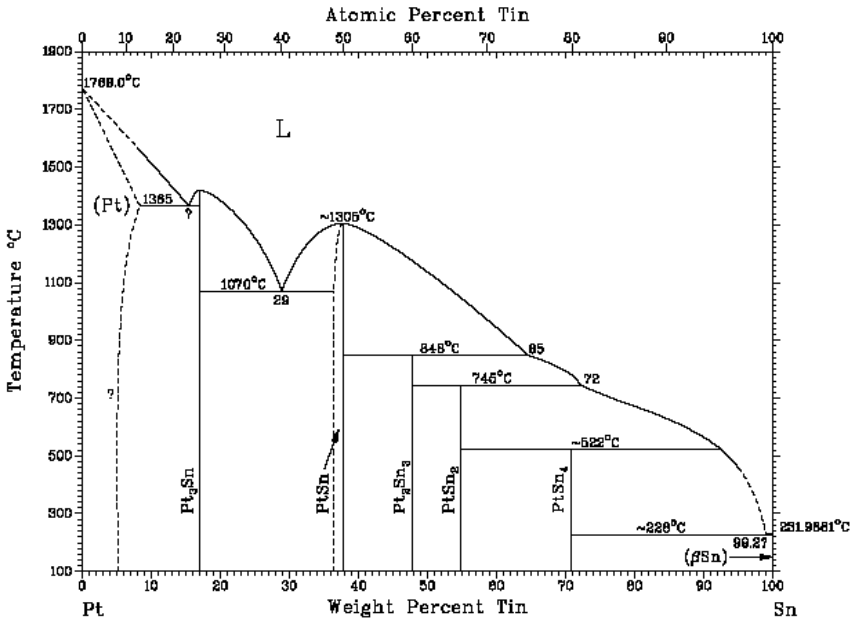


Figure 4.11 Pt-Sn Phase Diagram [57]

4.2.2 Differential Scanning Calorimeter (DSC) on Different Substrate

A differential scanning calorimeter (DSC) measurement of the unreflowed AgBiX solder paste on Ni/Au finish DBC substrate run in nitrogen is shown in Figure 4.12. The scan rate was 10^{o}C/min and was performed in N_2 atmosphere. The endotherm at ~141^{o}C corresponds to the Sn-Bi eutectic. As will be shown later, Sn is at least one component of "X" in AgBiX. The second endotherm at ~265^{o}C corresponds to the Bi-Ag eutectic. The AgBiX solder paste is Ag-rich compared to the AgBi eutectic composition and thus has a pasty range. Masayoshi, et. al. [58] has shown higher tensile strength and higher tensile elongation for Bi-Ag with higher Ag (11% vs 2.5%) concentrations.

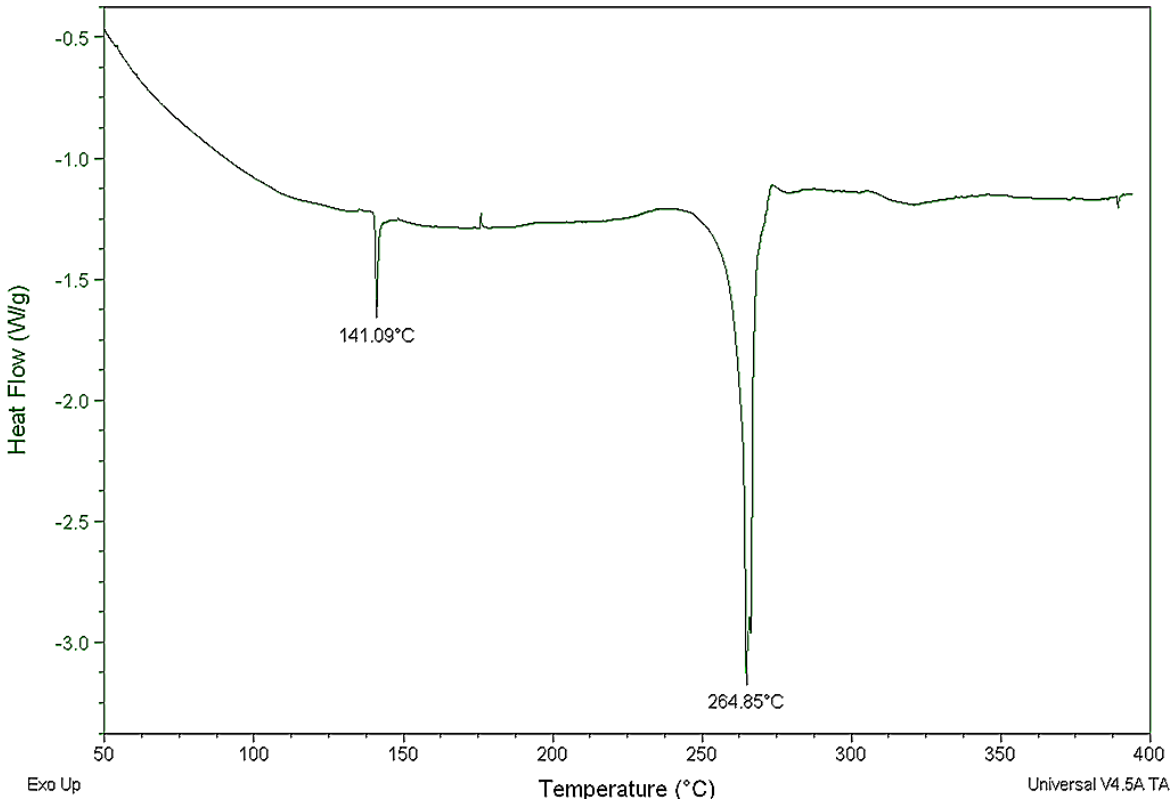


Figure 4.12 Differential Scanning Calorimeter Scan of Unreflowed AgBiX Solder Paste on Au Finish DBC Substrate

Figure 4.13 is a DSC measurement of a AgBiX sample after solder reflow on a Ni/Au finish DBC substrate. The scan rate was 10^{o}C/min. in nitrogen. The low temperature peak observed in Figure 4.12 at 141^{o}C is not present after reflow. The absence of this endotherm indicates that the Sn was consumed into intermetallic compounds (Ag-Sn, Ni-Sn) during solder reflow processing.

Similar DSC results were obtained for silver plated DBC, Ni/Au finish CuMo substrate and thick film Ag substrates.

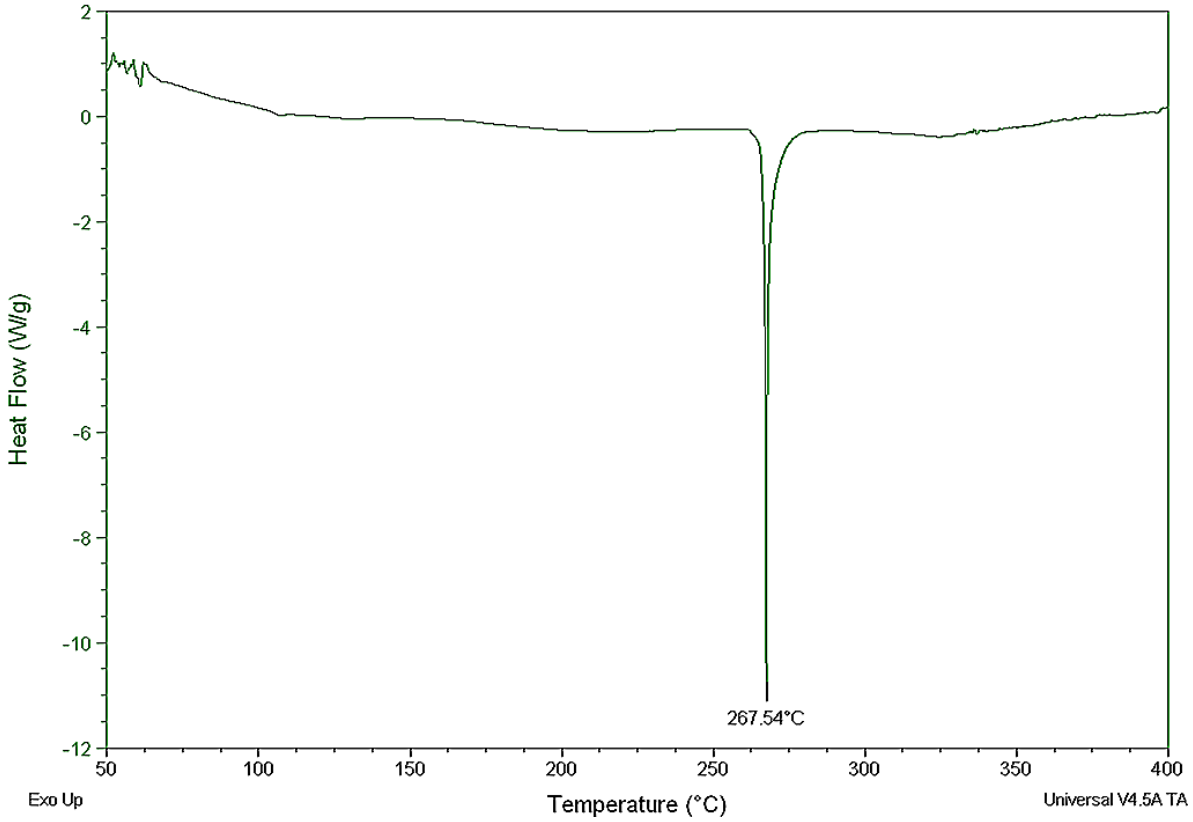


Figure 4.13 Differential Scanning Calorimeter Scan of Reflowed AgBiX Solder Paste on Ni/Au Finish DBC Substrate

Figure 4.14 is the DSC profile of an unreflowed solder sample on a thick film PdAg substrate. The scan was performed in a nitrogen atmosphere. Besides the endotherm of Sn-Bi eutectic and BiAg eutectic, the dip at 255^{o}C approximately corresponds to the Bi-Pd eutectic.

Figure 4.15 is the DSC plot of AgBiX solder after reflow on a PdAg metalized sample. The endotherm at 139^{o}C disappears, indicating that the Sn was consumed into intermetallic compounds during the reflow process. The endotherms at 250^{o}C and 257^{o}C remain due to the continued presence of the Bi-Ag and Bi-Pd eutectics.

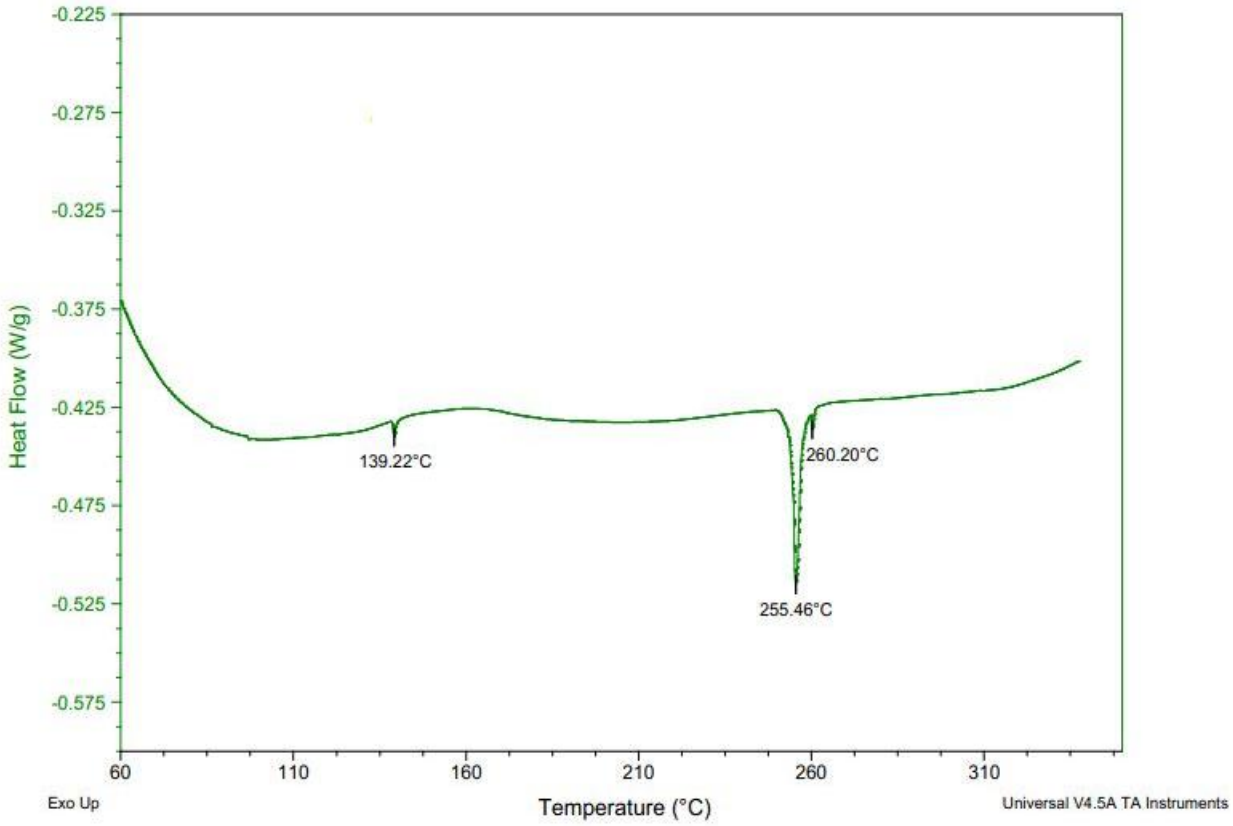


Figure 4.14 Differential Scanning Calorimeter Scan of Unreflowed AgBiX Solder Paste on PdAg Thick Film Substrate

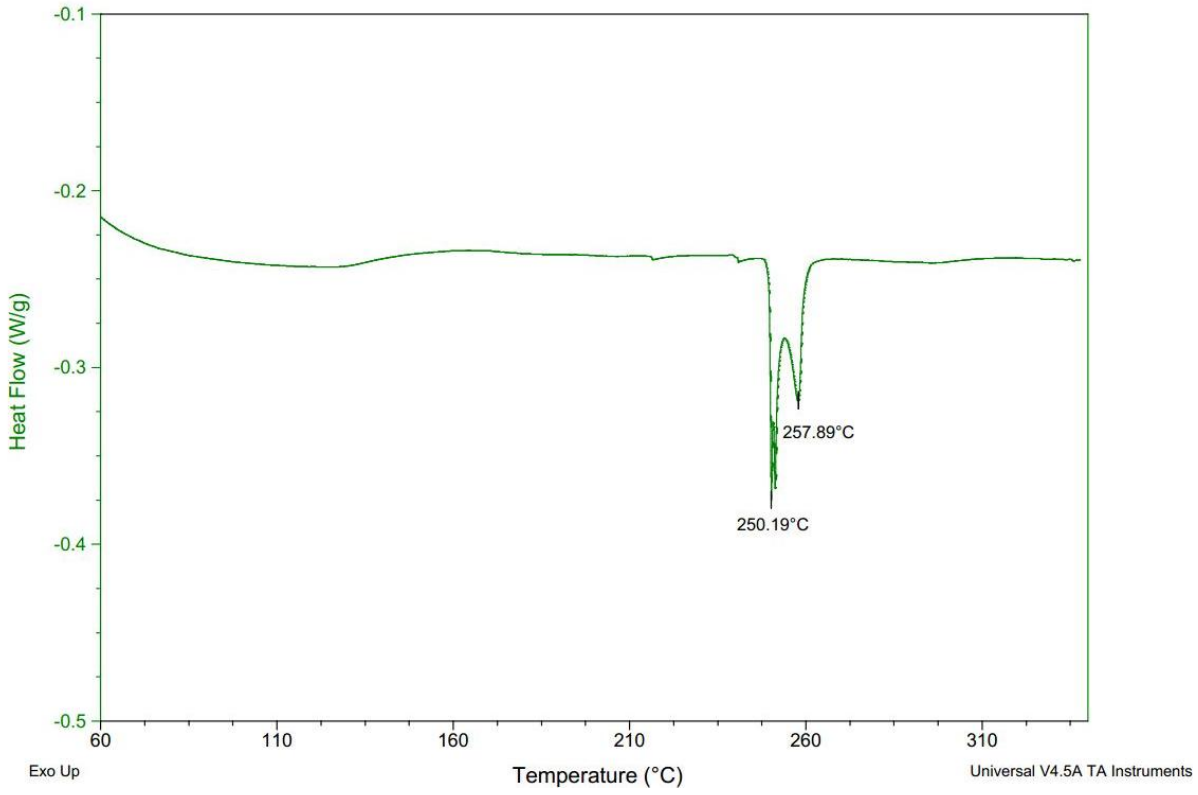


Figure 4.15 Differential Scanning Calorimeter Scan of Reflowed AgBiX Solder Paste on PdAg Thick Film Substrate

4.3 Test Die and Resistor

Test die were fabricated using SiC wafers. After the full cleaning process (described in Chapter 2), backside metallization was vacuum deposited on the carbon face of the wafer. The backside metallization of the SiC die was Ti/Ni/Ag and the deposition process was: 2 minutes of ion milling, 500A of Ti by e-beam evaporation, 1000A of Ni by sputtering and finally 500A of Ag by e-beam evaporation. The wafers were sawn into 2 mm x 2mm and 5 mm x 5 mm die. The 2 mm x 2 mm die were used for high temperature aging studies. To increase the die-to-substrate stresses in thermal cycling, 5 mm x 5 mm die were used for the thermal cycle test vehicles.

The SMT resistors used in the experiments were manufactured by KOA Speer Electronics (Part number: RK73B2BTTD1R0J). The resistors were Sn terminated and the size was 1206.

4.4 Test Substrates

The solder alloy was used to assemble SiC test die to ceramic substrates with direct bond copper (DBC), reactive brazed CuMo, thick film PtPdAu, thick film PdAg and thick film Ag. Surface mount chip resistors have also been attached to thick film metallized substrates.

Direct bond copper (DBC) substrates (5.08cm x 5.08cm) plated with 1.8 μm of Ni:B (sintered) and 0.17μm of Au were used for high temperature (200^{o}C) storage tests. Sintering of the Ni:B improves the adhesion of the plating. For thermal cycling, reactive brazed CuMo-on-Al_2O_3 substrates were used. This construction has previously been described in [58] for power modules with improved thermal cycle reliability. The CuMo (0.5mm thick) was plated with 4.1μm of Ni:B (sintered) and 0.7μm of Au. As shown in Figure4.16, the substrate was 7.225 cm x 8.66 cm.

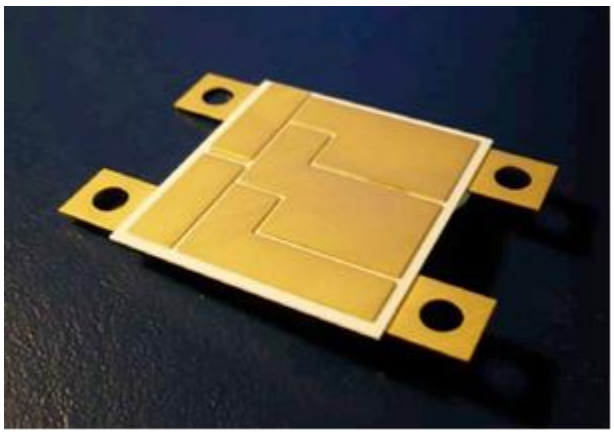


Figure 4.16 CuMo-on-Al_2O_3

DBC alumina substrates with Ag finish were also use for assembly. The substrates were 5.08cm x 5.08cm in size. The alumina was 0.625mm thick and the Cu was 0.203mm thick on both sides of the alumina. The Cu was plated with a 0.23mm (mean thickness) of Ag for the aging test substrates and 0.47mm (mean thickness) of Ag for the thermal cycle test substrates. The substrates were processed at different times, but to the same Ag thickness specification. The difference in Ag thickness was due to supplier process variation. Ag was selected as a solderable surface finish and to provide protection of the Cu from oxidation during reliability testing.

Thick film substrates were fabricated for die and resistor attach process development, high temperature storage tests and thermal cycle tests. Alumina substrates (5.08cm x 5.08cm) were printed and fired at 850^{o}C. Substrates were fabricated with PdAg, Ag, Au and PtPdAu thick film conductors. An additional group of substrates were printed and fired with a layer of PtPdAu, then overprinted and fired with a layer of pure (no binder system) Au.

4.5 Assembly Process

The die attach process was developed on the DBC and CuMo-on-Al_2O_3 substrates first. The AgBiX paste was stencil printed with a 0.127 mm thick stencil. The dies were placed with a Palomar Model 3500 automated placement system. For reflow, a PEO 601 quartz furnace was used for reflow. Bi has a melting point of 271^{o}C and Ag-Bi has a eutectic melting point of 262^{o}C. For assembly of the 2 mm x 2 mm SiC die on the DBC substrate, a 3-minute ramp profile to 320^{o}C was used. The location of the PEO 601 control thermocouple was in the substrate holder plate, so the peak temperature of the profile was not the actual temperature of the solder joint. In order to provide a pure nitrogen environment in the chamber, a 3 minute-purging was done prior to initiation of the reflow heat cycle.

After the reflow, non-destructive inspection was done first to check the wetting and voiding percentage. As shown in Figure.4.17, we can see there's no Au substrate exposed in the solder area, which means this solder wets well on the substrate. But from Figure.4.18, there's a black region on the solder surface after reflow and the perimeter of the die, they are the sign of oxidation during reflow.

The oxidation issue is due to the purity of N_2. We initially use the N_2 system in the lab for the reflow. It is not high purity nitrogen and may contain oxygen. The X-ray image shows the voiding is high (Figure 4.19). The voiding is primarily from the volatile flux. Solder oxidation before die attach will also increase the solder void percentage.

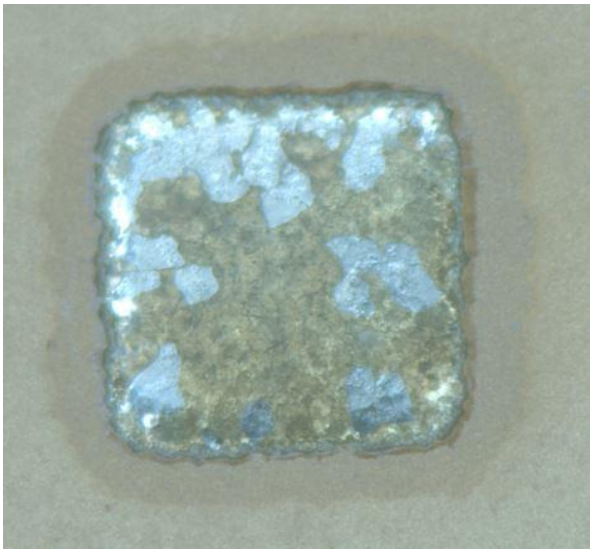


Figure 4.17 Solder without Die after Reflow Process

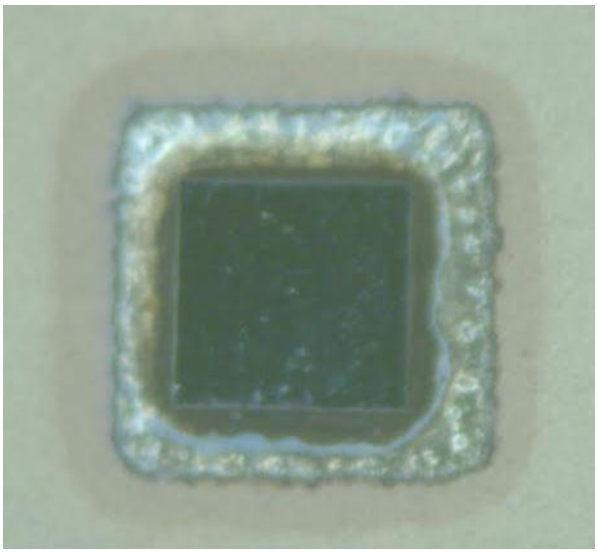


Figure 4.18 Solder with Die after Reflow Process

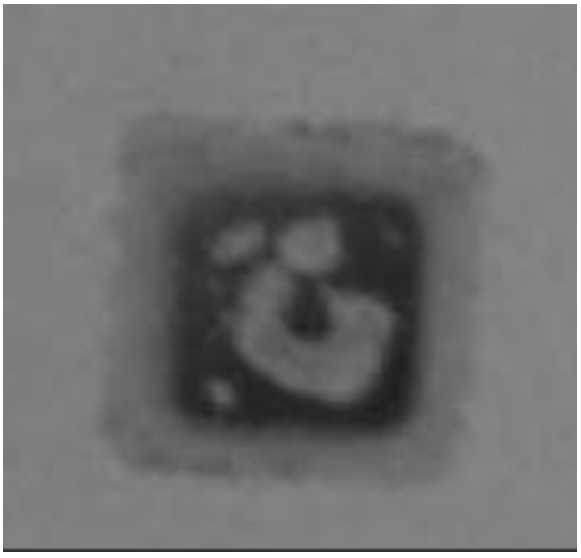


Figure 4.19 X-ray Inspection on the Die Attach on Au DBC Substrate

For the oxidation issue, we need to provide a high purity nitrogen environment. Thus instead of using the nitrogen system from our lab, the nitrogen source was changed to liquid N_2 tank. The purging time was also increased to assure the chamber was full of nitrogen.

The stencil aperture was designed to 92% of the die area to reduce the amount of solder applied on the substrate, so that we won't have excess flux. The assembly process was optimized through a series of assembly experience using voiding percentage as the criteria.

Figure 4.20 shows the optimized reflow profile for the DBC substrates. A six-minute purge was done prior to reflow to force oxygen from the chamber. The reflow profile was measured by a thin thermocouple attached on the test substrate. For the thermal cycle test vehicle assembly, the peak controller temperature was increased to 340^{o}C due to the significant thermal mass of the substrates.

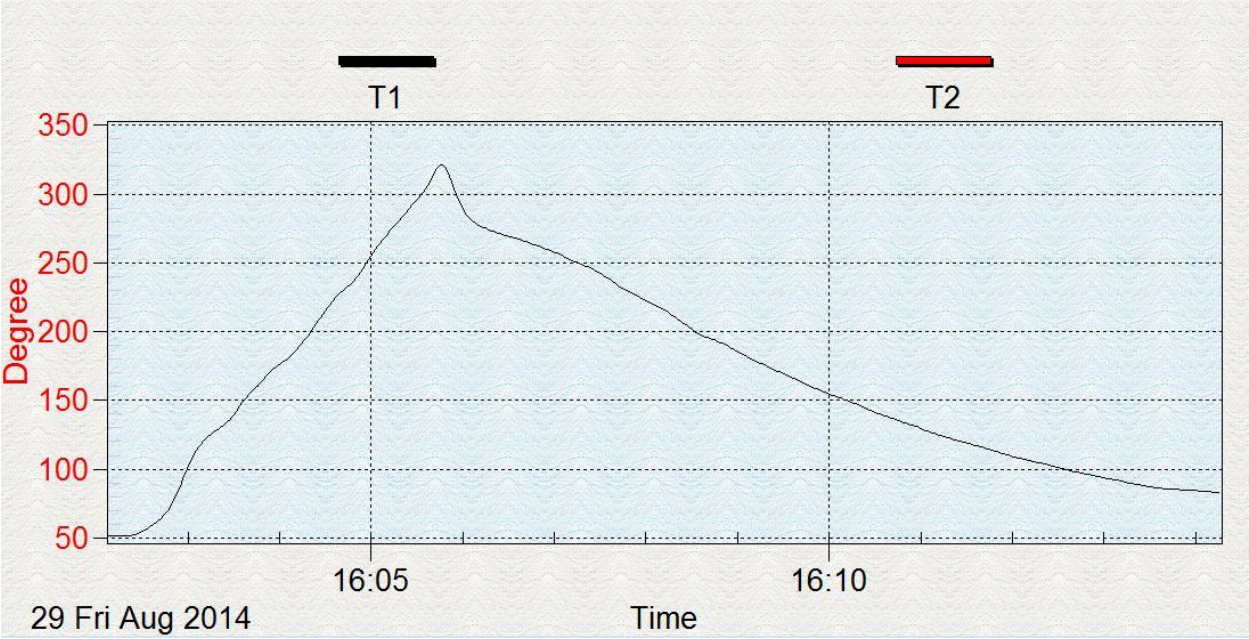


Figure 4.20 Reflow Profile for Measured on the Substrate

After process optimization, the inspection results are shown in Figures 4.21-4.23. From Figure 4.21, we can see the surface of the solder is clean and shiny. Figure 4.22 shows that the solder has wet the metallization around the die. Figure 4.23 is an X-ray of an assembled sample; the voiding percentage is less than 3%. Voiding of less than 5% was routinely obtained.

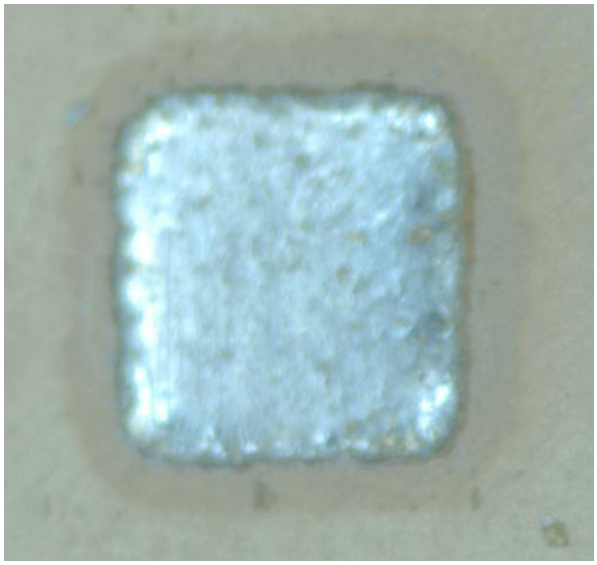


Figure 4.21 Solder Without Die after Optimized Reflow Process

Figure 4.22 Solder With Die after Optimized Reflow Process

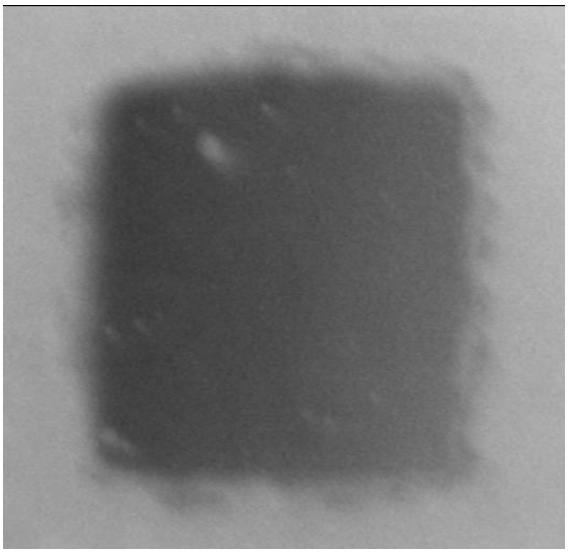


Figure 4.23 X-ray Inspection on the Die Attach on Au/Ni DBC Substrate With Optimized Reflow Process

SiC die attach samples were also assembled with Ag metalized DBC substrate and thick film metallized substrates. The assembly process was the same as used for the Au/Ni DBC substrates.

The SMT resistors were assembled to PdAg and Au metallized substrates. The AgBiX solder paste was printed with a 0.127 mm thick stencil. The resistors were placed with a Palomar Model 3500 placement system, and then reflowed in the PEO 601 in nitrogen with a 3 minutes ramp profile to 320^{o}C.

4.6 Assembly Results

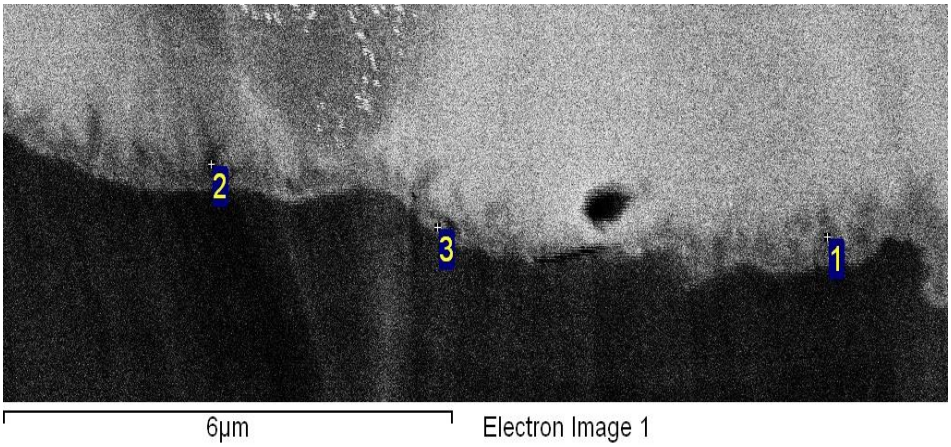
After assembly, the test vehicles were inspected under X-ray to determine the voiding percentage. Shear test was used to evaluate the mechanical reliability of the solder joint. SEM examination of sample cross-sections before shear and fracture surfaces after shear was also done to understand the failure location. The test vehicles fall into three categories by the

substrate type: Ni/Au finish DBC and CuMo substrates, Ag finish DBC substrates and thick film metalized substrate. The assembly results will be described for die attach samples on each substrates.

4.6.1 Die Attach on Ni/Au DBC and CuMo Substrate

The results of non-destructive inspection were present in the previous section. The shear test was done using a Dage PC2400 shear tester (shear limit 100kg). The smaller 2 mm x 2mm SiC on the DBC had an average shear strength of 4.67kg/mm^2 and the failure was in the solder. For the 5 mm x 5 mm SiC die on the CuMo-on-Al_2O_3 substrates, the shear strength was greater than 4kg/mm^2 and could not be sheared due to the limitation of the shear tester.

Figure 4.24 is an SEM image of a cross section of the as-assembled SiC die on DBC. Using SEM and energy dispersive X-ray spectroscopy (EDS) for elemental analysis (Figure 25), we found that a layer of Ni_3Sn_2 formed at the solder-to-substrate interface. Crystals containing Ag and Sn were also observed. EDS and micro X-ray diffraction (Figure.4.26) were used to determine these crystals were $Ag_{0.87}Sn_{0.13}$ (ζ phase). Since the amount of Sn available is limited, the Ag_3Sn intermetallic commonly observed in high-Sn, lead free solders was not observed. Au from the substrate metallization was also detected in the $Ag_{0.87}Sn_{0.13}$ phase intermetallic. The presence of Sn in the cross section confirms the earlier statement that Sn is at least one component of the "X" in the AgBiX solder paste.



Spectrum	Ni	Cu	Sn	Bi
1	37.19	8.82	24.43	29.55
2	37.39	9.06	27.49	26.06
3	25.87	11.84	14.40	47.90

Figure 4.24 EDS Results of Ni-Sn Intermetallic Layer on Ni/Au Substrate

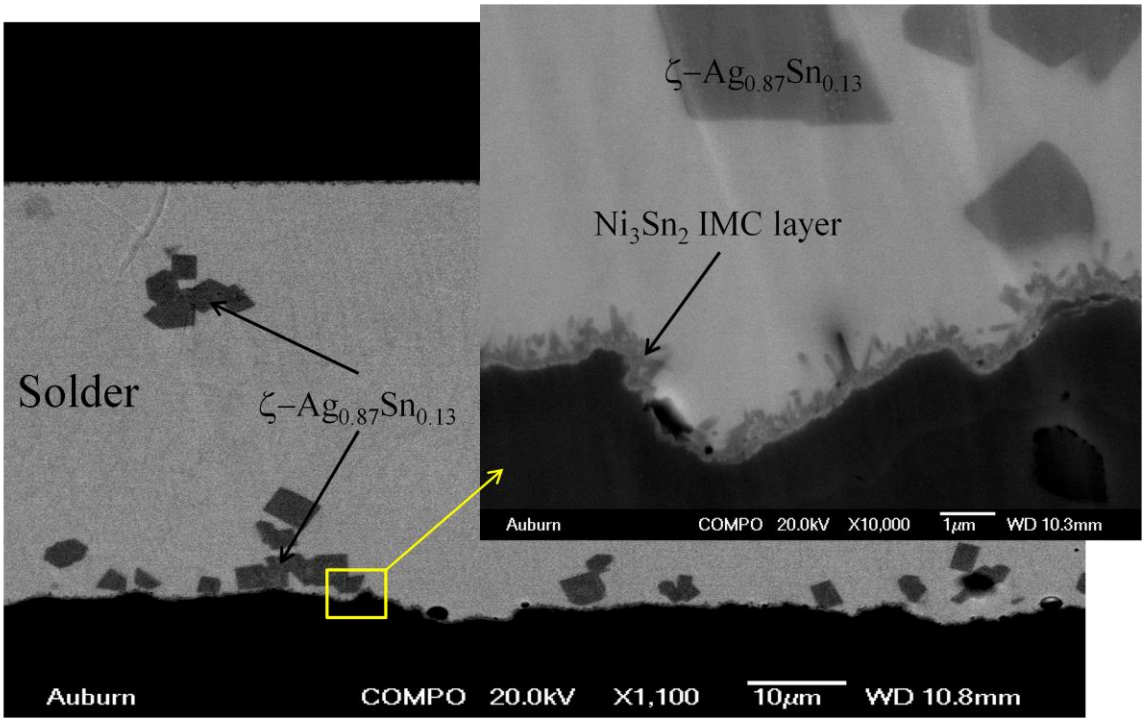


Figure 4.25 SEM Cross Section Image of the SiC Die Attach on a Ni/Au DBC Substrate

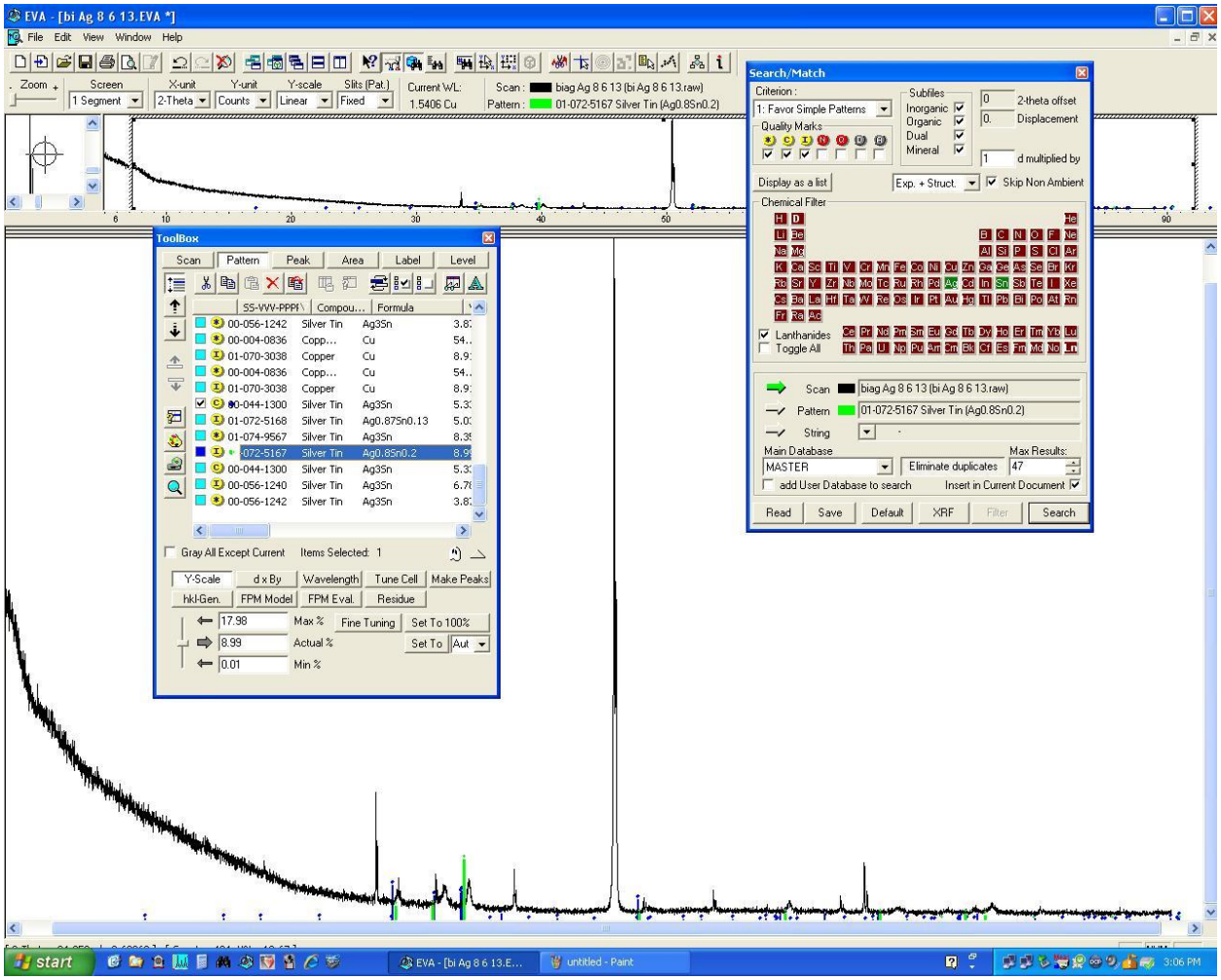


Figure 4.26 Micro X-ray Diffraction Results for the Ag-Sn Crystal in Die Attach on Ni/Au DBC Substrate

Figure 4.27 is a representative elemental analysis line scan of the solder-to-substrate interface. In addition to the Ni_3Sn_2 intermetallic, there is overlap of the Ni and Bi concentrations. The EDS results indicate it is likely $NiBi_3$. Ni and Bi have very limited mutual solubility. There is also an overlap of the Cu and Ni concentrations. This is due to a sintering operation that was used after plating to improve Ni-to-Cu adhesion.

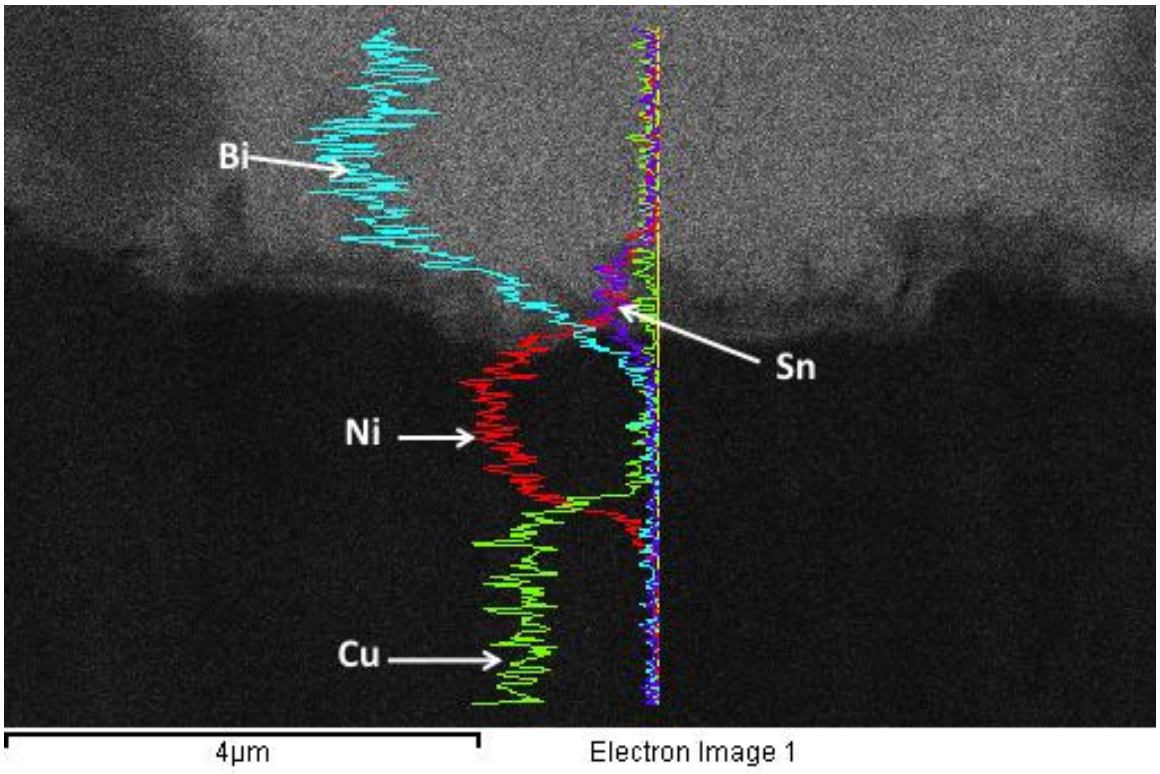
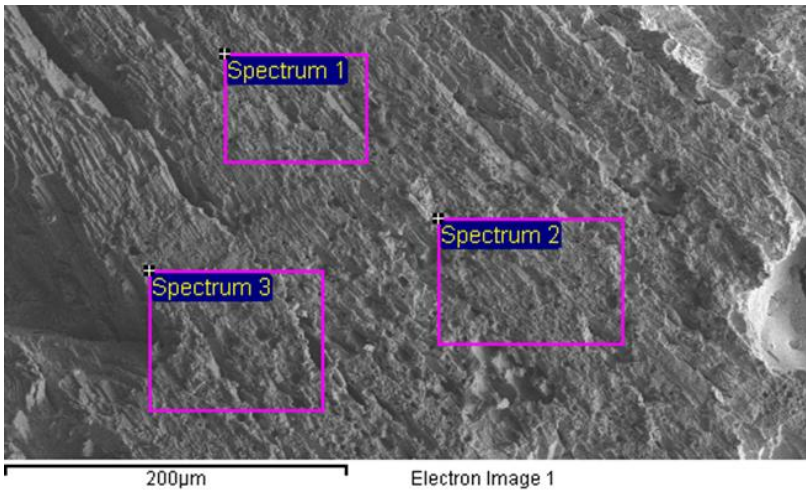


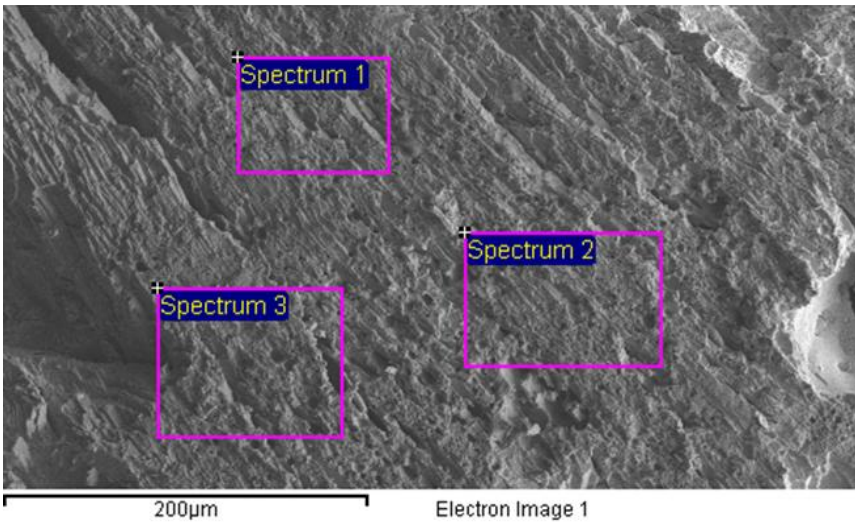
Figure 4.27 Elemental Analysis of Solder-to-Ni/Au DBC Substrate Interface

Fracture surface analysis was performed on the 2 mm x 2mm die samples after shear testing. The fracture surfaces and elemental analysis for the substrate side and die side are shown in Figures 4.28 and 4.29, respectively. Elemental analysis indicates failure in the solder (high Bi and Ag content) near the substrate intermetallic layer (low concentration of Ni and Sn).



Spectrum	Ni	Cu	Ag	Sn	Au	Bi
Spectrum 1	5.06	1.99	8.87	4.85	1.21	78.01
Spectrum 2	4.18	1.73	8.59	4.04	1.46	80.00
Spectrum 3	16.06	3.22	6.29	12.84	2.60	59.00

Figure 4.28 SEM Image and Elemental Analysis of DBC Substrate-side Fracture Surface



Spectrum	Ni	Ag	Sn	Bi
Spectrum 1	1.21	11.90	2.76	84.13
Spectrum 2	0.90	11.48	3.33	84.29
Spectrum 3	0.89	10.45	3.24	85.42

Figure 4.29 SEM Image and Elemental Analysis of Die-side Fracture Surface

4.6.2 Die Attach on Silver Finish DBC Substrate

The assembly process was the same as the previous die attach on Ni/Au finish DBC. A nitrogen cover gas was used to minimize voiding. Figure 4.30 is an example X-ray show the level of voiding.

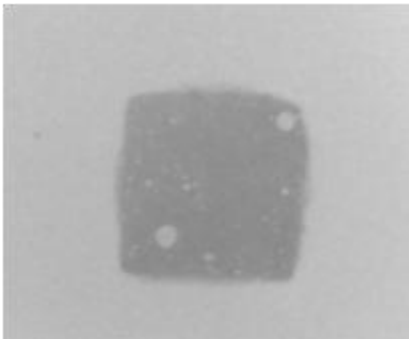


Figure 4.30 X-ray Image of Die Attach (4.1% void area)

Figure 4.31 is a cross section of the as-built sample, and Figure 4.32 is the region near the DBC substrate interface. The Cu_3Sn intermetallic layer has spalled and a layer of Bi exists between the Cu_3Sn layer and the bulk Cu. Spalling of the Cu_3Sn layer has previously been reported for high lead solders on Cu [59, 60] and results from the limited Sn available from the solder. The Bi layer forms a continuous bond with the Cu.

The crystals identified by locations 2 and 3 in Figure 4.32 are Ag crystals with Sn incorporated. According to the Ag-Sn phase diagram in Figure 4.3, Sn has a high solubility limit (~10 wt%, 9 at%)) in Ag at room temperature. Given the limited Sn available in the solder paste and the competition with Cu for forming intermetallic, the Ag_3Sn intermetallic does not form.

There are micro-voids in the Cu_3Sn layer. The formation of micro-voids has been related to voids or ‘caves” between the plated Ag and Cu created during the Ag plating process [61, 62]. Figure 4.33 is a cross section of the as-plated thermal cycle substrates. Voids are clearly present between the Cu and the plated Ag.

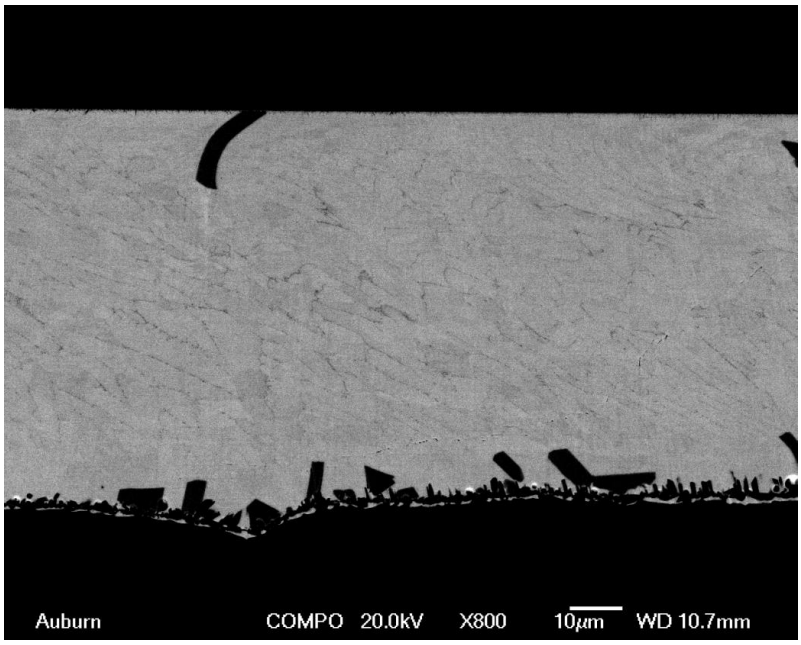
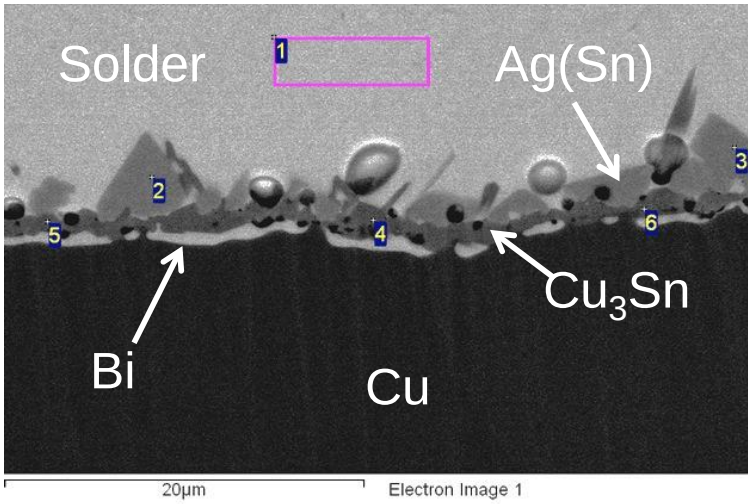


Figure 4.31 Cross Section of Solder Joint on As Built Sample



Location	Cu	Ag	Sn	Bi
1	0.0	0.0	0.0	100
2	0.0	92.5	7.5	0.0
3	0.0	92.1	7.9	0.0
4	73.8	0.0	26.2	0.0
5	75.2	0.0	24.8	0.0
6	78.4	0.0	21.6	0.0

Figure 4.32 Cross Section of Solder Joint (reflowed at 320^{o}C peak) near the Substrate Side and Elemental Analysis (atomic %).

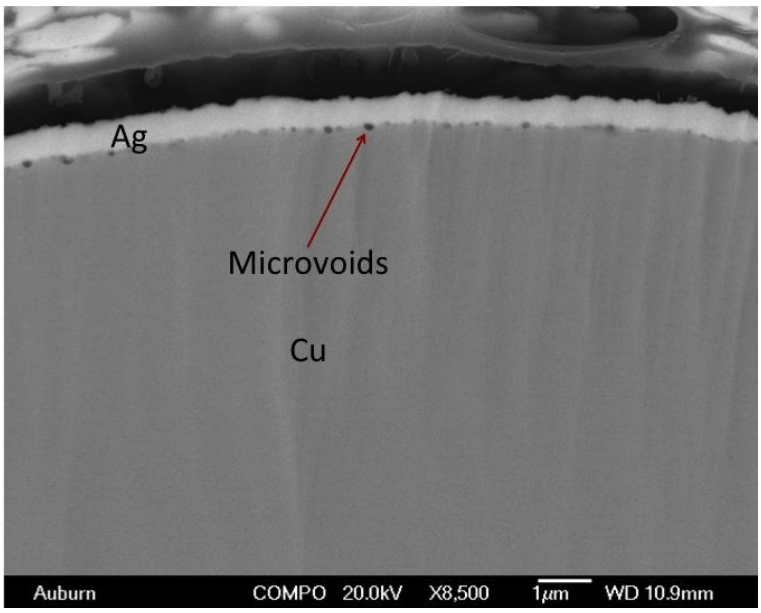


Figure 4.33. Cross Section of As-plated Ag on Cu showing Microvoids at Ag-to-Cu interface

Figure 4.34 shows a higher magnification of the bulk solder. A network of fine Ag particles can be seen at the Bi colony boundaries. This is consistent with the negligible solubility of Ag in Bi. Sn was not detected in the Ag particles by energy dispersive X-ray spectroscopy (EDS) analysis.

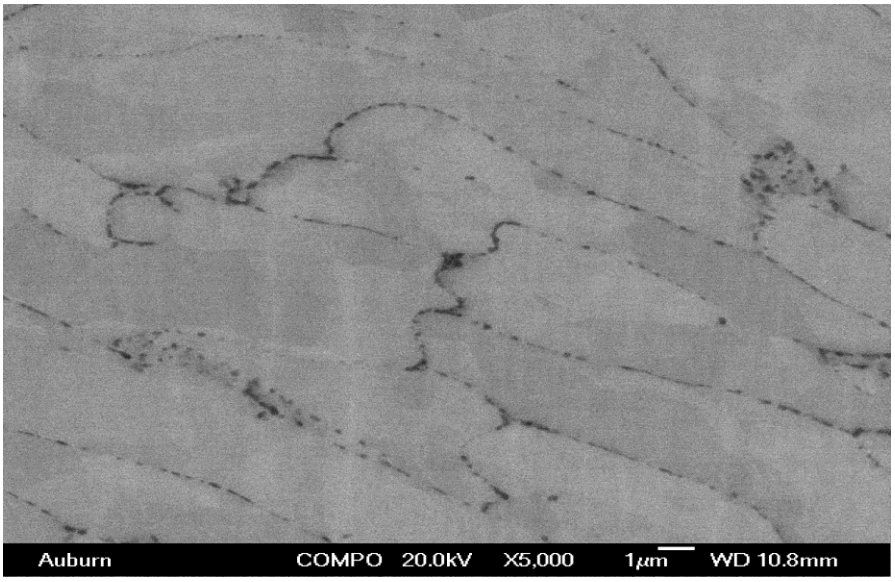


Figure 4.34 Cross Section Image of the Bulk Solder Showing Ag Particles at the Bi Colony Boundaries

Figure 4.35 is a cross section of the solder joint on the die side. Ni_3Sn_4 intermetallic is

observed at the die interface. Ag(Sn) crystals are also present.

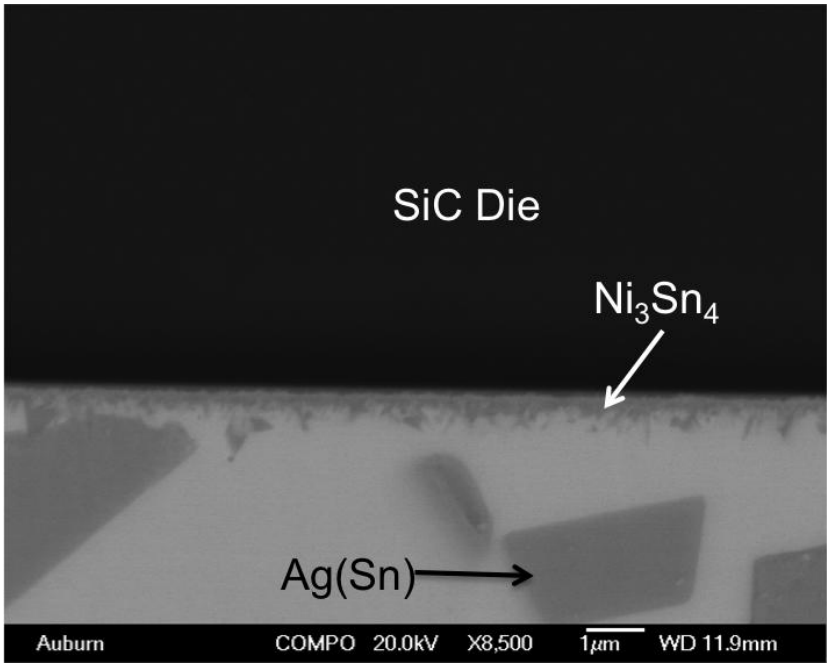


Figure 4.35 Cross Section Image of the Solder at the SiC Die Interface

To examine the effect of reflow temperature on the Cu_3Sn spalling, substrates with deposited solder paste were reflowed at lower temperatures. Even at a peak temperature of 280^{o}C, spalling was observed (Figure 4.36). Significant voiding was observed in the Bi layer between the Cu and the Cu_3Sn layer with reflow at 280^{o}C. Reflow at 320^{o}C was required to get good flow of the molten solder when assembling die and is consistent with the paste manufacturer's reflow recommendations. Based on these results all test samples were reflowed with a peak reflow temperature of 321^{o}C.

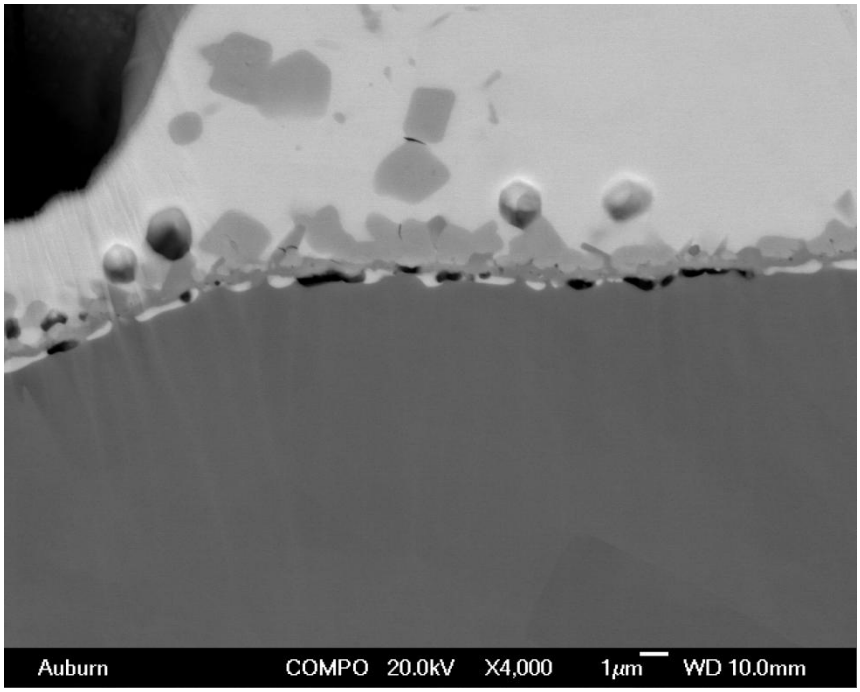


Figure 4.36 Cross Section of Solder Joint near the Substrate Side with Reflow at 280^{o}C Peak Temperature

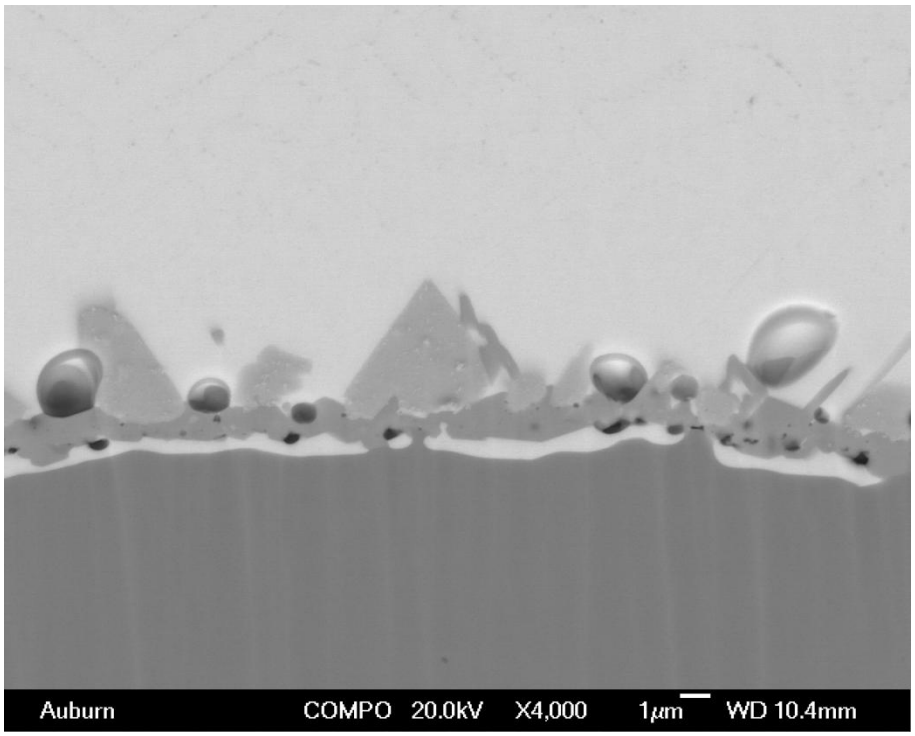


Figure 4.37 Cross Section of Solder Joint near the Substrate Side with Reflow at 321^{o}C Peak Temperature

Die shear testing of as-built high temperature aging samples was performed using a Dage PC2400 with a 100kg shear module. The average shear strength was 4.4kg and the failure was in the bulk solder. The cross section of sheared die and substrate were shown in Figure 4.38 and Figure 4.39.

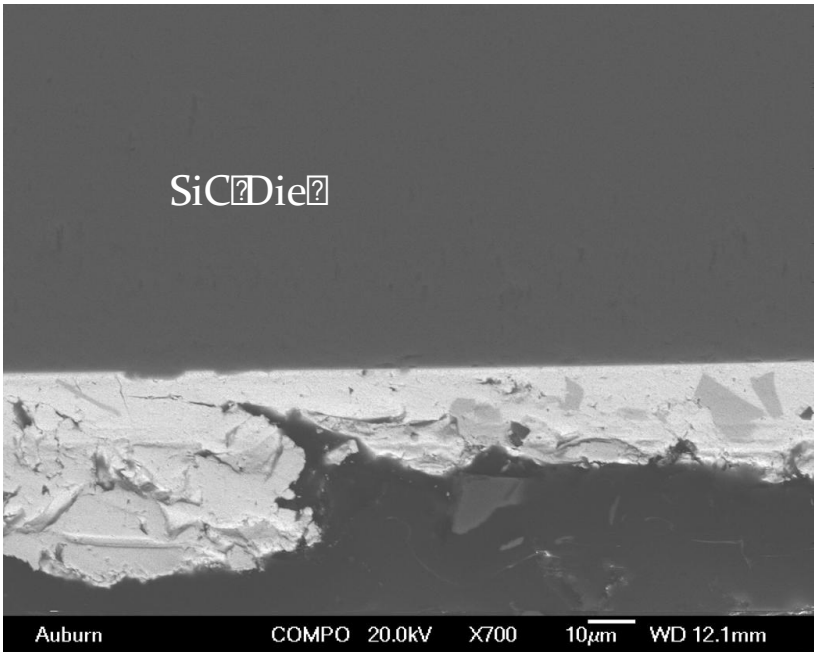


Figure 4.38 Cross Section of Die-side after Die Shear showing Failure in the Solder

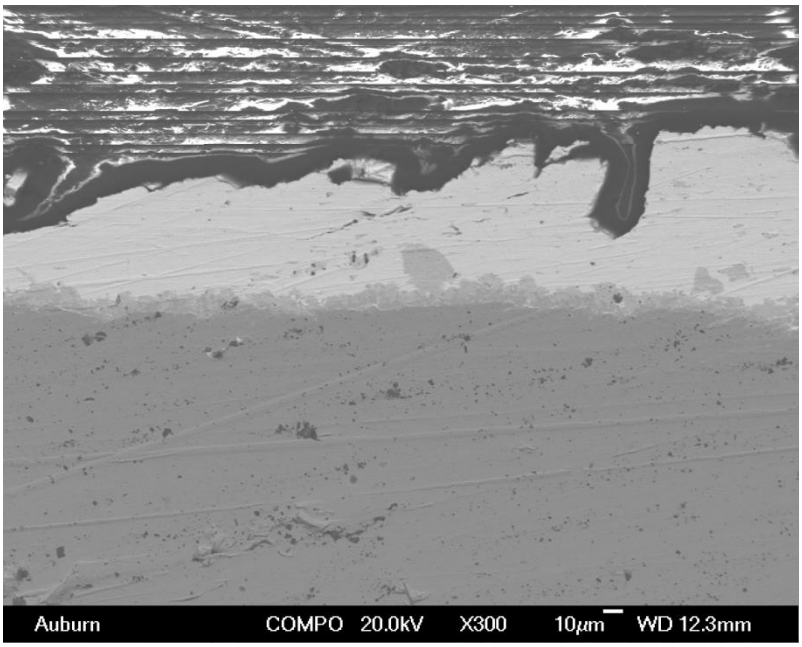


Figure 4.39 Cross Section of Substrate-side after Die Shear showing Failure in the Solder

4.6.3 Die Attach on Thick Film Metallized Substrate

Die Attach on thick film metallized substrate were also assembled to evaluate the performance of AgBiX solder paste. After assembly, the test vehicles were inspected for voiding using X-ray, as shown in Figure 4.40. Voiding of 5% or less was routinely obtained for die attach on Ag substrates, while the voiding of die attach on PdAg substrates was a little higher.

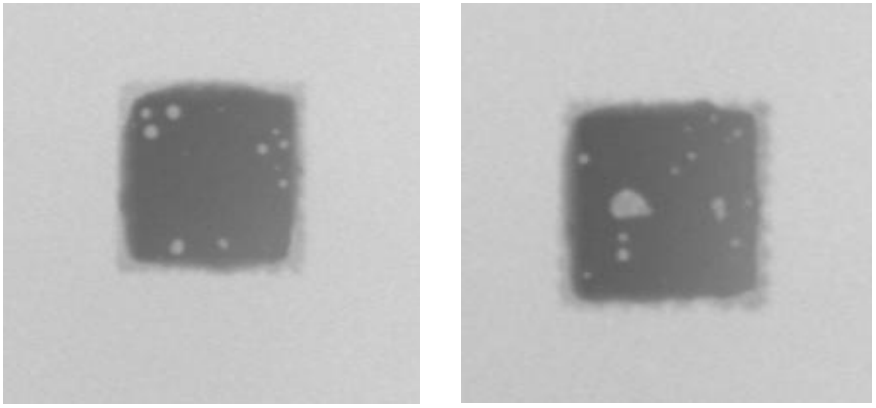


Figure 4.40 X-ray Image of 2 mm x 2 mm Die Assembled on Ag Substrate (left) and PdAg Substrate (Right)

SEM and EDS were also used to characterize the cross section of as built samples. Figure 4.41 is an SEM image of a cross section of an as built SiC die on a thick film Ag metallized alumina substrate. Sn and Ag from AgBiX solder paste forms Ag(Sn) crystals in the solder joint. In addition to Ag(Sn) crystals, the element analysis line scan of the die-to-solder interface in Figure 4.41 also shows there is overlap of Ni and Sn concentrations at the interface of the die and solder. From the results of energy dispersive X-ray spectroscopy (EDS), this intermetallic layer at the die-to-solder interface is likely Ni_3Sn_2. Ni is from the thin film metallization on the SiC die.

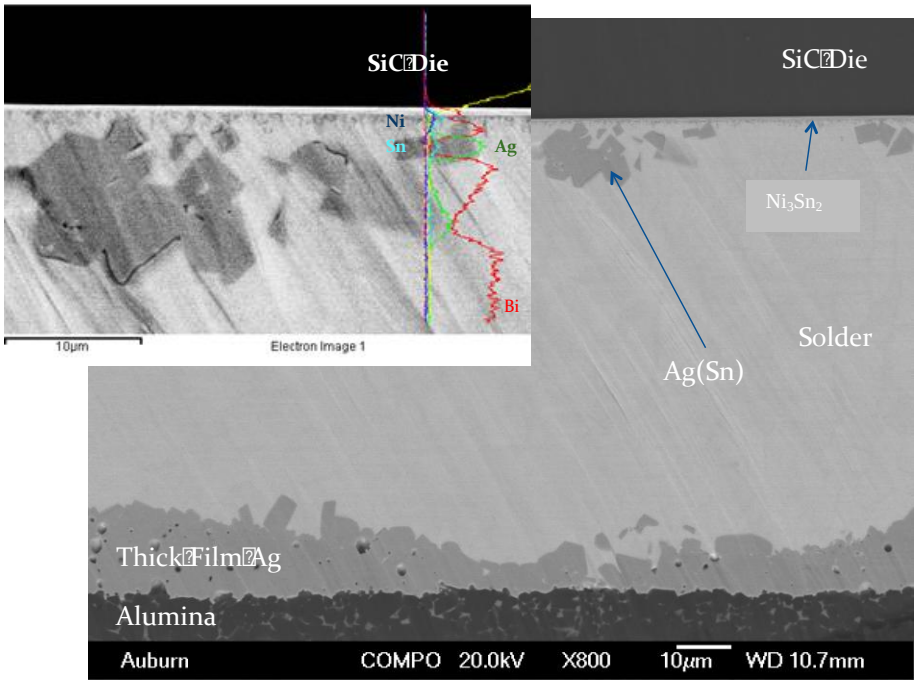
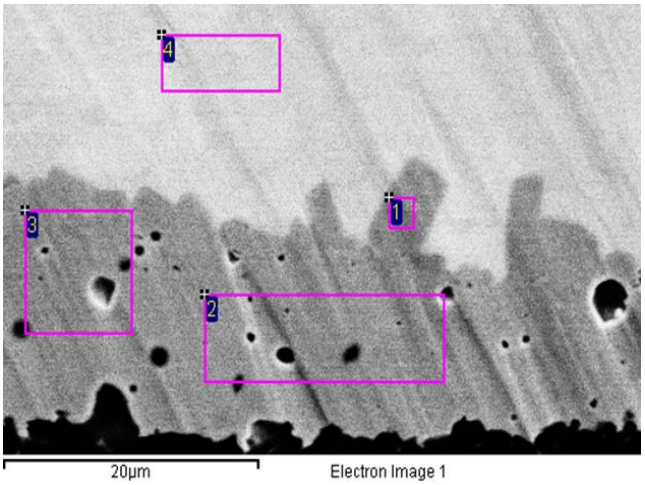


Figure 4.41 Initial Cross Section of Die Attach on Thick Film Ag Substrate

A closer at the interface of the solder and thick film Ag substrate metallization, reveals some crystal shapes on the top of the thick film layer. The EDS results in Figure 4.42 indicate these are Ag with dissolved Sn (Ag(Sn)). The absence of Sn and Bi in spectrums 2 and 3 indicates that neither Bi nor Sn diffused in to the thick film Ag layer, Sn just reacted with the Ag at the top of the thick film Ag layer.



Spectrum	Ag	Sn	Bi
1	91.32	8.68	0.00
2	100.00	0.00	0.00
3	100.00	0.00	0.00
4			100.00

Figure 4.42 SEM Image and Elemental Analysis of Solder-to-Ag Substrate Interface

Figure 4.43 is a cross section of a solder joint on a PdAg thick film metallized substrate. Like the cross section of die attach on the thick film Ag sample, Ni from the SiC thin film metallization forms a thin layer of Ni_3Sn_2 at the die. Besides the crystals of Ag(Sn) in the solder joint, there are a few lighter color crystals present. Elemental analysis of the "light color crystals" using EDS revealed: Bi 67.21 at.%, Pd 32.79 at.%. The ratio of Bi to Pd suggests the formation of a Bi_2Pd intermetallic. EDS results at the interface of the solder to thick film PdAg layer shows that Sn forms PdSn intermetallic with Pd from the thick film layer (spectrum 3 and 4 in Figure 4.44). The concentration of Bi decreased from the top of the PdAg layer to the bottom.

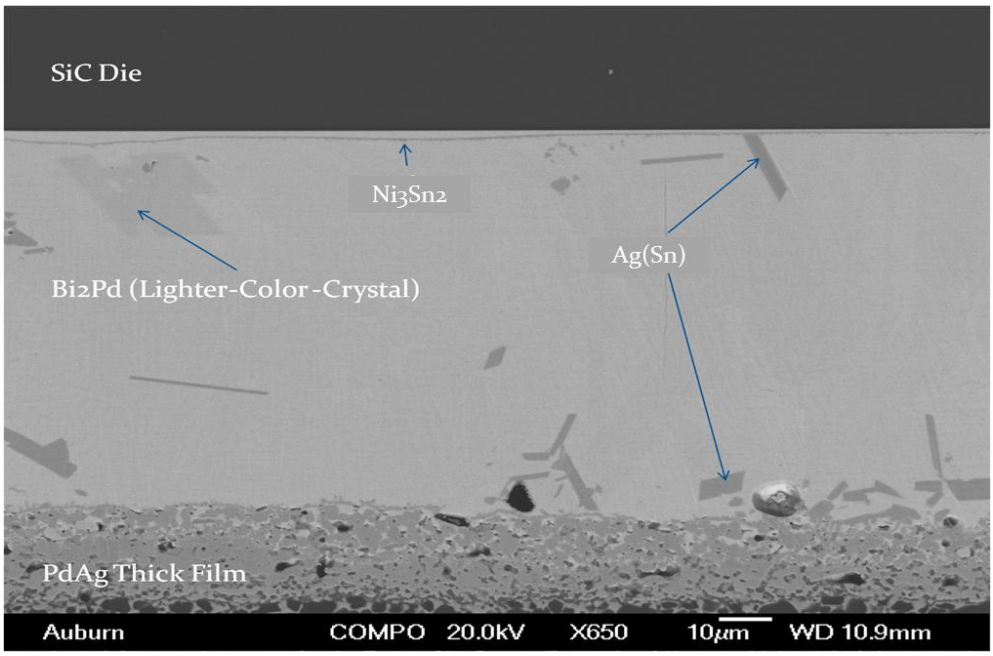
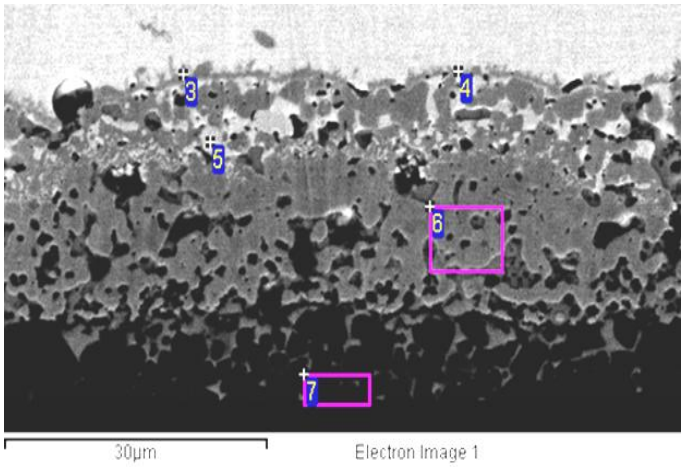


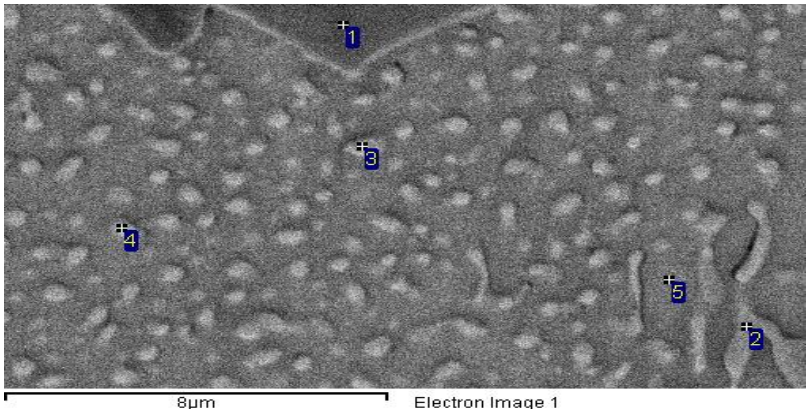
Figure 4.43 Initial Cross Section of Die Attach on Thick Film PdAg Substrate



Spectrum	Pd	Ag	Sn	Bi	Al	O
3	52.96		47.04			
4	50.57		49.43			
5	32.87	0.00	0.00	67.13		
6	23.67	69.50	0.00	6.83		
7		0.27		0.66	34.54	64.53

Figure 4.44 SEM Image and Elemental Analysis of Solder-to-PdAg Substrate Interface

The PtPdAu metallization did not wet well, resulting in low shear strengths. To address the wetting issue, a layer of pure Au (no binder) thick film was printed over the PtPdAu layer. This configuration wet well, but had lower shear strength than the Ag and PdAg samples. Figures 4.45 is the SEM picture of cross sections of the PtPdAu+Au assembly. The large crystal was composed of Ag and Au, while the smaller crystals contained Au and Bi. This indicates significant dissolution of Au into the molten solder during reflow. Two failure modes were observed in the die shear samples. The majority of the samples failed in the solder with Bi, Au, Ag and Sn present at both fracture surfaces. A few samples failed in the thick film near the thick film-to-substrate interface. Elemental analysis of the fracture surface revealed Sn and Bi present, indicating significant diffusion of Sn and Bi into the PtPdAu thick film layer during reflow.



Spectrum	Ag	Sn	Au	Bi
1	18.38	0.00	81.62	0.00
2	0.00	0.00	53.87	46.13
3	0.00	0.00	48.39	51.61
4	0.00	0.00	41.51	58.49
5	0.00	0.00	0.00	100.00

Figure 4.45 SEM Image and Elemental Analysis of Solder Joint on Au+PtPdAu Substrate

To evaluate the mechanical integrity of the solder joints, die shear and resistor shear tests were conducted with a Dage PC2400 shear tester. For the 2mm x 2mm SiC die attach on thick film Ag substrates, the average initial shear strength was 4.48kg/mm^2, with failure at the interface of thick film and the alumina substrate. For 2mm x 2mm die attach on thick film PdAg substrates, the initial shear strength was 4.67kg/mm^2, and the failure mode was in the solder. For PtPdAu substrate, the average shear strength was below 1kg/mm^2 due to the poor wetting on the substrate surface. For PtPdAu + Au substrate, the average shear strength was 1.4kg/mm^2, the major failure mode was in the solder near the die. After the analysis of preliminary results of die attach on different thick film metallized substrates, die attach on thick film Ag and thick film PdAg was chosen to continue the reliability tests.

For resistor attach, the initial shear force of samples on Ag substrates was 7.23kg and the failure was between the thick film Ag and the alumina substrate. For the PdAg substrate resistor test vehicles, the average shear force was 7.19Kg and the failure mode was in the solder. The resistor shear strength for the Au thick film metallization was low and the failure was at the thick film-to-substrate interface. Au and Bi have a eutectic temperature of 241^{o}C. During the assembly reflow processes, the Au thick film dissolves into the molten AgBiX solder, degrading the thick film-to-substrate adhesion.

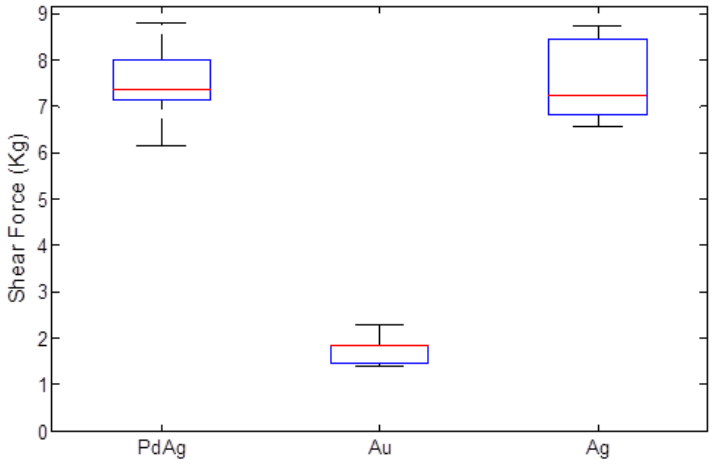


Figure 4.46 Initial Resistor Shear Test Results

4.7 Reliability Test

Test samples with Ni/Au finish DBC, Ni/Au finish CuMo on alumina, Ag finish DBC and thick film metalized alumina (Ag, PdAg) were evaluated in reliability tests. The reliability tests were high temperature storage tests and thermal cycling. For the high temperature storage test, the samples were aged at 200^{o}C in air. The samples were sheared at different time intervals to evaluate the mechanical performance of solder joint. For thermal cycle test, the samples were cycled from -55^{o}C to +195^{o}C in a single chamber thermal cycle system in ambient air. The thermal cycle profile is shown in Figure 4.47. SEM, EDS and XRD were used to analysis the cross section and fracture surface to understand the mechanism behind the change of the shear data.

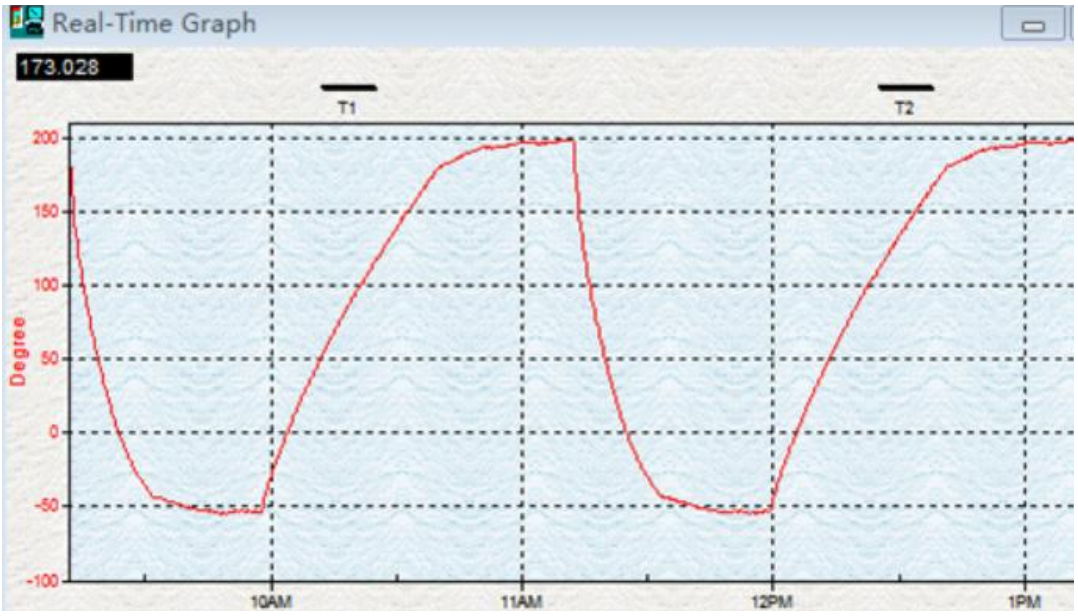


Figure 4.47 Thermal Cycle Profile

4.7.1 Die Attach on Ni/Au Finish DBC

4.7.1.1 High Temperature Storage Test

The die shear results are shown in Figure 4.48. There was a decrease in shear strength during the first 500 hours of storage, followed by a slower decrease through 2000 hours. The shear strength remained relatively constant from 2000 hours through 5000 hours. After 5000 hours, the average die shear strength exceeds MIL-STD-883, Method 2019.7 by more than a factor of three (i.e., >3x).

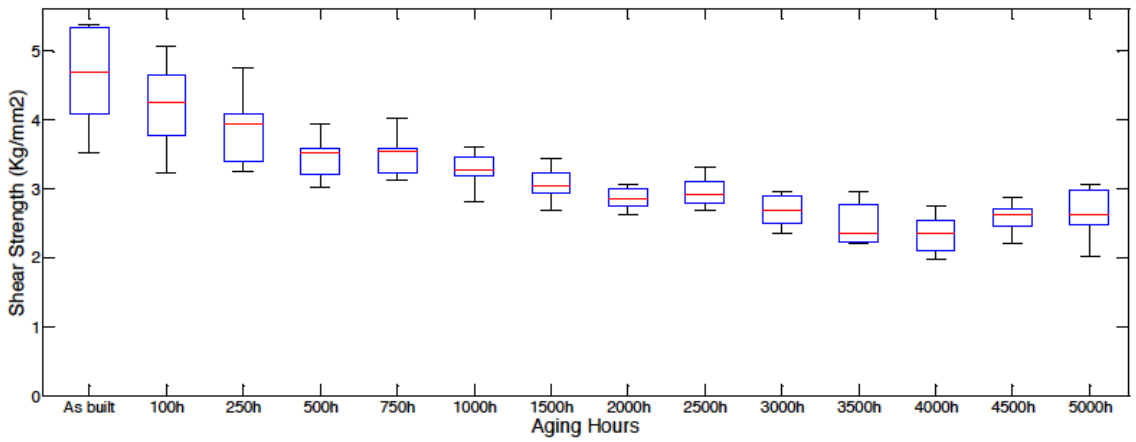
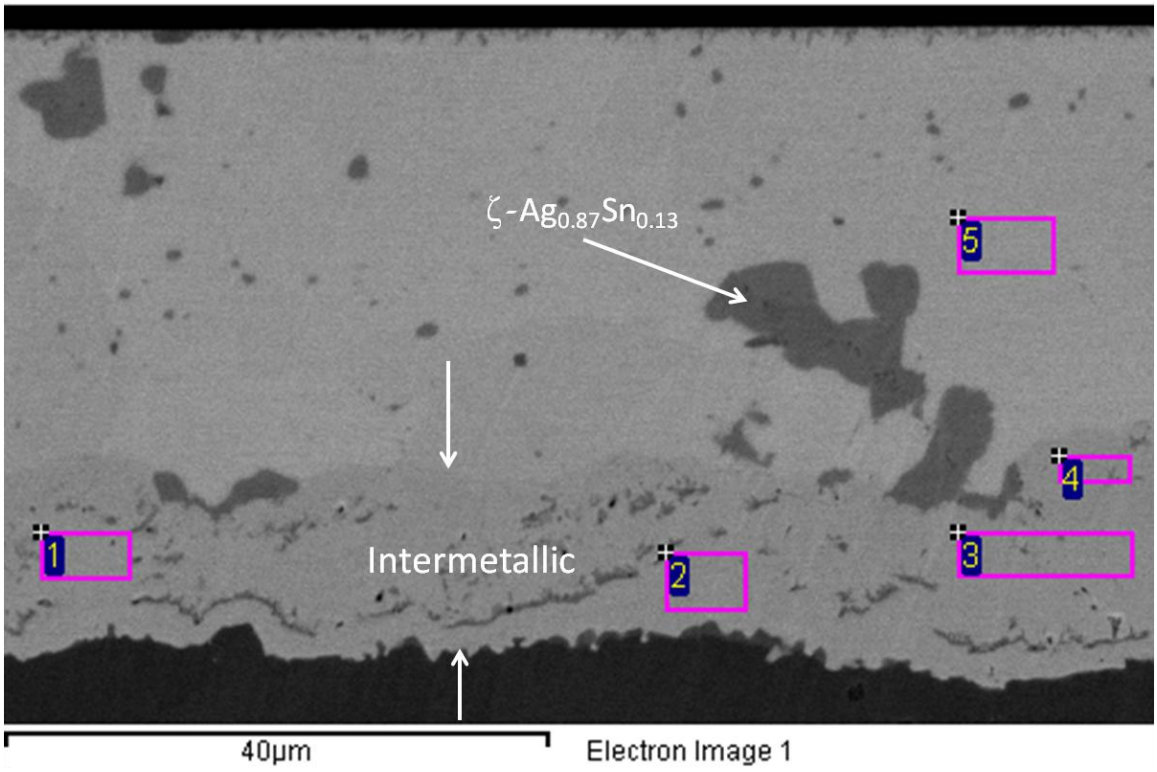


Figure 4.48 2 mm x 2 mm SiC Die Shear Strength as a Function of 200°C Storage Time

Figure 4.49 is a cross section of a solder joint after storage for 1000 hours at 200°C. As shown in Figure 4.50, Ni_3Sn_4 is present in the region labeled "Intermetallic" in Figure 4.51. Elemental analysis of the "Intermetallic" layer using EDS revealed: Ni 24.0 at.%, Bi 74.5 at.%, and Au 1.5 at.%. The Ni-to-Bi ratio suggests the formation of a $NiBi_3$ intermetallic. Micro X-ray diffraction was used to confirm the crystal structure of the intermetallic layer. The results are shown in Figure 4.57. The observed peaks closely correspond to $NiBi_3$. The shifts in the peaks are presumed to be the result of incorporation of Au within the crystal structure, slightly altering the lattice spacing. These results support the earlier assumption that a thin region of $NiBi_3$ formed in the initial solder joint.



Spectrum	Ni	Au	Bi
Spectrum 1	23.77	1.85	74.38
Spectrum 2	24.77	1.68	73.55
Spectrum 3	23.59	1.28	75.13
Spectrum 4	23.86	1.10	75.03
Spectrum 5			100

Figure 4.49 SEM Cross Section Image and Elemental Analysis of a Solder Joint after 1000 hours at 200^{o}C

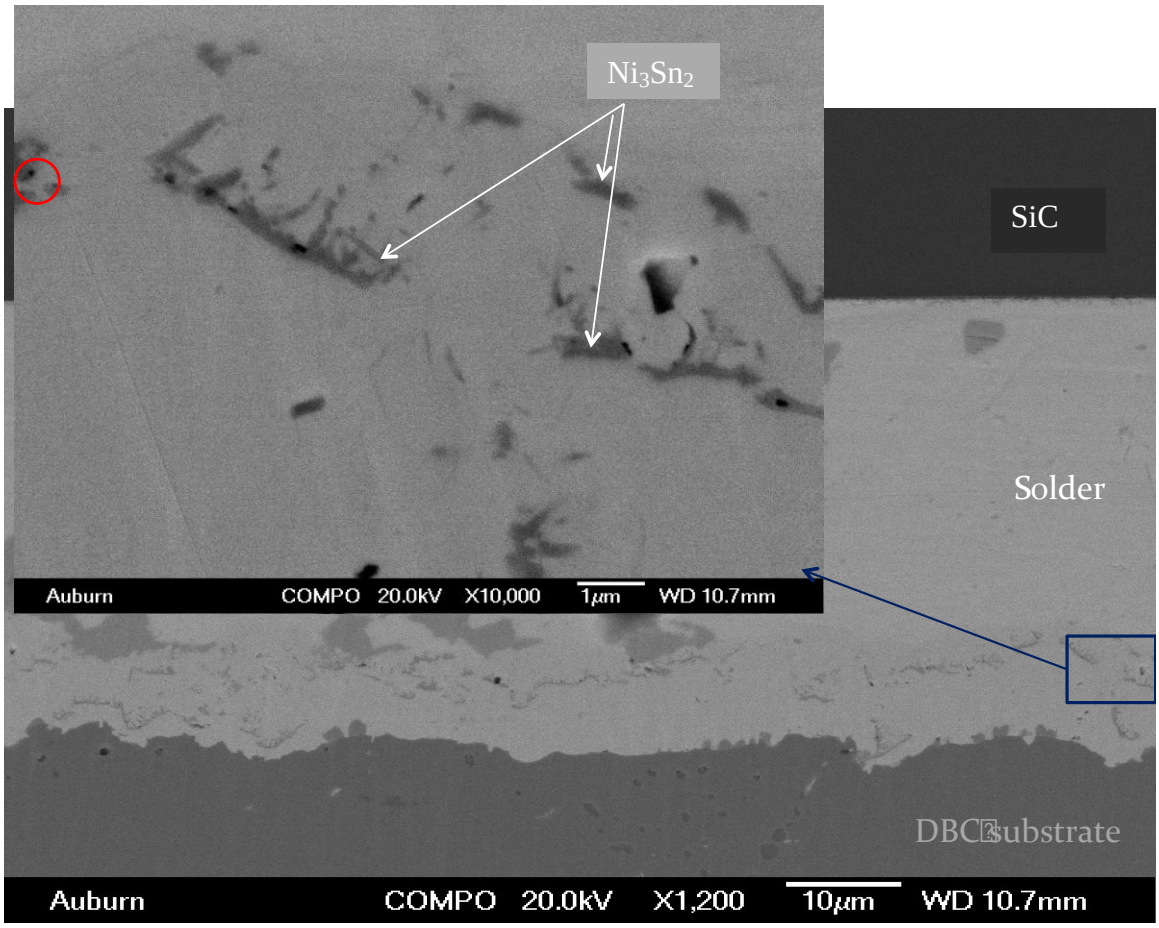
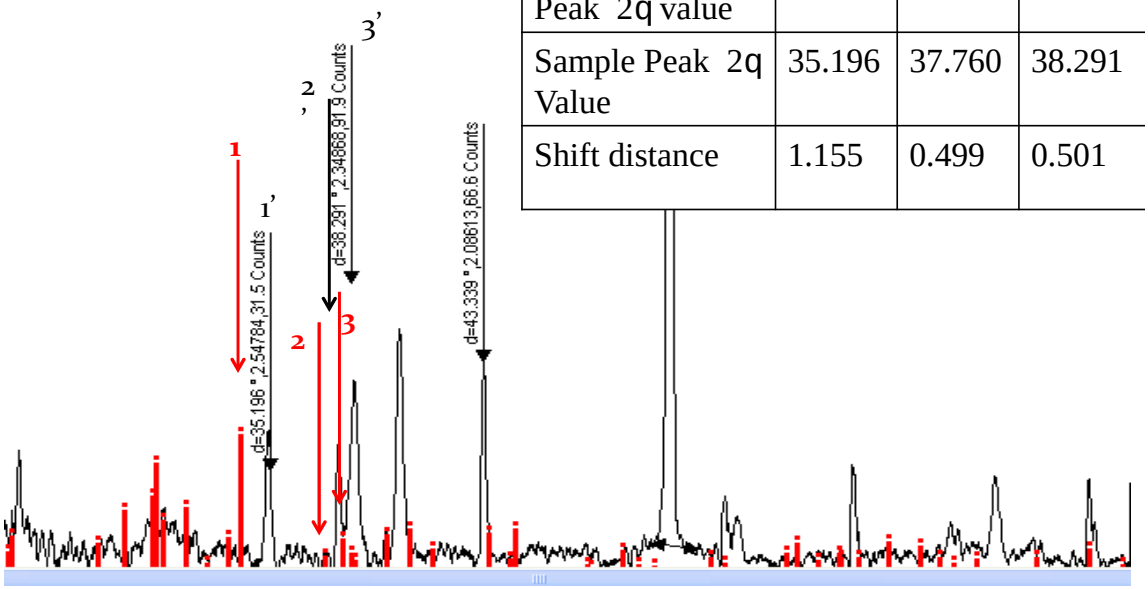


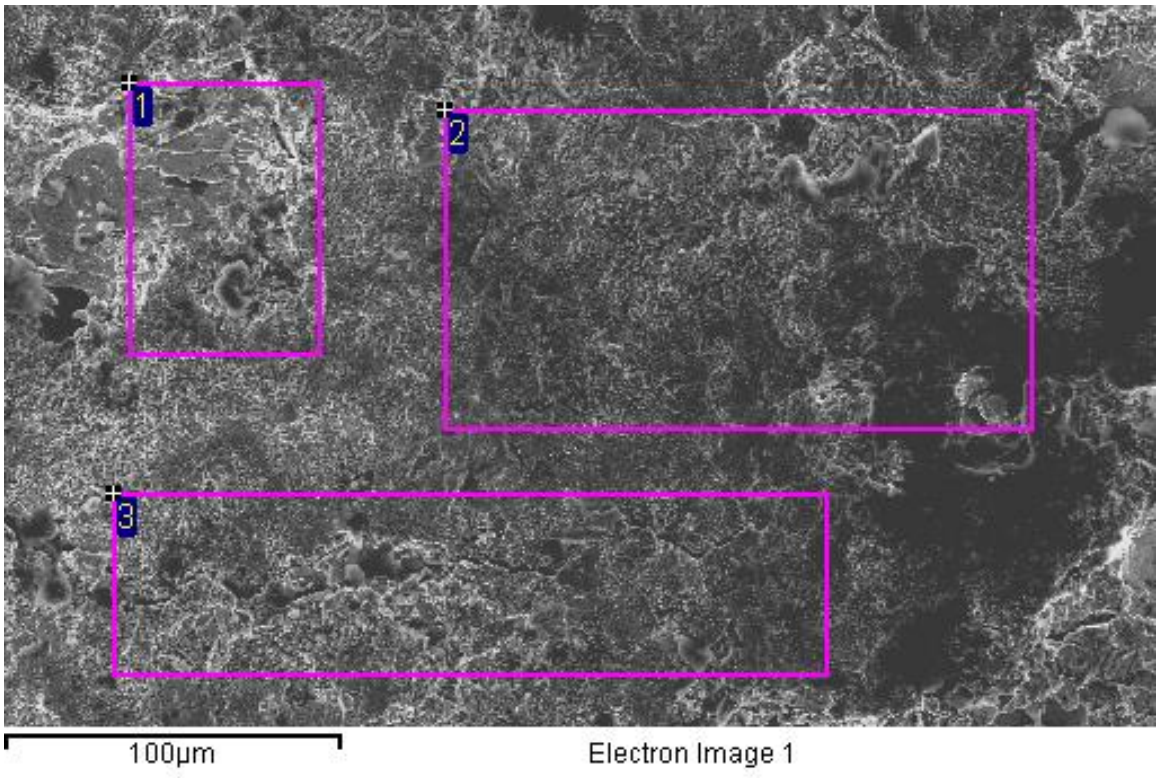
Figure 4.50 SEM Cross Section Image showing Ni_3Sn_2 within the "Intermetallic" Region



$NiBi_3$	Peak 1	Peak 2	Peak 3
Standard Peak 2θ value	34.041	37.261	37.790
Sample Peak 2θ Value	35.196	37.760	38.291
Shift distance	1.155	0.499	0.501

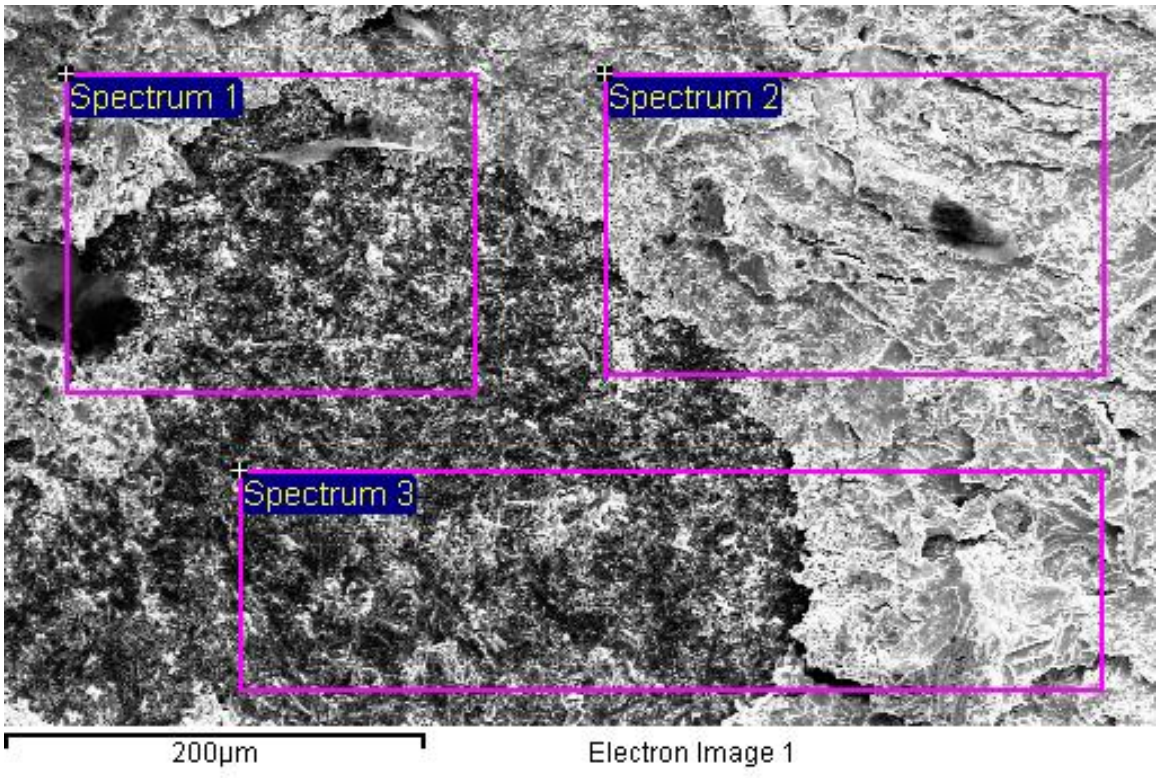
Figure 4.51 Micro X-ray Diffraction Results for the Intermetallic Layer after 1000 Hours of Storage

Figure 4.52 shows the die-side fracture surface after shear testing of a sample aged for 1000 hours. Figure 4.53 is the corresponding substrate-side fracture surface. From these results, we observe that the fractures occurred at and near the Cu-to-$NiBi_3$ interface.



Spectrum	Ni	Au	Bi	Sn
Spectrum 1	21.75	1.82	73.22	3.21
Spectrum 2	24.66	1.33	74.01	0.0
Spectrum 3	25.52	2.12	69.80	2.56

Figure 4.52 SEM Image and Elemental Analysis of Die-side Fracture Surface after Die Shear of a 1000h Aged Sample



Spectrum	Ni	Cu	Sn	Au	Bi
Spectrum 1	4.96	73.58	1.17	1.61	18.68
Spectrum 2	20.12	5.59	2.92	2.79	68.58
Spectrum 3	3.75	74.36	0.0	1.63	20.25

Figure 4.53 SEM Image and Elemental Analysis of Substrate-side Fracture Surface after Die Shear of a 1000h Aged Sample

As shown in Figure 4.54, after 5000 hours aging, we can see the thickness of Ni_3Bi didn't change much, still around 10 um. That is because after 1000 hours aging, Ni on the DBC substrate has been consumed totally in forming Bi_3Ni with Bi in the solder, so there's no additional Ni to form further intermetallic. Compared with the cross section of the 1000 hour aged samples, the micro-structure of the solder joint of 5000h aged sample looks very similar. The fracture surface analysis shows the failure was still in the Bi_3Ni layer. That's explains why the shear strength began to stabilize after 1000hours aging to 5000h aging.

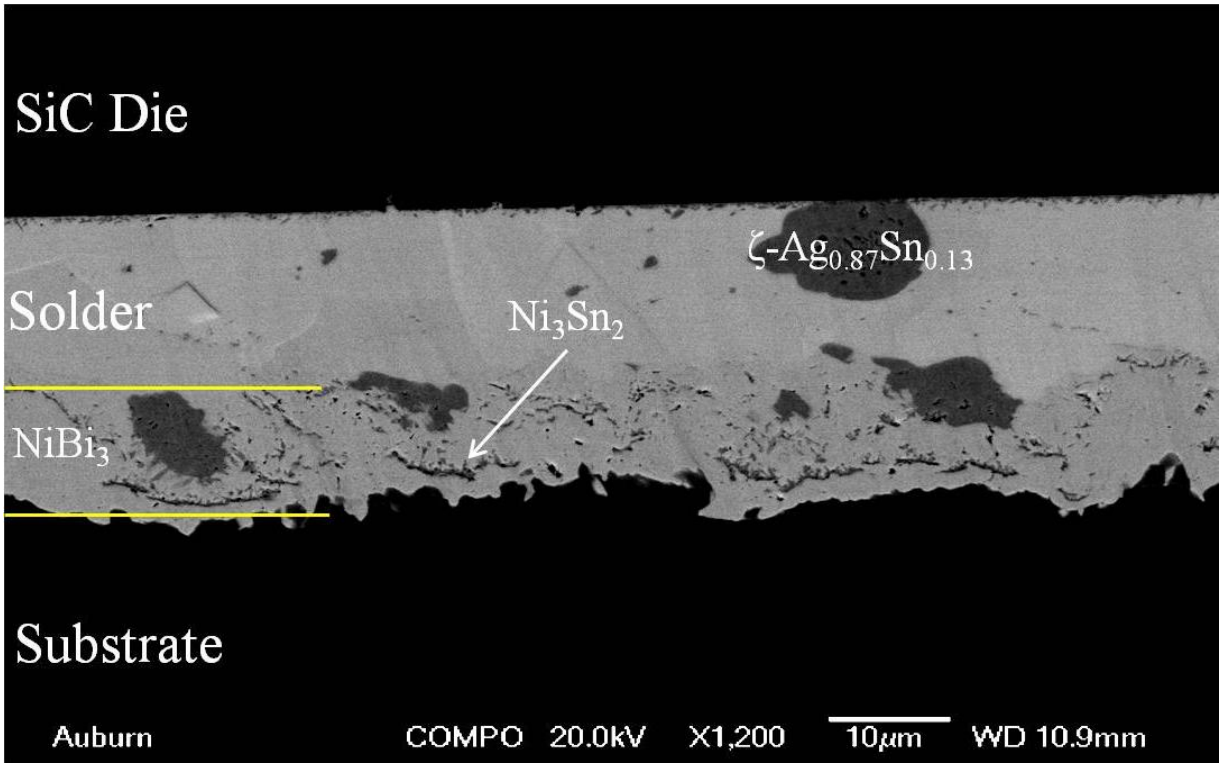


Figure 4.54 SEM on a Cross-section of 5000h Aged Sample

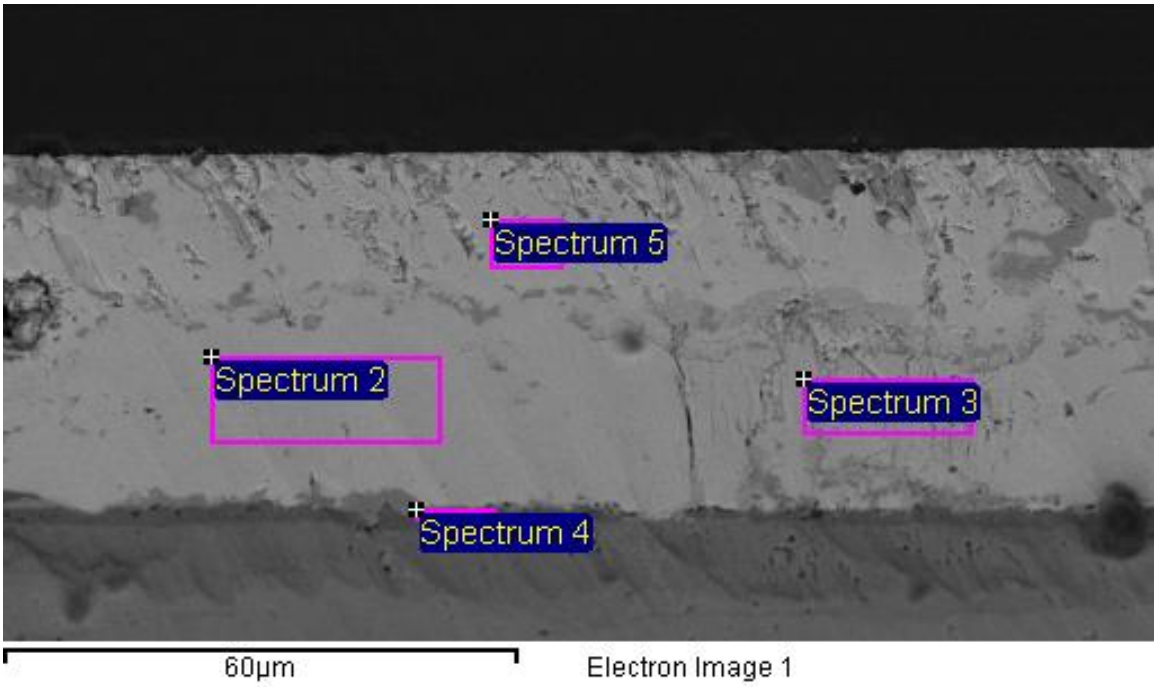
4.7.1.2 Thermal Cycle Test

Shear tests were performed after thermal cycling and the results are presented in Table 4.1. Eight samples were tested at each cycle interval. The initial shear strength of most samples exceeded the capability of the 100kg shear cartridge (>4kg/mm^2), which was consistent with the initial shear strength of the smaller die. After 2000 cycles, the die shear strength significantly exceeds MIL-STD-883, Method 2019.7 requirements for a 5 mm x 5mm die (0.1kg/mm^2).

Table 4.1 Die Shear Test Results after Thermal Cycling (kg/mm^2).

Initial	100 Cycles	250 Cycles	500 Cycles	1000 Cycles	1500 Cycles	2000 Cycles
>4	>4	>4	2.86	3.13	2.69	2.84
>4	>4	>4	3.61	3.31	2.82	2.29
>4	>4	>4	3.23	3.14	2.51	2.28
>4	>4	>4	3.01	2.91	2.93	2.59
>4	>4	3.75	3.16	2.74	2.86	2.33
>4	3.83	3.45	2.83	2.97	2.82	2.56
>4	3.41	3.68	3.15	3.01	3.02	2.50
>4	3.72	3.37	3.27	3.12	2.76	2.46
			Ave=3.14	Ave=3.04	Ave=2.79	Ave=2.47

Figure 4.55 shows a cross section of a sample after 1000 thermal cycles. The $NiBi_3$ intermetallic layer has formed, but has not consumed the entire Ni layer. SEM examination of cross sections after 2000 thermal cycles revealed the Ni layer was completely consumed into the $NiBi_3$ intermetallic layer.



Spectrum	Ni	Sn	Bi
Spectrum 2	25.29		74.71
Spectrum 3	29.63	7.33	63.32
Spectrum 4	98.02		1.98
Spectrum 5			100

Figure 4.55 SEM Cross Section Image and Elemental Analysis of a Solder Joint after 1000 Thermal Cycles

A cross section was taken through the middle of a die after 1000 thermal cycles. Figure 4.56 is an image taken near one edge of the die cross section. A crack approximately 90µm long is observed in the solder near the die. Figure 4.57 is a substrate-side fracture surface after die shear of a sample that had been thermal cycled 1000 times. The material around the perimeter of the substrate pad is Bi, while the interior composition is consistent with the $NiBi_3$ intermetallic and a remaining Ni layer. Thus the fracture in the perimeter area corresponds to the fatigue cracks resulting from the thermal cycling, while the fracture in the $NiBi_3$ intermetallic near the

Ni layer was a result of the applied force during the shear test. The percentage of solder area cracked around the perimeter during the 1000 thermal cycles was small. The decrease in shear strength with failure near the $NiBi_3$ intermetallic-to-Ni/Cu interface is consistent with the decrease in shear strength with high temperature aging, which also failed near the $NiBi_3$ intermetallic-to-Cu interface. Examination of the die shear fracture surfaces after 2000 cycles revealed limited perimeter solder cracking and failure near the $NiBi_3$ intermetallic-to-Cu interface.

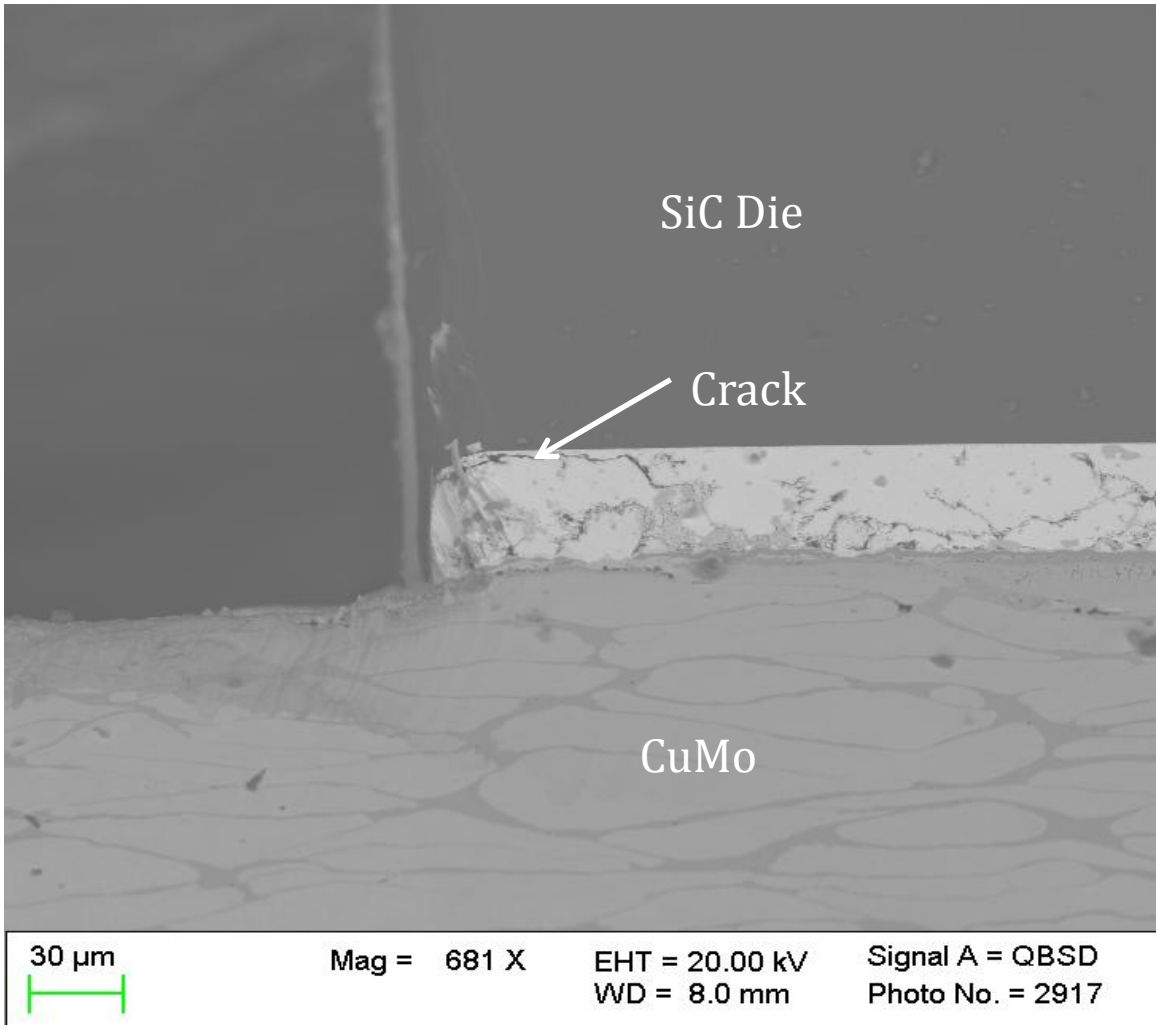
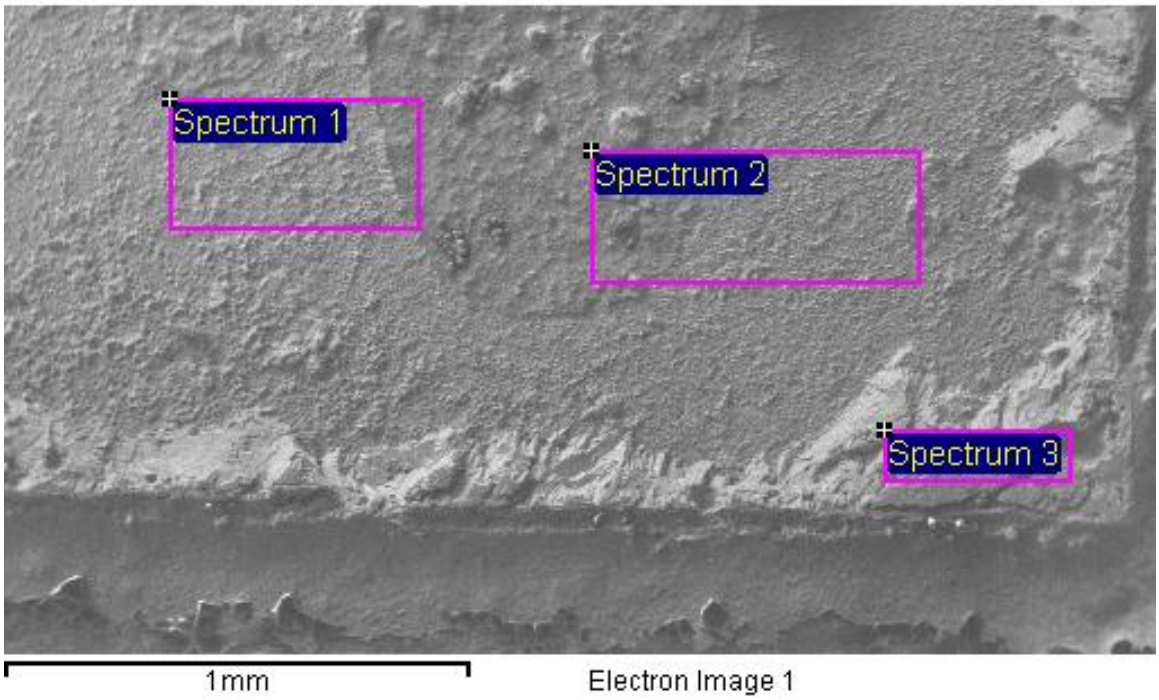


Figure 4.56 SEM Cross Section Image of a Sample after 1000 Thermal Cycles.



Spectrum	Ni	Cu	Sn	Au	Bi
Spectrum 1	26.40	1.27	10.40	2.23	59.70
Spectrum 2	24.04	3.88	10.33	3.51	58.24
Spectrum 3					100

Figure 4.57 SEM Image and Elemental Analysis of Substrate-side Fracture Surface after 1000 Thermal Cycles.

4.7.2 Die Attach on Ag finish DBC

From the previous study, we know that for die attach on Au/Ni finish DBC, there's an initial decrease in die shear strength during aging. The analysis reveals the decrease was caused by the formation of Ni_3Bi during aging. Ni comes from the substrate. Therefore, Ag finish DBC without Ni was chosen to conduct a new set of reliability tests.

4.7.2.1 High Temperature Storage Test

Assembled test vehicles were stored at 200°C in air with samples removed at scheduled intervals for shear testing. The shear test results are shown in Figure 4.58. There is a slight decrease (~10%) in average shear strength during the first 100 hours, then the shear strength remained relatively constant through 2000 hours of aging.

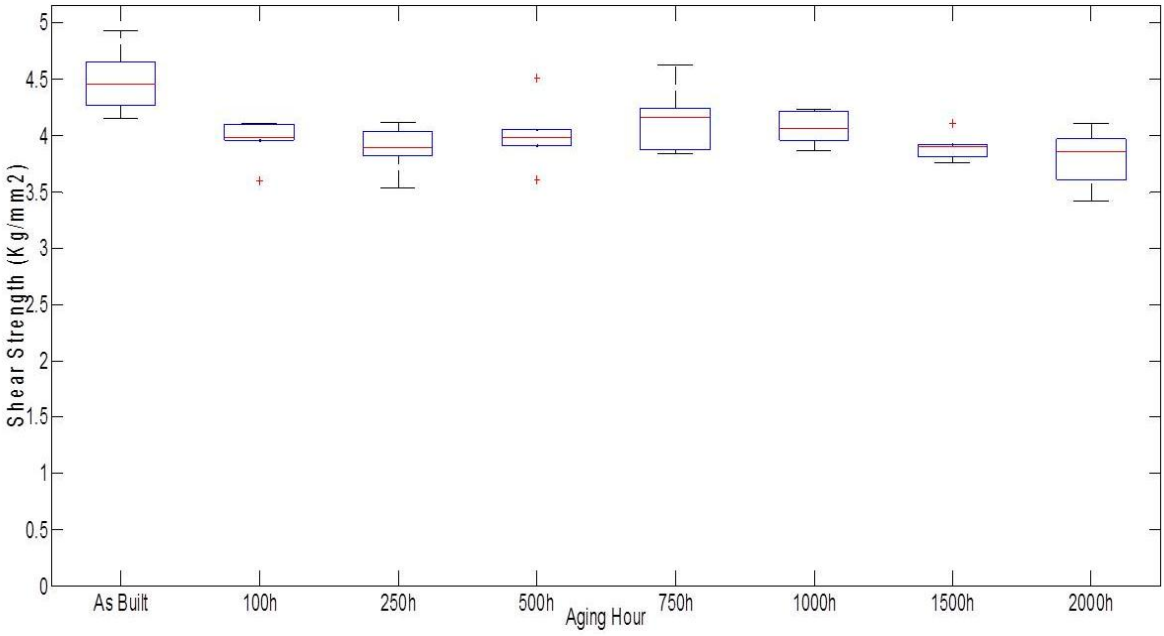


Figure 4.58 Die Shear Strength as a function of Aging at 200°C.

Figure 4.59 is an image of the solder-to-substrate interface of the solder joint after 100 hours of aging at 200°C. The image is very similar to the initial condition. With the Sn consumed during the initial reflow, there is no further intermetallic growth at this interface. Figure 4.60 is an SEM and EDS analysis of a 100 hour aged sample at the solder-to-die interface. Bi_3Ni has formed between the SiC die and the initial Ni_3Sn_4 intermetallic.

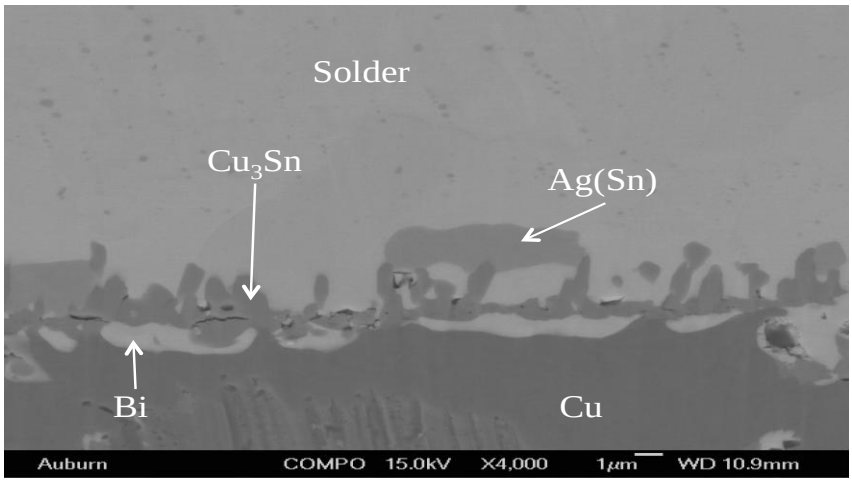
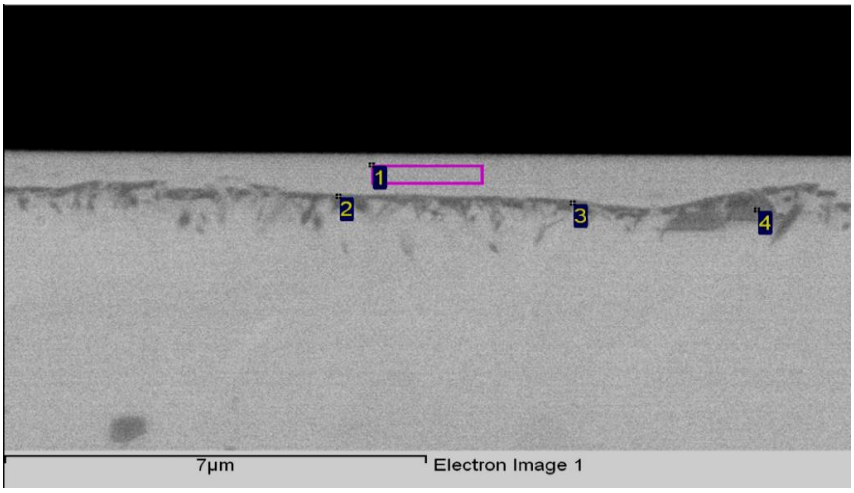


Figure 4.59 SEM Image of Solder-to-Substrate Interface after 100 Hours Aging at 200°C



Location	Ni	Ag	Sn	Bi
1	25.7	0.0	0.0	74.3
2	46.9	0.0	53.1	0.0
3	41.0	0.0	59.0	0.0
4	0.0	90.8	9.2	0.0

Figure 4.60 SEM Image and EDS Analysis (atomic %) of Solder-to-Die Interface after 100 Hours Aging at 200°C.

Figure 4.61 is a higher magnification of the solder. The Ag particles have grown in size and the network is less pronounced as compared to Figure 4.33.

Analysis of the fracture surfaces (Figure 4.62) of 100 hours aged samples after die shear revealed Cu on the substrate side indicating the failure occurred near the solder-to-Cu_3Sn interface. This was confirmed by examination of die and substrate cross sections after die shear. Sn was not detected by EDS as the expected Sn concentration would be near the system detection limit.

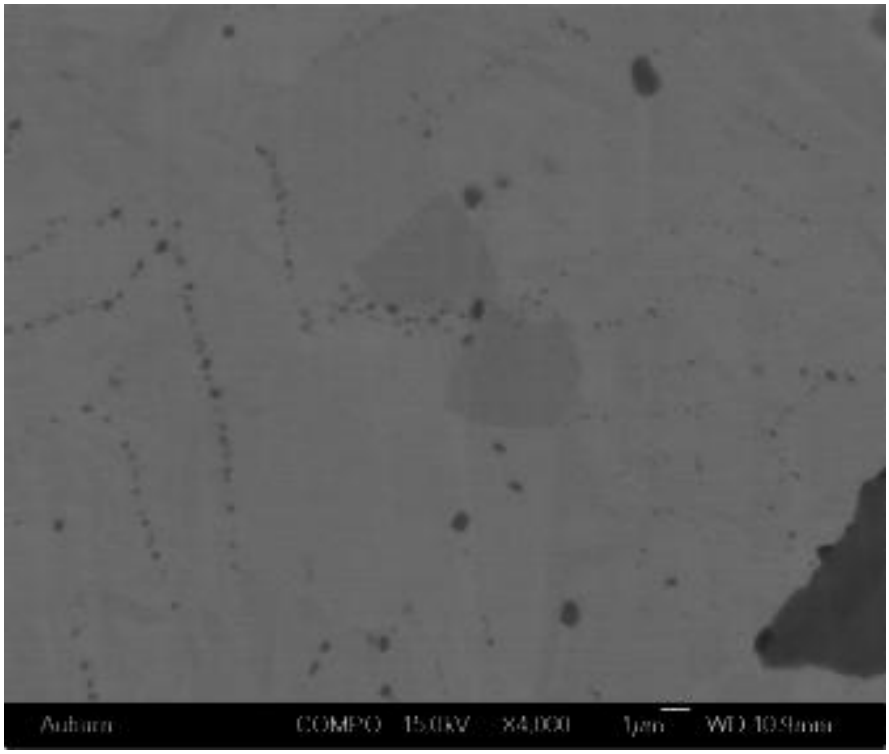
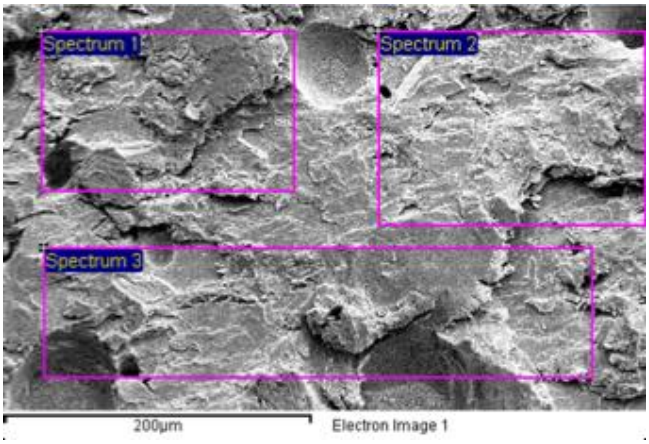
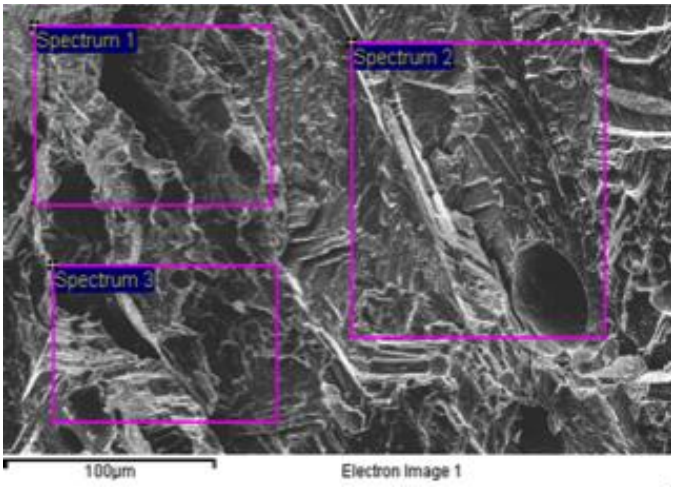


Figure 4.61 Higher Magnification Image of Solder after 100 Hours Aging at 200^{o}C.



Location	Cu	Ag	Sn	Bi
1	0.0	4.6	0.00	95.4
2	0.0	4.9	0.00	95.1
3	0.0	6.7	0.00	93.3

(Die Side)



Location	Cu	Ag	Sn	Bi
1	3.9	9.8	0.00	86.3
2	3.1	5.6	0.00	95.3
3	5.6	5.8	0.00	88.6

(Subtrate Side)

Figure 4.62 SEM and EDS Analysis (atomic %) of Fracture Surfaces after 100 Hours of Aging at 200^{o}C and Die Shear Testing

Figure 4.63 is a cross section of a sample after 2000 hours aging at 200°C. The image is very similar to the 100 hour cross section. The Ag particles continued to grow and the Ag particle network disappeared. The die shear failures were at the Cu_3Sn-to-solder interface as shown by fracture surface analysis (Figure 4.64). This was confirmed by examining cross sections of sheared die and substrates.

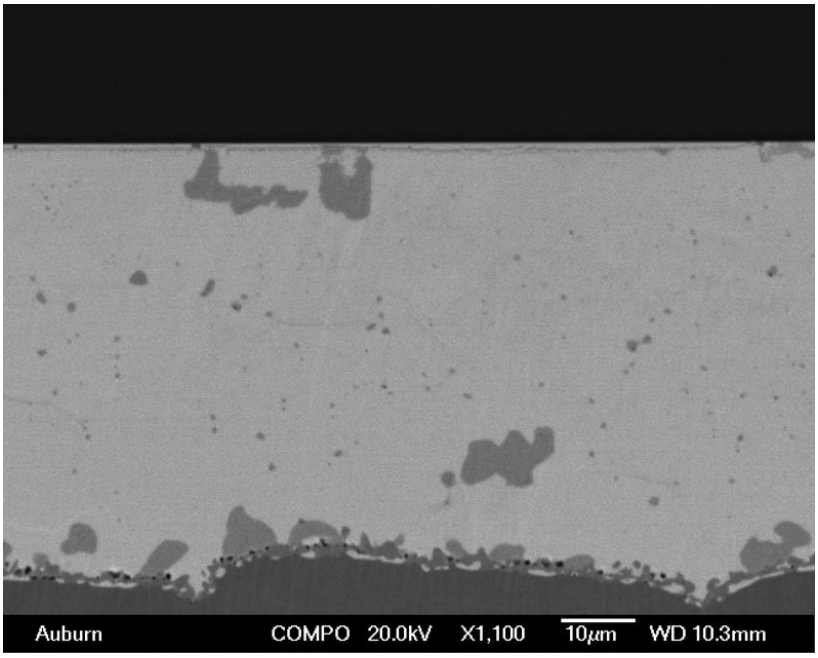
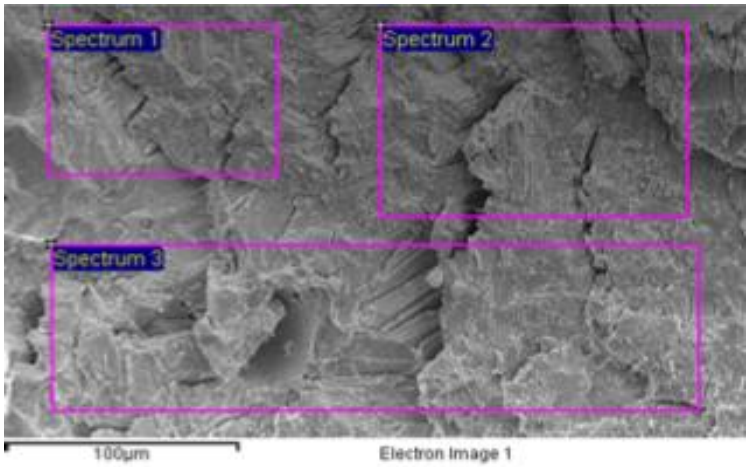
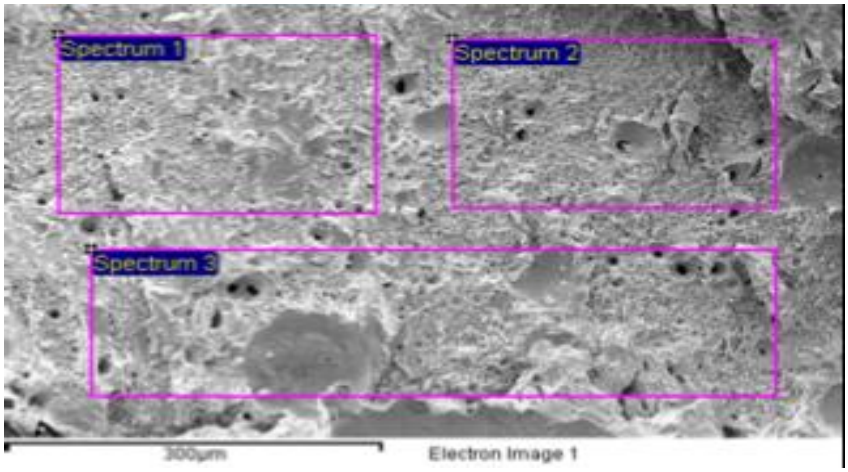


Figure 4.63 Cross Section of Solder Joint after 2000 Hours Aging at 200°C.



Location	Cu	Ag	Sn	Bi
1	0.0	7.6	0.0	92.4
2	0.0	8.5	0.0	91.5
3	0.0	8.7	0.0	91.3

(Die Side)



Location	Cu	Ag	Sn	Bi
1	15.7	10.4	5.5	68.4
2	21.6	15.6	5.5	57.3
3	14.8	13.2	5.3	66.7

(Substrate Side)

Figure 4.64 SEM and EDS Analysis (atomic %) of Fracture Surfaces after 2000 Hours Aging at 200^{o}C and Die Shear Testing

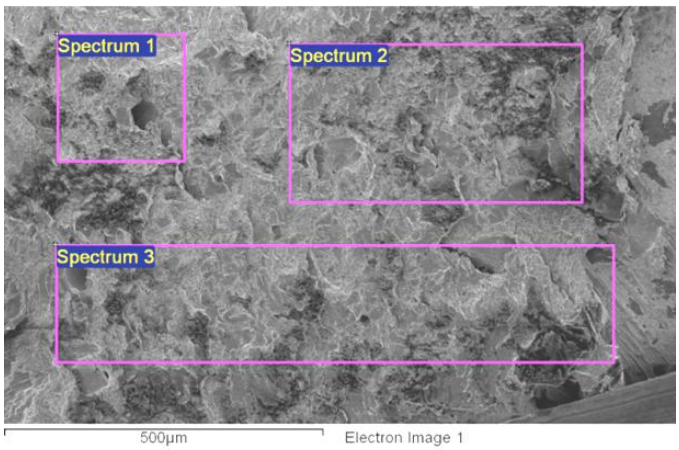
4.7.2.2 Thermal Cycling

Test samples were thermal cycled between -55^{o}C and +195^{o}C. Samples were removed periodically for die shear testing. The die shear results are presented in Table 4.2. Shear force entered as > 4kg/mm^2 indicates the die was not sheared at the test limit of 100kg shear force. While there is a decrease in shear strength with cycling, after 1000 thermal cycles the shear strength is quite high when compared to MIL-STD-883, Method 2019.7

Table 4.2 Thermal Cycle Die Shear Results in kg/mm^2

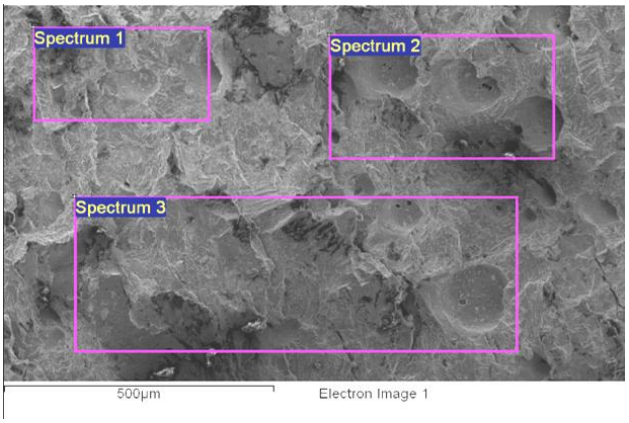
As Built	100 Cycles	250 Cycles	500 Cycles	1000 Cycles
>4	>4	>4	>4	3.64
>4	>4	>4	>4	3.55
>4	>4	>4	>4	2.86
>4	>4	3.20	3.81	3.41
3.92	3.64	3.64	3.70	3.29
3.81	3.79	3.73	3.86	3.70
3.92	3.85	3.49	3.77	3.10
3.87	3.81	3.85	3.75	3.21

Figure 4.65 shows the fracture surface and elemental analysis of one of the as-built samples that sheared during die shear testing. The failure was in the solder. The presence of Cu in Location 3 on the substrate side indicates the fracture is near the Cu_3Sn layer.



Location	Cu	Ag	Sn	Bi
1	0.0	4.6	0.0	95.4
2	0.0	3.5	0.0	96.5
3	0.0	3.3	0.0	96.7

Die Side



Location	Cu	Ag	Sn	Bi
1	0.0	3.7	0.0	96.3
2	2.0	3.7	0.0	94.3
3	0.0	3.7	0.0	96.3

Substrate Side

Figure 4.65 Fracture Surface and Elemental Analysis of a Sheared As-built Thermal Cycle Sample

Figure 4.66 is a cross section of a sample after 1000 thermal cycles. The crack extends in approximately 100μm.

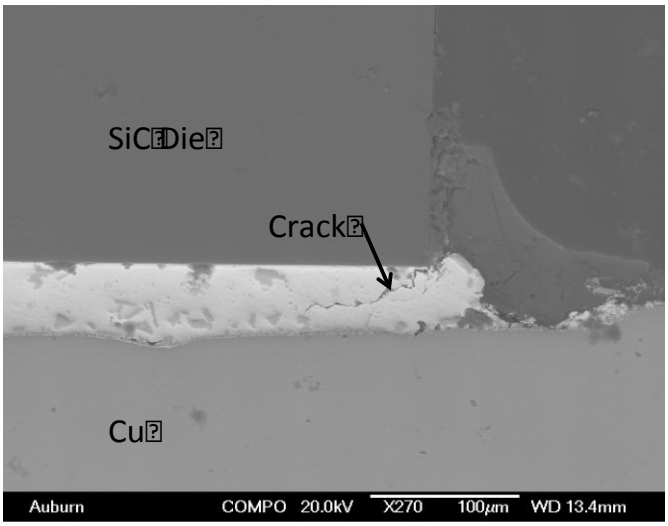


Figure 4.66 Cross Section of Sample after 1000 Thermal Cycles

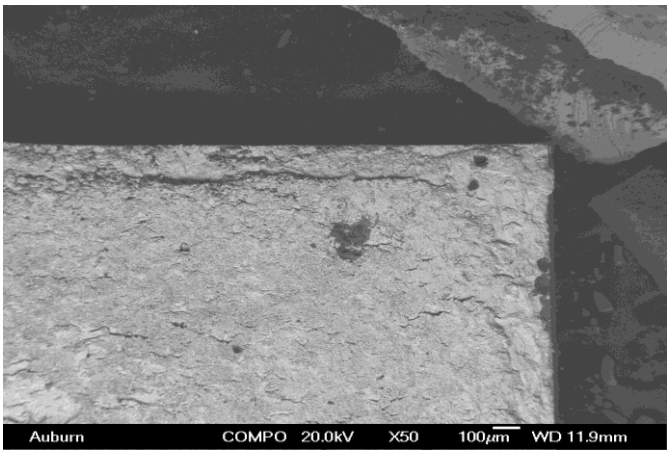


Figure 4.67 Die Side Fracture Surface after Die Shear of a Sample Thermal Cycled 1000 times

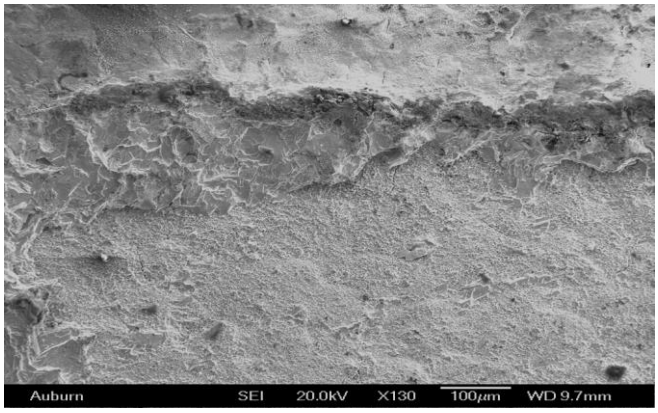
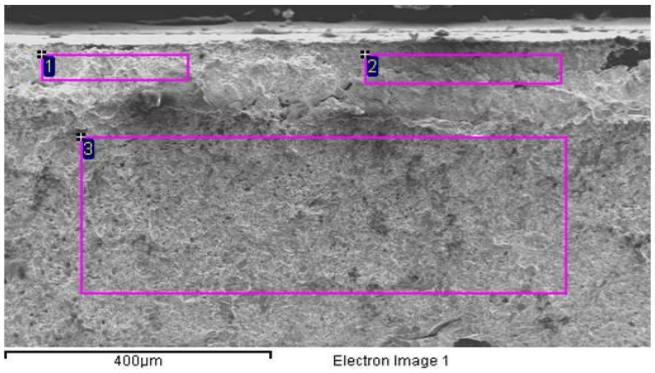


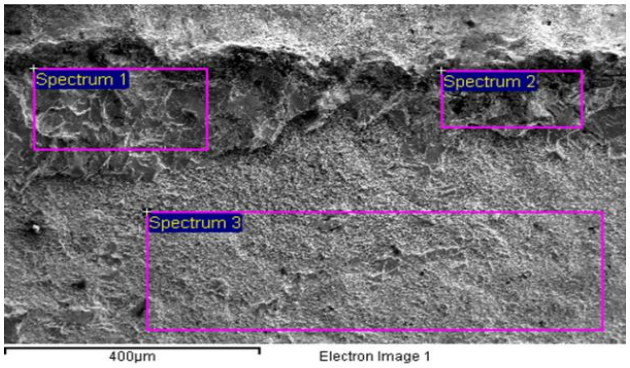
Figure 4.68 Substrate Side Fracture Surface after Die Shear of a Sample Thermal Cycled 1000 times

Figure 4.67 and 4.68 are images of the fracture surfaces after die shear. Figure 4.69 shows the elemental analysis. The failure surfaces around the perimeter of the die attach are in the solder and correspond to the crack in the solder resulting from thermal cycling. The failure surfaces in the interior of the die attach area are at the Cu_3Sn layer as evidenced by the presence of Cu and Sn on both the die and the substrate failure surfaces. Examination of fracture cross sections confirmed the interior failures were at the Cu_3Sn-to-bulk solder interface with some Cu_3Sn particles on the die side of the fracture. Thus, thermal cycling produced cracks in the bulk solder at the perimeter. Application of mechanical force during shear testing resulted in failure at the Cu_3Sn-to-bulk solder interface, very similar to the aged samples. From the measurements of the fracture surfaces after 1000 thermal cycles, it is estimated approximately 8% of the die attach area was cracked.



Location	Cu	Ag	Sn	Bi
1	0.0	7.0	0.0	93.0
2	0.0	0.0	0.0	100
3	15.0	6.3	6.8	71.9

(a) Die side



Location	Cu	Ag	Sn	Bi
1	0.0	5.2	0.00	94.8
2	0.0	18.7	3.8	77.5
3	58.9	4.1	17.3	19.7

(b) Substrate Side

Figure 4.69 SEM and EDS Analysis (atomic %) of Fracture Surfaces after 1000 Thermal Cycles and Die Shear Testing

4.7.3 Die/Resistor Attach on Thick Film Substrates

The thick film substrates with 2mm x 2mm SiC die were aged at 200^{o}C in air. Periodically samples were removed and shear tests were performed to characterize high

temperature storage performance of the die attach. Eight samples were sheared at each time interval. The die shear results were plotted in Figure 4.70 and Figure 4.71. For thick film Ag metalized samples, the shear strength was relatively constantly staying around 4kg/mm^2 through 2000 hours aging. The failure mode was at the interface of the Ag thick film and alumina substrate. The failure mode didn't change from initially through 2000 hours aging. After 1000 hours aging at 200^{o}C, the average shear strength exceeds MIL-STD-883, Method 2019.7 by more than 7 times. The PdAg samples had a decrease in shear strength during the first 750 hours of storage; the shear strength remained stable during the remainder of the test.

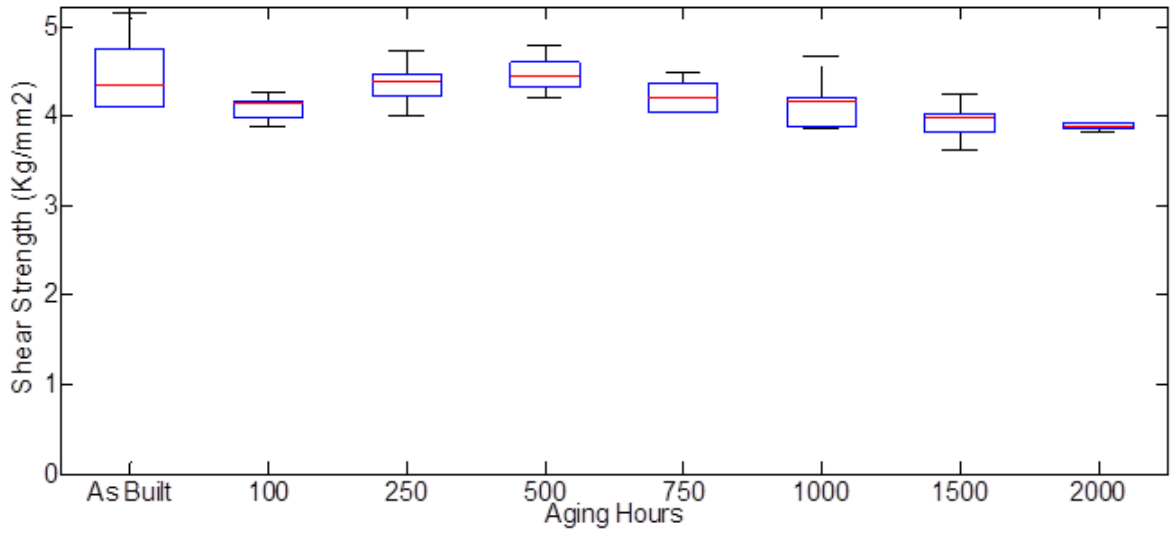


Figure 4.70 Shear Test Results for SiC Die Attached to Thick Film Ag Substrates as a Function of Storage Time at High Temperature

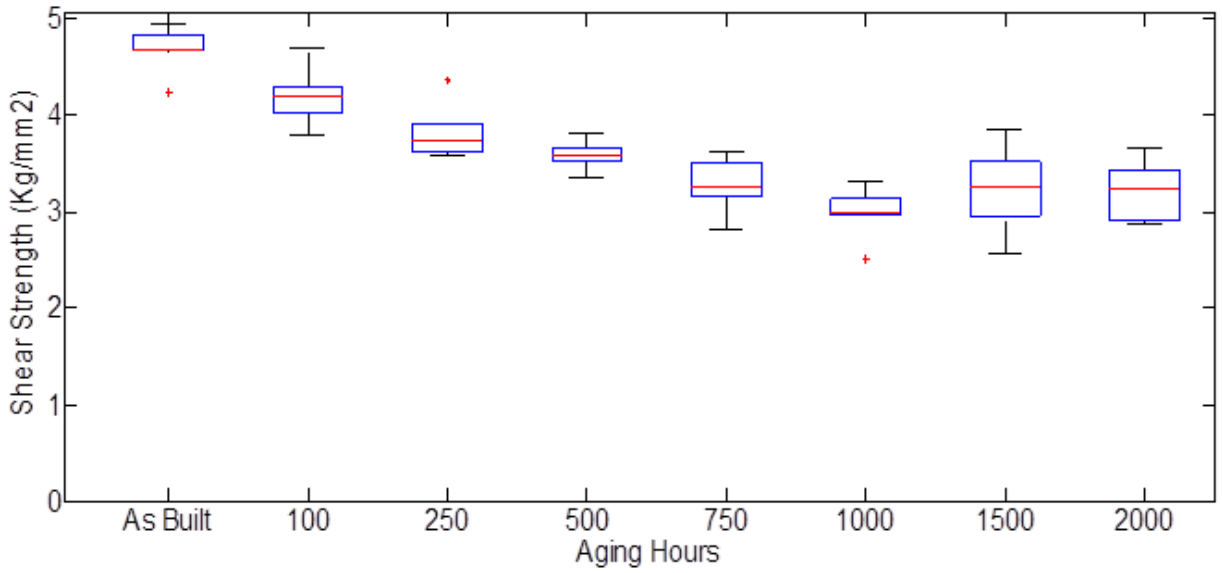


Figure 4.71 Shear Test Results for SiC Die Attached to Thick Film PdAg Substrates as a Function of Storage Time at High Temperature

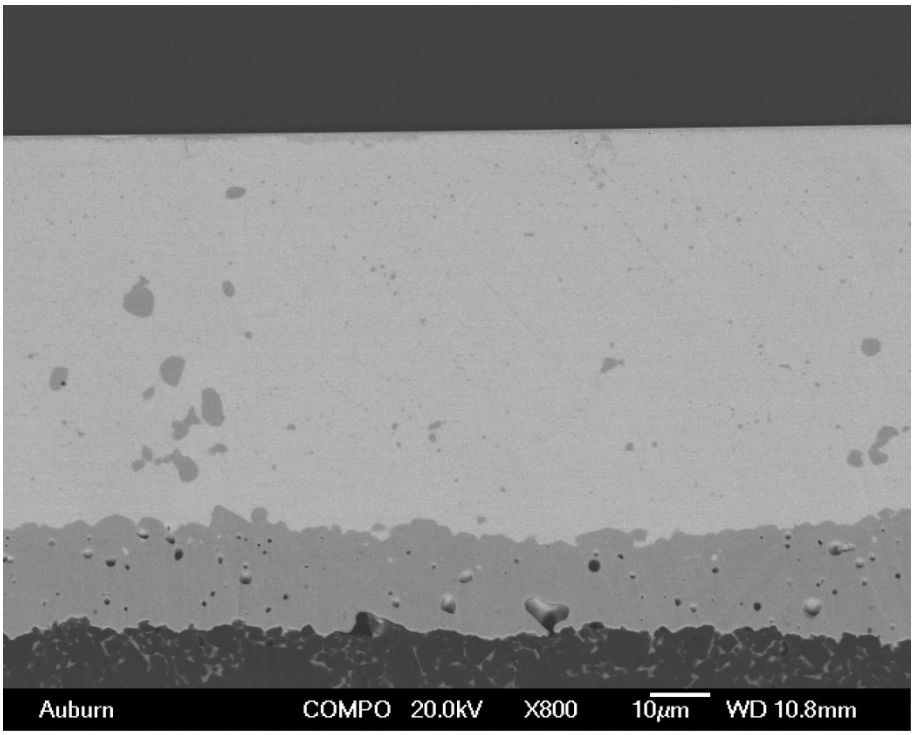
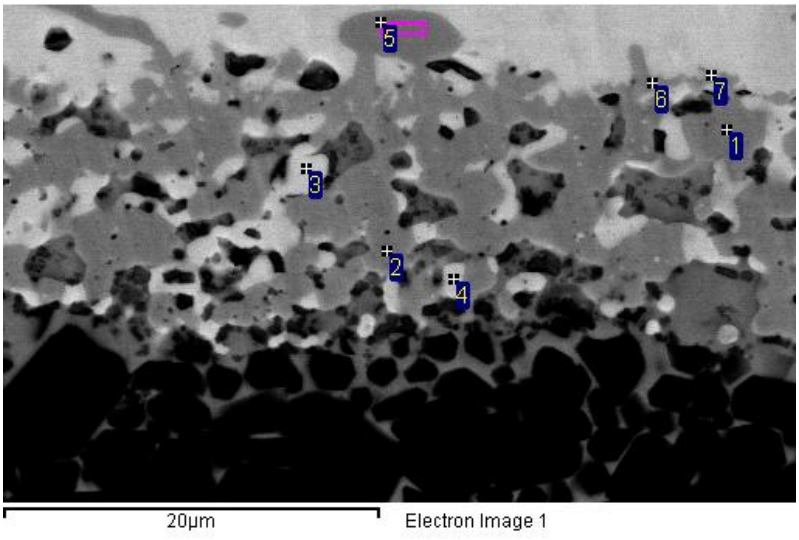


Figure 4.72 SEM Cross Section Image of Die Attach on Thick Film Ag Substrate after 2000 Hours at 200°C

Cross-sectional analysis of 2000 hour aged thick film Ag samples (Figure.4.72) exhibited no noticeable change compared to as built samples. The Sn did not diffuse into the Ag layer as is typical with high Sn containing Sn-Ag-Cu (SAC) lead-free solders.

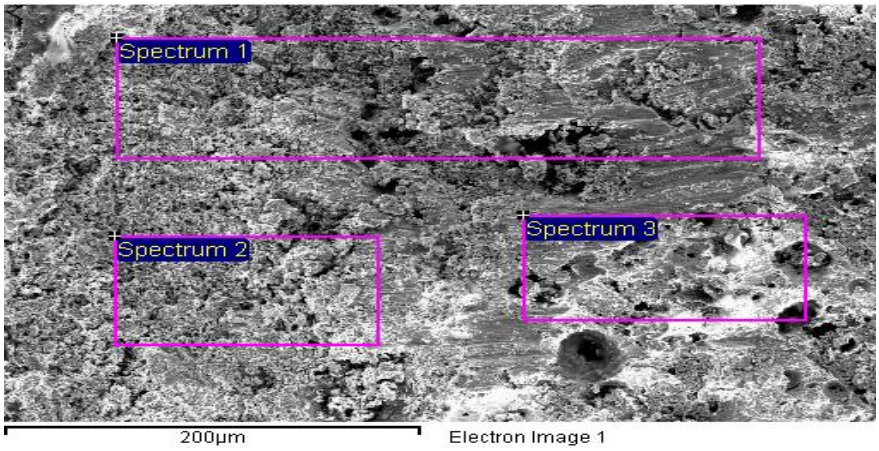
Figure 73 is an SEM image and EDS analysis of the PdAg thick film layer after 2000 hours of aging. There is no Pd left in the thick film layer, only regions of 100% Ag and 100% Bi. The Pd has diffused into the bulk solder, forming Bi_2Pd. Bi has diffused into the thick film layer, minimizing void formation. Locations 6 and 7 approximately correspond to Pd_2Sn.



Location	Pd	Ag	Sn	Bi
1	0.00	100.00	0.00	
2	0.00	100.00	0.00	
3	0.00		0.00	100.00
4	0.00	-	0.00	100.00
5		100.00	0.00	
6	63.8		36.2	
7	62.3		37.7	

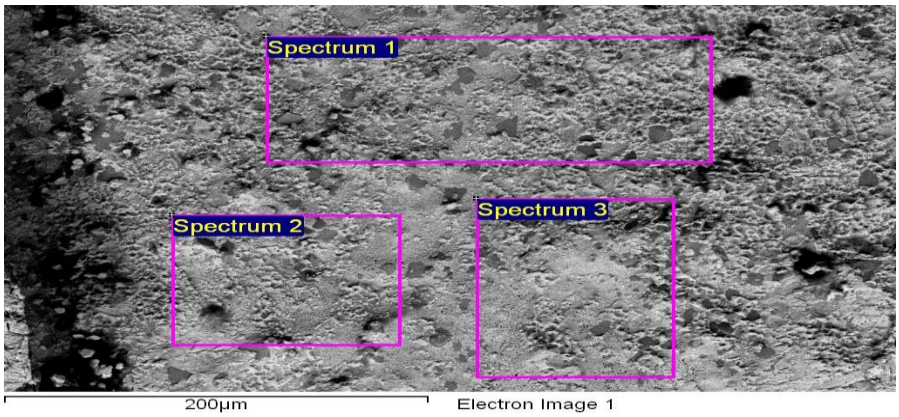
Figure 4.73 SEM Image and Elemental Analysis of PdAg Metallization after 2000 hours of High Temperature Storage

Figure 4.74 shows the fracture surface after shear testing of a 500 hours aged thick film PdAg sample. From the EDS results, it was observed the fractures occurred in the solder.



Spectrum	Pd	Ag	Sn	Bi	Total
Spectrum 1	8.43	19.15	4.60	67.82	100.00
Spectrum 2	7.51	27.21	3.95	61.34	100.00
Spectrum 3	14.36	9.64	6.64	69.36	100.00

(a) Substrate Side



Spectrum	Pd	Ag	Sn	Bi
Spectrum 1	9.62	18.45	0.00	71.93
Spectrum 2	8.67	12.16	0.00	79.17
Spectrum 3	8.57	21.92	0.00	69.51

(b) Die Side

Figure 4.74 SEM and EDS Analysis (atomic %) of Fracture Surfaces after 2000 Aging and Die Shear Testing

Similar shear results were obtained from the resistor attach samples as shown in Figure 4.75 and Figure 4.76. The average resistor shear force on thick film Ag decreased from 7.78kg to 6.56kg after the first 100 hours aging then stabilized at around 5kg through 2000 hours aging at 200^{o}C in air. The failure mode was at the interface of the thick film Ag and alumina substrate. For resistor attach on PdAg, the average shear strength decreased with aging time, and drop to 2.96kg after 2000 hours aging at 200^{o}C. The failure mode was in the solder.

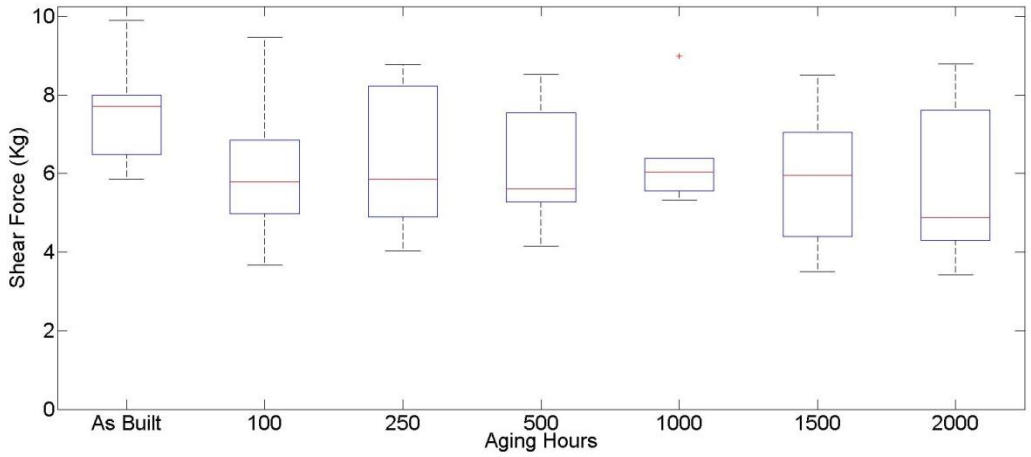


Figure 4.75 Shear Test Results for Resistors Attached to Thick Film Ag Substrates as a Function of Storage Time at High Temperature

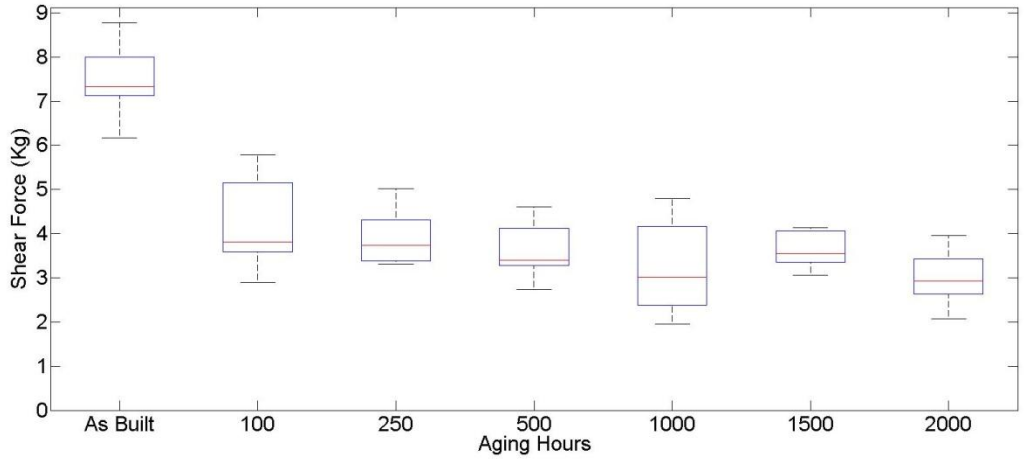


Figure 4.76 Shear Test Results for Resistors Attached to Thick Film PdAg Substrates as a Function of Storage Time at High Temperature

CHAPTER 5 CONCLUSIONS AND FUTURE WORK RECOMMANDATION

5.1 Die Attach Using LPT Bonding

Liquid phase transient bonding with AuSn preform provides a feasible die attach method for high temperature applications up to 500^{o}C. Die attach with AuSn preforms with excess Au provided by the die and substrate metallization shows good mechanical reliability for high temperature storage. Both single and double prints of the PtPdAu thick film layers were evaluated. The shear test results after 2000 hours aging at 500^{o}C shows there is no significant difference between the single and double prints. The decreasing in shear strength with aging is related to Sn diffusion into glass region in the thick film.

The assembly process for two test circuit boards using AuSn LPT bonding techniques for 300^{o}C application were developed. Thick film technology for fabrication of multichip modules(MCM) capable of 300^{o}C was explored. The MCM fabrication process includes passive component bonding and die attach using AuSn. The DIP socket board had contact stability beyond 3000 hours at 300^{o}C.

5.2 Die Attach Using Gold Sintering

The patterned gold die attach technology using micro-scale gold paste has been evaluated and showed the potential for applications at 500^{o}C. The patterns on both the thin film die metallization and the thick film substrate has successfully created controlled voiding which allows the burnout gas to escape during the firing process. The shear force test results after high temperature storage increased 90.41% compared to the initial shear force. Continued sintering of the Au atoms increased the strength of bonding during the 500^{o}C storage. While the die shear

strength of the micro-scale particle Au die attach was less than with the LPT AuSn, it meets the MIL-STD-883 die attach requirement and should be stable for use to at least 700^{o}C.

5.3 Die Attach Using AgBiX Solder Paste

The use of AgBiX solder on different substrates was studied. High temperature storage and thermal cycling experiments were performed and described. The solder paste has a controlled amount of Sn, limiting the amount of Sn intermetallic formation. This alloy has been used to assemble SiC test die to ceramic substrates with Ni/Au finish direct bond copper (DBC),Ni/Au finish reactive brazed CuMo, silver finish DBC, thick film Au and PtPdAu, thick film PdAg and thick film Ag. Surface mount chip resistors have also been attached to thick film metallized substrates. The assembly process and initial shear strength test results were presented. Assemblies have also been subjected to thermal cycling -55^{o}C to +195^{o}C) and high temperature (200^{o}C) storage.

For Ni/Au finish DBC substrate, the $NiBi_3$ intermetallic layer thickness grows with high temperature aging and the fracture interface during die shear shifts from the solder-to-intermetallic interface to the intermetallic-to-Cu interface. This is the main cause of decreasing die shear strength with high temperature exposure. Once all of the Ni is consumed, intermetallic growth stops and the die shear strength remains relatively stable with further aging.

The $NiBi_3$ intermetallic also grows during thermal cycling to +195^{o}C and there is a steady decrease in shear strength with increasing number of cycles. Fatigue cracks resulting from the thermal cycling are observed in the solder layer near the perimeter of the die. In the die shear test, the bulk of the failure is in the $NiBi_3$ intermetallic near the substrate interface. This is the same as was observed in the high temperature aged samples.

For die attach on Ag finish DBC substrate, the shear strength, failure mode and microstructure are relatively stable with aging from 100 to 2000 hours at 200^{o}C. Thermal cycling produces fatigue cracks (~100μm after 1000 thermal cycles) along the perimeter of the die attach in the solder layer. Mechanical fracture of thermal cycled samples by die shear, results in failure at the Cu_3Sn layer, similar to the die shear of aged samples. This indicates that except for the crack, the thermal cycling does not significantly damage the bulk solder. Use of Ag rather than Ni/Ag as the surface finish eliminates the formation of Bi_3Ni and results in better high temperature aging shear test results.

For thick film metalized substrates, AgBiX solder paste has shown excellent promise as a replacement for high lead solders on Ag thick film metallization for applications to 200^{o}C. Formation of Bi_2Pd intermetallic reduces the shear strength (force) of die and resistors assembled to PdAg thick film metallization. The PtPdAu thick film substrates had a wetting issue with this solder paste. The Au thick film substrates had Au dissolution and a resulting adhesion issue.

5.4 Future Work Recommendation

Based on the results presented in this dissertation, some recommendations for future work are as follows:

- For die attach using metal alloy die attach material, besides AuSn, different die attach material may be used, such as Au-Ge preforms or Au-Ge paste. Paste is preferred for assembling multichip modules.
- For AgBiX solder paste, this is a very promising solder paste for application of 200oC. In the Ni:B/Au DBC substrates, Bi_3Ni intermetallic formation was found and caused a decrease in the shear strength during high temperature aging. The reliability

with thinner Ni on the substrate would be interested to explore. Will Bi_3Ni formation change with Ni:P/Au DBC substrates? Further understanding of the mechanism of Bi_3Ni formation can help to improve the reliability performance of the solder joint.

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