INTEGRATION OF THIN FLIP CHIP IN LIQUID CRYSTAL POLYMER BASED FLEX

Except where reference is made to the work of others, the work described in this dissertation is my own or was done in collaboration with my advisory committee. This dissertation does not include proprietary or classified information

Zhenwei Hou

Certificate of Approval:

Thomas A. Baginski
Professor
Electrical and Computer Engineering

R. Wayne Johnson, Chair
Ginn Professor
Electrical and Computer
Engineering

Thaddeus A. Roppel
Associate Professor
Electrical and Computer Engineering

Jeffrey W. Fergus
Associate Professor
Materials Engineering

Stephen L. McFarland
Dean
Graduate School

INTEGRATION OF THIN FLIP CHIP IN LIQUID CRYSTAL POLYMER BASED FLEX

Zhenwei Hou

A Dissertation

Submitted to

the Graduate Faculty of

Auburn University

in Partial Fulfillment of the

Requirements for the

Degree of

Doctor of Philosophy

Auburn, Alabama
May 11, 2006

INTEGRATION OF THIN FLIP CHIP IN LIQUID CRYSTAL POLYMER BASED FLEX

Zhenwei Hou

Permission is granted to Auburn University to make copies of this dissertation at its discretion, upon the request of individuals or institutions at their expense. The author reserves all publication rights.

Signature of Author

Date of Graduation

VITA

Zhenwei Hou, son of Gengyuan Hou and Yueqin Chen, was born on November 26, 1964, in Shanghai, an eastern coastal city in the People’s Republic of China (PRC). In 1996 he enrolled in Graduate School at Auburn University, Alabama and married Unchin Cho in 2000. He received two Master of Science degrees in Textile Science and Electrical and Computer Engineering in 1997 and 2003, respectively. He then continued his education in the Ph.D. program in the Department of Electrical and Computer Engineering of Auburn University.

DISSERTATION ABSTRACT

INTEGRATION OF THIN FLIP CHIP IN LIQUID CRYSTAL POLYMER BASED FLEX

Zhenwei Hou

Doctor of Philosophy, May 11, 2006
(MS ECE, Auburn University, 2003)
(MS TS, Auburn University, 1997)

111 Typed Pages

Directed by R. Wayne Johnson

Thin embedded active assemblies have been developed that combine a lower profile and high functional density (per volume) with a flexible appearance, meeting the demands for the miniaturization of electronic products. The assembly investigated in this study was a thin flip chip embedded in liquid crystal polymer (LCP) based flex. The focus of this work was on establishing a process route to enable the integration of thin integrated circuit (IC) assemblies. The flexible assembly consists of three primary elements: the thin IC, the flexible substrate and small interconnections between the die and the substrate. Bending of the delicate thin dies and warping of the LCP substrate generated many new challenges for the assembly process, which are not an issue in the

assembly of conventional packages. The research work reported here was divided into three separate steps: die thinning, flexible substrate fabrication and assembly.

The preparation of the 50μm thick silicon dies included die thinning, thinned die transfer and gold stud bumping. Die thinning was accomplished by backside mechanical grinding. A quasi-waferscale thinning process, where shallow grooves were diced in the wafer before thinning, gives a high yield of quality thinned dies compared to the individual die thinning process which was employed in the early investigations. The die transfer was performed by mounting the delicate thin die on a thick flat handling die with adhesive, offering two benefits: easy handling and it maintained the thin die flat. The study of the transfer process was performed using a design of experiment approach to optimize the process. Gold stud bumps were directly applied to this transferred thin die by thermosonic bonding.

Liquid crystal polymer was used as the substrate material to provide high strength, light weight, flexibility, high melting temperature, thermal dimensional stability, and lower coefficient of thermal expansion (8 ppm/°C). A backside assembly design substrate was used for this research. The substrate fabrication was addressed in terms of three main processes: bottom copper circuit formation, via etching and copper surface finishing.

A thermal compression approach for the assembly of thin flip chip die onto the LCP flex was also investigated. The die was directly thermocompression bonded to the LCP substrate. This direct die attachment eliminates the need for underfill, further decreasing the overall height and improving the flexibility of the package.

A SOI CMOS based operational amplifier circuit was assembled to evaluate the electrical performance of this embedded membrane structure. The results demonstrated that this structure can withstand a large mechanical deformation with little impact on electrical performance.

ACKNOWLEDGEMENTS

The author acknowledges and extends his gratitude for the financial support from Jet Propulsion Laboratory (JPL) of California Institute of Technology. In particular, the cooperative support from Ms. Tan Zhang, his project coworker, and the valuable help from Mr. Mike Palmer, the manager of Auburn University Laboratory for Electronics Assembly and Packaging (LEAP), are deeply appreciated. The author would also like to thank his wife for her patience and continued support during the course of this work.

Style manual or journal used American Institute of Physics, Style Manual

Computer software used Microsoft Office 2003

TABLE OF CONTENTS

LIST OF TABLES……………………………………………………………………xi

LIST OF FIGURES…………………………………………………………………xii

CHAPTER 1 INTRODUCTION 1

CHAPTER 2 LITERATURE REVIEW 6

2.1 SILICON THINNING.. 7

2.1.1 Mechanical Surface Grinding 8
2.1.2 Chemical and Mechanical Polishing 10
2.1.3 Wet Chemical Etching.. 10
2.1.4 Plasma Etching 11

2.2 FLEXIBLE SUBSTRATE MATERIALS 14

2.2.1 Polyester 16
2.2.2 Polyimides 18
2.2.3 Liquid Crystal Polymers... 20

2.3 INTEGRATION OF FLEXIBLE ASSEMBLIES... 25

2.3.1 Reflow Soldering.. 29
2.3.2 Thermode Bonding 30
2.3.3 Adhesive Bonding 31
2.3.4 Isoplanar Interconnection 32

2.4 SUMMARY 33

CHAPTER 3 PREPARATION OF THIN SILICON DIE AND TRANSFER OF THINNED DIE... 34

3.1 EARLY WORK.. 34

3.2 DICING BEFORE THINNING PROCESS 40

3.3 TRANSFER OF THINNED TEST DIE... 41

3.4 GOLD STUD BUMPING OF TRANSFERRED DIE 47
3.5 SUMMARY 49

CHAPTER 4 PREPARATION OF FLEXIBLE LCP SUBSTRATES........ 51

4.1 OVERVIEW........ 51
4.2 FLEXIBLE SUBSTRATE PATTERNS AND MATERIALS........ 51
4.3 LCP SUBSTRATE FABRICATION PROCESS FLOW........ 53
4.3.1 Bottom Cu Trace Pattern Fabrication........ 55
4.3.2 Via Formation........ 56
4.3.3 Cu Trace Surface Finishing........ 58
4.4 SUMMARY 61

CHAPTER 5 THERMAL COMPRESSION ASSEMBLY OF THIN FLIP CHIP IN LCP FLEX........ 62

5.1 EARLY WORK........ 62
5.2 THERMAL COMPRESSION ASSEMBLY WITH GOLD-TO-GOLD INTERCONNECTIONS 67
5.2.1 Issues Related to the Assembly Process........ 68
5.2.2 Setting-Up the Thermal Compression Bonding Profile........ 69
5.3 SEALING WITH LOW MELTING TEMPERATURE LCP SHEET 72
5.4 SUMMARY 75

CHAPTER 6 ELECTRICAL PERFORMANCE OF THIN OPERATIONAL AMPLIFIER IN LCP FLEX SUBJECTED TO MECHANICAL BENDING........ 76

6.1 OVERVIEW........ 76
6.2 MATERIALS AND ASSEMBLY 77
6.3 INVESTIGATION OF THE EFFECT OF MECHANICAL BENDING ON THE ELECTRICAL PERFORMANCE OF THE OP AMP ASSEMBLY 80
6.4 SUMMARY 87

CHAPTER 7 CONCLUSIONS........ 88

CHAPTER 8 FUTURE WORK........ 90

REFERENCES........91

LIST OF TABLES

Table 2-1 Specification of Base Films for Flexible Substrates [11] 16

Table 3-1 L_8 (2^7) Orthogonal Arrays 44

Table 3-2 Two Levels of Process Parameters...45

Table 4-1 LCP Sheet Material Properties [41, 42, 43, 44, 45] 53

Table 4-2 Composition of the Nickel Electroplating Solution 60

Table 5-1 L_8 (2^7) Orthogonal Arrays 70

Table 5-2 The Two Levels of Thermal Compression Bonding Parameters 71

Table 6-1 DC/AC Electrical Performance of Embedded Op Amp in LCP Assembly 87

LIST OF FIGURES

Figure 1.1 Flowchart of Integrating Thin Die with Flexible LCP Substrate 2

Figure 1.2 The Thin Flip Chip in LCP Flex 2

Figure 1.3 Illustration of Topside Assembly and Backside Assembly 3

Figure 1.4 Cross-Section of the 50μm Thick PB8 Flip Chip in LCP Flex 4

Figure 2.1 Trends for Wafer Thickness, Wafer Diameter and Die Thickness [2]...........7

Figure 2.2 Atomic Force Micrographs (ATM) of the Surface of Silicon Wafers Subjected to 500-Grit and 2000-Grit Grindings, Respectively [4] 9

Figure 2.3 Cross-Section TEM Picture Showing Structural Defects Near the Wafer Surface after Fine Grinding [5] 9

Figure 2.4 The Chemical and Mechanical Polishing (CMP) Process [6] 10

Figure 2.5 The Wet Spin Etching Process [5] 11

Figure 2.6 The Plasma Etching of Silicon 12

Figure 2.7 The Atmospheric Downstream Plasma Etching Process [8] 13

Figure 2.8 The SEM Picture of the Surface of A Dry-Etched Silicon Wafer [8] 14

Figure 2.9 The Synthesis of Polyester 17

Figure 2.10 A Typical Manufacturing Process for Oriented Polyester Film [12] 18

Figure 2.11 Synthesis of Polyimide [14] 19

Figure 2.12 Thermotropic Liquid Crystalline Aromatic Polyesters [19] 21

Figure 2.13 Schematic of Nematic Mesophase [21] 22

Figure 2.14 Schematic of Counter-Rotating Die and Extrusion [24] 23

Figure 2.15 Dielectric Constant Variation: LCP, Polyimide and FR-4 [26] 24

Figure 2.16 Dissipation Factor Variation: LCP, Polyimide and FR-4 [26] 25

Figure 2.17 Warping of Thinned Wafer [27] 26

Figure 2.18 Elongated and Uneven Solder Joints 27

Figure 2.19 Uniform Solder Joints in 50µm Die on Polyimide 27

Figure 2.20 Schematics of Wirebonding and Flip Chip Packages 28

Figure 2.21 50µm-Thickness Flip Chips on Polyimide Substrate [28] 30

Figure 2.22 Principle of Thermode Bonding Process [34] 31

Figure 2.23 Cross Section of 40µm Pitch AuSn Thermode Bonded Assembly [34] 31

Figure 2.24 ACA Particle Trapped between Transponder IC Bump and Antenna Pad [34] 32

Figure 2.25 Isoplanar Connections [37] 33

Figure 3.1 The Top Profile of 50µm PB8 Test Die 35

Figure 3.2 Illustration of Post Die Thinning Process 36

Figure 3.3 Undercut of Die Sidewall after RIE 37

Figure 3.4 The Remaining of Silicon Fence Around the Thinned Die After the Completion of Deep Silicon RIE 37

Figure 3.5 Illustration of Pre-Die Thinning Process 38

Figure 3.6 The Top Profile of Transferred 50µm Thickness PB8 Die 39

Figure 3.7 Flowchart of Wafer Dicing before Thinning Process 41

Figure 3.8 Flowchart of The Thinned Die Transfer Process 42

Figure 3.9 Die Fractured During Stud Bumping and Entrapped Voids 43

Figure 3.10 The Main Effects Plots 46

Figure 3.11 The C-SAM Picture of Voids-Free Die Transfer with the Optimized Process 46

Figure 3.12 Topview of 50μm Thickness PB8 Die on Handling Chip 47

Figure 3.13 Cross Section of 50μm Thickness Die on Handling Chip 47

Figure 3.14 Close-up of Au Stud Bumps on the PB8 Test Die 48

Figure 4.1 Backside Design Substrate Patterns for PB8 Test Die 52

Figure 4.2 Scheme of Backside Assembly Design Substrate Fabrication 54

Figure 4.3 The Process Flowchart for LCP Substrate Fabrication 54

Figure 4.4 The Cross-section of the Vias in LCP Substrate 57

Figure 4.5 The Diagram of Electroplating System 59

Figure 4.6 Ni/Au Plated LCP Substrate 60

Figure 5.1 The Assembly Process of an Thin Die in Package with the Assistance of Sn63Pb37 Solder Paste 64

Figure 5.2 The Joints of Sn63Pb37-Gold Within the Via Wells Between the Thin Die and the LCP Substrate 65

Figure 5.3 X-Ray Image of Overflowing Solder Under Die 66

Figure 5.4 Solder Bridges Between Bottomside Traces Caused by Escaping Molten Solder 67

Figure 5.5 The Assembly Process For an Thin Flip Chip in LCP Flex with Gold-to-Gold Interconnections 68

Figure 5.6 One–Factor Effects for Four Thermal Compression Parameters 72

Figure 5.7 Cross-Section of Embedded 50μm Thick PB8 Flip Chip Package 74

Figure 6.1 The Top View of the Test Op Amp and Pad Location................................78

Figure 6.2 LCP Substrate Patterns for Test Op Amp 79

Figure 6.3 Wiring the Embedded Op Amp in LCP for Testing...................................80

Figure 6.4 Closed-Loop Testing Schematic for Measuring Input Offset Voltage.........81

Figure 6.5 Finding the Input Offset Voltage on the Unity Gain Plot 82

Figure 6.6 Testing Schematic for Measuring Common-Mode Voltage Gain 83

Figure 6.7 Transfer Characteristics of Op Amp with Common-Mode Input Voltages....83

Figure 6.8 Testing Schematic for Measuring Differential-Mode Voltage Gain....84

Figure 6.9 Transfer Characteristics of Op Amp with Differential-Mode Voltage Inputs....85

Figure 6.10 Testing Diagram for Measuring Gain Bandwidth Product....86

CHAPTER 1 INTRODUCTION

The objective of this work was to develop thin, flexible electronics by embedding semiconductors within a flexible substrate (abbreviated to flex). This technology provides a basis for conformal electronics that can be formed into 3-dimensional shapes or laminated to curved surfaces. The technology is also applicable to integration of distributed electronics in membrane antennas.

The work reported in this dissertation was divided into three phases: thin die preparation, flexible substrate fabrication and assembly, as shown in Figure 1.1. The reliability and failure analysis are to be performed by the Jet Propulsion Laboratory. Integrating a 50µm thick PB8 test die into a liquid crystal polymer (LCP) substrate was proposed in order to demonstrate the embedded die structure, shown in Figure 1.2.

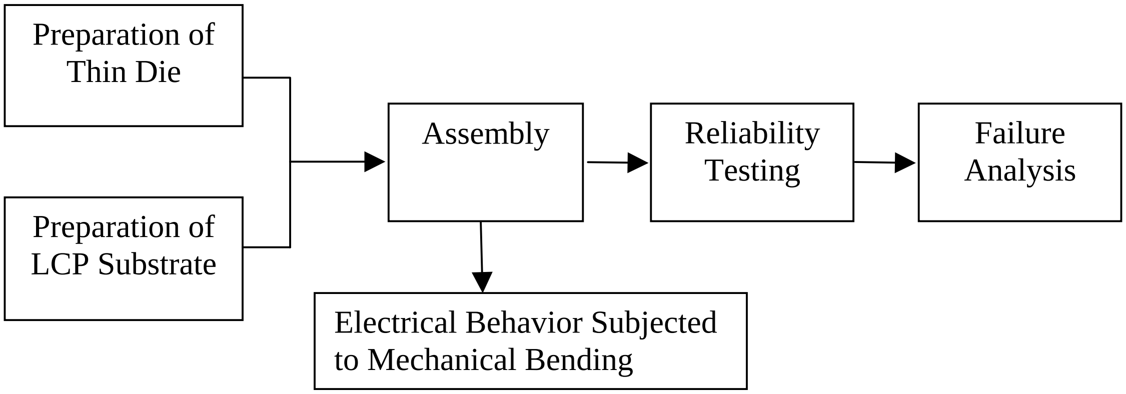

Preparation of Thin Die
Preparation of LCP Substrate
Assembly
Reliability Testing
Failure Analysis
Electrical Behavior Subjected to Mechanical Bending

Figure 1.1 Flowchart of Integrating Thin Die with Flexible LCP Substrate

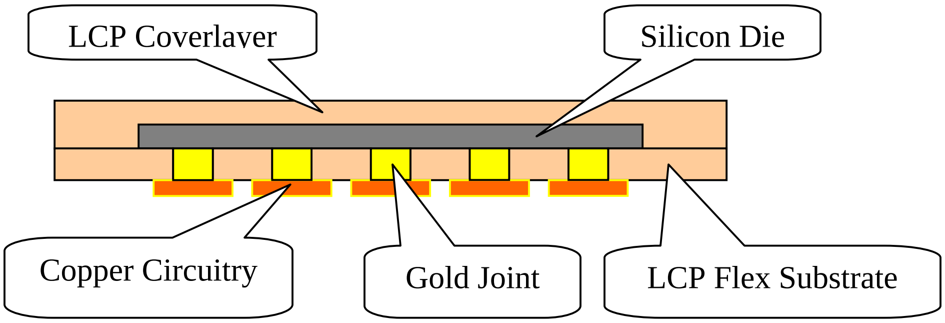
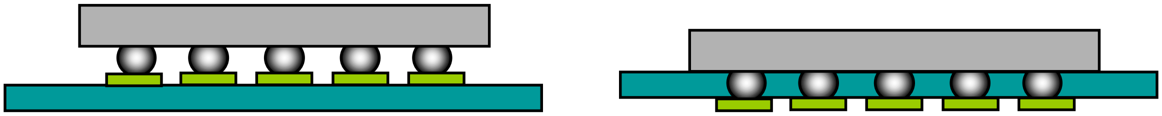


Figure 1.2 The Thin Flip Chip in LCP Flex

Thin ICs can be economically produced by mechanically grinding individual dies. However, the grinding impact often damages the thinned die edges during the thinning process, causing poor thin die quality and lowering the overall production yield. The poor quality achieved adversely affected the sequential die processing and assembly processing. Here, a modified waferscale grinding process, where the wafer was partially diced before thinning, was used. This thinning process shortens the exposure time of the die edges during grinding, resulting in both high yield and high quality.

Thin silicon dies tend to suffer from warping due to their asymmetrical structure, where the active circuit layer sits atop the bulk silicon. This curvature increases with decreasing die thickness and creates problems for die attachment and the formation of uniform interconnections. Thin silicon is too fragile to be directly handled and thus also causes difficulties for the assembly process. In this work, a die transfer technique was developed where the thin die was mounted on a thick flat handling die with adhesive prior to bumping and assembly. As a result, the transferred die could be directly handled through out the processing.

The total height is an important index for thin assemblies. A backside assembly substrate design was selected in order to reduce the overall thickness. In backside assembly, the vias are etched though the LCP, substrate dielectric material, exposing the underside of the copper pads (backside design). The flip chip die is assembled from the side opposite the copper pattern (Figure 1.3b). The LCP substrate was fabricated with clean room fabrication processes, such as photolithography, wet etching, dry etching and plating.



(a) Topside Assembly (b) Backside Assembly

Figure 1.3 Illustration of Topside Assembly and Backside Assembly

For this research, the thermal compression assembly of embedded thin die was performed with gold-to-gold interconnections. The direct silicon-LCP lamination eliminated the need for underfill. Underfill is an adhesive used to fill the gap between the die and the substrate which is widely used in conventional flip chip assemblies. Direct lamination reduced the overall thickness of the assembly and eliminated the loss of flexibility due to the rigidity of typical underfills. A thermal compression bonding profile was developed based on careful consideration of the formation of interconnections and the silicon-LCP lamination bonding during the process. After hot lamination with an LCP coverlayer, the 50µm PB8 flip chip in LCP flex was successfully achieved (Figure 1.4).

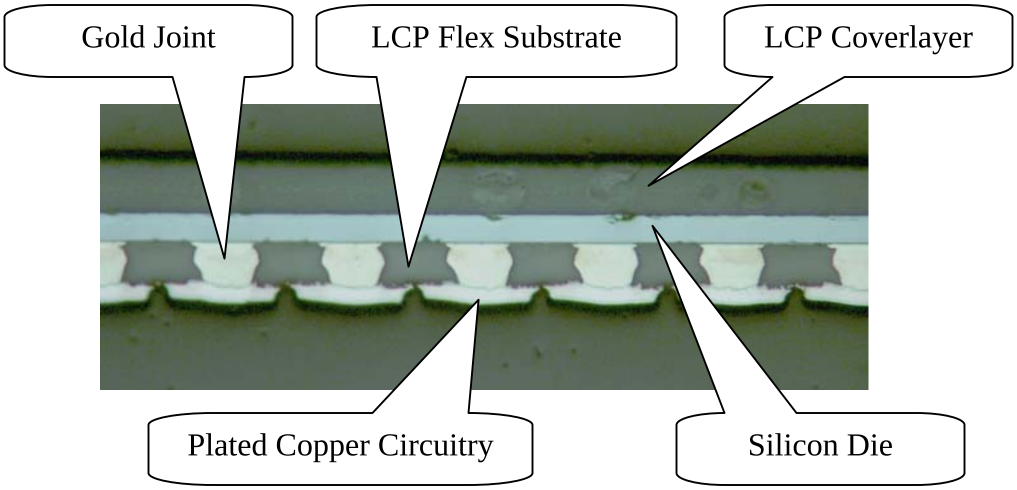


Figure 1.4 Cross-Section of the 50µm Thick PB8 Flip Chip in LCP Flex

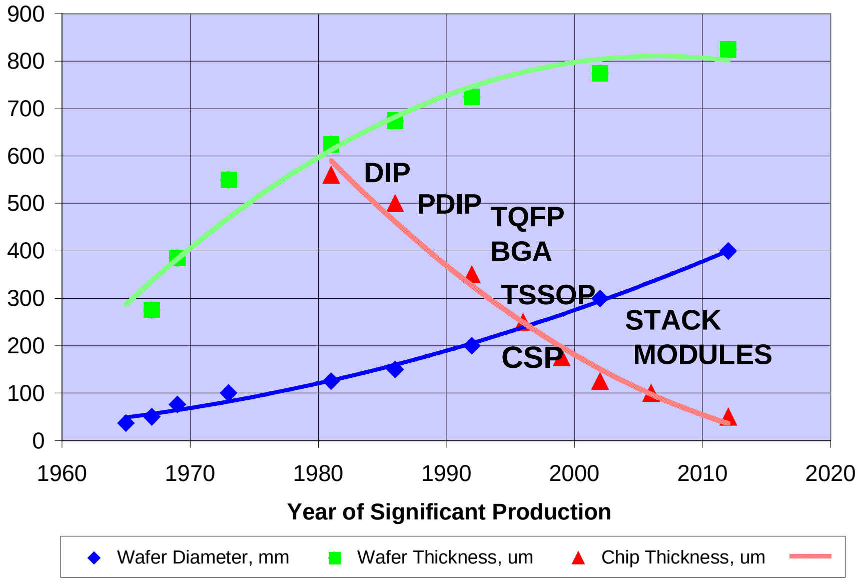
This dissertation is divided into literature review, thin die preparation, substrate fabrication, assembly and electrical performance testing. Chapter 2 briefly introduces the attributes and development trends of thin electronic assemblies. Four silicon thinning approaches are described with their procedures and advantages. Three polymeric materials suitable for flexible substrate are presented with their chemical compositions, structure and properties. Liquid crystal polymer was selected because of its low coefficient of thermal expansion, low moisture absorption and high melting temperature. Existing integration techniques for thin electronic assemblies are also examined. Chapter 3 presents the preparation of thin dies for this research work. Thin die transfer is employed for easing die handling and maintaining thin dies flat. Chapter 4 describes the fabrication process for the LCP substrate, including bottom circuitry formation, via formation and copper surface finishing. Chapter 5 discusses the integration process of thin flip chip in LCP flex with thermal compression bonding. The issues of bonding temperatures for development of the thermal compression bonding profile are described. In Chapter 6, a thin operational amplifier IC embedded in LCP is described. Its electrical properties were examined as a function of bending radius. Conclusions and recommendations for further work are made in Chapters 7 and 8, respectively.

CHAPTER 2 LITERATURE REVIEW

Electronic packaging is the housing that protects integrated circuit (IC) chips and components from external harsh environments. At the same time, it provides the mechanical interface necessary for testing and electrical connections to the next level of packaging [1]. Development of low profile electronic packages is being motivated by the ongoing miniaturization of electronic products. This is because the application of smaller feature size packages and components provide many benefits, such as smaller space requirements, lighter weight, and higher functionality (per area or per volume) [2]. The use of smaller components enables products to be slimmer in appearance, enhancing their portability. This is particularly significant for handheld products such as memory modules, smart cards, RFID tags, cell phones, digital cameras and camcorders, game boxes, medical devices, PDAs and laptop notebooks.

Package height is one of the most significant indexes, particularly for thin flexible assemblies, and it is driving a need for downscaling all construction elements, such as ICs and components, interconnections and substrates. Interconnections are continuously being downsized, from wire bonds, to solder joints, and then to anisotropic conductive adhesives. Thin substrate materials such as polyesters and polyimides have already been widely used to fabricate thin flexible substrates for flexible and semi-rigid assemblies. The thinned ICs being used in the electronics packaging industry are very thin silicon is attractive for developing thin IC assemblies. Figure 2.1 illustrates the trend of decreased die thickness in electronic packages [2].

In this chapter, die thinning, flexible substrate materials and assembly processes are reviewed. These are the critical elements for the development of thin, flexible assemblies.



BGA	Ball Grid Array
CSP	Chip Scale Package
DIP	Dual Inline Package
PDIP	Plastic Dual Inline Package
TQFP	Thin Quad Flat Pack
TSSOP	Thin Shrink Small Outline Plastic Package

Figure 2.1 Trends for Wafer Thickness, Wafer Diameter and Die Thickness [2]

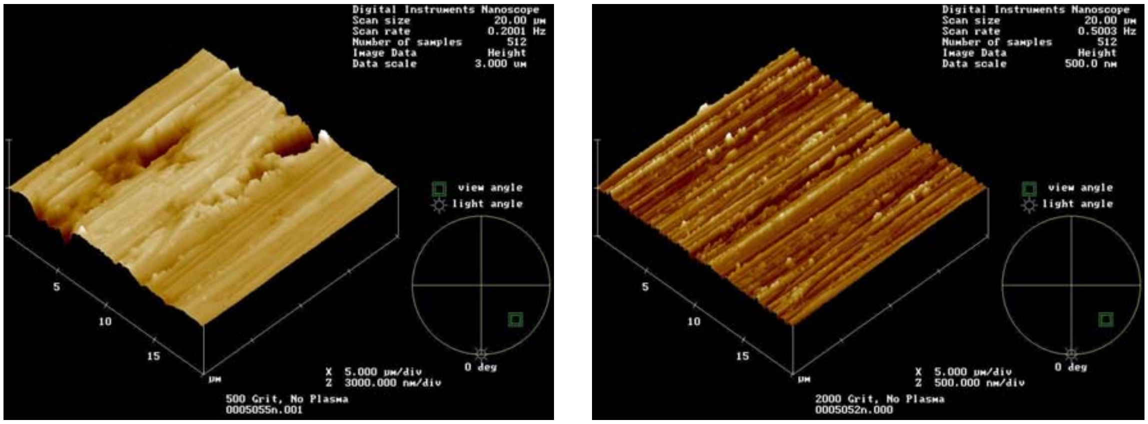
2.1 SILICON THINNING

For most ICs, the thickness of the active layer ranges from 3 to 10µm [3], a small fraction of the thickness of the silicon chip, which is usually 500-700µm thick. Four different methods are available for thinning chips or wafers: mechanical surface grinding, chemical mechanical polishing (CMP), wet etching, and plasma etching.

2.1.1 Mechanical Surface Grinding

Mechanical surface grinding [2,4,5] is carried out using diamond abrasive grinding wheels on rotary grinders. The grinding process consists of two phases: a coarse abrasive wheel grind and fine abrasive wheel grind. The coarse abrasive wheel grind (typically ~350-500 grit diamond abrasive) removes material rapidly, but damages the surface by gouging the silicon away. This is followed by a fine abrasive wheel grind which removes most of the grinding damage using a more gentle grinding with fine abrasive (2000-3000 grit). Mechanical grinding is the most commonly used process for thinning chips and wafers, although it does induce significant stress and damage into the silicon. Some of the coarse grinding damage remains even after fine grinding, and this damage is often driven into the silicon surface after the fine grinding process. Figure 2.2 shows ground surface profiles scanned by Atomic Force Microscopy (AFM) [4]. X-ray topography indicates that most of the damage is located within a region about 20µm deep. Figure 2.3 shows a transmission electron microscopy (TEM) scan that reveals defects within the region near the surface of the finely ground wafer [5]. These residual defects may lead to additional bowing and damaged chips and wafers often break during handling or further processing.

Mechanical grinding has a major advantage in that it can reduce bulk wafer thickness at a significant rate (5µm/sec for coarse grinding and 1µm/sec for fine grinding), thereby making it a very affordable process [5]. Consequently, backside grinders are generally utilized for both wafer fabrication and in some assembly areas.


Digital Instruments Nanoscope
Scan size 20.00 µm
Scan rate 0.2001 Hz
Number of samples 512
Image Data Height
Data scale 3.000 um
view angle
light angle
5
10
15
µm
X 5.000 µm/div
Z 3000.000 nm/div
0 deg
500 Grit, No Plasma
0005055n.001
Digital Instruments Nanoscope
Scan size 20.00 µm
Scan rate 0.5003 Hz
Number of samples 512
Image Data Height
Data scale 500.0 nm
view angle
light angle
5
10
15
µm
X 5.000 µm/div
Z 500.000 nm/div
0 deg
2000 Grit, No Plasma
0005052n.000

(a) After 500-grit grinding (b) After 2000-grit grinding

Figure 2.2 Atomic Force Micrographs (ATM) of the Surface of Silicon Wafers Subjected to 500-Grit and 2000-Grit Grindings, Respectively [4]

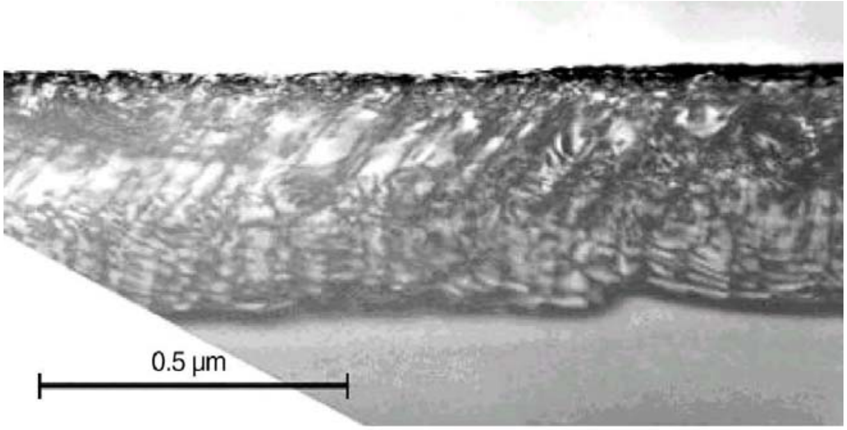


Figure 2.3 Cross-Section TEM Picture Showing Structural Defects Near the Wafer Surface after Fine Grinding [5]

2.1.2 Chemical and Mechanical Polishing

Chemical and mechanical polishing (CMP) [5] is used primarily in wafer manufacturing and device fabrication. The CMP process is usually carried out on mechanical grinders using buffered silica slurries. After CMP, a flat wafer surface is achieved with lower total thickness variation (TTV) values than mechanical grinding. Fine polishing can reduce the stresses that build up during the previous thinning stages, removing most of the damage while the stress is released. However, the thinning rate is only a few microns per minute. Obviously, this process is therefore more suitable for laboratory use. Figure 2.4 shows a typical CMP process [6].

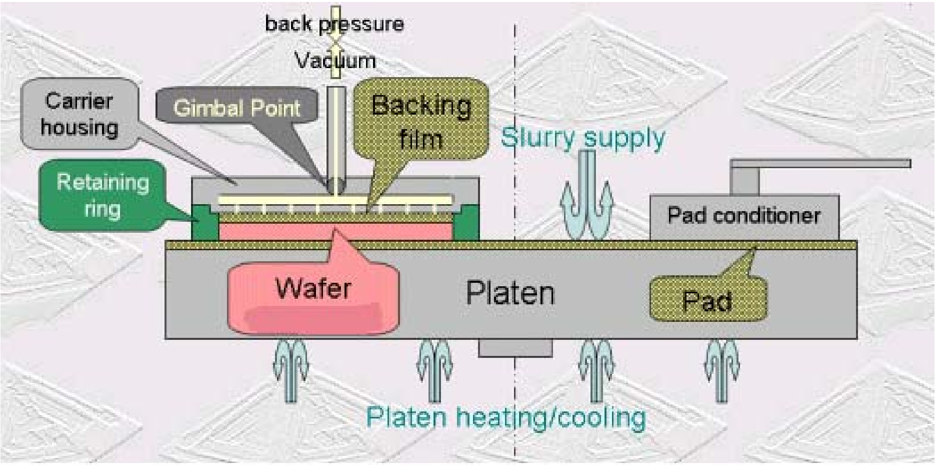

back pressure
Vacuum
Carrier housing
Gimbal Point
Backing film
Slurry supply
Retaining ring
Pad conditioner
Wafer
Platen
Pad
Platen heating/cooling

Figure 2.4 The Chemical and Mechanical Polishing (CMP) Process [6]

2.1.3 Wet Chemical Etching

Wet chemical etching [5] is another common thinning technique used in wafer manufacturing and device fabrication. One common approach is spin etching, in which a thin stream of an etchant is applied periodically over the surface of a rotating wafer, as shown in Figure 2.5 [5]. The etchant is a mixture of hydrofluoric acid (HF) and nitric acid (HNO_3). The etching rate is controlled by adjusting the mixing ratio. A common etching rate is about 10µm per minute. The surface flatness is dependant on the etching time and the flow of etchant across the wafer surface. The TTV value is comparable to that of the CMP process. This technique is preferred for its ability to reduce stress in wafers and planarize the device surface, rather than its ability to thin wafers.

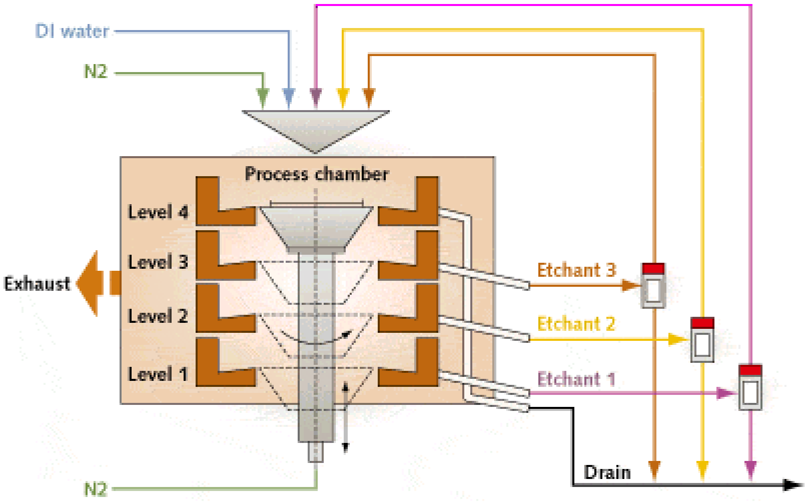


Figure 2.5 The Wet Spin Etching Process [5]

2.1.4 Plasma Etching

Plasma etching of silicon [2,7] is widely used in electronic device microfabrication, especially in microelectromechanical systems (MEMS). The plasma is generated by ionizing gaseous etchants within an electrical field into electrons, radicals and neutral particles. The three sequence steps of adsorption, reaction and desorption lead to etching. The reactive radicals bombard the exposed silicon guided by an electrical field or flow. The bombarded silicon atoms combine with reactive radicals to form a volatile substance, escaping from the bulk silicon with the assistance of heat or lower pressure. Figure 2.6 illustrates the three main steps of the surface chemistry in a plasma etching process.

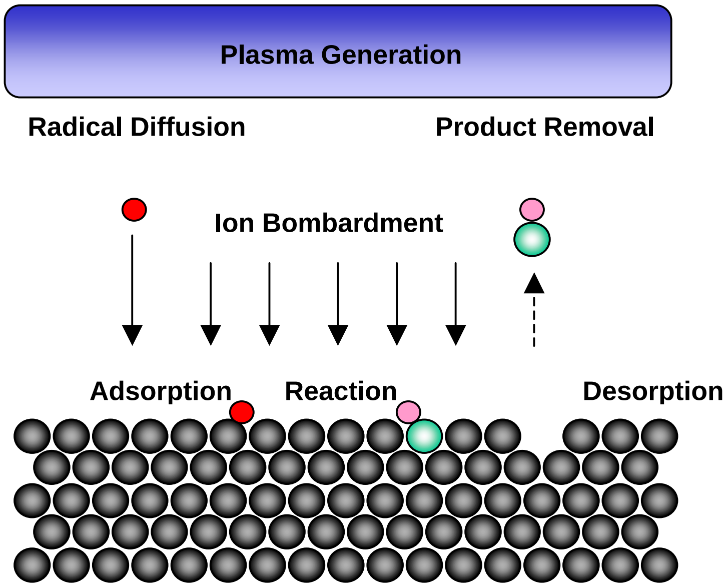
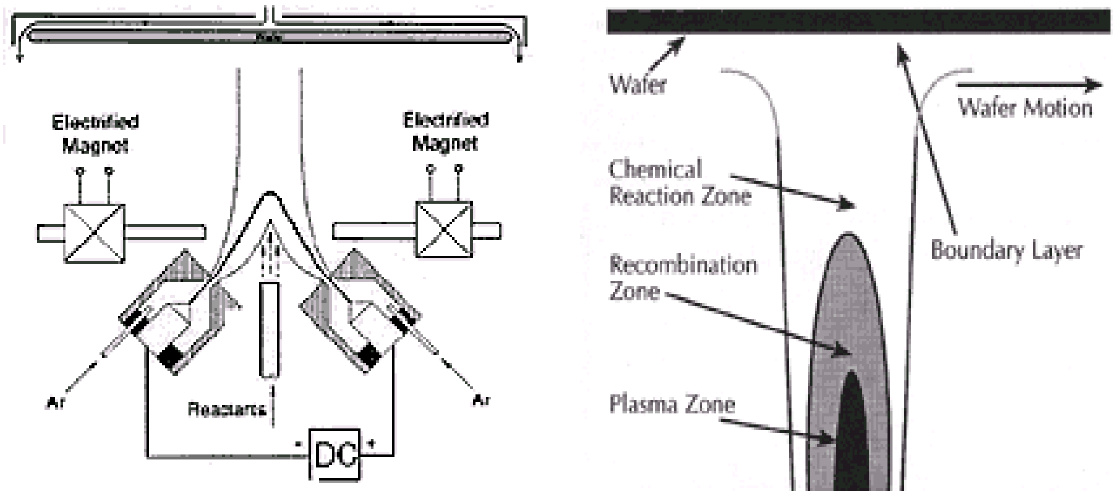

Plasma Generation
Radical Diffusion
Product Removal
Ion Bombardment
Adsorption
Reaction
Desorption

Figure 2.6 The Plasma Etching of Silicon

The most successful wafer plasma thinning process is the Atmospheric Downstream Plasma (ADP) process, developed by Tru Si Technologies, a Silicon Valley based company [2,7]. This technology combines the fast thinning capabilities of grinding with the stress removal capabilities of CMP and wet etching.

ADP isotropically etches uniform layers of silicon from the wafer surface. The ADP source incorporates two electrode units that are directed upwards at an angle of 90° to each other, as shown in Figure 2.7(a) [8]. The mainstream plasma gas (argon) is injected into the chamber and exits through the water-cooled orifice to create an accurately controlled atmospheric pressure plasma of high-energy activated species with a temperature of 10,000K and a velocity of about 10m/s.

Figure 2.7(b) shows a close-up of the plasma generation and reaction [8]. Once the plasma is generated, reactant gas (CF_4) is injected into this plasma where it is chemically decomposed into charged species and neutral particles in the plasma generation zone. The plasma flows through the orifice towards the wafer surface. Both physical interactions and chemical reactions occur on the surface of the wafer in the reaction zone. As the plasma flow reaches the wafer surface, its temperature is reduced to 500K. Because of the high pressure, there is a high species flux reaching the wafer surface. ADP etch rates are at least two orders of magnitude greater than conventional vacuum plasma etching systems. Figure 2.8 displays the surface topology of etched silicon, on which various size craters remain after plasma bombardment [8].


Electrified Magnet
Electrified Magnet
Ar
Reactants
Ar
DC
Wafer
Wafer Motion
Chemical Reaction Zone
Boundary Layer
Recombination Zone
Plasma Zone

(a) (b)

Figure 2.7 The Atmospheric Downstream Plasma Etching Process [8]

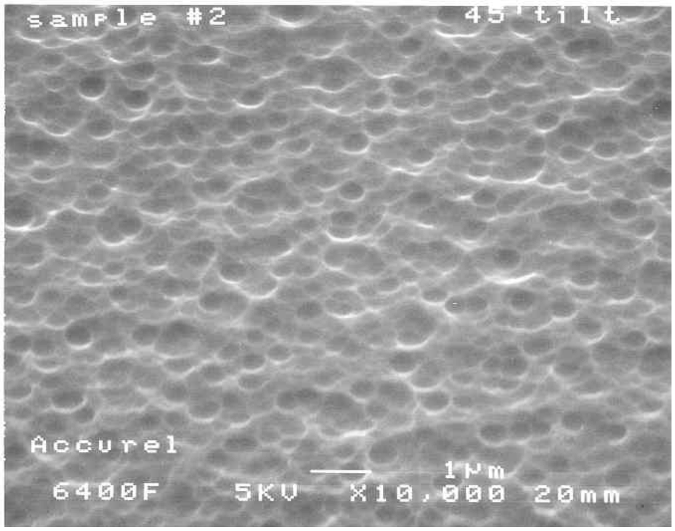


Figure 2.8 The SEM Picture of the Surface of A Dry-Etched Silicon Wafer [8]

2.2 FLEXIBLE SUBSTRATE MATERIALS

Substrates connect the ICs and components together or provide for the integration with external circuit elements [8]. Materials to be used as substrates must have a number of properties [9]:

- Good insulating characteristics, to ensure electrical isolation of the circuit lines and components;
- Low dielectric constants, to produce low capacitive loading of circuit lines and low capacitive coupling;
- High strength and toughness, for ruggedness and processibility;
- High dimensional stability;
- Coefficients of thermal expansion that are near those of the materials to be attached to them.

Besides these common requirements, thin assemblies also demand thinner substrates, as clearly a thinner substrate decreases the total assembly height. However, as the substrate thickness continuously decreases to very low values (less than 100µm), conventional substrate materials, such as ceramics and epoxy-based fiber reinforced laminates, no longer provide sufficient mechanical support for the ICs and components that are mounted on them. This is because their strength and impact resistance degrade dramatically along with their decreasing thickness [10]. Compared with conventional substrate materials, polyesters, polyimides and thermotropic liquid crystal copolyesters (LCP) demonstrate both a high modulus and a high strength, along with a great degree of flexibility. These material properties are listed in Table 2-1 [11], showing that these materials are attractive for use in fabricating flexible substrates for thin assemblies.

Table 2-1 Specification of Base Films for Flexible Substrates [11]

	Polyester	Polyimide	LCP
Melting point (°C)	243-260	-	277-254
Density (g/cm^3)	1.35-1.40	1.32-1.71	1.49-1.79
Tensile strength, yield (MPa)	$0.38\text{-}0.89\times10^2$	$0.32\text{-}0.87\times10^2$	$1.48\text{-}2.07\times10^2$
Tensile strength, break (MPa)	$0.48\text{-}0.73\times10^2$	$0.20\text{-}1.10\times10^2$	$0.62\text{-}2.07\times10^2$
Elongation, break	85.0-160.0%	0.5-10.0%	1.0-3.0%
Tensile modulus (GPa)	2.75-3.82	1.08-2.55	1.01-2.21
Flexural modulus (GPa)	0.88-1.76	0.59-1.93	0.94-1.60
Compression strength (MPa)	$0.96\text{-}1.26\times10^2$	$0.14\text{-}2.42\times10^2$	$0.45\text{-}0.80\times10^2$
Izod notched, R.T. (kg cm/cm)	1.6-22.7	1.4-19.7	3.8-16.7
Thermal conductivity (W/m-°K)	0.067-0.121	0.22-0.63	0.13-0.45
Linear thermal expansion (cm/cm-°C)	$14\text{-}90\times10^{-6}$	$13\text{-}52\times10^{-6}$	$2.0\text{-}27\times10^{-6}$
Deflection Temp. @ 264 psi (°C)	177-232	238-349	170-349
Continuous service temp. (°C)	166-193	249-288	-
Dielectric strength (V/mm)	$1.5\text{-}2.7\times10^4$	$0.8\text{-}2.7\times10^4$	$2.2\text{-}3.5\times10^4$
Dielectric constant @ 1MHz	2.9-3.2	3.0-5.2	3.1-4.3
Dissipation factor @ 1MHz	0.010-0.020	0.001-0.010	0.020-0.030
Water absorption, 24 hr	0.08-0.15%	0.27-0.97%	0.01-0.10%

2.2.1 Polyester

High modulus, high strength polyester films, such as Mylar, are thermoplastics made primarily from high-molecular-weight polyethylene terephthalate (PET) [12]. The synthetic reaction and biaxially oriented film-forming process are shown in Figure 2.9

and Figure 2.10 [12], respectively. PET resin is melted and immediately extruded onto a chilled roll drum to form a film. This as-extruded film is then biaxially oriented by stretching, first in the machine direction (MD) and then in the transverse direction (TD). The orientation is accomplished by passing the film over rollers that run at increasingly faster speed (MD orientation), then fed into a tenter frame, where it is pulled at right angles (TD orientation). This stretching rearranges the PET molecules into an orderly structure, substantially improving the material’s mechanical properties. Polyester films are colorless and highly transparent and their low cost is advantageous for many applications. However, polyester films have a relatively low service temperature (166-193°C), which may pose a problem in soldering applications [11]. Polyesters are also vulnerable to hydrolysis.

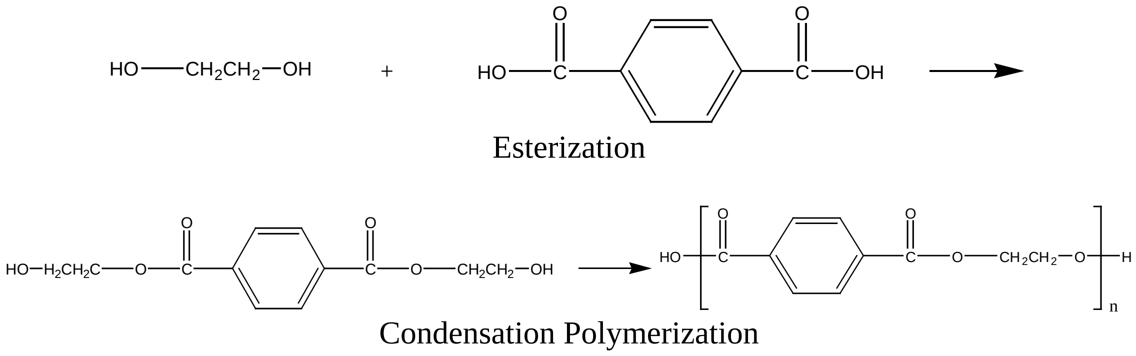

HO—CH2CH2—OH
+
HO—C(=O)—C6H4—C(=O)—OH
Esterization
HO—H2CH2C—O—C(=O)—C6H4—C(=O)—O—CH2CH2—OH
HO—[C(=O)—C6H4—C(=O)—O—CH2CH2—O]n—H
n
Condensation Polymerization

Figure 2.9 The Synthesis of Polyester

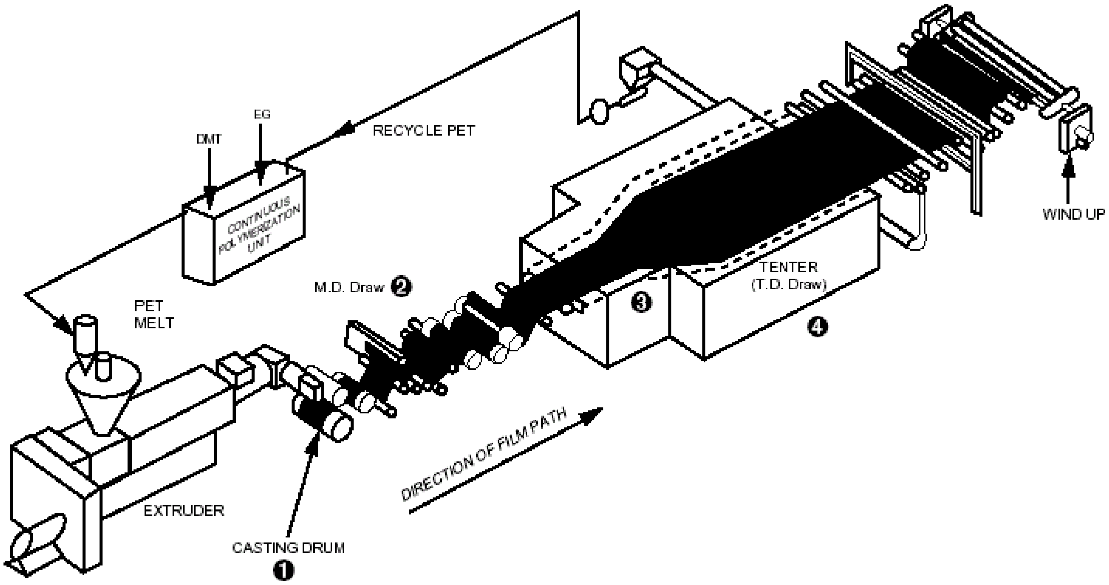

EG
DMT
RECYCLE PET
CONTINUOUS POLYMERIZATION UNIT
PET MELT
M.D. Draw ❷
TENTER (T.D. Draw)
❸
❹
WIND UP
DIRECTION OF FILM PATH
EXTRUDER
CASTING DRUM
❶

Figure 2.10 A Typical Manufacturing Process for Oriented Polyester Film [12]

2.2.2 Polyimides

Polyesters were one of the first materials used as flexible substrates, but they were rapidly replaced by polyimides. Polyimide films have excellent thermal stability, high mechanical strength and flexibility, matching the demand for building thin flexible substrates [13]. Today, polyimide films are the predominant material used in flexible substrates.

Polyimide films are amber in color and highly transparent, formed by the condensation reactions of aromatic dianhydrides with aliphatic or aromatic diamines (Figure 2.11) [14]. The synthesis includes two steps: the synthesis of polyamic acid, followed by thermal imidization. A tetracarboxylic acid dianhydride is mixed with a solution of diamine, generating an intermediate, polyamic acid. The intermediate is heated for cyclodehydration in the imidization stage, thus forming the corresponding polyimide [13].

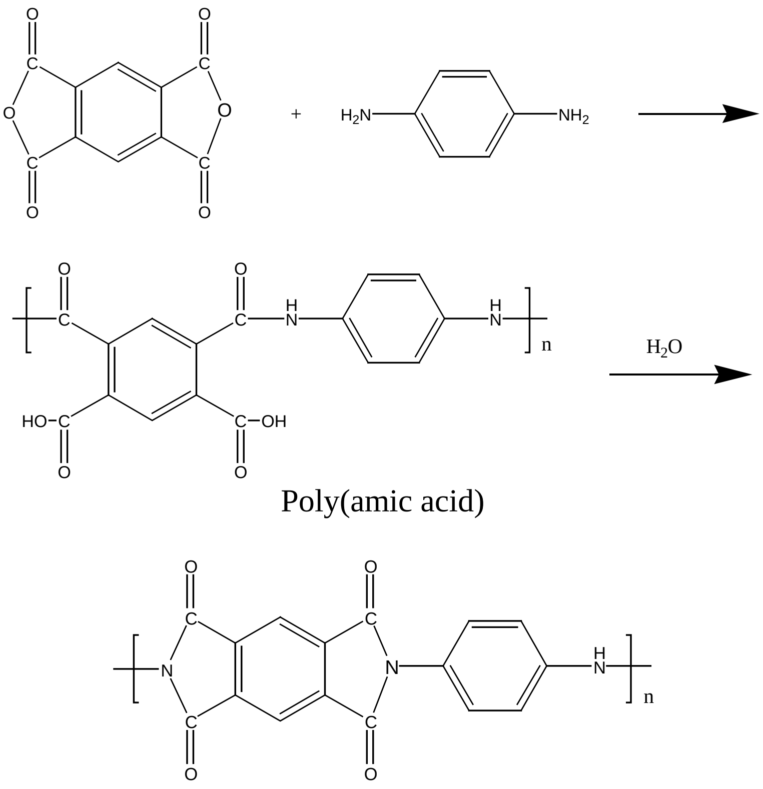


Figure 2.11 Synthesis of Polyimide [14]

Since polyimides are often insoluble and infusible, the polymer is usually processed in the form of the polyamic acid, which is thermally imidized in place. Polyimide films are manufactured by adding conversion chemicals (e.g. acetic anhydride) into the chilled polyamic acid solution, and then casting it on to a heated drum to produce a gelled film. In order to improve the tensile strength and modulus of the final polyimide film, the chemically converted gel film is stretched at 300°C [15].

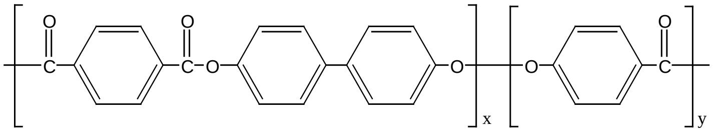
Polyimides have a ladder-type molecular structure with a backbone composed of rigid cyclic elements [16]. This stiff structure is beneficial for high strength/modulus applications. Polyimides also exhibit excellent thermal stability. DuPont reports that polyimides do not melt or burn, giving them the highest UL-94 flammability rating of V-0, and their outstanding properties allow them to be used at both high (400°C) and low (-269°C) temperature extremes [17].

2.2.3 Liquid Crystal Polymers

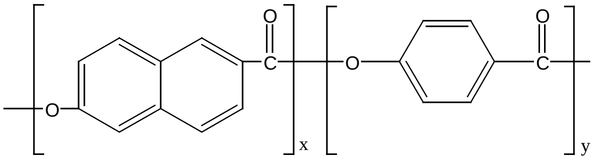
Recently, liquid crystal type polymers have been receiving a great deal of attention due to their good mechanical properties, lower thermal expansion and excellent dielectric characteristics. Currently, liquid crystal polymers (LCP) used as flexible substrates are referred to as thermotropic liquid crystalline aromatic copolyesters. They have sufficiently high concentrations of suitable aromatic units in the polymer backbone to permit the formation of a liquid crystalline phase [18].

Generally speaking, liquid crystal polymers can form a specific phase (mesophase) that falls between the crystalline state (solid) and the isotropic state (liquid). Within this mesophase, the polymers demonstrate mobility (like a liquid) and anisotropicity (like a crystal). There are two types of thermotropic liquid crystal copolyesters that are often used in flexible circuits and their molecular structures are shown in Figure 2.12 [19].

Due to the inclusion of aromatic groups in the backbone, the molecular chain demonstrates a rigid-rod structure. This stiff structure has excellent heat resistance. The type 1 copolyester has a melting point ranging from 300-350°C, while the type 2 has a melting point ranging from 200-250°C [19].



Type 1: Copolymer of terephthalic acid, 4,4’-dihydroxybiphenol and 4-hydroxybenzoic acid (TA-BP/HBA)



Type 2: Copolymer of 2-hydroxy-6-naphtholic acid and 4-hydroxybenzoic acid (HNA/HBA)

Figure 2.12 Thermotropic Liquid Crystalline Aromatic Polyesters [19]

These two types of LCPs are thermotropic liquid crystal polymers that possess a mesophase in the melt. Their liquid crystal mesophases are nematic [20]. In nematic mesophases there is only one orientational order, where the polymer chains lay parallel to one another along the same axis, as shown in Figure 2.13 [21]. Nematic liquid crystal polymers have a one-dimensional order structure and exhibit anisotropy in a preferred direction.

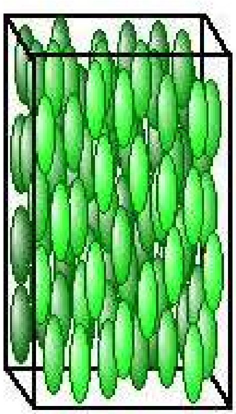


Figure 2.13 Schematic of Nematic Mesophase [21]

When LCP flows or is subjected to external electrical and magnetic fields in the liquid crystal state, the rigid molecules align with each other in the flow direction or along the field directions. The rigid nature of the molecules results in an extended chain structure, which is beneficial for generating a higher strength and modulus in the oriented direction. In Jackson and Kuhfuss' study, their samples exhibited tensile strengths of 107MPa along the flow direction and 29MPa across the flow direction [22].

The presence of an oriented structure also creates anisotropy. Early LCP film products exhibited significant differences in plane. For example, the coefficient of thermal expansion could be as low as 5 ppm/°C in the flow direction but 40 ppm/°C in the transverse direction [23]. The drawbacks of anisotropic film are curling, brittleness in the transverse direction, surface roughness, embedded particles, and discoloration [19]. These problems affect the roll-to-roll circuit process and generally result in poor circuit performance and reliability.

Foster-Miller Corporation invented a counter-rotating die technique to allow control of the fibrillar LCP orientation to any desired value. By utilizing a novel annular die, both sheets and films of the material can be produced with controlled directions of orientation. A combination of rotational shear and elongational flow during the extrusion process orients the LCP molecules. This controlled biaxial orientation balances the alignment in plane, while the shears in the two directions preserve the extended chain structure (for high strength and modulus). A schematic of the counter-rotating die is shown in Figure 2.14 [24].

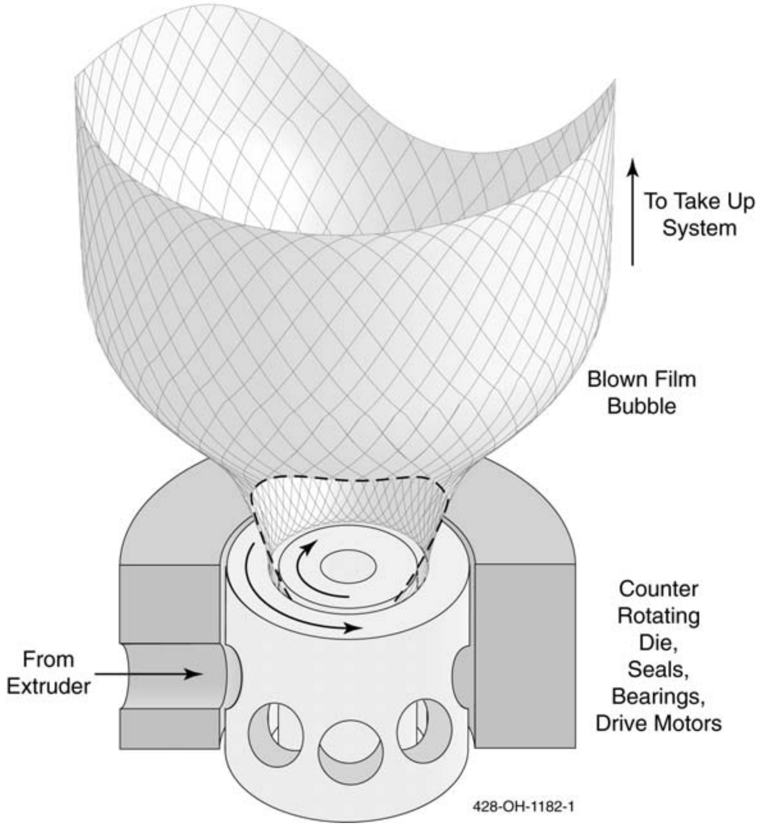

To Take Up System
Blown Film Bubble
Counter Rotating Die, Seals, Bearings, Drive Motors
From Extruder
428-OH-1182-1

Figure 2.14 Schematic of Counter-Rotating Die and Extrusion [24]

Compared with polyimide films, LCP films have very low moisture absorption (<0.1%) and low permeability to most common gases [25]. Their low coefficient of thermal expansion (CTE) in plane (about 8-17 ppm/°C) is comparable to that of ceramics

(6-8 ppm/°C), which can significantly reduce the in-plane stress associated with CTE mismatches. Although LCPs are thermoplastic, their melting points are quite high and thus suitable for high temperature applications. Another notable property is their low dielectric constants and dissipation factors (Figure 2.15 and Figure 2.16) [26], making them suitable for microwave applications. Figure 2.15 and Figure 2.16 also show the dielectric stability of LCP compared to polyimide and standard FR-4 epoxy-glass materials when exposed to moisture.

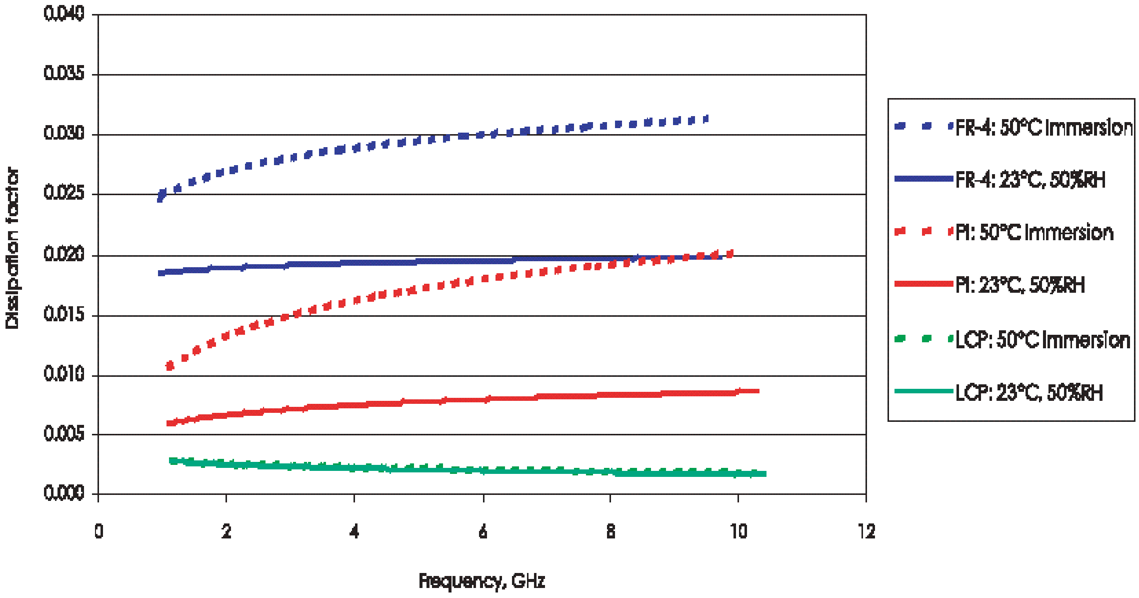


Figure 2.15 Dielectric Constant Variation: LCP, Polyimide and FR-4 [26]

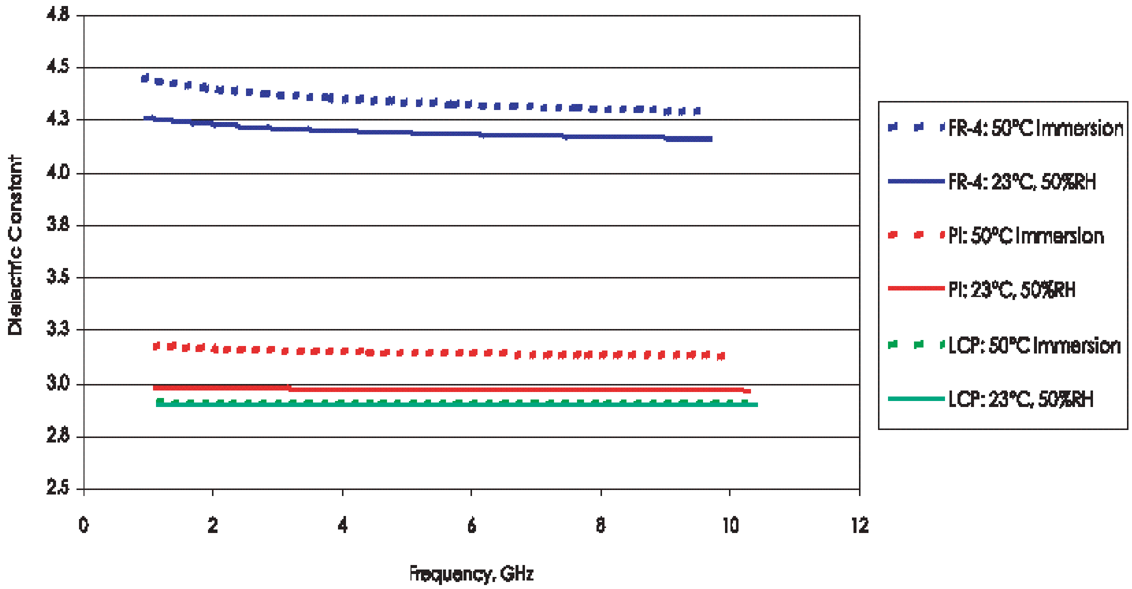


Figure 2.16 Dissipation Factor Variation: LCP, Polyimide and FR-4 [26]

2.3 INTEGRATION OF FLEXIBLE ASSEMBLIES

Establishing interconnects between the thin silicon chip and the flexible substrate is a vital part of the process for building thin flexible assemblies. Thinned silicon dies tend to warp due to their asymmetrical structure (see Figure 2.17) [27]. Thinned silicon is also very vulnerable compared with conventional thickness dies. Handling of the thin silicon dies is thus a major challenge for the assembly process, and thick flat handles are sometimes employed to support the thin dies [28, 29, 30]. After assembly, removal of the handling die is necessary, leaving the thinned die in place on the flexible substrate.

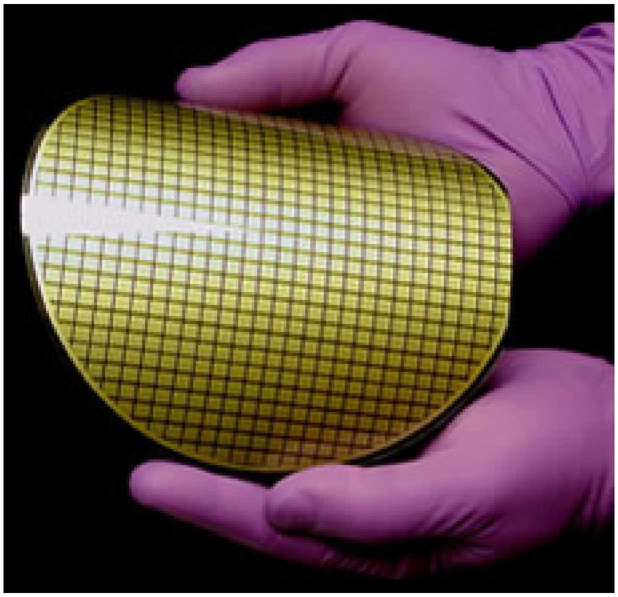


Figure 2.17 Warping of Thinned Wafer [27]

Compared with thinned silicon, flexible substrates conform more closely to the support surface. Asymmetrical constructions of flexible substrates tend to deform when exposed to hot environments, especially temperatures that are higher than the substrate material's glass transition temperature (T_g). The asymmetric construction results from the patterning of copper interconnect traces on one or both surfaces of the substrate. This may be an issue because a warped substrate will affect the formation of solder joints during reflow soldering. Figure 2.18 shows a normal thickness area array flip chip on a polyimide flex substrate assembled in this laboratory [28,29]. In the cross-sectional view, the pulled solder joints exhibit a hyperboloid contour; meanwhile, varying sizes of joints can be observed in the top view. This was due to warpage of the polyimide substrate during the reflow cycle.

Using a fixture, the flexible substrate was secured on a flat surface with a vacuum during the assembly process [29,30,31], resulting in uniform interconnections (Figure

2.19) [28,29]. The left side of the figure shows uniform drum-shape solder joints of a 50µm-thickness area array flip chip on polyimide flex; the right side of the figure shows a quasi-3D x-ray image that exhibits uniform joints in the top view.

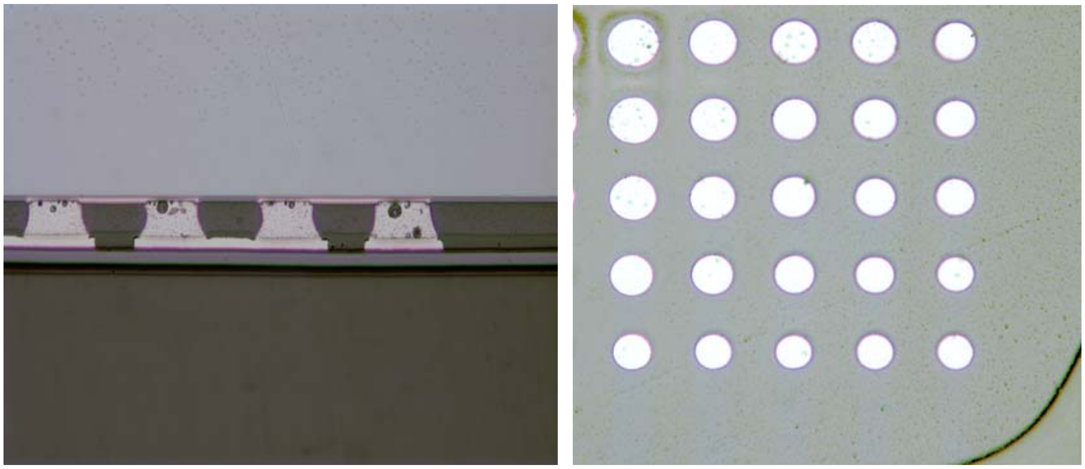


Figure 2.18 Elongated and Uneven Solder Joints

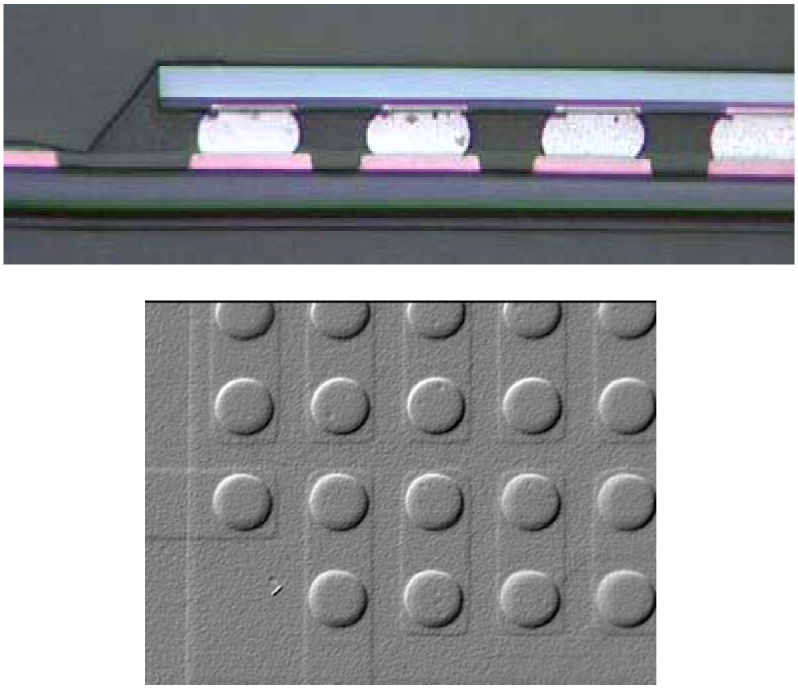


Figure 2.19 Uniform Solder Joints in 50µm Die on Polyimide

The interconnection strategies used with chips mounted on substrates are predominantly die attachment with wire bonding and flip chip interconnections on high-density I/O substrates. Wire bonding is the most common interconnection process, providing electrical connections between the silicon chip and the pads on the substrate using very fine bonding wires. In order to protect the wires and circuits from mechanical damage and the environment, the wire bonded die is generally encapsulated. Epoxy molding compound is transfer molded over the die and wire bonds. The construction of a wire bonded package is shown in Figure 2.20.

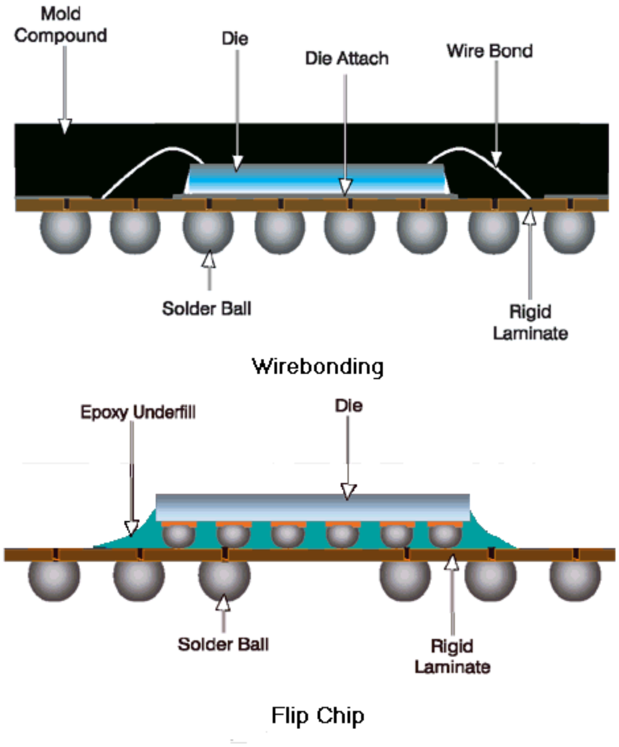

Mold Compound
Die
Die Attach
Wire Bond
Solder Ball
Rigid Laminate
Wirebonding
Epoxy Underfill
Die
Solder Ball
Rigid Laminate
Flip Chip

Figure 2.20 Schematics of Wirebonding and Flip Chip Packages

Flip chip is another popular interconnection technology, where the active side of the IC chip is attached upside down to the substrate and interconnections are established to provide electrical connectivity and mechanical support [32]. This approach provides light weight, minimal height, small footprint, and more I/Os compared with wire bonding. Of particular interest, flip chip solutions are ideal for many applications that require a low profile. Several thin flip chip integration methods are reviewed below.

2.3.1 Reflow Soldering

This approach is based on the Controlled Collapse Chip Connection (C4) technology that is now widely used in mass flip chip assemblies. However, conventional C4 technology must be modified for assemblies involving thinned dies on flexible substrates. Zhang and coworkers [30] employed a pick and place machine to directly place 100μm dies with peripheral solder bumps onto polyimide flex substrates. The polyimide substrates were secured on a rigid FR-4 board during the process. The assemblies on polyimide substrates with no solder mask had a 100% yield, but those with solder mask defined polyimide substrates had only a 60% yield.

In our laboratory [28], thin flip chips on polyimide flex substrates were assembled using conventional flip chip equipment by using thin dies on handles. The thicknesses of the thinned dies were 25, 50, 75, 150, and 250 μm. The thinned dies were mounted on flat handling dies with an adhesive prior to assembly. The flex substrates were held on a vacuum fixture which had been machined with a porous sintered block of stainless steel. After completing the reflow soldering stage, the handling dies were removed by immersing the parts in acetone to dissolve the adhesive. Figure 2.21 shows a flexible assembly of a 50μm area array flip chip on a polyimide substrate, demonstrating how flexible they are [28].

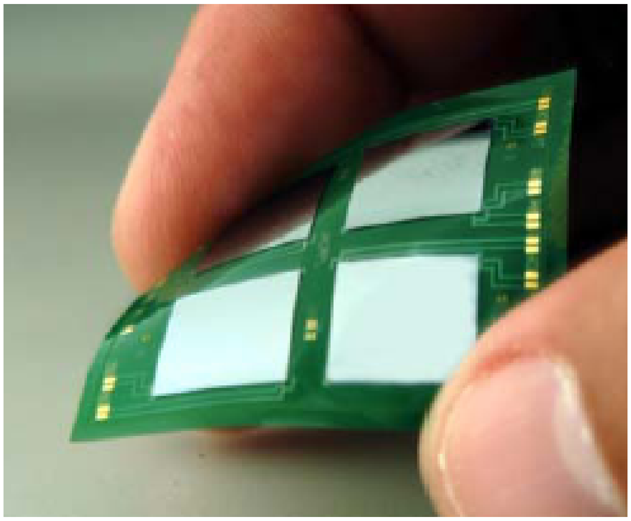


Figure 2.21 50μm-Thickness Flip Chips on Polyimide Substrate [28]

2.3.2 Thermode Bonding

Fraunhofer IZM invented a new thermode bonding approach with which to assemble its small solder bump die, mounted on a handling die, onto a flex substrate [33]. Here, the small solder bumps were deposited by immersion soldering. No-flow underfilling technology was employed, enabling the underfill material to be stencil printed on the bump side of the die. The coated dies were placed face down, accurately aligned with the matching sites on the substrate. The bonding nozzle incorporated pulsed heat thermodes that provided pulsed heat at very high heating rates to the die/underfill/substrate. The bonding temperature was significantly higher than the melting point of the solder, but was maintained for only a short time. During this short time, the solder bumps melted to form the joints between the die pads and substrate pads. At the same time, the curing of the underfill was initiated, thus firmly attaching the chip onto the substrate. The thermode bonding process is shown in Figure 2.22 [34]. Figure

2.23 shows a cross-sectional view of a 40µm pitch AuSn thermode bonded assembly produced using this method [34].

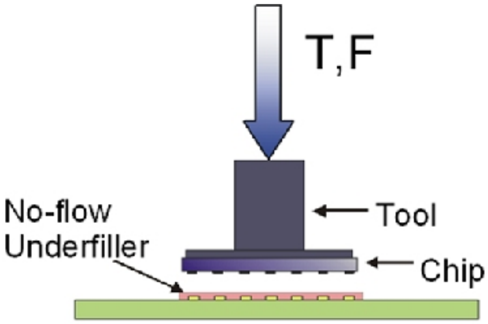


Figure 2.22 Principle of Thermode Bonding Process [34]

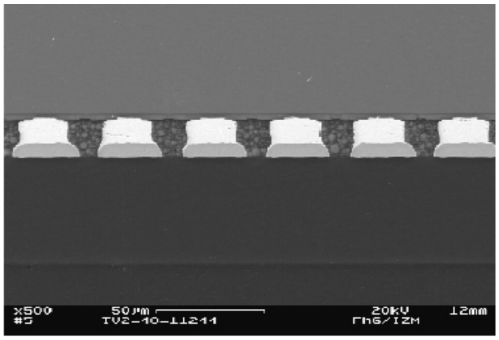


Figure 2.23 Cross Section of 40µm Pitch AuSn Thermode Bonded Assembly [34]

2.3.3 Adhesive Bonding

Adhesive bonding uses anisotropic conductive adhesive (ACA) to bond the die and substrate together under heat and pressure. ACA is a polymeric material filled with a low concentration of large conductive particles that is designed to conduct electricity in the Z direction, but not the X or Y directions [35]. ACA film is pre-attached onto the flexible substrate under low temperature and low pressure. The thinned die can then be placed onto the bond site. Bonding pressure allows the die pad and corresponding substrate pad to trap conductive filler particles between them. At the same time, heat is supplied to cure the adhesive, bonding the die and the substrate together. Figure 2.24 shows a trapped ACA particle between a transponder IC bump and an antenna pad [34].

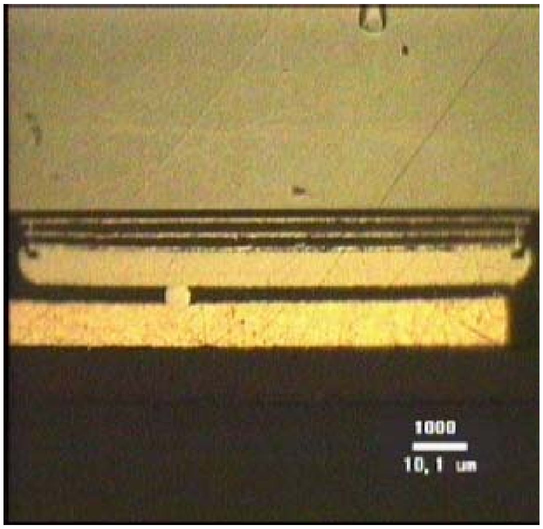
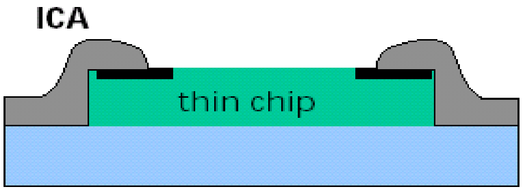


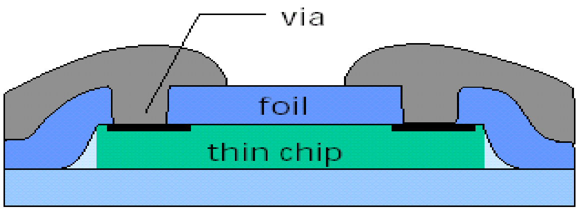
Figure 2.24 ACA Particle Trapped between Transponder IC Bump and Antenna Pad [34]

2.3.4 Isoplanar Interconnection

The isoplanar interconnection technique is a face up assembly that includes two major separate processes: the die is first attached onto the flexible substrate with adhesive, followed by the formation of the electrical connections [36]. A bonding adhesive is deposited on the flexible substrate by dispensing, printing or stamping. The IC die, which has been mounted on a handling die, is placed face up and attached onto the bond site on the substrate. Heat is then applied to cure the adhesive, bonding the die to the substrate, after which the handling die carrier is released, leaving the thinned die on the substrate. After completing the die attachment, a silver-filled polymer, which acts as a conductive adhesive, is dispensed or printed to establish an interconnection between the die pads and substrate pads. This approach is low cost, but restricted to low count I/Os on a relatively large pitch. Figure 2.25 displays two different isoplanar interconnection assemblies [37].



(a) Isoplanar Contact with Conductive Polymer Paste



(b) Isoplanar Contacts through Laminated Foil

Figure 2.25 Isoplanar Connections [37]

2.4 SUMMARY

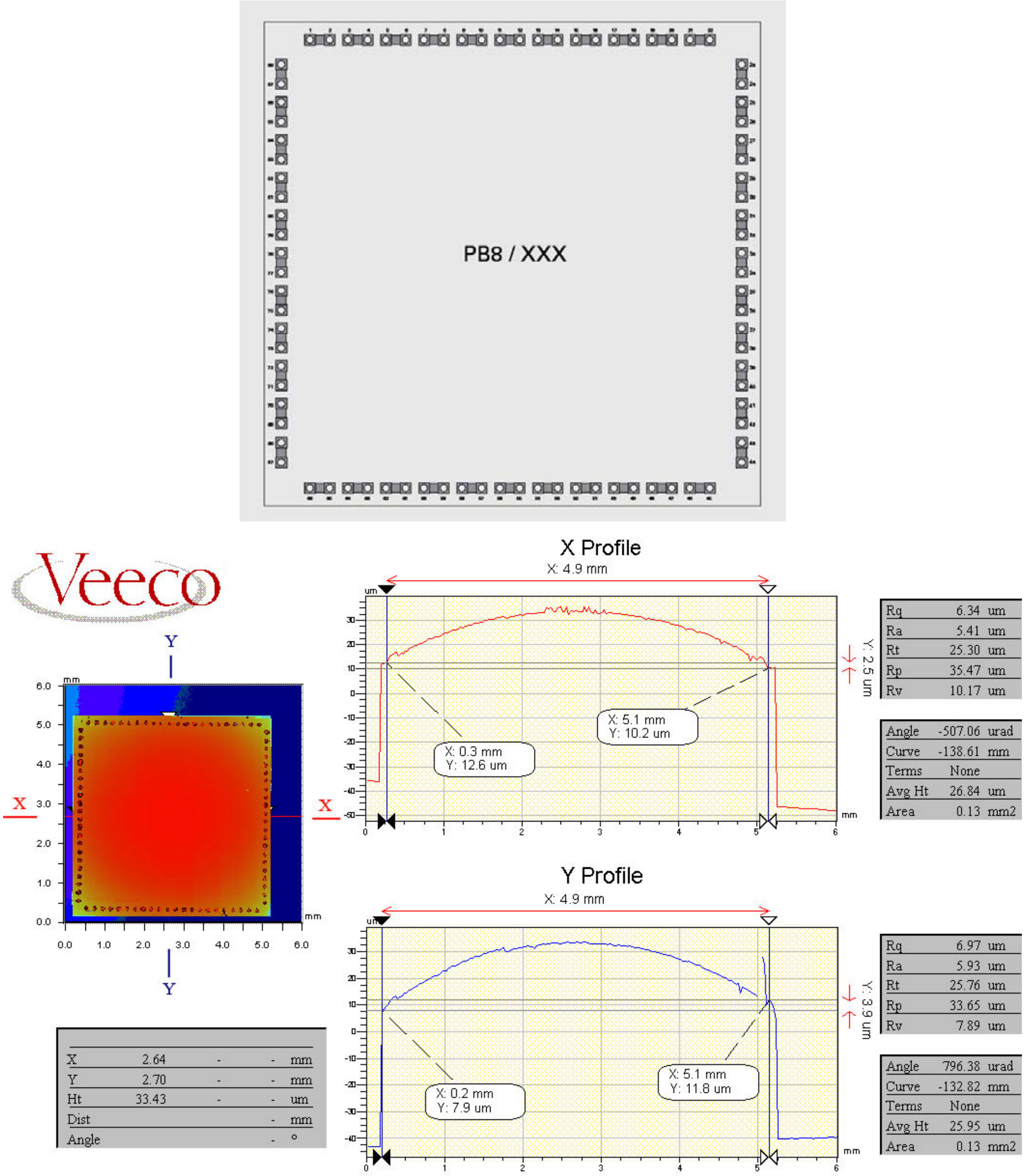
In this chapter, the status of thin electronic assemblies has been briefly reviewed. Die thinning and flexible substrates have also been discussed.

CHAPTER 3 PREPARATION OF THIN SILICON DIE AND TRANSFER OF THINNED DIE

3.1 EARLY WORK

Directly attaching a thin silicon die onto a flexible substrate is very difficult because the thin die is too fragile to handle using conventional techniques. For most ICs, the integrated circuit is fabricated only on one side of the silicon die using a series of microfabrication processes such as doping, deposition, and etching. The composition of the circuit layer is different from that of the silicon portion, generating a nonsymmetrical structure. When the die thickness is significantly reduced, the thin IC tends to warp, and the curvature increases with the decreased die thickness. Figure 3.1 displays the curvatures of a 50µm PB8 die in the x and y directions. Die placement on the substrate is usually accomplished with a precise pick and place machine. The accuracy of the die placement onto the substrate depends on the image clarity and the position precision of the aligning patterns on both. A warped die generates a deformed image, and in the worst case, the deformed image of the alignment pattern cannot be recognized by the machine. The die curvature also affects the planarity of the interconnection bumps on the warped die, degrading the contact between the bumps and the matching pads on the substrate.

This poor bump planarity tends to prevent the formation of uniform interconnections between the die and substrate, and often substantially lowers the assembly yield.



X	2.64	-	-	mm
Y	2.70	-	-	mm
Ht	33.43	-	-	um
Dist			-	mm
Angle			-	°

Rq	6.34	um
Ra	5.41	um
Rt	25.30	um
Rp	35.47	um
Rv	10.17	um

Angle	-507.06	urad
Curve	-138.61	mm
Terms	None	
Avg Ht	26.84	um
Area	0.13	mm2

Rq	6.97	um
Ra	5.93	um
Rt	25.76	um
Rp	33.65	um
Rv	7.89	um

Angle	796.38	urad
Curve	-132.82	mm
Terms	None	
Avg Ht	25.95	um
Area	0.13	mm2

Figure 3.1 The Top Profile of 50µm PB8 Test Die

To avoid the problems associated with thin silicon dies, a process that began by assembling a normal thickness die and followed by thinning of the bonded die was attempted in the early work of this research. A normal thickness die was placed face down and bonded on an LCP substrate by thermal compression bonding, and then the bonded die was etched by exposing the backside of the die to plasma. The process flowchart is shown in Figure 3.2. In this process, the die attachment could be easily performed through a typical surface mount technology assembly, similar to that used in conventional flip chip assemblies. However, lateral etching of the die sidewalls occurred during the course of thinning with deep silicon reactive ion etching (RIE). Figure 3.3 displays the lateral etching of the silicon die edge after two hours of RIE.

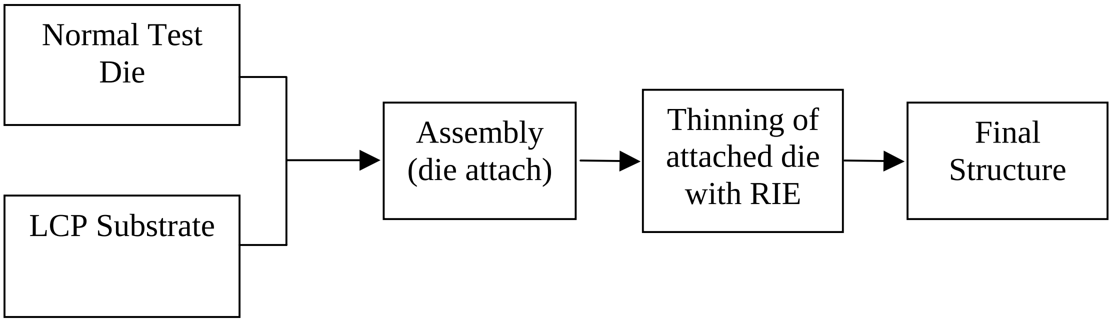


Figure 3.2 Illustration of Post Die Thinning Process

This kind of lateral etching is caused by the plasma loading effect, where the etch rate is dependent on location. The silicon etching rate at the die edge is faster than that in the center. To prevent the lateral etching of the die, photoresist was dispensed and cured around the perimeter of the assembled die. When the sidewalls of the die to be thinned were protected with photoresist, a silicon fence was formed during etching around the thinned die, as shown in Figure 3.4.

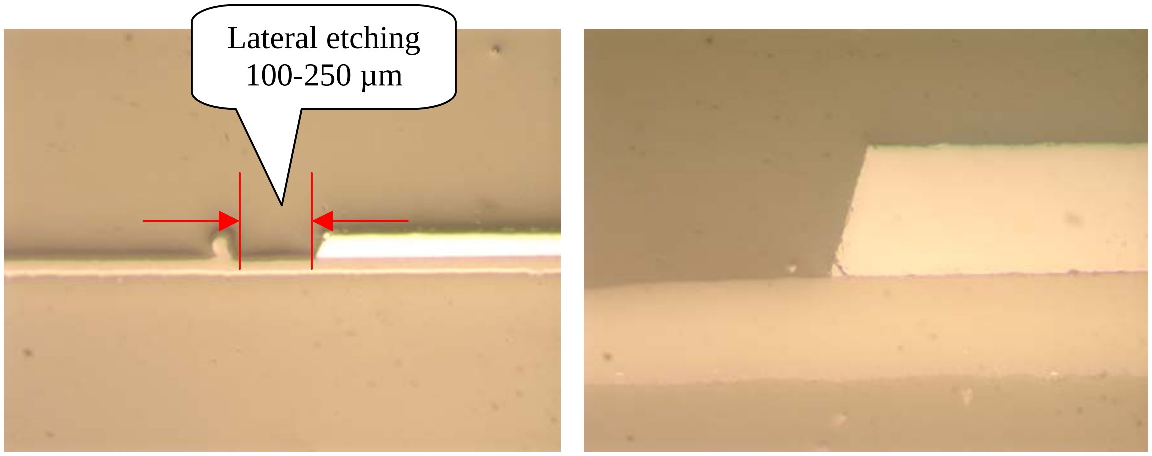


Figure 3.3 Undercut of Die Sidewall after RIE

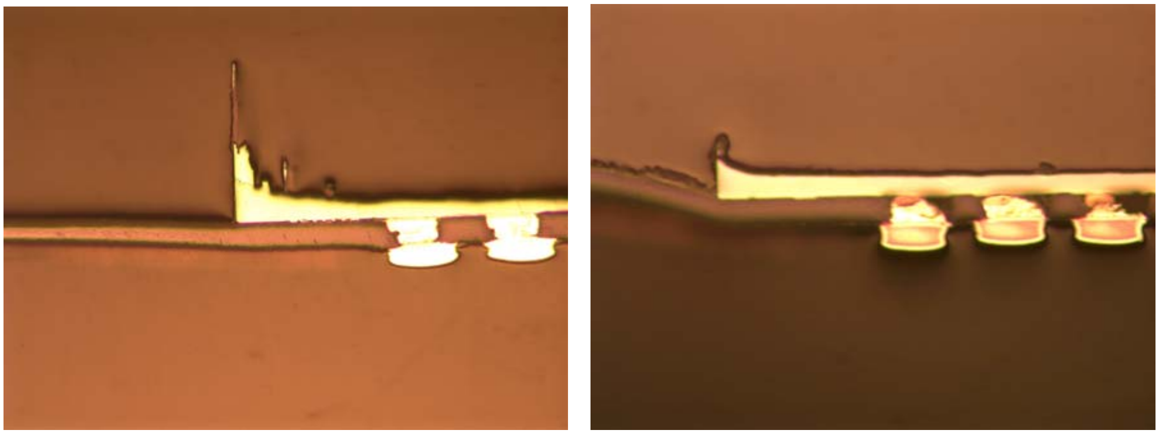


Figure 3.4 The Remaining of Silicon Fence Around the Thinned Die After the Completion of Deep Silicon RIE

A pre-thinning process was developed to replace the post-thinning process described in the previous paragraphs. Here, the die was thinned down to the target thickness prior to assembly (Figure 3.5). Mechanical grinding was introduced to replace the deep silicon RIE (plasma milling) to obtain better thinning uniformity. Dies were placed face down and hot laminated onto a flat glass disc with a temporary adhesive. The mounted dies were thinned by an outside vendor from the backside until the target thickness was reached.

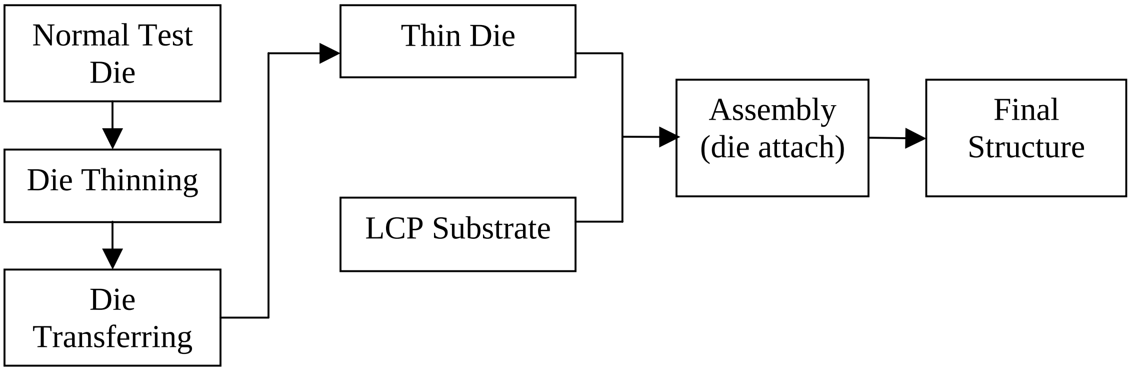
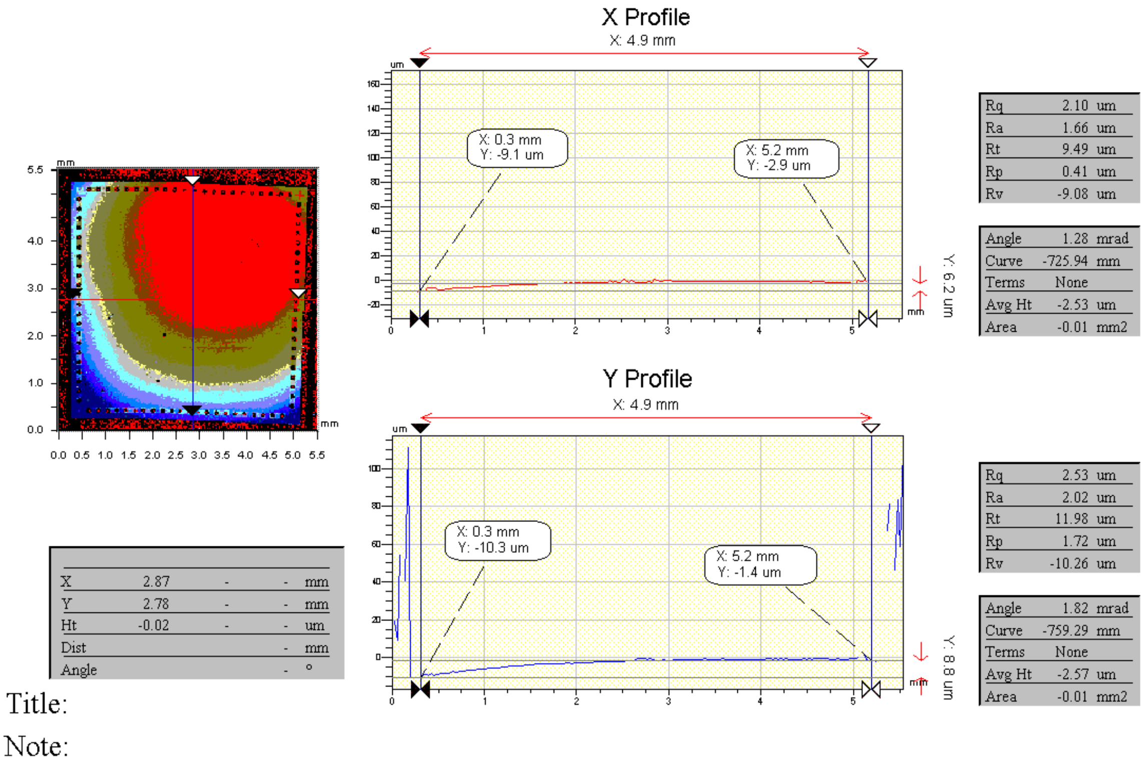

Normal Test Die
Die Thinning
Die Transferring
Thin Die
LCP Substrate
Assembly (die attach)
Final Structure

Figure 3.5 Illustration of Pre-Die Thinning Process

Thinned dies were successfully achieved with this thinning method. Attachment of the delicate thinned die to a handling die was used in order to solve the die handling problem. The backside of the thinned die was attached to a thick flat die with a temporary adhesive, and the circuit side was released from the glass disc. The image in Figure 3.6 shows the result obtained, with a considerably flatter top profile compared to the image in Figure 3.1. Thus, the transferred thin die could be handled and assembled with conventional assembly processes. After die attachment, the thin die assembly was achieved by releasing the handling die.


X Profile
X: 4.9 mm
X: 0.3 mm
Y: -9.1 um
X: 5.2 mm
Y: -2.9 um
Y: 6.2 um
um
mm
Y Profile
X: 4.9 mm
X: 0.3 mm
Y: -10.3 um
X: 5.2 mm
Y: -1.4 um
Y: 8.8 um
mm
5.5
4.0
3.0
2.0
1.0
0.0
0.0 0.5 1.0 1.5 2.0 2.5 3.0 3.5 4.0 4.5 5.0 5.5

Rq	2.10	um
Ra	1.66	um
Rt	9.49	um
Rp	0.41	um
Rv	-9.08	um

Angle	1.28	mrad
Curve	-725.94	mm
Terms	None	
Avg Ht	-2.53	um
Area	-0.01	mm2

X	2.87	-	-	mm
Y	2.78	-	-	mm
Ht	-0.02	-	-	um
Dist			-	mm
Angle			-	°

Rq	2.53	um
Ra	2.02	um
Rt	11.98	um
Rp	1.72	um
Rv	-10.26	um

Angle	1.82	mrad
Curve	-759.29	mm
Terms	None	
Avg Ht	-2.57	um
Area	-0.01	mm2

Title:
Note:

Figure 3.6 The Top Profile of Transferred 50μm Thickness PB8 Die

This process worked well and was used in early investigations. However, the quality of the thinned die was very poor, and the yield of thinned dies was less than 50%, as the die edges were often chipped and broken due to grinding impact during the grinding process. In order to improve thinning quality and yield, a modified waferscale thinning process was selected to replace this individual die thinning process that limits exposure of the die edges that are so vulnerable to damage. This thinning process significantly improved the thinning yield and thinned die quality. The following paragraphs describe this process, including wafer thinning, die transferring and die bumping.

3.2 DICING BEFORE THINNING PROCESS

In order to improve the thinning quality and yield, a modified waferscale thinning process was tested. 100-125μm deep grooves were sawn into the dicing streets on the front side of the wafer before thinning. The diced wafer was then sent to APTEK (San Jose, CA), a grinding vendor, for thinning. The diced wafer was mounted on a grinding fixture with a temporary adhesive. Backside thinning removed the bulk silicon. When the thickness of the thinned die was less than the depth of the grooves, the grids of the groove were exposed and the thinned wafer automatically became an array of thinned dies. The thinning process continued until the thickness reached the target value of 50μm. After completion of thinning, the thinned dies were released from the grinding fixture by dissolving the adhesive. The new process had a high yield and the die edges were relatively undamaged.

In this dicing before thinning process, whole wafer grinding occurs until the wafer thickness is less than the groove depth. The die edges are exposed and subjected to grinding impact only at the end of the process compared to individual die thinning. This shortens the impact time significantly, improving the die quality and survival. Another benefit to this approach is that it avoids the need to directly dice the thin wafer in the waferscale thinning process, which would also easily damage the thin dies.

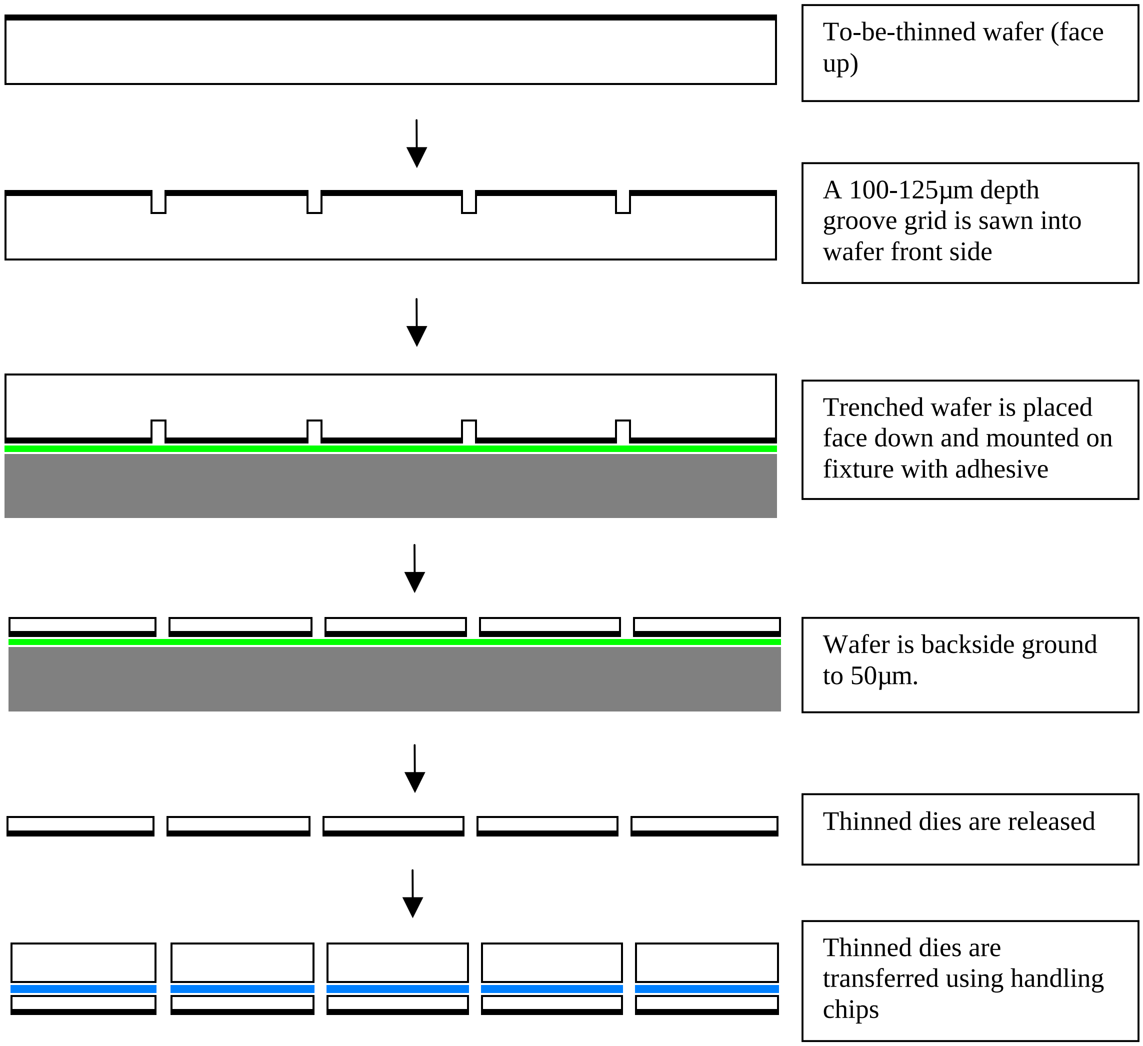
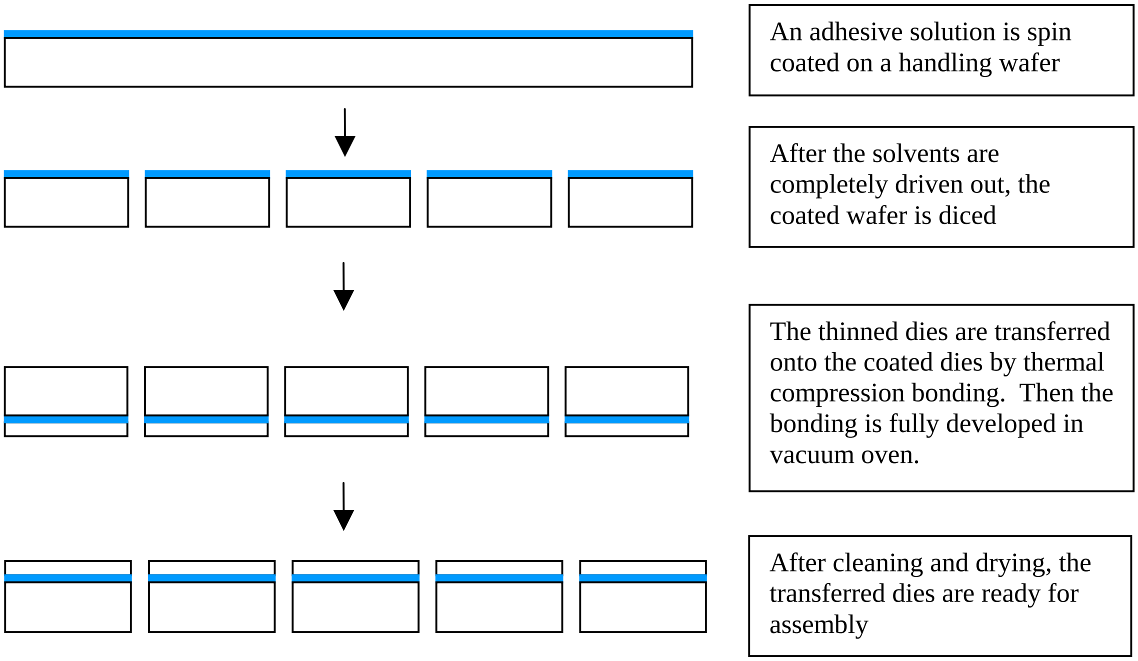

To-be-thinned wafer (face up)
A 100-125µm depth groove grid is sawn into wafer front side
Trenched wafer is placed face down and mounted on fixture with adhesive
Wafer is backside ground to 50µm.
Thinned dies are released
Thinned dies are transferred using handling chips

Figure 3.7 Flowchart of Wafer Dicing before Thinning Process

3.3 TRANSFER OF THINNED TEST DIE

For ease of handling through the assembly process, thinned dies were transferred onto thick flat handling dies with temporary adhesive. In this process (Figure 3.8), an adhesive was employed to temporarily bond the thinned die on the handling die. The adhesive, manufactured by Chase Corporation (Pittsburgh, PA), is a mixture of 35%wt acrylic based polymer with the solvents 50%wt toluene and 15%wt methyl ethyl ketone (MEK). The adhesive was spin-coated on a handling silicon wafer for 30 seconds. The as-coated wafer was heated at 90°C for 2 hours. After drying, the adhesive had solidified, forming a thin coating on the handling wafer. The coated wafer was diced into pieces matching the size of the thin dies. The coated handle dies were singularized from the diced wafer, and then dehydrated in a vacuum oven at 150ºC for 2 hours.

Bonding of the thinned dies to the coated handling dies was carried out using a thermal compression bonder. Each coated handling die was accurately aligned and placed on a thin die. Heat and pressure were applied to the handle through the nozzle. The adhesive was softened and tacked the handle on the backside of the thin die. To complete the bonding process the combined handling die/thinned die was heated in a vacuum oven for a given time period.



An adhesive solution is spin coated on a handling wafer

After the solvents are completely driven out, the coated wafer is diced

The thinned dies are transferred onto the coated dies by thermal compression bonding. Then the bonding is fully developed in vacuum oven.

After cleaning and drying, the transferred dies are ready for assembly

Figure 3.8 Flowchart of The Thinned Die Transfer Process

After the completion of the die transfer step, the transferred thinned dies were ready for stud bumping, in which gold balls as interconnection material were bonded onto the bondable pads on the thinned die. This will be discussed in detail in the next section. Some die damage was observed during the bumping process and was found to be related to entrapped voids within the adhesive between the thinned die and the handling die (Figure 3.9). A design of experiments (DOE) for the die transfer process was therefore conducted in order to achieve minimal voiding within the adhesive layer. Four parameters could be adjusted: coating thickness, bonding temperature, bonding time and bonding pressure. Due to the spin coating process used for the adhesive application, the adhesive thickness was determined by the spin speed, so the parameter of coating thickness was replaced by spinning rate. Influential parameter effects can be identified through DOE analysis for bonding efficiency, which is defined as the ratio of the bonded area to the total bondable area.

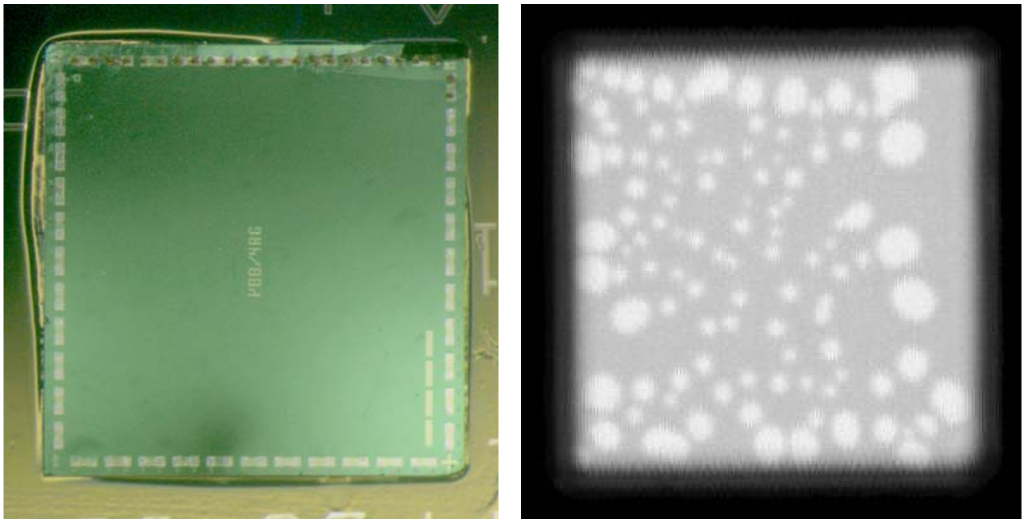

(a) die fractured during stud bumping (b) entrapped voids under die

Figure 3.9 Die Fractured During Stud Bumping and Entrapped Voids

For these four parameters, a full-factorial design would require $2^4 = 16$ runs, which would be very expensive. The Taguchi design of experiments (DOE) approach offers a more efficient way to arrange experiments while still maintaining effectiveness. Table 3-1 shows the L_8 orthogonal arrays, with "0" and "1" representing low and high levels, respectively, which are listed in Table 3-2. Instead of 16 runs, only eight runs are required using this approach. Five replications were tested for each run. The last column in Table 3-1 lists the average values of bonding efficiencies obtained.

Table 3-1 L_8 (2^7) Orthogonal Arrays

Run #	Spin Rate	Temperature	Time	Force	Efficiency (%)
1	0	0	0	0	17.47
2	0	0	0	1	23.87
3	0	1	1	0	95.17
4	0	1	1	1	92.80
5	1	0	1	0	18.02
6	1	0	1	1	16.98
7	1	1	0	0	97.97
8	1	1	0	1	99.50

Table 3-2 Two Levels of Process Parameters

	Low level (0)	High level (1)
Spin-Coating Rate (RPM)	500	1000
Bonding Temperature (ºC)	110	160
Bonding Time (hour)	2	12
Bonding force (gram-f)	400	800

Once the results were available, the data were analyzed to identify influential parametric effects. The one-factor effects were investigated and the results are displayed in Figure 3.10. In each one-factor plot, the vertical axis represents the magnitude of the bonding efficiency and the horizontal axis is one of the four parameters. The bonding efficiency values under the low and high levels of each parameter are connected to show the trend. It can be seen that three of the parameters (spin rate, bonding time and pressure) have no significant effect on the bonding efficiency compared to the effect of the bonding temperature, so bonding temperature was the main effect factor. Based on these results, the die transferring parameters were determined as spinning rate = 1000 rpm, bonding temperature =160°C, bonding time = 2 hours and bonding force = 400g-f. The die transfer with the optimized process achieved was proved to be voids-free, as shown in the C-SAM image in Figure 3.11. These parameters were therefore used for transferring thinned PB8 test dies. The transferred thin PB8 die is displayed in Figure 3.12 (topview) and Figure 3.13 (cross-section).

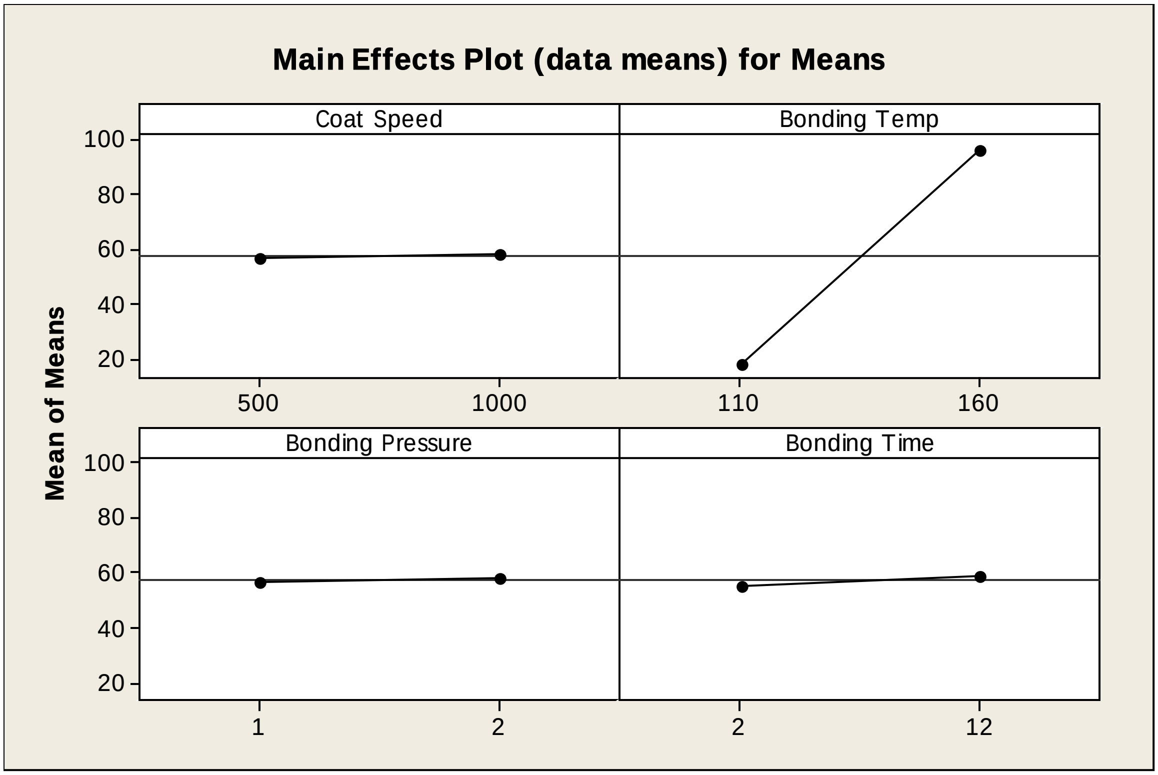


Figure 3.10 The Main Effects Plots

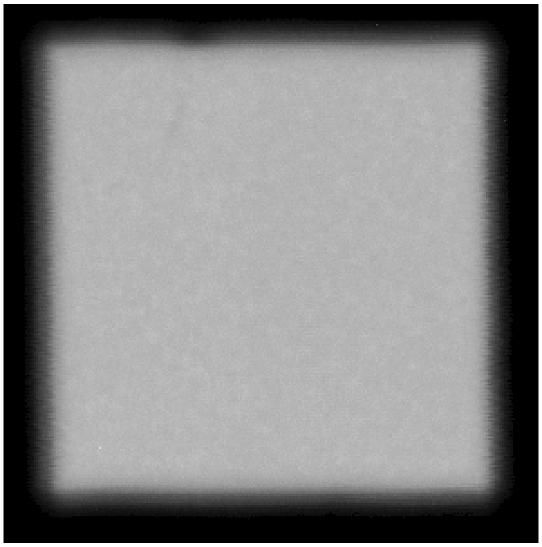


Figure 3.11 The C-SAM Picture of Voids-Free Die Transfer with the Optimized Process

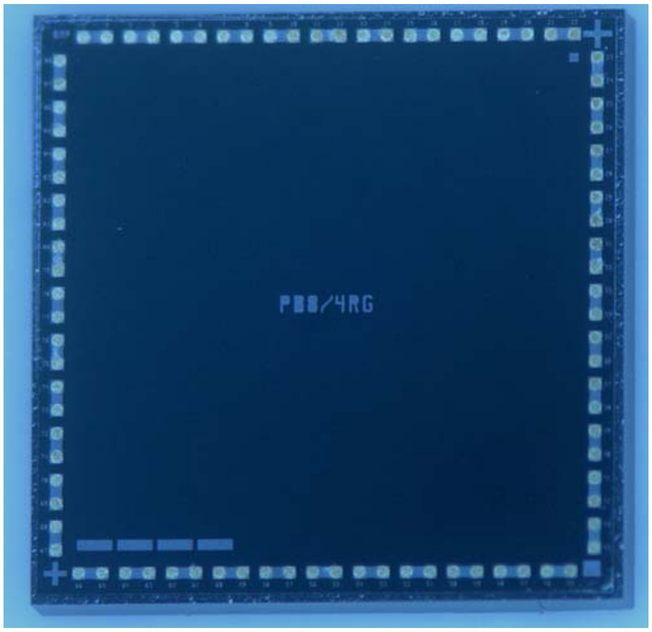


Figure 3.12 Topview of 50μm Thickness PB8 Die on Handling Chip

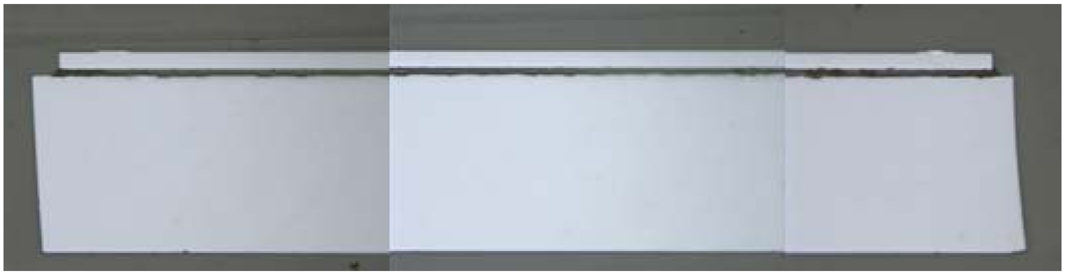


Figure 3.13 Cross Section of 50μm Thickness Die on Handling Chip

3.4 GOLD STUD BUMPING OF TRANSFERRED DIE

Gold interconnections were adopted for this work due to their reliability in both cold and high temperature environments. Gold stud bumps were placed on the die bond pads through a modification of the "ball bonding" process used in conventional wire bonding. The transferred die is placed face up and held on a vacuum stage, where the die is heated. In ball bonding, a predetermined length of Au wire protrudes from the capillary and is melted to form a ball at the end of capillary tip. The capillary brings the ball in contact with the bond pad on the die. This ball is pressed against the bond pad with mechanical force, heat, and ultrasonic movement (ultrasonic energy) to create a metallurgical bond. The ball bonding process is finished by breaking off the bond wire to begin another cycle.

In this work, Au stud bumping was accomplished using an automatic Hughes 2460-V wire bonder with optional software to facilitate bump formation. The bonding profile utilized optimal values for the force, ultrasonics, time, and die temperature. Due to the low melting temperature of the temporary adhesive in the transferred die, the die was heated to 90°C, preventing the re-melting of the adhesive. This stage temperature is relatively low compared to conventional bonding stage temperatures. To compensate for this lower stage temperature, the bonding force had to be increased to 55g-f and the ultrasonic displacement set to 1µm to achieve reliable bonds. Figure 3.14 shows the Au stud bumps on the PB8 test die. On average, the height of the gold bumps was 50µm.

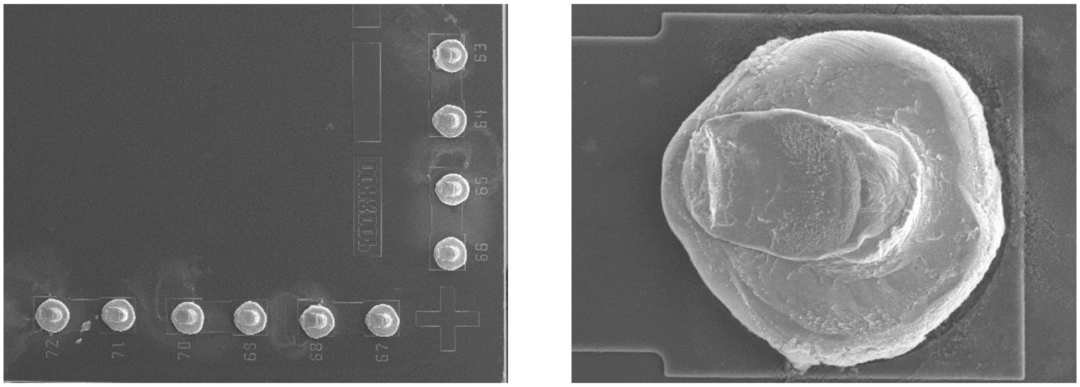


Figure 3.14 Close-up of Au Stud Bumps on the PB8 Test Die

3.5 SUMMARY

Due to the occurrence of die edge etching in the samples treated with deep silicon plasma etching, the results of the post thinning process were deemed unacceptable for this application. The individual die pre-thinning process offered another possibility for producing 50μm thick dies, but severe edge damage to the thinned dies occurred after grinding, lowering the yield considerably. The poor quality of the thinned dies also negatively affected the sequential bumping process and assembly with thermal compression bonding.

Ultimately, a dicing before thinning process was developed, with a high yield and high quality of 50μm thick dies. This method avoids problems due to the die edge being exposed to grinding impact during the early stages of the process, experienced in the individual die thinning process.

Mounting the thinned die on a thick flat handling die in order to maintain the die flatness eased handling problems. The transfer process was studied using a design of experiments approach. The experimental results indicated that the die transfer temperature was the most important factor for minimizing entrapped voids in the adhesive

Gold stud bumps were bonded on to bondable pads on the transferred thin die using a wire bonding machine. A lower stage temperature (90°C) was used to prevent the adhesive from softening and flowing during the bonding process. To compensate for this lower stage temperature, the bonding force had to be increased to 55g-f and the ultrasonic displacement set to 1μm in order to achieve reliable bonds. At the end of the preparation stage, gold stud bumped thin PB8 dies mounted on handling dies were ready for use in the subsequent assembly processes.

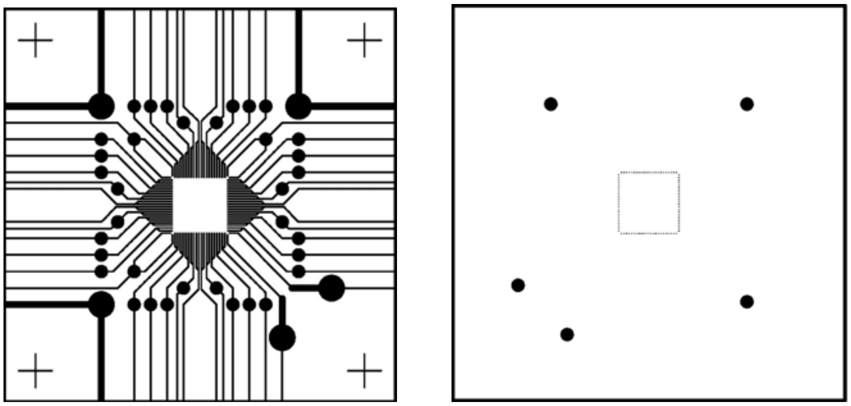
CHAPTER 4 PREPARATION OF FLEXIBLE LCP SUBSTRATES

4.1 OVERVIEW

A backside assembly substrate design was used in order to create a thinner embedded membrane structure compared to those possible using a conventional front side assembly design. Conventional clean room fabrication techniques (photolithography, wet etching, dry etching, and metallization) were employed to build these flexible LCP substrates. The details of the fabrication process will be described in this chapter, along with an explanation of the process flow.

4.2 FLEXIBLE SUBSTRATE PATTERNS AND MATERIALS

The backside design substrate pattern for the PB8 test die includes two fabrication patterns: a bottom circuitry pattern and a via-side pattern design, both of which are shown in Figure 4.1. The width of the copper trace on the bottom side was 175µm (7 mil), which is larger than the desired final line width to compensate for the copper lateral etching commonly encountered in wet etching. The via design diameter was 50µm (2mil), again based on a consideration of lateral etching.



(a) bottom circuitry pattern (b) via-side pattern

Figure 4.1 Backside Design Substrate Patterns for PB8 Test Die

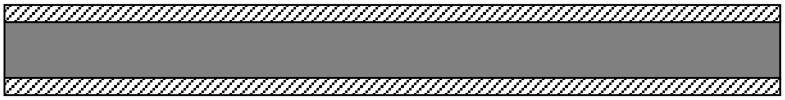
A double-sided copper clad liquid crystal polyester with a melting temperature of 315°C was used in this work, and was supplied by Foster-Miller (Boston, MA). Its properties are specified in Table 4-1.

Table 4-1 LCP Sheet Material Properties [41, 42, 43, 44, 45]

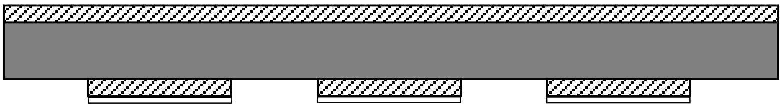
	LCP	
Dielectric Thickness, mil	2.0	-
Metal Cladding	Rolled Annealed Cu	-
Metal Thickness, µm (oz/ft^2)	18 (0.5)	-
Tensile Modulus, GPa	3.9	IPC – 2.4.19
Tensile Strength, MPa	98	IPC – 2.4.19
In-Plane CTE ($T < T_g$), ppm/K	8	IPC – 2.4.41.3 (TMA 30 – 150 °C)
Solder Resistance, °C	288+	IPC – 2.4.13
Thermal Conductivity Coefficient, W/m-°C	0.5	Kemtherm QTM – D3
Melt Temperature, °C	Up to 350	DSC
Dielectric Constant	2.9 (1 – 10 GHz)	IPC – 2.5.5.5.1
Dissipation Factor	0.002 (1 – 10 GHz)	IPC – 2.5.5.5.1
Surface Resistivity, ohms	3.4 E13	IPC – 2.5.17
Volume Resistivity, ohm – cm	3.4 E15	IPC – 2.5.17
Dielectric Strength, V/mil	4000	ASTM – D – 149
Chemical Resistance, Pass/Fail	Pass	IPC – 2.3.4.2
Water Absorption, %	0.04	IPC – 2.6.2 (23 °C/24 hrs)
Water Absorption Dimensional Change (CHE), ppm/% RH	4	60 °C
Flammability	VTM – 0	UL - 94

4.3 LCP SUBSTRATE FABRICATION PROCESS FLOW

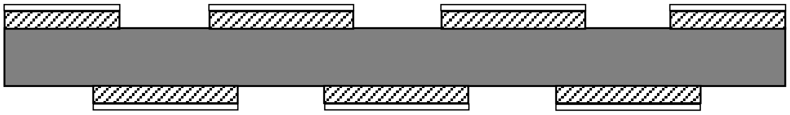
To build this backside design LCP substrate, the process was divided into three phases: bottom circuit fabrication, via formation and copper trace surface finishing. The process flow is illustrated in Figure 4.2 and Figure 4.3.



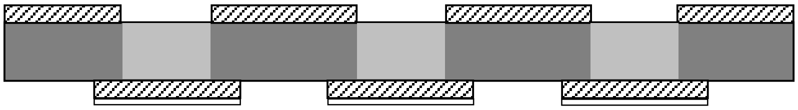
(a) Dielectric Materials with Adhesiveless Copper



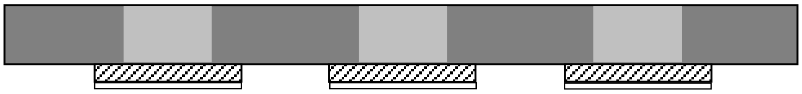
(b) Copper Circuitry Patterning



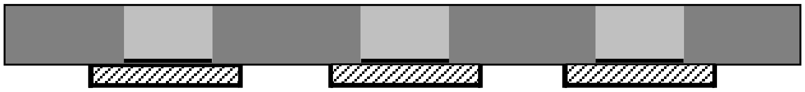
(c) Via Mask Patterning



(d) Via Etching



(e) Via Side Metal Etching



(f) Surface Finish

■ LCP □ Photoresist ▨ Copper ▒ Via ▬ Surface Finish

Figure 4.2 Scheme of Backside Assembly Design Substrate Fabrication

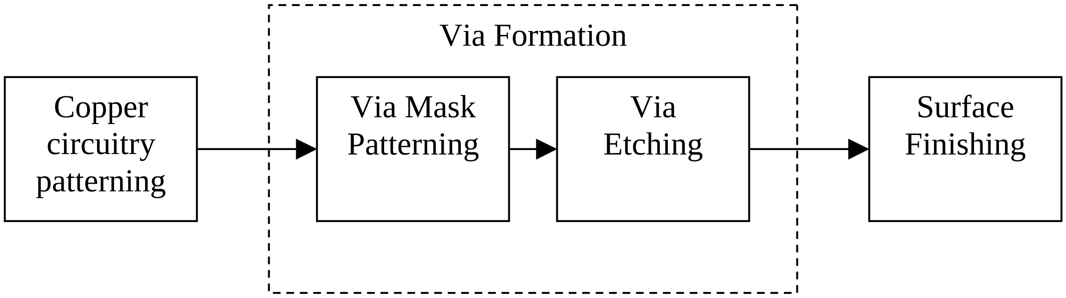

Via Formation
Copper circuitry patterning
Via Mask Patterning
Via Etching
Surface Finishing

Figure 4.3 The Process Flowchart for LCP Substrate Fabrication

4.3.1 Bottom Cu Trace Pattern Fabrication

The copper circuitry was formed on one side of the double-sided Cu clad LCP sheet using photolithography and Cu wet etching. The LCP sheet was cut into pieces sized to accommodate three substrates. A piece of LCP sheet was clipped to a 5-inch wafer and dehydrated at 125°C for 30 min in a box oven. Prior to the spin coating of the photoresist, the dehydrated LCP sheet was exposed to gaseous hexamethyldisilazane (HMDS) for 10 minutes in a desiccator to promote the photoresist adhesion to the copper. A positive photoresist (AZ® 5214-E IR) was spin coated onto the copper surface at a spin rate of 3000 rpm. After soft baking at 105°C for 60 sec on a hot plate, an approximate 1 µm thick photoresist uniformly covered the LCP sheet. Transferring of the trace pattern was conducted using a Karl Suss Double Sided Mask Aligner. A photomask containing the circuit pattern was placed in close proximity to the photoresist side of the LCP sheet, then exposed to UV light for 7.5 sec. After the UV exposure, the LCP sheet was soaked in a diluted AZ® 400K developer bath (one part of developer with two parts of DI water) to develop the photoresist pattern. Fifteen seconds later the unexposed photoresist was developed away, resulting in a photoresist pattern matching the mask design. The substrate was then rinsed with DI water. The photoresist patterned LCP sheet was then hard backed at 125°C for 60 sec to increase the chemical resistance of the photoresist. At this point, the photoresist patterned LCP sheet was ready for copper etching.

In this work the fine pitch copper circuit was wet etched using a ferric chloride ($FeCl_3$) aqueous solution of 50g $FeCl_3$ in 150ml DI water. The exposed copper was etched away, exposing the LCP under the etched copper. After Cu wet etching, the photoresist covered copper remained in place and was exposed after rinsing the photoresist with acetone. At this point, the bottom side copper circuit was complete.

4.3.2 Via Formation

Upon completion of the bottom side circuit fabrication, the process entered the phase of via formation. The vias through the LCP layer were designed to provide interconnections between die pads and substrate copper pads. The fabrication started with the preparation of the via mask on the Cu layer on the opposite side to the bottom circuit. This was followed with dry etching of the via and stripping of the copper mask.

The via layout design was patterned in the clad Cu on the LCP sheet opposite the circuit pattern side. This patterned Cu was used as a dry etching mask. The Cu mask was fabricated using the same photolithography and Cu wet etching procedures as those described in the previous section. After wet etching, the Cu openings in the Cu mask exposed the LCP to be dry etched.

Inductively coupled plasma (ICP) etching was used for the dry etching to make vias through the LCP layer. The etching process used an STS advanced oxide etcher (AOE ^{TM}, manufactured by Surface Technology Systems). The LCP sheet to be etched was mounted on a 5-in wafer with the via Cu pattern side uppermost. To prevent the occurrence of discharge damage, the LCP sheet was held on the handling wafer using a temporary adhesive (supplied by Dynatex International, Santa Rosa, CA) that was carefully applied to be without voids. The wafer with the LCP sheet attached was loaded into the ICP etcher chamber. A pressure of 60 mTorr and a gas mixture of 35 sccm O_2

and 8 sccm CF_4 was used for etching. The mixture was activated by the 13.56 MHz generator to generate a plasma composed of reactive radicals such as electrons, cations and neutral particles. The openings in the copper provided a pathway for the plasma to etch away the polymer. Sixty minutes of dry etching removed the LCP within the openings, exposing the underside of the bottom copper. The via profile is shown in Figure 4.4.

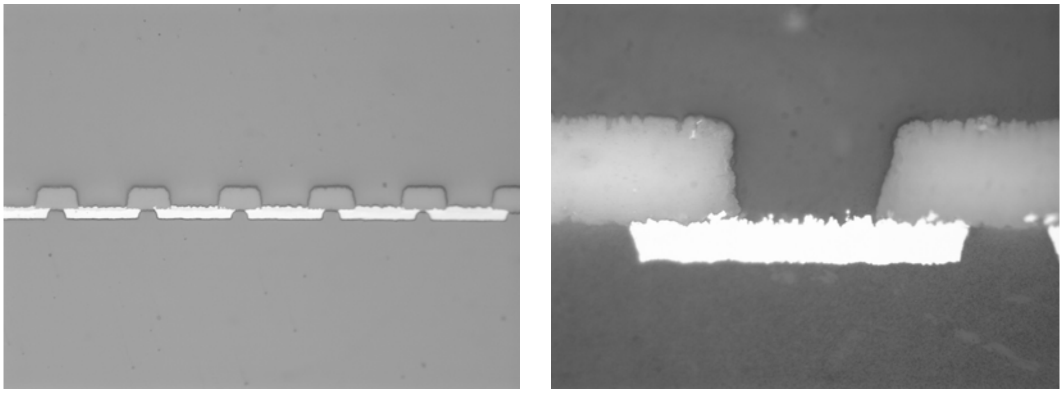


Figure 4.4 The Cross-section of the Vias in LCP Substrate

After the formation of the vias in the LCP, the via Cu mask was stripped by Cu wet etching. At this point, the copper pads within the vias had to be protected from wet etching. A third photomask was therefore designed to pattern photoresist covering the via pads. The stripping process was performed using photolithography and Cu wet etching. After Cu mask stripping, the backside design LCP substrate was almost complete.

4.3.3 Cu Trace Surface Finishing

A gold surface finish on the Cu pads was required for Au-to-Au thermal compression bonding. Due to copper migrating into the gold, a nickel (Ni) barrier is commonly used to prevent the copper from migrating into the gold. Formation of gold-to-gold interconnections requires a thick gold finish layer. In this research work, nickel and gold electroplating steps were performed to finish the LCP substrate.

First, Ni was electroplated. Prior to plating, the substrate to be plated was immersed in TSC Technic 1501 (supplied by Technic, Inc., Cranston, RI) cleaner solution at 60°C for 2-3 min for the removal of grease and organic residues. Then the substrate was cleaned in 5% v/v sulfuric acid aqueous solution for 2-3 min with ultrasonic agitation to eliminate the surface oxides from the copper. After rinsing with DI water, the cleaned substrate was ready for plating.

Figure 4.5 illustrates a typical electroplating system. For nickel electroplating, the substrate (cathode) to be plated is wired to the negative terminal of a power source, while a piece of nickel bar (anode) is connected to the positive terminal. Both are then immersed in the plating solution (bath), which has a composition as listed in Table 4-2. When the power is on, an electrical current flows through the system. As the current passes across the electrolyte, electrons are continuously supplied to the cathode, where positive Ni ions combine with electrons and are transformed into neutral Ni atoms that are deposit on the copper surface of the LCP substrate. Meanwhile, Ni atoms on the surface of the nickel bar are converted into positive Ni ions at the anode, entering into the plating solution to compensate for the loss of positive Ni ions due to the Ni-electron combination at the cathode. In this work, the plating current was adjusted to 2 mA and the plating process lasted for 30 min. A 3 to 5μm thick nickel layer was deposited on the copper surface. After rinsing with DI water, the nickel plated substrate was then ready for gold plating.

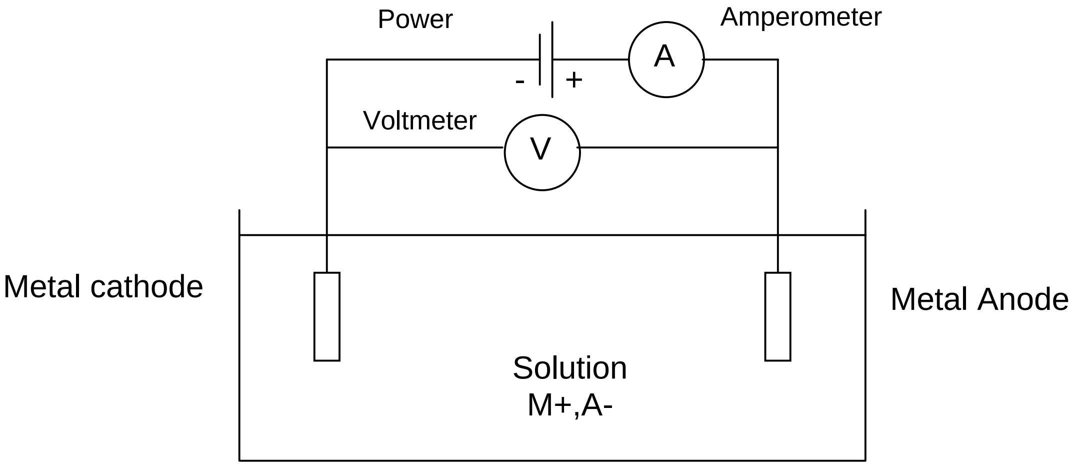


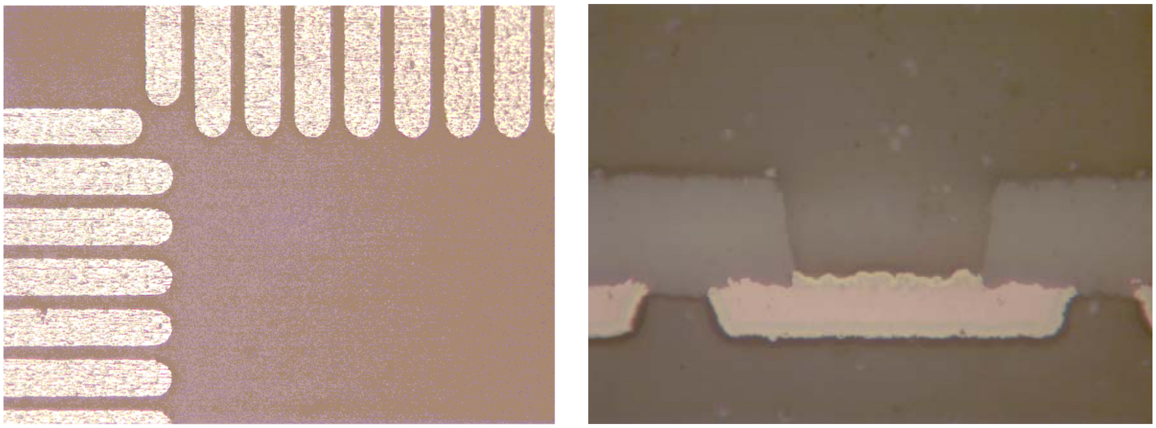
Figure 4.5 The Diagram of Electroplating System

Prior to the start of gold electroplating, the nickel plated substrate was electroplated in pre-plating solution (Orostrike C, supplied by Technic, Inc., Cranston, RI) at 37°C. This gold pre-plating insured better adhesion of the gold to the underlying nickel deposit. In this process, the substrate was connected to the negative terminal of the power supply and a piece of platinum mesh, which replaced the nickel bar was connected to the positive terminal. When the power was switched on, the chemicals in the pre-plating solution were ionized, and positive Au ions from the solution moved toward the cathode, depositing on the plated nickel. The current was set to 2 mA and the time was set to 2 min.

Table 4-2 Composition of the Nickel Electroplating Solution

Chemicals	Mount (g/L)
Nickel Sulfate	200
Nickel Chloride	5
Boric Acid	25
Ferrous Sulfate	8
Saccharin	3

Upon completion of the pre-gold plating step, the gold electroplating was performed. The plating connections were the same as those used for the pre-gold plating. 434 HS electrolyte (Technic, Inc., Cranston, RI) replaced the Orostrik C electrolyte. In this step, the current was kept at 2 mA for 30 min, depositing a 3-µm thick gold layer on the substrate traces and pads. After rinsing with DI water and air drying, a nickel/gold plated substrate suitable for the gold-to-gold interconnections had been fabricated.



(a) plated copper trace in bottomside (b) cross-section of plated LCP substrate

Figure 4.6 Ni/Au Plated LCP Substrate

4.4 SUMMARY

Three major steps were necessary for fabricating the backside assembly design LCP substrate, including bottom circuit fabrication, via formation and copper trace surface finishing. Clean room fabrication techniques were used in the substrate fabrication, including photolithography, wet etching for the copper pattern, dry etching for via formation, and electroplating for the copper surface finishing. The nickel/gold plated LCP substrates produced were deemed suitable for the backside assembly process.

CHAPTER 5 THERMAL COMPRESSION ASSEMBLY OF THIN FLIP CHIP IN LCP FLEX

5.1 EARLY WORK

After the completion of the die thinning and transfer, stud bumping, and substrate fabrication phases, the process moved into the assembly stage. In this stage, the gold stud bumped thin die was bonded with the LCP substrate forming the electrical connections. After sealing the assembly with another LCP sheet, the thin flip chip in LCP flex was finally produced.

In the early research of this project, eutectic tin lead solder (Sn63Pb37) was used to solder the bumps to the via pads. The solder paste was filled into the vias in the LCP substrate with a squeegee, and then reflowed. The as-reflowed LCP substrate was then cleaned, removing the flux residues. As the transferred die was mounted on the solder-deposited LCP substrate, the initial contacts between bumps on die and solder on the corresponding via pads were established. When the bonding temperature became high enough to melt the solder, the gold bumps were pushed into the molten solder, forming metallurgical contacts. After cooling, the corresponding joints formed within the vias. After bonding, the assembly was soaked in acetone for eight hours and the handling die was released when the adhesive was completely dissolved. In accordance with the design, an additional LCP sheet was laminated to seal the die, forming an embedded membrane structure. The process flowchart is shown in Figure 5.1.

The assemblies produced using this approach provided inconsistent electrical resistances. Cross-sectional pictures revealed a heterogeneous texture and the presence of embedded voids within the joints (Figure 5.2). These kinds of interconnections resulted in considerable resistance variations. Furthermore, early failures were observed in the course of air-to-air thermal shock testing. These joints were also brittle because of the formation of $AuSn_4$ which is very brittle. Gold dissolved into the molten SnPb solder and $AuSn_4$ formed during cooling and solidification according to the ternary phase diagram of Au-Sn-Pb. This occurred in both die attachment and LCP coverlayer lamination (sealing) steps.

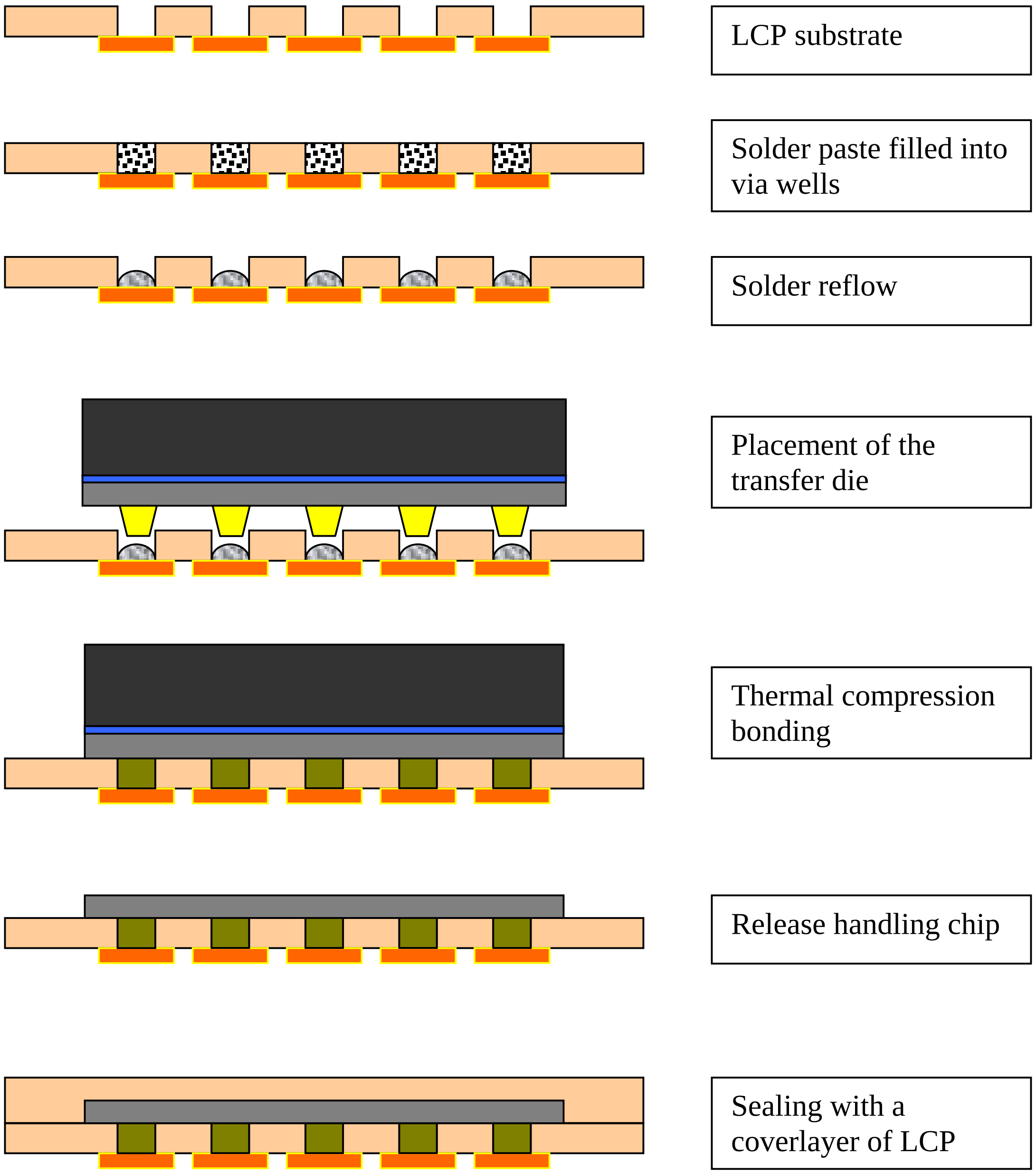
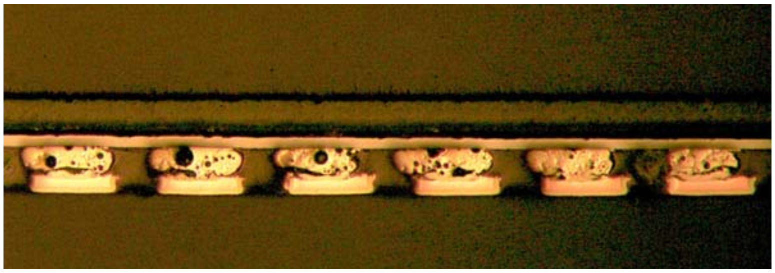
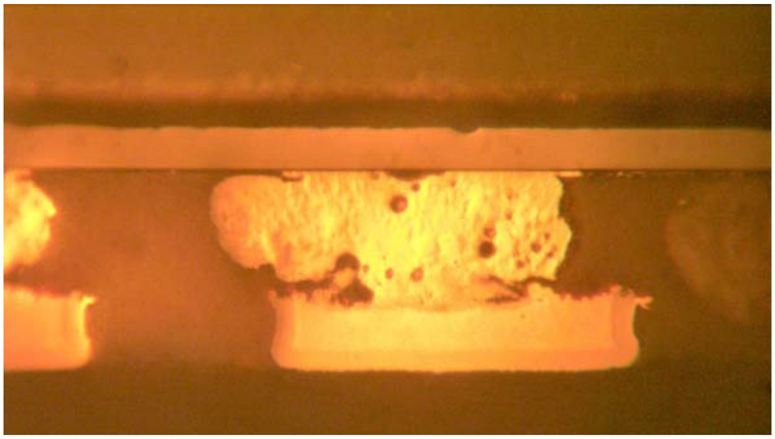

LCP substrate
Solder paste filled into via wells
Solder reflow
Placement of the transfer die
Thermal compression bonding
Release handling chip
Sealing with a coverlayer of LCP

Figure 5.1 The Assembly Process of an Thin Die in Package with the Assistance of Sn63Pb37 Solder Paste



(a) Low Magnification



(b) High Magnification

Figure 5.2 The Joints of Sn63Pb37-Gold Within the Via Wells Between the Thin Die and the LCP Substrate

There were additional problems with this process: solder overflowing under the die and bridging between traces. When the gold stud bump was pushed into the molten solder, any extra volume of solder tended to overflow between the die and the LCP. This overflowing solder caused bridging between adjacent joints, as shown in Figure 5.3.

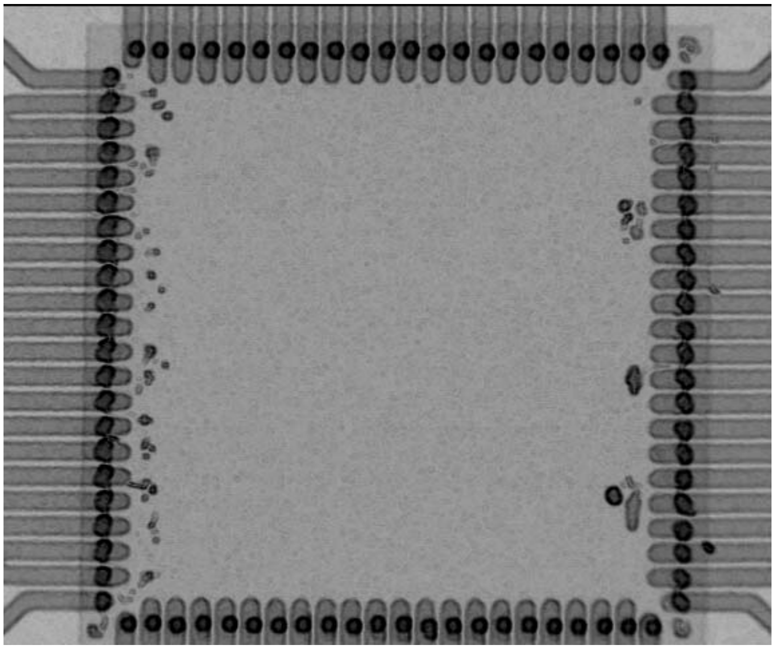


Figure 5.3 X-Ray Image of Overflowing Solder Under Die

Due to the process limitations governing the fabrication of the LCP substrates, copper trace lateral etching and via-to-trace misalignment may occur during the chemical etching and photolithography. In the worse cases, these defects may cause copper traces that fail to cover the whole via diameter, creating gaps. Molten solder escaped through these gaps and wet the nickel/gold plated traces on the bottom side, creating solder bridges between adjacent traces. Figure 5.4 shows such solder bridges.

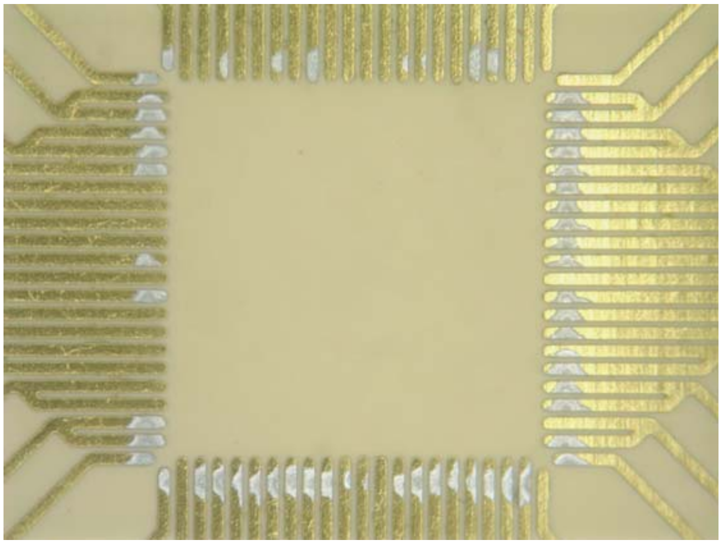


Figure 5.4 Solder Bridges Between Bottomside Traces Caused by Escaping Molten Solder

Obviously these problems increase the difficulty of the assembly process and lower the reliability of this kind of embedded assembly. At this point, using an assembly process with gold-to-gold interconnections was a better choice.

5.2 THERMAL COMPRESSION ASSEMBLY WITH GOLD-TO-GOLD INTERCONNECTIONS

The process of thermal compression assembly with gold-to-gold interconnections includes die attachment, release of handling die, and sealing steps. The transferred die was placed face down on an LCP substrate with a suitable thermal compression profile. The as-bonded part was then soaked in acetone until the handling die was separated from the bonded thin die. Finally, another LCP sheet was laminated on this intermediate to produce an embedded thin flip chip assembly. The process flowchart is shown in Figure 5.5.

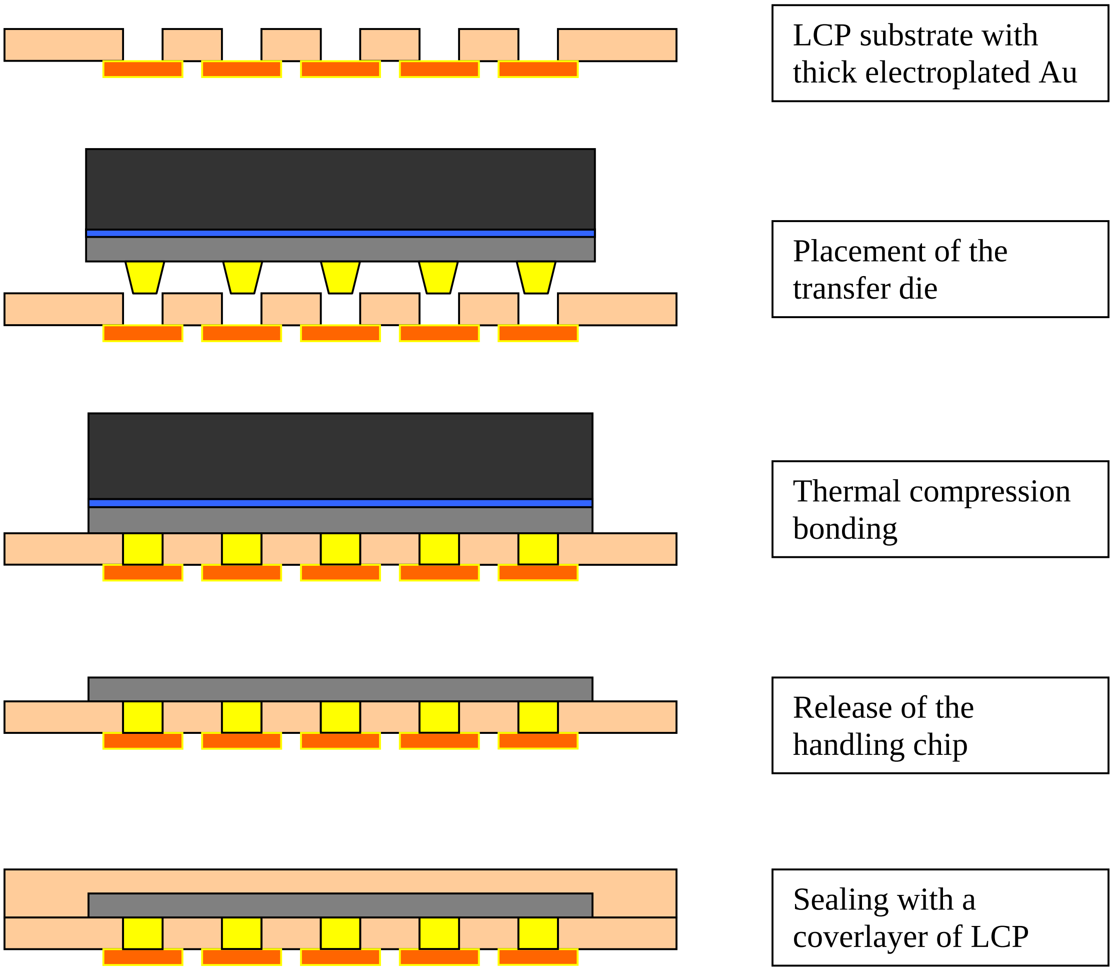

LCP substrate with thick electroplated Au
Placement of the transfer die
Thermal compression bonding
Release of the handling chip
Sealing with a coverlayer of LCP

Figure 5.5 The Assembly Process For an Thin Flip Chip in LCP Flex with Gold-to-Gold Interconnections

5.2.1 Issues Related to the Assembly Process

Formation of gold-to-gold interconnections demands that high temperature and force be applied during the course of the thermal compression bonding. High temperature excites gold atoms to move between the gold bumps and the plated gold on the via pads when they are in contact, thus enhancing joint formation. This technique typically requires bonding temperatures ranging from 350 – 400°C, and bonding forces up to 100g per bump [40].

As designed, the silicon die was directly bonded with the LCP substrate while the gold bumps were bonded with gold plated substrate pads within the vias. No additional adhesive was required. The LCP assumed the role of the adhesive in order to establish a bond between the die and itself. The bonding temperature had to be higher than the LCP melting temperature for the molten LCP to yield sufficient adhesion to bond with the silicon die in contact.

At the same time, the interconnections required a stable bottom circuit so that the bumps and corresponding via pads could be precisely aligned and bonded together. This required a temperature lower than the LCP melting point in order to prevent the deformation of the bottom circuit that would be caused by LCP reflow.

To meet these conflicting requirements, a non-symmetrical temperature profile was designed. The temperature on the bonding side was higher than the LCP melting temperature, allowing the surface LCP to re-melt to laminate the die, while the temperature of the bottom side (circuit side) was controlled to be as low as possible, keeping the deformation within the tolerance.

5.2.2 Setting-Up the Thermal Compression Bonding Profile

Four primary parameters are adjustable for controlling assembly quality, namely the arm (nozzle) temperature, chuck temperature, bonding time and bonding force. A design of experiment (DOE) with the die attachment process parameters was conducted to achieve better bonding quality. Normal thickness PB8 dies with gold stud bump and high melting temperature LCP coupons were used for these tests. The die shear strength was used to evaluate the bonding quality. The DOE was used to identify the influential parameter effects based on the data from the die shear test. As mentioned in Chapter 4, eight runs are sufficient using the Taguchi design of L_8 orthogonal arrays with two levels (Table 5-1). Each run was repeated five times. The parameter levels were predetermined based on the considerations stated in the previous section, listed in Table 5-2.

Table 5-1 L_8 (2^7) Orthogonal Arrays

Run #	Chuck Temp	Arm Temp	Time	Force	Average Shear Force (kg-f)
1	0	0	0	0	7.432
2	0	0	1	1	8.257
3	0	1	0	1	10.766
4	0	1	1	0	8.096
5	1	0	0	1	16.283
6	1	0	1	0	12.343
7	1	1	0	0	15.970
8	1	1	1	1	16.823

The one-factor effect plots in Figure 5.6 demonstrate the chuck temperature to be the most influential parameter for the process under these experimental conditions. A high chuck temperature improves the bonding quality. Arm temperature and bonding force also positively affected the bonding quality. Compared to these three parameters, bonding time at the peak temperature exhibited a negative effect for die bonding.

According to this result, high chuck temperature (300°C), a high arm temperature (410°C), large bonding force (5000g-f) and short bonding time (60sec) were set for the die bonding. For the later experiments, all die attachments were performed using these settings.

Table 5-2 The Two Levels of Thermal Compression Bonding Parameters

	Level 0	Level 1
Chuck Temperature (°C)	150	300
Arm Temperature (°C)	370	410
Bonding Time (sec)	60	300
Bonding Force (g-f)	1000	5000

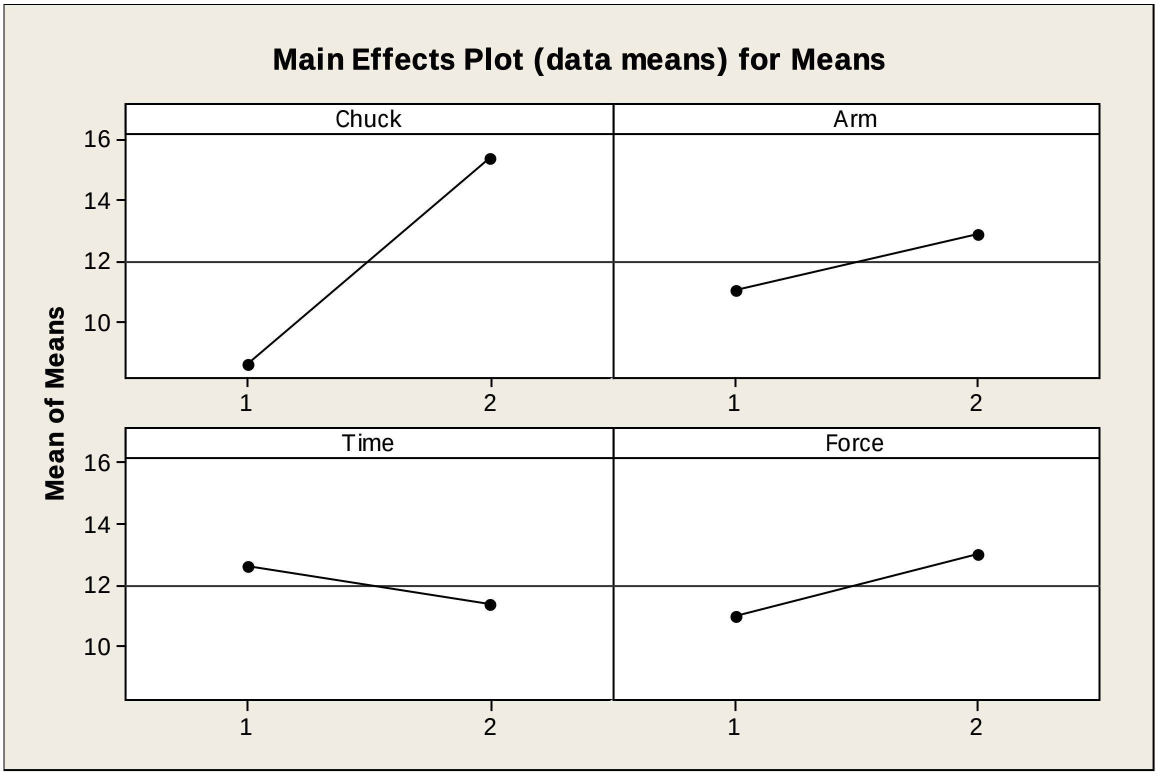


Figure 5.6 One–Factor Effects for Four Thermal Compression Parameters

5.3 SEALING WITH LOW MELTING TEMPERATURE LCP SHEET

After die attachment and release of the handling die, a thin PB8 flip chip on flex, an intermediate assembly, was achieved. As designed, a low melting temperature (m.p. = 285°C) LCP was then laminated on this intermediate to create the embedded membrane structure. The lamination process was performed on the same machine as that used in die attachment step. The lamination profile was set up by referencing the die attachment parameters. To protect the gold joints from external impact, the lamination force was reduced from 5000 to 1000g-f and the chuck temperature was lowered to 200°C. LCP with one side copper clad was used that had been prepared by etching the copper away from one side of the double sided copper clad LCP substrate.

The lamination arm held the LCP on the copper side and moved down to an intermediate position above the chuck. Once it contacted the assembly, heat and force were applied according to the predetermined process parameters. After completion of the lamination, the cover layer and intermediate assembly had become an integral embedded structure. Finally, the removal of the backside copper was performed. The backside copper was etched in a concentrated aqueous nitric acid solution, while the bottom circuit side was protected with a photoresist. After the protective photoresist was stripped away with acetone, the embedded 50μm thick PB8 flip chip package was completed. A cross-section of the final assembly is shown in Figure 5.7.

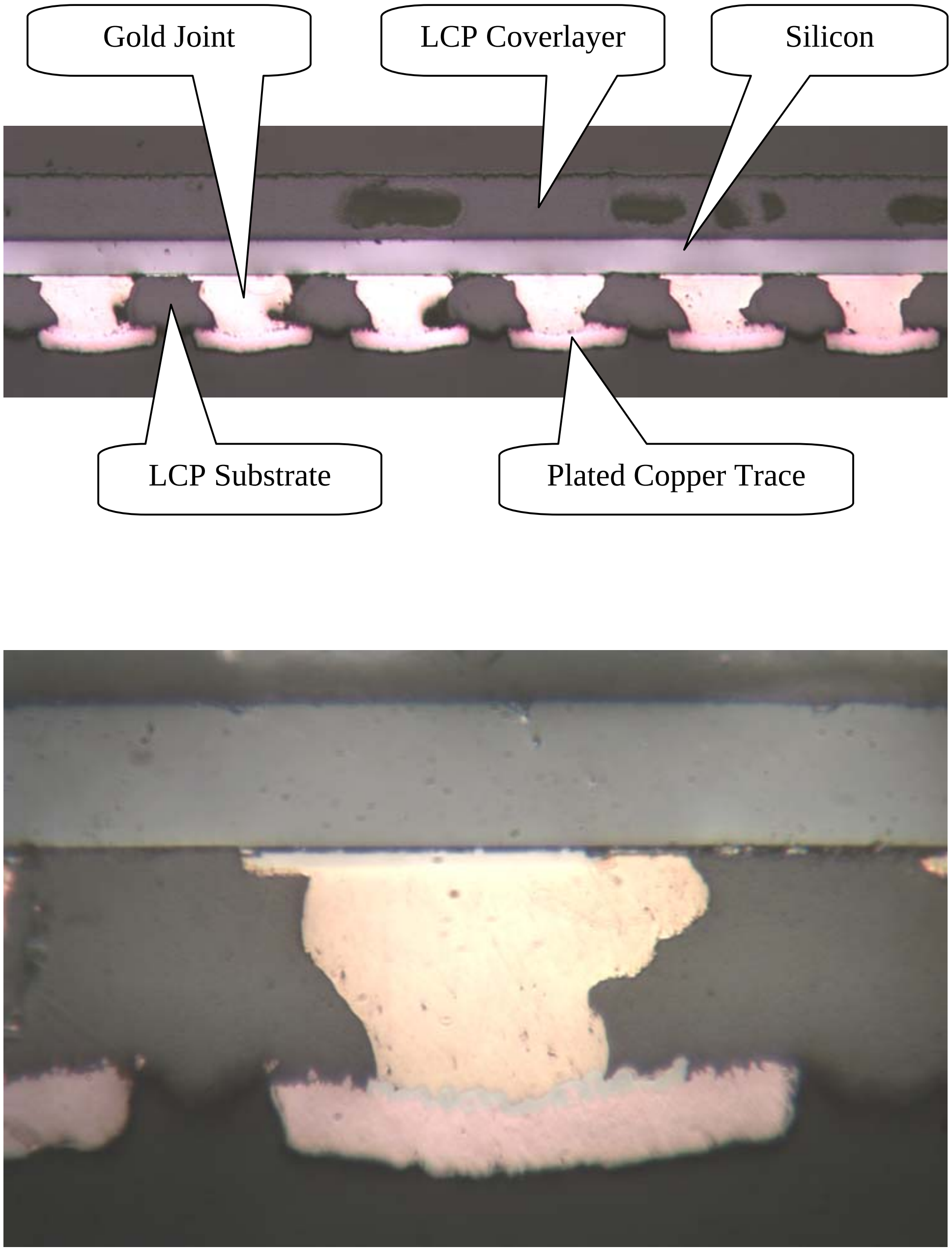

Gold Joint
LCP Coverlayer
Silicon
LCP Substrate
Plated Copper Trace

Figure 5.7 Cross-Section of Embedded 50µm Thick PB8 Flip Chip Package

5.4 SUMMARY

For the assembly stage, thin PB8 dies with gold bumps were bonded with backside assembly design LCP substrates to form integral structures using gold-to-gold interconnections and die-LCP lamination. After backside sealing with a low melting temperature LCP sheet, an thin PB8 flip chip in LCP flex was produced as designed.

Studies of the parameters controlling the attachment of the die revealed that a high chuck temperature, high arm temperature, large bonding force and short bonding time were beneficial for bonding quality.

CHAPTER 6 ELECTRICAL PERFORMANCE OF THIN OPERATIONAL AMPLIFIER IN LCP FLEX SUBJECTED TO MECHANICAL BENDING

6.1 OVERVIEW

Silicon demonstrates a change in its resistivity in response to the application of mechanical stress. This phenomenon is known as the piezoresistance effect [46]. Wymyslowski and coworkers investigated the relationship between resistance and mechanical deformation for a strip-shape resistor [47]. The general equation can be expressed as:

$$\frac{dR}{R} = \frac{d\rho}{\rho} + \varepsilon \cdot (1 + 2\nu)$$

where ρ is the bulk resistivity at a certain temperature and mechanical load, ε is the mechanical strain, and ν is Poisson's ratio. The relationship thus consists of two terms:

i. the term $\varepsilon\cdot(1+2\nu)$, which represents the geometric effect; and

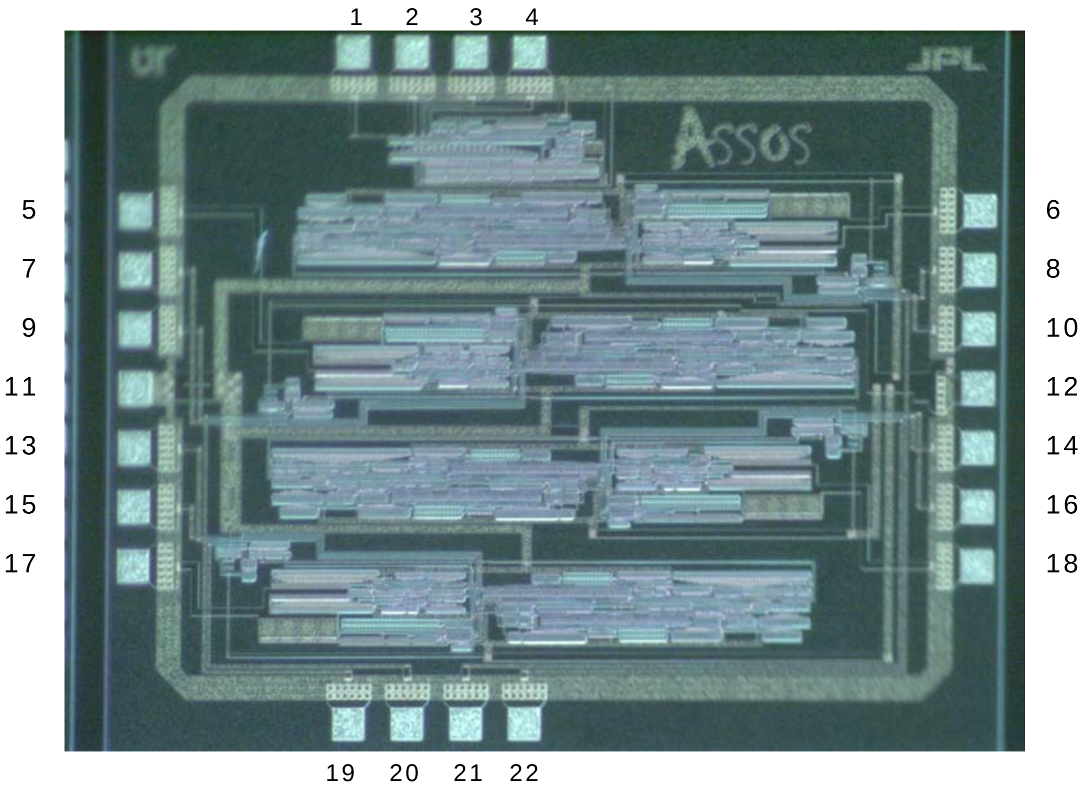
ii. the term $d\rho/\rho$, which describes the piezoresistive effect.

In metals the geometric effect dominates, while in semiconductors the piezoresistive effect is much larger than the geometric effect. Silicon is a typical piezoresistive material used to construct circuits.

The thin flip chip in LCP flex which is the focus of this research consisted of a silicon based IC, substrate with copper traces and gold joints. By design the assembly is flexible and deformation of the silicon is expected. Obviously, electrical performance as a function of deformation will therefore be an issue in the design.

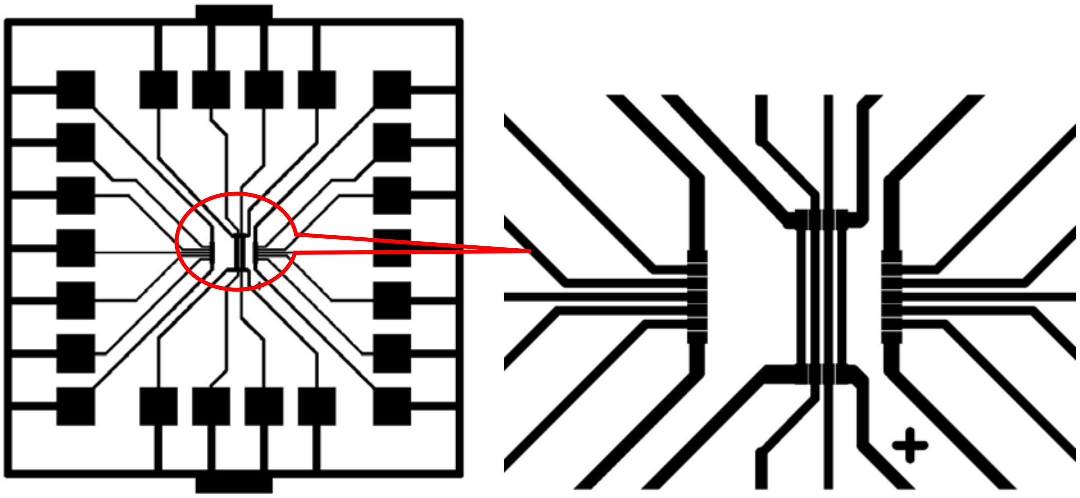
6.2 MATERIALS AND ASSEMBLY

In this work, an operational amplifier (op amp) IC was used to study the effect of mechanical bending on electrical performance. Operational amplifiers are one of the most useful electronic devices and are widely used in analog electronic circuitry to amplify an input signal to the required level. The test op amp circuit used here was a 5-V SOI CMOS quad rail-to-rail input and output operational amplifier. It was a 2.63mm × 3.16mm with 22 I/O pads on a 265µm thick wafer. The top view of the IC and function and location of the I/O pads are presented in Figure 6.1. The IC was designed at the University of Tennessee. To simplify the electrical bending testing, the four input bias currents (pads 19, 20, 21 and 22) were directly connected to the current reference generator (pads 1, 2, 3 and 4). In the corresponding substrate design, these four pairs of current input and output pads were each shorted with copper traces. The LCP substrate design patterns are shown in Figure 6.2.


1
2
3
4
UT
JPL
ASSOS
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22

1	I_{OUT1}	7	V_{IN3-}	13	V_{IN4+}	19	I_{BIAS1}
2	I_{OUT2}	8	V_{IN2-}	14	V_{IN1+}	20	I_{BIAS2}
3	I_{OUT3}	9	V_{IN3+}	15	V_{IN4-}	21	I_{BIAS3}
4	I_{OUT4}	10	V_{IN2+}	16	V_{IN1-}	22	I_{BIAS4}
5	V_{OUT3}	11	*VSS*	17	V_{OUT4}		
6	V_{OUT2}	12	*VEE*	18	V_{OUT1}		

Figure 6.1 The Top View of the Test Op Amp and Pad Location



(a) Bottom Circuit Pattern (b) Close-up of Bonding Pads

(c) Top Via Pattern

Figure 6.2 LCP Substrate Patterns for Test Op Amp

The test op amp die thinning and preparation, the LCP substrate fabrication, and the integration of the corresponding embedded assembly were performed using the same procedures described in previous chapters, except for the thermal compression bonding force. Compared to the PB8 die (5mm × 5mm with 88 bumps), the op amp die is relatively small (2.63mm × 3.16mm with 22 bumps), so the bonding force was proportionally reduced from 5000 g-f to 1000 g-f.

6.3 INVESTIGATION OF THE EFFECT OF MECHANICAL BENDING ON THE ELECTRICAL PERFORMANCE OF THE OP AMP ASSEMBLY

Before testing, long wires were soldered to the nickel/gold plated I/O pads of the test assemblies for convenient measurement, as shown in Figure 6.3. The wired part was constrained against a surface by taping four edges on the surface. For bending tests, metal pipes replaced the flat surface where the curvature of the test part was determined by each pipe's outer diameter. Pipes that were 3 and 6 inch in diameter were used in the experiment. Several important op amp parameters tested in this work included small-signal voltage gain (A_v), input offset voltage (V_{os}), common-mode voltage gain (A_{cm}), common-mode rejection ratio (CMRR) and gain bandwidth product (GB). Each of these parameters and test circuits are described below.

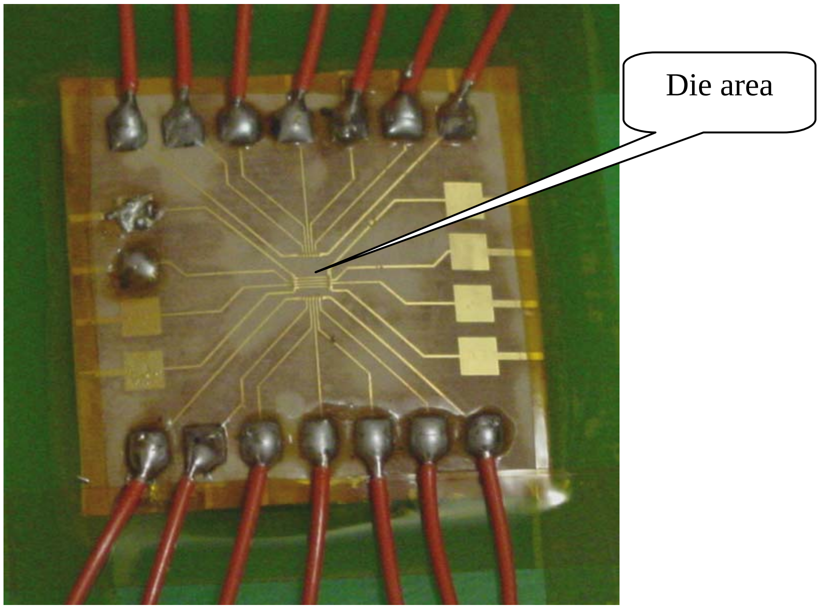


Figure 6.3 Wiring the Embedded Op Amp in LCP for Testing

(a) Input offset voltage

The input offset voltage is defined as the input voltage to the op amp when the output voltage is zero. Ideally, V_{out} will be zero when V_{in} is zero. In practice, however, this is not the case due to mismatches in the circuit. The input offset voltage was measured using a direct current (DC) voltage source connected to the positive input terminal ($V_{in}+$), as shown in Figure 6.4. The negative input terminal ($V_{in}-$) was connected to the output terminal (V_{out}), forming a closed loop with a unity gain. When V_{in} was swept from -5 to 5V, a similar magnitude voltage will be presented at the output, yielding a linear plot in the transfer characteristic, as shown in Figure 6.5. The value of V_{in} at the intercept of the plot and the x-axis is the input offset voltage (V_{os}).

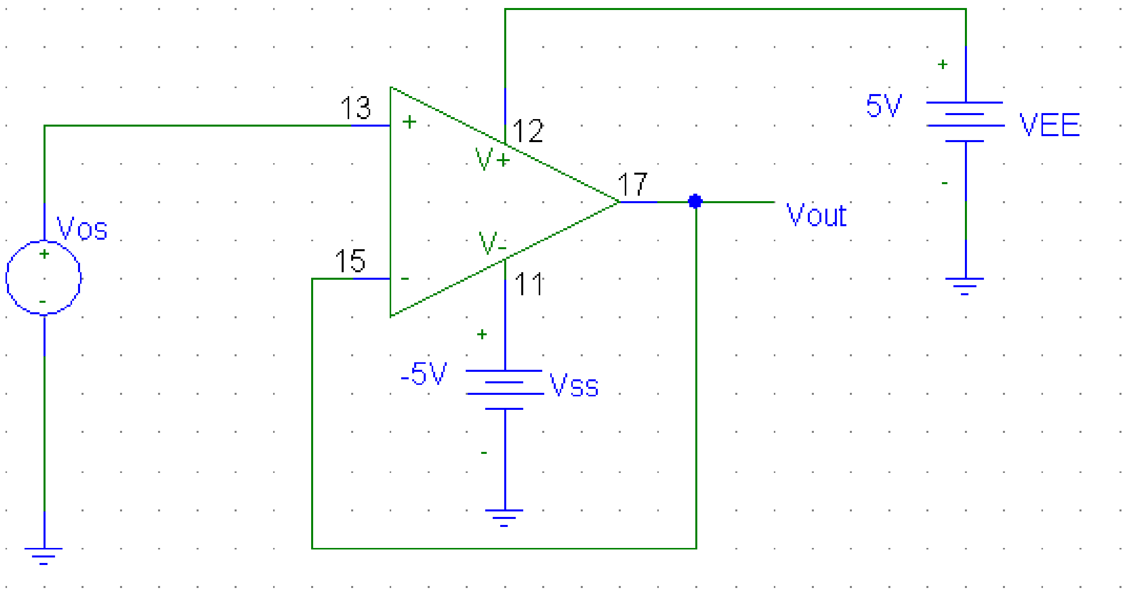


Figure 6.4 Closed-Loop Testing Schematic for Measuring Input Offset Voltage

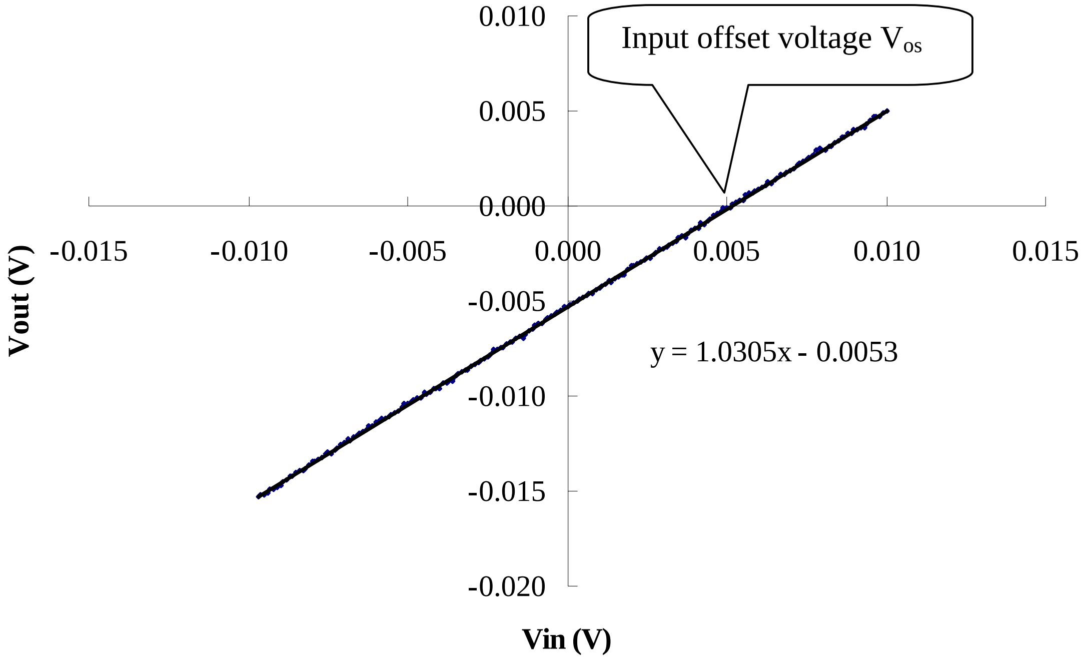


Figure 6.5 Finding the Input Offset Voltage on the Unity Gain Plot

(b) Common-mode input voltage gain

As stated previously, the output voltage should not change when the inputs are the same in ideal operational amplifiers. However, this is not true in real operational amplifiers, where a signal that is common to both inputs may also be amplified. The ratio of V_{out} to the common mode input V_{cm} is called the common-mode input voltage gain.

$$Acm = \frac{|Vout|}{|Vcm|}$$

In Figure 6.6, the shorted inputs are directly connected to a DC voltage source. The results are shown in Figure 6.7. The slope of the transfer characteristic plot corresponds to the common-mode voltage gain of the op amp.

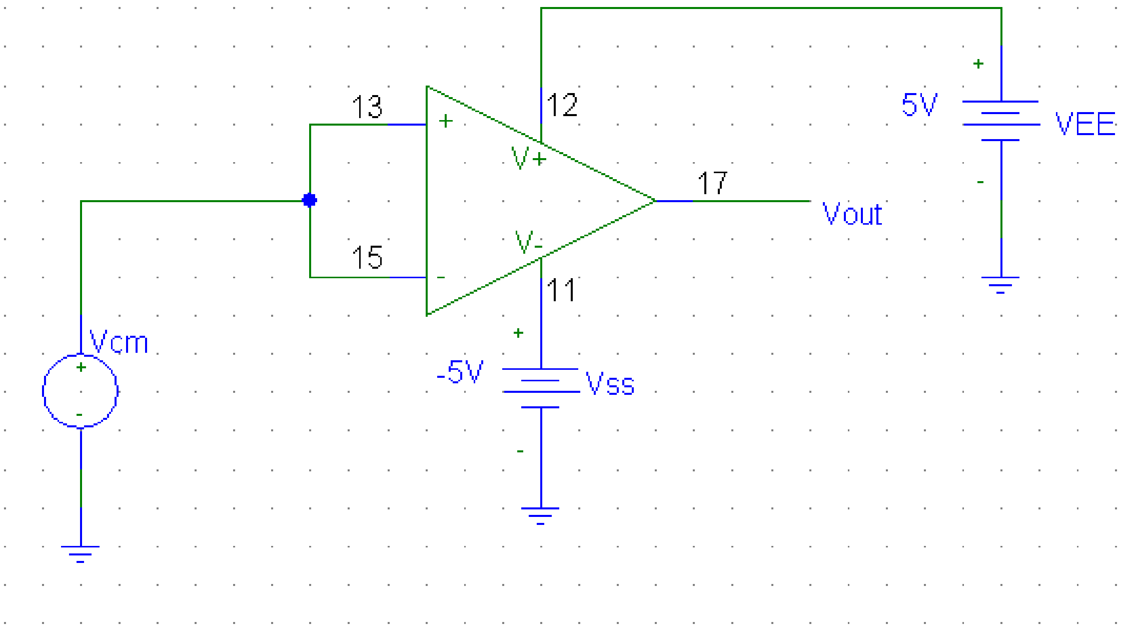

13
12
+
V+
5V
VEE
+
-
17
Vout
15
V-
-
11
Vcm
+
-
+
-5V
Vss
-

Figure 6.6 Testing Schematic for Measuring Common-Mode Voltage Gain

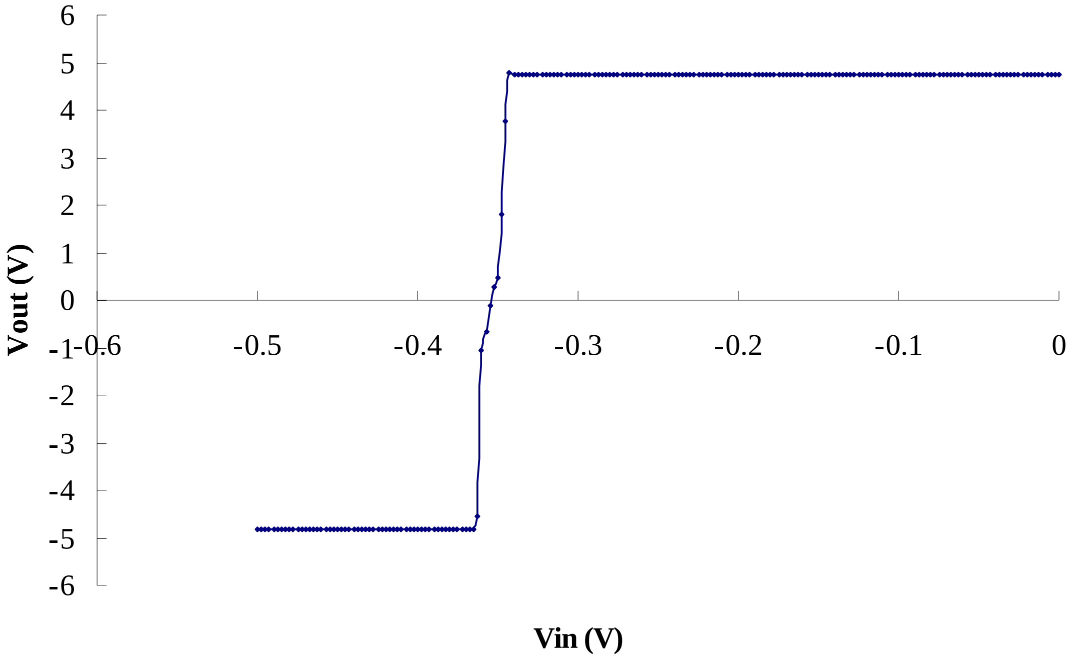


Figure 6.7 Transfer Characteristics of Op Amp with Common-Mode Input Voltages

(c) Differential-mode input voltage gain

When the two input voltages are equal in magnitude but with opposite polarity, the voltage gain is defined as the different-mode input voltage gain (A_{dm}), which may also be considered as the voltage gain when the common-mode input voltage gain is equal to zero. In this work, it also represents the small-signal voltage gain A_v. As shown in the testing schematic below, the two inputs are connected to two DC voltage sources that have the same voltage but with opposite polarity (Figure 6.8). The test results are shown in Figure 6.9. The slope of the transfer characteristic curve corresponds to the differential mode voltage gain. The measurement instrument (Agilent 4155C Semiconductor Parameter Analyzer) provided a minimal sweep step of 100 µV, so that the precision of the differential-mode input voltage gain (A_{dm}) was affected by this limit.

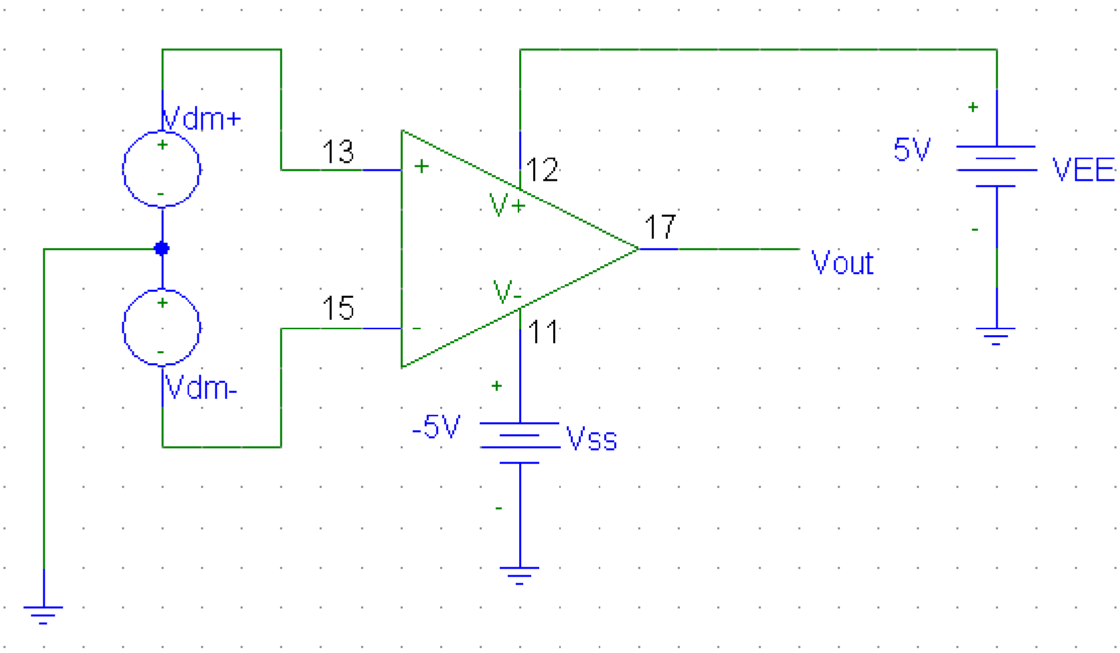


Figure 6.8 Testing Schematic for Measuring Differential-Mode Voltage Gain

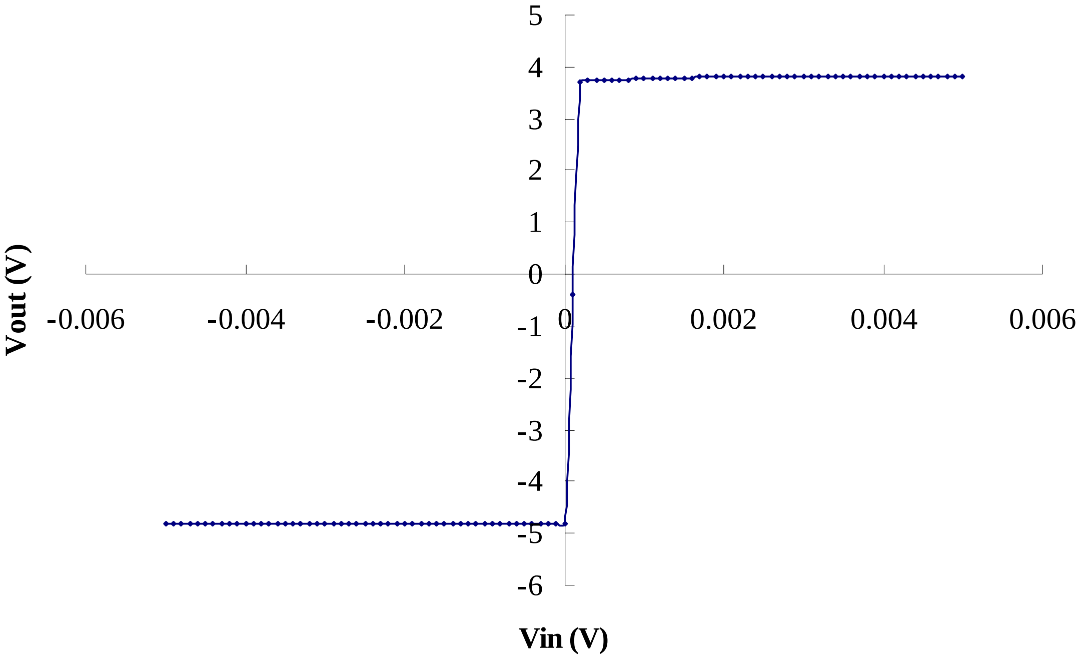


Figure 6.9 Transfer Characteristics of Op Amp with Differential-Mode Voltage Inputs

(d) Common-mode rejection ratio

The common-mode rejection ratio is the ability of the operational amplifier to reject a coupled noise (common signal) to both inputs. It is given by

$$CMRR = 20 \times \log\left(\frac{A_{dm}}{A_{cm}}\right)$$

(e) Gain bandwidth product

The gain bandwidth product is defined as the frequency for which $A_v = 1$ or $20\times\log|A_v| = 0$. It is commonly specified in dB. The testing schematic is shown in Figure 6.10. The inputs of the amplifier are connected to a signal generator producing a sinusoidal voltage, while the output voltage is connected to an oscilloscope. Initially, the frequency and the amplitude of waveform are kept small. The frequency is then slowly incremented until the amplitude of the output waveform drops to 0.707 of the amplitude of the input waveform. At this point, the frequency is considered to be the unity gain frequency f_T, or gain bandwidth product (GB)

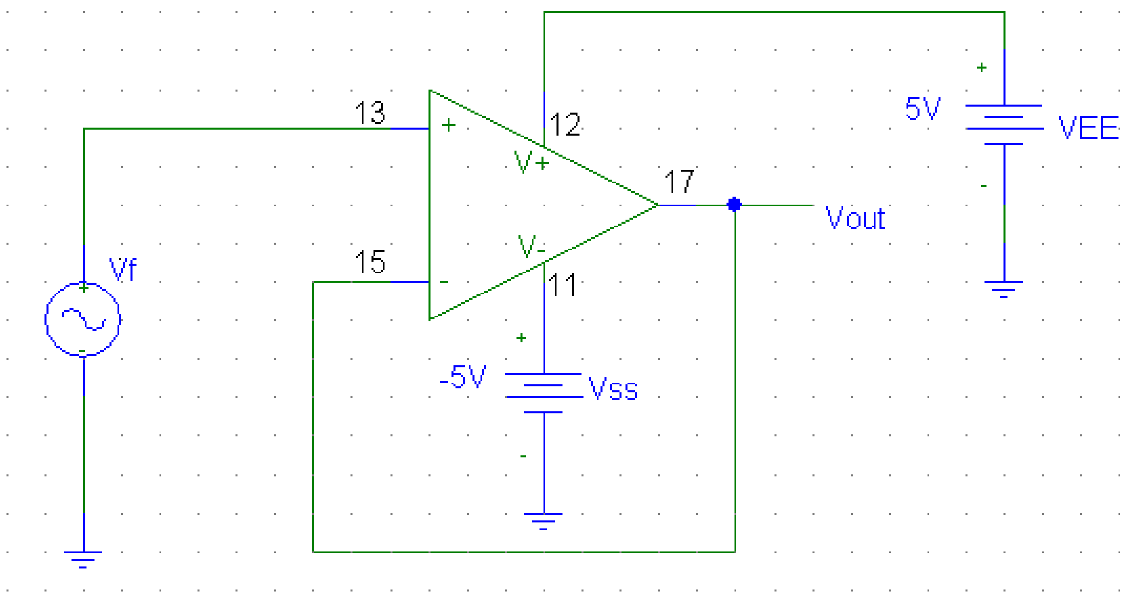


Figure 6.10 Testing Diagram for Measuring Gain Bandwidth Product

In all the electrical tests conducted for this research, DC power supplies were used to provide -5 and +5V voltages to the VSS and VEE, respectively. The experimental results are listed in Table 6-1. The changes in the small signal voltage gain, CMRR and gain bandwidth products are insignificant for the different bending curvatures, compared to the input offset voltage. The variations of input offset voltages falls into the reasonable range (less than 10 mV [48]). These data indicate that the flexible embedded op amp assembly provided stable DC/AC electrical performances even when subjected to significant amount of mechanical bending.

Table 6-1 DC/AC Electrical Performance of Embedded Op Amp in LCP Assembly

	Parameters	Conditions	Curvatures		
			flat	6” diameter	3” diameter
V_{OS}	Input Offset Voltage	$0<V_{in+}<5V$	5.14 mV	2.49 mV	0.02 mV
A_v or A_{dm}	Small signal Voltage Gain or differentifal mode voltage gain	$0<V_{dm+}<5$, $-5<V_{dm-}<0$	92.6 dB	93.5 dB	93.5 dB
A_{cm}	Common-mode voltage gain	$0<V_{cm}<5$	46.5 dB	52.6 dB	51.7 dB
CMRR	Common-mode rejection ratio		46.01 dB	40.9 dB	41.8 dB
GB	Gain Bandwidth Product		21.32 MHz	20.56 MHz	21.32 MHz

6.4 SUMMARY

A 5-V SOI CMOS quad rail-to-rail input and output operational amplifier was introduced to evaluate the effect of mechanical bending on the DC/AC electrical performance of this embedded thin op amp assembly. The experimental results indicated that the flexible op amp assembly had stable DC/AC electrical performance even when subjected to relatively high levels of bending.

CHAPTER 7 CONCLUSIONS

These studies on the integration of thin flip chip in liquid crystal polymer (LCP) based flex were performed as part of an ongoing joint research collaboration between Auburn University and the Jet Propulsion Laboratory to examine the feasibility of these thin flexible assemblies. A process sequence was established for the assembly using 50μm thick PB8 test dies with an LCP substrate. This dissertation has described studies covering three separate process phases - thin die preparation, liquid crystal polymer substrate fabrication, and the final assembly and sealing.

Partial dicing before the thinning process was ultimately selected in order to produce thin dies with a high yield and high quality. This process significantly shortened the exposure time of the die edge to adverse grinding impacts in the grinding operation compared to the individual die thinning process employed in the earlier investigations. Thin die transfer using a thick flat handling chip effectively solved the problems due to die handling and die planarity, substantially lowering the overall difficulty of the assembly process.

The backside assembly design decreased the overall height of the assembly by eliminating the die-to-substrate gap compared to a topside assembly design. The corresponding LCP substrates were fabricated using three steps: bottom circuitry formation, via etching and copper surface finishing.

Thermal compression bonding was employed for the formation of the gold-to-gold interconnections. Direct silicon/LCP lamination was used based on the LCP thermoplasticity, eliminating the need for underfill and thus decreasing the assembly height and eliminating the loss of flexibility due to a rigid underfill. The most influential parametric effects were identified using the results from a design of experiment approach in order to optimize the assembly process.

As a result of these integration studies, a thin flip chip in LCP flex was successfully assembled with good electrical continuity. The new process route was verified as a feasible way to build this kind of thin flexible assembly with embedded thin ICs.

Due to the flexibility of the thin flip chip in LCP, the effect of mechanical bending on the electrical performance of the assembly was a concern. A SOI CMOS quad rail-to-rail input and output operational amplifier was therefore introduced into this study by building a thin assembly with an embedded op amp. Its electrical performance was tested in the presence of mechanical bending. The experimental results obtained indicated that there were insignificant changes in the small signal voltage gain, CMRR and gain bandwidth products. The input offset voltages varied within a reasonable range. This study therefore confirmed that this thin op amp in LCP flex was able to maintain a stable DC/AC electrical performance even under the influence of a substantial deformation.

CHAPTER 8 FUTURE WORK

The thermal reliability testing is ongoing at JPL for both thin flip chip in LCP assemblies. The failed parts have to be analyzed to identify the failure mode and the corresponding modeling needs to be developed to understand the failure mechanism. This kind of modeling should be able to predict the thermal fatigue life of these kinds of structures with different thickness ICs. Furthermore, modeling needs to be developed to estimate the effect of mechanical bending on the electrical performance, particularly significant to the design of this kind of the thin flexible assembly with embedded IC.

Although the attempt failed in early investigations, the post thinning process is still very attractive due to its simplicity. This process started with the thick die attachment, avoiding the handling and planarity problems related to thin die. The failure was caused by the non-uniform deep silicon RIE. The application of photoresist around the die effectively prevented the lateral etching on the die sidewall. However, the silicon fence was formed around the thinned die during the course of the RIE process. The effect of the photoresist protective layer on the formation of silicon fence is still not understood. An extended study would be of interest to identify the mechanism of the formation of the silicon fence. The parameters for plasma etching can be employed for this study, including fluxes of etching gases, power supply to generate and maintain plasma, etching temperature, and time ratio of etch cycle to passivation cycle. Modeling of the plasma etching process including the effect of gas flow should also be pursued.

Damage and defects were observed on the surface of the plasma thinned die, caused by the plasma bombardment. The damage and defects may affect the sequential processes and testing, such as the lamination with LCP coverlayer by thermal compression bonding, and the quality of final structure. This effect will need to be evaluated. Isotropic silicon RIE process may be introduced to mill the die surface for eliminating the damages and defects.

Future work also could focus on the simplification and optimization of the process. Pre-stud bumping may enhance the bumping efficiency with gold bumps applied in the wafer stage prior to thinning, compared to individual die bumping after thinning and die transfer. Pre-bumping can also improve the bonding quality, as the bumping can be executed at a high stage temperature and thus avoid the silicon cracking that is present with thin die bumping. However, the problems caused by the presence of bumps will have to be considered in bumped wafer thinning.

Entrapped voids in the coverlayer LCP in the final structure were a cause of concern. The effect of voids in the coverlayer on the performance of the assembly therefore needs to be evaluated. Vacuum lamination may provide one solution to this problem and should be pursued.

REFERENCES

1. Harper C. A., Electronic Packaging and Interconnection Handbook (third edition), McGraw-Hill, New York, 2000, p7.1-7.3.

2. Savastiouk, S., Siniaguine, O. and Diorio M., The Next Dimension, Advanced Packaging, v7, n7, September/October 1998, p55-61.

3. New, D., Silicon Thinning and Stacked Packages, 27th Annual IEEE/SEMI International Electronics Manufacturing Technology Symposium (IEMT), 2002, 17-18 July 2002, p50-52.

4. Halahan, P. Marcoux, P., Kretz, F. and Schraub, T., Backgrinding for Thin Wafer Production, Chip Scale Review, January/February 2002.

5. Reiche, M., and Wagner, G., Wafer Thinning: Techniques for Ultra-Thin Wafers, Advanced Packaging, v12, n3, March 2003, p29-33

6. Alpsite website: www.crystec.com/alpovere.htm.

7. Savatiouk, G., Atmospheric Downstream Plasma-An Approach to 300-Mm Wafer Thinning, Semi Global 300mm Report, July 1998.

8. Source from website: www.nexxsystems.com/flipchip+apps.htm.

9. Hammer, R. B., Powell, D. O., Mukherjee, S., Tummala, R. and Raj, R. Chapter 10 Ceramics in Electronic Packaging in the book Principles of Electronic Packaging edited by Seraphim, D. P., Lasky, R. and Li, C.Y., McGraw-Hill, New York, 1989, p283.

10. Yeung, B. H., Hause, V., and Lee, T-Y., Assessment of Backside Process through Die Strength Evaluation, IEEE Transaction on Advanced Packaging, vol. 23, no.3, August 2003, p582-587.

11. The Loctite Design Guide for Bonding Plastic, Volume 2, p30, 40, and 52.

12. DuPont Teijin Films website: www.dupontteijinfilms.com

13. Harris, F. W., Synthesis of Aromatic Polyimides from Dianhydrides and Diamines, Chapter 1 of Polyimides, edited by Wilson, D., Stenzenberger, H. D. and Hergenrother, P. M., Blackie & Son, Glasgow, United Kingdom 1990.

14. Allcock, H. R. and Lampe, F. W., Contemporary Polymer Chemistry (2^{nd} edition), Prentice Hall, New Jersey 1990, p35.

15. Sroog, C. E., Films, Mouldings and Other Applications, Chapter 9 of Polyimides edited by Wilson, D., Stenzenberger, H. D. and Hergenrother, P. M., Blackie & Son, Glasgow, United Kingdom 1990.

16. Jawitz, M. W., Printed Circuit Board Materials Handbook, McGraw-Hill, New York, 1997, p3.9

17. Du Pont Product Literature, www.dupont/products/kapton/.

18. Griffin, A. C., Vaidya, S. R. and Steele, M. L., Liquid Crystalline Polymers: Phenomenological and Synthetic Aspects, collected in the book of Polymeric Liquid Crystals, edited by Blumstein, A., Plenum Press, New York, NY, 1985, p1-20.

19. Yang, R. and Hayden, T. F., Recent Advancements in Flex Circuit Technology Using Liquid Crystal Polymer Substrates, Chapter 11 of Foldable Flex and Thinned Silicon Multichip Packaging Technology, edited by Balde, J. W., Kluwer Academic Publishers, Boston, 2003, p257-288.

20. Lin, Y.G., and Winter, H.H., High-Temperature Recrystallization and Rheology of A Thermotropic Liquid Crystalline Polymer, Macromolecules v24, 1991, p2877-2882

21. Neubert, M., plc.cwru.edu/tutorial/enhanced/files/textbook.htm

22. Jackson, W. J. and Kuhfuss, H. F., J. Polymer Science: Polymer Chemistry Edition, v.14, 1976, p2043

23. Hoechst Celanese Product Literature, Document Number: TVC4A/5M/1988.

24. B. Farrell, K. Jayaraj and L. Felton, “Low Cost, Multichip Modules Based on Liquid Crystal Polymers,” 16th Digital Avionics Systems Conference, 1997, Irvine, California.

25. Khoo, C.G.L., Brox, B., Norrhede, R. and Maurer, F.H.J., Effect of Copper Lamination on the Rheological and Copper Adhesion Properties of A Thermotropic Liquid Crystalline Polymer Used in PCB Applications, IEEE Transaction on Components, Packaging, and Manufacturing Technology-Part C, v20, n3 July 1997, p219-226

26. Rogers Corporation Advanced Circuit Materials Data Sheet.

27. Picture from www.matech.com

28. Zhang, T., Hou, Z., Johnson, R.W., Moussessian, A., Castillo, L. D. and Banda, C., Flip Chip Assembly of Thinned Silicon Die on Flex Substrates, IPC/APEX/ECWC, 22-24 Feb 2005, Anaheim, CA.

29. Banda, C., Mountain, D. J., Charles, H. K., Lehtonen, J. S., Keeney, A. C., Johnson, R.W., Zhang, T. and Hou, Z., Development of Ultra-Thin Flip Chip Assemblies for Low Profile SiP Applications, IMAPS International 2004, November 14-18, 2004, Long Beach CA

30. Zhang, J. Skiner, J., Szczech, J., and Gamota, D., Ultra-Thin Flip Chip on Board Assembly, 2000 SMTA International Conference Proceedings.

31. Chen, R. and Baldwin, D.F., Smart Tooling for Assembly of Thin Flexible Systems, IEEE Transactions on Electronics Packaging Manufacturing, v22, n4, Oct 1999, p1181-1189

32. Baldwin, D.F., Next-Generation Flip Chip Materials and Processing, Chapter 17 of Area Array Packging Handbook edited by Gilleo, K., MaGraw-Hill, New York,2002.

33. Kallmayer, C., Jung, E., Kasulke, P., Azadeh, R., Azdasht, G., Zakel, E. and Reichl, H., A New Approach to Chip Size Package Using Meniscus Soldering and FPC-Bonding, 1997 Proceedings of 47th Electronic Components and Technology Conference, 18-21 May 1997, p114-119

34. Pictures from website: http://mst.tu-berlin.de/becap/research/topics/flex/flex.htm.

35. Prasad, R.P., Surface Mount Technology Principles and Practic (2nd edition), Kluwer Academic Publishers, Boston, 1997, p747

36. Adler, C., Klink, G., Feil, M., Ansorge, F. and Reichl, H., Assembly of Ultra Thin and Flexible ICs, 2000 Proceedings of 4th International Conference on Adhesive Joining and Coating Technology in Electronics Manufacturing, 18-21 June 2000, p20-23

37. Pictures from http://www.polytronik.fhg.de/inhalt/06materialien/praesentationen/Rolle-zu-Rolle_IZM_Muenchen.pdf

38. Ulaby, F.T., Fundamentals of Applied Electromagnetics (1999 edition), Prentice-Hall, New Jersey, p341

39. Source: www.emsstg.com/mont/anennas.asp

40. Jordan, J. Gold Stud Bump in Flip-Chip Applications, published in the website of Palomar Technologies, Inc. (www.palomar.com).

41. Yang, R., Liquid Crystal Polymer for Flexible Circuits, Advanced Packaging, v11, n13, March 2002, p17-22.

42. Bogatin, B., Liquid Crystal Polymers and Packaging, Semiconductor International, 2002.

43. Zhou, G., Gronqvist, H., Starski, J. P. and Liu, J., Characterization of Liquid Crystal Polymer for High Frequency System-in-a-Package Applications, IEEE Transactions on Advanced Packaging, Vol. 25, No. 4, November 2002, p503-508.

44. Farrell, B. and StLawrence, M., The Process of Liquid Crystal Polymer Printed Circuits, Proceedings-Electronic Components and Technology Conference, 2002, p667-671.

45. Nevreker, P., Liquid Crystal Polymer: The Next Generation of High Performance Flex Circuit Materials, CircuiTree, April, 2002.

46. Kloeck, B., and Rooij, N.F., Mechanical Sensors, Chapter 4 of Semiconductor Sensors edited by Sze, S. M., John Wiley & Sons, New York, 1994, p160-16

47. Wymyslowski, A., Santo-Zamik, M., Friedel, K. and Belavic, D., Numerical Simulation and Experimental Verification of The Piezoresistivity Phenomenon of the Printed Thick Film Piezoresistors, 2004 Proceedings of the 5th International Conference on Thermal and Mechanical Simulation and Experiments in Microelectronics and Microsystems, 2004, p359-366.

48. Jaeger, R. C., Microelectronic Circuit Design, Irwin/McGraw-Hill, Boston 1997, p516.