Modulation and Control of Energy Feedback Voltage Source Inverter and Matrix Converter

by

Chengzhu Piao

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Approved by

John Y. Hung, Chair, Professor of Electrical and Computer Engineering
S. Mark Halpin, Professor of Electrical and Computer Engineering
Robert N. Dean, Associate Professor of Electrical and Computer Engineering
R. Mark Nelms, Professor of Electrical and Computer Engineering

Abstract

In this research work, the modulation and control of energy feedback voltage source inverters and matrix converters are investigated. This paper analyzes the basic principle of the space vector pulse width modulation (SVPWM), and proposes a unified and simplified modulation algorithm as a pulse width modulation method for voltage source inverters and matrix converters. Using the proposed unified model of modulation, several additional contributions are developed for voltage source inverters and matrix converters.

Carrier-based discontinuous space vector pulse width modulation (DSVPWM) method for voltage source inverters and matrix converters are proposed. Based on the relationship between SVPWM and carrier based modulation, a simplified DSVPWM method for three-phase inverters and matrix converters is introduced by skillfully arranging two zero voltage vectors. In this method, the conventional space vector modulator with equal division of zero voltage vector time is modified to generate different discontinuous modulating waves.

A simple SVPWM scheme for operating three-phase voltage source inverters at higher modulation indexes, including overmodulation region, is proposed. Based on the study of existing overmodulation techniques published in literatures, two two-mode and two single-mode strategies based on simplified SVPWM overmodulation algorithms are proposed which can manage smooth transition from the linear control range to six-step operation.

An analysis and uniform compensation of dead-time effect in three-phase multi-level diode clamped voltage source inverters and matrix converters are proposed. This paper analyzes dead-time effects and proposes an approximate solution based on characteristics of simplified SVPWM. The approximation is a result of avoiding the need to determine output current direction. The value of dead time is adjusted online by the magnitude of

corresponding phase current. The deviation of voltage vectors caused by dead time effect is directly compensated to three phase reference voltages.

A simplified control strategy to balance dc-link capacitor voltage for multi-level diode clamped voltage source inverters based on DSVPWM is proposed. On the basis of a simplified SVPWM algorithm for multi-level inverter and discontinuous modulation, simplified DSVPWM methods are proposed here to balance the dc-link capacitor voltages. The proposed control method changes the path and duration time of the neutral point currents, making the voltages of series connected dc-link capacitors equal.

A simplified control scheme is proposed for three-phase voltage source inverters and matrix converters under unbalanced three-phase voltage conditions. On the basis of simplified SVPWM and carrier-based modulation, the concept of voltage modulation by using offset voltage is applied to an unbalanced three-phase grid voltage control method. The control objective is to balance three phase output currents and minimize total harmonic distortion of the output currents without ac current sensors under unbalanced grid voltage conditions.

An energy-feedback control scheme of voltage source inverters and matrix converters based on phase and amplitude control and simplified modulation method is proposed, achieves a unity power factor of feedback current and precise control of feedback current. To calculate phase angle σ and ratio of modulation M, two kinds of determination of feedback current are proposed.

Both direct and indirect matrix converters are considered. Computer simulations are used to study feasibility of all algorithms.

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Chapter 1

Introduction

This chapter is the introduction of the dissertation. This chapter introduces backgrounds of voltage source inverters, matrix converters, and pulse width modulation methods. The voltage source inverters and matrix converters are important to the dc-ac conversion and ac-ac conversion. Pulse width modulation methods, especially SVPWM are the most popular methods applied to voltage source inverters and matrix converters. In this chapter, the first section is dc-ac conversion, the second section is ac-ac conversion, the third section is pulse width modulation methods, the fourth section is contribution of dissertation, and the fifth section is dissertation framework.

1.1 The dc-ac conversion

With the development of the world economy, energy conservation and development utilization of environmental protection sustainable new energy become new problem. Variable frequency power supply energy feedback control has also been studied in these years. The rapid development of power electronics and frequency control create the conditions for the studies presented here.

Power electronics have transformed traditional industries, and play an important role in the promotion of establishment of automated industrial system. Power electronics applications are embodied in the form of energy conversion whether in the motor speed drives or in the power system for generation, transmission, and distribution. These transformations include dc-dc, dc-ac, ac-ac, and ac-dc. In contrast to rectifier circuits (ac-dc), dc-ac conversion circuit referred to the inverter circuit, it achieves dc-ac power transformation.

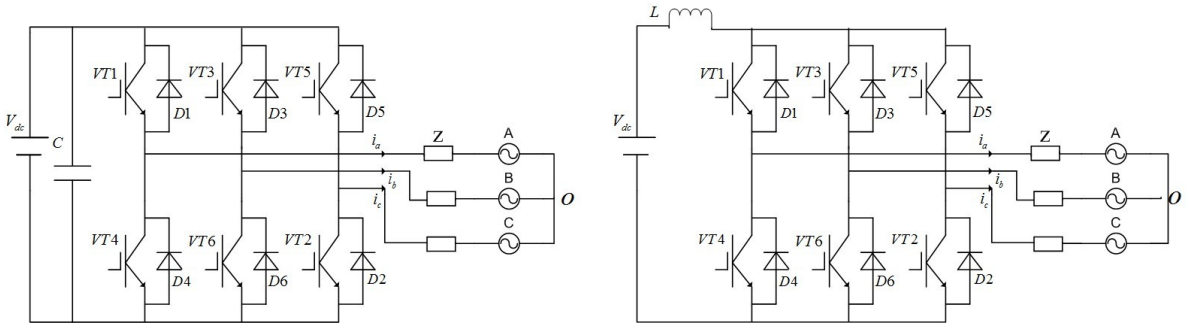
On the research of speed control, people further explore the potential of frequency control systems to improve efficiency and energy savings. One approach is that frequency conversion technology and optimum control provide energy according to demand. Minimize the input energy when the device meets the requirement of torque, speed, and dynamic response. Another approach is that the electrical energy from potential energy or kinetic energy recycled to the power grid. Through voltage source inverter (VSI) device, the method could feedback renewable energy to the ac grid. It not only has the advantage of precise motor brake, but also save energy and improves the dynamic performance of the motor. Therefore, the energy feedback system has great theoretical and practical significance [1].

Energy feedback VSI can transform energy from renewable energy or other energy source to power grid.

1) Distributed generation Distributed generation technologies can convert various forms of so-called "green" renewable energy into electrical form. Then, storage energy or direct deliver energy to the grid by using energy feedback system. Since these power generation facilities are not large, we can distribute energy in the vicinity of power load. In recent years, people made a lot of breakthrough study of new distributed generation technologies. Distributed generation is expected to occupy an increasing proportion of energy production, and have a significant impact to power systems. These new distributed generation technologies are micro-turbine, fuel cells, solar energy, and wind power technology [2].

Renewable energy such as photovoltaic, wind energy, and fuel cells are used to generate electricity and constitute distributed generation. An inverter is used to control energy flow between renewable generator and power grid, as Figure 1.1 shows. Inverter types include VSI and current source inverter (CSI). In this dissertation, the main research is focused on VSI because it is the type most commonly used.

The renewable energy flows to power grid through energy feedback VSI. By controlling VSI properly, the unity power factor is obtained.



(a) VSI (b) CSI

Figure 1.1: The topology of inverter

2) Regenerative type of power load A variety of power supply manufacturers perform reliability tests, and experimentally determine output power characteristics before manufacturing products. Traditional method is that energy is discharged using resistance, resulting in waste of energy. Energy feedback type of power simulation load has a good solution to this problem. It is a power electronics technology, computer control technology, and power system automation technology which can be designed and implemented for a variety of ac and dc power evaluation experiments.

3) Motor brake energy feedback With the development of electric drive and control technology, frequency control more and more widely used in all areas of society, and have a good solution to the problem of ac motor speed control. In recent years, the rapid development and wide application of ac frequency conversion technology have yielded good solutions for ac motor speed control [3] [4]. Commonly used general purpose converters are usually ac-dc-ac converter topology, as Figure 1.2 shows. The converter uses power electronic devices to transform grid frequency, voltage, and current to these of the user desired frequency, voltage, and current. Motor load is changed to achieve automatic, smooth acceleration or deceleration. The characteristics of adjust speed basically maintained the characteristics of the asynchronous motor, hence its high efficiency, wide range, and high precision is an ideal motor speed control method.

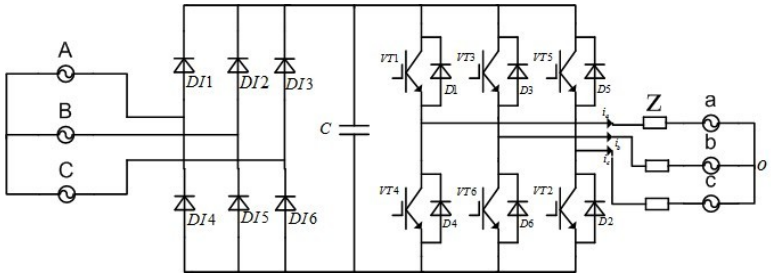


Figure 1.2: The topology of ac-dc-ac inverter

In this topology, three-phase power is converted into pulsating direct current through an uncontrolled rectifier bridge consisting of six diodes, and then filtered via electrolytic capacitors link, and finally delivered ac power to the load. This converter can only run in the first and third quadrants, cannot be directly used for a speed control system that demands quick start, braking and frequent reversals. Examples of such systems include high-speed elevators in mines, hoists, rolling mills, large planers, machine tool spindle drive systems, and tension system in winding institutions. These systems require bidirectional operation of the motor. Under conditions of motor braking, deceleration, or with potential energy load decentralization, the motor is in the renewable power generation state. Due to the diode rectifier is not reversible, regenerative energy can only be accumulated on the dc side of the filter capacitor, resulting in pumping voltage, and in severe cases damage to the dc-link.

To satisfy motor braking requirements, there are many methods to deal with the "pump energy", basically divided into two categories: (1) Heat or dissipation forms of consumption; (2) Use energy feedback circuit technology feedback to the ac power grid or other energy storage. The former type of method is relatively simple, but such methods not only waste energy but also only can brake for short time periods due to the limits of design temperature rise. Temperature rise is also unfavorable to overall system reliability. The latter type of method increases the energy utilization and improves energy conservation, but the structure is more complex. Especially for frequent starting, braking, or long-term use with potential

energy load systems such as elevators, energy feedback to the grid has a significant energy-saving effect. The energy feedback system can effectively solve pumping energy problems. Energy feedback system not only obtains a fast dynamic response but also feeds braking energy back to the grid, making the converter truly have bidirectional operation and reduced energy consumption [5]. With the development of the inverter, there have been many types of inverter, but mainstream inverter basically has the basic structure shown in Figure 1.3.

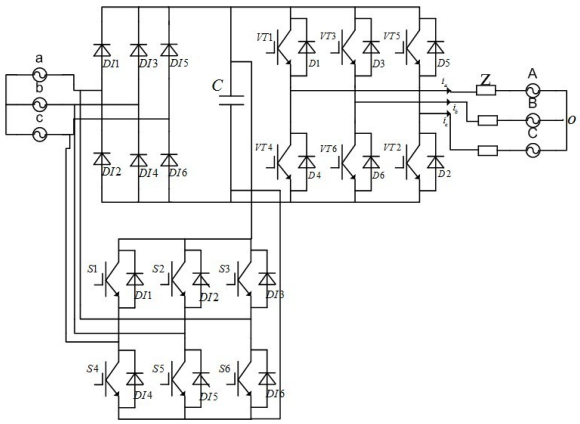


Figure 1.3: The modified topology of ac-dc-ac inverter

Due to the dc-link storage element, there is the advantage that both converter stages are large extent decoupled for control purposes. Furthermore, a constant and independent input quantity exists for the PWM inverter stage, which results in high utilization of the converter's power capability. On the other hand, the dc-link energy storage element has a relatively large physical volume, and when electrolytic capacitors are used, there is a potentially reduced system lifetime [6]. In today's growing tension of energy resources, this research has a very important practical significance.

1.2 The ac-ac conversion

An ac-ac power converter is able to generate controllable sinusoidal ac outputs in terms of magnitude and frequency from an ac supply. Many parts of industrial application request

ac-ac power conversion. According to the different ways of converter, it can be divided into indirect ac-ac converter and direct ac-ac converter.

1) Indirect ac-ac converter The ac-dc-ac indirect converter is composed of three parts, which are rectifier (ac-dc), inverter (dc-ac), and intermediate dc-link (inductive or capacitive). The most common design for an indirect ac-ac converter is the use of uncontrolled diode bridge rectifier at the supply side, as shown in Figure 1.2. Rectifier diodes are turned off by ac voltage power supply, and inverter thyristors are turned off by load synchronous motor ac voltage. The output current amplitude is controlled by rectifier; and the output frequency is controlled by the inverter. The control of this converter is simple because of the naturally commutate characteristics of the diode bridge rectifier.

However, this converter cannot be used in applications requiring regenerative condition. In applications requiring regenerative condition, a modified ac-dc-ac indirect converter is used, as shown in Figure 1.3; or controlled IGBT devices are used to replace the diode bridge rectifier, as shown in Figure 1.4. The modified ac-dc-ac converter and back to back VSI offer advantages of improved input current waveforms, improved total input power factor, and bi-directional power flow. However, the overall control method is more complicated than the traditional converter. It also has some disadvantages like increase the losses, converter volume, and cost.

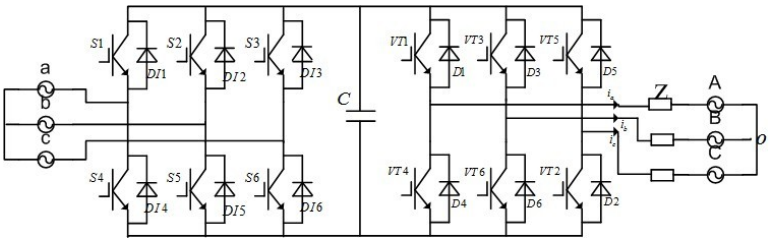


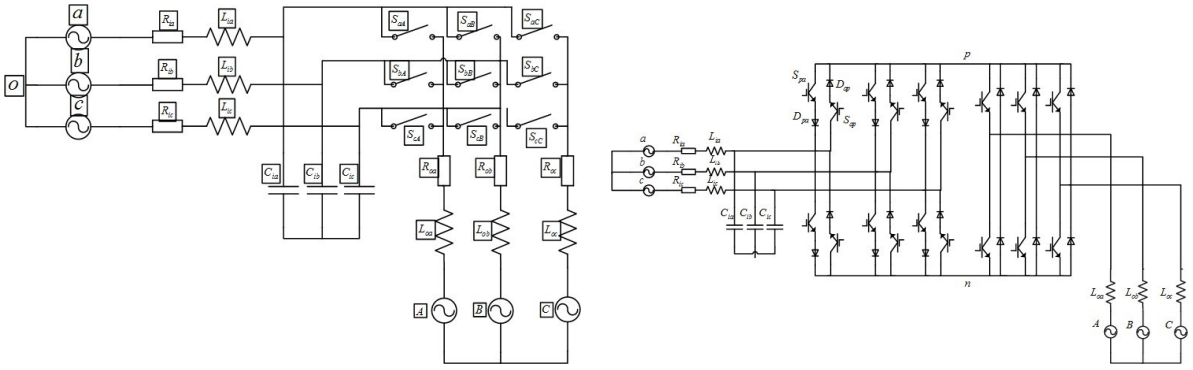
Figure 1.4: The topology of back-to-back VSI

2) Direct ac-ac converter The ac-ac direct frequency converter uses ac voltage of the power supply. By controlling power devices, it can obtain variable output frequency and

voltage. It consists of three sets of reversible rectifier (bridge or zero line, high power devices are used to bridge).

Due to the dc-link storage element, the dc-link energy storage element has a relatively large physical volume, and when electrolytic capacitors are used, in the case of a voltage dc-link, there is potentially a reduced system lifetime. With the goal of higher power density and reliability, recent studies consider matrix converter (MC) concepts that achieve three-phase ac-ac conversion without any intermediate energy storage element. Unlike the conventional frequency converter, the MC is frequency converter which does not contain a dc-link circuit. Thus, the MC may provide a solution for applications where large passive components are not allowed. A purely semiconductor-based solution provides an economically more efficient result than conventional frequency converter [7]. Recently, the MC has been considered for ac-ac applications because of its compactness in weight and size due to absence of a dc-link capacitor. In addition, the MC is capable of producing a variable output voltage, with unrestricted input and output frequency. These key features are obtained from the MC without using any large passive components [8]. Due to the significant advantages offered by MC, such as adjustable power factor, capability of regeneration, and high quality sinusoidal input/output waveforms, MC has been one of the ac-ac topologies that receive extensive research attention in the variable voltage and variable frequency ac drive applications.

With the goal of higher power density and reliability, it is hence obvious to consider mc that achieves three-phase ac-ac conversion without any intermediate energy storage element. MC can be divided into direct matrix converter (DMC) and indirect matrix converter (IMC), as Figure 1.6 shows. DMC carry out voltage and current conversion in one stage. Conversely, IMC separate stages to provide voltage and current conversion. MCs are frequently seen as a future concept for variable speed drives technology, but they have only achieved low industrial applications. The reason for this could be complex modulation algorithm and high topological variations.



(a) Direct matrix converter (b) Indirect matrix converter

Figure 1.5: The topology of MC

1.3 Pulse width modulation technology

With the development of power electronics and microprocessor technology, PWM technology has been studied extensively during the past decades and also widely used in the field of three phase inverters. PWM technology is the technology that modulates pulse width. PWM technology is through a series of pulse width modulation to obtain the desired waveform (including phase angle and amplitude).

Various PWM methods have been developed to achieve the following aims: wide linear modulation range, less switching losses, less total harmonic distortion (THD) in the spectrum of switching waveform, easy implementation, and less computation time. Sinusoidal pulse width modulation (SPWM) and space vector pulse width modulation (SVPWM) are the most popular modulation strategies applied to variable frequency and adjusting speed systems. So far, there has been a variety of PWM control technology, the most widely used algorithm is SPWM and SVPWM.

1.3.1 SPWM technology

SPWM due to its simple algorithm and clear physical concepts has been widely used in the inverter, but has low dc voltage utilization. SPWM method is one of the methods used more in common. The pulse width varies by sine law, and the area of output pulse voltage

is the same as the area of desired output sine wave at the corresponding sections. Through change the frequency and amplitude of modulation wave, we can adjust the frequency and amplitude of the output voltage. Implementation of SPWM methods are: natural sampling method, equal-area method, regular sampling method, and hardware modulation method. Among these methods, natural sampling method and equal-area method are used widely in practice. SPWM due to its simple algorithm and clear physical concepts has been widely used in the inverter, but has low dc voltage utilization. SPWM control is mainly focused on the output voltage is close to sinusoidal waveform.

1.3.2 SVPWM technology

SPWM control is mainly focused on the output voltage is close to sinusoidal waveform, is not take the output current waveform into account. However, the ultimate goal of ac motors require three-phase sinusoidal input current to form a circular rotating magnetic field in motor space, resulting in a constant electromagnetic torque. If alignment this goal, treat the inverter and the ac motor as a whole system, we can control inverter according to track circular rotating magnetic field, this technology is SVPWM method. In mid-1980s, scholars proposed a method based on space vector pulse width modulation. SVPWM has become one of the most popular and important PWM methods for three-phase converters. Compared with SPWM algorithm, SVPWM has a wide range of linear modulation, high utilization of dc voltage, low output harmonics, and easy digital implementation. The waveform of carrier triangular waveform and control signal of SVPWM algorithm is shown in Figure 1.6.

1.4 Dissertation contributions

The conventional SVPWM algorithm needs coordinate transformations, trigonometric calculations, sector number identification etc. The traditional SVPWM method for two-level inverter is not very difficult to implement. However, it becomes more and more complex and

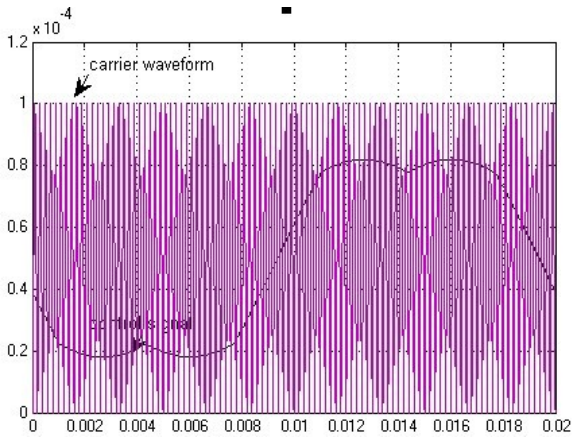


Figure 1.6: Carrier triangular waveform and control signal for SVPWM

difficult to realize as the level number of the inverter increases. To simplify modulation algorithm, according to the relationship between SVPWM and SPWM, the simplified SVPWM for multi-level voltage source inverters are proposed [9][10].

To obtain less switching losses and better harmonic characteristics based on the relationship between SVPWM and carrier based modulation, the discontinuous SVPWM strategies including six basic types of DSVPWM and eight novel types of DSVPWM are proposed and studied [11].

Generally, the overmodulation techniques for SVPWM inverter need to store lots of data in the controller beforehand, which produces a huge memory while the control resolution is not perfect. For operating a three-phase voltage source inverters at higher modulation indexes, including overmodulation region, two two-mode strategies and two single-mode strategies are proposed which can manage smooth transition from the linear control range to six-step operation [12].

The dead-time distorts the output waveform, however, and increases THD. Dead time compensation is necessary to minimize current distortion and reduce THD. This dissertation analyzes dead-time effects and proposes a approximate solution based on characteristics of simplified SVPWM. The approximation is a result of avoiding the need to determine output current direction [13].

Currents flowing into the neutral point of dc-link capacitors cause fluctuations of dc-link capacitor voltages in the diode-clamped inverter. Performance of the multi-level inverter system is affected by imbalances of the dc-link capacitor voltages. On the basis of a simplified SVPWM algorithm for multi-level inverter and discontinuous modulation, simplified DSVPWM methods are proposed here to balance the dc-link capacitor voltages. The proposed control method changes the path and duration time of the neutral point currents, making the voltages of series connected dc-link capacitors equal. While maintaining low switching losses and achieving effective voltage balancing, this method does not adopt any additional hardware or complicated calculations [14].

Unbalanced three-phase voltages lead to oscillation of system variables because of the appearance of negative sequence voltages and currents. Under unbalanced conditions, abnormal harmonics are introduced into the system and appeared at both the input and output terminals and causes distortions in the waveforms. A simplified control scheme based on simplified DSVPWM is proposed for VSI under unbalanced grid voltage conditions.

To achieve a unity power factor of feedback current, phase and amplitude control strategy is proposed and studied.

The conventional SVPWM algorithm of matrix converter needs coordinate transformations, trigonometric calculations, sector number identification etc. The algorithm is difficult to implement and complex calculations. To simplify the algorithm, a unified carrier-based modulation method for direct matrix converter which encompasses main carrier-based PWM strategies is proposed. The method presents a new point of view to better understand a matrix converter modulation method [15].

To prevent dead time effect of direct matrix converter, a compensation method for dead time effect is suggested. Similar to VSI, the value of dead time is adjusted online by the magnitude of corresponding phase current. The deviation of voltage vectors caused by dead time effect is directly compensated to three phase reference voltages [16].

The unified carrier-based modulation method for direct matrix converter is used to indirect matrix converter, dead-time compensation method for VSI and direct matrix converter is used to indirect matrix converter, unbalanced three-phase voltage control for VSI is used to direct matrix converter and indirect matrix converter, and energy feedback control for VSI is used to direct matrix converter and indirect matrix converter.

1.5 Dissertation framework

The contents of this dissertation are organized in seven chapters in the following manner.

Chapter 1 is the introduction of the dissertation. This chapter introduces the research of dc-ac inverter, ac-ac converter, and PWM method.

Chapter 2 describes several modulation methods for VSI. This chapter proposes and investigates SVPWM for two-level VSI, SVPWM for multi-level VSI, discontinuous SVPWM for VSI, and overmodulation method for VSI. Contributions from this research have been presented at [9] - [12].

Chapter 3 gives a control method for VSI. This chapter proposes and investigates dead time compensation method, dc-voltage control for multi-level VSI, unbalanced three phase control method, and energy feedback VSI method. Contributions from this research have been presented at [13][14].

Chapter 4 gives a research of direct matrix converter. This chapter proposes and investigates modulation method for DMC, dead time compensation method, unbalanced three-phase control, and energy feedback control method. Contributions from this research have been presented at [15][16].

Chapter 5 gives a research of indirect matrix converter. This chapter proposes and investigates modulation method for IMC, dead time compensation method, unbalanced three-phase control, and energy feedback control method.

Chapter 6 presents simulation results. This chapter delineates simulation results of energy feedback VSI and matrix converter.

Chapter 7 is the conclusion of the dissertation. This chapter summarizes the contributions of this research work and some suggestions are included for future work.

Chapter 2

Modulation methods for VSI

In this chapter, classical and new methods for space vector modulation (SVPWM) are presented. Continuous, discontinuous, and overmodulated cases are derived. New contributions are: (a) Simplified SVPWM algorithm for three-level neutral point clamped VSI is proposed according to the relationship between two-level SVPWM and SPWM [9]. (b) Simplified and unified SVPWM algorithm for multi-level diode clamped VSI is proposed according to the simplified SVPWM algorithm for two-level inverter and three-level inverter [10]. (c) Carrier-based discontinuous space vector modulation for inverter is proposed by skillfully arranging two zero voltage vectors [11]. (d) Two two-mode overmodulation and two single-mode overmodulation methods for VSI are proposed [12].

2.1 Continuous SVPWM for two-level VSI

2.1.1 Traditional SVPWM for two-level VSI

1) Definition of space vector Voltage, current, and magnetic flux of an ac motor winding are time-varying. They can be represented by time-varying vectors when analyzing the system. If we take the space windings where they belong into account, there signals can be also defined as space vectors. In Figure 2.1, A, B, and C respectively represent the axis of the space stationary three-phase stator windings. The difference between each phase is 120°; three-phase sinusoidal phase voltages (v_a, v_b, v_c) are applied to the three-phase windings. We can define three stator voltage v_a, v_b, v_c, so that they will always be in the direction of the axis of each phase winding, the amplitude changes with time, and the difference between each time phase is 120°. Their combined vector is a space vector that is rotating in the space, and its magnitude will not change. When the power frequency is constant, synthesis

of voltage space vector $v_{ref}^{\rightarrow}$ rotates with constant speed. The voltage vector can be expressed as follows.

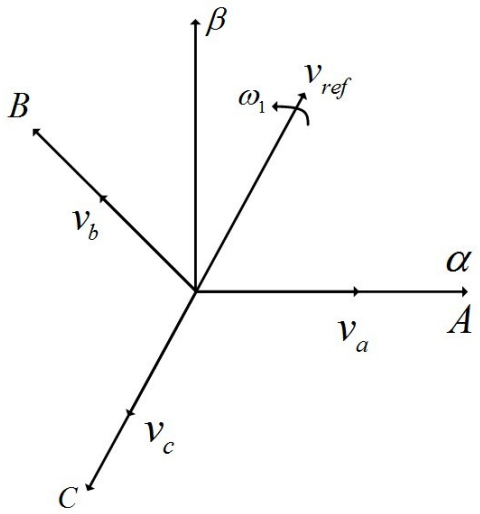


Figure 2.1: Voltage space vector

$$v_{ref}^{\rightarrow} = \frac{2}{3}(v_a + \zeta v_b + \zeta^2 v_c) \tag{2.1}$$

where $\zeta = e^{j\frac{2\pi}{3}}$. According to Euler transformation, ζ is as follows.

$$\zeta = e^{j\frac{2\pi}{3}} = \cos\frac{2\pi}{3} + j\sin\frac{2\pi}{3} = -\frac{1}{2} + j\frac{\sqrt{3}}{2} \tag{2.2}$$

Substituting (2.2) into (2.1), the voltage space vector $v_{ref}^{\rightarrow}$ can be expressed as follows.

$$\begin{cases} v_{ref}^{\rightarrow} & = \frac{2}{3}(v_a + v_b(-\frac{1}{2} + j\frac{\sqrt{3}}{2}) + v_c(-\frac{1}{2} - j\frac{\sqrt{3}}{2})) \\ & = \frac{2}{3}((v_a - \frac{v_b+v_c}{2}) + j\frac{\sqrt{3}(v_b-v_c)}{2}) = \frac{2}{3}||v_{ref}^{\rightarrow}||(\cos\theta + j\sin\theta) \end{cases} \tag{2.3}$$

where the real part represents the component of α axis and imaginary part represents the component of β axis. $||v_{ref}^{\rightarrow}||$ and θ are the length and phase angle for synthesis of reference voltage vector.

2) Coordinate transformations General mathematical model of inverter in the three-phase stationary symmetry coordinate (A, B, C) have clear physical meaning. However, in

this mathematical model, the ac side of inverter is time-varying ac value which is not easy to use for control system design. Therefore, the three-phase stationary coordinate system (A, B, C) is converted into two-phase stationary coordinate system (α, β) through coordinate transformation. The coordinate transformation can be one of two types: equivalent amount or equivalent power. Equivalent amount means voltage vector is equal before and after coordinate transformation, and is also known as $\frac{2}{3}$ conversion. Equivalent power means power is equal before and after coordinate transformation, and is also known as $\sqrt{\frac{2}{3}}$ conversion. In practice, one can arbitrarily choose the conversion type according to the specific requirements. The following coordinate transformation is $\frac{2}{3}$ conversion.

Voltage vectors v_a, v_b, and v_c are orthogonally decomposed on the α, β axis, as Figure 2.2 shows.

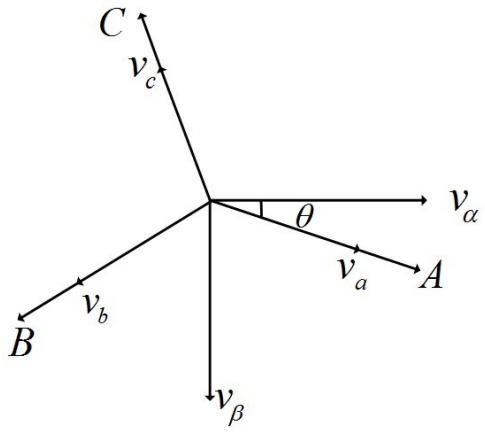


Figure 2.2: Equivalent amount coordinate transformation

$$\begin{cases} v_a &= v_\alpha \cos\theta + v_\beta \sin\theta \\ v_b &= v_\alpha \cos(\theta - \frac{2\pi}{3}) + v_\beta \sin(\theta - \frac{2\pi}{3}) \\ v_c &= v_\alpha \cos(\theta + \frac{2\pi}{3}) + v_\beta \sin(\theta + \frac{2\pi}{3}) \end{cases} \tag{2.4}$$

Matrix form is as follows:

$$\begin{Bmatrix} v_a \\ v_b \\ v_c \end{Bmatrix} = \begin{Bmatrix} \cos\theta & \sin\theta \\ \cos(\theta - \frac{2\pi}{3}) & \sin(\theta - \frac{2\pi}{3}) \\ \cos(\theta + \frac{2\pi}{3}) & \sin(\theta + \frac{2\pi}{3}) \end{Bmatrix} \begin{Bmatrix} v_\alpha \\ v_\beta \end{Bmatrix} \tag{2.5}$$

$$\begin{Bmatrix} v_\alpha \\ v_\beta \end{Bmatrix} = \frac{2}{3} \begin{Bmatrix} \cos\theta & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ \sin\theta & \sin(\theta - \frac{2\pi}{3}) & \sin(\theta + \frac{2\pi}{3}) \end{Bmatrix} \begin{Bmatrix} v_a \\ v_b \\ v_c \end{Bmatrix} \tag{2.6}$$

When $\theta = 0$, axis α and axis A are in the same direction. Then the matrix form is as follows.

$$\begin{Bmatrix} v_a \\ v_b \\ v_c \end{Bmatrix} = \begin{Bmatrix} 1 & 0 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \end{Bmatrix} \begin{Bmatrix} v_\alpha \\ v_\beta \end{Bmatrix} \tag{2.7}$$

$$\begin{Bmatrix} v_\alpha \\ v_\beta \end{Bmatrix} = \frac{2}{3} \begin{Bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & -\frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \end{Bmatrix} \begin{Bmatrix} v_a \\ v_b \\ v_c \end{Bmatrix} \tag{2.8}$$

The coordinate transformations are similar to the Park and Clark transformations.

3) The basic principle of SVPWM Figure 2.3 depicts the schematic of three-phase PWM inverter-fed induction motor. To make the motor work symmetrically, three-phase windings must be simultaneously powered. There must be three devices at different legs turned on simultaneously at any time, the other corresponding power devices are turned off. Thus from the inverter topology, there are eight working conditions. Eight kinds of working conditions are S6, S1, S2 turned on, S1, S2, S3 turned on, S2, S3, S4 turned on, S3, S4, S5 turned on, S4, S5, S6 turned on, S5, S6, S1 turned on, S1, S3, S5 turned on, and S2, S4, S6 turned on. From the normal operation of the inverter, the first six operation states are valid and the latter two operation states are meaningless.

Set δ_a, δ_b, δ_c are output state of each leg.

$$\delta_a, \delta_b, \delta_c = \begin{cases} 1 & \text{upper switch on} \\ 0 & \text{upper switch off} \end{cases} \tag{2.9}$$

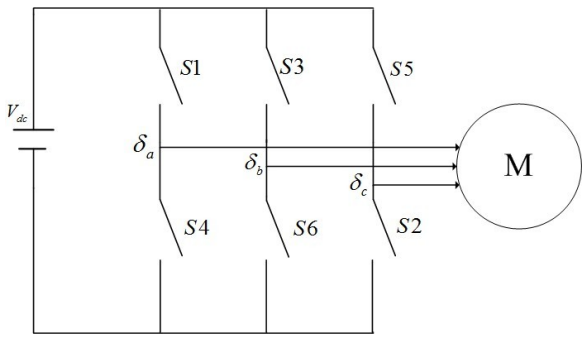


Figure 2.3: Schematics of three-phase PWM inverter-fed induction motor

For the three-phase inverter (as Figure 2.3 shows), its voltage vector $\vec{v_\delta}$ can be expressed as follows.

$$\begin{cases} \vec{v_\delta} &= \frac{2}{3}(\delta_a V_{dc} + \delta_b V_{dc}(-\frac{1}{2} + j\frac{\sqrt{3}}{2}) + \delta_c V_{dc}(-\frac{1}{2} - j\frac{\sqrt{3}}{2})) \\ &= \frac{2}{3}((\delta_a - \frac{\delta_b+\delta_c}{2})V_{dc} + j\frac{\sqrt{3}(\delta_b-\delta_c)V_{dc}}{2}) \end{cases} \tag{2.10}$$

where V_{dc} is the dc-link voltage of the inverter.

The eight kinds of switching states using δ_a, δ_b, and δ_c, are shown in Table 2.1 [17] - [20]. Eight switching states formed eight voltage vectors in the space (as shown in Table 2.2). Wherein the vectors $\vec{V_0}$ and $\vec{V_7}$ are equal, they coincide with the origin of coordinates. Eight voltage vectors divide the plane into six sectors, as shown in Figure 2.4. Vector $\vec{v_{ref}}$

Switching state	0	1	2	3	4	5	6	7
$[\delta_a, \delta_b, \delta_c]$	[000]	[100]	[110]	[010]	[011]	[001]	[101]	[111]

Table 2.1: Switching states of three-phase inverter

$\vec{V_1}$	$\vec{V_2}$	$\vec{V_3}$	$\vec{V_4}$	$\vec{V_5}$	$\vec{V_6}$	$\vec{V_7}$	$\vec{V_0}$
$\frac{2}{3}V_{dc}$	$\frac{2}{3}V_{dc}(\frac{1}{2} + j\frac{\sqrt{3}}{2})$	$\frac{2}{3}V_{dc}(-\frac{1}{2} + j\frac{\sqrt{3}}{2})$	$-\frac{2}{3}V_{dc}$	$\frac{2}{3}V_{dc}(-\frac{1}{2} - j\frac{\sqrt{3}}{2})$	$\frac{2}{3}V_{dc}(\frac{1}{2} - j\frac{\sqrt{3}}{2})$	0	0

Table 2.2: Voltage vectors of three-phase inverter

can be synthesized by eight voltage vectors. To determine the involvement voltage vectors, first determine sector number in which sector $\vec{v_{ref}}$ falls. For example, if $\vec{v_{ref}}$ fall into the first sector, $\vec{v_{ref}}$ is composed with two adjacent effective voltage vectors $\vec{V_1}$, $\vec{V_2}$ and zero voltage vectors $\vec{V_0}$, $\vec{V_7}$. T_0, T_1, ..., T_7 are defined as the applying time of the voltage vectors $\vec{V_0}$ ... $\vec{V_7}$ representing. T_s is one period of switching time. After sector number identification,

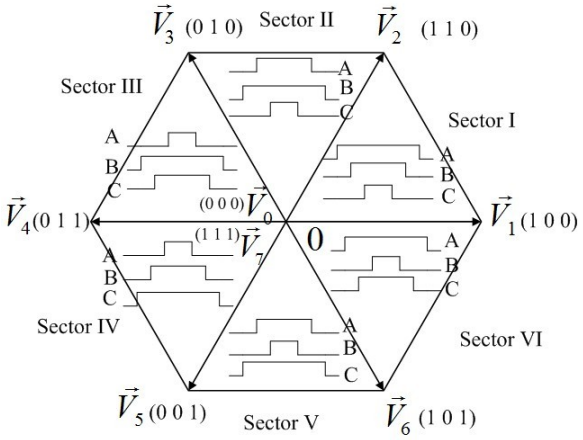


Figure 2.4: The relationship between voltage vectors and sectors

according to the principle of vector synthesis, the following equation is obtained.

$$\begin{cases} T_s \vec{v_{ref}} &= \vec{V_1} T_1 + \vec{V_2} T_2 \\ T_s &= T_1 + T_2 + T_0 + T_7 \end{cases} \tag{2.11}$$

When $\vec{v_{ref}}$ falls into the first sector, we can obtain the following results by solving equation (2.11).

$$\begin{cases} T_1 &= \frac{\sqrt{3}\|\vec{v_{ref}}\|T_s}{V_{dc}} \sin(\frac{\pi}{3} - \gamma) \\ T_2 &= \frac{\sqrt{3}\|\vec{v_{ref}}\|T_s}{V_{dc}} \sin(\gamma) \\ T_z &= T_s - T_1 - T_2 \end{cases} \tag{2.12}$$

where γ is an angle in a 60° sector, $||\vec{v_{ref}}||$ is a magnitude of reference voltage vector $\vec{v_{ref}}$, T_z is total applying time of zero voltage vectors, and V_{dc} is dc-link voltage.

Figure 2.5 shows seven-segment SVPWM regular sampling in sector 1.

In short, there are two key steps to achieve the SVPWM algorithm. 1) How to determine the sector number in which the synthesis of reference voltage space vector falls. 2) Use equation (2.12), solving T_1, T_2, and T_z. From the above discussion, dealing with these two issues can be very complex. This process must solve arctangent function and length for synthesis of reference voltage vector $||\vec{v_{ref}}||$. It is difficult to ensure the accuracy and speed of computing. Computing and storage of hardware systems require higher performance.

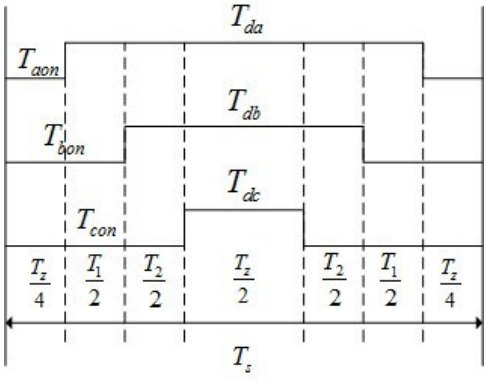


Figure 2.5: Switching signals of seven-segment SVPWM algorithm in sector 1

2.1.2 The intrinsic relationship between SVPWM and SPWM

Any given reference voltage vector $\vec{v_{ref}}$ is synthesized by a number of basic voltage vector in each sampling period. As shown in Figure 2.6, if the expected reference voltage vector $\vec{v_{ref}}$ is placed in the sector which is composed of $\vec{V_k}$ and $\vec{V_{k+1}}$, then $\vec{v_{ref}}$ is composed with two adjacent effective voltage vectors $\vec{V_k}$, $\vec{V_{k+1}}$ and zero voltage vectors $\vec{V_0}$, $\vec{V_7}$. By employing voltammetry balance law and parallelogram law, the applying time of two adjacent vectors are calculated in the following functions:

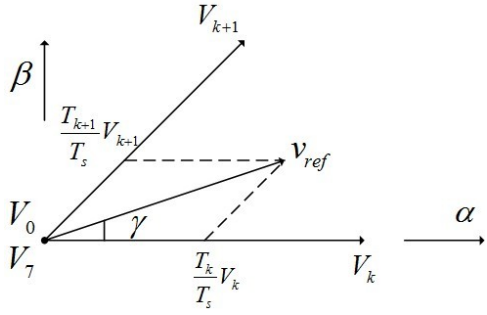
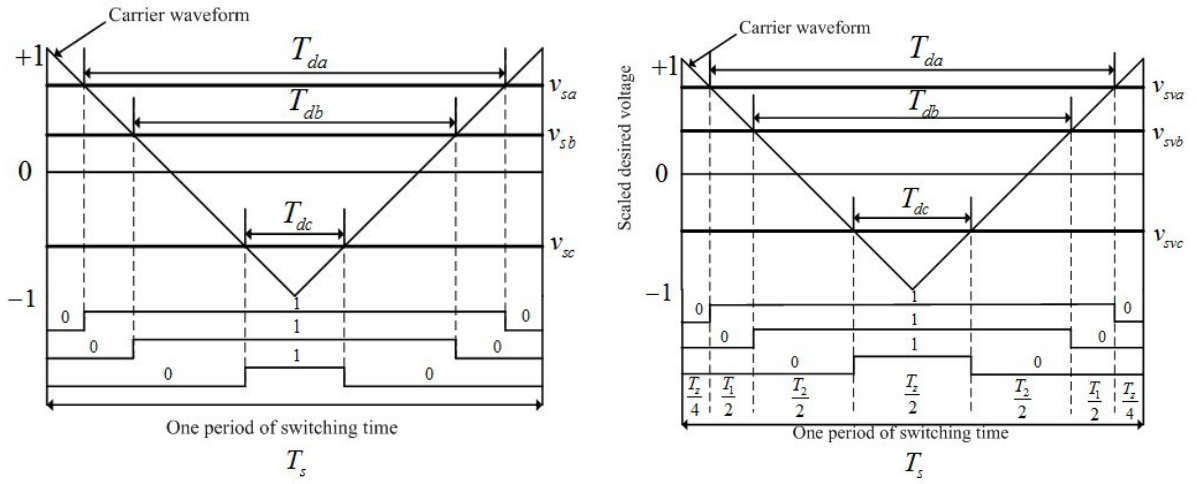


Figure 2.6: Voltage vector synthesis

$$\begin{cases} T_k & = \frac{\sqrt{3}\|\vec{v_{ref}}\|T_s}{V_{dc}} \sin(\frac{\pi}{3} - \gamma) \\ T_{k+1} & = \frac{\sqrt{3}\|\vec{v_{ref}}\|T_s}{V_{dc}} \sin(\gamma) \end{cases} \tag{2.13}$$

In the standard SVPWM algorithm, applying time of zero voltage vectors T_0 and T_7 are the same. Waveform comparison between two-level sinusoidal PWM (SPWM) and SVPWM in



(a) Switching signals of SPWM regular sampling

(b) Switching signals of seven-segment SVPWM regular sampling

Figure 2.7: Switching signals of PWM method

sector one is illustrated in Figure 2.7. From Figure 2.7, the waveform of SPWM symmetric regular sampling is similar to the waveform of seven-segment SVPWM symmetric sampling. The only difference is that the two methods have different operation time of zero voltage vectors. Therefore, modulation implicit functions of SVPWM are derived from modulation implicit functions of SPWM. From Figure 2.7(a), pulse width of SPWM is calculated by the following equations [21][9].

$$\begin{cases} T_{da} &= T_s \frac{1+v_{sa}}{2} \\ T_{db} &= T_s \frac{1+v_{sb}}{2} \\ T_{dc} &= T_s \frac{1+v_{sc}}{2} \end{cases} \tag{2.14}$$

where T_{da}, T_{db}, T_{dc} are pulse width of a, b, c three phase, v_{sa}, v_{sb}, v_{sc} are modulation implicit values of a, b, c three phase for SPWM. From formula (2.14), modulation implicit functions of SPWM are obtained.

$$\begin{cases} v_{sa} &= \frac{2\times T_{da}}{T_s} - 1 \\ v_{sb} &= \frac{2\times T_{db}}{T_s} - 1 \\ v_{sc} &= \frac{2\times T_{dc}}{T_s} - 1 \end{cases} \tag{2.15}$$

Figure 2.7(b) is the waveform of seven-segment SVPWM in the first sector, and its pulse width is as follows:

$$\begin{cases} T_{da} &= \frac{T_z}{2} + T_1 + T_2 \\ T_{db} &= \frac{T_z}{2} + T_2 \\ T_{dc} &= \frac{T_z}{2} \end{cases} \tag{2.16}$$

Since $T_z = T_s - T_1 - T_2$, the formula (2.16) can be expressed as following equations.

$$\begin{cases} T_{da} &= \frac{T_s+T_1+T_2}{2} \\ T_{db} &= \frac{T_s-T_1+T_2}{2} \\ T_{dc} &= \frac{T_s-T_1-T_2}{2} \end{cases} \tag{2.17}$$

Formula (2.17) into (2.15), modulation implicit functions of SVPWM are as follows.

$$\begin{cases} v_{sva} &= \frac{T_1+T_2}{T_s} \\ v_{svb} &= \frac{-T_1+T_2}{T_s} \\ v_{svc} &= \frac{-T_1-T_2}{T_s} \end{cases} \tag{2.18}$$

The relationship between three-phase voltages and sector numbers are illustrated in Figure 2.8. To make reference voltage vector $\vec{v_{ref}}$ in the first sector, the angle between $\vec{v_{ref}}$ and α axes is θ, then $\frac{\pi}{2} \leq \theta < \frac{5\pi}{6}$. From formula (2.12), $0 \leq \gamma < \frac{\pi}{3}$ when reference voltage vector is in the first sector.

$$\gamma = \theta - \frac{\pi}{2} \tag{2.19}$$

Formula (2.19) into (2.12), then applying time of effective voltages is deduced as follows:

$$\begin{cases} T_1 &= \frac{\sqrt{3}}{4} M T_s (\sqrt{3} \sin\theta - \cos\theta) \\ T_2 &= -\frac{\sqrt{3}}{2} M T_s \cos\theta \end{cases} \tag{2.20}$$

where M is ratio of modulation and $M = \frac{2V_m}{V_{dc}}$, V_m is amplitude of three-phase voltages. From equations (2.18) to (2.20), the expression of modulation implicit functions of SVPWM

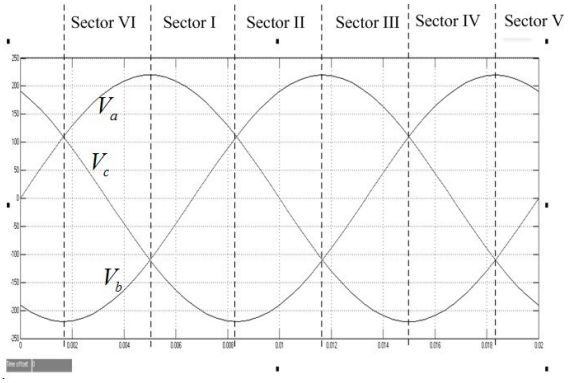


Figure 2.8: The division of the sector

v_{sva}, v_{svb}, v_{svc} in the first sector are as follows:

$$\begin{cases} v_{sva} &= \frac{\sqrt{3}}{2} M \sin(\theta - \frac{\pi}{6}) \\ v_{svb} &= \frac{3}{2} M \sin(\theta - \frac{2\pi}{3}) \\ v_{svc} &= \frac{\sqrt{3}}{2} M \sin(\theta + \frac{5\pi}{6}) \end{cases} \tag{2.21}$$

Similarly, it is possible to deduce modulation implicit functions of SVPWM in other sectors.

$$v_{sva} = \begin{cases} \frac{3}{2} M \sin\theta & 0 \le \theta < \frac{\pi}{6} \\ \frac{\sqrt{3}}{2} M \sin(\theta + \frac{\pi}{6}) & \frac{\pi}{6} \le \theta < \frac{\pi}{2} \\ \frac{\sqrt{3}}{2} M \sin(\theta - \frac{\pi}{6}) & \frac{\pi}{2} \le \theta < \frac{5\pi}{6} \\ \frac{3}{2} M \sin\theta & \frac{5\pi}{6} \le \theta < \frac{7\pi}{6} \\ \frac{\sqrt{3}}{2} M \sin(\theta + \frac{\pi}{6}) & \frac{7\pi}{6} \le \theta < \frac{3\pi}{2} \\ \frac{\sqrt{3}}{2} M \sin(\theta - \frac{\pi}{6}) & \frac{3\pi}{2} \le \theta < \frac{11\pi}{6} \\ \frac{3}{2} M \sin\theta & \frac{11\pi}{6} \le \theta < 2\pi \end{cases} \tag{2.22}$$

$$v_{svb} = \begin{cases} \frac{\sqrt{3}}{2}M\sin(\theta - \frac{\pi}{2}) & 0 \le \theta < \frac{\pi}{6} \\ -\frac{\sqrt{3}}{2}M\sin(\theta + \frac{\pi}{6}) & \frac{\pi}{6} \le \theta < \frac{\pi}{2} \\ \frac{3}{2}M\sin(\theta - \frac{2\pi}{3}) & \frac{\pi}{2} \le \theta < \frac{5\pi}{6} \\ \frac{\sqrt{3}}{2}M\sin(\theta - \frac{\pi}{2}) & \frac{5\pi}{6} \le \theta < \frac{7\pi}{6} \\ -\frac{\sqrt{3}}{2}M\sin(\theta + \frac{\pi}{6}) & \frac{7\pi}{6} \le \theta < \frac{3\pi}{2} \\ \frac{3}{2}M\sin(\theta - \frac{2\pi}{3}) & \frac{3\pi}{2} \le \theta < \frac{11\pi}{6} \\ \frac{\sqrt{3}}{2}M\sin(\theta - \frac{\pi}{2}) & \frac{11\pi}{6} \le \theta < 2\pi \end{cases} \tag{2.23}$$

$$v_{svc} = \begin{cases} \frac{\sqrt{3}}{2}M\sin(\theta + \frac{\pi}{2}) & 0 \le \theta < \frac{\pi}{6} \\ \frac{3}{2}M\sin(\theta + \frac{2\pi}{3}) & \frac{\pi}{6} \le \theta < \frac{\pi}{2} \\ \frac{\sqrt{3}}{2}M\sin(\theta + \frac{5\pi}{6}) & \frac{\pi}{2} \le \theta < \frac{5\pi}{6} \\ \frac{\sqrt{3}}{2}M\sin(\theta + \frac{\pi}{2}) & \frac{5\pi}{6} \le \theta < \frac{7\pi}{6} \\ \frac{3}{2}M\sin(\theta + \frac{2\pi}{3}) & \frac{7\pi}{6} \le \theta < \frac{3\pi}{2} \\ \frac{\sqrt{3}}{2}M\sin(\theta + \frac{5\pi}{6}) & \frac{3\pi}{2} \le \theta < \frac{11\pi}{6} \\ \frac{\sqrt{3}}{2}M\sin(\theta + \frac{\pi}{2}) & \frac{11\pi}{6} \le \theta < 2\pi \end{cases} \tag{2.24}$$

Decompose equations (2.22) to (2.24), the simplified modulation implicit functions of SVPWM are as follows:

$$\begin{cases} v_{sva} &= v_{sa} + v_z \\ v_{svb} &= v_{sb} + v_z \\ v_{svc} &= v_{sc} + v_z \end{cases} \tag{2.25}$$

$$\begin{cases} v_{sa} &= M\sin(\omega t) \\ v_{sb} &= M\sin(\omega t - \frac{2\pi}{3}) \\ v_{sc} &= M\sin(\omega t + \frac{2\pi}{3}) \end{cases} \tag{2.26}$$

$$v_z = \begin{cases} \frac{M}{2}\sin\omega t & 0 \le \theta < \frac{\pi}{6} \\ \frac{M}{2}\sin(\omega t + \frac{2\pi}{3}) & \frac{\pi}{6} \le \theta < \frac{\pi}{2} \\ \frac{M}{2}\sin(\omega t - \frac{2\pi}{3}) & \frac{\pi}{2} \le \theta < \frac{5\pi}{6} \end{cases} \tag{2.27}$$

The equation (2.27) can be expressed as the following equation.

$$v_z = -\frac{1}{2}(v_{max} + v_{min}) \tag{2.28}$$

where v_{max}, v_{min} are the maximum and minimum values of v_{sa}, v_{sb}, v_{sc}, respectively. The equation (2.25) shows that the modulation implicit functions of SVPWM can be obtained by adding component (zero voltage vectors) to the modulation implicit functions of SPWM. Pulse width of SVPWM can be calculated by formula (2.14).

2.1.3 A simplified SVPWM algorithm for two-level inverter

A simplified SVPWM algorithm for two-level inverter can be obtained by simplified modulation implicit functions. The algorithm uses the instantaneous values of three phase voltages to calculate modulation implicit functions, then compares with carrier triangular waveform, and finally calculates actual gating time for each inverter leg. It doesn't need coordinate transformations, trigonometric calculations, sector number identification, and calculation of actual gating time [9][22] - [24]. So it not only has the advantage of the conventional SVPWM algorithm with fast dynamic response, but also needs less computation time.

Assuming three phase desired voltages are as follows:

$$v_i = V_m \sin(\omega t - \frac{2l\pi}{3}) \quad i \in (a, b, c) \;\; l \in (1, 2, 3) \tag{2.29}$$

where V_m is magnitude of three-phase desired voltages and ω is angular frequency. Each phase voltage is scaled by reference voltage $\frac{V_{dc}}{2}$, so three phase desired voltages become modulation implicit functions of SPWM.

$$v_{si} = \frac{2V_m}{V_{dc}} \sin(\omega t - \frac{2l\pi}{3}) \quad i \in (a, b, c) \;\; l \in (1, 2, 3) \tag{2.30}$$

The modulation implicit functions of SVPWM are obtained by the following formula.

$$v_{svi} = v_{si} + v_z \quad i \in (a, b, c) \tag{2.31}$$

where v_z is zero voltage value. The modulation implicit functions are working as SPWM algorithm when $v_z = 0$, and the modulation implicit functions are working as continuous SVPWM (CSVPWM) algorithm when $v_z = (1 - 2k) - kv_{min} - (1 - k)v_{max}$, $0 < k < 1$, where v_{max}, v_{min} are maximum and minimum values of v_{sa}, v_{sb}, v_{sc}. It is standard SVPWM algorithm when $k = 0.5$. According to Figure 2.7, in a sampling period, pulse width of SVPWM is as follows:

$$T_{di} = T_s \frac{1 + v_{svi}}{2} \quad i \in (a, b, c) \tag{2.32}$$

From equation (2.32), the actual gating time of SVPWM algorithm is deduced as follows:

$$T_{ion} = \frac{T_s - T_{di}}{2} \quad i \in (a, b, c) \tag{2.33}$$

A simplified SVPWM algorithm, in which the three-phase desired voltages are used to calculate actual gating time for each inverter leg directly, is derived.

2.2 Continuous SVPWM for multi-level VSI

2.2.1 Traditional SVPWM for three-level neutral point clamped VSI

With the increasing demand of high-voltage and high-power equipments, such as high voltage ac drive, flexible ac transmission system, static var compensator, static compensator and so on, multi-level inverters especially three-level inverters have been focused on and became effective and practical solutions to high-power high-voltage application field. Compared with two-level inverters, three-level inverters have some advantages: (1) reduce voltage stress on switches; (2) lower harmonic distortion of output voltage and current; (3) lower switch losses. Three main topologies for three-level inverters are neutral point clamped

(NPC) inverters, cascaded H-bridge inverters, and the flying capacitors inverters. The NPC topology offers advantages such as reduced switching losses and smaller output current ripple. The three-level NPC inverter is probably the most widely used topology for medium voltage ac motor drives and PWM active rectifiers.

In 1980s, German scholar Joachim Holtz proposed and optimized three-level NPC VSI [25]. Since then, this topology has been widely used in high voltage and high power equipments. The topology of three-phase three-level NPC VSI is shown in Figure 2.9.

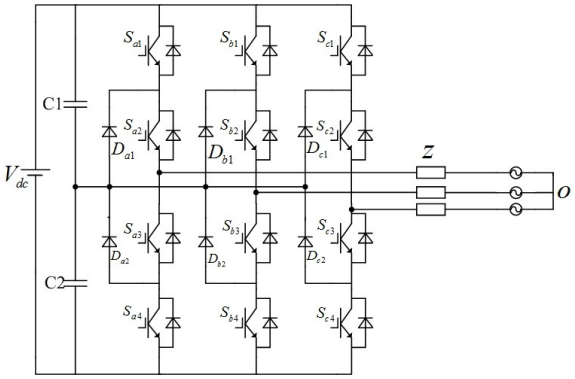


Figure 2.9: Main circuit of three-phase three-level NPC VSI

In the dc side, two capacitors C1 and C2 support and balance the dc voltage, so $C1 = C2$. Each phase has four power switches, four freewheeling diodes, and two midpoint clamped diodes. Table 2.3 shows the switching states of three-level inverter. Each phase has three output states, P, O, and N, corresponding to positive voltage (+), zero voltage (0), and negative voltage (-). Taking phase a as an example, if switch S_{a1} and S_{a2} are turned on, then phase a is in the P state; if switch S_{a2} and S_{a3} are turned on, then phase a is in the O state. Similarly, when switch S_{a3} and S_{a4} are turned on, then phase a is in the N state. Since three kinds of switching states exist in each phase, three-level inverter has 27 (3^3) switching states. Table 2.4 shows, vectors are divided into 6 large switching states, 6 middle switching states, 12 small switching states, and 3 zero switching states. Using $\frac{2}{3}$ coordinate transformation as section 2.1.1 explains and equation (2.10), we can determine 27 voltage vectors in the space corresponding to 27 switching states (as shown in Table 2.5 [26] - [32]).

Every switching states corresponding to specific voltage vectors, for example PNN corresponding to V_7 ($\frac{2}{3}V_{dc}\angle 0°$) and PPO corresponding to V_2 ($\frac{1}{3}V_{dc}\angle 60°$). Similarly, we can get 27 voltage vectors including 3 zero vectors, 12 small vectors, 6 middle vectors, and 6 large vectors. Wherein the voltage vector corresponding to PPP, OOO, and NNN are equal, they coincide with the origin of coordinates. The voltage space vector operates in a complex plane which is divided into six large sectors, and each of them is divided into six small sectors, as shown in Figure 2.10 [27] - [32]. As Figure 2.10 shows, the angle from 0° to 60° is big sector I, ..., 300° to 360° is big sector VI. The small sectors are obtained by small vectors, middle vectors, and large vectors, as shown in Figure 2.11.

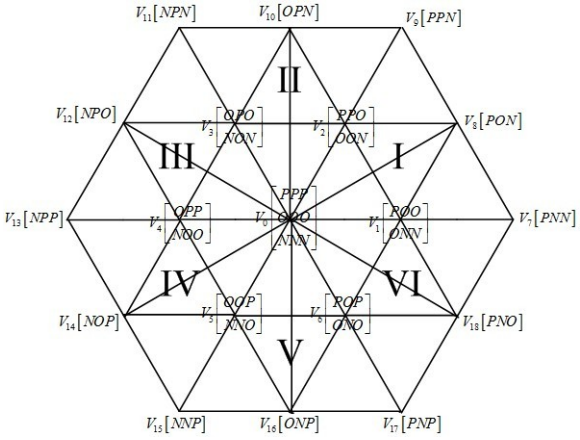


Figure 2.10: Switching state vectors for three-level inverter

Voltage $\vec{v_{ref}}$ can be synthesized by 27 voltage vectors. To determine the involved voltage vectors, first determine sector number in which sector $\vec{v_{ref}}$ falls. Assuming an expected reference voltage $\vec{v_{ref}}$ is located in the region E, as shown in Figure 2.11. Based on the principle of nearest triangle vector, reference voltage $\vec{v_{ref}}$ is composed of three vectors V_1,

Output State	S_1	S_2	S_3	S_4	Output voltage
$P(1)$	on	on	off	off	$+\frac{V_{dc}}{2}$
$O(0)$	off	on	on	off	0
$N(-1)$	off	off	on	on	$-\frac{V_{dc}}{2}$

Table 2.3: Relationship between switching states and output voltages of three-level inverter

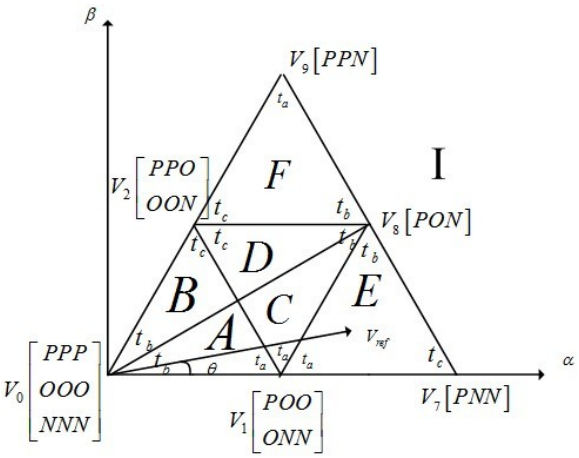


Figure 2.11: Division of sector I

V_7, and V_8. Reference voltage may locate in any region of all the vector space; we should determine the correct sector number it locates in. As Figure 2.11 shows, the reference voltage is located in the big sector I. Then using equations (2.34) to (2.37), we can calculate pulse width of three voltage vectors.

$$Region\ A\ and\ B : v_{ref}T_s = t_aV_1 + t_bV_0 + t_cV_2 \tag{2.34}$$

$$Region\ C\ and\ D : v_{ref}T_s = t_aV_1 + t_bV_8 + t_cV_2 \tag{2.35}$$

$$Region\ E : v_{ref}T_s = t_aV_1 + t_bV_8 + t_cV_7 \tag{2.36}$$

$$Region\ F : v_{ref}T_s = t_aV_9 + t_bV_8 + t_cV_2 \tag{2.37}$$

where T_s is one period of switching time; t_a, t_b, and t_c are pulse width of voltage vectors V_a, V_b, V_c, and $T_s = t_a + t_b + t_c$. Table 2.6 lists applying time of each voltage vector when

Output voltage vectors	Switching states
Large	PNN, PPN, NPN, NPP, NNP, PNP
Middle	PON, OPN, NPO, NOP, ONP, PNO
Small	POO, ONN, PPO, OON, OPO, NON, OPP, NOO, OOP, NNO, POP, ONO
Zero	PPP, OOO, NNN

Table 2.4: Classification of switching states

Switching states	voltage space vector
PPP, OOO, NNN	0
POO, ONN	$\frac{1}{3}V_{dc}$
PNN	$\frac{2}{3}V_{dc}$
PON	$\frac{\sqrt{3}}{3}V_{dc}\angle\frac{\pi}{6}$
PPO, OON	$\frac{1}{3}V_{dc}\angle\frac{\pi}{3}$
PPN	$\frac{2}{3}V_{dc}\angle\frac{\pi}{3}$
OPN	$\frac{\sqrt{3}}{3}V_{dc}\angle\frac{\pi}{4}$
OPO, NON	$\frac{1}{3}V_{dc}\angle\frac{2\pi}{3}$
NPN	$\frac{2}{3}V_{dc}\angle\frac{2\pi}{3}$
NPO	$\frac{\sqrt{3}}{3}V_{dc}\angle\frac{5\pi}{6}$
OPP, NOO	$\frac{1}{3}V_{dc}\angle\pi$
NPP	$\frac{2}{3}V_{dc}\angle\pi$
NOP	$\frac{\sqrt{3}}{3}V_{dc}\angle\frac{7\pi}{6}$
OOP, NNO	$\frac{1}{3}V_{dc}\angle\frac{4\pi}{3}$
NNP	$\frac{2}{3}V_{dc}\angle\frac{4\pi}{3}$
ONP	$\frac{\sqrt{3}}{3}V_{dc}\angle\frac{3\pi}{2}$
POP, ONO	$\frac{1}{3}V_{dc}\angle\frac{5\pi}{3}$
PNP	$\frac{2}{3}V_{dc}\angle\frac{5\pi}{3}$
PNO	$\frac{\sqrt{3}}{3}V_{dc}\angle\frac{11\pi}{6}$

Table 2.5: Relationship between switching states and voltage vectors

the reference voltage is located in the big sector I. Where $K = \frac{2\|\vec{v_{ref}}\|}{\sqrt{3}V_{dc}}$, θ is the phase angle

Region	t_a	t_b	t_c
A, B	$T_s[2Ksin(\frac{\pi}{3}-\theta)]$	$T_s[1-2Ksin(\frac{\pi}{3}+\theta)]$	$T_s[2Ksin(\theta)]$
C, D	$T_s[1-2Ksin(\theta)]$	$T_s[2Ksin(\frac{\pi}{3}+\theta)-1]$	$T_s[1-2Ksin(\frac{\pi}{3}-\theta)]$
E	$T_s[2-2Ksin(\frac{\pi}{3}+\theta)]$	$T_s[2Ksin(\theta)]$	$T_s[2Ksin(\frac{\pi}{3}-\theta)-1]$
F	$T_s[2Ksin(\theta)-1]$	$T_s[2Ksin(\frac{\pi}{3}-\theta)]$	$T_s[2-2Ksin(\frac{\pi}{3}+\theta)]$

Table 2.6: Applying time of three voltage vectors in big sector I

between reference voltage and α axis, $\|\vec{v_{ref}}\|$ is magnitude of reference voltage vector, and V_{dc} is the dc-link voltage.

Similarly, we can calculate applying time of three voltage vectors in other big sector. If take region A as an example, in a period of switching cycle, the output switching states are POO, OOO, OON, ONN, OON, OOO, POO when we are using seven-segment SVPWM algorithm, as Figure 2.12 shows. And the corresponding applying time are $\frac{t_a}{4}$, $\frac{t_b}{2}$, $\frac{t_c}{2}$, $\frac{t_a}{2}$, $\frac{t_c}{2}$,

$\frac{t_b}{2}$, and $\frac{t_a}{4}$. Similarly, we can get the output vectors and corresponding applying time when the reference voltage is placed in other region.

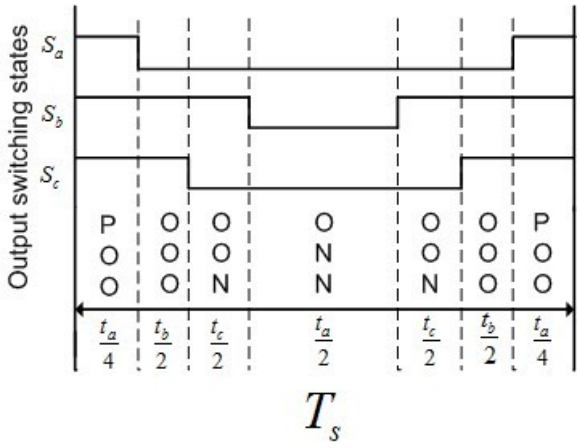
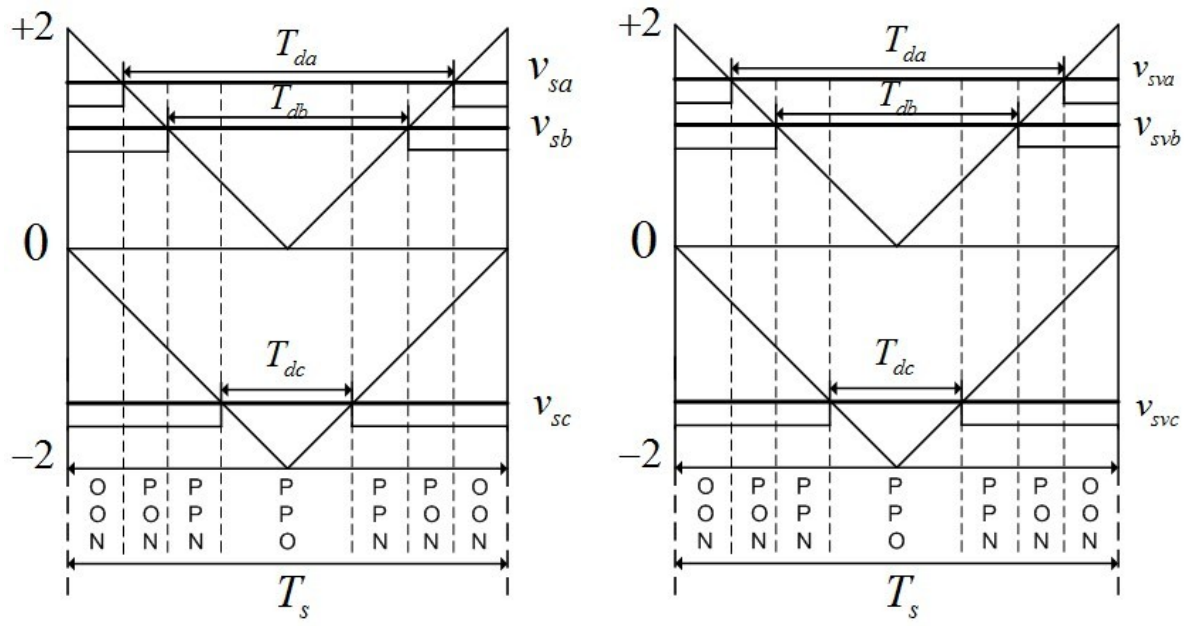


Figure 2.12: Switching states and corresponding applying time

Similar to two-level VSI, it is difficult to determine the sector number in which the synthesis of reference voltage space vector falls. And t_a, t_b, t_c are also hard to calculate quickly. This process must solve arctangent function and module length of synthesis of reference voltage vector. It is difficult to ensure the accuracy and speed of computing. Computing and storage of hardware systems require higher performance.

2.2.2 A simplified SVPWM algorithm for three-level inverter

1) The relationship between SVPWM and SPWM for three-level inverter As the modulation implicit functions of SVPWM for two-level inverter are deduced, the modulation implicit functions of SVPWM for three-level inverter can be derived in the same way. Similar with the relationship between SVPWM and SPWM for two-level inverter, the relationship between SVPWM and SPWM for three-level inverter is shown in Figure 2.13. From Figure 2.13, the waveform of SPWM symmetric regular sampling is similar to the waveform of seven-segment SVPWM symmetric sampling. The only difference is that the two methods have different operation time of zero voltage vectors. Therefore, modulation implicit functions of SVPWM are derived from modulation implicit functions of SPWM. The modulation implicit



(a) Switching signals of SPWM regular sampling (b) Switching signals of seven-segment SVPWM regular sampling

Figure 2.13: Switching signals for three-level inverter

functions of SVPWM are obtained by equations (2.25) to (2.28). The pulse width of SVPWM is obtained by formula (2.38).

$$T_{di} = T_s \frac{v_{svi}}{2} \quad i \in (a, b, c) \tag{2.38}$$

The pulse widths of SPWM and SVPWM can be compared with upper triangle waveform if the value is bigger than 0. In this case, power switches are at states P or O. Correspondingly, when the value is smaller than 0, then the pulse widths of SPWM and SVPWM can be compared with lower triangle waveform, and the power switches are at states O or N.

2) A simplified SVPWM algorithm for three-level inverter A simplified SVPWM algorithm for three-level inverter can be obtained by simplified modulation implicit functions of SVPWM. The algorithm uses the instantaneous values of three phase voltages to calculate modulation implicit functions of SVPWM, then compares with carrier triangular waveform,

finally calculates actual gating time for each inverter leg. It doesn't need coordinate transformations, trigonometric calculations, and sector number identification. So it not only has the advantage of the conventional SVPWM algorithm with fast dynamic response, but also needs less computation time [9][33][34].

Assuming three phase desired voltages are as follows:

$$\begin{cases} v_a &= V_m \sin(\omega t) \\ v_b &= V_m \sin(\omega t - \frac{2\pi}{3}) \\ v_c &= V_m \sin(\omega t + \frac{2\pi}{3}) \end{cases} \tag{2.39}$$

Each phase voltage is scaled by reference voltage $\frac{V_{dc}}{4}$, three phase desired voltages become modulation implicit functions of SPWM:

$$\begin{cases} v_{sa} &= \frac{4V_m}{V_{dc}} \sin(\omega t) \\ v_{sb} &= \frac{4V_m}{V_{dc}} \sin(\omega t - \frac{2\pi}{3}) \\ v_{sc} &= \frac{4V_m}{V_{dc}} \sin(\omega t + \frac{2\pi}{3}) \end{cases} \tag{2.40}$$

The modulation implicit functions of SVPWM are as follows:

$$v_{svi} = v_{si} + v_z \quad i \in (a, b, c) \tag{2.41}$$

$$v_z = (2 - 4k) - k v_{min} - (1 - k) v_{max} \quad 0 < k < 1 \tag{2.42}$$

where v_z is zero voltage value. When $v_z = 0$, then the modulation implicit functions are working as SPWM algorithm, and when $0 < k < 1$, then the modulation implicit functions are working as continuous SVPWM, where v_{max}, v_{min} are the maximum and minimum values of v_{ra}, v_{rb}, v_{rc}. It is standard SVPWM algorithm when $k = 0.5$. According to Figure 2.13, in a sampling period, the pulse width of SVPWM is obtained by the formula (2.38). The value of T_{di} might be positive or negative with different modulation index. After calculating pulse width of SVPWM, judge the sign of T_{di}, make duration of P states to be T_{di} and duration

of O states to be $T_s - T_{di}$ when $\text{sgn}(T_{di}) = 1$, and make duration of N states to be $||T_{di}||$ and duration of O states to be $T_s + T_{di}$ when $\text{sgn}(T_{di}) = -1$.

The procedures of simplified SVPWM algorithm for three-level inverters are as follows:

1. Specify three phase desired voltages.

2. Each phase voltage is scaled by reference voltage $\frac{V_{dc}}{4}$, then obtain modulation implicit functions of SPWM v_{si}.

3. Compare the amplitude of three phase voltages, find out v_{max} and v_{min}, then calculate zero voltage vector equation v_z.

4. Calculate $T_{di} = T_s \frac{v_{svi}}{2}$, obtain modulation implicit functions of SVPWM.

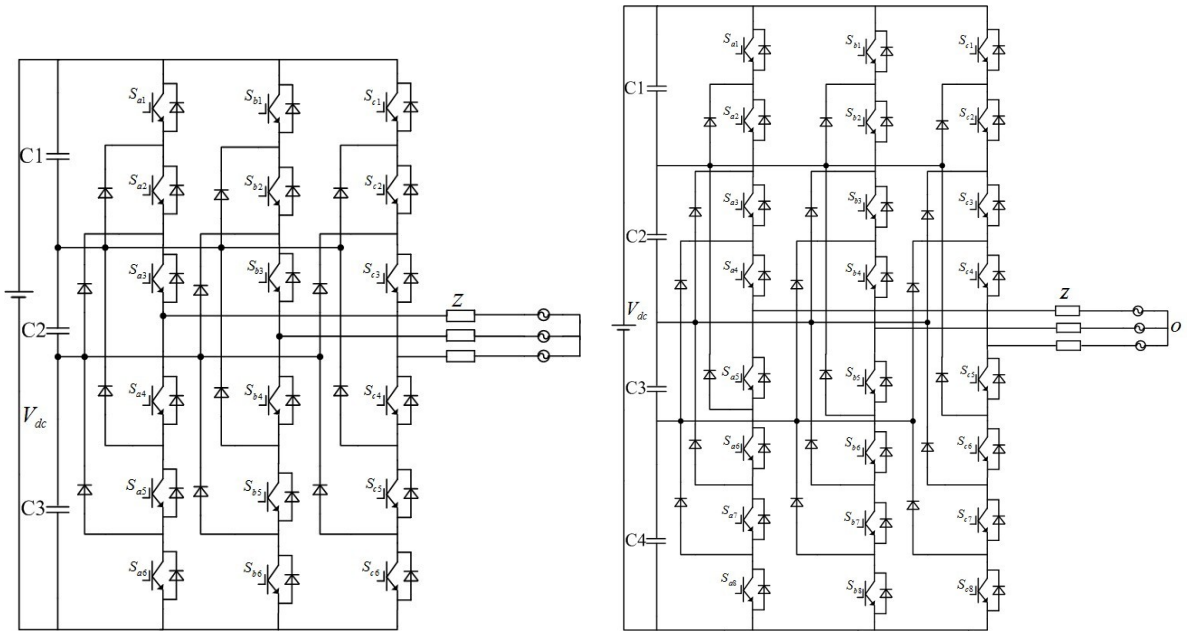
5. Judge the sign of T_{di}, make duration of P states to be T_{di} and duration of O states to be $T_s - T_{di}$ when $\text{sgn}(T_{di}) = 1$, make duration of N states to be $||T_{di}||$ and duration of O states to be $T_s + T_{di}$ when $\text{sgn}(T_{di}) = -1$.

6. Compare with the carrier triangular waveform; produce 12 switching pulses in one period of switching time.

2.2.3 A simplified and unified SVPWM algorithm for multi-level inverter

The traditional SVPWM method for two-level inverter is not very difficult to implement. However, it becomes more and more complex and difficult to realize as the level number of the inverter increases. As the simplified SVPWM algorithms for two-level and three-level inverter are deduced, the simplified and unified SVPWM algorithm for multi-level (m $\geq$ 3) diode clamped VSI (DCVSI) can be derived in the same way. A simplified and unified SVPWM algorithm for multi-level inverter can be drawn from the modulation implicit functions of SVPWM. The algorithm uses the instantaneous values of three phase reference voltages, calculates modulation implicit functions of SVPWM, and compares with carrier triangular waveform, finally calculates actual gating time for each inverter leg. It doesn't need coordinate transformations, trigonometric calculations, and sector number identification. The simplified and unified SVPWM algorithm for multi-level inverter can be composed of

odd-level inverter and even-level inverter cases [10][35][36]. Figure 2.16 shows the topologies of four-level and five-level VSI.



(a) Four-level inverter (b) Five-level inverter

Figure 2.14: The topology of multi-level inverters

1) A simplified SVPWM algorithm for odd-level inverter A simplified SVPWM algorithm for odd-level inverter is similar to the algorithm for three-level inverter. Given the multi-level number is m, switching signals for m-level inverter are shown in Figure 2.15 Each phase voltage is scaled by reference voltage $\frac{V_{dc}}{2(m-1)}$, which is modulation implicit function of SPWM. The modulation implicit functions for SVPWM are obtained by the equation (2.41). In the equation, the zero voltage vector equation for multi-level inverter is as follows:

$$v_z = m - 1 - (2m - 2)k - kv_{min} - (1 - k)v_{max},\ 0 \leq k \leq 1 \tag{2.43}$$

From Figure 2.15, pulse widths of SVPWM are given by:

$$\begin{cases} T_{di} &= \frac{T_s}{2}[v_{svi} - (n-3)],\ n-3 \leq v_{svi} \leq n-1 \\ T_{di} &= \frac{T_s}{2}[v_{svi} + (n-3)],\ 1-n \leq v_{svi} \leq 3-n \end{cases} \tag{2.44}$$

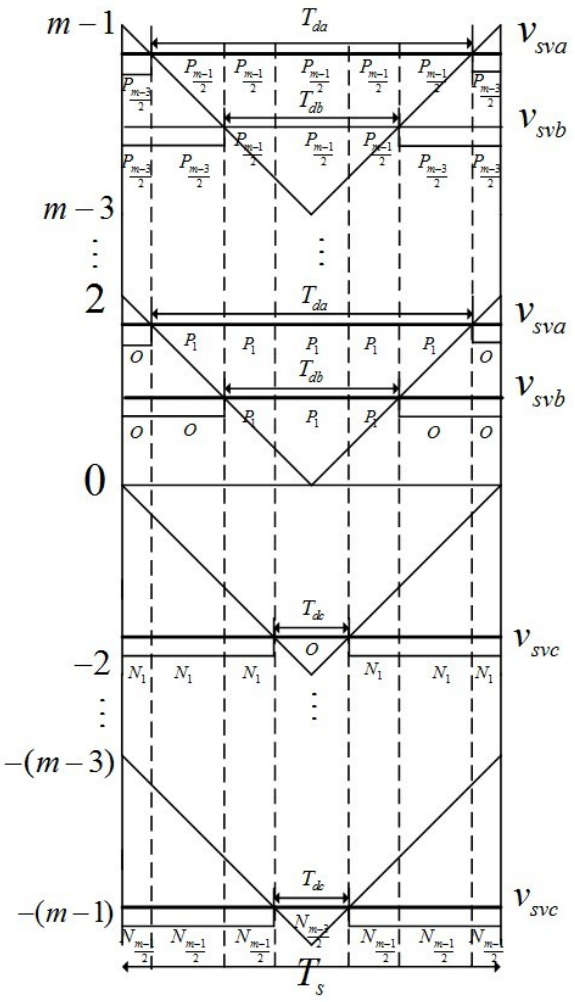


Figure 2.15: One period of PWM switching signals for odd-level inverter

where $3 \leq n \leq m$, n is an odd number, and $i \in (a, b, c)$.

In Figure 2.14, pulse widths of SVPWM can be compared with corresponding carrier triangular waveform to obtain the respective power switch states. If the modulation implicit function v_{svi} lies in [0, 2], then power switches are at states P_1 or O; if v_{svi} lies in between $m-3$ and $m-1$, then power switches are at states $P_{\frac{m-1}{2}}$ or $P_{\frac{m-3}{2}}$; if v_{svi} lies in between 0 and -2, then power switches are at states N_1 or O; if v_{svi} lies in between $-(m-3)$ and $-(m-1)$, then power switches are at states $N_{\frac{m-1}{2}}$ or $N_{\frac{m-3}{2}}$. Similarly, in other areas, power switches will be at the corresponding states.

2) A simplified SVPWM algorithm for even-level inverter A simplified SVPWM algorithm for even-level inverter is similar to the algorithm for two-level inverter. Given the multi-level number is m, switching signals for m-level inverter are shown in Figure 2.16. Each phase voltage is scaled by reference voltage $\frac{V_{dc}}{2(m-1)}$ is the modulation implicit function

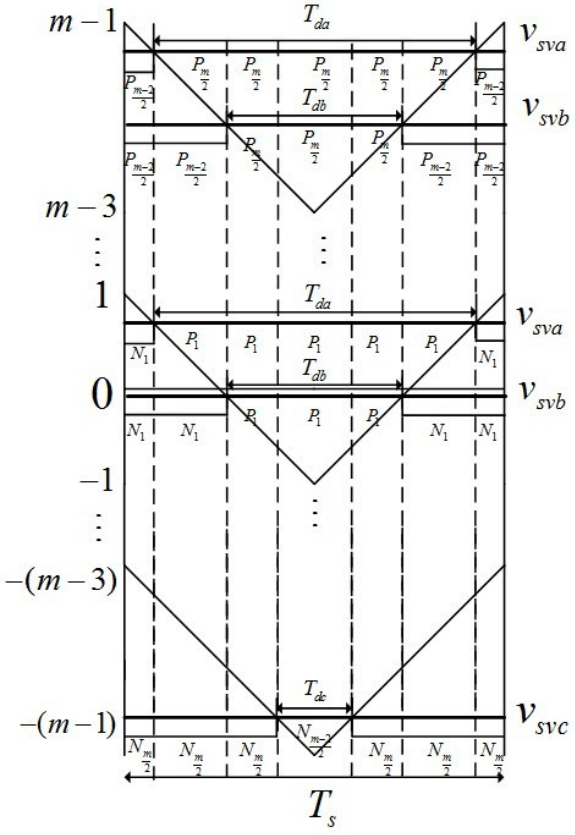


Figure 2.16: One period of PWM switching signals for even-level inverter

of SPWM. The modulation implicit functions of SVPWM are still obtained by equations (2.41) and (2.43). But from Figure 2.16, the pulse widths are given by:

$$\begin{cases} T_{di} &= \frac{T_s}{2}[v_{svi} - (n-3)], \ n-3 \le v_{svi} \le n-1 \\ T_{di} &= \frac{T_s}{2}(v_{svi}+1), \qquad -1 \le v_{svi} \le 1 \\ T_{di} &= \frac{T_s}{2}[v_{svi} + (n-3)], \ 1-n \le v_{svi} \le 3-n \end{cases} \tag{2.45}$$

where $4 \le n \le m$, n is an even number, and $i \in (a, b, c)$.

In Figure 2.16, pulse widths can be compared with corresponding carrier triangular waveform to obtain the respective power switch states. If the modulation implicit function $v_{svi} \in [-1, 1]$, then power switches are at states P_1 or N_1; if $v_{svi} \in [-(m-3), -(m-1)]$, then power switches are at states $N_{\frac{m}{2}}$ or $N_{\frac{m-2}{2}}$; if $v_{svi} \in [m-3, m-1]$, then power switches are at states $P_{\frac{m}{2}}$ or $P_{\frac{m-2}{2}}$. Similarly, in other areas, power switches will be at the corresponding states.

3) Realization of simplified and unified SVPWM algorithm for multi-level inverter The magnitudes of three phase reference voltages may change over time and switching states can be resolved at any given moment in the same way. The procedure of simplified and unified SVPWM algorithm for multi-level inverter is as follows:

1. Specify three phase desired voltages.

2. Each phase voltage is scaled by reference voltage $\frac{V_{dc}}{2(m-1)}$, then obtain modulation implicit function of SPWM v_{si}.

3. Compare the magnitudes of three phase voltages, find out v_{max} and v_{min}, then calculate zero voltage vector equation v_z.

4. Calculate the modulation implicit functions of SVPWM.

5. Determine odd-level inverter or even-level inverter.

6. Calculate pulse width of SVPWM using equations (2.44) and (2.45).

7. Determine the states of power switches, judge the sign of T_{di}, make duration of upper states to be T_{di} and duration of lower states to be $T_s - T_{di}$ when $\text{sgn}(T_{di}) = 1$, make duration of lower states to be $||T_{di}||$ and duration of upper states to be $T_s + T_{di}$ when $\text{sgn}(T_{di}) = -1$.

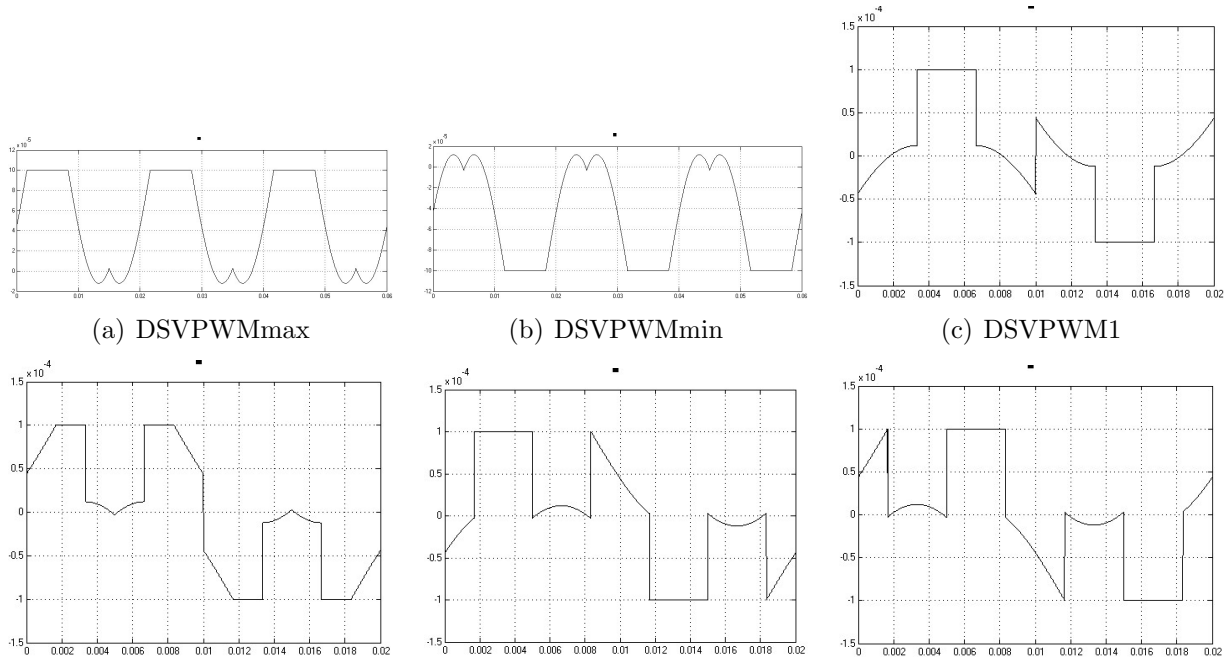
8. Compare with the carrier triangular waveform, produce switching pulses in one period of switching time.

2.3 Discontinuous SVPWM for VSI

The method of clamping input voltage of phase leg to the output bus is called discontinuous pulse width modulation (DPWM). As compared to continuous pulse width modulation (CPWM) strategies, reduction of switching losses is frequently achieved by adoption of DPWM modulation schemes. For a certain amount of fundamental period, the PWM modulation of each phase is halted and the output voltage is clamped to the positive or negative dc-link. Therefore, if the clamping intervals are properly chosen, the switching losses are reduced and better harmonic characteristics are obtained at high modulation index in comparison with CPWM. As a result, DPWM is widely applied to ac drives, active filters, dc converters, three-phase inverters, and have attracted many researchers in the field of power electronics.

In the DPWM methods, zero sequence signals are discontinuous. During each sampling period, one of the phases ceases modulation and the associated phase is clamped to the positive bus or negative bus. Hence, switching losses of the associated inverter legs are eliminated. The continuous SVPWM algorithm employs equal division of zero voltage vector time within a sampling period. This research proposes a new space vector based discontinuous PWM algorithm (DSVPWM), which utilizes the freedom of zero state division that result in a larger number of DSVPWM schemes. For example, consider two basic discontinuous PWMs, as DSVPWMmax and DSVPWMmin. DSVPWMmax is the case where the switching state of one VSI leg is turned on for a 120° period. In this case, $k = 0$ in formula (2.43). Conversely, DSVPWMmin is the case in which the switching state of one VSI leg is turned off during 120° period, and $k = 1$ in formula (2.43). Four other basic discontinuous modulations are DSVPWM0, DSVPWM1, DSVPWM2, and DSVPWM3. These basic DSVPWMs can be derived from DSVPWMmax and DSVPWMmin, depending on the sector. As sectors in Figure 2.10 shows, DSVPWM0 is like DSVPWMmin in sector 1, 3, 5 but is like DSVPWMmax in sector 2, 4, 6. Conversely, DSVPWM2 is like DSVPWMmax in sector 1, 3, 5 but is like DSVPWMmin in sector 2, 4, 6. DSVPWM1 is like DSVPWMmin

from $[30°, 90°]$ but is like DSVPWMmax from $[-30°, 30°]$. Conversely, DSVPWM3 is like DSVPWMmax from $[30°, 90°]$, but is like DSVPWMmin from $[-30°, 30°]$ [37] - [42].



(a) DSVPWMmax (b) DSVPWMmin (c) DSVPWM1

(d) DSVPWM3 (e) DSVPWM0 (f) DSVPWM2

Figure 2.17: Pulse widths of DSVPWMs

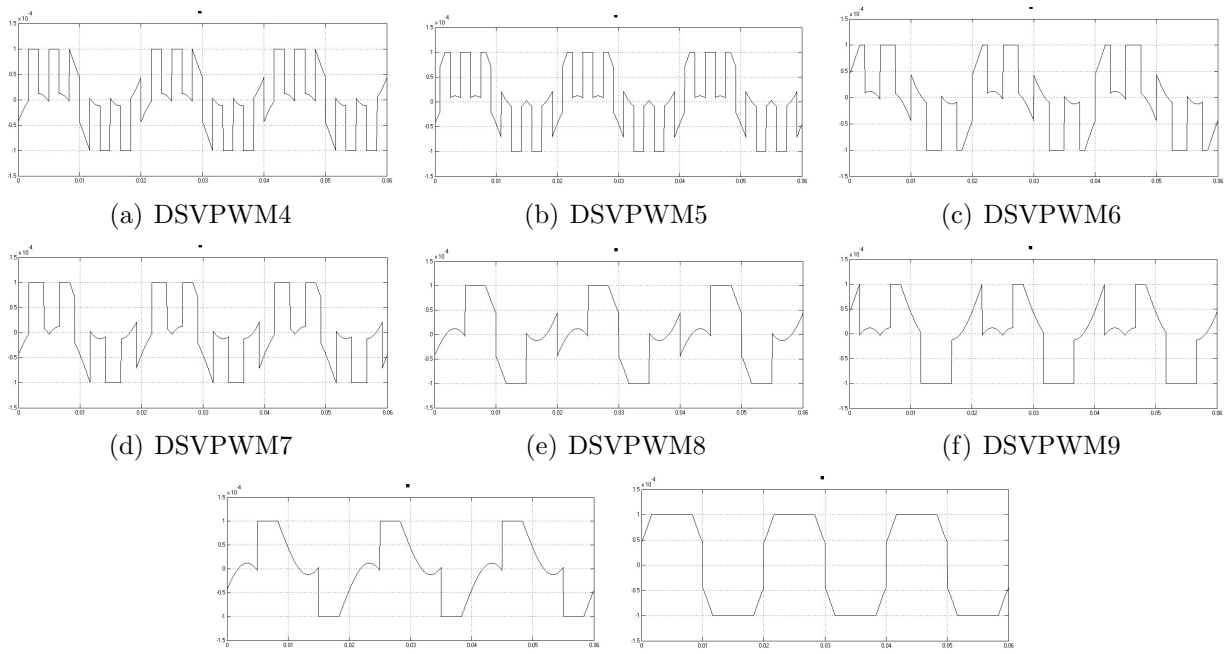
Figure 2.17 shows pulse widths of basic DSVPWMs. Pulse width of DSVPWMmax in Figure 2.17(a) has the unswitching interval of 120° in the positive half cycle of the reference voltage. Pulse width of DSVPWMmin in Figure 2.17(b) has the unswitching interval of 120° in the negative half cycle of the reference voltage. The unswitching interval of 120° in DSVPWM1 is separated into two parts of 60°, respectively appearing in the positive and negative half cycles, as shown in Figure 2.17(c). The unswitching interval of DSVPWM3 in Figure 2.17(d) is composed of four parts, two zero-crossing points and two peak points. DSVPWM0 in Figure 2.17(e) leads 30° over DSVPWM1, while DSVPWM2 in Figure 2.17(f) lags 30° behind DSVPWM1.

Exploring different locations of discontinuous modulation sectors in the positive and negative half cycles, eight additional DSVPWMs are proposed in this paper. DSVPWMmin and DSVPWMmax appear in turn every 60° for DSVPWM0 - DSVPWM3. DSVPWMmin

and DSVPWMmax appear in turn every 30° for DSVPWM4 and 5. DSVPWM4 is like DSVPWMmax from $[0°, 30°]$ and is like DSVPWMmin from $[30°, 60°]$, and DSVPWM5 is like DSVPWMmax from $[-15°, 15°]$ and is like DSVPWMmin from $[15°, 45°]$. DSVPWMmin and DSVPWMmax appear in turn every 45° for DSVPWM6 and 7. DSVPWM6 is like DSVPWMmax from $[0°, 45°]$ and is like DSVPWMmin from $[45°, 90°]$, and DSVPWM7 is like DSVPWMmax from $[30°, 75°]$ and is like DSVPWMmin from $[-15°, 30°]$. DSVPWMmin and DSVPWMmax appear in turn every 90° for DSVPWM8 and 9. DSVPWM8 is like DSVPWMmax from $[0°, 90°]$ and is like DSVPWMmin from $[90°, 180°]$, and DSVPWM9 is like DSVPWMmax from $[30°, 120°]$ and is like DSVPWMmin from $[120°, 210°]$. DSVPWMmin and DSVPWMmax appear in turn every 180° for DSVPWM10 and 11. DSVPWM10 is like DSVPWMmax from $[0°, 180°]$ and is like DSVPWMmin from $[180°, 360°]$, and DSVPWM11 is like DSVPWMmax from $[-90°, 90°]$ and is like DSVPWMmin from $[90°, 270°]$. According to the different locations of discontinuous modulation sectors and the different degree cycles, there still exist many DSVPWMs. Through the use of carrier-based PWM and simplified SVPWM algorithm, DSVPWMs can be easily obtained and implemented in a digital device. The pulse widths of DSVPWM4 to DSVPWM11 are illustrated in Figure 2.18 [11].

2.4 Overmodulation methods for VSI

Several PWM methods have been defined and tested in the undermodulation or linear region. However, operation in the overmodulation region, despite introduced low-order ac-voltage and current harmonics, is also important in many applications to exploit the full dc-link voltage. Typical applications are motion control systems, industrial drives, and high-power ac traction equipment. An overmodulation strategy of SVPWM with modulation factor extending from 0.9069 to near unity is essential if the drive is required to operate at extended speed including the field-weakening region in vector control with higher torque and power characteristics. To take full advantage of the dc bus voltage, several overmodulation techniques [43] - [53] are investigated and studied by many researchers.



(a) DSVPWM4 (b) DSVPWM5 (c) DSVPWM6

(d) DSVPWM7 (e) DSVPWM8 (f) DSVPWM9

(g) DSVPWM10 (h) DSVPWM11

Figure 2.18: Pulse widths of additional eight DSVPWMs (T_{da})

The modulation index (MI) is defined as follows:

$$MI = \frac{||\vec{v_{ref}}||}{2V_{dc}/\pi} \tag{2.46}$$

where $||\vec{v_{ref}}||$ is the amplitude of reference voltage vector, V_{dc} is dc-link voltage, and $\frac{2V_{dc}}{\pi}$ is the fundamental amplitude of six-step waveform.

As Figure 2.19 shows, the six-step mode has the maximum available output, and $0 \leq MI \leq 1$. In the linear modulation (MI$\leq$0.9069), there is $T_1 + T_2 \leq T_s$ and $T_z = T_s - T_1 - T_2$. Here T_1 and T_2 are applying time of two effective voltage vectors, T_z is applying time of zero voltage vector, and T_s is one switching period. When MI=0.9069, then $T_z = 0$ and the trajectory of reference voltage is an inscribed circle on the vector diagram, which is the maximum limit of linear modulation. When $MI > 0.9069$, $T_z < 0$ and the reference voltage vector exceeds the boundary of vector diagram and no effective vectors can synthesize reference voltage vector, which causes distortion of the actual output voltage.

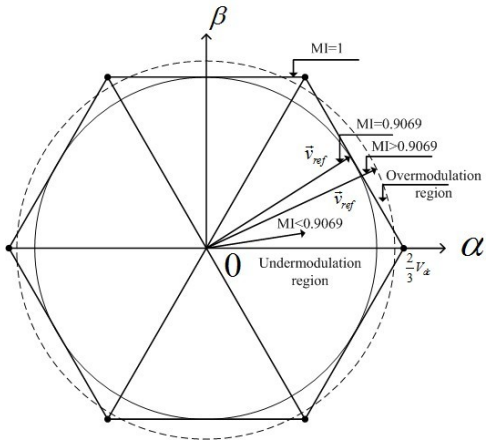


Figure 2.19: Modulation area of voltage space vector diagram (multi-level voltage vectors can also be applied)

Using overmodulation technique, the fundamental component of output voltage can track the desired voltage. Six-step mode corresponds to maximum MI. The key point of SVPWM overmodulation is to find an adequate modification method to modify reference voltage vector. Different modification method corresponds to different overmodulation method. The overmodulation method is composed of two-mode overmodulation and single-mode overmodulation. Several overmodulation methods are proposed by many researchers citeHoltz40[49][53]. In the following sections, according to the previous knowledge, two modified two-mode overmodulation techniques and two modified single-mode overmodulation techniques are proposed and investigated. From Figure 2.19, we can see that the vector diagram is divided into six identical sectors. Since the process is identical when the reference voltage vector locates in different sector, only sector I is considered here.

2.4.1 Two-mode overmodulation technique for VSI

Two-mode overmodulation is divided into mode I ($MI \in [0.9069, 0.9514]$) and mode II ($MI \in [0.9514, 1]$). Joachim Holtz and other researchers proposed and investigated two-mode overmodulation strategy [45][49][53]. Reference [45] proposes a two-mode overmodulation strategy. Mode I is not changed, and detailed description is as follows. In mode I, only amplitude of reference voltage vector is modified, and phase angle of reference voltage vector

is not modified. The following description is based on Figure 2.20. Assuming the amplitude of reference voltage vector is γ, and the phase angle between reference voltage vector and α axes is θ. In the overmodulation technique, reference vector γ becomes $\gamma^{'}$ according to MI, and angle θ equals to $\theta^{'}$. The equations are as follows [54]:

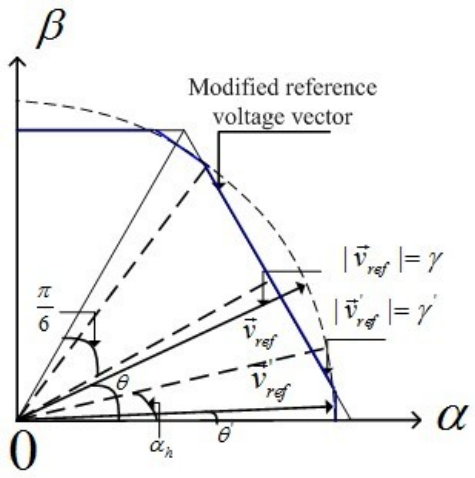


Figure 2.20: Two-mode overmodulation strategy (mode I)

$$\begin{cases} \gamma^{'} = \frac{V_{dc}}{\sqrt{3}\cos(\frac{\pi}{6}-\alpha_h)} & 0 \le \theta \le \alpha_h \\ \gamma^{'} = \frac{V_{dc}}{\sqrt{3}\cos(\frac{\pi}{6}-\theta')} & \alpha_h \le \theta \le \frac{\pi}{3}-\alpha_h \\ \gamma^{'} = \frac{V_{dc}}{\sqrt{3}\cos(\frac{\pi}{6}-\alpha_h)} & \frac{\pi}{3}-\alpha_h \le \theta \le \frac{\pi}{3} \end{cases} \tag{2.47}$$

where, α_h denotes the angle measured from the vertex to the intersection of the modified voltage vector trajectory with the boundary of vector diagram, $0 \le \alpha_h \le \frac{\pi}{6}$.

Because the modification of reference voltage vector is the same in all six sectors, formula (2.47) forms an example of modification of reference voltage vector for each sector. Selecting correct value of $\gamma^{'}$ can make the fundamental component of output voltage track the reference mi correctly. From the above equations, we can see that $\gamma^{'}$ has a relationship to α_h. Consequently, $\gamma^{'}$ and α_h determine the fundamental component of output voltage and the waveform of output voltage. Therefore, if we know the relationship between $\gamma^{'}$ (or α_h) and mi, then we can modify the value of $\gamma^{'}$ (or α_h) to track the reference mi correctly. When

α_h increases from 0 to $\frac{\pi}{6}$, correspondingly, the fundamental component of output voltage increases smoothly from 0.9069 to 0.9514.

The following part analyzes the waveform of output voltage modulated by overmodulation technique to achieve the relationship between γ' (or α_h) and frequency spectrum. Figure 2.21 shows the trajectory of modified voltage vector (bold line at the right half) and its corresponding waveform of modulated phase voltage in time domain (bold line at the left half). The following piecewise expression of phase voltage is obtained by the application of the relationship represented by (2.47). Phase voltage can be divided into four parts and formulated as follows:

$$\begin{cases} f_1 = \frac{V_{dc}\sin\phi'}{\sqrt{3}\cos(\frac{\pi}{6}-\alpha_h)} & 0 \le \phi \le \alpha_h \\ f_2 = \frac{V_{dc}\sin\phi'}{\sqrt{3}\cos(\frac{\pi}{6}-\phi')} & \alpha_h \le \phi \le \frac{\pi}{3}-\alpha_h \\ f_3 = \frac{V_{dc}\sin\phi'}{\sqrt{3}\cos(\frac{\pi}{6}-\alpha_h)} & \frac{\pi}{3}-\alpha_h \le \phi \le \frac{\pi}{3}+\alpha_h \\ f_4 = \frac{V_{dc}}{\sqrt{3}} & \frac{\pi}{3}+\alpha_h \le \phi \le \frac{\pi}{2} \end{cases} \tag{2.48}$$

The fundamental component $F(\alpha_h)$ of phase voltage can be expressed as follows:

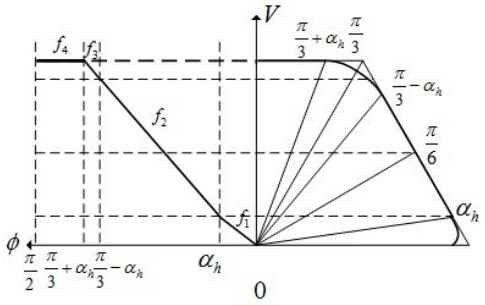


Figure 2.21: Analysis of two-mode overmodulation strategy mode I

$$\begin{cases} F(\alpha_h) = & \frac{4}{\pi}[\int_0^{\alpha_h} f_1(\phi)\sin\phi d\phi + \int_{\alpha_h}^{\frac{\pi}{3}-\alpha_h} f_2(\phi)\sin\phi d\phi \\ & + \int_{\frac{\pi}{3}-\alpha_h}^{\frac{\pi}{3}+\alpha_h} f_3(\phi)\sin\phi d\phi + \int_{\frac{\pi}{3}+\alpha_h}^{\frac{\pi}{2}} f_4(\phi)\sin\phi d\phi] \end{cases} \tag{2.49}$$

where $F(\alpha_h)$ is Fourier transform of phase voltage. Considering formula (2.46), the relationship between MI and α_h can be expressed as follows:

$$MI = \frac{\pi}{2V_{dc}} F(\alpha_h) \tag{2.50}$$

From the above equations, we can draw the relationship between MI and α_h, as Figure 2.22 shows. The output voltage is modulated by the modified reference voltage vector, and its fundamental component can precisely trace the instructive voltage given by MI. In Figure 2.22, $0 \leq \alpha_h \leq \frac{\pi}{6}$.

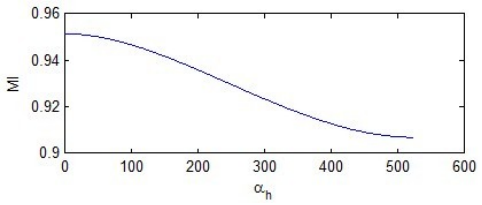


Figure 2.22: Relationship between MI and α_h

The following description investigates modified two-mode overmodulation technique-mode II according to the study of previous work.

1) Mode II-method 1 The following description is based on Figure 2.23. Assuming the amplitude of reference voltage vector is γ, and the phase angle between reference voltage vector and α axes is θ. In the overmodulation technique, reference vector γ becomes γ' according to MI, and angle θ becomes θ'. The equations are as follows:

$$\begin{cases} \theta' = 0 & 0 \leq \theta \leq \alpha_h \\ \theta' = \beta + (\frac{\pi}{6} - \beta)\frac{\theta - \alpha_h}{\frac{\pi}{6} - \alpha_h} & \alpha_h \leq \theta \leq \frac{\pi}{3} - \alpha_h \\ \theta' = \frac{\pi}{3} & \frac{\pi}{3} - \alpha_h \leq \theta \leq \frac{\pi}{3} \end{cases} \tag{2.51}$$

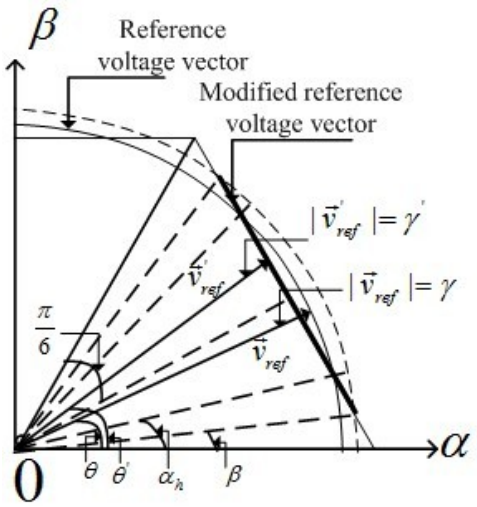


Figure 2.23: Two-mode overmodulation strategy-method 1

where, α_h denotes the angle measured from the vertex to the intersection of the modified voltage vector trajectory with the boundary of vector diagram, $0 \leq \alpha_h \leq \frac{\pi}{6}$, and β is the equation of α_h.

As Figure 2.24 shows, β have several solutions of α_h. Choosing one of the solutions $\beta = \frac{\alpha_h^3}{(\frac{\pi}{6})^2}$ as an example, the relationship between $\theta^{'}$ and $\gamma^{'}$ is as follows:

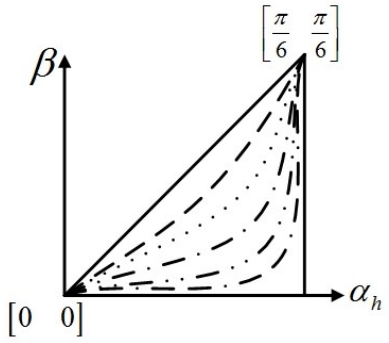


Figure 2.24: The relationship between β and α_h

$$\gamma^{'} = \frac{V_{dc}}{\sqrt{3}\cos(\frac{\pi}{6} - \theta^{'})} \tag{2.52}$$

Because the modification of reference voltage vector is the same in all six sectors, formula (2.51) and (2.52) form an example of modification of reference voltage vector for each sector.

Selecting correct value of $\gamma^{'}$ can make the fundamental component of output voltage track the reference mi correctly. From the above equations, we can see that $\gamma^{'}$ have the relationship to α_h, consequently, $\gamma^{'}$ and α_h determine the fundamental component of output voltage and the waveform of output voltage. Therefore, if we know the relationship between $\gamma^{'}$ (or α_h) and mi, then we can modify the value of $\gamma^{'}$ (or α_h) to track the reference mi correctly. When α_h increases from 0 to $\frac{\pi}{6}$, correspondingly, the fundamental component of output voltage increases smoothly from 0.9514 to 1.

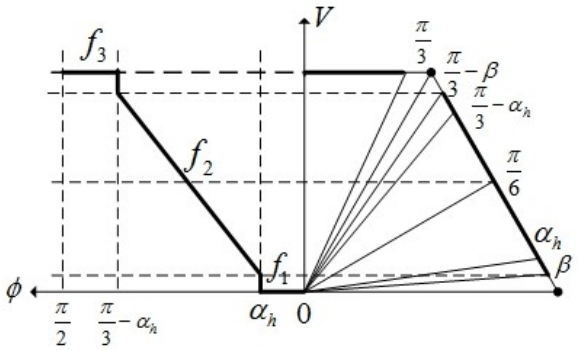


Figure 2.25: Modified vector and its corresponding waveform of modulated phase voltage

The following part analyzes the waveform of output voltage modulated by overmodulation technique to achieve the relationship between $\gamma^{'}$ (or α_h) and frequency spectrum. Figure 2.25 shows the trajectory of modified voltage vector (bold line at the right half) and its corresponding waveform of modulated phase voltage in time domain (bold line at the left half). The following piecewise expression of phase voltage is obtained by the application of the relationship represented by (2.51) and (2.52). Phase voltage can be divided into three parts and formulated as follows:

$$\begin{cases} f_1 = 0 & 0 \le \phi \le \alpha_h \\ f_2 = \frac{V_{dc}\sin\phi^{'}}{\sqrt{3}\cos(\frac{\pi}{6}-\phi^{'})} & \alpha_h \le \phi \le \frac{\pi}{3} - \alpha_h \\ f_3 = \frac{V_{dc}}{\sqrt{3}} & \frac{\pi}{3} - \alpha_h \le \phi \le \frac{\pi}{2} \end{cases} \tag{2.53}$$

The fundamental component $F(\alpha_h)$ of phase voltage can be expressed as follows:

$$\begin{cases} F(\alpha_h) = & \frac{4}{\pi}[\int_0^{\alpha_h} f_1(\phi)\sin\phi d\phi + \int_{\alpha_h}^{\frac{\pi}{3}-\alpha_h} f_2(\phi)\sin\phi d\phi \\ & + \int_{\frac{\pi}{3}-\alpha_h}^{\frac{\pi}{2}} f_3(\phi)\sin\phi d\phi] \end{cases} \tag{2.54}$$

The relationship between MI and α_h is obtained by formula (2.50). From the above equations, we can draw the relationship between MI and α_h $(0 \leq \alpha_h \leq \frac{\pi}{6})$, as Figure 2.26 shows. The output voltage is modulated by the modified reference voltage vector, and its fundamental component can precisely trace the instructive voltage given by MI.

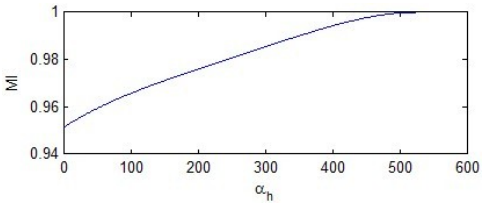


Figure 2.26: Relationship between MI and α_h

2) Mode II-method 2 The following description is based on Figure 2.27. Similar with the method mentioned above, in the overmodulation technique, angle θ becomes θ'. The equations of angle θ' are presented as follows [12]:

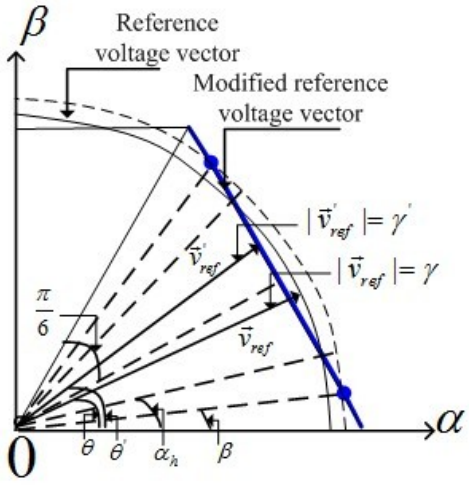


Figure 2.27: Two-mode overmodulation strategy-method 2

$$\begin{cases} \theta' &= 0 & 0 \le \theta \le \beta \\ \theta' &= \beta - \frac{\alpha_h - \theta}{1-\frac{\beta}{\alpha_h}} \frac{\beta}{\alpha_h} & \beta \le \theta \le \alpha_h \\ \theta' &= \beta + (\frac{\pi}{6} - \beta) \frac{\theta - \alpha_h}{\frac{\pi}{6} - \alpha_h} & \alpha_h \le \theta \le \frac{\pi}{3} - \alpha_h \\ \theta' &= \frac{\pi}{3} - \beta + \frac{\theta - (\frac{\pi}{3} - \alpha_h)}{1-\frac{\beta}{\alpha_h}} \frac{\beta}{\alpha_h} & \frac{\pi}{3} - \alpha_h \le \theta \le \frac{\pi}{3} - \beta \\ \theta' &= \frac{\pi}{3} & \frac{\pi}{3} - \beta \le \theta \le \frac{\pi}{3} \end{cases} \tag{2.55}$$

where, α_h denotes the angle measured from the vertex to the intersection of the modified voltage vector trajectory with the boundary of vector diagram, $0 \le \alpha_h \le \frac{\pi}{6}$.

As Figure 2.24 shows, β is the equation of α_h. The equation of $\gamma^{'}$ is obtained by equation (2.52). Figure 2.28 shows the trajectory of modified voltage vector (bold line at the right half) and its corresponding waveform of modulated phase voltage in time domain (bold line at the left half). The following piecewise expression of phase voltage is obtained by the application of the relationship represented by (2.52) and (2.55). Phase voltage can be divided into five parts and formulated as follows:

$$\begin{cases} f_1 &= 0 & 0 \le \phi \le \alpha_h \\ f_2 &= \frac{V_{dc} \sin \phi^{'}}{\sqrt{3} \cos(\frac{\pi}{6} - \phi^{'})} & \beta \le \phi \le \alpha_h \\ f_3 &= \frac{V_{dc} \sin \phi^{'}}{\sqrt{3} \cos(\frac{\pi}{6} - \phi^{'})} & \alpha_h \le \phi \le \frac{\pi}{3} - \alpha_h \\ f_4 &= \frac{V_{dc} \sin \phi^{'}}{\sqrt{3} \cos(\frac{\pi}{6} - \phi^{'})} & \frac{\pi}{3} - \alpha_h \le \phi \le \frac{\pi}{3} - \beta \\ f_5 &= \frac{V_{dc}}{\sqrt{3}} & \frac{\pi}{3} - \beta \le \phi \le \frac{\pi}{2} \end{cases} \tag{2.56}$$

The fundamental component $F(\alpha_h)$ of phase voltage can be expressed as follows:

$$\begin{cases} F(\alpha_h) = & \frac{4}{\pi}[\int_0^{\beta} f_1(\phi) \sin \phi d\phi + \int_{\beta}^{\alpha_h} f_2(\phi) \sin \phi d\phi \\ & + \int_{\alpha_h}^{\frac{\pi}{3} - \alpha_h} f_3(\phi) \sin \phi d\phi + \int_{\frac{\pi}{3} - \alpha_h}^{\frac{\pi}{3} - \beta} f_4(\phi) \sin \phi d\phi \\ & + \int_{\frac{\pi}{3} - \beta}^{\frac{\pi}{2}} f_5(\phi) \sin \phi d\phi] \end{cases} \tag{2.57}$$

The relationship between MI and α_h can be obtained by formula (2.50). From the above equations, we can draw the relationship between MI and α_h ($0 \le \alpha_h \le \frac{\pi}{6}$), as Figure 2.29

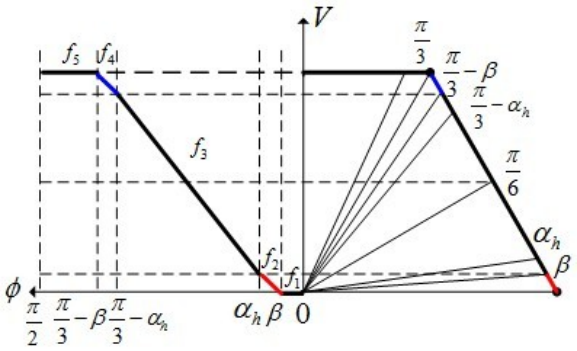


Figure 2.28: Modified vector and its corresponding waveform of modulated phase voltage

shows. The output voltage is modulated by the modified reference voltage vector, and its fundamental component can precisely trace the instructive voltage given by MI.

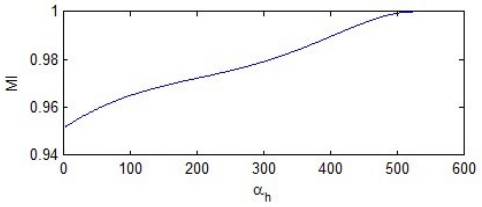


Figure 2.29: Relationship between MI and α_h

2.4.2 Single-mode overmodulation technique for VSI

In the following, two single-mode overmodulation techniques ($MI \in [0.9069, 1]$) are proposed and studied.

1) Method 1 The following description is based on Figure 2.30. Similar with the method mentioned above, in the overmodulation technique, angle θ becomes $\theta^{'}$. The equations of angle $\theta^{'}$ are presented as follows:

$$\begin{cases} \theta^{'} = \theta & 0 \le \theta \le \alpha_h \\ \theta^{'} = \frac{6\alpha_h\theta}{\pi} & \alpha_h \le \theta \le \frac{\pi}{6} \\ \theta^{'} = \frac{\pi}{3} - 2\alpha_h + \frac{6\alpha_h\theta}{\pi} & \frac{\pi}{6} \le \theta \le \frac{\pi}{3} - \alpha_h \\ \theta^{'} = \theta & \frac{\pi}{3} - \alpha_h \le \theta \le \frac{\pi}{3} \end{cases} \tag{2.58}$$

where, α_h denotes the angle measured from the vertex to the intersection of the modified

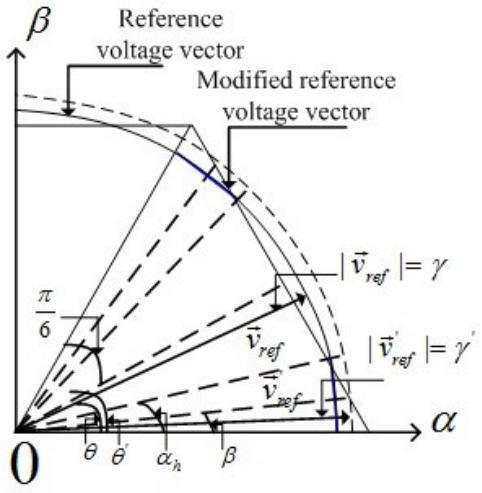


Figure 2.30: Single-mode overmodulation strategy

voltage vector trajectory with the boundary of vector diagram, $0 \leq \alpha_h \leq \frac{\pi}{6}$.

As Figure 2.24 shows, β is the equation of α_h. The equation of γ' is as follows:

$$\gamma' = R \quad R \in [\frac{V_{dc}}{\sqrt{3}}, \frac{2V_{dc}}{3}] \tag{2.59}$$

where, $\alpha_h(R) = \frac{\pi}{6} - \arccos(\frac{V_{dc}}{\sqrt{3}R})$, R is the control parameter.

Figure 2.31 shows the trajectory of modified voltage vector (bold line at the right half) and its corresponding waveform of modulated phase voltage in time domain (bold line at the left half). The following piecewise expression of phase voltage is obtained by the application

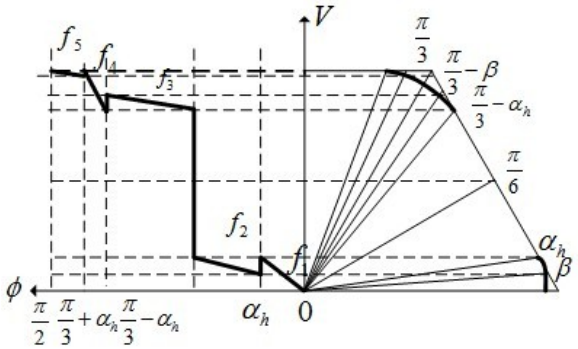


Figure 2.31: Modified vector and its corresponding waveform of modulated phase voltage

of the relationship represented by (2.58) and (2.59). Phase voltage can be divided into five parts and formulated as follows:

$$\begin{cases} f_1 = \frac{V_{dc}\sin\phi'}{\sqrt{3}\cos(\frac{\pi}{6}-\alpha_h)} & 0 \le \phi \le \alpha_h \\ f_2 = \frac{V_{dc}\sin\phi'}{\sqrt{3}\cos(\frac{\pi}{6}-\alpha_h)} & \alpha_h \le \phi \le \frac{\pi}{6} \\ f_3 = \frac{V_{dc}\sin\phi'}{\sqrt{3}\cos(\frac{\pi}{6}-\alpha_h)} & \frac{\pi}{6} \le \phi \le \frac{\pi}{3}-\alpha_h \\ f_4 = \frac{V_{dc}\sin\phi'}{\sqrt{3}\cos(\frac{\pi}{6}-\alpha_h)} & \frac{\pi}{3}-\alpha_h \le \phi \le \frac{\pi}{3}+\alpha_h \\ f_5 = \frac{V_{dc}\sin\phi'}{\sqrt{3}\cos(\frac{\pi}{6}-\alpha_h)} & \frac{\pi}{3}+\alpha_h \le \phi \le \frac{\pi}{2} \end{cases} \tag{2.60}$$

The fundamental component $F(\alpha_h)$ of phase voltage can be expressed as follows:

$$\begin{cases} F(\alpha_h) = & \frac{4}{\pi}[\int_0^{\alpha_h} f_1(\phi)\sin\phi d\phi + \int_{\alpha_h}^{\frac{\pi}{6}} f_2(\phi)\sin\phi d\phi \\ & + \int_{\frac{\pi}{6}}^{\frac{\pi}{3}-\alpha_h} f_3(\phi)\sin\phi d\phi] + \int_{\frac{\pi}{3}-\alpha_h}^{\frac{\pi}{3}+\alpha_h} f_4(\phi)\sin\phi d\phi] \\ & + \int_{\frac{\pi}{3}+\alpha_h}^{\frac{\pi}{2}} f_5(\phi)\sin\phi d\phi] \end{cases} \tag{2.61}$$

From the above equations, we can draw the relationship between MI and α_h $0 \le \alpha_h \le \frac{\pi}{6}$, as Figure 2.32 shows. The output voltage is modulated by the modified reference voltage vector, and its fundamental component can precisely trace the instructive voltage given by MI.

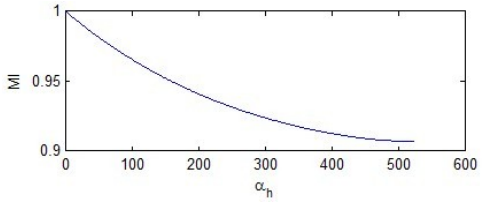


Figure 2.32: Relationship between MI and α_h

2) Method 2 The following description is based on Figure 2.33. Similar with the method mentioned above, in the overmodulation technique, angle θ becomes θ'. The equations of angle θ' are presented as follows [12]:

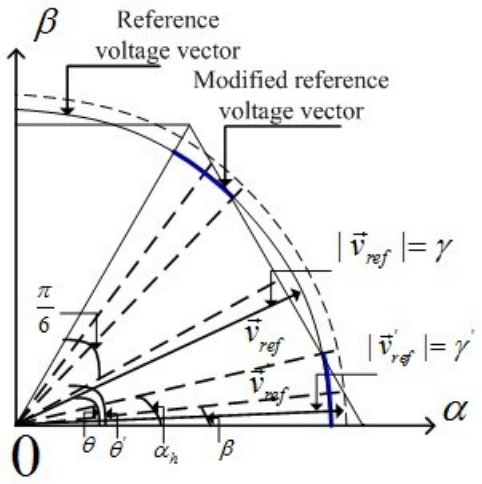


Figure 2.33: Single-mode overmodulation strategy

$$\begin{cases} \theta' = \theta & 0 \le \theta \le \beta \\ \theta' = \alpha_h - (\alpha_h - \beta)\frac{\frac{\pi}{6}-\theta}{\frac{\pi}{6}-\beta} & \beta \le \theta \le \frac{\pi}{6} \\ \theta' = \frac{\pi}{3} - \alpha_h + (\alpha_h - \beta)\frac{\theta-\frac{\pi}{6}}{\frac{\pi}{6}-\beta} & \frac{\pi}{6} \le \theta \le \frac{\pi}{3} - \beta \\ \theta' = \theta & \frac{\pi}{3} - \beta \le \theta \le \frac{\pi}{3} \end{cases} \tag{2.62}$$

where, α_h denotes the angle measured from the vertex to the intersection of the modified voltage vector trajectory with the boundary of vector diagram, $0 \le \alpha_h \le \frac{\pi}{6}$.

As Figure 2.24 shows, β is the equation of α_h. The equation of γ' is obtained by equation (2.59). Figure 2.34 shows the trajectory of modified voltage vector (bold line at the right half) and its corresponding waveform of modulated phase voltage in time domain (bold line at the left half). The following piecewise expression of phase voltage is obtained by the application of the relationship represented by (2.59) and (2.62). Phase voltage can

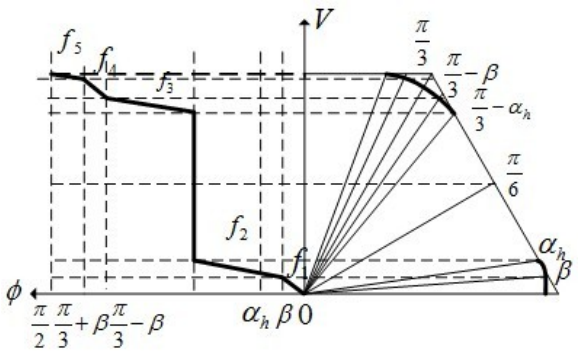


Figure 2.34: Modified vector and its corresponding waveform of modulated phase voltage

be divided into five parts and formulated as follows:

$$\begin{cases} f_1 = \frac{V_{dc}\sin\phi'}{\sqrt{3}\cos(\frac{\pi}{6}-\alpha_h)} & 0 \le \phi \le \beta \\ f_2 = \frac{V_{dc}\sin\phi'}{\sqrt{3}\cos(\frac{\pi}{6}-\alpha_h)} & \beta \le \phi \le \frac{\pi}{6} \\ f_3 = \frac{V_{dc}\sin\phi'}{\sqrt{3}\cos(\frac{\pi}{6}-\alpha_h)} & \frac{\pi}{6} \le \phi \le \frac{\pi}{3}-\beta \\ f_4 = \frac{V_{dc}\sin\phi'}{\sqrt{3}\cos(\frac{\pi}{6}-\alpha_h)} & \frac{\pi}{3}-\beta \le \phi \le \frac{\pi}{3}+\beta \\ f_5 = \frac{V_{dc}\sin\phi'}{\sqrt{3}\cos(\frac{\pi}{6}-\alpha_h)} & \frac{\pi}{3}+\beta \le \phi \le \frac{\pi}{2} \end{cases} \tag{2.63}$$

The fundamental component $F(\alpha_h)$ of phase voltage can be expressed as follows:

$$\begin{cases} F(\alpha_h) = & \frac{4}{\pi}[\int_0^{\beta} f_1(\phi)\sin\phi d\phi + \int_{\beta}^{\frac{\pi}{6}} f_2(\phi)\sin\phi d\phi \\ & + \int_{\frac{\pi}{6}}^{\frac{\pi}{3}-\beta} f_3(\phi)\sin\phi d\phi] + \int_{\frac{\pi}{3}-\beta}^{\frac{\pi}{3}+\beta} f_4(\phi)\sin\phi d\phi] \\ & + \int_{\frac{\pi}{3}+\beta}^{\frac{\pi}{2}} f_5(\phi)\sin\phi d\phi] \end{cases} \tag{2.64}$$

From the above equations, we can draw the relationship between MI and α_h, as Figure 2.35 shows. The output voltage is modulated by the modified reference voltage vector, and its fundamental component can precisely trace the instructive voltage given by MI.

In this chapter, a simplified and unified SVPWM algorithm for multi-level diode clamped VSI is proposed and studied. A discontinuous modulation method is studied based on the simplified SVPWM algorithm. And two two-mode overmodulation and two-single mode

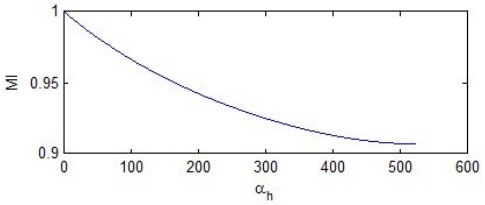


Figure 2.35: Relationship between MI and α_h

overmodulation is proposed and studied. In the following chapter, control methods for VSI are researched.

Chapter 3

Control methods for VSI

In this chapter, analysis and compensation of dead-time effect for multi-level VSI, dc-link capacitor voltage control strategy, unbalanced three-phase voltage control, and energy feedback control methods are presented. New contributions are: (a) A detailed analysis and uniform compensation of dead-time effect in three-phase multi-level VSI is described [13]. (b) A simplified control strategy to balance dc-link capacitor voltage for multi-level inverter based on DSVPWM is proposed [14]. (c) Control scheme of unbalanced three-phase voltage based on DSVPWM is described. (d) Phase and amplitude control method as energy feedback control method is studied.

3.1 Analysis and compensation of dead-time effect

In practical applications, switching devices have finite (non-zero) turn-on and turn-off times. To prevent a short circuit in the dc-link, a switching delay time is inserted into PWM signals. Finite switching times dictate that a blanking time be inserted in a phase leg when one device is being turned off and complementary device is being turned on, to prevent a short circuit or shoot-through condition. However, the dead time introduces a voltage error at the inverter phase terminal. This error is dependent on the polarity of phase current. The voltage error increases output voltage harmonic components and decreases control performance. Therefore, dead time compensation is desirable.

3.1.1 Analysis of dead-time effect

1) Two-level inverter During the dead-time interval, the output voltage is not controlled by power switches, but is related to the output current direction. Turn-on and turn-off of a

IGBT requires a certain period of time, and furthermore IGBTs and anti-parallel diodes have operating voltages. These factors lead to some errors in the output voltages and currents. There exists IGBT voltage drop V_s and freewheeling diode voltage drop V_d when current flows to the voltage source. The two-level three-phase VSI PWM system is shown in Figure 1.1. Define current flowing to the voltage source as positive polarity. The dead-time effect on the output voltage can best be examined from one phase of the PWM inverter, as illustrated in Figure 3.1.

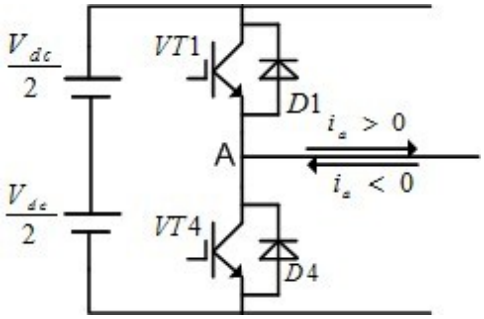


Figure 3.1: One pair of IGBT topology

Taking one phase of an IGBT bridge as an example, one can analyze the effect of dead time and turn-on turn-off time of devices on the output voltage. Examine the power device switching sequence when $VT1$ is turning off and $VT4$ is turning on, or $VT4$ is turning off and $VT1$ is turning on. There exists a moment when both power devices cease to conduct. Consider two possible commutation sequences when the current i_a is positive.

In the first sequence, $VT1$ is turning off and $VT4$ is turning on. In the dead-time period, the clamping diode $D4$ carries the current and the output state is O, so there is no voltage difference between the first state and the end state. In the second sequence, $VT1$ is turning on and $VT4$ is turning off. In the dead-time period, the clamping diode $D4$ carries the current and the output state is O. This condition results in a voltage difference between the first state and the end state. Similarly, dead time effects are analyzed when the current i_a is negative. The first sequence results in a voltage difference between the first state and

the end state and the second sequence results no voltage difference between the first state and the end state.

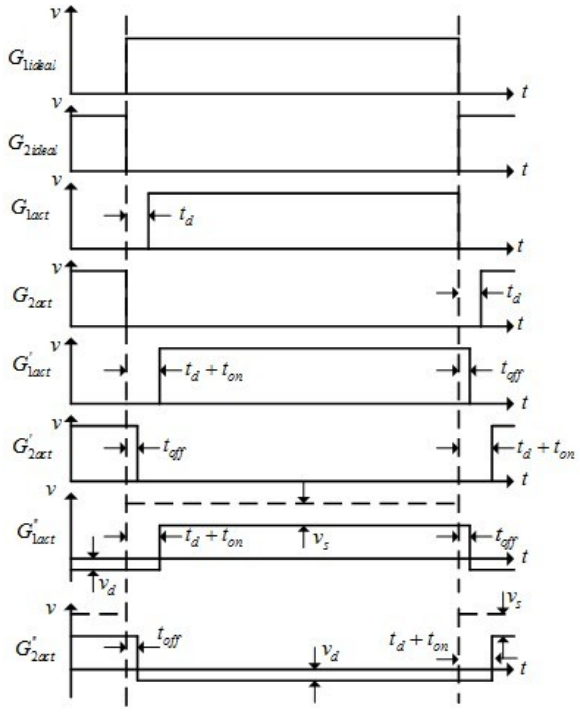


Figure 3.2: One period of PWM with dead time when $i_a > 0$

Figure 3.2 shows the effects of dead-time on hypothetical pulse times for power devices $VT1$ and $VT4$ [55]. In the picture, G_{1ideal}, G_{2ideal} are ideal gate signals of $VT1$, $VT4$, respectively; G_{1act} and G_{2act} are gate signals considering dead time; G'_{1act}, G'_{2act} are gate signals of considering dead time, and turn-on and turn-off time of devices; G''_{1act}, G''_{2act} are gate signals considering dead time, turn-on and turn-off time of devices, and conduction voltage drop of devices. According to the principle of equivalence of volt-second area between reference voltage and compensation voltage, we can deduce the effective deviation time of phase a [56][57] by following formula.

$$T_{DT\_a} = t_{ad} + t_{on} - t_{off} + \frac{MT_sV_s + (1-M)T_sV_d}{V_{dc} + V_d - V_s} \tag{3.1}$$

where t_{ad} is dead time of phase a, t_{on} and t_{off} are turn-on and turn-off time of switches, T_s is switching period, M is duty cycle, and V_{dc} is dc-link voltage, and V_s, V_d are the voltage drops of the switches and diodes, respectively.

When $i_a < 0$, the effective deviation time of phase a is as follows:

$$T_{DT\_a} = t_{ad} + t_{on} - t_{off} + \frac{MT_sV_d + (1-M)T_sV_s}{V_{dc} + V_d - V_s} \tag{3.2}$$

The loss of terminal voltage of phase a over one PWM period is given by:

$$V_{DT\_a} = \frac{T_{DT\_a}}{T_s} V_{dc} \tag{3.3}$$

Voltage losses of phases b and c can be derived in similar fashion. Through the above analysis, we can get the average voltage loss caused by dead time in one PWM period.

$$V_{DT\_j} = \frac{T_{DT\_j}}{T_s} V_{dc}\text{sgn}(i_j) \quad j \in (a,b,c) \tag{3.4}$$

where i_j is output current, and $\text{sgn}(i) = \begin{cases} 1 & i > 0 \\ -1 & i < 0 \end{cases}$.

Therefore, the actual three phase output voltages are as follows:

$$V_j' = V_j - \frac{T_{DT\_j}}{T_s} V_{dc}\text{sgn}(i_j) \quad j \in (a,b,c) \tag{3.5}$$

The disturbance voltage vector, which accounts for all three phases′ voltage drops caused by dead time is given by:

$$\begin{cases} \Delta V &= -\frac{V_{dc}}{T_s}[T_{DT\_a}\text{sgn}(i_a) \\ & \quad + e^{j\frac{2\pi}{3}} T_{DT\_b}\text{sgn}(i_b) + e^{j\frac{4\pi}{3}} T_{DT\_c}\text{sgn}(i_c)] \end{cases} \tag{3.6}$$

Dead time, turn-on turn-off time of devices, and voltage drop of devices are generating disturbance voltage ΔV. This not only changes the size of the output voltage but also changes the phase of output current. Therefore, dead time effect increases harmonic components of output voltage and current, and changes the phase angle between voltage and current.

2) Multi-level inverter The dead-time effect for multi-level inverter is similar to two-level inverter. The three-phase three-level inverter shown in Figure 2.10 [13] is studied as an example. Define current flowing to the voltage source as positive polarity. The dead-time effect on the output voltage can best be examined from one phase of the PWM inverter, as illustrated in Figure 3.3. Examine the power device switching sequence when S_{a1} is turning off and S_{a3} is turning on, or S_{a3} is turning off and S_{a1} is turning on. There exists a moment when both power devices cease to conduct. The dead-time effect also exists when switching the pair S_{a2} and S_{a4}. Consider four possible commutation sequences when the current i_a is positive.

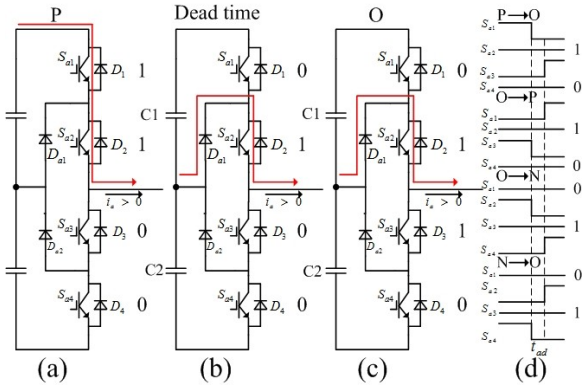


Figure 3.3: Phase leg status during P to O transition: (a) steady state P, (b) dead-time period, (c) steady state O, (d) each switch state during transition

In the first sequence, consider the output state transition from P to O. The four switches′ gate signals at the start and the end are correspondingly 1100 and 0110, as shown in Figure 3.3(a) and Figure 3.3(c). The devices are not ideal, however, so the gate signals cannot directly be changed from 1100 to 0110. Switch S_{a3} needs to remain open (its original state) for a dead time period, so there is a mid-state during the transition, as shown in

Figure 3.3(b). The clamping diode D_{a1} carries the current during the dead-time and the output state is O, so there is no voltage difference between the mid-state and the end state O.

In the second sequence, consider the output state transition from O to P. The four switches$'$ gate signals at the start and the end are correspondingly 0110 and 1100. Switch S_{a1} needs to remain open (its original state) for a dead time period, the clamping diode D_{a1} carries the current and the output state is O. This condition results in a voltage difference between the mid-state and the end state P.

In the third sequence, consider the output state transition from O to N. The four switches$'$ gate signals at the start and the end are correspondingly 0110 and 0011. Switch S_{a4} needs to remain open (its original state) for a dead time period, the freewheeling diode D_4 carries the current and the output state is N, so there is no voltage difference between the mid-state and the end state N.

In the fourth sequence, consider the output state transition from N to O. The four switches$'$ gate signals at the start and the end are correspondingly 0011 and 0110. Switch S_{a2} needs to remain open (its original state) for a dead time period, the freewheeling diode D_4 carries the current and the output state is N. This condition results in a voltage difference between the mid-state and the end state O.

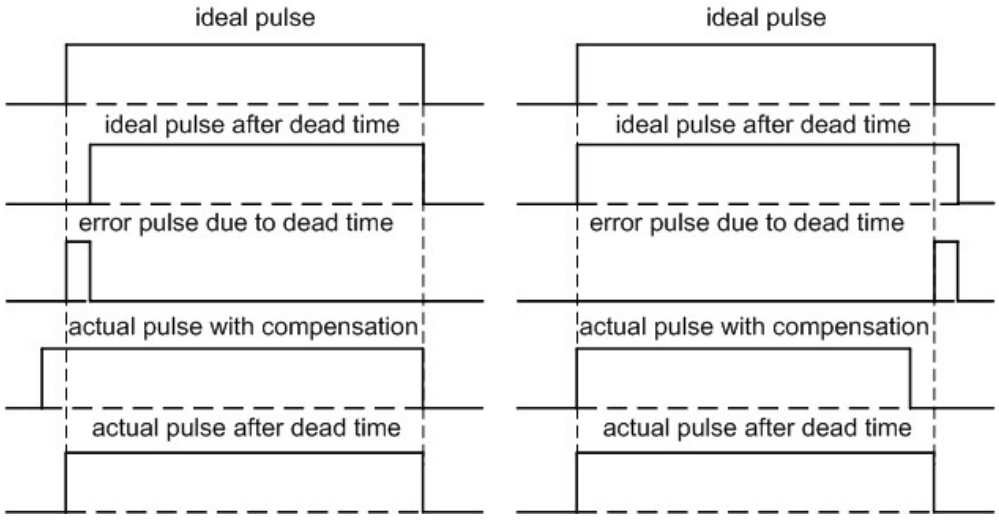
Similar, dead time effects occur when the current i_a is negative. The first condition results in a increase of voltage at the output voltage, the second condition results no voltage loss, the third condition results in a increase of voltage at the output voltage, and the fourth condition results no voltage loss.

The disturbance voltage caused by dead-time is obtained by the equations (3.1) to (3.6). Similarly, we can analyze dead time effects in other m-level DCVSI.

3.1.2 Dead-time compensation method

The pulse time compensation method is first reviewed. Then a voltage compensation approach based on a simplified SVPWM is developed.

1) Pulse time compensation method Pulse time compensation method updates turn-on time of power device at the beginning of PWM cycle and turn-off time of power device at the ending of PWM cycle by software correction. Correction is based on the polarity of output current, and it is independent of operating frequency or carrier frequency [58] - [62].



(a) $i_a > 0$ (b) $i_a < 0$

Figure 3.4: Pulse time compensation

Figure 3.4(a) shows pulse time compensation when $i_a > 0$. Actual pulse width of upper switch is shorter T_{DT} than ideal pulse width and actual pulse width of lower switch is shorter T_{DT} than ideal pulse width. For pulse time compensation, the pulse time is added to ideal pulse when $i_a > 0$. The compensation method is that reduce T_{DT} from ideal opening time of upper switch and reduce T_{DT} from ideal opening time of lower switch. This achieves the purpose that actual opening time of switch is equal to ideal opening time of switch and actual pulse width of switch is equal to ideal pulse width of switch.

Figure 3.4(b) shows pulse time compensation when $i_a < 0$. The correction is similar to $i_a > 0$, except pulse time is subtracted from ideal pulse time. The compensation method is that reduce T_{DT} from ideal closing time of upper switch and reduce T_{DT} from ideal closing time of lower switch. This achieved the purpose that actual closing time of switch is equal to ideal closing time of switch and actual pulse width of switch is equal to ideal pulse width of switch.

In a modulation period, t_{on} represents ideal opening trigger conduction time of switch and $t_{on}^{'}$ represents opening trigger conduction time of switch after compensation, t_{off} represents ideal closing trigger conduction time of switch and $t_{off}^{'}$ represents closing trigger conduction time of switch after compensation. If $i_a > 0$, then $t_{on}^{'} = t_{on} - T_{DT}$, and if $i_a < 0$, then $t_{off}^{'} = t_{off} - T_{DT}$. Using pulse time compensation method requires knowledge of the output current direction.

There are large harmonics in the output current, and it is difficult to determine the direction of output current when current is in zero-crossing period. So, it is difficult to determine the direction of current directly. But it is possible to predict current direction by power factor angle. As Figure 3.5 shows, reference voltage vector v_{ref} is synthesized by three-phase stator voltage v_a, v_b, v_c and current vector i_{ref} is synthesized by three-phase stator current i_a, i_b, i_c. Two vectors rotate at the angular velocity ωt in space. So, as long as one can determine angle θ, we can determine the direction of three phase currents. Each phase has a power factor angle φ between voltage and current, therefore, the angle between v_{ref} and i_{ref} is also equals to φ. In SVPWM modulation process, the angle ωt between v_{ref} and i_{ref} is known. It is possible to find the current vector angle if we determine angle φ [63].

$$\begin{cases} \theta &= \omega t - \varphi \\ \varphi &= \arctan \frac{Q}{P} \end{cases} \tag{3.7}$$

where θ is the angle between current and v_a, P is active power, and Q is reactive power. From equation (3.7), the angle φ is obtained from calculation of arctangent between active

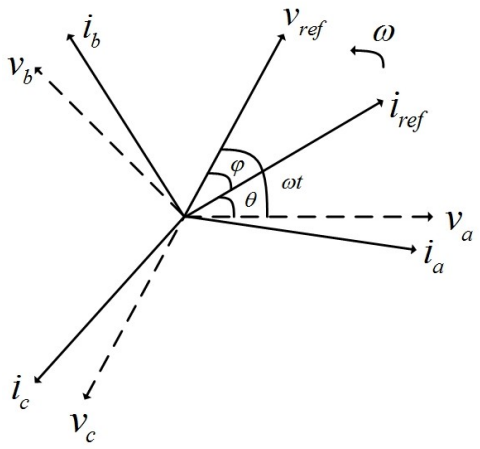


Figure 3.5: The relationship between voltage vector and current vector

θ	i_a	i_b	i_c
$-\frac{\pi}{6} - \frac{\pi}{6}$	+	-	-
$\frac{\pi}{6} - \frac{\pi}{2}$	+	+	-
$\frac{\pi}{2} - \frac{5\pi}{6}$	-	+	-
$\frac{5\pi}{6} - \frac{7\pi}{6}$	-	+	+
$\frac{7\pi}{6} - \frac{3\pi}{2}$	-	-	+
$\frac{3\pi}{2} - \frac{11\pi}{6}$	+	-	+

Table 3.1: The relationship between angle of current vector and current direction

and reactive power, and active and reactive power is obtained from measuring input current and voltage. As shown in Table 3.1, we can determine the direction of three phase currents if the angle of current vector θ is known.

2) Proposed voltage compensation method Voltage compensation method is that the dead time effect is considered as disturbance voltage vector and is eliminated by superimposing a compensation vector on the command voltage vector to offset disturbance voltage vector [65] - [68]. Generally, dead time is fixed at constant value. In this paper, however, dead time changes with the amplitude of output current, and dead time has a linear relationship with the amplitude of output current. Initially, set dead time equations as follows [64]:

$$t_{jd} = k \mid i_j \mid \quad j \in (a, b, c) \tag{3.8}$$

where k is a constant value and the specific value can be determined in the actual system.

According to (3.8), the value of dead time is close to zero when the output current is close to zero. To prevent dead time becoming too small, (3.8) is modified as follows:

$$t_{jd} = \begin{cases} k \mid i_j \mid & \mid i_j \mid \geq \frac{t_{DT\_min}}{k} \\ t_{DT\_min} & \mid i_j \mid \leq \frac{t_{DT\_min}}{k} \end{cases} \tag{3.9}$$

where t_{DT_min} is the minimum allowable dead time of inverter.

According to the equation (3.9), it is possible that the value of dead time may exceed the maximum value of dead time when the output current becomes larger. To solve this problem, consider k no longer as a constant value, smaller load current corresponds to larger k and larger load current corresponds to smaller k.

$$k = \frac{t_{DT\_max}}{\max(\sqrt{\frac{3}{2}} \mid i_a \mid, \sqrt{\frac{3}{2}} \mid i_b \mid, \sqrt{\frac{3}{2}} \mid i_c \mid)} \tag{3.10}$$

Then, when $i > 0$, the actual error time are as follows:

$$\begin{cases} T_{DT\_a} & = k \mid i_a \mid + t_{on} - t_{off} + T_s \frac{MV_s + (1-M)V_d}{V_{dc} + V_d - V_s} \\ T_{DT\_b} & = k \mid i_b \mid + t_{on} - t_{off} + T_s \frac{MV_s + (1-M)V_d}{V_{dc} + V_d - V_s} \\ T_{DT\_c} & = k \mid i_c \mid + t_{on} - t_{off} + T_s \frac{MV_s + (1-M)V_d}{V_{dc} + V_d - V_s} \end{cases} \tag{3.11}$$

The voltage compensation method is closely related to the SVPWM algorithm. Traditional SVPWM algorithm needs coordinate transformations, trigonometric calculations, sector number identification, and calculation of actual gating time. In this research, the simplified SVPWM algorithm directly uses the instantaneous values of three phase reference voltages to calculate actual gating time for each inverter leg. The method doesn't need coordinate transformations, trigonometric calculations, sector number identification, and calculation of actual gating time. The simplified SVPWM algorithm is very suitable for compensation of dead time effect. For two-level inverter, the simplified SVPWM algorithm

is obtained by using the equations (2.29) to (2.33); for multi-level inverter, the simplified SVPWM algorithm is obtained by using the equations (2.43) to (2.45).

The influences of turn-on and turn-off time of switch and voltage drop of devices are very small. If turn-on and turn-off time of switch and voltage drop of devices are ignore, then the dead time equations are as follows:

$$T_{DT\_j} = k \mid i_j \mid \quad j \in (a, b, c) \tag{3.12}$$

Average voltage loss in one PWM period caused by dead time is obtained.

$$V_{DT\_j} = \frac{V_{dc}}{T_s} k i_j \quad j \in (a, b, c) \tag{3.13}$$

The disturbance voltage vector caused by dead time is as follows:

$$\Delta V = \frac{V_{dc}}{T_s} k (i_a + e^{j\frac{2\pi}{3}} i_b + e^{j\frac{4\pi}{3}} i_c) \tag{3.14}$$

From equation (3.14), we can see that the disturbance of voltage vector has no relationship with the direction of output current. In the proposed voltage compensation method, the direction of current is not required to compensate the dead time effect. Voltage loss of each phase caused by dead time can be directly compensated to three phase input voltages [13].

$$v_j^{'} = v_j + V_{DT\_j} \quad j \in (a, b, c) \tag{3.15}$$

3.2 Dc-link capacitor voltage control strategy

As described in many literatures, by using multi-level technology, the voltage stress on each switch is reduced, the harmonic distortion of output voltage is diminished, and the ratings of voltage and power are increased. However, the dc-capacitor voltage fluctuation can impose several direct and indirect disadvantages on DCVSI operation, such as overvoltage

stress on switching devices, reduction of reliability, increase in output THD, and reduction of maximum switching frequency and output power. If the voltage drift of dc-link capacitors is not controlled, then imbalances of these capacitor voltages may even lead to collapse of voltage under a wide range of operating conditions.

3.2.1 Basic principle of dc-link capacitor voltage control

The following three-phase three-level inverter is studied as an example. The topology of three-level NPC inverter is shown in Figure 2.9. Zero voltage vectors cause the three phases to be short-circuited either to the midpoint of the series connected capacitors or to the positive dc-rail or to the negative dc-rail. Large voltage vectors connect one or two of three phases to the positive dc-rail and the rest of three phases to the negative dc-rail. The zero voltage vectors and the large voltage vectors are free from the variation of the neutral-point potential since the neutral-point (NP) current does not flow. For the medium voltage vectors, one of the three phases is always connected to the neutral point. Therefore, the NP current flows and its direction is decided according to the load current. The effect of middle vectors is not controllable. For small voltage vectors, every small voltage vector owns two statuses, positive or negative, which have opposite influences on the NP potential balance. Therefore, the NP current can be controlled by using small voltage vectors. The relationship between voltage vectors and NP currents is shown in Table 3.2 [69] - [72]. Dc-link

Small vector	i_{NP}	Small vector	i_{NP}	Medium vector	i_{NP}
ONN	i_a	POO	$-i_a$	PON	i_b
PPO	i_c	OON	$-i_c$	OPN	i_a
NON	i_b	OPO	$-i_b$	NPO	i_c
OPP	i_a	NOO	$-i_a$	NOP	i_b
NNO	i_c	OOP	$-i_c$	ONP	i_a
POP	i_b	ONO	$-i_b$	PNO	i_c

Table 3.2: Relationship between NP currents and voltage vectors

capacitor voltage balancing can be achieved by selecting appropriate small vectors during each sampling time. When the NP potential is higher than reference, the switching states,

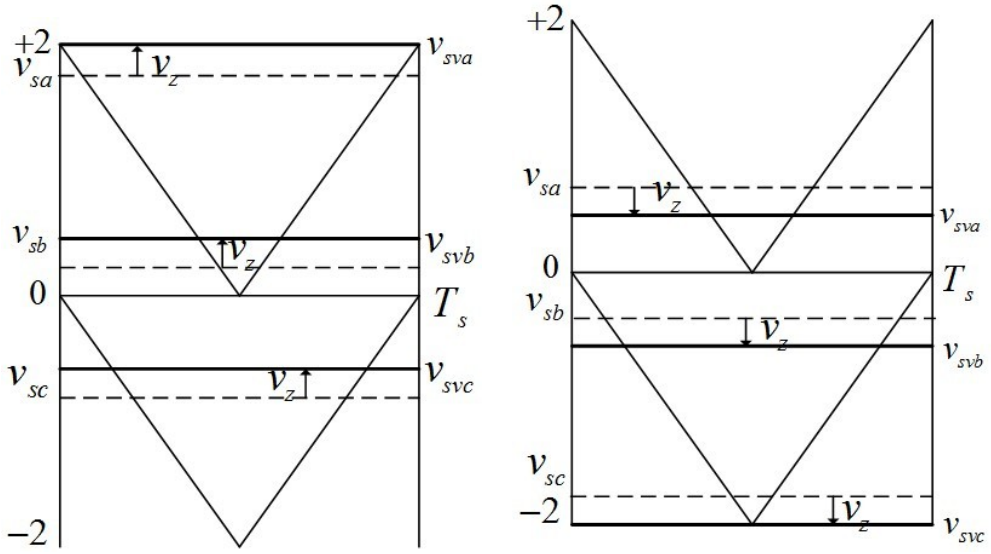
which make the current discharge the dc-link capacitor, are selected. Similarly, the switching states, which make the current charge the dc-link capacitor, are rejected. On the contrary, when the NP potential is lower than reference, the principle is employed too.

3.2.2 Proposed dc-link capacitor voltage control

To obtain lower THD in the output voltage of inverter and reduce some disadvantages caused by NP unbalance, NP control for multi-level inverter is necessary. Dc-link capacitor voltage balancing can be achieved by selecting appropriate small vectors during each sampling time, and rearrangement of zero voltage vectors can also solve the problem. The modulation implicit functions of SVPWM are obtained by adding zero voltage vectors to the modulation implicit functions of SPWM. Suppose switching states are shown as Figure 2.13, the switching states are OON, PON, PPN and PPO. In Figure 2.13, pulse width of PPO is larger than initial value after adding zero voltage vectors and pulse width of OON is smaller than initial value after adding zero voltage vectors. When capacitor voltage difference $\Delta V = V_{C1} - V_{C2} > 0$, duration of state N is reduced and duration of state P is increased. Conversely, when capacitor voltage difference $\Delta V = V_{C1} - V_{C2} < 0$, duration of state N is increased and duration of state P is reduced. If capacitor voltage difference $\Delta V > 0$, take a small value of k in order to increase the zero voltage vector. Similarly, if capacitor voltage difference $\Delta V < 0$, take a big value of k in order to reduce the zero voltage vector. Therefore, neutral point voltage can be controlled by adjusting the value of k.

As explained in the previous subsection, it is important to note that there are positive and negative small vectors that have opposite influences on the NP potential balance. Pulse width of positive small vector is larger than initial value after adding zero voltage vectors, while pulse width of negative small vector is smaller than initial value after adding zero voltage vectors. If capacitor voltage difference $\Delta V > 0$, DSVPWMmax can be used in order to decrease duration of state N, and similarly, if capacitor voltage difference $\Delta V < 0$, DSVPWMmin can be used in order to decrease duration of state P. According to Figure

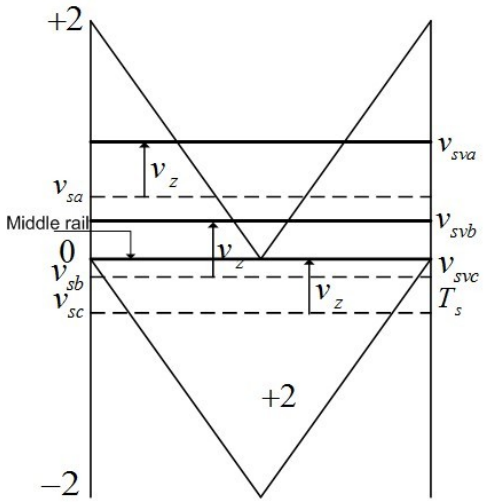
3.6(a), even though the DSVPWMmax method is used to decrease duration of state N, one or two voltages still have negative value. Similarly, in Figure 3.6(b), despite using the DSVPWMmin method to decrease duration of state P, one or two voltages still has positive value.



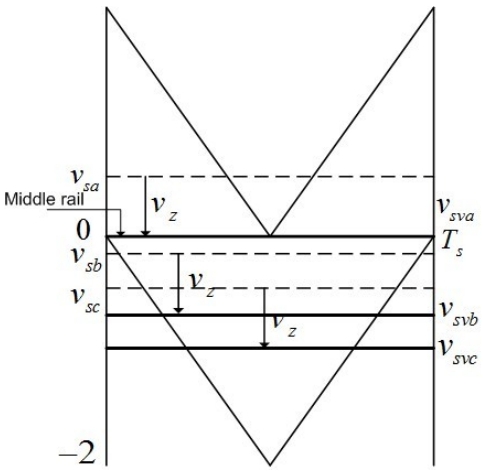
(a) Clamped to positive rail (b) Clamped to negative rail

Figure 3.6: DSVPWM method for three-level inverter

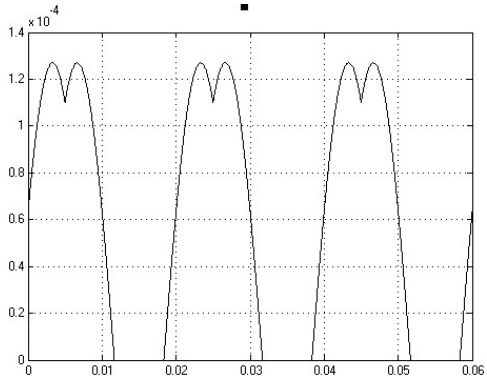
To balance dc-link capacitor voltages, alternative selection of zero voltage vectors has been proposed. In order to make the entire three phase modulation implicit functions locate at positive ordinate or negative ordinate, maximum and minimum modulation implicit values of three phases can be clamped to the middle rail is applied [73][14]. In this paper, another control method is synthesized by combining the simplified DSVPWM for multi-level inverter and the method of clamping to the middle rail. Figure 3.7(a) and (b) show three phase modulation implicit functions clamped to the positive and negative middle rail, respectively. Figure 3.7(c) and (d) show the waveforms of pulse width of modulation using the middle rail method. From the pictures, we can see that the waveform of modulation implicit value has been either positive or negative. The proposed DSVPWM method obtains maximum durations of state P and N, which eliminates drawbacks of DSVPWMmax and DSVPWMmin.



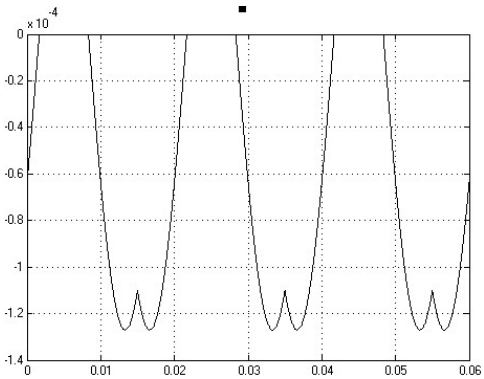
(a) Clamped to positive middle rail



(b) Clamped to negative middle rail



(c) PWM waveform based on positive middle rail



(d) PWM waveform based on negative middle rail

Figure 3.7: DSVPWM method and PWM modulation

In the control algorithm, if the DSVPWM4 method is used for three-level inverter, DSVPWM4 is like DSVPWMmax from [-15°, 15°] and is like DSVPWMmin from [15°, 45°]. From [-15°, 15°], if $\Delta V > 0$, then the DSVPWMmax method ($k = 0$ in formula (2.43)) can be used, else negative middle rail method (the zero sequence voltage vector equation $v_z = -max$) can be used to balance dc-link capacitor voltage. Similarly, during [15°, 45°], if $\Delta V < 0$, then the DSVPWMmin method ($k = 1$ in formula (2.43)) can be used, else positive middle rail method (the zero sequence voltage vector equation $v_z = -min$) can be used to balance dc-link capacitor voltage. There are three dc-link capacitors for the four-level inverter. Therefore, it is necessary to compare the pair v_{c1} and v_{c3}, then compare v_{c1}, v_{c2} and v_{c2}, v_{c3}. Similarly, we can get dc-link capacitor voltage control algorithm for other multi-level inverters.

3.3 Control scheme of unbalanced three-phase grid voltage

Most electrical systems are designed on the basis of balanced three-phase grid voltage at the fundamental frequency. However, under real operating conditions, three phase grid voltages are under unbalanced conditions. The performance of balanced grid voltage is not necessarily the same as the performance of unbalanced grid voltage. The operating conditions can be affected by faults or other kinds of disturbances at grid side. The most usual grid faults are two-phase and single-phase faults that, although less severe than three-phase faults, imply voltage imbalance which leads to oscillation of system variables because of the appearance of negative sequence voltages and currents. Under unbalanced conditions, abnormal harmonics are introduced into the system and appear at both the input and output terminals and causes distortions in the waveforms. Hence, the strategy to improve the operational performance of grid connected-VSI is under unbalanced network conditions has obtained a worldwide concern [74] - [79].

On the basis of simplified SVPWM and DSVPWM algorithm, the concept of voltage modulation by using offset voltage is applied to an unbalanced three-phase grid voltage

control method [80] - [82]. The algorithm is based on simple control structure and does not demand any filter for obtaining symmetrical components, e.g. notch or anti-resonant filter. The control objective is to balance three phase output currents and minimize THD of the output currents without ac current sensors under unbalanced grid voltage conditions. The attractive advantage of this controller is the possibility of effective operation under both balanced and unbalanced conditions.

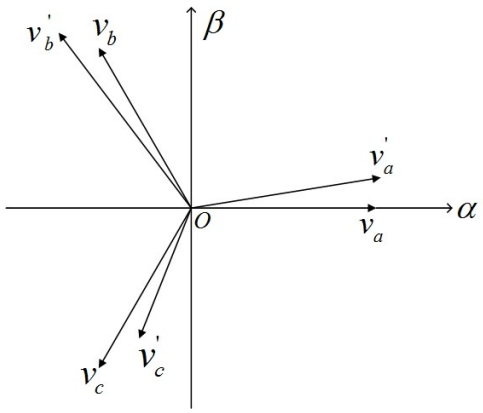


Figure 3.8: Three phase voltages

The main objective is to regulate the dc-link voltage and to achieve constant power transfer under all possible conditions and to achieve unity power factor for a balanced case. In the balanced three-phase conditions, as Figure 3.8 shows $v_a = 220\sin(\omega t)$, $v_b = 220\sin(\omega t - 120°)$, and $v_c = 220\sin(\omega t + 120°)$. In the unbalanced three-phase conditions, as Figure 3.8 shows $v_a' = 220\sin(\omega t + 10°)$, $v_b' = 260\sin(\omega t - 110°)$, and $v_c' = 180\sin(\omega t + 130°)$. The sum of balanced three phase grid voltages is equal to zero $v_a + v_b + v_c = 0$, and the sum of unbalanced three phase grid voltages is not equal to zero $v_a' + v_b' + v_c' \neq 0$. The zero sequence voltage is as follows:

$$v_{z0} = \frac{1}{3}(v_a + v_b + v_c) \tag{3.16}$$

If we know the parameters of three phase grid voltages, then the zero sequence voltage is obtained. The unbalanced voltages can be made balanced by subtracting the zero sequence voltage from the actual voltages. Actual zero sequence voltage is $v_{z0}' = \frac{1}{3}(v_a' + v_b' + v_c')$, then

the compensation method is that $v_a^{''} = v_a^{'} - v_{z0}^{'}$, $v_b^{''} = v_b^{'} - v_{z0}^{'}$, and $v_c^{''} = v_c^{'} - v_{z0}^{'}$. The zero sequence voltage from new set of voltages after compensation method is equal to zero.

$$v_{z0}^{''} = \frac{1}{3}(v_a^{''} + v_b^{''} + v_c^{''}) = 0 \tag{3.17}$$

The balanced three phase grid voltages after compensation of zero sequence voltage are still balanced three phase grid voltages, and the unbalanced three phase grid voltages can be made balanced after compensation of zero sequence voltage. The new set of voltages after compensation method are used as new three phase voltages and used for formula (2.30) or (2.40).

3.4 Energy feedback VSI control method

With the development of the world economy, energy conservation and development utilization of environmental protection sustainable new energy become new problem. Energy feedback VSI as access port to the power grid achieves energy conversion. Distributed generation, regenerative type of power dummy load, and motor brake energy feedback system are several occasions of energy feedback practical applications. From energy conservation and new energy technology perspective, the energy feedback VSI system has great theoretical and practical significance. The energy feedback control is divided into direct current control method and indirect current control method. The indirect current control method is used in this research.

Phase and amplitude control mainly represents indirect current control method [83] - [86]. Advantage of indirect current control method is simple control strategy, generally do not need a current feedback control. Disadvantage of indirect current control is slow current dynamic response. Indirect current control technique is essentially controlled by PWM method. Fundamental voltage waveform is controlled by the amplitude and phase angle, and the control method also stabilizes the dc-link voltage. The current control scheme is

purposed to control ac side current by directly controlling the ac side voltage, therefore this kind of method is indirect current control method.

The main circuit of energy feedback device is mainly composed of three phase intelligent power module and some peripheral circuits. The output terminal of the inverter bridge connected with the input terminals of converter through three choke reactors, and input terminal connected with dc side of converter P, N with two isolation diodes in order to protect energy unidirectional flow from converter to grid.

Phase and amplitude control method also known as indirect current control theory. The most significant advantages of this theory are simple structure, no current sensor, and excellent static performance. As phase a in Figure 1.3, shown in Figure 3.9, steady-state circuit equations of phase a voltage can be listed as follows:

$$E_a = j\omega L_a I_a + R_a I_a + V_a \tag{3.18}$$

where, E_a is grid voltage of phase a, I_a is output inverter current of phase a, L_a is choke inductance of phase a, R_a is equivalent resistance of phase a, and V_a is output voltage of phase a.

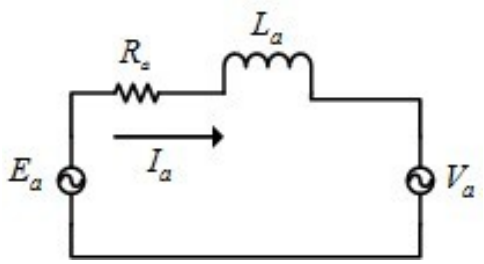
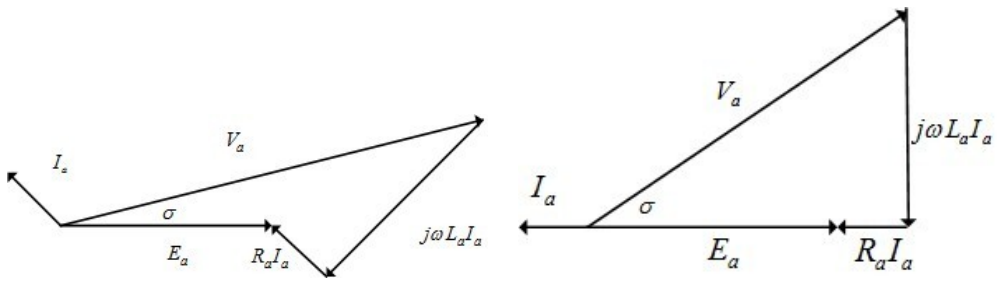


Figure 3.9: Steady state model of phase a

Formula (3.18) shows that as long as amplitude and phase angle of output voltage V_a is adjustable, we can control the amplitude and phase angle of output current I_a, for the case of constant grid voltage E_a, and choke inductance L_a. We can achieve the desired magnitude of feedback current and feedback power factor. However, it can be seen from equation (3.18)



(a) Non-unity power factor feedback (b) Unity power factor feedback

Figure 3.10: The vector diagram of feedback voltage

that amplitude and phase angle of voltage and current are coupled, so we need decoupling operations to get the desired control variables. Vector graphics of formula (3.18) are shown in Figure 3.10. This work only analyzes the relationship between variables in the case of unity power factor feedback. Because the non-unity power factor case has many disadvantages for power grid. From formula (3.18) and Figure 3.10, the following equations are obtained.

$$V_a \cos\sigma = E_a + R_a I_a \tag{3.19}$$

$$V_a \sin\sigma = \omega L_a I_a \tag{3.20}$$

where σ is phase angle.

Phase angle is obtained by the formula (3.21).

$$\sigma = \arctan \frac{\omega L_a I_a}{E_a + R_a I_a} \tag{3.21}$$

Also we know

$$V_a = \frac{M V_{dc}}{\sqrt{3}\sqrt{2}} \tag{3.22}$$

where, M is ratio of pulse width modulation and V_{dc} is dc bus voltage of converter.

By formulas (3.19) to (3.22), we can obtain

$$M = \frac{\sqrt{6}\omega L_a I_a}{V_{dc} \sin\sigma} \tag{3.23}$$

From the above analysis, we can calculate angle σ and ratio of pulse width modulation M using equations (3.21) and (3.23) as long as grid voltage E_a, dc bus voltage V_{dc}, and feedback current are determined. The desired output voltages are directly used for simplified SVPWM algorithm to control power switches to track the desired output currents. Through the phase angle and amplitude control theory we can achieve unity power factor control of energy feedback if we know σ and M.

Feedback current i_a can be determined by the conservation of energy or by the power balance. Energy storage of capacitor is as follows:

$$W = \frac{1}{2}CV^2 \tag{3.24}$$

As formula (3.24) shows, the energy stored in the dc bus is only related with the dc bus voltage in the case where smoothing capacitor have constant capacity. Seen from input and output energy balance of inverter, we can get formula (3.25).

$$0 = \frac{1}{2}C(V_k^2 - V_0^2) + 3TE_aI_a\cos\varphi \tag{3.25}$$

When feedback at unity power factor, $\cos\varphi = -1$, the above equation can be obtained as follows:

$$i_a = \frac{C(V_k^2 - V_0^2)}{6E_aT} \tag{3.26}$$

where C is smoothing capacitor value, V_k is dc bus voltage, V_0 is maximum bus voltage of converter state, E_a is grid voltage, T is feedback time and i_a is feedback current.

The maximum bus voltage of converter state refers to the maximum voltage that may appear on the dc bus. Assuming the grid voltage fluctuation is $\pm 15\%$ and grid voltage is $220V$, then the maximum bus voltage is as follows.

$$V_0 = \sqrt{3} \times \sqrt{2} \times 220 \times (1 + 15\%) = 619.72V \tag{3.27}$$

In order to avoid frequent start-stop at the vicinity of a voltage, define lower limit $V_L = 620V$ and upper limit $V_H = 680V$. Energy flows from dc side to grid network when the dc bus voltage continues to rise and exceeds start working voltage of inverter $680V$ (high limit), and the inverter is turned off when the dc bus voltage drops to shut down voltage of inverter $620V$ (low limit).

According to the equation (3.26), we can calculate feedback current i_a if feedback time T is determined. Feedback time T changes according to the capacitor energy. Reduce feedback time if the energy gradually increased, and increase feedback time if the energy gradually decreased. Feedback time is determined based on the dc bus energy, feedback cycle, and energy changes. Feedback time is not fixed but changed in real time.

Energy generated by generator may be higher than feedback energy, led to further increase of dc bus voltage. Therefore, the system must start emergency measures when the dc bus voltage exceeds a certain value. To prevent damage to the system, all the energy need to be feedback to the power grid in a few cycles.

Through input and output power balance of system, we can get formula (3.28) or (3.29) [1].

$$0 = 3E_a i_a \cos\varphi + V_k i_0 \tag{3.28}$$

$$0 = 3E_a i_a \cos\varphi + \frac{V_k^2}{R_0} \tag{3.29}$$

When feedback at unity power factor, $\cos\varphi = -1$, the following equation can be obtained as follows:

$$i_a = \frac{V_k i_0}{3E_a} \tag{3.30}$$

$$i_a = \frac{V_k^2}{3E_a R_0} \tag{3.31}$$

where, i_0 is dc bus current, R_0 is load resistance of converter in dc side.

When starting the inverter, the amplitude and phase difference of voltage directly determine the size of transient current and starting regulation time of system. Therefore, the

initial value of σ and M is very important. If the initial value is set properly, we can achieve unity power factor starting. If set improperly, the system is unable get into the steady state, produces big transient current, and in severe conditions damage to the power devices. The predictive voltage control is based on the starting parameters to calculate desired α and M values and use them as the initial value of starting system [87][88]. To improve dynamic performance of indirect current control method, references [87][88] propose and study the current feed-forward control method.

Chapter 4

Direct matrix converter

4.1 Introduction

In 1976, the direct matrix converter (DMC) which uses an array of $m \times n$ controlled bi-directional switch is proposed by reference [89]. The direct matrix converter generates n-phase variable output voltages with unrestricted frequency from m-phase ac source voltages. Figure 4.1 shows the direct matrix converter with an array of 3×3 power switches. The three-phase direct matrix converter has been researched due to its potential value to replace ac-dc-ac converter. Compared to traditional ac-dc-ac converter, the direct matrix converter has some advantages such as adjustable input displacement factor, irrespective of the load, capability of regeneration, high quality input and output waveforms, and without a bulky dc link capacitor. Compared to traditional ac-dc-ac converter, the direct matrix converter also has some disadvantages like limited voltage transfer ratio (0.866), more power switches, and complex control method.

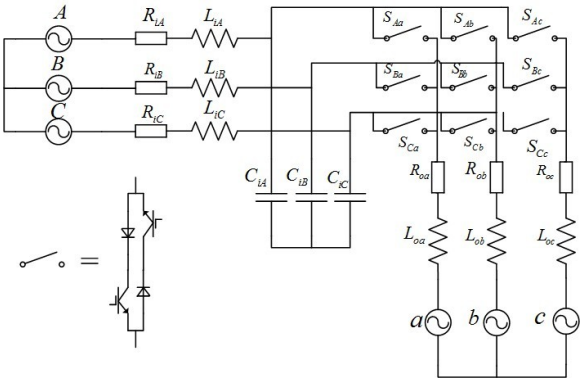


Figure 4.1: Power circuit topology of a three-phase direct matrix converter

The power circuit topology of a 3×3 direct matrix converter is shown in Figure 4.1. There are three legs, with each leg having three bidirectional power switches connected in

series. To obtain a bidirectional power flow, back to back switches are used. It requires two IGBT and two fast recovery diodes to allow a bidirectional power flow, as Figure 4.1 shows. The input is a three-phase power supply with RLC filters. The load attached to the matrix converter could be a star-connected load or an ac machine. The switching function is defined as S_{pj}=$\{$1 for closed switch, 0 for open switch$\}$, with $j = \{A, B, C\}$ (output) and $p = \{a, b, c\}$ (input). Due to the direct connection with voltage sources, the input lines must never be shorted to each other. If the switches cause a short circuit between the input voltage sources, infinite current flows through the switches and damages the circuit. Also, due to the inductive nature of typical loads, the output terminals must not be open-circuited. If any output terminal is open-circuited, the voltage across the inductor (and consequently across the switches) is infinite and switches will be damaged due to the over-voltage. The switching constraint rules are as follows:

$$S_{aj} + S_{bj} + S_{cj} = 1 \qquad j \in (A, B, C) \tag{4.1}$$

where S_{pj} is the switching function of a power switch, which is defined as:

$$S_{pj} = \begin{cases} 1 & S_{pj} \text{ closed} \qquad p \in (a, b, c) \qquad j \in (A, B, C) \\ 0 & S_{pj} \text{ opened} \end{cases} \tag{4.2}$$

Direct matrix converter is a direct ac-ac frequency converter that generates variable voltage variable frequency from the ac utility line using semiconductor switches arranged in the form of a matrix array. It has many desirable features such as bidirectional power flow, controllable input power factor, sinusoidal input and output waveforms, light-weight, long lifetime, and all without a bulky dc link capacitor. Due to the existing advantages, matrix converter has recently attracted much attention such as commercial, industrial, and aerospace applications [8]. The main task of modulation for the matrix converter is to generate the required output voltages while controlling the input currents or the power factor as required.

The performance of matrix converter is strictly depending on the modulation strategy employed to control the bidirectional switches. Various and numerous modulation strategies have been extensively investigated up to now. Alesina and Venturini [90][91] derived duty ratio functions that can be modulated by the carrier signal, popularly known as Alesina and Venturini method and Alesina and Venturini optimum method. Direct SVPWM method for the matrix converter explores more systematic approach to understand the operation of the matrix converter [92][93]. Various carrier-based modulation methods are also investigated in [94] - [99]. The following parts propose and investigate a unified carrier based modulation method for direct matrix converter. The control methods such as dead time compensation, unbalanced three-phase control, and energy feedback control are also proposed and studied.

4.2 Modulation method for direct matrix converter

This part describes the different modulation strategies for the direct matrix converter (DMC). These are the traditional SVPWM strategy and a unified carrier-based modulation method.

4.2.1 SVPWM method for direct matrix converter

The SVPWM algorithm is well known in the conventional inverter system. Space vector concept allows a 3-phase set of quantities to be represented by a single vector on a complex plane. This method is particularly popular with researchers in the area of vector control because it allows visualization of the spatial and time relationships between the resultant current and flux vectors in various reference frames. Traditional SVPWM method for direct matrix converter is presented at the following part [100] - [106].

Synthesis of voltage space vector and current space vector are as follows:

$$\begin{cases} V_o(t) = \frac{2}{3}(v_a(t) + \zeta v_b(t) + \zeta^2 v_c(t)) \\ I_i(t) = \frac{2}{3}(i_a(t) + \zeta i_b(t) + \zeta^2 i_c(t)) \end{cases} \tag{4.3}$$

where $\zeta = e^{j\frac{2\pi}{3}}$.

Geometrically, this amounts to plot the instantaneous values of three voltages along axes displaced by 120°, as shown in Figure 2.1. Compared to two-level three-phase VSI system, the three-phase to three-phase matrix converter has 27 switching states. 27 possible vectors can be split into 3 groups.

Group I: each output line is connected to a different input line.

Space vectors of output voltage rotate at ω_i, and space vectors of input current rotate at ω_o.

Group II: two output lines are connected to a common input line; the remaining output line is connected to one of the other input lines.

Space vectors of output voltage take one of 6 fixed positions (varying amplitude), and space vectors of input current take one of 6 fixed positions (varying amplitude).

Group III: all output lines are connected to a common input line.

All space vectors are at the origin (zero length).

Of these three groups, Group I is not useful, only Groups II (18 vectors) and III (3 vectors) which are shown in Table 4.1 are used in this method. Calculations can be performed

Vector number	Conducting switches	Output phase voltages	Output line to line voltages	Input line currents
$+1$	S_{Aa}, S_{Bb}, S_{Bc}	V_A, V_B, V_B	$V_{AB}, 0, -V_{AB}$	$I_a, I_b + I_c, 0$
-1	S_{Ba}, S_{Ab}, S_{Ac}	V_B, V_A, V_A	$-V_{AB}, 0, V_{AB}$	$I_b + I_c, I_a, 0$
$+2$	S_{Ba}, S_{Cb}, S_{Cc}	V_B, V_C, V_C	$V_{BC}, 0, -V_{BC}$	$0, I_a, I_b + I_c$
-2	S_{Ca}, S_{Bb}, S_{Bc}	$V_C, V_B V_B$	$-V_{BC}, 0, V_{BC}$	$0, I_b + I_c, I_a$
$+3$	S_{Ca}, S_{Ab}, S_{Ac}	V_C, V_A, V_A	$V_{CA}, 0, -V_{CA}$	$I_b + I_c, 0, I_a$
-3	S_{Aa}, S_{Cb}, S_{Cc}	$V_A, V_C V_C$	$-V_{CA}, 0, V_{CA}$	$I_a, 0, I_b + I_c$
$+4$	S_{Ba}, S_{Ab}, S_{Bc}	V_B, V_A, V_B	$-V_{AB}, V_{AB}, 0$	$I_b, I_a + I_c, 0$
-4	S_{Aa}, S_{Bb}, S_{Ac}	$V_A, V_B V_A$	$V_{AB}, -V_{AB}, 0$	$I_a + I_c, I_b, 0$
$+5$	S_{Ca}, S_{Bb}, S_{Cc}	V_C, V_B, V_C	$-V_{BC}, V_{BC}, 0$	$0, I_b, I_a + I_c$
-5	S_{Ba}, S_{Cb}, S_{Bc}	$V_B, V_C V_B$	$V_{BC}, -V_{BC}, 0$	$0, I_a + I_c, I_b$
$+6$	S_{Aa}, S_{Cb}, S_{Ac}	V_A, V_C, V_A	$-V_{CA}, V_{CA}, 0$	$I_a + I_c, 0, I_b$
-6	S_{Ca}, S_{Ab}, S_{Cc}	$V_C, V_A V_C$	$V_{CA}, -V_{CA}, 0$	$I_b, 0, I_a + I_c$
$+7$	S_{Ba}, S_{Bb}, S_{Ac}	V_B, V_B, V_A	$0, -V_{AB}, V_{AB}$	$I_c, I_a + I_b, 0$
-7	S_{Aa}, S_{Ab}, S_{Bc}	V_A, V_A, V_B	$0, V_{AB}, -V_{AB}$	$I_a + I_b, I_c, 0$
$+8$	S_{Ca}, S_{Cb}, S_{Bc}	V_C, V_C, V_B	$0, -V_{BC}, V_{BC}$	$0, I_c, I_a + I_b$
-8	S_{Ba}, S_{Bb}, S_{Cc}	V_B, V_B, V_C	$0, V_{BC}, -V_{BC}$	$0, I_a + I_b, I_c$
$+9$	S_{Aa}, S_{Ab}, S_{Cc}	V_A, V_A, V_C	$0, -V_{CA}, V_{CA}$	$I_a + I_b, 0, I_c$
-9	S_{Ca}, S_{Cb}, S_{Ac}	V_C, V_C, V_A	$0, V_{CA}, -V_{CA}$	$I_c, 0, I_a + I_b$

Table 4.1: 3×3 Matrix converter stationary and zero switching combinations

at a regular sampling frequency. The desired output voltage space vector rotates in the

space, but can be assumed that is fixed at a particular magnitude and phase angle during each sampling period.

Relationship between switching state and corresponding output line and phase voltages are shown in Table 4.1. 21 switching states formed 21 voltage vectors in the space, as shown in Table 4.2. wherein the vectors $0_1, 0_2, 0_3$ are equal, they coincide with the origin

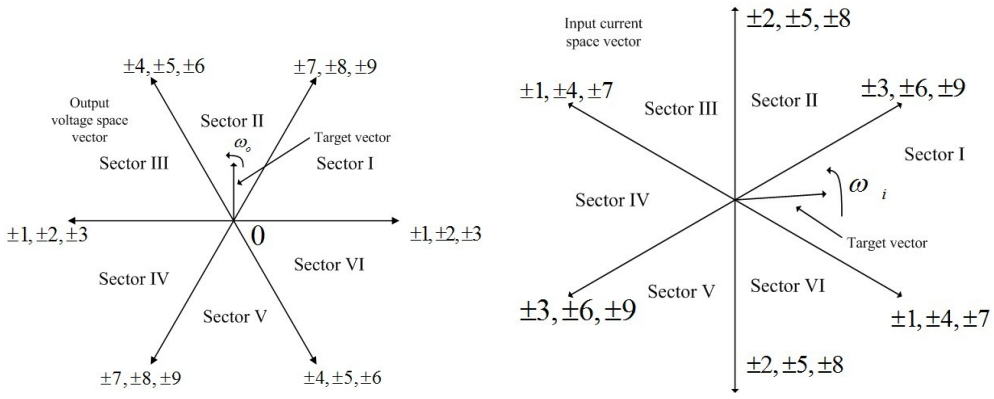
Switching configuration	Converter state	v_o	α_o	i_i	β_i
$+1$	S_{ABB}	$\frac{2}{3}v_{ABi}$	0	$\frac{2}{\sqrt{3}}i_{ao}$	$-\frac{\pi}{6}$
-1	S_{BAA}	$-\frac{2}{3}v_{ABi}$	0	$-\frac{2}{\sqrt{3}}i_{ao}$	$-\frac{\pi}{6}$
$+2$	S_{BCC}	$\frac{2}{3}v_{BCi}$	0	$\frac{2}{\sqrt{3}}i_{ao}$	$\frac{\pi}{2}$
-2	S_{CBB}	$-\frac{2}{3}v_{BCi}$	0	$-\frac{2}{\sqrt{3}}i_{ao}$	$\frac{\pi}{2}$
$+3$	S_{CAA}	$\frac{2}{3}v_{VAi}$	0	$\frac{2}{\sqrt{3}}i_{ao}$	$\frac{7\pi}{6}$
-3	S_{ACC}	$-\frac{2}{3}v_{CAi}$	0	$-\frac{2}{\sqrt{3}}i_{ao}$	$\frac{7\pi}{6}$
$+4$	S_{BAB}	$\frac{2}{3}v_{BAi}$	$\frac{2\pi}{3}$	$\frac{2}{\sqrt{3}}i_{bo}$	$-\frac{\pi}{6}$
-4	S_{ABA}	$-\frac{2}{3}v_{ABi}$	$\frac{2\pi}{3}$	$-\frac{2}{\sqrt{3}}i_{bo}$	$-\frac{\pi}{6}$
$+5$	S_{CBC}	$\frac{2}{3}v_{BCi}$	$\frac{2\pi}{3}$	$\frac{2}{\sqrt{3}}i_{bo}$	$\frac{\pi}{2}$
-5	S_{BCB}	$-\frac{2}{3}v_{BCi}$	$\frac{2\pi}{3}$	$-\frac{2}{\sqrt{3}}i_{bo}$	$\frac{\pi}{2}$
$+6$	S_{ACA}	$\frac{2}{3}v_{CAi}$	$\frac{2\pi}{3}$	$\frac{2}{\sqrt{3}}i_{bo}$	$\frac{7\pi}{6}$
-6	S_{CAC}	$-\frac{2}{3}v_{CAi}$	$\frac{2\pi}{3}$	$-\frac{2}{\sqrt{3}}i_{bo}$	$\frac{7\pi}{6}$
$+7$	S_{BBA}	$\frac{2}{3}v_{ABi}$	$\frac{4\pi}{3}$	$\frac{2}{\sqrt{3}}i_{co}$	$-\frac{\pi}{6}$
-7	S_{AAB}	$-\frac{2}{3}v_{ABi}$	$\frac{4\pi}{3}$	$-\frac{2}{\sqrt{3}}i_{co}$	$-\frac{\pi}{6}$
$+8$	S_{CCB}	$\frac{2}{3}v_{BCi}$	$\frac{4\pi}{3}$	$\frac{2}{\sqrt{3}}i_{co}$	$\frac{\pi}{2}$
-8	S_{BBC}	$-\frac{2}{3}v_{BCi}$	$\frac{4\pi}{3}$	$-\frac{2}{\sqrt{3}}i_{co}$	$\frac{\pi}{2}$
$+9$	S_{AAC}	$\frac{2}{3}v_{CAi}$	$\frac{4\pi}{3}$	$\frac{2}{\sqrt{3}}i_{co}$	$\frac{7\pi}{6}$
-9	S_{CCA}	$-\frac{2}{3}v_{CAi}$	$\frac{4\pi}{3}$	$-\frac{2}{\sqrt{3}}i_{co}$	$\frac{7\pi}{6}$
0_1	S_{AAA}	0	0	0	0
0_2	S_{BBB}	0	0	0	0
0_3	S_{CCC}	0	0	0	0

Table 4.2: Switching states for a three-phase to three-phase matrix converter

of coordinates. 21 voltage vectors divide plane into six sectors and 21 current vectors also divide plane into six sectors, as shown in Figure 4.2.

For any condition, magnitude and angle of output voltage and input current angle (displacement factor) is controlled by using 4 vectors. The switching configurations for any output voltage sector and input current sector are given in Table 4.3.

where K_V is sector number of desired output voltage and K_I is sector number of desired input current.



(a) Output voltage space vectors (b) Input current space vectors

Figure 4.2: Vectors plotted in the $\alpha\beta$ plane

When the sector number of input current and output voltage are both sector I, as Figure 4.3 shows, then we can write down the equations for the lengths of the output voltage and input current space vectors.

$$\vec{v_o'} = \vec{v_o^I}\delta^I + \vec{v_o^{II}}\delta^{II} = \frac{2}{\sqrt{3}} v_o \cos(\alpha_o - \frac{\pi}{3}) e^{j[(K_v-1)\frac{\pi}{3}+\frac{\pi}{3}]} \tag{4.4}$$

$$\vec{v_o''} = \vec{v_o^{III}}\delta^{III} + \vec{v_o^{IV}}\delta^{IV} = \frac{2}{\sqrt{3}} v_o \cos(\alpha_o + \frac{\pi}{3}) e^{j[(K_v-1)\frac{\pi}{3}]} \tag{4.5}$$

$$(\vec{i_i^I}\delta_I + \vec{i_i^{II}}\delta_{II} \cdot j e^{j\beta_i} e^{j(K_i-1)\frac{\pi}{3}} = 0 \tag{4.6}$$

$$(\vec{i_i^{III}}\delta_{III} + \vec{i_i^{IV}}\delta_{IV} \cdot j e^{j\beta_i} e^{j(K_i-1)\frac{\pi}{3}} = 0 \tag{4.7}$$

where δ^I to δ^{IV} are the duty cycles for the 4 switching states. Solving equations (4.4) to

$K_I \backslash K_V$	1	2	3	4	5	6
1	$+9,-7,-3,+1$	$-6,+4,+9,-7$	$+3,-1,-6,+4$	$-9,+7,+3,-1$	$+6,-4,-9,+7$	$-3,+1,+6,-4$
2	$-8,+9,+2,-3$	$+5,-6,-8,+9$	$-2,+3,+5,-6$	$+8,-9,-2,+3$	$-5,+6,+8,-9$	$+2,-3,-5,+6$
3	$+7,-8,-1,+2$	$-4,+5,+7,-8$	$+1,-2,-4,+5$	$-7,+8,+1,-2$	$+4,-5,-7,+8$	$-1,+2,+4,-5$
4	$-9,+7,+3,-1$	$+6,-4,-9,+7$	$-3,+1,+6,-4$	$+9,-7,-3,+1$	$-6,+4,+9,-7$	$+3,-1,-6,+4$
5	$+8,-9,-2,+3$	$-5,+6,+8,-9$	$+2,-3,-5,+6$	$-8,+9,+2,-3$	$+5,-6,-8,+9$	$-2,+3,+5,-6$
6	$-7,+8,+1,-2$	$+4,-5,-7,+8$	$-1,+2,+4,-5$	$+7,-8,-1,+2$	$-4,+5,+7,-8$	$+1,-2,-4,+5$

Table 4.3: Selection of switching configurations for each combination of K_V and K_I

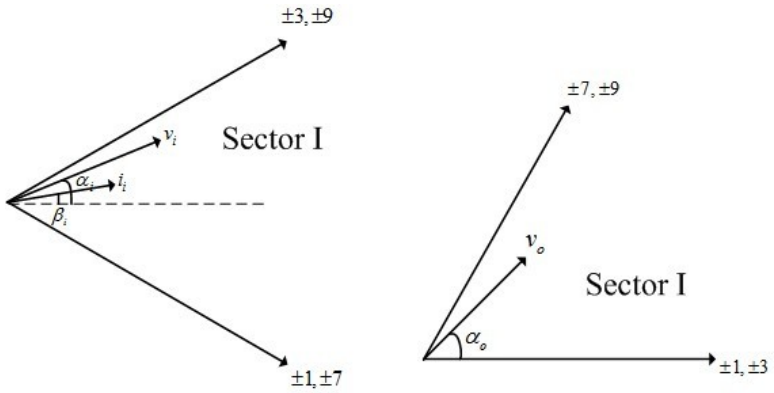


Figure 4.3: The required switching states when input current and output voltage are in sector I

(4.7), the duty cycles are obtained.

$$\delta^I = (-1)^{K_v+K_i+1}\frac{2}{\sqrt{3}}q\frac{\cos(\alpha_o-\frac{\pi}{3})\cos(\beta_i-\frac{\pi}{3})}{\cos\phi_i} \tag{4.8}$$

$$\delta^{II} = (-1)^{K_v+K_i}\frac{2}{\sqrt{3}}q\frac{\cos(\alpha_o-\frac{\pi}{3})\cos(\beta_i+\frac{\pi}{3})}{\cos\phi_i} \tag{4.9}$$

$$\delta^{III} = (-1)^{K_v+K_i}\frac{2}{\sqrt{3}}q\frac{\cos(\alpha_o+\frac{\pi}{3})\cos(\beta_i-\frac{\pi}{3})}{\cos\phi_i} \tag{4.10}$$

$$\delta^{IV} = (-1)^{K_v+K_i+1}\frac{2}{\sqrt{3}}q\frac{\cos(\alpha_o+\frac{\pi}{3})\cos(\beta_i+\frac{\pi}{3})}{\cos\phi_i} \tag{4.11}$$

where α_o and β_i are the angles of the output voltage and input current vectors, ϕ_i is the input phase displacement angle.

The restriction of duty cycles is as follows.

$$|\delta^I| + |\delta^{II}| + |\delta^{III}| + |\delta^{IV}| \leq 1 \tag{4.12}$$

The maximum transfer ratio q is obtained.

$$q \leq \frac{\sqrt{3}}{2}\frac{|\cos\phi_i|}{\cos\beta_i\cos\alpha_o} \tag{4.13}$$

For unity input power factor operation, $q \leq \frac{\sqrt{3}}{2}$. Then δ_0 is the total modulation duty cycle for the zero voltage vectors to complete the modulation period.

$$\delta_0 = 1 - (\delta^I + \delta^{II} + \delta^{III} + \delta^{IV}) \tag{4.14}$$

Using 4 (non-zero) vectors in each sampling period allow direction of input current space vector is controlled as well (for unity displacement factor). Any extra time in the sampling period not occupied by active vectors is filled with zero vectors. Sequence of the 4 active vectors is chosen to minimize commutations. Selection of vector sequence is not unique; the main vector sequences are as Figure 4.4 shows.

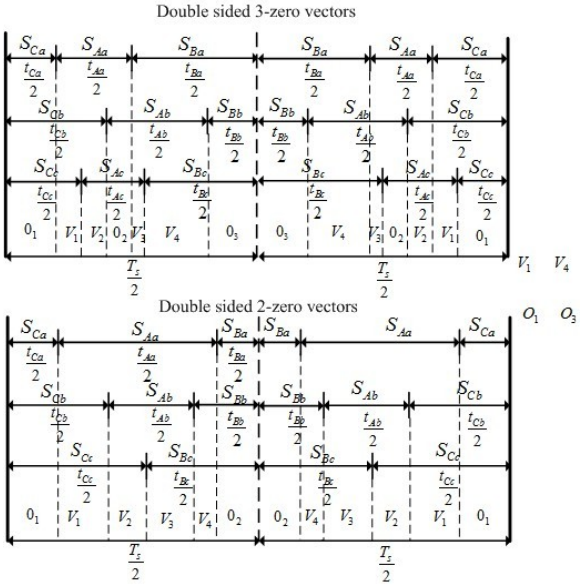


Figure 4.4: The main vector sequences

4.2.2 A unified and simplified carrier-based modulation method for direct matrix converter

This section proposes a unified framework for the carrier-based PWM theory of matrix converter [15]. The matrix converter modulation theory is investigated from the geometric transformation and the SVPWM algorithm for two-level and three-level voltage source

inverter [98][99]. Through a new viewpoint to understand the matrix converter modulation method such as single carrier based modulation technique for two-level VSI and double carrier based modulation technique for three-level VSI, a unified carrier-based modulation method for direct matrix converter is proposed.

The power circuit topology of a three-phase direct matrix converter is shown in Figure 4.1. The unified continuous carrier-based modulation method is composed of single-carrier-based modulation method and double-carrier-based modulation method.

1) Single-carrier-based modulation method In two-level three-phase VSI, the modulation method using offset voltage is that modulation implicit functions of SVPWM can be obtained by adding offset voltage to the modulation implicit functions of SPWM, then compared with carrier triangular waveform, and finally calculates actual gating time for each inverter leg. This method can be extended to the modulation of a direct matrix converter. Similar to two-level three-phase VSI, the single-carrier-based modulation method for matrix converter uses two input line to line voltages during each sampling period and all three phase input voltages are used. Using the concept of offset voltage, the modulation implicit functions of the direct matrix converter can be synthesized, then compared with the single-carrier triangular waveform, and finally the output voltages are obtained.

A) Method I: The carrier-based modulation method I is described in references [96] - [98]. The input three-phase voltages are v_a, v_b, and v_c; MAX, MID, and MIN are correspondingly maximum, medium, and minimum values of v_a, v_b, and v_c. The output three-phase voltages are v_A, v_B, and v_C; Max, Mid, and Min are correspondingly maximum, medium, and minimum values of v_A, v_B, and v_C. The three-phase input reference currents are I_a, I_b, and I_c; I_{MAX}, I_{MID}, and I_{MIN} are correspondingly maximum, medium, and minimum values of I_a, I_b, and I_c. The case that $I_{MAX} - I_{MID} > I_{MID} - I_{MIN}$ is mode I, and $I_{MAX} - I_{MID} <= I_{MID} - I_{MIN}$ is mode II. $H1$ and $L1$ are correspondingly high and low voltage of the input three-phase voltages during the T_1 period, $H1 = MAX$ and $L1 = MIN$

in method I. $H2$ and $L2$ are correspondingly high and low voltage of the input three-phase voltages during the T_2 period. In the case of mode I, $H2 = MAX$ and $L1 = MID$ in method I; and in the case of mode II, $H2 = MID$ and $L1 = MIN$ in method I. v_{z1} and v_{z2} are offset voltages during the T_1 period and T_2 period, respectively. v_{i1}^* and v_{i2}^* are modulation implicit voltage value of phase 'i' during T_1 period and T_2 period, respectively.

The triangular carrier waveform [98] and switching patterns can be described as shown in Figure 4.5. From Figure 4.5, one period of switching time T_s is divided into two parts, T_1 (falling slope of the triangular carrier) and T_2 (rising slope of the triangular carrier). During T_1 period, the carrier changes from nadir to the peak value, and the input line-to-line voltage between maximum and minimum value is used as an imaginary dc-link voltage. During T_2 period, according to the different conditions, the carrier changes from peak to medium value or medium value to nadir, and the input line-to-line voltage between maximum and medium value or between medium and minimum value is used as an imaginary dc-link voltage. The offset voltage (v_{z1} and v_{z2}) of the direct matrix converter is similar to zero voltage vectors in the SVPWM algorithm for two-level VSI. In the SVPWM algorithm for two-level VSI, the zero voltage vectors are calculated to place the modulation implicit functions of SVPWM in the middle of the dc-link voltage. Similar to two-level VSI, the matrix converter offset voltages of the period T_1 and T_2 can be calculated. The offset voltages of the period T_1 and T_2 are obtained by the following equation.

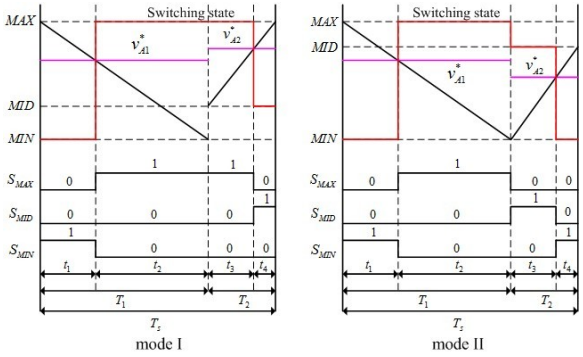


Figure 4.5: Carrier waveform and switching patterns for method I

$$\begin{cases} v_{z1} &= \frac{(H1+L1)-(Max+Min)}{2} \\ v_{z2} &= \frac{(H2+L2)-(Max+Min)}{2} \end{cases} \tag{4.15}$$

The offset voltage v_{z1} locates the modulation implicit voltage references v^*_{a1}, v^*_{b1}, v^*_{c1} in the middle of the input line-to-line voltage between $H1$ and $L1$ during T_1 period. Similar to v_{z1}, v_{z2} does the same function during T_2 period. For the T_1 period, the modulation implicit functions of direct matrix converter are calculated by the following equation.

$$\begin{cases} v^*_{A1} &= v_A + v_{z1} \\ v^*_{B1} &= v_B + v_{z1} \\ v^*_{C1} &= v_C + v_{z1} \end{cases} \tag{4.16}$$

For the T_2 period, the modulation implicit functions of direct matrix converter are as follows:

$$\begin{cases} v^*_{A2} &= v_A + v_{z2} \\ v^*_{B2} &= v_B + v_{z2} \\ v^*_{C2} &= v_C + v_{z2} \end{cases} \tag{4.17}$$

Therefore, the algorithm directly uses the instantaneous values of three-phase output reference voltages to calculate the modulation implicit functions of direct matrix converter. The switching state of phase a is described in Figure 4.5. From Figure 4.5, the modulation implicit functions of direct matrix converter are compared with the carrier triangular waveform, and generate switching states and switching signals to power devices. In the period T_1, the input line-to-line voltage between MAX and MIN is used. Therefore, the switching state of phase a is represented with MAX and MIN. The switching state is MAX when the modulation implicit functions of direct matrix converter bigger than carrier triangular waveform, and conversely, the switching state is MIN when the modulation implicit functions of direct matrix converter smaller than carrier triangular waveform. In the same manner, the switching state in the period T_2 can be investigated.

To improve the waveform of input current, the ratio between T_1 and T_2 can be modified while maintaining the sum of T_1 and T_2 as a fixed sampling period T_s. T_1 and T_2 can be determined by the input voltage angle β_i. The relationship between β_i and $\beta_i^{'}$ is shown in Figure 4.6. The modified period $T_1^{'}$ and $T_2^{'}$ can be obtained by the following equations.

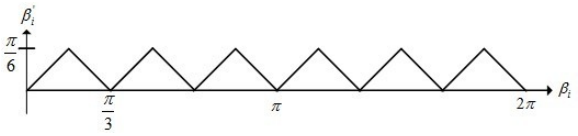


Figure 4.6: Relationship between β_i and $\beta_i^{'}$

$$\begin{cases} T_1 &= \frac{2}{\sqrt{(3)}} \sin(\beta_i^{'} + \frac{2\pi}{3}) \cos(\beta_i^{'}) T_s \\ T_2 &= \frac{2}{\sqrt{(3)}} \sin(\beta_i^{'}) \cos(\beta_i^{'} - \frac{\pi}{3}) T_s \\ T_s &= T_1 + T_2 \end{cases} \tag{4.18}$$

$$\alpha = \frac{H2 - L2}{Max - Min} \tag{4.19}$$

$$\alpha = \min(1, \frac{H2 - L2}{Max - Min}) \tag{4.20}$$

$$\begin{cases} T_2^{'} &= \frac{1}{\alpha} T_2 \\ T_1^{'} &= T_s + T_2 \end{cases} \tag{4.21}$$

$$k_c = \frac{T_2^{'}}{T_1{'}} (1 - \alpha) + 1 \tag{4.22}$$

$$v_{i1}^{'} = k_c v_i \quad i \in (A, B, C) \tag{4.23}$$

$$v_{i2}^{'} = \alpha v_i \quad i \in (A, B, C) \tag{4.24}$$

where α is the scaling factor which restricts output voltage to the available voltage region during T_2; k_c is the scaling factor to compensate output voltage during T_1; $T_1^{'}$ and $T_2^{'}$ are modified period; $v_{i1}^{'}$ and $v_{i2}^{'}$ are output voltage after compensation during T_1 and T_2, respectively.

As shown in Figure 4.6, if the switching state of phase a is MAX, then the load phase a is connected to the input phase whose voltage is MAX, in other words, the switch is turned on when the connected phase voltage is MAX. Similarly, if the switching state of phase a is MID, then the load phase a is connected to the input phase whose voltage is MID, the switch is turned on when the connected phase voltage is MID; if the switching state of phase a is MIN, then the load phase a is connected to the input phase whose voltage is MIN, the switch is turned on when the connected phase voltage is MIN. The other phase b and c can be derived in the same way.

B) Method II: From the above method, the following methods are investigated. The carrier-based modulation method II is similar to the method I. The only difference is that the two methods have different carrier triangular waveforms. The triangular carrier waveform and switching patterns can be described as Figure 4.7 shows.

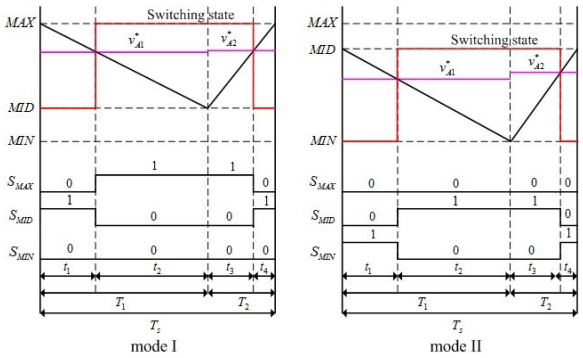


Figure 4.7: Carrier waveform and switching patterns for method II

From Figure 4.7, we can see that high and low voltage of the input three-phase voltages $H1 = MAX$, $L1 = MID$, $H2 = MAX$, and $L2 = MID$ in mode I; $H1 = MID$, $L1 = MIN$, $H2 = MID$, and $L2 = MIN$ in mode II. In the mode I, the carrier waveform can be described from MAX to MID because the input line-to-line voltage between MAX and MID is used as imaginary dc-link voltage. In the mode II, the carrier waveform can be described from MID to MIN because the input line-to-line voltage between MID and MIN is used as imaginary dc-link voltage. The modulation implicit functions of method II for direct matrix converter can be calculated by equations from (4.15) to (4.24).

C) Method III: From the above methods, the following methods are investigated. The carrier-based modulation method III is similar to the method I and method II. The only difference is that the three methods have different carrier triangular waveforms. The triangular carrier waveform and switching patterns can be described as Figure 4.8 shows.

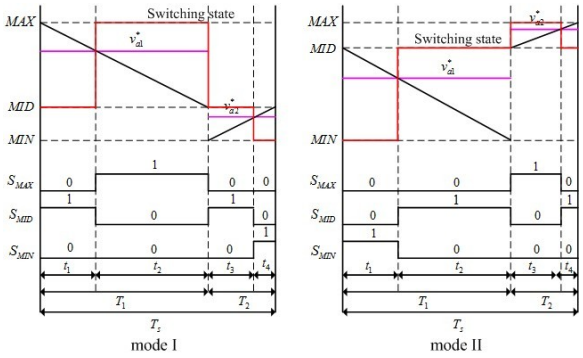


Figure 4.8: Carrier waveform and switching patterns for method III

From Figure 4.8, we can see that high and low voltage of the input three-phase voltages $H1 = MAX$, $L1 = MID$, $H2 = MID$, and $L2 = MIN$ in mode I; $H1 = MID$, $L1 = MIN$, $H2 = MAX$, and $L2 = MID$ in mode II. In the mode I, during T_1 period, the carrier waveform can be described from MAX to MID because the input line-to-line voltage between MAX and MID is used as imaginary dc-link voltage; during T_2 period, the carrier waveform can be described from MID to MIN because the input line-to-line voltage between MID and MIN is used as imaginary dc-link voltage. The carrier waveform in mode II is in contrast with the waveform in mode I. The modulation implicit functions of method III for direct matrix converter can be calculated by equations from (4.15) to (4.24).

D) Method IV: From the above methods, the following method is investigated. The carrier-based modulation method IV is similar to the previous methods. The only difference is that the four methods have different carrier triangular waveforms. The triangular carrier waveform and switching patterns can be described as Figure 4.9 shows.

From Figure 4.9, we can see that high and low voltage of the input three-phase voltages $H1 = MAX$, $L1 = MIN$, $H2 = MAX$, and $L2 = MIN$ in mode I; $H1 = MAX$, $L1 = MIN$, $H2 = MAX$, and $L2 = MIN$ in mode II. In the mode I, the carrier waveform

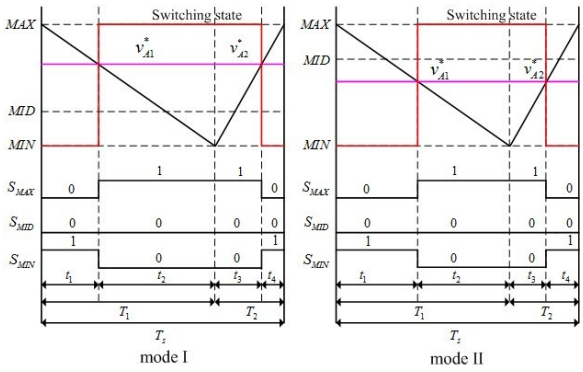


Figure 4.9: Carrier waveform and switching patterns for method IV

can be described from MAX to MIN because the input line-to-line voltage between MAX and MIN is used as imaginary dc-link voltage; in the mode II, the carrier waveform also can be described from MAX to MIN. The modulation implicit functions of method IV for direct matrix converter can be calculated by equations from (4.15) to (4.24).

2) Double-carrier-based modulation method The double-carrier-based modulation method is proposed in reference [99]. Compared to three-phase three-level VSI, it is clear that direct matrix converter in Figure 4.1 is intrinsically similar to three-phase three-level VSI. The differences are that the three-phase input voltages of thee-level inverter are dc and constant, while those of matrix converters are sinusoidal waveforms; thee-level inverter have 12 power switches, while direct matrix converter have 9 power switches. Therefore, double-carrier based modulation method presents a new viewpoint to consider the matrix converter as a three-level inverter and apply the modulation algorithm of three-level inverter to the matrix converter. The PWM switching signals can be generated using a well established double-carrier-based modulation method for three-level inverter, as shown in Figure 4.10. The general direct form of voltage equation of matrix converter is given by the following formula.

$$\begin{Bmatrix} v_A' \\ v_B' \\ v_C' \end{Bmatrix} = \begin{Bmatrix} v_A + v_z \\ v_B + v_z \\ v_C + v_z \end{Bmatrix} = \begin{Bmatrix} m_{11} & m_{12} & m_{13} \\ m_{21} & m_{22} & m_{23} \\ m_{31} & m_{32} & m_{33} \end{Bmatrix} * \begin{Bmatrix} v_a \\ v_b \\ v_c \end{Bmatrix} \tag{4.25}$$

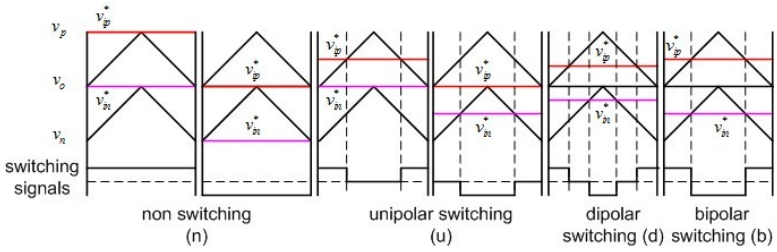


Figure 4.10: Double-carrier based PWM for generating switching signals

where m_{ij}, $i \in (1,2,3)$, $j \in (1,2,3)$ is the modulation matrix, and v_z is the injected zero voltage.

The two modulation implicit functions of matrix converter v_{ip}^*, v_{in}^* in the double-carrier-based PWM are obtained by formula (4.25).

$$\left\{ \begin{array}{c} v_{ip}^* \end{array} \right\} = \left\{ \begin{array}{c} m_{11} \\ m_{21} \\ m_{31} \end{array} \right\} = \left\{ \begin{array}{c} m_{11}^{'} + X \\ m_{21}^{'} + X \\ m_{31}^{'} + X \end{array} \right\} \geq \left\{ \begin{array}{c} 0 \end{array} \right\} \tag{4.26}$$

$$\left\{ \begin{array}{c} v_{in}^* \end{array} \right\} = \left\{ \begin{array}{c} -m_{13} \\ -m_{23} \\ -m_{33} \end{array} \right\} = \left\{ \begin{array}{c} -m_{13}^{'} - Z \\ -m_{23}^{'} - Z \\ -m_{33}^{'} - Z \end{array} \right\} \leq \left\{ \begin{array}{c} 0 \end{array} \right\} \tag{4.27}$$

where $i \in (A,B,C)$, X and Z are zero voltage vectors.

For unity input power factor, the two modulation implicit functions of matrix converter are calculated by the following equations.

$$v_{ip}^* = \frac{MAX}{MAX^2 + MID^2 + MIN^2} v_i + X \quad i \in (A,B,C) \tag{4.28}$$

$$v_{in}^* = -\frac{MIN}{MAX^2 + MID^2 + MIN^2} v_i - Z \quad i \in (A,B,C) \tag{4.29}$$

Formulas (4.28) and (4.29) indicate the two modulation implicit functions of matrix converter are proportional to the desired output voltages, and shifted by two zero voltage vectors. This

is similar to the simplified SVPWM algorithm for two-level and three-level VSI, except that matrix converter has more freedom in construction of the output voltages.

Similar to the SVPWM algorithm for three-level inverter, adding zero voltage vectors results in shifting the two modulation implicit functions v_{ip}^{*}, v_{in}^{*} up or down within the range of the upper and lower carrier waves. The allowable ranges of the zero voltage vectors are as follows:

$$\begin{cases} -\min(m_{11}^{'}, m_{21}^{'}, m_{31}^{'}) & \leq X \leq 1 - \max(m_{11}^{'}, m_{21}^{'}, m_{31}^{'}) \\ -\min(m_{12}^{'}, m_{22}^{'}, m_{32}^{'}) & \leq Y \leq 1 - \max(m_{12}^{'}, m_{22}^{'}, m_{32}^{'}) \\ -\min(m_{13}^{'}, m_{23}^{'}, m_{33}^{'}) & \leq Z \leq 1 - \max(m_{13}^{'}, m_{23}^{'}, m_{33}^{'}) \\ X + Y + Z & = 1 \end{cases} \tag{4.30}$$

where min and max are correspondingly minimum and maximum values.

The injection of two zero voltage vectors can be considered as zero voltage vectors in three-level inverter. The upper and lower modulation implicit functions can be shifted independently by adding zero voltage vectors. As Figure 4.10 shows, the PWM switching pattern for each output phase can be either none (n), unipolar (u), dipolar (d), or bipolar (b) switching. If the PWM switching patterns for three output phases are three dipolar [3d] conditions as shown in Figure 4.11, then the zero voltage vectors can be calculated by the following formula which is similar to three-level inverter.

$$\begin{cases} X & = \frac{1 - max_x + min_x}{2} \\ Z & = \frac{1 - max_z + min_z}{2} \\ Y & = 1 - X - Z \end{cases} \tag{4.31}$$

where max_x and min_x are maximum and minimum values of $m_{11}^{'}$, $m_{21}^{'}$, $m_{31}^{'}$; max_z and min_z are maximum and minimum values of $m_{13}^{'}$, $m_{23}^{'}$, $m_{33}^{'}$.

If the PWM switching patterns for three output phases are [1b1u1d] condition as shown in Figure 4.11, if the maximum value of the absolute value of three phase input voltages equal to the maximum value of three phase input voltages ($MAX = maximum(|v_a|, |v_b|, |v_c|)$),

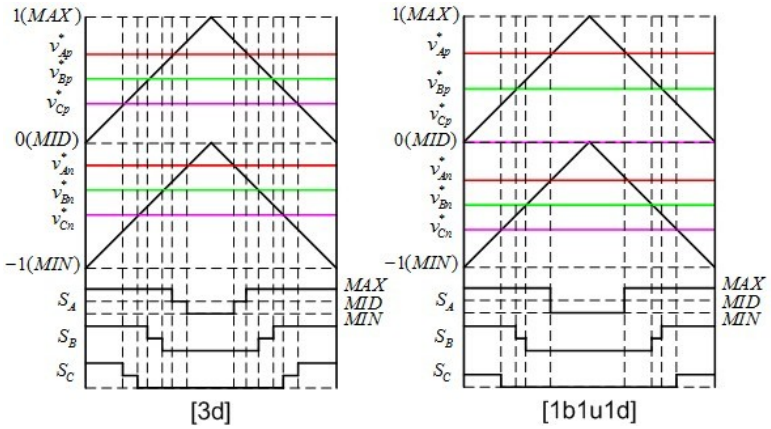


Figure 4.11: One period of PWM switching signals for [3d] and [1b1u1d]

then the zero voltage vectors are as follows:

$$\begin{cases} X &= -min_x \\ Y &= -min_y \\ Z &= 1 - X - Y \end{cases} \tag{4.32}$$

where min_y is minimum value of $m_{12}^{'}$, $m_{22}^{'}$, $m_{32}^{'}$.

If the maximum value of the absolute value of three phase input voltages equal to the absolute value of minimum value of three phase input voltages ($|MIN| = maximum(|v_a|, |v_b|, |v_c|)$), then the zero voltage vectors are as follows:

$$\begin{cases} X &= -min_x \\ Z &= 1 - max_z \\ Y &= 1 - X - Z \end{cases} \tag{4.33}$$

The switching state is MAX when v_{ip} bigger than upper carrier triangular waveform, the switching state is MID when v_{ip} smaller than upper carrier triangular waveform and v_{in} bigger than lower carrier triangular waveform, and the switching state is MIN when v_{in} smaller than lower carrier triangular waveform. There are three possible arrangements of the phase sequence, Figure 4.11 is the mid-phase reference [99]. The other two phase references

are similar to mid-phase reference, so they are not described in this paper. In Figure 4.11, S_A, S_B, and S_C are switching signals of three-phase switches.

4.2.3 A simplified and unified discontinuous carrier-based modulation method

The method of clamping input voltage of phase leg to the output bus is called DPWM. As compared to CPWM strategies, reduction of switching losses is frequently achieved by adoption of DPWM schemes. Carrier-based DPWM methods for matrix converter are investigated. In the discontinuous PWM methods, zero sequence signals are discontinuous. During each sampling period, one of the phases ceases modulation and the associated phase is clamped to the positive bus or the negative bus. Hence, the switching losses of the associated inverter legs are eliminated. The simplified and unified discontinuous carrier-based modulation method for direct matrix converter is obtained from the simplified and unified continuous carrier-based modulation method, as section 4.2.3 described [15]. Similar to the continuous carrier-based modulation method, discontinuous carrier-based modulation method is also composed of single-carrier-based modulation method and double-carrier-based modulation method.

1) Single-carrier-based modulation method A) Method I: As Figure 4.12 shows,

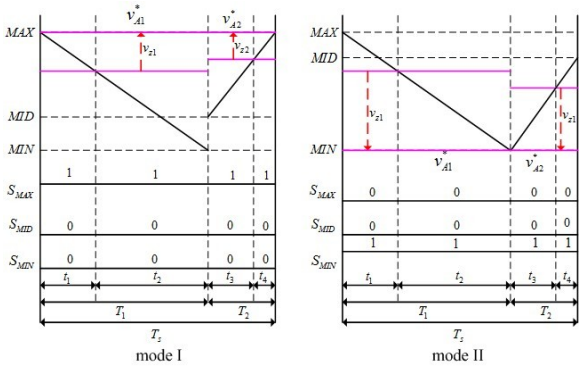


Figure 4.12: Modified zero voltage vectors and switching patterns for method I

DPWM can be implemented by modifying the zero voltage vectors which is similar to

DSVPWM in the VSI. For mode I, the zero voltage vectors are as follows:

$$v_{z1} = v_{z2} = MAX - Max \tag{4.34}$$

For mode II,

$$v_{z1} = v_{z2} = MIN - Min \tag{4.35}$$

B) Method II: As Figure 4.13 shows, the modulation implicit functions tend to MAX and

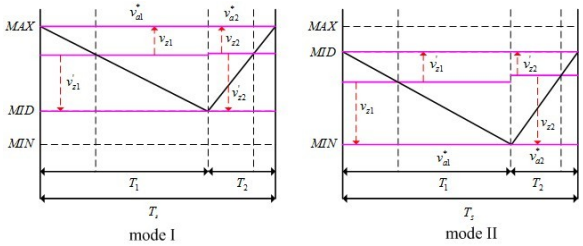


Figure 4.13: Modified zero voltage vectors for method II

MIN, the zero voltage vectors can be obtained using equations (4.34) and (4.35). The modulation implicit functions tend to MID, for mode I, the zero voltage vectors is as follows:

$$v_{z1} = v_{z2} = -MIN + Min \tag{4.36}$$

For mode II,

$$v_{z1} = v_{z2} = -MAX + Max \tag{4.37}$$

C) Method III: As Figure 4.14 shows, the modulation implicit functions tend to MID, the

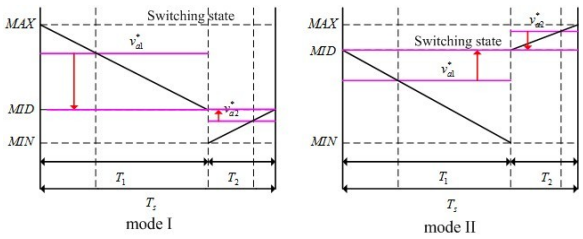


Figure 4.14: Modified zero voltage vectors for method III

zero voltage vectors can be obtained using equations (4.36) and (4.37). For mode I, using

equation (4.37) in T_1 period and using equation (4.36) in T_2 period. For mode II, using equation (4.36) in T_1 period and using equation (4.37) in T_2 period.

D) Method IV: As Figure 4.15 shows, the modulation implicit functions tend to MAX,

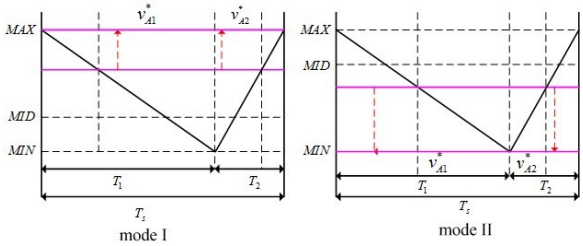


Figure 4.15: Modified zero voltage vectors for method IV

the zero voltage vectors can be obtained using equation (4.34); the modulation implicit functions tend to MIN, the zero voltage vectors can be obtained using equation (4.35).

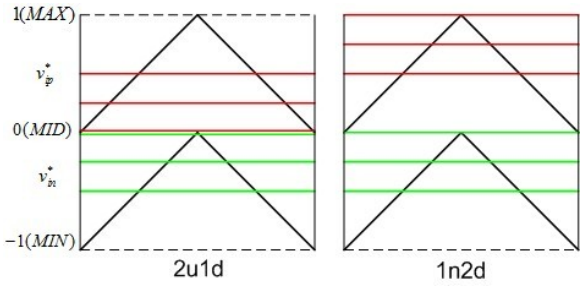


Figure 4.16: Three phase modulation implicit functions and corresponding PWM modes

2) Double-carrier-based modulation method As Figure 4.16 shows, DPWM can be implemented by modifying the zero voltage vectors which is similar to DPWM in the VSI. Each DPWM methods [2u1d], [1n2d] in Figure 4.19 uses zero voltage vectors differently. For [2u1d], the zero voltage vectors can be calculated by the following equation.

$$\begin{cases} X &= -min_x \\ Z &= -min_z \\ Y &= 1 - X - Z \end{cases} \tag{4.38}$$

For [1n2d], if $MAX = maximum(|v_a|, |v_b|, |v_c|)$, then the zero voltage vectors are as follows:

$$\begin{cases} X & = 1 - max_x \\ Z & = -min_z \\ Y & = 1 - X - Z \end{cases} \tag{4.39}$$

If $|MIN| = maximum(|v_a|, |v_b|, |v_c|)$, then the zero voltage vectors are as follows:

$$\begin{cases} X & = -min_x \\ Z & = 1 - max_z \\ Y & = 1 - X - Z \end{cases} \tag{4.40}$$

4.3 Control technique for direct matrix converter

4.3.1 Commutation method

1) Switch configuration As mentioned above, the realization of the direct matrix converter requires bi-directional switches which must be able to conduct positive and negative currents and must be able to block positive and negative voltages. There are 4 possible switch configurations which are diode bridge switch, common emitter switch, common collector switch, and reverse blocking IGBT switch [100].

The diode bridge switch is obtained by 4 diodes and 1 IGBT, as Figure 4.17 shows. The characteristics of diode bridge switches are high conduction losses (two diodes and a power switches conducting) and only one power device per switch.

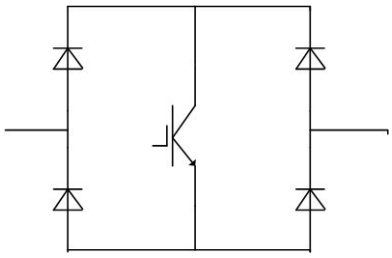


Figure 4.17: Diode embedded bi-directional switch

The common emitter switch is obtained by 2 diodes and 2 IGBTs, pair of switching devices arranged with emitters are connected, as Figure 4.18 shows. The characteristics of

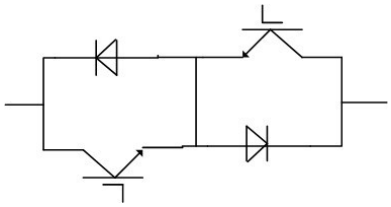


Figure 4.18: The common emitter switch

common emitter switches are both devices can be gated from the same isolated power supply and can control direction of current flow within each switch which is useful for most current commutation strategies.

The common emitter switch is obtained by 2 diodes and 2 IGBTs, pair of switching devices arranged with collectors are connected, as Figure 4.19 shows. The characteristics of

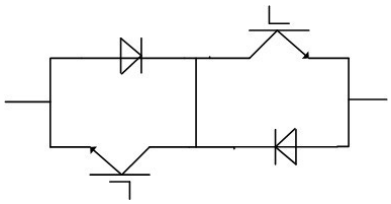


Figure 4.19: The common emitter switch

common collector switches are the direction of current through the active switching devices can be controlled and lower conduction losses compared to the diode bridge switches due to only two devices are conducting at any given time.

The reverse blocking IGBT switch is obtained by 2 pair of reverse blocking IGBTs, as Figure 4.20 shows. The characteristics of reverse blocking IGBT switches are lower conduction losses, can control direction of current flow within each switch, reverse recovery can be an issue and may lead to higher switching losses.

2) Commutation method Achieving proper commutation between switches in matrix converter is more difficult than a conventional VSI since there are no natural freewheeling

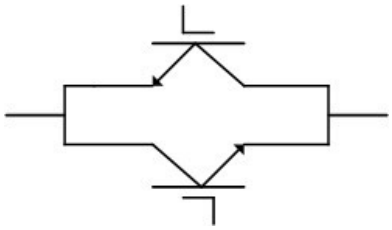


Figure 4.20: The reverse blocking IGBT switch

paths. As mentioned above, there are two basic rules restrict commutation. Rule 1 is that no two bi-directional switches are switched on at any one time, as shown in figure 4.24; rule 2 is that no two bi-directional switches are switched off at any one time, as shown in Figure 4.21. Rule 1 results in line-to-line short circuit and destroy the matrix converter due to over current. Rule 2 results in the absence of a path for the inductive load current and causing large over-voltages. There are many commutation methods.

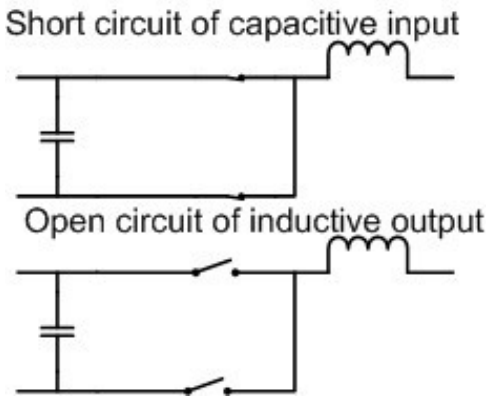


Figure 4.21: Basic rules for safe operation of the matrix converter

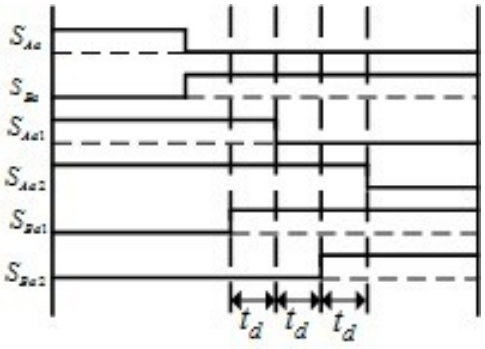


Figure 4.22: Four-step current commutation

Among several methods, the four-step current commutation is the most popular methods and one of the first methods that successfully switched matrix converter. As Figure 4.22 shows, there are four steps and four switches need to be individually controlled. Four-step current commutation has characteristics like reduction in device losses, increase in gate drive complexity to allow independent control of devices, control logic complexity, and require knowledge of output current direction in each output line.

4.3.2 Dead time compensation

In practical applications, switching devices have finite (non-zero) turn-on and turn-off times. The dead time introduces a voltage error at the matrix converter phase terminal. This error is dependent on the polarity of phase current. The voltage error increases output voltage harmonic components and decreases control performance. Therefore, dead time compensation is desirable. Through analysis of dead time effect, deviations of voltage vectors caused by dead time effect are dependent on the direction of output currents [107] - [109]. The voltage distortion increases harmonic components of output voltage and decreases control performance. Combined with the characteristics of carrier-based modulation method, to avoid determining the direction of output currents, a compensation method for dead time effect is suggested. The value of dead time is adjusted on-line by the value of corresponding phase current. The deviations of voltage vectors caused by dead time effect are directly compensated to three phase reference voltages.

The power circuit topology of a three-phase direct matrix converter is shown in Figure 4.1. To avoid short circuit of the power supply and open circuit of the load, there are many commutation methods. Among several methods, the four-step current commutation method is studied as an example. The commutation method is highly related to the modulation method. Define current flowing to the voltage source as positive polarity. The dead-time effect on the output voltage can best be examined from one phase of the matrix converter, as illustrated in Figure 4.23. In the picture, v_{max}, v_{mid}, v_{min} indicate maximum, medium,

and minimum voltage of the power supply. The four step commutation method is shown in Figure 4.24.

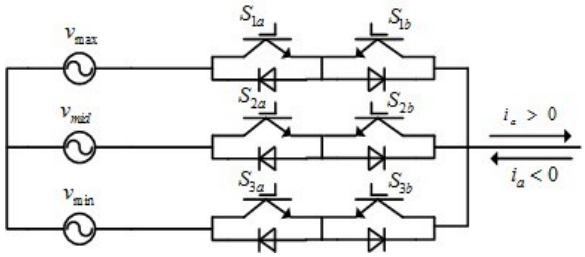


Figure 4.23: One phase of direct matrix converter

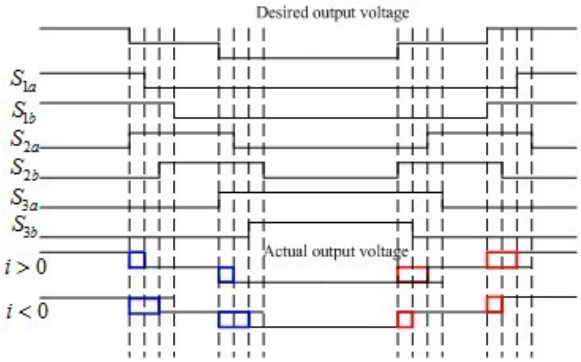


Figure 4.24: Output voltage error using four-step commutation

The loss of terminal voltage of phase a over one PWM period is given by [16]:

$$V_{DT\_a} = \frac{T_{DT\_a}}{T_s}(v_{max} - v_{min}) \tag{4.41}$$

Voltage losses of phases b and c can be derived in similar fashion. Through the above analysis, from Figure 4.24, we can get the average voltage loss caused by dead time in one PWM period.

$$V_{DT} = \frac{T_{DT}}{T_s}(v_{max} - v_{min})\text{sgn}(i) \tag{4.42}$$

where i is output current, and $\text{sgn}(i) = \begin{cases} 1 & i > 0 \\ -1 & i < 0 \end{cases}$. Therefore, the actual three phase output voltages are as follows:

$$V_j' = V_j - \frac{T_{DT\_j}}{T_s}(v_{max} - v_{min})\text{sgn}(i_j) \quad j \in (a, b, c) \tag{4.43}$$

The disturbance voltage vector, which accounts for all three phases′ voltage drops caused by dead time is given by:

$$\begin{cases} \Delta V &= -\frac{(v_{max} - v_{min})}{T_s}[T_{DT\_a}\text{sgn}(i_a) \\ & +e^{j\frac{2\pi}{3}}T_{DT\_b}\text{sgn}(i_b) + e^{j\frac{4\pi}{3}}T_{DT\_c}\text{sgn}(i_c)] \end{cases} \tag{4.44}$$

Dead time effect increases harmonic components of output voltage and current, and changes the phase angle between voltage and current. Similar to two-level three-phase VSI, the dead time compensation includes pulse time compensation and voltage compensation method. Pulse time compensation method is identical to the method of VSI. Voltage compensation method is also similar to the method of VSI.

Average voltage loss caused by dead time in one PWM period is given by:

$$V_{DT\_j} = \frac{(v_{max} - v_{min})}{T_s}ki_j \quad j \in (a, b, c) \tag{4.45}$$

The disturbance voltage vector, which accounts for all three phases′ voltage drops caused by dead time is given by:

$$\Delta V = \frac{(v_{max} - v_{min})}{T_s}k(i_a + e^{j\frac{2\pi}{3}}i_b + e^{j\frac{4\pi}{3}}i_c) \tag{4.46}$$

From equation (4.46), we can see that the disturbance of voltage vector have no relationship with the direction of output current. In the voltage compensation method, the direction of current is not required to compensate the dead time effect. Voltage loss of each phase caused

by dead time can be directly compensated to three phase input voltages.

$$v_j^{'} = v_j + V_{DT\_j} \quad j \in (a, b, c) \tag{4.47}$$

4.3.3 Unbalanced three-phase control and energy feedback control

1) Unbalanced three-phase control

The unbalanced three-phase control is similar to the two-level three-phase VSI. The only difference is that VSI has unbalanced three-phase grid voltage while direct matrix converter has unbalanced three-phase grid voltage and unbalanced input three-phase source voltage. On the basis of simplified carrier-based modulation method, the concept of voltage modulation by using offset voltage is applied to an unbalanced three-phase voltage control method. The algorithm is based on simple control structure and does not demand any filter for obtaining symmetrical components, e.g. notch or anti-resonant filter. The control objective is to balance three phase output currents and minimize THD of the output currents without ac current sensors under unbalanced grid voltage conditions and unbalanced input three-phase source voltage. The attractive advantage of this control is the possibility of effective operation under both balanced and unbalanced conditions. The balanced three phase voltages after compensation of zero sequence voltage are still balanced three phase voltages, and the unbalanced three phase voltages can be made balanced after compensation of zero sequence voltage. The new set of voltages after compensation method are used as new three phase voltages and used for formula (4.16).

2) Energy feedback control

In this direct matrix converter, the static indirect current control method (phase and amplitude control method) is proposed and studied. The energy feedback control method for direct matrix converter is identical to the energy feedback control method for VSI.

Vector graphics are shown as Figure 3.9. This dissertation only analyses relationship between variables in the case of unity power factor feedback. Phase angle is obtained by the

formula (3.21) and modulation index is obtained by the formula (3.23). We can calculate angle σ and ratio of pulse width modulation M using equations (3.21) and (3.23) as long as grid voltage E_a, dc bus voltage V_{dc}, and feedback current are determined. The desired output voltages are directly used for simplified SVPWM algorithm to control power switches to track the desired output currents. Through the phase and amplitude control theory we can achieve unity power factor control of energy feedback if we know σ and M.

Chapter 5

Indirect matrix converter

5.1 Introduction

The indirect matrix converter (IMC) topology is the physical implementation of the indirect modulation method [110][111]. As shown in Figure 1.5(b), the indirect matrix converter consists of a four-quadrant current source rectifier and a two-level voltage source inverter. This converter topology is able to produce input and output waveforms with the same quality as the direct matrix converter. In some applications, the indirect matrix converter may be preferred to the direct matrix converter due to simpler and safer commutation of switches [110], the possibility of further reducing the required number of power semiconductor switches [111] - [113] and the possibility to construct complex converter topology with multiple input and output ports [112].

As shown in Figure 1.5(b), the rectification stage is a three-phase to two-phase matrix converter formed with six bi-directional switches so that the indirect matrix converter topology is able to perform the four-quadrant operation like the direct matrix converter. The input side of indirect matrix converter has two mutually anti-parallel current link PWM rectifier stages and the output side of indirect matrix has PWM inverter stages. The simultaneous turn-on of two four-quadrant switches of the upper or the lower bridge halves would lead to a short circuit of two main phases and must therefore be avoided.

Indirect matrix converter family includes two-level indirect matrix converter, two-level sparse matrix converter, two-level very sparse matrix converter, two-level ultra sparse matrix converter, three-level output stage matrix converter, and indirect three-level sparse matrix converter [114][115].

The variant of an IMC shown in Figure 5.1 is called a sparse matrix converter (SMC also known as the swiss matrix converter). A more comprehensive simplification of the circuit topology is possible by limiting the converter to unidirectional power flow. The variant of an IMC shown in Figure 5.2 is called ultra sparse matrix converter (UMC also known as the unidirectional swiss matrix converter). The very sparse matrix converter (VSMC) shown in Figure 5.3, whose four-quadrant switches, cannot be controlled separately according to the current direction. For the IMC, the output stage is a two-level PWM inverter. If the output

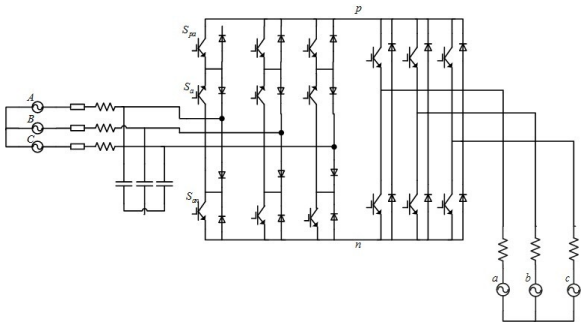


Figure 5.1: The circuit topology of SMC

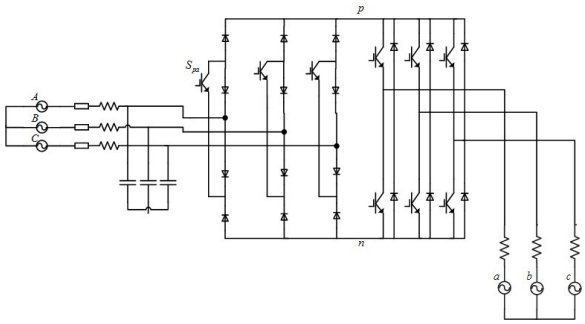


Figure 5.2: The circuit topology of UMC

stage is a three-level PWM inverter, as Figure 5.4 shows, the topology become three-level output stage indirect matrix converter. The variant of the three-level output stage indirect matrix converter shown in Figure 5.5 is called indirect three-level sparse matrix converter circuit. The following parts investigate and study direct SVPWM method and carrier based modulation method, propose and investigate a unified carrier based modulation method for

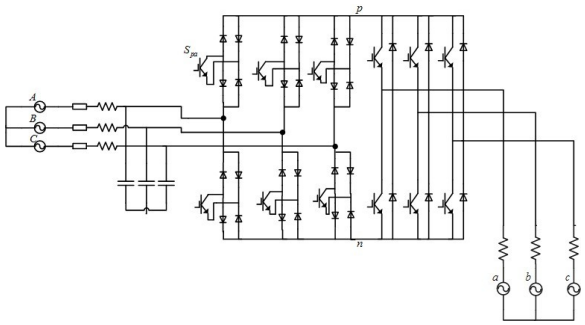


Figure 5.3: The circuit topology of VSMC

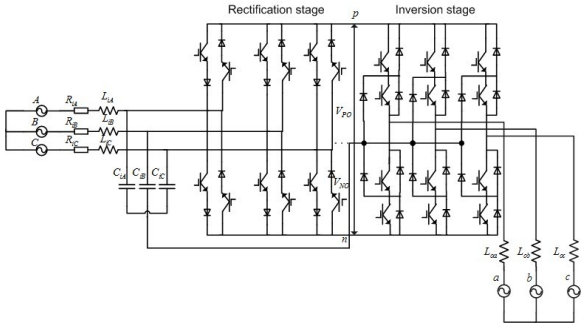


Figure 5.4: The schematic diagram of the three-level-output-stage matrix converter

indirect matrix converter. The control methods such as dead time compensation, unbalanced three-phase control, and energy feedback control are also proposed and studied.

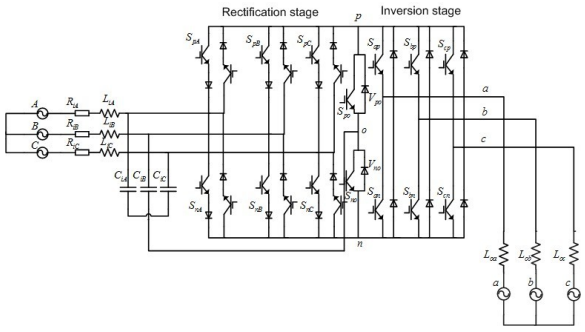


Figure 5.5: The schematic diagram of the indirect three-level sparse matrix converter

5.2 Modulation method for indirect matrix converter

5.2.1 Traditional SVPWM for two-level indirect matrix converter

In order to generate a set of balanced and sinusoidal input and output waveforms, the indirect matrix converter is modulated in such a way that the rectification stage and inversion stage are individually modulated by using SVPWM. In each stage, SVPWM produces a combination of vectors to synthesize a reference vector [116] - [119].

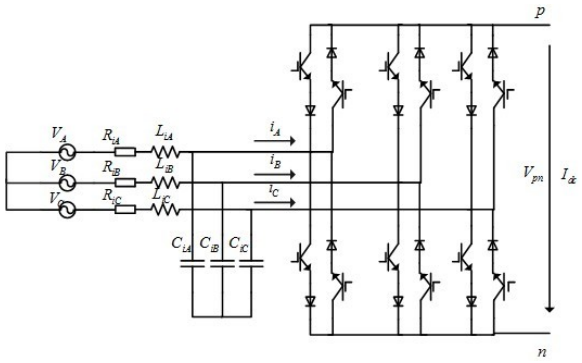


Figure 5.6: The current source rectifier loaded by a dc current generator

1) Rectification stage As Figure 5.6 shows, due to the inductive nature of typical load and the high switching frequency operation, the output current, i_p, is assumed constant for each switching period. To prevent a short circuit in the input lines, the following restriction is required.

$$S_{qA} + S_{qB} + S_{qC} = 1 \qquad q \in (p, n) \tag{5.1}$$

where S_{qk} is the switching state of a bi-directional switch.

All valid switching combinations of the rectifier and their generated voltages and currents are presented at Table 5.1. To maintain a set of input currents with controllable displacement angle with respect to the input voltages, the input currents have to be synchronized with the input voltages. By using the space vector transformation, reference input current space

vector $\vec{I_{in}}$ can be expressed as

$$\vec{I_{in}} = I_{im}e^{j(\omega_i t - \phi_i)} = I_{im}\angle\theta_i \tag{5.2}$$

where I_{im} is the magnitude, ω_i is angular frequency, and ϕ_i is the displacement angle of the input currents with respect to the input voltages.

Nine switching states form nine current vectors in the vector space, wherein the vector I_0 coincides with the origin of coordinates. Nine current vectors divide plane into six sectors, as Figure 5.7 shows. Similar to traditional SVPWM for two-level VSI, to determine the involved voltage vectors, first determine sector number in which vector V_{ref} falls. For example, if V_{ref} falls into the first sector, as Figure 5.7 shows, the reference current vector can be synthesized by two adjacent effective vectors (I_γ and I_δ) and zero current vector (I_0). The output line voltages in all six sectors are listed in Table 5.2. For a switching period, T_s, the reference vector can be synthesized as below:

$$\vec{I_{in}} = d_\gamma I_\gamma + d_\delta I_\delta \tag{5.3}$$

Switching state	Output voltages	Input currents
$S_{pA}, S_{pB}, S_{pC}, S_{nA}, S_{nB}, S_{nC}$	V_p, V_n, V_{pn}	i_A, i_B, i_C
$1,0,0,0,0,1$	V_A, V_C, V_{AC}	$i_p, 0, -i_p$
$0,1,0,0,0,1$	V_B, V_C, V_{BC}	$0, i_p, -i_p$
$0,1,0,1,0,0$	V_B, V_A, V_{BA}	$-i_p, i_p, 0$
$0,0,1,1,0,0$	V_C, V_A, V_{CA}	$-i_p, 0, i_p$
$0,0,1,0,1,0$	V_C, V_B, V_{CB}	$0, -i_p, i_p$
$1,0,0,0,1,0$	V_A, V_B, V_{AB}	$i_p, -i_p, 0$
$1,0,0,1,0,0$	$V_A, V_A, 0$	$0,0,0$
$0,1,0,0,1,0$	$V_B, V_B, 0$	$0,0,0$
$0,0,1,0,0,1$	$V_C, V_C, 0$	$0,0,0$

Table 5.1: 3×3 matrix converter stationary and zero switching combinations

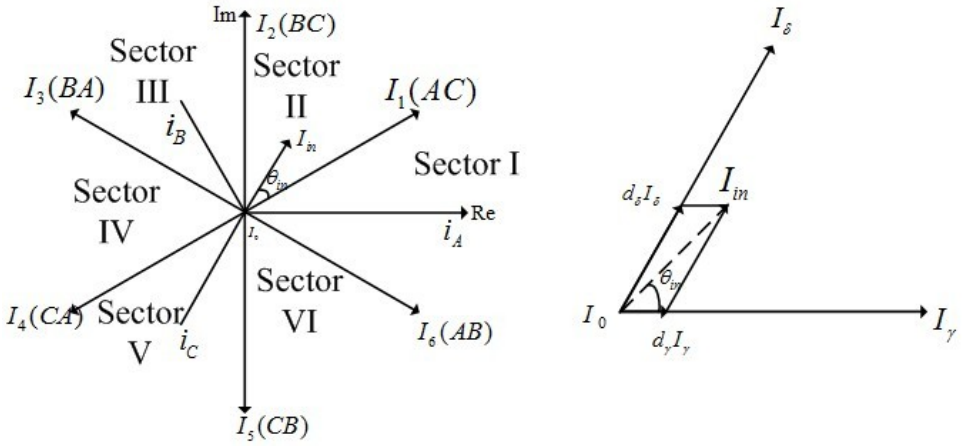


Figure 5.7: Current sector number

where d_γ and d_δ are the duty cycles of two adjacent current vectors (I_γ and I_δ) within the switching period. These duty cycles are calculated by the following equation.

$$\begin{cases} d_\gamma = m_R \sin(\frac{\pi}{3} - \theta_{in}) \\ d_\delta = m_R \sin(\theta_{in}) \end{cases} \tag{5.4}$$

where m_R is the modulation index of the rectifier, and θ_{in} is the angle of the reference vector within the sector.

$$0 \leq m_R = \frac{I_{im}}{i_p} \leq 1 \tag{5.5}$$

Sector	0	1	2	3	4	5
$\gamma - sequence:$	AC	BC	BA	CA	CB	AB
V_p	V_A	V_B	V_B	V_C	V_C	V_A
V_N	V_C	V_C	V_A	V_A	V_B	V_B
$V_{line-\gamma}$	V_{AC}	V_{BC}	V_{BA}	V_{CA}	V_{CB}	V_{AB}
$\delta - sequence:$	AB	AC	BC	BA	CA	CB
V_p	V_A	V_A	V_B	V_B	V_C	V_B
V_n	V_B	V_C	V_C	V_A	V_A	V_B
$V_{line-\delta}$	V_{AB}	V_{AC}	V_{BC}	V_{BA}	V_{CA}	V_{CB}

Table 5.2: Output phase voltage and line to line voltage

By determining the duty cycles d_γ and d_δ, the duty cycle of the zero current vector, I_0, can be determined as follows.

$$d_0 = 1 - d_\gamma - d_\delta \tag{5.6}$$

2) Inversion stage The inversion stage is similar to two-level three-phase VSI that supplied with a dc-link. To prevent a short circuit in the input side, the following restriction is required.

$$S_{jp} + S_{jn} = 1 \qquad j \in (a, b, c) \tag{5.7}$$

where S_{jp} and S_{jn} are the switching functions of the upper and lower power switches, respectively. There are eight kinds of switching states and eight switching states formed eight voltage vectors in the space (as shown in Table 2.3) wherein the vector V_0 and V_7 are equal, they coincide with the origin of coordinates. Eight voltage vectors divide plane into six sectors, as Figure 5.8 shows. To determine the involvement voltage vectors, first determine sector number in which sector V_{ref} falls. For example, if V_{ref} falls into the first sector, as Figure 5.8 shows, the reference voltage vector can be synthesized by two adjacent effective vectors (V_α and V_β) and zero current vector (V_0). For a switching period, T_s, the reference

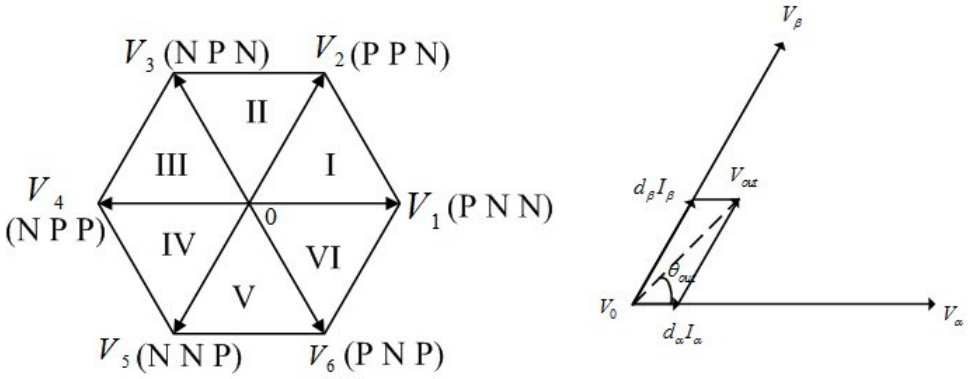


Figure 5.8: Switching states and voltage vectors

vector can be synthesized as below:

$$\vec{V_{out}} = d_\alpha V_\alpha + d_\beta V_\beta \tag{5.8}$$

The duty cycles d_α and d_β are obtained by the following equation.

$$\begin{cases} d_\alpha = m_I \sin(\frac{\pi}{3} - \theta_{out}) \\ d_\beta = m_I \sin(\theta_{out}) \end{cases} \tag{5.9}$$

where m_I is the modulation index of the voltage source inverter and θ_{out} is the angle of the reference vector within the sector.

$$0 \leq m_I = \sqrt{3}\frac{V_{om}}{V_{pn}} \leq 1 \tag{5.10}$$

By determining the duty cycles d_α, and d_β, the duty cycle of the zero voltage vector, v_0, can be determined as follows.

$$d_0 = 1 - d_\alpha - d_\beta \tag{5.11}$$

3) Synchronization between the rectification and inversion stages For the indirect matrix converter topology, the rectification stage is modulated to supply maximum average dc-link voltage so that maximum overall voltage transfer ratio can be obtained. The modulation index for the rectification stage, m_R, is set to unity and the displacement factor is controlled to zero. To simplify the overall modulation, removing the zero current vectors from rectification stage, hence, the switching sequence of rectification stage only consists of the two adjacent current vectors. To maintain duty cycle proportion, the duty cycles of rectification stage are then adjusted by the following equation.

$$\begin{cases} d_\gamma^R = \frac{d_\gamma}{d_\gamma + d_\delta} \\ d_\delta^R = \frac{d_\delta}{d_\gamma + d_\delta} \end{cases} \tag{5.12}$$

Due to the zero current vector cancellation, the average dc-link voltage is calculated by the following equation:

$$V_{pn\_avg} = d_\gamma^R V_{l-l\gamma} + d_\delta^R V_{l-l\delta} \tag{5.13}$$

The modulation on the inversion stage controls the overall voltage transfer ratio due to the unity rectifier modulation index. The modulation index of inversion stage is obtained by the following formula.

$$m_I = \frac{\sqrt{3}V_{om}}{V_{pn\_avg}} \tag{5.14}$$

Combining rectification stage and inversion stage, by selecting appropriate vectors, uniformly, producing a switching pattern shown in Figure 5.9 and Figure 5.10. In Figure 5.9, the duty cycles (d_γ^R, d_δ^R)of two adjacent current vectors are obtained by using equation (5.12), then switching pattern is obtained by combining rectification stage and inversion stage, finally using equation (5.15) calculates each duty cycle. In Figure 5.10, the time interval for each vector is obtained by using Figure 5.9 and equations (5.9) and (5.11). The duty cycles

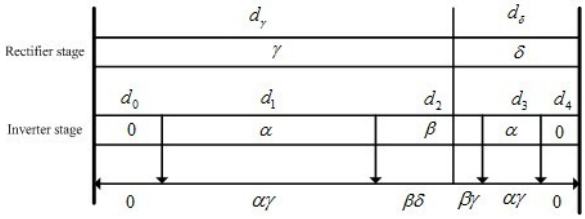


Figure 5.9: Switching pattern

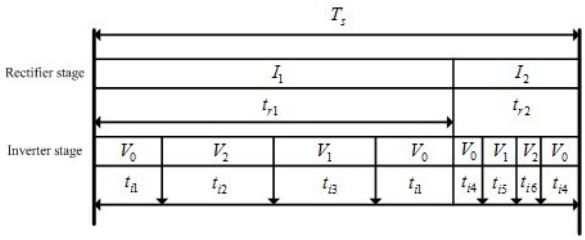


Figure 5.10: The switching pattern of the indirect matrix converter

in the Figure 5.9 are determined by the following equations.

$$\begin{cases} d_0 = d_\gamma^R[1-(d_\gamma+d_\delta)(d_\alpha+d_\beta)] \\ d_1 = d_\gamma d_\alpha \\ d_2 = (d_\gamma+d_\delta)d_\beta \\ d_3 = d_\delta d_\alpha \\ d_4 = d_\delta^R[1-(d_\gamma+d_\delta)(d_\alpha+d_\beta)] \end{cases} \tag{5.15}$$

The time interval for each vector in the Figure 5.10 can be determined by the following equations:

$$\begin{cases} t_{r1} = d_\gamma^R T_s \\ t_{i1} = 0.5 d_\gamma^R d_0 T_s \\ t_{i2} = d_\gamma^R d_\beta T_s \\ t_{i3} = d_\gamma^R d_\alpha T_s \\ t_{i4} = 0.5 d_\delta^R d_0 T_s \\ t_{i5} = d_\delta^R d_\alpha T_s \\ t_{i6} = d_\delta^R d_\beta T_s \end{cases} \tag{5.16}$$

The traditional SVPWM for two-level sparse matrix converter, two-level very sparse matrix converter, and two-level ultra sparse matrix converter are the same with the SVPWM method for two-level indirect matrix converter. The only difference is that the final switching signals are different. Therefore, the description of the traditional SVPWM for two-level sparse matrix converter, two-level very sparse matrix converter, and two-level ultra sparse matrix converter are not presented in this dissertation. The traditional SVPWM method for indirect three-level output stage matrix converter is proposed and investigated in references [115][120] - [123]. In order to make the multi-level matrix converter concept attractive in industrial applications, the indirect three-level sparse matrix converter has been proposed by the reference [115]. The traditional SVPWM for indirect three-level sparse matrix converter is similar to the SVPWM method of three-level output stage matrix converter [115][124].

The only differences are that combination of voltage vectors, duty cycle equations for voltage vectors, and the final switching signals.

5.2.2 A unified carrier-based modulation method for indirect matrix converter

A simplified and unified carrier-based modulation method for indirect matrix converter is similar to the method for direct matrix converter. The matrix converter modulation theory is investigated from the geometric transformation and the SVPWM algorithm for two-level and three-level VSI. The unified continuous carrier-based modulation method is composed of single-carrier based modulation method and double-carrier-based modulation method.

Single-carrier based modulation method and double-carrier-based modulation method are both applicable to the two-level indirect matrix converter, two-level sparse matrix converter, two-level very sparse matrix converter, and two-level ultra sparse matrix converter. Similarly, single-carrier based modulation method and double-carrier-based modulation method are both applicable to three-level output stage indirect matrix converter and indirect three-level sparse matrix converter. Using single carrier based modulation for three-level indirect matrix converter, due to the output states does not require 0 state, the performance of the three-level indirect matrix converter is the same as two-level indirect matrix converter. For double-carrier-based modulation method, if the PWM switching patterns for three output phases are dipolar [d] conditions, the output states MID connects to the minimum input voltage. It increases harmonic components and waveform distortion due to the imprecise control. Therefore, to reduce imprecise control, less [d] condition is proposed. Part of single-carrier based modulation method and double-carrier-based modulation method for indirect matrix converter is an approximate algorithm, not an precise algorithm.

5.3 Control method for indirect matrix converter

5.3.1 Switch commutation

Similar to direct matrix converter, the realization of the indirect matrix converter requires bi-directional switches which must be able to conduct positive and negative currents and must be able to block positive and negative voltages. There are 4 possible switch configurations which are diode bridge switch, common emitter switch, common collector switch, and reverse blocking IGBT switch (as Figure 4.20 to 4.23 shows). To prevent a short circuit in the input voltage source and output voltage load, no two bi-directional switches (on one line) are turned on simultaneously at any one time. Combining direct matrix converter and VSI, the commutation method is that four-step current commutation on the rectifier side and dead time commutation on the inversion side.

5.3.2 Dead time compensation

For two-level indirect matrix converter, dead time compensation method is highly related to the commutation method. When the commutation method is four-step current commutation on the rectifier side and dead time commutation on the inversion side, we can use dead time compensation for direct matrix converter on the rectifier side and dead time compensation for vsi on the inversion side. Similarly, we can use dead time compensation for direct matrix converter and dead time compensation for VSI to the SMC, VSMC, USMC, three-level output stage matrix converter, and indirect three-level sparse matrix converter.

5.3.3 Unbalanced three-phase voltage control

The unbalanced three-phase voltage control is proposed in references [125][126]. Due to the unified and simplified carrier-based modulation method for indirect matrix converter is similar to direct matrix converter, and the modulation method directly uses input voltages and output voltages, the unbalanced three-phase voltage control method is the same as

unbalanced three-phase voltage control for direct matrix converter. The balanced three phase grid voltages after compensation of zero sequence voltage are still balanced three phase grid voltages, and the unbalanced three phase grid voltages can be made balanced after compensation of zero sequence voltage. The new set of voltages after compensation method are used as new three phase voltages and used to carrier-based modulation method.

5.3.4 Energy feedback control

In this indirect matrix converter, the static indirect current control method (phase and amplitude control method) is proposed. The energy feedback control method for indirect matrix converter is identical to the energy feedback control method for direct matrix converter. We can calculate power factor σ and ratio of pulse width modulation M by using equations (3.63) and (3.65) as long as grid voltage E_a, dc bus voltage V_{dc}, and feedback current are determined. The desired output voltages are directly used for simplified SVPWM algorithm to control power switches to track the desired output currents. Through the phase and amplitude control theory we can achieve unity power factor control of energy feedback if we know σ and M.

Chapter 6

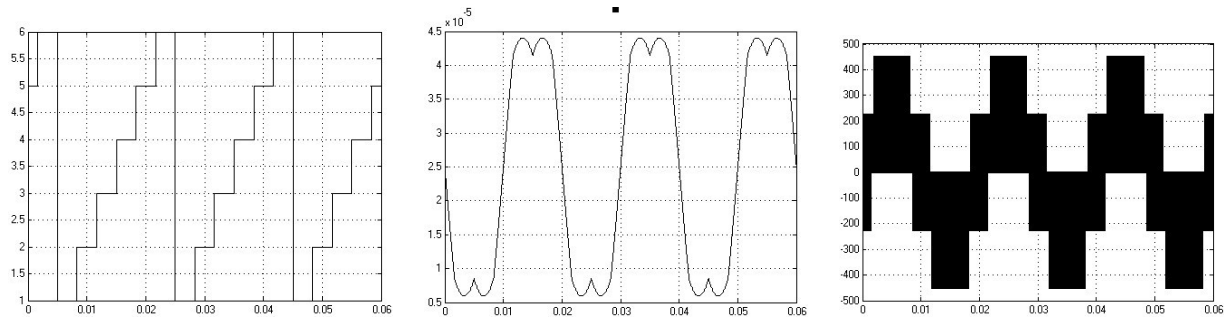
Simulation results

The modulation features are simulated with the help of MATLAB/SIMULINK. The following parts are simulation results of energy feedback VSI and matrix converter. In this chapter, the horizontal axis is time for all figures except FFT analysis. The horizontal axis is harmonic order for FFT analysis.

6.1 Simulation results of energy feedback VSI

6.1.1 Modulation method for VSI

1) SVPWM modulation As the inverter shown in Figure 1.1(a), the simulation model of the SVPWM for two-level VSI is obtained. The simulation parameters are as follows: dc bus voltage $V_{dc} = 680V$, the magnitude of the three-phase desired voltage is 220V, and switching period is 200us. In the figure, the carrier triangular frequency is 5 kHz and the frequency of reference voltage is 50Hz.

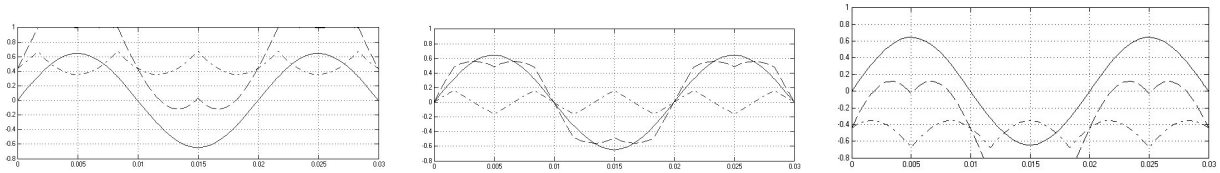


(a) Sector numbers

(b) Waveform of modulation implicit function of SVPWM

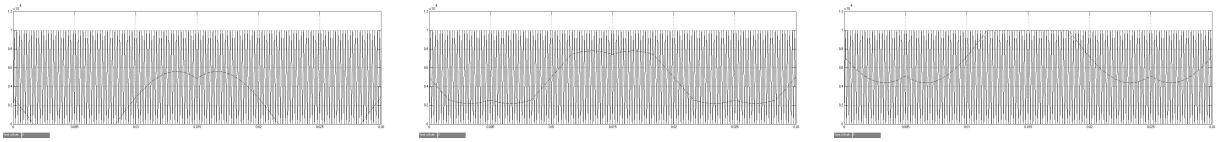
(c) Output voltage of phase a before filtering

Figure 6.1: The waveforms using traditional SVPWM for two-level VSI



(a) k=0 DSVPWMmin (b) k=0.5 standard SVPWM (c) k=1 DSVPWMmax

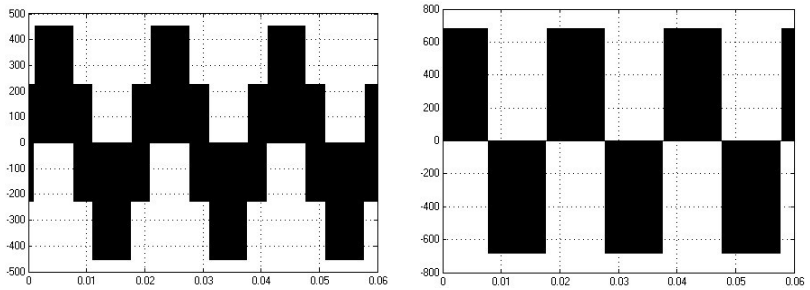
Figure 6.2: Modulation implicit functions of SVPWM v_a^{**} (- - - -), modulation implicit functions of SPWM v_a^* (the real line), zero voltage vector v_z^* (-·-·) at different k for two-level VSI



(a) k=0 DSVPWMmin (b) k=0.5 standard SVPWM (c) k=1 DSVPWMmax

Figure 6.3: Triangle waveform intersection with PWM modulation at different k for two-level VSI

Figure 6.1 shows the waveforms of sector numbers, modulation implicit function of SVPWM, output voltage of phase a, and line voltage before filtering based on the traditional SVPWM method for two-level VSI. In these figures, the vertical axis is sector number for (a), pulse width of SVPWM for (b), and voltage for (c) and (d). Figure 6.2 to Figure 6.4 are obtained by using simplified SVPWM algorithm for two-level VSI. Figure 6.2 shows the waveforms of modulation implicit function of SVPWM, modulation implicit function of SPWM, and zero voltage vectors. In these figures, the vertical axis is modulation implicit

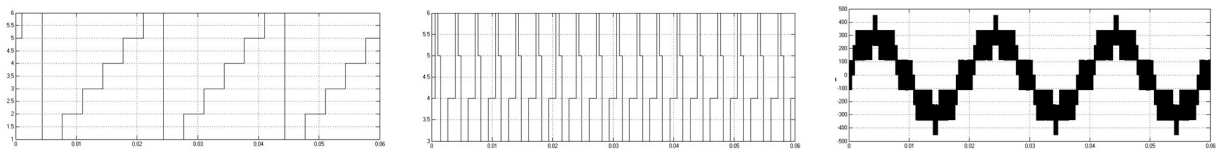


(a) Output voltage of phase a before filtering (b) Output line voltage V_{ab} before filtering

Figure 6.4: The waveforms of output voltage using simplified SVPWM for two-level VSI

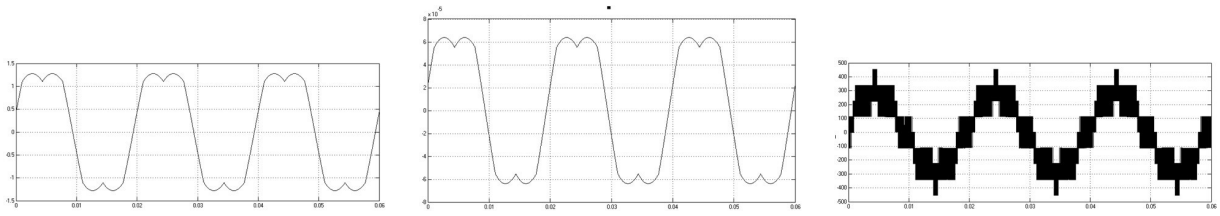
value. Figure 6.3 shows the waveforms of triangular carrier waveform intersection with PWM modulation at different k. In these figures, the vertical axis is pulse width of SVPWM. Figure 6.4 shows the waveforms of output voltage of phase a and line voltage before filtering. In these figures, the vertical axis is voltage. From three figures, we can see that the modulation implicit function of SPWM is sinusoidal waveform and the modulation implicit function of SVPWM is saddle waveform. After filtering, we can get the desired sinusoidal waveform.

The simulation model of simplified SVPWM algorithm for three-level VSI is easily established by using recommended procedure. The voltage source inverter shown in Figure 2.9, the simulation parameters are as follows: dc bus voltage $V_{dc} = 680V$, three phase reference voltage $V_{ref} = 220V$, switching cycle $T_s = 100us$, capacitor $C1 = C2 = 4.4mF$, and frequency $f = 50Hz$.



(a) Simulation results of large sectors (b) Simulation results of small sectors (c) Output voltage of phase a before filtering

Figure 6.5: The waveforms using traditional SVPWM for three-level VSI



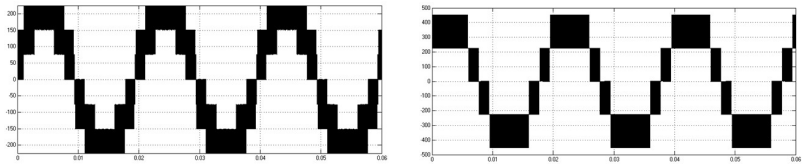
(a) Waveform of modulation implicit function of SVPWM (b) Waveform of pulse width of SVPWM (c) Output voltage of phase a before filtering

Figure 6.6: The waveforms using simplified SVPWM for three-level VSI

Figure 6.5 shows the waveforms of large sectors, small sectors, output voltage of phase a, and line voltage before filtering based on the traditional SVPWM method for three-level VSI. In these figures, the vertical axis is sector number for (a) and (b), voltage for (c) and (d).

Figure 6.6 shows the waveforms of modulation implicit function of SVPWM, pulse width of SVPWM, output voltage of phase a and line voltage before filtering for three-level VSI. In these figures, the vertical axis is modulation implicit value for (a), pulse width of SVPWM for (b), and voltage for (c) and (d). From the figures, we can see that the output voltage of phase a, and line voltage before filtering by using traditional SVPWM method is the same as simplified SVPWM algorithm. After filtering, we can obtain the desired sinusoidal waveform.

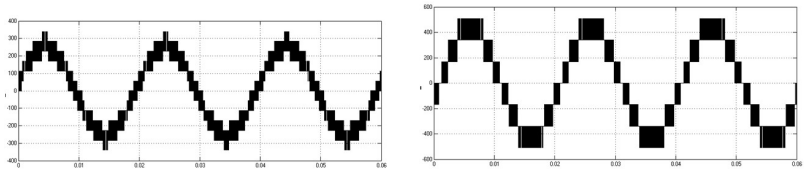
The simulation model of simplified SVPWM algorithm for multi-level VSI is easily established according to the section 2.2.3. The simulation parameters are as follows: dc bus voltage $V_{dc} = 200mV$ (m is modulation level), three phase reference voltage $V_{ref} = 220V$, switching cycle $T_s = 100us$, capacitor $C1 = C2 = 4.4mF$, and frequency $f = 50Hz$.



(a) Output voltage of phase a before filtering

(b) Output line voltage V_{ab} before filtering

Figure 6.7: The waveforms of output voltages using simplified SVPWM for four-level inverter



(a) Output voltage of phase a before filtering

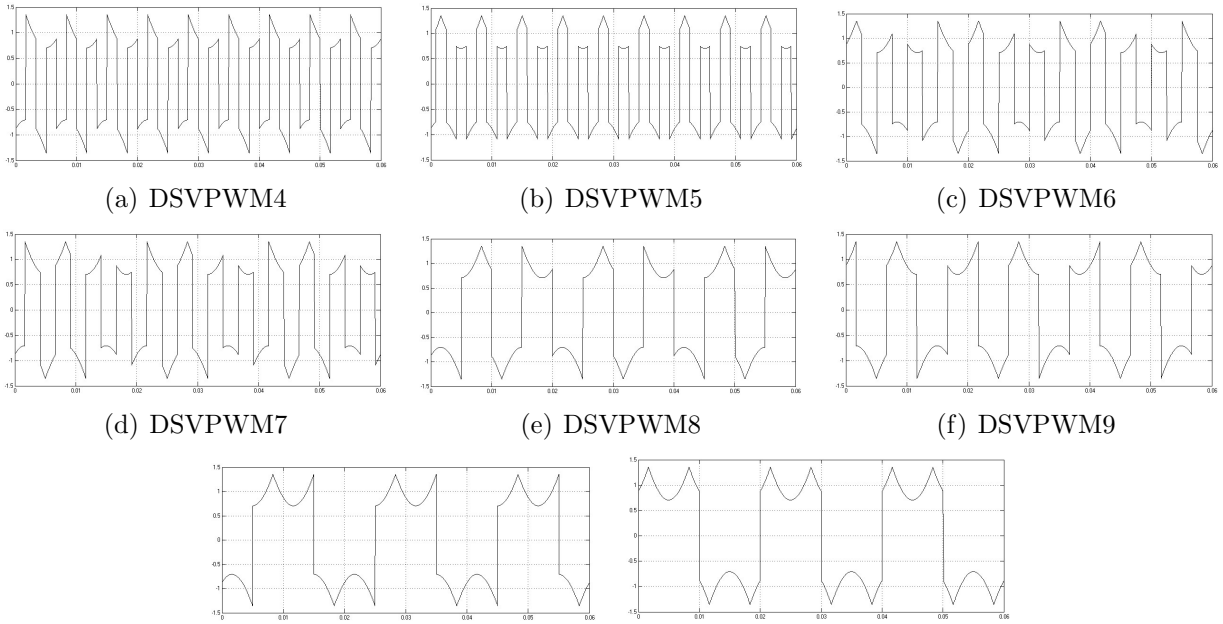
(b) Output line voltage V_{ab} before filtering

Figure 6.8: The waveforms of output voltages using simplified SVPWM for five-level inverter

The simulation results of the simplified SVPWM algorithm for four-level and five-level DCVSI are delineated in Figure 6.7 and 6.8. In the figure, the vertical axis is voltage. Figure 6.7(a) and Figure 6.8(a) are output voltage of phase a before filtering. Figure 6.7(b) and

Figure 6.8(b) are output voltage of line voltage before filtering. With the level number increases, the higher level waveform is smoother than lower level waveform. After filtering, we can get the desired sinusoidal waveform.

2) DSVPWM modulation The simulation results of the simplified DSVPWM strategies for three-level NPC inverters are delineated in Figure 2.18 and Figure 6.9. Figure 6.9 shows zero voltage vector v_z of DSVPWM4 to DSVPWM11. In these figures, the vertical axis is zero voltage vector value.



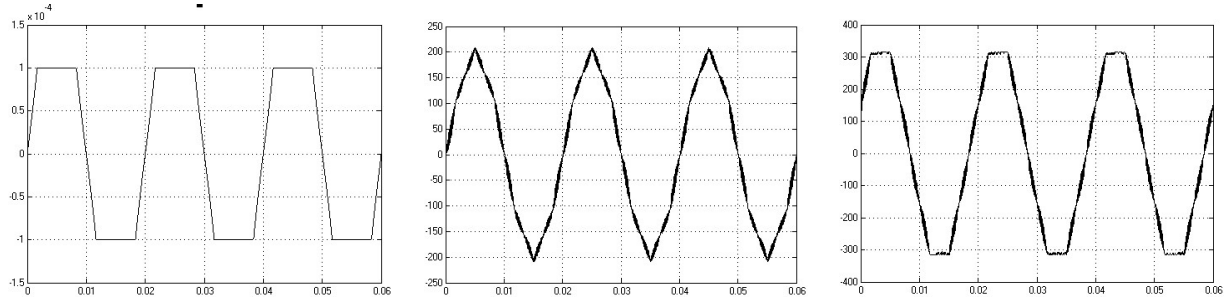
(a) DSVPWM4 (b) DSVPWM5 (c) DSVPWM6

(d) DSVPWM7 (e) DSVPWM8 (f) DSVPWM9

(g) DSVPWM10 (h) DSVPWM11

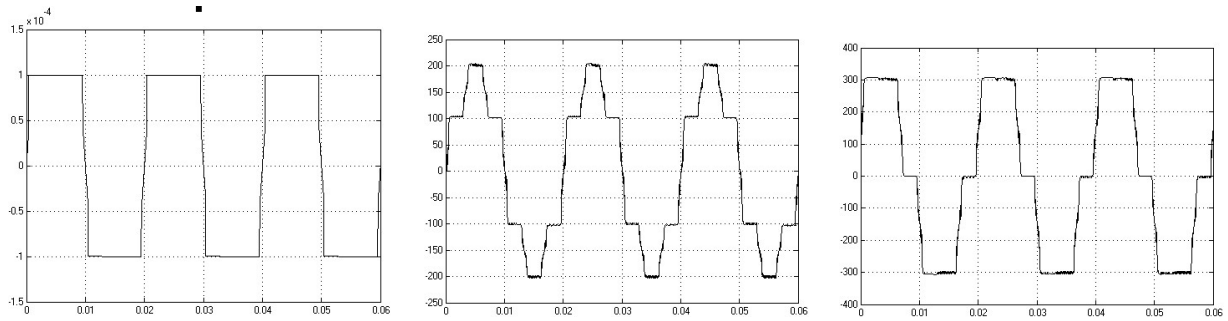
Figure 6.9: Waveform of zero voltage vector (v_z)

3) Overmodulation The simulation results of two-mode overmodulation method 1 for three-phase three-level NPC VSI based on the simplified SVPWM are delineated from Figure 6.10 to Figure 6.12. In these figures, the vertical axis is modulation implicit value for (a) and voltage for (b) and (c). The results are obtained by using simplified space vector modulation for three-level inverter. Figure 6.10(a) to Figure 6.12(a) show the waveforms of pulse width of SVPWM T_{da} for $MI = 0.9514$ to $MI = 1$; Figure 6.10(b) to Figure 6.12(b)



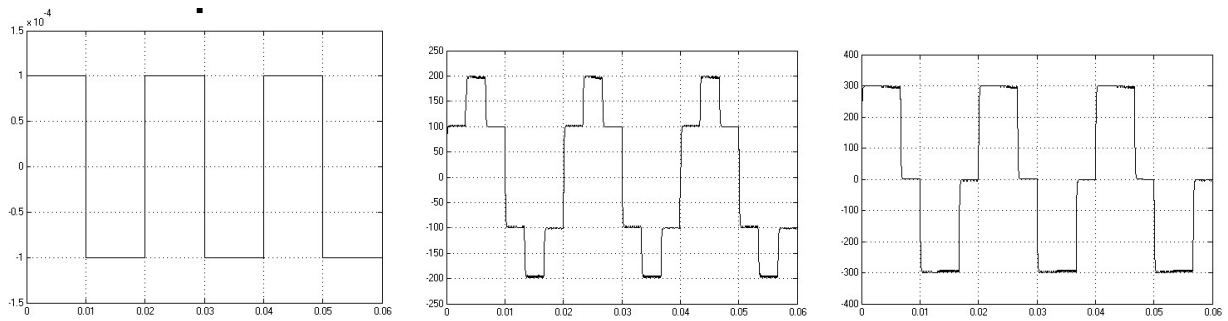
(a) Pulse width of SVPWM T_{da} for three-level inverter (b) Output phase a voltage after filtering (c) Output line voltage after filtering

Figure 6.10: Waveforms of two-mode overmodulation method 1 when MI=0.9514



(a) Pulse width of svpwm T_{da} for three-level inverter (b) Output phase a voltage after filtering (c) Output line voltage after filtering

Figure 6.11: Waveforms of two-mode overmodulation method 1 when MI=0.98

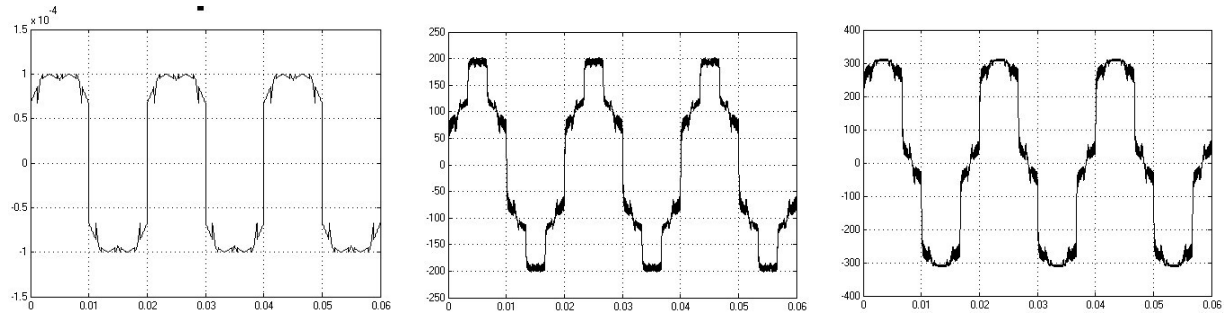


(a) Pulse width of SVPWM T_{da} for three-level inverter (b) Output phase a voltage after filtering (c) Output line voltage after filtering

Figure 6.12: Waveforms of two-mode overmodulation method 1 when MI=1

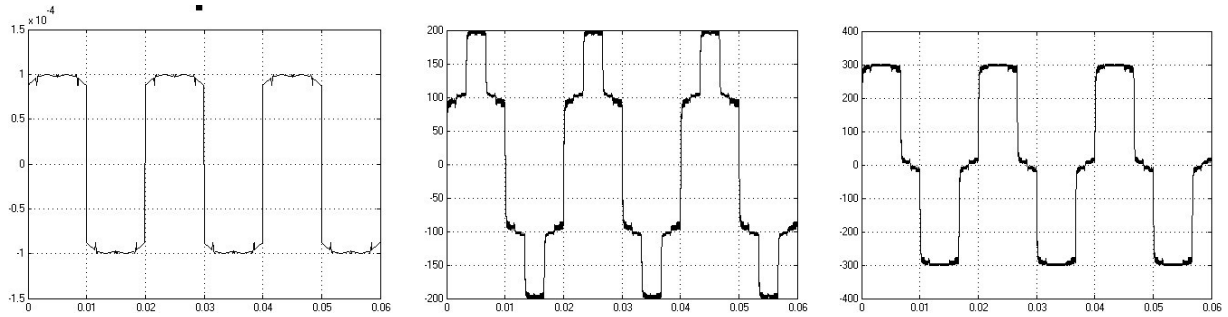
show the waveforms of output phase a voltage v_a after filtering for $MI = 0.9514$ to $MI = 1$; Figure 6.10(c) to Figure 6.12(c) show the waveforms of output line voltage v_{ab} after filtering for $MI = 0.9514$ to $MI = 1$. From the figures, we can see that pulse width of SVPWM gradually becomes a square wave and output voltage also gradually becomes a square wave with the reference voltage gradually becomes six-step operation.

The simulation results of single-mode overmodulation method 1 for three-phase three-level NPC VSI based on the simplified SVPWM are delineated from Figure 6.13 to Figure 6.15. The results are obtained by using simplified space vector modulation for three-level



(a) Pulse width of SVPWM T_{da} for three-level inverter (b) Output phase a voltage after filtering (c) Output line voltage after filtering

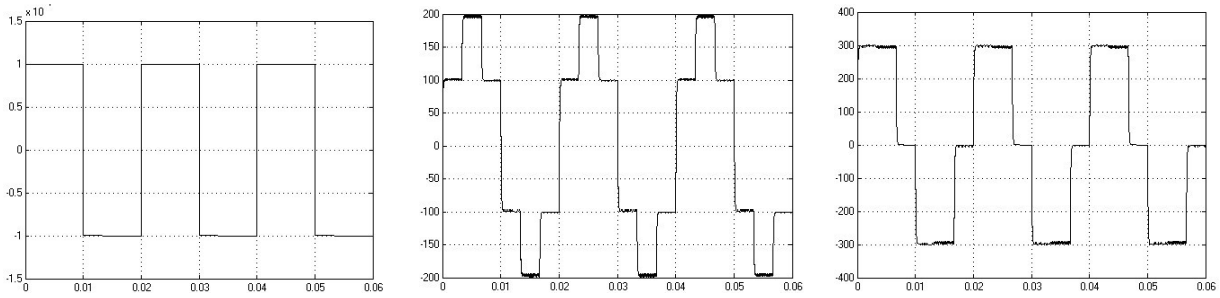
Figure 6.13: Waveforms of single-mode overmodulation method 1 when MI=0.9514



(a) Pulse width of SVPWM T_{da} for three-level inverter (b) Output phase a voltage after filtering (c) Output line voltage after filtering

Figure 6.14: Waveforms of single-mode overmodulation method 1 when MI=0.98

inverter. Figure 6.13(a) to Figure 6.15(a) show the waveforms of pulse width of SVPWM T_{da} for $MI = 0.9514$ to $MI = 1$; Figure 6.13(b) to Figure 6.15(b) show the waveforms of



(a) Pulse width of SVPWM T_{da} for three-level inverter

(b) Output phase a voltage after filtering

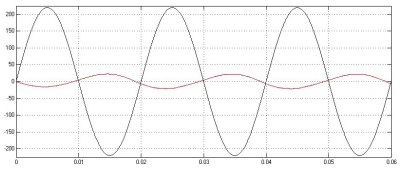
(c) Output line voltage after filtering

Figure 6.15: Waveforms of single-mode overmodulation method 1 when MI=1

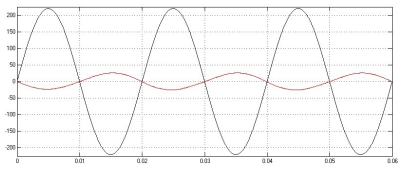
output phase a voltage v_a after filtering for $MI = 0.9514$ to $MI = 1$; Figure 6.13(c) to Figure 6.15(c) show the waveforms of output line voltage v_{ab} after filtering for $MI = 0.9514$ to $MI = 1$. In these figures, the vertical axis is modulation implicit value for (a), and voltage for (b) and (c). From the figures, we can see that pulse width of SVPWM gradually becomes a square wave and output voltage also gradually becomes a square wave with the reference voltage gradually becomes six-step operation.

6.1.2 Control methods for VSI

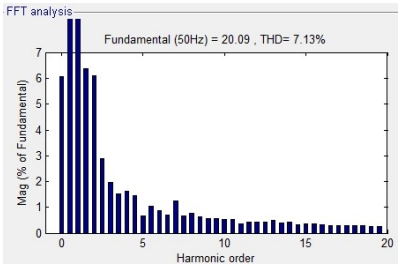
1) Dead time compensation Simulation parameters are as follows: voltage source $V = 220V$, frequency $f = 50Hz$, dc bus voltage $V_{dc} = 200mV$, inverter switching frequency $f_s = 5kHz$, inductance $L = 6mH$, capacitor $C = 4.4\mu F$, the minimum allowable dead time $T_{dmin} = 0.5\mu s$, and the maximum allowable dead time $T_{dmax} = 10\mu s$. The simulation results of dead time compensation for three-level NPC VSI are delineated in Figure 6.16. Figure 6.16(a) shows waveforms of feedback current and grid voltage without dead time compensation for three-level NPC VSI. Figure 6.16(b) shows waveforms of feedback current and grid voltage with inclusion of dead time compensation for three-level NPC VSI. Figure 6.16(c) shows fast fourier transform (FFT) analysis and THD of feedback current without dead time compensation for three-level NPC VSI and Figure 6.16(d) shows FFT analysis and THD of feedback current with inclusion of dead time compensation for three-level NPC



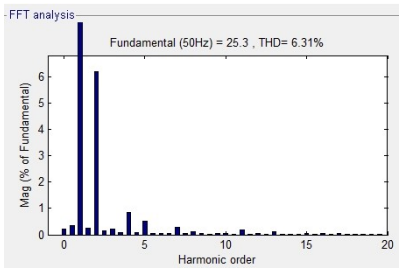
(a) Waveforms of feedback current and grid voltage without dead time compensation



(b) Waveforms of feedback current and grid voltage with inclusion of dead time compensation



(c) FFT analysis of feedback current without dead time compensation

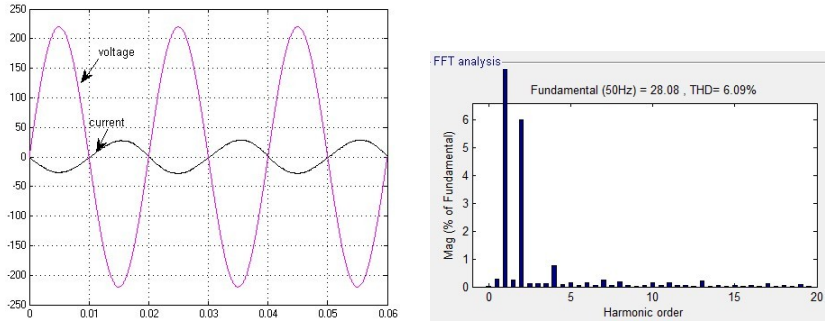


(d) FFT analysis of feedback current with inclusion of dead time compensation

Figure 6.16: Waveforms for three-level inverter

VSI. In these figures, the vertical axis is voltage for (a) and (b), fundamental amplitude for (c) and (d).

Fourier transform includes continuous Fourier transform, Fourier series, discrete time Fourier transform, and discrete Fourier transform. These four Fourier transform are applied to positive infinity and negative infinity signal that the length of signal is infinite. Extends limited length signal to unlimited length signal satisfy Fourier transform. Due to computer can only handle discrete numerical signal, the signal can be extended by the method of copying, so that the signal becomes a periodic discrete signal, then we can use a discrete Fourier transform methods. For computers, only discrete and limited length of data can be processed, we can only use the discrete Fourier transform method to transform discrete signals. Discrete Fourier transform approximately calculate a spectrum of continuous signal, and it can be realized by fast Fourier transform. In the Figure, the FFT analysis is used for discrete Fourier transform. In the simulation, about ten thousand samples are selected per cycle and near five thousandth harmonics are used to calculate THD, and parts of harmonic



(a) Waveforms of feedback current and grid voltage

(b) FFT analysis of feedback current with inclusion of dead time compensation

Figure 6.17: Waveforms after adding band-limited white noise

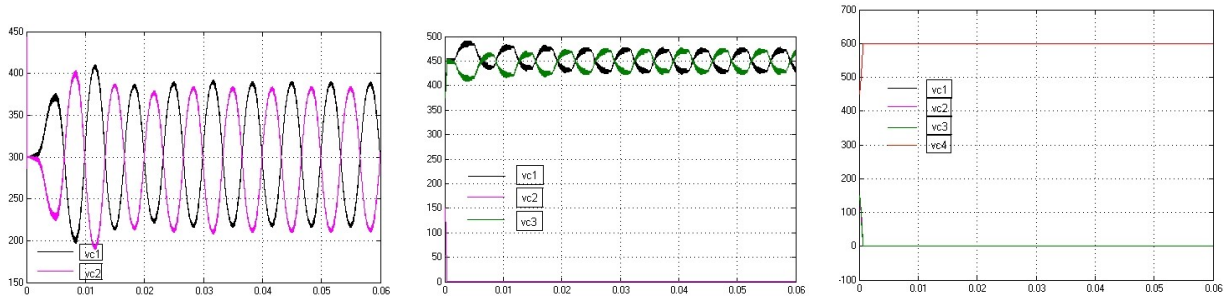
orders are placed in the figure. The following FFT analysis also uses the same discrete Fourier transform.

From the figures, we can see that there are obvious phase shift, fundamental amplitude of feedback current is much smaller than desired value, and THD is big without dead time compensation. With inclusion of dead time compensation, phase shift is well controlled, fundamental amplitude of feedback current is close to ideal value 26, and THD is also much smaller than without dead time compensation.

In the practical applications, noise will be added when measuring data. As .Figure 6.17 shows, after adding band-limited white noise into the input signal, the fundamental amplitude is increased and THD is decreased.

2) Dc-link capacitor voltage control strategy The simulation parameters are as follows: frequency $f = 50Hz$, three-level dc bus voltage $V_{dc} = 600V$, four-level dc bus voltage $V_{dc} = 900V$, five-level dc bus voltage $V_{dc} = 1200V$, inverter switching frequency $f_s = 5kHz$, filter inductance $L = 6mH$, and capacitor $C = 4.4\mu F$. The simulation results of three-phase multi-level diode-clamped VSI based on SVPWM without dc-link capacitor voltage control are delineated in Figure 6.18. The results are obtained by using simplified space vector modulation. Figure 6.18(a) shows the two unequal capacitor voltages for three-level inverter. Figure 6.18(b) shows the three unequal capacitor voltages for four-level inverter. Figure

6.18(c) shows the four unequal capacitor voltages for five-level inverter. In these figures, the vertical axis is voltage. From the figures, we can see that voltage fluctuations are large and some voltages are equal to zero in four-level and five-level inverter.

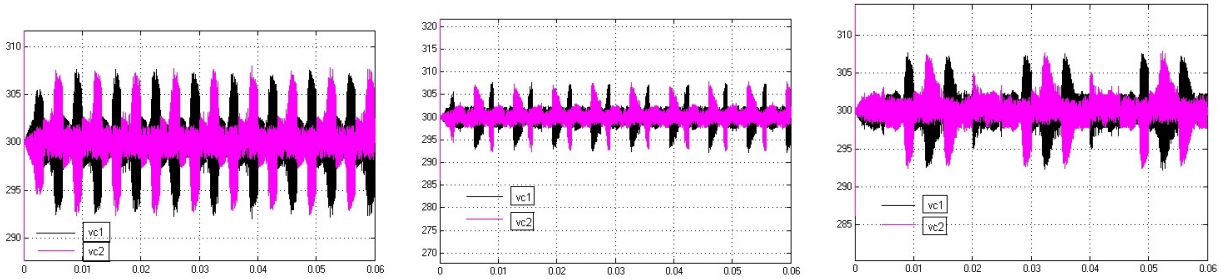


(a) Capacitor voltage for three-level inverter (b) Capacitor voltage for four-level inverter (c) Capacitor voltage for five-level inverter

Figure 6.18: The waveforms of capacitor voltage before control

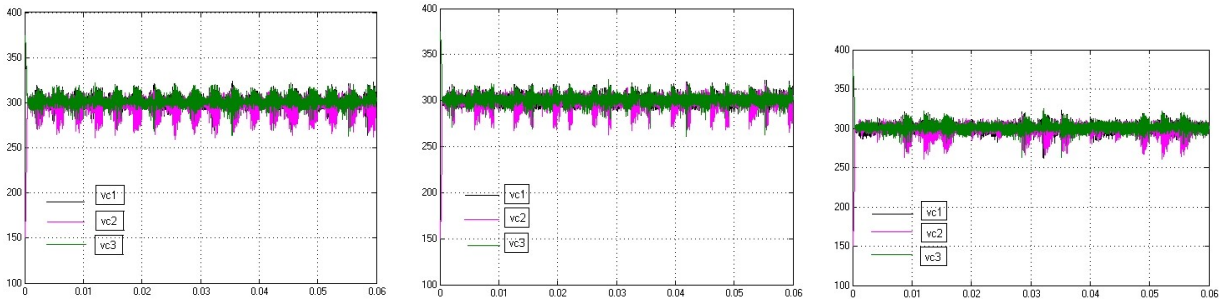
The simulation results of three-phase multi-level diode-clamped VSI based on DSVPWM with inclusion of dc-link capacitor voltage control are shown in Figure 6.19 to Figure 6.21. Figure 6.19 shows dc-link capacitor voltages based on DSVPWM for three-level inverter. Figure 6.20 shows dc-link capacitor voltages based on DSVPWM for four-level inverter, and Figure 6.21 shows dc-link capacitor voltages based on DSVPWM for five-level inverter. In these figures, the vertical axis is voltage. In all cases, the dc-link capacitor voltages are balanced at $300V$ after using the proposed simplified control strategy. The simulation results confirm that the proposed DSVPWM has a good performance for solving fluctuation of dc-link capacitor voltages in the diode-clamped inverter. This simplified control strategy based on DSVPWM is uncomplicated and should require very little computation time.

3) Unbalanced three-phase grid voltage control The simulation parameters are as follows: voltage source $V_a = 220V$, $V_b = 260V$, $V_c = 180V$, phase angle $\theta_a = 10°$, $\theta_b = -110°$, $\theta_c = 130°$, frequency $f = 49Hz$, dc bus voltage $V_{dc} = 680V$, inverter switching frequency $f_s = 5kHz$, inductance $L = 6mH$, and capacitor $C = 4.4\mu F$. The simulation results of three-level NPC VSI based on SVPWM without unbalanced three-phase grid voltage control



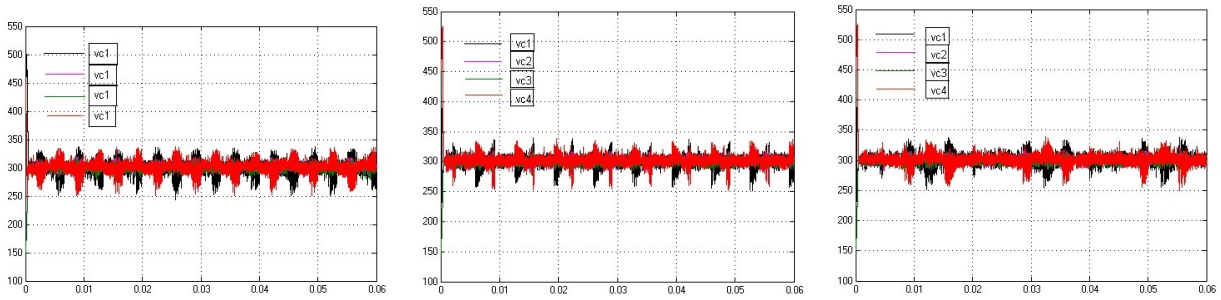
(a) DSVPWM3 (b) DSVPWM5 (c) DSVPWM6

Figure 6.19: Capacitor voltages for three-level inverter



(a) DSVPWM3 (b) DSVPWM5 (c) DSVPWM6

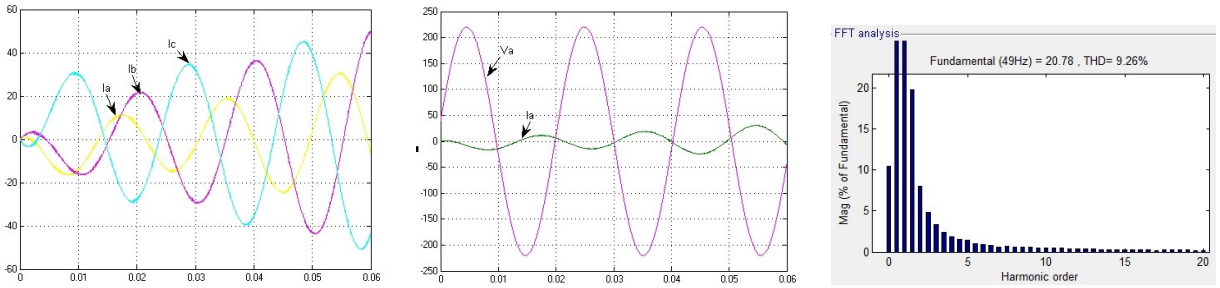
Figure 6.20: Capacitor voltages for four-level inverter



(a) DSVPWM3 (b) DSVPWM5 (c) DSVPWM6

Figure 6.21: Capacitor voltages for five-level inverter

are delineated in Figure 6.22. The results are obtained by using simplified space vector modulation and regard three phase grid voltages are balanced. Figure 6.22(a) shows the waveform of modulation implicit function of SVPWM, Figure 6.22(b) shows the waveforms of three phase output currents, Figure 6.22(c) shows the waveforms of feedback current and grid voltage, and Figure 6.22(d) shows FFT analysis of feedback current. In these figures, the vertical axis is current for (a), voltage for (b), and fundamental magnitude for (c). From Figure 6.22(b) to (d), three-phase currents are under unbalanced conditions, unity power factor of feedback current is not equal to 1, THD is large, and fundamental value is small.

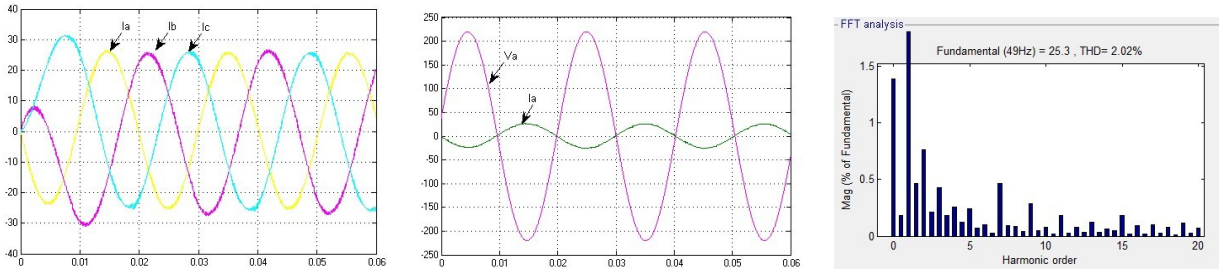


(a) Three phase output currents (b) Waveforms of feedback current and grid voltage (c) FFT analysis of phase a current

Figure 6.22: Waveforms without compensation

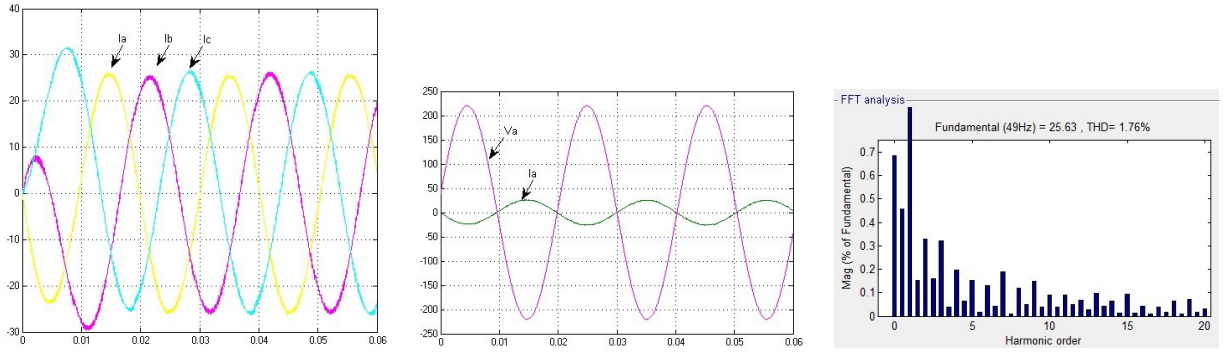
The simulation results of three-level NPC VSI based on simplified DSVPWM with inclusion of unbalanced three-phase grid voltage control are delineated from Figure 6.23 to Figure 6.24. Figure 6.23(a) and Figure 6.24(a) show the waveforms of three phase output currents, Figure 6.23(b) and Figure 6.24(b) show the waveforms of feedback current and grid voltage, and Figure 6.23(c) and Figure 6.24(c) show FFT analysis of feedback current. In these figures, the vertical axis is current for (a), voltage for (b), and fundamental magnitude for (c). Three phase output currents are balanced with inclusion of unbalanced three-phase grid voltage control. Unity power factor of feedback current is nearly equal to 1; feedback current and grid voltage have reverse phase sequence. With inclusion of unbalanced three-phase grid voltage control, THD is much smaller than without unbalanced three-phase grid voltage control, and fundamental value is also close to ideal value 26. From FFT analysis, we

can see that DSVPWM7 has smallest THD and biggest fundamental value. The compensation of unbalanced three-phase grid voltage in three-level NPC VSI based on the DSVPWM works well.



(a) Three phase output currents (b) Waveforms of feedback current and grid voltage (c) FFT analysis of phase a current

Figure 6.23: Compensation based on DSVPWM5

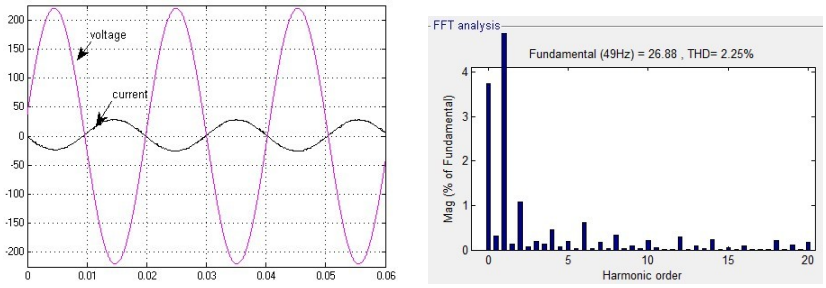


(a) Three phase output currents (b) Waveforms of feedback current and grid voltage (c) FFT analysis of phase a current

Figure 6.24: Compensation based on DSVPWM6

In the practical applications, noise will be added when measuring data. As .Figure 6.25 shows, after adding band-limited white noise into the input signal, the fundamental amplitude and THD is increased.

4) Energy feedback VSI control The phase and amplitude control method is used as energy feedback VSI control method. The simulation results of the energy feedback VSI control for three-level NPC VSI based on the SVPWM are delineated in Figure 6.26. Figure 6.26(a) shows waveforms of three phase feedback current and Figure 6.26(b) shows waveforms

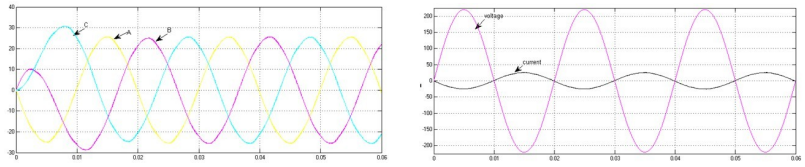


(a) Waveforms of feedback current and grid voltage

(b) FFT analysis of feedback current with inclusion of control

Figure 6.25: Waveforms after adding band-limited white noise

of feedback current and grid voltage. In these figures, the vertical axis is current for (a), voltage and current for (b).The sinusoidal feedback current is drawn as anti-phase (energy feedback) with the corresponding grid voltage; it shows the feedback control algorithm works well.



(a) Waveforms of three phase feedback currents

(b) Waveforms of feedback current and grid voltage

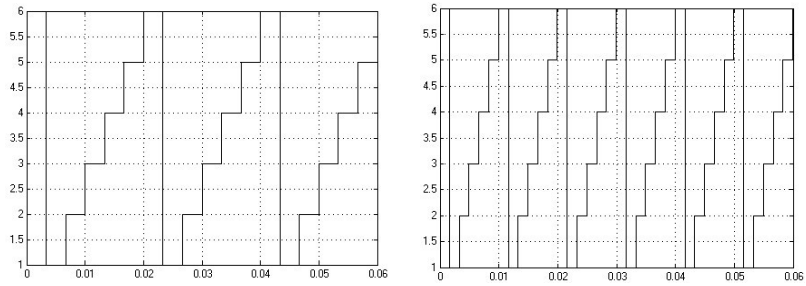
Figure 6.26: The waveforms of feedback currents and grid voltage

6.2 Simulation results of matrix converter

6.2.1 Direct matrix converter

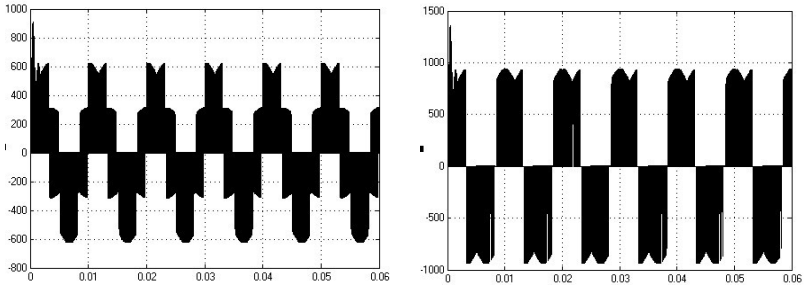
1) SVPWM method The simulation model of SVPWM algorithm for three-phase direct matrix converter can be established according to the previous description. As the direct matrix converter shown in Figure 1.6(a), the simulation parameters are as follows: input frequency $f_i = 50Hz$, three-phase input voltages $v_i = v_m \sin(\omega t + \frac{2\pi l}{3}), i \in (a, b, c), l \in (0, 1, 2)$, input RLC $R = 1\Omega$, $L = 0.3mH$, $C = 25\mu F$, output RL $R = 10\Omega$, $L = 10\mu H$, output frequency $f_o = 25Hz$, three-phase output voltages $v_j = v_m \sin(\omega t + \frac{2\pi l}{3}), j \in (A, B, C), l \in$

$(0, 1, 2)$, and carrier triangular frequency $f_s = 5kHz$. The simulation results of direct matrix converter based on the SVPWM method are delineated from Figure 6.27 to Figure 6.29. Figure 6.27 shows input current sectors and output voltage sectors. In these figures, the vertical axis is sector number. Figure 6.28 shows the output phase a voltage before filtering and output line voltage V_{ab} before filtering. In these figures, the vertical axis is voltage. Figure 6.29 shows the three-phase output currents and desired sinusoidal output voltage. From the figures, we can see that output current is tracking desired output voltage in real-time. In these figures, the vertical axis is voltage and current for (a), current for (b).



(a) Input current sectors (b) Output voltage sectors

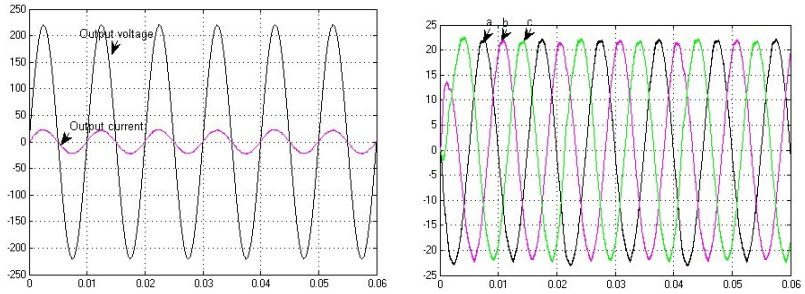
Figure 6.27: The waveforms of sectors



(a) Output phase voltage before filtering (b) Output line voltage before filtering

Figure 6.28: Output voltages before filtering

2) A simplified and unified carrier-based modulation method for direct matrix converter The simulation model of the unified carrier based modulation method



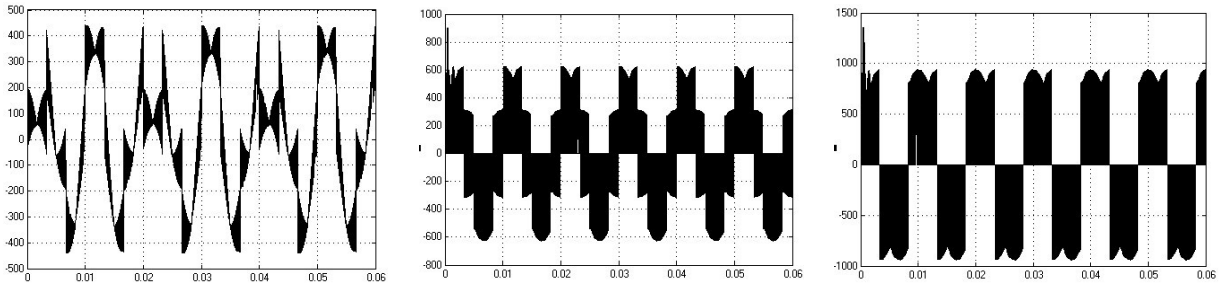
(a) Output current and desired voltage (b) Three-phase output currents

Figure 6.29: Output currents and desired voltage

can be easily established by using recommended procedure. The simulation parameters are as follows: input frequency $f_i = 50Hz$, three-phase input voltages $v_i = v_m \sin(\omega t + \frac{2\pi l}{3}), i \in (a, b, c), l \in (0, 1, 2)$, input RLC $R = 1\Omega$, $L = 0.3mH$, $C = 25\mu F$, output RL $R = 10\Omega$, $L = 10\mu H$, output frequency $f_o = 25Hz$, three-phase output voltages $v_j = v_m \sin(\omega t + \frac{2\pi l}{3}), j \in (A, B, C), l \in (0, 1, 2)$, and carrier triangular frequency $f_s = 5kHz$.

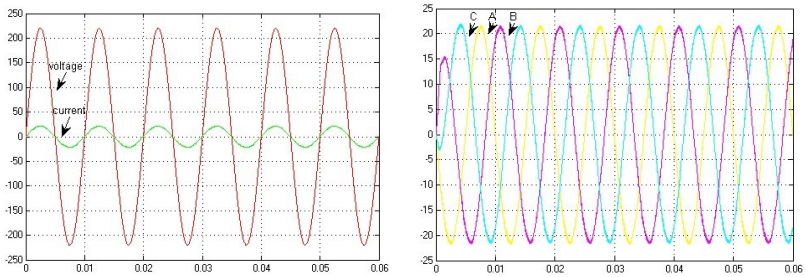
The simulation results of direct matrix converter based on the single carrier-based modulation method are delineated in Figure 6.30 and Figure 6.31. The simulation results are obtained by using the continuous single carrier-based modulation method I. Figure 6.30 shows the carrier waveform of method I, output phase a voltage before filtering, and output line voltage V_{ab} before filtering. In these figures, the vertical axis is voltage. Figure 6.31 shows the waveforms of output reference voltage v_A and output feedback current i_A. In these figures, the vertical axis is voltage and current for (a), current for (b). The feedback current is in phase with the desired output voltage.

The simulation results of direct matrix converter based on the double carrier-based modulation method are delineated in Figure 6.32 and Figure 6.33. The simulation results are obtained by using the continuous double carrier-based modulation method [1b1u1d]. Figure 6.32 shows the upper and lower modulation implicit functions of [1b1u1d], output phase a voltage before filtering, and output line voltage V_{ab} before filtering. In these figures, the vertical axis is modulation implicit value for (a), voltage for (b) and (c). Figure 6.33



(a) Carrier waveform of method I (b) Output phase voltage before filtering (c) Output line voltage before filtering

Figure 6.30: Output voltages before filtering

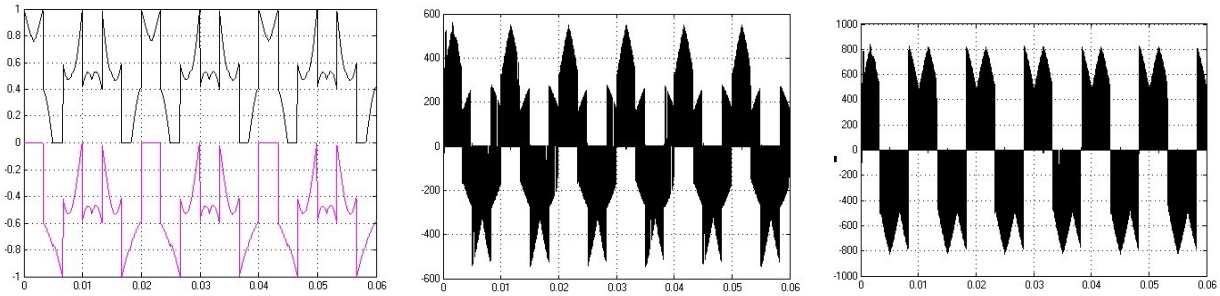


(a) Output current and desired voltage (b) Three-phase output currents

Figure 6.31: Output currents and desired voltage

shows the waveforms of output reference voltage v_A and output feedback current i_A. The feedback current is in phase with the desired output voltage. In these figures, the vertical axis is voltage and current for (a), current for (b).

The simulation results of direct matrix converter based on the single carrier-based discontinuous modulation method are delineated in Figure 6.34 and Figure 6.35. The simulation results are obtained by using the discontinuous single carrier-based modulation method IV (max). Figure 6.34 shows the carrier waveforms of single carrier-based modulation IV, output phase a voltage before filtering, and output line voltage V_{ab} before filtering. In these figures, the vertical axis is voltage. Figure 6.35 shows the waveforms of output reference voltage v_A and output feedback current i_A. In these figures, the vertical axis is voltage and

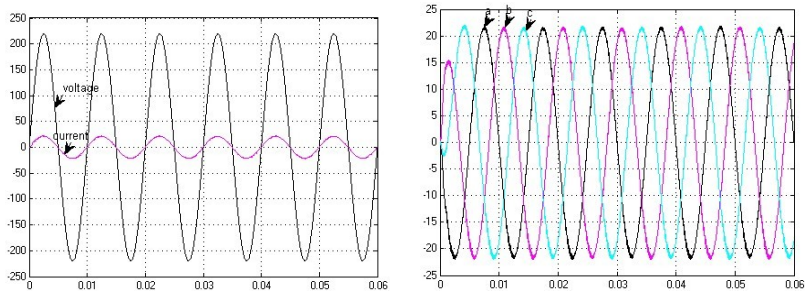


(a) Upper and lower modulation implicit function

(b) Output phase voltage before filtering

(c) Output line voltage before filtering

Figure 6.32: Output voltages before filtering



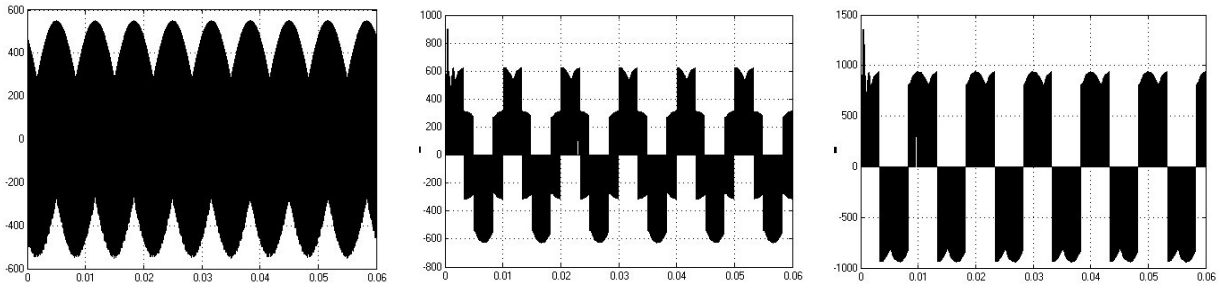
(a) Output current and desired voltage

(b) Three-phase output currents

Figure 6.33: Output currents and desired voltage

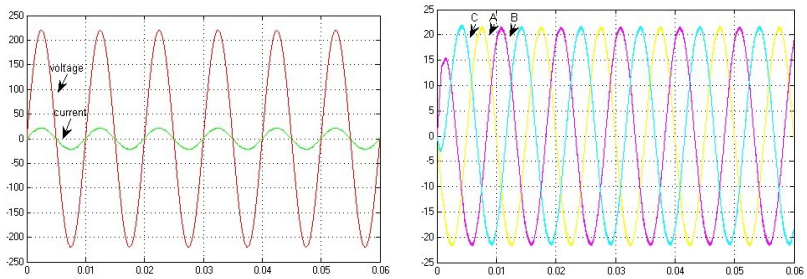
current for (a), current for (b). The feedback current is in phase with the desired output voltage.

The simulation results of direct matrix converter based on the double carrier-based discontinuous modulation method are delineated in Figure 6.36 and Figure 6.37. The simulation results are obtained by using the discontinuous double carrier-based modulation method [2u1d]. Figure 6.36 shows the upper and lower modulation implicit functions of [2u1d], output phase a voltage before filtering, and output line voltage V_{ab} before filtering. In these figures, the vertical axis is pulse width modulation for (a), voltage for (b) and (c). Figure 6.37 shows the waveforms of output reference voltage v_A and output feedback current i_A. In these figures, the vertical axis is voltage and current for (a), current for (b). The feedback current is in phase with the desired output voltage.



(a) Carrier waveform of method IV (b) Output phase voltage before filtering (c) Output line voltage before filtering

Figure 6.34: Output voltages before filtering



(a) Output current and desired voltage (b) Three-phase output currents

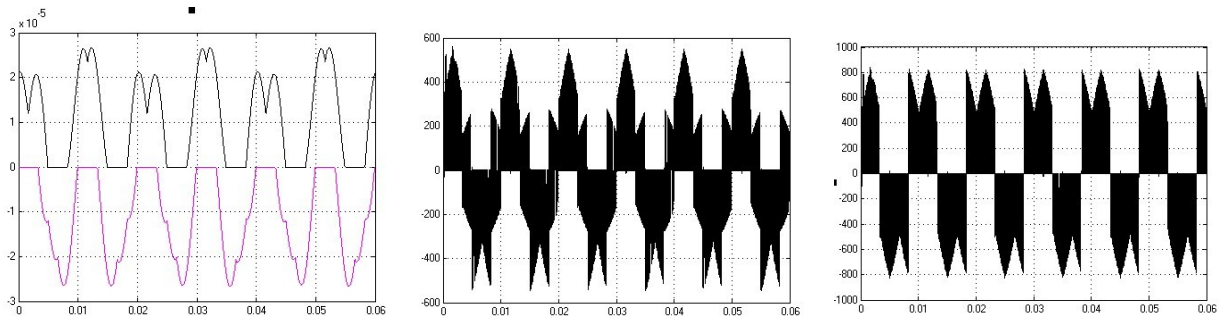
Figure 6.35: Output currents and desired voltage

The performance of the unified continuous carrier-based modulation methods are shown in Table 6.1. In the table, MI is modulation index, M is method, H is high, N is normal, L is low, GW is good waveform, NW is normal waveform, BW is bad waveform, ST is small THD, NT is normal THD, and LT is large THD. The performance of the unified

MI/M	I	II	III	IV	[3d]	[1b1u1d]
H	GW, ST	GW, NT	GW, ST	GW, ST	GW, ST	GW, ST
N	GW, ST	GW, NT	GW, ST	GW, ST	GW, ST	GW, ST
L	NW, NT	NW, NT	NW, NT	NW, NT	BW, LT	BW, LT

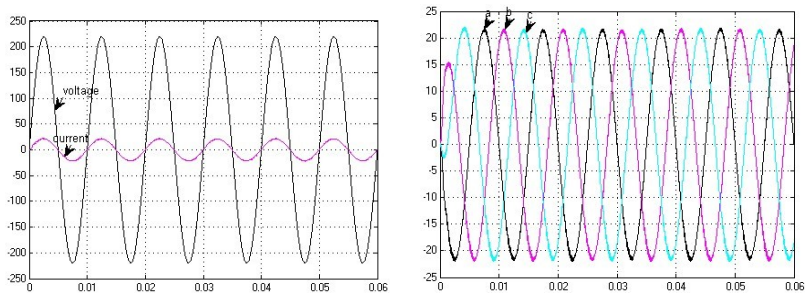
Table 6.1: The performance of continuous carrier-based modulation method

discontinuous carrier-based modulation methods are shown in Table 6.2. In the table, the modulation implicit functions tend to MAX and MIN is II.1, and tend to MID is II.2; the modulation implicit functions tend to MAX is IV.1, and tend to MIN is IV.2. From the



(a) Pulse width modulation (b) Output phase voltage before filtering (c) Output line voltage before filtering

Figure 6.36: Output voltages before filtering



(a) Output current and desired voltage (b) Three-phase output currents

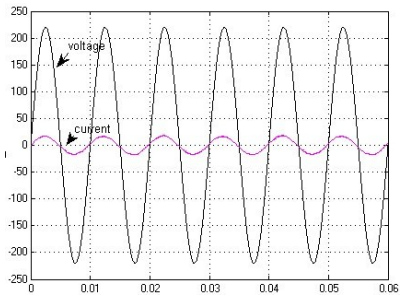
Figure 6.37: Output currents and desired voltage

tables, we can see that the performance of the unified carrier-based modulation method slightly different, most of the methods work well.

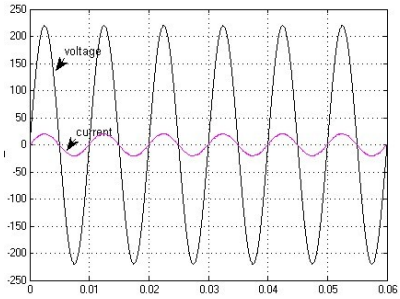
3) Dead time compensation The simulation parameters are as follows: input frequency $f_i = 50Hz$, three-phase input voltages $v_i = v_m \sin(\omega t + \frac{2\pi l}{3}), i \in (a, b, c), l \in (0, 1, 2)$, input RLC $R = 1\Omega$, $L = 0.3mH$, $C = 25\mu F$, output RL $R = 10\Omega$, $L = 10\mu H$, output frequency $f_o = 25Hz$, three-phase output voltages $v_j = v_m \sin(\omega t + \frac{2\pi l}{3}), j \in (A, B, C), l \in (0, 1, 2)$, carrier triangular frequency $f_s = 5kHz$, the minimum allowable dead time $T_{dmin} = 0.5\mu s$,

MI/M	I	II.1	II.2	IV.1	IV.2	[2u1d]	[1n2d]
H	GW, ST	GW, NT	GW, NT	GW, ST	GW, ST	GW, ST	GW, ST
N	GW, ST	GW, ST	GW, ST	GW, ST	GW, ST	GW, ST	GW, ST
L	BW, LT	BW, LT	NW, NT	BW, LT	GW, NT	NW, LT	GW, NT

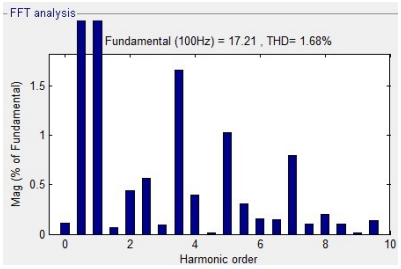
Table 6.2: The performance of discontinuous carrier-based modulation method



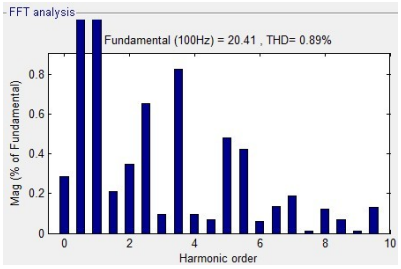
(a) Waveforms of feedback current and grid voltage without dead time compensation



(b) Waveforms of feedback current and grid voltage with inclusion of dead time compensation



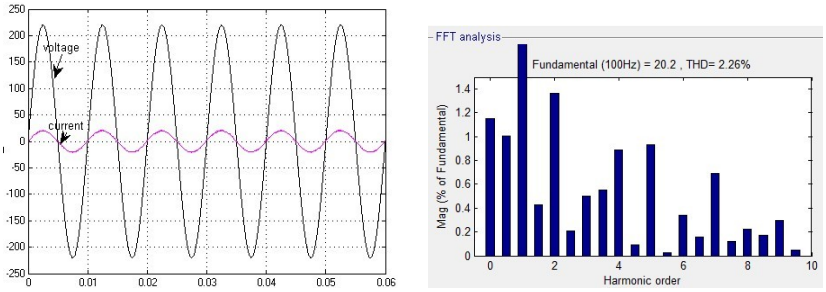
(c) FFT analysis of feedback current without dead time compensation



(d) FFT analysis of feedback current with inclusion of dead time compensation

Figure 6.38: Dead time compensation waveforms for DMC

and the maximum allowable dead time $T_{dmax} = 10\mu s$. The double carrier-based modulation method [2u1d] is used as modulation method. The simulation results of dead time compensation for DMC are delineated in Figure 6.38. Figure 6.38(a) shows waveforms of feedback current and grid voltage without dead time compensation control. Figure 6.38(b) shows waveforms of feedback current and grid voltage with inclusion of dead time compensation control. Figure 6.38(c) shows FFT analysis and THD of feedback current without dead time compensation control and Figure 6.38(d) shows FFT analysis and THD of feedback current with inclusion of dead time compensation control. In these figures, the vertical axis is voltage and current for (a) and (b), fundamental amplitude for (c) and (d). From the figures, we can see that fundamental amplitude of feedback current is much smaller than desired value, and THD is big without dead time compensation control. With inclusion of dead time compensation control, fundamental amplitude of feedback current is close to ideal value, and THD is also much smaller than without dead time compensation control.



(a) Waveforms of feedback current and grid voltage

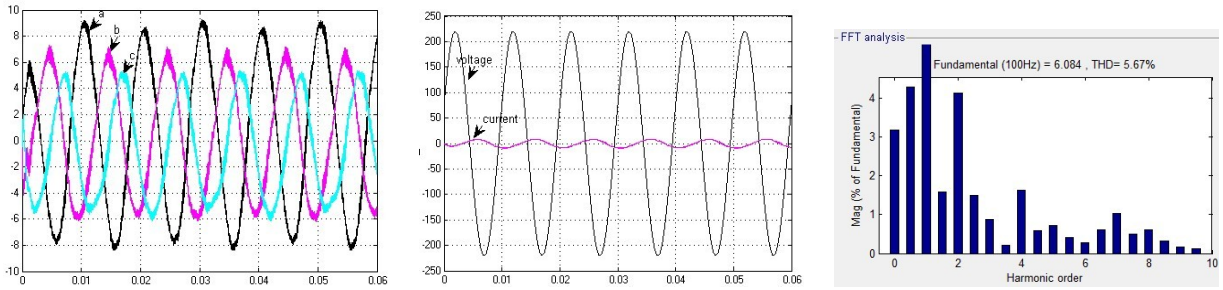
(b) FFT analysis of feedback current with inclusion of compensation

Figure 6.39: Waveforms after adding band-limited white noise

In the practical applications, noise will be added when measuring data. As .Figure 6.39 shows, after adding band-limited white noise into the input signal, the THD is increased.

4) Unbalanced three-phase voltage control The simulation parameters are as follows: voltage source $V_a = 900V$, $V_b = 1000V$, $V_c = 1100V$, phase angle $\theta_a = 10°$, $\theta_b = -110°$, $\theta_c = 130°$, frequency $f = 50Hz$, output voltage $v_a = 220V$, $v_b = 260V$, $v_c = 180V$, phase angle $\theta_a = 20°$, $\theta_b = -100°$, $\theta_c = 140°$, and frequency $f = 25Hz$. The simulation results of DMC based on double carrier-based modulation [2u1d] without unbalanced three-phase voltage control are delineated in Figure 6.40. Figure 6.40(a) shows the waveforms of three phase output currents, Figure 6.40(b) shows the waveforms of feedback current and grid voltage, and Figure 6.40(c) shows FFT analysis of feedback current. In these figures, the vertical axis is current for (a), voltage and current for (b), and fundamental amplitude for (c). From the figures, we can see that three phase currents are under unbalanced conditions, unity power factor of feedback current is not equal to 1, THD is large, and fundamental value is small.

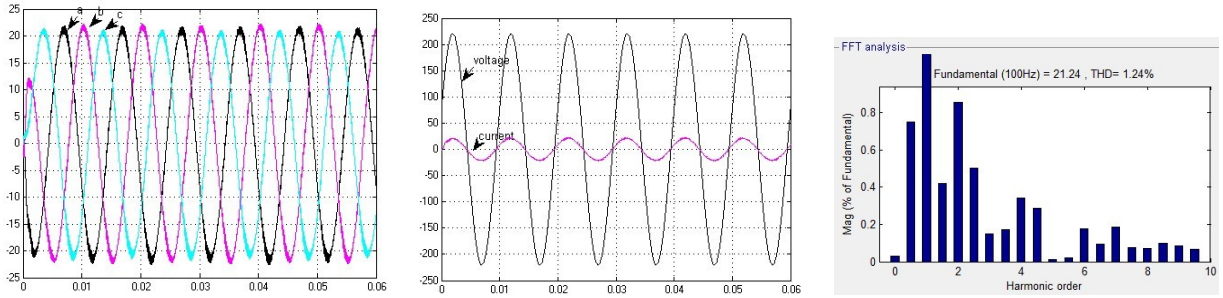
The simulation results of DMC based on the [2u1d] modulation method with inclusion of the unbalanced three-phase voltage control are delineated in Figure 6.41. Figure 6.41(a) shows the waveforms of three phase output currents, Figure 6.41(b) shows the waveforms of feedback current and grid voltage, and Figure 6.41(c) shows FFT analysis of output current. In these figures, the vertical axis is current for (a), voltage and current for (b), and



(a) Three phase output currents (b) Waveforms of feedback current and grid voltage (c) FFT analysis of output current

Figure 6.40: Waveforms without control

fundamental amplitude for (c). Three phase output currents are balanced with inclusion of unbalanced three phase voltages control. Unity power factor of feedback current is nearly equal to 1. With inclusion of unbalanced three phase voltages control, THD is much smaller than without unbalanced three phase voltages control and fundamental value is also close to ideal value 22. The compensation of unbalanced three-phase voltage in DMC based on the [2u1d] modulation method works well.

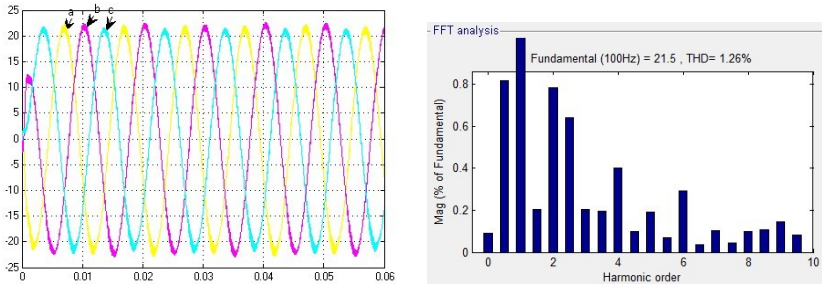


(a) Three phase output currents (b) Waveforms of feedback current and grid voltage (c) FFT analysis of output current

Figure 6.41: Waveforms with inclusion of control

In the practical applications, noise will be added when measuring data. As .Figure 6.42 shows, after adding band-limited white noise into the input signal, the fundamental amplitude and THD is increased.

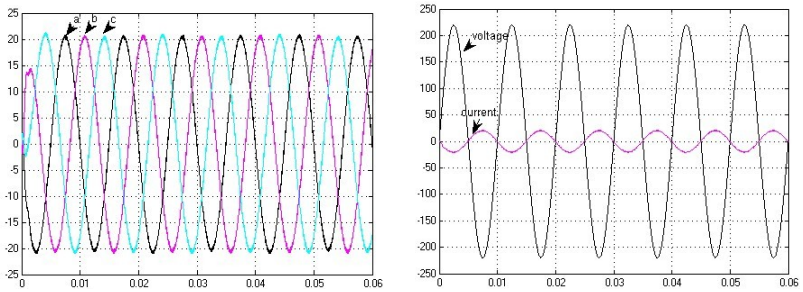
5) Energy feedback control Phase and amplitude control method is used as energy feedback control method. The simulation results of the energy feedback control for DMC



(a) Waveforms of feedback currents (b) FFT analysis of feedback current with inclusion of control

Figure 6.42: Waveforms after adding band-limited white noise

based on [2u1d] modulation method are delineated in Figure 6.43. Figure 6.43(a) shows waveforms of three phase feedback current and Figure 6.43(b) shows waveforms of feedback current and grid voltage. In these figures, the vertical axis is current for (a), voltage and current for (b). The sinusoidal feedback current is drawn as anti-phase (energy feedback) with the corresponding grid voltage; it shows the feedback control algorithm works well.



(a) Waveforms of three phase feedback currents (b) Waveforms of feedback current and grid voltage

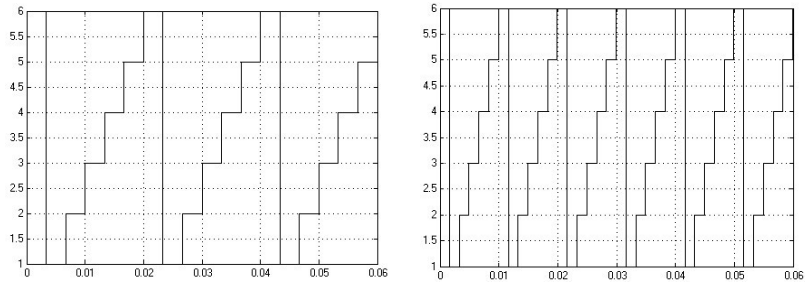
Figure 6.43: The waveforms of feedback currents and grid voltage

6.2.2 Indirect matrix converter

1) Two-level indirect matrix converter A) SVPWM method

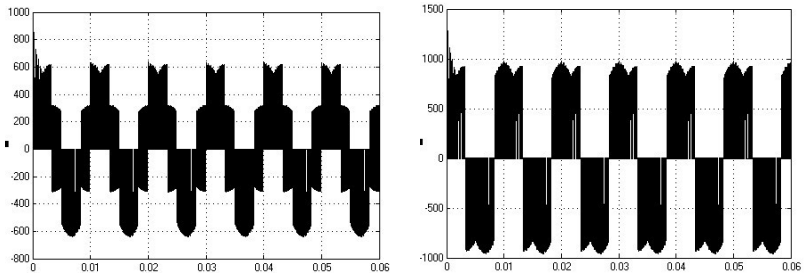
The simulation parameters are equivalent to the parameters of DMC. The simulation results of indirect matrix converter based on the SVPWM method are delineated from Figure 6.44 to Figure 6.46. Figure 6.44 shows input current sectors and output voltage sectors. In

these figures, the vertical axis is sector number for (a) and (b), voltage for (c) and (d). Figure 6.45 shows the output phase a voltage before filtering and output line voltage V_{ab} before filtering. In these figures, the vertical axis is voltage. Figure 6.46 shows the three-phase output currents and desired sinusoidal output voltage. In these figures, the vertical axis is voltage and current for (a), current for (b). From the figures, we can see that output current is tracking desired output voltage in real-time.



(a) Input current sectors (b) Output voltage sectors

Figure 6.44: The waveforms of sectors

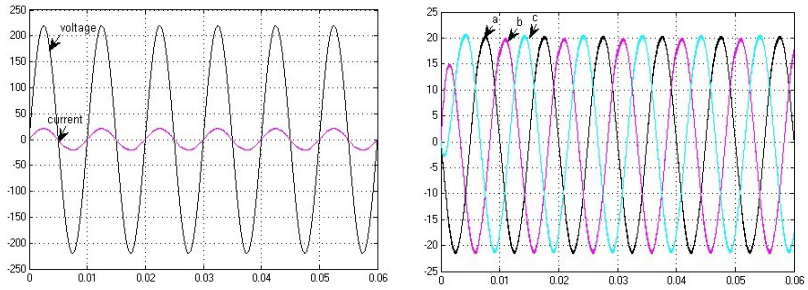


(a) Output phase voltage before filtering (b) Output line voltage before filtering

Figure 6.45: Output voltages before filtering

B) A simplified and unified carrier-based modulation method for indirect matrix converter

The simulation results of indirect matrix converter based on the single carrier-based modulation method are delineated in Figure 6.47 and Figure 6.48. The simulation results are obtained by using the continuous single carrier-based modulation method IV. Figure

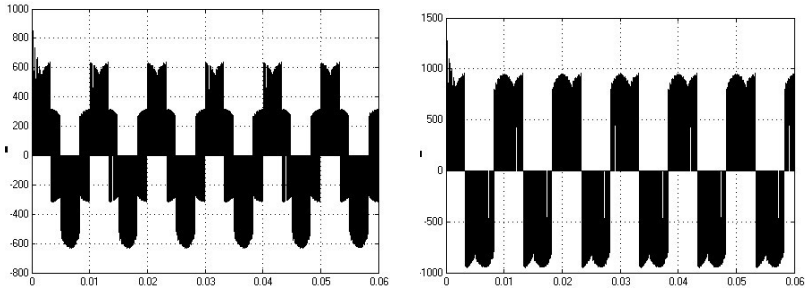


(a) Output current and desired voltage

(b) Three-phase output currents

Figure 6.46: Output currents and desired voltage

6.47 shows the output phase a voltage before filtering and output line voltage V_{ab} before filtering. In these figures, the vertical axis is voltage. Figure 6.48 shows the waveforms of output reference voltage v_A and output feedback current i_A. In these figures, the vertical axis is current for (a), voltage and current for (b). The feedback current is in phase with the desired output voltage.



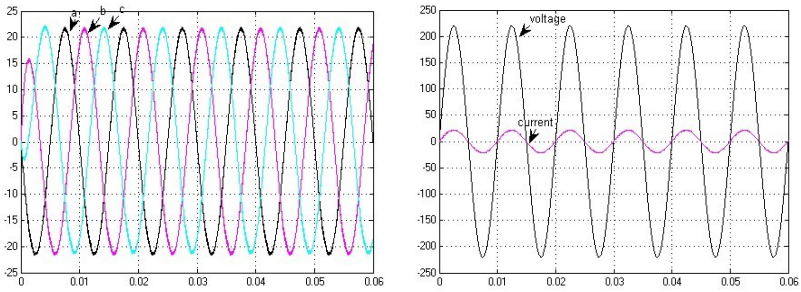
(a) Output phase voltage before filtering

(b) Output line voltage before filtering

Figure 6.47: Output voltages before filtering

C) Unbalanced three-phase voltage control and energy feedback control

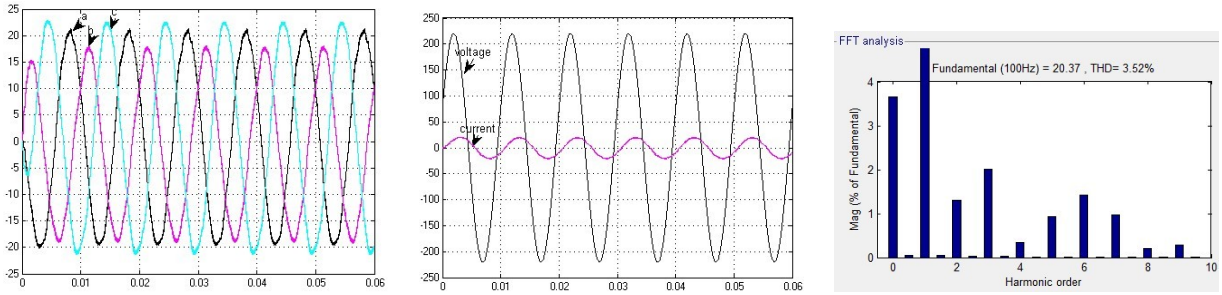
The simulation parameters are equivalent to the parameters of direct matrix converter. The simulation results of IMC based on the single carrier-based modulation method IV without unbalanced three-phase voltage control are delineated in Figure 6.49. Figure 6.49(a) shows the waveforms of three phase output currents, Figure 6.49(b) shows the waveforms of feedback current and grid voltage, and Figure 6.49(c) shows FFT analysis of feedback



(a) Output current and desired voltage (b) Three-phase output currents

Figure 6.48: Output currents and desired voltage

current. In these figures, the vertical axis is current for (a), voltage and current for (b), and fundamental amplitude for (c). From the figures, we can see that three phase currents are under unbalanced conditions, unity power factor of feedback current is not equal to 1, THD is large, and fundamental value is small.

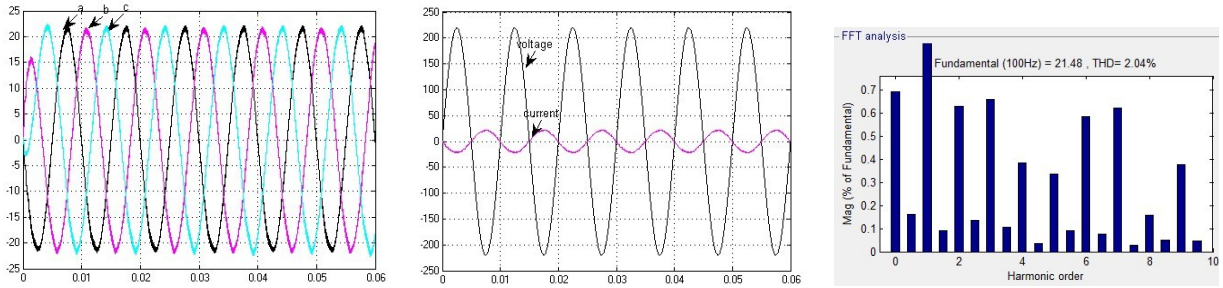


(a) Three phase output currents (b) Waveforms of feedback current and grid voltage (c) FFT analysis of output current

Figure 6.49: Waveforms without control

The simulation results of three-phase IMC based on the modulation method I with inclusion of unbalanced three-phase control are delineated in Figure 6.50. Figure 6.50(a) shows the waveforms of three phase output currents, Figure 6.50(b) shows the waveforms of feedback current and grid voltage, and Figure 6.50(c) shows FFT analysis of output current. Three phase output currents are balanced with inclusion of unbalanced three phase voltages control. In these figures, the vertical axis is current for (a), voltage and current for (b), and fundamental amplitude for (c). Unity power factor of feedback current is nearly equal to

1. With inclusion of unbalanced three phase voltages control, THD is much smaller than without unbalanced three phase voltages control, and fundamental value is also close to ideal value 22. The compensation of unbalanced three-phase voltage in IMC based on modulation method I work well. The sinusoidal feedback current is drawn as anti-phase (energy feedback) with the corresponding grid voltage; it shows the feedback control algorithm works well.



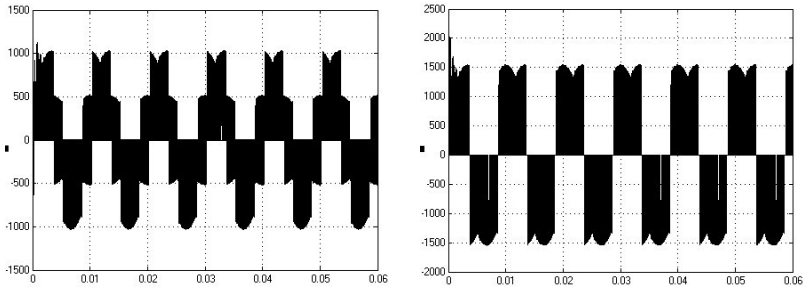
(a) Three phase output currents (b) Waveforms of feedback current and grid voltage (c) FFT analysis of output current and grid voltage

Figure 6.50: Waveforms with inclusion of control

2) Three-level IMC A) A single carrier-based modulation method I for three-level output stage matrix converter

The simulation parameters are equivalent to the parameters of three-level output stage matrix converter except magnitude of input voltage is 900V. The simulation results of indirect matrix converter based on the SVPWM method are delineated in Figure 6.51 and Figure 6.52. Figure 6.51 shows the output phase a voltage before filtering and output line voltage V_{ab} before filtering. In these figures, the vertical axis is voltage. Figure 6.52 shows the three-phase output currents and desired sinusoidal output voltage. In these figures, the vertical axis is voltage and current for (a), current for (b). In these figures, the vertical axis is voltage and current for (a), current for (b). From the figures, we can see that output current is tracking desired output voltage in real-time. The sinusoidal feedback current is drawn as anti-phase (energy feedback) with the corresponding grid voltage; it shows the feedback control algorithm works well.

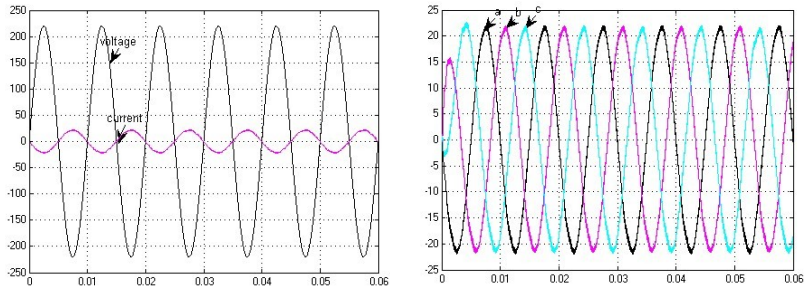
B) Unbalanced three-phase voltage control



(a) Output phase voltage before filtering

(b) Output line voltage before filtering

Figure 6.51: Output voltages before filtering

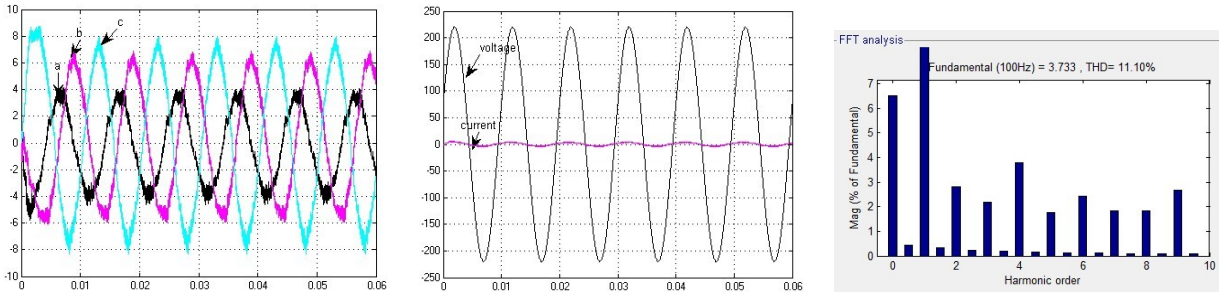


(a) Output current and desired voltage

(b) Three-phase output currents

Figure 6.52: Output currents and desired voltage

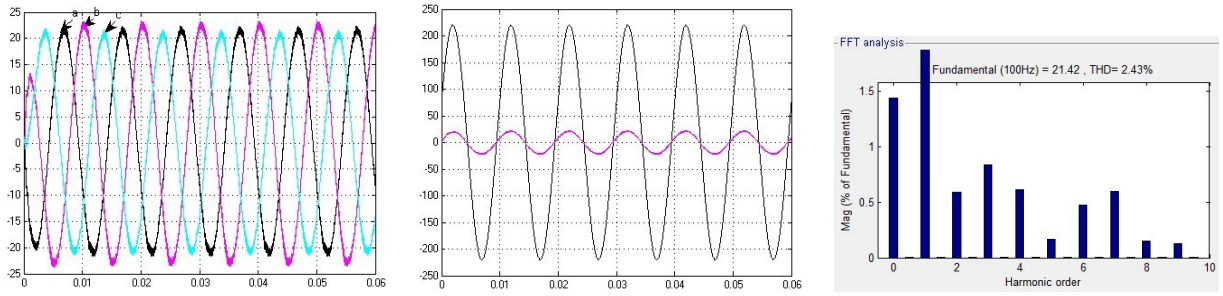
The simulation parameters are equivalent to the parameters of direct matrix converter except magnitude of input voltages are 1400V, 1500V, and 1600V. The simulation results of IMC based on the single carrier-based modulation method IV without unbalanced three-phase voltage control are delineated in Figure 6.53. Figure 6.53(a) shows the waveforms of three phase output currents, Figure 6.53(b) shows the waveforms of feedback current and grid voltage, and Figure 6.53(c) shows FFT analysis of feedback current. In these figures, the vertical axis is current for (a), voltage and current for (b), and fundamental amplitude for (c). From the figures, we can see that three-phase currents are under unbalanced conditions, unity power factor of feedback current is not equal to 1, THD is large, and fundamental value is small.



(a) Three phase output currents (b) Waveforms of feedback current and grid voltage (c) FFT analysis of output current

Figure 6.53: Waveforms without control

The simulation results of IMC based on the modulation method I with inclusion of unbalanced three-phase voltage control are delineated in Figure 6.54. Figure 6.54(a) shows the waveforms of three phase output currents, Figure 6.54(b) shows the waveforms of feedback current and grid voltage, and Figure 6.54(c) shows FFT analysis of output current. Three phase output currents are balanced with inclusion of unbalanced three phase voltages control. In these figures, the vertical axis is current for (a), voltage and current for (b), and fundamental amplitude for (c). Unity power factor of feedback current is nearly equal to 1. With inclusion of unbalanced three phase voltages control, THD is much smaller than without unbalanced three phase voltages control, and fundamental value is also close to ideal value 22. The compensation of unbalanced three-phase voltage in IMC based on the modulation method I work well.



(a) Three phase output currents (b) Waveforms of feedback current and grid voltage (c) FFT analysis of output current

Figure 6.54: Waveforms with inclusion of control

Chapter 7

Conclusions

7.1 Conclusions

This dissertation aims to investigate and study the modulation and control of the energy feedback VSI and MC. By studying reference works, some research works are proposed and investigated. The work presented in this thesis has made contribution to the research of modulation and control of energy feedback VSI and MC. Modulation methods and control methods for VSI and MC are investigated and proposed.

• Based on the traditional SVPWM method and simplified SVPWM method for two-level VSI, the intrinsic relationship between SVPWM and SPWM is deduced. According to the intrinsic relationship between SVPWM and SPWM, and the simplified SVPWM method for two-level VSI, the simplified SVPWM method for three-level inverter is proposed. The unified and simplified SVPWM method for diode clamped multi-level VSI is proposed by researching simplified SVPWM algorithm for two-level and three-level VSI. Compared with the conventional SVPWM algorithm, the simplified and unified SVPWM algorithm can be more easily implemented in a digital device because the state of each power switch can be determined directly and easily without much calculation. The advantages of new method are that realization of SVPWM is greatly simplified and complexity increases little as the number of inverter level increases. Unlike the conventional SVPWM algorithm which needs coordinate transformations, trigonometric calculations, sector number identification etc., the state of each power switch can be determined directly and easily without much calculation by using the simplified algorithm [9][10].

• According to the existing DSVPWM for two-level VSI, the additional simplified DSVPWM algorithm for multi-level diode clamped VSI is investigated and proposed by

skillfully arranging two zero voltage vectors. A constant-variable k ranging from 0 to 1 is used to generate larger number of modulating waves. The DSVPWM methods, including both six basic types and eight additional types of DSVPWM, is proposed and studied. By this method, switching losses of inverter are optimized and life expectancy of inverter can be increased by using a suitable discontinuous modulation technique [11].

• Based on the study of existing overmodulation techniques published in literatures, modified two two-mode strategies and two single-mode strategies are investigated and proposed which can manage the transition from the linear control range to six-step operation smoothly. The proposed overmodulation techniques make continuous control of the output voltage up to the maximum voltage with a smooth linear transition characteristics and minimum distortions. The strategy is simple and suitable for practical digital implementation [12].

• A detailed analysis and uniform compensation of dead-time effect in three-phase VSI is proposed. To prevent a short circuit in the dc-link, a switching delay time is inserted into PWM signals. This dissertation analyzes dead-time effects and proposes an approximate solution based on characteristics of simplified SVPWM. The approximation is a result of avoiding the need to determine output current direction. The value of dead time is adjusted online by the value of corresponding phase current. The deviation of voltage vectors caused by dead time effect is directly compensated to three phase reference voltages. This dead time compensation method is suitable for multi-level DCVSI [13].

• A simplified control strategy to balance dc-link capacitor voltage for multi-level DCVSI based on DSVPWM is investigated and proposed. On the basis of simplified SVPWM algorithm for multi-level inverter and discontinuous modulation, simplified DSVPWM methods are proposed to be applied to balance the dc-link capacitor voltage. The proposed control method changes the path and duration time of the neutral point current, making the voltages of series connected dc-link capacitors equal. While maintaining low switching losses and

achieving the effectiveness voltages balancing, this method does not adopt any additional hardware or complex calculations [14].

• A simplified control scheme based on simplified SVPWM is proposed for three-phase multi-level DCVSI under unbalanced grid voltage conditions. On the basis of simplified SVPWM algorithm, the concept of voltage modulation by using offset voltage is applied to an unbalanced three-phase grid voltage control method. The algorithm is based on simple control structure and does not demand any filter for obtaining symmetrical components, e.g. notch or anti-resonant filter. The control objective is to balance three phase output currents and minimize THD of the output currents without ac current sensors under unbalanced grid voltage conditions. The proposed compensation algorithm uses the instantaneous values of three phase grid voltages to calculate compensation value and directly compensates to simplified DSVPWM algorithm. Unity power factor operation is feasible when the system is balanced and a constant input power can be achieved in the unbalanced situation.

• By investigating direct current control method and indirect current control method, a phase and amplitude control method (indirect current control method) is used for energy feedback VSI system. We can calculate power factor σ and ratio of pulse width modulation M as long as grid voltage E_a, dc bus voltage V_{dc}, and feedback current are determined. The desired output voltages are directly used for simplified SVPWM algorithm to control power switches to track the desired output currents. Through the phase and amplitude control theory we can achieve unity power factor control of energy feedback if we know σ and M.

• A unified carrier-based modulation method for DMC is investigated and proposed. Various types of PWM methods are generated by using the offset voltage, changing slope of carrier waveform, and adjusting the free parameters in the modulation algorithm. The proposed method is equivalent to the SVPWM for two-level and three-level VSI. A new viewpoint to understand the MC modulation method such as single carrier-based modulation technique for two-level VSI and double carrier-based modulation technique for three-level VSI is presented. Using the proposed method, DPWM for the DMC is proposed. Therefore,

a unified simple algorithm suitable for the digital implementation of all continuous and discontinuous PWM strategies is proposed [15].

• By studying commutation method, a detailed analysis and compensation of dead-time effect in DMC is proposed. Through analysis of dead time effect, deviations of voltage vectors caused by dead time effect are dependent on the direction of output currents. The dead-time distorts the output waveform, however, and increases THD. Dead time compensation is necessary to minimize current distortion and reduce THD. This dissertation analyzes dead-time effects and proposes a solution based on characteristics of simplified carrier-based modulation. The solution is a result of avoiding the need to determine output current direction. The value of dead time is adjusted online by the value of corresponding phase current. The deviation of voltage vectors caused by dead time effect is directly compensated to three phase reference voltages. This dead time compensation method is suitable for DMC [16].

• Unbalanced three-phase input and output voltage control for DMC is proposed by using the unbalanced three-phase output voltage control method for VSI. The phase and amplitude control method for DMC is proposed and studied by using the phase and amplitude control method for VSI.

• By investigating traditional SVPWM method for two-level and three-level IMC, a unified carrier-based modulation method for DMC is used to two-level and three-level IMC. Using the proposed method, DPWM for the IMC is proposed. Therefore, a unified simple algorithm suitable for the digital implementation of all continuous and discontinuous PWM strategies is proposed.

• When the commutation method is four-step current commutation on the rectifier side and dead time commutation on the inversion side, we can use dead time compensation for DMC on the rectifier side and dead time compensation for VSI on the inversion side. Unbalanced three-phase input and output voltage control for IMC is proposed by using the unbalanced three-phase output voltage control method for VSI. The phase and amplitude

control method for IMC is proposed and studied by using the phase and amplitude control method for VSI.

7.2 Future work

Even though good simulation results are obtained for the proposed modulation and control of energy feedback VSI and MC, the followings are some of the interesting topics in which further research can be undertaken in order to develop the modulation and control of energy feedback VSI and MC.

• To improve the accuracy of the algorithm, accurate measurements of required current and voltage values are needed. The research is needed to improve the measurement accuracy.

• Due to the high frequency of the power switches, computing speed need to be improved.

• Further improve the dynamic response of the phase and amplitude control method. More research is needed to the grid-connected control.

• More effective unbalanced three-phase control for VSI and MC needs further research.

• To propose simplified modulation method which uses zero state, further research is needed to the modulation method for three-level IMC.

• The overmodulation method for matrix converter and neutral-point control method for three-level indirect matrix converter are still need to be researched.

• The proposed modulation algorithms and control methods for energy feedback VSI and MC are verified by simulation results (MATLAB/SIMULINK), the modulation algorithms and control methods need to be verified by practical applications.

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