Extreme Environment Reliability of Components for Computing with SAC305 and Alternative High Reliability Solders

by

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Abstract

The semiconductor and packaging industries have been moving away from the use of Lead (Pb) due to the increasing awareness of the health and safety concerns surrounding its use. For many applications, the industry has moved from eutectic Sn-Pb solder to the near-eutectic Sn-Ag-Cu (SAC) solders, and more applications – including those considered “extreme environment” – are likely to take place in the near future. However, the reliability of electronic assemblies with SAC solder joints has proven hard to predict based on previous experience with SnPb solders.

The reliability of electronic solder joints is determined by a variety of factors including bulk solder properties and failure mechanics. Both the composition and microstructure of the solder joint will affect its bulk properties. Although an initial microstructure will be present following assembly – which will involve one or more soldering steps – this structure will continue to evolve over the lifetime of the joint. The microstructure and microstructural evolution of the Sn-Ag-Cu solders differ significantly from that of eutectic SnPb solders. Because of the risks and uncertainties involved, a new body of reliability engineering knowledge must be built of for the Sn-Ag-Cu solders based on application-specific process and service parameters.

This experiment considers the thermal cycle reliability of an assortment of different electronic components and evaluates them on a 0.200” (200 mils) thick printed circuit board. Two substrate materials are tested: FR4-06 and Megtron6. Organic

Solderability Preservative (OSP) surface finish is used with all test vehicles. The primary solders for package attachment in this experiment are SnPb and SAC305. Two solders designed for high-temperature reliability are also considered, including a Bi-doped SAC material and the six-element alloy Innolot (Sn3.8Ag0.7Cu3Bi1.4Sb0.15Ni).

Isothermal storage at high temperature was used to accelerate the aging of the assemblies. Aging Temperatures are 25ºC, 50ºC, and 75ºC. Aging durations are 0-Months (No Aging, baseline), 6-Months, 12-Months, and 24-Months. The test vehicles were then subjected thermal cycles of -40°C to +125°C on a 120-minute thermal profile in a single-zone environmental chamber to assess the solder joint performance.

The as-reflowed failure data (No Aging Group) was found to follow specific reliability trends depending on the type and size of the component. The smaller plastic ball grid array (BGA) packages show the following pattern in Characteristic Life value, listed from best to worst: (1) Matched Innolot, (2) [S]SAC305 doped with [P]Innolot, (3) Matched SAC305, and (4) Matched SnPb. However, when considering the effects of isothermal aging on the relative reliability of various packages, the data indicate that even components that show similar initial reliability trends may display differences following aging. Following isothermal aging, several components exhibit higher reliability when paired with SnPb solder than with the SAC solder materials.

Significant differences in reliability were seen between equivalent packages mounted to the two substrate materials tested (FR4-06 and Megtron6). For all of the over-molded plastic BGA components, reliability was higher on the standard glass-epoxy material (FR4-06). Performance for these packages on the high-electrical-performance polyphenylene oxide (PPO) blend material (Megtron6) was much worse. The degradation

in reliability with aging were also found to be worse on Megtron6 for the Sn-Ag-Cu materials when paired with these components. However, the two Super-BGA components – SBGA 304 and SBGA 600 – dramatically reverse this substrate-based reliability trend.

For the smaller plastic BGA packages, Innolot doping (micro-alloying) appears to be an effective strategy for improving characteristic life. However, as component size and pitch increase, this improvement seems to wane (and in some cases reverse itself altogether). This may be attributable to under-doping of the large-component joints. Based on assembly-level reliability, the “paste doping” strategy appears to be a promising approach to improve reliability in high-stress environments, but one that requires significant further study.

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Table of Contents

Abstract ii

Acknowledgments v

List of Tables xii

List of Figures xiii

List of Abbreviations xix

Chapter 1 1

1.1 Printed Circuit Assemblies 1

1.2 Printed Circuit Assemblies: Introduction 6

1.2.1 Through-Hole Mount Technology (THMT) 7

1.2.2 Surface Mount Technology (SMT) 9

1.2.3 Area Arrays 14

1.2.4 No-Lead (Lead-Less) Components 17

1.2.5 Internal Structure of Common Surface Mount Components 18

1.3 Substrates for Electronic Assemblies 20

1.3.1 Types of PCBs 21

1.3.2 Laminate Substrates 23

1.3.3 Solder Mask 24

1.3.4 PCB Surface Finishes 25

1.4 Trends in Electronic Packaging 27

Chapter 2...31

2.1 Soldering 31

2.2 Solder Joints for Electronic Assemblies 32

2.2.1 Overview of Surface Mount Manufacturing Process.. 33

2.2.2 Solder Paste and Flux.. 35

2.3 Solder Joint Properties 37

2.3.1 Properties Important to Manufacturability.. 41

2.3.2 Properties Important to Reliability.. 42

2.4 A Brief History of Solder in Electronic Assemblies.. 42

2.4.1 Tin-Lead Solder: An Industry Dominating Solution 43

2.4.2 Tin-Lead Solders: The Decline 46

2.4.3 Tin-Lead Solder: Searching for a Replacement... 48

2.4.4 Electronic Solders: Near-Eutectic Sn-Ag-Cu (SAC) Solders................................. 49

2.5 Eutectic SnPb Solder: A Closer Look... 51

2.5.1 Eutectic SnPb Solder: Material Properties... 53

2.5.2 Eutectic SnPb Solder: Microstructural Evolution.. 53

2.6 Near-Eutectic Sn-Ag-Cu (SAC) Solder: A Closer Look 56

2.6.1 Near-Eutectic Sn-Ag-Cu (SAC) Solder: Material Properties 61

2.6.2 Near-Eutectic Sn-Ag-Cu (SAC) Solder: Microstructural Evolution 62

2.7 Other Elements commonly found in Tin-Rich Solders... 63

2.7.1 Silver (Ag) 64

2.7.2 Bismuth (Bi).. 65

2.7.3 Copper (Cu) 65

2.7.4 Indium (In) 65

2.7.5 Antimony (Sb) 66

2.7.6 Zinc (Zn) 66

Chapter 3 67

3.1 Introduction... 67

3.2 Failure Modes in Electronic Assemblies 68

3.3 Characteristic Solder Joint Failures 70

3.3.1 Typical BGA Joint Failure Locations... 71

3.3.2 Some Factors Affecting BGA Solder Joint Failures... 73

3.3.3 Experimentally Locating BGA Solder Joint Failures 74

3.4 Understanding Solder Joint Failures.. 76

3.4.1 Fatigue.. 78

3.4.2 Creep & Grain Boundary Sliding 79

3.4.4 Effects of Thermal Cycling on Solder Joints 82

3.4.5 Failure Mechanics 83

3.5 Predicting Solder Joint Reliability under Thermal Cycling 85

3.5.1 Analytical Solutions 86

3.5.2 Numerical Methods 88

3.5.3 Experimental Methods 90

3.6 Experimental Methods: Thermal Cycle Testing 91

3.6.1 Thermal Cycle Testing: Statistical Analysis 94

Chapter 4 100

4.1 Introduction 100

4.2 Thermal Cycle Reliability of Sn-Pb and Sn-Ag-Cu Solders, As Reflowed 101

4.3 Reliability Effects of Composition on Sn-Ag-Cu (SAC) Solders 102

4.4 Reliability Effects of Process Parameters on Sn-Ag-Cu Solders 104

4.5 Reliability Effects of Test Parameters on Sn-Ag-Cu Solders 105

4.6 Effects of Isothermal Aging on Sn-Pb and Sn-Ag-Cu Solders 108

4.6.1 Effects of Isothermal Aging on Sn-Ag-Cu Solders: Mechanical Properties 109

4.6.2 Effects of Isothermal Aging on Sn-Ag-Cu Solders: Reliability Data 112

4.7 Impact of Current Work 114

Chapter 5 116

5.1 Electronic Assemblies and Solder Joints 116

5.2 Test Vehicle Design – TC1-SRJ Test Board 117

5.3 Test Vehicle: Components and Circuit Board Assemblies (CBAs) 121

5.4 Test Plan.. 124

5.5 Surface Mount Assembly.. 127

5.6 Experimental Methods 133

5.6.1 Experimental Methods: Thermal Cycle Test Parameters and Equipment 134

5.6.1 Experimental Methods: The Effects of Test Magnitude...................................... 137

5.6.2 Experimental Methods: Data Acquisition and Monitoring Equipment 143

5.6.3 Experimental Methods: Data Analysis Techniques and Software........................ 149

5.6.4 Experimental Methods: Failure Analysis Protocol and Methods 151

Chapter 6 153

6.1 Weibull Graphs and Results... 153

6.2 CABGA 36 [6mm, 0.8mm pitch] 154

6.3 CABGA 208 [15mm, 0.8mm pitch] 155

6.4 CABGA 256 [17mm, 1.0mm pitch] 162

6.5 CTBGA 84 [6mm, 0.5mm pitch]... 166

6.6 CVBGA 97 [5mm, 0.4mm pitch] 169

6.7 CVBGA 432 [13mm, 0.4mm pitch] 171

6.8 Memory Module [LGA Socket + PGA] 174

6.9 PBGA 1156 [35mm, 1.0mm pitch]... 177

6.10 SBGA 304 [31mm, 1.27mm pitch].. 181

6.11 SBGA 600 [45mm, 1.27mm pitch] 183

Chapter 7 188

7.1 Failure Analysis 188

7.2 Preliminary Failure Analysis: FR4-06 Substrates 188

7.2.1 FR4-06: No Aging Group (0 Cycles) 189

7.2.2 FR4-06: No Aging Group (1000 Cycles) 194

7.2.3 FR4-06: No Aging Group (2000 Cycles) 195

7.2.4 FR4-06: No Aging Group (3000 Cycles) 197

7.3 Preliminary Failure Analysis: Megtron6, No Aging, 3000 Cycles 201

7.3.1 Megtron6: CABGA 208, [P]SAC305, [S]SAC105 202

7.3.2 Megtron6: CABGA 208, [P]SAC305, [S]SAC305 204

7.3.3 Megtron6: SBGA 304, [P]SAC305, [S]SAC305 206

7.3.4 Megtron6: CABGA 256, [P]SAC305, [S]SAC305 208

Chapter 8 210

8.1 Results and Conclusions: TC1-SRJ Project 210

8.2 Ongoing and Future Work: TC1-SRJ Project 217

8.3 Ongoing and Future Work: Follow-On and Related Projects 218

References 220

List of Tables

Table 1.1. Principal Types of Gull Wing and J-Lead Packages [2,6]................................ 9

Table 1.2. Principal Types of Gull Wing and J-Lead Packages [2,6].............................. 14

Table 1.3. Area Array Packages [5,6].. 16

Table 1.5. Some Important Properties of Printed Circuit Boards.................................... 22

Table 2.1. Large Organizational efforts to find Pb-Free solutions [28]........................... 49

Table 2.2. Select properties of 63Sn-37Pb [2].. 53

Table 2.3. Phases in Sn-Ag-Cu Solder [from NIST] 58

Table 2.4. Properties of some component materials [3]. 61

Table 3.1. Effects of some Design Parameters on BGA Package Fatigue Life [6,55]. 74

Table 3.2. Common Non-destructive and Destructive Interconnect FA Methods [56].... 75

Table 3.3. CTE values of some circuit assembly materials [3]. 79

Table 3.4. Dwell Temperatures for TC testing by application [3,13,51,65]..................... 93

Table 4.1. Summary of Lead-Free and Sn-Pb Thermal Cycle data from [51]............... 101

Table 5.1. Top-Side CBAs.. 123

Table 4.2. Bottom-Side CBAs. 124

Table 4.3. Test Plan. 126

Table 5.4. Thermal Cycle Chambers used for testing the TC1-SRJ test vehicle............ 137

Table 5.5. US and European Grip Paper standard systems [112]................................. 151

Table 8.1. Rough joint composition numbers. [S]SAC305 with [P]Innolot.................. 212

List of Figures

Figure 1.1. Levels of Packaging. Adapted from [2]. 2

Figure 1.2. Dual In-Line Package (DIP) [2]. 3

Figure 1.3. First Level Packaging options [2]........ 3

Figure 1.4. Printed Circuit Board........ 4

Figure 1.5. Through-Hole Mount vs. Surface Mount Attachment. Adapted from [2]. 5

Figure 1.6. Through-Hole Mount Technology Component and Solder Joint [2,5]. 9

Figure 1.7. Gull Wing Leads (left) and J-Leads (right) [2]. 13

Figure 1.8. Area Array Component and Solder Joint [5]........ 15

Figure 1.9. No-Lead Component and Solder Joint [5]........ 17

Figure 1.10. Standard BGA (left) and Cavity-Down BGA (right) 19

Figure 1.11. Some Ball Grid Array Structure Options [5]........ 20

Figure 1.12. NSMD versus SMD PCB lands........ 25

Figure 1.13. Increases in Packaging Density over time [5]. 29

Figure 2.1. Key steps in SMT Assembly [3]. 33

Figure 2.2. Solder Paste (modified from [3])........ 35

Figure 2.3. (Conceptual) Equilibrium Bond Length vs. Bonding Energy [20]. 39

Figure 2.4. Tension and Shear (left) and typical Stress-Strain curves (right) [20]. 40

Figure 2.5. Strain Hardening [20]. 40

Figure 2.6. Tin-Lead Binary Phase Diagram [23]. 44

Figure 2.7. Rough Time-Line of Major Lead-Free Solder Consortia [28]. 49

Figure 2.8. Tin-Lead Binary Eutectic Phase Diagram [2]. 51

Figure 2.9. Interdiffusion in Lamellar Solidification [30]. 52

Figure 2.10. Microstructural Evolution in Eutectic SnPb Solder [17]............................. 55

Figure 2.11. From NIST: Sn-Ag-Cu Phase Diagrams. 57

Figure 2.12. (a) Optical and (b) BSE images of typical SAC Joint Microstructure [32].. 60

Figure 2.13. Cu pad IMCs with HASL after 500 hours of aging [37]. 60

Figure 2.14. Cu pad IMCs with Ni/Ag after 1000 hours of aging [37]. 60

Figure 2.15. IMC Evolution at Ni Pad [36]. 62

Figure 3.1. Common Flip-Chip Failure Modes [6]. 70

Figure 3.2. Common Joint Failure Modes. 71

Figure 3.3. FEA model: Induced stress maximized at the upper corner of the joint [6]... 72

Figure 3.4. Stress and Strain vs. DNP [6]. 73

Figure 3.5. Some Failure Modes seen in BGA-type solder joints. 77

Figure 3.6. (a) Deformation Mechanism Map for Silver [61], (b) Stages of Creep [20].. 81

Figure 3.7. Grain Boundary Sliding [61]. 81

Figure 3.8. DNP Model [2]. 86

Figure 3.9. Schematic of Thermal Cycle. 91

Figure 3.10. Cyclic Fatigue Damage during Thermal Cycling [3]. 92

Figure 3.11. Probability Density Function (pdf) and its application to Reliability [66]... 94

Figure 3.12. Bathtub Curve [67]. 95

Figure 3.13. A Weibull Plot on Probability Paper [50]. 99

Figure 4.1. From [68]. Survey of the market share of lead-free solders. 100

Figure 4.2. From [51]. TC Characteristic life vs. Silver content, CABGA192. 103

Figure 4.3. A series of Nanoindentations in a SAC solder joint [104]. 111

Figure 4.4. TV7 Project: Characteristic Life degradation with aging for CABGA 208. 113

Figure 5.1. Size Comparison: TC1-SRJ vs. Sheet of Paper.. 118

Figure 5.2. TC1-SRJ Test Vehicle: Top-Side (Schematic and Un-assembled PCB). 120

Figure 5.3. TC1-SRJ Test Vehicle: Bottom-Side (Schematic and Un-assembled PCB).120

Figure 5.4. Summary of some important sub-groups from the Test Matrix.................. 126

Figure 5.5. Speedline Technologies MPM Momentum.. 127

Figure 5.6. Juki KE-2080L (left) and Juki JX3 (right) pick-and-place machines. 128

Figure 5.7. Heller a1913 MKIII Reflow Oven. 129

Figure 5.8. Setup Board used for Thermal Profiling of the Reflow Oven..................... 129

Figure 5.9. SnPb Reflow Profile, Bottom-Side... 130

Figure 5.10. SnPb Reflow Profile, Top-Side. 131

Figure 5.11. Lead-Free Reflow Profile, Bottom-Side... 131

Figure 5.12. Lead-Free Reflow Profile, Top-Side. 132

Figure 5.13. TC1-SRJ Assemblies being stacked for Isothermal Aging. 134

Figure 5.14. TC1-SRJ Thermal Profile, Theoretical (left) vs Experimental (right). 135

Figure 5.15. Thermotron, 16 cft (left) and ETC16 (right) Thermal Cycling Chambers. 136

Figure 5.16. Several hundred TC1-SRJ boards being sorted at Auburn University....... 138

Figure 5.17. IB-4 Interface Board (Schematic and PCA)... 140

Figure 5.18. GRD-IB-1 Ground Interface Board (Schematic and PCA)....................... 141

Figure 5.19. Setup Page of IB-4 Sampling Program. 142

Figure 5.20. Scanning Page of IB-4 Sampling Program... 143

Figure 5.21. Electrical Daisy Chaining for continuity testing. 144

Figure 5.22. TC1-SRJ boards stacked (left) and corresponding wiring (right). 145

Figure 5.23. Monitoring System for the TC1-SRJ experiment (24A Group, LHS). 146

Figure 5.24. Diagram of the TC1-SRJ Monitoring System. 147

Figure 5.25. Weibull++ Software User Interface. 150

Figure 6.1. All data at 12-Months of Aging (75ºC). CABGA 36 – [P][S]SnPb............ 154

Figure 6.2. Key Groups on FR4-06. CABGA 208 – No Aging.................................... 156

Figure 6.3. Characteristic Life values. CABGA 208 – FR4-06 – No Aging. 157

Figure 6.4. All data on FR4-06. CABGA 208 – 12-Month Aging – 75ºC. 158

Figure 6.5. Key groups on FR4-06. CABGA208 – No Aging and 12-Month (75ºC). ... 159

Figure 6.6. All data on Megtron6. CABGA 208 – 12-Month Aging – 75ºC................. 160

Figure 6.7. Key Groups at 24-Months Aging (75ºC). CABGA 208.............................. 161

Figure 6.8. All data on Megtron6. CABGA 208 – 24-Month Aging – 75ºC................. 162

Figure 6.9. All data on FR4-06. CABGA 256 – No Aging. 163

Figure 6.10. All data on FR4-06. CABGA 256 – 12-Month Aging – 75ºC. 164

Figure 6.11. All data on FR4-06. CABGA 256 – 24-Month Aging – 75ºC. 165

Figure 6.12. All data on Megtron6. CABGA 256 – 24-Month Aging – 75ºC............... 166

Figure 6.13. All data at No Aging. CTBGA 84 – 12-Month Aging – 75ºC. 167

Figure 6.14. All data at 12-Months of Aging (75ºC). CTBGA 84. 168

Figure 6.15. Substrate Comparison. CVBGA 97 – [P][S]SnPb – No Aging................. 169

Figure 6.16. Substrate Comparison. CVBGA 97 – [P][S]SnPb – 12-Months at 75ºC. .. 170

Figure 6.17. Solder Paste Comparison. CVBGA 432 – FR4-06 – No Aging................ 172

Figure 6.18. All data on FR4-06. CVBGA 432 – 12-Month Aging – 75ºC. 173

Figure 6.19. All data at 24-Months (75°C). CVBGA 432. Note horizontal axis. 174

Figure 6.20. All data at No Aging. Memory Module. 175

Figure 6.21. Aging Temperature Comparison. Memory Module – 12-Month Aging. ... 176

Figure 6.22. All data at 1300 cycles. Memory Module – 24-Month Aging – 75°C. 177

Figure 6.23. Characteristic Life values. PBGA 1156 – FR4-06 – No Aging. 178

Figure 6.24. Substrate Comparison. PBGA 1156 – [P][S]SnPb – No Aging. 179

Figure 6.25. Key groups on FR4-06. PBGA 1156 – No Aging and 12-Month (75°C). . 180

Figure 6.26. All data on FR4-06. PBGA 1156 – 24-Month Aging – 75°C. 181

Figure 6.27. SBGA 304 – FR4-06 – No Aging. 182

Figure 6.28. Weibull Plot: SBGA304 – No Aging and 12-Month (75°C)...................... 183

Figure 6.29. Characteristic Life values. SBGA 600 – FR4-06 – No Aging. 184

Figure 6.30. Substrate Comparison. SBGA 600 – No Aging – [P][S]SnPb. 185

Figure 6.31. SBGA 600 – FR4-06 – With Heatsinks – 12-Month Aging – 75°C. 186

Figure 6.32. SBGA 600 – FR4-06 – With Heatsinks – 24-Months Aging – 75°C. 187

Figure 7.1. SE (left) and BSE (right) micrographs, Polishing Procedure 1. 190

Figure 7.2. EDS Line Scan, Polishing Procedure 1, PCB-Side IMC Layer. 191

Figure 7.3. EDS MAPS, Polishing Procedure 1, PCB-Side IMC Layer. 191

Figure 7.4. EDS Line Scan, Polishing Procedure 1, Component-Side IMC Layer. 192

Figure 7.5. BSE micrograph, Polishing Procedure 2. 193

Figure 7.6. SE (left) and BSE (right) electron micrographs. Polishing Procedure 3. 194

Figure 7.7. Board- (left) and Component-Side (right) IMC, SAC305, 1000 TCs. 195

Figure 7.8. Board- (left) and Component-Side (right) IMC, Innolot, 1000 TCs. 195

Figure 7.9. Overview SE Micrograph showing Characteristic Solder Joints. 196

Figure 7.10. Board- (left) and Component-Side (right) IMC, SAC305, 2000 TCs. 196

Figure 7.11. Roughly equivalent cracking (left); crack initiation at board-side (right).. 197

Figure 7.12. Overview SE Micrograph showing Characteristic Solder Joints. 198

Figure 7.13. A variety of crack propagation modes, SAC305-paste. 199

Figure 7.14. Overview SE Micrograph showing Characteristic Solder Joints. 200

Figure 7.15. A variety of crack propagation modes, Innolot-paste. 201

Figure 7.16. Overview BSE Micrograph showing Characteristic Failure Modes. 202

Figure 7.17. Roughly equivalent cracking at Board/Component-Side of two joints...... 203

Figure 7.18. Predominant Board-Side Cracking. 203

Figure 7.19. Overview BSE Micrograph showing Characteristic Failure Modes. 204

Figure 7.20. Primary cracking at IMC Boundaries. 205

Figure 7.21. Traumatic failure in Right-most Joint. 206

Figure 7.22. Overview BSE Micrograph showing Characteristic Solder Joints............ 207

Figure 7.23. Primary cracking along the Top-Side IMC Boundaries 207

Figure 7.24. Overview SE Micrograph showing Characteristic Failure Modes............ 208

Figure 7.25. Roughly equivalent cracking at Top and Bottom 209

Figure 8.1. Solder Paste Comparison, No Aging Group... 211

Figure 8.2. Substrate Comparison, No Aging Group.. 213

Figure 8.3. Characteristic life vs. Isothermal Aging Time. Key packages, FR4-06. 215

Figure 8.4. Characteristic life vs. Isothermal Aging Time. Key packages, Megtron6. .. 215

List of Abbreviations

BGA	Ball Grid Array
BSE	Back-Scattered Electron
GPIB	General Purpose Interface Bus
LGA	Land Grid Array
PCA	Printed Circuit Assembly
PCB	Printed Circuit Board
PGA	Pin Grid Array
RTD	Resistance Temperature Detector
SAC	Tin (Sn) – Silver (Ag) – Copper (Cu)
SCPI	Standard Commands for Programmable Instruments
SEM	Scanning Electron Microscope
SE	Secondary Electron
SMC	Surface Mount Component
SMR	Surface Mount Resistor
SnPb	Tin – Lead
THMC	Through-Hole Mount Component
UBM	Under-Bump Metallurgy

Chapter 1
A Brief Introduction to Electronic Assemblies

1.1 Printed Circuit Assemblies

In 1996, the Electronic Industry surpassed the Automotive Industry to become the largest industry in the world [1]. Since that time, the industry has continued to grow and mature, finding new applications such as smartphones and wearables that have transformed and may continue to transform the way that people interact with each other and incorporate information into their lives. Electronics have come become indispensable in industry, consumer applications, and for public record keeping and civic involvement, and they show little sign of slowing down their ever expanding influence.

Active electronic components begin life as a Silicon “die,” or chip, which is diced from a single-crystal Silicon Wafer. The silicon chip contains many solid-state electronic devices (transistors, resistors, inductors, and capacitors) that have been defined and connected to form functional electrical circuitry [2]. The production of such semi-conductor-based electronic devices is one of the crowning technological achievements of the modern era, involving a laundry list of fields including semiconductor physics, chemical and materials engineering, surface science and thin-film physics and engineering, electrical engineering and design, very large systems integration, and advanced optical processing technologies, to name a few. Continuing advancements in photolithography, materials, and manufacturing practices have enabled seemingly endless increases in the functional density of silicon chips – immortalized in the public

imagination via Moore's Law – and provided the driving force for many of the necessities and conveniences of modern life.

However, the story of the silicon chip does not end at wafer dicing. The silicon dies need protection from the outside environment and will often need to be combined with other electrical elements so as to create the desired circuit. This is where the Packaging of the electrical components comes in. Here, by packaging, we are not referencing containers intended for shipping. Rather, we mean "the placement and connection of many electronic and electro-mechanical components…in an enclosure which protects the system from the environment and provides easy access for routine maintenance" [2]. There are four (4) main functions of electronic packaging [2]:

1. Signal Distribution
2. Power Distribution
3. Heat Dissipation
4. Protection (Mechanical, Chemical, & Electromagnetic)

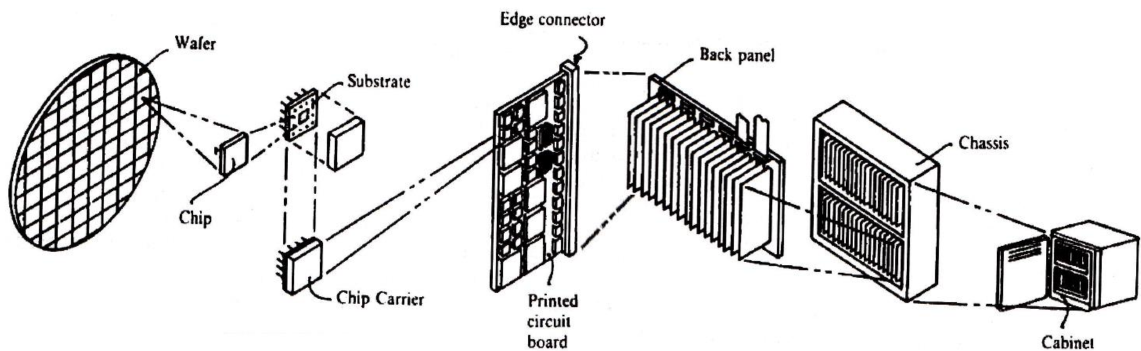


Figure 1.1. Levels of Packaging. Adapted from [2].

The first level of electronic packaging is the Chip Carrier. Typically, the silicon die is mechanically affixed to a lead-frame or interposer layer, and electrical connections are made between the chip and carrier using small wires ("wire bonding") or solder joints

("flip-chip BGA", etc.) [2,3]. Chip Carriers come in a vast array of options, differentiated by the type of attachment to the substrate, internal structure, materials used for construction, as well as other factors such shape, size, vertical standoff, and lead pitch. In addition to active components (i.e. components that involve some form of gate or switching action), a variety of passive components – such as resistors, capacitors, or inductors – are available. These can also range significantly in their internal complexity, and are found in a plethora of sizes and shapes [3].

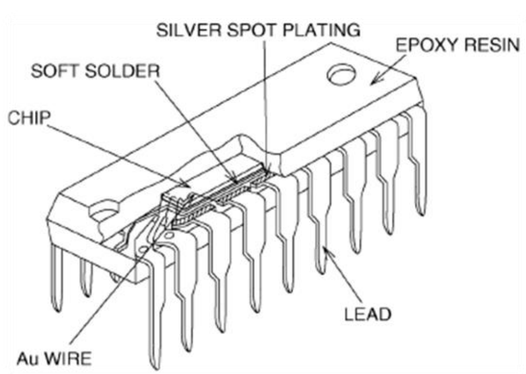


Figure 1.2. Dual In-Line Package (DIP) [2].

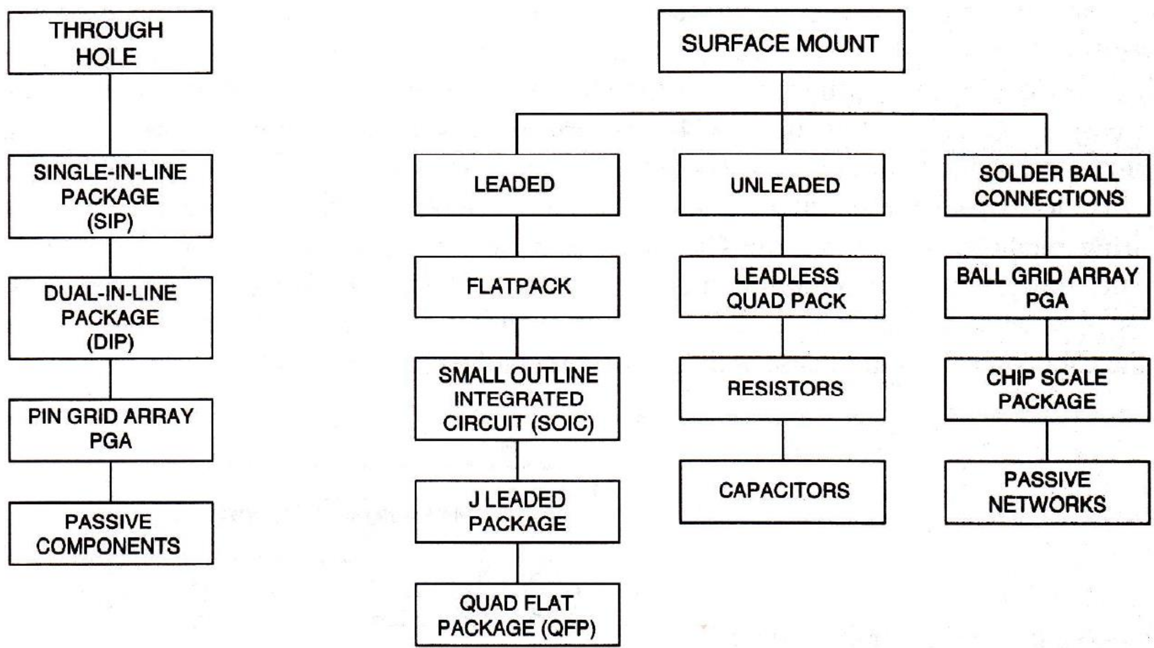


Figure 1 Error! No text of specified style in document.**.3. First Level Packaging options [2].**

The second level of packaging is the electronic assembly, or Printed Circuit Assembly (PCA). Anyone who has opened up their PC to view its "motherboard" has

experience in dealing with electronic assemblies. Just as a chip carrier has an interposer layer or lead-frame, an electronic assembly has a substrate – usually called a Printed Circuit Board, or PCB. The Printed Circuit Board is typically a rigid laminate constructed of layers of fiberglass-epoxy composite. (Other materials, such as ceramic, metal/metal-core, and flexible polymer are also possible.) This substrate also contains external – and often internal – Copper metallization layers. The Copper layers are photolithographically defined so as to provide the 'wires' for the electrical circuit (as well as to provide thermal design enhancements, etc.). Thus, the Printed Circuit Board provides a flat surface for mechanical fixturing of the components, thermal redistribution and dissipation, electrical isolation (bulk substrate, typically) and electrical connection (via the copper traces) where needed to form the appropriate circuit [2,3].

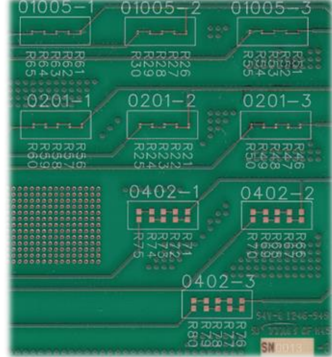


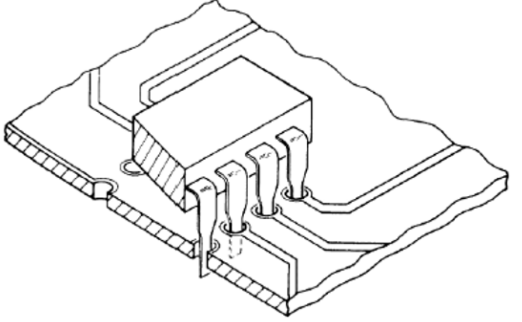
Figure 1.4. Printed Circuit Board.

The components are attached to the substrate using solder. The solder is a metal – typically an alloy – of reasonable melting point that is used to form a metallurgical bond between the component-side leads or terminations and the corresponding copper pads (known as "lands") on the Printed Circuit Board surface. The solder joints formed during assembly provide an electrical, thermal, and mechanical connection between the PCB and the component [2,3]. Solder and its use in Printed Circuit Assemblies will be discussed in Chapter 2.

Since the 1970s, the electronics packaging industry has been dominated by two component "mounting" technologies: each of which has its own associated soldering technology, manufacturing process, component design restrictions, etc. Through-hole

Mount Technology, or THMT, is typified by component leads that pass through the Printed Circuit Board and are clinched on the backside prior to soldering via the Wave Soldering process. Surface Mount Technology, or SMT, involves components that are attached to the copper pads ("lands") on the same side of the PCB using a Reflow Soldering process [3].

Through-Hole Mount Attachment **Surface Mount Attachment**



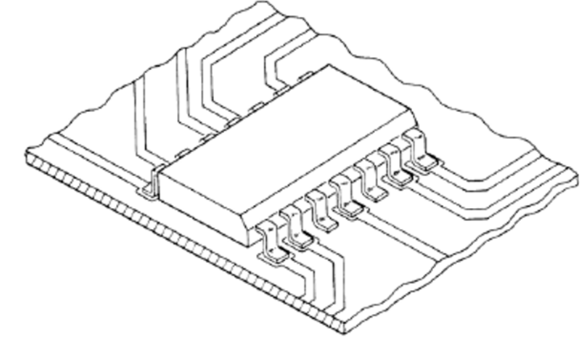


Figure 1.5. Through-Hole Mount vs. Surface Mount Attachment. Adapted from [2].

For a typical Printed Circuit Assembly (PCA) containing only surface mount components, some of the key assembly steps include paste printing, component placement and solder reflow. Solder paste is a thickened flux/solvent vehicle containing small (around 35-45 microns in diameter for Type 3 paste) spheres of the solder alloy. It is applied to the substrate's exposed copper pads, or "lands," via a screen printing process. In modern applications, this mostly involves a metal stencil and squeegee blade. Components are carefully placed so that their leads, BGA balls, or metalized pads are sitting (ideally) directly on top of the appropriate paste deposit. During solder reflow, the assembly passes through a multi-zone reflow oven/furnace, culminating with the solder alloy exceeding its Liquidus temperature for a short period of time – typically 30-90 seconds. Above liquidus, the solder is fully melted, and it "wets" to the metal surfaces. Upon cooling a solid and continuous metallic joint has been formed [3].

1.2 Printed Circuit Assemblies: Introduction

Although computers existed before its invention, the advent of the modern electronics industry depends principally on the invention of the transistor in 1947. Prior to the creation of the transistor, electronics were famously dominated by slow, large, power-hungry, and failure-prone Vacuum Tubes. Electronics were traditionally wired and assembled by hand. This process was slow and inefficient, and reliability was dismal, so the incentives to keep things simple were numerous. J. R. Pierce, the Bell Labs engineer credited with coining the term “transistor” is quoted as saying “Nature abhors the vacuum tube” [4]. Once unencumbered of the limitations of the vacuum tube, engineers were freed to imagine circuits of ever-growing complexity.

Although this was a significant boon, it soon became clear that a new approach to the traditional hand-assembly and wiring approaches was needed in order to deal with the large number of high-quality interconnects (“wires”) needed. Additionally, smaller transistors (and other circuit components) and shorter interconnects were desirable so as to increase circuit response speed (reduce propagation delay) [4].

In response, the monolithic semiconductor “integrated circuit,” or IC, was invented by Jack Kilby of Texas Instruments in 1958. The integrated circuit was also separately developed by Robert Noyce, one of the co-founders of Intel, about half a year later. Noyce also developed techniques for depositing interconnects by adding a top layer of metal and then etching away unused areas, making his device more practical than Kilby’s [4].

To fully realize the potential of the integrated circuit, electronic packaging designers now needed to solve many of the same challenges that motivated its invention. The assembly of electronics at the time involved hand-wired, “point-to-point,” interconnects, and (often) no substrate of any kind [3]. The creation of the printed circuit board – or PCB – predates the invention of the transistor, but printed circuit boards initially had few uses. Now, suddenly, the printed circuit board became a very attractive option as a mounting surface, and new types of integrated circuit “packages” and techniques for mounting them to PCBs were needed [4].

1.2.1 Through-Hole Mount Technology (THMT)

The basic idea of through-hole mount technology consists of drilling vias (through-holes) in the Printed Circuit Board, passing component leads through these vias, and crimping them on the backside. This is followed by soldering (adding solder around) the component leads, which joins them to the appropriate metal traces of the PCB [3]. The principal method of soldering in through-hole mount assembly is ‘wave soldering’ technique, which involves a standing wave of molten solder. The PCB is passed over the wave, soldering all of the through-hole connections at once. After some initial quality concerns had been allayed, the electronic packaging industry was quick to adopt wave soldering technology, as the throughput advantages were overwhelming.

Later, techniques for metal plating of the through-holes were created, and the need for greater component densities was met by first adding a second metal interconnect layer (on the component side of the board) and eventually by adding multiple interconnect layers built into the printed circuit board. Automated placement machines

were also developed that would take a THMT component and quickly place it on the PCB (including all necessary wire cutting, forming, and crimping).

One of the enduring advantages of THMT, even when compared to more modern approaches, is the excellent reliability of the solder joints. Assuming voiding is controlled, the soldered through-hole connection is extremely sound mechanically, and the lead/pin attached to the through-hole mount component (THMC) effectively takes up stresses resulting from thermal expansion in the PCB substrate, etc. These advantages allowed THMT to dominate the electronic packaging arena from the 1950s to the 1980s. Even to the present day, THMT is still used in certain applications, such as when components are too large for surface-mounting technology due to high power requirements or mechanical limitations, or subjected to very high mechanical stress.

On the downside, since through-hole mount technology requires vias to be drilled through the printed circuit board, I/O connections can only be placed along two edges of the components without compromising the mechanical integrity of the PCB. Lead pitch reductions are limited by the same concern, as well as by the fact that smaller through-hole leads will not support the (generally heavy) though-hole mount components. Additionally, since the through-holes pass all the way through the PCB, all metal interconnects must be routed around them to avoid shorting. Eventually, it became clear that a new technology was needed to achieve higher I/O and component densities and keep pace with IC advances.

The basic form of a Through-Hole Mount Technology Component and Solder Joint are shown below in Figure 1.6. These solder joints are typically the easiest joints to

inspect by eye, with metallic luster, surface appearance, wetting/feathering angle, wetting/filleting coverage, etc. all being readily apparent to the unaided eye.

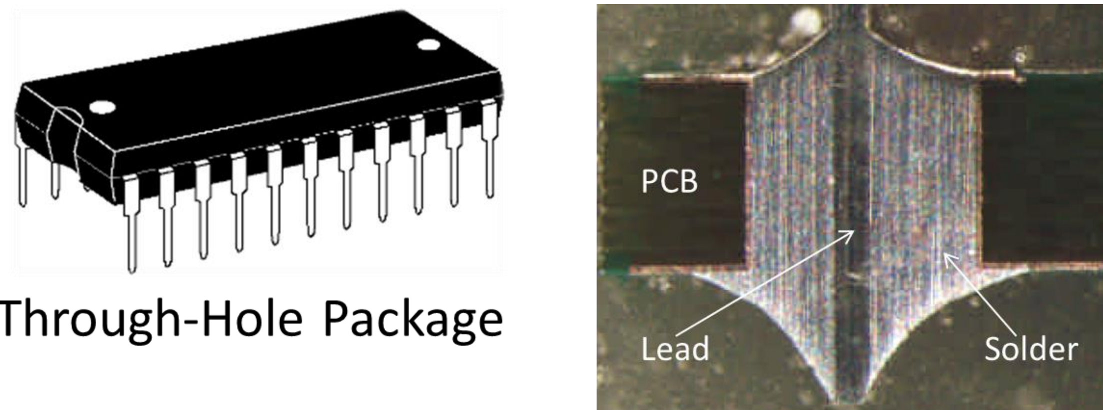


Figure 1.6. Through-Hole Mount Technology Component and Solder Joint [2,5].

There are a variety of Through-Hole Mount Components, including varieties of the package types listed below. The Dual In-Line Package (DIP) was the most popular THMC, with many forms available such as PDIP (Plastic DIP), CDIP (Ceramic DIP), CERDIP (CDIP, Glass Sealed), SDIP (Skinny DIP), etc. Table 1.1 lists a few of the primary types of THMC.

Table 1.1. Principal Types of Gull Wing and J-Lead Packages [2,6]

Single In-Line Package (SIP)		Zig-Zag In-Line Package (ZIP)	
Dual In-Line Package (DIP)			

1.2.2 Surface Mount Technology (SMT)

Surface Mount Technology was originally developed in the 1960s, but was ahead of its time. High component prices (due largely to low production volumes), high capital

investment requirements during switchover, a lack of widespread technical knowledge on how to effectively use it, and other factors led to SMT being used only in niche applications (primarily military and aerospace) until the 1980s. As THMT ran aground of its physical limitations, however, SMT became more attractive [3]. By the 1980s, the development of VLSI integrated circuit technology meant that through-hole packaging techniques simply could no longer provide for the necessary I/O capabilities to keep up with industry and consumer demand.

In general, Surface Mount Technology can be described as a process for soldering components directly to the surface of a printed circuit board, foregoing the need for a through-hole. Surface mount components (SMC) were initially similar to through-hole mount components, re-engineered to have short leads of various design (“leaded”) or contact pads (“lead-less”). Rather than using a wave soldering process, surface mount components typically have solder paste pre-applied to the PCB contact pads (through a silk-screening or stencil process). After components are placed on the board, the paste is ‘reflowed’ (heated above Liquidus and then allowed to cool) in a reflow oven, causing it to form a solid joint [3].

SMT brings with it several design advantages compared to THMT. Since no through-holes are required, components can be placed on both sides of a printed circuit board more easily, significantly increasing the useable PCB surface area. Surface Mount Components also provide finer lead pitches, and I/O can be placed around all four sides of the component. SMCs are also typically smaller than their THMC contemporaries, often less than half as large. These allow for significant increases in component and

input/output density. Smaller, lightweight components are also highly desirable in certain applications such as aerospace [3,7].

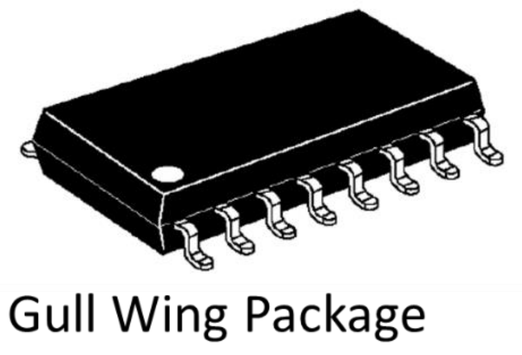
The cost of Surface Mount Components was initially significantly higher than that for Through-Hole Mount Components, but much of this was eventually offset by cost savings via maturation of the part production processes and economies of scale. Today SMCs are typically less costly than their THMC equivalents. Since surface mount components have higher I/O capabilities, the number of functions per component can also be higher, meaning that the cost per function is even more heavily weighted in favor of SMCs. However, more precise interconnect layout technologies are also required, which have offsetting costs associated with them. Since fewer vias need to be drilled into the PCB for surface mount technology-based boards, time and money are saved here. Rework of defective parts is also easier and faster (and therefore lower cost), although it typically requires more expensive equipment up front [3].

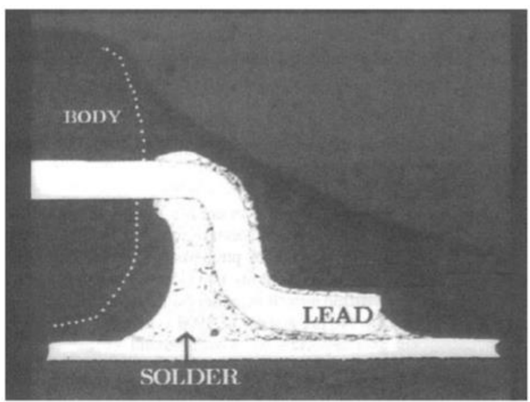
The manufacturing process is generally simpler and faster for surface mount technology, although process parameters need to be determined and maintained to fairly exacting standards. Material handling is easier and fewer placement machines are typically needed, as a single ‘pick-and-place’ machine can install essentially any surface mount component. During the solder reflow operation, the surface tension of the molten solder will cause surface mount components to “self-align” (align correctly to the corresponding PCB pads), leading to higher quality than during THM production. However, reliability can be an issue, as SMT joints tend to be more mechanically fragile [2,3]. One hidden benefit of surface mount manufacturing is worker safety: the most dangerous piece of equipment is generally the pick-and-place machine, which can

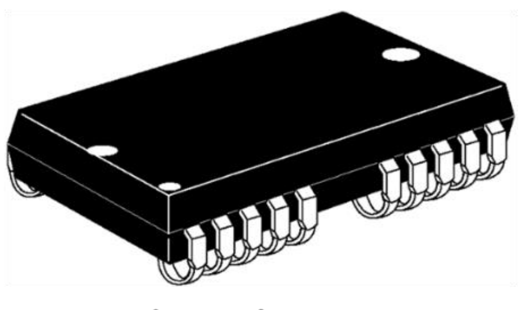
significantly damage hands placed unwarily into it. Through-hole mount technology, on the other hand, generally requires the use of a wave solder machine, which contains a vat of liquid metal solder. Accidents involving a wave soldering apparatus can be quite severe.

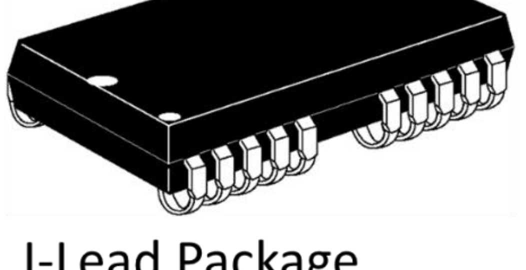
The electrical performance of surface mount interconnects is typically better, due to the shorter leads employed. On the other hand, thermal management can become more complicated, as thinner leads – necessary for finer pitch I/O – also have higher thermal resistance [3]. Smaller components also lead to a higher concentration of thermal energy, exacerbating this problem. Thermal damage during reflow is also a concern. Although the temperature of the solder bath is higher in wave soldering systems, the heating and cooling is somewhat limited to the leads of the through-hole mount components. Surface mount components, on the other hand, experience a mostly identical thermal profile to the reflowed joints themselves.

There are a variety of (perimeter array) surface mount solder joints, each of which will be dictated by the type of lead/attachment to the PCB land. For leaded packages (excluding BGAs), the two most important lead types/shapes are Gull Wing and J-Lead. These are shown schematically in Figure 1.7, below. Note that the geometry of the solder joint differs between the two lead types: the main solder fillet on the Gull Wing joint reaches back toward the body of the component, whereas the main fillet on the J-Lead joint reaches outward away from the component [3].









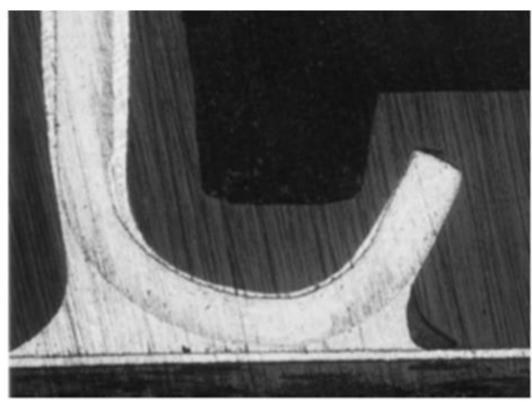


Figure 1.7. Gull Wing Leads (left) and J-Leads (right) [2].

A large variety of Surface Mount Components exist, including both Gull Wing packages, J-Lead packages, and other types yet to be discussed. Table 1.2 lists only a few of the primary categories for Gull Wing and J-Lead packages.

Table 1.2. Principal Types of Gull Wing and J-Lead Packages [2,6]

Gull Wing Packages		J-Lead Packages	
Small Outline IC (SOIC)		Small Outline J-Lead (SOJ)	
Quad Flat Pack (QFP)		Plastic Leaded Chip Carrier (PLCC)	
Small Outline Transistor (SOT)			

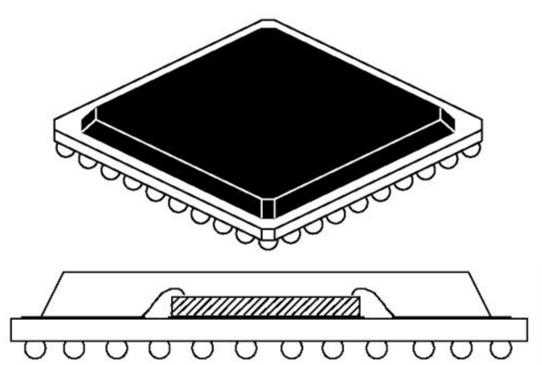
1.2.3 Area Arrays

As input/output requirements for ever more advanced IC components continued to grow, finer pitch I/O interconnects were needed. However, finer pitches come with a range of manufacturability concerns, including increasing fragility of finer-pitch leads and "bridging" (unwanted electrical connection, generally via reflowing solder) between closely spaced contact pads on the Printed Circuit Boards. Eventually, it becomes prohibitively difficult to further decrease the lead pitches for standard SMC chip carriers. Fortunately, a solution had been around for some time.

Once one has made the transition to surface mounted technology, there is no fundamental reason that I/O should be limited to the perimeter of a component. Since no through-holes have to be drilled, I/O can be installed in a full 2-dimensional lattice, or Area Array, under a surface mounted component. For a square component with n leads

along each edge, this approach increases the number of potential I/O channels from approximately 4n to n^2 (although, depending on the component, I/O may cover only part of the allowable area). Area arrays allows one to dramatically increase I/O capabilities without having to decrease the lead pitch [5].

Since Surface Mount Technology had already been developed by the time Area Arrays became popular, the underlying manufacturing and cost structures were fairly similar. (Although time and money had to be spent adapting the existing processes to new I/O strategies such as the Ball Grid Array.) However, higher interconnect counts require more board level wiring, raising per-assembly prices. (As before, per-function prices continued to decrease.) When using BGAs, yield and manufacturability increase with respect to fine pitch chip carriers, as the solder balls used are more robust than traditional leads. As always, shorter interconnects lead to improved electrical performance. Decreasing part sizes and increasing I/O counts lead to thermal management issues [3].



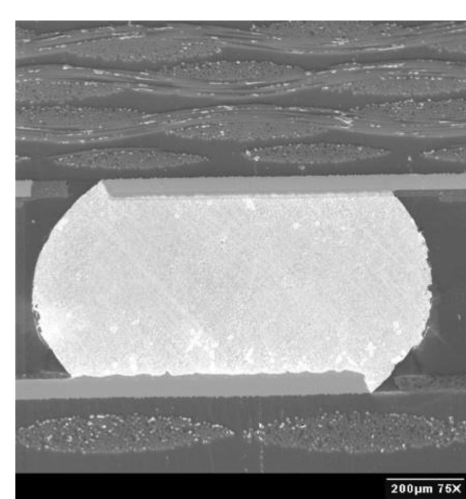


Figure 1.8. Area Array Component and Solder Joint [5].

The predominate Area Array component is the Ball Grid Array, or BGA. Ball Grid Arrays have small spheres of solder (“solder bumps”) applied to the grid of contact pads built into the bottom of the component. These solder bumps are placed onto

corresponding solder paste deposits as if they were component leads. Typically, during reflow soldering, the bumps reflow (i.e. melt) and wet together with the solder paste to form a hamburger shaped solder joint. This "ball collapse" process means that lead Coplanarity is not an issue for BGA packages, although other problems – such as head-in-pillow – can occur.

There are, however, applications in which a higher standoff distance from the printed circuit board is preferred. In such circumstances, a higher melting-point solder can be used for the solder bumps. This substitution increases the standoff height of the component because only the solder paste will reflow during soldering. A similar strategy can be used, except with small columns of (high-T_m) solder instead of spheres, resulting in an even more exaggerated stand-off. This type of component is known as a Column Grid Array (CGA). Another area array is the Pin Grid Array, where thick metal pins (similar to through-hole leads) are attached in lieu of solder spheres or columns [2,3]. This type of package often used in conjunction with socket into which the pins are inserted.

As with the previously described packages, a variety of BGA packages are available, including Plastic BGA (PBGA), Ceramic BGA (CBGA), Thin Chip BGA (CTBGA), Very Thin Chip (CVBGA), Super-BGA (SBGA), and Flip-Chip BGA (FCBGA) packages, among others.

Table 1.3. Area Array Packages [5,6]

Ball Grid Array (BGA)		Pin Grid Array (PGA)	

1.2.4 No-Lead (Lead-Less) Components

The leads on a component (most often made of copper) can flex, and thereby take up the stress generated by linear Coefficient of Thermal Expansion mismatches between a component and printed circuit board. However, for Surface Mount attachment, there is no conceptual reason that one cannot do away with the component leads entirely. In such cases, the bare metal terminations on the bottom of the component are placed directly onto the solder paste deposit atop the corresponding copper lands of the Printed Circuit Board.

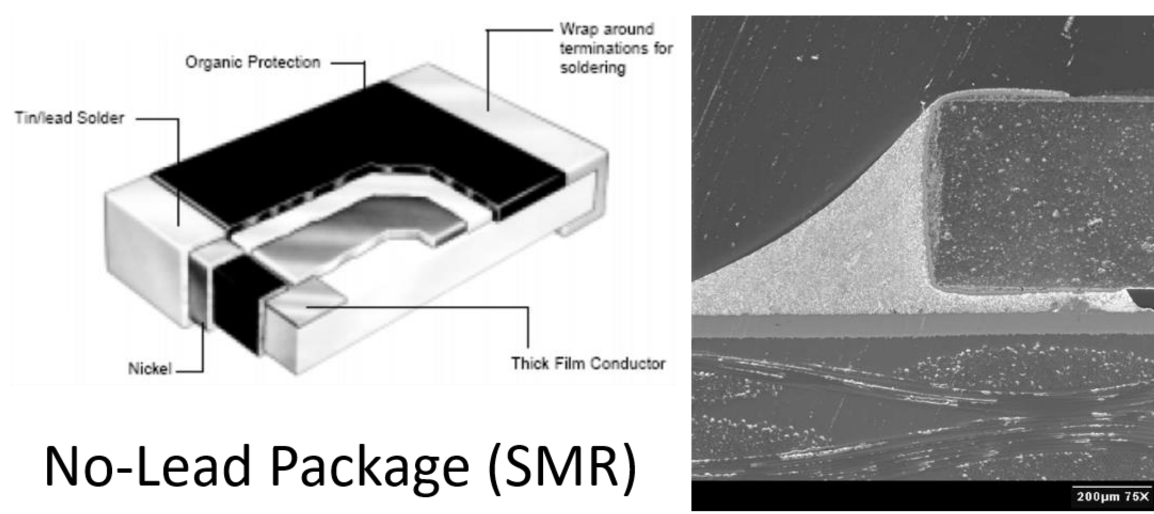


Figure 1.9. No-Lead Component and Solder Joint [5].

Components of this type that lack leads are called Lead-less or No-Lead packages. Typically, the PCB land extends beyond the shadow of the component termination, causing the major solder fillet of the resulting joint to point outward away from the package. Since the solder deposit typically starts at only a few mils in height and slump occurs during reflow soldering, the standoff height of the component is quite low. This low standoff can be a disadvantage for larger packages, as contaminants such as flux residue become difficult to clean from between the PCB and component [2,3].

There are a variety of lead-less components common to surface mount assembly. These include the Surface Mount Resistor (SMR), Metal Electrode Leadless Face (MELF), and Quad Flat No-Lead (QFN) packages. Another type of No-Lead package is the Land Grid Array, or LGA. This is a type of area array the closely resembles the Ball Grid Array, with the key difference that no solder spheres are added to the component terminations.

1.2.5 Internal Structure of Common Surface Mount Components

The production of a typical active Surface Mount Components starts with an appropriate Interposer Layer. The Interposer is a small substrate, with functions similar to those described for the Printed Circuit Board (discussed below), except at the component level (i.e. first level of packaging). In most applications, a rigid organic or ceramic interposer is used. Bismaleimide Triazine (BT) is a common base material for organic laminates, whereas most ceramic interposers are made from a sintered mixture of alumina and glass with a low Coefficient of Thermal Expansion close to that of the silicon die. Other interposer options include the use of a metal lead-frame (generally copper) or a flexible organic film (such as polyimide). Interposers will have one or more copper metallization layers for transferring power and electrical signals between various circuit points [2,3].

The most common method of electrical connection between the Interposer and Silicon Die is the Wire-Bond. Wire-bonding involves connecting an (electrical) pad on the die to a matching pad on the interposer using a thin (10s of microns in diameter) metal wire. The bonding pads are generally 40 or 50 microns on a side. The wire is

bonded to the first pad, drawn out, bonded to the second pad, and clipped. The bonding normally takes place in around 1/10 of a second, and wire-bonding equipment must be able to accurately form many wire-bonds in quick succession. The most common wire material used is Gold (>90% prevalence), with Aluminum being used in some applications. Aluminum wire is used in certain applications, with additional strong interest in copper as a material of the future. The bonding process is performed using thermo-compression in the case of Gold wire-bond and using ultrasonic bonding in the case of Aluminum wire-bonds [2,3].

There are two main internal structures employed for plastic BGA packages with wire-bonded silicon dies. Figure 1.10 shows the standard ("cavity up") configuration on the left and the "cavity down" configuration on the left. The cavity-down package in this figure incorporates a head-slug, which would aid in heat transfer out the 'top' of the component.

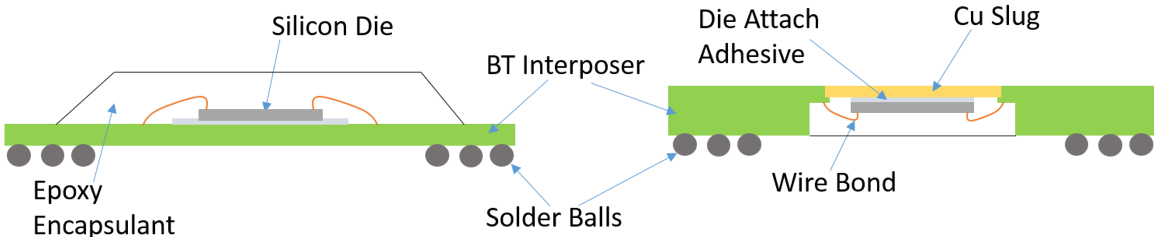


Figure 1.10. Standard BGA (left) and Cavity-Down BGA (right)

Two other options for forming connections between the die and interposer are Flip-Chip attachment and Tape-Automated Bonding (TAB). In Flip-Chip attachment, the silicon die has small solder bumps added to its electrical contact pads. The chip is then inverted and reflow mounted onto the interposer similar to the attachment of a BGA package to the PCB. Tape-Automated Bonding involves the use of a thin, flexible tape onto which the pattern of wire-bonds has been built up using patterned gold-plated

copper film. The die is placed in the same orientation as in wire-bonding, and the tape is aligned above the die and then pressed down such that all electrical connections are made at once using thermo-compression [2,3].

In the case of wire-bonding or tape-automated bonding, the mechanical connection between the die and interposer is made by affixing the bottom of the die to the interposer using a thermally conductive adhesive. In Flip-Chip attachment, and ‘underfill’ material (typically a glass-filled epoxy) is injected under the die and fills the spaces between the solder joints. The solder joints and underfill jointly provide the mechanical attachment. Ceramic packages are then generally hermetically sealed using a ceramic lid. In plastic (organic) packages, the silicon die is over-molded using an epoxy-based molding compound. A variety of internal structures can be created using largely similar production processes [2,3]. A few of the structure options are shown below in Figure 1.11.

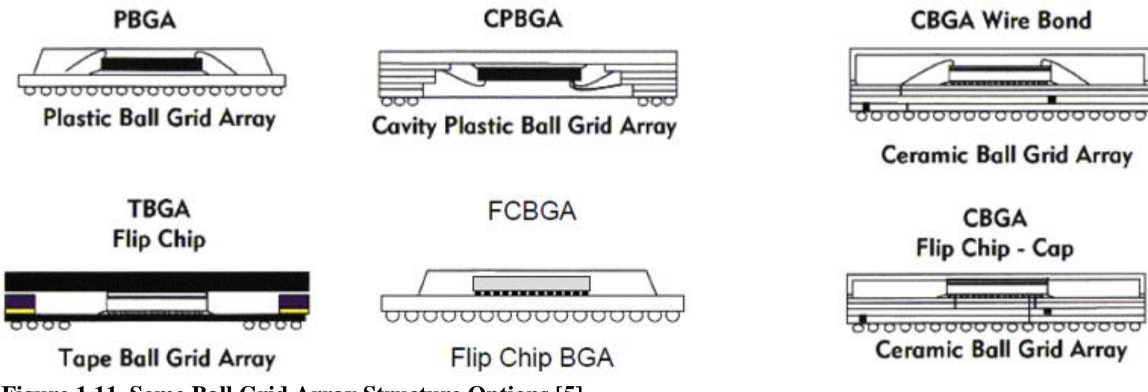


Figure 1.11. Some Ball Grid Array Structure Options [5].

1.3 Substrates for Electronic Assemblies

A Printed Circuit Board, or PCB, consists of a (generally rigid) substrate material with flat metal traces on one or both sides and (potentially) incorporated internally into the substrate itself. Passive and active circuit components then need to be attached

mechanically to the substrate “board” and electrically to the metal traces. The printed circuit board provides mechanical support for the components, while the built-in metal traces provide electrical interconnect between the components. The PCB is also responsible for thermal conduction and dissipation and electrical isolation (anywhere no metal traces are placed). Modern PCBs also incorporate a range of secondary features, including the special markings used in component alignment (fiducials), additional electrical access points for circuit testing, and text and visual markings to aid in identification, service, and maintenance [2,3,7].

1.3.1 Types of PCBs

Printed Circuit Boards are typically classified as either Rigid Laminate, (Organic) Flexible, or Ceramic, with Metal Core Substrates as an additional option. Substrates of each type exhibit very different properties, and the selection of an appropriate substrate for a given product will depend on matching these properties to the application in question, the components to be used, and the processing windows available. One of the most important material properties to be considered in substrate selection is the PCB’s linear Coefficient of Thermal Expansion (CTE). One of the most common strategies for increasing assembly reliability is to match the CTE of the Printed Circuit Board to that of the components, for reasons that will be discussed in Chapter 3 [2,3,7]. Other important properties include:

Table 1.5. Some Important Properties of Printed Circuit Boards.

General Properties	Material Properties
Meets Performance Requirements	Coefficient of Thermal Expansion (CTE)
(Low) Cost	Glass Transition Temperature (if applicable)
Ease of Use / Manufacturability	Stiffness (Modulus)
Durability	Strength and Toughness
	Electrical Properties

Ceramic substrates are normally used with ceramic components, as this provides nearly-ideal matching between the Coefficient of Thermal Expansion (CTE) of the component and PCB. The CTE of ceramic substrates is also sufficiently close to that of silicon that flip-chip reliability is significantly improved versus a rigid laminate. The base materials used are metal oxides such as alumina and beryllia. The conductive traces are added using either a thick-film, additive process or a thin-film, subtractive process. The thin-film process allows for finer line-widths and tolerances, but is more expensive. Ceramic substrates are made up of many layers and there are two processes for combining the various layers together to form the full PCB. The conventional method used with thick-film is a sequential process where each ceramic sheet and conductive layer is applied one at a time, with a firing step between each sheet addition. However, a co-firing process can also be used: wherein all sheets are aligned and fired at the same time. This improves yield and substrate planarity, at the expense of the conductor trimming step [2,3,7].

Flexible (organic) substrates are manufactured by attaching a thin metal foil to a flexible polymer film using an adhesive. As with the ceramic substrates, several layers

can be bonded together to allow for multiple copper layers. This is necessary to form complex circuitry. As with the rigid laminates (discussed below), the copper layers are defined photolithographically. The main advantages over rigid laminates are thinness and the ability to bend or roll-up the substrate, which allows for very different product designs than either ceramic or rigid laminate [2,3,7].

One other type of Printed Circuit Board worth noting is the constraining core substrate. Constraining core substrates, a category that includes metal-core substrates, incorporate a central "core" that is CTE-matched to some other structure (e.g. components, copper traces). In the case of metal core substrates, this core would be a metal sheet or metal-matrix composite material. Outer layers are added above and below the core using conventional rigid laminate construction techniques [2,3,7].

1.3.2 Laminate Substrates

For most commercial applications, a Rigid Laminate substrate is used. As with ceramic substrates, rigid laminates are typically constructed of many layers. In this case, however, each of the layers is composed of a reinforcing cloth that has been impregnated with a polymer matrix material. These composite sheets come in two varieties, known as core and prepreg layers, which are stacked in an alternating fashion and then laminated together (i.e. joined using temperature and pressure) [2,3,7].

The core sheets are (potentially) clad in a copper layer that is photolithographically defined so as to create the appropriate electrical circuitry or thermal distribution layers. These layers are fully cured, allowing them to maintain their shape during the copper processing steps. The copper cladding is typically denoted using

“weights” such as half-ounce or one-ounce: these are meant to represent the weight of copper over a 1 ft^2 area. A one-ounce foil will, therefore, be 1.34 mils or about 34 microns thick [2,3,7].

The prepreg layers are partially cured sheets that will not be fully polymerized until the lamination process takes place. This allows them to conform topologically to the copper traces from the abutting core sheets. Following the lamination process, through-holes are drilled and plated in order to allow for vertical electrical or thermal interconnects [2,3,7].

1.3.3 Solder Mask

The copper traces on the Printed Circuit Board surface must be protected from oxidation and corrosion. In areas where no electrical contact needs to be made, the traces are coated with a Solder Mask, which both protects them from the elements and prevents solder from wetting to them. Solder masks are typically applied either as dry films or wet (screen) printed onto the PCB surface. Common solder mask materials are acrylic or epoxy polymers [2,3,7].

As one of the purposes of the solder mask is to prevent wetting of solder onto the copper during reflow, the contact pads (“lands”) on the Printed Circuit Board surface must be kept clear of solder mask. However, the pads can be ‘defined’ in two different manners. One method is to print the solder mask around the copper pad, leaving a space between the two. Pads that are defined in this way are known as Non-Solder Mask Defined (NSMD). NSMD pads have been shown to provide higher resistance to thermal-mechanical fatigue, as the geometry of the solder-pad interface creates lower stress

concentrations. This has contributed to NSMD pads becoming the standard for PCB lands. Copper pads can also by defined by printing the solder mask such that only the desired pad area is exposed. This type of pad is known as Solder Mask Defined (SMD). SMD pads are used on the bottom pads of component interposers, in large part because they can help prevent delamination between the pads and substrate ("pad lifting/peeling") and tearing of the copper traces [2,3]. Figure 1.11, below, shows the difference between NSMD and SMD pads.

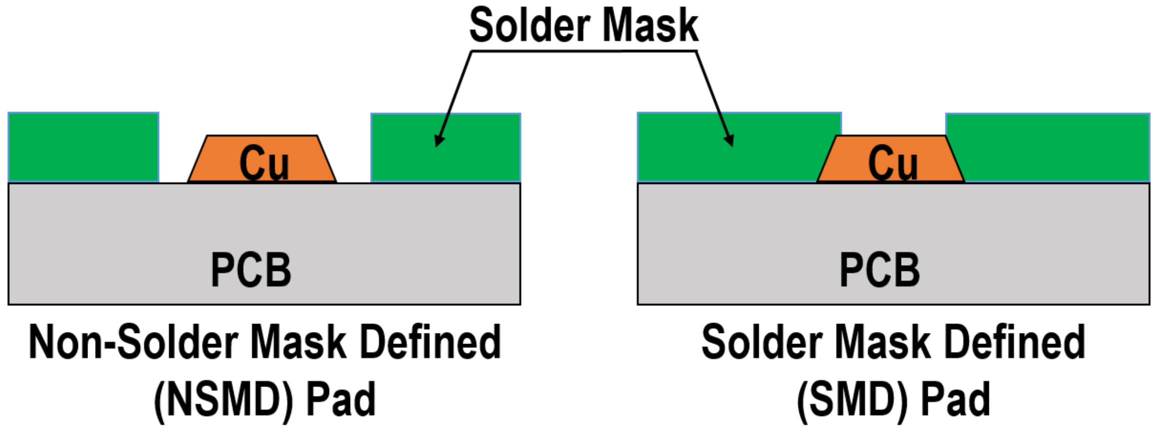


Figure 1.12. NSMD versus SMD PCB lands.

1.3.4 PCB Surface Finishes

Since the Solder Mask cannot extend over the areas where electrical contact needs to be made, a separate "surface finish" is therefore applied to remaining exposed copper areas. This surface finish allows them to be preserved as either conductive test points, fiducials, or lands for solder wetting. Ideally, the surface finish will allow for multiple reflow soldering steps while maintaining the Solderability of the copper lands. A variety of different surface finishes have been developed over the years [2,3,7].

The primary surface finish used with Tin-Lead (SnPb) solder was a thin solder coating applied via the Hot Air Solder Leveling (HASL) process. In the HASL process,

the Printed Circuit Board is dipped into a molten solder bath. The solder clings to any exposed metal surfaces not covered by the solder mask. As the board is pulled up out of the solder bath, a hot air ‘knife’ is used to blow off most of the solder, clearing the vias and through-holes and leaving only a thin coating on the copper surfaces. Historically, the HASL process was primarily used with a Tin-Lead solder bath. The process is more challenging to use with (higher melting temperature) Lead-Free solders, and it does not produce the very flat and uniform coatings needed for fine-pitch components. Therefore, the HASL process has fallen significantly in popularity in recent years [2,3].

A variety of alternative surface finishes are now available that facilitate the production of Lead-Free assemblies and are provide better compatibility with modern components due to their superior planarity and uniformity. Some of the alternative surface finishes now available include:

- Organic Solderability Preservative (OSP)
- Electroless Nickel / Immersion Gold (ENIG)
- Electroless Nickel / Electroless Palladium / Immersion Gold (ENEPIG)
- Immersion Silver (ImmAg, ImAg, IAg)
- Immersion Tin (ImmSn, ImSn, ISn)

Organic Solderability Preservative (OSP) is substantially different from the other coating options, which are all metal-based. OSP is an organic compound-based anti-tarnish coating that relies on a thin (0.7-1.0 microns, typically) carbon-based layer to protect the copper pads from oxidation and contamination. These coatings are the lowest cost surface finish option available. They also provide excellent planarity and solderability, easy visual inspection, and multiple reflow capabilities [2,3].

The other alternative surface finishes rely on the deposition of one or more metals using three primary film deposition processes: Electroplating, Electroless Plating, and Immersion Plating. All three plating processes involve a buffer solution, or plating bath, into which ions of the desired metal are dissolved from an appropriate chemical precursor. The ions will physically impinge on the exposed metal surfaces, but must be bonded in place to produce the coating. The metal ions have a positive electric charge, and providing them with electrons causes them to become neutralized and plate the metal surfaces (a process known as reduction). In Electroplating, the necessary electrons are supplied by passing an electrical current through the existing metal traces. This process is cheap and fast, but each surface to be plated must receive current, so it is not generally used when many discrete pads need to be coated. Electroless Plating replaces the external current (as a source of electrons) with a chemical added to the bath called a Reducing Agent. In Immersion Plating, a reducing agent is not used. Instead, the base metal (generally Copper) surrenders electrons to the bath, ionizing some of the surface. A more noble metal such as Tin or Silver absorbs the electrons and replaces the surface ions. This replacement reaction is self-limiting and produces a coating that is non-porous, extremely thin, and dense [2].

1.4 Trends in Electronic Packaging

Subsequent to the invention of the integrated circuit, the history of the IC industry can largely be described by a continuous decrease in the size of transistors (and other circuit components) and a corresponding increase in their density, leading to an exponential increase in the number of circuit components in each IC. In a 1965 paper,

Gordon Moore (one of the co-founders of Intel) noted that the number of components per IC had doubled every year since 1958, and confidently predicted that this trend would continue "for at least 10 years. [8]" Few could have predicted that the doubling predicted by Moore would continue all the way to the present day, a span of nearly 50 years.

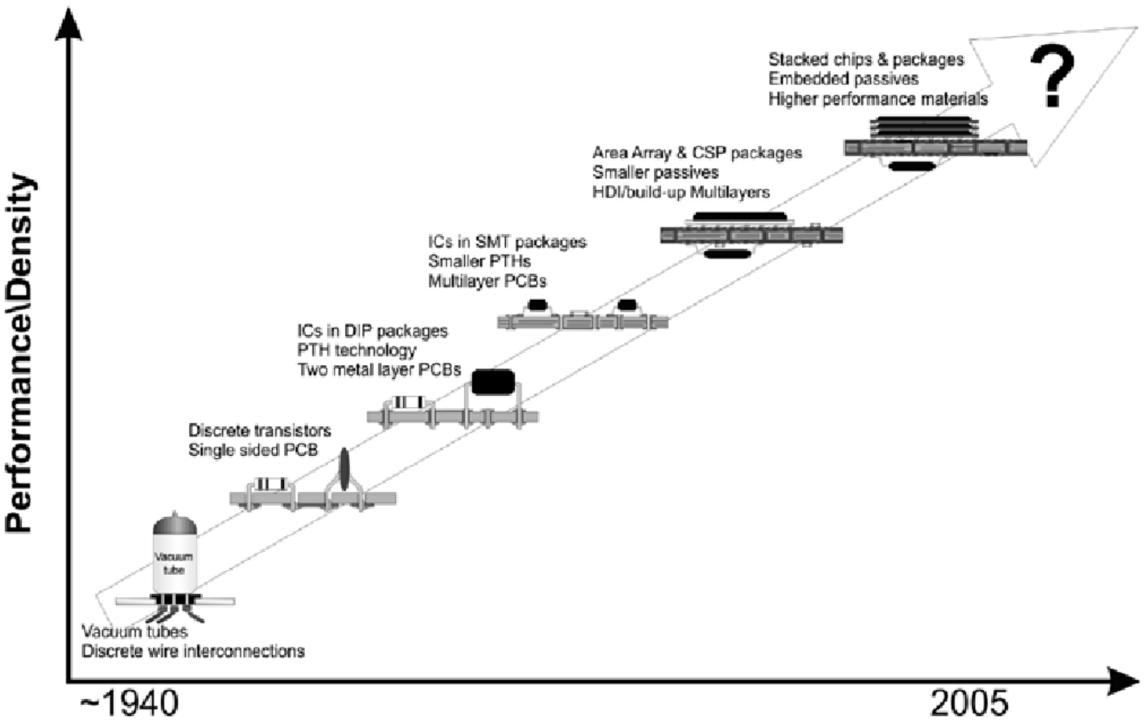
As the electronics industry blossomed, advances in IC technology had a dramatic effect on the corresponding electronic packaging technologies required. Smaller components allowed for increasing IC complexity. To connect these increasingly complex IC components, larger and larger numbers of input/output (I/O) channels are needed. At the same time, smaller components also allow identical circuits to be built into a continually shrinking silicon wafer (or "die"), a process known as die shrink. Component and die shrink also allow for improved circuit response time and lower power usage (in general), by lowing threshold voltages and reducing parasitics (unwanted resistive, capacitive, and inductive losses in metal interconnects). As a result, the overall dynamic is one of packaging technology forced to continually improve to keep pace with shrinking IC components (feature size reductions of approximately 15% per year) [9].

Traditional trends in the electronic packaging industry include: [6]

- Smaller and Lighter Packages
- Faster Circuit Responses
- Increased Circuit Density
- Higher Power Density
- Larger Semiconductor Dies
- More Inputs/Outputs (I/O's)
- Lower Cost per functional unit

- Higher Reliability

Figure 1.12, below, shows the trend of increasing packaging density over time.



Note: Complexity has increased significantly over the years but there are limits to what extrapolated technologies can offer in terms of cost and performance

Figure 1.13. Increases in Packaging Density over time [5].

As IC technologies continued to advance, the push to achieve higher I/O counts and lower package sizes continues. Consequently, electronic packaging technologies will need to continue to advance to keep pace with improvements in integrated circuits. In 2009, the International Technology Roadmap for Semiconductors (ITRS), determined that "[i]nnovation in assembly and packaging is accelerating in response to the realization that packaging is now the limiting factor in cost and performance for many types of devices" [10]. However, many of the currently available or next generation technologies, such as the Multi-Chip Module (MCM) and System-in-Package (SiP), are easily understood in the overall historical context of finding ways to improve the functional density of components. Moreover, the main processing breakthrough involved in cutting-

edge applications such as 2.5D and 3D packaging is the through-silicon via (TSV), which is fundamentally an IC technology.

Chapter 2
A Brief Introduction to Electronic Solders

2.1 Soldering

An assortment of techniques has been developed over the years for joining separate metal work pieces. These include Welding, Brazing, and Soldering. In soldering, the surfaces to be joined are heated in the presence of a distinct filler material, called the Solder. The solder melts and flows between the surfaces and, upon cooling, forms a metallurgical bond between them. A chemical agent known as a flux, which removes oxides and contamination to leave behind a readily solderable surface, is often used when soldering [3,11,12].

Soldering takes place at temperatures below 450ºC – otherwise, it would be considered Brazing – and, additionally, must be done at temperature low enough to avoid damaging other components of the system that is being soldered [3,13]. Solders are therefore generally alloys with a low melting temperature. Alloys are solid solutions of two or more metals (or mixtures of several phases that are solid solutions) that exhibit metallic bonding. Alloys are typically stronger than pure metals, and can have much lower melting points, making them extremely useful for solder applications [14,15].

In order for a robust joint to be formed during soldering, a metallurgical bond must be created between the solder material and the work pieces that are being soldered. To forge this bond, the solder must flow easily (low viscosity) and 'wet' rapidly (have low surface energy) with the surface finish. Additionally, an intermetallic compound layer must be formed at the solder-surface interface – this is what provides the

metallurgical bonding between the two materials [16]. Because most Intermetallics are brittle, however, the thickness of the IMC layer should be controlled. Such control is typically accomplished by limiting the time-above-liquidus of the solder during the soldering process [17].

2.2 Solder Joints for Electronic Assemblies

Solder joints are vital to the quality, performance, and reliability of Electronic Assemblies. Solder joints enable electrical power and signals to pass into and out of electronic components. Signals route through the joints and out through the copper traces of the substrate to other components and connectors. The loss of a single key signal pathway could dramatically alter the behavior of a circuit, or cause it to fail entirely. Therefore, quality and reliability are highly desirable. Electrical "parasitics" – unwanted resistive, capacitive, and inductive losses in metal interconnects – are also clearly undesirable in an electronic solder joint [3].

In cases where no underfill material is used, the solder joints also provide the only mechanical connection between the components and the substrate. They must take up mechanical stresses from CTE (coefficient of thermal expansion) mismatches, and be strong enough to deal with vibration and drop conditions. Additionally, they must maintain their strength over an extensive period of time, during which they must resist degradation due to environmental factors, electromigration, and diffusion-based microstructure evolution [3].

Finally, the solder joints provide the path for most of the thermal energy produced in an electronic package to be drawn into the substrate and dissipated. Many packages generate sufficient thermal energy to damage themselves, were they reliant on air-cooling

alone. The solder joints must provide a sufficient thermal connection, otherwise expensive add-ons such as heat sinks may be required. Simultaneously, many of the joint-weakening actors are enhanced at elevated temperature [3].

2.2.1 Overview of Surface Mount Manufacturing Process

In order for a solder material to be acceptable for electronics manufacturing, it must be compatible with the materials and manufacturing processes used. Figure 2.1, below, shows some of the primary stages of a typical surface mount technology assembly process.

Figure 2.1. Key steps in SMT Assembly [3].

The first principal step in Surface Mount Assembly is Paste Printing. Solder paste is printed onto the copper lands of the Printed Circuit Board, and is important both during the soldering process and before, as the tackiness (e.g. stickiness) of the paste is what holds most Surface Mount Components in place prior to reflow. The most common method of applying the solder paste to the PCB lands is via a screen or stencil printing process. The screen or stencil is aligned over each PCB and has apertures through which the solder paste is pushed onto the lands. Screens are typically constructed using a wire mesh with an emulsion matrix filling the gaps where solder should not pass. Stencils are

thin metal sheets in which the appropriate apertures have been ablated or etched. Stencils allow for tighter feature spacing and are therefore more common in modern production settings [3].

Following paste printing and (optional) automated optical inspection, components are aligned with their corresponding land pattern on the Printed Circuit Board and placed onto the board such that their leads or terminations rest on the solder paste. Registration of the appropriate land pattern for each component is facilitated by the use of visual markers on the board surface known as fiducials. Global fiducials help set the coordinate system for the board, and – for very fine pitch land patterns – an additional local fiducial may be added near the component's corresponding land pattern to help guarantee proper alignment. Component placement machines are differentiated by a large number of variables including placement speed and accuracy, the type of components and feeders that can be used, serviceable board sizes, mechanical action, optical alignment and inspection capabilities, and many others [3].

For a pure Surface Mount assembly, the only soldering process required is Reflow Soldering. Reflow soldering is most commonly carried out using a large convection oven with multiple, independently-controlled temperature zones. During solder reflow, the assembly passes through the reflow oven, experiencing a specific thermal profile (i.e. temperature versus time) designed to create quality solder joints at all necessary locations on the board while avoiding bridging and other common manufacturing defects. Reflow takes place when the solder alloy exceeds its Liquidus temperature briefly – typically 30-90 seconds – causing it to melt and (re)flow between the component leads or terminations and the copper lands of the Printed Circuit Board [3].

2.2.2 Solder Paste and Flux

Solder paste is a suspension of metal powder particles (of the solder material) in a fluid "vehicle," or carrier, that contains solvents, flux activators, rheological modifiers, and other additives. Figure 2.2 shows (conceptually) the solder paste system. Because of the high surface-area-to-volume ratio of small particles, surface oxidation of the metal powder particles can be a major problem. Oxide formation inhibits wetting and reduces the available volume of solder [3].

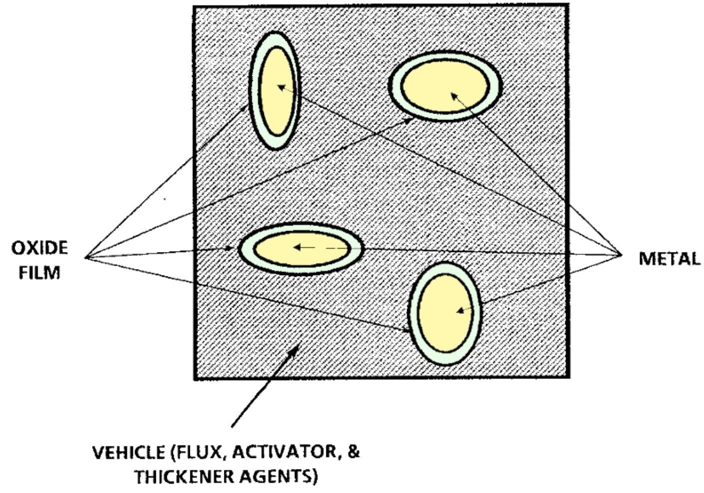


Figure 2.2. Solder Paste (modified from [3]).

Two primary strategies are employed to reduce surface oxide formation. First, the particles are produced under an inert gas atmosphere, thus keeping the oxygen available to form the oxide layers to a minimum. Second, the particle production process is optimized to produce particles that are as spherical as possible, minimizing the surface area for a given particle volume. Non-spherical particles are also undesirable because they can clog the screens and stencils used when the solder paste is printed onto the Printed Circuit Board [3].

The size of the metal particles in solder paste is also important. Similar to the effect mentioned above in conjunction with irregularly shaped particles, larger particles

will tend to clog screens and stencils. However, smaller particles are more susceptible to oxidation and other surface effects (as their surface-area-to-volume ratio continues to increase). Smaller particles are also more likely to allow small pockets of paste to separate from the main paste deposit. That can lead to the formation of what are known as 'solder balls' during reflow soldering. Solder balls endanger the electrical isolation of lands on the Printed Circuit Board surface because they can create a metal pathway between different pads. To provide a framework for companies working in the assembly industry, the particle sizes are classified into groups or 'Types' by Joint Industry Standards (J-STD-005). The usual rule-of-thumb is to use the largest particle size that works with the solder bumps in question, as this reduces problems with solder balls and also reduces overall cost [3].

The solder pastes used in surface mount electronic assemblies typically have a high metal content, about 90% metal by weight. However, because of the differences in density, this only amounts to a metal content of about 50% by volume. It follows that 50% of the solder paste volume is taken up by the flux vehicle, rather than the actual metal particles. The flux vehicle is a viscous fluid containing 'activators' – usually mild acids – that promote wetting of the solder material during reflow by removing oxides and other surface contaminants. Fluxes also contain solvents, which dissolve the flux and impart the pasty characteristic that allows it to be screen printed, and additives (e.g. rheological modifiers). Solvents, in particular, must be carefully selected, as they are a key element in the formation of voids (unfilled volumes) within solder joints. The flux vehicle must also coat the exposed metal surface (to prevent reoxidation) and provide a sump for the byproducts produced during flux activation [3].

There is also a Joint Industry Standard for fluxes. This standard, J-STD-004, classifies the fluxes into three categories – low, medium, or high – based on their level of activity (i.e. how acidic they are). The flux compositions are (generally): Rosin (RO), Resin (RE), Organic (OR), and Inorganic (IN) [3]. Fluxes that are water soluble commonly fall under the Organic designation, while 'No Clean' fluxes are often Resin based. No Clean fluxes allow (in theory) a post-reflowed assembly to be put into service without cleaning with no fear that left-over paste residue will cause electrical shorting, although it should be noted that surface residues still exist when using these fluxes and problems can arise due to them [9].

2.3 Solder Joint Properties

Selecting a solder material for use in a Printed Circuit Assembly involves understanding and balancing a wide array of properties. Some properties are universally desirable while others may be desirable for some applications but not others. For instance, high stiffness may be advantageous to an application involving highly demanding thermal cycling conditions, but disadvantageous in an application involving high-strain-rate (e.g. drop) conditions. The proper selection of an electronics solder must take into account the existing materials and processing of the components and substrates, solder strength as a function of temperature, cost of the solder, and other restrictions (such as health and environmental factors). Solder materials must provide good thermal and electrical conductivity, be easily manufacturable, and have adequate reliability for the intended application [2,3,18].

A variety of physical and mechanical properties are highly desirable in the solder joints of microelectronic assemblies. These properties affect the manufacturability, quality, strength and reliability of the joints. It can be tempting to treat these properties as single values to be looked up and plugged into equations. However, many of the most critical properties are properly treated as tensors. Properties may be either Isotropic (the same in all directions) or Anisotropic (different for different directions), and an understanding of the crystal structure of the material is helpful in predicting such behavior. (Neumann's Principle states that "[t]he symmetry elements of any physical property of a crystal must include the symmetry elements of the point group of the crystal" [19].) Additionally, an understanding of the microstructure of the solder joint is necessary to understand when a material can be treated as principally homogenous and when inhomogeneity needs to be taken into account.

Depending on the physical or mechanical property that one is interested in, it will be important to focus more on a material's composition (bonding, crystal structure) or processing (microstructure). For instance, Figure 2.3, below, shows a conceptual diagram of the bonding energy vs. bonding length for two bonded atoms. Because the energy well is asymmetrical, an increase in temperature will cause the equilibrium bond length to increase (as the higher one "fills up" the well, the further to the right the mid-point will shift). Similarly, because the slope of the two sides of the well is different, the elastic response (modulus) of the material will be higher in compression than in tension. Moreover, because these quantities relate directly to the bonding length, one knows that these quantities will be almost unaffected by changes in the microstructure of the material [20,21].

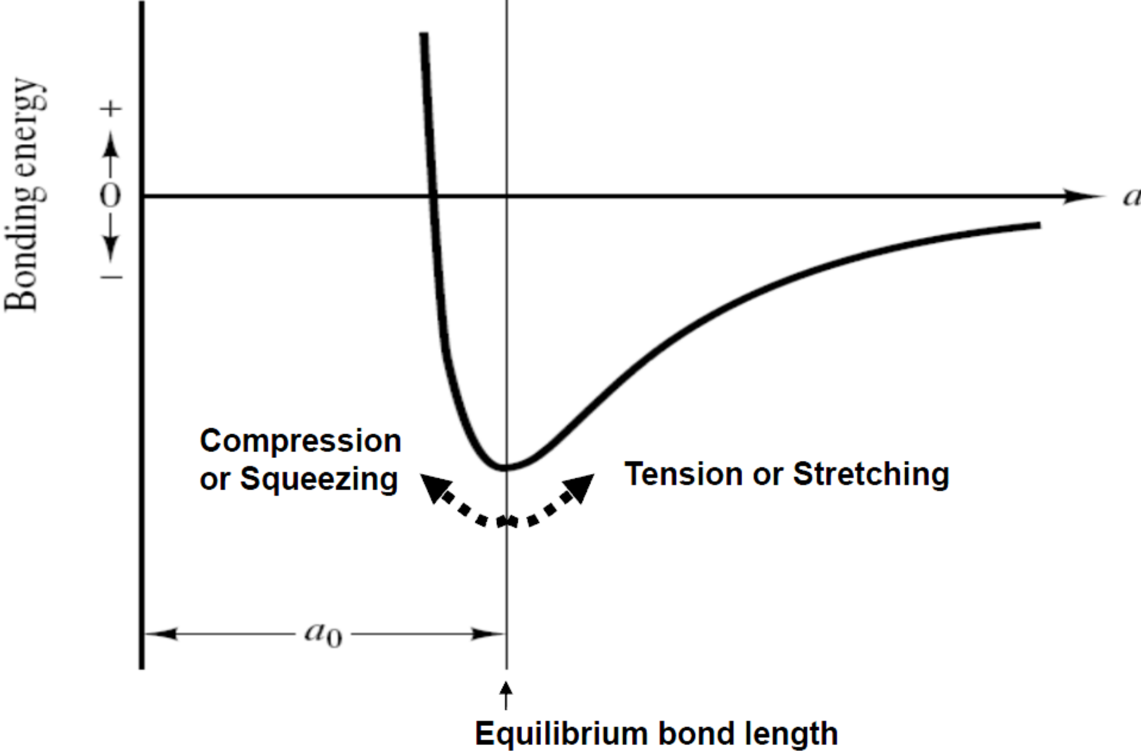


Figure 2.3. (Conceptual) Equilibrium Bond Length vs. Bonding Energy [20].

Since real materials don't typically behave in a purely elastic manner, it is common to compare their mechanical responses using a Stress-Strain curve. This involves applying a force to a sample of the material. When normalized to the initial area over which it is applied, this is the applied Engineering Stress – typically denoted as σ (tension) or τ (shear). The corresponding change in dimension of the sample is then recorded. When normalized to the original length, this is the resulting Engineering Strain – typically denoted as ε (tension) or γ (shear) [20]. Figure 2.4 shows the typical form of some Stress-Strain Curves for metal samples.

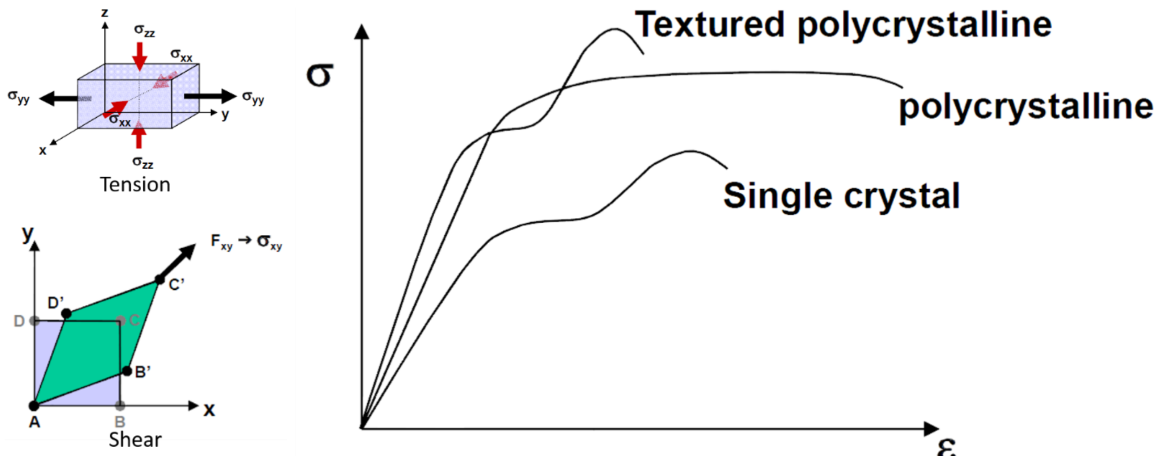


Figure 2.4. Tension and Shear (left) and typical Stress-Strain curves (right) [20].

Many of a material's important mechanical properties (i.e. Modulus, Yield Stress, Ultimate Tensile Stress, Fracture Stress, and Toughness) are encompassed by its Stress-Strain curve. Critically, this Stress-Strain curve depends very strongly on the material's microstructure. For instance, because

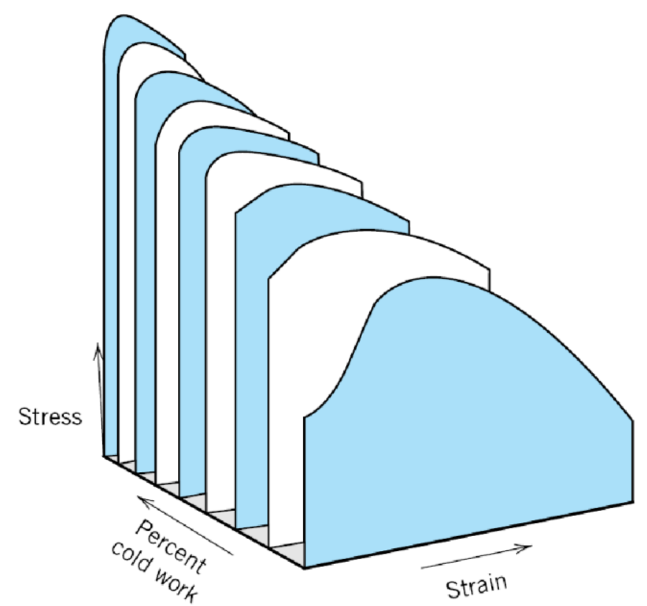


Figure 2.5. Strain Hardening [20].

polycrystalline materials contain many grain boundaries, they experience much faster strain hardening (cold working) than single crystal samples of the same material. Therefore, in many applications, it is necessary to understand and – via processing – control the microstructure of a material even through the composition may be fixed [20]. Figure 2.5 shows the effects of strain hardening on a typical polycrystalline metal Stress-Strain curve.

2.3.1 Properties Important to Manufacturability

Some of the properties of a solder material that are important for manufacturability include: [2,3,18,22]

- Cost
- Melting Temperature/Range
- Solderability (wetting, adhesion)
- Drossing
- Compatibility with the substrate metallization and component UBM
- Compatibility with common Flux Systems
- Compatibility with manufacturing processes of solder balls and powder
- External Visual Appearance (for inspection)
- Health and Environmental Concerns

The melting point (or range) of a solder material is particularly important from a manufacturability standpoint. Not only do energy expenditures in the soldering process scale with the temperature, but higher temperatures can result in printed circuit board warping, component or die cracking, and a variety of other manufacturing defects. At high enough temperatures, expensive engineering changes, such as switching to ceramic packages and substrates, becomes necessary. Therefore, lower temperatures of melting are ordinarily advantageous from a manufacturing perspective. Moreover, a single melting temperature (rather than a range) helps prevent components from moving during solidification of the solder, and is preferred for automated soldering operations.

2.3.2 Properties Important to Reliability

The melting temperature (or range) of a solder material is also important from a reliability perspective. However, in this context, a higher melting temperature is advantageous. The higher a material's melting temperature, the more resistant it will tend to be against thermally-driven failure mechanisms (e.g. Creep). Very low melting-temperature solders are therefore limited in their application potential.

Other Properties important for Reliability include: [2,3,18,22]

- Coefficient of Thermal Expansion (CTE)
- Voiding Percentage
- Grain Growth
- Intermetallic Formation
- Microstructure
- Mechanical Properties (Modulus, Tensile and Shear properties)
- Failure Modes (Crack initiation and growth, Creep, Fatigue)
- Performance under Thermal Cycling
- Resistance to Corrosion and Oxidation

2.4 A Brief History of Solder in Electronic Assemblies

Solder has been around for many thousands of years – likely around 7,000 – with written records of their use dating back to at least 3,500 BCE. Early solders were based primarily on Gold and used in the creation of metal artwork. The Romans later developed soft Tin-Lead (SnPb) solders, including Sn-37Pb Eutectic solder, for much more

utilitarian purposes such as plumbing. (In fact, the Romans based their work on existing knowledge from the 'barbarian' Celts and Gauls.) [3,12,14]

2.4.1 Tin-Lead Solder: An Industry Dominating Solution

Historically, the solder materials of choice for electronic assemblies have been Tin-Lead (SnPb) solders. Tin-lead solders have been used by humans for various purposes for thousands of years and were the mainstay of the modern electronic packaging industry from its advent until very recently. Incredibly, a fine-pitch micro-electronic package assembled in the U.S. in the late 1990s (or even today, for some applications) had the same general composition and properties as that used by the ancient Romans to seal their sewer pipes [3,12,14]. Tin-Lead solders have a variety of advantages in electronic applications [22,23]:

- Lead (Pb) is inexpensive and plentiful. Tin-Lead (Sn-Pb) alloys have relatively low melting temperatures suitable for the soldering of electronic assemblies.
- Sn-Pb alloys have low surface tension (which is advantageous to the solder wetting process), with Lead (Pb) acting to reduce the surface tension of pure Tin (Sn).
- Sn-Pb alloys form strong intermetallic bonds with the copper pads used in electronics, with Lead (Pb) acting as a solvent metal during IMC formation.
- Sn-Pb alloys have good mechanical properties, with Lead (Pb) acting to improve the ductility of pure Tin (Sn).

The most popular tin-lead solder for electronics manufacturing is the mixture of 63% Tin and 37% Lead by weight [2,3,12]. This alloy was particularly dominant in surface mount assembly, while 60Sn-40Pb was a popular choice for through-hole mount

wave soldering operations [3]. The 63Sn-37Pb has a combination of properties that allowed it to dominate the electronics manufacturing industry from its inception until quite recently.

The key feature separating Sn-37Pb solder from other Tin-Lead solders is that it is a 'eutectic' alloy. Eutectic alloys have a single temperature at which the entire alloy melts (when increasing temperature) and solidifies (when decreasing temperature). This makes them very easy and predictable to work with. Eutectic alloys behave very differently from most alloy compositions, which typically have a 'pasty range.' The pasty range is a range of temperatures within which the alloy is partially solid and partially liquid, but the solid and liquid components have different compositions. Solders with a pasty range can be 'worked' during cooling through the two-phase region. A pasty range is advantageous for certain applications such as plumbing, but undesirable in electronics, where the preferred result is for the joint to "freeze out" without last-minute shifting.

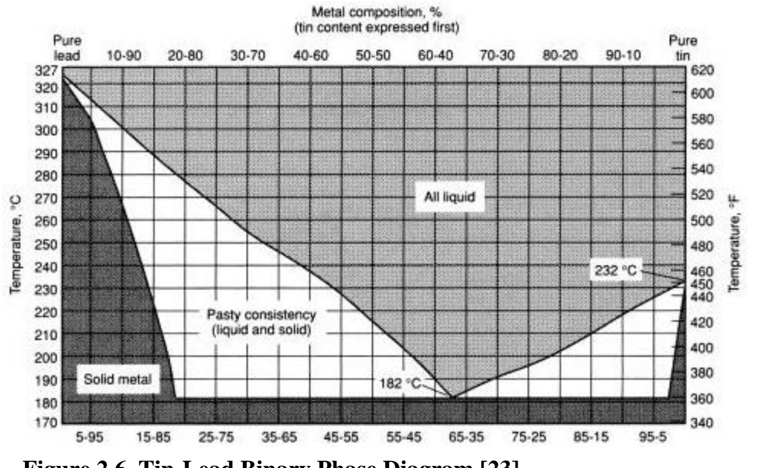


Figure 2.6. Tin-Lead Binary Phase Diagram [23].

Eutectic alloys will have more homogeneous compositions, and provide the lowest possible melting temperature for a given alloy system. For instance, the phase diagram on the right shows the binary alloy system formed by Tin and Lead [23]. The 63% Tin, 37% Lead composition has the lowest melting point, at about 183°C. This melting temperature is quite advantageous. Too low, and the joint would be in danger of

melting during operation; too high, and the processing temperatures necessary to create the joints in an electronic assembly become damaging to other parts of the assembly. 183°C is high enough without posing too high a risk of damage to the typical glass-epoxy substrates or plastic die-packages.

For electronic assemblies, eutectic 63Sn-37Pb solder has a wide range of advantages, including: [2,3,12,18]

- Eutectic Composition (i.e. single transition temperature)
- Low melting point (183°C)
- Low Cost (made from relatively abundant/cheap elements)
- Good Wetting and Manufacturability
- Adequate Fatigue Resistant
- Good joint integrity
- Excellent electrical conductivity

With the exception of bonding directly to gold- or silver-rich metals, eutectic SnPb solder performs admirably in the typical electronics assembly production environment. It 'wets' well, forms good bonds with contact pads on both the package and substrate, and is generally easy to work with from a manufacturability perspective. Mild, naturally-derived fluxes are sufficient for working with SnPb solder [23].

Tin-Lead eutectic solder also provides the mechanical, electrical, and thermal performance needed in most electronic packaging applications. The joints are durable: while more 'modern' lead-free solders often have superior 'out the gate' performance, eutectic SnPb undergoes a more limited microstructure evolution, with corresponding reductions in the loss of reliability and mechanical strength in the joint over time [24].

2.4.2 Tin-Lead Solders: The Decline

Unfortunately for the electronics industry, despite its many advantages, eutectic SnPb solder has a fatal flaw. One of its two constituent elements, Lead (Pb), presents a significant toxicity concern. Harm from lead toxicity is most often caused by long-term, cumulative exposure and is a particular threat to children. (One can get "lead poisoning" from acute exposure, but this is less common.) Symptoms of high lead exposure can include: [25]

- Anemia
- Decreased renal function
- Increased blood pressure and cardiovascular disease
- Anti-social behavior
- Learning disabilities
- Mental retardation

Given the nature of these threats, it's no wonder that governments in most developed nations have placed severe controls on the use of lead in a variety of products. In the United States, for instance, the use of lead in automotive gasoline and most paints were outlawed in 1976 and 1978, respectively. In the late 1990s and early 2000s, countries such as Japan and the European Union (EU) became concerned about the use of lead in electronics-industry solders.

Electronic devices have been advancing steadily, and, therefore, one generation of electronics tends to be replaced very quickly by a new generation of products. Simultaneously, the recycling costs for most electronic products have continued to be

very high. As a result, a large amount of electronic waste ends up in landfills. A study by Turbini found that in 1998, less than 2% of computer products were recycled [26].

The idea was that because electronics are commonly disposed of in landfills following their useful life, over time, lead from the tin-lead solder might leach out into the soil and become an environmental and health hazard. By the mid-2000s, both Japan and the EU had begun to enforce restrictions on the use of lead in electronics (either via governmental action or industry self-mandate), dragging much of the worldwide packaging and assembly industry along with them. In Japan, the advisory committee of Japan Institute of Electronics Industry Development Association (JEIDA) created a roadmap in 1998 for the commercialization of lead-free solders. Although no direct governmental action has been taken in Japan, the Japanese electronics industry has been ahead of the curve in the implementation of lead-free products. In the European Union, direct action was taken by the government. In 2000, the EU adopted two directives that were (in part) designed to phase out the use of lead in electronics. The Waste of Electrical and Electronic Equipment (WEEE) directive stipulated that lead was to be removed from all electrical and electronic components at their end-of-life. The Directive of the Restriction of the Use of Certain Hazardous Substances (RoHS) prohibits the use of lead in electrical and electronic components manufactured after July 1, 2006 [27]. In the Unites States, no direct governmental action has been taken, but market forces have pushed the US electronics industry toward the adoption of lead-free practices. In 2000, the IPC developed a roadmap for lead-free research and development in the United States [26].

2.4.3 Tin-Lead Solder: Searching for a Replacement

With eutectic SnPb being phased out as the solder of choice for electronic assemblies, a successor or successors were needed. This is where lead-free solders come into the picture. So as to quickly meet the requirement for lead removal while minimizing the impact on other areas of the assembly process, scientists and engineers sought out a 'drop-in' replacement: something they could substitute for the SnPb solder and essentially have no one the wiser. For this strategy to work, the replacements need to have properties similar to or better than the eutectic SnPb [2,3,26–28].

Some of the properties to consider for Lead-Free solders include: [2]

- Liquidus and Solidus temperatures similar to 63Sn-37Sb
- Small temperature differences between Liquidus and Solidus in the Equilibrium Phase Diagram region of interest
- Material Properties that are similar to or better than SnPb (e.g. electrical and thermal conductivity, CTE, strength, ductility, etc.)
- Compatibility with production processes for solder spheres, powder for solder paste, and solder wire
- Wetting and viscosity close to SnPb
- Low oxidation and dross formation
- Compatibility with existing flux system chemistries
- Non-Toxic

A variety of research efforts took place over the 1990s and early 2000s to determine the optimal lead-free solder composition for various consumer electronics applications. Large organizational efforts include: [28]

Table 2.1. Large Organizational efforts to find Pb-Free solutions [28].

Country/Region:	Group/Organization:
USA	National Center for Manufacturing Sciences (NCMS)
	National Electronics Manufacturing Initiative (NEMI)
Japan	Japan Institute for Electronics Packaging (JIEP) Working Group
	Japan Electronic Industry Development Association (JEIDA)
Europe	[U.K.] Department of Trade and Industry (DTI)
	[E.U.] IDEALS Consortium

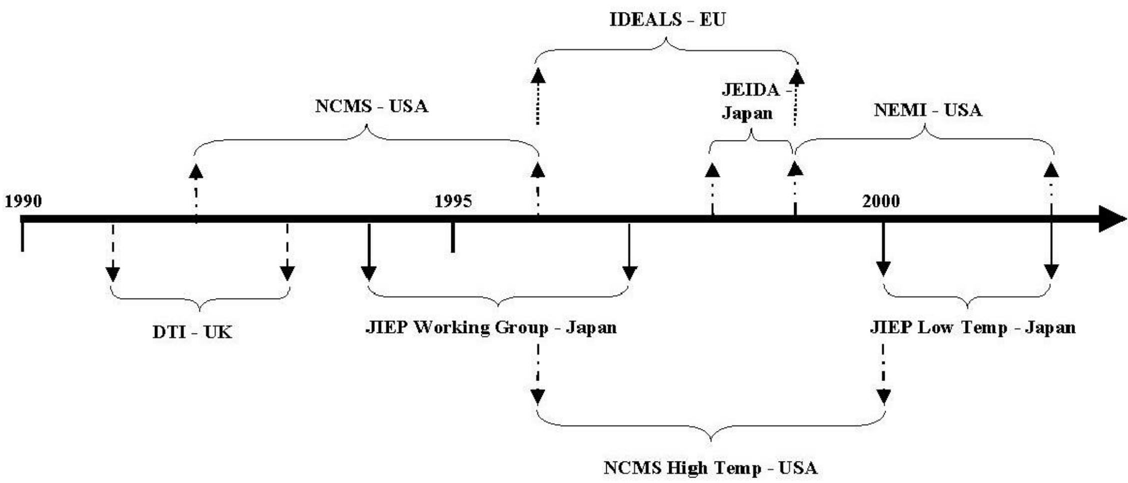


Figure 2.7. Rough Time-Line of Major Lead-Free Solder Consortia [28].

2.4.4 Electronic Solders: Near-Eutectic Sn-Ag-Cu (SAC) Solders

Eventually, most research into lead-free alternative to Sn-37Pb converged on a series of Tin-rich solder materials: the near-eutectic Tin-Silver-Copper solder alloys. These Sn-Ag-Cu solder materials, or simply “SAC” solders, roughly meet the qualifications needed for a SnPb replacement. Their melting temperatures lie between that of pure tin (232°C) and SnPb eutectic (183°C). They also provide adequate

wettability, generally good mechanical properties (often in excess of SnPb, at least as initially reflowed), good interfacial properties, and relatively low grain coarsening rates [2,3,29].

The most widely accepted Sn-Ag-Cu solders have compositions in the near-eutectic region, typically with 3–4 % Silver (Ag) and 0.5–1 % Copper (Cu). Although most common SAC solders have compositions very close to the Sn-Ag binary eutectic composition, the addition of small amounts of copper was found to lower the solder melting temperature and improve the wetting properties. Copper is also cheaper than Silver, which lowers costs [29].

Here are a few examples of SAC-family solders: [2,3] (Note that some non-SAC are included for completeness.)

- Tin-Copper Eutectic (Sn99.3Cu0.7) – Eutectic mixture of Tin and Copper. Melting temperature still quite high at 227ºC. Inexpensive, but poor mechanical properties, poor quality when air reflowed, and prone to Tin Whiskers.
- Tin-Silver Eutectic (Sn96.5Ag3.5) – Eutectic mixture of Tin and Silver. Somewhat high melting temperature of 221ºC, despite it eutectic nature. It was found that the addition of small amounts of copper could lower the melting temperature, while simultaneously reducing the amount of (expensive) silver used.
- SAC305 (Sn96.5Ag3.0Cu0.5) – Very popular SAC solder for use in the U.S. electronics industry. Pasty range around 217ºC to 225ºC. Good mechanical characteristics. Based on recommendation from JEIDA.
- SAC105 (Sn98.5Ag1.0Cu0.5) – Popular in certain sectors of the electronics industry, most commonly for use in cell-phone manufacturing. (Favored for this use

because of superior drop/shock resistance.) Also has a lower cost premium, due to reduced silver content.

- SAC387 (Sn95.5Ag3.8Cu0.7) – Original recommendation of the European IDEALS Consortium. Not commonly used in the United States.
- SAC396 (Sn95.5Ag3.9Cu0.6) – Based on research by U.S. NEMI group. Used occasionally in the United States.

2.5 Eutectic SnPb Solder: A Closer Look

The Sn-Pb system involves two (2) elements: Tin (Sn) and Lead (Pb). White Tin (β-Sn) is a lustrous silvery metal with a body-centered tetragonal crystal structure and anisotropic material properties and Lead (α-Pb) is a greyish metal with a face-centered cubic crystal structure and isotropic material properties. The Binary Phase Diagram is shown below (Figure 2.5).

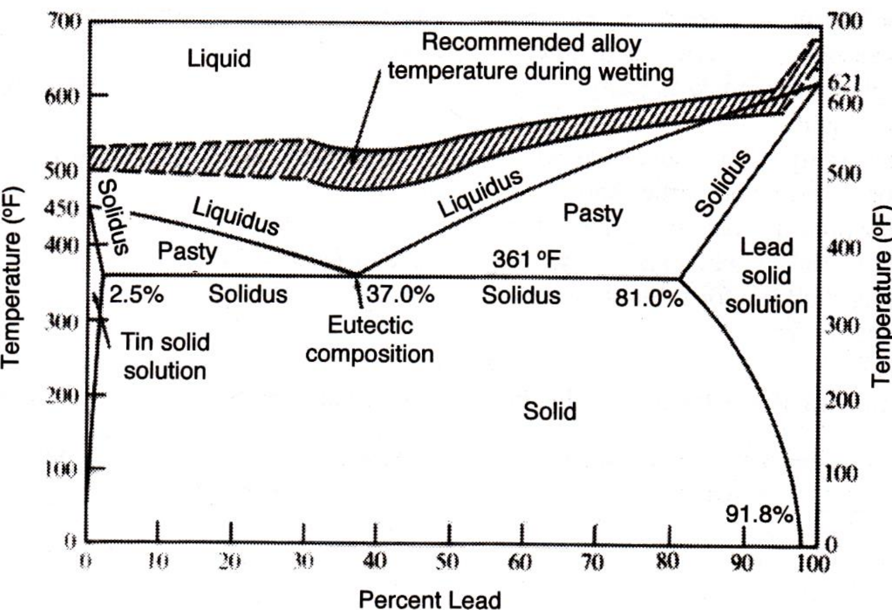


Figure 2.8. Tin-Lead Binary Eutectic Phase Diagram [2].

Eutectic 63Sn-37Pb exhibits the standard, or "normal," binary eutectic microstructure. The normal eutectics solidify either as thin alternating layers ("lamellae") or as rods of the minor phase imbedded within the major phase [30]. Eutectic SnPb solder in electronics applications will solidify into the lamellar microstructure [17]. The solidification process takes place "cooperatively behind an essentially planar solidification front" [30]. As the solid phases grow, the Tin-rich phase rejects Lead into the remaining liquid phase, where it travels to a nearby Lead-rich phase and is absorbed. Similarly, Tin is rejected from the Lead-rich phases and travels to nearby Tin-rich phases. The inter-lamellar spacing (i.e. how thick the lamellae are) is determined by an energy balance involving volumetric and surface energy terms, with the primary control parameter being the amount of undercooling (more undercooling leads to thinner lamellae) [30].

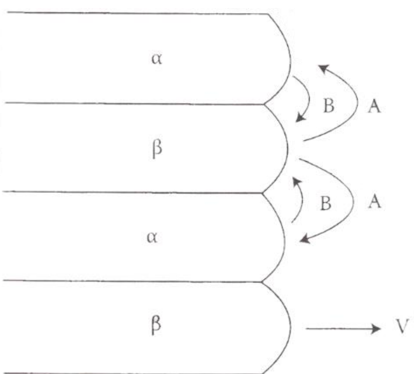


Figure 2.9. Interdiffusion in Lamellar Solidification [30].

Lead (Pb) does not form Intermetallic compounds with either Tin (Sn), the other component of SnPb solder joints, or with the principal interconnect/pad material Copper (Cu). Tin, however, forms two primary IMCs with Copper: Cu_6Sn_5 and Cu_3Sn. The IMCs create a metallurgical bonding between the Cu pads and the bulk solder. However, almost

all known Intermetallic Compounds are brittle, and therefore, IMC layers that are too thick negatively affect joint reliability [29].

2.5.1 Eutectic SnPb Solder: Material Properties

Although the material properties of Tin are anisotropic, the presence of soft (malleable) Lead-rich lamellae separating the Tin-rich lamellae, in conjunction with grains that are small in comparison to most solder joints, allows for relatively homogeneous properties and responses [17]. A table of select properties for eutectic Tin-Lead solder is shown in Figure 2.7, below [2].

Table 2.2. Select properties of 63Sn-37Pb [2].

Property	Value (unit)	Property	Value (unit)
Mechanical		**Electrical**	
Density	7.4 (g/cm^3)	Electrical Conductivity % IACS	11.9
Tensile Strength	30.6 (MPa)	Electrical Resistivity	14.5 (μΩ-cm)
Yield Strength	(27.2 MPa)	**Thermal**	
Total Elongation	48%	Thermal Coeff. Expansion	24-25 × 10^{-6} /°K
Elastic Modulus	34-40 (GPa)	Thermal Conductivity	50.9 [W/(m-°K)]
Poisson's Ratio	0.4	Melting Temperature	183 °C
Shear Strength	27.4 (MPa)	Wetting Angle	14 – 16°
Fatigue Strength* at 20 °C at 100 °C	 16.2 (MPa) 10.2 (MPa)		
Creep Strength at 20 °C at 100 °C	 3.3 (MPa) 1.0 (MPa)		
Hardening Exponent	0.033		

* This composition was 60% Sn and 40% Pb.

2.5.2 Eutectic SnPb Solder: Microstructural Evolution

The solder joints used in electronic assemblies are small enough that the length scales of microstructural features are relatively large in comparison to many other

engineering applications. As a result, seemingly small changes in the microstructure of solder joints may have a large impact on the overall performance of the joint. Evolution (here meaning simply “change over time”) of the solder joint microstructures “is known to have a strong influence on damage initiation and propagation” (and therefore on joint reliability) [31].

During thermal cycling (to be discussed in Chapter 3) or isothermal aging, the microstructure of solder joints will change over time. (Thermal cycling leads to faster evolution than isothermal aging [31].) The primary mechanism of such changes is generally diffusion (thermally activated movement of ions within the material) down a chemical potential gradient (“downhill diffusion”). More than one mass transport mechanism may be involved, such as dislocation pipe diffusion, grain boundary diffusion, bulk diffusion, short-range / interface-controlled diffusion [17]. However, other sources of evolution can also exist within a solder joint, including such things as relaxation (conversion of elastic to plastic strain) and electromigration. There are two main effects of evolution seen within the microstructure of SnPb solder joints. The first is grain coarsening and the second is IMC thickening.

As typical for two-phase solids, grain coarsening within eutectic SnPb solder is driven by a reduction in the interfacial energy, either at Pb-Pb or Sn-Sn grain boundaries or at Sn-Pb domain interfaces [17]. Grain Coarsening is observed within appropriately prepared solder joint cross-sections as an increase in the average size of the beta-Sn and alpha-Pb lamellae over time, as shown in Figure 2.8 below. ‘Over time’ can equate either to time held continuously at high temperature (isothermal aging) or over the course of periodic thermal cycles that involve a high temperature dwell.

In eutectic SnPb solder, external loading (as in during thermo-mechanical cycling) was known to have a strong influence on grain coarsening and phase separation. Elastic energy stored in the solder during loading causes a shift of the binodal points (of the free energy) and decreases the interface width. This was shown to lead to an increase in the decomposition rate and grain coarsening [31]. During thermo-mechanical cycling, the grain coarsening process will not be homogeneous. Instead, regions of high shear strain will be coarsened more. These regions are also known to be preferred crack nucleation sites [31].

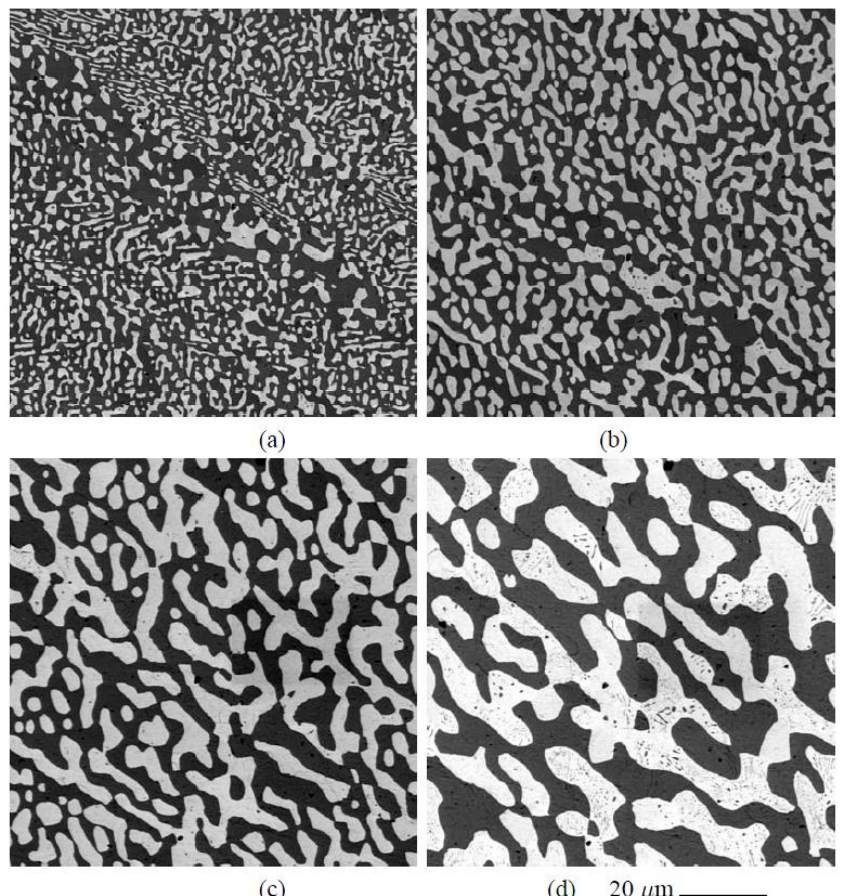


Figure 2.10. Microstructural Evolution in Eutectic SnPb Solder [17].

Intermetallic Compound (IMC) thickening also occurs due to diffusion within the solder joint. The IMCs that are energetically favorable will experience a net influx of ions

over time and increase in volume correspondingly. Since the Intermetallic layers in question form initially as thin layers along the wettable surfaces of the joint, this leads observationally to IMC layer “thickening” over time.

2.6 Near-Eutectic Sn-Ag-Cu (SAC) Solder: A Closer Look

The Sn-Ag-Cu system involves three (3) constituent elements: Tin (Sn), Silver (Ag), and Copper (Cu). Both Silver and Copper have face centered cubic crystal structures, high thermal and electrical conductivity, and metallic lusters corresponding to their names. The Equilibrium Ternary Phase Diagram of the Sn-Ag-Cu system is shown in Figure 2.9, at left. The Sn-Ag-Cu phase diagram exhibits a ternary eutectic point in the Tin-rich region, at a composition of approximately 95.6Sn-3.5Ag-0.9Cu (SAC359), which has a melting temperature of about 217.2ºC. It is this Tin-rich corner of the ternary phase diagram (shown on right in Figure 2.9) that has sufficiently low melting temperatures such that the near-eutectic compositions were considered viable lead-free solder candidates [32].

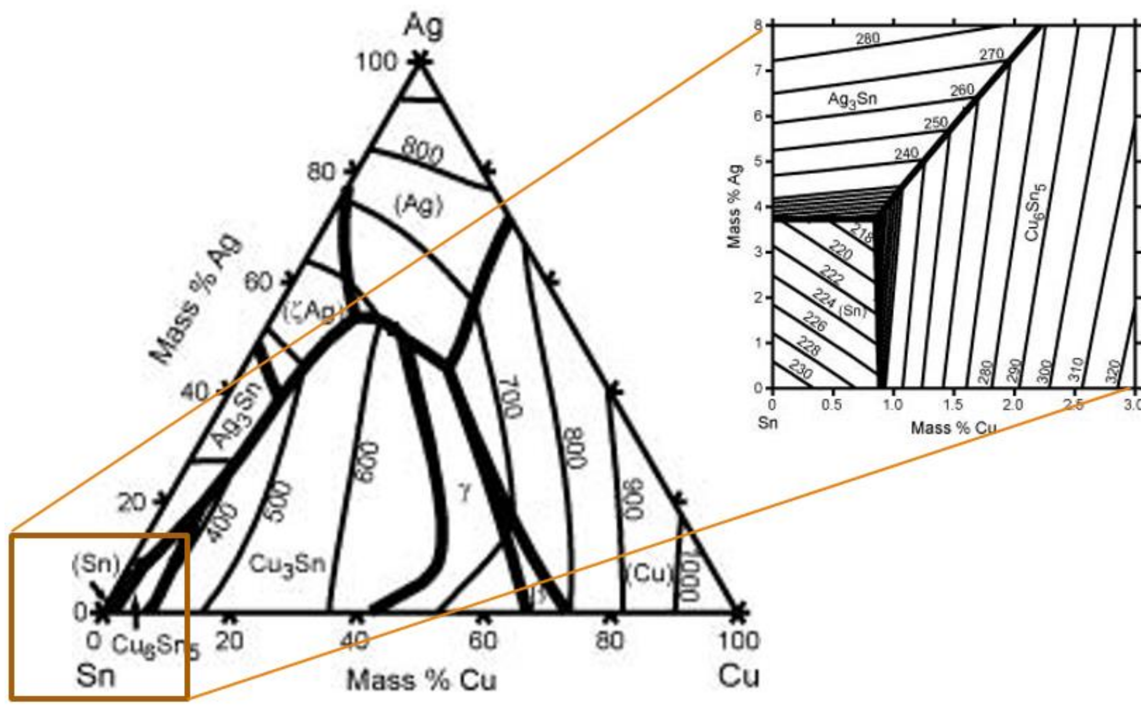


Figure 2.11. From NIST: Sn-Ag-Cu Phase Diagrams.

Also, unlike Sn-37Pb, which has the lamellar structure characteristic of eutectic alloys, SAC alloys are typified by one or few grains of β-Tin with Intermetallic particulates at the grain or dendritic boundaries. There are three phases in the near-eutectic region of the Sn-Ag-Cu phase diagram, all of which are typically seen upon solidification. These are β-Sn, Ag_3Sn and Cu_6Sn_5.

Another IMC, Cu_3Sn, exists, but does not form except at higher Copper contents, and, therefore, is not seen within the bulk of the solder. No Intermetallics exist between Silver (Ag) and Copper (Cu) [32].

Table 2.3. Phases in Sn-Ag-Cu Solder [from NIST]

Phase	Structure	Morphology
β-Sn	Body-Centered Tetragonal ($I4_1/amd$)	Interconnected Dendritic Structure
Ag_3Sn	Pmmn	Small Needles or Platelets
Cu_6Sn_5	$P6_3/mmc$	Small Needles (in bulk) / Scalloped (at pad)
Cu_3Sn	Cmcm	Planar (at pad)

The initial microstructure of Tin-rich solder joints, including the SAC solders, is highly sensitive to the solidification process from the liquid state. Although all three phases are seen in solidified Sn-Ag-Cu samples, the ternary eutectic phase is not usually observed. This absence is due to the significant undercooling typically required to nucleate the β-Sn (10–50°C), which suppresses the eutectic structure even in compositions quite close to the eutectic. On the other hand, the Intermetallic Compound (IMC) precipitates take only minimal undercooling, and, therefore, they will begin to nucleate before the β-Sn [29,32–35].

As a consequence, if the amount of undercooling is small, the Intermetallic Compound precipitates can grow to be quite large before the full joint solidifies. These IMC precipitates are known as “primary” precipitates, whereas smaller IMC particles between the β-Sn dendrites are known as “secondary” precipitates. The primary precipitates take the form of large Ag_3Sn platelets and Cu_6Sn_5 rods. As the primary precipitates nucleate and grow, they pull Silver and Copper out of the remaining liquid phase, reducing the Ag and Cu content far below equilibrium values [29,32].

Once β-Sn nucleation initiates, the freezing process proceeds very quickly, typically taking less than one (1) second for a SAC solder joint. This is due to the large amount of constitutional (compositional) undercooling in the interfacial region and the inherently rapid growth kinetic of Tin [24,27]. During solidification, the β-Sn adopts a dendritic (pine tree like) morphology, with plentiful branching. As the dendrites grow, Silver and Copper are rejected into the remaining liquid. This creates the constitutional undercooling, but also creates small Ag and Cu rich regions that undergo solidification "as monovariant or invariant eutectic microconstituents, depending on local composition" [29] – creating the secondary precipitates [29,33,35].

The Intermetallic Compounds (Ag_3Sn and Cu_6Sn_5) have higher strength and higher modulus than the β-Sn. Therefore, a higher concentration of Cu_6Sn_5 rods and (particularly) Ag_3Sn platelets increases the effective modulus (stiffness) of a Sn-Ag-Cu solder joint. Overly large Ag_3Sn plates should be avoided, however, as they act as crack initiation sites under tensile and shear stresses. For a typical SAC solder (3–4 % Ag and 0.5–1 % Cu), Ag_3Sn plates outnumber Cu_6Sn_5 rods. Since, the IMC Ag_3Sn is the only phase containing Silver (Ag) in a SAC solder, an increase in Ag content results in a corresponding increase of Ag_3Sn IMC precipitates [29,33,35].

The morphology of Sn-Ag-Cu solder joints also depends on the joint size. This dependence is due to Intermetallic Compound formation at the component- and PCB-side pads (which draws Sn from the solder) and because the size of the joint affects the amount of undercooling that can be applied (particularly using standard surface mount assembly processes) [34].

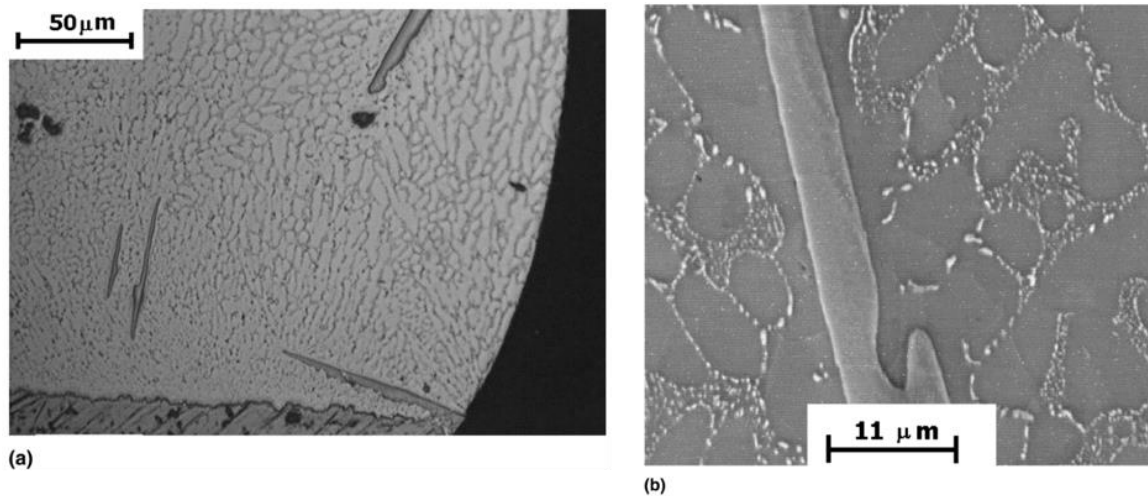


Figure 2.12. (a) Optical and (b) BSE images of typical SAC Joint Microstructure [32].

As with SnPb solder, the interfacial IMCs found in conjunction with Copper pads are Cu_6Sn_5 and Cu_3Sn. Typically, the Cu_6Sn_5 is observed immediately post-reflow, whereas the Copper-rich Cu_3Sn IMC may only be observed after thermal cycling or isothermal aging. On a Nickel (Ni) clad pad (e.g. ENIG surface finish), the Intermetallics formed will depend on the Copper (Cu) content of the bulk solder. Ni-Sn IMCs can form, but in the presence of sufficient Cu, (Ni,Cu)-Sn type IMCs will grow. The primary Intermetallic formed is $(Ni,Cu)_3Sn_4$, with as-reflowed layers of $(Cu,Ni)_6Sn_5$ being reported in cases where the Copper content of the solder exceeds 0.5% by weight [34,36].

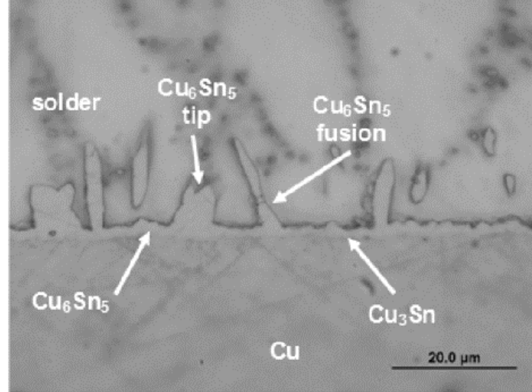


Figure 2.13. Cu pad IMCs with HASL after 500 hours of aging [37].

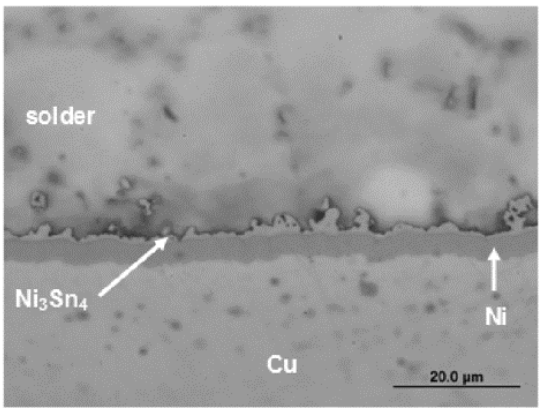


Figure 2.142. Cu pad IMCs with Ni/Ag after 1000 hours of aging [37].

2.6.1 Near-Eutectic Sn-Ag-Cu (SAC) Solder: Material Properties

Various Sn-Ag-Cu solders have their own unique material properties. Most formulations should be relatively similar to Sn-3.5Ag, shown in Table 2.4, below.

Table 2.4. Properties of some component materials [3].

Properties	Copper	Silver	Gold	Tin	96.5Sn3.5Ag
Melting point (°C)	1083	961	1063	231	221
Density (g/cc)	8.94	10.5	19.3	7.29	7.4
Thermal conductivity (W/cm K)	3.862	4.075	3.151	0.665	0.78
Electrical conductivity (/Ω cm)	5.88×10^5	6.25×10^5	4.17×10^5	0.87×10^5	0.812×10^5
Thermal expansion coefficient (/°C)	16.42×10^{-6}	18.6×10^{-6}	14.2×10^{-6}	22.2×10^{-6}	30.2×10^{-6}
Yield strength (psi)	10,000	1000	250	1300	3600
Ultimate tensile strength (psi)	32,000	21,000	17,000	2000	5000–7000
Young's modulus (psi)	1.92×10^7	1.18×10^7	1.12×10^7	6.89×10^6	7.8×10^6
Elongation at break (%)	51	50	50	50–80	37
Hardness (Brinell)	37	25	18.5	3.7	14.8

Dislocation interactions with secondary precipitates is the dominant strengthening mechanism in Sn-Ag-Cu solders (i.e. "precipitate hardening"). The IMC precipitates act as pinning sites and hinder dislocation motion, making the solder harder to deform [29]. Because precipitate hardening is the dominant strengthening mechanism, the SAC solders are intrinsically sensitive to process parameters and aging conditions.

Because Sn-Ag-Cu solder joints tend to form with only a few Tin grains (and β-Sn is anisotropic [38]), rather than numerous small grains as with eutectic SnPb solder, the mechanical properties of the joint will depend strongly on the exact number and orientation of the β-Sn grains present. The size of the β-Sn grains is known to be quite sensitive to the Silver (Ag) and Copper (Cu) content of the joint [34].

Due to the anisotropic nature of the coefficient of thermal expansion and other material properties in Tin, stress will be induced at Tin grain boundaries during thermal cycling. (CTE mismatch and the DNP formula are covered in Chapter 3.) Unlike SnPb solders, Sn-Ag-Cu (SAC) solders do not have either a lamellar microstructure or the

relative malleability of Lead-rich phases to act as a strain buffer [17]. Therefore, both macro and local level CTE mis-matches must be considered.

2.6.2 Near-Eutectic Sn-Ag-Cu (SAC) Solder: Microstructural Evolution

As with eutectic SnPb solder, some grain coarsening occurs in the near-eutectic Sn-Ag-Cu solders during isothermal aging or thermal cycling. Chen et al. found that the β-Sn grains in SAC solder joints gradually coalesce during thermal cycling. At the same time, low-angle boundaries were found to emerge as a precursor to dynamic recrystallization (discussed in Chapter 3) [39].

However, a more important microstructural evolution mechanism in the Sn-Ag-Cu solders is grain coarsening of the Intermetallic precipitates, rather than the β-Sn domains. Zhang et al. [40] performed isothermal aging on Sn–3.5Ag–1.0Cu interconnects and found a rapid coarsening of the Ag_3Sn secondary precipitates, leading to a reduction in the resistance to shear of the solder material. Lu et al. [41] found that the larger Ag_3Sn plates are also affected by isothermal aging, undergoing "edge spheroidization and cylinderation" [29], but found that this did not lead to a degradation in joint mechanical properties. A variety of other studies have shown that coarsening of the secondary precipitates is a significant driver in the reduction of strength in SAC solder joints during aging [42–46].

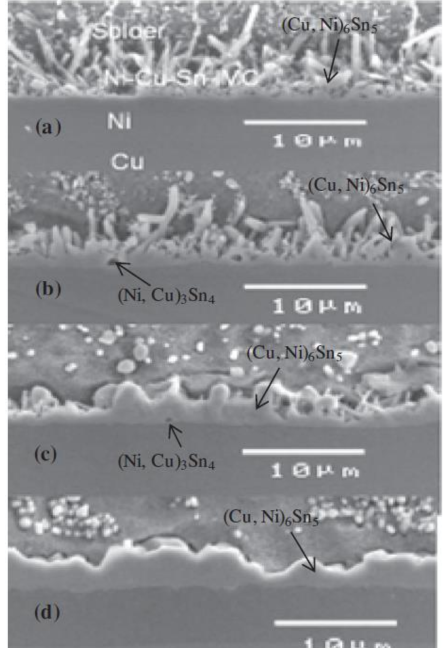


Figure 2.15. IMC Evolution at Ni Pad [36].

At Copper (Cu) pads, the $Cu6Sn5$ and $Cu3Sn$ Intermetallic layers undergo similar thickening as with the SnPb joints. At the Nickel (Ni) pads, if the $(Ni,Cu)_6Sn_5$ needles formed during solder reflow, these will thicken into a relatively flat, planar layer over the course of aging. The $(Ni,Cu)_6Sn_5$ layer will then undergo IMC thickening as a function of time. The $(Ni,Cu)_3Sn_4$ intermetallic forms between any observed $(Cu,Ni)_6Sn_5$ IMC and Ni Pad. This $(Ni,Cu)_3Sn_4$layer is thinner than the $(Cu,Ni)_6Sn_5$ layer and any thickening is not as apparent [36].

2.7 Other Elements commonly found in Tin-Rich Solders

Most of the alloys that have been considered as Lead-Free Solders involve Tin (Sn) as a major component. Tin, atomic number 50, is a silvery-white metal that is malleable and ductile. Pure Tin has a melting temperature of about 232℃. Two allotropes exist, each stable at different temperatures. Beta-Tin (β-Sn) has a body-centered tetragonal crystal structure and is thermodynamically preferred at temperatures above 13.2ºC [47]. Its lattice parameters are: a = b = 0.5632 nm and c = 0.3182 nm at 25◦C. This gives a ratio c/a of 0.546, making β-Sn highly anisotropic [17]. Alpha-Tin (α-Sn) has a diamond cubic crystal structure and is thermodynamically stable below 13.2℃ [47].

One of tin’s key properties is that is does not oxidize readily at room temperature, even in the presence of moisture [48]. Tin is also non-toxic. Tin has the ability to wet to (form intermetallic compounds with) a number of metals, making it attractive as a solder material. In addition to having a highly anisotropic crystal structure, key physical

properties such as elastic moduli and coefficients of thermal expansion are also strongly anisotropic [17].

Two main problems with the use of Tin as a solder material are Tin Pest and Tin Whiskers. Tin Pest refers to an allotropic phase transition that Tin undergoes a transition at about 13.2ºC. This has the effect (at lower temperatures) of causing the tin to become powder and disintegrate. Tin Whiskers are fine wire-like single-crystals of tin that grow on the tin solder surface and can eventually cause electrical bridging. Tin Pest can be effectively ameliorated (i.e. the transition temperature lowered or fully suppressed) via alloying, and it is hoped that Tin Whiskers may be dealt with in a similar fashion (research here is ongoing) [23].

2.7.1 Silver (Ag)

The Sn-Ag Binary Phase Diagram exhibits a eutectic point at a composition of 96.5Sn-3.5Ag (weight percentage) and temperature of 221℃ [2,3]. The microstructure at the eutectic composition consists of Ag_3Sn IMC platelets immersed in a beta-Sn matrix [22]. Eutectic SnAg provides relatively good wetting to Copper surfaces, good mechanical strength, and a relatively long life in cyclic fatigue testing (as compared to Sn-37Pb) [2]. The solid solubility of Silver in Tin is lower than that of Lead. This difference engenders higher resistance to grain growth over time and a “more stable and reliable grain structure than tin-lead solders” [2].

2.7.2 Bismuth (Bi)

The Sn-Bi Binary Phase Diagram exhibits a eutectic point at a composition of 48Sn-52Bi (weight percentage) and temperature of 138°C. The eutectic composition provides both a low melting temperature and high mechanical strength. Strength increases with Bismuth content. Counter-intuitively, its melting temperature may be considered too low for certain applications. Availability of Bismuth is also a concern for lead-free solder alloys containing a high percentage of Bismuth [2].

2.7.3 Copper (Cu)

The Sn-Cu Binary Phase Diagram exhibits a eutectic point at a composition of 99.3Sn-0.7Ag (weight percentage) and temperature of 227°C. The eutectic composition provides good mechanical strength at very low cost. However, the relatively high melting temperature is a concern for some applications, and this solder is better suited for wave soldering processes than reflow soldering [2,3].

2.7.4 Indium (In)

The Sn-In Binary Phase Diagram exhibits a eutectic point at a composition of 48Sn-52Ag (weight percentage) and temperature of 118°C. The eutectic composition provides a very low melting temperature, which can be advantageous for some applications. However, the mechanical strength is low, and the cost is high (low Indium availability). The Indium is also susceptible to corrosion in humid environments [2,3].

2.7.5 Antimony (Sb)

The non-eutectic composition of 95Sn-5Sb (weight percentage) has a pasty range of 232-240℃ [2,3]. "This solder is a solid solution of Antimony in a Tin matrix that has a relatively high melting point, making it suitable for high temperature applications" [2]. Strength and hardness increases with Antimony content and, for Sn-5Sb, is comparable to eutectic SnAg. Thermal fatigue performance is also good. However, wetting properties are relatively poor, and the toxicity of Antimony (Sb) is a potential concern [2,3].

2.7.6 Zinc (Zn)

The Sn-Zn Binary Phase Diagram exhibits a eutectic point at a composition of 91Sn-9Bi (weight percentage) and temperature of 199℃. Strength and temperature tolerance increases with Zinc content. However, Zinc is prone to oxidation and, therefore, this solder suffers from wetting problems, high drossing, and corrosion issues [2].

Chapter 3
Reliability of Electronic Solder Joints

3.1 Introduction

Quality and Reliability are among the most desirable attributes that an engineered product can display. Reliability can be defined as "[t]he probability that an item will perform a required function without failure under stated conditions for a stated period of time" [43]. Quality is similarly defined, but in reference to the exact condition of the product at it is delivered, rather than over a period of time [49,50].

Both the propensity of failures and the severity of the consequences of failure can vary widely between different products and applications. In cases where product margins are low and the consequence of failure is merely inconvenience, companies may choose to avoid the perceived overhead of formal reliability engineering efforts. Similarly, in cases where the product is a very simple or proven design with well understood reliability, traditional quality control approaches may be sufficient. Formal Reliability Engineering efforts are mostly restricted to cases of relatively complicated applications: applications where the consequences of failure are severe, or cases in which the reliability of the new products is hard to predict. Reliability Engineering has several objectives: [49,50]

1. To prevent or reduce the probability/frequency of failures
2. To understand and correct failures that do occur
3. To design strategies for coping with failures that cannot be prevented
4. To analyze reliability data and estimate the probable reliability of new designs

Reliability Engineering often involves the use of mathematical and statistical methods for quantifying and analyzing data. However, this mathematical analysis must always be backed up by engineering knowledge of the system or product being studied. Otherwise, it becomes impossible to understand the causes of failures and the possible methods for dealing with them. In general terms, the most common causes of failures in engineered products include: [49]

1. Inherent Incapability of the Design itself
2. Errors in specification, design, or manufacturing/production
3. Overstress Failure
4. Variations (either in the product or environment/stresses)
5. Wearout (e.g. Fatigue)
6. Other Time-Dependent Mechanisms (e.g. Creep)

3.2 Failure Modes in Electronic Assemblies

The history of Reliability Engineering is inseparable from that of the electronic assembly. The evolution of R.E. as an independent engineering discipline took place in the Unites States in the 1950s due to the expanding reliance of the military on electronics combined with the ever increasing complexity of electronic systems. At the time, the electronics industry was starting to employ a large number of new components, manufacturing process, and novel designs, and this lead to a reduction in product reliability and increasing system downtime and repair complexity. Consequently, the Advisory Group on Reliability of Electronic Equipment (AGREE) was created as a joint effort between the US Department of Defense and the electronics industry in 1952. A

new standards-based approach was created, which included specific reliability testing requirements. The initial AGREE report was published as US Military Standard (MIL-STD) 781, *Reliability Qualification and Production Approval Tests*. Over time, other organizations such as the International Electrochemical Commission (IEC) have issued their own standards and the standards themselves have evolved as new technologies have entered the market [49,50].

Figure 3.1, below, shows several of the common failure modes in a flip-chip mount assembly. When a flip-chip is assembled onto a laminate substrate, an underfill is used, typically an epoxy matrix with glass filler particles to control the Coefficient of Thermal Expansion and Modulus. This underfill is necessary to prevent catastrophic loss of reliability during thermal cycling. The common mechanical failure modes include: [2]

- Die Fracture
- Severing of Interconnections
- Wire Bond Failure
- Underfill or Encapsulant Cracking
- Delamination of Material Interfaces
- Solder Joint Fatigue

In the case of more conventional packages, cracking through the molding compound and failure of the wire-bonds or flip-chip interconnects can also be a problem [2].

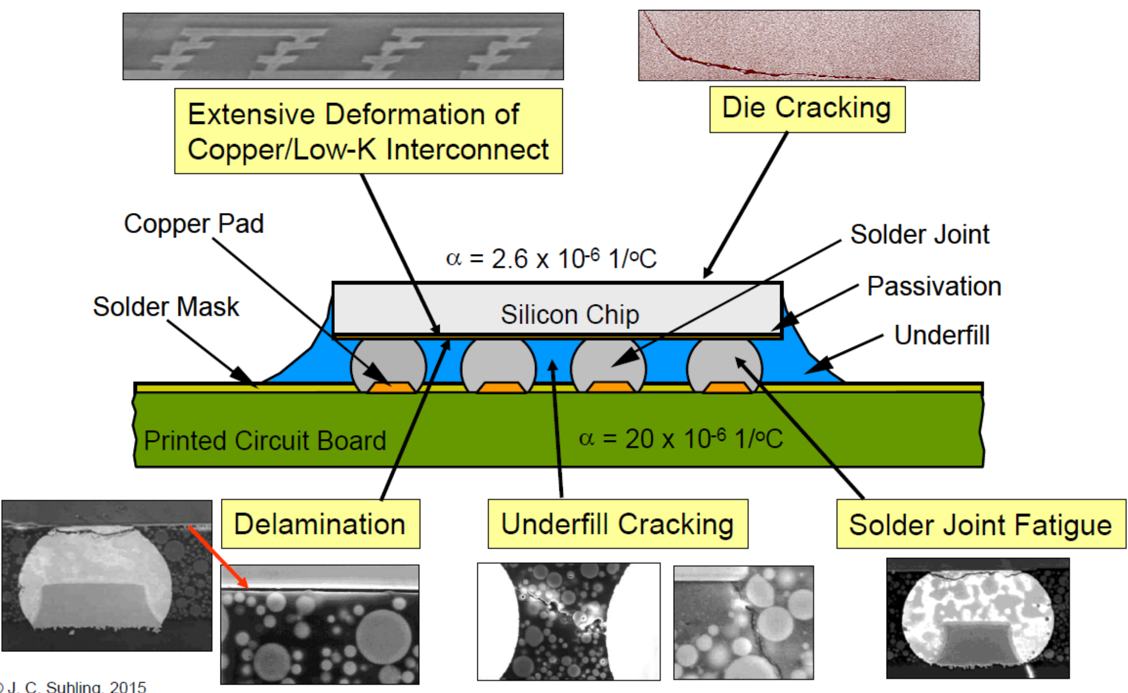


Figure 3.1. Common Flip-Chip Failure Modes [6].

Because the solder material has the lowest stiffness (modulus) of the major materials involved, the solder joints take up much of the strain accompanying thermal cycling of the circuit assembly [2].

3.3 Characteristic Solder Joint Failures

Electrical failure of an electronic component can most often be traced to the solder joints. Since certain types of failure (e.g. ductile) are more predictable and generally take longer, they are considered preferable to other types of failure (e.g. brittle). Two of the common failure modes observed in BGA-type solder joints are failure along the solder near the IMC boundary regions, and failures through the bulk solder material.

FAILURE ALONG IMC BOUNDARY FAILURE THROUGH BULK SOLDER

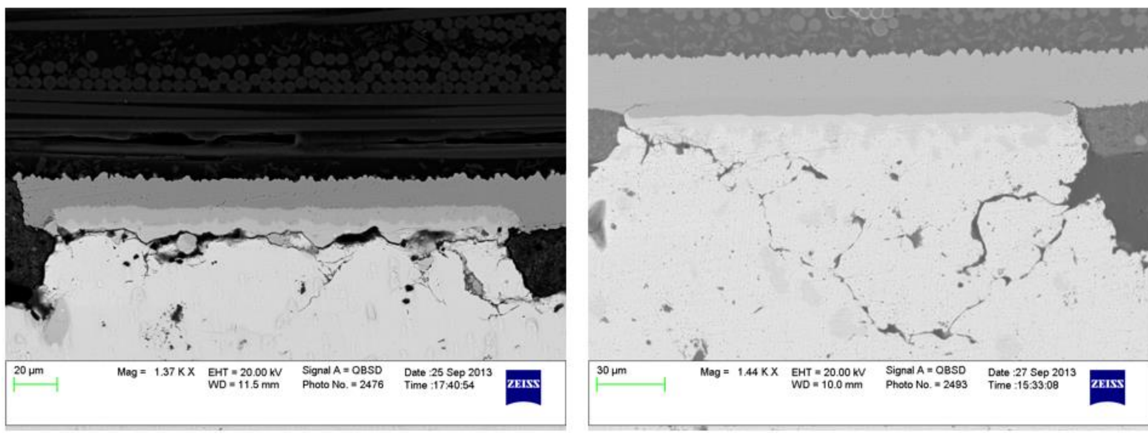


Figure 3.2. Common Joint Failure Modes.

Crack initiation most often occurs at locations along the top of the joint near the Intermetallic Layer. Cracks can propagate along the IMC interface layer, boundaries with other IMC inclusions, grain boundaries, or through the bulk solder (typically along twin boundaries). Crack propagation along the IMC interface layer leads to lower reliability and failure across the bulk solder is preferable from a reliability perspective [51–54].

3.3.1 Typical BGA Joint Failure Locations

Evaluation of the von Mises stress distribution indicates that the highest stress concentrations for an individual solder joint (of the BGA type) occur at the outside edges of the joint at the top and bottom (i.e. near the metallization layers of the component and substrate, respectively). For non-solder-mask-defined (NSMD) substrate lands, which have a characteristic divot shape, the highest stress concentrations are found at the opposite side of the joint, near the component UBM [51–54]. Because the highest stress concentration is typically found at the component-side, this is where crack initiation will subsequently occur (explaining the above experimentally observed crack initiation behavior [6].

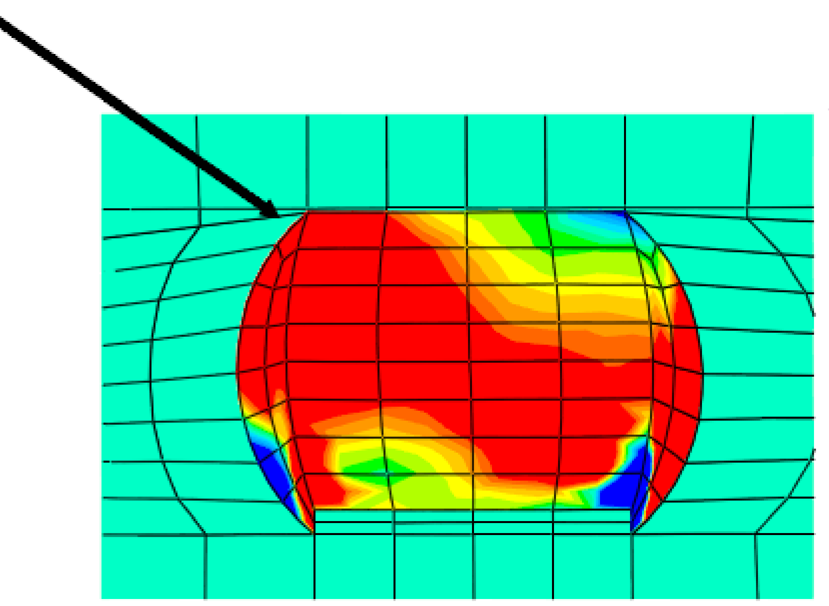


Figure 3.3. FEA model: Induced stress maximized at the upper corner of the joint [6].

Simple reliability prediction methods such as the Distance to Neutral Point (DNP) formula predict that failure will always occur at the outer-most solder joint (the joint furthest from the vertical center-line of the package). However, it should be noted that has been conclusively demonstrated this is not the case for many modern package types. For modern plastic packages, it is common to keep track of the position of the 'die shadow' within the package. The die shadow is the area underneath the silicon die, which does not extend the full width of the package [6].

The interposer layer and molding compound used in the construction of plastic packages are relatively closely matched to rigid laminate substrates in terms of the respective Coefficient of Thermal Expansion (CTE) values. The CTE mismatch between the silicon die and Printed Circuit Board (as well as other parts of the component) is much greater. As a consequence, the mismatch induces stresses are not maximized at the outermost joint, but at a joint close to the edge of the die shadow. The first solder joint to

fail will then typically be in around the edge of the die shadow and not along the outer edge of the package [2].

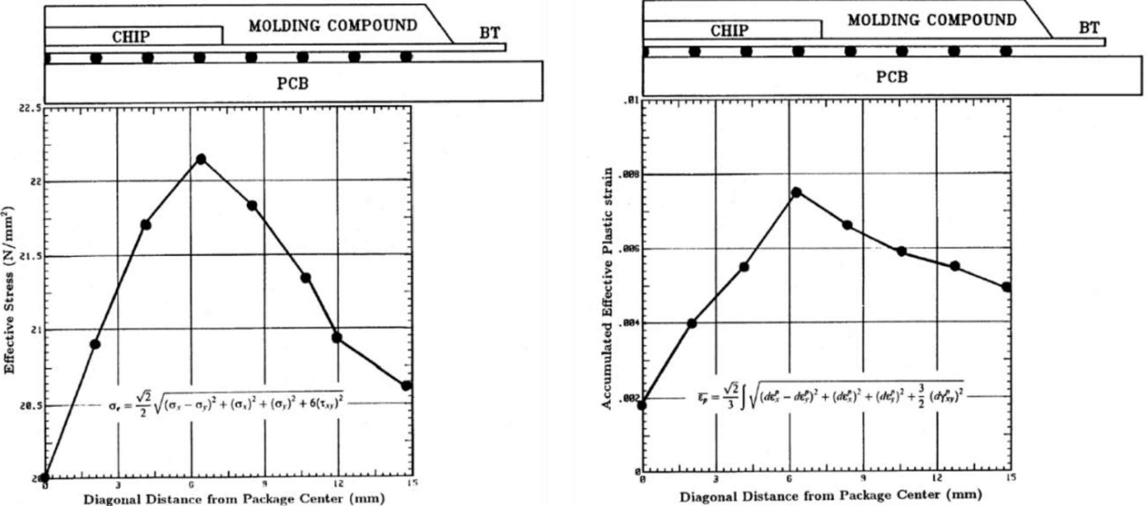


Figure 3.4. Stress and Strain vs. DNP [6].

Additionally, in Sn-Ag-Cu solder balled components, the failure of SAC solder joints far from the areas of maximum shear stress may be observed. This effect is hypothesized to occur because the microstructure of one joint may be very different than that of a neighboring joint. For instance, one joint may have a single β-Sn grain while a neighboring joint may have several grains. In some joints, grains may align in a manner more susceptible to shear modes experienced during thermal cycling. In conjunction with the known large anisotropies in the thermomechanical response of β-Sn, this means that damage progression in some joint will be much faster than in others. [34,42].

3.3.2 Some Factors Affecting BGA Solder Joint Failures

Other than the choice of solder material and assembly parameters, a variety of design parameters are known to have a predictable effect on the characteristic fatigue life of plastic BGA packages. The following list is adapted from Hai [55] and Suhling [6].

Since the shear stresses generated by the coefficient of thermal expansion (CTE) mismatch between the printed circuit board (PCB) and component are driving the fatigue process, is stands to reason that thicker PCBs result in significantly lower fatigue life.

Table 3.1. Effects of some Design Parameters on BGA Package Fatigue Life [6,55].

Design Parameter	Fatigue Life Improved by	Magnitude of Effect
Size of Silicon Die	Smaller is better	Large
Package Standoff	Higher is better	Large
SMD vs. NSMD Pads	NSMD is better	Large
Interposer Thickness	Thicker is better	Large
PCB Thickness	Thinner is better	Large
Mold Compound CTE	Higher is better	Large
Thickness of Silicon Die	Thinner is better	Small
Mold Compound Thickness	Thinner is better	Small
Mold Compound Modulus	Lower is better	Small

3.3.3 Experimentally Locating BGA Solder Joint Failures

A variety of non-destructive and destructive analysis techniques are common in the failure analysis of electronic interconnects. Some common methods are listed below in Table 3.2.

Table 3.2. Common Non-destructive and Destructive Interconnect FA Methods [56].

Non-Destructive	Destructive
Visual/Optical Inspection	Dye and Pry Testing
X-Ray (transmission) Inspection	Cross-Sectioning
Acoustic Microscopy (A-, B-, or C-Mode)	Scanning Electron Microscopy
Tomographic Acoustic Microimaging (TAMI)	Energy-Dispersive X-ray Spectrometry (EDS)
	High Powered (Optical) Microscopy

Cross-sectioning is one of the most common methods of destructive failure analysis used in assessing electronic solder joints. These techniques are adapted from typical metallurgical analysis methods. In order to examine the microstructure a specimen must first undergo a multi-step sample preparation process. The basic steps in metallurgical sample preparation are: [57]

- Sectioning
- Mounting
- Grinding
- Polishing
- Etching (optional, depending on specimen type)

Once a specimen has been prepared for study, it can be examined using optical or electron microscopy. Optical (white and polarized light) microscopy predates the invention of the scanning electron microscope by a few hundred years, and can be used effectively to examine the microstructure of materials. Optical microscopes are fast and easy to operate, generally (relatively) inexpensive, and don’t require a working vacuum.

They can provide magnifications (M) as high as approximately 5000X. However, the effective magnification of an optical microscope is limited by the optics' resolution, which is the minimum distance between two nearby points at which they can be visually distinguished as discrete from one another. Attempting to use a higher magnification will produce a larger image, but not necessarily a higher level of detail. Electron Microscopes can reach magnifications on the order of 20X to 100,000X and also provide superior depth of field (on the order of micrometers at 10,000X magnification) [57].

In addition to standard optical and scanning electron microscopy (BSE), several other analytical techniques are sometimes used in examining electronic solder joints. Energy dispersive spectometry is commonly used to garner compositional information during examination within the SEM. In cases where grain orientation information is also desired, Electron Back-Scatter Diffraction (EBSD) can also be used within properly outfitted SEMs. Beta-Tin can also be examined using Polarized Light Microscopy (PLM) in order to examine grain orientations. This technique relies on the birefringence of β-Sn, which arrises due to its tetragonal crystal structure [58–60].

3.4 Understanding Solder Joint Failures

As noted by Lau [56], a variety of environmental stress factors can result in the structural failure of solder joints or other electronic interconnects. These include: [56]

- Temperature
- Voltage
- Humidity
- Corrosion

- Current Density (Electromigration)
- Mechanical Bending, Shearing, or Twisting
- Mechanical Shock (Drop)
- Vibration

However, the most common types of failures in the field are Overstress ("overload") failures and Fatigue failures. Overstress failures occur when the applied stress on the solder joint exceeds the joint's capacity. This is similar to bending a metal girder until it snaps. Fatigue failures occur to localized plasticity under lower cyclic loads that leads to the initiation and propagation of a crack (or cracks) within the joint. Eventually, the joint will become unstable and fail when too little solder area remains connected.

Figure 3.5 shows some of the failure modes that are typically seen in ball grid array (BGA) type solder joints. Part (a) shows characteristic fatigue failure across the component-side near-interfacial region. Part (b) shows brittle failure (left-hand side) and ductile failure (right-hand side). Part (c) shows failure across a possible "dynamic recrystallization" zone.

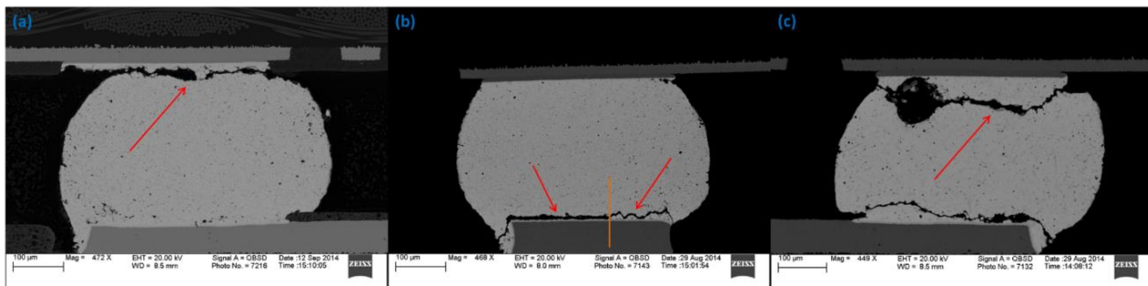


Figure 3.5. Some Failure Modes seen in BGA-type solder joints.

3.4.1 Fatigue

Fatigue failures result from cyclic stress loading at stress levels below the typical yield stress associated with the onset of necking and eventual failure. Fracture most often occurs under tensile conditions, and is time-delayed: Failure may not occur for 1,000s or even 100,000s of stress cycles. In many cases, the fracture surface will have characteristic lines referred to as "clam shell markings." Each line, or band, represents a period of fracture growth, rather than a single stress cycle. Once the surviving surface can no longer sustain the applied stress, catastrophic failure will result, which will often leave "chevron markings" on the remaining surface [61].

Fatigue crack growth can be ordered into three distinct stages. Stage 1 is crack initiation and transient growth. Cracks are formed in regions of high stress concentration – this is almost always at the sample surface, at a surface notch or other defect. If surface notches or other defects are present, they can aid in crack initiation. In general, however, the cyclic stress will lead to the formation of Persistent Slip Bands (PSBs), or zones of high cyclic slip activity. Local plasticity within the PSBs leads to the creation of small surface extrusions and intrusions, with the intrusions becoming micro-crack initiation sites. Stage 2 is steady-state crack growth. In this stage, under repeated stress cycling, the crack will propagate via repeated blunting (plastic deformation) and sharpening (fracture) of the crack tip. This is what leads to the characteristic "clam shell markings" that are often observed. Finally, Stage 3 is interaction and saturation. Here, small cracks will have grown to the point where they meet (interact), at which point the conglomerated crack propagates rapidly until failure occurs [61].

The majority of failures in engineered materials are attributable to fatigue. Solder joints for electronic assemblies are no exception, with the majority of joint failures driven by fatigue [13,62,63]. Fatigue in electronic solder joints is primarily caused by thermal cycling and CTE Mismatch issues. The Linear Coefficient of Thermal Expansion (CTE) is a way of approximating the expansion of a material along a single axis as a function of ΔT, the change in temperature. Here are some CTE values that are important for typical electronic assemblies using glass-epoxy laminate substrates and a variety of surface mount components:

Table 3.3. CTE values of some circuit assembly materials [3].

Material	CTE (ppm/^{o}C)
Epoxy	50-80
Glass Reinforcement	0.5
Substrate (x-y)	14-20
Substrate (z)	100
Copper Traces	16
Components	6-20
Bulk Silicon	2.6
Ceramic Alumina (SMR)	6.2

3.4.2 Creep & Grain Boundary Sliding

At low temperature, the dominant deformation mechanisms in crystalline solids such as solders are dislocation motion and twinning. However, at higher temperatures, other deformation mechanisms become important, and can even dominate the

deformation response of a material. Since the exact values of "high" and "low" temperature vary significantly, it is useful to define a temperature – known as the homologous temperature – by normalizing temperature values to the melting temperature of the material (i.e. T/T_m in K). We can then define "low temperature" as $T_H < 0.5T_M$ and "high temperature" as $T_H > 0.5T_M$, where T_H is the homologous temperature and T_M is the melting temperature of the material [61].

Creep is a time-dependent plastic deformation that can occur even at low stress levels if the homologous temperature of the material in question is high (e.g. greater than 0.5) [39,61]. Creep typically occurs via thermally-activated, stress-directed diffusion of atoms within a material ("diffusional creep"). However, creep can also occur via the movement of dislocations ("dislocation creep"). Researchers have posited a number of different creep mechanisms: [61]

- Nabarro-Herring Creep – atomic diffusion from grain boundaries experiencing tensile stress to those experiencing compressive stress through the bulk
- Coble Creep – atomic diffusion along grain boundaries
- Dislocation Creep – diffusion of dislocations for which several models exist (e.g. Weertman proposed edge-dislocation climb away from dislocation barriers)

As shown in Figure 3.5, part (a), it is common in materials engineering to create a deformation mechanism map based on the temperature and applied stress. Creep testing is commonly done by placing a bulk sample under tensile stress (generally constant load) and recording the strain (elongation) as a function of time. In general, three (3) distinct regions will be seen: (1) Primary (Transient) Creep, (2) Secondary (Steady State) Creep, and (3) Tertiary (Final) Creep, as shown in part (b) of Figure 3.6. As the material begins

to elongate, strain hardening mechanisms take hold (transient creep). Then, strain recovery mechanisms become active, and temporarily balance with the hardening mechanisms (steady state creep). Finally, recovery mechanism dominate, leading the material to soften until failure occurs (tertiary creep). The steady-state creep rate is both the minimum value observed and typically occurs for the longest time, and it is therefore taken as the reportable value [20,61].

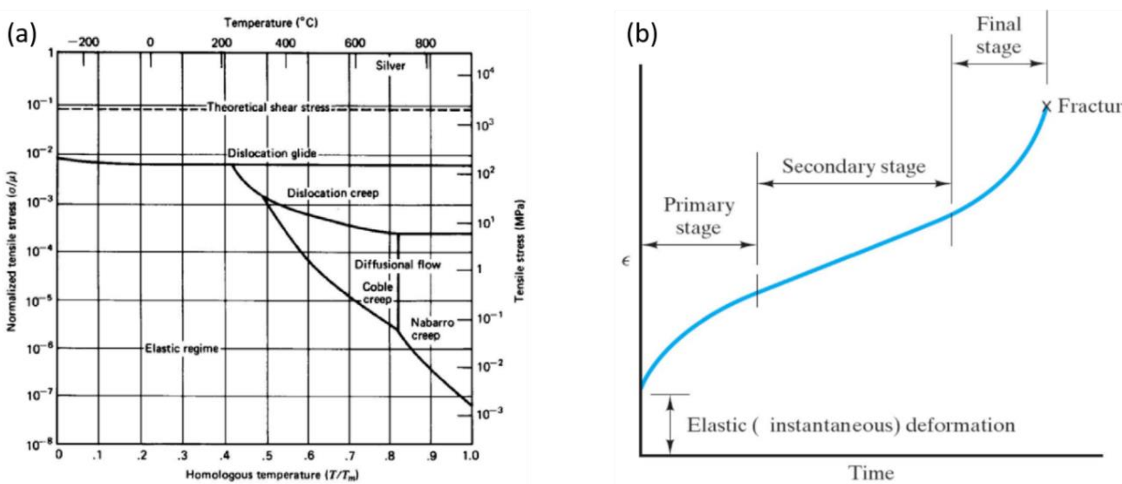


Figure 3.6. (a) Deformation Mechanism Map for Silver [61], (b) Stages of Creep [20].

Another important high temperature deformation mechanism is Grain Boundary Sliding. Grain Boundary Sliding does not occur independently but rather always takes place in conjunction with other deformation mechanisms (such as creep or bulk diffusion). Figure 3.7, shows how stress-directed diffusional elongation of grains in a material (a) would typically lead to inter-granular separation (b), but can be accommodated by grain boundary sliding (c).

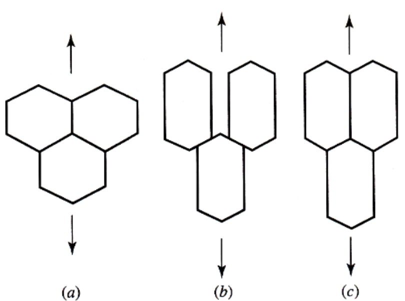


Figure 3.7. Grain Boundary Sliding [61].

3.4.4 Effects of Thermal Cycling on Solder Joints

Most electronics are not operated continuously in the steady state. Instead, use varies over time. Commonly, users will turn their electronics on, run them for some time, and then switch them back off. When an assembly is on and running, it will generate heat resistively. When it is turned off, it will cool again. This creates a cyclic thermal environment on the assembly. For non-climate-controlled environments, this thermal cycling is exacerbated by natural variations in temperature over the course of each day [2,3,13].

Electronic solder joints are mechanically constrained by the other materials of the electronic assembly (e.g. component and PCB) [17]. Because the Coefficient of Thermal Expansion differs for various parts of the assembly – in particular, the substrate and components – these cyclic thermal variations are converted to cyclic stress loads. For instance, let's say that the assembly has been 'switched on' and is heating from room temperature. The substrate has a higher CTE than a particular component we are examining. Because the substrate will expand faster than the component, stress is generated, which will be taken up largely by the solder joints attaching the components to the substrate [2,3]. In addition to the coefficient of thermal expansion mismatches between various parts of the electronics assembly, there are also local, microstructural-scale CTE mismatches between the various microstructural constituents in the solder and between the different grains of Tin (due to their anisotropy) [17]. This combination of thermal and mechanical effects is known as thermo-mechanical fatigue.

3.4.5 Failure Mechanics

Failures in electronic solder joints occur due to the combination of accumulated damage and overstress conditions. As damage builds up within the microstructure of the joint, at some point it can no longer withstand the applied stress, and failure occurs. Damage occurs when external energy from a source such as CTE mis-matches is stored as internal energy within the joint, typically in the form of dislocations (a type of lattice defect) within the crystal structure of the joint. As stress is applied, some energy is stored elastically (reversibly) via stretching of the atomic bonds within the solder. However, some energy will be stored via plastic deformation in the form of an increased density of dislocations [39].

Additionally, because the typical operating temperatures of electronic solder joints are relatively high in comparison with the solder melting temperature (i.e. high homologous temperature), Creep mechanics must also be considered. For most Sn-Ag-Cu solder materials, Tin (Sn) is the dominant component, and Tin has a homologous temperature (T/T_m in K) of about 0.6 at room temperature. The creep properties of SAC solders are therefore critical in determining the overall reliability of SAC solder joints [39].

Once internal energy has been stored in the solder material during plastic deformation, it then acts as the driving force for changes in the microstructure of the joint known as “restoration processes.” The principal restoration processes are (1) dynamic recovery (relaxation) and (2) dynamic recrystallization. Dynamic Recovery is a well-known process that occurs within many engineered materials and occurs via the “annihilation of lattice defects…by their movement to the grain boundaries where they

disappear and their rearrangement to form subgrain networks by polygonization" [39]. Dynamic Recrystallization a process where new grain boundaries are formed dynamically (i.e. during heating, but while stress is still being applied) within a material. This can occur through a variety of mechanisms. During plastic deformation, pure Tin is known to undergo recrystallization and grain growth even at relatively low temperature (i.e. room temperature) [35]. Telang et al. [64] reported that an incremental recrystallization process was observed in which a twin orientation originally in the minority of a grain (as reflowed) "grew and consumed the dominant initial orientation" [64].

The recovery process requires less activation energy than recrystallization, and would normally be the dominant restoration process in pure β-Sn [39]. However, dynamic recovery becomes more difficult in the presence of impurity atoms, particulate phases, and in areas where tangling has decreased dislocation mobility [39]. The presence of these impedances can inhibit recovery and allow for dynamic recrystallization to take place. A number of groups have demonstrated that dynamic recovery is taking place in Sn-Ag-Cu solder joints under power cycling conditions or in thermal cycle the testing [32,39].

Crack propagation has been shown to follow regions where microstructural changes due to recrystallization have occurred [32,35,39,64]. This susceptibility to cracking happens because the finer grain structure within the recrystallized region "fosters enhanced grain boundary sliding and strain localization in the recrystallized regions" [32]. Crack propagation results from the grain boundary sliding damage within the strain localized region (i.e. creep deformation [35]). As cyclic deformation continues,

intergranular cracking eventually results in a remaining joint that can no longer sustain the applied stress, resulting in final joint failure [32].

Henderson et al. [32] found that the amount of penetration of the recrystallized zones into the solder joint varied significantly between joints during fatigue failure. In particular, differences in penetration were often associated with existing β-Sn grain boundaries. This association indicates that in addition to the applied stress field, the stochastic nature of the existing (as reflowed) crystal orientations must be taken into account when considering the recrystallization process.

Various reports have found that fatigue crack propagation in Sn-Ag-Cu solder joints with high-Silver joints generally follow the IMC boundary failure pattern, whereas crack propagation in the bulk solder is more common in low-Silver joints. This difference in failure mode is commonly attributed to the higher ductility of low-Ag SAC solder joints. Additionally, large Cu_3Sn plates are more common in high-Ag SAC solder joints, and the role of Cu_3Sn plates in joint reliability is complex. Plates may act as crack propagation inhibitors in some cases, but large plates that end up aligned with the direction of a crack will instead facilitate propagation and are significantly detrimental to joint reliability [35].

3.5 Predicting Solder Joint Reliability under Thermal Cycling

The ability to predict reliability of solder joints subject to thermal cycling is self-evidently an invaluable planning tool. Because the electronics industry revolved around the use of eutectic SnPb solder for so long, a reasonable body of engineering knowledge was built up about the use and reliability of Tin-Lead solder. All too often, industry

insiders will attempt to use the performance of SnPb solder joints as a critical reference for any solder joint material. Unfortunately, the performance and reliability of lead-free solder joints have proven to be a different animal, and such simple comparisons often turn out to be misleading. Standard accelerated life testing was initially interpreted to favor lead-free joint reliability, but reliability in service may show just the opposite trend [34].

There are three general methods for determining the reliability of solder interconnects: (1) Analytical Solutions, (2) Numerical Methods, and (3) Experimental Testing and Data Analysis [2,6].

3.5.1 Analytical Solutions

Analytical solutions to solder joint reliability are obtained by creating a theoretical model of the system and solving the equations describing the system exactly. Often this involves generating a system of non-linear partial differential equations and solving the system based on using the obtained boundary values. However, the mathematical problem to be solved will depend on the model created. In some cases, very simple models can yield very simple equations and yet provide value by elucidating the important controlling variables of the system or useful order-of-magnitude estimates [2].

One analytical solution related to solder joint reliability that involves a very simple model and yet yields important physical insights is the Distance-to-

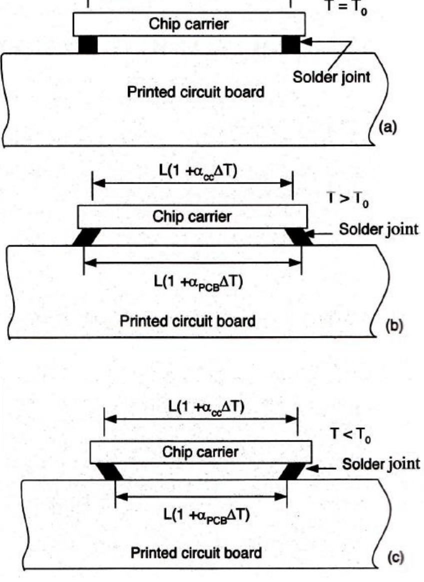


Figure 3.8. DNP Model [2].

Neutral Point, or DNP Formula. In the DNP model, we consider a two-dimensional model with a chip carrier surface mounted to a printed circuit board. A zero-stress temperature (T_o) is postulated, and temperatures changes to higher and lower temperatures are considered. Two solder joints are included in the model at either side of the chip carrier, but are considered to have zero modulus. Instead, the chip carrier and printed circuit board both undergo un-constrained linear expansion under the influence of temperature. Because the chip carrier has a much lower coefficient of thermal expansion than the printed circuit board, the PCB will expand (at elevated temperature) and contract (at reduced temperature) much more dramatically than the chip carrier [2].

Based on the different magnitude of the thermal expansion of the chip carrier and printed circuit board, the solder joints will be sheared in opposite directions depending on if the temperature is raised above T_o or lowered below T_o. The DNP formula uses a small-angle approximation to estimate this induced shear based on only a few simple factors: [2]

$$\gamma = \frac{(\alpha_{PCB} - \alpha_{CC}) * \Delta T * DNP}{h}$$

, where DNP = Distance-to-Neutral-Point is the distance between the inner edge of the solder joint at the PCB side to the mid-line of the system (i.e. line of bilateral symmetry, which is a stress neutral point), ΔT is $T-T_o$ (the change in temperature from the stress neutral temperature), α_{PCB} and α_{CC} are the CTEs of the printed circuit board and chip carrier (respectively), and h is the height of the solder joint. The DNP Formula states that the induced shear strain in the solder joint increases linearly with the distance-to-neutral-point and the change in temperature, and decreases linearly with the height of the solder joints [2].

Although the DNP Formula only predicts the induced solder joint shear stress, another analytical solution exists that directly predicts the fatigue life under thermal cycling based only on the plastic (irreversible) shear strain experienced by the joint during each thermal cycle. This is the Coffin-Mansion Relation:

$$N_f = 1.29(\Delta\gamma_p)^{-1.96}$$

, where N_f is the number of thermal cycles until joint failure and $\Delta\gamma_p$ is the plastic shear strain induced during each thermal cycle [2].

3.5.2 Numerical Methods

Unfortunately, the DNP and Coffin-Mansion relations have not proven as useful with modern package types and lead-free solders as one could hope [2,54]. In the absence of exact analytical solutions, numerical methods are often used. One type of numerical method that is very popular when considering the reliability of electronic packages and interconnects is the Finite Element Method (FEM). The FEM works by creating a model of some object of interest by cutting ("discretizing") it into a number of small regions. A set of governing field equations (based on solid mechanics) is specified and then modeled using approximating functions. The properties of each element are given initial values, and the elements are "assembled" into the proper form. A set of boundary conditions is specified, completing the model [54].

Because the governing field equations are derived from solid mechanics, they require an understanding of the stress-strain behavior of the material being modeled. A material's stress-strain response will depend not only on process variables but will also

change depending on the service conditions that need to be modeled. A variety of different stress-strain behaviors can exist, including: [54]

- Elastic
- Plastic
- Elastic-Plastic
- Viscoelastic
- Viscoplastic
- Continuum Damage

One advantage of the Finite Element approach over typical analytical solutions is that the FEM model can account for non-linear changes in material properties as a function of temperature [2]. Finite Element models must also take into account changes in material properties as a function of time. This is particularly important for materials that undergo significant microstructure evolution and are sensitive to changes in microstructure such as lead-free solders [31].

Because of the high homologous temperatures experienced by Sn-rich solders, the solder Creep behavior is very critical in calculating the deformations. An assortment of mathematical models have been proposed for use with Sn-Ag-Cu solder joints. Two common models used in simulating SAC solder behavior are the Elastic-Plastic-Creep (EPC) model and the Anand Viscoplastic (AV) model. The Anand model consists of "a flow equation and three evolution equations that describe strain hardening or softening during the primary and secondary creep stages" [39].

3.5.3 Experimental Methods

Experimental reliability testing and failure analysis are critical components of reliability engineering of electronic assemblies and are critical to supporting appropriate Design for Reliability [56]. Design for Reliability (DfR) begins by relying on existing engineering knowledge and often proceeds to initial proofing using some form of finite-element simulation, but subsequent experimental testing and failure analysis of a set of sample devices is still required for electronics, where device life is complex and often difficult to predict [56].

A variety of reliability tests can be used when assessing electronic assemblies: [56]

- Thermal (temperature) Cycling (TC)
- Thermal Shock (TS)
- Power Cycling
- Functional Cycling
- Moisture Sensitivity (e.g. IPC/JEDEC-020C)
- Temperature + Humidity (e.g. 85/85 testing)
- High-Voltage extended-life
- Salt-atmosphere (MIL-STD-883D)
- Pressure-cook test
- Mechanical bending, twisting, and shear (e.g. IPC/JEDEC-9702)
- Mechanical Shock (i.e. Drop Testing)
- Vibration
- Electromigration

- Etc.

3.6 Experimental Methods: Thermal Cycle Testing

The most common type of Accelerated Life Testing for electronics assemblies is the thermal cycling (TC) test. This is because thermal cycling tests simulate the effects of thermo-mechanical fatigue due to normal thermal variations during service life. Powered functional testing and mechanical cycling are also quite common. Powered functional and thermal cycling test are considered to be the most realistic for inducing solder joint fatigue. Powered functional testing should be performed in conditions that closely mimic those of the application environment [3]. Hence, it is far easier to standardize thermal cycling tests and compare results across experiments.

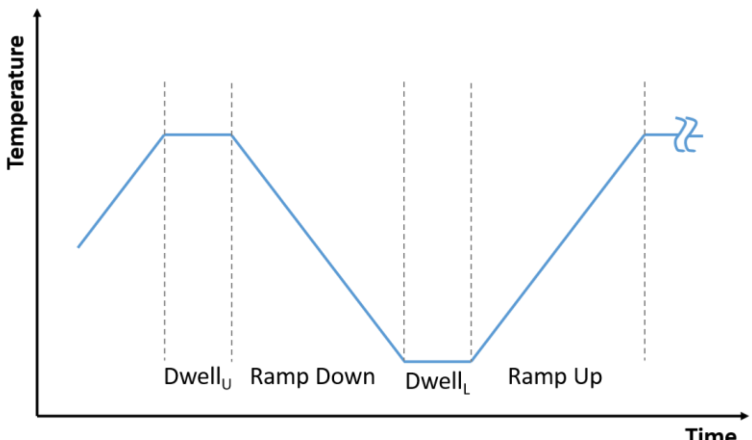


Figure 3.9. Schematic of Thermal Cycle.

Thermal cycling typically takes place in a single-zone chamber, in which the temperature is controlled to match a particular periodic pattern, or cycle. It is common to define each thermal cycle (or temperature cycle) using two (2) temperatures – an upper and lower dwell temperature – and four (4) time segments – the upper and lower dwell time and a ramp-up time and ramp-down time [56]. Many thermal cycles simplify this further by defining the a single dwell time for both upper and lower peak temperatures and a single ramp time for both ramp-up and ramp-down.

The most important parameters of a thermal cycling test are the dwell temperatures, the dwell times, and the ramp rates/times [3]. During each thermal cycle of the test, the components of the test vehicle/board experience thermomechanical fatigue that simulates the effects natural thermal cycles during service life. Figure 3.10, below, shows the cyclic fatigue damage during thermal cycling with and without taking into account the stress relaxation mechanisms that affect the joint during the high-temperature dwell. The case on the left would apply for a material such as Copper, where creep is negligible at the temperatures of the test (low homologous temperature). The case on the right would apply for materials that experience significant creep at the testing temperatures (i.e. solder materials).

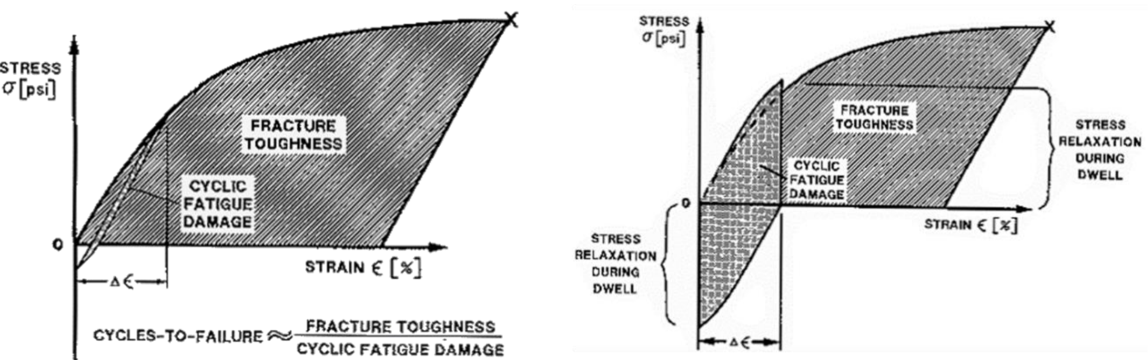


Figure 3.10. Cyclic Fatigue Damage during Thermal Cycling [3].

During thermal cycling, the cyclic fatigue damage from each cycle accumulates and eventually depletes the available fracture toughness, at which point failure occurs. Because high-temperature mechanisms (e.g. creep) are time-dependent, the longer the high-temperature dwell, the more stress relaxation will take place, and the higher the cyclic fatigue damage per cycle will be. As a consequence, longer dwell times at high temperature will cause fatigue failures to occur in fewer cycles.

As noted by Prasad [3], the high-temperature dwell experienced by printed circuit assemblies in the field are typically much longer than those used in thermal cycle testing. Therefore, thermal cycle tests require more cycles to cause fatigue failures. Therefore, accelerated testing has the counter-intuitive effect of requiring more cycles-to-failure. (Note, however, that this is the number of cycles, and not the total time that is required to generate failures.) This difference in cyclic fatigue damage needs to be taken into account when estimating product reliability. Product reliability can also be improved by minimizing the cyclic fatigue damage. This is often done by controlling the coefficient of thermal expansion (CTE) and modulus of various parts of the assembly [3].

Since the thermal environment of the assembly will vary depending on the desired application, it is important for reliability testing purposes to assess assemblies in an application-specific manner. There is no consensus among different markets of the thermal cycling parameters to be used [3]. Here are a few application areas and the corresponding typical dwell temperatures used in thermal cycle testing:

Table 3.4. Dwell Temperatures for TC testing by application [3,13,51,65]

Market	Low Temperature	High Temperature
Consumer	0ºC	70ºC
Telecommunications	0ºC	100ºC
Industry	-40ºC	85ºC
Automotive	-40ºC	125ºC
Military	-55ºC	125ºC

3.6.1 Thermal Cycle Testing: Statistical Analysis

The evaluation of experimental data from thermal cycling and other accelerated life testing is done using Reliability Statistics. Reliability Statistics are typically divided into three areas: Point Processes, Discrete Functions, and Continuous Functions. However, since statistics is a set of mathematical tools for analyzing and interpreting data sets, the difference between Discrete and Continuous functions is essentially one of how the data is treated [66].

When numerically analyzing life data such as data from thermal cycling tests, it is very common to take the discrete data points (i.e. Failures) and "fit" them with continuous functions, which are easier to deal with mathematically. The functions used for fitting are referred to as "distributions" in statistics. This method of treating the data is known as the parametric method and includes the following steps: [50]

- Plotting the Data
- Identifying a Candidate Distribution
- Fitting the Distribution to the Data
- Extracting Information from the Fitted Distribution

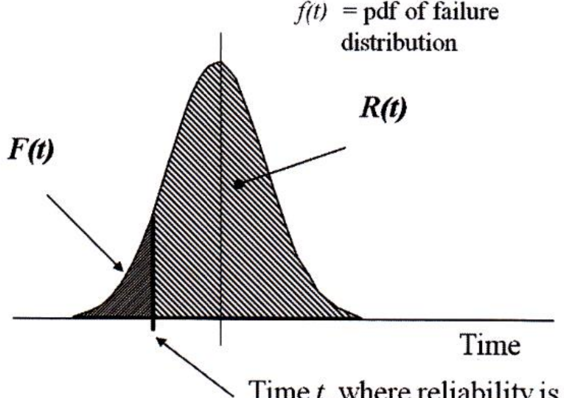


Figure 3.11. Probability Density Function (pdf) and its application to Reliability [66].

If one plots failures against time, a probability density function (PDF), f(t), can be fitted to the experimental data. By definition, the cumulative distribution function (CDF), F(t), is then the total

percent of failures as a function of time. The CDF may also be referred to as the Unreliability, Q(t). The Reliability is defined as the percent of survivors as a function of time, R(t), and is related to the CDF via the equation R(t)=1-F(t) [56]. Figure 3.11 shows the relationship between these three functions graphically.

Another function commonly used in Reliability analysis is the Failure Rate – or "Hazard Rate" – h(t). This is found by dividing the probability density function by the reliability function h(t) = f(t)/R(f). Many products have a failure rate (hazard rate) with three distinct sections, as shown in Figure 3.12, below. This type of failure rate curve is known as "bathtub curve" [50,66,67].

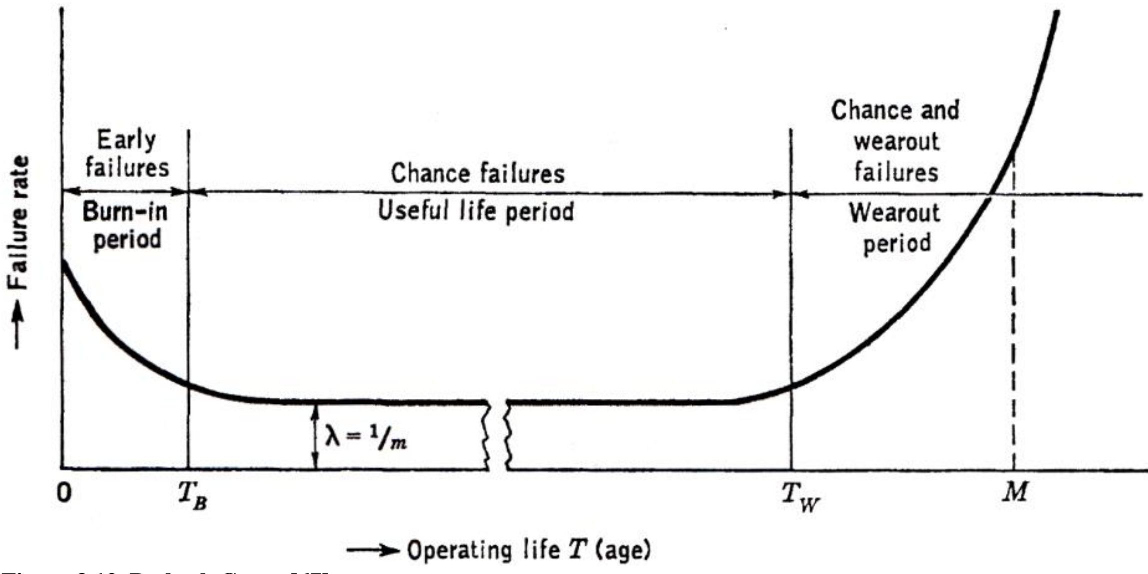


Figure 3.12. Bathtub Curve [67].

Early failures in the first section are referred to as "infant mortality". These infant failures are due (primarily) to inherent defects in the item that stem from the manufacturing processes used. Because the failure rate is decreasing in this section, so long as failed components/products are removed from a population, the reliability of the population increases with time during this zone. Burn-in is performed in this section to weed out the weak units (which are either removed or repaired). In the second section,

"random" (or catastrophic) failures occur. This area of the curve is considered to be the "useful life" of the product. The failure rate in this area is at its lowest point and is often treated as being approximately constant. This failure rate is due to the cumulative effects of a large number of random and uncontrollable variables (e.g. an end-user drops their phone). In the third section, "wearout" failures take place. The failure rate here increases sharply over time. These are failures due to accumulated stress from the operating environment: aging, wear, and fatigue [2,66,67].

The attribute of constant failure rate observed during the "useful life" area of the above bathtub curve is unique to a particular statistical distribution known as the exponential distribution. The probability density function of the Exponential distribution is:

$$f(x) = \lambda e^{-\lambda x} = \left(\frac{1}{\theta}\right) e^{\frac{-x}{\theta}}, \quad where \left(\frac{1}{\theta}\right) = \lambda$$

For real-world reliability numbers, however, the exponential distribution is not always the best distribution with which to fit the data. Ebeling [50] writes that identifying candidate distributions with which to fit reliability data is "both an art and a science." It is important to both know the characteristics of the distribution and to have an understanding of failure process(es) of the product [50].

In practice, many Reliability Engineers primarily use the Weibull distribution, which can be thought of as a generalized form of the exponential distribution. The 2-Parameter Weibull distribution has the advantages of ubiquity and ease of interpretation/communication of parameters, and is the most commonly used. It is very common to fit experimental data from thermal cycling and other accelerated life testing

using the 2-Parameter Weibull distribution. The probability density function, cumulative distribution function, and reliability function of the 2-Parameter Weibull distribution are:

$$f(x) = \left(\frac{\beta}{\eta}\right)\left(\frac{x}{\eta}\right)^{\beta-1} e^{-\left(\frac{x}{\eta}\right)^{\beta}}$$

$$F(x) = 1 - e^{-\left(\frac{x}{\eta}\right)^{\beta}}$$

$$R(x) = e^{-\left(\frac{x}{\eta}\right)^{\beta}}$$

, where x is the "time" (i.e. number of thermal cycles), β is the Shape ("slope") Parameter, and η is the Characteristic Life (63.2% failure point) [56].

Note that the Weibull distribution Characteristic Life is not equal to the mean-time-to-failure (MTTF), but serves a similar purpose when comparing data. The Characteristic Life represents the point in "time" at which 63.2% of a population will have failed. The Shape (or "slope") parameter is a new addition when moving from the Exponential distribution, and allows the Weibull distribution great flexibility. The Weibull distribution can "look" very different depending on what value the shape parameter takes on: [66]

- $\beta < 1$: Distribution has a decreasing failure rate (DFR) {see infant mortality}
- $\beta = 1$: Distribution has a constant failure rate {Exponential distribution}
- $\beta > 1$: Distribution has an increasing failure rate (IFR) {see wearout}
- $\beta = 3.5$: Weibull distribution approximates the Normal Distribution

As the Shape Parameter of the Weibull distribution increases, the distribution morphs from a DRF appearance to a "bell curve." At a shape parameter of 3.5, the Weibull approximates the Normal distribution. As the shape parameter continues to increase, the peaked-ness of the distribution increases in turn. This flexibility means that

the 2-Parameter Weibull can be used to fit a wide variety of life data [66]. The two parameters are easily compared between experiments and each conveys clear and important information about the distribution.

In order to make use of the Weibull distribution for analysis purposes, it was traditional to create a "Weibull Graph." Weibull graphing was originally done by hand using the power of logarithms. By taking the double log of the Weibull reliability function, one obtains the following:

$$\ln \ln[\frac{1}{1 - F(x)}] = \beta \ln x - \beta \ln \eta$$

Originally, life data would be taken and formatted as shown in the left-hand-side of the equation, and then plotted on a special Weibull paper (or probability paper). When the independent variable is taken to be ln(x), the right-hand-side of the equation becomes a straight line. Prior to the advent of modern computers, engineers would simply draw a line of best-fit by hand based on the plotted data. In a modern context, computer software is available that will fit the line using a least-squares fitting algorithm and provide goodness-of-fit information (such as residuals). Figure xxx shows the use of probability paper to fit Weibull data. Once the graph has been completed, the extraction of the Characteristic Life and Shape parameter is quite easy. The Characteristic Life is simply the corresponding "time" value at the intersection point of the fitted line with a horizontal line drawn at the 63.2% cumulative percentage level. The slope of the fitted line is equal to the Shape parameter. (For this reason, the shape parameter is sometimes loosely referred to simply as the "slope.")

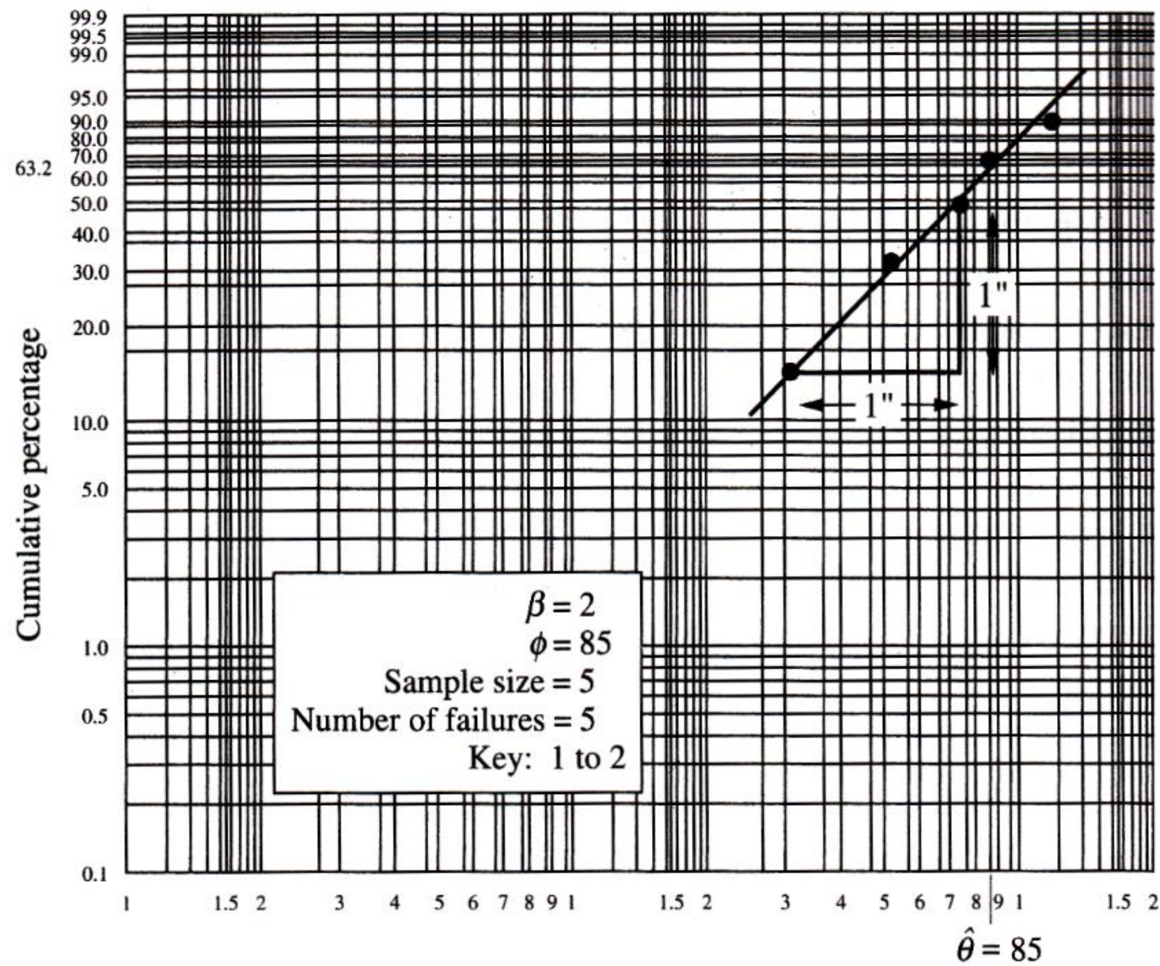


Figure 3.13. A Weibull Plot on Probability Paper [50].

Chapter 4
Reliability Impact of Shift to Lead-Free Solder Joints

4.1 Introduction

The semiconductor and packaging industries have been moving away from the use of Lead (Pb) due to the increasing awareness of the health and safety concerns surrounding its use. For many applications, the industry has moved from eutectic Sn-Pb solder to the near-eutectic Sn-Ag-Cu (SAC) solders. Figure 4.1 shows that the Sn-Ag-Cu, or SAC, solders dominate the lead-free market (c2011). Part (a) shows different lead-free solders and Part (b) shows different types of SAC solder alloys.

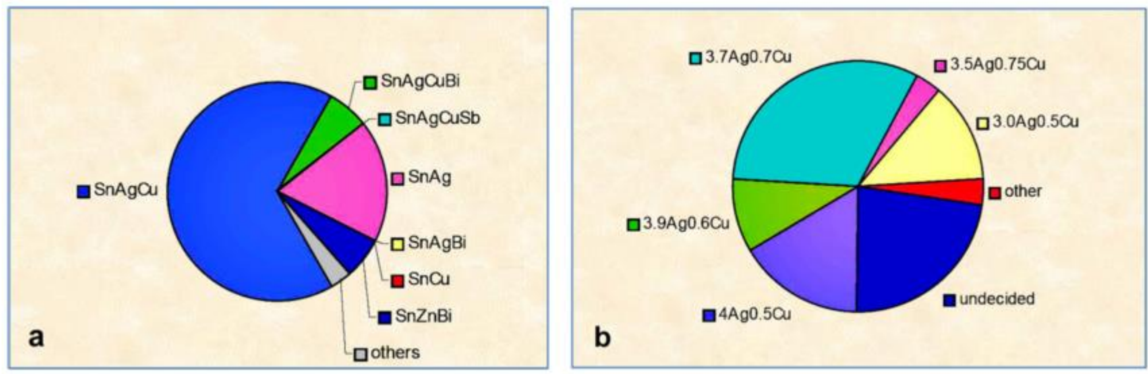


Figure 4.1. From [68]. Survey of the market share of lead-free solders.

More applications of SAC solders – including those considered extreme environment – are likely to take place in the near future. However, the reliability of electronic assemblies with SAC solder joints has proven hard to predict based on previous experience with SnPb solders.

4.2 Thermal Cycle Reliability of Sn-Pb and Sn-Ag-Cu Solders, As Reflowed

One of the factors motivating the selection of the Sn-Ag-Cu solders as a replacement for Sn-Pb eutectic solder is the performance of these solders in comparison to Sn-Pb in as-reflowed thermal cycling tests. As-reflowed, SAC solders typically display higher characteristic life in thermal cycle testing compared with SnPb controls. Table 4.1, below, shows data from the iNEMI Pb-Free Alloy Characterization Project Report (Part II). Two different thermal cycles are summarized, each of which has 10-minute dwell times.

Table 4.1. Summary of Lead-Free and Sn-Pb Thermal Cycle data from [51].

		CABGA 192		CTBGA 84	
Solder Alloy	Temp. Cycle	Char. Life (η)	Slope (β)	Char. Life (η)	Slope (β)
SnPb	0/100 °C	1477	12.39	2381	11.01
SnPb	-40/125 °C	658	6.77	988	5.67
SAC405	0/100 °C	6164	8.17	11433	5.63
SAC405	-40/125 °C	1298	5.62	2417	2.91
SAC305	0/100 °C	5718	6.99	9819	7.05
SAC305	-40/125 °C	1611	6.52	2430	5.83
SAC205	0/100 °C	5312	10.66	9062	7.12
SAC205	-40/125 °C	1268	5.49	2232	6.50
SAC105	0/100 °C	4910	5.40	6826	7.87
SAC105	-40/125 °C	940	4.94	1581	3.85
SN100C	0/100 °C	3066	10.03	6625	8.00
SN100C	-40/125 °C	826	7.95	1682	5.09

The most obvious top-level take-away from the iNEMI data is that the Characteristic Life of all of the tested Lead-Free alloys exceeds that of eutectic SnPb solder in as-reflowed thermal cycle testing. Osterman and Dasgupta [69] performed a

variety of mechanical and reliability testing comparing SnPb and SAC solders. They found that SAC solders yield at lower stress values than eutectic SnPb, but have a higher resistance to creep. They posit that "[t]he higher creep resistance helps explain the generally observed longer fatigue life of SAC as compared with Sn37Pb under temperature cycle loading" [69]. A number of other studies have also shown higher as-reflowed thermal cycling performance for SAC solders compared with SnPb [70–74].

As noted in section 4.5, however, although SAC solders have superior as-reflowed reliability under most test conditions, in cases of low package compliance and high-stress conditions, SnPb solder may perform better [69,75].

4.3 Reliability Effects of Composition on Sn-Ag-Cu (SAC) Solders

As discussed in Chapter 2, a variety of elements can be used in Lead-Free solder alloys. However, in the case of the near-eutectic Sn-Ag-Cu (SAC) solders, the materials are predominantly Tin (Sn) with relatively small amounts of Silver (Ag) and Copper (Cu) added. Typical mixtures involve [1-4] percent Silver and less than 1 percent Copper. Due to the high cost of Silver and its role in the formation of large primary (Ag_3Sn) precipitates – which have a significant role in the overall mechanical properties of the solder – most studies have focused on examining the role of varying Silver content on the reliability of different SAC formulations.

In general, studies [51,68,72,73,76–83] have found that there is a decrease in the thermal cycling performance of Sn-Ag-Cu solders as the Silver (Ag) content is decreased. Figure 4.2, from [50], shows the characteristic life under thermal cycle testing of

CABGA192 packages as a function of Silver content in Lead-Free Solders (Ag content is decreasing to the left).

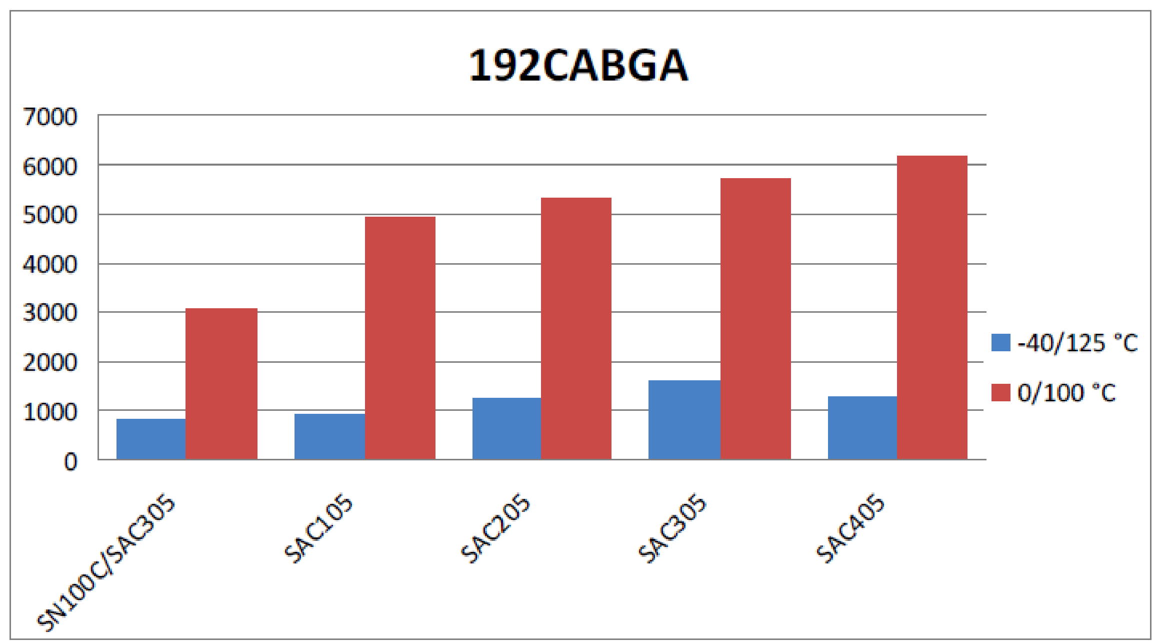


Figure 4.2. From [51]. TC Characteristic life vs. Silver content, CABGA192.

Shnawah et al. [68] performed a variety of mechanical and reliability testing on a series of Sn-Ag-Cu solders with varying Silver (Ag) contents. Their results confirm that high silver content (≥3%) SAC solder provide higher thermal cycling reliability than low silver content (≤2%) SAC solders. They attribute this thermal cycling improvement to three factors: [68]

1. Higher numbers of primary Ag3Sn precipitates, which increase the effective modulus and help suppress dynamic recrystallization
2. Higher incidence of initial microstructures that are either single crystal-like or fine-grained, as these are more resistant to thermo-mechanical fatigue
3. Higher numbers of coincidence site lattice (CSL) boundaries, as these are also more resistant to thermos-mechanical fatigue

However, Shnawah, et al. [68] also found that that high silver content (≥3%) SAC solder suffer from much lower drop impact reliability than low silver content (≤2%) SAC solders. They attributed this to the lower effective modulus and higher plastic energy dissipation of the low silver content SAC solders. This result is in line with other studies [81,84], and indicates that a single SAC composition is unlikely to be found that performs well in both drop applications and thermal cycling applications.

Furthermore, it is believed that the occurrence of very large Ag_3Sn plates (primary precipitates) in large numbers, which can occur in high silver content SAC solders such as SAC387, can undermine overall joint reliability [54]. Kang et al. [54] found that low silver content can be beneficial to thermal fatigue life under specific test parameters (low ΔT and frequency) but not for others (higher ΔT and frequency).

4.4 Reliability Effects of Process Parameters on Sn-Ag-Cu Solders

As mentioned in Chapter 2, the near-eutectic Sn-Ag-Cu solders require a significant amount of undercooling (10–50ºC) to nucleate the β-Sn grains. Also, unlike Sn-37Pb, which has the lamellar structure characteristic of eutectic alloys, SAC alloys are typified by one or few grains of β-Tin with Intermetallic particulates at the grain or dendritic boundaries [29,32–35]. Therefore, it should be expected that the SAC solders are more sensitive to changes in the soldering process parameters, particularly the cooling rate. From a materials engineering perspective, microstructures with fewer – ideally a single – grain are expected to be more resistant to creep-based failure mechanics.

Qi et al. [70] assembled SAC387 test vehicles for thermal cycle testing with three different cooling rates: 1.6°C/sec, 3.8°C/sec, and 6.8°C/sec. Predictably, the pad-side

intermetallic thickness was found to increase as the cooling rate decreased. The medium cooling rate (3.8°C/sec) was found to have the best wetting and lowest voiding percentage, and also performed the best in thermal cycle testing. SAC387 samples were found to have lower overall wetting that SnPb controls, and finite-element analysis performed indicated that "poor wetting could increase the total strain in the solder joint" [70].

Meanwhile, Kim et al. [63] found that lower cooling rates were beneficial to SAC387 solder joints, but that low silver content joints were relatively insensitive to cooling rate. They attribute the benefits of lower cooling rate to two factors: 1) lower residual stress and strain following solidification and 2) coarser β-Sn dendrite/grain structure (beneficial to creep resistance). Coyle et al. [72] observe an improvement in thermal cycle fatigue life for both high silver content and low silver content SAC formulations, which they attribute to a "more elongated or lamellar intermetallic morphology which appears to be more resistant to coarsening."

4.5 Reliability Effects of Test Parameters on Sn-Ag-Cu Solders

For Tin-Lead solder joints, the effects of thermal cycle test parameters were relatively predictable, and Acceleration Factors were commonly calculated using equations such as:

$$\alpha = \left(\frac{f_o}{f_T}\right)^q \left(\frac{\Delta T_T}{\Delta T_o}\right)^c e^{1414\left(\frac{1}{T_o}-\frac{1}{T_T}\right)}$$

, where the subscripts T and O indicated testing and operating conditions, respectively, and f is the thermal cycling frequency and T and ΔT the temperature and

temperature range in degrees Celsius. For SnPb solders, typical values used for the parameters q and c are: $q = 1/3$ and $-c = [1.9, 2.0]$

It is not yet known if similar metrics will be applicable to Lead-Free solders, but so far they have proven much harder to model. It has been reported that "the thermal-fatigue behavior of Pb-free solder joints is dramatically more sensitive to the choice of accelerated thermal cycle (ATC) temperature range and peak temperature than eutectic Sn-Pb controls" [35]. Some researchers have suggested that the higher accelerating factors typically used in thermal cycle testing may be too high and produce unrealistic failure modes in Lead-Free solders [85]. However, this is clearly very dependent on the intended application area.

The iNEMI report found what they considered to be an "unexpected or anomalous" effect on Lead-Free solders from the temperature range. Thermal Cycle Testing using the automotive range (-40/125 °C) was found to accelerate Lead-Free solder fatigue failures "much faster than expected," – an acceleration factor almost 5 times faster that for the telecommunications range (0/100 °C) rather than the anticipated 2-3.5 times [51]. SnPb solder was relatively insensitive to the choice of temperature range. Hokka et al. [86] also compared characteristic lifetimes under "extreme-operation" (-40/125 °C) and "standard" (25/125 °C) accelerated conditions, and found a similar significant reduction in both cycles-to-failure and time-to-failure at more extreme dwell temperatures for Lead-Free solders. Hou et al. [87] studied Flip Chips using (-40/125 °C) liquid-to-liquid shock testing and found that SAC solder performed slightly worse than SnPb.

Qi et al. [75] examined the impact of ramp rate and temperature range on Lead-Free and Tin-Lead solders using two components: one BGA package (PBGA 256) and one SMR (SMR 2512). They found that "the higher ramp rate reduced the testing time while retaining the same failure modes, and that the damage per cycle increased with the temperature difference" [75]. Interestingly, they found that for the surface mount resistors (SMR 2512) the lead-free solder performed better for the smaller ΔT tested, but – surprisingly – were inferior at the larger ΔT. The lead-free solder performed better under both test conditions when used on the BGA package. Therefore, in cases of low package compliance and high-stress test conditions, SnPb solder may perform better that lead-free solders [75]. This result is in agreement with findings from Osterman and Dasgupta [69] and Smetana et al. [88]. Clech [89] also reports that SnPb is relatively insensitive to ramp rates, as compared with the SAC solders.

Lall and Mirza [90] looked at the effect of mean temperature on thermal cycle reliability of Lead-Free solders. They compared test vehicles subjected to three different temperature cycles: 1) (-50/50°C), 2) (0/100°C), and 3) (50/150°C). The difference in dwell temperatures (high-low) was constant at 100°C for all three profiles, but the mean temperature changes from: 1) 0°C to 2) 50°C to 3) 100°C. They found that as the mean temperature of the thermal cycle was increased there was "higher plastic work per cycle and a lower cyclic thermal fatigue life" [90].

The effect of dwell time on the thermal cycle reliability of Lead-Free solders is also significant, although perhaps not anomalous. Coyle et al. [72] found a similar reduction in characteristic life upon changing dwell time for both SnPb and Lead-Free (SAC405, SAC305, and SAC105) solders when testing with surface mount resistors

(SMRs). Wilcox et al. [91] found a 50% reduction in the characteristic life of SAC305 when increasing dwell times from 10 minutes to 60 minutes (0/100ºC), and assert that this 50% reduction is in line with other studies found in the literature for the same package (CTBGA 84).

It should also be noted that the normal decrease in characteristic lifetime of Sn-Ag-Cu solders as Silver (Ag) content may also be tempered for test conditions involving large temperature ranges (ΔT). For instance in the iNEMI Report Part II (see Table 4.1), Parker et al. found that "The relationship between fatigue life and Ag content is more apparent with the 0/100 °C cycling and less noticeable with the -40/125 °C cycling" [51]. Lee and Ma [92] similarly found a relatively small thermal cycling performance difference between SAC305 and SAC105 using a high-stress temperature range (ΔT). The attributed this to rapid coarsening of the primary Ag_3Sn precipitates at high temperatures. These results are confirmed by Coyle et al. [73], who find that "the beneficial effect of Ag on accelerated thermal cycling reliability…diminishes as the severity of the accelerated thermal cycling, defined by greater DT, higher peak temperature, and longer dwell time, increases" and also by Zhang et al. [40].

4.6 Effects of Isothermal Aging on Sn-Pb and Sn-Ag-Cu Solders

As discussed in Chapter 2, both Sn-Pb solder and the near-eutectic Sn-Ag-Cu Solders undergo significant microstructural evolution during isothermal aging. As with eutectic SnPb solder, some grain coarsening occurs in the near-eutectic Sn-Ag-Cu solders during isothermal aging. Chen et al. found that the β-Sn grains in SAC solder joints gradually coalesce during thermal cycling. At the same time, low-angle boundaries were

found to emerge as a precursor to dynamic recrystallization [39]. IMC thickening also takes place at the metal pad surfaces in both Sn-Pb and SAC solder joints [63].

However, in the Sn-Ag-Cu an additional important microstructural evolution mechanism solders exists: grain coarsening of the Intermetallic precipitates, rather than the β-Sn domains. A variety of studies have shown that coarsening of the secondary precipitates is a significant driver in the reduction of strength in SAC solder joints during aging [40,42–46].

It should be noted that while softening due to grain coarsening is disadvantageous from a thermal cycling reliability perspective, it can improve drop reliability [93]. However, thickening of the pad-side Intermetallics, in conjunction with Kirkendall Voiding, can eventually offset or overwhelm this advantage [94].

4.6.1 Effects of Isothermal Aging on Sn-Ag-Cu Solders: Mechanical Properties

A number of studies have been performed on bulk Sn-Ag-Cu solder samples, showing that isothermal aging can cause reductions in a variety of mechanical properties including modulus, yield stress and ultimate tensile stress and creep resistance [95–98]. Lall et al. [99] also studied the effect of isothermal aging on the material properties of Innolot (Sn3.8Ag0.7Cu3Bi1.4Sb0.15Ni). They examined aging at 50oC for durations of 1 day, 30 days, and 60 days and measured stress-strain curves at two different strain rates (10/s and 35/s). Comparing the Innolot results to previous work they had performed on SAC105 and SAC305, they concluded that Innolot was much more strain-rate dependent, but experienced much lower degradation in material properties as a function of aging time [99]. However, there is some doubt about the ability of these bulk property

measurements to accurately map to the properties of solder joints, which may display dissimilar microstructures. This presents a significant experimental difficulty.

The standard tools used in mechanical and materials engineering to test the mechanical properties of materials have traditionally been designed to work with relatively large, “macro-scale” samples. Historically, these tools were primarily intended to understand the strength of large structural members such as those found in an automobile or building. With such large samples, micro-scale differences in the grain structure of different coupons become unimportant, and the average of the physical and mechanical properties from a large number of grains is observed.

Since most solder joints for standard ball grid array (BGA) packages have dimensions on the order of 1mm or less, solder materials have – until recently – been quite difficult to study mechanically in their true/application form. Bulk properties were all that was available. However, these bulk measurements do not take into account the anisotropy of the individual β-Sn grains or give information about the intermetallic phases present. Particularly for Lead-Free solders that exhibit a grain structure with one to a few grains (i.e. the SAC solders), these properties were often misleading.

Recently, a new measurement technique has gained in popularity. This technique is known as Nanoindentation (or sometimes “instrumented indentation”). Nanoindentation is capable of measuring the properties of individual β-Sn grains and intermetallic phases within a ball grid array (BGA) solder joint. Nanoindentation involves driving a small indenter into the surface of the sample while measuring the load on the indenter and the displacement/penetration of the indenter. The Modulus and Hardness of the material surface can then be calculated from the resulting load-displacement plot [61].

The tips used on the Nanoindenter are typically a three-sided shallow pyramid ("Berkovich indenter") [61], and are small enough that many indents can usually be made in a single β-Sn grain.

The use of Nanoindentation as a tool to examine the mechanical properties of solder materials appears to be gaining in popularity. A number of studies using this technique are now available that examine the change in mechanical properties of lead-free solders during thermal cycling or isothermal aging, several of which are by the Suhling group at Auburn University. Kang et al. [54] found that the microhardness of SAC solder joints was decreased thermal cycle testing. This degradation in microhardness was found to increase as the TC conditions (ΔT and frequency) became more severe.

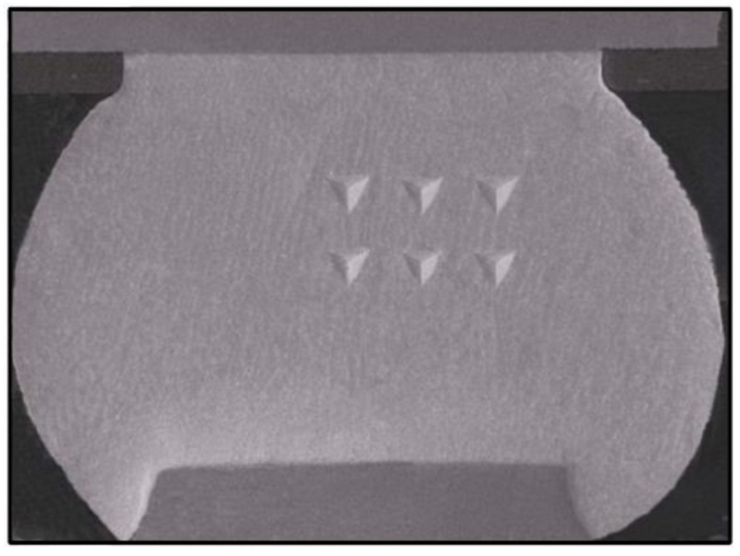


Figure 4.3. A series of Nanoindentations in a SAC solder joint [104].

A number of new studies from the Suhling group [100–104] have found that Nanoindentation results largely confirm the previously observed degradation in SAC solder mechanical properties such as modulus and hardness. These are observed to decrease by ~30-40% over the course of 12 months of aging at 125ºC, which is in line with the results from bulk specimen testing. However, the increases in creep rate observed via Nanoindentation were found to be in the range of 8-50X the as-reflowed

rate. Although a 50-fold increase in creep rate is clearly significant (and deleterious), there increases are far less than those previously observed for bulk samples, which ranged from 200-1000X. Since the Nanoindentation testing occurs within a single b-Sn grain, they surmise that “the lack of the grain boundary sliding creep mechanism in the single grain joints is an important factor in avoiding the extremely large creep rate degradations (up to 10,000X) occurring in larger bulk SAC samples” [104].

4.6.2 Effects of Isothermal Aging on Sn-Ag-Cu Solders: Reliability Data

A number of studies, many of them performed by the Evans group at Auburn University, have demonstrated a reliability problem with the Sn-Ag-Cu (SAC) solders. Namely, the microstructural evolution experienced by the SAC solders during isothermal aging, and the subsequent degradation in mechanical properties, are mirrored by a loss of reliability in a variety of tests, including thermal cycling and vibration tests [13,24,55,91,105–110].

In work involving the Test Vehicle 7 (TV7) at Auburn University, a variety of BGA, CSP, and QFN packages ranging in size between 5mm and 19mm were tested at aging times of up to 24 months and aging temperatures of up to 125°C. The reliability of SAC105, SAC305, and SnPb (control) solders was examined using thermal cycle testing and vibration testing [13,24,55,105–109]. Although the as-reflowed SAC solders were found to outperform SnPb in thermal cycle testing, larger degradations in the characteristic life of both SAC105 and SAC305 packages were observed than for SnPb. The pattern of characteristic life degradation was observed to be very non-linear in the case of the SAC solders, as compared with the SnPb solder – with the SAC solders

experiencing a very fast initial drop-off in reliability that eventually becomes shallower at longer aging times.

Very significant decreases in reliability were observed when compared to the as-reflowed state. For instance, using the 19mm BGA package, at 12-months of aging at 125ºC, SAC305 was found to exhibit a 50% decrease in characteristic life and SAC105 was found to exhibit a 55% decrease in characteristic life [108]. Significant degradations in characteristic life were also observed for the lead-free solders in vibration testing of a modified TV7 board [13]. Figure 4.4, below, shows the degradation in characteristic life values for the 15mm package (CABGA 208) as a function of isothermal aging.

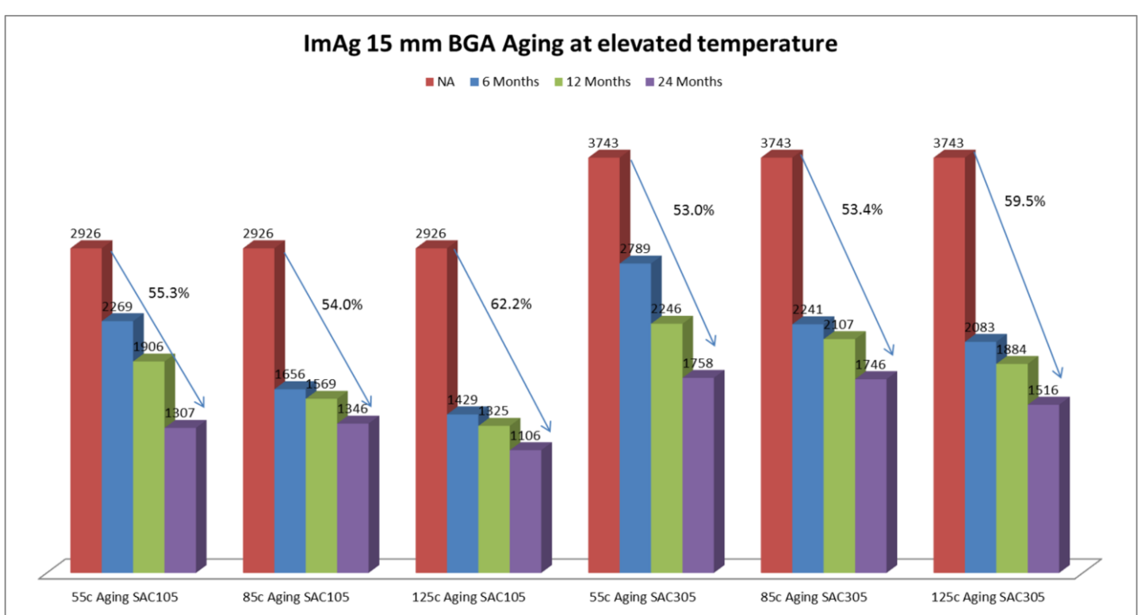


Figure 4.4. TV7 Project: Characteristic Life degradation with aging for CABGA 208.

Wilcox et al. [91] noted that isothermal aging prior to thermal cycle testing produced a measurable reduction in the observed characteristic life values of SAC solder joints while testing a CTBGA 84 CSP. They report that twenty (20) days of aging at 125oC caused a fatigue life reduction of 15% for SAC305 joints [91].

Chiu et al. [110] performed a study involving drop and mechanical testing and found that isothermal aging led to a significant degradation in drop testing performance. They attributed this degradation to the thermally driven formation and coalescence of Kirkendall voids at the solder/Cu-pad interface [110].

4.7 Impact of Current Work

There are a range of operating environments in which the evolution of the microstructure and mechanical properties of Lead-Free solder materials could potentially pose a reliability problem. Although typically thought of as “harsh environment” by electronic manufacturers, many of these applications are critical to our everyday lives. For instance, Lall and Mirza [90] note that the electronics in “underhood” automotive applications “may be subjected to temperatures in the neighborhood of 150°C to 175°C.” Modern automobiles can have up to several hundred electronic controllers, and new uses for computing power – such as lane departure warnings, automated collision avoidance systems, etc. – continue to be implemented and are clearly safety critical. Electronics Reliability is also a major concern in other high-performance markets such as aerospace and military.

The known issues of the Sn-Ag-Cu (SAC) materials in high temperature and high-stress environments have created a significant amount of uncertainty as to what lead-free materials are best suited for such applications. The primary current technique being applied to the problem is via micro-alloying, or “doping.” Micro-alloying involves adding low levels of alternative alloying elements to Sn-rich or SAC-based solder formulations. Currently, a limited number of solders designed for high-temperature

reliability are available on the market, and more are in development. Scientists and engineers in the field are presently in the development of so-called "third generation" lead-free solder alloys, which often involve significant additions of elements such as Bismuth (Bi), Antimony (Sb) and Indium (In) [73]. In instances where acquiring components balled with a high-temperature reliability solder is impractical, one potential avenue is to use a separate formulation of solder in the solder paste (paste doping), to change the overall composition of the resulting solder joints.

Because of the risks and uncertainties involved, a new body of reliability engineering knowledge must be built of for the Sn-Ag-Cu solders based on application-specific process and service parameters. This experiment considers the reliability of a variety of different electronic components and evaluates them on 0.200" printed circuit boards using thermal cycling. Two substrate materials – FR4-06 and Megtron6 – are considered, both with OSP surface finish. The primary solders for package attachment in this experiment are SnPb and SAC305. Two solders designed for high-temperature reliability are also considered, including a Bi-doped SAC material and the six-element alloy Innolot (Sn3.8Ag0.7Cu3Bi1.4Sb0.15Ni).

Chapter 5
Experimental Design and Methods

5.1 Electronic Assemblies and Solder Joints

The semiconductor and packaging industries have been gravitating toward the use of smaller and more reliable packages to meet the growing market demand for hand held electronics. Simultaneously, industry has been moving away from the use of Lead (Pb) due to the increasing awareness of the health and safety concerns surrounding its use.

Current industry standards for ball grid array (BGA) and solder interconnect reliability testing rely mainly on pass/fail electrical continuity functionality test criterion, with limited knowledge of factors contributing towards the failure. A variety of factors affect the reliability of the solder joints used in those electronic components. Chip dimension, component structure, and BGA pad size are some of the factors to be considered, in addition to the principal factor of solder material properties.

Electronic packages are subjected to thermally-induced stress due to power cycling, ambient temperature changes, and a variety of other reasons. The combination of disparate coefficients of thermal expansion (CTEs) and temperature changes can result in excessive stress, leading to weakening of the solder joints and eventual component/package failure. It is therefore important to test the reliability of these packages under such conditions to determine applicable product lifetimes, etc. Such testing is particularly vital in the case of products intended for use in harsh environments. During a Thermal Cycling (TC) test, solder materials are typically subjected to higher temperatures above half of their melting point (i.e. greater than 0.5 in terms of their

homologous temperature), facilitating thermally driven evolution and failure mechanisms.

Both the composition and microstructure of the solder joint will affect its bulk properties. These will determine a joints ability to provide the necessary mechanical and electrical connection and strongly affect the reliability of the joint. Although an initial microstructure will be present following assembly – which will involve one or more soldering steps – this structure will continue to evolve over the lifetime of the joint.

5.2 Test Vehicle Design – TC1-SRJ Test Board

The TC1-SRJ test vehicle was designed by Peter Narbus and manufactured by TTM Technologies (Time-To-Market Interconnect Solutions), Chippewa Falls Division. Overall board dimensions are 173 mm (10 inches) by 254 mm (6.81 inches) with a board thickness of 5 mm (0.2", or 200 mils). When the components are assembled onto the printed circuit board (PCB), each TC1-SRJ printed circuit assembly (PCA) weighs close to a pound (lb), or 0.454 kilograms (kg). To put the size of the assembly into context, a standard sheet of paper is 10" by 6.81", with a thickness of 0.004" or 4 mils. Figure 5.1, below, shows the size comparison of a TC1-SRJ PCA to a sheet of paper.

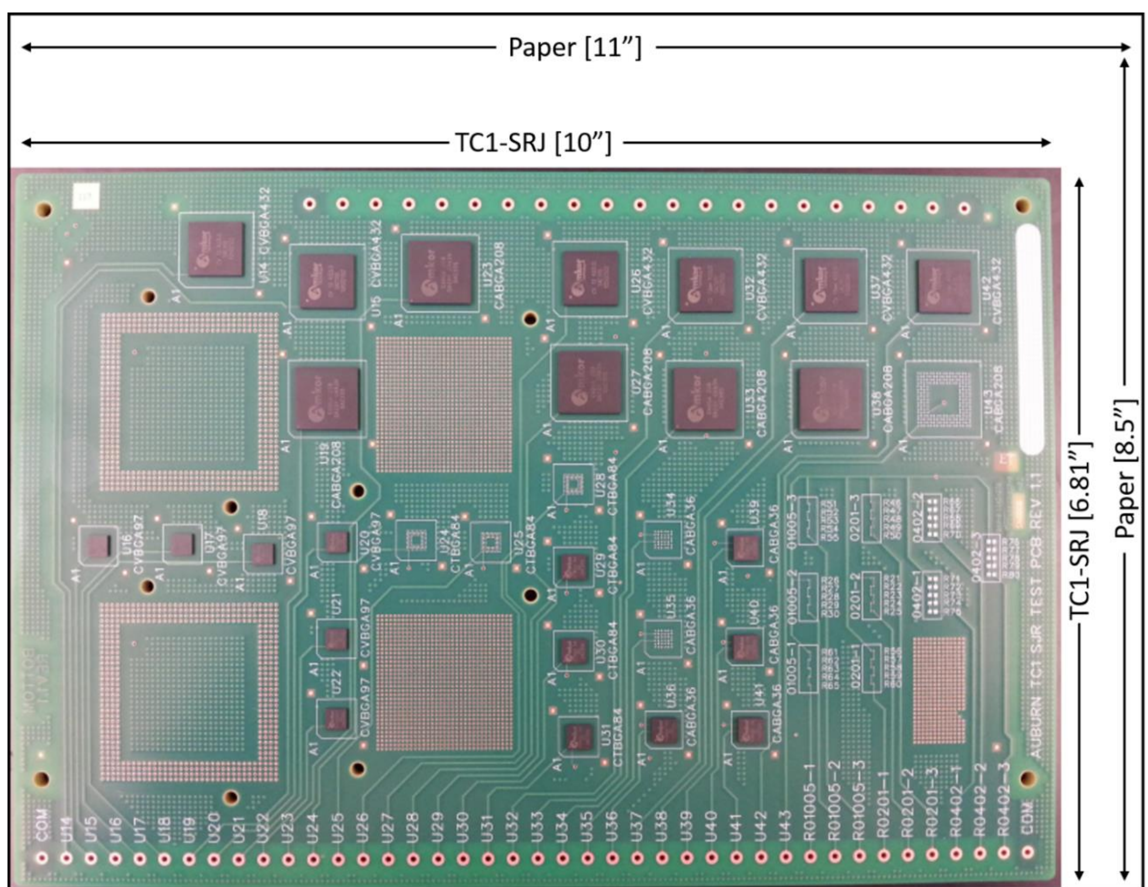


Figure 5.1. Size Comparison: TC1-SRJ vs. Sheet of Paper.

The printed circuit board (PCB) used in the TC1-SRJ test vehicle is a commercial-grade laminate board with 6 Copper (Cu) layers. Two different printed circuit board materials were tested: FR4-06 and Megtron6. The FR4-06 board material used in this experiment was a high-temperature multi-functional glass-epoxy laminate with a glass-transition temperature (T_g) of 170°C, whereas the Megtron6 board material used in this experiment was a high-temperature Polyphenylene Ether blend with a glass-transition temperature (T_g) of 210°C.

Each printed circuit board (PCB) used in the TC1-SRJ test vehicle incorporates 14,607 pins, 3590 through-holes, and 11017 copper pads. The board also includes 12 tool-holes, each of which has a diameter is 3.8 mm and the distance from the edge of

packages/board-features to the center of the holes is at least 7mm. The surface finish for all boards was Organic Solderability Preservative (OSP).

Each printed circuit board has land patterns available for the placement of up to 249 components. Each component land-pattern is electrically connected to one of the through-holes for monitoring, except for the surface mount resistor (SMR) components, which are electrically daisy-chained together in groups of five (5) for readout through a single channel. All components and SMR groups are attached to a common ground channel by way of completing the electrical circuit.

The design pattern used for the top- and bottom-side of the board are different. With each component or surface mount resistor group monitored through on data channel, in total there are 19 channels and one ground on the top-side of the board, and an additional 39 channels on the bottom-side (ground shared). Boards were assembled single-sided, with components on only one side of the board. Two groups were assembled: in one group, components were placed on the 'Top' side of the board; in the second group, components were placed on the 'Bottom' side of the board. The top- and bottom-side assembled boards are shown in Figures 5.2 and 5.3, below.

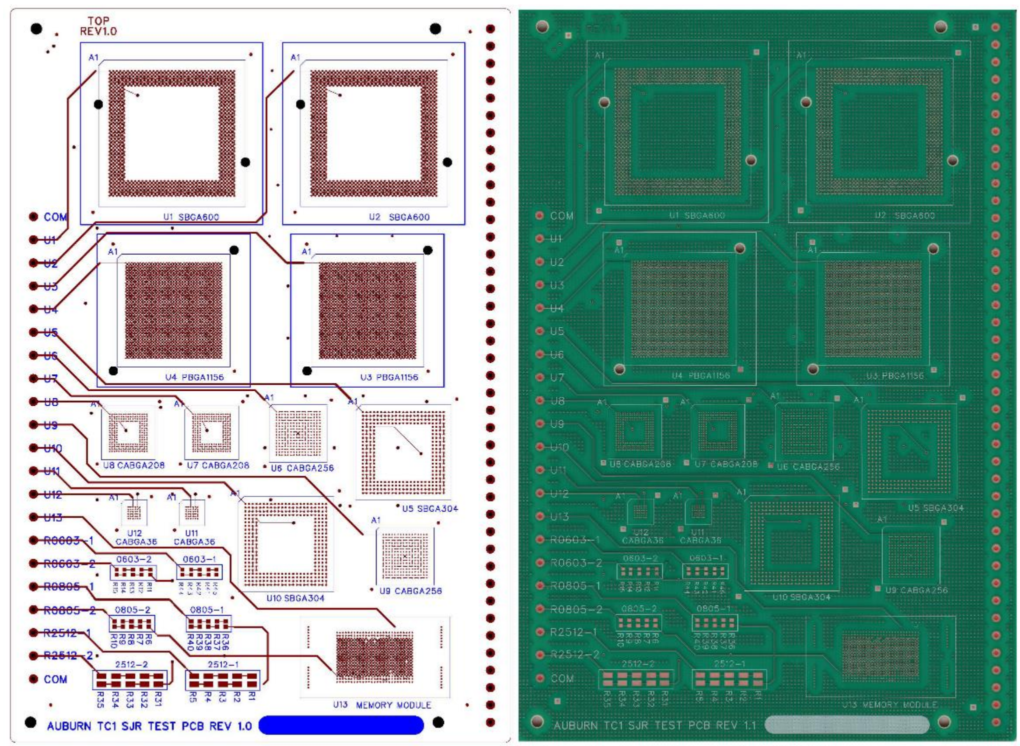


Figure 5.2. TC1-SRJ Test Vehicle: Top-Side (Schematic and Un-assembled PCB).

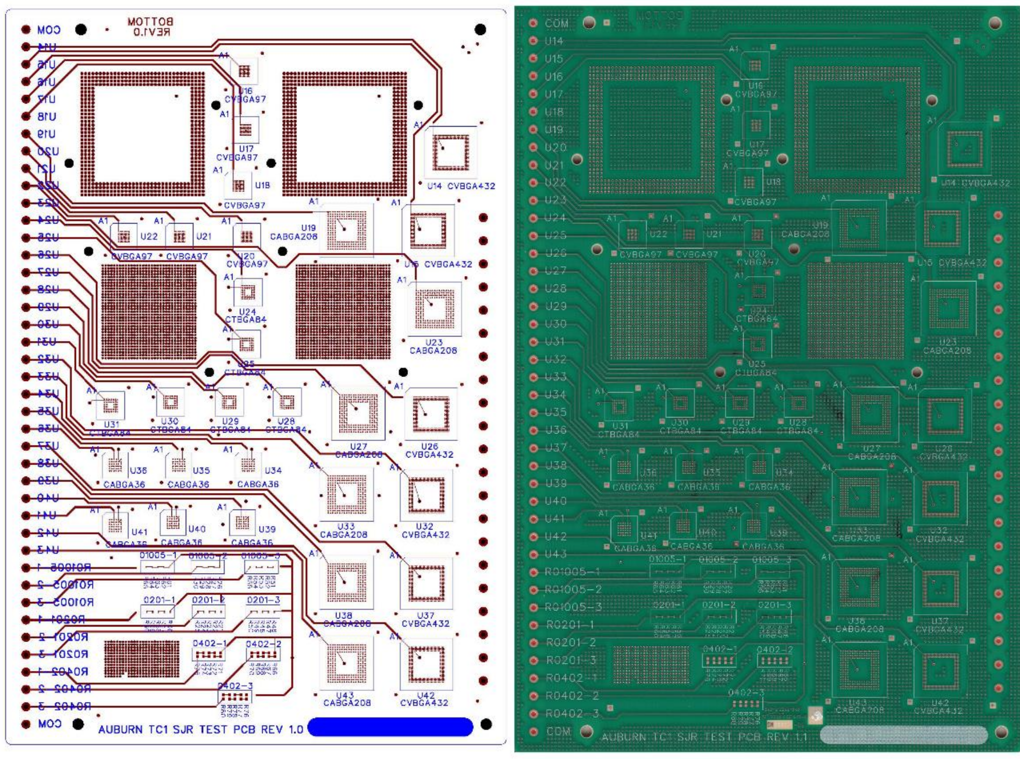


Figure 5.3. TC1-SRJ Test Vehicle: Bottom-Side (Schematic and Un-assembled PCB).

5.3 Test Vehicle: Components and Circuit Board Assemblies (CBAs)

The primary components included in this experiment are plastic Ball Grid Arrays of various size and type, ranging in size from 5mm x 5mm (footprint) to 45mm x 45mm. All components are sourced from Practical Components. These are “dummy die” components (die is non-functioning). Each component is “daisy chained” such that (when assembled) an electrical signal applied to the component’s data channel will pass through each solder joint of the component in series. This allows a single two-wire electrical test to be performed on the component, with every solder joint of the component being checked at the same time. If a single solder joint failure occurs, the immediate result is an open electrical circuit for that component.

The test vehicle incorporates land patterns for 5 mm, 6mm, 13mm, 15mm, 17mm, 31mm, 35mm and 45 mm Ball Grid Array (BGA) packages with solder ball pitch ranging from 0.4 mm to 1.27 mm. Most of the BGA components are plastic over-molded packages, while the 31mm and 45mm packages are Super-BGAs (SBGAs). Several surface mount resistors (SMRs) are also tested. Both the socket for the Memory Module and the SMRs are No-Lead packages, which will give information on the effect of paste-composition in the absence of mixing with solder sphere material.

The Top and Bottom of the test vehicle do not have the same component spots available. The Bottom-Side of the test vehicle is populated with the smaller BGAs and SMRs, while the Top-side of the board is populated with the larger BGAs and SMRs and the Memory Module. The Memory Module consists of a Land Grid Array (LGA) socket attached during the regular assembly process, paired with a Pin Grid Array (PGA) component. The PGA was manually placed into the LGA socket once the circuit board

assemblies had been received and sorted at Auburn University. Only two components appear on both sides of the board: the CABGA 36 (6mm plastic BGA) and the CABGA 208 (15mm plastic BGA).

Boards were assembled single-sided, with components on only one side of the board. Two groups were assembled: in one group, components were placed on the 'Top' side of the board; in the second group, components were placed on the 'Bottom' side of the board.

Three (3) different solder paste materials were used, in combination with four (4) different solder sphere/bump materials and a limited number of land grid arrays (LGA). The three solder pastes that were used are: SnPb, SAC305, and Innolot. The solder sphere materials include these three and an additional SAC-based, Bismuth-doped solder in limited quantity (listed as Reballed-Y in the CBAs). Components on Innolot-paste boards that are listed as "Reballed" are balled with Innolot spheres and provide the "matched" (solder paste + spheres) data. The SAC305 paste and the Innolot paste were provided by Cookson while the SnPb eutectic paste was sourced from Kester. Type 4 paste was used.

Several different circuit board assemblies were used based on the solder paste composition, board material, and – in some cases – inclusion of Reballed components of specific solder sphere composition in order to produce the combinations appropriate for subsequent testing. The top- and bottom-side Circuit Board Assemblies (CBAs) are shown in Tables 5.1 and 5.2, below.

Table 5.1. Top-Side CBAs.

Top-Side			Solder Paste		SAC		SAC-y		SAC-M6		Innolot		SnPb
			Design		T1		T3		T4		T5		T2
			FR-406		200		100		0		90		150
			Meg 6		0		0		60		0		60
Reference	Component	Pitch	Dimension	Ball Alloy		Ball Alloy		Ball Alloy		Ball Alloy		Ball Alloy	
U1	SBGA 600	1.27mm	45mm	105	0	105	0	305	1	105	0	SnPb	1
U2	SBGA 600	1.27mm	45mm	305	1	305	1	305	1	305	1	SnPb	1
U3	PBGA 1156	1.00mm	35mm	105	1	105	1	305	1	105	1	SnPb	1
U4	PBGA 1156	1.00mm	35mm	305	1	305	1	305	1	305	1	SnPb	1
U5	SBGA 304	1.27mm	31mm	105	0	105	0	305	1	105	0	SnPb	1
U6	CABGA 256	1.0mm	17mm	105	1	105	1	305	1	105	1	SnPb	1
U7	CABGA 208	0.8mm	15mm	105	1	105	0	305	1	105	1	SnPb	1
U8	CABGA 208	0.8mm	15mm	305	1	Reballed-Y	1	305	1	105	1	SnPb	1
U9	CABGA 256	1.0mm	17mm	305	1	305	1	305	1	305	1	SnPb	1
U10	SBGA 304	1.27mm	31mm	305	1	305	0	305	1	305	1	SnPb	1
U11	CABGA 36	0.8mm	6mm	105	0	105	0	305	1	Innolot	1	SnPb	1
U12	CABGA 36	0.8mm	6mm	305	1	Reballed-Y	1	305	0	305	1	SnPb	1
U13	Memory Module				1		1		1		1		0
R0603-1	0603 SMR		0.6X0.3mm	100%Sn	1	100%Sn	1	100%Sn	1	100%Sn	1	100%Sn	1
R0603-2	0603 SMR		0.6X0.3mm	100%Sn	1	100%Sn	1	100%Sn	1	100%Sn	1	100%Sn	1
R0805-1	0805 SMR		2.0x1.2mm	100%Sn	1	100%Sn	1	100%Sn	1	100%Sn	1	100%Sn	1
R0805-2	0805 SMR		2.0x1.2mm	100%Sn	1	100%Sn	1	100%Sn	1	100%Sn	1	100%Sn	1
R2512-1	1206 SMR		3.2x1.6mm	100%Sn	1	100%Sn	1	100%Sn	1	100%Sn	1	100%Sn	1
R2512-2	1210 SMR		3.2x2.6mm	100%Sn	1	100%Sn	1	100%Sn	1	100%Sn	1	100%Sn	1

Table 4.2. Bottom-Side CBAs.

Bottom-side			Solder Paste		SAC		SAC-M6		Innolot		SnPb
			Design		B1		B1-1		B3		B2
			FR-406		100		0		30		50
			Meg 6		0		20		0		20
Reference	Component	Pitch	Dimension	Ball Alloy		Ball Alloy		Ball Alloy		Ball Alloy	
U14	CVBGA 432	0.4mm	13mm	105	1	105	1	105	1	SnPb	1
U15	CVBGA 432	0.4mm	13mm	305	1	305	1	305	1	SnPb	1
U16	CVBGA 97	0.4mm	5mm	105	1	105	1	105	1	SnPb	1
U17	CVBGA 97	0.4mm	5mm	305	1	305	1	305	1	SnPb	1
U18	CVBGA 97	0.4mm	5mm	105	1	105	1	105	1	SnPb	1
U19	CABGA 208	0.8mm	15 mm	105	1	105	1	105	1	SnPb	1
U20	CVBGA 97	0.4mm	5mm	105	1	105	1	105	1	SnPb	1
U21	CVBGA 97	0.4mm	5mm	305	1	305	1	305	1	SnPb	1
U22	CVBGA 97	0.4mm	5mm	305	1	305	1	305	1	SnPb	1
U23	CABGA 208	0.8mm	15 mm	305	1	305	1	305	1	SnPb	1
U24	CTBGA 84	0.5mm	6mm	nil	0	nil	0	nil	0	SnPb	1
U25	CTBGA 84	0.5mm	6mm	305	1	305	1	305	1	SnPb	1
U26	CVBGA 432	0.4mm	13mm	105	0	105	0	105	1	SnPb	1
U27	CABGA 208	0.8mm	15 mm	Reballed Y	1	105	1	Reballed	1	SnPb	1
U28	CTBGA 84	0.5mm	6mm	nil	0	nil	0	nil	0	SnPb	1
U29	CTBGA 84	0.5mm	6mm	305	1	305	1	305	1	SnPb	1
U30	CTBGA 84	0.5mm	6mm	nil	0	nil	0	nil	1	SnPb	1
U31	CTBGA 84	0.5mm	6mm	305	1	305	1	305	1	SnPb	1
U32	CVBGA 432	0.4mm	13mm	305	1	305	1	305	1	SnPb	1
U33	CABGA 208	0.8mm	15 mm	Reballed Y	0	305	0	Reballed	1	SnPb	1
U34	CABGA 36	0.8mm	6mm	105	1	105	1	105	1	SnPb	1
U35	CABGA 36	0.8mm	6mm	305	1	305	1	305	1	SnPb	1
U36	CABGA 36	0.8mm	6mm	Reballed Y	1	305	1	Reballed	1	SnPb	1
U37	CVBGA 432	0.4mm	13mm	105	1	105	1	105	1	SnPb	1
U38	CABGA 208	0.8mm	15 mm	105	1	105	1	105	1	SnPb	1
U39	CABGA 36	0.8mm	6mm	105	1	105	1	105	1	SnPb	1
U40	CABGA 36	0.8mm	6mm	305	1	305	1	305	1	SnPb	1
U41	CABGA 36	0.8mm	6mm	Reballed Y	0	305	0	Reballed	1	SnPb	1
U42	CVBGA 432	0.4mm	13mm	305	1	305	1	305	1	SnPb	1
U43	CABGA 208	0.8mm	15 mm	305	1	305	1	305	1	SnPb	1
R01005-1	01005 SMR		0.4X0.2mm	100%Sn	1	100%Sn	1	100%Sn	1	100%Sn	1
R01005-2	01005 SMR		0.4X0.2mm	100%Sn	1	100%Sn	1	100%Sn	1	100%Sn	1
R01005-3	01005 SMR		0.4X0.2mm	100%Sn	1	100%Sn	1	100%Sn	1	100%Sn	1
R0201-1	0201 SMR		0.6x0.3mm	100%Sn	1	100%Sn	1	100%Sn	1	100%Sn	1
R0201-2	0201 SMR		0.6x0.3mm	100%Sn	1	100%Sn	1	100%Sn	1	100%Sn	1
R0201-3	0201 SMR		0.6x0.3mm	100%Sn	1	100%Sn	1	100%Sn	1	100%Sn	1
R0402-1	0402 SMR		1.0X0.5mm	100%Sn	1	100%Sn	1	100%Sn	1	100%Sn	1
R0402-2	0402 SMR		1.0X0.5mm	100%Sn	1	100%Sn	1	100%Sn	1	100%Sn	1
R0402-3	0402 SMR		1.0X0.5mm	100%Sn	1	100%Sn	1	100%Sn	1	100%Sn	1

5.4 Test Plan

A total of 910 boards were built: 750 boards of FR4-06 material, and 160 boards of Megtron6 material. 30 boards from the FR4-06 lot were used exclusively for setup during assembly while the remaining 720 FR4-06 and 160 Megtron6 were used in active testing. (Note that these are all nominal numbers.)

There are 3 Top-Side printed circuit assemblies for every 1 Bottom-Side assembly. This difference is because there are 2 of each component on a Top-Side assembly, versus 6 of each component on a Bottom-Side assembly.

Isothermal storage at high temperature was used to accelerate the aging of the assemblies. Aging Temperatures are 25ºC, 50ºC, and 75ºC. Aging durations are for 0-months (No Aging), 6-months, 12-months, and 24-months. Table 4.3 shows the Test Plan for this experiment (raw numbers), and Figure 5.4 shows highlights of some of the important subgroups (nominal numbers).

Table 4.3. Test Plan.

		Top Side		Bottom Side		Total	Aging
FR 406	SAC	30 [30,0,0]	74 [74,0,0]	10 [10,0,0]	25 [25,0,0]	99[99,0,0]	No Aging
	SnPb	14 [14,0,0]		5 [5,0,0]			
	Innolot	30 [30,0,0]		10 [10,0,0]			
Meg 6	SAC	15 [15,0,0]	30 [30,0,0]	5 [5,0,0]	10 [10,0,0]	40 [40,0,0]	
	SnPb	15 [15,0,0]		5 [5,0,0]			
FR 406	SAC	90 [30,30,30]	162 [44,44,74]	30 [10,10,10]	55 [15,15,25]	217 [59,59,99]	6 months
	SnPb	42 [14,14,14]		15 [5,5,5]			
	Innolot	30 [0,0,30]		10 [0,0,10]			
Meg 6	SAC	15 [0,0,15]	30 [0,0,30]	5 [0,0,5]	9 [0,0,9]	39 [0,0,39]	
	SnPb	15 [0,0,15]		4 [0,0,4]			
FR 406	SAC	90 [30,30,30]	132 [44,44,44]	30 [10,10,10]	45 [15,15,15]	177 [59,59,59]	12 months
	SnPb	42 [14,14,14]		15 [5,5,5]			
	Innolot	0		0			
Meg 6	SAC	15 [0,0,15]	30 [0,0,30]	5 [0,0,5]	10 [0,0,10]	40 [0,0,40]	
	SnPb	15 [0,0,15]		5 [0,0,5]			
FR 406	SAC	90 [30,30,30]	162 [44,44,74]	30 [10,10,10]	55 [15,15,25]	217 [59,59,99]	24 months
	SnPb	42 [14,14,14]		15 [5,5,5]			
	Innolot	30 [0,0,30]		10 [0,0,10]			
Meg 6	SAC	15 [0,0,15]	30 [0,0,30]	5 [0,0,5]	10 [0,0,10]	40 [0,0,40]	
	SnPb	15 [0,0,15]		5 [0,0,5]			
		Total Top Side =	650 [236,132,282]	Total Bottom Side =	219 [80,45,94]	Total Boards = 869[316,177,376]	

Number of Total Board [# aged at 25C, # aged at 50C, # aged at 75C]

	FR 406	Meg 6	Total
No Aging	100	40	140
6 months	220	40	260
12 months	180	40	220
24 months	220	40	260
Total	720	160	880

		SAC	SnPb	Innolot
FR 406	Top	300	150	90
FR 406	Bottom	100	50	30
Meg 6	Top	60	60	Nil
Meg 6	Bottom	20	20	Nil

Total # of Boards	
FR 406	720
Meg 6	160
Total	880

	FR 406	Meg 6
Top	540	120
Bottom	180	40
Total	720	160

Figure 5.4. Summary of some important sub-groups from the Test Matrix.

There are a different number of TC1-SRJ test vehicles in each aging groups. The nominal number of boards in each aging-time group is as follows:

- No Aging Group: 140 Test Vehicles
- 6-Month Aging Group: 260 Test Vehicles
- 12-Month Aging Group: 220 Test Vehicles
- 24-Month Aging Group: 260 Test Vehicles

There are two reasons for the differences in board-count between these groups. First, the No Aging Group has fewer boards because it does not require duplicate boards for isothermal aging at 25°C, 50°C, and 75°C. Consequently, the No Aging group is by far the smallest group in the test. Second, not all sub-groups are found in each aging-time group. In particular, several sub-groups were added to the Test Matrix in the latter stages of planning, and only as funding allowed:

- Innolot-paste boards: Innolot paste is only found on FR4-06 boards and these boards are only included in the 75°C aging temperature groups. Additionally, there are no Innolot-paste boards incorporated into the 12-Month aging group.
- Megtron6 substrate boards: Megtron6 boards are only included in the 75°C aging temperature groups. Because of the cost premium for Megtron6 printed circuit boards – quite substantial at the time of purchasing – there are also fewer Megtron6 boards per aging-time group than equivalent FR4-06 boards.

5.5 Surface Mount Assembly

The TC1-SRJ test vehicle PCBs were assembled by STI Electronics Inc. at their home location in Madison, Alabama. Board Assembly was done in two parts. Bottom boards were assembled from Dec. 17-19, 2012 and Top boards were assembled from Jan. 22-28, 2013.

Figure 5.5. Speedline Technologies MPM Momentum.

The screen printing machine used was a Speedline Technologies MPM Momentum (right). The stencil thicknesses used were:

- Bottom-Side Assemblies = 3 mil stencil
- Top-Side Assemblies = 5 mil stencil

Bottom-side boards were double-printed in order to get adequate solder volume on the small-pitch components. Otherwise, print parameters where held constant for all assemblies.

Two pick-and-place machines were used for the Phase II assembly: the Juki KE-2080L (below, left) and Juki FX3 (below, right).

Figure 5.6. Juki KE-2080L (left) and Juki JX3 (right) pick-and-place machines.

Solder reflow was done using a Heller 1913 MKIII reflow oven (shown below). Two different reflow profiles were used: one for the SnPb boards and one for the Lead-Free boards. The actual thermal profiles experienced by the board also differ slightly between top-side and bottom-side reflow. The thermal profiles were selected on the basis of attempting to meet (solder paste) manufacturer recommendations while adjusting based on the realities of balancing time-above-liquidus, peak reflow temperature, etc. for a board of such high thermal mass.

Figure 5.7. Heller a1913 MKIII Reflow Oven.

To get accurate thermal readings, a test board was fitted with three thermocouples as shown on right and passed through the reflow oven while attached to a thermal readout and recording device [EDC M.O.L.E. Thermal Profiler]. The oven temperature zones and pass-through speed were

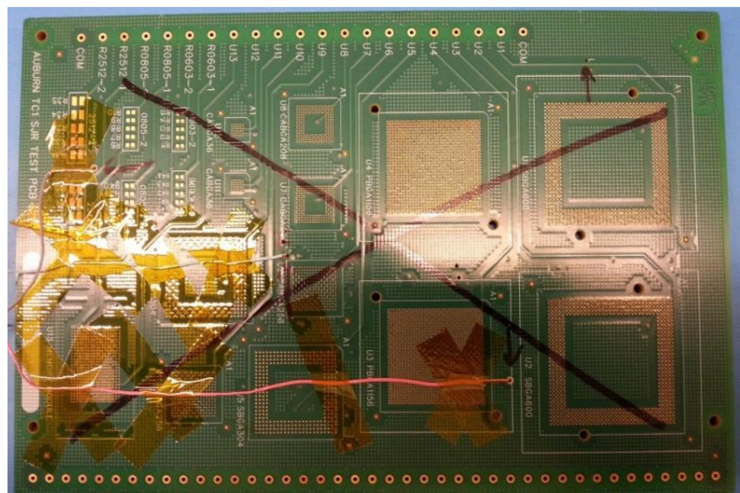


Figure 5.8. Setup Board used for Thermal Profiling of the Reflow Oven.

adjusted iteratively until a feasible reflow profile was obtained. The reflow profiles shown below are the ones used for all test vehicles.

Because of the large thermal mass of the TC1-SRJ test vehicle, the thermal profile used for reflow had to be adjusted very significantly, removing the typical soak zone. Instead, the temperature is ramped aggressively to reach the peak temperature. Aggressive cooling was also needed to limit the time-above liquidus. Two different reflow profiles were for both the Top-Side and Bottom-Side assemblies: one for the Tin-Lead eutectic solder paste boards and one for the Lead-Free solder paste boards (SAC305 and Innolot). Figures 5.9-5.12 show the reflow profiles used during assembly of the TC1-SRJ test vehicles.

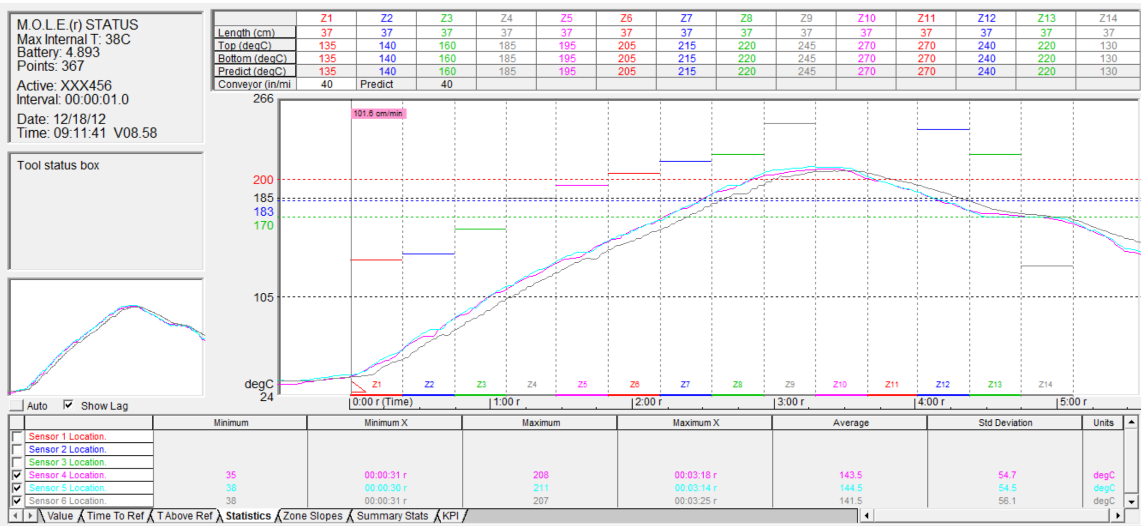


Figure 5.9. SnPb Reflow Profile, Bottom-Side.

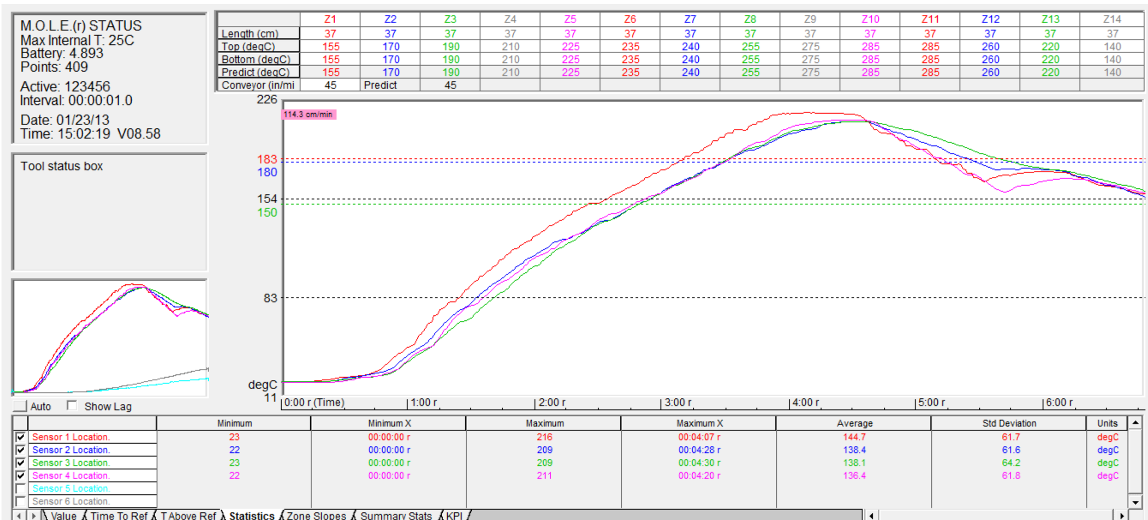


Figure 5.10. SnPb Reflow Profile, Top-Side.

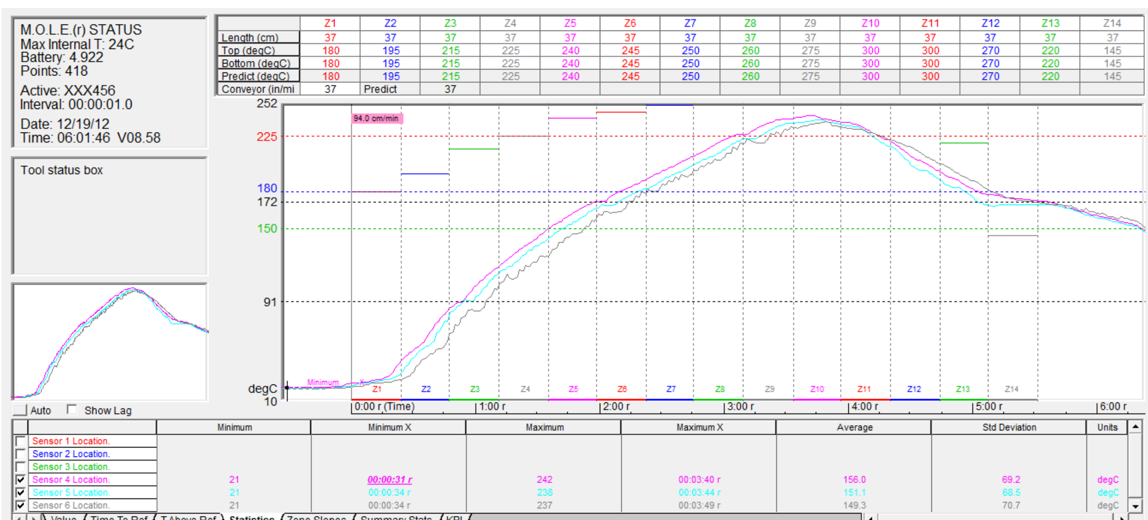


Figure 5.11. Lead-Free Reflow Profile, Bottom-Side.

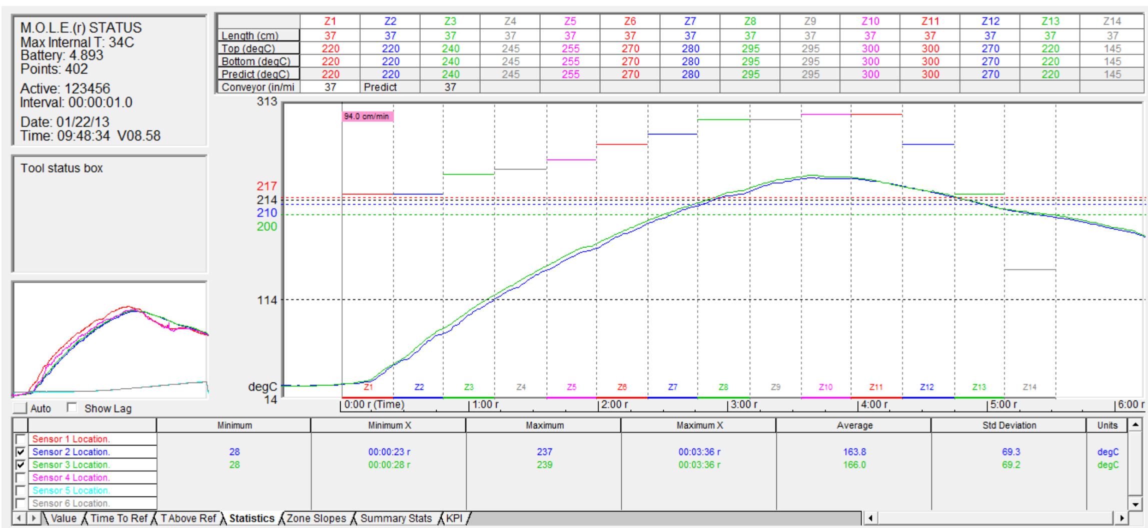


Figure 5.12. Lead-Free Reflow Profile, Top-Side.

Setup boards were used for each material, top- and bottom-side, to verify paste print and reflow prior to beginning the production run for that material. (Only FR4-06 boards were used for setup.) Print alignment, paste coverage, and solder volume were checked and corrective steps were taken as necessary (i.e. minor alignment corrections) before running the corresponding set of test boards. Post-reflow wetting was also verified.

A number of quality assurance steps were taken. The resistance of each daisy-chained circuit component was checked by hand following reflow in order to eliminate them from inclusion in further testing. Boards were also optically inspected, and transmission X-ray tomography analysis was used to determine typical solder joint quality following reflow. In one instance, several components on one of the setup boards were sacrificed in a 'pry test' to assure the mechanical strength of the solder joints as reflowed.

Overall build quality was found to be very good. One board was 'rubbed,' dislocating several components (this board was removed from testing). Some problems

were found with the SBGA 600 components, which is prone to lifting at the corners during reflow, resulting in some head-in-pillow defects.

Two components required additional, post-assembly processing. The Memory Module consists of a Land Grid Array (LGA) socket attached during the regular assembly process, paired with a Pin Grid Array (PGA) component. The PGA was manually placed into the LGA socket once the circuit board assemblies had been received and sorted at Auburn University. Additionally, the heat sinks for the 45mm and 35mm components were added by hand.

5.6 Experimental Methods

Isothermal storage at high temperature was used to accelerate the aging of the assemblies. Aging Temperatures are 25°C, 50°C, and 75°C. Aging durations are for 0-months (No Aging), 6-months, 12-months, and 24-months.

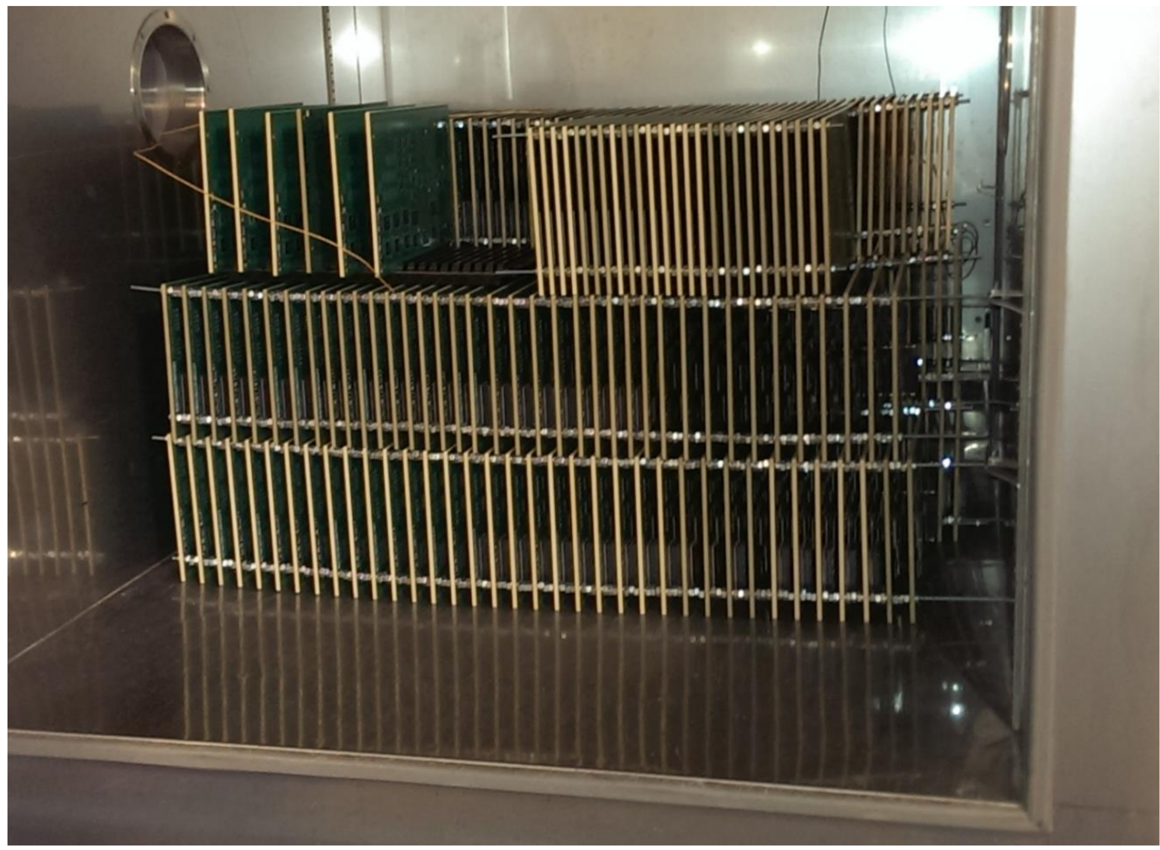


Figure 5.13. TC1-SRJ Assemblies being stacked for Isothermal Aging.

5.6.1 Experimental Methods: Thermal Cycle Test Parameters and Equipment

Following isothermal aging, the assemblies were subjected to a (modified) JEDEC JESD22-A104-B standard high-and-low temperature test in a single-zone environmental chamber to assess the solder joint performance. Thermal cycles had dwell temperatures of -40°C to +125°C. A ramp rate of 15℃ per minute is a stipulated condition in the JEDEC JESD22. However, depending on the thermal capacity, an appropriate condition in the range of 10ºC to 15℃ can be selected. Due to equipment limitations, for this test a ramp rate of 10℃ per minute was selected for the single zone chamber. Therefore, the thermal profile was specified to have 45-minute Ramps with 15-minute Dwells for an overall cycle time of 120 minutes. Each test group was subjected to

3000 thermal cycles. Figure 5.14, below, shows the theoretical (left) and experimental (right) thermal profile for the No Aging group.

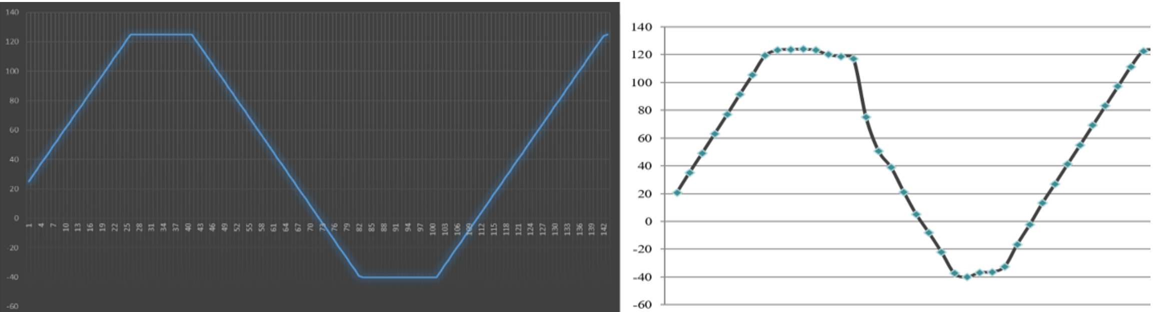


Figure 5.14. TC1-SRJ Thermal Profile, Theoretical (left) vs Experimental (right).

Several different thermal cycle chambers were needed in order to run the TC1-SRJ thermal cycling test. All of the thermal chambers are single-zone, water-cooled machines employing a cascade-type refrigeration system. All of the chambers used for thermal cycling were 16 ft^3 chambers. Figure 5.15, below, shows the two types of thermal chambers used in this test.

Figure 5.15. Thermotron, 16 cft (left) and ETC16 (right) Thermal Cycling Chambers.

The Thermal Cycle Chambers used are listed below in Table 5.4. Each chamber has a limited number of test vehicles that if can cycle at one time. Typically, and for this test, this limit is based on the chamber's ability to cool from the high dwell temperature down to the low dwell temperature quickly enough. Based on the limits of the available thermal cycle chambers, the two largest aging groups (6-Month and 24-Month) needed to be divided into two groups for cycling in separate chambers. In these cases, the boards within each sub-group (based on substrate, solder paste, etc.) were pro-rated such that the percentage of boards from each subgroup was roughly the same in both chambers.

Table 5.4. Thermal Cycle Chambers used for testing the TC1-SRJ test vehicle.

Aging Group	Designation	Chamber Name	Chamber Details
No Aging	0A	Oregon	Blue M ETC16
6-Month Aging	6A	Washington	Blue M ETC16
	6B	Alabama	Thermotron 16 ft^3
12-Month Aging	12A	Oregon	Blue M ETC16
24-Month Aging	24B	Washington	Blue M ETC16
	24A	Tennessee	Blue M ETC16

5.6.1 Experimental Methods: The Effects of Test Magnitude

The TC1-SRJ project provided a significant challenge in terms of the amount of monitoring that needed to be done. As previously noted, a total of 910 printed circuit boards were built: 30 boards were used exclusively for setup during assembly while the remaining 880 boards were used in active testing. (Note that these are all nominal numbers.) With each printed circuit assembly weighing close to 1 lb., the test vehicles alone weigh perhaps 850 lbs. Figure 5.16, below, shows TC1-SRJ test vehicles being organized after arriving at Auburn University.

Figure 5.16. Several hundred TC1-SRJ boards being sorted at Auburn University.

In addition to the simple logistical problems of running such a large test, the scale of the test created a significant challenge in terms of the electrical monitoring that needed to be accomplished. With up to 20 wires needed per Top-Side printed circuit assembly and up to 40 wires needed per Bottom-Side PCA (including grounding wires), on average, up to 25 wires are needed per PCA. (There are 3 Top-Side assemblies for every 1 Bottom-Side assembly.) With approximately 880 printed circuit assemblies to test, a back-of-the-envelope calculation yields a need for up to 22,000 wires. (Not including other wires needed elsewhere in the monitoring system.) With each wire requiring a length of 4-5 feet, that corresponds to 88,000-110,000 feet of temperature-resistant wire.

Each of these wires needed to be cut to length, striped, pre-tinned, crimped, and inserted into a 10-pin connector (for connection to the interface boards). The wires also needed to be individually hand-soldered to the TC1-SRJ test vehicles. The 10-pin

connectors also needed to be labeled and tracked with their respective test vehicles in order to track each data channel accurately in the monitoring system.

Previous thermal cycling tests at Auburn University have used the same Keithley equipment as the current test, but employed an older LabVIEW program developed for CAVE3 called "MarkDano" after its developer. In addition, an older interface board (IB-3) was used to connect the wires from the test boards to the 96-pin ribbon cables used by the Keithley 7002 switching system. Each IB-3 interface board allows monitoring of 40 data channels and takes up 1 of 10 cards installed in the Keithley 7002 mainframe. Therefore, this system could only test 400 channels using one (1) switching system, one (1) multi-meter, and ten (10) IB-3 interface boards.

The smallest test group in the TC1-SRJ test is the No Aging Group, with 140 test vehicles. With an average of 25 wires per test vehicle (upper limit), that corresponds to 3,500 wires that need monitoring for even the smallest test group. Monitoring the TC1-SRJ No Aging group with the old monitoring setup would have required nine (9) Keithley 7002 switching systems, nine (9) Keithley 2001 Digital Multi-Meters, and eighty-eight (88) IB-3 interface boards. Due to equipment and space limitations, this older system was not sufficient to run the TC1-SRJ project.

Therefore, a new monitoring system was developed based on a ground-switching concept. A diode-isolation model was proposed by Dr. Wayne Johnson to Dr. John Evans. New interface board designs were created by Thomas Sanders using the FreePCB CAD program. Two new interface boards were required. The IB-4 interface board is capable of servicing up to 400 data channels, and attaches to a card in the Keithley 7002

switching system using 96-pin connector and ribbon cable (top of board in Figure 5.17, below).

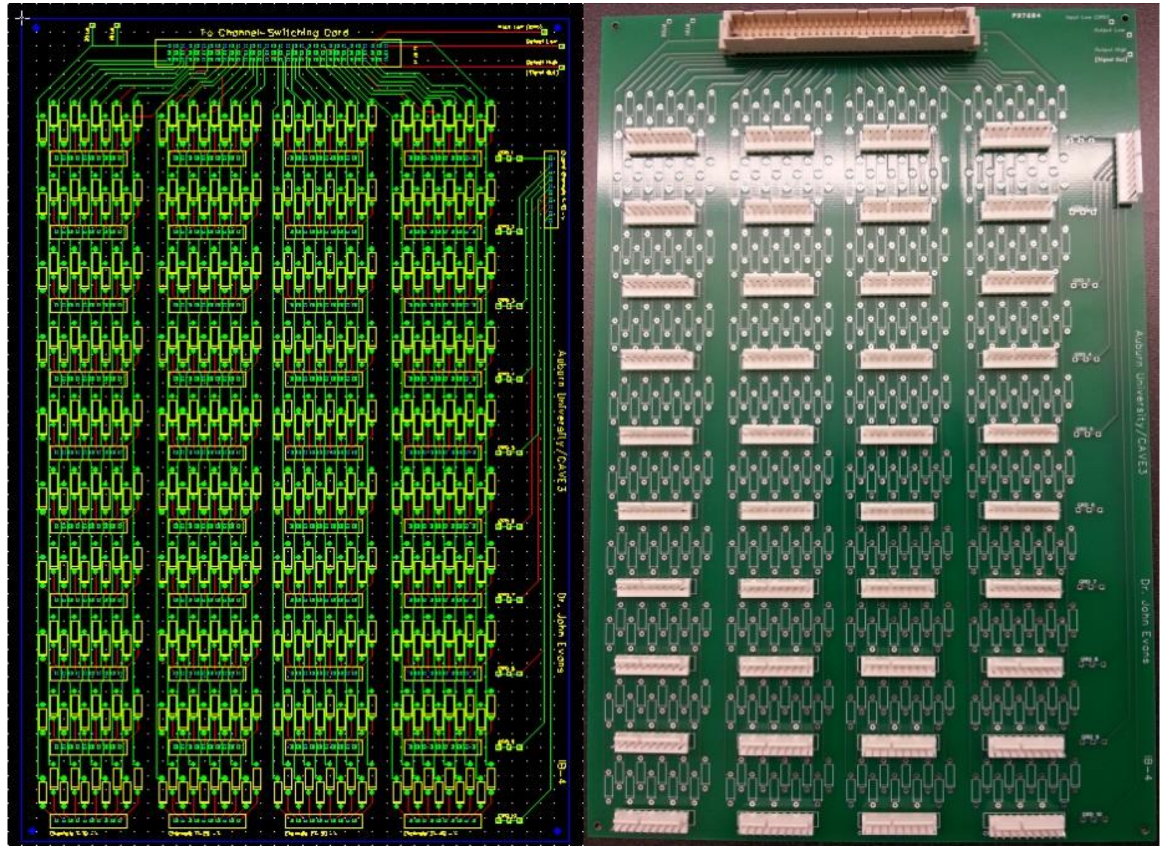


Figure 5.17. IB-4 Interface Board (Schematic and PCA).

In the new monitoring setup, up to nine (9) IB-4 interface boards can be connected to cards 1-9 of the Keithley switching system. However, a separate interface board is needed to facilitate the ground switching system. This “ground interface board” (GRD-IB-1) is shown below in Figure 5.18. The ground interface board is connected to card 10 of the Keithley switching system. In order to prevent shorting through the switching system, certain wires must be cut in this switching system card, which would normally connect it to the “analog backplane” of the Keithley 7002. Rather than 400 channels, the new monitoring system can monitor up to 3600 channels using a using one

(1) Keithley switching system and one (1) digital multi-meter. (This requires nine (9) IB-4 interface boards and one (1) GRD-IB-1 ground interface board.)

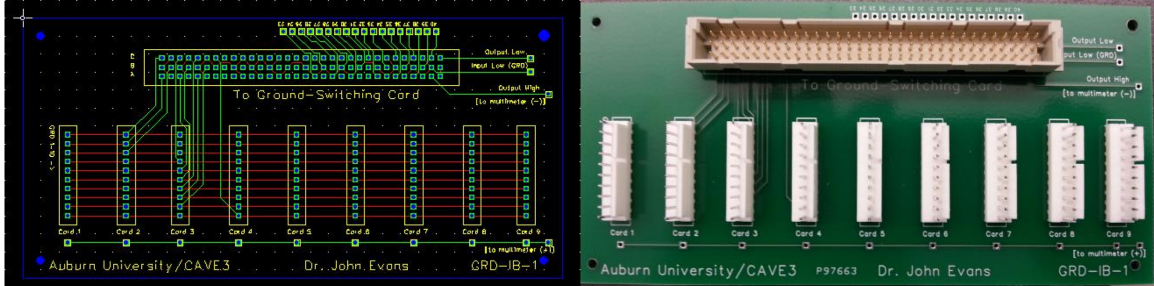


Figure 5.18. GRD-IB-1 Ground Interface Board (Schematic and PCA).

In addition to the hardware changes necessitated by the unprecedented scale of the TC1-SRJ test, new software needed to be developed to facilitate the new ground-switching approach. An initial LabVIEW program was coded by Dr. Colin Stevens (then a graduate student in Electrical Engineering at Auburn University), who also aided in the initial system deployment. This software was later replaced by an improved LabVIEW program written by Thomas Sanders. The new software allows for automated data logging, improved data formatting, temperature tracking and graphing, an improved user interface, the addition of various debugging tools for setting up the monitoring system, and much more. Data is exported by the software to MS Excel files for logging and archiving. The new LabVIEW program is known as the “IB-4 Scanning Protocol.” Figures 5.19 and 5.20, below, show screenshots of the new LabVIEW monitoring program.

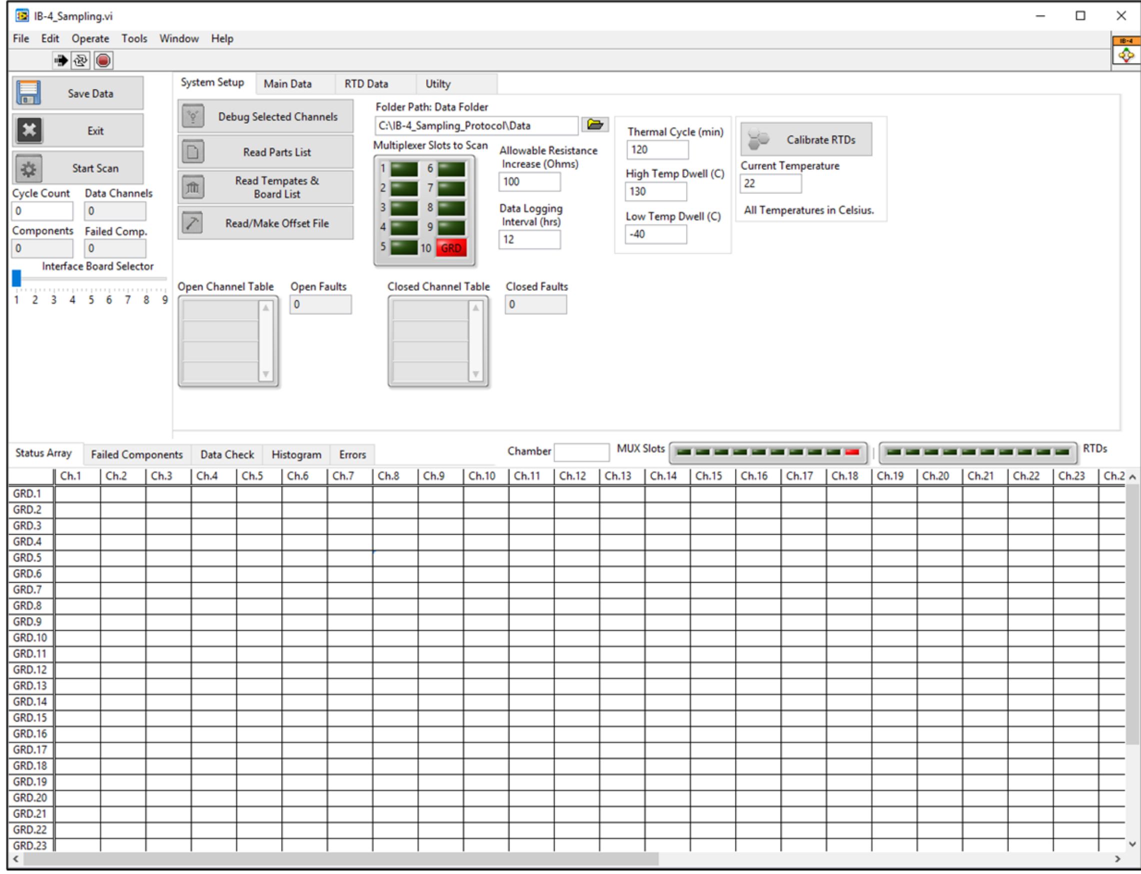


Figure 5.19. Setup Page of IB-4 Sampling Program.

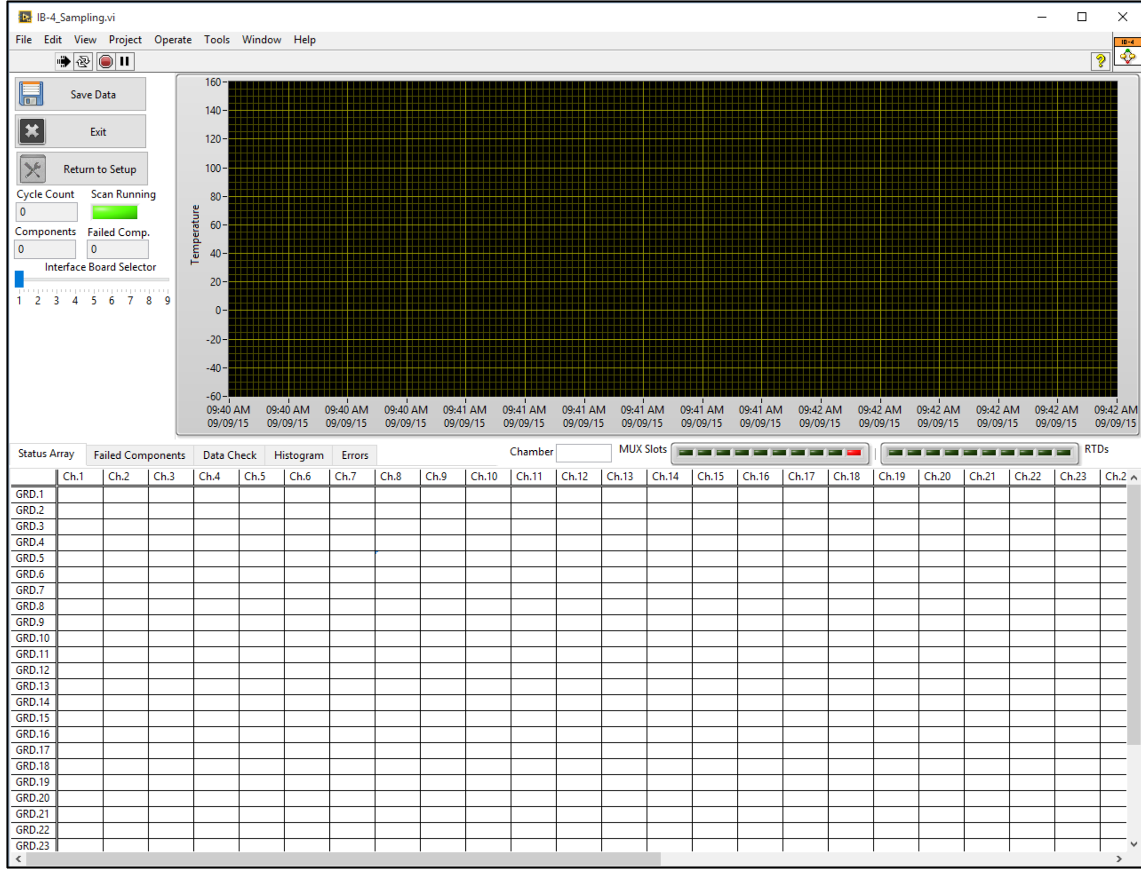


Figure 5.20. Scanning Page of IB-4 Sampling Program.

5.6.2 Experimental Methods: Data Acquisition and Monitoring Equipment

The electrical components for this experiment were “daisy-chained” for electrical continuity testing and in-situ monitoring during the thermal cycling (TC) test. These are “dummy die” components (die is non-functioning). The electrical resistance for each component was independently monitored during the test.

Figure 5.21, below, shows the daisy chaining conceptually. The daisy chaining is done such that when the components are assembled to the printed circuit board, an electrical signal applied to a component’s data channel will pass through each solder joint of the component in series. This allows a single two-wire electrical test to be performed on the component, with every solder joint of the component being checked at the same

time. If a single solder joint failure occurs, the immediate result is an open electrical circuit for that component.

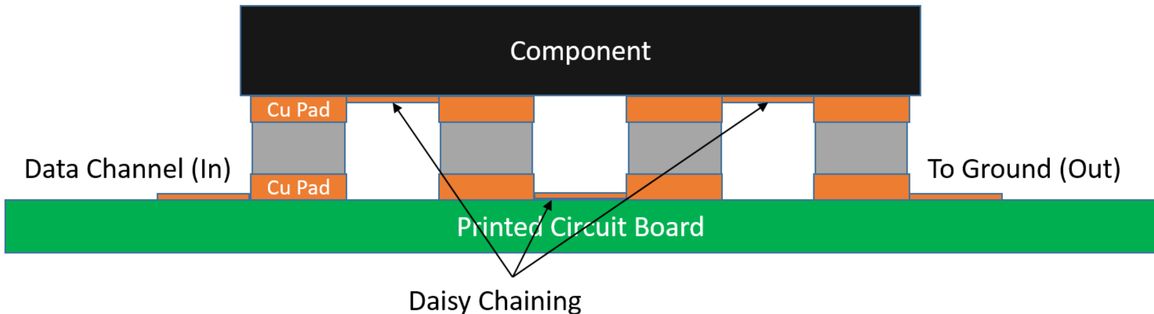


Figure 5.21. Electrical Daisy Chaining for continuity testing.

During thermal cycling, the test boards are mounted vertically in the cycling chamber using heat-resistant plastic dividers. Temperature resistant wires were hand-soldered to each active data channel and ground channel for all test boards, and the wiring passed through the independent access ports of the thermal cycling chamber to a LabVIEW-based monitoring system. Figure 5.22 shows approximately 50 (out of 140) of the No Aging TC1-SRJ test vehicles stacked in a thermal cycle chamber (left) and the corresponding test wiring exiting the chamber aperture (right).

Figure 5.22. TC1-SRJ boards stacked (left) and corresponding wiring (right).

The monitoring system utilizes Keithley 7002 switching systems and Keithley 2000 and 2001 digital multi-meters (DMMs), as well as the two custom interface boards shown in the previous section. Data transfers and equipment commands are sent over the GPIB bus system using the NI 488.2 software architecture, with commands to the Keithley equipment being sent in SCPI. An additional Trigger Link cable is used to synchronize the actions of the switching system and digital multi-meter. Figure 5.23 shows the monitoring system equipment (about one-half of the monitoring needed for the 24-Month aging group). The full Monitoring System is shown on the left. On the right is the Keithley Switching System and Digital Multi-Meter from the front (top) and the back (bottom). The DMM is sitting on top of the Switching System.

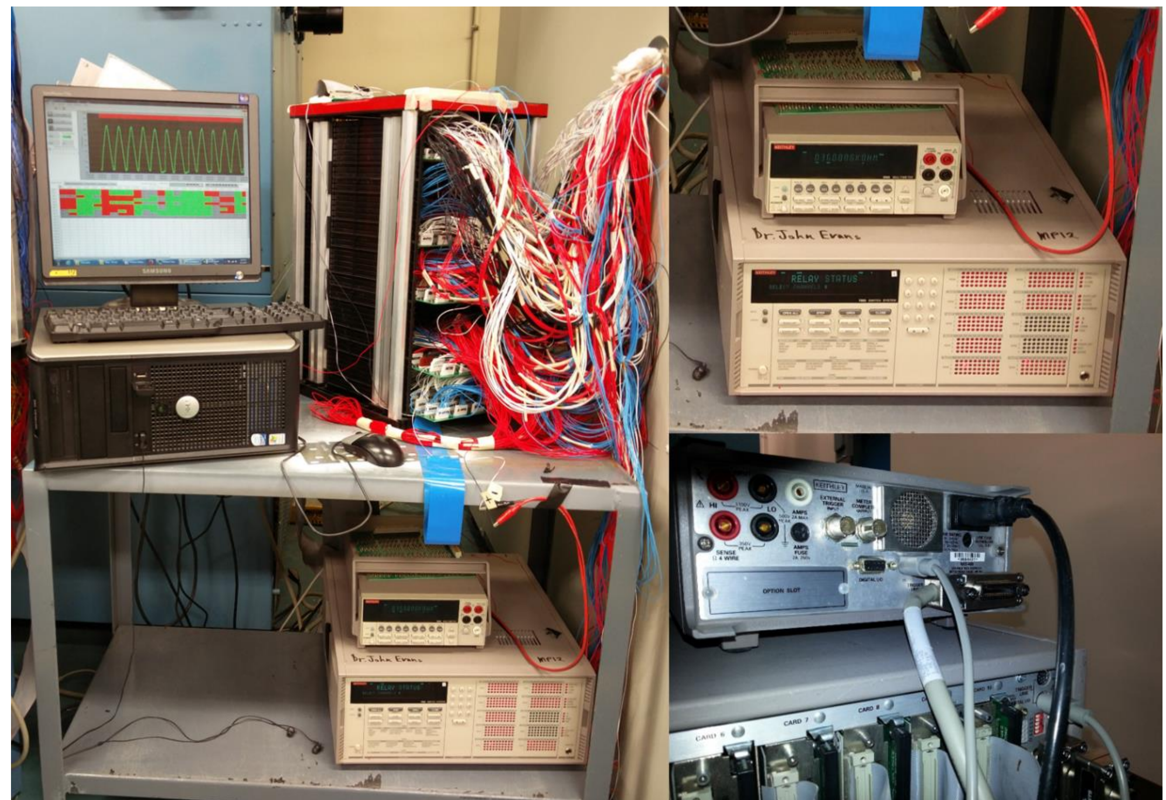


Figure 5.23. Monitoring System for the TC1-SRJ experiment (24A Group, LHS).

Monitoring was accomplished by cyclically scanning the resistance on each channel in a standard two-wire resistance test. During the scan, the Keithley switching System uses card 10 and the GRD-IB-1 interface board to "set" a particular ground channel (1-10). It then uses cards 1-9 and the connected IB-4 interface boards to scan through all of the desired data channels for that ground (up to 40 channels per IB-4, or up to 360 total channels per ground). Each ground channel (up to 10 possible ground channels) is scanned in turn. For a system with the maximum number of channels (3600), the scan will run in about five (5) minutes. Figure 5.24 shows a diagram of the main components of the monitoring system diagrammatically.

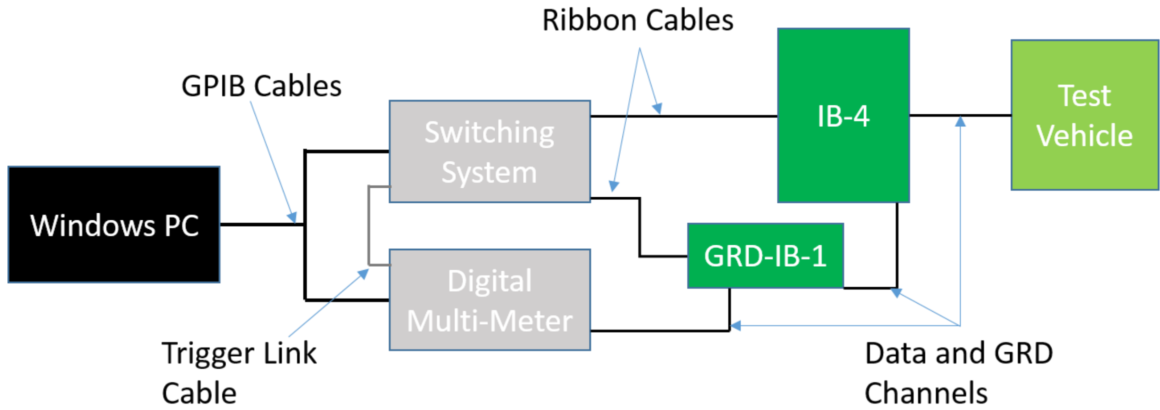


Figure 5.24. Diagram of the TC1-SRJ Monitoring System.

To register failures, the monitoring system needs to check the resistance of each channel and then determine if the resistance of a particular channel indicates that the corresponding component has failed or not failed. For this test, component failure ("failure criteria") was defined as an increase in electrical resistance greater than 100 Ohms above the baseline resistance in 5 consecutive readings. This is loosely similar to the "high speed data acquisition" criteria from the JESD22-B111 JEDEC drop standard. Typical failure criteria in the literature range from a 20% increase in resistance (generally≤10 Ohms) [71,86] to a 1000 Ohm increase [91,111]. Henshall et al. [82] compared the effects of using three different failure criteria: 1) a 20% increase (same T), 2) a 500 Ohm resistance, and 3) an "infinite" resistance (hard open). They found that the 500 Ohm and "infinite" resistance criteria gave very similar curves. Using the 20% increase criteria caused failures to register "typically…200 to 500 cycles sooner than for the coarser criteria, though somewhat more scatter was evident" [82].

Once the monitoring system is set up but prior to the start of the thermal cycle testing, the resistance of each channel is recorded. This value acts as the baseline resistance for the channel and is stored along with the other information concerning that channel in the monitoring system. Typical component resistance values are in the range

of 2 to 5 Ohms as assembled, with the diodes of the ground-isolation system adding about 360 Ohms of resistance to each channel. When the scan is running, the current resistance value for each channel is measured and compared with the baseline plus the allowable increase (100 Ohms). If the current resistance of a channel exceeds this value, an "over-limit warning" is registered for the channel. A count of the total and the consecutive number of over-limit warnings is kept by the monitoring system for each channel. Channels that exhibited five (5) consecutive threshold-exceeding events (over-limit warnings) are recorded as a failure in the monitoring system. At the maximum scan time of approximately 5 minutes, 5 over-limit warnings will take around 25 minutes to take place. This gives 1/2-cycle resolution for any failures with any thermal cycle of 50 minutes or longer. (The cycle for this experiment was 120 minutes.) Due to wiring limitations, the 6-Month aging group was hand-probed at ~50 cycle intervals, with failures corresponding to 'open' resistance values.

To keep track of when failures are taking place, each failure is marked with a time-stamp and the cycle count at the time of failure. The monitoring system therefore needs a method to keep track of the cycle count. To do this, Resistance Temperature Detectors (RTDs) were positioned in the thermal cycle chamber in order to track the temperature. (Each RTD contains a platinum filament whose resistance changes in a predictable manner as the temperature changes.) An RTD scan is run between each main data scan and checks the resistance of each RTD. Up to 10 RTDs can be used with each monitoring system. The resistance of each RTD is then converted to a temperature using the Callendar–Van Dusen equation. All valid readings are averaged to calculate a chamber temperature. As the chamber transits from low-to-high temperature (as

determined by the mid-point of the high and low dwell temperatures) or visa-versa, the cycle count is incremented by 0.5. The new version of the LabVIEW software also incorporates a graph that displays the chamber temperature as a function of time.

5.6.3 Experimental Methods: Data Analysis Techniques and Software

Experimental data from the monitoring system is saved in Excel files periodically by the LabVIEW program ("IB-4 Scanning Protocol"). Once per thermal cycle, two primary files are saved:

(1) A "Config" file that contains all of the pertinent information needed by the monitoring system (Main/Failure, RTD, Thermal Cycle, and Configuration data) and is primarily machine readable, and

(2) A "PartsList" file that contains the Main/Failure data for each channel in a format intended for human readability.

In addition, a time-stamped "DataLog" file (which is simply a copy of the Config file) is saved every 24 hours (or as set by the user) for backup and archival purposes. Later versions of the LabVIEW program also incorporate a feature that lets the user generate "Weibull++ Reports," which are files that contain the Main/Failure data for each component broken down by substrate, solder paste, and isothermal aging time and temperature. These files are formatted such that data can be copied directly into the Weibull++ Software mentioned below.

To evaluate the reliability of different subgroups within the test, the data was first sorted based on key parameters such as the component, substrate, solder paste, isothermal aging time, isothermal aging temperature, etc. This was initially done by hand, but can now be done automatically by the LabVIEW program. (Some manual sorting is still

needed in order to look at other parameters such as Heatsink vs. No Heatsink.) The failure data was analyzed and graphed using the standard two-parameter Weibull approach. (See Section 3.6.1.) The reliability of the solder joints was determined in terms of the characteristic life (η) and slope (β) from this 2-parameter Weibull analysis.

The software used to perform Weibull Analysis for this experiment was Weibull++, part of the Reliasoft Synthesis 9 software suite. Figure 5.25, below, shows the user interface of the Weibull++ software. The columns for data entry are as follows: 1) Last Inspected (Cyc), 2) State (F or S), 3) Time to F or S (Cyc), 4) Subset ID 1. The “F or S” indicates whether the component has Failed (F) or Survived (S) to the indicated cycle count. Data is stored with interval censoring to allow for a single/universal data file format for all reliability data for the research group and to allow for various events involving a temporary loss of monitoring (i.e. building loses power, etc.).

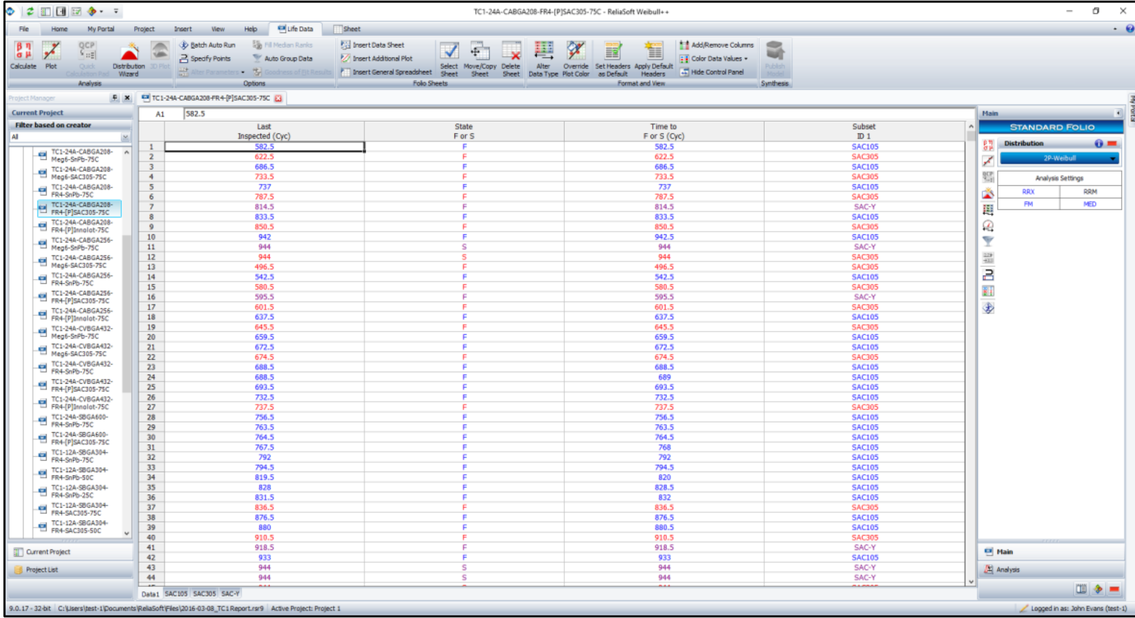


Figure 5.25. Weibull++ Software User Interface.

5.6.4 Experimental Methods: Failure Analysis Protocol and Methods

Component sectioning was done using an Allied Trim Saw and diamond sectioning blade, following by cold mounting (cast mounting) using a two-part epoxy system (resin + hardener). All grinding and polishing steps were done on a Pace Technologies FEMTO-1000 (with NANO-1000T polishing head) semi-automated polishing machine. Rough and Fine Grinding are accomplished using standard PSA-backed Silicon Carbide (SiC) grit papers (see Table 5.5, below).

Table 5.5. US and European Grip Paper standard systems [112].

Standard Grit Size (ANSI) [US System]	European P-grading System	Median Particle Diameter (microns)	Rc-30 Steel Surface Roughness (Ra-micron)
240	P220	63	300
320	P360	45.5	
400	P800	21.8	120
600	P1200	15.3	75
800	P2400	6.5	
1200	P4000	2.5	20

Rough Grinding was done to reach the “site of interest” – in this case, a plane passing through the center of the solder joints. Currently, our rough grinding process involves two (2) steps: 320 Grit and 600 Grit (both SiC). The purpose of all subsequent grinding steps (“fine grinding”) and subsequent polishing is to remove surface damage caused by the proceeding steps and reveal the true microstructural details of the sample. Our fine grinding process involves two (2) steps: 800 Grit and 1200 Grit (both SiC).

Polishing involves the use of a cloth pad and abrasive particles that are applied as a paste, slurry or spray. Initially, the abrasive particles are not fixed to the cloth pad, and move between the pad and specimen (this is a type of lapping) [113]. However, the abrasive particles quickly become fixed in the cloth pad, cutting into the sample as in grinding. Proper polishing is critical because your polishing steps must completely remove surface damage from all preceding sample preparation steps [60,61]. The ATLANTIS Polishing Pad was used for both intermediate and final polishing, although this is always subject to refinement. The intermediate polishing step was done using 1-micron alumina particles and the final polishing with 0.05-micron alumina.

Following polishing, the samples are carbon coated and examined using Scanning Electron Microscopy. Backscatter Electron (BSE) mode detection is used, as these are metallic samples. Additionally, Energy Dispersive Spectrometry (EDS/EDX) is done to acquire compositional information. EDS is performed in the Scanning Electron Microscope (SEM) using the characteristic X-Rays emitted during normal electron-beam – sample interactions.

Chapter 6
Reliability Testing Results

6.1 Weibull Graphs and Results

This experiment considers the thermal cycle reliability of an assortment of different electronic components and evaluates them on 0.200" (200 mils) printed circuit boards. Two substrate materials are tested: FR4-06 and Megtron6. Organic Solderability Preservative (OSP) surface finish is used with all test vehicles. The primary solders for package attachment in this experiment are SnPb and SAC305. Two solders designed for high-temperature reliability are also considered, including a Bi-doped SAC material and the six-element alloy Innolot (Sn3.8Ag0.7Cu3Bi1.4Sb0.15Ni).

Isothermal storage at high temperature was used to accelerate the aging of the assemblies. Aging Temperatures are 25ºC, 50ºC, and 75ºC. Aging durations are 0-Months (No Aging, baseline), 6-Months, 12-Months, and 24-Months. The test vehicles were then subjected thermal cycles of -40°C to +125°C on a 120-minute thermal profile in a single-zone environmental chamber to assess the solder joint performance. The temperature cycling test results below show some the reliability data from the 0-Month (No Aging) group, the 12-Month aging group, and (preliminary data from) the 24-Month aging groups. (Data is shown for the 24-Month aging group up to approximately 1300 thermal cycles; data taking for this group is ongoing at the time of publication.)

6.2 CABGA 36 [6mm, 0.8mm pitch]

The CABGA 36 component is one of the smallest BGA packages in this test, at 6mm x 6mm, but is of medium pitch (0.8mm). It is found on both the top- and bottom-side of the TC1-SRJ test vehicle and within all groups, allowing for multiple comparisons across various experimental parameters.

The CABGA 36 component was one of the slower failing components tested. Consequently, too few failures occurred in most test subgroups to form Weibull distributions. Failure data is available for the CABGA 36 component in the 12-Month Aging Group. Figure 6.1 shows the available failure data, which is 75°C aging and primarily for matched SnPb solder.

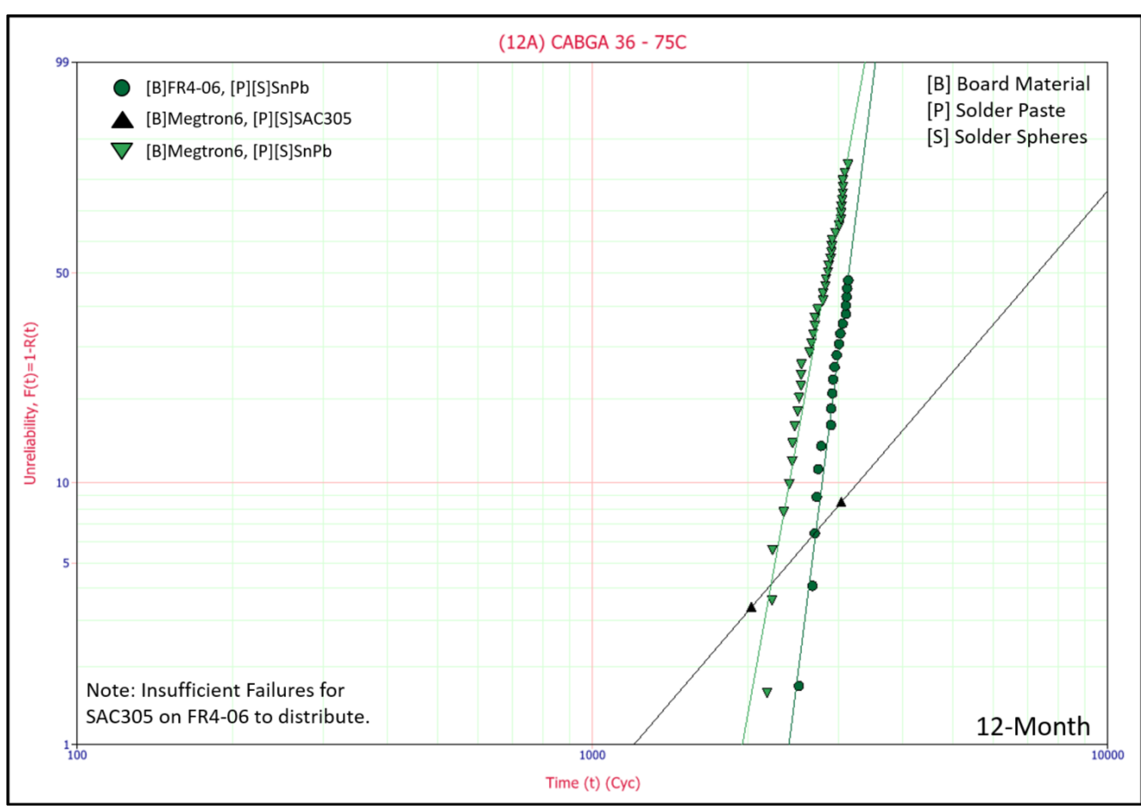


Figure 6.1. All data at 12-Months of Aging (75°C). CABGA 36 – [P][S]SnPb.

A few failure points for SAC305 solder joints are available, but it is difficult to say at this point whether these are outliers or fit well with the overall distribution. The

Lead-Free materials appear to outperform Tin-Lead in terms of the characteristic life, but an early failure does exist that may indicate a cross-over in reliability at low failure percentages. Based on the available data (Figure 6.1), the only other result that can presently be drawn is that the FR4-06 substrate outperforms the Megtron6 substrate. This substrate effect appears to be consistent for all standard (cavity-up) plastic ball grid array (BGA) packages tested, irrespective of any other factor. Further data can be expected from the 24-Month Aging group testing, which is currently ongoing.

6.3 CABGA 208 [15mm, 0.8mm pitch]

The CABGA 208 component is also found on both the top- and bottom-side of the TC1-SRJ test vehicle and within all groups, allowing for multiple comparisons across various experimental parameters. This is a larger package, at 15mm x 15mm, but shares the same 0.8mm pitch as the CABGA36.

The CABGA 208 is one of the earlier failing packages (behind the CABGA 256 and CVBGA 432), and a substantial amount of failure data is available for it. All three of these components appear to display largely similar reliability trends (e.g. when comparing different subgroups) and the CABGA 208 data serves as a good starting point for understanding these trends. Figure 6.2, below, shows the Weibull graph for all CABGA 208 subgroups on the FR4-06 substrate material for the No Aging Group.

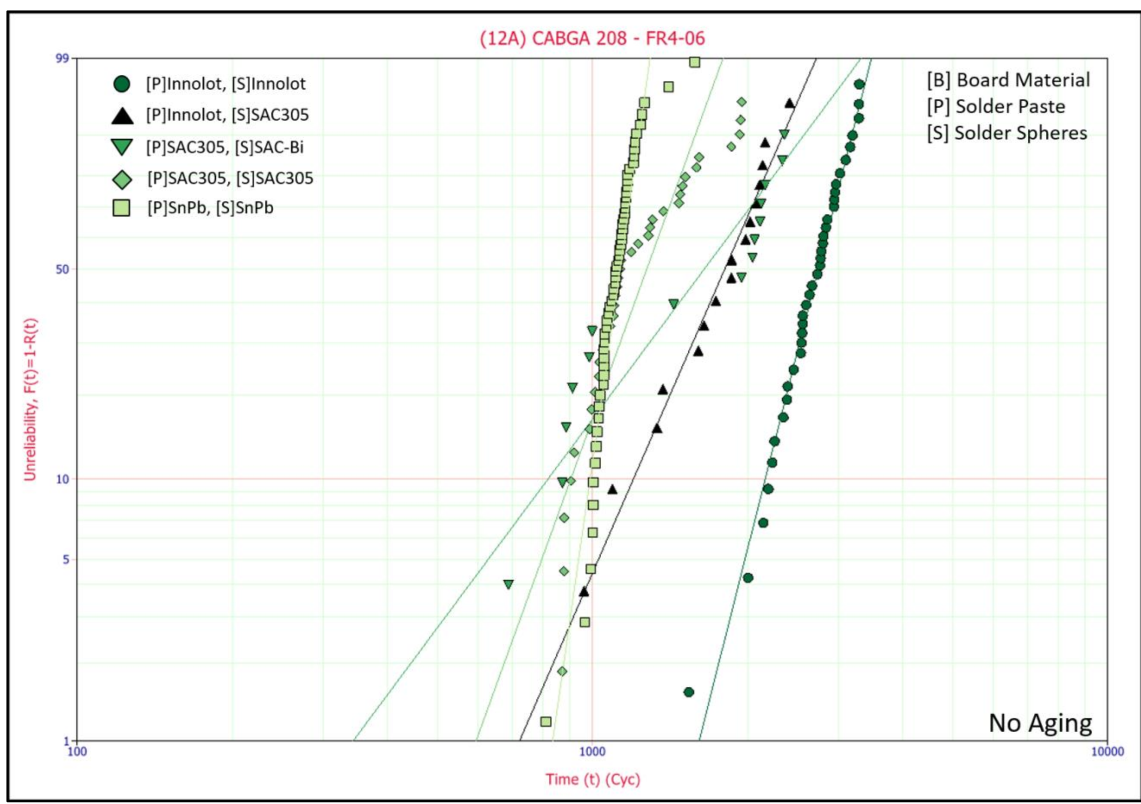


Figure 6.2. Key Groups on FR4-06. CABGA 208 – No Aging.

When comparing the reliability of various solder paste [P] and solder sphere [S] combinations, the Characteristic Life values show the following pattern for the No Aging Group, ranked from best to worst:

(1) Matched [P][S]Innolot

(2) [S]SAC305 doped with [P]Innolot

(3) Matched [P][S]SAC305

(4) Matched [P][S]SnPb

The above trends are found for both substrate materials, with the proviso that Innolot data is not available on the Megtron6 substrate. Figure 6.3 shows the trends in characteristic life for the No Aging group and CABGA 208 component.

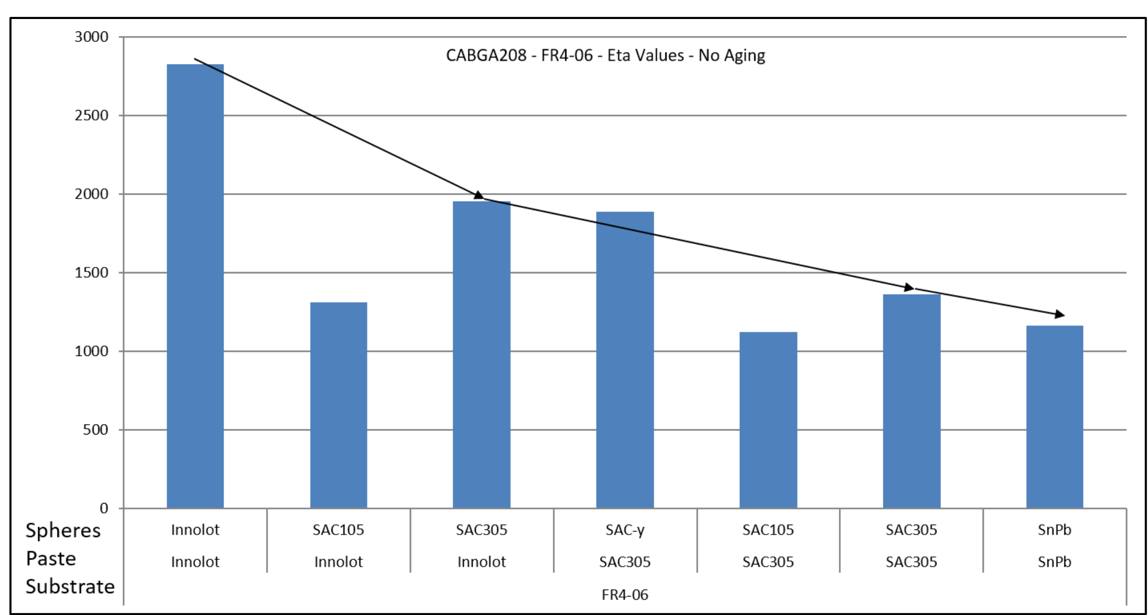


Figure 6.3. Characteristic Life values. CABGA 208 – FR4-06 – No Aging.

Components balled with SAC305 spheres are more reliable than equivalent SAC105 balled components. This pattern holds for both SAC305 and Innolot solder pastes. However, the components balled with SAC105 solder tend to exhibit a higher shape parameter (slope). Lower slope values indicate a less peaked Weibull distribution, or greater variance in the failure data. Lower slope values mean that it is more difficult to predict when failures will occur. Hence, although SAC 305 demonstrates higher characteristic life, predictability may be an issue for some applications. This slope difference may stem from SAC105's higher ductility, which makes (relatively predictable) failures across the bulk solder more common in SAC105. Slope values of 6 and higher would be preferable; however, both SAC 105 and SAC 305 typically exhibit lower slope values than Sn-Pb controls.

No difference is seen in the pattern of failures when comparing components found on the Top-Side of the board and the Bottom-Side of the board, with the exception of the SAC-Y (Bi-doped) spheres. Since the top-side and bottom-side stencils used in this

experiment were of different heights, the paste volume – and therefore the ‘paste doping’ – on the top- and bottom-side assemblies will be different.

The fact that the Bismuth-doped material has slightly different reliability on the top-side vs. bottom-side test vehicles may indicate that the Bismuth-doped material is more sensitive to the paste dilution. Higher sensitivity to reflow parameters is another possible explanation. The characteristic life of the Bismuth-doped SAC-based solder exceeds that of SAC305, but not of Innolot (Sn3.8Ag0.7Cu3Bi1.4Sb0.15Ni).

Figure 6.4 shows the Weibull plot for the CABGA 208 component with 12-Month Aging on the FR4-06 substrate material, and Figure 6.5 shows key groups form the No Aging and 12-Month Aging Group. Note that every subgroup may not appear on each graph, and also, that the color coding of the groups may vary between graphs. Data is from 75°C aging unless otherwise marked.

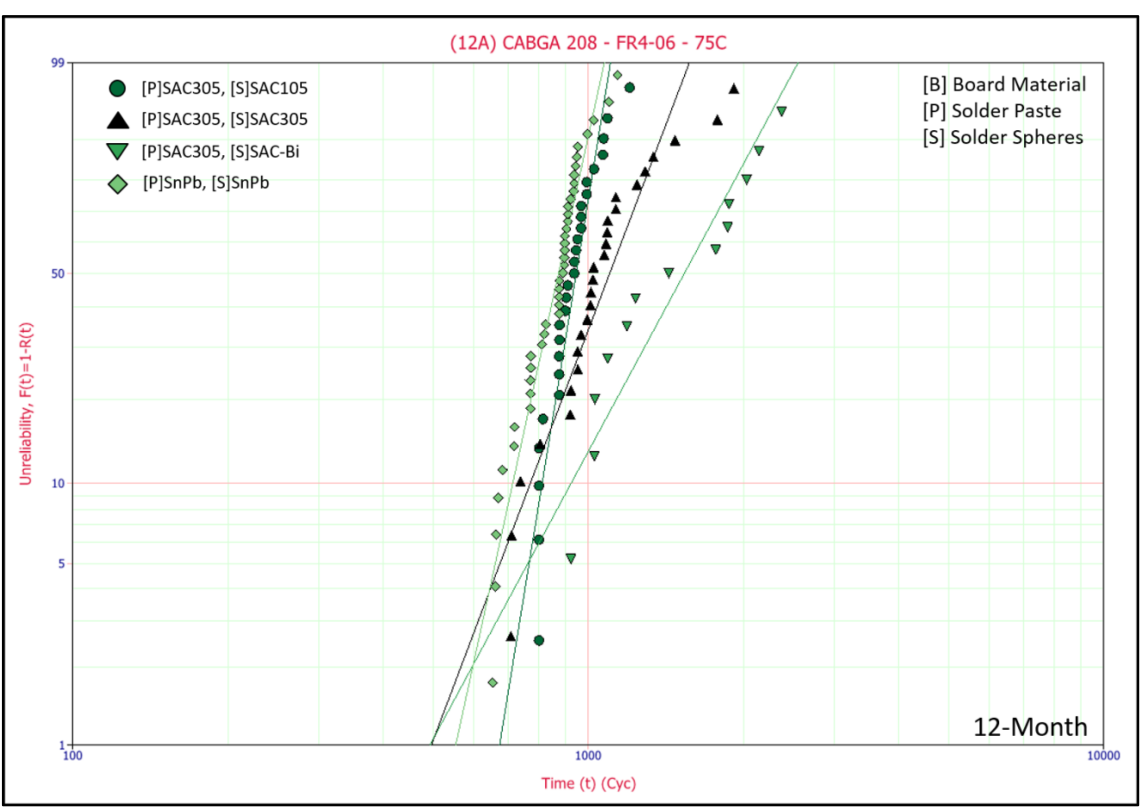


Figure 6.4. All data on FR4-06. CABGA 208 – 12-Month Aging – 75°C.

The 12-Month reliability data shows the same overall trends as the No Aging data on FR4-06. The Lead-Free solders continue to outperform the SnPb control after 12 months of aging at 125°C. As with the No Aging data, the Bismuth-doped SAC-based solder outperforms SAC305. No Innolot boards are included in the 12-Month Aging group. Consequently, no conclusion can be drawn about that material for this aging group. Figure 6.5, below, shows the Weibull graph for key subgroups from the No Aging and 12-Month Aging sets on FR4-06.

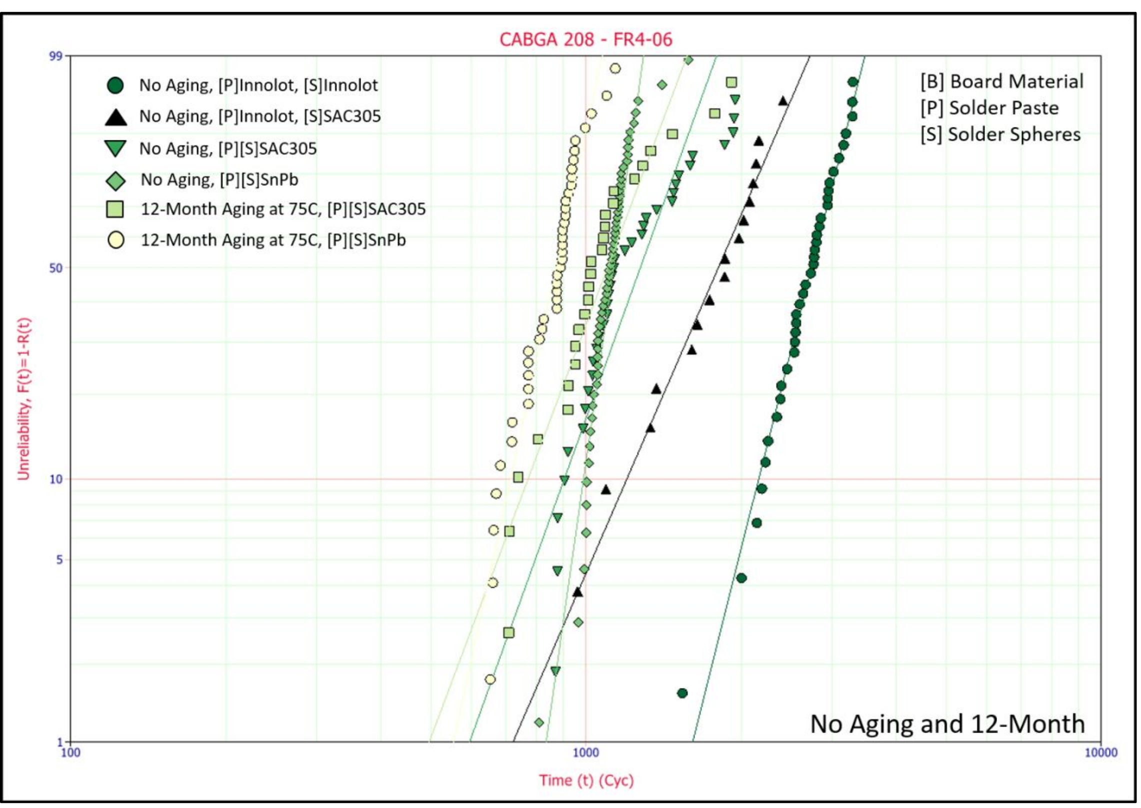


Figure 6.5. Key groups on FR4-06. CABGA208 – No Aging and 12-Month (75°C).

Both the SAC305 and SnPb control are seen to experience significant degradation in reliability after aging for 12 months at 75°C. A clear crossover is not seen in the reliability of the two solder materials except when projecting to low values of

unreliability. Figure 6.6, below, shows the 12-Month Aging group on the Megtron6 substrate.

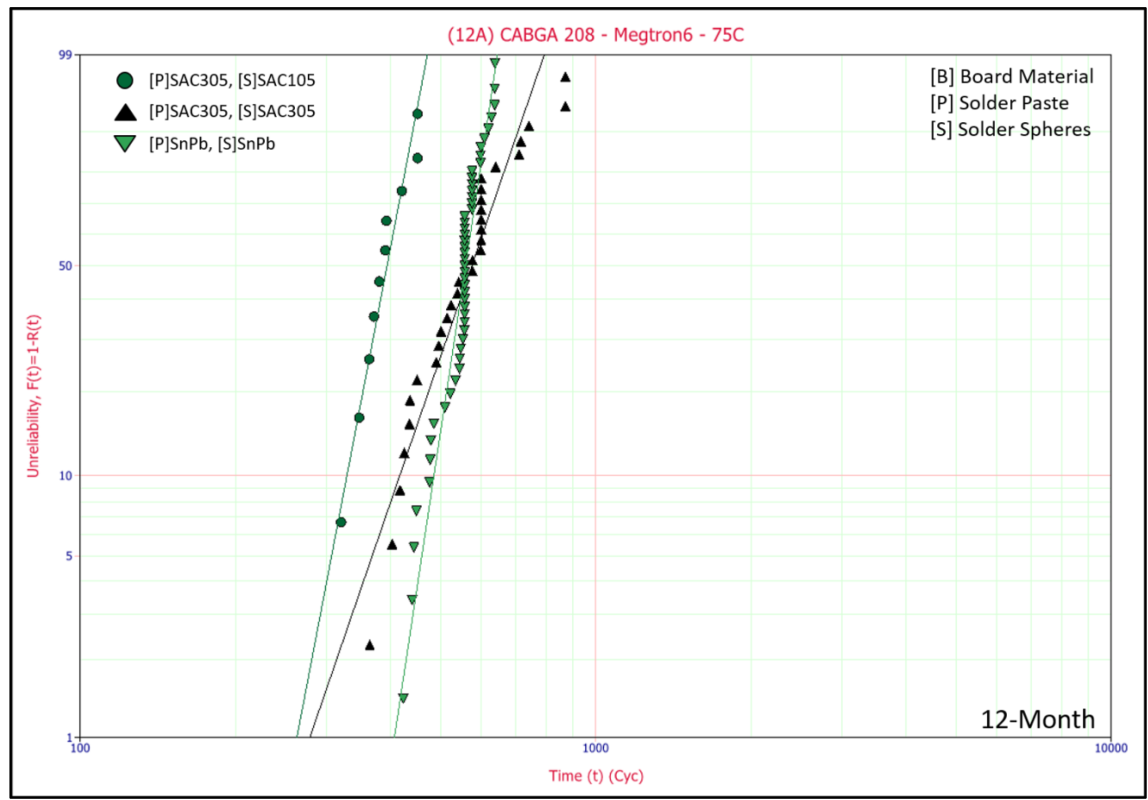


Figure 6.6. All data on Megtron6. CABGA 208 – 12-Month Aging – 75°C.

Note that there is a very clear difference between the relative degradation seen on the two substrates. On Megtron6, unlike on FR4-06, a cross-over can be seen at approximately 45-50 percent unreliability between the SnPb control group and the matched SAC305 group. SAC105 spheres perform even worse. This indicates that for certain applications, SnPb will perform better than SAC305 even after 12-Months of Aging (75°C).

Figure 6.7 shows the Weibull plot for the CABGA 208 component at 24-Month Aging (75°C) for key subgroups on both substrates.

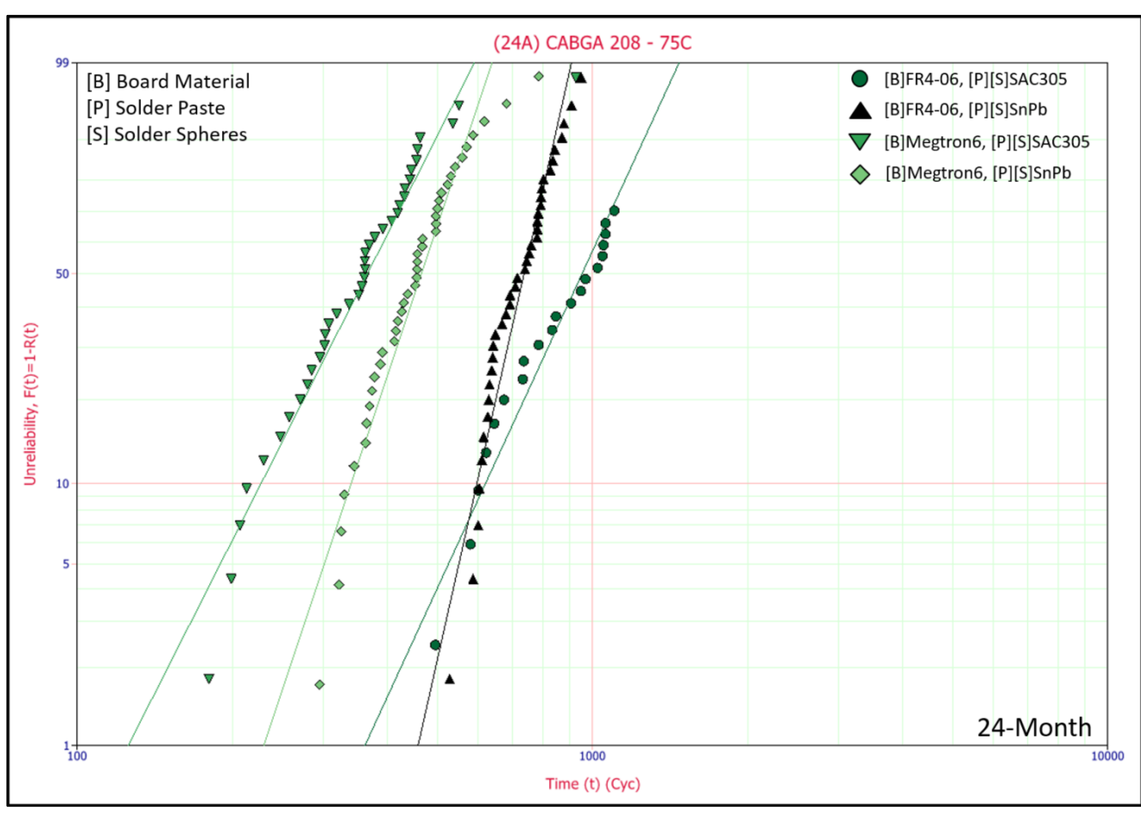


Figure 6.7. Key Groups at 24-Months Aging (75°C). CABGA 208.

The 24-Month data available shows an interesting divergence. As shown in Figure 6.7, above, the FR4-06 substrate continues to vastly outperform the Megtron6 substrate when comparing the reliability data for comparable packages mounted to the two substrates. However, a cross-over in the reliability data for the matched SAC305 and matched SnPb solder materials is not observed for CABGA 208 components on FR4-06 while one is observed for comparable packages on Megtron6. This disparity is most likely due to differences in material properties between the two substrates, although evolution of the substrate properties over time may play a role. Finite element modeling may prove useful in elucidating the role of each.

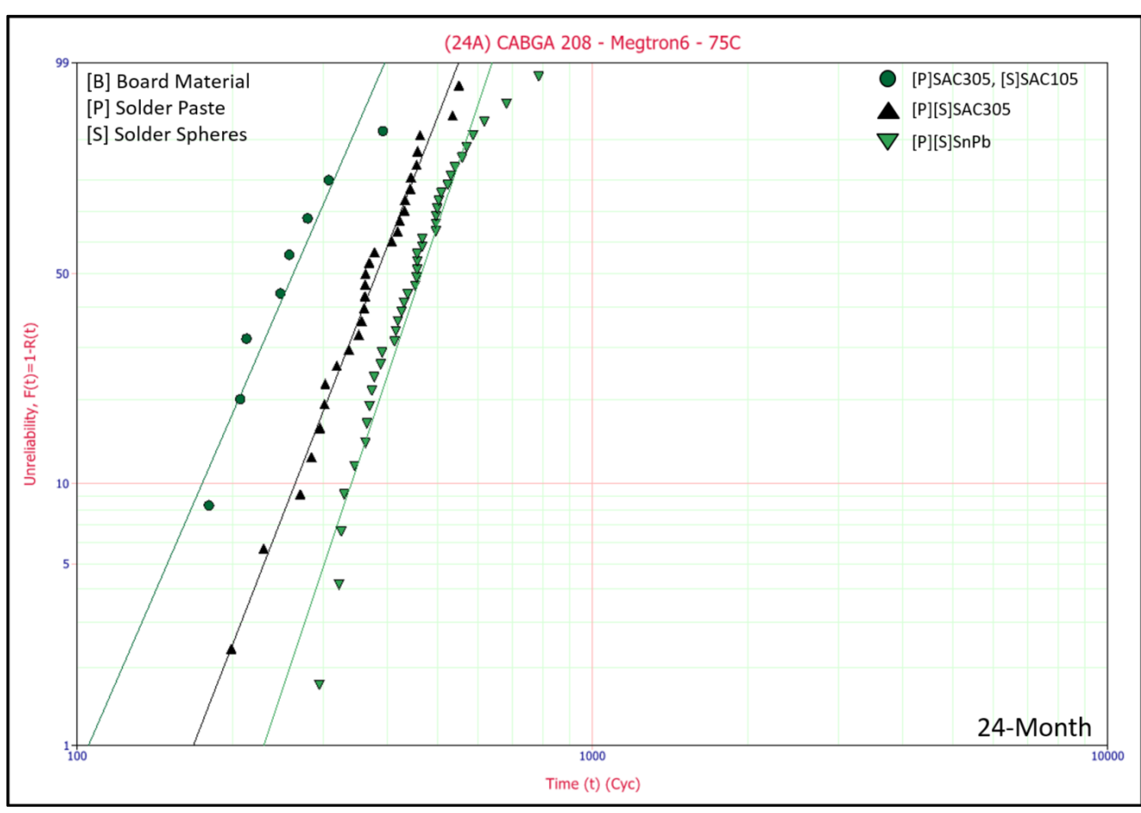


Figure 6.8. All data on Megtron6. CABGA 208 – 24-Month Aging – 75°C.

Figure 6.8, above, shows the Weibull graph for CABGA 208 packages mounted on Megtron6 with 24-Months Aging at 75°C. The SnPb control group is found to perform significantly better than matched [P][S]SAC305. Components with SAC105 solder spheres assembled in conjunction with SAC305 solder paste perform worst.

6.4 CABGA 256 [17mm, 1.0mm pitch]

The CABGA 256 is slightly larger than the CABGA208, at 17mm x 17mm. It also has a larger pitch at 1.0mm. This component is found within most test groups (no reballing) and is only on the Top-Side of the TC1-SRJ test vehicle.

The CABGA 256 (along with the CVBGA 432) is one of the first-failing components in the test. Figure 6.9, below, shows the Weibull graph for all CABGA 256 subgroups on the FR4-06 substrate material for the No Aging Group.

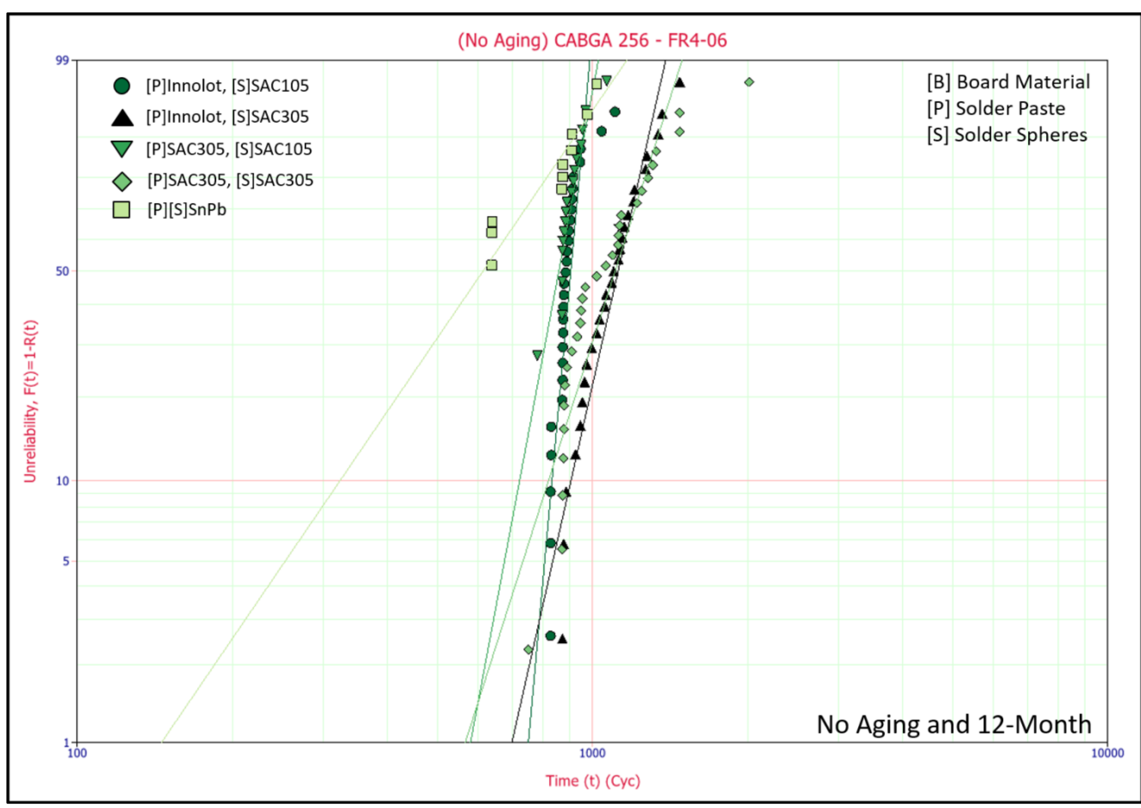


Figure 6.9. All data on FR4-06. CABGA 256 – No Aging.

Overall reliability trends for the CABGA 256 are very similar to those for the slightly smaller CABGA 208. No Aging data trends are the same for both substrates. However, as with the CABGA 208, the FR4-06 substrate outperforms the Megtron6 substrate when comparing equivalent packages.

One interesting point is that the CABGA 256 package – which is slightly larger, has more joints, and has larger joints than the CABGA 208 – demonstrates a somewhat lower reliability improvement from the use of Innolot solder paste. This holds true both for SAC105 and SAC305 spheres.

Figure 6.10 shows the Weibull graph for all CABGA 256 subgroups on the FR4-06 substrate material for the 12-Month Aging Group. The Sn-Ag-Cu solder materials continue to outperform the SnPb control in for this component and aging temperature. Unlike the CABGA 208 component, there is not a crossover observed on Megtron6.

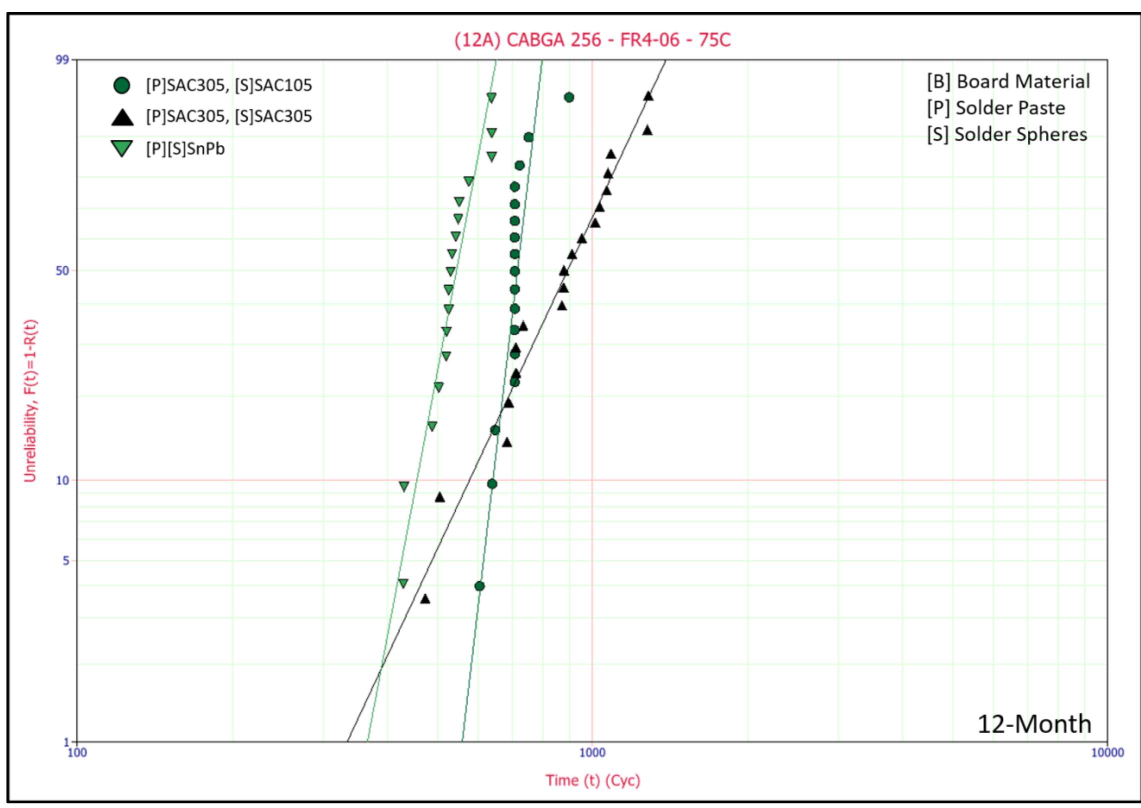


Figure 6.10. All data on FR4-06. CABGA 256 – 12-Month Aging – 75°C.

Figure 6.11, below, shows failure data on FR4-06 from the 24-Month Aging Group. Note that the reliability of Lead-Free solder joints here continues to exceed that of SnPb joints, except for projections to low values of unreliability. All groups show significant degradation. At 24-Month Aging, Innolot solder paste doping does not show a significant reliability improvement (over the use of standard SAC305 paste).

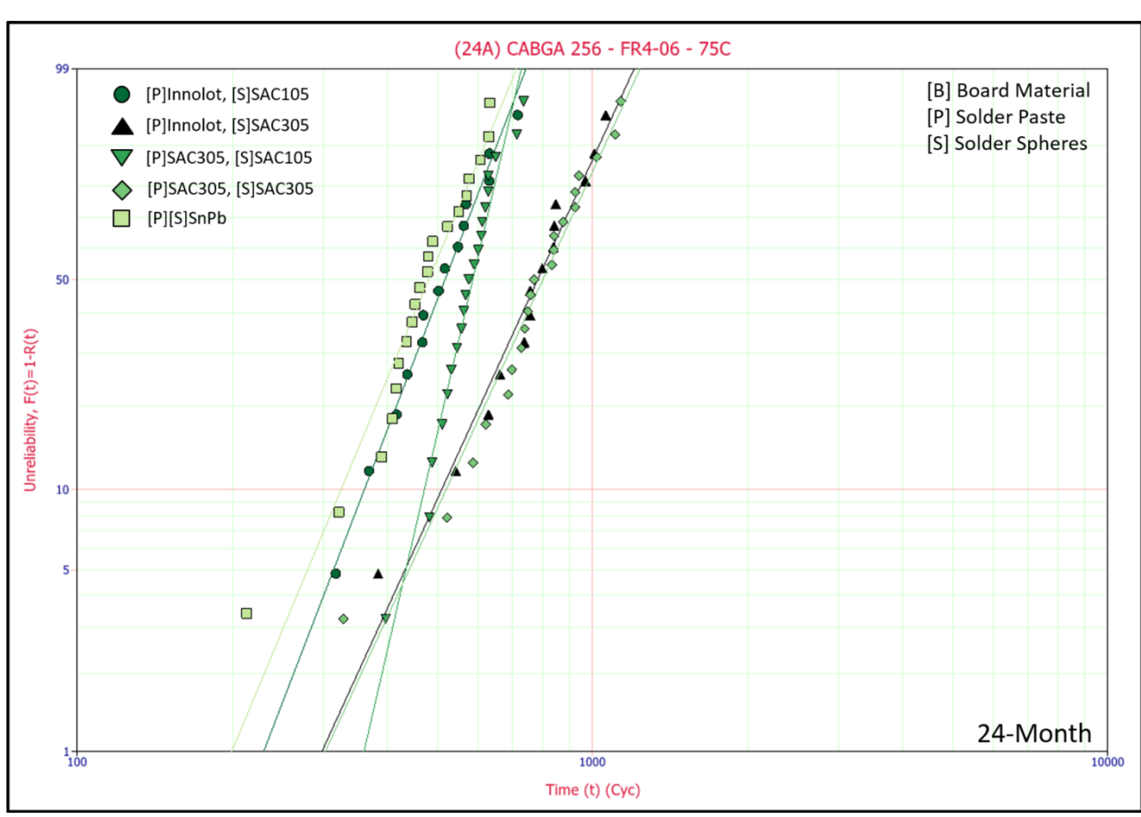


Figure 6.11. All data on FR4-06. CABGA 256 – 24-Month Aging – 75°C.

Figure 6.12 shows failure data on Megtron6 from the 24-Month Aging Group. On the Megtron6 substrate, the degradation of SAC305 respective to SnPb is again more significant than on the FR4-06 substrate. This is similar to what was observed with the CABGA 208 component. Here, the two Weibull curves have a cross-over point at around 280 cycles, or 30-40% unreliability. Overall reliability also continues to be worse on the Megtron6 substrate than on the FR4-06 substrate.

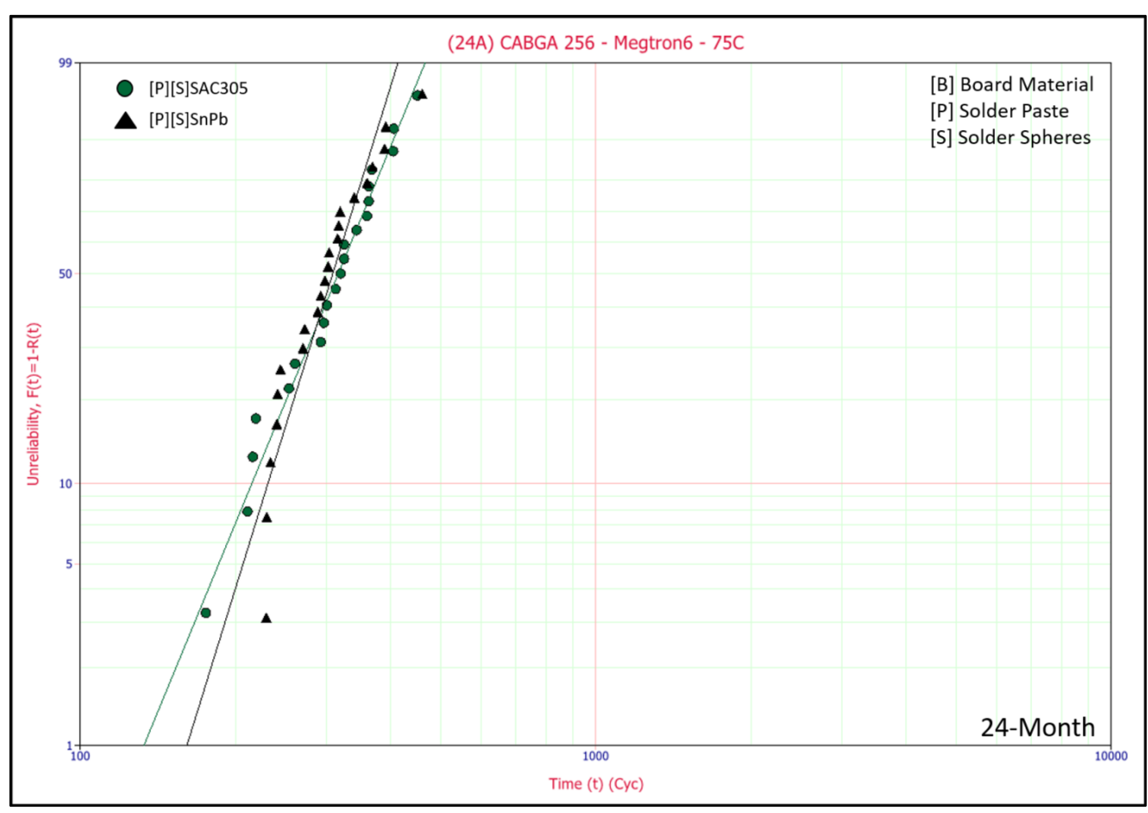


Figure 6.12. All data on Megtron6. CABGA 256 – 24-Month Aging – 75°C.

6.5 CTBGA 84 [6mm, 0.5mm pitch]

The CTBGA 84 is a second 6mm x 6mm component, but with a smaller pitch than the CABGA36 (0.5mm, rather than 0.8mm). This component is found only on the bottom-side of the TC1-SRJ test vehicle.

The CTBGA 84 component was one of the slower failing components tested. Consequently, too few failures occurred in most test subgroups to form Weibull distributions. Failure data is available for the CTBGA 84 component in the No Aging and 12-Month Aging Groups. Figure 6.13, below, shows the available failure data from the No Aging Group, which is primarily for matched SnPb solder, with a few SAC305 failures. Data is for 75°C aging unless otherwise marked.

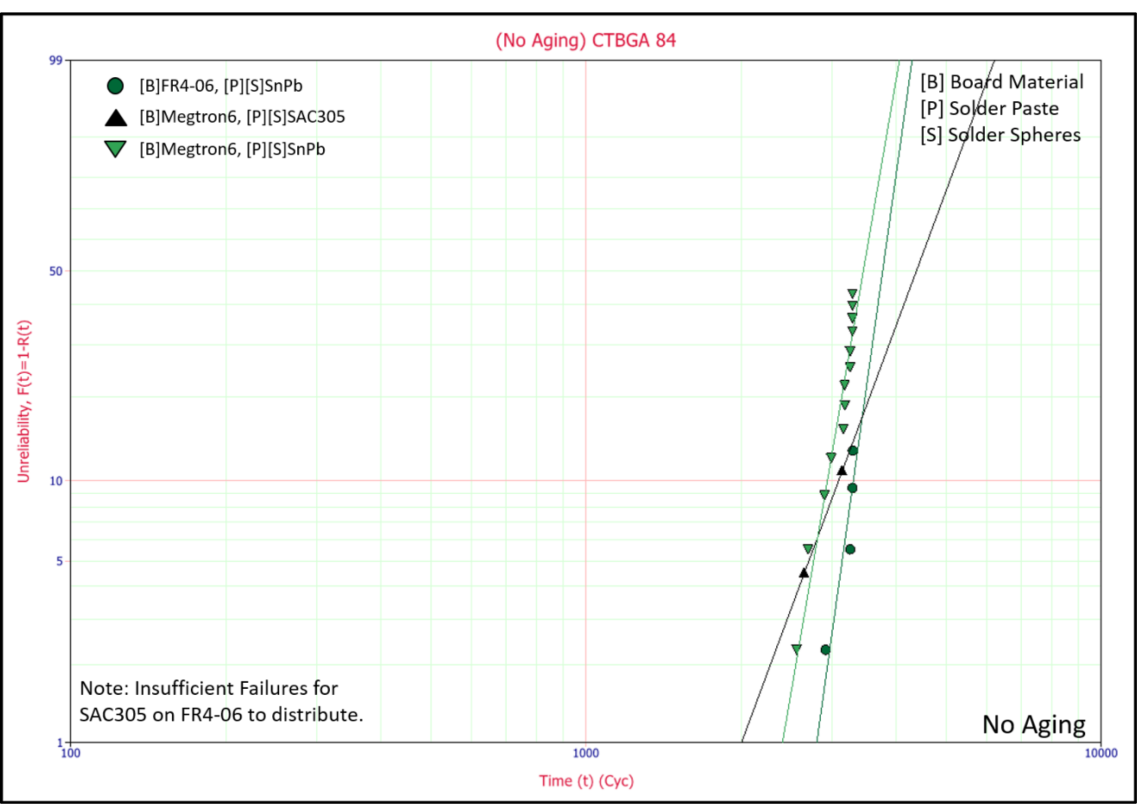


Figure 6.13. All data at No Aging. CTBGA 84 – 12-Month Aging – 75°C.

As with the other plastic ball grid array (BGA) components examined so far, the reliability of the CTBGA 84 package is higher when assembled on the FR4-06 substrate material than on the Megtron6 substrate material. This substrate effect appears to be consistent for all standard (cavity-up) plastic ball grid array (BGA) packages tested, irrespective of any other factor.

A few failure points for SAC305 solder joints are available, but it is difficult to say at this point whether these are outliers or fit well with the overall distribution. The Lead-Free materials appear to outperform Tin-Lead in terms of the characteristic life, but an early failure does exist that may indicate a cross-over in reliability at low failure percentages. Figure 6.14 shows the same comparison for the 12-Month Aging Group, which is also primarily for matched SnPb solder and 75°C aging, with a few SAC305 failures.

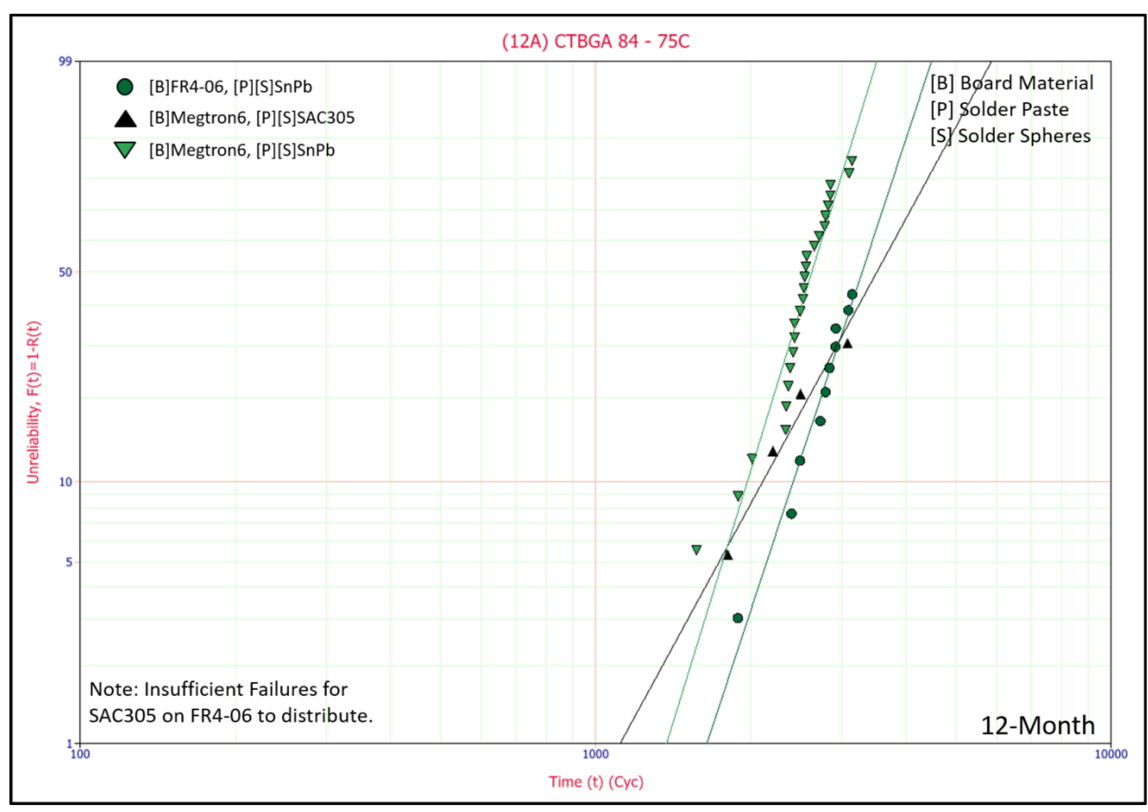


Figure 6.14. All data at 12-Months of Aging (75°C). CTBGA 84.

The reliability trends at 12-Months Aging (75oC) are largely unchanged from those seen in the No Aging group. The FR4-06 substrate continues to outperform the Megtron6 substrate. A cross-over in reliability between the Lead-Free and Tin-Lead solder joints is not observed, except for projections to low values of unreliability. Perhaps the most interesting data point is the apparent increase in the reliability gap between the two substrate materials. The difference in characteristic life between matched SnPb components on FR4-06 and Megtron6 increases from around 300 cycles (<10%) in the No Aging group to over 700 cycles (>25%) in the 12-Month Aging group. Further data can be expected from the 24-Month Aging group testing, which is currently ongoing.

6.6 CVBGA 97 [5mm, 0.4mm pitch]

The CVBGA 97 is the smallest BGA package in this test at 5mm x 5mm and has the finest pitch of any BGA component in test (at 0.4mm, tied with CVBGA 432). This component is found only on the bottom-side of the TC1-SRJ test vehicle.

The CVBGA 97 component was one of the slower failing components tested. Consequently, too few failures occurred in most test subgroups to form Weibull distributions. Figure 6.15, below, shows the Substrate Comparison from the No Aging Group with matched SnPb solder. As with the other plastic ball grid array (BGA) components tested, the FR4-06 substrate outperforms the Megtron6 substrate. This substrate effect appears to be consistent for all standard (cavity-up) plastic ball grid array (BGA) packages tested, irrespective of any other factor.

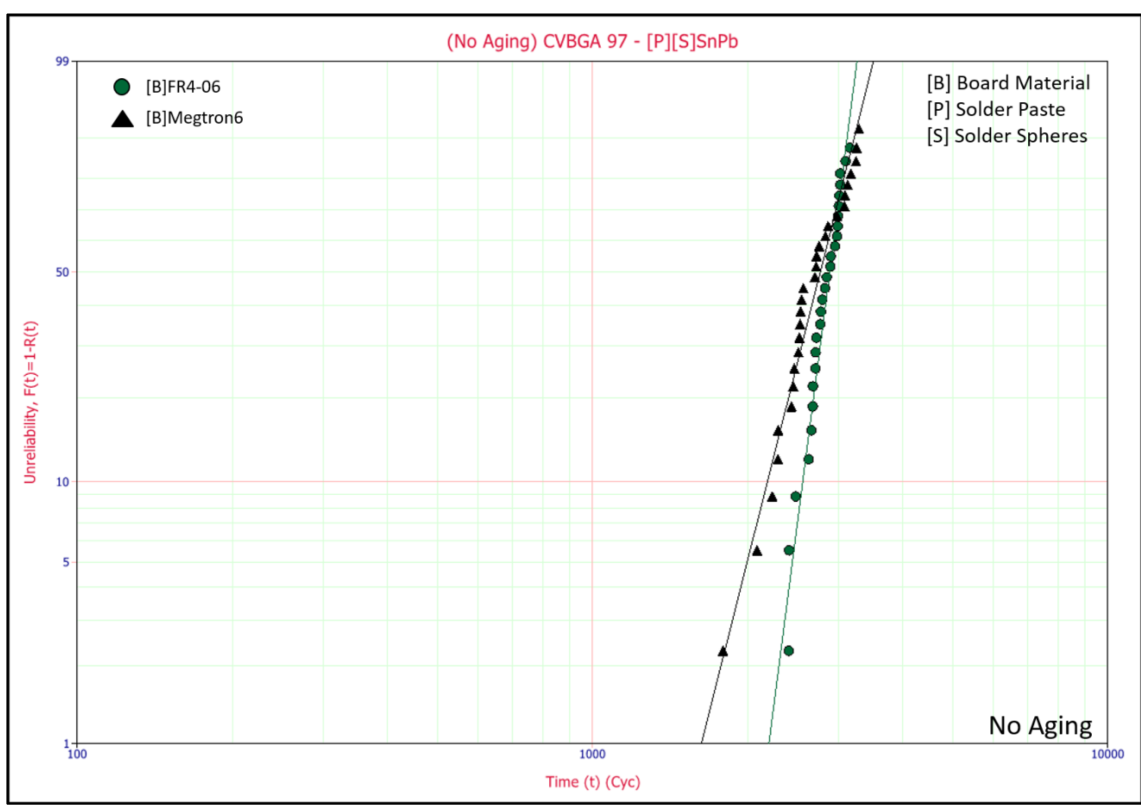


Figure 6.15. Substrate Comparison. CVBGA 97 – [P][S]SnPb – No Aging.

Figure 6.16, below, shows the available failure data for the 12-Month Aging Group, which is also for matched SnPb solder and 75°C aging. The FR4-06 substrate material continues to outperform the Megtron6 substrate material, and the difference in reliability seems to increase with isothermal aging, as seen with the CTBGA 84.

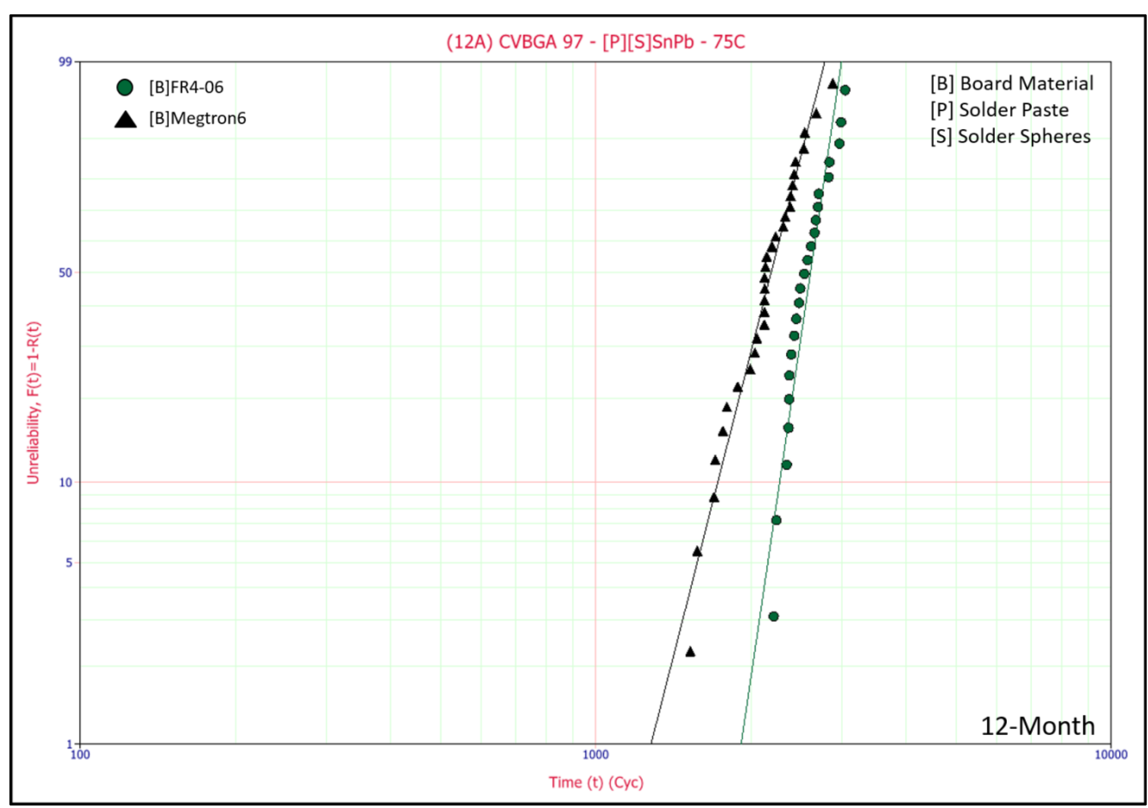


Figure 6.16. Substrate Comparison. CVBGA 97 – [P][S]SnPb – 12-Months at 75°C.

The fact that the Tin-Lead solder has sufficient failure data to distribute, but the Sn-Ag-Cu (SAC) solder materials do not demonstrates that the SAC solders have superior reliability for this package and aging time. (This is the case for both No Aging and 12-Month Aging.) Further data can be expected from the 24-Month Aging group testing, which is currently ongoing.

6.7 CVBGA 432 [13mm, 0.4mm pitch]

The CVBGA 432 has the finest pitch of any BGA component in this test (at 0.4mm, tied with CVBGA 97). However, it has a 13mm x 13mm footprint, making it significantly larger than the CVBGA 97. This component is found only on the Bottom-Side of the TC1-SRJ test vehicle.

The CVBGA 432 (along with the CABGA 256) is one of the first-failing components in the test. Reliability trends in the No Aging group are similar to those shown for the CABGA 208 and CABGA 256. One interesting note is that the CVBGA 432 package – which is slightly smaller, has more joints, and has smaller joints than the CABGA 208 – demonstrates a somewhat higher reliability improvement from the use of Innolot solder paste. This holds true both for SAC105 and SAC305 spheres. Figure 6.17 shows the solder paste comparison on the FR4-06 substrate material for the No Aging Group.

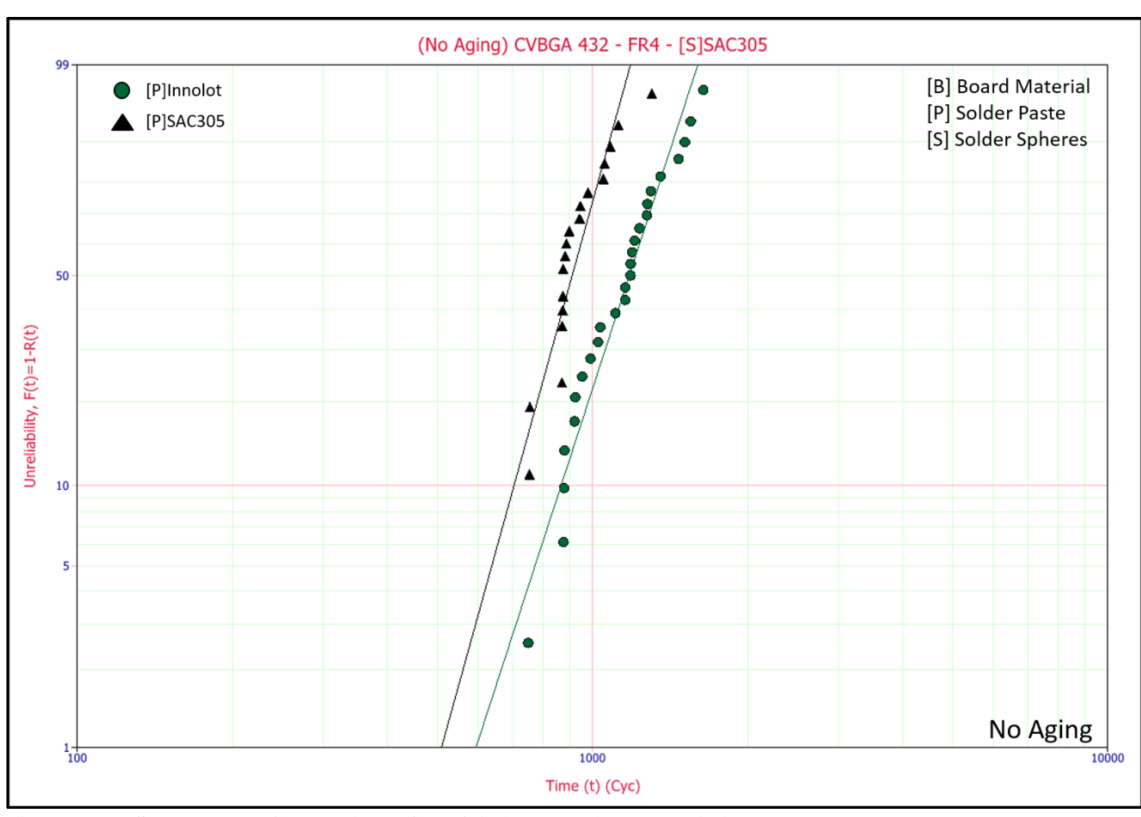


Figure 6.17. Solder Paste Comparison. CVBGA 432 – FR4-06 – No Aging.

Figure 6.18, below, shows the Weibull graph for all CVBGA 432 subgroups on the FR4-06 substrate material for the 12-Month Aging Group (75°C). The Sn-Ag-Cu solder materials continue to outperform the SnPb control in for this component and aging temperature. No Innolot boards are included in the 12-Month Aging group. Consequently, no conclusion can be drawn about that material for this aging group.

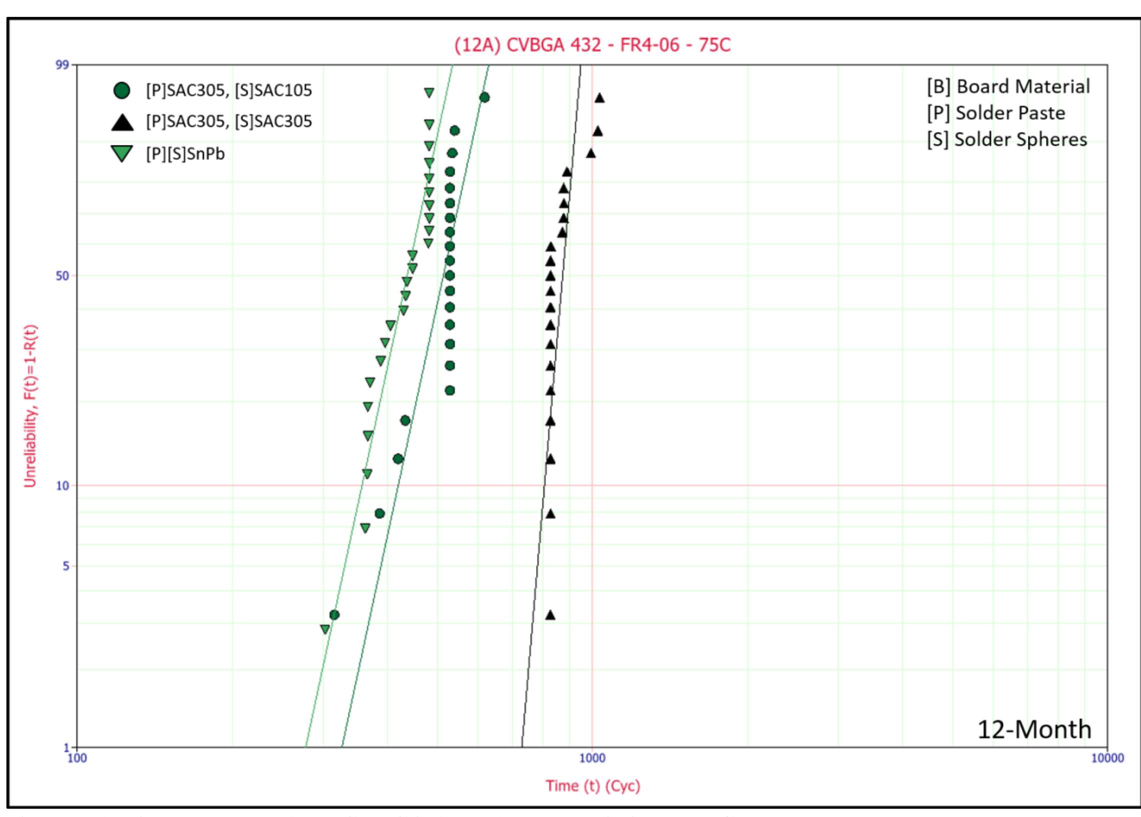


Figure 6.18. All data on FR4-06. CVBGA 432 – 12-Month Aging – 75°C.

Figure 6.19 shows the available failure data from the 24-Month Aging Group. It appears that although the CVBGA 432 initially exhibited similar reliability trends to the CABGA 208, this relationship does not hold true over the course of isothermal aging. For the CVBGA 432, the lead-free solders continue to outperform SnPb on both FR4-06 and Megtron6. The reliability difference between the two solder materials is smaller on Megtron6 however. This is somewhat in-line with the trends seen for the other plastic packages, in that the reliability degradation with isothermal aging appears to be magnified for lead-free solders on Megtron6.

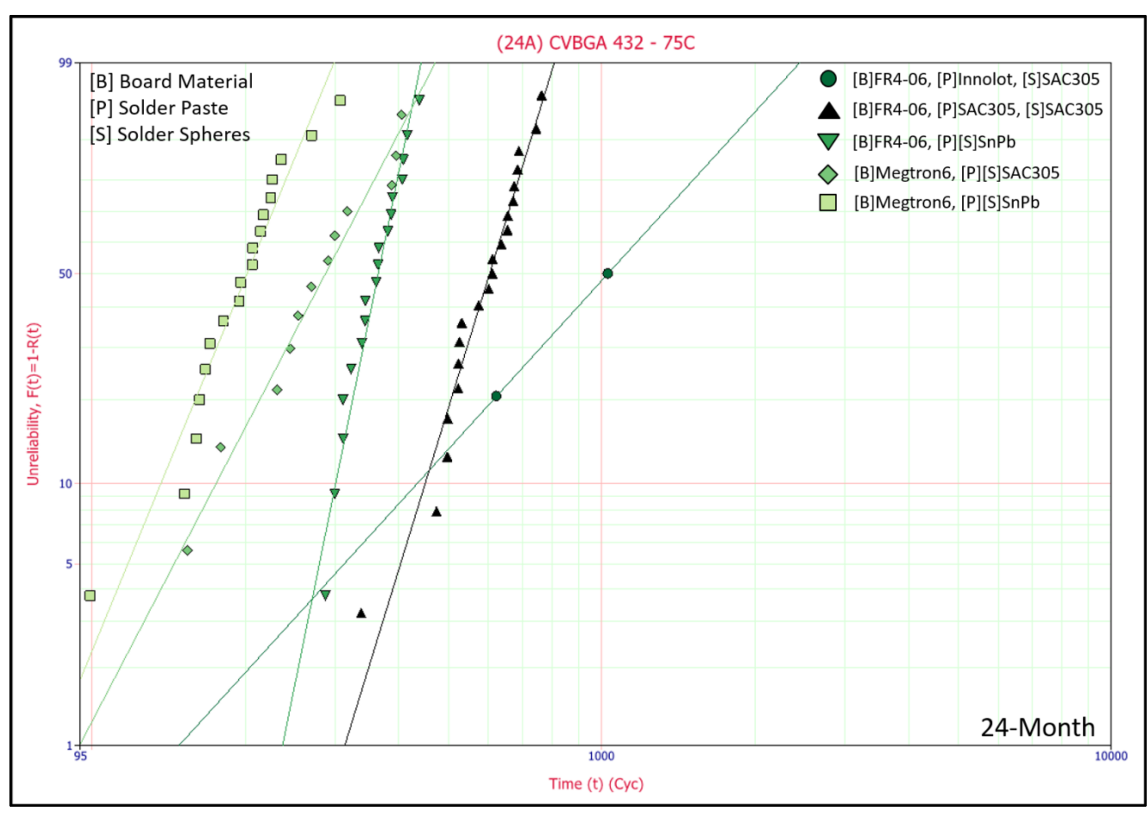


Figure 6.19. All data at 24-Months (75°C). CVBGA 432. Note horizontal axis.

6.8 Memory Module [LGA Socket + PGA]

The Memory Module is a large pin grid array (PGA) mounted by hand into a land grid array (LGA) socket on the printed circuit board following principal assembly. This component is only found on the top side of the TC1-SRJ test vehicle and is not found on [P][S]SnPb test vehicles.

As-reflowed, the Memory Module components are typically late failing in this format (PGA+LGA socket). However, the shape parameters (slopes) are quite low for many Memory Module Weibull distributions, demonstrating – at the very least – a higher variance and lower predictability in failure times. Some distributions may be exhibiting multiple slopes, which would indicate that multiple failure mechanisms are in play. Since the PGAs were inserted by hand into the LGA sockets (by inexperienced students), it is

possible some components were slightly damaged during assembly. Figure 6.20, below, shows the Weibull graph for all Memory Module subgroups for No Aging. Note that the Memory Modules are not included on the SnPb test vehicles and therefore no SnPb data is available from this experiment.

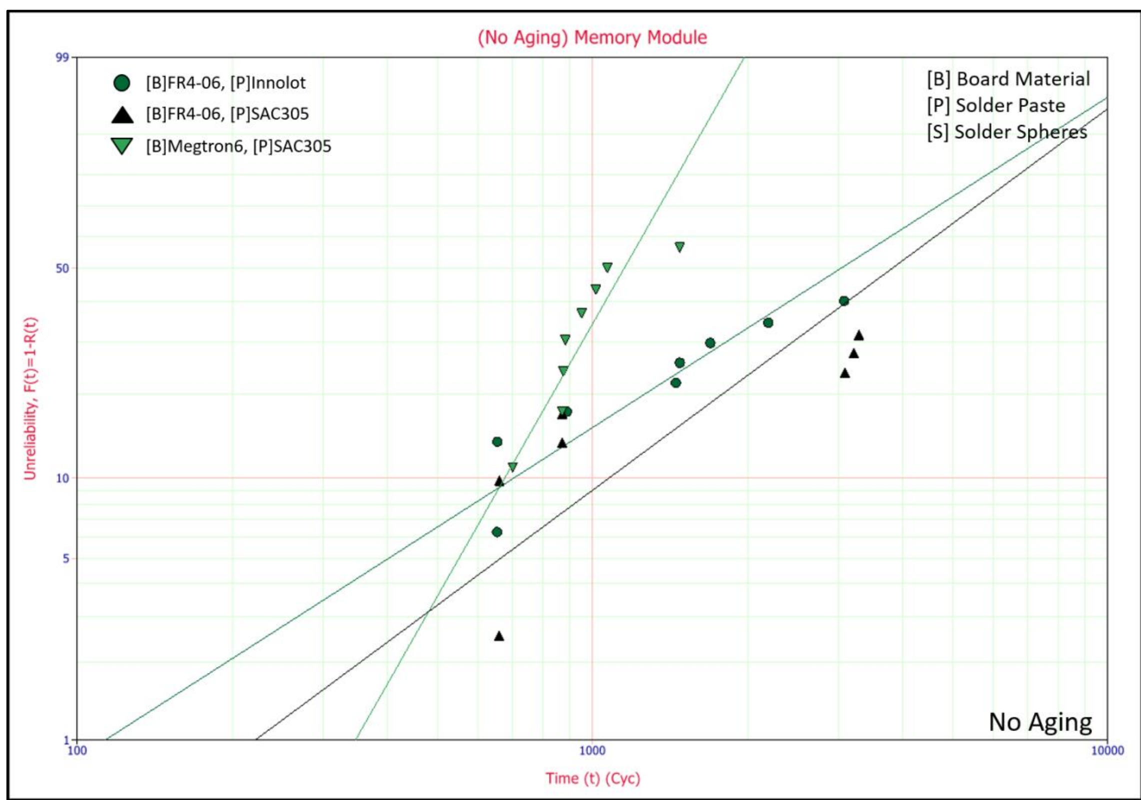


Figure 6.20. All data at No Aging. Memory Module.

Figure 6.21 shows the Weibull graph for all Memory Module subgroups for the 12-Month Aging Group. The Memory Module shows a significant degradation in reliability after 12 months of aging at higher tempertures (50°C and 75°C), with a smaller degradation for 25°C aging.

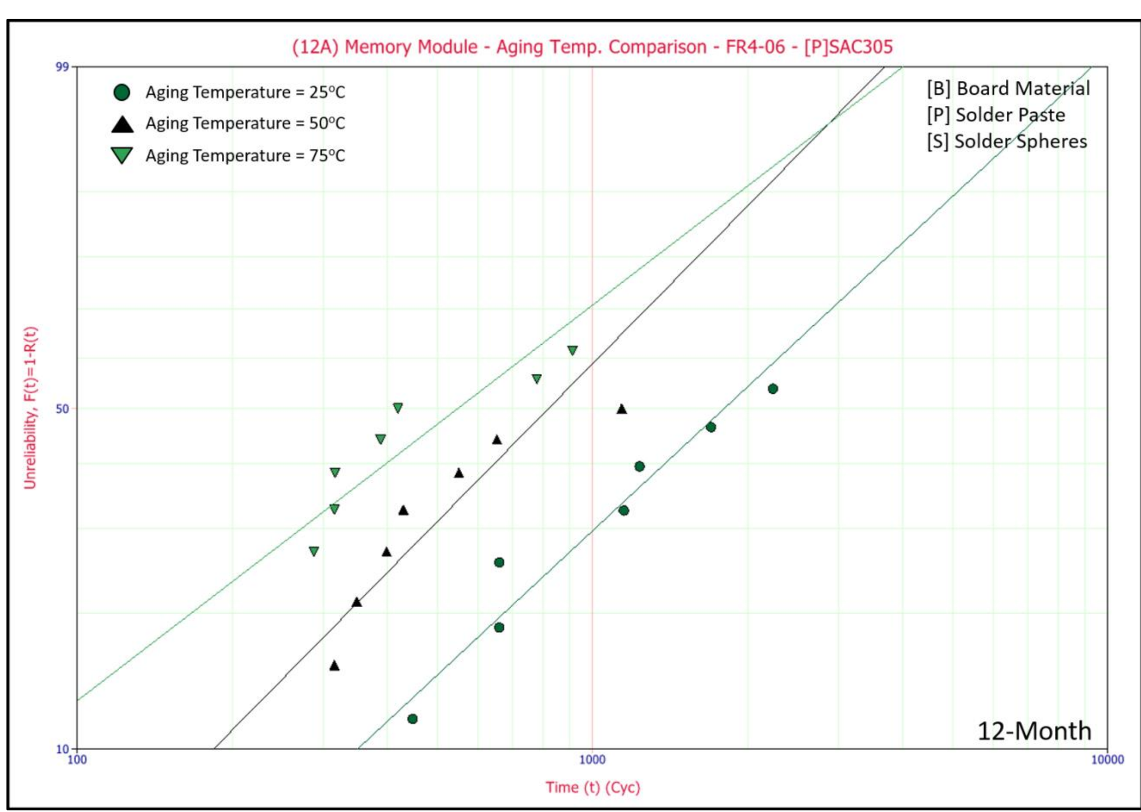


Figure 6.21. Aging Temperature Comparison. Memory Module – 12-Month Aging.

Figure 6.22 shows the available failure data for the 24-Month Aging Group. The Memory Modules continues to perform better on FR4-06 than on Megtron6. The 24-Month data also confirms that this component does not necessarily see a boost in reliability when Innolot paste. In this case, a cross-over is seen between the Innolot-paste and SAC305-paste groups, but the Innolot-paste components exhibit several early failures before failures are seen with SAC305.

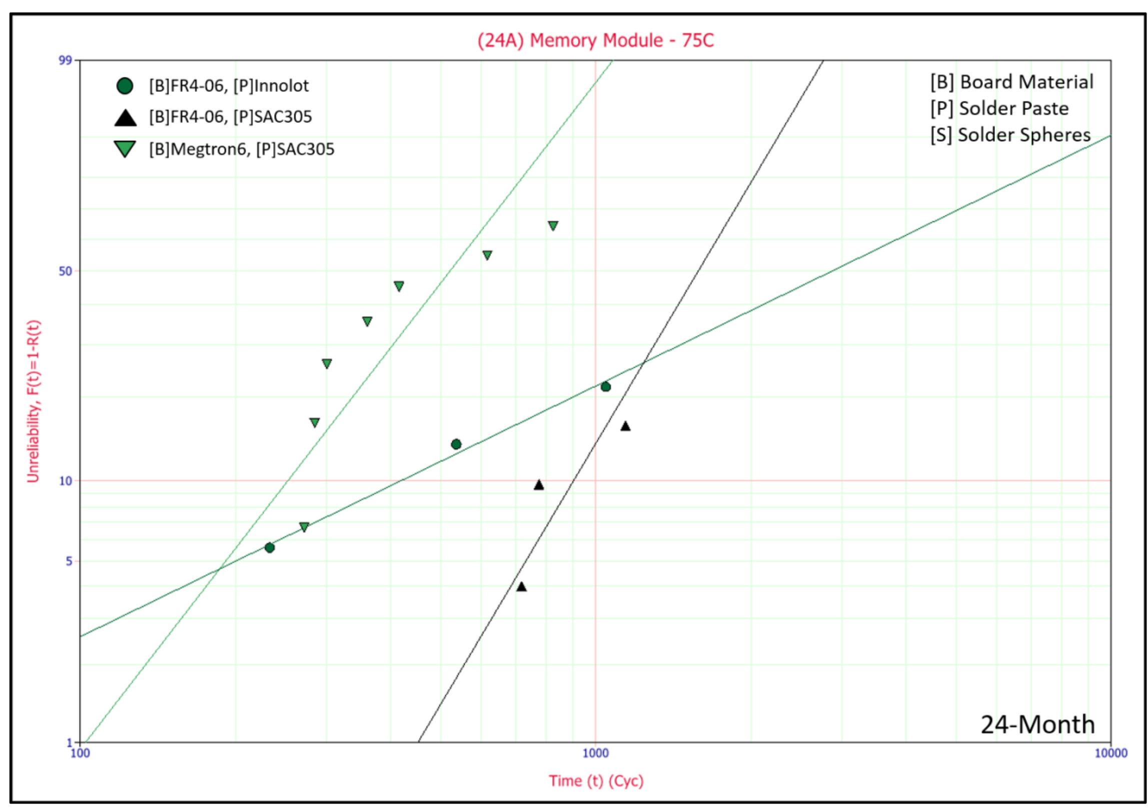


Figure 6.22. All data at 1300 cycles. Memory Module – 24-Month Aging – 75°C.

6.9 PBGA 1156 [35mm, 1.0mm pitch]

The PBGA 1156 is the largest of the cavity-up plastic ball grid array (BGA) components, at 35mm x 35mm, and has a moderate pitch of 1.0mm. This component is found only on the top-side of the TC1-SRJ test vehicle. With a solid 34 x 34 I/O array, the PBGA 1156 has by far the largest I/O count of any component in this experiment.

The PBGA 1156 is the largest cavity-up ball grid array (BGA) component in this test and is one of the slower failing components in the experiment. An additional variable is tested for these components: some PBGA 1156 packages have 'heatsinks' (fin systems) added by hand following the standard assembly process. Reliability data is therefore broken down on the basis of Heatsink vs. No Heatsink, as well as the other variable

already in play. Figure 6.23, below, shows the characteristic life values for PBGA 1156 mounted to the FR4-06 substrate with No Aging.

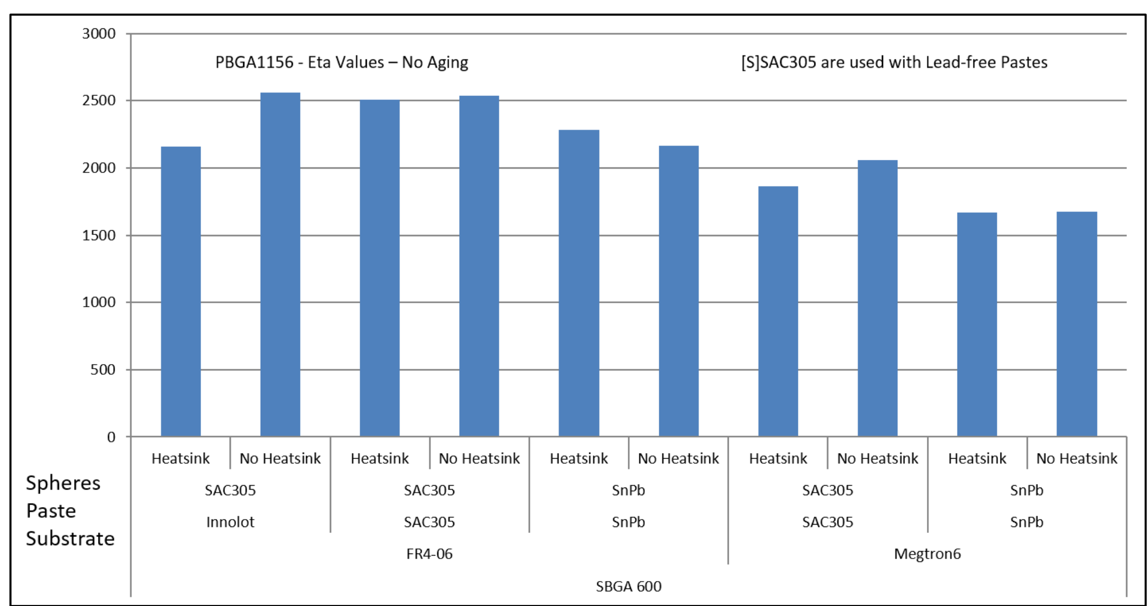


Figure 6.23. Characteristic Life values. PBGA 1156 – FR4-06 – No Aging.

There are several noteworthy trends in the reliability data of the PBGA 1156 package:

- Many early failures occur for packages with the heatsinks attached, with failures occurring later for packages without heatsinks. This appears to be ubiquitously true for the lead-free solders.
- When evaluating performance based on solder sphere composition, this component exhibits the standard trend, with SAC305 solder sphered outperforming SAC105 solder spheres.
- In both the No Aging and 12-Month Aging Groups, this component does not appear to show an improvement with the use of Innolot paste.

- The substrate effect remains the same as that observed for all plastic packages (for which comparison data is available), with the Megtron6 substrate performing worse than the FR4-06.

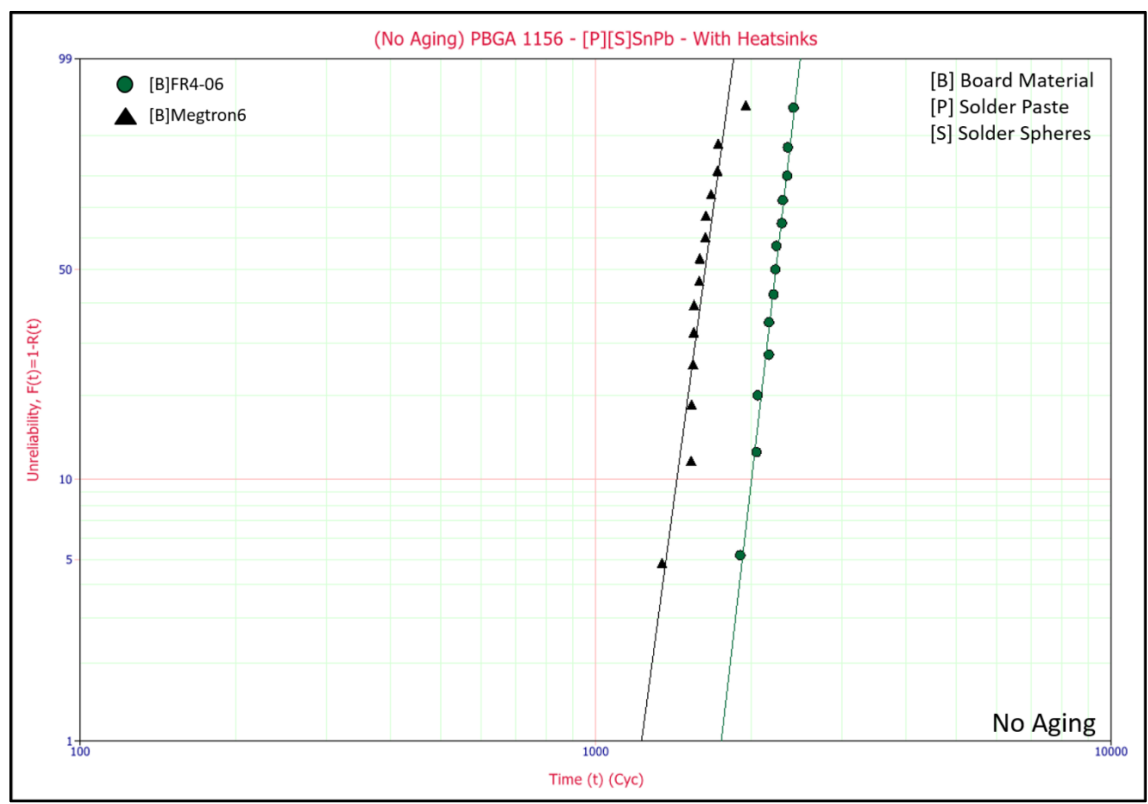


Figure 6.24. Substrate Comparison. PBGA 1156 – [P][S]SnPb – No Aging.

Figure 6.25, below, shows the Weibull graph for key subgroups from the No Aging and 12-Month Aging sets. Note that in after 12 months of aging, the reliability of Lead-Free solder joints is lower than that for SnPb, when considering the actual failure data. All groups show significant degradation.

Figure 6.25. Key groups on FR4-06. PBGA 1156 – No Aging and 12-Month (75°C).

Figure 6.26 shows early failure data available for the PBGA 1156 component in the 24-Month Aging Group. The available data for the 24-Month Aging Group is currently limited to components with SAC105 solder spheres on the FR4-06 substrate. As with previous aging groups, components assembled with heatsinks perform poorly in comparison with those assembled without heatsinks. The Innolot paste also continues to underperform the SAC305 paste for this component at 24-months of aging, based on the available data.

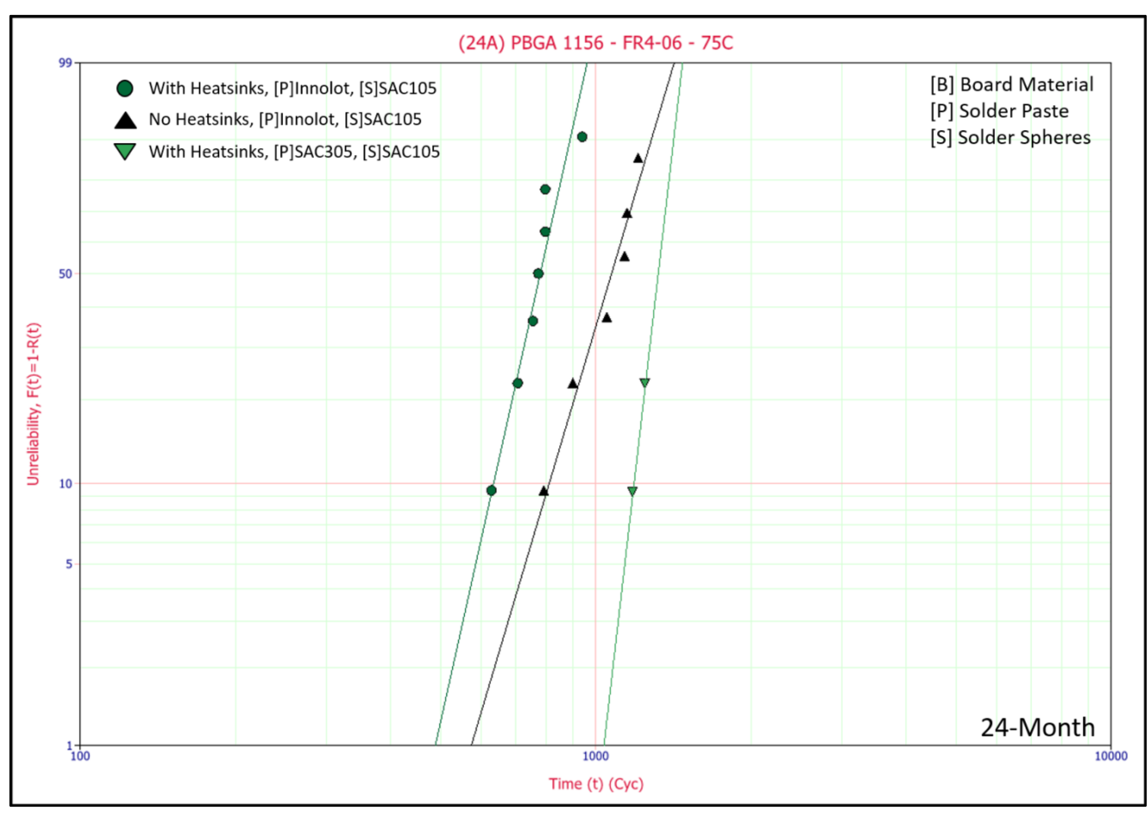


Figure 6.26. All data on FR4-06. PBGA 1156 – 24-Month Aging – 75°C.

6.10 SBGA 304 [31mm, 1.27mm pitch]

The SBGA 304 package is a large-pitch (1.27mm) component found only on the top-side of the TC1-SRJ test vehicle. This metal-capped, cavity-down package has a footprint of 31mm x 31mm. This makes it the third largest component in the experiment, after the SBGA 600 and PBGA 1156.

The SBGA 304 is a metal-capped, cavity-down component design and is therefore mechanically distinct from the previously discussed plastic ball grid array packages. SAC105 solder spheres were unavailable with this component. Figure 6.27 shows the available failure data for the No Aging Group. For No Aging, there were almost no failures on the Megtron6 substrate for this component.

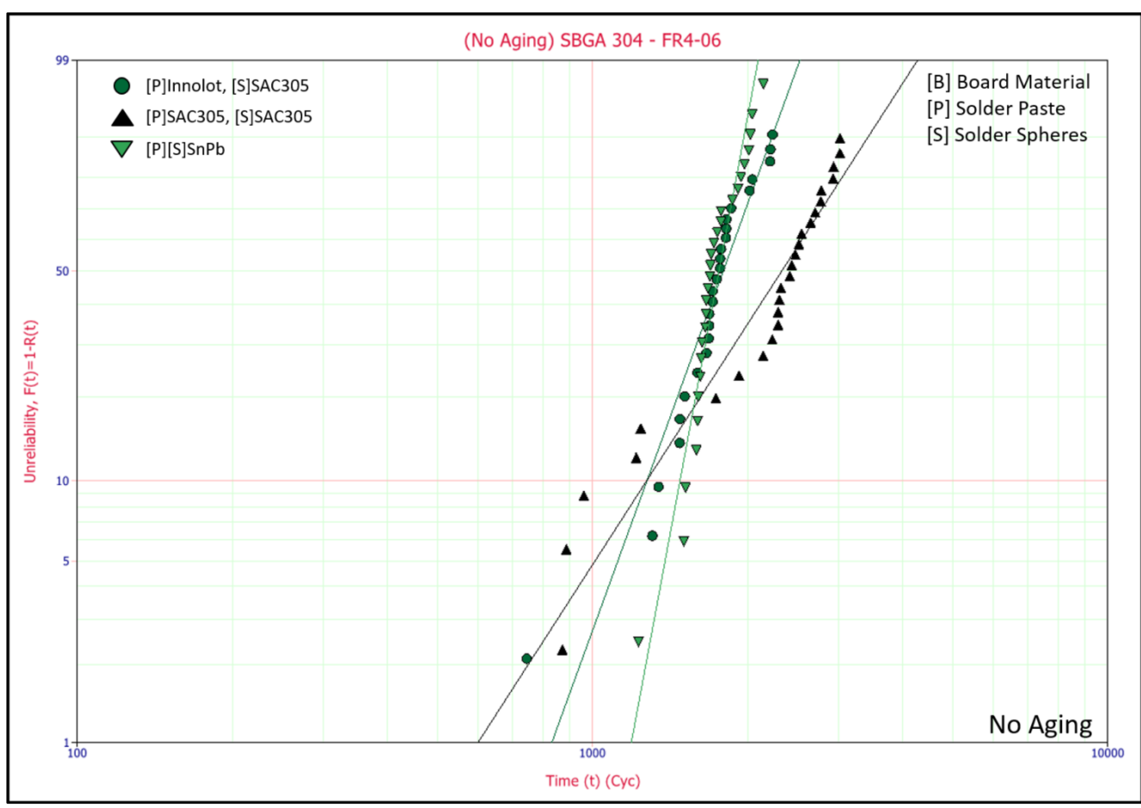


Figure 6.27. SBGA 304 – FR4-06 – No Aging.

There are several noteworthy trends in the reliability data of the PBGA 1156 package:

- The reliability is higher on Megtron6 as compared with FR406. (Insufficient failure data is available to plot for Megtron6 substrates in No Aging Group.) This reverses the trend seen with the plastic packages (all of which have smaller pitch).
- Additionally, Innolot paste underperforms SAC305 paste with SAC305 packages, which contradicts the trend from the smaller packages.

However, it should be noted that overall reliability of this package is higher in all cases than that of the smaller plastic BGAs, so overall system reliability should be judged on basis of improvements to the reliability of the smaller packages, which is observed with Innolot Paste.

Figure 6.28, below, shows the reliability data for key subgroups from the No Aging and 12-Month Aging sets. Although degradation occurs, the matched SAC305 solder continues to perform better than the SnPb control after 12 months of aging.

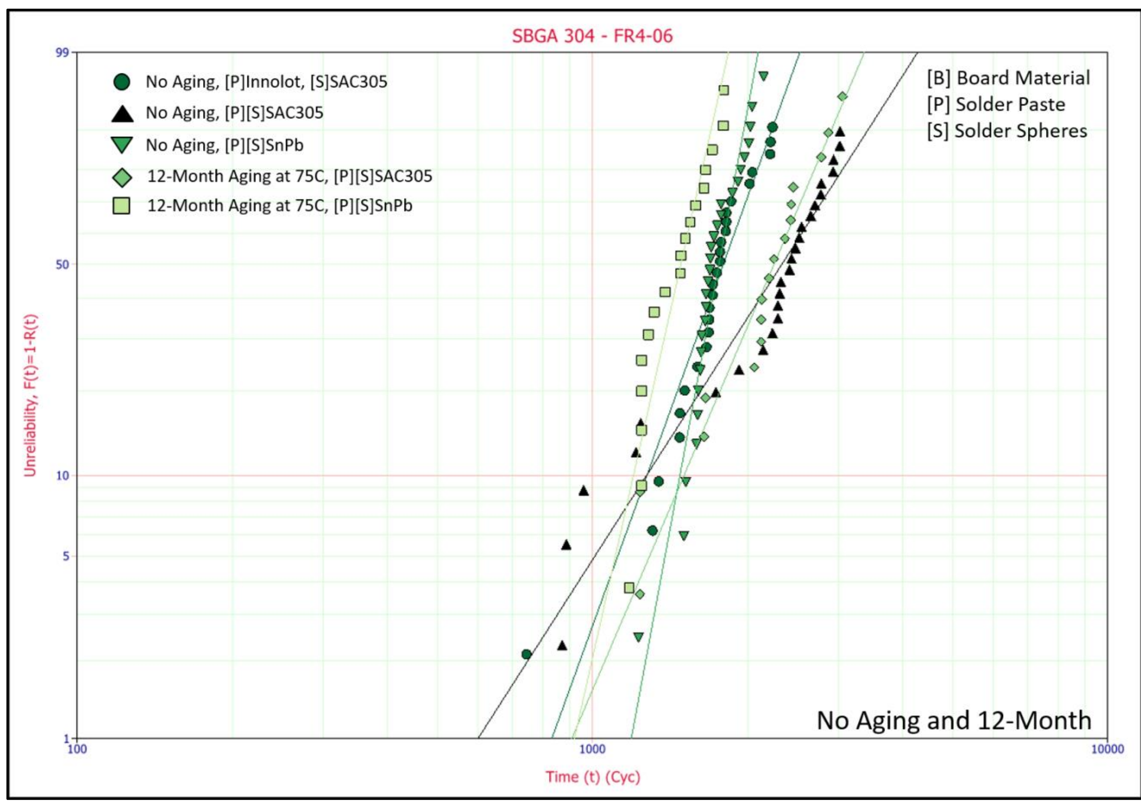


Figure 6.28. Weibull Plot: SBGA304 – No Aging and 12-Month (75°C)

6.11 SBGA 600 [45mm, 1.27mm pitch]

The SBGA 600 component has the largest footprint in this experiment (45mm x 45mm), and is found solely on the top-side of the TC1-SRJ test vehicle. Like the SBGA 304, this is a metal-capped, cavity-down package with large pitch (1.27mm).

The SBGA 600 component, like the SBGA 304, is a metal-capped, cavity-down design and is therefore mechanically distinct from the previously discussed plastic ball grid array packages. An additional variable is tested for these components: some PBGA 1156 packages have 'heatsinks' (fin systems) added by hand following the standard

assembly process. Reliability data is therefore broken down on the basis of Heatsink vs. No Heatsink, as well as the other variable already in play.

Figure 6.29 shows the Characteristic Life values for the SBGA 600 package with No Aging. The failure trends for the SBGA 600 component have been consistent across all aging groups, based on currently available data. Specifically:

- Early failures are for packages with the heat-sinks attached, with failures occurring later for packages without heat-sinks.
- The failures in the SBGA metal-capped packages reverse the substrate failure trends seen for the plastic packages: failures take place first on the FR4-06 substrate, and are seen later on the Megtron6 substrate.
- As with the SBGA 304, Innolot paste underperforms SAC305 paste with SAC305 packages, which contradicts the trend from the smaller packages.

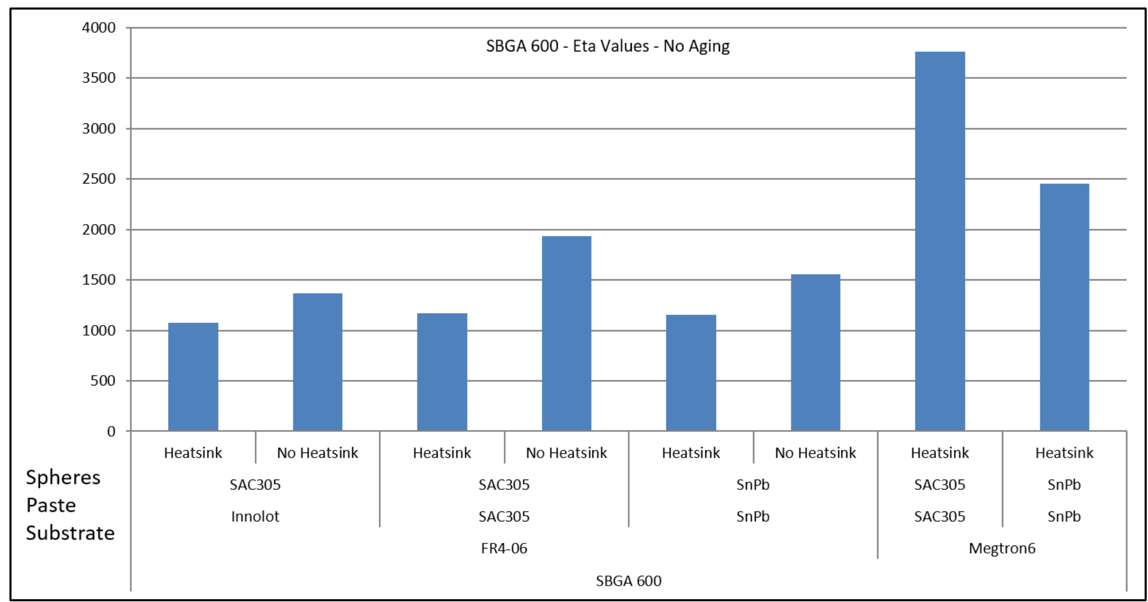


Figure 6.29. Characteristic Life values. SBGA 600 – FR4-06 – No Aging.

Figure 6.30, below, shows the Substrate Comparison for matched SnPb components with Heatsinks. Note that for this component, the substrate trend observed

with the standard plastic BGA packages is reversed. Here, failures occur first on the FR4-06 substrate, and are seen later on the Megtron6 substrate.

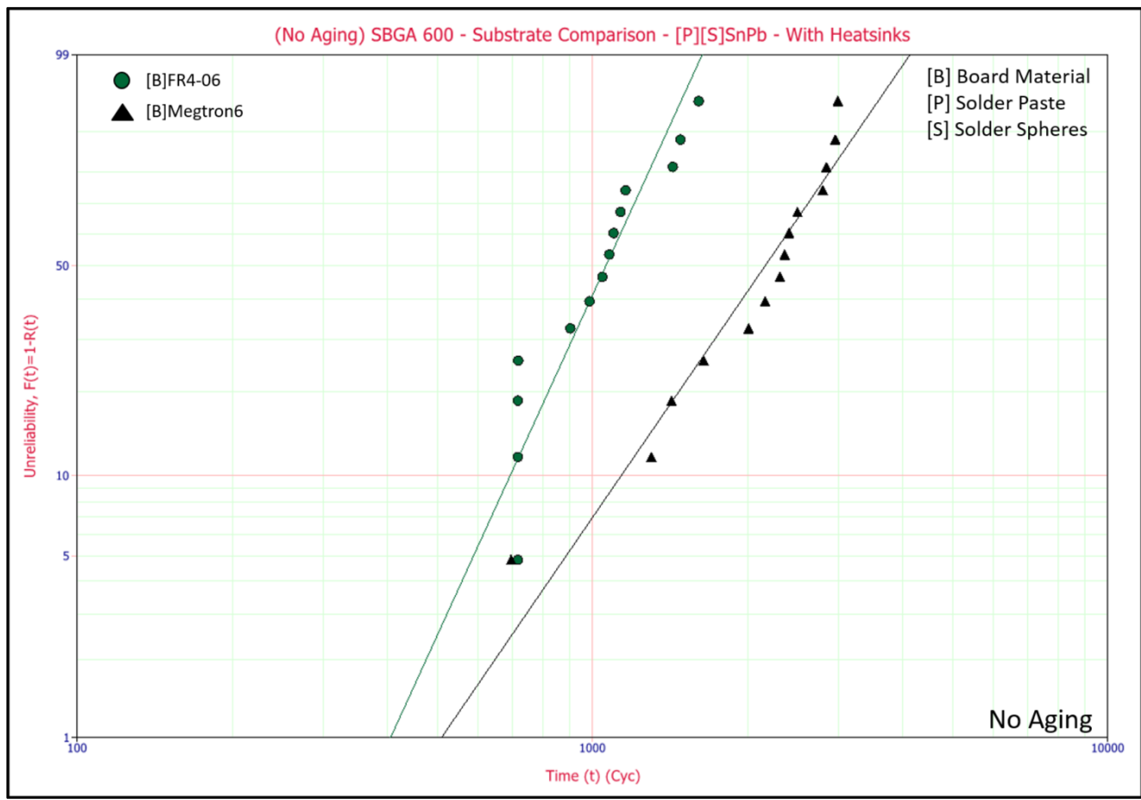


Figure 6.30. Substrate Comparison. SBGA 600 – No Aging – [P][S]SnPb.

Figure 6.31, below, shows available failure data for the SBGA 600 component in the 12-Month Aging Group. SAC305 continues to outperform the SnPb control after 12 months of aging.

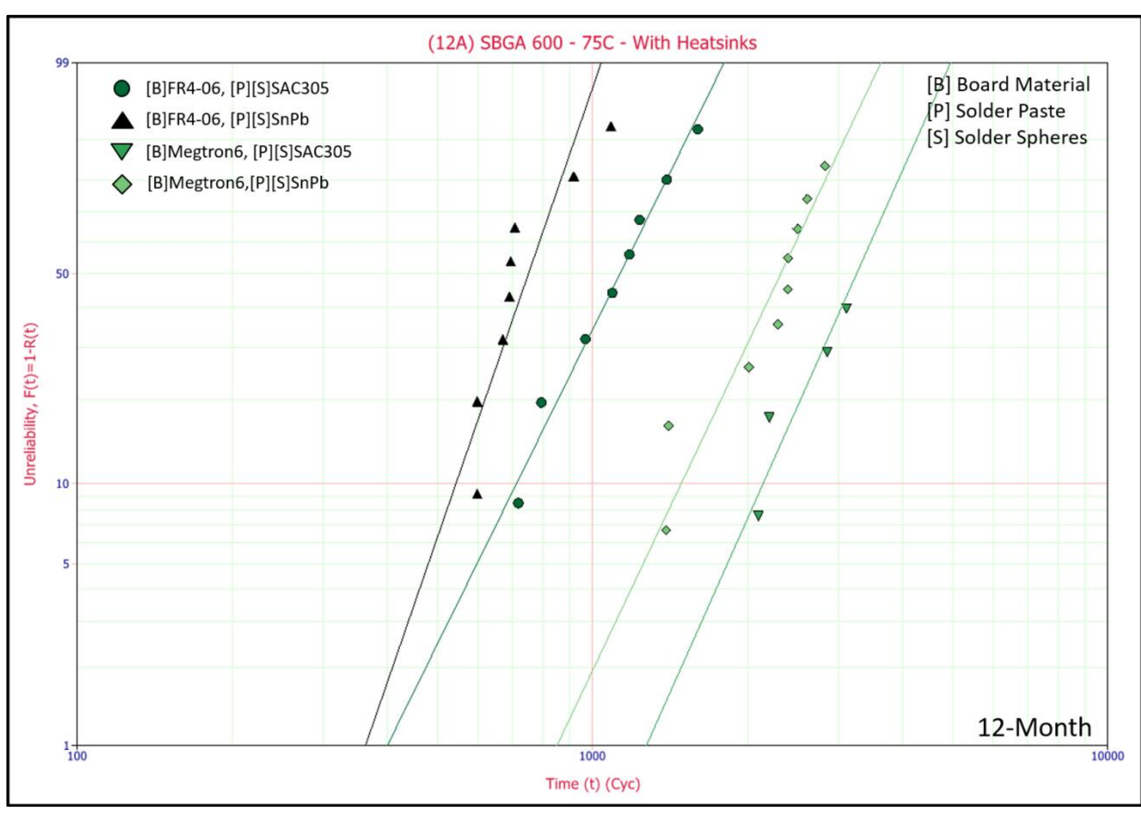


Figure 6.31. SBGA 600 – FR4-06 – With Heatsinks – 12-Month Aging – 75°C.

Figure 6.32 shows new failure data for the SBGA 600 component in the 24-Month Aging Group. As with previous aging groups, for this package early failures occurred on the FR4-06 substrate, and for components with Heatsinks attached. The matched SnPb and matched SAC305 curves appear to cross-over; however, more data is desirable to confirm this result. The slope of the SnPb distribution is lower than that typically observed. The other interesting trend is that Innolot paste appears to continue to underperform SAC305 paste for the available 24-Month aging data.

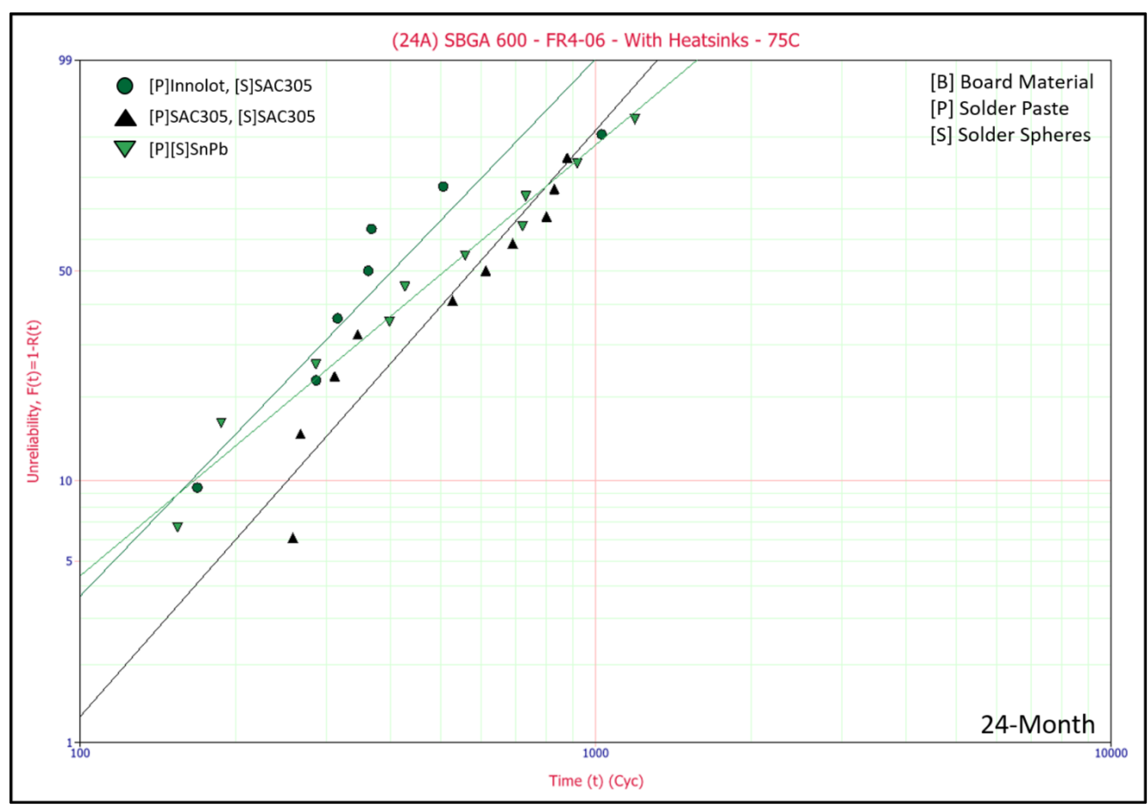


Figure 6.32. SBGA 600 – FR4-06 – With Heatsinks – 24-Months Aging – 75°C.

Chapter 7
Failure Analysis Results

7.1 Failure Analysis

Cross-sectioning is one of the most common methods of destructive failure analysis used in assessing electronic solder joints. These techniques are adapted from typical metallurgical analysis methods. To allow examination of its microstructure, a specimen must first undergo a multi-step sample preparation process. The basic steps in metallurgical sample preparation are 1) Sectioning, 2) Mounting, Grinding, Polishing, Etching (optional, depending on specimen type) [57]. Once a specimen has been prepared for study, it can be examined using optical or electron microscopy. Here, Cross-Sectional Measurements on representative solder balls are shown including:

- SEM (Scanning Electron Microscope) SE (Secondary Electron) Images
- SEM (Scanning Electron Microscope) SE (Back-scattered Electron) Images
- EDS (Energy Dispersive Spetrometry) Points-of-Interest and Maps
- IMC (Intermetallic Compound) thickness measurements

7.2 Preliminary Failure Analysis: FR4-06 Substrates

Sets of FR4-06 substrate test vehicles were pulled following isothermal aging and at intervals of 1000 cycles during the thermal cycle testing (i.e. at cycle counts of 0, 1000, 2000, and 3000 cycles). Due to the number of boards available and other factors, only the following subgroups were sampled in this manner: SAC305-paste boards (25°C, 50°C, and75^{o}C) and Innolot-paste boards (75°C). The cross-sectional images in this section are

from samples in the No Aging group and represent the currently known failure modes for components mounted to the FR4-06 substrate.

7.2.1 FR4-06: No Aging Group (0 Cycles)

Test samples for this group were prepared in conjunction with Pace Technologies as the protocol for cross-sectioning outlined in the Section 5.6.4 was being developed with their input. Note that these samples were Gold coated, rather than Carbon coated, which will affect the observed EDS values. These samples were also hot-mounted using phenolic resin, whereas subsequent samples are all cold-mounted using a two-part epoxy system. A number of grinding/polishing procedures were tested, as outlined below.

Procedure 1:

- SiC 320 grit until plane.
- SiC 600 grit for 1 min.
- SiC 800 grit for 1 min.
- SiC 1200 grit for 1 min.
- 1-micron Polycrystalline diamond suspension on an Atlantis pad for 4 mins.

Procedure 1 produced samples that had large/obvious scratches remaining, as well as residual carbon residue. The carbon inclusions are attributable to imbedded SiC particles (from the grit paper) that were not properly removed from the sample surface during polishing. The quality of samples from this polishing procedure was deemed to be inadequate.

On the printed circuit board (PCB) side, there is a very thin coating of OSP surface finish over the PCB copper lands. For the ‘as received’ (as-reflowed) test vehicles

with SAC305 solder, the Cu-Sn Intermetallic Compound thickness was found to be ~5 microns thick on the board-side. On the component-side (package-side), there is a nickel cladding layer (~8 microns) and a thin (~0.05 micron) gold “flash” that dissolves into the solder during reflow, backed by the component copper pad. The (Ni,Cu)-Sn IMC layer on the component-side is more difficult to measure accurately, as it has a scalloped (rather than planar) interface. However, this IMC layer appears to be ~3 microns thick (on average) as-reflowed. The existence of a high amount of Copper at this interface indicates that it has either diffused through the Nickel cladding layer or segregated to the interface from the bulk solder.

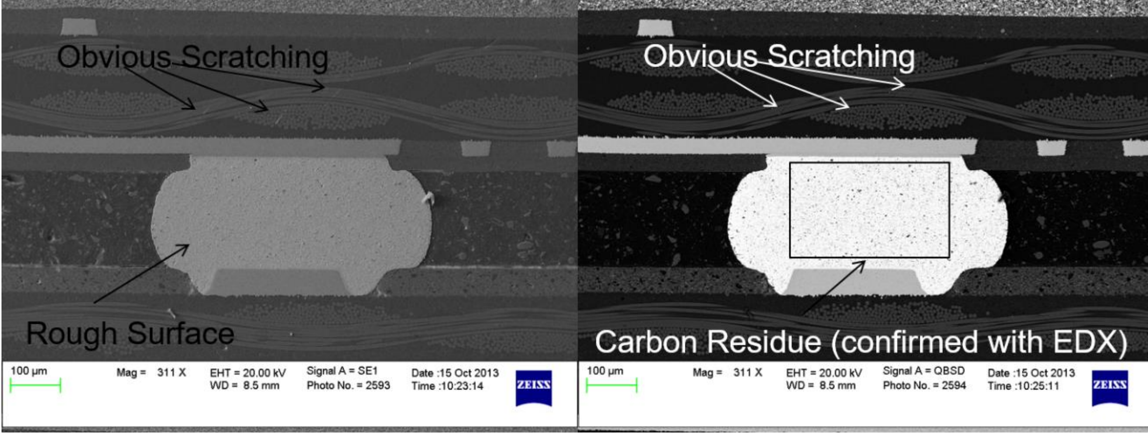


Figure 7.1. SE (left) and BSE (right) micrographs, Polishing Procedure 1.

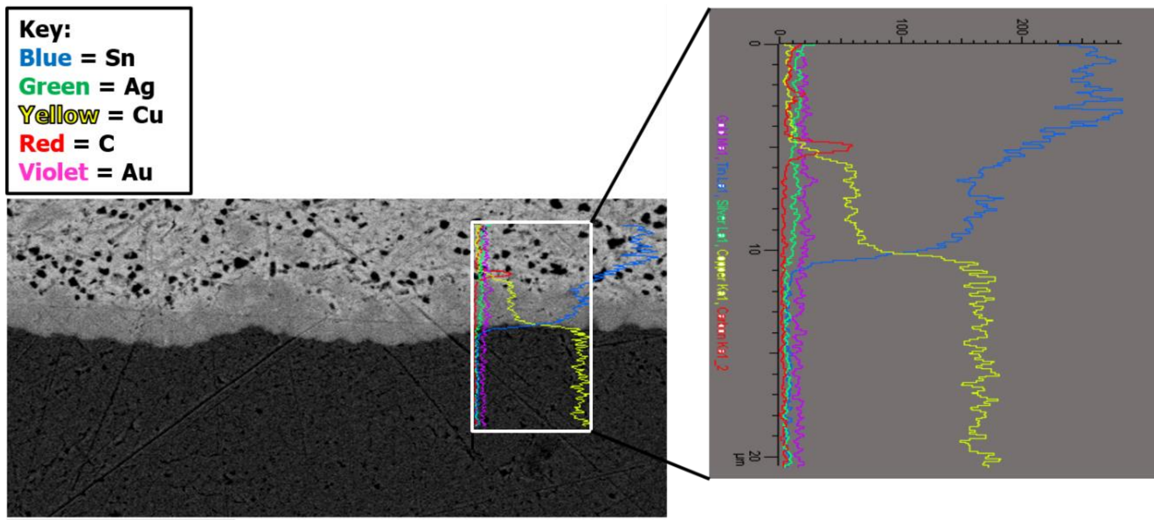


Figure 7.2. EDS Line Scan, Polishing Procedure 1, PCB-Side IMC Layer.

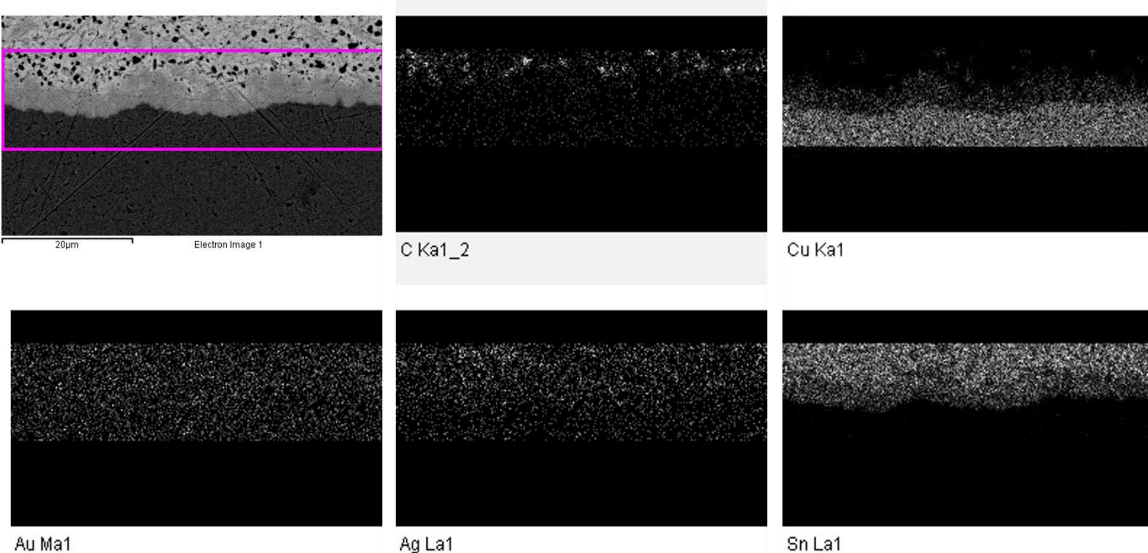


Figure 7.3. EDS MAPS, Polishing Procedure 1, PCB-Side IMC Layer.

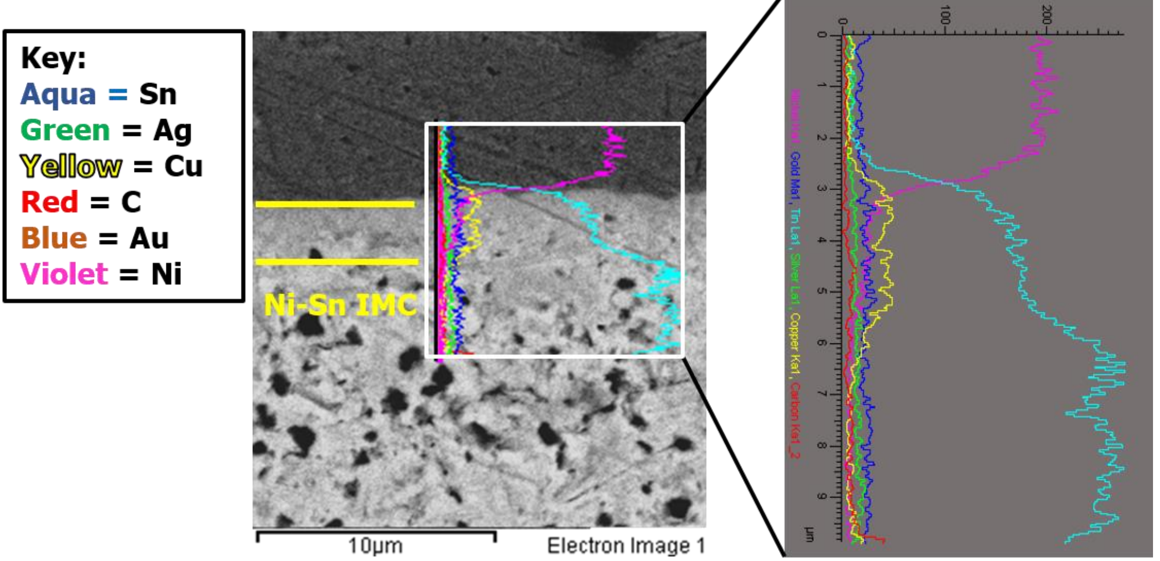


Figure 7.4. EDS Line Scan, Polishing Procedure 1, Component-Side IMC Layer.

Procedure 2:

- SiC 320 grit until plane.
- SiC 600 grit for 1 min.
- SiC 800 grit for 1 min.
- SiC 1200 grit for 1 min.
- 0.05-micron alumina suspension on an Atlantis pad for 4 mins.

Procedure 2 produced samples that had large/obvious scratches remaining, as well as residual carbon residue. The carbon inclusions are attributable to imbedded SiC particles (from the grit paper) that were not properly removed from the sample surface during polishing. This particular sample also suffered from (unrelated) resin voiding issues. The quality of samples from this polishing procedure was deemed to be inadequate.

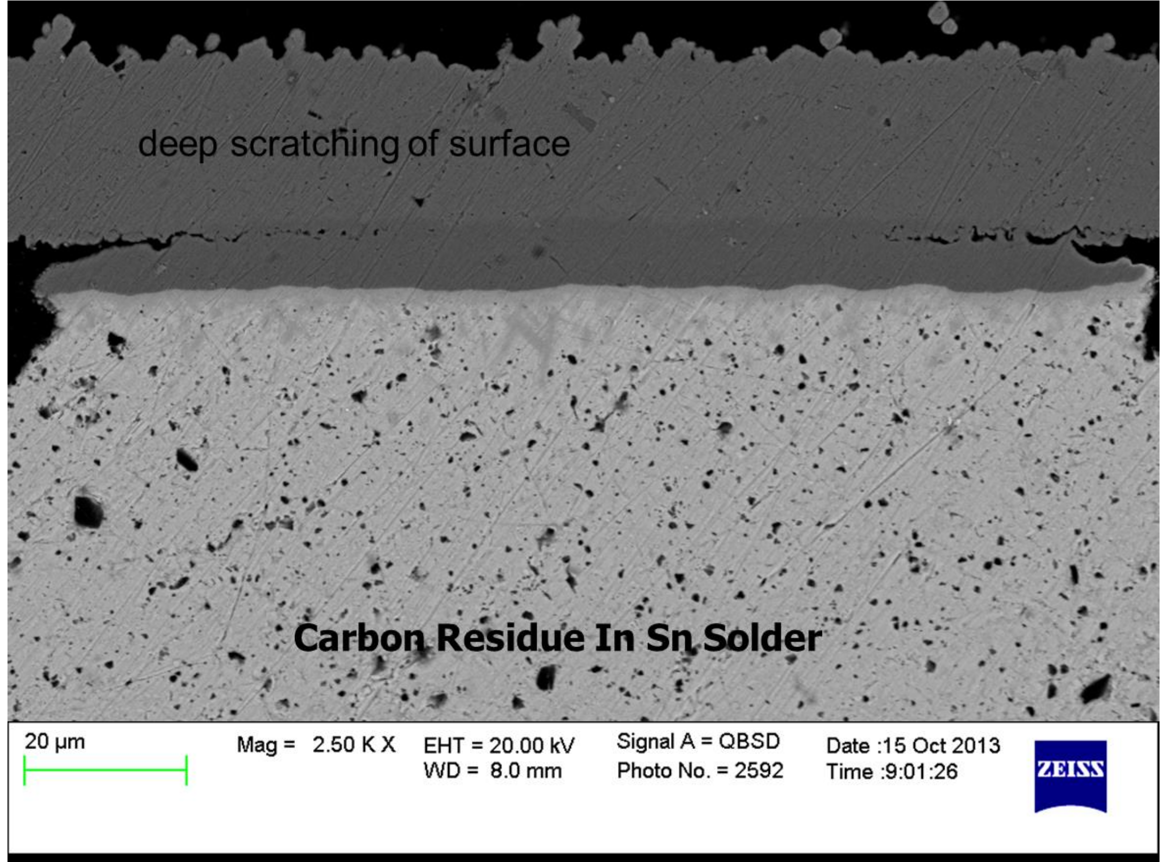


Figure 7.5. BSE micrograph, Polishing Procedure 2.

Procedure 3:

- SiC 320 grit until plane.
- SiC 600 grit for 1 min.
- SiC 800 grit for 1 min.
- SiC 1200 grit for 1 min.
- 0.05-micron alumina suspension on an Atlantis pad for 4 mins.
- Vibratory polishing for 45 minutes.

Procedure 3 produced samples that had a few large/obvious scratches remaining, but with mostly well-polished surfaces. The residual carbon residue seen with the previous polishing procedures is absent. This particular sample also suffered from

(unrelated) resin voiding issues. The quality of samples from this polishing procedure was deemed to be adequate. However, the vibratory polishing was not feasible due to equipment limitations (need for a vibratory polishing machine) and throughput concerns. It was therefore replaced in subsequent cross-sections with a two-step (rough/fine) polishing procedure (1-micron alumina/0.05-micron alumina).

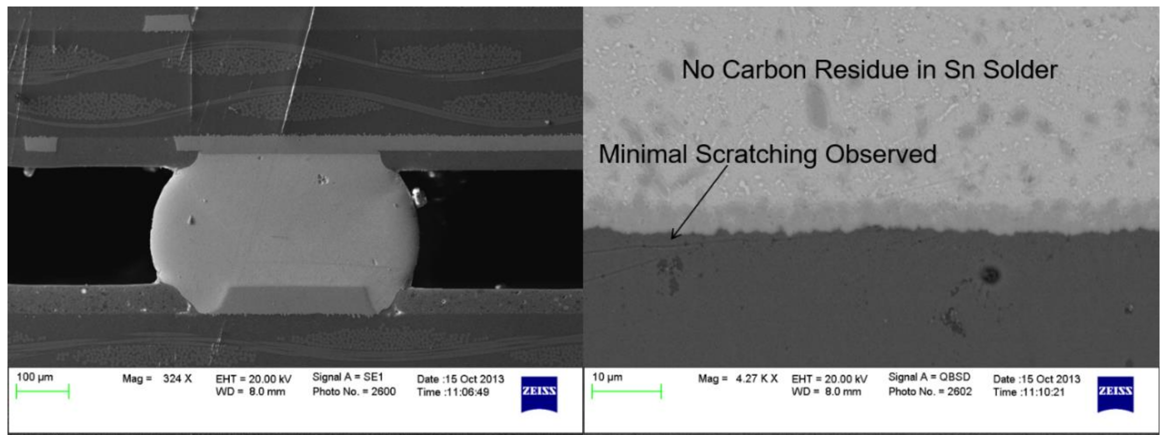


Figure 7.6. SE (left) and BSE (right) electron micrographs. Polishing Procedure 3.

7.2.2 FR4-06: No Aging Group (1000 Cycles)

Additional samples were prepared at 1000 thermal cycles (No Aging Group) for SAC305- and Innolot-paste boards. The new polishing protocol was finalized and enabled the elimination of most Silicon Carbine imbedded particles without relying on a lengthy final vibratory polishing step. At 1000 cycles, no crack propagation was observed in these samples. Figures 7.7, below, shows the board- and component-side SEM micrographs for a 1000 cycle SAC305 sample.

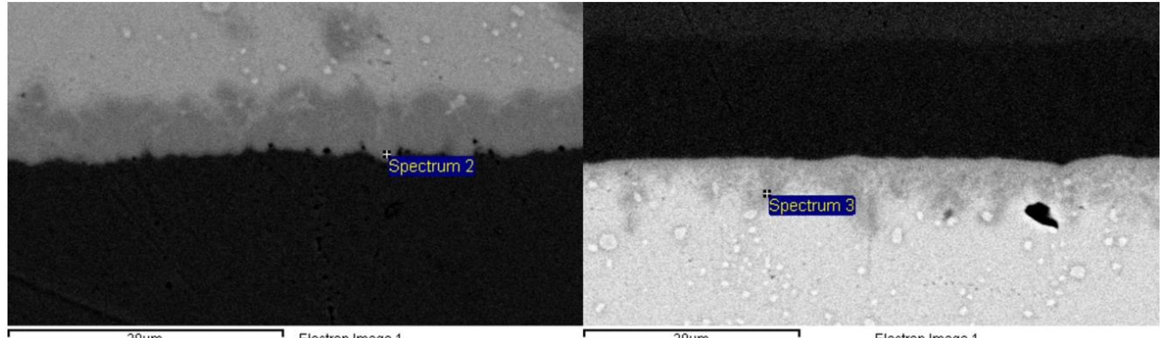


Figure 7.7. Board- (left) and Component-Side (right) IMC, SAC305, 1000 TCs.

IMC Thickness is ~5 microns for both sides, but the IMC layer is much more variable at the component-side, and EDX analysis shows that the IMC there is still developing. The board-side initial Cu-Sn IMC is Cu_6Sn_5. Figures 7.8, below, shows the board- and component-side SEM micrographs for a 1000 cycle Innolot sample. IMC layers here are very similar to SAC305.

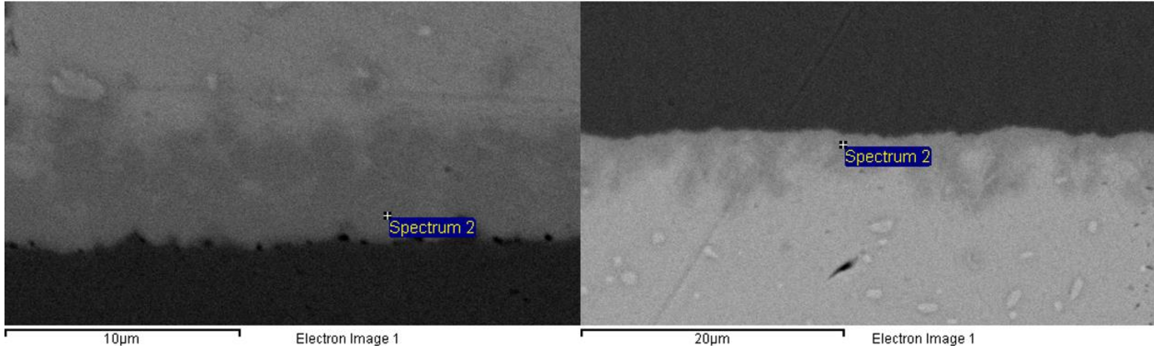


Figure 7.8. Board- (left) and Component-Side (right) IMC, Innolot, 1000 TCs.

7.2.3 FR4-06: No Aging Group (2000 Cycles)

Additional samples were prepared at 2000 thermal cycles (No Aging Group) for SAC305- and Innolot-paste boards. Figure 7.9, below, shows a SE micrograph overview of three solder joints which are typical of this set, from a SAC305 board.

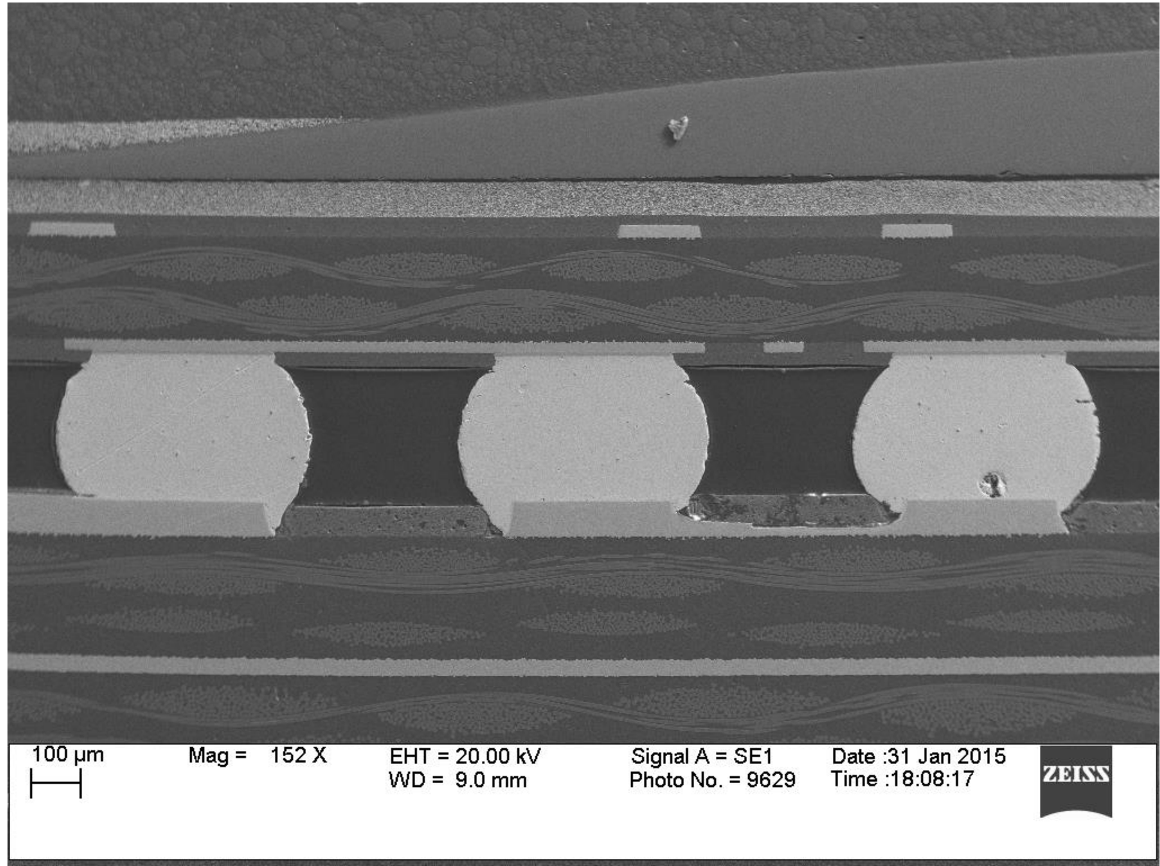


Figure 7.9. Overview SE Micrograph showing Characteristic Solder Joints.

Figure 7.10, below, shows the board- and component-side SEM micrographs for a 2000 cycle SAC305 sample. Micro-cracking and some micro-voiding (porosity) can be observed.

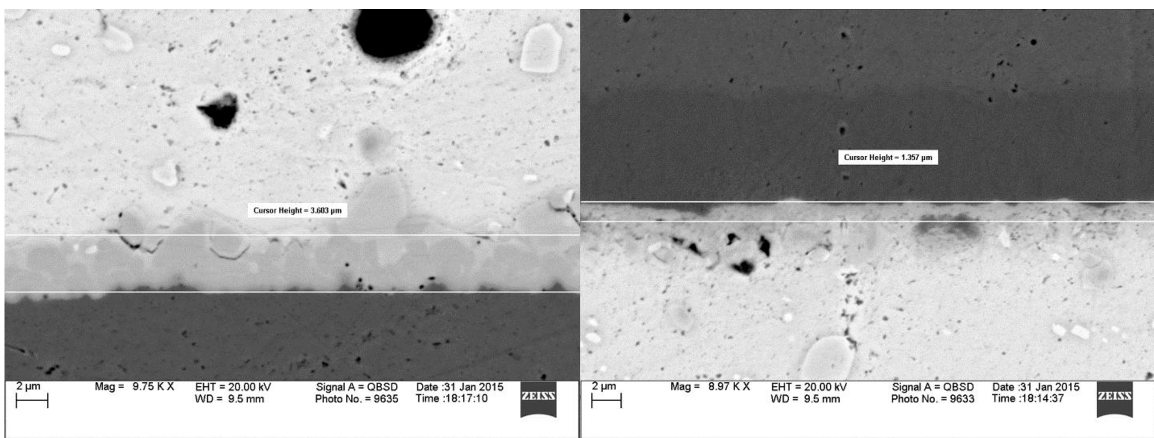


Figure 7.10. Board- (left) and Component-Side (right) IMC, SAC305, 2000 TCs.

Some crack propagation can be observed at 2000 cycles. More crack initiation is observed at the board-side than at the component-side for these samples. Some joints exhibit roughly equivalent cracking at both the board- and component-side, as shown in Figure 7.11.

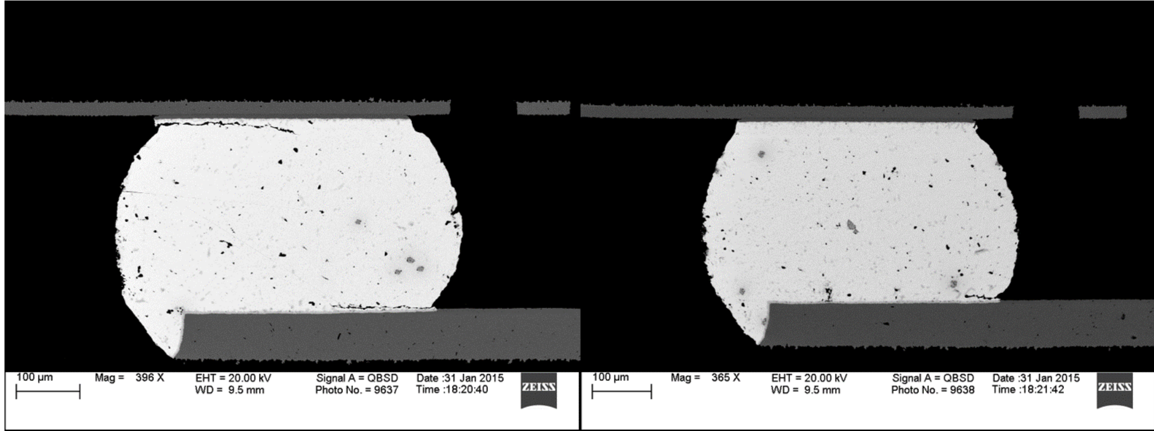


Figure 7.11. Roughly equivalent cracking (left); crack initiation at board-side (right).

7.2.4 FR4-06: No Aging Group (3000 Cycles)

Additional samples were prepared at 3000 thermal cycles (No Aging Group) for SAC305- and Innolot-paste boards. Figure 7.12, below, shows a BSE micrograph overview of three solder joints from a SAC305 board.

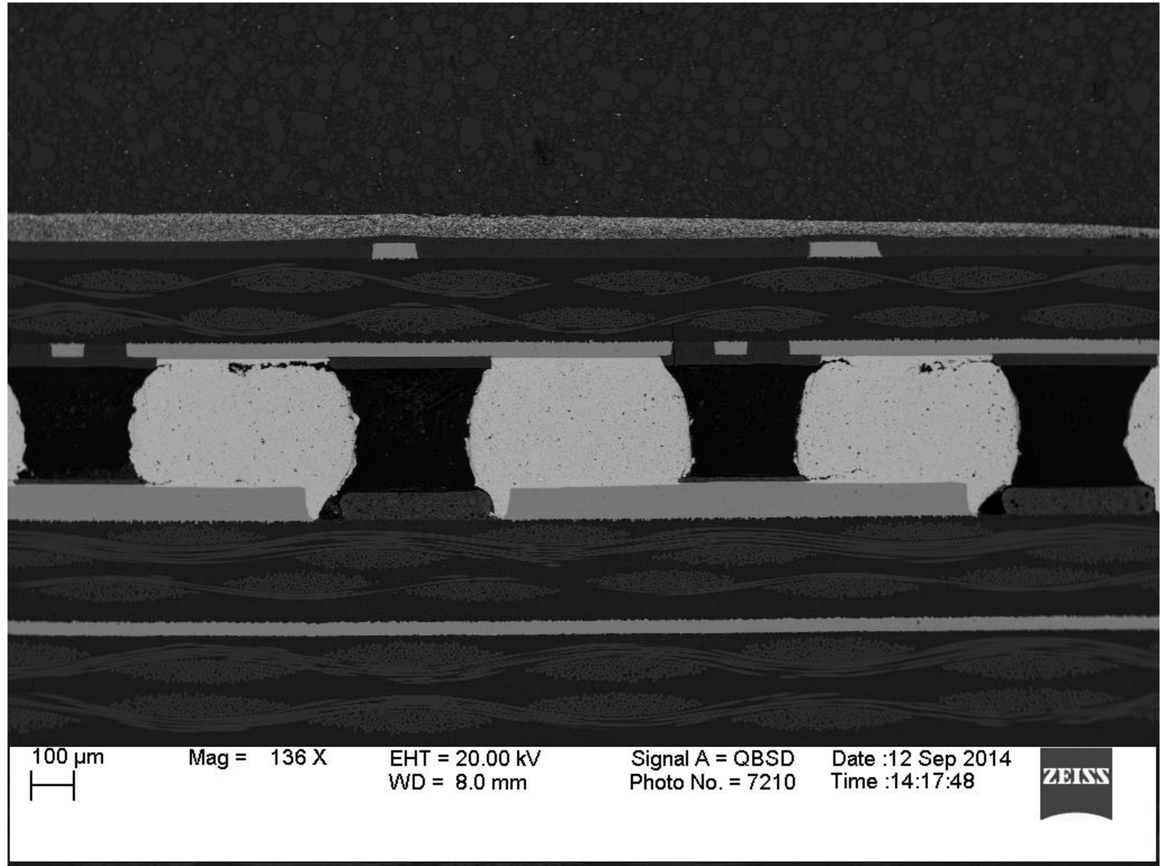


Figure 7.12. Overview SE Micrograph showing Characteristic Solder Joints.

A variety of crack propagation modes can be observed for the SAC305 solder joints at 3000 cycles. Figure 7.13 shows dominant Board-Side cracking (top to images), roughly equivalent cracking at Board-Side and Component side (bottom-left) and crack initiation at board-side (bottom-right). More crack initiation is observed at the board-side that at the component-side for these samples.

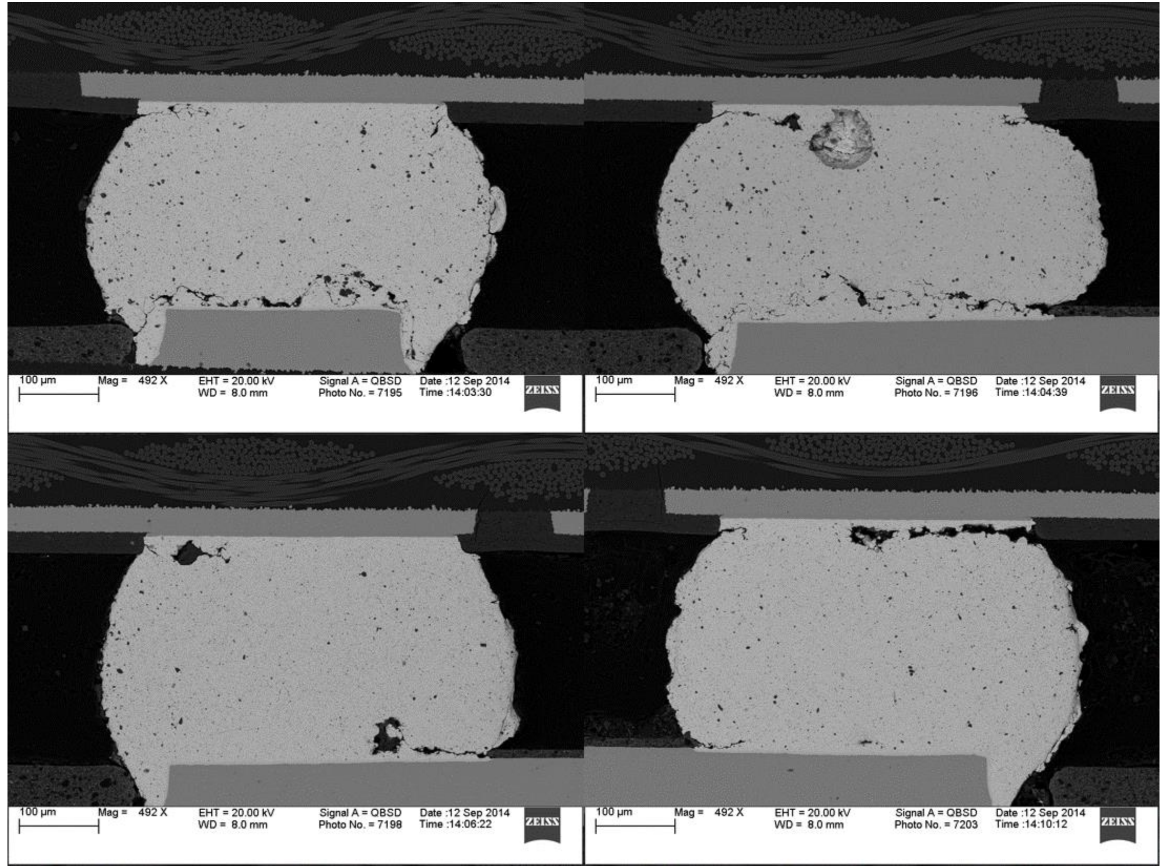


Figure 7.13. A variety of crack propagation modes, SAC305-paste.

Figure 7.14, below, shows a BSE micrograph overview of three solder joints which display the most common failure characteristics observed from an Innolot-paste board.

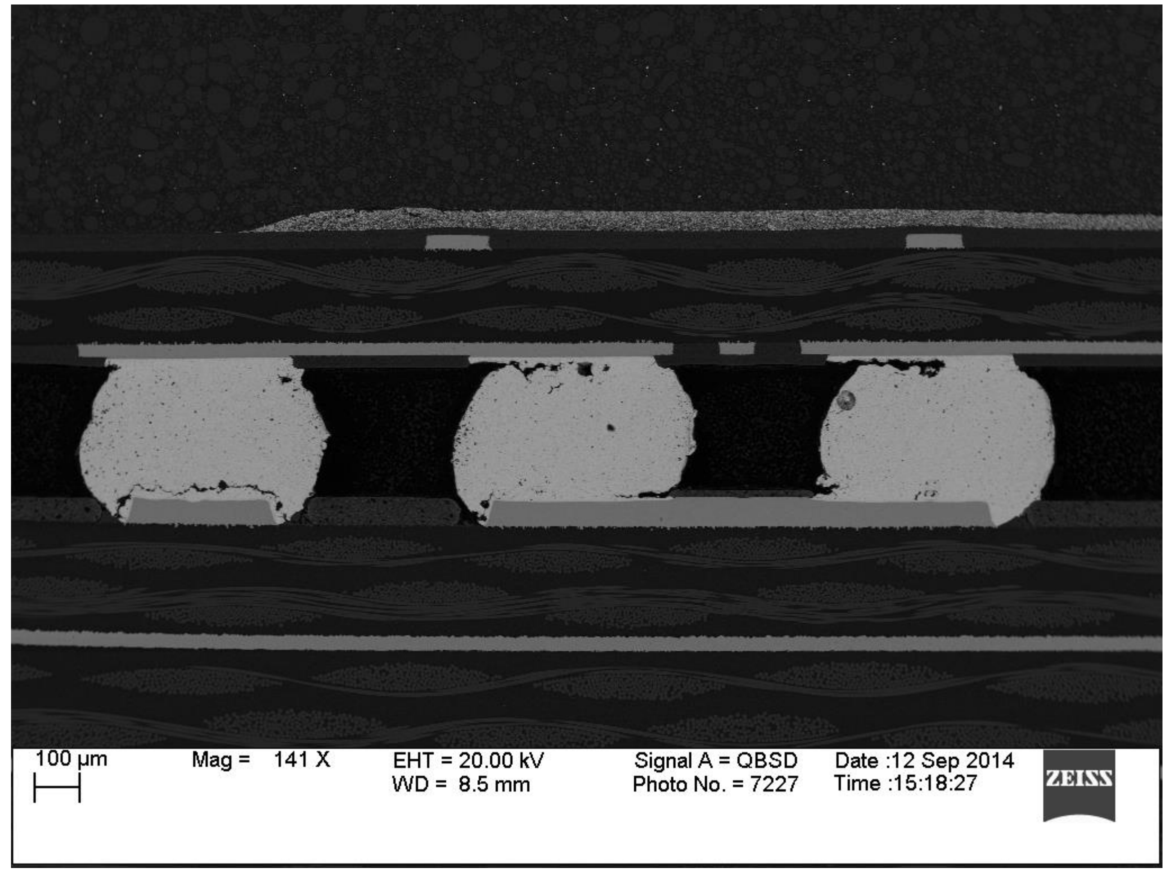


Figure 7.14. Overview SE Micrograph showing Characteristic Solder Joints.

A variety of crack propagation modes can be observed for the Innolot solder joints at 3000 cycles, as shown in Figure 7.15. Crack initiation is observed at the board-side and the component-side without apparent strong preference in these samples.

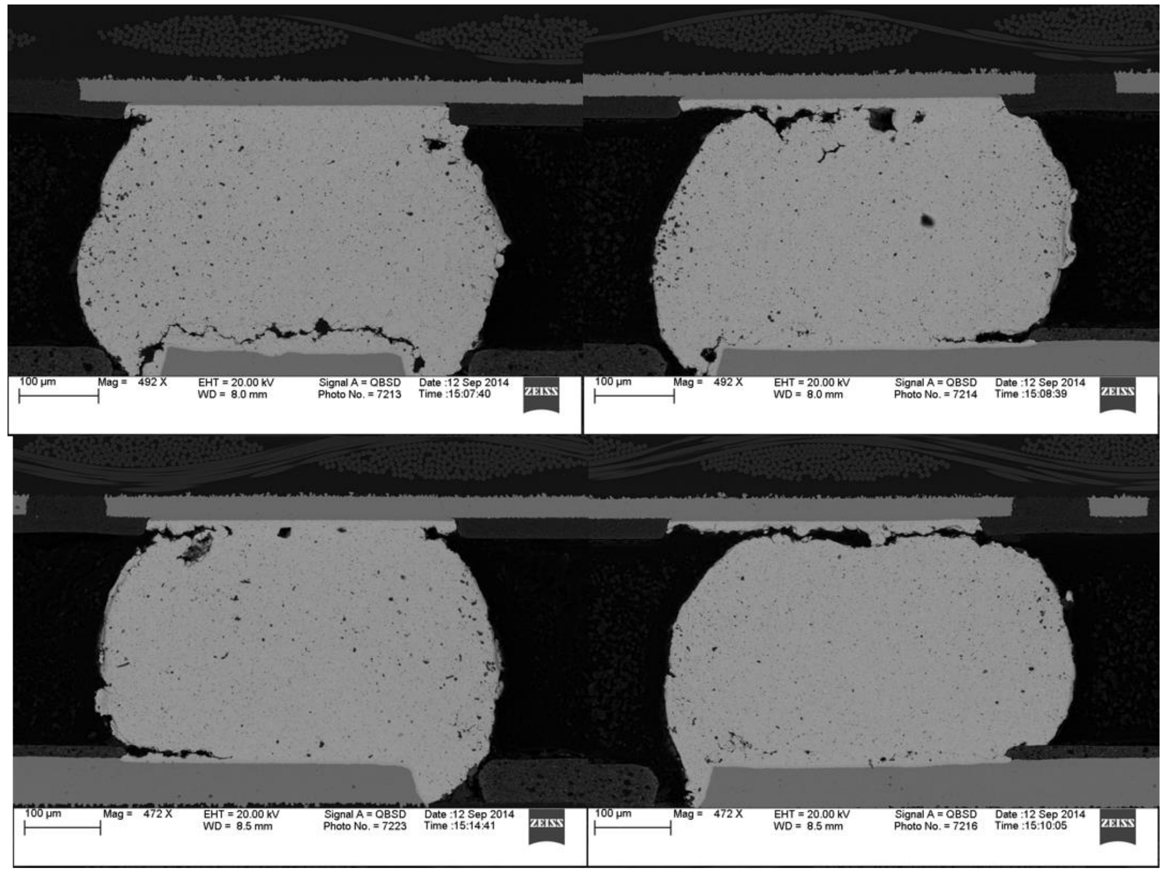


Figure 7.15. A variety of crack propagation modes, Innolot-paste.

7.3 Preliminary Failure Analysis: Megtron6, No Aging, 3000 Cycles

Because of limitations on the number of test boards, it was infeasible to 'pull' Megtron6 substrate test boards for Materials and Failure Analysis while the test was running. This is particularly problematic because of key reliability trends observed – namely that the plastic ball grid array (BGA) packages have superior reliability on the FR4-06 substrate than on the Megtron6 substrate (with this trend reversing itself for the metal-capped packages). The cross-sectional images in this section are from samples in the No Aging group and represent the currently known failure modes for components mounted to the Megtron6 substrate.

7.3.1 Megtron6: CABGA 208, [P]SAC305, [S]SAC105

Figure 7.16, below, shows a BSE micrograph overview of three solder joints which display the most common failure characteristics observed. This sample (and others in this set) displays a variety of failure modes not seen so far in our No Aging failure analysis. Further samples representing the full range of test factors need to be cross-sectioned and analyzed before we determine if these failure modes are common to other test groups or represent a unique failure type on Megtron6 substrate.

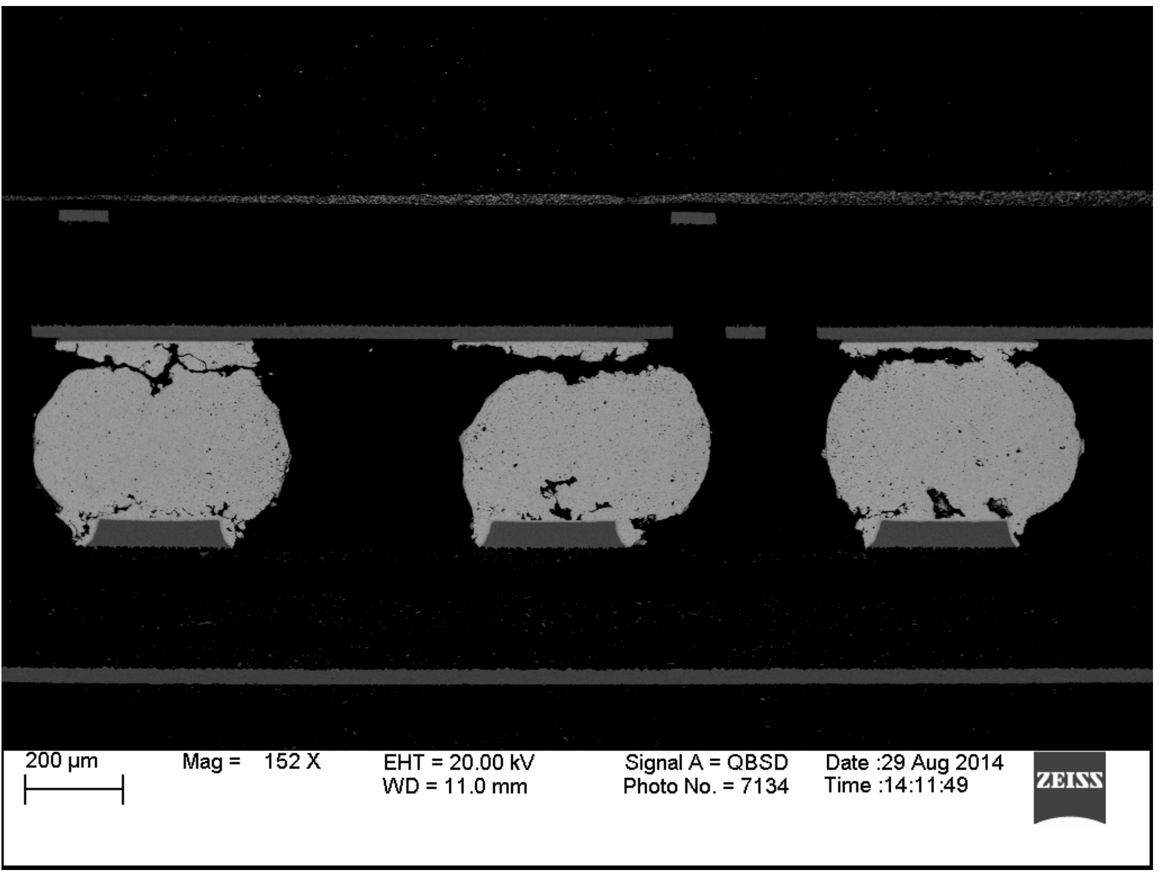


Figure 7.16. Overview BSE Micrograph showing Characteristic Failure Modes.

There are different failure modes observed than in the FR4-06 samples. Namely, the joints fail fully across the top (component-side), with secondary cracks appearing at the bottom (board-side) of the joint. The board-side cracks, however, do not fully cross/compromise the joint. In should be noted that in some joints, the component-side

cracks are close to the IMC (intermetallic compound) layers while in other cases they move through areas of the “bulk” solder in a form that may indicate dynamic recrystallization driven failures.

However, not all joints within this sample display the same failure mode. Figure 7.17 shows roughly equivalent cracking at top and bottom sides of the same joint whereas Figure 7.18 shows failure across the bottom (board-side) of the joint with only secondary smaller cracks occurring at the top (component-side). At this late date (3000+ cycles) it is difficult to determine which mode of joint failure led to the initial failure of the overall package.

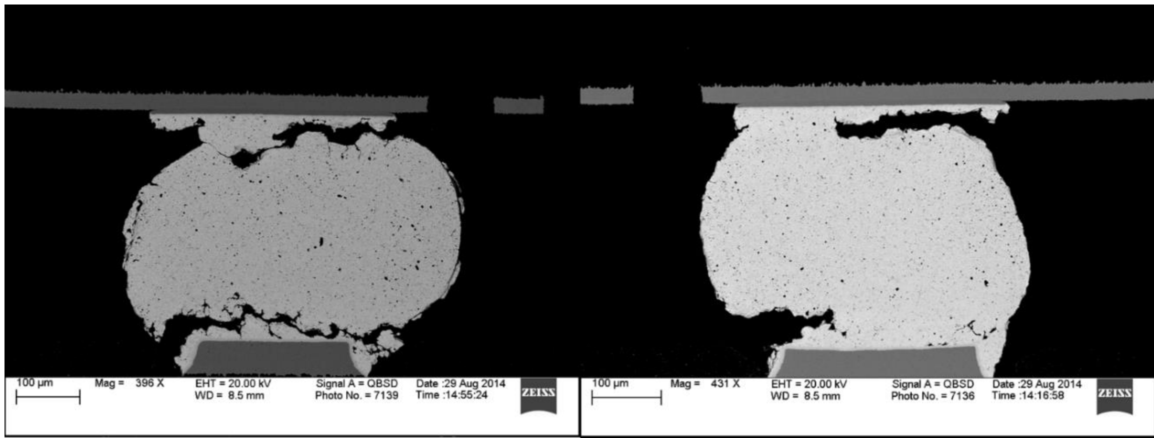


Figure 7.17. Roughly equivalent cracking at Board/Component-Side of two joints.

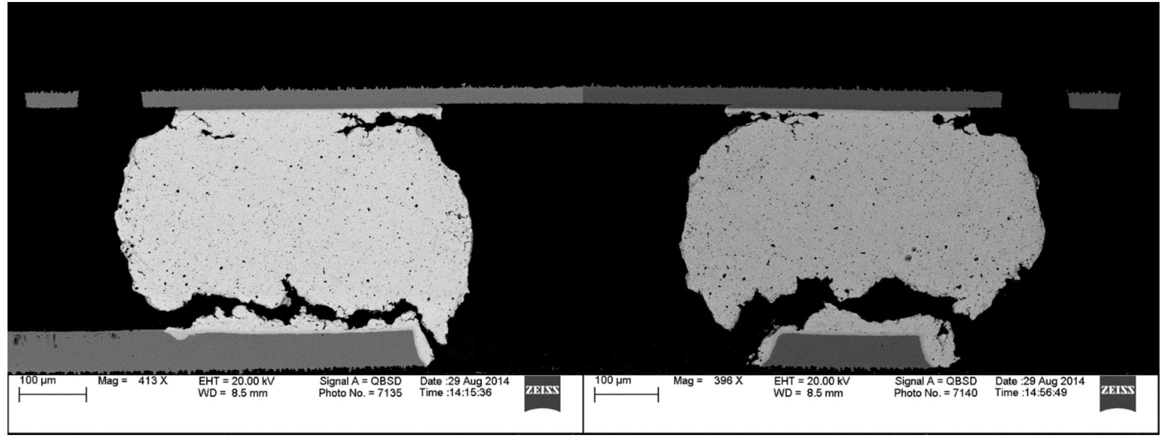


Figure 7.18. Predominant Board-Side Cracking.

7.3.2 Megtron6: CABGA 208, [P]SAC305, [S]SAC305

Figure 7.19, below, shows a BSE micrograph overview of three solder joints which display the most common failure characteristics observed.

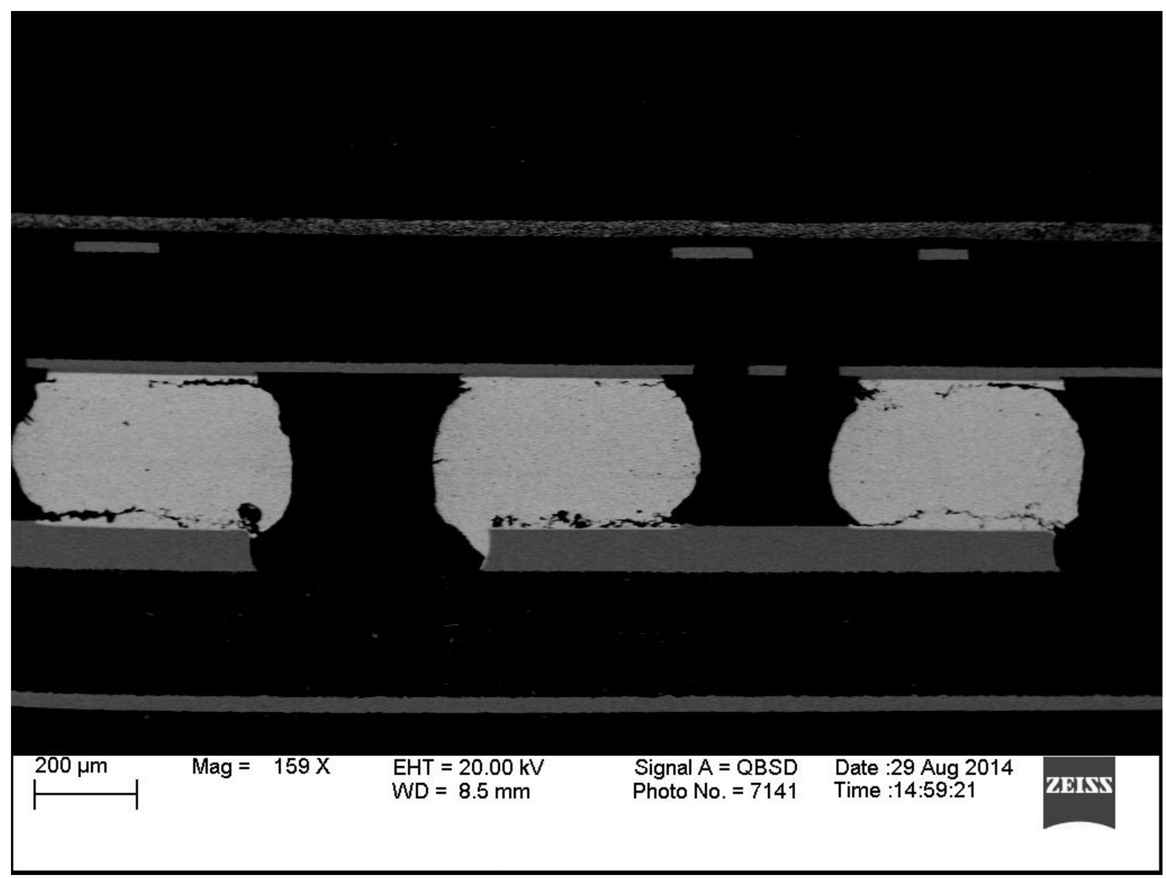


Figure 7.19. Overview BSE Micrograph showing Characteristic Failure Modes.

This sample exhibits a higher number of dominant cracks at the bottom side. These cracks sometime propagate along the IMC boundary and sometimes through the bulk solder in the near-interfacial region. Secondary cracks often appear along the top (component-side) of the joint; these generally progress along the IMC boundary region. In some cases, the top-side cracks are clearly the cause of joint failure with full cracking at the top and only partial at the bottom.

Figure 7.20, below, shows IMC boundary cracks at the bottom and top (of two different samples) for comparison. Note that while in both cases, cracking occurs in the IMC boundary region, the primary crack has propagated along the board-side in one case and along the component-side in the other. In each case, secondary cracking or crack initiation can be observed in the opposing side IMC boundary region.

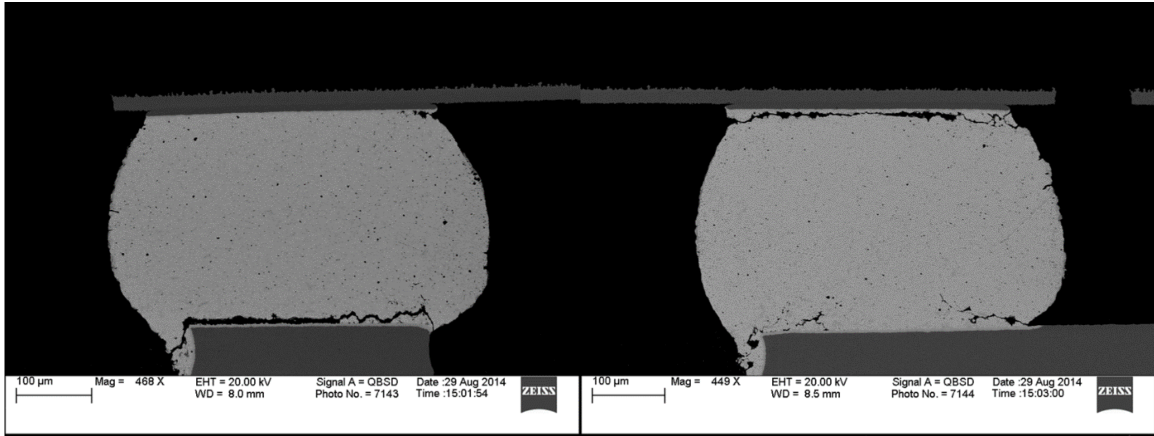


Figure 7.20. Primary cracking at IMC Boundaries.

Figure 7.21, below, shows a corner joint from the same component. It is impossible to definitively determine the overall cause of failure for the package at this time. However, the right-most joint displays a unique failure mode not seen elsewhere. This joint exhibits a brittle and extremely traumatic failure at the board-side, paired with a primarily brittle failure at the component-side. The bulk of the joint itself is “floating” away from its normal position. Since the joint is at a corner-point, we expect this joint to be one of the leading candidates for early failure.

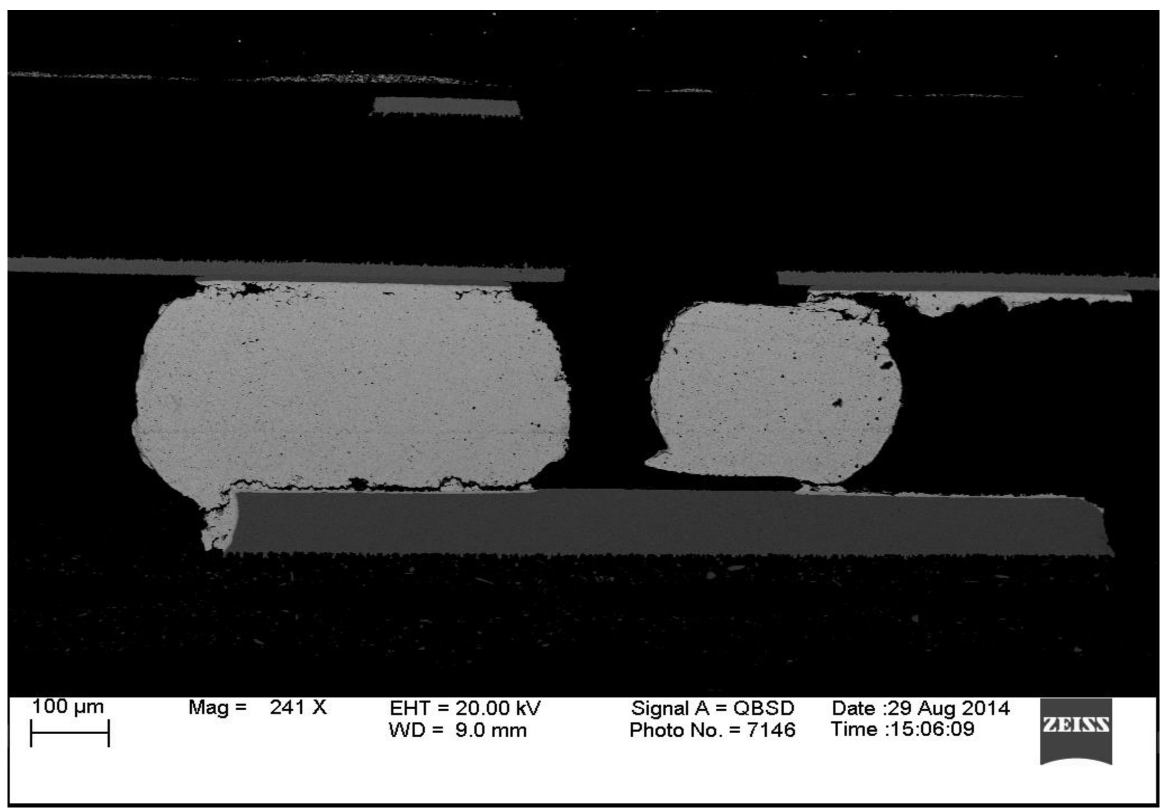


Figure 7.21. Traumatic failure in Right-most Joint.

7.3.3 Megtron6: SBGA 304, [P]SAC305, [S]SAC305

Figure 7.22, below, shows a BSE micrograph overview of three solder joints which are typical of this set. In this particular cross-section, no “full joint” cracks were observed. The component shown did in fact fail, but the cause of failure is not apparent from this sample. (Recall that each cross-section only shows one row of solder joints.) The larger SBGA304 component had to be sectioned into quarters to be properly mounted for metallurgical polishing, so we can examine only half of the joints we normally would for one polished sample.

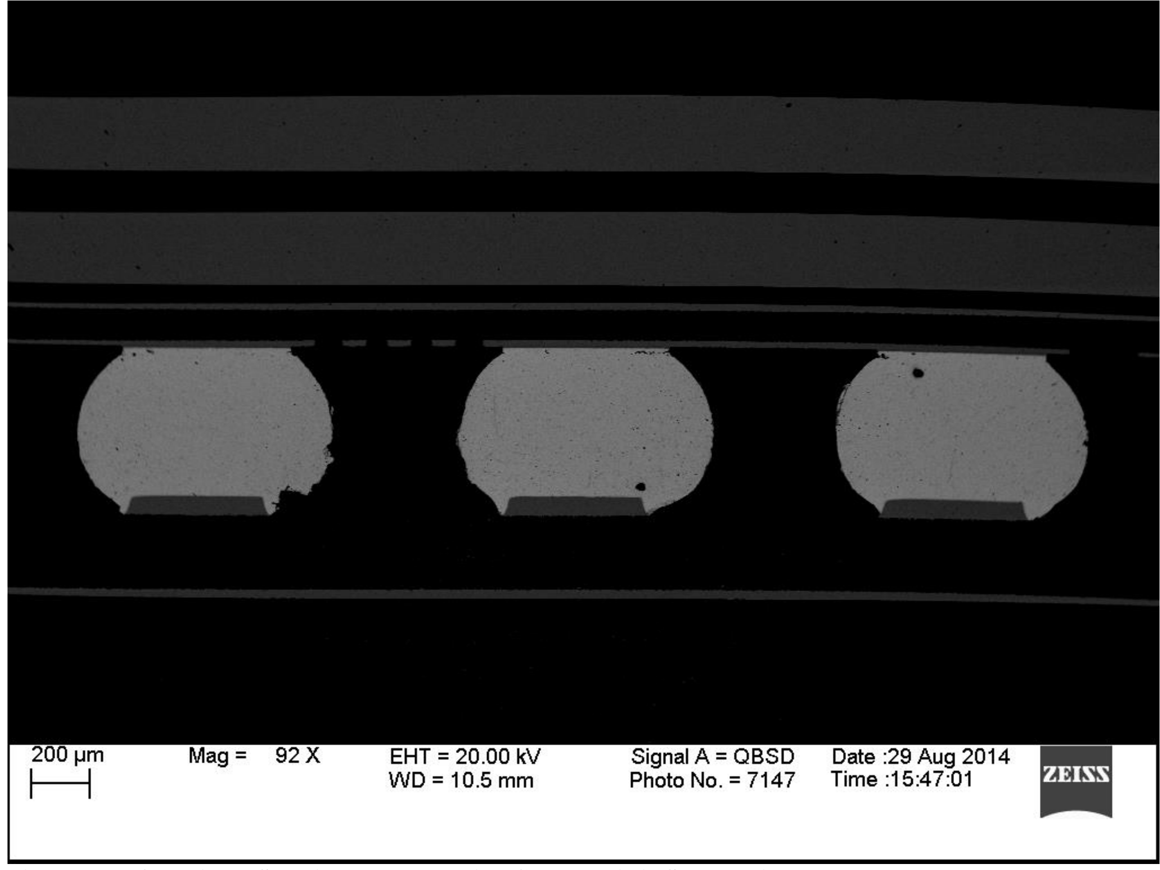


Figure 7.22. Overview BSE Micrograph showing Characteristic Solder Joints.

Some cracking is observed, which is predominantly at the top-side (component-side). In some cases, potential crack initiation sites also appear near the middle or bottom-side of the joint. Figure 7.23 below, shows characteristic top-side cracks which appear to be exclusively along the IMC boundary for the joints we can observe.

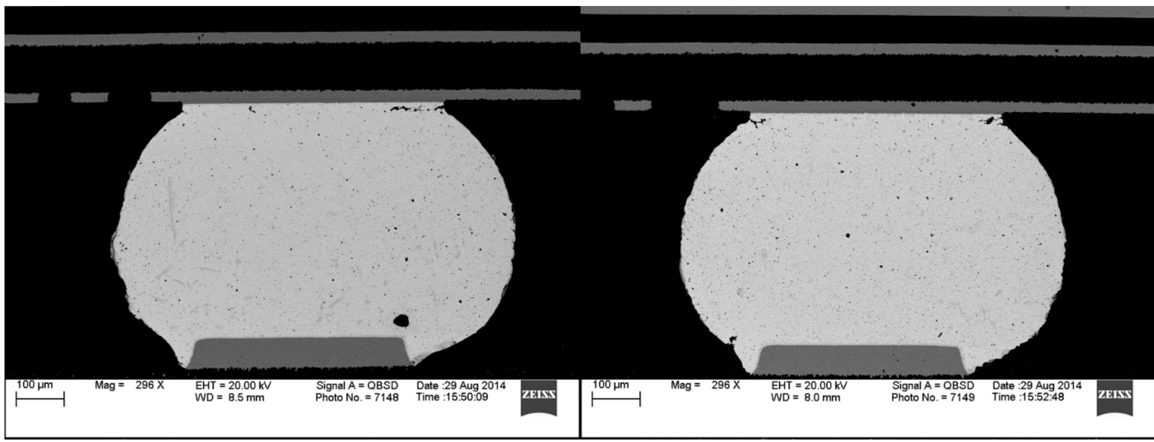


Figure 7.23. Primary cracking along the Top-Side IMC Boundaries

7.3.4 Megtron6: CABGA 256, [P]SAC305, [S]SAC305

Figure 7.24, below, shows a SE micrograph overview of three solder joints which display the most common failure characteristics observed. The joints fail fully across the component-side, with secondary cracks appearing at the board-side. The board-side cracks however, do not fully cross/compromise the joint. In most cases, the top-side cracks propagate through areas of the "bulk" solder that may indicate dynamic recrystallization driven failures.

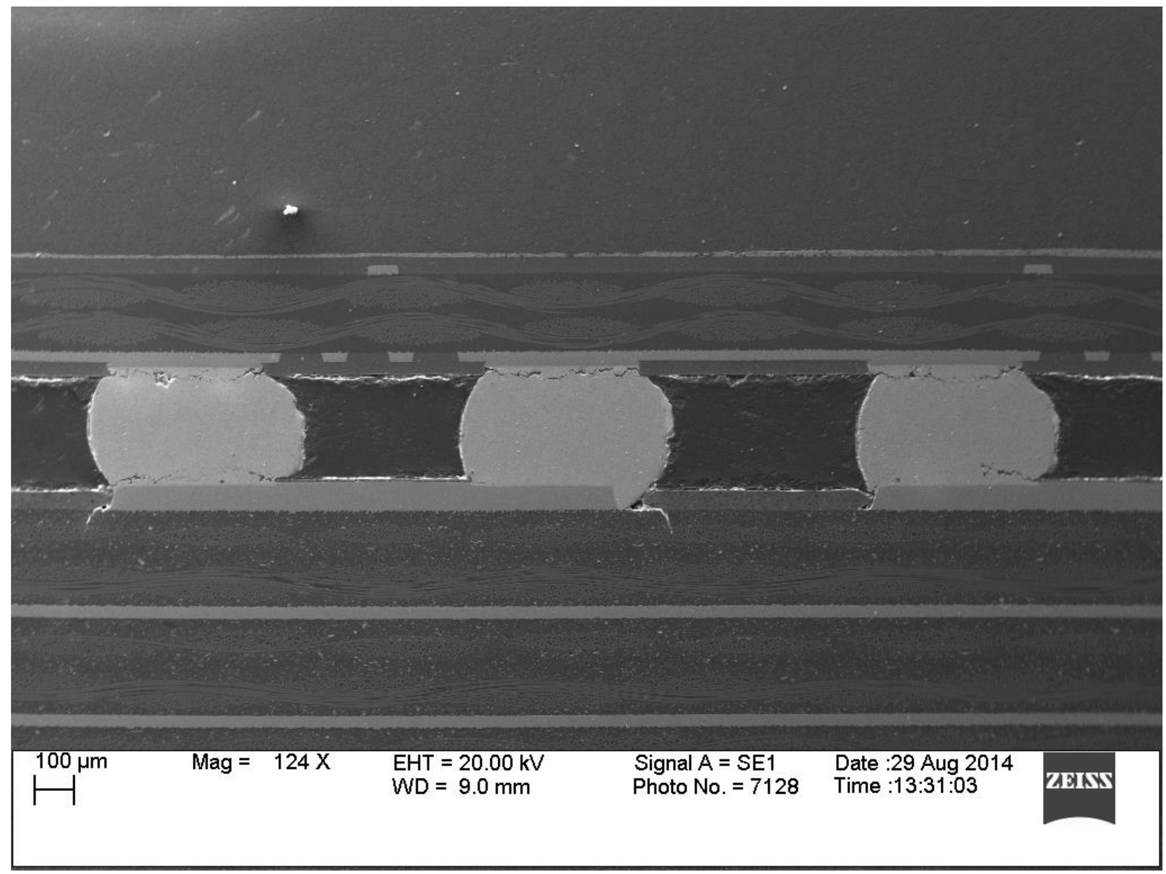


Figure 7.24. Overview SE Micrograph showing Characteristic Failure Modes

Many joints also displayed full cracks at both the component-side and the board-side. The component-side cracks appear to be indicative of possible dynamic recrystallization failures, while the board-side cracks remain closer to the interfacial

region. It cannot be proven at this point whether the top or bottom of these joints failed first. Figure 7.25, below, shows joints with both component-side and board-side cracking.

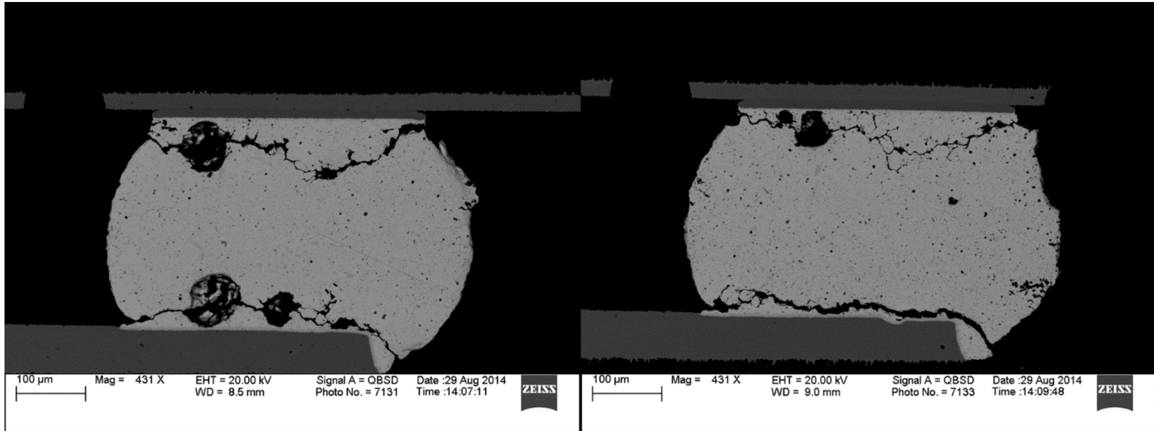


Figure 7.25. Roughly equivalent cracking at Top and Bottom

Chapter 8
Results and Conclusions

8.1 Results and Conclusions: TC1-SRJ Project

In this experiment, we have considered the thermal cycle reliability of an assortment of different electronic components and evaluated them on a 0.200" (200 mils) thick printed circuit board. Two substrate materials were tested: FR4-06 and Megtron6. Organic Solderability Preservative (OSP) surface finish was used with all test vehicles. The primary solders for component attachment in this experiment were SnPb and SAC305. Two solders designed for high-temperature reliability were also considered, including a Bi-doped SAC material and the six-element alloy Innolot (Sn3.8Ag0.7Cu3Bi1.4Sb0.15Ni).

The as-reflowed failure data (No Aging Group) was found to follow specific trends depending on the type and size of the component. The smaller plastic ball grid array (BGA) packages (13mm – 17mm) show the following pattern in Characteristic Life value, listed from best to worst:

(1) Matched Innolot*

(2) [S]SAC305 doped with [P]Innolot

(3) Matched SAC305

(4) Matched SnPb

*Note that Matched Innolot data is available only for the CABGA 208 and CABGA 36 components.

Figure 8.1, below, summarize of the characteristic life values for the No Aging Group for SAC305 solder spheres with either Innolot or SAC305 solder paste, with matched SnPb joints for scale.

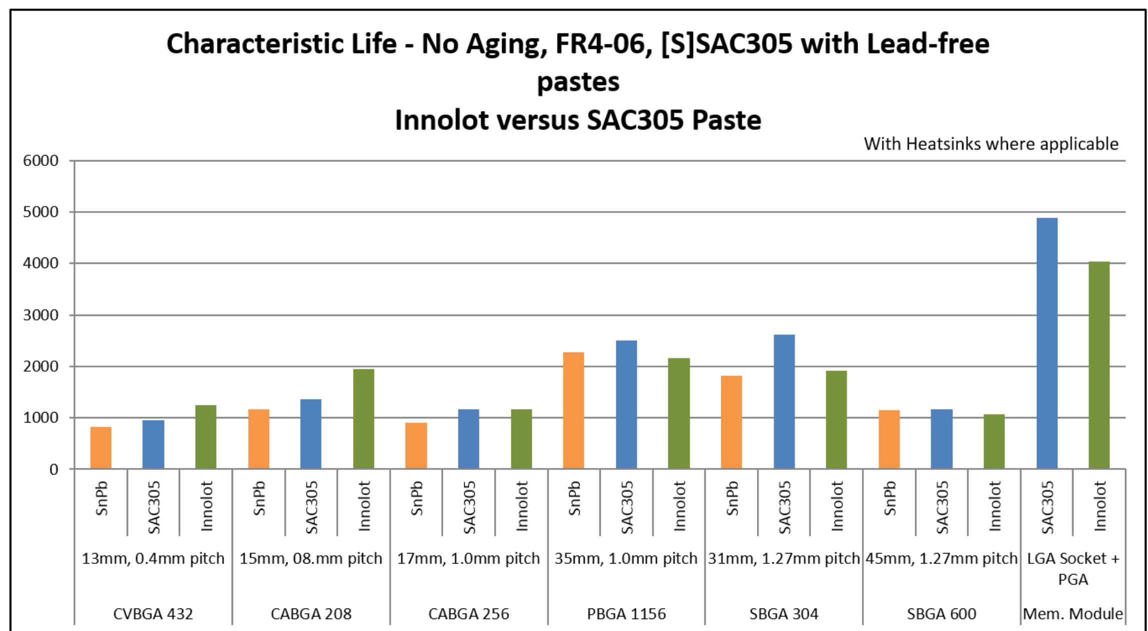


Figure 8.1. Solder Paste Comparison, No Aging Group.

As shown in Figure 8.1, above, some general trends can be seen in the reliability data based on the solder paste employed. For the smaller plastic BGA packages, Innolot doping (micro-alloying) appears to be an effective strategy for improving characteristic life. However, as component size and pitch increase, this improvement seems to wane (and in some cases reverse itself altogether). Improvements appear to bottom out at the 19mm component (1.0mm pitch), with larger components/pitches showing little or no improvement. This reliability trend appears to be largely stable over long periods of isothermal aging.

Table 8.1, below, shows rough joint composition numbers for [S]SAC305 with [P]Innolot. These are nominal values, and leaching during reflow is ignored. As the component pitch increases, the percentage of the joint metal deriving from the solder

paste decreases. Thus, the decreased effectiveness of Innolot paste doping for the larger components could potentially be engendered by under-doping of the resulting joints.

Table 8.1. Rough joint composition numbers. [S]SAC305 with [P]Innolot.

Component	Board Side	Percent of Joint from Solder Paste	Percent Silver (Ag)	Percent Copper (Cu)	Percent Bismuth (Bi)	Percent Antimony (Sb)	Percent Nickel (Ni)
SBGA 600	Top	0.0196	3.0157	0.5039	0.0588	0.0274	0.0029
SBGA 304	Top	0.0196	3.0157	0.5039	0.0588	0.0274	0.0029
PBGA 1156	Top	0.0248	3.0199	0.5050	0.0745	0.0348	0.0032
CABGA 256	Top	0.0248	3.0199	0.5050	0.0745	0.0348	0.0032
CABGA 208	Top	0.0340	3.0272	0.5068	0.1021	0.0476	0.0051
CABGA 208	Bottom	0.0207	3.0166	0.5041	0.0621	0.0290	0.0031
CVBGA 432	Bottom	0.0465	3.0372	0.5093	0.1395	0.0651	0.0070

Only two components are found on both sides of the TC1-SRJ test vehicle: the CABGA 208 and the CABGA 36. Since the CABGA 36 is slow-failing, the CABGA 208 is the component for which comparisons can easily be made between the 5 mil stencil (Top-Side) and the 3 mil stencil (Bottom-Side). The combination of [P]Innolot and [S]SAC305 is only found on the bottom-side of the test vehicle, however. Reliability data from the No Aging group indicates that a significant difference is not seen between matched [P][S]Innolot components or [P]Innolot with [S]SAC105 assembled on the Top- versus the Bottom-Side of the test vehicle. This could be shown to change in the full 24-Month Aging data, however.

When considering the overall effectiveness of the paste-doping strategy, it is important to investigate which components are "first-to-fail" on the test vehicle, since this will drive the assembly-level reliability. The CVBGA 432 component, which would normally be first-to-fail, does benefit from Innolot paste doping. Therefore, a measurable

improvement in assembly life is seen with the switch to Innolot solder paste. (Additionally, under-doping may be responsible for at least some of lack of improvement observed with larger components.) On the basis of the current data, the “paste doping” strategy appears to be a promising approach to improve assembly-level reliability in high-stress environments, but one that requires significant further study.

Figure 8.2, below, shows the effect of the substrate material on the characteristic life values of early failing components.

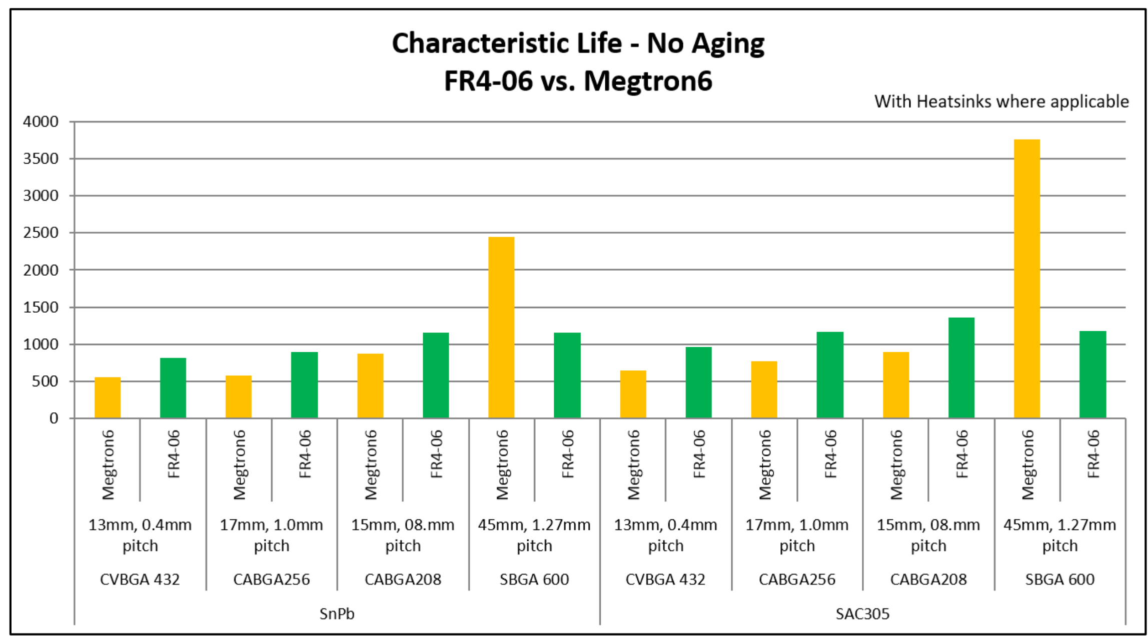


Figure 8.2. Substrate Comparison, No Aging Group.

Significant differences in reliability were seen between equivalent packages mounted to the two substrate materials tested (FR4-06 and Megtron6). For all of the over-molded plastic BGA components, reliability was higher on the standard glass-epoxy material (FR4-06). Performance for these packages on the high-electrical-performance polyphenylene oxide (PPO) blend material (Megtron6) was much worse. This difference appears to be stable over long periods of isothermal aging.

Conversely, the two Super-BGA components – SBGA 304 and SBGA 600 – dramatically reverse this substrate-based reliability trend. The Super Ball Grid Array (SBGA) components are metal-capped, cavity-down designs and are therefore structurally distinct from the other ball grid array packages considered. Both of the Super-BGA components display higher reliability on the Megtron6 substrate than on the FR4-06 substrate. This difference also appears to be stable over long periods of isothermal aging. Finite Element Analysis (FEA) may be beneficial in understanding these differences.

When considering the effects of Isothermal Aging on the relative reliability of various packages, the data indicate that even components that show similar initial reliability trends may display differences following aging. Although the No Aging reliability data show similar trends for all of the smaller plastic packages (5mm-17mm), this uniformity does not appear to extend universally to aged data. In particular, the amount of reliability degradation of the lead-free solders relative to tin-lead solder appears to be package-dependent.

On Megtron6, the 15mm CABGA 208 package demonstrates a clear and complete crossover in reliability distributions, with the SnPb solder superior to SAC305 in the 24-Month aging group. However, for the 17mm CABGA 256 package, only a partial cross-over between the SnPb and SAC305 (matched) solders is seen. For the 13mm CVBGA 432 package, the SAC305 solder is still superior to SnPb even after 24 months of aging at 75°C.

Figure 8.3 shows the characteristic life values as a function of time for the CVBGA 432, the CABGA256, and the CABGA 280 components on the FR4-06

substrate material. Degradations in reliability are seen in all components and subgroups. The observed reductions in reliability are not more severe for the SAC305 material than for the SnPb control on the FR4-06 substrate, however.

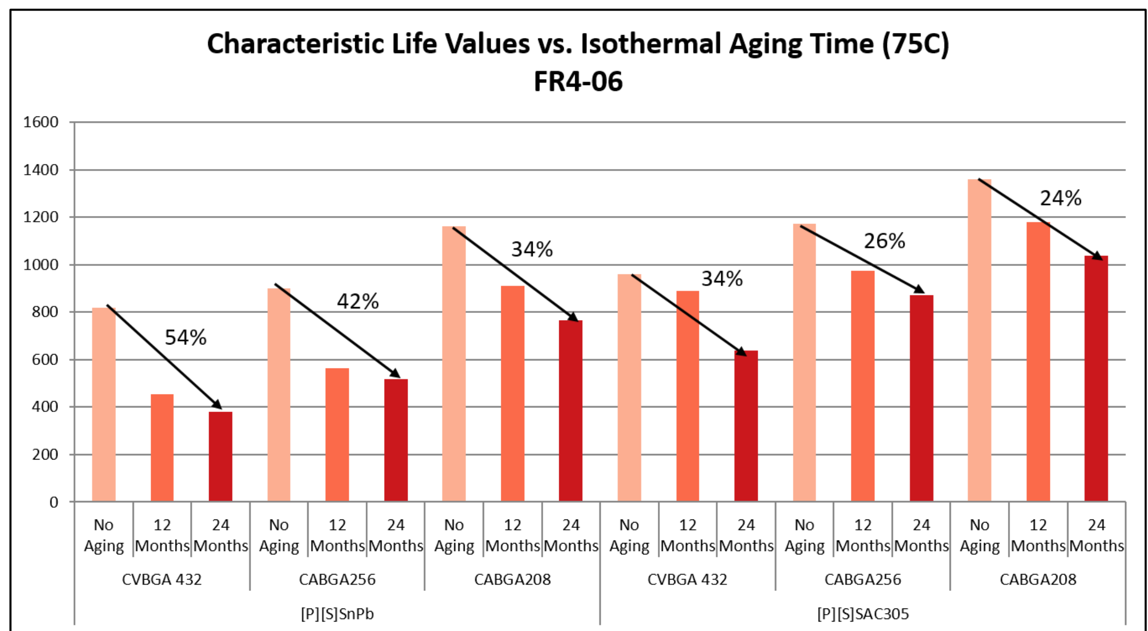


Figure 8.3. Characteristic life vs. Isothermal Aging Time. Key packages, FR4-06.

Figure 8.4, below, shows the same comparison on the Megtron6 substrate material.

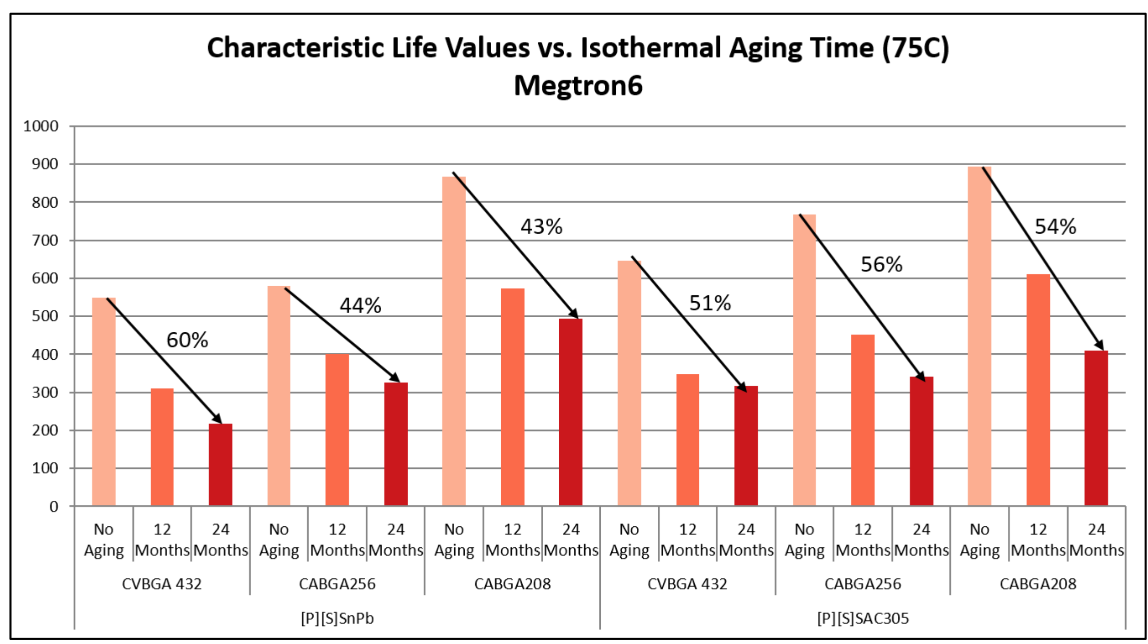


Figure 8.4. Characteristic life vs. Isothermal Aging Time. Key packages, Megtron6.

As was the case on FR40-6, degradations in reliability are seen in all components and subgroups. However, the relative degradation between the SAC305 and SnPb groups is starkly different on the Megtron6 substrate material. With the exception of the CVBGA 432 package, isothermal-aging-induced reliability degradations appear to be more severe for SAC305 than for SnPb on Megtron6. Finite Element Analysis (FEA) may be beneficial in understanding why the Megtron6 substrate seems to affect the lead-free materials so aversely.

Failure Analysis performed thus far demonstrates that a variety of crack propagation and failure modes are present even when considering only a limited set of components. Depending on the subgroup examined, crack propagation may occur predominantly at the component-side, predominantly at the (printed circuit) board-side, or at roughly equivalent rates at both sides of the solder joint. Failures – both at the component- and board-side – are observed to occur either in the near-interfacial IMC region or across the bulk of the joint.

Failures across the bulk of the solder joint are more common in cases where SAC105 solder joints were used than for the other lead-free materials tested. This difference likely stems from SAC105's higher ductility, which makes (relatively predictable) failures across the bulk solder more common. Failures that occur through the bulk solder may indicate that 'dynamic recrystallization' mechanisms are dominating the crack propagation mechanics in these joints. However, further study will be needed in order to confirm this hypothesis.

8.2 Ongoing and Future Work: TC1-SRJ Project

Current project status for the Thermal Cycling (TC) test is as follows: The No Aging, 6-Month Aging, and 12-Month Aging test groups have passed 3000 thermal cycles and are now finished with TC testing. An initial pro-rated set of 24-Month Aging boards is at approximately 1300 cycles (Group 24A). A second pro-rated set of 24-Month Aging boards has started thermal cycle testing and is at approximately 100 cycles (Group 24B). Failures have mostly concluded for the medium-size plastic ball grid array (BGA) packages (13mm-19mm), with failures continuing for the smaller (5mm-6mm) and larger (31mm-45mm) packages. Data taking continues, and additional information may clarify points from the current knowledge-base.

In terms of the Failure Analysis effort, this is not an experiment where a small number of samples can be cross-sectioned and simple conclusions about overall characteristic failure modes drawn. An extensive and lengthy investigation requiring many resources will be required to fully elucidate how the failure mechanics relate to the experimental variables. A move to a lower cost scanning electron microscope solution has been in the works for the last year and should allow for faster and easier FA work. Additionally, a shift to heavier reliance on optical microscopy is planned and equipment purchases are planned. This should allow for significantly faster throughput and lower cost. Additional microscopy work will continue to proceed on this basis, both on additional No Aging samples and on more samples from subsequent aging groups. A large number of samples is available from the existing test vehicles, including a subset that has been stored at low temperature to control ongoing microstructural evolution.

In additional to the conclusion of the 24-Month Aging Thermal Cycling test and further Failure Analysis, another key aspect of ongoing efforts needs to be the addition of FEA (Finite Element Analysis) modeling. Although such models are not necessarily accurate for predicting failures, they are generally effective for understanding the significance of different test parameters and understanding critical factors in the mechanics of failure. Our research group has partnered with Dr. J.C. Suhling's group (Auburn University, Mechanical Engineering Dept.) in order to produce FEA models for the TC1-SRJ project. These models should help to shed light on some of the most interesting results, such as the substrate effects noted and, hopefully, why micro-alloying appears to be effective for some packages but not for others.

8.3 Ongoing and Future Work: Follow-On and Related Projects

As the "paste doping" (micro-alloying) strategy appears to be a promising approach for improving the reliability of printed circuit assemblies exposed to high-stress environments, a series of follow-on experiments were/are planned. Some of these follow-on studies have concluded, some are currently ongoing, and more are still in the planning phases. Some of the ongoing and concluded work include the following studies.

The "Downselect" Test: This test was a "crash and burn" test involving a large number of solders designed for high-temperature thermal cycling reliability. Ten (10) different solder manufacturers supplied fourteen (14) different solder materials for testing. Some materials were available in both solder paste and solder spheres (which were used to ball LGA packages), while others were available in only paste or spheres. Two smaller test vehicles were used. There were two test groups: No Aging and 6-Month

Aging at 125ºC. Three (3) testing methods were employed: 1) liquid-to-liquid thermal shock, 2) Vibration (white noise), and 3) Drop Testing. The goal of the test was to determine the top five (5) materials for further testing on the TC1-SRJ test vehicle under thermal cycle testing. The test was successful in selecting five materials that exhibit liquid-to-liquid thermal shock reliability far in excess of that of SAC305.

The "TV9/TC11" Test: A thermal cycling test involving several of the higher performing materials from the Downselect test. The liquid-to-liquid thermal shock board design was used (rather than TC1) as this board is closer to commercial applications in its thickness and material (FR4-06). This test is ongoing at close to 1000 thermal cycles.

The TC1-SRJ Phase II Test: Using the TC1-SRJ test vehicle and Megtron6 substrate material, this test will evaluate the thermal cycling reliability of the five (5) "high-temperature reliability" solder materials identified in the Downselect test. Only paste doping will be tested (no component reballing). There are four test groups: No Aging, 6-Month Aging at 75ºC, 12-Month Aging at 75ºC, and 24-Month Aging at 75ºC. The assembly for this experiment has concluded, and the No Aging group has begun thermal cycling (approximately 200 cycles).

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