POST ION-IMPLANTATION SURFACE PLANARIZATION PROCESS FOR 4H-SIC

WAFERS USING CARBON ENCAPSULATION TECHNIQUE

Except where reference is made to the work of others, the work described in this is my own or was done in collaboration with my advisory committee. This thesis does not include proprietary or classified information.

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Kashyap Yellai

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POST ION IMPLANTATION SURFACE PLANARIZATION PROCESS FOR 4H-SIC WAFERS USING CARBON ENCAPSULATION TECHNIQUE

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Signature of Author

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Date

VITA

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THESIS ABSTRACT

POST ION-IMPLANTATION SURFACE PLANARIZATION PROCESS FOR 4H-SIC WAFERS USING CARBON ENCAPSULATION TECHNIQUE

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Metal oxide semiconductor (MOS) technology forms the core of the semiconductor power devices. The electronic properties of wide band gap semiconductor materials like 4H-SiC has attracted considerable interest for fabrication of high power and high frequency devices. The Si-face terminated 4H-SiC is extensively used in fabrication of these devices. However, the rate of oxidation of Si-face 4H-SiC is lower compared to C-face 4H-SiC materials. This high rate of oxidation of C-face 4H-SiC can be used as an advantage in decreasing the overall fabrication time. Extensive gate oxide reliability Si terminated 4H-SiC are available in literature. However, the gate oxide reliability studies on C-face 4H-SiC are still in early stages. In this work, the reliability of the thermally grown gate oxide on C-face 4H-SiC is studied. Oxides grown on epitaxial material showed superior oxide reliability compared to oxides grown on aluminum (Al) and nitrogen (N) doped substrates. This is attributed to the damage of the surface caused by high energy ions used for implantation. In addition, the surface is further roughened

during the high temperature activation annealing (1450 ^{0}C - 1650 ^{0}C) which is performed to make the impurity atoms electrically active. Atomic force microscopy (AFM) analysis was performed at Vanderbilt University on the surfaces of C-face 4H-SiC to study the damage caused by implantation and post-implant annealing processes. The roughness values obtained by AFM were correlated with the oxide reliability measurements. Current-voltage (I-V) measurements were performed to calculate the dielectric breakdown field strength values for Al and N implanted samples with varying concentrations of 8 x 10^{15} to 6 x 10^{19} atoms/cm^3. These concentrations correspond to the source/drain region implants for *p*- and *n*- channel MOSFETs. AFM results indicate that the surface of the substrate roughens with increase in implant concentration. Ion channeling experiments on the surface of C-face 4H-SiC subjected to high temperature implantation and activation annealing substrates showed a deviation from the stoichiometric SiC to a carbon rich compound. This non-stoichiometric compound is detrimental for the performance of the gate oxide at high electric fields.

In this thesis work, a protective carbon (graphitic) cap was used on the C-face 4H-SiC substrates to protect the surface from annealing damage. The AFM and IV results of the samples protected by the carbon cap revealed that the carbon encapsulation technique prevents the annealing damage, thereby increasing the reliability of the gate oxides.

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1. INTRODUCTION

Modern day instrumentation invariably incorporates active solid state devices. This class of devices primarily consists of components whose operation depends on movement of the charge carriers called electrons and holes that undergo energy level changes in the materials. The most common active solid state devices are diodes, transistors and thyristors. These devices work as rectifiers, amplifiers and switches [1]. Depending upon the input current (I) and voltage (V), these devices can be classified as either low power or high power devices. The definition of high power is somewhat arbitrary, but any device which is capable of switching at least 1 ampere of current is referred to as a power device. The following characteristics are expected of a power device. For switching operations, the device should have zero admittance when OFF and zero impedance when ON. In addition, the device should be capable of performing instantaneous transitions from ON to OFF and OFF to ON, with zero switching losses. It also should have low triggering power and good noise immunity [2]. These power electronic devices are made of semiconductor materials. The following sections discuss the physics and applications of semiconductor power devices.

1.1 Semiconductor Power Devices

Diodes, thyristors, triacs and power transistors are the core components of semiconductor power electronics. These devices find extensive applications in aerospace,

telecommunication, transportation and utility industries as rectifiers, converters, inverters, regulators and switches. This study focuses on power transistors.

Power transistors are broadly classified as unipolar or bipolar transistors or a combination of both known as the insulated gate bipolar transistor (IGBT). Metal oxide field effect transistors (MOSFET) fall under the classification of unipolar transistors i.e., the conduction in the device takes place entirely in either the *n*- or *p*- regions rather than both. For moderate power and high frequency applications (> 500 KHz) the MOSFET is the device of choice. The structure of an IGBT is similar to a vertical double diffused MOSFET, and they are commonly used for high voltage (> 1200 V) and low frequency applications. A brief description of an IGBT will be given in the Section 1.3, where it is compared with the vertical double diffused MOSFET. This current research examines the study of the oxide reliability for 4H-SiC devices used for moderate power and moderate frequency applications. Hence, review of MOSFET devices and applications is provided.

1.2 The Metal Oxide Semiconductor Field Effect Transistor

The metal oxide semiconductor field effect transistor (MOSFET) is an important component of many semiconductor integrated circuits (ICs). From its initial conception as a transistor to its more recent development as a power device, MOSFET technology has matured significantly. In this section, the fundamental operating principles of the MOSFET are discussed with an emphasis on silicon based transistors. In light of the recent trend in using wide band gap semiconductors for high power applications, the advantages and limitations of using silicon carbide based MOSFET devices will be explained. The critical issues involved in fabricating SiC MOSFETs and optimizing their performance will also be discussed.

1.2.1 Operation of MOSFET

The general structure of a MOSFET is shown in Fig. 1. Two *pn* junctions are placed side by side on the silicon substrate, which can be either *p*-type or *n*-type. The current flow is from source to drain, and the magnitude of the current can be controlled by changing the gate voltage V_G (relative to ground). The source and the back of the substrate are always grounded. The drain to gate bias is always reverse. To understand how the drain current varies during operation, the drain voltage V_D is initially set to zero. Since the device under consideration is *p*-type, the region between the source and the drain contains holes. This situation can be viewed as an open circuit. Figure 2 shows a schematic of a MOSFET. The operation of the device involves three stages, namely accumulation, depletion and inversion. These stages can be controlled by the gate bias. In the initial stage, when V_G is given a negative voltage, the majority of the charge carriers move to the oxide-semiconductor interface. This is called the accumulation stage. The depletion stage occurs when the gate potential is made slightly positive. During this stage the holes are repelled by the positive potential on the gate. As this positive potential is further increased the hole concentration decreases and an increase in the electron concentration is observed. This stage where the charge carriers in the channel change the polarity is called inversion. The characteristic gate voltage that controls this shift is designated by V_T and is known as the depletion-inversion transition point. When V_D is set to zero and the V_G is increased in steps, the MOSFET progress through these three stages of operation. When $V_G > V_T$ (inversion bias), an inversion layer is formed adjacent to the silicon and silicon dioxide interface. This inversion layer is electron rich in *p*-type semiconductors and thus is called the *n*-channel.

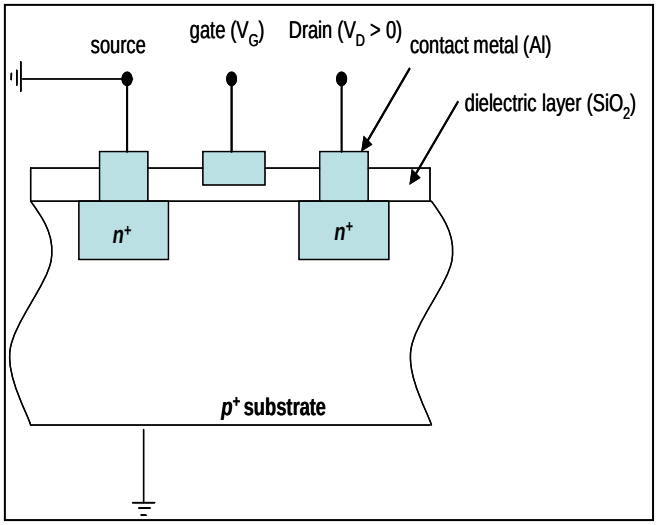

Figure 1: Schematic of an *n*- channel MOSFET

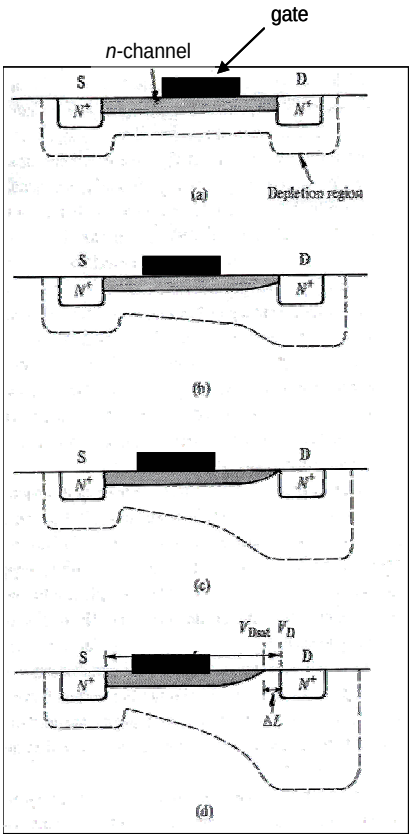

Figure 2: Operation phases of MOSFET when $V_G > V_T$ [3]

The greater the inversion layer electron concentration, the greater the *n*-channel conduction. Let us now examine this sequence in more detail by applying the inversion bias $V_G > V_T$ and by increasing the drain voltage in steps starting from $V_D = 0$ [3]. Fig. 2a shows the system in thermal equilibrium when $V_D=0$ and no drain current is observed. As the drain voltage increases slightly, the channel acts as a simple resistor and there is a linear relationship between the drain current (I_D) and V_D. When V_D increases further, as shown in Fig. 2b, the depletion region widens along the source to channel direction and the inversion channel decreases. As V_D continues to increase, the inversion layer depletes and pinches off, as shown in Fig. 2c. At this point, the region near the drain becomes completely devoid of channel charge carriers and there is no inversion channel. The slope of I_D versus V_D decreases, flattening to zero as the drain voltage increases beyond the saturation voltage called, V_{Dsat}. This type of device without a built-in channel is referred to as *normally-OFF* or *enhancement* type MOSFET (E-MOSFET). A transistor is referred to as *normally-ON* or *depletion* type MOSFET if it has either an *n*- type or a *p*-type built-in channel. This type of device can be turned off by reverse biasing the gate to drain region. Unlike *n*-channel MOSFETs, *p*-channel MOSFETs utilize *n*-type substrates with *p*-doped source and drain regions. During biasing, a *p*-channel is formed in the region between the source and the drain. Of the two types of MOSFETs, *n*-conduction channel E-MOSFETs are most widely used in power conditioning and integrated circuits because of higher mobility of the electrons compared to holes. All further discussion in this work will focus on the use of E-MOSFETs as switches in moderate power and moderate frequency applications. The lateral MOSFETs described above have source and drain on the same side of the substrate, as shown in Fig. 1. The advantages of lateral

MOSFETs are their low gate signal power requirements and fast switching speeds, but they also suffer the disadvantage of high channel ON resistance (R_{ON}), which leads to significant power dissipation within the *n*-channel. Vertical double diffused MOSFETs which will be described in the next section overcome this disadvantage of high channel resistance.

1.2.2 Vertical Double Diffused MOSFET

An ideal cross section view of a vertical double diffused MOSFET (VDMOSFET) is shown in Fig. 3. Silicon DMOS is manufactured using lateral diffusion technology. On the n^+ substrate a resistive n^- epitaxial layer is grown. The thickness of n^- layer determines the blocking voltage capability. On the lower side of the substrate a metal layer is deposited to form the drain, after which p^- regions are diffused into the n^- epitaxial layer. Then n^+ regions are diffused into the p^- regions to form source regions. When the gate voltage is made positive with respect to the source, an electric field is established, and an inversion *n*-channel is formed in the p^- region as shown in Fig. 3. At this point the electrons enter the source terminal and flow laterally through the inversion channel under the gate to the *n*-drift region. The electrons then flow vertically through the *n*- drift region to the drain terminal. The conventional current direction is from drain to source. The conductivity of the channel is modulated by the gate bias voltage, and the current flow is determined by the resistance of the various resistive components as shown in Fig. 3.

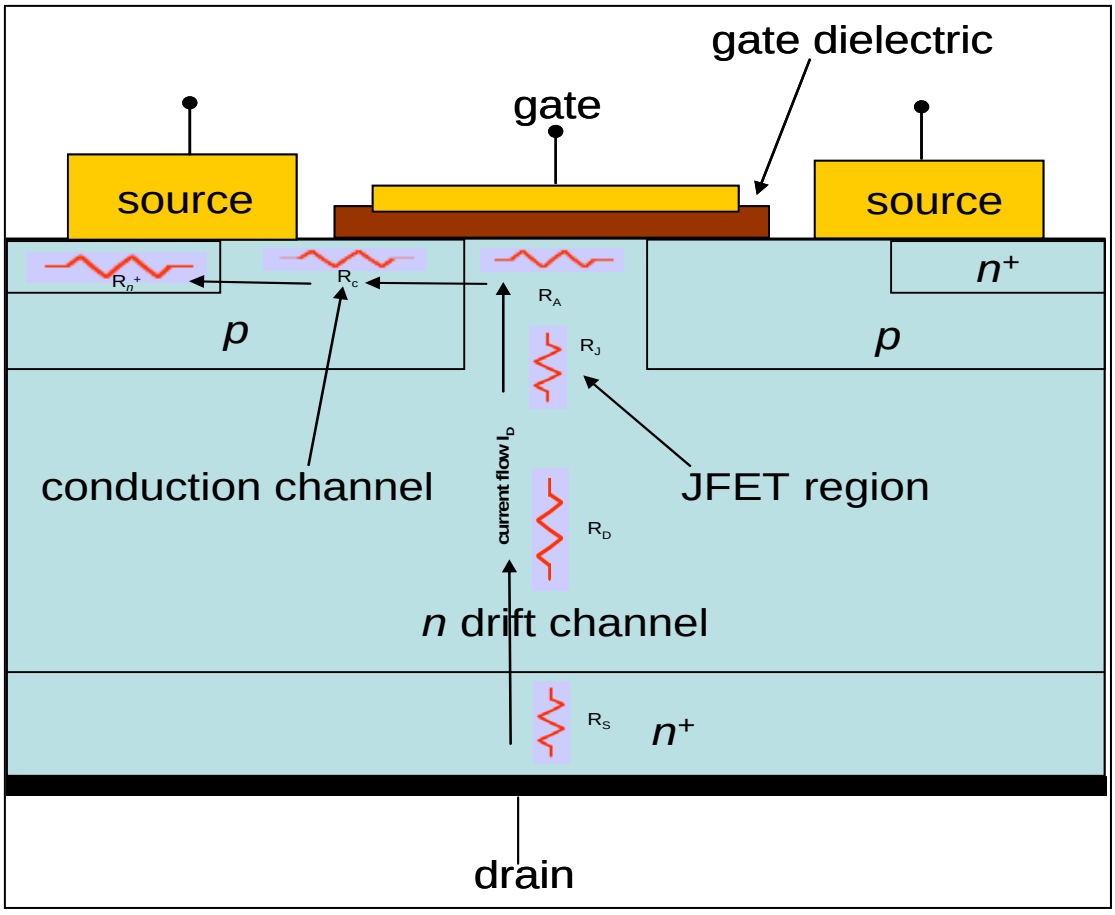

Figure 3: Schematic of a typical VDMOSFET showing various resistive components inside the device

The total R_{ON} is given by [4]

$$R_{ON} = R_{n^+} + R_C + R_A + R_J + R_D + R_S \quad \textbf{Eq 1}$$

R_{n^+}: resistance of n^+ regions

R_C: channel resistance

R_A: accumulation layer resistance

R_J: resistance from the drift region and *p*-base due to pinch-off

R_D: drift region resistance

R_S: substrate resistance

For an ideal MOSFET, at higher break down voltages, R_{n^+}, R_A, R_J and R_S are negligible, and only the resistances due to the channel (R_C) and drift regions (R_D) need be considered. Hence, the channel and drift resistances must be reduced in an efficiently functioning power MOSFET. Silicon, which is the material currently used for power MOSFETs, cannot be used for high power, high frequency and high temperature applications. Silicon carbide is known to be a suitable material for these extreme operating environments. In this study, silicon carbide will be considered as viable alternative to silicon for manufacturing power MOSFETs.

1.2.3 Silicon carbide Power MOSFETs

SiC exhibits one-dimensional polymorphism, which is generally referred to as polytypism. So far, 200 polytypes of SiC have been identified. Common polytypes are 3C, 2H, 4H, 6H, 8H, 9R, 10H, 14H and 24H. The nomenclature used refers to the structure of the polytypes, which depending upon the stacking, are divided into cubic (C), hexagonal (H) and rhombohedral (R) structures.

Cubic SiC has one polytype, known as 3C-SiC or α-SiC. Each Si-C bilayer can be oriented into one of only three possible positions with respect to the lattice without

disrupting the tetrahedral bonding. If these three layers are arbitrarily called A, B and C, then the stacking sequence is given by ABCABC…. This structure is known as cubic zinc blende. 3C-SiC possess the lowest band gap E_g (~ 2.4 eV) of any of the known polytypes and also has largest electron mobility (~ 800 cm^2 /V.s). However, 3C-SiC is not yet available commercially in bulk form, though it is grown in the laboratory environment [5]. For 2H-SiC, the stacking of the bilayers follows the pattern ABAB…. which results in hexagonal symmetry. All the other SiC polytypes consists of a mixture of hexagonal and cubic bonding. For example, 4H-SiC is comprised of equal number of hexagonal (wurtzite) and cubic (zinc blende) bonding, while 6H-SiC is composed of two-thirds cubic and one-third hexagonal bonding. The overall symmetry is hexagonal for both these polytypes. The type of bonding and its crystal structure both influence the electronic properties of SiC. 4H and 6H-SiC are the only polytypes currently available in wafer form, and both are used extensively for electronic devices. The material's electrical properties also have an impact on the performance of the semiconductor device. Table 1 shows a comparison of the electrical properties of three popular polytypes 3C-SiC, 4H-SiC and 6H-SiC, with Si. Assuming that the power losses are only due to the power dissipation in the ON-state caused by the current flow through the ON-resistance of the power FET, Baliga derived a figure of merit to minimize the conduction losses [6]. This is given by,

$$BFOM = \varepsilon.\mu.E_G^3 \qquad \textbf{Eq 2}$$

Quantity	3C-SiC	4H-SiC	6H-SiC	Silicon
E_g (eV) (T< 5K)	2.4	3.26	3.02	1.12
E_B (MV/cm)	2.12	2.2	2.5	0.25
Θ_k (W/cm.K) @ 300K	3.2	3.7	4.9	1.5
N_i @ 300 K (cm-3)	1.5×10^{-1}	5×10^{-9}	1.6×10^{-6}	1.0×10^{10}
v_{sat} (cm/s) parallel to c-axis	-	2.0×10^{7}	2.0×10^{7}	1.0×10^{7}
μ_e (cm2/V.s)	800	1000	400	1400
μ_{per}/μ_{para} @ 300 K	-	0.73-0.83	6	-
μ_h (cm2/V.s	40	115	101	471
ε_s	9.72	-	-	11.7

Table 1: List of electronic properties of silicon carbide polytypes and silicon [5]

where,

ε is the dielectric constant of the material

μ is the mobility of the majority carriers

E_G is the bandgap of the semiconductor

Johnson's figure of merit (JFOM) which is used to define the power-frequency product for a low voltage transistor [7], is given as

$$JFOM = \frac{E_c . \nu_s}{2\pi} \qquad \textbf{Eq 3}$$

where, E_c is the critical electric field breakdown

ν_s is the saturated drift velocity

Keyes figure of merit (KFOM) describes the thermal limitations on the switching behavior of transistors used in integrated circuits [8] and is given by,

$$KFOM = \lambda[\frac{c.\nu_s}{4\pi\varepsilon}]^{1/2} \qquad \textbf{Eq 4}$$

Applying the values listed in Table 1 to equations 2-4 reveals that 4H-SiC has superior electronic properties and high figures of merit compared to 6H-SiC and silicon. Hence, 4H-SiC is the first choice for use as an alternative material for the fabrication of power semiconductors. In addition, 4H-SiC has higher intrinsic electric field breakdown (E_c) and saturated drift velocity (ν_s) values than pure silicon, so thin 4H-SiC substrates can be used to block high voltage. Thinner *n*-type substrates also help in decreasing the drift resistance.

1.3 Issues with 4H-SiC Power Devices

As explained in section 1.2.2, silicon DMOS devices are fabricated using a series of diffusion doping processes to form *p*-base and n^+ source regions in silicon substrate.

Unfortunately for silicon carbide, diffusion doping is not possible due to its inherently strong bonding nature. The hot ion-implantation method of doping is therefore extensively used for silicon carbide. One of the major problems associated with ion-implantation for SiC is the incongruent evaporation of silicon atoms from the SiC surface during the high temperature post ion implantation annealing process, which leads to stoichiometric disturbances i.e, non-uniform Si and C atom concentrations with dangling silicon bonds, oxygen vacancies and carbon clusters at the SiO_2/SiC interface after oxidation. A rough interface between the gate oxide (SiO_2) and SiC surface is also formed during oxidation. During the inversion channel formation process, the carriers (electrons for an *n*- channel MOSFET) are trapped by these imperfections at the SiO_2/SiC interface. The traps are called interface states. In addition to the imperfections, the surface roughness developed during the post implantation annealing process may also act to scatter the conduction of electrons. These interfacial trap densities decrease the channel mobility, resulting in high channel resistance. From equation 1, any increase in channel resistance will lead to an increase in ON resistance. Figs. 4 and 5 show schematics of the interactions between the channel carriers (electrons) and the interfacial traps for each of these cases, respectively. In Fig. 4, the carrier electrons are trapped by defects such as dangling silicon bonds, oxygen vacancies and carbon clusters. These trapped electrons obstruct the motion of the other electrons and scatter them in random directions, thereby decreasing the channel mobility. In Fig. 5, electrons are trapped within the grooves of the surface that are developed due to the uneven surface. These trapped electrons terminate the electric field at the respective charge centers, leading to a non-uniform electric field in the channel causing scattering of the conduction channel

electrons. This increases the channel resistance and, hence, the overall ON resistance of the device.

The insulated gate bipolar transistor (IGBT) is another device which is extensively used in power electronics applications. IGBTs are similar to the VDMOSFET structure in construction. The main difference between the two devices is the presence of p^+-type region above the anode (drain) and below the n^- drift region. Fig. 6 compares the structures of a MOSFET and an IGBT [9]. The IGBT is a combination of MOS and bipolar structures. This type of structure also encounters the same problems with increasing ON resistance as MOSFETs due the interfacial traps at the SiO_2/SiC interface. This current work focuses on developing processes to decrease the channel resistance caused by the surface roughness of the substrate. A thorough literature review was conducted, and the relevant research is summarized in Chapter 2. The experiments and the results obtained are explained in Chapter 3 and Chapter 4, respectively. The findings are discussed and compared with the results obtained by previous authors in Chapter 5 and conclusions are drawn. Suggestions for further research are given in Chapter 6.

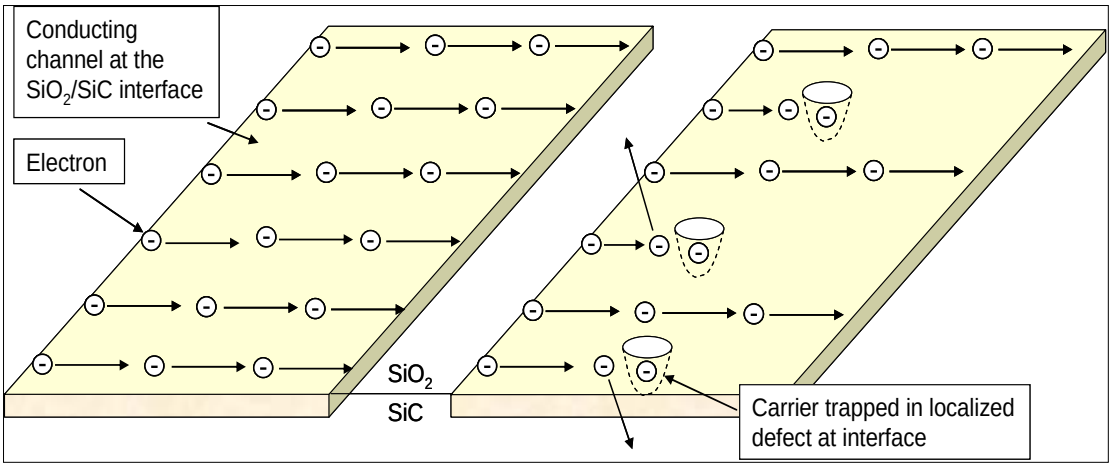

Figure 4: Illustration of the scattering of carriers (electrons) by interfacial traps

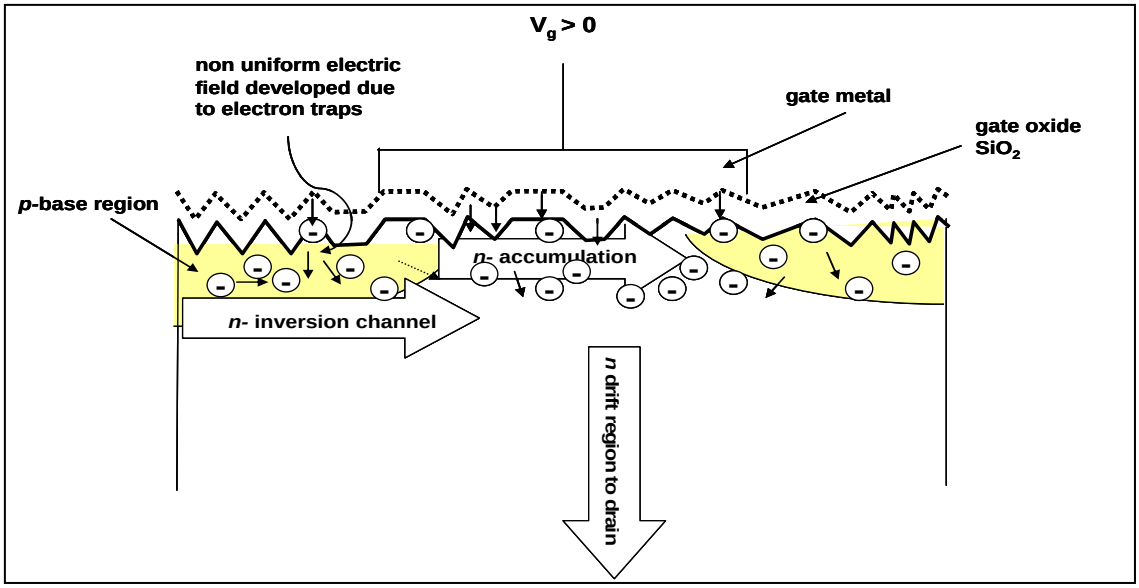

Figure 5: Illustration of trapped electrons in a rough SiO_2/SiC interface

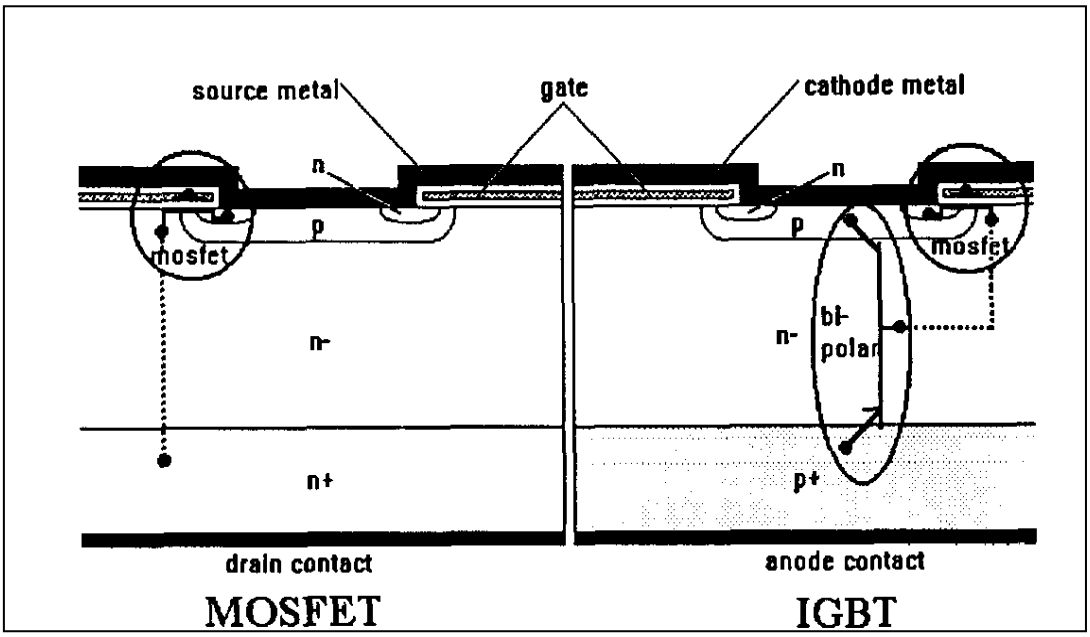

Figure 6: Comparison of MOSFET and IGBT structures [9]

2. LITERATURE REVIEW

MOSFETs, as discussed in Section 1.3 form the core of the power electronic devices. Silicon carbide power MOSFETs can potentially be used as switches for a wide variety of applications [10]. Metal oxide semiconductor capacitors (MOS-C) are the simplest of all MOS devices [3]. Capacitance is the primary observable in a MOS device. The MOS capacitance and voltage (C-V) characteristics provide the basic information required to predict the characteristics of more complicated MOSFETs, while the current and voltage (IV) characteristics determine the reliability of the dielectric layer on the semiconductor substrate. For this purpose, a brief review of MOS-C devices is given in the following section.

2.1 Characteristics of MOS Capacitor [3]

A MOS capacitor is a two terminal device consisting of a thin SiO_2 (dielectric) layer sandwiched between a metal contact and a semiconductor substrate. The metal contact on the oxide layer and a metal layer at the bottom of the substrate form the electrical connections. A MOS-C device can be understood by studying its energy band diagram. Fig. 7 shows the band energy diagrams for a metal, insulator and semiconductor. In the figure E_f denotes an important theoretical variable referred to as the Fermi energy which is defined as “the highest energy an electron assumes at T=0 K” [11]. The Fermi energy determines the statistical distribution of the electrons and does

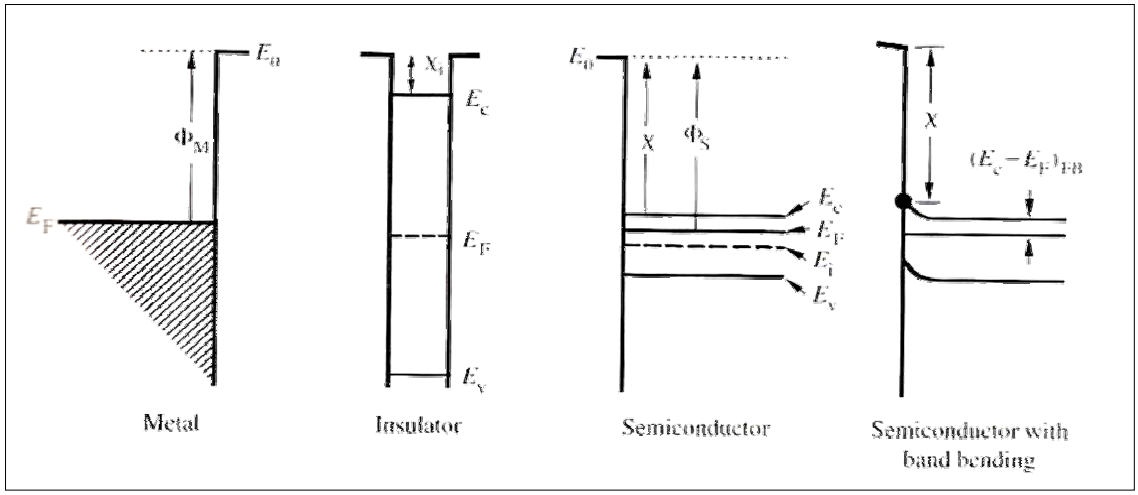

Figure 7: Energy band diagrams for metal, insulator and semiconductor [3]

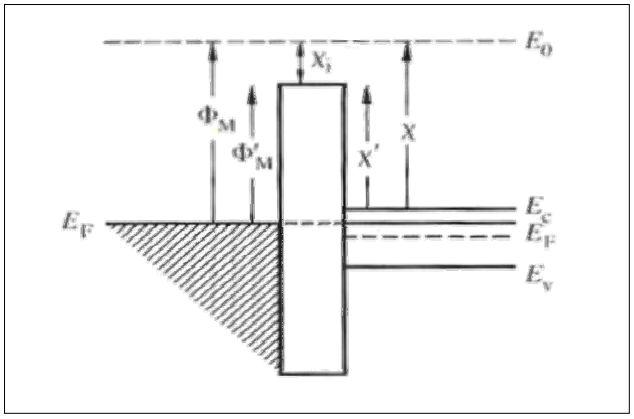

Figure 8: Equilibrium energy band diagram for an ideal MOS structure. The work function of the metal and the semiconductor are equal [3]

not correspond to an allowed energy level. The ledge at the top shows the minimum energy E_0 required by an electron to free itself from the atom. The difference in the energies (E_0-E_f) is the work function and is denoted by Φ ; Φ_m, Φ_i and Φ_s denote work the functions of a metal (M), insulator (I) and semiconductor (S), respectively. E_c and E_v denote the conduction and valance band energies of the semiconductor. The difference (E_0-E_c) is called the electron affinity and is denoted by χ. Fig. 8 shows the energy band diagram of an ideal MOS structure, where $\phi_M = \phi_S$. Fig 8 depicts the "flat band" of the MOS capacitor. In biasing, the semiconductor is grounded and only the gate metal voltage is changed from $V_G>0$ to $V_G<0$. As the barrier heights are fixed, the movement of the metal's Fermi level distorts the position of the semiconductor's Fermi level.

For an *n*-type semiconductor substrate, the application of positive bias $V_G>0$ lowers the Fermi level in the metal relative to the Fermi level in the semiconductor and causes a positive slope for the energy bands in both the insulator and semiconductor, as shown in Fig. 9a. In this condition the electron concentration is given by:

$$n = n_i \exp[(\frac{E_f - E_i}{kT})] \qquad \textbf{Eq 5}$$

The electron concentration increases as one approach the oxide-semiconductor interface, and the majority carrier concentration at the interface is greater than the bulk semiconductor concentration. This situation is called the accumulation. When a small negative voltage $V_G < 0$ is applied, the E_f in the metal is raised relative to E_f in the semiconductor. This causes a small negative slope for the energy bands in both the insulator and the semiconductor, as shown in Fig. 9c. In this condition the concentration

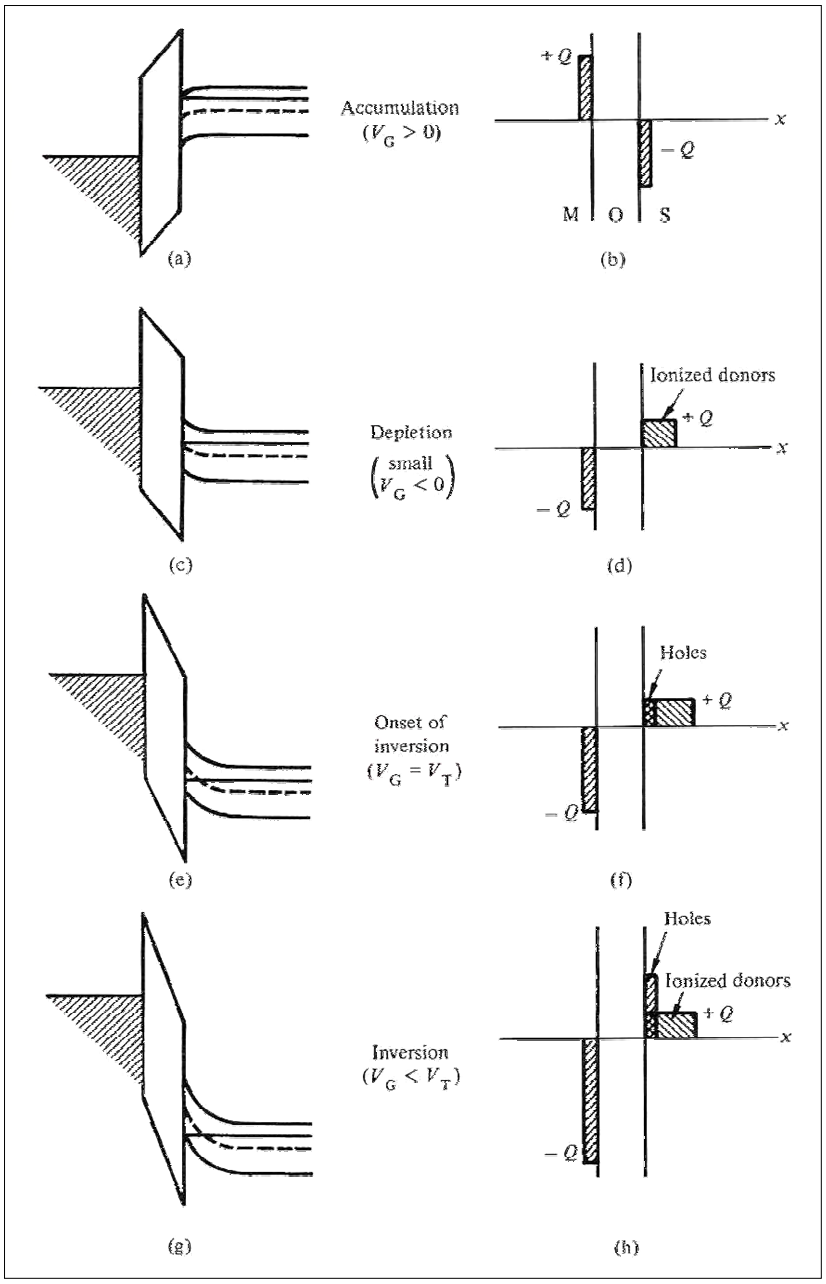

Figure 9: Energy band diagrams describing the static state in an ideal *n*-type MOS capacitor [3]

of the majority carriers (electrons) decreases at the interface depletion stage. With an increase in the negative biasing, the bands in the semiconductor. This condition is called the bend further. The hole concentration increases at the interface, and an inversion of the charge carrier polarity takes place. This situation is shown in Fig. 9e.

According to the equation,

$$p_s = n_i \exp[\frac{E_i(surface) - E_f}{kT}] = n_i \exp[\frac{E_f - E_i(bulk)}{kT}] = n_{bulk} = N_D \qquad \textbf{Eq 6}$$

the hole concentration p_s at the surface increases systematically from less than n_i when E_i (surface) < E_f, to n_i when E_i (surface) = E_f, to greater than n_i when E_i (surface) exceeds E_f. Clearly, the surface is no longer depleted when p_s= N_D for a special bias voltage $V_G = V_T$ (threshold voltage). With further increase in the negative bias $V_G < V_T$, p_s exceeds n_{bulk} = N_D. This mode of operation is called the inversion stage (Fig. 9e) in which the semiconductor surface changes its character from *n*-type to *p*-type. Thus, depending upon the bias voltage V_G, the semiconductor MOS-C undergoes three distinct changes called accumulation, depletion and inversion. The dividing line at $V_G = 0$, where no band bending occurs, is called the flat band region.

2.2 Potential Gate Dielectrics Used in SiC MOS Devices

As discussed in Section 1.2.3, silicon carbide has superior material properties such as wider band gap, higher breakdown field and higher thermal conductivity compared to silicon. The bulk properties listed in Table 1 are sufficient for many useful applications of semiconductor materials. However, a large variety of applications are critically dependent on both the bulk and the surface properties. Of all the semiconductor materials available, only silicon and silicon carbide permit surface defects to be passivated to the required levels for a wide range of device applications [12]. Silicon

carbide, like silicon, forms SiO_2 as a native oxide. However, it has been shown that the oxide layer formed on the SiC surface is not of electronic device quality due to the inferior bulk wafer quality of SiC and inherent problems related to the clustering of carbon during oxidation. Lipkin, et al showed that for a reliable gate dielectric, the material's dielectric constant should be higher than that of SiC [13]. This is because the maximum blocking voltage is often limited by the field in the dielectric rather than the semiconductor. Ideally, the higher the dielectric constant, the lower the electric field in the insulator. The product of the relative dielectric constant (ε) and the safe operating electric field (E_o) should be lower than that of SiC. Of all the insulators currently under investigation, AlN and TiO_2 look most promising based on this requirement.

The insulators have to perform two major functions, providing high energy barriers to block the electron and hole injection from the semiconductor and the gate metal. An insulator must also be defect free, with uniform deposition on the surface of the semiconductor [14]. Due to the ease of oxidation of SiC and its good insulating properties, SiO_2 is preferred over other dielectric materials. In addition, the breakdown field strength at high temperatures was observed to be highest for SiO_2 of a number of insulators studied [13]. Table 2 shows a list of the potential dielectric materials which have been studied for MOS devices. Researchers have noted that the surface of the bulk substrate must be uniform in order to provide a smooth interface between the insulator and surface, which facilitates high inversion channel mobility by decreasing the number of interfacial traps [15]. In the following sections, the oxidation and passivation methods that can be used to decrease the number of interfacial traps will be discussed.

Material	Dielectric Constant	Critical Field (MV/cm)	Operating Field (MV/cm)	εE_0 (MV/cm)
SiC	10	3	3	30
Thermal SiO_2	3.9	11	2	7.8
Deposited SiO_2	3.9	11	2	7.8
Si_3N_4	7.5	11	2	15
ONO	6	11	~2	~12
AlN	8.4	10-12	~3	~30
AlO:N	12.4	8	~1	~12
$Si_xN_yO_z$	4-7	11	~2	~8-14
$(Ba,Sr)TiO_3$	75-250	2	_0.1	~8
TiO_2	30-40	6	~0.2	~4
Ta_2O_5	25	10	~0.3	~7.5

Table 2: Electrical properties of insulators [13].

2.3 Thermal Oxidation of Silicon Carbide

Thermal oxidation of silicon carbide leads to the formation of silicon dioxide. The surface of the SiC, oxidation conditions and the post oxidation processing methods all affect the density of interfacial defects. In this section, the kinetics and mechanisms of the oxide growth will be discussed.

The oxidation kinetics of SiC are generally described using the Deal and Grove model. This model was originally formulated to describe the oxidation of single crystal silicon in both the linear and the parabolic phases [16]. According to this model, the silicon oxidation kinetics follows the relationship given by [17]:

$$x_0^2 + Ax_0 = B(t + \tau) \qquad \textbf{Eq 6}$$

where, x_o is the total oxide thickness

$$A \equiv 2D_{eff}C^*(\frac{1}{k} + \frac{1}{h})$$

$$B \equiv \frac{2D_{eff}C^*}{N_1}$$

$$\tau \equiv \frac{(x_i^2 + Ax_i)}{B}$$

D_{eff} is the effective diffusion coefficient

k and h are the rate constants

C^* is the equilibrium concentration of oxidant in the oxide

x_i is the thickness of the initial oxide layer on the surface

N_1 is the number of oxidant molecules incorporated into a unit volume of the oxide layer

Equation 4, when solved for quadratic roots with the limiting case of relatively large times $t \geq\geq A^2/4B \,\&\, t \geq\geq \tau$ gives:

$$x_0^2 \cong Bt \qquad \textbf{Eq 7}$$

This is a parabolic law describing oxidation over relatively long periods. For relatively short oxidation times $t \leq\leq A^2/4B$, the solution is given by:

$$x_0 \cong \frac{B}{A}(t+\tau) \qquad \textbf{Eq 8}$$

This is a linear relationship. The coefficient B is the parabolic rate constant, and the ratio B/A is the linear rate constant. This general relationship is shown in Fig. 10. Here, the experimental data obtained by Deal and Grove clearly follow the linear and parabolic relationships at relatively short and long oxidation times, respectively. Costello and Tressler observed that SiC single crystals follow the general relationship described for the oxidation of silicon, noting that the oxidation rate for (000-1) C face terminated SiC single crystal is higher for a (0001) Si face terminated single crystal [16]. Song, et al proposed a detailed and modified Deal Grove model for the thermal oxidation of SiC [18]. According to their modified Deal Grove model, the oxidation of SiC follows the following chemical reaction:

$$SiC + 1.5O_2 \rightarrow SiO_2 + CO \qquad \textbf{Eq 9}$$

In this model, the out-diffusion of the CO molecules is accounted for, and the equation modified accordingly. Figs. 11-13 show the experimental thickness of the oxide layers formed on 4H-SiC single crystals with (000-1) C face, (11-20) *a* face and (0001) Si face terminations, respectively. These results indicate that the growth rate on the C face is

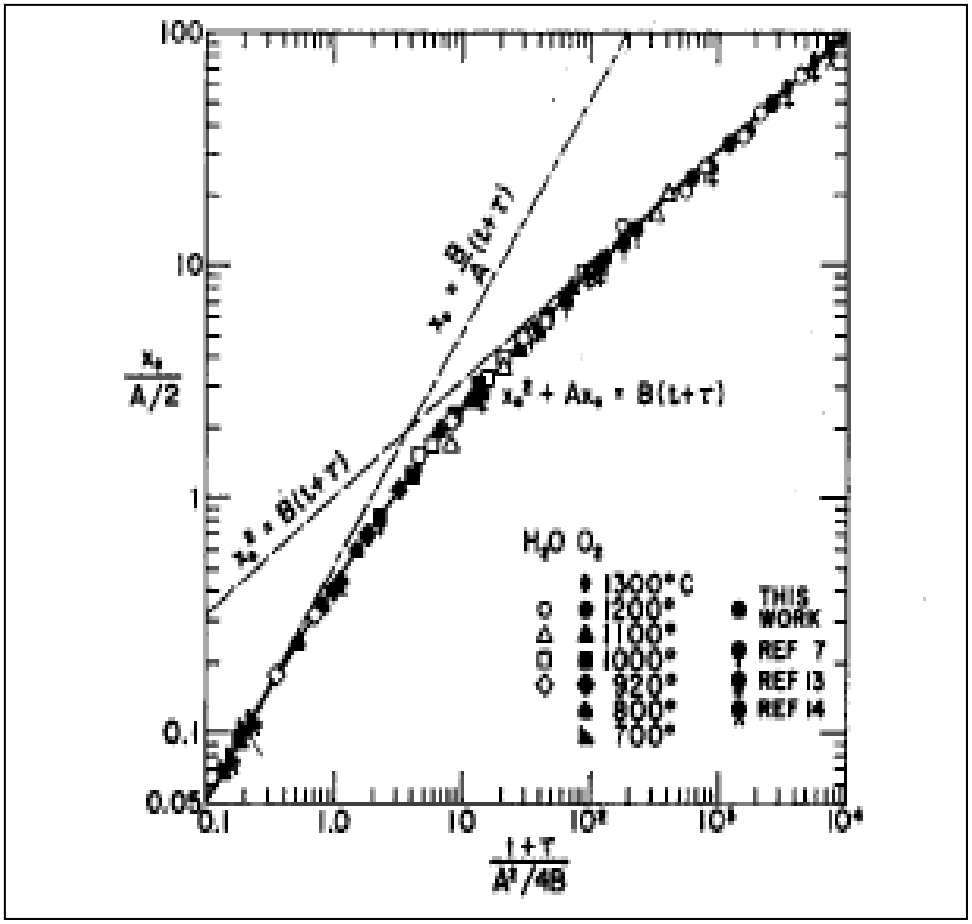

Figure 10: Experimental data for the oxidation of silicon showing the linear and parabolic relationships for short and long times, respectively [17]

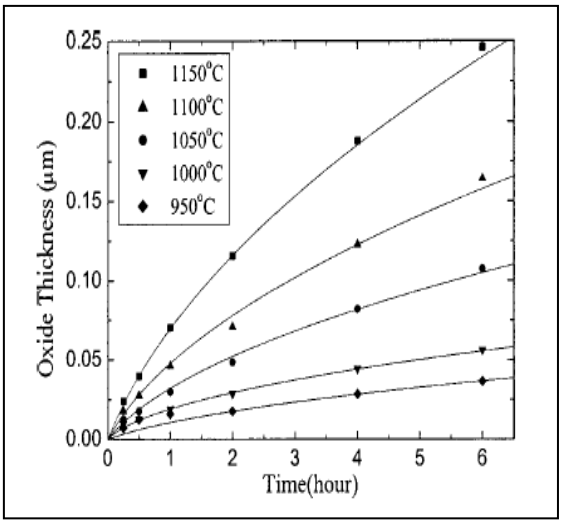

Figure 11: Oxidation rate of C face 4H-SiC [18]

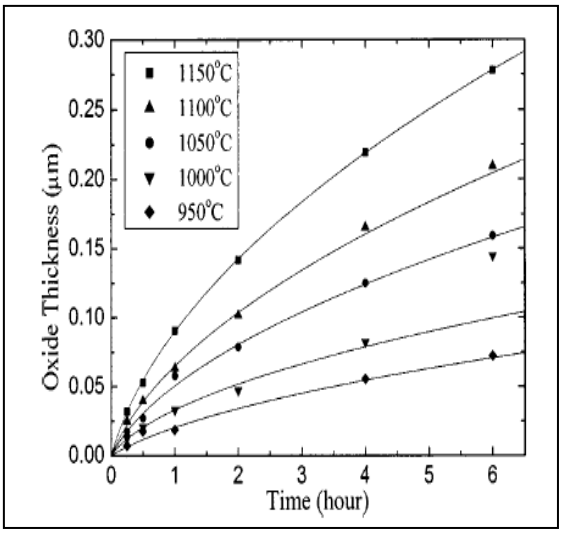

Figure 12: Oxidation rate of *a* face 4H-SiC [18]

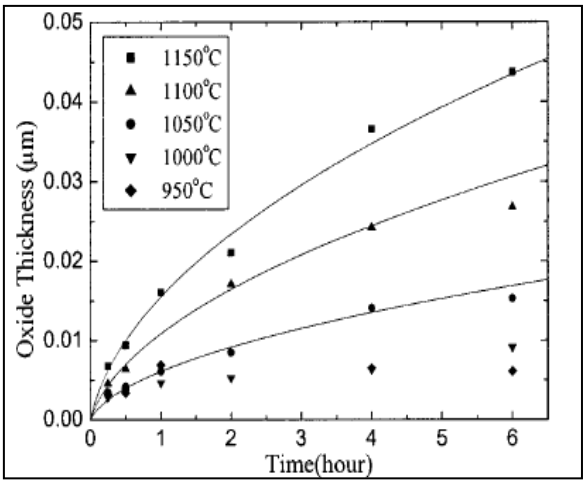

Figure 13: Oxidation rate of Si face 4H-SiC [18]

higher than that on the *a* face which is higher than the rate on the Si face. In addition, the surface morphology and doping concentrations play a key role in the oxidation rates of SiC. SiC electronic devices are usually manufactured on Si face terminated surfaces. However, C face SiC has superior properties such as higher oxidation rate and smoother surface compared to the Si face [19]. Table 1 clearly indicates that 4H-SiC has better electrical properties like wide band gap and high electron and hole mobilities compared to other polytypes of SiC. For these reasons the 4H-SiC polytype has been extensively studied.

2.4 Oxide Traps in 4H-SiC Polytype MOS Devices

The electrical properties described above have made SiC a promising candidate for high temperature and high frequency applications. Among the polytypes available, 4H-SiC has the highest band gap and highest bulk electron mobility [20]. However, the electron mobility of the 4H-MOSFET inversion channel has been observed to be highly degraded. Afans'ev, et al [20] have reported that for 4H-SiC, the mobility values lie below 20 cm^2/Vs. This value is very low when compared to the reported bulk mobility value of ~ 700 cm^2/Vs at a donor concentration of $1x10^6$ cm^{-3} and 300K. This degradation in the channel mobilities has been attributed to a high density of interface defects, which trap electrons from the inversion layer at the SiC/SiO_2 interface. These interface defects originate due to intrinsic defects at the SiO_2/SiC interface, and the effect on channel mobility is higher in 4H-SiC compared to 6H-SiC. This is because the defect concentration is largest at ~ 2.9 eV above the 4H and 6H valance band edges. Thus, for 6H-SiC (E_g ~ 3 eV), most of these states lie in the conduction band, while for 4H-SiC (E_g ~ 3.3 eV), most of these states lie in the band gap. An electron density of 10^{13} $cm^{-2}.eV^{-1}$ is

trapped at the interface and removed from the 4H-SiC inversion layer [21]. These electrons are immobile and cannot contribute to the charge conduction in the channel. In addition, they create a Coulomb repulsive force that also perturbs the motion of other electrons in the channel. This reduces the effective channel mobility. Rudenko and Olafsson [22] used thermally stimulated current (TSC) and room temperature CV techniques to study the interface traps for 4H-SiC/SiO_2. They observed that the electron traps near the 4H-SiC conduction band edges are composed of two groups with different filling and emptying mechanisms. The filling mechanism of the first group is temperature independent, and its emptying mechanism is a strong function of the electric field at the interface. This indicates that the traps are located close to the interface with activation energies of about ~ 0.1 eV. In contrast, the second group of traps depends on thermal energy for its filling process. Electric field was observed to have no effect on the emptying process, unlike the first group of traps. It can be assumed that both types of interfacial defects are energetically located near the 4H-SiC band edge and are spatially distributed from the interface into the oxycarbide transition region [22]. Pre-/post-oxidation treatments of the SiC/SiO_2 interfaces can be used to minimize the density of interfacial traps. This mechanism is explained below.

2.4.1 NO Passivation on 4H-SiC MOS Capacitors

From the above discussion, it can be concluded that the presence of interface defects in SiC/SiO_2 structures could be due to the carbon clusters and near interfacial defects in the oxide layer. Chung, et al [23] have demonstrated that using NO as a post-oxidation annealing technique will decrease the density of interfacial traps (D_{it}). They suggested that the introduction of N atoms that are thus available to bond with C atoms

and C clusters could be a passivation mechanism. However, the exact nature of passivation is not fully understood. Dhar, et al [24] demonstrated that the density of interfacial traps is dependent on the SiC surface termination, observing that the D_{it} of SiO_2/4H-SiC was considerably higher near the semiconductor conduction band edge for dry thermal oxides on the C face compared to the Si and *a* faces. However, passivating the oxide with NO followed by hydrogen decreased the D_{it}. Anthony, et al [25] studied the reliability of wet and dry oxides on the *n*-type 4H-SiC and reported that the oxides formed by a dry process were able to sustain a higher electric field before break down compared with those formed using a wet process, in spite of having similar D_{it} values. This was thought to be due to the post-oxidation processing techniques used after the dry oxidation process to form ohmic contacts.

2.4.2 Hot Ion-implantation and Surface Roughness

The doping of SiC is not possible using a standard diffusion process because the thermal diffusion coefficients of the desired dopants are extremely small compared to those for Si. Hence, ion-implantation must be used to dope SiC substrates to the desired levels. However, the ion implantation technique used for SiC doping has problems associated with it. A post ion implantation annealing process is performed after hot-ion implantation to minimize the surface damage caused during implantation and also to move the dopant atoms into electrically active substitutional lattice positions. Stoichiometric disturbances are caused during implantation. This results in non-uniform Si, C atom and Si, C vacancy distributions [26]. These problems combine to produce a poor surface quality, which in turn leads to poor device performance. Step bunching is also observed in SiC wafers after the post implantation annealing process. This effect is

attributed to the sublimation and re-deposition of Si species such as Si, Si_2C and SiC_2. Rao [25] reported that the depth and width of the groves increased with increasing annealing temperatures. In addition, ion implantation damage leads to damage induced stress, which also results in step bunching. The sublimation of Si species also leads to the loss of both the surface material and dopants during annealing. It has been demonstrated that this annealing damage can be prevented by covering the SiC surface with a cap composed of AlN or graphite [27]. Conventional dielectric encapsulation using SiO_2 and Si_3N_4 did not prove effective due to their volatility in the temperature range of 1400-1700 ^{0}C. Fig. 14 shows atomic force microscope (AFM) images of the implanted and annealed samples both with and without an AlN protective cap. The sample annealed with the cap is noticeably smoother.

The use of AlN encapsulation protects the surface at 1650 ^{0}C if the annealing time does not exceed 10 min. Most previous research has focused on the (0001) Si face, and very little information is available for the (000-1) C face. In this research study *n*-type (000-1) C face SiC wafers were used for the investigation of the surface damage induced by the ion implantation and annealing post-implantation process. A graphite cap was used as a protective encapsulation.

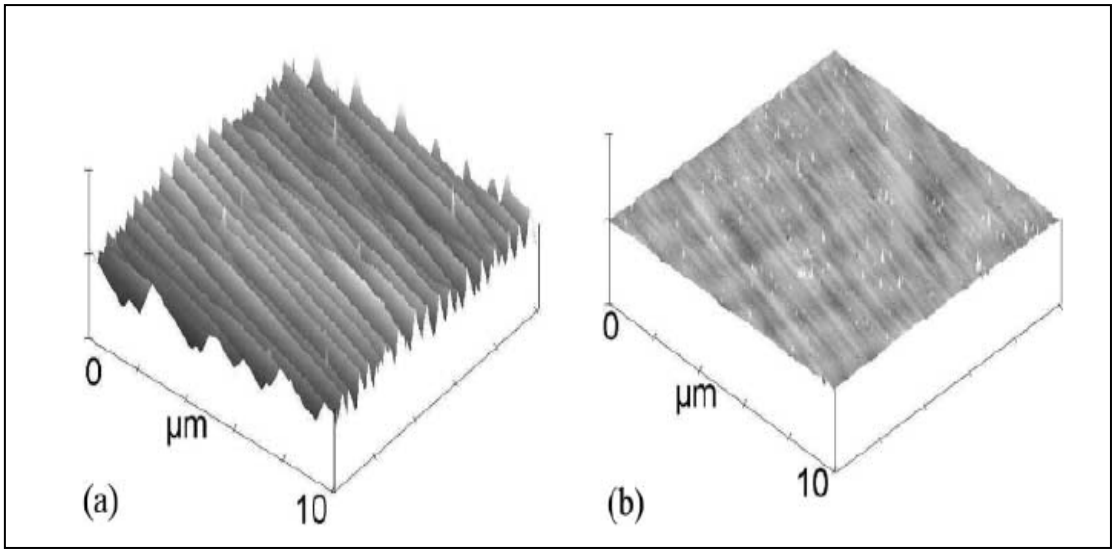

Figure 14: Si face 4H-SiC samples annealed at 1600 ^{0}C in Ar for 15 min a) without b) with AlN encapsulation [26].

3. EXPERIMENTAL

This chapter describes the experiments performed to examine the influence of the surface roughness caused by hot ion-implantation and high temperature post annealing treatment on the SiO_2/4H-SiC interface. 4H-SiC metal oxide semiconductor capacitors (MOS-C) were fabricated using standard fabrication processes and tested for dielectric field breakdown using current (I) and voltage (V) measurements. The experimental setup and process parameters used for fabrication of the 4H-SiC MOS-C will be described in detail.

3.1 4H-SiC Wafer Cleaning

A 2" *n*-type (000-1) C face 4H-SiC wafer with 5 μm thick *n*-type epi-layer (doped with nitrogen at 8 x 10^{15}/cm^3) was procured from Cree Inc., Durham, NC. This wafer was diced into 5 x 5 mm square pieces. These smaller pieces were used as starting substrates for the fabrication of the *n*MOS-C. Cleaning was performed in two steps: organiccleaning followed by a second step of standard RCA cleaning. Organic cleaning was first performed to remove the adherent dirt and dust using the following sequential steps:

i. 5 min ultrasonic cleaning in acetone
ii. 5 min ultrasonic cleaning in tetrachloroethylene (TCE)
iii. 5 min ultrasonic cleaning in acetone
iv. 5 min ultrasonic cleaning in methyl alcohol
v. 5 min ultrasonic cleaning in methyl alcohol

vi. Rinsed in de-ionized (DI) water for 5 min

vii. Immersed in buffer oxide etchant (BOE) for 4 min to remove any native oxide on the samples

viii. Rinsed well in DI water for 2-3 min

After the initial organic cleaning, RCA cleaning was performed to clean the samples of organic contamination, alkali and hydroxyl ions. The following steps were used.

i. Samples were immersed in 1:1 sulfuric acid (H_2SO_4) : hydrogen peroxide (H_2O_2) for 15 min

ii. Rinsed in DI water

iii. Immersed in BOE for 1 min to etch the oxide layer formed during the first step

iv. Immersed in 5:1.5:1.5 DI water: ammonia hydroxide (NH_4OH): hydrogen peroxide

v. Rinsed in DI water

vi. Immersed in BOE for 1 min

vii. Immersed in 5:1.5:1.5 DI water: hydrochloric acid (HCl): hydrogen peroxide

viii. Rinsed in DI water

ix. Immersed in BOE for 1 min

x. Rinsed well in DI water for 2 min and dried with nitrogen gas

The samples were then stored under vacuum until further use.

3.2 Topography Analysis

The surfaces of the cleaned samples were studied using atomic force microscopy (AFM) at Vanderbilt University. This step was repeated before every stage of the

fabrication of the *n*MOS-C in order to observe any topographical changes. Results and will be discussed in the Result and Discussion section.

3.3 Hot-Ion Implantation

The RCA cleaned samples were loaded into the heavy ion implantation chamber of the 6SDH-2 Pelletron accelerator, which is shown in Fig. 15. The samples inside the chamber were heated to 700 ^{0}C using a borographite resistance heater. The 6SDH-2 Pelletron is a tandem accelerator in which both ends of the accelerator are maintained at ground potential with respect to the high voltage terminal located at the center of the accelerator. Two sources as shown Fig. 16 are used to generate ions. The RF source generates helium ions, and the source for negative ions by cesium sputtering II (SNICS II) is used to produce negative ions of aluminum, nitrogen, phosphorous, gold, etc. The Pelletron accelerator can produce ions in the range of 100 KeV to 5 MeV. For the current work, aluminum and nitrogen were used as the *p*-type and *n*-type dopants, respectively. Box profiles of the dopant concentrations as a function of depth were generated using SRIM (stopping and range of ions in matter) and TRIM (transport of ions in matter) simulation software. Aluminum ions with a range of concentrations of 8.00×10^{15} ions/cm^3, 5.00×10^{17} ions/cm^3 and 6.00×10^{19} ions/cm^3 were used to dope (000-1) C face 4H-SiC samples. These concentrations were chosen based on the shallow doping concentrations used for source and drain implantations of MOSFET devices. Fig. 17 shows the concentration as a function of depth generated using TRIM. To bring the lowest energy ions to the SiC surface, a layer of molybdenum (Mo) with thickness in the range of 1000 to 1500 ^{0}A was put down prior to implantation.

Figure 15: 6SH-2 Pelletron ion beam accelerator

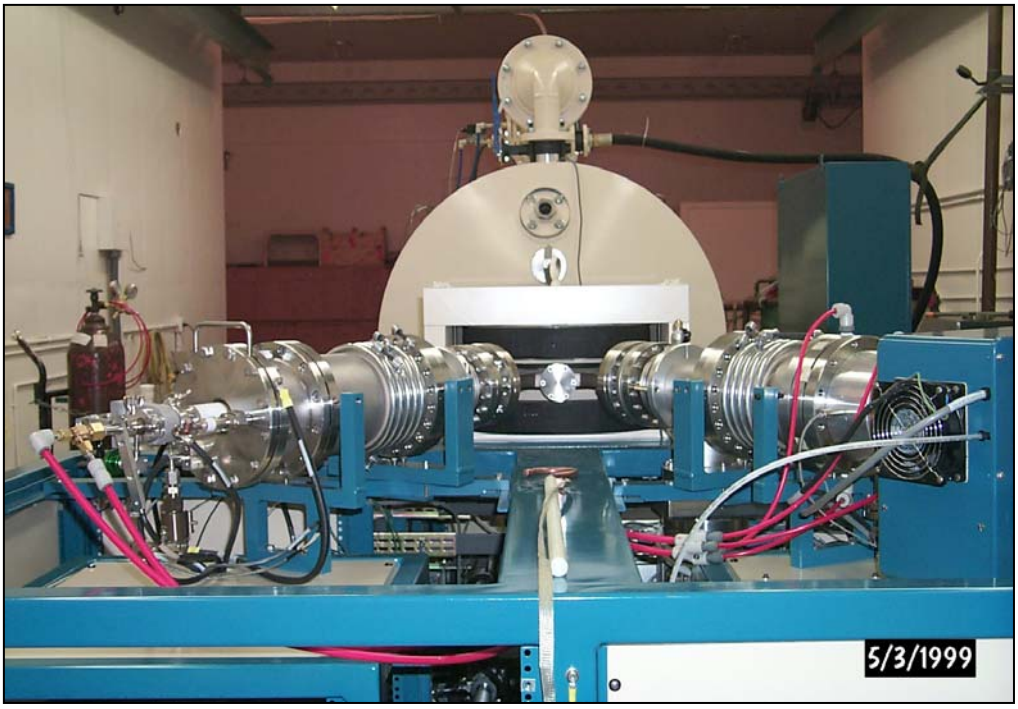

Figure 16: Ion sources. The SNICS source on the left was used for nitrogen and aluminum doping

The depth of penetration of nitrogen ions into the 4H-SiC substrate was restricted to 3500 ^{0}A, and the energies for implantation were in the range of 125 KeV to 225 KeV. Implanted species generally occupy the interstial lattice of the substrate and thus do not contribute to the electrical conduction of the material. These impurities must be made electrically active by thermal annealing.

3.4 High Temperature Thermal Annealing

The implanted samples were shipped to Vanderbilt University for the AFM studies. The annealing chamber shown in Fig. 18 was used for high temperature activation. The chamber was pumped down to 30 mTorr pressure using a mechanical roughing pump. A diffusion pump was then used to further pump down the chamber to $6x10^{-7}$ Torr. The implanted samples were annealed in an argon atmosphere. The activation annealing of nitrogen and aluminum doped samples was performed both with and without a carbon cap. The carbon cap encapsulation technique is discussed below. The samples, both with and without caps, were placed face down inside a graphite pill box which was then placed between the two heating strips as shown in Fig. 19.

3.4.1 Carbon Capping Procedure

The carbon cap was prepared on the samples by spinning photoresist for 30 sec at 4000 rpm. AZ5214E negative photoresist was used for this process. The thickness of the photoresist was measured using a KLA-Tencor profilometer. The thickness of the as-spun samples was around 16000 ^{0}A. The samples with photoresist were soft baked on a hot plate for 1 min at 100 ^{0}C. The same activation annealing chamber was used for the hard bake. The samples were placed on the heating filament and hard baking was performed in argon atmosphere at 600 ^{0}C for 30 min.

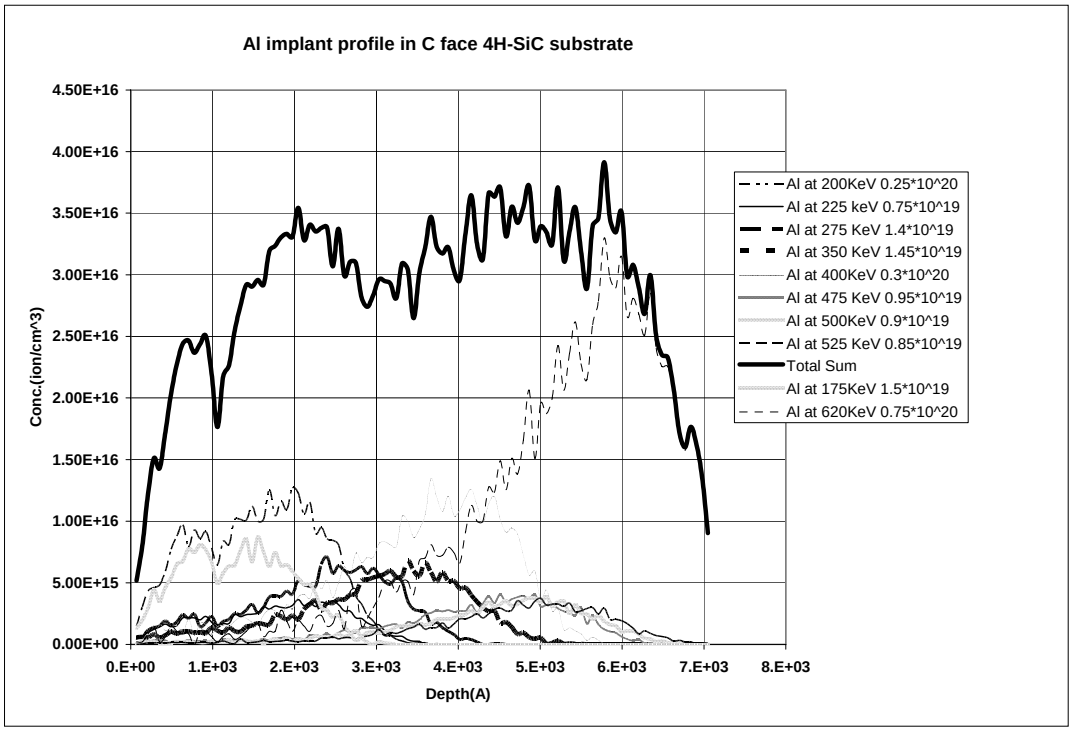

Figure 17: Box profile for Al ions generated using TRIM

Figure 18: Chamber used for activation annealing

Figure.19: Graphite sample holder

A pyrometer was used to monitor the temperature. At this temperature the volatile components from the photoresist are vaporized, and the samples are left covered with carbon cap. The thickness of the carbon cap was measured using RBS and the profilometer and found out to be approximately 1500 ^{0}A. These carbon capped samples were subsequently used for activation annealing.

3.4.2 Aluminum Activation Annealing Process

For aluminum dopants, the samples with and without carbon caps were placed facing down in a graphite pill box. The pill box was placed between the heating filaments and the chamber was pumped down to $6x10^{-7}$ Torr. Argon gas was allowed to flow through the chamber. The temperature of the chamber was increased from 25 ^{0}C to 1650 ^{0}C at a ramp rate of approximately 2 ^{0}C/sec using a variac. The samples were annealed at this temperature for 30 min. After 30 min, the samples were removed from the chamber after the chamber was to cooled to room temperature in an Ar atmosphere.

3.4.3 Nitrogen Activation Annealing Process

Nitrogen doped samples were annealed at 1450 ^{0}C for 30 min in argon. The same ramping rate of 2 ^{0}C/ sec was used for heating the samples. The cooled samples were then removed from the chamber and stripped of the cap using reactive ion etching.

3.5 Reactive Ion Etching (RIE) to Strip the Carbon Cap

The RIE chamber shown in Fig. 20 was used to remove the carbon cap from both the aluminum and nitrogen doped samples. The samples were loaded into the chamber which was then flushed with nitrogen gas to remove residual gases in the chamber. The chamber was then pumped down to approximately 20 mTorr. Oxygen gas was passed into the chamber at an approximate flow rate of 65-67 sccm (standard cubic centimeters

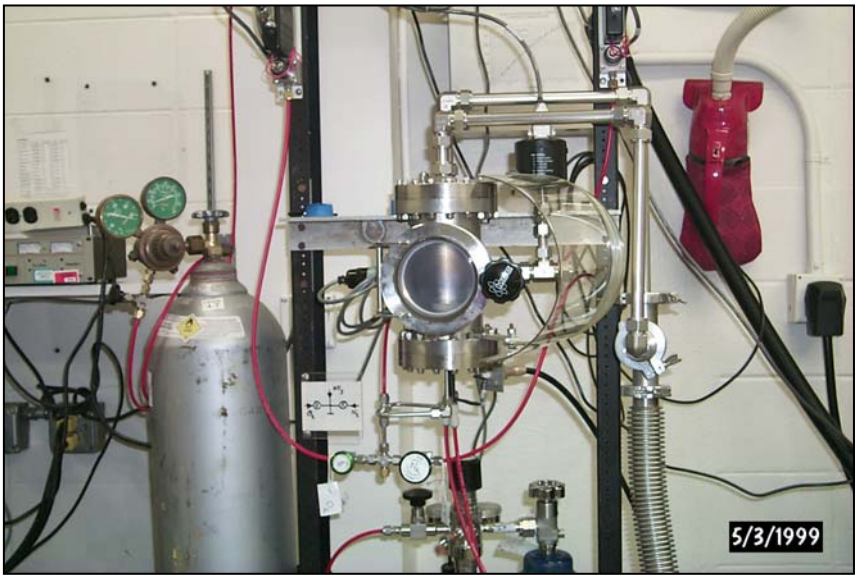

Figure 20: Reactive ion etching (RIE) chamber used for carbon cap ashing

per minute). The RF power was then turned on and oxygen plasma generated. The samples were etched for 30 min in the oxygen plasma. After 30 min, the samples were removed and cleaned as described in Section 3.1. The samples were then shipped to Vanderbilt University for further AFM imaging.

3.6 Oxidation of C face 4H-SiC Samples

The horizontal tube furnace used for oxidation is shown in Fig. 21. The furnace was installed in a fume hood as a safety precaution. The furnace in the idle condition is always under vacuum at 900 ^{0}C. The furnace was ramped to 1050 ^{0}C at a ramp rate of 5 ^{0}C/min with argon flow of 500 sccm through the tube. Once the furnace reached 1050 ^{0}C, argon was stopped and oxygen at 500 sccm was passed through the furnace for 3 hrs. Upon completion of 3 hrs, the oxygen flow was stopped, and the samples were annealed in argon at 577 sccm for 30 min. The temperature of the furnace was then raised to 1175 ^{0}C at a ramp rate of 5 ^{0}C/min. At this temperature the argon flow was stopped, and nitric oxide (NO) gas was passed through the tube for 2 hrs. After the 2 hrs of passivation, NO gas was stopped, and the furnace was cooled to 900 ^{0}C at a ramp rate of 10 ^{0}C/min in flowing argon. The samples were removed and patterned for MOS capacitors.

3.7 Patterning

The oxidized sample was mounted on a 200 mm silicon wafer using silver paste. Positive photoresist AZ 5214-EIR procured from Clariant Corporation was spin coated on the sample for 30 sec at 4000 rpm. The silicon wafer was then soft baked using a hot plate for approximately 1 min at 100 ^{0}C. The dried sample was loaded into a Karl Suss contact mask aligner. A chrome plated glass mask with the pattern shown in Fig. 22 was

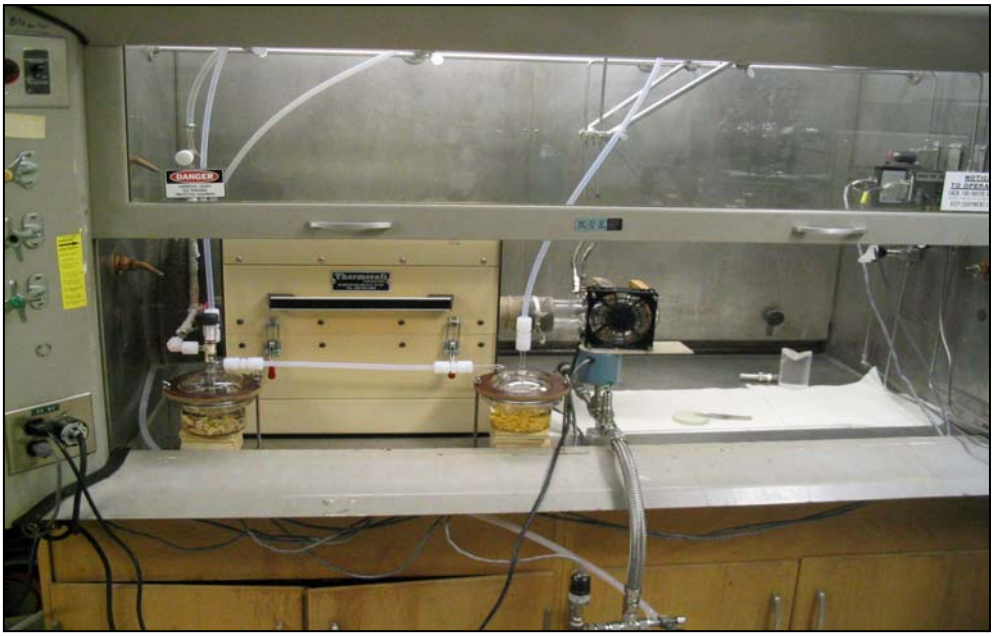

Figure 21: Horizontal tube furnace used for oxidation of 4H-SiC samples

used for lithography. The samples were exposed to ultra violet light from mercury lamp for 30 sec. The sample was removed from the aligner and immersed in a developer prepared with one part of AZ developer in three parts of DI water. The patterned sample was dried in dry nitrogen gas, then sent for metal contact deposition.

3.8 Contact Metal Deposition

The patterned samples were loaded into the sputter chamber shown in Fig. 23 for Mo and Au contact metal deposition. The chamber was then pumped to 10^{-3} torr using a roughing pump, then to $5x10^{-7}$ torr approximately using a turbo-molecular pump. Ar gas at the rate of 106.4 sccm and a pressure of 20mT was supplied to the chamber. The chamber was flushed with Ar for 1 min. Chilled water was turned on, to keep the sputter gun from over heating. The power supply was turned on, and the voltage was adjusted to create a plasma arc. The voltage was adjusted to stabilize the plasma. Mo and Au targets were used to sputter Mo and Au thin films. After the set time of 5 min, an 800 ^{0}A thick Mo film was deposited at 0.25 amp of current. The voltage was lowered to zero, and the power is turned off. The Au sputter is target was connected to DC magnetron power source and the voltage was turned up slowly to again generate plasma. After the pre-sputter time, the samples were coated with Au for 4 min. The Au film coating was approximately 600 A. The power was turned off, and the samples were removed from the chamber. The next step in the fabrication of the MOS capacitors was pattern lift-off.

3.9 Photo-resist Lift-off

The sputtered samples were removed from the silicon wafer and immersed in beaker with acetone for 5-8 min. The photo resist layer was observed to separate from the samples. The samples were then rinsed in acetone and ethanol for complete removal of

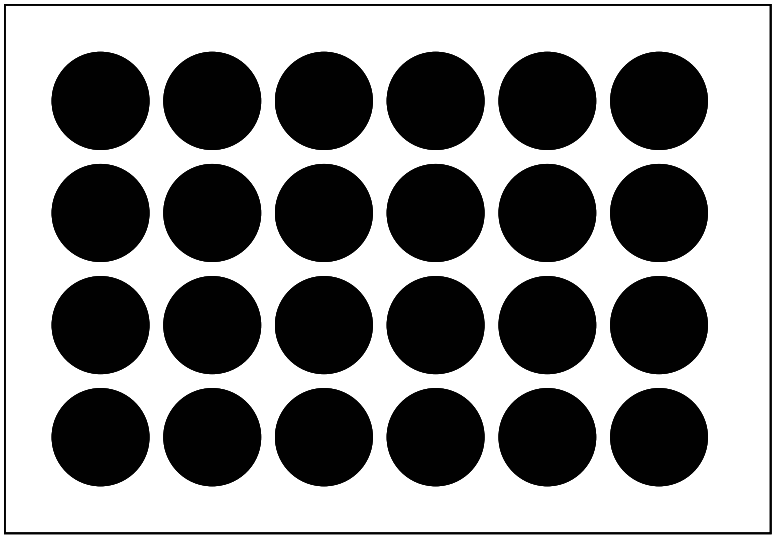

Figure 22: Chrome plated glass mask pattern used for lithography

Figure 23: Sputter chamber used for contact metal deposition

the photoresist layer. The samples were then cleaned in DI water and dried in nitrogen gas.

3.10 Electrical Testing

Capacitance-voltage (CV) and current-voltage (IV) measurements were performed on the MOS capacitors which were fabricated as described above. The following sub-sections describe the gate oxide reliability testing procedure.

3.10.1 Capacitance–Voltage (CV) Measurements

Keithley's CV probe tester shown in Fig. 24 was used to extract the CV characteristics of the MOS capacitors. The C-face 4H-SiC substrate was connected to ground, and the gate metal contact was biased. The capacitance measurements were simultaneously made in quasi-static and high frequency (100 KHz) modes starting from accumulation region and ending in depletion. The software provided with probe tester calculated CV characteristics of the MOS capacitors. The CV results obtained are discussed in the Results and Discussion section.

3.10.2 Current-Voltage (IV) Measurements

The IV measurements were performed on the MOS capacitors using the Keithley's IV probe tester which is shown in Fig. 25. The C-face 4H-SiC substrate was connected to ground, and the gate metal was biased. The current density of 10^{-3} amp/cm^2 was set for the breakdown limit. All the devices were tested until the gate oxide failed. The results obtained from IV tests are explained under Results and Discussion section.

Figure 24: Keithley's CV probe tester

Figure 25: IV probe teste

4. RESULTS AND DISCUSSION

4.1 AFM Results

As described in the previous section, all the samples were shipped to Vanderbilt University for AFM analysis before the start of new a process for the fabrication of MOS capacitors. AFM was done in tapping mode with different scan sizes.

4.2 AFM Results for Virgin and Implanted C-face 4H-SiC Samples

Four pieces of as received 5 mm x 5 mm *n*-type C-face 4H-SiC were labeled ‘A to D’ and shipped to Vanderbilt University for AFM studies. Figs 26 - 30 show the AFM images of the samples. The root mean square (RMS) roughness values were calculated by taking the average of RMS values obtained at two different locations on each sample. Samples A and B were used as standard samples to compare the surface topology with the oxidized, ion implanted and activation annealed samples. Table 3 shows the sample number, ion implantation species used, activation annealing conditions and average RMS roughness values. Samples C and D were implanted with aluminum (*p*-type) and nitrogen (*n*-type) species respectively. Activation annealing was performed on both these samples, and both were sent for AFM analysis. These samples along with samples A and B were oxidized in horizontal tube furnace as described in Section 3.6. A thin oxide layer of approximately 65 nm was grown on the surface. Samples ‘A to D’ were then sent again for AFM analysis to determine average RMS roughness. Afterward, the oxide layer was etched in 5 % strength BOE for 10 min. The samples were thoroughly cleaned and shipped again for final AFM analysis.

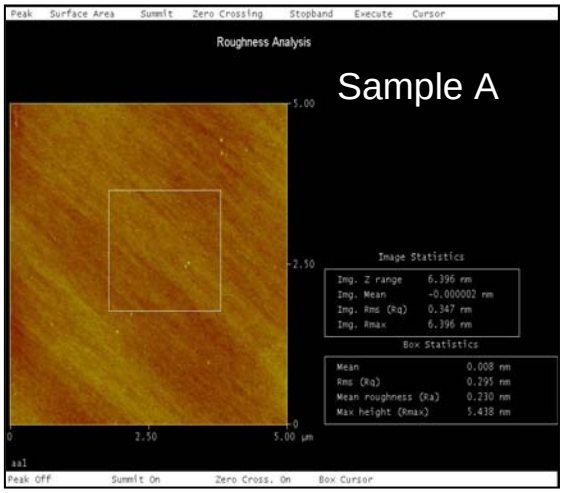

Figure 35: AFM image of virgin 4H-SiC (Sample A) at region 1

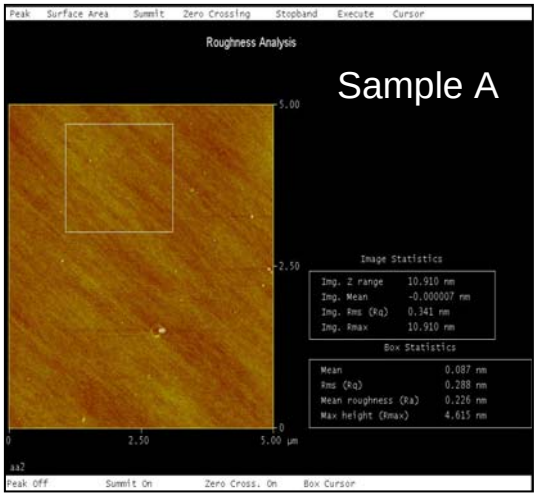

Figure 36: AFM image of virgin 4H-SiC (Sample A) at region 2

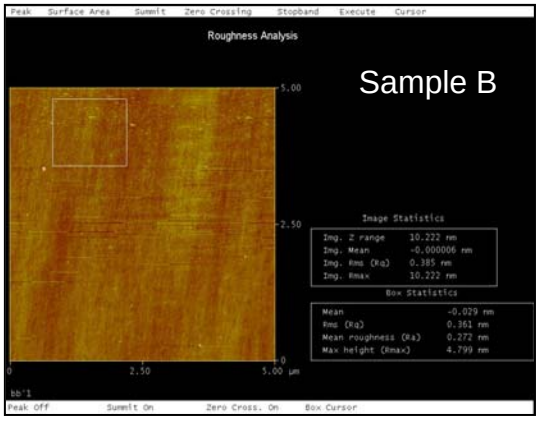

Figure 37: AFM image of virgin 4H-SiC without NO anneal (Sample B)

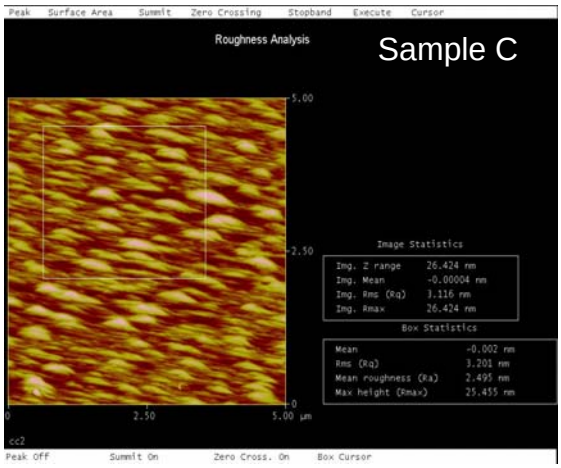

Figure 38: AFM image of N doped 4H-SiC (Sample C)

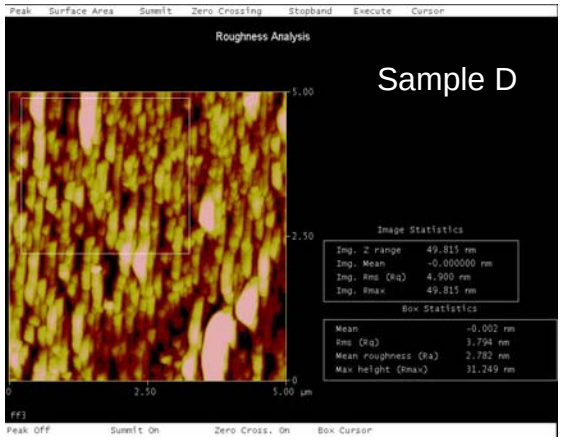

Figure 39: AFM image of Al doped 4H-SiC (Sample D)

Table 3 summarizes the average RMS roughness values after each stage of AFM analysis.

The average RMS roughness value for Al doped samples was observed to be greater than N doped samples. There was no significant change in the RMS values of oxidized samples. This can be attributed to the conformal oxidation of the C- face 4H-SiC samples. However, the oxide etched samples showed significant change in the roughness values. This could be due to the surface roughness developed during hot ion implantation and the subsequent activation annealing which exposed *a*-face (11-20) and Si-face (0001) surfaces. As explained in Section 2.3, the rate of oxidation of 4H-SiC is strongly dependent on the surface orientation. This may contribute to roughness of the surface after oxide etching. Figure 31 shows the bar chart representation of Table 3. The average RMS roughness of the Al doped samples is greater compared to virgin and N doped samples. Hence, for the further studies only C face 4H-SiC samples doped with different doses of Al species were used for AFM analysis.

4.2.1 AFM Results for Carbon Capped Samples

Samples 'E and F' and 'G and H' were implanted with Al at a doping concentrations of 5 x 10^{17} ions/cm^3 and 6 x 10^{19} ions/cm^3, respectively. Out of the four samples, Samples E and G were subsequently annealed using a carbon cap. The carbon encapsulation technique was described in Section 3.4.1. All these samples were annealed in an Ar atmosphere with the capped face down in a carbon pill box at 1650 ^{0}C for 30 min. The carbon was removed by RIE technique which was described in Section 3.5. All samples were RCA cleaned and sent for AFM analysis. Figs. 32-35 show the AFM

Sample Number	Dopants (ions/cm^3)	Activation Anneal	Av RMS before oxidation (nm)	Oxidation conditions	Av RMS after oxidation (nm)/oxide etch (nm)
A	-	-	0.40	3 hr at 1050 ^{0}C with 2 hr NO passivation at 1175 ^{0}C	0.345/0.756
B	-	-	0.35	3 hr at 1050 ^{0}C without NO passivation	0.32/0.256
C	N: 6E+19	1550 ^{0}C in Ar for 30 min	2.72	3 hr at1050 ^{0}C with 2 hr NO passivation at 1175 ^{0}C	2.63/2.779
D	Al:8E+15	1650 ^{0}C in Ar for 30 min	4.77	3 hr at1050 ^{0}C with 2 hr NO passivation at 1175 ^{0}C	3.55/4.002

Table 3: Average RMS roughness values of samples A to D with various implantation doses and activation annealing conditions

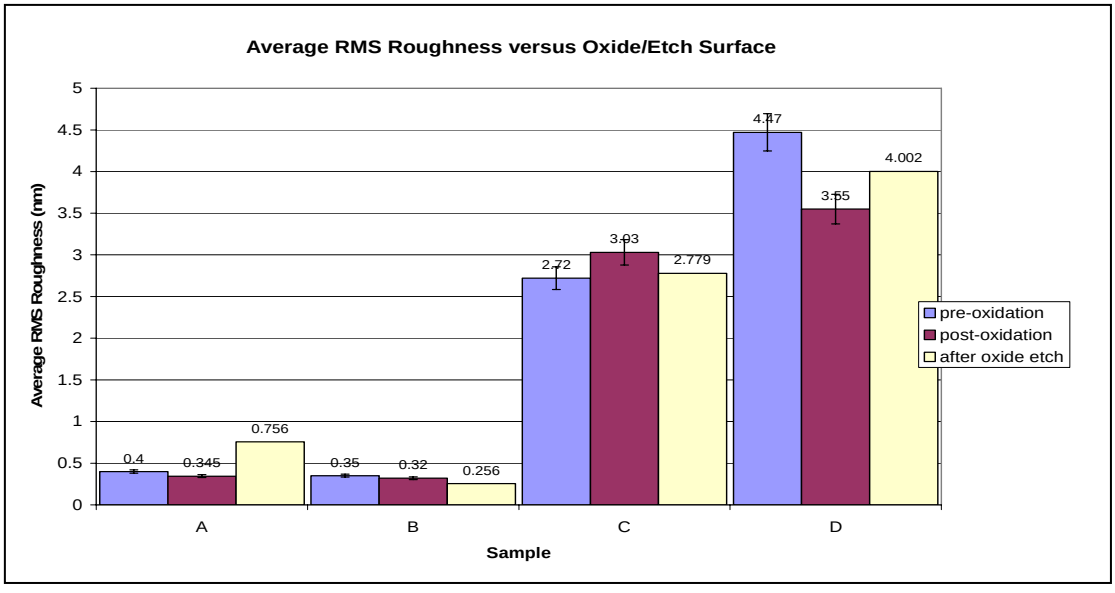

Figure 31: Average roughness values of virgin, Al and N doped samples before and after oxidation

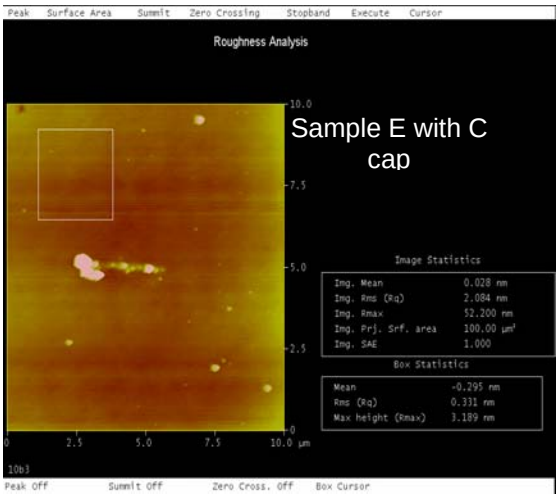

Figure 41: AFM image of Al doped (5E17 ions/cm^3) and annealed with carbon cap (Sample E)

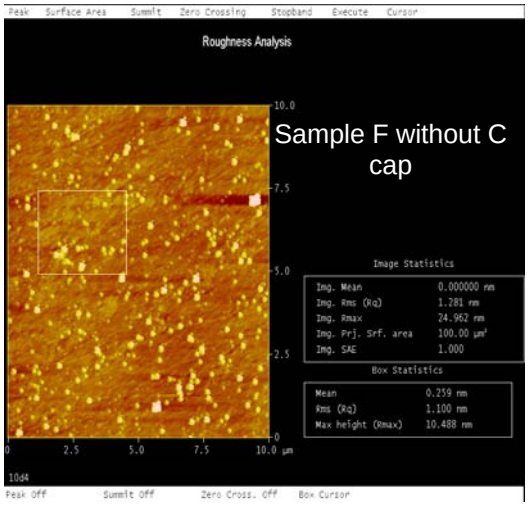

Figure 42: AFM image of of Al doped (5E17 ions/cm^3) and annealed without carbon cap (Sample F)

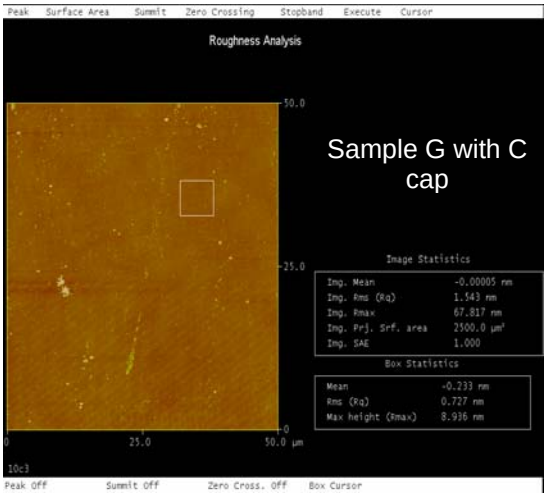

Figure 43: AFM image of Al doped (6E19 ions/cm^3)and annealed with carbon cap (Sample G)

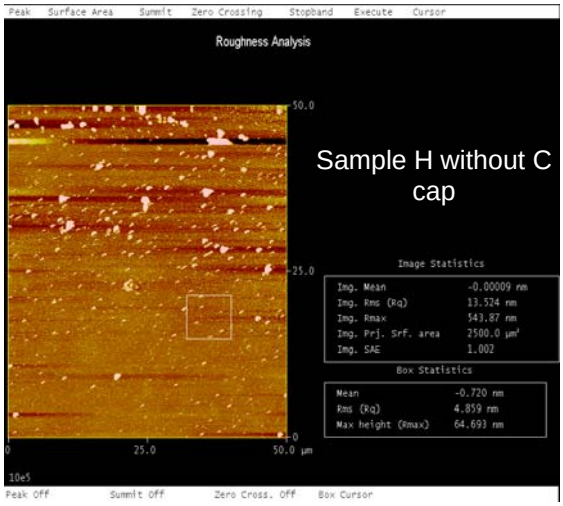

Figure 44: AFM image of Al doped (6E19 ions/cm^3) and annealed without carbon cap (Sample H)

Sample Number	Dopants (ions/cm3)	Activation Anneal	Av RMS (nm)
E	Al:5E17	1650 ^{0}C in Ar for 30 min with cap	0.33 (10 μm scan)
F	Al:5E17	1650 ^{0}C in Ar for 30 min without cap	1.29 (10 μm scan)
G	Al: 6E+19	1650 ^{0}C in Ar for 30 min with cap	0.72 (50 μm scan)
H	Al:6E19	1650 ^{0}C in Ar for 30 min without cap	4.77 (50 μm scan)

Table 4: Average RMS roughness values of Al doped samples with and without carbon cap

images of the above samples. The average RMS values for the implanted and activation annealed samples with and without carbon caps are shown in the Table 4. The AFM scan sizes varied from 5 μm to 125 μm.

The average RMS values were observed to be dependent on the scan dimensions. Fig. 36 shows the variation of the average RMS roughness values of C-face 4H-SiC samples as a function of scan size and capping conditions. The larger the scan size, the higher the observed RMS roughness value. This could be due to the nanometer sized carbon particles left over on the 4H-SiC surface after the carbon cap stripping. Fig. 37 shows the comparison of average RMS values of virgin C-face 4H-SiC samples annealed with and without a carbon cap in Ar at 1650 ^{0}C for 30 min. RBS experiments were performed at Vanderbilt University to investigate the surface morphology of the C-face 4H-SiC samples with and without the carbon cap. Results are shown in Fig. 38. These peaks near the channel numbers 200 and 300 represent respectively, the carbon and silicon content on the sample surface. The number of surface carbon atoms per unit area is much higher for the sample without a carbon cap compared to the sample with a carbon cap. This can be attributed to the clustering of carbon atoms during the high temperature annealing process. The sublimation of silicon atoms from the surface is significantly larger for the uncapped sample. This resulted in the formation of dangling carbon bonds which clustered together to form a graphitic layer. The carbon cap protects the sample surface from sublimation, thereby decreasing the unbound carbon content. Therefore, the carbon cap can be effectively used for protecting the surface during high temperature activation annealing.

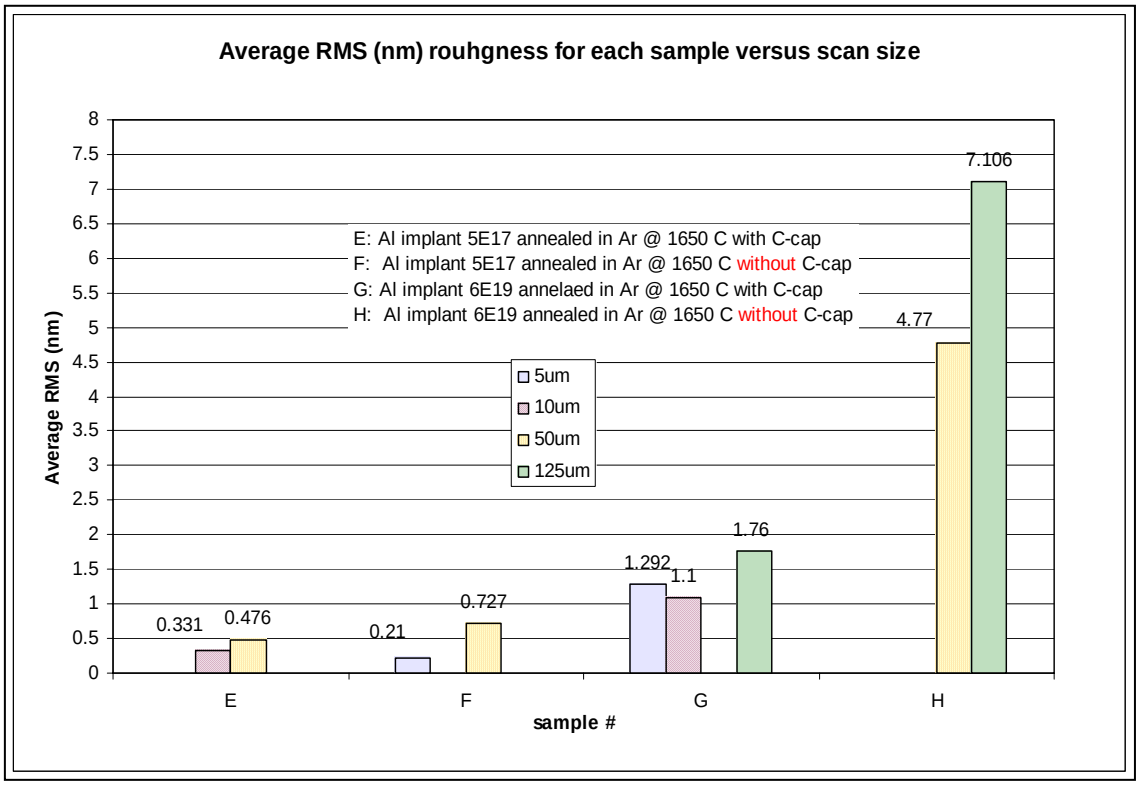

Figure 36: Variation of average RMS roughness with scan sizes

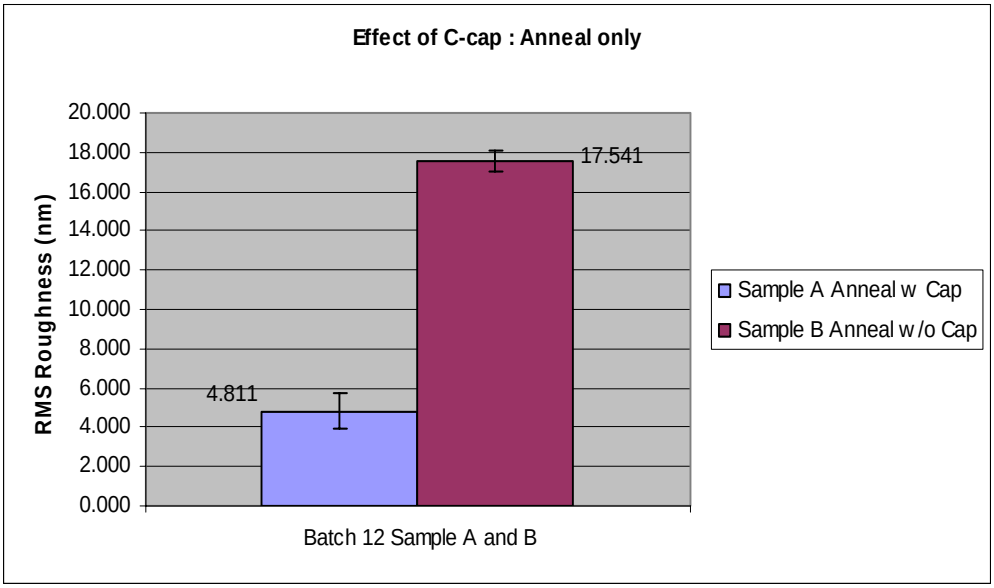

Figure 37: Average RMS roughness 4H-SiC surface annealed with and without carbon cap

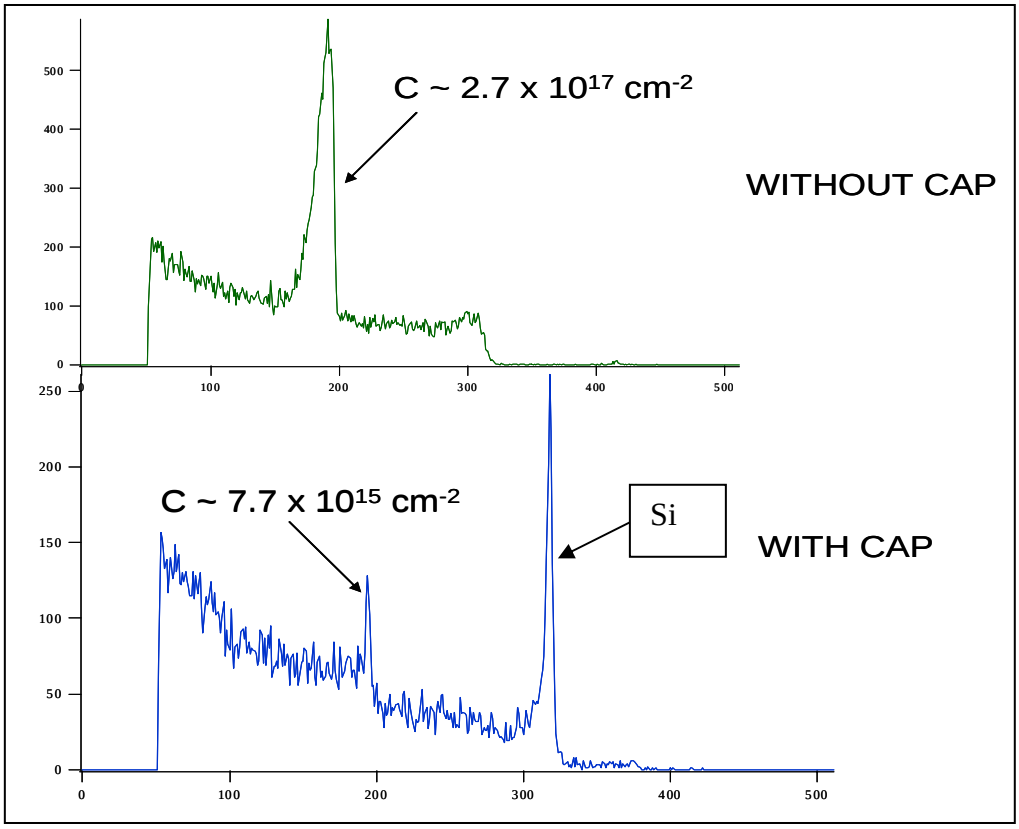

Figure 38: RBS plots of samples with and without carbon cap

4.2.1 Comparison of Virgin Si-face and C-face Surface

Fig. 39 shows AFM images of Si-face and C-face 4H-SiC samples. The average of the RMS roughness values measured at different locations on the each sample is plotted in Fig. 40. The average RMS value is 37% higher for C-face. This can be attributed to difference in the way that epitaxial layers grow on the two surfaces. The average RMS roughness value of 0.4 nm was taken as the standard for the comparison with all the AFM results obtained.

4.3 Electrical Reliability Measurements

Capacitance-voltage (C-V) and current-voltage (I-V) measurements were performed on MOS capacitors as described in Sections 3.10.1 and 3.10.2. Results are presented in the following sections.

4.3.1 CV Measurements

MOS capacitors of 350 μm dot size were fabricated on samples A and B which were described in Section 4.1. Sample A was passivated in nitric oxide (NO) for 2 hr at 1175 ^{0}C following oxidation for 3hr at 1050 ^{0}C, and sample B was oxidized without NO passivation. Figs. 41 and 42 show the capacitance as a function of applied gate voltage and density of interfacial traps (number of defects/eV.cm^2) as a function of trap energy for capacitors on each sample. The density of interfacial traps (D_{it}) was calculated by the software using the quasi static capacitance and high frequency capacitance (100 KHz). It can be seen that the D_{it} for the sample B which was oxidized without NO anneal is approximately two orders of magnitude higher compared to sample A which was annealed in NO after oxidation. This high value of D_{it} decreases the mobility of carriers in the channel, thereby increasing the overall ON resistance (R_{ON}) for a MOSFET. The

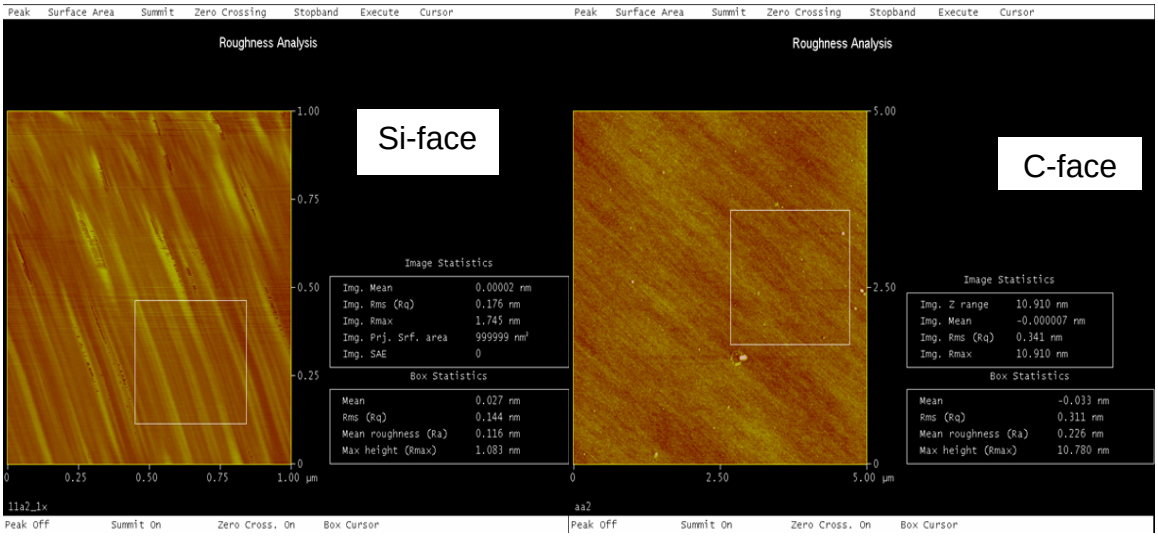

Figure 39: AFM images for as-received Si-face and C-face 4H-SiC samples

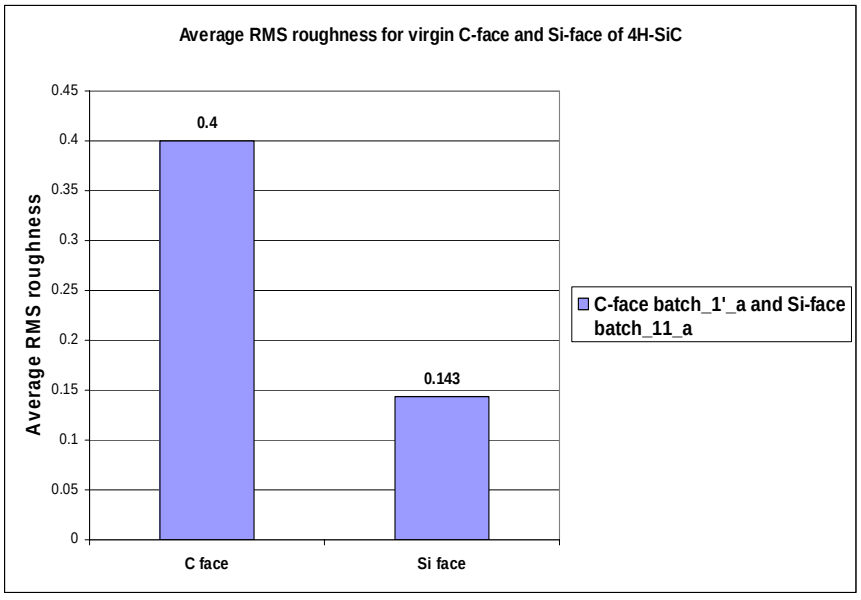

Figure 40: Comparison of average RMS roughness values of Si-face and C-face 4H-SiC

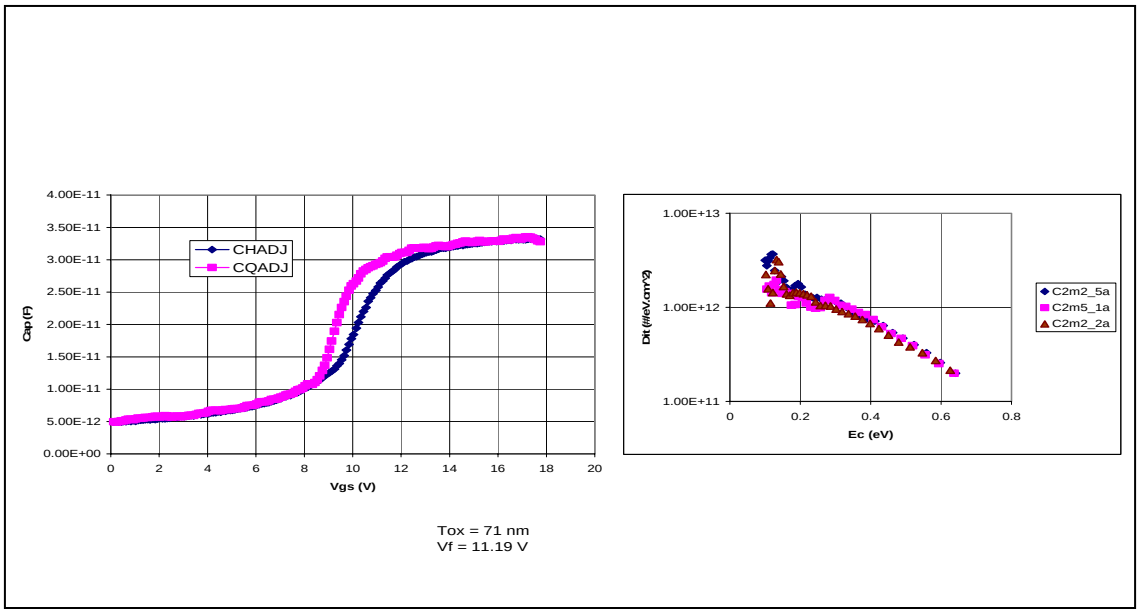

Figure 41: CV and D_{it} plots for MOS capacitor with no implants passivated in NO after oxidation

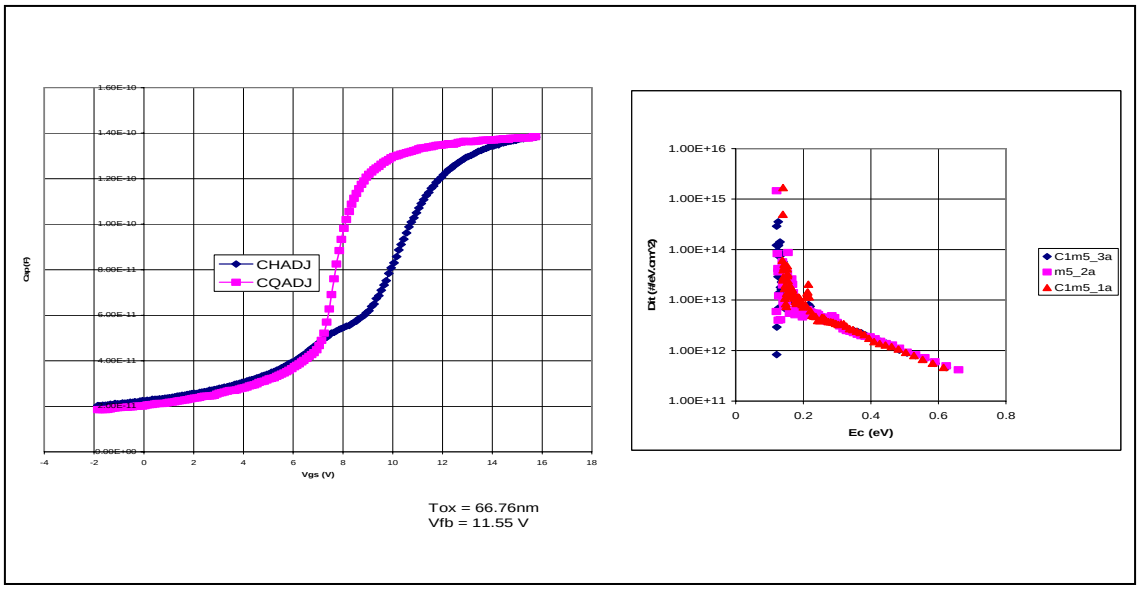

Figure 42: CV and D_{it} plots for MOS capacitor with no implants and without passivation after oxidation

passivation effect of NO on the interfacial defects is not understood completely. However, some authors have reported that the decrease in D_{it} after the NO passivation could be due to the bonding of nitrogen atoms from NO molecules with the dangling bonds of Si and C atoms produced during the oxidation process.

4.3.2 Reliability Test Results

The samples 'A to C' as described in Sections 4.1 and 4.1.1 were tested for dielectric (silicon dioxide) breakdown. The procedure for testing was described in the Section 3.10.1. Due to unavailability of *p*-type substrates for C face 4H-SiC IV, tests were not performed on the Al implanted samples 'D to H'. The dielectric breakdown field for all the samples was calculated by using the equation

$$E_B = \frac{V_G - \phi_{MS}}{t_{ox}} \qquad \textbf{Eq 10}$$

where,

E_B = dielectric breakdown field (MV/cm)

V_G = applied gate voltage (V)

ϕ_{MS} = metal-semiconductor work function difference (eV)

t_{ox} = oxide thickness (nm)

The metal-semiconductor work function difference (ϕ_{MS}) is given by

$$\phi_{MS} = \phi_M - (\chi_S + \frac{E_g}{2} + \phi_B) \qquad \textbf{Eq 11}$$

where,

ϕ_M and χ_S are the work functions of the metal and the electron affinity of the semiconductor, respectively

E_g is the bandgap energy of 4H-SiC

ϕ_B is the barrier height defined as the difference between the Fermi level (E_f) of the doped substrate and intrinsic Fermi level (E_i)

ϕ_B for an *n*-type semiconductor is given by

$$\phi_B = E_f - E_i = \frac{kT}{q} \ln \left[\frac{N_D - N_A}{n_i} + \frac{n_i}{N_D - N_A} \right]_{n-type} \quad \textbf{Eq 12}$$

and for a *p*-type semiconductor

$$\phi_B = E_f - E_i = \frac{kT}{q} \ln \left[\frac{N_A - N_D}{n_i} - \frac{n_i}{N_A - N_D} \right]_{p-type} \quad \textbf{Eq 13}$$

where,

k is the Boltzmann's constant = 1.38 x 10^{-23} JK^{-1}

T is the room temperature for all experiments = 298 K

q is charge of the an electron = 1.6 x 10^{-19} C

N_D donor concentration (species/cm^3)

N_A acceptor concentration (species/cm^3)

n_i intrinsic charge carrier concentration (species/cm^3)

It is safe to assume that $N_D >> N_A$ and $N_A >> N_D$ for *n*-type and *p*-type semiconductors, respectively. The values of ϕ_B and the oxide thickness values for the un-implanted samples A and B were obtained by the CV measurements. The average values of ϕ_B and oxide thickness (t_{ox}) were 1.42 eV and 62.5 nm. The metal semiconductor work function (ϕ_{MS}) difference was calculated using Equation 11. Table 5 shows the values of ϕ_{MS} for various doping levels in C-face 4H-SiC.

Dopant	N_a (ions/cm^3)	N_d	kT/q	n_i (ions/cm^3)	ϕ_B (eV)	ϕ_S (eV)	ϕ_M (eV)	Eg/2 (eV)	ϕ_{MS} (eV)
Nitrogen	0	6.00E+19	0.025	5.00E-09	1.62	3.60	4.69	1.63	1.08
Al	8.00E+15	0	0.025	5.00E-09	1.39	3.60	4.69	1.63	0.85
Al	5.00E+17	0	0.025	5.00E-09	1.50	3.60	4.69	1.63	0.957
Al	6.00E+19	0	0.025	5.00E-09	1.62	3.60	4.69	1.63	1.08
No implant	0.00E+00	0	0.025	5.00E-09	1.42	3.60	4.69	1.63	8.80

Table 5: Work function values of 4H-SiC doped with nitrogen and aluminum

The breakdown electric field was calculated using Equation 10. Fig. 43 shows the plot of current density versus the dielectric breakdown field for the sample A. The electric field corresponding to the current density of 10^{-4} A/cm^2 was taken as the dielectric breakdown field. Capacitors tested with zero check showed lower gate leakage currents compared to the capacitors tested with no zero check, which is a process that corrects for stray leakage currents in I-V measurement systems. Hence, the reliability measurements on the rest of samples were performed with zero check. The average dielectric breakdown field strength of good capacitors on sample A is 9.5 MV/cm. Fig. 44 shows the plot of dielectric breakdown field versus current density for the Sample B. The average dielectric breakdown filed for the good capacitors on Sample B is 6.92 MV/cm. NO passivation improves breakdown performance.

4.3.1.1 I-V Results for Implanted and Activation Annealed Samples

Nitrogen with a concentration of 6 x 10^{19} atoms/cm^3 was implanted and activated in Ar for 30 min at 1550 ^{0}C. MOS capacitors were fabricated and tested and as described previously. Fig. 45 shows the plot of current density versus dielectric breakdown field for Sample C. The average dielectric breakdown field was observed to be approximately 6.03 MV/cm. The nitrogen implanted sample (C) showed considerable decrease in dielectric breakdown field compared to unimplanted Sample A. This could be attributed to the surface roughness caused by implantation and activation annealing.

4.3.1.2 IV Reliability Results for Aluminum Doped Samples

The C face 4H-SiC substrate obtained from Cree Inc., was *n*-type, and the Al implanted samples were only physically characterized for surface damage using AFM.

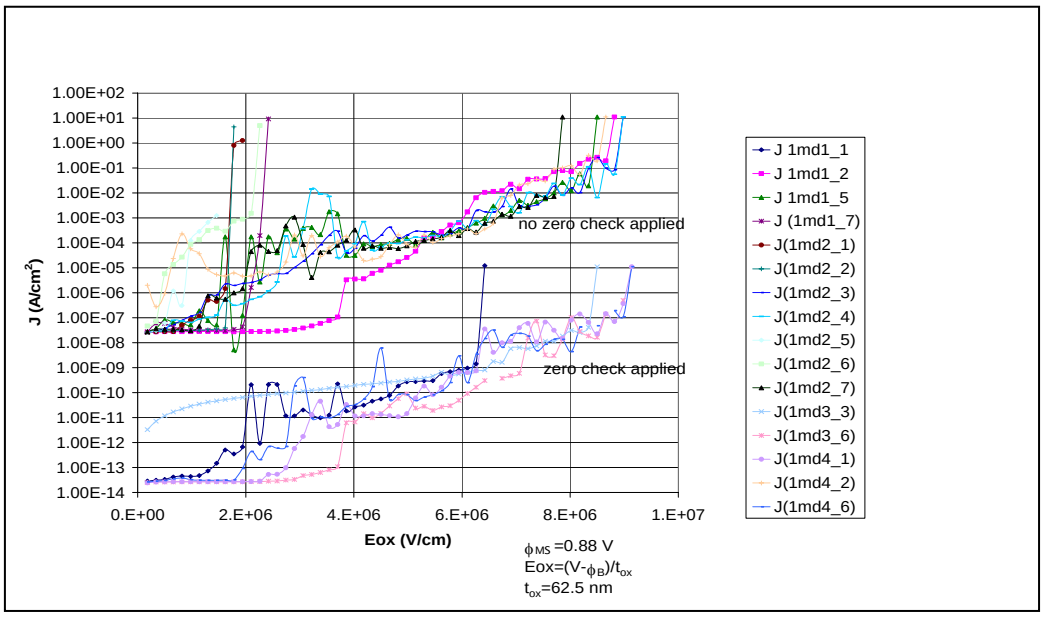

Figure 43: Current density versus dielectric breakdown field for unimplanted C face 4H-SiC MOS-C with NO passivation with 350 µm capacitor (Sample A)

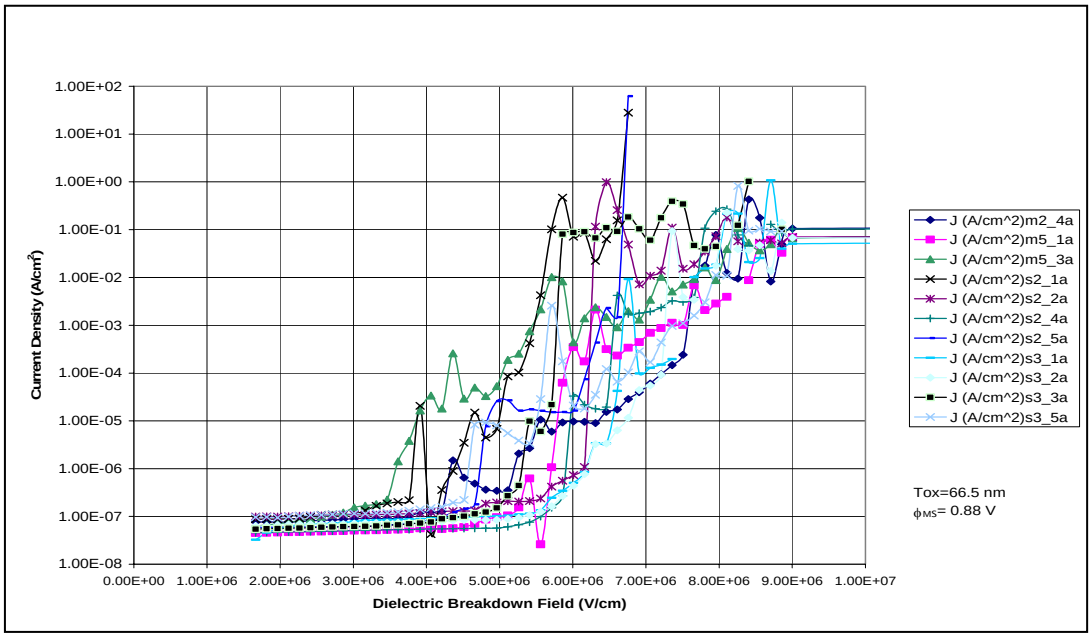

Figure 44: Current density versus dielectric breakdown field for unimplanted C face 4H-SiC without NO passivation with 350 µm capacitor

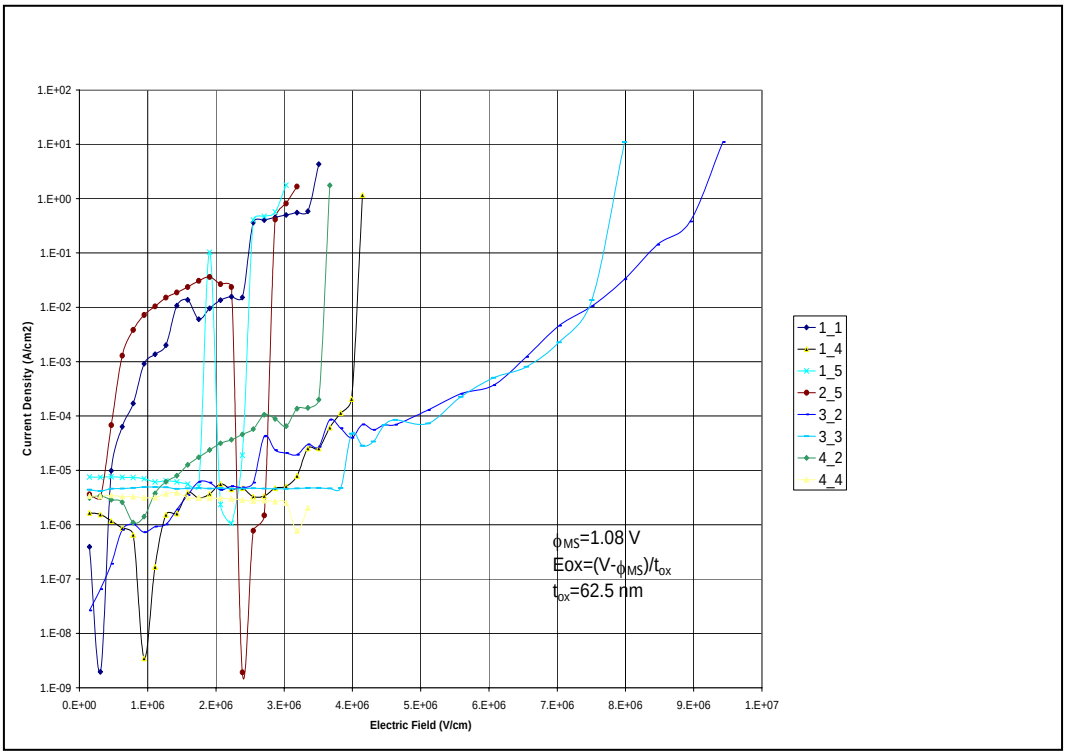

Figure 45: Current density versus dielectric breakdown field for nitrogen dope (6 x10^{19}/cm^{3}) C face 4H-SiC MOS-C with 350 μm capacitor (Sample C)

I-V reliability tests were not performed. Only the average RMS surface roughness values were used for comparison of the surface damage caused by ion-implantation.

4.4 Correlation of Dielectric Breakdown Field Strength and Surface Roughness

Table 6 shows the comparison of average RMS roughness values with dielectric breakdown filed strength for samples ‘A to D’. The average RMS roughness values are higher for samples implanted with nitrogen and aluminum. The dielectric breakdown field strength decreased with increased roughness. In the Table 6, the RMS roughness value for the Sample D is shown for comparison. Table 7 shows only the average RMS roughness values aluminum implanted samples with and without carbon cap. The same trend of increase in surface roughness with increase in implant concentration can be observed.

Sample Number	Dopants (ions/cm^3)	Activation Anneal	Av RMS after oxidation (nm)/oxide etch (nm)	Av Dielectric Breakdown Field (MV/cm)
A	-	-	0.345/0.756	9.51
B	-	-	0.32/0.256	6.92
C	N: 6E+19	1550 ^{0}C in Ar for 30 min	2.63/2.779	6.03
D	Al:8E+15	1650 ^{0}C in Ar for 30 min	3.55/4.002	-

Table 6: Average RMS roughness and dielectric breakdown field strength values for Sample A, B, C and D. Sample A (no implant) was NO passivated after oxidation and Sample B (no implant) was tested without NO passivation.

Sample Number	Dopants (ions/cm3)	Av RMS (nm)
E (with carbon cap)	Al:5E17	0.33 (10 μm scan)
F(without carbon cap)	Al:5E17	1.29 (10 μm scan)
G(with carbon cap)	Al: 6E+19	0.72 (50 μm scan)
H(without carbon cap)	Al:6E19	4.77 (50 μm scan)

Table 7: Average RMS roughness and dielectric breakdown field strength value

5. CONCLUSIONS

- AFM analysis on as received C face 4H-SiC samples showed higher surface roughness compared to as received Si face 4H-SiC samples.
- MOS capacitors fabricated on *n*-type C-face 4H-SiC epi-layers failed at an average electric field of 9.51 MV/cm, which is comparable to *n*-type Si-face 4H-SiC samples.
- The oxidation rate of C-face 4H-SiC samples was observed to be higher than that of Si-face 4H-SiC.
- The average RMS roughness values of C face 4H-SiC samples increased with increasing implantation doping concentration and activation annealing temperature.
- Current-voltage (C-V) reliability measurements performed on different samples with varying surface roughness showed a decrease in dielectric breakdown field strength with increasing surface roughness.
- Carbon encapsulation protected the sample surface from damage during activation annealing.
- Samples protected with carbon caps failed at a higher electric field compared to samples without carbon caps.
- Removal of carbon by RIE does not always lead to a planar surface. Residual carbon on the surface increases the overall surface roughness.

6. FUTURE WORK

- The carbon encapsulation technique is a local planarization process. An alternative process such as chemical-mechanical planarization (CMP) can be studied for global planarization.
- The higher oxidation rate of C-face 4H-SiC can be used as an advantage in decreasing the overall fabrication process time for power device fabrication. However, additional work must be undertaken to further reduce the interface trap density for C-face. Near the 4H-SiC conduction band edge, this trap density is currently 3 to 5 times higher for the C face compared to Si face.

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