RF Reconfigurable Filter

by

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Abstract

As the rapidly progressing RFIC (Radio Frequency Integrated Circuit) technology, the requirement for wireless receive is more complicated and stringent. Therefore, a programmable band selection front end meets the current requirement for different band wireless communication. For most of the conventional frontend design, they can only handle single band signal with high NF (Noise Figure) and low gain through the entire receiver chain. Furthermore, they also need SAW (Surface-Acoustic-Wave) filter at the input port for rejecting the out-of-band signal which may cause higher insertion loss leading to worse performance since the signal at the input is sensitive.

In this paper, a fully differential noise-cancelling LNA (Low Noise Amplifier) with out-of-band rejection notch filter combined with a programmable gain-boost N-path bandpass filter is proposed. The wide-band noise-cancelling LNA is at the first stage for the noise dominant and input matching while the notch filter is rejecting the out-of-band signal, followed by gain-boost N-path bandpass filter for further gain improvement and frequency selection. The center frequency is determined by the switching frequency of the N-path filter, while the RC-time constant defines the bandwidth. Mostly the high-Q filter can be achieved by the frequency selection.

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I am also grateful to my parents. They always respect my decision and support me. Without their support, I will never get a chance to step into America and study at Auburn University and met many friends here. They encouraged and guided me whenever I was in depressed.

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List of Abbreviations

CML	Current Mode Logic
VCO	Voltage Control Oscillator
FoM	Figure of Merit
LNA	Low Noise Amplifier
NF	Noise Figure
IIP3	Input Third-order Intercept Point
SAW	Surface-Acoustic Wave
LPTV	Linear Periodically Time-variant
LTI	Linear Time Variant

Chapter 1

Introduction

1.1 Motivations

Nowadays, with the rapidly increasing requirement for the RF receiver, the wireless frontend needs to support different band frequency. As the first stage of the whole RF frontend chain, MIMO (Multiple Input and Multiple Output) LNA may be required to meet the different network frequency. However, multiple SAW filter and additional switches may need to be put in the input of receiver for selecting the different band which may cause higher noise and insertion loss.

In the past, a conventional alternatively narrowband LNA must be able to be tuned to the wanted frequency, and the external preselection SAW filter was added. However, that way is unable to meet the requirement of modern portable devices. In recent years, a new noise-cancelling LNA was proposed and have been widely used in many systems for its low noise, wide band matching, and high gain as well as linearity. The tunable high-quality factor N-path bandpass filter is also a popular topic theses years. The off-chip passive filter is already can be replaced by the on-chip inductor-less filter.

Nowadays, multi-band is able to be supported by the most of the phones. GSM networks, CDMA, WiFi are all using different frequency band which may have interference with each other. Therefore, narrow band selection and out-of-band rejection seems important in modern cell phone technology. In this work, a fully-differential noise canceling LNA with notch filter for the out-of-band rejection followed by gain-boost N-path band pass filter are designed. The noise canceling LNA is in the first stage for the low noise domain and wide-band input matching while the notch filter can reject the out-of-band frequency signal to reduce the interference. The

programmable band selection filter is followed by the LNA for the extra gain and narrow band frequency selection. The filter is clocked by 25% duty cycle ring oscillator using Miller capacitor canceling technology. The Miller capacitor canceling structure can help improve the phase noise of the ring oscillator and inject lower noise to the second stage amplifier.

1.2 Thesis Organization

This thesis is organized to present low noise amplifier with notch filter and gain-boost N-path filter with the clock theory. Chapter 2 analyzed the structure of fully differential LNA with notch filter including noise figure, input matching, linearity and the Q-enhanced cross couple structure. Chapter 3 analyzed the gain-boost N-path filter including the comparison between the conventional N-path filter and proposed gain-boost N-path filter. LPTV, bandwidth will also be discussed in chapter 3. The clock used for N-path filter is ring oscillator using CML cell with Miller capacitor cancellation structure which improves phase noise and increases FoM. Simulation and Measurement result will be provided in each chapter.

Chapter 2 Low Noise Amplifier Design

2.1 Introduction of Previous Work on LNA

LNA is the first stage in the RF receivers. It followed by the antenna and plays a significant role in the entire performance. The noise comes from the LNA will add to the overall receiver directly. Recently, as the smaller size transistor technology shows up, the whole RX noise figure lower than 6 dB can be achieved. Thus, for the LNA, it is required to contribute only 2 to 3 dB noise figure.

In modern CMOS technology, the common source (CS) amplifier and common-gate (CG) amplifier are widely used as LNA while the common-drain (CD) amplifier is usually used as a buffer or in level shifters. For the CS amplifier, it is always with inductive degeneration for the input impedance match. CS amplifier has better noise performance, and its input real part can be matched by the degeneration inductor and C_{gs} of the transistor. But it will be limited by the wide band application. At the same time, the low input impedance of the CG amplifier is attractive for the wide band application. When the channel length modulation and body effect are neglected, the input impedance will be $1/g_m$ which means we only need to make the g_m of CG transistor equal to 20ms, then the input impedance can be matched to 50Ω. However, when the input impedance is perfectly matched, the NF is still reaching above 3 dB. For the CD amplifier which also called as a source follower, it has high input impedance and low output impedance. The input signal is coming from the gate of the transistor while the output is taken from the source of the transistor. Thus the output voltage will follow the input voltage since the output voltage is directly equal to input voltage minus constant overdrive and threshold voltage.

2.2 A Differential Noise-Cancelling LNA with Notch Filter

2.2.1 Introduction of Noise Cancelling LNA

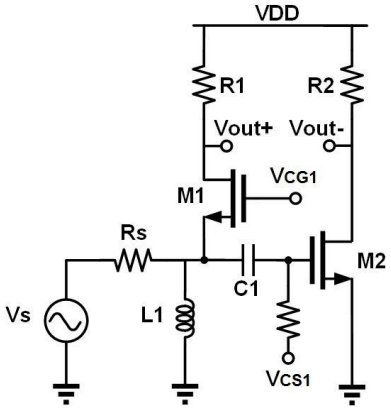


Fig. 2.1. Noise-Cancelling LNA

As Fig. 2.1 shows are the core structure of balun noise canceling LNA where the CG transistor (M1) and CS transistor (M2) are in parallel [1]. Because the gate of the ideal transistor has infinite impedance and the output resistor of transistor can be assumed as infinite also, the input impedance of this LNA is $R_{in} = 1/g_{m1}$. And the gain of CG and CS stage are $\mathrm{A}_{v1} = g_{m1} \cdot R_1$ and $\mathrm{A}_{v2} = g_{m2} \cdot R_2$. To acheve balun requirement of this LNA, the total gain of this LNA can be written as:

$$\mathrm{A}_{v1} = -\mathrm{A}_{v2} = \frac{R_1}{R_s} \tag{2.1}$$

$$\mathrm{A}_v = \frac{V_{out+} - V_{out-}}{V_{in}} = g_{m1} \cdot R_1 + g_{m2} \cdot R_2 \tag{2.2}$$

Fig. 2.2. depicts the noise current source $\boldsymbol{i_n}$ comes from CG transistor which will generate a voltage at input node and an anti-phase voltage at the output node [1]. If the gain of CG and CS stage meet equation (2.1), then the voltage generated by noise current will be equal at the output node. Thus, the noise at CG output node will be cancelled, and the output signal balance can be achieved.

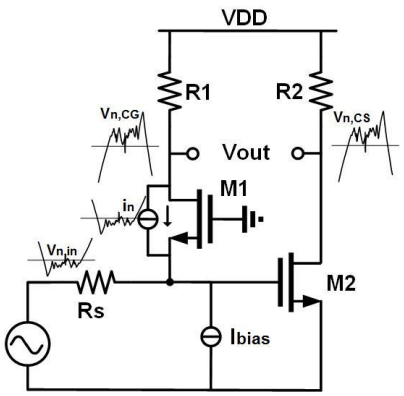


Fig. 2.2. Noise-Cancellation Analysis

Furthermore, this structure can cancel the distortion also, and it is similar to noise cancellation. The nonlinear current of CG transistor $\boldsymbol{i_{ds}}$ is caused by input voltage $\boldsymbol{v_s}$, and be converted to nonlinear voltage $\boldsymbol{v_{in}}$ through linear source resistor $\boldsymbol{R_s}$. The nonlinear voltage $\boldsymbol{v_{in}}$ can be depicted as:

$$\boldsymbol{v_{in} = \alpha_1 v_s + \alpha_2 {v_s}^2 + \alpha_3 {v_s}^3} \tag{2.3}$$

where $\boldsymbol{\alpha}$ is Taylor coefficient and $\boldsymbol{\alpha_1}$ is the first Taylor coefficient which can be defined as:

$$\boldsymbol{\alpha_1 = \frac{1/g_{m1}}{1/g_{m1} + R_s}} \tag{2.4}$$

where $\boldsymbol{1/g_{m1}}$ is the input impedance of CG transistor. Based on equation (2.1) and (2.3), the output voltage of CS and CG stage can be written as:

$$\boldsymbol{v_{out,CS} = -v_{in} \cdot \frac{R_1}{R_s} = -(\alpha_1 v_s + \alpha_2 {v_s}^2 + \alpha_3 {v_s}^3) \cdot \frac{R_1}{R_s}} \tag{2.5}$$

$$\boldsymbol{v_{out,CG} = i_{in} \cdot R_1 = [(1 - \alpha_1) \cdot v_s - \alpha_2 {v_s}^2 - \alpha_3 {v_s}^3] \cdot \frac{R_1}{R_s}} \tag{2.6}$$

Thus, the signal at the output node will be:

$$\boldsymbol{v_{out} = v_{out,CG} - v_{out,CS} = v_s \cdot \frac{R_1}{R_s}} \tag{2.7}$$

From equation (2.7), the nonlinear part in (2.5) and (2.6) will be canceled in the output node.

Therefore, the noise canceling LNA structure can cancel the noise and nonlinear distortion generated by CG transistor. Moreover, the CS transistor will dominate the total noise and linearity in this LNA. The linearity and noise will be further analyzed in next few sections.

2.2.2 Analysis of Differential Noise-Cancelling LNA

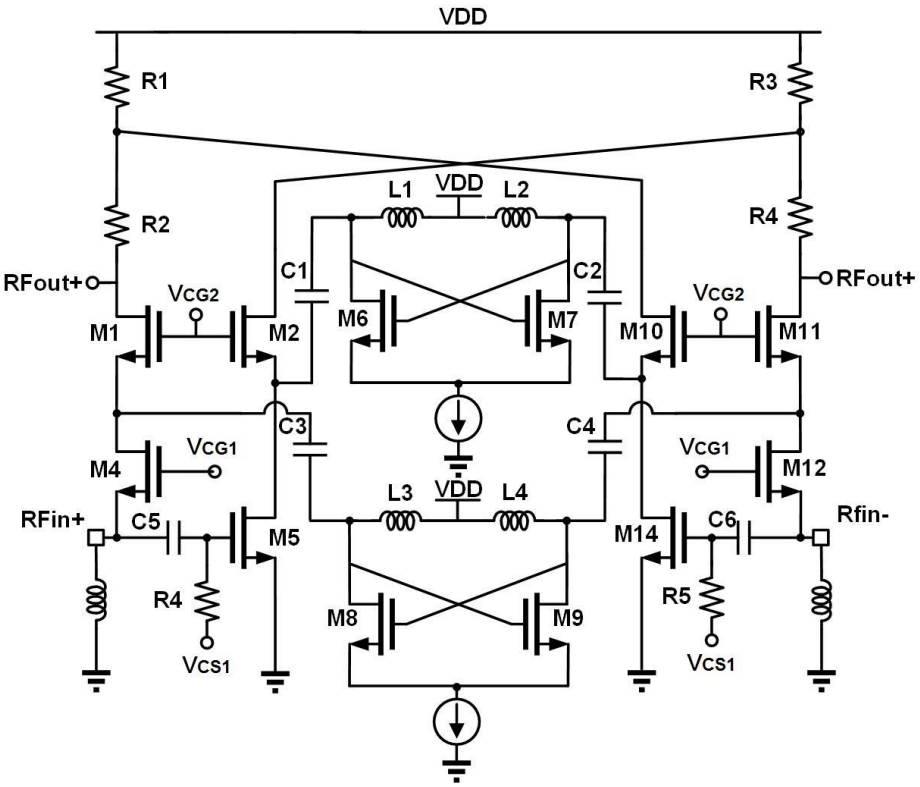


Fig. 2.3. Differential Noise-Cancelling LNA with Notch Filter

As Fig. 2.3 depicts the fully differential noise canceling LNA. Different from the single-end balun noise canceling LNA, the differential input LNA needs to sense four output signals instead of two. However, with structure Fig. 2.3, it can meet the requirement of only two outputs.

Fig. 2.4 simplifies the CG branch of differential noise canceling LNA for further analyze [2]. The cascade transistor M1 is added to improve the reverse isolation and an approach to lower the input impedance. Thus, the impedance looking into the drain of M1 can be written as:

$$\boldsymbol{R_x = \frac{R_1 + R_2 + r_{o1}}{1 + g_{m1} r_{o1}}} \tag{2.8}$$

where r_{o1} is the output impedance of M1.

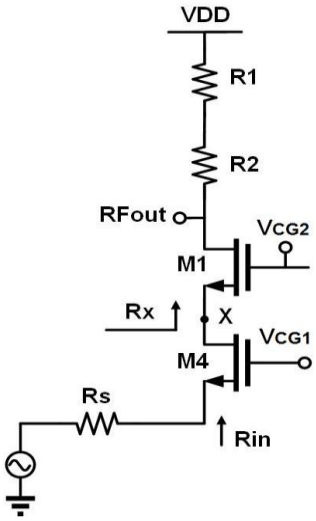


Fig. 2.4. Simplified CG branch for analysis

Furthermore, the input impedance of the CG branch can be depicted as:

$$R_{in} = \frac{R_x + r_{o4}}{1 + g_{m4} r_{o4}} \approx \frac{1}{g_{m4}} + \frac{R_1 + R_2}{g_{m4} \cdot r_{o4} \cdot g_{m1} \cdot r_{o1}} + \frac{1}{g_{m4} \cdot r_{o4} \cdot g_{m1}} \tag{2.9}$$

where r_{o4} is the output impedance of M4. Assuming r_{o1} and r_{o4} are infinite in an ideal transistor, we have $g_m \cdot r_o \gg 1$ which the input impedance will become: $R_{in} \approx 1/g_{m4}$.

For the noise analyze for Fig. 2.3, assuming the output of each transistor is infinite, and the bias current for both CG and CS are an ideal source which would not inject extra noise. Since the noise due to CG stage will be fully canceled at the output node, $g_{m4} = N \cdot g_{m5}$, $R_1 = R_3 = R/N$ and $R_2 = R_4 = (N-1) \cdot R/N$ will be chosen. Therefore, the noise figure of this LNA will be given as:

$$\begin{aligned} F &= 1 + \frac{r_{g5}}{Rs} + \frac{\gamma}{g_{m5} \cdot Rs} + \frac{Rs}{R1 + R2} + \frac{1}{g_{m5} \cdot (R1 + R2)} \\ &= 1 + \frac{r_{g5}}{Rs} + \frac{\gamma}{g_{m5} \cdot Rs} + \frac{Rs}{R} + \frac{1}{g_{m5} \cdot R} \end{aligned} \tag{2.10}$$

where r_{g5} is the gate resistor of the CS transistor. The dominate noise here are the thermal noise generated by transistors and the load resistors. But the noise factor will be lower if the gain is higher and the gate resistor can be lower if the layout is done properly.

2.2.3 Non-Linearity Analysis

If there are two large signals at $\boldsymbol{\omega 1}$ and $\boldsymbol{\omega 2}$ applied to the nonlinear system, then these signals can generate unwanted thrid-order intermodulation which called IM3. This phenomenon will increase when two frequency components as their power are large enough. As LNA is the first stage of the whole RF chain, its input third intercept point (IIP3) must be large enough to withstand intermodulation effects [3].

Assuming there are two closely frequency signals $\boldsymbol{\omega 1}$ and $\boldsymbol{\omega 2}$ at the LNA input which means:

$$\boldsymbol{x(t) = A_1 cos\omega_1 t + A_2 cos\omega_2 t} \qquad (\mathbf{2.11})$$

where $\boldsymbol{A_1}$ and $\boldsymbol{A_2}$ are the amplitute of two signals. Then we will have:

$$\boldsymbol{y(t) = \alpha_1(A_1 cos\omega_1 t + A_2 cos\omega_2) + \alpha_2(A_1 cos\omega_1 t + A_2 cos\omega_2)^2}$$
$$\boldsymbol{+\alpha_3(A_1 cos\omega_1 t + A_2 cos\omega_2)^3} \qquad (\mathbf{2.12})$$

where α_1 can be defined as the small signal gain. To further derive (2.12), we can have the following intermodulation products:

$$\omega = (\alpha_1 A_1 + \frac{3}{4}\alpha_3 {A_1}^3 + \frac{3}{2}\alpha_3 A_1 {A_2}^2) \cdot cos\omega_1 t$$
$$+\left(\alpha_1 A_2 + \frac{3}{4}\alpha_3 {A_2}^3 + \frac{3}{2}\alpha_3 A_2 {A_1}^2\right) \cdot cos\omega_2 t \qquad (2.13)$$

where the IM3 products are generated at ω_1 and ω_2. Assuming i_{IM3+} and i_{IM3-} represents nonlinear a current source of two input branches of the LNA. Then we have order three input voltage as:

$$v_{in,IM3} = \frac{R_s i_{IM3}}{2} \tag{2.14}$$

thus, the IM3 product generated by CG transistor at output voltage can be expressed as:

$$v_{out,CG,IM3} = -\frac{R \cdot i_{IM3,CG}}{2} \tag{2.15}$$

moreover, the IM3 product generated by CS transistor at output voltage can be expressed as:

$$v_{out,CS,IM3} = -\frac{R}{N}\left(i_{IM3,CS} - \frac{g_{m5} R_s \cdot i_{IM3,CG}}{2}\right) \tag{2.16}$$

based on $g_{m4} = N \cdot g_{m5}$, $R_1 = R_3 = R/N$ and $R_2 = R_4 = (N-1) \cdot R/N$, we have:

$$v_{out,IM3} = 2 \cdot R(-\frac{i_{IM3,CS}}{N} + \frac{i_{IM3,CG}}{2}\left(\frac{g_{m5} R_s}{N} - 1\right) \tag{2.17}$$

which is the IM3 product at the differential output. As described in section in 2.2, the distortion due to the CG transistor can be canceled. Thus, the dominant nonlinear device is the CS device, and it can be written as:

$$v_{out,IM3} = \frac{\mu C_{ox} R}{4(1+\theta V_{dsat})}(\frac{W}{L})_5 \cdot \left(\frac{1}{V_{dsat} \cdot (2+\theta V_{dsat})\left(1+\frac{3sC_{in}R_s}{4}\right)} - 3\theta\right) v_{in}^3 \tag{2.18}$$

where V_{dsat} is the overdrive voltage of CS transistor and $C_{in} = C_{gs,CS} + C_{gs,CG}$. Based on (2.18), the IIP3 product can be calculated at differential output as:

$$v_{IIP3} = \frac{4\sqrt{2} V_{dsat}(1+V_{dsat})(2+\theta V_{dsat})\sqrt{|1+3sC_{in}R_s|/4}}{\sqrt{\left|1-3\theta V_{dsat}(2+\theta V_{dsat})(1+\frac{3sC_{in}R_s}{4})\right|}} \tag{2.19}$$

From (2.19), there are two dominant terms which are the IM3 product generated by

second-order nonlinearity and the third-order nonlinearity of CS transistor from the fundamental component in the small input signal.

2.2.4 Notch Filter with Q-Enhanced Cross-Coupled Pair

From Fig. 2.3., there is an LC notch filter. However, the notch filter always suffers from poor selectivity due to the low Q factor of the inductor and the lossy tank. Furthermore, intermodulation, harmonics even image signal will also affect the performance of notch filter. Therefore, as depicts in Fig. 2.5, the Q-enhancement structure is proposed to add to the notch filter to improve the selectivity of the filter [4].

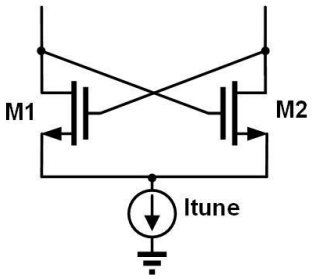


Fig. 2.5. Implementation of $-g_m$ cell using cross-coupled transistors

The LC circuit applied to the drain of M1 and M2 will resonate at $1/(2\pi\sqrt{fc})$ and have low impedance to the cross-coupled transistors at resonate frequency. However, the loss caused by notch filter will largely affects the frequency selectivity. Thus, the $-g_m$ cell is added to provide compensation the loss and increase the Q factor of the notch filter. In this structure, I_{tune} is used to control the negative trans conductance of transistor. Since the notch filter is added in between the first and second stage, and the signal is already amplified by the first stage, the noise contribution comes from the notch filter is fairly low.

2.3 Simulation Result

As Fig. 2.3 shows, the circuit is simulated in Cadence tool using S-parameter simulation. The S-parameter result is as Fig. 2.6:

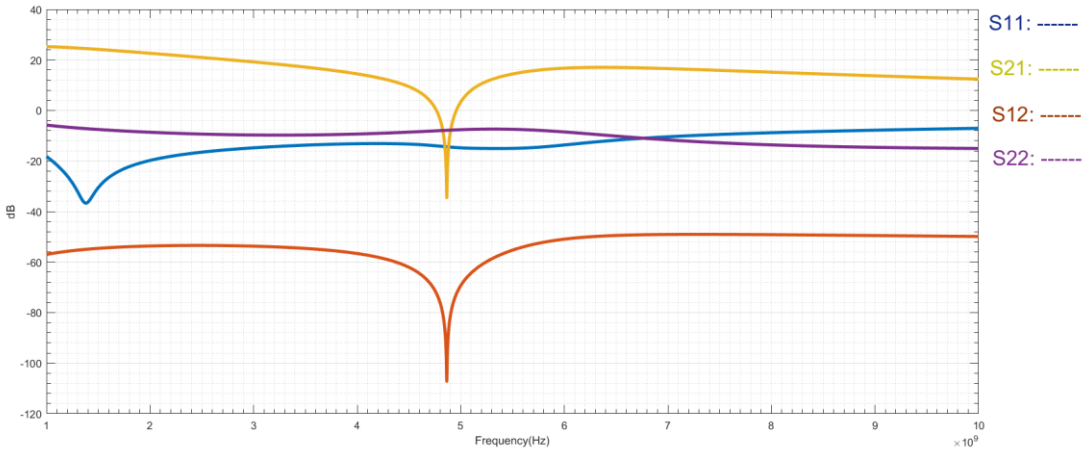


Fig. 2.6. S-parameter simulation result

The simulation is from 1GHz to 10GHz giving 1.8V supply voltage. From Fig. 2.6, it is, of course, that S11 is below -10 dB from 1GHz to around 7GHz which proves the wide band matching due to the noise-cancelling structure. The gain achieves 20 dB except for the frequency at around 4.8GHz. The notch filter provides about 58 dB rejection ratio. Reverse isolation is well below -50 dB due to the second stage CG transistor which enhances reverse isolation. Total power consumption is 36mW at the 1.8V supply voltage.

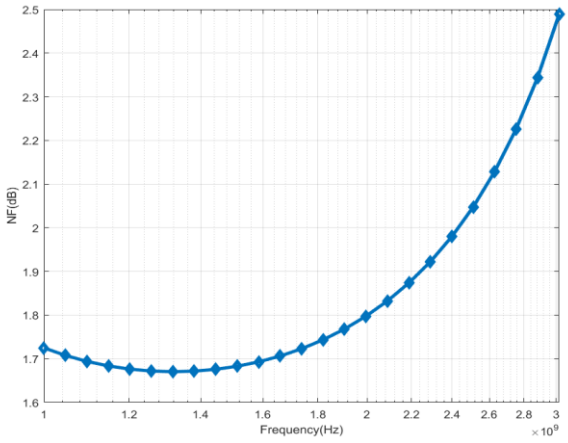


Fig. 2.7. Noise Figure

Fig2.7 gives noise figure where we can see the lowest noise is at 1.3GHz achieves 1.68 dB while below 2.5 dB at 3 GHz. The noise figure is high at 4.8 GHz due to the notch filter rejection.

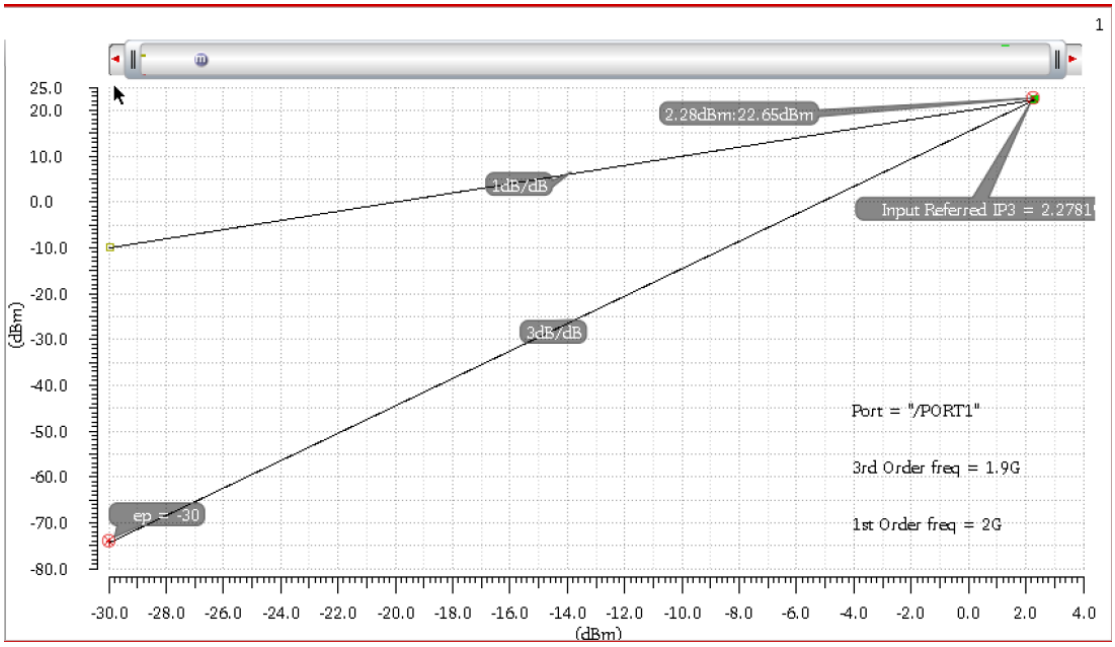


Fig. 2.8. Input-Referred IP3 of proposed LNA

Fig. 2.8 shows the IIP3 is 2.27dBm when input power is -30 dBm.

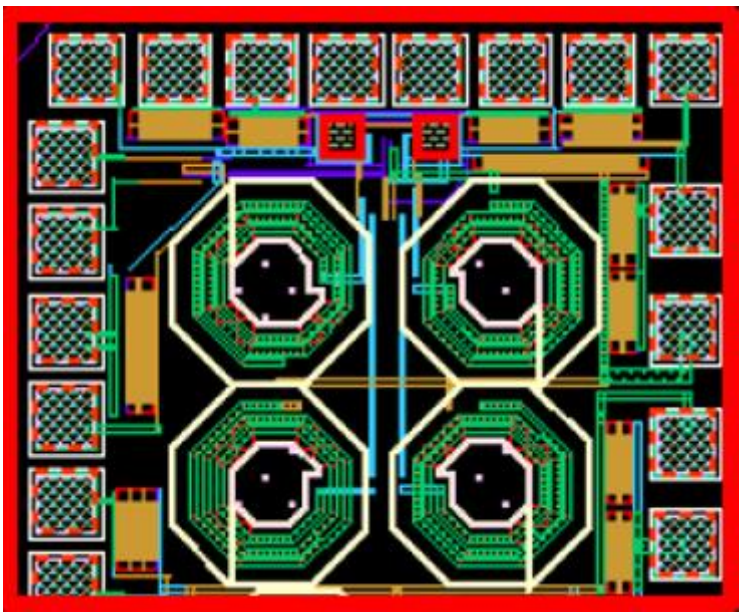


Fig. 2.9. Layout of the proposed LNA

As Fig. 2.9 demonstrates the layout of the proposed LNA. DRC and LVS are clean for tape-out.

2.4 Summary

This chapter introduces the theory of noise-cancelling LNA. Fully differential noise-cancelling LNA is proposed in this chapter while the input matching, noise figure and linearity is analyzed in this chapter. The simulation result is provided in the last section which gives us good matching, low noise figure and high Q factor of the notch filter added in the LNA.

Chapter 3 Gain-Boost N-Path Bandpass Filter

3.1 Introduction of Conventional N-Path Bandpass Filter

Recently, a tunable N-path bandpass filter is popular in filter design. The switched RC N-path filter is an inductor-less filter which can save a lot on-chip area. Its center frequency is determined by the clocking frequency while the filter bandwidth is determined by RC time constant and duty cycle of the clocking. The conventional 4-Path filter is as follow [5]:

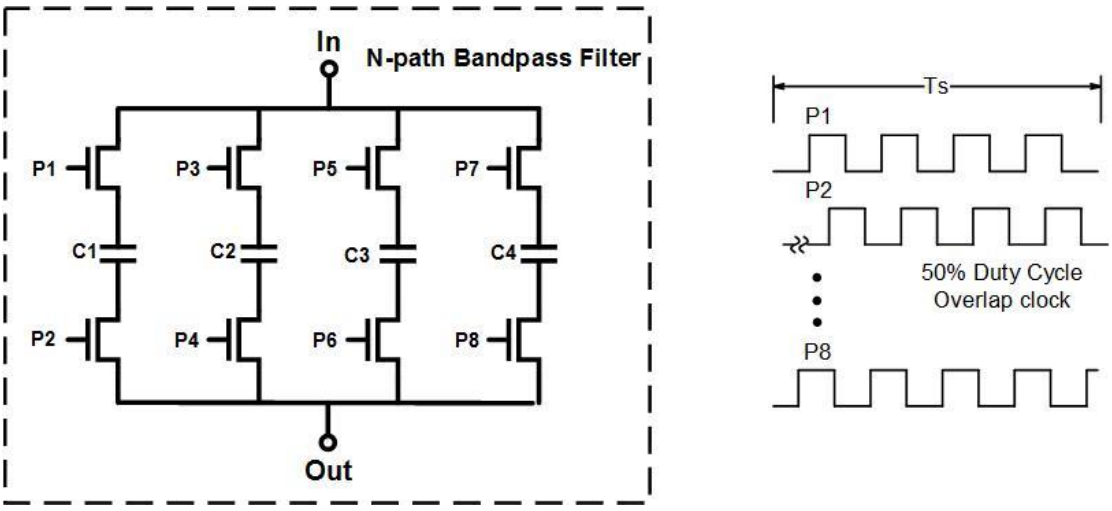


Fig. 3.1. Four-Path filter and eight phase clock

Fig. 3.1. shows the conventional N-path filter and the phase of clocking. The N-path filter is the down-convert cell with low-pass filter and an up-convert cell which behaves as a band-pass filter. From fig. 3.1. we can see there is one path connecting at a time while the clocking is 50% duty cycle. When looking into the output of the filter, the output is connecting one capacitor at a time which are C1, C2, C3 and C4. When the input signal frequency f_{in} is equal to the output signal frequency f_{out}, the input signal is charging the four capacitors in order through the on resistor of transistor. The on resistor of transistor can be defined as:

$$R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th})} \tag{3.1}$$

where μ_n is the mobility of the transistor and C_{ox} is the oxide capacitor of transistor. When the capacitors are charged enough periods, the DC value of the capacitors are equal to the average of the input signal while output is looking all of those DC voltages. Thus, the output signal is the staircase approximation of input signal as Fig. 3.2. shows.

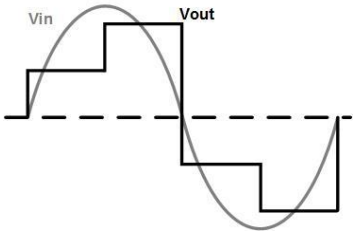


Fig. 3.2. In-band input and output signal

From Fig. 3.2, it is easy to conclude that the more path we have, the output signal will be more approximately close to the input signal. The Ron of the transistor and the capacitor will behave like a low pass filter while the bandwidth can be expressed as $\frac{1}{2\pi RC}$. Because there are four paths there, the capacitors can be regards as N times bigger and the bandwidth can be expressed as: $\frac{1}{2\pi R \cdot N \cdot C}$. For the quality factor, it can be defined as:

$$Q = \frac{f_{center}}{Bandwidth} = 2\pi R \cdot N \cdot C \cdot f_{center} \tag{3.2}$$

where Q can be high when it applicated in Giga Hertz and the bandwidth is small. Thus, the conventional N-path filter has benefited with high Q factor, tunable by the different clock frequency and contains only transistors and capacitors and low power. However, because of the bandwidth is based on RC time constant, the performance is limited by the R_{on} of the transistor and the value of capacitors. From above concerns, small R_{on} which causes smaller insertion loss

may require large transistors. The large transistors represent high load for the clock which means it needs to burn more power to drive the transistors. Large capacitors are also required for the small bandwidth which may cause large area on the chip. Thus, a gain-boost N-path bandpass filter will be proposed and analyzed in next chapter.

3.2 A Gain-Boost N-path Bandpass Filter

3.2.1 Introduction

A new gain-boost N-path bandpass filter is proposed in this chapter. This filter is based on a resistor feedback trans conductance amplifier with an N-path filter in its feedback network. The signal coming from the input will be filtered both in input and output. An eight path overlap clocking filter which can be modeled as a high Q factor RLC network is also proposed in this work. This eight-path filter can be realized as a narrow bandwidth filter which is tunable with the clock frequency. As Fig. 3.3 shows the structure of gain-boost N-path filter and the structure of the eight-path filter [6].

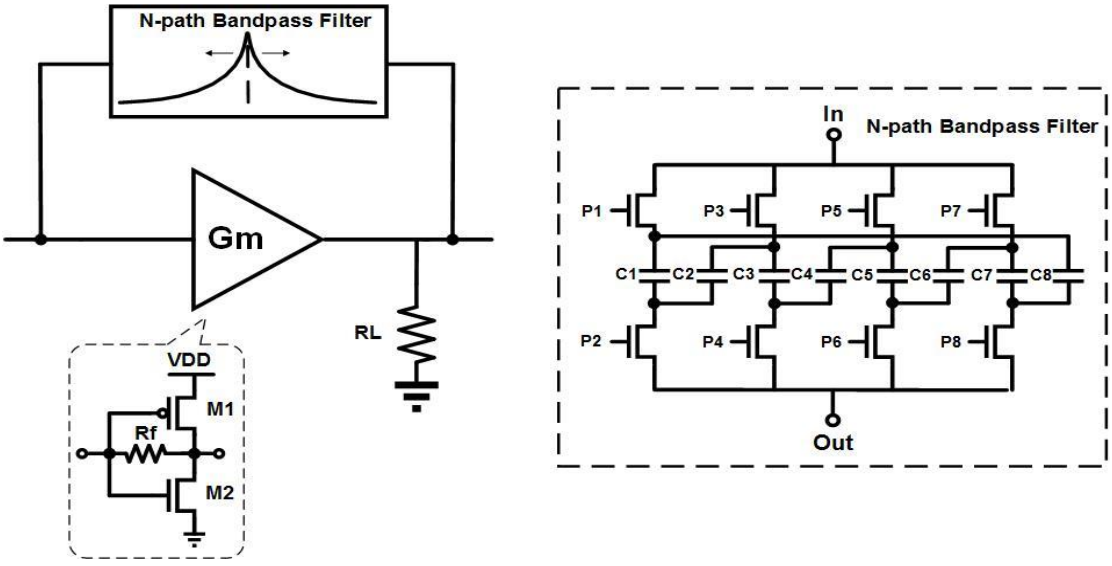


Fig. 3.3. Gain-Boost N-path filter with eight path bandpass filter in the feedback

In this structure, the performance is improved to reduce capacitors size but keep the same narrow bandwidth comparing to the conventional N-path filter which is not with a gm cell and will be analyzed in Section 3.2.1. From Fig. 3.3, the eight-path filter only has four paths that are with switches. Every two capacitors are sharing the same switch which will help reduce the load for the clock driving and clock power dissipation. The clock is 25% duty cycle overlap eight phase generated by the ring oscillator. In this way, the signal can go through each path at a time, and the clock on the same side of the filter will not be overlapped to avoid the neighbor capacitor discharge at the same time.

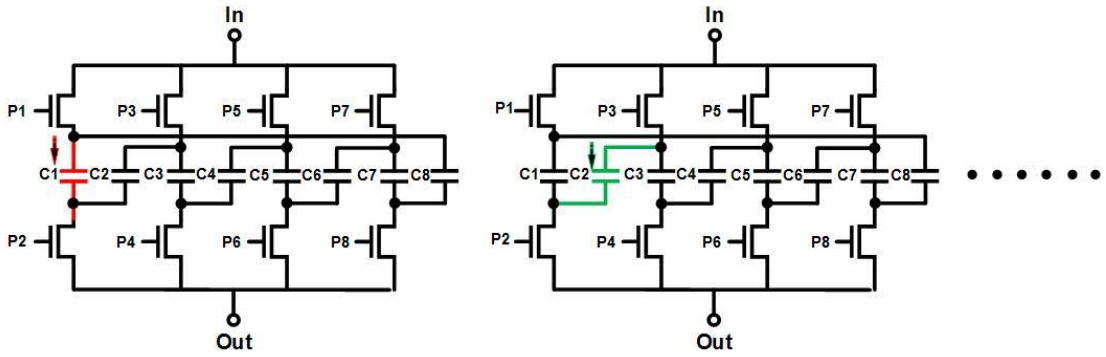


Fig. 3.4. Eight-path Filter

The ring oscillator is using Miller capacitance cancellation structure which will improve phase noise and Figure of Merit (FoM). The clock technology will be discussed in section 3.3.

3.2.2 Analysis of LPTV Circuit and Gain

As Fig. 3.3 depicts, the Gm stage is a voltage inverter with resistor feedback as self-bias. The inverter can be regarded as a trans conductance stage which can provide gain, and the output impedance can be modeled as R_L. Different from the conventional passive N-path filter, the capacitor in the feedback loop of the gain stage is similar to the capacitor multiplier. The capacitor

looking into the input will be multiplied by the gain of the Gm stage. In this way, the capacitors can be reduced to a small number which can save a lot of area on chip. Assuming the clocking frequency is equal to the input signal frequency, the N-path filter and be modeled as a RLC network and the LC will be resonated at clock frequency as Fig. 3.5 shows.

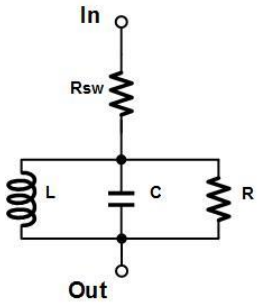


Fig. 3.5. RLC Network

In an LPTV network, the relationship between input spectrum and output spectrum can be defined as:

$$Y(f) = \sum_{-\infty}^{\infty} H_n(f) \cdot U(f - nf_s) \tag{3.3}$$

where $U(f - nf_s)$ can be regarded as the inverted input spectrum and $H_n(f)$ depicts the spectral shaping properties of the LPTV network. Thus, based on equation 3.3, the voltage on the N-path filter is defined as:

$$V(j\omega) = \sum_{-\infty}^{\infty} H_n(j\omega) V_{signal}\big(j(\omega - n \cdot \omega_s)\big) \tag{3.4}$$

where the n in $H_n(j\omega)$ is the number of harmonic of center frequency and $H_n(j\omega)$ depicts the harmonic transfer function which can be found as:

$$H_n(f) = \sum_{m=0}^{N-1} \exp(-j2\pi n\sigma_s f_s) \cdot \frac{1}{1+\frac{jf}{f_{\tau c}}} \cdot \left(\frac{1-\exp(-j2\pi n\tau_0 f_s)}{j2\pi n} + \frac{1+\exp(j2\pi\tau_1(f-nf_s)-j2\pi n\tau_0 f_s}{\frac{2\pi f_{rc}}{f_s}} \cdot G_{0,m(f)} \right) \tag{3.5}$$

where $G_{0,m(f)}$ can be defined as:

$$G_{0,m(f)} = \frac{\exp(j2\pi\tau_m(f-nf_s) - \exp(-2\pi\tau_m f_{rc})}{\exp(j\pi(f-nf_s)/f_s) + \exp(-2\pi\tau_m f_{rc})} \cdot \frac{1}{1+j(f-nf_s)/f_{rc}} \tag{3.6}$$

where $\tau_{m+1} = \frac{1}{f_s} \cdot \frac{1}{2-\tau_m}$ and $H_n(f)$ is generated by the N-path. Based on equation 3.5, we are able to define the selectivity of the harmonics at center frequency f_s. Assuming $f_s > f_{rc}$, $f = nf_s$, we have:

$$H_{0,signal}(nf_s) \approx \frac{2N(1-\cos(2\pi nD))}{4D(n\pi)^2} + (1-ND) \tag{3.7}$$

where D is duty cycle of the clock which is eight is this case. Assuming n=1 and D=12.5 for a 12.5%-duty-cycle eight phase clock, we have:

$$H_{0,signal}(f_s) = 32/\pi^2 \tag{3.8}$$

Furthermore, from Fig. 3.5 we can calculate the transfer function can be defined as:

$$H(s) = \frac{s/(R_{sw}C)}{s^2 + (R+R_{sw})s/(R_{sw}RC) + 1/(LC)} \tag{3.9}$$

where $s = -4\pi D f_{rc} \pm j2\pi f_s$. Therefore, the LC in Fig. 3.5 can be calculated as:

$$C = \frac{R_{sw}+R}{8RR_\pi D f_{rc}} \tag{3.10}$$

$$L = \frac{1}{4\pi^2 C(f_s^2 + 4(Df_{rc})^2)} \approx \frac{1}{C(2\pi f_s)^2} \tag{3.11}$$

where L and C resonate at f_s.

In this structure, the out-of-band frequency can be filtered not only at the input but also at the output. From Fig. 3.3 and Fig. 3.5, the gain at f_s at output can be defined as:

$$A_v = \frac{V_{out}}{V_{in}} = \frac{R_L[1 - g_m \cdot (R_f//(R + R_{sw}))]}{2R_S(1 + g_m R_L)} \tag{3.3}$$

where R_L is the output impedance, R_f is the feedback resistor in Gm cell and R_S is the input impedance. When g_m is the total g_m of the Gm cell, we assume $g_m R_L \gg 1$, thus equation 3.3 can be approximated to:

$$A_v|_{f_s} = \frac{V_{out}}{V_{in}} = \frac{R_L[1 - g_m \cdot (R_f//(R + R_{sw}))]}{2R_S \cdot g_m R_L} \tag{3.4}$$

For the $f_s + \Delta f_s$ signal, the RLC network can be regarded as short circuit, thus the gain at $f_s + \Delta f_s$ can be defined as:

$$A_v|_{f_s+\Delta f_s} = \frac{V_{out}}{V_{in}} = \frac{1 - g_m \cdot R_{sw}}{1 + g_m \cdot R_S + \frac{R_S}{R_L} + \frac{R_{sw}}{R_L}} \tag{3.5}$$

From equation 3.5, it is easy to find that if $g_m \cdot R_{sw} = 1$, then the gain at $f_s + \Delta f_s$ frequency will be zero which means the out-of-band filtering is infinite. Comparing to the conventional N-path filter which is not able to reject the out-of-band signal, the N-path filter in the feedback network is able to provide the wanted signal gain and reject the out-of-band signal. Furthermore, the performance of conventional N-path filter is limited by R_{on} of the transistor which determined bandwidth and rail to rail voltage of the clock which affects R_{on} of the transistor. The

new structure is determined by R_L, g_m etc.. which is more flexible and has high power efficiency.

3.2.3 Analysis of Bandwidth

From the last section, the RLC model represents N-path filter is analyzed. However, LC could only affect the center frequency of the circuit. From Fig. 3.5, the bandwidth of the passband at the input node can be approximately as:

$$\boldsymbol{BW_{in} = \frac{1}{\pi R_s C_i}} \quad (\boldsymbol{3.6})$$

where $\boldsymbol{C_i} \approx (1 + A_{vi}) \cdot C$ is multiplied by the gain of Gm stage. Regarding the gain at input node is:

$$A_{vi} = \frac{v_o}{v_i} = \frac{R_L(1 - g_m(R_f//(R + R_{sw})))}{R_s(1 + g_m R_L)} \quad (3.7)$$

the bandwidth can be defined as:

$$BW_{in} = \frac{1}{\pi R_s \left(1 + \frac{R_L(1 - g_m(R_f//(R + R_{sw})))}{R_s(1 + g_m R_L)} \cdot C\right)} \quad (3.8)$$

Comparing to the conventional N-path which the bandwidth limited by R_{sw} and capacitor, the capacitor in this structure is multiplied by gain which can save a large amount of area on chip. Assuming 3dB point is at f_{3dB} frequency, combined with equation 3.4, the gain at output node at f_{3dB} can be defined as:

$$A_{vo} = \frac{R_L(1 - g_m R_{3dB})}{R_s(1 + g_m R_{3dB})} \quad (3.9)$$

where $R_{3dB} = jL_{3dB}//R_F//R$. Because at 3dB point, $v_o/v_{3dB} = \sqrt{2}$, combined with 3.7, the bandwidth at output node can be defined as:

$$BW_{out} = \frac{1}{\pi \cdot R_F // R \cdot C} \tag{3.10}$$

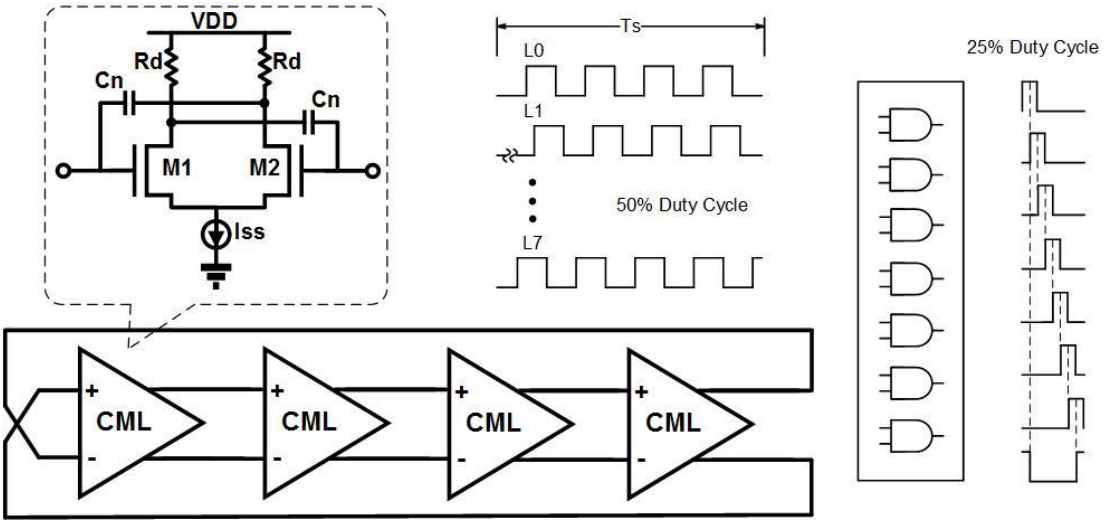


Fig. 3.5.1 Clocking

The way of clocking is presented in Fig. 3.5.1 where we can see eight phases are generated by CML cell using Miller capacitor cancellation structure which will be analyzed in next section [7]. 50% duty cycle phases are produced by ring oscillator and are sent to the AND gate for the 25% duty cycle phases. The N-path filter is clocked by eight 25% duty cycle overlapping phases which are shown in Fig. 3.3 instead of conventional non-overlapping phases. The non-overlapping clock which needs sharp edges consumes much power due to the large load from the switch. Therefore, the eight capacitors can be selected in order by 25% overlapping clock.

3.3 Clock

3.3.1 Introduction

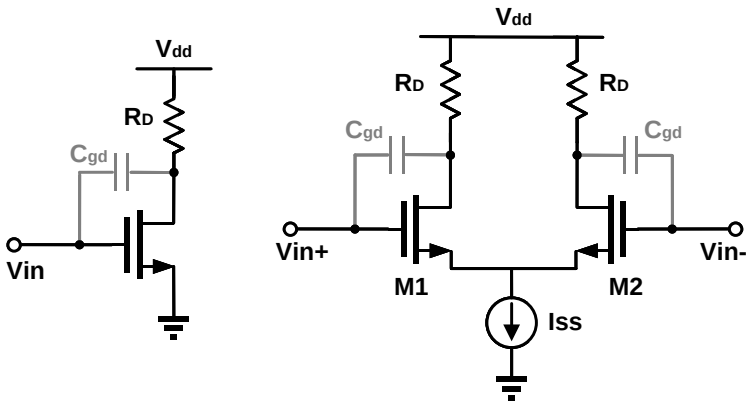
The oscillator is a significant part used in many communication systems such as phase locked loop (PLL) and N-path filter nowadays [8]. There are two main types of voltage-controlled oscillators (VCOs) which are ring oscillator and LC oscillator. LC oscillator has lower phase noise comparing to ring oscillator, but it also costs a larger area on chip and more efforts to design a high Q inductor. Thus, a ring oscillator is widely used in modern technology for it has a smaller area which is technology scalable and wider frequency tuning range based on the power supply, bias current, and component parameters while LC oscillator is limited by the Q factor of its inductor [9].

The single ended ring oscillator using inverter cell and differential pair ring oscillator using current mode logic (CML) are two of the most popular ring oscillator structure. For CMOS inverter-based ring oscillator, it contains the odd number of stages which creates the odd number of phases, and the oscillation frequency is determined by the number of stages [10]. On the other hand, the CML-based ring oscillator can create a fully differential even number of phases that can be used as a clock in the different application. Furthermore, the only parameter that can be changed in inverter-based ring oscillator is the transistor which is limited by modern fabrication technology while the performance of CML-based ring oscillator can be determined by the load resistor, transistor parameter, tail current source even output capacitor [11]. Also, the differential pair also has a higher rejection of supply noise which decreases the requirement of the supply voltage.

In this thesis proposes a CML-based ring oscillator using miller-cancelling structure. Fabricated under 130nm technology, the ring oscillator has four stages which create eight differential phases that oscillate at the 632MHz frequency.

3.3.2 Miller Capacitor Canceling Ring Oscillator

As shown in Fig. 3.3.1(a) the Miller capacitor exist in every transistor and cannot be avoided. Miller capacitor is the overlap capacitance between gate and drain named by John Milton Miller who found it first. Miller capacitor is known by all of the IC designers for its increasing switching losses and input capacitance, leading to worse frequency response.



(a) (b)

Fig. 3.6. (a) CS amplifier with Miller Capacitor. (b) Single CML cell with Miller Capacitor.

From Fig.3.6 (a), gate driving can be understood as a process of charging and discharging the gate capacitor. When the voltage in capacitor reaches the threshold voltage, the transistor will turn on. At the same time, I_{ds} starts to increase while V_{ds} start to drop. Because it needs time to charge miller capacitor, V_{gs} will not increase until miller capacitor is fully charged. Thus, miller capacitor blocks the decreasing of V_{ds} which increase the depletion time. The transit frequency f_t can be used to describe the high-frequency characteristic of a transistor which is given by:

$$\omega_T = 2\pi f_T = \frac{g_m}{C_{gs} + C_{gd}} \tag{3.11}$$

where $g_m = \mu C_{ox} \frac{W}{L}(V_{gs} - V_{th})$, then we have:

$$f_T = \frac{\mu C_{ox} \frac{W}{L} (V_{gs} - V_{th})}{C_{gs} + C_{gd}} \tag{3.12}$$

Thus we can see from (3.12) the Miller capacitor will also decrease the transit frequency and affect the high-frequency characteristic. Fig.3.6 (b) shows the single cell of CML ring oscillator without Miller capacitor canceling structure. The Miller capacitor C_{gd} across input and output node will affect the isolation from input to output and the forward gain of CS (common source) amplifier. Basically, an oscillator can be regarded as a negative-feedback amplifier which means the gain of CS amplifier should be high enough to maintain oscillation. Thus, the decreased forward gain of CS amplifier may also increase the difficulty of oscillators.

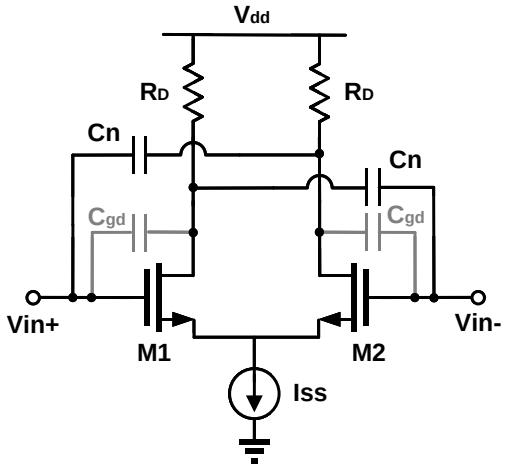


Fig.3.7 Proposed Miller capacitor canceling structure.

The proposed Miller capacitor is cancelling structure of Fig. 3.7 uses a capacitor across V_{in+} and V_{out+} (V_{in-} and V_{out+} respectively) to achieve Miller capacitor cancelling. If $C_n = C_{gd}$, the gain cross C_n is equal to the opposite gain across C_{gd}. Furthermore, the signal leak through C_n is reversed in phase when comparing to the signal leak through C_{gd}. Finally, the leaked signal through C_n and C_{gd} will be neutralized since they have the same magnitude and reversed phase

which means the isolation and forward gain will be improved [12]. Then the power is reduced, and the FoM has improved also.

Fig. 3.7 shows the four stages CML ring oscillator using Miller capacitor canceling structure. However, the oscillator requires a positive gain of each stage to make sure the oscillation occurs.

If the simple negative-feedback transform function can be view as:

$$\frac{V_{out}}{V_{in}}(s) = \frac{H(s)}{1 + H(s)} \tag{3.13}$$

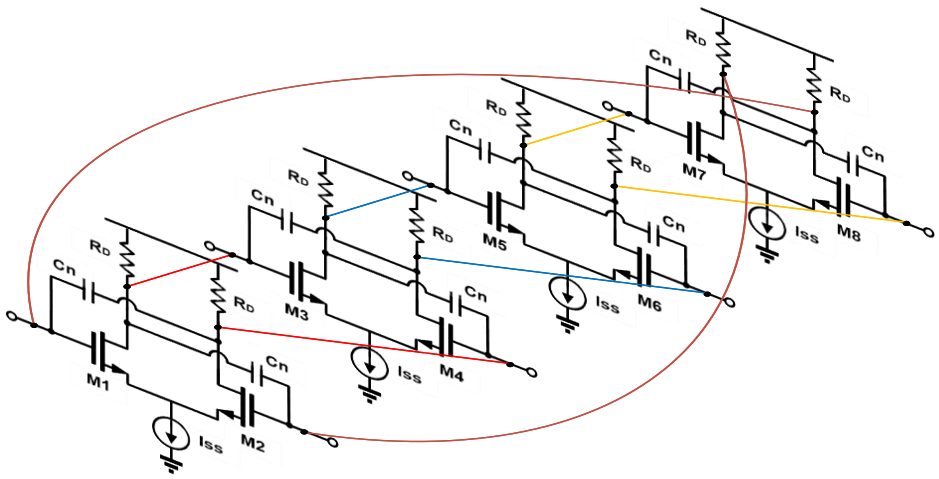


Fig. 3.8 Proposed four stages CML ring oscillator.

The oscillation only occurs when there are enough phase shifts to cause the whole feedback reaches positive which means it needs to satisfy:

$$|H(j\omega_0)| \geq 1 \tag{3.14}$$

$$\angle H(j\omega_0) = 180^{\circ} \tag{3.15}$$

where ω_0 is the oscillation frequency. Different from conventional invertor ring oscillator, CML ring oscillator shown in Fig. 3.8 is able to oscillate at the even number of stages by putting one stage not invert. Thus, for the four stages ring oscillator to oscillate:

$$H(j\omega_0) = -\frac{{A_0}^4}{\left(1+\frac{s}{\omega_0}\right)^4} \tag{3.16}$$

Each stage has to have 45° Phase shift. Thus, we have $A_o = \sqrt{2}$ to make sure the oscillation occur. And the output voltage is $V_{dd} - I_{ss}R_d$. However, if supply voltage V_{dd} is lower than a certain level, it may cause the tail transistor to reach triode region. Assuming the minimum voltage across tail transistor to make sure it operates at saturation region is V_{min}. Thus, the supply voltage V_{dd} has to satisfy:

$$V_{dd} \geq V_{min} + V_{th} + \sqrt{\frac{I_{ss}}{\mu_o C_{ox}\left(\frac{W}{L}\right)}} + \frac{R_d \cdot I_{ss}}{2} \tag{3.17}$$

to make sure the tail transistor operates at saturation region.

3.3.3 Bias and Phase Noise Analysis

The tail current transistor is necessary for providing a stable current source to ensure oscillation occurs. The tail current transistor needs to operate in the saturation region as a current source. For low phase noise and stable oscillation, it is required that the current source transistor to be the large size to achieve low flicker noise which can be modeled as:

$$\overline{V_n^2} = \frac{K}{C_{ox} \cdot W \cdot L} \cdot \frac{1}{f} \tag{3.18}$$

where K denotes a process-dependent constant. However, although large transistor has lower flicker noise, the unstable current source would still inject additional noise to the oscillator. Based on the drain current equation, both μ_n and threshold voltage are easily affected by environmental temperature which may cause unstable current source. To avoid this situation, a "current mirror" structure is needed to provide the constant current source. As Fig. 3.9 shows, M1 and the other transistors act as "current mirror" where I_{REF} is mirrored to I_{SS}. Both I_{REF} and I_{SS} can be defined as [13]:

$$I_{REF} = \frac{1}{2}\mu_n c_{ox}\left(\frac{W}{L}\right)_1 (V_{GS1} - V_{th})^2 \tag{3.19}$$

$$I_{SS} = \frac{1}{2}\mu_n c_{ox}\left(\frac{W}{L}\right)_{2,3,4,5} \left(V_{GS2,3,4,5,} - V_{th}\right)^2 \tag{3.20}$$

so we have:

$$I_{SS} = \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1} I_{REF} \tag{3.21}$$

where we have a temperature independence current source to provide stable tail current.

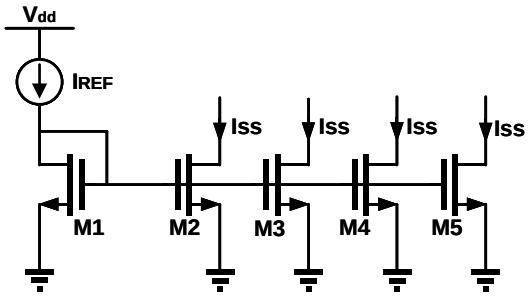


Fig. 3.9 Bias circuit diagram

The Linear Time-Variant (LTV) phase noise model provided by Dr. Hajimiri is the most widely used model in phase noise analysis [14]. Moreover, it predicts that the up-conversion noise into close-in phase noise. For the phase noise in the $1/f^3$ region is given by:

$$\mathcal{L}\ \{\Delta\ \omega\} = 10 \cdot \log(\frac{c_0^2}{q_{max}^2} \cdot \frac{\frac{\overline{\imath_n^2}}{\Delta\ f}}{8 \cdot \Delta\ \omega^2} \cdot \frac{\omega_{\frac{1}{f}}}{\Delta\ \omega}) \quad (3.22)$$

Where $\overline{\imath_n^2}/\Delta\ f$ denotes the noise source contribution at the output, and $\omega_{1/f}$ is the device $1/f$ noise while c_0 is the coefficient. q_{max} can be described as $C_{tot} * V_{swing}$ at the output node. And c_0 is the function of effective impulse sensitivity function (ISF):

$$c_0 = \frac{1}{\pi} \int \Gamma_{eff}(x) dx \quad (3.23)$$

where Γ_{eff} is the effective ISF. Thus we can reduce the up-conversion low-frequency noise by reducing c_0. The symmetry of half-circuit in differential ring oscillator becomes important since it creates the differential signal [8]. Furthermore, because the swing is due to the RC time constant, using linear resistive load is important to improve the supply noise rejection. In addition, 50% duty cycle will also reduce c_0 through changing ISF which means the CML ring oscillator will help improve phase noise.

3.3.4 Ring Oscillator Simulation and Measurement Result

The proposed Miller canceling CML ring oscillator was implemented in a 0.13 μm RF CMOS technology. The oscillator and output buffer are placed together with core area only $140\times72um^2$ as shown in Fig. 3.13. The oscillator uses four stages of the single cell which create two differential phases at each stage and the total number of phases are eight. Fig.3.10 shows the measured phase noise when oscillating at 632MHz frequency which is -113.76 dBc/Hz while total current is only 3.6mA current under 1.4V power supply. The oscillation tuning range is from 450MHz to 690MHz as shown in Fig. 6 where we can see the frequency increase as power consumption increase. As Fig. 3.10 shows the measured phase noise versus frequency. With the supply voltage and power

increase, the frequency will increase while the phase noise even lower. The calculated FoM can reach -162.78 dBc/Hz using the equation:

$$FoM = \mathcal{L}\ \{\Delta\ \omega\} - 20 \cdot \log\left(\frac{\omega_0}{\Delta\ \omega}\right) + 10 \cdot \log(P_{DC}) \tag{3.24}$$

where P_{DC} is the total power consumption of the ring oscillator and $\mathcal{L}\ \{\Delta\ \omega\}$ is the phase noise at ω_0 oscillation frequency. $\Delta\ \omega$ is the offset frequency where we use 1MHz here. Therefore, the proposed inductor-less Miller capacitor cancelling CML ring oscillator is able to oscillate at megahertz frequency and achieves lower phase noise and lower power consumption with summarized comparison Table I. And we are still doing further improvement in smaller feature size technologies. As Fig. 3.10 shows that the simulated eight phase oscillator and Fig. 3.11 shows the simulated phase noise.

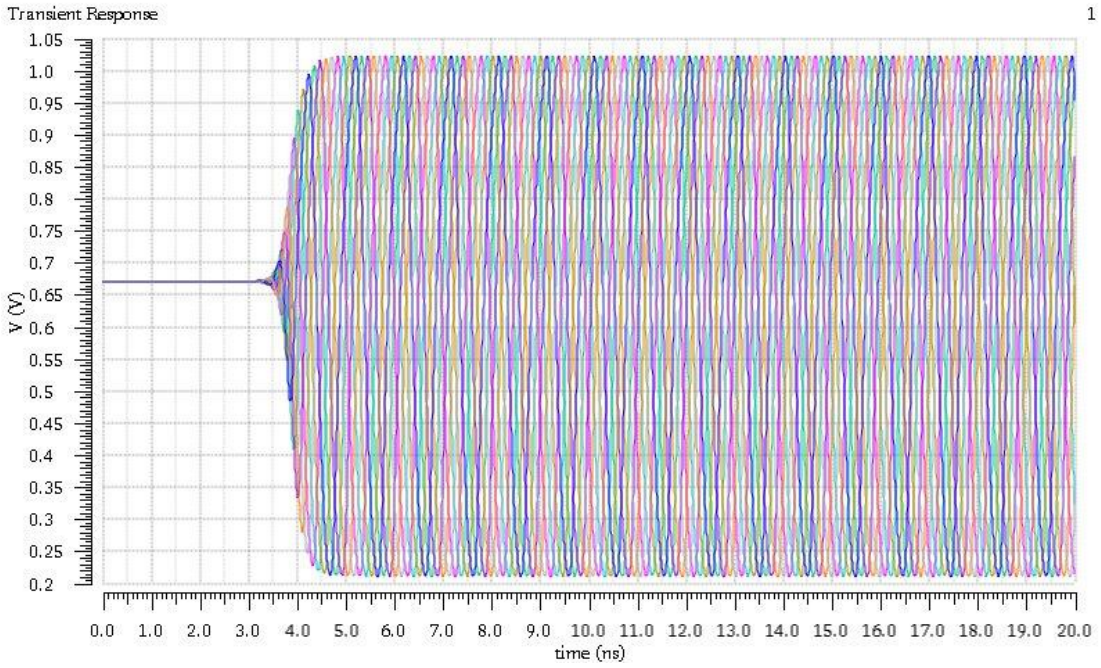


Fig. 3.10 Eight phase generated by oscillator

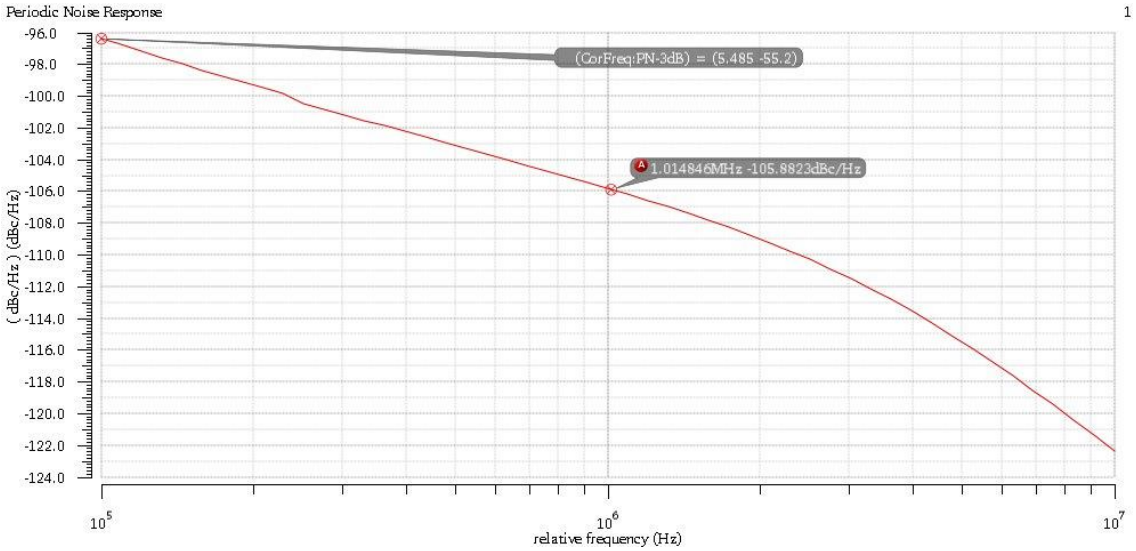


Fig. 3.11 Simulated phase noise of oscillator

The supply voltage for ring oscillator is 1.2V while each CML cell in it consumes 2.7mA current. Therefore, the total current for ring oscillator is 10.8mA under 1.2 supply voltage which represents the most power dissipation of the gain-boost N-path filter. From Fig. 3.11, the simulated phase noise is -105.8 dBc/Hz at the 1GHz operating frequency.

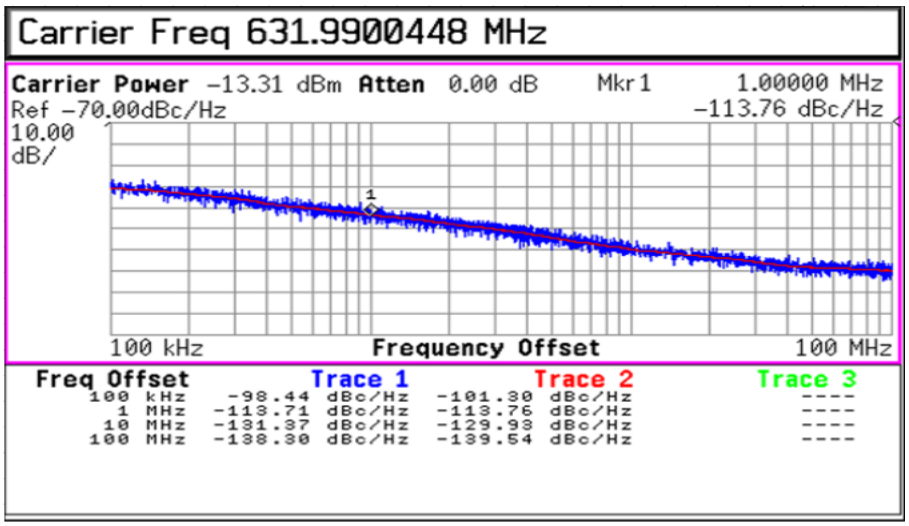


Fig. 3.12 Measured phase noise

Measurement is using Spectrum Analyzer for phase noise measurement. Chip is wire bonding in the package which soldered in PC board. The parasitic capacitor is within expected which causes

the frequency decreased. The measurement data includes return loss comes from the impedance line. The comparison table is provided below.

TABLE I PERFORMANCE COMPARISON OF RING OSCILLATOR

	[8]	[15]	[16]	[17]	This work
Technology	65 nm	90 nm	90 nm	65 nm	130 nm
Tuning range (GHz)	-----	0.63~8.1	0.2~1.8	0.882~1.36	0.45~0.69
PN @ 1MHz (dBc/Hz), f_0	-100.8, 0.891GHz	-106, 0.63GHz	-110, 1GHz	-90, 0.9GHz	-113.76, 632MHz
Power Consumption (mW)	0.98	7	4.7	0.36	5
Output phases	8	4	6	8	8
Structure	Fully-diff	Single-ended	Single-ended	Fully-diff	Fully-diff
FoM @ 1MHz (dBc/Hz)	-159.8	-135	-163	-153.61	-163

From table1 this work of ring oscillator can create eight output phase which can be used in N-path filter. Lower phase noise is measured when comparing to other works list above.

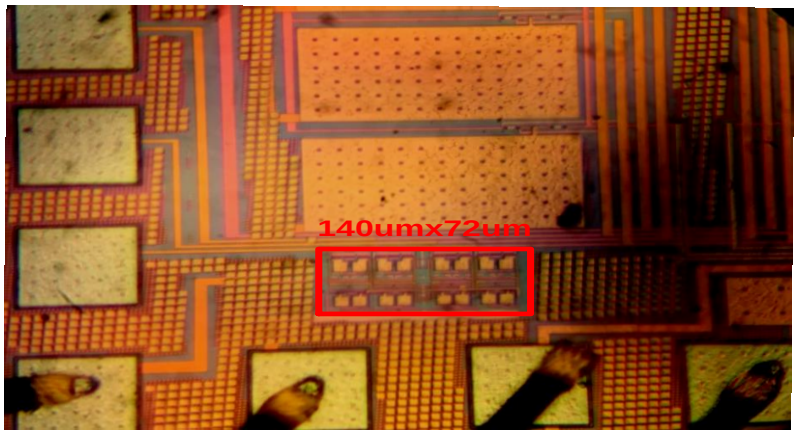


Fig. 3.13 Die photo of the oscillator

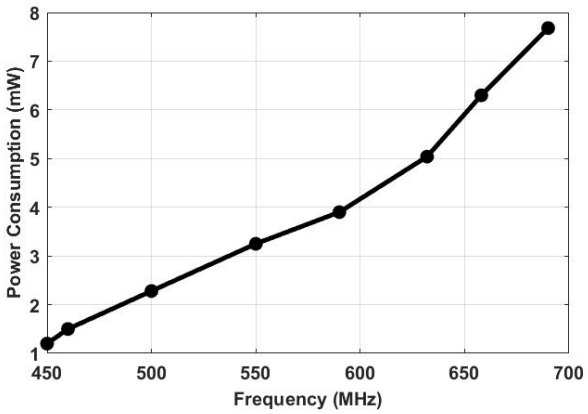


Fig. 3.14 Measured power consumption versus oscillation frequency

3.3.5 Oscillator Conclusions

This section proposed an inductor-less CML ring oscillator using Miller capacitor canceling structure. The Miller capacitor in the transistor can be neutralized by adding capacitor which is equal to C_{gd} which leads to the improved input and output isolation and forward voltage gain that help reduce the power consumption under given power supply and oscillates even under the lower power supply. Furthermore, the bias circuit was shown to provide the constant current source and the phase noise has been analyzed. In addition, the performance of proposed structure was verified by a 632MHz oscillator implemented in 130nm CMOS technology. The measured phase noise is -113.76 dBc/Hz at 1MHz offset frequency with -163 dBc/Hz FoM. Therefore, the proposed ring oscillator is able to generate the low power consumption, low phase noise multi-phases.

3.4 Gain-Boost N-path Bandpass Filter Simulation Result

The gain boost N-path bandpass filter is simulated in Cadence using PSS (Period Steady State Analysis) and PAC (Periodic AC Analysis). The PSS simulation can compute the period steady-state response of a circuit in the time domain. The shooting Newton method is used in this

simulation which allows calculating frequency translation using the saved matrices at every time point. PAC simulation is used to analyze the small-signal. The transfer function includes frequency translation can be analyzed around periodically time-varying operating points. It will compute the transfer function from one input to multi-output which is appropriate for the filter simulation. From

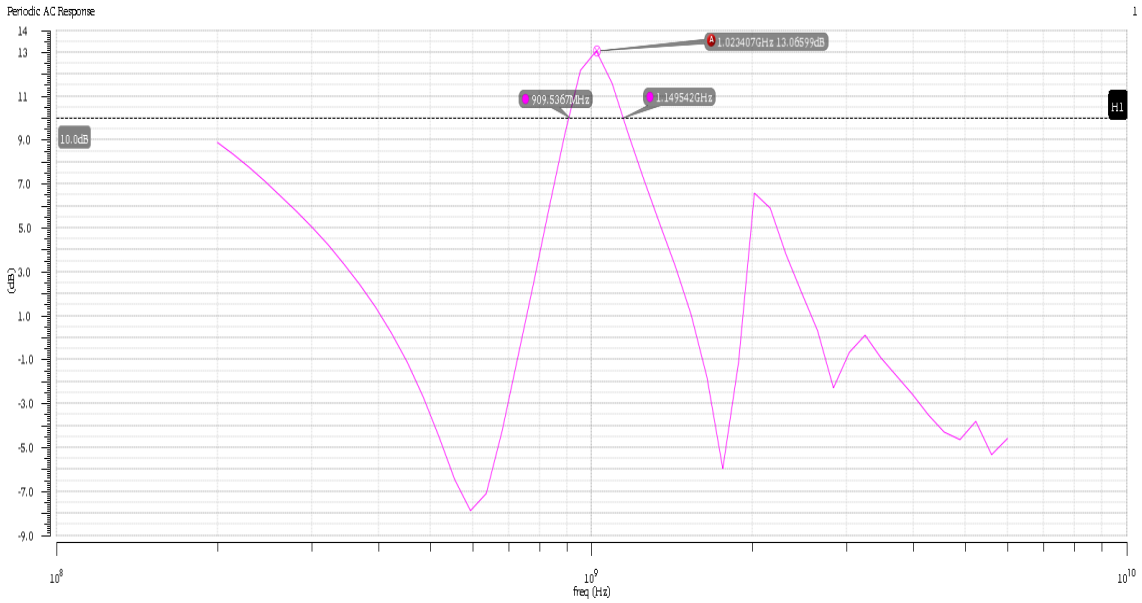


Fig. 3.15 Simulated gain-boost N-path filter (Using 4pF Cap.)

As Fig. 3.13 shows the simulation result at 1GHz input frequency. The highest gain point is at 1GHz which is +13dB. The 3dB point is from 900MHz to 1.15GHz which means the bandwidth is 215MHz. Here we use 4pF capacitor in each path of the filter, and the on resistor of each transistor is chosen to be 10 ohms. Furthermore, the out-of-band rejection can reach -8dB which give us 24dB rejection ratio.

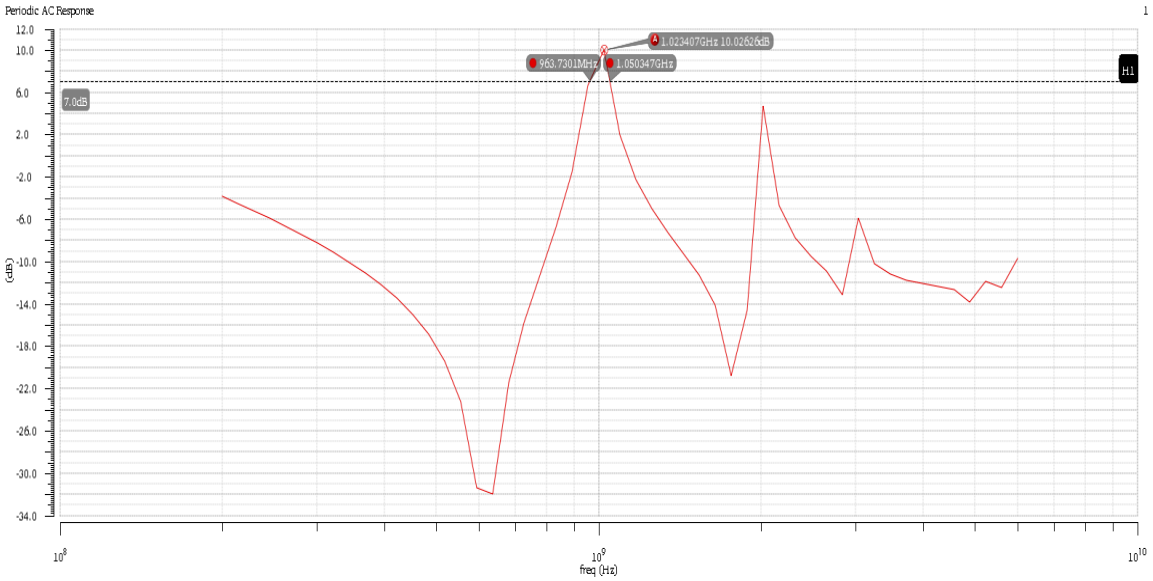


Fig. 3.16 Simulated gain-boost N-path filter (Using 20pF Cap.)

As Fig. 3.14 shows the simulation result using 20pF capacitors in each path. Since the bandwidth is reciprocal to the capacitor, the bandwidth is 87MHz from a simulation using a 20pF capacitor which is much smaller than Fig. 3.13 using 4pF capacitors in the simulation. Furthermore, the out-of-band rejection can achieve 40 dB due to the larger capacitors. The total power consumption 12mW while using a 0.13um length of the transistor as a switch in N-path filter and 0.3um length transistor in Gm stage due to the limited technology. This structure can be improved using smaller feature size technology.

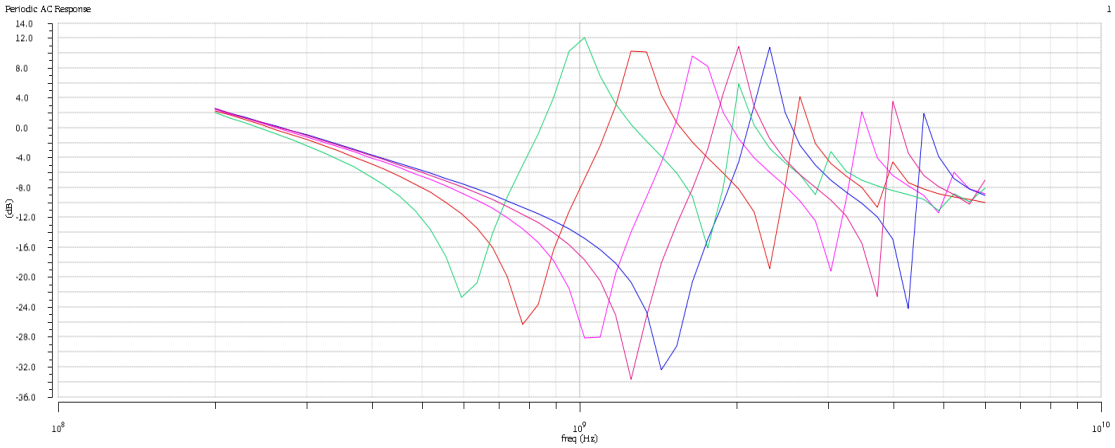


Fig. 3.17 Different frequency selection of gain-boost N-path filter

Fig. 3.15 shows the passband is selected by the clock and input frequency under 1Ghz, 1.3GHz, 1.7GHz, 2GHz, and 2.3GHz. The 3dB bandwidth is around 90MHz if 20pF capacitors are chosen in each path. The gain is higher than 10 dB while about 12mW power is burning. Out-of-band rejection ratio is achieving about 40dB.

Chapter 4 Reconfigurable Filter Design

4.1 Architecture Overview

As analyze in last few chapter, noise-canceling LNA has been popular in academic research due to its wideband matching and low noise figure. However, because of the complexity frequency band in wireless communication, the wideband matching LNA is interfered easily by the out-of-band signal. Furthermore, the filter first structure is suffered from the bad noise and limited matching due to the noise sensitivity of the first stage in frond-end. The LNA-first for the wideband matching and out-of-band rejection is proposed in this paper while the gain-boost N-path filter is put at the second stage for band selection and further gain enhancement. The proposed structure is given by Fig. 4.1.

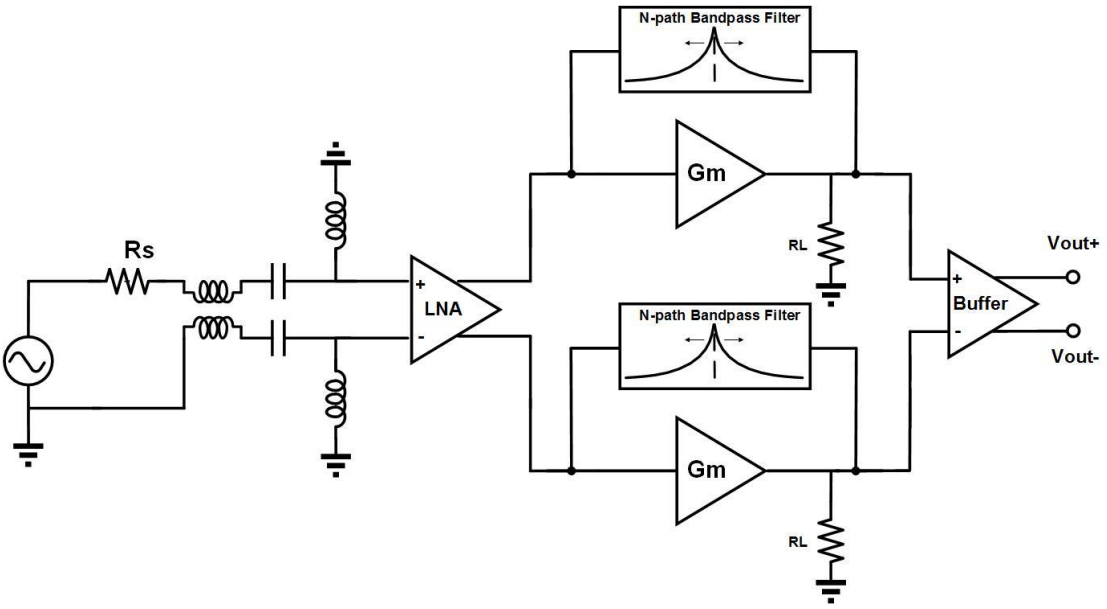


Fig. 4.1 Reconfigurable Filter

As Fig. 4.1 shows, the fully differential LNA which proposed at Section 2 is put at the first stage for the noise domain and wideband input matching while the Q-enhanced notch filter in the LNA can help reject the out-of-band signal. The gain-boost N-path filter is put at the second stage of the

band selection. The optimized N-path filter is more flexible in tuning the bandwidth which can help save a large area on the chip while the filtering effect is determined by both input filtering and output filtering.

4.2 Input Matching, Noise, and Gain

The input matching of the LNA has been discussed in Section 2 where the gm of the CG transistor has to achieve:

$$R_{in} = \frac{1}{g_{m_{CG}}} \tag{4.1}$$

for the wideband matching. Given the input impedance match the gain of CG and CS has to achieve $g_{m\_CG} = N \cdot g_{m\_CS}$, $R_1 = R_3 = R/N$ and $R_2 = R_4 = (N-1) \cdot R/N$ where R_1, R_2, R_3, R_4 has been defined in Fig. 2.3 which are the load resistor of the LNA for the noise cancellation. Once the CG transistor noise be canceled, the domain noise is coming from CS stage transistor which can be defined as:

$$F = 1 + \frac{r_{g5}}{Rs} + \frac{\gamma}{g_{m5} \cdot Rs} + \frac{Rs}{R} + \frac{1}{g_{m5} \cdot R} \tag{4.2}$$

which is the same as equation 2.10. The noise comes from the N-path filter can be ignored due to its noise will be divided by the gain of the first stage which is $A_{v\_LNA} = \frac{V_{out+} - V_{out-}}{V_{in+} - V_{in-}} = 2g_{m\_CG}R_{load}$. Combined with equation 3.4 which is the gain of the gain-boost N-path filter, the total gain of the system can be given by:

$$A_{v\_total} = 2g_{m\_CG}R_{load} \cdot \frac{R_L[1 - g_m \cdot (R_f//(R + R_{sw}))]}{2R_S \cdot g_m R_L} \tag{4.3}$$

where g_m is the total g_m of the Gm stage and the other parameter can be found in Fig. 3.3.

4.3 Simulation Result

The simulation is based on PSS and PSP. S-parameter is as Fig. 4.2 shows while the noise figure is shown in Fig. 4.3.

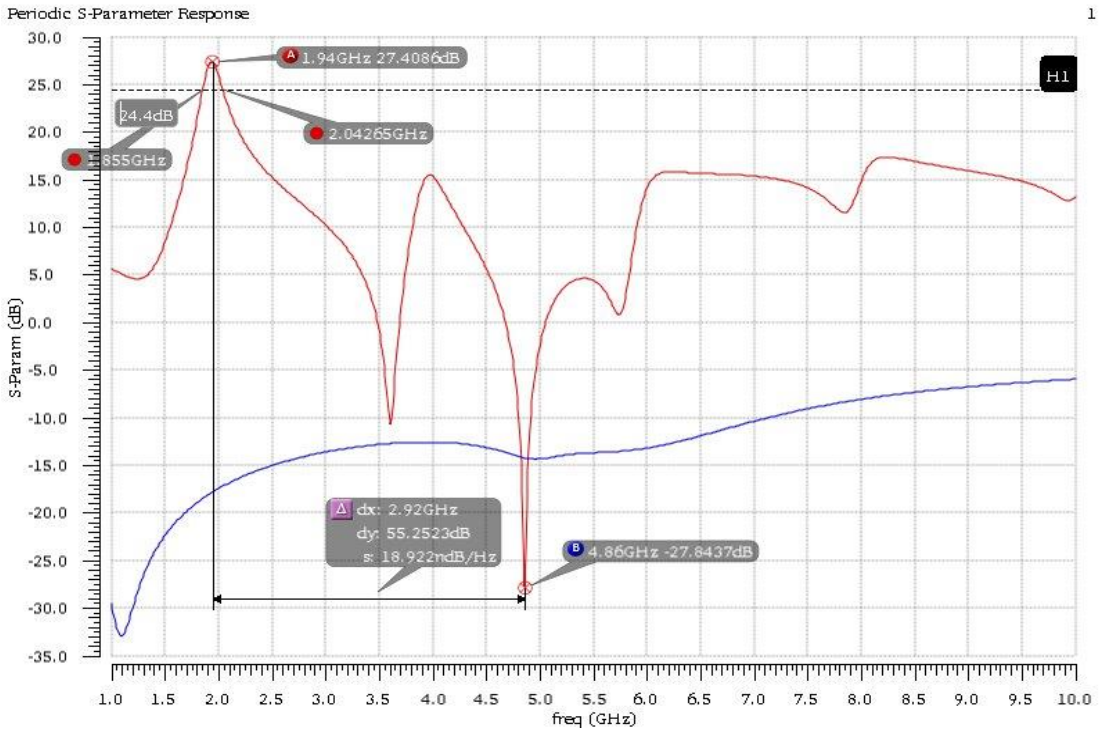


Fig. 4.2 Reconfigurable filter S-parameter simulation result

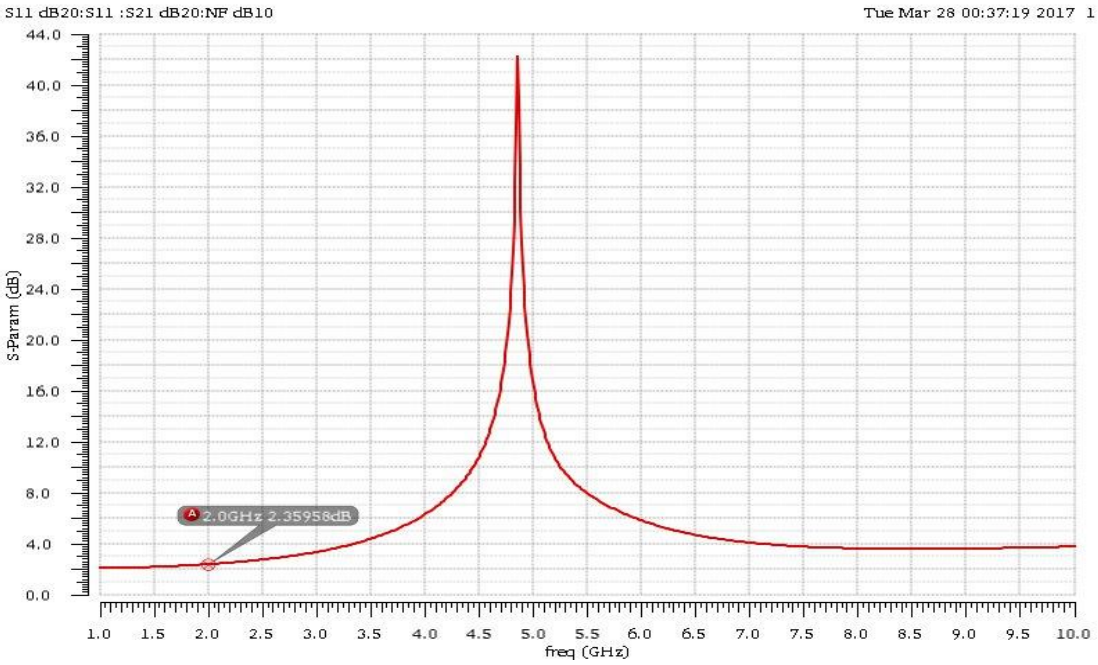


Fig. 4.3 Reconfigurable filter noise figure simulation result

From Fig. 4.2, assuming the input signal is 2GHz, and the clock is 2GHz also. The total gain of the system at 2GHz is about 27dB while the -3dB bandwidth is 185MHz using 4pF capacitor in each path in the gain-boost N-path filter. The notch filter resonates at 4.86GHz while the rejection ratio is 55.2dB. Input matching is from 1GHz to 7GHz (S11 below -10dB) which is wideband matching. Noise figure is only 2.3dB at 2GHz as shown in Fig. 4.3.

Chapter 4 Conclusion

In this thesis, a linear differential noise-canceling LNA is demonstrated. For noise-canceling LNA the broadband input impedance can be achieved by CG stage which has been analyzed in Chapter 2. The CG transistor's noise and distortion can be canceled at the output due to the same amplified signal coming from the CG stage and CS stage. Based on the resistor load in LNA, the 1.8V supply voltage is provided. The derived linearity and noise equation are all analyzed in Chapter 2 where we can see the domain noise and non-linearity contribution are coming from CS stage. From simulation result, we can see the noise can achieve lower than 2 dB while the linearity is higher than +2dBm at 2 GHz frequency. The design is implemented in 0.13um RF CMOS technology.

Furthermore, a gain-boost N-path filter is analyzed in Chapter 3. The conventional N-path filter has also been analyzed and is compared to the gain-boost N-path filter. The gain loss and extra noise contribution when put it in first stage coming from the N-path filter can be avoided by adding a transconductance stage which is inverter in this case. The N-path filter is put in the feedback loop of the Gm stage which can achieve frequency selection while maintaining extra gain. Tuning bandwidth is more flexible than the conventional N-path filter which only depends on the on resistor of switch and capacitor. The capacitor in the feedback loop can be regard as the Miller capacitor which will be multiplied by the gain of the Gm stage thus it can save more area on the chip. The clock for N-path filter is using 25% duty cycle overlapping eight phase which is generated by the ring oscillator. Miller capacitor cancellation structure is proposed for the ring oscillator which can improve phase noise, and FoM and further help reduce flicker noise in gain-boost N-path filter. The measured phase noise of the ring oscillator is provided in Chapter 3

while the simulation result of gain-boost N-path filter is also provided in Chapter 3.

References

[1] S. C. Blaakmeer, E. A. M. Klumperink, D. M. W. Leenaerts and B. Nauta, "Wideband Balun-LNA With Simultaneous Output Balancing, Noise-Canceling and Distortion-Canceling," in *IEEE Journal of Solid-State Circuits*, vol. 43, no. 6, pp. 1341-1350, June 2008

[2] Razavi B, Behzad R. RF microelectronics[M]. New Jersey: Prentice Hall, 1998

[3] J. Jussila and P. Sivonen, "A 1.2-V Highly Linear Balanced Noise-Cancelling LNA in 0.13-μm CMOS," in *IEEE Journal of Solid-State Circuits*, vol. 43, no. 3, pp. 579-587, March 2008

[4] D. Ma and F. F. Dai, "A 7.27 GHz Q-Enhanced Low Noise Amplifier RFIC With 70 dB Image Rejection Ratio," in *IEEE Microwave and Wireless Components Letters*, vol. 20, no. 8, pp. 456-458, Aug. 2010.0

[5] A. Ghaffari, E. A. M. Klumperink, M. C. M. Soer and B. Nauta, "Tunable High-Q N-Path Band-Pass Filters: Modeling and Verification," in *IEEE Journal of Solid-State Circuits*, vol. 46, no. 5, pp. 998-1010, May 2011

[6] Z. Lin, P. I. Mak and R. P. Martins, "Analysis and Modeling of a Gain-Boosted N-Path Switched-Capacitor Bandpass Filter," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, no. 9, pp. 2560-2568, Sept. 2014

[7] J. Zhu, H. Krishnaswamy and P. R. Kinget, "Field-Programmable LNAs With Interferer-Reflecting Loop for Input Linearity Enhancement," in *IEEE Journal of Solid-State Circuits*, vol. 50, no. 2, pp. 556-572, Feb. 2015

[8] S. Abdollahvand, L. B. Oliveira, L. Gomes and J. Goes, "A low-voltage voltage-controlled ring-oscillator employing dynamic-threshold-MOS and body-biasing techniques," *2015 IEEE International Symposium on Circuits and Systems (ISCAS)*, Lisbon, 2015, pp. 1294-1297

[9] S. Abdollahvand, J. Goes, L. B. Oliveira, L. Gomes and N. Paulino, "Low phase-noise temperature compensated self-biased ring oscillator," *2012 IEEE International* Symposium *on Circuits and Systems*, Seoul, 2012, pp. 2489-2492.

[10] E. J. Pankratz and E. Sanchez-Sinencio, "Multiloop High-Power-Supply-Rejection Quadrature Ring Oscillator," in *IEEE Journal of Solid-State Circuits*, vol. 47, no. 9, pp. 2033-2048, Sept. 2012.

[11] Song S, Kim B, Xiong W. "The Oscillation Frequency of CML-based Multipath Ring Oscillators." *Journal of semiconductor technology and science*, vol 15, issue 6, pp. 671-677, 2015.

[12] D. J. Cassan and J. R. Long, "A 1-V transformer-feedback low-noise amplifier for 5-GHz wireless LAN in 0.18-μm CMOS," in *IEEE Journal of Solid-State Circuits*, vol. 38, no. 3, pp. 427-435, Mar 2003.

[13] B. Razavi, Design of Analog CMOS Integrated Circuits, 2001, McGraw-Hill.

[14] A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators," in *IEEE Journal of Solid-State Circuits*, vol. 33, no. 2, pp. 179-194, Feb 1998.

[15] Chih-Kong Ken Yang, R. Farjad-Rad and M. Horowitz, "A 0.6/spl mu/m CMOS 4Gb/s Transceiver With Data Recovery Using Oversampling," *VLSI Circuits, 1997. Digest of Technical Papers., 1997 Symposium on*, 1997, pp. 71-72.

[16] E. J. Pankratz and E. Sanchez-Sinencio, "Multiloop High-Power-Supply-Rejection Quadrature Ring Oscillator," in *IEEE Journal of Solid-State Circuits*, vol. 47, no. 9, pp. 2033-2048, Sept. 2012.

[17] Chunyang Zhai, J. Fredenburg, J. Bell and M. P. Flynn, "An N-path filter enhanced low phase noise ring VCO," *2014 Symposium on VLSI Circuits Digest of Technical Papers*, Honolulu, HI, 2014, pp. 1-2.