Multi-phase Clock Generation Techniques Based on Coupled Oscillators

by

Rong Jiang

A dissertation submitted to the Graduate Faculty of
Auburn University
in partial fulfillment of the
requirements for the Degree of
Doctor of Philosophy

Auburn, Alabama
December 16, 2017

Keywords: voltage-controlled oscillator (VCO), multi-phase clock generation, phase noise, phase accuracy, Alder's equation, transformer coupling

Approved by

Fa Foster Dai, Chair, Reynolds Family Endowed Professorof of Electrical and Computer Eng.
Bogdan M. Wilamowski, Professor of Electrical and Computer Engineering
Michael C. Hamilton, Associate Professor of Electrical and Computer Engineering
Guofu Niu, Alumni Professor of Electrical and Computer Engineering

Abstract

This dissertation presents high-performance coupled-oscillator systems based on the LC oscillator, and covers both the theoretical analysis and the implementation. To that end, it starts with the introduction of both the LC oscillator and coupled-oscillator systems, and includes general considerations, basic principles, performance metrics, design factors, and design methodologies.

In addition, this dissertation reviews the following proposed and implemented novel circuits, techniques, and application: 1- two types of high-performance oscillators; 2- two types of multi-phase clock generation techniques; and 3- an application for the multi-phase clock. The wideband transformer-based voltage-controlled oscillator (VCO) utilizes a highly-compact transformer, which is designed with two (2) pairs of overlapped and interleaved inductors to achieve a strong mutual coupling factor and occupy a small on-chip area. With a strong mutual coupling factor, the equivalent inductance can be tuned using paired capacitor banks; thus, increasing the frequency tuning range.

The 8.8 GHz voltage-controlled oscillator employs a dual-tank structure and the impulse sensitivity function (ISF) manipulation technique. By utilizing these techniques, the behavior of both the tail and the cross-coupled transistors is optimized compared to the conventional VCO; therefore, the noise from the transistors and the low quality factor of the tank is reduced; resulting in a better phase noise performance.

The capacitive-coupling multi-phase clock generation technique which employs an oscillator core equipped with both dual tanks and the adaptive biasing feedback configuration achieves both low phase noise and low power consumption. To prove the concept, a four-core coupled oscillator is implemented, and an analytical model of its phase noise performance and phase error are presented by using the generalized Alder's Equation for the first time.

The transformer-based multi-phase clock generation technique achieves low phase noise while maintaining strong coupling among oscillator cores. The proposed transformer-based dual-tank topology forms a loop of coupling path for enhanced multi-phase coupling. The phase noise optimization is accomplished by leveraging the dual-tank and the adaptive-biasing feedback techniques, while the transformers facilitate strong magnetic coupling among oscillator cores. Full electro-magnetic (EM) modeling of all transformers and the passive interconnecting routes has been performed using the EMX software in order to ensure that simulated performance reflects measurement environment.

The single-ended two-port switched-RC 8-path filter followed by a low-noise amplifier (LNA) is of "filter-first" type, where the 8-path filter precedes the LNA; similar to the current state-of-the-art RF frontend circuits in mobile wireless devices, where the SAW/BAW filter precedes the LNA. The 8-path filter is driven by one of the proposed on-chip tunable 8-phase LC oscillators.

Acknowledgments

It has been a great pleasure working with the faculty, staff, and students at the Electrical and Computer Engineering Department of Auburn University during my Master's and Doctoral studies.

Firstly, I would like to express my greatest thanks and appreciation to Prof. Fa Foster Dai, who provided me with the opportunity to join his research group, where I enhanced my theoretical knowledge and gained valuable design experience, which I have been using since I joined the industry and will continue to benefit during my engineering career. As my academic advisor, Prof. Dai helped me with my research as well as in personal life in every possible way. He treated me as a student, a friend, and even a family member. I also would like to take this opportunity to express my gratitude to the Committee Members; Prof. Bogdan M. Wilamowski, Prof. Michael Hamilton, Prof. Guofu Niu, and the University Reader, Prof. Liu Bo for sacrificing their own time to help me finalize my dissertation. Without their support, I could not have made it this far in my academic life. I would like to thank Prof. Bogdan M. Wilamowski for introducing me the field of neural networks, and sharing his insights and thoughts on analog circuit design. His kindness and great sense of humor encouraged me in so many ways. I would like to thank Prof. Michael Hamilton as well as Mr. Mike Palmer for their great support in the lab and help during the implementation stage. I would like to thank Prof. Guofu Niu for taking me to the world of semiconductor devices. His patience on every discussion and explanation as well as his profound knowledge solidified my understanding of this field.

I would like to extend my thanks to the great friends and co-workers, who provided unconditional help, when needed: Dr. Feng Zhao for the invaluable discussions on circuit design; Hechen Wang, Zhan Su, Yinzhou Yun, Dongyi Liao, Ruixin Wang, Lingxiao Wang, Xuetao Wang, Zequn Liu, Yu Wang, Junchao Wei, NianJun Fu, and Ning Hou who accompanied me through many difficult and delightful times in school. Special thanks to Hossein Noori, Haopei Deng, Li Ke and Yucheng Tong for their close collaborations at work, and especially to Hossein Noori, whom I collaborated with over several projects at work and academic research and publications.

I would also like to give my thanks to my employer Peregrine Semiconductor Corp., and my managers, Jonathan Klaren, Michael Conry, and Nicholas Comfoltey for their great support on my research and publications.

My academic work and achievements could not have been possible without the love and encouragement from my parents, my family members, and the people who shared their love with me. I would like to express my cordial appreciation to them for their selfless support.

Table of Contents

List of Figures

List of Tables

Chapter 1 Introduction

1.1 The Motivation of Multi-Phase Clock

For the past decades, the market for the mobile-phone and satellite networks is growing at astonishing rate. To meet the market needs, the requirement for the radio frequency integrated circuit becomes increasingly stringent, especially for the wireless system, the high performance on-chip transceiver and its sub-block circuits which are largely of demand. As one of the essential blocks, Phase lock loop (PLL) or digital phase lock loop (DPLL) plays a crucial role on up-down conversion and signal modulation. To synthesize the clean and accurate carrier signal from PLL or DPLL, the voltage control oscillator or digital control oscillator (DCO) must be low noise. For certain applications, the oscillators may even be required to cover several frequency bands or work with low power consumption.

Evolved from single-phase clock, multi-phase clock synthesizer is a newly emerging tool that is able to improve the performance of the entire transceiver, since it can be reused by more than one block. The most popular category of multi-phase family is IQ oscillator which is also named quadrature oscillator. The local oscillator (LO) signals which have 90-degree difference can be used for signal modulation or image rejection. As expanded from IQ oscillator, the multi-phase signals which have more than four phases can be used for the following applications:

A. The sub-harmonic mixer (Fig 1.1 (a)) can use multi-phase clock as LO signals to down-convert the RF signal, thus eliminate the DC offset problem in direct down-conversion structure.

B. The N-path filter (Fig 1.1 (b)) needs multi-phase signals to drive its switch arrays to form the filter profile, and the more the number of phases is the strong the out-of-band rejection is.

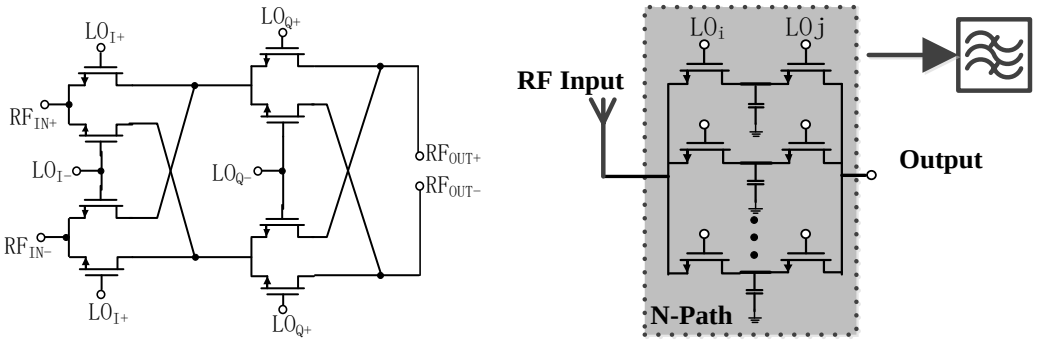
C. Interleaved analog to digital converter (ADC) (Fig 1.1 (c)) or time to digital converter (TDC) requires more number of phases to increase the sampling rate.

D. Clock data recovery (CDR) (Fig 1.1 (d)) needs multi-phase clock for phase detector to retime the clock of input signal.

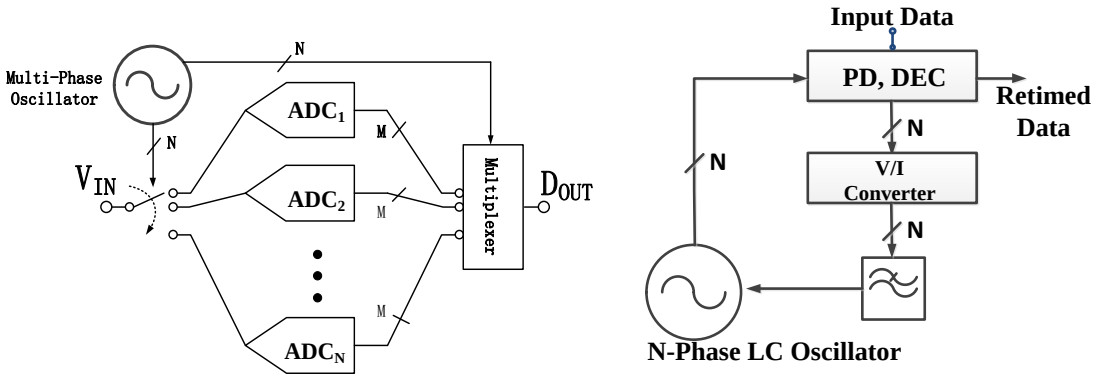
E. Phase-array requires enough number of phases of LO to finely control the direction of beam forming.

Furthermore, as the number of phases of the clock generator increases, certain benefits are obtained for those applications; e.g., less harmonic distortion for the N-path filter and higher sample rate for the ADC. Therefore, an efficient and expandable solution to generate a multi-phase clock is of high demand.

In summary, the multi-phase clock plays important and different roles in various RF blocks. However, the generation technique of multi-phase signals is still lacking attention. It's urging to have an extendable and high performance solution for it.



(a) (b)



(c) (d)

Fig. 1.1 The applications of multi-phase clock: a) sub-harmonic mixer, (b) N-path filter, (c) interleaved analog to digital converter, d) clock data recovery.

1.2 Introduction of Multi-Phase Clock Generation Techniques

According to recent publications, several techniques can be utilized for the generation of multi-phase signals. However, most conventional multi-phase clock generation mechanisms are not suitable candidates:

A. The ring oscillator has a poor phase noise, and is not qualified for GHz frequency applications;

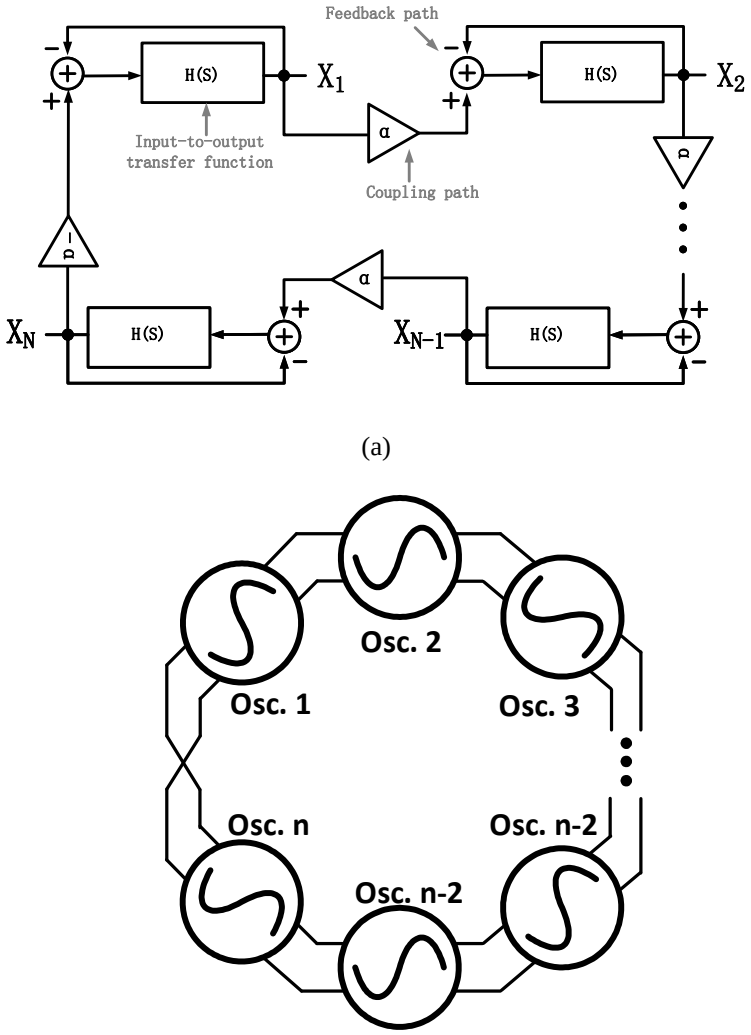
B. The divider-based generator requires a VCO with N times higher operating frequency, which increases the design complexity as the number of phases increases;

C. The ploy-phase-filter-followed structure is narrow-band, and cannot meet the requirements of today's Soft Defined Radio (SDR).

To achieve both high performance and functionalities, the coupled LC oscillators architecture seem to be the best candidate, since it can achieve a high performance, and is easy to expand to a higher number of phases by adding oscillator cells to the coupling path.

As shown in Fig.1.2 (a), the system model of coupled oscillators has three essential parts: input-to-output transfer function H(s), the feed-back path and the coupling path. The transfer function H(s) and the negative feedback path form the individual oscillator system. The coupling path couples the signals from the previous oscillator to the next. It is worth noting that the gain of the coupling path at the last stage has the same value as other stages but a negative sign. Thus, the closed-loop multi-phase system can be formed.

In addition, the equivalent model of differentially coupled oscillators is shown in Fig 1.2 (b); differential coupling signals is feeding forward to the next adjacent oscillator and the negative coupling sign can be easily implemented by crossly wiring the differential signals between the last and the first oscillators.



(a)

(b)

Fig. 1.2 Models of coupled oscillators: (a) system model of coupled oscillators, (b) equivalent model of differentially coupled oscillators.

Moreover, the noise performance of coupled oscillators is naturally superior to other systems. According to [1], as number of oscillator cores (N) increases in the coupling system, the overall oscillator phase noise will be improved by $10\log_{10} N$, if the coupling path is ideal. This indicates that additional phases and less phase noise can be achieved at the same time by using coupled oscillators.

1.3 Prior Art of High Performance Oscillator

The performance of an oscillator-coupled multi-phase clock is highly related to the performance of its individual oscillator core. Thus, the high quality multi-phase system design has to start with the design of high performance oscillators.

Regarding the performance of oscillator, low phase noise and low power consumption are the two major goals to achieve. In conventional LC oscillator design, shown in Fig. 1.3 (a), several factors directly contribute to the performances of noise and power consumption, and those are the quality factor of the LC tank Q, the noise from the cross-coupled transistor, and impulse sensitivity function which determined by the structure of the oscillator. Also, as revealed in the Leeson's equation [2], which is

$$\mathcal{L}_{vco}(\Delta f) = 10log\left\{\frac{FkT}{2P_s}\left[1+\left(\frac{f_0}{2\Delta f Q}\right)^2\right]\left[1+\frac{f_c}{|\Delta f|}\right]\right\}, \quad (1.1)$$

where the quality factor Q, K is Boltzman constant and T is absolute temperature and the noise factor F related to the transistors are two essential factors of the phase noise.

In general thought, the quality factor Q of the LC tank can be optimized by making the inductor to a certain geometry that has the least parasitic components. However, in the oscillator design, the LC tank is also loaded with passive and active devices which will also degrade the Q. For example, if the cross-coupled transistors are operating in the triode region, their small output impedances will load the tank, thus degrade the Q of the tank. To minimize this kind of degradation, the dual-tank structure [3] and class-F structure [4] were proposed and is shown in Fig. 1.3 (a). The basic concept of both structures is changing the amplitude or the shape of output waveforms to reduce the operating time in the triode region.

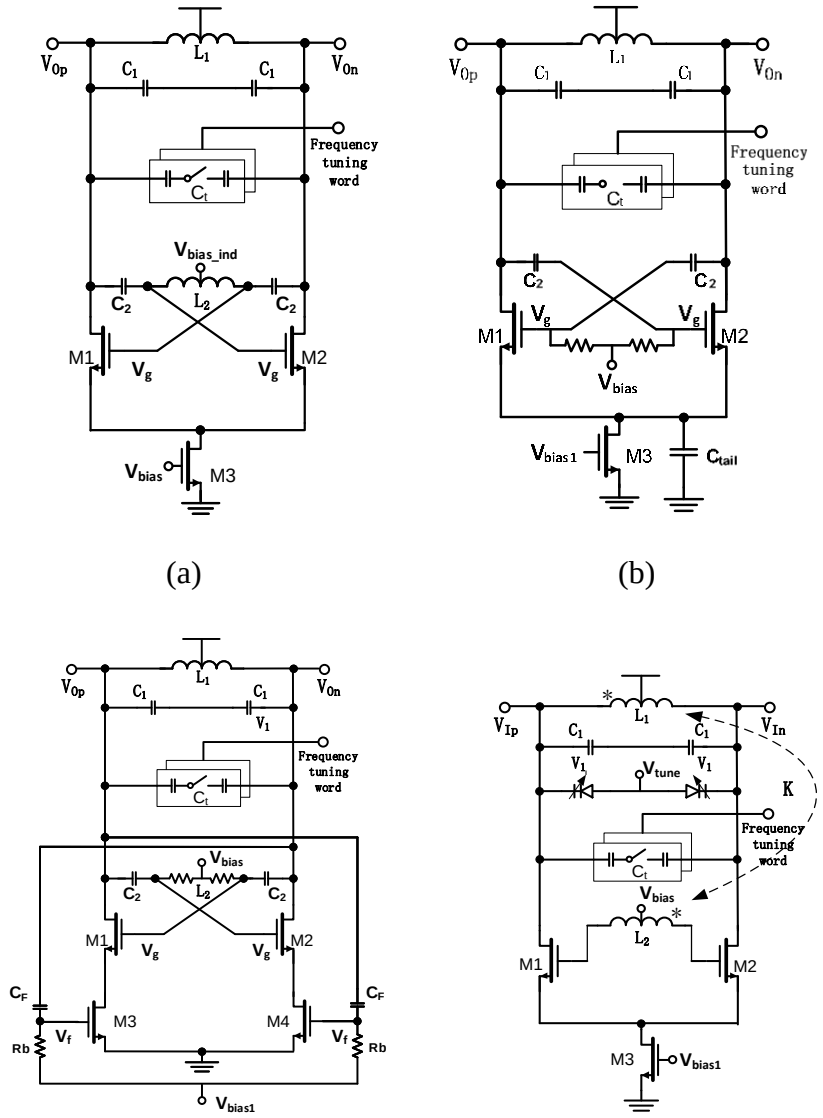


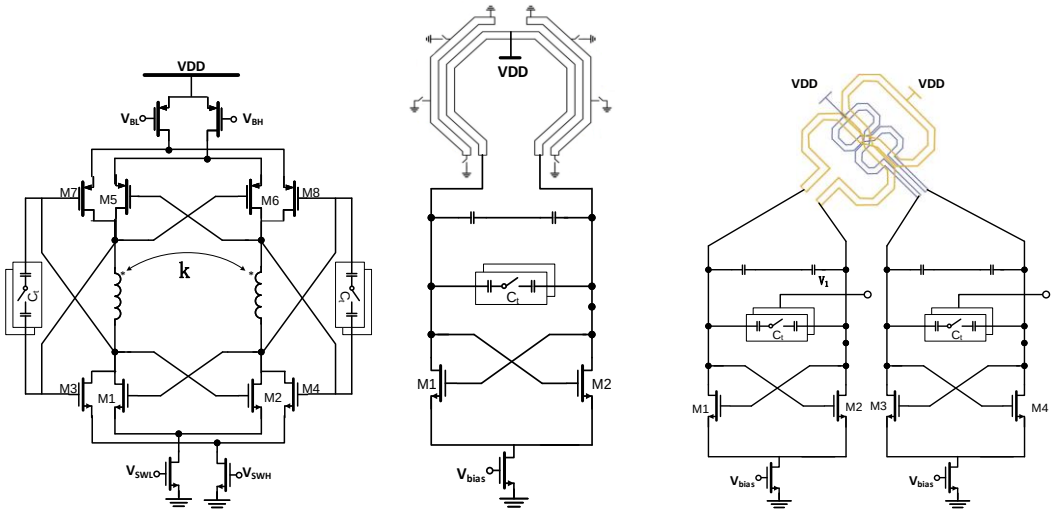
Fig. 1.3 The prior high-performance oscillator core: (a) dual-tank structure, (b) tailed capacitor (class C) structure, (c) adaptive biasing feedback structure, (d) class-F structure.

For the noises coming or converted from the transistors, it can be reduced by modifying the conventional topology to optimize the ISF of the structure or eliminate the harmonic that can be converted to output. As shown in Fig. 1.3 (b), the minimum change that can be made is to add the tail capacitor [5] to bypass the second order harmonic signal and shift its phase, thus reduce the noise conversion from the tail transistor. Other than that, as shown in Fig. 1.3(c), a more

advanced topology, which has been presented in recent year, utilize separate biasing transistors and ISF manipulation technique [6] to achieve ultra-low phase noise.

Some of those techniques which are used to achieve high-performance will be discussed in the later chapter and even adopted in the proposed designs. Also, the more insightful relation between those techniques and multi-phase clock generation will be discussed.

1.4 Prior Art of Wide Band Oscillator



(a) (b) (c)

Fig. 1.4 The schematics of the prior wide-band oscillators: (a) the active switching network based structure (b) the switchable transformer based structure (c) the Oct-shaped transformer structure.

To meet the soft defined radio (SDR) needs, the oscillators with wide frequency tuning range sometimes are of demand. However, the wide frequency tuning range and low phase noise is always a trade-off in the conventional oscillator design, because that the capacitor arrays, varactor, transformer and i.e. which are used for frequency tuning have parasitic components that will degrade the quality factor of the tank. In order to cover a wide frequency band while maintaining a good phase noise, many novel structures have been presented in recent years. For example, as shown in Fig. 1.4(a), by making the active circuit a switchable network, it allows to change the direction of the current flowing through the wings of transformer-based tank, thus to control the sign of the coupling factor and further switch between even-mode (low frequency band) and odd-mode (high frequency band) [7]; as shown in Fig. 1.4(b), by adding switches to the secondary coil of the transformer, the different segment of the transformer can be shunt to the ground thus to vary the different current return path [8], therefore the coil ratio between the

transformer pair is changed; as shown in Fig. 1.4(c), by creating the transformer based on Oct-shaped inductors, it can reduces the interference between each inductor coil, since the nature of Oct-shape inductor is to strongly immune any magnetic field that is not generated by itself [9].

In the following chapter of this thesis, a novel transformer-based quad-core oscillator will be present to illustrate how wide-band frequency can be achieved by using multiple transformers and cores.

1.5 Prior Art of Coupled Oscillators

As discussed, among all those multi-phase clock generation techniques in Fig. 1.2, coupled oscillators technique is the best candidate. However, the coupling strategy has to be carefully chosen, since improper coupling will degrade the performance of the system. The most common coupling methods including active and passive ones are shown in Fig. 1.6. The first two topologies in Fig. 1.6 are using active coupling, and two extra transistors transfer the voltage signals from the adjacent core into the current which is bumped into the tank to form coupling path. However, the structure with the parallel coupling transistor suffers from higher power consumption and the excess noise from additional active devices. Although the structure with a series coupling transistor [10] has s better phase noise performance, it requires extra headroom, which translates to higher power consumption. The last two structures are using passive cell to form the coupling paths, while one is using capacitive path [11] and another is using transformer path [12]. Comparing to the active coupling method, the passive ones have less noise source, thus are recommended and can achieve better noise performance. In addition, between the capacitor and transformer coupling, the former one is easier to implement and has better control of coupling strength; the latter one is more difficult to modeling, but the coupling path is embedded in the transformer, thus the layout of it can be cleaner and has less unexpected coupling.

In coupled oscillator, the coupling strength factor m is one key factor that represents the ratio of the injection signal over the signal sustaining the oscillation. The value factor m has to be chosen properly, since it is highly related to the performance of phase accuracy and phase noise. Different structure defines m in a different way, and even is determine by different components.

For example, the coupling strength for both active coupling in Fig. 1.5(a) (b) equals to the ratio of the transistors' size:

$$m = \frac{W_{M4}}{W_{M1}} \frac{L_{M1}}{L_{M4}}, \tag{1.2}$$

where W and L represent the width and length of the transistor, respectively.

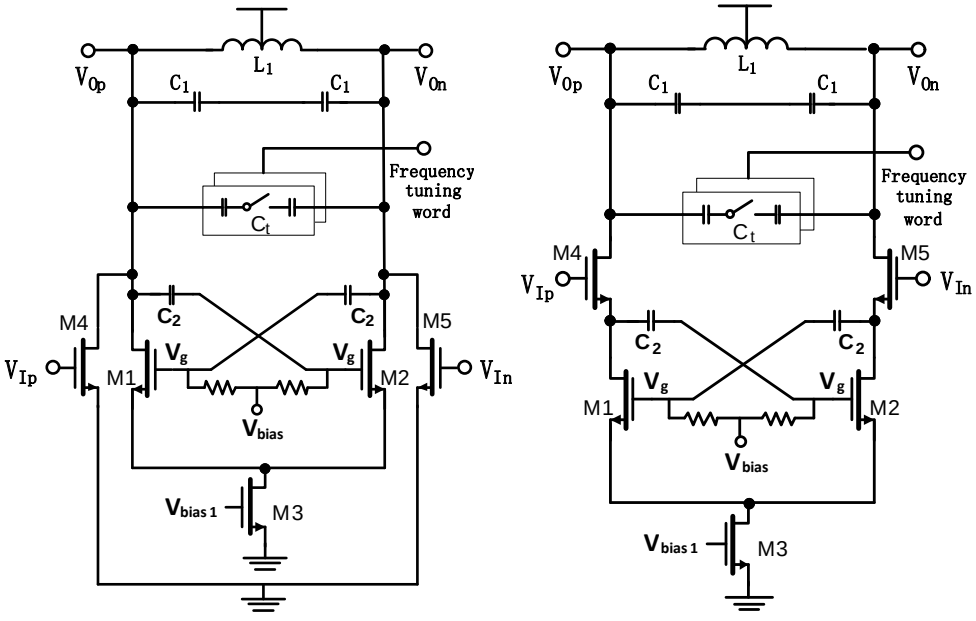
Furthermore, in Fig. 1.5(c), the coupling strength is determined by the capacitor ratio which is equal to

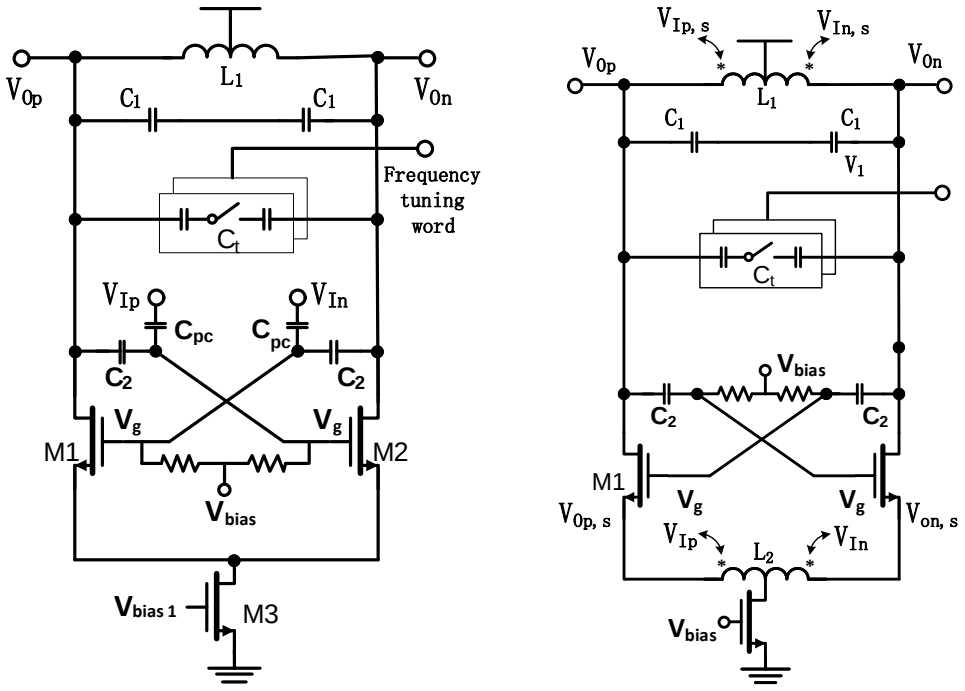
$$m = \frac{C_{PC}}{C_2}. \tag{1.3}$$

For the magnetic coupling structure in figure Fig. 1.5(d), if assuming that the coupling factor K is equal to 1, the coupling strength is

$$m = \frac{2N}{N^2-1}. \tag{1.3}$$

where N is the ratio of turns of inductor L_1 over that of inductor L_2.





(c) (d)

Fig. 1.5 The schematics of prior coupled-oscillator: (a) transistor-in-parallel coupling, (b) transistor-in-series coupling, (c) capacitive coupling, (d) inductive coupling.

1.6 Organization of Dissertation

The rest of the thesis will focus on high-performance structures of oscillator cores and multi-phase generation techniques based on coupled oscillators and passive coupling. To provide insightful views on the oscillator design, it starts with chapter 2 which covers most essential metrics and factors that need to be considered in single oscillator design, and provides detailed introduction and discussion by taking selected novel techniques as examples.

In chapter 3, silicon verifications of two oscillators will be introduced, including a wide frequency band transformer-based voltage controlled oscillator and a novel technique of frequency band enhancement based on highly compact transformer. The dedicated transformer is designed with four inductors of two pairs in overlapped structure to achieve strong mutual factors and small the inductors' area. In addition, it will present a novel 8.8 GHz voltage controlled oscillator which is employed both dual-tank structure and impulse sensitivity function manipulation technique. The behavior of both tailed and cross-coupled transistors are optimized comparing to conventional VCO, therefore the noise from transistors and tank quality degradation are reduced, resulting in better performance on phase noise.

The comprehensive discussion on coupled oscillators starts in chapter 4, where all design factors in single oscillator design will be re-defined. In addition, challenges and concerns in coupled-oscillator design are raised and addressed by proposed structures with analytical models. Moreover, to maximize the compatibility between the coupling mechanism and the proposed individual oscillator architecture, examples of coupling path designs are demonstrated with equivalent passive models.

Chapter 5 is focusing on silicon verifications of two coupled-oscillator structures, including an advanced multi-phase clock generation technique, which employs coupled oscillators with capacitive-coupling mechanism to achieve both low-power and low-noise characteristics. The oscillator core equipped with both dual tanks and adaptive feedback technique is used. In addition, by using similar oscillator core, another coupled-oscillator system with inductive-coupling mechanism is proposed to achieve stronger coupling and more symmetric flour plan. In both cases, a four-core system is fabricated to prove the concept.

Chapter 6 introduces a reconfigurable receiver frontend RFIC whose structure is based on a tunable single-ended two-port switched-RC 8-path filter f followed by a low-noise amplifier (LNA)

Chapter 7 summaries this dissertation and suggests future research topics.

Chapter 2 Design Methodology of LC Oscillator

2.1 Introduction

As introduced in the first chapter, most publications of oscillator designs are focusing on achieving low phase noise and wide frequency tuning range, since those are two key metrics for the performance of oscillators. This chapter will continue the discussion on phase noise and frequency tuning especially to the perspective of practical design. Frist, we are going to review some design factors, such as sources of phase noise and limitations on frequency tuning, based on conventional oscillator structures.

To address those issues in design, few mechanisms from the first chapters and previous publications will be presented with analytical model. In addition, essential design factors of oscillator, like response of LC tank, start-up condition and ISF, will be introduced. Their behaviors and definitions in different structures will be explained by using theoretical models and equations.

2.2 Phase Noise

2.2.1 Sources of Noise

Besides the quality factor Q of the LC tank, phase noise could be affect by the noise from all the active components in the circuit. To make it simple, we take the conventional cross-coupled structure as an example.

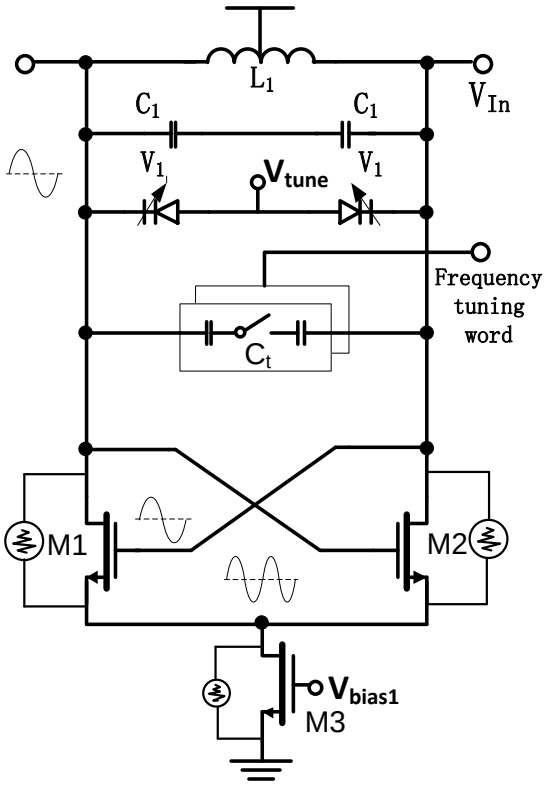


Fig. 2.1 Schematic of the conventional cross-coupled VCO.

As shown in Fig. 2.1, the sources of noise can be summarized as:

A. Noise from cross-coupled transistors (M1, M2)

B. Noise from biasing transistors (M3)

C. Low Q components seen from the tank (V1, M1 and M2)

The noise from cross-coupled transistors is varying from its states. Generally, three types of typical conditions [13] are recognized from their behavior. As shown in Fig. 2.2, during one cycle of oscillation, transistor M_1 will go through fully-off, fully-on, and the equilibrium (during transition between on and off) conditions. When the transistor is fully off, neither noise nor negative trans-conductance is generated. When the transistor is fully on, the degeneration resistor R_S, which is also the output impedance of the tail transistor in this case, can suppress the noise of the cross-coupled transistors. The gain that the noise experiences is equal to

$$G = g_m R_p/(1 + g_m R_S) \qquad (2.1)$$

where R_P is the tank impedance at the Oscillation frequency. Therefore, the noise could be high if it is not suppressed properly.

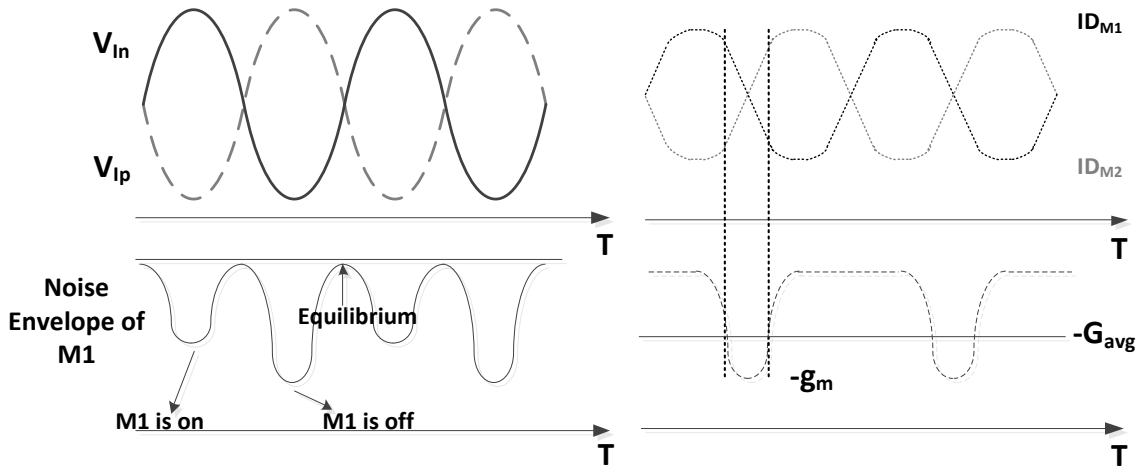


Fig. 2.2 The behavior of cross-coupled transistor over VCO output cycles.

During the equilibrium condition, when both M_1 and M_2 are on, transistors conduct the most amount of noise to the output, because that, at this time, the output voltage swing is at the zero crossing point, which is the most sensitive to the noise.

The noise from the biasing transistor will not directly affect phase noise, since, instead of going to the load, it can also going the ground. However, the modulated noise from it can be converted to the output. As shown in Fig. 2.1, the second order harmonic is formed at the drain of the biasing transistor, thus it can generate in-band noise by mixing with the cross-coupled transistors.

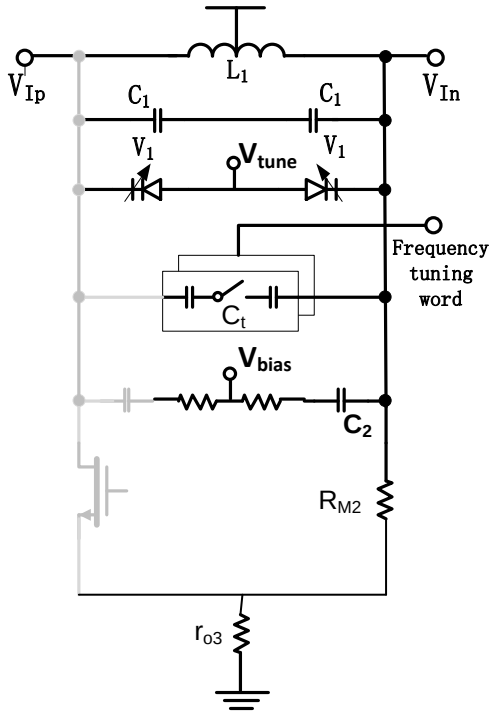


Fig. 2.3 Equivalent schematic of convention VCO when one transistor is on.

The Q degradation can be easily caused by the loss from the varactor V1, especially when the maximum capacitance C_{max} of V1 over its minimum capacitance C_{min} is too large. In addition, during triode region, the transistor not only contribute large portion of noise, but also degrades tank quality factor, because the transistors are acting like switches, thus much lower resistance is going to load the tank, as shown in Fig .2.3, where only one transistor is operating and in the triode region. Therefore, the impedance seen from the tank is equal the sum of R_{M2}

and r_{o3}, instead of $g_m r_{o1} r_{o3}$, when that transistor is in saturation region. In the conventional single-tank and cross-coupled structure, the swing of the output (drain) voltage follows the swing of the gate voltage, but they are 180 degrees out of phase. Thus, according to the saturation boundary condition which is $V_{GS} - V_{DS} < V_{TH}$, the cross-coupled transistors will operate at triode region for a long period of time in the conventional case.

2.2.2 Phase Noise Reduction

To address above mentioned degradations on phase noise, the mechanisms of few techniques will be presented in this section.

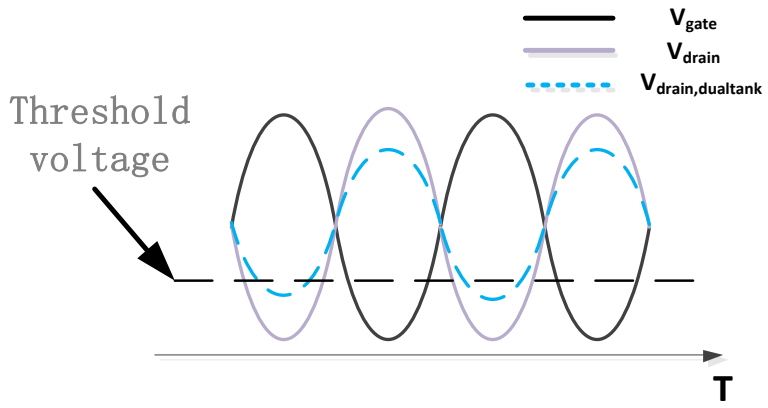


Fig. 2.4 The voltage swing of cross-coupled transistors in dual-tank structure.

Regarding the Q degradation from active cells, it can be improved by using different structures and changing the waveforms of voltages at different nodes. As mentioned in the first chapter, one way to do that is to use dual-tank structure, which is shown in Fig. 1.3(a). Because two inductors are used, the swing at the gate of the cross-coupled transistor is enhanced and can be larger than the swing at the drain. This way, the voltage swing of the drain can be reduced while keeping the voltage swing of the gate. In other words, the operation time in the triode region is reduced, as shown in Fig. 2.4.

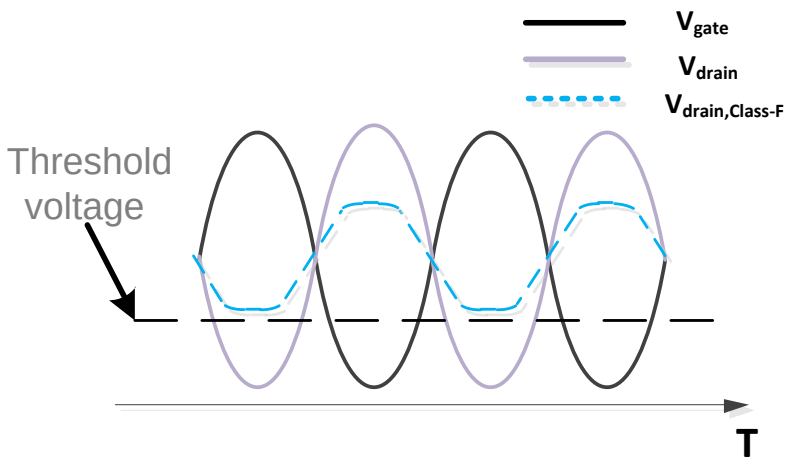


Fig. 2.5 The voltage swing of cross-coupled transistors in class-F structure.

Alternative way to do that is using Class-F structure, which is shown in Fig. 1.3(d). By combining the 3rd harmonics from the transformer, the output waveform (Drain voltage) becomes pseudo-square wave instead of sine wave. In this way, the peak value of the threshold voltage is limited to a relative value, which ensures that the cross-coupled transistors will not run into triode region, as shown in Fig. 2.5.

Since the noise converted from biasing transistor is concern, both Class-C structure and separate biasing transistor can be utilized to improve the phase noise caused by that. As shown in Fig. 1. 3(b), by adding extra capacitor to bypass the second order harmonic signal and shift its phase thus reduces the noise conversion from the tail transistor. However, it is worth noting here that Class-C only works when cross-coupled transistors are always working in the saturation region.

Similar to the structure in Fig. 1.3 (c), in the two-transistor biasing scheme, the second harmonic node is eliminated; therefore, the noise which is converted from the tail transistor and is present at output is only at low frequencies, and the second harmonic which is far from the oscillation frequency contribute negligible fluctuation to the output phase.

In addition, in Fig. 1.3(C), another technique is used, and that is adaptive basing feedback. Since the feedback will enhance the current during this condition, it might appear that it will increase both the thermal and the flicker noise; however, this is not necessarily true. That is because the cross-coupled average trans-conductance, G_{avg}, will be equal to $1/R_P$, and the extra gm generated by the feedback will force $M_{1/2}$ to switch faster, and spend less time in the equilibrium condition. Therefore, due to the constant G_{avg}, the increase in peak gm due to adaptive biasing feedback will not necessarily hurt the noise performance. In contrast, adaptive biasing feedback increases the bias current when it is needed in order to speed up the transition for suppression of the noise, as shown in Fig. 2.6.

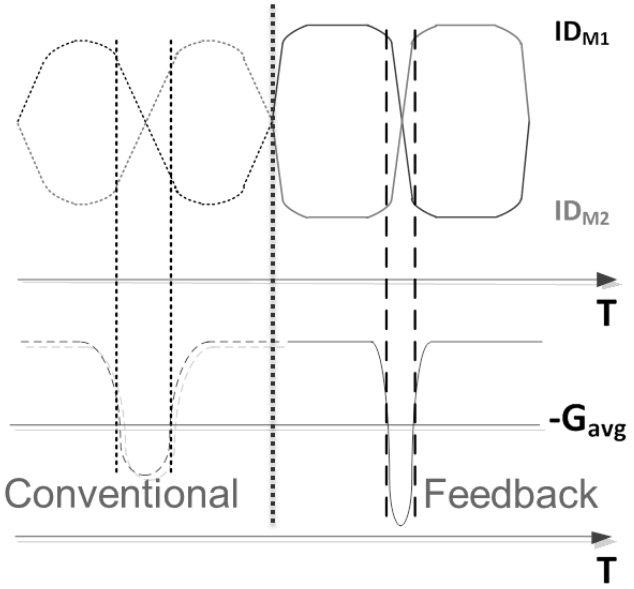


Fig. 2.6 The comparison of behaviors of cross-coupled transistors under conventional and adaptive feedback cases.

2.2.3 Boosting Signal Power

Other than reducing the noise, we can also boost the signal power to improve the phase noise, as revealed in the Lesson's equation. However, ways like increase the supply voltage and current might damage the transistor and cause reliability issue. The alternative way to do that is by using coupled-oscillators. As shown in Fig. 2.7, the simplified model of two-core coupled case, where m and m' stand for current ratio between injection current and sustaining current, namely,

$$m = I_{c1}/I_1 \tag{2.2}$$

$$m' = I_{c2}/I_2 \tag{2.3}$$

By using alder's equation [14], which will be introduced in the later chapter, the phasor relationships between two cores can be obtained:

$$\frac{d\theta_1}{dt} = \omega_0 - \frac{\omega_0}{2Q}\frac{I_{c,1}\,sin(\theta_2-\theta_1)+\frac{\pi}{4}i_n\,sin(\theta_n-\theta_1)}{I_1-I_{c,1}\,cos(\theta_2-\theta_1)+\frac{\pi}{4}i_n\,cos(\theta_2-\theta_1)} \tag{2.4}$$

$$\frac{d\theta_2}{dt} = \omega_0 + \frac{\omega_0}{2Q}\frac{I_{c,2}\sin(\theta_1-\theta_2)}{I_2+I_{c,2}\cos(\theta_1-\theta_2)} \tag{2.5}$$

where $\theta_1 = \omega_{osc}t + \ddot{\Theta}_1, \theta_2 = \omega_{osc}t + \ddot{\Theta}_2$ and $\theta_n = +\omega_m t$, θ_n is the white noise, $\ddot{\Theta}_1$ and $\ddot{\Theta}_2$ are phase fluctuation due to white noise. Therefore, it can lead to

$$\mathcal{L}(\omega_m) = \frac{1}{2V_0^2}\frac{KT}{C}\frac{\omega_0}{Q}\frac{1}{\omega_m}\frac{1}{(1+m)^2}\left(1+\frac{1}{(1+m)^2}\right) \tag{2.6}$$

If m is close to 1, around 5dB phase noise improvement can be achieved by burning extra power consumption.

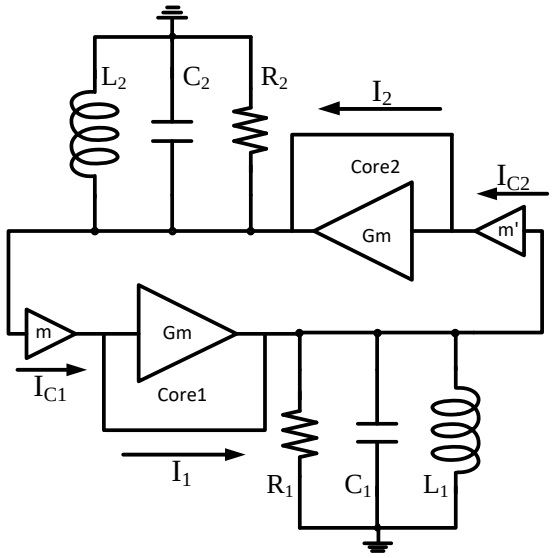


Fig. 2.7 The simplified model of two-core coupled case.

2.2.4 Noise Suppression

Although, , the noise is relatively smaller when one side of cross-coupled transistors is fully on comparing to when it is in the equilibrium region, it could be large if the noise coming from it is not properly suppressed. For example, in some case, the Q of the tank might be too small, and larger current is used to drive the tank; therefore, the output impedance of the biasing transistor becomes smaller and the noise at 'fully-on' state is less suppressed.

By using differential biasing scheme as shown in Fig 2.8, only one of the tail transistors is on; as such, the equivalent degeneration resistor exhibited by the output resistance of the tail transistor will be doubled and sufficient to attenuate the equivalent noise presented at the gate of the cross-coupled transistors, if assumes total current is the same as the single tailed structure.

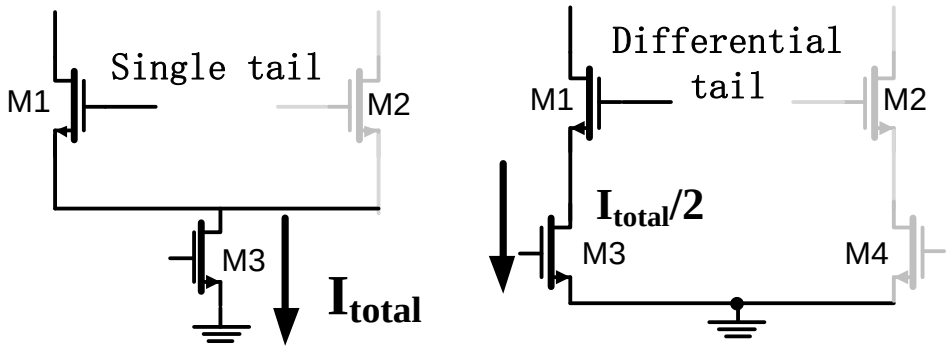


Fig. 2.8 Illustration of the current flows of both single-tail and differential-tail biasing.

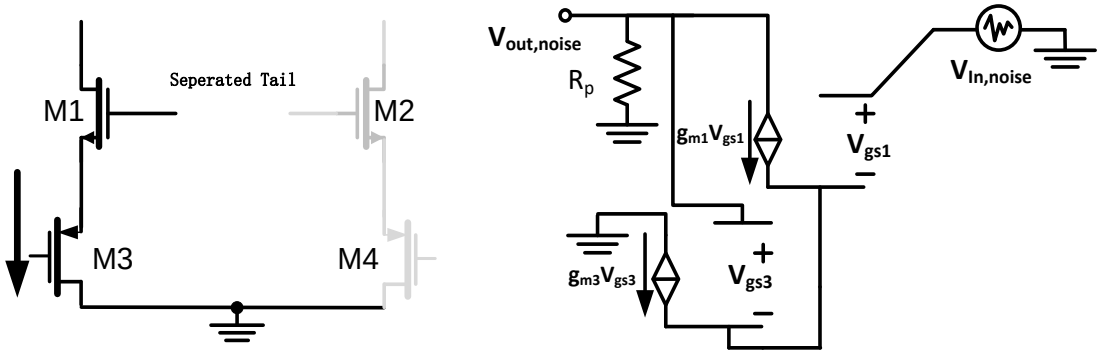


Fig. 2.9 The schematic and equivalent small signal model of differential PMOS Scheme

In some scheme, biasing transistors are replaced by PMOS, as shown in Fig. 2.9. The degenerated impedance seen from M1 is the source of M3. Therefore, the noise gain is equal to

$$G_{noise} = {R_p}\Big/\left(R_p + {(g_{mn}+g_{mp})}\Big/{g_{mn}g_{mp}}\right) \tag{2.7}$$

where g_{mn} and g_{mp} are trans-conductance of M_1 and M_3 and by making g_{mn} and g_{mp} relatively small M1 noise during on condition can be suppressed.

2.3 Frequency Tuning

Wide-band VCO design is challenge due to its trade-off between the wide frequency tuning range and the low phase noise requirements. The most common way to increase frequency tuning range is done by employing large varactor, whose parasitic components degrades Q factor of oscillator tank. Instead of using large varactor, switched capacitor arrays can be used to provide further tuning on the tank capacitance. However, increasing number of capacitor arrays will make parasitic capacitance and resistance in MOS switches non-ignorable, as a result those parasitic components will degrade the Q factor as well.

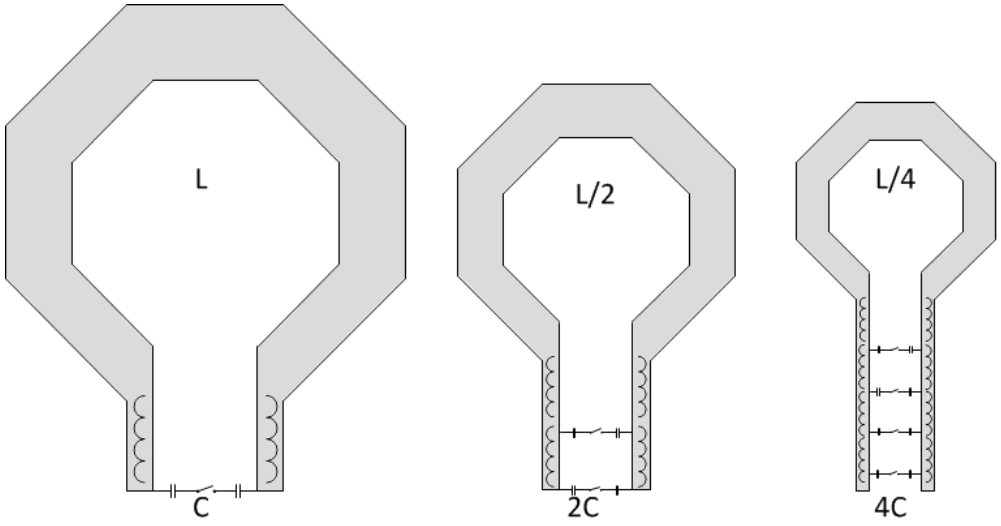


Fig. 2.10 Illustration of changes of tank by changing only passive components.

In addition, regardless of degradation on Q, the tank deign will be another challenge. As show in Fig. 2.10, as increase the scale of capacitor arrays, the load inductance L has to be scaled down accordingly to keep the same center frequency. Therefore, as the load inductor reduces and the length of the trace connecting to capacitors increases, the load inductor becomes more and more sensitive to the parasitic inductance on those traces. As a result, it's hard to estimate oscillation frequency without magnetic modeling.

In order to further increase frequency tuning range, it is desirable to explore other frequency tuning mechanisms.

2.3.1 Multi-Band VCO

The most conventional structure to overcome above mentioned issues is multi-band VCO. The concept is straight forward: use multiple oscillators and run each of them at different center frequencies to cover wide frequency band. The example of a dual-band VCO is shown in Fig. 2.11,

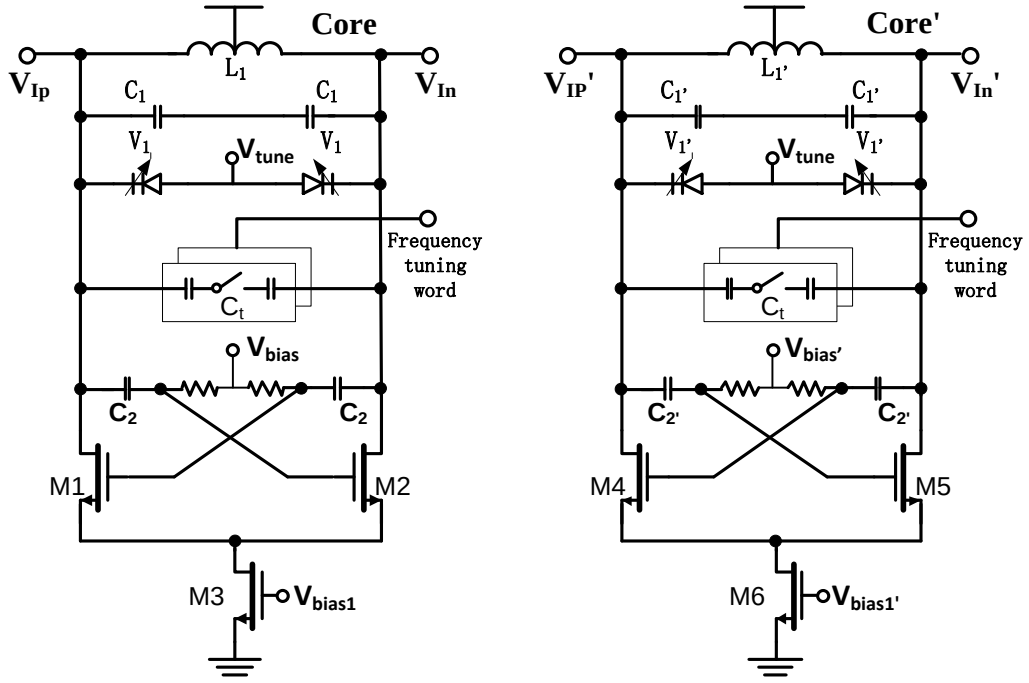


Fig. 2.11 Schematic of dual-band VCO.

where the center frequency of the first core is $\omega_0 = 1/\sqrt{L_1 C_2}$ and that of second core is $\omega_0' = 1/\sqrt{L_1' C_2'}$. By changing the operating core, the center frequency can be easily changed. This way might sound brutal, but it is the most effective way and the only concern for this structure is the chip area.

2.3.2 Transformer Based Frequency Tuning

If die area is the concern, there has another option. As mentioned, it's almost impossible to using capacitive tuning to further frequency range without degrading the phase noise, therefore transformer based mechanisms seems to be a good candidate to widen the frequency tuning range, as recent publications have already shown some of its potential, as listed in Fig. 1.4. In this section, the novel transformer-based frequency tuning mechanism is proposed.

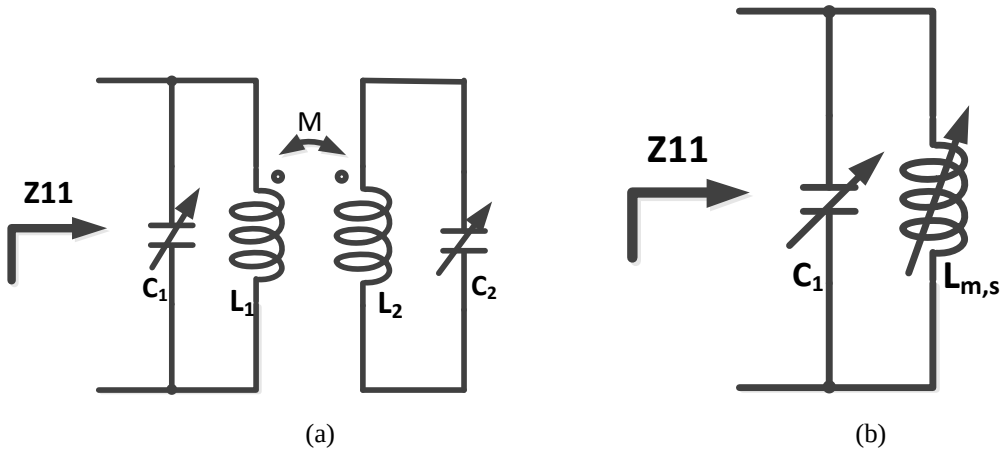


Fig. 2.12. Simplified transformer model, (a) Z_{11} of a transformer, (b) its equivalent circuit.

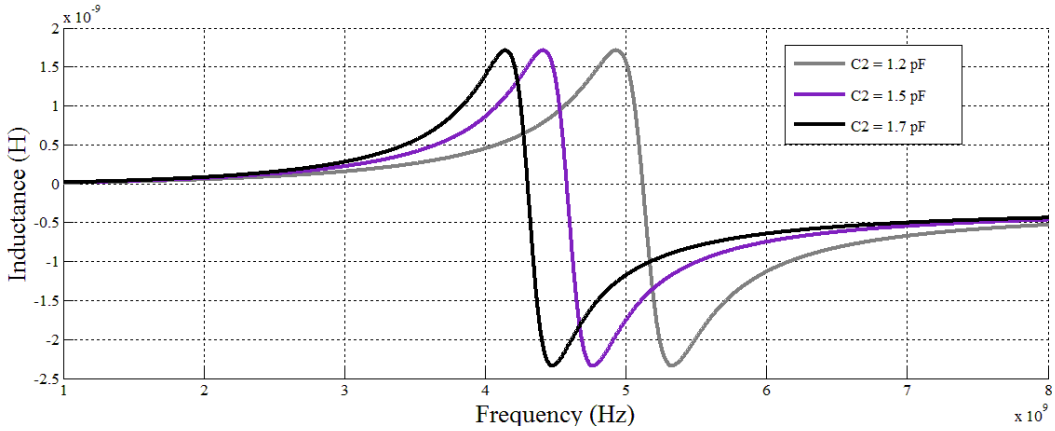


Fig. 2.13 Plots of equivalent inductance values under different C_2 values.

The proposed technique enhances the frequency tuning by switching the capacitor banks

and varactor in the coupled tank of same transformer pair, thus reuses the existing capacitors to achieve wider frequency tuning range without further degrading noise performance. This kind of mechanism can be explained by analyzing transformer tank impedance. To facilitate the analysis, it is assumed that tanks in a pair has strong mutual coupling effect and Q is infinite large. The tank impedance of Z_{11} seen from tank 1 is show in Fig. 2.12(a), where C_1, C_2 are total capacitor including varactor and capacitor bank.

Fig. 2.12 (b) shows an equivalent circuit of tank impedance, and, due to the strong coupling factor, the equivalent inductance of the tank be tuned by changing the value of C_2:

$$L_{m,s} \approx k^2 L_1 \frac{\omega_1^2 L_2 C_2}{(1-\omega_1^2 L_2 C_2)} + L_1, \tag{2.8}$$

where $\omega_1 = 1/\sqrt{C_1 L_1}$. As shown in Fig. 2.13, by increasing the value of C_2, $L_{m,s}$ will increase under certain frequency.

2.4 Voltage and Impedance Response of the Tank

Voltage and impedance response of the tank is a good tool for analyzing the behavior of the tank including oscillation frequencies and voltage swing at different voltage nodes. Hand-calculation may be sufficient enough for the conventional first –order tank, since one oscillation frequency exits, and it is also where the peak voltage is over frequencies. However, as tank structure get more complex, multiple oscillation frequencies and voltage swings might exist and it becomes hard to have intuitive feeling about the final converging state.

Take dual tank structure as an example, the equivalent circuit is shown Fig. 2.14 by injecting AC current to the tank, the plot of the voltage swing response from both gate and drain is shown in Fig. 2.15.

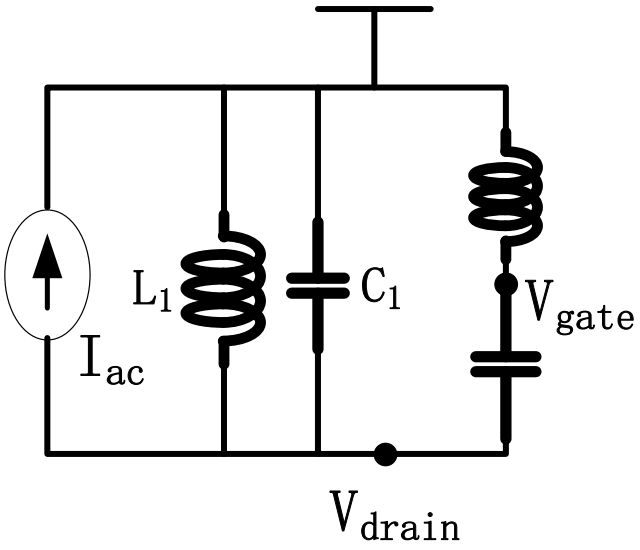


Fig. 2.14 The equivalent circuit of dual-tank structure.

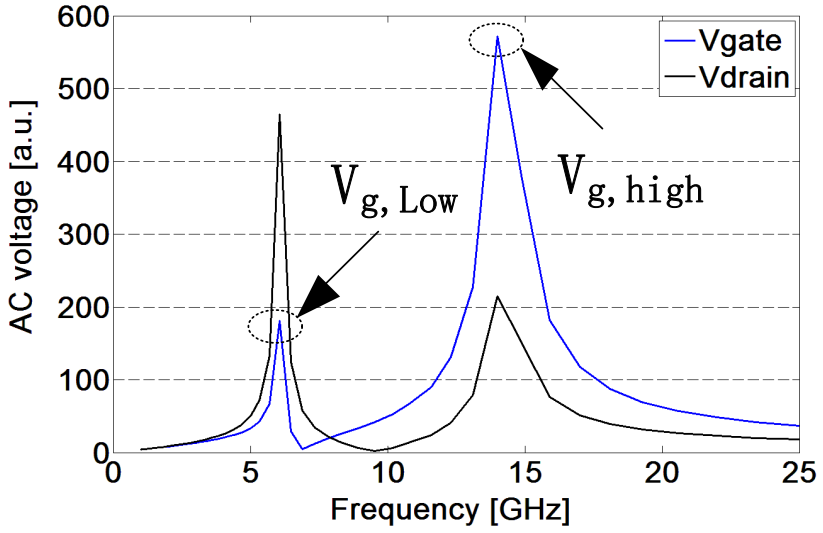


Fig. 2.15 The equivalent circuit of dual-tank structure.

As shown in Fig. 2.15, it indicates that there exist two possible oscillation frequencies. The first oscillation frequency is locating at lower frequency, where V_{gate} is smaller than V_{drain}. The second oscillation frequency happens at higher frequency, and the V_{gate} is large than V_{drain}. Since the second one is willing, only the higher frequency is the wanted one.

By plotting the real part impedance of the tank versus frequency, the peak impedance happens at the oscillation frequency. Therefore, it provides a much easier and faster way to characterize the tank. It's worth noting that the negative impedance paralleled with the tank will also affects its behavior, especially for the oscillation frequency.

The application of this technique will be discussed in the later chapter, when analyzes more complex tank structure.

2.5 Start-up Condition

The start-up condition of LC tank based oscillator is straight forward. By providing enough negative impedance to compensate the loss of the tank, the oscillator is able to sustain its output swing. In other words, the way to characterize the start-up condition for an oscillator is to characterize its impedance in parallel with the tank.

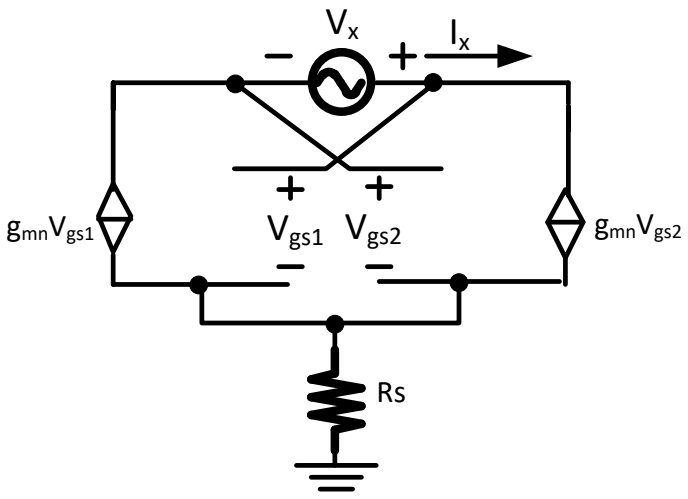


Fig. 2.16 The small signal model of the cross-coupled structure.

As shown in Fig. 2.16, in the conventional cross-coupled structure, the impedance seen from the tank is simply equal to

$$V_x/I_x = -2/g_{m1} \tag{2.9}$$

where g_{m1} is the trans-conductance of the cross-coupled transistor and R_s is the output impedance of the biasing transistor.

Since the start-up condition may vary from structures, some structures allow the oscillator to have more relaxed condition. For example, the small signal model of the active part of the biasing feedback architecture in Fig. 1.3(c) is shown in Fig. 2.17.

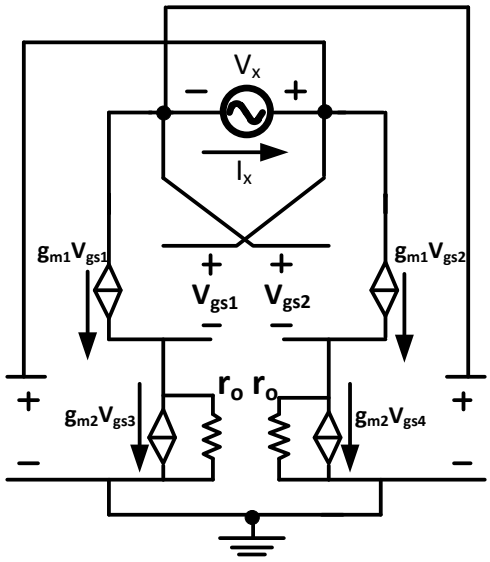


Fig. 2.17 Equivalent circuit for negative trans-conductance of the basing feedback architecture.

As a result of the feedback path, the start-up condition could be relaxed in this oscillator structure. Assume that the gate width of the bias transistors is larger than that of the cross-coupled transistors, only their output resistance, r_o, is included in the small-signal model for simplicity. For a single-core oscillator, the negative impedance seen from the tank is equal to

$$R_{startup} = \frac{2}{g_{m1}} \frac{1 + g_{m1} r_o}{1 + g_{m2} r_o} \tag{2.10}$$

which as well must be smaller or equal to the tank loss, R_p. Compare to the conventional oscillator, where the negative impedance is fixed and equal to $-2/g_{m1}$, in the proposed oscillator architecture, it is easier to achieve any negative resistance due to the factor $(1 + g_{m1} r_o)/(1 + g_{m2} r_o)$. In summary, if g_{m2} is larger than g_{m1}, which is the case in the proposed design, the startup condition will be relaxed.

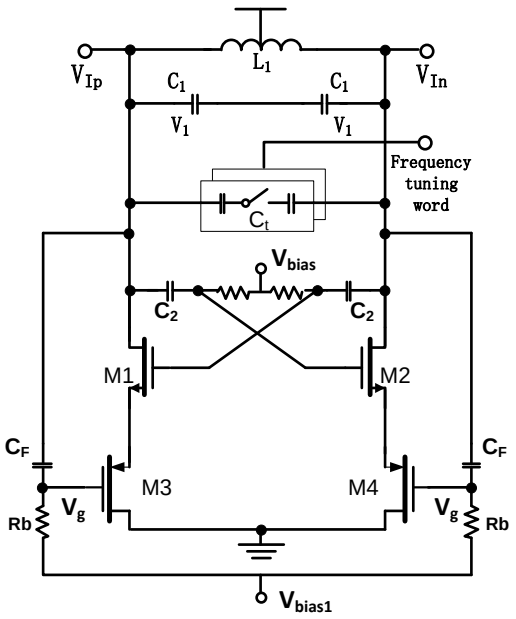


Fig. 2.18 Schematic of adaptive biasing feedback technique.

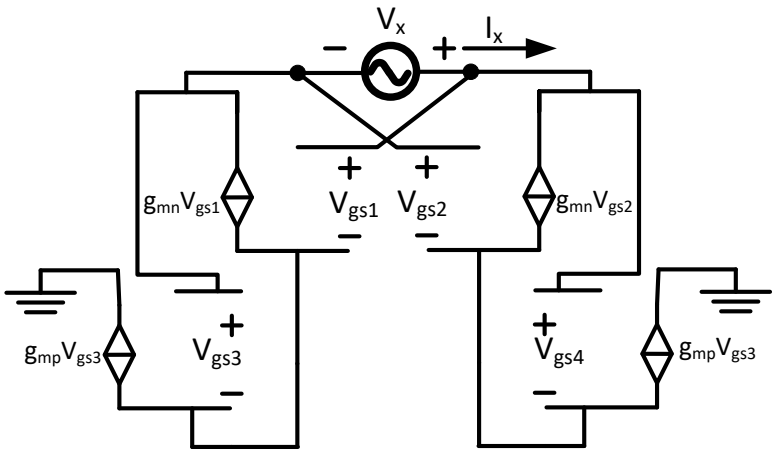


Fig. 2.19 The simplified equivalent circuit of –gm stage of proposed structure.

In some cases, the biasing transistor could affect start-up condition as much as cross-coupled transistor does. In [6], the biasing transistor is replaced by PMOS, as shown in Fig. 2.18, and its equivalent small signal model is shown in Fig. 2.19

In this case, since the PMOS is the current tail, we no longer see high impedance as conventional biasing does. In addition, the added feedback enable the role of the PMOS playing on start-up condition, therefore the negative impedance is equal to

$$V_x/I_x = -\left(1/g_{mn} + 1/g_{mp}\right). \quad (2.11)$$

If comparing to Eq. 2.7 and 2.11, it is found that the start-up trans-conductance and the suppression of the noise is another trade-off, which should be taken into considered in design.

2.6 Impulse Sensitivity Function

Impulse sensitivity function introduced by Hajimiri and Lee [15] reveals the immunity of oscillator system to noise and interruption at a specific point over one period of oscillation. Compare to Lesson's equation, it gives more intuitive guidance on how to improve phase noise in practical design. By utilizing ISF, we can easily found out those weak points which should be avoid from interruption, especially for coupled oscillators, whose coupling signal is not in phase with output signal. In addition, it's a useful tool to verify that if we properly implement techniques to improve phase noise. In this section, we are going to give a brief introduction on ISF, and start with reviewing two common impulse responses in a system level.

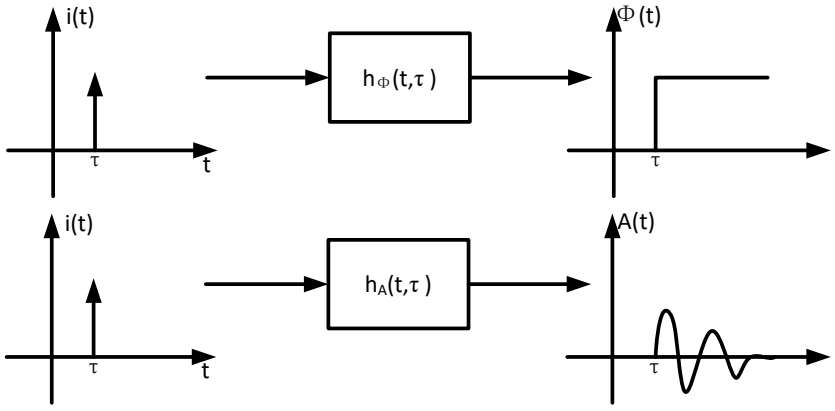


Fig. 2.20 Illustration of phase and amplitude impulse responses of oscillator system.

As shown in Fig. 2.20, signal pulse is injecting into an oscillator system and its response can be separated into two different responses, which are phase response $h_\phi(t,\tau)$ and amplitude impulse response $h_A(t,\tau)$. Fortunately, the oscillator will eventually recover its amplitude over time, thus the response on amplitude will be damped. However, the interruption on phase is going to cause a permanent shift, which the oscillator cannot recover by itself. That's why the interruption on amplitude is more welcome.

The easiest way to check those responses of an oscillator system is to look at its output waveforms. As shown in Fig. 2.21, by injecting interruption pulses at different time points, the oscillator will respond differently. Let's assume that the output signal is

$$V = A_0(t)\cos\big(\omega t + \phi_0(t)\big). \tag{2.12}$$

In a conventional oscillator structure, injecting the pulse at the peak of the output signal, only the amplitude response will be obtained, and the output is going to be

$$V_1 = \big(A_0(t) + A(t)\big)\cos\big(\omega t + \phi_0(t)\big). \tag{2.13}$$

On the contrary, injecting the pulse at the zero-crossing of the output signal, only the phase response will be obtained, and the output is going to be

$$V_1 = A_0(t)\cos\big(\omega t + \phi_0(t) + \phi(t)\big), \tag{2.14}$$

where $\phi(t)$ is the permanent phase shift caused by the pulse.

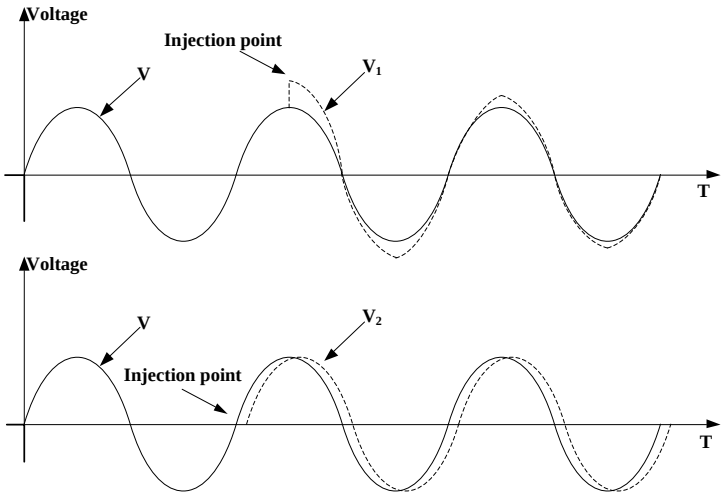


Fig. 2.21 Illustration of waveforms of phase and amplitude impulse responses.

Based on above introduction, the ISF can be roughly defined as normalized phase delay caused by a pulse at its injected phase, namely

$$h_\phi(\tau) = \Delta\phi(\tau)\delta(t-\tau)/i_n(t) \tag{2.15}$$

where $\Delta\phi(\tau)$ is the phase shift and $i_n(t)$ is the amplitude of the pulse. Normally, the ISF has its max value at zero crossing point, which also means the most sensitive point to noise, and it minimum value at peak swing.

Chapter 3 Implementations of LC Oscillators

In this chapter, implementations of two novel structures which adopt previously-mentioned techniques are presented with design details, simulation and measurement results. The first proposed structure is a quad-core dual band oscillator which utilizes both transformer based frequency tuning and signal boosting techniques to achieve wide frequency band as well as low phase noise with compact die size. Another implemented oscillator is designed to achieve low-phase noise at high operating frequency by utilizing both dual-tank and adaptive biasing feedback techniques.

3.1 A Quad-Core Dual Band Oscillator

3.1.1 Introduction

The proposed dual-band quad-core VCO utilizes strong coupling factor between coils in a pair to achieve increased tuning range by sharing their capacitor banks. The coils in a pair of the transformer are implemented using multi metal layers that exactly overlap with each other. One pair of transformer is placed inside another coil pair. As a result, no additional die area is needed to realize the dual-band transformer coupled VCO. The four transformer coils are connected to four individually controlled VCO cross-coupled cores and capacitor banks that can be turned on

or off for frequency switching. By the turning both cores in a pair on, signal strength can be enhanced for noise reduction purpose.

3.1.1 The Architecture of the Transformer-Based Oscillator

The conceptual drawing of the proposed VCO is shown in Fig. 3.1. It consists of four VCO cores connected with four inductor wings Ls, Lp Ls' and Lp', where Lp and Lp' forms the 1st transformer pair while Ls and Ls' forms the 2nd transformer pair. The structural view of the transform pairs is illustrated in Fig. 3.2. All VCO cores include capacitor arrays and varactor for frequency tuning and cross-couple stage for oscillation.

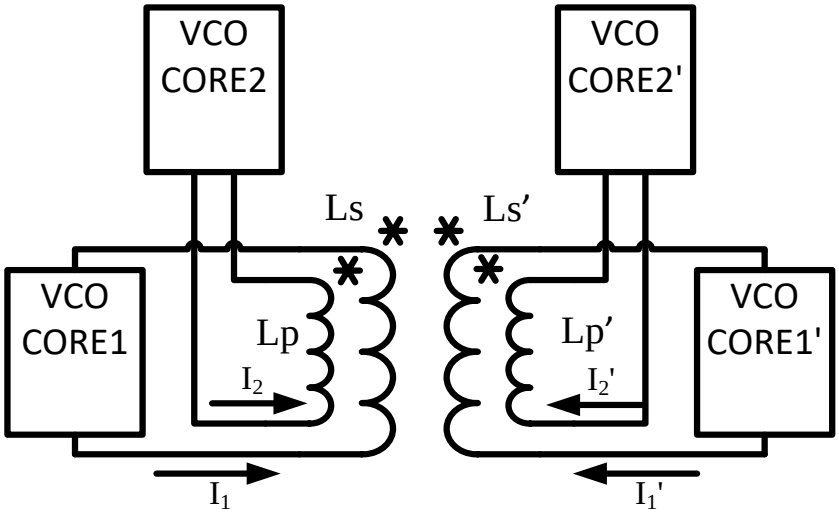


Fig. 3.1 The diagram of proposed oscillator.

The proposed structure allows frequency getting output from any of the four VCO cores. Since core1 and core1' have identical inductor geometry, they contribute to the same frequency band. Similarly, core2 and core2' contribute to another frequency band. Hence, two distinguished frequency bands can be achieved by switching either core1 and core1' pair or core2 and core2' pair on.

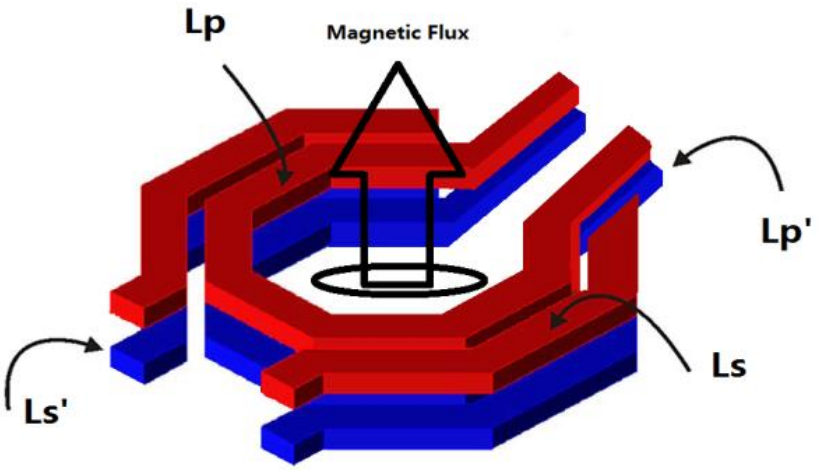


Fig. 3.2 The 3D drawing of the proposed transformer.

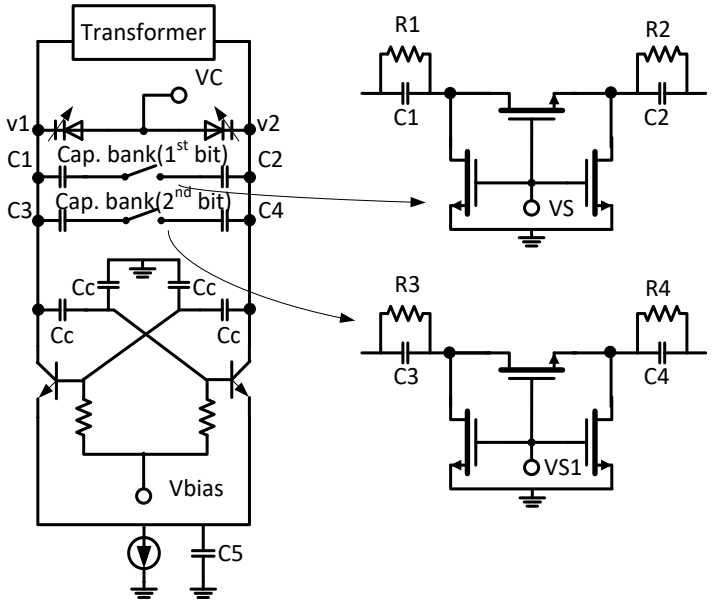


Fig. 3.3 The schematic of proposed VCO core..

Furthermore, since mutual inductance between the transformer wings can be varied by switching the capacitance in coupling cores within the same pair, tuning range can thus be further enhanced. By overlapping the transformer wings, magnetic coupling is maximized, which leads to the enhanced mutual coupling effect. There is weaker coupling between the core1/core1'

and core2/core2' pairs. The space between inner and outer coils is intentionally increased to weaken the coupling factor out of pair. To avoid overlapping of frequency tuning, it's recommended that the two pairs should not be turned on simultaneously and further to avoid phase noise degradation due to eddy effect.

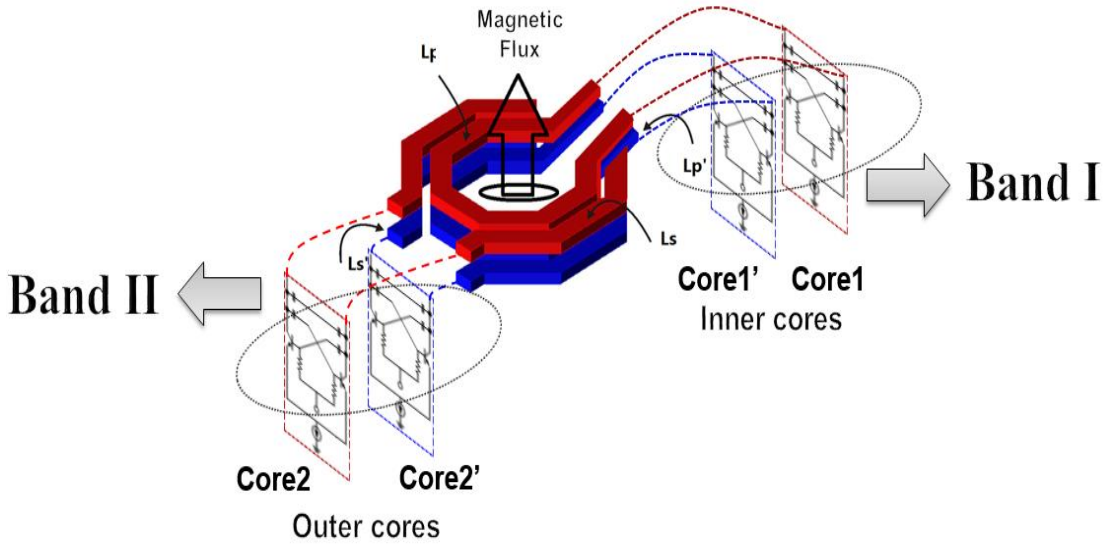


Fig. 3.4 The entire view of transformer-based oscillator

The schematic of transformer-based VCO core is shown in Fig. 3.3. It consists of cross-coupled BJT pair for –gm generation. Frequency tuning of the core is achieved by tuning the varactor as well as switching two control bits of the capacitor arrays. All cores share the similar structure, and the cores in an overlapped transformer pairs have the identical circuits.

This design uses SiGe HBT for -gm stage due to its lower noise and higher gm efficiency. Capacitors Cc are used on the cross-couple path to allow separate biasing for the bases of the HBTs and to reduce its voltage swings through the capacitor dividers. Capacitor C5 is used to weaken the dc noise up-conversion by 2nd order harmonics caused by the current tail. The value of C5 is carefully chosen to provide phase shift [5] on the noise signal generated by the current tail such that it's off the zero-crossing of the oscillation signal. This approach minimizes the

phase noise due to the current sources. The switch for capacitor array consists of one switching and two pulling down NMOS transistors, as well as the resistors across the capacitors to prevent the voltage from floating at source and drain of the switching transistor when it is turned off.

What is more, the entire view of transformer-based oscillator is shown in Fig. 3.4, where the band I servers for a higher frequency band and the band II servers for a lower frequency band.

3.1.2 Signal Strength Enhancement for Phase Noise Reduction

A Transformer coupling not only enhances the tuning range, but also benefits the phase noise reduction. The proposed VCO has two operational modes corresponding to turning either one core or two cores on. In the 1st stand-alone mode, only the main oscillation core is turned on. In the 2nd coupling mode, both the main core and the coupling core (inner pair or outer pair) are turned on. In the 1st mode, the power consumption is relatively low, but suffers from higher phase noise. In 2nd mode, the coupling working mechanism improves the phase noise and form the loop of signal boosting as introduced in chapter 2 Fig. 2.3, where m and m' can be re-write as

$$m = I_{c1}/I_1 \approx M/L_1 \quad (3.1)$$

$$m' = I_{c2}/I_2 \approx M/L_2 \quad (3.2)$$

where M is mutual inductance and equal to $M = k\sqrt{L_1 L_1}$,, while k is the coupling factor. If k is close to 1, around 5dB phase noise improvement can be achieved by burning extra power consumption.

3.1.3 The Mechanism of Frequency Tuning Range Augment

This technique is introduced in chapter 2. By substituting design parameters of band I into Eq. (2.8), the tank impedance is estimated in Fig. 3.5. It is shown that about 200MHz frequency tuning can be achieved by switching the capacitor array control bits of the coupled tank.

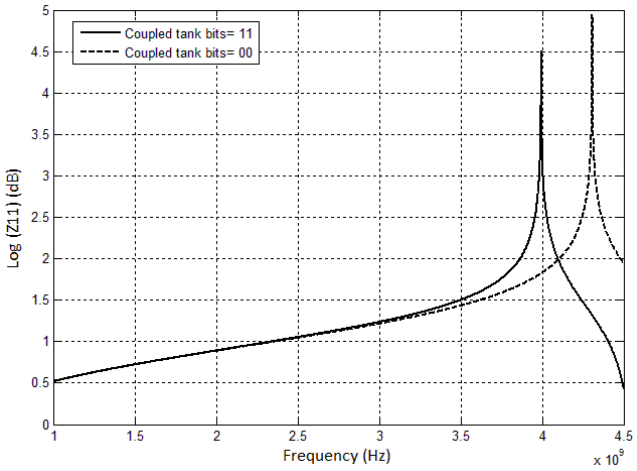


Fig. 3.5 Simulated additional frequency tuning caused by capacitor array control bits of the coupled core.

In addition, the summary of the main band and its sub-band frequency are listed in table 3.1. As shown in table 3.1, only cores in a pair have effect on each other's frequency tuning, and the frequency range can be expanded by switching the bits of paired tank. Although bias current also has effect on frequency tuning, it is not recommended to use it since it affects the phase noise.

Table 3.1: Frequency Bands

Band	**Output**	**Core1 bits**		**Core1' bits**		**Core2 bits**		**Core2' bits**		**Freq.**
Band I	Core1	0	0	0	0	/	/	/	/	High
		0	1							
		1	0	1	1	/	/	/	/	
		1	1							
	Core1'	0	0	0	0	/	/	/	/	
				0	1					To
		1	1	1	0	/	/	/	/	
				1	1					
Band II	Core2	/	/	/	/	0	0	0	0	
						0	1			Low
		/	/	/	/	1	0	1	1	
						1	1			
	Core2'	/	/	/	/	0	0	0	0	
								0	1	
		/	/	/	/	1	1	1	0	
								1	1	

3.1.4 Transformer Design

The transformer is based on four differential inductors. Ls and Ls' are outer inductors coils with one turn for high frequency bands, while Lp and Lp' are inner inductors made of 3 turn coils for lower frequency bands. Each pair is designed with the same vertical dimensions using different metal layers for coupling purpose. Ls and Lp are fabricated with top metal layer (metal 6) which has thickness of 2.92 μm, and metal 5 was used for crossing and under interconnection of upper inductors. Ls' and Lp' are fabricated with lower metal layer (metal 3), which has thickness of 0.5μm, and metal 2 and metal 4 were used for its interconnection. Due to different metal thickness, Ls' and Lp' have inductance which is smaller than Ls and Lp. This topology avoids frequency overlapping in the wide frequency range. In addition, oscillation frequencies of the two bands are separated from each other in order to minimize their mutual coupling effect.

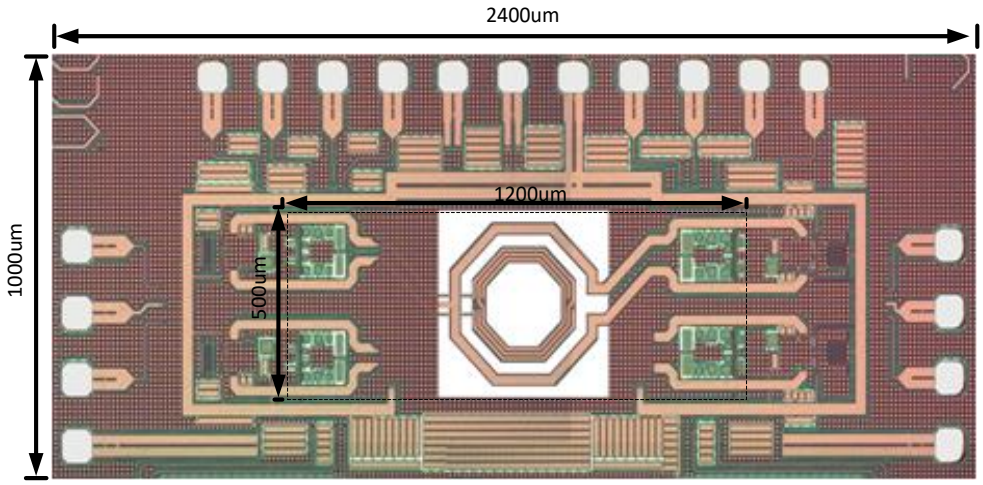


Fig. 3.6 Die photo of the proposed transformer-coupled VCO.

3.1.5 Measured Results

The prototype of this transformer coupled dual band frequency generator RFIC is implemented in a 0.18μm SiGe BiCMOS process. The VCO core consumes 23/42mW for band I stand-alone and coupling operation modes, and 7/13mW for band II stand-alone and coupling

operation modes. The die photograph of the RFIC is shown in Fig. 3.6 with total area including bond pads of 1.0x2.4 mm2. The VCO core area is 0.5x1.2mm2, and the rest of area is occupied by tuning logic, buffers, etc. Table 3.2 summarizes the performance of this work and compares with previous wide tuning range VCO designs using other techniques. The equations used to evaluate figure-of-merit FoM and FoM_T are expressed as

$$FoM = 10log\left[\left(\frac{f_0}{\Delta f}\right)^2 \frac{1mW}{P}\right] - \mathcal{L}(\Delta f)_{m,s} \tag{3.5}$$

$$FoM_T = FoM + 10log\left[\frac{TR(\%)}{Vtune}\right]. \tag{3.6}$$

Phase noise measurements were performed using an Agilent E4446A spectrum analyzer with phase noise measurement option. The phase noise is measured as 114.8/120.45 dBc/Hz for band I and -115.8/121 dBc/Hz for band II at 1 MHz offset. As shown in Fig. 3.7, the coupling mode has 5.6 dB phase noise improvement comparing to the phase noise measured in its stand-alone mode.

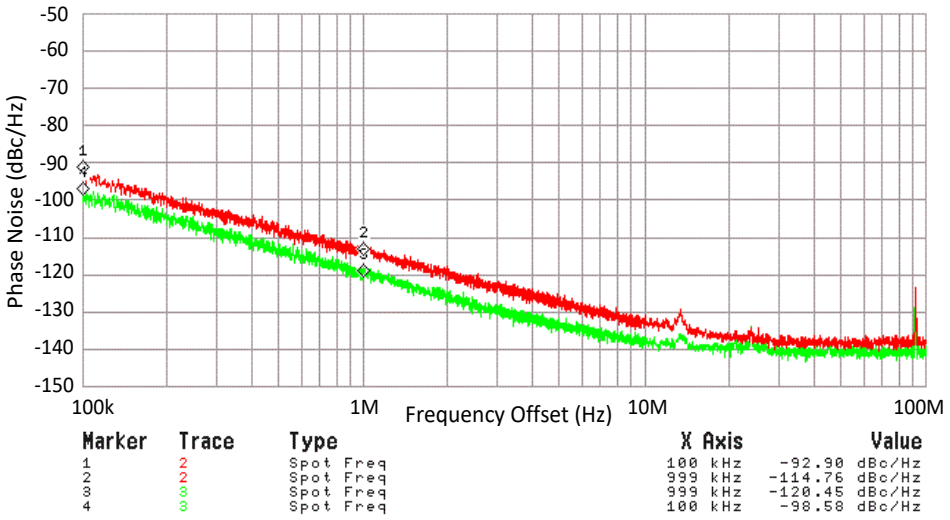


Fig. 3.7 Measured frequency tuning range vs. capacitor control bits of all cores.

The measured frequency tuning range containing all the bands is shown in Fig. 3.8, in which frequencies between each tuning bit are smoothly covered by varactor tuning (shown in Fig. 3.9). The band I achieves 32.7% tuning range, covering frequency range from 3.09 GHz to 4.3 GHz. The band II has 30.1% tuning range that covers frequency range from 1.58GHz to 2.14GHz. The frequency jump from band I and band II are about 200 MHz and 100 MHz respectively. Those sub-bands are labeled as band 1 and band 2. As shown, frequency tuning range is enhanced by switching capacitor arrays of both main core and coupling core.

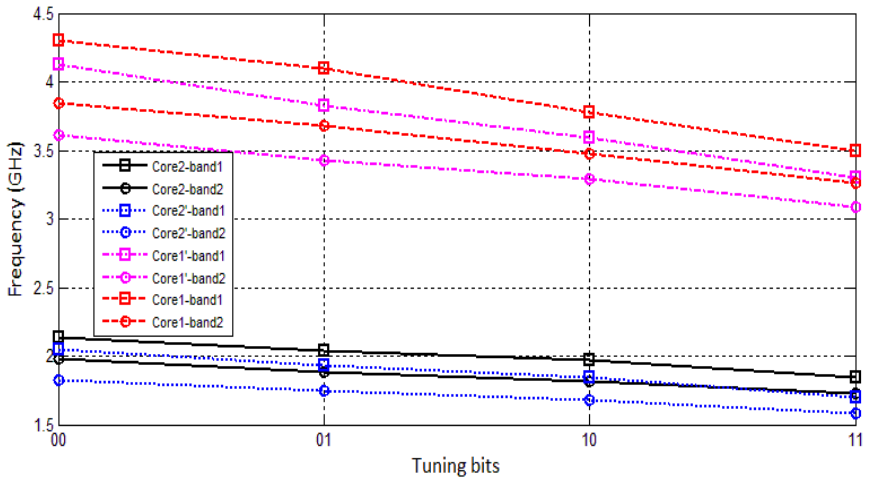


Fig. 3.8 Measured frequency tuning range vs. capacitor control bits of all cores.

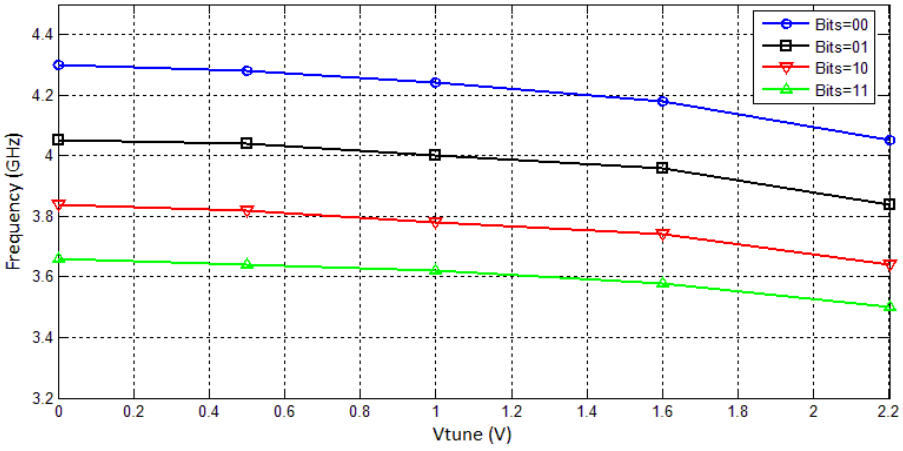


Fig. 3.9 Measured frequency tuning range vs. capacitor control bits of all cores.

3.1.6 Conclusions

A wide-band transformer coupled VCO with phase noise reduction is presented. By using compact transformer structure, the area of inductors is greatly reduced by almost 3 times which occupying only 0.6 mm2. However, since the metal layers below top metal are too resistive in the implemented fabrication process, the transformer is suffering from large Q degradation, which leads to higher power consumption and poorer phase noise as shown in measurement, therefore only function and concept were proved in this letter. Fortunately, there are some foundries supporting 3 top metal layers, which can be good candidate to implement proposed structure in the future

Table 3.2: Performance Summary and Comparison of QVCOs with Different Coupling Techniques

Parameter	[9]	[16]	[8]	This work
Structure	8-shape coil Transformer	Switching Cap/core	Switching Inductor	TBDBVCO
Technology	65 nm CMOS	130 nm CMOS	65 nm CMOS	180 nm SiGe
Power Supply(V)	0.4	1.2	/	2.2
Frequency (GHz)	2.4~3.6 3.4~5.3	3.14~5.2	57-65.5	1.58~2.14/ 3.09~4.3
Relatively Tuning Range	75%	49.4%	14.2%	30% / 32.7%
Power (mW)	4.4~6	2.5~9.2	6	1st mode 7/22
				2nd mode 13/43
Phase noise (dBc/Hz)	-139~-149 @10 MHz offset	-119 ~-114.9 @ 1 MHz offset	-110.8 @ 1 MHz offset	-115.8/-114.7 @ 1 MHz offset
				-121/-120.5 @ 1 MHz offset
FoM (dBc/Hz)	187~189	179.3~184	-176.2	175.8/175.5
FoM_T (dBc/Hz)	/	195.5	-179.3	184.1 184.2

.

3.2 A Low Phase Noise 8.8 GHz VCO Based on ISF Manipulation and Dual-tank Technique

3.2.1 Introduction

Since high frequency clock is increasingly in demand on radar, optical, high-speed communication and these emerging applications, the oscillator with high purity is urgently required in those frequencies. As known, as frequency goes higher, the oscillator design is getting harder, because that fabrication process is limited and the circuit is more sensitive to both noise and parasitic components. In the conventional LC tank VCO design, the phase noise is mainly determined by 1) the quality factor Q of LC tank, 2) cyclostationary noise from cross-coupled transistors, 3) flicker noise from tailed transistors, 4) ISF function which is always determined by the structure. Unfortunately, most of above factors are more challenging on high frequency VCO design. For example, low quality factor of tank is always an issue as frequency goes higher, not only because the trade-off between inductor's geometry and its parasitic components, but also Q degradation is more serious from active devices. Since Q is lower, decreased paralleled resistance requires larger –gm value to compensate. Therefore, cross-coupled and tailed transistors that together determined –gm are pushing VCO into noisier working condition, and this means more cyclostationary noise and flicker noise are induced to the output node. In addition, ISF function manipulation is not always a good choice in high frequency, since, in most case, feedback and more components are needed, therefore it always increases the design complexity and adds extra noise sources.

To overcome above limitations, this paper presents a novel VCO combined both dual-tank structure and ISF manipulation technique, and can optimize high frequency VCO in following

major aspects: 1) dual-tank structure reduces Q degradation from cross-coupled transistor by separate voltage swing control of drain and gate, which decrease operation time in triode region. In addition, it creates an equivalent tank that can operate at twice frequency comparing to single tank. 2) ISF manipulation reshapes the tailed current and half the tail transistors' noise by feedback. Thus, it changes the transfer function of cross-coupled transistors and makes them operate with least noise. Therefore, low phase noise is achievable by the proposed structure.

3.2.2 The Architecture of the Oscillator

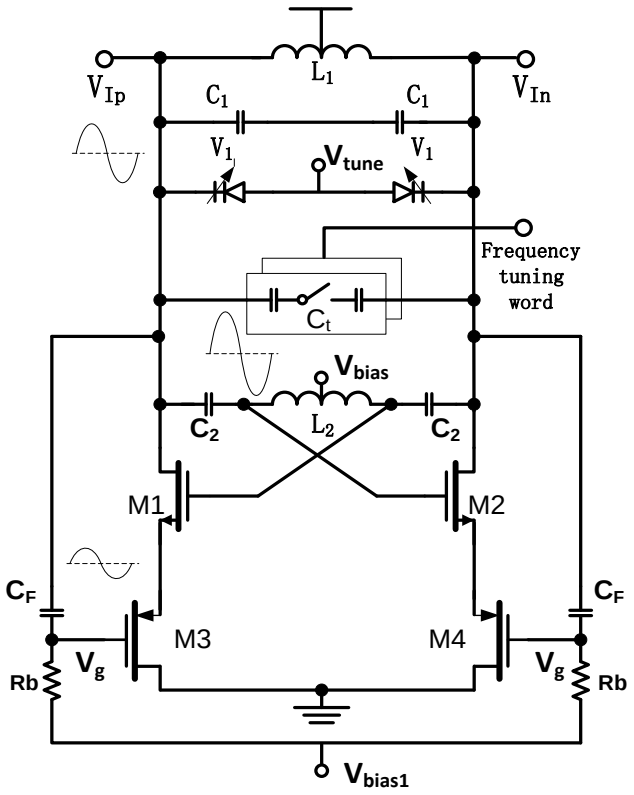


Fig. 3.10 Schematic of 8.8GHz VCO.

Fig.3.10 shows the schematic of the proposed VCO. L_1 and L_2, which are differential inductors, together with C_1 and C_2 form the dual-tank structure. This allows that the swing of gate and drain voltages can be separated for phase noise optimization. Different from conventional one NMOS transistors current tail, two PMOS (M_3 and M_4) provides tail current.

They not only have less flicker noise, but also provide a small resistance path to the ground, thus shut part of the output noise. What's more, C_F and R_b provides feedback path from outputs to the gate of M_3/M_4 and allows dynamic biasing for M_4 and M_3 and optimization on ISF with least added components and noise sources, and V_{bias1} provides DC bias for M_3 and M_4. Including giving DC value for M_1 and M_2, V_{bias} can also be used to optimize noise from M_1 and M_2. C_t is capacitors bank for frequency coarse-tuning, while V_1 is the varactor for fine-tuning. In addition, the signal strength at different nodes is also illustrated, and this will be discussed later.

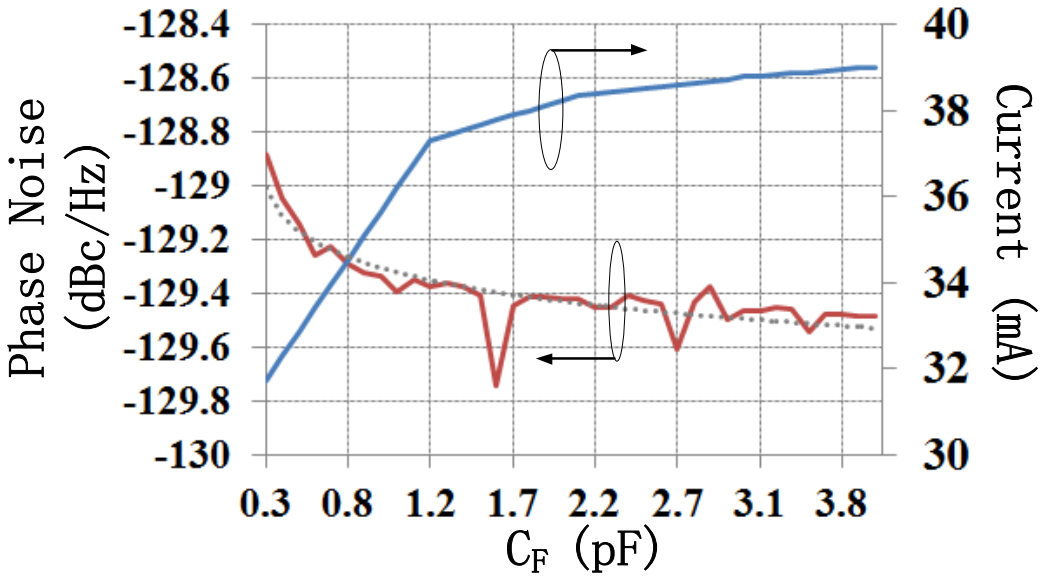


Fig. 3.11 Simulated results of C_F value versus both current and Phase noise.

3.2.3 Noise Reduction Technique

As mentioned, the phase noise is optimized by two techniques: ISF manipulation and dual-tank. The former one is implemented by two steps. First, the conventional single tail NMOS transistor is replaced with two PMOS transistors. This way, the noise current of cross-coupled transistors will see the low impedance through PMOS to the ground, thus the noise going to the output is reduced during equilibrium condition. In the conventional single-transistor tail, the

second harmonic is present at the common node of the cross-coupled transistors; therefore, its noise will be converted to the close-in noise of the output signal.

Furthermore, because of the feedback, the behavior of tail transistors $M_{3/4}$ follows the behavior of their respective branch transistors $M_{1/2}$, and that one of the tail transistors will turn off during the half oscillation cycle. Therefore, the noise from tail transistors is largely suppressed. In other words, the noise modulation function (NMF) is almost reduced in half, which leads to smaller ISF_{eff}.

For the dual-tank technique, it optimizes phase noise by reducing triode region operation time for M_1 and M_2. Here needs to be clarified that this optimization is different from feedback mechanism, because that the feedback technique is to reduce equilibrium time when noise is highest and transistors are not necessary be in triode region during equilibrium, and dual-tank is to reduce triode region time during equilibrium.

In addition, it needs to be cautioned that the C_F, which determines the feedback strength, can neither be too small or too large. If it is too small, the phase noise will suffer. If it is too large, it only occupies the area of the die without improving performance. Therefore, to have the best trade-off value of $C_{F,}$ we plot the phase noise and current versus C_F (Fig. 3.11). As shown in Fig. 3.11, after C_F larger than 1.2 pF, though current is increasing as C_F increase, the FoM is almost keeping constant. It is also worth noting that since the drain swing is reduced, the feedback from C_F is weakened; therefore, a larger C_F may be required. Moreover, additional optimization can be implemented by setting the DC level of V_{bias} away from Vdd; thus, the triode region time can be further reduced, and the excess noise factor can also be minimized at the same time due to the reduced overdrive voltage.

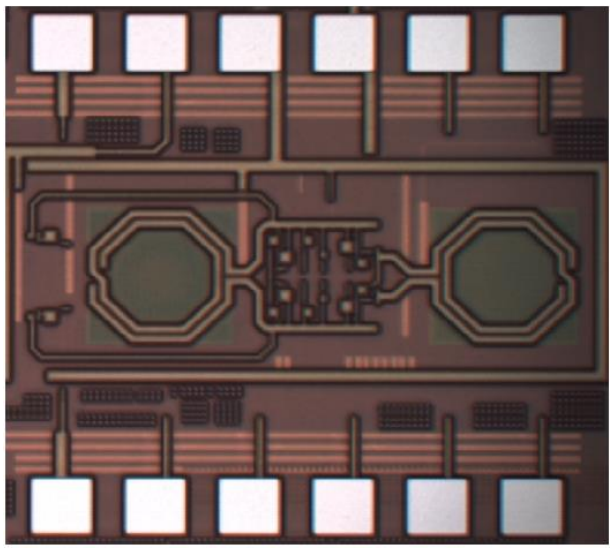


Fig. 3.12 Die photos of the implemented 8.8 GHz VCO.

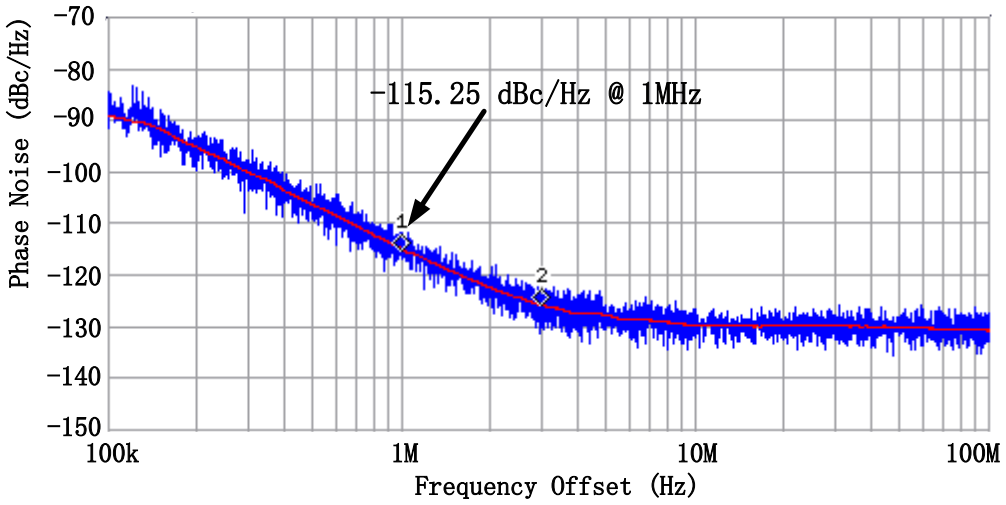


Fig. 3.13 Measured phase noise at 8.79 GHz.

3.2.4 Measurement Results

The prototype of the dual-tank and ISF-manipulation-based high-frequency clock generator MMIC is implemented in a 0.13μm BiCMOS process. The proposed circuit consumes 80-100mW of power from a 2.5V power supply. The die photograph is shown in Fig. 3.12 with a total area (including bond pads) of 1.0 x 1.0 mm^2. The VCO area is 0.83 x 0.35 mm^2, and the rest

of the area is occupied by the bias circuit, buffers, etc. Table 3.3 summarizes the performance of this work and compares it with the previous high-frequency VCOs that utilize other techniques.

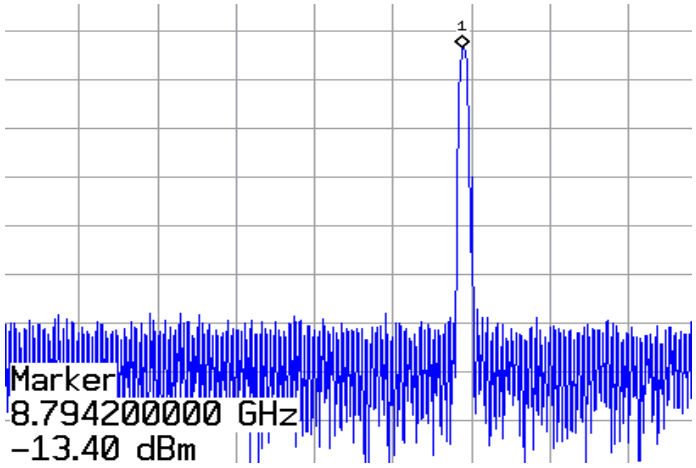


Fig. 3.14 VCO output spectrum measurement result.

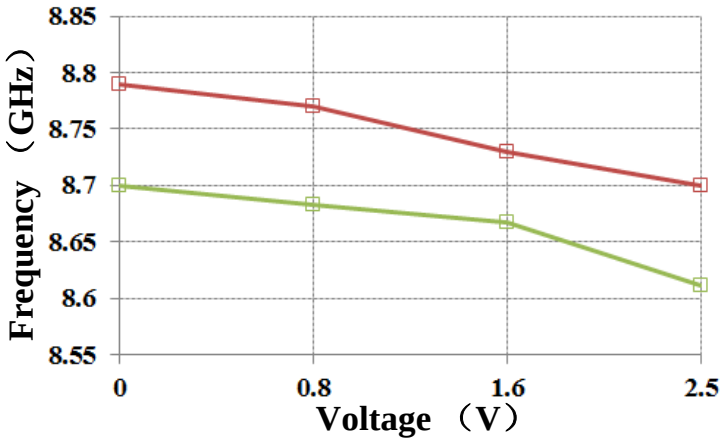


Fig. 3.15 Measured tuning frequency versus voltage.

Phase noise and output frequency measurements were performed on the E4440 Agilent spectrum analyzer by using the phase noise measurement option. The phase noise is measured as -115.25 dBc/Hz at 1 MHz offset (Fig. 3.13), and the measured frequency is 8.79 GHz with an output power of -13.40 dBm (Fig. 3.14). The measured frequency tuning range using only the capacitor bank and the varactor with constant DC bias point is shown in Fig. 3.15. Also, the phase noise versus frequency @ 1MHz offset in one tuning band is plotted in Fig. 3.16.

3.2.5 Conclusion

A novel high-frequency VCO structure is designed and fabricated. The operating center frequency is 8.8 GHz with 4 percent tuning range. By implementing both the dual-tank structure and the ISF manipulation technique, the phase noise is greatly optimized by reducing noise and minimizing Q degradation from both the tail and the cross-coupled transistors; achieving phase noise of -115.23 dBc/Hz and FoM of 175 dBc/Hz at 1MHz offset.

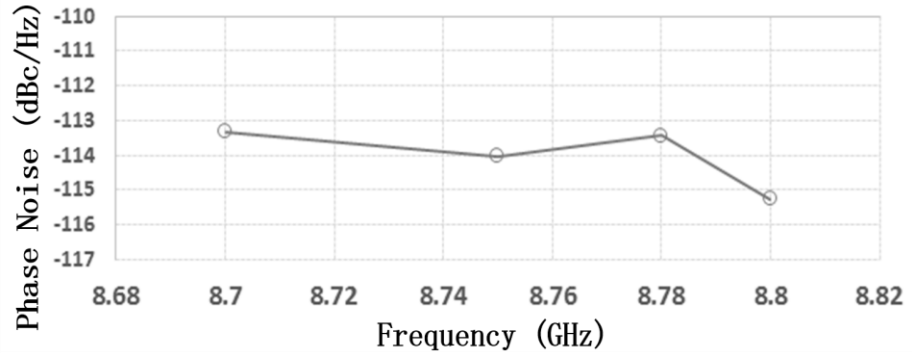


Fig. 3.16 Measured tuning frequency versus phase noise in one frequency band.

Table 3.3: Performance Summary of the Implemented VCO and QVCOs

	[17]	[18]	[19]	**This work**
Technology	250nm CMOS	130nm CMOS	Si	130nm BiCMOS
Power Supply (V)	2.5	1	3	2.5
Frequency (GHz)	3.7	43	9.2	8.8
Frequency Range	23%	4.2%	22%	4%
Power(mW)	7.5	7	24	80
Phase noise (dBc/Hz) @1MHz	-117	-90	-116.2	-115.25
FoM(dBc/Hz)	179.6	174	181.6	175

Chapter 4 Design Methodology of Coupled-Oscillator System

4.1 Introduction

As mentioned in the first chapter, the emerging technologies such as N-path filters, phased array antennas, interleaved data converters, and sub-harmonic mixers escalate the need for multi-phase clock generation circuits. Additionally, as the number of phases of the clock generator increases, certain side benefits are achieved; e.g., less harmonic distortion for the N-path filter. Therefore, an efficient and expandable solution to generate a multi-phase clock is of utmost importance. However, most conventional multi-phase clock generation mechanisms are not suitable candidates. For example, the delay-cell-based ring oscillator has poor phase noise, and is not qualified for gigahertz and mm-wave applications.

Furthermore, the ploy-phase-filter-followed structure is narrow-band, and cannot meet the requirements of today's Software-Defined Radio (SDR). Additionally, the frequency-divider-based clock generator requires an oscillator with N times higher operating frequency, and while it could still be a valid candidate for lower gigahertz applications, it will increase the design complexity and power consumption as the number of phases and operating frequency increase. With the above in mind, the coupled oscillator architecture is a potential candidate for multi-phase clock generation.

This chapter presents general concepts and concerns in coupled-oscillator design, such as phase noise, phase shift and start-up condition, and their comparisons to single oscillator design. Along with those thoughts, different coupling mechanisms will be introduced as well as some proposed structures. In addition, it's going to present grafting proposed coupling mechanisms on those high-performed techniques in single oscillator designs and give discussions on them with the help of behavior and analytical model.

Finally, the Adler's equations will be introduced. Based on that, the analytical equations of phase noise, phase error and phase shift on four-core system are derived.

4.2 Phase Noise for Multi-Phase VCOs

4.2.1 General Concepts

As mentioned earlier, regardless of the degradation caused by coupling, if number of oscillator cores (*N*) increases in the coupling system, the overall oscillator phase noise will be improved by $10\log_{10} N$. However, in some cases, the degradation on phase noise caused by coupling can easily exceed the improvement of the phase noise from $10\log_{10} N$. Especially for the two cores cases, only 3dB headroom is left for the phase noise degradation from coupling.

The phase noise degradation from coupling can be caused by coupling components and coupling mechanisms. In fact, the degradation caused by coupling components is relatively smaller than the latter and can be easily avoided. Since the root cause of such degradation is extra noise sources, none-active coupling strategies and high Q coupling components can be utilized to mitigate it.

The phase noise caused by coupling mechanisms is ISF related. In other words, the phase and amplitude of the coupling signal are important, and they are determined by coupling paths.

4.2.2 Trade-off between Phase Noise and Coupling Strength

In most coupled-oscillator system, the phase of the coupling signal which is injected from another core is determined by the number of cores (N), and equals to π/N in ideal case. Because of that, the amplitude of the coupling signal determines both phase noise and coupling strength, and creates trade-off between them. Take the conventional a capacitive coupling QVCO (CC-QVCO), which is shown in Fig. 4.1, as example, the peak of the coupling is aligning with the zero-crossing point of the output. $V_{g,coupling}$ is from the coupling signal and presenting at the gate of the being coupled core, and equal to $mV_{In}/(1+m)$, where $m = \frac{C_{PC}}{C_2}$. Therefore, the

stronger the coupling strength is the larger $V_{g,coupling}$ is, however, the more the coupling signal is interrupting the phase of the output, resulting in worse phase noise.

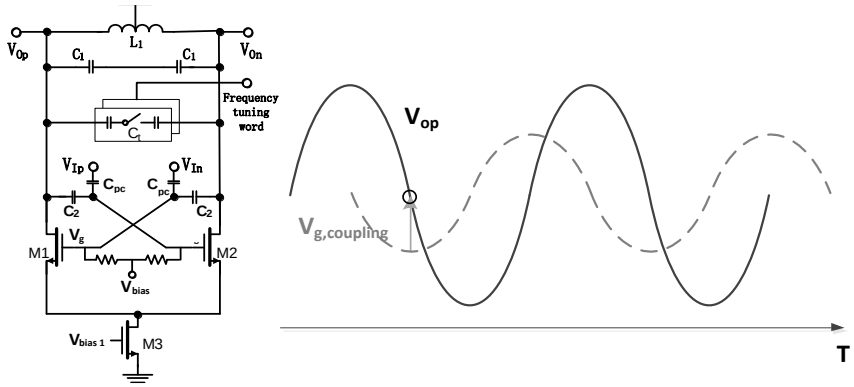


Fig. 4.1 A generic CC-QVCO and waveforms of its output and coupling signals.

This phenomenon can also explained by the modified Lesson's equation:

$$L(\Delta\omega) = \frac{KTr_p}{V_0^2(1+m)^2}\left(1+\left(\frac{m}{1+m}\right)^2\right)\left(\frac{\omega_0}{Q\Delta\omega}\right)^2 \tag{4.1}$$

Fortunately, the trade-off between coupling strength can be more relieved as number of coupling cores is increasing. As shown in Fig. 4.2, the coupling signal moves towards the peak of the output signal as number of cores increases, therefore it degrades less on phase noise.

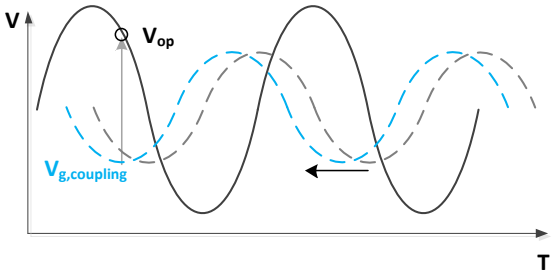


Fig. 4.2 Illustration of the motion of the coupling signal $V_{g,coupling}$ as number of cores increases.

By re-writing Eq. (4.1), the general equation can be obtained as

$$L(\Delta\omega) = \frac{KTr_p}{V_0^2\left(1+m\cos\left(\frac{360}{2N}\right)\right)^2}\left(1+\left(\frac{m\sin\left(\frac{360}{2N}\right)}{1+m\cos\left(\frac{360}{2N}\right)}\right)^2\right)\left(\frac{\omega_0}{Q\Delta\omega}\right)^2 \tag{4.2}$$

4.3 Phase Shift

4.3.1 Conventional Structure

As discussed in the previous chapter, QVCO greatly suffers from the degradation on phase noise due to coupling signal. To address this issue, the extra phase shift can be added to the coupling signal by using phase shift components. The most conventional structure is by adding extra capacitor.

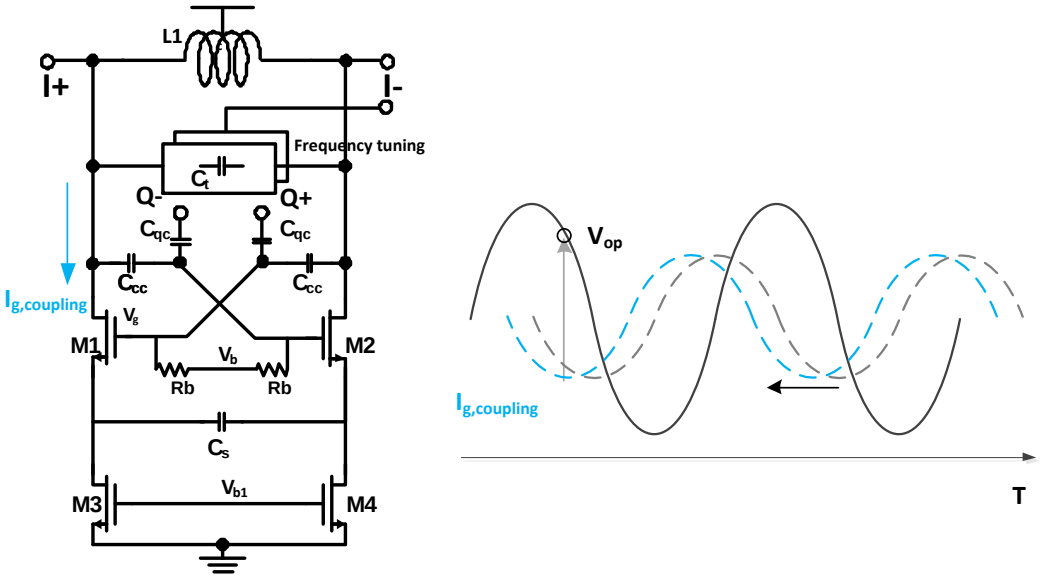


Fig. 4.3 The conventional capacitive coupling structure with phase shift component C_S and the illustration of its shifted coupling current.

As shown in Fig. 4.3, instead of directly shifting the voltage, the coupling current is shifted to a less sensitive point. Therefore, the Lesson's equation can be re-write as

$$L(\Delta\omega)_{QVCO} = 10\log\left[\frac{kTR}{2A_{osc}^2}F_{min,QVCO}\left(\frac{\omega_0}{Q\Delta\omega}\right)^2\right] \tag{4.3}$$

$$F_{min,QVCO} = 1 + \left(\frac{sin\varphi_{gm} + mcos\varphi_{gm}}{cos\varphi_{gm} + msin\varphi_{gm}}\right)^2 + \gamma\left(\frac{cos\varphi_{gm}}{cos\varphi_{gm} + msin\varphi_{gm}}\right)^2 \tag{4.4}$$

where φ_{gm} is phase shift due to C_S.

4.3.2 Capacitive Coupled QVCO with Tunable Cs

In the above presented CC-QVCO, phase noise performance is sensitive to the phase delay that is further affected by oscillation frequency. Since the degeneration capacitance C_S can affect the phase of trans-conductance, we revise the design with a tunable C_S to achieve the best phase noise performance across the entire tuning range.

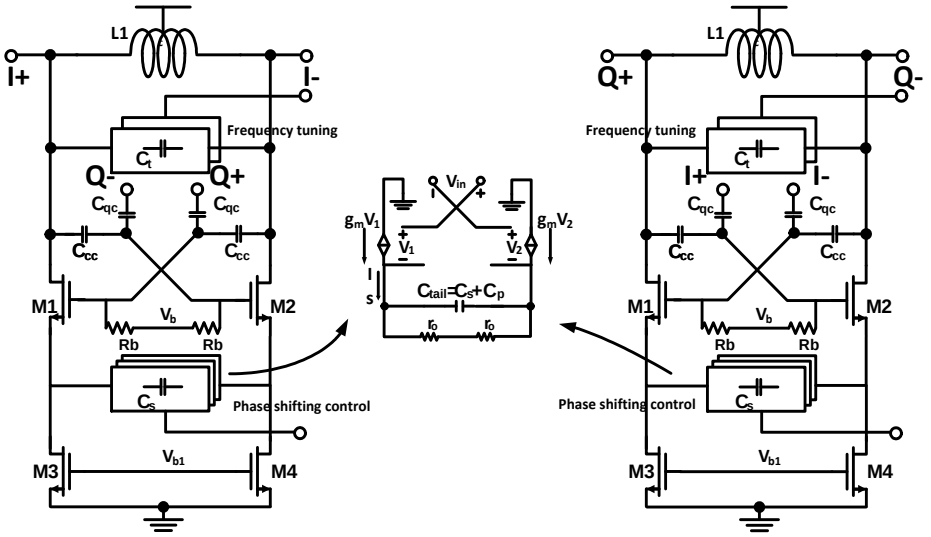


Fig. 4.4 Schematic and equivalent circuits of CC-QVCO with Tunable Cs.

Fig. 4.4 illustrates the schematic and equivalent circuit of the revised QVCO with degeneration capacitor. Assuming the signal of in-phase core is $V_I = V_o \cos \omega t$ and that of the quadrature core is $V_Q = V_o \sin \omega t$, the gate voltage of the oscillation transistor in core-I can be expressed as $V_{I,gate} = [1/(1+m)]V_I + j[m/(1+m)]V_Q$, where the first part is contributed by the core-I itself and the 2nd part is coupled from the core-Q. Thus, the coupling effect from another core contributes a phase shift φ_1 expressed as $\varphi_1 = \tan^{-1}(m)$. Without degeneration capacitor C_S, output current I_s follows the phase of gate voltage V_{gate}. As a result, I_s has a phase difference of φ_1 comparing to its output voltage V_o. This injection, which is off the ideal alignment condition by a phase shift of φ_1, makes the oscillator more sensitive to noise. Adding

C_S, the phase delay of the transconductance of oscillation transistors $\varphi_{gm} = \tan^{-1}(2\omega C_S/g_m)$ is introduced. It is now possible to shift I_s back to its ideal alignment angle with a proper C_S value. In another word, in order to minimize phase noise, φ_1 and φ_{gm} should be equal, which leads to the optimized C_S value expressed as $C_s = \frac{g_m}{2m\omega}$, which clearly shows that the optimized C_S is dependent upon frequency and it provides a design guide to choose the optimize C_S for best phase noise performance across the tuning range.

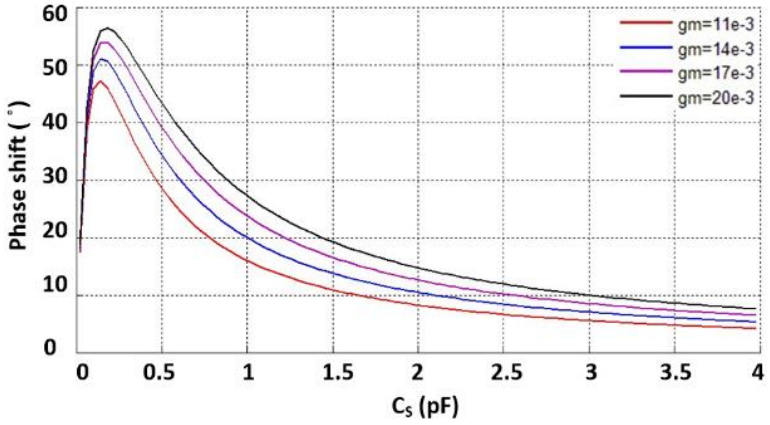


Fig. 4.5 Phase shift vs. Cs under different gm (r_o=1kΩ, frequency=3GHz).

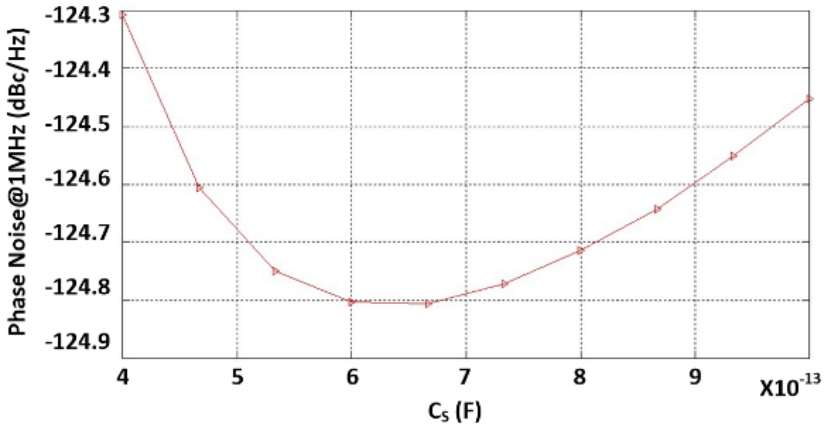


Fig. 4.6 Phase noise versus C_S value.

In Fig. 4.5, we plot the trans-conductance phase shift φ_{gm} versus capacitance value C_S under different g_m conditions. It shows that both C_S and g_m can alter the phase relationship.

Current source output resistance r_o contributes a pole and together with g_m determines the maximum phase angle that can be shifted. Since g_m has to be tuned to overcome the tank loss, it is normally kept as a constant to ensure stable oscillation. On the other hand, r_o is chosen to balance the low flicker noise and the large phase shift. As a result, C_S is most suitable to serve as a tunable parameter for phase shift adjustment.

As shown, phase noise can be minimized by shifting the peak value of noise source current away from the zero-crossing point of the desired output signal. Firstly, all parameters are selected to achieve the desired performance at center of the tuning curve. Secondly, C_S is adjusted to further achieve the optimized phase noise at different oscillation frequency. An example of phase noise reduction by tuning C_S is illustrated in Fig. 4.6.

In Fig. 4.7, phase noise at the center band frequency has been optimized. If C_S is kept constant when frequency is tuned, phase noise optimization effect gradually disappears. By adjusting C_S across the tuning range using a 3-bit tuning control, phase noise optimization remains valid even at the edges of the tuning curve.

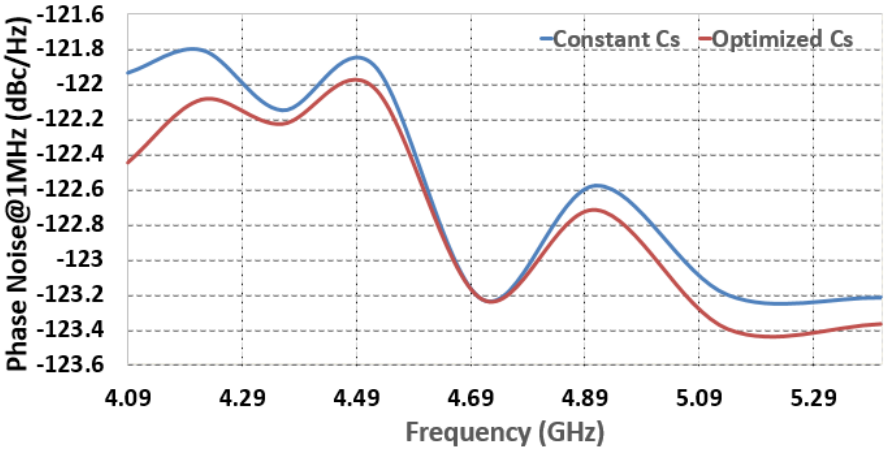


Fig. 4.7 Phase noise over frequency tuning with and without C_S optimization.

4.3.3 Capacitive Coupled N-Phase VCO

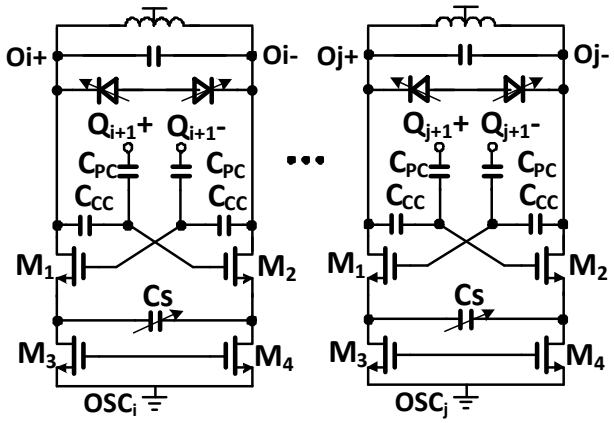


Fig. 4.8 A capacitive-coupled N-phase oscillator and its oscillator cores.

The proposed phase shift technique can be extended to N-phase VCO designs, as shown in Fig. 4.8. The overall phase noise performance of an N-phase CC-VCO can usually benefit from the coupling since its phase noise scales down with the number of coupling stages, but at the cost of N times of the power consumption. The phase noise of an N-phase VCO can be written as $L_N(\Delta f) = L_1(\Delta f) - 10logN$ where $L_1(\Delta f)$ is the phase noise of a single-phase VCO. However, the noise improvement is based on the assumption that the coupling between oscillators doesn't introduce extra noise. Therefore, a noiseless coupling technique such as the proposed capacitive coupling is desirable to achieve the maximum noise benefit from coupling N oscillator stages.

To form an N-phase ring VCO, each core is coupled with its neighbors with 360/2N phase difference between the stages. For an N-phase VCO, the above derived equations can be revised as

$$\varphi_1 = \tan^{-1}\left(\frac{\mathrm{m}\sin\frac{360}{2\mathrm{N}}}{1+\mathrm{m}\cos\frac{360}{2\mathrm{N}}}\right) \tag{4.5}$$

$$\mathrm{C_s} = \frac{g_m}{2\omega}\frac{1+\mathrm{m}\cos\frac{360}{2\mathrm{N}}}{\mathrm{m}\sin\frac{360}{2\mathrm{N}}} \tag{4.6}$$

$$\mathrm{L}(\Delta\omega) = \frac{\mathrm{KTr_p}}{\mathrm{V_0^2}\left(1+\mathrm{m}\cos\left(\frac{360}{2\mathrm{N}}-\varphi\right)\right)^2}\left(1+\left(\frac{\mathrm{m}\sin\left(\frac{360}{2\mathrm{N}}-\varphi\right)}{1+\mathrm{m}\cos\left(\frac{360}{2\mathrm{N}}-\varphi\right)}\right)^2\right)\left(\frac{\omega_0}{\mathrm{Q}\Delta\omega}\right)^2 \tag{4.7}$$

4.4 Embedding of Coupling Mechanisms

By utilizing those advanced techniques in single oscillator designs, it is possible to achieve better performance of the entire system. However, it's going to be extremely tricky, when combining those techniques with coupling mechanisms. That's because that the coupling signal and output signal are not in phase, thus some unexpected interruptions will happen and collapse the performance of the system.

In this section, both embedding of capacitive and inductive coupling mechanisms are going to be briefly introduced, and analytical passive models will be given.

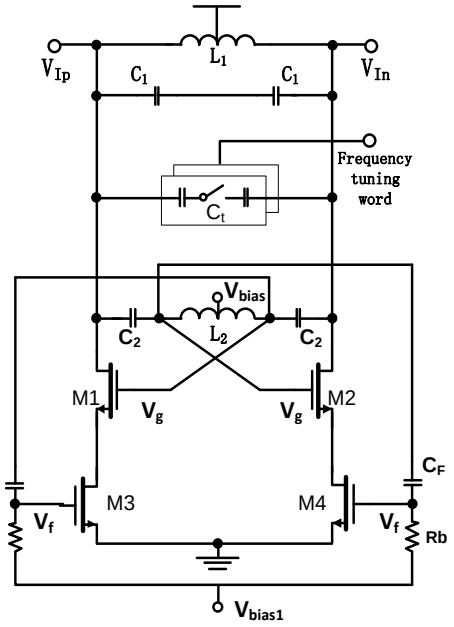


Fig. 4.9 The schematic of the proposed structure with dual-tank and adaptive feedback techniques.

4.4.1 Capacitive Coupling Based Structure

As shown in Fig. 4.9, the structure, which is similar to what we've mentioned in the earlier chapter and uses both dual-tank and adaptive biasing feedback techniques, is taken as an example. To maximize the circuit performance and properly combine the proposed single

oscillator with the capacitive coupling mechanism, two key points should be kept in mind: first, the capacitive coupling shall have the least interaction with the dual-tank structure, and shall not affect the voltage swings on the gate and the drain of the cross-coupled transistors; second, the signal on the feedback path shall always be in phase with the output and not be interrupted by the coupling path in order to keep ISF minimum.

As shown in Fig. 4.10, there exist two candidate coupling points; i.e., V_f and V_g, where j refers to the oscillator core number. In addition, it can be seen that the coupling at Vf is through bottom transistors while it is through cross-coupled transistors for that of Vg.

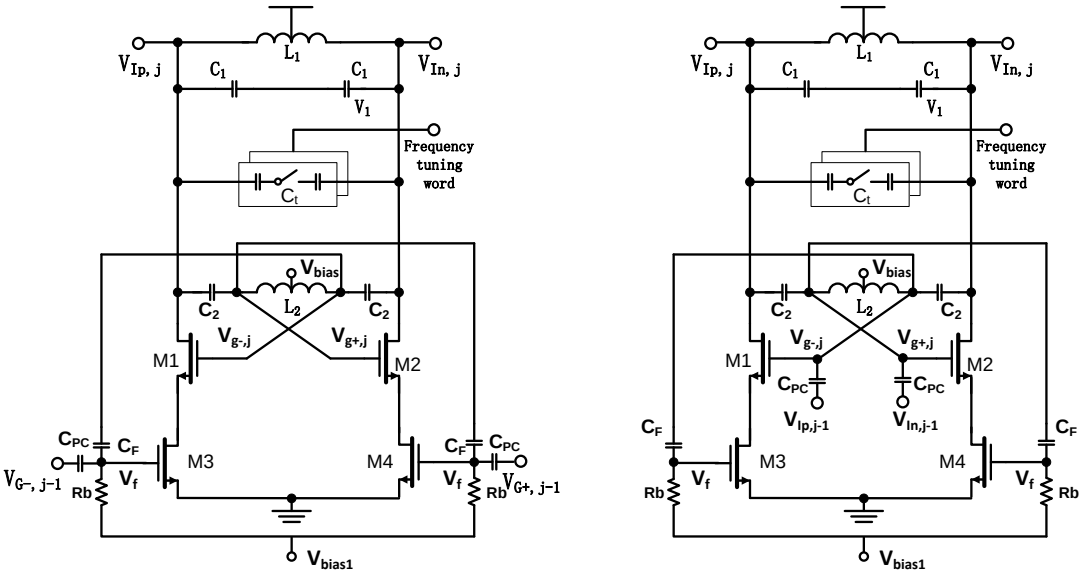


Fig. 4.10 Schematic diagrams of two candidate implementations of capacitive coupling. (a) coupling at node $V_{f\pm,j}$. (b) coupling at node $V_{g\pm,j}$.

Fig. 4.10(a) illustrates the coupling at node V_f. In order to create a coupled signal that is comparable in strength to the signal from the feedback path, the coupled signal is obtained from the gate of the cross-coupled transistors of the adjacent core. However, this kind of coupling will directly interrupt the feedback, and result in phase noise degradation.

Fig. 4.10(b) shows the coupling at node Vg, where the coupled signal is obtained from the output of the adjacent core. However, coupling at node Vg will also interrupt the phase at Vg; therefore, Vg is no longer in phase with the output voltage; resulting in the degradation of the phase noise. Moreover, the coupling strength is a function of the ratio C_{PC}/C_2, which will affect the $G_{g/d}$ of the dual tank. Therefore, it will create a new trade-off between the coupling strength and the ratio of the gate voltage over the drain voltage.

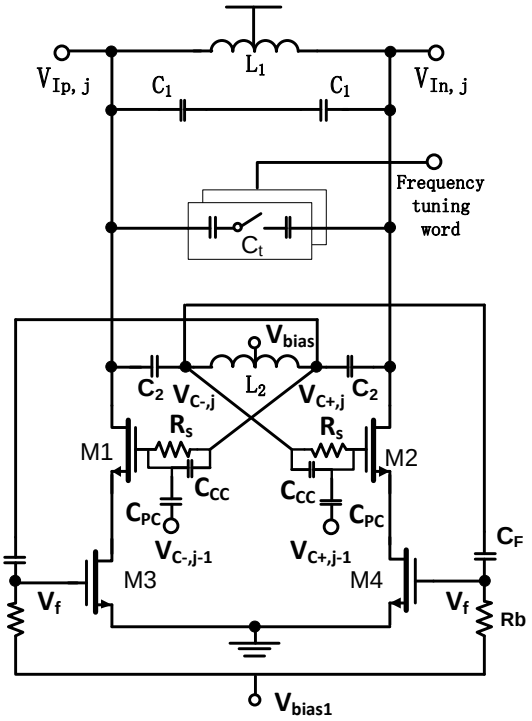


Fig. 4.11 The proposed oscillator architecture with coupling path.

In order to implement capacitive coupling without interrupting the feedback path and the dual-tank, the proposed coupling circuit is further modified. As shown in Fig. 4.11, two capacitors C_{CC} and C_{PC} form the coupling path, and R_S passes the DC voltage from Vbias to M1/M2.

Furthermore, C_{CC} enables M1/M2 to form cross-coupled transistors, which present –Gm impedance to the tank, and maintain the oscillation. Additionally, C_{PC} is the path for coupling the

voltage signal from an adjacent oscillator. The coupled signal is then converted to current by the cross-coupled transistors and injected in the tank. The coupling strength factor, M, is defined as $\mathrm{M} = \mathrm{C}_{PC}/\mathrm{C}_{CC}$, which also represents the ratio of the injection signal to the self-resonance signal.

The proposed structure fulfills our goals in two aspects: first, $\mathrm{C_{CC}}$ prevents direct coupling to the two sides of inductor L_2; thus, Vc remains in phase with the output. Second, the voltage swing of various nodes in the dual tank is affected by the total capacitance $\mathrm{C_{tot}} = \mathrm{C_{CC}}//\mathrm{C_{PC}}$; therefore, the coupling strength and $\mathrm{G_{g/d}}$ are not interacting with each other if $\mathrm{C_{tot}}$ is a constant.

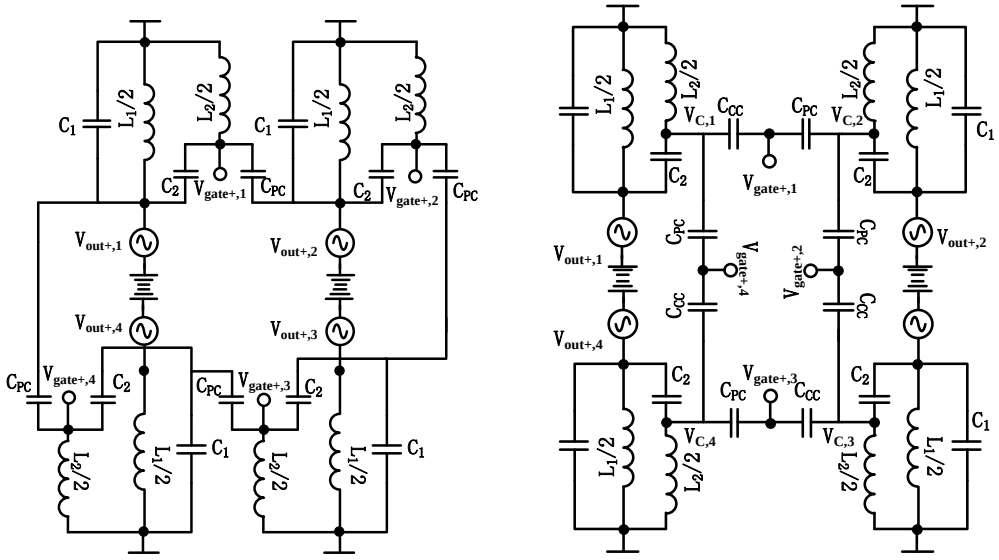
4.4.2 Passive Models of Capacitive Coupling Structure

The capacitive coupling paths among the four tanks are shown in Fig. 4.12, where only one branch of the differential structure is illustrated in order to facilitate the analysis. Figure 4.12(a) represents the coupling paths in Fig. 4.10(a), while Fig. 4.12(b) exhibits that of Fig. 4.10(b). Both Figs. 4.12(a) and 4.12(b) are shown side-by-side in order to demonstrate the coupling implementation discussed in section A, and provide further details. As shown in Fig. 4.12(a), the gate voltage $\mathrm{V_{gate,j}}$ of the cross-coupled transistors has two sources: the first source $V_{out+,j}$ comes from its own tank through C_2, and the second source $V_{out+,j+1}$ is from the adjacent core through $\mathrm{C_{PC}}$. Therefore, the gate voltage is equal to

$$V_{gate,j} = (1/(1+M))G_{g/d'}V_{out+,j+1} + (M/(1+M))G_{g/d'}V_{out+,j} \tag{4.8}$$

where $M = \mathrm{C_{PC}}/\mathrm{C}_2$ is the coupling strength factor, and $G_{g/d'}$ is the re-defined ratio of the gate voltage over the drain voltage, and is equal to

$$G_{g/d'} = \frac{(\frac{L_2}{2})/(1-\omega_0^2 L_2 \mathrm{C_{PC}})}{(\frac{L_2}{2})/(1-\omega_0^2 L_2 \mathrm{C_{PC}}) - 2/(\mathrm{C}_2\omega_0^2)} \tag{4.9}$$



(a) (b)

Fig. 4.12 Equivalent circuit of the coupling path.

Since the feedback signal is also directly obtained from $V_{gate,j}$, the voltage on the feedback path is obviously not in phase with $V_{out,j}$. Therefore, the phase of the injected current to the bottom transistor will move to a point which is more sensitive to noise. In addition, based on (2) and (3), C_2 and C_{PC} which are a function of the dual-tank system, determine the coupling strength M; thus, increasing the design complexity. This leads us to use the proposed structure in Fig. 5.9 (b). As shown in Fig. 5.9(b), the gate voltage is separated from the feedback, and is still equal to (2); however, the coupling strength factor M is modified to C_{PC}/C_{CC}. The feedback signal is now obtained from $V_{C,j}$, which is in phase with the output voltage $V_{out,j}$. Now, $G_{g/d'}$ in (3) is re-defined as follows:

$$G_{g/d'} = \frac{(\frac{L_2}{2})/(1-\omega_0^2 L_2 C_{tot})}{(\frac{L_2}{2})/(1-\omega_0^2 L_2 C_{tot}) - 2/(C_2\omega_0^2)} \tag{4.10}$$

where C_{tot} is equal to $C_{PC}//C_{CC}$. Therefore, C_2 and C_{tot} are only a function of the dual tank in the proposed circuit. In other words, if C_{tot} is a constant, M and $G_{g/d'}$ are not related. Therefore,

C_2 and C_{tot} are only a function of the dual tanks. In other words, if C_{tot} is a constant, M and $G_{g/d'}$ are not related, as show in Fig. 4.13, where, as M increases, the voltage ratio $G_{g/d'}$ of the proposed capacitive coupling structure is kept mostly constant, while that of the conventional capacitively-coupled structure is decreasing

In order to visualize the relationship among $G_{g/d'}$, oscillation frequency, and C_{tot}, the simulated results are plotted in Fig. 4.14. As shown in this figure, it is clear that both $G_{g/d'}$ and the oscillation frequency of the tank will decrease as C_{tot} increases.

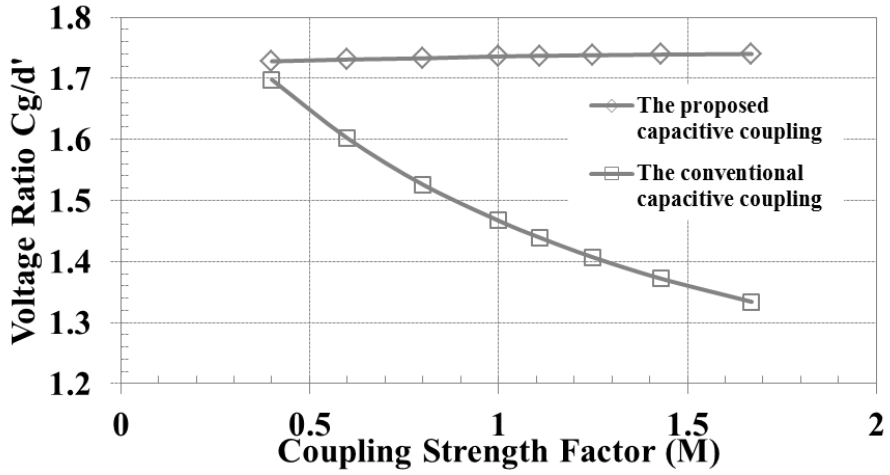


Fig. 4.13 Voltage ratio $G_{g/d'}$ versus M with both the proposed and the conventional capacitive coupling structures.

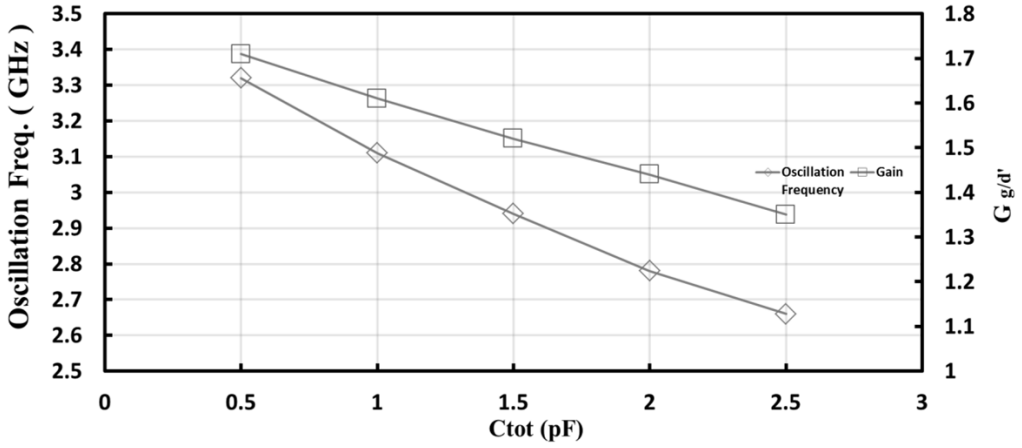


Fig. 4.14 Simulated oscillation frequency and $G_{g/d'}$ versus C_{tot}.

4.4.3 Inductive Coupling Based Structure

The embedding of inductive coupling has different concerns as compare to capacitive coupling. The similar structure based same oscillator, which is shown in Fig. 4.9, will be taken as example.

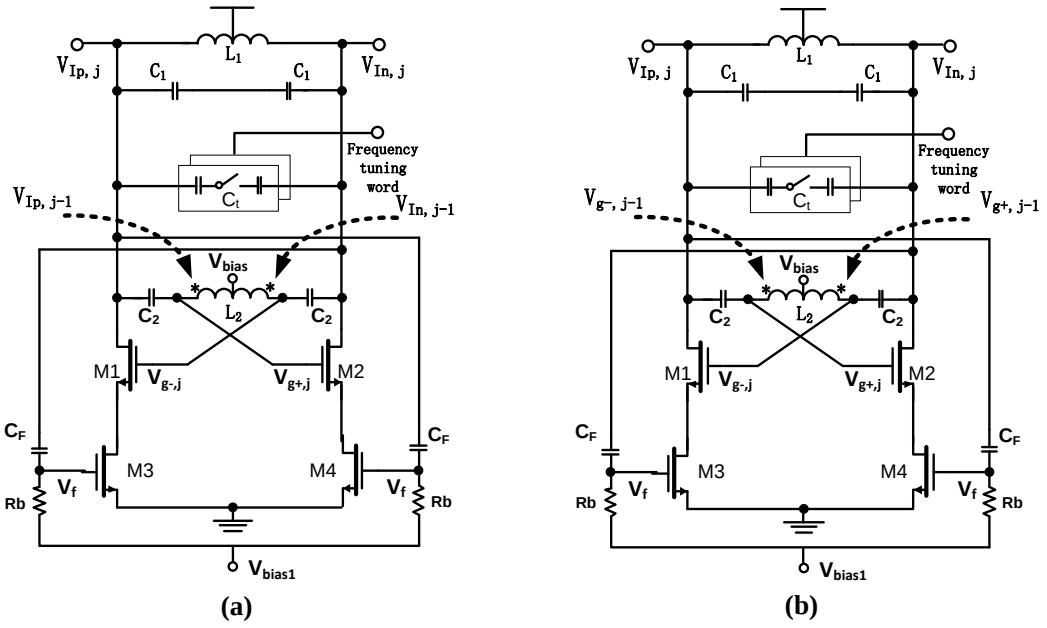


Fig. 4.15 Schematic diagrams of two candidate implementations of inductive coupling. (a) coupling at node $V_{f\pm,j}$. (b) coupling at node $V_{g\pm,j}$.

Similar to the capacitive coupling, there're few candidates to choose and two of them are shown in Fig. 4.15. In the first structure, the coupling signal is drawn from the output of the oscillator and the coils of the transformer including L_1 of the current core and L_2 of the adjacent core. In the second structure, the coupling signal is drawn from the gate of the cross-coupled transistor and the coils of the transformer including L_1 of the current core and L_1 of the adjacent core.

In fact, for QVCO, both structures can function properly though in different manners. However, unlike capacitive coupling, in certain inductive coupling structures, the complexity of

the transformer design is going to increase dramatically as number of coupling cores increases. For instance, the structure in figure Fig. 4.15(b) is not a good candidate for higher number of cores. The reason for that is that the number of coils in the transformer has to scale with the number of cores, and it's going to be too unrealistic to design such a transformer.

Fortunately, the structure in Fig. 4.15(a) is extremely easy to expand. For example, the schematic diagram of the proposed 4-core-coupled oscillator is shown in Fig. 6.2, where the dashed lines represent the coupling paths among the transformers. Signal is drawn from the drain of the cross-coupled transistors and coupled to the gate of the same transistors in the next core; forming the coupling path.

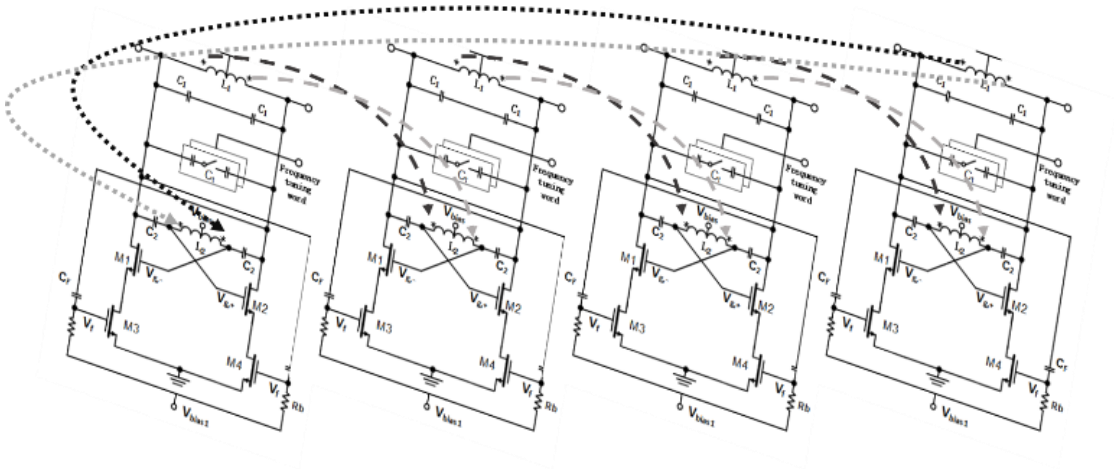


Fig. 4.16 The schematic diagram of the proposed 8-phase oscillator.

4.4.4 Passive Models of Inductive Coupling Structure

Take the structure in Fig. 4.15(a) as example to show inductive coupling mechanism works. In this particular case, the large coupling strength is the goal and the voltage at the gate of the cross-coupled transistor is the superposition of two voltages: 1) the one coming from the output of the same core; and, 2) that from the output of the adjacent core.

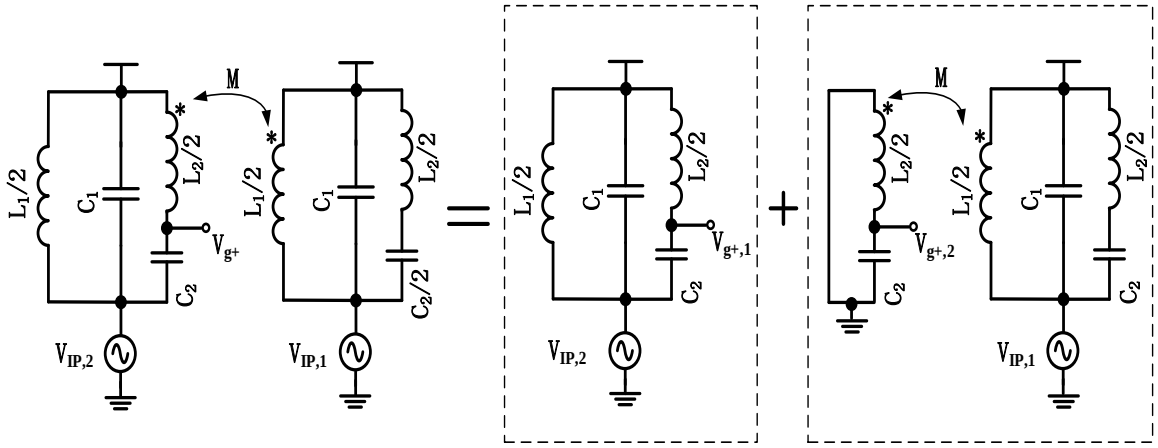


Fig. 4.17 The simplified equivalent model of coupling paths.

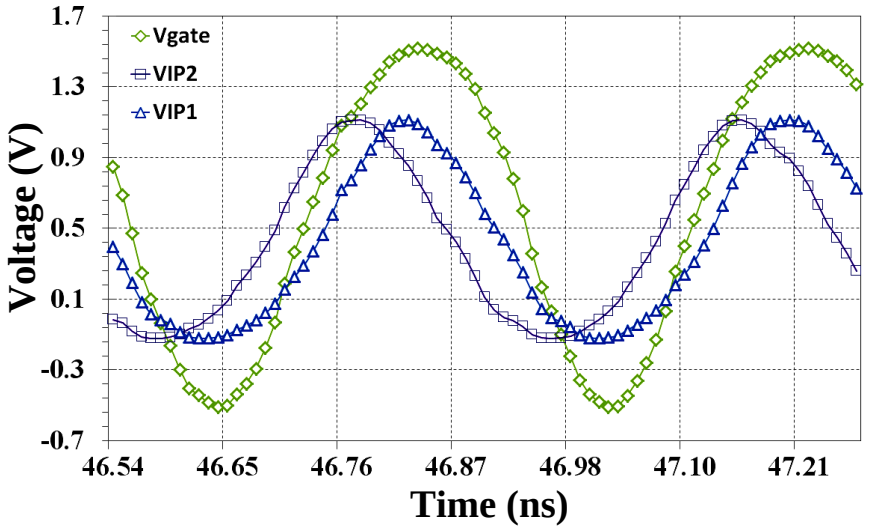


Fig. 4.18 Simulated plots of the transient waveforms of V_{IP1}, V_{IP2}, and Vg+.

Fig. 4.17 illustrates the signal flows in the simplified circuit, where V_{g+} is the gate voltage and only one side of the cross-coupled network is shown. $V_{g+,1}$ is the part of the gate voltage that comes from the output of the same core, and its major role is to provide the oscillation signal. $V_{g+,2}$ is the other part of the gate voltage that comes from the output of the adjacent core, and contributes to both coupling and oscillation. Assuming that the output sources $V_{IP,1}$ and $V_{IP,2}$ are independent, the two parts of the gate voltage can be separated and expressed as follows:

$$V_{g+,1} = V_{IP,2} * s^2 L_2/(2 + s^2 L_2 C_2) \quad (4.11)$$

$$V_{g+,2} = V_{IP,1} * k\sqrt{L_2/L_1} \quad (4.12)$$

where k is the coupling factor of the transformer. The proposed structure is unlike the conventional dual-tank configuration, where the ratio of L_2/L_1 is small and the ratio of the gate voltage of the cross-coupled transistor over its drain voltage is large. In order to ensure strong coupling, the ratio of L_2/L_1 must be sufficiently large in the proposed architecture. As a result, the impedance of $L_2/2$ dominates that of C_2. Therefore, $V_{g+,1} \approx V_{IP,2}$, and V_{g+} is dominated by $V_{g+,2}$. In addition, the transient waveforms are plotted in Fig. 4.18, and the coupling strength, *m*, is equal to

$$m = s^2 k(2 + s^2 L_2 C_2)/\sqrt{L_2 L_1} \approx k\sqrt{L_2/L_1} \quad (4.13)$$

4.5 Start-up Condition

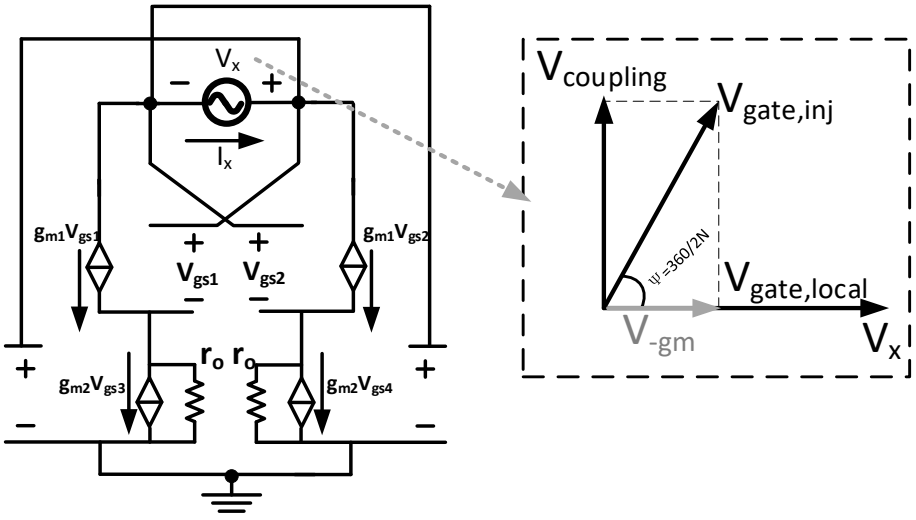


Fig. 4.19 Equivalent circuit for negative trans-conductance of the proposed oscillator architecture.

For the general case of multi-core coupling, the signal from both the local core and the coupling core contributes to the startup. To illustrate this idea, the equivalent circuit in Fig. 2.17 is redrawn and its gate voltage also includes the portion from coupling signal, as shown in Fig. 4.19.Suppose V_{gate} is the gate voltage in a single-core case. As a result, in the multi-core case, the part of the gate voltage originating from the local core will be $V_{gate,local} = V_{gate}(M/(1+M))$, and that coming from the coupling core will be $V_{gate,inj} = V_{gate}(1/(1+M))$. Therefore, only the part of $V_{gate,inj}$ that is V_{-gm} and in phase with $V_{gate,local}$ contributes to the negative impedance, and the rest contributes to the coupling. Thus, assuming all oscillator cores are operating at a stable condition, and V_x is equal to $V_{gate}\left(\frac{M}{1+M} + \frac{1}{1+M}\cos(\pi/N)\right)$ and Eq. (2.10) can be re-written as follows:

$$R_{startup} = \frac{2}{g_{m1}}\frac{1+g_{m1}r_o}{1+g_{m2}r_o}\left(\frac{M}{1+M} + \frac{1}{1+M}cos(\pi/N)\right) \quad (4.14)$$

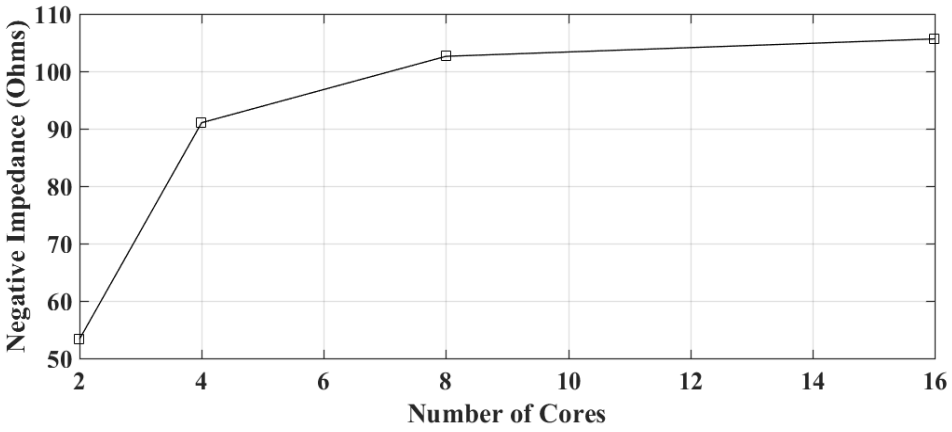


Fig. 4.20 Negative impedance versus the number of coupled core.

As shown in Fig. 4.20, as the number of cores increases, the coupling system starts up more easily, because the coupled signal increases the portion of voltage that is in phase with the injected output.

4.6 Alder's Equation

Alder's equation [1], [20-21] explains the behaviors of the signal injection between two oscillators and especially between free running oscillator whose frequency can be changed externally and impressed oscillator whose frequency is fixed.

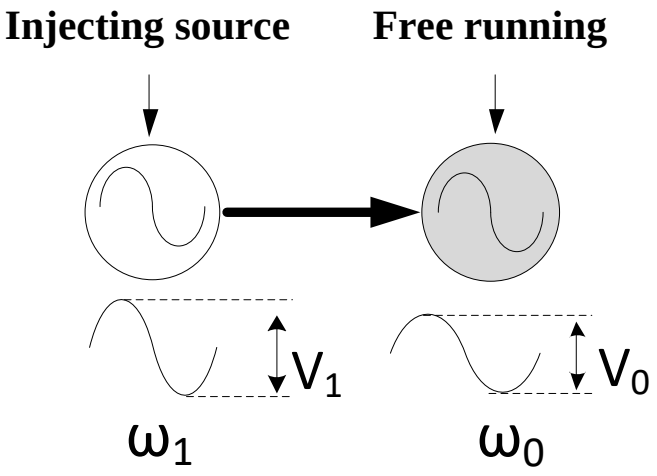


Fig. 4.21 Illustration of concept of Alder's equation.

Its original concept is illustrated in Fig. 4.21, where shows that an impressed oscillator, whose operating frequency is at ω_1, injects its signal to another free-running oscillator, whose operating frequency is at ω_1. Assuming that the free running oscillator is locked by the impress oscillator, the frequency of the free running oscillator will be the same as the frequency of impressed one. However, due to the different of their initial frequencies, the phase difference between two cores is going to be

$$\theta_1 - \theta_0 = \sin^{-1}\left(2Q\frac{V_0}{V_1}\frac{\Delta\omega_0}{\omega_0}\right) \tag{4.15}$$

where θ_0 is the phase from the injection source, θ_1 is the phase of free running oscillator after locking, $\Delta\omega_0$ is equal to $\omega_1 - \omega_0$, Q represents the quality factor of the resonator and V_1 and V_0 are the voltage swings from impressed oscillator and free running one, respectively.

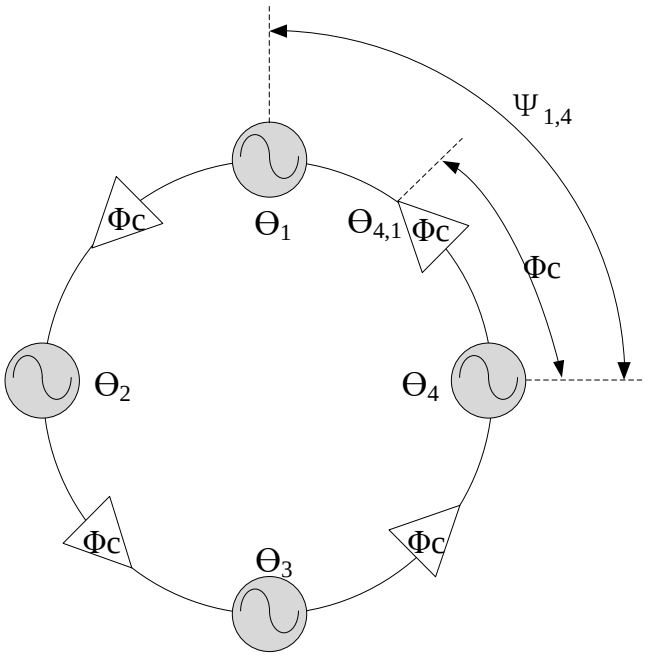


Fig. 4.22 Diagram of conventional coupled-oscillator system.

4.6.1 Coupled Oscillators in the Closed-Loop System

The coupled-oscillator system used for multi-phase clock generation is usually a closed-loop system. Some of its behavior can also be explained by generalized Alder's equation. In Fig. 4.22, the diagram of conventional coupled-oscillator system is shown, where $\Psi_{1,4}$ is the phase difference between adjacent cores and equal to $\theta_4-\theta_1$; Φ_c is the phase delay from the output of the previous core to the input of its next core and equals to $\theta_{4,1}-\theta_4$. Therefore, Alder's equation can be rewrite as follows:

$$\omega_1 - \omega_0 = \frac{\omega_0}{2Q}\frac{V_1}{V_0}\sin\left(\Phi_c - \Psi_{1,4}\right), \tag{4.16}$$

where $\Phi_c - \Psi_{1,4} = \theta_4-\theta_{4,1}$ is the phase difference between the output of the local core and coupling signal from adjacent core. In sum, the equation reveals that by changing $\Phi_c - \Psi_{1,4}$, the

operating frequency can be tuned. Vice versa, if we intentionally offset the oscillation frequencies among those cores, the phase between adjacent cores can be tuned.

In the following sections, the behavior of the coupled-oscillator will be further analyzed by utilizing Adler's equation, and a four-core system will be taken as an example.

4.6.2 The Derivation on Phase Relationship

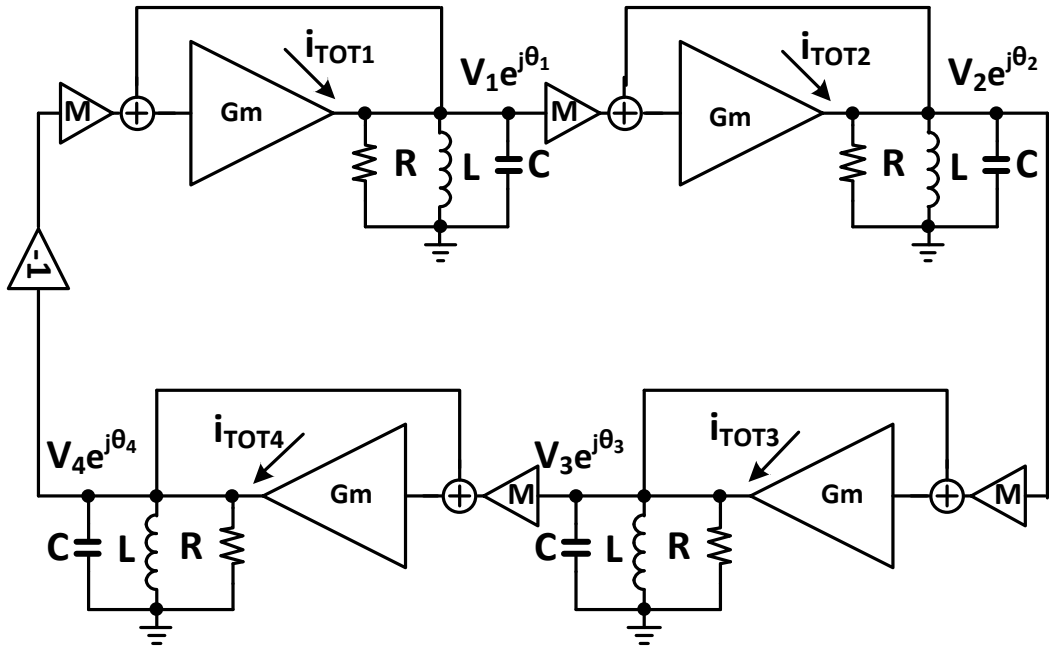


Fig. 4.23 Equivalent circuit of the coupling path.

As mentioned in [21], the Generalized Alder's equation is a strong tool for analyzing the coupling effects among LC oscillators. To begin the analysis, the equivalent model of the multi-phase oscillator is illustrated in Fig. 4.23, where $i_{TOT,j}$ is the sum of self-resonance current I_j and the coupling current $I_{c,j}$, and their ratio $I_{c,j}/I_j$ is equal to the coupling strength factor M. θ_j is the phase of a given tank, and is expressed as $\theta_j = \omega_{\mathrm{osc}}\mathrm{t} + \Psi_j$. In addition, in this case, the phase delay Φ_c is assumed to be zero, which is common in most coupled-oscillator system. Therefore, the differential equations for phases and amplitudes based on the Generalized Adler's Equation are as follows:

$$\frac{d\theta_1}{dt} = \omega_0 - \frac{\omega_0}{2Q}\frac{I_{c,4}\,sin(\theta_4-\theta_1)}{I_1 - I_{c,4}\,cos(\theta_4-\theta_1)} \tag{4.17}$$

$$\frac{d\theta_2}{dt} = \omega_0 + \frac{\omega_0}{2Q}\frac{I_{c,1}\sin(\theta_1-\theta_2)}{I_2+I_{c,1}\cos(\theta_1-\theta_2)} \tag{4.18}$$

$$\frac{d\theta_3}{dt} = \omega_0 + \frac{\omega_0}{2Q}\frac{I_{c,2}\sin(\theta_2-\theta_3)}{I_3+I_{c,2}\cos(\theta_2-\theta_3)} \tag{4.19}$$

$$\frac{d\theta_4}{dt} = \omega_0 + \frac{\omega_0}{2Q}\frac{I_{c,3}\sin(\theta_3-\theta_4)}{I_4+I_{c,3}\cos(\theta_3-\theta_4)} \tag{4.20}$$

$$RC\frac{dA_1}{dt} + A_1 = \frac{4R}{\pi}(I_1 - I_{c,4}\,cos(\theta_4-\theta_1)) \tag{4.21}$$

$$RC\frac{dA_2}{dt} + A_2 = \frac{4R}{\pi}(I_2 + I_{c,1}\,cos(\theta_1-\theta_2)) \tag{4.22}$$

$$RC\frac{dA_3}{dt} + A_3 = \frac{4R}{\pi}(I_3 + I_{c,2}\,cos(\theta_2-\theta_3)) \tag{4.23}$$

$$RC\frac{dA_4}{dt} + A_4 = \frac{4R}{\pi}(I_4 + I_{c,3}\,cos(\theta_3-\theta_4)) \tag{4.24}$$

where A_j is the amplitude of the voltage of a given tank. In the ideal case, since there is no mismatch among oscillators, the tank currents are equal to one other, and so are the injection currents.

Assuming Ψ_1 is a reference phase, which is zero degrees, two sets of solutions with a stable condition can be obtained: 1) Ψ_1= 0, Ψ_2= π/4, Ψ_3= π/2, and Ψ_4= 3π/4; 2) Ψ_1=0, Ψ_2= -π/4, Ψ= -π/2, and Ψ_4= -3π/4. By inserting phases in equations (4.17) to (4.24), the oscillator frequencies and amplitudes for both modes are equal to

$$\omega_{m1} = \omega_0 + \frac{\omega_0}{2Q}\frac{M\sqrt{2}/2}{1 + M\sqrt{2}/2} \tag{4.25}$$

$$\omega_{m2} = \omega_0 - \frac{\omega_0}{2Q}\frac{M\sqrt{2}/2}{1 + M\sqrt{2}/2} \tag{4.26}$$

$$A_{m1} = A_{m2} = \frac{4R}{\pi} I(1 - M\sqrt{2}/2) \tag{4.27}$$

where ω_{m1} and ω_{m2} are the oscillation frequencies when Ψ_2= -π/4 and Ψ_2= π/4, respectively. It can be seen that both modes have the same amplitude; however, the oscillation frequency of one mode is higher than the resonance frequency of the LC tank, while that of the other mode is lower. Simulation shows that the proposed oscillator architecture tends to oscillate at a higher frequency.

Compared to the quadrature-coupled oscillator, it can be seen that as the number of cores increases to four in the proposed oscillator architecture, the oscillation frequencies of the cores approach ω_0, and the amplitude of the voltage swing increases. That is because the phase difference between the injected current and the self-resonance current is small, and requires a smaller angle for the tank to rotate in order to convert current to voltage.

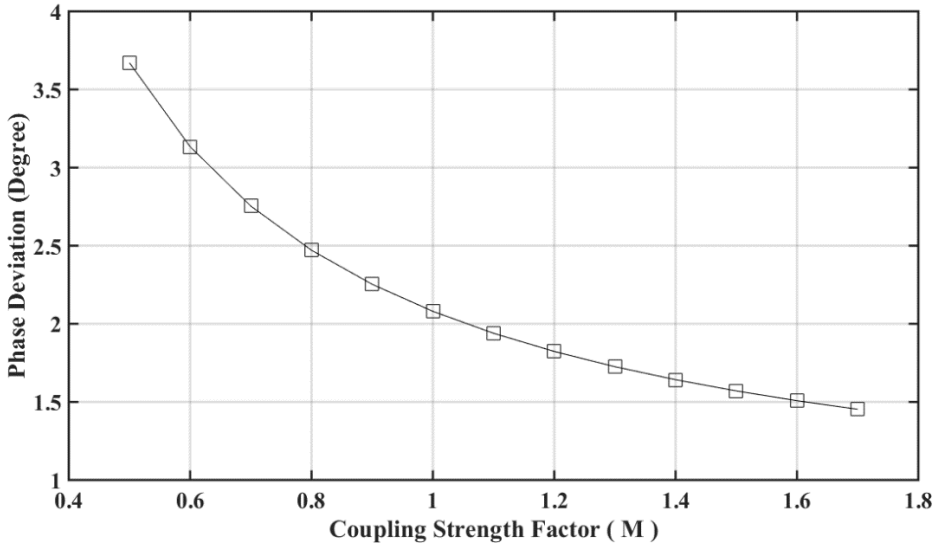


Fig. 4.24 The plot of phase deviation versus coupling strength factor.

Phase error can be analyzed by introducing mismatch to the tank. Let us assume that the tank mismatch occurs in the first tank, and the phase difference among cores is $-\pi/4$. By substituting ω_0 with $\omega_0 - \Delta\omega$ in Eq. (4.16), and setting $\theta_1 = \omega_{osc}t$, $\theta_2 = \omega_{osc}t - \pi/4 + \Delta\varphi_2$,

$\theta_3 = \omega_{osc}t - \pi/2 + \Delta\varphi_3$, and $\theta_4 = \omega_{osc}t - 3\pi/4 + \Delta\varphi_4$ in equations (4.17) to (4.24)it can be concluded that $\Delta\varphi_2 = \Delta\varphi = \Delta\varphi_2/2 = \Delta\varphi_3/3$. Therefore, the phase deviation due to the tank mismatch can be written as follows:

$$\Delta\varphi = \frac{Q}{2}\frac{(1 + M\cos(\pi/4))^2 + \frac{M}{2Q}(2\sin(\pi/4) + M)}{M(M + \cos(\pi/4))}\frac{\Delta\omega}{\omega_0} \tag{4.28}$$

where $\Delta\varphi$ is also the phase deviation between adjacent cores. $\Delta\varphi$ versus M with one percent mismatch in the tank capacitor is plotted in Fig. 4.24.

4.6.3 The Derivation on Phase Noise

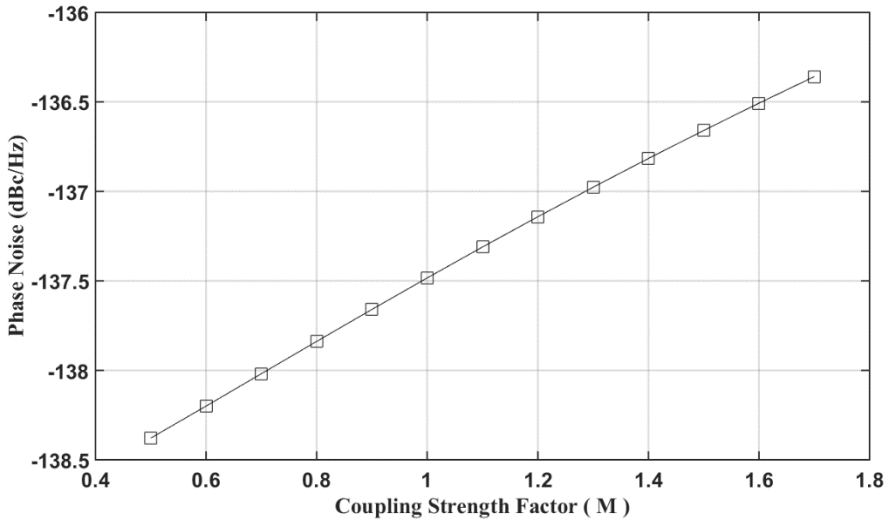


Fig. 4.25 The plot of phase noise versus coupling strength factor.

The phase noise of a coupled-oscillator system can be analyzed by further applying the Generalized Adler's Equation. Again, the equivalent circuit shown in Fig. will be taken as example. In order to obtain a complete expression for the phase noise, the contribution from both the white noise and the transistor noise is taken into account. First, let us introduce the white noise to the tank by injecting noise current i_n, whose spectral density is $4KT/R$ and whose phase is $\theta_n = \omega_{osc}t + \omega_m t$. Consequently, the phases of the oscillators become $\theta_1 = \omega_{osc}t + \hat{\theta}_1$,

$\theta_2 = \omega_{osc}t - \pi/4 + \hat{\theta}_2$, $\theta_3 = \omega_{osc}t - \pi/2 + \hat{\theta}_3$, and $\theta_4 = \omega_{osc}t - 3\pi/4 + \hat{\theta}_4$, where $\hat{\theta}_1$, $\hat{\theta}_2$, $\hat{\theta}_3$, and $\hat{\theta}_4$ are the phase fluctuation due to the injected noise. To analyze this noise, Eq. (4.17) is modified to the following:

$$\frac{d\theta_1}{dt} = \omega_0 - \frac{\omega_0}{2Q}\frac{I_{C,4}\sin(\theta_4-\theta_1)+\frac{\pi}{4}i_n\sin(\theta_n-\theta_1)}{I_1-I_{C,4}\cos(\theta_4-\theta_1)+\frac{\pi}{4}i_n\cos(\theta_n-\theta_1)} \tag{4.29}$$

By inserting the phases in (4.17)-(4.20), and further simplifying, we obtain:

$$\begin{aligned}\frac{d\hat{\theta}_1}{dt} &= \frac{\omega_0}{2Q}\frac{M(\cos(\pi/4)+M)}{(1+M\cos(\pi/4))^2}\left(\hat{\theta}_2-\hat{\theta}_1\right)\\ &-\frac{\omega_0}{2Q}\frac{\pi}{4}\frac{i_n/I}{1+M\cos(\pi/4)}\sin\omega_m t -\\ &\frac{\omega_0}{2Q}\frac{\pi}{4}\frac{i_n/I(M\sin(\pi/4))}{(1+M\cos(\pi/4))^2}\cos\omega_m t\end{aligned} \tag{4.3.}$$

$$\frac{d\hat{\theta}_2}{dt} = \frac{\omega_0}{2Q}\frac{M(\cos(\pi/4)+M)}{(1+M\cos(\pi/4))^2}\left(\hat{\theta}_3-\hat{\theta}_2\right) \tag{4.31}$$

$$\frac{d\hat{\theta}_3}{dt} = \frac{\omega_0}{2Q}\frac{M(\cos(\pi/4)+M)}{(1+M\cos(\pi/4))^2}\left(\hat{\theta}_4-\hat{\theta}_3\right) \tag{4.32}$$

$$\frac{d\hat{\theta}_4}{dt} = \frac{\omega_0}{2Q}\frac{M(\cos(\pi/4)+M)}{(1+M\cos(\pi/4))^2}\left(\hat{\theta}_1-\hat{\theta}_4\right) \tag{4.33}$$

If only the close-in phase noise is considered when $\omega_m \ll M(\cos(\pi/4)+M)/(1+M\cos(\pi/4))^2$, the phase variation is equal to:

$$\begin{aligned}\hat{\theta}_1 \approx \hat{\theta}_2 \approx \hat{\theta}_3 \approx \hat{\theta}_4 &\approx -\frac{\omega_0}{8Q}\frac{\pi}{4}\frac{i_n/I}{1+M\cos(\pi/4)}\frac{1}{\omega_m}\\ &\times\left(\cos\omega_m t - \frac{M\sin(\pi/4)}{1+M\cos(\pi/4)}\sin\omega_m t\right)\\ &\approx -\frac{\omega_0}{8Q}\frac{\pi}{4}\frac{Ri_n}{V}\frac{1}{\omega_m}\left(\cos\omega_m t - \frac{M\sin(\pi/4)}{1+M\cos(\pi/4)}\sin\omega_m t\right)\end{aligned} \tag{4.34}$$

By repeating the above analysis for both the regenerative and the coupled noise from the cross-coupled transistors, the ratio of the spectral densities is as follows:

$$\frac{\mathcal{L}_{SW,C}}{\mathcal{L}_{SW,C}} = M\left(\frac{cos(\pi/4)+M}{1+M\,cos(\pi/4)}\right)^2 \tag{4.35}$$

By combining (22) and (23), the overall phase noise is

$$\mathcal{L}(\omega_m) = \frac{kTR}{2V^2} F \left(\frac{\omega_0}{Q\omega_m}\right)^2 \tag{4.36}$$

where the noise factor is

$$F_{min} = 1 + \left(\frac{M\,sin(\pi/4)}{1+M\,cos(\pi/4)}\right)^2 + \gamma \left[\frac{1}{1+M\,cos(\pi/4)}\left(1 + M\left(\frac{cos(\pi/4)+M}{1+M\,cos(\pi/4)}\right)^2\right)\right] \tag{4.37}$$

The graph of the phase noise versus M (Fig. 4.25) also illustrates the same trend as the simulation results.

4.6.4 Artificial Phase Shift

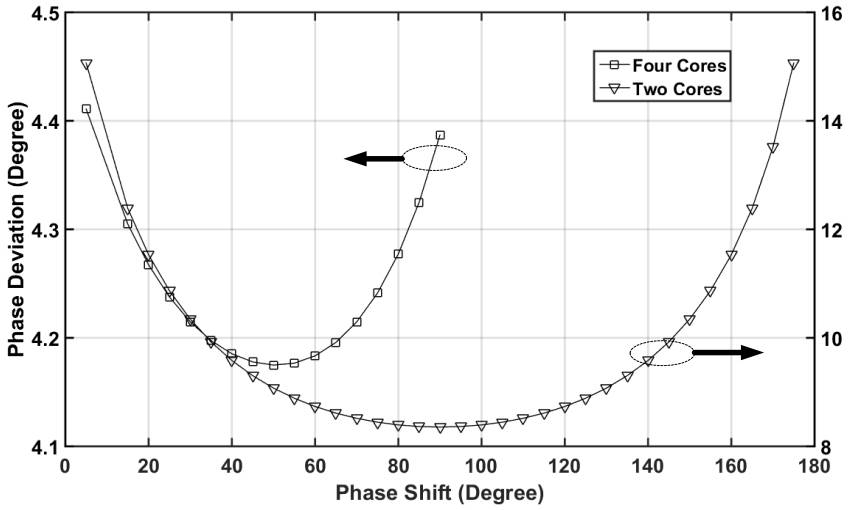


Fig. 4.26 Plot of phase deviation versus frequency for both the four-core and two-core cases.

As mentioned earlier, by adding a certain phase shift to the coupling path, the interruption from the coupling signal will be mitigated, therefore both the phase noise and the phase accuracy can be further optimized, especially for two-core (quadrature) oscillator [22]-[23], where the peak of coupling signal is right at the output signal. However, as number of coupled cores increases, the improvement by adding phase shift will be smaller. Thus, it is worth comparing both the two-core and four-core structure, when phase shift is added to coupling path. Since equations for four-core system is not given in any publication, they will be introduced here. By

inserting the phase shift $\Phi_c = \varphi$, and repeating the above phase noise and phase accuracy analyses, (4.28) and (4.37) are re-written as follows:

$$\varphi = \frac{Q}{2}\frac{(1+M\cos(\pi/4-\varphi))^2+\frac{M}{2Q}(2\sin(\pi/4-\varphi)+m)}{M(M+\cos(\pi/4-\varphi))}\frac{\Delta\omega}{\omega_0} \tag{4.38}$$

$$F_{min} = 1+\left(\frac{M\sin(\pi/4-\varphi)}{1+M\cos(\pi/4)}\right)^2 + \gamma\left[\frac{1}{1+M\cos(\pi/4)}\left(1+M\left(\frac{\cos(\pi/4-\varphi)+M}{1+M\cos(\pi/4)}\right)^2\right)\right]$$

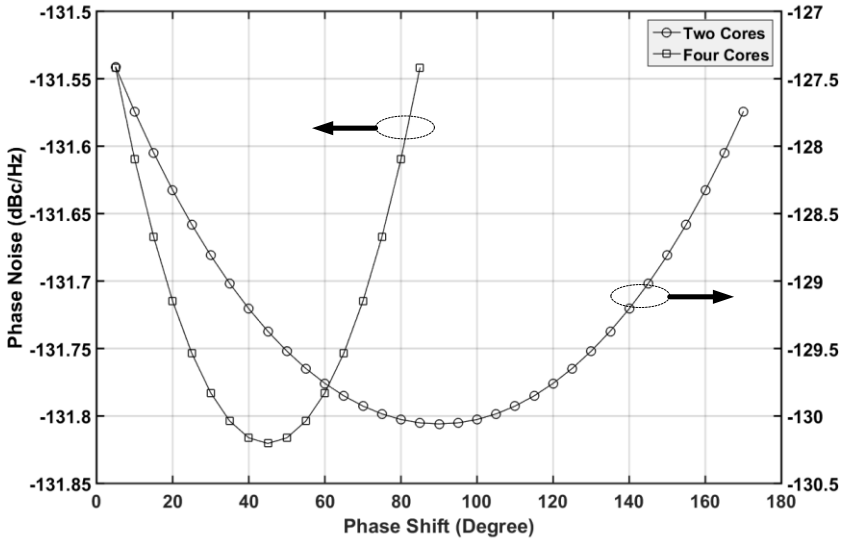


Fig. 4.27 Plot of phase noise versus frequency for both the four-core and the two-core cases.

From Figs. 4.26 and 4.27, the following two major differences are observed between the proposed oscillator and the quadrature case: 1) the optimization of the phase noise and the phase accuracy are not as effective as those of the quadrature oscillator. 2) The best optimization point is shifted from 90 degrees to approximately 45 degrees. As a matter of fact, these results are expected, because as the number of cores increases, the phase of the coupled signal becomes closer to the phase of the output signal. Therefore, it intrinsically moves the peak value of the coupled signal to the point which is less sensitive to noise. On the other hand, if the phase shift moves from 45 degrees to 90 degrees in a quadrature oscillator, there will be little improvement

in performance. Since the phase shift would increase noise, and might cancel its own improvement, we are not introducing any phase shift to the coupling path in any of our proposed structure, nor do we recommend doing so.

Chapter 5 Implementations of Coupled-Oscillator Systems

In this chapter, implementations of two proposed coupled oscillators will be introduced. Including the simulation and measured results, the design methodologies of the proposed techniques are given. To cover most interests, both capacitive coupling and inductive coupling techniques are implemented. The capacitive coupling based structure focuses on achieving ultra-low phase noise with low power consumption. However it is challenging to route coupling paths with symmetric floor plan by using capacitive coupling technique. To address this issue, we implement the inductive coupling structure, where the symmetric coupling paths can be naturally achieved, since coupling signal can be prorogate through transformer. In addition, the proposed inductive coupling can achieve ultra-high coupling strength by utilizing resonate transformer technique.

5.1 A Novel Multi-Phase Generation Architecture Based on Capacitive Coupling

5.1.1 Introduction

The proposed multi-phase clock generator consists of four oscillators and four coupling paths. Since the oscillators are of differential type, an eight-phase clock can be generated. The coupling among the first three oscillators (i.e., Oscillators1, 2, and 3) is in phase, while that

between oscillators 1 and 4 is 180 degrees out of phase in order to create a negative gain stage to meet the multi-phase system's phase requirement.

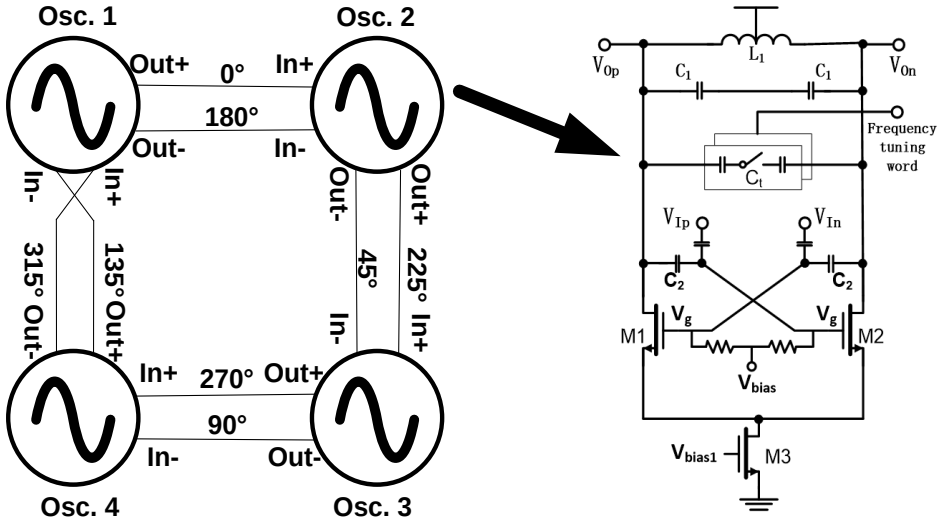


Fig. 5.1 The concept of coupled oscillator with capacitive coupling mechanism.

In addition, this chapter utilized a low-phase-noise and low-power oscillator core, which is similar to the structure in chapter 3, in order to achieve the best phase noise performance for the entire system. The proposed single oscillator core employs both dual tanks and an adaptive biasing feedback technique, which together with the customized coupling mechanism, feature the following to improve the phase noise:

A. Using the capacitive coupling mechanism to shift the injection current to a less sensitive point;
B. Using the intrinsic advantage of the N-core coupled system to reduce the phase noise by a factor of $10\log_{10} N$ (theoretically);
C. The dual-tank structure minimizes Q degradation due to the cross-coupled transistors by separating the voltage swing control of the drain and the gate and reducing the operation time in the triode region;

D. Using separate transistors for biasing to eliminate the second-order harmonic voltage that is generated with a single-transistor bias, and minimize the noise conversion from the bias transistor to the output;

E. The adaptive biasing feedback path reshapes the tail current and halves the tail transistor's noise;

F. The adaptive biasing feedback path changes the behavior of the cross-coupled transistors, and makes them switch faster in the equilibrium region.

This chapter will progressively describe how the proposed single oscillator core utilizes the capacitive coupling to generate multiple phases while exhibiting excellent phase noise performance.

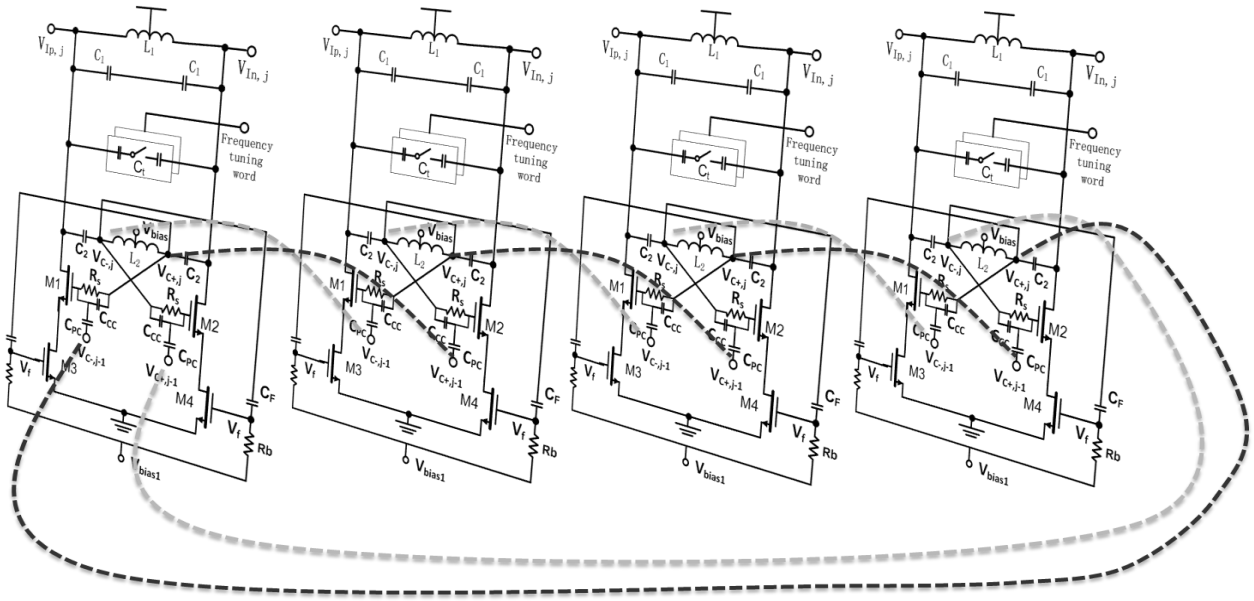


Fig. 5.2 The schematic diagram of the entire multi-phase oscillator.

5.1.2 The Architecture of the Individual Core

The single oscillator schematic without the coupling path is shown in Fig. 4.8, which is similar to the one introduced in chapter 3. The advantages from the separate biasing, adaptive

biasing and dual-tank are still kept. However, the bottom PMOS transistors are replace with NMOS ones for a better biasing scheme, since the PMOS transistor will require negative voltage at the gate when the supply voltage is low, and resulting in working into triode region.

By combining the proposed VCO structure and the coupling mechanism, we arrive at the entire circuit as shown in Fig. 5.2.

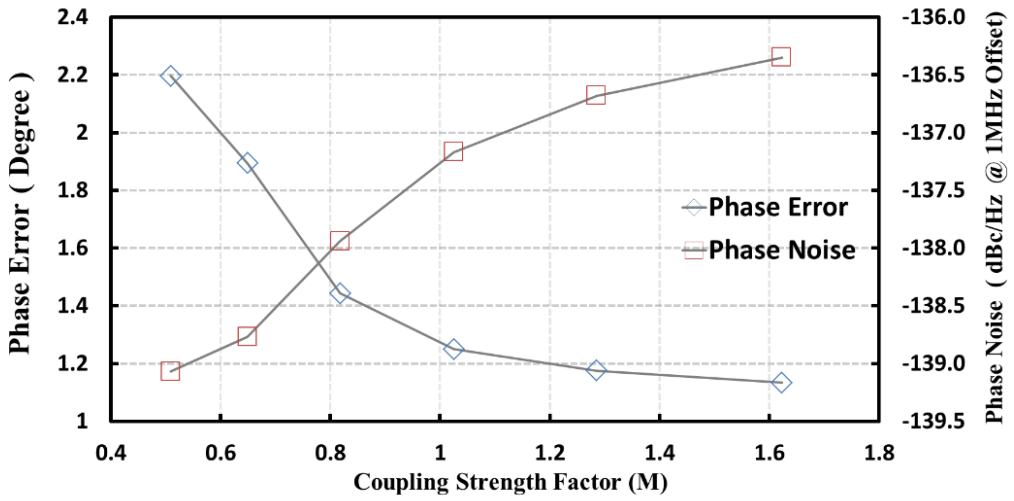


Fig. 5.3 Simulated phase error and phase noise versus coupling strength factor

As mentioned in chapter 4, the coupling strength creates a trade-off between the phase noise and the phase accuracy. In the proposed structure, this kind of trade-off exists, as well. By increasing the coupling strength factor, M, the phase accuracy will improve; however, the peak of V_{gate} is shifted towards the zero-crossing point of the output signal, where it has the highest noise sensitivity; thus, the phase noise will be degraded. In order to identify the best trade-off between the phase noise and the phase accuracy, these parameters were plotted versus the coupling strength as shown in Fig. 5.3. In order to generate phase error in the simulation, one percent capacitance mismatch was added to the LC tank. As M increases from 0 to 2, the

variation of phase error becomes quite stable for M greater than 1, and the phase noise continues to increase almost linearly.

5.1.3 Design Methodology

Since the proposed structure is modified by adding extra components and even changing the behavior of the dual-tank in order to make it compatible with each technique employed, it is worth discussing the justification behind the choice of some key components from the design perspective.

As mentioned earlier, R_S is added to the critical signal path to provide the DC voltage to the gate of the cross-coupled transistors; therefore, its value will directly affect the noise performance. As shown in Fig. 5.4, if R_S is so small and comparable to the impedance of capacitor C_1 (1pF) @ 2.4GHz (i.e., 66 Ohms), it will degrade the phase noise. Once Rs increases to 2.8 kΩ, the phase noise becomes flat and starts degrading slightly due to the increased thermal noise from Rs.

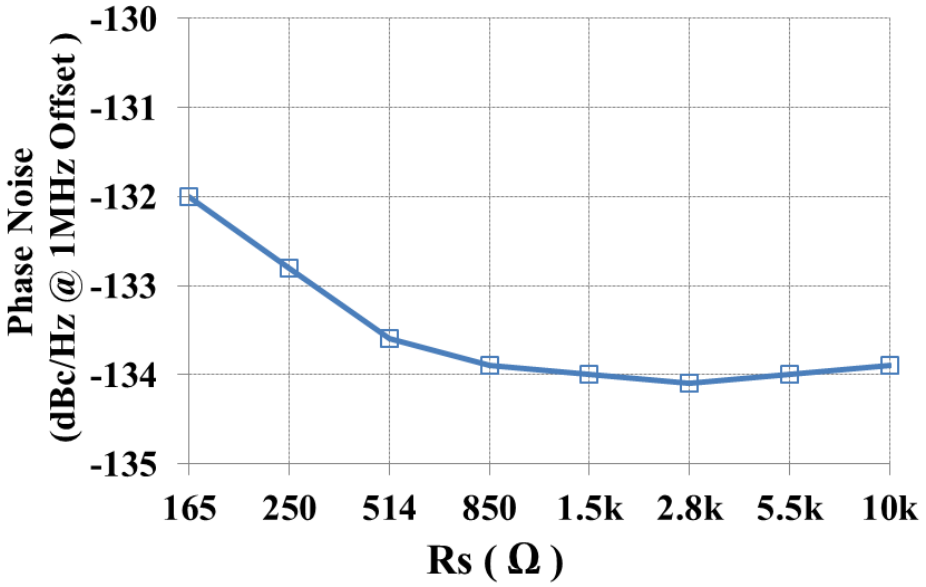


Fig. 5.4 Simulated phase noise versus R_S.

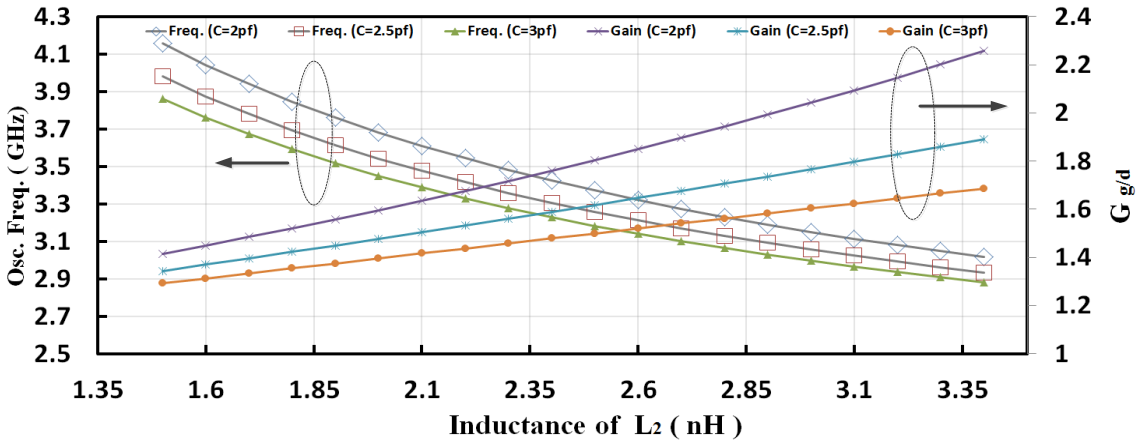


Fig. 5.5 Oscillation frequency and $G_{g/d}$ versus L_2 for different C_2 values.

As discuss in earlier chapter, the voltage swings of the dual tank are a function of the values of the passive components, and reveals that two oscillation frequencies exist in the dual-tank structure. In order to make the oscillator work at the desired frequency and condition, the ratio of the voltage swing of the gate over that of the drain should be large enough and equal to

$$G_{g/d} = {V_{gate}}/{V_{drain}} = 1/\left[1 - \left({\omega_2}/{\omega_0}\right)^2\right] \tag{5.1}$$

where $\omega_2 = \sqrt{2}/\sqrt{L_2C_2}$, and $\omega_0$is the desired oscillation frequency. By tuning the values of L_2 and C_2, the desired oscillation frequency and voltage ratio can be obtained. As shown in Fig. 5.5, if L_2 increases, the oscillation frequency and $G_{g/d}$ will increase. On the other hand, if C_2 decreases, the oscillation frequency will decrease and $G_{g/d}$ will increase.

To provide the design details of the dual-tank oscillator, we have analyzed three cases with different L_1 and L_2 combinations. As shown in Fig. 5.6, the voltage and impedance responses are plotted by injecting current to tank, where Z_{real} is the real part of the impedance seen from the output node. In the first case, where L_1 is smaller than L2, the voltage ratio $G_{g/d}$ is smaller than the other two cases; therefore, the FoM can still be improved. In the third case, where L_1 is larger than L_2, although the simulation shows a better FoM than the second case, the voltage ratio $G_{g/d}$

is exaggerated and there are a few potential issues. For example, the tank capacitor C_1 needs to be much larger in order to keep the same operating frequency, which will potentially affect the frequency tuning range. Additionally, since the output impedance is higher, the current must be reduced in order to maintain the voltage swings of both the gate and the drain. This will force the bottom device to be smaller; thus, potentially affecting the start-up condition. This will be discussed in the following section. It is also worth noting that other oscillation modes will be suppressed as L_1 increases and L_2 decreases.

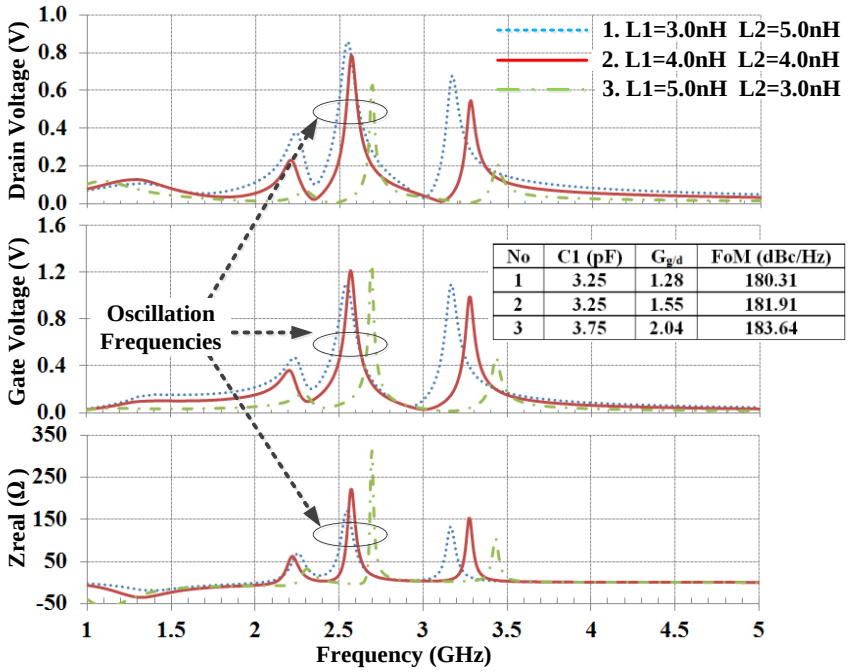


Fig. 5.6 Voltage and Impedance response of the proposed dual-tank structure.

The overall function and performance of the proposed oscillator can be verified by looking at the ISF function. As shown in Fig. 5.7, compared to the conventional structure (Fig. 5.1), the ISF of the proposed structure is largely reduced, and the effective ISF, which is the product of ISF and noise-modulating function (NMF), is close to zero more than three quarters of the time in an operation cycle.

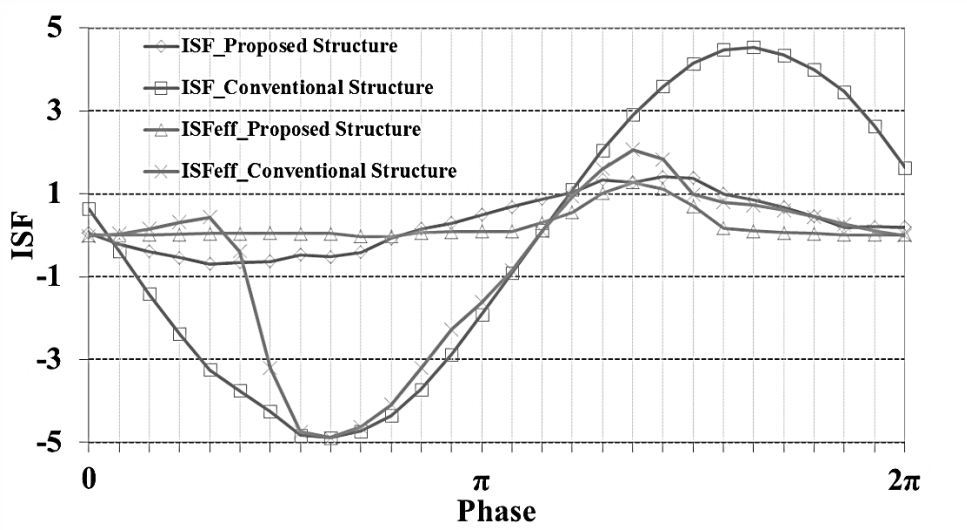


Fig. 5.7 Simulated ISF and ISF_{eff} of both conventional and proposed structure.

5.1.4 Measurement Results

The proposed four-core coupling oscillator is implemented in a 130nm RF SOI process, and the die photo is shown in Fig. 5.8. The four-core coupled oscillator occupies 2 x 1 mm^2 of chip area. Also, the solder bump is used for flip-chip type PCB.

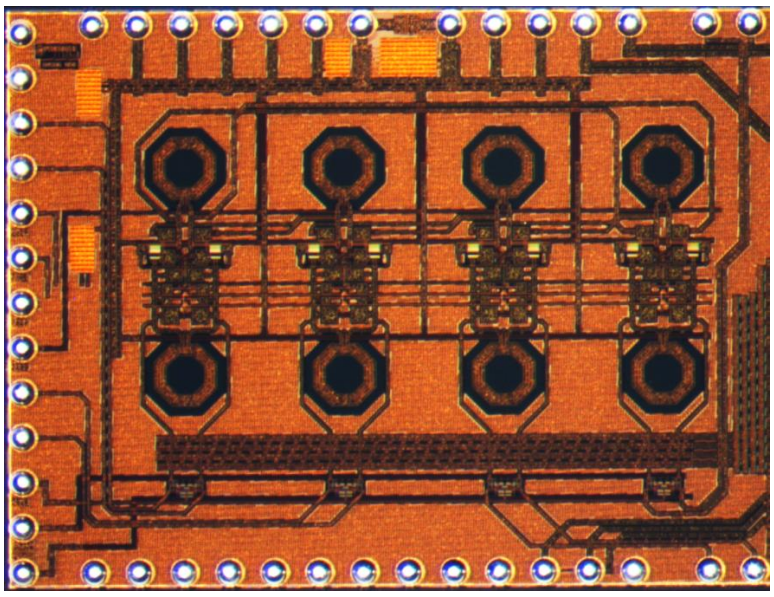


Fig. 5.8 Die photo of the proposed four-core oscillator.

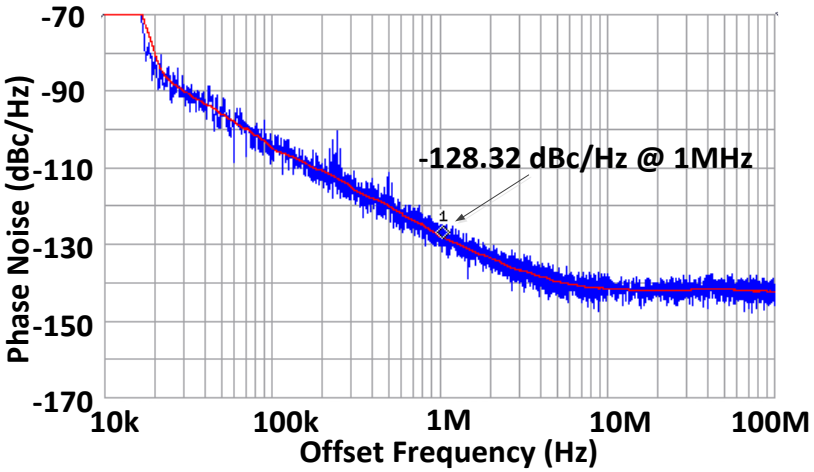


Fig. 5.9 Measured phase noise at 2.33 GHz (6mA each core).

The phase noise is measured using an Agilent E4440 spectrum analyzer with phase noise option without averaging. Figs. 5.9 to 5.11 illustrate the measured results of the phase noise at 2.33 GHz under different DC operating conditions. When the currents for each core are 6mA (0.7V), 10mA (1V), and 17mA (1.5V), the values of phase noise are -128.32 dBc/Hz, -132.94 dBc/Hz, and 135.52 dBc/Hz @ 1MHz offset, respectively. Since two frequency-tuning bits are implemented in the design, the operating frequency can be set to 2.22 GHz, 2.6 GHz, 2.9 GHz, and 2.33 GHz. In addition, Fig. 5.13 illustrates the noise figure versus operating frequencies for three different DC operating points.

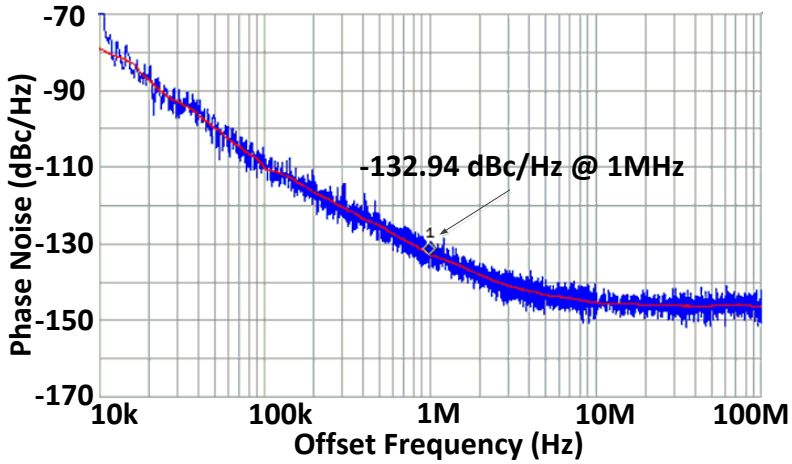


Fig. 5.10 Measured phase noise at 2.33 GHz (6mA each core).

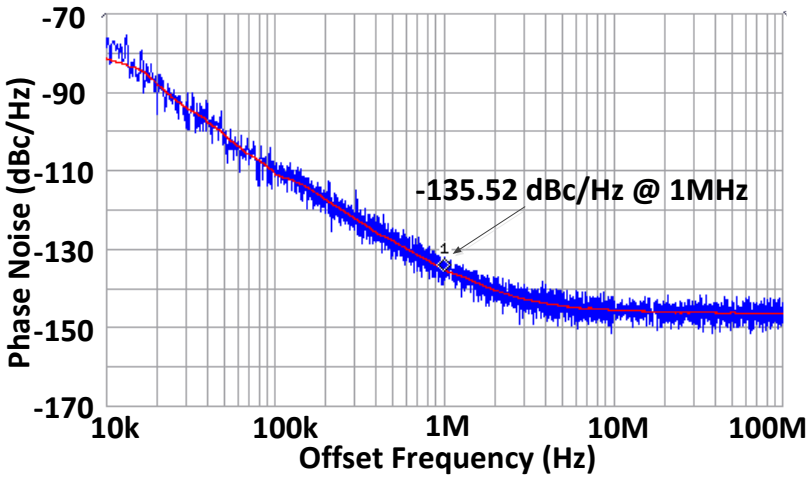


Fig. 5.11 Measured phase noise at 2.33 GHz (17mA each core).

The output waveforms of the proposed four-core oscillator are measured by a Rohde & Schwarz RTO Digital Oscilloscope, which supports simultaneous measurement of four channels. Fig. 5.13 exhibits four measured phases, out of eight phases, of the four-core oscillator, where the other four phases are the differential counterparts and not plotted. The phase differences between adjacent outputs, from left to right, are 46.04˚, 40.18˚, and 47.7˚, respectively.

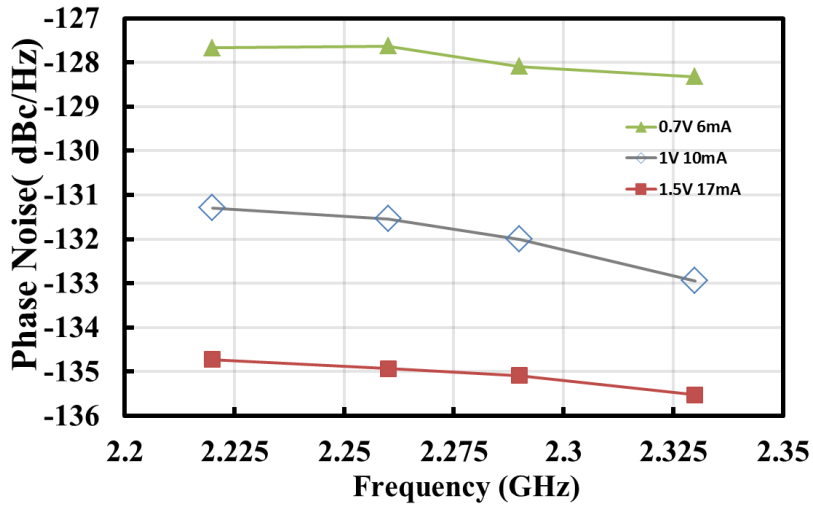


Fig. 5.12 Measured phase noise versus frequency for two DC operating points.

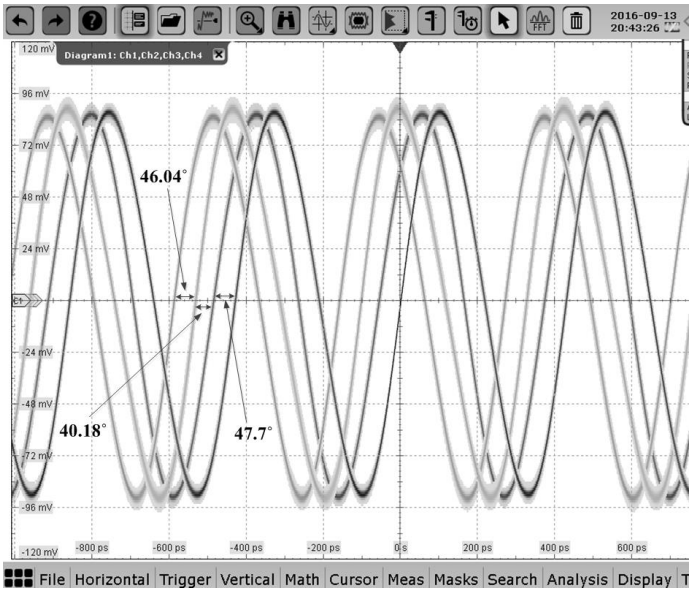


Fig. 5.13 Measured output waveforms of the proposed four-core oscillator.

Table 5.1 summarizes the performance of the proposed four-core oscillator and compares with recent multi-phase clock generation publications.

Table 5.1: Performance Summary and Comparison of Multi-phase Clock Generation Techniques

Ref.	Process	Freq. (GHz)	P.N. (dBc/Hz) @1 MHz	Power (mW)	FoM	No. of Phases	FoM Per Phase
This work	**130nm CMOS**	**2.33**	**-128.32**	**16.8**	**183.3**	**8**	**192.3**
			-133	**40**	**184.3**	**8**	**193.3**
			-135.52	**102**	**183**	**8**	**192**
[10]	65nm CMOS	14	-110	15	181.2	8	190.2
[24]	65nm CMOS	4.07	-136	126	188	4	194
[25]	65nm CMOS	3.8	-123.7	7	185	4	191

5.1.5 Conclusion

This paper presented a novel oscillator architecture with both dual-tank and feedback techniques, and coupled it for the purpose of multi-phase generation. The development of the proposed coupling strategy is illustrated, and a brief analysis of the proposed architecture is

demonstrated. The promising performance is verified by the measurement, which confirms the ultra-low phase noise of -135.52 dBc/Hz @ 1MHz.

5.2 A Novel Multi-Phase Generation Architecture Based on Transformer Coupling

5.2.1 Introduction

In the previous section, we present a capacitive coupled technique, and it shows very promising performance on the phase noise. However, there exists some potential issues as the number of the coupled oscillator cores goes up. For example, on the layout perspective, it becomes harder to achieve the symmetric routes of coupling paths and the size of the layout will grow dramatically, therefore dual-tank architecture which is mentioned in the previous chapter and size hungry cannot be used. Fortunately, transformer-based coupling mechanism provides us a solution that can achieve the symmetric routing and save the area for the multi-tank structures. Different from active and capacitive coupling mechanisms, the coupling path is embedded in the transformer and coupling signal can pass between adjacent cores through magnetic coupling, thus transformer coupling mechanism doesn't need extra paths for coupling signals, which make it easier for the layout floor plan. However, transformer design requires a careful EM modeling to ensure strong correlation between simulation and measurement.

In this section, we present the implementation of the novel magnetic coupling topology, which transforms the conventional dual-tank oscillator structure to one based on the transformer. With the adaptive biasing feedback, low phase noise and strong coupling strength can be achieved simultaneously. Additionally, using the EM modeling tool, all passive routing is carefully modified in order to minimize unnecessary coupling. The implementation of the highly symmetric floorplan will show at the later section.

5.2.2 The Transformer Coupled Oscillator

The proposed unit oscillator core is also mentioned in the Fig. 4.15, which adopts the dual-tank and the adaptive biasing feedback techniques, where *j* is the sequence number of the oscillator core. As introduced in the previous chapter, L_1 and L_2 are differential inductors, and, together with C_1 and C_2, form the dual-tank structure; two separate NMOS transistors (i.e., M_3 and M_4) provide the bias current; C_F and R_b provide the feedback path for adaptive biasing, which passes the AC voltage from the output to the gate of M_3/M_4. C_t represents the 3-bit digitally-controlled capacitor array for frequency tuning. The transformer is composed of coils L_1 and L_2, where coil L_1 is from the previous adjacent core and coil L_2 is from the current core; therefore, the output of the previous core can couple its signal to the gates of the cross-coupled transistors of the next oscillator core.

The complete schematic diagram of the proposed 8-phase oscillator is shown in Fig. 4.16. Unlike current transformer-based structures [26], signal is drawn from the drain of the cross-coupled transistors and coupled to the gate of the same transistors in the next core; forming the coupling path.

5.2.3 Phase Noise Optimization

In the proposed structure, phase noise is optimized using two techniques: 1) adaptive biasing; and, 2) dual tank. The first technique is implemented by feeding back the signal from the gate of $M_{1/2}$ to the gate of $M_{3/4}$. Since $M_{3/4}$ adjust their currents to follow the output signal, $M_{1/2}$ will be forced to switch faster, and spend less time in the equilibrium, where noise is the highest. Therefore, the adaptive biasing feedback increases the bias current when it is needed in order to expedite the transition and suppress the noise. In addition, by using two transistors for biasing, the second harmonic, which is present in the common node of the structure biased with a single

transistor, is eliminated, and the flicker noise is significantly suppressed. The conventional dual-tank structure optimizes the phase noise by increasing the voltage swing at the gate and thus reducing the operation time in the triode region, where the output impedance of the cross-coupled transistors is the smallest and the Q of the load is degraded. A similar optimization can be performed in the proposed transformer-based architecture, but in a much different manner.

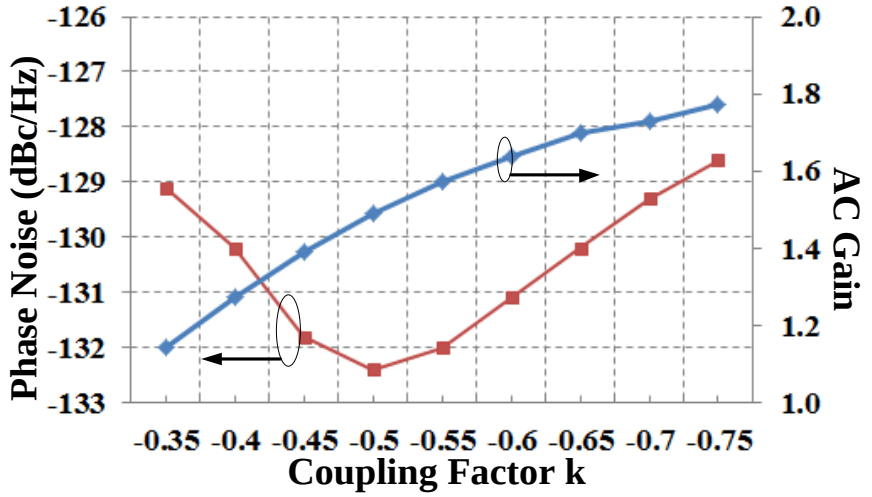


Fig. 5.14 Simulated phase noise and ac voltage gain versus the coupling factor of the transformer.

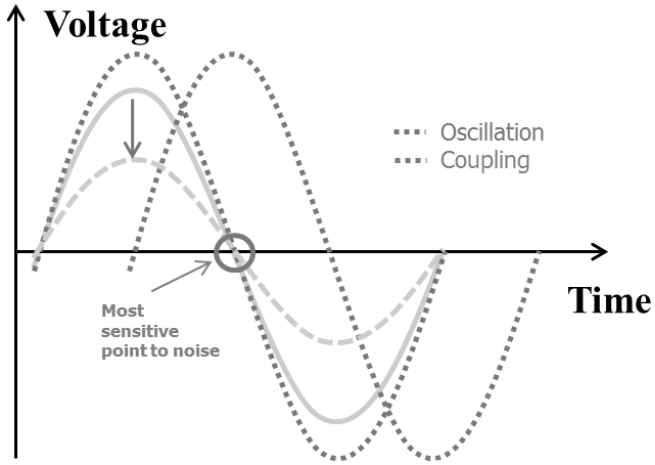


Fig. 5.15 Illustration of output and injected waveforms.

One major functional difference between the transformer-based and the conventional dual-tank oscillator is that the former affects both the coupling strength and the voltage swing at the

gates of the cross-coupled transistors at the same time. Therefore, the trade-off between the phase noise and the coupling strength does not follow the same convention as most coupled oscillators, where decreasing the coupling strength always leads to better phase noise. In order to illustrate this matter clearly, the simulated phase noise versus coupling factor, *k*, of the transformer is shown in Fig. 5.14, where AC gain is the ratio of $V_{IP,1}$ over $V_{g+,2}$, while constant current is maintained for different *k* values. As the coupling factor changes from -0.35 to -0.5, the coupling strength increases, and the phase noise improves. That is because when *k* is relatively small, phase noise still benefits from reduced operation time in the triode region. By further increasing the coupling factor, phase noise starts to degrade due to injection of the coupling signal at zero-crossing of the oscillation waveform, which is also the case for most prior-art coupled oscillators without phase shifting on the coupling paths.

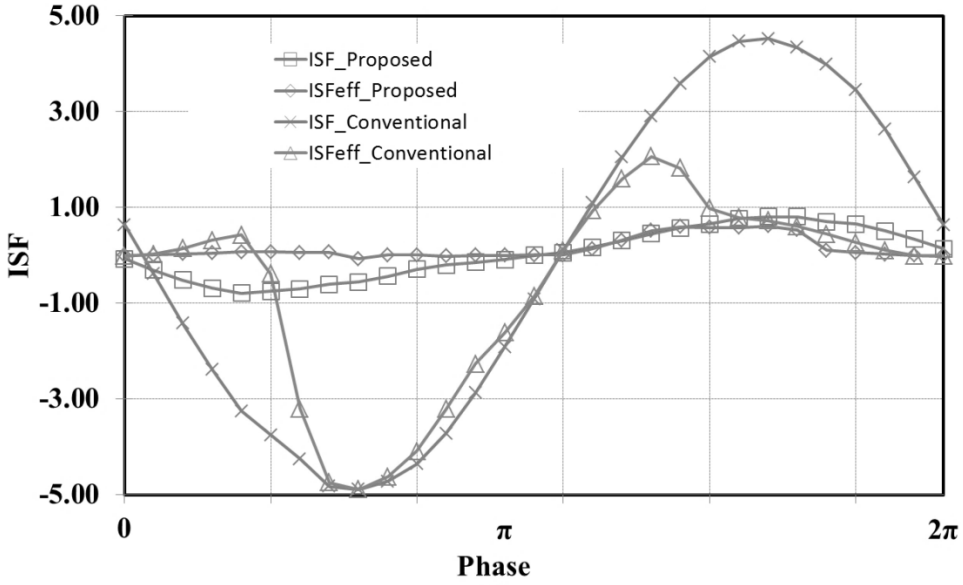


Fig. 5.16 ISF functions of proposed and conventional VCO structures.

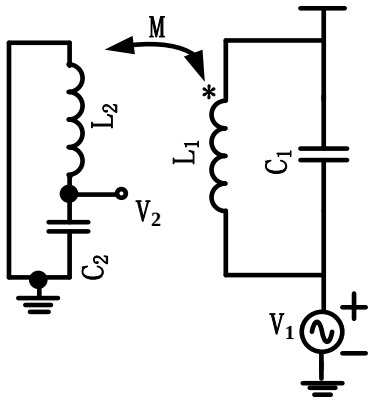
This can be also visualized in Fig. 5.15, where the signal coming from another core is broken down to two components: one for oscillation and one for coupling. As the voltage swing

of the output is reduced, the zero crossing point of it is going to be more sensitive to the injected signal.

In addition, the optimization of the phase noise can be verified by looking at the ISF function. As shown in Fig. 5.16, compared to the conventional structure, the ISF of the proposed structure is largely reduced, and the effective ISF, which is the product of ISF and NMF, is close to zero nearly three quarters of the time in an operation cycle.

5.2.4 Resonate Transformer Coupling

In conventional transformer structure, the voltage ratio between the coils is approximately equal to $V_2/V_1 = k\sqrt{L_2/L_1}$. Therefore, if coupling factor k and L_2/L_1 are small, limited voltage ratio can be achieved. In Fig. 5.17 case 1, no additional capacitance is added to the coupled coil and C_2 is the parasitic capacitator of L_2. In this case, the voltage ratio is equal to 0.79 which is even smaller than one, as shown in Fig. 5.18 (a), where L_2' is inductance counting in both C_2 and L_2. By adding additional capacitance to the coupled coil, the self-resonance frequency is also pushing towards the oscillation frequency of the tank, as shown in Fig. 5.18(b), the voltage ratio is largely enhanced and is roughly equal to 1.61.



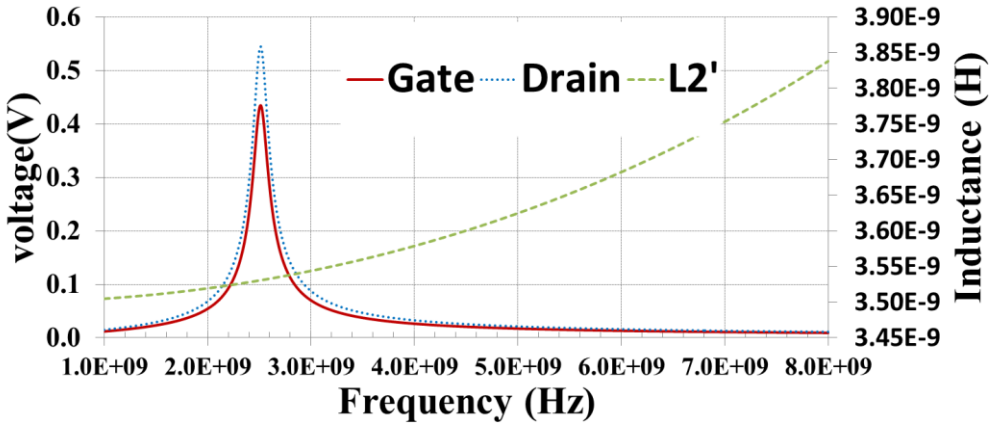
Component	Case1	Case2
L1	2 nH	2 nH
L2	3.5 nH	3.5 nH
C1	2 pF	1 pF
C2	10 fF	1 pF

Fig. 5.17 Equivalent model of transformer coupling and values of components in two different cases.

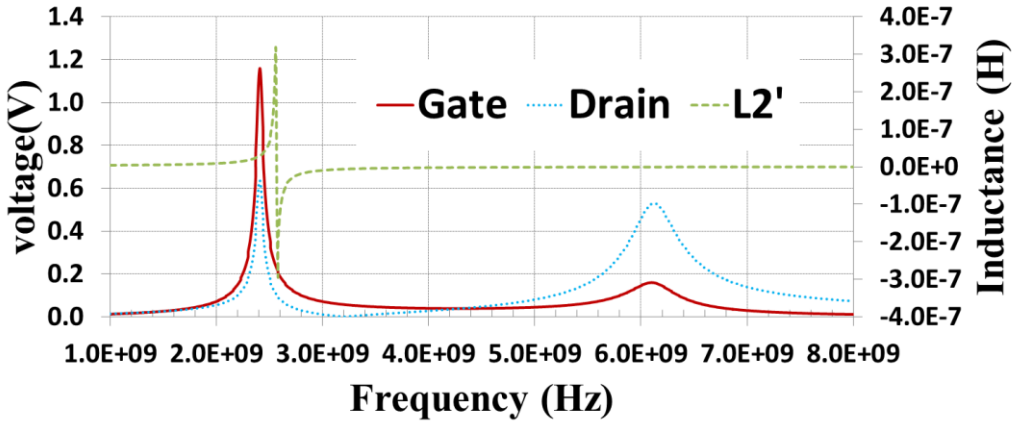
This phenomenon can be explained by the equivalent circuit in Fig. 5.22, where M is the mutual inductance and equal to $M = k\sqrt{L_1 L_2}$. Therefore, the voltage of V_2 is equal to

$$V_2 = V_1 \frac{Z_1}{j\omega L_1 + Z_1} \frac{1}{j\omega C_2 Z_2} \tag{5.2}$$

where $Z_1 = j\omega M \| Z_2$ and $Z_2 = j\omega L_2 + \frac{1}{j\omega C_2}$.



a)



b)

Fig. 5.18 Simulated results of two different cases. (a) conventional transformer coupling. (b) resonate transformer.

To properly graft this technique to the proposed structure, both C_1 and C_2 were swept to check the performance. As shown in Fig. 5.20, C_2 mainly determines the enhanced voltage ratio while changing C1 to keep oscillation frequency constant, and values and frequencies are listed

in Table 5.2. As C_2 increase, the voltage ratio increase but phase noise decrease. That indicates the voltage ratio is over-saturated, which is similar to the effect when coupling factor k is too large. What's more, if C_2 is too large, the oscillator might jump into undesired mode, where voltage ratio is close to 1 and FoM is largely degraded. On the other hand, if C_2 is too small, the reliability becomes an issue as well as the start-up condition.

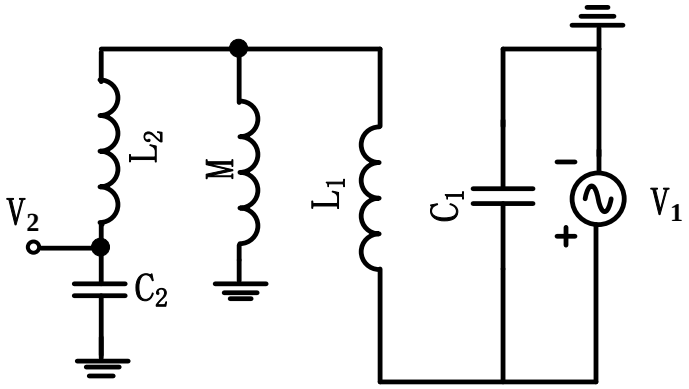


Fig. 5.19 Equivalent circuit of resonate inductive coupling.

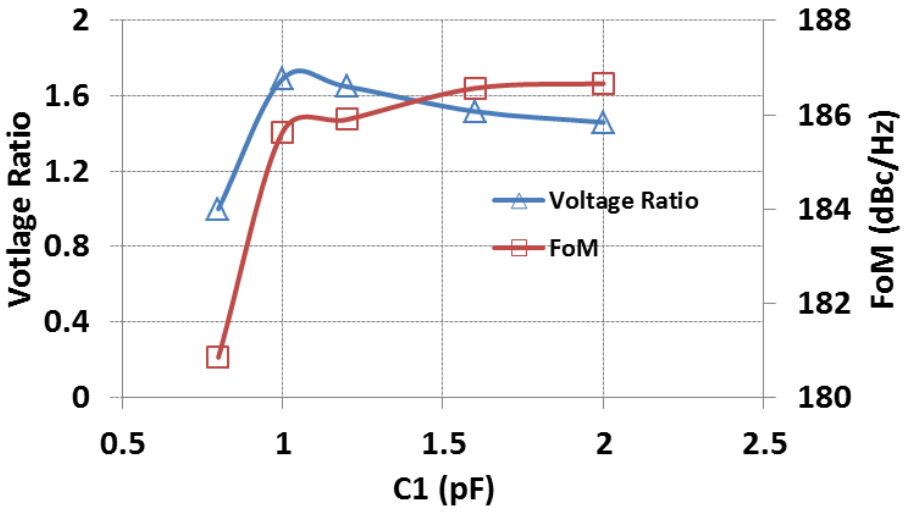
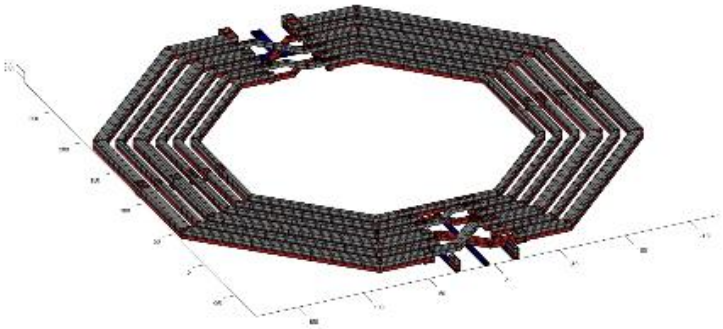


Fig. 5.20 Voltage ratio and FoM versus C_1.

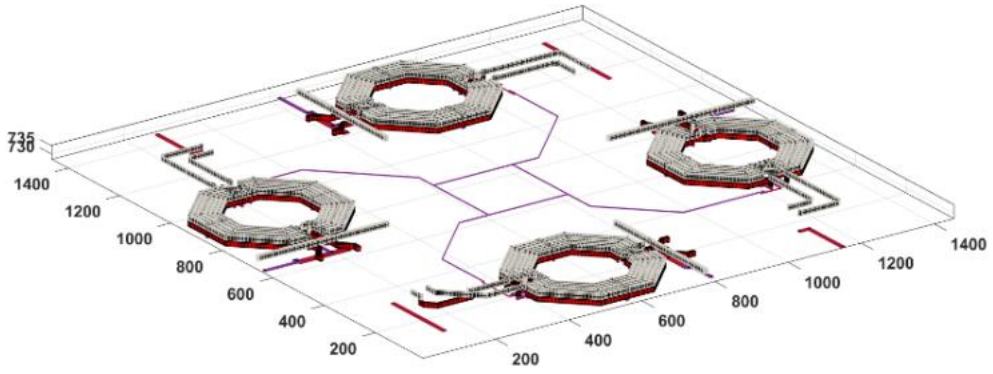
Table 5.2: Values of Capacitors and Operating Frequencies in Fig. 6.11.

C1 (F)	C2 (F)	Frequency (GHz)
802f	902f	4.835*
1p	834f	2.467
1.2p	789f	2.44
1.6p	509f	2.47
2p	340f	2.439

5.2.5 Transformer and Passive Design



a)



b)

Fig. 5.21 (a) The 3D view of the transformer and (b) the 3D view of the transformers and the passive routings.

In order to obtain the strong coupling factor *k*, a transformer with interleaved turns is used as shown in Fig. 5.21(a). The coils of the transformer are made by stacking two top metals in order to minimize the DC resistance and achieve the best possible quality factor. Simulated plots of the transformer performance are shown in Fig. 5.22, where L_1 and L_2 are 2.5nH and 7.4nH, respectively, @ 2.4 GHz.

In addition, in order to capture the capacitive and magnetic coupling among all critical routings in the layout, the EM model is created using *EMX 5.2 from Integrand Software, Inc.*. As shown in Fig. 5.21(b), the 37-port EM model includes the transformers, the routings among all oscillator cores, and the routings of control signals, the power supply, and ground traces. The reference ground plane is at the substrate of the die, and the mesh and the thickness parameters of the EM simulation are set to 1. Therefore, undesired coupling among routings can be avoided during layout design. In addition, the oscillation frequency is accurately predicted; e.g., the difference between simulated and measured frequency is only 80MHz.

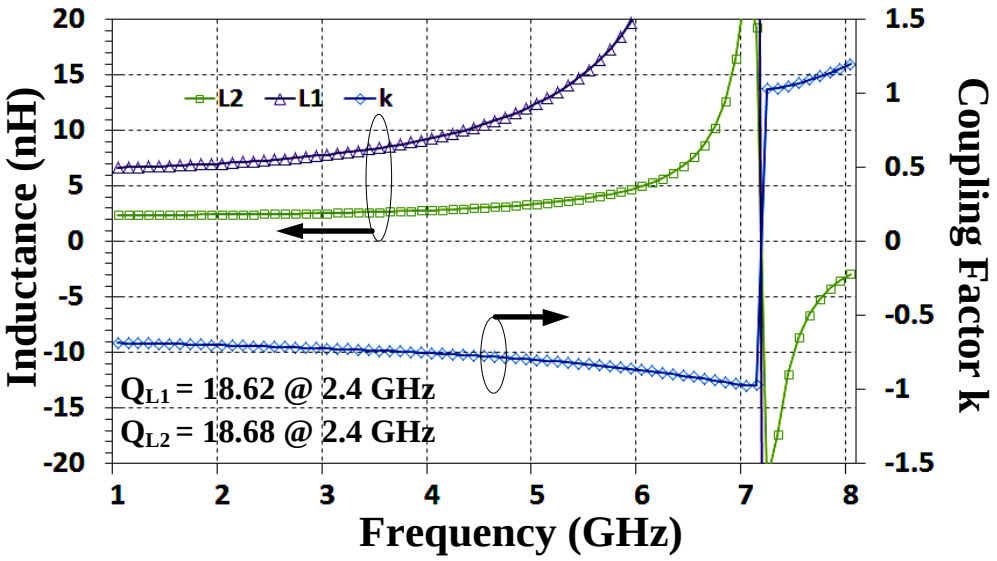


Fig. 5.22 Simulated plots of the transformer performance.

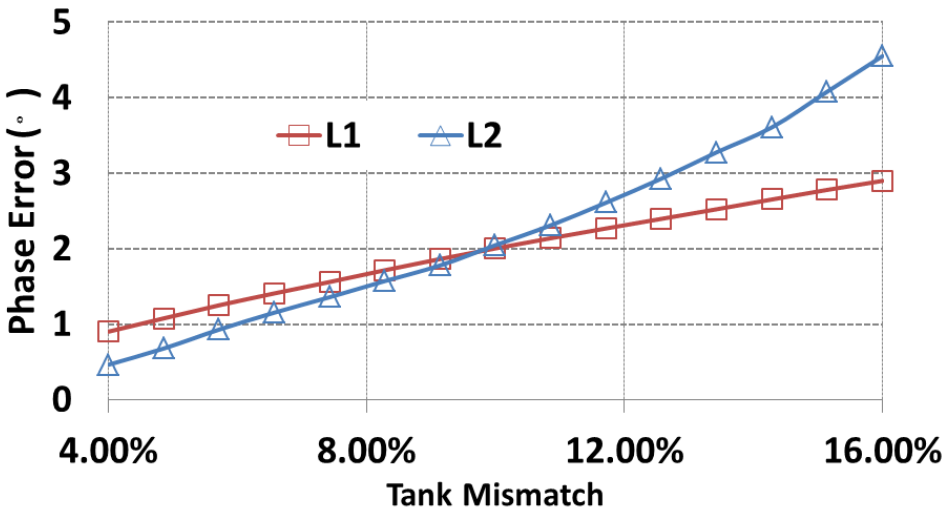


Fig. 5.23 Phase error versus mismatches in the transformer.

Since the proposed structure adopted the resonating inductive coupling technique, the mismatches are introduced to both inductors to check their sensitivity on phase error. As shown in Fig. 5.23, it is expected that, as the percentage of the mismatch increases, the phase error increases. Since the oscillation frequency in the proposed mode is mainly dominated by L_2, the phase error is more sensitive to the mismatches in L_2.

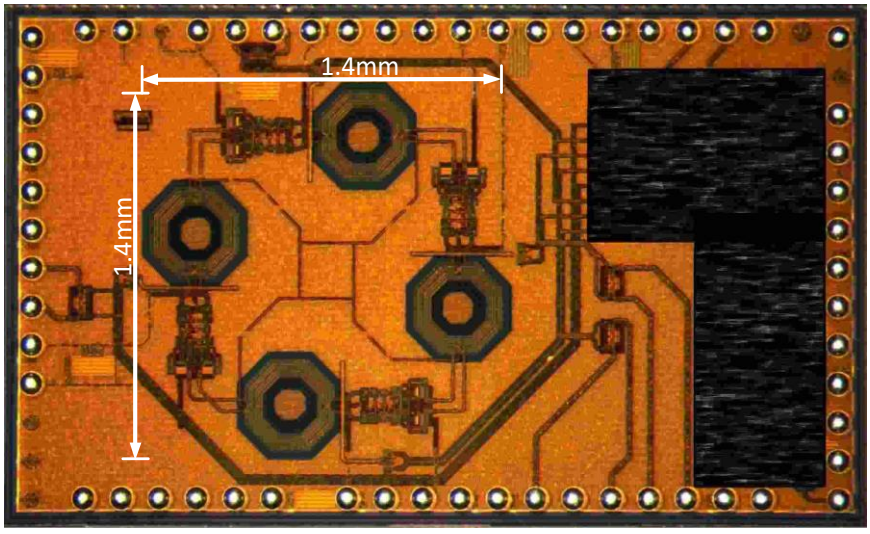
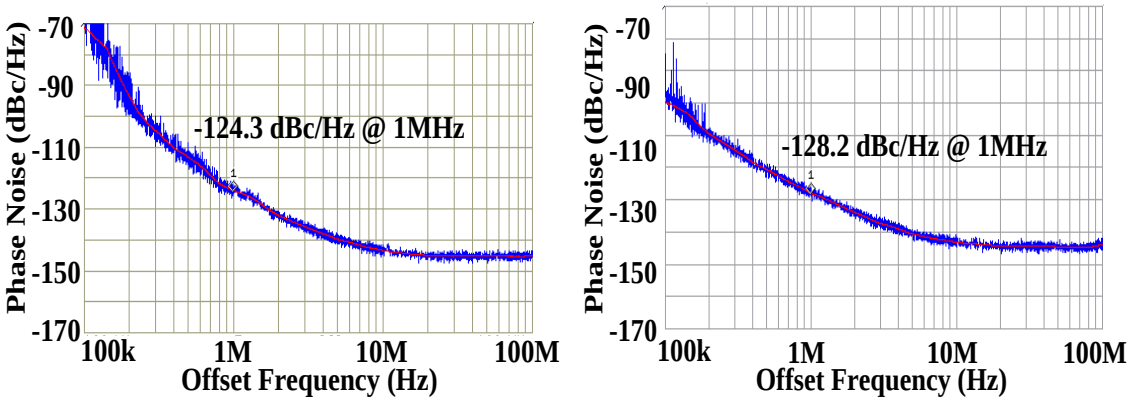


Fig. 5.24 The die photo of the proposed multi-phase VCO RFIC.

5.2.6 Measurement Results

The prototype 8-phase oscillator is fabricated in a 60nm CMOS RF SOI process. The die photo is shown in Fig. 5.24. The core area of the proposed VCO circuit is 1.4x1.4 mm^2. In order to make the connections among oscillator cores more symmetric, a circular floor plan is adopted by taking advantage of the transformers. Table 5.3 summarizes the performance of this work and provides comparison with state-of-the-art multi-phase oscillator designs.



a) b)

Fig. 5.25 Measured phase noise.

The phase noise is measured using an Agilent E4440 spectrum analyzer with phase noise option. Fig. 5.25 illustrates measured phase noise of –124.3 dBc/Hz and -128.2 dBc/Hz @ 1MHz offset from 2.41GHz with power consumption of 28mW and 60mW, respectively. Since a three-bit capacitor array is implemented for frequency tuning, the operating frequency can be digitally tuned from 1.815GHz to 2.42GHz. In addition, measured phase noise versus the operating frequency is shown in Fig. 5.26 under three different DC operating points for each core: 1) V=0.7V and I=5mA; 2) V=1V and I=7mA; 3) V=1.5V and I=10mA.

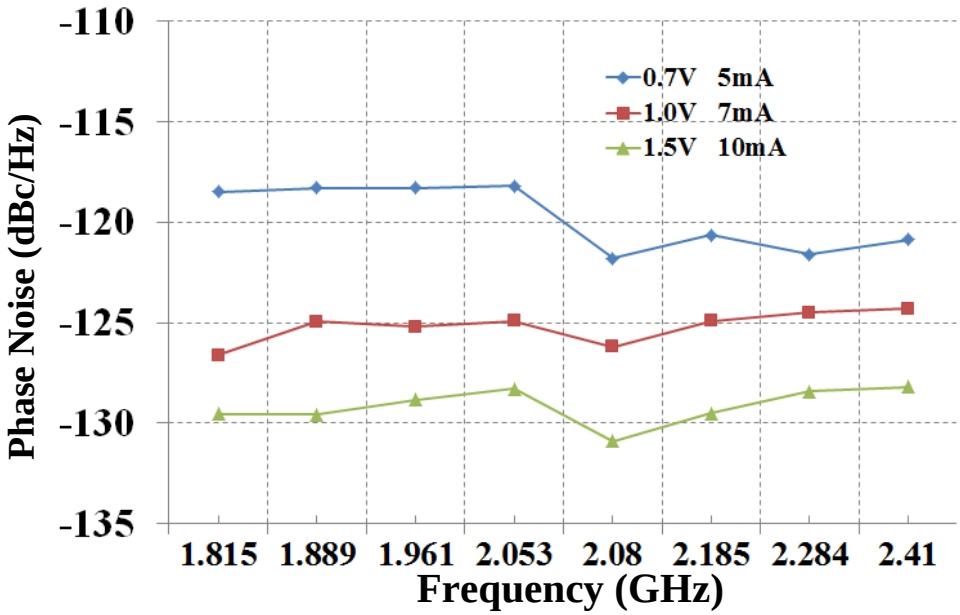


Fig. 5.26 Measured phase noise @ 1MHz offset versus the operating frequencies under different DC bias currents.

Table 5.3: Performance Summary and Comparison of Multi-phase Clock Generation Techniques

Ref.	Performance Metrics						
	Process	***Freq. (GHz)***	***P.N (dBc/Hz) @ 1MHz***	***Power (mW)***	***FoM***	***No. of Phases***	***FoM Per Phase***
This work	60nm CMOS	2.41	-120.1	14	176.3	8	185.3
			-124.3	28	177.5	8	186.6
			-128.2	60	178	8	187
[24]	65nm CMOS	4.07	-136	126	188	4	194
[25]	65nm CMOS	3.8	-123.7	7	185	4	191
[26]	0.18µm CMOS	1.1	-128	20	180.1	4	186.1
[27]	0.13µm CMOS	4.9	-112	3.2	180.8	4	186.8

The output waveforms of the proposed 8-phase oscillator are measured by a Rohde & Schwarz RTO scope, which supports simultaneous four-channel measurement. Fig. 5.27 exhibits four measured phases, out of eight phases, of the four-core oscillator, where the other four phases are the differential counterparts and not shown.

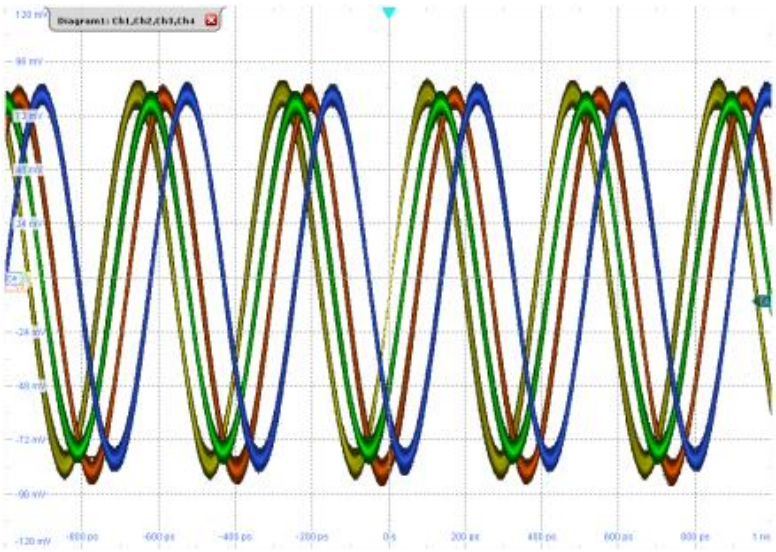


Fig. 5.27 Measured multi-phase output.

5.2.7 Conclusions

This chapter presented a novel transformer-based architecture for multi-phase clock generation. The concept of the prototype circuit is proven by both simulation and measurement. EM modeling was utilized to ensure proper coupling among routings, thus improving the correlation between simulation and measurement. The highest measured FoM is 187 dBc/Hz at 1MHz offset from the carrier, and the frequency range can be digitally tuned from 1.815 GHz to 2.41 GHz with 8 steps.

Chapter 6 Brief Introduction of A SAW-Less Reconfigurable Frontend RFIC Driven by Multi-Phase Clock

6.1 Introduction

As mentioned in the early chapter, multi-phase clock performs as an essential block in several RF applications. In this chapter, we are going to introduce one of those applications that are implemented by us to prove the concept.

Since that the number of cellular frequency bands is increasing at an amazing rate; however, state-of-the-art commercial mobile wireless devices continue to employ a dedicated filter and LNA for each frequency band; increasing the cost, complexity, and size of the receiver frontend module. These filters are usually of surface acoustic wave (SAW) or bulk acoustic wave (BAW) type, and have a fixed frequency response. Additionally, due to the significantly different technology used in manufacturing these filters, they cannot be integrated with the receiver frontend integrated circuit (IC). As a result, they introduce significant undesired parasitic elements at the input of the receiver frontend IC. LC filters, while capable of being integrated, are large, have a fixed frequency response, and exhibit poor insertion loss and out-of-band rejection.

This chapter only gives a brief introduction of the Reconfigurable Fronted RFIC, and focusing on the implementation and measurements, thus the design details will not be introduced. The 8-path filter substitutes the SAW filter, and is driven by a high-performance integrated 8-phase LC coupled oscillator whose frequency can be tuned from 1.8 GHz to 2.4 GHz; enabling realization of a tunable 8-path filter and subsequently a reconfigurable receiver frontend.

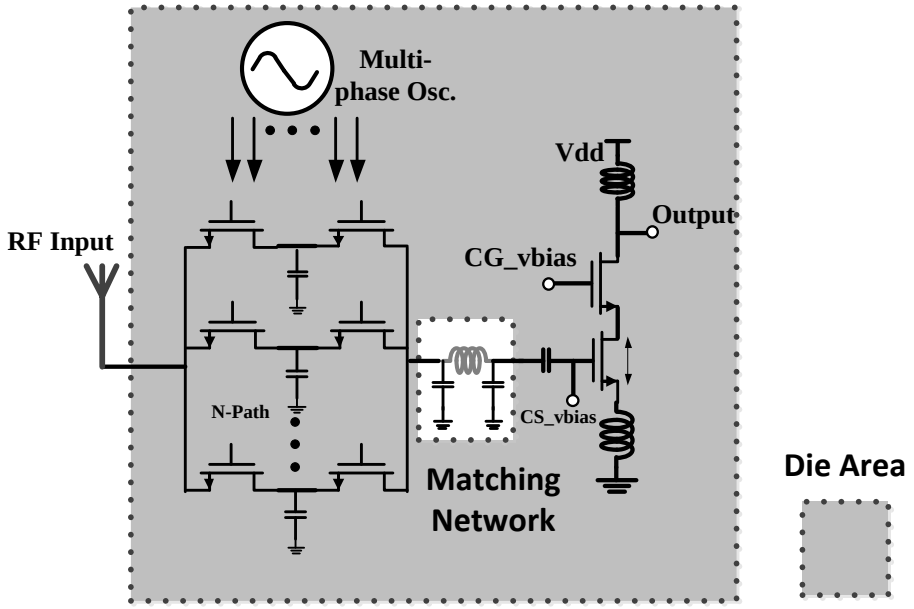


Fig. 6.1 Architecture of the proposed reconfigurable receiver frontend.

6.2 Design Architecture

Fig. 6.1 illustrates the architecture of the proposed fully-integrated reconfigurable receiver frontend. The signals generated by the integrated 8-phase coupled LC oscillator which is mentioned in chapter 5 are fed to the two-port switched-RC bandpass 8-path filter; realizing a filter with a center frequency that is identical to the oscillation frequency of the 8-phase oscillator. As a result, the input RF signal experiences bandpass filtering when passing through

the 8-path filter. The signal is then amplified by the LNA, and fed to the transceiver module, as is the case in the commercial mobile wireless devices.

6.3 Measurement Results and Comparison

Figs. 6.2-5 illustrate the performance of the receiver frontend when the oscillator operates at 1.8GHz.

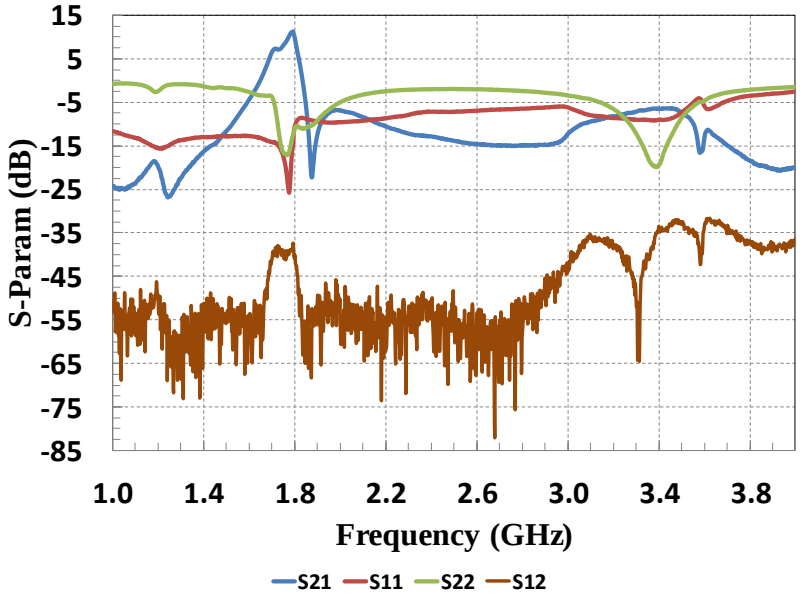


Fig. 6.2 Measured s-parameters of the reconfigurable receiver frontend.

It shall be noted that during simulation, the inverter supply voltage was 2V (i.e., pulse HIGH = 2V); however, in measurement, it could not be increased beyond 0.8V for reliable operation. This increased R_{SW} from 1.8 Ω to 3.8 Ω; resulting in significant reduction in measured gain (S21) and increase in measured noise figure. The simulated noise figure of the entire receiver frontend was sub 2dB.

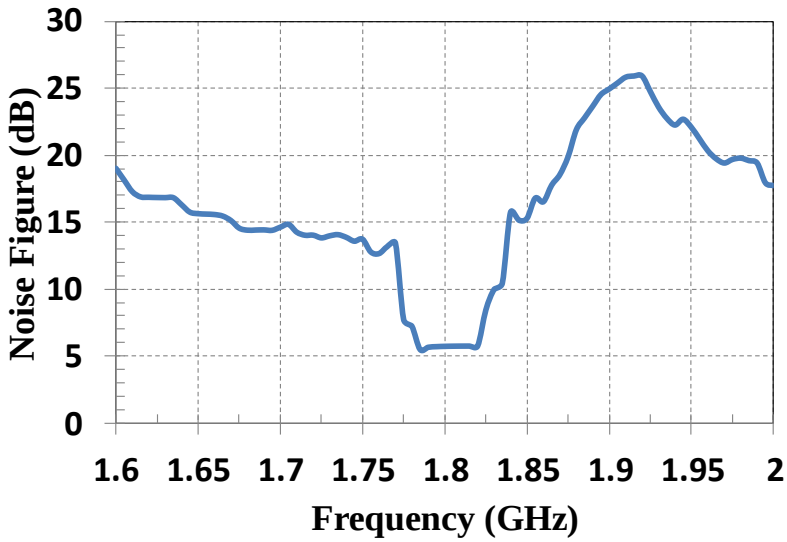


Fig. 6.3 Measured linearity of the reconfigurable receiver frontend.

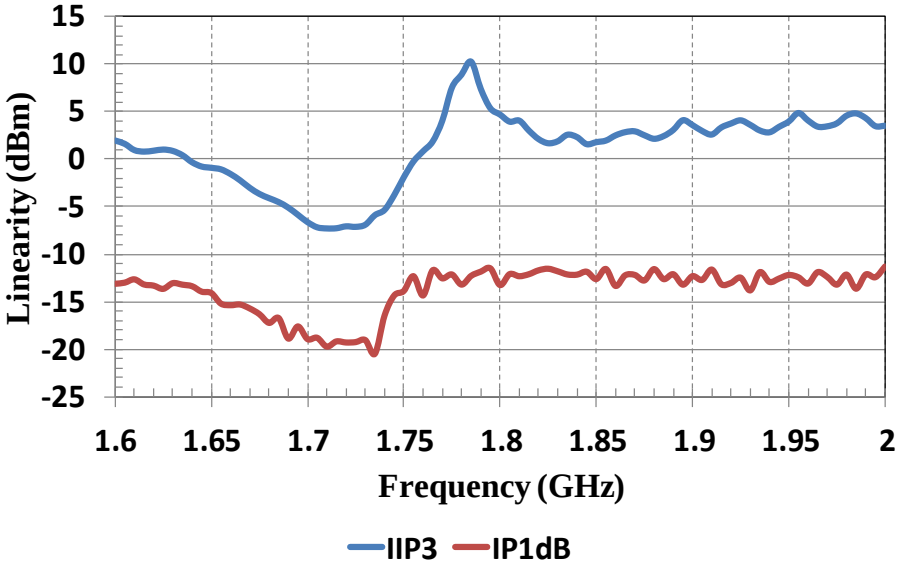


Fig. 6.4 Measured s-parameters of the reconfigurable receiver frontend.

Finally, given that the 8-path filter feeds a narrowband LNA, which requires matching and biasing for a given frequency, measured data are shown for one (1) frequency only; however, similar performance is expected for other frequencies within the 1.8 GHz – 2.4 GHz frequency range.

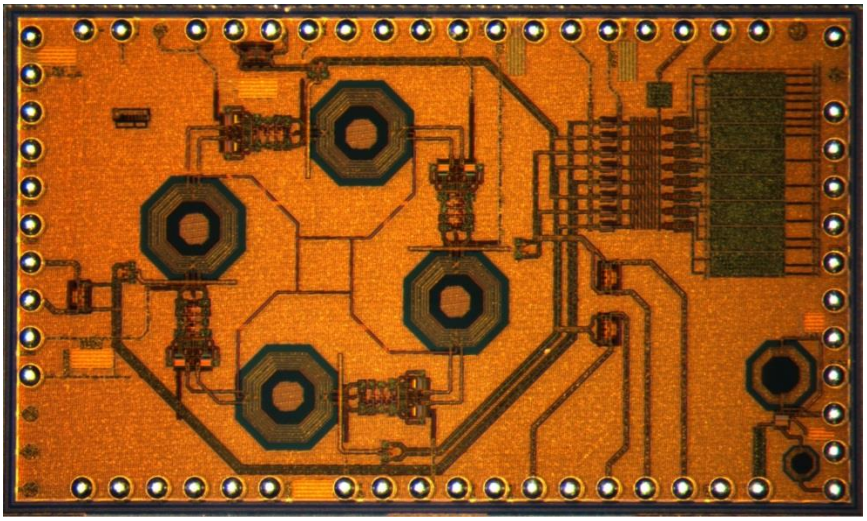


Fig. 6.5 Measured noise figure of the reconfigurable receiver frontend.

Table 6.1: Performance Summary and Comparison

	[This work]	[29]	[30]	[31]
Circuit Type	RF Frontend	Filter	Filter	Receiver
Technology	60nm SOI CMOS	65nm CMOS	65nm CMOS	65nm CMOS
Center Freq. (GHz)	1.8 – 2.4	0.1 - 1	0.4-1.2	0.05-2.5
Order of filter	8	4	4	8
3dB Bandwidth (MHz)	53	35	21	0.35-20
RF Rejection (dB)	33.2	17	55	N/A
Power gain, S21 (dB)	+11.3	-2b	-2/-3.2b	38b
IB/OOB IIP3 (dBm)	-7/+10.3	+14	+9/+29	-20/+10
Noise figure (dB)	5	3-5	10	2.9
Active area (mm2)	0.59a	0.07	0.127	0.82
Power consumption (mW)	31.6a (1.8G)	2-16	21.4	20 (2G)

[a.] Without on-chip 8-phase oscillator

[b.] Voltage gain. In [29], RF-to-baseband gain is reported.

6.4 Conclusions

Introduction, implementation, and measurement results of the reconfigurable receiver frontend utilizing two-port 8-path filter, on-chip 8-phase LC oscillator, and an LNA are presented. The entire system is proven to be functional and the performance is competitive to recent publications.

Chapter 7 Summary and Future Work

7.1 Summary of the Works

This dissertation mainly presents types of high-performance VCO and multi-phase clock generation techniques which can achieve low phase noise and low power consumption. A key contribution is combining two types of coupling techniques (capacitive coupling and inductive coupling) with various techniques used in the single oscillator to form coupled-oscillators systems and improve overall noise performance. By using Adler's equation, the equation based theoretical model of four-core system is proposed for first time, and provides more insightful explanation of behaviors of the coupled-oscillators system. In addition, detailed design methodologies for both capacitive and inductive coupling based structures are given, so that other designers can easily reuse the proposed techniques and repeat simulations.

All proposed VCOs and multi-phase generation techniques have been implemented and proved the concepts: 1) transformer-based wide-band VCO was implemented 0.18μm BiCMOS process. 2) 8.8GHz VCO was in 0.18μm BiCMOS process. 3) capacitive coupled multi-phase systems in implemented in 0.13μm CMOS SOI process while the inductive one is implemented in 65nm CMOS SOI. The necessary EM models are created to ensure the simulation accuracy and largely reduced the discrepancy between measurement and simulation.

Another major contribution is that we proposed and built the novel reconfigurable receiver frontend for the first time in this field, and proved the concept with reasonable measured results.

7.2 Future Work

The proposed multi-phase clock generation techniques are also a good candidate for RF applications over 10GHz, which could be potentially used for 5G products in the future. In addition, as number of phases and coupling cores increases, there's no need for extra phase shift to improve the phase noise and phase accuracy, unlike QVCO. However, although coupling strength and phase accuracy can be enhanced by utilizing different techniques, the phase error could cause by the asymmetric and unclean flour plan of layouts, which require more accurate EM model analysis for further compensation.

The proposed reconfigurable receiver frontend opens a new page of future frontend. As operating frequency goes higher, it becomes harder to make the filter near the antenna side meet the industrial standard. If the power consumption and chip area of the proposed type frond-end could be reduced, it will be a good candidate to replace with current widely-used structure.

References

[1] Heng-Chia Chang, Xudong Cao, U. K. Mishra and R. A. York, "Phase noise in coupled oscillators: theory and experiment," in IEEE Transactions on Microwave Theory and Techniques, vol. 45, no. 5, pp. 604-615, May 1997

[2] D. B. Leeson, "A simple model of feedback oscillator noise spectrum," in Proceedings of the IEEE, vol. 54, no. 2, pp. 329-330, Feb. 1966.

[3] Y. Wachi, T. Nagasaku and H. Kondoh, "A 28GHz Low-Phase-Noise CMOS VCO Using an Amplitude-Redistribution Technique," ISSCC, vol., no., pp.482-630, 3-7 Feb. 2008.•

[4] M. Babaie and R. B. Staszewski, "A Class-F CMOS Oscillator," in IEEE Journal of Solid-State Circuits, vol. 48, no. 12, pp. 3120-3133, Dec. 2013

[5] A. Mazzanti and P. Andreani, "Class-C Harmonic CMOS VCOs, With a General Result on Phase Noise," in IEEE Journal of Solid-State Circuits, vol. 43, no. 12, pp. 2716-2729, Dec. 2008.•

[6] A. Mostajeran, M. S. Bakhtiar and E. Afshari, "25.8 A 2.4GHz VCO with FOM of 190dBc/Hz at 10kHz-to-2MHz offset frequencies in 0.13μm CMOS using an ISF manipulation technique," ISSCC, 2015 IEEE International, vol., no., pp.1-3, 22-26 Feb. 2015

[7] S. J. Yun, H. D. Lee, K. D. Kim, S. G. Lee and J. K. Kwon, "A Wide-Tuning Dual-Band Transformer-Based Complementary VCO," in IEEE Microwave and Wireless Components Letters, vol. 20, no. 6, pp. 340-342, June 2010.

[8] W. Fei, H. Yu, H. Fu, J. Ren and K. S. Yeo, "Design and Analysis of Wide Frequency-Tuning-Range CMOS 60 GHz VCO by Switching Inductor Loaded Transformer," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 61, no. 3, pp. 699-711, March 2014.

[9] L. Fanori, T. Mattsson and P. Andreani, "21.6 A 2.4-to-5.3GHz dual-core CMOS VCO with concentric 8-shaped coils," 2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC), San Francisco, CA, 2014, pp.

[10] P. Andreani, A. Bonfanti, L. Romano and C. Samori, "Analysis and design of a 1.8-GHz CMOS LC quadrature VCO," in IEEE Journal of Solid-State Circuits, vol. 37, no. 12, pp. 1737-1747, Dec 2002.

[11] F. Zhao and F. F. Dai, "A 0.6-V Quadrature VCO With Enhanced Swing and Optimized Capacitive Coupling for Phase Noise *Reduction," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 59, no. 8, pp. 1694-1705, Aug. 2012.*

[12] A. W. L. Ng and H. C. Luong, "A 1-V 17-GHz 5-mW CMOS quadrature VCO based on transformer coupling," IEEE J. Solid-State Circuits, vol. 42, no. 9, pp. 1933–1941, Sep. 2007.

[13] B. Razavi, RF Microelectronics Second Edition, New Jersey, USA, Prentice Hall, 2011

[14] R. Adler, "A Study of Locking Phenomena in Oscillators," in Proceedings of the IRE, vol. 34, no. 6, pp. 351-357, June 1946.

[15] A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators," in IEEE Journal of Solid-State Circuits, vol. 33, no. 2, pp. 179-194, Feb 1998.

[16] Guansheng Li; Li Liu; Yiwu Tang; Afshari, E., "A Low-Phase-Noise Wide-Tuning-Range Oscillator Based on Resonant Mode Switching," Solid-State Circuits, IEEE Journal of , vol.47, no.6, pp.1295,1308, June 2012

[17] J. Maget, M. Tiebout and R. Kraus, "Influence of novel MOS varactors on the performance of a fully integrated UMTS VCO in standard 0.25-µm CMOS technology," in IEEE Journal of Solid-State Circuits, vol. 37, no. 7, pp. 953-958, Jul 2002.

[18] A. P. van der Wel, S. L. J. Gierkink, R. C. Frye, V. Boccuzzi and B. Nauta, "A robust 43-GHz VCO in CMOS for OC-768 SONET applications," in IEEE Journal of Solid-State Circuits, vol. 39, no. 7, pp. 1159-1163, July 2004.

[19] A. Scuderi and G. Palmisano, "A low-phase-noise voltage-controlled oscillator for 17-GHz applications," in IEEE Microwave and Wireless Components Letters, vol. 16, no. 4, pp. 191-193, April 2006.

[20] B. Razavi, "A study of injection locking and pulling in oscillators," in IEEE Journal of Solid-State Circuits, vol. 39, no. 9, pp. 1415-1424, Sept. 2004.

[21] A. Mirzaei, M. E. Heidari, R. Bagheri, S. Chehrazi and A. A. Abidi, "The Quadrature LC Oscillator: A Complete Portrait Based on Injection Locking," in IEEE Journal of Solid-State Circuits, vol. 42, no. 9, pp. 1916-1932, Sept. 2007.

[22] F. Zhao and F. F. Dai, "A capacitive-coupling technique with phase noise and phase error reduction for multi-phase clock generation," Proceedings of the IEEE 2014 Custom Integrated Circuits Conference, San Jose, CA, 2014, pp. 1-4.

[23] A. Mazzanti, E. Sacchi, P. Andreani and F. Svelto, "Analysis and Design of a Double-Quadrature CMOS VCO for Subharmonic Mixing at Ka-Band," in IEEE Transactions on Microwave Theory and Techniques, vol. 56, no. 2, pp. 355-363, Feb. 2008.

[24] S. A. R. Ahmadi-Mehr, M. Tohidian and R. B. Staszewski, "Analysis and Design of a Multi-Core Oscillator for Ultra-Low Phase Noise," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 63, no. 4, pp. 529-539, April 2016

[25] M. M. Bajestan, V. D. Rezaei and K. Entesari, "A Low Phase-Noise Wide Tuning-Range Quadrature Oscillator Using a Transformer-Based Dual-Resonance LC Ring," in IEEE Transactions on Microwave Theory and Techniques, vol. 63, no. 4, pp. 1142-1153, April 2015.

[26] T. Xi, S. Guo, P. Gui, D. Huang, Y. Fan and M. Morgan, "Low-Phase-Noise 54-GHz Transformer-Coupled Quadrature VCO and 76-/90-GHz VCOs in 65-nm CMOS," in IEEE Transactions on Microwave Theory and Techniques, vol. 64, no. 7, pp. 2091-2103, July 2016..

[27] Hye-Ryoung Kim, Choong-Yul Cha, Seung-Min Oh, Moon-Su Yang and Sang-Gug Lee, "A very low-power quadrature VCO with back-gate coupling," in IEEE Journal of Solid-State Circuits, vol. 39, no. 6, pp. 952-955, June 2004.

[28] Chan Tat Fu and Howard C., "A 0.8-V CMOS quadrature LC VCO using capacitive coupling," 2007 IEEE Asian Solid-State Circuits Conference, Jeju, 2007, pp. 436-439.

[29] A. Ghaffari et al., "Tunable High-Q N-Path Band-Pass Filters: Modeling and Verification," in IEEE J. of Solid-State Circuits, vol. 46, no. 5, pp. 998-1010, May 2011.

[30] M. Darvishi et al., "Widely Tunable 4th Order Switched Gm-C Band-Pass Filter Based on N-Path Filters," in IEEE J. of Solid-State Circuits, vol. 47, no. 12, pp. 3105-3119, Dec. 2012.

[31] J. W. Park et al., "Channel Selection at RF Using Miller Bandpass Filters," in IEEE J. of Solid-State Circuits, vol. 49, no. 12, pp. 3063-3078, Dec. 2014.

[32] G. Cusmai, M. Repossi, G. Albasini, A. Mazzanti, and F. Svelto, "A magnetically tuned quadrature oscillator," IEEE J. Solid-State Circuits, vol. 42, no. 12, pp. 2870-2877, Dec. 2007.

[33] F. Zhao and F. F. Dai, "A 0.6-V Quadrature VCO With Enhanced Swing and Optimized Capacitive Coupling for Phase Noise Reduction," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 59, no. 8, pp. 1694-1705, Aug. 2012.

[34] E. Hegazi, H. Sjoland and A. A. Abidi, "A filtering technique to lower LC oscillator phase noise," in IEEE Journal of Solid-State Circuits, vol. 36, no. 12, pp. 1921-1930, Dec 2001

[35] A. Nikpaik, A. Nabavi, A. H. M. Shirazi, S. Shekhar and S. Mirabbasi, "A dual-tank LC VCO topology approaching towards the maximum thermodynamically-achievable oscillator FoM," CICC, 2015 IEEE, vol., no., pp.1-4, 28-30 Sept. 2015.

[36] Guansheng Li; Li Liu; Yiwu Tang; Afshari, E., "A Low-Phase-Noise Wide-Tuning-Range Oscillator Based on Resonant Mode Switching," Solid-State Circuits, IEEE Journal of , vol.47, no.6, pp.1295,1308, June 2012

[37] F. Zhao and F. F. Dai, "A capacitive-coupling technique with phase noise and phase error reduction for multi-phase clock generation," Proceedings of the IEEE 2014 Custom Integrated Circuits Conference, San Jose, CA, 2014, pp. 1-4.

[38] R. Jiang, H. Noori, F. F. Dai, J. Fu, W. Zhou and Y. Wang, "A low phase noise 8.8 GHz VCO based on ISF manipulation and dual-tank technique," 2017 IEEE International Symposium on Circuits and Systems (ISCAS), Baltimore, MD, USA, 2017, pp. 1-4

[39] Rong Jiang, Hossein Noori, Fa Foster Dai, "A 2.33GHz, -133 dBc/Hz, 8-Phase VCO RFIC in 130nm CMOS RF SOI", 2017 Texas Symposium on Wireless and Microwave Circuits and Systems (WMCS), Waco, TX, 2017, pp. 1-4. •

[40] Rong Jiang, Hossein Noori, Fa Foster Dai, "A Multi-Phase Coupled Oscillator Using DualTank Magnetic Coupling Technique," IEEE Bipolar / BiCMOS Circuits and Technology Meeting , Miami, FL, Oct. 2017.

[41] Rong Jiang, Fa Foster Dai, Feng Zhao, Guofu Niu, Michael Hamilton, Jun Fu, Wei Zhou and Yudong Wang, "Dual-band Quad-Core Transformer Coupled VCO with Phase Noise Optimization," IEEE Bipolar / BiCMOS Circuits and Technology Meeting , Boston, MA, Oct. 2015 •

[42] Fa Foster Dai, Feng Zhao, Rong Jiang, "Low Noise Coupling Techniques for Multi-Phase Oscillators (invited paper)," in ASIC, 2015. ASICON '15. 11th International Conference on, Nov. 2015.

[43] H. Noori, R. Jiang, F. F. Dai, J. Fu, W. Zhou and Y. Wang, "A 1.8 GHz - 2.4 GHz SAW-Less Reconfigurable Receiver Frontend RFIC in 60nm CMOS RF SOI," 2018 IEEE International Symposium on Circuits and Systems (ISCAS). (submitted)

[44] Rong Jiang, Hossein Noori, Fa Foster Dai, " A 2.33GHz, -133 dBc/Hz, 8-Phase Oscillator with Dual Tanks and Adaptive Feedback," in IEEE Transactions on Microwave Theory and Techniques, 2017. (accepted)