Accelerated Life-Cycle Testing of Various Lead-Free Solder Alloys by Mechanical Shock and Thermal Cycling Techniques

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Abstract

For the last couple of decades, our inclination towards computer technology has increased broadly. Personal device assistants also known as PDA's have become a part of our daily needs. Hence, the reliability of these handheld electronic devices has become a major concern for the manufacturers as they are subjected to drop, shock and thermal cycling conditions during their day-to-day operation.

Board level drop impact testing is one of the most important methods of evaluating the reliability of electronic assemblies. The first phase of this study examines the drop impact performance of no-aged and isothermally aged flip chip packages on laminate assemblies for various doped lead-free solder paste alloys. A potential solution to replace the industrial standard solder paste Sn96.5 Ag3.0 Cu0.5 (SAC305) is carried out. The test vehicle consists of 16 ball grid array packages (BGA) which are 15mm chip array ball grid array's (CABGA208) with perimeter solder balls on 0.8mm pitch. In this experimental study, SAC305 solder spheres and SAC305 solder paste are selected to be the baseline, Solder pastes with 12 different dopants are investigated in comparison with the baseline to determine their reliability. Two sets of printed circuit boards (PCB) are manufactured, the first being no-aged and the second set of boards are isothermally aged at 125C for 6 months prior to testing. The boards are further categorized into 3 different reflow

temperatures and 2 different stencil thicknesses, 4 mil and 6 mil respectively. JEDEC BS111 test standard is followed to conduct the drop testing where the half sine impact pulse duration of 0.5ms with peak acceleration at 1500G's is maintained. The boards are subjected to accelerated life testing where the test end state is 300 drops, and the data is collected at an interval of every 20 drops. The results of no-aged and aged samples are categorized and compared using data analytics and Weibull analysis. Failure analysis is carried out to determine best solder paste, solder ball, reflow temperature profile and stencil size.

In the second phase of the study, the reliability performance of various electronic assemblies during thermal cycling testing are investigated. Best performed doped low creep lead free solder alloys designed for high-temperature reliability from phase 1 testing are used. The test boards are 0.200” thick power computing printed circuit boards with MEGTRON6 substrate material and OSP coating. Single-sided assemblies are built separately for the Top-side and Bottom-side of the boards. JEDEC JESD22-A104-B test standard is followed; the test boards are subjected for thermal cycling between the temperatures -40^{0}C and +125^{0}C respectively, 120-minute cycle profile with 45-minute transitions and 15-minute dwells at peak temperatures is maintained. The test assemblies include surface mount resistors, 5mm, 6mm, 13mm, 15mm, 17mm, 31mm, 35mm and 45mm ball grid array packages respectively. The failure data of the test

assemblies are used in this study to understand the effect of solder paste composition on the solder joint reliability during thermal cycling testing.

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List of Abbreviations

BGA	Ball Grid Array
BSE	Back-Scattered Electron
GPIB	General Purpose Interface Bus
LGA	Land Grid Array
PCA	Printed Circuit Assembly
PCB	Printed Circuit Board
PGA	Pin Grid Array
RTD	Resistance Temperature Detector
SAC	Tin (Sn) – Silver (Ag) – Copper (Cu)
SCPI	Standard Commands for Programmable Instruments
SEM	Scanning Electron Microscope
SE	Secondary Electron
SMC	Surface Mount Component
SMR	Surface Mount Resistor
SnPb	Tin – Lead
THMC	hrough-Hole Mount Component

Chapter 1. A Brief Introduction to Electronic Assemblies

1.1 Electronics Packaging

Electronic Packaging Industry is the largest industry in the world [1]. The term of "Package" in electronic manufacturing industry refers to a supportive case that encloses a semiconducting material to prevent it from corrosion and physical damages. Electronic packaging refers to the method of enclosing, protecting or providing physical structure to either electronic components, assemblies of components or finished electronic devices. The manufacturing of this package is known as electronic packaging.

The manufacturing phase of an integrated circuit can be divided into two steps. The first, wafer fabrication, is a sophisticated and intricate process of manufacturing the silicon chip. The second, is a highly precise and automated process of packaging the die. Those two phases are commonly known as "Front-End" and "Back-End", respectively. Each electronic package should provide circuit support and protection, heat dissipation, signal distribution, manufacturability, serviceability and power distribution. This is a multi-disciplinary subject among Mechanical, Electrical and Industrial Engineering, Chemistry, Physics and even Marketing [2]. Market dictates the demand, then the engineers design, chemists and physicists investigate new materials and methods and Industrial engineers work on the manufacturing of the parts. Although more functional and smaller packages are desirable, they also are required to be qualified based on

reliability and feasible pricing. More functional devices produce more heat and require complex cooling system which both increases the price and complexity. There is a tradeoff among functionality, reliability, size and price which always makes challenges for engineers.

An IC chip which is enclosed inside the package is a very delicate and complex device. It has thousands of transistors and I/Os (input/output links) which are spaced very closely (within nanometers) to reduce electrical delay and current leakage. Contrary to popular opinion, IC chips are not being shrunk in size simply because they need to be made more compact. The primary purpose of miniaturization is to reduce electrical delay. When two switches/transistors/logic devices communicate with each other, their speed of communication depends on how far they are from each other. Higher the distance, slower the communication (which will increase computation speed in turn), it is essential to bring the logic devices as close to each other as possible [3]. This is the primary goal of miniaturization. An inevitable consequence of miniaturization is that billions of transistors are placed on a single chip, which means lots of input/output links (I/Os) inside a single chip which need to be connected to other devices such as memories, connectors, power devices etc. One of the biggest challenges in the electronics industry is figuring out how to protect these delicate ICs, at the same time successfully connecting all the I/Os from the chip to the board and to other chips. Scaling the interconnects to achieve reliable connectivity with acceptable delay is the main challenge. Figures 1.1&1.2 show the hierarchy of packaging

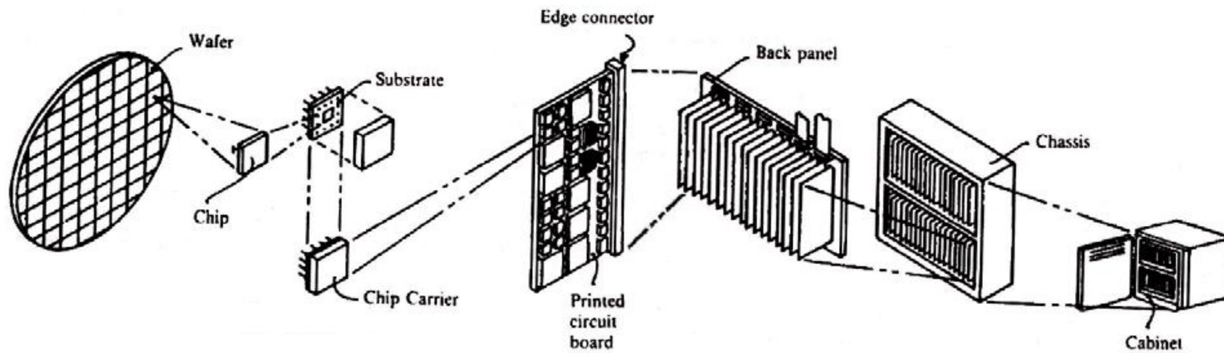


Figure 1.1 Levels of Packaging. Adapted from [2]

1.2 Packaging Classification

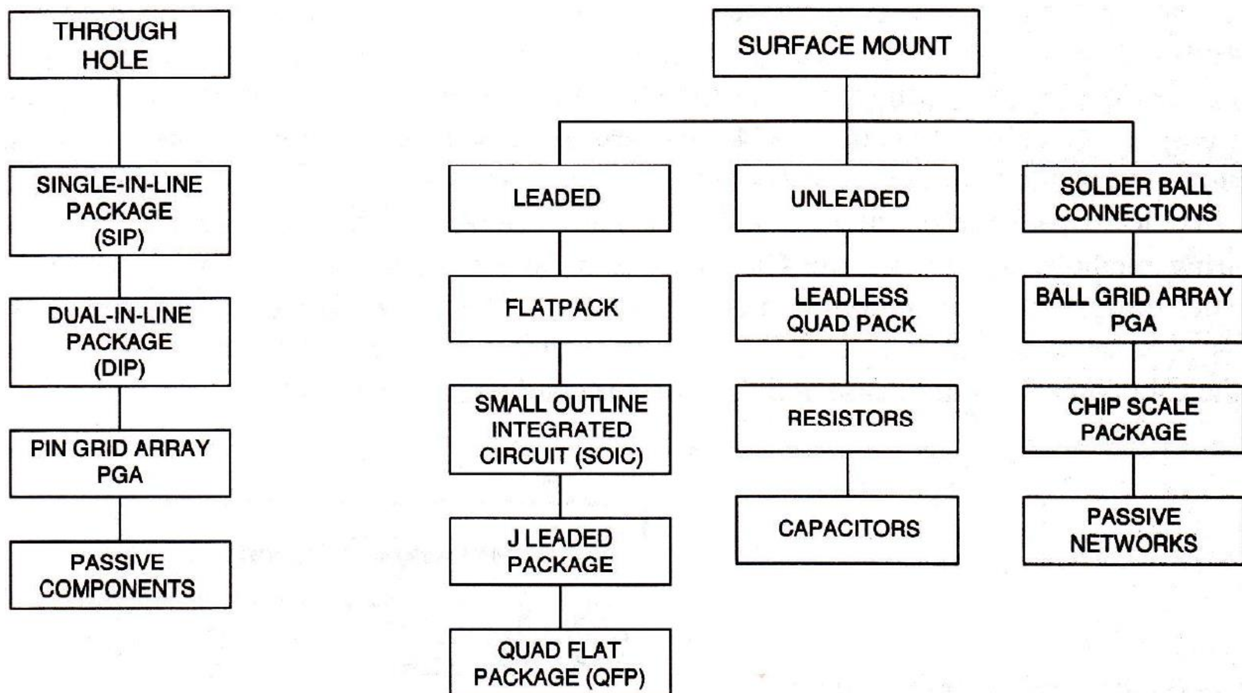


Figure 1.2 Packaging classification [2]

1.2.1 Through Hole Mount Technology

It is a mounting scheme used for electronic components that involves the use of leads on the components that are inserted into holes drilled in printed circuit boards (PCB). This is followed

by soldering (adding solder around) the component leads, which joins them to the appropriate metal traces of the PCB [3]. The principal method of soldering in through-hole mount assembly is ‘wave soldering’ technique, which involves a standing wave of molten solder. The PCB is passed over the wave, soldering all the through-hole connections at once. The electronic packaging industry was quick to adopt wave soldering technology, as the throughput advantages was overwhelming. A typical THMT Component is Dual In-Line Package (DIP). Figure 1.3 shows an example of a DIP, and its side-view [4].

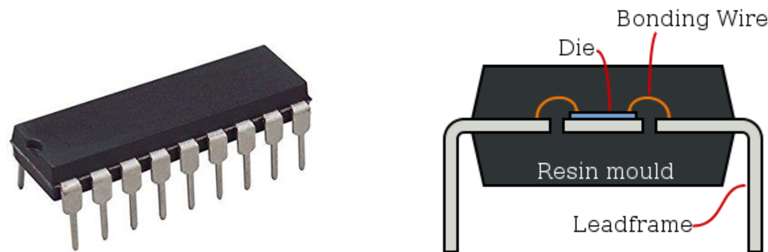


Figure 1.3 DIP and Its Side View [2]

While through-hole mounting provides strong mechanical bonds when compared to SMT techniques due to its lead frame structure effectively taking up stresses resulting from thermal expansion in the PCB substrate, additional drilling required makes the boards more expensive to produce. They also limit the available routing area for signal traces on layers immediately below the top layer on multilayer boards since the holes must pass through all layers to the opposite side. Through-hole mounting techniques are now usually reserved for that which require the additional mounting strength, or for components such as plug connectors or electromechanical relays that require great strength in support. On the downside, it became clear that a new technology was needed to achieve higher I/Os, component densities and keep pace with IC advances.

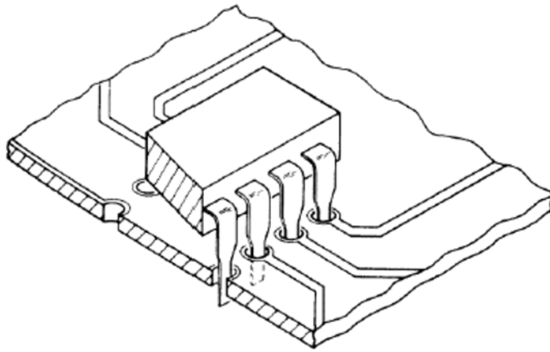
1.2.2 Surface Mount Technology

The increase in demand for the leads and surface area constraints in the board led to development of Surface Mount Technology. It is a method for constructing electronic circuits in which the components are mounted directly onto the surface of the printed circuit boards. This largely replaced the through-hole technology construction method of fitting components with wire leads into holes in the circuit board. An SMT component is usually smaller than through-hole component because it has either smaller leads or no leads. SMT components can be placed on both sides of the PCB since no through-holes are required, which increases the usage of the surface area significantly.

The electrical performance of surface mount interconnects is typically better due to the shorter leads employed. On the other hand, thermal management can become more complicated, as thinner leads – necessary for finer pitch I/O – also have higher thermal resistance [5]. Also, with less solder for each joint, reliability of solders joints is more of a concern [6].

SMT components normally have flat profile made of tin-lead, silver, or gold-plated copper pads without holes, called solder pads. Solder paste is first applied to all the solder pads using a screen printing process. These are then conveyed into the reflow soldering oven where the component leads are bonded with the pads on the circuit board [5]. Figure 1.4 shows THMT vs SMT

Through-Hole Mount Attachment **Surface Mount Attachment**



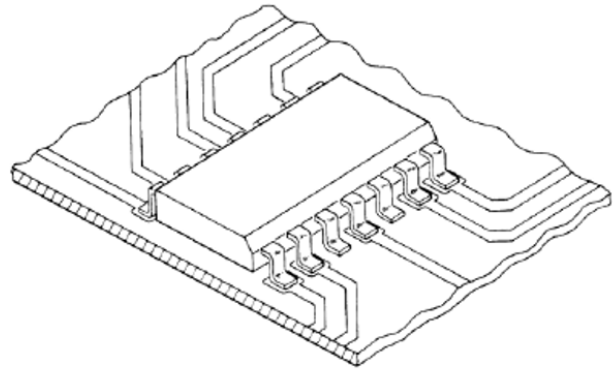


Figure 1.4 Through-Hole Mount Attachment vs. Surface Mount Attachment. Adapted from [2]

1.2.3 Leaded Components

There are variety of leaded components: Gull Wing and J-Lead are the most common ones. It can be noticed that a Gull Wing device is a surface mount component and has leads folded out from its body in the shape of a 'L', while a J-leaded device is a surface mount component that has it's leads folded under its body in the shape of a 'J' [5]. Finally, all the THMT components are leaded components. The figure 1.5 shows some of the leaded components that are widely used.

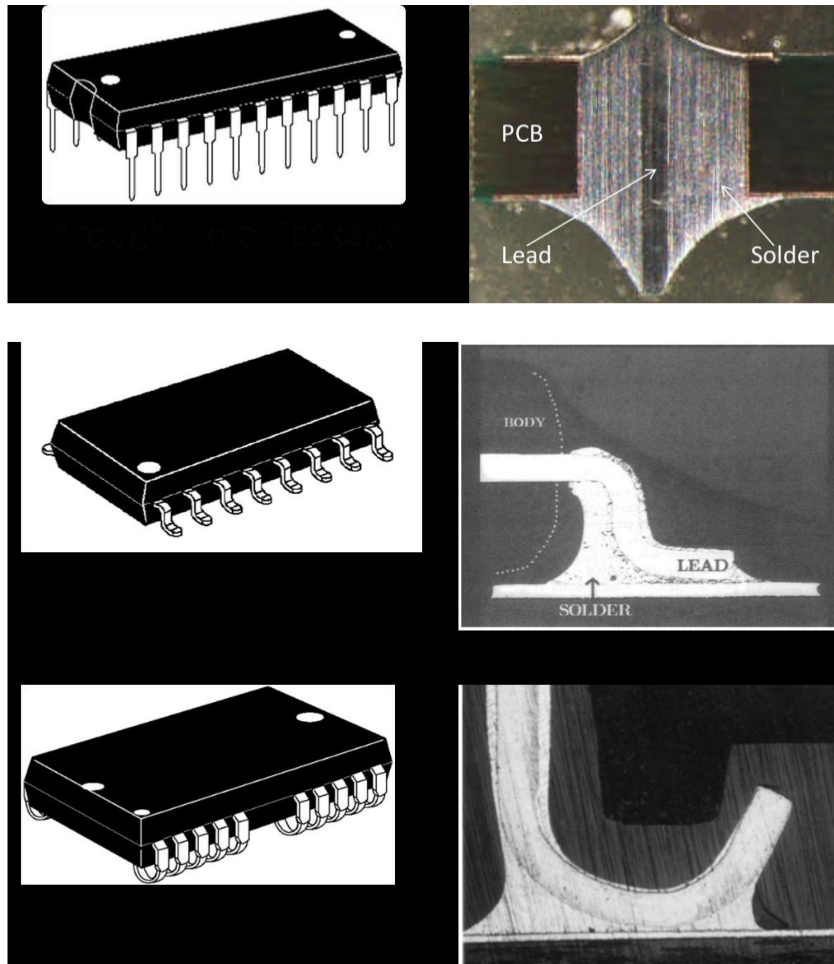


Figure 1.5 DIP, Gull Wing Component and J-Lead Component [2,5]

1.2.4 No-lead Lead-Less Components

Components with no leads are called Lead-Less or No-Leads components. There are a variety of lead-less components common to surface mount assembly. These include the Surface Mount Resistor (SMR), Metal Electrode Leadless Face (MELF), and Quad Flat No-Lead (QFN) packages. These components are designed to be placed flat on the PCB. They have bare metal terminations on the bottom of the component and are placed directly onto the solder paste printed on the copper pad of PCB [5].

SMT components are usually plastic encapsulated, in which the die is wire bonded with planar copper lead frame. The copper lead frame forms perimeter lands on the component bottom to provide electrical connections to the PCB. Flat no-lead Components usually are square or rectangular, and includes an exposed thermal pad at center of the component bottom to improve heat transfer out [7]. Figure 1.6 shows the side view of a QFN Component.

The advantages for No-Leads Components include reduced lead inductance, a small sized (near chip scale) footprint, and low weight, so that they have good thermal and electrical performance. Disadvantage for No-Leads Components, especially the one with small sized of exposed contact as well as large area of exposed thermal pad that they are easy to float on the pool of molten solder under the thermal pad during reflow assembly.

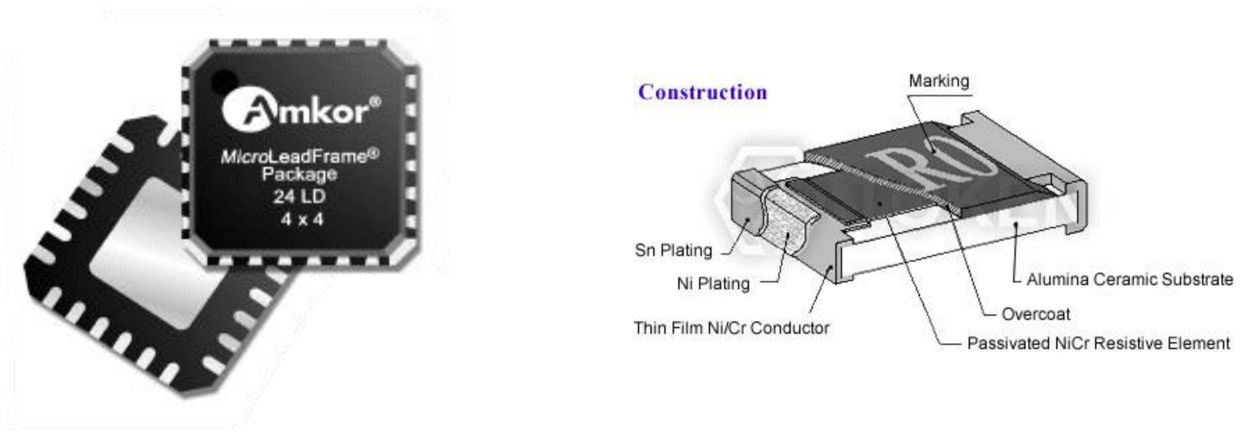


Figure 1.6 QFN Component and SMR Component [116]

1.2.5 Area Arrays

These types of SMT Components have finer pitch I/O interconnects which allows greater number of connections than lead type component where only the outer perimeter is used [8]. Their need increased as the requirement for advanced IC components continue to grow. Since no through-holes are needed, I/O's can be installed in a full 2-dimensional lattice, or Area Array, under a surface mounted component. For a square component with n leads along each edge, this approach increases the number of potential I/O channels from approximately 4n to n2 (although, depending on the component, I/O may cover only part of the allowable area). Area arrays allows one to dramatically increase I/O capabilities without having to decrease the lead pitch [9].

However, finer pitches come with a range of manufacturability concerns, including increasing fragility of finer-pitch leads and "bridging" between closely spaced contact pads on the Printed Circuit Boards. Eventually, it becomes difficult to further decrease the lead pitches for standard SMC chip carriers.

1.3 Ball Grid Array

Ball grid array or BGA packages are predominant area array packages, they do not have solderable leads in a few straight rows. Instead, their leads are solder spears applied to the grid of contact pads built into the bottom of the component. These solder bumps are placed onto corresponding solder paste deposits as if they were component leads. Typically, during reflow soldering, the bumps melt and wet together with the solder paste to form a hamburger shaped solder joint as shown in the figure 1.7 thus eliminating the lead coplanarity issue. On the contrary, BGA Components are not mechanically compliant, given that the solder balls are as flexible as leads are. These joints are prone to failure due to CTE mismatch between PCB and BGA when the

package is exposed to thermal or mechanical harsh environments. This reliability issue can be overcome in a process called Underfilling, where epoxy material is filled under the BGA after soldering it on to the PCB.

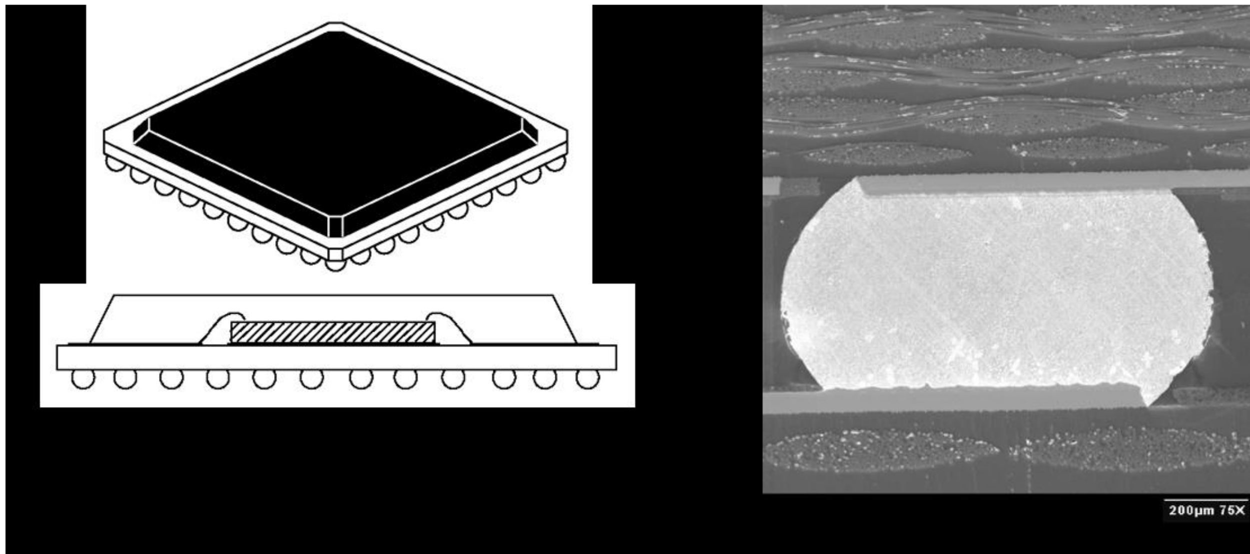


Figure 1.7 BGA package and Solder Joint [5].

A variety of BGA packages are available, including Plastic BGA (PBGA), Ceramic BGA (CBGA), Thin Chip BGA (CTBGA), Very Thin Chip (CVBGA), Super-BGA (SBGA), and Flip-Chip BGA (FCBGA) packages, among others. Figure 1.8 shows some of the cross-sectional views of some components listed above.

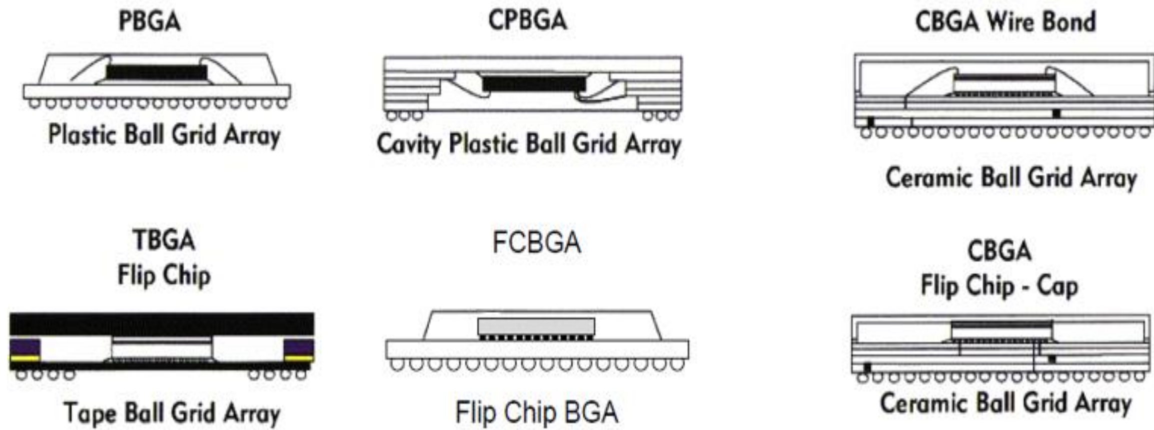


Figure 1.8 Some Ball Grid Array Structure Options [5]

Another area array is the Pin Grid Array, where thick metal pins (like through-hole leads) are attached in lieu of solder spheres or columns [2,5]. This type of package often used in conjunction with socket into which the pins are inserted.

Compared to traditional DIP, PGA allows for more I/O. There are different types of PGA, including Plastic Pin Grid Array (PPGA), Flip-Chip Pin Grid Array (FCPGA), Ceramic Pin Grid Array (CPGA), and Organic Pin Grid Array (OPGA).

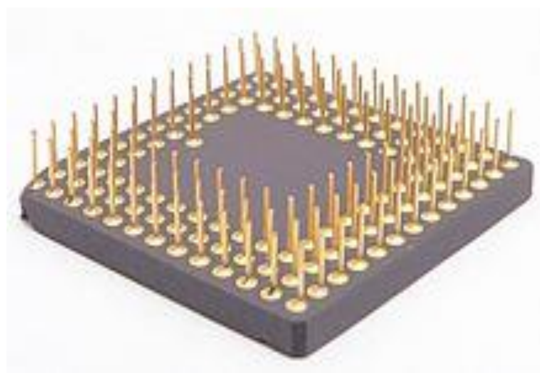


Figure 1.9 A PGA Component Used in Motorola 68020 Microprocessor [116]

1.4 Substrates for Electronic Packaging

Substrates used for PCB manufacturing is a multibillion dollar industry. They can be typically classified into Rigid Laminate, (Organic) Flexible, or Ceramic, with Metal Core Substrates as an additional option. Each substrate type exhibit different properties and the selection of an appropriate one depends on the requirement. The primary requirement to be considered during substrate selection is PCB's coefficient of thermal expansion. Some of the other properties are listed below –

General properties	Material properties
Meets Performance Requirement	Coefficient of thermal expansion
Cost	Glass Transition temperature
Ease of use	Stiffness
Durability	Strength and toughness
Machinability	Good Static dissipation
Dimensional stability	Reduce creep and warp
Resistance to moisture	Dielectric performance

Typically, a PCB consists of a non-conductive substrate, on which conductive traces are etched from copper sheets which are laminated. PCBs can be single sided, double sided, or a multi-layer of laminated substrates. Conductive parts on different layers are electronically connected with each other through vias. A via can be through hole, or a blind one exposed on one side, and or sometimes buried inside to connect internal layers without being exposed on either surface [10]. Figure 1.10 shows a cross-section view of a PCB with all three types of vias.

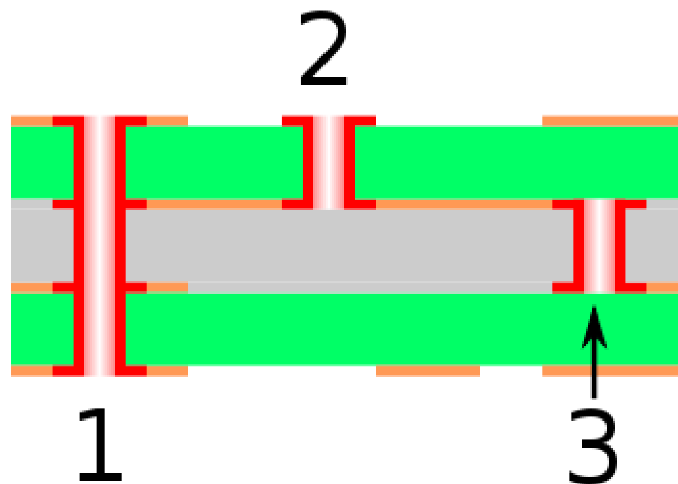


Figure 1.10 Cross-section view of a PCB with different types of vias: (1) Through hole; (2) Blind via; (3) Buried via. The green and gray layers are non-conducting, while the thin orange layers and vias are conductive.

Laminate substrates are most widely used ones in the industry. Ceramic substrates are normally used with ceramic components, as the CTE match is ideal between them. Flexible organic substrates are used to form complex circuitry. They are manufactured by attaching a thin metal foil to a flexible film using an adhesive. Constraining core substrates are metal core substrates. They incorporate a core that is CTE matched to components and other structures. The metal core used in these would be metal sheet or metal matrix composite material.

1.4.1 Laminate Substrates

Most commercial applications use rigid laminate substrates. They are typically constructed with many layers. The raw materials involved in the manufacturing process are Glass Fabric, Resin and Copper Foil. The different raw materials are rolled onto each other to form a strong sturdy single layer. This process is called impregnation. The layer that comes out of the impregnation process is treated to make the material homogenous. The lamination lay-up is followed by another process where the copper foil is embedded to the Pressplates and Presspregs. The different layers of laminates obtained are compressed and pressed by applying pressure and heat for a long period in the Laminate Pressing step. The resulting product is an inseparable single unit product. The resulting layers are broken down in the breakdown process. The core sheets are (potentially) clad in a copper layer that is photolithographically defined to create the appropriate electrical circuitry or thermal distribution layers. The finished product is subjected to lamination process, through-holes are drilled and plated to allow for vertical electrical or thermal interconnects [2,5,11] and a final inspection to check for errors.

The primary advantage of utilizing laminate substrate is higher layer counts which help in increasing the routing capability of the embedded components and the component density. The main advantage that pushes the laminate substrate printed circuit boards to the forefront is the relatively lower cost of manufacturing and better utility. [2]

1.4.2 Solder mask

Copper traces on the PCB must be protected from oxidation, corrosion and bridging. Solder mask is a thin lacquer like layer commonly made of acrylic or epoxy polymers coated where no electrical contact is needed on the PCB [2,5,11].

One of the purposes of the solder mask is to prevent wetting of solder onto the copper during reflow, the contact pads ("lands") on the Printed Circuit Board surface must be kept clear of solder mask. There are two types of solder mask designs for a PCB. One is to print the solder mask around the copper pad and it is called Non-Solder Mask Defined(NSMD). The other is to print solder mask such that just the desired pad area is exposed and it is called Solder Mask Defined(SMD). In NSMD, a small space is left while printing the mask around the copper pad, whereas in SMD the desired exposed area is smaller than the copper pad. Figure 1.11 shows difference between NSMD and SMD PCB design.

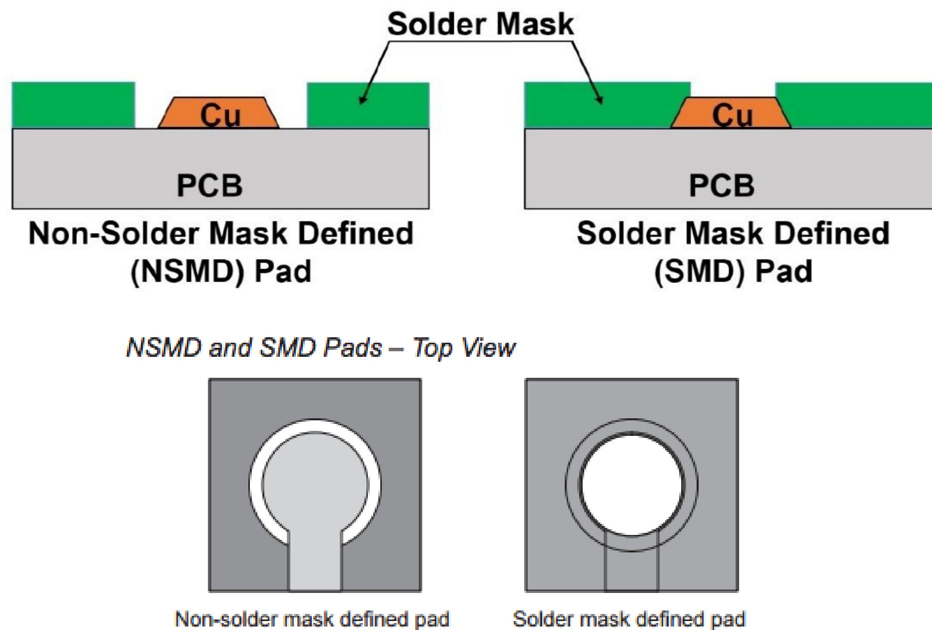


Figure 1.11 NSMD versus SMD PCB lands.

1.4.3 Surface Finishes

Surface finishes are applied over the exposed copper pad areas as the solder mask can only protect copper traces. This finish allows them to be preserved as either conductive test points, fiducials or lands for solder wetting. Besides protecting copper pad from corrosion and oxidization, surface finish can also increase solderability of solder paste to the copper pad, by dissolving the outermost layer of surface finish during reflow or wave soldering. A variety of different surface finishes have been developed over the years and some of them are discussed below [2,5,11,12].

Hot Air Solder Leveling (HASL): In this process the PCB is immersed into a molten tin-lead bath. The solder clings on to the exposed metal surfaces that are not covered by the solder mask. Hot air "knives" are used to blow off the excess solder, clearing the through holes and vias and leaving only a thin coat on the copper surfaces. This is one of the least expensive surface finishes available and facilitates excellent solderability. This process was primarily used with tin-lead baths, and proved challenging to use with lead-free solders as their melting temperature was higher. Another drawback of this process is the coating is not even and the coplanarity of the surface is poor. Also, thermal shock damage to the PCB is a common issue therefore, the popularity of HASL has fallen significantly in recent years.

Organic Solderability Preservative (OSP): is an organic compound-based anti-tarnish coating. It uses a thin protective layer (typically 0.7-1microns) of carbon-based organic layer to protect the copper pad oxidation and contamination. OSP finish is the leader in low cost surface finishes, has superior co-planarity and solderability, facilitates easy visual inspection and multiple reflow capabilities [2,5]. Disadvantage of OSP finish including poor shelf life, sensitive to handling, and difficulty during circuit testing because the coating is non-conductive.

A variety of alternative surface finishes are available to support the production of lead-free assemblies. They are more compatible with newer packages and have superior planarity and uniformity. They rely on deposition of one or more metals using Electroplating, Electroless Plating, and Immersion Plating. A buffer solution or a plating bath is used into which ions of desired metal are dissolved. When the boards are dipped the metal ions impinge the exposed metal surface and bond in place to produce the coating. Below is the list of alternative surface finishes available -

- Immersion Tin (ImSn, ImmSn, ISn)
- Immersion Silver (ImAg, ImmAg, IAg)
- Electroless Nickel Immersion Gold (ENIG)
- Electroless Nickel/Electroless Palladium/Immersion Gold (ENEPIG)

PCB Surface finishes are chosen depending on the application, cost, quality and reliability. Every Surface Finish has its strengths weaknesses; the Table 1.1 lists some of the properties of Surface Finishes discussed in this topic.

Type	Planarity	Solderability	Al Wire Bondable	Au Wire Bondable	Contact Surface
HASL	POOR	GOOD	NO	NO	NO
LFHASL	FAIR	GOOD	NO	NO	NO
OSP	GOOD	GOOD	NO	NO	NO
IMM Ag	GOOD	GOOD	YES	NO	NO
IMM Sn	GOOD	GOOD	NO	NO	NO
ENIG	GOOD	GOOD	YES	NO	YES
ENEPIG	GOOD	GOOD	YES	YES	YES
Elec Au	GOOD	GOOD	YES	(soft only)	YES

** Finish cost factor only, all other features being equal.*

Table 1.1 Summary of Properties of Surface Finishes

1.5 Electronic Packaging Trends

The achievements in electronics packaging so far has helped to reach higher state of integrity by utilizing new materials, employing more accurate processes and configurations. This needs a new methodology to electronic design and layout of semiconductor chips, circuits and systems. In this section the roadmap of modern packaging that shows the path to system integration is presented [2].

"Electronic packaging is traditionally defined as the back-end process that transforms bare integrated circuits (IC) into functional products." [15] Electronics packaging technologies are not mature technologies, and many technological aspects will still affect the application possibilities. Strongly, it can be stated that by technological driving forces, the electronics and information technologies have changed and it will change the manufacturing technologies [13]. The electronics industries through the past few decades have tried to reduce the dimensions of components as well as complete electronics systems. To reach a reliable and cost-effective system, the size and weight is being reduced by employing lower voltages and higher speeds. The recent progress in electronic manufacturing tends includes achievements in higher integration such as better materials, process, and configurations which leads to the design of more efficient and better layout of semiconductor chips, circuits and systems. Furthermore, the quality and cost should be considered as essential factors. Since all the components such as semiconductor chips and passives must be placed inside the system, all the concerns such as electrical (signal processing), physical (heat transfer and cooling), mechanical, chemical and technological should be solved [14].

In figure 1.12 and 1.13 shows the integration development of packages where the industry moved from Dual in Line (DIL) to Leaded Chip Carrier (LCC) and other (PGA, QFP etc.) which cause dramatic changes in components such as microprocessors, memories, etc.

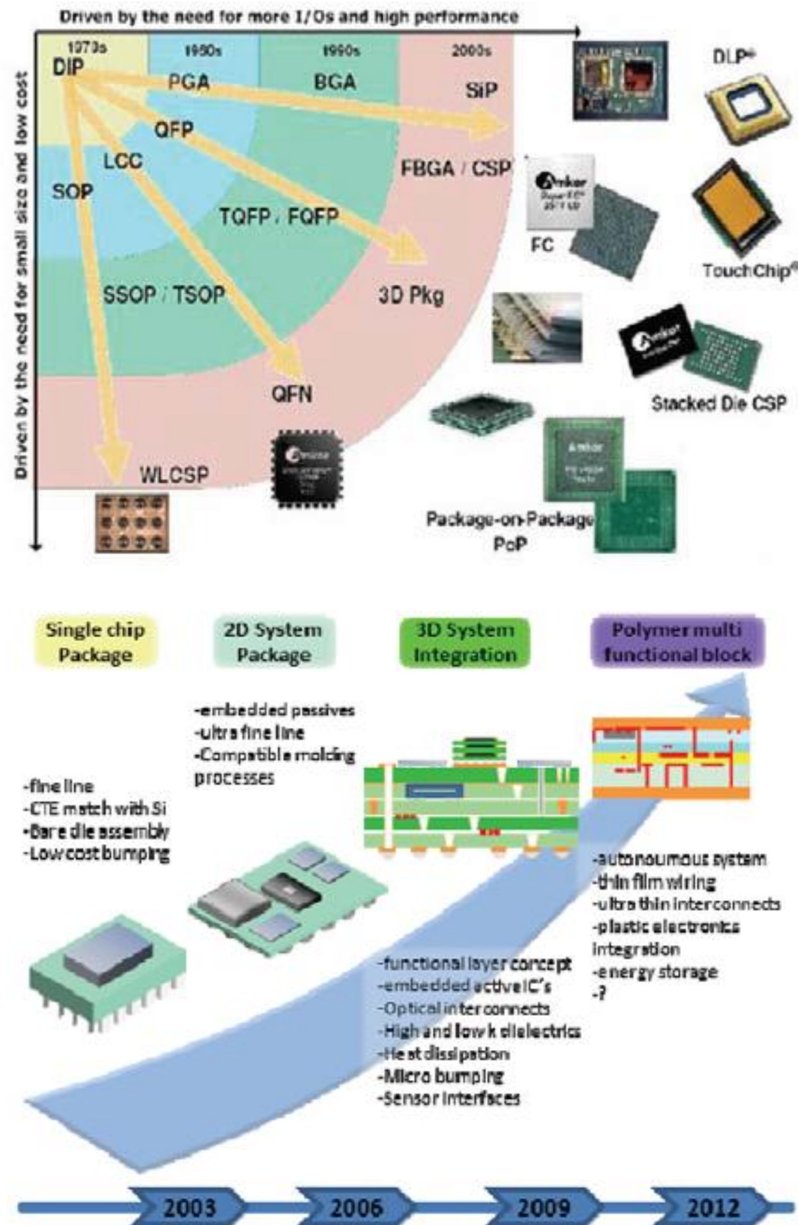


Figure 1.12 Integration development of packages in the last decades [14,15,16]

In the past, two types of packaging have been used for semiconductor chips non-hermetic (plastic) and hermetic (metal and ceramic). Plastic packages were more commercial applications due to low cost (one half to one tenth the cost of ceramic and metal packages) and small size comparing to the ceramic and metal packages. While the Hermetic packages have been used mostly for military, space and medical applications because of their perceived reliability advantage over plastic packages [14]. The new packaging process focusing on three-dimensional (3-D) packaging including interconnection to provide better electrical performance and packaging density comparing to the two-dimensional (2-D) packages which was popular in the past is here.

Besides, three-dimensional packaging has potential to increase the density more than 50 times by stacking ICs. Figure 1.13 shows the packaging trends through the time: single chip packaging, 2-D system packaging, 3-D system packaging and future polymer multifunctional solution [14]. Eventually, electronic packaging is developing very fast through the coming soon future [14]. Moreover, the cost is focused more today as the most significant factor with increasing the number of elements on chip [14].

In another study, Nakamura and Katogi studied the evolution of packaging technology through the time. As shown in figure 1.14, the trends of semiconductor packages have been traced differently in their work. They divided the trends into three main categories: Logic IC; System in a Package (SIP); and Memory IC [17]. Moreover, they suppose that three-dimensional packages will be popular in near future. Good example for three dimensional packages would be Package on Package (POP) for stacking logic and memory IC, stacking Multi Chip Packages (MCP) for stacking multiple semiconductor chips, and Chip on Chip (COC) for connecting two semiconductor chips directly [17]. Typical POP stacks the memory packaging on the logic packaging which is popular for mobile information terminals such as smartphones. BGA can be

good example of POP which is used for lower packaging. Moreover, the materials have become thinner according to the requirements of structural components. Besides, packaging wrap and reflow resistance have been focused to improve the packaging process. For example, the rate of pin count increase is 8% to 11% per year since 1997; the cost per pin has been reduced only 5% per year; and the original size from year 1997 to 2001 decreased to 60%. In general, electronics technology will continue to progress in various fields such as robotics, automobile industries, medical equipment etc. and its progress is very depend on many factors, but one of the most important one is development on materials technology in 20 years ahead which based on chemistry and some other technologies such as: polymer synthesis technology; interface control technology in molecular units; bonding technology for different kinds of materials; development of signal transmission technology; and super-fine photosensitivity technology [17].

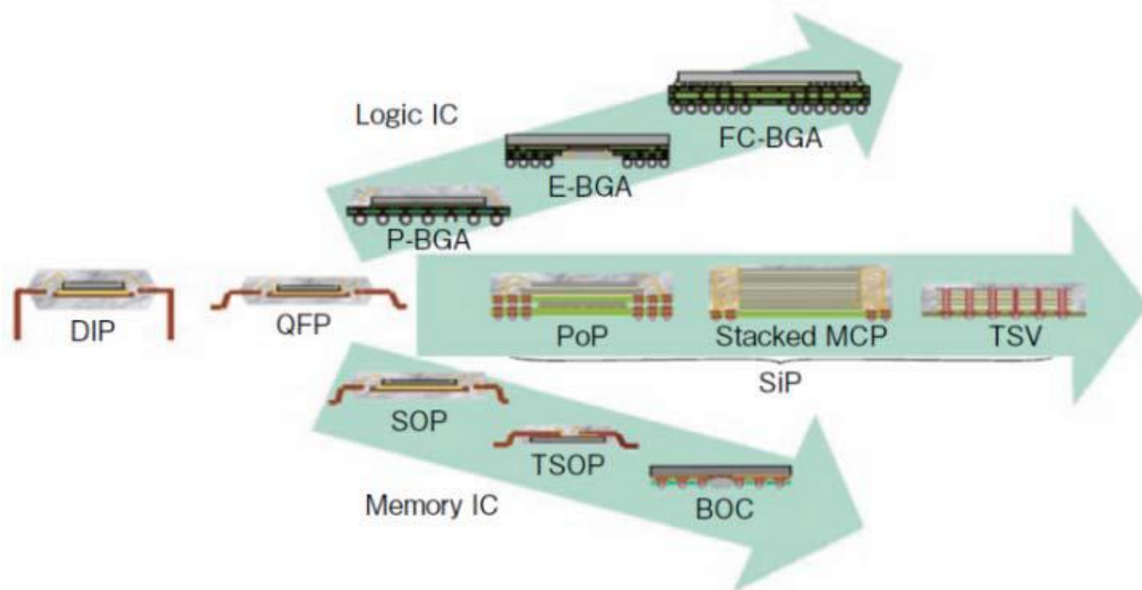


Figure 1.13 Trends of semiconductor packages [17]

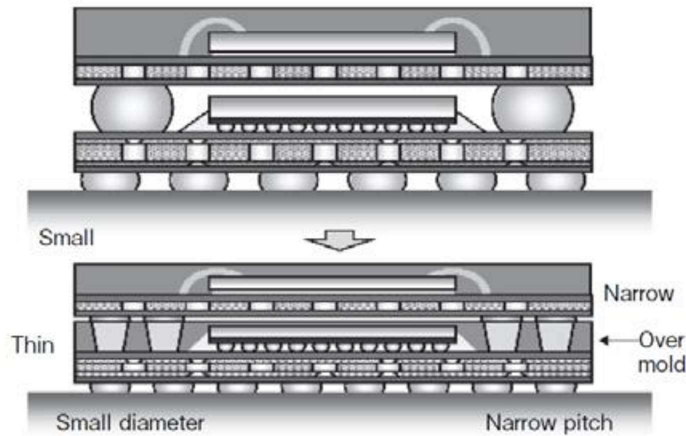


Figure 1.14 High density 3D semiconductor packaging [17]

Gerlatch et al. in their book named "Bio and Nano Packaging Techniques for Electronic Devices" studied on System on Chip (SoC) technology and its trend through the electronics manufacturing history. It states that SoC technology was developed for high volume custom devices by using design elements from different semiconductor devices or by using of reprogrammable logic [18]. Figure 1.15 shows the trend of SoC from 2005 to 2015.

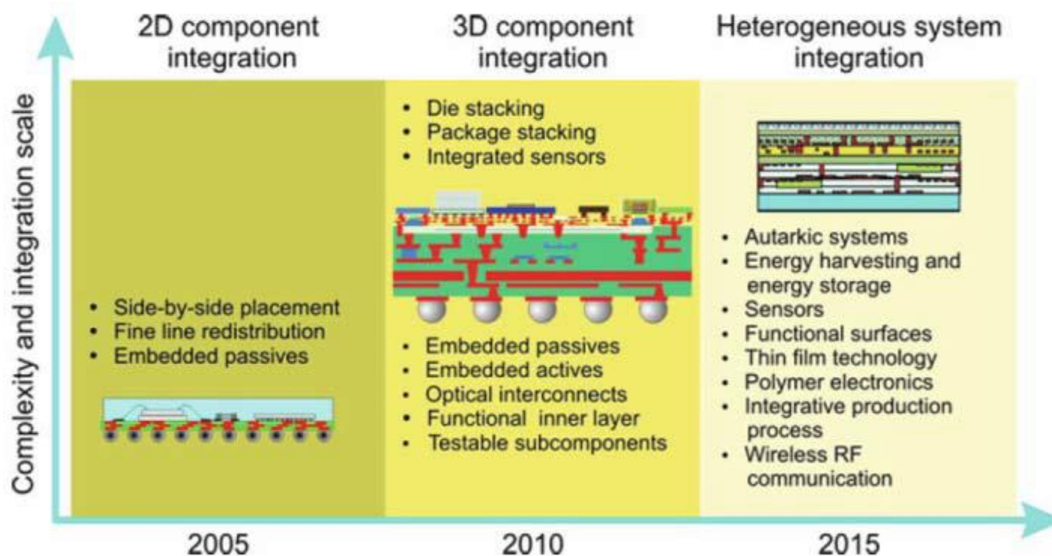


Figure 1.15 Trends in System-in-Package technology [18]

1.6 Evolution of Solder

Many techniques have been developed over the years for joining metal work pieces. Some of the common ones are welding, brazing and soldering. In all the 3 techniques, the surfaces of the metals to be joined are heated in the presence of a filler material which forms a metallurgical bond and upon cooling turns into a sold joint and in-turn joining the work pieces. A chemical agent known as a flux, which removes oxides and contamination to leave behind a readily fusible surface, is often used during this process [5,19,20].

Solder is derived from old French, soudure, which means fasten together. Its use in English as a noun meaning "a fusible metallic alloy used for uniting less fusible metal surface or parts" and dates to 1350. Lead was first obtained as a by-product of silver production, during cupellation of lead from ores. The softness and malleability of lead was later recognized. Lead was used as a setting agent to fix posts in ground and lock mortised stones. Solders containing alloys of lead and tin were found from surviving artifacts and literary source of the Roman Imperial Period. Analysis of solder joints have revealed that both tin-rich and lead-rich alloys were used. In the 20th Century, modern practices developed with the improvement of extraction techniques gave raise to exotic metal at affordable cost along with the alloy phase diagrams paving the path for diversity in alloy making today.

1.7 Soldering

Soldering is a process of joining two metal surfaces using a molten filler metal with or without the use of a flux agent. A metallurgical bond is formed as soon as the filler metal solidifies. This metal joining techniques amongst many others can be called as Soldering only when the filler metal melt below 450^0C [5] additionally, must be done at temperature low enough to avoid

damaging other components of the system that is being soldered [5,6]. Therefore, solders are generally alloys with low melting temperature. Often in this process fluxes are used to clean the mating surfaces and remove most of oxides and organic films before soldering process.

To forge this bond, the solder must flow easily (low viscosity) and 'wet' rapidly (have low surface energy) with the surface finish. Additionally, an intermetallic compound layer must be formed at the solder-surface interface. This is what provides the metallurgical bonding between the two materials [21]. Most Intermetallics are brittle, however, the thickness of the IMC layer should be controlled. Such control is typically accomplished by limiting the time-above-liquidus of the solder during the soldering process [22].

1.8 Solder Joints for Electronic Assemblies

Electronics soldering is a process where the components are attached to the PCB. Most common methods followed to do it are wave soldering process and reflow soldering process. In both processes a strong mechanical connection is created between the components and the PCB. This joint provides electrical, thermal and mechanical continuity in the assembly. The properties of the joint vary with solder and substrate material. Additionally, they must take up mechanical stresses from CTE (coefficient of thermal expansion) mismatches, and be strong enough to deal with vibration and drop conditions. Also, they must maintain their strength over an extensive period, during which they must resist degradation due to environmental factors, electro migration, and diffusion-based microstructure evolution [5]. Table 1.2 is the summary of properties to be considered for the solder alloy selection.

Manufacturing	Reliability
Melting/liquidus temperature	Electrical conductivity
Wettabilitty (of copper)	Thermal conductivity
Cost	Coefficient of thermal expansion
Environmental friendliness	Shear properties
Availability and number of suppliers	Tensile properties
Manufacturability using current processes	Creep resistance
Ability to be made into balls	Fatigue properties
Copper pick-up rate	Corrosion and oxidation resistance
Recyclability	Intermetallic compound formation
Ability to be made into paste	

Table 1.2 Summary of Properties to be Considered for Solder Alloy Selection

1.9 Rise and fall of tin-lead solder

Tin-Lead (SnPb) solder alloys has been the material of choice for the electronic industry and its history dates to thousands of years to prove its popularity. For electronics manufacturing industry, the eutectic Tin-Lead solder with 63% Tin and 37% lead (63Sn37Pb) by weight is the most universal option. A fine-pitch micro-electronic package assembled in the U.S. in the late 1990s (or even today, for some applications) has the same general composition and properties as

that used by the ancient Romans to seal their sewer pipes [5,20,23]. Tin-Lead solders have a variety of advantages in electronic applications [24,25].

- Lead (Pb) is inexpensive and plentiful. Tin-Lead (Sn-Pb) alloys have relatively low melting temperatures suitable for the soldering of electronic assemblies.
- Sn-Pb alloys have low surface tension (which is advantageous to the solder wetting process), with Lead (Pb) acting to reduce the surface tension of pure Tin (Sn).
- Sn-Pb alloys form strong intermetallic bonds with the copper pads used in electronics, with Lead (Pb) acting as a solvent metal during IMC formation.
- Sn-Pb alloys have good mechanical properties, with Lead (Pb) acting to improve the ductility of pure Tin (Sn). The most popular tin-lead solder for electronics manufacturing is the mixture of 63% Tin and 37% Lead by weight [2,5,20].

1.10 Eutectic Alloy and 63Sn-37Pb

The term eutectic is derived from the Greek word eutektos, meaning ‘easily melted’. Eutectic alloys have a single temperature at which the entire alloy melts (when increasing temperature) and solidifies (when decreasing temperature) which makes it easy to predict and work with. These alloys have a pasty range and behave very differently from most alloy compositions. Pasty range is a range of temperatures in which the alloys is partially solid and partially liquid and this is not recommended in electronics. Figure 1.16 shows the pasty range and eutectic point of SnPb alloy.

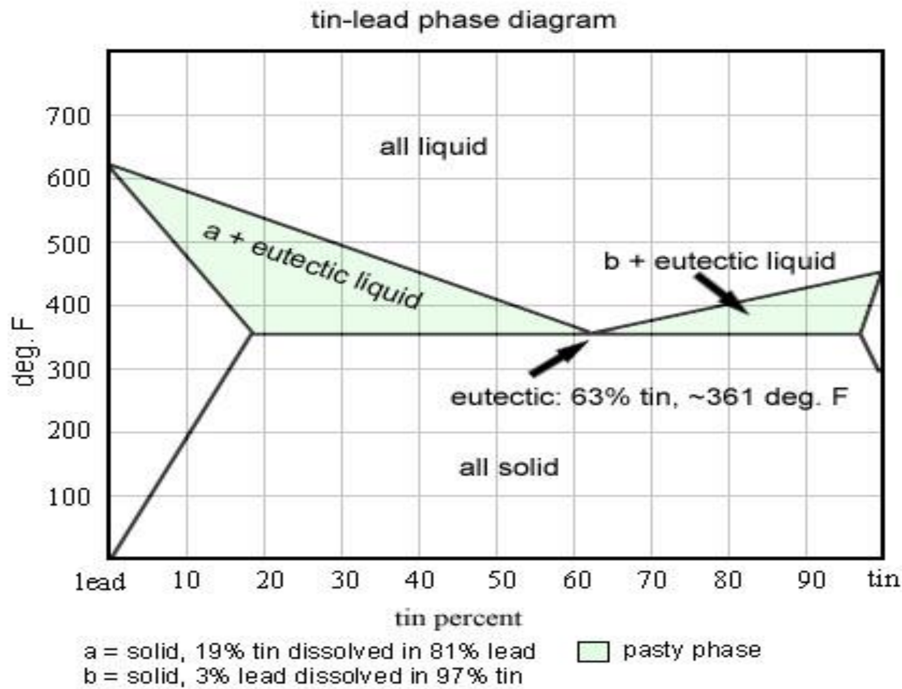


Figure 1.16 Phase Diagram for Tin-Lead Solder Alloy

Eutectic alloys have more homogenous compositions and provide lowest possible melting temperatures. The phase diagram below shows binary alloy system of tin-lead.

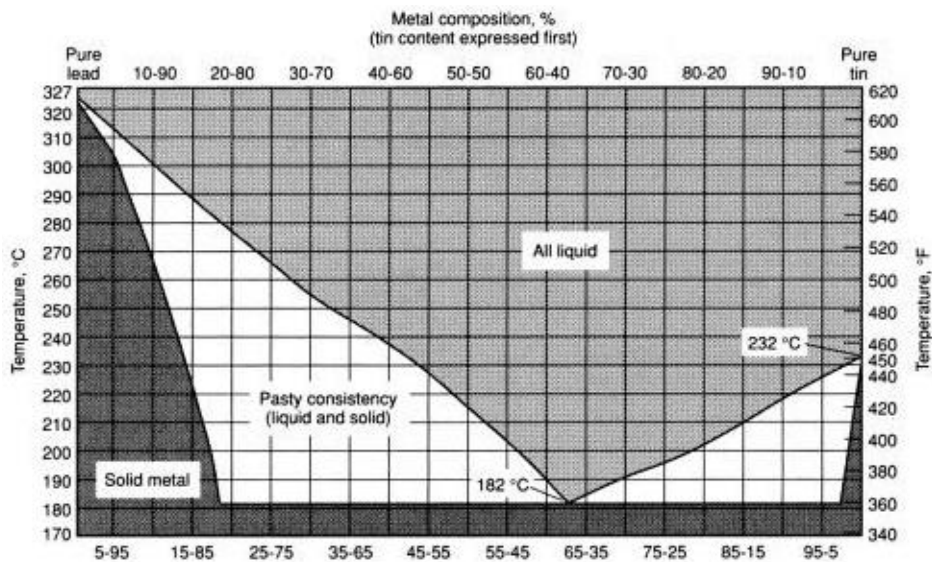


Figure 1.17 Tin-Lead Binary Phase Diagram [23]

From the Figure 1.17 we can see that the 63%Tin,37%Lead composition has the lowest melting temperature of 183^0C which is very favorable. Any temperature lower than this will weaken the joint and any higher will be damaging the parts of the assembly. Advantages of 63Sn-37Pb solder include [2,5,20,26]

- Eutectic Composition (i.e. single transition temperature)
- Low melting point (183oC)
- Low Cost (made from relatively abundant/cheap elements)
- Good Wetting and Manufacturability
- Adequate Fatigue Resistant
- Good joint integrity
- Excellent electrical conductivity

Despite the many advantages of the Sn-Pb solder alloys, it has a fatal flaw. Lead (Pb), presents a grave danger of toxicity. The effects are mostly long term, cumulative exposure and a threat to children. Symptoms of high lead exposure can include: [27]

- Anemia
- Decreased renal function
- Increased blood pressure and cardiovascular disease
- Anti-social behavior
- Learning disabilities
- Mental retardation

Given the nature of these effects, attracted a lot of attention and concern. Finally, in Japan, the advisory committee of Japan Institute of Electronics Industry Development Association (JEIDA) created a roadmap in 1998 for the commercialization of lead-free solders. Although no direct governmental action has been taken in Japan, the Japanese electronics industry has been ahead of the curve in the implementation of lead-free products. In 2000, the EU adopted two directives that were designed to stop the use of lead in electronics. The Waste of Electrical and Electronic Equipment (WEEE) directive stipulated that lead needed to be removed from all electrical and electronic components at their end-of-life. The Directive of the Restriction of the Use of Certain Hazardous Substances (RoHS) prohibits the use of lead in electrical and electronic components manufactured after July 1, 2006 [28]. In the Unites States, no direct governmental action has been taken, but market forces have pushed the US electronics industry toward the adoption of lead-free practices. In 2000, the IPC developed a roadmap for lead-free research and development in the United States [29].

1.10 Near-Eutectic Sn-Ag-Cu (SAC) Solder

With the bans of Sn-Pb, researchers started replacing Pb with copper (Cu), Silver (Ag), Bismuth (Bi), Indium (In), Zinc (Zn), Antimony (Sb) and others. Tin was still chosen as the base element because of its ability to wet and excellent ability to form intermetallic compounds with other metals. Amongst all the combinations Sn-Ag-Cu was chosen as the quick fix in the electronic industry. SAC alloys are near eutectic with melting temperatures range between 232^0C and 183^0C. both silver and copper have face centered cubic crystal structure which provides high thermal, electrical conductivity and metallic luster to their properties. The Equilibrium Ternary Phase Diagram of the Sn-Ag-Cu system is shown in Figure 1.18. The phase diagram shows the ternary eutectic point in the Tin-rich region, at a composition of approximately 95.6Sn-3.5Ag-0.9Cu

(SAC359), which has a melting temperature of about 217.2 ^{0}C. This near-eutectic composition with sufficiently low melting temperature was considered a viable lead-free solder candidate [32].

The ternary phase diagram Figure 1.18 also shows three possible precipitates near the eutectic SnAgCu region: Ag_3Sn, Cu_6Sn_5 and Cu_3Sn. IMC, Cu_3Sn, exists, but does not form except at higher copper contents and therefore, is not seen within the bulk of the solder. No Intermetallics exist between Silver (Ag) and Copper (Cu) [30].

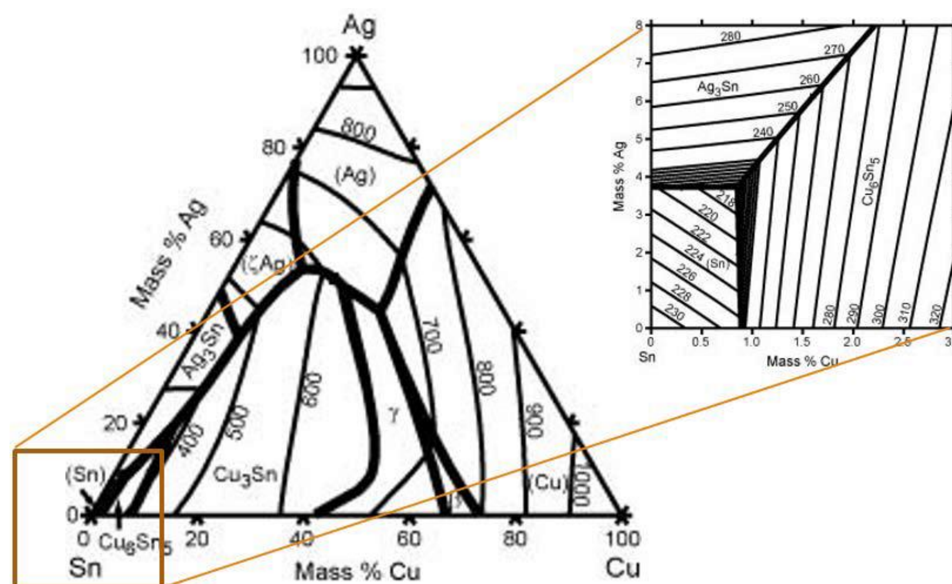
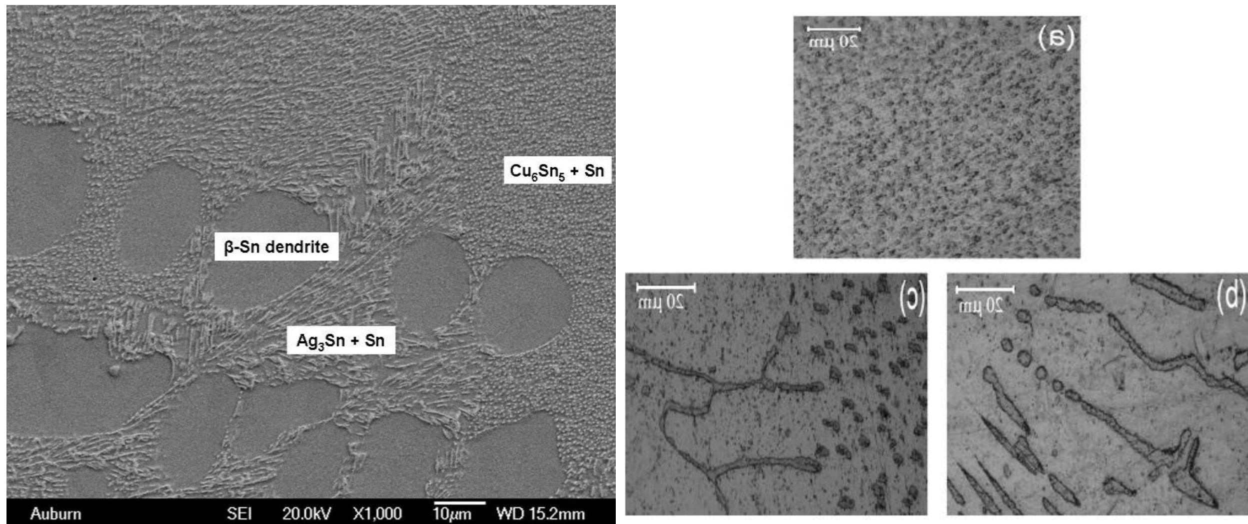


Figure 1.18 From NIST: Sn-Ag-Cu Phase Diagrams

The ternary eutectic microstructure of SAC solders consists of β-Sn dendrites (primary phase), eutectic Sn-Ag regions (needle-shape Ag_3Sn intermetallic dispersed within β-Sn matrix), and eutectic Sn-Cu regions (scallop-shape Cu_6Sn_5 intermetallic dispersed within β-Sn matrix), as shown in Figure 1.19. These interspersed fine intermetallic particles are capable of pinning and blocking the movement of dislocations, and will thus enhance mechanical strength and reliability of solder joints when compared to eutectic Sn-Pb alloy [96,97].



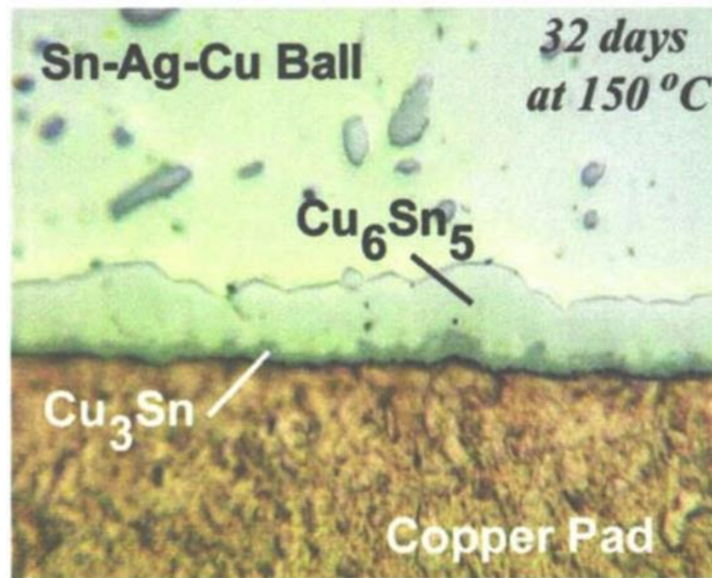


Figure 1.19 SEM Micrograph of Typical Sn-Ag-Cu Solder, Ag3Sn and Cu_6Sn_5 Morphology

The Intermetallic Compounds (Ag_3Sn and Cu_6Sn_5) have higher strength and higher modulus than the β-Sn. Therefore, a higher concentration of Cu_6Sn_5 rods and (particularly) Ag_3Sn platelets increases the effective modulus (stiffness) of a Sn-Ag-Cu solder joint. Overly large Ag_3Sn plates should be avoided, as they act as crack initiation sites under tensile and shear stresses. For a typical SAC solder (3–4 % Ag and 0.5–1 % Cu), Ag_3Sn plates outnumber Cu_6Sn_5 rods. Since,

the IMC Ag_3Sn is the only phase containing Silver (Ag) in a SAC solder, an increase in Ag content results in a corresponding increase of Ag_3Sn IMC precipitates [98,99,100].

Following are some of the SAC-family solders that were developed as a lead-free replacement:

- SAC305 (Sn96.5Ag3.0Cu0.5): most popular SAC solder alloy, especially in automotive and consumable electronics industry. Pasty melting range is around 217℃ to 220℃. Low cost, excellent fatigue resistance, good mechanical characteristics, best wetting SAC alloy.
- SAC105 (Sn98.5Ag1.0Cu0.5): popular in automotive and cellphone industry, because of superior drop and vibration resistance. Pasty melting range is around 220℃ to 225℃. Low cost.
- SAC405 (Sn95.5Ag4.0Cu0.5): contains more Silver. More thermal fatigue resistance and expensive than SAC305.
- SAC387 (Sn95.5Ag3.8Cu0.7): recommendation of the European IDEALS Consortium. Not commonly used in the United States.
- SAC396 (Sn95.5Ag3.9Cu0.6): recommendation of the U.S. NEMI group. Used in the United States occasionally.
- SnCu Eutectic (Sn99.3Cu0.7): eutectic mixture of Tin and Copper. Eutectic melting point is 227℃. Low cost, but poor mechanical properties, and easy to have Tin Whiskers.
- SnAg Eutectic (Sn96.5Ag3.5): eutectic mixture of Tin and Silver. Eutectic melting point is 221℃.

1.12 Solder Paste and Flux

In the reflow soldering of surface mount assemblies, solder paste is used for the connection between the leads of the surface mount components and the lands on the PCB. Solder paste is a

suspension of solder alloy particles in a fluid vehicle or a carrier that contains solvents, flux activators, rheological modifiers and other additives. Figure 1.19 shows the solder paste system.

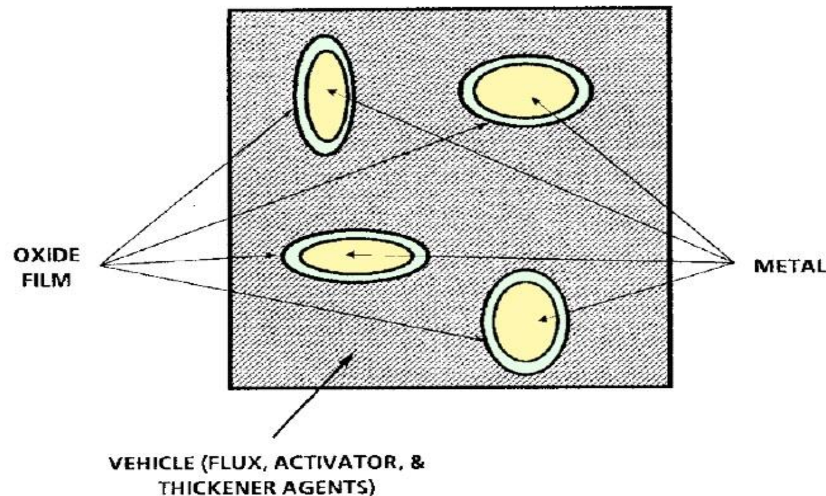


Figure 1.19 Solder Paste

The size of the solder particles in the solder paste is an important factor, couple of effects commonly seen are listed below

- Irregularly shaped and larger solder particles tend to clog the screens and the stencils.
- Smaller particles are more susceptible to oxidation and other surface effects.
- Smaller particles allow small pockets of paste to separate from the main paste deposit. This can lead to electrical isolation of the lands on the PCB.

The usual rule-of-thumb is to use the largest particle size that works with the solder bumps in question, as this reduces problems with solder balls and reduces overall cost [5].

Solder pastes have high solder content, typically 90% by weight. However, because of difference in the density, it amounts to about 50% by volume. The additional 50% is taken up by the flux vehicle.

Flux vehicle is a viscous fluid containing 'activators' – usually mild acids to promote wetting of the solder material during reflow by removing oxides and other surface contaminants. Fluxes also contain solvents, which dissolve the flux and impart the pasty characteristic that allows it to be screen printed, and additives (e.g. rheological modifiers). Solvents must be carefully selected, as they are a key element in the formation of voids (unfilled volumes) within solder joints. The flux vehicle must also coat the exposed metal surface to prevent re-oxidation and provide a sump for the byproducts produced during flux activation [5].

Joint Industry Standard for Fluxes, J-STD-004, classifies fluxes into three categories – low, medium and high, based on their level of activity (I.E how acidic they are). Flux compositions are: Rosin (RO), Resin (RE), Organic (OR) and Inorganic (IN) [5].

Figure 1.21 Picture of Solder Paste

1.13 Overview of SMT Process

In this process, the electronic components are attached on to the copper pads of the PCB. SMT is the central part of the entire SMP packaging technology [31]. The figure below shows the typical SMT assembly process flow.

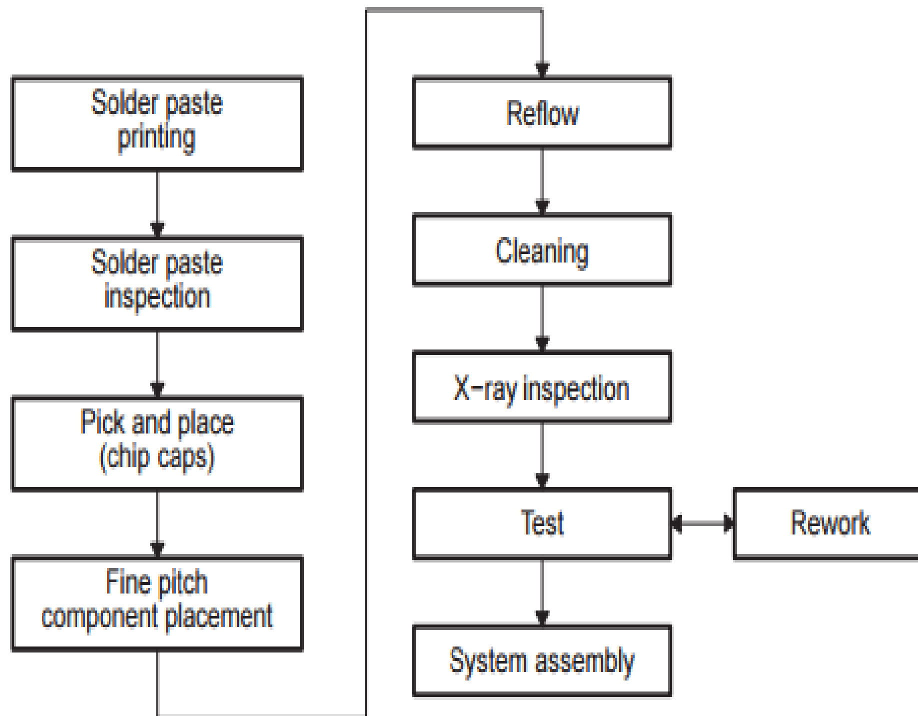


Figure 1.20 Typical SMT Assembly Process Flow

The first step of the SMT assembly process is solder past printing. In this step, solder paste is printed onto the copper pads of the PCB. The figure 1.21 shows the picture of solder paste. Typically, the consistency of it is like toothpaste. This paste is applied on to the copper pads located on the PCB through a process called Stencil printing. Stencil is a sheet of material (usually made of stainless steel) manufactured with desired thickness and with series of apertures cut into it to match the PCB on to which it need to be printed. The main aim for Stencil Printing Process is to accurately deposit correct amount of solder paste onto the copper pads of the PCB surface so that

the solder joint between PCB and component terminal have acceptable electrical contact and mechanical strength. In this process a squeegee blade is used to apply the solder paste. Necessary force is applied on the squeegee to move the paste across the stencil to deposited the paste on to the pad. Figures 1.21 show the squeegee in the assembly line waiting for a PCB to print the paste. The other figure shows the side view of the printing process where squeegee blade is dragging the paste across the stencil to get a good print on the copper pads.

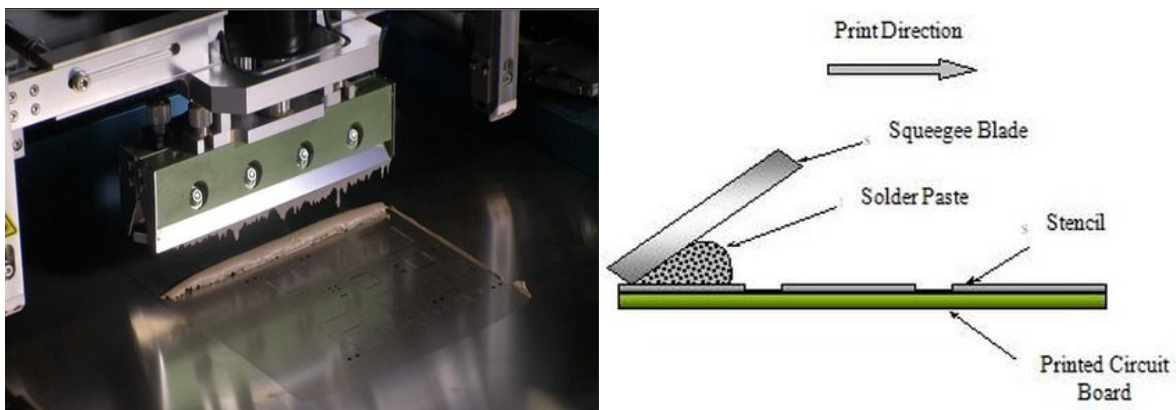


Figure 1.21 A Picture of Stencil Printer and Cross-Section View of a Squeegee Printing Solder Paste on Stencil

Some of the important parameters that need to be taken care of during this process is squeegee speed, squeegee pressure, stencil separation speed, stencil cleaning, print stroke, storage and handling. Figure 1.22 shows unsatisfying prints

The quality of the paste print is evaluated by a 2D & 3D inspection process. In 2D process the area of the paste deposit is inspected and for the 3D volume of the paste deposited is inspected. The figures below show the images of 2D and 3D inspection processes.

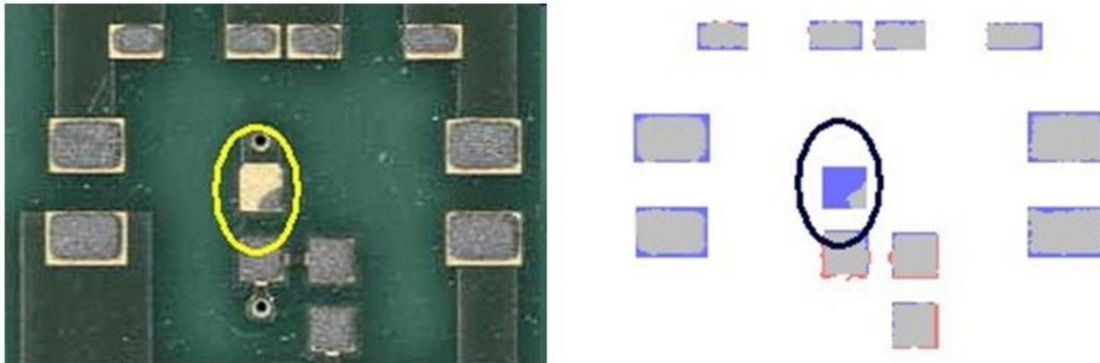


Figure 1.22 Example of Fault Found by 2D and 3D inspection respectively

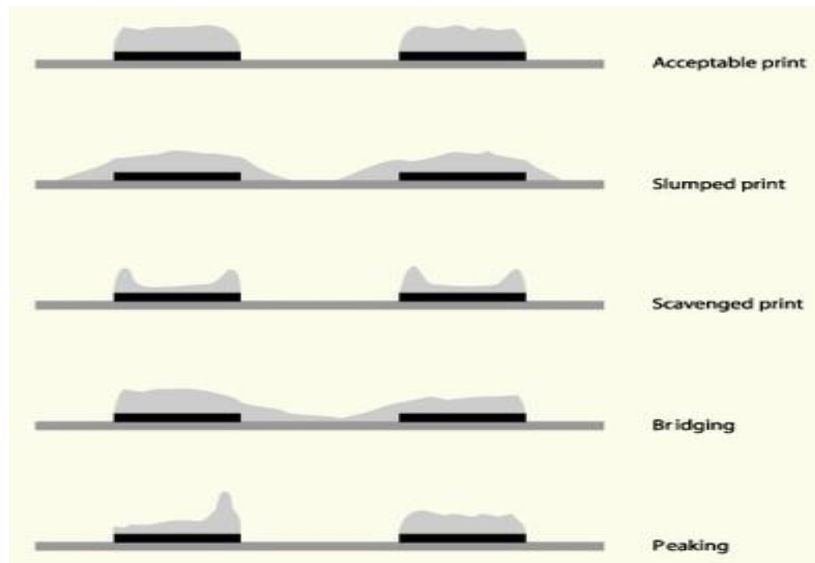


Figure 1.23 Different Types of Unsatisfied Printing Result

Various automatic machines are used to place different electronic assemblies on to the PCB. There are many Pick-and-place machines and are differentiated by lot of variables, the important ones being placement, speed and accuracy. Others include, types of feeders, serviceable board size, inspection capabilities, cost and many more [9].

Reflow soldering process – In this process the PCB with paste printed and electronic assemblies mounted on them enter an oven where the solder joint melt and upon cooling a

permanent metallurgical bond between the copper pad on the PCB and the electronic assembly is formed. The reflow oven uses either infrared or convection as a source of heat. It consists of multiple zones and the temperature of these zones can be individually controlled. The PCB assembly moves across these zones on a conveyor belt, and is therefore subjected to a controlled time-temperature profile [32]. The figure 1.24 show an example of a reflow oven and its labeled sectional view.

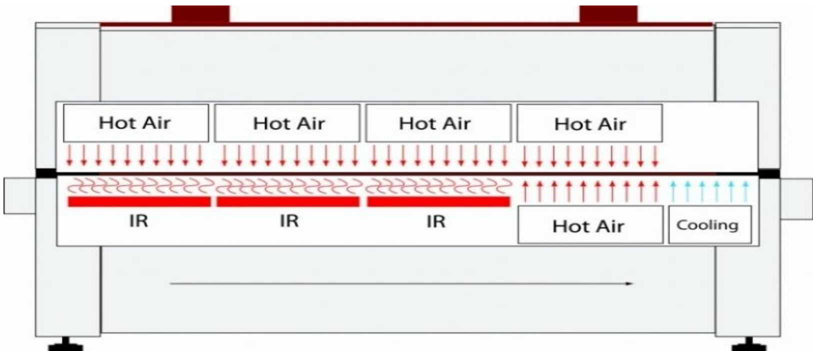


Figure 1.24 Example of a Reflow Oven, With Its Cross-Section View of Structure

The controlled time-temperature profile in the reflow soldering process helps to create a good metallurgical bond between the component and the PCB without overheating and damaging the assembly. Figure below shows a typical reflow profile of an SMT process.

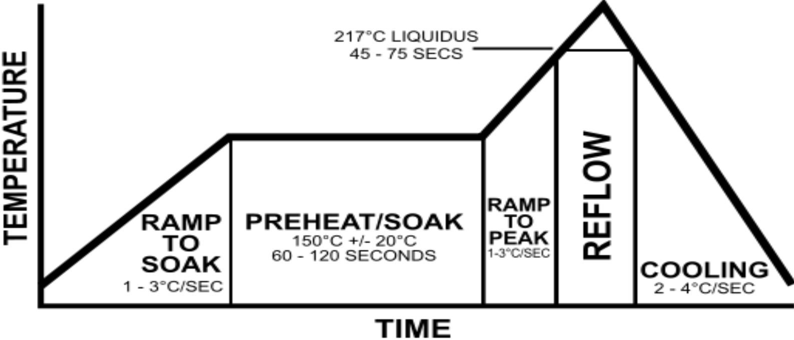


Figure 1.25 A Typical Reflow Thermal Profile [33]

The boards coming out the reflow oven is thoroughly cleaned which is followed by inspection and testing. In this step, either X-Ray inspection or Automated Optical Inspection is performed, to look for the defects that may have occurred in the SMT process [47]. Areas inspected in this phase include component presence, polarity, solder deposition, dry joints, solder shorts to name some. Mechanical and electrical tests are finally conducted to assure the quality of the soldering process. The figure 1.26 shows a typical SMT assembly line.

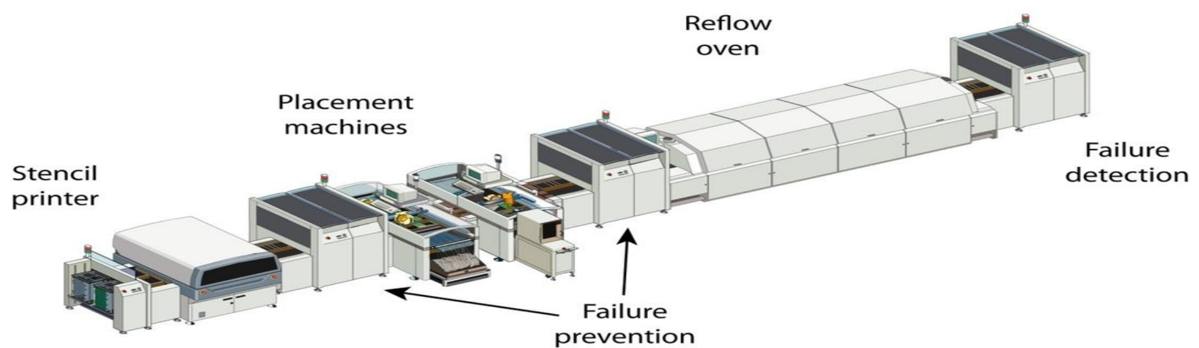


Figure 1.26 A Typical SMT Assembly Production Line

Chapter 2. Literature Review

2.1 Properties of a Solder Joint

Solder alloy selection for a printed circuit assembly involves in understanding and balancing a wide array of properties. Though some of the properties are universally desirable but others depend on the area of application. Some factors that needs to be concerned for the selection of solder materials include, processing of components and substrates, solder strength as a function of temperature, cost, restrictions concerning health and environmental factors.

Solder materials must provide good thermal and electrical conductivity, be easily manufacturable, and have adequate reliability for the intended application [2,5,6]. There are many physical and mechanical properties that are highly desirable in solder joint of electronic assemblies. These properties affect the manufacturability, quality, strength and reliability of the solder joints. Depending on the physical or mechanical properties that one is interested in, it will be important to consider the material composition and processing.

2.1.1 Properties Important to Manufacturability

Some of the properties of a solder material that are important for manufacturability include: [2,5,6,24]

- Cost
- Melting Temperature Range
- Solderability (wetting, adhesion)
- Drossing
- Compatibility with the substrate metallization and component UBM
- Compatibility with common Flux Systems
- Compatibility with manufacturing processes of solder balls and powder
- External Visual Appearance (for inspection)
- Health and Environmental Concerns

Melting temperature range of a solder material is an important form property from manufacturability standpoint. Higher temperatures can result in printed circuit board warping, component or die cracking and many other defects. Also, it can add up the energy expenditure of the soldering process. Therefore, lower melting temperatures are preferred and considered advantageous from a manufacturing perspective.

2.1.2 Reliability of a Solder Joint

By now, we know that the electronics industry is after higher component density, better mechanical performance, higher real-estate and lower cost of an SMT assembly. This sort after qualities make reliability of an electronics package more critical and essential for consideration. Reliability can be defined as the ability of a system or a component to function under stated conditions for a specific period [34].

Reliability of a surface mount assembly considers Wafer Level Reliability, Chip Level Reliability, and Board Level Reliability (BLR), corresponding to hierarchy of interconnection levels [35]. Azira, et al. [36] mention that Board Level Reliability is also known as an interconnect reliability testing and is used to evaluate the quality and reliability of solder connections (BGA, QFN, SMT Resistor, and others) after mounting an IC package to a printed circuit board (PCB). Matin, et al. [37] mention that during a product life cycle, solder joint is exposed to an environment of thermal-mechanical fatigue, including temperature excursions, vibration, drop and shock, which will cause failure of solder joint. Especially when the environment is harsh it will have a severe influence on the Board Level Reliability. Shen, et al. [38] found that fatigue can cause microstructure evolution and deformation due to Coefficient of Thermal Expansion (CTE) between SMT components and the Printed Circuit Board. Zhang, et al. [39] investigated solder joint crack propagation along intermetallic layer between interfaces of the solder joint with component as well as PCB substrate. Zhou, et al. [40] studied the effect of long-term isothermal aging at elevated temperatures on package characteristic lifetime reliability. Basit, et al. [41] developed Finite Element Analysis (FEA) models to simulate solder alloys behavior during thermal aging and cycling. Table 2.1 summaries factors that affect BGA solder joint reliability.

Feature	Lower Reliability	Moderate Reliability	Higher Reliability
Part Type	CBGA	CCGA	PBGA
Die size to part ratio	Largest		Smallest
Ball to pad ratio	Smaller		Larger
Pad type	SMD		NSMD
Via type	In-pad unfilled	In-pad filled	Interstitial open
Via size, min. (aspect ratio)	< 0.020” (> 4:1)		≥ 0.020” (≤ 4:1)
Ball size	Smaller		Larger
Stencil thickness	< 0.006”		≥ 0.006”
Underfill	Reworkable UF	No UF	Non-reworkable UF

Table 2.1 Factor affect BGA solder joint reliability

2.1.3 Properties Important for Reliability

The melting temperature range of the solder material is an important property from reliability perspective. However, here higher temperatures are considered advantageous, which make it resistant against thermally-driven failures (Creep). Other important reliability properties include: [2,5,26,24]

- Coefficient of thermal Expansion (CTE)
- Voiding
- Aging
- Grain Growth and Microstructure

- Intermetallic Formation
- Mechanical Properties (Modulus, Tensile and Shear properties)
- Failure Modes (Crack initiation and growth, Creep, Fatigue)
- Performance under Thermal Cycling
- Resistance to Corrosion and Oxidation

2.2 Failure Modes in Electronic Assemblies

Reliability engineering plays a very important role in electronic assembly. The need of R.E in electronics industry has increased drastically in last couple of decades' newer components, manufacturing processes and novel designs are being implemented.

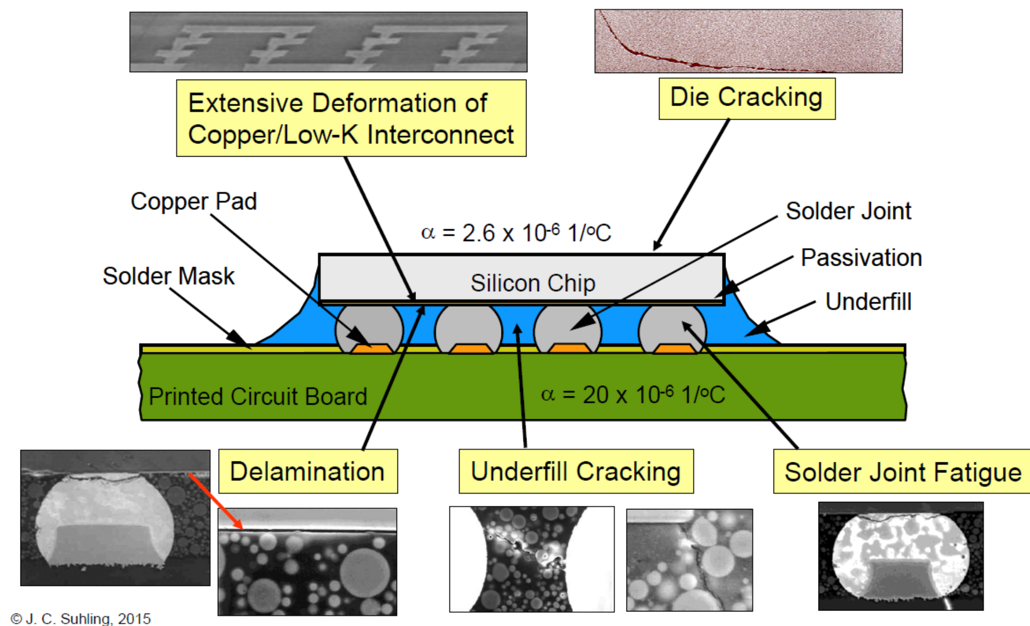


Figure 2.1 Common Flip-Chip Failure Modes [6]

Figure 2.1 shows some of the common failure modes that are seen in a flip-chip assembly. Underfill which is typically an epoxy matrix with glass filler particles is used to when assembling a flip-chip package onto a laminate substrate to control the Co-efficient of thermal expansion and modulus. This prevents failure during thermal cycling.

Common mechanical failure modes include: [2]

- Die Fracture
- Severing of Interconnects
- Wire bond failure
- Underfill or encapsulant cracking
- Delamination of material surfaces
- Solder joint fatigue.

In the case of more conventional packages, cracking through the molding compound and failure of the wire-bonds or flip-chip interconnects can also be a problem [2].

2.3 Characteristic Solder Joint Failures in BGA's

Electrical failure of an electronic component most commonly occurs in the solder joints. Two of the common failure modes observed in BGA's are failure near the IMC boundary regions and failure through the bulk solder material.

For non-solder-mask-defined (NSMD) substrate lands, which have a characteristic divot shape, the highest stress concentrations are found at the opposite side of the joint, near the component UBM [42,43]. Because the highest stress concentration is typically found at the component-side, this is where crack initiation will subsequently occur (explaining the above

experimentally observed crack initiation behavior [44]. These developed cracks can propagate along the IMC boundaries, grain boundaries or through the bulk solder. Figures 2.2 & 2.3 show the failure modes.

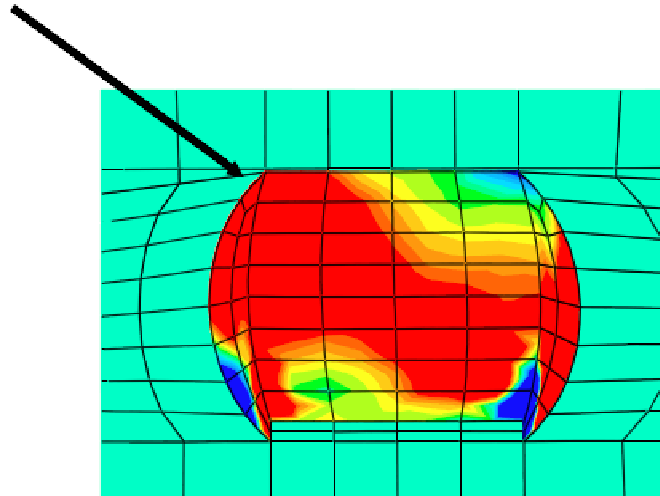


Figure 2.2 FEA model showing induced stress is maximized at the upper corner of the joint [6]

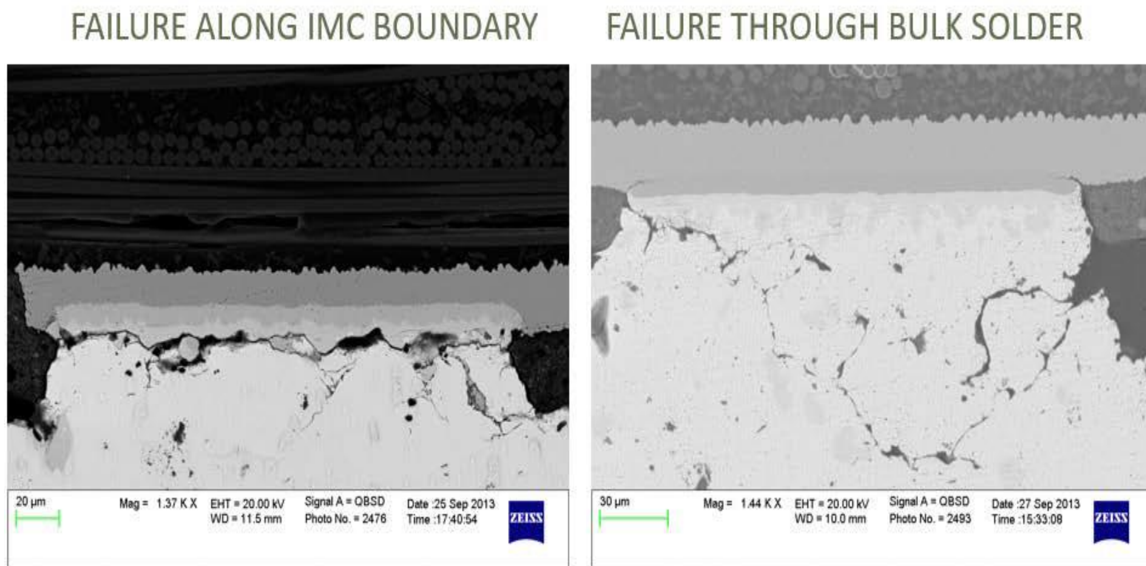


Figure 2.3 Common Joint Failure Modes

Lau [45], a variety of environmental stress factors can result in the structural failure of solder joints or other electronic interconnects. These include: [45]

- Temperature
- Voltage
- Humidity
- Corrosion
- Current density (Electronmigration)
- Mechanical Bending, Shearing, or Twisting
- Mechanical Shock (Drop)
- Vibration

However, most common types of failures are due to over stresses and fatigue. Fatigue failures are lower cyclic loads that initiates and propagates a crack within the joint. Over a period will result in failure. Figure 2.4 shows characteristic fatigue failure.

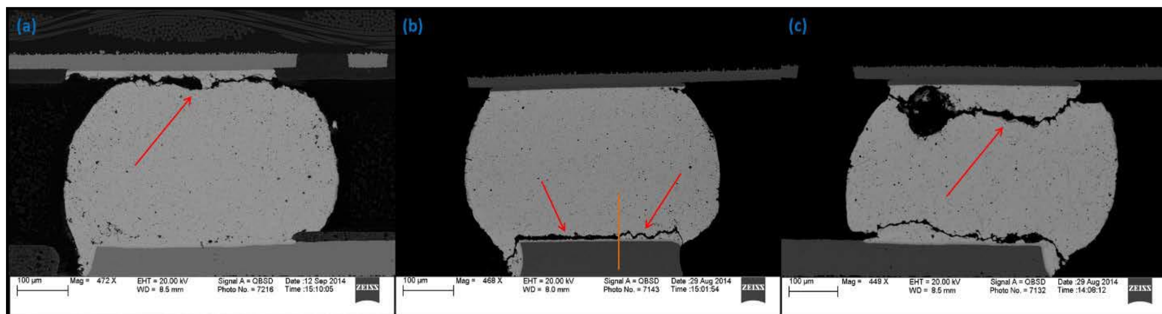


Figure 2.4 (a) Characteristic fatigue failure; (b) Left-hand-side: brittle failure, Right-hand-side: ductile failure; (c) Failure across possible "dynamic recrystallization" zone.

2.3.1 Fatigue

Majority of failures in engineered materials are attributed with fatigue. Solder joints for electronic assemblies are no exception, with many joint failures driven by fatigue [46,47]. Fatigue failures result from cyclic stresses loading at stress levels below the typical yield stress point. It is often considered as one of the most critical failure category. Solder joint fatigue is attributed primarily to the stress brought by the temperature swings and mismatch of coefficient of thermal expansion of materials. Before the fracture, solder joints undergo cyclic deformation from the stresses as the temperature alternate between low and high values. This type of failure is caused by localized stress concentrations. Micro-cracks initiate and lead to stress concentration at boundaries. Higher stresses lead to crack propagation into the material. This crack causes reduction in the cross-sectional area of the material. After a point the material fails to withstand the load exerted thus resulting in a fracture, which is called fatigue fracture, and this can be seen in Figure 2.5. Most material, when subjected to load, will deform. When the load is reversed, the material regains the original form to some extent. Hence there is relatively little plastic deformation which is cumulative and leads to unexpected failure. Ductile materials often behave like brittle materials when subjected to fatigue [48].

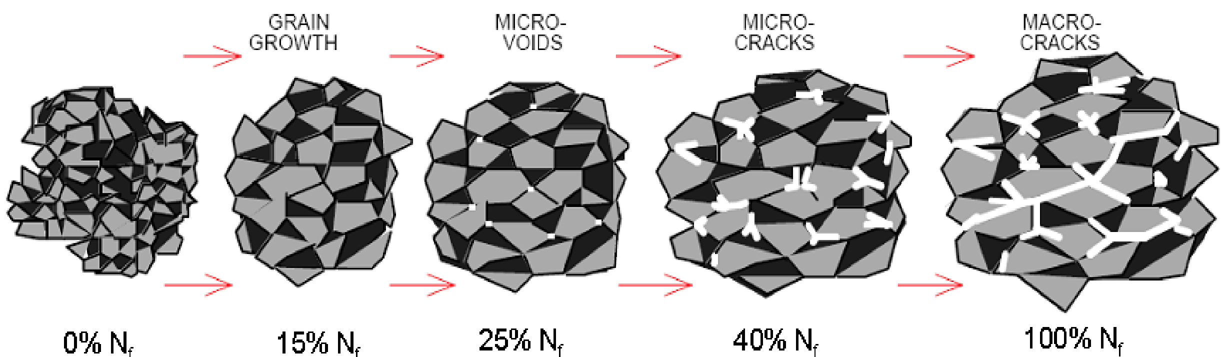


Figure 2.5 Depiction of the Effects of the Accumulating Fatigue Damage [101]

Fatigue crack growth takes place in three stages. These include: initiation and transient crack growth; steady state crack growth; and crack interaction and saturation [3rd stage crack growth].

- Stage 1: Crack initiation and transient growth cracks are formed in the regions where the stress is concentrated, indents, interior corners, dislocation slops and micro-cracks initiate.
- Stage 2: Steady state crack growth along the crystal planes which have higher shear stress, cracks propagate which has flat surface, and cracks propagate perpendicular to the applied stress, they grow by repetitive blunting and sharpening at the tip of the crack featuring rough surface.
- Stage 3: Interaction and Saturation cracks grow to attain a point where one crack crossed the other causing wider cracks to propagate rapidly to ultimate failure.

2.3.2 Creep

Creep is a time dependent plastic deformation that can occur at low stress levels if the homologous temperature of the material in question is high (e.g. greater than 0.5) [49,50]. Creep typically occurs via thermally-activated, stress-directed diffusion of atoms within a material (“diffusional creep”). However, creep can also occur via the movement of dislocations (“dislocation creep”).

When electronic assemblies are subjected to long periods of constant high temperature, the solder joints are subjected to creep. This type of deformation is one of the major types of failure modes of solder joints for electronic packaging modules [47]. In other words, creep is a measure of time needed for a material to fail under constant load and temperature [50].

Creep testing is commonly done by placing a bulk sample under tensile stress (generally constant load) and recording the strain (elongation) as a function of time. The failures from creep takes place in three stages and the same can be seen in figure 2.6.

- Stage 1: Primary creep is a period of primary transient creep, in this period the resistance to creep increases until stage2 due to strain hardening which reduces deformation.
- Stage 2: It is known as steady state creep; in this period, it is found that the rate of creep is roughly constant as strain hardening and recovery softening reaches a dynamic balance. At higher temperature, strain hardening is associated with sub-grain formation caused by the rearrangement of dislocations. Recovery softening is related to thermally activated cross-slip and edge dislocation climb [48].
- Stage 3: In the tertiary creep stage, necking takes place which results in the reduction of the cross sectional area. This accelerated creep may be related to weakening metallurgical instabilities such as intercrystalline fracture and corrosion [48].

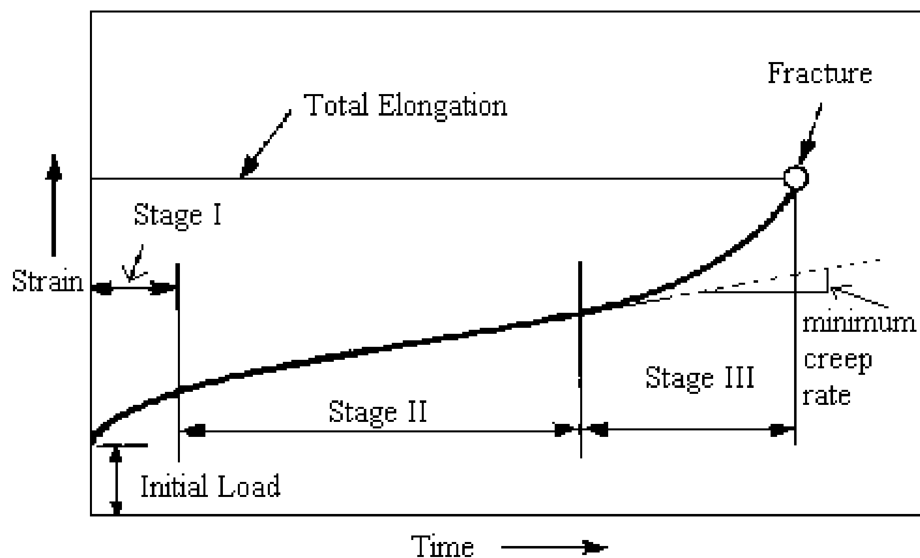


Figure 2.6 Different stages of creeps

2.3.3 Coefficient of Thermal Expansion

Any Electronic component that is powered to function generates heat. Generated heat results in thermal expansion of the components. An electronic assembly consists of components mounted on to the PCB's. When there is a mismatch in the coefficient of thermal expansion of the component and the substrate material, stresses are induced. In ideal condition, if the CTE of all the materials in the assembly are same, they expand and contract together with no thermal stresses induced. But almost all the packages have a mismatch of CTE due to wide array material used in present day electronic packaging. Typically, the component at ON condition expands and contracts when it cools at OFF condition which result in cyclic stresses in the solder joints as shown in the figure 2.7. It is important to know the spatial and temporal distribution of the cyclic stress usually takes the form of solder joint shearing. The range of temperature variation, the component configuration and solder joint distribution, the solder joint geometry, solder alloy elastic-plastic and creep constitutive relationship are some of the factors that define the solder joint shearing due to CTE mismatch.

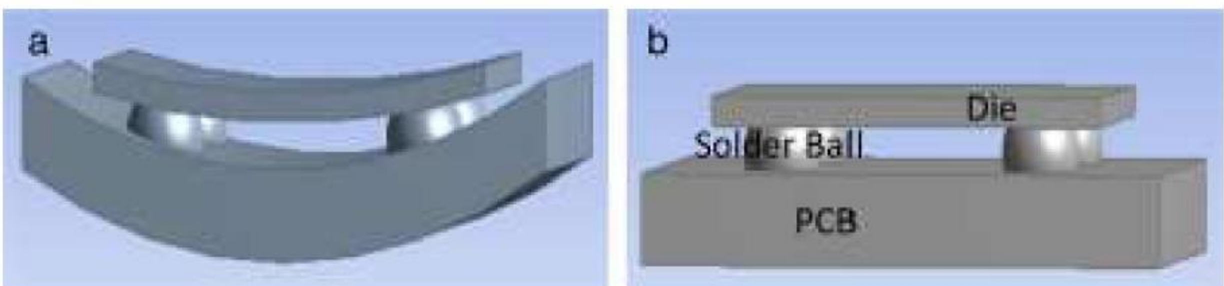


Figure 2.7 a) Cyclic Stress Induced by CTE Mismatch after expansion, b) before expansion

2.3.4 Tensile Properties

Solder Joints in the electronic component are the subjected to tensile loading when the assembly undergo flexing. To determine the tensile deformation limit of the joint before it sustain failure, the tensile properties of the solder alloy such as yield strength, ultimate tensile strength and elastic modulus are important. The figure 2.8 shows tensile loading of a BGA package.

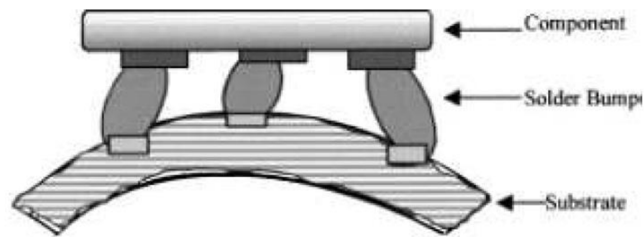


Figure 2.8 Tensile loading [36]

The material strength can be defined as the load it could undergo without deformation. This can be determined by a tensile test results in the form of stress-strain graph. Below is a typical format of a stress-strain graph that provides the data about the material's tensile strength without regard for material's physical size or shape [48]

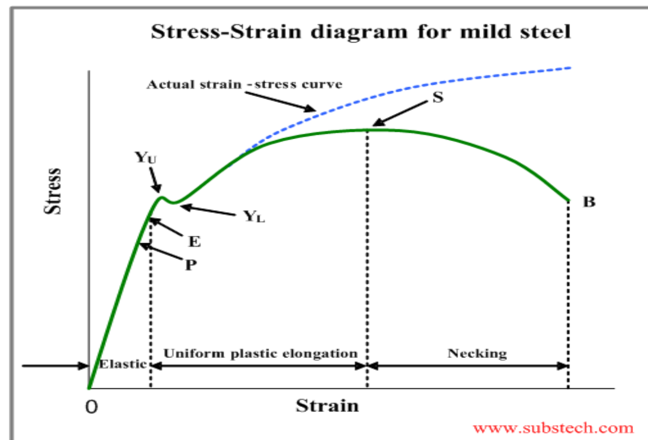


Figure 2.9 Stress-Strain relationships

In the graph 2.9, the blue line represents the true stress-strain curve. Strain is the ratio of increase in dimension to the original dimension. Tensile stress is the ratio of the tensile load F applied to the specimen to its original cross-sectional area S0, Eq. 1.1. The initial straight line (OP) of the curve characterizes proportional relationship between the stress and strain. The stress value at the point P is called the limit of proportionality; this behavior conforms to the Hook's Law. E is a constant, known as Young's Modulus or Modulus of Elasticity. The line OE in the Stress-Strain curve indicates the range of elastic deformation, upon removal of the load at any point of this part of the curve results in return of the specimen length to its original value. The elastic behavior is characterized by the elasticity limit which is the stress value at the point E. A point where the stress causes sudden deformation without any increase in the force is called yield limit. The highest stress (point YU), occurring before the sudden deformation is called upper yield limit. The lower stress value, causing the sudden deformation (point YL) is called lower yield limit. As the load increase, the specimen continues to undergo plastic deformation and at a certain stress value its cross-section decreases due to "necking". At the point S in the Stress-Strain Diagram, the stress reaches the maximum value, which is called ultimate tensile strength.

$$F/S_0 \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad \text{Eq.1.1}$$

2.3.5 Shear Properties

Constant power fluctuations in an electronic assembly, shear stress is induced due to the mismatch in the coefficient of thermal expansion. The silicon die and the substrate are subjected to shear stress due to the mismatch in CTE and the same is shown in the figure 2.10.

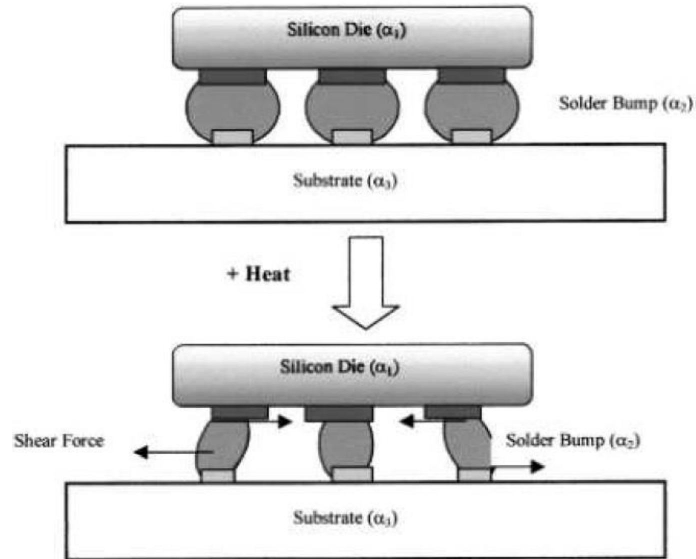


Figure 2.10 Solder Joints Subjected to Shear Strain due to CTE Mismatch [36]

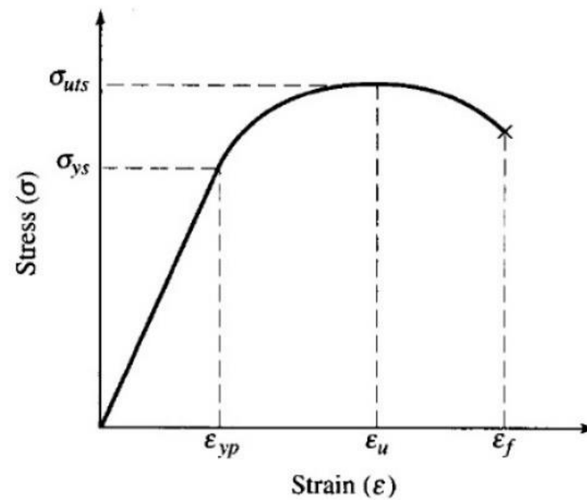


Figure 2.11 Solder state under shear load

When a material is subjected to shear load, it behaves in linear-elastic manner and exhibit a proportional limit σ_{ys} until ultimate shear stress σ_{uts}, strain hardening will take place. The shear strength drops when the material fractures and the fracture strength is obtained from point at which material fracture. Due to CTE mismatches and thermal differences, electronic assemblies often

undergo combined shear deformation, warpage, and distortion. Under such circumstances, solder joints are usually subjected to a combination of shear and tensile loading which results in failure.

2.3.6 Intermetallic Compound Layer (IMC)

During soldering process, the IMC layer is generated between the solder and the copper pad on the PCB to form a metallurgical bond. [51] IMC is formed in the reflow oven during reflow stage, when the solder alloy begins to liquefy or melt. Tin present in the solder paste will migrate to copper through a process called wetting. The growth of IMC continues as long as the temperature is above the melting point of the solder alloy. If there is no intermetallics then there is no solder joint [52] and IMC layer is the most brittle part of the solder joint. Cracks easily propagate along the interface hence thick layer of IMC layer is bad for the solder joint reliability.

2.3.7 Effect of Aging on Solder

Solder alloy undergoes various types of aging after they are manufactured. During the assembly process, the solder alloys are exposed to elevated temperature, which results in aging of the second level solder joints [53]. The mechanical properties and aging effects of the solder bars are different when compared with solder joints. Lampe [54] found the aging effects of solder joint at room temperature. Up to 20% of the shear strength and hardness is lost after 30 days of storage at room temperature. In 1956, Medvedev [55] observed 30% loss of tensile strength for bulk Sn Pb stored at room temperature for 450 days at the same time there was a loss of 23% loss of tensile strength for solder joints stored at room temperature for 435 days. Lee et al. also observed that in 3 days room temperature aging after reflow, shearing stress of solder joints decreased by up to 10 % [56,57]

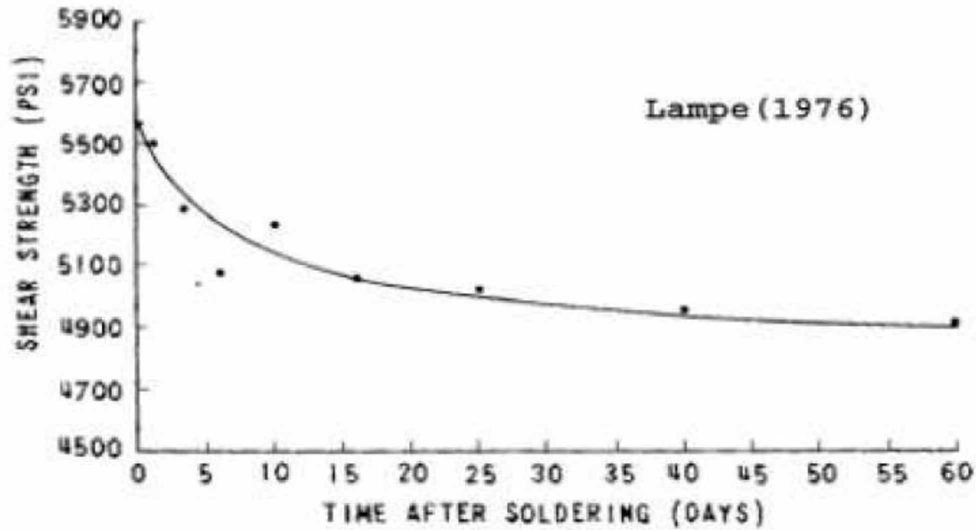


Figure: 2.12 Effect of Aging at Room temperature for Sn-Pb solder [65]

Xiao studied stress-strain curve of SAC396 after different period of aging at room temperature and showed a loss of ultimate tensile strength up to 25 % over days [58,59]. At elevated temperature of 180^0C, it was observed that there was quick softening of the material during the first 24 hours followed by a gradual hardening with time.

The solder behavior is influenced by external factors like applied strain rate, temperature and mechanical loads over a duration of time [60,61]. For SAC alloys it has been demonstrated before, that time and temperature are some of the most critical factors which influence the solder performance [62,63,64,65,66]. The aged specimens were also found to creep much faster than un-aged ones by a factor of up to 20 times for both SAC305 and SAC405 solder alloys [67].

SAC432. SAC396 and SAC387 are few alloys which exhibit a reduction in their flow strength with increasing test temperatures after aged at 125°C for 24 hours, and their degree of strength is highly dependent on their composition [65].

Studies [68,69,70,71] have been performed to understand the degradation of BGA ball shear strength with elevated temperature aging at 125°C or 150°C. It has been documented that microstructure coarsening and intermetallic layer growth take place during the aging period. Chiu found significant reductions in drop reliability when aged at elevated temperature [68], the formation of voids and coalesce were the dominant mechanism for solder joint strength and board level reliability degradation. Ma, et al. [72] observed that the evolution and saturation of Young's modulus, yield strength, and ultimate strength of a series of SAC alloys under various aging conditions. He developed a linear-exponential model to describe the material property evolution. Aging effects on creep resistance in terms of secondary creep strain rate were also studied. Xiao, et al. [63] reported that SAC396 has much lower absolute creep rates compared with eutectic Sn-Pb and tried the increase in creep resistance to the finely dispersed intermetallic compound (IMC) precipitates in the Sn matrix. Aging effects on primary creep was found to be more dramatic than on secondary creep [66].

Lau [73,74,75] observed significant hardness losses and microstructural coarsening for Sn-Pb, Sn-Ag, and Sn-Zn eutectic solders stored at 25°C for 1000 hours, whereas Chilton [76] observed a 10-15% decrease in the fatigue life of single SMD joints after room temperature aging.

2.3.8 Effect of Aging on the Intermetallics

Aging leads to phase coarsening of both β-Sn and precipitates, the dispensing and coalescing of IMC particles, as well as the accelerated growth of grains, and the interfacial IMC thickness between Cu trace and bulk solder joints. Thermal aging of a solder joint results in dramatic changes in the mechanical and microstructural properties. The formation of intermetallic layer is beneficial and is necessary to the bond formation between the component lead and the

solder, solder and the board pad. A very thin or excessively thick intermetallic layer result in the failure of the solder joint. Desired intermetallic thickness is 1-5 microns and over time, the intermetallic layer grow. Thermal cycling show accelerated growth of intermetallic thickness which is detrimental to the solder joint reliability as the joint become brittle. Aging softening has also been observed for solder subjected to elevated temperature aging. Pang et al. [77] measured microstructure changes, intermetallic layer growth, and shear strength degradation in SAC single ball joints aging at elevated temperature.

2.4 Drop/Mechanical Shock Testing

Drop impact test is conducted using experimental techniques at board level and product level to evaluate the solder joint reliability in electronic products for harsh environments. This test on completed products provide a realistic scenario of the level of shock experienced buy the solder interconnects. But this approach is expensive, hence board level drop testing is preferred as it mimics the real-life drop impacts and are more controllable when compared to product level drop tests. Shock response experienced by the PCB in product level drop can be used to set up the board level drop to reproduce the real-time conditions that the package components and solder joints undergo during actual drop. To address these issues, extensive experimental tests are carried out to understand the variations in the dynamic responses of the PCB subject to board or product level drop. A product level and board level drop tests on a mobile phone and its PCB was carried out by Lim et al. [78]. Wu et al. [79] carried out product level drop tests on a customized drop tester equipped with a drop control mechanism to control drop orientation and achieve a high degree of reliability. Xie et al. [80] performed free fall board level and product level drops of area array LGA packages and measured the accelerations at the board and package side. Lall et al. [81, 82]

performed a controlled drop test of BGA and CSP packages from different heights in the vertical direction.

It has been reported from a product level drop test that a horizontal drop orientation gives the largest impact responses. Wong et al, identified three board-level drop impact characteristics; (a) elongation and bending of interconnection due to differential flexing of PCB and package, (b) inertia force from electronic packages, and (c) longitudinal stress wave from impact.

According to IPC-9703, there are eight different failure modes expected from a drop test [99]. These are shown in Figure 2.13. Previous studies [83,84,85,86] show that the onset of failure will occur at the corner joints of BGA packages, either due to a fracture at the BGA package/IMC interface, or fracture at the PCB metal/IMC interface.

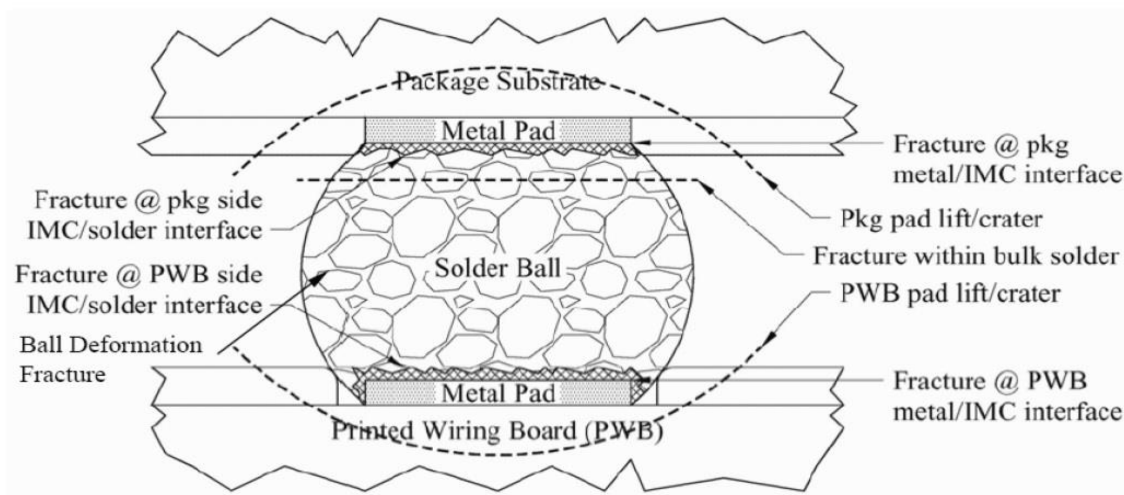


Figure 2.13 Expected Failure Modes from Drop Testing [99]

2.5 Thermal Cycling Testing

Most electronics are not operated continuously in steady state. Instead, they are used over a period of time. Commonly, users will turn their electronics on, run them for some time, and then switch them back off. When an assembly is on and running, heat is generated. When it is turned off, it will cool again. This creates a cyclic thermal environment on the assembly as shown in figure 2.14 For non-climate-controlled environments, this thermal cycling is exacerbated by natural variations in temperature over the course of each day [2,5,6].

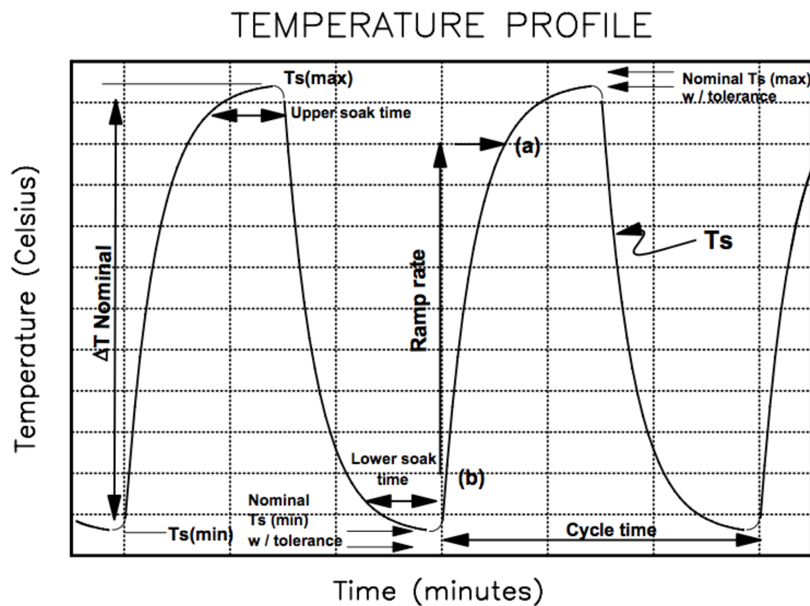


Figure 2.14 Representative Temperature Profile for Thermal Cycle Test Conditions.

Electronic solder joints are mechanically constrained by the other materials of the electronic assembly (e.g. component and PCB) [22]. Because the Coefficient of Thermal Expansion differs for various parts of the assembly – in particular, the substrate and components – these cyclic thermal variations are converted to cyclic stress loads. In addition to the coefficient of thermal expansion mismatches between various parts of the electronics assembly, there are also

local, microstructural-scale CTE mismatches between the various microstructural constituents in the solder and between the different grains of Tin (due to their anisotropy) [22]. This combination of thermal and mechanical effects is known as thermo-mechanical fatigue.

2.6 Accelerated Lifecycle Testing

Accelerated life testing is the process of testing a product by subjecting it to environmental conditions such as strain, stress, temperatures, voltage, vibration, drop, thermal aging, thermal cycling etc., more than its normal working parameters to discover potential failures in a short period. Engineers can make predictions for the reliability performance of the product to help them deal with Design for Reliability (DFR) or Design for Manufacturing (DFM), by analyzing the test result. Accelerated lifecycle testing is essential in both product development stage and maintenance after it is purchased by the customer [87].

2.7 Failure Mechanics

Failure in the solder joint occur due to the induced stresses, accumulated damage and over stress condition. These stress builds up over a period and at some point, the joint can no longer withstand the applied stress, this results in failure. This occurs when external energy such as CTE mismatch is stored as internal energy within the joint, especially in form of dislocations within the crystal structure. As the stress is applied, some energy is stored elastically via stretching of atomic bonds within the solder. However, some energy will be stored via plastic deformation in form of an increased density of dislocations [49].

Additionally, because the typical operating temperatures of electronic solder joints are relatively high in comparison with the solder melting temperature (i.e. high homologous

temperature), Creep mechanics must also be considered. For most Sn-Ag-Cu solder materials, Tin (Sn) is the dominant component, and Tin has a homologous temperature (T/Tm in K) of about 0.6 at room temperature. The creep properties of SAC solders are therefore critical in determining the overall reliability of SAC solder joints [49].

Internal energy stored in the solder material during plastic deformation, it then acts as the driving force for changes in the microstructure of the joint known as "restoration processes." The principal restoration processes are (1) dynamic recovery (relaxation) and (2) dynamic recrystallization. Dynamic Recovery is a well-known process that occurs within many engineered materials and occurs via the "annihilation of lattice defects…by their movement to the grain boundaries where they disappear and their rearrangement to form subgrain networks by polygonization" [49]. Dynamic Recrystallization a process where new grain boundaries are formed dynamically (i.e. during heating, but while stress is still being applied) within a material. This can occur through a variety of mechanisms. During plastic deformation, pure Tin is known to undergo recrystallization and grain growth even at relatively low temperature (i.e. room temperature) [43]. Telang et al. [102] reported that an incremental recrystallization process was observed in which a twin orientation originally in the minority of a grain (as reflowed) "grew and consumed the dominant initial orientation" [102].

The recovery process requires less activation energy than recrystallization, and would normally be the dominant restoration process in pure β-Sn [49]. However, dynamic recovery becomes more difficult in the presence of impurity atoms, particulate phases, and in areas where tangling has decreased dislocation mobility [49]. The presence of these impedances can inhibit recovery and allow for dynamic recrystallization to take place. A number of groups have

demonstrated that dynamic recovery is taking place in Sn-Ag-Cu solder joints under power cycling conditions or in thermal cycle the testing [30,49].

Crack propagation has been shown to follow regions where microstructural changes due to recrystallization have occurred [30,43,49,102]. This susceptibility to cracking happens because the finer grain structure within the recrystallized region “fosters enhanced grain boundary sliding and strain localization in the recrystallized regions” [30]. Crack propagation results from the grain boundary sliding damage within the strain localized region (i.e. creep deformation [43]). As cyclic deformation continues, intergranular cracking eventually results in a remaining joint that can no longer sustain the applied stress, resulting in final joint failure [30].

Henderson et al. [30] found that the amount of penetration of the recrystallized zones into the solder joint varied significantly between joints during fatigue failure. In particular, differences in penetration were often associated with existing β-Sn grain boundaries. This association indicates that in addition to the applied stress field, the stochastic nature of the existing (as reflowed) crystal orientations must be taken into account when considering the recrystallization process [104].

Various reports have found that fatigue crack propagation in Sn-Ag-Cu solder joints with high-Silver joints generally follow the IMC boundary failure pattern, whereas crack propagation in the bulk solder is more common in low-Silver joints. This difference in failure mode is commonly attributed to the higher ductility of low-Ag SAC solder joints [104]. Additionally, large Cu3Sn plates are more common in high-Ag SAC solder joints, and the role of Cu3Sn plates in joint reliability is complex. Plates may act as crack propagation inhibitors in some cases, but large plates that end up aligned with the direction of a crack will instead facilitate propagation and are significantly detrimental to joint reliability [43].

2.8 Solder Doping

With the need for better drop resistance, many lead-free solder alloys are being developed. Since SAC305 has significantly lower drop resistance when compared to SnPb solder alloy, manufacturers are in search of an alternative lead-free solder alloy. Though SAC105 being the most sort after replacement, solder manufacturers are looking for the third generation lead free solder alloy, which often involve in significant additions of element, often referred as dopant [103]. These elements are Bismuth (Bi), Antimony (Sb) and Indium (In) [105]. These additives create finer grain boundaries and reduce the intermetallic formations of the tin with silver or copper, resulting in a more reproducible grain as well as a more uniform grain formation in the lead-free alloy. This process is called solder doping, or solder micro-alloy, or solder addition [105].

Therefore, there is much interest in the industry on establishing optimal SAC-based lead-free solder alloys to meet all demands. According to the results of many recent studies, these goals can be accomplished by metallurgical approaches, i.e. micro-alloying, to strengthening the solder matrix or the matrix/intermetallic interface regions of the solder joint [103].

Bi additions to lead free solders have been the subject of many investigations. It has been shown that Bi can lower the solidus temperature, improve the wetting and alloy spreading, refine the Sn matrix through precipitation hardening, and suppress the formation of large Ag_3Sn IMCs in the bulk solder [108]. On the negative side, it is also reported that Bi atoms segregate along the Cu/IMC interface and lead to brittle fracture [109]. However, according to the observation of Pandher et.al [107], using the appropriate amount of Bi doping is highly important. They found that the addition of 0.01% Bi resulted in improved drop shock and ball pull response for low silver content SAC solder, i.e. SAC0307. In addition, they also observed the reduction in the IMC growth

and the partition to the Cu/IMC interface for Bi-doped SAC0307 solder. Tateyama, *et al.* [110] conducted a study on the effects of Bi content on mechanical properties and bump interconnection reliability of Sn-Ag solder alloys. They suggested a 3% or less Bi doping level in Sn-Ag solder so that the optimal enhancement could be achieved.

The effect of Ni doping has been discussed by several authors [115,103], i.e. a thorough review by Tegehall [111]. It is reported that Ni doping can inhibit the allotropic transformation of Cu_6Sn_5 [115], suppress the formation of Kirkendall voids, and slow the growth of interfacial IMC layers [103]. On the other hand, it has also been demonstrated that the introduction of Ni would soften the SAC solder material and form brittle Cu-Ni-Sn ternary IMCs [103]. Pandher, *et al.* [107] proposed a 0.05% Ni doping to SAC0307 + 0.1% Bi solder to obtain the optimal drop resistance and tarnish resistance [103].

With respect to mechanical properties, Zn modified SAC alloys have been reported to exhibit a combination of high tensile strength and great ductility [105]. The most tremendous benefit of Zn doping is attributed to its enhancement of microstructure stability and aging resistance [106]. Song, *et al.* [105] studied the effect of Zn doping on the microstructure characteristics of SAC solder. They found that the addition of 0.5% Zn significantly reduced the degree of undercooling for Sn-3.3Ag-0.5Cu solder, and thus suppressed the formation of large Ag_3Sn platelets. In addition, Zn-doped SAC solders were observed to have an increased volume fraction of eutectic phases without formation of any Zn-bearing IMCs. Anderson, *et al.* [106] reported that no significant microstructure evolution in bulk Sn-3.5Ag-0.74Cu-0.21Zn solder joints was observed even after 1000 hours of aging at 150 ºC. Similar work was also performed by Kang, *et al.* [112]. They concluded that a minor addition of Zn (<1%) to SAC387 was very effective in suppressing the IMC growth on Cu pads.

It has been demonstrated that other transition metals such as Co and Fe can refine the microstructure for bulk solder joints, as well as hinder the IMC growth near the interface [113,114]. According to the microstructure studies conducted by Anderson, *et al.* [113], Co exhibited a solidification catalysis effect on Cu6Sn5 phase in the Sn-3.7Ag-0.6Cu-0.3Co solder matrix with a desirable (reduced) volume fraction and size (smaller). They also observed the significant effect that the minor substitution of iron for copper promoted highly refined Sn dendrites in the solidified solder matrix. Syed, *et al.* [114] carried out package level tests on a wide selection of SAC-X solders, indicating that SAC355Co solder had the best performance in both ball pull and ball shear tests regardless of aging conditions. Based on their observations, they also suggested that the refined, stabilized microstructure of Co-doped SAC solder was the fundamental reason resulting in the improved resistance to deformation.

Other doping choices for optimizing SAC solders, such as Mn, Cr, Ge, Ti, Si, B, Al, In, etc, have also been studied extensively by various researchers and groups. Liu et.al [115] compared the interfacial IMC growth and drop performance for 14 different doped solder alloys, and concluded that SAC105 + 0.13Mn alloy outperformed all other alloys, including conventional Sn-Pb solder. Anderson, et al. [106] claimed that the aging resistance of SAC3595 improved tremendously by merely adding 0.05% Al. Amagai, et al. [116] found that doping with In could reduce Kirkendall voiding but had little effect on the growth of Cu3Sn IMC. Ge, different from other “diffusion compensators” such as Ni and Co, is acknowledged to refine the Sn matrix as well as improve corrosion behavior [107].

This dissertation discusses the reliability performance of variety of electronic components with more than 10 SAC lead-free solder joints with dopants, under the effect of long-term isothermal aging, and thermal cycling.

2.9 Weibull Analysis

In practice, many Reliability Engineers primarily use the Weibull distribution, which can be thought of as a generalized form of the exponential distribution. The 2-Parameter Weibull distribution has the advantages of ubiquity and ease of interpretation/communication of parameters, and is the most commonly used [104]. It is very common to fit experimental data from thermal cycling and other accelerated life testing using the 2-Parameter Weibull distribution.

The probability density function, cumulative distribution function, and reliability function of the 2- Parameter Weibull distribution is:

$$f(x) = \left(\frac{\beta}{\eta}\right)\left(\frac{x}{\eta}\right)^{\beta-1} e^{-\left(\frac{x}{\eta}\right)^{\beta}}$$

$$F(x) = 1 - e^{-\left(\frac{x}{\eta}\right)^{\beta}}$$

$$R(x) = e^{-\left(\frac{x}{\eta}\right)^{\beta}}$$

where x is the “time” (i.e. number of thermal cycles), β is the Shape (“slope”) Parameter, and η is the Characteristic Life (63.2% failure point) [119].

The Characteristic Life represents the point in “time” at which 63.2% of a population will have failed. The Shape (or “slope”) parameter is a new addition when moving from the Exponential distribution, and allows the Weibull distribution great flexibility. The Weibull distribution can “look” very different depending on what value the shape parameter takes on: [118]

- $\beta < 1$: Distribution has a decreasing failure rate (DFR) {see infant mortality}
- $\beta = 1$: Distribution has a constant failure rate {Exponential distribution}

- $\beta > 1$: Distribution has an increasing failure rate (IFR) {see wearout}
- $\beta = 3.5$: Weibull distribution approximates the Normal Distribution

This flexibility means that the 2-Parameter Weibull can be used to fit a wide variety of life data [118]. (ρ) Indicates the probability plot which indicates how well the data fits the regression line.

Chapter 3. Experimental Setup

3.1 Why BGA?

Majority of the electronics OEM market is moving towards miniaturization with higher level functional integrity. The best examples of this are the new smart phones, mobile and wireless devices. Whether the industry is prepared or not, the fine and ultra-fine pitch chip scale packages, micro BGA's and other active devices are being adapted by designers of next generation of thinner, faster and sleeker portable devices. Number of electronics sub-assembly houses and OEMs are forging ahead using earlier generation knowledge without knowing the consequences and how it affects the reliability along with the complication factor of being lead free.

3.2 Purpose of Study

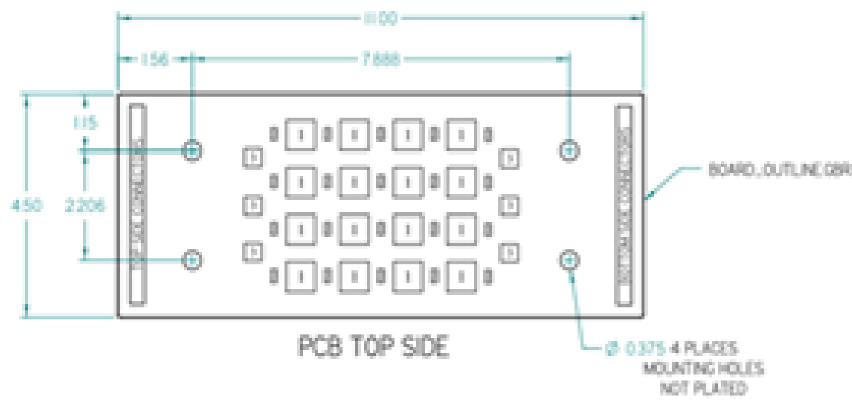
From previous studies and tests provide an idea of how time and temperature affect the reliability of solder joints under different condition. Fine pitch lead free packages have started to enter critical everyday instruments but the knowledge of the combined effect has only scratched the surface of the reliability effect. Especially for doped solder joint, the failure mechanism as well as failure modes have been seldom investigated. The need to know more in a reliability standpoint is higher than ever. The mechanical properties of SAC alloys have shown to change at elevated temperature, but a time conscious approach is in need to study the effect and to get a better understanding. The purpose of this project is to find a manufacturable solder paste with dopants

that can mitigate the effect of aging and find a solder material to replace the SAC spheres and enhance the package reliability. Tests conducted to evaluate the performance of various solder alloys include drop impact test and thermal cycling test at both no aged and aged conditions.

3.3 Test Vehicle Design and Assembly

3.3.1.1 Drop Test Board Design – Phase 1

The substrate material selected for the test boards are standard FR-406, and are covered using a thin Non-solder mask defined (NSMD) pads on both sides and an overlaid silkscreen for labeling. The substrate material is known for retaining mechanical and electrical insulating qualities in both dry and humid environments and has a glass transition temperature of around 170°C. All the components mounted on the boards are chosen carefully to study their drop reliability with various doped solder pastes in both non-aged and aged conditions. The test boards have 16 BGA's, 20 Resistors and 6 QFN's respectively, figure 3.1 shows test board design and a finished board.



ITEM	QTY	DESCRIPTION	SUPPLIER	PART NUMBER
1	16	15mm BGA, 208 I/O, 0.8mm pitch, 0.46mm ball, 17X17 matrix	PC	A-CABGA208-.8-15-DC
2	20	2512 Chip resistor	PC	2512SMR-PA-SN-0
3	6	5mm QFN, 20 I/O, 0.65mm pitch	PC	A-MLF20-5MM-.65MM-DC

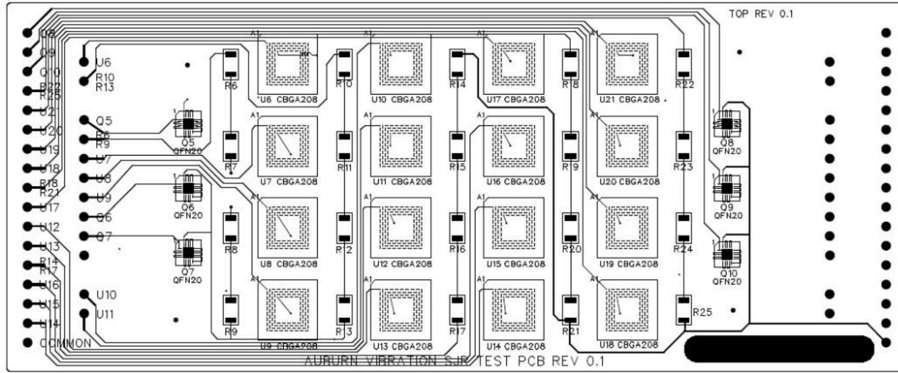


Figure 3.1 Test board design and finished board

3.3.1.2 Test Components

As the study is designed to test both SAC105& SAC305 solders, BGA's are built with both alloys. The test boards consisted of 75% SAC305 and 25% SAC105 of BGA components. Also, the BGA's arrangement on the test board is categorized into 4 zones, the ones with black circle represent the SAC105 packages, and the same can be seen in figure 3.2. Both the SAC105/305 BGA components are placed across the 4 zones strategically to get a better understanding of their failure.

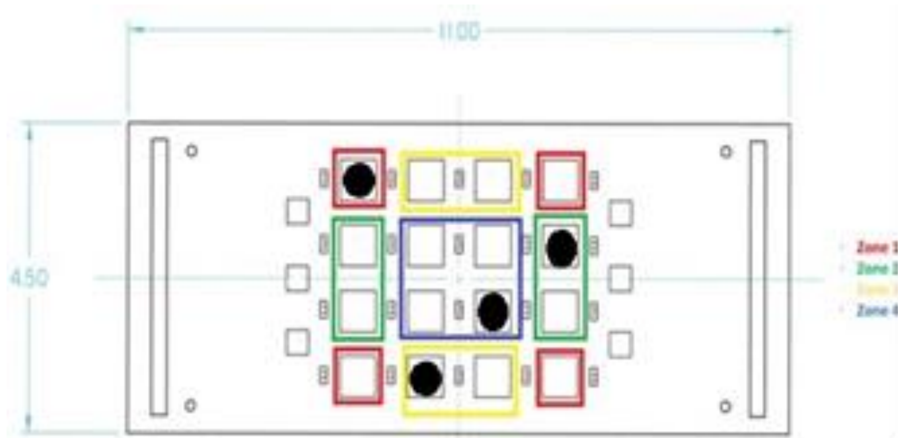
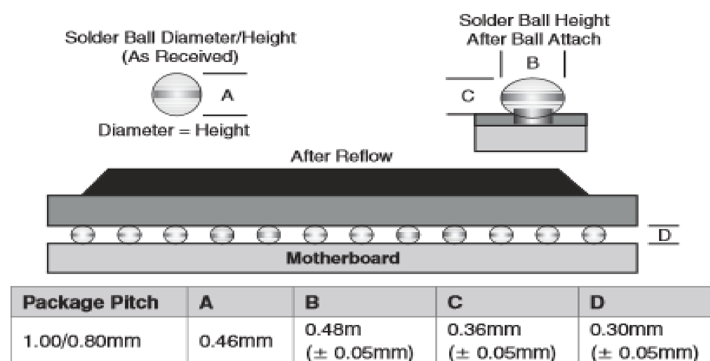


Figure 3.2 Zone wise distribution of BGA packages

BGA Design – This study mainly focused on the evaluation of the performance of various doped solders alloys used with the BGA components. hence we chose the 15mm CABGA 208 package, it consists of 208 I/O's with a 0.8mm lead pitch. The solder balls are 0.46mm in the diameter and are arranged in 17X17 matrix. Standard daisy-chain wiring scheme is chosen. Figure 3.3 gives a detailed description of the same.



Package Pitch	A	B	C	D
1.00/0.80mm	0.46mm	0.48m (± 0.05mm)	0.36mm (± 0.05mm)	0.30mm (± 0.05mm)

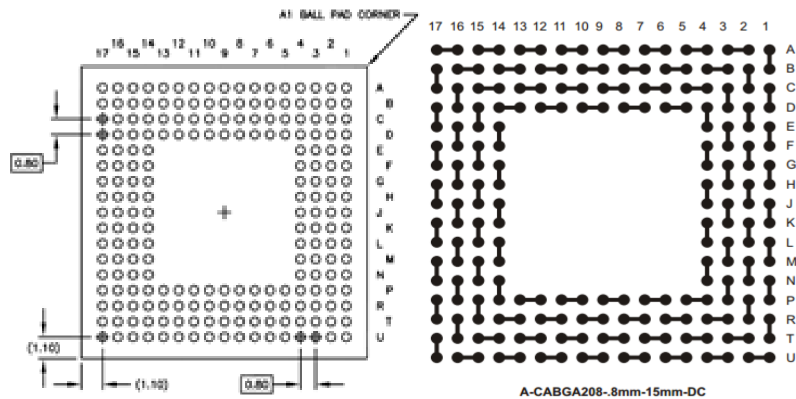
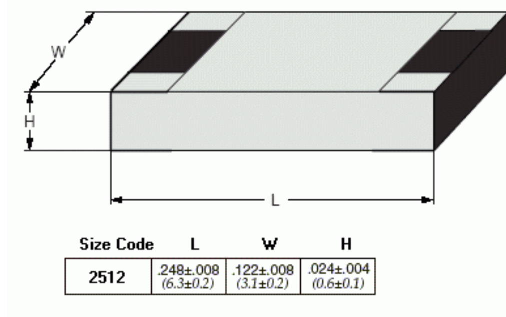


Figure.3.3 BGA Design [8-9]

Resistor design - We know that the large components are prone to failure in the drop tests. Hence, we chose 2512 as it is the most common and the largest size resister used in the electronics industry. The exact physical design can be found in figure 3.4



Size Code	L	W	H
2512	.248±.008 (6.3±0.2)	.122±.008 (3.1±0.2)	.024±.004 (0.6±0.1)

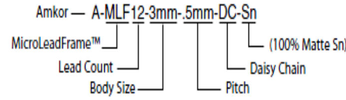
Figure.3.4 Resistor Design [10]

QFN design **-** A-MLF20-5mm-0.65mm QFN is chosen. This package employes an Amkor® MicroLeadFrame®, it consists of 20 leads at 0.65 pitch with total size 5mm^2 as shown in figure 3.5

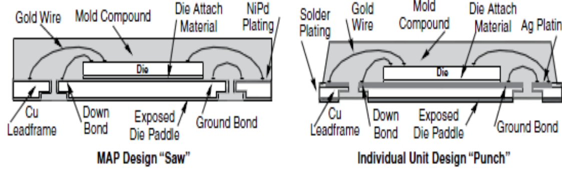
Notes

- Parts are packaged in tubes (standard).
- Parts are available in trays or on tape and reel upon special request.
- Solder plating finish available is 100% Matte Sn.
- Moisture sensitivity level is JEDEC 1.
- Two MLF® designs are available: Punch or Saw (see the cross-section drawing).
- Small size (50% space reduction as compared with TSSOP).
- MLF® package is a near CSP plastic encapsulated package with a copper leadframe substrate.
- MLF® is also known as QFN, MCC or MLP.
- 0.6mm to 1.5mm maximum height
- Body sizes ranging from 3 x 3mm to 12 x 12mm.
- Pin counts and body sizes change on an ongoing basis. Please call for updated listing of available packages.

Part Description System



Cross-Sections MLF®



For kits see pages 93, 96, 98, 106 and 109.

Figure 3.5 QFN Design [11]

3.3.1.3 Build Matrix

Test boards are built using 12 different doped solder materials which are supplied from 8 different solder manufacturing companies. SAC105/305 components and SAC305 paste data is considered as the baseline for this study. The table 3.1 shows that the boards are built with 3 different temperature profiles namely low/high/best and 2 different stencil sizes 4mil and 6mil respectively the reflow profile zone temperatures and the process windows of the same can be seen in table 3.2 & 3.3 respectively. We also built limited sets of boards as per availability which has both solder balls and the pastes of the same material, these are called the matched boards. Each combination has 10 boards built, out of which 5 are tested in no-aged condition and the remaining after aging. All the samples are tested electrically after the build, and the yield is 100%.

Paste code	Stencil Size	Company	Paste	Component Mix	Profile
A	6mil		Alpha CVP390	50% SAC305 50% 105	Best
B				75% SAC305 25% 105	Best
C	6mil			MATCHED INNOLOT	Best
D	6mil			75% SAC305 25% 105	Low
E	6mil		Innolot	75% SAC305 25% 105	High
M				75% SAC305 25% 105	Best
M	6mil			MATCHED INNOLOT	Best
M	6mil			75% SAC305 25% 105	High
M	6mil	ALPHA	Maxrel Plus	75% SAC305 25% 105	Low
F	6mil		Alpha CVP390	CYCLOMAX	Best
G	6mil	ACCURUS	Alpha CVP390	ECOUOY	Best
H	4mil			75% SAC305 25% 105	Best
H	6mil			75% SAC305 25% 105	High
H	6mil		Innolot	75% SAC305 25% 105	Low
I	4mil			75% SAC305 25% 105	Best
I	6mil			MATCHED INNOLOT	Best
I	6mil			75% SAC305 25% 105	High
I	6mil	Heraeus	HT1.02	75% SAC305 25% 105	Low
J	4mil			75% SAC305 25% 105	Best
J	6mil			M758	Best
J	6mil			75% SAC305 25% 105	High
J	6mil			75% SAC305 25% 105	Low
N	6mil	SENJU	M794	770	Best

Paste code	Stencil Size	Company	Paste	Component Mix	Profile
K	4mil			75% SAC305 25% 105	Best
K	6mil			75% SAC305 25% 105	Low
K	6mil		90SCLF318AGS88.5	75% SAC305 25% 105	High
L	4mil			75% SAC305 25% 105	Best
L	6mil			75% SAC305 25% 105	High
L	6mil	HENKEL	90SCHF212DAP88.5	75% SAC305 25% 105	Low
O	4mil			75% SAC305 25% 105	Best
O	6mil			75% SAC305 25% 105	High
O	6mil		8399Y	75% SAC305 25% 105	Low
P	4mil			75% SAC305 25% 105	Best
P	6mil			75% SAC305 25% 105	High
P	6mil	INDIUM	Material 2	75% SAC305 25% 105	Low
R	6mil	INVENTEC	Ecorel Free 405Y-16	75% SAC305 25% 105	Best
S	6mil	AIM	NC 258 91-2,88.5-T3	75% SAC305 25% 105	Best

Table 3.1 Test board/Solder Paste build matrix

3.3.1.4 Drop Test Board SMT Assembly

All the test boards were assembled at University of Alabama, Huntsville Electronics Packaging Lab. 12-Hour bake out process at 150^0C is performed to remove moisture from the reflow oven. The E-FAB Electroform stencil of thicknesses 4mil and 6mil is used for printing. MPM UP2000 HiE machine is used to print the solder paste, this is followed by 3D inspection process to check the area and volume of the paste deposit. Universal GSM-1 pick-and-place

machine with tray feeder is used to place the components on the test boards which is followed by another inspection to check for alignment. Figure 3.6 shows the assembly line at UAH.

Figure 3.6 SMT Assembly Line at UAH

Figure 3.7 shows the Rehm V7 convectional reflow oven that is used for the soldering. Table 3.2 and 3.3 shows the reflow profile process window and the reflow profile zone set point temperatures that was used for this test board build.

Relfow Oven: Rehm V7

Figure 3.7 Reflow Oven

Statistic Name	Low Limit	High Limit
Max Rising Slope (°C/seconds)	0	3
Preheat Time (seconds)	60	100
Soak Time (seconds)	60	90
Peak Temperature (°C)	235	245
Total Time above Liquidus Temperature (seconds)	45	90

Table 3.2 Reflow profile process window

Profile	Conveyor speed (inch/min)	Zone Setpoint Temperature (°C)							
		1	2	3	4	5	6	7	8
Best	26	165	170	185	180	183	236	257	260
Low	29.6	165	175	190	180	180	240	260	260
High	23	160	170	180	180	180	240	255	255

Table 3.3 Reflow profile zone set point temperatures

All the test boards are inspected for quality of the solder joints using transmission X-ray tomography system. This helps to check for defects such as insufficient solder, solder bridging, voids in joints, black pad, and head-in-pillow.

3.3.1.5 Drop Test Setup

Each board is mounted on vertical aluminum fixtures and are fastened onto the drop base plate for mechanical load testing on a Lansmont M23 drop tower. First, it is necessary to calibrate the test parameters of the equipment. This test method is intended to evaluate and compare drop performance of solder interconnects for assembled in an accelerated test. This test is intended to simulate a real-time situation of where an excessive flexure of a circuit board can cause product

failure. The excessive flexure of a circuit board in normal product life can be caused due to repeated impact drops.

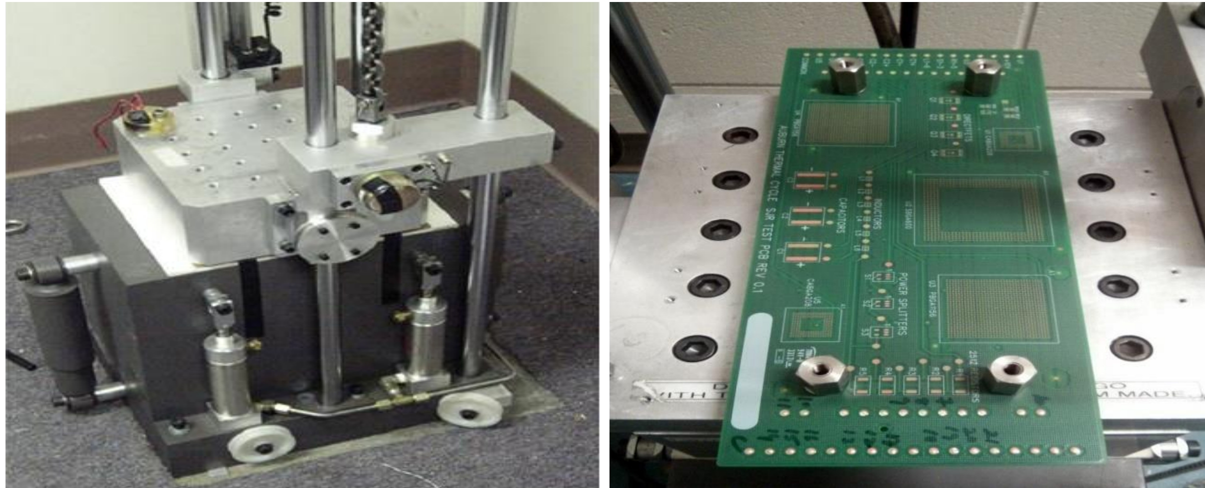


Figure 3.8 Drop tower base and fixture

3.3.1.6 Test Method

A process capability study is carried out to evaluate the drop tower. The base plate was dropped at height's 25in and 30in respectively. The results of this is shown in the figure 3.9. The drop impact test on each of the board is performed as per JESD22-B111 specifications to maximum peak acceleration of 1500 G and half-sine shock pulse duration of 0.5 milliseconds as shown in figure 3.10. Each of the assembled board is dropped to a minimum of 200 times each and is also tested to fail to determine the characteristic life data for various package sizes and structures. Each of the individual electronic components for this experiment is daisy chained for electrical continuity and the resistance for each package is measured after ever 20 drops. This test method is intended to evaluate and compare drop performance of solder interconnects for assembled CABGA208 in an accelerated test. This test is intended to simulate a real-time situation of where an excessive flexure of a circuit board can cause product failure. The excessive flexure of a circuit

board in normal product life can be caused due to repeated impact drops. SAE F5/ASTM 26R1 standard felt is used to absorb the generated shock in this experiment.

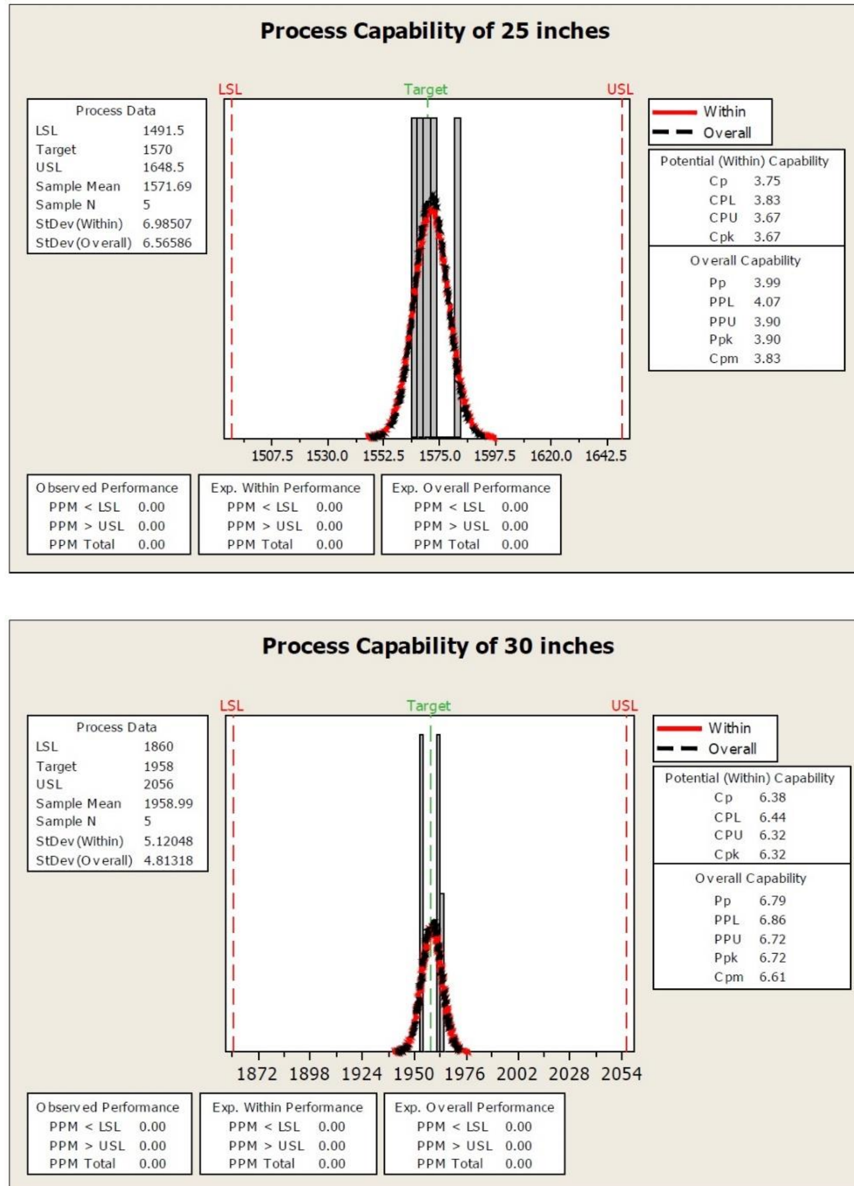


Figure 3.9 Process capability test results

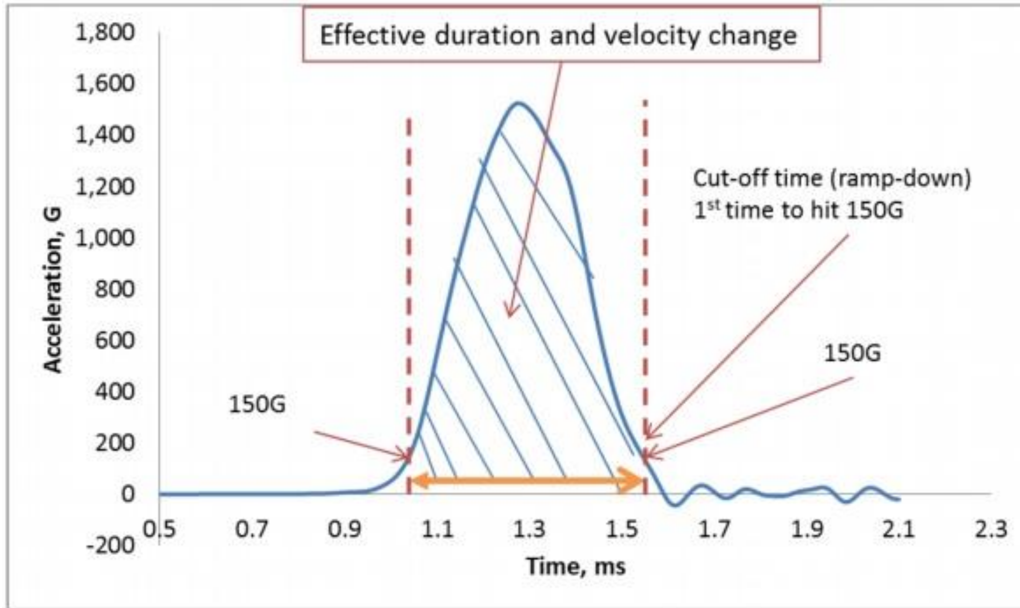


Figure 3.10 Drop test profile

Failures are defined in accordance with the IPC-SM785 standard. A JESD 22B111 failure is defined as the first event of intermittent discontinuity followed by three additional such events during the five subsequent drops. In an impact load drop test, it is observed that a horizontal drop orientation generally gives the largest impact responses. The boards are mounted horizontally on the aluminum base of the drop tower. The drop height of the fixture is adjusted till the desired impact profile is achieved for different packages and boards. The drop height is determined to a standard of 15 to 16 inches. The accelerometer connected to the event detector logs the half sine pulse generated from the standard drop height. The unfiltered result generated for the no-load impact test from the event detector is shown in Figure 3.10. Based on IPC-SM785, the solder joint failure is defined as an interruption of electrical continuity greater than 1000 ohms.

3.3.2.1 Thermal Cycling Test Board Design – Phase 2 – (TC2 SRJ Test Board)

The test vehicle TC2-SRJ was based off of the TC1-SRJ board which was designed by Peter Narbus and manufactured by TTM Technologies (Time-To-Market Interconnect Solutions), Chippewa Falls Division. Overall board dimensions are 173 mm (10 inches) by 254 mm (6.81 inches) with a board thickness of 5 mm (0.2", or 200 mils). When the components are assembled onto the printed circuit board (PCB), each TC1-SRJ printed circuit assembly (PCA) weighs close to a pound (lb), or 0.454 kilograms (kg). To put the size of the assembly into context, a standard sheet of paper is 10" by 6.81", with a thickness of 0.004" or 4 mils.

The TC2-SRJ test vehicle PCBs were assembled by STI Electronics Inc. at their home location in Madison, Alabama. Board Assembly was done from October 20 to October 23, 2015. A total of 260 test boards were built, along with an additional 20 boards used solely for setup purposes during assembly. All test boards are Megtron6 substrate material, FR4-06 boards were used for setup.

Five solder paste materials are selected for incorporation in this test based on their performance in Phase I. Four (4) Isothermal Aging times are included in the test plan: No Aging (0-month), 6-Month Aging, 12-Month Aging, and 24-Month Aging. Board are divided equally into these four aging groups.

3.3.2.3 Test Vehicle Design and Specifications

Boards are assembled single-sided, with components on only one side of the board. Two groups are assembled: in one group, components are placed on the 'Top' side of the board; in the second group, components are placed on the 'Bottom' side of the board. The top- and bottom-side assembled boards are shown in Figures 3.11 and 3.12.

The TC2-SRJ board has 6 copper layers and over 14,600 pins. Up to 19 components can be assembled on the Top-Side, while up to 39 components can be assembled on the Bottom-Side (counting each set of 5 daisy-chained resistors as one component).

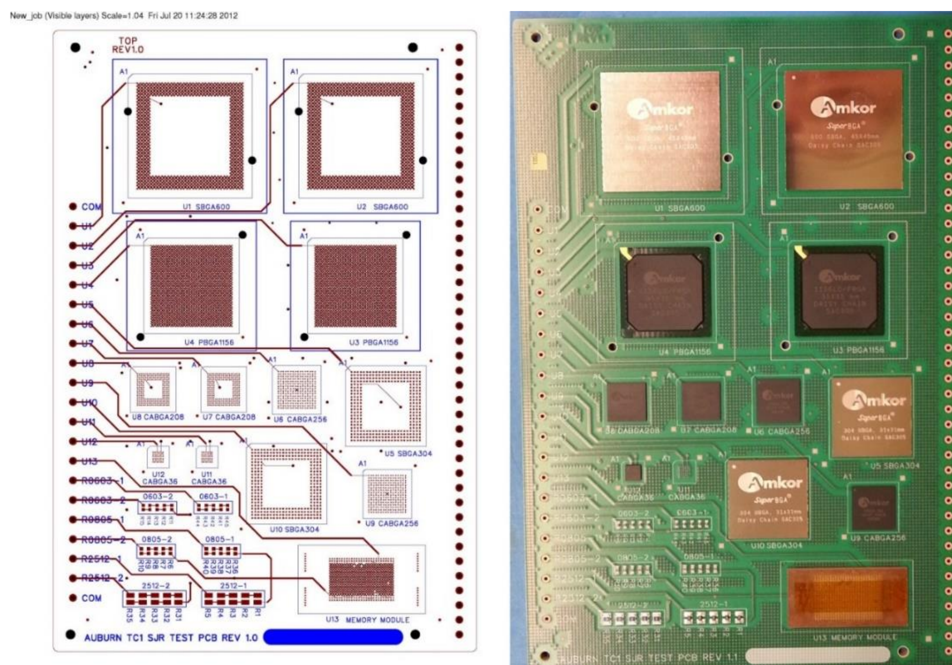


Figure 3.11 TC2-SRJ Test Vehicle: Top-Side View

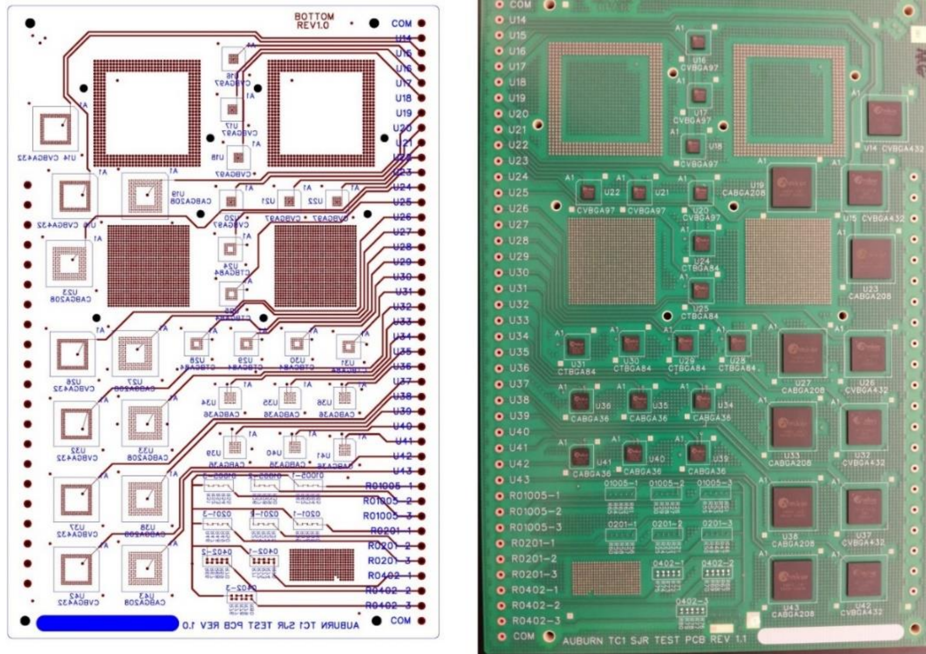


Figure 3.12 TC2-SRJ Test Vehicle: Bottom-Side View

3.3.2.3 Test Plan

A total of 260 test boards are built, along with an additional 20 boards used solely for setup purposes during assembly. All test boards are Megtron6 substrate material. The boards are being built/assembled in two groups: 'Top-side' boards have only the top-side components added, while 'Bottom-side' boards have only the bottom-side components added.

Four (4) Isothermal Aging times are included in the test plan: No Aging (0-month), 6-Month Aging, 12-Month Aging, and 24-Month Aging. Board are divided equally into these four aging groups. For each material, there are 9 'Top-Side' boards and 4 'Bottom-Side' boards for every aging group. This yields a total of 52 boards per material (36 Top and 16 Bottom), with 13 boards in each aging group.

	Material A-E				
CBA	Setup	0-m Aging	6-m Aging	12-m Aging	24-m Aging
Top	1	9	9	9	9
Bottom	1	4	4	4	4

Aging	**Material**	**Top Side**	**Bottom Side**	**Total**
No Aging	A	9	4	13
	B	9	4	13
	C	9	4	13
	D	9	4	13
	E	9	4	13
6 months	A	9	4	13
	B	9	4	13
	C	9	4	13
	D	9	4	13
	E	9	4	13
12 months	A	9	4	13
	B	9	4	13
	C	9	4	13
	D	9	4	13
	E	9	4	13
24 months	A	9	4	13
	B	9	4	13
	C	9	4	13
	D	9	4	13
	E	9	4	13
		Total = 180	**Total = 80**	**Total Boards = 260**

Table 3.4 Test board build matrix

3.3.2.4 General Build Matrix/Assembly Information

Reference	Component	SAC Alloy	Pitch	Dimension	Place
U1	SBGA 600	305	1.27mm	45mm	1
U2	SBGA 600	305	1.27mm	45mm	1
U3	PBGA 1156	305	1.00mm	35mm	1
U4	PBGA 1156	305	1.00mm	35mm	1
U5	SBGA 304	305	1.27mm	31mm	1
U6	CABGA 256	305	1.0mm	17mm	1
U7	CABGA 208	105	0.8mm	15mm	1
U8	CABGA 208	105	0.8mm	15mm	1
U9	CABGA 256	305	1.0mm	17mm	1
U10	SBGA 304	305	1.27mm	31mm	1
U11	CABGA 36	105	0.8mm	6mm	1
U12	CABGA 36	105	0.8mm	6mm	1
U13	Memory Module				0
R0603-1	0603 SMR	100%Sn			1
R0603-2	0603 SMR	100%Sn			1
R0805-1	0805 SMR	100%Sn			1
R0805-2	0805 SMR	100%Sn			1
R2512-1	2512 SMR	100%Sn			1
R2512-2	2512 SMR	100%Sn			1

Table 3.5 Phase II Top-Side component matrix

Reference	Component	SAC Alloy	Pitch	Dimension	Place
U14	CVBGA 432	305	0.4mm	13mm	0
U15	CVBGA 432	305	0.4mm	13mm	1
U16	CVBGA 97	305	0.4mm	5mm	1
U17	CVBGA 97	305	0.4mm	5mm	1
U18	CVBGA 97	305	0.4mm	5mm	1
U19	CABGA 208	305	0.8mm	15 mm	1
U20	CVBGA 97	305	0.4mm	5mm	1
U21	CVBGA 97	305	0.4mm	5mm	1
U22	CVBGA 97	305	0.4mm	5mm	1
U23	CABGA 208	305	0.8mm	15 mm	1
U24	CTBGA 84	305	0.5mm	6mm	0
U25	CTBGA 84	305	0.5mm	6mm	1
U26	CVBGA 432	305	0.4mm	13mm	1
U27	CABGA 208	305	0.8mm	15 mm	1
U28	CTBGA 84	305	0.5mm	6mm	1
U29	CTBGA 84	305	0.5mm	6mm	1
U30	CTBGA 84	305	0.5mm	6mm	1
U31	CTBGA 84	305	0.5mm	6mm	1
U32	CVBGA 432	305	0.4mm	13mm	1
U33	CABGA 208	305	0.8mm	15 mm	1

Reference	Component	SAC Alloy	Pitch	Dimension	Place
U34	CABGA 36	305	0.8mm	6mm	1
U35	CABGA 36	305	0.8mm	6mm	1
U36	CABGA 36	305	0.8mm	6mm	1
U37	CVBGA 432	305	0.4mm	13mm	1
U38	CABGA 208	305	0.8mm	15 mm	1
U39	CABGA 36	305	0.8mm	6mm	1
U40	CABGA 36	305	0.8mm	6mm	1
U41	CABGA 36	305	0.8mm	6mm	1
U42	CVBGA 432	305	0.4mm	13mm	1
U43	CABGA 208	305	0.8mm	15 mm	1
R01005-1	01005 SMR	100%Sn			1
R01005-2	01005 SMR	100%Sn			1
R01005-3	01005 SMR	100%Sn			1
R0201-1	0201 SMR	100%Sn			1
R0201-2	0201 SMR	100%Sn			1
R0201-3	0201 SMR	100%Sn			1
R0402-1	0402 SMR	100%Sn			1
R0402-2	0402 SMR	100%Sn			1
R0402-3	0402 SMR	100%Sn			1

Table 3.6 Phase II Bottom-Side component matrix

3.3.2.5 Solder Paste and Screen Printing

Figure 3.14 Screen printing machine

Five different solder paste materials are used, each from different suppliers. The screen printing machine used is a Speedline Technologies MPM Momentum (right). The stencil thicknesses used are

- Bottom-Side Assemblies = 3 mil stencil
- Top-Side Assemblies = 5 mil stencil

Bottom-side boards are double-printed to get adequate solder volume on the small-pitch components. Otherwise, print parameters where held constant for all assemblies.

3.3.2.6 Component Placement

Two pick-and-place machines are used for the Phase II assembly: the Juki KE-2080L and Juki FX3, figure 3.15

Figure 3.15 Pick and Place machines

3.3.2.7 TC2-SRJ Reflow Profiles

Solder reflow was done using a Heller 1913 MKIII reflow oven (shown below). Two different reflow profiles are used: one for the Top-Side boards and one for the Bottom-Side Boards. The reflow profiles were designed to match as closely as possible the original TC1-SRJ profile, which in turn was selected based on attempting to meet (solder paste) manufacturer recommendations while adjusting based on the realities of balancing time-above-liquidus, peak reflow temperature, etc. for a board of such high thermal mass.

Figure 3.16 Reflow oven

To get accurate thermal readings, a test board was fitted with three thermocouples and passed through the reflow oven while attached to a thermal readout and recording device [EDC M.O.L.E. Thermal Profiler]. The oven temperature zones and pass-through speed were adjusted iteratively until a feasible reflow profile was obtained. The reflow profiles shown in figures 3.17 and 3.18 were used for top and bottom board assembly.

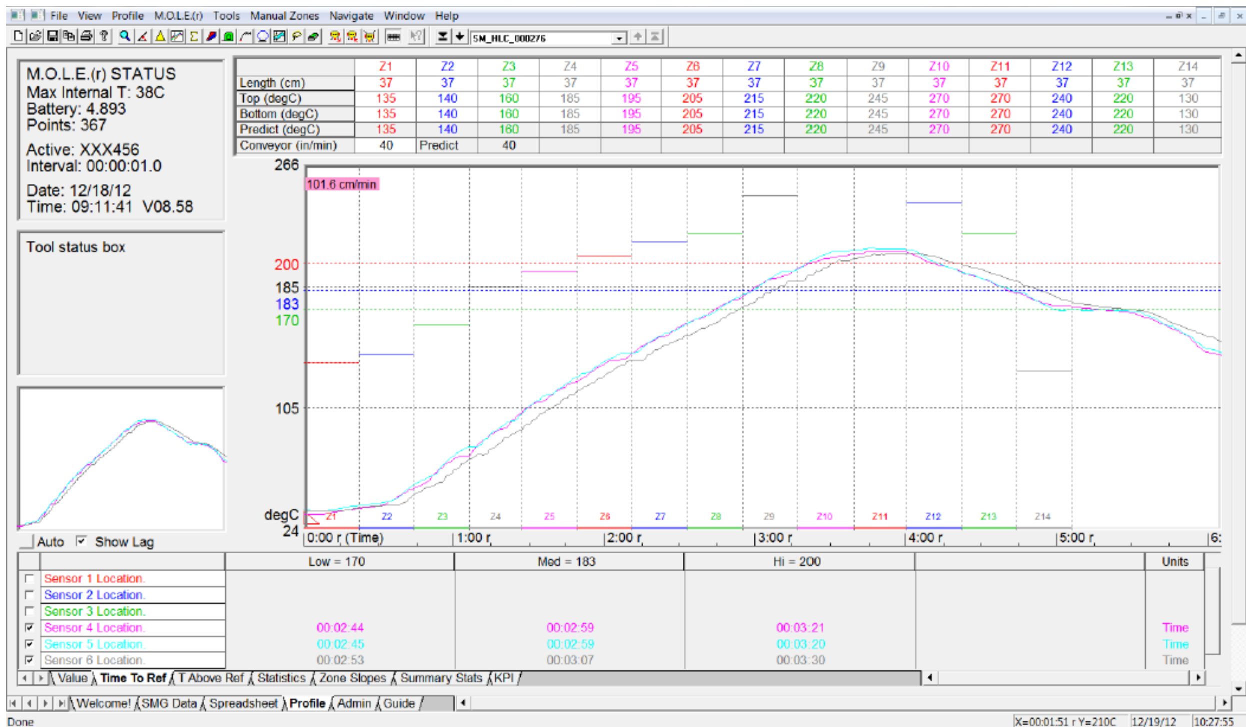


Figure 3.17 Phase II Top-Side Reflow Profile

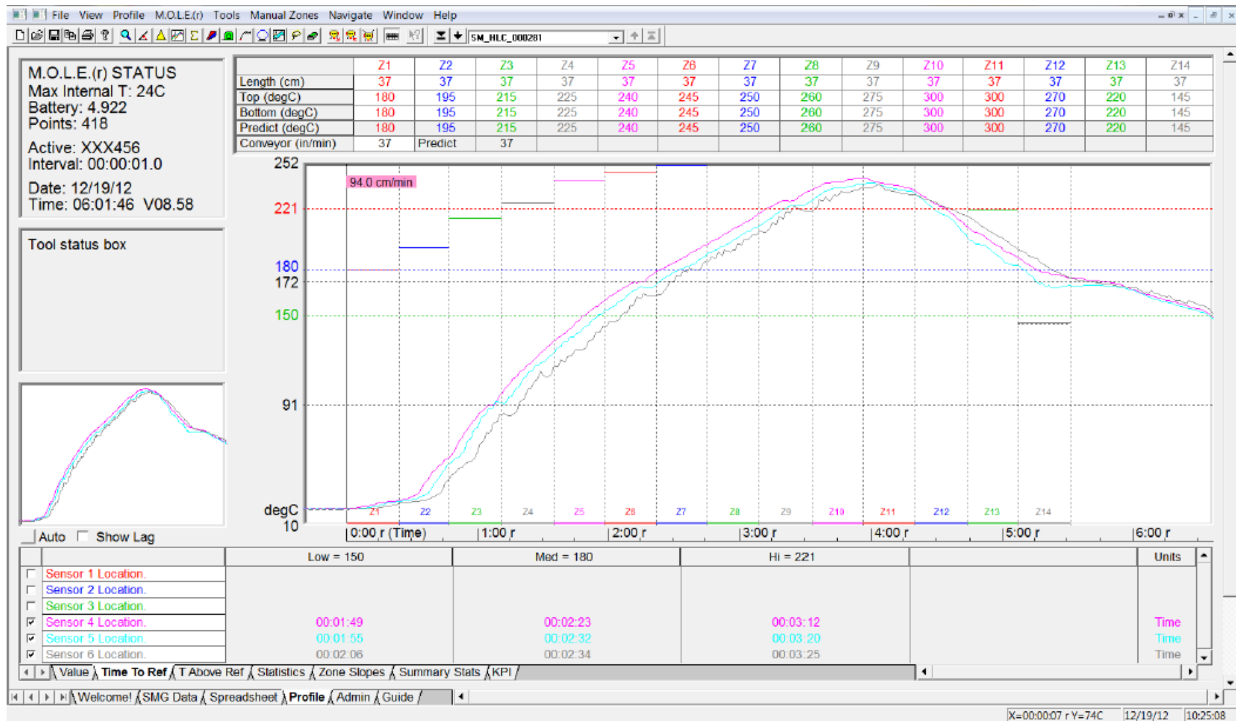


Figure 3.18 Phase II Bottom-Side Reflow Profile

3.3.2.8 Quality Assurance

Several quality assurance steps were taken. The resistance of each daisy-chained circuit component was checked by hand following reflow to eliminate them from inclusion in further testing. Boards were also optically inspected and x-ray analysis was used to determine typical solder-joint quality following reflow. In one instance, several components on one of the boards were sacrificed in a ‘pry test’ to assure the mechanical strength of the solder joints as reflowed.

Overall build quality was found to be very good. There were some solder-paste specific manufacturability issues. Some problems were found with the SBGA 600 components, of which a few components had missing or misaligned solder spheres/balls. In combination with a failure of the AOI algorithm for this component on the Juki KE-2080L, this led to the failure of several assembled SBGA 600 components.

3.3.2.9 Thermal Cycling Test Parameters and Equipment

As per the test plan the assemblies are subjected for thermal cycling testing. A modified JEDEC JESD22-A104-B standard high and low temperature test in a single zone environment chamber is used to assess the solder joint performance. The cycles have dwell temperatures of -40^{0}C to $+125^{0}$C and a ramp rate of 15^{0}C per minute. This results to a thermal profile with 45 minute ramps with 15 minute dwells and totals to 120 minutes for an overall cycle. Each test group are subjected to 3000 thermal cycles. The figure 3.19 shows the thermal profiles.

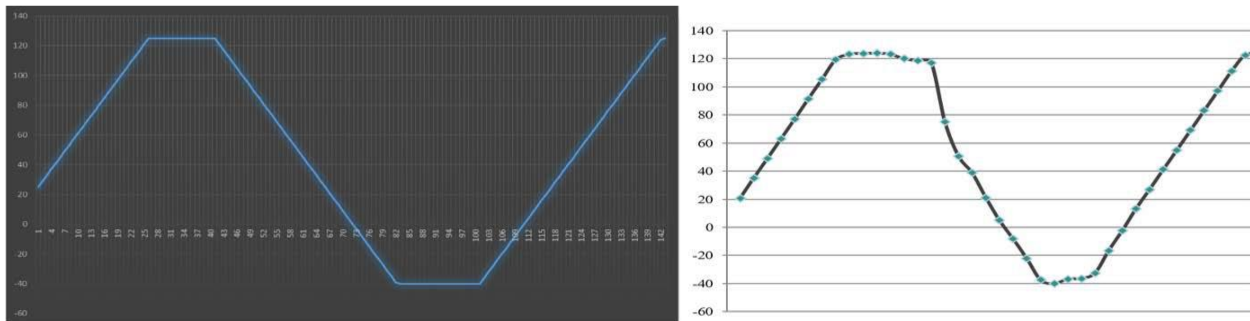


Figure 3.19 Thermal Profile used in TC testing of the TC1-SRJ test vehicle, Theoretical (left) vs Experimental (right)

Thermotron thermal cycling chambers are used for the thermal cycling testing and the same is shown in the figure 3.20

Figure 3.20 Thermotron Thermal cycling test chambers

3.3.2.10 Data Acquisition System

The electrical components used for this experiment are 'daisy-chained' for electrical continuity testing. The electrical resistance for each component was independently monitored. For the thermal cycling testing the test boards are mounted vertically on a heat-resistant plastic dividers before placing them inside the chamber. Temperature resistance wires are hand soldered to each active data channel and ground channel for all the test boards. A LabVIEW based data acquisition system developed by Dr. Thomas Sanders of Auburn University is used. A switch scanning system is coupled with a digital multimeter, to continuously monitor the resistance change of the components. This system is couple with LabVIEW software to control and record the test results. IPC-9701 standard is used to define the solder joint failure [89-92]. resistance increased (from

baseline) by over 100 ohms for 5 sequential resistance measurements. Figure 3.21 shows the data acquisition system. Figure 3.22 shows the schematic design of the monitoring system.

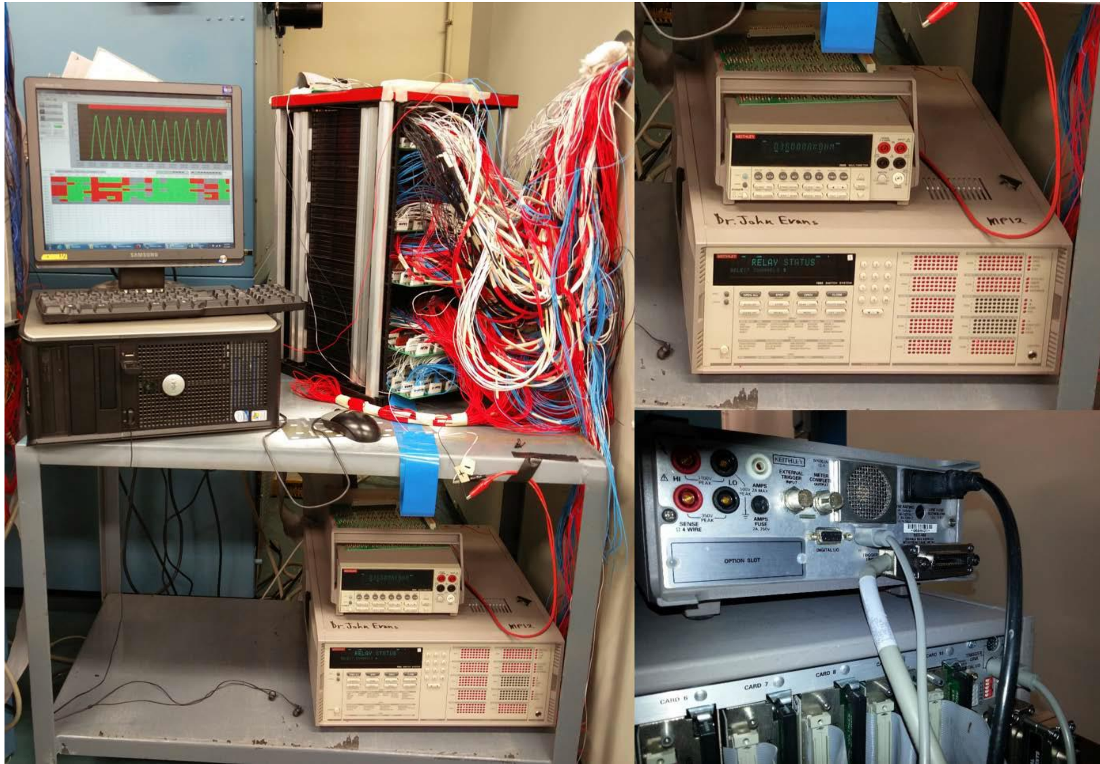


Figure 3.21 Full Monitoring System (left) Keithley Switching System and Digital Multi-Meter from front (right, top) and back (right, bottom). The DMM is sitting on top of the Switching System

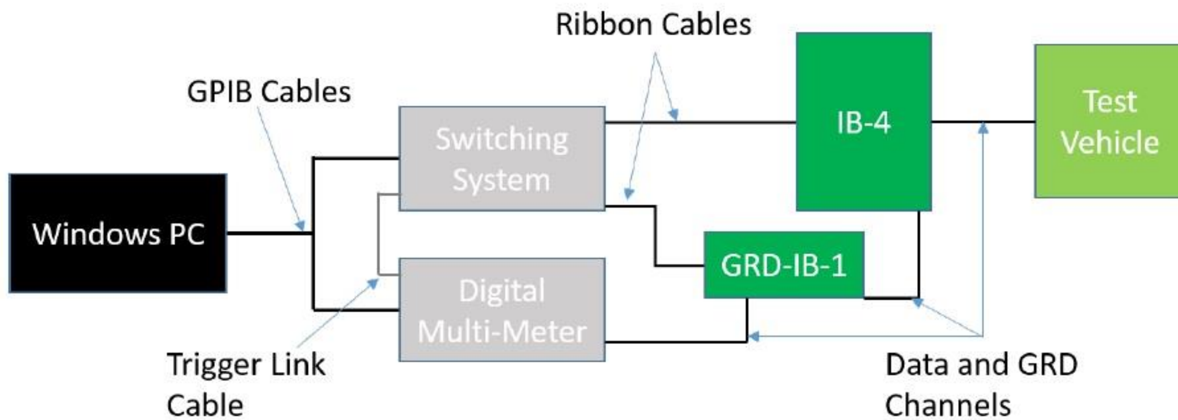


Figure 3.22 Diagram of the TC2-SRJ Monitoring System

3.4 Failure Analysis and Sample Preparation Protocol

Failed test samples taken out and cross-sectioned for further microscopic investigation. The cross-section and sample preparation procedure include cutting of the sample with diamond sectioning blade. This is followed by cold mounting using two-part epoxy system (resin+hardner). Cured samples are polished using semi-automated Pace Technologies FEMTO – 1000 (with NANO-1000T polishing head) machine. PSA backed silicon carbide (SiC) grinding grit papers are applied in sequence [93] as shown in the table 3.7

Standard Grit Size (ANSI) [US System]	**European P-grading System**	**Median Particle Diameter (microns)**	**Rc-30 Steel Surface Roughness (Ra-micron)**
240	P220	63	300
320	P360	45.5	
400	P800	21.8	120
600	P1200	15.3	75
800	P2400	6.5	
1200	P4000	2.5	20

Table 3.7 US and European Grip Paper standard systems [112]

Final polishing involves use of cloth pad and abrasive particles applied in form of slurry, paste or spray. Proper polishing is critical because your polishing steps must completely remove surface damage from all preceding sample preparation steps [94]. ATLANTIS Polishing Pad is used for both intermediate and final polishing, although this is always subject to refinement. The

intermediate polishing step was done using 1-micron alumina particles and the final polishing with 0.05-micron alumina.

Following polishing the samples are carbon coated and examined using scanning electron microscope (SEM). As the samples are metallic backscatter electron (BSE) mode of detection is used. Additionally, energy dispersive spectrometry (EDX) is done to record the material composition information [95].

Chapter 4. Reliability Test Results

4.1 Introduction

This project was split into 2 phases due to the complexity of project design, sample size and various test procedures. In this chapter, we will be discussing the reliability data gathered from Phase 1 and Phase 2. Tests carried out in Phase 1 include Drop, vibration and liquid shock. This was followed by thermal cycling tests. A 2-parameter Weibull (β, η) is used for analyzing the reliability data for all the packages. The slope (β) is the Weibull shape parameter which represents any change in the failure mode and the characteristic life (η) is the number of cycles at which 63.2% of the population is expected to fail. (ρ) Indicates the probability plot which explains how well the data fits the regression line.

4.2 Weibull Graphs and Results

4.2.1 Phase 1 Results

The Phase 1 results discuss the results from mechanical shock/drop performance tests. During the experiment, none of the QFN's and resistors failed at both no aged or aged. Only CABGA208 package with SAC305 solder bumps were used. 12 different solder pastes supplied from 8 different manufacturers are tested. Only 3 of the solder pastes results are discussed in this report as their performance was close to that of the baseline.

4.2.1.1. CABGA 208 [15mm, 0.8mm pitch]

Figure 4.1 shows the Weibull plot of boards that had CABGA 208 packages, built with SAC305 solder bumps and solder paste A at the best temperature profile. This test data has been considered as a baseline for the Phase 1 study. We can clearly see from the plot, the deterioration in the reliability after the aging. The characteristic lifetime of solder paste A reduced to 95 drops from 154 after aging. 30% BGA packages survived even after 300 drops in no age condition. But all the BGA packages tested after aging failed and the same can be seen in Figure 4.2.

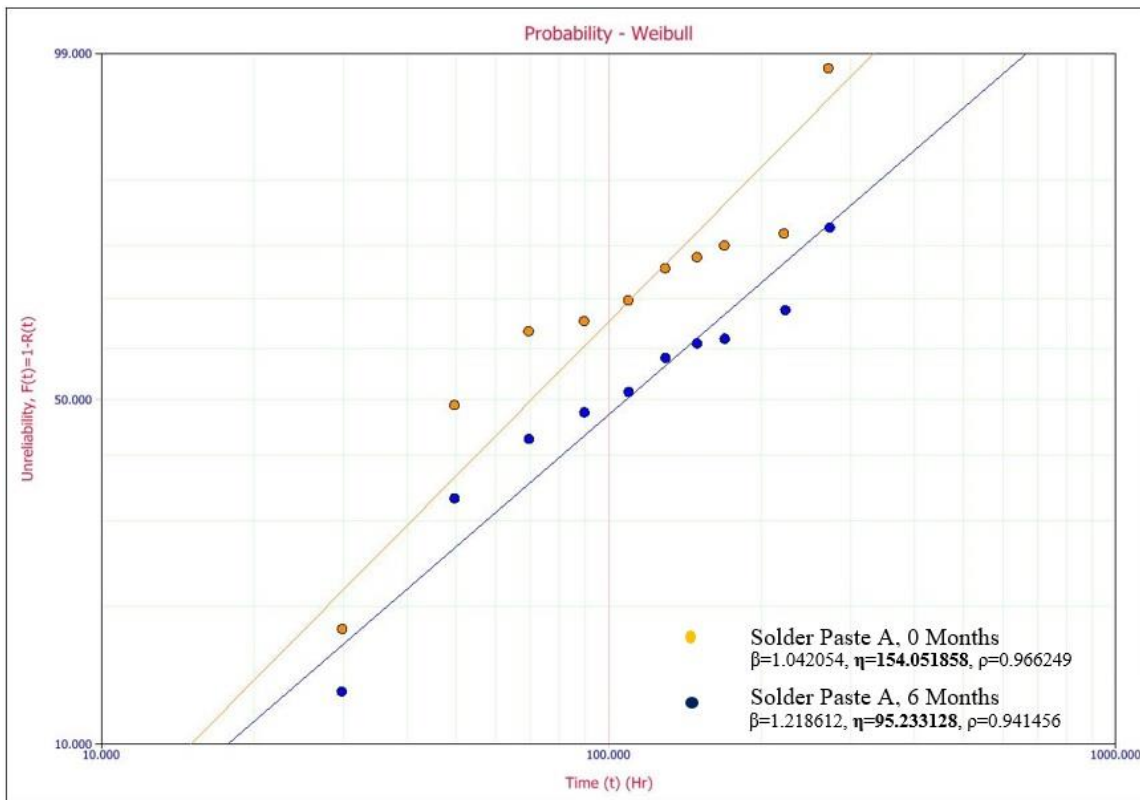


Figure 4.1 Drop impact reliability of the baseline material solder paste A at no aged and aged conditions.

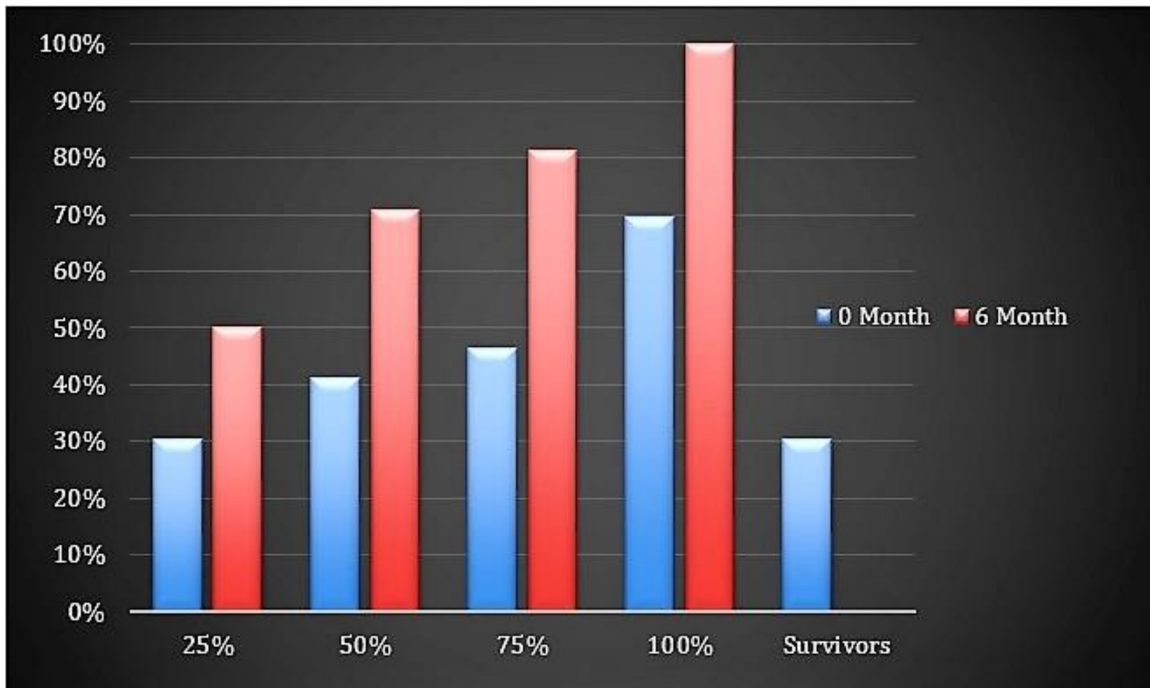


Figure 4.2 Percentage failure comparison of the baseline.

From the figure 4.3, we can see the solder paste C's characteristic lifetime is higher at 184 drops compared to 154 drops of the baseline at the no-aged condition. With aging the baseline Solder Paste, A proves to be more reliable. Figure 4.4 shows the percentage failure of the BGA's in both no aged and aged conditions during the testing. We can see that the performance of solder paste C was close to the baseline, and some packages survived after even after 300 drops.

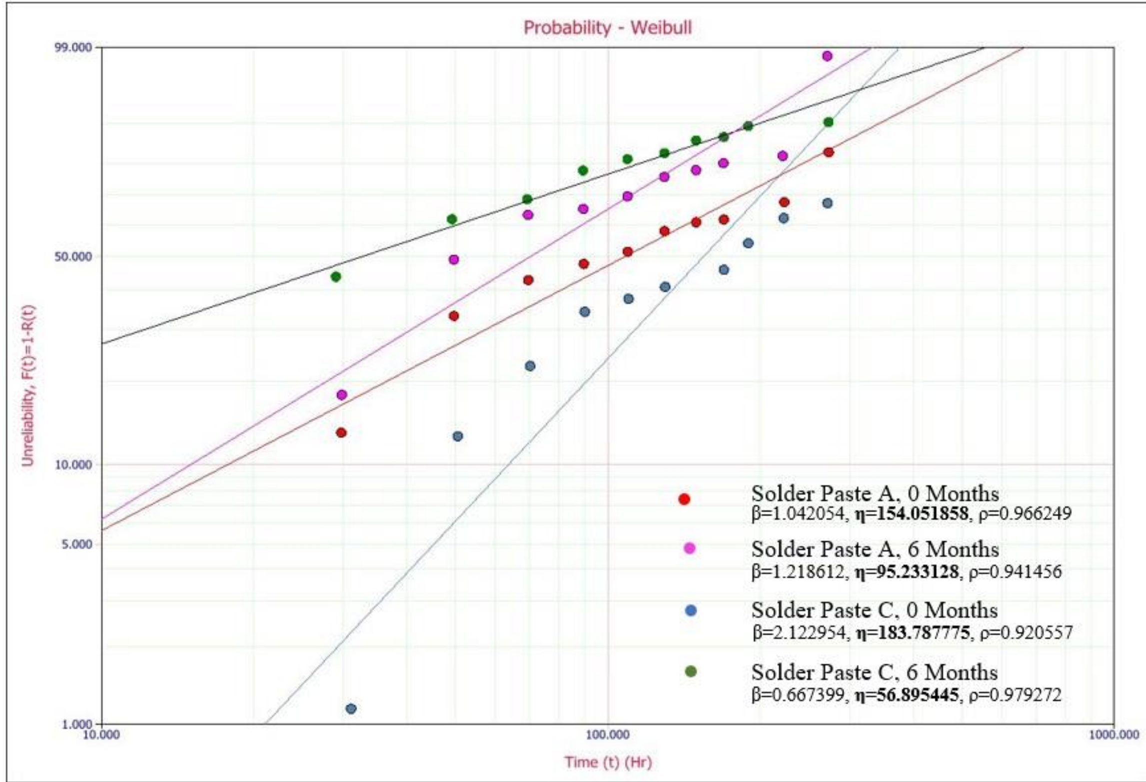


Figure 4.3 Drop impact reliability comparison of solder paste C with the baseline

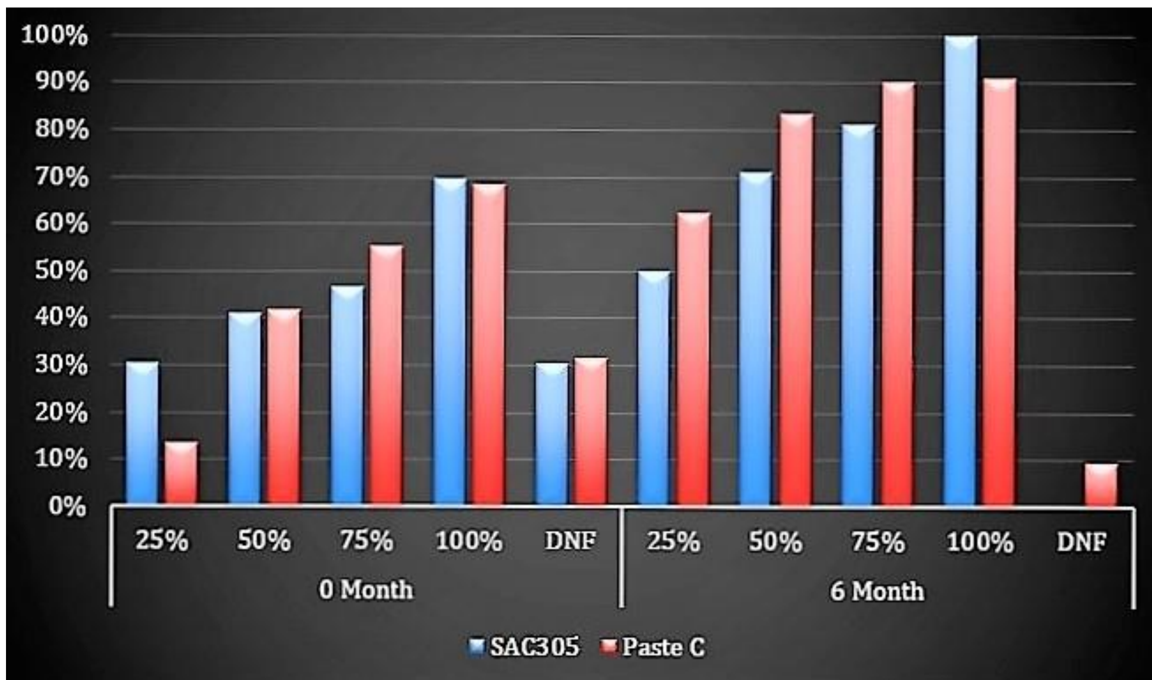


Figure 4.4 Percentage failure comparison of solder paste C with the baseline.

Solder paste F had a characteristic life of 187 drops compared to that of 154 drops of the baseline at no aged condition, something similar to the paste C performance. But after aging the characteristic life of solder paste F and the baseline decreased to 76 drops and 95 drops respectively. The same can be seen in figure 4.5 and Figure 4.6

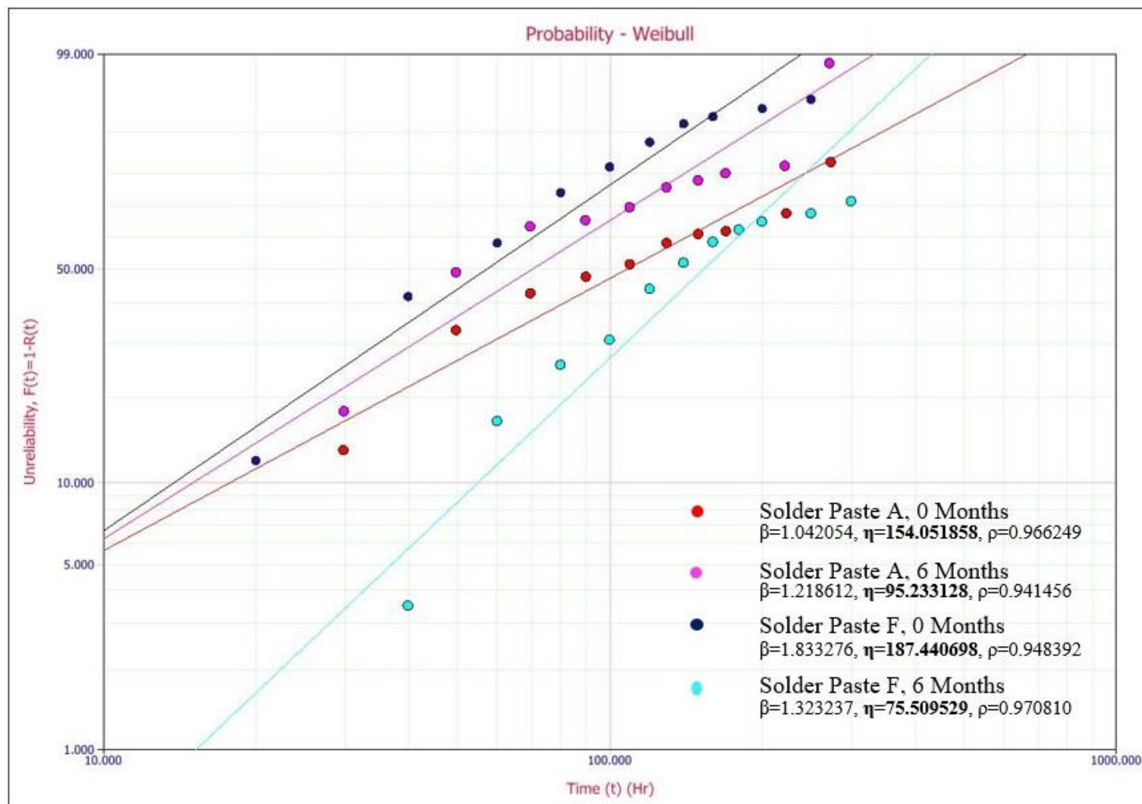


Figure 4.5 Drop impact reliability comparison of solder paste F with the baseline

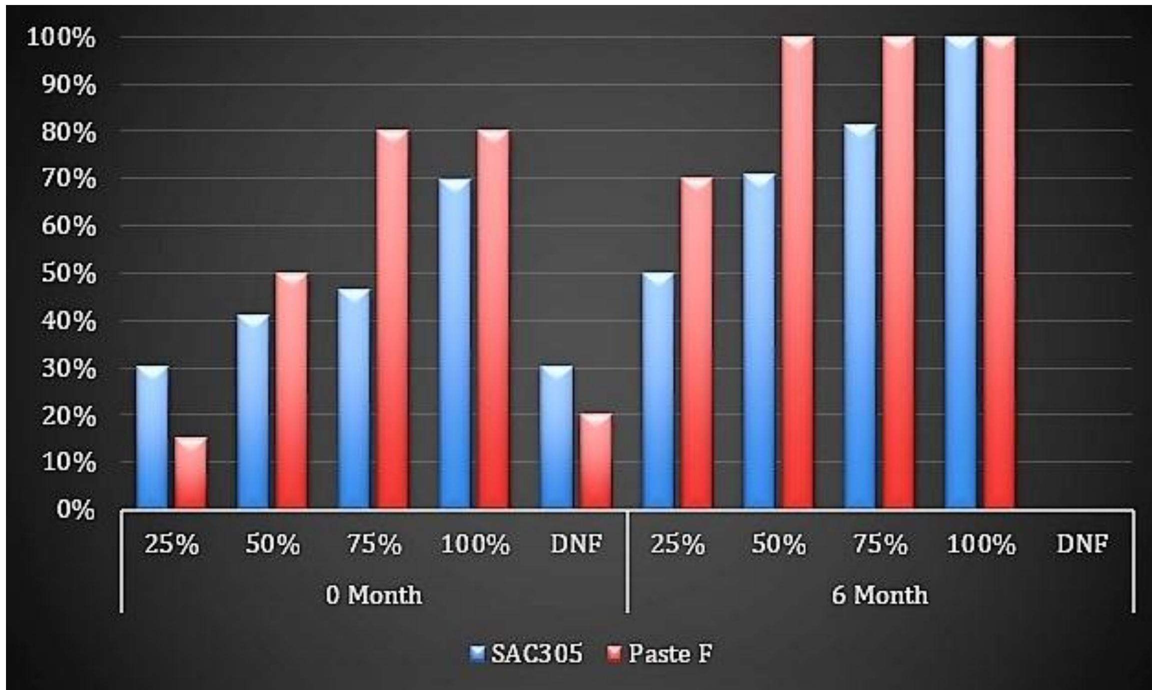


Figure 4.6 Percentage failure comparison of solder paste F with the baseline.

Solder paste J proved to be less reliable at both no aged and aged condition when compared with the baseline. The characteristic life values of this paste is lower than that of the baseline at both no-aged and aged conditions. The same can be seen in figure 4.7 and 4.8.

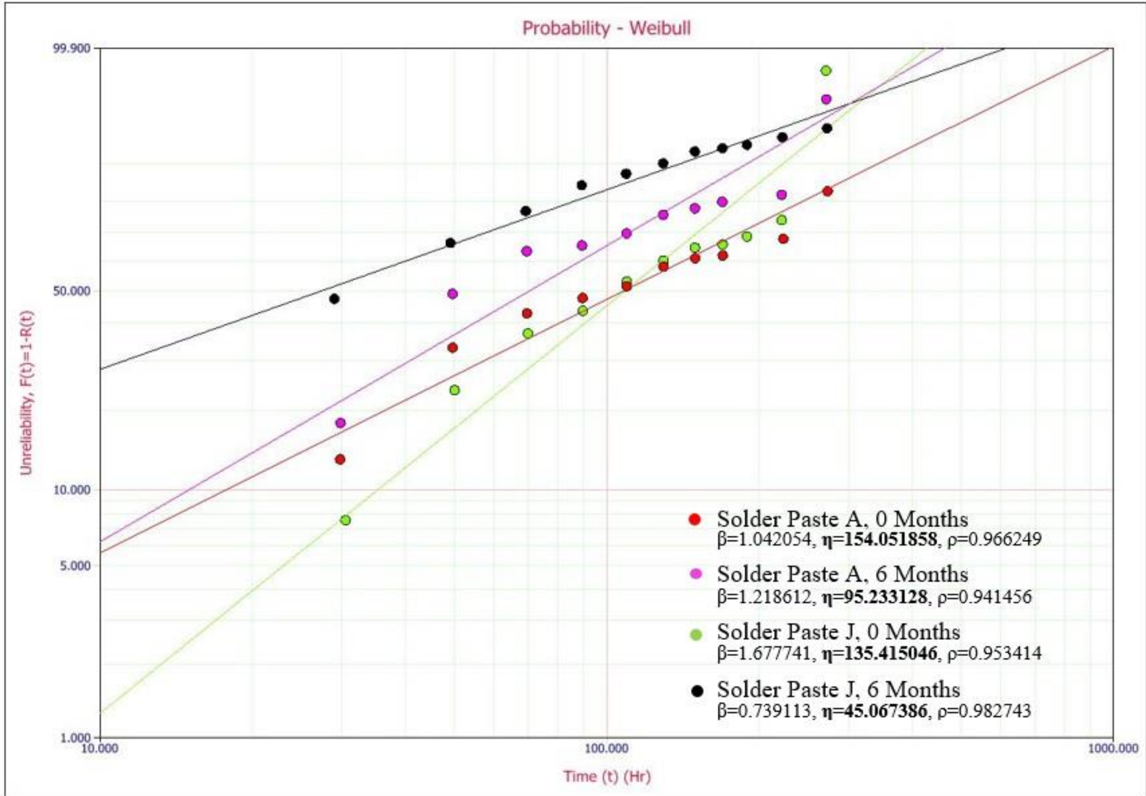


Figure 4.7 Drop impact reliability comparison of solder paste J with the baseline

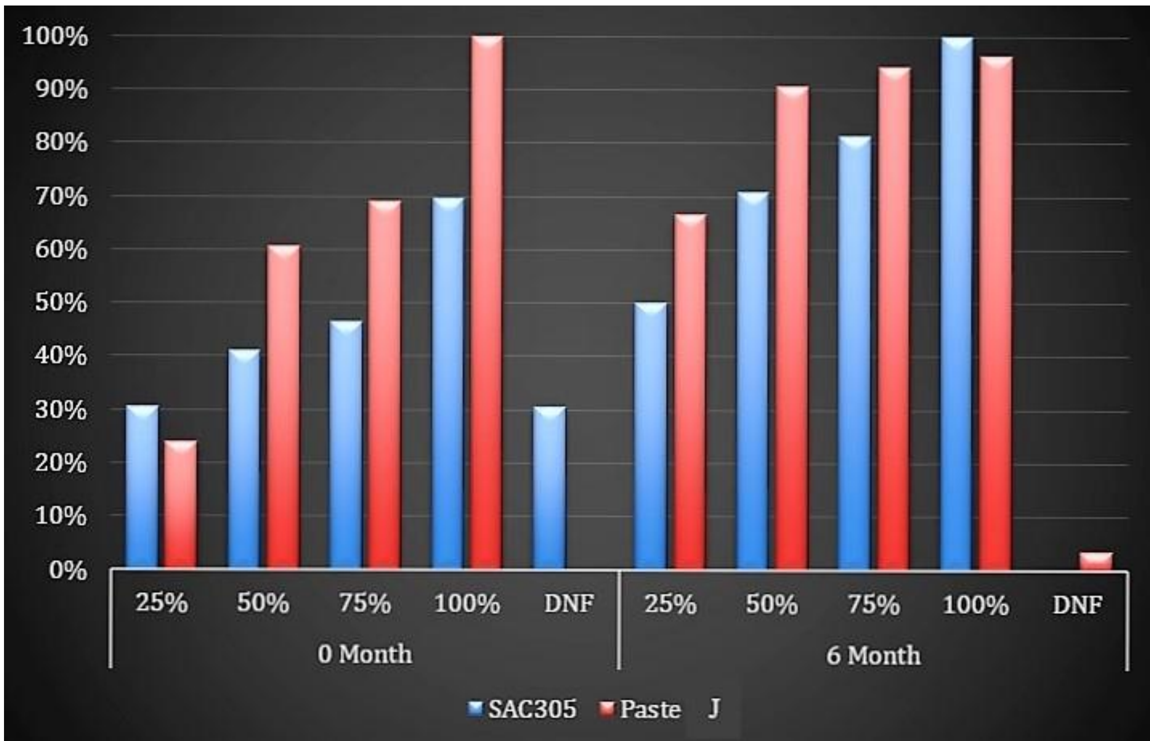


Figure 4.8 Percentage failure comparison of solder paste J with the baseline.

Phase 1 testing also included vibration and liquid shock testing. All the solder pastes were tested under these conditions. SAC305 solder spheres and Paste A remained as baseline for all the phase 1 tests. The top 5 performing solder paste materials from Liquid shock, Vibration and Drop testing were chosen for the phase 2

Tables 4.1, 4.2 and 4.3 shows the test summary of Drop, vibration and Liquid shock tests.

Unclassified//FOR OFFICIAL USE ONLY

Solder Paste Materials	Overall Performance F-Fair/ G-Good/B-Bad	Stencil Size Improvents (4 mil, 6 mil)	Profile Improvements (H/L/B)	Matched Improvements (Y/N)
Alpha SAC305	Baseline	Only in 6 mil	Only in Best	N/A
Accurus Cyclomax	F	Only in 6 mil	Only in Best	N/A
Accurus EcoUoy	B	Only in 6 mil	Only in Best	N/A
AIM	B	Only in 6 mil	Only in Best	N/A
Alpha Innolot	**F**	**None**	**None**	**Y**
Alpha Maxrel Plus	**G**	**4 mil**	**Best (0m)**	**N**
Henkel 90SCLF318AGS88.5	B	None	None	N/A
Henkel 90SCHF212DAP88.5	B	None	None	N/A
Heraeus Innolot	B	None	None	N
Heraeus HT1.02	B	None	None	N
Indium 8399Y	B	None	Non e	N
Indium Material 2	F	None	None	N
Inventec	B	Only in 6 mil	Only in Best	N/A
Senju M794(SAC 305)	B	None	None	N/A
Senju M759	B	Only in 6 mil	Only in Best	N
Senju 770	**F**	**Only in 6 mil**	**Only in Best**	**N**

Trysail II

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Table 4.1 Drop test summary

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Solder Paste Masterials	Overall Performance F-Fair/B-Bad	Stencil Size Improvents (4 mil, 6 mil)	Profile Improvements (H/L/B)	Matched Improvements
Alpha CVP390 (Baseline)	Baseline	Only 6 mil	Only Best	N/A
Accurus Cyclomax	B	Only 6 mil	Only Best	N/A
Accurus EcoUoy	B	Only 6 mil	Only Best	N/A
AIM	B	Only 6 mil	Only Best	N/A
Alpha Innolot	**F**	**None**	**None**	**N**
Alpha Maxrel Plus	B	None	None	Y
Henkel 90SCLF318AGS88.5	**F**	**6**	**High**	N/A
Henkel 90SCHF212DAP88.5	B	None	None	N/A
Heraeus Innolot	B	None	None	N
Heraeus HT1.02	B	Only 6 mil	High	N
Indium 8399Y	B	None	None	N
Indium Material 2	**F**	**6**	**Low**	N
Inventec*	B	Only 6 mil	Only Best	N/A
Senju M794 (SAC 305)	F	6	High	N
Senju M759	B	Only 6 mil	Only Best	N
Senju 770	B	Only 6 mil	Only Best	N

Trysail II

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Table 4.2 Vibration test summary

Unclassified//FOR OFFICIAL USE ONLY

Solder Paste materials	Overall Performance VG-Very Good/G-Good/B-Bad	Package	Stencil Size Improvents (4 mil, 6 mil)	Profile Improvements (H/L/B)	Matched Improvements (Y/N)
Alpha SAC305	Baseline	SBGA 304	Only In 6 mil	Only in Best	N/A
Accurus Cyclomax	G	SBGA304	Only In 6 mil	Only in Best	N/A
Accurus EcoUoy	B	N/A	Only In 6 mil	Only in Best	N/A
AIM	**VG**	**2512**	**Only In 6 mil**	**Only in Best**	**N/A**
Alpha Innolot	**VG**	**N/A**	**6**	**Low**	**Y**
Alpha Maxrel Plus	G	None	None	None	N/A
Henkel 90SCLF318AGS88.5	**VG**	**SBGA304**	**N/A**	**N/A**	**N/A**
Henkel 90SCHF212DAP88.5	G	SBGA304	None	None	**N/A**
Heraeus Innolot	**VG**	**SBGA304**	**None**	**None**	**N**
Heraeus HT1.02	G	None	None	None	N
Indium 8399Y	B	PBGA1156	None	None	**N**
Indium Material 2	**VG**	**SBGA304**	**None**	**None**	**N**
Inventec	**VG**	**2512**	**Only In 6 mil**	**Only in Best**	**N/A**
Senju M794 (SAC305)	G	SBGA304	None	None	**N/A**
Senju M759	B	SBGA304	Only in 6 mil	Only in Best	N
Senju 770	G	CABGA208	Only in 6 mil	Only in Best	N

Trysail II

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Table 4.3 Liquid shock test summary

4.2.2. Phase 2 Results

The Top 5 solder paste materials chosen from phase 1 were used in building the TC2-SRJ boards. MEGTRON6 was used as the substrate material. All the BGA packages have SAC305 solder spheres. The stencil thicknesses used are 5mil and 3mil for top-side and bottom side assemblies respectively. Bottom-side boards have been double-printed to get adequate solder volume on the small-pitch components. Otherwise, all the print parameters are held constant for all assemblies.

All the BGA packages have SAC305 solder balls, five different solder paste materials from different suppliers have been used. The stencil thicknesses used are 5mil and 3mil for top-side and bottom side assemblies respectively. Bottom-side boards have been double-printed to get adequate solder volume on the small-pitch components. Otherwise, all the print parameters are held constant for all assemblies

A total of 260 test boards were built, along with additional 20 boards used solely for setup purposes during assembly. The no-aging (0-month) were tested right after the build, 6-month, 12-month and 24- month aging boards were isothermally aged at 75^{0}C before their testing. For each material, there were 9 ‘Top-Side’ boards and 4 ‘Bottom-Side’ boards for every aging group. This yields a total of 52 boards per material (36 Top and 16 Bottom), with 13 boards in each aging group. Below are the 0 and 6-months results of this test, paste Material 2 Innolot has been chosen to be the baseline and the performance of the remaining 4 paste materials are studied against the baseline.

4.2.2.1 CABGA 256 [17mm, 1.0mm pitch]

This is a larger BGA package measuring at 17mm X 17mm with 1.0mm pitch. This component has SAC 305 spheres and is assembled on the Top-Side TC2-SRJ boards. This along with CVBGA 432 are one of the first failing components in this test. The same failure trend was seen during TC1-SRJ testing.

In the Weibull graphs below we present the reliability performance of the paste material 3 and 4 chosen from Phase 1 based on their performance from mechanical testing (Vibration and Drop. Figure 4.9 shows the thermal cycling reliability of the above-mentioned paste materials with the baseline Innolot at no-aged condition. We can see that the characteristic life of paste 4 match closely with the baseline Innolot. The same trend follows with 6-months aged data and can be seen in Figure 4.10.

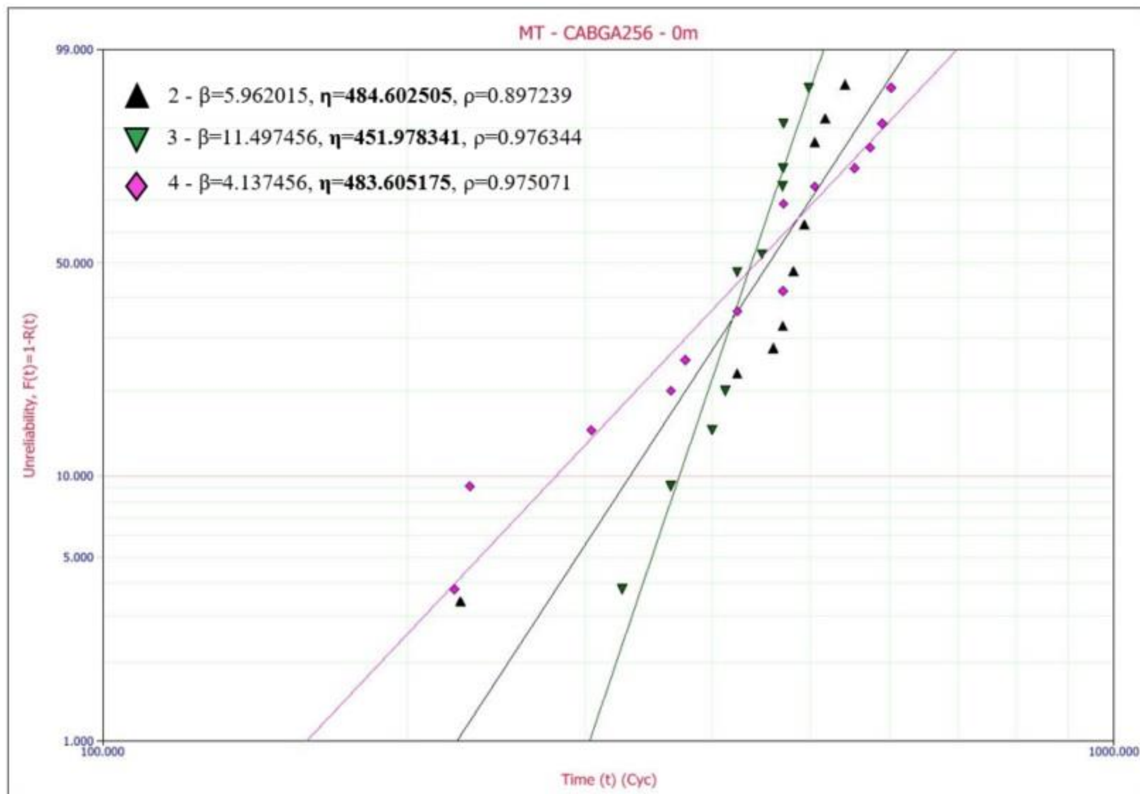


Figure 4.9 Thermal Cycling reliability comparison of materials 3 and 4 with the baseline 2 (Innolot) at no-aging

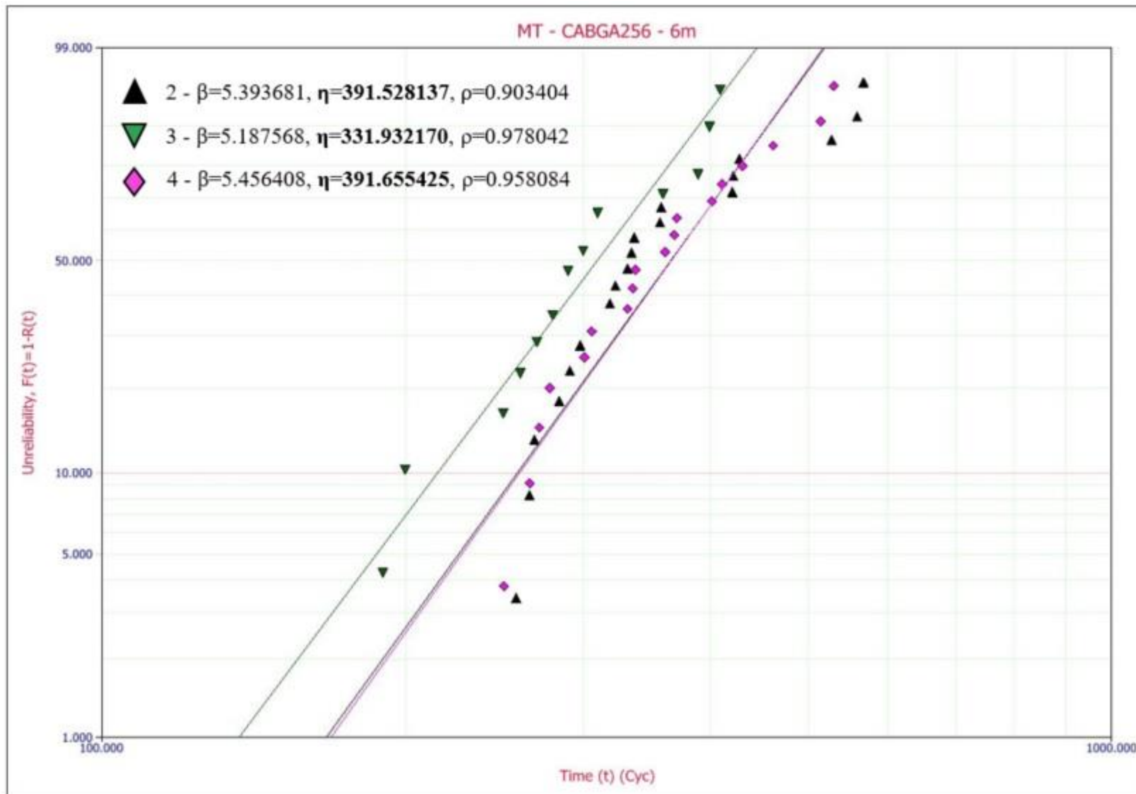


Figure 4.10 Thermal Cycling reliability comparison of materials 3 and 4 with the baseline 2 (Innolot) after 6-months aging

Weibull graphs 4.11 and 4.12 shows the reliability of all the pastes chosen from phase 1, this include both mechanical testing and liquid shock testing. From Figure 4.11 we can clearly see that characteristic life of paste 5 is substantially higher than the baseline Innolot and the other pastes. The same trend can be seen in the characteristic life numbers from 6-month aged test results. Graph below show the IMC thickness measurements for no-aged and aged CABGA256 components. There is a considerable increase in the thickness of IMC layer with aging. Paste 5 las the least IMC growth and the same can be seen in graph below. The Table 4.4 summarizes the

CABA256 reliability performance and paste material 4 and 5 can be a suitable replacement for the Innolot paste

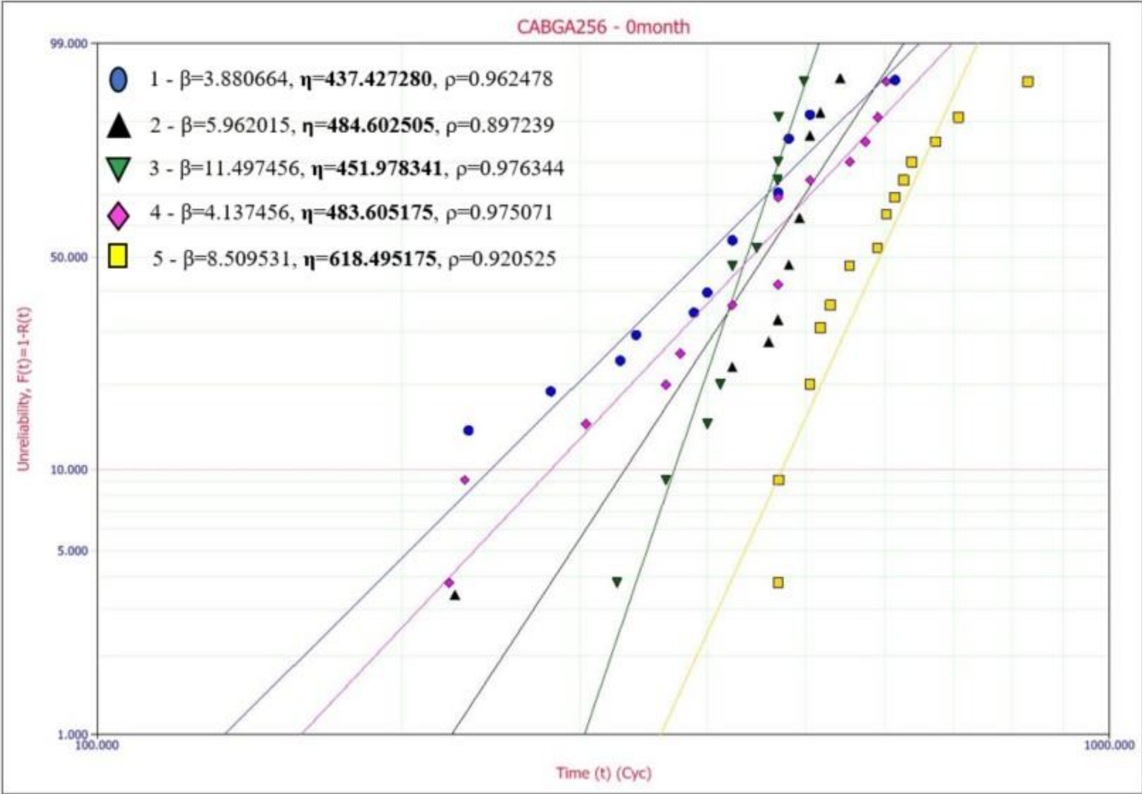


Figure 4.11 Thermal Cycling reliability comparison at no-aging

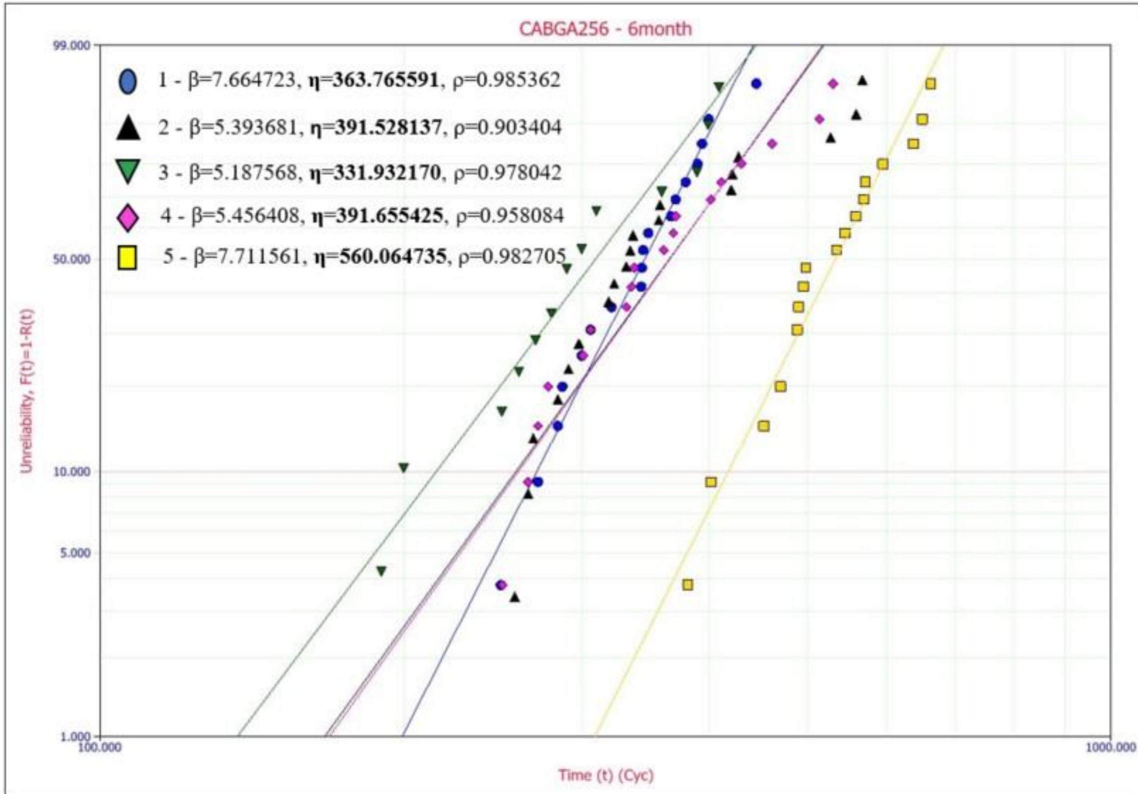


Figure 4.12 Thermal Cycling reliability comparison after 6-months aging

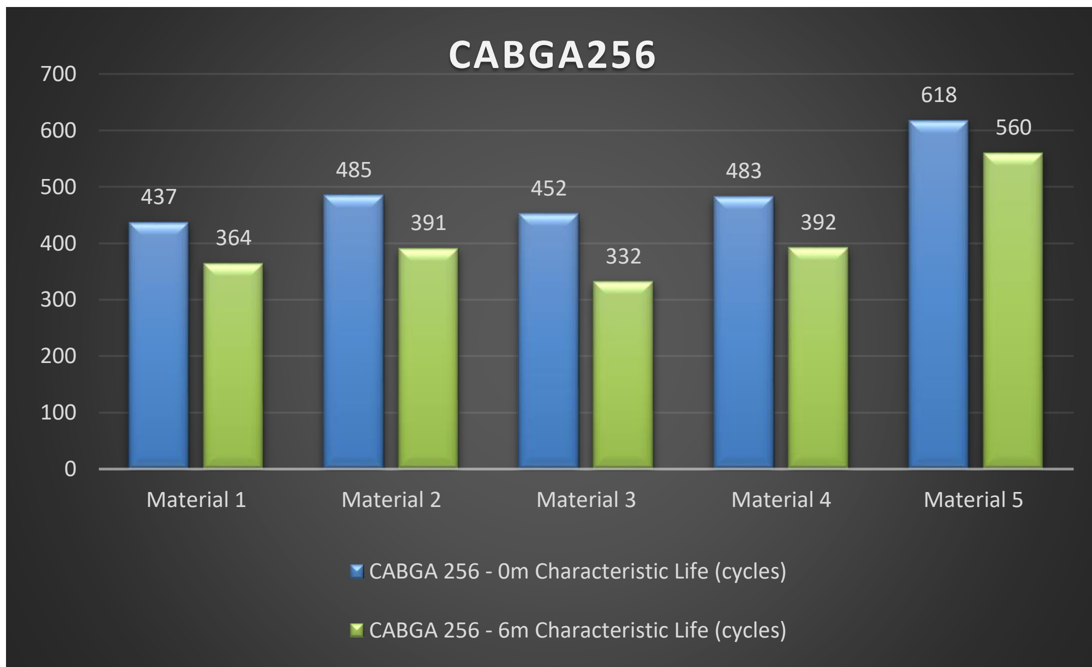
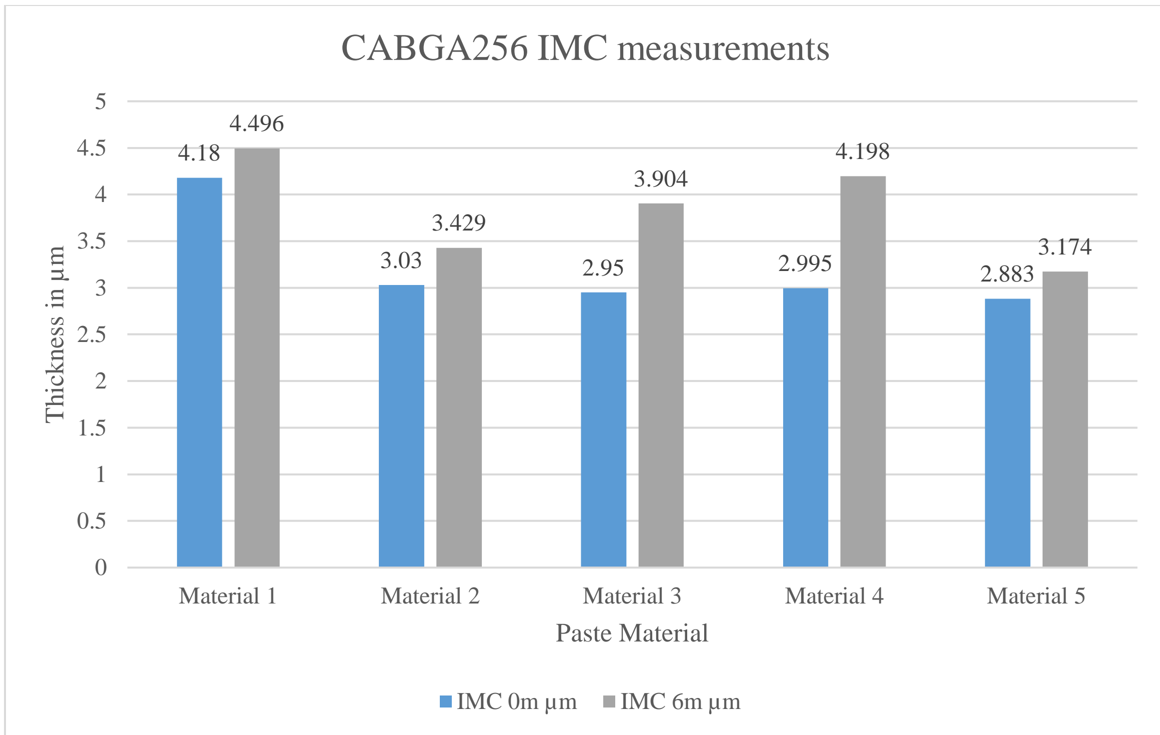


Table 4.4 CABGA256 test summary



IMC thickness measurement for CABGA256

4.2.2.2 CABGA 208 [15mm, 0.8mm Pitch]

This is a commonly used package in the electronics industry. Also, an important one for this test and it has been used in both Phase 1 and Phase 2 testing. Its measures 15mm X 15mm with 0.8mm pitch. This component has SAC spheres and is assembled on both the Top-Side and Bottom-Side TC2-SRJ boards. Hence, we have substantial amount of failure data available for it.

In the Weibull graphs below we present the reliability performance of the paste material 3 and 4 chosen from Phase 1 based on their performance from mechanical testing (Vibration and Drop. Figure 4.11 shows the thermal cycling reliability of the above-mentioned paste materials with the baseline Innolot at no-aged condition. We can see that the characteristic life of paste 3 and 4 are considerably higher than the baseline Innolot. The same trend follows with 6-months aged data and can be seen in Figure 4.12.

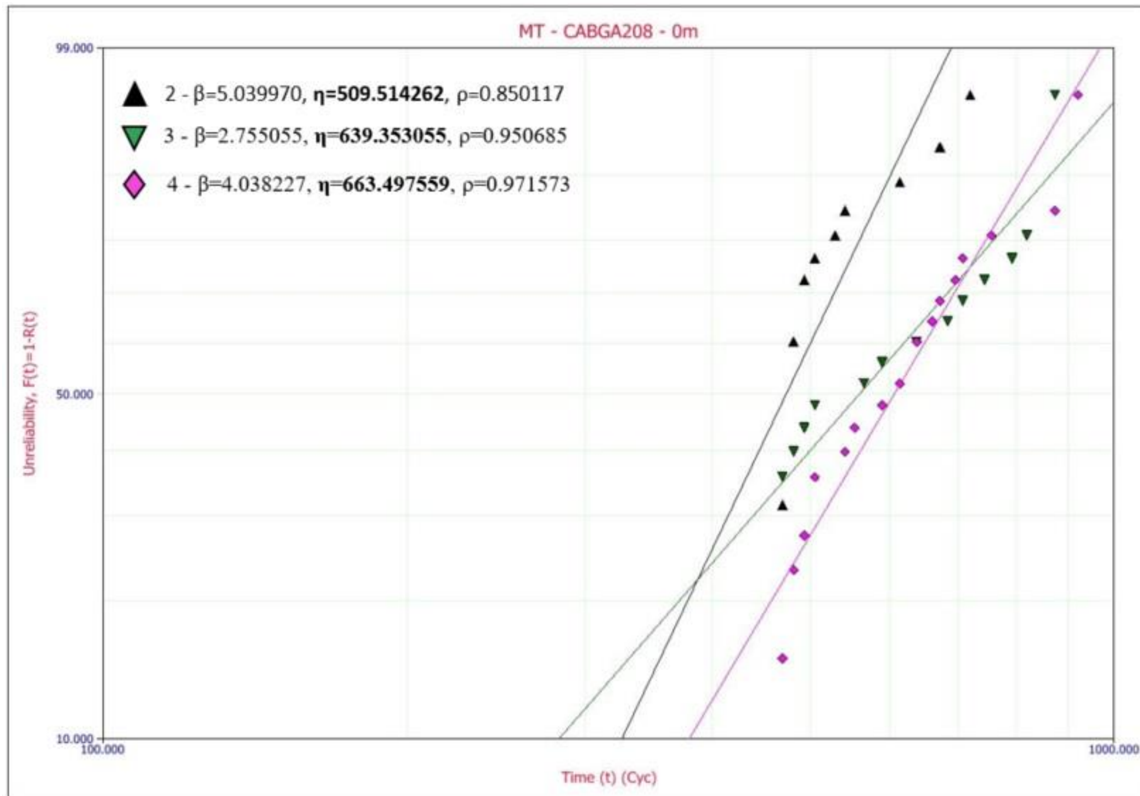


Figure 4.13 Thermal Cycling reliability comparison of materials 3 and 4 with the baseline 2 (Innolot) at no-aging

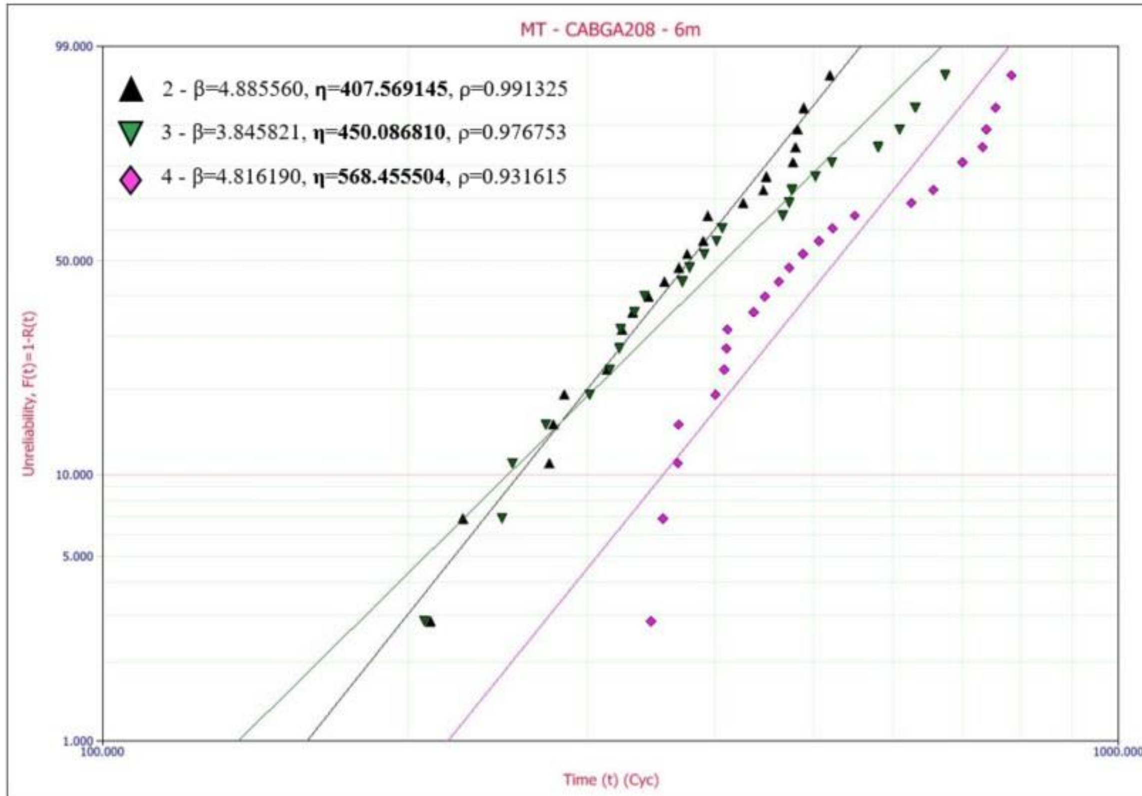


Figure 4.14 Thermal Cycling reliability comparison of materials 3 and 4 with the baseline 2 (Innolot) after 6-months aging

Weibull graphs 4.13 and 4.14 shows the reliability of all the pastes chosen from phase 1, this include both mechanical testing and liquid shock testing. From Figure 4.13 we can clearly see that characteristic life of paste 5 is substantially higher than the baseline Innolot and all other pastes perform better than the baseline Innolot. The same trend can be seen in the characteristic life numbers from 6-month aged test results from Figure 4.14. Graph below show the IMC thickness measurements for no-aged and aged CABGA208 components. There is a considerable increase in the thickness of IMC layer with aging. Paste 5 las the least IMC growth and the same can be seen in graph below. The table summarizes the CABA208 reliability performance, though all the pastes performed better than the baseline the paste material 5 has the highest characteristic life and can be considered as a suitable replacement for the Innolot paste.

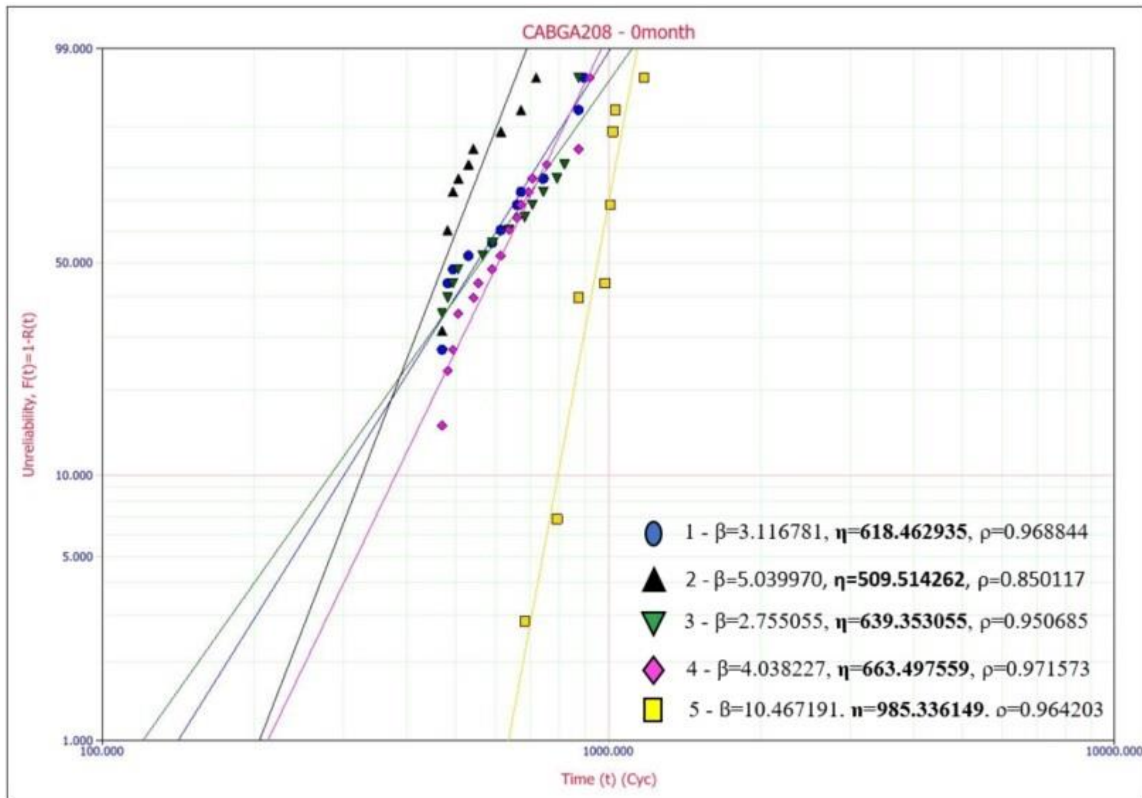


Figure 4.15 Thermal Cycling reliability comparison at no-aging

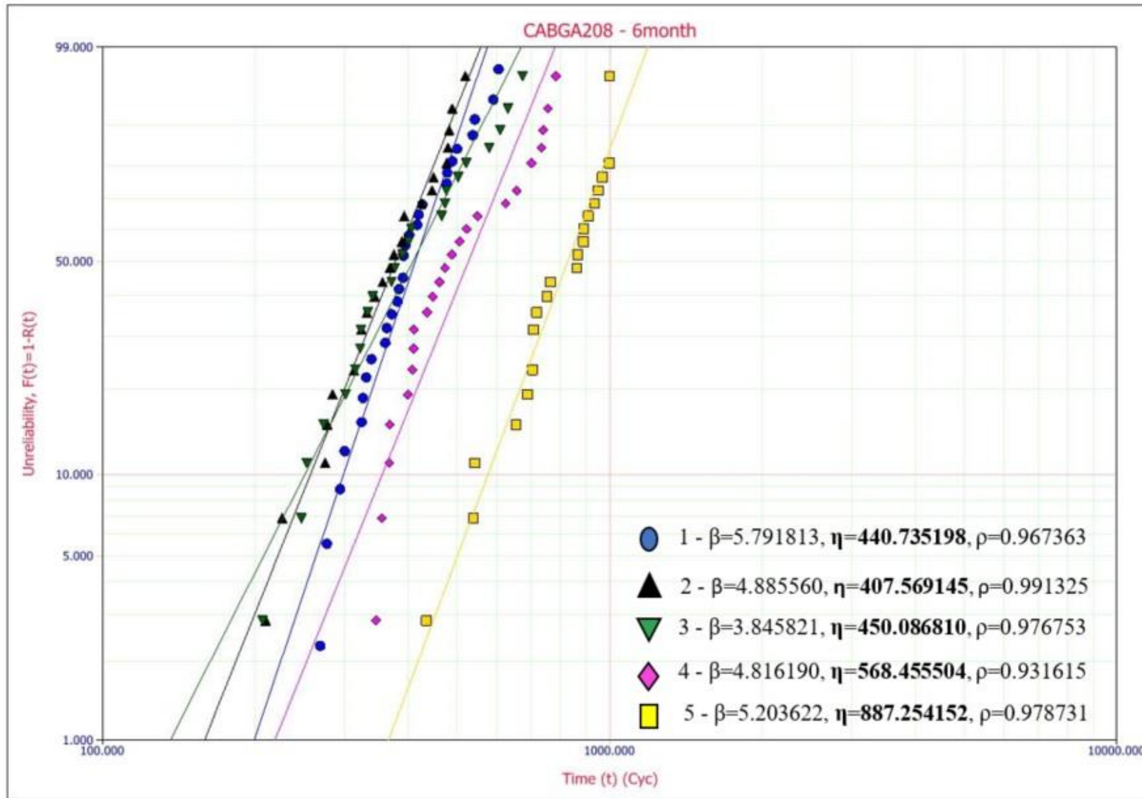


Figure 4.16 Thermal Cycling reliability comparison after 6-months aging

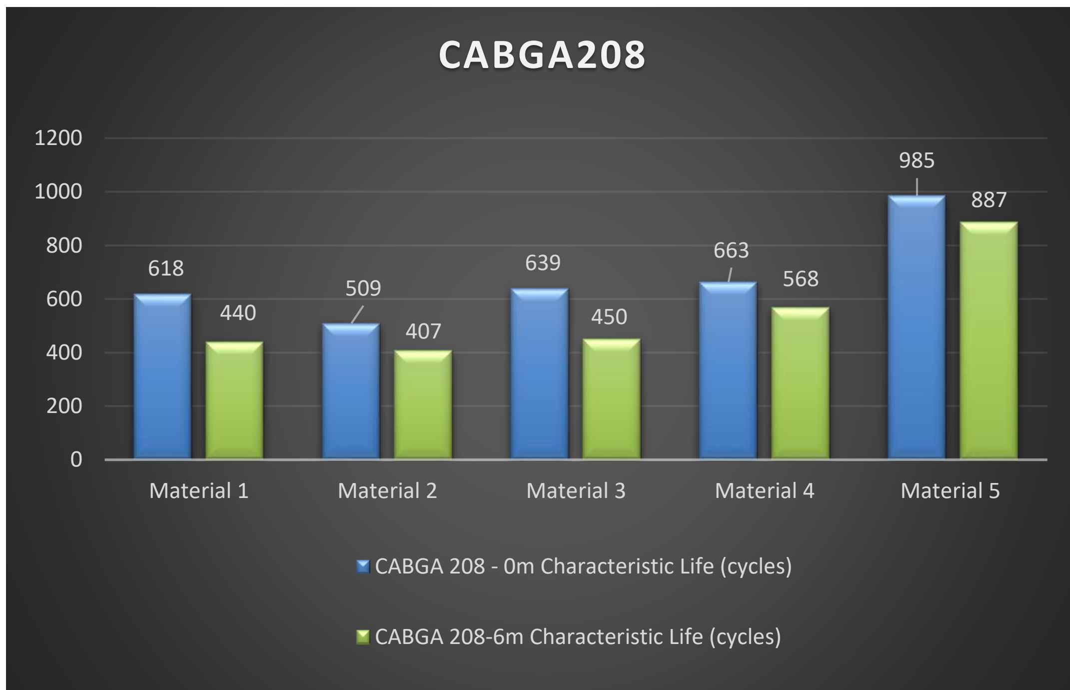
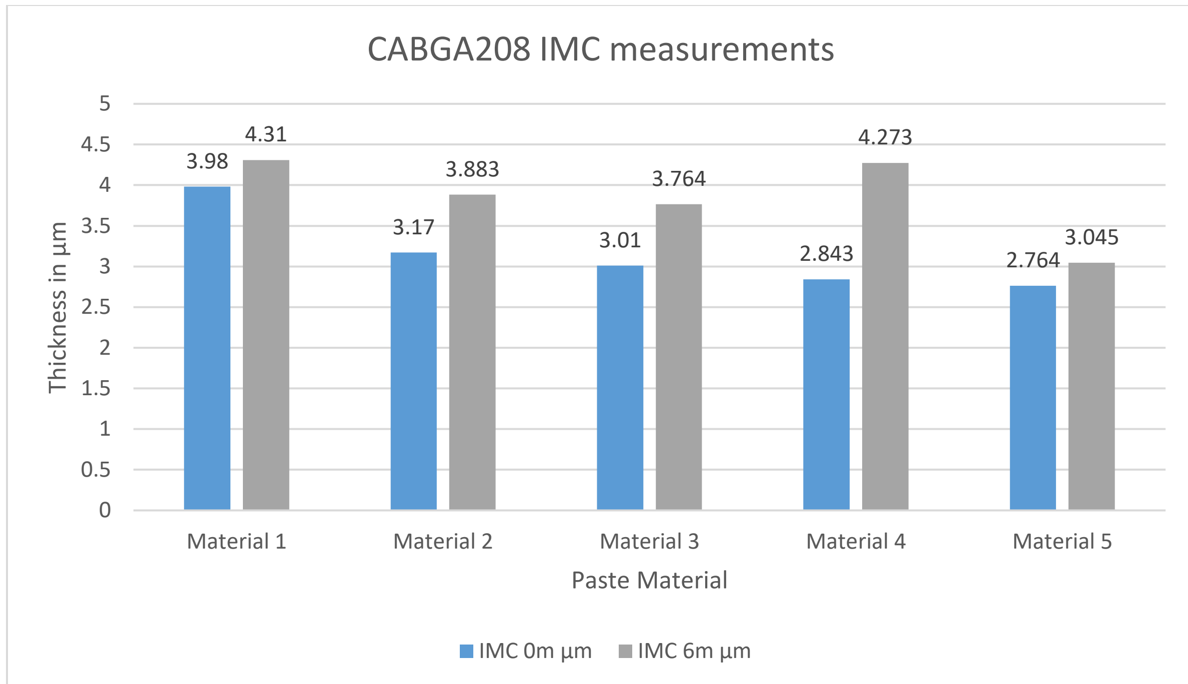


Table 4.5 CABGA208 test summary



IMC thickness measurement for CABGA208

4.2.2.3 CVBGA 432 [13mm, 0.4mm Pitch]

The CVBGA 432 has the finest pitch of any BGA component used in this test (at 0.4mm, tied with CVBGA 97). However, it measures 13mm X 13mm, making it significantly larger than the CVBGA 97. This component is found only on the Bottom-Side of the TC2-SRJ test vehicle.

The CVBGA 432 (along with the CABGA 256) is one of the first-failing components in phase 2 testing. This package exhibits lower reliability when compared with the CABGA256 and CABGA 208. Figures 4.17 and 4.18 shows the reliability performance of these packages at both no-aged and aged conditions. We can see that the characteristic life numbers of all the packages matches closely with the baseline Innolot data.

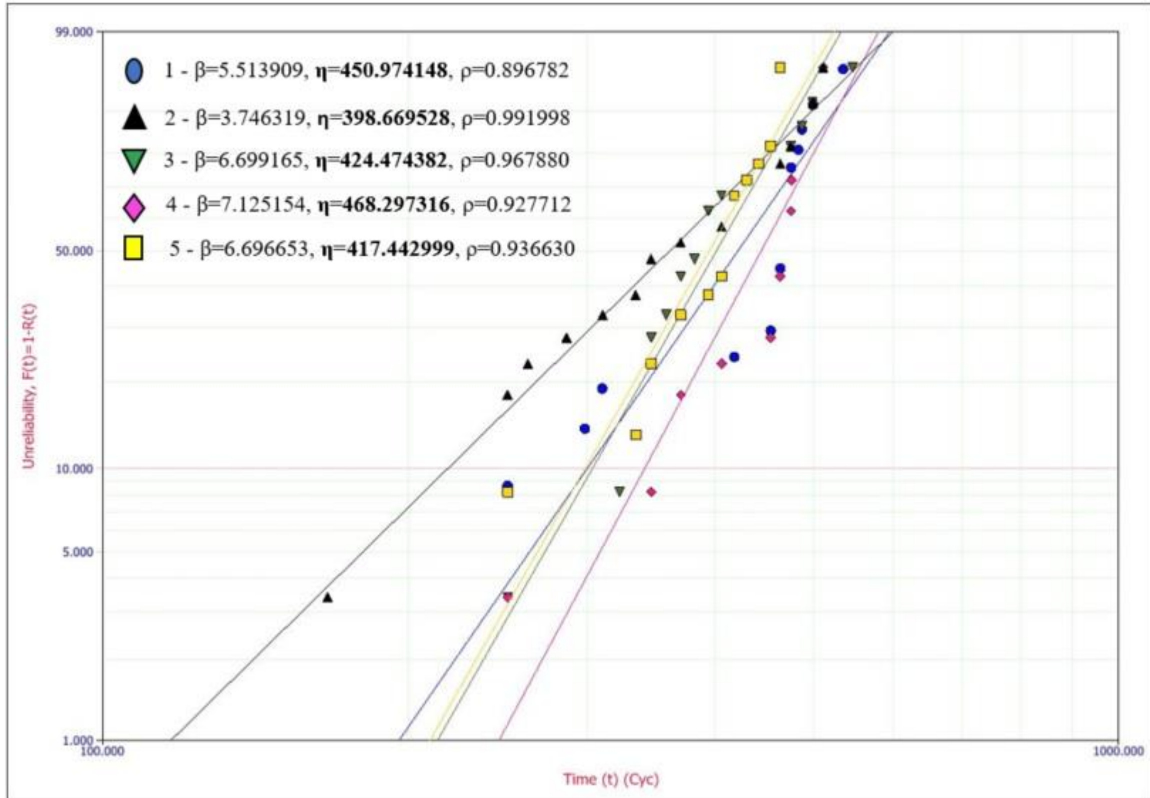


Figure 4.17 Thermal Cycling reliability comparison at no-aging

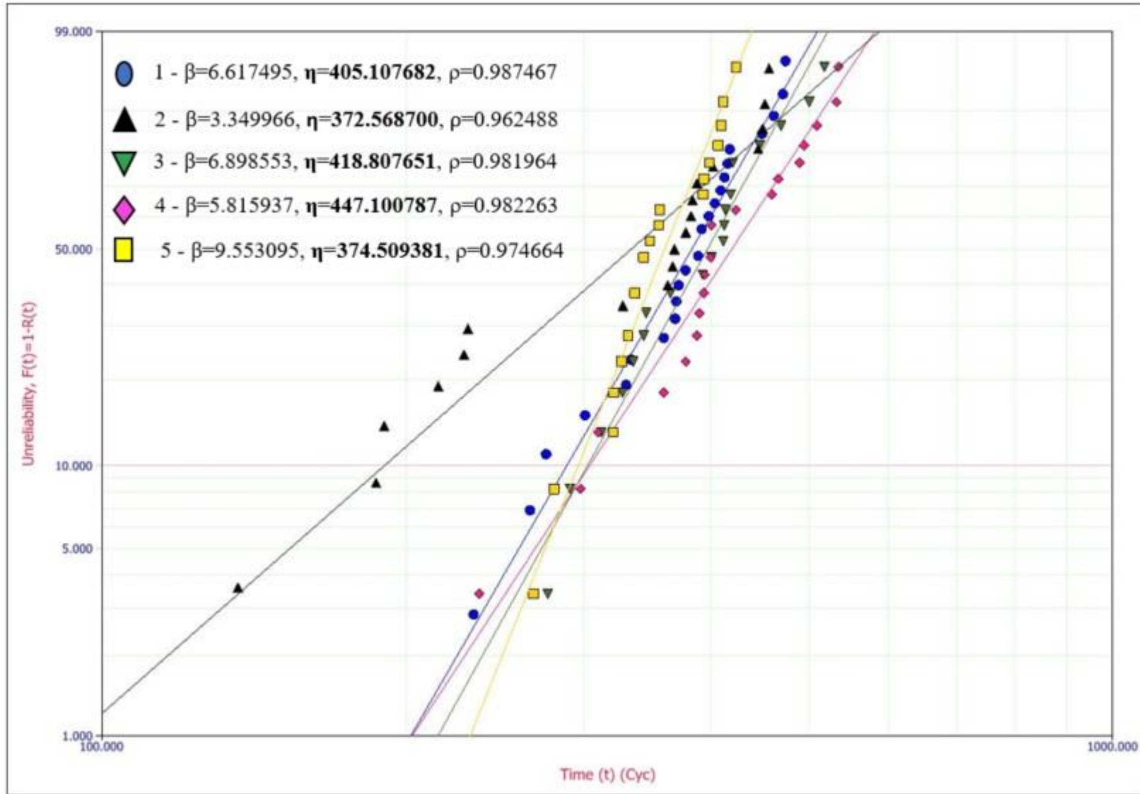


Figure 4.18 Thermal Cycling reliability comparison after 6-months aging

4.2.2.4 SMR2512

These are some of the larges resistors available in the market. All the 2512 resistors are mounted on the Top-Side boards. They use 100%Tin instead of SAC305 and are connected in series of 5 on 2 channels. Figures 4.19 and 4.20 shows the reliability performance of the pastes at no-aged and aged condition. We can see that there is a shift in the trend when compared to the BGA data. Reliability performance of paste material 3 is similar to that of the baseline. Form this data we cannot conclude a replacement for the baseline Innolot material.

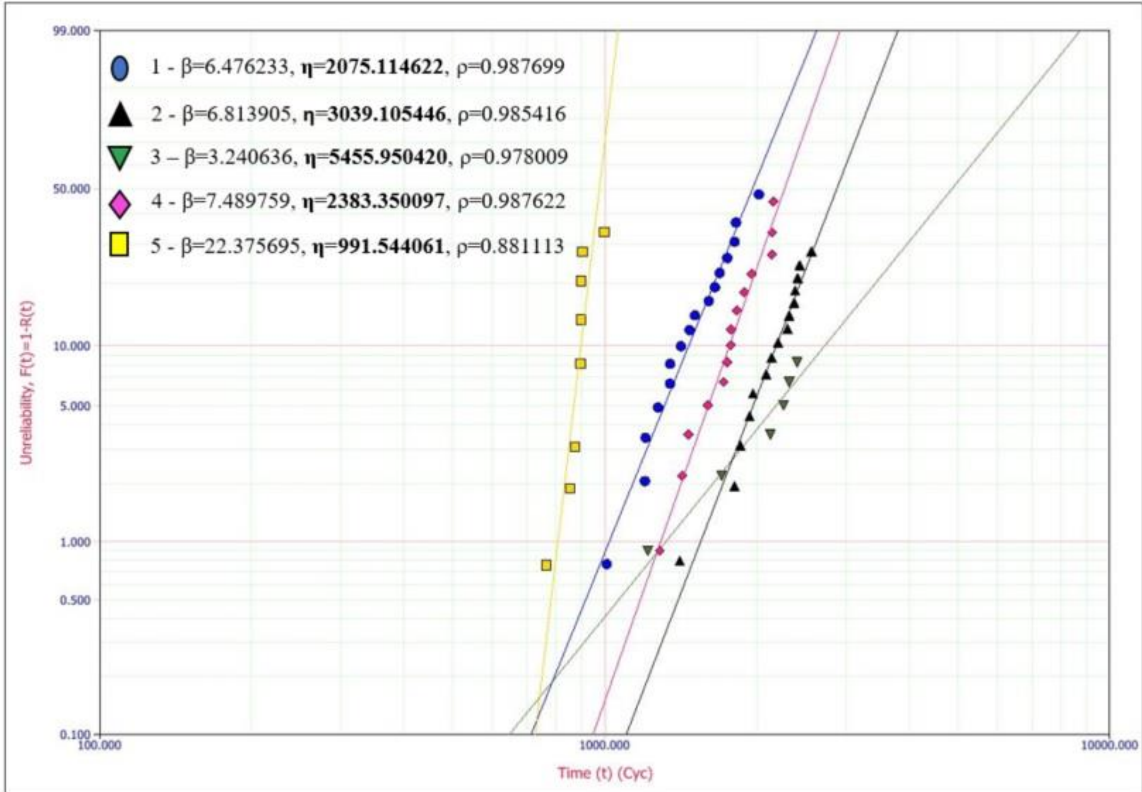


Figure 4.19 Thermal Cycling reliability comparison at no-aging

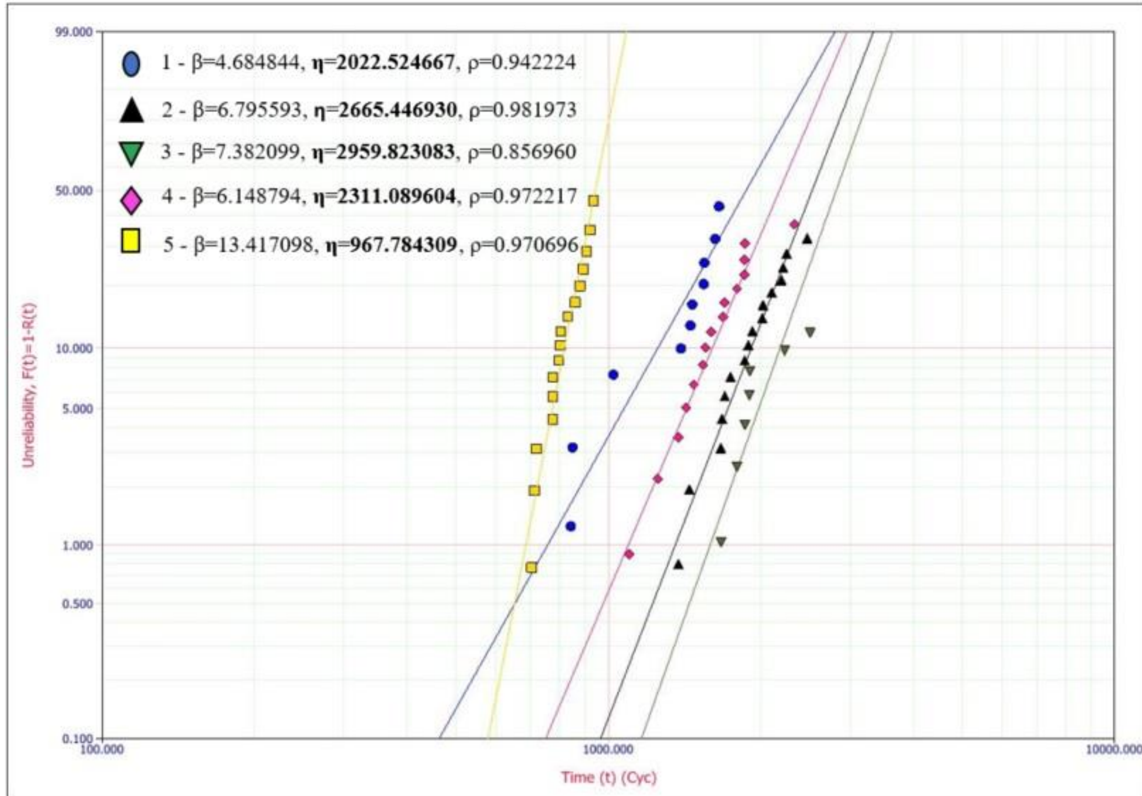


Figure 4.20 Thermal Cycling reliability comparison after 6-months aging

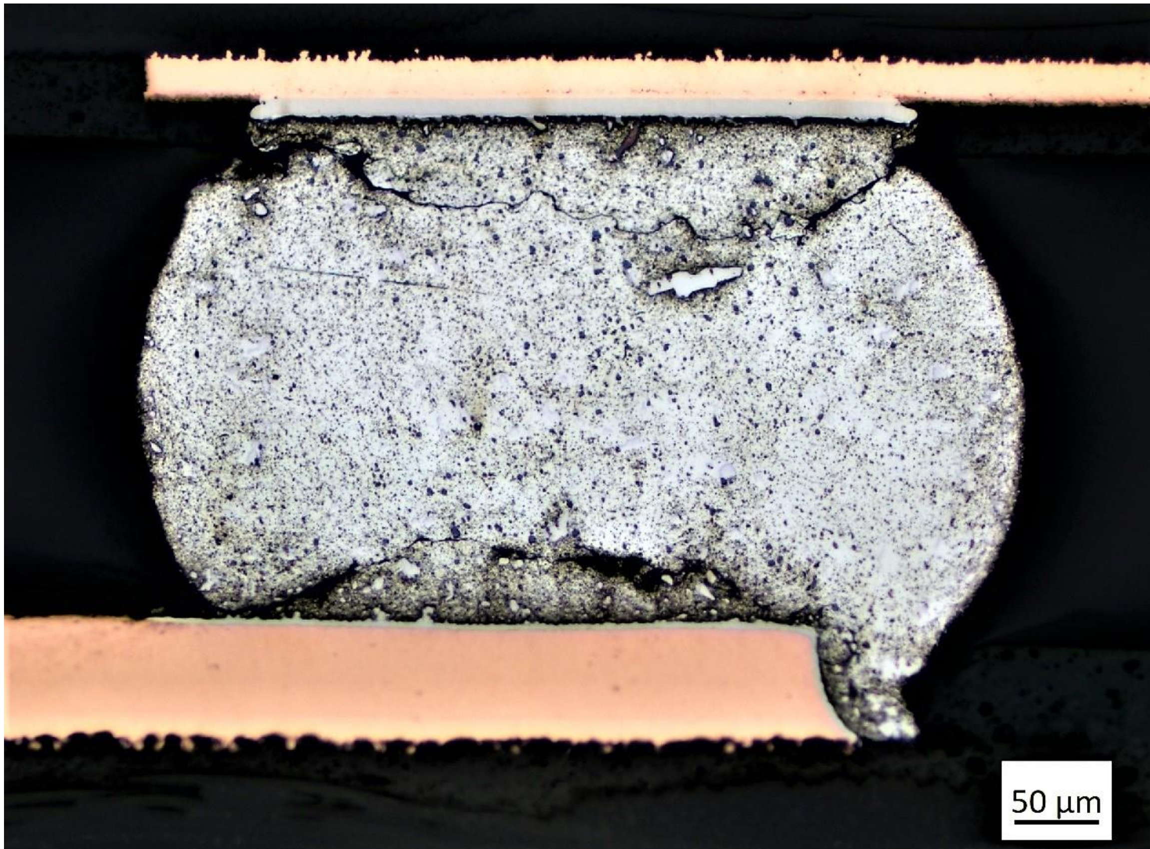
Chapter 5. Failure Analysis

5.1 Cross Sectioning and Failure Analysis

Cross-sectioning is one of the most common methods of destructive failure analysis used in assessing electronic solder joints. These techniques are adapted from typical metallurgical analysis methods. To allow examination of its microstructure, a specimen must first undergo a multi-step sample preparation process [104]. The basic steps in metallurgical sample preparation are 1) Sectioning, 2) Mounting, Grinding, Polishing, Etching (optional, depending on specimen type) [57]. Once a specimen has been prepared for study, it can be examined using optical or electron microscopy.

Cracks in the solder joint results with increase in the electrical resistance, which eventually open circuit in the BGA components. Cracks usually initiate from the regions with the largest stresses (corner areas for BGA package), and then propagate following the stress distribution. During thermal aging and cycling, the solder joint undergoes deformation due to the thermal expansion (CTE) mismatch between the solder joint and the printed circuit board (PCB) and the component, as well as local CTE differences between grains within the solder. Solder microstructural changes include intermetallic compound (IMC) layer growth at PCB/solder joint/package interface or along grain boundaries in the solder bulk and grain coarsening over time

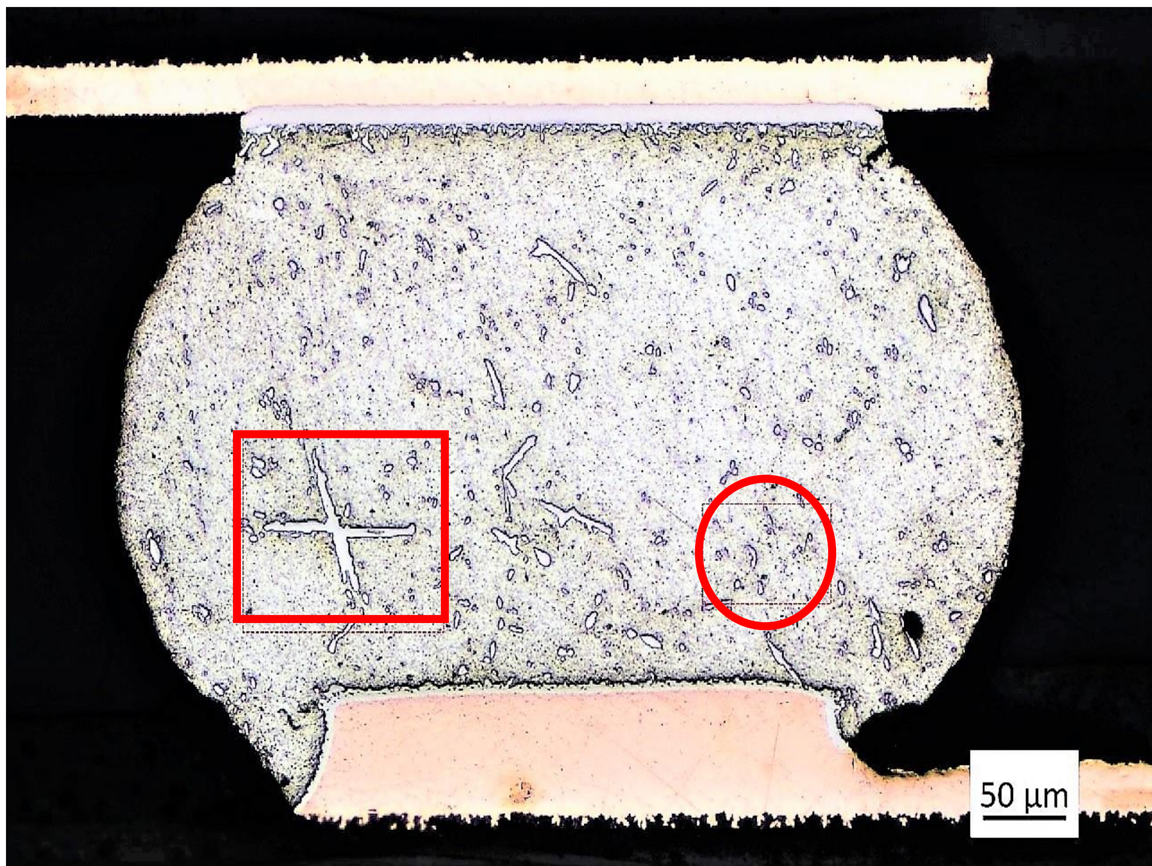
and temperature. During thermal aging and cycling, IMC layer in both the component- and board-side interfaces thicken continuously, consuming material from the copper pads and solder joint. This region is often the principal area in which crack initiation and propagation are observed due to high stress concentration and fatigue. Figure 5.1 shows crack through bulk solder in a BGA



5.1 Microstructure of a BGA Solder Joint

In a typical SAC solder joint with OSP finish, typical IMC layers are $Cu6Sn5$ and $Cu3Sn$ at the Sn/Cu interface and $Ag3Sn$ precipitate in the solder bulk [101]. $Cu3Sn$ exists only at higher Copper contents, therefore is not seen within the bulk of the solder. Initially $Cu6Sn5$ forms adjacent to the copper layer during the reflow process, then during isothermal aging and cycling, $Cu3Sn$ forms by solid-state diffusion between the copper pad and the $Cu6Sn5$ layer. The morphology of $Ag3Sn$ precipitate can be particle-like, needle-like, or plate-like depending on

different cooling rate during reflow process. Volume fraction of the fine $Ag3Sn$ IMC particles in the bulk alloy microstructure of SAC solder alloy increase with increasing of Ag. Figure 5.2 shows the cross-section of the CABGA208 solder joint built using paste material 2 (Innolot). The highlighted rectangular region in the image shows Ag_3Sn precipitates and the highlighted circular region shows Cu_6Sn_5 precipitates from the IMC.



5.2 CABGA208 SAC350 Solder Joint

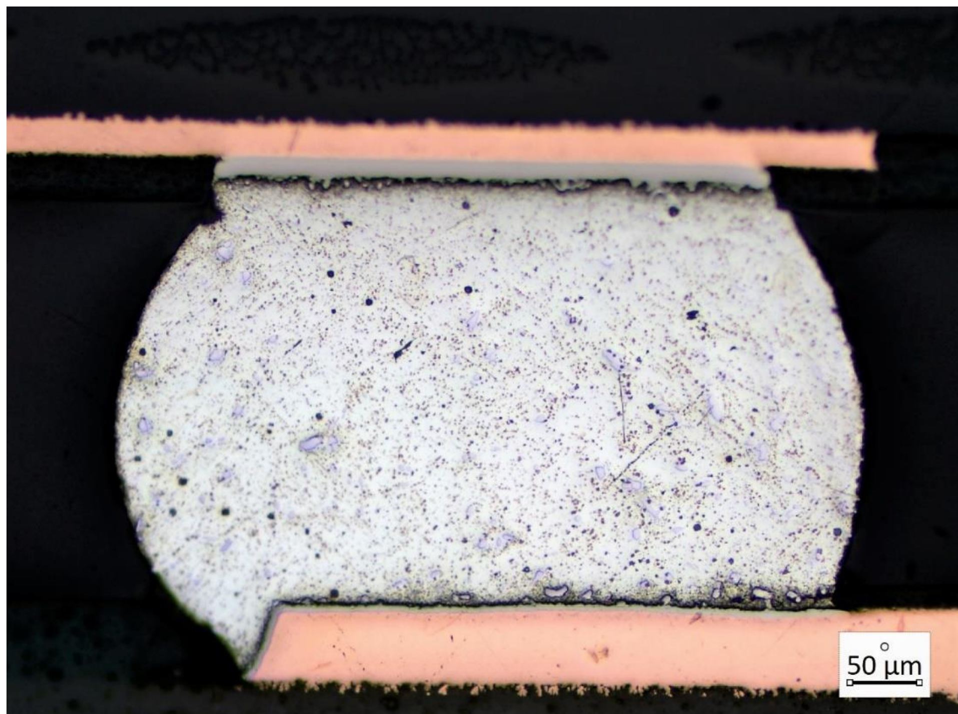
5.3 Failure Modes

This section presents micrographs taken with the Carl Zeiss optical microscope. Micrographs and Polarized Light Microscopy (PLM) of the test samples was used to examine the

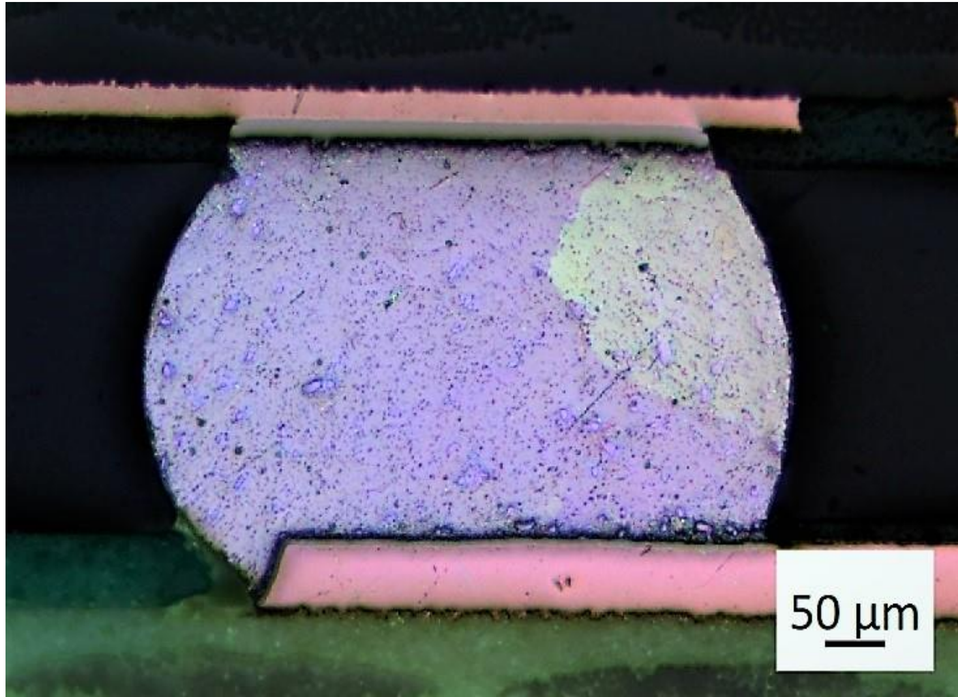
grain orientations changes and understand the failure mechanism in the solder joint after thermal aging and cycling.

5.3.1 Paste Material 1 CABGA208

This micro alloy composition is unknown, large voids were see in the samples built from this paste material. Due to this voiding issue, our analysis is limited. We, observed large multi grain structures and cracks propagating through the bulk solder across the grains. Figures 5.3 and 5.4 show the large multigrain structures.

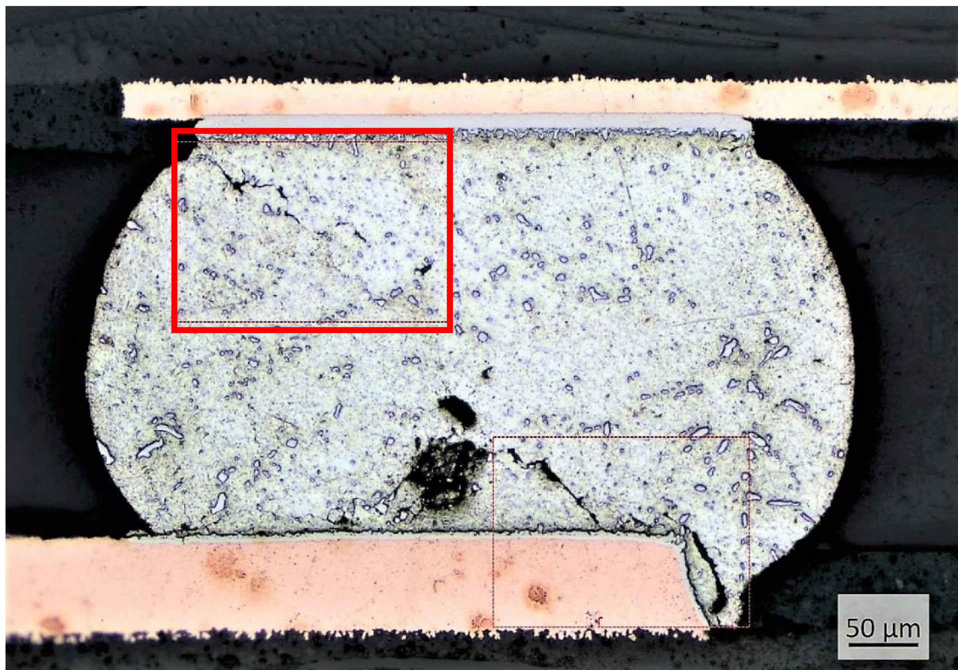


5.3 Paste Material 1 CABGA208



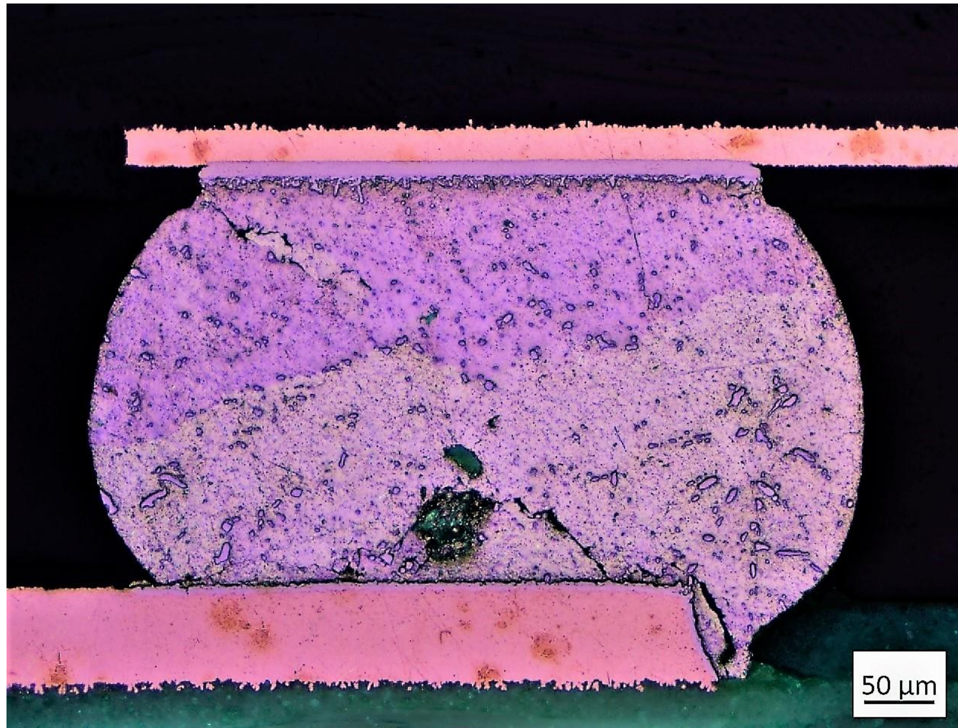
5.4 Paste Material 1 CABGA208 polarized

Figure 5.6 shows the crack propagating through the bulk solder and the highlighted region can be see in the figure 5.7

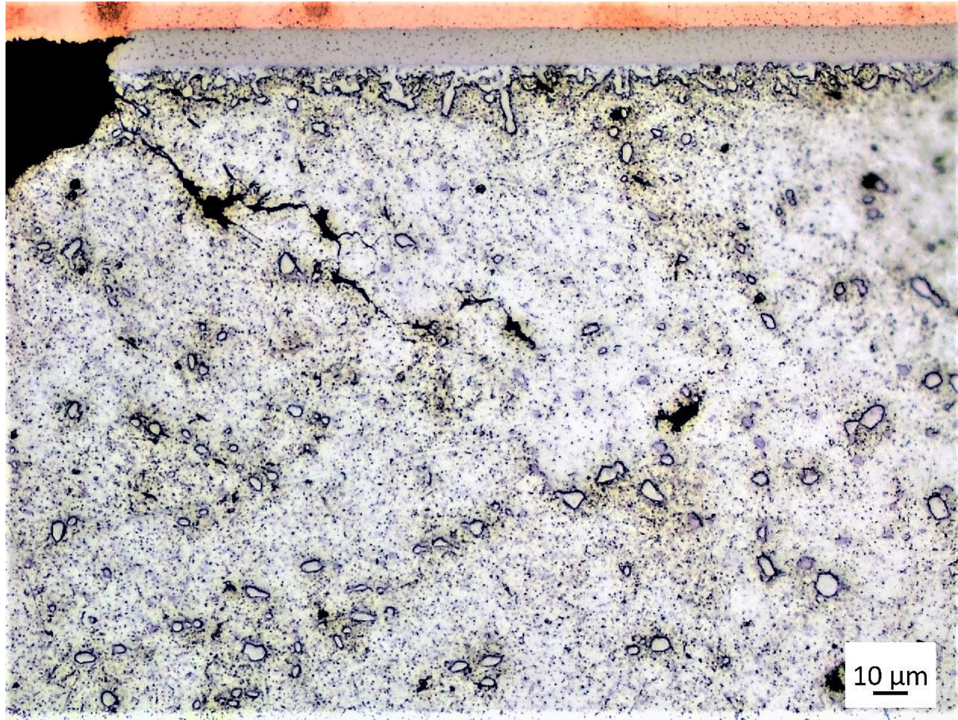


5.5 Paste Material 1 CABGA208

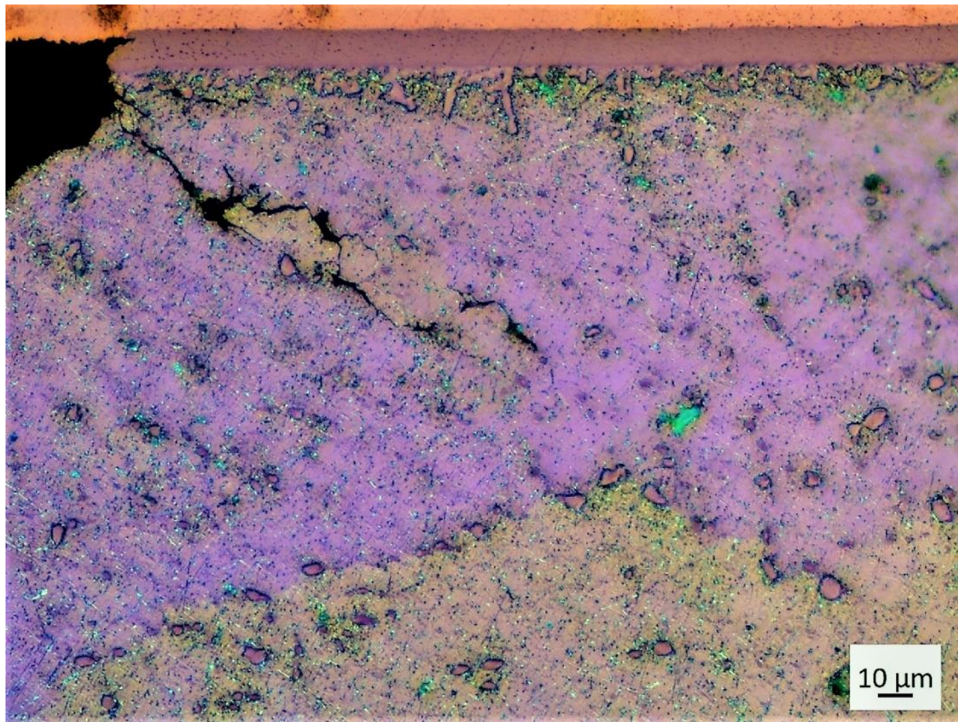
Figure 5.6 Shows the cross polarized image of the cracked solder joint. We can clearly see the 2 large grains and the crack propagating across the grains through the bulk solder. The highlighted section shows the crack propagation, refer Figure 5.8



5.6 Paste Material 1 CABGA208 polarized



5.7 Paste Material 1 CABGA208

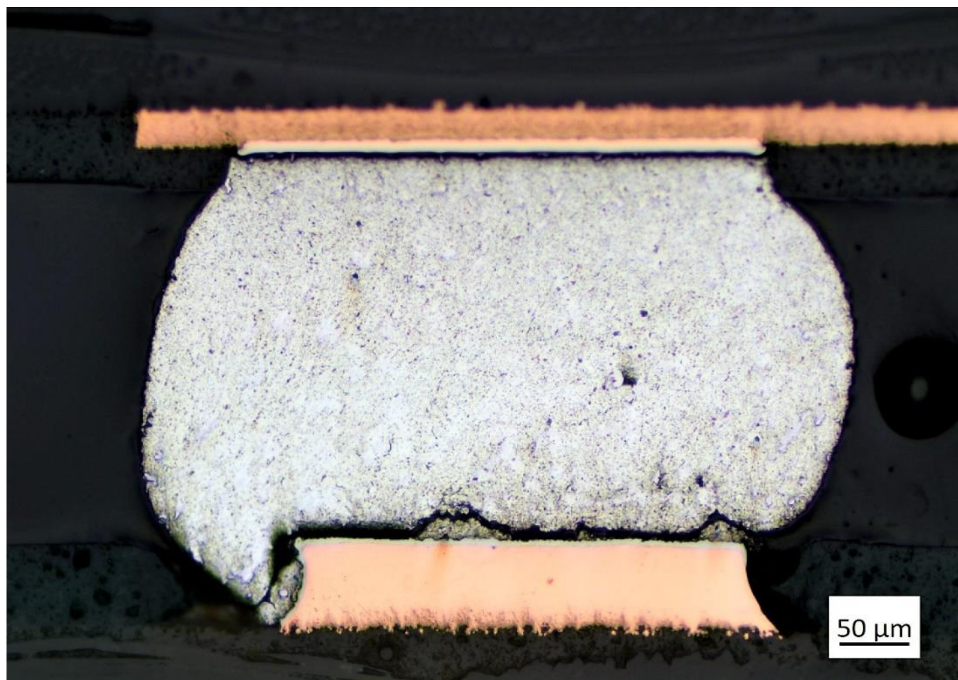


5.8 Paste Material 1 CABGA208 polarized

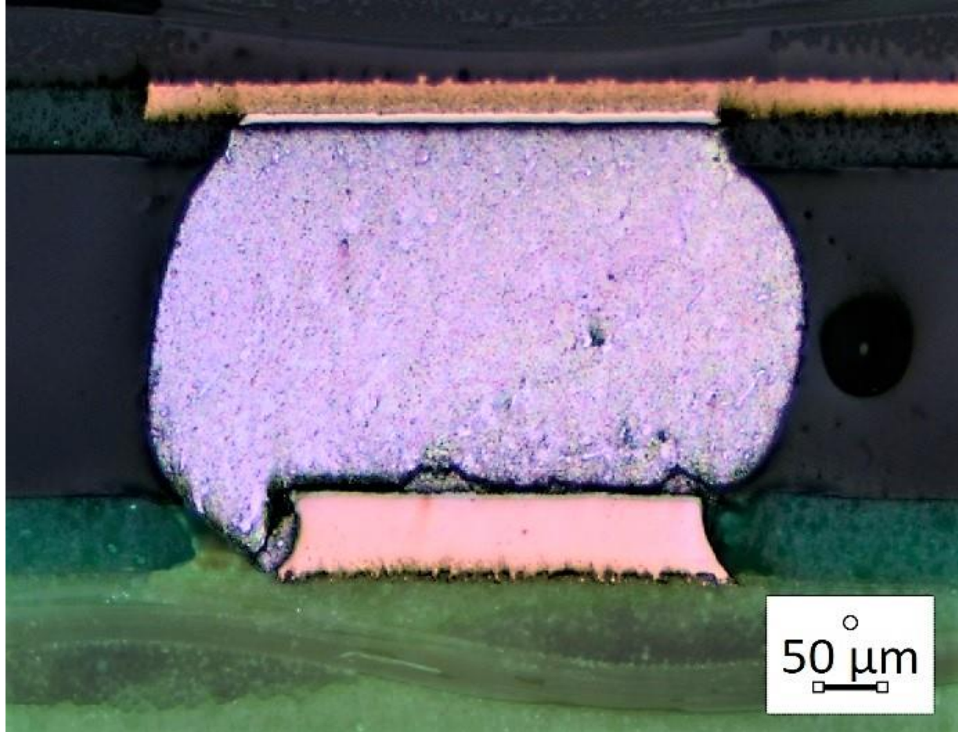
5.3.2 Paste Material 2 (Baseline - Innolot) CABGA208

Paste material 2 is a Bi-doped SAC based alloy with six elements, the composition of which is 90.9Sn-3.8Ag-0.7Cu-3.0Bi-1.4Sb-0.15Ni. This paste material is commercially known as Innolot and often used in automotive industry. This paste material was designed to be used in harsh environments (high temperature and vibration) where the standard SAC alloys could not excel. From previous experiment, we have that paste material 2 experienced much lower degradation in material properties as a function of aging time, hence had an improvement in the reliability. This was the main reason to choose it as the baseline for this testing.

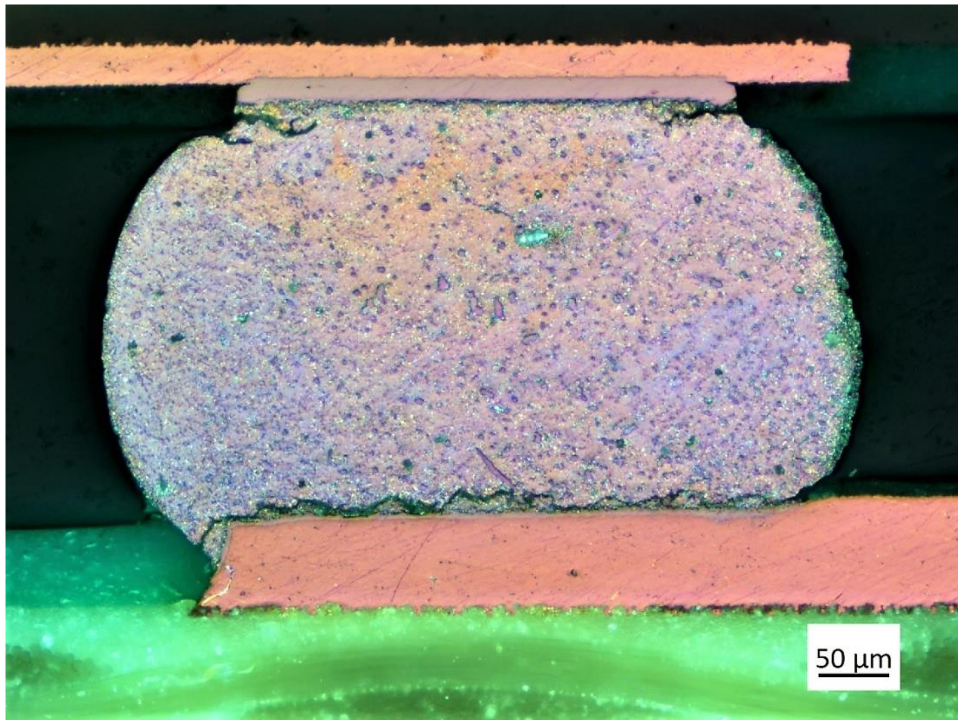
Figures 5.9, 5.10 and 5.11 shows cross section images of a failed solder joint build using paste material 2 (Innolot). There was no solder ball voiding and we observed a majority of single grain in the solder joints. Majority of the failures we observed were through the bulk solder and were brittle fractures on the board side, figures below show the failure trend that was observed.



5.9 Paste Material 2 (Baseline - Innolot) CABGA208



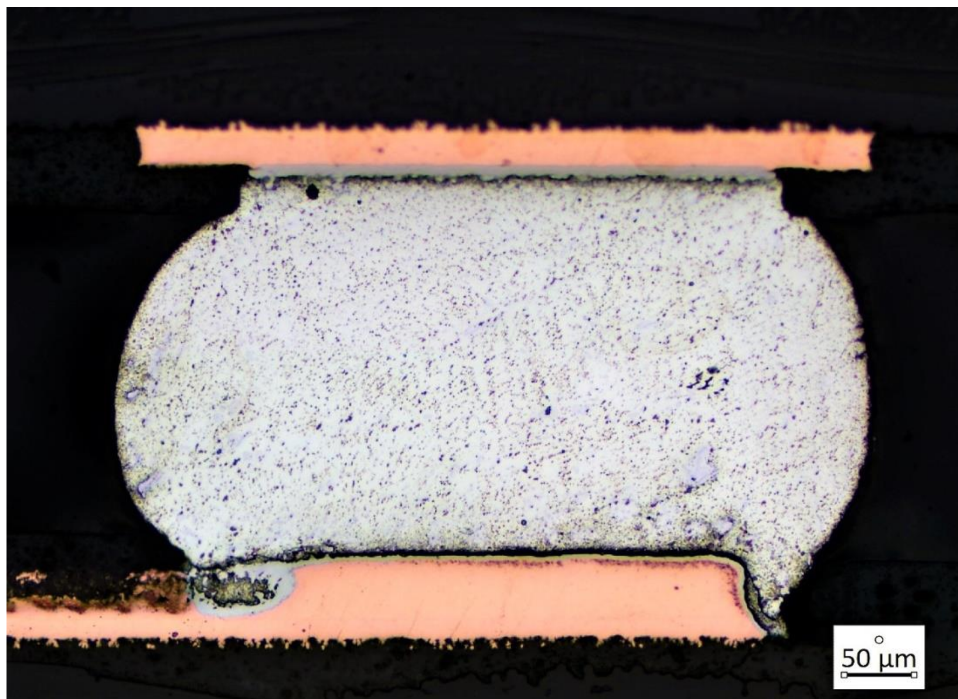
5.10 Paste Material 2 (Baseline - Innolot) CABGA208 polarized



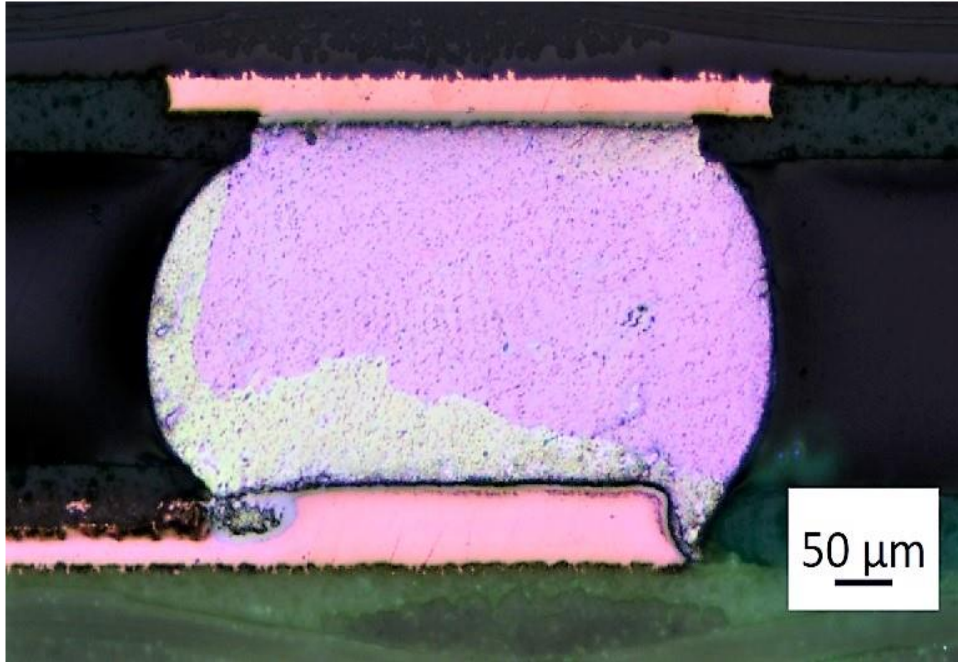
5.11 Paste Material 2 (Baseline - Innolot) CABGA208 polarized

5.3.3 Paste Material 3 CABGA208

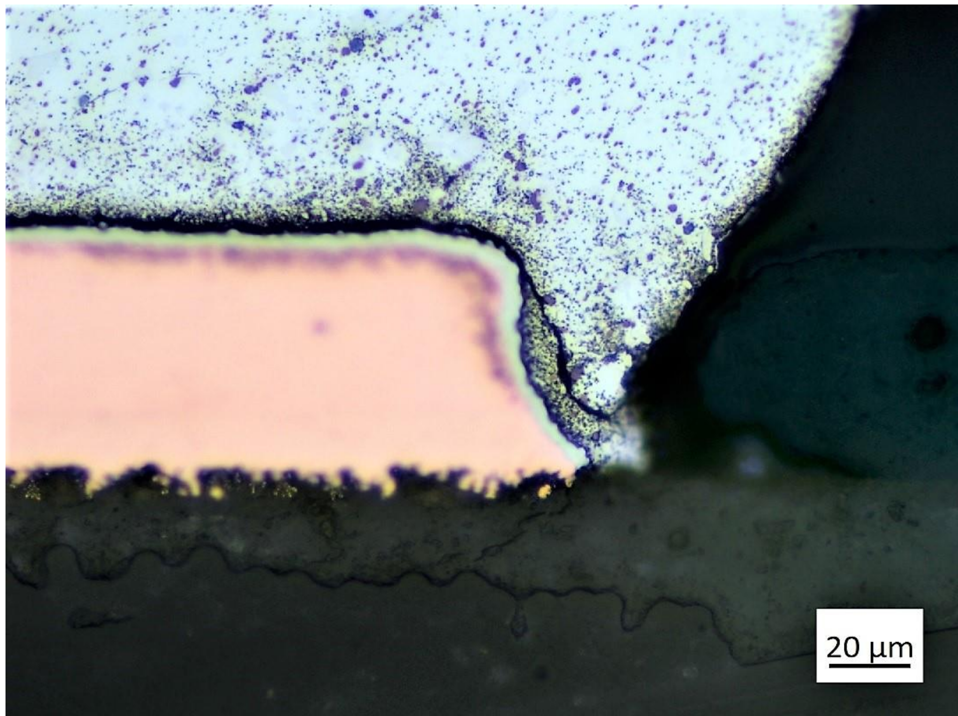
This material is a SAC based microalloy with nickel bismuth and antimony as the dopants. This paste performed well in the Phase 1 liquid shock testing with reliability performance higher than the SAC305 and Innolot paste. In this study, we observed lot of voids in the solder spheres and large grains in the microstructure the same can be seen in the Figures 5.12, 5.13. Figure 5.14 shows the section highlighted form the figure 5.12 where we can see the crack on the board side in the bulk solder. We are unable to get more micrographs due to the voids in the solder spheres.



5.12 Paste Material 3 CABGA208



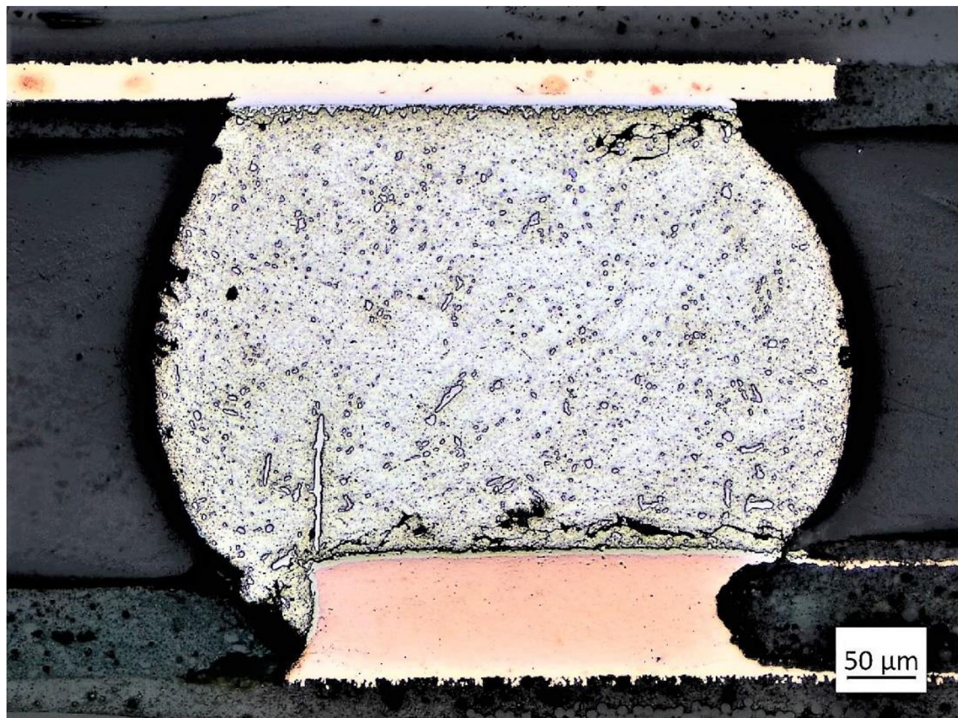
5.13 Paste Material 3 CABGA208 polarized



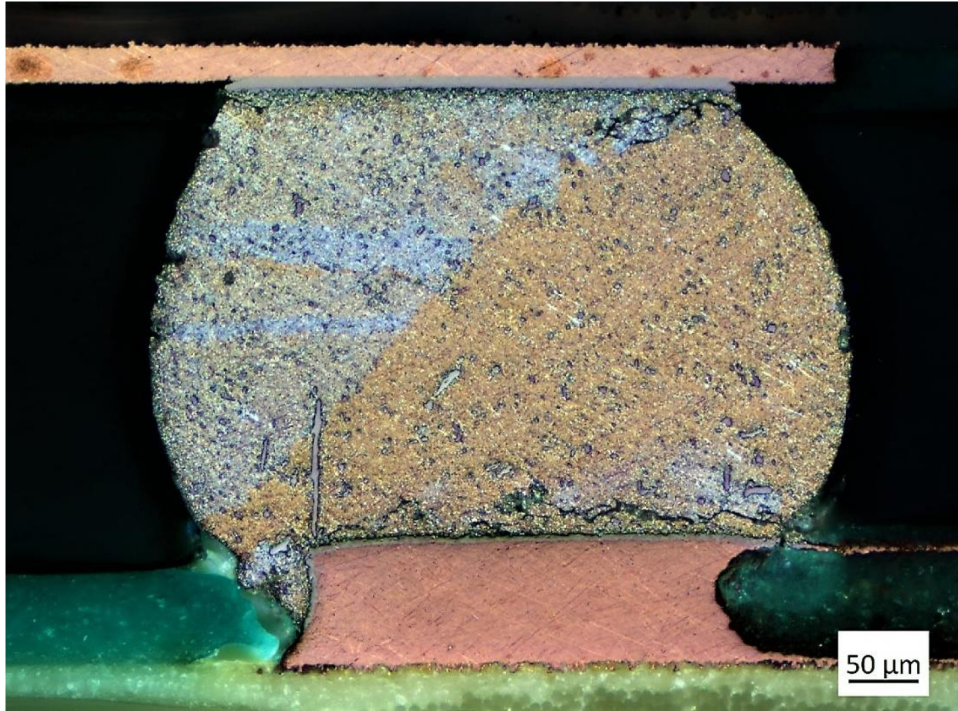
5.14 Paste Material 3 CABGA208

5.3.4 Paste Material 4 CABGA208

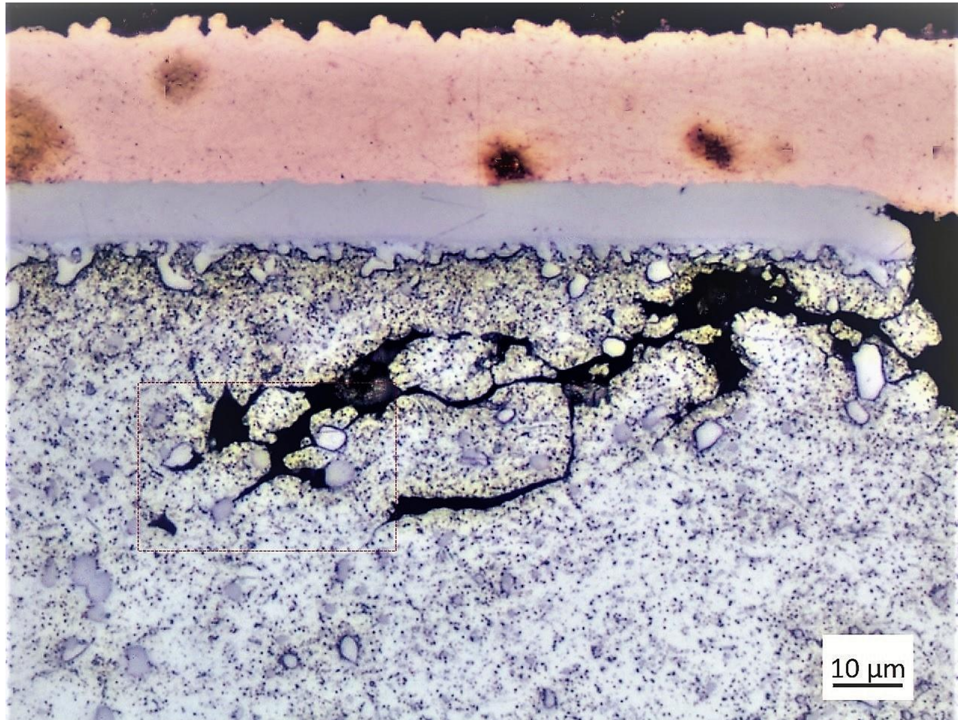
This paste material is a SAC based microalloy with antimony as the dopant. No solder sphere voiding was observed, large grains were observed in the cross sectioned images. We observed the cracks on both board and the component side propagating through the bulk solder and the same can be seen in the figures 5.15 and 5.16. Figures 5.16 and 5.18 shows the crack propagating along the grain boundary. Figures 5.17 and 5.18 shows a magnified view of the highlighted area in Figure 5.15. In these images, we can see the crack initiation and its propagation through the bulk solder. We can also see that the Cu6Sn5 precipitates from the IMC resist the crack from propagation, a similar observation was made in Dr.Zhao's studies



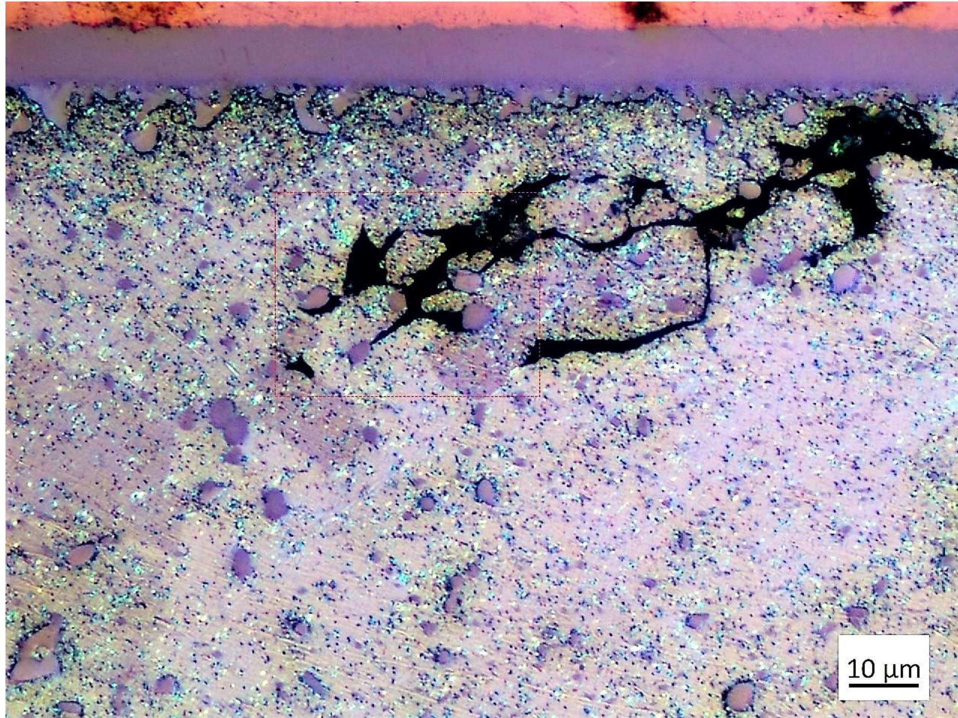
5.15 Paste Material 4 CABGA208



5.16 Paste Material 4 CABGA208 polarized



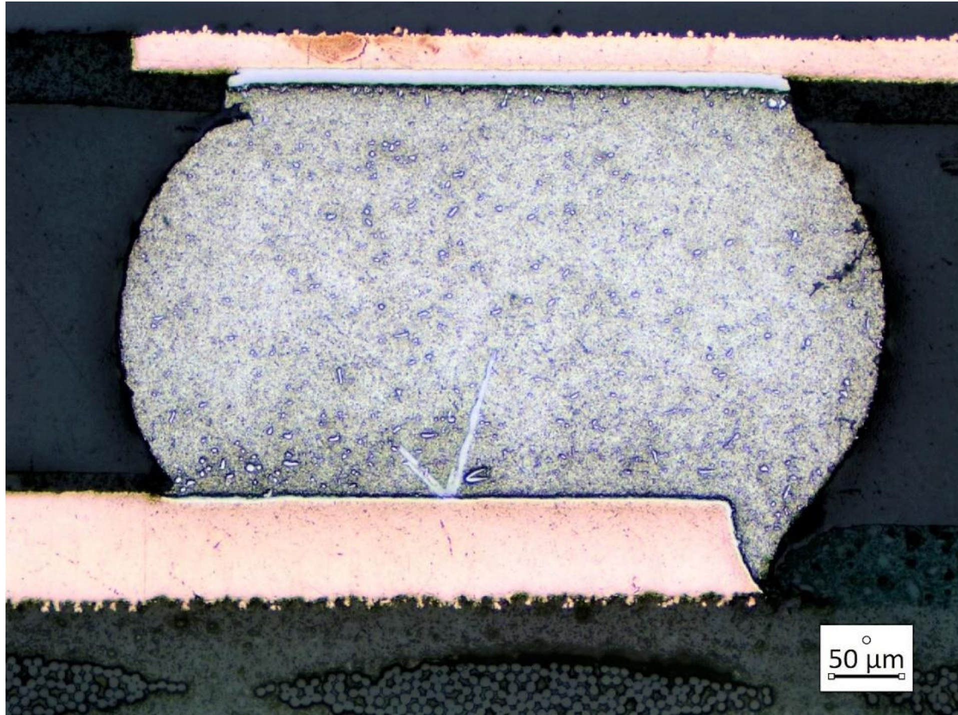
5.17 Paste Material 4 CABGA208



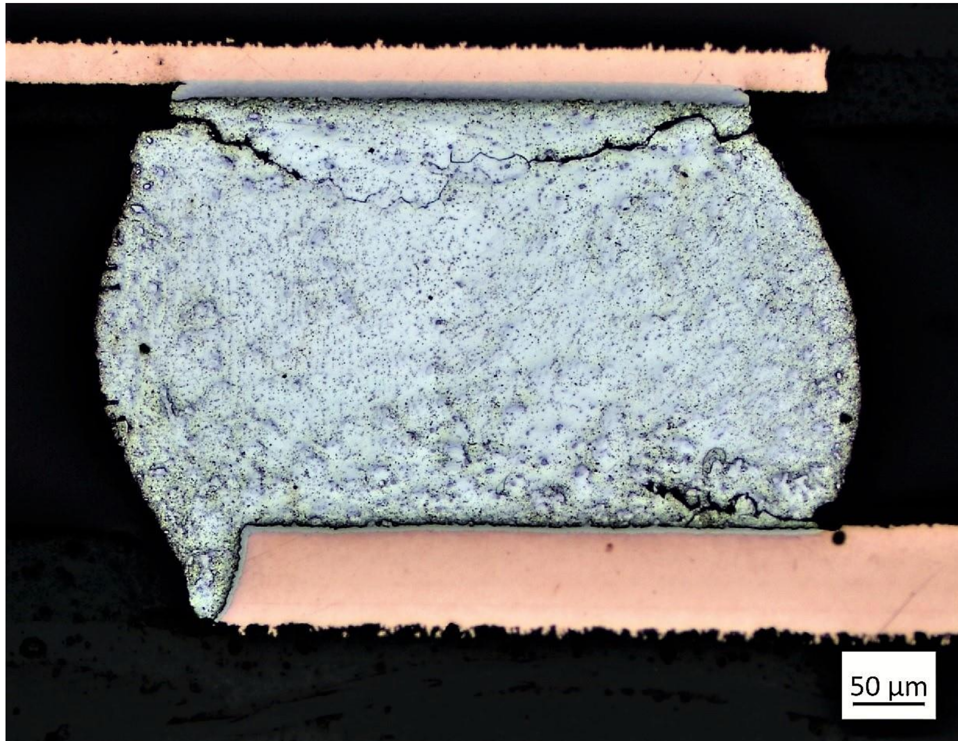
5.18 Paste Material 4 CABGA208 polarized

5.3.5 Paste Material 5 CABGA208

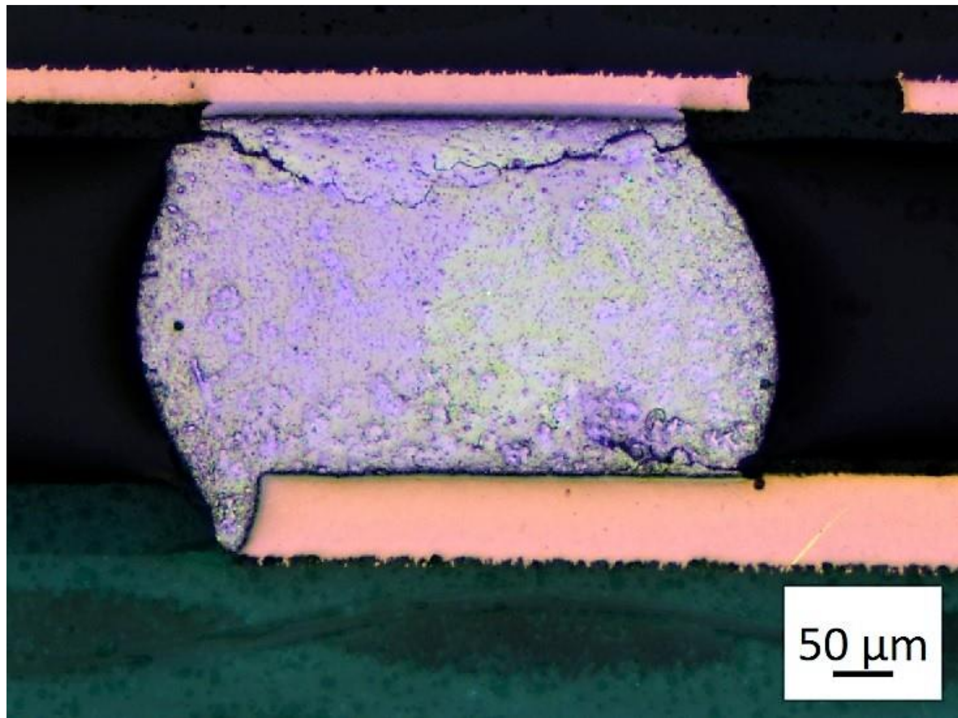
This paste material is a SAC based microalloy with nickel as the dopant. No solder sphere voiding was observed, large multi grains were observed in the cross sectioned images. Figure 5.19 shows the Cu_6Sn_5 IMC precipitates spread across the solder sphere homogenously. We observed the cracks on both board and the component side propagating through the bulk solder and the same can be seen in the figures 5.19 and 5.20.



5.19 Paste Material 5 CABGA208



5.19 Paste Material 5 CABGA208



5.20 Paste Material 5 CABGA208

Chapter 6. Summary and Conclusion

6.1 Phase 1 Summary

Board level drop impact testing is one of the most important modes of evaluating the reliability of assemblies. In this study, we examined the drop impact, vibration and liquid shock performance of no aged and isothermally aged flip chip packages on laminate assemblies for various doped lead-free solder paste alloys. A potential solution to replace the industrial standard solder paste Sn96.5 Ag3.0 Cu0.5 (SAC305) was carried out. The drop and vibration test vehicle consisted of 16 ball grid array packages (BGA) which were 15mm chip array ball grid array's (CABGA208) with perimeter solder balls on 0.8mm pitch. In this experimental study, SnAgCu solder bumps and SAC305 solder paste were selected to be the baseline, Solder pastes with 12 different dopant levels were investigated in comparison with the baseline to determine their reliability. Two sets of printed circuit boards (PCB) were manufactured, the first being no aged and the second set of boards were isothermally aged at 125C for 6 months and then tested. The boards were further categorized into 3 different reflow temperatures and 2 different stencil thicknesses, 4 mil and 6 mil respectively. The results of non-aged and aged samples were categorized and compared using data analytics and Weibull analysis. Failure analysis was carried out to determine best solder paste, solder ball, reflow temperature profile and stencil size. The top 5 solder paste materials from phase 1 project was selected for the phase 2 testing.

6.2 Phase 2 Summary

This study was carried out to investigate the reliability performance of different electronic assemblies during thermal cycling testing. The top 5 performing solder paste material form phase 1 were used. The test boards used were 0.200" thick power computing printed circuit boards with MEGTRON6 as substrate material and OSP coating. Single-sided assemblies were built separately for the Top-side and Bottom-side of the boards. JEDEC JESD22-A104-B test standard was followed, the test boards were subjected to thermal cycling between the temperatures -40^{0}C and +125^{0}C respectively and 120-minute cycle profile with 45-minute transitions and 15-minute dwells at peak temperatures. The test assemblies include surface mount resistors, 5mm, 6mm, 13mm, 15mm, 17mm, 31mm, 35mm and 45mm ball grid array packages respectively. The failure data of 15mm CABGA208 and 17mm CABGA256 are mainly used in this study to understand the effect of solder paste composition on the solder joint reliability during isothermal aging and thermal cycling testing.

6.3 Conclusion

Failure analysis demonstrates that during thermal aging and cycling, the solder joint undergoes deformation due to the thermal expansion (CTE) mismatch between the solder joint and the printed circuit board (PCB) and the component, as well as local CTE differences between grains within the solder. Solder microstructural changes include intermetallic compound (IMC) layer growth at PCB/solder joint/package interface or along grain boundaries in the solder bulk and grain coarsening and recrystallization over time and temperature. For solder pastes that contain high Silver content, large plate-like $Ag3Sn$ bulk IMC can usually be noticed, together with

particle-like $Cu6Sn5$ bulk IMC. There are also particle-like $Ag3Sn$ bulk IMC, with particle size to be much smaller than $Cu6Sn5$ bulk IMC.

- 5 materials outperformed the SAC305 solder material in Phase 1 testing
- The characteristic life of one paste increased after aging and this was observed during drop testing. Grain coarsening resulted in softening the solder joint and consequently shifting the fracture mode from brittle to ductile [117].
- Weibull analysis shows that different solder spheres (SAC105, SAC305, and Matched) and temperature profiles combinations deliver different solder joint reliabilities.
- Weibull analysis also shows that dopants in solder pastes helps mitigate the effect of isothermal aging on the reliability of solder joint. Results from CABGA208, CABGA256 and CVBGA432 clearly shows that paste materials 4 and 5 have superior performance than Innolot.
- Cross sectioned images show that paste material 1 and 3 have voiding defects
- Micrographs of paste material 5 show a good spread of IMC precipitates across the solder sphere
- Cracks through the bulk solder is widely seen in all the solder paste materials. No instance of cracks at IMC layer was observed.
- We also observed the crack propagating through bulk solder stops at the Cu6Sn5 precipitates, and go around it in some cases.
- From the cross polarized images, we saw the cracks propagating along the grain boundaries and across the grain boundaries.
- We also observed brittle failures on the board side in the solder spheres.

From the results of phase 1 and 2 testing conducted at Auburn University, a total of 12 different solder pastes from 8 different solder manufacturing companies were tested. The tests included, mechanical shock, vibration and liquid shock for evaluating the solder paste performance. The top 5 pastes from these tests were chosen for the phase 2 testing that involved thermal cycling. In this paper, the results from the phase 2 of the project have been discussed.

From the above-presented results, the author concludes that the paste material 5 has a characteristic life much higher than the other pastes that were tested. Its reliability performance in thermal cycling has proven to be far superior to the baseline paste material 2 (Innolot) at both no-aged and aged conditions. This Ni-based micro alloy can be a potential replacement for the widely used SAC305 and Innolot paste materials for thermal cycling and liquid shock applications.

6.4 Future work

Since this in an ongoing project, all the results published in phase 2 are form 0-month and 6-month aging group. The phase 2 project ends with 12-month and 24-month testing. Hence the presented results and recommendations are from the data available till 6-months.

In addition to further data which is to be collected for another year, failure analysis needs to be done by the construction of simulation modeling by Finite Element Analysis (FEA). These models would help understanding critical factors of failure mechanism. Dr. Jeff Suhling's research group from Mechanical Engineering Department of Auburn University is currently working on an FEA model. The simulation data and our test data would be a great deal of information to understand the failure mechanism and predictive modelling.

With this information, we will have enough understanding of the failure mechanism and this can be used to find better performing micro alloys for mechanical shock, drop and vibration applications.

Finally, since this project is designed to investigate the effect of dopants added in traditional SAC solder alloy on the reliability of solder joints under thermal aging and cycling, we are proposing another project to test new solder alloys with dopants that can improve reliability for vibration and drop applications. Our goal is to finally find a “magic paste” that delivers good reliability performance for thermal and drop as well as vibration at the same time, with a reasonable cost.

References

[1] Lau, J. H., Wong, C. P., Lee, N. C., and Lee, S. W. R., 2003, Electronics Manufacturing with Lead-Free, Halogen-Free, & Conductive-Adhesive Materials., McGraw-Hill Handbooks.

[2] Dally, J. W., Lall, P., and Suhling, J. C., 2008, Mechanical Design of Electronic Systems.

[3] IPC, 2007, From Vacuum Tubes to Nanotubes: An Amazing Half Century. The Emergence of Electronic Circuit Technology 1957-2007., IPC - Association Connecting Electronics Industries.

[4] Intel (1996). Packaging. Mcgraw-hill Inc. ISBN 1-55512-254-X.

[5] Prasad, R., 1997, Surface mount technology: principles and practice., Springer Science & Business Media.

[6] Vijayakumar, N. P., 2012, "The Effects of Thermal Aging on the Mechanical Behavior of Fine Pitch Electronics Packages," Auburn University.

[7] Bonnie C. Baker, "Smaller Packages = Bigger Thermal Challenges", Microchip Technology Inc.

[8] Ken Gilleo (2003). Area array packaging processes for BGA, Flip Chip, and CSP. McGraw Hill Professional. p. 251. ISBN 0-07-142829-1

[9] Evans, J. L., 2013, "Lectures given at Auburn University."

[10] A. R. Djordjevic, R. M. Biljic, V. D. Likar-Smiljanic and T. K. Sarkar, "Wideband Frequency Domain Characterization of FR-4 and Time-Domain Causality", IEEE TRANSACTIONS ON ELECTROMAGNETIC COMPATIBILITY, VOL. 43, NO. 4, NOVEMBER 2001

[11] Harper, C. A., 2002, Electronic Assembly Fabrication: Chips, Circuit Boards, Packages, and Components, McGraw-Hill.

[12] C. Coombs, H. Holden, “Printed Circuits Handbook”, 2003

[13] IPC, 2007, From Vacuum Tubes to Nanotubes: An Amazing Half Century. The Emergence of Electronic Circuit Technology 1957-2007., IPC - Association Connecting Electronics Industries

[14] I. Szendiuch, "Development in Electronic Packaging – Moving to 3D System Configuration," Radio engineering 20, vol. no 1, pp. 214-220, 2011

[15] A. G. W. A. F. B. Elshabini, "Future trends in electronic packaging," Smart structures and materials, pp. 61720Z-61720Z, 2006

[16] R. ASCHENBRENNER, "Greetings from IEEE/CPMT," in 30th International Spring Seminar on Electronics Technology ISSE, Cluj Napoca (Romania), 2007

[17] S. K. Yoshihiro Nakamura, "Technology trends and future history of semiconductor packaging substrate material," Hitachi Chemical Technical Report No. 55, 2013

[18] K.-J. W. Gerald Gerlatch, Bio and Nano Packaging Techniques for Electron Devices, London: Springer, 2012.

[19] Gilleo, B. K., 1994, “The First 7 , 000 Years of Soldering , Part I,” (October)

[20] Hunt, and LePrevost, “Getting the Lead Out - Soldering with Lead-free Solders.pdf,” Proceedings of the RCI 22nd International Convention.

[21] Nakamura, Y., Sakakibara, Y., Watanabe, Y., and Amamoto, Y., 1998, “Microstructure of solder joints with electronic components in lead-free solders,” Solder. Surf. Mt. Technol., **10**(1), pp. 10–12.

[22] Matin, M. A., 2005, “Microstructure evolution and thermomechanical fatigue of solder materials,” Technische Universiteit Eindhoven

[23] Ii, P., and Gilleo, B. K., 1994, “The First 7 , 000,” (November), pp. 44–45.

[24] Zhang, J., 2012, “The Effects of Aging on the Reliability of Lead Free Fine-Pitch 215 Electronics Packaging,” Auburn University

[25] Turbini, L. J., Munie, G. C., Bernier, D., Gamalski, J., and Bergman, D. W., 2001, “Examining the environmental impact of lead-free soldering alternatives,” IEEE Trans. Electronic. Package. Manuf., **24**(1), pp. 4–9.

[26] Bozack, M. J., 2014, “Lectures given at Auburn University.”

[27] World Health Organization, 2005, Childhood lead poisoning prevention.

[28] Hwang, J. S., 2004, Implementing lead-free electronics., McGraw-Hill.

[29] Ma, H., and Suhling, J. C., 2009, “A review of mechanical properties of lead-free solders for electronic packaging,” J. Mater. Sci., **44**(5), pp. 1141–1158.

[30] Henderson, D. W., Woods, J. J., Gosselin, T. a., Bartelo, J., King, D. E., Korhonen, T. M., Korhonen, M. a., Lehman, L. P., Cotts, E. J., Kang, S. K., Lauro, P., Shih, D.-Y., Goldsmith, C., and Puttlitz, K. J., 2004, “The microstructure of Sn in near-eutectic Sn–Ag–Cu alloy solder joints and its role in thermomechanical fatigue,” J. Mater. Res., **19**(06), pp. 1608–1612.

[31] S. F. Al-sarawi, D. Abbott, and P. D. Franzon, “A Review of 3-D Packaging Technology”, IEEE TRANSACTIONS ON COMPONENTS, PACKAGING, AND MANUFACTURING TECHNOLOGY—PART B, VOL. 21, NO. 1, FEBRUARY 1998.

[32] Girouard, Roland. "Mark5 Reflow Oven". Heller Industries Website. Heller Industries Inc.

[33] E. Kamen, A. Goldstein, O. Asarangchai, A. Fraser, K. Klatka, J. Belmonte, R. Huber, “Analysis of Factors that Affect Yield in SMT Assembly”.

[34] Institute of Electrical and Electronics Engineers (1990) IEEE Standard Computer Dictionary: A Compilation of IEEE Standard Computer Glossaries. New York, NY ISBN 1-55937-079-3

[35] J. Zhang, Z. Hai, S. Thirugnanasambandam, J.L. Evans, M. J. Bozack, "Correlation of Aging Effects on Creep Rate and Reliability in Lead Free Solder Joints", Journal of Surface Mount Technology, (2012), Vol. 25 (3), pp. 19-28 Orlando, FL.

[36] Azira N.M.M, N.M Mohd Nan, M.A Idris and M.Z Bukhari, "Board Level Reliability (BLR) - board design, test, and application", ICRAMME 2005, Malaysia

[37] M.A. Matin, W.P. Vellinga, M.G.D. Geers. "Thermomechanical fatigue damage evolution in SAC solder joints," Materials Science and Engineering A 445–446 (2007), pp. 73–85

[38] C. Shen, C. Zhao, Z. Hai, J. Zhang, M. J. Bozack, J. C. Suhling, and J.L. Evans, "Sn-Ag-Cu Solder Joints Interconnection Reliability of BGA Package during Thermal Aging and Cycling", Proceedings of the 48th IMAPS, October 2015

[39] Zhang, J., Hai, Z., Thirugnanasambandam, S., and Evans, J. L., 2009, "Isothermal Aging Effects on the Dynamic Performance of Lead-Free Solder Joints," pp. 390–397.

[40] Zhou Hai, Jiawei Zhang, Chaobo Shen, John. L. Evans and M. J. Bozack, "Long-term Aging Effects on Reliability Performance of Lead-Free Solder Joints", SMTA International 2013, 2013

[41] Munshi Basit, Mohammad Motalab, Jeffrey C Suhling, John L Evans, Pradeep Lall, "FEA Based Reliability Predictions for PBGA Packages Subjected to Isothermal Aging Prior to Thermal Cycling", 2015 InterPACK, 2015

[42] Parker, R., Coyle, R., Henshall, G., Smetana, J., and Benedetto, E., iNEMI Pb-FREE ALLOY CHARACTERIZATION PROJECT REPORT : PART II - THERMAL FATIGUE RESULTS FOR TWO COMMON TEMPERATURE CYCLES Hewlett-Packard Co ., Palo Alto , CA , USA.

[43] Kang, S. K., Lauro, P., and Shih, D.-Y., 2004, "Evaluation of thermal fatigue life and failure mechanisms of Sn-Ag-Cu solder joints with reduced Ag contents," 2004 Electronic Components and Technology Conference, pp. 661–667.

[44] Suhling, J. C., 2015, “Lectures given at Auburn University.”

[45] Lau, J. H., 2011, Reliability of RoHS Compliant 2D and 3D IC Interconnects., McGraw-Hill.

[46] Vijayakumar, N. P., 2012, “The Effects of Thermal Aging on the Mechanical Behavior of Fine Pitch Electronics Packages,” Auburn University.

[47] Pirondi, A., 1997, “Mechanical Failure in Microelectronic Packaging,” Convegno IGF 13.

[48] Frear, D. R., Jang, J. W., Lin, J. K., and Zhang, C., 2001, “Pb-free solders for flip-chip interconnects,” Jom, **53**(6), pp. 28–33.

[49] Chen, H., Mueller, M., Mattila, T. T., Li, J., Liu, X., Wolter, K.-J., and Paulasto-Krockel, M., 2011, “Localized recrystallization and cracking behavior of lead-free solder interconnections under thermal cycling,” J. Mater. Res., **26**(16), pp. 2103–2116

[50] Hertzberg, R. W., Vinci, R. P., and Hertzberg, J. L., 2012, Deformation and Fracture Mechanics of Engineering Materials, Wiley.

[51] Aaron Olson, “What are Intermetallics and How Can We Overcome the Failures Associated with Them”, STI Electronics

[52] Eric Basstow, “Intermetallics In Soldering”, Indium Corporation, 11/11/2011

[53] Bansal, Anurag, Lee, Tae-Kyu, Liu, Kuo-Chuan, Xue, Jie, Effects of Isothermal Aging and In-Situ Current Stress on the Reliability of Lead-Free Solder Joints, Electronic Components and Technology Conference, 2010

[54] Lampe, B. T., "Room Temperature Aging Properties of Some Solder Alloys," Welding Journal, Vol. 55, pp. 330s-340s, 1976

[55] Medvedev, A. S., "Aging of Tin-Lead Solders and Joints Soldered by Them, "MetallovedenieiObrabotkaMetallov, No.7, pp. 16-23, 1956

[56] Chung, C. K., Aspandiar, R., Leong, K. F., and Siew, T. C., "The Interactions of Lead(Pb) in Lead-Free Solder (Sn/Ag/Cu) System," Proceedings of the 52nd Electronic Components and Technology Conference, pp. 168-175, 2002.

[57] Hunt, C., Nottay, J., Brewin, A., and Dinsdale, A., "Predicting Microstructure of Mixed Solder Alloy System," NPL Report, 2002.

[58] Bath, J., Hu, L., and Chiang, D., "Reliability Evaluation Of Lead-Free Snagcu Pbga676Components Using Tin-Lead And Lead-Free Snagcu Solder Paste," SMTA International Conference Proceedings, pp. 891-901, 2005.

[59] Clech, J. P., "Lead-Free and Mixed Assembly Solder Joint Reliability Trends, "Proceedings of APEX, Paper S28-3, pp. 1-14, 2004.

[60] Fouassier, O., Heintz, J. M., Chazelas, J., Geffroy, P. M., and Silvain, J. F.,"Microstructural Evolution and Mechanical Properties of SnAgCu Alloys," Journal Of Applied Physics, Vol. 100, Paper 043519, pp. 1-8, 2006.

[61] Jones, W. K., Liu, Y., Zampino, M. A., Gonzalez, G., and Shah, M., "A Study on Mechanical Properties of Eutectic and Solid Solution Pb-Sn-Ag Solders from 200 °C to 150 °C " Design and Reliability of Solders and Solder Interconnections, pp. 85-96, 1997.

[62] Pang, J. H. L., Xiong, B. S., Neo, C. C., Mang, X. R., and Low, T. H., "Bulk Solder and Solder Joint Properties for Lead-Free 95.5Sn-3.8Ag-0.7Cu Solder Alloy," Proceedings of the 53rd Electronic Components and Technology Conference, pp. 673-679, 2003.

[63] Qiang, X., Luu, N., and Armstrong, W. D., "Aging and Creep Behavior of Sn3.9Ag0.6Cu Solder Alloy," Proceedings of the 54th Electronic Components and Technology Conference, pp. 1325-1332, 2004.

[64] Qiang, X., Harold, J. B., and Armstrong, W. D., "Aging Effects on Microstructure and Tensile Property of Sn3.9Ag0.6Cu Solder Alloy," Journal of Electronic Packaging, Vol. 126, pp. 208-212, 2004.

[65] Vianco, P., and Rejent, J., "The Compression Stress-Strain Behavior of Sn-Ag-Cu Solder," JOM Journal of the Minerals, Metals and Materials Society, Vol. 55, pp. 50-55,2003.

[66] Mysore, K., Chan, D., Bhate, D., Subbarayan, G., Dutta, I., Gupta, V., Zhao, J. and Edwards, D., "Aging-Informed Behavior of Sn3.8ag0.7cu Solder Alloys," Proceedings of the 11th Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems, pp. 870-875, 2008.

[67] Darveaux, Robert, Heckman, Jim, Syed, Ahmer, Mawer, Andrew, Solder joint fatigue life of fine pitch BGAs- impact of design and material choices, Microelectronics Reliability 40, 2000.

[68] Chiu, T. C., Kejun, Z., Stierman, R., Edwards, D., and Ano, K., "Effect of Thermal Aging on Board Level Drop Reliability for Pb-Free BGA Packages," Proceedings of the 54th Electronic Components and Technology Conference, pp. 1256-1262, 2004.

[69] Hasegawa, K., Noudou, T., Takahashi, A., and Nakaso, A., Thermal Aging Reliability of Solder Ball Joint for Semiconductor Package Substrate, Proceedings of the 2001 SMTA International, pp. 1-8, 2001.

[70] Li, M., Lee, K. Y., Olsen, D. R., Chen, W. T., Tan, B. T. C., and Mhaisalkar, S., Microstructure, Joint Strength and Failure Mechanisms of SnPb and Pb-Free Solders in BGA Packages, IEEE Transactions on Electronics Packaging, Vol. 25(3), pp. 185-192, 2002.

[71] Law, C. M. T., and Wu, C. M. L., Microstructure Evolution and Shear Strength of Sn-3.5Ag-RE Lead Free BGA Solder Balls, Proceedings of HDP‘04, pp. 60-65, 2004.

[72] Ma, H., Suhling, J. C., Zhang, Y., Lall, P., and Bozack, M. J. "The Influence of Elevated Temperature Aging on Reliability of Lead Free Solder Joints," Proceedings of the 57th Electronic Components and Technology Conference, pp. 653-668, 2007

[73] Lau, John, et al., Reliability Testing and Data Analysis Of High-Density pakcages' Lead-Free Solder Joints, IPC SMEMA Council APEX, 2003

[74] Pan, Jianbiao, Wang, Jyhwen, Shaddock, David M, Lead-Free Solder Joint Reliability-State of the Art and Perspectives, Proceedings of the 37th International Symposium on Micro-electronics, Long Beach, CA, 2004.

[75] Joe Smetana, et al., Pb-free Solder Joint Reliability in a Mildly Accelerated Test Condition, IPC SMEMA Council APEX, 2011

[76] Hertzberg, R. W., Deformation and Fracture Mechanics of Engineering Materials, 4 Ed., John Wiley & Sons, Inc., 1996

[77] Pang, J.H.L., Kwang Hong Tan, Xunqing Shi. And Z.P. Wang, "Thermal Cycling Aging effects on Microstructural and Mechanical Properties of a single PBGA Solder Joint Specimen" IEEE Transactions on Components and Packaging Technologies, Vol.24, No.1, March 2001.

[78] Lim, C. T., Ang, C. W., Tan, L. B., Seah, S. K. W., Wong, E.H., "Drop Impact survey of Electronic Products", Proceedings of the 53rd Electronic Components and Technology Conference, pp. 113-120, 2003.

[79] Wu, J., Song, G., Yeh, C., Wyatt, K., "Drop/Impact Simulation and Test Validation of Telecommunication Products", Proceedings of the InterSociety Conference on Thermal Phenomena, pp. 330-336, 1998.

[80] Xie, D., Arra, M., Yi, S., Rooney, D., “Solder Joint Behavior of Area Array Packages in Board Level Drop for Handheld Devices”, Proceedings of the 53rd Electronic Components and Technology Conference, pp. 130-135, 2003.

[81] Lall, P., Panchagade, D., Choudhary, P., Suhling, J., Gupte, S., “Failure- Envelope Approach to Modeling Shock and Vibration Survivability of Electronic and MEMS Packaging”, Proceedings of the 55th Electronic Components and Technology Conference, pp. 522-529, 2005.

[82] Lall, P., Panchagade, D., Liu, Y., Johnson, W., Suhling, J., “Models for Reliability Prediction of Fine-Pitch BGAs and CSPs in Shock and Drop Impact”, Proceedings of the 54thElectronic Components and Technology Conference, pp.1296-1303, 2004.

[83] L. Zhu and W. Marcinkiewicz, “Drop Impact Reliability Analysis of CSP Packages at Board and Product Levels Through Modeling Approaches,” IEEE Transactions on Components and Packaging Technologies, vol. 28, no. 3, pp. 449-456, 2005.

[84] T. Chiu, K. Zeng, R. Stierman, D. Edwards, and K. Ano, “Effect of Thermal Aging on Board Level Drop Reliability for Pb-free BGA Packages,” in Proc. 2004Electronic Components and Technology Conference, pp. 1256-1262, 2004.

[85] C. Yeh, Y. Lai, and C. Ka, “Evaluation of board-level reliability of electronic packages under consecutive drops,” Microelectronics Reliability, vol. 46, no. 7, pp.1172-1182, 2006.

[86] Y. Lai, P. Yang, and C. Yeh, “Experimental Studies of Board-Level Reliability of Chip-Scale Packages Subjected to JEDEC Drop Test Condition,” Microelectronics Reliability, vol. 46, no. 7, pp. 645-650, 2006.

[87] P. Nemeth, “Accelerated Life Time Test Methods for New Package Technologies”, Electronics Technology: Concurrent Engineering in Electronic Packaging, 2001, pp. 215-219

[88] Coyle, R. J., Sweatman, K., and Arfaei, B., 2015, “Thermal Fatigue Evaluation of Pb-Free Solder Joints: Results, Lessons Learned, and Future Trends,” J. Mater., **67**(10), pp. 2394–2415.

[89] Kim, D.-H., Elenius, P., and Barrett, S., 2002, “Solder Joint Reliability and Characteristics of Deformation and Crack Growth of Sn – Ag – Cu Versus Eutectic Sn – Pb on a WLP in a Thermal Cycling Test,” IEEE Trans. Electron. Packag. Manuf., **25**(2), pp. 84–90.

[90] Hokka, J., Mattila, T. T., Xu, H., and Paulasto-Kröckel, M., 2013, “Thermal cycling reliability of Sn-Ag-Cu solder interconnections. part 1: Effects of test parameters,” J. Electron. Mater., 42(6), pp. 1171–1183.

[91] Wilcox, J., Coyle, R., Lehman, L., Smetana, J., and Hill, M., 2014, “EFFECT OF 219

[92] Chiu, T.-C., Keng, K., Stierman, R., Edwards, D., and Ano, K., “Effect of thermal aging on board level drop reliability for Pb-free BGA packages,” 2004 Proceedings. 54th Electronic Components and Technology Conference (IEEE Cat. No.04CH37546), IEEE, pp. 1256–1262.

[93] Zipperian, D., 2011, Metallographic Handbook, Pace Technologies.

[94] Buehler, L., 2007, Buehler Sum-Met – The Science Behind Materials Preparation, Buehler.

[95] José María Servín Olivares and Cynthia Gómez Aceves. TOF SIMS Analysis for SnxOy Determination on Lead-Free HASL PCBs. SMT Magazine • October 2013 28-44.

[96] Zhu, Q. S., Zhang L., Wang Z. G., Wu S. D., Shang J. K., “Effect of Intermetallics Ag3Sn on the Tensile Property of Sn3.8Ag0.7Cu Solder Alloy”, Acta Metallurgica Sinica, Vol. 43(1), pp. 41-46, 2007.

[97] Ganesan, S., Pecht, M., Lead-free Electronics, Wiley-Interscience Publication, pp. 51-52, 2006.

[98]Pei M., Qu J. M., “Effect of Rare Earth Elements on Lead-Free Solder Microstructure Evolution”, Proceedings of the 57th Electronic Components and Technology Conference, pp. 198-204, 2007.

[99] Vianco P. T., “Fatigue and Creep of Lead-free Solder Alloys: Fundamental Properties,” Chapter 3 of Lead-free Solder Interconnect Reliability, Edited by D. Shangguan, ASM International, pp. 67-106, 2006.

[100] McCabe, R. J., Fine, M. E., “Athermal and Thermally Activated Plastic Flow in Low Melting Temperature Solders at Small Stresses,” Scripta Materialia, Vol. 39(2), pp. 189-195, 1998.

[101] Lu, H. Y., Balkan, H., and Ng, K. Y. S., 2006, “Effect of Ag content on the microstructure development of Sn-Ag-Cu interconnects,” J. Mater. Sci. Mater. Electron., **17**(3), pp. 171–188.

[102] Telang, A. U., Bieler, T. R., Zamiri, A., and Pourboghrat, F., 2007, “Incremental recrystallization/grain growth driven by elastic strain energy release in a thermomechanically fatigued lead-free solder joint,” Acta Mater., **55**(7), pp. 2265–2277

[103] Zijie Cai, “Reduction of Lead Free Solder Aging Effects Using Doped SAC Alloys” Auburn University

[104] Thomas Edward Sanders “Extreme Environment Reliability of Components for Computing with SAC305 and Alternative High Reliability Solders” Auburn University

[105] Song, J. M., Huang, C. F., Chuang, H. Y., “Microstructural characteristics and vibration fracture properties of Sn-Ag-Cu-TM (TM = Co, Ni, and Zn) alloys,” Journal of Electronic Materials, Vol. 35(12), pp.2154-2163, 2006.

[106] Anderson, I., Walleser, J., Harringa, J., Labbs, F., Kracher, A., “Nucleation Control and Thermal Aging Resistance of Near-Eutectic Sn-Ag-Cu-X Solder Joints,” Journal of Electronic Materials, Vol. 38(12), pp. 2770-2779, 2009.

[107] Pandher, R. S., Lewis, B. G., Vangaveti, R., Singh, B., "Drop Shock Reliability of Lead-Free Alloys - Effect of Micro-Additives," Proceedings of the 57th Electronic Components and Technology Conference, pp. 669-676, 2007

[108] Huang, M. L., Wang, L., "Effects of Cu, Bi and In on Microstructure and Tensile Properties of SnAg-X (Cu, Bi, In) Solders," Metallurgical and Materials Transactions A, Vol. 36(6), pp. l439-1446, 2005.

[109] Liu, P. L., Shang, J. K., "Interfacial Segregation of Bismuth in Cu/Sn-Bi Solder Interconnect," Scripta Meterialia, Vol. 44(7), pp. 1019-1023, 2001.

[110] Tateyama, K., Ubukata, H., Yamaoka, Y., Takahashi, K., Yamada, H., Saito, M., "Effects of Bi Content on Mechanical Properties and Bump Interconnection Reliability on Sn-Ag Solder Alloys," International Journal of Microcurcuits and Electronic Packaging, Vol. 23(1), pp. 131-137, 2000.

[111] Tegehall, P.E., IVF Project Report (ELFNET), 2006.

[112] Kang, S. K., Leonard, D., Shih, D. Y., Gignac, L., Henderson, D. W., Cho, S., Yu, J., "Interfacial Reactions of Sn-Ag-Cu Solders Modified by Minor Zn Alloy Addition," Journal of Electronic Materials, Vol. 35(3), pp. 479-485, 2006.

[113] Anderson, I., Cook, B., Harringa, J., Terpstra, R., "Sn-Ag-Cu solders and solder joints: Alloy development, microstructure, and properties," Journal of the Minerals, Metals and Materials Society, Vol. 54(6), pp. 26-29, 2002.

[114] Syed, A., Kim, T. S., Cho, Y. M., Kim, C. W., Yoo, M., "Alloying Effect of Ni, Co, and Sb in SAC Solder for Improved Drop Performance of Chip Scale Packages with Cu OSP Pad Finish," Electronics Packaging Technology Conference, pp. 404-411, 2006.

[115] Liu, W. P., Lee, C. N., “The Effects of Additives to SnAgCu Alloys on Microstructure and Drop Impact Reliability of Solder Joints,” Journal of The Minerals, Metals and Materials Society, Vol. 59(7), pp. 26-31, 2007.

[116] Amagai, M., Toyoda, Y., Ohnishi, T., Akita, S., “High Drop Test Reliability: Lead-Free Solders,” Proceedings of the 54th Electronic Components and Technology Conference, Vol. 2, pp. 1304-1309, 2004.

[115] Nogita K., “Stabilisation of Cu6Sn5 by Ni in Sn-0.7Cu-0.05Ni lead-free solder alloys”, Intermetallics, Vol. 18(1), pp. 145-149, 2010

[116] Cong Zhao, Auburn University, “Board Level Reliability of Lead-Free Solder Interconnections with Solder Doping Under Harsh Environment “

[117] Arnab Dasgupta, Fengying Zhou, Christine LaBarbera, Weiping Liu, Paul Bachorik, and Ning-Cheng Lee, “Reliability of PCB solder joints assembled with SACM™ solder paste”, Proceedings of SMTA International, 2014, Rosemont, IL.

[118] Sona, M., and Prabhu, K. N., 2013, “Review on microstructure evolution in Sn-Ag-Cu solders and its effect on mechanical integrity of solder joints,” J. Mater. Sci. Mater. Electron., 24(9), pp. 3149–3169

[119] Ubachs, R. L. J. M., Schreurs, P. J. G., and Geers, M. G. D., 2004, “Microstructure evolution of tin-lead solder,” IEEE Trans. Components Packag. Technol., 27(4), pp. 635–642.