Advances in Electronic Chaotic Oscillators with Applications in Communication Systems and Radar System

by

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Abstract

Chaos theory is an emerging topic in electronics due to some of the inherent properties that can be considered advantageous in particular applications. Some of these properties include topological mixing, continuous power spectral density, and long-term aperiodic behavior. In particular, the topological mixing and long-term aperiodic behavior can be useful in generating random numbers for security or encryption applications. Similarly, the continuous power spectral density could be advantageous in communication and radar systems. Many of these systems are often defined mathematically using an ideal set of ordinary differential equations. These systems are usually classified as either autonomous or non-autonomous systems. An autonomous system is not explicitly dependent on any variable, where as a non-autonomous system is explicitly dependent on a variable. This variable is often a time dependency. These dependencies can lead to both systems being implemented in electronics with different types of challenges. An autonomous system might have an elegant mathematical solution or can be implemented in a single PCB, but often requires high component count in addition to dealing with finite switching times and propagation delays in the feedback path. These limitations can lead to difficulty in scaling the hardware realizations to higher frequency applications. A non-autonomous system may be somewhat difficult to find a closed-form solution to, but it can be realized in a variety of very simple electronic circuits. These simple circuits are externally excited, which can be a problem in some applications. This work investigates these challenges by designing, simulating, and implementing both autonomous and non-autonomous systems in hardware. Three different systems are presented here in this work. The first is an autonomous exactly solvable chaotic system with a second-order filter. The second is a similar autonomous exactly solvable chaotic system with a first-order filter. The third system is a non-autonomous nonlinear transistor circuit where the forcing function is integrated onto a single PCB.

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List of Abbreviations

RNG	Random number generator
COTS	Commercial off the shelf
NSG	Noise signal generator
ASIC	Application specific integrated circuit
NIC	Negative impedance converter
GBP	Gain bandwidth product
AWGN	Additive white Gaussian noise
PCB	Printed circuit board
BJT	Bi-polar junction transistor

Chapter 1

Introduction

In this work, a collection of chaotic systems have been simulated, modeled, and realized in electronics. Many of these systems have been demonstrated to have advantageous properties either numerically or analytically; however, these properties may not be easily maintained in the electronic realization. Since many of the chaotic systems are defined using ideal mathematical equation or set of equations, it is important to investigate the design trade offs between how easy the system is to analyze mathematically versus the degree of difficulty in implementing these systems in electronics. A majority of the methods for analyzing nonlinear systems are often significantly more complex than methods used for linear systems. In addition, these nonlinear methods might be applied only under specific operational range or other restrictive circumstances. An alternative to analyzing these systems is to linearize them and use traditional techniques; however, this often omits some of the system's dynamics that may be very important.

This work looks at some of the limitations of emulating these systems in electronics. An example of these limitations would be the finite bandwidth, propagation delay, and switching times found in physical electronic devices and how they affect the maximum fundamental frequency that can be realized in hardware. In general, as the overall complexity of the electronic system increases, it becomes increasingly difficult to model the system mathematically. For this reason, this work also presents alternate toplologies of these systems that could potentially lead to more simple implementations.

Sometimes these chaotic equations can have a unique structure that can lead to elegant mathematical solutions [1]. One of these systems is based on an exactly solvable chaotic system

that is topologically conjugate to the iterated shift map (sometimes called the Bernoulli shift map) [1], [2]. This system can be rewritten as a linear convolution of symbols with a fixed basis pulse, which allows for the chaotic system to have an exact analytic solution [1]. This solution can be used to realize a matched filter for this system, making it an ideal candidate for chaos based communication systems, since a matched filter is the ideal detection method in the presence of additive white Gaussian noise (AWGN) [3]. This demonstrates that different types of chaotic system may be more applicable in certain applications over others. This work presents a chaotic communication system that was implemented in hardware using one of the chaotic oscillators developed in this work.

These chaotic systems are often placed into two different categories: autonomous and non-autonomous [4]. An autonomous system is not explicitly dependent on any particular variable. Similarly, a non-autonomous system is explicitly dependent on one or more variables. Typically this variable is time, but it can be any other parameter. These classifications help define the structure of these systems when they are implemented in electronics. In order to build an autonomous system, the circuit must be laid out in a manner that allows for a closed-loop feedback path. The initial conditions of this system need to be non-zero in order to make the system oscillate since it does not require an external input. This often happens naturally, because any practical system has thermal or some other external noise. Since the systems require a feedback path, finite propagation delays, switching times, slew rate, and internal coupling must be considered in the design. Similarly, external interference could cause the system to behave unexpectedly. One advantage of autonomous systems is that they can function as a stand-alone PCB that can be integrated into a larger system.

A non-autonomous system is often a nonlinear passive or active network that is driven by an external source, such as a function generator. Many of these non-autonomous systems are excited from a linear forcing function, such as a sine wave. Since these systems are excited externally, they often do not require any feedback. This also means that a bulky function generator or similar device is required if it is to be integrated into a larger system. This problem can be somewhat mitigated by integrating the forcing function onto a single PCB with nonlinear

passives. This effectively makes the non-autonomous system functionally the same as an autonomous system. These systems have been shown to be more resistant to external noise when being synchronized [5].

This work investigated some of the trade-offs associated with implementing both autonomous and non-autonomous chaotic systems in electronics. In order to do this, two similar autonomous and one non-autonomous system were constructing using PCB technology and commercial-off-the-shelf (COTS) parts. For these designs, alternate typologies were investigated for potentially increasing the fundamental operating frequency. While these systems are designed for different applications, they represent some of the challenges in designing that particular type of system.

An example of this can be seen in a non-autonomous chaotic nonlinear transistor circuit, that is composed of a NPN BJT and some passives [6]. This work takes that circuit and integrates the forcing function onto the same PCB. This circuit has also been shown to be capable of being used in chaotic synchronization [7]. This implementation uses four op-amps, a single transistor, resistors, and capacitors. No inductor is required. Even with the sinusoidal oscillator included on the board, the physical footprint of the design is only approximately 2.5 cm by 3.0 cm. The forcing function is generated using a twin-T op-amp oscillator and a nonlinear transistor circuit with two RC integrating constants. Using the appropriate resistor and capacitor values, the system can be operated from 2 kHz up to 9.6 MHz. This system could potentially be applied to a wide range of applications, such as an entropy source for random number generation (RNG).

The second system presented is an autonomous system based on the exactly solvable system originally introduced by Saito et al. in 1981 [2]. This system is one that lends itself well to applications, such as communications systems and radar [1]. This system is analogous to a negative resonance tank (RLC) circuit with discrete switching events. The negative resistor is implemented using a NPN BJT, and discrete capacitors and an inductor were used for the resonant elements. The switching events were triggered using a mixed-signal feedback network.

The third system is similar to the second one; however, this one is based on a first-order filter [8]. While this system appears to be relatively simplistic, further modifications can be

made in order to reduce the complexity of the system further. These modifications include replacing op-amps and comparators with inverters, as well as separating the analog and digital grounds. These modifications allow for the form factor of the system to be reduced as well as to make it more favorable for increasing the fundamental frequency of the oscillator.

Chapter 2

Background

In the 1960s, chaos was observed by scientists studying electrical devices [9], meteorological events [10], and population growth models [11]. Since these early studies, chaos has been observed and examined in a wide variety of disciplines [12], [13], [14]. Chaos theory has been used to help provide insight into predicting economical and financial events [15], modeling biological patterns for respiratory diseases [16], [17], studying the philosophy of education [18], [19], explaining the seemingly random underlying similarities across different disciplines and cultures [20], quantum systems [21], [22], astronomy and astrophysics, [23], [24], avoiding simulated annealing when solving approximate global optimization problems [25], modeling and simulation of chemical reactions and kinetics [26], [27], simulation algorithms for simulating both macroscopic and microscopic dynamics [28], [29], and modeling the the nonlinear effects of vibrations in physical structures [30], [31], [32].

Chaos is undesirable in some systems, such as some chemical reactions [33], [34], power electronics with switching DC to DC converters [35], [36], [37], chaotic motion in MEMS cantilever beam structures and oscillators [38], [39], chaotic vibrations in ground vehicle models [40], stabilization of an electro-chemical cells [41], control of complex time-varying networks [42], stabilization of a chaotic laser [43], [44], built in self test (BIST) for MEMS devices [45], avoiding arrhythmia or any other irregular heart beat problems [46], [47], and synchronization of chaotic oscillators [48], [49], [50]. In many of these applications, chaotic regime of operation is often problematic therefore avoided.

This motivation of modeling a specific phenomenon has now shifted towards taking advantage of the inherent properties found in chaos for various applications, such as communication

systems [51], [52], [53], [54], radar [55], [56], through-the-wall imaging [57], security and encryption algorithms, [58], [59], [60], random number generation (RNG) [61], [62], [63], [64], super computing applications [65], image encryption [66], [67], [68], [69], and noise signal generation [70]. Some of the advantageous properties include continuous power spectral density for communication, radar and noise signal generation. Additionally, the topological mixing and long-term aperiodic nature of chaos is beneficial in RNG [4].

While it may seem counterintuitive, but there have been various methods of control used to avoid chaos or stabilize periodic orbits. There are a wide range of methods used to control chaos [71], [72]. One method involves using small voltage perturbations that are periodically applied to a free running oscillator [73]. This method is sometimes referred to as the OGY chaos control, named after the authors initials Edward Ott, Celso Grebogi, and James York. OGY control requires that the desired unstable periodic orbit to be known prior to applying this method. Another method of chaos control is called proportional feedback control [74], [75], [76]. This method applies a control signal that is proportional to the difference of the current value of the oscillator with the desired value. A third method of controlling chaos is through dynamic limiting [77]. This method involves using a diode that turns off and on at a specific threshold in order to keep an oscillation at a desired trajectory. This can be can be visualized as adding or subtracting energy from a system in order to control the oscillator. These control methods can be used to encode information into a chaotic waveform for use in communication systems [54]. Another method of chaos control is by adding weak periodic pulses and noise to the system [78], [79]. This method has proven effective in electronic circuits [80]. A reliable control method is required in order to encode information into a chaotic waveform for it to be used in a communication system.

Many of the chaotic systems are defined by ideal autonomous third-order (or higher) ordinary differential equations [2], [81], [82]. In order to take advantage of the underlying characteristics of the chaotic systems in various applications, these systems often need to be implemented in electronic circuitry. The structures of autonomous systems often require a feedback path, which is negligible at lower frequencies. However, when the frequency is significantly increased, the finite propagation delays, switching times, slew rates, and limited bandwidth

associated with physical devices can cause problems in recreating the ideal system's dynamics [83]. One method of trying to minimize the overall propagation delay through the feedback path is to avoid the use of operational amplifiers and realize a similar function using only transistors. This can reduce the design complexity if the final product is intended for implementation in an ASIC [84]. However, some non-autonomous systems might scale more favorably with frequency when compared with an autonomous systems. [85].

The structure of non-autonomous systems typically consists of a linear forcing function and some sort of passive nonlinearity. Many of these systems are described in literature using ideal mathematical definitions, but some of these were observed when analyzing a nonlinear system in a laboratory environment [86], [87]. Chaos may be observed in nonlinear circuits possessing transistors or diodes with a tabletop function generator [6], [88]. These experiments are often used as a way to demonstrate the inherent nonlinearities in devices such as transistors or diodes [89]. While these are effective at demonstrating the underlying nonlinear dynamics, they are often at very low frequencies (in the range of tens of Hertz) and require external equipment, which limits in potential applications where high frequency operation can be beneficial [90].

In order to take advantage of these particular systems, the linear forcing function can be integrated onto a single printed circuit board (PCB) with these passive nonlinear circuits. There is a wide range of options to generate the linear sinusoidal oscillators. Some of the simplest methods to create sinusoidal signals include the usage of operational amplifiers (op-amps), which are sufficient for low to moderate frequencies. For higher frequencies, a transistor-based approach would most likely be better; however, circuit topology analysis is more difficult when transistors are present.

2.1 Autonomous and Non-autonomous Systems

One of the common classifications of dynamical systems is whether it is autonomous or non-autonomous. Explicit dependence on an independent variable (e.g., time) determines if a system is autonomous. This classification does play an important role on how these systems are realized in electronics.

An autonomous system relies on feedback in order to oscillate. When seeking high frequency versions of these systems in electronics, the finite propagation delays, switching times, limited bandwidth, and slew rates can become problematic. An autonomous system is typically defined mathematically and has been numerically or analytically analyzed using traditional techniques. To emulate these systems in electronics, it often requires complex functions and a large amount of components to be realized. One of the primary advantages of an autonomous system is that it does not require an external trigger in order to oscillate.

Similarly, non-autonomous systems do not require a feedback path, which means that propagation delay is less of an issue. However, it can still adversely be affected by limited bandwidth and switching times of physical devices. These systems (when realized in electronics) tend to rely on nonlinear device parameters in order to achieve chaotic motion. Since many of these devices are somewhat difficult to accurately model, less research efforts have been utilized to analyze these systems mathematically.

2.2 Autonomous Systems: Chaos Based on First-Order and Second-Order Filters

There are two types of autonomous systems presented in this work. Both of these systems are topologically conjugate to the iterated shift map. The underlying dynamics of these two systems will be explained in the following sections.

Both of these systems have been shown in previous work to have an exact analytical solution [1], [8]. This solution can be used to develop a matched fitler for this system [91]. Chaotic communication systems have an elegant methods for encoding information into the waveform [54]. In order to do this, a system's allowable grammar must be analyzed. The grammar of a system is the allowable symbol sequences that a system can exhibit. This is done by looking at the free-running oscillations of the system. These oscillations are then mapped to a discrete system, which requires that certain unique segments of the waveform to be identified. An example of this may be the mapping of a local maxima or minima to the discrete states of a binary system, which can be done with a bi-polar type of system [54].

As previously stated, the use of small voltage perturbations can control the oscillations to specific trajectories of free-running waveforms [73]. This is a way of encoding the information

into the chaotic waveform. One advantage chaotic communication has over other traditional spread spectrum methods is that encoding a single received symbol can contain the information of more than one symbol. This is because there are a finite number of allowable sequences of symbols described by the symbolic dynamics of the system. Restricting the grammar means that, in order to decode certain symbols, only some of the subsequent symbols need to be sampled. This means that in order to decode certain symbols, only some of the subsequent symbols needs to be sampled. This results in a more efficient encoding scheme over other traditional techniques where every part of the received signal must be sampled.

2.2.1 Exactly Solvable Chaos Based on a Second-Order Filter

Simple systems can sometimes exhibit very complex behavior. An example of this can be seen in one dimensional maps, where chaotic motion can exist. The one dimensional map of particular interest is the iterated shift map, which is sometimes referred to as the Bernoulli shift map or sawtooth map, shown in Fig. 2.1. This map is mathematically defined using the modulo function, mod, shown in (2.1) [4].

$$x_{n+1} = 2x_n[mod(1)] \tag{2.1}$$

This discrete timed map can be described as a binary decimal with an initial condition of x_0 as seen in (2.2). Here, the binary decimal a_j can be either a "0" or a "1".

$$x_0 = 0.a_1a_2a_3... = \sum_{j=1}^{\infty} 2^{-j}a_j \tag{2.2}$$

Each new iterate of the map will result in a bit-shift of the initial condition to the right, replacing anything before the decimal point with a zero. This process demonstrates that the more precise bits, which are very insignificant in the initial value, will gradually become more significant in each iteration. Here, it can be seen that small changes in the starting value can significantly impact the system's future states. This is an example of the system's sensitivity to initial conditions, a characteristic of chaotic systems.

A chaotic system that is conjugate to the iterated shift map was previously developed by Saito and Fujita [2]. This particular chaotic system was synthesized from a linear continuous-timed, second-order differential equation combined with discrete states. The system is defined by the differential equation seen in (2.3). Here, the continuous time variable is u and the nonlinear switching event is $s(t)$.

$$\ddot{u} - 2\beta\dot{u} + (\omega^2 + \beta^2)(u - s(t)) = 0 \tag{2.3}$$

The discrete states of the nonlinear switching event are defined by $s(t)$, as shown in (2.4). The discrete states switch when a specific guard condition criterion is satisfied.

$$s(t) = \begin{cases} +1 & u(t) \geq 0,\ \dot{u}(t) = 0 \\ -1 & u(t) < 0,\ \dot{u}(t) = 0 \end{cases} \tag{2.4}$$

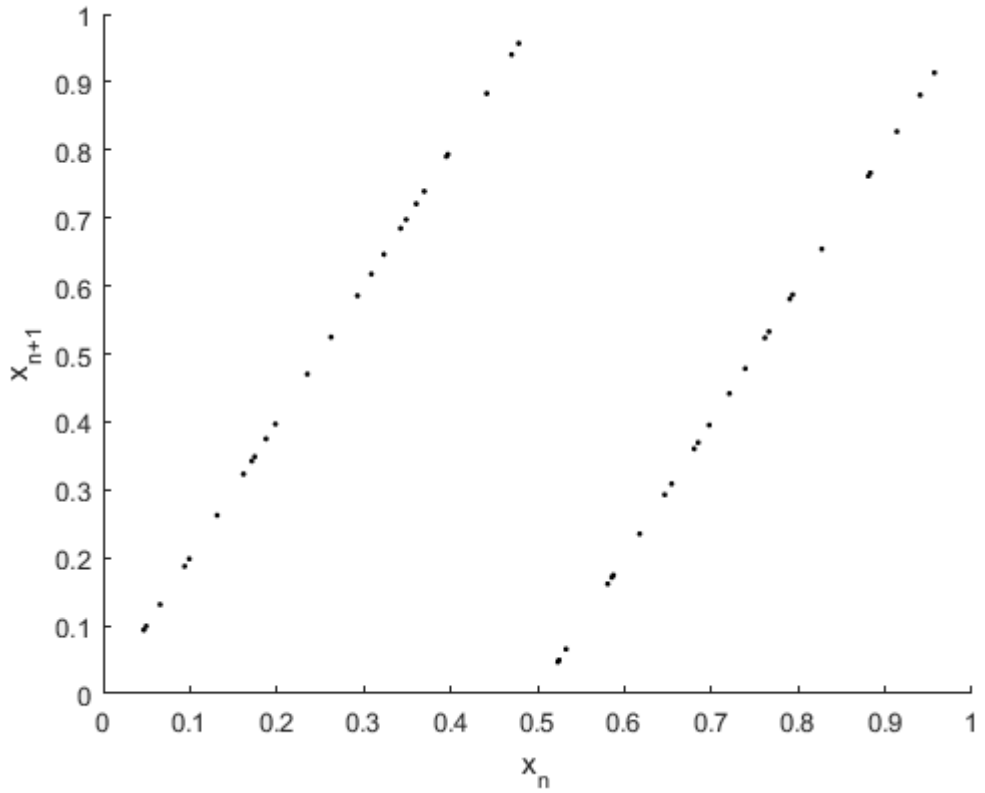

Figure 2.1: Ideal shift map generated from (2.1).

For simplification purposes, the system parameter ω is often defined at a normalized frequency, where $\omega = 2\pi$. The parameter β is a positive Lyapunov exponent of the linear second-order differential equation that provides energy to the system. β is restricted over the range $0 < \beta \leq \ln(2)$. With low values of β, the grammar of the oscillator is restricted. As the value of β increases, more stable trajectories appear in the oscillations. If β is greater than $\ln(2)$, then the positive Lyapunov exponent dominates, and the system becomes globally unstable. The initial conditions for this system are defined as $x(0) = x_0$ and $\dot{x}(0) = y_0$. Together, linear, second-order ordinary differential equation and the discrete switching function define a chaotic system with three degrees of freedom.

When the $s(t)$ is defined as $s(t) = \{+1, -1\}$, as shown in (2.4), the trajectory resembles a double-scroll or butterfly attractor. This type of oscillation does not exhibit banding; however, it is often referred to as the "shift band" or "shift map" oscillator. This electronic oscillator implementation is designed to operate in the shift band. The nonlinear switching event defined by $s(t)$ will switch states when the guard condition is satisfied. This condition is met when there is a simultaneous zero crossing of both output, $u(t)$, and its derivative, $\dot{u}(t)$.

The nonlinear switching function in (2.4) defines the equilibrium points for the system. The discrete states could be defined as $s(t) = \{0, -1\}$ or $s(t) = \{+1, 0\}$, which results in similar dynamics to the folded phase space. This system is conjugate to the tent map and is often referred to simply as the folded band. The selection of the sign of discrete state "1" determines if the phase space is a right- or left-handed fold.

2.2.2 Exactly Solvable Chaos Based on a First-Order Filter

In the previous subsection, an exactly solvable system based on a second-order filter was discussed; here, an exactly solvable system based on a first-order filter is discussed. [8]. Like the second-order system, this system is also topologically conjugate iterated shift map, previously defined by (2.1), and this system was shown to have an exact analytical solution. One thing that makes this system different from many other chaotic systems is that it requires an external clock.

This system is governed by the equation found in (2.5), where V_s is defined by (2.6). Here, the states of the system are the two variables V and V_s. The parameter V is the continuous time state and V_s is the discrete state. The fundamental frequency of the chaotic system is defined by the time constant of the parameters R and C. As mentioned previously, this system is clocked. This clock is defined by, $f_{CLK} = \frac{1}{T}$. The system will be chaotic if $f_{CLK} \geq \ln 2$. The system's underlying dynamics can be thought of as an asynchronous switching square wave that is applied to an unstable first-order filter feedback network.

$$RC\frac{dV}{dt} = V - V_s \tag{2.5}$$

$$V_s(nT) = \begin{cases} +1, & v(nT) > 0 \\ -1, & v(nT) < 0 \end{cases} \tag{2.6}$$

This system has been shown to have a closed-form, exact analytical solution. This is done by writing the discrete states of $s(t)$ as the summation found in (2.7). In this equation, $s_n \in \pm 1$ and Φ is defined by the discrete peicewise function (2.8).

$$s(t) = \sum_{n=-\infty}^{+\infty} s_n \cdot \Phi(t - nT) \tag{2.7}$$

$$\Phi(t) = \begin{cases} 1, & 0 \leq 0 < T \\ 0, & \text{otherwise} \end{cases} \tag{2.8}$$

Looking at (2.5), you can define $V(t)$ as a first-order equation that is forced by the discrete feedback signal $s(t)$. From this, $V(t)$ can be solved in an integral form, as seen in (2.9).

$$u(t) = \int_t^{+\infty} s(\tau) \cdot e^{-t} d\tau \tag{2.9}$$

By substituting (2.7) into (2.9), we get the resulting equation found in (2.10).

$$u(t) = \sum_{n=-\infty}^{+\infty} s_n \cdot \int_t^{+\infty} \Phi(\tau - nT) \cdot e^{t-\tau} d\tau \tag{2.10}$$

We can then say the variable θ be Defining θ as $\theta = \tau - nT$, which means,

$$\int_{t}^{+\infty} \Phi(\tau - nT) \cdot e^{t-\tau} d\tau = e^{t-\tau} \cdot \int_{t-nT}^{+\infty} \Phi(\theta) e^{-\theta} d\theta \tag{2.11}$$

This results in the simplified summation,

$$u(t) = \sum_{n=-\infty}^{+\infty} s_n \cdot P(t - nT) \tag{2.12}$$

where P is the basis function that is defined as,

$$u(t) = e^{t} \cdot \int_{t}^{+\infty} \Phi(\theta) e^{\theta} d\theta \tag{2.13}$$

Evaluating Φ results in the following simplified piece-wise basis function,

$$P(t) = \begin{cases} (1 - e^{-T}) \cdot e^{t}, & t < 0 \\ 1 - e^{t-T}, & 0 \leq t < T \\ 0, & T \leq t \end{cases} \tag{2.14}$$

2.3 Non-Autonomous System: Nonlinear Transistor Circuit

There have been a wide range of nonlinear circuits with a relatively simple topology and minimal component count [92]. When considering potential systems that could be realized in electronics, the two types of systems often evaluated are autonomous and non-autonomous systems [93, 94]. Both of these types of systems have advantages and disadvantages when trying to build them in hardware. Autonomous systems, which are not explicitly dependent on any other variable (often time), are stand-alone oscillatory systems that can be realized with a feedback topology in electronics. One drawback to these autonomous systems at high frequency is that the propagation delay through the feedback path begins to limit the frequency scaling of the design [83]. This can make it difficult to realize these systems at very high frequencies.

Non-autonomous systems, which are explicitly dependent on another variable, are forced by an external source. Since these systems often do not have a feedback topology, they require

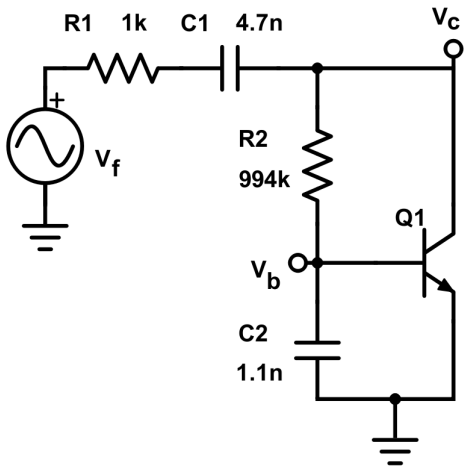

Figure 2.2: Schematic of the single transistor circuit.

some other form of external excitation, which in hardware could be a table-top function generator. Alternatively, the system's forcing function could potentially be integrated onto the same circuit board as the non-autonomous system. These forcing functions are often sinusoidal, which have a wide range of possible implementations [95, 94, 96, 97].

This work seeks to increase the frequency of operation of the nonlinear transistor circuit, which was previously discussed in a low frequency topology [6]. This circuit contains only one active component and four passive components, as seen in Fig. 2.2. The simple circuit was demonstrated in SPICE and on a prototype board, where the fundamental frequency was in the low audio frequency range (approximately 1.7 kHz to 2 kHz) [6, 7].

The single active device, an NPN BJT, is connected to two different resistor-capacitor (RC) filter networks. These two filter networks have different integrating time constants. One of these constants is associated with the forward active region, and the other is associated with the reverse active region of the BJT. The BJT oscillates by switching back and forth from the two integrating constants [6]. The time domain response appears to increase (with higher frequency oscillations) while in the forward active region, until the BJT switches to the reverse region. The switching times are aperiodic.

The nonlinear transistor circuit will transition between periodic and chaotic trajectories as the amplitude and frequency of the forcing function vary. This has been demonstrated in hardware prototypes on the frequency range from approximately 1 kHz to 8 kHz [98]. This

can be seen using a table-top variable function generator; however, this implementation of the circuit includes the forcing function on the same board. This was done using a twin-T oscillator and a variable gain stage. The frequency of the forcing function remained fixed and the amplitude was varied using a variable gain amplifier. This still allows for the hardware to demonstrate the periodic and chaotic solutions of the circuit, by sweeping through different amplitudes with a constant frequency.

Chapter 3

Design Approach

Many of these chaotic systems often require a large number of components in order to implement them in electronics. In order to make this process more manageable, it is often helpful to divide the system into smaller subsystems. This chapter details how the three electronic circuits were developed and built by using this process.

The autonomous second-order exactly solvable system can be divided into three subsystems that are typically used in chaos to describe how chaotic systems evolve over time. These subsystems are the stretch, twist, and folding mechanisms. The first-order system's original circuit topology was investigated. It was determined that the system could be implemented using alternate components while maintaining the same functionality by separating the analog and digital grounds. This alternate topology is later shown to be favorable for higher frequency operation.

While the non-autonomous nonlinear transistor circuit is relativity simple since it only consists of 5 circuit components, it does require an external forcing function. This forcing function has been integrated onto the PCB with the nonlinear transistor circuit, which defines the subsystems. These subsystems are the forcing function generator, a variable gain stage, and the nonlinear transistor circuit.

3.1 Exactly Solvable Chaos

These two exactly solvable chaotic systems share similar characteristics; however, the major difference is the order of the filter used in the feedback loop. In the electronic realizations of

these, one of these is based on a second-order RLC resonant tank, while the other is based on a first-order RC resonant circuit. These next two sections detail how these two systems were divided into subsystems to make them more easily realized in electronics [51], [99], [100].

3.1.1 Second-Order Filter

The design approach for this oscillator is inspired in part by E. Ott, who described the "stretch-twist-fold" operation of a chaotic system based on the iterated shift map [4]. He illustrated this process using a circle. The circle undergoes a stretching process in which the radius increases in size. When the radius has reached a certain point, the circle undergoes a twisting process where it is twisted into a figure-8 shape. From this state, the figure-8 shape undergoes a folding process, in which two loops of the figure-8 are overlaid on top of each other. This process shares similar characteristics to the system described by (2.3) and (2.4). Therefore, these descriptions will be used as guidance to define the separate subsystems of the electronic oscillator's design.

The oscillator design has been divided into three separate subsystems: the stretching mechanism, the folding mechanism, and the guard condition in the structure, shown in Fig. 3.1. The stretching mechanism dynamics can be described as an exponential growth of a sinusoid, similar to the stretching process described above for the circle. This subsystem alone is unstable, and shares characteristics with the parameter β in (2.3). The stretching mechanism supplies energy to the system, which is required to achieve stable electronic oscillations in a practical system.

The stretching subsystem is constrained by a feedback network comprising the folding mechanism and the guard condition. The unstable oscillations of the stretching mechanism are stabilized by this feedback network. The folding mechanism subsystem acts in a similar manner to the "twist" and "fold" operation illustrated by the circle example. The third subsystem, the guard condition, generates an asynchronous clock signal that triggers the folding mechanism process. The guard condition of this system is triggered when two specific criterion are met simultaneously. The first is when there is a zero crossing of the output of the oscillator. The second criterion is triggered when there is a zero crossing of the derivative of the oscillator's output.

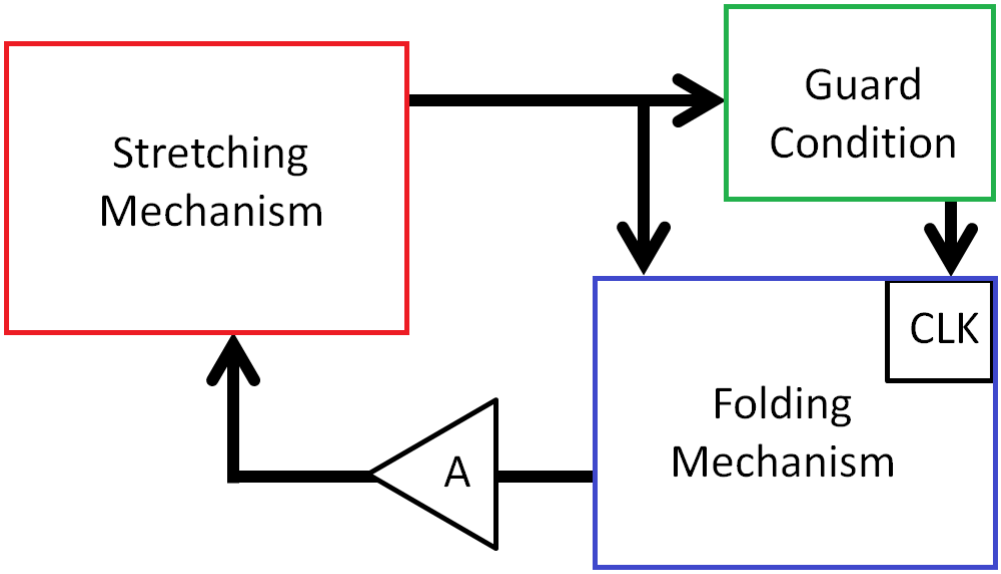

Figure 3.1: Generalized block diagram of the oscillator design.

The folding mechanism and the guard condition generate the discrete states of the chaotic oscillator defined by $s(t)$ in (2.4). In practice, these two subsystems will be composed primarily of comparators and digital logic components. For this reason, a gain block, A, is included to convert the equivalent logic levels to the desired ± 1 V.

The generalized circuit schematic for the oscillator design is presented in Fig. 3.2. The electronic implementation of the stretching mechanism uses a single transistor configured in a common-base amplifier topology. The amplifier is combined in parallel with a LC resonant tank circuit. These three components, plus the biasing resistors for the transistor, define the stretching mechanism subsystem. The output of the stretching mechanism is taken at the collector port of the transistor. The simulation results take into account the non-ideal device properties by using detailed empirical models for the components.

The parallel LC resonant elements set the fundamental frequency of the oscillator, as defined in equation (3.1). As seen in Fig. 3.2, the two capacitors, $C1$ and $C2$, are effectively in series. Using the values from the schematic in Fig. 3.2, the fundamental frequency of the oscillator should be approximately 18.9 kHz, as shown in equation (3.1).

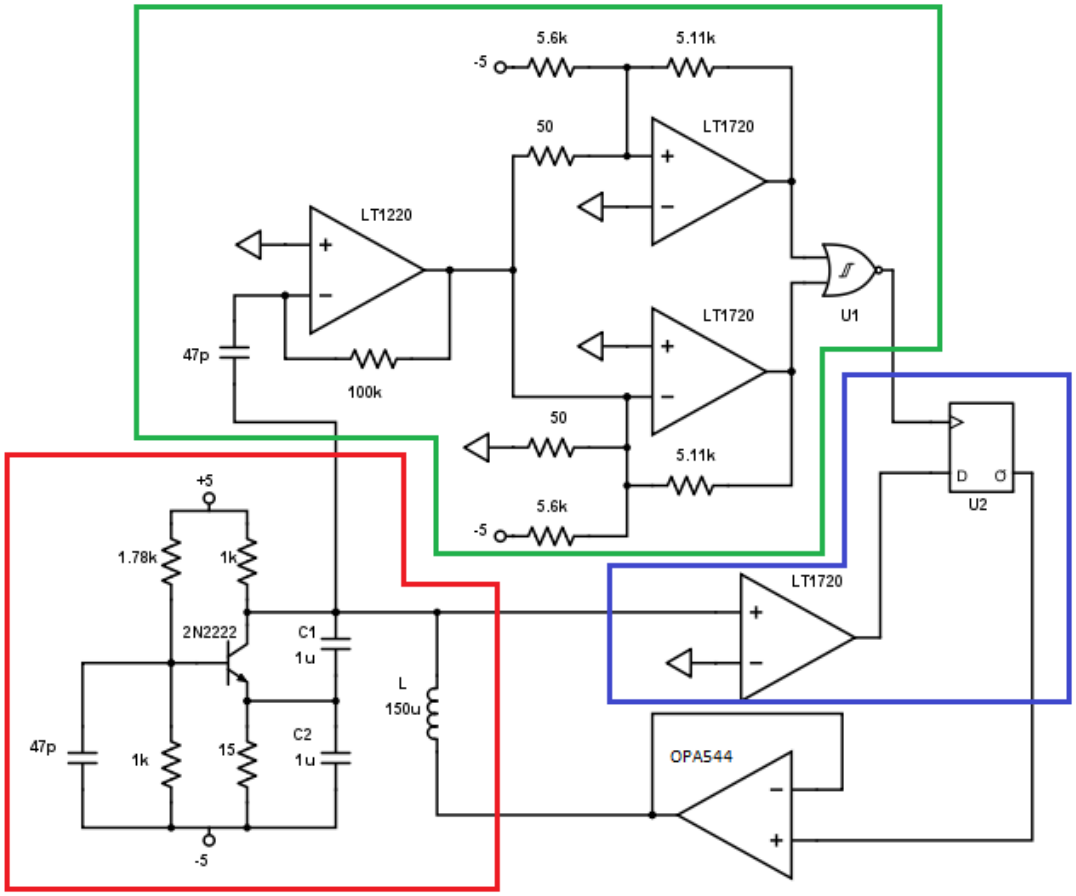

Figure 3.2: Generalized schematic of oscillator with the stretching mechanism (red), folding mechanism (blue), and guard condition (green) subsystems.

$$f_n = \frac{1}{2\pi\sqrt{L(\frac{1}{C1} + \frac{1}{C2})}} \approx 18.9 \text{ kHz} \tag{3.1}$$

The folding mechanism and guard condition use the output of the stretching mechanism to generate the feedback signal, V_s. These two systems complete the feedback network of the oscillator. The folding mechanism subsystem is implemented using a comparator that determines the sign of the oscillator's output. This is fed into the data input terminal, labeled D, on the D-latch.

The guard condition is implemented using a zero crossing detector of the derivative with hysteresis. The derivative signal is generated using an analog differentiator. The zero crossing detector requires two comparators, one to detect the zero crossings of the falling edges and the other for the rising edges. The hysteresis is applied using feedback resistors in a Schmitt trigger

topology. The hysteresis is important because it decreases the system's sensitivity to noise. The zero crossing detector clocks the D-latch.

3.1.2 Common-base Colpitts Oscillator

The proposed circuit topology replaces the NIC with a common-base Colpitts oscillator. This circuit topology, found in Fig. 3.3, has been used as a linear oscillator as well as a nonlinear oscillator that can exhibit chaos [101]. Here, the parameter C_{BP} is the bypass capacitor for the small signal base connection to ground and the resistors R_{B1} and R_{B2} set the bias point of the transistor. Using the hybird-pi small signal model for the BJT, the schematic simplifies to the schematic found in Fig. 3.4. The transistor's transconductance is defined as $g_m = \frac{I_c}{V_T}$, where I_c is the collector current, V_t is the thermal voltage, and the parameter $r_\pi = \frac{\beta}{g_m}$, where β is the gain of the transistor.

For the system to oscillate, the Barkhausen criterion must be satisfied such that the loop gain, $A \cdot B = 1\underline{/0^\circ}$ at the fundamental frequency. For the system to have negative damping, $|A \cdot B| > 1$. Breaking the loop between the points A and B in Fig. 3.4, the resistance looking into the terminal is defined by R_A in (3.2). Here the voltage, V_T, is the voltage across the lower capacitor and the current, i_T, is the current flowing out of the same capacitor.

$$R_A = \frac{V_T}{i_T} = \frac{1}{\frac{1}{r_\pi} + \frac{1}{R_2} + g_m} \tag{3.2}$$

By substituting R_A into the schematic and breaking the node between A and B from Fig. 3.4, we get the resulting shcematic found in Fig. 3.5. Using this schematic, the three voltage nodes, V_{in}, V_o, and V_1, are used to calculate the loop gain, AB. In order to do this, the two capacitors, C, act as a voltage divider between the voltage node V_1 and V_o. Treating these capacitors as an ideal capacitive transformer leads to the relationship of R_A to R_1 as $R'_A = n^2 R_A$. Further simplification yields that $\frac{1}{n} = \frac{1}{2}$. Using this, the loop gain terms A and B can be seen in (3.3) and (3.4), respectively. Combining these two results in the overall loop gain found in (3.6). When the magnitude of (3.6) is greater than 1, then the system will exhibit growing oscillations in amplitude.

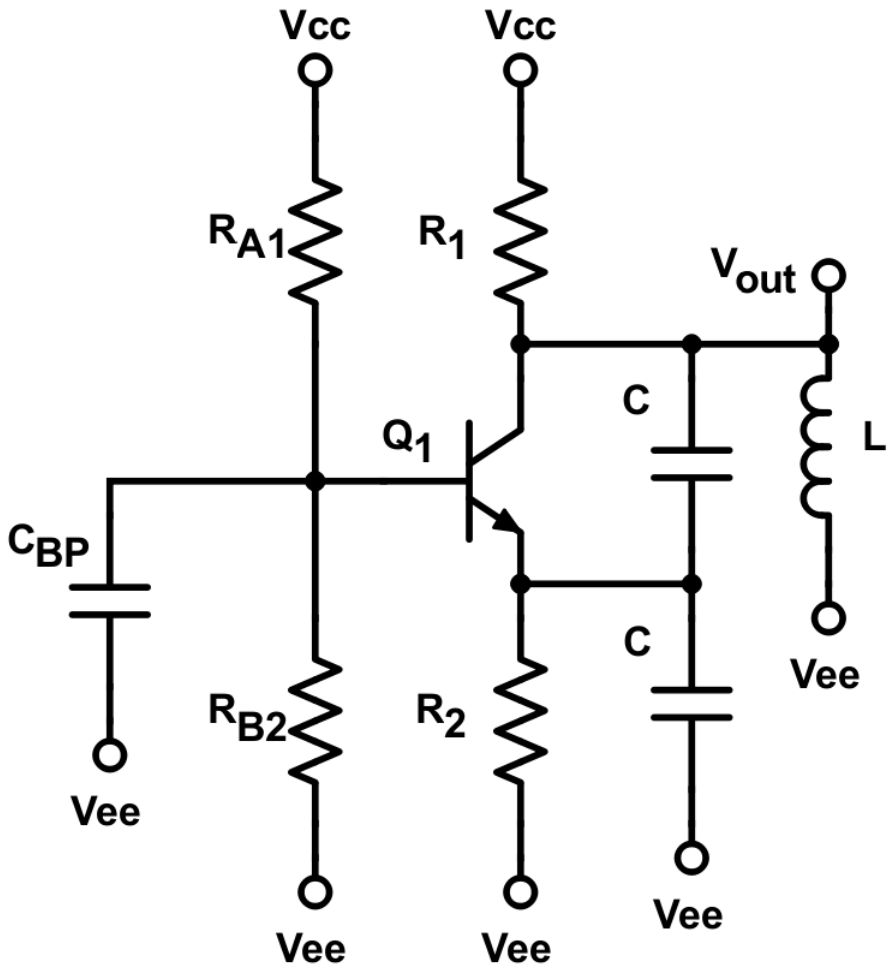

Figure 3.3: Schematic of the common-base Colpitts oscillator.

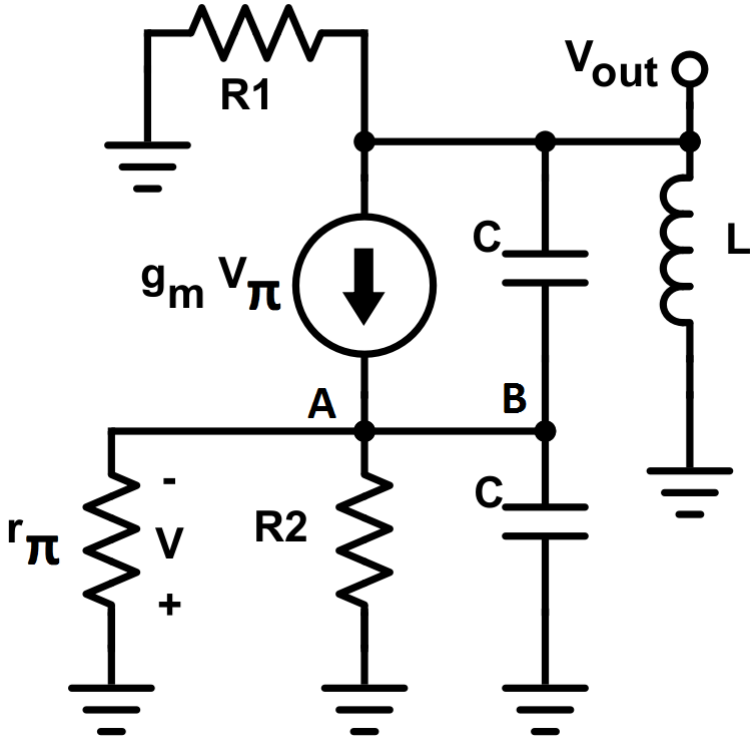

Figure 3.4: Schematic of the common-base Colpitts oscillator with the hybrid-pi small signal model.

$$A = \frac{V_1}{V_{in}} = \frac{g_m}{\frac{1}{R_1} + \frac{1}{4R_A}} \tag{3.3}$$

$$B = \frac{V_o}{V_1} = \frac{C}{C + C} = \frac{1}{2} \tag{3.4}$$

$$AB = \frac{g_m}{2(\frac{1}{R_1} + \frac{1}{4R_A})} \approx \frac{g_m R_1}{2(1 + \frac{g_m R_1}{4})} \tag{3.5}$$

$$AB = \frac{g_m R_1}{2[1 + \frac{R_1}{4}(\frac{1}{r_\pi} + \frac{1}{R_2} + g_m)]} \tag{3.6}$$

3.1.3 First-Order Filter

The original first-order system was realized using three op-amps, a comparator, a D flip-flop, and various passives, as seen in Fig. 3.6 [8]. This design used an amplifier that operated on

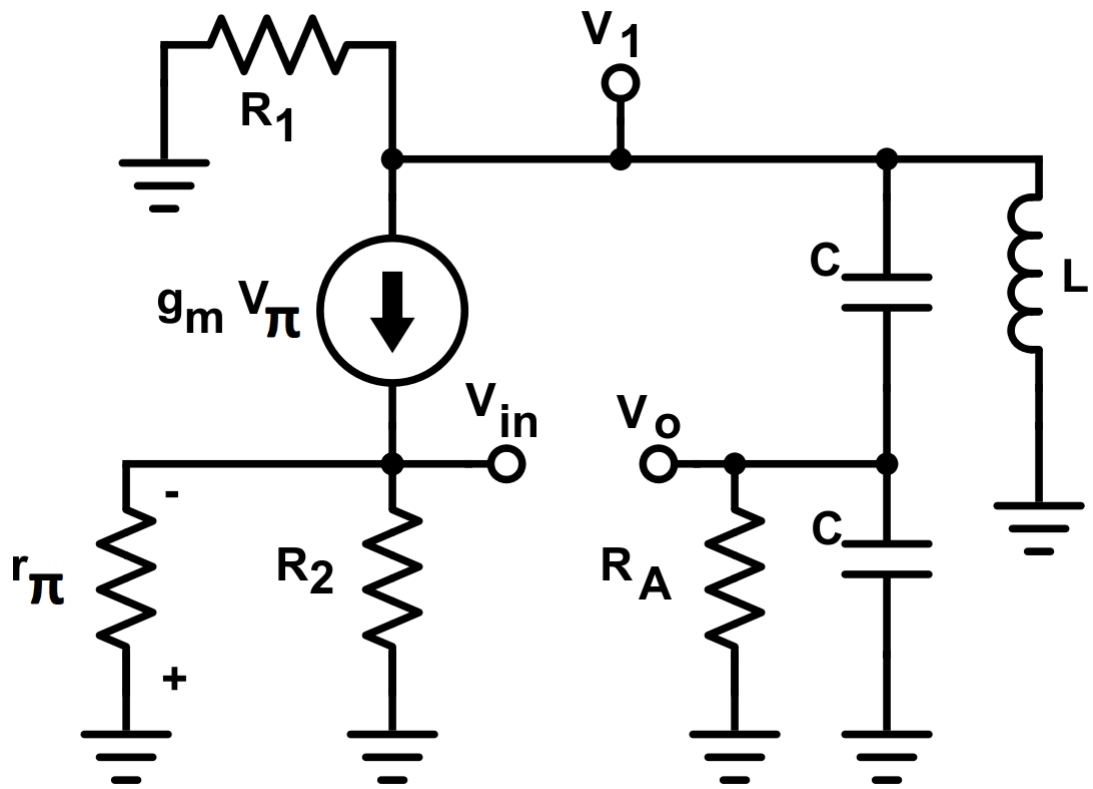

Figure 3.5: Schematic of the simplified circuit.

a differential power supply and the digital components operated on a single positive power supply. This meant that the analog ground of the amplifier and the digital ground were both at 0V, which is why the level shifting circuit was required. The comparator determines when the analog signal, V, changes signs.

The alternate circuit topology is designed to operate from 0V up to V_{dd} [102]. This allows for the digital grounds to stay at 0V, while the analog ground is moved to $V_{dd}/2$. This is important because the typical trip voltage of a CMOS inverter is $V_{dd}/2$, which allows for the inverter to effectively replace the comparator. Since the analog ground is now set at $V_{dd}/2$, the zero crossings of the analog ground can be detected by simply using an inverter. Two inverters were used in order to maintain the polarity of the original signal. The same D flip-flop was used for both circuit topologies. This unstable filter network portion of the circuit is equivalent to a -RC circuit. The -R is realized using an op-amp circuit topology called a negative impedance converter (NIC), which is combined with the capacitor, $C1$, to form the filter.

3.2 Forced Nonlinear Transistor Circuit

The design of the nonlinear transistor circuit can be divided into three separate subsystems, as defined in Fig. 3.8 [103], [104]. The first subsystem is a linear oscillator that generates the forcing function. This is realized using a single op-amp and a network of resistors and capacitors. The next subsystem modifies the linear forcing function so that the magnitude of the sinusoidal waveform can be adjusted. This is variable gain stage subsystem. The final subsystem is the non-autonomous nonlinear transistor circuit.

3.2.1 Sinusoidal Forcing Function

The nonlinear transistor circuit is non-autonomous and is often demonstrated in hardware using a tabletop function generator. This is fine for demonstration purposes; however, there are other ways that the system can be forced. By integrating the forcing function onto the board with the nonlinear transistor circuit, the overall system can be viewed as functioning in a similar manner to an autonomous system.

There are many different ways to generate a linear sinusoidal response in electronics. One of these methods uses an unstable op-amp topology with a feedback network of resistors and capacitors. These passive devices are configured in a shape similar to the capital English letter "T". The topology uses two of these RC networks, one configured as a high pass filter and the other as a low pass filter. These are combined in parallel and function as a notch filter with a large stop band. Therefore, this circuit topology is called the twin-T oscillator.

In order to maintain the linear sinusoidal oscillations, the tolerance on the feedback resistors and capacitors needs to be very tight; otherwise, the oscillation will decrease in amplitude. This can be somewhat problematic in practice since precision resistors are readily available in various values with very tight tolerances, while capacitors are more difficult to manufacture at high tolerances in a wide range of values. The twin-T circuit requires both a nominal capacitor value and one that is double that value. In order to realize this, capacitors can be combined in parallel by stacking two capacitors on top of each other on a single 0805 SMD resistor footprint. This way, any precision capacitor value can be used without requiring twice the value to

be manufactured in precision accuracy. By varying only the capacitors in the twin-T oscillator and the capacitors in the transistor circuit, the PCB was tested at varying frequencies with promising results. The capacitors of interest are those that set the forcing function's frequency (C3, C4, and C5 in Fig. 3.8) and sizing the transistor capacitors appropriately (C1 and C2 in Fig. 3.8).

3.2.2 Variable Magnitude and Frequency

Since the system undergoes multiple bifurcations based on the magnitude and the frequency of the sinusoidal forcing function, there needs to be a way to modify the magnitude and frequency in the circuit in order to see various orbits of the nonlinear transistor. Unfortunately, the twin-T network oscillates at a fixed frequency and magnitude. In order to change this on the oscillator, multiple capacitors or resistors need to be variable. For this reason, the forcing function has been chosen to operate at a fixed frequency; however, an additional circuit is added to the output of the twin-T to make the magnitude of the sine wave adjustable. This is done using an inverting op-amp circuit with a potentiometer as the feedback resistor. In order to observe different frequencies of operation, multiple boards were assembled with different RC values in the twin-T network.

While this subsystem appears to be one of the simplest of the three, it actually requires the most board real estate. This is due in part to the relative size of the potentiometer and the fact that the variable gain stage needs to be buffered from both the twin-T circuit and the nonlinear transistor circuit. This is done using two unity-gain voltage follower op-amp circuits.

3.2.3 Nonlinear Transistor Circuit

The nonlinear transistor circuit is a non-autonomous system consisting of a single BJT, two resistors, and two capacitors. The resistors and capacitors are configured such that there are two RC integrating time constants that are formed with the single transistor. These two RC integrators effectively oppose each other and this nonlinear interaction on the device level of the transistor can result in both periodic and chaotic motion. The mode of operation is determined by the magnitude and frequency of the forcing function. Since the sinusoidal twin-T oscillator

is held at a fixed frequency based on the populated capacitor values, the mode can be changed by adjusting the magnitude of the forcing function using the potentiometer.

In order to achieve chaotic motion, both the RC component tolerances and the layout must be taken into special consideration. In particular, the tolerances on the two capacitors, C1 and C2 from Fig. 3.8, need to be within 5% of their nominal value. The layout of the transistor with respect to the resistor, R2, and capacitor, C2, needs to be considered for higher frequency operation. The trace lengths required to make these connections need to be minimized while still taking into account any possible stray capacitance that could affect these two components. For this reason, the two components are located on the back very close to the transistor and shielded by the back layer of the board's ground fill on the PCB.

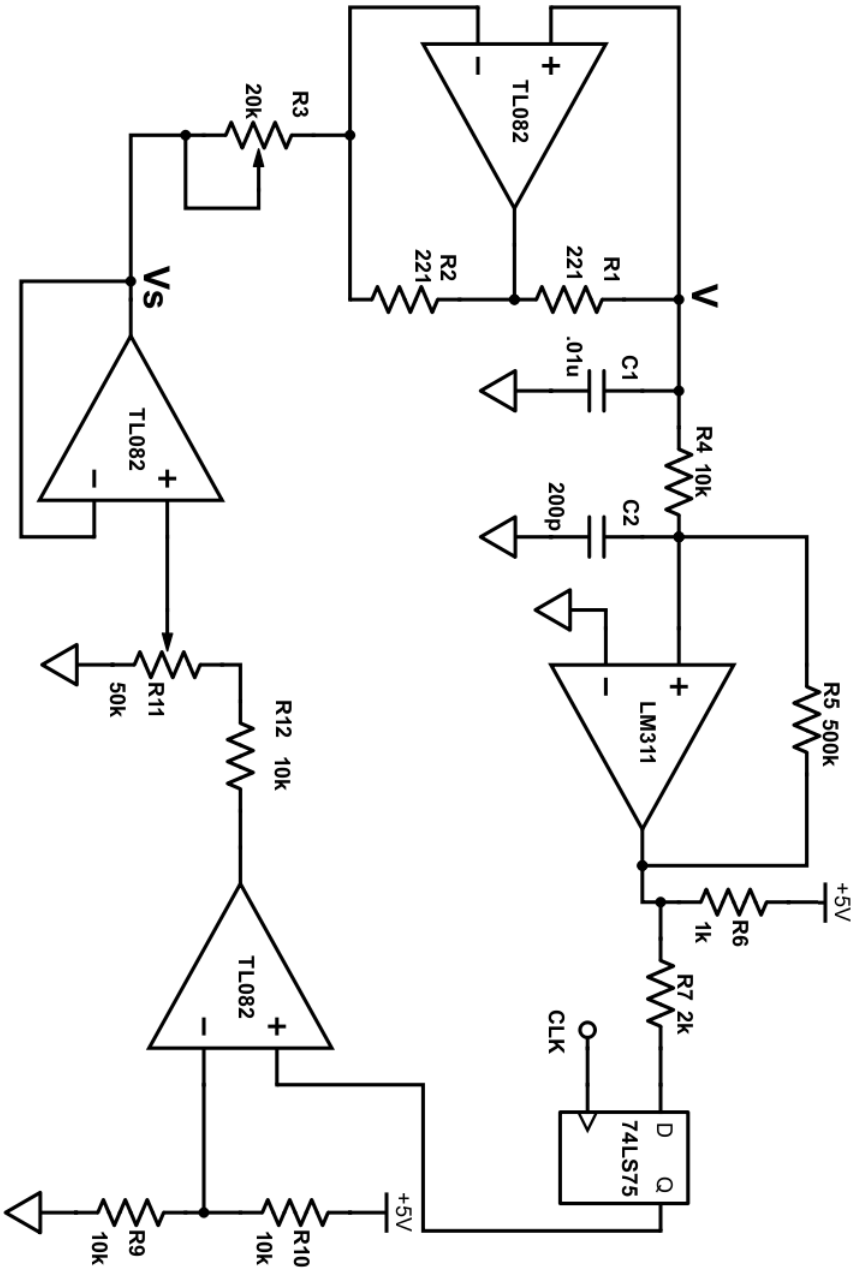

Figure 3.6: Schematic of the original first-order system with comparator and level shifting op-amp.

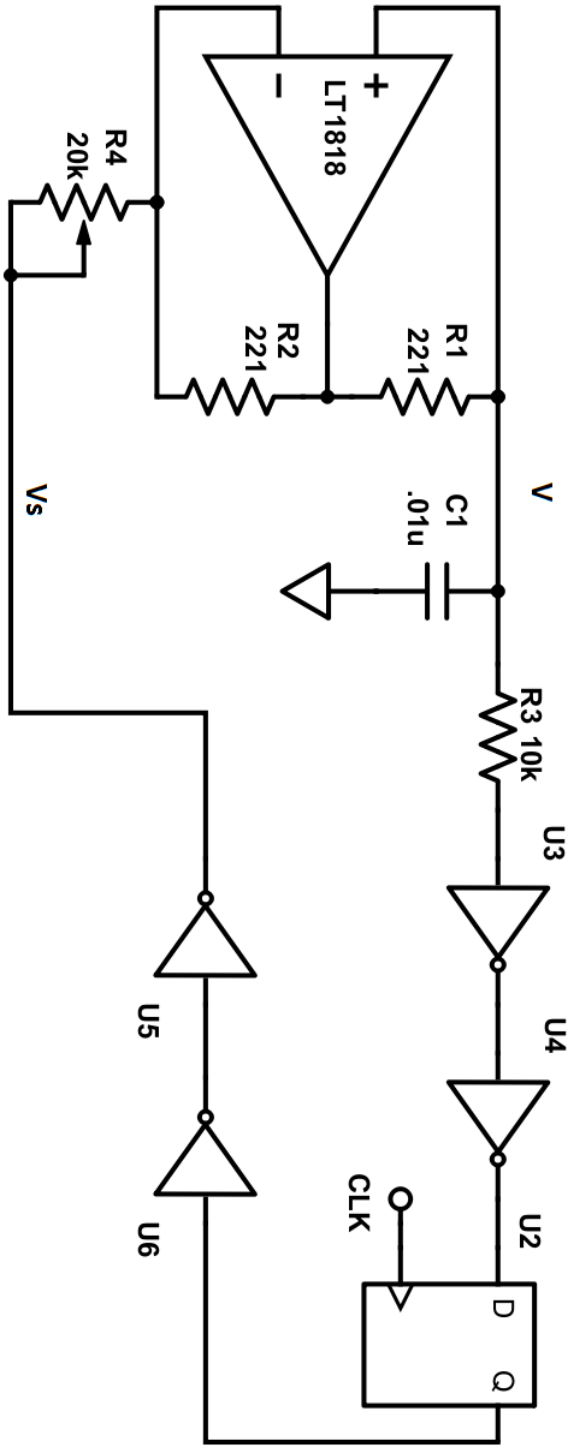

Figure 3.7: Schematic of the alternate topology of the first-order system.

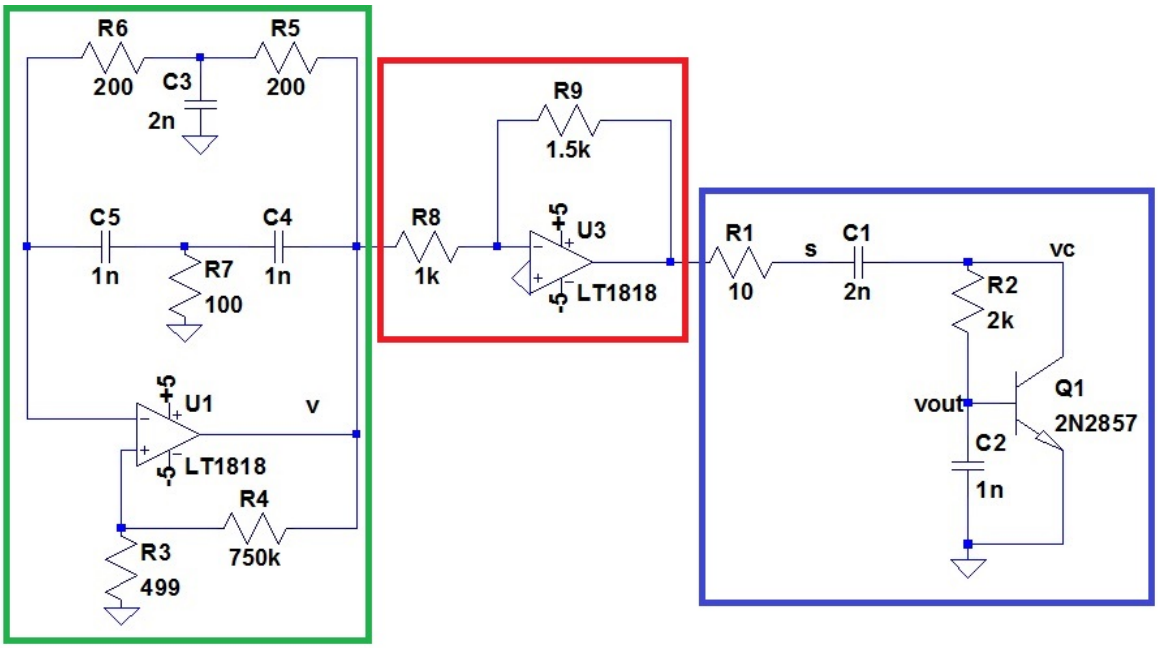

Figure 3.8: Schematic of the complete system, where green box is the sinusoidal forcing function, red box is the variable magnitude stage, and blue box is the nonlinear transistor circuit

Chapter 4

Simulation Results

Both of the exactly solvable systems and the nonlinear transistor system were simulated in SPICE. The simulations used detailed SPICE models of COTS devices where appropriate. The software used was LTspice. Many different components were simulated to find the best commercially available solutions while still maintaining a reasonable price point. Multiple parameters were taken into consideration, such as the bandwidth of the operational amplifiers and transistors, sensitivity to device tolerances, propagation delay, switching times, and slew rates.

The second-order exactly solvable system was initially designed using mostly operational amplifiers originally developed by Linear Technologies (LT1220), which was purchased by Analog Devices. While this device is a great general purpose amplifier, it does unfortunately come with a relatively high price point. For this reason, a less expensive amplifier (LT1818) is used as a replacement in some of the designs depicted. Based on the simulations, both of these devices perform very similarly for a majority of the amplifier configurations. Some exceptions for this are when the amplifier is configured as integrating or differentiating typologies. The LT1818 is very unstable in these configurations, and so these topologies should be avoided. For this reason, the LT1220 is used for the analog differentiation stage on the exactly solvable chaotic oscillator. The LT1818 is used for all other functions.

The first-order exactly solvable system was designed using the same LT1220 op-amp. Since the previously mentioned alternate topology contains now other analog components, digital models were used for the invertors and the D-flip flop. Many different devices were considered for this design, since the trip voltage of the invertors could vary across a wide range. It was also noted that some of these invertors have built-in Schmitt trigger inputs for better resistance

to false switches on noisy input signals. In this case, the Schmitt trigger input would set the trip voltage at a different voltage than one half the power supply rails. For this reason, inverters with Schmitt trigger inputs were not used.

The circuit configuration for the nonlinear transistor circuit does not require any integrating or differentiating amplifiers; therefore, the LT1818 was used for the designs. Multiple transistors were considered for the nonlinear transistor circuit. Some transistors produced distorted waveforms, which were easily demonstrated by the phase portraits.

4.1 Exactly Solvable Chaos Simulations

Both of the exactly solvable systems were simulated in LTspice using a wide range of device models. Both of these systems were intended to be used in a communication or radar application, so increasing the fundamental frequency of the oscillators was desirable.

4.1.1 Second-Order Filter

The results of the simulation are in high agreement with the original motivation system's dynamics. All the circuit simulation results were obtained using LTspice. The time domain results display the aperiodic output of the oscillator and the feedback signal in Fig. 4.2. Plotting the successive local maxima of the oscillator's output reconstructs a plot very close to the iterated shift map, as shown in Fig. 4.1. The code that generates this from the time domain data can be seen in Appendix A. The gain of the feedback signal and the offset of the oscillator scale the shift map plot to a range approximately of ± 1V.

The system exhibits dense orbits, an indication of topological mixing, that is shown in the phase space in Fig. 4.3. This implementation also demonstrates sensitivity to initial conditions, which is shown in Fig. 4.4. This plot displays two different simulation results with an initial condition of 1 (Red) and 1.0001 (Blue). Initially, the two trajectories are very close. However, after a short amount of time, the two trajectories diverge.

This topology eliminates the bandwidth limitation associated with the op-amp-based NIC's gain bandwidth product (GBP) by using a single transistor that is limited by the device's unity-gain current frequency (f_t). Generally this frequency will be much higher than an op-amps

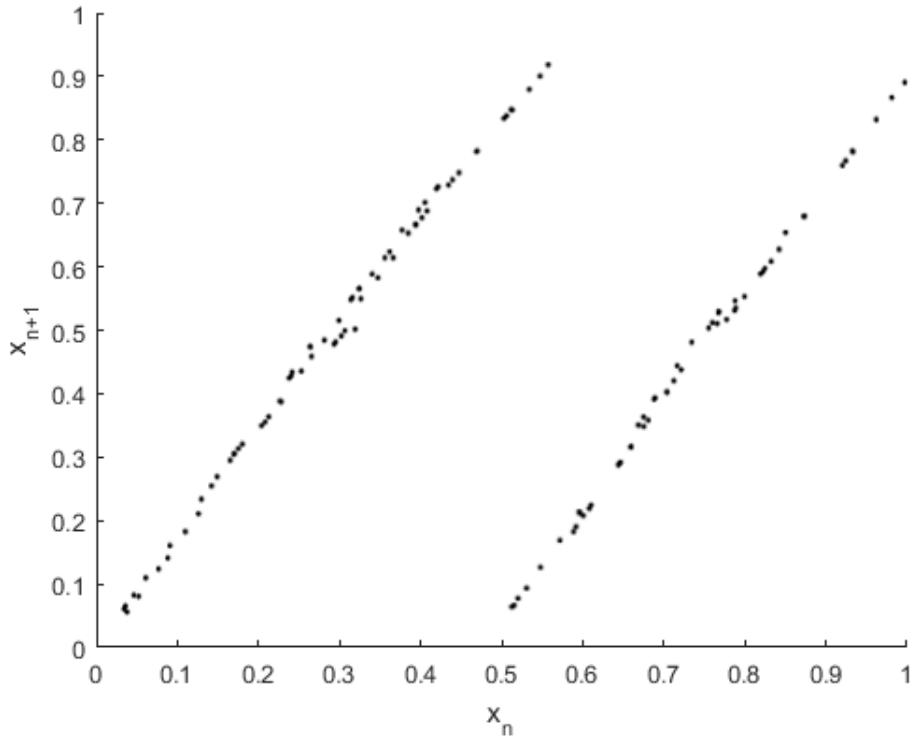

Figure 4.1: Plot of the local successive maxima of the oscillator from the simulated SPICE model.

GBP. From the simulation results, it was determined that the primary limiting factor in this design is the propagation delay through the electronic components in the feedback path. This design constraint is present in both the NIC and the transistor implementations; however, the NIC's bandwidth limitations concealed this in previous designs. This limitation of many COTS designs is somewhat mitigated by using high speed components, where the frequency could be increased to an order of 1 MHz.

By modifying the resonant tank circuit from Fig. 3.2, this circuit topology simulated from 2 kHz up to 7.8 MHz. For this, the capacitors $C1$ and $C2$ were changed to 500 pF, and the inductor L was changed to 0.8 μH, as shown in equation 4.1. The resulting time domain response for voltage nodes V and V_s is shown in Fig. 4.5. The corresponding phase space of the voltage nodes V versus V_d is shown in Fig. 4.6. It is worth noting that in both the time and phase space plots, there is noticeable distortion and ringing around the switching events for V_s. This is likely caused by the BJT portion of the circuit that provides the negative resistance. This is the maximum frequency that could be simulated in this topology. In the higher frequency

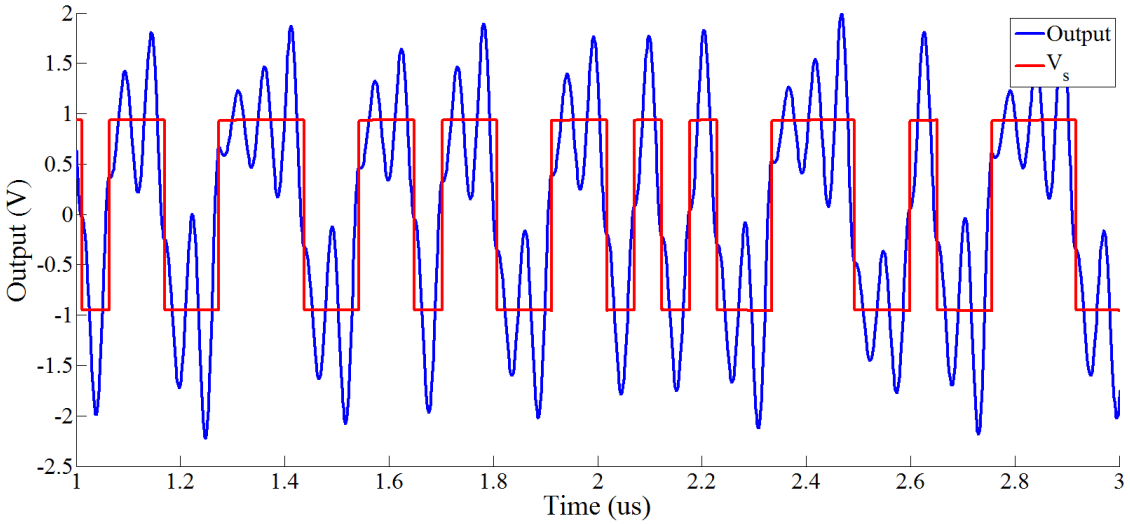

Figure 4.2: Time domain simulation results of the chaotic oscillator, where the output of the oscillator is plotted as blue and the output of the feedback network, V_s, is plotted as red.

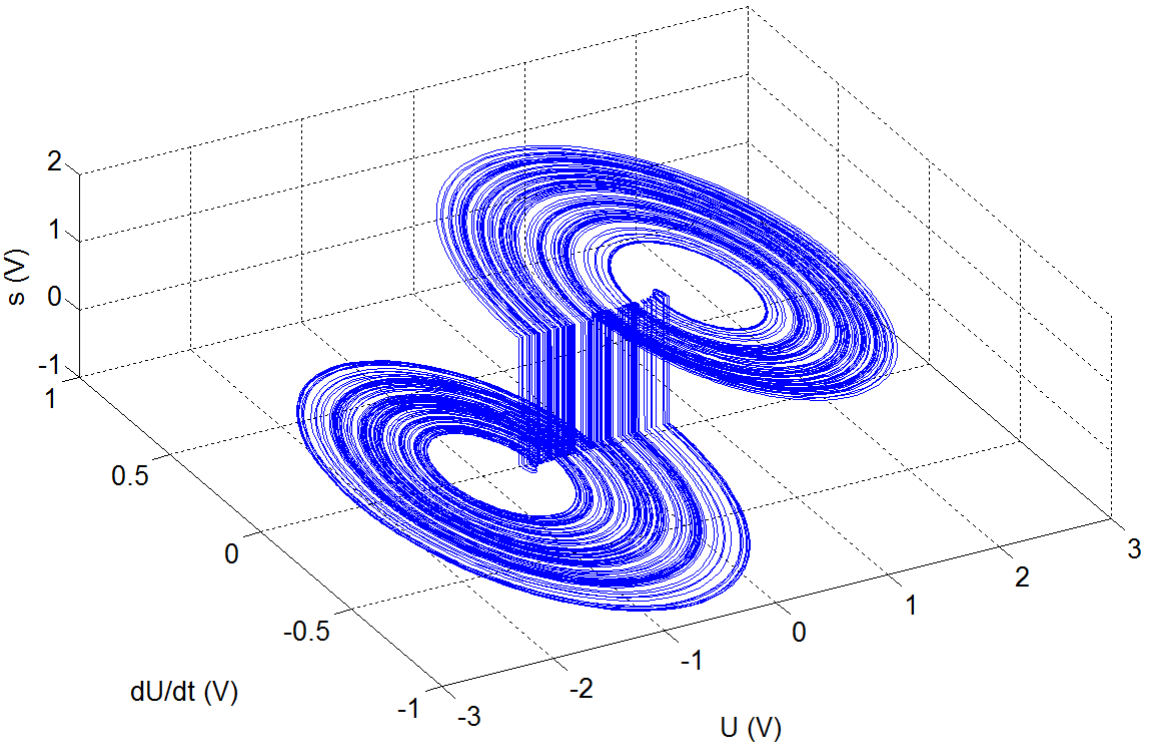

Figure 4.3: Phase space simulation results of the chaotic oscillator.

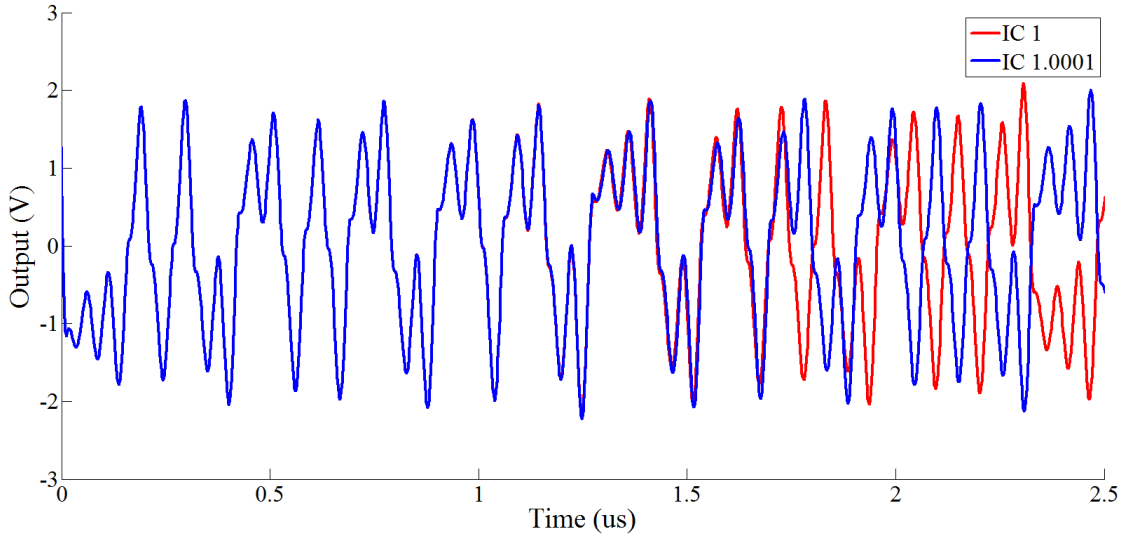

Figure 4.4: The initial output voltage of 1 is plotted as blue, and the initial output voltage of 1.0001 is plotted as red.

simulations, the BJT was no longer able to provide a sufficient negative resistance due to a lack of bandwidth.

$$f_n = \frac{1}{2\pi\sqrt{L(\frac{1}{C1} + \frac{1}{C2})}} \approx 7.8 \text{ MHz} \tag{4.1}$$

4.1.2 First-Order Filter

The alternate topology was simulated using LTspice. The SPICE model for the LT1220 was used; however, ideal models with user defined parameters were used for the inverter and the D flip-flop. The ideal inverters were defined to operate using 5V as a logic high and a trip voltage of 2.5V. Similarly, the D flip-flop operated at 5V and was given an ideal 1kHz clock. This clock was used to simulate a function generator.

The time domain response for the voltage nodes V and V_s from Fig. 3.7 can be seen in Fig. 4.7. By plotting the successive voltage node V at each of the rising edges of the clock versus the next one, the shift map from Fig. 4.8 can be generated. The simulation results are in agreement with the original system's dynamics.

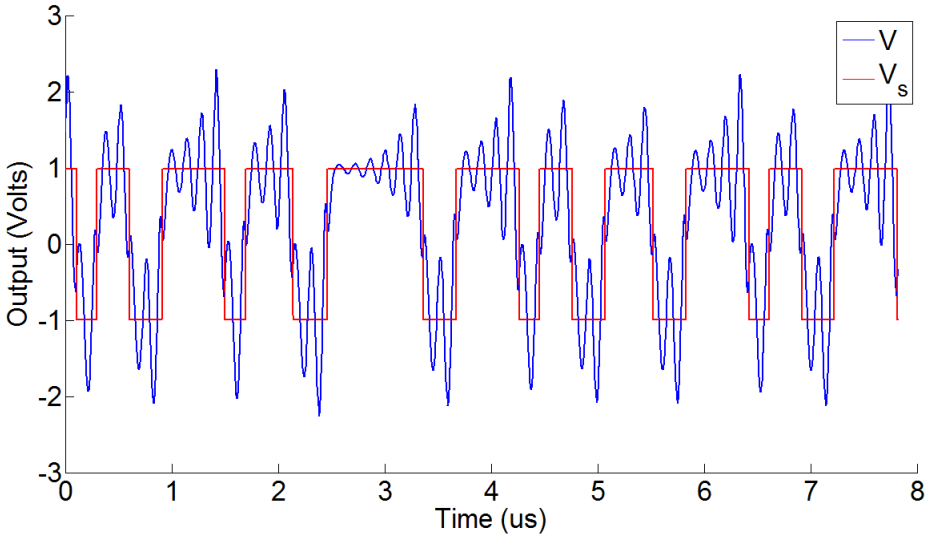

Figure 4.5: Time domain response of the voltage nodes V and V_s, where the fundamental frequency is 7.8MHz.

4.2 Forced Nonlinear Transistor Circuit Simulations

In order to provide more insight into how the BJT circuit works, a mathematical model was derived. If the nonlinear transistor circuit is modeled using traditional small signal techniques, the resulting system would not exhibit chaos. For the circuit to oscillate in a chaotic manner, both the forward and reverse active regions must be included in the model. Most of the small signal models for an NPN transistor are only intended to be used for the forward active region; however, the Ebers-Moll model does describe both of these regions [105]. This model consists of two ideal diodes and two ideal voltage-dependent current sources, as shown in the schematic of Fig. 4.9, where the NPN transistor is replaced with its Ebers-Moll equivalent model. In the forward active region, the diode D2 is "off", which blocks the current from IAF, and D1 is "on". This means that all of the current flows from the dependent source IAR and through D1. Similarly, in the reverse active region, D1 is "off", which blocks the current from IAR, and D2 is "on". This means that all of the current from the dependent source IAF flows through D2. Using nodal analysis, the three equations can be written as

$$\frac{v_1(t)-V_f}{R_1} + c_1(\dot{v}_1(t) - \dot{v}_c(t)) \quad = 0 \tag{4.2}$$

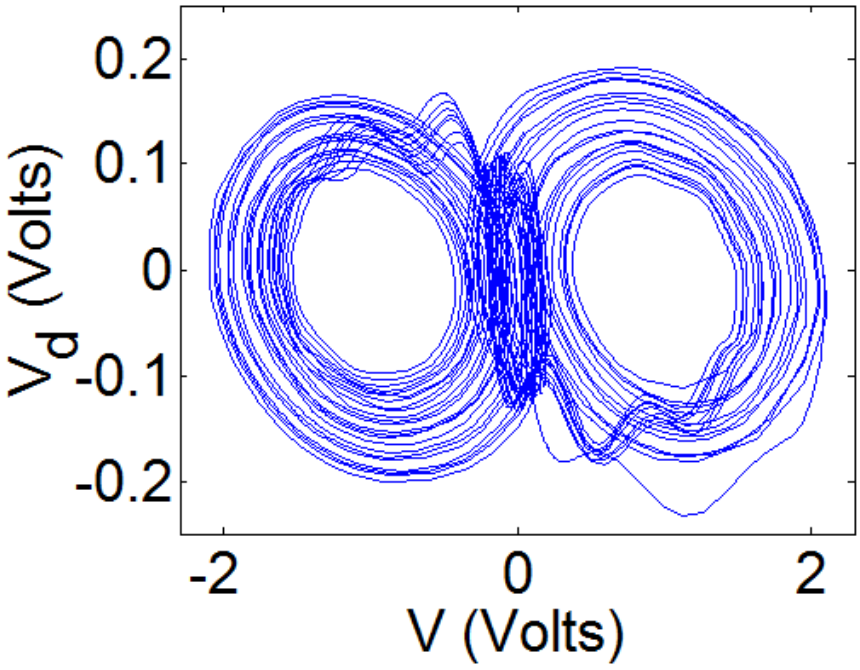

Figure 4.6: Shift map generated from the continuous timed waveform from voltage node V, where the fundamental frequency is 7.8MHz.

$$c_1(\dot{v}_c(t) - \dot{v}_1(t)) + \frac{(v_c(t) - v_b(t))}{R_2} = \quad i_R - IAF \tag{4.3}$$

$$\frac{v_b(t) - v_c(t)}{R_2} + c_2\dot{v}_b(t) = \quad IAF + IAR - i_F - i_R \tag{4.4}$$

where currents are defined as

$$i_F = I_{ES}(e^{\frac{v_b(t)}{v_T}} - 1) \tag{4.5}$$

$$i_R = I_{CS}(e^{\frac{v_b(t) - v_c(t)}{v_T}} - 1) \tag{4.6}$$

$$IAF = \alpha_F i_F \tag{4.7}$$

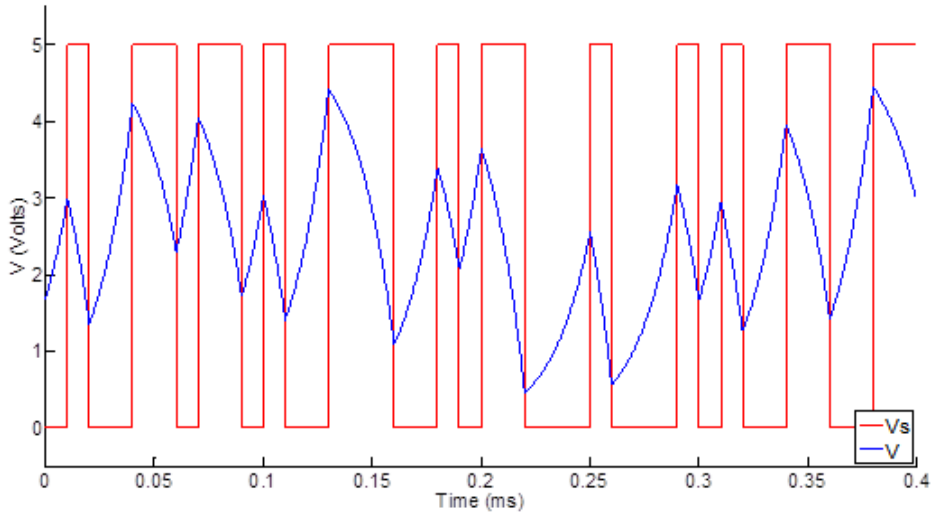

Figure 4.7: Time domain response of the voltage nodes V and V_s.

Parameter	Value	Units
V_T	25.85	mV
R_1	0.1	Ω
R_2	4.7	kΩ
C_1	150	pF
C_2	150	pF
α_F	0.9973	A/A
α_R	0.5	A/A
I_s	0.1434	pA
a	3.4	V

Table 4.1: Table of the parameters used in the numerical simulation of equations (4.2)-(4.4).

$$IAR = \alpha_R i_R \tag{4.8}$$

In these equations, the nodes are labeled as v_1, v_b, and v_c, which are, respectively, the voltage between R1 and C1, the base voltage, and the collector voltage. The circuit parameters used for the numerical simulation can be found in table 4.1. The forcing function voltage node is defined as $v_f = a\sin(\omega t)$ where the amplitude of the forcing function is a and the forcing frequency is ω. The unknown currents are defined as $I_{ES} = \frac{I_S}{\alpha_F}$ and $I_{CS} = \frac{I_S}{\alpha_R}$. Here, α_F is the forward short-circuit current gain, α_R is the reverse current gain, and I_S is the transistor's reverse saturation current for the Ebers-Moll model. Similarly, the base to emitter voltage simplifies to be just the base voltage, defined as $v_{BE}(t) = v_b(t)$. The base to collector

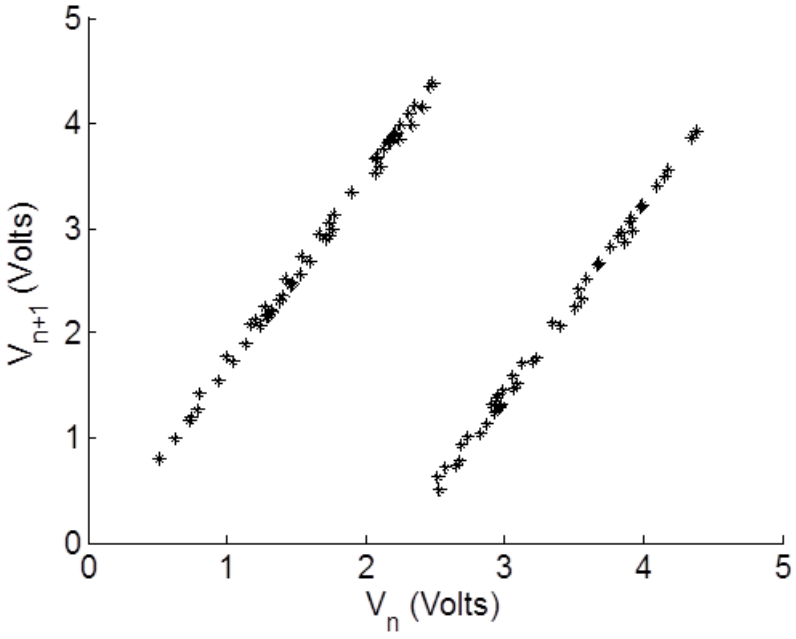

Figure 4.8: Shift map generated from the continuous timed waveform from voltage node V.

voltage, $v_{BC}(t)$, is the difference between the base voltage and collector voltage, defined a $v_{BC}(t) = v_b(t) - v_c(t)$. Together, (4.2)-(4.4) describe both the forward active region and the reverse active region of the circuit schematic shown in Fig. 4.9.

The numerical simulations of the time domain and phase space responses using equations (4.2)-(4.4) are in good agreement with the SPICE and hardware results when compared to the low frequency prototype previously demonstrated [6, 7]. The time domain plot of the transistor's base voltage, when undergoing periodic motion, is shown in Fig. 4.10a with a period-4 solution. The phase space of periodic motion of the base voltage versus the forcing function can be seen in Fig. 4.10b. The time domain of the transistor's base voltage shows transitions between the forward active region, when the forcing frequency is increased. Each time the transistor enters the reverse active region, V_b becomes negative. This occurs at an aperiodic interval. This can be seen in the chaotic time domain response in Fig. 4.10c and in the phase space of the base voltage versus the forcing function in Fig. 4.10d.

The nonlinear transistor circuit demonstrates both periodic and chaotic motion, depending on the amplitude and frequency of the forcing function, $V_f = a\ sin(\omega t)$. In order to illustrate that the Ebers-Moll model includes both the forward and reverse active regions of the transistor,

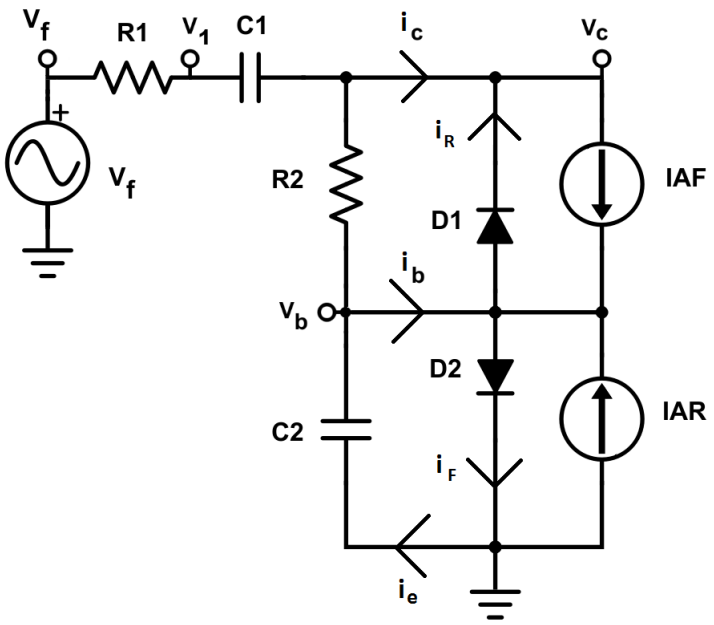

Figure 4.9: Schematic of the single transistor circuit using the Ebers-Moll model for an NPN BJT.

bifurcation diagrams were calculated by separately varying the amplitude and frequency. By varying the forcing amplitude from 0 V to 10 V and finding the Poincaré sections for the base voltage, the bifurcation diagram for the system was constructed, which is shown in Fig. 4.11. Similarly, by varying the forcing frequency from 10 Hz to 6 kHz and finding the Poincaré sections for the base voltage, the bifurcation diagram for the system was constructed, which is shown in Fig. 4.12. For each bifurcation diagram, the forcing frequency was used as the clock frequency to find the Poincaré sections of the base voltage.

The circuit from Fig. 3.8 was tested using SPICE simulation software. The op-amp used for both the twin-T oscillator and the variable gain stage was the LT1818. This op-amp was chosen because of its high gain-bandwidth product (GBW) and reliable operation. Multiple transistors were found suitable for operation at lower frequencies; however, the 2N2857 was found to operate at higher frequencies while minimizing the distortion of the waveform. This transistor is a general purpose RF BJT that is often used in oscillators for communication and radar applications. A list of the other NPN BJTs tested for this circuit topology and the hardware results can be found in Table 4.2. This table includes the maximum collector-base voltage and collector current ratings for the parts, the type of package, and indicates if the BJTs

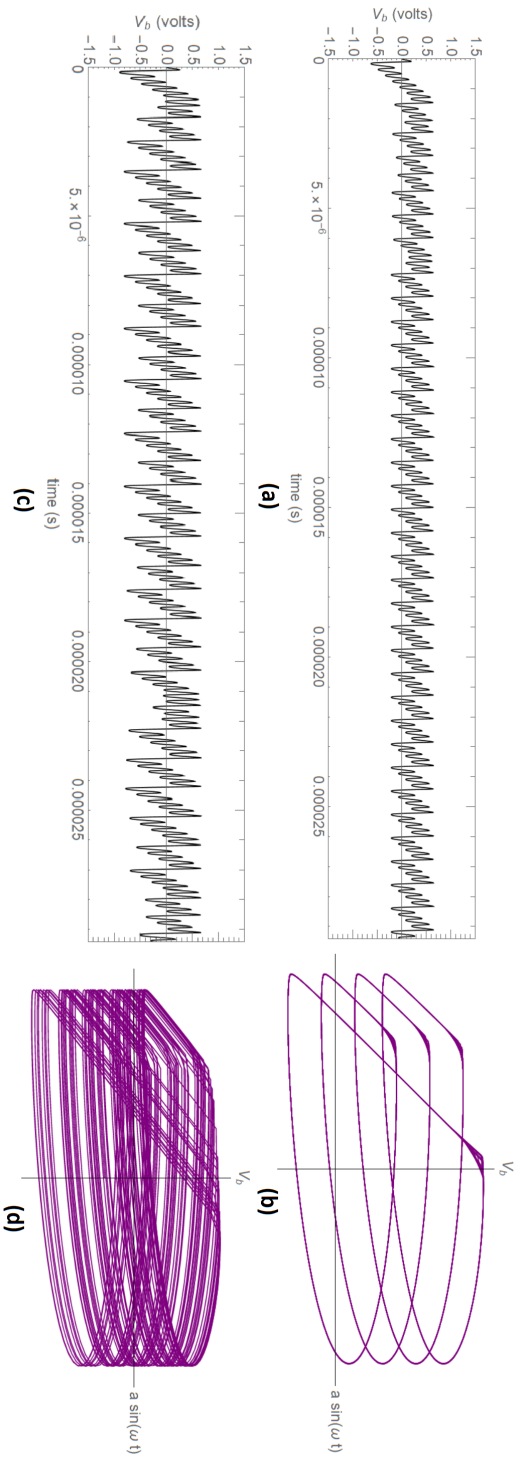

Figure 4.10: By solving equations (4.2)-(4.4) in Mathematica, the following responses were found. (a) Time domain response of period-4 orbit of the transistors base voltage, where the forcing function has parameters set as $a = 2.53$ V and $f = 5.1$ MHz. (b) Phase space of the period-4 orbit. (c) Time domain response of chaotic orbit of the transistors base voltage, where the forcing function has parameters set as $a = 3.4$ V and $f = 5.1$ MHz. (d) Phase space of the chaotic orbit.

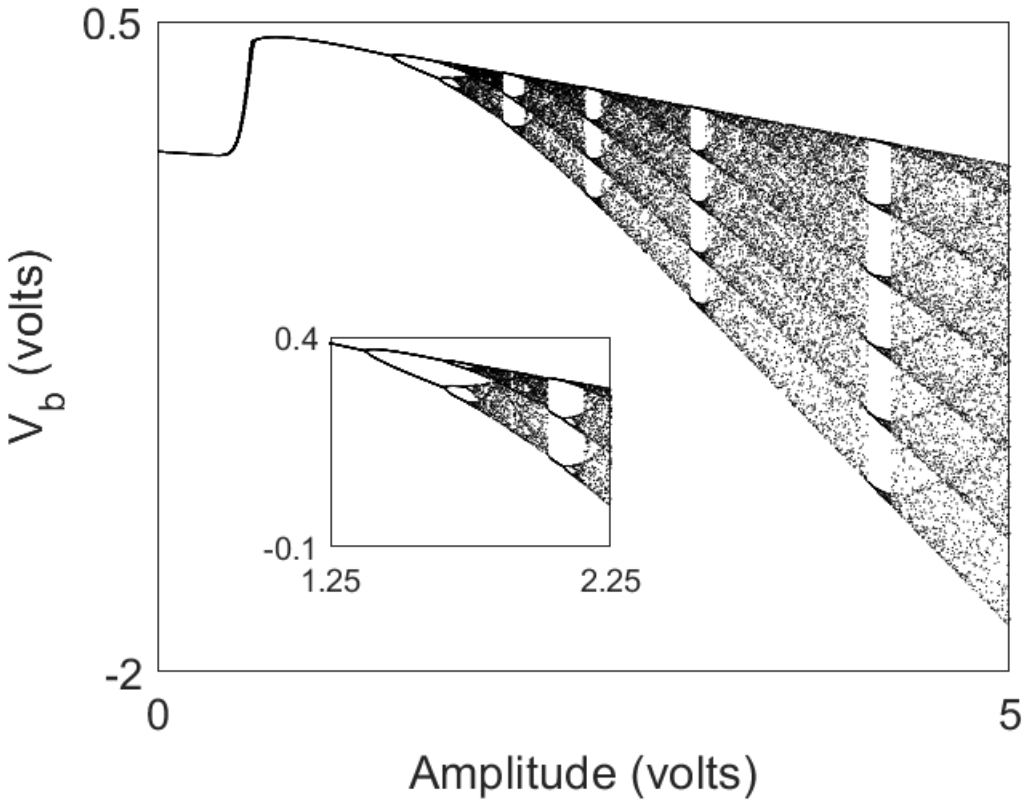

Figure 4.11: For the Ebers-Moll model (equations (4.2) - (4.4)), the bifurcation diagram was generated by varying the forcing amplitude and and finding the Poincaré sections of the base voltage. The frequency was held constant at 5.1 MHz. A period-3 region is presented in the inset figure.

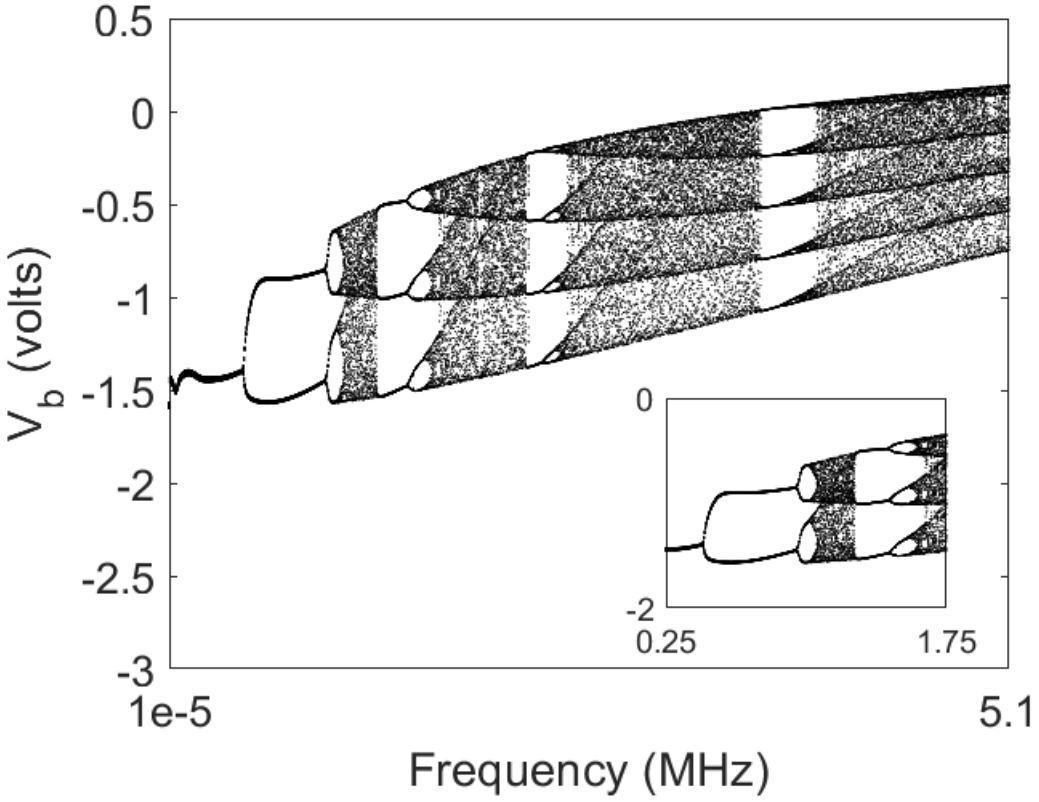

Figure 4.12: For the Ebers-Moll model (equations (4.2) - (4.4)), the bifurcation diagram was generated by varying the forcing frequency and finding the Poincaré sections of the base voltage. The amplitude was held constant at 3.40 V. A period-3 region is presented in the inset figure.

BJT Part No.	V_{max} (V)	I_{max} (mA)	Package	Oscillate?
2N5089	25	50	TO-92	Yes
2N2369A	15	200	TO-18	Yes
2SC3837	11	50	SOT-346	No
2SC3838	11	50	SOT-346	No
2N2857	15	40	TO-72	Yes
2N2369A	15	200	TO-18	Yes
2N708	0.5	10	TO-18	No
MMB2369A	15	200	SOT-23	No
MMB2222	40	600	SOT-23	No
CMP2369	15	500	SOT-23	No
2N5179	12	50	TO-72	No
PN2369A	40	100	TO-92	No

Table 4.2: Table of the parameters used in the numerical simulation of equations (4.2)-(4.4).

oscillated or not. The surface mound devices were tested on the breadboard using a breakout board.

There are a few node voltages and currents from the transistor that are of interest in the nonlinear transistor circuit. One of these is the transistor's base voltage. Time domain simulation results can be seen in Fig. 4.13 where the fundamental frequency of the oscillation is approximately 700 kHz. This waveform best depicts how the two integration constants are interfering with each other in the transistor circuit. The waveform tends to "reset" itself after an unpredictable amount of time. This can also be seen in the large current spikes in the collector current of the transistor, as shown in Fig. 4.14.

Another voltage node is the linear forcing function that is generated by this circuit. This is best shown when plotted in a phase space of the forcing function versus the base voltage, shown in Fig. 4.15. This particular phase space is a demonstration of topological mixing represented in only 2 dimensions in the nonlinear transistor circuit. Another phase space can be seen in the plots of the collector voltage versus the collector current shown in Fig. 4.16.

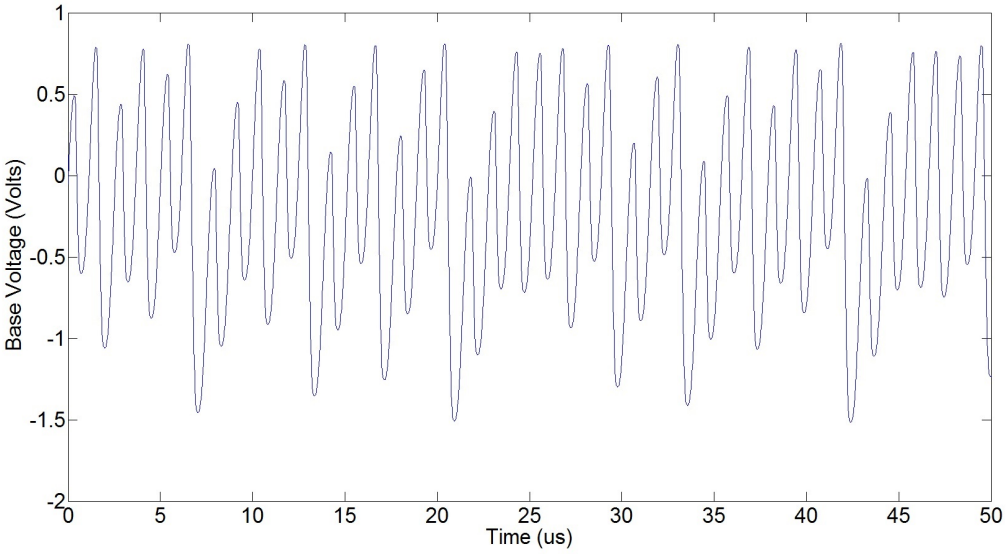

Figure 4.13: Time domain plot of the transistor's base voltage

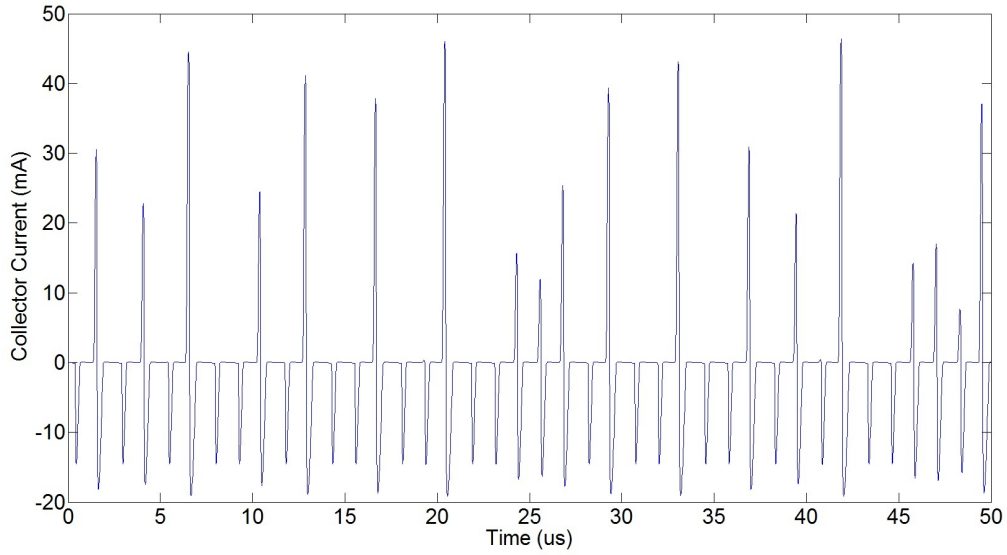

Figure 4.14: Time domain plot of the transistor's collector current

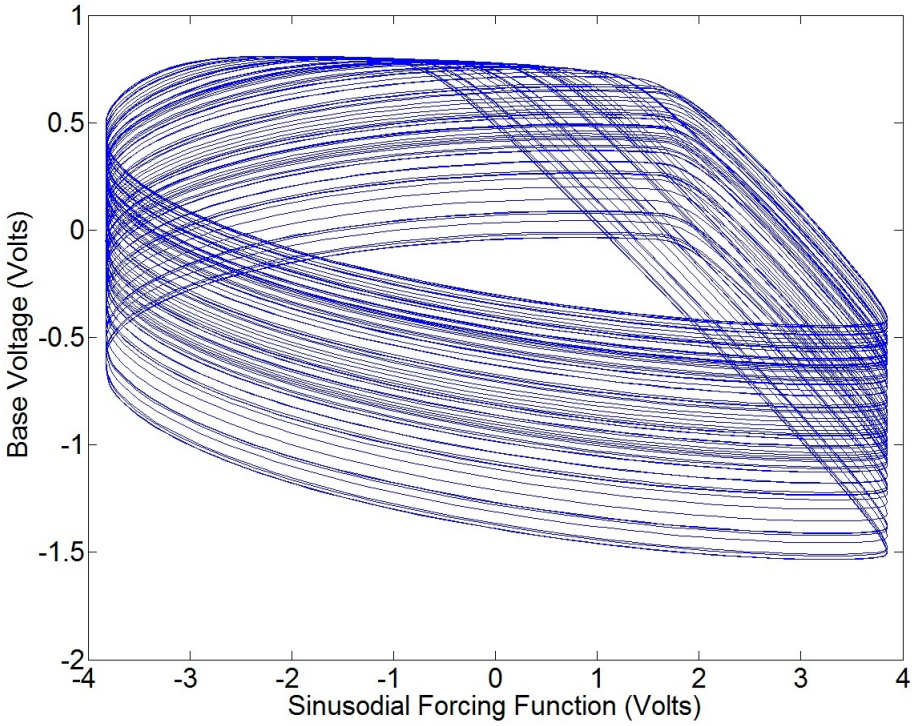

Figure 4.15: Phase space plot of the the linear forcing function vs. the transistor's base voltage

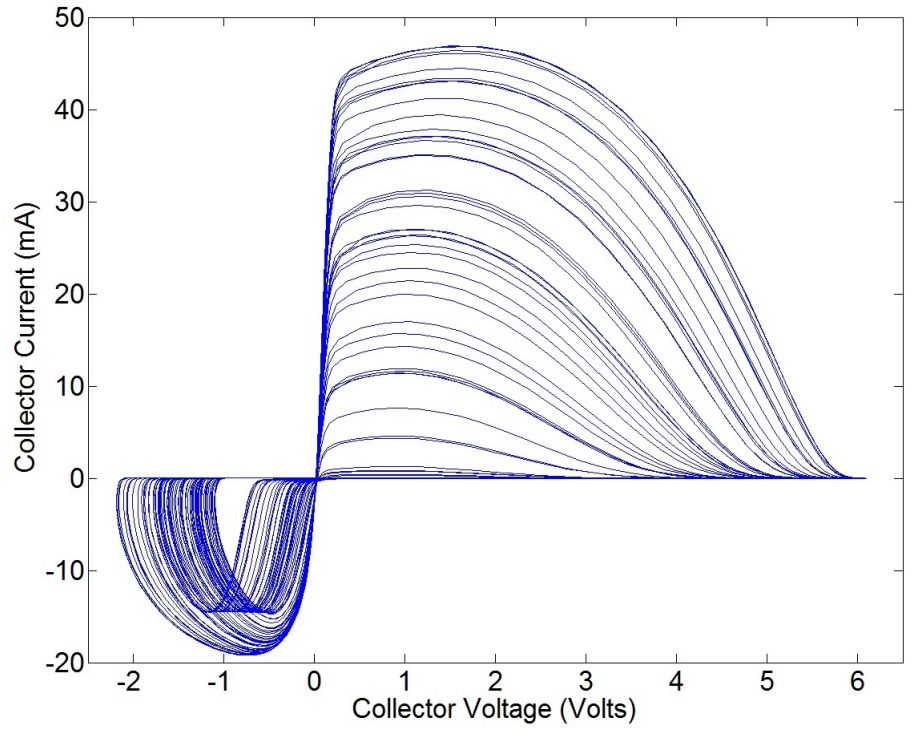

Figure 4.16: Phase space plot of the transistor's collector voltage vs. the collector current

Chapter 5

Hardware Results

The simulation schematics were realized in hardware on PCBs using the computer aided design tool called KiCAD. Some of these PCBs were manufactured by Advanced Circuits; however, a majority of them were manufactured by OSH Park. Multiple testing points were included in each of the designs for troubleshooting any problems in the hardware. Each of these designs went through multiple design iterations. For some of the designs, the static resistors were replaced with potentiometers in order to tune the chaotic oscillators.

5.1 Exactly Solvable PCB Design

Both of the exactly solvable PCBs were designed using KiCAD. These custom designs were intended to be used with COTS op-amps, comparators, digital logic, and 0805 passive resistors and capacitors.

5.1.1 Second-Order Filter

A proof of concept of the oscillator has been implemented in hardware. This design was implemented using COTS parts and a custom PCB designed to operate at 18.4 kHz. Careful consideration went into the PCB design for the mixed-signal oscillator design, as seen in Fig. 5.1. This prototype includes multiple testing components, buffers, an output voltage level shifting circuit, and a 50Ω matching network for an SMA connection. The components were placed in a roughly circular path to minimize the trace length required to complete the feedback loop. A four layer board was constructed where almost all the traces were on the top copper layer to further minimize the trace lengths to reduce the use of vias for the signal lines.

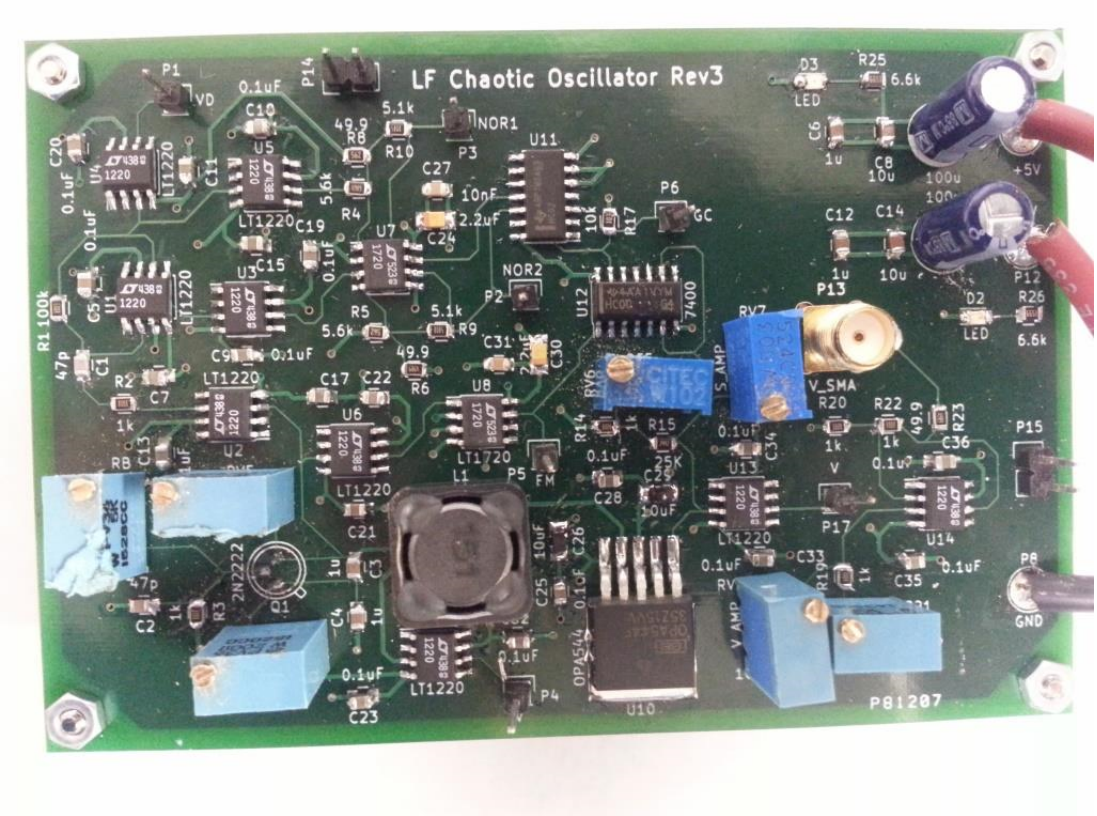

Figure 5.1: Photograph of the populated PCB of the chaotic oscillator.

The remaining three layers were used for power and ground planes. The second layer, which is directly below the top copper trace layer, was a ground plane to provide isolation from the third layer which contained the positive and negative power rails. The fourth and bottom layer was another ground plane to further isolate the power rails. The two ground planes were used to reduce interference by isolating the devices and signal traces from the power planes. The ground planes isolate the high speed comparators to minimize false triggers caused by noise or external signals. Trimmer potentiometers were used for the common-base biasing resistors to reduce the tolerance required on the parts. This addition to the board eliminated the oscillator's sensitivity to thermal effects because they could be manually nulled.

The time domain results of the hardware can be seen in Fig. 5.2 with the output of the oscillator (yellow), the derivative signal (green), and the feedback signal, V_s (blue). Plotting the oscillator's output versus its derivative results in the phase space plot found in Fig. 5.3. This plot demonstrates that the mixed-signal shift band chaotic oscillator design exhibits thick solution bands, an indication of the chaotic characteristic of topological mixing. A plot of

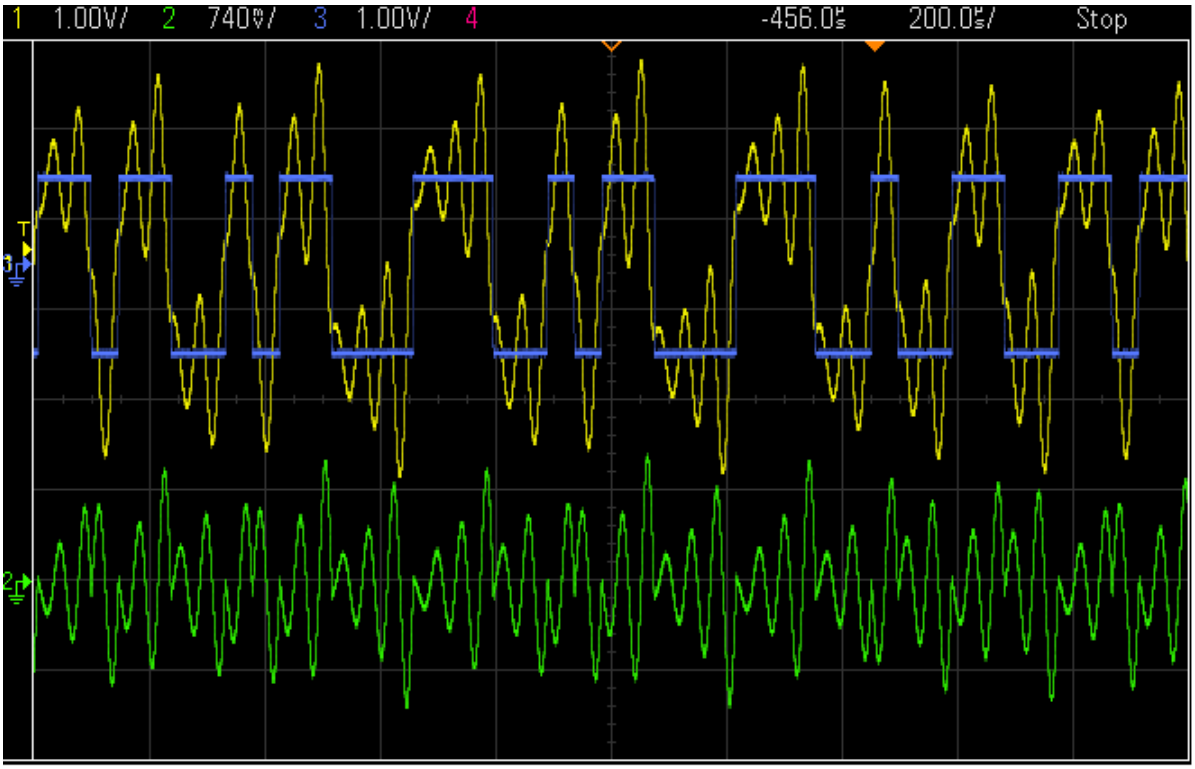

Figure 5.2: Time domain results of the oscillator measured by an oscilloscope (Yellow: Output, Blue: feedback signal V_s, Green: Derivative of output.)

the successive local maxima of the time domain data results are shown in Fig. 5.4. The code to generate the shift map from hardware data can be found in Appendix B and Appendix C. All three of the hardware results in Fig. 5.2-5.4 are in agreement with the original system's dynamics and simulations.

Since this system has an exact analytical solution, the hardware matched filter was developed [91]. For this reason, this system was developed as a communication system. The system overview for this implementation can be seen in Fig. 5.5. This communication system was configured to transmit ASCII characters entered in via a computer keyboard or saved in a text document over a wireless channel to be received by another computer on the other side of the room that communcates with a microcontroller over a serial connection. This information was encoded by a microcontroler into the exactly solvable chaotic oscillator with the help of an analog controller [74].

The control technique used for this implementation is called proportional feedback control [74]. Two of the desired outputs of the waveforms were saved on the microcontroller

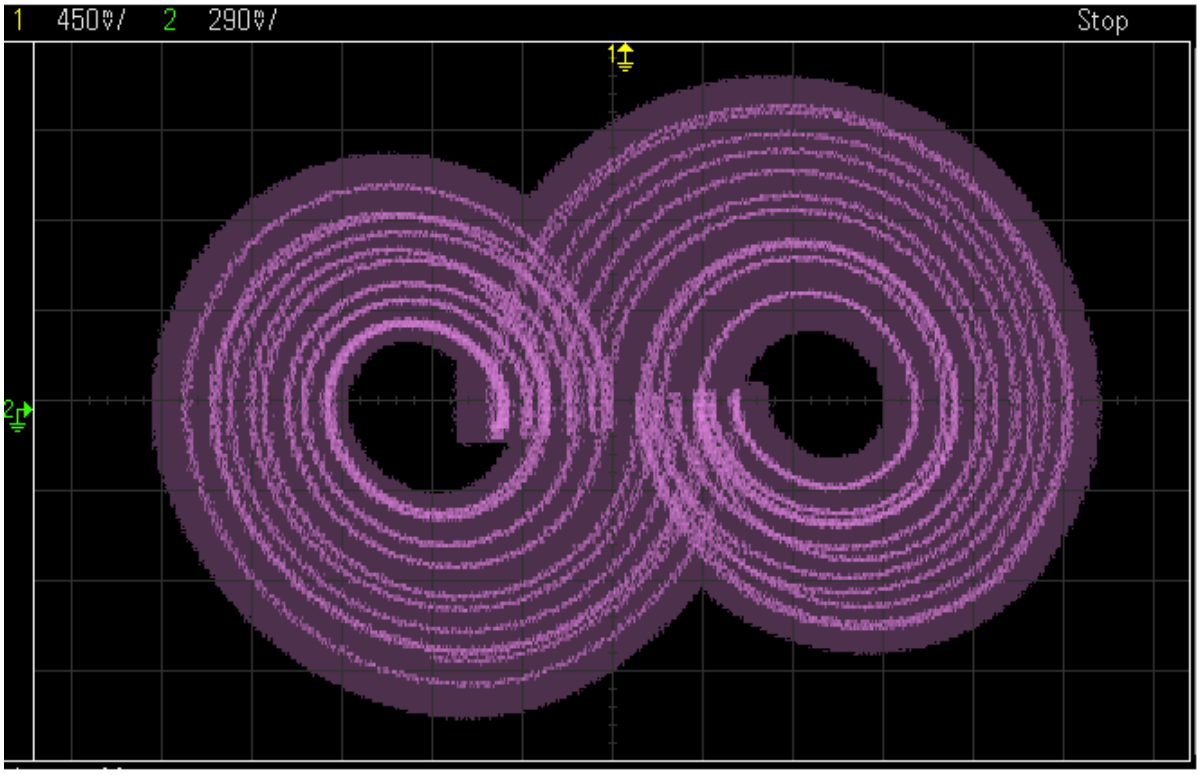

Figure 5.3: Phase space of the electronic oscillator measured by an oscilloscope.

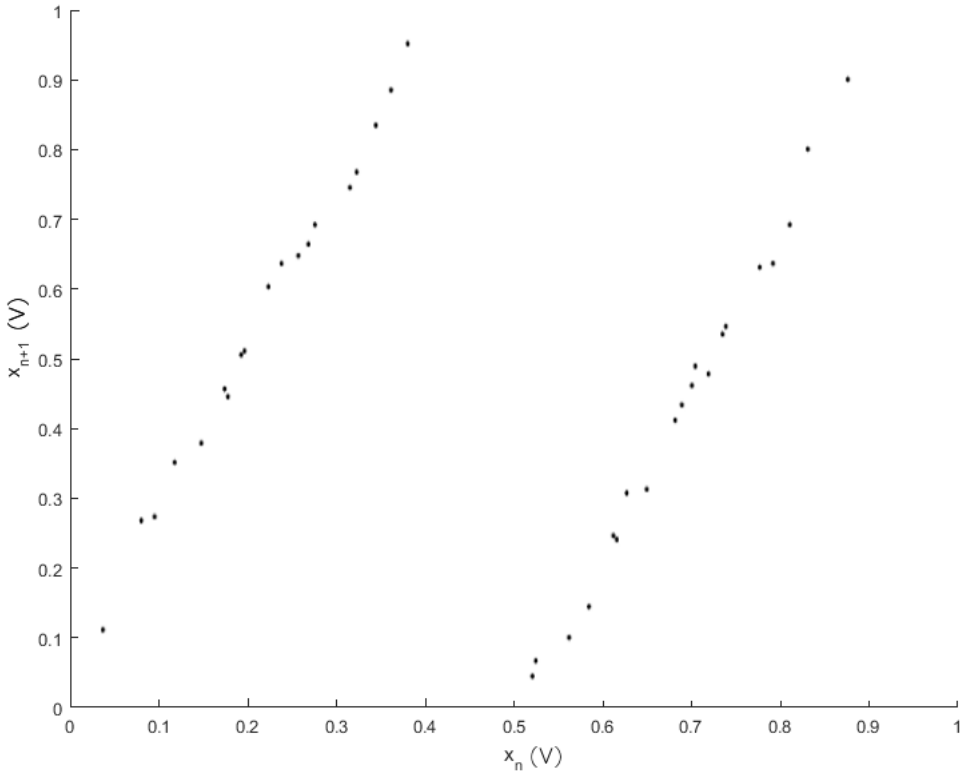

Figure 5.4: Plot of the local successive maxima of the oscillator from the measured data from the hardware.

in a lookup table. These two desired waveforms are then compared with the current state of the oscillator using an analog controller. The difference between these signals determines the magnitude of the control effort. The control effort is applied by using small aperodic voltage perturbations in order to steer the trajectory to the desired one. The time at which the voltage perturbations are applied is determined by the analog controller. The analog controller takes the derivative signal off the oscillator board and determines when there is a zero crossing of the derivative signal. At each zero crossing, the control effort is applied.

This signal is modulated using a commercial FM transmitter, and received by a commercial FM receiver and processed by a custom matched filter, and decoded by a microcontroller [91]. A software version of this matched filter was also developed [106]. This message is then transmitted over a serial connection and displayed on a computer monitor. An example of the encoding scheme can be seen in the waveforms depicted in Fig 5.6. Here, the green waveform is the information to be encoded into the oscillator waveform, the yellow waveform is the output of the oscillator with the information encoded, the purple waveform is the output of the matched filter, and the blue waveform is the decoded information sent from the microcontroller to the displaying computer.

Note that the fundamental frequency of the chaotic oscillator used was approximately 18.9 kHz. This low frequency version of the oscillator did limit the data rate at which the system could transmit; however, the lower operating frequency of this design was required for the information to be reliably encoded into the waveform. The propagation delay through the feedback paths need to be significantly shorter than the period of the fundamental frequency of the oscillator in order for the controller to work.

The matched filter for this system also means that it is a candidate choice for use in radar system applications as well [91]. This was demonstrated using a previously developed version of the same system [52]. One of the fundamental differences between this design and the one presented in this work is that the previous oscillator used an op-amp based negative impedance converter. That system's fundamental frequency was approximently 1.8 MHz, which was too high to use with the proportional feedback control scheme [74]. However, this oscillator design is still suitable for radar applications because there is no need to encode information into the

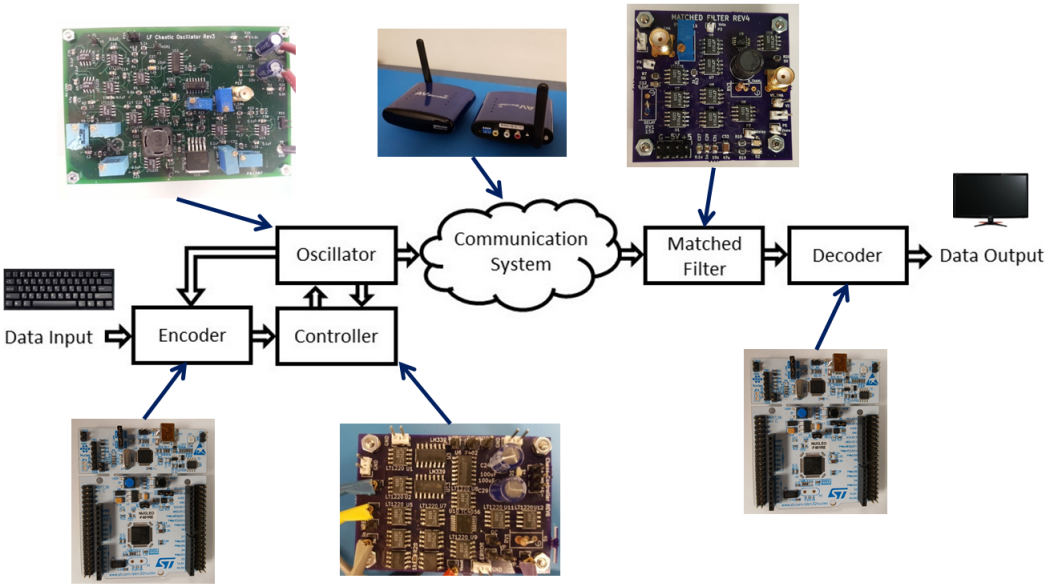

Figure 5.5: Overview of the the communication system.

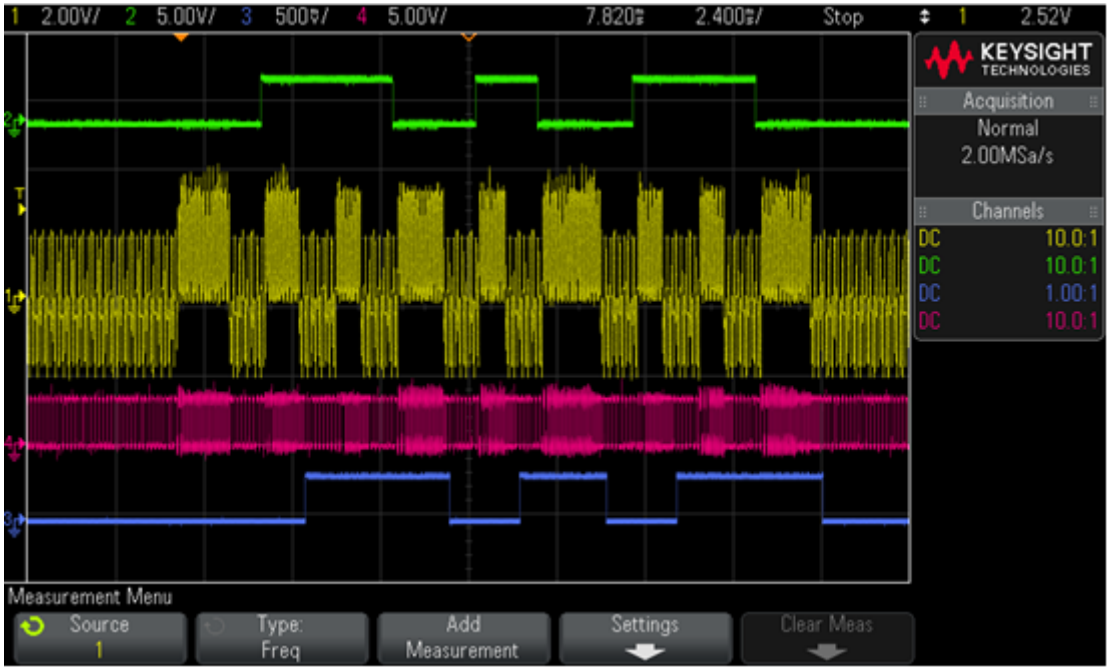

Figure 5.6: Oscilloscope capture of the communication system's input and outputs. Here the green waveform is the information to be encoded into the oscillator waveform, the yellow waveform is the output of the oscillator with the information encoded, the purple waveform is the output of the matched filter, and the blue waveform is the decoded information sent from the microcontroller to the displaying computer..

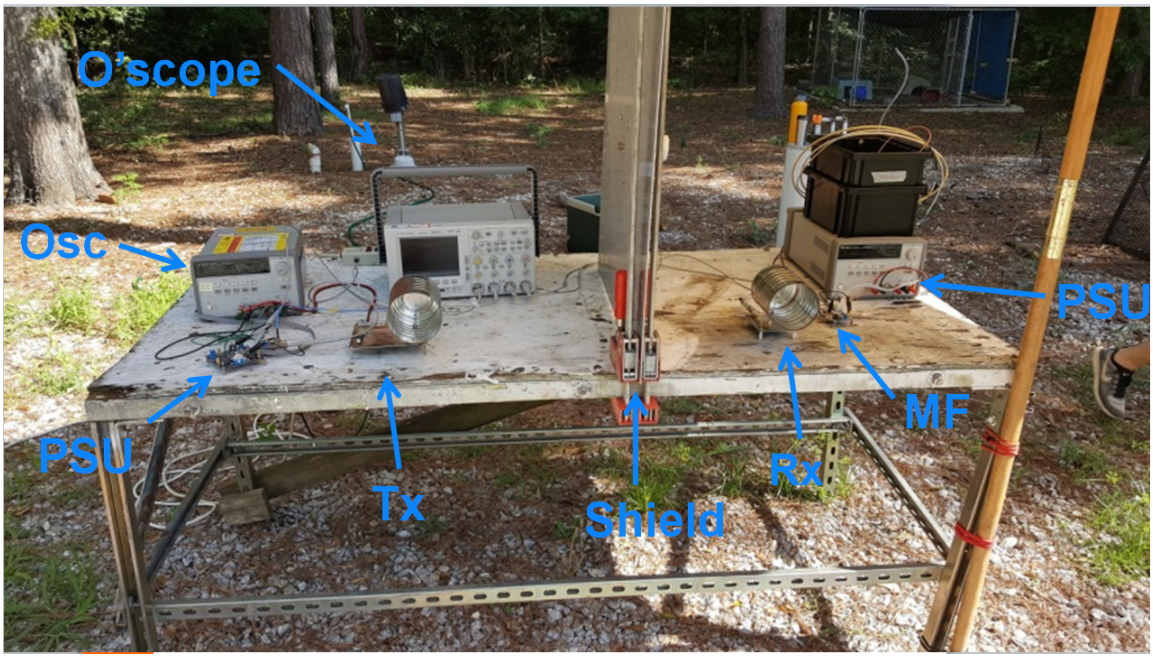

Figure 5.7: Hardware demonstration of the chaos based radar where the oscilloscope (O'scope), chaotic oscillator (osc), power supplies (PSU), RF transmitting circuitry (Tx), RF receiving circuitry (Rx), and the matched filter (MF) are marked. A large metal plate was used to shield (Shield) the transmitting and receiving circuitry.

system. Instead, the oscillator can be left to free run and the transmitted and received waveforms can be saved and compared in order to determine the delay between the two waveforms.

Using this system in a radar application has been shown to be effective in field tests, as shown in Fig. 5.7. Using directional tin-can antennas and COTS parts to create an amplitude modulated (AM) communication system, this system was used in a radar demonstration. The transmitting and receiving circuitry was isolated using a large metal plate and the target used was the back of a sports utility vehicle. Data was collected over three different runs and shows a somewhat linear response, as seen in Fig. 5.8. These results are in agreement with the measured distances of the car from the test bench.

5.1.2 First-Order Filter

A low frequency prototype on a custom PCB of the first-order system was constructed using COTS parts, as shown in Fig. 5.9 and Fig. 5.10. The PCB measures approximately 3 cm by 4 cm and includes multiple testing points. A potentiometer was used for resistor R4 from Fig. 3.7 so that the gain of the NIC stage could be tuned to the appropriate value to achieve

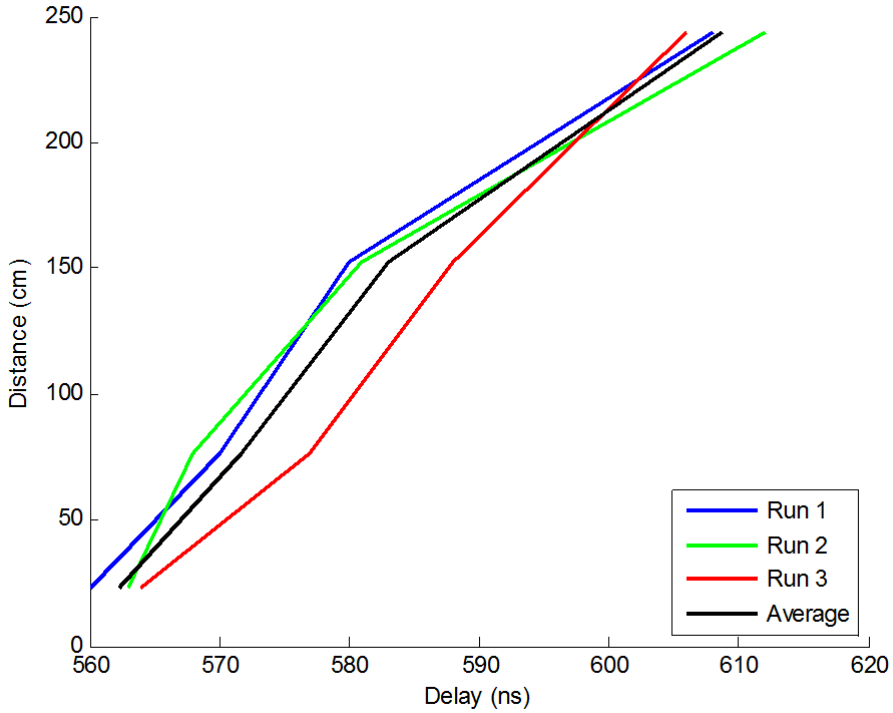

Figure 5.8: Plot of the results from the chaos radar demonstration.

both chaotic and periodic responses. Since these chaotic systems have an extreme sensitivity to initial conditions, the oscillator can be greatly affected by the environment it operates in. Small changes in things such as the ambient temperature can cause the system to not operate as expected.

The circuit only required three active ICs. A hex inverter (SN7404N) was used to provide the four inverting stages. The remaining inputs to the two unused inverters were grounded to mitigate the affects of noise on the other inverters. The outputs of the unused inverters were left unconnected. The D flip-flops' chosen was the MC14175B which is a quad package. Similarly to the inverters, the unused flip-flops inputs were grounded and the outputs were left unconnected. The op–amp used for the NIC was the LT1220. This op-amp operates off of $\pm$15V power rails, while the two digital components operated off a single sided 5V power supply. The resulting waveforms for the voltage nodes V and V_s are shown in Fig. 5.11.

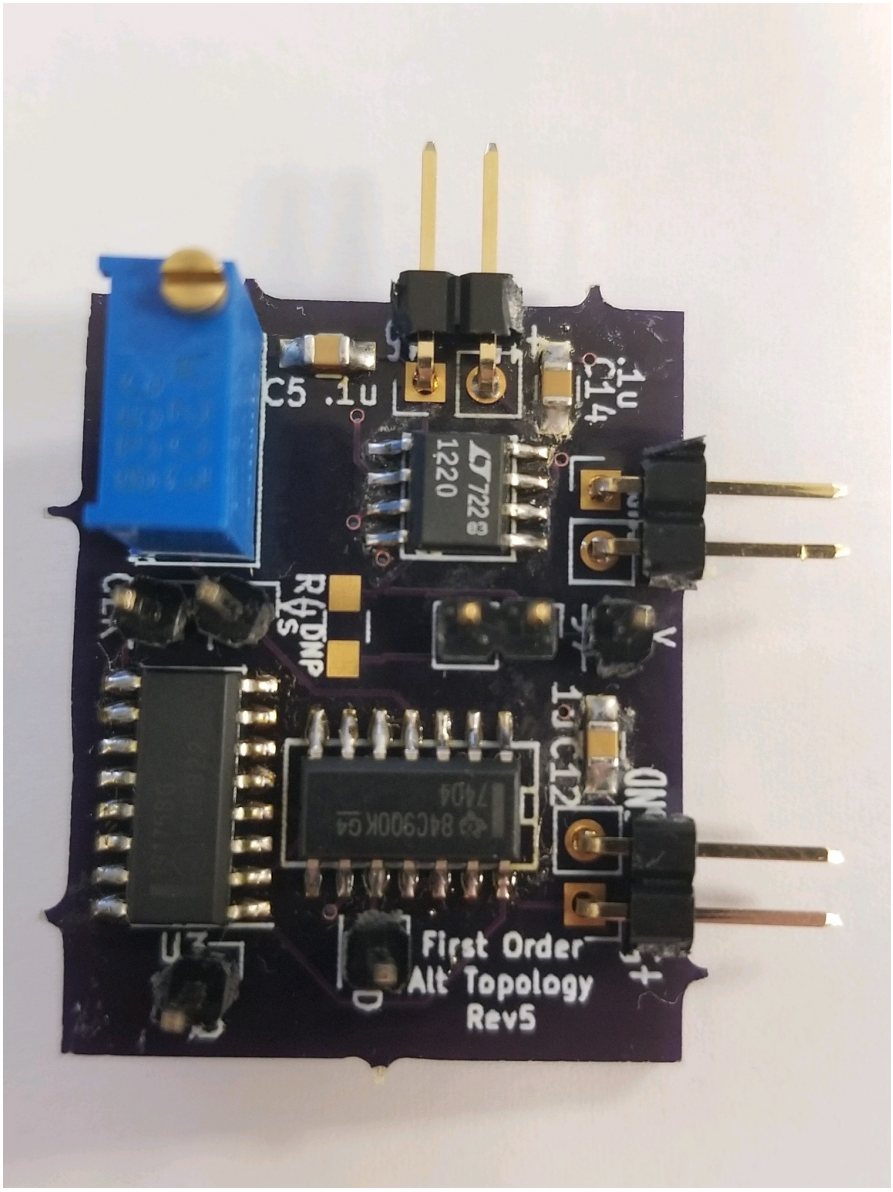

Figure 5.9: Front of the PCB of the first-order system.

5.2 Forced Nonlinear Transistor Breadboard Prototype

Before a PCB of the nonlinear transistor oscillator was constructed, a hardware based investigation of the various NPN BJTs was explored, as shown in the schematic shown in Fig. 5.12. This was done in order to analyze the nonlinear transistor circuit independent of the twin-T sinusoidal forcing function previously simulated. In order to test a large number of transistors very quickly, the prototype was built on a breadboard, as shown in Fig. 5.13. In addition to testing multiple transistors, the resistor values for R1 and R2 and the capacitor values for C1 and C2 were varied. Initially, the values from the original paper were used to demonstrate what is

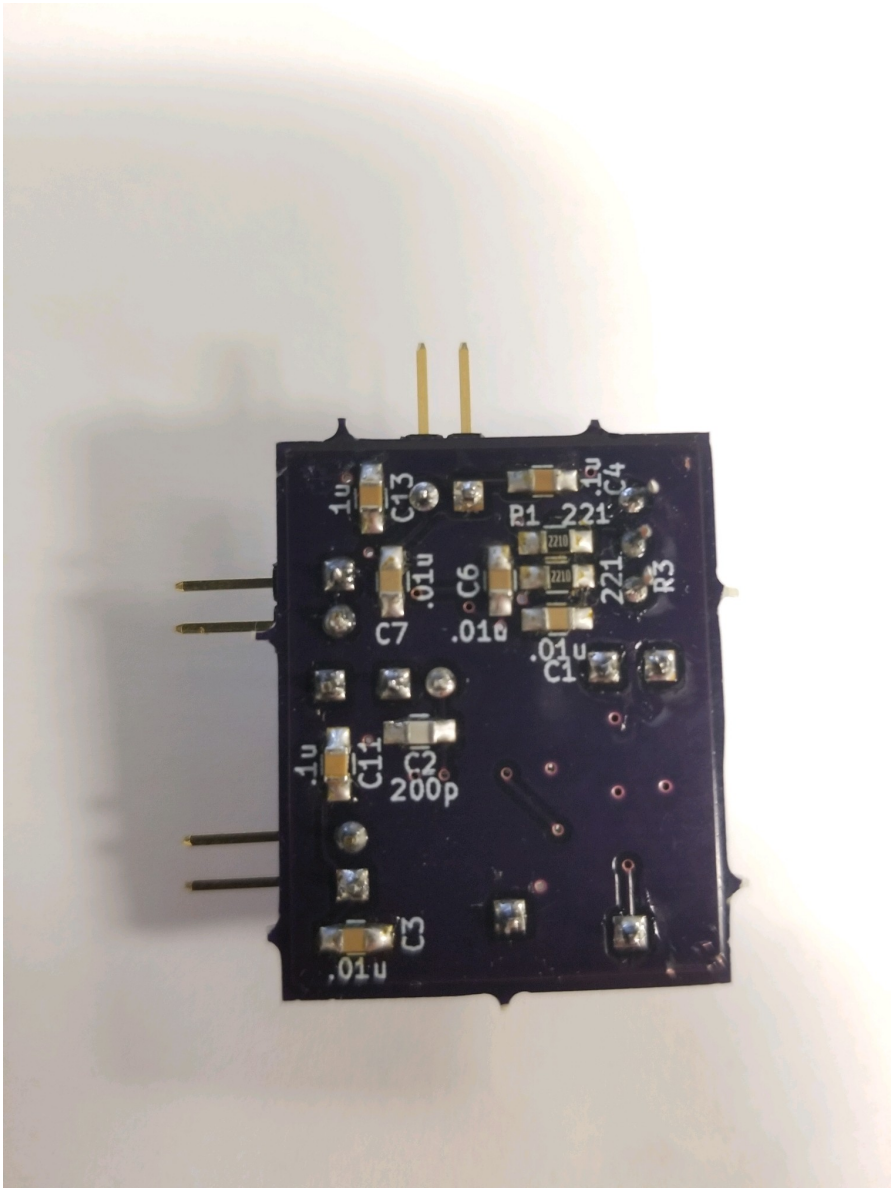

Figure 5.10: Back of the PCB of the first-order system.

to be expected from this system. Some of the through-hole transistors that were tested include the 2N2222, 2N5089, 2N3391A, 2N4401, and the 2N5210B. Of these transistors, the 2N2222 and the 2N5089 were determined to perform the best on the breadboard prototype.

The original transistor circuit was forced by a 2 kHz sinewave. Using the parameters given in the paper and the 2N5089 transistor, the time domain results can be seen in Fig. 5.14. Here, the green waveform is the voltage across the base of the transistor and the yellow waveform is the collector voltage. Note that the collector voltage is not the sinusoidal forcing function; however, it does demonstrate the nonlinear interactions between the two RC networks. The

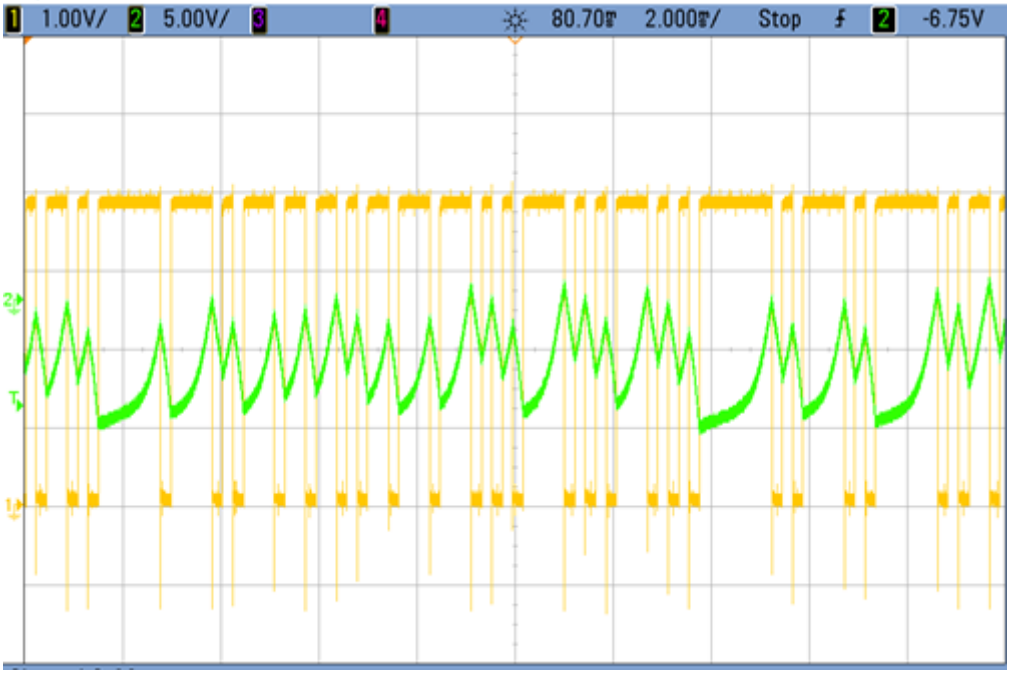

Figure 5.11: Hardware oscilloscope capture of the oscillator, where the voltage node V is in green and V_s is in yellow.

transistor's base voltage depicts how the transistor is resting on aperiodic intervals. Plotting the forcing function versus the base voltage results in the phase space shown in Fig. 5.15. Similarly, the phase space of the collector voltage versus the base voltage can be seen in Fig. 5.16.

Increasing the frequency of the function generator and a modifying the appropriate circuit parameters, the system can be pushed to oscillate over 1 MHz. In order to increase the frequency of the oscillations, the values for the capacitors needed to be lowered. An example of this is shown in Fig. 5.17, where the time domain plots of the collector voltage is in yellow the and base voltage is in green are shown using the 2N5089. In particular, the base voltage shows significant distortion when compared to the results in Fig. 5.14. Fig. 5.18 shows the phase portrait for the sinusoidal forcing function versus the transistor's base voltage and Fig. 5.19 shows the phase space for the transistor's collector voltage versus the base voltage. There is significant distortion in the phase portraits when compared to the phase space plots of the 2 kHz oscillations.

This design was tested again using the 2N2222 transistor to compare the performance difference. The time domain results for the collector voltage in yellow and the base voltage in green are shown in Fig. 5.20. The phase space for the sinusodial forcing function versus

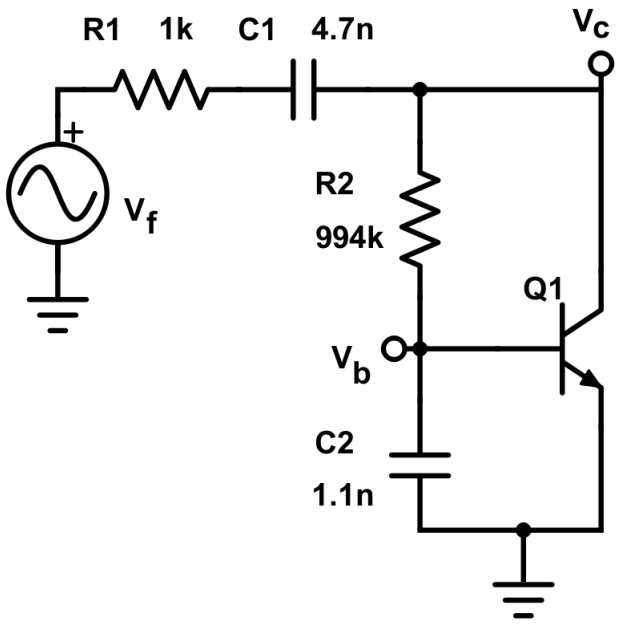

Figure 5.12: Schematic of the forced non-autonomous system.

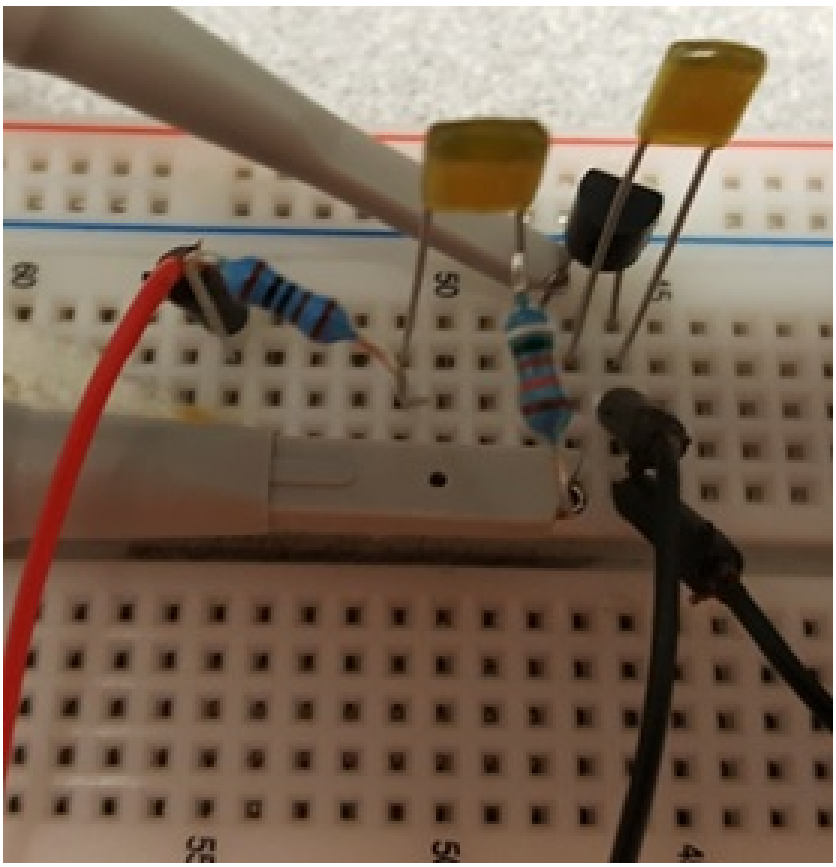

Figure 5.13: Breadboard of the forced oscillator using the 2N5089 driven by a table-top function generator.

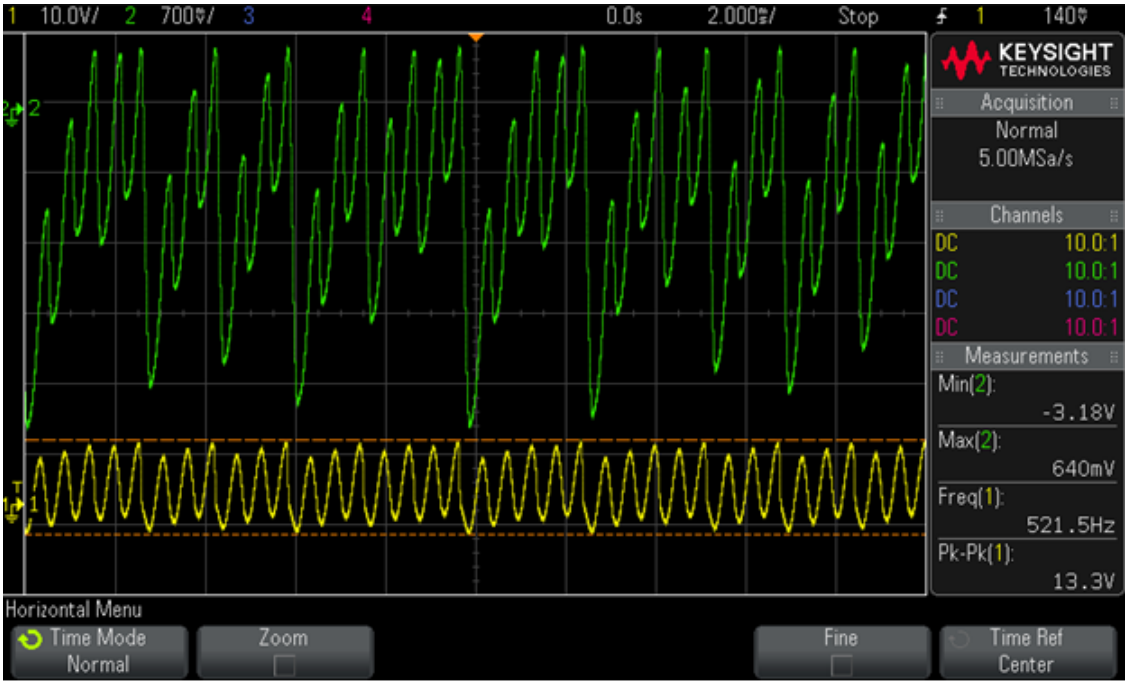

Figure 5.14: Time domain plot of the base voltage (green) and collector voltage (yellow) of the 2 kHz forced oscillator using the 2N5089.

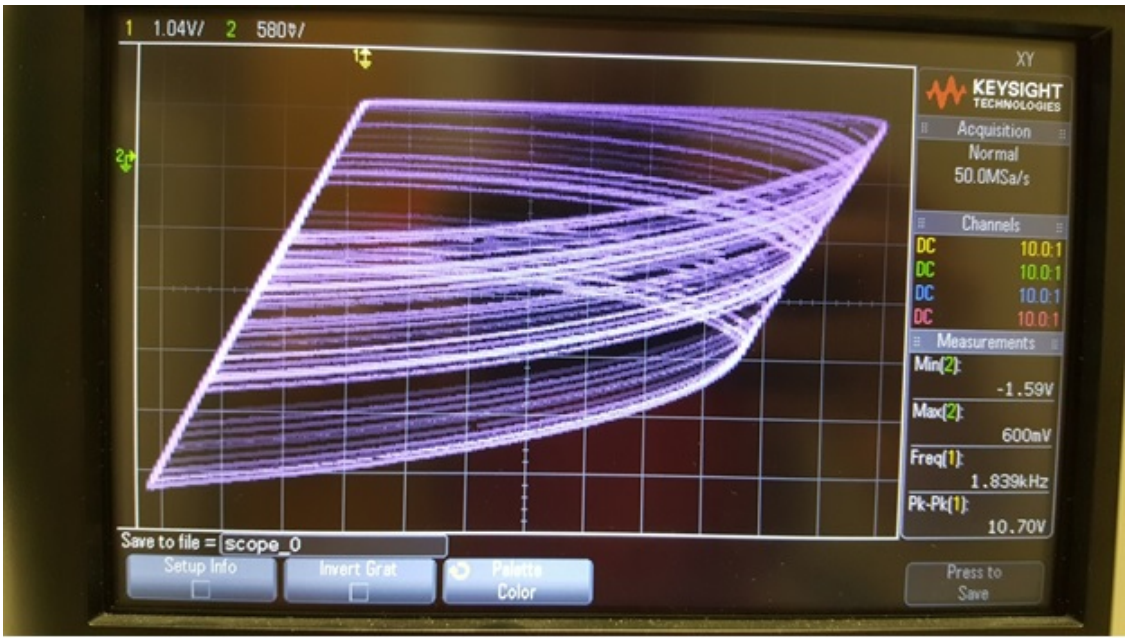

Figure 5.15: Phase space of the sinusoidal forcing function vs. base voltage of the 2 kHz oscillator using the 2N5089.

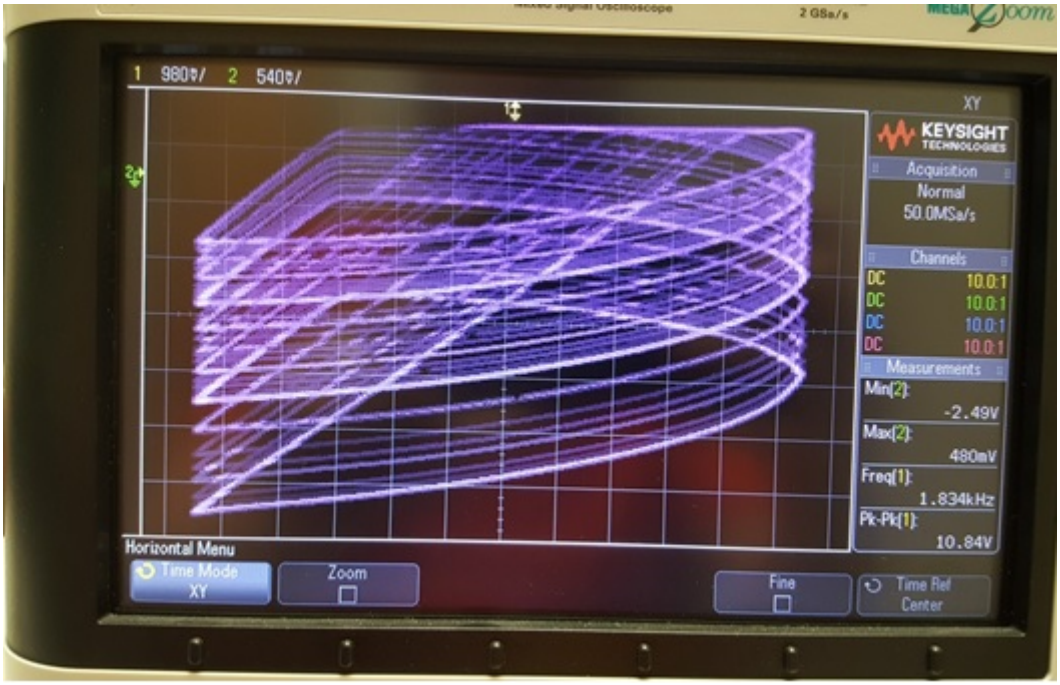

Figure 5.16: Phase space of the collector voltage vs. base voltage of the 2 kHz oscillator using the 2N5089.

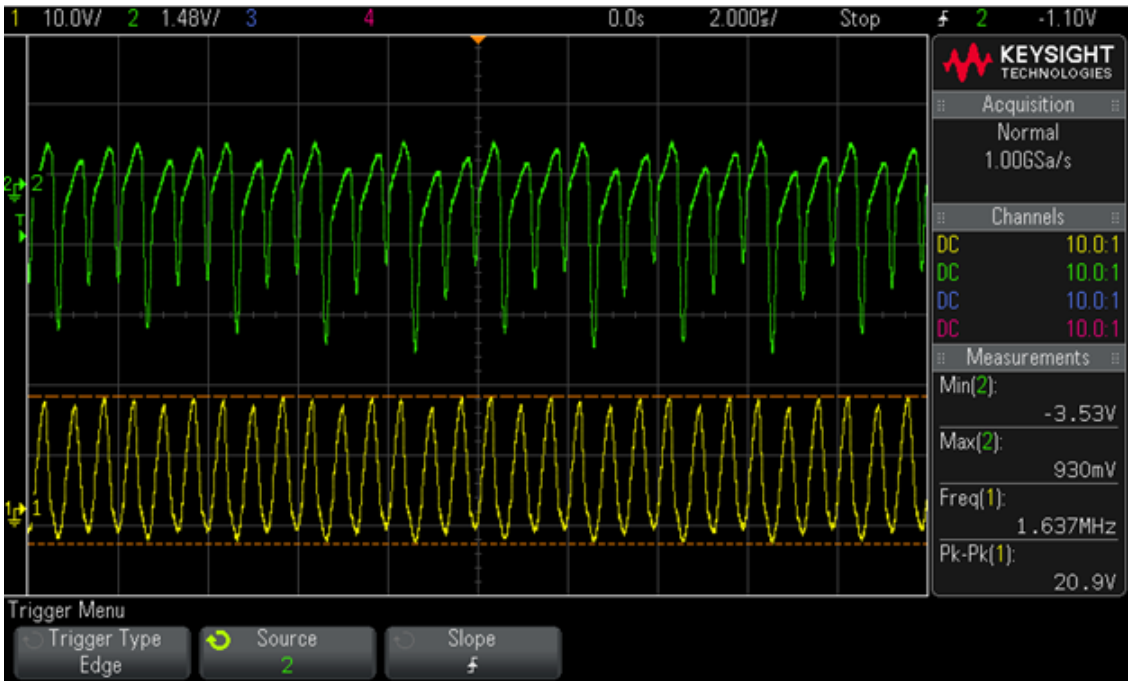

Figure 5.17: Time domain plot of the base voltage (green) and collector voltage (yellow) 1 MHz forced oscillator using the 2N5089.

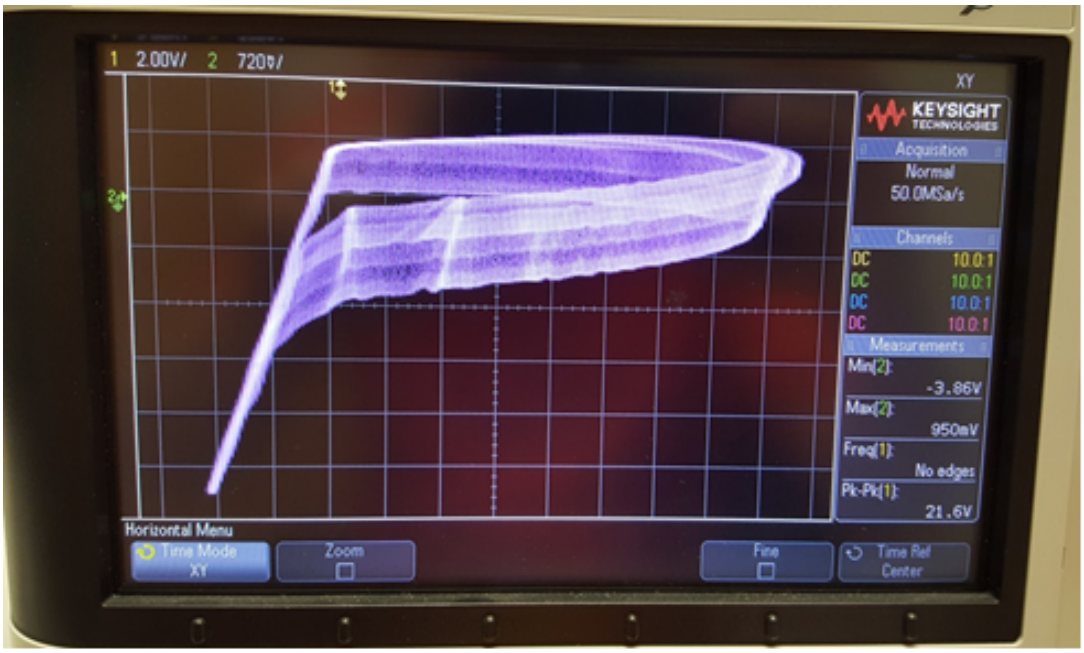

Figure 5.18: Phase space of the sinusoidal forcing function vs. base voltage of the 1 MHz oscillator using the 2N5089.

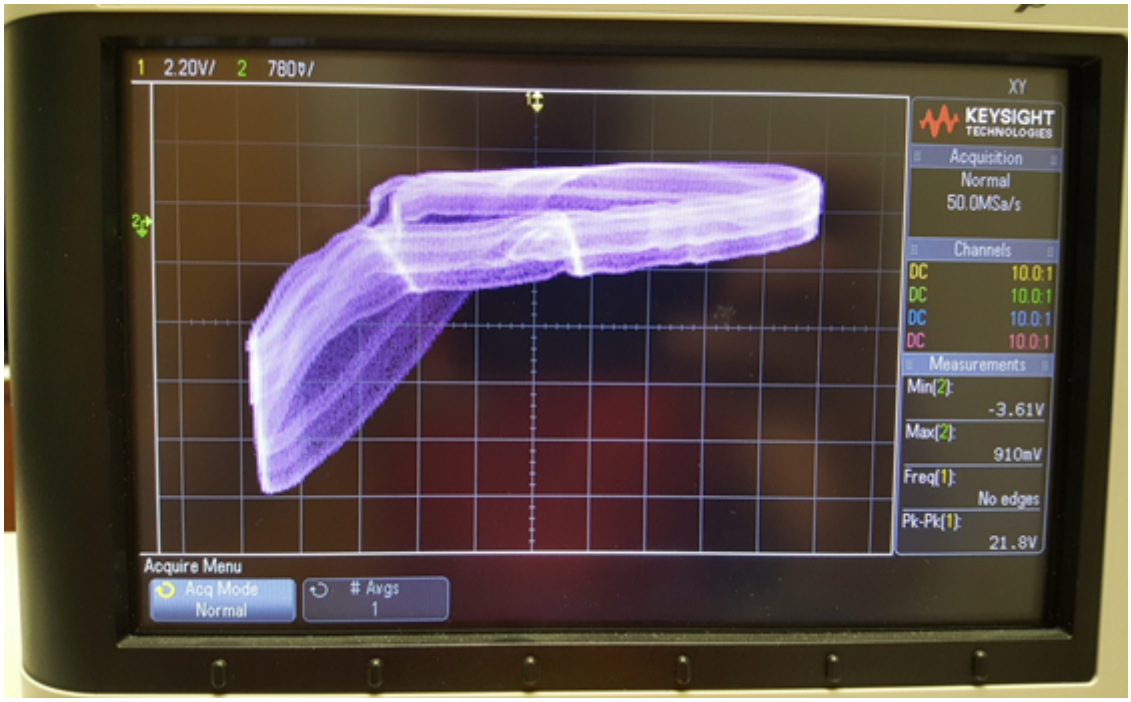

Figure 5.19: Phase space of the collector voltage vs. base voltage of the 1 MHz oscillator using the 2N5089.

Figure 5.20: Time domain plot of the base voltage (green) and collector voltage (yellow) 1 MHz forced oscillator using the 2N2222.

the base voltage can be seen in and Fig. 5.21. These results demonstrate that the 2N2222 performance is very similar to the 2N5089. This distortion could potentially be caused in part from the function generator, but it is more likely a result of the transistor's limited bandwidth while operating near the cut off frequency.

5.3 Forced Nonlinear Transistor PCB Design

Two PCBs were constructed in order to demonstrate the nonlinear transistor circuit, as shown in Fig. 5.22 and Fig. 5.23. One of these boards was populated with appropriate resistors and capacitors in order to achieve a fundamental frequency of approximately 5.1 MHz, shown in the top of Fig. 5.23. This board is approximately 2.5 cm by 3.0 cm and a large portion of the board's real estate is dedicated to the forcing function and the variable gain stage of the design. Time domain results for the linear forcing function and the transistor's base voltage can be seen in Fig. 5.24. Here, the yellow waveform produced is the output of the twin-T oscillator that is used as the forcing function and the green waveform is the transistor's base voltage. Plotting these two outputs versus each other results in the phase space seen in Fig. 5.25. The included potentiometer allows for the gain of the forcing function to be tuned into periodic orbits as well.

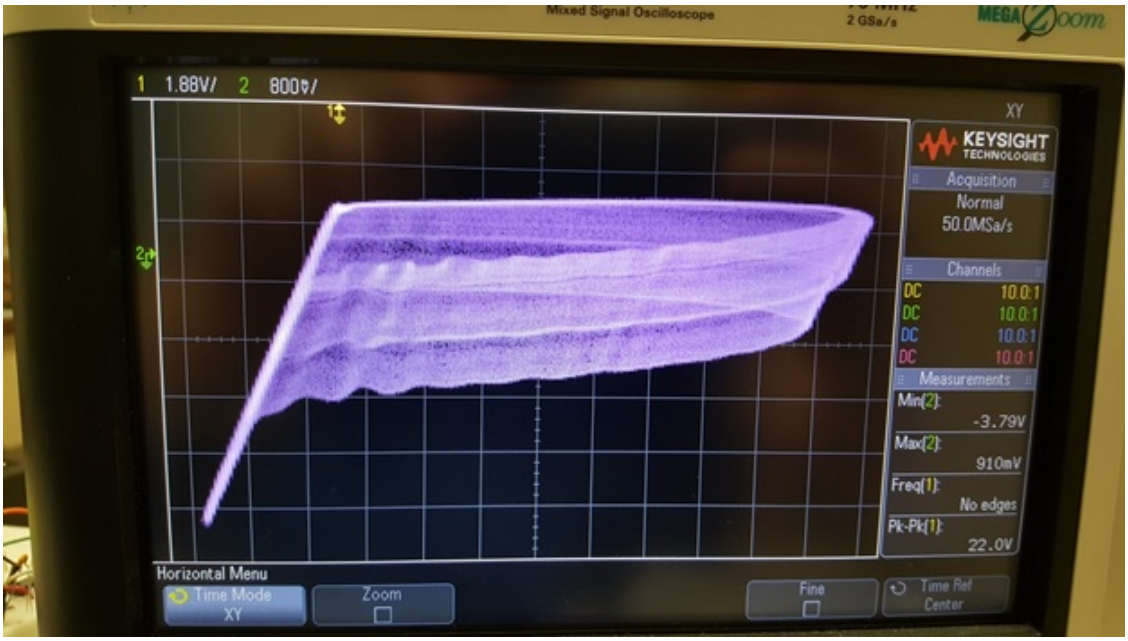

Figure 5.21: Phase space of the sinusoidal forcing function vs. base voltage of the 1 MHz oscillator using the 2N2222.

An example of this can be seen in Fig. 5.26, where a period-4 orbit of the oscillator is shown in the base voltage of the transistor. The corresponding phase space of the base voltage versus the forcing function can be seen in Fig. 5.27.

A second board, shown at the bottom of Fig. 5.23, has been modified so that the collector current can be measured using a Hall effect sensor, as shown in Fig. 5.28. A demonstration of this can be seen in Fig. 5.29, where the board is oscillating at approximately 700 kHz. This phase space is a plot of the collector voltage versus the collector current. This board has a trace discontinuity that allows for two jumper wire leads to be connected to complete the transistor's collector current lead. This allows for the current to be measured off the board with the Hall effect sensor. It is noted that the introduction of the long wire and the Hall effect sensor introduces some interference in the transistor circuit, which limits the maximum operational fundamental frequency. These results are in good agreement with the original oscillator's circuit dynamics and simulations. Another phase space, depicted in Fig. 5.30, is a plot of the transistor's base voltage versus the collector current.

In a similar manner to the breadboard prototype of the nonlinear transistor circuit, the values of the capacitors were gradually decreased in order to test the circuit at higher frequencies. In order to further push the frequency of the design, a different transistor was used. The 2N2369A was used over the 2N5089 because of its significantly higher transition frequency of 50 MHz and 300 MHz, respectively. The capacitors on the PCB are surface mount, so a hot air rework station was used to remove the capacitors. Both the capacitors in the nonlinear transistor

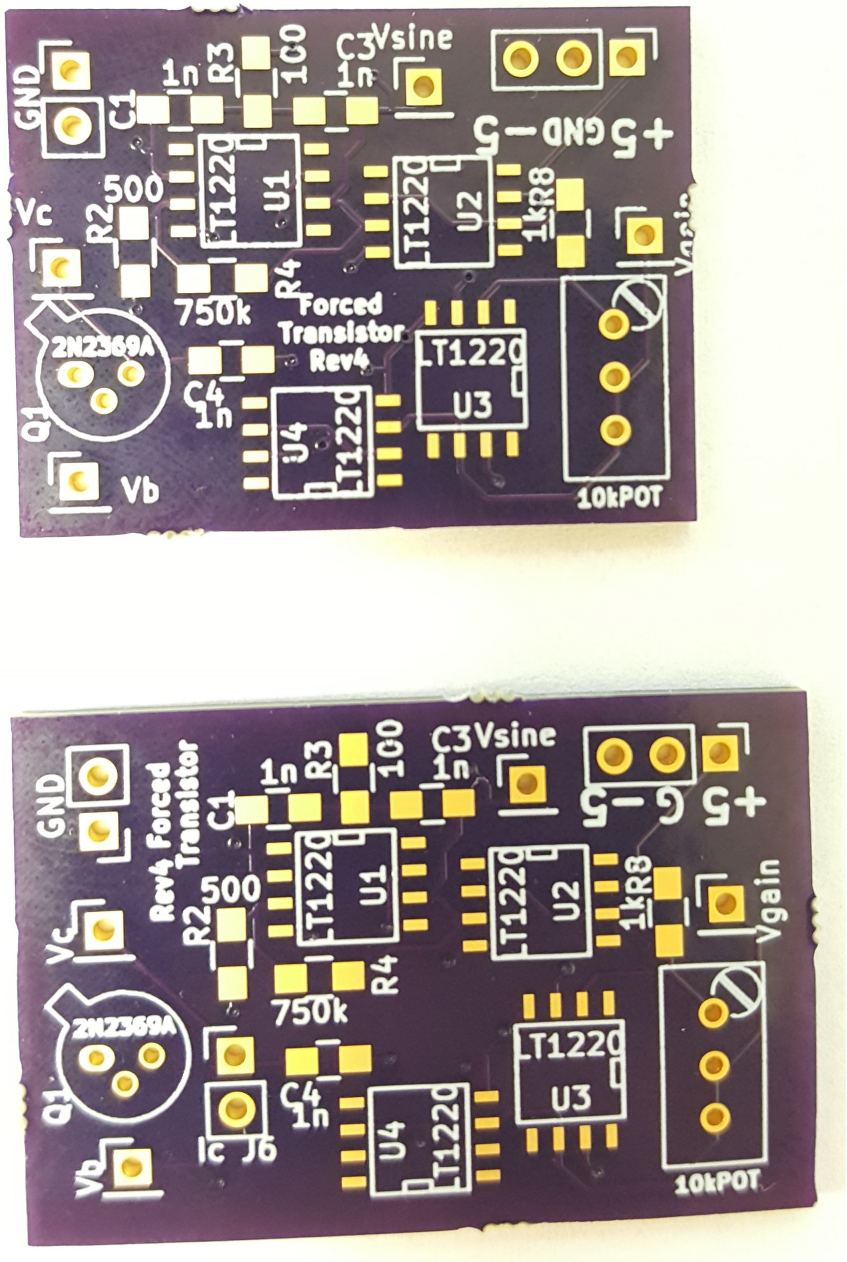

Figure 5.22: Two unpopulated PCBs of the forced transistor circuit with a fundamental frequency of 5.1 MHz (top) and 700 kHz design modified for current measurements (bottom).

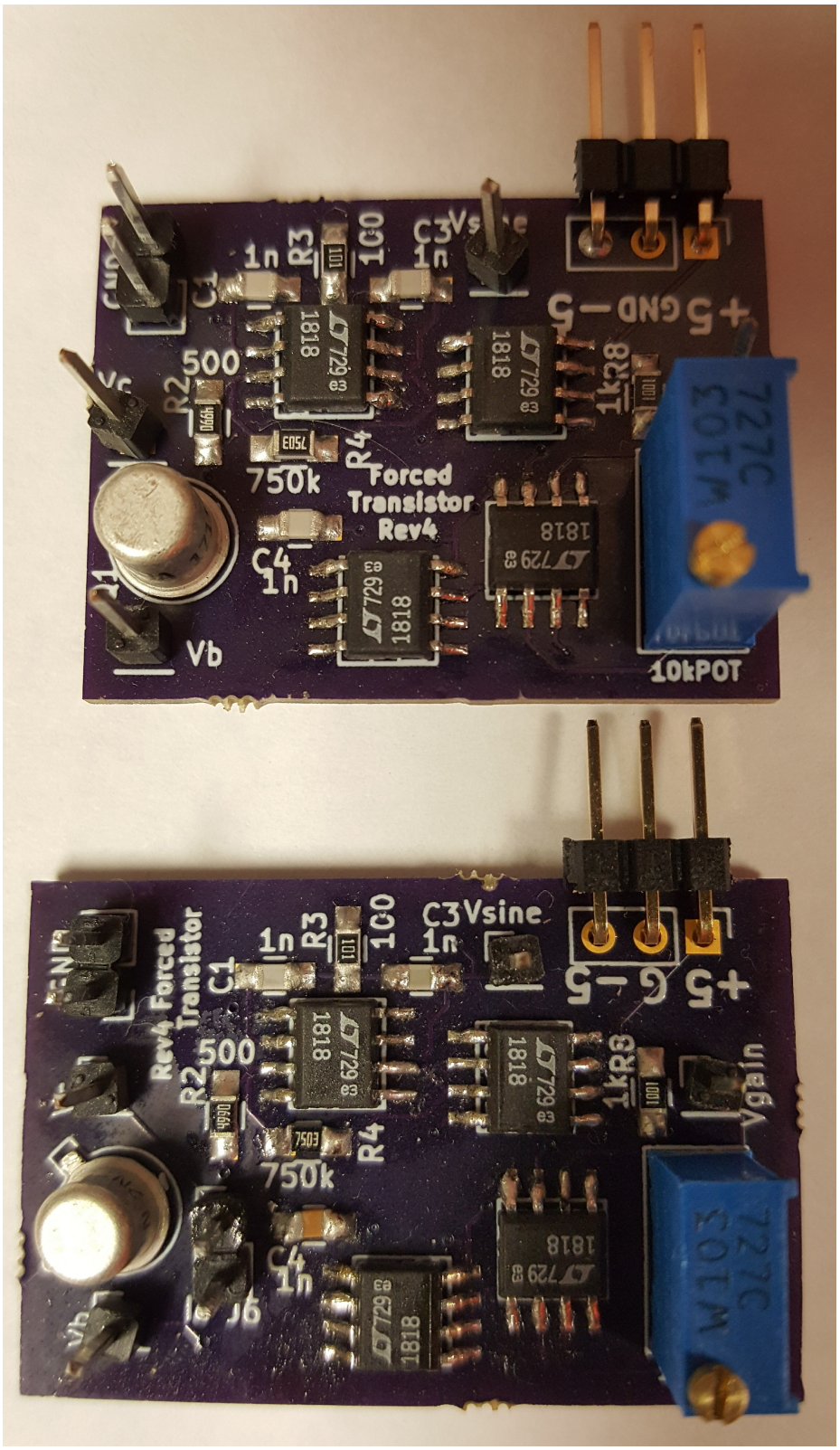

Figure 5.23: Two populated PCBs of the forced transistor circuit with a fundamental frequency of 5.1 MHz (top) and 700 kHz design modified for current measurements (bottom).

circuit and the twin-T oscillator have to be changed in order to achieve different fundamental operating frequencies. By choosing the appropriate capacitor values, the frequency of the oscillations was increased. For a capacitor value of 150 pF for C1 and C2, shown in Fig 5.12, results in a fundamental frequency of approximately 5.1 MHz, shown in Fig 5.31. Plotting the

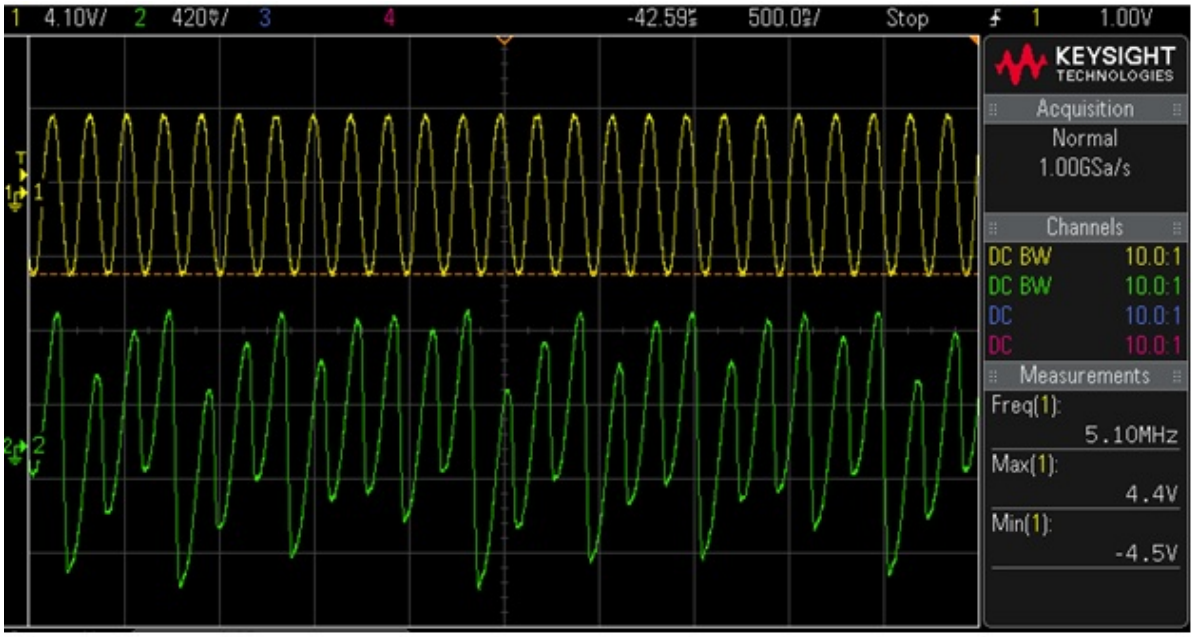

Figure 5.24: Hardware results for the 5.1 MHz forcing function (yellow) and the transistor's base voltage (green).

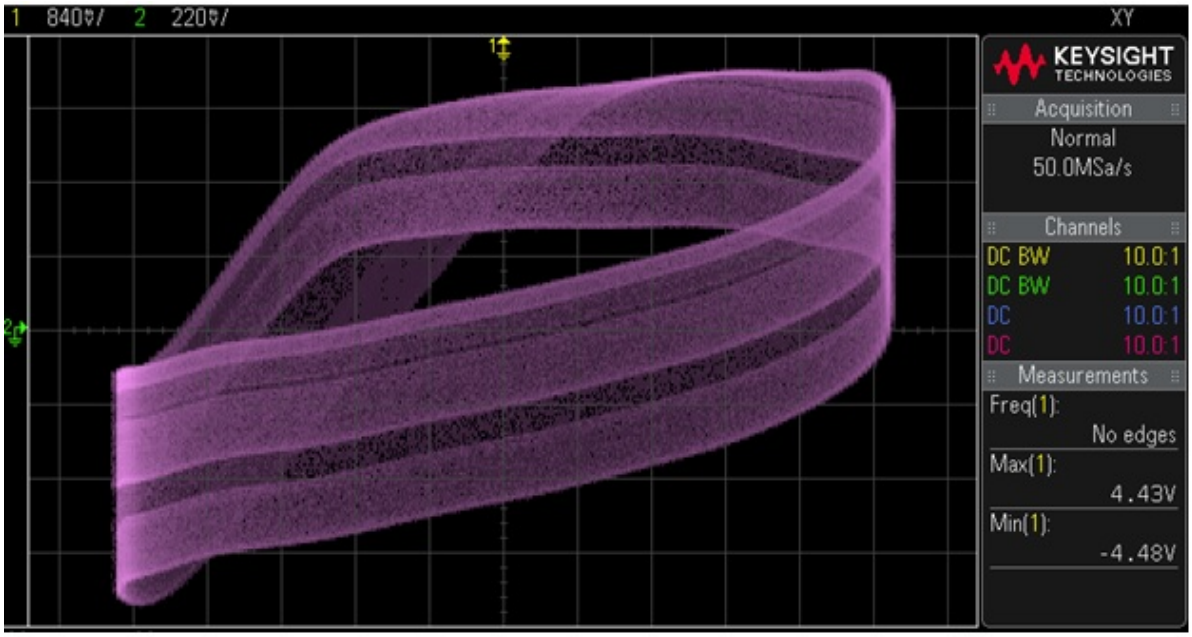

Figure 5.25: Phase space for the hardware results of the forcing function versus the transistor's base voltage.

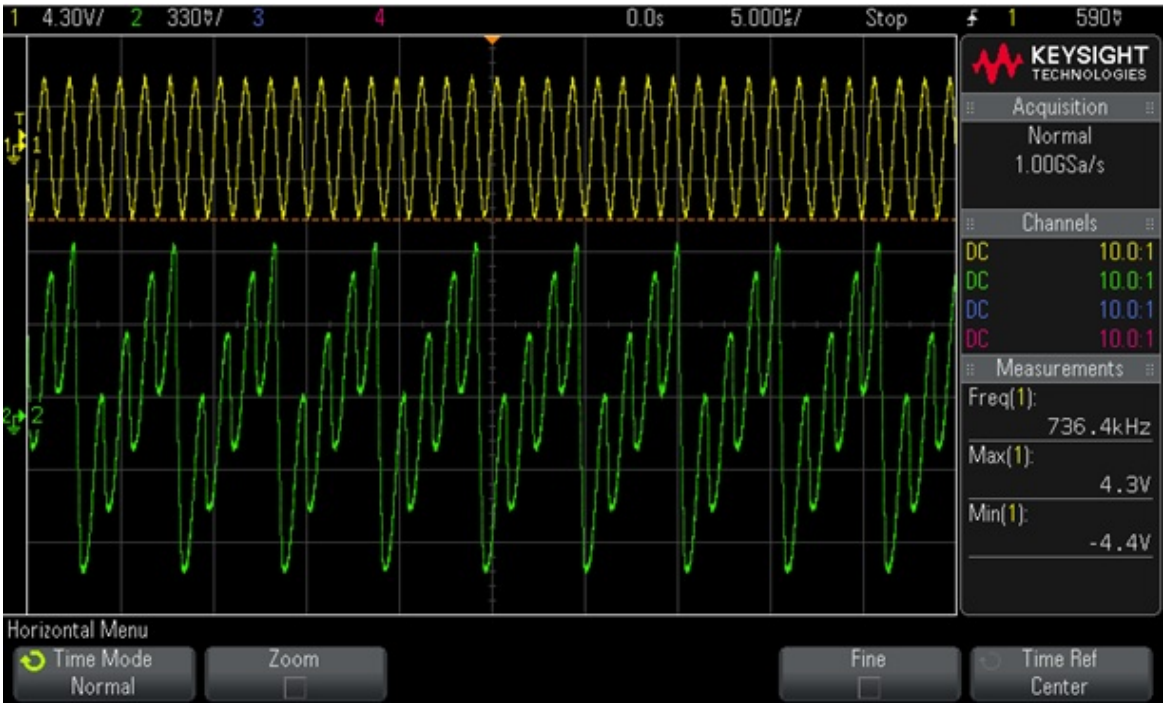

Figure 5.26: Time Domain of the oscillator with a period-4 orbit, where the forcing function is in yellow and the base voltage is in green.

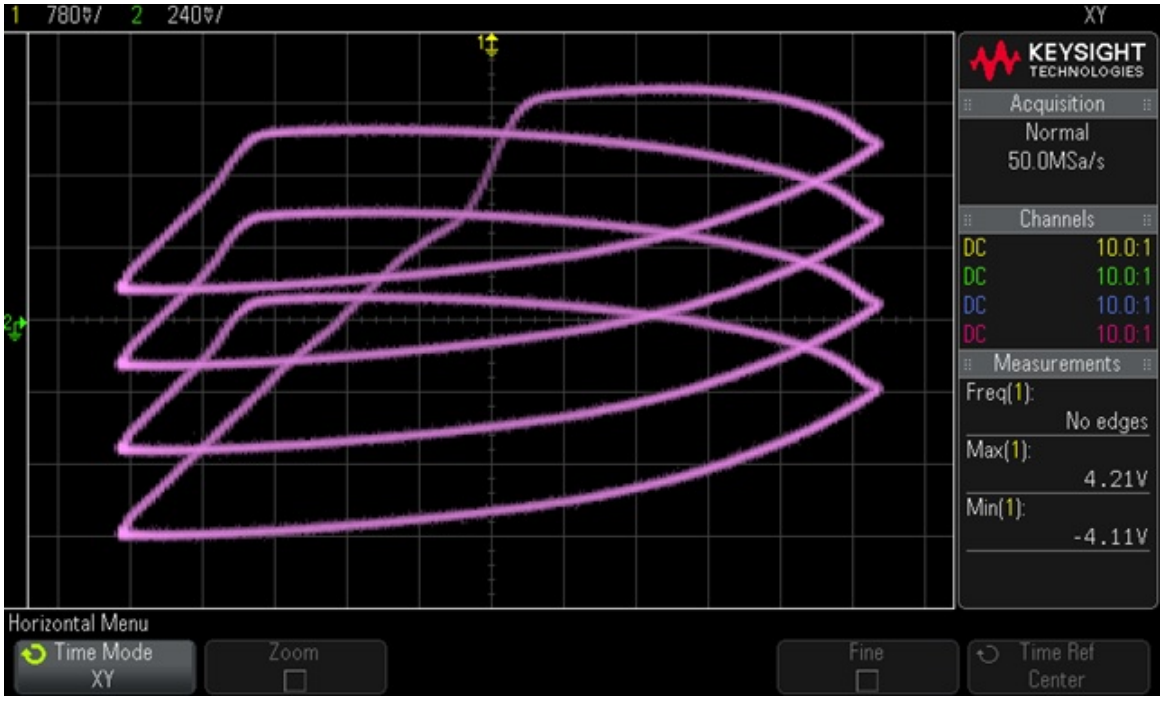

Figure 5.27: Phase space of the oscillator with a period-4 orbit.

forcing function versus the transistor's base voltage results in the phase space, which is shown in Fig. 5.32.

Decreasing the capacitors down to 120 pF increases the fundamental frequency up to 6.25 MHz. The time domain results for the forcing function and the base voltage can be seen in Fig. 5.33 where the yellow waveform is the forcing function and the green waveform is the base voltage. Plotting these two versus each other results in the phase space shown in Fig. 5.34. Comparing the phase space in Fig. 5.32 and the somewhat thinner region of attraction in Fig. 5.34 indicate that increasing the frequency of the design might restrict the grammar of the system. However, both frequencies exhibit both periodic and chaotic windows of oscillation, like the lower frequency breadboard design.

Increasing the frequency further to 7.45 MHz requires a capacitor value of 100 pF. The time domain and phase space results for chaotic motion at 7.45 MHz are shown in Fig. 5.35 where the forcing function is in yellow and the transistor's base voltage is in green. Plotting the forcing function versus the base voltage yields the phase space found in Fig. 5.36. Once again, the bands in the phase portrait seem to be slightly thinner than the lower frequency results. The distortion is also obvious in the transistor's base voltage waveform.

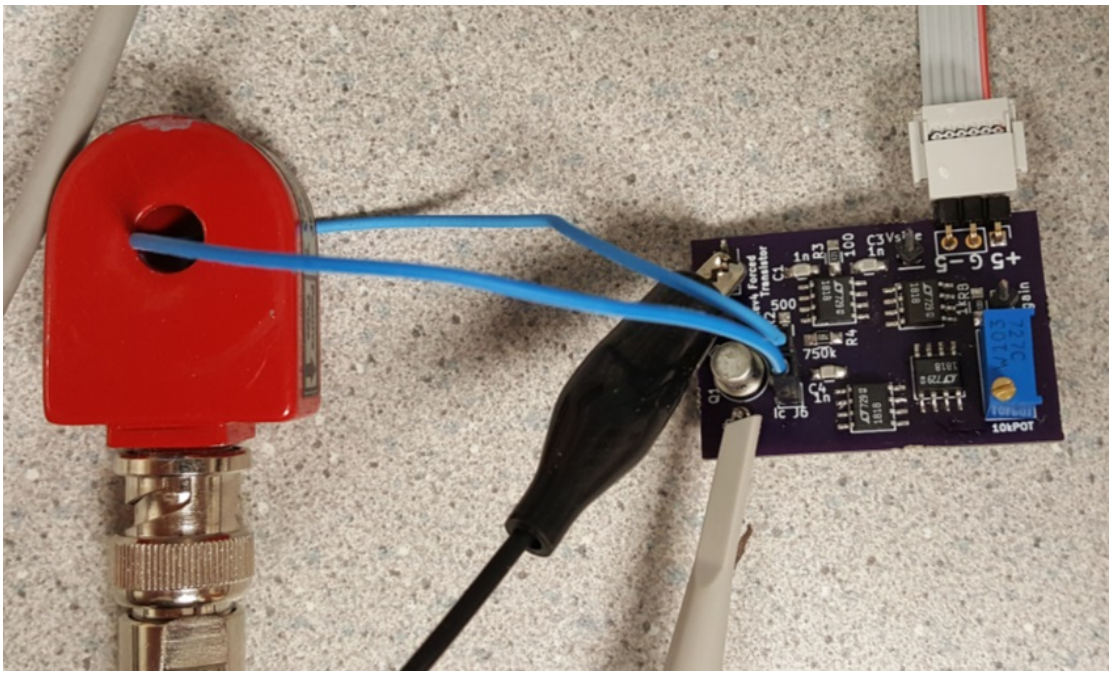

Figure 5.28: A close up of the Hall effect current probe connected PCB.

This trend follows until the oscillator reaches it maximum obtainable frequency at approximately 10.5 MHz. These results are shown in Fig. 5.37 and Fig. 5.38. While the twin-T oscillator can be pushed well beyond 10 MHz, there are a number of factors in the transistor circuit that could contribute to frequency scaling limitations. One of these is that the values of the capacitors start to become very small, which can be affected significantly by packaging and layout parasitics. Another limiting factor is that the only active element in nonlinear portion of

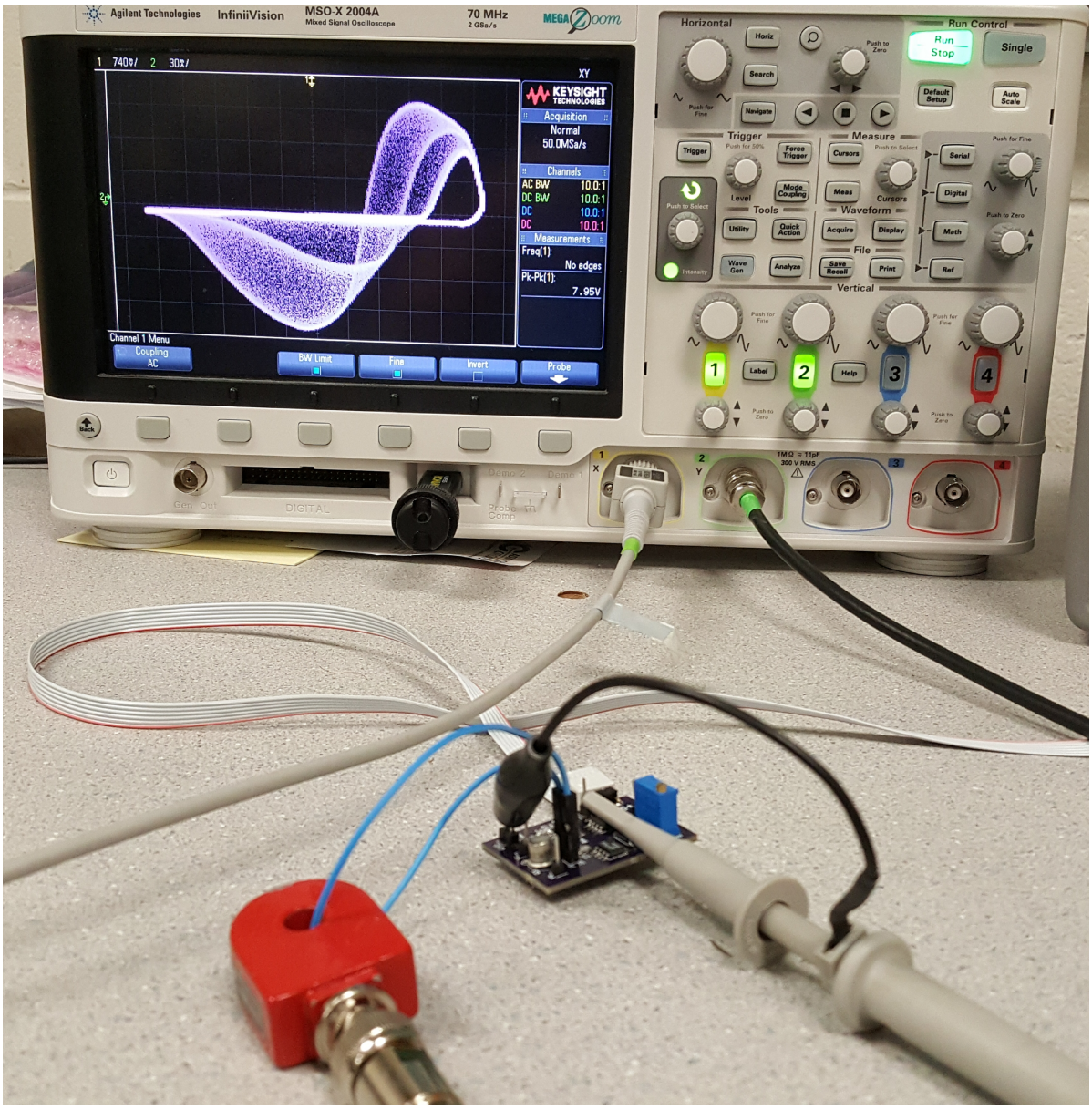

Figure 5.29: Phase space for the hardware results of the collector voltage versus the collector current.

the circuit is a transistor (2N2369A), that has a transition frequency of 300 MHz. A summary of all the differnt capactior values and operating frequencies can be found in Table 5.1.

Since the nonlinear transistor circuit transitions from periodic to chaotic solutions based on the frequency and amplitude of the forcing function, one of these parameters needs to be variable. For this reason, the twin-T oscillator was set to operate at a fixed frequency by using static resistors and capacitors in the feedback path. In order to vary the amplitude of the forcing function, an analog inverting amplifier was used where the feedback resistor was replaced with

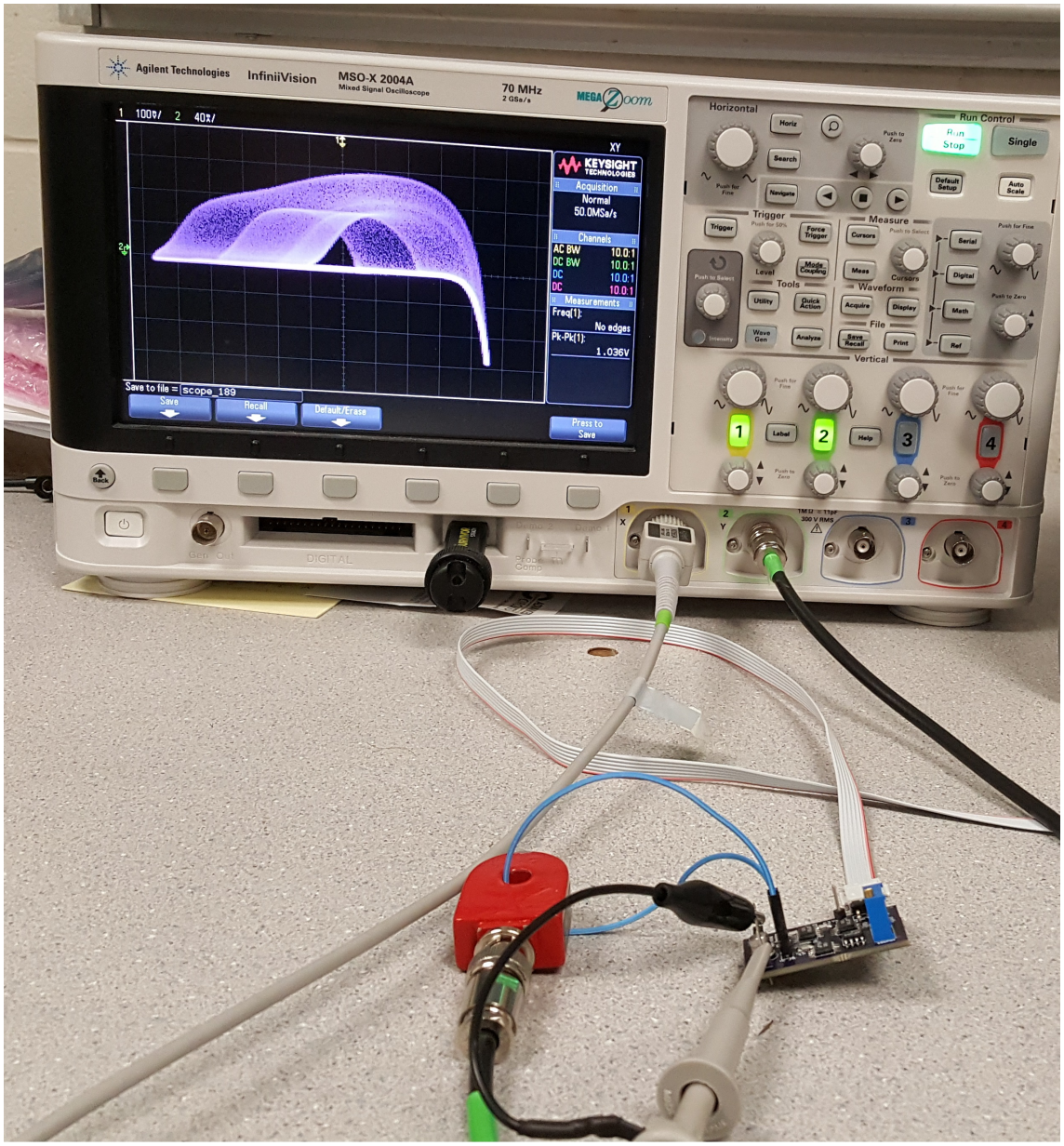

Figure 5.30: Phase space for the hardware results of the base voltage versus the collector current.

a potentiometer. By manually tuning this potentiometer, the chaotic time domain trajectory in Fig. 5.39a was found. The fundamental frequency of this circuit is 795 kHz. The forcing function is plotted in yellow, while the transistor's base voltage is plotted in green. The corresponding phase space of the forcing function versus the transistor's base voltage can be seen in Fig. 5.39b. Tuning the potentionmeter results in the periodic solution found in Fig. 5.39c and

Figure 5.31: Time domain results (yellow: forcing function, green: base voltage) of the transistor circuit with capacitor values of 150 pF, which results in a 5.1 MHz oscillation.

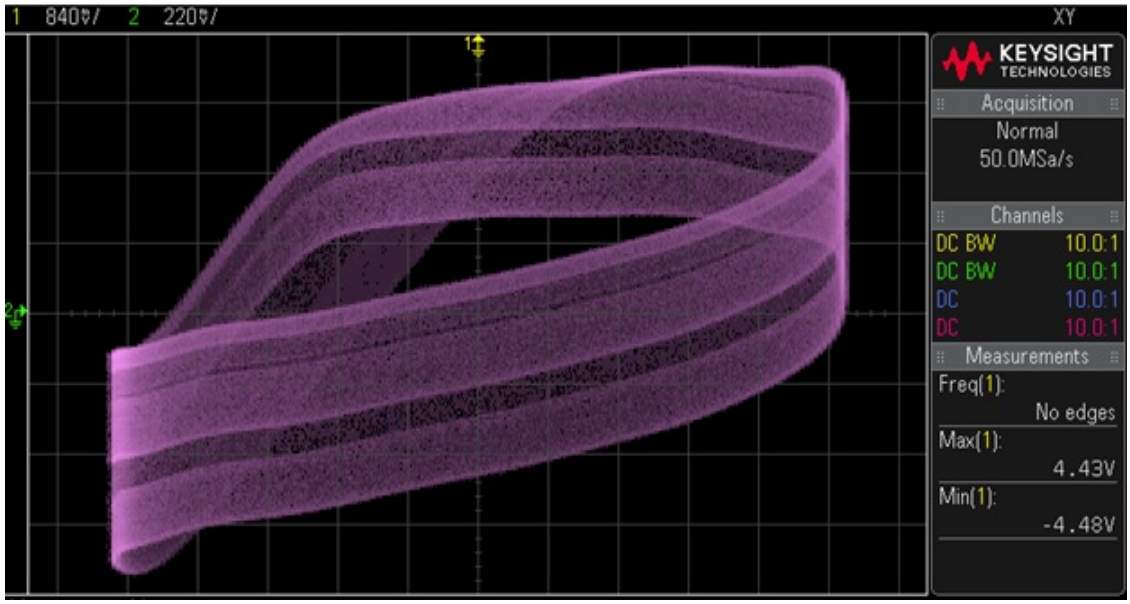

Figure 5.32: Phase space plot of the base voltage vs. the sinusoidal forcing function of the transistor circuit with capacitor values of 150 pF, which results in a 5.1 MHz oscillation.

Fig. 5.39d. Here, the forcing frequency is approximately 735 kHz, which is plotted in yellow, and the transistor's base voltage is plotted in green. The fundamental frequency of this board is slightly lower than the other different operating frequency of the twin-T oscillator. By changing values of the capacitors and resistor in the twin-T oscillator, the fundamental frequency of operation can be increased to approximately 5.1 MHz, as shown in Fig. 5.39e. The corresponding phase space at this frequency can be seen in Fig. 5.39f.

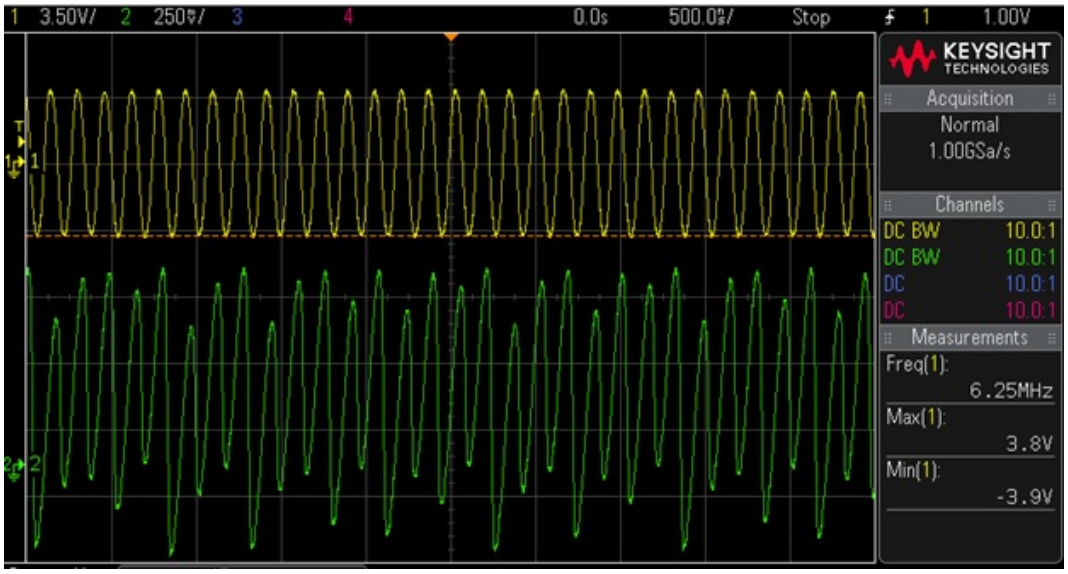

Figure 5.33: Time domain results (yellow: forcing function, green: base voltage) of the transistor circuit with capacitor values of 120 pF, which results in a 6.25 MHz oscillation.

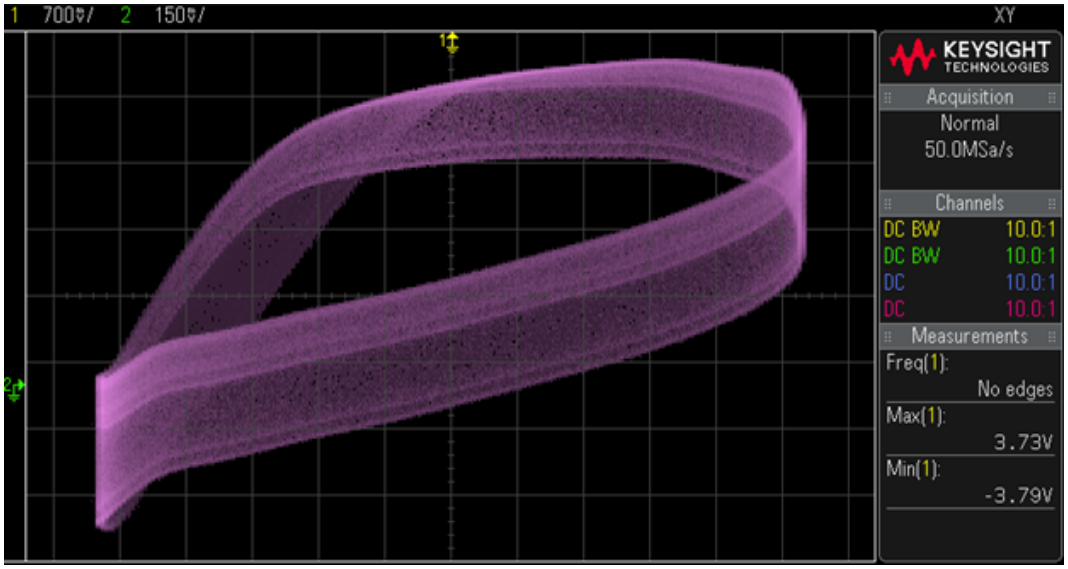

Figure 5.34: Phase space plot of the base voltage vs the sinusoidal forcing function of the transistor circuit with capacitor values of 120 pF, which results in a 6.25 MHz oscillation.

A comparison of the simulation results from equations (4.2)-(4.4) with the hardware results can be seen in Fig. 5.40. Here, the time domain response of the Ebers-Moll model (Fig. 5.40a) is seen to be qualitatively similar to the experimental results (Fig. 5.40b). Similarly, the phase space of the Ebers-Moll model (Fig. 5.40c) is seen to be qualitatively similar

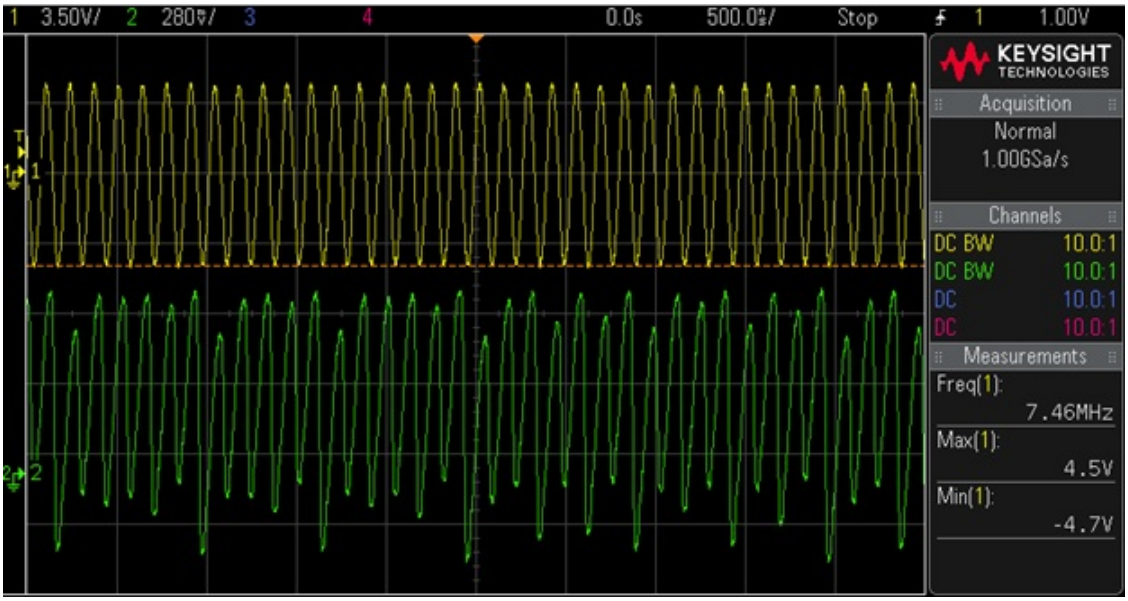

Figure 5.35: Time domain results (yellow: forcing function, green: base voltage) of the transistor circuit with capacitor values of 100 pF, which results in a 7.45 MHz oscillation.

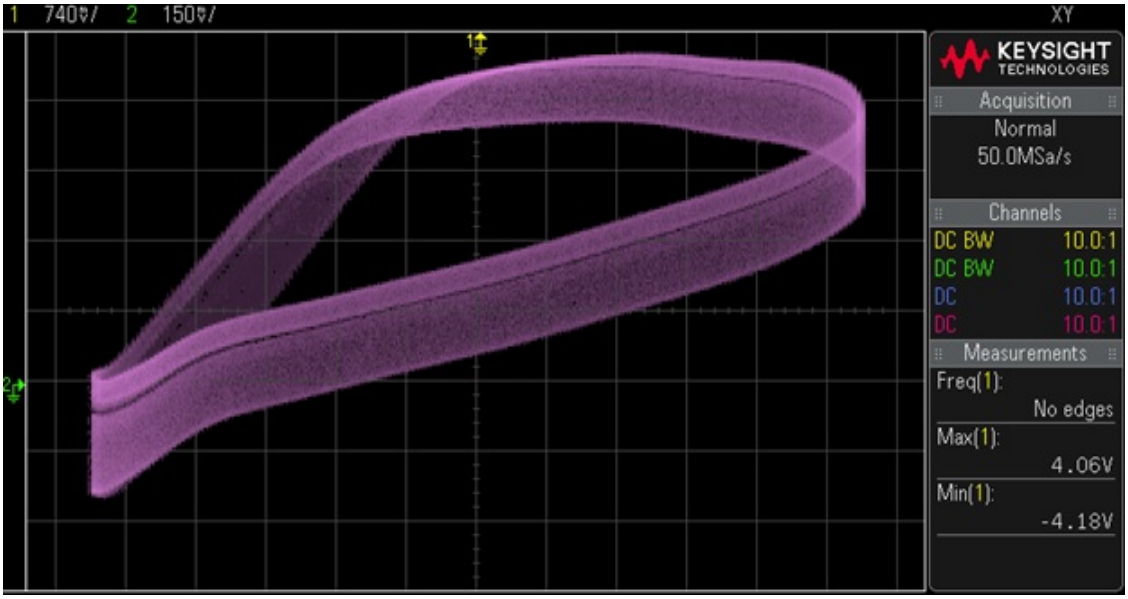

Figure 5.36: Phase space plot of the base voltage vs the sinusoidal forcing function of the transistor circuit with capacitor values of 100 pF, which results in a 7.45 MHz oscillation.

to the experimental results (Fig. 5.40d). This comparison shows that the simulation model using the Ebers-Moll model for the BJT is in good agreement with the hardware results.

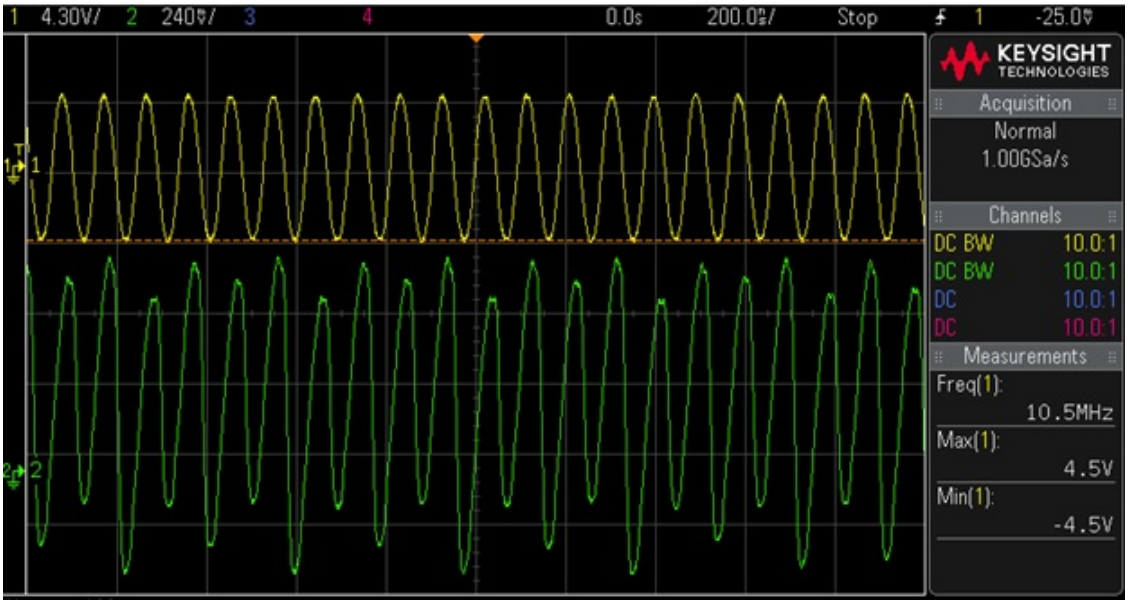

Figure 5.37: Time domain results (yellow: forcing function, green: base voltage) of the transistor circuit with capacitor values of 68 pF for twin-T and 39 pF for the transistor circuit, which results in a 10.5 MHz oscillation.

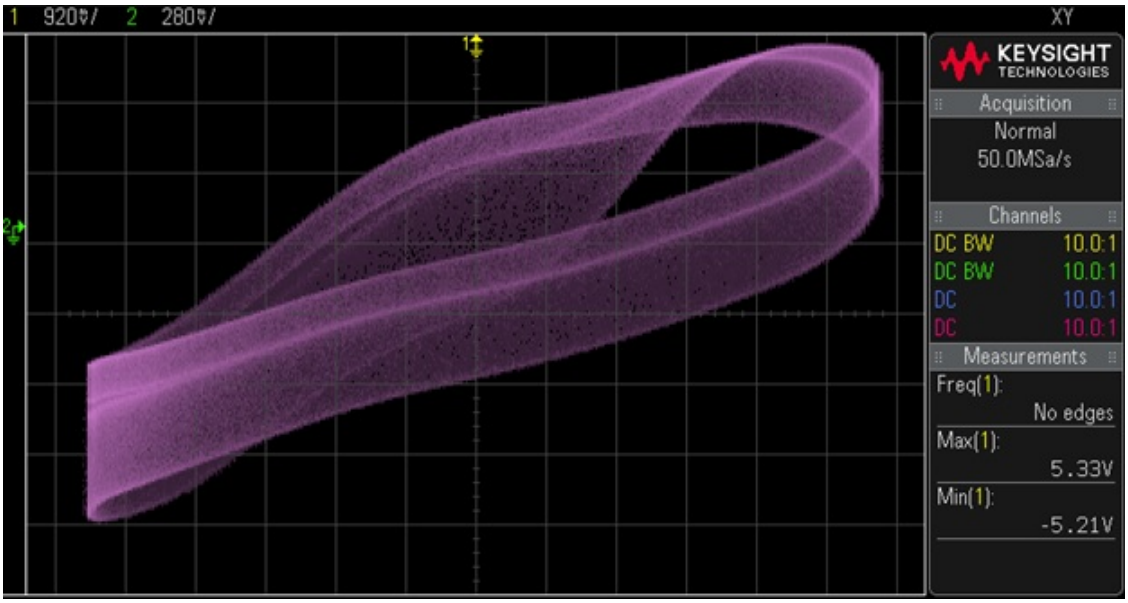

Figure 5.38: Phase space plot of the base voltage vs the sinusoidal forcing function of the transistor circuit with capacitor values of 68 pF for twin-T and 39 pF for the transistor circuit, which results in a 10.5 MHz oscillation.

Frequency (MHz)	C_1 (pF)	C_2 (pF)
5.1	150	150
6.25	120	120
7.45	100	100
10.5	39	68

Table 5.1: Table summarizing the capacitor values for C_1 and C_2 and resulting frequency of the nonlinear transistor circuit.

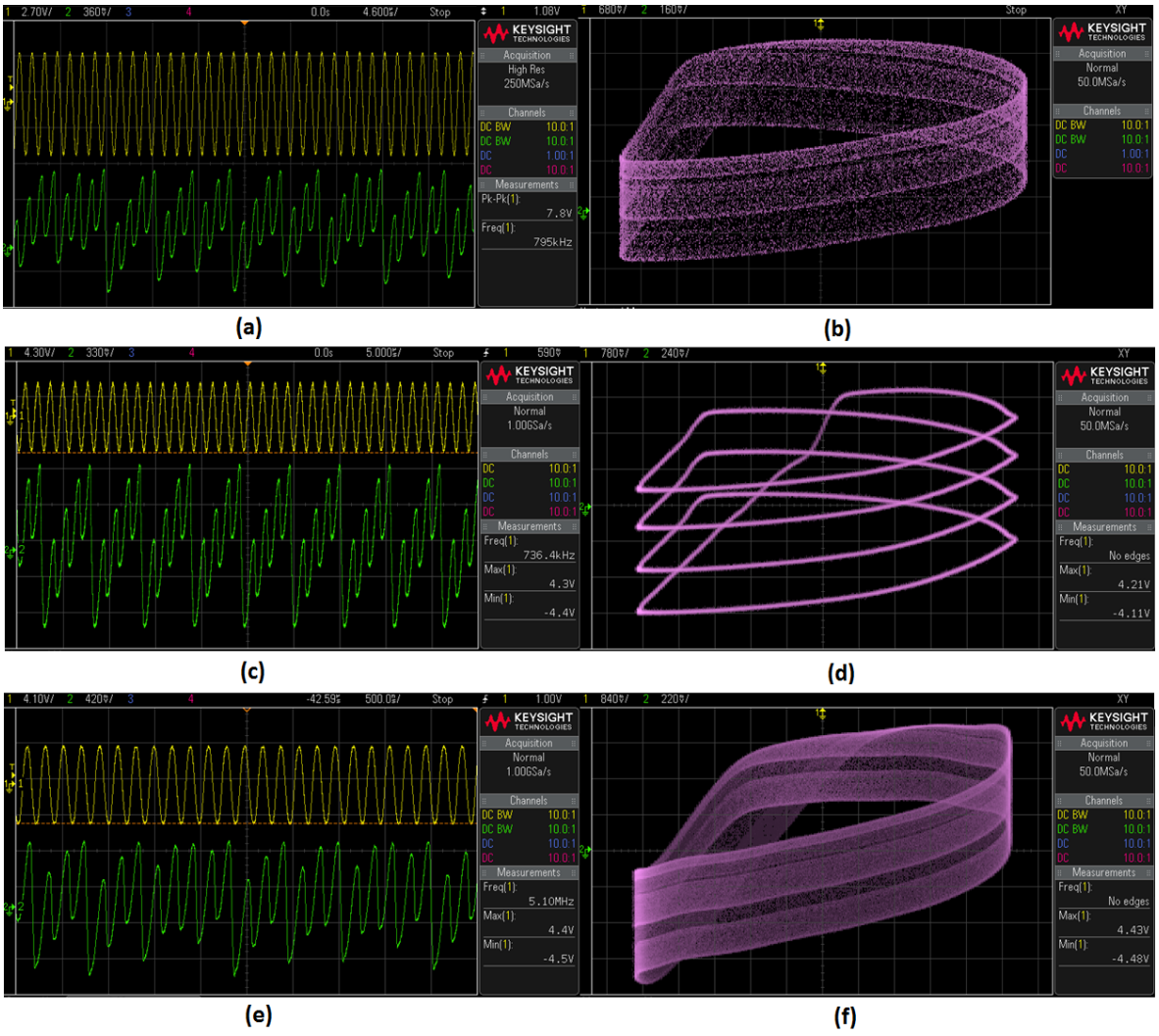

Figure 5.39: (a) Time domain plot of the chaotic response, where $f = 795$ kHz. (b) Phase space of the chaotic orbits, where $f = 795$ kHz. (c) Time domain plot of the periodic response, where $f = 735$ kHz. (d) Phase space of the periodic orbits, where $f = 735$ kHz. (e) Time domain plot of the chaotic response, where $f = 5.1$ MHz. (f) Phase space of the chaotic orbits, where $f = 5.1$ MHz.

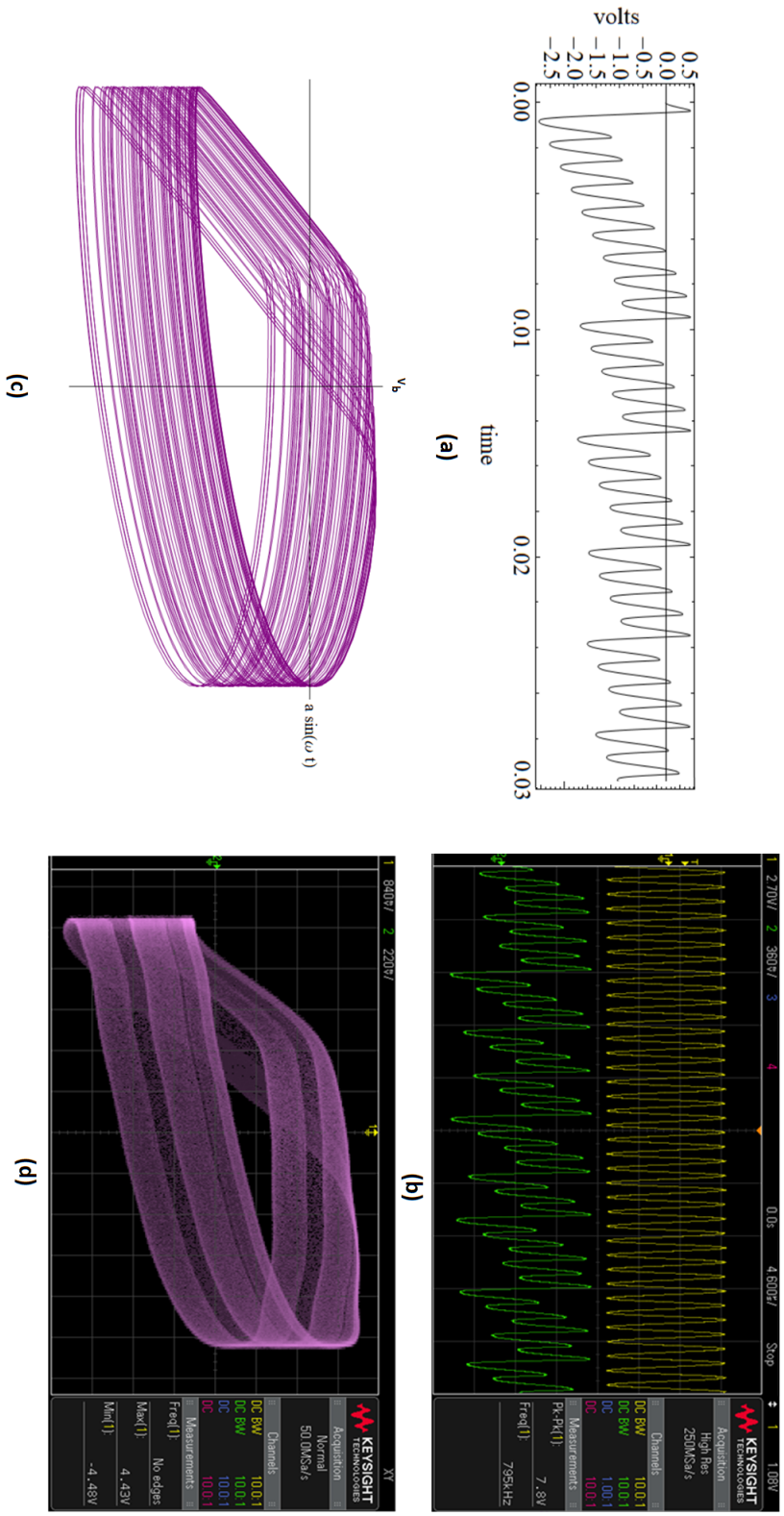

Figure 5.40: (a) Time domain plot of the chaotic response from Ebers-Moll simulation. (b) Time domain plot of the chaotic response from the experiment. (c) Phase space of the chaotic orbits from simulation. (d) Phase space of the chaotic orbits from the experiment.

Chapter 6

Conclusions

Chaos electronics have a wide range of potential applications; however, many of these are based on theoretical calculations or ideal mathematical definitions which may be difficult or impractical to realize in electronic circuits. This work investigated some previous work done on these systems and proposes some potential alternate topologies. These are topologies that may lend itself to more practical and reliable implementations in electronics. These typologies might scale more favorable in frequency while still maintaining the original system's functionality.

In this work, three chaotic systems were analyzed, simulated, and constructed in hardware. Two of these autonomous systems have been shown to have exact analytical solutions, which were used to develop matched filters for these systems. This makes both of these systems ideal candidates for communication and radar applications. One of the presented systems was demonstrated in a chaos based communication system. This system was controlled using proportional feedback control in order to encode information into the oscillator's waveform.

While both of these exactly solvable systems share underlying dynamics that are conjugate to the iterated shift map, the primary difference between them is the order of the filter. One system is based on a second-order filter and the other is based on a first-order filter. These designs were simulated using SPICE, where alternate topologies from the original motivation work were developed. Both of these designs were implemented using COTS parts on custom designed PCBs.

The second system demonstrated shared the underlying dynamics as the previously mentioned system. Both of these systems are conjugate to the iterated shift map; however, this one was based on a first-order filter instead of a second-order filter. The original circuit proposed

contained a comparator and level shifting op-amps in the feedback path. By separating the analog and digital grounds, the feedback componets could be replaced by CMOS invertors. Since the trip voltage of the comparators is roughly half the power supply voltage, they could effectively act as a comparator.

This alternate topology was implemented using a custom PCB that was approximately 2.54 cm by 2.54 cm. Multiple ICs were replaced by a single IC while still maintaining functionality. SMD COTS parts were used to further reduce the form factor of the electronic chaotic system.

The third system was a non-autonomous circuit based on a nonlinear transistor circuit. This circuit topology was modeled using the Ebers-Moll model for a NPN BJT. From this model, a system of equations was derived using nodal analysis and numerically simulated. These results were shown to be qualitatively similar to the SPICE and hardware results. This system was sinusoidal forced and it could exhibit both chaotic and periodic motion based on the amplitude and frequency of the forcing function. From varying these two parameters, bifurcation diagrams were constructed of the system.

This relatively simple circuit consisted of two capacitors, two resistors, and a single NPN BJT; it was implemented on a custom PCB. In order to minimize the overall footprint of the design, the sinusoidal forcing function was integrated onto the PCB with the nonlinear transistor circuit.

Two PCBs were constructed, one at 5.1 MHz and one at approximately 750 kHz, to demonstrate high frequency operation and to show the phase space featuring the collector current of the transistor. Both of these designs fit on an approximately 2.5 cm by 3.0 cm PCB. Simulation and hardware results were in were in good agreement with the original motivation. These designs show that the inherent nonlinearities in electronic devices can be realized in a relativity small footprint across a wide range of frequencies. This can lead to easier integration into potential applications, such as RNG, communications, and radar, where chaotic properties are advantageous.

There are a wide range of applications that could benefit from high frequency chaotic oscillators, such as communication systems, radar, and RNGs. For this reason, the nonlinear

transistor circuit was modified to operate at higher frequencies by changing component values. This design was able to operate at an upper limit of approximately 5.1 MHz, before the waveform began to deviate from expected operation.

Chapter 7

Future Work

Much of the work in this dissertation was focused on developing these electronic chaotic systems. Future work on these systems would include pushing the fundamental frequency of these designs. One approach to doing this would be to design the chaotic systems into an ASIC. It is noted that moving to an ASIC would significantly increase the cost as well as take significantly longer to manufacturer and test. The advantage of quick prototyping is lost on this approach.

The presented design for the exactly solvable chaotic system based on the second-order filter operated at a fundamental frequency of approximately 18.9 kHz. This frequency was chosen in order for information to be easily and reliably encoded into the waveform for use in a communication system. One of the primary advantages of an ASIC for an oscillator is the reduction of the overall propagation of the feedback path since all the devices are included in a single package as well as having matching capacitors and transistors. The proposed topology has advantages over the NIC design since a single transistor oscillator is easier to implement than a single or a network of op-amps in an ASIC.

Similarly, the design for the exactly solvable chaotic system based on the first-order filter could benefit from being implemented in an ASIC. A very high bandwidth op-amp could be designed for the op-amp based NIC, which could greatly increase the fundamental frequency of the design. This, combined with high speed logic designs, could greatly decrease the propagation delay through the feedback path.

The nonlinear transistor circuit was tested at various frequencies, where the primary limiting factor was found to be the GBP of the transistor and the size of the capacitors in the circuit.

In the same breathe as the other two designs, moving the design to an ASIC would be beneficial for this design. Since the PCB design of this board is at a moderately high frequency, this design could also be tested as an RNG. This could be done by using a very precise data logging oscilloscope and tested using the NIST or Dieharder statistical testing suites.

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Appendices

Appendix A

MATLAB Code To Generate Shift Map From Simulation Data

```
%%
%plot shift map from sim

%read in results from "data" which is : by 5 array
time=data(:,1);  %time domain points
clk=data(:,2);   %system clock for D-flip flop
clk2=data(:,3);  %half the frequency of the system clock
V=data(:,4);     %voltage node V
Vs=data(:,5);    %feed back voltage node Vs

%find zero crossings
% Returns Zero-Crossing Indices Of Argument Vector
zci = @(v) find(v(:).*circshift(v(:), [-1 0]) <= 0);
% Approximate Zero-Crossing Indices
zx = zci(clk2-2.5);

% V=V-mean(V);

%clear arrays
Vzc=[];
Tzc=[];


%find pointers
for i = 1:length(zx)
    Vzc(i)=V(zx(i));
    Tzc(i)=time(zx(i));
end

% count=1;
% for i = 1:(length(zx)/2)-1
%     Vzc(count)=V(zx(count));
%     Tzc(count)=time(zx(count));
%     count=count+2;
```

```
% end

%Plot the shift map
hold on
for i = 1:100    \%if you want all points (length(zx)-1)
    scatter(Vzc(i),Vzc(i+1),'*','k')
end
xlim([0,5]) \%Vcc was 5V
ylim([0,5])
 xlabel('V_n (Volts)')
 ylabel('V_{n+1} (Volts)')
set(gca,'FontSize', 15)
```

Appendix B

MATLAB Code To Generate Shift Map From Hardware Data

```
%%
%plot shift map from hardware

%read in results from "data" which is : by 5 array
time=data(:,1);  %time domain points
% clk=data(:,2);   %half the frequency of the system clock
clk2=data(:,3);  %system clock for D-flip flop
V=data(:,2);     %voltage node V
Vs=data(:,4);    %feed back voltage node Vs

%find zero crossings
% Returns Zero-Crossing Indices Of Argument Vector
zci = @(v) find(v(:).*circshift(v(:), [-1 0]) <= 0);
% Approximate Zero-Crossing Indices
zx = zci(clk2);
zx = zx(1:2:end);  %take every other ZC

% V=V-mean(V);

%clear arrays
Vzc=[];
Tzc=[];


%find pointers
for i = 1:length(zx)
    Vzc(i)=V(zx(i));
    Tzc(i)=time(zx(i));
end



% count=1;
% for i = 1:(length(zx)/2)-1
```

```
%     Vzc(count)=V(zx(count));
%     Tzc(count)=time(zx(count));
%     count=count+2;
% end

%normalize
% Vzc_max =(max((Vzc)));
Vzc_min =(min((Vzc)));
% % Vzc=(Vzc+Vzc_max)/(Vzc_max);
Vzc=(Vzc-Vzc_min);
Vzc_max =(max((Vzc(2:end))));
Vzc=Vzc/abs(Vzc_max);
%Plot the shift map
hold on
for i = 1:(length(zx)-1)
%if you want all points (length(zx)-1)
    scatter(Vzc(i),Vzc(i+1),'.','k')
end
xlim([0,1])  %Vcc was 5V
ylim([0,1])
 xlabel('V_n (Volts)')
 ylabel('V_{n+1} (Volts)')
set(gca,'FontSize', 15)
```

Appendix C

MATLAB Code To Generate Shift Map From Hardware Data in Noise

```
%%
%%input is a single vector array called 'data'
%find the peaks and valleys of the time domain data
signal=1*data(:,2);
%peaks = mag
%
%%note this only works on versions of matlab2014 or newer
clear peaks valleys timeOfPeak timeOfValley max
clear peaksValleys catValleys catPeaks
% [peaks,loc]= findpeaks
(signal,'MinPeakProminence',0.2,'MinPeakDistance',100);
[peaks,loc]=
findpeaks(data(:,2),'MinPeakProminence',.5);
% [peaks,loc]=findpeaks(signal);%,'MINPEAKHEIGHT',1);
for i = 1:length(peaks)
    timeOfPeak(i) = data(loc(i),1);
end
% timeOfPeak=timeOfPeak';

% h=figure;
% hold on;
% plot(data(:,1),data(:,3),'-r')
% scatter(timeOfPeak, peaks);


% [valleys,loc2] = findpeaks
(-1*signal,'MinPeakProminence',0.2,'MinPeakDistance',100);
[valleys,loc2] =
findpeaks(-1*data(:,2),'MinPeakProminence',.5);
% [valleys,loc2] =
findpeaks(-1*signal);%,'MinPeakProminence',0.5);
for j = 1:length(valleys)
timeOfValley(j) = data(loc2(j),1);
end
```

```
% timeOfValley = timeOfValley';
valleys=valleys*-1;


% scatter(timeOfValley, -1*valleys);
% xlim([0 1e-3])
%find max
max_u=max(signal);
avg=mean(signal);
% avg=0;
% Delete the unwanted outside points
% Q=sortrows(peaksValleys,2);

Q=find((abs(peaks-avg)<0.5));
% Q=find((peaks));
peaks(Q) = [];
timeOfPeak(Q) = [];
%
Q=find((abs(valleys-avg)<0.5));
% Q=find((valleys));
valleys(Q) = [];
timeOfValley(Q) = [];

%%save peaks plot b4 the account for max
% peaks_plot = peaks;
% valleys_plot=valleys;

%account for max
peaks = peaks - max_u+avg;
valleys = valleys + max_u-avg;

%test remove s(t)
% peaks = peaks - 1;
% valleys = valleys - 1;

% peaks = peaks'
%combine all the peaks and valleys into a single array
catPeaks = cat(2,timeOfPeak', +1*peaks);
catValleys = cat(2,timeOfValley',+1*valleys);
peaksValleys = cat(1,catPeaks,catValleys);
%sort values
[values, order] = sort(peaksValleys(:,1));
peaksValleys = peaksValleys(order,:);
%old sort values
% peaksValleys=sort(peaksValleys,'ascend');

 peaksValleys = peaksValleys*0.5;
```

```
 peaksValleys(:,2) = peaksValleys(:,2)+.5;


h = figure;
hold on
% plot(data(:,1),signal,'-r')
scatter(peaksValleys(:,1), peaksValleys(:,2))
xlim([0 1e-3]);
% xlim([0 20]);
% xlim([0 15]);
hold off

% %plots the x coordinates of peakValleys
% h=figure;
% hold on
% for i=1:(length(peaksValleys)-1)
%     scatter(peaksValleys(i,1),peaksValleys(i+1,1))
% end

%plots the y coordinates of peakValleys
count=1;
h=figure;
hold on
for i=1:(length(peaksValleys)-1)
% for i=1:4
scatter(peaksValleys(count,2),peaksValleys(count+1,2),'.')
count = count+1;
end
xlabel('x_n')
ylabel('x_{n+1}')

xlim([0 1])

ylim([0 1])
```