Design and Implementation of High Performance Pipelined SAR ADC for Wireless Communications

by

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Abstract

As the process keeps scaling down, successive approximation register (SAR) architecture becomes an attractive candidate in low-power, moderate-speed A/D converter (ADC) due its mostly digital operation. For high speed application, pipelining and SAR are combined to further improve the speed. As the bottleneck in traditional pipeline ADC, the associated residue generation and amplification continues to be extensively researched to achieve higher resolution.

This work presents a dual-residue pipelined successive approximation register (SAR) A/D converter (ADC) architecture that relaxes the accuracy requirement for residue amplifications to fully utilize the benefits of power efficiency and technology scalability based on zero-crossing (ZX) only signals. The dual-residue architecture is illustrated with design of an 11b two-step pipelined ADC consisting of 8b coarse and 5b fine (with 2b over-range) SAR sub-ADCs, which resolve 2b and 1b per SAR conversion cycle, respectively. Two ZX signals (or dual-residues) in opposite polarities automatically available in each 2b SAR cycle are sampled and held at the end of the coarse conversion for use as the full-scale (FS) reference for the fine SAR that quantizes a fixed input of zero. An on-chip foreground offset calibration circuit is proposed and implemented to correct the offset mismatch in the dual residues. Simulation and measurement results are provided to demonstrate the operation and performance of the proposed ADC architecture.

This work also discussed the continuous time analog low pass filter which is usually placed in front of ADC to prevent aliasing. Operational transconductance-C filter and active-RC filter are explored and designed. The simulation and measurement results are provided to demonstrate the functionality and performance.

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List of Abbreviations

ADC	Analog to digital Converter
SAR	Successive approximation register
ZX	Zero-crossing
DAC	Digital to analog converter
CDAC	Capacitive digital to analog converter
RA	Residue Amplifier
ZCD	Zero-crossing detection
DA	Dynamic amplifier
FS	Full scale
ENOB	Effective Number of Bits
INL	Integral Non-Linearity
DNL	Differential Non-Linearity
SFDR	Spurious Free Dynamic Range
SNR	Signal to Noise Ratio
SNDR	Signal to Noise and Distortion Ratio
SINAD	Signal to Noise and Distortion
FET	Field Effect Transistor
MOS	Metal Oxide Semiconductor
CMOS	Complementary Metal Oxide Semiconductor

FoM	Figure of Merit
LSB	Least Significant Bit
MSB	Most Significant Bit
DFF	D-Flip-Flop
LPF	Low Pass Filter
SFG	Signal-Flow-Graph

Chapter 1 Introduction

1.1 Background and Motivation

As pipelining [1-3] being widely used in SAR ADCs to overcome the speed and resolution bottlenecks [4-22], issues associated residue generation and amplification for high-resolution (≥10b) pipelined ADCs come back to plague SAR ADC designs; and as a result, power efficient and technology friendly residue amplifiers (RA) continue to be a focus of research. In the past, zero-crossing detection (ZCD) based RAs [23-24] were explored to eliminate the need for accurate and power-hungry settling of closed loop op-amps. Recently, open-loop dynamic amplifiers (DA) [16] and inverter-based ring-amps [26] have become popular for minimizing RA power consumption and improving technology scalability, where residue gain calibration and reference sharing across pipeline stages are used to align the residue full scale (FS) with the succeeding fine quantization FS.

This work employs a dual-residue architecture where the alignment is automatic. The first attempt in this direction was made with an interpolation based dual-residue architecture [23]23], within where the fine quantizations are carried out with interpolations between two adjacent coarse residues of opposite polarities. Since the difference of the dual residues determines the fine interpolation range, the residue FS and fine quantization FS are inherently aligned irrespective of the residue gain as long as it is the same for the two residues. Gain mismatch between the dual residues causes signal-dependent variation in the residue difference and should be limited within

one LSB of the fine quantization. Even though this matching requirement can be readily met with integrated-circuit RA replicas for identical residue inputs, it imposes a challenge to the RA linearity as the two RA inputs could differ by as much as the ADC input FS. It is for this reason that the dual-residue architecture has not gained the expected popularity, though it was revisited recently for design of a calibration-free pipelined ADC [24].

Fortunately, the linearity issue can be mitigated using coarse SAR sub-ADCs that can generate arbitrarily small residues with increasing SAR cycles. Based on this important observation, dual-residue SAR ADC architectures have been proposed [27-29]. This work details the design and operation principles using an 11b two-step pipelined dual-residue ADC as example that removes both the accuracy and linearity bottlenecks for residue amplification.

1.2 Organization of the Dissertation

The remainder of the dissertation is organized as follows. The overview of the ADC architecture is presented in Chapter 2, where the basic building block of SAR ADC are explained, it also briefly discussed pipelined SAR ADC and its limitations. Chapter 3 introduces the dual residue concept and addresses how it can be extended into SAR ADC operation, a high-level analysis of the impact on the dual residues from non-idealities including noise, nonlinearity, gain mismatch and offset mismatch are illustrated. Based on such foundation, in Chapter 4, a ZX based dual residue pipelined SAR ADC architecture is proposed and presented. Chapter 5 details the implementation of the proposed ADC, the sub blocks including coarse ADC, pipeline stage and sub ADC are illustrated. A proposed switch scheme which benefits the SAR operation in the coarse ADC is also explained. Chapter 6 addressed the offset correction and detailed the implementation of an automatic calibration loop. Chapter 7 demonstrated a 400MS/s 11b ADC prototype in 45nm

SOI CMOS based on simulation results and measurement results of a 250MS/s 10b ADC prototype in 45nm SOI CMOS. Chapter 8 presents the design of low-pass filter which can be used as anti-aliasing filter for sampling system. Chapter 9 summarized this work and proposed future work.

Chapter 2 Overview of Pipelined SAR ADC

2.1 Overview of SAR ADC

To convert an analog signal to digital codes, an N bit ADC needs to sample the signal first and then quantize the signal based on 2^{N-1} uniformly distribution thresholds with its size determined by full scale. Each threshold corresponding to one digital code. The searching for signal and its closet thresholds is called quantization. For a conventional SAR ADC, the quantization process is done by binary searching as shown (use 4bit as an example) in figure 2.1, the full scale is defined by the $2V_{ref}$ and the searching process begins by comparing the input V_X and the half thresholds which is at the middle – 0, it finds out the input is lower than the threshold and then generates 1 as the most significant bit (MSB) and continues to the next search at ¼ of FS at $0.5V_{ref}$ and generate 0, the process then repeats two times and resolves the rest bits. As clearly shown in the figure 2.1, there is still a small Δ after the least significant bit (LSB) is resolved and it is called quantization error or residue. The residue is due to fact that the ADC resolution is finite and for an N bit ADC it should be less than $V_{FS}/2^N$ which is equal to the size of LSB.

The building blocks of SAR ADC is shown in figure 2.2, the input signal V_X is sampled by the sampling switch and held as V_s seen by the Capacitive DAC (CDAC), a SAR logic controls the CDAC and generates the voltage V_1 that is the difference between V_s and 0 (assume the

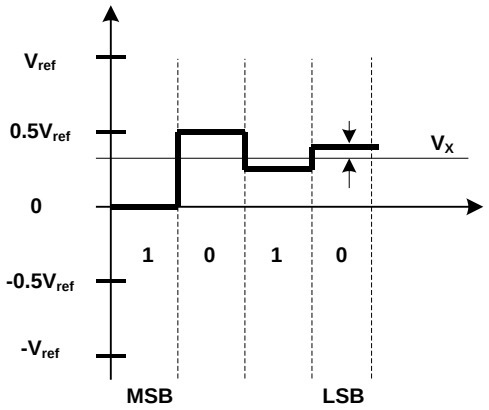


Figure 2.1 A 4bit quantization binary searching process

middle threshold is 0 in the 1st cycle), V_1 is then sent to the comparator and generates 1 or 0 which is used by the SAR logic to generate the next threshold, the process repeats as mentioned above until all the bits are resolved.

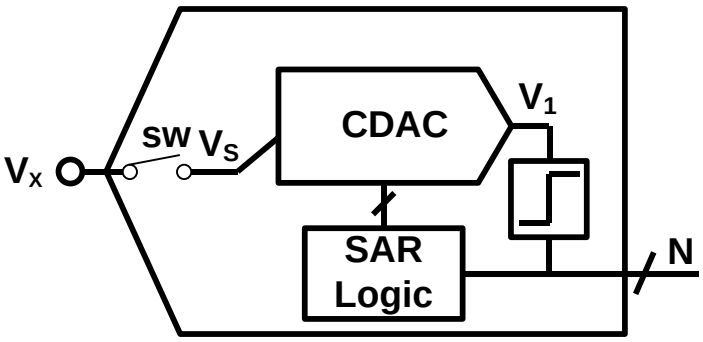


Figure 2.2 Simplified block diagram of SAR ADC

The CADC is one of the key building blocks in SAR ADC and a 4bit implementation for bottom plate sampling is shown in figure 2.3. The input V_x are connected to the CDAC top plate by multiple switches and the sampling is done by switching off the switches controlled by Φ_1. The signal is sampled across the capacitors and it appears at the bottom plate by switching the reference switches connected to V_{refh} and V_{refl} to reference common mode meaning half of the capacitor weighting is connected to V_{refl} and other half is connected to V_{refh}.

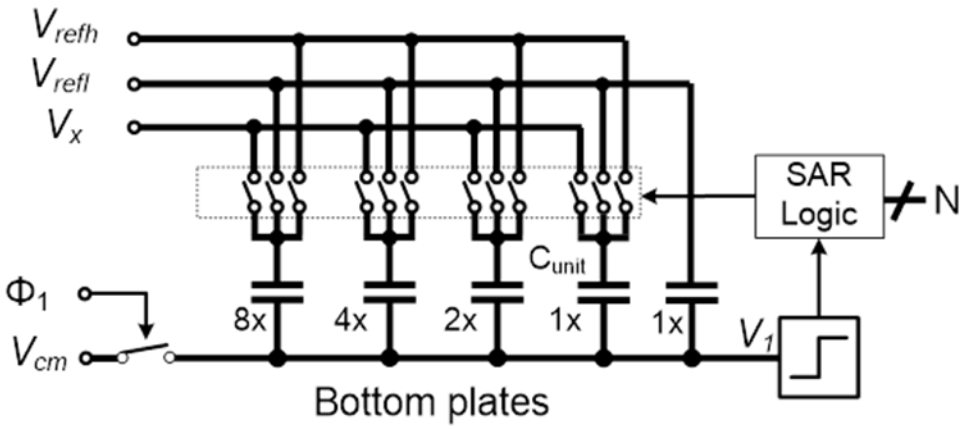
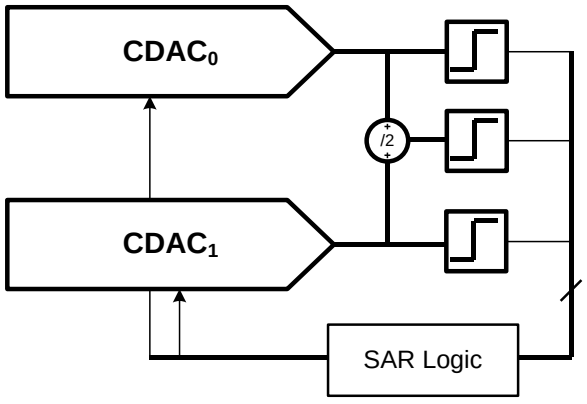


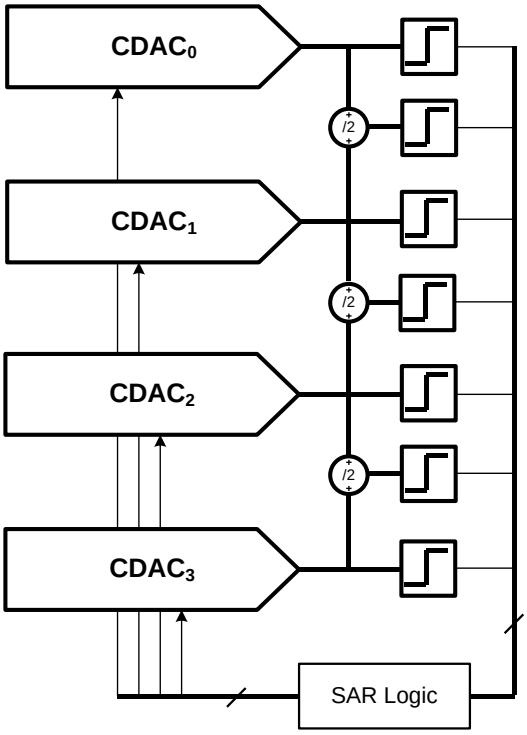
Figure 2.3 An implementation of 4bit CDAC

The CDAC consists of an array of capacitors, the smallest cap C_{unit} has the weighting of 1x and the other caps has the weighting of 2x, 4x and 8x. This radix 2 weighting arrangement allows the SAR ADC to perform binary search by toggling the reference switches connection through the SAR logic whose control is given based on the output of comparator.

One bit is resolved in each cycle when using one CDAC in traditional SAR ADC. To speed up the conversion, multiple CDACs [31] can be employed to generate evenly distributed ZX signals at the same time. For N bit/cycle conversion, 2^N-1 comparators are also needed in order to detect the ZX signals in parallel. As shown in figure 2.4(a), a minimum of two CDACs are needed to achieve 2b/cycle conversion, the two CDACs generate their corresponding ZX signals directly and the middle ZX signals can be derived from the interpolation of them. Similarly, a 3b/cycle SAR needs a minimum of four CDACs as shown in figure 2.4(b), seven comparators are used to resolve the ZX signals simultaneously. In theory, more bits/cycle can be done by utilizing more CDACs and comparators. But the exponential growth of power and area makes them less attractive and often impractical in implementation when more than 3b/cycle is needed.



(a)



(b)

Figure 2.4 Simplified diagram of 2b/cycle SAR ADC (a) and 3b/cycle SAR ADC (b)

2.2 Pipelined SAR ADC

Pipelining **Error! Reference source not found.**[1-3] has always been a method to increase the conversion speed of ADC and it has been employed recently to enhance the throughput of SAR ADCs as well [4-22]. Figure 2.5 shows a conceptual diagram of the two-stage pipelined SAR ADC. The input V_x is sampled to coarse stage SAR ADC1, after the it finished its conversion the residue V_1 is amplified by RA stage and feed into the substage SAR ADC2. The SAR ADC2 repeats the same SAR operation and resolve the rest LSBs. The timing required the two stage SARs and the amplification time required by RA are often designed to balanced. With the help of gain provided by RA stage, the design requirement of SAR ADC2 is often relaxed.

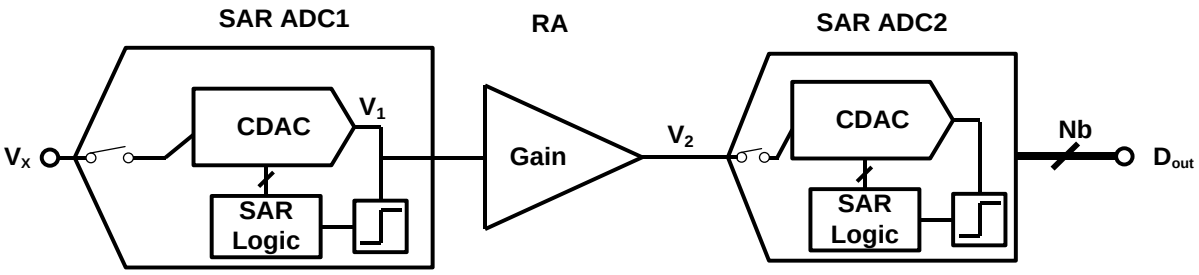


Figure 2.5 Conceptual diagram of two stage pipelined SAR

There are three variables involved in this design, the reference voltage of SAR ADC1 which defines the full scale of coarse stage, the gain of the RA and the reference voltage of SAR ADC2. Since its operation is similar to traditional pipeline ADC, the residue V_2 needs to be accurate before passing to the next stage, which indicates the alignment needs to be done among those stages. This alignment is usually achieved by high gain high bandwidth op-amp, trimming and complex calibration [1,19]. The additional residue signal processing compromises the SAR ADC advantages in power efficiency, design simplicity, and technology portability.

Chapter 3 Dual Residue Pipelining

3.1 Dual Residue Introduction and Extension

Residues are ideally linear zero-crossing (ZX) signals $v_i(v_x - V_i)$ [30] that cross zero ($v_i = 0$) when the input v_x equals the quantization threshold V_i with the ZX slope equal to the residue gain A, i.e., $v_i = A*(v_x - V_i)$. For an n-bit dual-residue ADC with N+1 quantization thresholds V_i (i = 0, 1, …, $N = 2^n$) the interpolation starts (as shown in Fig. 1) with generation of the two extreme ZX signals

$$v1_0 = A*(v_x - V_{refl}) \tag{3.1}$$

and

$$v1_{N1} = A*(v_x - V_{refh}) \tag{3.2}$$

by two replica RAs in the n1-bit first stage ($N1 = 2^{n1}$), where the ADC reference voltages $V_{refl} = V_0$ and $V_{refh} = V_N$ set the ADC input full-scale $FS = V_{refh} - V_{refl}$. By resistive interpolation between $v1_0$ and $v1_{N1}$, the ZX signals $v1_j$ (j = 1, 2, …, N1 – 1) for the coarse quantization are generated at

the (N1– 1) taps across the first stage resistor string. The polarities of the ZX signals $v1_j$ are detected in

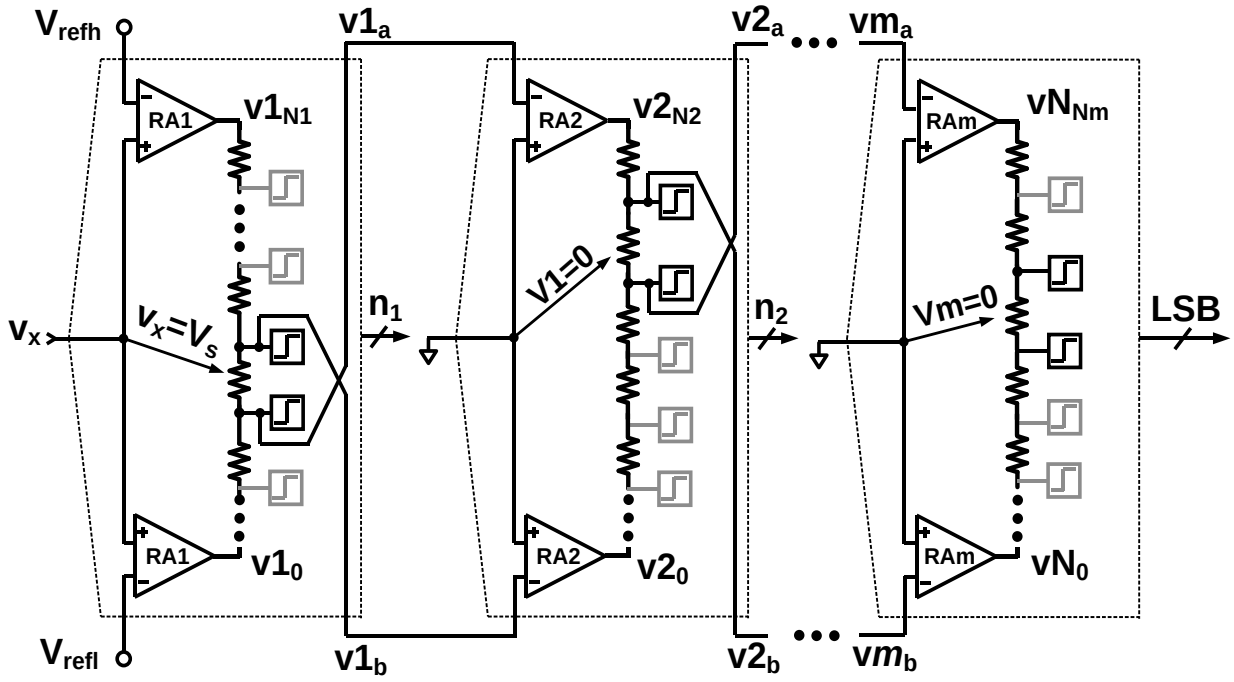


Figure 3.1 The schematic of an interpolation based dual-residue ADC [23]

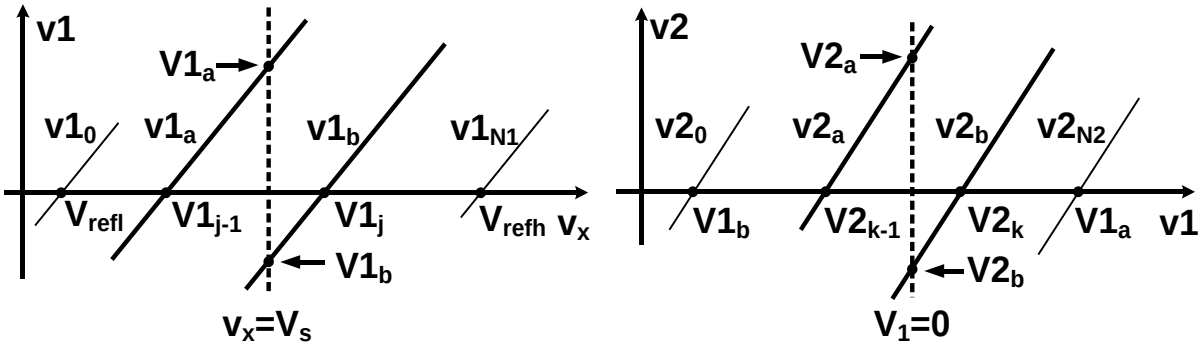


Figure 3.2 The residue signals in the first two stages of the sub-ADCs

parallel with regenerative latches for a given input sample $v_x = V_s$ to identify the string section that contains the zero of the first-stage string voltage v1. The two identified ZX signals, $v1_b = v1_j$ and $v1_a = v1_{j-1}$ that encompass the zero are amplified by the second stage RAs to drive the second stage string for fine quantization. The interpolated fine ZX signals $v2_k$ (k = 1, 2, …, N2 – 1, where N2 = 2^{n2}) and the fine dual residues $v2_a$ and $v2_b$ are generated in the second stage for the third-stage interpolation and quantization, and so on.

The first-stage RA (RA1) output must meet the highest (n-bit full resolution) linearity requirement over the full-scale input range. The second-stage linearity requirement can be relaxed by increasing the coarse resolution (n1), but to a limited extent constrained by the exponential growth in complexity, power, and input capacitance of the parallel interpolation based coarse sub-ADC. The RA linearity requirement and coarse sub-ADC complexity tradeoff can be avoided in principle using serial interpolation for efficient coarse quantization. This is possible based on an important observation that the flash-type sub-ADC stages in figure 3.1 can be black-boxed and substituted with any other types such as SAR ADCs as shown in figure 3.2, where the fine residues are generated by serial interpolations between the references for each stage. The first stage sub-ADC takes input signal v_x with the references connected to external sources. Starting the 2^{nd} stage, the sub-ADC inputs are set to zero while the reference pins are connected to the dual residue outputs of the preceding stage.

In figure 3.2, the required dual residues are readily available from the three parallel ZX signals generated for the 2b/cycle conversion [29]. The costly RAs in the first stage of figure 3.1 are now replaced with two fixed voltage reference buffers without linearity requirement. The RA overheads of the following stages are drastically reduced by increasing the number of coarse SAR cycles so that the dual residues are arbitrarily small and linear without worsening the coarse sub-

ADC complexity. As for the last stage without the need to generate the dual residues, a 1b/cycle SAR is better choice, because only one comparator offset needs to be calibrated. The INL degradation by coarse comparator offsets can be avoided by over-ranging the succeeding fine stage.

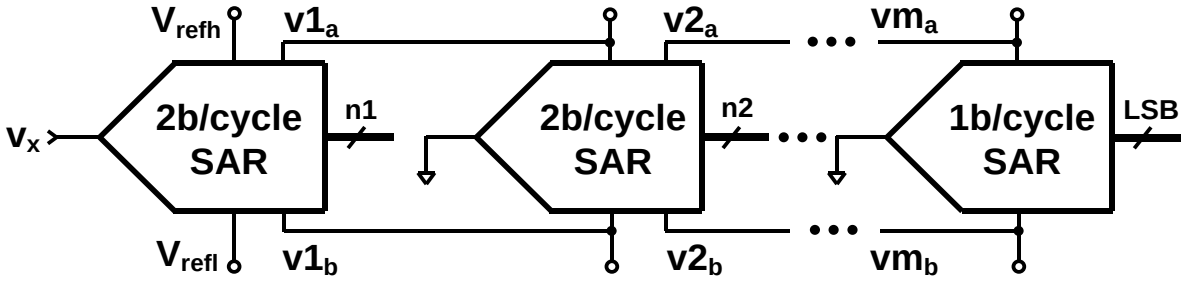


Figure 3.3 Dual residue ADC architecture extended to use SAR sub-ADCs

With the RA accuracy and linearity bottlenecks both removed, the pipelined dual-residue SAR ADC preserves the ZX-only operation and power efficiency of SAR ADCs. In addition, sub-ADCs operating in different signal domains can be exploited with little concern about the accuracy of signal conversions, say, from the voltage to the time domain [32] and vice versa. The resulted sub-ADC modularity thus opens a new dimension for design of pipelined ADCs.

3.2 Dual Residue Error Due to Circuits Non-idealities

As mentioned in Chapter 2.2, for a traditional pipelined SAR ADC the residue needs to be accurate in terms of absolute value. The ZCD based operation dual residue pipelined SAR relaxed

the absolute residue accuracy by relying on the matching between the two residues. In the real implementation, the matching can degrade due to circuit non-idealities including nonlinearity of buffering, amplification, gain mismatch, noise and offset mismatch [23-24]. The residue generation and the interpolation in SAR is fairly accurate due to its mostly digital operation and the inherent decent linearity comes with the properly sized CDAC. The pipeline stage as shown in figure 3.8 usually dominates those error sources because of the usage of active devices.

To evaluate the impact comes from the nonlinearity the transfer function of the pipeline stage can be generalized as

$$v2_0 = \alpha_1 v1_a + \alpha_3 {v1_a}^3 \tag{3.3}$$

$$v2_{N2} = \alpha_1 v1_b + \alpha_3 {v1_b}^3 \tag{3.4}$$

where $v1_a, v1_b$ and $v2_0, v2_{N2}$ are the input and output correspondingly, α_1 and α_3 are the coefficient associated with the fundamental and third order harmonics, the 2nd order is not considered here because of the differential operation, higher order harmonics is not considered since their contribution is low thanks to the substantial reduction of residue amplitude by 8-bit of coarse SAR. Another assumption is the non-linear characteristics are the same between the two RA1s and RA2s since their designs are identical.

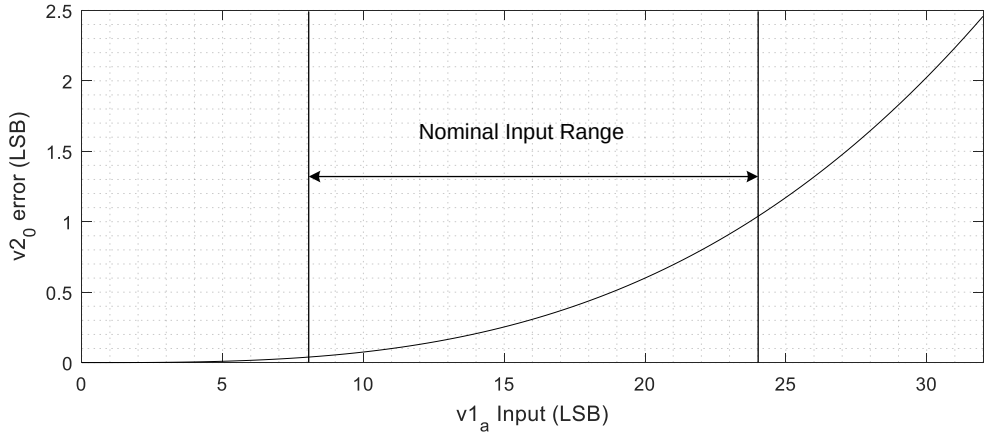


Figure 3.4 A transfer function example of the nonlinear pipeline stage - $v2_0$ error vs. $v1_a$

The ZX based operation relaxed the linearity requirement of RA1 and RA2 as illustrated below. Figure 3.4 shows an example of a transfer function example of the output nonlinear behavior of pipeline stage for a 5b sub ADC, assuming the proposed ADC coarse stage only uses +/- 4 LSBs so the input range of pipeline stage is from 8-LSB to 24-LSB as shown below, the output of pipeline stage produces 1 LSB error. And the error grows to 2.5 LSB when the full range is used. The ZX location can be derived by comparing the ideal case to the condition defined by Eq. (3.4) and (3.5), the ZX error in LSB can be described as

$$\Delta ZX = \frac{-\frac{\alpha_3}{\alpha_1} v1_a\left[(v1_a - v1_b)^2 - 3(v1_a - v1_b)v1_a + 2{v1_a}^2\right]}{1+\frac{\alpha_3}{\alpha_1}\left({v1_a}^2 + v1_a v1_b + {v1_b}^2\right)} \tag{3.5}$$

Based on Eqs. (3.5) the ZX error can be observed in figure 3.5, as clearly shown in the figure, the max error becomes less than 0.25 LSB when the input is in the same nominal input range as described previously.

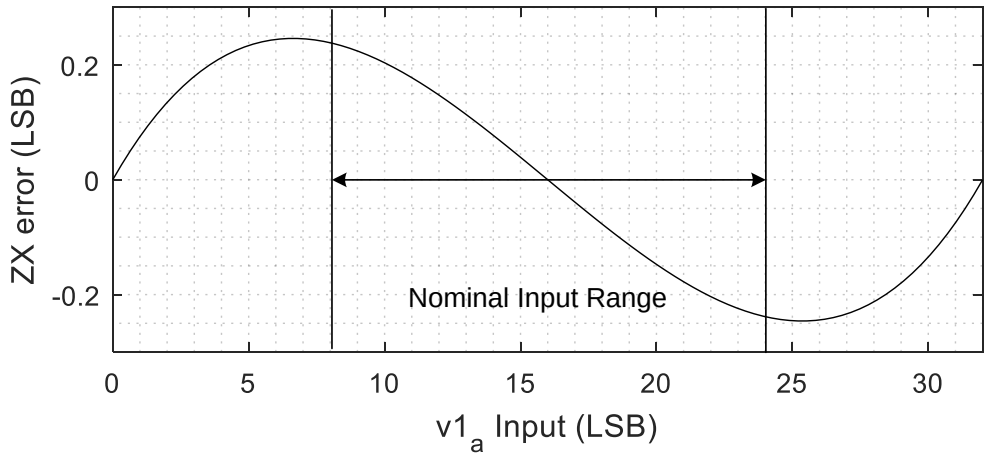


Figure 3.5 ZX error for the given nonlinearity show in figure 3.4

The ZX error also shows some interesting characteristics, the error becomes zero when the input is at its extreme ZX location – 0, 32 LSBs and in the middle code – 16 LSB. This can be understood intuitively, when the input is at either side of the boundary, the linearity is dictated by the AMP which imposes the largest weighting in the interpolation. Thus, the linearity is very good given the smallest input at those conditions. When the ZX location is in the middle, both amplifiers produce exactly the same nonlinearity since the amplitude to both amps are the same (only the polarity is the opposite), therefore the ZX location is still in the middle at the output which gives zero error.

Another ZX error can come from pipeline stage is the gain mismatch between two residues, the gain mismatch can be expressed as shown below by Eqs. (3.6) and (3.7)

$$v2_0 = \alpha_1(1 + G_\Delta)v1_a \tag{3.6}$$

$$v2_N = \alpha_1(1 - G_\Delta)v1_b \tag{0.3}$$

where G_Δ is the gain mismatch, the ZX error due to gain mismatch can be derived as

$$\Delta ZX = \frac{-2G_\Delta v1_a v1_b}{[(1+G_\Delta)v1_a-(1-G_\Delta)v1_b](v1_a-v1_b)} \tag{3.8}$$

Based on the Eqs. (3.8) the ZX error vs ZX input $v1_a$ is shown in figure 3.6 for 5% mismatch case, the gain error generates a DC component that doesn't contribute non-linearity in the final ADC output thus it is removed from the plot. For amplifier with 5% gain mismatch the 5b sub ADC will generate error larger than 1LSB if only one amplifier is used and the error goes down to less than 0.6LSB in interpolation-based operation.

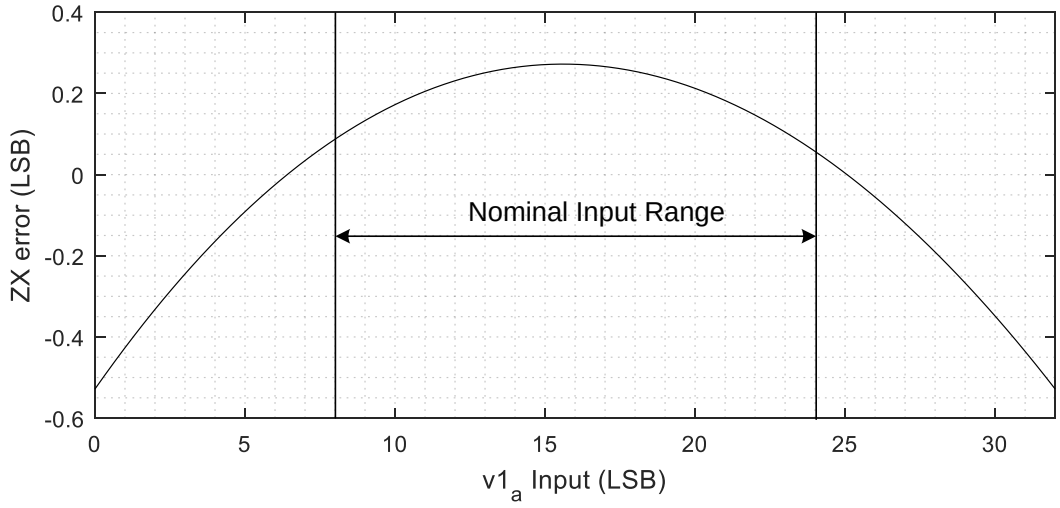


Figure 3.6 ZX error vs $v1_a$ due to gain mismatch

Since the noise of two amplifiers are uncorrelated, the noise from the two amplifiers have different impact on the ZX location compared to the influence on absolute value from a single amplifier. The impact can be express as in Eqs. (3.9) and in figure 3.7.

$$NC = \frac{{v1_a}^2 + {v1_b}^2}{(v1_a - v1_b)^2} \tag{3.9}$$

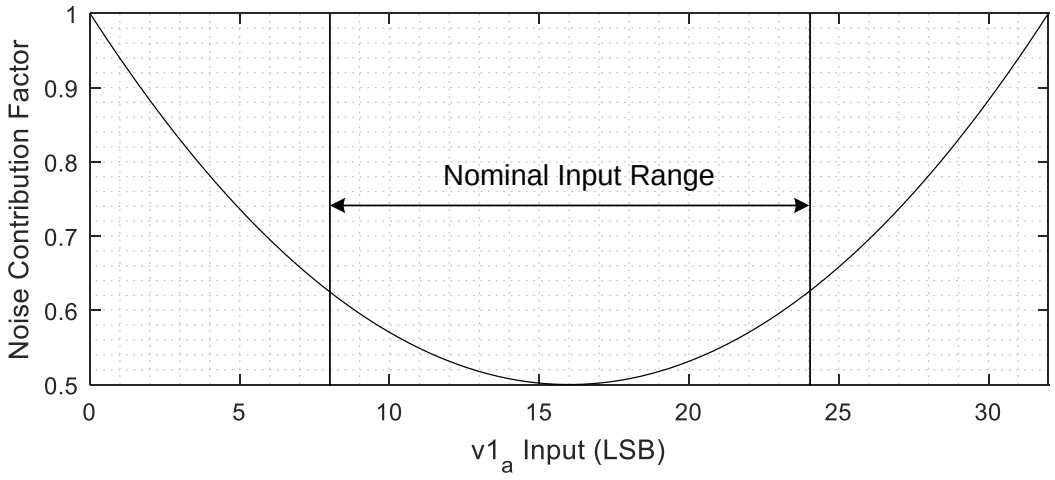


Figure 3.7 Noise contribution factor vs $v1_a$

As show in figure 3.7, the noise contribution factor is halved when the input is in the middle simply because half of the noise averaged out when the weighting from two amplifier are identical. When the ZX is in the extreme locations, the noise contribution factor is 1 because the weighting from the other amplifier is zero and the ZX sees the whole noise generated from one amplifier.

The offset mismatch (differential offset) also needs to be considered as it directly moves the ZX location. Assume v_{os} is the differential offset between amplifiers in the pipeline stage the output can be expressed as

$$v2_0 = \alpha_1 v1_a + v_{os} \tag{3.10}$$

$$v2_N = \alpha_1 v1_b - v_{os} \tag{3.11}$$

The ZX error can be derived as in Eqs. (3.12) and assumes 2LSB differential offset and error is shown in figure 3.8.

$$\Delta ZX = \frac{-v_{os}(v1_a+v1_b)}{(v1_a-v1_b)(v1_a-v1_b+2v_{os})} \tag{3.12}$$

The ZX error is zero when the input in the middle as the interpolation weighting from the two amplifiers are identical such that the differential offsets moves the ZX to the opposite direction by the same amount. The error grows as the input moves away from the center as the offset contribution from one amplifier starts to dominate. The first amplifier in the pipeline usually contribute most of the offset as the following stage contribution can be attenuated by first stage gain. Sizing up the first amplifier input transistor reduces the offset mismatch, but the area occupation could become unrealistic to achieve the accuracy needed in the proposed ADC. A calibration scheme discussed in Chapter 6 addressed this issue.

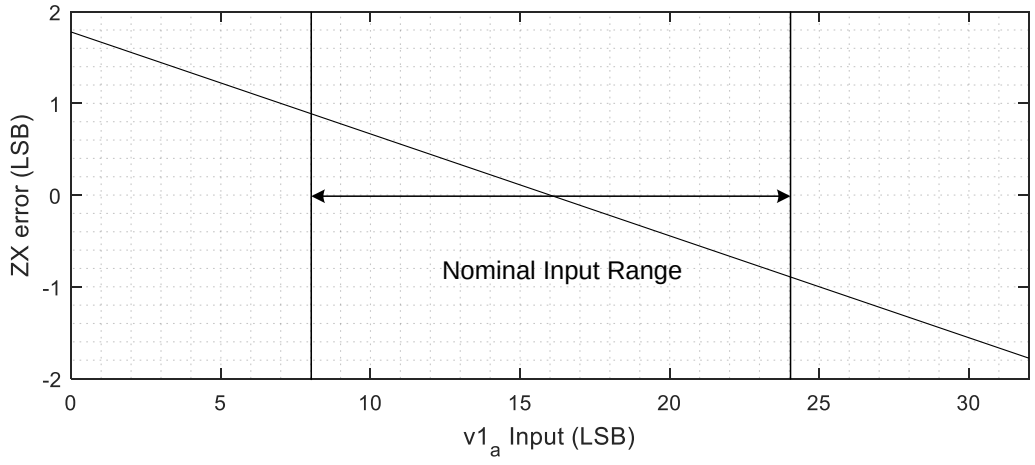


Figure 3.8 ZX error due to offset mismatch

Chapter 4 Architecture of Proposed Zero-Crossing Based Dual-Residue Pipelined SAR ADC

4.1 Architecture Overview and Operation

The proposed zero-crossing based dual-residual pipelined SAR ADC architecture [29][29] and the operation timing is shown in figure 4.1. It consists of three stages, the first stage is 2b/cycle 8b SAR ADC and it can readily generate dual residues at the end of the conversion because the usage of two CDACs - $CDAC_a$ and $CDAC_b$. The 2^{nd} stage is the pipeline stage which is used to sample the dual residues available at the coarse ADC CDACs and hold it for the conversion in the next stage, the pipeline stage has two of amplifiers $AMP_1$and AMP_2, between the two amplifiers there are the sampling switch and sampling capacitors. The 3^{rd} stage is the sub-range ADC consists of a 1b/cycle SAR, the input of this SAR ADC is the differential zero which represents the ZX location. The references are the output of AMP_2 in pipeline stage and SAR operation of this stage will perform the interpolation of the references to locate the ZX location.

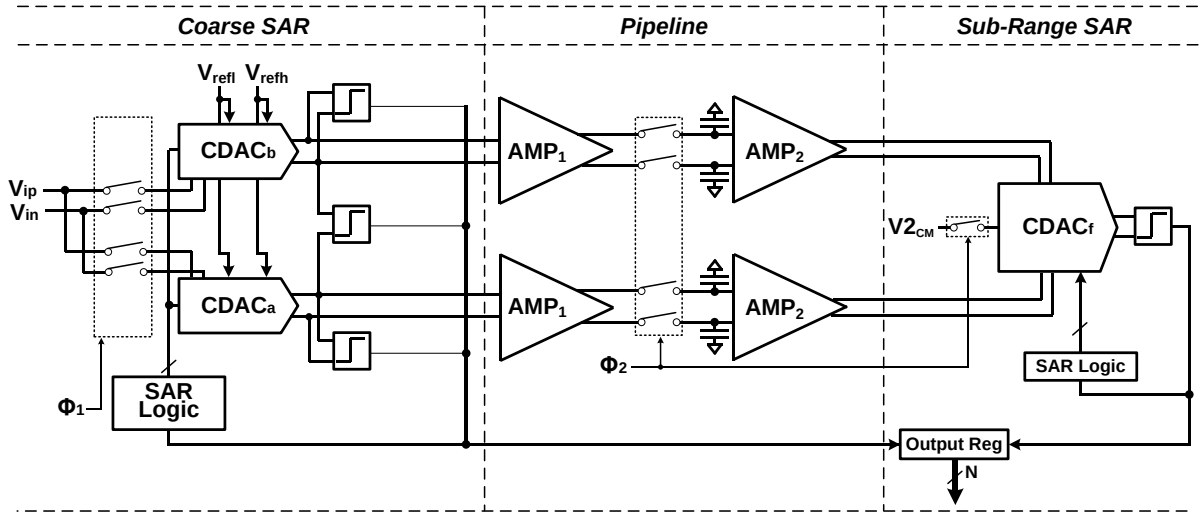


Figure 4.1 The proposed zero-crossing based dual residue pipelined SAR ADC

4.2 Coarse 8b SAR ADC

The coarse ADC is the first stage of the pipelined ADC and it needs to meet the overall linearity and noise requirement of the entire ADC. The block diagram of the coarse ADC is shown in figure 4.2. The SAR ADC architecture is chosen as the first stage due to its power efficient operation since it resolves the input by performing ZX searching in digital fashion. For better linearity performance the coarse ADC tracking switch is bootstrapped [36] and bottom plate sampling is used to remove the signal dependent charge injection as it is a common limitation of linearity from top plate sampling. Two identical capacitor DACs, $CDAC_a$ and $CDAC_b$ – $CDAC_a$ and $CDAC_b$ are used so the dual residues

can be generated automatically at the end of the conversion. With the help two CDACs, two bits can also be resolved in each conversion as long as three thresholds can be generated during conversion. The first and third thresholds are readily available at each of the CDAC, $CMP1_b$ and

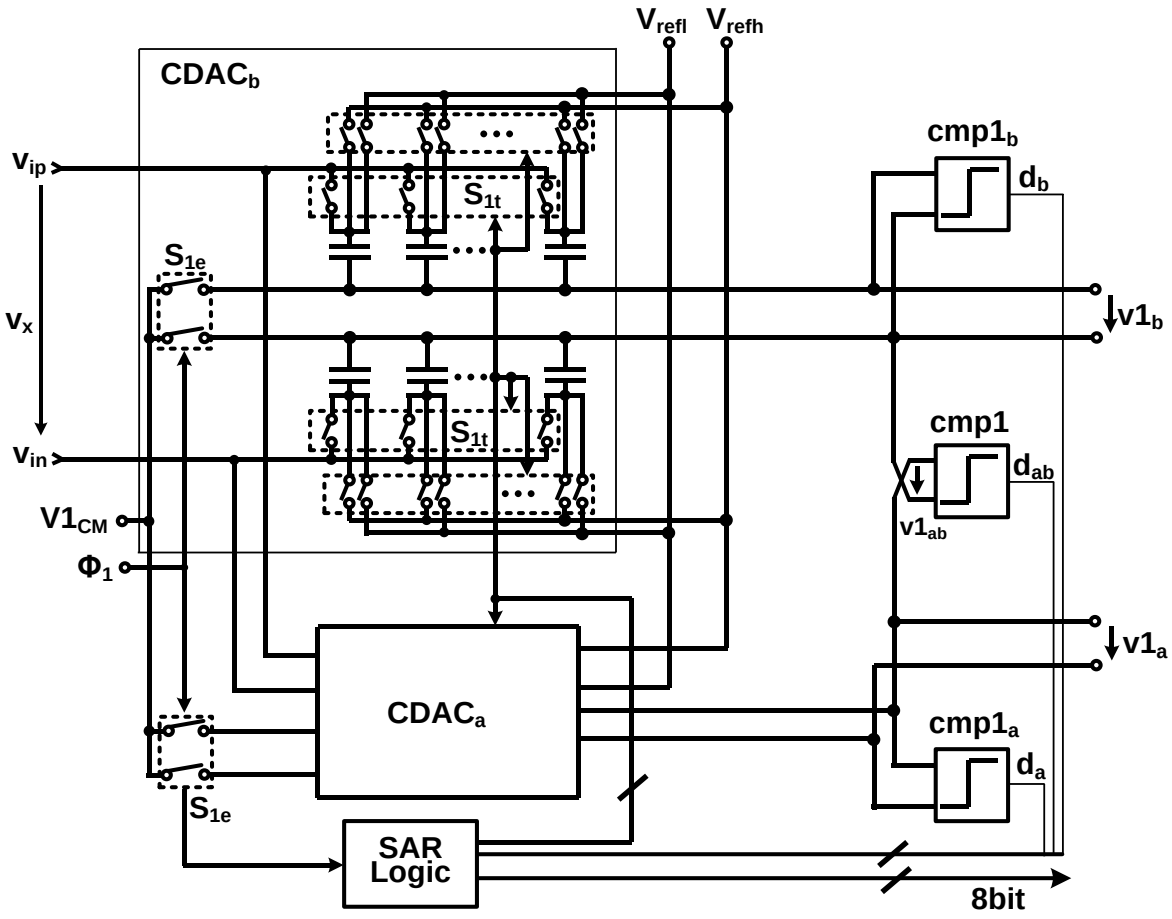


Figure 4.2 The block diagram of the coarse 8b SAR ADC

$CMP1_a$ are used to detect the ZX of those two thresholds. The third threshold can be extracted by feeding the single ended signal with opposite polarity from each CDAC and it will be detected by the CMP1.

The operation of the coarse 8b SAR ADC is the following, during track phase ($\Phi 1 = 0$) as shown in figure 4.2 the S_{1e} and S_{1t} are closed to allow $CDAC_a$ and $CDAC_b$ to track the differential input signal $v_x = v_{ip} - v_{in}$. To perform bottom plate sampling the switches S1e are opened slightly earlier than the input top-plate switch S1t, the sampled signal v_x is then held at the CDACs. In the

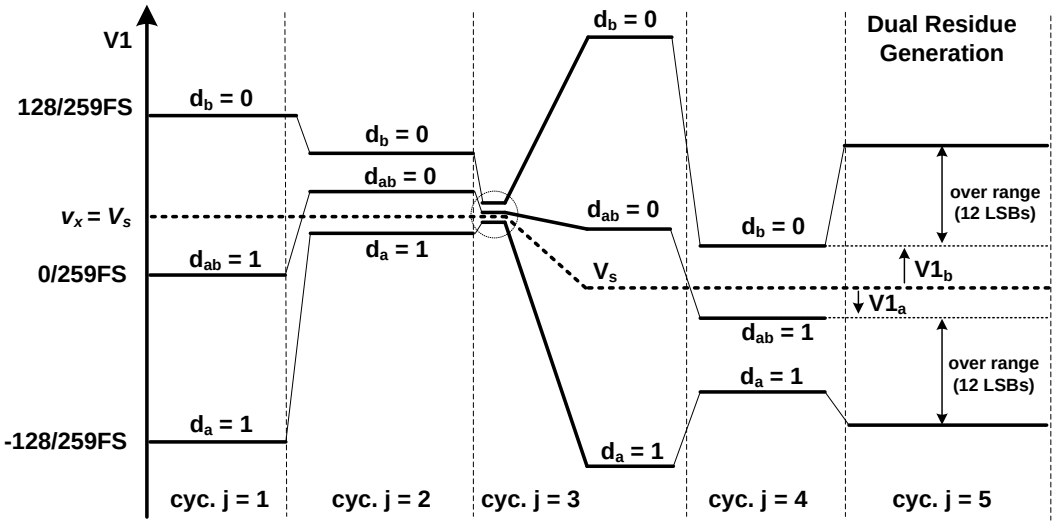


Figure 4.3 Coarse quantization thresholds generated in each conversion cycle for a given input sample $v_x=V_s$

coarse conversion phase B ($\Phi 1 = 0$), the $CDAC_a$ and $CDAC_b$ top plates are switched to either reference voltage V_{refl} or V_{refh} to generate the CDAC output ZX signal samples, on $CDAC_a$ $V1_a = -(V_s - V_{ja})$ is generated where on $CDAC_b$ it is $V1_b = -(V_s - V_{jb})$, V_{ja} and V_{jb} are the quantization thresholds produced by the CDAC during the j-th conversion cycle as shown in Figure 4.3. The quantization thresholds are generated by the connecting to references through the top-plate switches, the exact thresholds are determined by the corresponding CDAC weighting formed in

such connections. As mentioned previously, the third threshold also needs to be generated to perform 2b/cycle conversion and the third ZX sample $V1_{ab} = -(V_s - V1_j)$ is interpolated from v1a and v1b as shown in Figure 4.2. The three comparators cmp1a, cmp1b, and cmp1 detect the polarities of the corresponding ZX samples at the end of each 2b conversion cycle and determine the CDAC top-plate reference connections for the next cycle ZX sample generation. As shown in figure 4.3 after four cycles (j = 1 to 4) of conversion 8b are resolved as the MSBs and are retimed to the registers.

4.3 Dual Residue Generation and Interstage Over-range

After the coarse SAR enters cycle j = 5 in phase C ($\Phi_1 = 0$, $\Phi_2 = 1$) as shown in figure 4.3 the ZX samples $V1_a$ and $V1_b$ are generated as the dual residues for fine quantization. Noticed to generate $V1_a$ and $V1_b$ the coarse SAR doesn't need to move any reference switches as they appear naturally at the two CDACs top plate at the end of the cyc. j = 4. The rest LSBs can be determined by interpolating between $V1_a$ and $V1_b$, before they are sampled and converted in the sub-range ADC, a 2b over-ranging is introduced to correct errors during the coarse ADC conversion. The errors can be corrected by this over-range are the reference settling error, comparator kickback and random comparator offsets which are discussed next.

Even though the coarse SAR only needs to resolve 8b and ZX accuracy still needs to meet 11b requirement since the signal is not amplified before sampling. During coarse ADC conversion, the activities of reference switches inevitably introduce transient spikes or glitches due to circuits non-idealities such as parasitics on switches and finite bandwidth of reference buffers. Those are error sources and need to be settled and settling is determined by the finite switch resistance and

the CDAC size it is driven. To achieve less than half LSB error for an N-bit resolution ADC, it can be calculated as

$$e^{-\frac{t}{\tau}} \leq \frac{1}{2^{N+1}} \tag{4.1}$$

where τ is the time constant derived from switch resistance and CDAC size, it is clearly that t needs to be at least (N+1) * τln(2). For high speed SAR operation, after reference switches are toggled the comparator needs to make the decision as soon as possible to speed up the conversion, thus very little time is allocated between the switch event and the firing of comparator.

Thus, if the comparator decision is made based on incomplete reference settling the resolved ZX location could be wrong. In the example shown in figure 4.4(a), after the reference switch event at t_1, the reference was kicked and introduces some settling behavior shown during t_{r1} and generates wrong ZX value if comparator clock t_2 is triggered during this time region, this error will settled out in t_{r2} but this settling time could last too long which will have bigger impact on conversion speed, in real design, t_2 is often chosen to be close the end of t_{r1} and before t_{r2} to speed up conversion, therefore the decision is often erroneous.

Due to FET non-idealities, the devices in comparator are usually mismatched and thus presents an input referred offset usually dominate by comparator input stage as shown in figure 4.4(b). Unlike the incomplete settling error in references which eventually settles out, the offset directly applied to the signal. For 1/cycle SAR ADC, the offset only introduces a DC shift and is generally considered harmless. But for 2b/cycle or multi-bit per cycle SAR ADCs, multiple comparators are running in parallel during each conversion, the offset mismatch among those comparators can lead DNL errors, this error can be minimized by equipping offset calibration

circuits. As mentioned previously, the coarse ADC needs to meet 11b accuracy, the design and implementation of such calibration circuits become impractical. Another error from comparator input stage is the noise as shown in figure 4.4(b). Same as offset, the noise directly applied to the input signal and corrupt the ZX location, and power and input devices size could be way too large if the comparators noise needs to be designed to meet the 11b ADC requirement. For bottom-plate sampling ADC, larger comparator input device size also means bigger attenuation of input signal and thus degrades SNR.

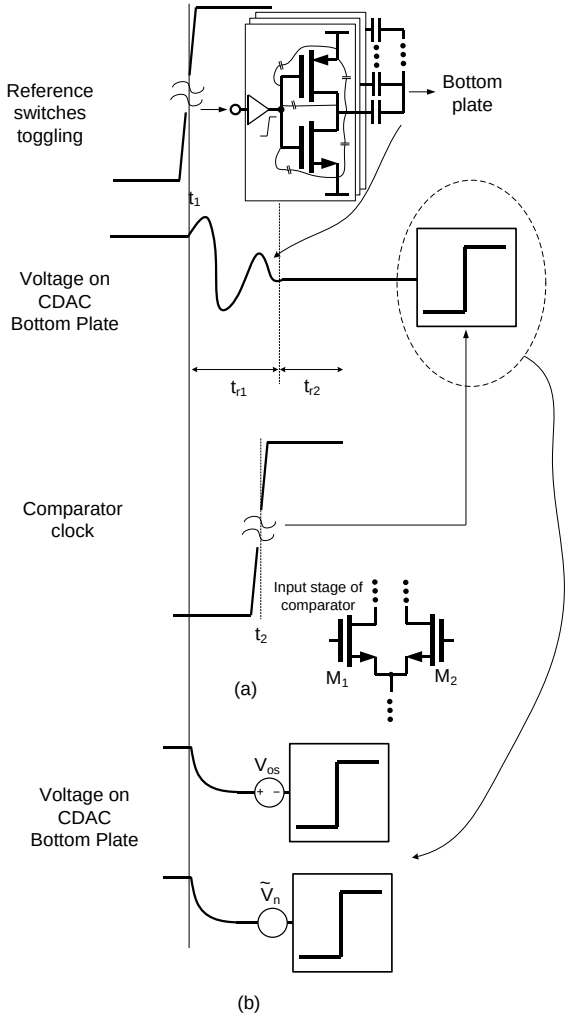


Figure 4.4 ZX error due to reference incomplete settling (a) and comparator offset mismatch and noise (b) during coarse ADC conversion

To tackle those challenges, a 2b over-range is introduced in cyc j = 5 as shown in figure 4.3. This extends the fine quantization FS from 8 LSBs to 32 LSBs, where one LSB = $2(V_{refh} - v_{refl}) /2^{11} \sim 0.6$ mV for the 11b prototype. This is realized by offsetting the ZX points that define the fine FS by –12 LSB and +12 LSB, respectively. The offsets are injected with a small auxiliary CDAC in each of $CDAC_a$ and $CDAC_b$. As a result, total tolerance for the coarse comparator offsets and the coarse CDAC incomplete settling increases by 24 LSBs or +/–6 mV. The offset mismatch between the two residue paths is corrected with auxiliary CDACs to be described in Chapter 6.

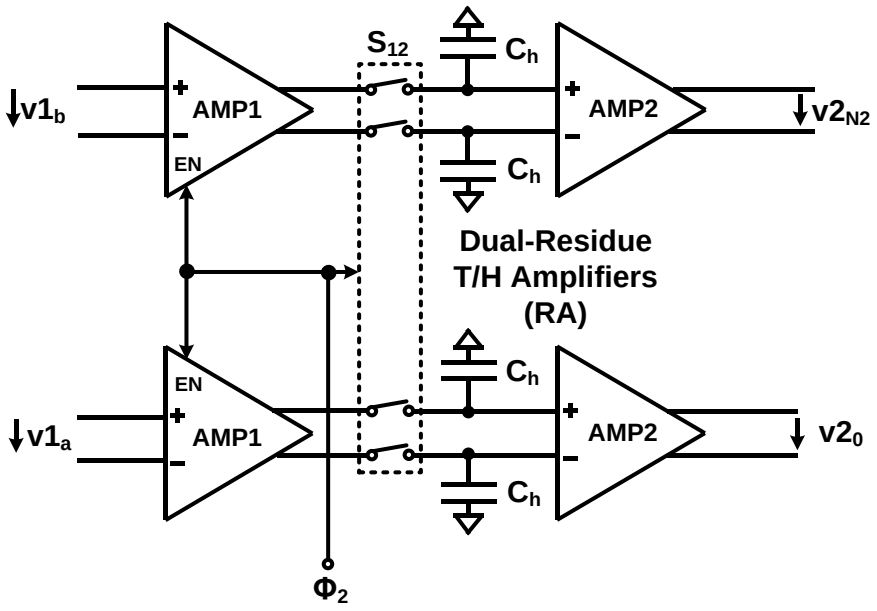


Figure 4.5 The block diagram of the pipeline stage

4.4 Pipeline Stage

The pipeline stage consists of sampling switches and capacitors, two stage of amplifiers AMP1 and AMP2 as shown in figure 4.5. The AMP1 received the $V1_a$ and $V1_b$ during sub ADC track phase D ($\Phi_2 = 1$) as shown in figure 4.7. The hold switch S_{12} is turned on and the amplified dual residues are stored on capacitor C_h. And then the S_{12} is turned off and the residues are held on C_h and get buffered/amplified to $v2_0$ and $v2_{N2}$ to the sub-range ADC. The gain of the AMP1 will help to relax the following stage design such as noise and offset. An EN signal allows the AMP1 to enter power down mode when not in use when $\Phi_2 = 0$ to save power. AMP2 mainly serves as buffer stage to provide driving strength to the following stage and also provides extra gain to further relax the design of sub ADC.

4.5 Sub 5b SAR ADC

The LSBs from dual residues $v2_0$ and $v2_{N2}$ can be resolved by searching the ZX and the SAR architecture is also the best candidate here due to its low power operation to perform interpolation. During sub ADC track phase D ($\Phi_2 = 1$), the fine $CDAC_f$ top plates and bottom plates connected to a differential ground $V2_{CM}$ and zero respectively, the reference switches are open and other sides are connected to $v2_0$ and $v2_{N2}$ as shown in figure 4.6. $V2_{CM}$ is set to match the AMP2 output CM to avoid CM jump at CMP_f input eliminating the need for low-impedance CM voltage source. The 1b/cycle fine conversion phase E ($\Phi2 = 0$) starts as $\Phi2$ falls, with the fine references $v2_0$ and $v2_{N2}$ sampled by S_{12} and held by C_h. Simultaneously, the $CDAC_f$ split-cap top plates are switched to $v2_0$ and $v2_{N2}$ by half and half, respectively, generating the first-cycle fine ZX signal $v2 = v2_1(v1 = 0) = –(0 – V2_1)$ at the $CDAC_f$ bottom plate output, where $V2_1 = (v2_0 + v2_{N2}) / 2$ is the first fine quantization threshold. The fine comparator CMP_f detects the ZX polarity resolving the fine MSB and switches one of the fine MSB split caps from 0 to 1 or 1 to 0 for fine

MSB = 0 or 1, respectively, generating the ZX signal for the second cycle conversion. This continues till the 5 fine bits are all resolved and the next tracking phase of the fine SAR starts.

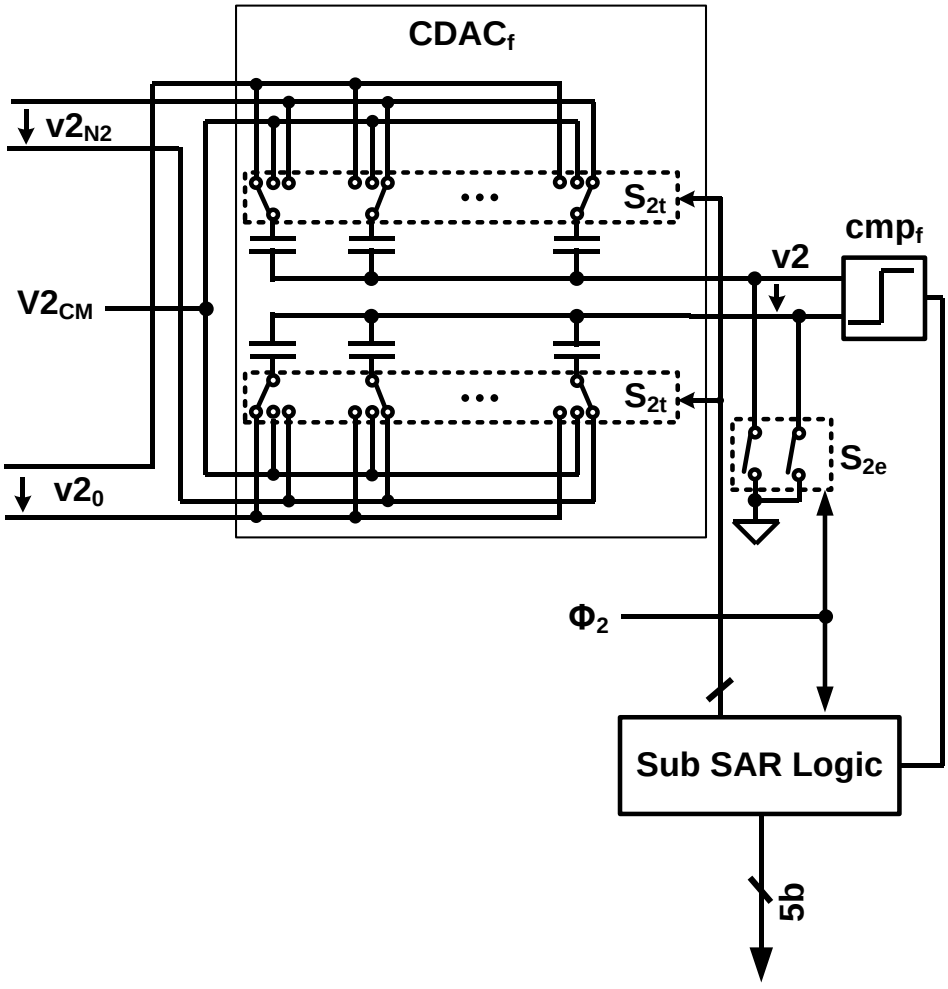


Figure 4.6 The block diagram of the 5b sub SAR ADC

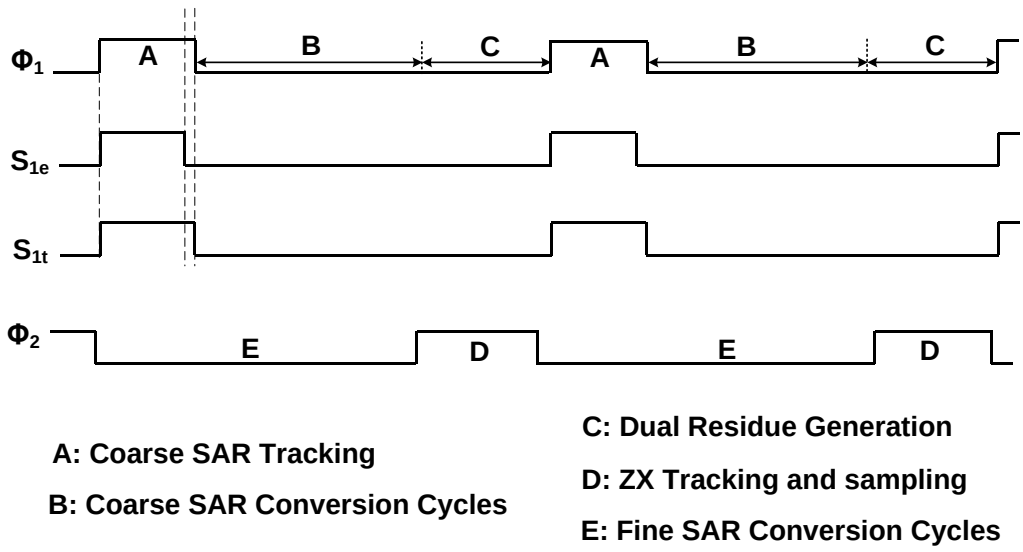


Figure 4.7 The timing diagram of the proposed ADC

Chapter 5 Circuit Implementation

5.1 Coarse SAR CDAC Array with Capacitor Splitting

One of the major building blocks in the coarse 8b SAR ADC is the differential CDAC. During the coarse ADC conversion, different thresholds are formed by switching the reference switches which consumes dynamic power and may introduce settling issues. Figure 5.1 shows the traditional 8b SAR with 2b/cycle CDAC setting when initialized during track phase. Two identical CDACs are used to generate three thresholds by different switch configuration. The single-ended CDAC consists of 256-unit caps due to 8b quantization level requirement.

To illustrate the way to generate three thresholds in conversion the entire CDAC is break into 4 Groups as indicated by Group 1, Group 2, Group 3 and Group 4. After initialized the caps in $CDAC_a$ in the Group 1 are connected to opposite polarity (in this example it is '1') of the rest caps differentially as shown in figure 5.1. The caps in $CDAC_b$ are initialized to the complementary configuration. The thresholds are generated as 128/256, -128/256 and 0 which is produced by interpolating between two CDACs. The MSB conversion is done by comparing the thresholds and the input using three comparators. The three comparators generate three outputs which in return to control each 64X of caps in Group 1 to prepare the next conversion. In the given example the cap switch configuration after MSB is shown in figure 5.2. By examining the switch configuration, it is clearly that in order to prepare the next conversion the Group 2 caps also need to be toggled to

complete the thresholds generation. The way the caps switched in Group 2 follows exactly the how the 64X caps are switched in Group 1 during initialization.

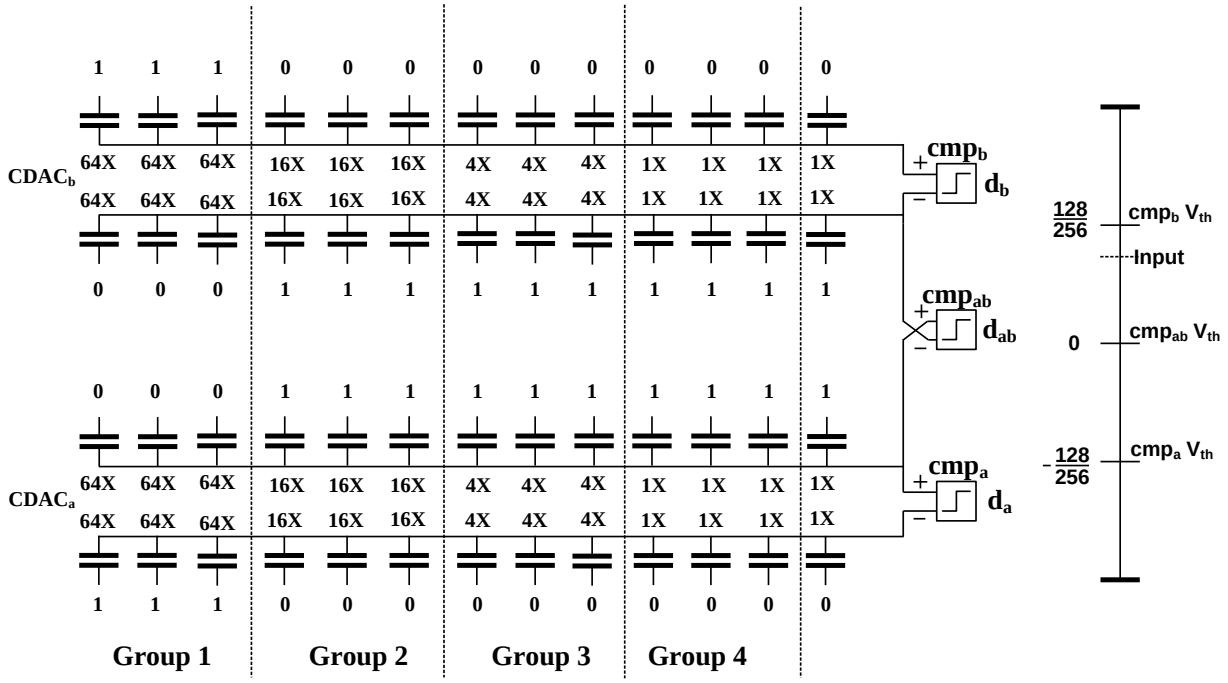


Figure 5.1 CDAC setting in traditional 8b SAR 2b/cycle switch scheme after initialization

This switching activity usually creates two problems, the first problem is the waste of switching energy and it can be intuitively seen that part of the caps switched to ‘1’ position while other caps switched to ‘0’. The charge transfer involved is the summation of both switching activity but the threshold change on CDAC is the net voltage change of them. The other problem it creates is often more detrimental. The toggling of the cap switches is often not aligned by design or due to layout constraints and it generate glitches when switching up (‘1’) and down (‘0’) are not

happened at the same time. Depends on the threshold change, it introduces overshoot or undershoot which might move the threshold in the opposite direction during CDAC voltage settling and it will create conversion error if the comparator is fired too soon. For high speed SAR ADC, the comparator is asynchronously clocked at very high speed and this problem is often more pronounced. There are a few ways to correct this error by introducing redundancy during conversion, however it is better to minimize this error and budget the redundancy to other non-idealities in SAR which are harder to correct.

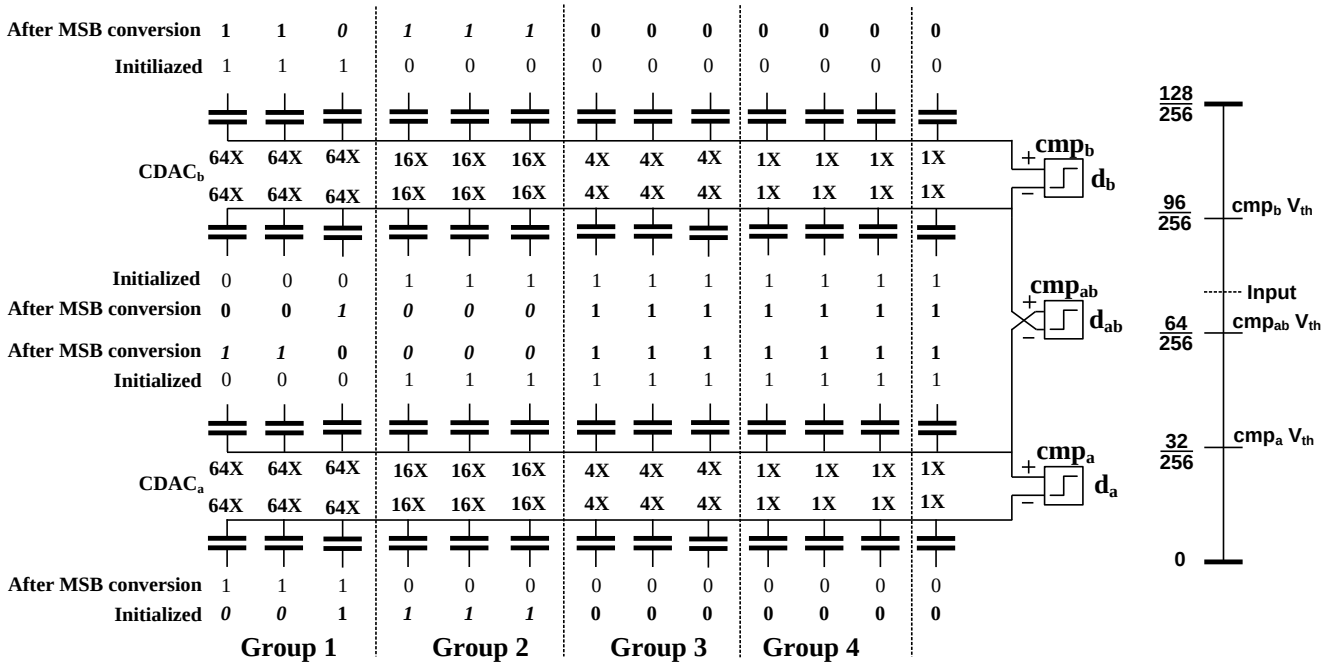


Figure 5.2 CDAC setting in traditional 8b SAR 2b/cycle after MSB conversion

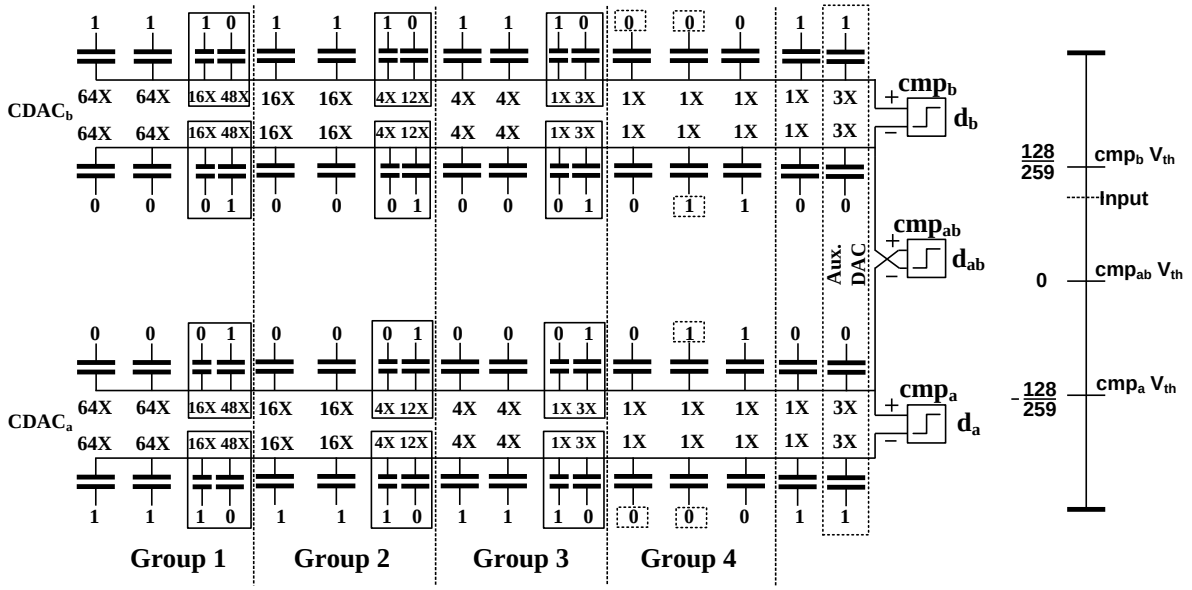


Figure 5.3 CDAC setting in the proposed 8b SAR 2b/cycle after initialization

The shortcoming mentioned above can be mitigated by extending the 1b/cycle split-cap scheme [33] to 2b/cycle operation and presetting the caps properly. The proposed the CDAC capacitor array is shown in figure 5.3. Compare to the traditional 2b/cycle setting, one of the three identical caps in each group is split in weight with 1:3 ratio as shown in the solid box. The preset of those caps is labelled as '1' or '0'. Since the "0" connection state of each split capacitor in $CDAC_b$ is compensated with the same total weight of "1" connection states in the subsequent groups on the right-hand side, each group effectively has all the three connections preset to "1", and all the subsequent groups amount to one "0" connection. Therefore, each group in $CDAC_b$

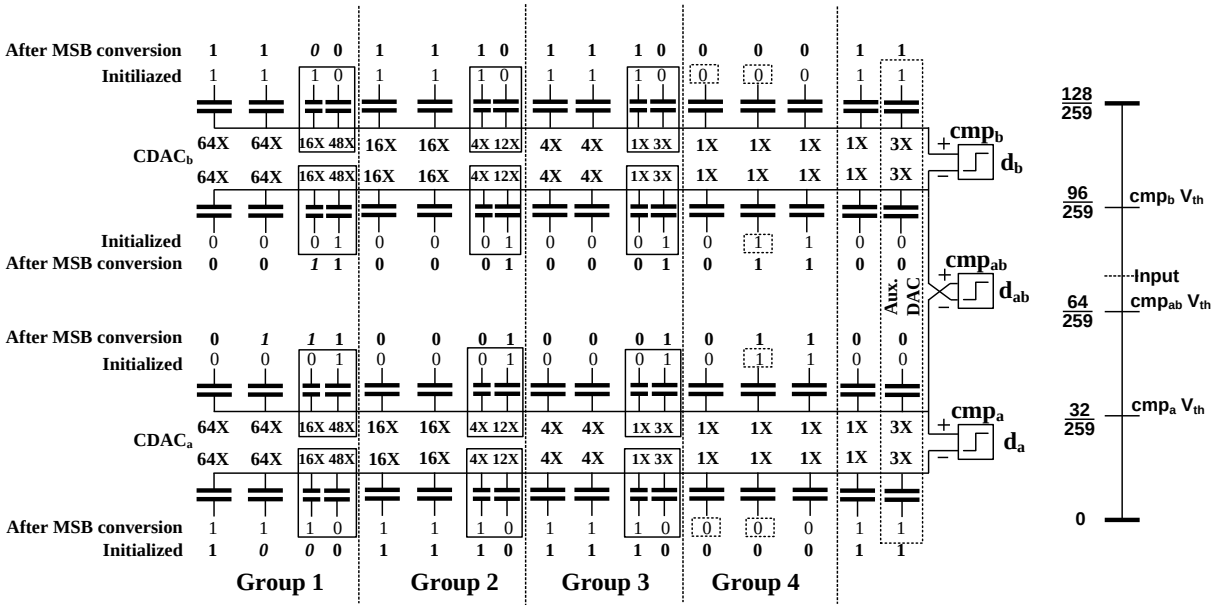


Figure 5.4 CDAC setting in the proposed 8b SAR 2b/cycle after MSB conversion

generates a threshold at ¾ of the subrange for the corresponding cycle. Similarly, the same $CDAC_a$ group generates a threshold at ¼ of subrange due to the initial complementary connections. The midpoint threshold at ½ subrange is generated by interpolation of the $CDAC_a$ and $CDAC_b$ outputs. Upon sampling of the differential input, $CDAC_a$ and $CDAC_b$ top-plate connections are switched from the input to the preset initial state shown in figure 5.3. The cap switches connection after MSB conversion is shown in figure 5.4. With such configuration each group is only responsible for one conversion since the rest of the CDAC will generate threshold automatically by their preset value. The total amount of charge transfer is greatly reduced not only because the switching of split capacitors causes less charge transfer but also because switching happens only once at most for each capacitor. This also guarantees the monotonic threshold generation and significantly reduces the chance of decision error. An example of the complete 8b conversion is shown in figure

5.5, the group numbers are now corresponding to cycle j = 1 ~ 4 since caps involved in each cycle is constrained in each group. The connection state of the three identical capacitors (including the split capacitor) in each group is switched to equal the three comparator outputs (d_b d_{ab} d_a) or (d_a d_{ab} d_b) for $CDAC_a$ or $CDAC_b$, respectively, at the end of the corresponding cycle.

To meet the 11b kT/C noise requirement for ADC FS = 1.2 Vppd, the total capacitance of $CDAC_a$ and $CDAC_b$ is chosen to be 500fF (single-ended) each. Implemented with MOM capacitors, the CDAC is large enough to ensure 11b matching precision.

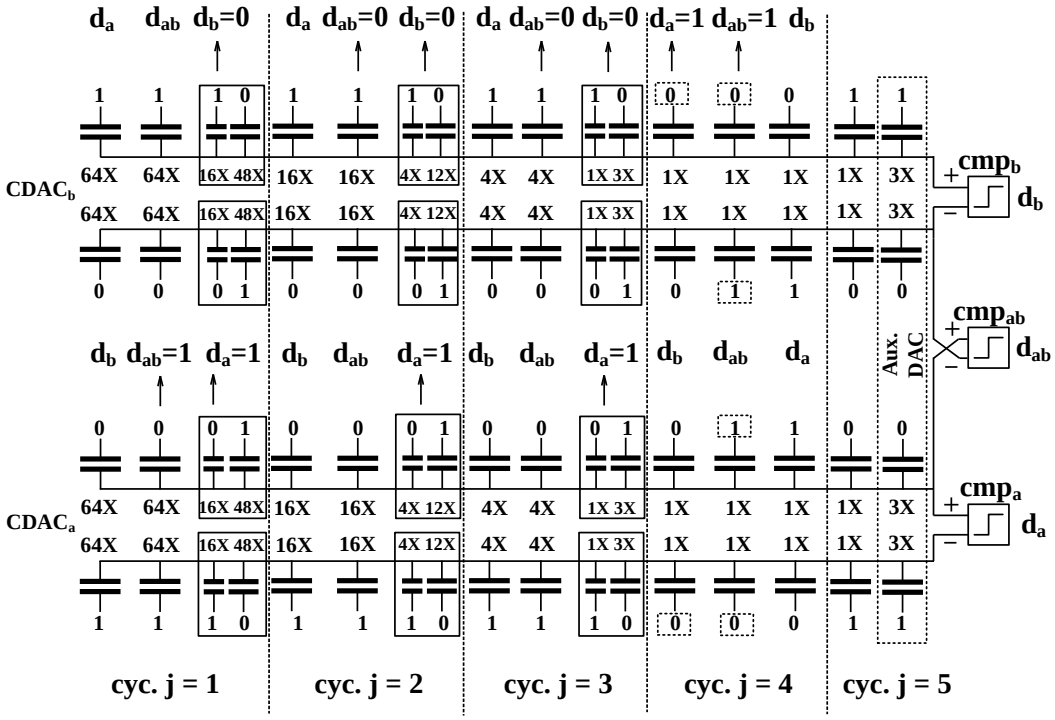


Figure 5.5 The coarse CDAC capacitor top-plate initial connections to the references (0 for Vrefl and 1 for Vrefh) and the connection transitions for each conversion cycle given the same input sample vx=Vs as shown in figure 4.3

5.2 Auxiliary CDAC

A 2b over-range is introduced to perform error correction and it is done by adding a small auxiliary DAC (Aux. DAC) on each of the single-ended CDAC. The Aux. DAC consists of a 3X capacitor added at the LSB end of the capacitor array (figure 5.3). The Aux. DAC decreases the full scale (FS) of ADC by ~1.2% which has negligible impact on SNR. Normally the Aux. DAC toggles in the opposite direction between $CDAC_b$ and $CDAC_a$ to 'enlarge' the output sub range by a conversion completion flag. In the proposed design, the 3X capacitor connection state is preset to "1" in $CDAC_b$ and "0" in $CDAC_a$ such that 24 LSB (3X8) extra threshold or over-range is automatically generated between the $CDAC_a$ and $CDAC_b$ output residues after the completion of 4-cycle coarse conversion. Thus, the residues can be generated as early as possible and minimize the settling time required by the pipeline stage. To compensate for the 3X capacitor impact on the coarse conversion, some capacitors for cycle 4 are also preset, as shown in the dashed boxes in figure 5.3 - figure 5.5. As a result, the total capacitance preset to 1 and 0 remains differentially unchanged for both CDACs.

5.3 Residue Amplifiers

To highlight the architecture benefits, simple open-loop switched-capacitor amplifier circuits that scale well with technology are utilized without aggressive circuit-level power minimization. The residue T&H amplifier schematic is shown in figure 5.6. To help relaxing the following stage design the coarse residues are amplified. Since the coarse SAR significantly shrank the residues (given peak-peak differential (ppd) residue = $4*FS / 2^8 < 20$ mV), the first stage of the amplifier AMP1 is designed with a simple differential pair with resistive loading which can easily achieve the linearity requirement for the following stages. It provides 5X gain and generate less than 100 mVppd to the sample and hold circuits consists of open-loop switched capacitor (S_{12}

and C_h). The second stage of the amplifier AMP2 has 3.5X gain which further amplifies the residue to 350 mVppd. In addition, a source follower output stage drives $CDAC_f$ for fast settling and for CM lowering that allows $CDAC_f$ top plates to be switched with simple NMOS FETs. AMP2 is source degenerated for extra margin in residue linearity. The size and currents are scaled as shown in figure 5.6 to meet the 11b input referred noise requirement. The S_{2t} (figure 5.6) is able to tolerate the bigger voltage swing than S12 because $CDAC_f$ driven by the residue amplifier source followers settles much faster in the conversion phase E than C_h in the track phase D.

As a result of the residue amplification, the inter-stage hold capacitor C_h and the sub range fine SAR $CDAC_f$ can adopt very small capacitance of 30fF and 40fF respectively. In the hold phase while the coarse SAR is doing conversion, the S'_{12} is closed to short the AMP1 output to better isolate the activities from the coarse SAR switching activities. The bias of AMP1 is turn off by Φ_2 when not in use to save power.

The gain mismatch between the two residues causes INL error in sub range ADC. To achieve better than 5b gain matching, the bias circuits for two AMP1s and two AMP2s are shared and the device sizes are chosen to meet the requirement based on Monte-Carlo simulation.

A foreground calibration loop to be described in Chapter 6 cancels the amplifier input referred offset for 11b accuracy.

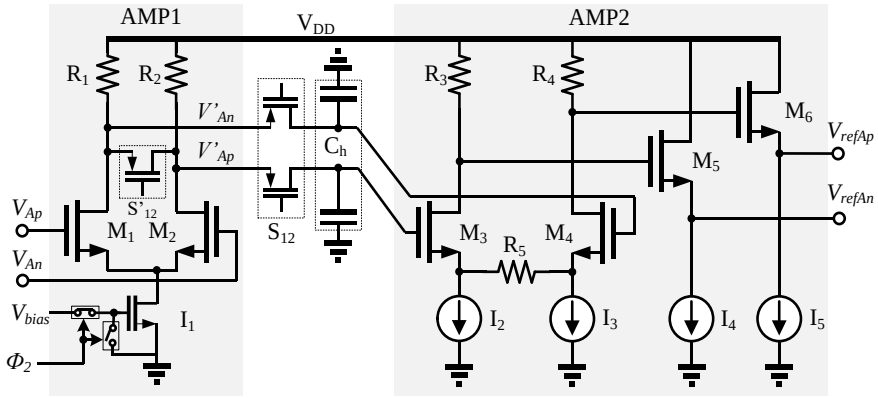


Figure 5.6 Schematic of the interstage residue T&H amplifier

Table 1 Device sizes of T&H schematic as shown in figure 5.6

Device	**Parameters**	**Unit**
R_1, R_2	2.5k	Ω
R_3, R_4	4.5k	Ω
R_5	1.7k	Ω
M_1, M_2	W = 30; L = 0.112	µm
M_3, M_4	W = 14; L = 0.112	µm
M_5, M_6	W = 14; L = 0.56	µm
I_1	240	µA
I_2, I_3	80	µA
I_4, I_5	100	µA

5.4 Comparators

High speed SAR operation relies heavily on the speed of the comparators. Dynamic comparator gains a lot of popularity in the high-speed design and it doesn't consume static power. It consists of preamp stage followed by a cross-coupled latch. Usually there are two configurations to build the dynamic comparator, strongArm comparator which has the stack the preamp and latch in the same branch which has the benefit of higher speed but is more challenge to optimize other parameters, the other type of the comparator is double tail dynamic latch [34] which provides higher flexibility in term of trading off the noise, speed and kickback. It also suitable for low supply due to its folded architecture, however, the speed is compromised due to two stage operation. Because of the high speed and power efficiency, the strongArm comparator is chosen in this prototype. The three coarse comparators and the fine comparators are using the same strongArm dynamic latch with the schematic and transistors sized as shown in figure 5.7 and Table 2 to meet 1mVrms noise target. A foreground comparator offset calibration using capacitors attached to the input pair differential nodes [35] reduces the comparator offset from 25 mV (3σ) to 2.5 mV. The coarse SAR comparator offsets and noise do not cause ADC output error because they are all within the fine quantization over-range of +/-6 mV, where the extra margin covers incomplete settling of the coarse CDACs. The fine comparator noise and calibrated offset are negligible given the >10X residue gain.

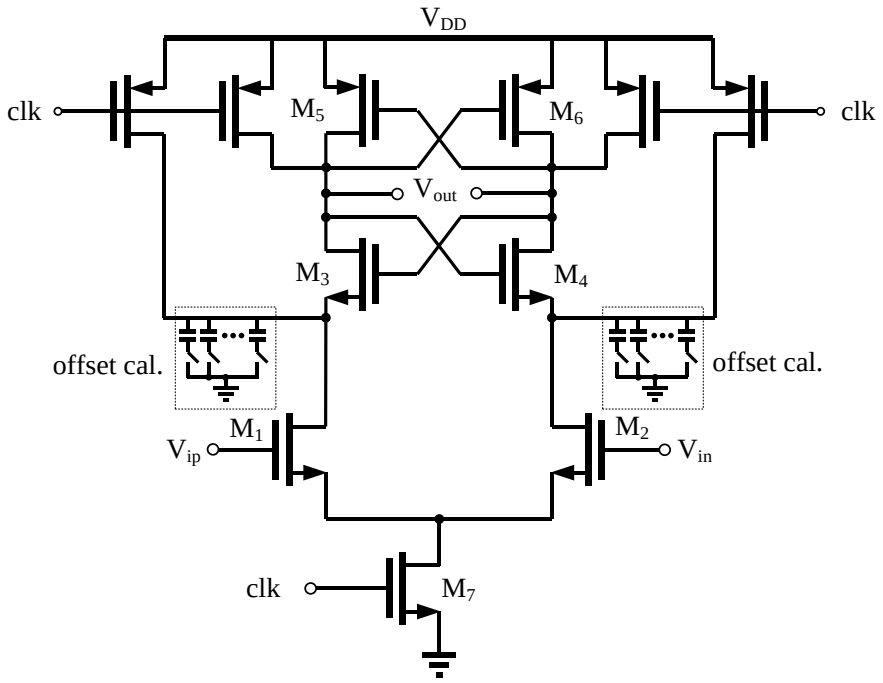


Figure 5.7 Schematic of the comparator with offset calibration capacitor array

Table 2 Device sizes of comparator schematic as shown in figure 5.7

Device	**Parameters**	**Unit**
M_1, M_2	W = 5.2; L = 0.56	µm
M_3, M_4	W = 2.6; L = 0.56	µm
M_5, M_6	W = 2.6; L = 0.56	µm
M_7	W = 2.4; L = 0.4	µm

Chapter 6 Offset Calibration Design and Implementation

6.1 Offset Calibration Overview

An automatic foreground offset calibration loop is designed to correct the 1) offset in coarse and fine SAR comparators and 2) dual residue offset in inter-stage T&H amplifiers. As mentioned in Section 4.4, the offset in comparator is calibrated through a small cap array. The calibration is performed by going through binary successive approximation process and the cap control codes are save in a 7b register. Upon the completion of the first calibration, the fine comparator is ready to be used in dual residue offset correction and the second calibration starts, this calibration repeated for signal path a and signal path b with shared control logic. The details will be discussed in next section. The flow chart for the calibration procedure is shown in figure 6.1.

6.2 Dual Residue Offset Calibration Scheme

For a 1b/cycle SAR conversion, DC offset is of less concern because it only creates a DC shift which reduces the dynamic range. But for 2b/cycle conversion the impact of the DC offset is different and can be categorized into two parts, common mode offset and differential mode offset. The common mode part of the offsets in the dual residues only lead to a DC shift just like the case

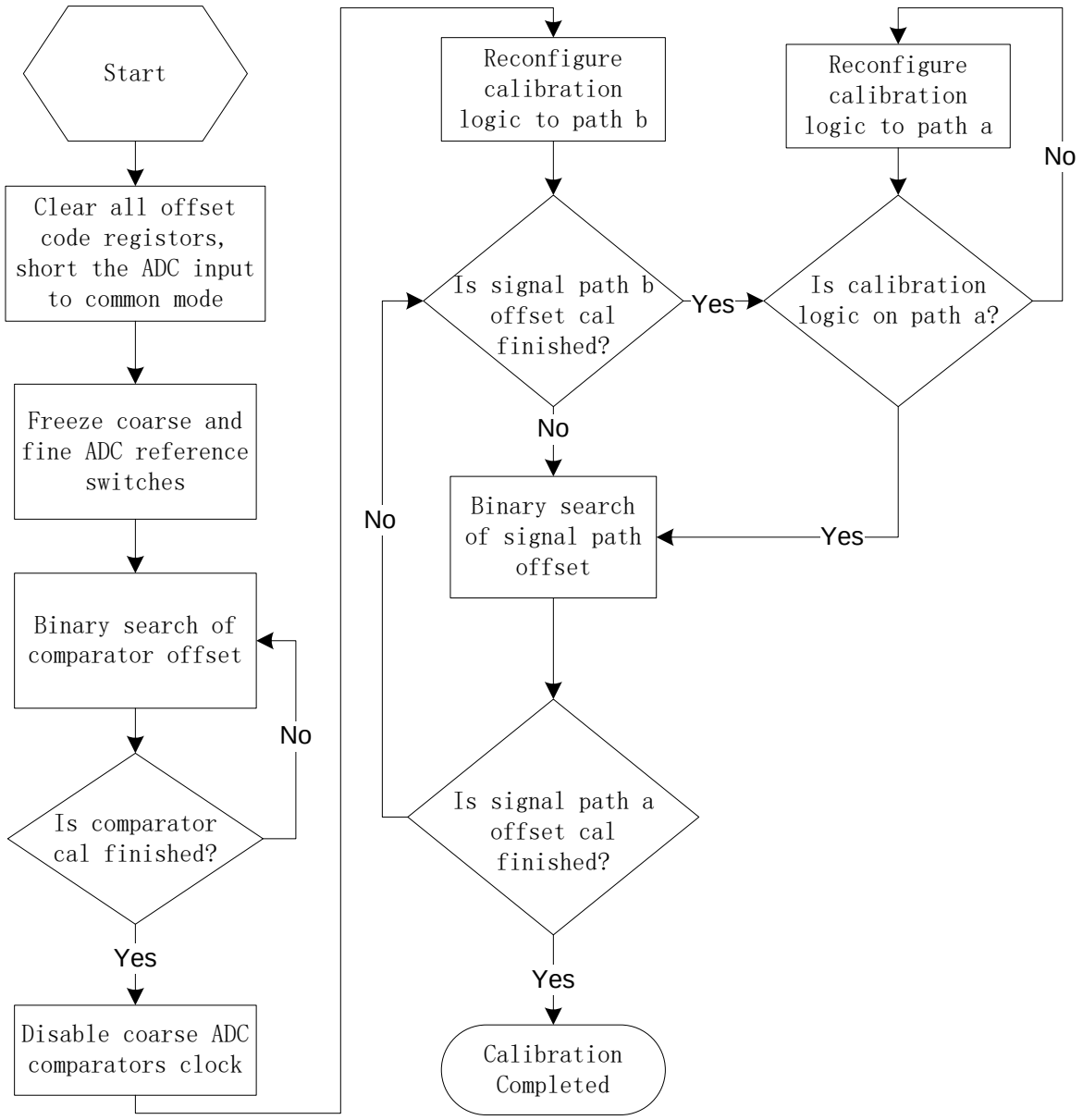


Figure 6.1 Flow chart of offset calibration procedure

in 1b/cycle. However, this DC shift needs to be within the designed over-range otherwise it can go beyond the dynamic range of the sub range ADC and causes the conversion error. The differential part of the offsets (offset mismatch) directly adds to the fine quantization range, causing misalignment with the residue FS range and therefore additional quantization error. To achieve less than one LSB INL the differential offset should be less than one LSB which is ~0.6mV.

Therefore, a calibration scheme is needed to remove the offset on the dual residues. One of the biggest sources of the offset is coming from the input FETs M_1 and M_2 in the AMP1 in the inter-stage as shown in figure 6.2. The following stage such as S_{12} and AMP_2 also create offset but their impact is much lower due to the gain of the AMP_1.

There are different approaches to remove this offset, one way is to design the offset calibration circuit in AMP_1 as shown in figure 6.2, the resistive load of the AMP1 can be made tunable by a resistor DAC (in the form of ladder), however, the gain will be affected and a complicated resistor ladder needs to be design to keep the constant gain. Besides this, the FETs in the resistor adds more mismatch to the load and it has negative impact on the speed, offset and gain over PVT. Another way to perform offset calibration is to use auto-zeroing amplifier in the AMP_1 as shown in figure 6.3. The auto-zeroing clock can be controlled by introducing Φ_3, so the C_o stores the offset voltage right before the ZX tracking and sampling phase ($\Phi_2 = 1$), this offset will be removed when $\Phi_3 = 1$ and it is ready for the sub range ADC for conversion.

The advantage of using auto-zeroing architecture is the offset always tracks with PVT and it is automatically done in each sampling. This approach seems to perfectly fit our design but there are some drawbacks which pose great design challenge in our prototype. First before the AMP1 a pair of series switches need to be added on CDAC (where V_{Ap} and V_{An} is), those switches slows

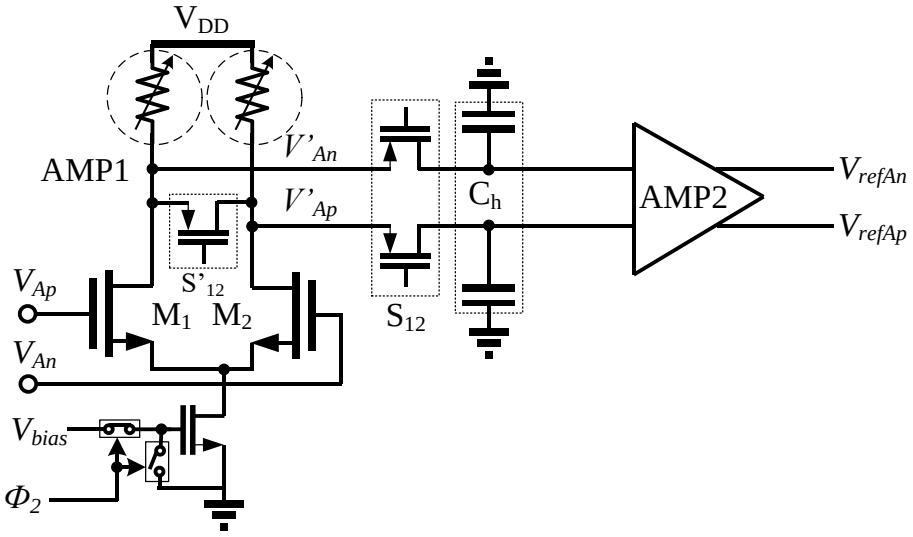


Figure 6.2 Use resistor ladder to calibrate the offset in inter-stage

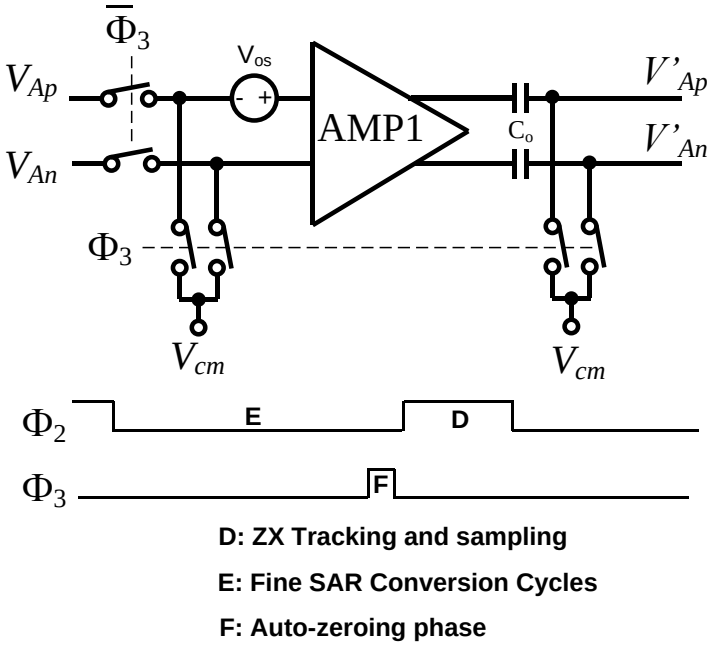


Figure 6.3 Use auto-zeroing amplifier to calibrate the offset in inter-stage

down the ZX tracking phase and more importantly, the charge injection and clock feedthrough becomes another source of offset which cannot be calibration because it is not being seen by the AMP1 in auto-zeroing phase. The C_o also introduces excess attenuation of the amplified dual residues and makes the following stages non-idealities more pronounced.

The proposed offset calibration method is by adding a small array of calibration caps (as shown in figure 6.4) on the coarse CDACs and use it to inject offset correction charge to the $CDAC_b$ and $CDAC_a$ outputs during the fine quantizer tracking phase. As the goal is to remove the offset mismatch on the dual residues for sub range ADC, signal path a as selected in solid line and signal path b as selected in dashed line are treated equally in terms of offset calibration. As shown in the figure 6.4, path a and path b shared the same sub range ADC so it can be used to detect the offset of the other blocks in the two paths and eventually make the two paths each sees almost the same offset. As a result, the offset mismatch is minimized between the two paths.

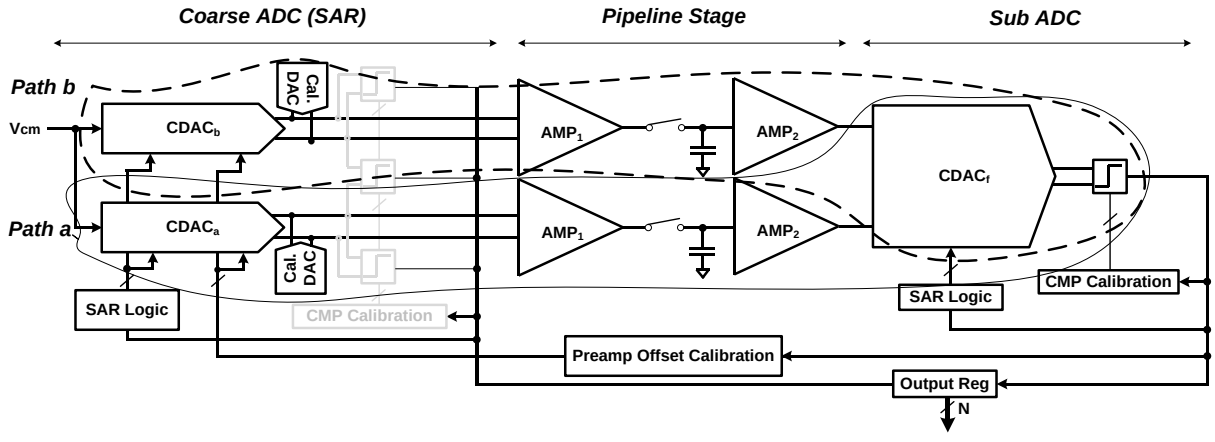


Figure 6.4 Use added offset calibration DAC (Cal. DAC) to calibration inter-stage offset

Figure 6.5 shows the implementation calibration scheme of on signal path b (path a is not shown here since the procedure is identical). The simulated DC offset 3σ is 7.5mV in signal path a and b. The calibration DAC is designed to have a 5b cap array and it can provide +/-9mV correction range at the required sub-1mV resolution. The two paths are calibrated upon startup in two separate steps to remove the respective DC offset, the timing diagram of the calibration procedure is shown in figure 6.6.

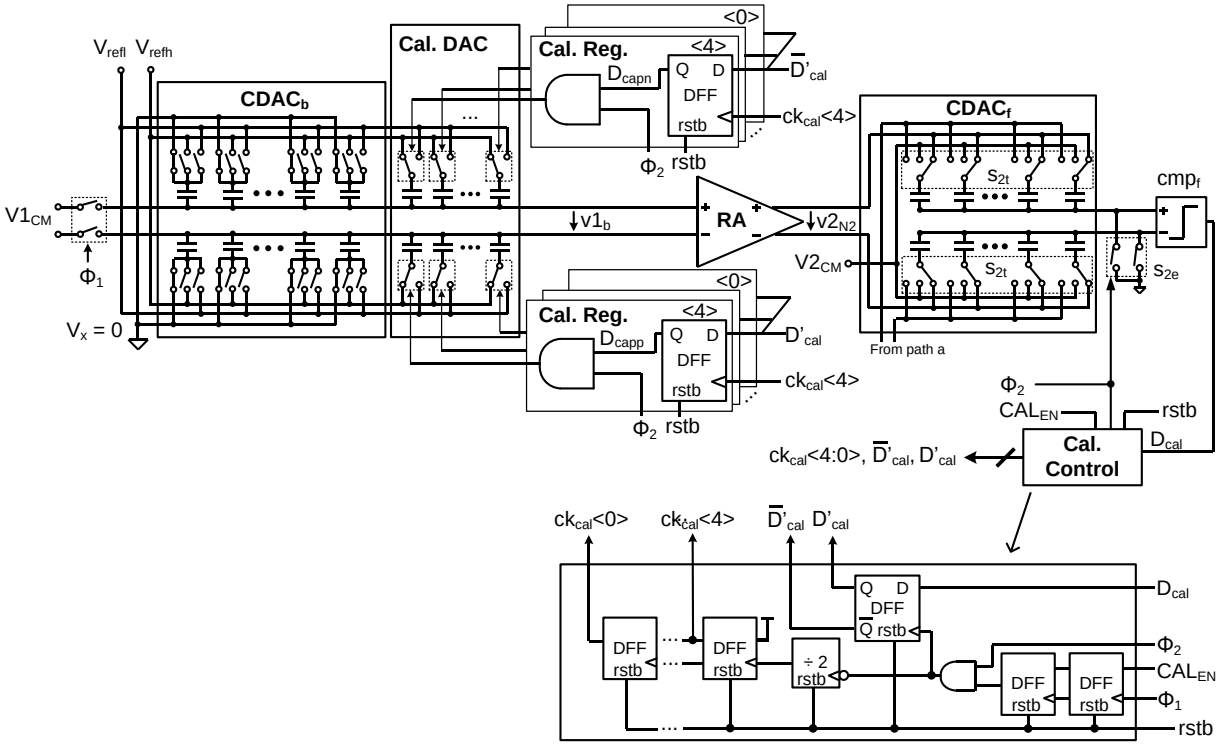


Figure 6.5 Residue offset calibration illustrated for signal path b

6.3 Dual Residue Offset Calibration Procedure

The entire ADC is initialized when rstb = 0, it sets all the 10 calibration registers and its complement that store the calibration codes to 0, in the meantime, it connected the all the calibration capacitor top plates to low reference voltage V_{refl}. The dual residue offset calibration mode works in foreground and it is entered with CAL_{EN} = 1. Which shorts the ADC differential input to a common-mode voltage $V1_{CM}$ and disables the clock goes to coarse ADC comparators.

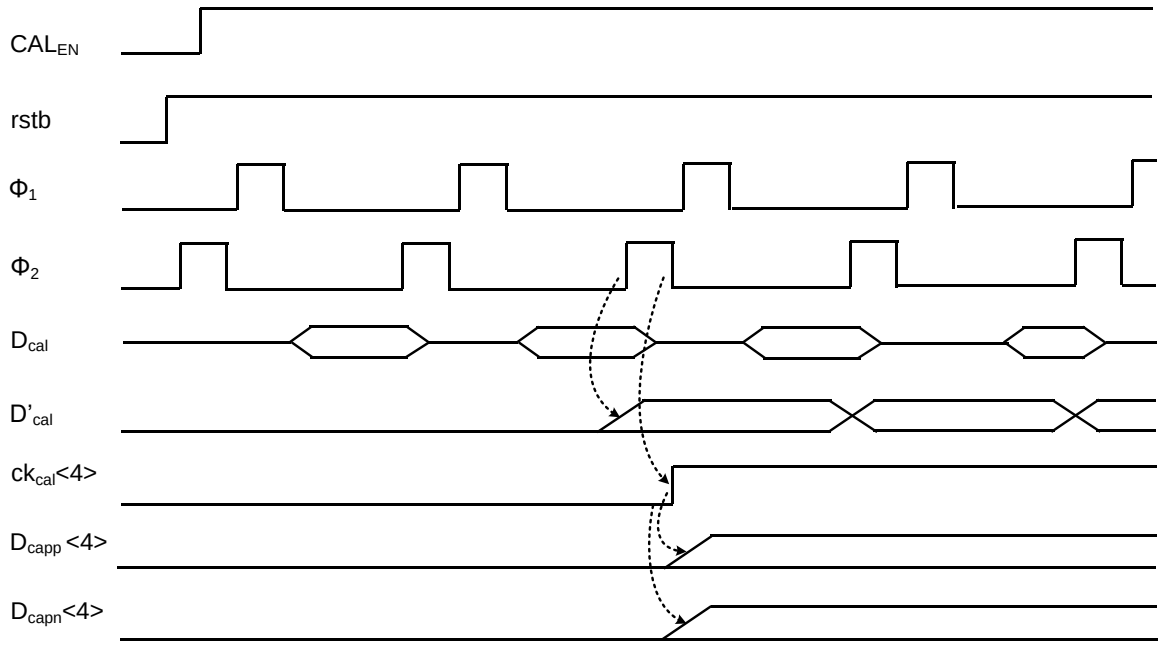


Figure 6.6 Timing diagram of residue offset calibration for signal path b

The first rising edge of Φ_1 prepares the calibration clock generation by retiming the CAL_{EN} to remove the potential glitches when it is AND with Φ_2.

Since the coarse comparators are disabled, the ADC enters dual residue tracking and sampling phase without going through coarse conversion. At the Φ_2 falling edge, the inter-stage T/H samples and holds the $CDAC_b$ output and then the sub ADC enters conversion phase but with modified SAR logic as follows. The reference switches in fine ADC are all connected to $v2_{N2}$ and the asynchronous loop is reprogrammed to clock the comparator once in each conversion.

The bottom-plate switches S_{2e} of $CDAC_f$ sample the zero differential input, and then the top-plate switches S_{2t} connection from the common mode voltage $V2_{CM}$ to the RA output $v2_{N2}$. After a preset short delay, the sampled offset voltage appearing at the $CDAC_f$ output and then is latched by the fine comparator cmp_f. At this time, the offset of signal path b is detected, and it can feedback the information back to calibration DAC. At the next Φ2 falling edge (i.e., ckcal<4> rising edge), the calibration DAC MSB register D'cal<4> and the complement are updated with the comparator output D_{cal}. At the following Φ_2 rising edge, the calibration DAC subtracts or adds one MSB from or to the sampled offset for D'cal<4> = "1" or "0". In two Φ2 cycles, D'cal<3> is updated upon the rising edge of ckcal<3>, and eventually, the 5b offset correction code for path b is resolved through this binary successive approximation process. This is then repeated to correct the offset in path a.

Chapter 7 Simulation and Measurement Results

7.1 Simulation Results

The prototype ADC is designed in a 45 nm Global Foundry SOI CMOS process, it occupies an active area of 0.07 mm^2 as shown in figure 7.1, the ADC is able to achieve up to a sampling rate of 400MS/s. The power consumption breakdown is shown in figure 7.2. The coarse SAR consumes most of the power because it needs to meet noise requirement of the entire ADC, with the help of gain from interstage of AMP1 and AMP2, the Fine SAR only needs to burn a fraction of coarse ADC power to resolve the LSBs. The total power is 3.16mW which corresponds to a Scherier FoM of 171.4dB. The Monte-Carlo simulation is performed including the thermal noise, random MOSFET and resistor mismatch at typical corner, the parasitics are back-annotated based on extracted result. It shows the comparator offset calibration improves the near Nyquist SNDR from 51.2dB to 56.1dB as shown in figure 7.3 (a)(b), and it further improves the SNDR to 63.4dB after removing the offset of the dual residues as shown in figure 7.3 (c), the SFDR of the ADC reaches 75.8dB and 88dB for near Nyquist and low frequency inputs (figure 7.3 (d)), respectively. The INL and DNL are shown in figure 7.4 and both are within 1.05LSB. Figure 7.5 shows the SFDR and SNDR variation are very small despite more than +/- 25% variation in the RA gain over 100^{o}C temperature range, the differential offset which is process depend also shows very little variation. Figure 7.6 shows the SFDR and SNDR of ADC prototype vs. (a) input frequency with supply variation, sampling rate at 400MS/s, (b) sampling frequency.

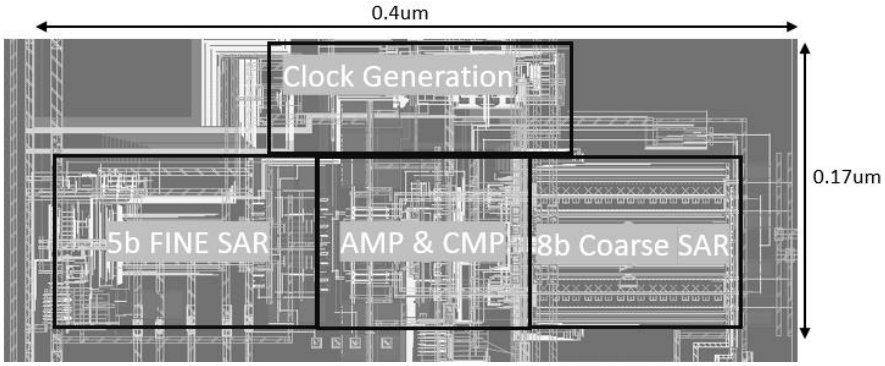


Figure 7.1 ADC prototype layout

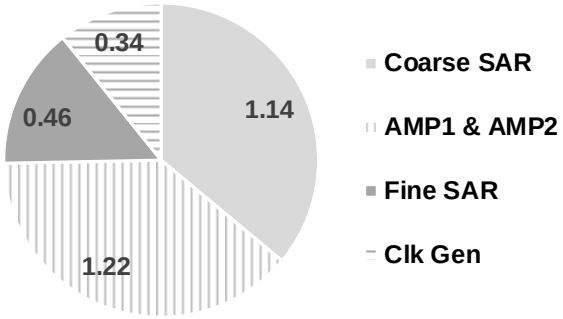
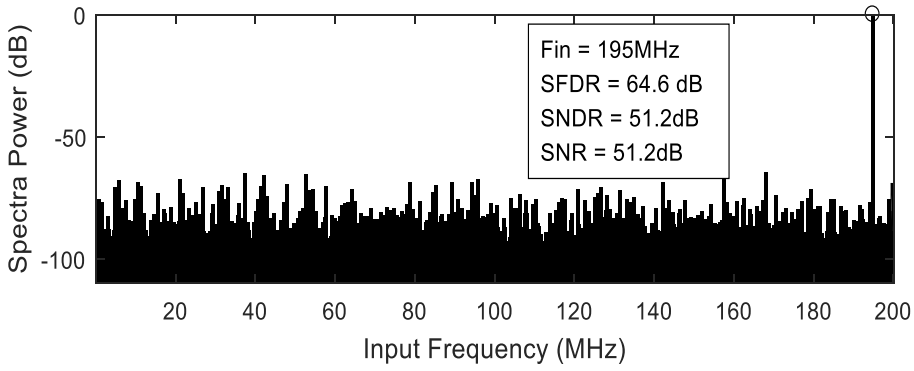
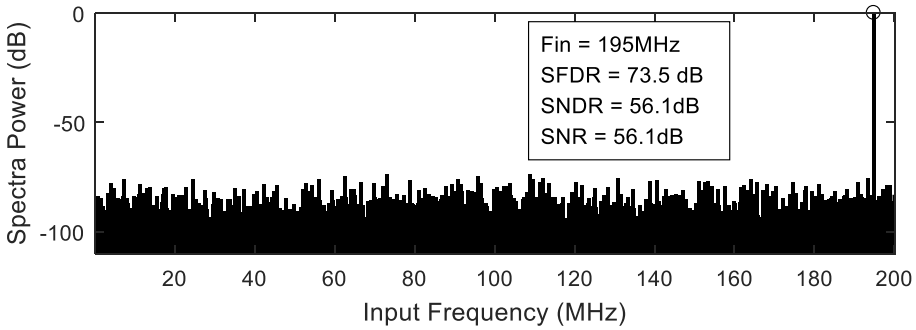


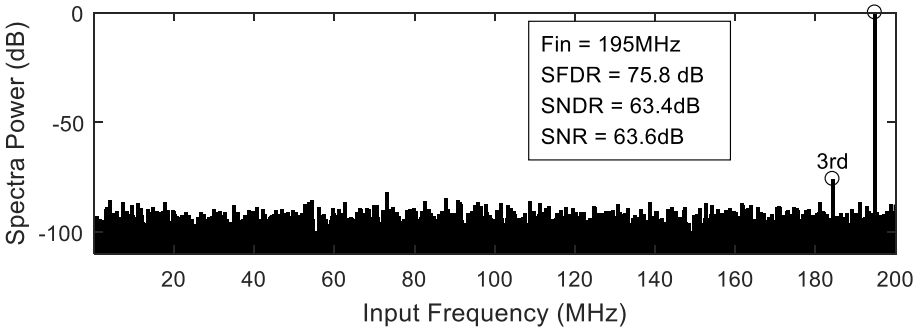
Figure 7.2 Power consumption breakdown (mW)


Fin = 195MHz
SFDR = 64.6 dB
SNDR = 51.2dB
SNR = 51.2dB
Spectra Power (dB)
0
-50
-100
20
40
60
80
100
120
140
160
180
200
Input Frequency (MHz)

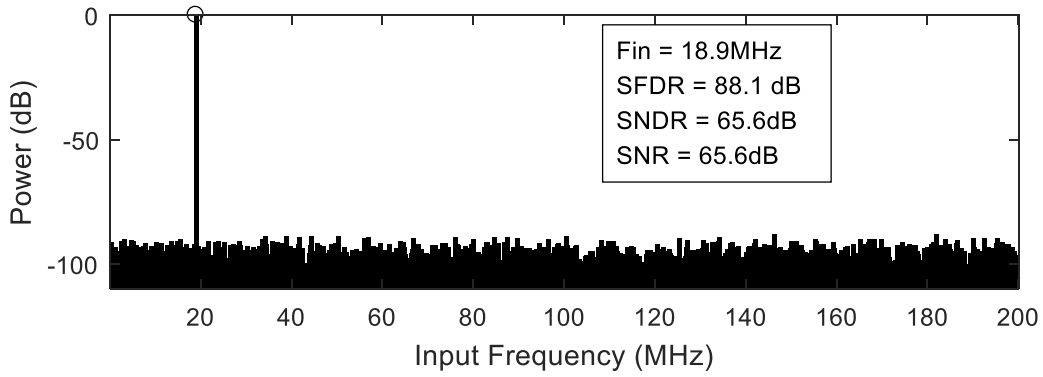
(a)


Fin = 195MHz
SFDR = 73.5 dB
SNDR = 56.1dB
SNR = 56.1dB
Spectra Power (dB)
0
-50
-100
20
40
60
80
100
120
140
160
180
200
Input Frequency (MHz)

(b)


Fin = 195MHz
SFDR = 75.8 dB
SNDR = 63.4dB
SNR = 63.6dB
3rd
Spectra Power (dB)
0
-50
-100
20
40
60
80
100
120
140
160
180
200
Input Frequency (MHz)

(c)



(d)

Figure 7.3 Typical-corner output spectra from Monte-Carlo simulations of the prototype ADC running at 400 MS/s with (a) Nyquist input before offset calibrations, (b) after comparator calibrations, (c) after residue offset calibrations, and (d) low frequency input after all calibrations. Device random mismatch and thermal noise are included in the simulations

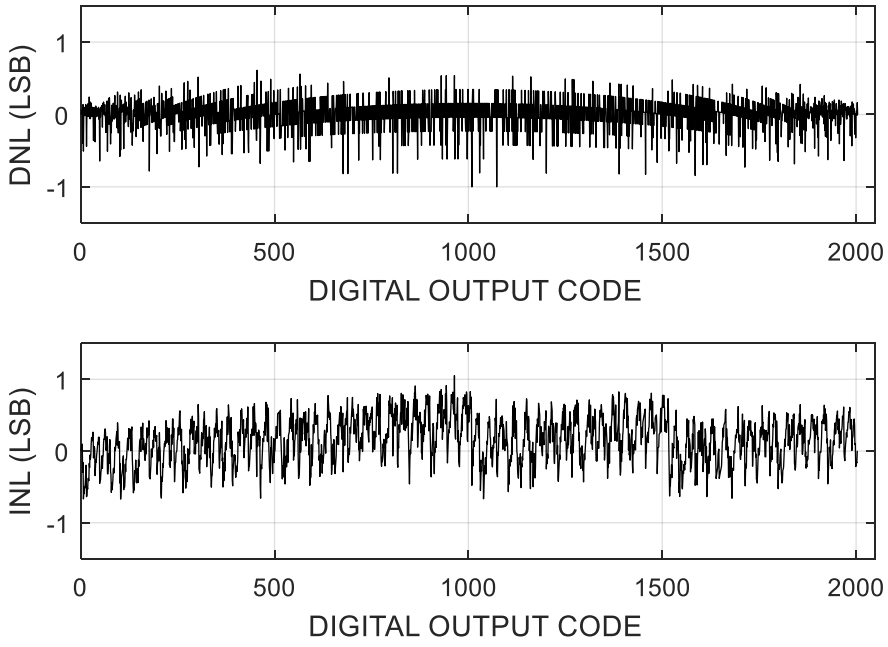
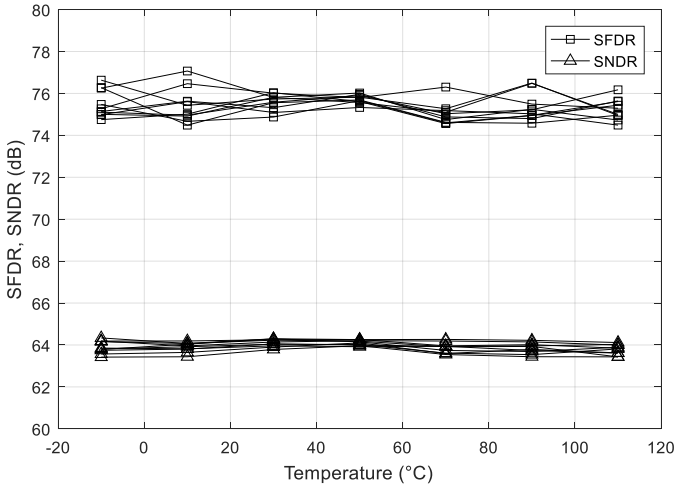
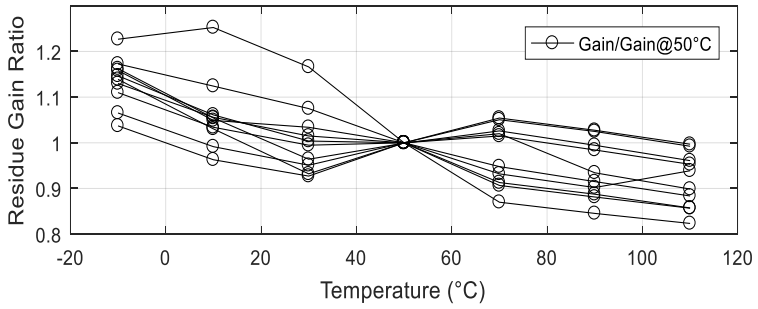


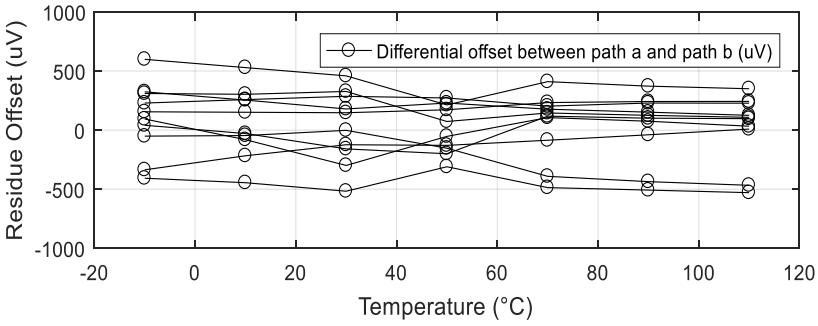
Figure 7.4 Typical-corner DNL and INL from Monte-Carlo simulations of the prototype ADC after offset calibration



(a)

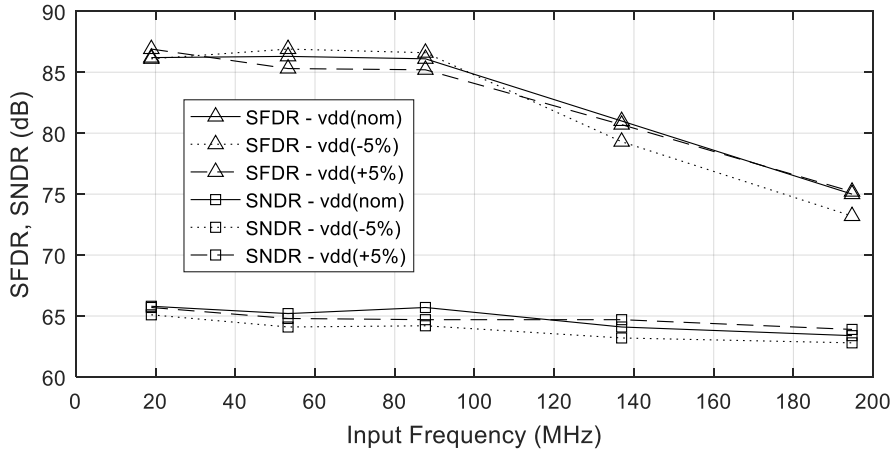


(b)

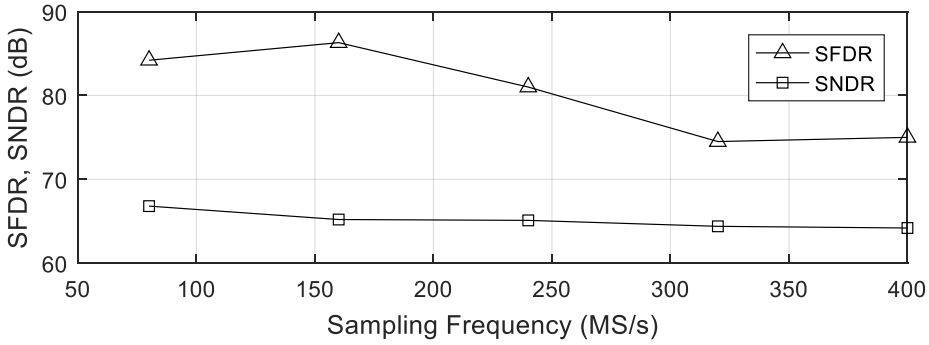


(c)

Figure 7.5 Temperature dependence of (a) the typical-corner SFDR and SNDR, (b) residue gain, and (c) residue offset from Monte-Carlo simulations. The foreground residue offset calibrations are simulated at 50°C



(a)



(b)

Figure 7.6 SFDR and SNDR of ADC prototype vs. (a) input frequency with supply variation, sampling rate at 400MS/s, (b) sampling frequency

7.2 Measurement Results

This prototype ADC employs the identical architecture as discussed in this Chapter 4 except the sub-ADC is implemented with 4b resolution SAR instead of 5b. It is designed and fabricated in a 45 nm Global Foundry SOI CMOS process and it occupies an active area of 0.04mm2 as shown in figure 7.7, it achieves 0.71-LSB INL, 0.72-LSB DNL, 58.2-dB SNDR, and 70.2-dB SFDR at 250MS/s as shown in figure 7.8 with total 2.7 mA drawn from a 1-V supply. The effect of offset calibration at Nyquist conversion is shown in figure 7.9. The performance dependences on input signal frequency, conversion rate, and input signal amplitude are shown in figure 7.10, respectively.

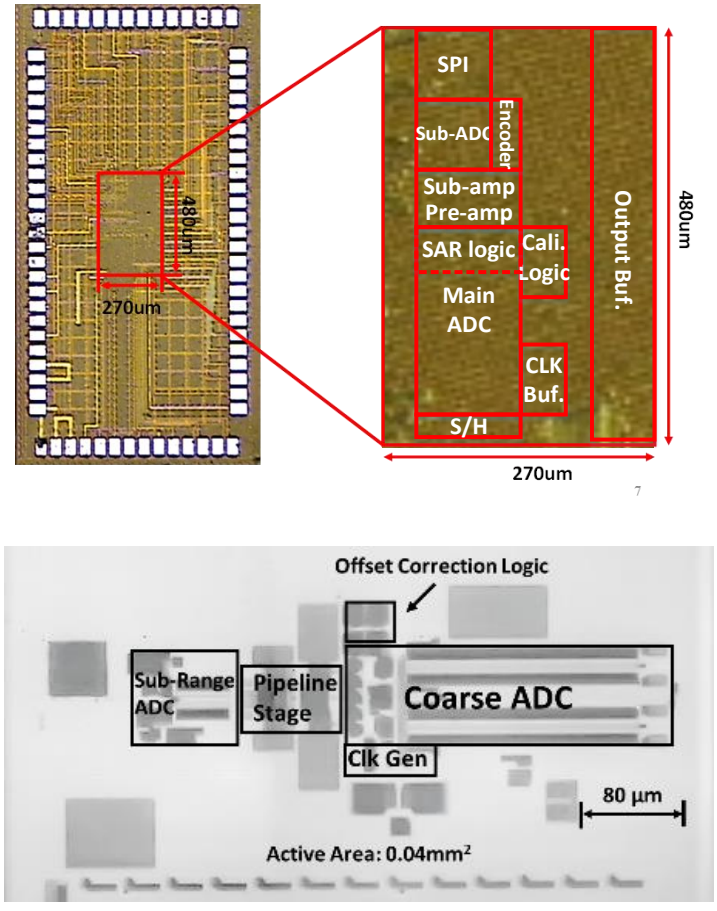
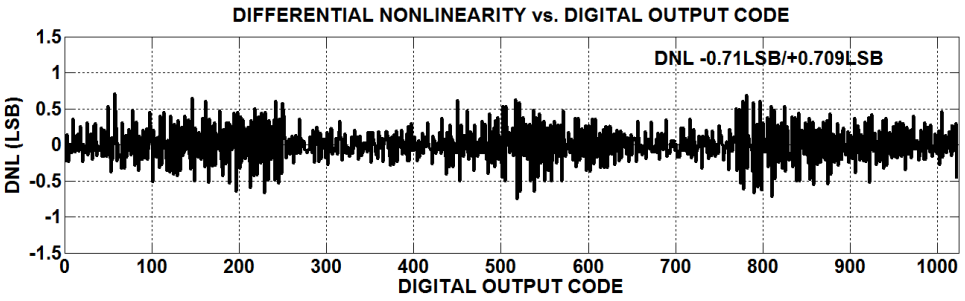
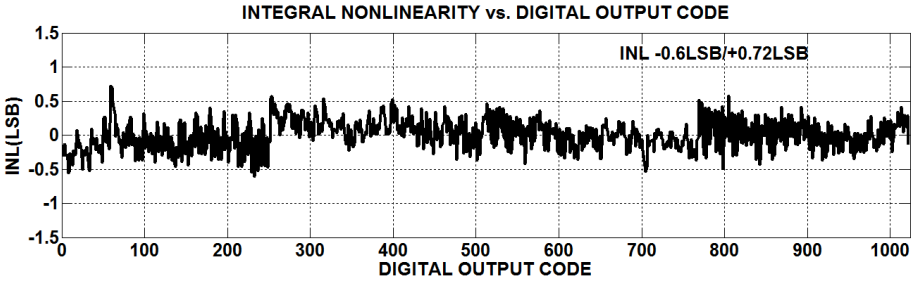


Figure 7.7 ADC prototype die photo

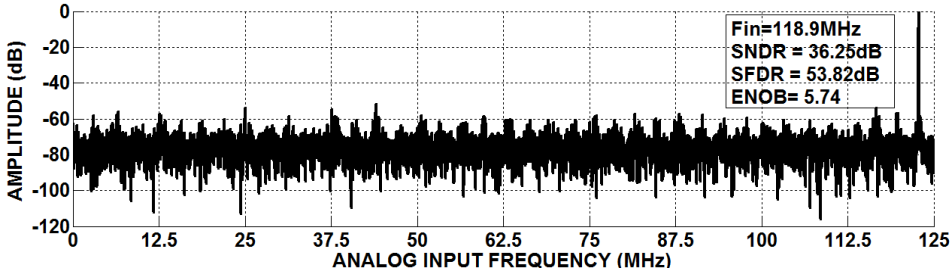


(a)

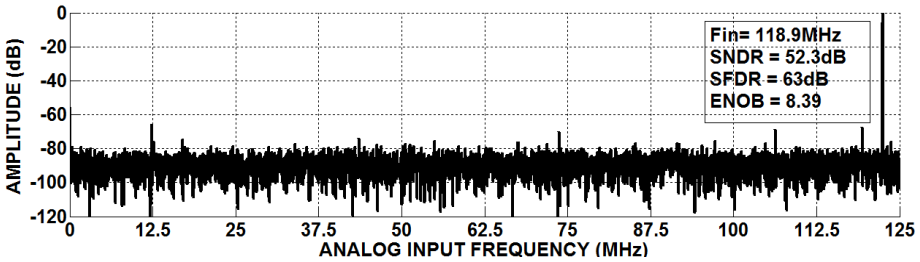


(b)

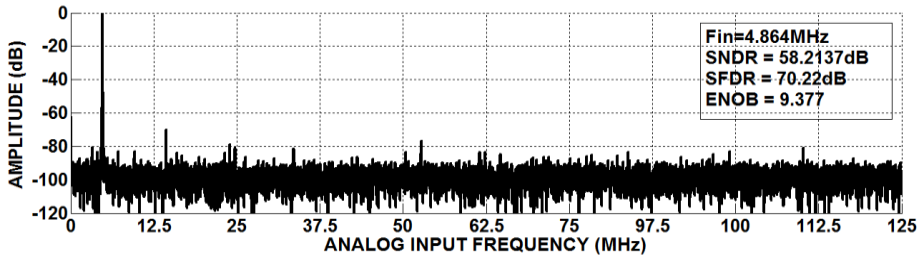
Figure 7.8 Measured DNL (a) and INL (b) of ADC prototype



(a)

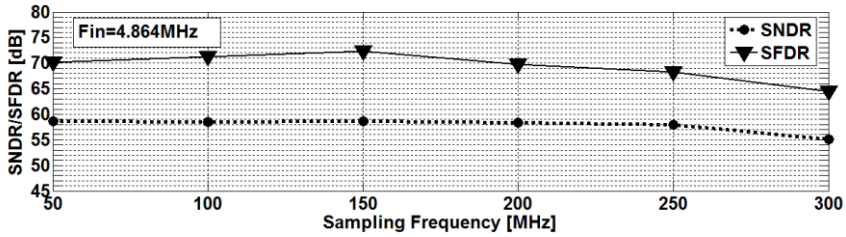


(b)

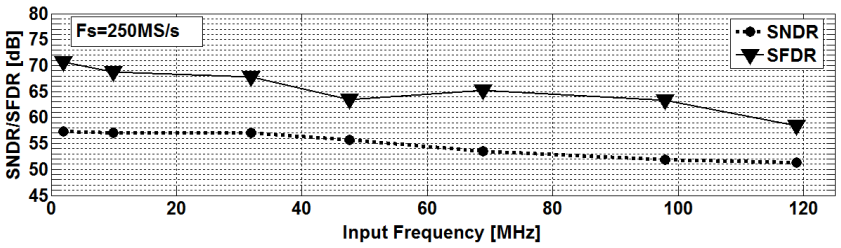


(c)

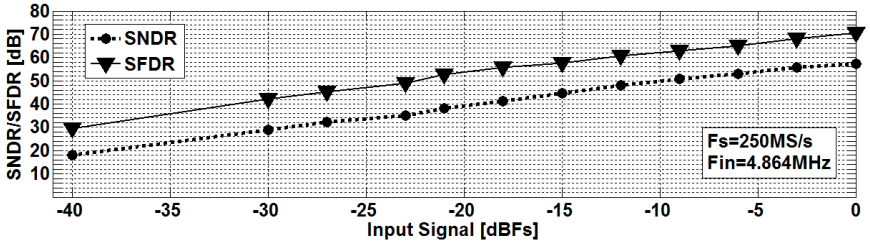
Figure 7.9 Measured ADC spectrum with near Nyquist input before (a) and after (b) foreground offset calibration , and low input frequency after foreground offset calibration (c) with sampling rate 250MS/s



(a)



(b)



(c)

Figure 7.10 Measured ADC SNDR versus sampling frequency (a), input frequency (b) and input amplitude (c)

7.3 Summary

summarized the ADC prototypes performance. To compare FoM, the ADCs demonstrated in Table 3 and [7, 24] are designed in similar technology in 40nm and are considered the most relevant to the proposed 11b ADC with similar SNDR around 60dB, and not much different speeds in hundreds of MS/s. It is unfair to compare the simulated results directly with the measured counterparts but given one-bit ENOB reduction to account for silicon performance degradation, the resulted FoM = 171.4 – 6 = 165.4 dB for the prototype is still much better than the 155 dB Schreier FoM calculated for the latest dual-residue counterpart [24]. The lane speed is also faster (400MS/s vs. 200MS/s) than this counterpart that uses multistage flash sub-ADCs. The better overall performance can be ascribed to the use of power efficient SAR sub-ADCs and simple open-

loop RAs. Compared with [7] that uses power-efficient dynamic RA, this prototype does not exhibit definite advantage in the FoM. However, it avoids the postprocessing used in [7] for residue gain correction, which would have significantly worsened the FoM if implemented on chip as background calibration to track out the impact of PVT variations. In contrast, the prototype can further enhance the FoM using dynamic RAs without any concern of background calibration.

Table 3 Pipelined ADC Performance Comparison

	The 11b ADC prototype *	The 10b ADC prototype **	Vecchi JSSC 2011 [24]	Verbruggen JSSC 2012 [7]
Residue(s)	Dual	Dual	Dual	Single
Sub-ADC	SAR	SAR	Flash	SAR
Process (nm)	40	40	40	40
Resolution (bit)	11	10	12	11
Speed (MS/s) (Lanes)	400	250	800 (4-way)	250 (2-way)
Full Scale (V_{ppd})	1.2	1.2	1.2	-
Supply (V)	1	1	1, 2.5	1.1
SNDR Nyquist (dB)	63.4	52.3	59	56
SNDR Peak (dB)	65.6	58.2	-	-
SFDR Nyquist(dB)	75.8	63	70.1	67
SFDR Peak	88.1	70	-	-
Power (mW)	3.16	2.7	155^{+}	1.7
FoM Nyquist(dB)	171.4	159	155	164.7
FoM Peak (dB)	173.6	164.9	-	-
Area (mm^2)	0.07	0.04	0.88	0.07
Residue Amplifier	CML Open loop	CML Open loop	Opamp Closed loop	DA Open loop
Residue Gain Adjustment	No	No	No	Post Processing

* Simulation results of 11b ADC prototype

** Measurement result of 10b ADC prototype

$^{+}$ Including reference buffer power consumption

Chapter 8 Anti-Aliasing Low Pass Filter

8.1 Introduction

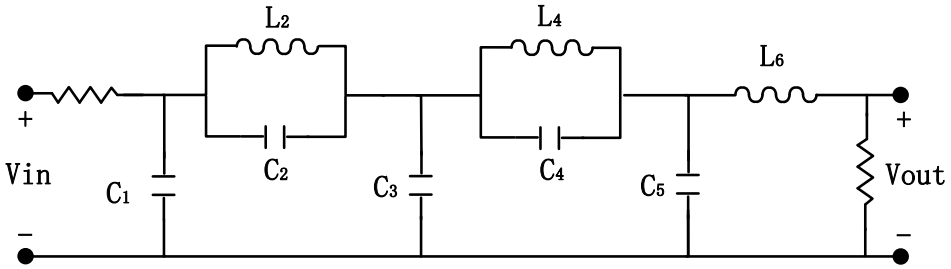
Baseband continuous-time low pass filter is a key building block in sampling system [37-40]. According to Nyquist sampling theorem, the sampling rate needs to be at least twice the maximum frequency component of the signal of interest. Otherwise, the higher than Nyquist frequency components may alias into the band of interest and degrade the system performance. To prevent this from happening, a low pass filter is usually placed in the front stage to provide enough attenuation of the unwanted signal before it feeds into ADC. This work will present two low pass filter designs targeting for this application.

8.2 Design of 6th Order Low Pass Inverse-Chebyshev Active-RC Filter

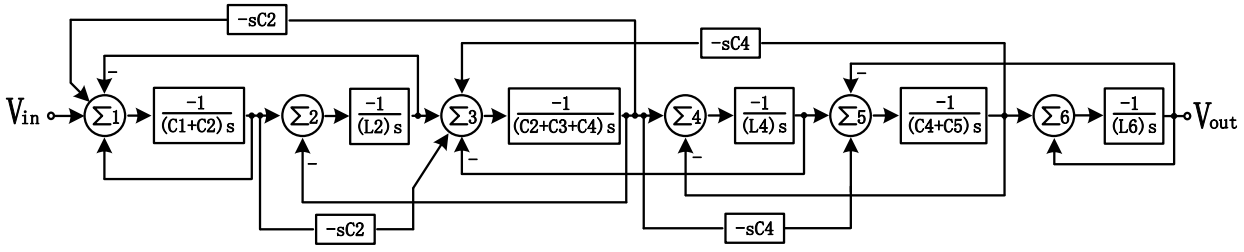
Active-RC low pass filters [37, 39-40] is a popular choice in low pass design due to its high linearity performance which requires high gain-bandwidth op-amp. For filter types with sharp transition band such as Chebyshev, inverse-Chebyshev and Elliptic filters, the gain-bandwidth requirements are even higher to maintain the high Q of the poles. Another potential issue in the design is the large passive component spread when low passband ripple and high stopband attenuation filter is designed. Capacitor spread is more critical as the area is usually limited by the smaller capacitor that can be realized accurately, too big capacitor spread sometime leads to unrealistic area consumption and becomes a bottleneck in the whole chip. This work presents a 6th

order low pass active-RC filter with tunable frequency from 1MHz to 10MHz [46]. The filter achieves zero capacitor spread by replacing derivative feedforward and derivative feedback capacitor with resistor [38]. A hybrid-compensated op-amp with push-pull output stage is also proposed to extend the gain-bandwidth without increasing power consumption. To compensate PVT variations, a low-power, fast convergency tuning circuit is designed to tackle PVT variations. The tuning circuit is based on digital delay locked loop reported in [47] but with a SAR controller to achieve fast tuning.

Usually there are two ways to build high order filter. The first way is to build from cascading several biquads together and it is relatively easy to design and tune but suffers from high passband sensitivity due to component variations. Another way is to design it based on passive ladder LC prototype which has low sensitivity to component variations [50]. The proposed filter topology of 6^{th} order inverse-Chebyshev ladder prototype and the signal flow graph are shown in figure 8.1(a) and (b). The components are shown in Table 4.



(a)



(b)

Figure 8.1 The ladder prototype (a) and the signal-flow-graph of the ladder prototype (b)

Table 4 Device sizes of LC prototype as shown in figure 8.1(a)

Device	**Parameters**	**Unit**	**Device**	**Parameters**	**Unit**
C1	902.8	pF	L2	8.394	μH
C2	674.4	pF	L4	10.56	μH
C3	4.915	nF	L6	3.765	μH
C4	1.072	nF			
C5	3.27	nF			

As shown in figure 8.1 and Table 3, C2 and C4 create derivative feedforward and derivative feedback path. The table also shows they have large spread with respect to other capacitors and make the match among them very challenge. A method reported in [62] greatly improved the match among capacitors by replacing the capacitors with resistors with modified the SFG. And zero capacitor spread can be achieved by making all the integrators identical. By doing this the resistor spread may increase but it is often of less concern since resistor occupies less area.

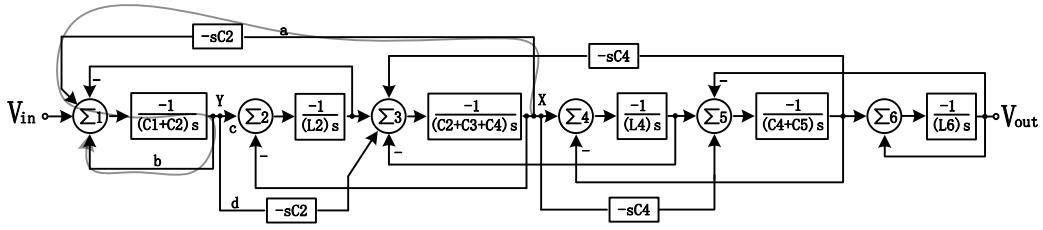
It can be examined from figure 8.2(a-c) that the voltage on net X to Σ_1, Σ_2 and Σ_3 can be express as

$$\Sigma_1 = V_X \frac{C_2}{C_1+C_2} \tag{8.1}$$

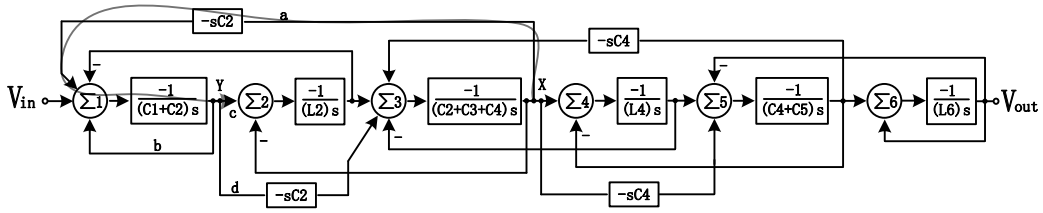
$$\Sigma_2 = V_X \frac{C_2}{C_1+C_2} \tag{8.2}$$

$$\Sigma_3 = V_X \frac{-sC_2^2}{C_1+C_2} \tag{8.3}$$

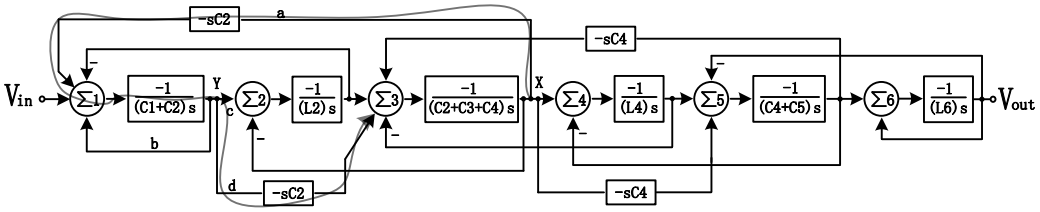
This means those paths can be replaced by a transfer function which can be realized purely by resistor after considering derivative path and integration path together, this can be seen from figure 8.3, the derivative path on path a is replaced by a transfer function by combining path a and path b. Repeat these procedures on all the derivative paths, the modified SFG with zero capacitor spread by using the method mentioned above is shown in figure 8.4(a). Compared with the SFG shown in figure 8.1, the capacitor branch consists of C2 and C4 are replaced with resistors as shown in figure 8.4(b) where all transfer functions can be realized by using resistors.



(a)



(b)



(c)

Figure 8.2 Voltage on net X and its effect on (a) Σ_1, (b) Σ_2 and (c) Σ_3

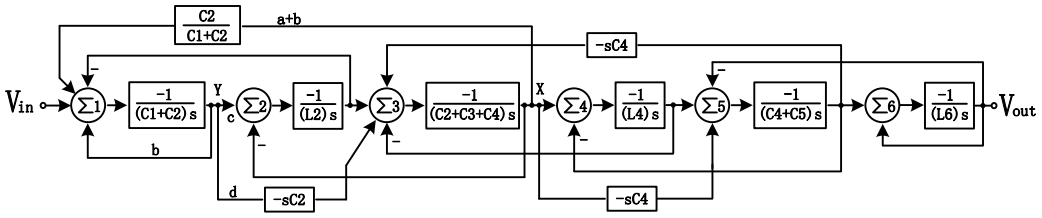
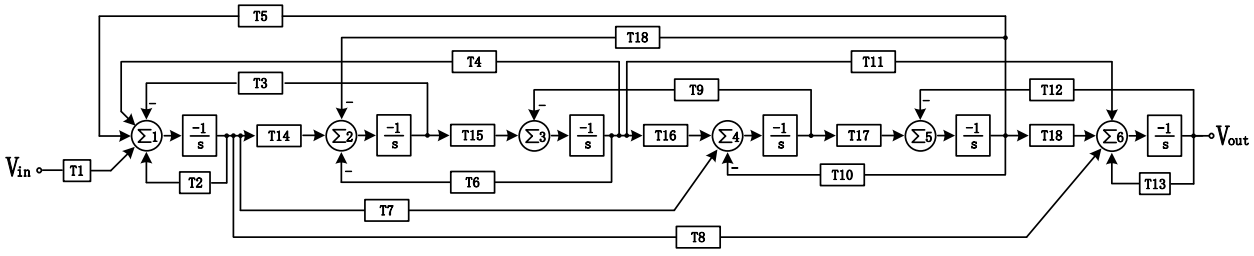
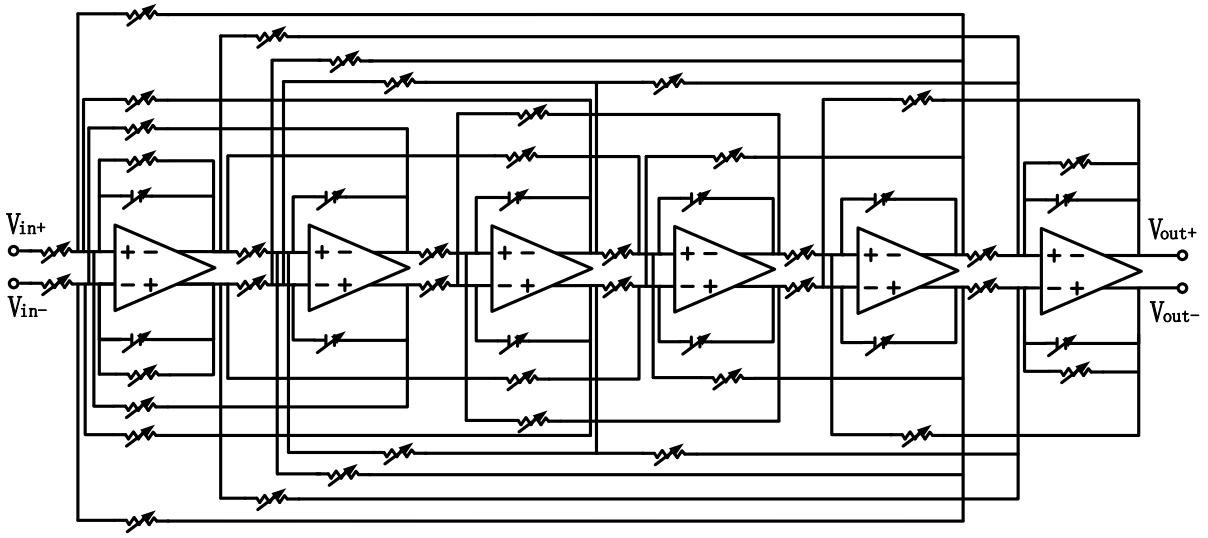


Figure 8.3 Combine path a and path b to a single path a+b



(a)



(b)

Figure 8.4 The modified signal-flow-graph of the ladder prototype (a), the schematic of the proposed 6th order low pass filter (b)

The main challenge for active-RC filter is the operational amplifier design. Large gain-bandwidth is required when filters designed with high Q poles. Usually, filters with sharp transition band and high stopband attenuation require high gain-bandwidth op-amp. Two stage op-amp is often used to achieve high gain and proper compensation method is needed to compensate the op-amp to avoid stability problem. Traditional two-stage op-amp with Miller compensation may end up with extremely high power consumption to achieve the required gain-bandwidth. In this paper, a low power bandwidth extended is proposed to achieve high gain over a wide band with no extra power consumption. Push-pull stage is used to provide high drive strength with low static power consumption. The overall op-amp schematic is shown in figure 8.5. The first stage of the op-amp is a commonly used folded cascode stage consists of Mn1 to Mn3 and Mp1 to Mp2. An output

stage with bias circuit reported in [41] achieves push-pull behavior with small die area consumption is used in the proposed op-amp. The second stage a push-pull stage consists of Mp3 and Mn4. Mbp and Mbn are used to bias the push-pull stage. Hybrid compensation is employed in the op-amp to save power while achieve high gain-bandwidth. Mc1 to Mc4 serves as common-mode feedback circuit.

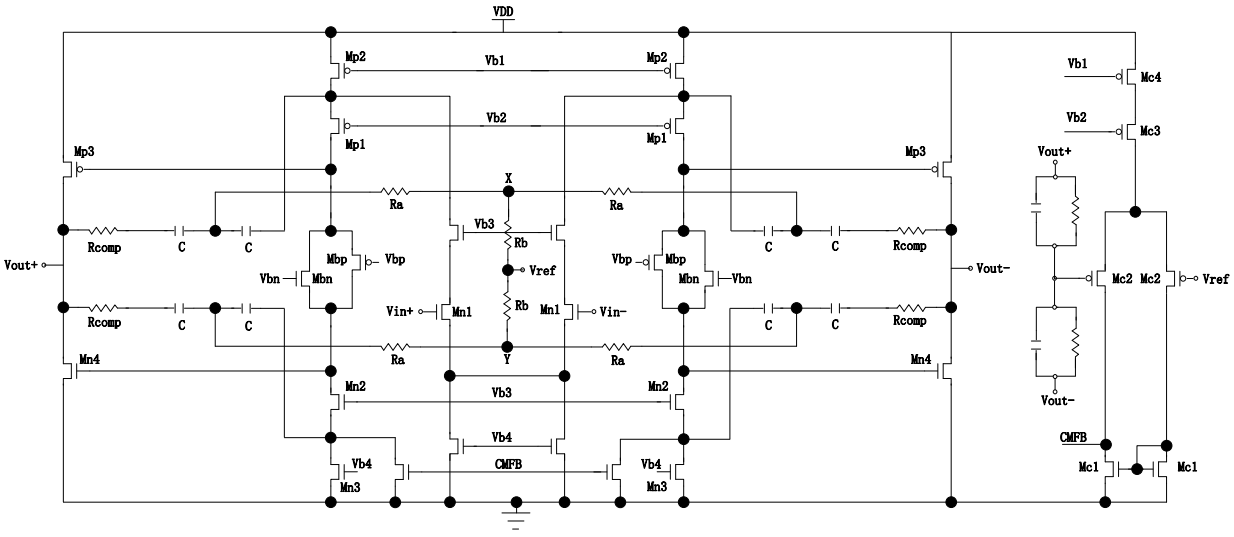


Figure 8.5 The bandwidth extended op-amp with push-pull output stage

A fast compensation method for single end op-amp is proposed in [42]. In this paper it has been further exploit for the hybrid compensated fully differential op-amp. The bandwidth extension is achieved by splitting the compensation capacitor into two series capacitors with the same value labeled C in the figure 8.5. The bode diagram of the proposed op-amp and traditional op-amp is shown in figure 8.6.

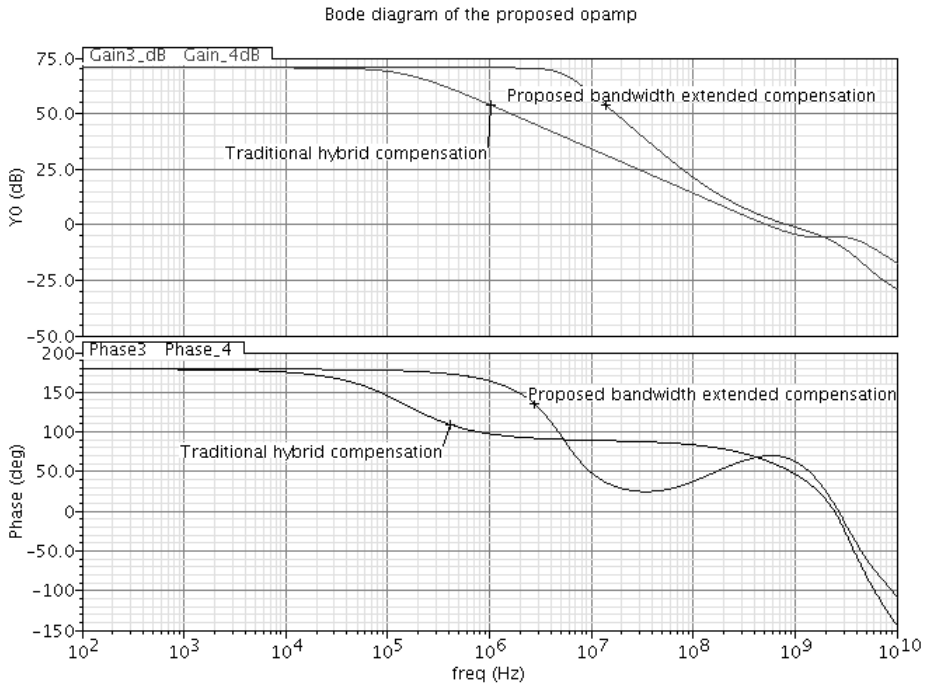


Figure 8.6 The bode diagram of proposed op-amp and traditional op-amp

As we can see in figure 8.6, traditional hybrid compensation op-amp has a classic 20dB/dec drop of gain over the frequency band after the dominant pole. The proposed op-amp extended the bandwidth over a decade without sacrificing too much phase margin. This bandwidth extension technique can be understood in an intuitive way. Ra is chosen to have smaller impedance compared to the impedance of C. Thus at low frequency, the signal will not see the whole Miller capacitor but go through Ra to an ac ground labeled as X and Y shown in the figure 8.5. Rb is chosen to be very large to have a high common-mode impedance seeing at node X and Y. At high frequency, however, the impedance of C becomes small compared to Ra, thus the signal will go through Miller capacitor and the gain has a sharp drop when the frequency approaching unity gain-bandwidth.

For integrated analog filters, a tuning circuit is necessary because of PVT variations. A tuning circuit based on digital delay lock loop is reported in [47]. In [47] an n bit counter is used

to switch the resistor array to adjust time constant. In this paper, a fast tuning circuit is proposed by using SAR controller. In the worst case n bit counter requires 2^n cycles to finish the tuning process, but for an n bit SAR controller it only requires n cycles to finish the tuning. The diagram of the tuning circuit is shown in figure 8.7. The goal of the tuning circuit is to associate the RC time constant with an external reference. In the proposed tuning circuit, the external reference is set by the delay block. In the actual implementation, the delay block is simply a divide-by-2 circuit so the reference becomes the period of the clock signal which can be controlled very accurately. The rising time of the voltage at the input of comparator is related to RC constant. The closed-loop operation will bring two inputs of latch closer which means tuning is finished.

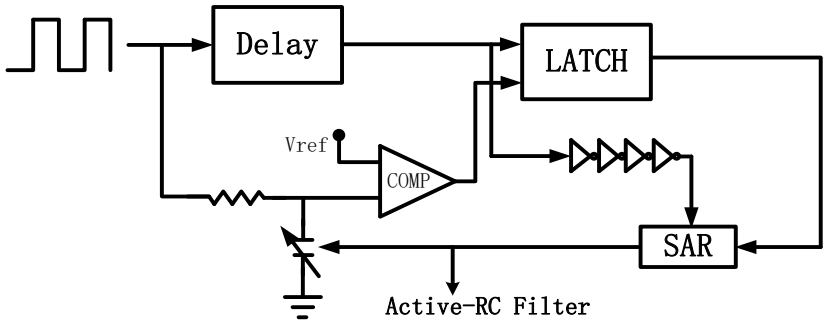


Figure 8.7 Simplified diagram of proposed fast tuning circuit

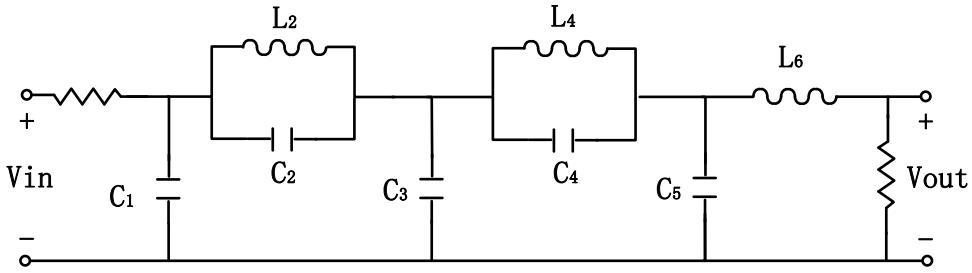
Table 5 Performance summary of the proposed 6^{th} order inverse-Chebyshev LPF

Process	0.13um CMOS
Filter Type	6^{th} order inverse-Chebyshev LPF with zero capacitor spread
Cutoff frequency tuning range	1MHz to 10MHz
Power supply	1.5V
1dB CP	13dBm
THD	-80dB with 2V Vppd input
Input-referred noise	60nV/sqrt(Hz)
Current consumption	6.3mA

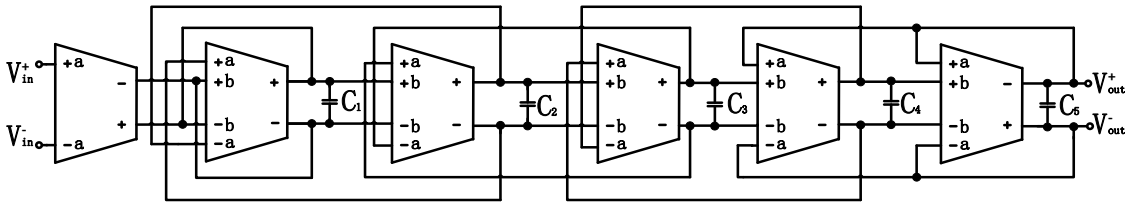
8.3 Design of 5th Order Fully Differential CMOS Transconductance-C Low Pass Filter

As mentioned previously active-RC filter has superior linearity performance, however, for high frequency applications, open-loop transconductance-C filter [48] is often preferred. The key point is designing tunable high frequency transconductance-C filter is to maintain the other aspects of performance while providing required programmable cutoff frequency. The transconductance (gm) cell should provide good high frequency performance over the entire tuning band.

In this work, a widely-tunable transconductance-C low pass filter with cutoff frequency tunable from 25MHz to 135MHz is proposed and implemented [43-44]. The architecture of the filter is synthesized based on a 5th order low pass Butterworth ladder prototype as shown in figure 8.8(a). The active circuitry implementation can be built based on the SFG of the passive ladder. The fully differential architecture consists of gm cell is shown in figure 8.8(b).



(a)



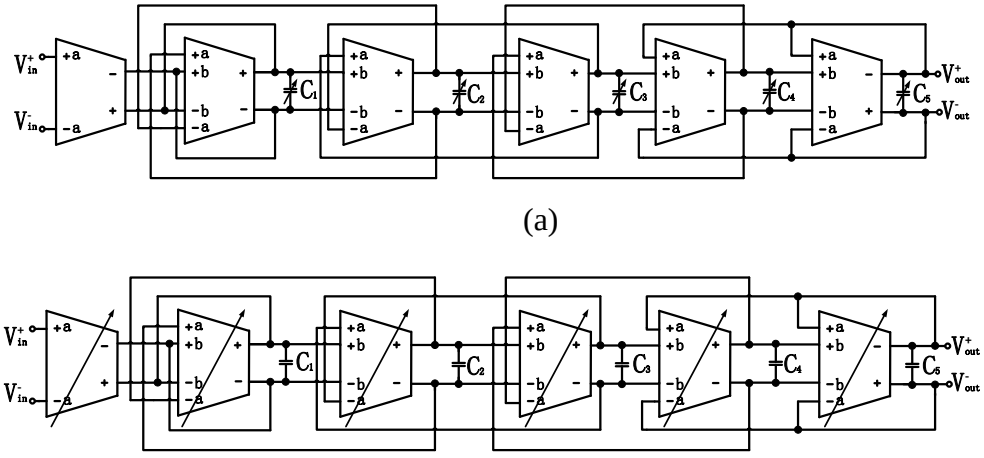
(b)

Figure 8.8 The ladder prototype (a) and the active realization (b) of fully differential 5th order Butterworth filter

The cutoff frequency of low pass transconductance-C filter is proportional to the time constant given in eqs. 8.4.

$$f_c \propto \frac{g_m}{C} \tag{8.4}$$

where gm indicates the transcendence of the gm cell, C indicates the loading capacitance. As shown in the Figure 8.8, there are two ways to achieve the programmability of the filter. One way is called constant gm topology in which fixed gm cell is used and the cutoff frequency is tuned by switching capacitor array. Another way is to use constant C topology meaning the capacitor is fixed and the frequency tuning is achieved by tuning transconductance of the gm cell. Constant gm topology simplified the design of gm cell because only one gm cell is needed in each stage. However, constant C approach can often lead to optimal balance between power and noise [49].



(a)

(b)

Figure 8.9 Transconductance-C filter using (a) constant gm topology, (b) constant C topology

As clearly show in eqs. 8.4, if constant gm approach is used, the gm needs to be predesigned to satisfy the highest cutoff frequency requirement which implies a waste of power consumption when lowest cutoff frequency is selected. Another issue raised by constant gm method is it may lead to unnecessary large capacitor area. This can be examined by assuming the minimum capacitor value to be $C_{\min}$, which satisfy the highest frequency requirement from eqs. 8.8.

$$f_{highest} = \frac{g_{m\_const}}{C_{\min}} \tag{8.5}$$

g_{m_const} is the gm value predesigned to satisfy the largest cutoff frequency. The capacitor value needed for the lowest cutoff frequency would be

$$C_{\max} = \frac{f_{highest}}{f_{lowest}} C_{\min} \tag{8.6}$$

where $f_{highest}$indicates the highest cutoff frequency f_{lowest} indicates the lowest cutoff frequency. It would be easy to see that large tuning range may lead to a waste of die area. This problem becomes severe when large capacitor spread exists because the minimum capacitor has to be realized accurately which posed a limitation of smallest overall capacitor area.

From the noise point of view, constant gm topology requires the filter to meet the noise budget at the highest frequency. This is because noise from the gm is constant which means the smallest capacitor determines the overall noise of the filter. Unlike constant gm topology, constant C topology experiences the same noise performance over the tuning band. To illustrate it clearly, the input referred noise of OTA cell is denoted as $\tilde{V}_{n\_gm}^2$ which satisfies the equation below,

$$\tilde{V}_{n\_gm}^2 \propto \frac{1}{g_m} \tag{8.7}$$

At high cutoff frequency gm value is high which means input referred noise is low which can be represented by $\tilde{V}^2_{n\_gm\_lo}$. The overall integrated noise is given by

$$\tilde{V}^2_{n\_overall1} = \int_0^{f_{hi}} \tilde{V}^2_{n\_gm\_lo} \tag{8.8}$$

At low cutoff frequency gm value is low which means input referred noise is high which can be represented by $\tilde{V}^2_{n\_gm\_hi}$. The overall integrated noise is given by

$$\tilde{V}^2_{n\_overall2} = \int_0^{f_{lo}} \tilde{V}^2_{n\_gm\_hi} \tag{8.9}$$

Based on eqs. 8.4, $\tilde{V}^2_{n\_gm\_hi}$ and $\tilde{V}^2_{n\_gm\_lo}$ satisfies

$$\frac{\tilde{V}^2_{n\_gm\_lo}}{\tilde{V}^2_{n\_gm\_hi}} = \frac{g_{m\_hi}}{g_{m\_lo}} \tag{8.10}$$

Therefore, we can derive the following

$$\frac{\tilde{V}^2_{n\_gm\_lo}}{\tilde{V}^2_{n\_gm\_hi}} = \frac{f_{hi}}{f_{lo}} \tag{8.11}$$

Reexamining eqs. 8.8, 8.9 and 8.11 we find that overall integrated noise is the same. To illustrate this intuitively, at high cutoff frequency though we have small input-referred noise but the integration bandwidth is wide, at low cutoff frequency the integration bandwidth is narrow but we have large input-referred noise. Thus the overall noise performance is determined by load capacitor value which means it is constant by using constant C topology.

Based on the discussion above, constant C topology is used in this filter. In order to make the gm value tunable, binary weighted unit gm cells are adopted. Compared to variable gm cell, this approach can maintain good power and linearity balance while provide programmability. Since continuous cutoff frequency tuning is not required in this filter and linearity performance is not critical in transmitter path, the OTA design is relaxed. The overall OTA consists of three binary

weighted gm cells is shown in figure 8.10. All the binary weighted gm cells consist of the same unit gm cell. Control signal is added to activate and deactivate the OTA, Gmf is fixed value and G_{m0} indicates the unit gm value. The corresponding gm value of the OTA is tunable from $G_{mf}+G_{m0}$ to $G_{mf}+7G_{m0}$.

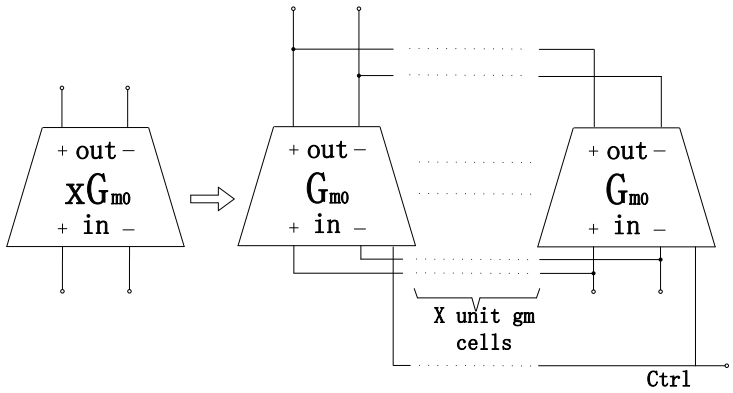


Figure 8.10 Tunable transconductance cell topology

An ideal OTA should have infinite input and output impedance. Linearity of the OTA design is of another important concern. There are different ways to improve the linearity of the OTA, some of them adopted complicated linearization techniques to achieve good linearity. But for high frequency operation, the internal node impedance of the OTA should be kept as small as possible to avoid parasitic poles. A simple linearity improvement approach is to use source degeneration technique, but it is at the cost of increasing power consumption. Since the input and output swing of the filter does not need to be very large, a simple fully differential folded-cascode amplifier with common-mode feedback is used as the unit gm cell as shown in figure 8.11. The gm cell has large output impedance and low impedance internal nodes.

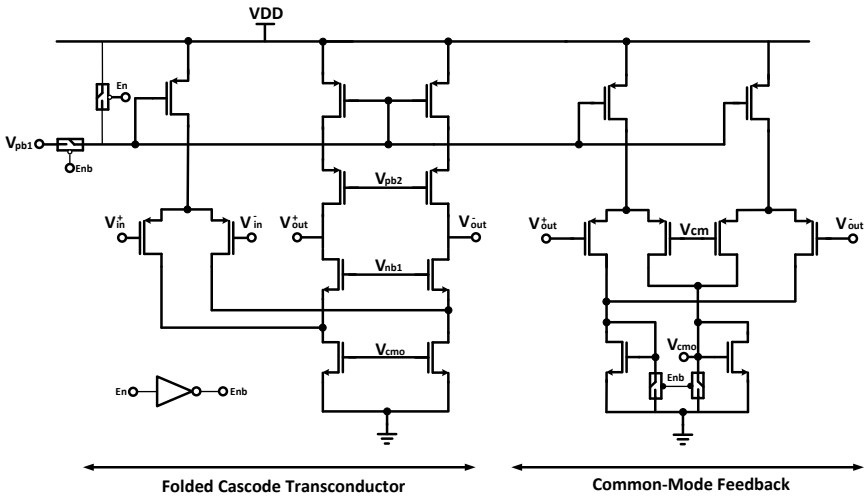


Figure 8.11 Schematic of unit gm cell

The switches shown in the schematic are used to switch on and off the unit gm cell. Switching off the unit gm cell is achieved by simply turning off the current sources of the main folded cascode amplifier and the common-mode feedback circuit. Another design consideration is the effect on pole position coming from parasitic load capacitance, the parasitic capacitances are relatively small compared to the load capacitance, thus switching on and off unit gm cells has negligible effect on pole positions.

The filter was fabricated in 0.13um CMOS process. Due to the 2.2V power supply thick-oxide CMOS transistors are used to prevent any breakdown issues. The die photo of the 5th order low pass filter is shown in figure 8.12. The core of the filter occupies an area of 550um*550um.

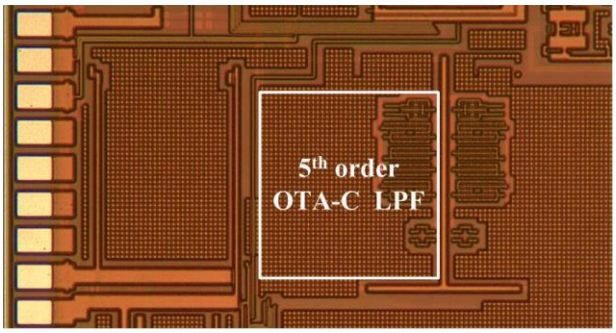


Figure 8.12 Die photo of the 5th order low pass filter

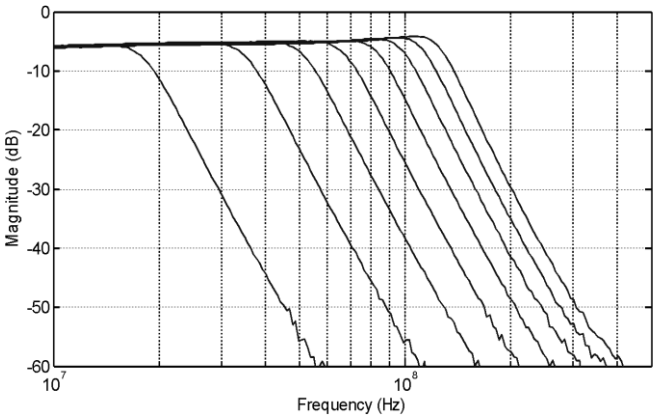


Figure 8.13 Measured frequency response of the 5th order low pass filter

Figure 8.13 shows the measured frequency response of the filter with the cutoff frequency tuned from 23MHz to 135MHz. Figure 8.14 shows the measured IIP3 of the proposed filter is 5 dBm. The filter performance is summarized in Table 6.

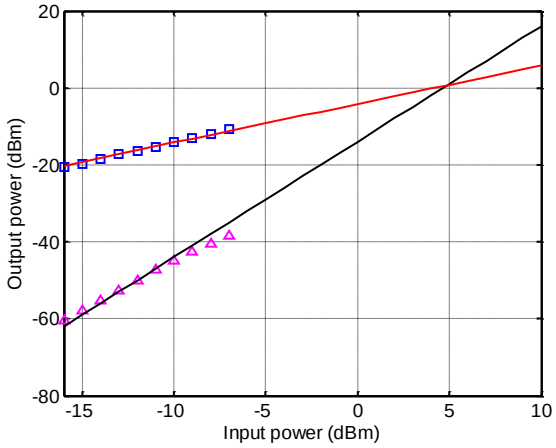


Figure 8.14 Measured IIP3 of the 5th order low pass filter

Table 6 Performance summary of 5th order low pass Butterworth prototype

Process	0.13um CMOS
Filter Type	5th order low pass Butterworth
Cutoff frequency tuning range	23-135MHz
IIP3	4.9 dBm
Power Supply	2.2V
Current Consumption	3mA at 18MHz cutoff frequency 25mA at 135MHz cutoff frequency
Area	550um*550um

Chapter 9 Conclusion and Future Work

9.1 Conclusion

This work extends the dual-residue architecture to use any sub-ADCs that can generate dual residues as reference for the succeeding sub-ADCs and to use any sub-ADCs that can take the dual residues as reference to terminate the pipeline. This extension allows use of efficient SAR sub-ADCs to remove the sub-ADC complexity and the RA linearity bottlenecks of the traditional parallel interpolation-based dual-residue ADCs. When small enough, the dual residues degenerate into the zero-crossing signals inherently available in multibit sub-ADCs, leading to much lower RA overhead. Small dual residues can be realized using a relatively high resolution 2b/cycle SAR sub-ADC for coarse quantization with little tradeoff in sub-ADC complexity and power efficiency. This results in a pipelined dual-residue SAR ADC architecture that preserves the SAR advantages of power efficiency and technology scalability using only ZX signals. The advantages are illustrated by design and comparison of an 11b pipelined two-step SAR to the state-of-the-art pipelined dual and single residue ADCs. To prevent aliasing for the sampling system, a 6^{th} order active-RC low pass filter and a 5^{th} order transconductance-C low pass filter have been discussed, the simulation and measurement results are shown to demonstrate the function and performance of the prototypes.

9.2 Future Work

The sub ADC can be designed with time domain interpolation quantizer, in general time domain design consist even more digital circuits which can benefit from technology scaling. The time step usually suffers from PVT variation but the proposed interpolation method can largely maintain the performance as long as the variation is matched which can be achieved by careful layout and properly sized transistor. The dual residues from coarse SAR can be converted into time domain by voltage-to-time converter (VTC) and their timing of the dual residues can be detected by a counter which can be implemented by a single TDC efficiently. Since only the relative timing is critical to calculate the zero crossing location, the end result is immune to the output timing of VTC and the time step variation in TDC.

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