

# **Control, Modeling, and Analysis of Inverter-Based Resources**

by

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## Abstract

The increased penetration level of Inverter-Based Resources (IBR) presents new challenges to the planning and operation of electric grids traditionally designed, protected, and operated based on the inherent characteristics of synchronous machines. Inverters do not have the same inherent properties as synchronous machines and respond based on their control algorithms. The inverter control and design are proprietary, resulting in black-box models provided by inverter manufacturers for proposed interconnections. This work develops a generic model specification and model prototype implementation in an electromagnetic transients simulator of an inverter applied in large IBR plants. The inverter control is designed and tuned to meet the voltage ride-through response performance requirements specified in IEEE P2800 Draft Standard for Interconnection and Interoperability of Inverter-Based Resources Interconnecting with Associated Transmission Systems. The control objective, process model, control implementation, and analytical tuning approach are detailed for each controller. Instantaneous sequence component detection methods proposed in the literature are investigated and modified to allow controlled negative sequence current injection. A current limit logic is developed to ensure the current in each phase is limited to the inverter's current limit and the prioritization of the incremental sequence components of the current is consistent with the performance requirements in IEEE P2800. Time-domain simulations in PSCAD™ show that the inverter model's low voltage ride-through response meets the performance specifications for symmetrical and asymmetrical faults. Further, comparisons of the time-domain simulations to laboratory testing measurements of a 2.2 MVA battery storage inverter verify the capability of the model to predict the controlled response of a commercial inverter for terminal voltages consistent with symmetrical and asymmetrical faults.

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## List of Abbreviations

$\alpha\beta$	Alpha-Beta Stationary Reference Frame
BESS	Battery Energy Storage System
dq	d-axis and q-axis Reference Frame (same as Synchronous Reference Frame)
DER	Distributed Energy Resource
DDSRF	Decoupled Double Synchronous Reference Frame
DSOGI	Dual Second Order Generalized Integrator
EHV	Extra High Voltage
FERC	Federal Energy Regulatory Commission
FFT	Fast Fourier Transform
FRT	Fault Ride-Through
HV	High Voltage
HVDC-VSC	High Voltage Direct Current – Voltage-sourced Converter
HVRT	High Voltage Ride-Through
IBR	Inverter-Based Resource
IUT	Inverter Under Test
LGIP	Large Generator Interconnection Procedures
LPF	Low Pass Filter
LVRT	Low Voltage Ride-Through

MW	Megawatt
NERC	North American Electric Reliability Corporation
OEM	Original Equipment Manufacturer
PCC	Point of Common Coupling
PI	Proportional-Integral Compensator
PLL	Phase-Locked Loop
POM	Point of Measurement
PPC	Power Plant Controller
PPS	Primary Power Source
pu	Per Unit
PV	Photovoltaic
PWM	Pulse Width Modulation
ROCOF	Rate of Change of Frequency
RMS	Root Mean Square
SCR	Short Circuit Ratio
SRF	Synchronous Reference Frame
STATCOM	Static Synchronous Compensator
VOC	Voltage Oriented Control
VRT	Voltage Ride-Through

VSC Voltage-Sourced Converter

WTG Wind Turbine Generator

## List of Symbols

$\mathbf{E}$	space vector of the inverter voltage
$f$	scalar
$\mathbf{f}$	vector
$\vec{f}$	space vector
$\hat{f}$	peak value
$\mathbf{F}$	phasor
$f^*$	reference setpoint
$f_1$	positive sequence component
$f_2$	negative sequence component
$\mathbf{f}_{\alpha\beta}$	$\alpha\beta$ components
$\mathbf{f}_{dq}$	d-axis and q-axis components
$f_s$	switching frequency
$\mathbf{i}$	space vector of the inverter output current
$I_{cap}$	DC link capacitor voltage current
$i_{d1}$	positive sequence d-axis component of inverter output current
$i_{d2}$	negative sequence d-axis component of inverter output current
$i_{p1}$	magnitude of the positive sequence active current phasor

$i_{p2}$	magnitude of the negative sequence active current phasor
$I_{pv}$	PV array DC current
$i_{q1}$	positive sequence q-axis component of inverter output current
$i_{q2}$	negative sequence q-axis component of inverter output current
$i_{r1}$	magnitude of the positive sequence reactive current phasor
$i_{r2}$	magnitude of the negative sequence reactive current phasor
$\theta$	Instantaneous phase angle of the space vector of the grid voltage
$\theta_{PLL}$	phase angle of the PLL
$V_{dc}$	DC link voltage
$\mathbf{v}_g$	space vector of the grid voltage
$V_{pv}$	PV array DC voltage
$\mathbf{v}_t$	space vector of the inverter terminal voltage at the PCC
$\omega$	angular frequency of the grid
$\omega_0$	nominal angular frequency of the grid
$\omega_{PLL}$	angular frequency of the PLL

# **1. Introduction: The Changing Electrical Transmission Grid**

## **1.1. Recent Trends in the Increase of Renewable Energy**

A recent report by Lawrence Berkeley National Labs indicates a few noteworthy trends in the increased renewable energy installations. Specifically, the report noted that from 2015-2019, 59% of all new generation capacity added in the U.S. was either solar or wind [1]. It is forecasted that more than 80% of the new generation capacity in 2021 will be either solar, wind, or battery resources [2]. A survey of generator interconnection queues indicates that this trend is expected to continue. At the end of 2020, approximately 755 GW of generation capacity was in interconnection queues in the U.S., with 90% being solar, wind, or storage [3]. The report also indicates a significant uptick in battery storage. To put this in perspective, the total generation capacity in the U.S. as of 2021 is estimated to be ~1200 GW [4]. Note that [3] also indicates that less than a quarter of the proposed generation in the interconnection queues reaches commercial operation.

An example of this trend is evident in Texas. The Electric Reliability Council of Texas (ERCOT) operates the electric grid for 90 percent of the state of Texas. ERCOT's record peak load is 74,820 MW set in August of 2019 [5]. A snapshot of the generator interconnection queue in November of 2020 shows over 134 GW of proposed generation. Of this total, over 126 GW are resources such as wind, solar, and batteries that will be connected to the grid via power electronic converters [6].

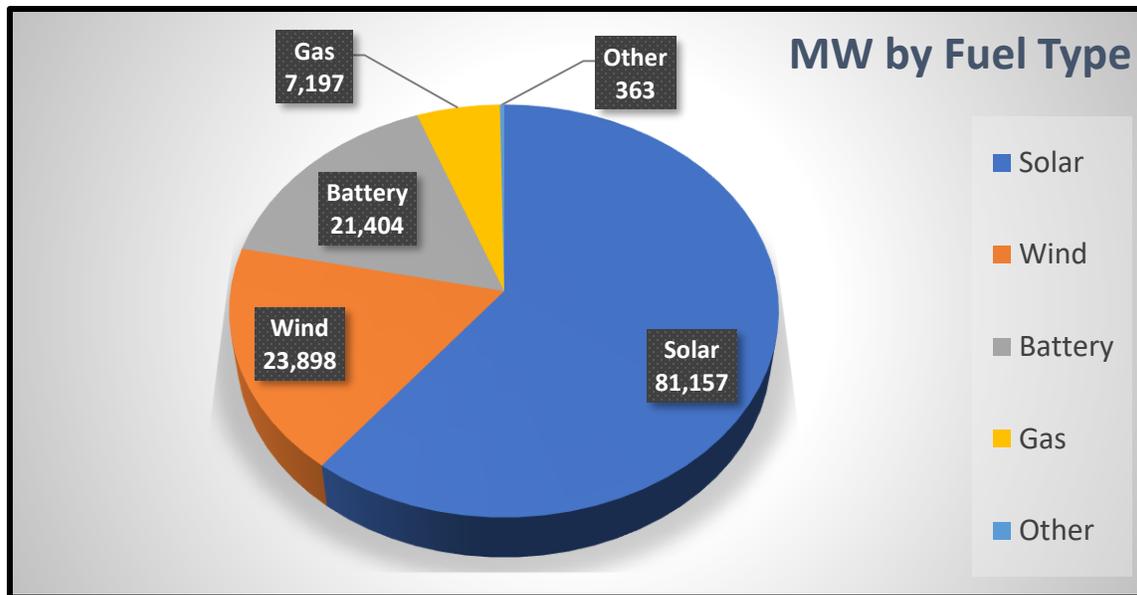


Figure 1-1: 11-2020 Snapshot of Generation Resource Interconnection Request in ERCOT adapted from [6]

From the grid planning perspective, the installed capacity of renewable energy only tells part of the story. Since the fuel cost of wind and solar is essentially zero, once the plant is installed, it is typically operated to extract the maximum available power from the resource. Therefore, an arguably equally important metric is the instantaneous penetration level of renewable resources at any given time. Grid planners and operators must account for these peak hours to ensure grid stability is maintained. For example, in ERCOT, the installed capacity of wind accounted for 23.3% of the total generating capacity in 2020; however, the instantaneous wind penetration level reached 59.3% in May 2020 [5]. A similar example is the Southwest Power Pool (SPP), where the installed capacity of wind accounts for 24.9% of the total generating capacity, but the instantaneous penetration level of wind reached 72.4% in April of 2020 [7-9]. This was quickly surpassed with an instantaneous wind peak of 81.85% in March of 2021 [10]. Furthermore, SPP has ~91 GW of IBR in their interconnection queue, of which ~47 GW is wind, ~35 GW is PV, and ~9 GW is battery, that are not yet in commercial operation as of January 2021 [11].

## 1.2. Power Electronics Coupled Generation

The main interest in this topic is because renewable energy technologies such as solar PV are connected to the grid via power electronic converters. Furthermore, the dynamics of power electronics coupled generators are fundamentally different from those of traditional synchronous generators. The response of a synchronous generator to changes in terminal voltage magnitude, phase, and frequency occurs naturally based on the design of the machine, followed by the response of the excitation and speed governing systems. Conversely, the dynamics of power electronics coupled generators are largely determined by the controllers of the inverter converting the DC power to AC power at the system frequency and voltage [12]. For this reason, they are commonly referred to as Inverter-Based Resources (IBR) in North America [13].

The inverter and its controllers have dynamics ranging from the nano-second time frame of the turn-on and turn-off time of the power electronic switches to the seconds time frame for higher-level controls. The wide range of potential dynamics of IBR led to a revision of the Power System Dynamic Performance Committee of IEEE definition and classification of power system stability to include converter-driven stability [14, 15]. The converter-driven stability is further classified into fast interaction converter-driven stability on the order of 100s of Hz to kHz and slow-interaction converter-driven stability typically in the subsynchronous frequency range [15]. Figure 1-2 superimposes the closed-loop bandwidth of the different converter controllers discussed in Chapter 3, the converter-driven stability definitions introduced in [15], and the response time of traditional synchronous machine governor and excitation systems. This chart also can be used as a starting point to determine how detailed the IBR model needs to be depending on the bandwidth of the phenomena of interest.

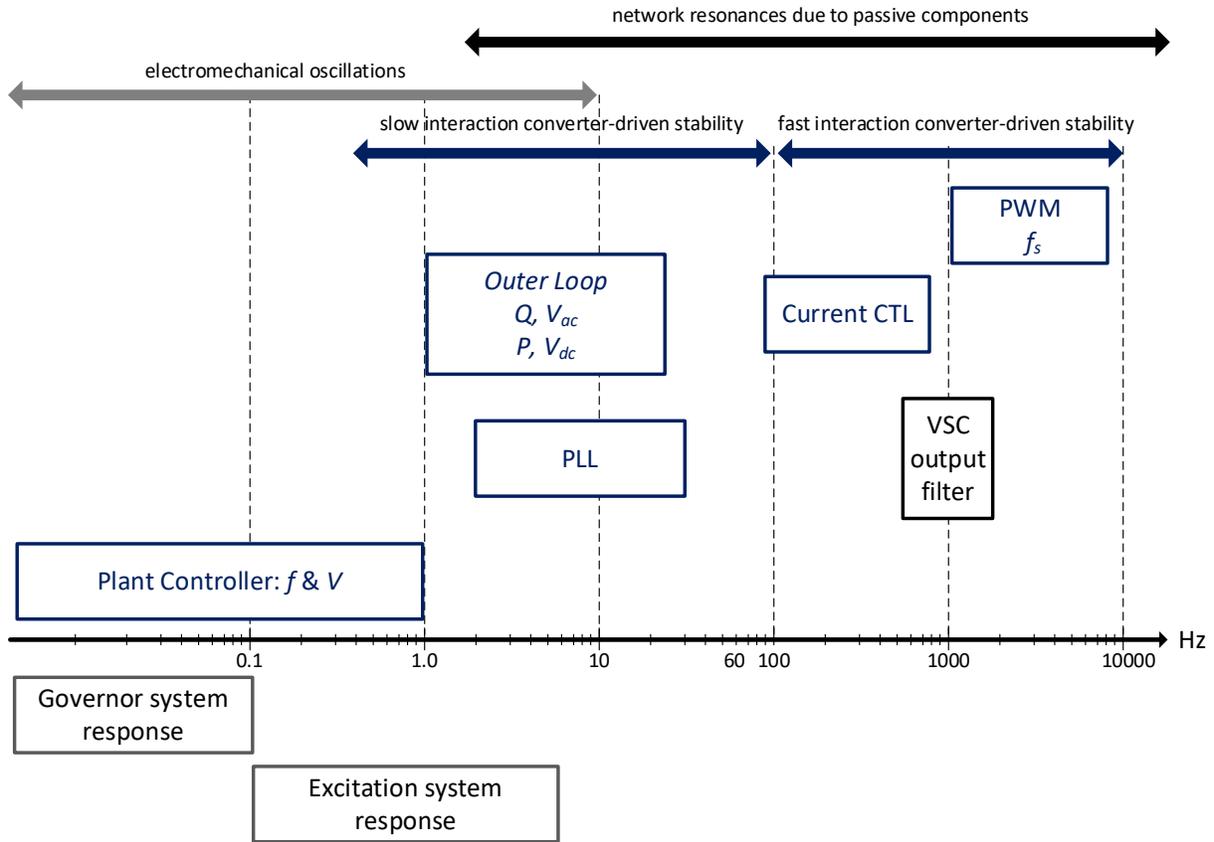


Figure 1-2: Illustration of converter controller closed-loop bandwidth and the response time of traditional synchronous generator excitation and governor control.

While increased penetration levels of IBR present a challenge to existing grid planning and operation norms, it also presents an opportunity as these devices are highly controllable compared to synchronous machines. Due to the IBR response being largely determined by its control, the grid planner can, to some extent, prescribe the desired performance of the IBR. Therefore, to make informed grid planning strategies and performance requirements, researchers and grid planners need appropriate tools to investigate the desired controlled response of the resources in future grids considering the full range of the dynamics present.

### **1.3. Detailed Models of IBR**

The interconnection process for large IBR plants is governed by the Federal Energy Regulatory Commission (FERC), which sets the Large Generator Interconnection Procedures (LGIP) in the U.S. For the required studies as part of this process, the plant developer provides the modeling information for the proposed plant. The modeling requirements imposed by grid planners vary significantly across the U.S. However, the current trend is towards very detailed models of the IBR implemented in an electromagnetic transients (EMT) simulation tool. These simulation tools allow for modeling the IBR and their controls in a high level of detail at the expense of increased computational burden and data requirements compared to positive sequence fundamental frequency transient stability simulation tools.

To protect the proprietary nature of the inverter controls and hardware design, the detailed inverter models provided by the inverter OEMs are typically black box models. Black box models limit the end-user's visibility into the control structure, parameters, settings, and control signals. The level of black-boxing of the model tends to vary by inverter OEM. For example, some OEMs black box the entire model such that the only thing accessible to the end-user is the AC terminal voltage and output current of the inverter. Other OEMs may only black box the inverter level control. While necessary to protect the secrecy of the design and control, it presents a challenge for grid planners and operators tasked with planning and operating the electric grid. For example, if a simulation shows instability or tripping of an IBR, how does one determine the cause of the issue and potential solutions? In practice, any uncertainties in the model's response must be addressed by the model developer and inverter OEM. It is easy to see how this problem grows as more of such models are in the study case.

The previous example was based on studies of a proposed or operational IBR plant where the inverter OEM is known. Another consideration is the long-term planning process. In this case, futuristic studies are performed over a range of generation, load, and network expansion assumptions. In this case, open and configurable models of IBR are needed. These types of studies can help determine the necessary expansion of the transmission system and necessary performance requirements of IBR interconnecting to the transmission system.

#### **1.4. Generic Models**

Generic models are publicly available, open, and configurable models that aim to represent the response of a device or piece of equipment not limited to a specific OEM's control or design. They are commonly implemented and maintained by the simulation software vendors reducing computer science related issues. The open nature and documentation of these models facilitate ease of configuration for sensitivity analysis and insight into a particular observed issue.

Generic models are widely used in fundamental frequency positive sequence transient stability simulations in North America. The second-generation renewable energy system models are used to represent IBR plants, including PV, wind, and battery [16]. The demerit given to generic models is that they are not based on the exact proprietary control of the inverter. However, [17-19] show the efficacy of these generic models for dynamics that are observable in positive sequence transient stability simulators.

EMT models of IBR have also been proposed and developed [20, 21]. EMTP® includes a PV plant model in their renewable energy toolbox [22]. PSCAD™ provides a publicly available PV plant model on their knowledge base website [23]. However, there is a need to have verified generic EMT models of the different types of IBR that are open, publicly available, and commonly

implemented across the EMT software platforms. In 2021, CIGRE convened a new working group, C4.60, with a focus on generic EMT models of IBR [24]. This group includes grid planners, inverter OEMs, researchers, and EMT software vendors. One of the objectives of this working group is to provide generic EMT models for different types of IBR.

## **1.5. Research Focus**

This dissertation focuses on the control and modeling of an inverter applied in a transmission connected IBR plant. Given that the control and design of commercial inverters are proprietary, the performance specifications in the draft IEEE P2800 standard [25] are used to develop and tune generic inverter controllers. Of primary interest is the control necessary to meet the low voltage ride-through (LVRT) response performance requirements in IEEE P2800 and the German (VDE) [26, 27] and Spanish (NTS) [28] applications of the European Grid Code [29]. The increased complexity of the control design due to performance specifications based on phasor domain quantities is investigated in this research.

## **1.6. Organization of the Dissertation**

Following the introduction in this chapter, Chapter 2 describes the modeling of a two-level voltage-sourced converter (VSC). Chapter 3 details the control of the VSC in both normal and abnormal grid conditions. Chapter 4 presents the verification of the model prototype based on the voltage ride-through (VRT) performance requirements in the IEEE P2800 draft standard and with measured data from laboratory testing of a commercial MW-scale inverter. Chapter 5 discusses the conclusions of this work and ideas for future work.

## 2. Modeling of the VSC

This chapter presents the model of a two-level VSC. For generation resources connected to the grid via VSC, the VSC mostly operates in the inverter mode. Therefore, in this context, the VSC is commonly referred to as an inverter. However, for resources such as batteries, the VSC operates in both rectifying and inverter modes corresponding to the charging and discharging of the battery. Further, if there is no DC input power from the PPS, there is the capability to operate the VSC as a STATCOM to provide reactive support. In this case, the VSC will absorb active power to maintain the DC bus voltage<sup>1</sup>. In this chapter, it is assumed that the PPS of the inverter is PV arrays.

Presently, large bulk-connected PV plants are typically designed with 10s to 100s of central inverters with ratings on the order of 1 to 5 MVA. Central PV inverters are assumed to be single-stage without a DC-DC converter on the DC side. Reference [30] indicates the single-stage design is common due to reduced cost and higher efficiency for higher power ratings. Numerous topologies of three-phase inverters are proposed in literature, including two-level, three-level, and modular multiple-level converters used in high power design such as HVDC-VSC. Reference [31] provides an overview of the basics of these common topologies. The generic PV inverter in this work is assumed to be a two-level, three-phase VSC with an LCL output filter. The switching model and averaged model representations of the inverter are presented. The LCL output filter

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<sup>1</sup> An example is “night-var” operation of a PV inverter.

parameterization is then detailed based on the inverter rating and switching frequency. Inverter modeling simplifications useful for control design and analysis are highlighted.

## 2.1. Switching Model

A two-level, three-phase PV inverter model is shown in Figure 2-1. The PV inverter consists of a DC bus capacitor and three half-bridge legs. The power electronics switches are assumed to be IGBTs each with an antiparallel diode. The turn-on and turn-off dynamics and solid-state characteristics of the power electronic switches are not of interest in this model. Thus, each IGBT and antiparallel diode combination is assumed to be an ideal switch.

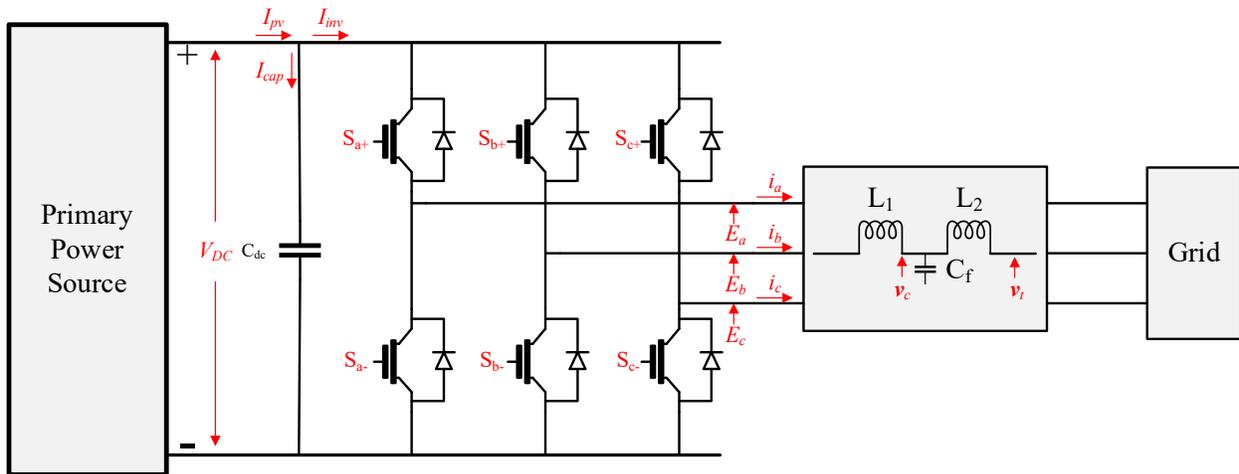


Figure 2-1: Three-phase, two-level PV inverter.

The gate pulses of the IGBTs are determined by the PWM scheme to synthesize the desired output voltage,  $E^*$ . The PWM scheme implemented in this model utilizes a triangle carrier signal of amplitude of 1.0 and frequency,  $f_s$ , corresponding to the switching frequency. The modulating signal,  $\mathbf{m}_{abc}$ , is based on the desired output voltage. The PWM control block diagram is shown in Figure 2-2. If the modulating signal is greater than the carrier signal, the corresponding switch control signal,  $S_+$ , is a logical 1. If the modulating signal is less than the carrier signal, the

corresponding switch control signal,  $S_-$ , is a logical 1. The implemented PWM scheme is simplified in that it does not include the intentional delay or dead time added to prevent short-circuiting the DC positive rail to the DC negative rail [32].

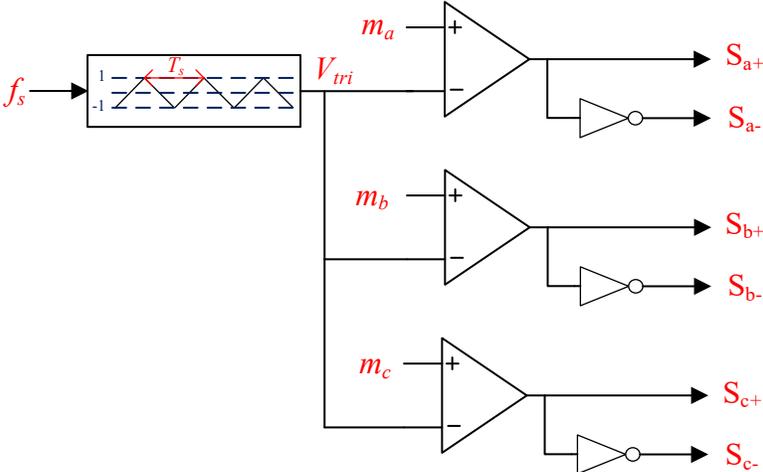


Figure 2-2: PWM control scheme.

The output phase voltages switch between the positive and negative rail of the VSC. In this model, the negative rail is assumed to be grounded resulting in the inverter output voltage switching between  $+V_{DC}$  and  $0V$ . Figure 2-3 shows the control signals of the PMW scheme, the inverter output phase-to-ground voltages, and inverter output phase-to-phase voltages.

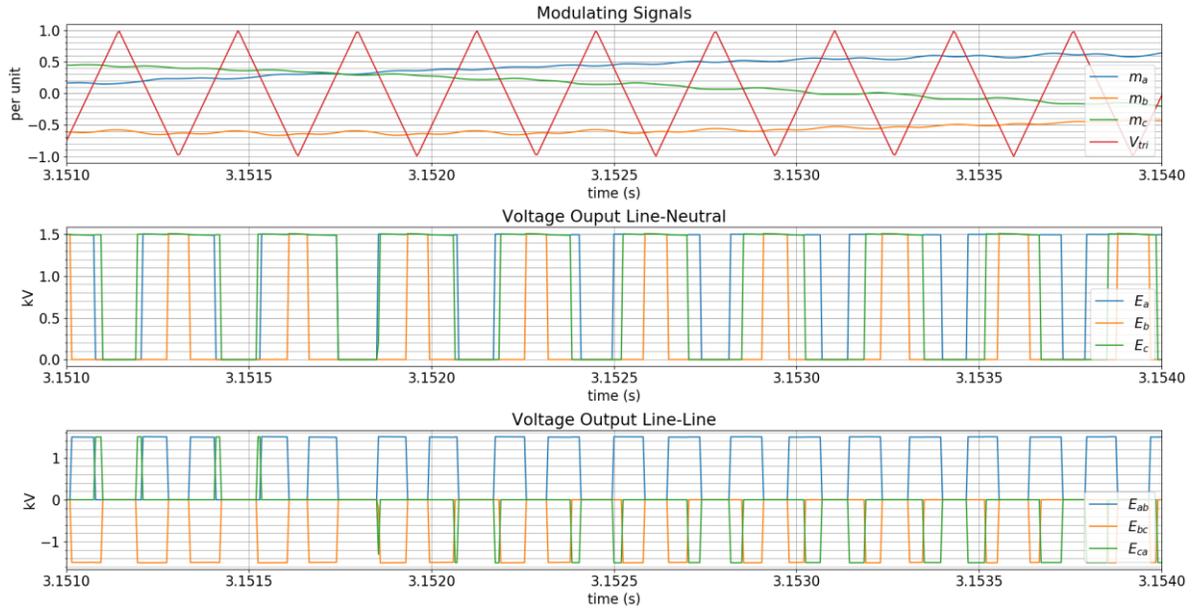


Figure 2-3: PWM scheme signals and resulting output voltage. Top plot: modulating signals  $m_a$ ,  $m_b$ , and  $m_c$ , and the carrier signal  $v_{tri}$ . Middle plot: inverter output voltage line-neutral. Bottom plot: inverter output voltage line-line.

Reference [33] examines the output voltage of a single leg of a PWM VSC analytically by developing the Fourier series of a signal with two time variables; the modulating signal as a function of  $2\pi f_0 t$  and the carrier signal as a function of  $2\pi f_s t$ . The resulting decomposition in exponential form in terms of the notation in this work is provided in (1). The main conclusion is that the resulting wave form consists of a DC component, components at harmonics of the fundamental, components at harmonics of the switching frequency, and components at the sidebands of the switching frequency. Further, for the sine-triangle modulation scheme, the coefficients  $E_{n0}$  are all zero except for the fundamental,  $E_{10}$ . Thus, the harmonic spectrum of the voltage output of a sinusoidal PWM VSC is concentrated at harmonics of the switching frequency and its sidebands.

$$\begin{aligned}
E(t) &= E_{00} + \sum_{n=-\infty}^{\infty} E_{n0} e^{jn2\pi f_0 t} + \sum_{m=-\infty}^{\infty} E_{0m} e^{jm2\pi f_s t} \\
&+ \sum_{\substack{n=-\infty \\ n \neq 0}}^{\infty} \sum_{\substack{m=-\infty \\ m \neq 0}}^{\infty} E_{nm} e^{j(n2\pi f_0 + m2\pi f_s)t} \\
&= \frac{V_{dc}}{2} + m(t) \frac{V_{dc}}{2} + \sum_{\substack{n=-\infty \\ n \neq 0}}^{\infty} \sum_{\substack{m=-\infty \\ m \neq 0}}^{\infty} E_{nm} e^{j(n2\pi f_0 + m2\pi f_s)t}
\end{aligned} \tag{1}$$

For a three-phase VSC, choosing the switching frequency as an integer multiple of three is advantageous as the triplen harmonics cancel in the line-line voltage [34]. Therefore, the default switching frequency used in the PWM scheme in the model prototype in this work is  $f_s = 3060$  Hz corresponding to the 51<sup>st</sup> harmonic of the fundamental frequency,  $f_0 = 60$  Hz. The harmonics spectrum of the line-to-neutral voltage of phase A is shown in Figure 2-4. The harmonics are concentrated at the switching frequency and its sidebands as predicted in (1). Figure 2-5 shows that the component at the switching frequency is not present in the harmonic spectrum of the line-to-line voltage.

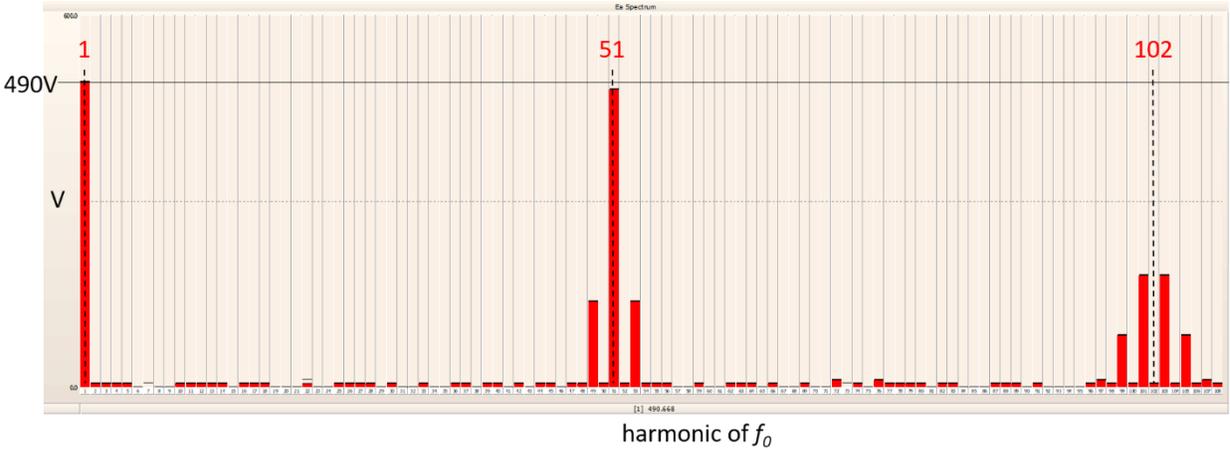


Figure 2-4. Harmonic spectrum of the output line-to-neutral voltage of the generic 2-level, 3-phase, PWM inverter model with a switching frequency of 3060 Hz. The vertical scale is voltage and the horizontal axis is harmonic of  $f_0$ .

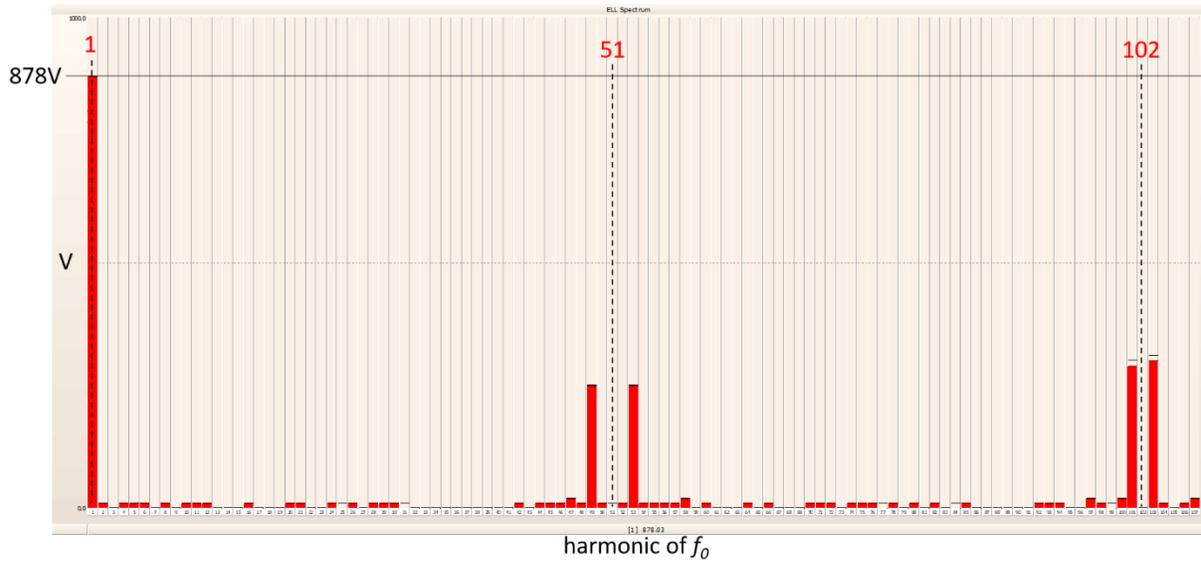


Figure 2-5. Harmonic spectrum of the output line-to-line voltage of the generic 2-level, 3-phase, PMW inverter model with a switching frequency of 3060 Hz. The vertical scale is voltage and the horizontal axis is harmonic of  $f_0$

## 2.2. Averaged Model

The averaged model representation of switched dc-dc converters was proposed in [35] showing that switched dc-dc converters can be approximated for low frequency dynamics with a continuous model based on the average of the switch duty ratio. From a control design perspective, this relates the plant output to the control signal input, in this case the duty ratio. From a simulation perspective, this simplification reduces the computational burden. For example, if the switching of the power electronic switches is not modeled, the numerical integration time step can be increased. The justification of averaging is based on linear system theory where a system of low pass characteristics will reject high-frequency components of the input [36]. This prerequisite holds true for the current-controlled VSC. For example, Section 2.3 details the output filter of the VSC used to attenuate high frequency components and Section 3.2 details the closed-loop current control which is designed with a bandwidth much less than the PWM switching frequency. The averaged model representation is common for the control design and analysis of the VSC [31] and

is used for this purpose in this work. This section presents the averaged model representation of the PV inverter assumed in this work such that the assumptions and approximations are documented to provide insight into potential limitations.

If the switching frequency is much greater than the fundamental frequency, the dynamics of the switching will not have much impact on the dynamics related to the fundamental frequency. Ideally, if the switching frequency is infinite, the synthesized output voltage only contains a fundamental frequency component equal to the reference voltage,  $E^*$ . To develop the averaged model of the VSC, the average value of the state variables is determined. In this case, the state variables are the inductor current and the capacitor voltage.

Considering one leg of the two-level, three-phase VSC shown in Figure 2-1, the output current through the inductor is given by:

$$\frac{di(t)}{dt} = \frac{1}{L_f} (E(t) - Ri(t) - V_g(t)) \quad (2)$$

and the DC link capacitor voltage is given by:

$$I_{pv} - I_{inv} = C \frac{dV_{dc}}{dt} \quad (3)$$

The inverter output voltage and current will contain ripple related to the switching frequency as shown in (1). The average values of the inverter voltage and current are determined over one switching period in terms of the duty ratio of the switches. Figure 2-6 shows the two circuit configurations of the VSC based on the positions of S1 and S4.

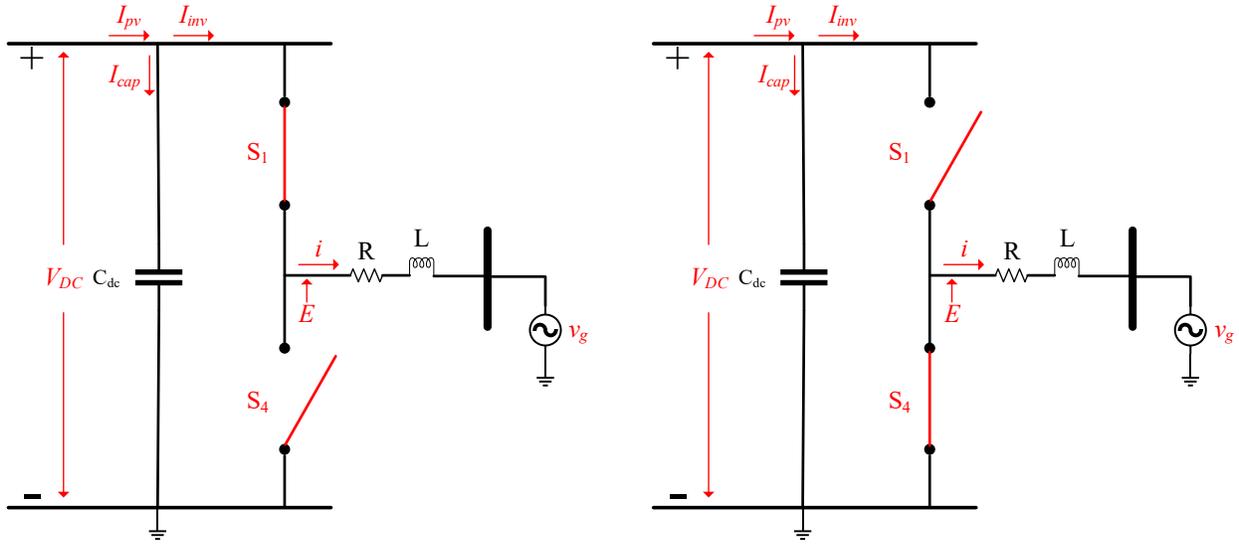


Figure 2-6. VSC circuit based on switch position. Left: switch S1 closed and the bottom switch S4 open. Right: top switch S1 open and the bottom switch S4 closed.

With S1 closed and S4 open, the AC side of the VSC is directly tied to the positive rail resulting in:

$$E(t) = V_{dc} \quad (4)$$

$$I_{cap} = I_{pv} - i(t) \quad (5)$$

With S1 open and S4 closed, the AC side of the VSC is directly tied to the negative rail which is grounded resulting in:

$$E(t) = 0 \quad (6)$$

$$I_{cap} = I_{pv} \quad (7)$$

The moving average of a signal over the period  $T_s$  is calculated as:

$$\langle x(t) \rangle_{T_s} = \frac{1}{T_s} \int_{t-T_s}^{T_s} x(t) dt \quad (8)$$

Applying the moving average over a switching period to the DC current and output voltage shows these quantities are related to the duty ratios of S1 and S4;  $d_1$  and  $d_4$ .

$$\langle E(t) \rangle_{T_s} = \frac{1}{T_s} \int_0^{T_s} E(t) dt = \frac{1}{T_s} \int_0^{d_1 T_s} V_{dc} dt = d_1 V_{dc} \quad (9)$$

$$\begin{aligned} \langle I_{cap} \rangle_{T_s} &= \frac{1}{T_s} \int_0^{T_s} I_{cap} dt = \frac{1}{T_s} \int_0^{d_1 T_s} (I_{pv} - i(t)) dt + \frac{1}{T_s} \int_{d_1 T_s}^{T_s} I_{pv} dt \\ &= \langle I_{pv} \rangle_{T_s} - d_1 \langle i \rangle_{T_s} \end{aligned} \quad (10)$$

Note that the assumption in (9) and (10) is that the state variables' dynamics are slower than the switching frequency. The dynamic equations of the averaged signals in terms of the duty ratio of S1:

$$\frac{d}{dt} \langle i \rangle_{T_s} = \frac{1}{L} (d_1 \langle V_{dc} \rangle_{T_s} - R \langle i \rangle_{T_s} - \langle V_g \rangle_{T_s}) \quad (11)$$

$$\frac{d}{dt} \langle V_{dc} \rangle_{T_s} = \frac{1}{C} (\langle I_{pv} \rangle_{T_s} - d_1 \langle i \rangle_{T_s}) \quad (12)$$

It is desired to write the equations in terms of the modulating signal, given it is the control output signal of the inverter control. The modulating signal can be related to the duty ratio by noting the duty ratio varies between 0 and 1, while the modulating signal varies between -1 and 1. This results in the following relationship:

$$d = \frac{m + 1}{2} \quad (13)$$

The dynamic equations written as functions of the modulating signal are:

$$\begin{aligned}\frac{d}{dt}\langle i \rangle_{T_s} &= \frac{1}{L} \left( \left( \frac{m+1}{2} \right) \langle V_{dc} \rangle_{T_s} - R \langle i \rangle_{T_s} - \langle V_g \rangle_{T_s} \right) \\ &= \frac{1}{L} \left( \frac{\langle V_{dc} \rangle_{T_s}}{2} + \frac{m \langle V_{dc} \rangle_{T_s}}{2} - R \langle i \rangle_{T_s} - \langle V_g \rangle_{T_s} \right)\end{aligned}\quad (14)$$

$$\begin{aligned}\frac{d}{dt}\langle V_{dc} \rangle_{T_s} &= \frac{1}{C} \left( \langle I_{pv} \rangle_{T_s} - \left( \frac{m+1}{2} \right) \langle i \rangle_{T_s} \right) \\ &= \frac{1}{C} \left( \langle I_{pv} \rangle_{T_s} - \frac{\langle i \rangle_{T_s}}{2} - \frac{m \langle i \rangle_{T_s}}{2} \right)\end{aligned}\quad (15)$$

The component of (14) corresponding to the averaged value of the VSC output voltage over a switching period is consistent with the DC offset and low frequency terms in (1). The dynamic equations can be extended to represent a three-phase VSC.

$$\frac{d}{dt}\langle i_a \rangle_{T_s} = \frac{1}{L} \left( \frac{\langle V_{dc} \rangle_{T_s}}{2} + \frac{m_a \langle V_{dc} \rangle_{T_s}}{2} - R \langle i_a \rangle_{T_s} - \langle V_{ga} \rangle_{T_s} \right) \quad (16)$$

$$\frac{d}{dt}\langle i_b \rangle_{T_s} = \frac{1}{L} \left( \frac{\langle V_{dc} \rangle_{T_s}}{2} + \frac{m_b \langle V_{dc} \rangle_{T_s}}{2} - R \langle i_b \rangle_{T_s} - \langle V_{gb} \rangle_{T_s} \right) \quad (17)$$

$$\frac{d}{dt}\langle i_c \rangle_{T_s} = \frac{1}{L} \left( \frac{\langle V_{dc} \rangle_{T_s}}{2} + \frac{m_c \langle V_{dc} \rangle_{T_s}}{2} - R \langle i_c \rangle_{T_s} - \langle V_{gc} \rangle_{T_s} \right) \quad (18)$$

$$\begin{aligned}\frac{d}{dt}\langle V_{dc} \rangle_{T_s} &= \frac{1}{C} \left( \langle I_{pv} \rangle_{T_s} - \frac{\langle i_a \rangle_{T_s}}{2} - \frac{\langle i_b \rangle_{T_s}}{2} - \frac{\langle i_c \rangle_{T_s}}{2} - \frac{m_a \langle i_a \rangle_{T_s}}{2} - \frac{m_b \langle i_b \rangle_{T_s}}{2} \right. \\ &\quad \left. - \frac{m_c \langle i_c \rangle_{T_s}}{2} \right)\end{aligned}\quad (19)$$

For a three-wire system, there is no zero-sequence current. Therefore (19) can be simplified to:

$$\frac{d}{dt} \langle V_{dc} \rangle_{T_s} = \frac{1}{C} \left( \langle I_{pv} \rangle_{T_s} - \left( \frac{m_a \langle i_a \rangle_{T_s}}{2} + \frac{m_b \langle i_b \rangle_{T_s}}{2} + \frac{m_c \langle i_c \rangle_{T_s}}{2} \right) \right) \quad (20)$$

The averaged model representation of the PV inverter is shown in Figure 2-7. Corresponding to (16)-(19), the controlled voltage sources and current source are driven by the following equations:

$$E_a = \frac{m_a V_{dc}}{2} \quad (21)$$

$$E_b = \frac{m_b V_{dc}}{2} \quad (22)$$

$$E_c = \frac{m_c V_{dc}}{2} \quad (23)$$

$$I_{inv} = \frac{m_a i_a(t)}{2} + \frac{m_b i_b(t)}{2} + \frac{m_c i_c(t)}{2} \quad (24)$$

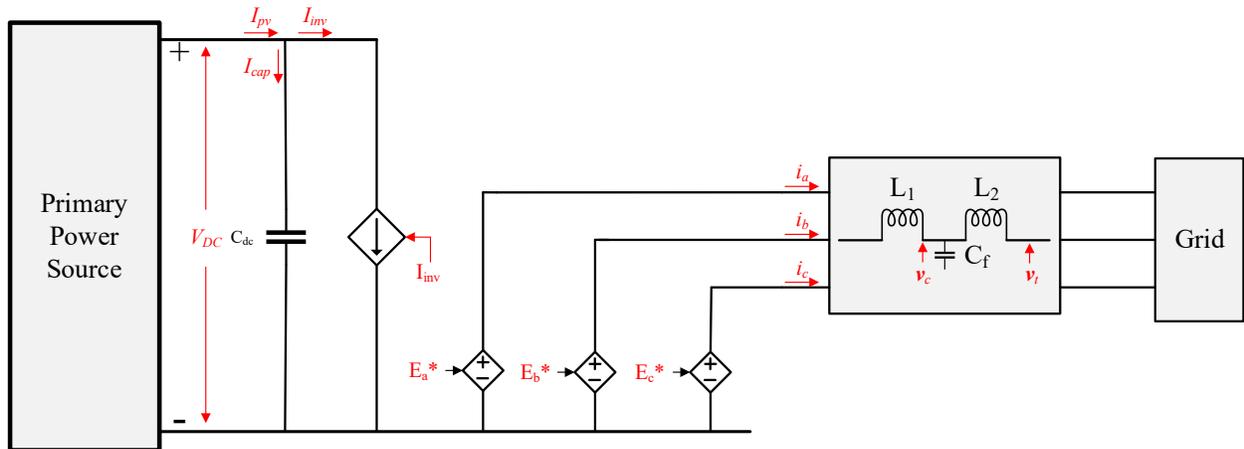


Figure 2-7: Averaged model representation of the 3-phase 2-level VSC.

The previous derivations provide insight into the potential limitations of the averaged model representation of the VSC. It is shown in [37] that the averaging operator in the time-domain in

(8) resembles a LPF with zero phase shift in the frequency domain with a  $-3dB$  frequency of  $\sim 0.425f_s$ .

$$\langle X(s) \rangle_{T_s} = \left( \frac{e^{\frac{sT_s}{2}} - e^{-\frac{sT_s}{2}}}{sT_s} \right) X(s) \quad (25)$$

This provides an approximate frequency range of applicability of the averaged model. However, for frequencies greater than  $\sim 0.425f_s$ ,  $X(s)$  becomes attenuated and therefore the average model may not accurately predict these higher frequency dynamics.

Figure 2-8 compares the DC link voltage, DC current, and the capacitor current of the averaged model and the switching model. The DC link capacitor for this simulation is  $50,000 \mu\text{F}$ . Figure 2-9 compares the AC line-to-line voltage and AC line current of the inverter of the averaged model and the switching model. For the switching model, the line-to-ground output voltage switches between  $+V_{dc}$  and  $0 \text{ V}$  creating a DC offset. The DC offset is removed in the line-to-line voltage. The plots of the current show the current ripple in the switching model which is not present in the averaged model. These plots show the averaged model represents the fundamental component of the signals but does not represent the ripple caused by the switching of the power electronics.

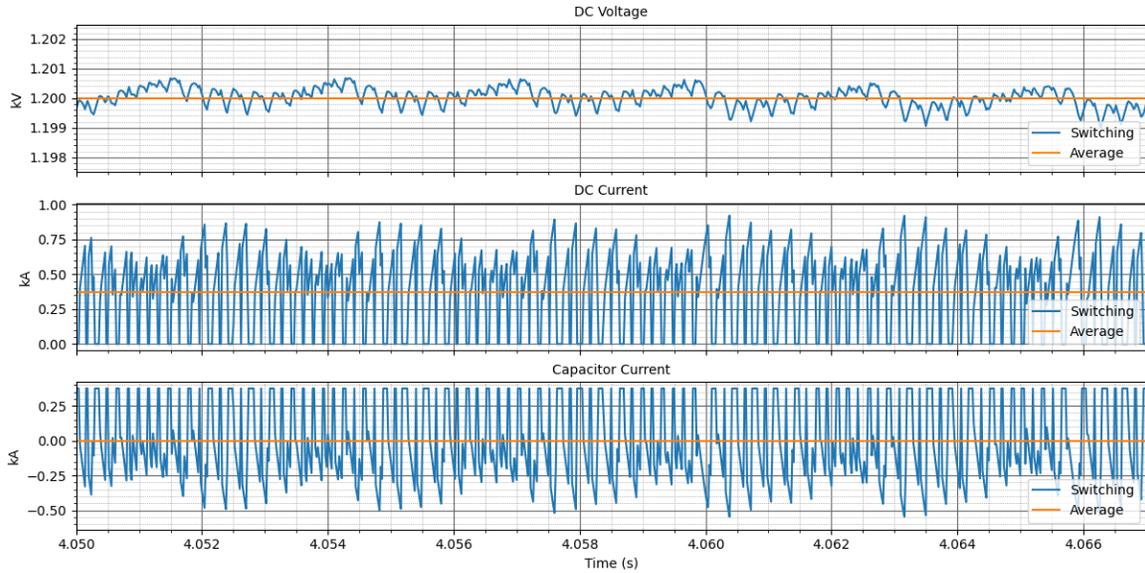


Figure 2-8. Comparison of the DC link voltage (top chart), inverter DC current (middle chart), and the capacitor current (bottom chart) in the switching model and the average model.

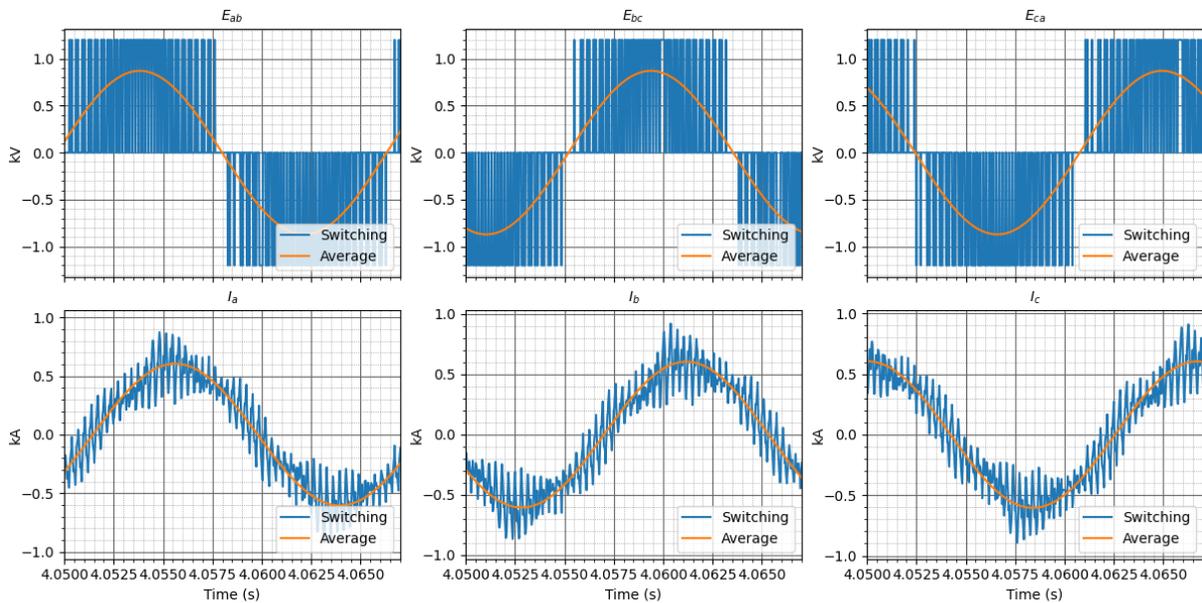


Figure 2-9. Comparison of the line-to-line voltage (top charts) and line currents (bottom charts) in the switching model and the average model.

The previous examples considered steady-state conditions where the magnitude and frequency of the space vector of the inverter terminal voltage were constant. Figure 2-10 compares the current response of the switching model and the averaged model for a three-phase fault at the high-side of

the inverter step-up transformer. The inverter control during normal and abnormal conditions will be presented in Chapter 3. However, this example is provided to show the model comparison under abnormal conditions.

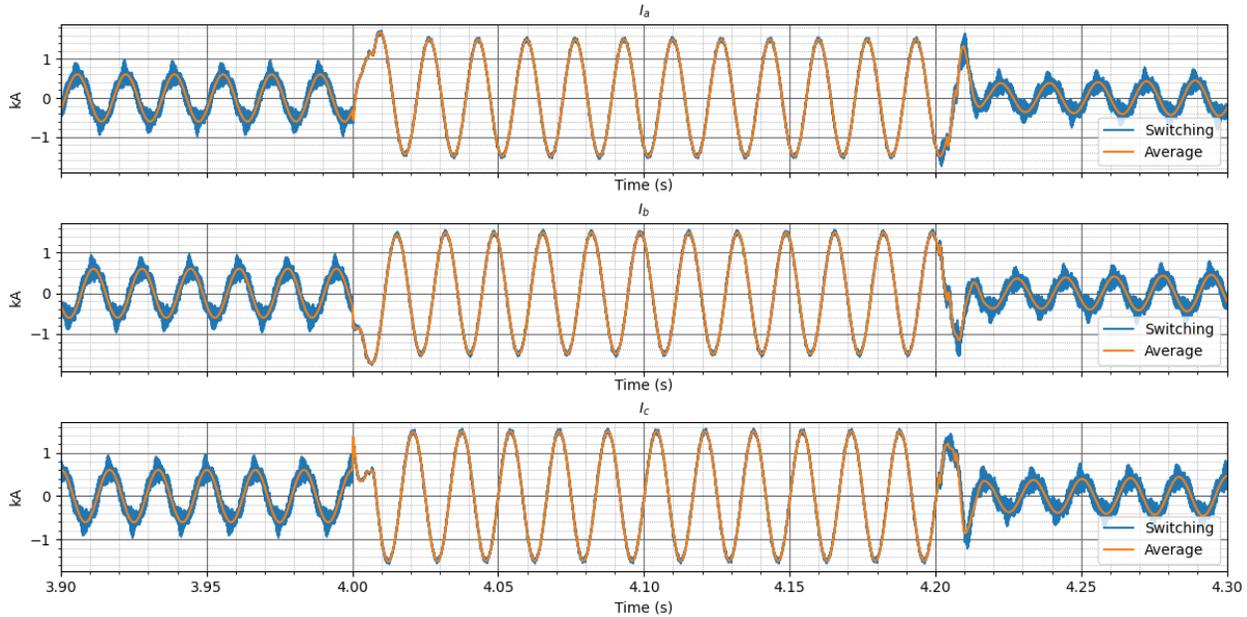


Figure 2-10. Comparison of the line currents in the switching model and the average model for a three-phase fault at the high-side of the inverter step-up transformer.

### 2.3. Output Filter

The output filter in this model is assumed to be an LCL filter as shown in Figure 2-1. In Section 2.2, one of the justifications for the use of the averaged model assumes the design includes an output filter of low-pass characteristic with the cutoff frequency less than the switching frequency [38]. The LCL filter is parameterized based on the design procedure in [39, 40]. A resistor,  $R_d$ , is added in series with the filter capacitor for passive damping. Care is taken to ensure the filter resonant frequency is lower than the switching frequency and higher than the current controller bandwidth. The corresponding parameters are shown in Table 2-I.

Table 2-I. LCL Filter Parametrization

Parameter	Value
Inverter rating	1.0 MVA
AC output voltage	600.0 V RMS line-line
Inverter step-up transformer impedance	6% on 1.0 MVA base ( $L_t = 0.0573$ mH)
$L_1$	0.1 mH
$L_2$	0.0 mH <sup>a</sup>
C	294 $\mu$ F
$R_d$	0.11 $\Omega$

<sup>a</sup> The inverter step-up transformer impedance is used as  $L_2$ .

Figure 2-11 shows the LCL filter as a two-port network to analyze the currents as a function of the filter impedance and external source. In Section 3.2, the inverter control is developed to regulate the output current by applying the appropriate voltage  $E$ .

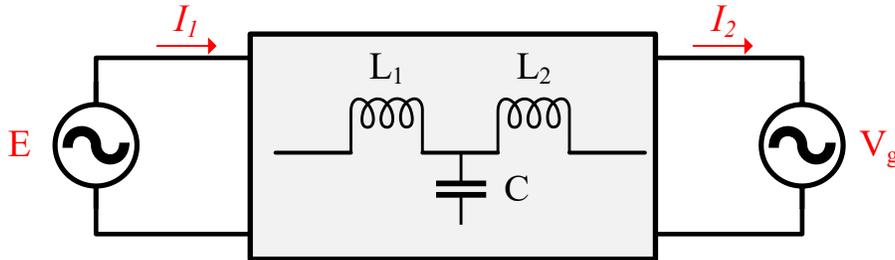


Figure 2-11. LCL filter represented by a two-port network.

The equations governing the current can be written in terms of superposition.

$$I_1 = Y_{11}E + Y_{12}V_g \quad (26)$$

$$I_2 = Y_{21}E + Y_{22}V_g \quad (27)$$

The admittances are calculated as:

$$\begin{aligned}
Y_{11} &= \left. \frac{I_1}{E} \right|_{V_g=0} = \frac{(s^2 L_2 C + 1)}{s^3 L_1 L_2 C + s(L_1 + L_2)} \\
Y_{12} &= \left. \frac{I_1}{V_g} \right|_{E=0} = \frac{-1}{s^3 L_1 L_2 C + s(L_1 + L_2)} \\
Y_{21} &= \left. \frac{I_2}{E} \right|_{V_g=0} = \frac{1}{s^3 L_1 L_2 C + s(L_1 + L_2)} \\
Y_{22} &= \left. \frac{I_2}{V_g} \right|_{E=0} = \frac{-1(s^2 L_1 C + 1)}{s^3 L_1 L_2 C + s(L_1 + L_2)}
\end{aligned} \tag{28}$$

resulting in

$$I_1 = \frac{(s^2 L_2 C + 1)}{s^3 L_1 L_2 C + s(L_1 + L_2)} E + \frac{-1}{s^3 L_1 L_2 C + s(L_1 + L_2)} V_g \tag{29}$$

$$I_2 = \frac{1}{s^3 L_1 L_2 C + s(L_1 + L_2)} E + \frac{-1(s^2 L_1 C + 1)}{s^3 L_1 L_2 C + s(L_1 + L_2)} V_g \tag{30}$$

The admittance  $Y_{21}$  represents the transfer function from the inverter voltage  $E$  to the grid current  $I_2$  if the grid voltage is shorted. This transfer function is of particular interest because the inverter voltage  $E$  is used to control the output current as detailed in Section 3.2. Figure 2-12 compares the admittance  $Y_{21}$  and the admittance without the capacitance. The parameters of the LCL filter are given in Table 2-I. If the range of frequencies considered in the frequency response is limited to  $1/10^{\text{th}}$  of the switching frequency, the frequency response is the same with and without the filter capacitor. The closed-loop bandwidth of the current control is set to be less than  $1/10^{\text{th}}$  of the switching frequency. This result allows for approximating the LCL filter by an L filter in the control design in the next chapter.

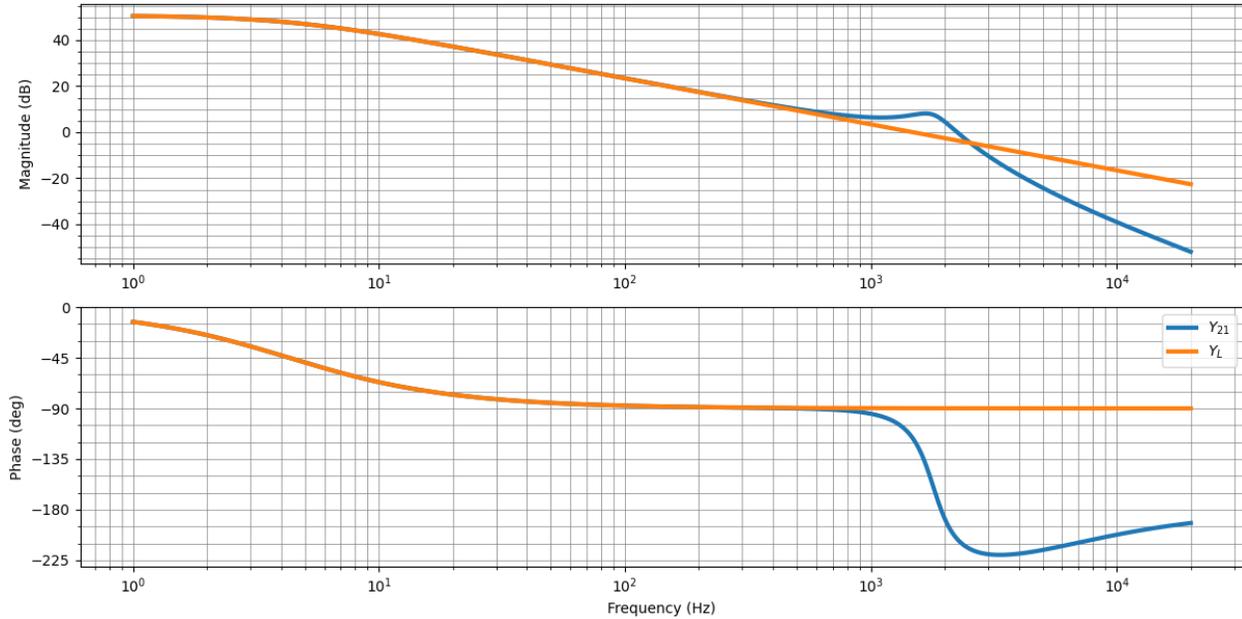


Figure 2-12. Comparison of the admittance  $Y_{21}$  (blue trace) and the admittance of an L filter (orange trace).

## 2.4. Summary

This chapter provides an overview of the inverter modeling. The switching model of a two-level sinusoidal PWM controlled inverter is first presented. The switching model is then simplified to an averaged model of the inverter which is used in the control design in Chapter 3. The assumptions made to develop the averaged model are detailed such that the limitations are considered in the use of the model prototype. It is shown mathematically that the averaging operator used for the average model development results in a low pass characteristic with a cut-off frequency of approximately  $0.425f_s$ . Lastly, the output LCL filter implemented in the model is presented. It is shown from frequency domain analysis that the LCL filter can be approximated by an L filter for frequencies less than the resonant frequency. This is leveraged in Chapter 3 to develop the control law of the inverter. The EMT model prototype includes the LCL filter and both a switching model and averaged model representation of the inverter.

### **3. Inverter Control**

This chapter presents the control of a PV inverter typically applied in large, utility-scale plants connected to the transmission system. The control implementation in the model prototype is modular such that it can be readily extended to other full converter technologies. The control is developed based on the performance requirements in draft 6.1 of IEEE P2800 [25], NERC Reliability Guidelines [13] and international grid codes such as the German (VDE) [26, 27] and Spanish (NTS) [28] applications of the European Grid Code [29]. These grid codes, guidelines, and standards are performance-based, not control design standards. Therefore, they are used to define the control objective of the inverter for different conditions. The remaining sections in this chapter provide an overview of the inverter control architecture followed by a detailed description of each controller. This includes the model of each process to be controlled, the control implementation in the model prototype, an analytical tuning procedure of each controller, and verification of the controller response.

#### **3.1. IBR Plant Control Overview**

Figure 3-1 shows an example single line diagram of a PV plant connected to the transmission system. Large PV plants (e.g., > 100 MW) may consist of tens to hundreds of central PV inverters or hundreds to thousands of string inverters. A plant-level controller is typically applied in large plants to coordinate the response of the individual inverters. The plant-level controller monitors

the voltage and current at the point of measurement (POM<sup>2</sup>) or the low voltage side of the station main transformer and provides the active power and reactive power or voltage setpoint references to the individual inverters in the plant. The bandwidth of the plant-level control is much lower than the inverter-level control. A common control strategy is for the inverters to follow the reference setpoints provided by the plant-controller in normal operation and to take autonomous control when the AC terminal voltage is outside the inverter's continuous operating range (e.g., LVRT) to provide fast grid support. This is the approach followed in this work.

The inverter-level control in Figure 3-2 processes the reference setpoints from the plant-level control to synthesize a sinusoidal output voltage for which the magnitude and phase are controlled. The control structure cascades an outer loop to an inner loop current controller. This structure is applied to facilitate tight control of the inverter AC output current to protect the power electronic devices and to improve the rejection of disturbances, e.g., the inverter terminal voltage. The fast current regulation effectively controls the voltage-sourced inverter to respond like a current source for dynamics slower than the current controller bandwidth. This is referred to as current mode control in the power electronics literature. An alternative control approach is voltage mode control. Appendix B provides a brief overview of this approach.

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<sup>2</sup> The Point of Measurement is defined in IEEE P2800 D6.1 as “a point between the high voltage bus of the IBR and the interconnection system.” In many cases, it is the high-voltage terminal of the main transformer in the plant.

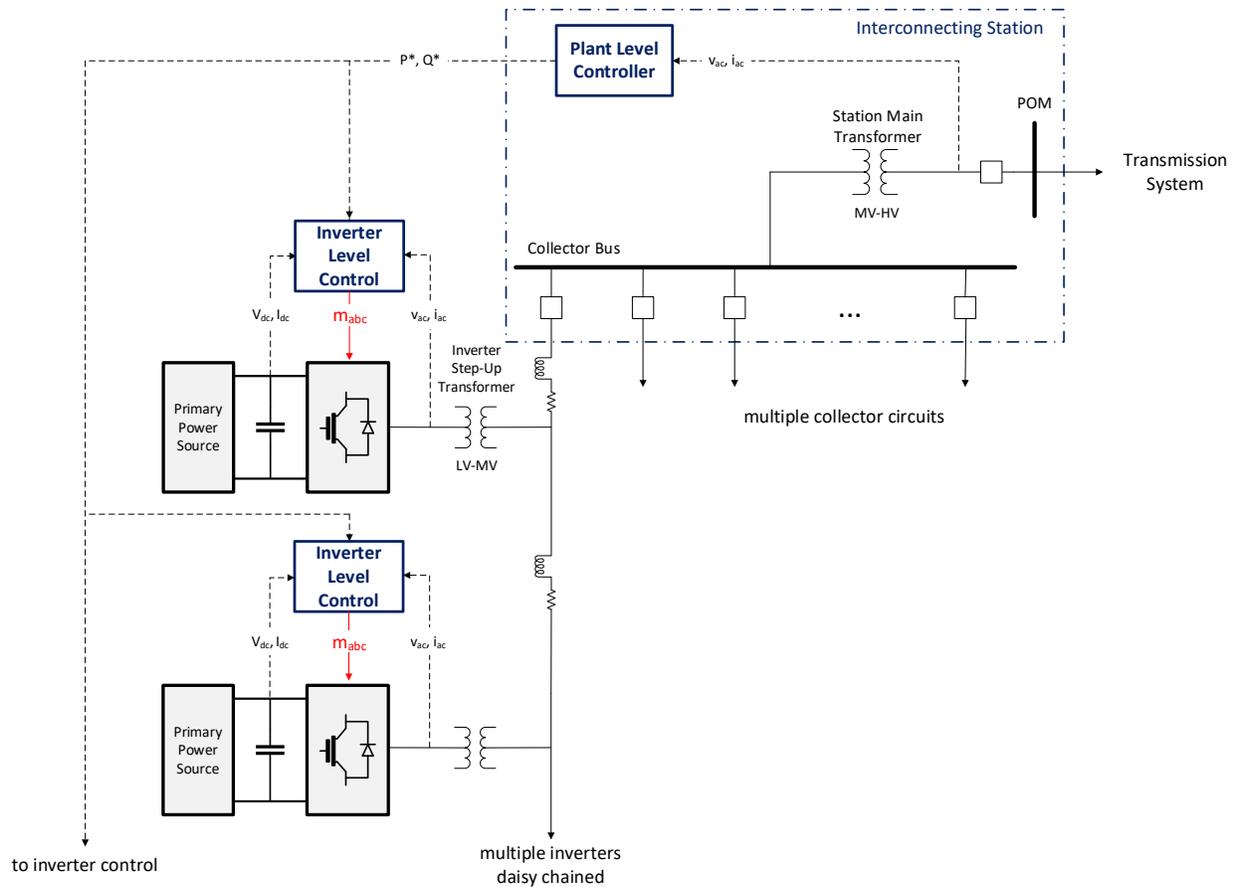


Figure 3-1: Single line diagram of a typical IBR plant design.

In current mode control, the outer loop control determines the current reference setpoints based on the specific control objective, e.g., controlling the DC link voltage. A common approach is to separate the bandwidths of the outer and inner loop controllers by an order of magnitude to decouple the control loops [31, 41]. The inverter control is implemented in a synchronously rotating reference frame, SRF, with the d-axis aligned to the space vector of the inverter AC terminal voltage. Controlling the inverter in the SRF provides many advantages. Balanced and undistorted three-phase sinusoidal signals are DC signals in the SRF established based on the fundamental frequency. This simplifies the compensator design. Proportional plus integral (PI) controllers are extensively used in this chapter given they are the most widely used controller industry [42, 43]. The alignment of the d-axis of the SRF to the space vector of the grid voltage

helps decouple the d-axis and q-axis control loops. In Section 3.5, it is shown that this structure allows the active power to be controlled by the d-axis current and the reactive power to be controlled by the q-axis current. However, the transformation of the signals to the SRF relies on the knowledge of the instantaneous phase angle of the grid voltage. This is discussed in Section 3.3. Control in the SRF can also result in dynamics close to the fundamental frequency and into the subsynchronous range that manifest in the transformation of SRF signals to the ABC reference frame [44, 45].

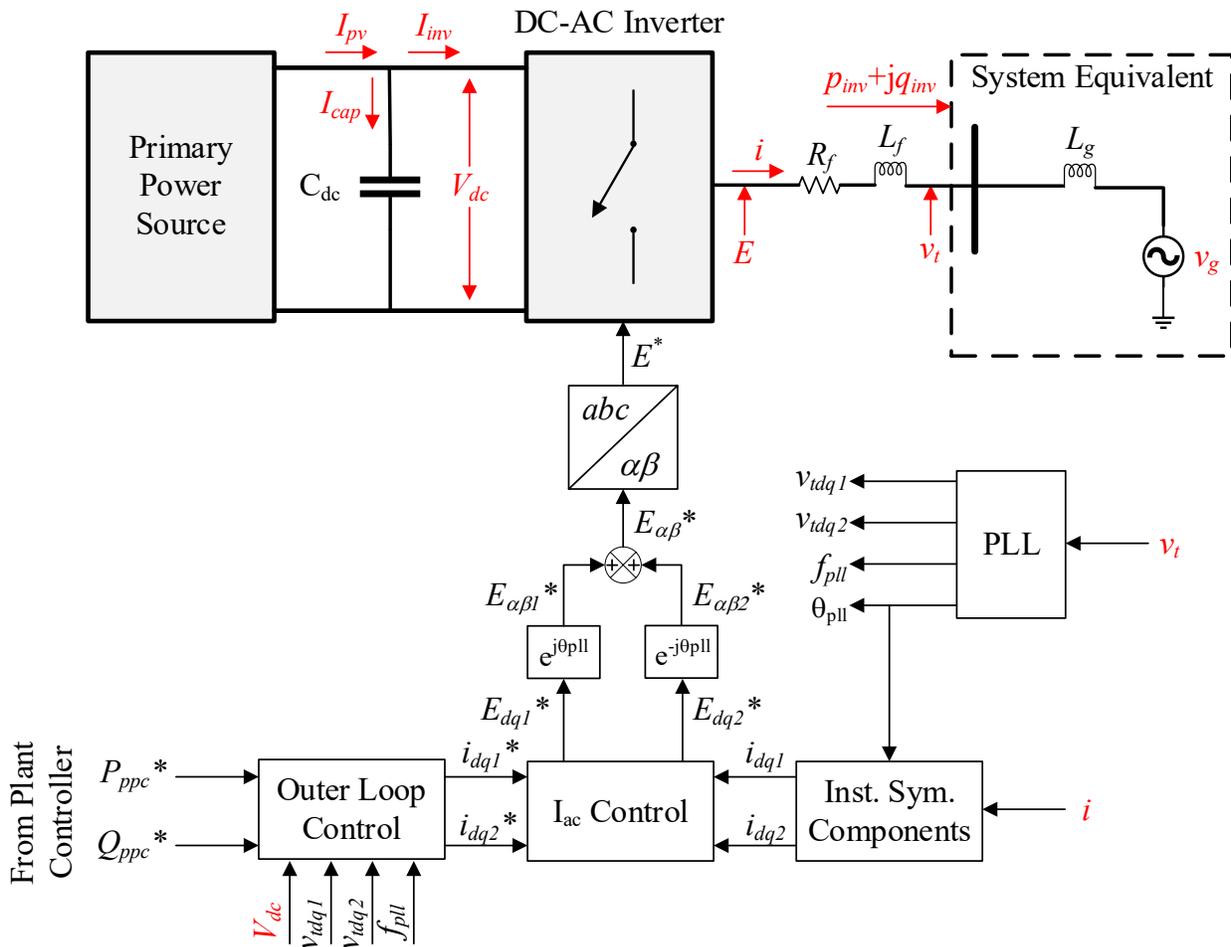


Figure 3-2: Inverter cascade control structure.

## 3.2. Current Controller

Presently, conventional control of inverters connected to the grid regulates the AC output current with an inner current control loop [46, 47]. The capability to control the current's positive and negative sequence components is present in some commercial inverters, e.g., to allow suppression of the negative sequence current for unbalanced terminal voltage. Based on evolving grid codes requiring negative sequence current injection, this capability is expected to become standard. Thus, the current controller in the model prototype regulates both positive and negative sequence current components. The system from the AC terminal of the inverter to the inverter step-up transformer is assumed to be a three-wire system. Therefore, there is no component of current in the zero sequence. For control in the SRF, a positive SRF and a negative SRF are applied as proposed in [48]. These reference frames are defined based on the PLL and described further in Section 3.3. This section develops the model of the output current, details the current controller design, and the tuning of the compensator used in the model prototype.

### 3.2.1. Model of the Current Dynamics

The dynamics of the inverter output AC current in Figure 3-2 can be written based on KVL in terms of the space vectors of the voltages and currents.

$$\mathbf{E} = R_f \mathbf{i} + L_f \frac{d}{dt} \mathbf{i} + \mathbf{V}_t \quad (31)$$

The space vectors are decomposed into their positive and negative sequence components based on superposition. The positive sequence components are transformed to the positive SRF via the Park transform. The resulting equations describe the dynamics of the d1-axis and q1-axis currents.

$$E_{d1} = R_f i_{d1} + L_f \frac{di_{d1}}{dt} - L_f \frac{d\theta_{PLL}}{dt} i_{q1} + V_{td1} \quad (32)$$

$$E_{q1} = R_f i_{q1} + L_f \frac{di_{q1}}{dt} + L_f \frac{d\theta_{PLL}}{dt} i_{d1} + V_{tq1} \quad (33)$$

Similarly, transforming the negative sequence components of (31) to the negative sequence SRF gives the dynamic equations for the negative sequence d2-axis and q2-axis currents. Appendix D provides a derivation of (32) – (35).

$$E_{d2} = R_f i_{d2} + L_f \frac{di_{d2}}{dt} + L_f \frac{d\theta_{PLL}}{dt} i_{q2} + V_{td2} \quad (34)$$

$$E_{q2} = R_f i_{q2} + L_f \frac{di_{q2}}{dt} - L_f \frac{d\theta_{PLL}}{dt} i_{d2} + V_{tq2} \quad (35)$$

Re-writing (32) – (35) in state-space form, i.e.,  $\dot{x} = f(x, u, \epsilon)$ :

$$\frac{di_{d1}}{dt} = \frac{1}{L_f} (-R_f i_{d1} + \omega_{PLL} L_f i_{q1} + E_{d1} - V_{td1}) \quad (36)$$

$$\frac{di_{q1}}{dt} = \frac{1}{L_f} (-R_f i_{q1} - \omega_{PLL} L_f i_{d1} + E_{q1} - V_{tq1}) \quad (37)$$

$$\frac{di_{d2}}{dt} = \frac{1}{L_f} (-R_f i_{d2} - \omega_{PLL} L_f i_{q2} + E_{d2} - V_{td2}) \quad (38)$$

$$\frac{di_{q2}}{dt} = \frac{1}{L_f} (-R_f i_{q2} + \omega_{PLL} L_f i_{d2} + E_{q2} - V_{tq2}) \quad (39)$$

$$\frac{d\theta_{PLL}}{dt} = \omega_{PLL} \quad (40)$$

The state variables are the inductor currents and the output of the PLL. Neglecting the state variable associated with the PLL, which is discussed in Section 3.3, Figure 3-3 shows a diagram of the current dynamics.

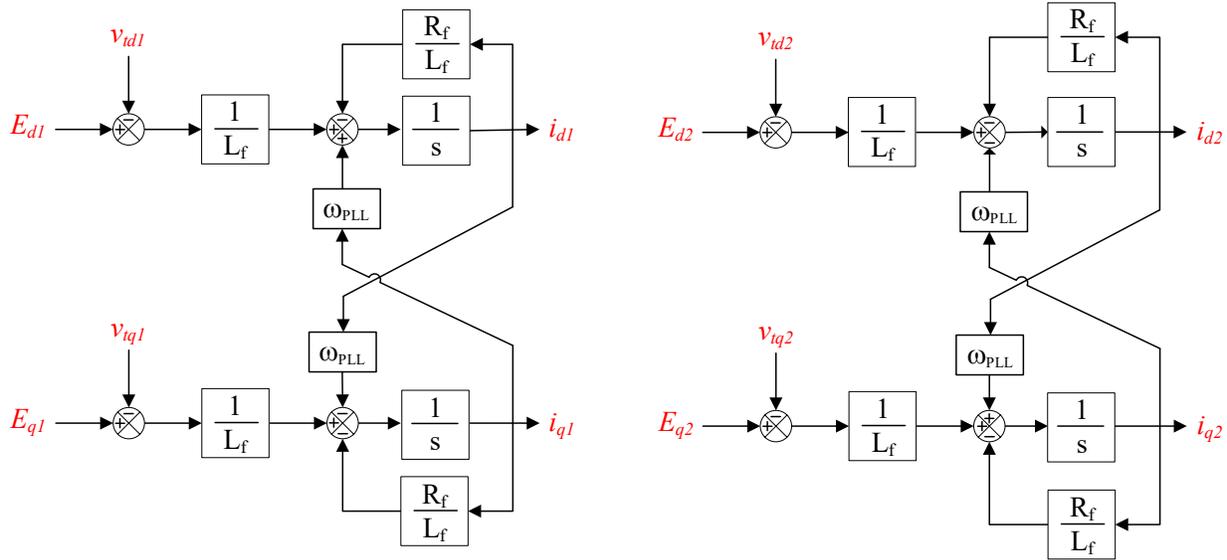


Figure 3-3. Model of the current dynamics in the positive and negative SRFs.

### 3.2.2. Current Controller

From Figure 3-3 and (36) – (39), it is evident the inverter output current components can be controlled by the corresponding components of the inverter voltage,  $\mathbf{E}$ . Coupling between the d-axis and q-axis components of the current dynamics in both the positive and negative sequences result due to the reference frame transformation. The cross-coupling terms between the d-axis and q-axis controllers, as well as the grid voltage,  $\mathbf{V}_t$ , can be considered disturbances. Feedforward of the measured terminal voltage is applied to improve disturbance rejection, and feedforward of the measured current is applied to negate the cross-coupling [31, 49, 50]. The compensator generating the inverter voltage reference  $\mathbf{E}^*$  consists of a PI controller acting on the error between the current reference and the measured current in addition to the feedforward terms. Figure 3-4 shows the

current controllers for the positive and negative SRFs. Note that the feedforward signals must be measured which may influence the dynamics.

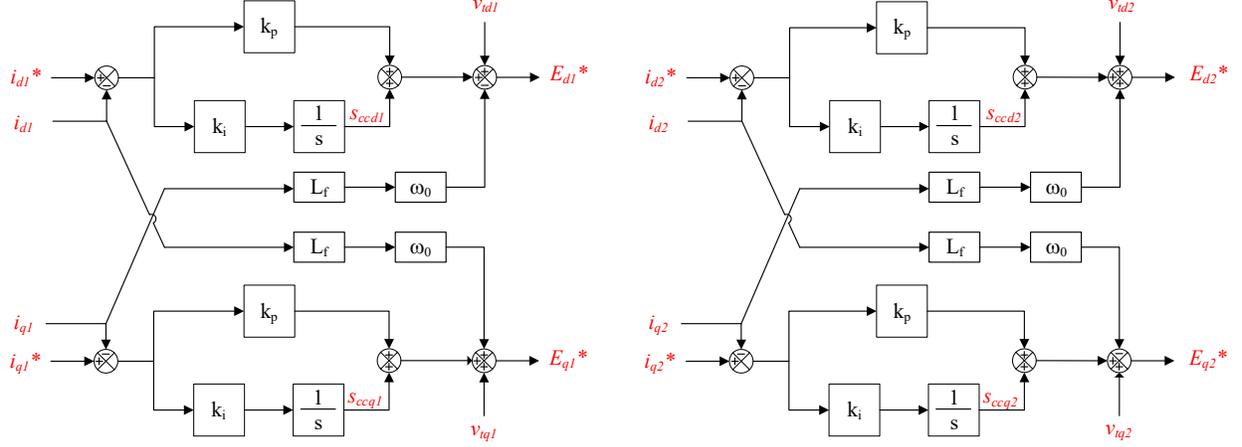


Figure 3-4. Control diagram of the current controllers in the positive and negative SRFs.

From Figure 3-4, the voltage references  $E^*$  are given by:

$$E_{d1}^* = (i_{d1}^* - i_{d1})k_p + s_{ccd1} + v_{td1} - L_f\omega_0 i_{q1} \quad (41)$$

$$\frac{ds_{ccd1}}{dt} = (i_{d1}^* - i_{d1})k_i \quad (42)$$

$$E_{q1}^* = (i_{q1}^* - i_{q1})k_p + s_{ccq1} + v_{tq1} + L_f\omega_0 i_{d1} \quad (43)$$

$$\frac{ds_{ccq1}}{dt} = (i_{q1}^* - i_{q1})k_i \quad (44)$$

$$E_{d2}^* = (i_{d2}^* - i_{d2})k_p + s_{ccd2} + v_{td2} + L_f\omega_0 i_{q2} \quad (45)$$

$$\frac{ds_{ccd2}}{dt} = (i_{d2}^* - i_{d2})k_i \quad (46)$$

$$E_{q2}^* = (i_{q2}^* - i_{q2})k_p + s_{ccq2} + v_{tq2} - L_f\omega_0 i_{d2} \quad (47)$$

$$\frac{ds_{ccq2}}{dt} = (i_{q2}^* - i_{q2})k_i \quad (48)$$

The current dynamics are now written including the PI controller and feedforward terms. It is assumed that the PLL frequency is the same as the nominal system frequency, i.e.,  $\omega_{PLL} = \omega_0$ , and it is assumed the inverter voltage is equal to the reference,  $\mathbf{E} = \mathbf{E}^*$ .

$$\frac{di_{d1}}{dt} = \frac{1}{L_f} (-R_f i_{d1} + (i_{d1}^* - i_{d1})k_p + s_{ccd1}) \quad (49)$$

$$\frac{di_{q1}}{dt} = \frac{1}{L_f} (-R_f i_{q1} + (i_{q1}^* - i_{q1})k_p + s_{ccq1}) \quad (50)$$

$$\frac{di_{d2}}{dt} = \frac{1}{L_f} (-R_f i_{d2} + (i_{d2}^* - i_{d2})k_p + s_{ccd2}) \quad (51)$$

$$\frac{di_{q2}}{dt} = \frac{1}{L_f} (-R_f i_{q2} + (i_{q2}^* - i_{q2})k_p + s_{ccq2}) \quad (52)$$

The dynamics of the four components of the current all have the same form and are independent based on the assumption of perfect canceling of the cross-coupling terms. Therefore, the transfer function given in (53) can be used to determine the gains for the four current controllers.

$$\frac{i(s)}{i^*(s)} = \frac{k_p s + k_i}{L_f (s^2 + \frac{(k_p + R_f)}{L_f} s + \frac{k_i}{L_f})} \quad (53)$$

The assumption of perfect cancelation is shown in Section 3.2.3 to not be completely accurate.

The output of the current control is the inverter reference voltage,  $\mathbf{E}^*$ . This consists of a superposition of the positive sequence and negative sequence component in each phase. The

inverter reference voltage is then multiplied by the inverse of the inverter gain to create the modulation signal. The block diagram is shown in Figure 3-5.

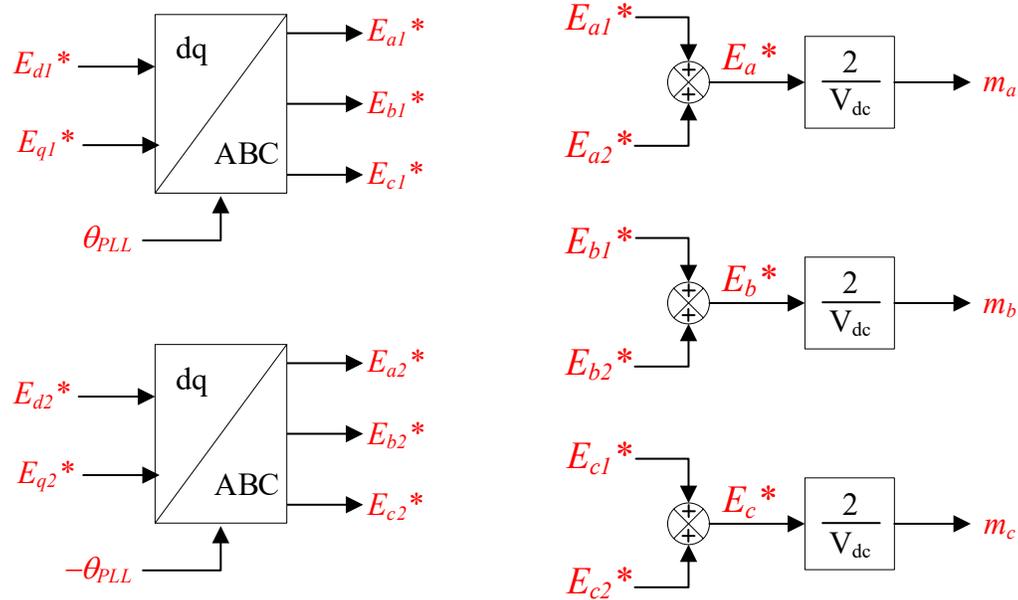


Figure 3-5. Block diagram of the development of the modulating signal for PWM.

### 3.2.3. Current Controller Gains

Various tuning approaches can be used to shape the desired time-domain response of the inverter output current. This section uses pole placement to tune the PI gains analytically based on the derived process model. Noting this is a 2<sup>nd</sup> order system and the output filter inductance and resistance is known, the PI gains can be set based on the target rise time and damping [51]. An estimate of the rise time of a second-order system is given by:

$$t_r \cong \frac{1.8}{\omega_n} \quad (54)$$

Equating the terms of the characteristic equation of the second-order system provides the proportional and integral gains:

$$k_p = 2\zeta\omega_n L_f - R_f \quad (55)$$

$$k_i = L_f\omega_n^2 \quad (56)$$

In [52], testing of three utility-scale converters showed that the closed-loop bandwidth of the current controller is on the order of 100 Hz to 2 kHz. The closed-loop bandwidth of the current controller is set to be less than or equal to 1/10 of the switching frequency ( $f_s = 3060\text{Hz}$ ) in the model prototype. Table 3-I provides the current controller PI gains for three desired rise times based on the output filter inductance and resistance.

Table 3-I: Current Controller PI Gains

Parameter	Value	Value	Value
$t_r$ (target)	1ms	2ms	3ms
$f_{BW} \sim 0.35/t_r$	350Hz	175Hz	116.7Hz
Damping ratio $\zeta$	0.9	0.9	0.9
$R_f$	0.75m $\Omega$	0.75m $\Omega$	0.75m $\Omega$
$L_f$	0.1mH	0.1mH	0.1mH
$k_p$	0.323	0.16125	0.10725
$k_i$	324.0	81.0	36.0

The analytically calculated PI gains of the current controllers are based on estimates of the relationship between the rise time and the undamped natural frequency of a second-order system. The transfer function of the closed-loop current control in (53) is not in the standard form of a second-order system assumed in these previous estimates. Figure 3-6 shows the influence of the zero in (53) on the step response. Comparing the step response of (53) with the standard second-

order form, the rise time decreases, and the overshoot increases. The green trace shows the deviation from the response of the standard form of a second-order system is dependent on the proportional gain and filter inductance based on the analytical tuning method used. For example, Figure 3-7 shows that as the desired damping ratio is increased (resulting in the increase in the calculated proportional gain), the rise time decreases, and the overshoot increases. This effect should be considered when using (55) and (56) to analytically calculate the PI controller gains to ensure the rise time is in the desired range.

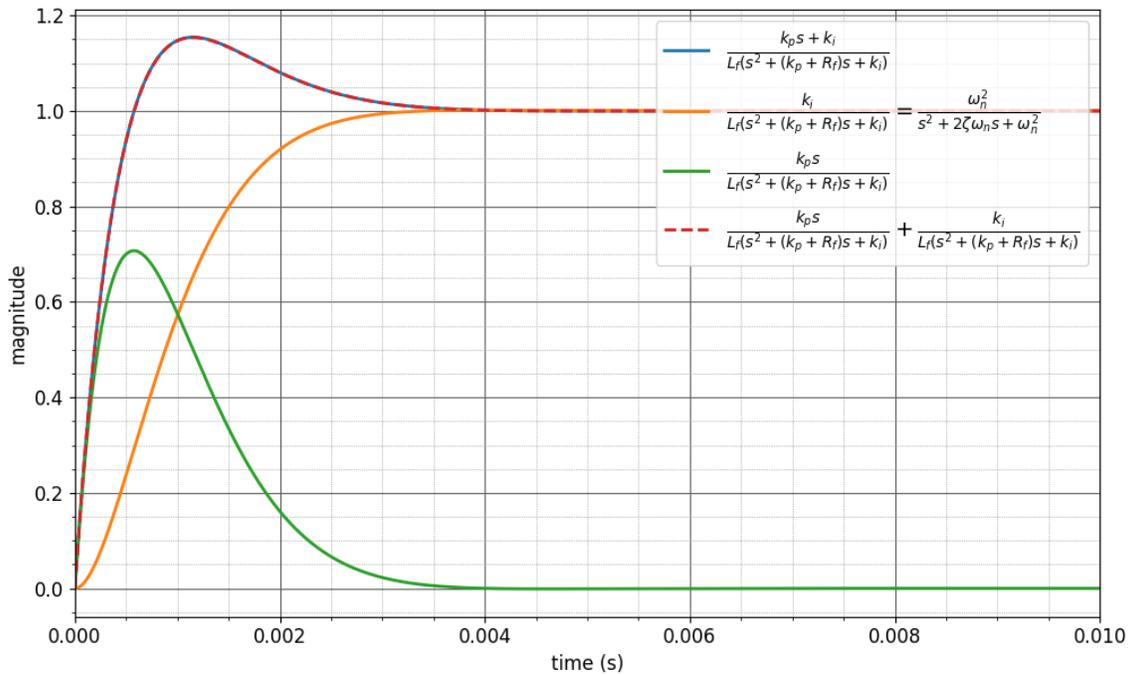


Figure 3-6. Step response of the current controller (blue trace), standard 2<sup>nd</sup> order form (orange trace), difference between the current controller and standard form (green trace), and the summation of the two components of the current response (dashed red trace).

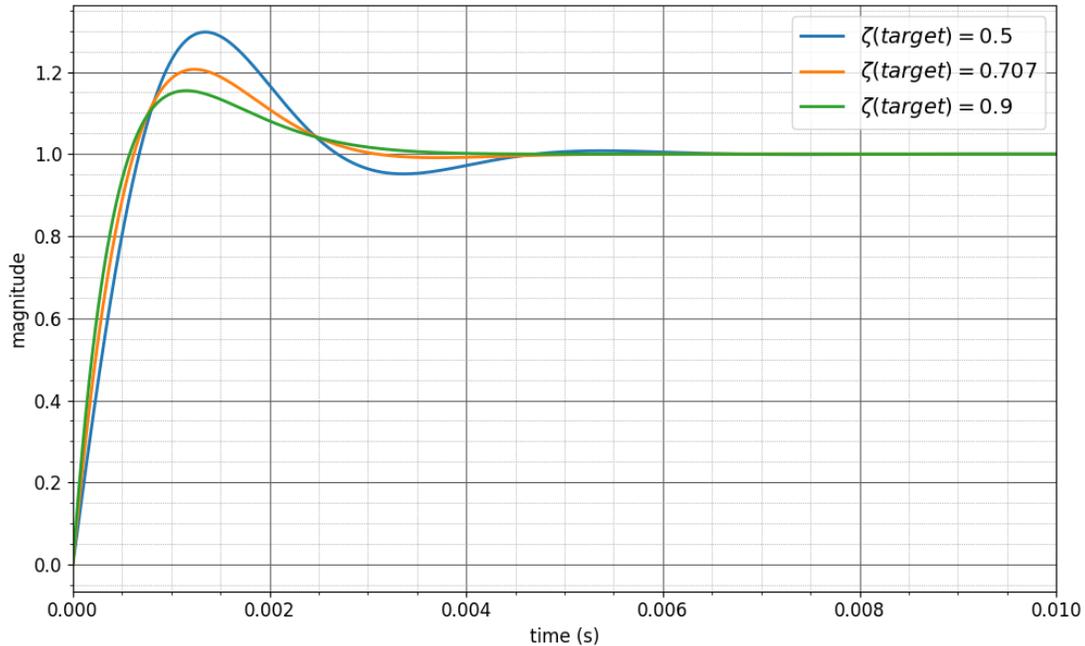


Figure 3-7. Step response of the current controller varying the desired damping ratio.  $\zeta = 0.5$  (blue trace),  $\zeta = 0.707$  (orange trace), and  $\zeta = 0.9$  (green trace).

Lastly, the response of the current controller is tested in the full model prototype in PSCAD™. The current references from the outer loop are held constant, and at  $t = 3\text{s}$  a negative 0.05pu step change in the positive SRF q1-axis current reference is applied. The outer loop controllers detailed in Section 3.5 were disabled, and the d1-axis current reference was set to 0.9pu. The three sets of PI gains shown in Table 3-I are considered. The step response in the full model shows the same characteristics as the current response observed in the previous section. The response is faster than the target rise times used in the analytical calculations of the gains. The previous section showed this might be due to the zero. If this is significant, setpoint weighting can be applied to the proportional gain. The response of the full model also shows the coupling between the two controllers where a step change in  $i_{q1}$  results in a change in  $i_{d1}$ . The change in  $i_{d1}$  is on the order of 10% of the step change magnitude in  $i_{q1}$ . Overall, the response meets the time-domain requirements and can be further tuned if necessary.

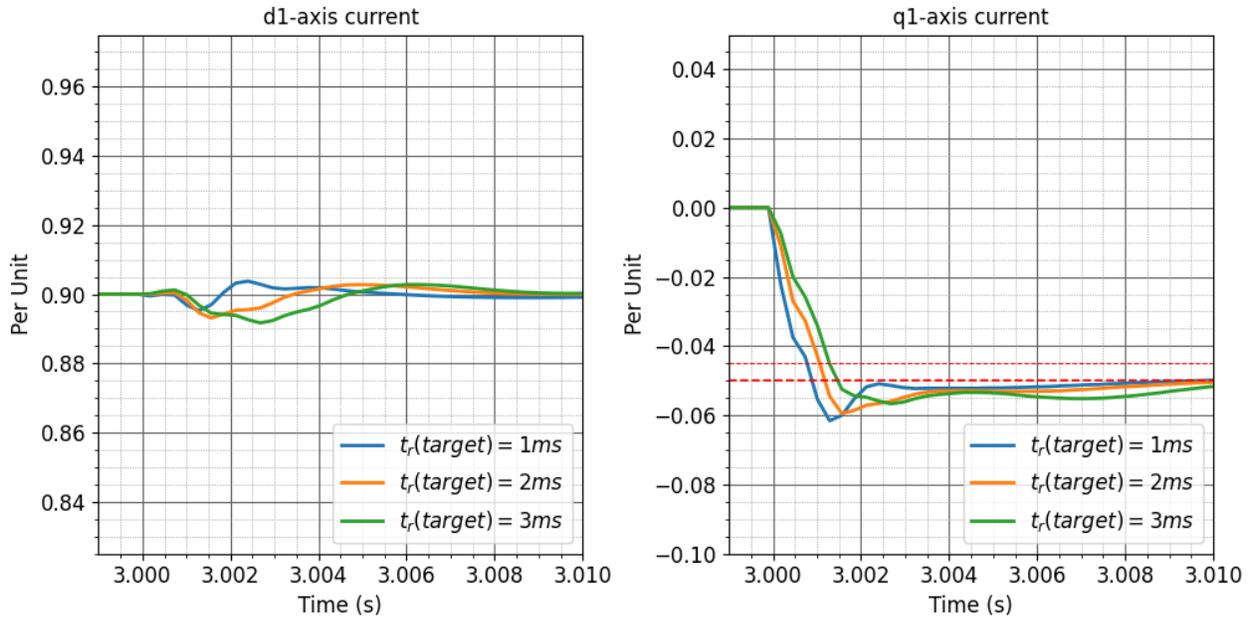


Figure 3-8. Step response of the d1-axis current (left) and the q1-axis current (right) for a step change in the q1-axis current reference for three sets of PI gains.

### 3.3. Synchronization to the Grid Voltage

A critical component of the current mode-controlled inverter is detecting the grid voltage's positive sequence fundamental frequency component. As discussed in Section 3.2, the inverter synthesizes a voltage  $\mathbf{E}$  to generate the desired current through the output filter based on (31). The reference frame transformation to the SRF of the measured AC voltages and currents is based on the estimate of the instantaneous value of the angle of the positive sequence fundamental frequency component of the grid voltage. Therefore, control in the SRF is influenced by the ability of the controller to detect the grid angle for the reference frame transformation. This section discusses the fundamentals of the phase-locked loop (PLL), the structure of the SRF-PLL, tuning of the SRF-PLL, and derivatives of the SRF-PLL applied in the model prototype.

### 3.3.1. PLL

It is common to use a PLL algorithm to synchronize the inverter control to the grid voltage [53]. The control objective of the PLL is to track the phase angle of the input signal. The principal components of a PLL are the phase detector (PD), the loop filter (LF), and the voltage-controlled oscillator (VCO) shown in Figure 3-9 [54].

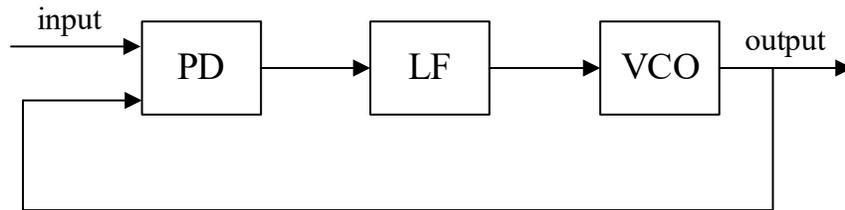


Figure 3-9: Basic PLL control structure adapted from [54].

### 3.3.2. SRF-PLL

The SRF-PLL shown in Figure 3-10 is a common PLL structure for three-phase inverters [55]. The control strategy of the SRF-PLL is to align the d-axis of the SRF to the space vector of the grid voltage. This is achieved by regulating the q-axis component of the grid voltage to zero.

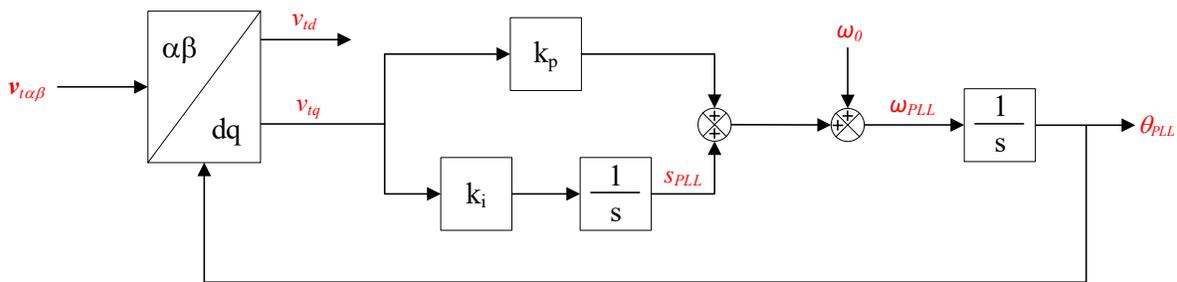


Figure 3-10. SRF-PLL.

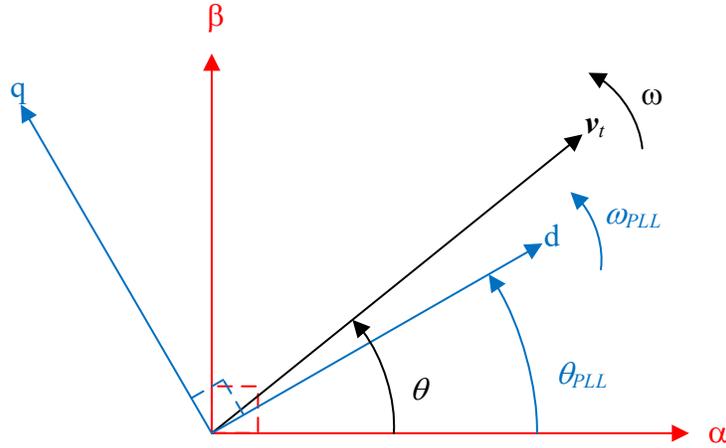


Figure 3-11 SRF coordinates in the  $\alpha\beta$  plane.

The space vector of the grid voltage in Figure 3-11 is defined as:

$$\mathbf{v}_t = |\mathbf{v}_t|e^{j\theta(t)} = v_{t\alpha}(t) + jv_{t\beta}(t) \quad (57)$$

where:

$$\theta(t) = \omega t + \theta_0 \quad (58)$$

From Figure 3-11, the d-axis and q-axis components of the voltage can be inferred graphically.

$$v_{td} = |\mathbf{v}_t|[\cos(\theta - \theta_{PLL})] \quad (59)$$

$$v_{tq} = |\mathbf{v}_t|[\sin(\theta - \theta_{PLL})] \quad (60)$$

Based on (59) and (60), controlling  $v_{tq}$  to zero results in the d-axis aligning with  $\mathbf{v}_t$  and therefore  $\theta_{PLL} = \theta$ . In Figure 3-10, the  $\alpha\beta$  to dq transformation is the phase detector of the SRF-PLL. The q-axis component of the grid voltage is the error signal input to the loop filter, implemented via a PI controller. If the difference between  $\theta$  and  $\theta_{PLL}$  is constant with respect to time, the angular frequency calculated by the PLL,  $\omega_{PLL}$ , is the angular frequency of the grid,  $\omega$ ,

and the PLL is said to be “locked”. Furthermore, if the magnitude of the space vector of the grid voltage is constant and the difference between  $\theta$  and  $\theta_{PLL}$  is constant with respect to time, the dq components of the voltage are DC signals. This result is one of the advantages of implementing the inverter control in the SRF. If the grid voltage is unbalanced or distorted, the magnitude of the space vector of the grid voltage will not be constant, and the SRF components will contain sinusoidal terms.

### 3.3.3. Model of the SRF-PLL Dynamics

Figure 3-10 and (60) show the SRF-PLL contains nonlinearities such as sinusoidal terms. Other nonlinearities such as amplitude limiters and anti-windup of the integral control are not shown in Figure 3-10. A linearized model of the SRF-PLL is developed to apply linear control and system analysis techniques to investigate the dynamics of the SRF-PLL. The state-space model of the SRF-PLL in Figure 3-10 is written as:

$$\frac{d\theta_{PLL}}{dt} = \omega_{PLL} = \omega_0 + v_{tq}k_p + s_{PLL} \quad (61)$$

$$\frac{ds_{PLL}}{dt} = v_{tq}k_i \quad (62)$$

The linearized model is determined by small-signal analysis. For reference, the procedure used is outlined in Appendix C.

$$\begin{aligned} \Delta\dot{\theta}_{PLL} &= \Delta\omega_{PLL} \\ &= |v_{t0}|[\cos(\theta_0 - \theta_{PLL0})\Delta\theta - \cos(\theta_0 - \theta_{PLL0})\Delta\theta_{PLL}]k_p \\ &\quad + \Delta s_{PLL} = |v_{t0}|(\Delta\theta - \Delta\theta_{PLL})k_p + \Delta s_{PLL} \end{aligned} \quad (63)$$

$$\begin{aligned}\Delta \dot{S}_{PLL} &= |v_{t0}| [\cos(\theta_0 - \theta_{PLL0}) \Delta \theta - \cos(\theta_0 - \theta_{PLL0}) \Delta \theta_{PLL}] k_i \\ &= |v_{t0}| (\Delta \theta - \Delta \theta_{PLL}) k_i\end{aligned}\quad (64)$$

The subscript ‘0’ denotes the steady-state value upon which the system is linearized. Figure 3-12 shows the block diagram of the linearized model around a steady state-operating point of  $|V_{t0}| = 1.0pu$  and  $\theta_{PLL0} = \theta_0$ .

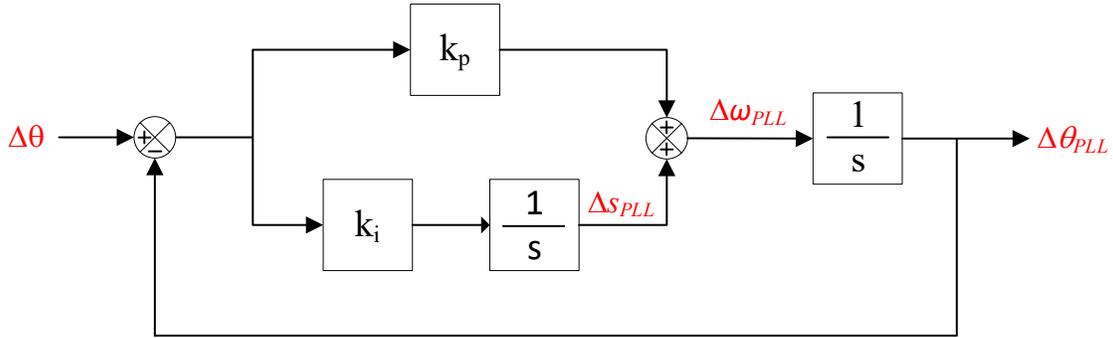


Figure 3-12. Linearized model of the SRF-PLL

The Laplace transform of (63) and (64) provides the closed-loop transfer function of the linearized model in Figure 3-12.

$$\frac{\theta_{PLL}(s)}{\theta(s)} = \frac{k_p s + k_i}{s^2 + k_p s + k_i} \quad (65)$$

### 3.3.4. SRF-PLL Controller Gains

Pole placement is used to tune the SRF-PLL PI controller analytically. Given (65) is a second-order system, the poles are placed according to the desired rise time and damping of the SRF-PLL.

The PI gains are calculated as:

$$t_r \cong \frac{1.8}{\omega_n} \quad (66)$$

$$2\zeta\omega_n = k_p \quad (67)$$

$$\omega_n^2 = k_i \quad (68)$$

High bandwidth PLLs have been shown to cause instability in weaker grids [56]. The bandwidth of the SRF-PLL is set much lower than the bandwidth of the current controllers. A few example gain calculations are provided in Table 3-II for reference.

Table 3-II: SRF-PLL Controller PI Gains

Parameter	Value	Value	Value
$t_r$ (target)	50 ms	100 ms	150 ms
$f_{BW} \sim 0.35/t_r$	7 Hz	3.5 Hz	2.33 Hz
Damping ratio $\zeta$	0.707	0.707	0.707
$k_p$	50.9	25.4	17.0
$k_i$	1296.0	324.0	144.0

Figure 3-13 shows the step response of the linearized model for the gains in Table 3-II. The step response time is decreased compared to the target value. This is again due to the zero in the transfer function as discussed in Section 3.2.3.

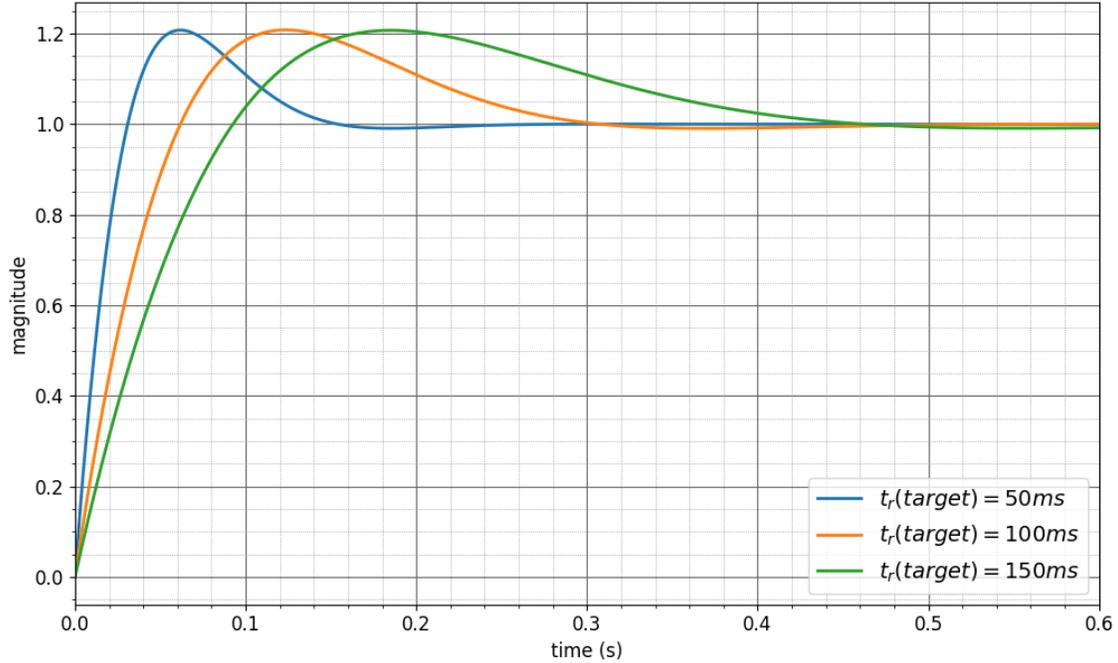


Figure 3-13. Step-response of the linearized SRF-PLL.

The SRF-PLL in Figure 3-10 is implemented in PSCAD™ to verify the performance of the implemented model. The simulations included only a test voltage and did not include the other parts of the inverter model. The PI controller gains are set according to (67) and (68) based on a target rise time of 100 ms and damping ratio of 0.707. Figure 3-14 shows the SRF-PLL response to a positive sequence step change of  $30^\circ$  in the voltage phase angle. Recalling that  $v_{tq}$  is the error signal, the top right plot shows the step response is approximately 50ms. Figure 3-15 shows the SRF-PLL response to a  $30^\circ$  step change in the phase A voltage angle. Figure 3-16 shows the response of the SRF-PLL response to a step change in the magnitude of the phase A voltage from 1.0 to 0.8. These two examples highlight the limitation of the SRF-PLL when the voltage is unbalanced. The  $dq$  signals show 120Hz oscillations due to the negative sequence component of the voltage. These simulations show that the SRF-PLL response is adequate for balanced signals but cannot track unbalanced signals with zero steady-state error.

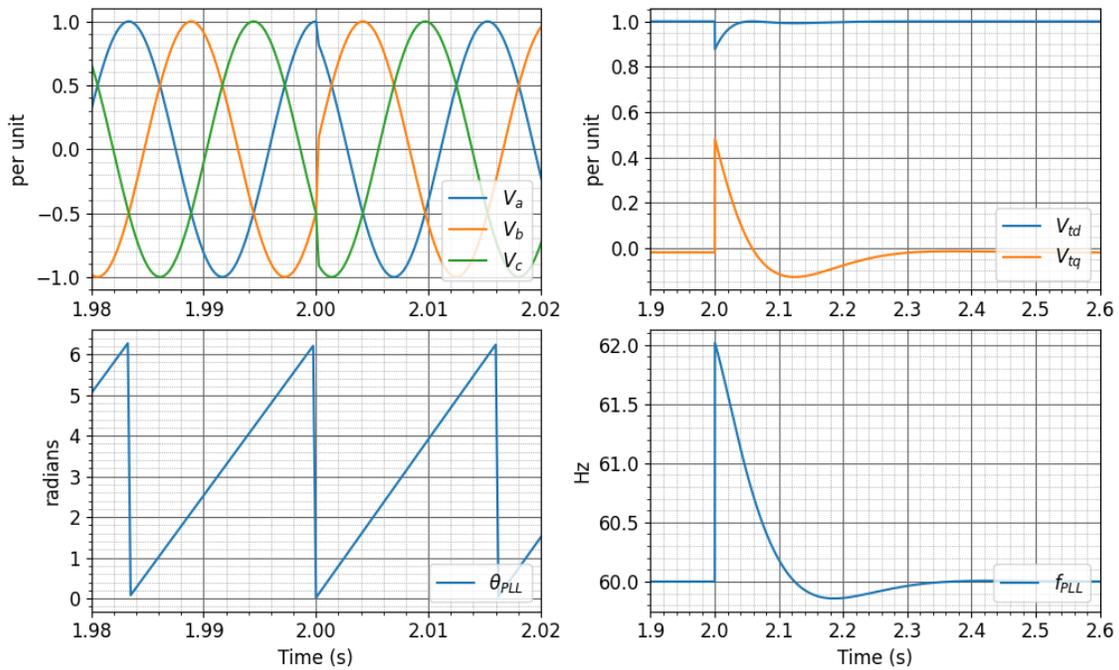


Figure 3-14. Response of the SRF-PLL for a balanced 30° step change in the voltage phase angle. PI gains:  $k_p = 25.4$  and  $k_i = 324$ . Top left: test voltage. Bottom left: PLL phase angle. Top right: d1-axis and q1-axis components of test voltage. Bottom right: PLL unfiltered frequency.

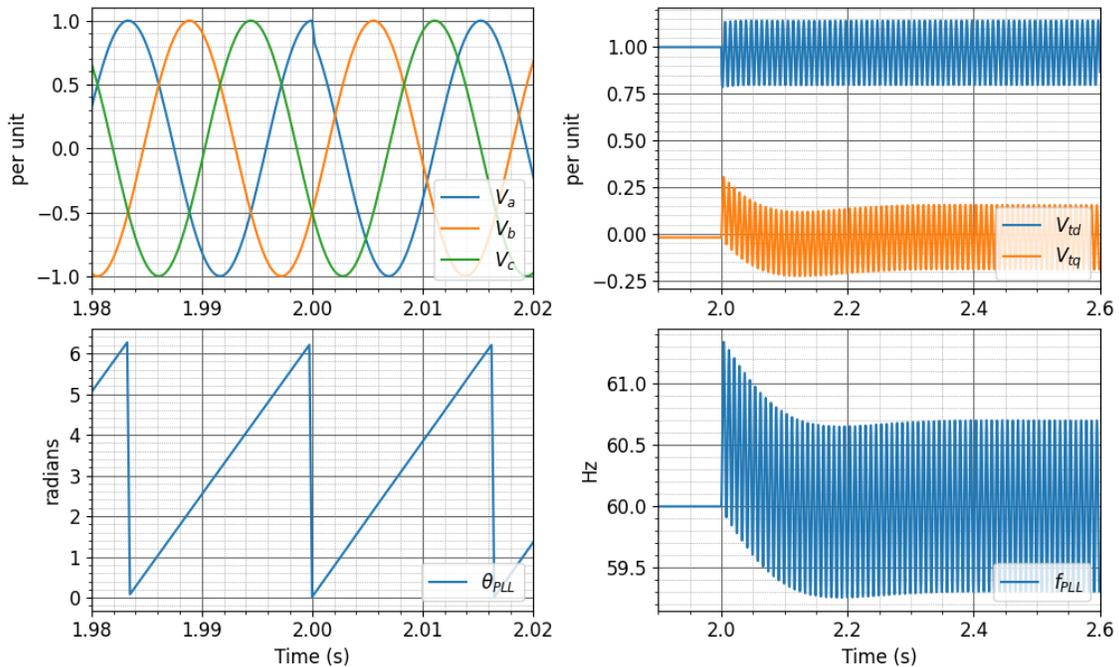


Figure 3-15. Response of the SRF-PLL for a 30° step change in the phase A voltage phase angle. PI gains:  $k_p = 25.4$  and  $k_i = 324$ . Top left: test voltage. Bottom left: PLL phase angle. Top right: d1-axis and q1-axis components of test voltage. Bottom right: PLL unfiltered frequency.

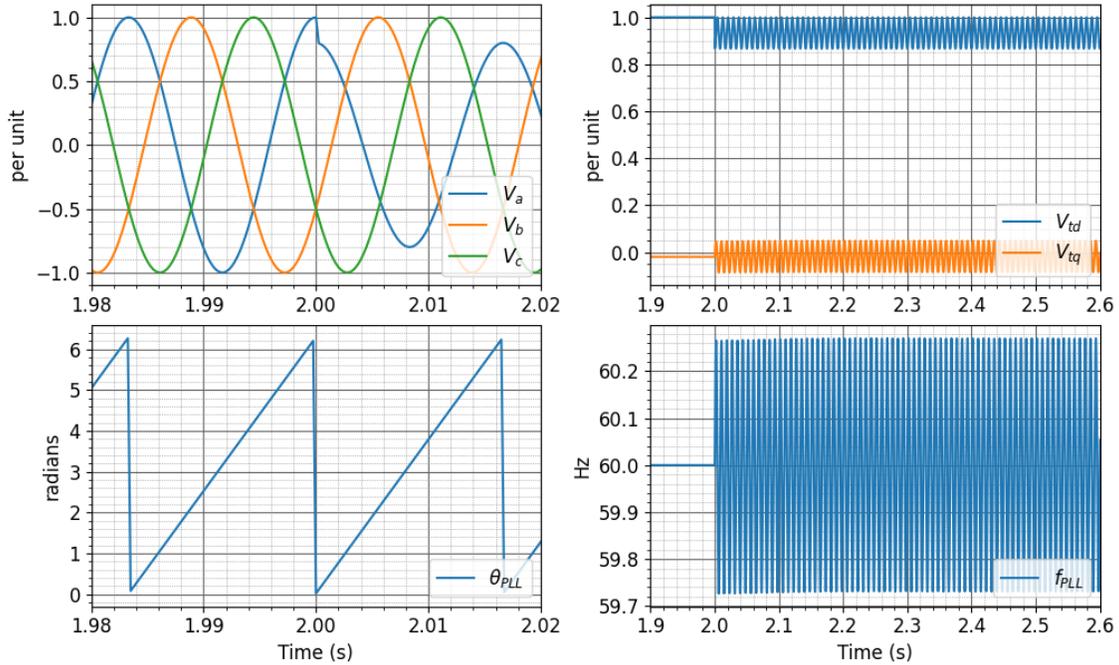


Figure 3-16. SRF-PLL response to a step change of -0.2pu in the phase A voltage. PI gains:  $k_p = 25.4$  and  $k_i = 324$ . Top left: test voltage. Bottom left: PLL phase angle. Top right: d1-axis and q1-axis components of test voltage. Bottom right: PLL unfiltered frequency.

### 3.3.5. Advanced PLLs

The simulations of the SRF-PLL show that the performance deteriorates when the grid voltage is unbalanced. Many grid codes require IBR to remain connected and provide grid support by injecting reactive current for low or high voltage conditions. Further, grid codes and performance standards such as [26-28, 57] require the inverter to provide negative sequence reactive current for asymmetrical grid faults based on the negative sequence voltage. Therefore, the inverter control needs the capability to detect the grid voltage's positive sequence and negative sequence fundamental frequency components.

To improve the performance of the SRF-PLL for voltage unbalance, many PLLs proposed in the literature add filtering to the SRF-PLL framework [58]. Two such SRF-PLLs are implemented in the model prototype: the Dual Second Order Generalized Integrator (DSOGI) PLL shown in

Figure 3-17 and the Decouple Double Synchronous Reference Frame (DDSRF) PLL shown in Figure 3-18. Appendix E shows the mathematical formulation of the DSOGI SRF-PLL proposed in [59] and the DDSRF PLL proposed in [60].

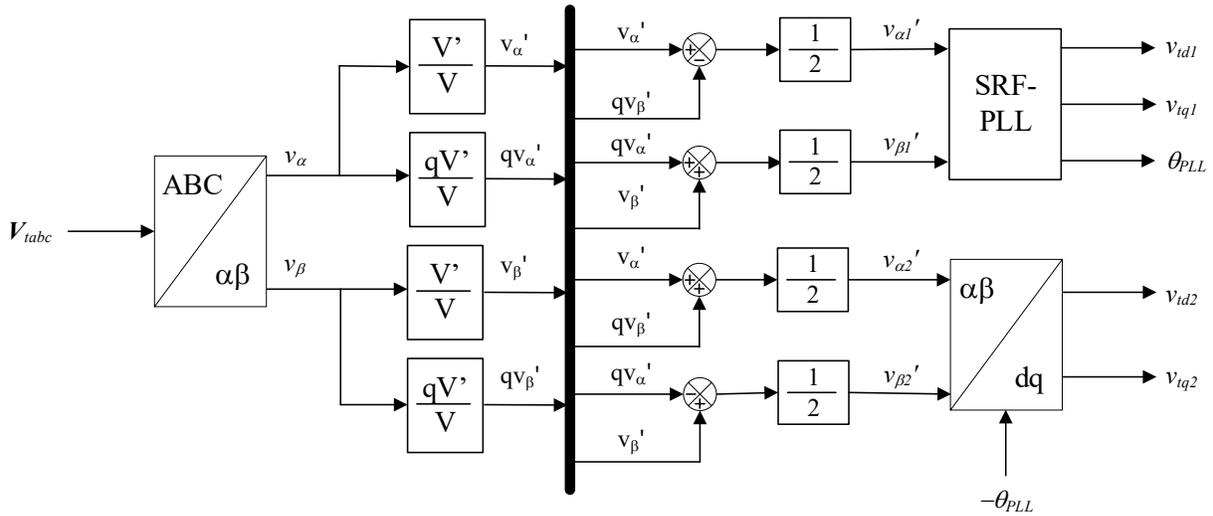


Figure 3-17: Block diagram of DSOGI SRF-PLL.

The transfer functions of the SOGI blocks are:

$$\frac{v'}{v} = \frac{k\omega_{PLL}S}{s^2 + k\omega_{PLL}S + \omega_{PLL}^2} \quad (69)$$

$$\frac{qv'}{v} = \frac{k\omega_{PLL}^2}{s^2 + k\omega_{PLL}S + \omega_{PLL}^2} \quad (70)$$

Figure 3-19 shows the response of the DSOGI SRF-PLL for a step change in the phase A voltage magnitude. The top right and bottom right plots show the test voltage's positive and negative SRF components calculated by the DSOGI SRF-PLL. The bottom left chart shows the DSOGI PLL frequency. Note that the 120Hz components observed in the PLL frequency and SRF signals in Figure 3-16 are removed. Figure 3-20 shows the response of the DDSRF-PLL for the same test input. Comparing the response of the PLL frequency and the SRF components, the

DSOGI SRF-PLL shows better attenuation of the 120Hz components compared to the DDSRF PLL.

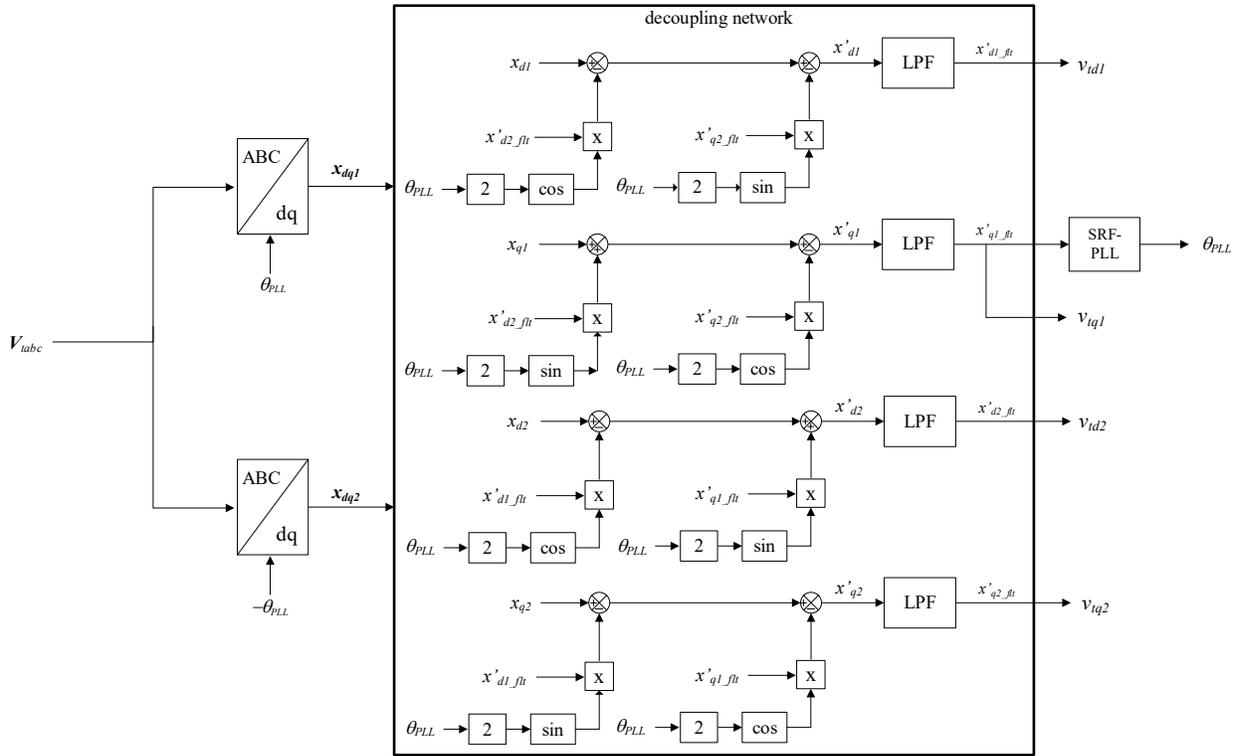


Figure 3-18. Block diagram of DDSRF SRF-PLL.

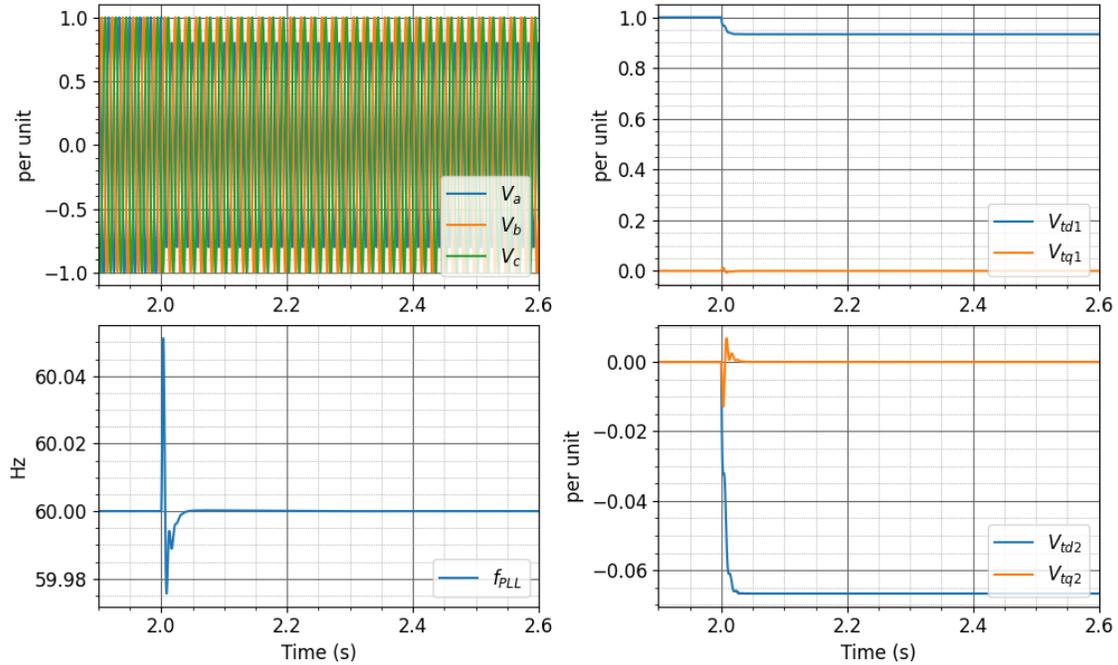


Figure 3-19. DSOGI SRF response to a step change of -0.2pu in the phase A voltage. PI gains:  $k_p=25.4$  and  $k_i=324$ . Top left: test voltage. Bottom left: PLL unfiltered frequency. Top right: d1 and q1 components of test voltage. Bottom right: d2 and q2 components of test voltage.

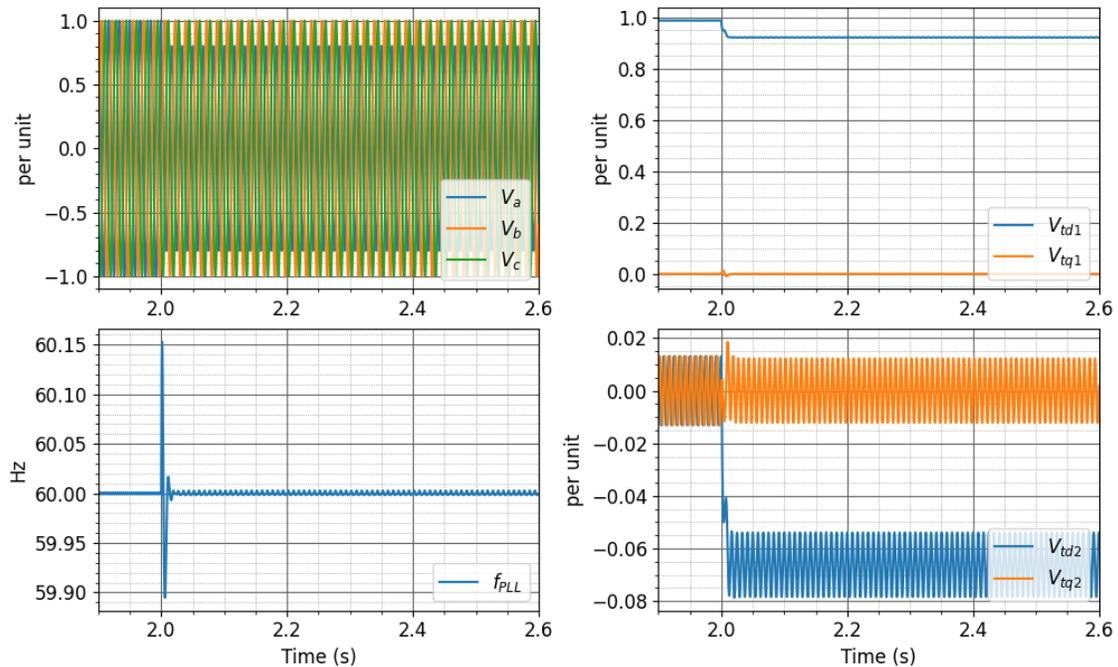


Figure 3-20. DDSRF SRF response to a step change of -0.2pu in the phase A voltage. PI gains:  $k_p=25.4$  and  $k_i=324$ . Top left: test voltage. Bottom left: PLL unfiltered frequency. Top right: d1 and q1 components of test voltage. Bottom right: d2 and q2 components of test voltage.

### 3.3.6. Summary

This section detailed the SRF-PLL structure and provided an analytical tuning method based on pole placement for the PLL LF implemented as a PI controller. Voltage unbalance and voltage distortion are shown to degrade the performance of the SRF-PLL significantly. The current mode-controlled inverter must track the grid voltage's positive and negative sequence fundamental frequency components to meet the performance requirements during asymmetrical grid faults. The DSOGI SRF-PLL and the DDSRF-PLL are implemented in the model prototype. Simulations of unbalanced voltages show that both the DSOGI SRF-PLL and the DDSRF PLL can detect the grid voltage's positive and negative sequence components. However, both PLLs' performance will deteriorate for distorted voltages without further additions. The DSOGI SRF-PLL and the DDSRF PLL can be tuned based on the analytical methods presented for the SRF-PLL.

### 3.4. Positive and Negative Sequence Components of the Current

In Section 3.2, current controllers were applied in both the positive and negative SRFs. However, the determination of these components from the measured current was not discussed. For the current controllers in Figure 3-4, the detection of the positive and negative sequence components of the current is required in the feedback signals. In Section 3.3, both the DSOGI SRF-PLL and the DDSRF PLL are shown to be capable of determining the fundamental frequency positive and negative sequence components of the terminal voltage. This allows the tracking of the phase angle of the positive sequence fundamental frequency component of the voltage, establishing the positive SRF. The negative SRF is established by the same instantaneous angle but rotating in the opposite direction. Figure 3-21 shows the positive and negative SRFs rotating in the  $\alpha\beta$ -plane. The positive SRF rotates counterclockwise at an angular frequency of  $\omega_{PLL}$ . The

negative sequence SRF rotates clockwise at an angular frequency of  $\omega_{PLL}$ . The d2-axis of the negative SRF is located at  $-\theta_{PLL}(t)$ .

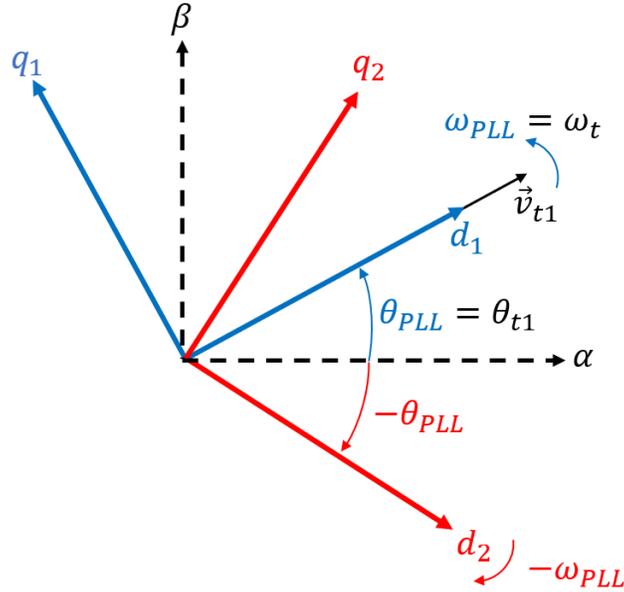


Figure 3-21: Positive SRF (blue) and negative SRF (red) established by the PLL.

### 3.4.1. Cross Coupling of Positive and Negative SRFs

Transforming unbalanced signals to the positive and negative SRFs via the Park transform results in coupling between the signals in the two SRFs. The positive SRF signals contain  $2f_0$  components related to the magnitude of the negative sequence component, and the negative SRF signals contain  $2f_0$  components related to the magnitude of the positive sequence component. This section shows the mechanism of the cross-coupling between the positive and negative SRFs. Given an unbalanced current consisting of positive and negative sequence components, the space vector of the current is written as a superposition of the components.

$$\mathbf{i}_{\alpha\beta}(t) = |\mathbf{i}_{\alpha\beta 1}|e^{j\theta_{i1}(t)} + |\mathbf{i}_{\alpha\beta 2}|e^{j\theta_{i2}(t)} \quad (71)$$

$\theta_{i1}$  and  $\theta_{i2}$  are the instantaneous phase angles of the positive and negative sequence space vectors.

$$\theta_{i1}(t) = \omega_0 t + \angle I_1 \quad (72)$$

$$\theta_{i2}(t) = -\omega_0 t - \angle I_2 \quad (73)$$

$I_1$  and  $I_2$  are the positive and negative sequence phase A current phasors. Transforming the current to the positive SRF by multiplying by  $e^{-j\theta_{PLL}}$  results in:

$$\mathbf{i}_{dq1} = |\mathbf{i}_{\alpha\beta1}| e^{j\theta_{i1}(t)} e^{-j\theta_{PLL}} + |\mathbf{i}_{\alpha\beta2}| e^{j\theta_{i2}(t)} e^{-j\theta_{PLL}} \quad (74)$$

It is assumed that the PLL is perfectly tracking the positive sequence fundamental frequency component of the grid voltage such that:

$$\theta_{PLL} = \omega_0 t + \angle V_{t1} \quad (75)$$

Substituting (75) into (74) shows a DC component equal to the magnitude of the positive sequence current and sinusoidal component with a frequency of  $2f_0$  and a magnitude of the negative sequence current.

$$\mathbf{i}_{dq1} = |\mathbf{i}_{\alpha\beta1}| e^{j(\angle I_1 - \angle V_{t1})} + |\mathbf{i}_{\alpha\beta2}| e^{-j(2\omega_0 t + \angle V_{t1} + \angle I_2)} \quad (76)$$

Similarly, transforming the current to the negative SRF by multiplying by  $e^{j\theta_{PLL}}$  results in:

$$\mathbf{i}_{dq2} = |\mathbf{i}_{\alpha\beta1}| e^{j(2\omega_0 t + \angle V_{t1} + \angle I_1)} + |\mathbf{i}_{\alpha\beta2}| e^{j(\angle V_{t1} - \angle I_2)} \quad (77)$$

Equations (76) and (77) show how the sinusoidal double fundamental frequency component is manifested in the cross-coupling between the positive and negative SRFs.

### 3.4.2. Decoupling of Positive and Negative SRF Components

The cross-coupling can be avoided by transforming only the positive sequence component of the signal to the positive SRF and only the negative sequence component of the signal to the negative SRF. This is the approach taken in the DSOGI SRF-PLL, where the signals are filtered and decoupled in the stationary reference frame to determine their positive and negative sequence components [59].

Another approach is to apply filtering to the signals in the SRF. However, the desired closed-loop bandwidth of the current response on the order of 100s of Hz limits the ability to use low pass filtering to attenuate the  $2f_0$  component. For example, consider the simplified current control diagram including a 1<sup>st</sup> order LPF in the feedback path as shown in Figure 3-22.

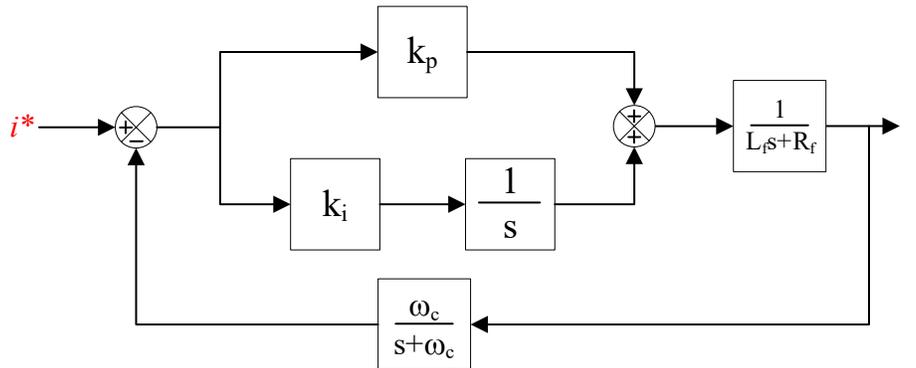


Figure 3-22: Simplified current control block diagram with 1<sup>st</sup> order LPF in the feedback path.

For illustration purposes, the LPF is set with a cut-off frequency of 60 Hz, resulting in an approximately 55% reduction of the 120 Hz component magnitude in the feedback path. The current controller PI gains are set to  $k_p = 0.32$  and  $k_i = 324.0$  based on a target rise time of 1ms referring to Table 3-I. Figure 3-23 compares the open loop frequency response of the current with and without filtering in the current control feedback path. The response of the LPF is included for reference. With the inclusion of the LPF, the frequency response shows a negative phase margin

indicating instability. The eigenvalues of the closed-loop system indicate two poles in the RHP, confirming the system is unstable. Figure 3-23 shows that increasing the target rise time of the current by an order of magnitude to 10 ms results in a phase margin of  $\sim 35$  degrees. However, this is outside of the desired bandwidth of the current controller. This example shows the performance of the current control is significantly deteriorated by the addition of the LPF to attenuate the 120Hz component of the signal. Further, the 120Hz component is not completely removed. The frequency response in this example shows the decrease in phase due to the LPF. Increasing the order of the LPF is not a viable solution as this results in faster deterioration of the phase. The LPF solution is more feasible for lower bandwidth controllers such as the PLL in Section 3.3.

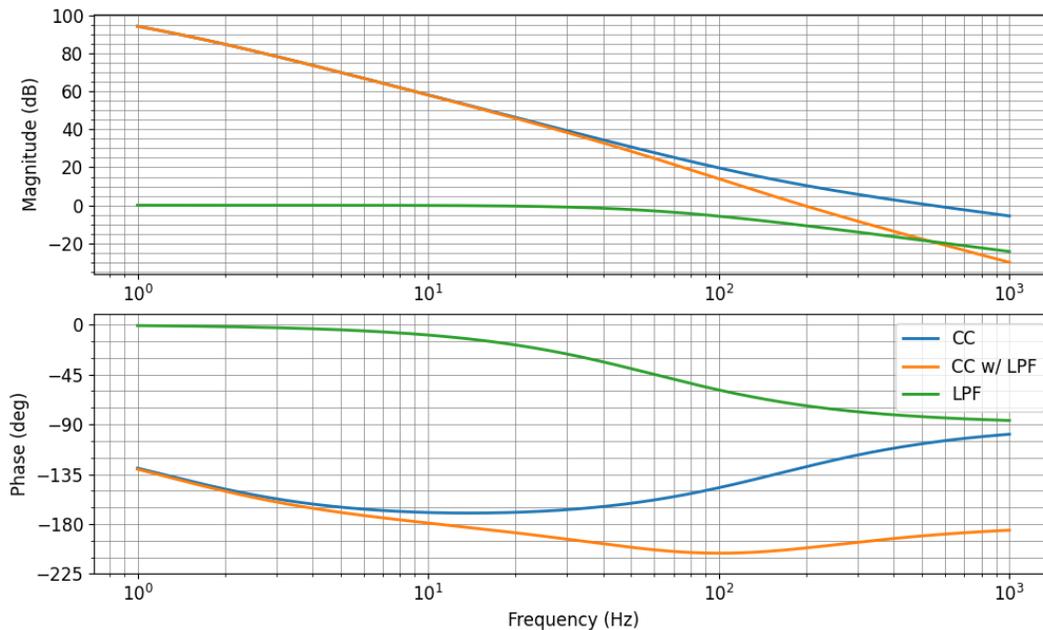


Figure 3-23: Frequency response of the LPF (green trace) and the current with (orange trace) and without (blue trace) LPF filtering for a target rise time of 1ms.

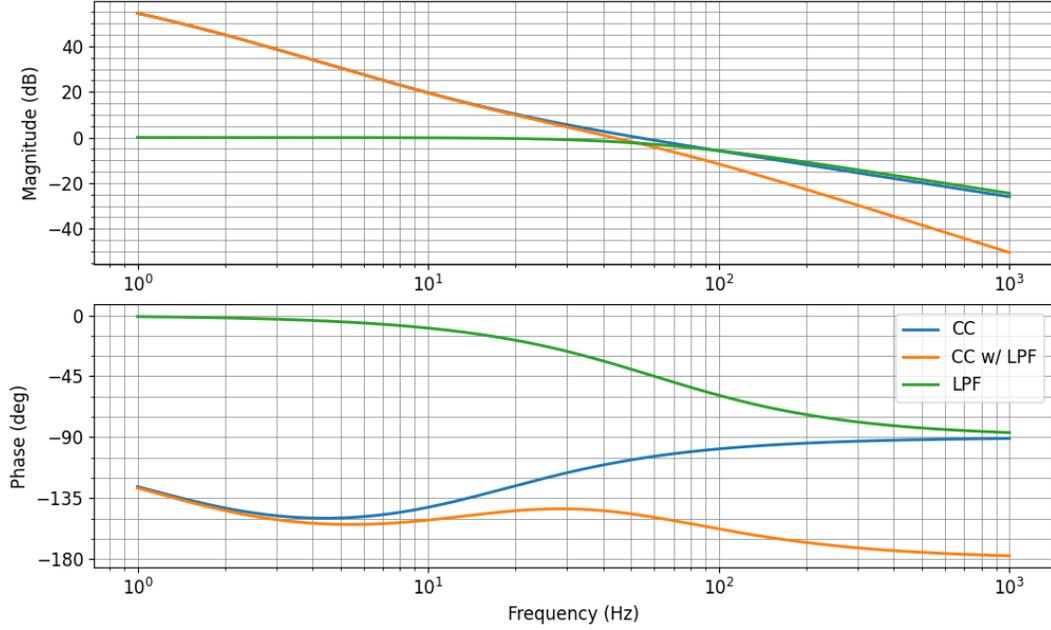


Figure 3-24. Frequency response of the LPF (green trace) and the current with (orange trace) and without (blue trace) LPF filtering for a target rise time of 10ms.

The authors in [48] propose adding a notch filter tuned to 120Hz to remove the coupling between the positive and negative sequence SRF components. The transfer function of a second-order notch filter is:

$$G_n(s) = \frac{s^2 + \omega_r^2}{s^2 + 2\zeta\omega_r s + \omega_r^2} \quad (78)$$

where  $\omega_r$  is the resonant frequency and  $2\zeta\omega_r$  is the -3dB bandwidth of the filter. Figure 3-25 shows the frequency response of the second-order notch filter in (78) with the resonant frequency set to  $\omega_r = 2\pi 120 \text{ rad/s}$  for various values of  $\zeta$ . As the bandwidth is increased, a larger range of frequencies are attenuated, and more phase lag is added for frequencies less than the resonant frequency.

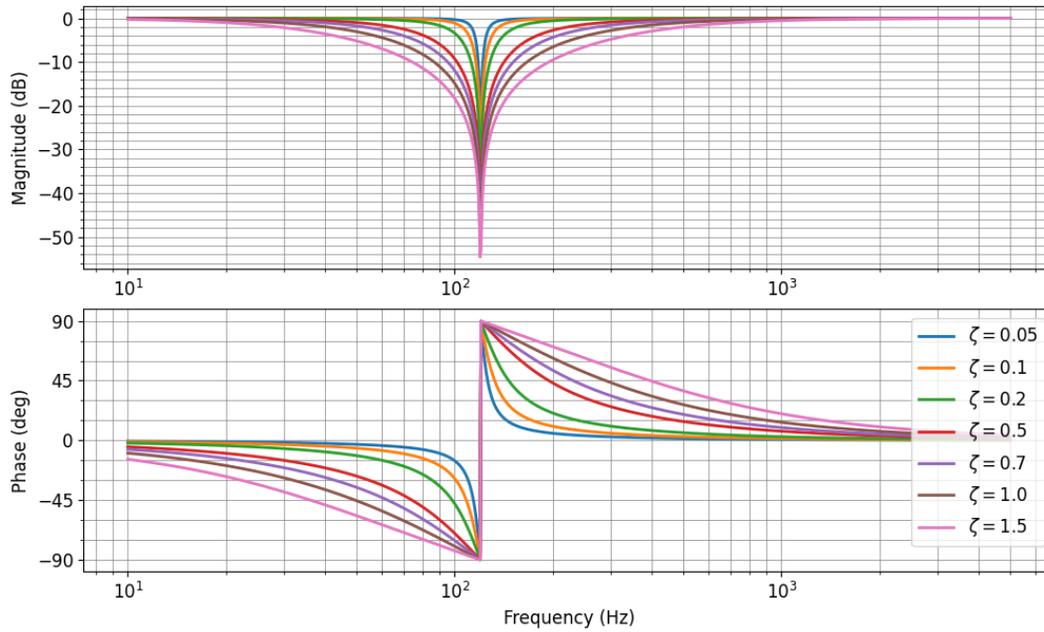


Figure 3-25. Frequency response of a second-order notch filter with a resonant frequency of 120 Hz.

The second-order notch filter was implemented in the full model prototype to attenuate the 120 Hz components in the SRF current signals. The notch filter bandwidth had to be reduced to approximately 12Hz ( $\zeta = 0.05$ ) to obtain a stable response. The simplified model of the closed-loop current control in Figure 3-22 was modified by replacing the LPF with a second-order notch filter to investigate further. Figure 3-26 compares the frequency response of the open loop current control with and without the notch filter for two bandwidths. Figure 3-27 compares the corresponding step response of the closed-loop simplified model. The frequency response and step response of the simplified linear model predict the poor performance and instability of the closed-loop current control with the addition of the notch filter. Figure 3-28 shows that increasing the rise time of the current controller, i.e., reducing the current controller bandwidth, will result in a stable response like the LPF example.

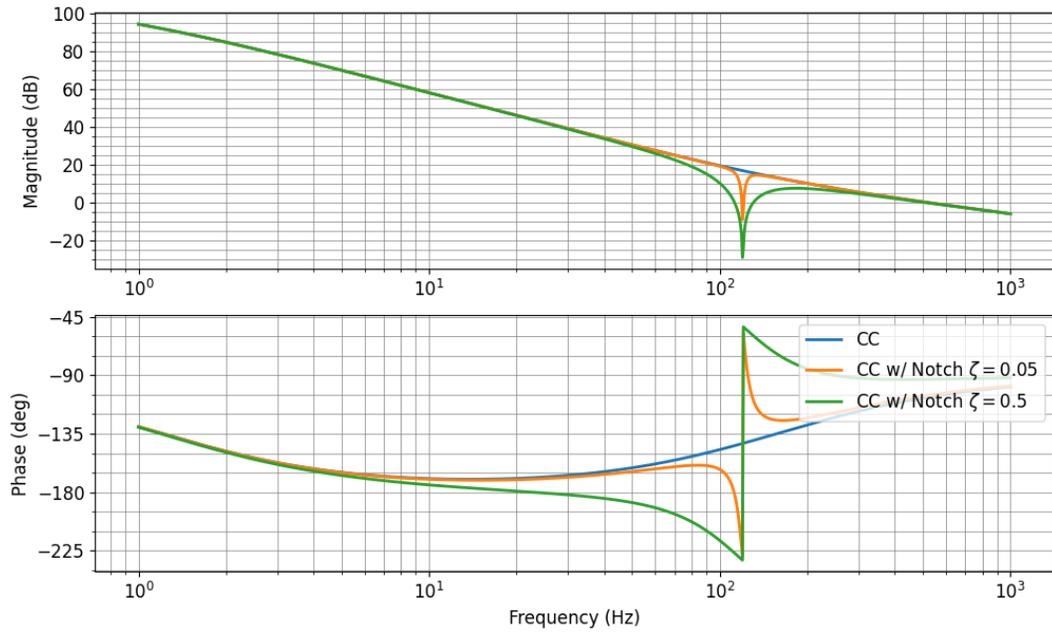


Figure 3-26: Open loop frequency response of the current with a notch filter (orange trace and green trace) and without a notch filter (blue trace) in the feedback path.

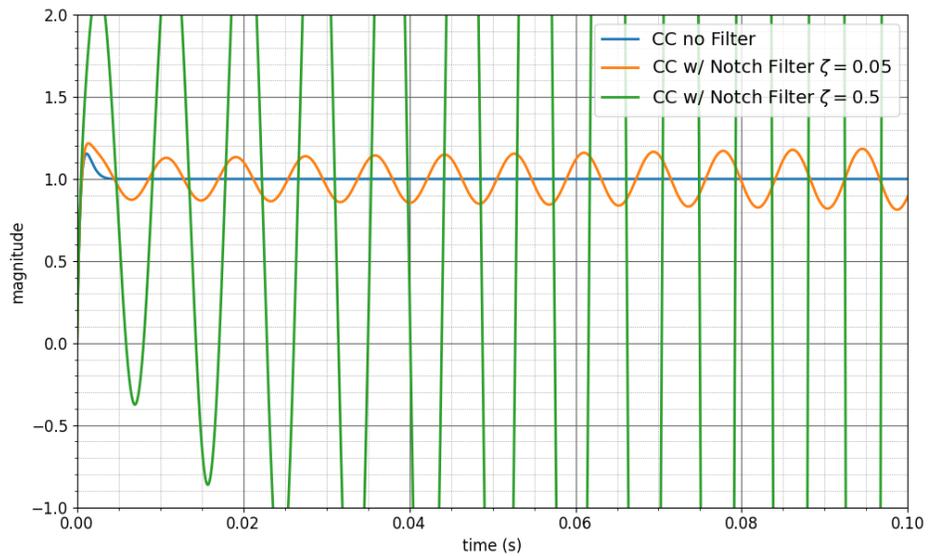


Figure 3-27: Step response of the current with a notch filter (orange trace and green trace) and without a notch filter (blue trace) in the feedback path.

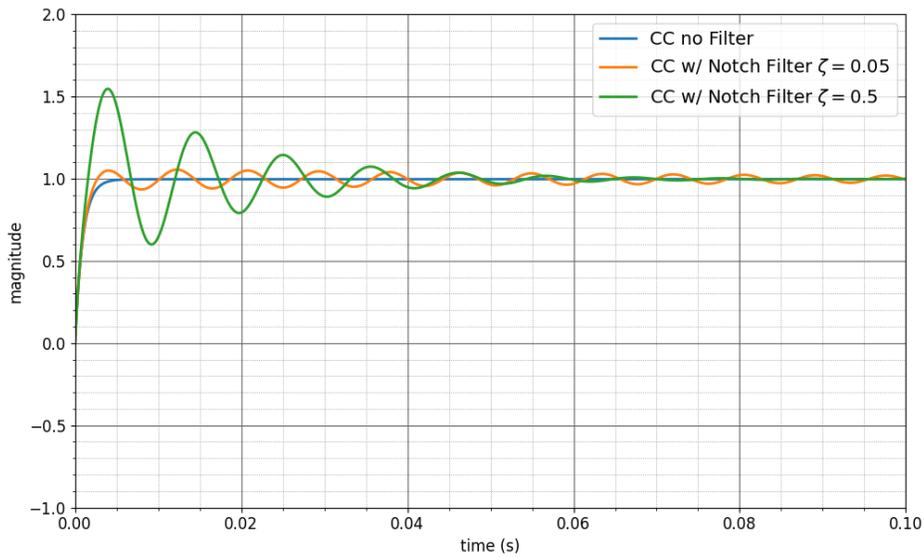


Figure 3-28. Decreased current controller bandwidth. Step response of the current with a notch filter (orange trace and green trace) and without a notch filter (blue trace) in the feedback path.

The other approach considered in the model prototype is a slight modification of the DDSRF framework proposed in [60]. The DDSRF uses a decoupling network in the SRF that includes low pass filtering. The DDSRF was adequate for the PLL but was not stable when implemented in the current control. The previous examples indicate this is likely due to the current controller's much higher bandwidth than the PLL. Therefore, the output of the DDSRF is taken before the LPF, as shown in red in Figure 3-29, to reduce the impact of the LPF on the closed loop stability.

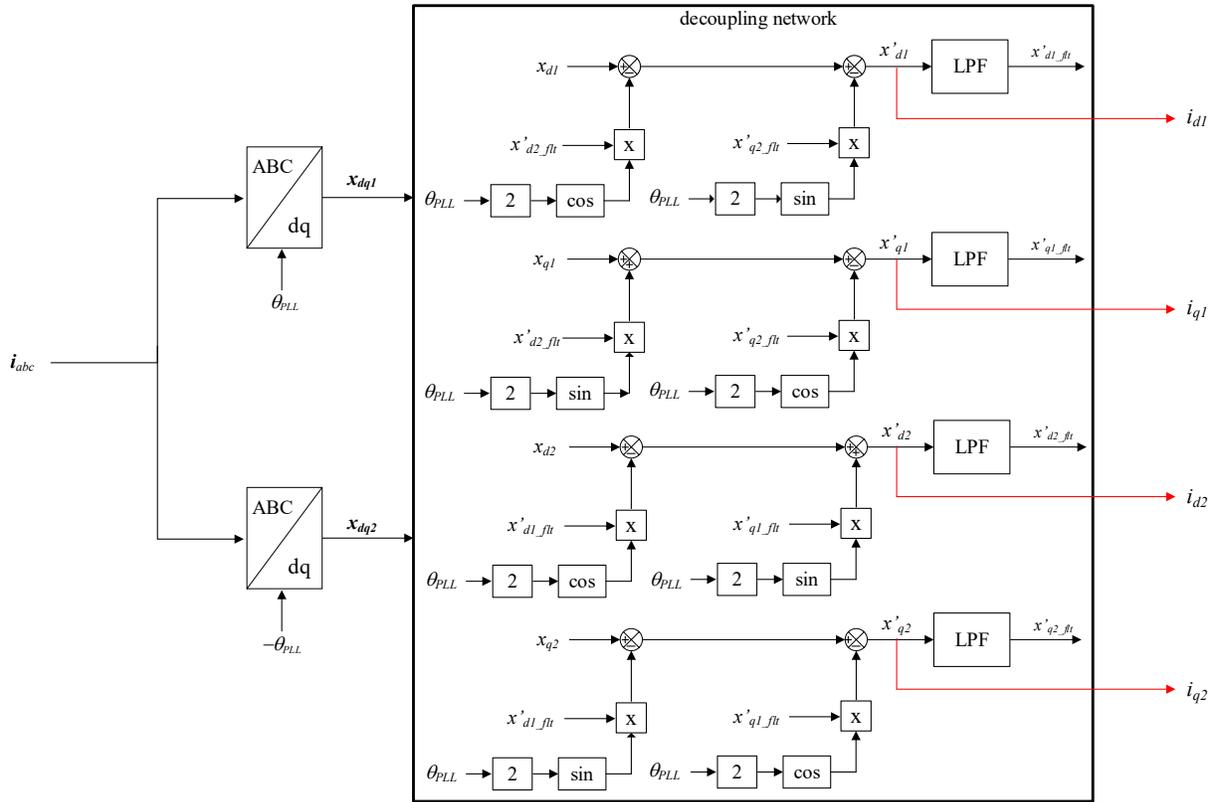


Figure 3-29: Modified DDSRF block diagram used to extract the positive and negative SRF components of the current.

The modified DDSRF block diagram in Figure 3-29 is implemented and tested in the full model prototype. A step change in the negative sequence q-axis current reference,  $i_{q2}^*$ , of 0.05 pu is considered for the three sets of gains in Table 3-I of the current controller. Figure 3-30 shows the response of the current components with the modified DDSRF. The negative sequence current step response is consistent with the positive sequence current response analyzed in Section 3.2.3. Similar cross-coupling between the negative SRF d-axis and q-axis is also observed. Cross-coupling between the positive and negative SRF components is shown, but significantly less compared to the magnitude of the cross-coupling between the d-axis and q-axis signals in each SRF. Figure 3-31 compares the response of the current control with the modified DDSRF and the notch filter. The current controllers with the modified DDSRF provide a superior response to those

using a notch filter. The coupling between the positive and negative SRFs is much stronger with the notch filter implementation. Therefore, the modified DDSRF is used in the model prototype for the sequence current decomposition.

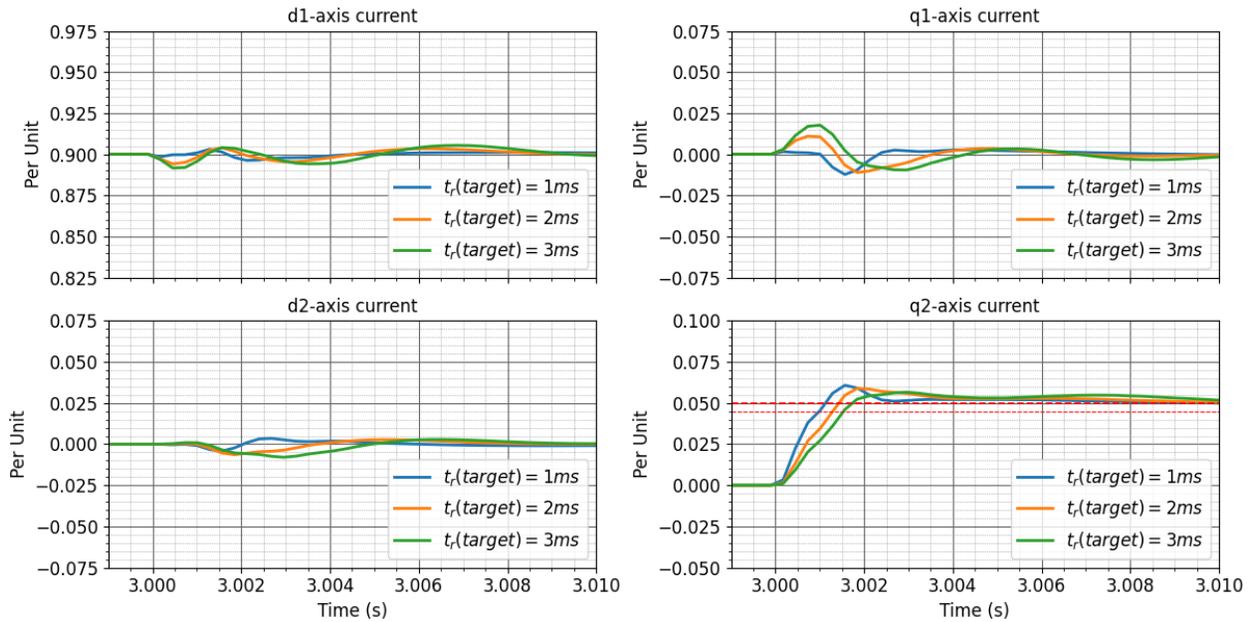


Figure 3-30. Response of the dual SRF currents to a step change in  $i_{q2}^*$  in the full model prototype.

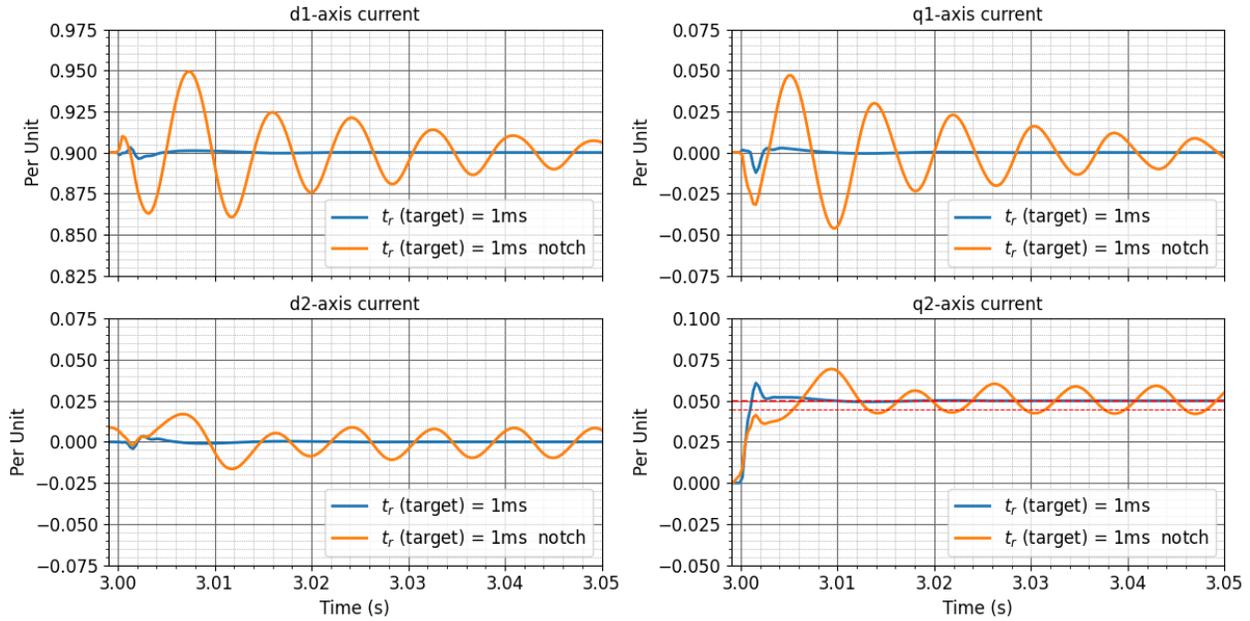


Figure 3-31. Comparison of the current response to a step change of  $i_{q2}^*$  in the full model prototype with the current controller including the modified DDSRF (blue trace) and the current controller including a notch filter (orange trace) in the feedback path.

### 3.4.3. Summary

This section discusses the detection of the positive and negative sequence current components in the feedback path of the dual SRF current controllers. The coupling between the positive and negative sequence SRFs manifests as a  $2f_0$  component due to the transformation to the positive and negative SRFs. The same cross-coupling is present with the voltage signals, but the lower bandwidth of the PLL compared to the current controllers allows various filtering options to provide adequate performance. The phase lag introduced by the filtering below the desired bandwidth of the control negatively impacts the stability of the higher bandwidth current control loops. Two approaches are discussed and implemented in the model prototype. The modified DDSRF shown in Figure 3-29 is the default in the model prototype due to its superior performance to the notch filter.

### **3.5. Outer Loop Control**

The inverter's active power, reactive power, AC voltage, and DC voltage control functions are included in the outer loop of the cascade control structure. The model prototype is configurable for different combinations of control objectives. When the inverter AC terminal voltage is within the continuous operating range (magnitude and frequency), a typical control approach is for the inverter to regulate the DC link voltage and follow a reactive power reference from the plant controller. The control objective of the inverter changes depending on the terminal voltage conditions. When the inverter terminal AC voltage is outside the continuous operating range, the inverter autonomously controls its terminal voltage to provide grid support. This is referred to as fault ride-through (FRT) control mode in this work. Two distinct control modes, continuous and FRT, are implemented in the model prototype and automatically selected based on the measured terminal voltage and configuration. This section details the control objective, the process model, and an analytical tuning method for each controller that is part of the outer loop in the model prototype.

#### **3.5.1. Instantaneous Active and Reactive Power**

The concept of instantaneous active and reactive power, also referred to as “p-q Theory” in the literature, is convenient for analyzing and designing controllers for inverters. p-q Theory provides a time-domain description of active and reactive power based on instantaneous values of voltage and current that are valid for both steady-state and transient conditions [61]. In contrast, active and reactive power calculations based on phasor domain signals require the system to be in sinusoidal steady state. For a three-phase, three-wire system, the instantaneous active and reactive power exchanged with the grid based on the nomenclature in this work is given by:

$$\mathbf{s}_{inv} = \frac{3}{2} [(v_{t\alpha}i_\alpha + v_{t\beta}i_\beta) + j(-v_{t\alpha}i_\beta + v_{t\beta}i_\alpha)] \quad (79)$$

where the  $3/2$  term is added to maintain power invariance based on the assumed scalar in the Clarke transformation. Given that the inverter control is implemented in the SRF, the  $\alpha\beta$  signals are multiplied by  $\exp(-\theta_{PLL})$  to transform to the SRF.

$$\begin{aligned} \mathbf{s}_{inv} &= \frac{3}{2} \mathbf{v}_{t\alpha\beta} \overline{\mathbf{i}_{\alpha\beta}} = \frac{3}{2} (\mathbf{v}_{tdq} e^{j\theta_{PLL}}) \overline{(\mathbf{i}_{dq} e^{j\theta_{PLL}})} \\ &= \frac{3}{2} [(v_{td}i_d + v_{tq}i_q) + j(-v_{td}i_q + v_{tq}i_d)] \end{aligned} \quad (80)$$

The overbar signifies the complex conjugate.

Equation (80) shows a major benefit of implementing the inverter control in the SRF. If the SRF's d-axis is aligned to the space vector of the grid voltage, then  $v_{tq} = 0$ . This result provides decoupling of the d-axis and q-axis control loops where the active power is controlled by the d-axis current and the reactive power is controlled by the q-axis current.

$$p_{inv}(v_{tq} = 0) = \frac{3}{2} v_{td}i_d \quad (81)$$

$$q_{inv}(v_{tq} = 0) = -\frac{3}{2} v_{td}i_q \quad (82)$$

Note that if the PLL is not perfectly tracking the phase angle of the grid voltage, there will be a non-zero component of  $v_{tq}$ . This results in the q-axis current contributing to the active power and the d-axis current contributing to the reactive power. In this case, the simplified equations (81) and (82) are inaccurate.

### 3.5.2. Active Power Control

The power output of a PV array depends on the solar irradiance, the voltage, and the operating temperature of the solar cells comprising the PV array. Of these, the voltage is directly controllable. A common approach is to control the voltage across the PV array to extract the maximum available power based on the given atmospheric conditions by operating at the maximum power point (MPP) of the array's V-I curve. When the control objective is to operate at the MPP of the resource, the inverter control ensures the balance of power between the inverter's DC side and AC side by regulating the DC link voltage [53].

Alternatively, the active power can be limited to a reference value less than the maximum power available from the resource. This strategy may be used if it is required to limit the plant output or maintain headroom to respond to low frequency events on the grid. In this case, the control of the PPS must be regulated to find the corresponding operating point. From the plant owner's perspective, not operating at the maximum power available from the resource results in a loss in potential revenue as the fuel cost is zero. In the U.S., FERC Order 842 requires all resources under their jurisdiction to have the capability to provide primary frequency response [62]. Draft 6.1 of IEEE P2800 also requires the IBR to have the capability to provide a frequency-droop response. Further, Draft 6.1 of IEEE P2800 requires utilization of this capability for low frequency if headroom is available and for high frequency if operating above its minimum power limit. However, neither require headroom to be maintained to allow response to low frequency. A common control architecture is for the frequency-droop control to be implemented at the plant level. However, in the future, it may become more common to implement this function in the inverter-level control with the immediate benefit of removing some of the delay associated with the communication from the plant controller to the inverters.

With this background, the remaining parts of this section detail the control functions of the inverter that affect the active power exchange with the grid. This includes DC link voltage control, frequency-droop control, and active power setpoint following. The assumptions made in the modeling of the DC input power from the PPS are also discussed.

### 3.5.2.1. DC Link Voltage Control

The control of the inverter's active power involves controlling both the DC power input and the AC power output. The energy storage capacity of the DC bus is typically small. Therefore, all the DC input power from the PPS (e.g., PV, batteries, wind) must be injected into the AC grid. If this balance is not maintained, the DC bus voltage will change based on the DC link capacitor voltage dynamics. In this section, it is assumed that the PPS is operated at its MPP. Therefore, the inverter controls the balance of power by controlling the DC link voltage.

#### 3.5.2.1.1. DC Link Voltage Dynamics Model

Figure 3-32 shows one leg of a two-level, three-phase voltage-sourced inverter. The DC link capacitor voltage dynamics depend on the DC input current from the PPS and the inverter output current.

$$I_{pv} - I_{inv} = I_{cap} = C_{dc} \frac{dV_{dc}}{dt} \quad (83)$$

Based on (83), if  $I_{pv}$  does not equal  $I_{inv}$ , the DC link voltage will change with time. As discussed in Section 2.2, from the control perspective, we are interested in the average value of the DC link voltage.

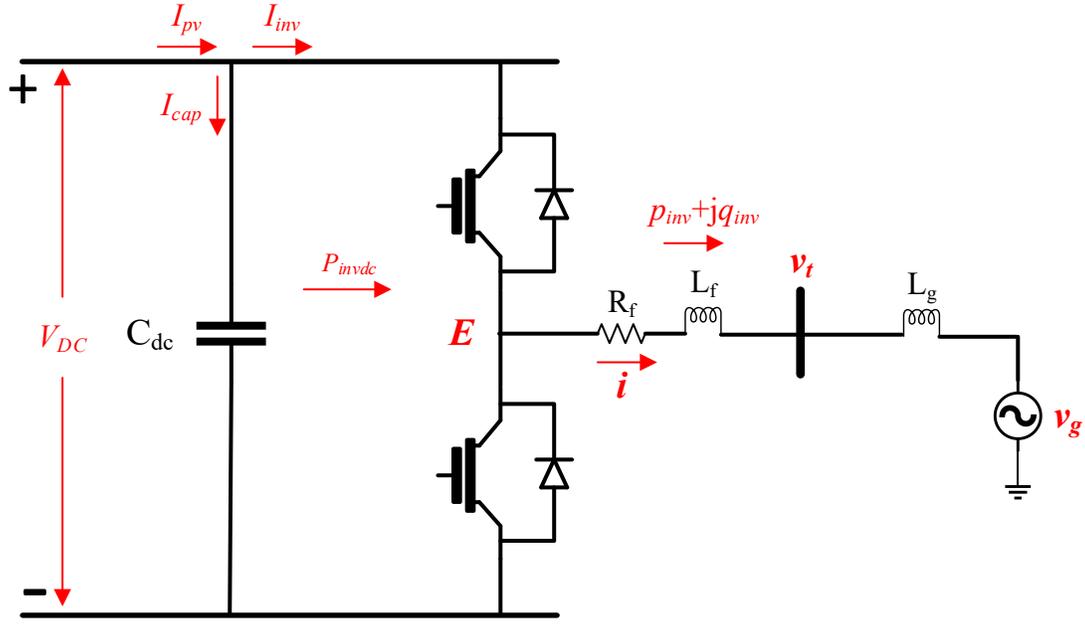


Figure 3-32. Simplified diagram of one leg of a three-phase voltage-sourced inverter.

The inverter power at the boundary is considered to develop a relationship between the DC voltage and the inverter AC current. The inverter DC power is equal to the AC power plus losses. Therefore, the inverter DC current is related to the d-axis and q-axis signals by:

$$V_{dc}I_{inv} = P_{invdc} = p_{inv} + P_{loss} = \frac{3}{2}(v_{td}i_d + v_{tq}i_q) + P_{loss} \quad (84)$$

Combining (84) and (83) and neglecting losses, the DC voltage dynamics in state-space form are given by:

$$\frac{dV_{dc}}{dt} = \frac{I_{pv}}{C_{dc}} - \frac{3}{2V_{dc}} \frac{1}{C_{dc}} (v_{td}i_d + v_{tq}i_q) \quad (85)$$

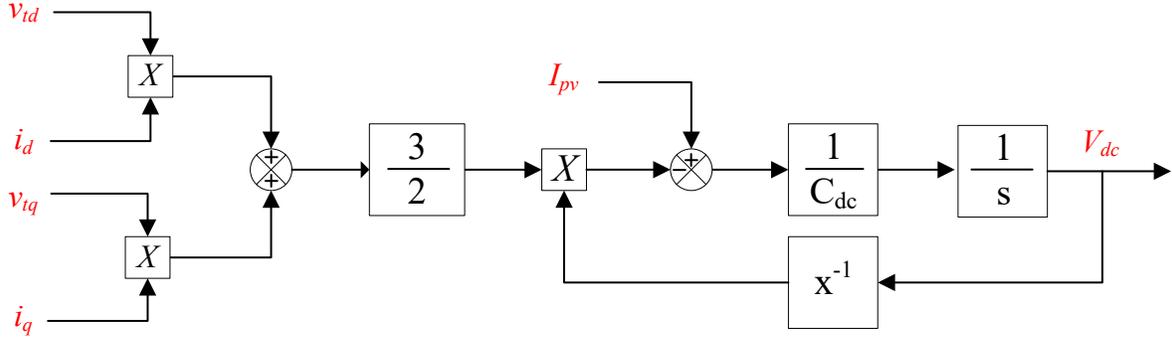


Figure 3-33. Block diagram of the DC link voltage dynamics.

The model in Figure 3-33 is linearized to apply linear control techniques. The small-signal model of the capacitor voltage is:

$$\begin{aligned} \Delta \dot{V}_{dc} = & \frac{\Delta I_{pv}}{C_{dc}} + \Delta V_{dc} \frac{3}{2V_{dc0}^2} \frac{1}{C_{dc}} (v_{td0}i_{d0} + v_{tq0}i_{q0}) \\ & - \frac{3}{2V_{dc0}} \frac{1}{C_{dc}} (\Delta v_{td}i_{d0} + v_{td0}\Delta i_d + \Delta v_{tq}i_{q0} + v_{tq0}\Delta i_q) \end{aligned} \quad (86)$$

In steady-state,  $v_{tq0} = 0$  based on the PLL. Substituting  $p_{inv0} = \frac{3}{2}(v_{td0}i_{d0} + v_{tq0}i_{q0})$  and  $v_{tq0} = 0$  results in the linearized model of the DC link capacitor voltage shown in Figure 3-34.

$$\begin{aligned} \Delta \dot{V}_{dc} = & \frac{\Delta I_{pv}}{C_{dc}} + \Delta V_{dc} \frac{1}{C_{dc}V_{dc0}^2} P_{inv0} \\ & - \frac{3}{2V_{dc0}} \frac{1}{C_{dc}} (\Delta v_{td}i_{d0} + v_{td0}\Delta i_d + \Delta v_{tq}i_{q0}) \end{aligned} \quad (87)$$

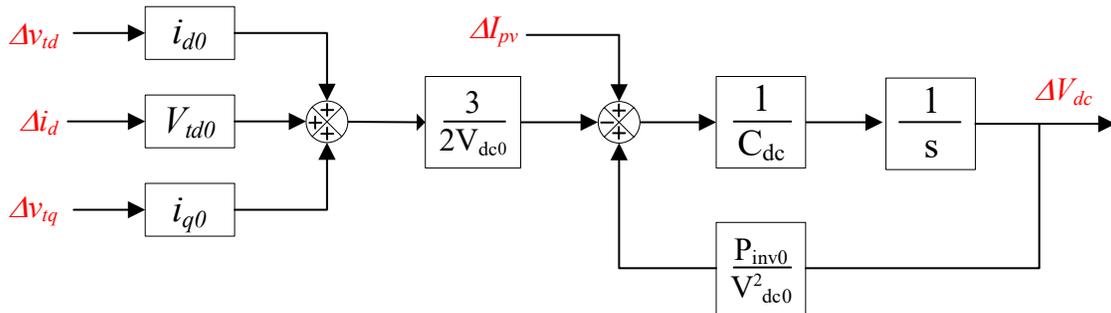


Figure 3-34. Block diagram of the small-signal model of the DC-link voltage dynamics.

### 3.5.2.1.2. DC Link Voltage Controller

From Figure 3-33, the DC link voltage can be controlled by the d-axis current of the inverter or the input current into the DC bus from the PPS. In this model, the inverter controls the DC link voltage. All perturbations in (87) other than the d-axis current are set to zero to develop the transfer function of the small-signal model of the d-axis current to the DC link voltage. Transforming to the frequency domain gives the following transfer function.

$$\frac{\Delta V_{dc}(s)}{\Delta i_d(s)} = -\frac{3v_{td0}}{2(sC_{dc}V_{dc0} - \frac{P_{inv0}}{V_{dc0}})} \quad (88)$$

Figure 3-35 shows the DC voltage control block diagram. The output of the PI controller is the d-axis reference current to the inner current controller. The current input from the PV arrays,  $I_{pv}$ , can be used as a feedforward signal. The DC voltage controller is tuned to have a bandwidth less than 1/10 of the bandwidth of the current controllers. Thus, the current regulator is neglected in the tuning for simplicity.

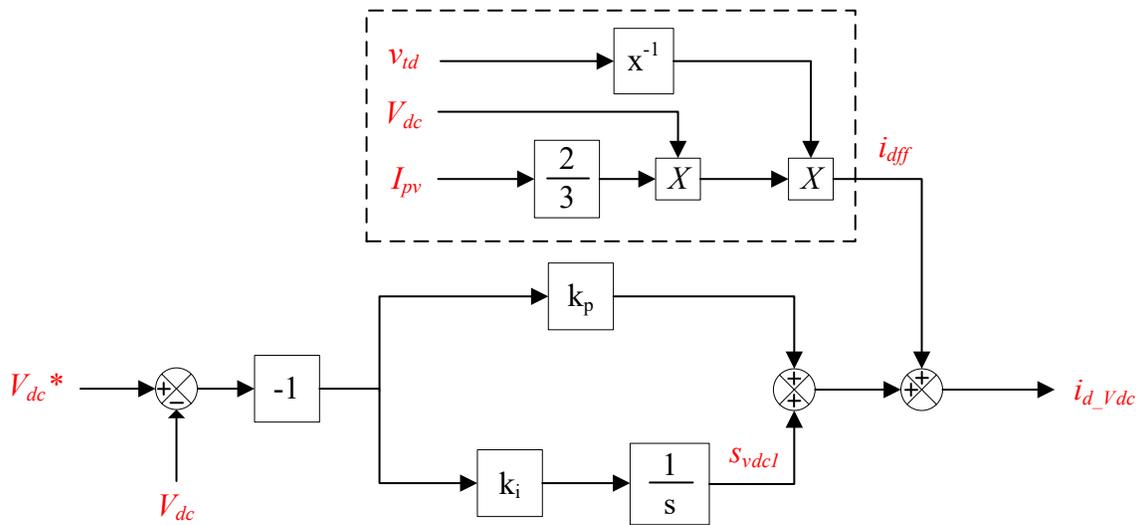


Figure 3-35: DC voltage controller block diagram.

The resulting closed-loop transfer function of the small-signal model of the DC voltage control is given by:

$$\frac{V_{dc}(s)}{V_{dc}^*(s)} = \frac{3v_{td0}(k_p s + k_i)}{2C_{dc}V_{dc0}^2 \left( s^2 + \frac{(3V_{dc0}v_{td0}k_p - 2P_{inv0})}{2C_{dc}V_{dc0}^2} s + \frac{3v_{td0}k_i}{2C_{dc}V_{dc0}} \right)} \quad (89)$$

The PI gains are calculated by pole placement like the previous sections based on the target rise time and damping of the response.

$$k_p = \frac{4\zeta\omega_n C_{dc}V_{dc0}^2 + 2P_{inv0}}{3V_{dc0}v_{td0}} \quad (90)$$

$$k_i = \frac{2\omega_n^2 C_{dc}V_{dc0}}{3v_{td0}} \quad (91)$$

The zero in (89) causes significant overshoot and a decrease in the rise time of the DC voltage response for smaller values of DC link capacitance. To increase the modularity of the model prototype and keep the tuning simple, the PI controller is implemented based on setpoint weighting of the proportional gain. Appendix C provides further details on this approach. Table 3-III shows the resulting PI controller gains for a variety of DC link capacitance values. Also included is the weighting factor,  $b$ , for the proportional gain acting on the reference setpoint. The implemented controller in the model prototype is shown in Figure 3-36. Note, setting  $b = 1$  results in the same structure as shown in Figure 3-35.

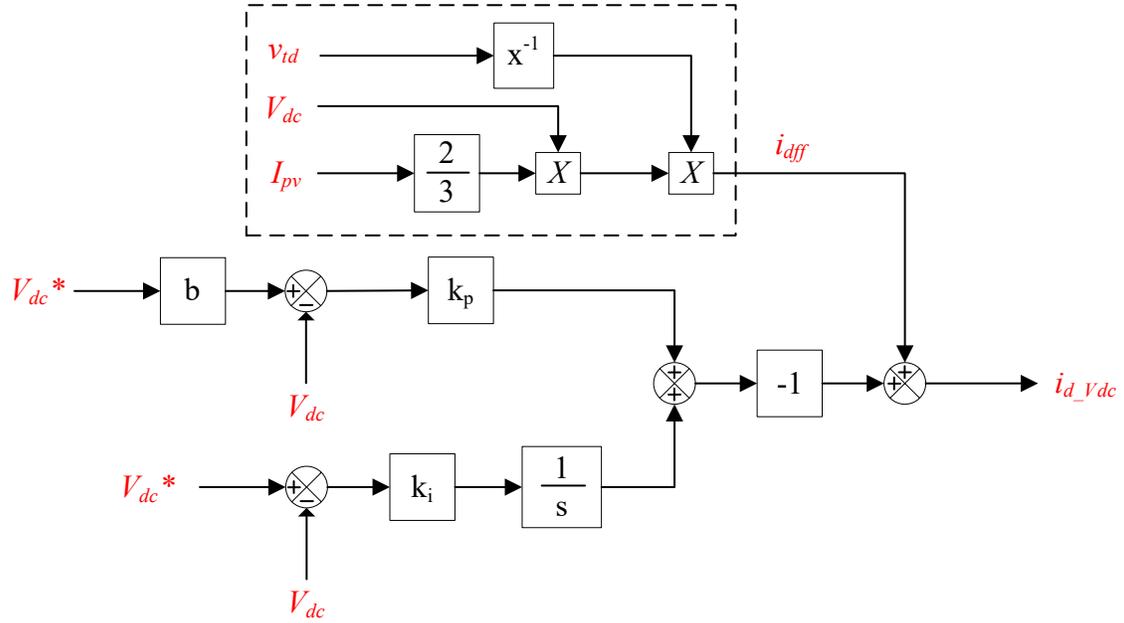


Figure 3-36. Control block diagram of the Vdc controller with setpoint weighting of the proportional gain.

Table 3-III: DC link Voltage Controller PI Gains

Parameter	$C_{dc} = 1 F$	$C_{dc} = 0.1 F$	$C_{dc} = 0.05 F$	$C_{dc} = 0.01 F$
$t_r$ (target)	100 ms	100 ms	100 ms	100 ms
$f_{BW} \sim 0.35/t_r$	3.5 Hz	3.5 Hz	3.5 Hz	3.5 Hz
Damping ratio $\zeta$	0.707	0.707	0.707	0.707
$v_{td0} = v_{dqbase}$	489.9 V	489.9 V	489.9 V	489.9 V
$V_{dc0}$	1200.0 V	1200.0 V	1200.0 V	1200.0 V
$P_{inv0}$	0.9 MW	0.9 MW	0.9 MW	0.9 MW
$k_p$	42.6	5.18	3.1	1.44
$k_i$	529.1	52.91	26.45	5.3
$b$	0.69	0.56	0.474	0.205

Figure 3-37 shows the step response of the DC voltage control corresponding to the gains and DC link capacitor size in Table 3-III. The top chart shows that as the value of the DC link capacitor decreases, the zero's impact is increased. The bottom chart shows that with the setpoint weighting applied, the response is consistent. The influence of the setpoint weighting is also evident in Table 3-III by comparing the calculated values of  $b$  to maintain the zero at  $s = -\omega_n$ .

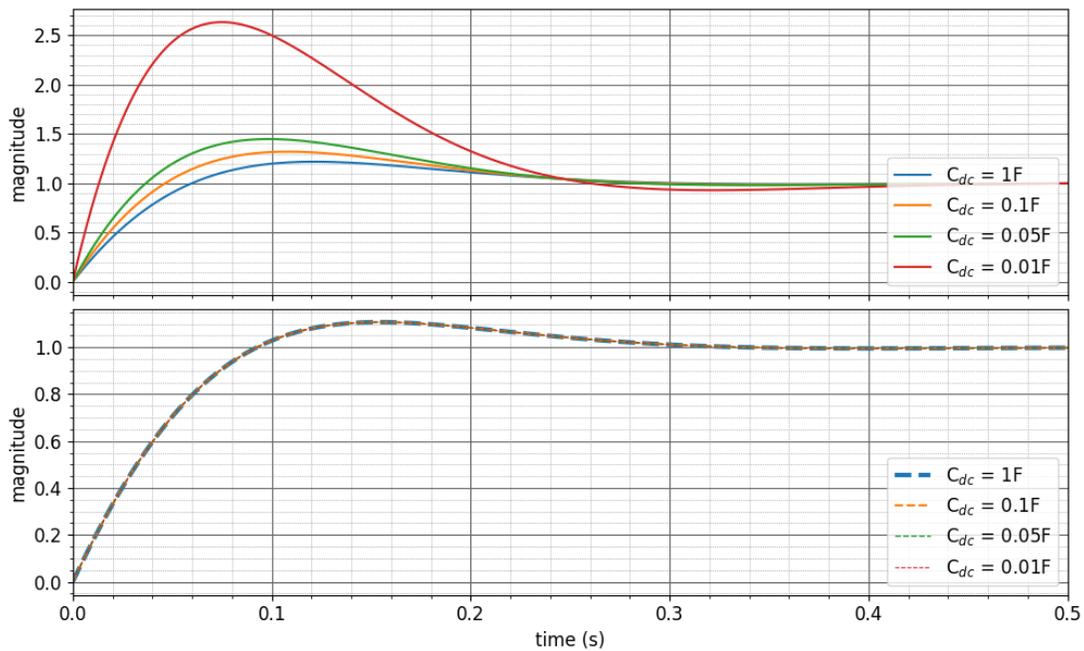


Figure 3-37. Step response of the DC voltage without setpoint weighting (top chart) and with setpoint weighting (bottom chart).

The DC voltage response is tested in the model prototype for a 5% step change in  $V_{dc}^*$ . Three DC link capacitor values are considered. The PI gains and the setpoint weighting gains for the proportional control are as shown in Table 3-III. The response in the full model prototype shown in Figure 3-38 is consistent with the linearized small-signal model except for the case where the DC link capacitor is 1.0F. In this case, the DC voltage response is a ramp due to the amplitude limiter. The current amplitude limiter is further described in Section 3.5.5. The current limit is also

used as the saturation value to prevent excessive integral windup in this controller. The integrator anti-windup method implemented in this work is detailed in Appendix C.

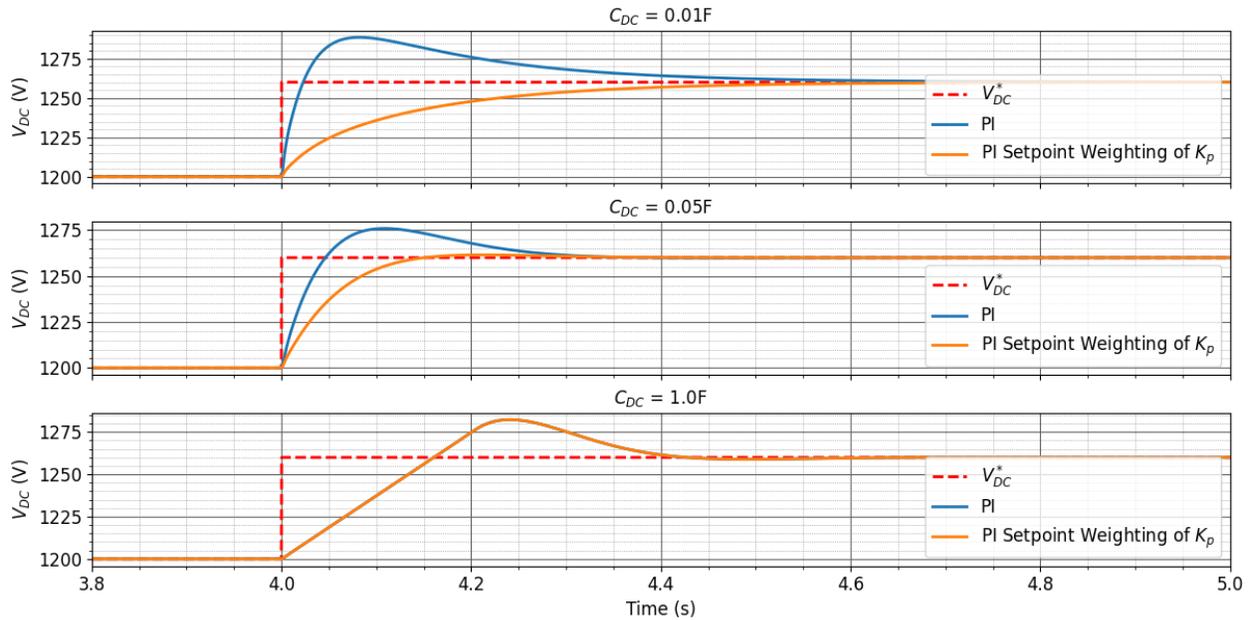


Figure 3-38. Step response of the DC link voltage comparing the PI controller implementation (blue trace) to the PI controller implementation with setpoint weighting of the proportional gain (orange trace). DC link capacitor values of 0.01F (top chart), 0.05F (middle chart), and 1.0F (bottom chart).

### 3.5.2.2. Frequency - Droop Control

A frequency - droop controller is implemented using the structure in the 2<sup>nd</sup> generation renewable energy positive sequence transient stability plant controller model, ‘repc\_\*

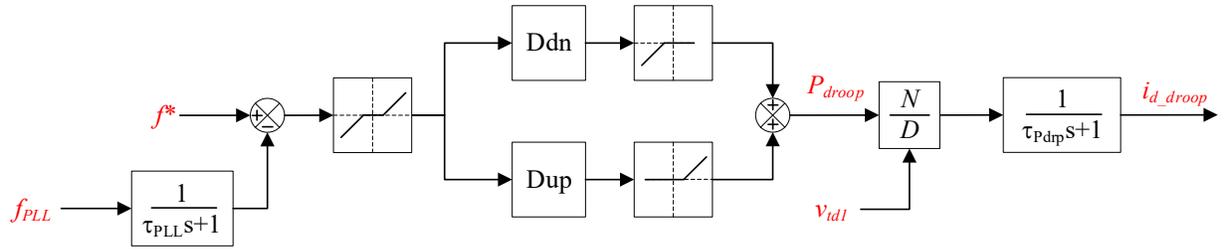


Figure 3-39. Frequency-droop controller block diagram.

A key parameter in the frequency-droop controller is the time constant of the LPF of the PLL frequency. As discussed in Section 3.3, the objective of the PLL is to track the phase angle of the space vector of the grid voltage. In steady-state, the PLL frequency matches the grid frequency. When the PLL is not locked, it is either speeding up or slowing down the rotation of the d-axis based on the error signal,  $v_{tq}$ . This is reflected in the PLL frequency,  $\omega_{PLL}$ , as shown in the response of the PLL in Figure 3-14. It follows that this signal must be filtered if used to represent the grid frequency in the frequency – droop control or in protection functions. The default setting of the LPF time constant in the model prototype is  $\tau_{PLL} = 100ms$ . This is consistent with the recommendations in [13].

Figure 3-40 and Figure 3-41 show the response of the inverter for a step change in the frequency of the grid equivalent voltage source. The inverter is assumed to have headroom and the frequency droop control is set as shown in Table 3-IV. For the high frequency case, the test voltage source frequency was changed to 60.1Hz at  $t = 4s$ . For the low frequency case, the test voltage source frequency was changed to 59.9Hz at  $t = 4s$ . The responses show that the inverter-level control determines the frequency and provides the target droop response. In both cases, an ideal voltage supplies the input DC power in the simulation.

Table 3-IV. Configuration of the Frequency Droop Controller

Parameter	Setting
Deadband (fdb)	$\pm 0.0006$ pu (0.36 mHz)
Droop gain for high frequency (Ddn)	20.0 (5% droop)
Droop gain for low frequency (Dup)	20.0 (5% droop)
1st order filter time constant of the PLL frequency ( $\tau_{PLL}$ )	0.1 s
1st order filter time constant of the output current reference signal ( $\tau_{Pdroop}$ )	0.001 s

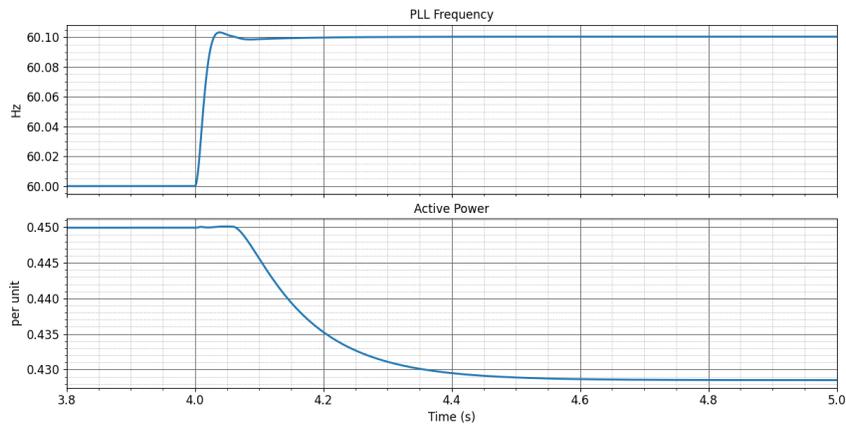


Figure 3-40. Frequency - droop response to high frequency.

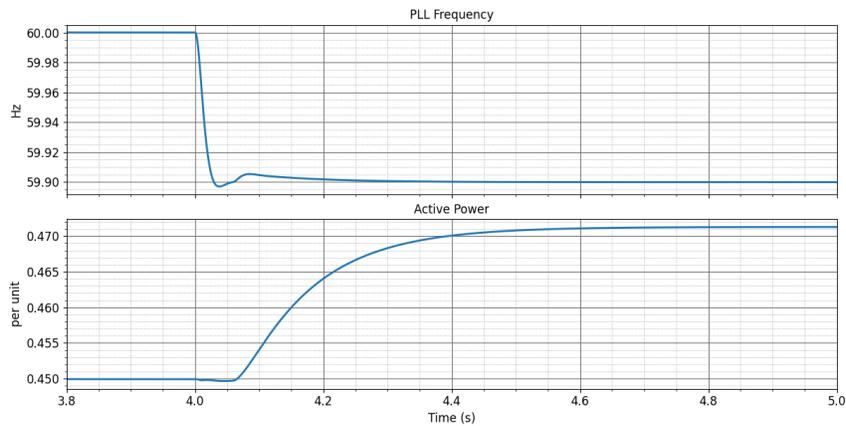


Figure 3-41. Frequency - droop response to low frequency.

### 3.5.2.3. Active Power Setpoint

In this control mode, the inverter follows an active power reference setpoint from the plant-level controller. The open loop implementation shown in Figure 3-42 is based on (81). The closed-loop implementation shown in Figure 3-43 is also implemented in the model prototype.

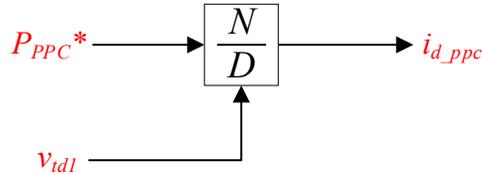


Figure 3-42. Open loop active power setpoint control block diagram in per unit.

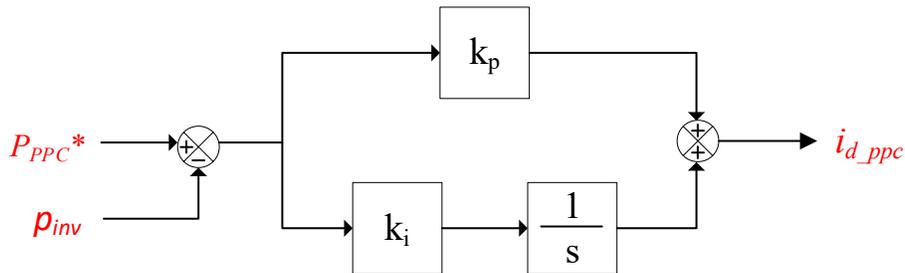


Figure 3-43. Closed-loop active power setpoint control block diagram.

### 3.5.2.4. D-Axis Current Reference Control Mode Selection

For the active power control detailed in this section, the controller's output is the d-axis current reference. The control mode is selected in the model prototype by the appropriate setting of the control flags in Table 3-V. Figure 3-44 shows the flags used to set the desired control mode and the resulting d-axis current reference. The sample and hold block is part of the HVRT/LVRT logic discussed in Section 3.5.4. Setting this flag to a logical 1 results in the d1-axis current reference freezing during LVRT and HVRT.

Table 3-V. Control Flag Description for Active Power Control.

Flag	Description
Vdc_flg	1: sets the control mode to regulate the DC link voltage 0: Pref setpoint and assumes constant DC link voltage (voltage source enabled on DC link)
f_flg	1: enables inverter-level frequency droop control 0: disables inverter-level frequency droop control
idfrz_flg	1: holds the last setpoint if the inverter is in LVRT or HVRT control mode 0: continues updating the d-axis current reference in LVRT or HVRT control mode

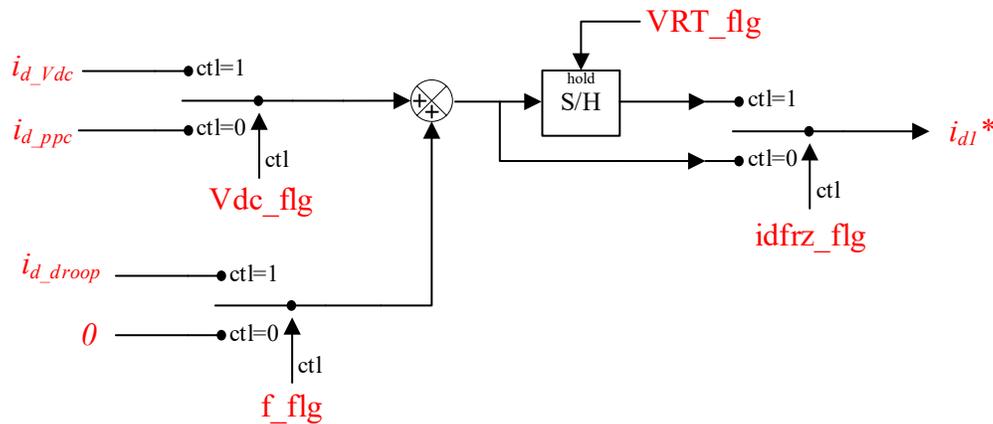


Figure 3-44. Selection of d1-axis current reference in the continuous operating range.

### 3.5.2.5. DC Input Power from PV

The dynamics of the DC input power from the PPS will depend on the resource type and control objective. Considering PV, the DC input power from the PV arrays depends on the PV array's design, solar irradiance, temperature, and operating point on the PV array's V-I curve. The operating point is controlled by an MPPT algorithm that determines the maximum power operating point on the PV array's V-I curve for the present condition. In a single-stage design shown in

Figure 3-45, the inverter control includes the MPPT which sets the DC link voltage reference to the DC link voltage controller. In a two-stage design shown in Figure 3-46, a DC-DC converter is added to the DC circuit that controls the voltage across the PV array,  $V_{pv}$ . In this case, the DC link voltage controller reference,  $V_{DC}^*$ , is constant. Reference [30] indicates that the single-stage design is more cost-effective for central inverters and large string inverters. A sampling of MW-scale PV inverter datasheets indicates that the single-stage design is typical for commercially available MW-scale PV inverters [63-65]. Therefore, the model prototype assumes a single-stage design.

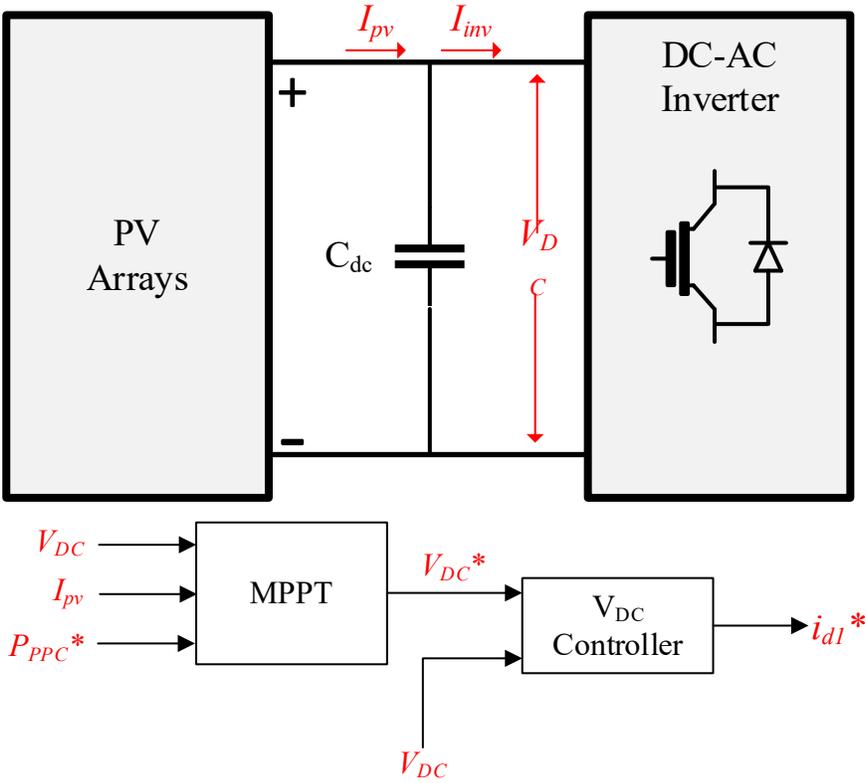


Figure 3-45. Diagram of a single-stage PV system design.

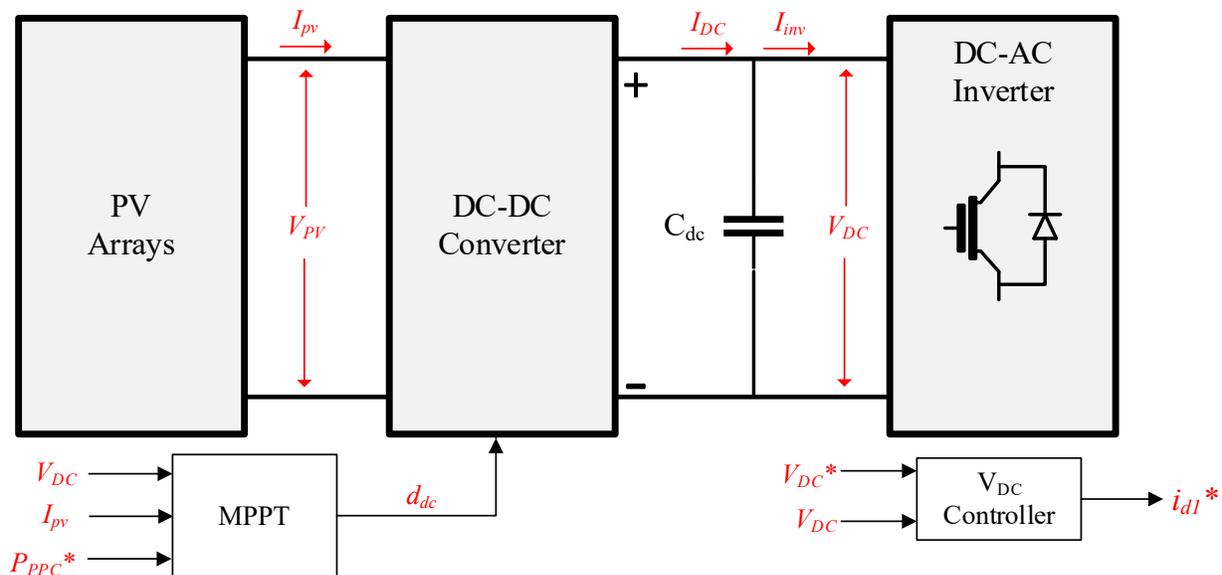


Figure 3-46. Diagram of a two-stage PV system design.

The DC input power from the PPS in Figure 3-2 is modeled in three ways in the model prototype and is selectable by the end-user. This includes:

- Constant current
- Generic PV array model
- Generic PV array model and generic MPPT control block

Figure 3-47 shows a diagram of how the model of the DC input power is implemented and the associated control flags in the model prototype. The constant current model is implemented as a controlled current source based on the active power reference setpoint,  $P_{PPC}^*$ , and the rated DC voltage. Many EMT simulators (e.g., PSCAD™, EMTP®, MATLAB Simscape™) include a PV array model and an MPPT controller as part of their model library. The model prototype utilizes the generic PV array block to model the V-I characteristics of a PV array based on the DC link voltage. In addition, a generic MPPT control block from the EMT simulator's model library is added to provide the DC link voltage reference if the impacts of the MPPT are of interest. The

selection of the DC input modeling approach is achieved via the setting of control flags shown in Table 3-VI.

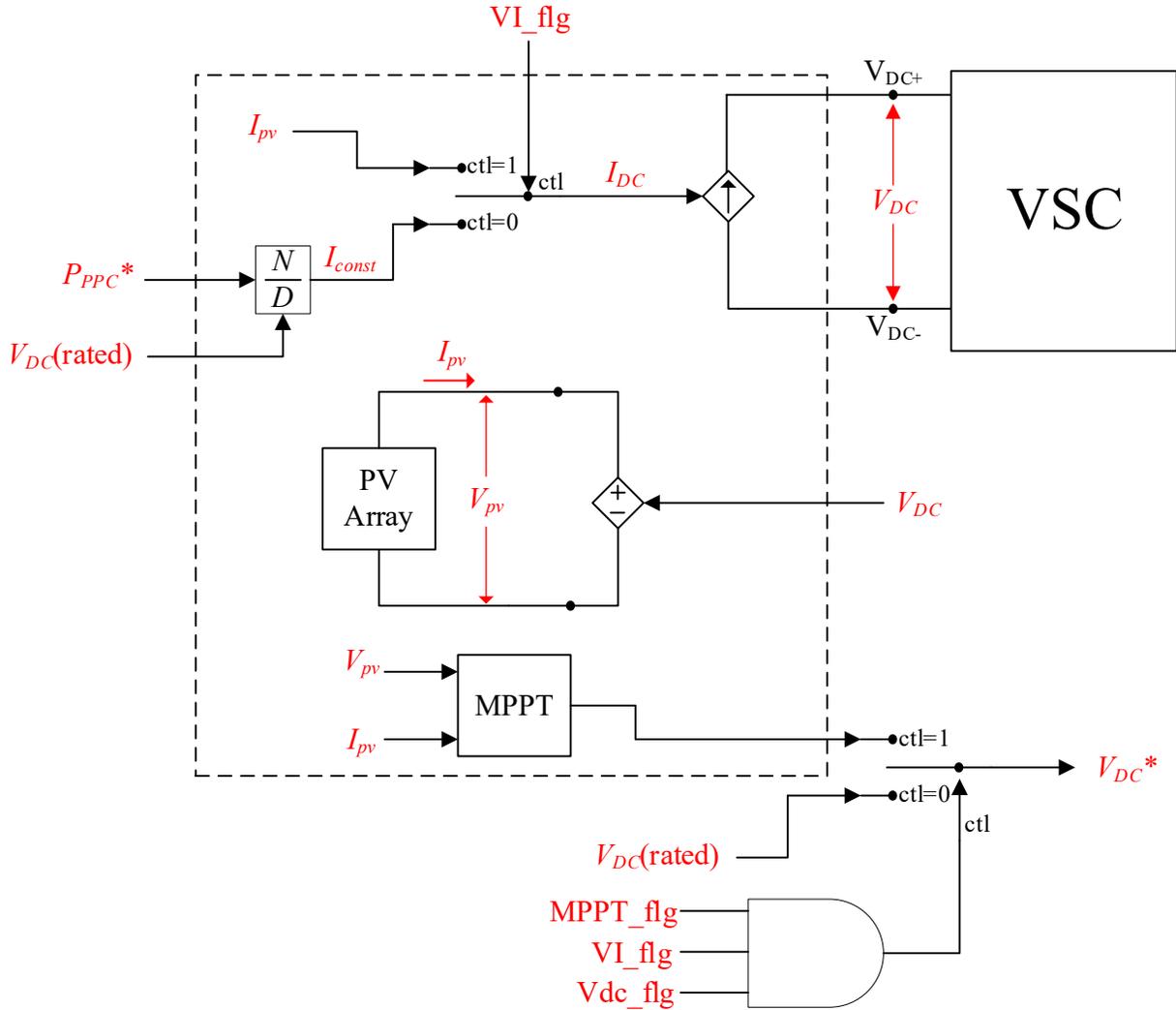


Figure 3-47. Block diagram of the PPS model.

Table 3-VI. Control flag settings for DC input power.

DC Input Power Mode	Control Flag Settings
Constant current	$VI\_flg = 0$
PV array	$VI\_flg = 1$ $MPPT\_flg = 0$

	MPPT_flg = 1
PV array w/ MPPT control	VI_flg = 1
	Vdc_flg = 1

---

Given the modularity of the model prototype, the modeling of the input power dynamics from the PPS can be readily extended. For example, more complex MPPT algorithms, a DC-DC converter to model a two-stage design, and/or a DC-DC converter to model DC coupled batteries. The constant current input is used if the DC input power dynamics are not of interest or details of the PPS are unknown.

#### **3.5.2.6. Summary**

This section presents the inverter-level active power control implemented in the model prototype. The dynamic model of the DC link voltage is derived and a small-signal model is developed. A PI controller with setpoint weighting on the proportional gain is applied as the DC link voltage controller. An analytical tuning approach based on pole placement is presented to tune the DC link voltage controller. Other control approaches implemented in the active power loop, including frequency-droop control and active-power reference setpoint from the plant controller, are shown. The variety of DC configurations that impact the dynamics of the DC input power from the PPS is briefly discussed, along with the DC input power models included in the model prototype.

#### **3.5.3. Reactive Power Control in the Continuous Operating Region**

The default reactive power – voltage control strategy for transmission connected IBR in IEEE P2800 is closed-loop plant level voltage control. The plant controller develops the reference

setpoints for the inverter outer loop control to regulate the plant-level voltage. The reactive power or voltage references are transmitted to the inverters, as shown in Figure 3-1. Based on (82), the inverter’s reactive power exchange with the grid can be controlled by the q-axis current. The closed-loop plant level voltage control response specifications in Draft 6.1 of IEEE P2800 require a reaction time of < 200ms and indicate the step response time is typically in the range of 1s to 30s [25].

### 3.5.3.1. Reactive Power Setpoint

In the reactive power setpoint control mode, the inverter follows a reactive power reference setpoint from the plant controller. The reactive power control at the inverter level can be controlled in open loop based on (82) as shown in Figure 3-48 or in closed-loop at the inverter level as shown in Figure 3-49. The signals in both control loops are in per unit.

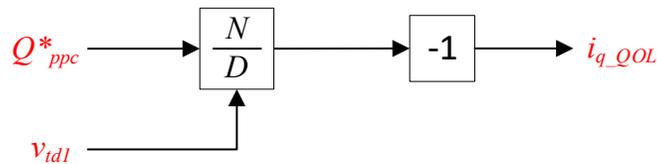


Figure 3-48. Control block diagram of the inverter open loop reactive power setpoint control in per unit.

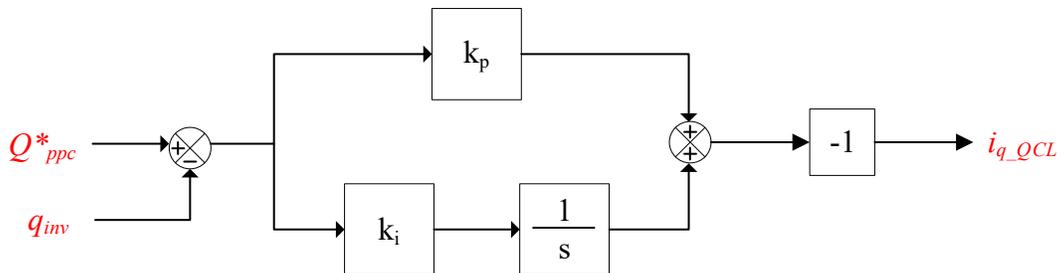


Figure 3-49. Control block diagram of the inverter closed-loop reactive power setpoint control.

### 3.5.3.2. Inverter-Level Terminal Voltage Control

This section describes the inverter level closed-loop terminal voltage controller implemented in the model prototype. The input to this controller is the terminal voltage reference setpoint which can be a static setpoint or provided by another control loop such as the plant controller.

#### 3.5.3.2.1. Inverter AC Terminal Voltage Model

The inverter terminal voltage in Figure 3-2 is described by:

$$\mathbf{v}_t = R_g \mathbf{i} + L_g \frac{d}{dt} \mathbf{i} + \mathbf{v}_g \quad (92)$$

Converting to the SRF results in the d-axis and q-axis voltage components:

$$v_{td} = R_g i_d + L_g \frac{di_d}{dt} - L_g \frac{d\theta_{PLL}}{dt} i_q + v_{gd} \quad (93)$$

$$v_{tq} = R_g i_q + L_g \frac{di_q}{dt} + L_g \frac{d\theta_{PLL}}{dt} i_d + v_{gq} \quad (94)$$

If the PLL is locked to the space vector of the grid voltage,  $v_{tq} = 0$ . Therefore, the control of the inverter AC terminal voltage in the SRF is implemented by controlling  $v_{td}$ . The small-signal model of the inverter terminal voltage in the SRF shown in Figure 3-50 is given as:

$$\Delta v_{td} = \Delta i_d R_g - L_g (\Delta i_q \omega_{PLL0} + i_{q0} \Delta \omega_{PLL}) + \Delta v_{gd} \quad (95)$$

$$\Delta v_{tq} = \Delta i_q R_g + L_g (\Delta i_d \omega_{PLL0} + i_{d0} \Delta \omega_{PLL}) + \Delta v_{gq} \quad (96)$$

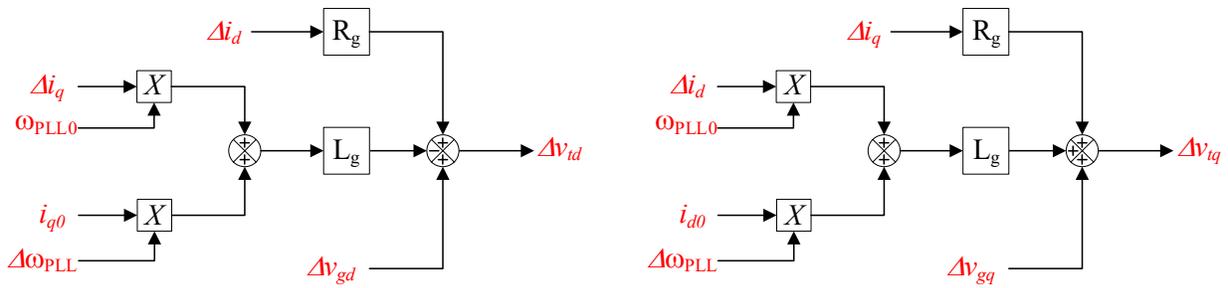


Figure 3-50. Block diagram of the small-signal model of the SRF components of the inverter terminal voltage.

Figure 3-51 shows the voltage components as a vector diagram. This diagram shows an example where the q-axis current is negative and the d-axis current is positive.

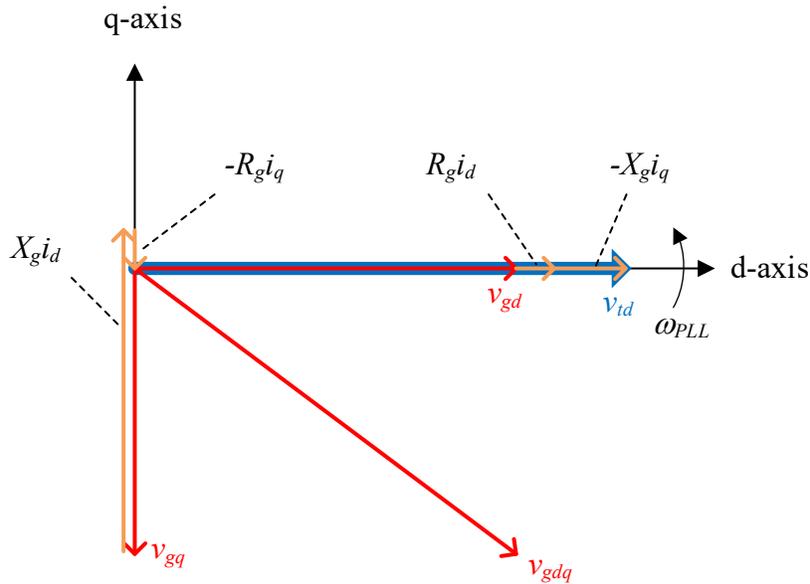


Figure 3-51. Vector diagram of the terminal voltage SRF current components in steady-state.

For transmission systems, the X/R ratio is typically high enough such that the  $R_g i_d$  can be ignored. For distribution systems, the X/R ratio is typically lower and the  $R_g i_d$  term may need to be considered. Given that this work focuses on inverters applied in transmission-connected IBR plants, the terminal voltage control is accomplished via the q-axis current. The transfer function of the q-axis current to the d-axis voltage is determined by setting all other perturbation variables to

zero. This is simply a gain with a magnitude equal to the grid reactive impedance, as shown in Figure 3-51. The negative sign is due to the assumed orientation of the q-axis leading the d-axis.

$$\frac{\Delta v_{td}}{\Delta i_q} = -\omega_{PLL0} L_g = -X_g \quad (97)$$

### 3.5.3.2.2. Inverter AC Terminal Voltage Controller

The voltage controller is implemented with a PI compensator as shown in Figure 3-52. The closed-loop current control is approximated as a 1<sup>st</sup> order LPF for simplicity given the separation in the bandwidth of the voltage controller and the current controller. The closed-loop transfer function of the voltage controller is given by:

$$\frac{\Delta v_{td}(s)}{\Delta v_{td}^*(s)} = \frac{X_g(k_p s + k_i)}{s^2 \tau_{cc} + (X_g k_p + 1)s + X_g k_i} \quad (98)$$

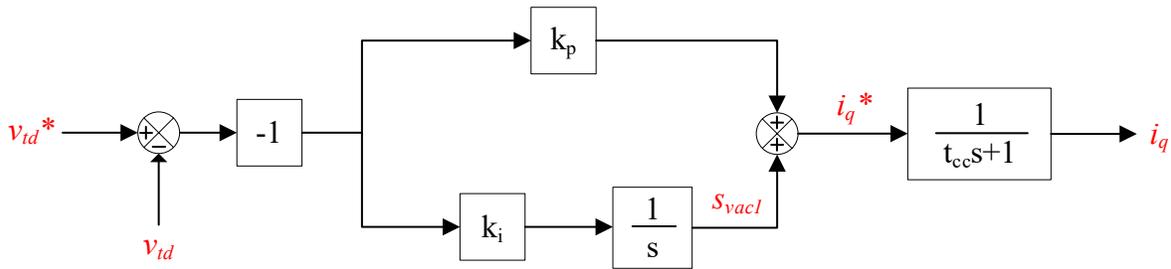


Figure 3-52. Block diagram of the inverter-level AC voltage controller.

If we assume the closed-loop current controller bandwidth is an order of magnitude larger than the target closed-loop bandwidth of the voltage controller, (98) can be further simplified to:

$$\frac{\Delta v_{td}(s)}{\Delta v_{td}^*(s)} = \frac{X_g(k_p s + k_i)}{(X_g k_p + 1)s + X_g k_i} \quad (99)$$

Using these approximations implies that the simplified model is only valid for frequencies less than the current control closed-loop bandwidth.

Pole placement is used to tune the gains of the PI controller. Noting the characteristic equation of (99) is of order one, we can only place one pole. Setting  $k_p = 0$  results in the following transfer function.

$$\frac{\Delta v_{td}(s)}{\Delta v_{td}^*(s)} = \frac{X_g k_i}{s + X_g k_i} = \frac{1}{\frac{1}{X_g k_i} s + 1} = \frac{1}{\tau_{vtd} s + 1} \quad (100)$$

Thus,  $k_i$  can be set based on the target time constant of the voltage response.

$$k_i = \frac{1}{X_g \tau_{vtd}} \quad (101)$$

Table 3-VII provides calculations for the PI gains based on the target first-order time constant of the voltage response and the SCR at the connection point. SCR is a metric commonly used to describe system strength at the connection point of an IBR relative to the size of the IBR. In its simplest form, the SCR is the inverse of the Thevenin equivalent impedance in per unit with  $S_{base} = S_{inv}$ . The interested reader is referred to [66] for a detailed discussion on system strength and various approaches to calculate SCR.

$$SCR = \frac{\sqrt{3} V_{LL} I_{3\phi fault}}{S_{inv}} = \frac{SC_{MVA}}{S_{inv}} = \frac{V_{LL}^2}{Z_{th} S_{inv}} = \frac{Z_{base}}{Z_{th}} \quad (102)$$

Table 3-VII: Inverter Terminal Voltage Controller PI Gains

Parameter	Value	Value	Value	Value
$\tau_{vtd}$ (target)	50ms	20ms	10ms	10ms
SCR	5	5	5	2
$k_p$	0	0	0	0
$k_i$	100	250	500	200

To verify the response predicted by the analytical small-signal model, a 5% step change is applied to the inverter terminal d-axis voltage reference. Figure 3-53 shows the closed-loop step response for an SCR of 5 and the corresponding PI gains listed in Table 3-VII. For the target first-order time constant of 50ms and 20ms, the model prototype response is as predicted by the analytical model. For the target first-order time constant of 10ms, the response contains approximately 5% overshoot. This response is acceptable, but more interestingly, it highlights the coupling of a step change in  $v_{td}^*$  to the q-axis voltage and the PLL. Figure 3-54 compares the voltage for an SCR = 5 and an SCR = 2 with a target first-order time constant of 10ms. The PI gains are set based on Table 3-VII to have the same first-order response. With decreasing SCR, i.e., increased grid reactive impedance  $X_g$ , the variation in  $v_{tq}$  and  $f_{PLL}$  is more pronounced. Referring to (94), this may be related to the  $L_g \frac{di_q}{dt}$  component of  $v_{tq}$  since the influence is increased with the faster response and the increased grid inductance,  $L_g$ . Any change in  $v_{tq}$  causes the PLL frequency to change based on the SRF-PLL dynamics described by (61) and (62). This shows the impact of increased grid impedance, which is the basis for the weak grid problem.

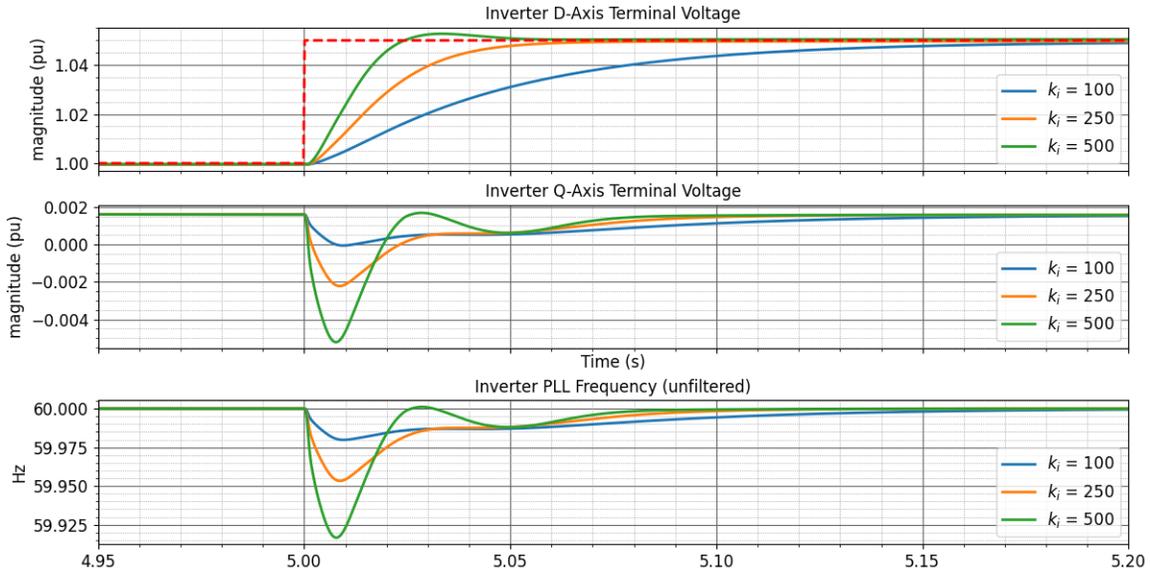


Figure 3-53. Step response of the d-axis voltage (top), q-axis voltage (middle), and PLL frequency (bottom) for a 5% step change in  $v_{td}^*$  for varying values of  $k_i$  in the model prototype for an SCR of 5.

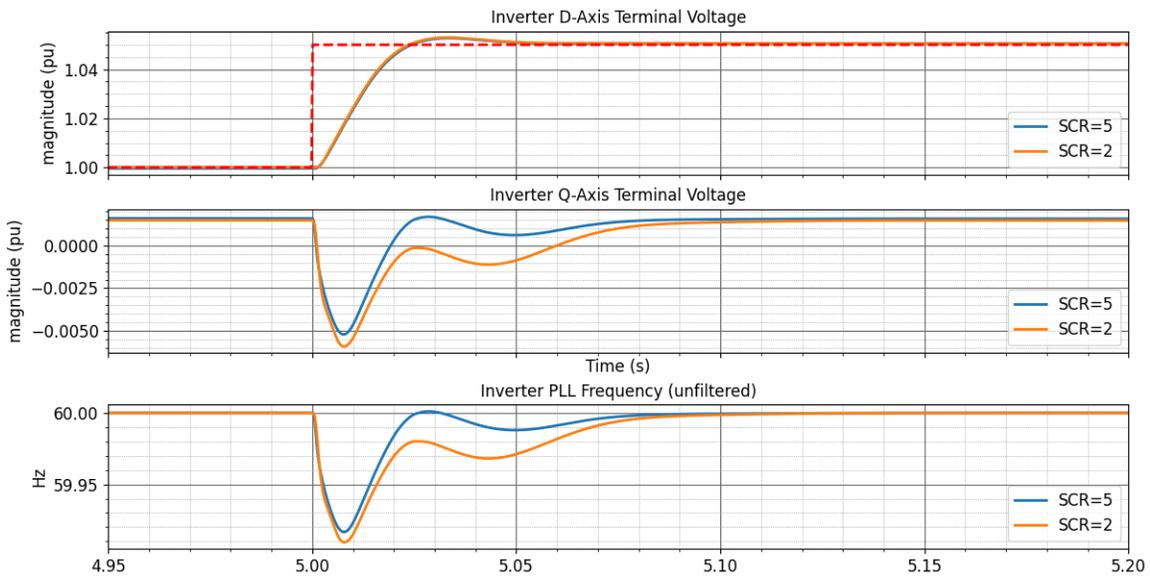


Figure 3-54. Step response of the d-axis voltage (top), q-axis voltage (middle), and PLL frequency (bottom) for a 5% step change in  $v_{td}^*$  for SCR = 5 (blue trace) and SCR = 2 (orange trace) in the model prototype.

Note that this tuning approach is reliant on knowledge of the grid reactive impedance,  $X_g$ . The grid impedance is time-varying. For example, the impedance is influenced by the transmission network configuration and the synchronous machines in-service. Figure 3-55 shows the step

response of the inverter AC terminal voltage control varying the grid impedance,  $X_g$ . As the grid impedance is increased, the step response rise time decreases for the same PI compensator gains. If other active devices are electrically close, their influence on the impedance across a wide frequency range must be considered. Care must be taken to understand the range of expected grid impedances such that the control is appropriately tuned.

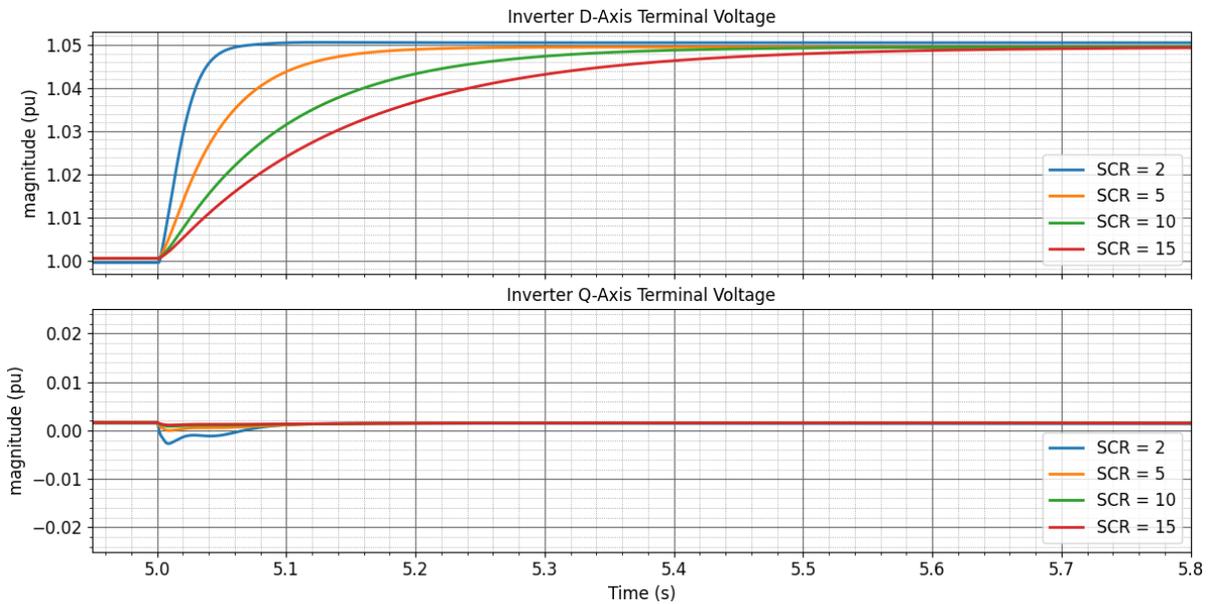


Figure 3-55. Step response of the d-axis voltage (top) and q-axis voltage (bottom) for a 5% step change in  $v_{td}^*$  varying the SCR in the model prototype.

### 3.5.3.3. Q-Axis Current Reference Control Mode Selection

For the reactive power – voltage control detailed in this section, the output of the controller is the q-axis current reference. The control mode is selected in the model prototype by the appropriate setting of the control flags in Table 3-VIII. Figure 3-56 shows the flags used to set the desired control mode and the resulting q-axis current reference. The sample and hold block is part of the HVRT/LVRT logic discussed in Section 3.5.4.

Table 3-VIII. Control Flag Description for Reactive Power Control.

Flag	Description
Vt_flg	1: enables closed-loop Vref setpoint control 0: disables closed-loop Vref setpoint control
Qctl_CL_flg	1: enables closed-loop Qref setpoint control 0: enables open loop Qref setpoint control

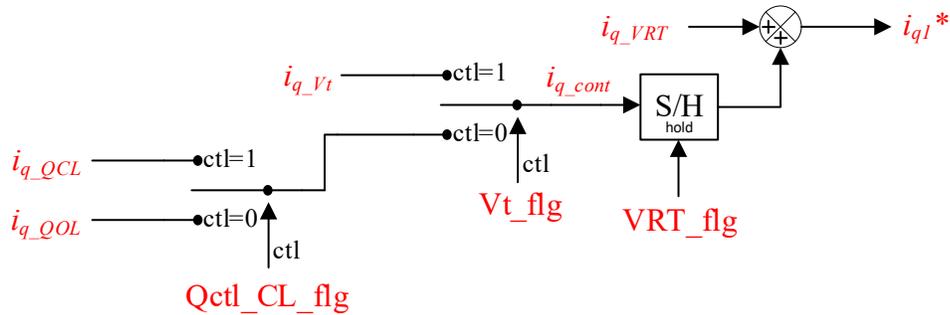


Figure 3-56. Selection of q-axis current reference in the continuous operating range.

### 3.5.3.4. Summary

This section details the inverter-level reactive power - voltage control in the continuous operating range implemented in the model prototype. The model prototype can regulate the reactive power reference setpoint in open loop or closed-loop. An inverter level closed-loop voltage controller is also implemented. A model of the AC terminal voltage and the voltage controller is developed and linearized. An analytical tuning approach based on pole-placement is presented to tune the AC voltage controller. Examples are presented that show the impact of the grid strength on the response of the voltage controller. Finally, the control flags that select the control mode of the inverter are presented.

### 3.5.4. Fault Ride-Through Control Mode

Thus far, this section has presented the outer loop control of the inverter during normal operation when the AC terminal voltage is within the inverter’s continuous operating range. One of the main objectives of this work is to develop an inverter model that can emulate the required response of the inverter during system faults. A typical control approach for IBR is for the inverter control to autonomously control the inverter during abnormal conditions based on the measured terminal voltage. This enables a much faster response of the inverter and collectively the IBR to support grid stability. Therefore, the inverter control in this work has two distinct control modes: continuous and fault ride-through (FRT). If the grid voltage goes outside of the continuous operating range, the inverter switches to the FRT control mode. The FRT control in this section is designed to meet the performance capability requirements in draft 6.1 of IEEE P2800 [25]. The German (VDE) [26, 27] and Spanish (NTS) [28] application of the European Grid Code [29] are also used as references as the performance requirements provide more specificity. The primary focus of this section is on low voltage ride-through (LVRT) due to faults on the electric grid. A summary of the LVRT performance response requirements considered in the generic model control development of this work is shown in Table 3-IX.

Table 3-IX: Grid Code FRT Response Performance Requirements

Parameter	IEEE P2800 D6.1 [25]	VDE 4120/30 [26, 27]	NTS [28]
Incremental positive sequence reactive current, $\Delta I_{R1}$	Dependent on $V_1$	$\Delta I_{1R} =  \Delta V_1 k_1$	$\Delta I_{1R} =  \Delta V_1 k_1$
Incremental negative sequence reactive current, $\Delta I_{R2}$	Dependent on $V_2$	$\Delta I_{2R} =  \Delta V_2 k_2$	$\Delta I_{2R} =  \Delta V_2 k_2$

Phase angle of $\mathbf{I}_2$ with respect to $\mathbf{V}_2$	Leads $\angle \mathbf{V}_2$ by $90^\circ$ to $100^\circ$	Leads $\angle \mathbf{V}_2$ by $90^\circ$	Leads $\angle \mathbf{V}_2$ by $90^\circ$
Step response time: $t_r$	$\leq 2.5$ cycles <sup>a</sup> [41.67 ms at 60Hz]	$\leq 30$ ms	$\leq 50$ ms
Settling time: $t_s$	$\leq 4.0$ cycles <sup>a</sup> [66.67 ms at 60Hz]	$\leq 60$ ms	$\leq 80$ ms
Default current priority	Reactive	Reactive	Reactive
Default current priority for asymmetrical fault	$\Delta i_{r1} \geq \Delta i_{r2}$ with preference of equal reduction of $\Delta i_{r1}$ and $\Delta i_{r2}$ .	Preference: uniform reduction of $i_{r1}$ and $i_{r2}$ .	Reduction of $\Delta i_{r1}$ and $\Delta i_{r2}$ in equal proportion

<sup>a</sup> Evaluated based on phasor quantities with 1-cycle moving average window.

Given that the required response times are on the order of a few periods of the fundamental frequency and the parameters are in terms of phasor quantities, one interesting question is, how is satisfactory performance determined? The authors in [67] show how the evaluation of the time-domain specification is influenced by the calculation method and propose a 1-cycle window positive sequence calculation. Draft 6.1 of IEEE P2800 specifies that a DFT applied to a moving 1-cycle of the fundamental window is used to calculate the sequence components of the active and reactive currents. The effect of the window length is included in the response time requirements meaning that the response of the instantaneous signals will be faster than the phasor domain specifications in IEEE P2800.

The inverter LVRT and HVRT control is designed to meet the performance response requirements in Table 3-IX. The VRT performance response includes requirements for positive sequence and negative sequence voltage deviations at the inverter AC terminal. The VDE and the NTS LVRT and HVRT performance requirements contain more specificity than IEEE P2800

regarding the magnitude of the current response for a given voltage deviation. The additional reactive current injection required is proportional to the voltage deviation at the inverter terminal. The proportional gain is in units of pu/pu and is configurable. The VDE requires this gain to be configurable in the range of 2.0 to 6.0. These requirements are used as the basis for the VRT response control design.

#### 3.5.4.1. Positive Sequence Current Response

The positive sequence current reference during VRT is developed by closed-loop control of the positive sequence voltage at the inverter AC terminals. The compensator is a proportional gain,  $k_{qv1}$ , such that the inverter provides reactive current injection in proportion to the voltage deviation. The positive sequence voltage,  $v_{td1}$ , is determined by the DSOGI SRF-PLL or the DDSRF-PLL as described in Section 3.3.5.

Figure 3-57 shows the VRT control of the positive sequence voltage. The response is obtained by adding a control activated by the terminal voltage magnitude outside the continuous operating range. The default values defining the continuous operating range are 0.9 pu to 1.1 pu as default. If the terminal voltage is higher than a specified limit, 1.1 pu in this example, the HVRT flag is a logical 1. If the terminal voltage is lower than a specified value, 0.9 pu in this example, the LVRT flag is a logical 1. The VRT\_flg logic is shown in Figure 3-58. VRT\_flg is a logical 1 if either the HVRT or the LVRT flag is a logical 1. When the VRT control is activated (VRT\_flg = 1), the pre-disturbance current reference ( $i_{q1i} = i_{q\_cont}$ ) is held constant and added to the current reference developed by the positive sequence VRT control ( $i_{q1VRT}$ ) as shown in Figure 3-57. The following equations illustrate the positive sequence current reference during VRT in Figure 3-57.

$$i_{q1}^* = i_{q1i} + i_{q1VRT} \quad (103)$$

$$\Delta i_{q1} = v_{td1e} k_{qv1} \quad (104)$$

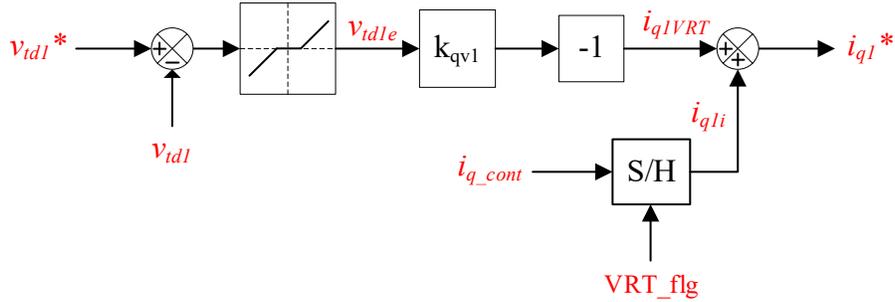


Figure 3-57. Block diagram of the positive sequence voltage control during VRT.

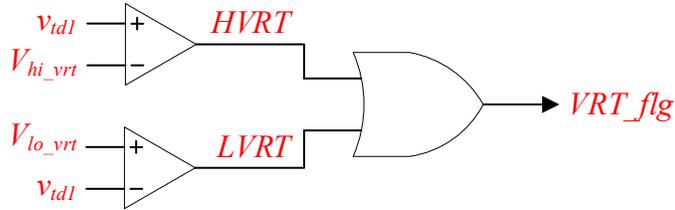


Figure 3-58. VRT control flag logic.

### 3.5.4.2. Negative Sequence Current Response

During asymmetrical grid faults, the grid voltage will contain a negative sequence component. The negative sequence current reference is developed by closed-loop control of the negative sequence voltage at the inverter AC terminals. The negative sequence voltage,  $v_{tdq2}$ , is determined by the DSOGI SRF-PLL or the DDSRF-PLL as described in Section 3.3.5. In Figure 3-21, the positive sequence SRF is aligned to the positive sequence component of the space vector of the grid voltage. The negative sequence SRF rotates in the opposite direction as the positive sequence SRF. The position of the d2 axis in the  $\alpha\beta$  plane at any instant in time is  $-\theta_{PLL}(t)$ . The negative sequence voltage may contain both d2-axis and q2-axis components based on how the negative

SRF is defined in this work. Thus, unlike the positive sequence control, the negative sequence control must consider both the d2 and the q2 components based on this control structure.

The negative sequence voltage controller in Figure 3-59 is developed based on the VDE-4120-2018 [27] requirement of additional reactive current in the negative sequence proportional to the voltage deviation. This approach meets the performance requirements in draft 6.1 of IEEE P2800, which is less specific than the VDE. Based on this control objective, the magnitude of the negative sequence voltage is used as the error signal input to a proportional gain,  $k_{qv2}$ . To ensure the negative sequence current phasor is purely reactive and leads the negative sequence voltage phasor, 90 degrees is subtracted from the phase of  $v_{tdq2}$ . Appendix G provides a derivation of the negative sequence control and the relationship between the negative SRF components and symmetrical components.

$$\mathbf{i}_{dq2}^* = |\mathbf{v}_{tdq2}| \angle [\angle(\mathbf{v}_{tdq2}) - 90^\circ] k_{qv2} \quad (105)$$

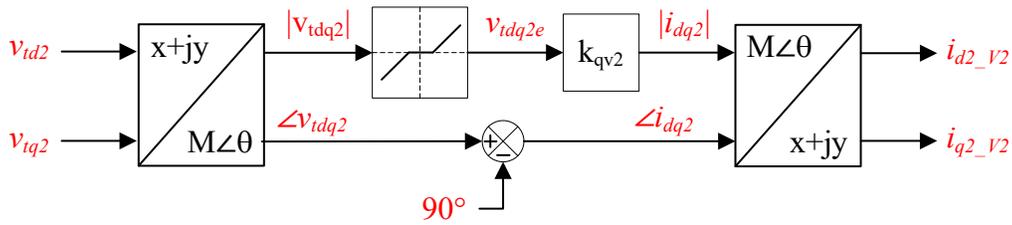


Figure 3-59. Block diagram of the negative sequence voltage control during VRT.

The VDE negative sequence current injection requirement is mathematically identical to the proposal in [68], which proposed negative sequence current injection for WTGs. The authors show that their proposed approach results in the WTG having a steady-state negative sequence impedance of  $j/k_{qv2}$ . However, as will be discussed in Section 3.5.5, the inverter current must be limited to protect the power electronic devices. Presently, the current limit is close to or potentially

the same as the steady-state current limit. This means that the impedance will only appear linear for a limited range. Figure 3-60 shows conceptually the influence the current limit of the inverter has on the apparent impedance. This is equally applicable to the positive sequence apparent impedance.

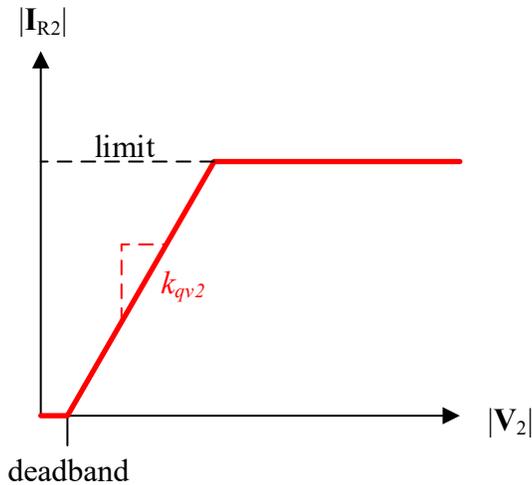


Figure 3-60. Effect of the current limit on the apparent negative sequence impedance.

The negative sequence voltage control can be disabled in the model prototype by setting the control flag  $V2\_flg$  to zero as shown in Figure 3-61. In this case, the control will regulate the negative sequence current to zero. This is commonly referred to as negative sequence current suppression. From Figure 3-59, if  $k_{qv2}$  is set to zero, this also results in negative sequence current suppression.

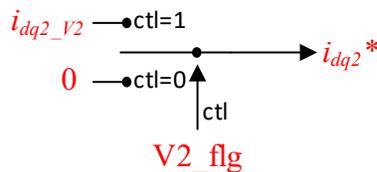


Figure 3-61. Control flag to enable V2 control.

### 3.5.5. Inverter Current Limit

The inverter control in the previous sections was developed without consideration of the current limit of the inverter. One of the advantages of using current mode control is that the output current is tightly regulated with a relatively fast time constant. When the voltage is less than nominal, the magnitude of the current must increase to maintain the desired active power and reactive power exchange with the grid, as evident in (81) and (82). The power electronic devices are sensitive to their thermal loading and junction temperature [69, 70]. Presently, commercial inverters have current limits that are approximately the same magnitude for continuous operation and for time durations on the order of normal clearing of grid faults (~50-500ms). The lack of temporary overload capability on timescales on the order of normally cleared grid faults is one major distinction between the response of inverters and synchronous machines.

For the inverter, the current must be limited such that the phase current does not exceed the maximum allowed current of the power electronic devices. Therefore, a priority must be established to determine the reference currents passed to the inner current controllers. The default in many grid codes, e.g., Table 3-IX, is to prioritize the reactive current during low voltage. Considering just positive sequence current injection, prioritizing the reactive current can be accomplished by:

$$\begin{aligned} i_{qmax} &= \pm I_{lim} \\ i_{dmax} &= \sqrt{I_{lim}^2 - i_{q1ref}^2} \end{aligned} \tag{106}$$

The current limit logic is further complicated with the inclusion of negative sequence current injection. The performance requirements in Table 3-IX specify if the current limit of the inverter

is reached, the priority is given to the reactive current. Further, if the combination of the positive and negative sequence reactive components of the desired current would cause the inverter to exceed its current rating, then the preference is a reduction of both components. In IEEE P2800, this is specified in terms of a uniform reduction in the incremental reactive current. In the VDE, this is specified in terms of the sequence components of the current. While similar, this would yield slightly different current components depending on the pre-disturbance reactive current. The current limit logic is developed based on these specifications to maintain the phase current within the limits of the converter.

The inverter is assumed to be a three-wire system which implies no zero-sequence component of the current. Considering the single line diagram in Figure 3-2, the inverter current can be decomposed into its positive and negative sequence components.

$$\mathbf{i}_{\alpha\beta} = \mathbf{i}_{\alpha\beta 1} + \mathbf{i}_{\alpha\beta 2} = |\mathbf{i}_{\alpha\beta 1}|e^{j(\omega t + \angle I_1)} + |\mathbf{i}_{\alpha\beta 2}|e^{-j(\omega t + \angle I_2)} \quad (107)$$

Figure 3-62 shows  $\mathbf{i}_{\alpha\beta}$  graphically as a superposition of the positive and negative sequence components in the  $\alpha\beta$  plane. The blue circle is the locus of the positive sequence component of the current space vector that rotates counterclockwise at the fundamental frequency. The negative sequence component of the current space vector rotates in the clockwise direction at the fundamental frequency. The resulting superposition of the current's positive and negative sequence components form the ellipse shown in green. The magnitude of  $\mathbf{i}_{\alpha\beta}$  is time varying if the signal contains both positive and negative sequence components. The maximum current in each phase of the inverter will be dependent on the magnitude and relative phase of the positive and negative sequence components. Note that Figure 3-62 is a snapshot in time when the two vectors are aligned, i.e.,  $\angle(\mathbf{i}_{\alpha\beta 1}) = \angle(\mathbf{i}_{\alpha\beta 2})$ .

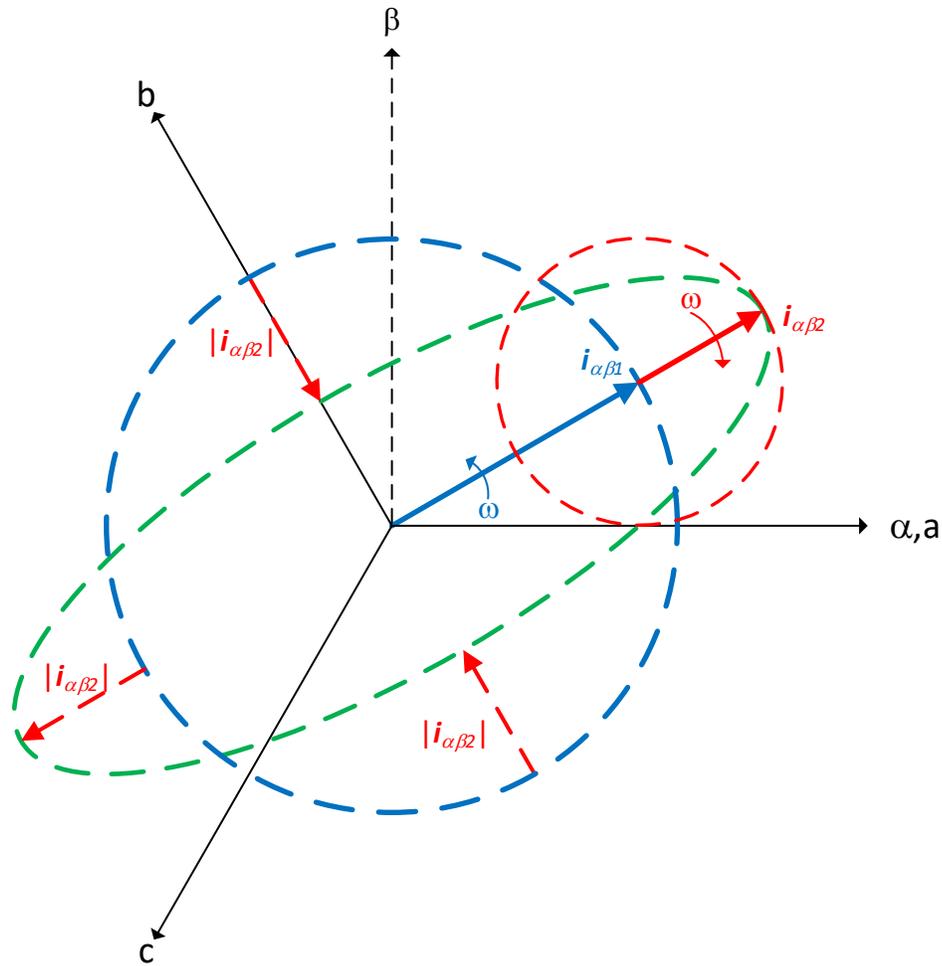


Figure 3-62. Graphical relationship of the positive and negative sequence components of the  $\alpha\beta$  current to the phase current peak magnitude.

### 3.5.5.1. Method 1

Method 1 of the current limit logic is implemented by comparing the maximum value of  $\mathbf{i}_{\alpha\beta}$  to the inverter's current limit. The vectors  $\mathbf{i}_{\alpha\beta 1}$  and  $\mathbf{i}_{\alpha\beta 2}$  will be aligned twice each period of the fundamental frequency. Thus, the maximum value of the space vector of the current is the addition of the magnitude of the positive and negative sequence components.

$$\max(\mathbf{i}_{\alpha\beta}) = |\mathbf{i}_{\alpha\beta 1}| + |\mathbf{i}_{\alpha\beta 2}| \quad (108)$$

The current references that were developed in the positive and negative sequence SRFs are transformed to the stationary reference frame.

$$\mathbf{i}_{\alpha\beta 1} = (i_{d1}^* + ji_{q1}^*)e^{j\theta_{PLL}} \quad (109)$$

$$\mathbf{i}_{\alpha\beta 2} = (i_{d2}^* + ji_{q2}^*)e^{-j\theta_{PLL}} \quad (110)$$

The superposition of the positive and negative sequence components gives the total current as a function of time.

$$\begin{aligned} \mathbf{i}_{\alpha\beta} &= \mathbf{i}_{\alpha\beta 1} + \mathbf{i}_{\alpha\beta 2} \\ &= |i_{d1}^* + ji_{q1}^*|(e^{j\theta_{PLL}})e^{j\theta_{PLL}} + |i_{d2}^* + ji_{q2}^*|(e^{j\theta_{PLL}})e^{-j\theta_{PLL}} \end{aligned} \quad (111)$$

The highest priority during FRT is given to the reactive components of the positive and negative sequence currents. Thus,  $i_{d1}^*$  is initially assumed to be 0 resulting in:

$$i_{\alpha\beta max} = |i_{q1}^*| + |i_{d2}^* + ji_{q2}^*| \quad (112)$$

The current limit logic checks if the maximum value of the space vector of the current in (112) is greater than the current limit of the inverter. If so, the current references are reduced such that the reduction is uniform for the incremental positive sequence and negative sequence reactive current components as prescribed in Table 3-IX. If the maximum value of the space vector of the current in (112) is less than the phase current limit of the inverter, the remaining capacity is then used for  $i_{d1}$ .  $i_{d1max}$  is determined by setting (111) equal to the current limit and solving for  $i_{d1}$ .

$$I_{lim} \geq |i_{d1}'^* + ji_{q1}'^*| + |i_{d2}'^* + ji_{q2}'^*| \quad (113)$$

Solving for  $i_{d1}'^*$ , the  $dI$ -axis current limit is:

$$i_{d1max} = \sqrt{\left(I_{lim} - \sqrt{(i'_{d2*})^2 + (i'_{q2*})^2}\right)^2 - (i'_{q1*})^2} \quad (114)$$

The pseudo-code of the current limit logic, where  $I_{lim}$  is the specified current limit of the inverter, is given by:

if  $i_{\alpha\beta max} > I_{lim}$ :

if  $\Delta i_{q1} > 0$ :

$$scale = \frac{I_{lim} - i_{q1i}}{|\Delta i_{q1}| + |i_{d2}^* + j i_{q2}^*|}$$

else:

$$scale = \frac{I_{lim} + i_{q1i}}{|\Delta i_{q1}| + |i_{d2}^* + j i_{q2}^*|}$$

$$i'_{q1*} = \Delta i_{q1} * scale + i_{q1i}$$

(115)

$$i'_{d2*} + j i'_{q2*} = \min(|i_{d2}^* + j i_{q2}^*|, \Delta i_{q1}) * scale \angle \left( \tan^{-1} \frac{i_{q2}^*}{i_{d2}^*} \right)$$

else:

$$i'_{q1*} = i_{q1}^*$$

$$i'_{d2*} = i_{d2}^*$$

$$i'_{q2*} = i_{q2}^*$$

$$i_{d1max} = \sqrt{\left(I_{lim} - \sqrt{(i'_{d2*})^2 + (i'_{q2*})^2}\right)^2 - (i'_{q1*})^2}$$

### 3.5.5.2. Method 2

Depending on the phase difference between  $I_1$  and  $I_2$ , using the maximum value of the space vector of the current in (112) as a proxy for the maximum value of the three-phase currents may overestimate the maximum phase current. For illustration purposes, Figure 3-63 shows the maximum amplitude of each phase current as the phase difference between  $I_1$  and  $I_2$  is varied between  $0^\circ$  and  $360^\circ$ . This shows there are phase relationships between the positive and negative sequence current components where the current limit logic in method 1 will not utilize the full capacity of the inverter current of at least one phase during asymmetrical faults.

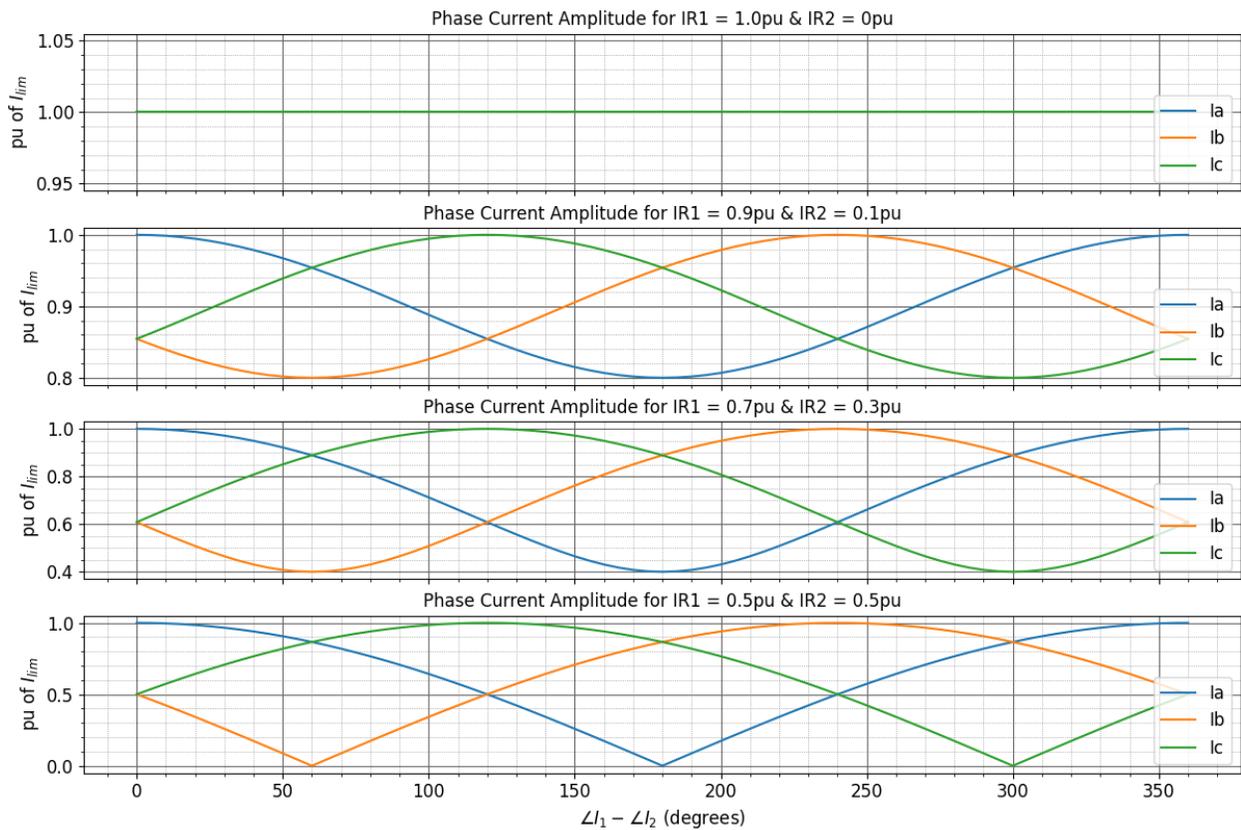


Figure 3-63. Example of the amplitude of each phase current as a function of the phase difference of the symmetrical components of the current.

The authors in [71] proposed a negative sequence current injection that maximizes the current capacity of the inverter given a desired positive sequence current injection. The approach solves for the negative sequence current reference as a function of the positive sequence current reference and the symmetrical components of the terminal voltage. This is not used directly in the model prototype because it would not meet the requirements in Table 3-IX. Recall that the control objective is closed-loop control of the positive and negative sequence voltages. If the current limit of the inverter is exceeded, the components are then uniformly reduced. However, the derivation of the negative sequence current reference in [71] provides insight into the conditions the current limit logic of method 1 would result in at least one phase not reaching the maximum current.

Given the symmetrical components of the current, assuming  $I_0 = 0$ , the phasor currents are given as:

$$\begin{aligned} \mathbf{I}_a &= \mathbf{I}_1 + \mathbf{I}_2 \\ \mathbf{I}_b &= a^2 \mathbf{I}_1 + a \mathbf{I}_2 \\ \mathbf{I}_c &= a \mathbf{I}_1 + a^2 \mathbf{I}_2 \end{aligned} \tag{116}$$

Solving for the magnitude of each phasor current by applying:

$$|\mathbf{A} + \mathbf{B}| = \sqrt{|\mathbf{A}|^2 + |\mathbf{B}|^2 + 2|\mathbf{A}||\mathbf{B}| \cos(\angle \mathbf{A} - \angle \mathbf{B})} \tag{117}$$

results in:

$$\begin{aligned} |\mathbf{I}_a| &= \sqrt{|\mathbf{I}_1|^2 + |\mathbf{I}_2|^2 + 2|\mathbf{I}_1||\mathbf{I}_2| \cos(\angle \mathbf{I}_1 - \angle \mathbf{I}_2)} \\ |\mathbf{I}_b| &= \sqrt{|\mathbf{I}_1|^2 + |\mathbf{I}_2|^2 + 2|\mathbf{I}_1||\mathbf{I}_2| \cos(\angle \mathbf{I}_1 - \angle \mathbf{I}_2 + 120^\circ)} \end{aligned} \tag{118}$$

$$|\mathbf{I}_c| = \sqrt{|\mathbf{I}_1|^2 + |\mathbf{I}_2|^2 + 2|\mathbf{I}_1||\mathbf{I}_2| \cos(\angle \mathbf{I}_1 - \angle \mathbf{I}_2 - 120^\circ)}$$

To apply to the current limit logic in method 1, the phase angle difference between the positive and negative sequence current components is calculated.

$$\angle \mathbf{I}_1 - \angle \mathbf{I}_2 = \text{atan2}\left(\frac{i_{q1}}{i_{d1}}\right) + \text{atan2}\left(\frac{i_{q2}}{i_{d2}}\right) \quad (119)$$

The magnitude of the positive and negative sequence components of the current is calculated as:

$$|\mathbf{I}_1| = \sqrt{i_{d1}^2 + i_{q1}^2} \quad (120)$$

$$|\mathbf{I}_2| = \sqrt{i_{d2}^2 + i_{q2}^2} \quad (121)$$

Note that the symmetrical component phasors are written as peak values instead of RMS for simplicity. Appendix G provides more information on the relationship between the symmetrical component phasors and the  $\alpha\beta$  and SRF signals. Based on the relationships in (118), a scaling factor is defined as:

$$\text{scale}_{phmax} = \frac{I_{lim}}{\max(|\mathbf{I}_a|, |\mathbf{I}_b|, |\mathbf{I}_c|)} \quad (122)$$

Figure 3-64 shows a block diagram of the addition to the current limit logic. The current references that were the output of the method 1 current limit logic are the input. The limiter prevents the scaling factor from going outside of the prescribed range during transients.

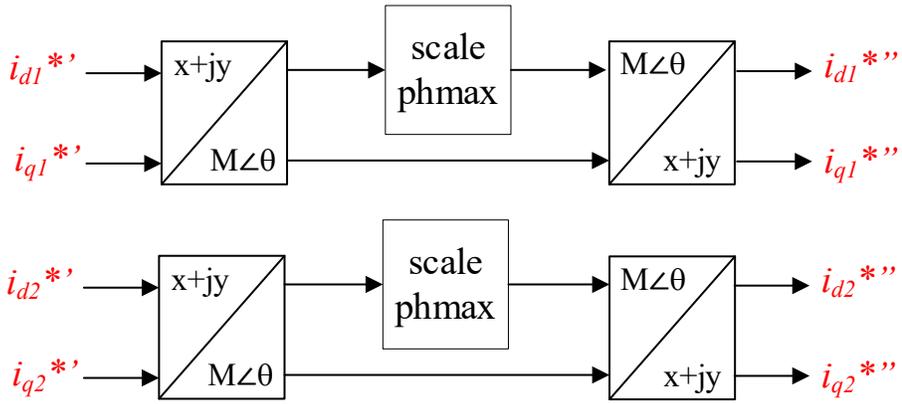
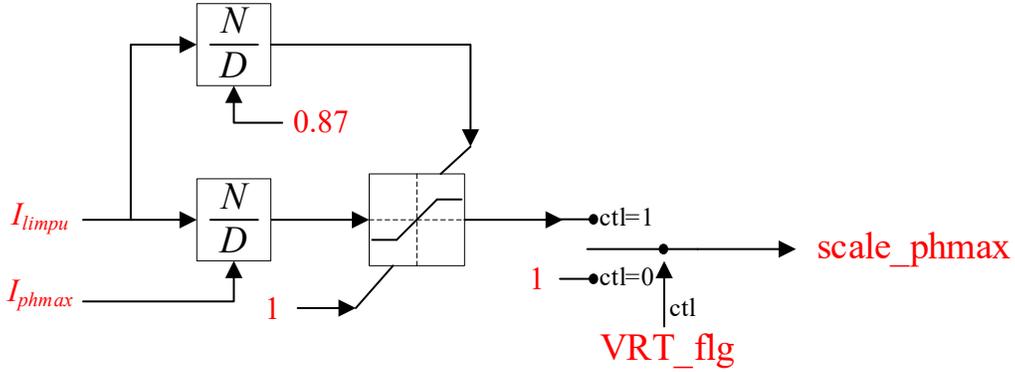


Figure 3-64. Scaling factor for current logic based on maximum phase current.

### 3.5.5.3. Verification of Current Limit Logic

The two current limit methods are compared to show the improvement the 2<sup>nd</sup> method provides under certain phase relationships between the positive and negative sequence current. The simulations are of phase B to phase C faults on the MV side of the inverter step-up transformer shown in Figure 3-65. The inverter is configured with  $k_{qv1} = k_{qv2} = 2.0$ . This results in the inverter reaching the current limit set to 1.0 pu during the fault. The MV transformer winding configuration is changed for each example to vary the difference in the positive and negative sequence current phase angles. The plots are of the inverter terminal voltage and current.

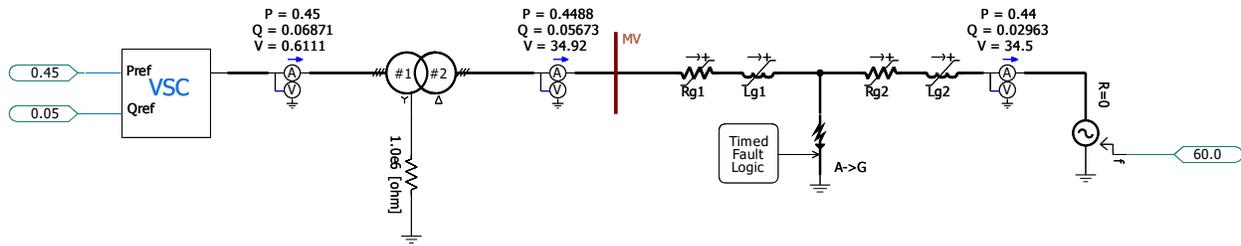


Figure 3-65. Simulation test system.

The first example considers  $\angle I_1 - \angle I_2 = 180^\circ$ . The inverter step-up transformer is configured delta-delta. For this scenario, the example in Figure 3-63 predicts that the current limit method 1 will result in the phase B and phase C current peak of  $0.87I_{lim}$  and the phase A current will be zero. Figure 3-66 shows the phase B and phase C currents are limited to  $0.87I_{lim}$  using method 1 for the current limit logic as predicted. Figure 3-67 shows that with the current limit method 2, the phase B and phase C currents are limited to the current limit of 1.0pu as desired.

The second example considers  $\angle I_1 - \angle I_2 = 120^\circ$ . The inverter step-up transformer is configured wye ungrounded (LV) – delta (MV) with the delta windings configured to lead the LV terminal phase by  $30^\circ$ . For this scenario, the example in Figure 3-63 predicts that the current limit method 1 will result in phase C current peak of  $1.0I_{lim}$ . In this case, method 1 shown in Figure 3-68 and method 2 shown in Figure 3-69 show identical results.

The third example considers  $\angle I_1 - \angle I_2 = -120^\circ$ . The inverter step-up transformer is configured wye ungrounded (LV) – delta (MV) with the delta windings configured to lag the LV terminal phase by  $30^\circ$ . For this scenario, the example in Figure 3-63 predicts that the current limit method 1 will result in phase B current peak of  $1.0I_{lim}$ . In this case, method 1 shown in Figure 3-70 and method 2 shown in Figure 3-71 show identical results.

These examples illustrate that for certain values of phase difference between the positive and negative sequence current components, method 2 results in higher current injection up to the

current limit of at least one phase while adhering to the grid code requirements. In the model prototype, both current logic methods are implemented and can be enabled by the end-user.

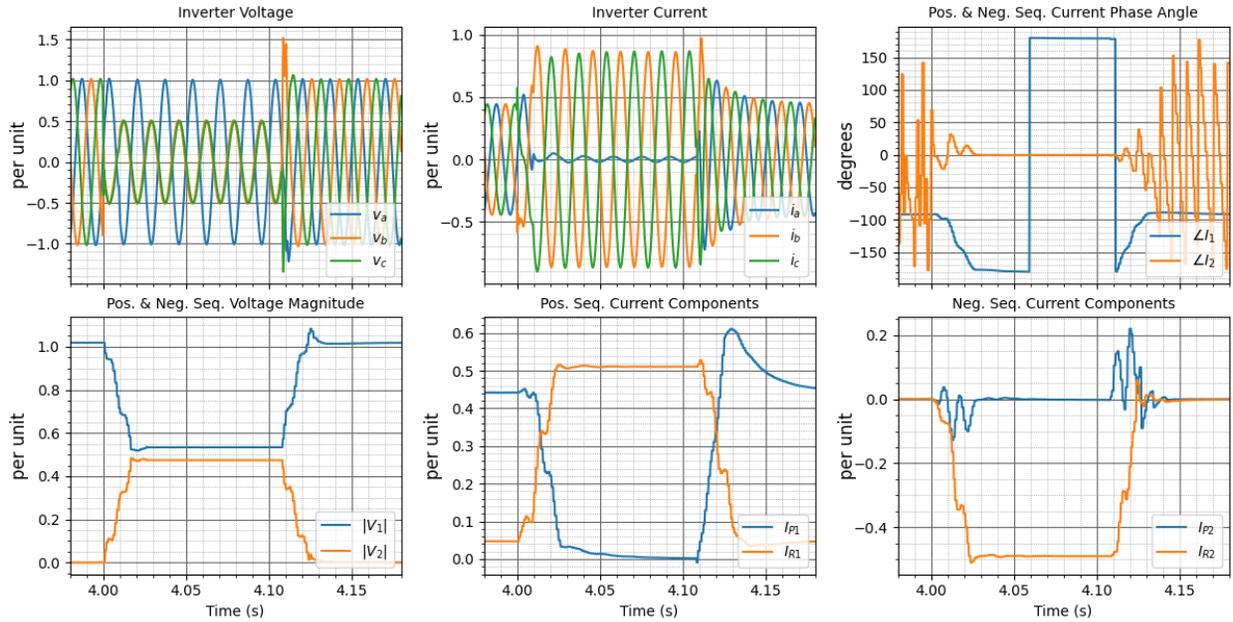


Figure 3-66. B-C fault at MV side of inverter step-up transformer.  $180^\circ$  phase angle difference between  $I_1$  and  $I_2$ . Current limit method 1.

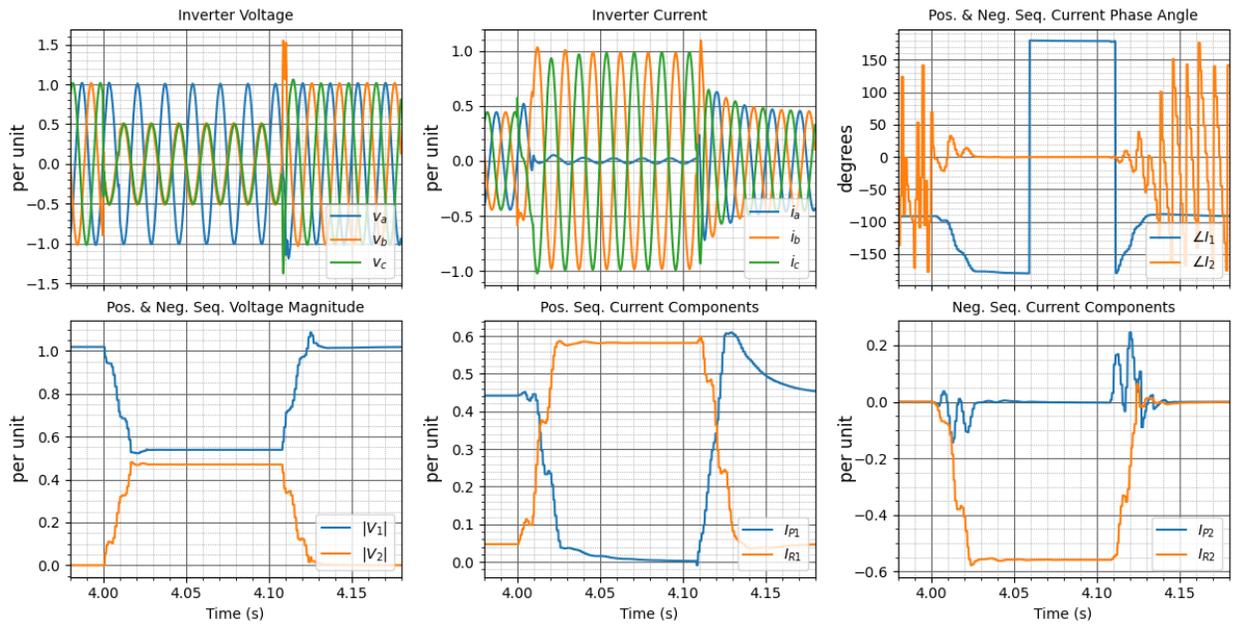


Figure 3-67. B-C fault at MV side of inverter step-up transformer.  $180^\circ$  phase angle difference between  $I_1$  and  $I_2$ . Current limit method 2.

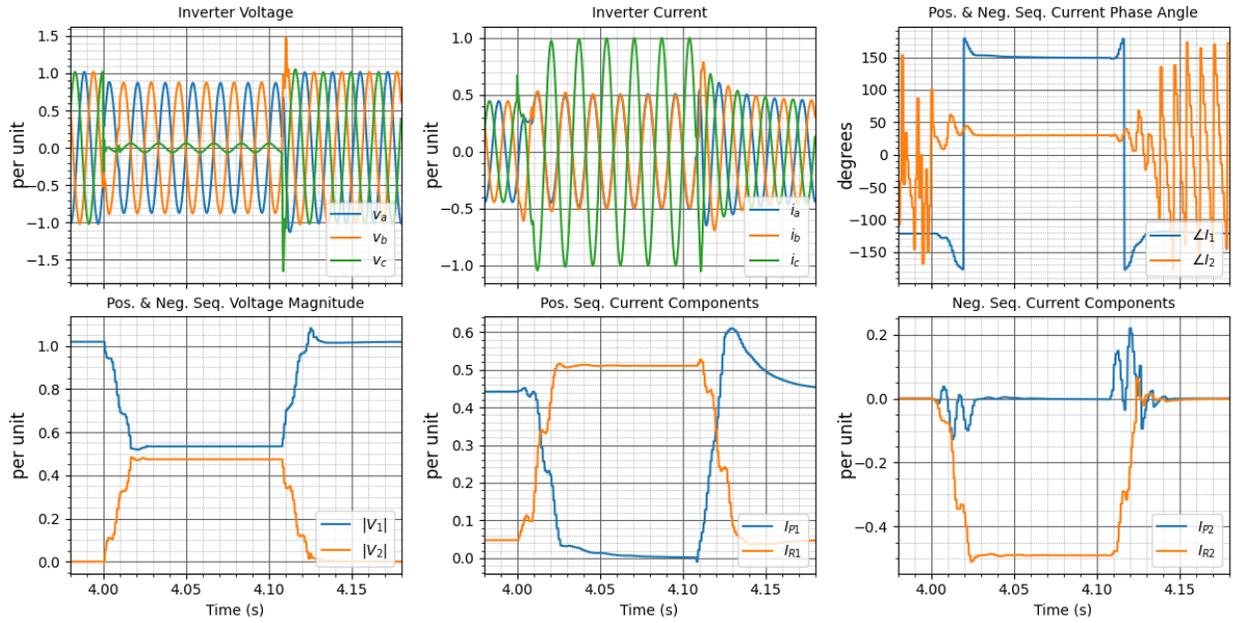


Figure 3-68. B-C fault at MV side of inverter step-up transformer.  $+120^\circ$  phase angle difference between  $I_1$  and  $I_2$ . Current limit method 1.

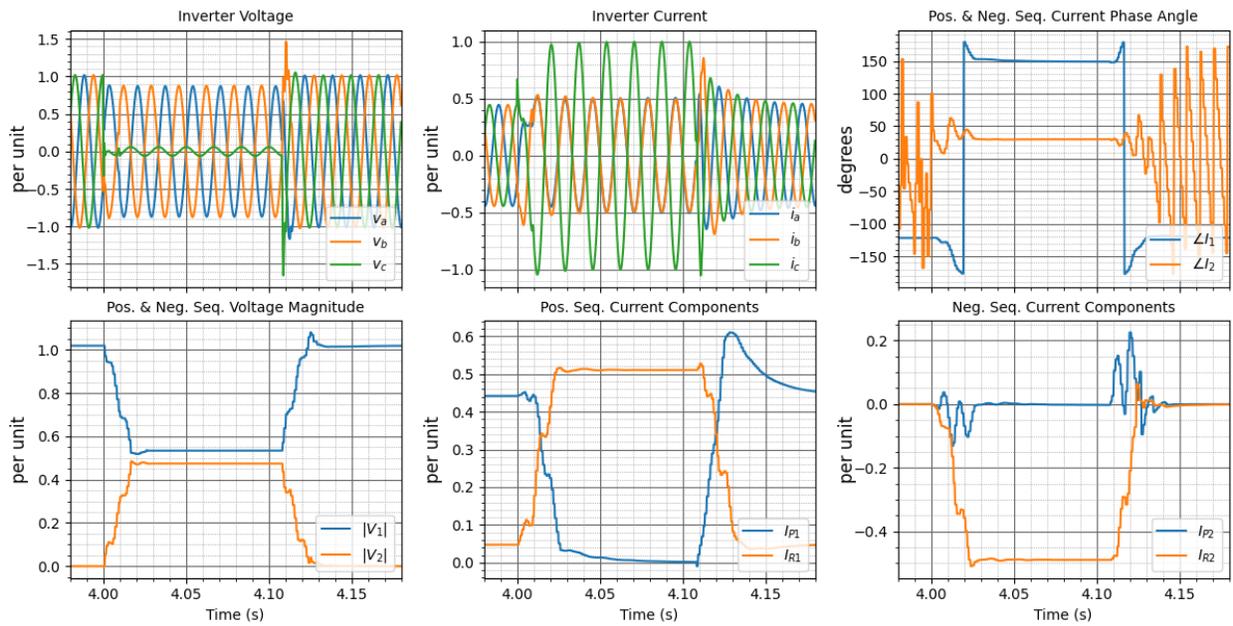


Figure 3-69. B-C fault at MV side of inverter step-up transformer.  $+120^\circ$  phase angle difference between  $I_1$  and  $I_2$ . Current limit method 2.

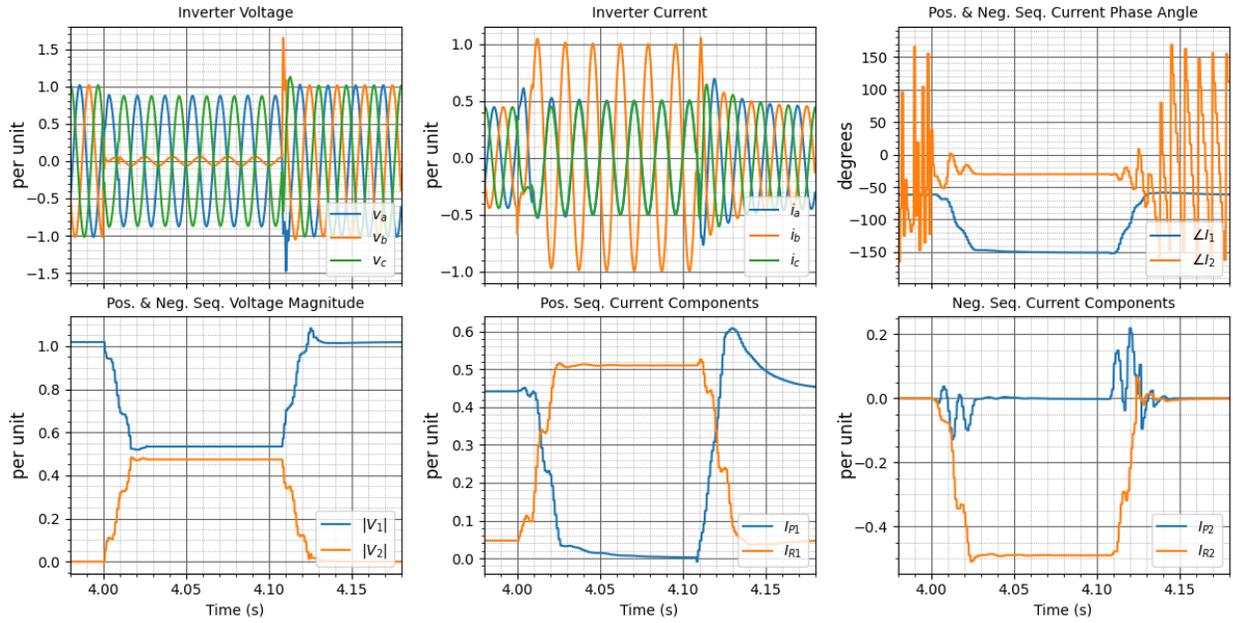


Figure 3-70. B-C fault at MV side of inverter step-up transformer.  $-120^\circ$  phase angle difference between  $I_1$  and  $I_2$ . Current limit method 1.

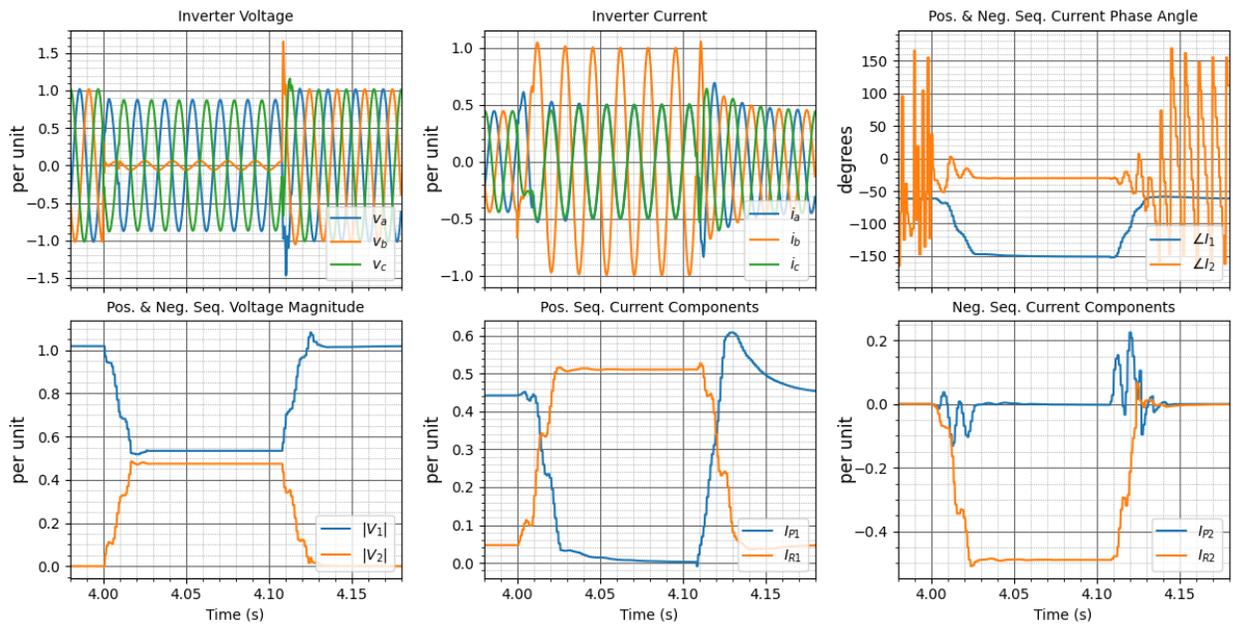


Figure 3-71. B-C fault at MV side of inverter step-up transformer.  $-120^\circ$  phase angle difference between  $I_1$  and  $I_2$ . Current limit method 2.

## 4. Model Verification

The inverter model presented in Chapter 2 and Chapter 3 is developed to represent inverters capable of meeting the performance requirements in Table 3-IX. It does not represent any specific OEM's control or design. The performance requirements were used to determine the control objective of the inverter under different conditions. The inverter control is then designed to meet these objectives.

In Chapter 2 and Chapter 3, the different control functions and controllers are verified mainly by step tests of the reference setpoint. The focus of the model verification in this chapter is on the controlled response of the inverter during FRT control mode. The inverter model response is verified in two ways in this chapter. First, simulations are performed showing that the inverter model response meets the performance requirements for LVRT. Second, the inverter model response is compared to measurements from laboratory testing of a commercial inverter.

The terms “verification” and “validation” are sometimes used interchangeably in terms of modeling. They may have different connotations, including legal implications, in different industries. The position taken is that a validated model would necessitate an accepted defined metric of required model accuracy and an associated validation procedure or requirements. In the absence of such a metric in North America at present, verification is used in this chapter to describe the process of evaluating the model's response. The term verification is also consistent with the language used in the NERC MOD-026-1 and NERC MOD-027-1 standards. The chosen term should not distract from the purpose of this chapter which is to show the capability and potential limitations of the model.

#### 4.1. Model Verification Based on Performance Requirements

This section shows the capability of the inverter model to meet the LVRT performance requirements shown in Table 4-I. Time-domain simulations are performed in PSCAD™ to verify the current components, step response time, settling time, and current prioritization meet the minimum performance requirements.

Table 4-I. IEEE P2800 Draft 6.1 LVRT Response Performance Requirements

Parameter	Description	IEEE P2800 D6.1 [25]
$\Delta i_{r1}$	Incremental positive sequence reactive current	Dependent on $V_1$ at inverter terminal
$\Delta i_{r2}$	Incremental negative sequence reactive current	Dependent on $V_2$ at inverter terminal
$\angle I_2$	Phase angle of negative sequence with respect to negative sequence voltage	Leads $\angle V_2$ by $90^\circ$ to $100^\circ$
Step response time: $t_r$	Time for the signal to reach 90% of the final value upon step change in input	$\leq 2.5$ cycles <sup>a</sup> [41.67 ms at 60Hz]
Settling time: $t_s$	Settling band defined as -2.5%/+10% of inverter maximum current	$\leq 4.0$ cycles <sup>a</sup> [66.67 ms at 60Hz]
Default current priority	Prioritization of current components if the current limit is reached	Reactive current priority. If asymmetrical fault: $\Delta i_{r1} \geq \Delta i_{r2}$ with preference of equal reduction of $\Delta i_{r1}$ and $\Delta i_{r2}$ .

<sup>a</sup> Evaluated based on phasor quantities with 1-cycle moving average window.

The LVRT performance requirements in Table 4-I are specified in terms of sequence components which are frequency domain quantities. To evaluate the inverter's response with

respect to these requirements, the signals are decomposed into their fundamental frequency, active and reactive components in the positive and negative sequences. A DFT applied to a one-cycle moving window is used to calculate the fundamental frequency phasor quantities. The phasor quantities are then decomposed into the active and reactive current in both the positive and negative sequences and plotted as a function of time. The notation used in this chapter to represent these components is provided in (123), (124), (125), and (126). The positive sequence fundamental frequency active current component is given by:

$$i_{p1} = |I_1| \cos(\angle V_1 - \angle I_1) \quad (123)$$

The positive sequence fundamental frequency reactive current component is given by:

$$i_{r1} = |I_1| \sin(\angle V_1 - \angle I_1) \quad (124)$$

The negative sequence fundamental frequency active current component is given by:

$$i_{p2} = |I_2| \cos(\angle V_2 - \angle I_2) \quad (125)$$

The negative sequence fundamental frequency reactive current component is given by:

$$i_{r2} = |I_2| \sin(\angle V_2 - \angle I_2) \quad (126)$$

Examination of (124) indicates that  $i_{r1}$  is greater than zero for positive sequence reactive current lagging the positive sequence voltage. The negative sequence current phasor should lead the negative sequence voltage phasor by  $90^\circ$  based on the performance requirements. Examination of (125) and (126) indicates that  $i_{r2}$  is less than zero and  $i_{p2}$  is equal to zero for purely reactive current injection leading the negative sequence voltage in this notation. These components are similar to the positive and negative SRF signals used in the inverter control. The main differences

being the SRF signals are instantaneous time-domain signals and the negative SRF is not aligned to the negative sequence voltage space vector. The positive and negative sequence SRF signals are also plotted to provide insight into the control signals of the inverter.

The simulation test system is shown in Figure 4-1. The test system consists of the inverter model, a 1 MVA 600 V-34.5 kV transformer, and an ideal voltage source behind a grid equivalent resistance and inductance. The grid equivalent impedance is set to achieve an SCR = 5 at the inverter 600 V bus. The inverter settings configuration is detailed in Table 4-II. The target magnitude of the incremental positive sequence and negative sequence reactive current based on the control strategy detailed in Section 3.5.4 and the configuration of the inverter detailed in Table 4-II is given by:

$$|\Delta i_{r1}| = (|\Delta V_1| - db)k_{qv1} \quad (127)$$

$$|\Delta i_{r2}| = (|\Delta V_2| - db)k_{qv2} \quad (128)$$

Table 4-II. Inverter and Test System Configuration.

Parameter	Setting
Inverter	1.0 MVA, 600 V
Inverter current limit	$I_{lim} = 1.1 pu$
LCL output filter	$L_{1flr} = 0.1 mH, L_{2flr} = 0.0 mH, C_{flr} = 147.36 \mu F,$ $R_d = 0.11 \Omega$
Enable V2 control	$V2\_flg = 1$
Constant DC voltage	$Vdc\_flg = 0$
Q control	$Vt\_flg = 0$

LVRT control	$V_1$ control: $k_{qv1} = 2.0$ , $db = \pm 0.1$ $V_2$ control: $k_{qv2} = 2.0$ , $db = \pm 0.01$ $k_p = 0.32325$ , $k_i = 324.0$
Current control	$V_{ff\_flg} = 0$ (feedforward control disabled) Current limit method 2
PLL (DSOGI)	$k_p = 77.0$ , $k_i = 7.0$
Grid equivalent	$R_g = 16.67 \Omega$ , $L_g = 0.442$ mH 600 V (wye-ungrounded)– 34.5 kV (delta)
Inverter step-up transformer	Rating = 1 MVA $Z = 6\%$

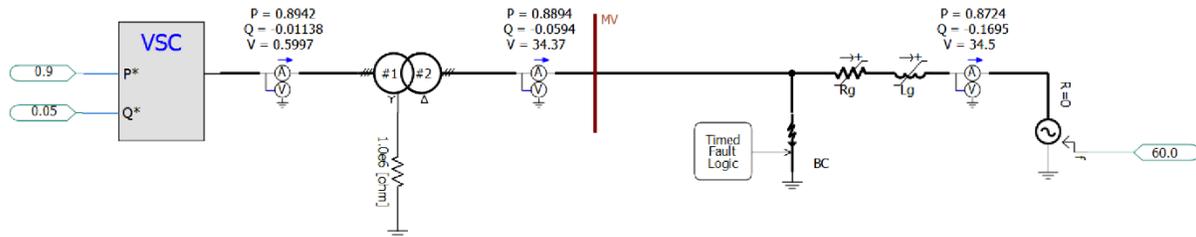


Figure 4-1. Simulation test system.

#### 4.1.1. Symmetrical Fault Simulations

A three-phase to ground fault (3PH) at the MV bus is simulated showing the response of the inverter. The fundamental frequency symmetrical components are plotted as a function of time in Figure 4-2 verifying the inverter response meets the performance requirements. In this case, the inverter injects purely reactive current in the positive sequence. The maximum allowable step response time and settling time are superimposed as the vertical red lines in the plots of the current components. The current response meets the specified step response time and settling time requirements. The current is limited to the specified current limit superimposed as horizontal red

lines in the plot of the instantaneous currents verifying the current limit logic. The active current,  $i_{p1}$ , is ramp-rate limited to 1.0 pu/s post fault clearing. At the fault inception and the fault clearing, the sequence components in Figure 4-2 calculated based on a DFT applied to a one cycle window contain unidirectional and oscillatory transients. It is shown in Chapter 8 of [72] that these are due to the calculation method and have no physical meaning.

Figure 4-3 shows the inverter response in terms of the positive and negative sequence SRF components of the voltage and current, the PLL frequency, and the instantaneous active and reactive power. The PLL frequency exhibits large variations at fault inception and fault-clearing, but the ideal voltage source frequency is constant through the simulation. As described in Section 3.3.3, the PLL's objective is to determine the instantaneous angle of the positive sequence component of the grid voltage space vector. The PLL frequency increases or decreases from nominal to lock onto the grid voltage angle. This underscores the potential issues using the PLL frequency directly without filtering to represent the system frequency in the inverter control or protection. The instantaneous active and reactive power show that the severity of the voltage dip limits the amount of reactive power the inverter can exchange with the grid even when the inverter is using the full current capacity for reactive current.

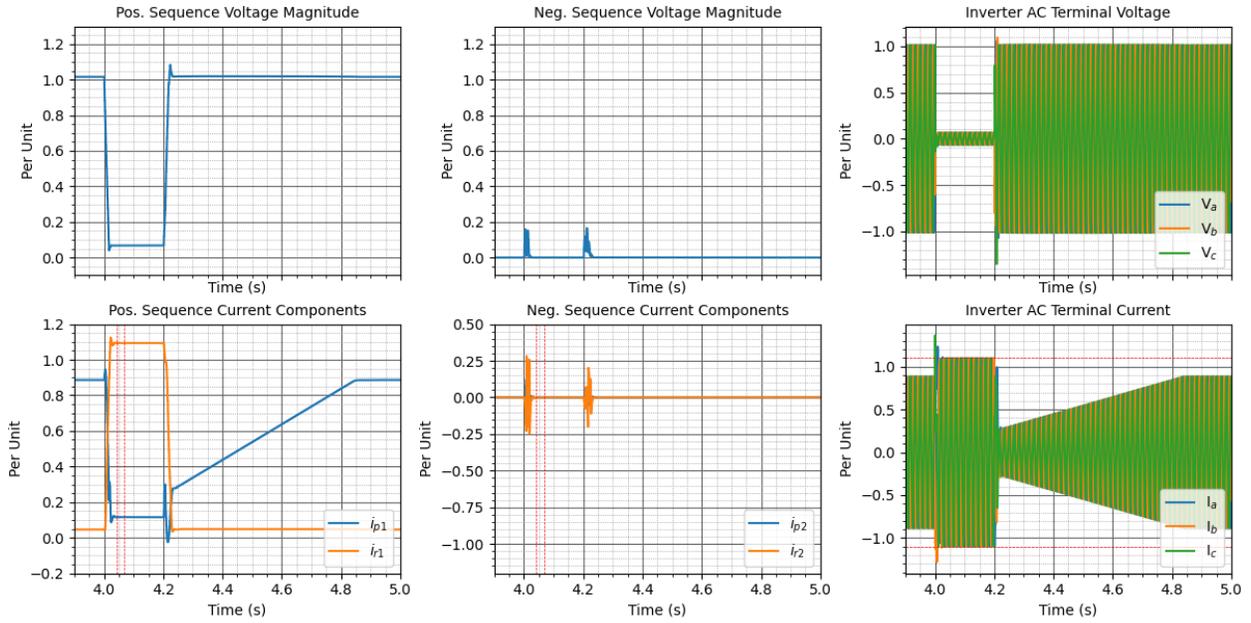


Figure 4-2. Fundamental frequency components and instantaneous voltage and current for a 3PH fault at the MV bus.

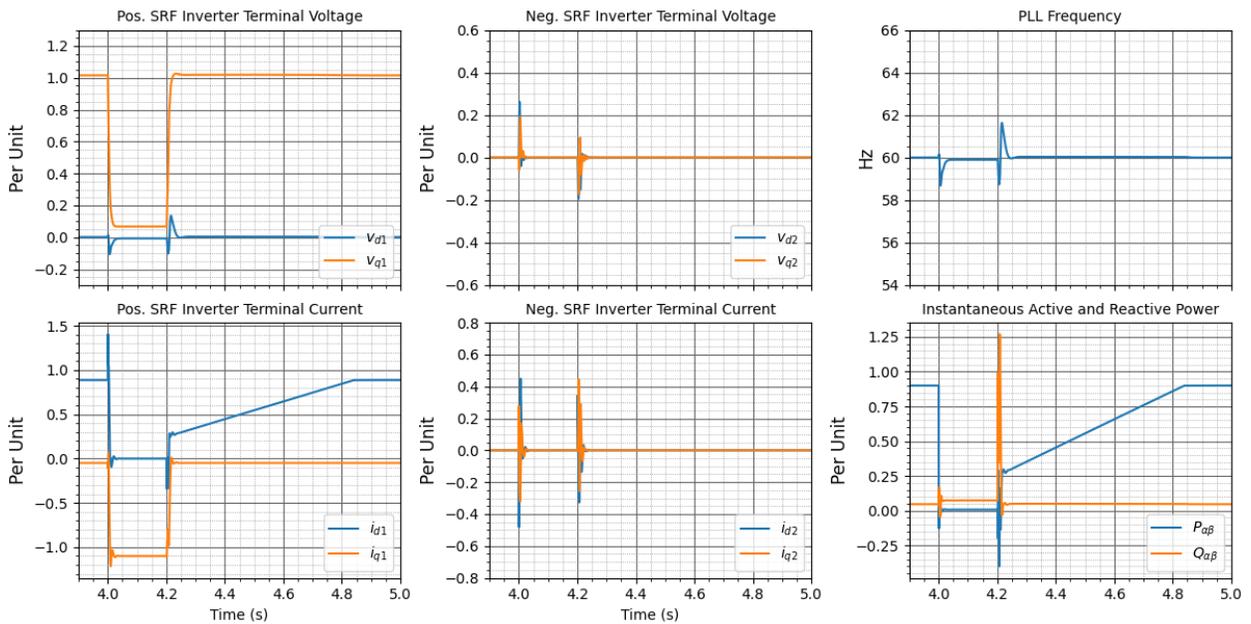


Figure 4-3. SRF voltage and current, PLL frequency, and instantaneous active and reactive power for a 3PH fault at the MV bus.

#### 4.1.2. Asymmetrical Fault Simulations

In this section, phase-to-phase faults and phase-to-ground faults are considered to verify the inverter's response to system faults that result in negative sequence voltage. The same approach used in the previous section to evaluate the response is used in this section. The presence of negative sequence voltage facilitates verification of the negative sequence current injection during LVRT. This also allows testing of the inverter current limit logic to verify the inverter prioritizes reactive current in both the positive and negative sequences and uniformly reduces the incremental reactive currents in the positive and negative sequences if the limit is reached. For a B-C fault at the MV bus, Figure 4-4 shows the inverter injects both positive and negative sequence reactive current. The plot of the instantaneous phase currents shows the current is limited such that the maximum phase current is equal to the current limit. The response shows the reactive current is prioritized and uniformly reduced in both the positive and negative sequences. Figure 4-5 shows the inverter response in terms of the positive and negative sequence SRF components of the voltage and current, the PLL frequency, and the instantaneous active and reactive power. The 120 Hz component in the instantaneous active and reactive power signals indicates the presence of negative sequence components. The absence of these 120 Hz components in the voltage and current SRF signals indicates the approach used for the decomposition of the sequence components is effective.

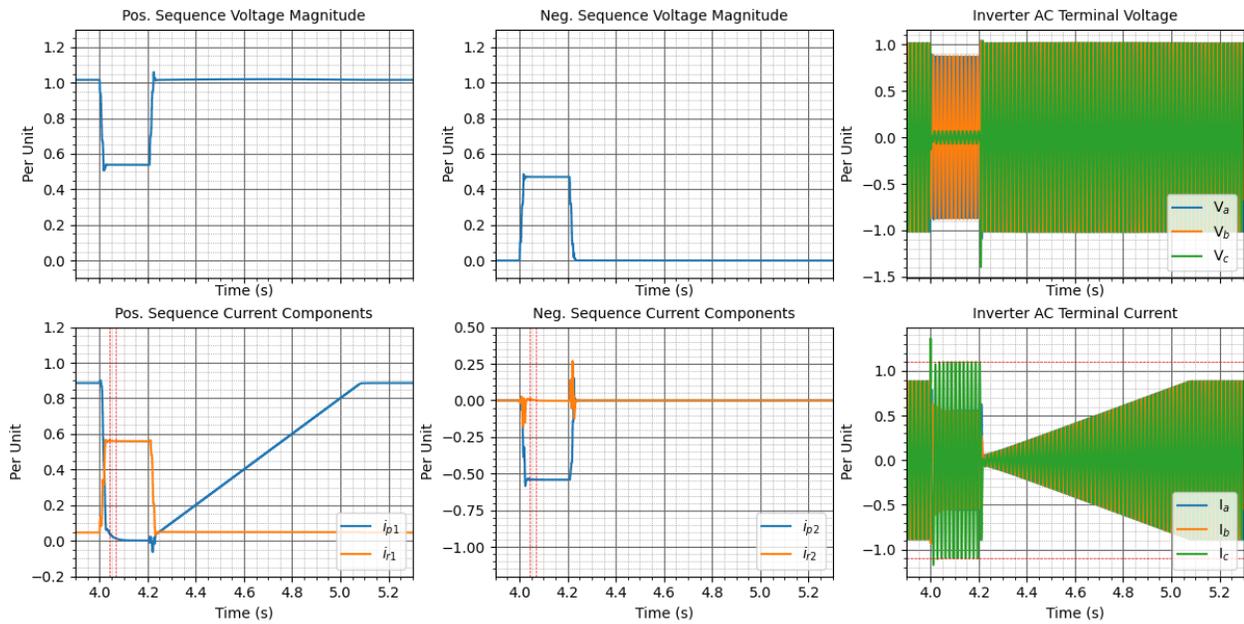


Figure 4-4. Fundamental frequency components and instantaneous voltage and current for a BC fault at the MV bus.

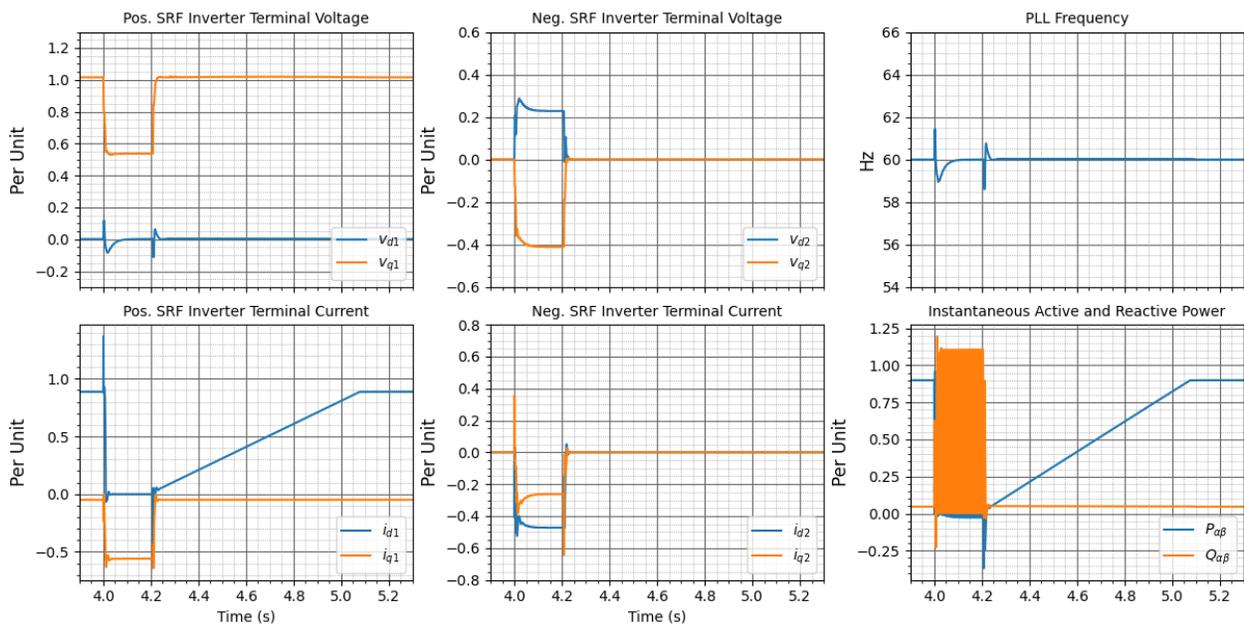


Figure 4-5. SRF voltage and current, PLL frequency, and instantaneous active and reactive power for a BC fault at the MV bus.

Figure 4-6 shows the inverter response for an A-B fault at the MV bus. The response is the same as for the B-C fault in terms of the magnitudes of the sequence components. This simulation

shows the LVRT voltage control is decoupled between the positive and negative sequence until the current limiter logic. This results in the same symmetrical current components based on how they are defined in (123), (124), (125), and (126) for the A-B fault and the B-C fault. The relative phase angle difference between  $I_1$  and  $I_2$  effects the resulting phase currents as discussed in Section 3.5.5. In Figure 4-6, the resulting instantaneous current waveforms show the maximum phase current is phase B whereas for the B-C fault, the maximum current was phase C. In both cases, the maximum phase current is limited to the current limit.

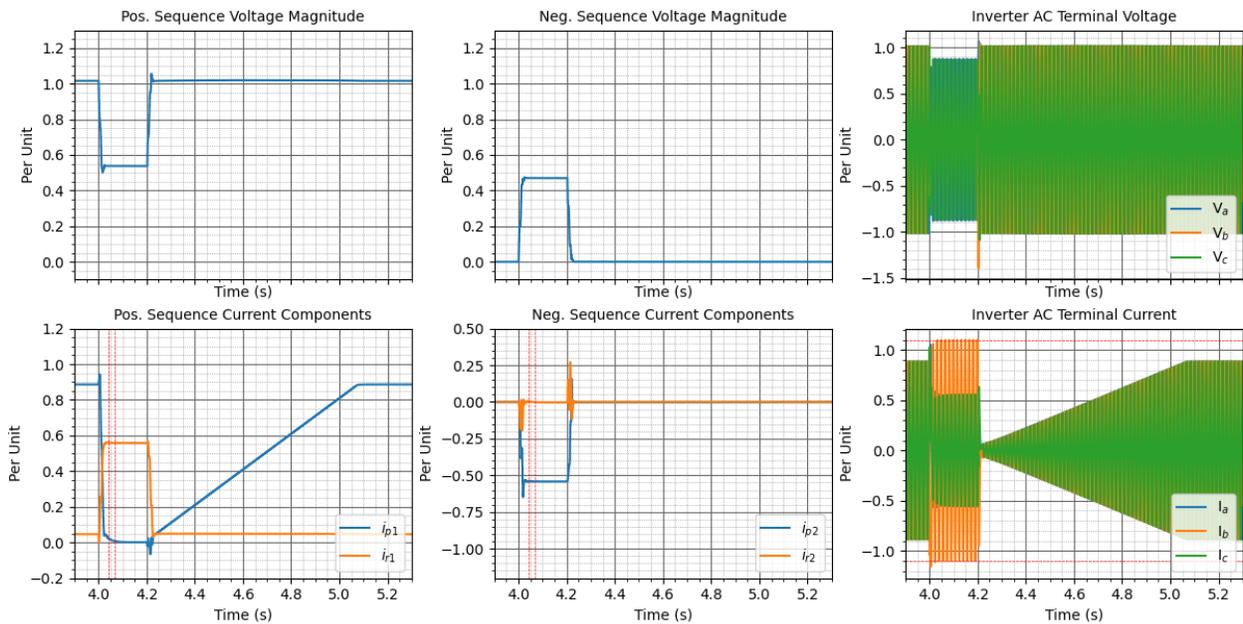


Figure 4-6. Fundamental frequency components and instantaneous voltage and current for an AB fault at the MV bus.

Figure 4-7 shows the inverter response for an A-G fault. This simulation verifies the response of the inverter when the full current capability is not utilized by the reactive component of the current. In this case, the target  $\Delta i_{r2}$  is greater than the target  $\Delta i_{r1}$ . Based on the performance requirements,  $\Delta i_{r2}$  is limited to be  $\leq \Delta i_{r1}$ . The active current component,  $i_{p1}$ , uses the remaining current capacity. Phase A is the highest phase current and is limited to the current limit.

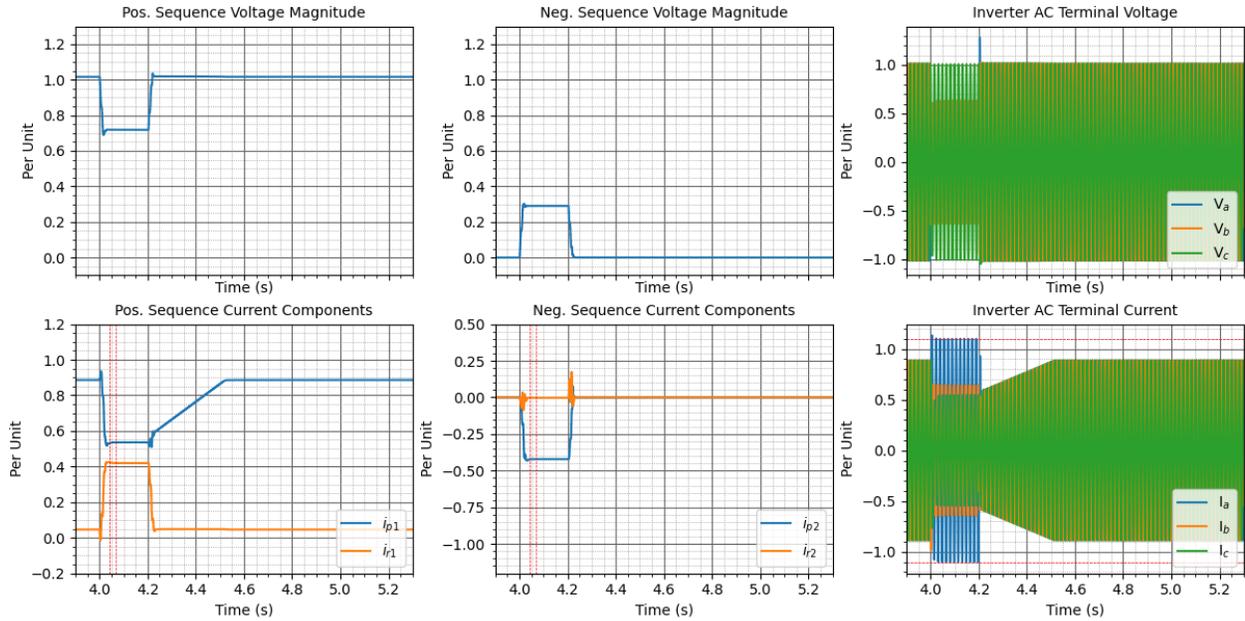


Figure 4-7. Fundamental frequency components and instantaneous voltage and current for an AG fault at the MV bus.

### 4.1.3. Summary

This section shows that the inverter control developed and implemented in the model prototype meets the LVRT response performance requirements in the draft IEEE P2800 standard. The inverter response is verified in terms of step response time, settling time, magnitude, and current prioritization. The standard does not prescribe a specific incremental current magnitude for a given voltage deviation. This determination is left to the grid operator underscoring one of the use cases of the model developed in this work. A white-box, open model that meets the IEEE P2800 range of LVRT performance requirements can be used to investigate the desired response of an IBR interconnecting to a grid operator's system.

## 4.2. Model Verification Based on Laboratory Testing

The previous section showed the inverter control implemented in the model prototype could be configured to meet the IEEE P2800 D6.1 LVRT response requirements. This section shows the

capability of the inverter model to be configured to predict the LVRT response behavior of a commercial inverter.

#### 4.2.1. Commercial Inverter Laboratory Testing

The inverter under test (IUT) is a 2.2 MVA commercial central storage inverter. The inverter tests were performed at the National Renewable Energy Laboratory (NREL) test facility. A single-line diagram of the test circuit is shown in Figure 4-8. The voltages and currents are measured at the 13.2 kV bus with a 50 kHz sampling rate. The measured response includes the influence of the inverter step-up transformer. Current measurements from the LV side of the inverter step-up transformer were not available.

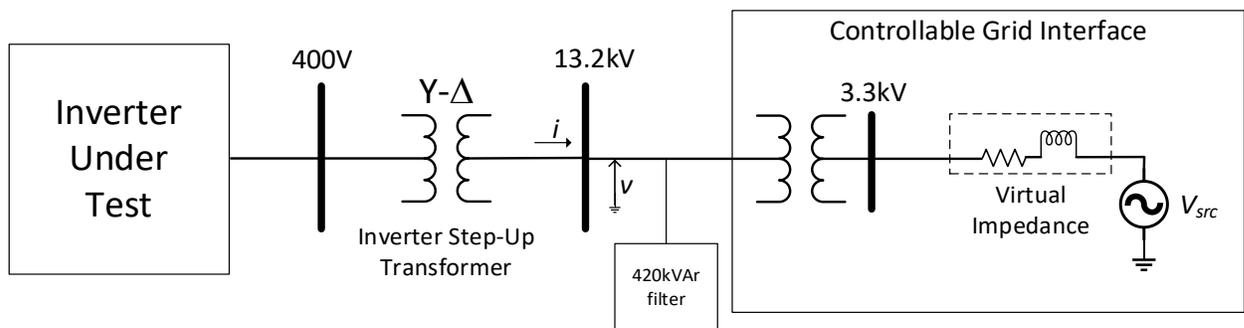


Figure 4-8. Single-line diagram of the laboratory test circuit.

A test plan was developed to characterize the response of the inverter for the purposes of model development, improvement, and verification. The LVRT tests were developed to characterize the response of the inverter for voltage dips at the inverter terminal representative of faults on the transmission system. Both symmetrical and asymmetrical faults were considered. The test voltage waveforms were developed to represent three-phase (3PH) faults, line-line (LL) faults, and single-line-ground (SLG) faults. The voltage test vectors represent Type III, Type II, and the

recommended Type I voltage sags defined in IEEE Standard 1668-2017 [73]. The LVRT response test procedures are detailed in Chapter 3 of [74].

The laboratory test circuit is modeled in PSCAD™ along with the generic inverter model developed in this work, as shown in Figure 4-9. The test procedures in Chapter 3 of [74] specify that the target voltage dips are without the inverter under test connected since the inverter response will influence the inverter terminal voltage. The measured 13.2 kV bus voltage of the laboratory tests with the inverter disconnected is used to drive the controllable voltage source in the EMT simulations.

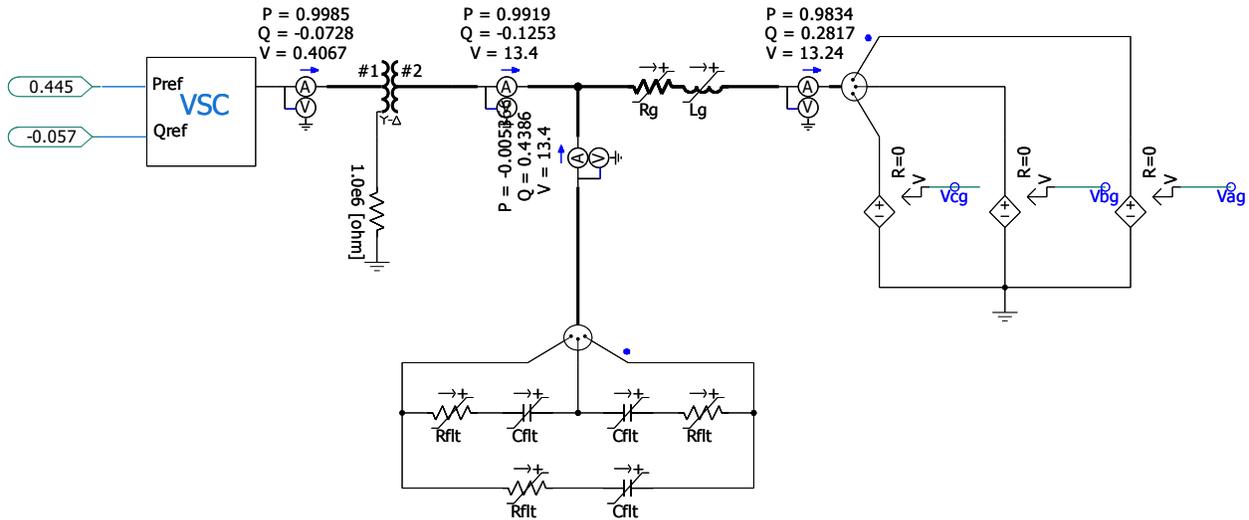


Figure 4-9. PSCAD model of the laboratory test circuit.

The specifics of the inverter under test's design and control are unknown. The parameterization of the generic model in Chapter 2 and Chapter 3 was used as a starting point. The parameters were then fine-tuned based on the laboratory testing data. Table 4-III gives the inverter prototype model configuration corresponding to the comparison plots.

Table 4-III. Inverter Model Configuration for Verification Via Laboratory Testing.

Parameter	Setting
Inverter	2.2 MVA, 400.0 V
Inverter current limit	$I_{lim} = 1.0 pu$
LCL output filter	$L_{1flr} = 0.013 mH, L_{2flr} = 0.0 mH, C_{flr} = 900 \mu F, R_d = 0.11 \Omega$
Enable V2 control	V2_flg = 1
Constant DC voltage	Vdc_flg = 0
Q control	Vt_flg = 0
LVRT control	V <sub>1</sub> control: kqv1 = 2.0, db = ±0.1 pu V <sub>2</sub> control: kqv2 = 2.0, db = ±0.1 pu kp = 0.01632, ki = 6.948
Current control	Vff_flg = 0 (feedforward control disabled) Current limit method 1
PLL (DDSRF)	kp = 80., ki = 8.0
Grid equivalent	$R_g = 0.529 \Omega, L_g = 0.0141 mH$
Inverter step-up transformer	400 V (wye-ungrounded) – 13.2 kV (delta) Rating = 1.1 MVA, Z = 6%

The verification of the model prototype is performed by comparing the model's response to the measured response of the inverter in the laboratory tests. Of primary interest is the controlled response of the inverter to different types of voltage dips consistent with symmetrical and asymmetrical grid faults. The calculated positive and negative sequence SRF components of the voltage and current, the instantaneous active and reactive power, and the three-phase voltage and current of the laboratory measurements (blue traces) are compared to the model response in simulation (dashed orange traces) on the same plots. There was no access to the control signals of

the inverter under test. Therefore, the positive sequence and negative sequence SRFs are set by assuming a constant frequency of 60 Hz in the comparison plots. The positive SRF is set by:

$$\theta_1(t) = 2\pi 60.0t \quad (129)$$

and the negative SRF is set by:

$$\theta_2(t) = -2\pi 60.0t \quad (130)$$

Section 3.4 showed how the coupling of the positive and negative sequence SRFs signals results due to the transform of the three-phase signals to the SRF. A notch filter is used to remove the resulting 120 Hz sinusoidal component of the SRF and instantaneous power signals. This is implemented in the processing of the measured signals with a band stop filter using the signal processing toolbox of the SciPy library in Python [75]. The resonant frequency of the filter is set to 120 Hz and the bandwidth is set to 20 Hz. The filter is applied to the signals forward and backwards to eliminate phase distortion introduced by the filter.

#### **4.2.2. Symmetrical Faults**

This section compares the model prototype response in simulation to the laboratory test measurements for 3PH faults. Two 3PH fault tests are presented. The first is for a retained voltage of 0.3 pu at the 13.2 kV bus. The second is for a retained voltage of 0.5 pu at the 13.2 kV bus. The target values of retained voltage at the 13.2 kV bus are with the inverter under test disconnected. With the inverter online injecting reactive current, the resulting 13.2 kV bus voltage is higher as shown in the plots in this section.

#### 4.2.2.1. 3PH Fault with 0.3 pu Retained Voltage

Figure 4-10, Figure 4-11, and Figure 4-12 show comparisons of the calculated positive and negative sequence SRF components of the voltage and current, the instantaneous active and reactive power, and the three-phase voltage and current for a 3PH fault with 0.3 pu retained voltage at the 13.2 kV bus. Figure 4-10 shows by comparison of the positive and negative sequence SRF current signals that the model predicts the controlled response of the inverter. Figure 4-11 shows the same conclusion by comparison of the instantaneous active and reactive power.

During the transient in the current at fault inception and fault clearing, the laboratory measured current contains a larger magnitude compared to the model response in simulation. Figure 4-12 compares the three-phase current and Figure 4-13 further focuses on the three-phase current during the time interval of the fault inception. The comparison of the three-phase current shows that the difference in the model response compared to the measured response is mainly limited to approximately the first  $\frac{1}{4}$  cycle of the fundamental frequency period. An exponentially decaying DC offset in the laboratory-measured current is also present for approximately 200 ms following the start of the transient.

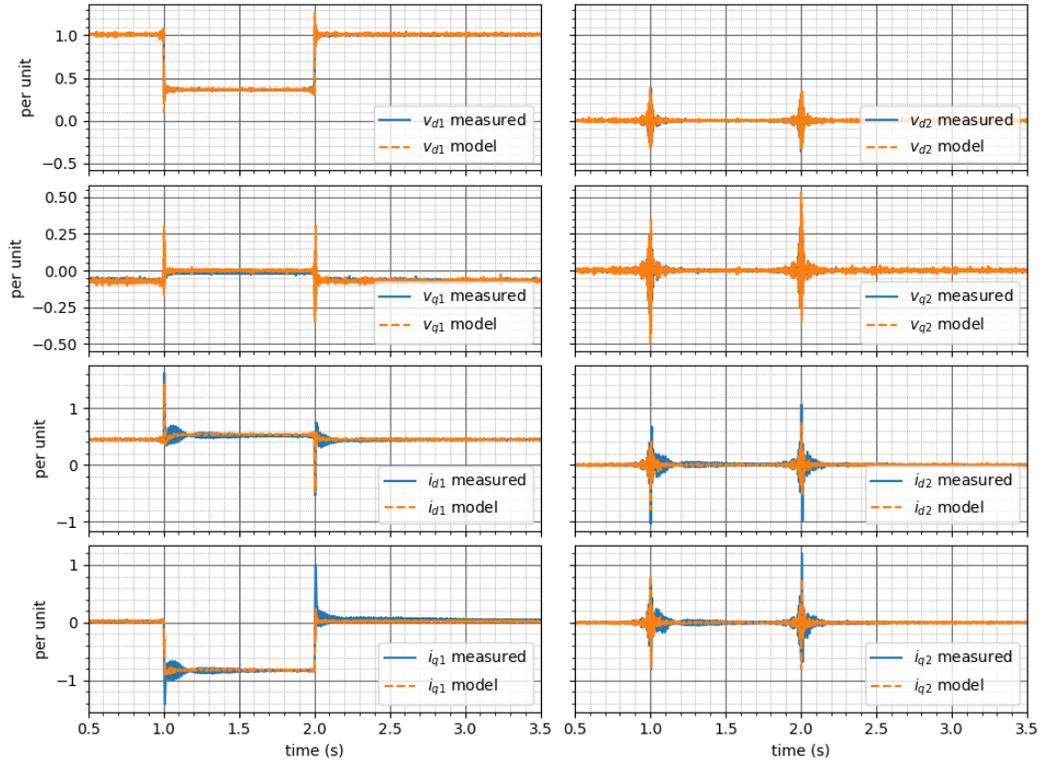


Figure 4-10. Positive and negative SRF components of the 13.2 kV voltage and current for a 3PH fault with 0.3 pu retained voltage.

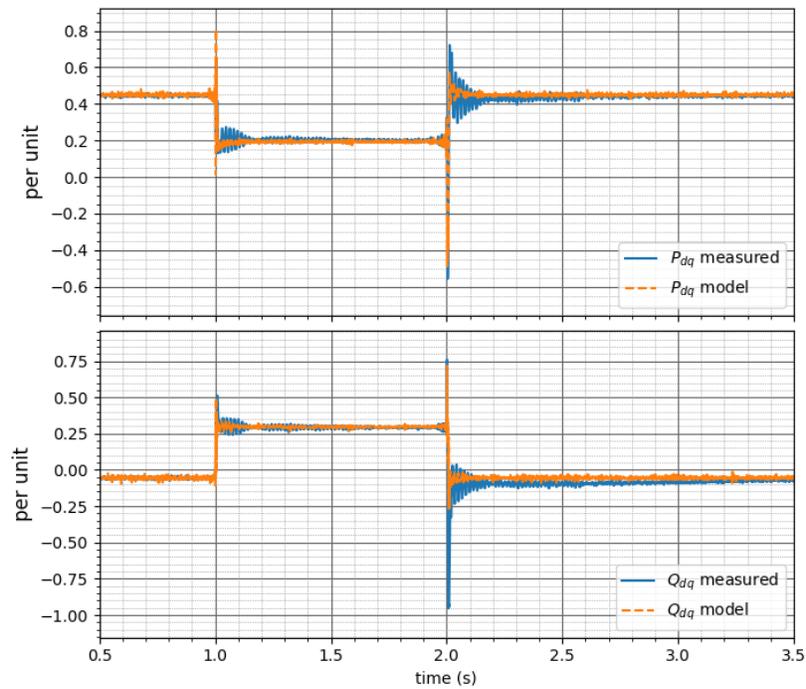


Figure 4-11. Instantaneous active and reactive power for a 3PH fault with 0.3 pu retained voltage.

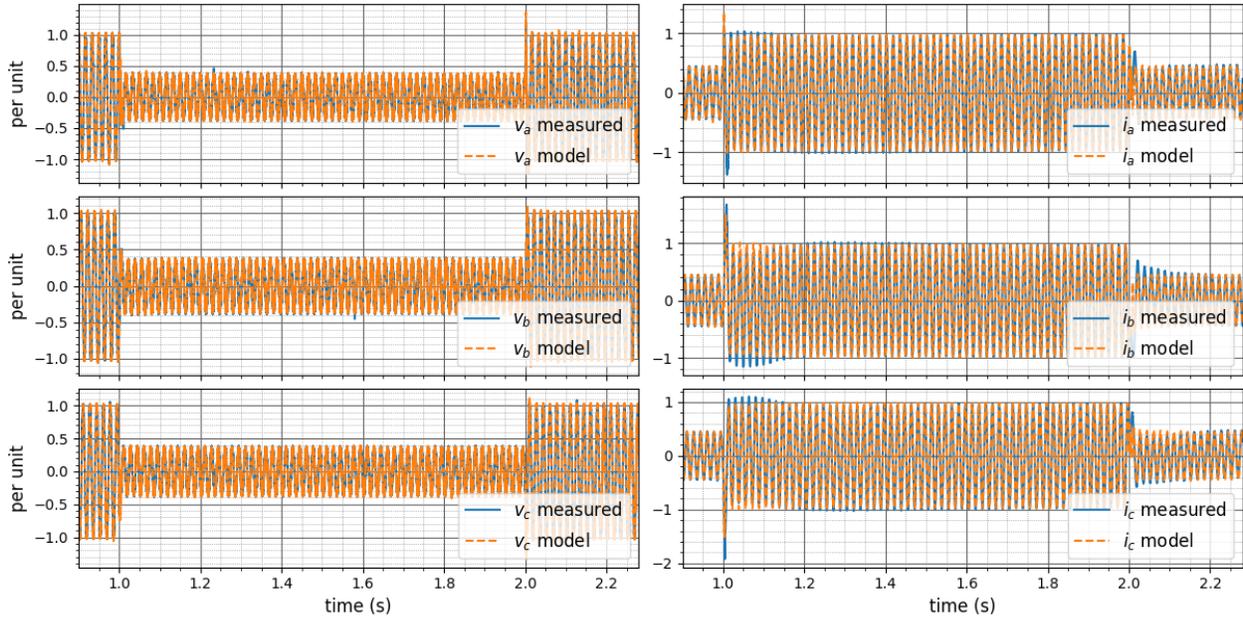


Figure 4-12. 13.2 kV three-phase voltage and current for a 3PH fault with 0.3 pu retained voltage.

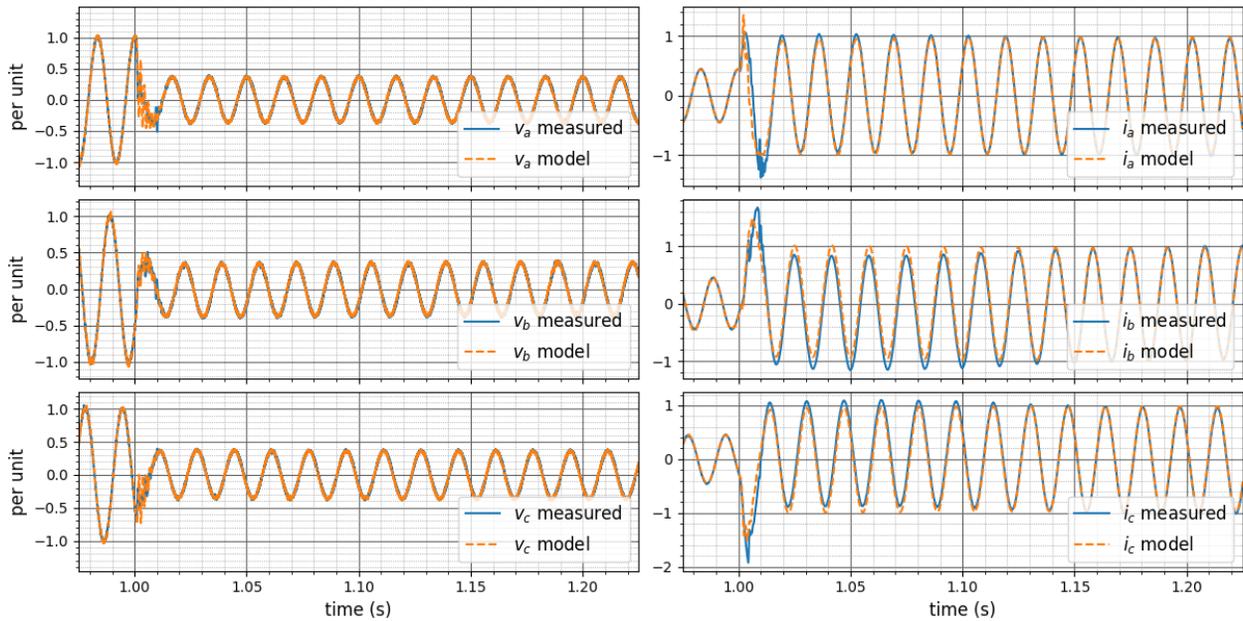


Figure 4-13. 13.2 kV three-phase voltage and current for a 3PH fault with 0.3 pu retained voltage zoomed in on the fault initiation.

Based on the observed decaying unidirectional component of the measured current in the laboratory tests, the signals are processed through a high pass filter (HPC) with a cut-off frequency

of 5 Hz for illustration purposes. The resulting filtered three-phase voltage and current are shown in Figure 4-14. The comparison of the signals passed through a HPF, forward and backwards, shows the primary difference in the model and measured signals is the decaying DC component.

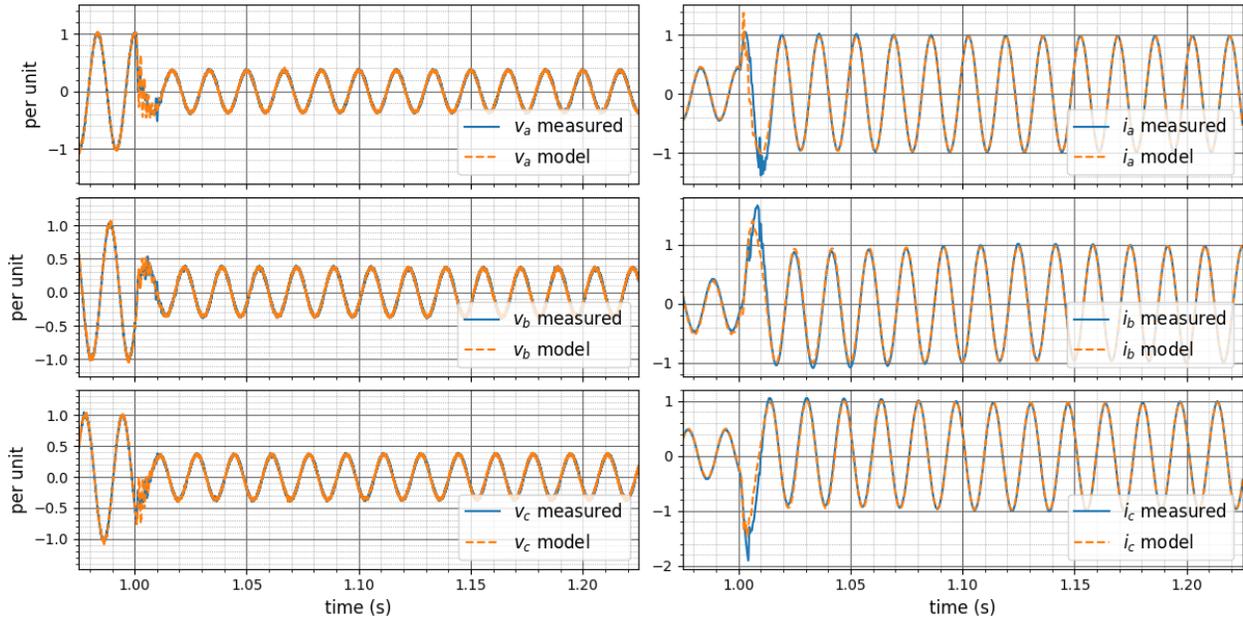


Figure 4-14. 13.2 kV measured voltage and current passed through a HPF forward and backwards with a cut-off frequency of 5 Hz for a 3PH fault with 0.3 pu retained voltage.

#### 4.2.2.2. 3PH Fault with 0.5 pu Retained Voltage

Figure 4-15, Figure 4-16, Figure 4-17, and Figure 4-18 show comparisons of the calculated positive and negative sequence SRF components of the voltage and current, the instantaneous active and reactive power, and the three-phase voltage and current for a 3PH fault with 0.5 pu retained voltage at the 13.2 kV bus. Figure 4-19 compares the three-phase current passed through a HPF. These plots show the same conclusions as for the tests with a 3PH fault with 0.3 pu retained voltage.

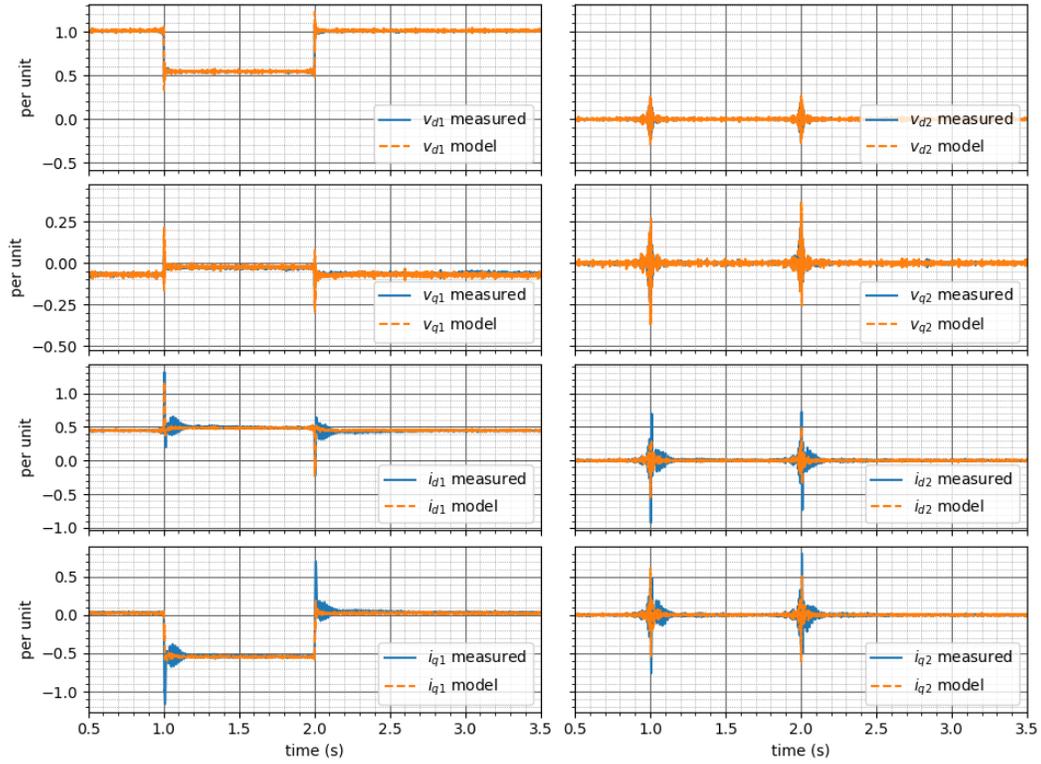


Figure 4-15. Positive and negative SRF components of the 13.2 kV voltage and current for a 3PH fault with 0.5 pu retained voltage.

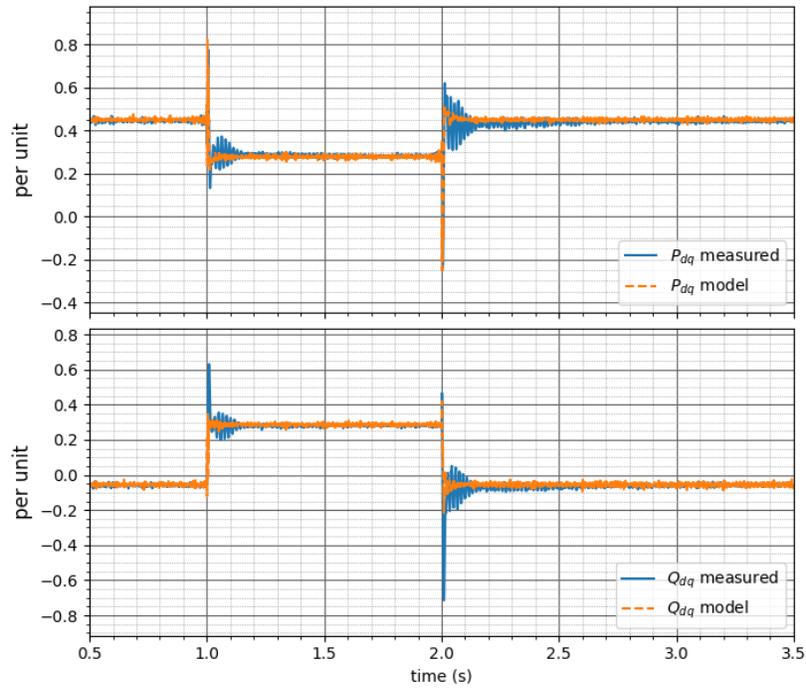


Figure 4-16. Instantaneous active and reactive power for a 3PH fault with 0.5 pu retained voltage.

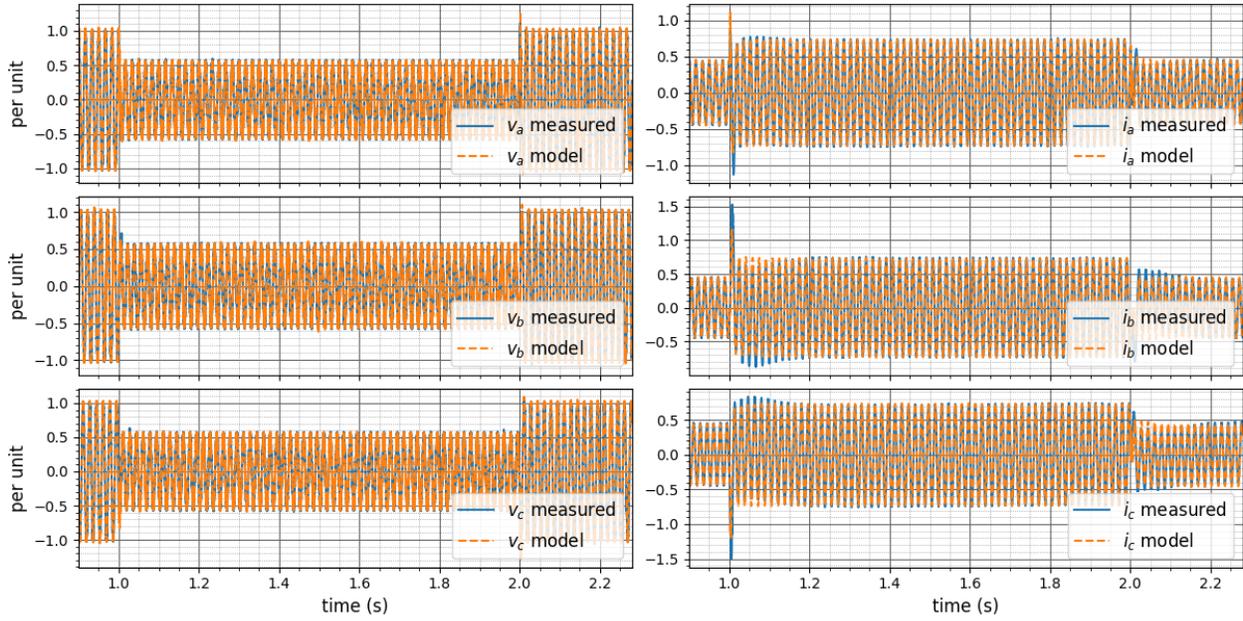


Figure 4-17. 13.2 kV three-phase voltage and current for a 3PH fault with 0.5 pu retained voltage.

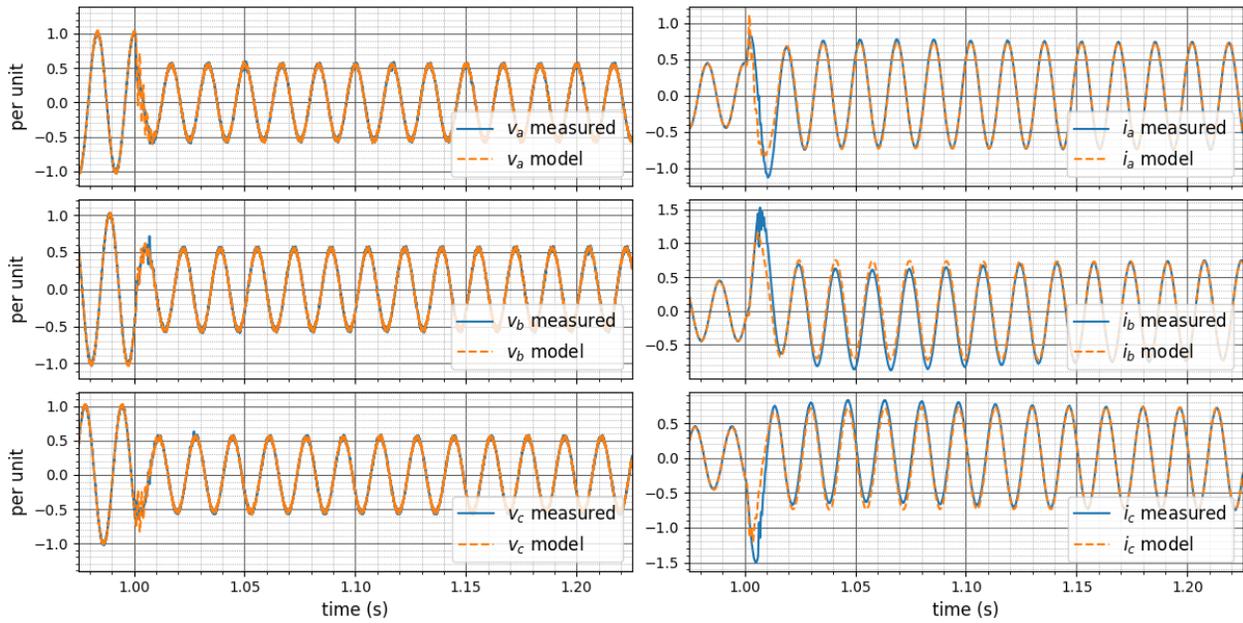


Figure 4-18. 13.2 kV three-phase voltage and current for a 3PH fault with 0.5 pu retained voltage zoomed in on the fault initiation.

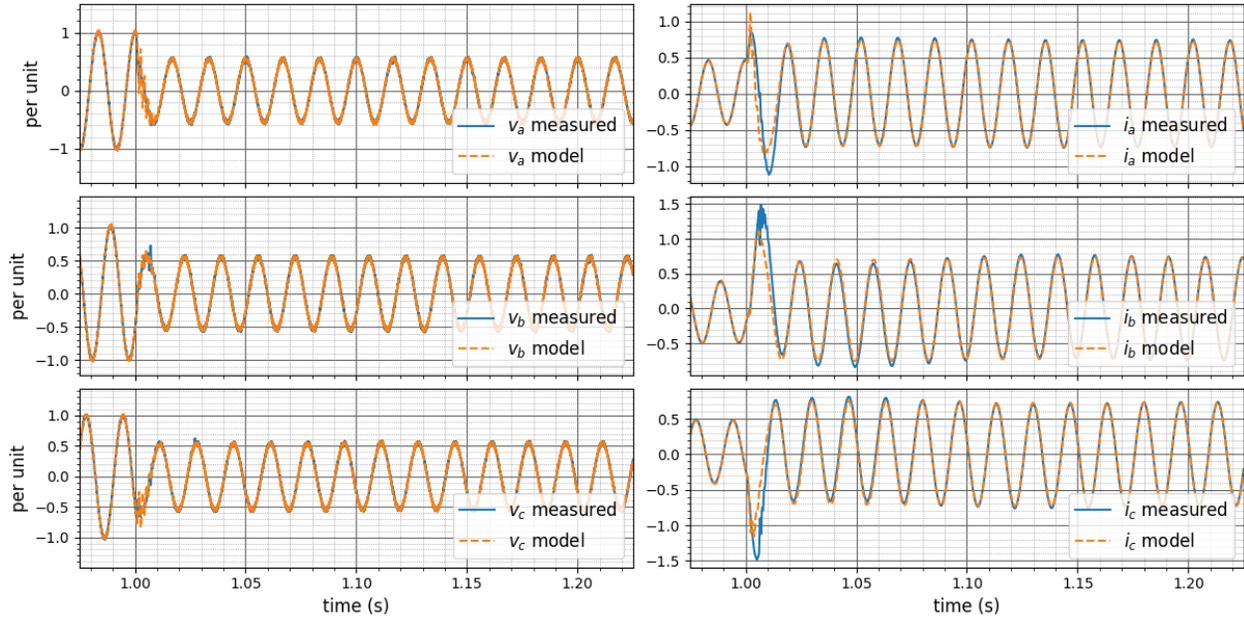


Figure 4-19. 13.2 kV measured voltage and current passed through a HPF forward and backwards with a cut-off frequency of 5 Hz for a 3PH fault with 0.5 pu retained voltage.

### 4.2.3. Asymmetrical Faults

This section compares the model prototype response in simulation to the laboratory test measurements for LL faults. Two LL fault tests are presented. The first is for a retained voltage of 0.3 pu between phase B and phase C voltage at the 13.2 kV bus. The second is for a retained voltage of 0.5 pu between phase B and phase C voltage at the 13.2 kV bus. The target values of retained voltage at the 13.2 kV bus are with the inverter under test disconnected.

#### 4.2.3.1. B-C Fault with 0.3 pu Retained Voltage

Figure 4-20, Figure 4-21, Figure 4-22, and Figure 4-23 show comparisons of the calculated positive and negative sequence SRF components of the voltage and current, the instantaneous active and reactive power, and the three-phase voltage and current for a B-C fault with 0.3 pu retained voltage at the 13.2 kV bus. These results show the inverter model can emulate the controlled current response of the commercial inverter in both the positive and negative sequences.

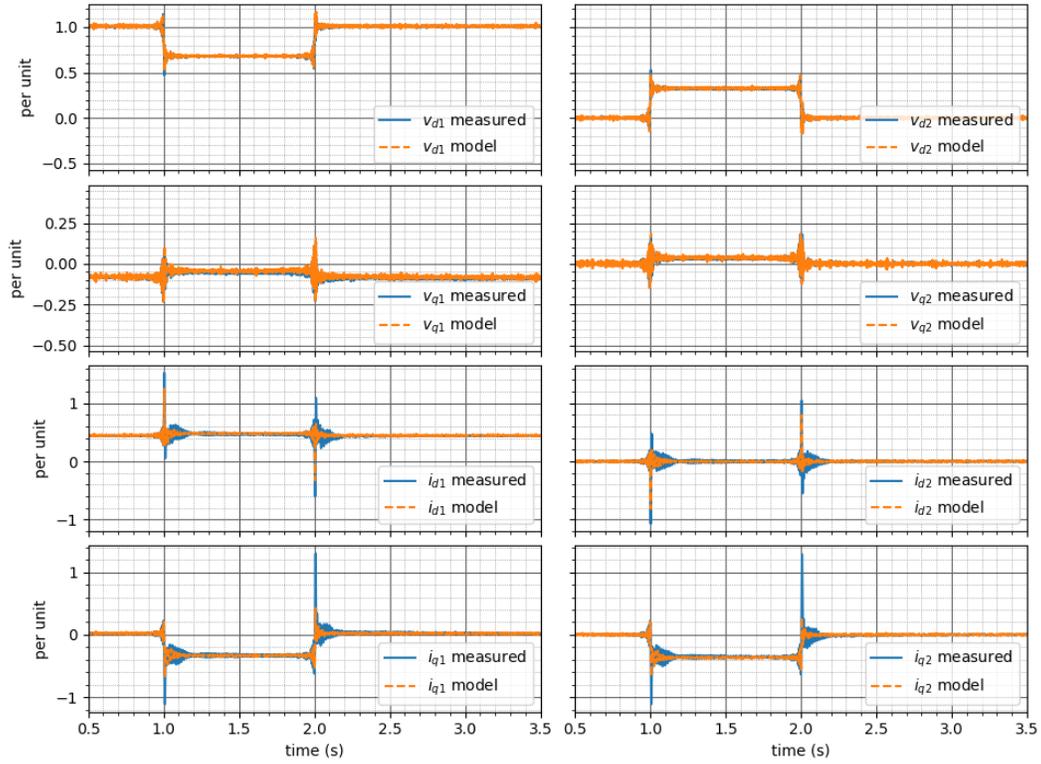


Figure 4-20. Positive and negative SRF components of the 13.2 kV voltage and current for a B-C fault with 0.3 pu retained  $V_{bc}$ .

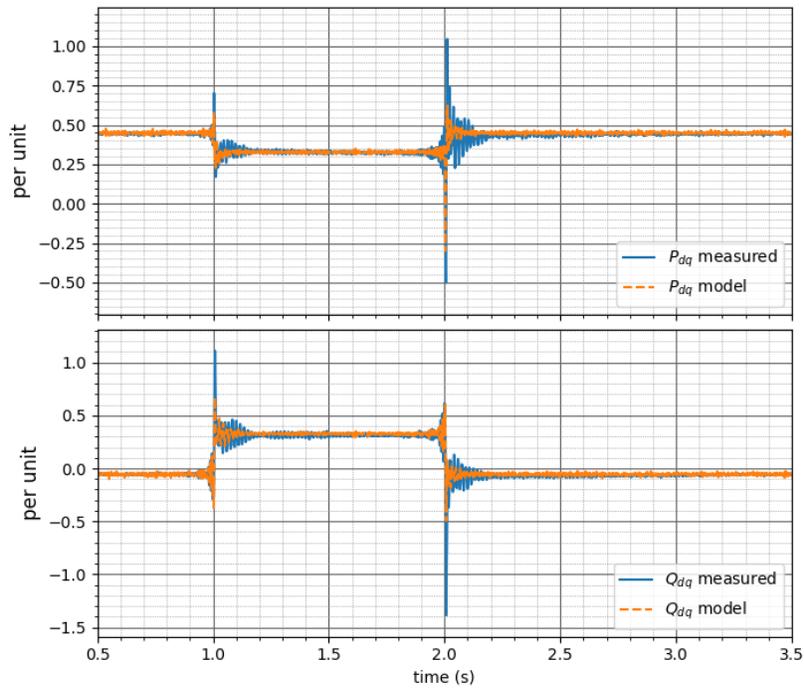


Figure 4-21. Instantaneous active and reactive power for a B-C fault with 0.3 pu retained  $V_{bc}$ .

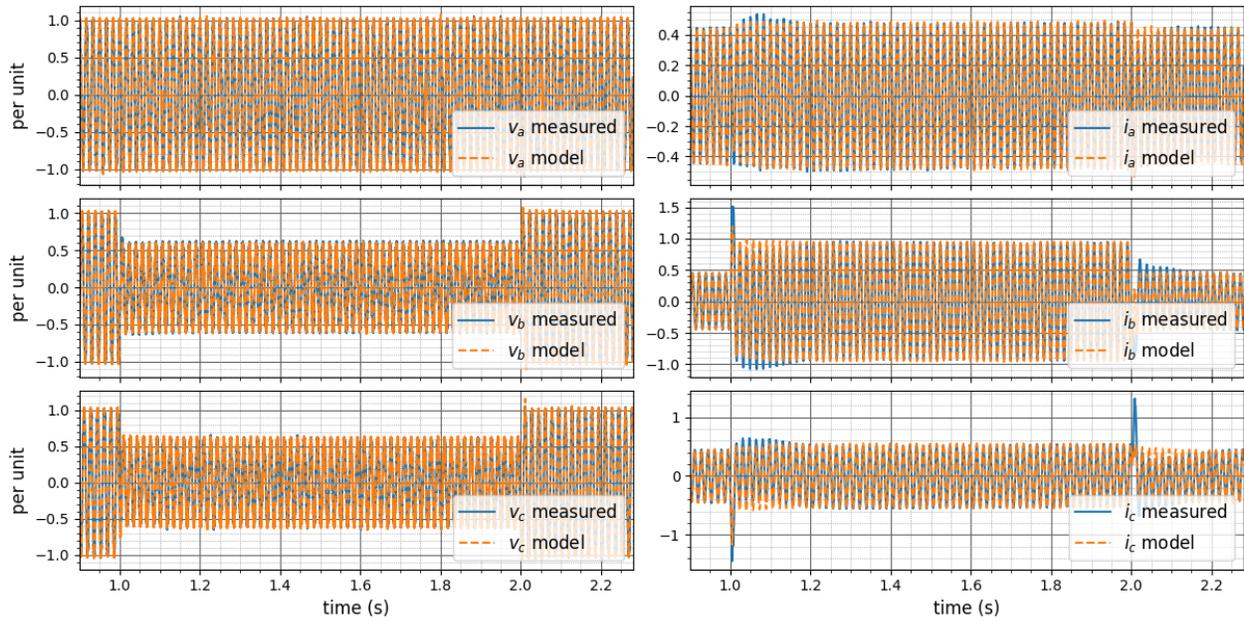


Figure 4-22. 13.2 kV three-phase voltage and current for a B-C fault with 0.3 pu retained  $V_{bc}$ .

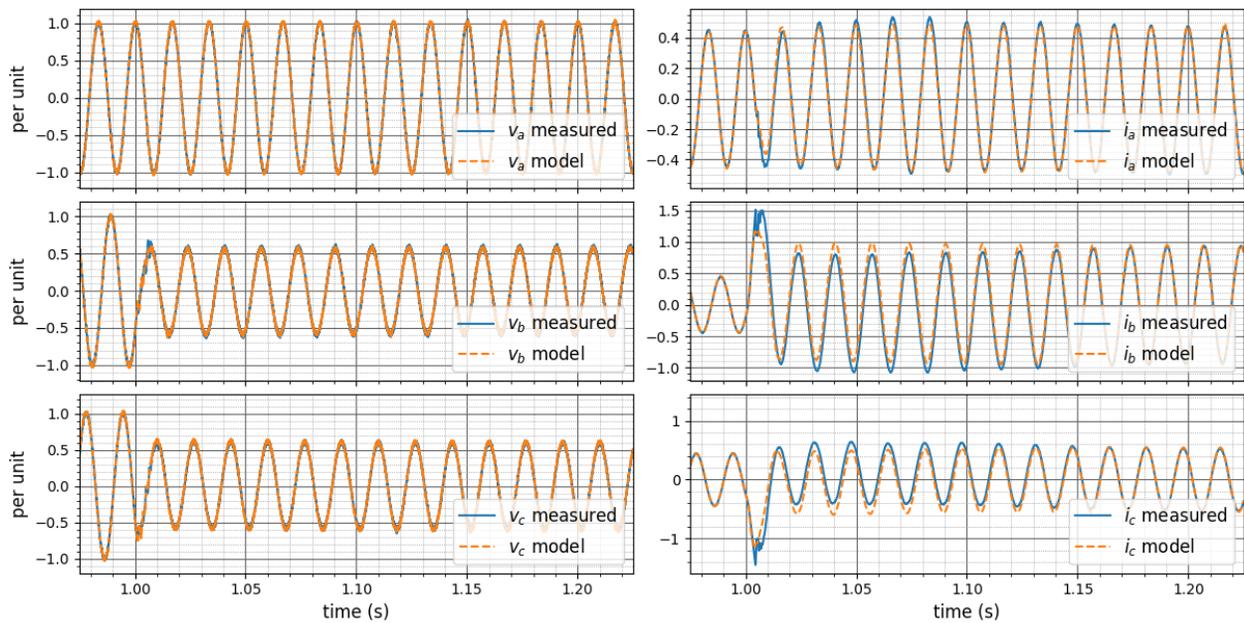


Figure 4-23. 13.2 kV three-phase voltage and current for a B-C fault with 0.3 pu retained  $V_{bc}$  zoomed in on the fault initiation.

Figure 4-24 compares the three-phase current passed through a HPF showing the main difference between the laboratory measurements and the simulation results is the exponentially decaying unidirectional component of the current.

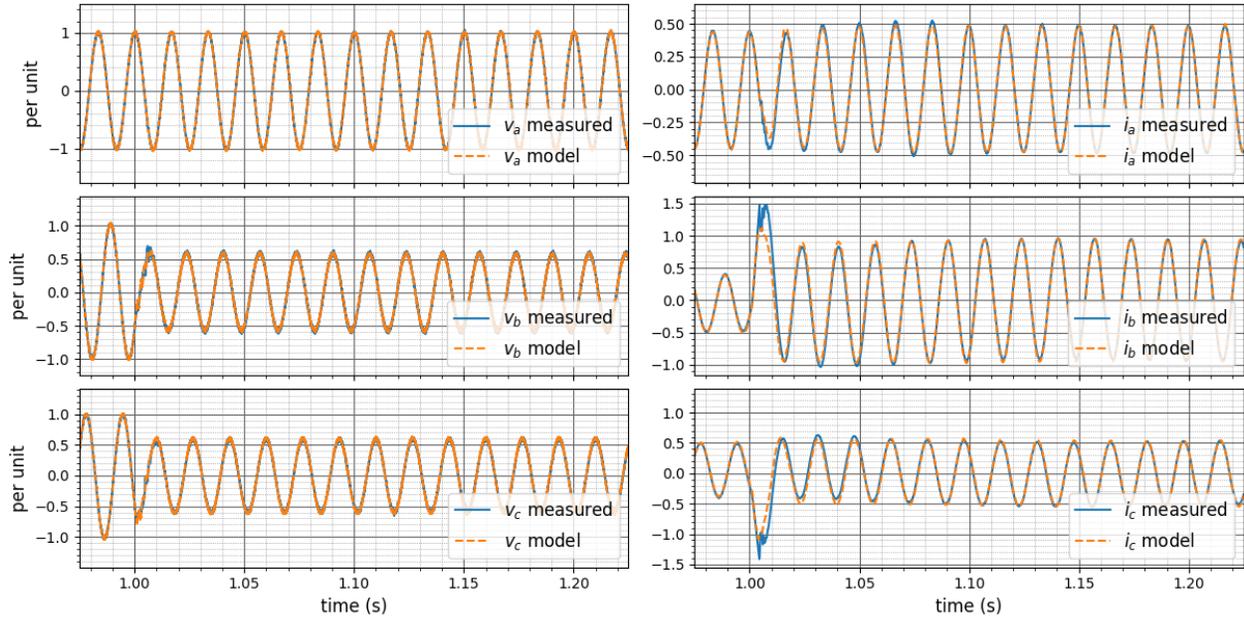


Figure 4-24. 13.2 kV measured voltage and current passed through a HPF forward and backwards with a cut-off frequency of 5 Hz for a B-C fault with 0.3 pu retained  $V_{bc}$ .

#### 4.2.3.2. B-C Fault with 0.5 pu Retained Voltage

Figure 4-25, Figure 4-26, Figure 4-27, and Figure 4-28 show comparisons of the calculated positive and negative sequence SRF components of the voltage and current, the instantaneous active and reactive power, and the three-phase voltage and current for a LL fault with 0.5 pu retained voltage at the 13.2 kV bus. Figure 4-29 compares the three-phase current passed through a HPF. These plots show the same conclusions as for the tests with a LL fault with 0.3 pu retained voltage.

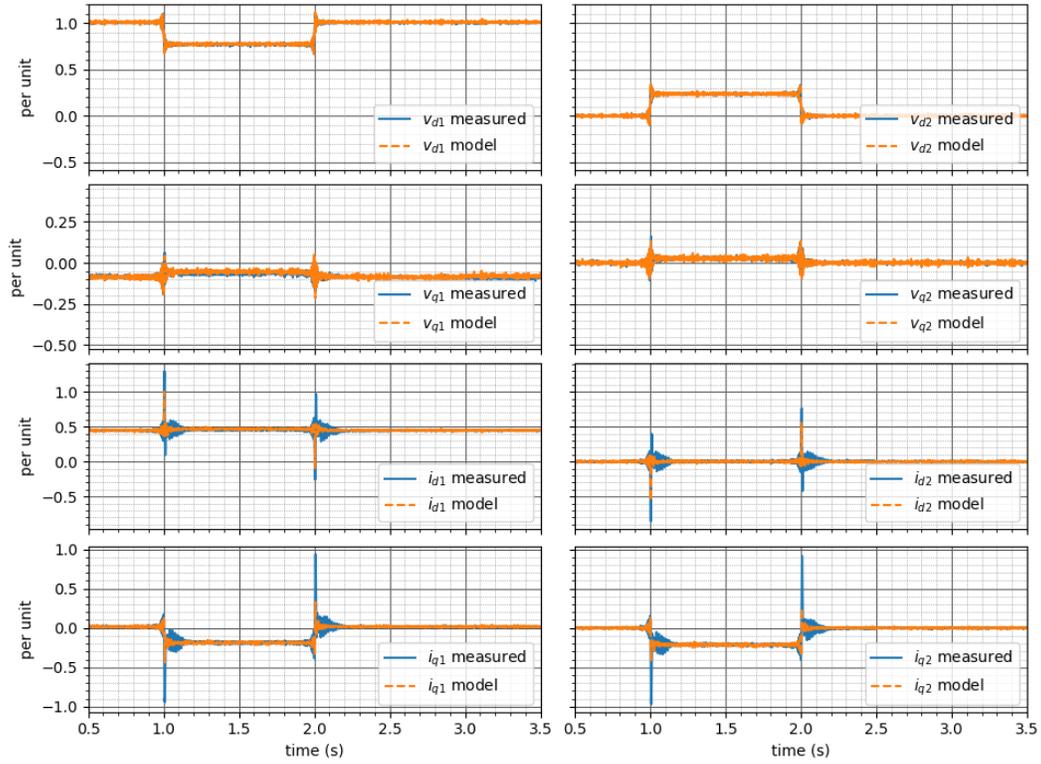


Figure 4-25. Positive and negative SRF components of the 13.2 kV voltage and current for a B-C fault with 0.5 pu retained  $V_{bc}$ .

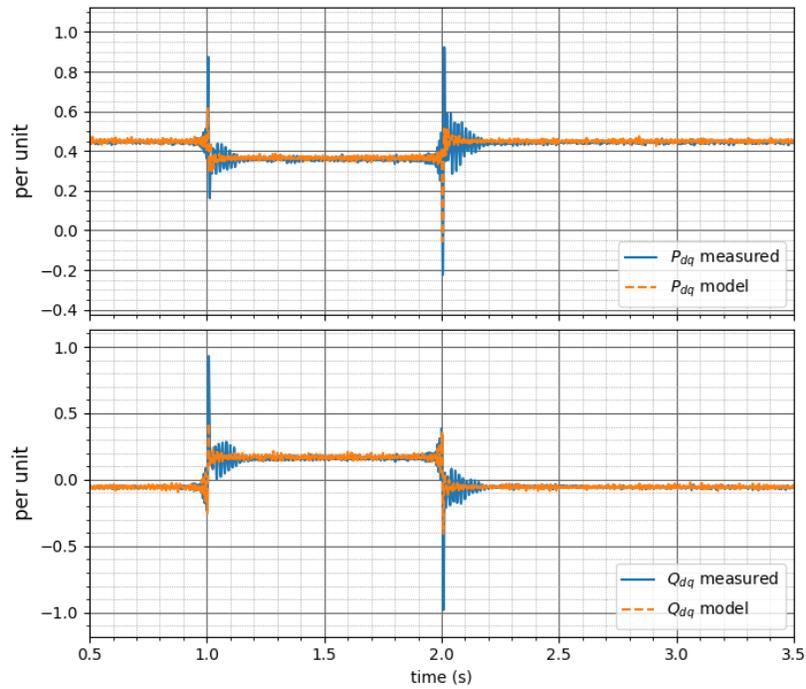


Figure 4-26. Instantaneous active and reactive power for a B-C fault with 0.5 pu retained  $V_{bc}$ .

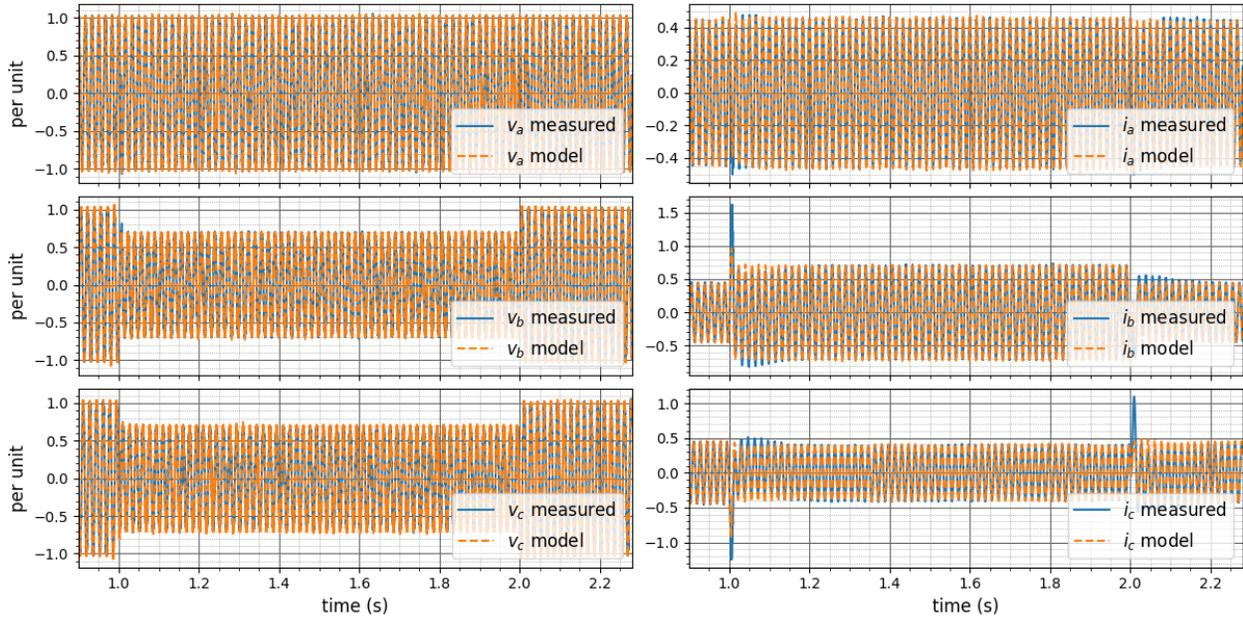


Figure 4-27. 13.2 kV three-phase voltage and current for a B-C fault with 0.5 pu retained  $V_{bc}$ .

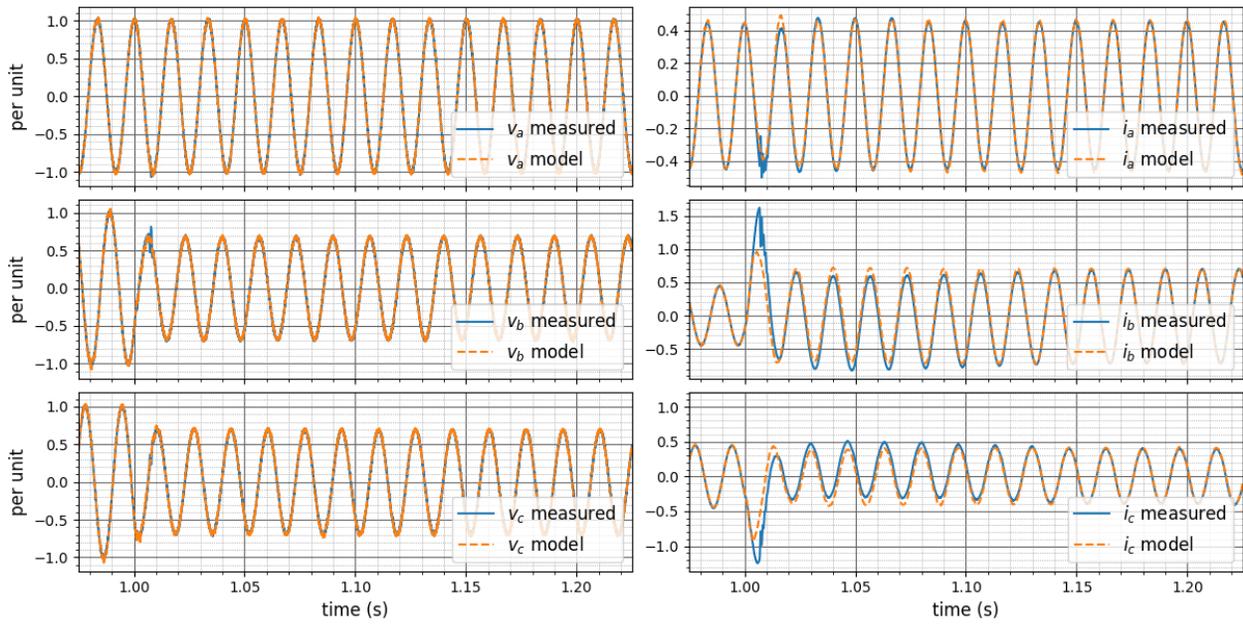


Figure 4-28. 13.2 kV three-phase voltage and current for a B-C fault with 0.5 pu retained  $V_{bc}$  zoomed in on the fault initiation.

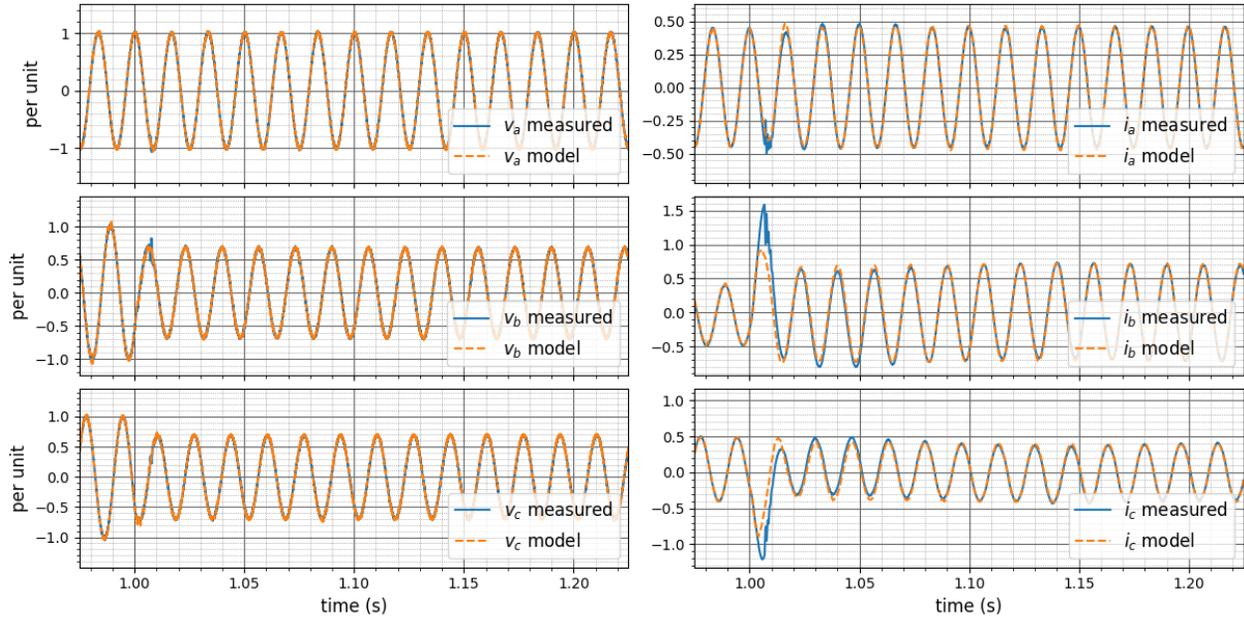


Figure 4-29. 13.2 kV measured voltage and current passed through a HPF forward and backwards with a cut-off frequency of 5 Hz for a B-C fault with 0.5 pu retained  $V_{bc}$ .

#### 4.2.4. Summary

The comparison of the model response to the laboratory test measurements shows that the model developed in this work can be configured to emulate the controlled response of the inverter tested. Test voltages representing both 3PH and LL faults with different dip magnitudes were considered to ensure model fidelity over a range of terminal voltage conditions. Two differences are noted comparing the laboratory measurements to the simulation results.

The first is the magnitude of the current upon a change in the test voltage. This is limited to approximately the first quarter cycle of the fundamental frequency period. Sensitivity analysis of the inverter model parameters indicates the initial current magnitude upon fault inception is sensitive to the inverter output filter inductance, current controller bandwidth, and point-on-wave of the voltage change.

The second is the decaying unidirectional component of the current present in the laboratory measurements. The laboratory currents were measured using a Rogowski coil with a specified accuracy of  $\pm 1\%$  of the measurement value, a phase shift of  $0.9 \pm 0.1$  degrees, and a -3dB bandwidth of 0.6 Hz to 1 MHz [76]. The current transducer used does not measure direct current [77], but the low end of its bandwidth may allow accurate representation of the decaying DC component. Another consideration is that Rogowski coils can show DC offset for large  $di/dt$  depending on the design [78].

The inverter under test's output filter type (e.g., L, LCL, LLC), control structure, and control configuration are unknown. The laboratory test measurements are at the MV side of the inverter step-up transformer. Detailed modeling parameters of the transformer are not available. Further, it is unclear if the response is an artifact of the measurement equipment. Therefore, it is not expected for the model to provide a perfect match at the initial onset of the fault without more information about the inverter under test. Precise measurements are needed at the inverter terminal, transformer modeling data, and potentially details of the inverter output filter and control design to investigate this response further.

Given the proprietary nature and range of possible inverter hardware, modulation approaches, control, and equipment-specific protection functions to protect the power electronics during the initial transient, if the initial transient of a specific inverter is of interest, an OEM-specific model is more appropriate. This section also shows the importance of modeling other components that may have an impact on the response, such as the inverter-step up transformer. However, the necessary level of detail is dependent on the phenomena of interest in the study. Large IBR plants may contain 100s of inverters, collection system cables and overhead lines, and multiple transformations, as discussed in Section 3.1. The initial transient at the inverter terminal is assumed

to have less influence on the overall aggregate response of the plant at the point of interconnection with the transmission system. It is currently common practice to aggregate the model of the inverter, even with highly detailed black-box OEM-specific models, and collection system in the interconnection study process. This highlights a use case of the inverter model prototype to investigate potential limitations in the present-day modeling approaches commonly used to study the impact of IBR on electric grids.

## 5. Conclusions and Future Work

This work develops a verified, generic EMT model of a current mode controlled PV inverter that meets the response performance requirements of the draft IEEE P2800 standard. The model prototype can also represent a storage inverter. Both a switching model and an averaged model of the VSC are implemented. The derivation of the averaged model representation of the VSC shows the potential used cases and limitations of the averaged model in terms of the frequency of the dynamics of interest. The design of each controller is presented along with the closed-loop small-signal model of the controller and the process. The LVRT control is developed to inject positive and negative sequence currents by control of the positive and negative sequence voltage. The LVRT response is verified to meet the performance requirements via simulation of both symmetrical and asymmetrical faults. Finally, the model prototype is verified by comparison to measurements from laboratory testing of a 2.2 MVA storage inverter.

At their base, models are mathematical representations that can be used to predict how the system will behave. Therefore, they are always an approximation of the system they are designed to represent. In this case, the system includes unknown control algorithms and hardware design. For this reason, the assumptions that went into the control design and model implementation are detailed in Chapter 2 and Chapter 3. The use cases of the model prototype are related to grid planning studies and research. A few examples include:

- Planning and futuristic studies where the exact equipment is yet to be specified or OEM-specific models are not available.
- Evaluation and development of IBR performance requirements.
- Insight into limitations and improvement of commonly used simplified models such as positive sequence transient stability and phasor domain short circuit models.

- Case studies of grids with high penetration levels of IBR.
- Development of tools to analyze the stability of grids with high penetration levels of IBR.

The contributions of this work are:

- A verified, generic inverter model prototype that can be used for PV and storage inverters applied to transmission connected IBR plants.
- An analytical tuning method for each controller in the model prototype such that the end-user can readily use it for different applications.
- A current limit logic to maintain the inverter output phase currents within the current limit accounting for both positive and negative sequence current injections. The logic ensures if the current limit is reached, the maximum allowable current is injected in at least one phase based on the target positive and negative sequence components while also implementing the specified prioritization of current.
- Insight into controller bandwidth limits based on required control of sequence components of the current.

The primary objective of this work is to provide a model that helps grid planners and researchers plan and design solutions for future grids with high penetration levels of IBR. The model developed in this research is in an EMT simulation platform to facilitate detailed modeling of the inverter's control. However, grid planners commonly evaluate grid stability using large cases (e.g., models of the complete interconnection) and evaluate numerous potential contingencies under different scenarios. Performing these assessments completely in an EMT simulator may not be feasible due to the increase in the computational burden, the data requirements, and the expertise required. Positive sequence transient stability tools are presently the main platform for these evaluations due to their computational efficiency. However, the underlying simplifications based on inherent properties of synchronous machines made to enhance the computational efficiency may not be appropriate for grids comprised of mostly IBR. Future work related to this research looks to use the model developed to identify limitations in positive

sequence transient simulation tools and models and investigate ways to extend their use. For example, the sequence data of the network can be used to extend these tools to facilitate a three-phase representation. This data may already be present in the simulation case if the case is also used for phasor domain short circuit analysis. Other future work related to this research will investigate screening tools and approaches that can limit the number of detailed EMT simulations by identifying scenarios where detailed analysis is needed. Finally, the small-signal models of the controllers developed in this work provided insight into control instability associated with different control approaches and the influence of the grid strength on the control performance and stability. Future work will continue expanding these models to provide insight into IBR control instability.

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## Appendix A Transformations

This section summarizes the various reference frames and associated transforms used in the analysis and control of the inverter in this work. These include space vectors in the stationary reference frame, vectors in a synchronous reference frame, and symmetrical components in the phasor domain. The following 3-phase signal is used to illustrate each reference frame and associated transform.

$$\begin{aligned}f_a(t) &= \hat{f}_a RE\{e^{j(\omega t + \phi_a)}\} = \hat{f}_a \cos(\omega t + \phi_a) \\f_b(t) &= \hat{f}_b RE\{e^{j(\omega t + \phi_b)}\} = \hat{f}_b \cos(\omega t + \phi_b) \\f_c(t) &= \hat{f}_c RE\{e^{j(\omega t + \phi_c)}\} = \hat{f}_c \cos(\omega t + \phi_c)\end{aligned}\tag{131}$$

### Space Vector

The space vector of the 3-phase signals is given by:

$$\vec{f}(t) = \frac{2}{3} \{f_a(t)e^{j0} + f_b(t)e^{j2\pi/3} + f_c(t)e^{-j2\pi/3}\}\tag{132}$$

The scaling factor of  $2/3$  corresponds to the peak value of the space vector. Other scaling factors are commonly used such as  $\sqrt{2}/3$  to represent RMS values and  $\sqrt{2/3}$  to maintain power invariance. If the three-phase signals are balanced, the space vector reduces to:

$$\vec{f}(t) = \hat{f}_a e^{j(\omega t + \phi_a)} = \sqrt{2} |\mathbf{F}_1| e^{j(\omega t + \angle \mathbf{F}_1)}\tag{133}$$

### Clarke Transform

The Clarke transform [79] converts signals between the ABC reference frame and the  $\alpha\beta 0$  stationary reference frame. The zero-sequence component is ignored in this work based on the

inverter being a 3-phase, 3-wire system. If a 3-phase, 4-wire system is present, the zero-sequence component will have to be considered.

$$\begin{bmatrix} f_\alpha(t) \\ f_\beta(t) \\ f_0(t) \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} f_a(t) \\ f_b(t) \\ f_c(t) \end{bmatrix} \quad (134)$$

$$\begin{bmatrix} f_a(t) \\ f_b(t) \\ f_c(t) \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & 1 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & 1 \end{bmatrix} \begin{bmatrix} f_\alpha(t) \\ f_\beta(t) \\ f_0(t) \end{bmatrix} \quad (135)$$

The  $\alpha\beta$  representation of the three-phase signal, ignoring the zero-sequence component, is equivalent to the space vector representation.

$$\mathbf{f}(t) = f_\alpha(t) + jf_\beta(t) \quad (136)$$

### Park Transform

The Park transform [80] converts signals between the ABC reference frame or the  $\alpha\beta 0$  stationary reference frame and a synchronous reference frame aligned with  $\theta(t)$ . The conversion between ABC and dq0 is given by:

$$\begin{bmatrix} f_d(t) \\ f_q(t) \\ f_0(t) \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos(\theta) & \cos(\theta - 120) & \cos(\theta + 120) \\ -\sin(\theta) & -\sin(\theta - 120) & -\sin(\theta + 120) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} f_a(t) \\ f_b(t) \\ f_c(t) \end{bmatrix} \quad (137)$$

$$\begin{bmatrix} f_a(t) \\ f_b(t) \\ f_c(t) \end{bmatrix} = \begin{bmatrix} \cos(\theta) & -\sin(\theta) & 1 \\ \cos(\theta - 120) & -\sin(\theta - 120) & 1 \\ \cos(\theta + 120) & -\sin(\theta + 120) & 1 \end{bmatrix} \begin{bmatrix} f_a(t) \\ f_q(t) \\ f_0(t) \end{bmatrix} \quad (138)$$

The scaling factor of 2/3 corresponds to the peak value of the space vector.

The conversion between ABC and  $\alpha\beta 0$  is given by:

$$\begin{bmatrix} f_a(t) \\ f_q(t) \\ f_0(t) \end{bmatrix} = \begin{bmatrix} \cos(\theta) & \sin(\theta) & 0 \\ -\sin(\theta) & \cos(\theta) & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} f_\alpha(t) \\ f_\beta(t) \\ f_0(t) \end{bmatrix} \quad (139)$$

$$f_a(t) + jf_q(t) = [f_\alpha(t) + jf_\beta(t)]e^{-j\theta(t)} \quad (140)$$

$$\begin{bmatrix} f_\alpha(t) \\ f_\beta(t) \\ f_0(t) \end{bmatrix} = \begin{bmatrix} \cos(\theta) & -\sin(\theta) & 0 \\ \sin(\theta) & \cos(\theta) & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} f_d(t) \\ f_q(t) \\ f_0(t) \end{bmatrix} \quad (141)$$

$$[f_d(t) + jf_q(t)]e^{j\theta(t)} = f_\alpha(t) + jf_\beta(t) \quad (142)$$

Note that the Park transform and the Clarke transform are equivalent if the Park transform angle  $\theta(t) = 0$ .

For the control of the inverter in this work, the angle used for the Park transform is determined by the PLL. The PLL is designed to track the fundamental frequency positive sequence component of the grid voltage such that:

$$\theta(t) = \theta_{PLL}(t) = \omega t + \angle \mathbf{V}_1. \quad (143)$$

where  $\angle \mathbf{V}_1$  is the phase angle of the positive sequence component of the phase A voltage.

Consider the space vector of a signal with a DC component, a fundamental component, and harmonic components.

$$\mathbf{f}(t) = f_{dc} + f_1 e^{j\omega_1 t} + \sum_{h=2}^{\infty} f_h e^{j\omega_h t} \quad (144)$$

Transforming to the SRF set by the fundamental frequency implies a multiplication by  $\exp(-j\omega_1 t)$ . The SRF signals given by:

$$\mathbf{f}_{dq} = f_{dc} e^{-j\omega_1 t} + f_1 + \sum_{h=2}^{\infty} f_h e^{j(\omega_h - \omega_1)t} \quad (145)$$

In the SRF, the DC component of the space vector is a sinusoid at the fundamental frequency, the fundamental component is DC, and all harmonics are sinusoids at the harmonic frequency minus the fundamental frequency.

### Symmetrical Components

The method of symmetrical components is based on the classic paper by Fortescue [81] that showed a system of n-phasors can be resolved into n-systems of balanced phasors. For a three-phase system, the positive, negative, and zero sequence components are related by:

$$\begin{bmatrix} \mathbf{F}_a \\ \mathbf{F}_b \\ \mathbf{F}_c \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ \mathbf{a}^2 & \mathbf{a} & 1 \\ \mathbf{a} & \mathbf{a}^2 & 1 \end{bmatrix} \begin{bmatrix} \mathbf{F}_{a1} \\ \mathbf{F}_{a2} \\ \mathbf{F}_{a0} \end{bmatrix} \quad (146)$$

$$\begin{bmatrix} \mathbf{F}_{a1} \\ \mathbf{F}_{a2} \\ \mathbf{F}_{a0} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & \mathbf{a} & \mathbf{a}^2 \\ 1 & \mathbf{a}^2 & \mathbf{a} \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} \mathbf{F}_a \\ \mathbf{F}_b \\ \mathbf{F}_c \end{bmatrix} \quad (147)$$

$$\mathbf{F}_{b1} = \mathbf{a}^2 \mathbf{F}_{a1} \quad (148)$$

$$\mathbf{F}_{c1} = \mathbf{a} \mathbf{F}_{a1}$$

$$\mathbf{F}_{b2} = \mathbf{a}\mathbf{F}_{a2} \quad (149)$$

$$\mathbf{F}_{c2} = \mathbf{a}^2\mathbf{F}_{a2}$$

$$\mathbf{a} = (1\angle 120) = (1\angle -240) = -\frac{1}{2} + j\frac{\sqrt{3}}{2} \quad (150)$$

$$\mathbf{a}^2 = (1\angle 240) = (1\angle -120) = -\frac{1}{2} - j\frac{\sqrt{3}}{2}$$

This approach is based on the frequency domain representation of the signal at a given frequency. For example, the phasor representation of the fundamental frequency component  $\omega_1$  of  $f(t)$  can be written as:

$$f(\omega_1) = |f(\omega_1)|\angle f(\omega_1) \quad (151)$$

Note that this representation is valid during steady-state for the stated frequency.

### Time-domain Symmetrical Components

The space vector notation can be used to relate the time-domain signals to symmetrical components. Consider the 3-phase signals in a 3-wire system written as a superposition of the positive and negative sequence components.

$$\begin{aligned} f_a(t) &= \sqrt{2}|F_1|\cos(\omega t + \phi_{a1}) + \sqrt{2}|F_2|\cos(\omega t + \phi_{a2}) \\ f_b(t) &= \sqrt{2}|F_1|\cos(\omega t - 120^\circ + \phi_{a1}) + \sqrt{2}|F_2|\cos(\omega t + 120^\circ + \phi_{a2}) \\ f_c(t) &= \sqrt{2}|F_1|\cos(\omega t + 120^\circ + \phi_{a1}) + \sqrt{2}|F_2|\cos(\omega t - 120^\circ + \phi_{a2}) \end{aligned} \quad (152)$$

Transforming the positive sequence components to the  $\alpha\beta$  reference frame results in:

$$f_{\alpha\beta 1}(t) = \sqrt{2}|F_1|e^{j(\omega t + \phi_{a1})} \quad (153)$$

Transforming negative sequence components to the  $\alpha\beta$  reference frame results in:

$$\mathbf{f}_{\alpha\beta 2}(t) = \sqrt{2}|\mathbf{F}_2|e^{-j(\omega t + \phi_{a2})} \quad (154)$$

The  $\alpha\beta 0$  components are related to the symmetrical components by:

$$\begin{aligned} f_{\alpha}(t) &= f_1(t) + f_2(t) \\ f_{\beta}(t) &= -j[f_1(t) - f_2(t)] \\ f_0(t) &= f_0(t) \end{aligned} \quad (155)$$

$$\begin{aligned} f_1(t) &= \frac{1}{2}[f_{\alpha}(t) + jf_{\beta}(t)] \\ f_2(t) &= \frac{1}{2}[f_{\alpha}(t) - jf_{\beta}(t)] \\ f_0(t) &= f_0(t) \end{aligned} \quad (156)$$

The sequence components can also be related to the positive and negative sequence SRFs. The positive sequence SRF is established by the PLL tracking the positive sequence fundamental frequency component of the grid voltage at the inverter terminal. Multiplying by  $\exp[-j(\omega t + \angle \mathbf{V}_1)]$  gives the positive SRF component.

$$\mathbf{f}_{dq1}(t) = \sqrt{2}|\mathbf{F}_1|e^{j(\phi_{a1} - \angle \mathbf{V}_1)} \quad (157)$$

The negative sequence SRF is established by taking the negative of the angle determined by the PLL. Multiplying by  $\exp[j(\omega t + \angle \mathbf{V}_1)]$  gives the negative SRF component.

$$\mathbf{f}_{dq2}(t) = \sqrt{2}|\mathbf{F}_2|e^{j(\angle \mathbf{V}_1 - \phi_{a2})} \quad (158)$$

The phasor domain can be transformed to the time-domain based on knowledge of previous values of the signal by noting  $\mathbf{a}$  corresponds to 1/3 of the period of the frequency for which the

phasor is defined [72]. In this case, the negative phase shift of  $\mathbf{a}$  must be considered as the future value of the signal is unknown.

$$\begin{aligned}
 f_1(t) &= \frac{1}{3} \left[ f_a(t) + f_b \left( t - \frac{2}{3}T \right) + f_c \left( t - \frac{1}{3}T \right) \right] \\
 f_2(t) &= \frac{1}{3} \left[ f_a(t) + f_b \left( t - \frac{1}{3}T \right) + f_c \left( t - \frac{2}{3}T \right) \right] \\
 f_0(t) &= \frac{1}{3} [f_a(t) + f_b(t) + f_c(t)]
 \end{aligned} \tag{159}$$

Note that the time-domain calculations are based on previous values of the signal up to 2/3 of a period of the signal frequency.

## Appendix B Voltage Mode Control

Voltage mode control of the VSC can be illustrated by considering the diagram of the inverter connected to a simple grid equivalent in Figure 3-2. The active and reactive power flow can be described in the phasor domain as:

$$P_{inv} = \frac{|E||V_t|}{X} \sin(\angle E - \angle V_t) \quad (160)$$

$$Q_{inv} = \frac{|E|^2}{X} - \frac{|E||V_t|}{X} \cos(\angle E - \angle V_t) \quad (161)$$

This relationship can be used to directly determine the voltage reference of the inverter,  $E^*$  as shown in Figure B-1. The phase angle of the inverter voltage is modulated to control the active power. The magnitude of the inverter voltage is used to control the reactive power. Given the inverter control is implemented in the time domain, a reference frequency is also needed.

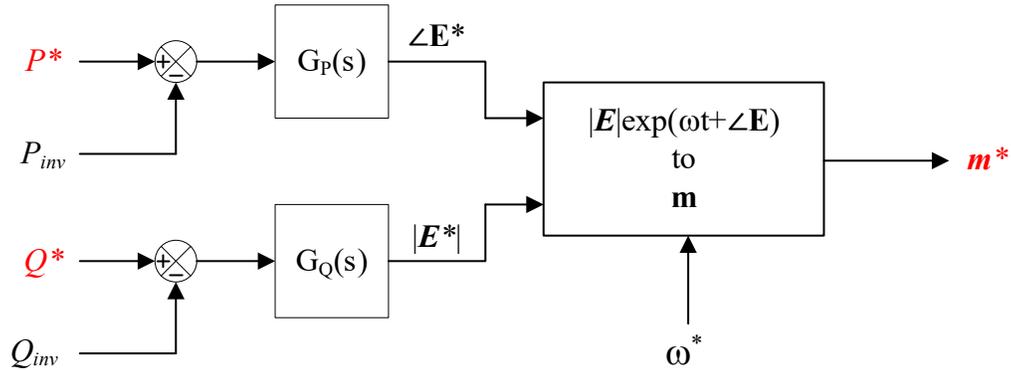


Figure B-1. Example structure of voltage mode control of the VSC.

Voltage mode control is the basis for what is referred to in the literature as grid-forming control. This is due to the control generating a voltage reference directly based on the control objective [82]. In contrast, grid-following control develops a current reference based on the control

objective and knowledge of the grid voltage (magnitude, frequency, and phase). The interested reader is referred to [83] for more detail on grid-forming control structures.

## Appendix C Linear Control

### Second-Order System

Most of the controllers in this work are implemented as PI compensators. Pole-placement is used to shape the desired dynamics of the closed-loop response. In the case of the 2<sup>nd</sup> order system, this allows the gains to be tuned based on the desired natural frequency and damping of the system. This results in matching coefficients of the analytically derived model and the standard form of a 2<sup>nd</sup> order system given by:

$$H(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (162)$$

In order to relate these parameters to the system rise time or bandwidth, the undamped natural frequency can be estimated based on the desired rise time estimated as shown in [51] as:

$$\omega_n \cong \frac{1.8}{t_r} \quad (163)$$

where  $t_r$  is the rise time and  $\omega_n$  is the undamped natural frequency. The closed-loop bandwidth,  $f_{BW}$ , can be estimated by:

$$f_{BW} \cong \frac{0.35}{t_r} \quad (164)$$

Therefore, given a target rise time, or bandwidth, and damping, the corresponding PI gains can be calculated by equating the closed-loop linearized model transfer function to the 2<sup>nd</sup> order transfer function in (162). This results in a systematic tuning approach for each controller that can be readily implemented by the end-user of the model for different applications. Ultimately, the

response must be verified with the full model due to nonlinearities and the numerous assumptions taken to reduce each controller to a SISO system.

### Setpoint Weighting

Most of the closed-loop models derived in this work are not in the standard form because they include a zero. The influence of a zero close to a pole is to reduce to decrease the rise time and increase the overshoot. This is due to the derivative term in the time response, as shown in [51]. Considering the example where the plant is an integrator, the resulting transfer function after the pole-placement process is:

$$\frac{Y(s)}{R(s)} = \frac{k_p s + k_i}{s^2 + k_p s + k_i} \quad (165)$$

Splitting into a superposition of the standard form:

$$\frac{Y(s)}{R(s)} = \frac{k_i}{s^2 + k_p s + k_i} \left( \frac{k_p s}{k_i} \right) + \frac{k_i}{s^2 + k_p s + k_i} \quad (166)$$

Therefore, the zero ( $s_z = -k_i/k_p$ ) quantifies the impact of the zero which is the derivative of the target response.

Chapter 8 of [84] provides an overview of common modifications to the PID structure. One of these modifications, setpoint weighting, is used in the model prototype to reduce the influence of the zero. In this approach shown in Figure C-1, the reference setpoint and the feedback of the controlled signal are treated separately. This structure allows the system to respond the same for disturbances but respond differently for setpoint changes, minimizing the influence of the zero [42].

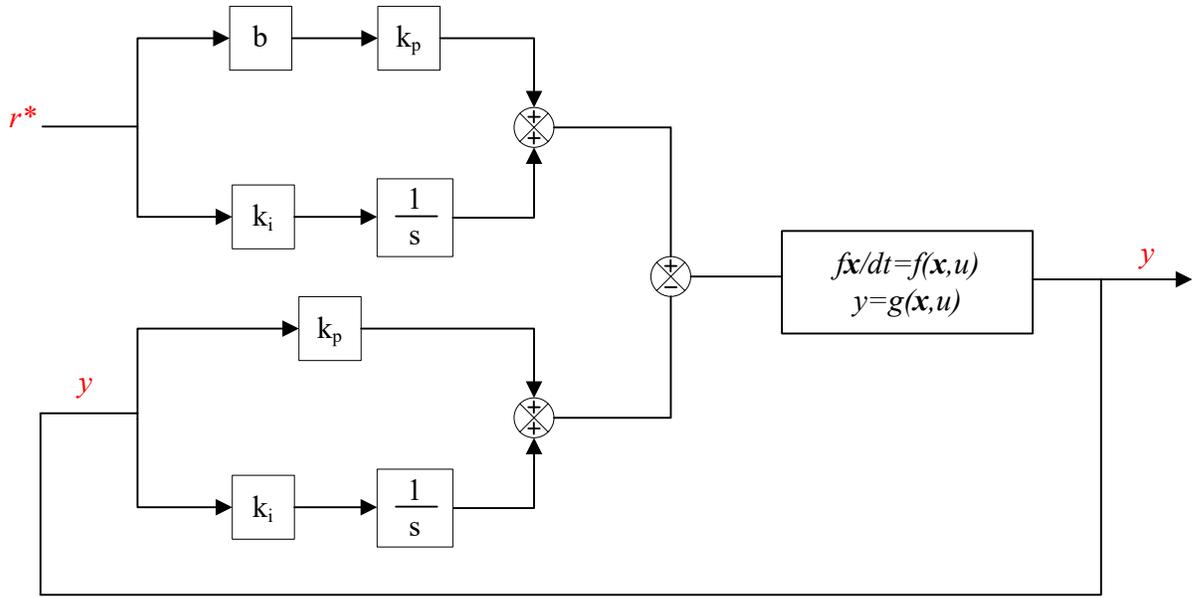


Figure C-1. PI structure with setpoint weighting.

For the pole-placement approach taken in this work, it is recommended by the authors in [42] to use the weighting factor to move the zero to the left of the dominant pole. Given that the tuning procedure used sets the natural frequency based on the desired rise time or bandwidth of the system, following the approach in [42], the weighting factor on the reference setpoint proportional gain is set as:

$$b = \frac{k_i}{k_p \omega_n} \quad (167)$$

### Integrator Windup

The PI controllers implemented in the model prototype incorporate the anti-windup mechanism shown in Figure C-2. This prevents the continued integration of the error signal when the output has reached a limit.

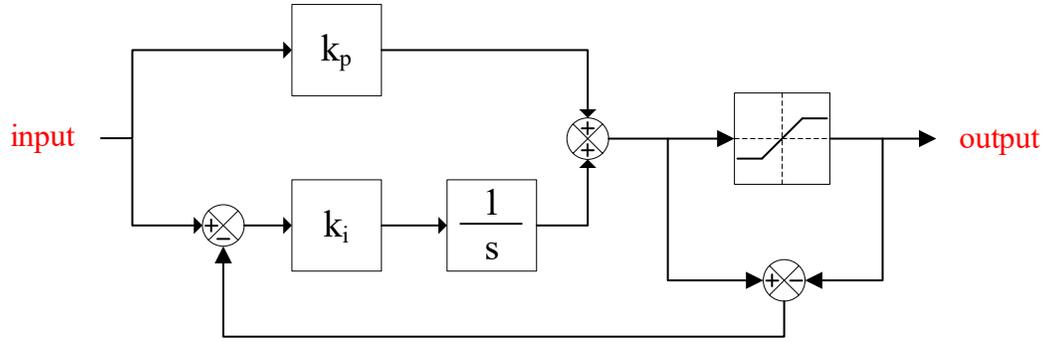


Figure C-2. PI controller with anti-windup.

### Linearization

Most of the controllers implemented in this work have nonlinearities. Considering only the average model representation of the inverter, i.e., neglecting the switching of the power electronics, many of the nonlinearities appear as sinusoidal terms, dead-bands, ramp-rate limiters, and amplitude limiters. Other nonlinearities in the inverter control are related to control mode switching, e.g., switching to FRT control mode during abnormal conditions. The models are linearized to apply linear analysis and control techniques. However, it is important to keep in mind the type of nonlinearities present. For example, many of the nonlinearities in the model are discontinuous and cannot be linearized. Therefore, the controller design and analysis by linear techniques are supplemented with time-domain simulations of the full model including the nonlinearities. The linearization approach used is based on linearization by small-signal analysis following the procedure outlined in Chapter 3 of [85] and Chapter 9 of [51]. For reference, the linearization process is summarized in this section based on the nomenclature used in this dissertation.

Given the model:

$$\dot{\mathbf{x}} = f(\mathbf{x}, \mathbf{u}) \quad (168)$$

In steady state, by definition, the derivatives of the state variables are zero.

$$\dot{\mathbf{x}} = 0 \quad (169)$$

The state variables and input signals are written as a perturbation about the steady-state value.

$$\mathbf{x} = \mathbf{x}_0 + \Delta\mathbf{x} \quad (170)$$

$$\mathbf{u} = \mathbf{u}_0 + \Delta\mathbf{u} \quad (171)$$

The model is rewritten in terms of the steady-state variables and the perturbation variables.

$$\dot{\mathbf{x}}_0 + \Delta\dot{\mathbf{x}} \cong f(\mathbf{x}_0, \mathbf{u}_0) + \mathbf{A}\Delta\mathbf{x} + \mathbf{B}\Delta\mathbf{u} \quad (172)$$

The steady-state portion of the model can be neglected based on (169). Therefore, the model of interest describes the dynamics of the perturbations.

$$\Delta\dot{\mathbf{x}} = \mathbf{A}\Delta\mathbf{x} + \mathbf{B}\Delta\mathbf{u} \quad (173)$$

The  $\mathbf{A}$  and  $\mathbf{B}$  matrices are the partial derivatives of  $f(\mathbf{x}, \mathbf{u})$  with respect to  $\mathbf{x}$  and  $\mathbf{u}$  respectively, evaluated at the steady-state operating point,  $\mathbf{x}_0$  and  $\mathbf{u}_0$ .

$$\mathbf{A} = \left. \frac{\partial f(\mathbf{x}, \mathbf{u})}{\partial \mathbf{x}} \right|_{\mathbf{x}_0, \mathbf{u}_0} \quad (174)$$

$$\mathbf{B} = \left. \frac{\partial f(\mathbf{x}, \mathbf{u})}{\partial \mathbf{u}} \right|_{\mathbf{x}_0, \mathbf{u}_0} \quad (175)$$

## Appendix D Current Control

For the control of AC signals, such as the inverter output current, the plant can be derived by KVL or KCL. In [31], the KVL of the space vectors of the 3-phase signals is transformed to the SRF. This is the approach followed in this work. This section shows the derivation of the dynamics of the positive and negative sequence components of the current. The current dynamics in terms of the space vectors of the signals in Figure 3-2 is derived by applying KVL.

$$\mathbf{E} = R_f \mathbf{i} + L_f \frac{d}{dt} \mathbf{i} + \mathbf{v}_t \quad (176)$$

To consider the dynamics of the PLL, the SRF is defined by the output of the PLL,  $\theta_{PLL}$ .

### Positive Sequence Current Dynamics

Equation (176) is rewritten in terms of the SRF components by substituting  $f_{\alpha\beta 1} = f_{dq1} \exp(j\theta_{PLL})$ .

$$\mathbf{E}_{dq1} e^{j\theta_{PLL}} = R_f \mathbf{i}_{dq1} e^{j\theta_{PLL}} + L_f \frac{d}{dt} (\mathbf{i}_{dq1} e^{j\theta_{PLL}}) + |\mathbf{v}_{t\alpha\beta 1}| e^{j\theta_{t1}} \quad (177)$$

The derivative of the current is expanded based on  $\frac{d}{dt}(uv) = uv' + u'v$ :

$$\begin{aligned} \mathbf{E}_{dq1} e^{j\theta_{PLL}} = R_f \mathbf{i}_{dq1} e^{j\theta_{PLL}} + L_f \left[ j \mathbf{i}_{dq1} e^{j\theta_{PLL}} \frac{d\theta_{PLL}}{dt} + \frac{d\mathbf{i}_{dq1}}{dt} e^{j\theta_{PLL}} \right] \\ + |\mathbf{v}_{t\alpha\beta 1}| e^{j\theta_{t1}} \end{aligned} \quad (178)$$

Simplifying:

$$\mathbf{E}_{dq1} = R_f \mathbf{i}_{dq1} + L_f \left[ j \mathbf{i}_{dq1} \frac{d\theta_{PLL}}{dt} + \frac{d\mathbf{i}_{dq1}}{dt} \right] + |\mathbf{v}_{t\alpha\beta1}| e^{j\theta_{t1}} e^{-j\theta_{PLL}} \quad (179)$$

Separating into real and imaginary components:

$$E_{d1} = R_f i_{d1} - \frac{d\theta_{PLL}}{dt} L_f i_{q1} + L_f \frac{di_{d1}}{dt} + |\mathbf{v}_{t\alpha\beta1}| \text{RE}[e^{j(\theta_{t1}-\theta_{PLL})}] \quad (180)$$

$$E_{q1} = R_f i_{q1} + L_f \frac{d\theta_{PLL}}{dt} i_{d1} + L_f \frac{di_{q1}}{dt} + |\mathbf{v}_{t\alpha\beta1}| \text{IM}[e^{j(\theta_{t1}-\theta_{PLL})}] \quad (181)$$

where:

$$v_{td1} + jv_{tq1} = |\mathbf{v}_{t\alpha\beta1}| \cos[\theta_{t1} - \theta_{PLL}] + j|\mathbf{v}_{t\alpha\beta1}| \sin[\theta_{t1} - \theta_{PLL}] \quad (182)$$

### Negative Sequence Current Dynamics

The negative sequence current dynamics are derived using the same approach. The difference is the angle used to transform the space vector to the negative SRF is the opposite based on the control design. Equation (176) is rewritten in terms of the negative SRF components by substituting  $f_{\alpha\beta2} = f_{dq2} \exp(-j\theta_{PLL})$ .

$$\mathbf{E}_{dq2} e^{-j\theta_{PLL}} = R_f \mathbf{i}_{dq2} e^{-j\theta_{PLL}} + L_f \frac{d}{dt} (\mathbf{i}_{dq2} e^{-j\theta_{PLL}}) + |\mathbf{v}_{t\alpha\beta2}| e^{j\theta_{t2}} \quad (183)$$

where  $\theta_{t2}$  is the phase angle of the negative sequence component of  $\mathbf{v}_t$ . The derivative of the current is expanded recalling  $\frac{d}{dt}(uv) = uv' + u'v$ :

$$\begin{aligned} E_{dq2} e^{-j\theta_{PLL}} &= R_f i_{dq2} e^{-j\theta_{PLL}} \\ &+ L_f \left[ -j i_{dq2} e^{-j\theta_{PLL}} \frac{d\theta_{PLL}}{dt} + \frac{d i_{dq2}}{dt} e^{-j\theta_{PLL}} \right] + |v_{t\alpha\beta 2}| e^{j\theta_{t2}} \end{aligned} \quad (184)$$

Simplifying:

$$E_{dq2} = R_f i_{dq2} + L_f \left[ -j i_{dq2} \frac{d\theta_{PLL}}{dt} + \frac{d i_{dq2}}{dt} \right] + |v_{t\alpha\beta 2}| e^{j\theta_{t2}} e^{j\theta_{PLL}} \quad (185)$$

Separating into real and imaginary components:

$$E_{d2} = R_f i_{d2} + \frac{d\theta_{PLL}}{dt} L_f i_{q2} + L_f \frac{d i_{d2}}{dt} + |v_{t\alpha\beta 2}| \text{RE}[e^{j(\theta_{t2} + \theta_{PLL})}] \quad (186)$$

$$E_{q2} = R_f i_{q2} - L_f \frac{d\theta_{PLL}}{dt} i_{d2} + L_f \frac{d i_{q2}}{dt} + |v_{t\alpha\beta 2}| \text{IM}[e^{j(\theta_{t2} + \theta_{PLL})}] \quad (187)$$

Comparing (180) to (186) and (181) to (187) shows the dynamics are the same except for a change of sign in the coupling between the negative sequence d-axis and q-axis current components. Therefore, the same control structure can be used where  $E_{d2}$  is used to control  $i_{d2}$  and  $E_{q2}$  is used to control  $i_{q2}$ .

## Appendix E Advanced SRF-PLL Structures

### DSOGI SRF-PLL

This section considers the DSOGI-PLL proposed in [59], an adaptive instantaneous sequence component detection filter applied to a traditional SRF-PLL. The basic principle is to create two SRFs, one rotating with respect to the positive sequence component of the grid voltage and another rotating in the opposite direction which represents the negative sequence component. The signals are first filtered in the stationary  $\alpha\beta$  reference frame to avoid the coupling between the two SRFs. Consider the space vector of the system voltage:

$$\mathbf{v}_t = |\mathbf{v}_t|e^{j\theta(t)} = v_{t\alpha}(t) + jv_{t\beta}(t) \quad (188)$$

Neglecting any zero-sequence component, the voltage can be represented by a superposition of its instantaneous positive sequence and negative sequence components.

$$\mathbf{v}_{t\alpha\beta} = \mathbf{v}_{t\alpha\beta 1} + \mathbf{v}_{t\alpha\beta 2} \quad (189)$$

where:

$$\mathbf{v}_{t\alpha\beta 1} = |\mathbf{v}_{t\alpha\beta 1}|e^{j(\omega t + \theta_{1i})} = v_{t\alpha 1} + jv_{t\beta 1} \quad (190)$$

$$\mathbf{v}_{t\alpha\beta 2} = |\mathbf{v}_{t\alpha\beta 2}|e^{-j(\omega t + \theta_{2i})} = v_{t\alpha 2} + jv_{t\beta 2} \quad (191)$$

Figure E-1 shows a snapshot in time of the positive and negative sequence components of the grid voltage space vector. The dashed blue circle represents the magnitude of the positive sequence component, the dashed red circle represents the magnitude of the negative sequence component, and the green vector is the vector sum of the two at an instant in time.

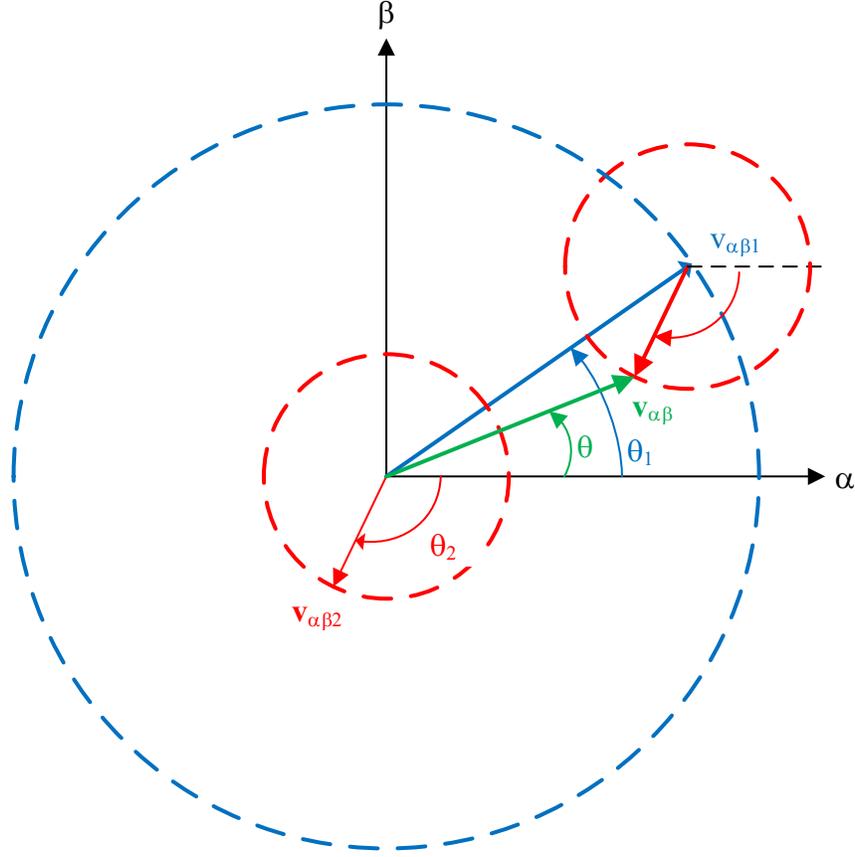


Figure E-1. Grid voltage space vector in  $\alpha\beta$  plane

The  $\alpha\beta$  components of the voltage can be represented by a superposition of the positive and negative sequence components. Combining the real and imaginary terms:

$$\begin{aligned} v_{t\alpha}(t) &= v_{t\alpha1}(t) + v_{t\alpha2}(t) \\ &= |\mathbf{v}_{t\alpha\beta1}| \cos(\omega t + \theta_{1i}) + |\mathbf{v}_{t\alpha\beta2}| \cos(\omega t + \theta_{2i}) \end{aligned} \quad (192)$$

$$\begin{aligned} v_{t\beta}(t) &= v_{t\beta1}(t) + v_{t\beta2}(t) \\ &= |\mathbf{v}_{t\alpha\beta1}| \sin(\omega t + \theta_{1i}) - |\mathbf{v}_{t\alpha\beta2}| \sin(\omega t + \theta_{2i}) \end{aligned} \quad (193)$$

Multiplying both components by  $-j$ :

$$-jv_{t\alpha}(t) = |\mathbf{v}_{t\alpha\beta1}| \cos(\omega t + \theta_{1i} - 90) + |\mathbf{v}_{t\alpha\beta2}| \cos(\omega t + \theta_{2i} - 90) \quad (194)$$

$$=|v_{t\alpha\beta 1}|\sin(\omega t + \theta_{1i}) + |v_{t\alpha\beta 2}|\sin(\omega t + \theta_{2i})$$

$$\begin{aligned} -jv_{t\beta}(t) &= |v_{t\alpha\beta 1}|\sin(\omega t + \theta_{1i} - 90) - |v_{t\alpha\beta 2}|\sin(\omega t + \theta_{2i} - 90) \\ &= -|v_{t\alpha\beta 1}|\cos(\omega t + \theta_{1i}) + |v_{t\alpha\beta 2}|\cos(\omega t + \theta_{2i}) \end{aligned} \quad (195)$$

$v_{t\alpha 1}$  can be calculated by:

$$v_{t\alpha}(t) + jv_{t\beta}(t) = 2|v_{t\alpha\beta 1}|\cos(\omega t + \theta_{1i}) = 2v_{t\alpha 1}(t) \quad (196)$$

$v_{t\alpha 2}$  can be calculated by:

$$v_{t\alpha}(t) - jv_{t\beta}(t) = 2|v_{t\alpha\beta 2}|\cos(\omega t + \theta_{2i}) = 2v_{t\alpha 2}(t) \quad (197)$$

$v_{t\beta 1}$  can be calculated by:

$$v_{t\beta}(t) - jv_{t\alpha}(t) = 2|v_{t\alpha\beta 1}|\sin(\omega t + \theta_{1i}) = 2v_{t\beta 1}(t) \quad (198)$$

$v_{t\beta 2}$  can be calculated by:

$$v_{t\beta}(t) + jv_{t\alpha}(t) = -2|v_{t\alpha\beta 2}|\sin(\omega t + \theta_{2i}) = 2v_{t\beta 2}(t) \quad (199)$$

Given the alpha and beta components of the three-phase voltage the positive and negative sequence components can be found as:

$$\begin{aligned} 2v_{t\alpha 1}(t) &= v_{t\alpha}(t) + jv_{t\beta}(t) \\ 2v_{t\beta 1}(t) &= v_{t\beta}(t) - jv_{t\alpha}(t) \\ 2v_{t\alpha 2}(t) &= v_{t\alpha}(t) - jv_{t\beta}(t) \\ 2v_{t\beta 2}(t) &= v_{t\beta}(t) + jv_{t\alpha}(t) \end{aligned} \quad (200)$$

In the DSOGI implementation, the second order generalized integrator (SOGI) shown in Figure E-2 is used to develop the quadrature components of the alpha and beta grid voltage components in (200).

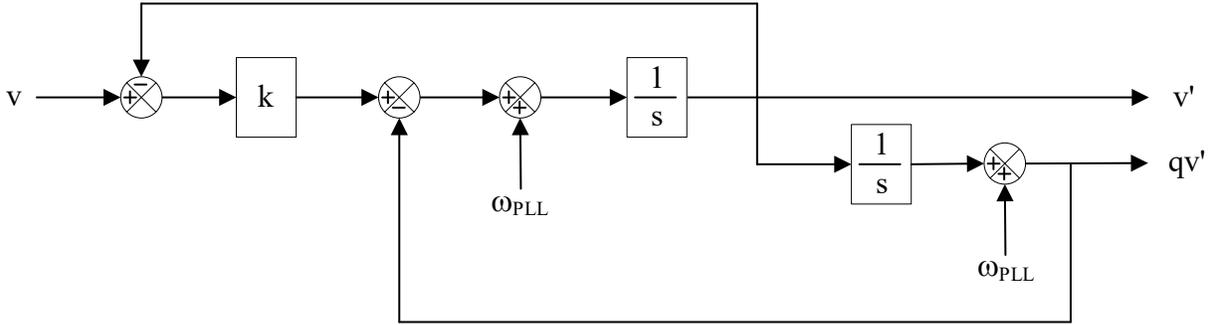


Figure E-2. Second-Order Generalized Integrator

The transfer functions of the voltage in Figure E-2 are:

$$\frac{v'}{v} = \frac{k\omega_{PLL}s}{s^2 + k\omega_{PLL}s + \omega_{PLL}^2} \quad (201)$$

$$\frac{qv'}{v} = \frac{k\omega_{PLL}^2}{s^2 + k\omega_{PLL}s + \omega_{PLL}^2} \quad (202)$$

Figure E-3 shows the Bode plots of the SOGI transfer functions. The transfer function in (202) extracts the 60 Hz voltage signal component, adding 90 degrees of phase lag. The transfer function in (201) extracts the 60Hz component without adding phase lag. The parameter  $k$  determines the bandwidth of the passband.

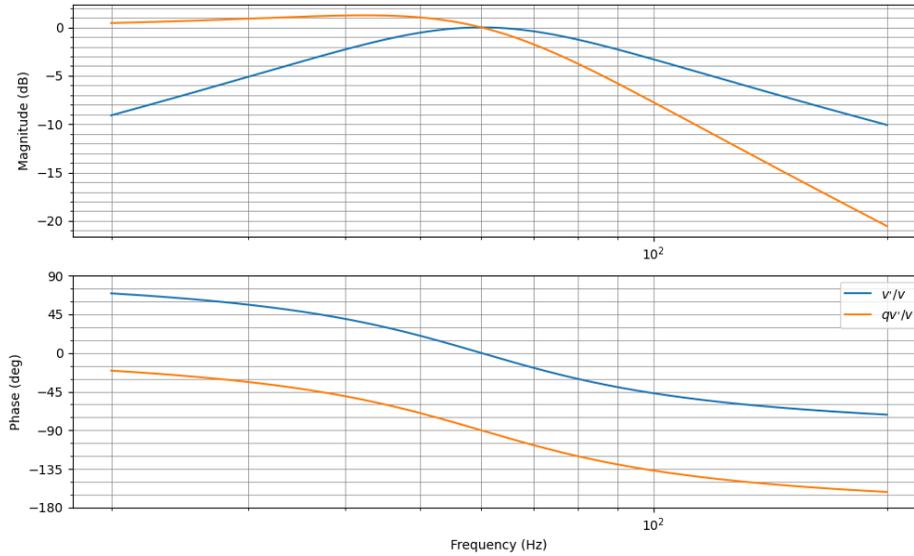


Figure E-3. Bode plot of SOGI transfer functions.

The DSOGI structure consists of two SOGI blocks. The positive sequence components extracted from the input voltage via the DSOGI are used as an input to a standard SRF-PLL discussed in Section 3.3.2. This allows the SRF-PLL to track the phase angle of the positive sequence fundamental component of the grid voltage resulting in improved performance in the presence of unbalanced voltage. The negative sequence component of the voltage can also be readily extracted if needed for the inverter controls. The general structure of the DSOGI-PLL is shown in Figure E-4. Example gains of the DSOGI SRF-PLL are given in Table E-1.

Table E-1. DSOGI SRF-PLL configuration

Parameter	Value
PLL PI controller proportional gain	$k_p = 25.4$
PLL PI controller integral gain	$k_i = 324.0$
SOGI gain	$k = 1$

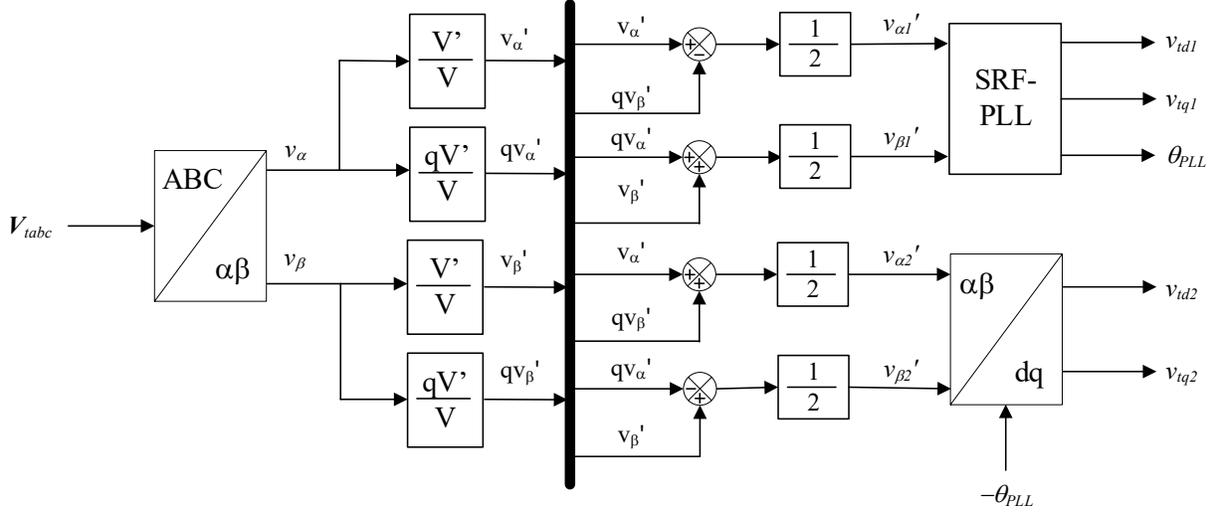


Figure E-4. DSOGI SRF-PLL

### DDSRF-PLL

This section considers the DDSRF-PLL proposed in [60]. The DSOGI SRF-PLL discussed in the previous section filters the positive and negative sequence components of the grid voltage in the  $\alpha\beta$  stationary reference frame. The DDSRF PLL decouples the cross-coupling of the positive and negative sequence components after transformation to the positive and negative SRFs. Transforming (188) to the positive sequence SRF by multiplying by  $\exp(-j\theta_{PLL})$ :

$$\mathbf{v}_{tdq1} = |\mathbf{v}_{ta\beta1}| e^{j(\omega t + \theta_{1i})} e^{-j(\omega t + \angle V_1)} + |\mathbf{v}_{ta\beta2}| e^{-j(\omega t + \theta_{2i})} e^{-j(\omega t + \angle V_1)} \quad (203)$$

Simplifying:

$$\mathbf{v}_{tdq1} = |\mathbf{v}_{ta\beta1}| e^{j(\theta_{1i} - \angle V_1)} + |\mathbf{v}_{ta\beta2}| e^{-j(2\omega t + \angle V_1 + \theta_{2i})} \quad (204)$$

Substituting  $\theta_{PLL} = \omega t + \angle V_1$ :

$$\mathbf{v}_{tdq1} = |\mathbf{v}_{ta\beta1}| e^{j(\theta_{1i} - \angle V_1)} + |\mathbf{v}_{ta\beta2}| e^{-j(2\theta_{PLL} - \angle V_1 + \theta_{2i})} \quad (205)$$

Separating the real and reactive components:

$$v_{td1} = |\mathbf{v}_{\alpha\beta 1}| \cos(\theta_{1i} - \angle \mathbf{V}_1) + |\mathbf{v}_{\alpha\beta 2}| \cos(2\theta_{PLL} - \angle \mathbf{V}_1 + \theta_{2i}) \quad (206)$$

$$v_{tq1} = |\mathbf{v}_{\alpha\beta 1}| \sin(\theta_{1i} - \angle \mathbf{V}_1) - |\mathbf{v}_{\alpha\beta 2}| \sin(2\theta_{PLL} - \angle \mathbf{V}_1 + \theta_{2i}) \quad (207)$$

Simplifying  $v_{td1}$  based on  $\cos(A + B) = \cos A \cos B - \sin A \sin B$ :

$$v_{td1} = |\mathbf{v}_{\alpha\beta 1}| \cos(\theta_{1i} - \angle \mathbf{V}_1) + |\mathbf{v}_{\alpha\beta 2}| \cos(\theta_{2i} - \angle \mathbf{V}_1) \cos(2\theta_{PLL}) - |\mathbf{v}_{\alpha\beta 2}| \sin(\theta_{2i} - \angle \mathbf{V}_1) \sin(2\theta_{PLL}) \quad (208)$$

Simplifying  $v_{tq1}$  based on  $\sin(A + B) = \sin A \cos B + \cos A \sin B$

$$v_{tq1} = |\mathbf{v}_{\alpha\beta 1}| \sin(\theta_{1i} - \angle \mathbf{V}_1) - |\mathbf{v}_{\alpha\beta 2}| \cos(\theta_{2i} - \angle \mathbf{V}_1) \sin(2\theta_{PLL}) - |\mathbf{v}_{\alpha\beta 2}| \sin(\theta_{2i} - \angle \mathbf{V}_1) \cos(2\theta_{PLL}) \quad (209)$$

Transforming (188) to the negative SRF by multiplying by  $\exp(j\theta_{PLL})$ :

$$\mathbf{v}_{tdq2} = |\mathbf{v}_{\alpha\beta 1}| e^{j(\omega t + \theta_{1i})} e^{j(\omega t + \angle \mathbf{V}_1)} + |\mathbf{v}_{\alpha\beta 2}| e^{-j(\omega t + \theta_{2i})} e^{j(\omega t + \angle \mathbf{V}_1)} \quad (210)$$

Simplifying:

$$\mathbf{v}_{tdq2} = |\mathbf{v}_{\alpha\beta 1}| e^{j(2\omega t + \theta_{1i} + \angle \mathbf{V}_1)} + |\mathbf{v}_{\alpha\beta 2}| e^{j(\angle \mathbf{V}_1 - \theta_{2i})} \quad (211)$$

Separating into the real and reactive components results in:

$$v_{td2} = |\mathbf{v}_{\alpha\beta 1}| \cos(\theta_{1i} - \angle \mathbf{V}_1) \cos(2\theta_{PLL}) - |\mathbf{v}_{\alpha\beta 1}| \sin(\theta_{1i} - \angle \mathbf{V}_1) \sin(2\theta_{PLL}) + |\mathbf{v}_{\alpha\beta 2}| \cos(\angle \mathbf{V}_1 - \theta_{2i}) \quad (212)$$

$$v_{tq2} = |\mathbf{v}_{\alpha\beta 1}| \cos(\theta_{1i} - \angle \mathbf{V}_1) \sin(2\theta_{PLL}) + |\mathbf{v}_{\alpha\beta 1}| \sin(\theta_{1i} - \angle \mathbf{V}_1) \cos(2\theta_{PLL}) + |\mathbf{v}_{\alpha\beta 2}| \sin(\angle \mathbf{V}_1 - \theta_{2i}) \quad (213)$$

The following observations are made:

- The positive sequence SRF components contain both a DC component due to the positive sequence component of the voltage and a double fundamental frequency component due to the negative sequence component of the voltage.
- The negative sequence SRF components contain both a DC component due to the negative sequence component of the voltage and a double fundamental frequency component due to the positive sequence component of the voltage.

Based on these observations, the SRF components are written as:

$$v_{td1} = v'_{td1} + v'_{td2} \cos(2\theta_{PLL}) + v'_{tq2} \sin(2\theta_{PLL}) \quad (214)$$

$$v_{tq1} = v'_{tq1} - v'_{td2} \sin(2\theta_{PLL}) + v'_{tq2} \cos(2\theta_{PLL}) \quad (215)$$

$$v_{td2} = v'_{td2} + v'_{td1} \cos(2\theta_{PLL}) - v'_{tq1} \sin(2\theta_{PLL}) \quad (216)$$

$$v_{tq2} = v'_{tq2} + v'_{td1} \sin(2\theta_{PLL}) + v'_{tq1} \cos(2\theta_{PLL}) \quad (217)$$

The DC components are given by:

$$v'_{td1} = |\mathbf{v}_{\alpha\beta 1}| \cos(\theta_{1i} - \angle \mathbf{V}_1) \quad (218)$$

$$v'_{tq1} = |\mathbf{v}_{\alpha\beta 1}| \sin(\theta_{1i} - \angle \mathbf{V}_1) \quad (219)$$

$$v'_{td2} = |\mathbf{v}_{\alpha\beta 2}| \cos(\angle \mathbf{V}_1 - \theta_{2i}) \quad (220)$$

$$v'_{tq2} = |\mathbf{v}_{\alpha\beta 2}| \sin(\angle \mathbf{V}_1 - \theta_{2i}) \quad (221)$$

The DDSRF determines the DC component by subtracting the double fundamental frequency sinusoidal terms from the equations (214)-(217). Figure E-5 shows a diagram of the DDSRF-PLL structure. The authors propose in [60] that the cut-off frequency of the LPF should be set based on (222) to obtain a balance between the dynamic response speed and stability of the system.

$$\omega_{LPF} = \frac{\omega}{\sqrt{2}} = 266.57 \text{ rad/sec} \quad (222)$$

$$G_{LPF} = \frac{\omega_{LPF}}{s + \omega_{LPF}} \quad (223)$$

From the DDSRF-PLL structure in Figure E-5, a few observations are noted:

- This PLL structure allows the tracking of the positive sequence component of the grid voltage.
- The DC values of the positive and negative sequence  $dq$  components of the voltage are available as outputs.
- A LPF is utilized to attenuate any remaining double fundamental frequency sinusoidal components.

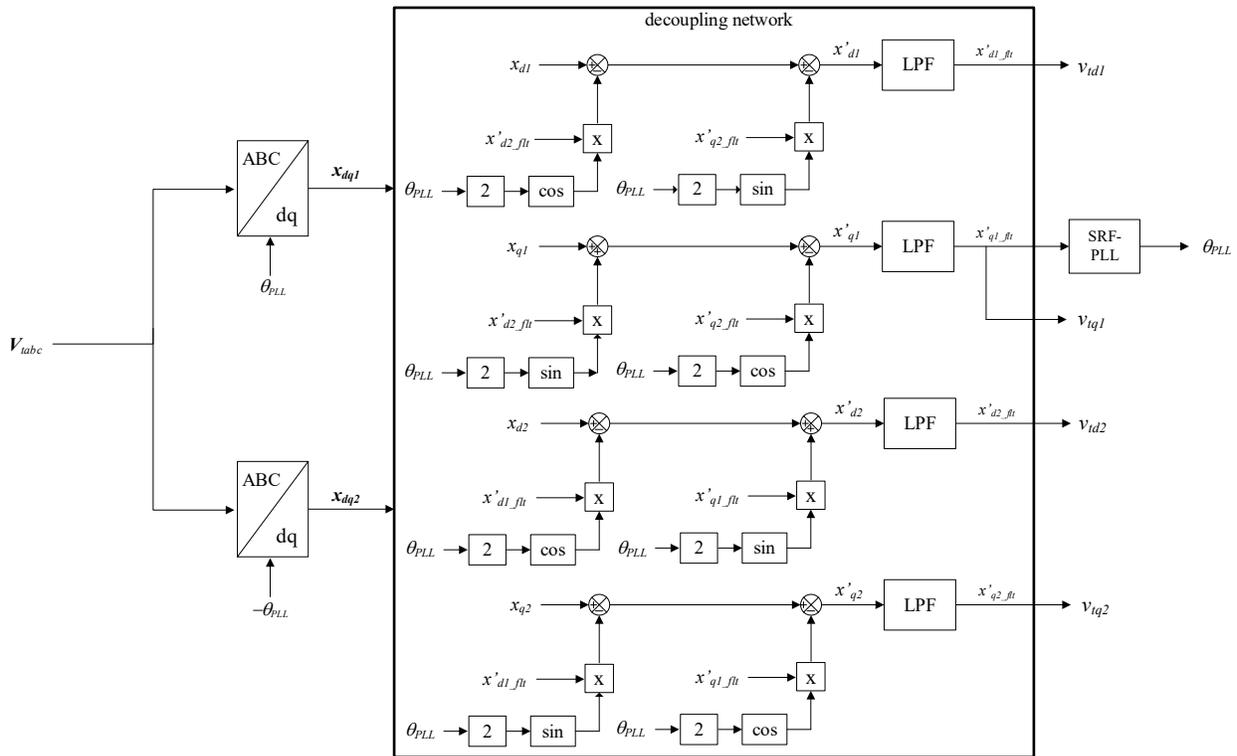


Figure E-5. DDSRF-PLL structure

The performance of the DDSRF-PLL and DSOGI SRF-PLL are compared via time-domain simulations in PSCAD™. The gains of the DSOGI SRF-PLL implemented are given in Table E-1,

and the DDSRF-PLL gains are given in Table E-2. Table E-3 summarizes the simulations and compares the response. Both show improved performance for unbalanced voltage.

Table E-2. DDSRF-PLL configuration

Parameter	Value
PLL PI controller proportional gain	$k_p = 25.4$
PLL PI controller integral gain	$k_i = 324.0$
LPF cut off frequency	$\omega_{LPF} = 2\pi 60/1.41$

Table E-3. Simulation descriptions of PLL comparison.

Simulation description	Observation	Figure
Step change in the phase A test voltage from 1.0pu to 0.8pu at $t = 2.0$ seconds	DDSRF-PLL 120Hz component magnitude is greater than that of the DSOGI SRF-PLL implementation	Figure E-6
Step change in the phase angle of phase A voltage of $30^\circ$ at $t = 2$ seconds	DDSRF-PLL 120Hz component magnitude is greater than that of the DSOGI SRF-PLL implementation	Figure E-7
Addition of 0.2pu magnitude 5 <sup>th</sup> harmonic component to the test voltage at $t = 2.0$ seconds	DDSRF-PLL frequency signal oscillation magnitude is greater than that of DSOGI SRF-PLL.	Figure E-8

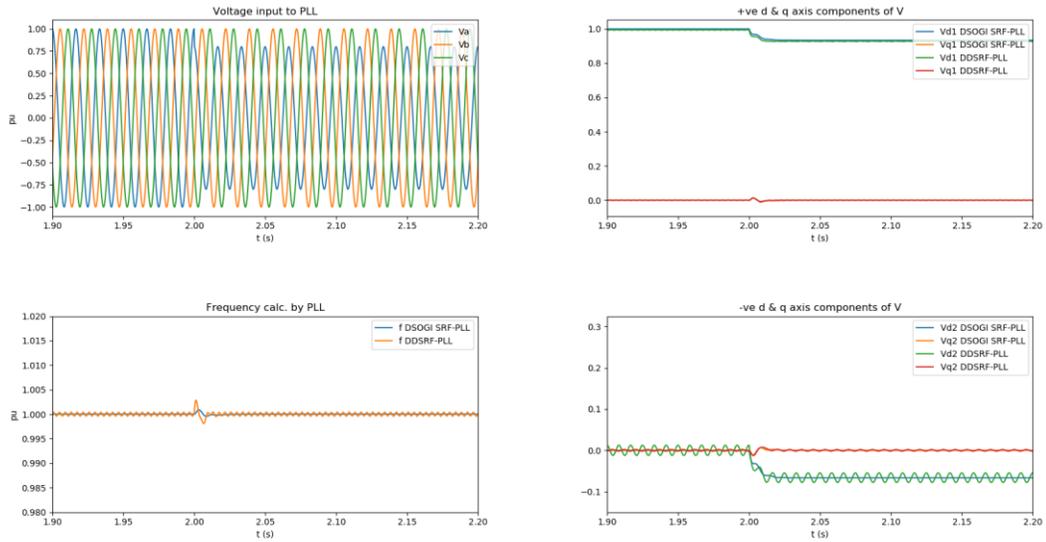


Figure E-6. Comparison of the DDSRF-PLL vs the DSOGI SRF-PLL for a step change in the magnitude of phase A input voltage.

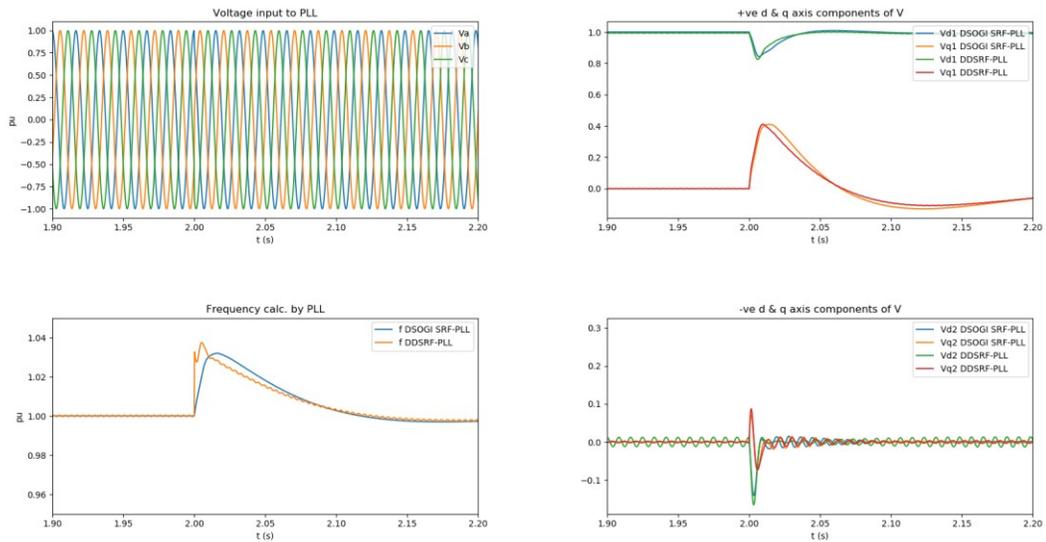


Figure E-7. Comparison of the DDSRF-PLL vs the DSOGI SRF-PLL for step change in the phase angle of phase A voltage of  $30^\circ$ .

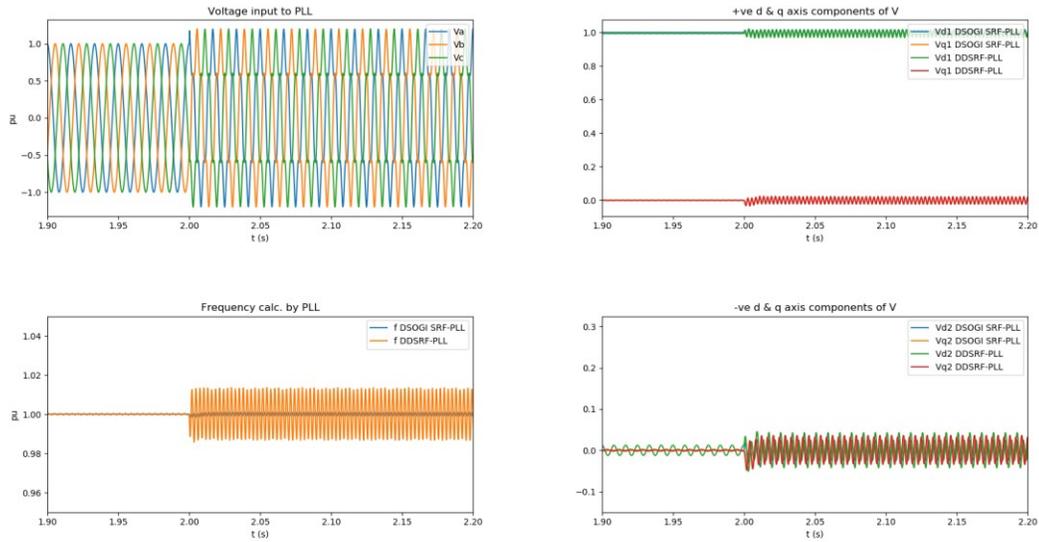


Figure E-8. Comparison of the DDSRF-PLL vs the DSOGI SRF-PLL for 0.2 pu 5<sup>th</sup> harmonic component of the input voltage.

The implementation of the DDSRF-PLL in PSCAD™ showed that the response is sensitive to the low pass filtering and the input signal to the SRF-PLL. Figure E-9 shows a few sensitivities considered. Using the filtered value of the positive sequence q-axis voltage as input to the SRF-PLL as opposed to the prefiltered value reduced the 120 Hz oscillation magnitude but resulted in slower response during the transient. Reducing the LPF cut-off frequency resulted in inferior performance during the transient. Increasing the SRF-PLL bandwidth resulted in increased oscillation magnitude and inferior performance in the transient. A higher-order filter resulted in inferior dynamic performance during the transient.

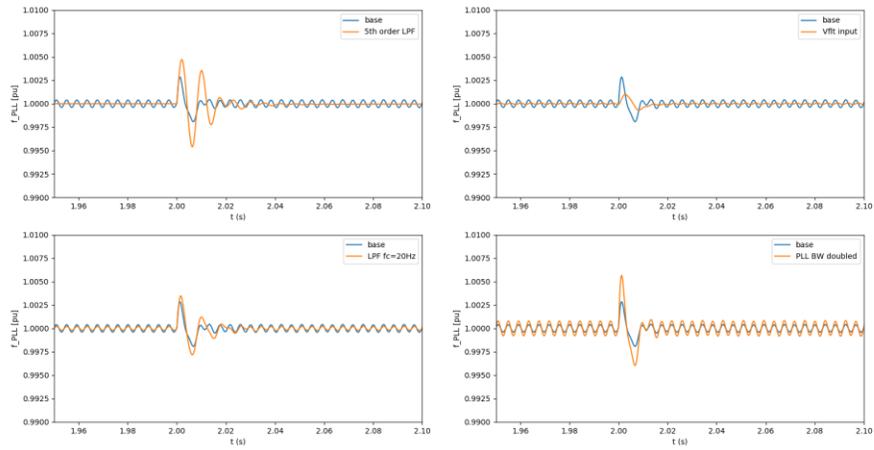


Figure E-9. DDSRF-PLL parameter sensitivity for step change in phase A voltage magnitude. Top left: LPF filter order increased from 1 to 5. Top right: input voltage to SRF-PLL changed to filtered  $V'_{q1\_flt}$ . Bottom left: LPF cutoff frequency reduced from 42.5 Hz to 20 Hz. Bottom right: PLL bandwidth doubled.

## Appendix F Dynamics of the Square of the DC Link Voltage

The DC link voltage can be modeled based on the input power into the DC bus from the PPS and the output power into the AC system. This approach results in modeling the square of the DC link voltage by using the relationship of the energy stored in a capacitor.

$$P_{pv} - P_{inv} = \frac{d}{dt} \left( \frac{1}{2} C_{dc} V_{dc}^2 \right) = \frac{1}{2} C_{dc} \frac{dV_{dc}^2}{dt} \quad (224)$$

Figure F-1 shows the plant of the square of the DC link voltage.

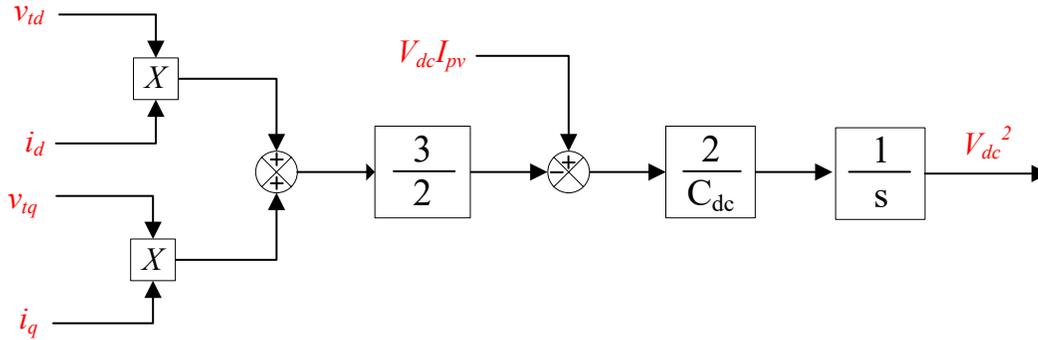


Figure F-1. Dynamics of the square of the DC link voltage.

Re-writing (224) letting  $x = V_{dc}^2$ :

$$\frac{dx}{dt} = \frac{2}{C_{dc}} I_{pv} \sqrt{x} - \frac{3}{C_{dc}} (v_{td} i_d + v_{tq} i_q) \quad (225)$$

The small-signal model of the dynamics of the square of the DC link voltage is:

$$\begin{aligned} \Delta x = & \frac{2V_{cd0}}{C_{dc}} \Delta I_{pv} + \frac{I_{pv0}}{C_{dc} V_{cd0}} \Delta x \\ & - \frac{3}{C_{dc}} (\Delta v_{td} i_{d0} + v_{td0} \Delta i_d + \Delta v_{tq} i_{q0} + v_{tq0} \Delta i_q) \end{aligned} \quad (226)$$

Writing in terms of  $V_{dc}^2$  and substituting  $v_{tq} = 0$  in steady-state gives the small-signal model.

$$\Delta \dot{V}_{dc}^2 = \frac{2V_{cd0}}{C_{dc}} \Delta I_{pv} + \frac{I_{pv0}}{C_{dc}V_{cd0}} \Delta V_{dc}^2 - \frac{3}{C_{dc}} (\Delta v_{td} i_{d0} + v_{td0} \Delta i_d + \Delta v_{tq} i_{q0} + v_{tq0} \Delta i_q) \quad (227)$$

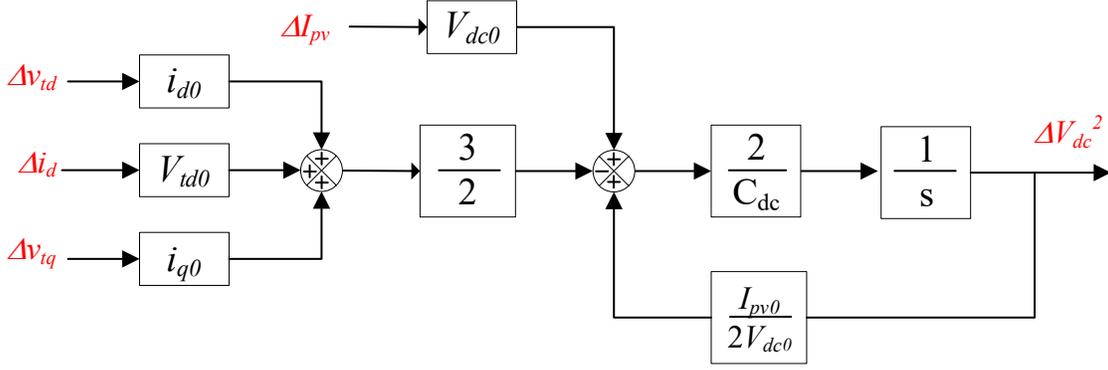


Figure F-2. Small-signal model of the dynamics of the square of the DC link voltage.

The transfer function from the d-axis current to the square of the DC link voltage is given as:

$$\frac{\Delta V_{dc}^2}{\Delta i_d} = -\frac{3v_{td0}}{sC_{dc} - \frac{P_{inv0}}{V_{dc0}^2}} \quad (228)$$

The resulting closed-loop transfer function is:

$$\frac{V_{dc}^2(s)}{V_{dc}^{*2}(s)} = \frac{3V_{td0}(k_p s + k_i)}{C_{dc} \left( s^2 + \frac{(3V_{td0}k_p - \frac{P_{inv0}}{V_{dc0}^2})}{C_{dc}} s + \frac{3V_{td0}k_i}{C_{dc}} \right)} \quad (229)$$

The PI gains can be calculated by pole placement based on the target rise time and damping of the response.

$$k_p = \frac{2\zeta\omega_n C_{dc} + \frac{P_{inv0}}{V_{dc0}^2}}{3V_{td0}} \quad (230)$$

$$k_i = \frac{\omega_n^2 C_{dc}}{3V_{td0}} \quad (231)$$

## Appendix G Negative Sequence Current Injection

Grids with high penetration levels of synchronous generators have a predictable relationship of the negative sequence current with respect to the negative sequence voltage. This is due to the physical properties of synchronous machines. The negative sequence reactance of a synchronous machine is approximately equal to the average of the machine's  $d$ -axis and  $q$ -axis subtransient reactances,  $X''_d$  and  $X''_q$  [86]. Unlike synchronous machines, the response of IBR to faults is dependent on the control algorithm implemented in the inverter. Given this is implemented in software, the response is not predictable unless there are grid code requirements that standardize the response and verification to ensure correct implementation.

The variability in the inverter response to faults may have undesirable consequences on traditional protection schemes. For example, negative-sequence polarization schemes applied to determine the fault direction for unbalanced faults in networked transmission protection rely on the relationship between the negative sequence voltage and current in grids dominated by synchronous machines [87-90]. A 2020 study led by Sandia National Laboratories [91] investigated the response of IBR to unbalanced faults to determine their impact on existing protection practices by simulation of four OEM-specific, black-box, IBR EMT models representing PV, Type 3 WTGs, and Type 4 WTGs. The study indicated that not all inverters inject negative sequence current for unbalanced grid disturbances. Further, for those inverters that inject negative sequence current, the response was found not always to be consistent with the phase relationship of the negative sequence current with respect to the negative sequence voltage for traditional grids comprised of mostly synchronous generation.

In 2013, the authors in [68] proposed extending grid code requirements in Germany to require WTGs to inject negative sequence current during faults due to potential impacts to conventional

protection schemes in grids with high penetration of IBR. The German (VDE) [26, 27] and Spanish (NTS) [28] applications of the European Grid Code [29] require negative sequence current injection based on the magnitude of the negative sequence voltage as shown in Table 3-IX. In 2020, the IEEE Power System Relay and Control Committee recommended that transmission owners and regulators require IBR to provide negative sequence current for unbalanced faults [89]. Draft 6.1 of IEEE P2800 [25] requires IBR to have the capability to inject negative sequence reactive current during unbalance faults based on the negative sequence voltage at the inverter AC terminals.

### Negative Sequence Current Reference

This section presents the derivation of the negative sequence voltage control in the negative SRF. Considering the simple system shown in Figure 3-2, neglecting the grid resistance  $R_g$ , the voltage  $v_t$  can be written:

$$v_t = L_g \frac{di}{dt} + v_g \quad (232)$$

The control is implemented in the negative SRF, therefore the negative sequence component of (232) is transformed to the negative SRF.

$$v_{tdq2} e^{-j\theta_{PLL}} = L_g \frac{d(i_{dq2} e^{-j\theta_{PLL}})}{dt} + v_{g\alpha\beta2} \quad (233)$$

Expanding the derivative term results in:

$$v_{tdq2} e^{-j\theta_{PLL}} = L_g \frac{d(i_{dq2})}{dt} e^{-j\theta_{PLL}} - jL_g i_{dq2} \frac{d(\theta_{PLL})}{dt} e^{-j\theta_{PLL}} + v_{g\alpha\beta2} \quad (234)$$

Dividing through by  $e^{-j\theta_{PLL}}$ :

$$\mathbf{v}_{tdq2} = L_g \frac{d(\mathbf{i}_{dq2})}{dt} - jL_g \mathbf{i}_{dq2} \frac{d(\theta_{PLL})}{dt} + \mathbf{v}_{g\alpha\beta2} e^{j\theta_{PLL}} \quad (235)$$

The objective is to control the magnitude of  $\mathbf{v}_{tdq2}$  ideally to zero. Therefore, the terminal voltage and current in (235) is written in polar form and  $\omega_{PLL}$  is substituted for  $\dot{\theta}_{PLL}$ .

$$\begin{aligned} |\mathbf{v}_{tdq2}| e^{j\angle(\mathbf{v}_{tdq2})} &= L_g \frac{d(\mathbf{i}_{dq2})}{dt} + L_g \omega_{PLL} |\mathbf{i}_{dq2}| e^{j\angle(\mathbf{i}_{dq2})} e^{-j90^\circ} \\ &+ \mathbf{v}_{g\alpha\beta2}(t) e^{j\theta_{PLL}} \end{aligned} \quad (236)$$

Neglecting the derivative of the current and the grid voltage  $\mathbf{v}_g$ ,  $|\mathbf{v}_{tdq2}|$  can be controlled by the current  $\mathbf{i}_{dq2}$ . If the phase of  $\mathbf{i}_{dq2} e^{-j90^\circ}$  is  $180^\circ$  different from the phase of  $\mathbf{v}_{tdq2}$ , then  $|\mathbf{v}_{tdq2}|$  can be directly controlled by  $|\mathbf{i}_{dq2}|$ . This gives the following relationship to ensure  $\mathbf{i}_{dq2}$  is  $180^\circ$  out of phase with  $\mathbf{v}_{tdq2}$ :

$$\angle(\mathbf{v}_{tdq2}) - \angle(\mathbf{i}_{dq2} - 90^\circ) = \pm 180^\circ \quad (237)$$

Solving for  $\angle \mathbf{i}_{dq2}$  gives:

$$\angle(\mathbf{i}_{dq2}) = \angle(\mathbf{v}_{tdq2}) - 90^\circ \quad (238)$$

Therefore, the negative sequence voltage control is designed can generate a current reference signal based on the magnitude of  $\mathbf{v}_{tdq2}$  and then ensure the control signal lags  $\mathbf{v}_{tdq2}$  by  $90^\circ$ . A block diagram of an implementation using proportional control is shown in Figure G-1.

$$\mathbf{i}_{dq2}^* = |\mathbf{v}_{tdq2}| k_{qv2} \angle (\mathbf{v}_{tdq2} - 90^\circ) \quad (239)$$

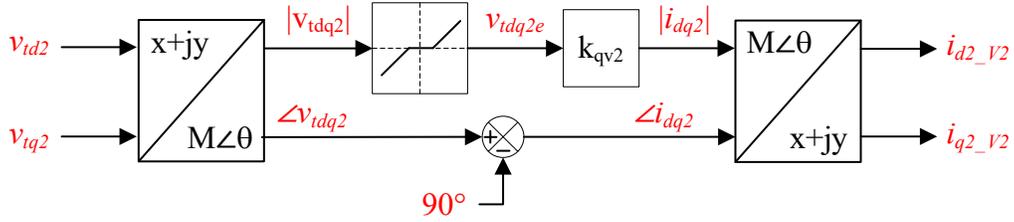


Figure G-1. Negative sequence voltage control block diagram.

### Transform to Sequence Components

The previous section presented the negative sequence voltage control where the objective is to reduce the negative sequence voltage magnitude. Given that the control is implemented in the negative SRF, this section shows how this relates to the voltage and current sequence components in the phasor domain to ensure the control strategy meets the grid code requirements. Given the negative sequence voltage in the negative SRF:

$$v_{td2} + jv_{tq2} = |\mathbf{v}_{tdq2}| e^{j\angle v_{tdq2}} \quad (240)$$

Converting from the negative SRF to the stationary reference frame:

$$\mathbf{v}_{t\alpha\beta 2} = |\mathbf{v}_{tdq2}| e^{j\angle v} e^{-j\theta_{PLL}} \quad (241)$$

Substituting for  $\theta_{PLL}$  gives the space vector of the negative sequence terminal voltage:

$$\begin{aligned} \mathbf{v}_{t\alpha\beta 2} &= |\mathbf{v}_{tdq2}| e^{j\angle v_{tdq2}} e^{-j(\omega t + \angle V_{t1})} \\ &= |\mathbf{v}_{tdq2}| e^{-j(\omega t + \angle V_{t1} - \angle v_{tdq2})} \end{aligned} \quad (242)$$

Following the same approach for the negative sequence current in the SRF and noting that the control subtracts  $90^\circ$  from the phase of  $v_{tdq2}$  in the negative SRF gives the space vector of the negative sequence current.

$$\begin{aligned} \mathbf{i}_{\alpha\beta 2} &= |\mathbf{i}_{dq2}| e^{j(\angle v_{tdq2} - 90^\circ)} e^{-j(\omega t + \angle V_{t1})} \\ &= |\mathbf{i}_{dq2}| e^{-j(\omega t + \angle V_{t1} - \angle v_{tdq2} + 90^\circ)} \end{aligned} \quad (243)$$

The space vector of the voltages and currents are now transformed to the ABC reference frame via the inverse Clarke transform. The signals are in the form:

$$\mathbf{x}_{\alpha\beta 2} = |\mathbf{x}_{\alpha\beta 2}| e^{j\angle \mathbf{x}_{\alpha\beta 2}} \quad (244)$$

For convenience, the inverse Clarke transform is written in terms of trigonometric functions:

$$\begin{bmatrix} x_a(t) \\ x_b(t) \\ x_c(t) \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ \frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} x_\alpha(t) \\ x_\beta(t) \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ \cos(120^\circ) & \sin(120^\circ) \\ \cos(-120^\circ) & \sin(-120^\circ) \end{bmatrix} \begin{bmatrix} x_\alpha(t) \\ x_\beta(t) \end{bmatrix} \quad (245)$$

This allows the application of the following trigonometric functions.

$$\cos(a) \cos(b) = \frac{1}{2} (\cos(a + b) + \cos(a - b)) \quad (246)$$

$$\sin(a) \sin(b) = \frac{1}{2} (\cos(a - b) - \cos(a + b)) \quad (247)$$

The resulting components in the ABC reference frame are given by:

$$x_a = |\mathbf{x}_{\alpha\beta 2}| \cos(\angle \mathbf{x}_{\alpha\beta 2}) \quad (248)$$

$$\begin{aligned}
x_b &= |x_{\alpha\beta 2}| \left[ \cos(x_{\alpha\beta 2}) \cos(120^\circ) + \sin(x_{\alpha\beta 2}) \sin(120^\circ) \right] \\
&= |x_{\alpha\beta 2}| \cos(x_{\alpha\beta 2} - 120^\circ) \\
x_c &= |x_{\alpha\beta 2}| \left[ \cos(x_{\alpha\beta 2}) \cos(-120^\circ) + \sin(x_{\alpha\beta 2}) \sin(-120^\circ) \right] \\
&= |x_{\alpha\beta 2}| \cos(x_{\alpha\beta 2} + 120^\circ)
\end{aligned}$$

Substituting the negative sequence  $\alpha\beta$  voltage results in:

$$\begin{aligned}
v_{ta2}(t) &= v_{t\alpha 2}(t) = |v_{tdq2}| \cos(-(\omega t + \angle V_{t1} - \angle v_{tdq2})) \\
&= |v_{tdq2}| \cos(\omega t + \angle V_{t1} - \angle v_{tdq2}) \\
v_{tb2}(t) &= |v_{tdq2}| \cos(-(\omega t + \angle V_{t1} - \angle v_{tdq2}) - 120^\circ) \\
&= |v_{tdq2}| \cos(\omega t + \angle V_{t1} - \angle v_{tdq2} + 120^\circ) \\
v_{tc2}(t) &= |v_{tdq2}| \cos(-(\omega t + \angle V_{t1} - \angle v_{tdq2}) + 120^\circ) \\
&= |v_{tdq2}| \cos(\omega t + \angle V_{t1} - \angle v_{tdq2} - 120^\circ)
\end{aligned} \tag{249}$$

Substituting the negative sequence  $\alpha\beta$  voltage results in:

$$\begin{aligned}
i_{a2}(t) &= i_{\alpha 2}(t) = |i_{dq2}| \cos(-(\omega t + \angle V_{t1} - \angle v_{tdq2}) - 90^\circ) \\
&= |i_{dq2}| \cos(\omega t + \angle V_{t1} - \angle v_{tdq2} + 90^\circ) \\
i_{b2}(t) &= |i_{dq2}| \cos(-(\omega t + \angle V_{t1} - \angle v_{tdq2}) - 90^\circ - 120^\circ) \\
&= |i_{dq2}| \cos(\omega t + \angle V_{t1} - \angle v_{tdq2} + 210^\circ) \\
i_{c2}(t) &= |i_{dq2}| \cos(-(\omega t + \angle V_{t1} - \angle v_{tdq2}) - 90^\circ + 120^\circ) \\
&= |i_{dq2}| \cos(\omega t + \angle V_{t1} - \angle v_{tdq2} - 30^\circ)
\end{aligned} \tag{250}$$

The resulting time-domain ABC signals (249) and (250) have ACB phase rotation indicating they are negative sequence. The negative sequence phasors of the terminal voltage and current in terms of the peak values are written with respect to the frequency  $\omega$ :

$$V_{t2} = |v_{tdq2}| \angle(\angle V_{t1} - \angle v_{tdq2}) = |v_{tdq2}| \angle v_{tdq2} \tag{251}$$

$$I_2 = |i_{dq2}| \angle (\angle V_{t1} - \angle v_{tdq2} + 90^\circ) = |i_{dq2}| \angle (V_{t2} + 90^\circ) \quad (252)$$

Figure G-2 shows the controlled current and input voltage in the negative SRF, their transformation to the  $\alpha\beta$  reference frame, and the resulting symmetrical component phasors. From (251) and (252), in the phasor domain, the negative sequence current leads the negative sequence voltage by  $90^\circ$ . This is consistent with the phasor relationship of the negative sequence voltage and current in grids comprised of mostly synchronous machines, the performance requirements in [25-27], and the recommendation in [91]. Therefore, the control implementation meets the control objective.

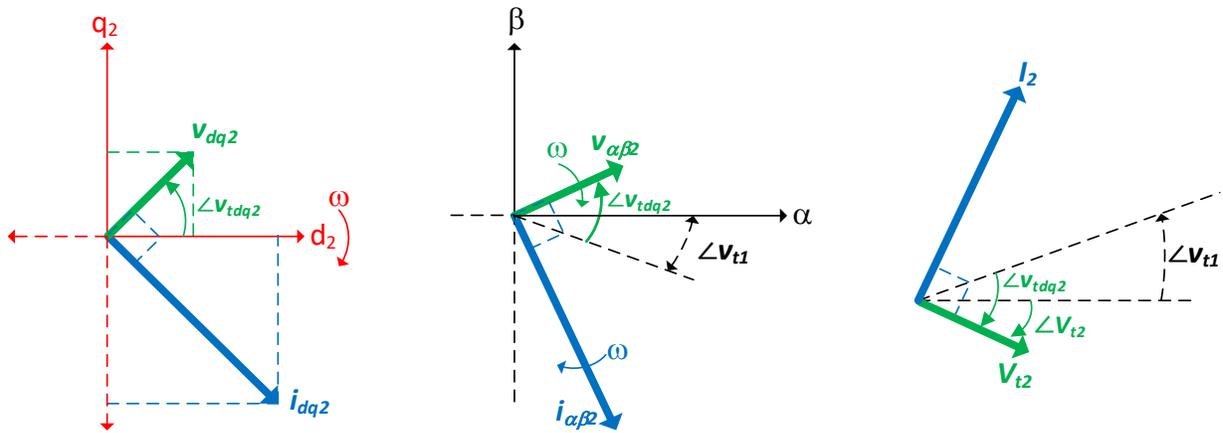


Figure G-2. Diagram of the manifestation of the negative sequence control from the negative SRF (left), to the space vector (middle), and the phasor domain (right).

## **Appendix H     Response of a Synchronous Machine to System Fault**

This section provides a few examples of the response of a synchronous machine to short circuit conditions at the high side terminal of the generator step-up transformer (GSU). The response of a synchronous machine to faults on the power system has been well studied by power system engineers. As mentioned in Chapter 1, the way the traditional power system is planned, operated, and protected is based on the response of synchronous machines. Therefore, only a few representative examples are included. Simulations of a synchronous machine response to a balanced and an unbalanced fault are presented. The simulations are performed in PSCAD™. The nomenclature used to describe the different components of the current in Chapter 4 is used in this section.

### **Test System**

Figure H-1 shows the simple system that consists of a 1 MVA synchronous machine connected to a voltage source behind a resistance and an inductance. The IEEE 421.5-2016 static excitation system model ST4C is used to model the excitation system. The ST4C model is parameterized using the sample data in Table H.31 of IEEE 421.5-2016 [92], as shown in Table H-2. A governor model is not included, and therefore, the input mechanical torque is held constant. The parameters assumed for the synchronous machines are given in Table H-1. The parameters for the test system are given in Table H-3.

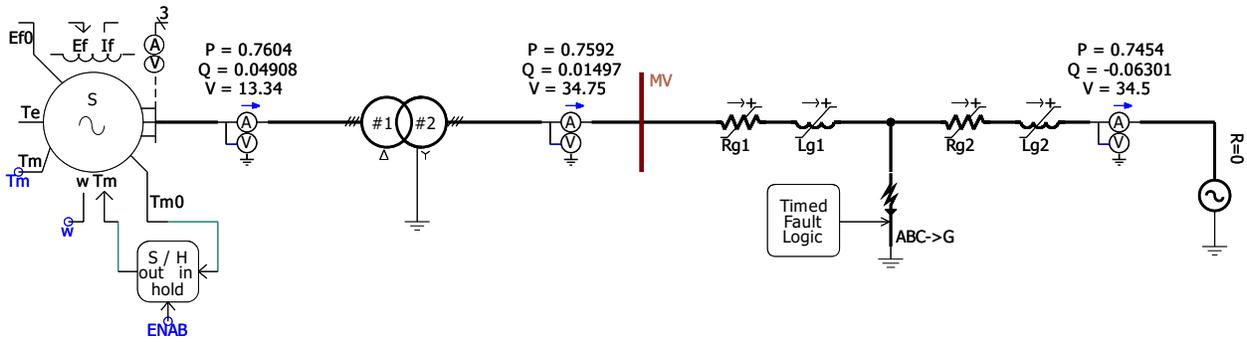


Figure H-1. Test system for simulations of the fault response of a synchronous machine.

Table H-1. Synchronous Machine Parameters

Parameter	Value
MVA rating	1.0 MVA
voltage rating	13.2 kV
rated speed	376.992 rad/s
inertia constant	4.0 s
d-axis synchronous reactance	2.1 pu
q-axis synchronous reactance	2.0 pu
d-axis transient reactance	0.2 pu
q-axis transient reactance	0.5 pu
d-axis subtransient reactance	0.18 pu
q-axis subtransient reactance	0.18 pu
d-axis transient open-circuit time constant	7.0 s
q-axis transient open-circuit time constant	0.75 s
d-axis subtransient open-circuit time constant	0.03 s
q-axis subtransient open-circuit time constant	0.05 s

Table H-2. ST4C Excitation System Parameters

Parameter	Value
voltage regulator proportional gain	10.75 pu
voltage regulator integral gain	10.75 pu/s
thyristor bridge firing control equivalent time constant	0.02 s
maximum regulator output	1.0 pu
minimum regulator output	-0.87 pu
forward proportional gain of inner loop field regulator	1.0 pu
forward integral gain of inner loop field regulator	0.0 pu
maximum output of field current regulator	99 pu
minimum output of field current regulator	-99 pu
maximum exciter output	99 pu
minimum exciter output	- 99 pu
feedback gain of field current regulator	0 pu
feedback time constant of field current regulator	0 pu
maximum feedback voltage for field current regulator	99 pu
power source selector	A
rectifier loading factor proportional to commutating reactance	0.113 pu
potential circuit (voltage) gain coefficient	9.3 pu
compound circuit (current) gain coefficient	0 pu
reactance associated with potential source	0.124 pu
potential circuit phase angle (degrees)	0 degrees
maximum available exciter voltage	11.63 pu

Table H-3. System Parameters

Parameter	Value
transformer MVA rating	1.0 MVA
transformer impedance	0.06 pu, X/R = 30.0
transformer connection	delta – wye grounded
system impedance	Z = 0.14 pu , X/R = 10 1 MVA, 34.5 kV base

### Example of a Symmetrical Fault

The first example is a three-phase fault at the high side terminal of the GSU. Figure H-2 shows the voltages and currents measured at the high side terminal of the GSU. The instantaneous currents show an exponentially decaying DC offset. This DC offset manifests in the dq components as a 60 Hz component. Figure H-3 shows the symmetrical components of the voltages and currents measured at the high side terminal of the GSU. Figure H-4 shows the instantaneous active and reactive power and the synchronous machine speed.

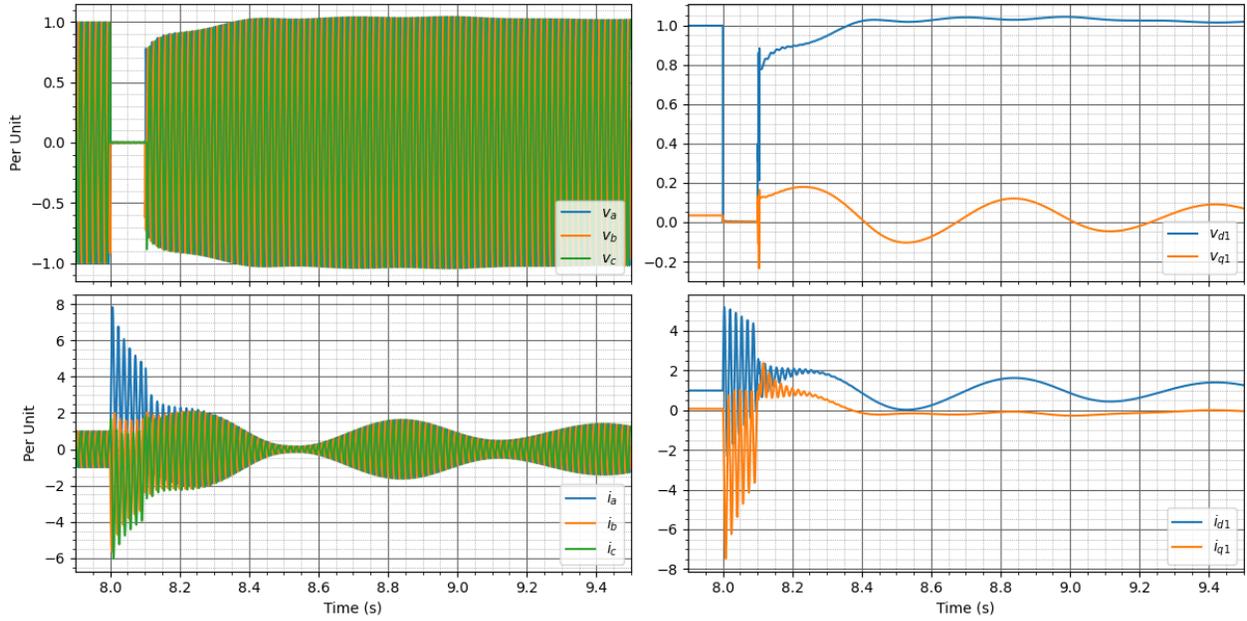


Figure H-2. Instantaneous voltage and current (left) and dq components of voltage and current (right) measured at the high side of the GSU for a 3PH fault at the high side terminal of the GSU.

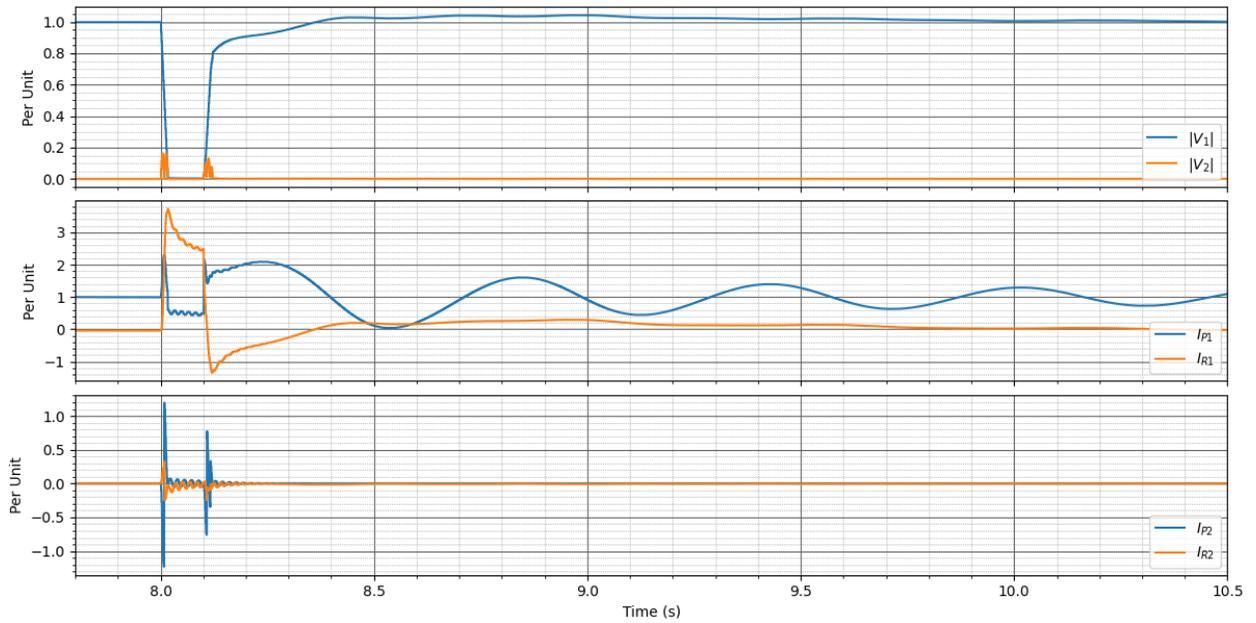


Figure H-3. Symmetrical components of the voltage (top), positive sequence active and reactive components of the current (middle), and negative sequence active and reactive components of the current (bottom) for a 3PH fault at the high side terminal of the GSU.

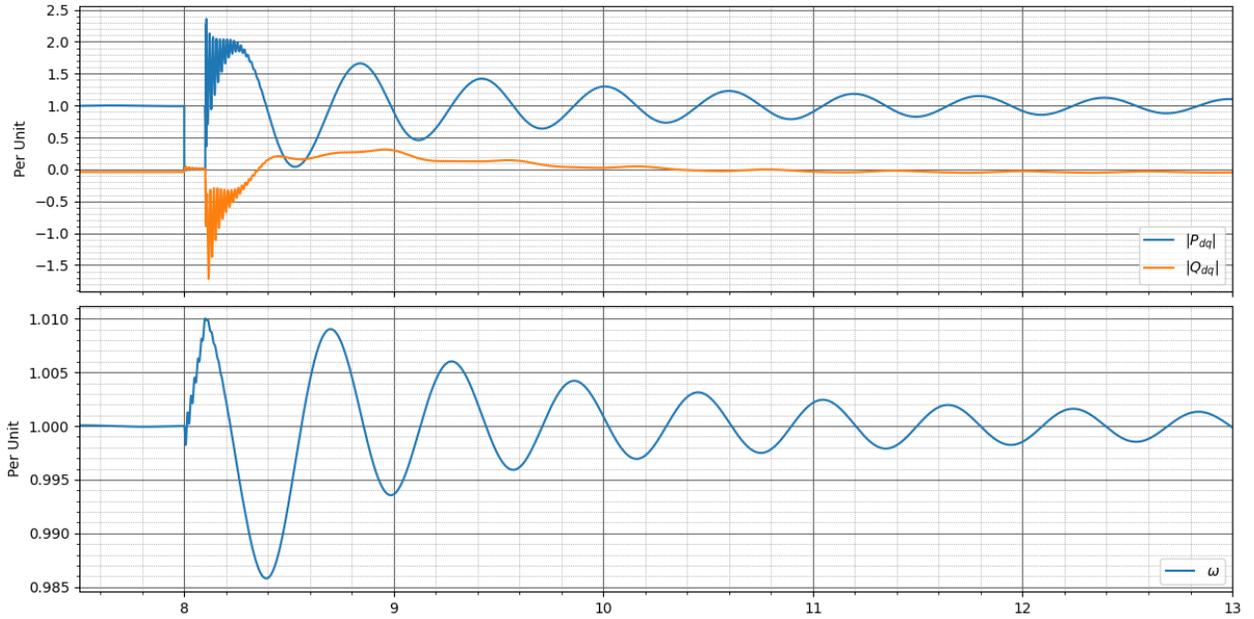


Figure H-4. Instantaneous active and reactive power (top) and machine speed for a 3PH fault at the high side terminal of the GSU.

### Example of an Asymmetrical Fault

The second example is a phase B to phase C fault (BC) at the high side terminal of the GSU. Figure H-5 shows the voltages and currents measured at the high side terminal of the GSU. Figure H-6 shows the symmetrical components of the voltages and currents measured at the high side terminal of the GSU. Figure H-7 shows the instantaneous active and reactive power and the synchronous machine speed. The negative sequence components are evident in the dq signals and the instantaneous active and reactive power signals by the 120 Hz component of the signals.

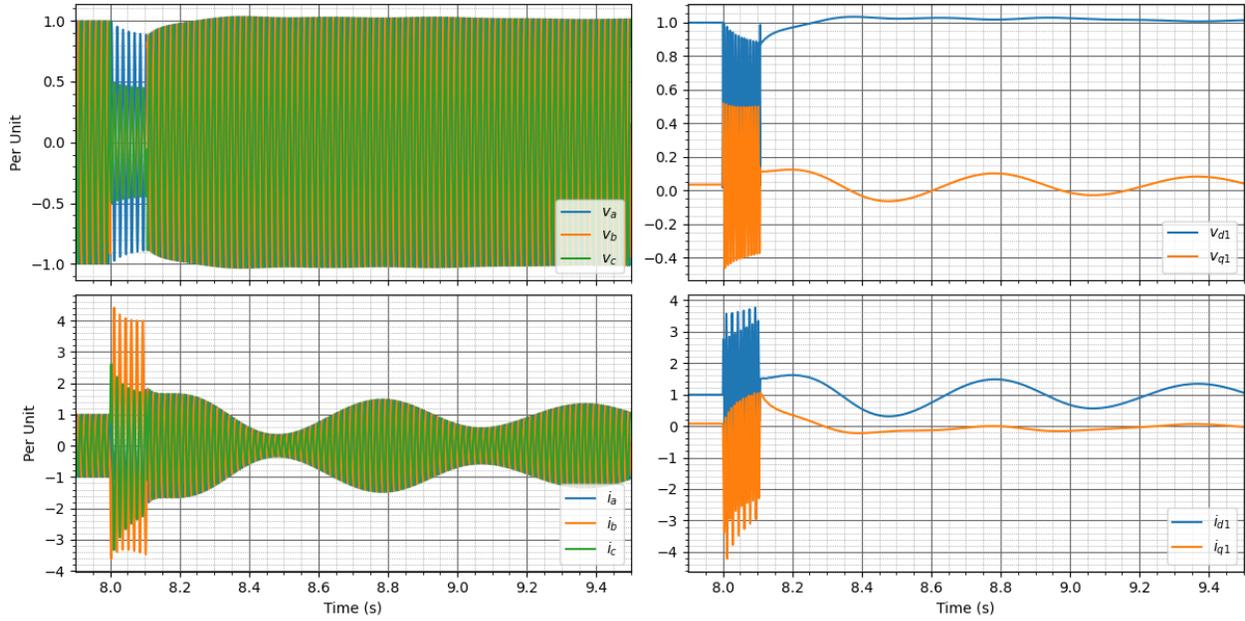


Figure H-5. Instantaneous voltage and current (left) and dq components of voltage and current (right) measured at the high side of the GSU for a BC fault at the high side terminal of the GSU.

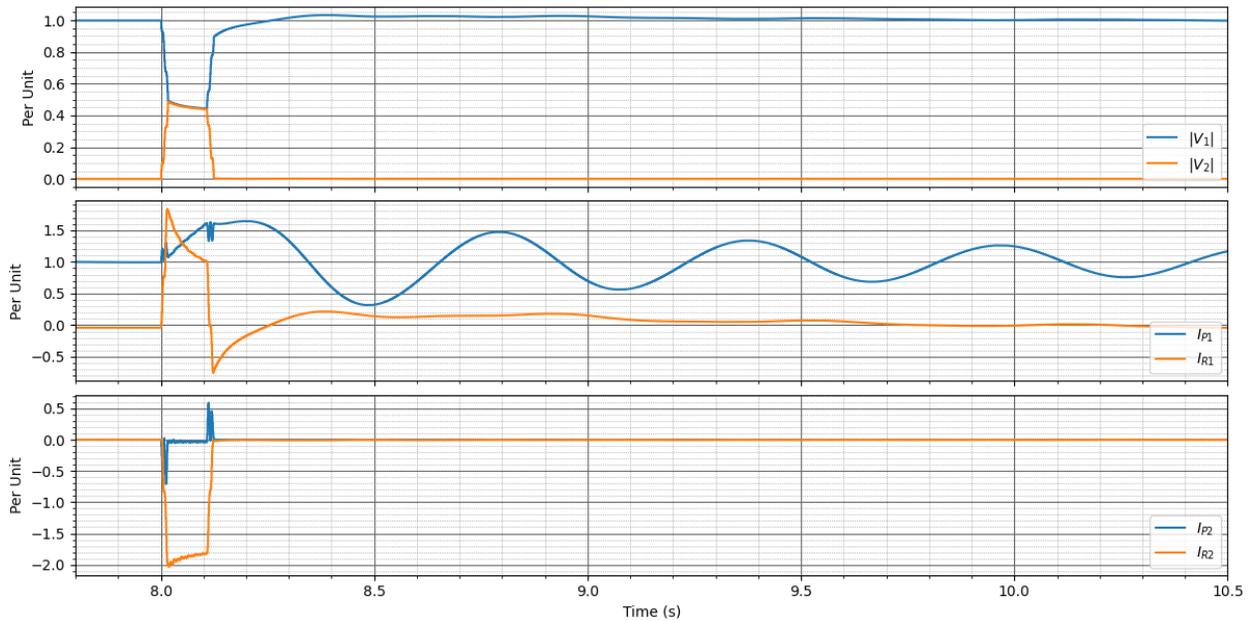


Figure H-6. Symmetrical components of the voltage (top), positive sequence active and reactive components of the current (middle), and negative sequence active and reactive components of the current (bottom) for a BC fault at the high side terminal of the GSU.

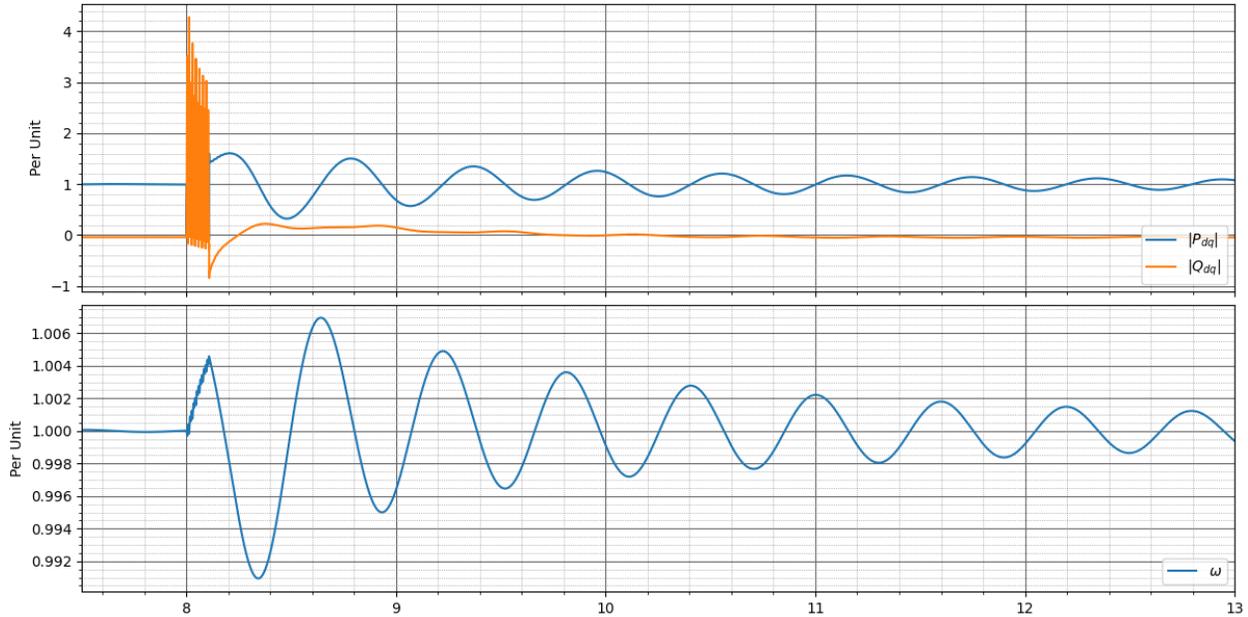


Figure H-7. Instantaneous active and reactive power (top) and machine speed for a BC fault at the high side terminal of the GSU.

## Summary

These simple examples highlight some of the key differences in a synchronous machine's response to grid faults compared to an IBR. Section 3.7 of [86] details the response of the synchronous machine for faults. A few of these points are highlighted based on this example.

- The response is primarily determined by the physical parameters of the machine.
- The synchronous machine injects close to 4 pu current in response to the fault based on the parameters used in this case. The fault current decreases with time due to the changing internal voltage of the machine.
- There is a DC component that decays based on the L/R ratio of the machine. The magnitude of the DC offset will vary based on the point-on-wave of the voltage at the instant of the fault.
- For the BC fault, the negative sequence reactive component of the current is larger in magnitude than the positive sequence reactive component of the machine current after the subtransient period. Recall that the negative sequence reactance of a machine is approximately equal to the subtransient reactance [93].
- The impact of the machine inertia is observed in the oscillations.