**Drop Shock Performance of Solder Alloys in BGA Assemblies under Different Thermal Conditions**

by

Palash Pranav Vyas

A dissertation submitted to the Graduate Faculty of
Auburn University
in partial fulfillment of the
requirements for the Degree of
Doctor of Philosophy

Auburn, Alabama
May 6th, 2024

Keywords: Drop shock, solder joint, lead-free, elevated temperature, reliability

Copyright 2024 by Palash Pranav Vyas

Approved by

Sa’d Hamasha, Chair, Associate Professor, Department of Industrial and Systems Engineering
George Flowers, Professor, Department of Mechanical Engineering
Michael Bozack, Emeritus Professor, Department of Physics
Jia Liu, Assistant Professor, Department of Industrial and Systems Engineering
Farah Kandah, Associate Professor, Department of Computer Science and Software Engineering

**Abstract**

Lead-free soldering has become mainstream since the Restriction of Hazardous Substances (RoHS) Directive. Solders have come a long way from the traditional SnPb (Tin-Lead) to lead-free alloys doped with elements such as Bismuth (Bi), Antimony (Sb), Nickel (Ni), etc. Following the transition from ductile lead-based alloys to strong but brittle lead-free solder alloys, the board-level drop test has become a vital reliability evaluation criterion for electronic packages. Board-level drop impact testing is one of the most critical methods of evaluating the reliability of electronic assemblies. The main objective of this dissertation is to model the drop shock reliability of various lead-free solder alloys under different acceleration levels and temperatures.

The first study investigates the drop shock reliability of ball grid array (BGA) assemblies utilizing various SAC-based alloys and compares their performance with the established SnPb alloy benchmark. Drop test was conducted at different acceleration levels and pulse widths. Additionally, the input energy for each specific acceleration level was determined. A drop life prediction model was then developed for each alloy at different energy levels. In parallel, a hardness test was performed for all alloys under pristine conditions, and the results were correlated with the corresponding drop life performance. A comprehensive microscopy analysis has been performed to ascertain the failure modes and identify trends in failure patterns as a function of acceleration levels. The study findings revealed that SAC-Bi alloys exhibit superior performance compared to both SAC305 and SnPb alloys at lower energy levels. Moreover, the failure mode for SAC-Bi alloys and SnPb remains independent and constant across all energy levels, while SAC305 exhibits variability in its failure mode.

Traditionally, drop shock tests have predominantly been performed at room temperature, failing to accurately simulate real-world conditions where electronic circuits contend with operational or environmental thermal strains during normal operation. To address this knowledge gap, the second study aims to conduct drop shock tests at elevated temperatures, ensuring the reliability of solder joints in practical applications. In the second study, ball grid array (BGA) assemblies containing SAC305 solder alloy were tested at various temperatures. The drop shock experiments were performed according to the Joint Electron Device Engineering Council (JEDEC) drop test standards, with a peak acceleration of 1500G and a pulse duration of 0.5ms. Subsequently, the drop shock reliability of the solder joints under each test condition was assessed using a two-parameter Weibull analysis. The Arrhenius model was also applied to develop a drop life prediction model. Furthermore, comprehensive microscopy analysis was performed to identify the failure modes and trends with increasing temperature. The results indicated that SAC305 performs best at room temperature (25°C). However, its lifespan experiences a substantial decrease as the temperature rises, with reductions of 64%, 76%, and 78% at 50°C, 75°C, and 100°C, respectively. Moreover, a failure mode transition was observed with an increase in temperature.

The third study employed drop shock tests at 25°C and 75°C with SAC305 and SACQ solder alloys on OSP and ENIG surface finishes. Analysis revealed that SACQ generally outperformed SAC305 except for ENIG at 25°C, while both alloys experienced decreased drop life with higher temperature and ENIG surface finish. Notably, SACQ OSP at 25°C showed the best performance, while SAC305 ENIG at 75°C displayed the worst. Additionally, SAC305 OSP exhibited a shift in failure mode from the IMC layer at 25°C to bulk solder at 75°C, while other conditions consistently demonstrated IMC layer failures. These findings underline the significant influence of both temperature and surface finish on drop shock reliability, suggesting SAC-Q and OSP surface finish

as potential choices for drop-resistant devices and emphasizing the importance of considering these factors for optimal solder joint performance in real-world electronics.

## Acknowledgments

I want to acknowledge my deep and sincere gratitude to my advisor, Dr. Sa'd Hamasha, for his immense support, patience, and continuous encouragement. I express my gratitude to him for offering invaluable guidance and sound advice throughout the course of this study. His vast knowledge and logical school of thought have been of great value to me.

I am deeply grateful to my committee members, Dr. George Flowers, Dr. Michael Bozack, Dr. Jia Liu, and Dr. Farah Kandah, for their valuable suggestions and time. I am thankful to the CAVE$^3$ consortium for the technical support. I would also express my gratitude to Dr. Ali Alahmer and Dr. Menghong Wang for consistently providing guidance.

During this work, I have collaborated with several of my colleagues for whom I have great regard: Dr. Xin Wei, Dr. Francy Akkara, Dr. Minghong Jian, Dr. Wally Belhadi, Arvind Srinivasan, Raj Kiran Akula, Abdullah Alakayleh, Sergio Bolanos, Saddam Daradkeh, Shaheen Pouya, Qais Qasaimeh, Soorosh Alavi and Waad Torman.

I sincerely thank my parents, Pranav Vyas, Disha Vyas, and my sister, Prachi Vyas, for their enduring love and immense moral support. I want to express my warm and sincere thanks to my friends, Pooja, Aathi, Madhu, and many more, for their continuous motivation and encouragement.

## Table of Contents

**Chapter 1 General Introduction** ........ 1

1.1 Electronics Packaging ........ 1

1.2 Reliability ........ 4

1.3 Weibull Distribution Analysis ........ 4

1.4 Solder joint reliability ........ 6

1.4 Problem Statement ........ 6

1.5 Research Objective ........ 8

1.6 Dissertation Organization ........ 9

**Chapter 2 Background** ........ 10

2.1 Solder Alloys ........ 10

2.1.1 Tin-Lead Solder ........ 10

2.1.2 Lead-Free Solder ........ 12

2.1.3 SnAgCu Solder Alloys ........ 13

2.1.4 Micro-alloying/Doping ........ 14

2.2 Substrate ........ 15

2.2.1 Substrate Material ........ 16

2.2.2 Surface Finish ........ 17

2.2.3 Solder Mask ........ 18

2.3 Surface Mount Technology Assembly Process ........ 20

2.3.1 Through-Hole Mount Technology (THMT) ........ 26

2.3.2 Surface Mount Technology (SMT) ........ 27

**Chapter 3 Literature Review** ........ 31

3.1 Drop and Shock Testing ........ 31

3.2 Drop Shock Test – Physics of Failure ........ 44

3.3 Effect of Aging on Solder Joints ........ 46

3.3.1 Effect of Thermal Aging on Shock Performance ........ 47

3.4 Effect of Vibration on Solder Joints ........ 48

3.5 Effect of Solder Doping on Reliability ........ 50

3.6 Solder Joint Failure Mechanism ........ 52

3.8 Reliability Prediction Models ........ 54

3.8.1 Input Energy Predictive Model ........ 54

3.8.2 Stress-based Criterion ........ 56

3.9.3 Strain-based Criterion ........ 57

3.9 Hardness Test ........ 57

3.9.1 Vickers Hardness Test ........ 58

3.10 Gaps in the Literature ........ 59

3.10.1 Test Board ........ 59

3.10.2 Experiment........................................................................................................ 60

**Chapter 4 Materials and Methods**........................................................................... 61

4.1 Why BGA?.................................................................................................................. 61

4.2 Solder Alloys.............................................................................................................. 61

4.3 Test Vehicle................................................................................................................ 62

4.4 CABGA208 Design.................................................................................................... 64

4.5 Surface Mount Assembly........................................................................................... 66

4.6 Experimental Setup.................................................................................................... 72

4.6.1 Drop Test Physics.................................................................................................. 76

4.6.2 Room Temperature Drop Test Setup..................................................................... 78

4.6.3 Elevated Temperature Drop Test Setup................................................................. 79

4.6.4 Data Acquisition System........................................................................................ 83

4.7 Failure Analysis.......................................................................................................... 85

4.8 Testing Plans.............................................................................................................. 88

4.8.1 Study I.................................................................................................................... 88

4.8.2 Study II................................................................................................................... 89

4.8.3 Study III.................................................................................................................. 90

**Chapter 5 Comparative Drop Shock Reliability Study of SAC-Based Alloys in BGA Assemblies**........................................................................................................................ 92

5.1 Introduction................................................................................................................ 92

5.2 Test Matrix ........ 93
5.3 Results and Discussions ........ 94
5.3.1 Weibull Analysis ........ 94
5.4 Predictive Modeling ........ 99
5.5 Microstructure Analysis ........ 102
5.5.1 Microstructure Analysis of Eutectic SnPb ........ 104
5.5.2 Microstructure Analysis of SAC305 ........ 107
5.5.3 Microstructure Analysis of Innolot ........ 111
5.5.4 Microstructure Analysis of Cyclomax ........ 114
5.5.5 Microstructure Analysis of Sabix ........ 117
5.6 Hardness Test ........ 120
5.7 Solder Joint Failure Mechanism ........ 122
5.8 Conclusions ........ 123
**Chapter 6 Drop Shock Testing Analysis at Elevated Temperature: Assessing SAC305 Solder Alloy Reliability in BGA Assemblies** ........ 125
6.1 Introduction ........ 125
6.2 Test Matrix ........ 126
6.2 Graphical Abstract ........ 126
6.3 Results and Discussion ........ 127
6.3.1 Weibull Analysis ........ 127

6.3.2 Predictive Modeling ........................................................................................ 130

6.3.3 Microstructure Analysis ........................................................................................ 132

6.4 Conclusions ........................................................................................ 135

**Chapter 7 Drop Shock Test of SAC-Based Alloys at Elevated Temperature** ..................... 137

7.1 Introduction ........................................................................................ 137

7.2 Test Matrix ........................................................................................ 137

7.3 Results and Discussion ........................................................................................ 138

7.3.1 Weibull Analysis ........................................................................................ 138

7.3.2 ANOVA Analysis ........................................................................................ 146

7.3.3 Linear Regression ........................................................................................ 150

7.3.3 Microstructure Analysis ........................................................................................ 152

7.4 Conclusions ........................................................................................ 160

**Chapter 8 Overall Summary, Conclusions, and Future Work** ........................................... 162

8.1 Overall Summary and Conclusions ........................................................................................ 162

8.2 Future Work ........................................................................................ 164

**Bibliography** ........................................................................................ 162

## List of Tables


Table 4.1 Alloy Composition........................................................................................... 61

Table 4.2 Lansmont M23 drop tower specifications ................................................................ 72

Table 4.3 PCB Piezotronics accelerometer specifications......................................................... 73

Table 4.4 Study I test matrix........................................................................................... 88

Table 4.5 Study II test matrix ......................................................................................... 89

Table 4.6 Study III test matrix ........................................................................................ 90

Table 5.1 Test matrix…………………………………………………………………….. 92

Table 5.2 Comprehensive Weibull analysis summary across all alloys………………………..98

Table 6.1 Test matrix……………………………………………………………………..125

Table 6.2 Comprehensive Weibull analysis summary…………………………………………129

Table 7.1 Test matrix…………………………………………………………………….. 137

Table 7.2 Comprehensive Weibull analysis summary…………………………………………145

Table 7.3 Analysis of variance……………………………………………………………146

Table 7.4 Table of Coefficients…………………………………………………………...150

## List of Figures

Figure 1.1 Hierarchy of electronic packaging [6] .......... 3

Figure 1.2 PDF of Weibull distribution with various shape parameters [10] .......... 5

Figure 2.1 Phase diagram of Tin-Lead (SnPb) solder alloy [14] .......... 11

Figure 2.2 Market share of lead-free alloys [18] .......... 15

Figure 2.3 Top view of SMD (left) and NSMD pads (right) [28] .......... 19

Figure 2.4 Cross-section view of SMD and NSMD pads [28] .......... 19

Figure 2.5 SMT assembly process [31] .......... 20

Figure 2.6 Cross-section representation of squeegee blade printing [32] .......... 21

Figure 2.7 Different types of solder paste print [33] .......... 22

Figure 2.8 Types of fiducials [34] .......... 23

Figure 2.9 A typical reflow oven (Left) Reflow zones (Right) [35] .......... 24

Figure 2.10 CABGA X-ray imaging [36] .......... 25

Figure 2.11 Overview of SMT assembly process [37] .......... 26

Figure 2.12 THMT component (examples) [39] .......... 27

Figure 2.13 BGA component (examples) [40] .......... 30

Figure 3.1 Mechanical drop event use conditions [41] .......... 31

Figure 3.2 Typical drop test apparatus (left), assembly set up with board (right) [42] ............... 33

Figure 3.3 Drop test performance [50] ........................................................................................ 35

Figure 3.4 Typical test board in the literature [54] ..................................................................... 37

Figure 3.5 Failure modes analysis [54]......................................................................................... 37

Figure 3.6 IMC of SAC based solder with OSP surface finish .................................................. 39

Figure 3.7 IMC of SAC-based solder with ENIG surface finish................................................ 40

Figure 3.8 Characteristic life comparisons during drop test [65] ............................................... 41

Figure 3.9 Number of drops to failure [68].................................................................................. 43

Figure 3.10 MDOF structural system for JEDEC drop test [70] ................................................ 44

Figure 3.11 PCB bending upon drop impact ............................................................................... 46

Figure 3.12 Cycles to failure under combined temperature-vibration loading [96] .................... 49

Figure 3.13 Solder joint failure modes [110]............................................................................... 53

Figure 3.14 Loading on PCB during drop test............................................................................. 55

Figure 3.15 Schematic of indentation for Vickers microhardness.............................................. 59

Figure 4.1 Test vehicle illustration .............................................................................................. 63

(a) Front side.................................................................................................................................. 64

(b) Back side .................................................................................................................................. 64

Figure 4.3 CABGA208 daisy chain pattern.................................................................................. 65

Figure 4.4 Solder sphere dimensions in CABGA208 component .............................................. 66

Figure 4.5 DEK Europa stencil printing machine.................................................................. 67

Figure 4.6 Pick and place machine ........................................................................................ 68

Figure 4.7 Reflow oven........................................................................................................... 69

Figure 4.8 SnPb and SAC alloys reflow profile ..................................................................... 70

Figure 4.9 X-ray machine ....................................................................................................... 71

Figure 4.10 CABGA208 X-Ray image.................................................................................... 72

Figure 4.11 Lansmont M23 drop tower .................................................................................. 75

Figure 4.12 Acceleration profile; 1500G, 0.5ms .................................................................... 76

Figure 4.13 Typical set of boards and board location............................................................ 78

Figure 4.14 Board location and orientation ............................................................................ 79

Figure 4.15 Typical elevated temperature board setup ........................................................... 81

Figure 4.16 Drop test layout with heating chamber................................................................ 81

Figure 4.17 Drop tower with heating chamber ....................................................................... 82

Figure 4.19 Silicone rubber heater.......................................................................................... 83

Figure 4.20 Keysight DAQ system......................................................................................... 84

Figure 4.21 Multiplexer; 22 channels ..................................................................................... 84

Figure 4.22 Keysight BenchVue software .............................................................................. 85

Figure 4.23 Pace Technologies automated grinding-polishing machine ..................................... 86

Figure 4.25 Polishing alumina suspension of various sizes........................................................ 87

Figure 4.26 ZEISS Axio Imager.M2m optical microscope ........................................................ 88

Figure 5.1 Acceleration profiles; 500G -3000G ......................................................................... 94

(a) SnPb Weibull plot................................................................................................................... 95

(b) SAC305 Weibull plot ............................................................................................................. 96

(c) Innolot Weibull plot ............................................................................................................... 96

(d) Cyclomax Weibull Plot .......................................................................................................... 97

(e) Sabix Weibull plot.................................................................................................................. 97

Figure 5.2 Weibull plots for all alloys at all G levels (a) SnPb (b) SAC305 (c) Innolot (d) Cyclomax (d) Sabix ................................................................................................................... 98

Figure 5.3 Characteristic lives for all alloys ............................................................................... 98

Figure 5.4 Velocity change calculation for 1500G and 0.5 ms pulse based on effective pulse with acceleration ≥ 150G ................................................................................................................ 100

Figure 5.5 Characteristic life vs Input energy............................................................................ 102

(a) SnPb solder joint after reflow................................................................................................ 105

(b) SnPb at 500 G - bulk solder failure ....................................................................................... 105

(c) SnPb at 1000G - bulk solder failure ...................................................................................... 106

(d) SnPb at 1500 G – bulk solder failure ........ 106

(e) SnPb at 2000G – bulk solder failure........ 107

Figure 5.6 SnPb solder joint microstructure after reflow and post failure for all G levels........ 107

(a) SAC305 solder joint after reflow ........ 108

(b) SAC305 at 1000 G - bulk solder failure........ 108

(c) SAC305 at 1500 G – mixed failure pattern ........ 109

(d) SAC305 at 2000 G - mixed failure pattern ........ 109

(e) SAC305 at 2000 G – mixed failure at board side and IMC layer failure at component side 110

(f) SAC305 at 2500 G - IMC layer failure........ 110

(g) SAC305 at 2500 G - IMC layer failure at component side ........ 111

Figure 5.7 SAC305 solder joint microstructure after reflow and post failure for all G levels ... 111

(a) Innolot solder joint after reflow........ 112

(b) Innolot at 1500 G - IMC layer failure ........ 112

(c) Innolot at 2000 G - IMC layer failure ........ 113

(d) Innolot at 2500 G - IMC layer failure ........ 113

(e) Innolot at 3000 G - IMC layer failure ........ 114

Figure 5.8 Innolot solder joint microstructure after reflow and post failure for all G levels...... 114

(a) Cyclomax solder joint after reflow........ 115

(b) Cyclomax at 1500 G - IMC layer failure ... 115

(c) Cyclomax at 2000 G - IMC layer failure ... 116

(d) Cyclomax at 2500 G - IMC layer failure ... 116

(e) Cyclomax at 3000 G - IMC layer failure ... 117

Figure 5.9 Cyclomax solder joint microstructure after reflow and post failure for all G levels. 117

(a) Sabix solder joint after reflow ... 118

(b) Sabix at 1500 G - IMC layer failure ... 118

(c) Sabix at 1500 G - IMC layer failure ... 119

(d) Sabix at 2500 G - IMC layer failure ... 119

(e) Sabix at 3000 G - IMC layer failure ... 120

Figure 5.10 Sabix solder joint microstructure after reflow and post failure for all G levels ... 120

Figure 5.11 Hardness test for all the alloys Each bubble represents a data point. The lower upper sides of the box represent 25$^{th}$ and 75$^{th}$ percentiles. The bars represent 10$^{th}$ and 90$^{th}$ percentiles. ... 121

Figure 5.12 Characteristic life vs hardness correlation ... 121

Figure 5.13 Solder joint failure mechanism ... 122

Figure 5.14 SAC305-Board 7, C1 Joint at 2500G ... 123

Figure 6.1 PCB Fabrication and Reliability testing overview ... 127

Figure 6.2 Weibull plots for all temperatures ........................................................................ 129

Figure 6.3 Characteristic life and β10 life for all temperatures ............................................... 129

Figure 6.4 Arrhenius model fitting curve .................................................................................. 131

Figure 6.5 Summary of all observed failure modes .................................................................. 133

Figure 6.6 Microstructure Analysis SAC305 solder joints at all temperatures: (a) 25°C- IMC layer failure, (b) 50°C – IMC layer failure, (c) 75°C – Bulk solder failure, (d) d) 75°C – Mixed failure pattern, (e) 100°C, Mixed failure pattern, and (f) 100°C – Bulk solder failure………...134

Figure 7.1.1 Weibull plot for SAC305 with OSP Surface finish at 25°C and 75°C. Each data point represents the number of drops to failure for each test vehicle. Scale parameter represents 63.2% of failures and shape parameter represents the slope of the fitted plot........................... 139

Figure 7.1.2 Weibull plot for SACQ with OSP Surface finish at 25°C and 75°C...................... 140

Figure 7.1.3 Weibull plot for SAC305 with ENIG Surface finish at 25°C and 75°C ................ 141

Figure 7.1.4 Weibull plot for SACQ with ENIG Surface finish at 25°C and 75°C ................... 142

Figure 7.1.5 Weibull plot for all conditions.............................................................................. 143

Figure 7.2 Characteristic life for all conditions SACQ in general exhibited a higher drop shock life compared to SAC305 except for one case at 25°C and ENIG surface finish where SAC305 outperformed SACQ. ............................................................................................................ 144

Figure 7.3 B10 life for all conditions.......................................................................................... 145

Figure 7.4 Interaction plot of characteristic life at 25°C Each data point represents the characteristic life at that condition. Bottom left plot represents the change in characteristic life as

the alloy changes, for both surface finishes. Top right plot represents the change in characteristic life as the surface finish changes, for both alloys. ..................................................................... 148

Figure 7.5 Interaction plot of characteristic life at 75°C .......................................................... 149

Figure 7.6 Main effect plot of characteristic life Each data point represents the mean of characteristic life for each condition. The plot represents the trend in characteristic life with variable change. ........................................................................................................... 150

Figure 7.7 SAC305_OSP_25°C – IMC layer failure.................................................................. 153

Figure 7.8 SAC305_OSP_75°C – bulk failure ........................................................................... 154

Figure 7.9 SAC305_ENIG_25°C – IMC layer failure ............................................................... 155

Figure 7.10 SAC305_ENIG_75°C – IMC layer failure ............................................................. 156

Figure 7.11 SACQ_OSP_25°C – IMC layer failure.................................................................. 157

Figure 7.12 SACQ_OSP_75°C – IMC layer failure.................................................................. 158

Figure 7.13 SACQ_ENIG_25°C – IMC layer failure................................................................ 159

Figure 7.14 SACQ_ENIG_75°C – IMC layer failure................................................................ 160

## List of Abbreviations

| | |
|---|---|
| $\beta$ | Shape Parameter |
| β1, β2, β3. β4 | Regression coefficients |
| β10 | 10% life |
| $\theta$ | Scale parameter |
| A | Pre-exponential factor |
| Ag | Silver |
| Au | Gold |
| a(t) | Input acceleration |
| AOI | Automated optical inspection |
| BGA | Ball Grid Array |
| Bi | Bismuth |
| $C_1$ and $C_2$ | Constants |
| C4 | Controlled collapse chip connection |
| CABGA | Ceramic array ball grid array |
| CCGA | Ceramic column grid array |
| CTE | Coefficient of thermal expansion |
| CSP | Chip scale package |
| Cu | Copper |
| $E_{input}$ | Input Energy |
| $E_a$ | Activation Energy |
| EDX | Energy dispersive X-Ray |

| | |
|---|---|
| ENIG | Electroless nickel immersion gold |
| FR | Flame retardant |
| HASL | Hot air solder leveling |
| I/O | Input/output |
| IC | Integrated circuit |
| IMC | Intermetallic compound |
| ImAg | Immersion silver |
| In | Indium |
| IR | infrared |
| JEDEC | Joint electron device engineering council |
| JEIDA | Japan Electronics Industry Development Association |
| k | Number of drops to failure |
| L | Drop life |
| MDOF | Multiple degrees of system |
| NSMD | Non-solder mask defined |
| Ni | Nickel |
| OEM | Original equipment manufacturer |
| OSP | Organic solderability preservative |
| P | Phosphorus |
| Pb | Lead |
| Pd | Palladium |
| PBGA | Plastic ball grid array |
| PC | Personal computer |

| | |
|---|---|
| PCA | Printed circuit assembly |
| PCB | Printed circuit board |
| PDF | Probability density function |
| QFP | Quad Flat Package |
| R | Gas constant |
| RoHS | Restriction of hazardous substances |
| SA | Solder alloy |
| SAC | SnAgCu |
| Sb | Antimony |
| SEM | Scanning electron microscope |
| SF | Surface finish |
| SMD | Solder mask defined |
| SMR | Surface mount resistor |
| SMT | Surface mount technology |
| Sn | Tin |
| TAL | Time above liquidus |
| TBGA | Thin ball grid array |
| THMT | Through hole mount technology |
| V | Velocity |
| WEEE | Waste Electrical and Electronic Equipment |
| Zn | Zinc |

# Chapter 1 General Introduction

## 1.1 Electronics Packaging

Electronic packaging is an electronic manufacturing process involving the assembly of electronic components. This method creates the interconnection and operating environment for the electronic components to perform the required functions. The Printed Circuit Board (PCB), a thin board constructed of fiberglass, composite epoxy, or other laminate material, is used in many electronic devices. This electronic board may be the foundation upon which other electronic parts are attached. One side or both sides of the PCB may have connections. The PCB offers the necessary electrical connections between various components and mechanical support for other electronic components. Transistors, resistors, capacitors, and integrated circuits are active and passive electronic components that can be attached to the PCB. [2] Through-Hole Mount Technology (THMT) and Surface Mount Technology are the two main techniques for mounting electronic components on the PCB (SMT). Through-hole components' leads are inserted into the board via through-holes to connect the package and PCB in the THMT. After that, the leads, pads, and solder are joined. Surface energy and cooling are used to create a solid metallic bond. Wave soldering is one of the most popular techniques for mounting in THMT, under which multiple components are soldered simultaneously. Components are either placed on the PCB or introduced during wave soldering. Their legs are cut close to the board and bent to keep the component in place. The PCB is then carried across a wave of liquid flux, where the bottom side of the board interacts with the flux. After being heated, the PCB is carried across a wave of melted solder. The soldering is complete when the solder adheres to the component legs and solder pads. Numerous problems with this mounting technique include cracked joints, lifted components, solder skip, inadequate

penetration, and a limited number of connection points. [3] Solder joints are another typical method of component mounting in SMT. The components are mounted using a filler metal "solder" in SMT. Solder refers to an alloy (a substance composed of two or more metals) that creates a joint (connection) between the components and the PCB. As a result, a solder joint is used to connect the two parts. Several benefits can be obtained when SMT is used instead of THMT, such as the ability to assemble PCBs on both sides, achieve smaller pitch sizes, reduce electrical noise and delay, and ease with which SMT can be automated. Considering these two mounting options, there are three assembly options for electronic packaging, each with a unique set of processing steps. In the second type, SMT is utilized on one side of the PCB, and SMT and THMT are used for the assembly on the second side. The final type of assembly is carried out using THMT on one side and SMT on the other. Different alloys, such as SAC solder alloys and leaded solder alloys, can be used in SMT to create solder joints. Reflow soldering is the process of melting solder paste, a combination of flux and solder powder, while carefully regulating the reflow oven's temperature to form strong connections between the substrate and the electronics components [4]. Intermetallic compounds (IMC), whose thickness depends on the reflow duration and temperature, are created between the solder and the pad during reflow [5]. The decline in the lifetime and electrical performance is a function of the thickening IMC layer, which causes problems with long-term reliability. The electronic packaging process has three main functions. These functions are signal distribution, power distribution, heat dissipation, and protection [6]. Moreover, there are four primary levels of packaging (Figure 1.1) which are:

1$^{st}$ level: Integrated circuit assembled in the silicon chip

2$^{nd}$ level: Connection between chip and package

3$^{rd}$ level: Interconnections between the chip carrier and PCB

$4^{th}$ level: Mounting of daughterboards to the motherboard

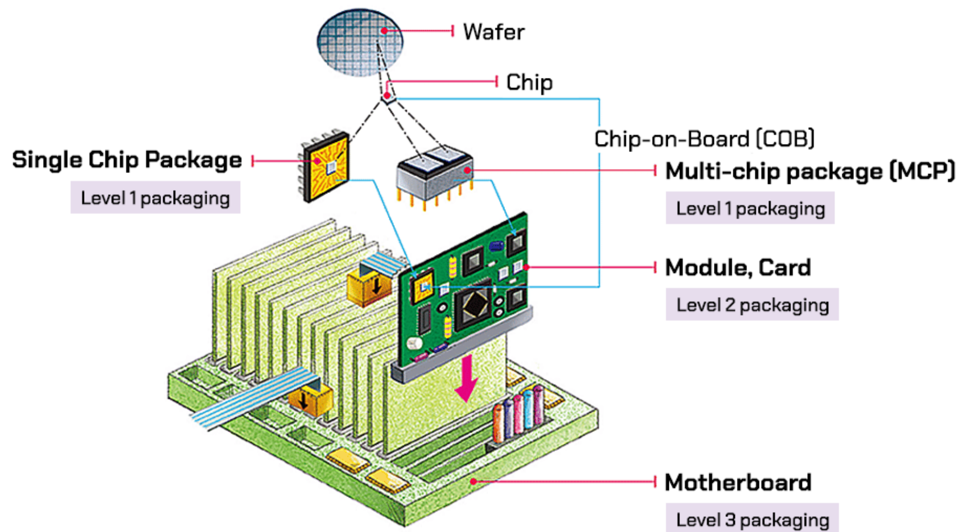



Figure 1.1 Hierarchy of electronic packaging [7]

Level zero is a gate-to-gate interconnection in the silicon die. It is mainly the fabrication of the silicon die from the single-crystal silicon wafer and numerous solid-state electronic components, such as transistors, resistors, and capacitors, to make functional electrical circuitry.

Level one refers to the connection between the package and the manufactured silicon chip formed in level zero. This is the level where the silicon chip is joined to the lead frame or interposer layer utilizing wire bonding or flip-chip technology. This link gives silicon chip mechanical support, active region protection, thermal management, and handling.

Level two is the package and PCB connection. The Printed Circuit Board is usually a rigid laminate consisting of layers of fiberglass-epoxy composite. The PCB or substrate offers thermal management, electrical connection and isolation, and a flat mounting surface for soldering parts [4].

Level 3 is the connection between printed circuit boards, for instance, mounting a daughter card to a motherboard. This PCB is typically used to give the device some extra capabilities. For instance, anyone may upgrade their PC with a new, powerful graphics card to improve performance and visual quality.

### 1.2 Reliability

Reliability is the probability that a system or component will carry out a necessary function for a predetermined time when operated under predetermined conditions. Poet Samuel Taylor Coleridge was the one who first used the term, which dates to 1816 [8]. The reliability, or failure probability, increases over time due to variations in production processes and operational circumstances. Failure distributions as a function of time are produced using failure data from the tests (accelerated life testing). Electronic devices are divided into three categories based on the various requirements for service life and reliability as per IPC-STD-001B [9], [10]

Class I: Consumer goods or goods for everyday use. This class has a service life of fewer than five years and has a low-reliability criterion. Among these goods include TVs, PCs, etc.

Class II: Industrial products. This class has a longer service life and a more significant reliability requirement than class I. Ovens, washing machines, and other items fall under this category.

Class III: Critical products. Here, the highest reliability standards apply, and the service life is over 20 years. Failure can threaten your life. These goods include ships, space shuttles, and other things.

### 1.3 Weibull Distribution Analysis

The Weibull distribution analysis is widely used to evaluate the experimental data from accelerated life testing. The key benefit of the Weibull analysis is its flexibility in modeling many types of data sets, as it can be used to assume the characteristics of many different distributions. The

capacity to provide somewhat accurate failure analysis and forecasts with small samples is another benefit of the Weibull analysis [10]. The Weibull distribution's probability density function (PDF) is expressed as:

$$F(t) = \frac{\beta}{\theta}(\frac{t}{\theta})^{\beta-1} - e^{-\left(\frac{t}{\theta}\right)^{\beta}} \quad (1.1)$$

Here, Beta ($\beta$) is the shape parameter. For $\beta$<1, the PDF is similar to the exponential distribution; for $\beta$>3, the PDF is likely to be symmetric, similar to the normal distribution; for 1<$\beta$<3, the PDF is skewed. When $\beta$=1, the failure rate is constant, and the distribution is identical to the exponential distribution. Figure 1.2 shows the effect of shape parameters on the Weibull distribution probability density function.

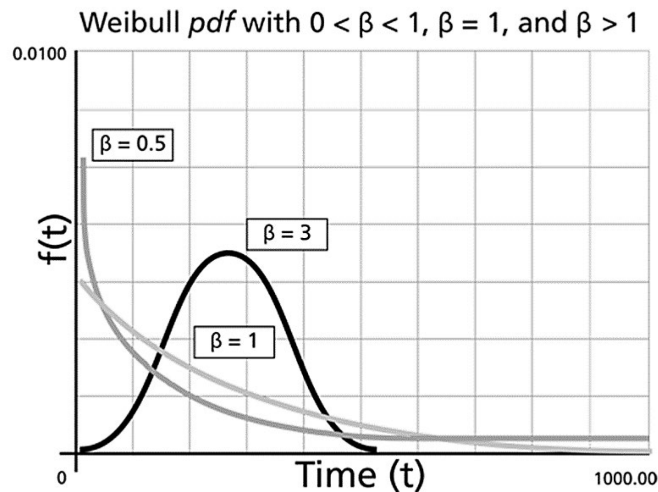



Figure 1.2 PDF of Weibull distribution with various shape parameters [11]

Theta ($\theta$) is the scale parameter, also known as the characteristic life, and it denotes the probability of failure for 63.2% of the population. To forecast the fatigue life in a fatigue test, the theta parameter of the Weibull distribution is commonly used. For a Weibull distribution with only $\beta$

and $\theta$ parameters it is called a two-parameter Weibull distribution. When there is a minimum life $t0$ ($T$>$t0$) exiting, a three-parameter Weibull distribution ($\beta$, $\theta$ $and$ $t0$) will be the best fit. By applying the three-parameter Weibull distribution, we assume no failures will occur before the minimum life $t0$.

### 1.4 Solder joint reliability

Solder joints are used to connect electronic components mechanically and electrically to printed circuit boards (PCBs) and other electronic substrates. The reliability of these joints is important for the overall performance and reliability of the device. During a mechanical drop shock test, the solder joints in an electronic device are subjected to shock loads and impacts that can affect their strength and reliability. If the solder joints cannot withstand the shock loads, they may fail, which can cause complete failure of the PCB.

### 1.4 Problem Statement

Portable electronic products such as cellular phones, digital cameras, and tablets are growth areas for the electronics manufacturing industry. The product and packaging design trends continue pushing for smaller form factors and increased functionalities. Portable electronic products are prone to accidental drops. They can cause internal circuit board damage, for example, solder joint failures by brittle fracture at the solder joint intermetallic compound (IMC) interfaces or by impact fatigue in the solder materials. If the solder joint is robust, the failure site can migrate to the board copper traces or even resin cracking. When an electronic product drops on the ground, impact force, and deformation are transferred internally to the printed circuit board (PCB), solder joints, and Integrated Circuits (IC) packages. The IC packages are susceptible to solder joint cracks induced by PCB bending and mechanical shock inertia during the impact event. If a single drop event does not cause failure, repeated drop events can cause impact fatigue or accumulated damage

and rupture of interconnection joints and assembly materials. Drop testing provides a practical experimental approach to design for drop reliability.

The switch to lead-free doped solders is a concern receiving more attention. How lead-free doped interconnects would behave in drop shock tests is primarily unknown. Many of these solders' dynamic properties are still being studied. Only a limited number of drop tests have been conducted to compare the drop resistance of Pb-free doped and leaded solders. Additionally, the need to develop new PCB design guidelines for Pb-free, doped, drop-resistant packages has increased as a result in the electronic packaging industry.

Studies have been conducted on the effect of PCB surface finish (e.g., ENIG or OSP) on the thermal fatigue reliability performance of Sn–Ag–Cu solder joints and their underlying failure mechanism. However, the influence of surface finish on drop impact reliability has not been readily documented, and the failure mechanism needs further characterization.

Solder joints are often exposed to temperature-changing environments, in addition to drop/vibration in actual service conditions, exposing them to thermal and/or mechanical stresses for an extended period. Electronic packages experience warpage and distortion during temperature excursions during the manufacturing process and in real-world operating conditions, in addition to shear deformation brought on by CTE mismatch. Additionally, solder joints may be subjected to mechanical and environmental stresses (drop, vibration) in actual service. As a result, shear and tensile loads are applied to solder joints in most applications [12].

While most studies focus on drop shock reliability at room temperature, only a small amount of research has been presented to examine the drop shock performance of solder joints under various elevated temperatures [13]. There is a need to systematically study the effect of simultaneous

thermal and mechanical loadings on the drop shock performance of SAC-based alloys in BGA assembly.

### 1.5 Research Objective

The motivation behind this dissertation is to determine the drop shock reliability of various lead-free solder alloys under realistic service conditions. Several commercially available solder alloys will be tested under varying temperatures and impact profiles and on boards with different surface finishes. Reliability prediction models will be developed for these solder alloys for realistic conditions.

Below are the objectives of this research:

1. Develop test design, testing fixture, and experimental setup for testing different solder alloys at room and elevated temperature conditions.
2. Study the drop shock reliability of different lead-free solder alloys at various acceleration levels.
3. Study the effect of temperature on drop shock testing for lead-free solder alloys.
4. Study the effect of surface finish on the drop shock performance of lead-free alloys under room and elevated temperature conditions.
5. Perform Weibull analysis and determine reliability parameters such as characteristic life ($N_{63}$) and β -10 life to compare the drop shock performance of various solder alloys.
6. Develop reliability prediction models based on the physics of failure for solder alloys tested under different acceleration levels and temperature conditions.

7. Perform microstructure analysis to determine the failure modes and its trends using optical microscopy.

### 1.6 Dissertation Organization

This dissertation consists of eight chapters. Chapter I introduces electronic packaging and reliability. It also provides a detailed problem statement and research objectives. Chapter II introduces various concepts related to electronics packaging and electronics reliability. Chapter III provides a thorough literature review in accordance with drop testing (room and elevated temperatures), thermal cycling, thermal aging, vibration testing, reliability modeling and solder joint failure mechanisms. Chapter IV describes the test vehicle, experimental setup, solder alloys, failure analysis, and the three study plans. Chapter V explores the drop shock performance of solder alloys SnPb, SAC305, Innolot, Cyclomax, and Sabix in BGA assemblies at various G-levels. Chapter VI Studies the drop shock performance of SAC305 solder alloy in BGA assemblies at four different temperatures. Chapter VII studies the drop shock performance of SAC305 and SACQ solder alloys in BGA assemblies assembled with two different surface finishes at two different temperatures. Chapter VIII summarizes the dissertation work and provides conclusions and future work.

# Chapter 2 Background

## 2.1 Solder Alloys

Solder alloys, which are mixtures of several metals, are used to create solder joints. Solder joints serve as a permanent metallurgical bond between PCBs and electronic components. Tin (Sn), lead (Pb), copper (Cu), silver (Ag), bismuth (Bi), and other elements are frequently used in the electronic industry to make solder alloys. The connections between components and the PCB are solder joints during the soldering process. Solder joints can provide mechanical, electrical, and thermal connections, making them essential to the effectiveness, reliability, and quality of electronic components.

### 2.1.1 Tin-Lead Solder

Tin-Lead (SnPb) solder has been the most widely used solder alloy. Over 2000 years ago, the Romans began using it in aqueducts [14]. The electronic industry's most prevalent SnPb solder alloys is a mix of 63%Sn and 37%Pb by weight [4] This choice was made because the alloy is eutectic, meaning it has a critical temperature above which the entire alloy melts and a critical temperature below which it solidifies. The eutectic 63%Sn-37%Pb alloy has a 183°C melting temperature. Figure 2.1 below displays the binary alloy Sn-phase Pb's diagram.

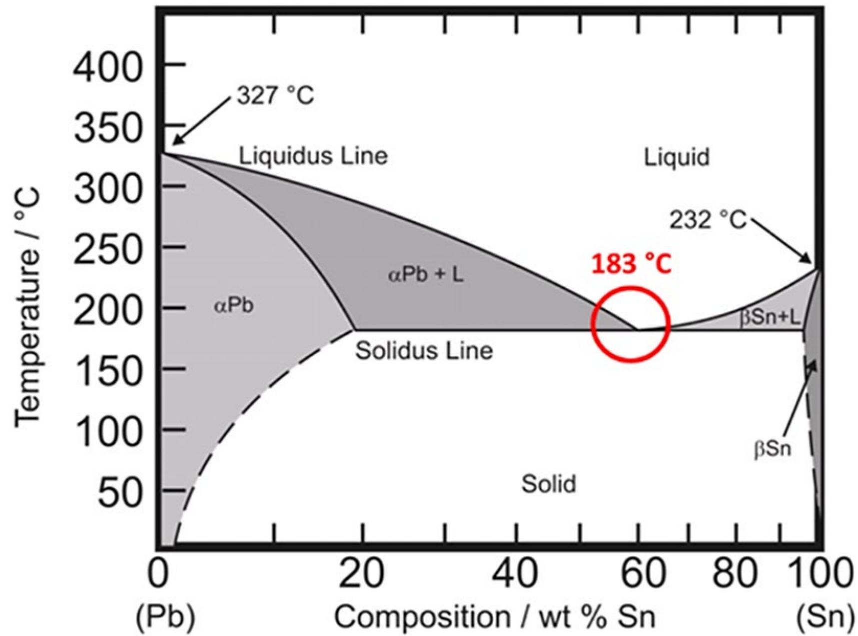



Figure 2.1 Phase diagram of Tin-Lead (SnPb) solder alloy [15]

Compared to non-eutectic alloys with a pasty range, the eutectic SnPb alloy is simpler to work with. A set of temperatures known as the "pasty range" is when the alloy is both partially solid and liquid. For instance, a 60%Sn-40%Pb alloy has a pasty range between 183°C and 188°C, where 188°C causes the alloy to become liquid. Regarding surface mount assembly, pasty range alloys are not advised. The 63%Sn-37%Pb alloy has a melting point of roughly 183°C, which is lower than the Sn and Pb elements' 232°C and 327°C, respectively. There are many benefits of the eutectic 63%Sn-37%Pb alloy over other tin-lead alloys such as [4]:

- Eutectic composition with a unique melting temperature
- Provides excellent electrical, thermal, and mechanical performance in electronic packaging
- Strong joint above or below room temperature
- Low cost
- Good wetting

- Fair fatigue resistant
- Higher electrical conductivity

### 2.1.2 Lead-Free Solder

Despite the widespread use of SnPb solders in the electronic industry, lead usage raises environmental issues. If lead is present in an electronic product, there is no issue. After being used, the product is disposed of in a landfill, where lead may seep out and eventually build up in drinking water pipes. Leads negatively impact human health. It can lead to neurological, reproductive, and physical development issues. Young children who are lead-poisoned suffer from impaired brain growth [16].

Considering the dangers of lead, legislation was explored restricting its use in the United States in the early 1990s. The Japan Electronics Industry Development Association (JEIDA) committee created the roadmap to commercialize lead-free solders in 2000. The IPC organization in the US put up a strategy in the year 2000 that focused on lead-free solder research and development [17]. The Directive on Waste of Electrical and Electronic Equipment (WEEE) and the Directive on the Restriction of Hazardous Substances (RoHS) in electrical and electronic equipment were two pieces of legislation the European Commission proposed in 2008.

After the proposed legislation, the electronics industry looked for a new alloy solder to replace the standard tin-lead solder known as lead-free solders. In selecting lead-free solder alloy, the following aspects were considered:

- Environment-friendly
- Good wetting
- Similar physical properties as eutectic tin-lead
- Melting temperature similar to eutectic tin-lead

• Smaller pasty range temperature in the phase diagram

• Longer shelf life

Lead-free solder alloys were not available to replace the eutectic tin-lead. Commercially available lead-free solder alloys were available, depending on the utilization application. Studies were done to select the best alloys for particular purposes. Industries ultimately settled on the SAC alloys.

### 2.1.3 SnAgCu Solder Alloys

Sn-Ag-Cu (SAC) solder alloys are the most widely used lead-free solders and are considered the best substitutes for eutectic Sn-Pb solder alloys. They were chosen since neither silver nor copper is oxidation or corrosion-sensitive. It has also been demonstrated that tin gains more mechanical qualities when combined with silver and copper. Due to their proximity to eutecticity, relatively low melting temperature, good thermal fatigue resistance, solderability, strength, and wettability, SAC family solder alloys are pretty standard. The most popular SAC solder alloys typically have a eutectic composition with 3-4% Ag, 0.5-1% Cu, and Sn as the last component. SAC alloys such as SAC305 (96.5Sn-3.0Ag-0.5Cu), SAC105 (98.5Sn-1.0Ag-0.5Cu), SAC387 (95.5Sn-3.8Ag-0.7Cu), SAC396 (95.5Sn-5.5Ag-0.6Cu) and more have all been introduced by solder firms and research organizations. Each of these alloys has been employed for a range of applications.

Even though the SAC solder alloy family has demonstrated some excellent properties, they still have significant drawbacks compared to Sn-Pb solder alloys in terms of melting temperature, cost per unit, and some reliability issues (e.g., Sn-Pb components show better board level reliability in drop test than SAC305).

### 2.1.4 Micro-alloying/Doping

Several elements were doped or micro-alloyed into lead-free solder alloys based on SAC to enhance their qualities. Doping is a process used in the semiconductor industry to create new alloys by adding dopants to conventional solder alloys. However, in solders, the proportion of dopants may be much higher than in the semiconductor business, which is restricted to less than 1%. Some elements employed as dopants are Bi, Sb, In, Mg, Ti, Zn, Ce, Co, Ni, and La [18]. It has been discovered that micro-alloying with these elements improves wetting, shock/drop resistance, and other mechanical qualities. For instance, adding bismuth (Bi) to lead-free solder alloys improves shear strength and reduces the thickness of the IMC layer. There are also applications where other elements replace Cu or Ag in SAC-based alloys. Some examples of such cases are listed below.

Sn42Bi58 - solder with a Tin-Bismuth Eutectic composition and a 138°C low melting point could reduce thermal damage. Bismuth content also improves mechanical strength. However, bismuth is not very readily available in the market.

48Sn52In - Tin-Indium with a melting point of 118°C is a eutectic solder. While indium is not easily accessible, its presence reduces the alloy's mechanical strength.

20Sn80Au - Tin-Gold eutectic solder with a high melting point of 280°C. Despite a high melting point, this alloy is still considered solder because its temperature is lower than 350°C, which is the temperature at which braze materials begin to melt. High alloy hardness results in more rigidity than conventional solders but poses some manufacturing challenges. Additionally, gold makes it pricey.

95Sn5Sb - Tin-Antimony is a non-eutectic solder with a pasty range of 232°C - 240°C. It could be employed in high-temperature applications because of its high melting point. Sb increases the

alloy's strength and hardness and performs well in thermal fatigue. However, the alloy has poor wetting characteristics, and antimony toxicity is another issue.

91Sn9Zn - Tin-Zinc Eutectic solder with a melting point of 199°C. With an increase in zinc content, strength and melting point rise. However, zinc is prone to corrosion, so this alloy has poor wettability and corrosion concerns.

Figure 2.2 represents the market share of lead-free alloys.

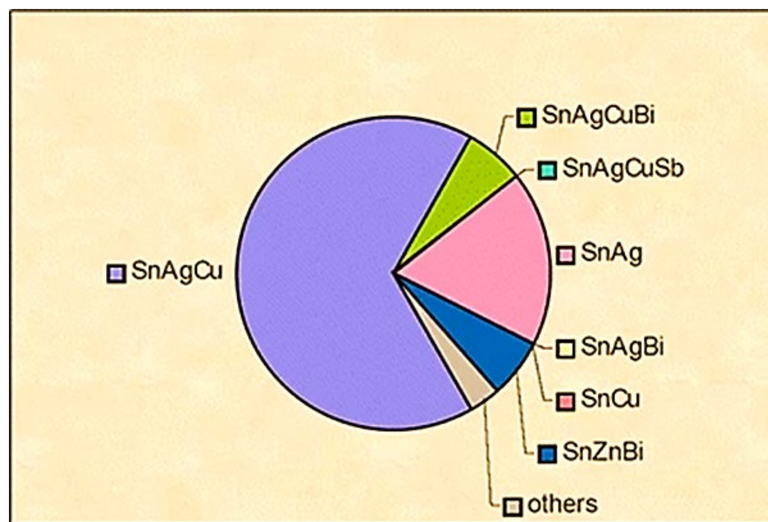



Figure 2.2 Market share of lead-free alloys [19]

## 2.2 Substrate

A Printed Circuit Board (PCB) is usually a rigid structure comprising a non-conductive substrate and metal traces. The electronic components are soldered mechanically to the flat substrate and electrically to the traces; in other words, a PCB's flat surface supports electronic components mechanically, and the metal traces bring the components together electrically. The PCB is also responsible for electrical isolation and heat dissipation. A single layer of circuitry (on top or bottom) or several layers of circuitry stacked together may make up the board. Vias could be used

to connect different layers electrically. The different types of vias include buried vias, which are incorporated inside the PCB to connect internal layers; blind vias, which are exposed on one side of the board; and through-hole vias, which electrically connect the top and bottom layers. Sometimes, thermal vias are designed in specific applications to help speed up heat dissipation.

### 2.2.1 Substrate Material

Printed circuit boards are built using a dielectric core material with poor electrical conductivity, followed by additional metal and dielectric layers to ensure the best circuitry transmission possible. Polymer substrates such as Teflon, phenolic, epoxy, polyimide, and polyamide and reinforcement such as paper, glass fabric, and kevlar are often used for dielectric material. When choosing the suitable substrate material for real applications, one should carefully consider the glass transition temperature since, at this temperature, the CTE of the substrate material changes from brittle to elastic. The maximum operating temperatures for FR-4 and polyimide are 120°C and 230°C, respectively (their glass transition temperature). Additionally, the CTE of substrates varies greatly from horizontal to vertical. Constrained expansion in the x-y plane is made possible by additional glass reinforcing; however, the CTE may be anisotropic. While the CTE of the laminate substrate in the x-y plane is typically between 14 and 18 ppm/°C to match well with copper's 16 ppm/°C, it is ten times higher in the Z direction at 100 to 200 ppm/°C. Designing a substrate with a reasonable thickness is crucial to prevent potential reliability difficulties.

The standard dielectric material for PCB is FR-4, a flame-resistant composite of woven fiberglass cloth and epoxy resin. FR represents flame retardant, and 4 indicates woven glass-reinforced epoxy resin [20]. Here, glass fibers are the base material that provides laminate stability, while epoxy resin enables additional ductility. Besides, the ceramic substrate is also available in harsh-environment applications such as military and aerospace. Even though ceramic substrate prices are

much higher, the characteristics of higher thermal conductivity and lower CTE are preferred by PCB designers since more options are available.

### 2.2.2 Surface Finish

The surface finish is applied to the PCB with the primary goal of preventing Cu oxidation, which will improve the soldering of the component. The most popular surface treatments include Hot Air Solder Leveling (HASL), Immersion Silver, Immersion Tin, Ni/Au Electroless Process, Ni/Au Electroplating Process, Pd or Ni/Pd Electroless Plating, and Organic Solderability Preservative (OSP). A surface finish is applied after cleaning the copper that was exposed after curing the solder mask. By using flux and dipping into Sn/Pb solder, the HASL surface finish is accomplished. While the solder is still molten, extra solder is removed from the pads using hot air knives. This procedure leaves the copper covered in a thin layer of solder. A few problems with the HASL surface finish include board warping, delamination, waves in the plated surface, uniformity in the solder paste, and damage to the plated holes [21].

After applying a solder mask to the PCB, the electroless Ni is applied over the exposed copper. A layer of gold follows this to complete the Ni/ Au electroless surface finish. This surface finish also makes use of the immersion Au process. This method results in a flat and uniform surface with good wettability. For this kind of surface finish, issues concerning brittle interfacial fracture are addressed [22]. The Ni coating, which produces a homogeneous surface, is the main component of the Ni/Au electroplating surface finish. The Au finish gives good wettability and high strength. The "black pad" issue affects the pad site and is related to this surface finish. The black pad, essentially a fracture in the solder joint leaving an open circuit with dark corroded nickel, is visible after removing the BGA [23], [24]. Another surface finish is immersion Ag; employing it lowers the probability of embrittling Au-Sn intermetallic compounds developing (IMCs). The primary

benefits of an immersion Ag surface finish include ease of application, provision of a solderable coating, and low cost [25].

Two layers of $Cu_3Sn$ and $Cu_6Sn_5$ are formed between the Sn and the Cu layer in the immersion tin surface finish. The growth in the thickness of these layers depends on the temperature and time. A thin coating is created on the substrate due to immersion tin, which provides a good solderability feature. The inside surface of copper water tubing is finished with immersion tin to avoid corrosion. Tiny whiskers grow as time goes on, reducing reliability [26], [27]. The organic coating is penetrated into the exposed copper in the OSP surface finish, where it is dissolved into the flux and molten solder before being wet onto the copper surface to create the solder joint. This creates a temporary layer that prevents copper oxidation. The thermal processes that must be completed before attaching the solder sphere to the OSP substrate depend on the thermal resistance and anti-oxidation of the copper surface. There are two ways to protect the copper surface: to apply the OSP surface finish. The first method, which is not considered the best, employs resins or active resins for preflux. The second method, considered the most effective for applying the OSP surface finish, uses benzotriazoles and imidazole chemistries. Compared to other surface finish types, the OSP surface finish is less expensive, has excellent pad coplanarity and constant solderability, and is simple to visually detect any deteriorated copper. On the other hand, it has a short shelf life—typically between six and twelve months—is too sensitive to physical contact, and degrades quickly in hot or humid settings [28].

### 2.2.3 Solder Mask

Solder mask is a gloss-like polymer layer applied to the PCB to protect the Cu traces (usually Acrylate and Epoxy). The main objective is to stop solder bridges and protect copper traces from oxidation. The pads might be solder mask-defined (SMD) or non-solder mask-defined (NSMD).

SMD pads have solder mask apertures such that the opening is smaller than the diameter of the copper pad. SMD is weaker than NSMD because there is less contact area due to the distance between the mask and the pads. Figures 2.3 and 2.4 illustrate the NSMD and SMD regions.

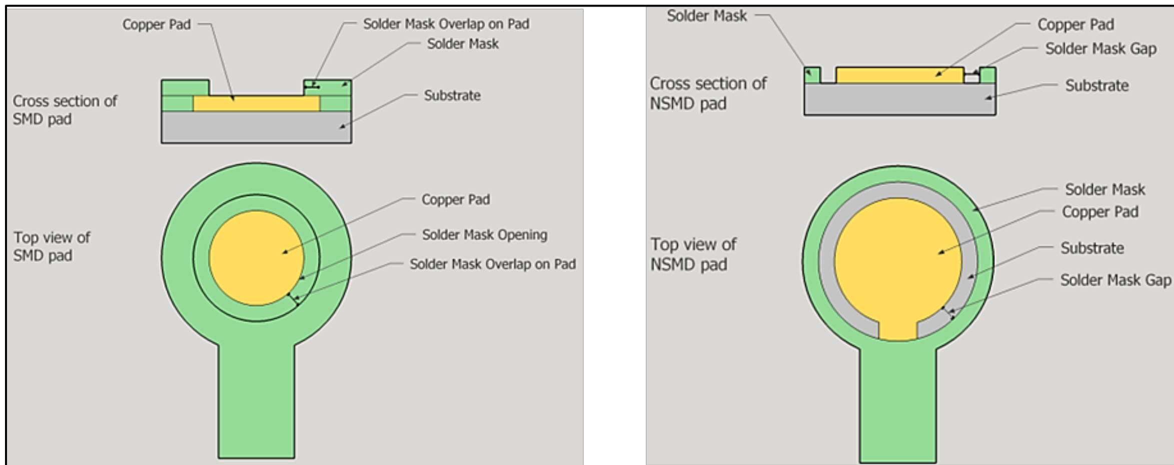



Figure 2.3 Top view of SMD (left) and NSMD pads (right) [29]

The SMD gives less area than the original Cu pad, as seen in the image above, where it overlaps the Cu pad area. In contrast, the soldered region fills all the pads in NSMD because there is room between the Cu pad and mask. Due to better stress distribution throughout the contact region than SMD, NSMD showed improved resistance to thermo-mechanical fatigue [4], [30], [31].

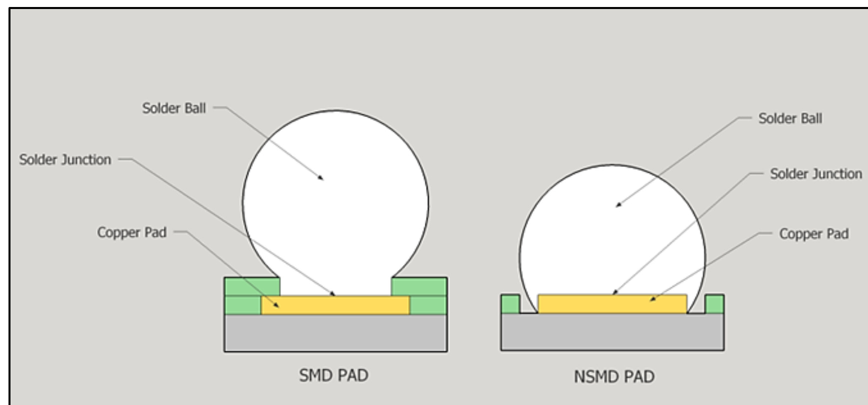



Figure 2.4 Cross-section view of SMD and NSMD pads [29]

### 2.3 Surface Mount Technology Assembly Process

Surface Mount Technology (SMT) refers to the attachment of packages on the copper pad coated with solder paste, and the solder interconnection is created through reflow soldering. The general SMT assembly process is shown below in Figure 2.5.

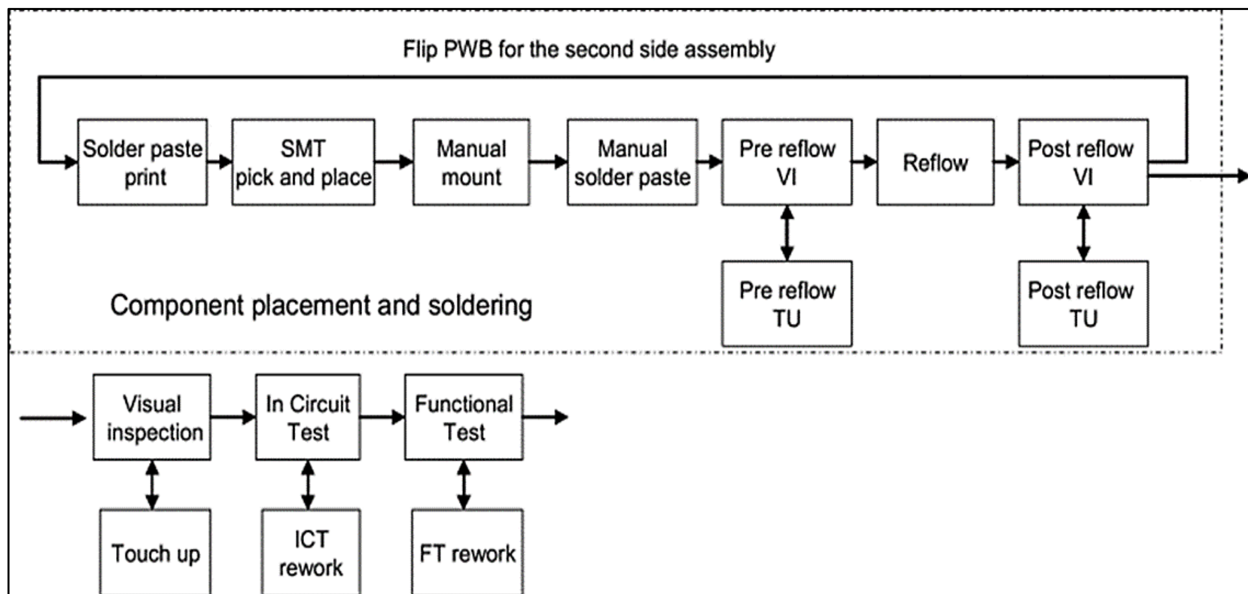



Figure 2.5 SMT assembly process [32]

Surface Mount Technology assembly consists of the following steps:

1. Solder paste printing: The first stage in SMT assembly is solder paste printing. The copper pads on the PCB are first applied with solder paste using a stencil. A stencil is made of a thin stainless steel metal sheet with holes or apertures corresponding to the component design of a PCB. Stencil printing is used to deposit the solder paste on copper pads correctly. To achieve electrical and mechanical performance, the solder paste between the package terminals and the PCB should be

at an acceptable level. Squeegee blade printing is the common stencil printing technique, as seen below in Figure 2.6.

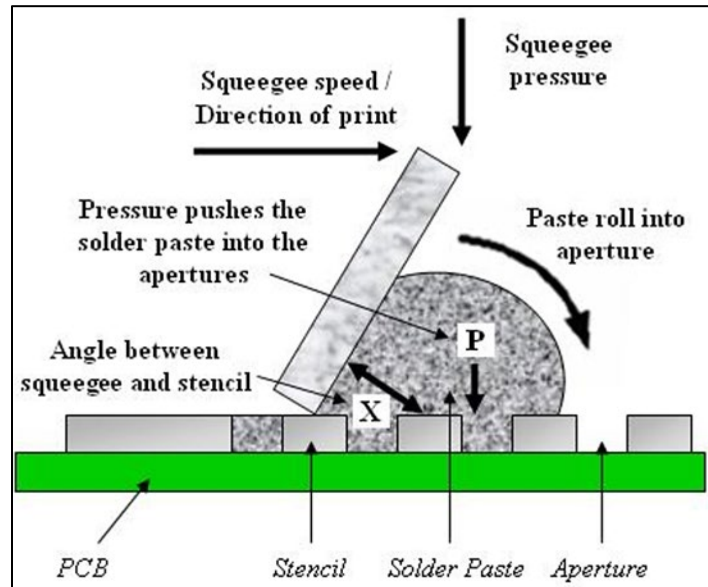



Figure 2.6 Cross-section representation of squeegee blade printing [33]

A squeegee blade is a tool used to print solder paste across the PCB. Back-and-forth printing is done. Squeegee blades are often made of polyurethane or metal. Squeegee speed, squeegee pressure, stencil cleaning, stencil separation speed, PCB support, printing stroke, inspection, storage, and handling are crucial elements for a successful printing process.

The quality of the paste printing is inspected after printing. The paste area is inspected using 2-D inspection, and its volume is inspected using 3-D inspection. Figure 2.7 depicts the various types of prints that could appear.

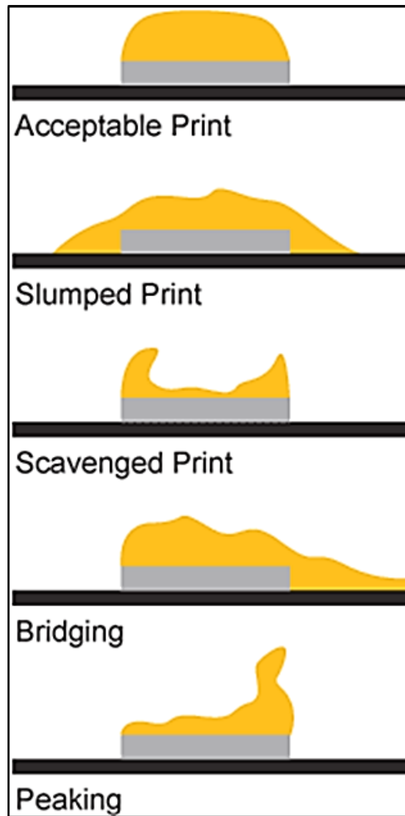



Figure 2.7 Different types of solder paste print [34]

The squeegee can produce slumped print, scavenged print, bridging, or peaking if any of the above-mentioned crucial factors are neglected.

Once the print quality has been verified, a pick-and-place machine installs the components on the PCB. According to the PCB's design land pattern, the components are arranged so that the solder termination of the package sits on the solder paste. The fiducial visual markings on the board make it easier to place the components. Global and local fiducials are the two types of fiducials. Local fiducial is utilized for precisely positioning fine pitch components, whereas global fiducial assists in setting the coordinate system for PCB. Any of the three corners can be used as the global fiducial. The package's corner or center are both acceptable locations for local fiducial. There are

several types of component placement machines depending on the board size, placement speed, accuracy, component kinds and their feeders, optical alignment, and efficacy of the inspection [4]. Typical global and local feducials on a PCB are illustrated in Figure 2.8.

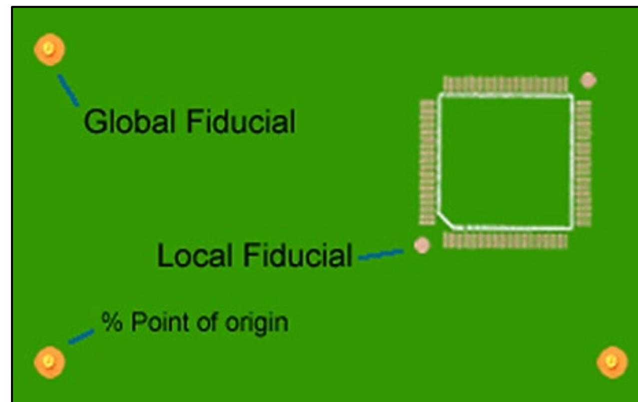



Figure 2.8 Types of fiducials [35]

3. Reflow Soldering: Following the installation of the components on the PCB, the PCB is put into a reflow oven where a strong metallurgical bond is made between the package termination and the copper pad. There are two types of reflow ovens: infrared and convection. The convection oven has various zones, each adjusted at a different temperature, as schematically depicted in Figure 2.9. Before creating a joint, the PCB is moved on a conveyor belt and subjected to a time-temperature profile.

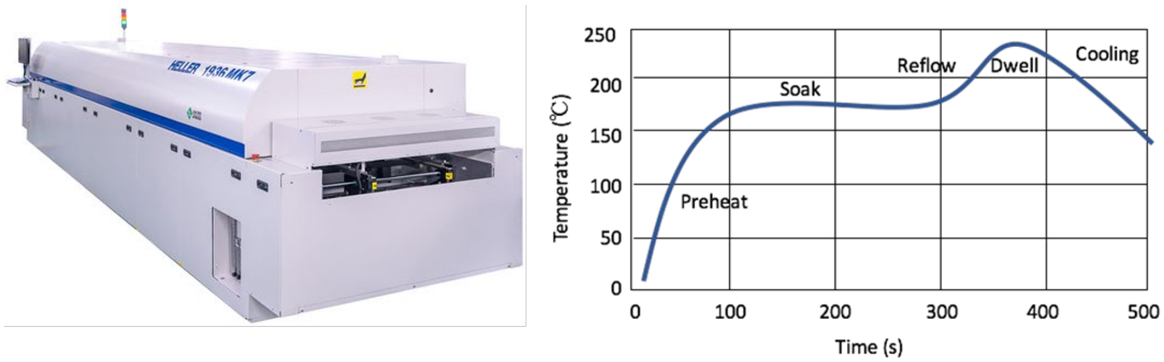



Figure 2.9 Typical reflow oven (Left) Reflow zones (Right) [36]

A typical reflow profile is composed of four zones, they are:

a. Preheat zone: At first, PCB is heated at a pace of no more than 3°C/sec to the desired temperature. The solvent in the solder paste is outgassed in this stage. The components may crack if the temperature rises too quickly.
b. Soak zone: The solder paste volatile is eliminated, and the flux is activated following the preheating cycle. This zone lasts for 60 to 120 seconds. Before reflowing, the thermal equilibrium of the entire PCB is attained when this zone is finished.
c. Reflow zone: The temperature in the oven is above the point at which solder paste will melt and become liquid, and this zone is also referred to as time above liquidus (TAL). For proper wetting, the TAL is set between 30 and 60 seconds. The greater reflow temperature must be closely watched because it can harm components.
d. Cooling zone: After the reflow zone, this area solidifies solder joints. The maximum cooling rate permitted is 4°C/second.
e. Inspection: An X-ray examination or Automated Optical Inspection (AOI) is carried out after the reflow soldering procedure to ensure no flaws in the solder joints. The AOI scans

for the presence of components, polarity, solder, and solder shorts. To find solder voids and damaged interior components, use X-ray technology. Figure 2.10 shows an example of an X-ray image of a CABGA component.

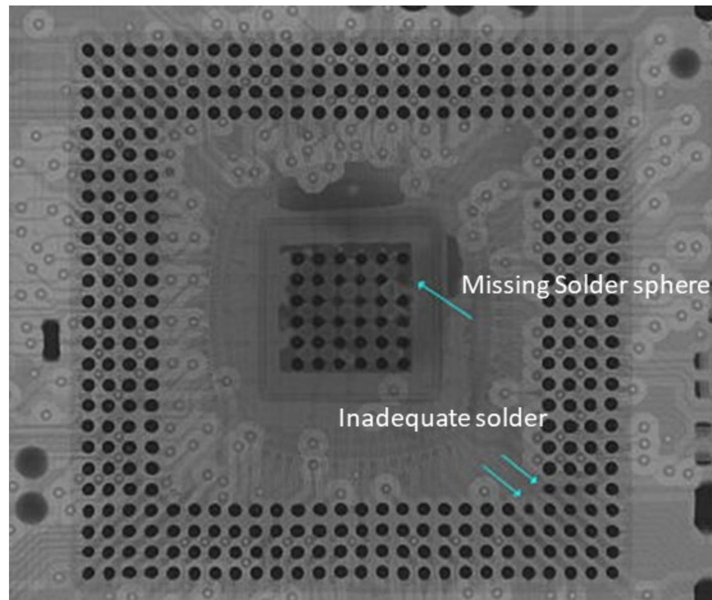



Figure 2.10 CABGA X-ray imaging [37]

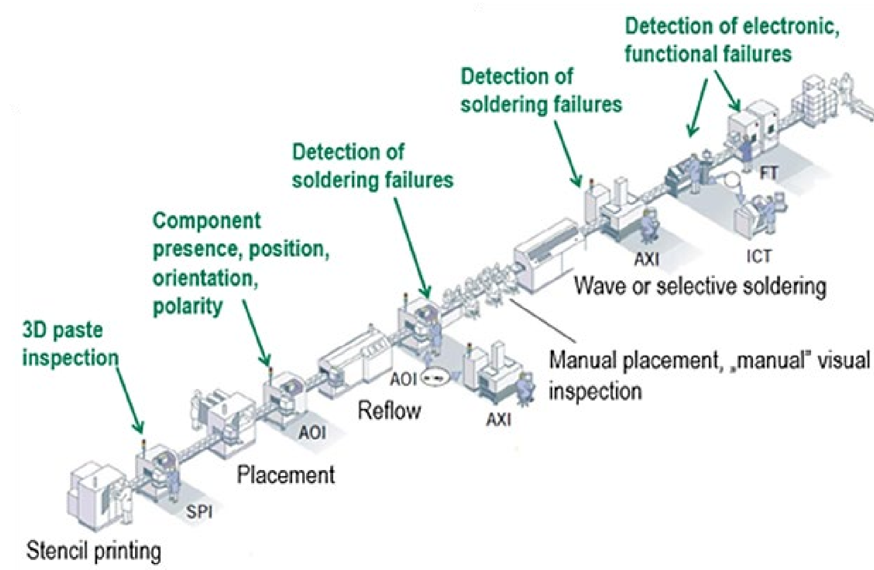



Figure 2.11 Overview of SMT assembly process [38]

Figure 2.11 depicts an overview of a typical SMT assembly. After assembly and inspection, mechanical or thermal tests are run to evaluate the reliability of the solder joint.

**2.3.1 Through-Hole Mount Technology (THMT)**

Through-Hole Mount Technology (THMT) is a conventional method in electronic assembly where components are mounted onto a printed circuit board (PCB) by inserting their leads into holes drilled through the board. This technology has been a mainstay in the electronics industry for several decades, although it has seen some decline with the rise of Surface Mount Technology (SMT). Despite this, THMT remains relevant for specific applications with paramount advantages. One notable advantage of THMT is its robust mechanical strength and reliability. Components mounted through holes tend to withstand mechanical stresses, making them suitable for environments with extreme conditions or applications subject to frequent handling. Additionally, THMT facilitates easier manual soldering and rework, as the leads are more accessible than densely packed SMT components. This accessibility makes THMT particularly advantageous in

prototyping and low-volume production. Moreover, Through-Hole Mount Technology supports the integration of various components, including resistors, capacitors, and connectors, offering versatility in design. The holes in the PCB allow for a secure and stable connection, making THMT well-suited for applications where durability and stability are critical factors. While Surface Mount Technology dominates many modern electronics applications, Through-Hole Mount Technology plays a vital role in specific niches, ensuring a balance between tradition and innovation in electronic assembly processes. Figure 2.12 shows examples of THMT components [4], [39].

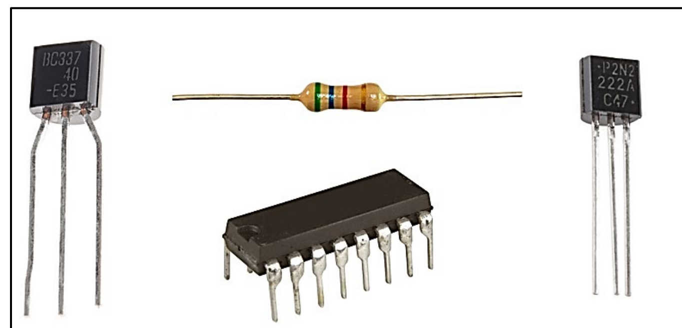



Figure 2.12 THMT component (examples) [40]

### 2.3.2 Surface Mount Technology (SMT)

Surface Mount Technology (SMT) is a pivotal electronic assembly technique that has transformed the landscape of printed circuit board (PCB) manufacturing. Unlike traditional Through-Hole Mount Technology (THMT), SMT involves placing electronic components directly onto the surface of the PCB, eliminating the need for leads or holes. This method has become the industry standard due to its numerous advantages. One key advantage of SMT is its space efficiency. With smaller and more compact components, electronic devices can be designed with reduced size and increased functionality. This miniaturization is crucial in developing portable devices like smartphones, tablets, and wearables. SMT's ability to place components closer together on both

sides of the PCB contributes to modern electronics' overall compactness and sleek design. Automation is another significant benefit of SMT. The process allows for high-speed and precise assembly through automated pick-and-place machines. This not only improves efficiency but also enhances the accuracy and reliability of the manufacturing process. As a result, SMT has played a crucial role in meeting the demands of mass production in the electronics industry.

Moreover, SMT enables the use of advanced and miniaturized components, such as Ball Grid Arrays (BGAs) and Quad Flat Packages (QFPs), further enhancing the performance and functionality of electronic devices. The versatility of SMT has propelled its widespread adoption, making it the preferred choice for a diverse range of applications, from consumer electronics to industrial equipment. In essence, Surface Mount Technology stands as a cornerstone in modern electronics manufacturing, driving innovation and shaping the sleek and powerful devices that define the digital era.

Fine pitch packages solve the problem of less I/Os by utilizing more pins with less pitch distance. This requires precise and tightening processes but lowers the package yield due to fragile leads during handling. Besides the challenges of handling and rework, the high cost of these packages is another concern. As a result, BGAs showed promising characteristics to solve the problems mentioned above related to fine pitch components. BGAs provide high density with significant yield improvement. Also, they have short leads, which implies fewer parasitic losses and signal propagation delay. BGAs could be either ceramic or plastic-type. The most remarkable characteristic of BGAs is their self-alignment during reflow, even when misplaced by up to 50%. BGAs arrays might be perimeter or full array, with ball pitches of 40, 50, and 60 mils and pin count varying from 16-2400. Unlike plastic ones, Ceramic BGAs (CBGAs) are hermetic and tightly sealed, which results in zero water or vapor absorption. The result is eliminating the

popcorn effect that occurred due to moisture absorption. Their standoff is measured by ball diameter, which is commonly 35 mils and is proven adequate for rework. The drawbacks of CBGAs are the high thermal mass and CTE mismatch with glass-epoxy substrates. The former issue causes difficulties in the reflow profile and threatens reliability. This problem could be solved by utilizing a ceramic substrate but increasing the cost significantly. Another version of CBGAs is the ceramic column grid array (CCGA), where columns replace spheres with a diameter of 20 mils and height ranging between 0.05-0.087 inches. The extra height improves reliability because more stress could be taken up due to a mismatch in CTE [30], [39].

On the other hand, taller joints reduce the electrical performance and add more cost to the package profile, with more susceptible to handling damage. Plastic BGAs (PBGAs) are widespread in the industry due to their lower cost. Its internal connection might be either a wire bond or flip-chip interconnection. Heat slug could be utilized within the package to enhance thermal performance. Resins form part of the mold, which enhances the stability performance of these packages by reducing the mismatch with PCB. Generally, PBAGs are low in cost but could be increased if fine pitches are utilized.

Other BGAs include tape BGAs (TBGAs) and chip-scale packages (CSPs). The latter is a modified version of BGAs, but the significant difference is the higher ratio of dying to overall package dimensions. The percentages of the bare area around the silicon die are no more than 20%. CSPs have two main concerns: larger package sizes and lower electrical performance than BGAs. Figure 2.13 provides an example of components from the BGA family.

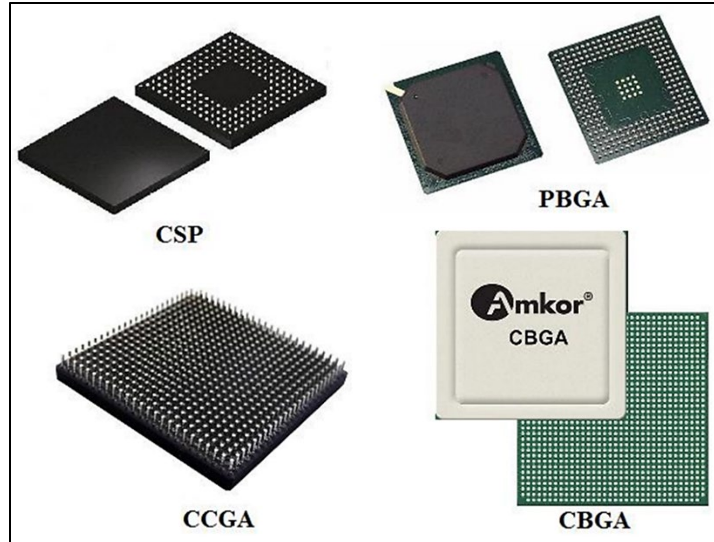



Figure 2.13 BGA component (examples) [41]

# Chapter 3 Literature Review

## 3.1 Drop and Shock Testing

The use of products by customers in various environments can expose them to hazards that may result in damage. For instance, a package may be mishandled and dropped in a warehouse, or a smart device like a phone or tablet may be dropped from a height during use (Figure 3.1). To mitigate the risk of damage, it is crucial for products to possess adequate mechanical shock durability. Shock and drop testing is performed to assess the shock resistance of products and guarantee their high quality.

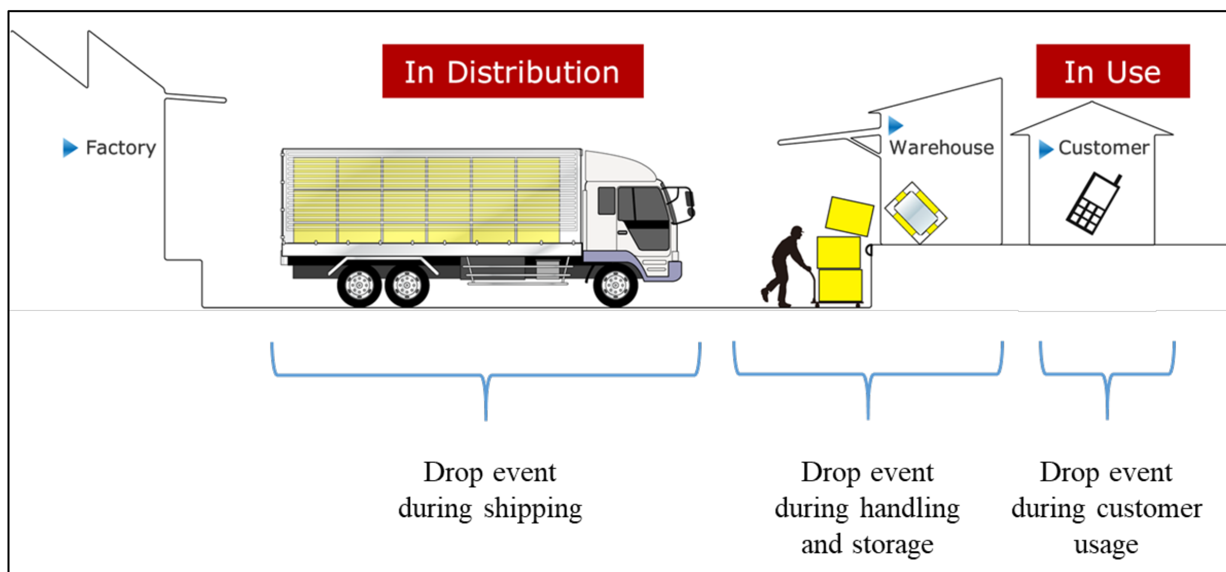



Figure 3.1 Mechanical drop event use conditions [42]

In the electronics industry, there has been an increase in the demand for portable gadgets. As a result, the electronic sector is continuously working to introduce new, smaller products with advanced features. Accidental drops could cause the hardware in these gadgets to be damaged. Accidental drops to handheld electronic devices can harm internal components. Interfacial or bulk

cracks could cause the failure to propagate to the solder connection. Due to cumulative damage and fatigue, repeated exposure to the drop shock causes the electronic assembly to fail completely. To assess the reliability of the solder joints, board-level tests are usually conducted on a drop testing machine based on the JEDEC Standards [43]. The PCBs are mounted onto the drop table in the horizontal position with four or six screws. The drop table falls along two guide rods onto the rigid base, inducing out-of-plane displacement in the PCBs upon impact. The impact surface can be altered by changing the felt material to vary the profile of the impact force. Upon impact, the PCBs vibrate at their natural frequency. Test instruments include accelerometers on the drop tower, strain gages on the PCBs, and a data acquisition system. The number of drops before failure is the metric used to describe reliability. According to Wong et al. [44], the time it takes for the stress waves to bounce off the free end and return as tensile waves determines the length of the shock pulse during the drop test. A portion of the compressive wave goes into standoffs and undergoes flexural wave transformation from the longitudinal waves in the PCB. The clamped ends of the PCB experience the highest acceleration since they are physically attached to the drop fixture. The peak acceleration occurs at the impact instant, and other acceleration spikes occur after a certain time basis how much time it takes for the flexural wave to reach the center of the PCB.

The JEDEC drop test is a widely used drop test for handheld electronics. It is a common component-level test for determining how reliable PCB assemblies are at the board level [43]. A PCB assembly with first-level packages undergoing the JEDEC drop test is subjected to a 1500G, 0.5-millisecond half-sine shock pulse. The JEDEC test's specifications are described in total [43]. The size of the board, height of the stand-offs, number of components on the board, and the loadings are all tailored for the JEDEC drop test. According to researchers, this customization may

not accurately depict real-world scenarios of damage from impacts. Although JEDEC has shortcomings, researchers nonetheless often use it to evaluate component-level testing of electronics subjected to drop and shock. According to the results of the vertical drop and horizontal drop experiments, vertical drop results in less flexing of the solder joints in the PCB than horizontal drop. As a benchmark test, researchers have employed the JEDEC drop, which has a 0-degree or horizontal drop, as depicted in Figure 3.2.

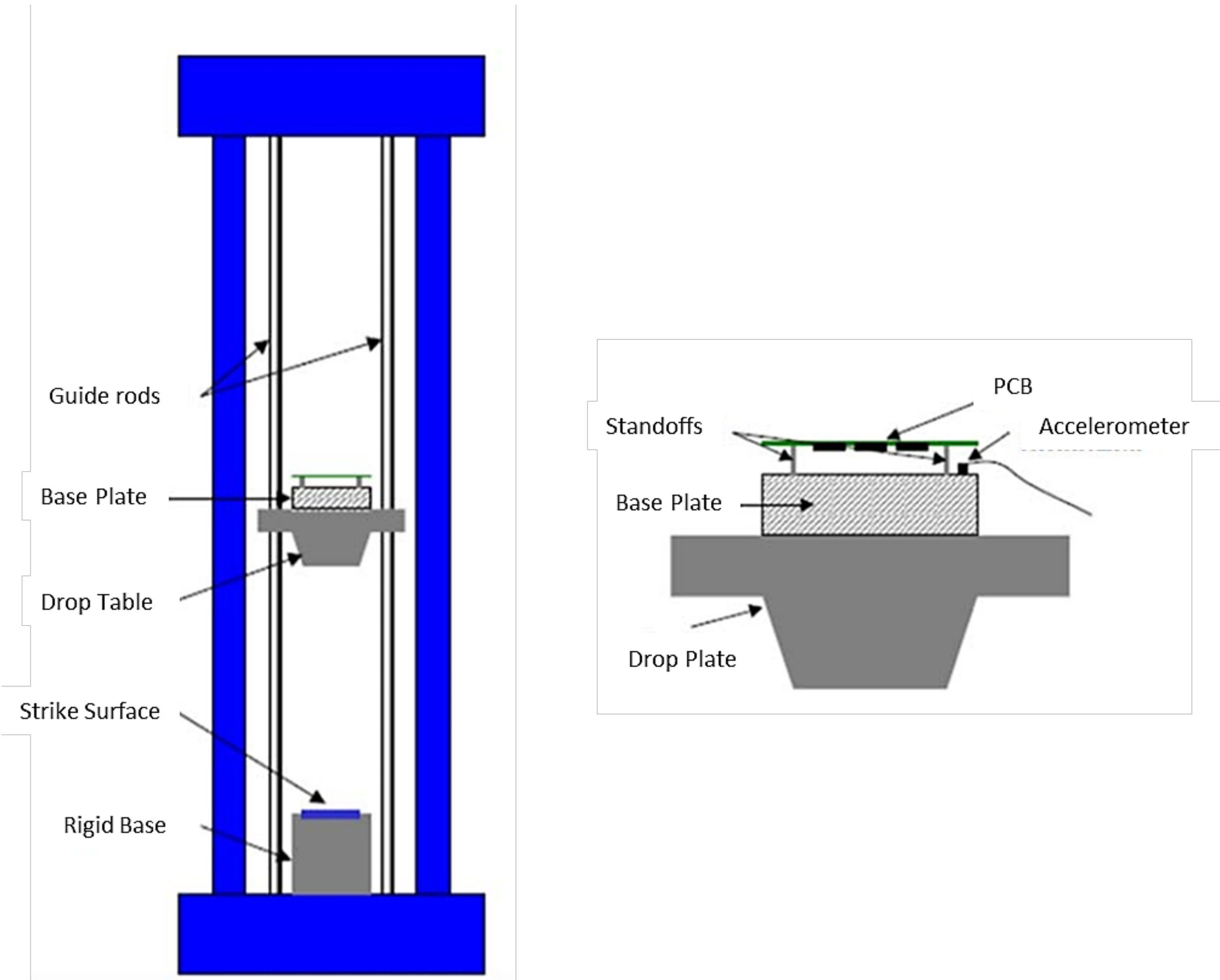



Figure 3.2 Typical drop test apparatus (left), assembly set up with board (right) [43]

Lim et al. [45] conducted product-level and board-level drop testing on a mobile phone and its PCB. Using a drop tower, the test vehicle was held in various orientations and allowed to drop to the ground from various heights. The results showed that the PCB would deform if the product were dropped due to a severe rebound impact. Accelerations, stresses, and impact forces were studied when different mobile phones and personal digital assistants were dropped from a height of one meter in various orientations. The highest PCB accelerations and stresses were measured during a horizontal product level drop. To regulate drop orientation and achieve higheliability, Wu et al. [46] performed product-level drop tests on a customized drop tester with a drop control mechanism**.** Area array LGA packages were dropped free-fall at the board and product levels by Xie et al. [47], who then measured the accelerations at the board and package sides. BGA and CSP packages were tested using controlled drops from various heights in the vertical direction by Lall et al. [48], [49].

Agarwal et al. [41] conducted board-level drop tests at different acceleration levels, pulse widths, and board orientations. The PCBs tested had 5 CABGA 100 components attached with SAC305 solder spheres. Upon examination of the failure data, a few clear trends were noticeable. The typical life reduces as peak input acceleration rises. The characteristic life reduces as the shock pulse duration increases, and the characteristic life improves as the drop orientation angle increases. The energy relationship developed in this study was used to explain these patterns more broadly. The fatigue life is reduced with an increase in the input energy. The area under the input acceleration curve was used to determine the input energy. Farris et al. conducted board level drop test for chip scale packages assembled with SAC305 solder alloy. The test vehicle consisted of 15 packages. It was found that, in general, packages towards the center of the board fail faster as a result of higher strains.

Drop test reliability for lead-free solders was examined by Amagai et al. [51]. The solder alloys used for the study were SnPb, SAC305, Sn-1.0Ag0.1 Cu-P-In, and Sn-1.0Ag-0.lCu-0.2In-0.04Ni. BGA packages were tested for both aged and non-aged conditions. The results are in the figure below (Figure 3.3).

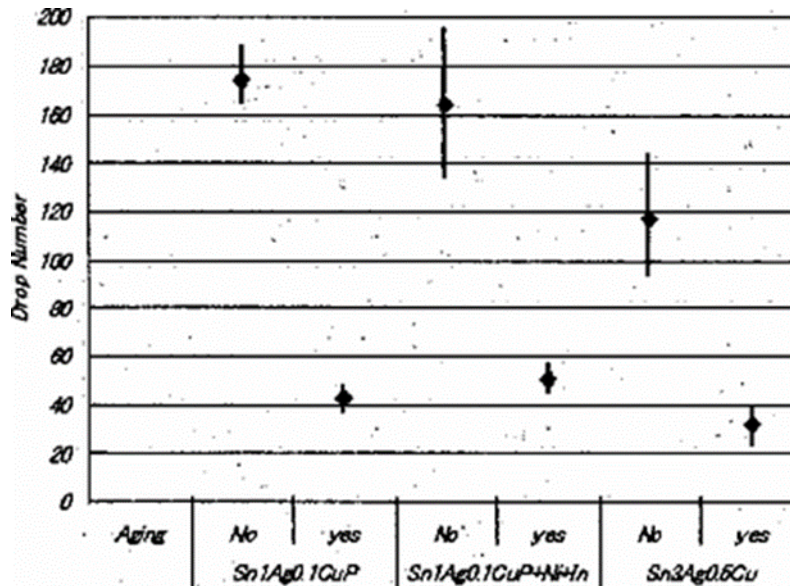



Figure 3.3 Drop test performance [51]

Doped SAC solder alloys were found to have better reliability than SAC305. It was also found that Indium and Nickel are responsible for improving drop test performance following the thermal aging process.

Lee et al. [52] performed a drop shock test to determine the solder joint reliability at various board thicknesses. In the study, SAC 305 solder joints with SMD and NSMD pad designs were tested for PCBs with thicknesses of 31 mil, 62 mil, and 93 mil. The drop reliability of solder joints was found to reduce with increased board thickness. It was also observed that boards with NSMD pad

design largely failed due to laminate crack or IMC crack, while boards and boards with SMD pad design predominantly failed due to IMC crack.

Iyer et al. [53] conducted drop test comparison between SAC305 and SAC105 solder alloys. The PCBs were subjected to 1500 G acceleration and 0.5ms pulse width. In the drop test, it was discovered that Pb-free solder SAC105 performed better than SAC305 by 45% for the mean time to failure and by 73% for the first failure. Due to its stiffness in comparison to SAC305 or its higher elasticity modulus, SAC105 Pb-free solder performs better. A solder with a lesser modulus has lesser stiffness and, hence, is more capable of shock absorption. As a result, the SAC 105 Pb-free solder has a longer life than SAC305 because it accumulates less strain energy after each drop cycle. Additionally, SAC 105 solder's reduced silver concentration aids in the formation of less brittle intermetallics (Ag3Sn), which lowers stress risers in the bulk solder.

Vickers et al. [54] Conducted a drop test study at different G levels and studied the failure modes. The test vehicles were designed per the JEDEC specifications for drop test boards with eight-layer FR-4 boards and 15 chip scale packages (Figure 3.4). Each CSP consisted of 228 SAC305 solder joints with 0.5mm pitch. In addition, the boards were drop tested with acceleration and pulse width of 900G, 0.7ms; 1500G, 0.5ms; and 2900G, 0.3ms. A dye penetration test and cross-sectioning SEM analysis were performed post drop testing to identify the failure modes. After analyzing 60 CSPs, five failure modes were observed: (1) pad cratering, 2) solder joint crack near the board, 3) solder joint crack near the component, 4) input/output trace fracture, and 5) Daisy chain fracture. The results are summarized in the figure below (Figure 3.5).

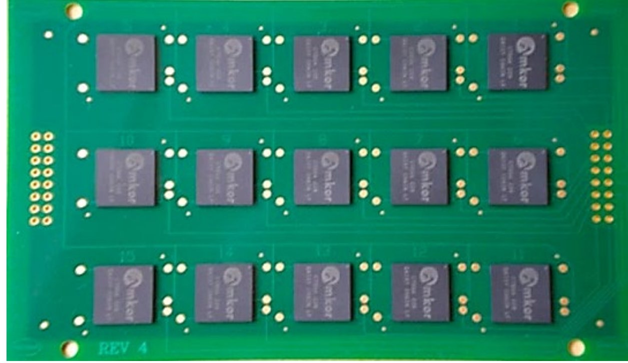


Figure 3.4 Typical test board in the literature [55]

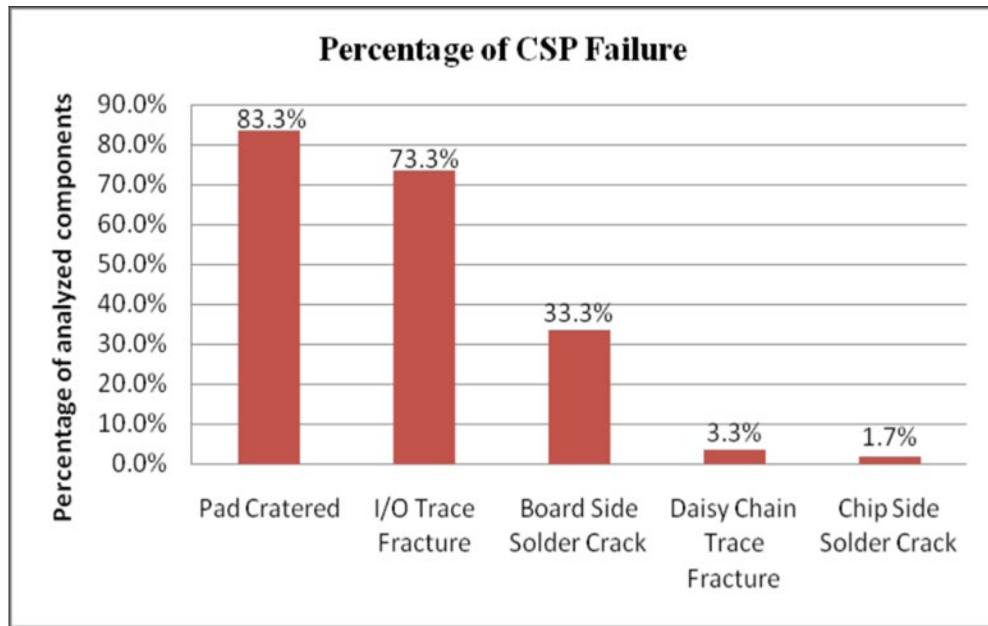



Figure 3.5 Failure modes analysis [55]

It was observed that pad cratering was the most dominant failure mode, followed by trace failure and board-side solder failure. Similar results were observed in another study by Roggerman et al. [56] and Farris et al. [57], where pad cratering and trace failures were the dominant failure modes. Ferris et al. also observed that components towards the center of the board are more prone to failure due to higher strains.

To determine the impact of various solder materials and peak reflow temperatures on the reliability and failure mode of the solder interconnects, Lee et al. [58] performed board-level drop testing. A Plastic Ball Grid Array (PBGA) component attached to a six-layer FR4 board with an ENIG surface finish was used as a test vehicle. It was discovered that eutectic Sn-Pb solder joints outperformed Pb-free solder joints in performance. Three failure points were identified: within the bulk solder, at the solder joint and copper pad interface, and fracture of the copper trace close to the pad-trace junction. Heaslip et al. [59], [60] compared the drop reliability of eutectic SnPb and Sn95.5Ag3.8Cu0.7 solders and proved that the failure mode and failure site change with drop height and solder type. Similarly, board-level drop tests have been used to examine the reliability of Pb-free solders with various compositions [61] and surface finishes [62].

Chai et al. [63] investigated the impact of board design, failure mechanisms, and component reliability. QFP and CSP components were tested as per the JEDEC standards. SAC405 and SnPb solder were tested, and the surface finishes used were OSP and ENIG. Components with OSP surface finishes demonstrated higher reliability when employed with SAC solder joints than those with ENIG surface finishes. Failure analysis revealed intermetallic failure between the $Ni_3Sn_4$ and Ni-P layers for all ENIG samples and copper trace failure for all OSP samples.

The widespread application of Electroless Nickel (phosphorus)/Immersion Gold (ENIG) as a surface finish for copper (Cu) pads in printed circuit boards and package substrates is a well-established practice. The role of Electroless Ni(P) as a diffusion barrier between solder and Cu pads contributes significantly to extending the lifetime of the joints, as it diminishes dissolution and reaction rates in comparison to untreated copper. This unique property positions ENIG as an optimal choice for minimizing Intermetallic Compounds (IMCs) accelerated growth during solid-state aging, especially when juxtaposed with solder joints on untreated copper.

Nevertheless, recent investigations bring to light a noteworthy finding: solder joints composed of as-reflowed Sn-Ag-Cu/ENIG demonstrate inferior drop impact reliability performance compared to their counterparts on copper pads treated with the organic solderability preservative (OSP) surface finish. OSP, an organic layer applied to Cu pads, serves as a protective barrier against oxidation during storage. Throughout the solder reflow process, the OSP layer on Cu pads tends to undergo evaporation, exposing the underlying Cu surface. Consequently, direct contact between Sn-Ag-Cu (SAC) solder and bare Cu occurs. The ensuing rapid reaction between SAC solder and Cu results in the formation of CuSn Intermetallic Compounds (IMCs) at the interface. Illustrative solder joint with IMC layer images are provided in Figures 3.6 and 3.7.

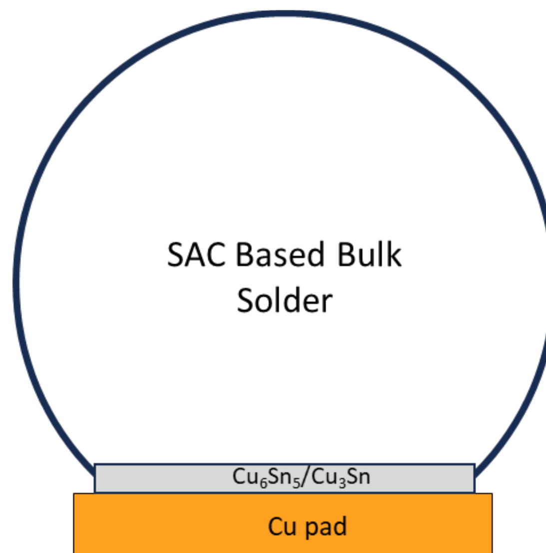



Figure 3.6 IMC of SAC based solder with OSP surface finish

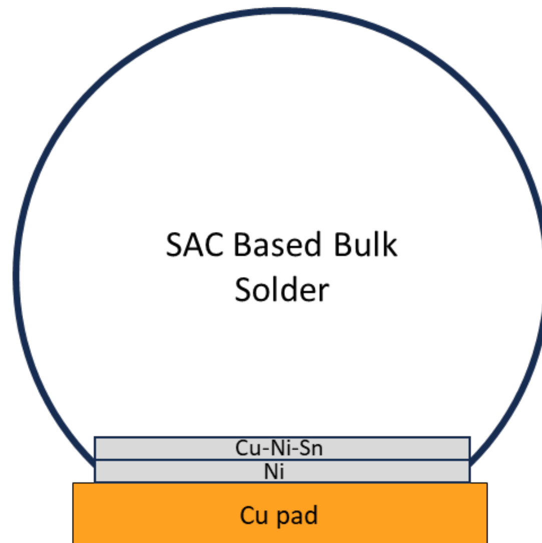



Figure 3.7 IMC of SAC-based solder with ENIG surface finish

Researchers have studied the effect of different pad finishes, including electroless nickel immersion gold (ENIG), solder on pad (SOP), hot air solder leveling (HASL), immersion silver, and immersion gold when subjected to high strain rate events like cyclic bend tests and mechanical shock [64]. Under ball pull tests, it has been demonstrated that flip-chip BGA substrates with SOP surface finishes outperform Electrolytic NiAu and ENIG.

A predictive fatigue model for SAC 1205N and SAC 105 based on a power law equation was developed by Mei-Ling Wu et al. [65]. The test vehicle was a rectangular board with 15 components. The test was conducted at 1500 G acceleration and 0.5 ms pulse width. The findings of the study indicate that a solder alloy containing a small amount of nickel can enhance the fatigue life performance for the drop test. The design of the copper traces, the copper via had an impact on the solder joint fatigue life. It was also noted that during the PCB assembly, one of the significant problems that could affect the reliability of the drop test during PCB assembly is the

warping of the package. As a result of the package's unequal warping, the test board's mounting can be uneven, ultimately decreasing the bonding between the copper pad and the solder junction.

Su et al. [66] analyzed the data from drop tests using a 2-parameter Weibull distribution with right and interval-censored approaches. As seen in Figure 3.4, the characteristic life from the tests from the Weibull analysis was obtained and shown as a function of solder paste. While Innolot displayed the lowest life, Ecolloy nearly shared SAC305's characteristic life (Figure 3.8). Overall, solder pastes with higher ductility performed better in mechanical shock testing, allowing the solder substance to absorb more energy through deformation when subjected to mechanical shock.

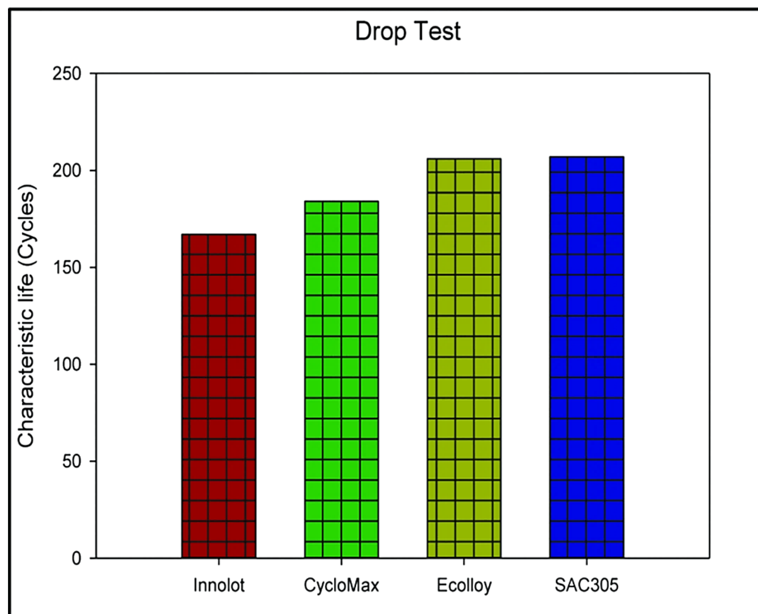



Figure 3.8 Characteristic life comparisons during drop test [66]

A study by Shin et al. [57] examined mechanical stress in multi-chip packages with a logic chipset package at the bottom—physical inspection allowed for observing numerous failure modes. One package had a corner solder sphere failure at the IMC layer on the board side. Spheres nearest to

the corner were found to have an IMC crack on the package side. On the package side of another package, an IMC crack was seen. In another work, Saha et al. [67] found that in thin (30-100 m) solder interconnects, the formation of a $Cu_6Sn_5$ intermetallic reaction layer led to an excellent metallurgical bond with the Cu pad at the component and board interface.

The stability of solder joints for flip-chip ball grid array (FCBGA) electronic packages subjected to mechanical shock was examined by Lee et al. [68]. From ambient temperature to 100°C, the test vehicle was examined under various isothermal conditions. It was determined that the capacity to withstand high mechanical strain is crucial in dynamic shock conditions. Furthermore, it was discovered that the pad design at the board interface has a vital role in shock performance in these circumstances. Unlike solder mask-defined (SMD) pads, non-solder mask-defined (NSMD) pads have a greater bonding area between the Cu pad and the solder spheres. Hence, Failures typically happen at the package side interface.

During normal operation, electronic circuits encounter a range of loads, encompassing thermomechanical loads due to temperature variations and mechanical loads from shocks and vibrations. These concurrent loads can significantly impact circuit reliability [3], [4]. Thermomechanical effects manifest from the expansion and contraction of materials due to temperature changes. Electronic circuits commonly comprise materials with differing coefficients of thermal expansion (CTE), leading to varying rates of expansion and contraction [5], [6]. This diversity induces stress in the solder interconnects that link circuit board components. Over time, this stress can cause fatigue and failure in these interconnects. Electronic circuits are exposed to thermal and mechanical loads in many applications. This combined exposure creates a synergistic effect, resulting in more severe damage than either load type would induce independently.

Mittila et al. [69] conducted drop tests at three different temperatures (RT, 70 °C, 110 °C), and the component was heated with integrated heater elements inside the component and printed wiring boards. Chip scale packaged (CPS) components were utilized with SnAgCu-bumped 12 mm x 12 mm BGA component having 168 (14 x 14 peripheral array). The boards were reflowed with Sn3.8Ag0.7Cu solder. A statistically significant decrease in drops to failure was recorded with increased testing temperature (Figure 3.9). Two different failure modes were identified cracking of the component side intermetallic compound (IMC) layers and cracking of the resin-coated copper (RCC) layer underneath the copper soldering pads.

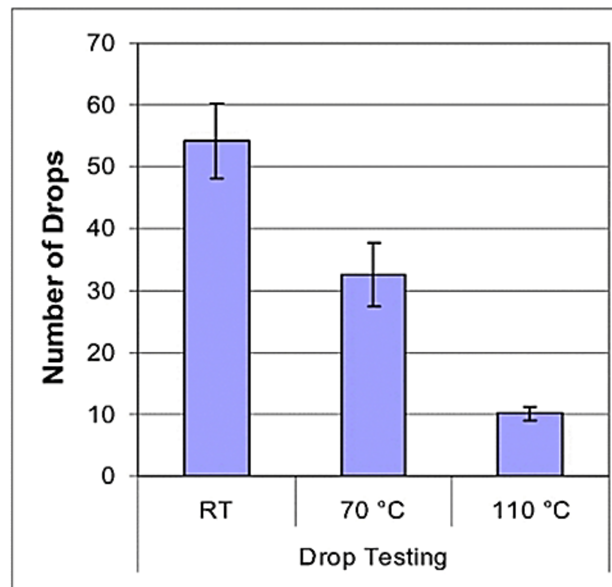



Figure 3.9 Drops to failure at elevated temperature [69]

In another work, Lee et al. [70] studied the effect of external temperature by testing flip-chip BGA components. Two pad designs, NSMD and SMD, were used, with SAC305 as the solder alloy. The boards were tested at room temperature and 100°C. From room to elevated temperature, there was a 75% life degradation in the boards with NSMD pads, and laminate crack was the dominant

failure mode. There was 50% degradation in the boards with the SMD pad, and the dominant failure mode was the IMC crack.

These studies illustrate the substantial influence of temperature on the drop test reliability of electronic components. This impact is attributed to temperature's impact on the mechanical characteristics of solder interconnects and the materials within the electronic circuit. Solder interconnects exhibit decreased stiffness and increased ductility at higher temperatures, rendering them more prone to failure upon impact. Furthermore, the thermal expansion and contraction in the electronic circuit generate stress, which can also contribute to failure.

### 3.2 Drop Shock Test – Physics of Failure

The drop test apparatus can be simplified as a structural system of multiple degrees of system (MDOF), for which components regarded as lumped masses are connected by springs and dashpots of different coefficients [71]. The simplified MDOF system of the drop test apparatus is shown in Figure 3.10. The impact force, F(t), is introduced from the impact of the drop table and the striking surface. This diagram explains the stress waves path as it travels from the drop plate to the package post-impact.

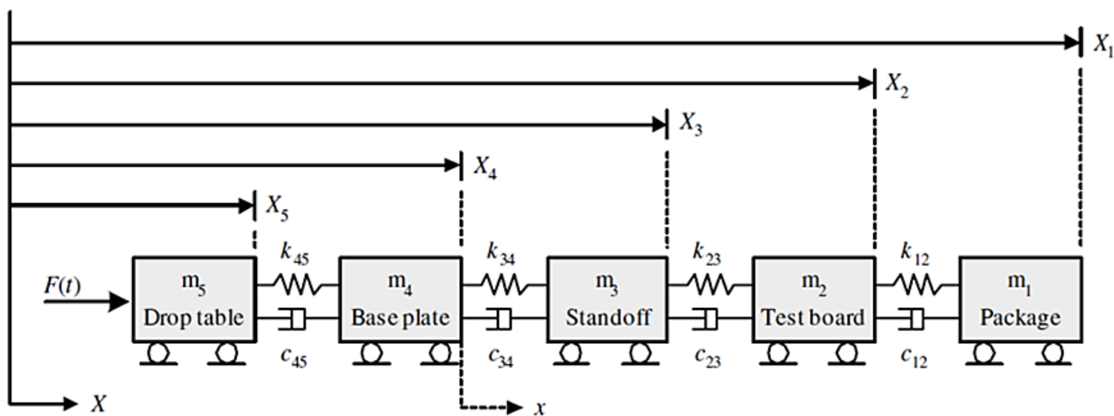



Figure 3.10 MDOF structural system for JEDEC drop test [71]

The stresses experienced by the electronics package and the solder joints during impact depend on various factors. These include external factors such as drop height and the impacting object; product factors such as the materials, stiffness, mass, exterior shape, and form of the product, as well as the packing clearance between components [l]; printed circuit board (PCB) factors such as the size and shape of PCB, the methods of attaching the PCB to the product, as well as the mass distribution of the components on the PCB; component factors such as the package construction, package size, the interconnection between the packages and the printer circuit board.

Literature has identified three board-level drop impact failure drivers, which are as follows [44]:

1) Elongation and bending of interconnection due to differential flexing of PCB and package: The interconnection at the outer most of the package experienced the highest stress in both upward and downward deflection (Figure 3.11). A similar mechanism has been responsible for vibration fatigue.

2) Inertia forces from electronic package: The individual interconnection will experience inertia force given by $F = m \times a$, where m is the equivalent mass distributed over the interconnection. It has also been found that the PCB adjacent to the supports could experience up to thousands of gravitational accelerations. Similarly, a package mounted on the PCB near the supports could experience the same acceleration.

3) Longitudinal stress waves during impact: Besides the high inertia stress, the interconnection adjacent to the support may also experience a high magnitude of longitudinal stress transmitted from the steel support.

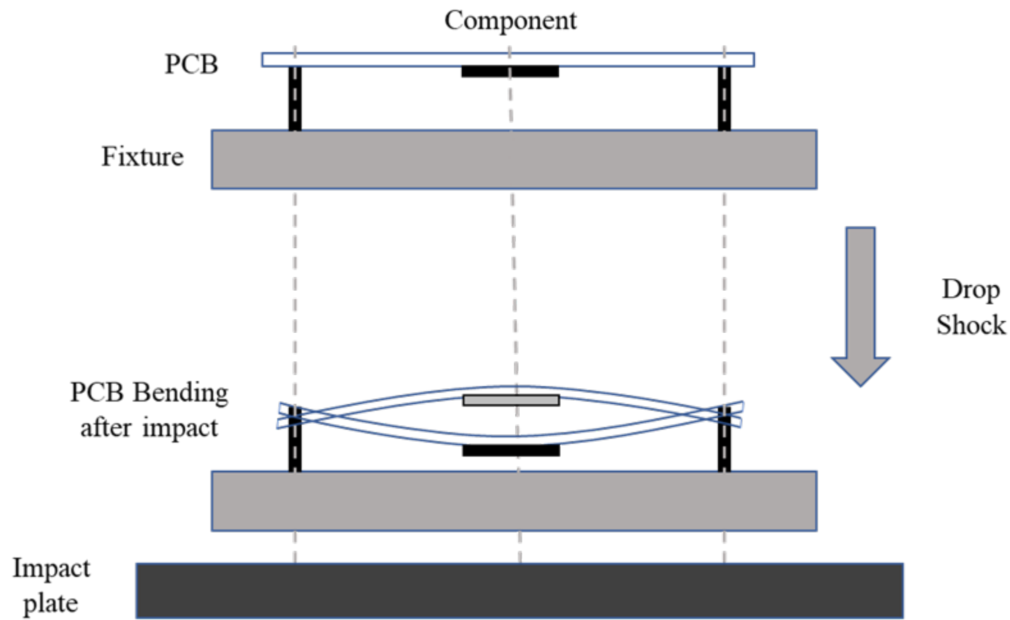



Figure 3.11 PCB bending upon drop impact

### 3.3 Effect of Aging on Solder Joints

After being manufactured, solder alloys undergo a variety of types of aging. During the assembly process, the solder alloys are exposed to elevated temperatures, which results in the aging of second-level solder joints [72]. Compared to solder joints, solder bars have different mechanical properties and aging effects. Lampe discovered the aging effects of solder joints at room temperature [73]. After 30 days of storage at room temperature, the shear strength and hardness can lose up to 20% of their original value. In 1956, Medvedev [74] found that bulk SnPb held at room temperature for 450 days lost 30% of its tensile strength, while solder joints stored at room temperature for 435 days lost 23% of its tensile strength. Lee et al. also noted that the shearing stress of solder joints dropped by up to 10% after 3 days of room temperature aging following reflow [75], [76]. At room temperature, Chuang et al. [77] investigated the impact of aging on the microstructure. Sn-9Zn and Sn-9Zn-0.5Al eutectic solder alloys were seen to coarsen overall

between 30 and 180 days of aging at 30°C, and the size of tin-rich precipitate increased. At room temperature, the ultimate strength, stiffness, strain, and yield stress significantly decreased by over 40% after 6 months of aging [78]. Lead-free Sn-0.7Cu, Sn-3.5Ag, Sn-3.8Ag-0.7Cu, and Sn-Pb solder alloys preconditioned for 51 days at room temperature showed a 5% to 8% drop in shear strength. Five popular lead-free solder alloys were tested by Sinan et al. [79] to determine how long-term room temperature aging affected the alloys' fatigue performance. The findings demonstrated that aging solder joints at room temperature for four years significantly impacted their fatigue life. Furthermore, under the same testing conditions, doped elements degraded less than SAC105 and SAC305 [72]. Investigations have been done into how aging at high temperatures affects mechanical properties. After 1500 hours of aging at 150°C, both Sn-Pb and Sn-3.5Ag solder compositions lose significant shear strength [80]. Kim et al. discovered a similar pattern, observing an average 5% drop in solder material strength after 300 hours of aging at 150 °C [81]. Increasing aging time results in decreased reliability, increased plastic strain, and increased inelastic work per cycle [82]. When solder joints were thermally cycled from 0 °C to 100 °C with a 10-minute dwell time and isothermally aged at 150 °C, another research found a 44% reduction in a lifetime [83]. However, it was also found that aging when cycling temperatures range between 20°C and 80°C improves the reliability of specific components**.**

### 3.3.1 Effect of Thermal Aging on Shock Performance

Thermal aging can alter the solder joints' mechanical properties, which could affect the drop performance of electronic devices. Miniature Charpy tests were conducted by Date et al. [84] on Cu-bonded solder sphereaged 150 °C for up to 1000 hours. As aging progressed, it was observed that the change from ductile to brittle, accompanied with fracture inside the solder into the interfacial IMC layer. After aging at 150 °C for 0, 50, 250, 500, and 1000 hrs., Ahat [85] reported

on a study of the interface microstructure and shear strength of 96.5Sn3.5Ag and 62Sn36Pb2Ag on Cu. After 1000 hours of age, fracture mode changed from a mixture of solder and IMC at zero aging time to a complete fracture of the IMC layer. Furthermore, the shear strength of both the Sn-Ag and Sn-Pb-Ag was reduced.

Mattila et al. [86] examined the performance of three SAC solder joint compositions (Sn-3.1Ag-0.52Cu, Sn-3.0Ag-0.52Cu-0.24Bi, and Sn-1.1Ag-0.52Cu-0.1Ni) under mechanical shock loading and cyclic thermal loading conditions. The boards with the low-silver nickel composition (Sn-Ag-Cu-Ni) had the highest average number of drops-to-failure, whereas the alloys with bismuth (Sn-Ag-Cu-Bi) had the lowest average number. On the other hand, the thermal cycling tests revealed that boards with Sn-Ag-Cu-Bi performed best while those with Sn-Ag-Cu-Ni interconnections fared worst. In both assessments, Sn-Ag-Cu was positioned in the middle. This study shows that a better test result under one load may not necessarily apply to a different load.

### 3.4 Effect of Vibration on Solder Joints

Liu [87] and Wong [88] conducted experiments for high cycle fatigue vibration of BGA packages. Their experimental setup offers controls for adjusting the applied load's magnitude and cycling frequency. The solder interconnects failure in BGA specimens was documented using a direct visual monitoring method. The BGA solder sphere and the ENIG plating on the copper pads of the PBGA substrate were found to initiate and propagate cracks along the nickel/solder interface in every test scenario, which led to BGA connection failure. According to Zhang [89], [90], SnPb solder has a steeper slope on its fatigue curve than Pb-free SAC, which was acquired during lap-shear testing. As a result, it was discovered that SAC was more robust at high load levels, whereas SnPb was more robust at low load levels (high-cycle-fatigue), with a cross-over at intermediary stress levels. Several studies on the vibration reliability of PBGA were undertaken by Yang et al.

[91], [92], [93], including modal analysis of the board and vibration reliability characterization under out-of-plane excitation. The dynamic behavior of an electronic package and the reliability of BGA solder joints were simulated by Yu [94] and Shah [95]. Intermetallic compounds' impact on vibration fatigue of µBGA solder joints was studied by Tu [96]. Kim et al. [81] proposed a novel technique to assess BGA packages' vibration-induced high-cycle fatigue strength using Pb-free and Pb solder, securing a weight and applying mixed-mode stress to the joints and the package. The test frequency of 15–25 Hz was unaffected by the solder joint fatigue strength employed in the experiment. Lall et. al. [1]examined the effect of elevated temperature on vibration fatigue life. The test vehicle consisted of components such as BGA, QFP, SOP and TSOP with SAC305 solder alloy. The test matrix included three temperatures 25°C, 85°C, and 125°C and two acceleration levels 10G and 14G. It was observed that the board deformation increases with an increase in temperature and the reliability of all test components reduced with an increase in temperature under combined temperature-vibration loading (Figure 3.12).

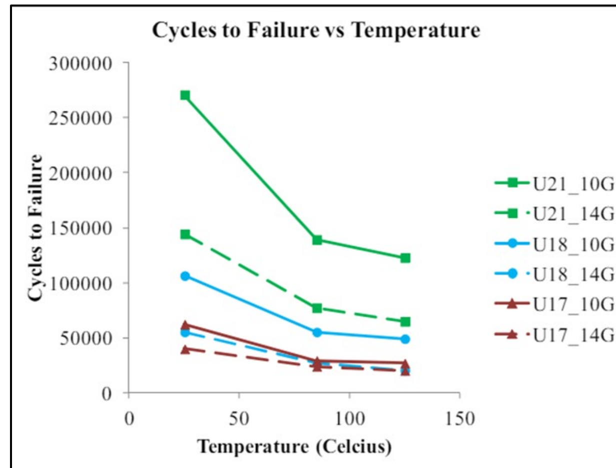



Figure 3.12 Cycles to failure under combined temperature-vibration loading [96]

### 3.5 Effect of Solder Doping on Reliability

Many lead-free solder alloys are being created to improve drop resistance. Manufacturers are looking for an alternate lead-free solder alloy since SAC305 has much less drop resistance than SnPb solder alloy. Despite SAC105 being the most demanded substitute, makers of solder are searching for the third-generation lead-free solder alloy, which frequently involves considerable additions of the element, also known as dopants [97]. Bismuth (Bi), antimony (Sb), and indium (In) are among these elements [85]. These additives create finer grain boundaries and reduce the intermetallic formations of the tin with silver or copper, resulting in a more reproducible grain and a more uniform grain formation in the lead-free alloy. This process is called solder doping, solder micro-alloy, or solder addition [85]. In the lead-free alloy, these additions produce finer grain boundaries and lessen the intermetallic formations of the tin with silver or copper. This leads to a more reproducible grain and a more consistent grain formation. As a result, developing the optimal SAC-based lead-free solder alloys to suit all specifications is of great importance to the industry.

Numerous publications have explored the impact of Ni doping [97], including a comprehensive review by Tegehall [48]. According to reports, Ni doping can prevent Kirkendall voids from forming, slow the growth of interfacial IMC layers, and prevent the allotropic transition of $Cu_6Sn_5$ [98]. However, it has also been shown that adding Ni would cause the SAC solder material to soften and result in brittle Cu-Ni-Sn ternary IMCs [97]. To achieve the best drop and tarnish resistance, Pandher et al. suggested 0.05% Ni doping SAC0307 + 0.1% Bi [45].

Zn-modified SAC alloys combine high tensile strength and high ductility [85]. The increase of microstructure stability and aging resistance provided by Zn doping is its most significant effect [99]. Zn doping's impact on the SAC solder's microstructure properties was researched by Song et al. [76]. They discovered that adding 0.5% Zn dramatically decreased the undercooling in the Sn-

3.3Ag-0.5Cu solder, preventing the growth of big Ag3Sn platelets. Additionally, it was shown that Zn-doped SAC solders had a higher volume fraction of eutectic phases without forming Zn-bearing IMCs. According to Anderson et al. [99], even after 1000 hours of aging at 150°C, no apparent microstructure change was seen in bulk Sn-3.5Ag-0.74Cu-0.21Zn solder joints. Kang et al. [100] also completed work along similar lines. They concluded that SAC387 was very effective at inhibiting the growth of the IMC on Cu pads, even with a small amount of Zn (1%).

Solder alloys with a higher Bi content have shown better ultimate shear strength than the SAC305 alloy [101]. A study also found that Sn-3 Ag-0.5 Cu-3 Bi and Sn-3 Ag- 0.5 Cu-1 Bi have better resistance to crack growth, resulting from the alloy's strengthening effect of Bi constituent [102]. Bi of approximately 1% weight in SAC can slow down the growth rate of the IMC layer, reduce Cu consumption, and reduce the solder's melting temperature [103]. Furthermore, adding Bi and Ni has been found to enhance thermal fatigue life and drop shock reliability [104]. A study has also shown that Bi can decrease solder elongation and increase tensile strength [105].

Numerous researchers and groups have also researched other doping options for SAC solders, including Mn, Cr, Ge, Ti, Si, B, and Al. The performance of 14 different doped solder alloys was examined by Liu et al. [98], who concluded that SAC105 + 0.13Mn alloy performed better than all other alloys, including traditional Sn-Pb solder. According to Anderson et al. [107], adding just 0.05%, Al significantly increased SAC3595's aging resistance. Amagai et al. [108] discovered that while using In as a dopant could lessen Kirkendall voiding, it did not impact the development of Cu3Sn IMC. Ge is acknowledged to purify the Sn matrix and enhance corrosion behavior, unlike other "diffusion compensators" like Ni and Co [109].

### 3.6 Solder Joint Failure Modes

Eight possible failure scenarios are anticipated from a drop test, as per IPC-9703 Standards [110]. They are depicted in Figure 3.13. It should be noted that the locations of shock-induced failures are determined by a combination of the properties of the printed board (such as the board material, composite construction, board design, and board thickness), the properties of the solder, and the solder joint (such as the surface finish, solder alloy, lead material, and design, and the standoff height), and the properties of the component (such as component weight, size, and design). Cracking is likely to initiate at the point where the shock-induced stress is greater than its material strength. An initiated crack will continue to propagate as long as there is a sufficient energy release rate to overcome a material's fracture toughness. Interfacial voids are closely related to brittle solder joint fractures, according to the observations of Newman et al. [111]. Many packaging configurations were tested. They varied in solder composition (63Sn37Pb, 62Sn36Pb2Ag, and 96Sn3.5Ag0.5Cu), packaging construction and materials, solder and package geometries, package assembly location, and the time between reflow and test. They also varied in the type of substrate plating (exposed Cu, electrolytic NiAu, and electroless-Ni/immersion Au).

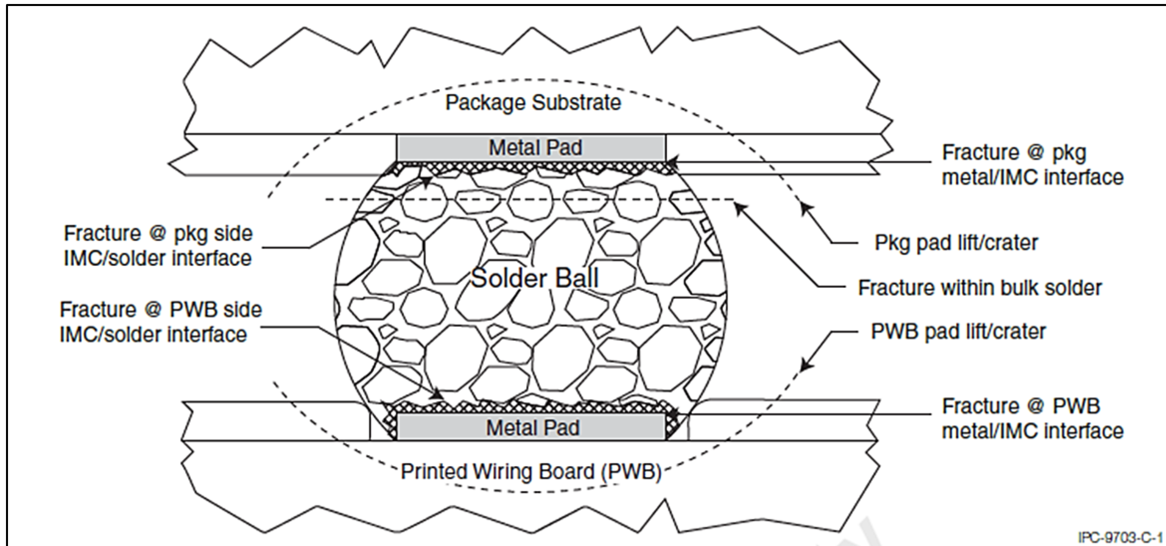



Figure 3.13 Solder joint failure modes [110]

Failures in copper pads could also take place. The separation of the copper pad from the epoxy resin of the board laminate can also occur under shock loading. Finer copper patterns, thinner copper foils, or high-frequency applications influence the strength of the copper and epoxy resin bond. To provide better resistance to cracking and delamination, the copper's adherence to the epoxy resin of the PCB must be improved. A copper trace failure from pad tear-out might result in the loss of the intended electrical connection. With a focus on copper trace failure, Kraemer et al. [112] and Tee et al. [113] provide helpful descriptions of failure modes. Pad cratering, which is the development of a crack or fracture in the PCB material beneath the copper pad, is another shock-induced failure. The crack may initiate from the intersection of the solder, copper pad, and laminate. This is a stress concentration location [114]. Delamination of the epoxy from the reinforcing glass bundles it has encapsulated may also result in pad cratering. Copper trace failure and electrical continuity loss might result from pad cratering.

Pad pullout and pad cratering can both result in copper trace failure. Additionally, mechanical

cycling and stress concentration at the pad-to-trace interface can cause fracture initiation and growth, leading to copper trace failure. Menon et al. [115], Lall [116], and Farley [117] investigated copper trace failure, estimated stress at the copper's pad to trace area, and put forth fatigue life models.

A basic understanding of failure mechanisms accompanied by analytical, experimental, numerical, and statistical techniques is necessary for product reliability over the design life. According to earlier research [97], [117], [118], [119], BGA package corner joints will experience the first signs of failure due to either a fracture at the BGA package/IMC interface or a fracture at the PCB metal/IMC interface. All studies demonstrated that Sn-Pb outperformed LF in terms of performance and reliability.

### 3.8 Reliability Prediction Models

#### 3.8.1 Input Energy Predictive Model

The input shock is caused by the drop block's abrupt deceleration and transmitted into the PCB by the four corner supports. The board bends due to the input acceleration acting as a forcing function. This can be approximated in the quasi-static situation by assuming the supports are stationary and delivering an evenly distributed force (acceleration) throughout the board's surface, as shown in Figure 3.14.

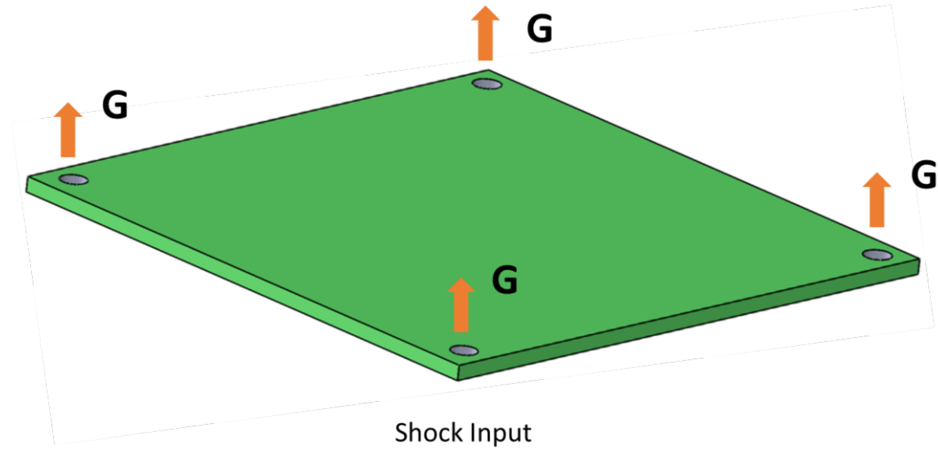



Figure 3.14 Loading on PCB during drop test

The summation of strain energy and kinetic energy gives the total board energy. We consider just kinetic energy [49]; this is defined as:

$$T = \frac{1}{2}\rho lwh \iint_A V^2 \, dxdy \qquad (3.1)$$

Where l is the board's length, w its breadth, h its thickness, and ρ is the density. A is the area of the board, and V is the velocity in the out-of-plane direction. The double integral function is necessary since the velocity depends on the location (x, y). As a result, each component location has a different energy term. We assume that the response energy, T, is proportional to the input in this study because all components are situated at the symmetric (x, y) coordinates, and the board was constant for each test cell.

The input energy is easily measured and is not a function of location on the PCB. The force input, f(t), is a function only of time. Since we know the acceleration input, the 'smeared' force is,

$$f(t) = m \times a(t) \qquad (3.2)$$

Where a(t) is the known acceleration input, and m is the mass of the board. According to Figure 3.6, this force is distributed uniformly across the board area. This input's energy is then,

$$E_{input} = \frac{1}{2} m \times V^2 \tag{3.3}$$

Where V, the change in velocity, is determined by integrating the input acceleration curve. The input curve is only integrated between the 10% levels to maintain compliance with the JEDEC requirement for pulse duration.

The characteristic life ($N_{63}$) and input energy can be plotted on a log-log plot. This gives a linear power law relationship between reliability and input energy on the log-log scale. The resulting equation is,

$$N_f(63.2\%) = C_1 \times E_{input}^{C_2} \tag{3.4}$$

where $E_{input}$ is the calculated input energy from (3), and C1 and C2 are constants [49].

### 3.8.2 Stress-based Criterion

The stress criterion of prediction is used when failure mode is peel-dominant, and the maximum peeling stress is the failure criterion for solder spheres under drop shock. Maximum peeling stress is the root cause of brittle failures in the solder joints, such as a crack in the IMC on the board or PCB side. Brittle failures depend on the hardness of the alloys and are the failure mode for very hard alloys. A fatigue life prediction model is formulated using power law to relate the mean impact life and maximum peeling stress.

$$N_{mean} = C_1 \times \sigma_Z^{C_2} \tag{3.5}$$

Here, $N_{mean}$ is the mean impact life, $\sigma_Z$ is the maximum peeling stress (MPa) in the critical solder sphere, $C_1, C_2$ are the constants [120].

### 3.9.3 Strain-based Criterion

Ductile failure modes are usually caused due to plastic strain. Usually, softer solders will undergo such failures compared to harder ones that undergo brittle failure. This failure mode will be observed in the PCB or component side bulk solder. Since plastic strain is the criterion for the bulk solder, we can use the Coffin-Manson relationship to predict the drop impact life. Coffin-Manson is one of the most used fatigue life prediction models. Here, the average number of drops to failure is related to accumulated plastic strain $\Delta\varepsilon$ in the following way:

$$N_{mean} = C \times \Delta\epsilon^{-\alpha} \tag{3.6}$$

Here, C and $\alpha$ are the constants. Drop tests must be carried out to determine the constants, along with the finite element simulation for all the tested boards. The tested impact life and the simulated plastic strain are curves fitted in the above equation (3.6) to determine the constants [120].

## 3.9 Hardness Test

Hardness testing is a mechanical technique for determining a material's resistance to plastic deformation [121]. The concept generally entails applying a load (from an indenter) to the sample's surface. The hardness values are then numerically evaluated by dividing the applied load by the projected surface area. In short, the following factors and test criteria are used to assess lead-free solder [121], [122]:

- Indenter is an element that pierces the surface of the solder alloy. The indenter's geometry makes it possible to determine the projected surface area.

- Load is the force exerted on the solder alloy's surface (N, g, or kgf). The anticipated area is mostly partitioned to produce the hardness value.
- Dwell time is the amount of time the indenter is held after reaching the relevant load to ensure enough indentation.

### 3.9.1 Vickers Hardness Test

The Vickers microhardness characterizes the rectangular pyramidal tip for the hardness measurement (Figure 3.15). The greatest stress applied and the resulting contact area of the indentation are used to determine the hardness [123]. Used in lead-free solder characterizations, the Vickers hardness test is particularly useful. Solder joints and bulk solder alloy can both be evaluated for hardness.

The following equation represents Vickers microhardness (HV),

$$HV = 1.854 \frac{F}{d^2} \tag{3.7}$$

Here, F is the force applied in kgf and d is the average length of the diagonal impression left by the indenter in mm.

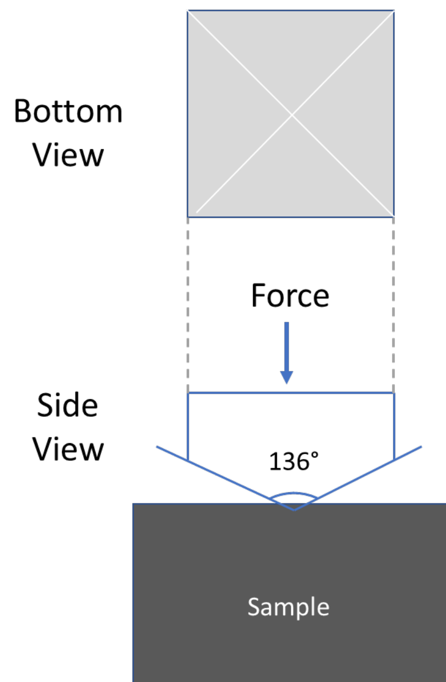



Figure 3.15 Schematic of indentation for Vickers microhardness

## 3.10 Gaps in the Literature

### 3.10.1 Test Board

A typical drop test board in literature is rectangular in shape and consists of multiple components. This results in uneven stresses experienced by the corner solder joints because of the board flexure during impact. Symmetry ensures that the board experiences the same shock loading in all directions, which makes it easier to compare results and draw conclusions about the performance of the solder alloys. Additionally, the majority of these boards in the literature have non-solder mask-defined (NSMD) pads, which results in failures occurring in the copper traces or laminate rather than the solder joint. Copper trace and laminate (pad cratering) failures during drop testing do not help determine the reliability of the solder joint. Such failures occur due to the solder alloys

being much stronger. To address these challenges, the board design has been modified, which will be discussed in the following section.

### 3.10.2 Experiment

There are very limited studies in the literature that involve drop shock testing of doped SAC-based alloys and comparing them with eutectic SnPb. Apart from this, it is necessary to study how the performance of solder joints for various acceleration levels. No prior research has been conducted to examine SAC-based solder alloys and to develop a physics of failure based predictive model for varying acceleration levels.

Most studies regarding drop shock reliability primarily focus on room temperature, with limited literature on elevated temperatures. This knowledge gap is critical since electronic devices are frequently employed in diverse environments, including those with elevated temperatures. Moreover, further investigation is required to systematically explore the combined impacts of thermal and mechanical loads on the drop shock performance of SAC-based solder joints within BGA assemblies. Additionally, no research is available on how different surface finishes affect drop reliability at elevated temperatures. These gaps in the literature will be addressed in this dissertation, as described in the following section.

# Chapter 4 Materials and Methods

## 4.1 Why BGA?

The need for compact devices is on the rise due to customers' desire for small but multifunctional devices. With a greater degree of functional integrity, the majority of the electronics OEM market is going toward miniaturization. The most recent smartphones, wireless devices, and mobile devices are the best instances of this. The tiny and ultra-fine pitch chip scale packages, micro BGA's, and other active devices are being adapted by designers of the next generation of thinner, faster, and sleeker portable gadgets, whether the industry is ready for it. The future packaging trends for handheld devices are 0.3mm or less ultra-fine pitch BGA’s.

## 4.2 Solder Alloys

In this research, five solder alloys are included. The BGA components were pre-balled with the solder sphere. The copper pads on the test vehicle were stencil printed with solder pastes, and then the component is placed over the PCB and reflowed. The solder paste constituted about 16% of the solder joint. The solder sphere and paste match was maintained in all the studies. The composition of the five solder alloys is tabulated in Table 4.1.

Table 4.1. Solder alloy composition

| Solder Alloy | Pb | Ag | Cu | Bi | Sb | Ni | In | Melting Temp. |
|---|---|---|---|---|---|---|---|---|
| SnPb | 37 | - | - | - | - | - | - | 179 |
| SAC305 | - | 3 | 0.5 | - | - | - | - | 217 |
| Innolot | - | 3.8 | 0.7 | 3 | 1.5 | 0.13 | - | 205 |
| Cyclomax | - | 3.4 | 0.5 | 3.3 | - | - | | 205 |
| Sabix | - | 3.5 | 0.8 | 0.5 | - | - | 6 | 205 |

**4.3 Test Vehicle**

The test vehicle's substrate material of preference was FR-406. The grade FR-4 is assigned to substrates with glass-reinforced epoxy laminates; it is composed of woven fiberglass cloth with a flame-retardant or self-extinguishing epoxy resin binder. The material is proven to maintain its mechanical and electrical insulating properties in both dry and humid settings. It has a glass transition temperature of around 170°C. The test board's dimensions are 2.952 x 2.952 inches (76 x 76 mm), and its thickness is 0.062 ± 0.007 inches, measured from laminate to laminate. The board's dimensions and the tooling holes are shown in Figure 4.1. The copper is distributed in four circuit layers to give a typical CTE for the thermal cycling test. A half ounce of copper is included on each layer.

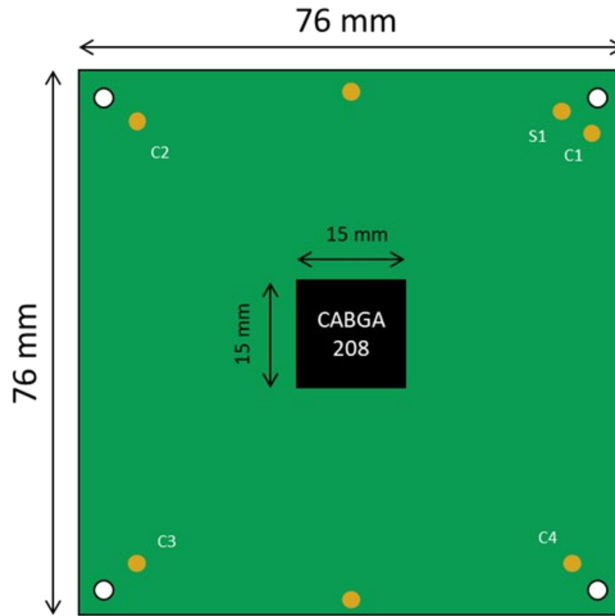
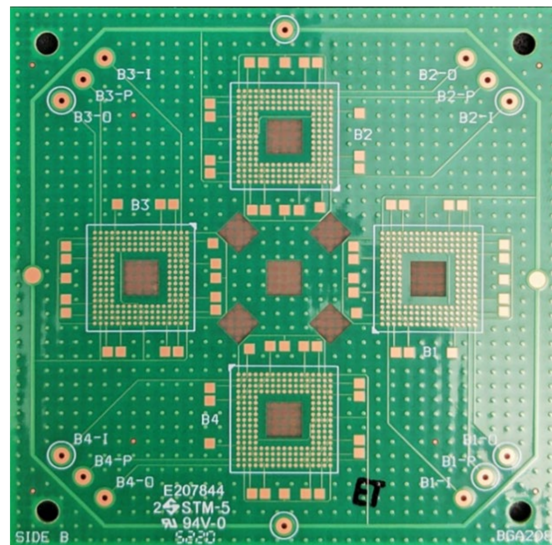



Figure 4.1 Test vehicle illustration

The board type is rigid and consists of six layers. The rigid printed circuit board conformed to the requirements of IPC-6012 class 2. The material used complied with IT-180A. The finished copper outer layer is as per IPC-6012 Class 3. The solder mask is of wet film type with green color. The base copper thickness corresponds to 0.5oz of copper for the inner and outer layers. The literature shows that the corner joints are most susceptible to failure, as they are under most stress. The board is designed to monitor the corner joints separately. Monitoring pads C1, C2, C3, and C4 monitor the corner joints, while S1 monitors the rest of the joints. The board has no vias. The drop boards have non-solder mask-defined (NSMD) pads, and the traces are teardrop shaped. The surface finish used is OSP. The board is designed in a way that it avoids trace and laminate failures. The design of the test vehicle has been modified, changing the point of stress experienced by the component. The PCB is UL-approved. This latest test board design is optimal for determining solder joint reliability. Figure 4.2 depict the front and the back side of an assembled board.

(a) Front side




(b) Back side

Figure 4.2 Test Vehicle with CABGA208 component

**4.4 CABGA208 Design**

This research mainly focuses on evaluating the performance of various doped solder alloys used with BGA components on FR4 substrate. The package chosen is a 15 mm CABGA208. All packages are daisy-chained, as depicted in Figure 4.3. It consists of 208 Input / Output (I/O) with a 15x15 mm body size and has a 17x17 matrix. The pitch is 0.8 mm. The solder spheres are 0.457 mm in diameter. The package thickness is 1.5 mm. Moisture sensitivity is JEDEC level 3. Figure 4.4 provides various solder sphere-related dimensions.

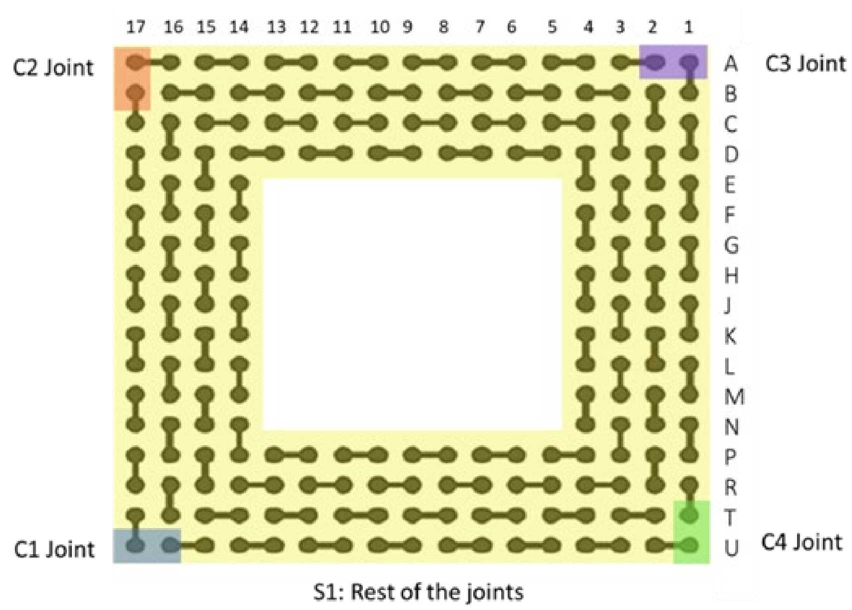
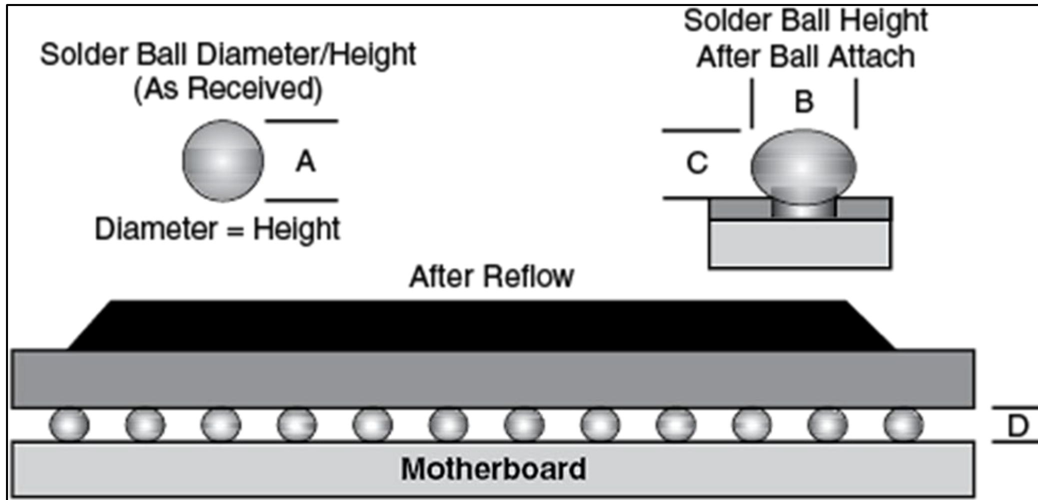



Figure 4.3 CABGA208 daisy chain pattern




| A | B | C | D |
|---|---|---|---|
| 0.46 mm | 0.48mm (± 0.05mm) | 0.36mm (± 0.05 mm) | 0.30mm (± 0.05 mm) |

Figure 4.4 Solder sphere dimensions in CABGA208 component

**4.5 Surface Mount Assembly**

The test boards were assembled at Universal Instrument in Conklin, New York. Flux KESTER TSF-6502 JCR & 6502T and stencil printing with a 6-mil thickness were used to attach the solder balls to the BGA package. Solder paste printing was carried out using a printer, a DEK Europa stencil printing machine, as seen in Figure 4.5. After the paste has been deposited on the PCB substrate, the assembly is visually inspected and certified using a 3D inspection procedure called SPI. This process measures the SPI (solder-paste inspection) paste deposit's volume and surface area.

Figure 4.5 DEK Europa stencil printing machine

The DEK Europa machine was used to print solder paste. After the paste had been printed on the PCB substrate, an SPI quality check was carried out to evaluate the printing's quality and to identify any problems with the solder paste's volume, height, or area as well as any misalignment issues of PCB and the stencil printing). All components are picked and placed using a GSM XE006 tray feeder pick and place machine (Figure 4.6). The machine used a pre-stored algorithm to pick and place packages on the PCB correctly. A second inspection of the assembly is performed to check for package positioning irregularities. Once the components have been placed, the assembly is reflowed in a 10-zone BTU Pyramax 125N convection reflow oven with a conveyor speed of 26 inches/min, as depicted in Figure 4.7. The reflow oven operates in a nitrogen atmosphere.

Figure 4.6 Pick and place machine

Figure 4.7 Reflow oven

The thermal reflow profile was chosen to represent a typical manufacturing process. Both SAC305 and SAC-Bi alloys underwent the same thermal reflow profile. The pre-heat stage lasted approximately 120 seconds, with the temperature increasing from 35 °C to 155 °C. Subsequently, the assembly entered the soak stage, maintaining a temperature range between 155 °C and 200 °C for approximately 60 seconds. The peak temperature reached was 241 °C, and the duration above the liquidus temperature of 217 °C (melting point for SAC305) lasted around 56 seconds. The maximum observed ramp rate was 1.39 °C per second, while the cooling rate employed was 1 °C per second.

For the SnPb alloy, the reflow process is initiated with a pre-heat stage lasting approximately 88 seconds. The temperature gradually rose from 35 °C to 100 °C during this stage. Subsequently,

the assembly progressed into the soak stage, where a temperature range between 100 °C and 150 °C was maintained for about 71 seconds. The peak temperature reached during soldering was 204 °C, with a total duration spent above the melting point of SnPb (183 °C) of around 72 seconds. The ramp rate, which signified the rate of temperature increase, was measured at 0.73 °C per second. After the soldering process was completed, the cooling rate was measured at 1.28 °C per second. The fully assembled boards were then subjected to electrical continuity testing to ensure proper board connections. The reflow profile is visualized in Figure 4.8.

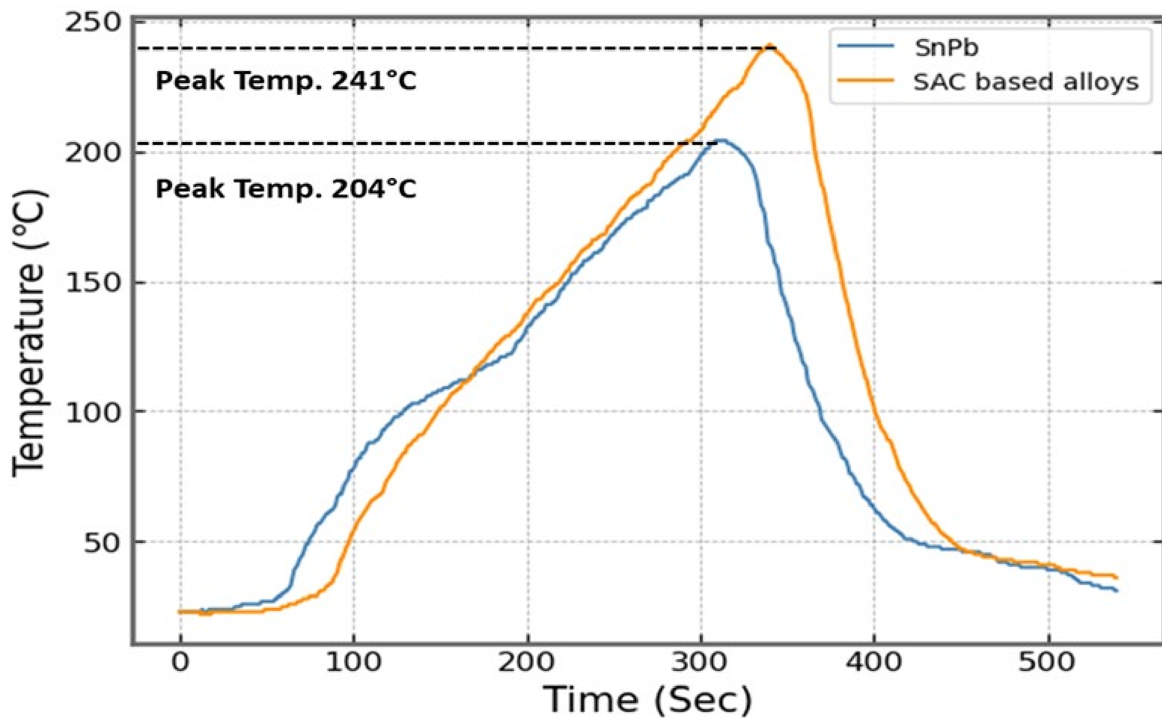



Figure 4.8 SnPb and SAC alloys reflow profile

After the reflow process, an x-ray inspection was performed to check for voids, solder bridging, and other quality concerns in the solder joints in the assemblies. CABGA208 is commonly used

due to the high density of I/Os without complicating the PCB design for this type of component. The solder joints are localized underneath the package. The inspection process is streamlined by X-ray by checking for any defects. Solder bridging is a common defect that develops when solder joints are too near. The formation of voids inside the solder joint is another defect. Because they hinder heat conductivity and can seriously affect reliability, voids are a prevalent problem. An X-ray inspection machine used after assembly is shown in Figure 4.9. An X-Ray image of a CABGA208 component is depicted in Figure 4.10.

Figure 4.9 X-ray machine

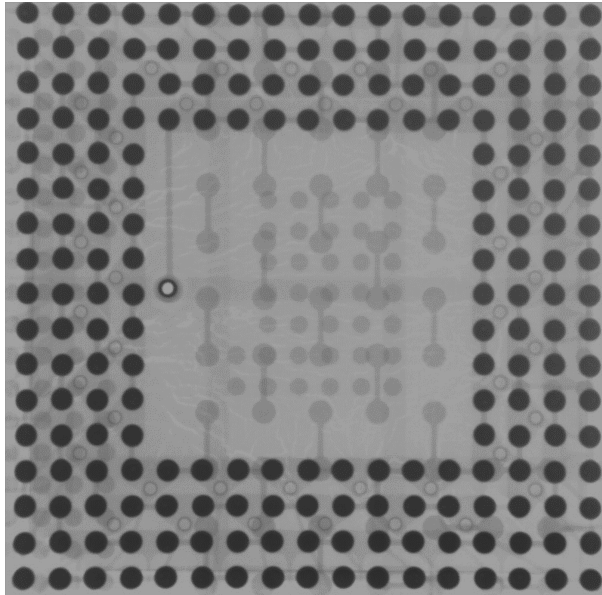


Figure 4.10 CABGA208 X-Ray image

### 4.6 Experimental Setup

Lansmont M23 drop tower was used as the impact tester (Figure 4.11); its specification is provided in Table 2. The drop tower has a cast iron seismic base with dampers. A horizontal fixture made up of aluminum is attached to the shock table. The test boards are mounted on the aluminum drop plate. During the test, the shock table is lifted along the guiding rods to the desired height and then released. Upon release, the shock table strikes the seismic base with a felt cloth attached to it to achieve the desired shock pulse. As per the JEDEC standards, the test boards were placed horizontally with components facing downwards as horizontal board orientation with components facing down results in maximum PCB flexure and, thus, the worst orientation for failures. Test vehicles are mounted symmetrically on top of the drop stage using hexagonal stainless-steel screws as standoffs. The standoff screws are of the dimensions 1/4" Hex, 3/8" Long, 4-40 to 4-40 Thread. The screws were tightened with a torque of 5lb-in as per JEDEC standards. Upon impact, the drop response of interest is the static resistance of daisy-chained solder joints. The accelerometer is used

to determine and adjust the acceleration and the pulse duration during the drop test. The accelerometer used for the tests is PCB Peizotronics 353B04; its specification is provided in Table 3. The drop height was adjusted to achieve the specified G level and pulse duration. Figure 4.12 depicts 1500G, 0.5ms half-sine pulse acceleration.

Table 2. Lansmont M23 drop tower specifications

| **Shock Machine** | |
|---|---|
| **Model** | Lansmont M23 |
| **Machine Type** | Accelerated fall along the guide rods |
| **Shock Table** | |
| **Table Size** | 9.06 in x 9.06 in (23 cm x 23 cm) |
| **Table Weight** | 35 lbs. (16 kg) |
| **Max. Payload** | 80 lbs. (36 kg) |
| **Max. Acceleration** | 5000 G |
| **Min. Pulse Duration** | 0.25 msec (half sine) |
| **Max. Velocity change** | 24 - 32 ft. /sec (7.3 - 9.7 m/sec) |
| **Compatible Pulse Shapes** | Half sine, Trapezoidal, Terminal peak sawtooth |

Table 3. PCB Peziotronics accelerometer specifications

| **Accelerometer** | |
|---|---|
| **Make** | PCB Peizotronics |
| **Model** | 353B04 |
| **Sensitivity** | (±5%)10 mV/g (1.02 mV/(m/s²)) |
| **Measurement Range** | ±500 g pk |
| **Frequency Range** | (±5%) 1 to 7000 Hz |
| **Size** | Height: 1.14 in, Hex: 0.5 in |
| **Weight** | 0.38 oz |

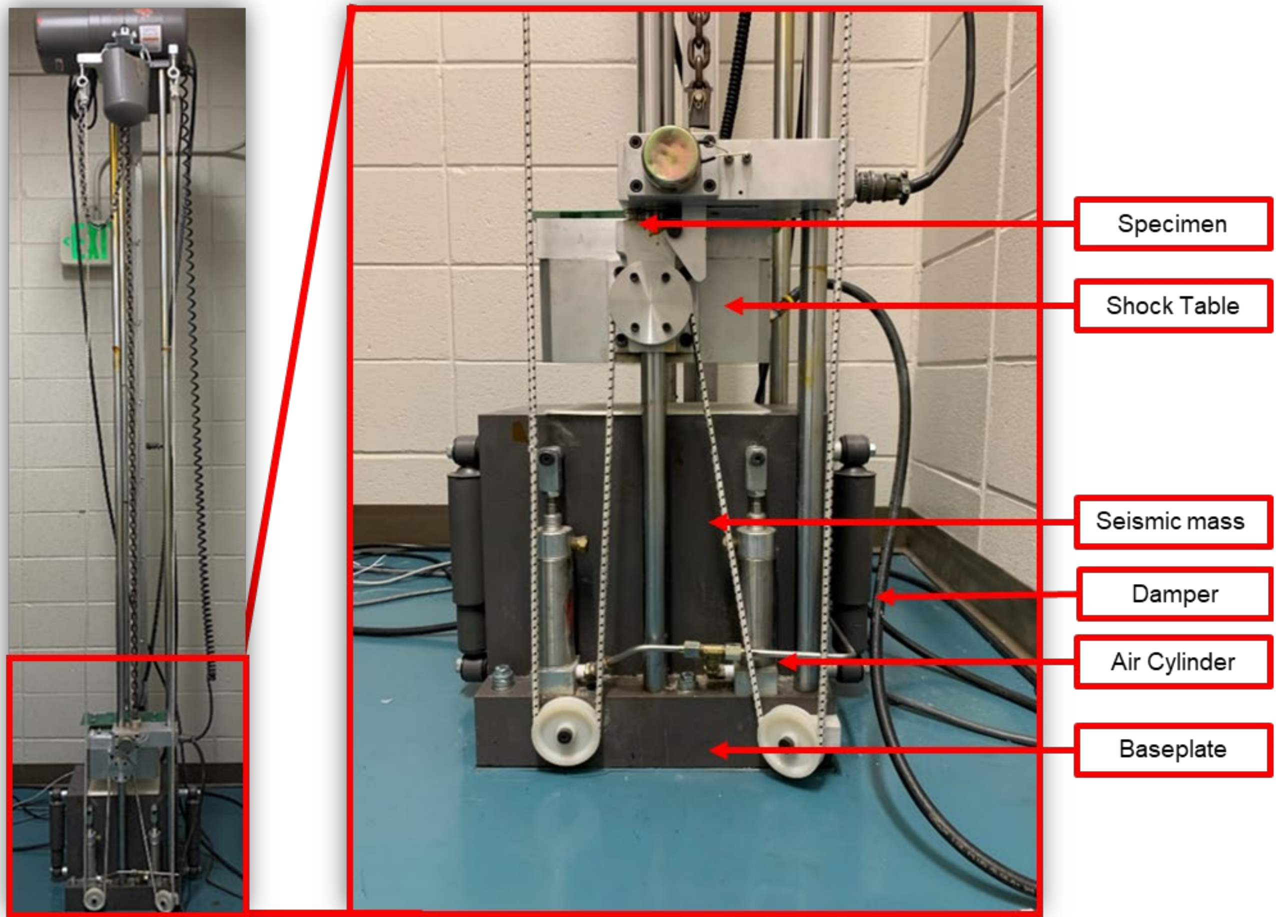



Figure 4.11 Lansmont M23 drop tower

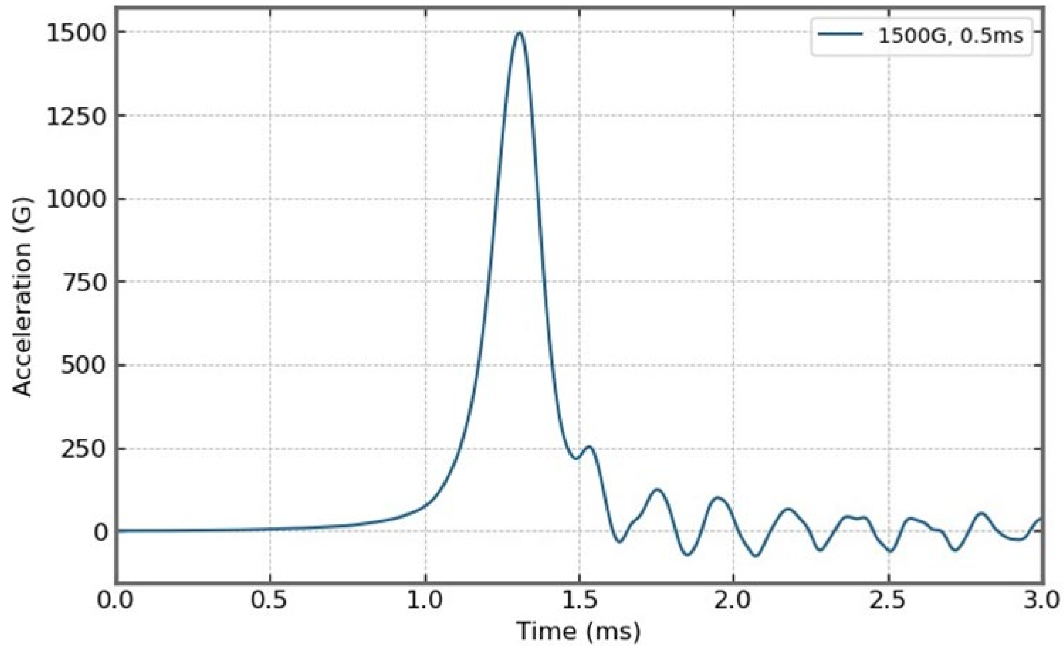



Figure 4.12 Acceleration profile; 1500G, 0.5ms

### 4.6.1 Drop Test Physics

Another crucial element of control is achieving appropriate G levels and impact time duration. The height and kind of strike surface can both be changed to alter the G level. According to kinematics, the relationship between the theoretical impact velocity, $V_b$, and drop height, *H,* is given by:

$$V_b = \sqrt{2gH} \tag{4.1}$$

Here, g is the free-fall acceleration, i.e., 9.81m/s$^2$. Assuming the input will yield a half-sine acceleration curve (from JEDEC standard [43]) with the following equation:

$$G(t) = G_m \sin\frac{\pi t}{T} \tag{4.2}$$

Here, *G(t)* is the acceleration at time *t*, $G_m$ is the peak acceleration level, and T is the duration of impact. The peak acceleration, $G_m$, for a perfectly plastic case (no rebound) when the potential energy is fully transformed into kinetic energy, can be defined as:

$$G_m = \frac{\pi\sqrt{gH}}{T\sqrt{2}} \quad (4.3)$$

Where $g$ is the acceleration due to gravity (9.81 m/s2), $H$ is the drop height, and $T$ is the impact duration. For a perfectly elastic case (complete rebound), $G_m$ is two times larger than the values given in Eq. (4.2). The effect of striking surface is not considered in this equation and should be determined experimentally. At fixed drop height, the product of $G_m$ $and$ T is a constant.

$$G_{m1}T_1 = G_{m2}T_2 \quad (4.4)$$

The felt thickness, drop height, and impact surface conditions (material, shape, and flatness) typically need to be fine-tuned to get the required sinusoidal shape of the acceleration curve (Gm and T values). Thicker felt generates lower peak acceleration and a longer impact duration.

As per the impulse and momentum theory, the velocity after impact, $V_a$, is in the range between 0 (zero rebound) and -$V_b$ (full rebound). Assuming $V_a$ is some fraction of $V_b$, $V_a$= $cV_a$, then according to the impulse-momentum theorem,

$$-mcV_b - mV_b = -\int_0^t mG(t)dt \quad (4.5)$$

$$V_b = \frac{1}{1+c}\int_0^t G(t)dt \quad (4.6)$$

where c is the coefficient of restitution, and its value is between 0 (perfectly plastic impact) and 1 (perfectly elastic impact), G(t) is the acceleration at time t during impact, T is the impact duration, and m is mass. By substituting Eq.(4.1) into Eq.(4.6),

$$A = \int_0^T G(t)dt = (1+c)\sqrt{2gH} \quad (4.7)$$

Where A is the area under *G(t)* (acceleration curve).

### 4.6.2 Room Temperature Drop Test Setup

Specific fixtures were designed which could hold four test boards to conduct room temperature drop tests. Four test boards are mounted symmetrically on the drop plate. Figure 4.13 shows a typical set of boards on the drop table. All the components face downwards. The boards are fastened such that the C4 measuring pad faces the center of the drop plate, and C2 pad is diagonally opposite to C4 pad (Figure 4.14).

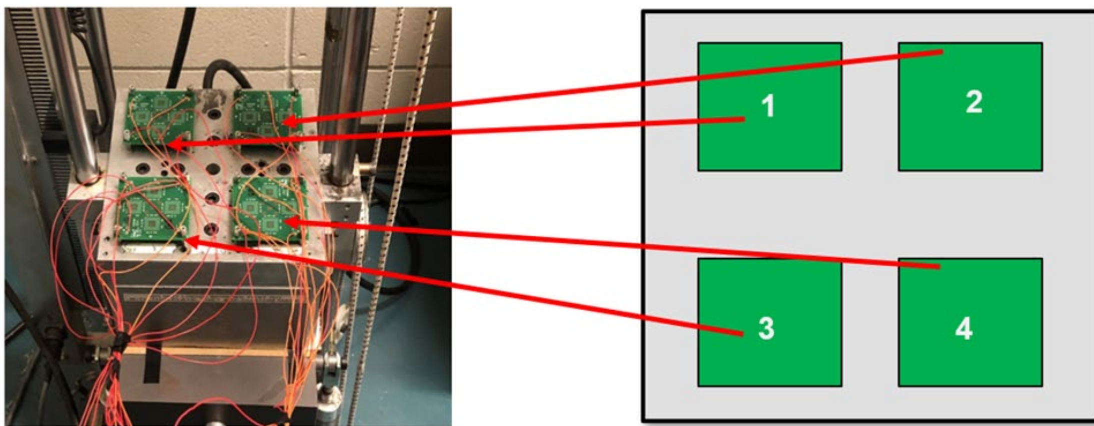



Figure 4.13 Typical set of boards and board location

Proper strain relief is also provided to the cables/wires to avoid failures at the wire-to-board interconnect. All cables are cleared from the drop path. The initial resistance of all nets for each PCB assembly shall be measured and logged before conducting the first drop. The electrical resistance of each net shall be measured in situ during each drop, and all failures are logged.

Calibration and checks were performed after each 100-150 drops. The G-level was calibrated to ensure consistent G-level. The standoff screws were tightened. Cables soldered to the test vehicles were inspected to make sure none of them got disconnected. The guide rods were inspected to make sure it has sufficient lubrication.

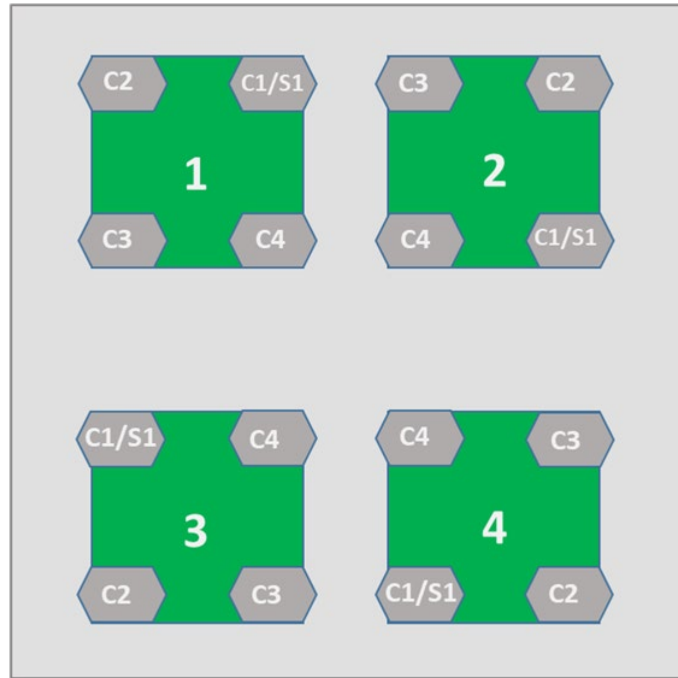



Figure 4.14 Board location and orientation on fixture

### 4.6.3 Elevated Temperature Drop Test Setup

A sheet metal (steel) chamber was designed to conduct drop tests at elevated temperatures. This chamber is 0.25 cm thick and measures 17 cm in length, 15 cm in width, and 15 cm in height, with angles welded at the bottom on each side. It was fastened to the base plate using bolts inserted through the angles, with three bolts used on each side of the chamber. The chamber was designed with four bolts welded to the top surface on the inside. These bolts supported two 9 x 9 cm steel plates of 0.25cm thickness with a flexible silicone rubber heater sandwiched between them. The steel plates were employed to stabilize the heaters during drop impacts, preventing any movement, enhancing their durability, and to evenly diffuse the heat onto the chamber. The sandwich assembly was affixed in place using double nuts on each side of the four bolts to secure its position and prevent any movement due to impact vibrations. The flexible heaters were specifically chosen to protect the heating elements during impacts. These heaters measured 3 x 3 inches and operated

at 120 volts, 90 watts. The chamber was externally insulated using a combination of materials: a 0.35-inch-thick Fiberglass Fabric strip, a 0.25-inch cork sheet, and a 0.25-inch silicone rubber sheet. Additionally, the drop plate was insulated using a 0.25-inch silicone rubber sheet. Each test involved examining one test board at a time (Figure 4.15). The test board was secured at the center of the drop plate using four standoff screws of 4-40 thread, each 5/8 inches in length. Temperature regulation in the chamber was achieved using an Inkbird PID temperature controller alongside a K-Type thermocouple. To minimize movement during testing, the thermocouple was securely positioned inside the chamber. A secondary thermocouple was attached to the component of the test board to confirm it reached the desired test temperature. This thermocouple was later removed before initiating the test. The entire temperature control system was assembled within an aluminum casing measuring 7 inches in length, 5 inches in width, and 3 inches in height. The drop test layout is depicted in Figure 4.16 while the drop tower with the heating chamber is depicted in Figure 4.17.

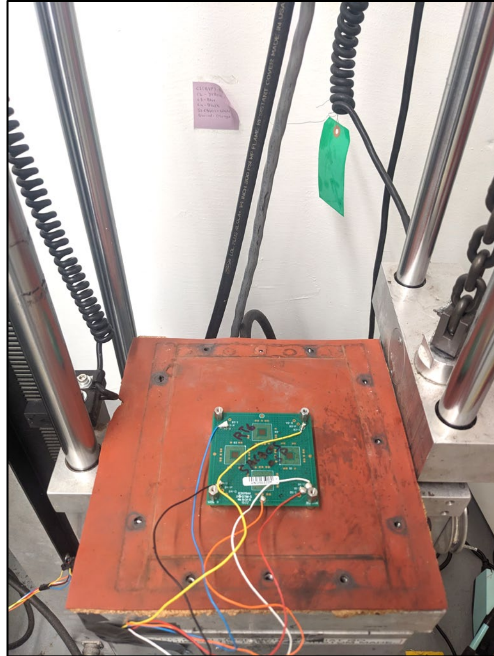


Figure 4.15 Typical elevated temperature board setup

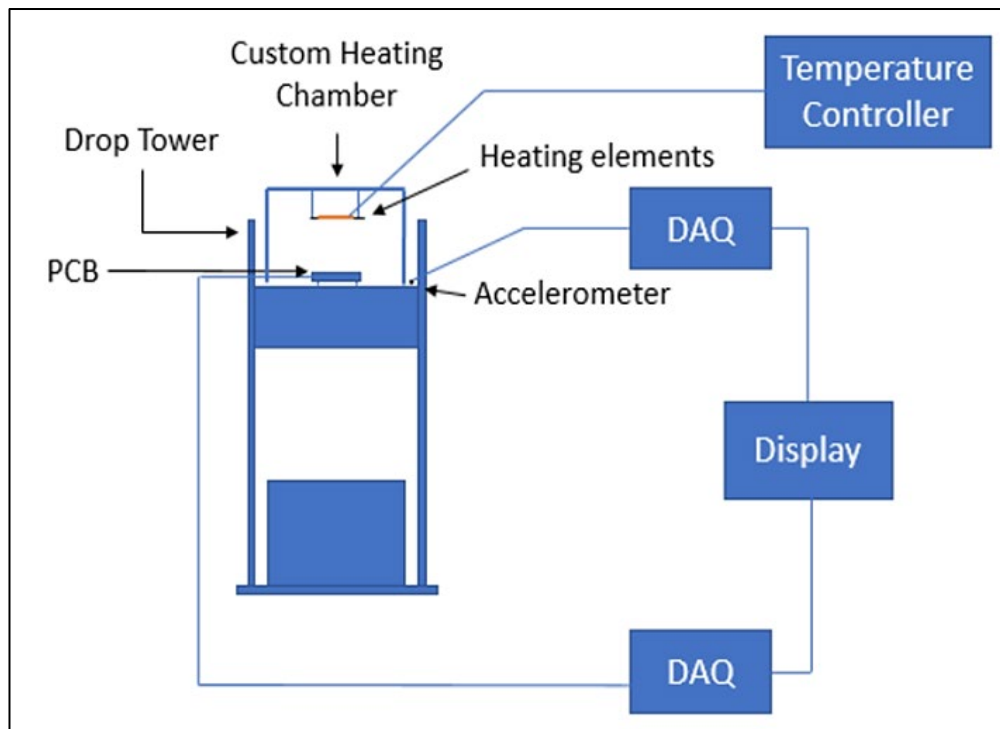



Figure 4.16 Drop test layout with heating chamber

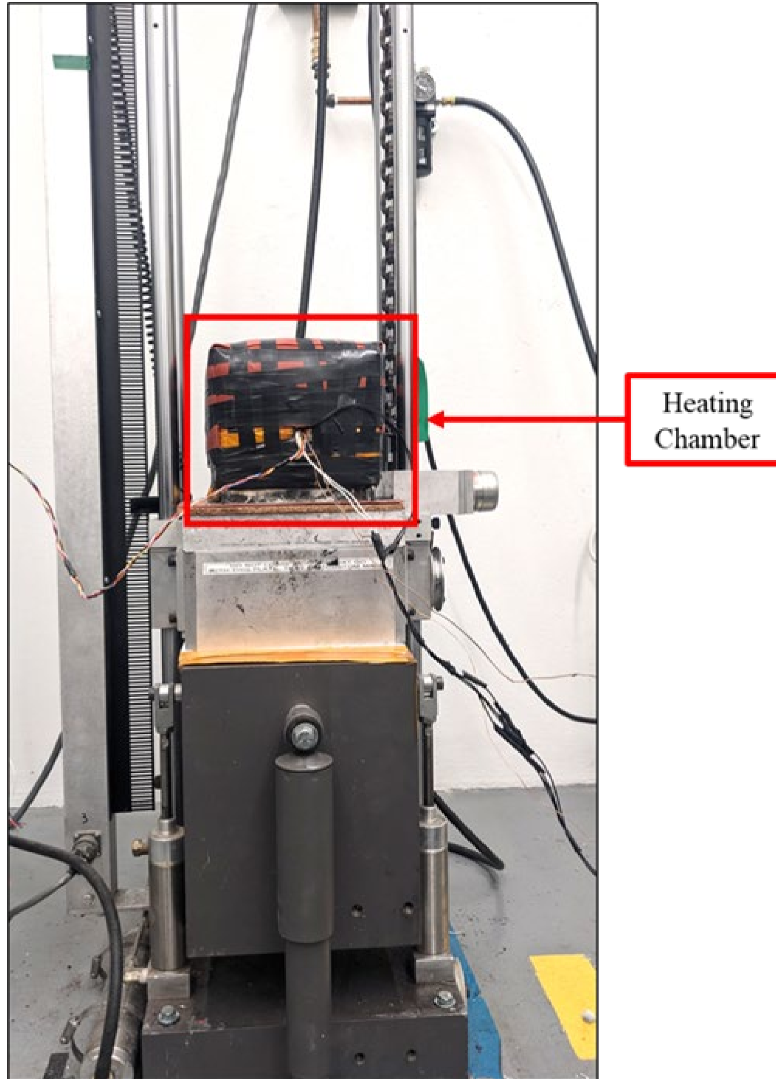



Figure 4.17 Drop tower with heating chamber

The Inkbird PID temperature controller was used to control the chamber temperature. The thermocouple used was of K-Type. The temperature controller system was assembled inside an aluminum casing with dimensions 7 in length x 5 in width x 3 in height, depicted in Figure 4.18. While the flexible heater is depicted in Figure 4.19.

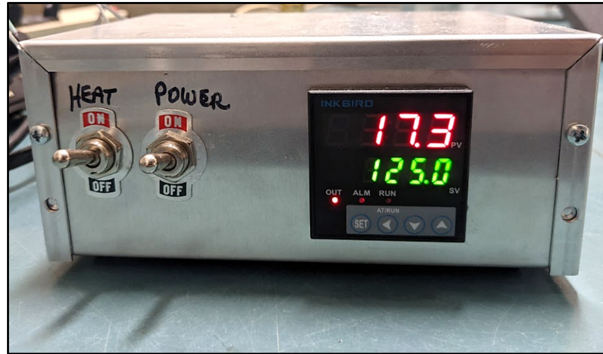



Figure 4.18 Temperature controller

Figure 4.194 Silicone rubber heater

### 4.6.4 Data Acquisition System

The test vehicles are mounted on the drop plate, as shown in earlier in Figure 4.15. Wires are soldered to all the monitoring pads (C1, C2, C3, C4, S1) and the ground pad, the other end of the wires are connected to the data acquisition system to measure the resistance after each drop. The data acquisition system used is Keysight DAQ970A (Figure 4.20). This data acquisition system comes with a 22-channel multiplexer, which can be extended to 66 channels (Figure 4.21). The software interface used is BenchVue (Figure 4.22). The software can be programmed to measure the resistance after specific intervals for the duration of the test, in our case, after each drop. Based on the IPC-9701 standard, the solder joint failure is defined as an increase in resistance of more

than 1,000 ohms. In this study, the solder joint failure is defined as an increase in daisy chain resistance of 100 ohms from the baseline resistance for three consecutive measurements.

Figure 4.20 Keysight DAQ system

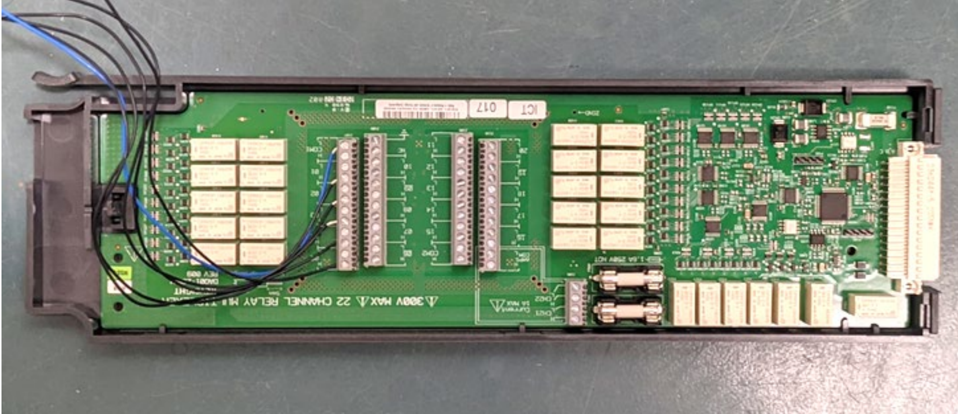


Figure 4.21 Multiplexer; 22 channels

Figure 4.22 Keysight BenchVue software

### 4.7 Failure Analysis

The failed samples are used for microstructure analysis after the test. The failed sample is separated from the PCB using a saw from Allied High Tech Products, Inc. with a diamond sectioning blade. The component is then installed using an epoxy solution (resin and hardener). Hardener and resin are mixed in a 1:6 ratio to prepare the epoxy. A unique label is created for each sample, and it is mounted upright using a Buehler sample holder clip. For curing, the epoxy is placed in the mold for 20–24 hours. The sample is then removed from the mold and prepared for grinding and polishing. All grinding and polishing operations are carried out using the semi-automated grinding machine from Pace Technologies, depicted in Figure 4.23. The grit sizes of the grinding paper are 120, 400, 600, 800, 1000, and 1200, with 1200 being the finest and 120 being the roughest. Once the solder joint's midsection becomes visible, grinding should be halted for 120-grit paper. The sample is rotated 90 degrees after each grit size change. This would ensure that the subsequent, finer paper covers any cuts created by the prior paper. Samples are examined under a microscope

to look for cuts left over from the previous grinding grit after each grinding step. As soon as the grinding is finished, polishing begins. There are four levels of polishing solutions: 3, 1, 0.05, and 0.02 m. The first three solutions contain colloidal silica base material, while the fourth solution contains alumina base particles or suspension. To ensure that the scratches from the previous stage are removed, each polishing stage lasts between 15 to 20 minutes. Residuals from the polishing process are cleaned with an ultrasonic cleaner. Figure 4.24 depicts polishing and grinding pads. In Figure 4.25, polishing solutions of various sizes are also depicted.

Figure 4.23 Pace Technologies automated grinding-polishing machine

Figure 4.24 Grinding pads (left) and polishing pads (right)

Figure 4.25 Polishing alumina suspension of various sizes

An advanced ZEISS Axio Imager prepares samples for optical microscope examination. The sample is examined to identify the failure mode using an M2m optical microscope, an Axiocam 503 color microscope camera, and ZENCore software. To verify for recrystallization, polarized pictures are also produced. Software for interfaces includes the option to save data for later study. Figure 4.26 depicts a ZEISS microscope with a camera. Hitachi S-2460N Scanning Electron Microscope is utilized for additional analysis.

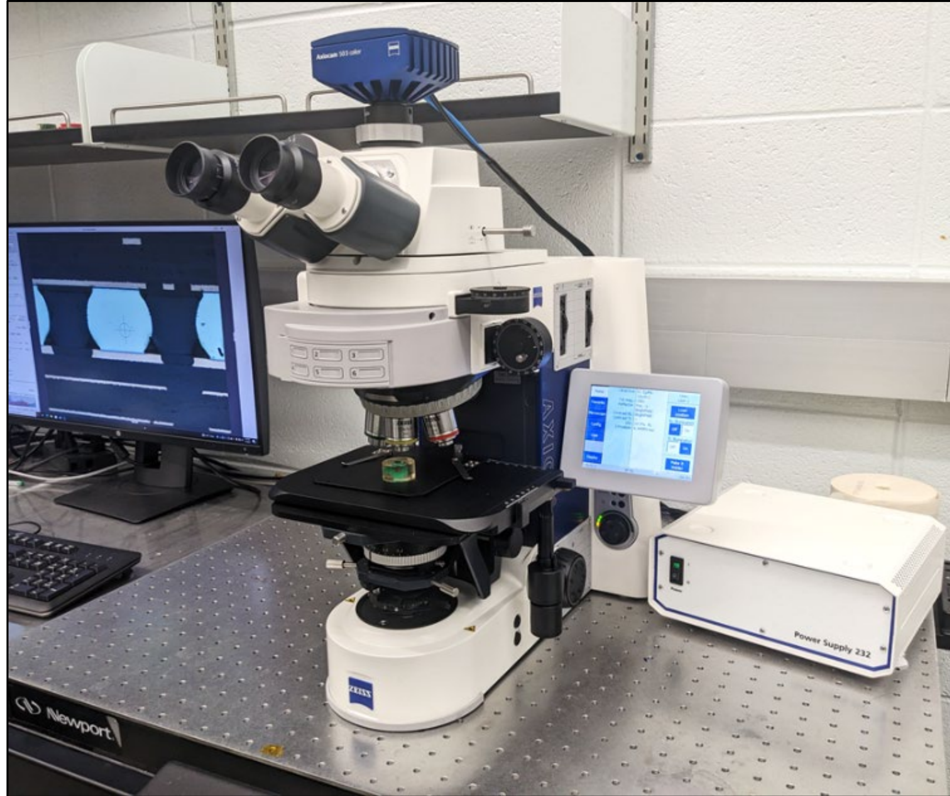



Figure 4.26 ZEISS Axio Imager.M2m optical microscope

### 4.8 Testing Plans

#### 4.8.1 Study I

The first study investigates the drop shock reliability of SAC-based solder alloys compared with SnPb. Five representative solder alloys: SnPb, SAC305, Cyclomax, Innolot, and Sabix were assembled on the test boards with CABGA208 components. This test was carried out at four G-Levels for each alloy, ranging from 500 G to 3000 G. Pulse width ranged from 0.3.ms to 0.6 ms. The test matrix is shown in Table 4.4. The test boards were assembled with OSP surface finish, and all the tests were carried out at room temperature.

Weibull analysis was performed to study the drop shock reliability for each test condition. Additionally, a predictive model based on input energy equation was developed. Microstructure

analysis was performed to determine the failure mode and, the failure location, and crack transitions.

Table 4.4 Study I test matrix

| Solder Alloy | G-Level and Pulse width | | | | | |
|---|---|---|---|---|---|---|
| | 500G, 0.6ms | 1000G, 0.55ms | 1500G, 0.5ms | 2000G, 0.4ms | 2500G, 0.35ms | 3000G, 0.3ms |
| SnPb | 8 | 8 | 10 | 10 | | |
| SAC305 | | 8 | 10 | 10 | 8 | |
| Cyclomax | | | 10 | 10 | 8 | 8 |
| Innolot | | | 10 | 10 | 8 | 8 |
| Sabix | | | 10 | 10 | 8 | 8 |

### 4.8.2 Study II

This study aims at determining the drop shock reliability of SAC305 solder at an elevated temperature. Until now, most of the drop shock testing has been performed at room temperature. Conducting drop shock tests at an elevated temperature is paramount to assure solder joints' reliability under real-life operating temperatures. The boards were tested at temperatures of 25°C, 50°C, 75°C, and 100°C. Eight boards were tested at each temperature. Test boards were assembled on CABGA components with OSP surface finish. The test matrix is given in Table 4.5. The tests were performed at a peak acceleration of 1500G and 0.5ms pulse width as per JEDEC drop test standards B. Weibull analysis was performed post-drop tests to determine the drop shock reliability at each test condition. Additionally, a predictive model based on Arrhenius equation was created. Microstructure analysis was performed to determine the failure location and the failure modes.

Table 4.5 Study II test matrix

| Temperature (°C) | Number of SAC305 Boards |
|---|---|
| **25** | 8 |
| **50** | 8 |
| **75** | 8 |
| **100** | 8 |

**4.8.3 Study III**

This study aims to determine the effect of surface finish on the drop shock reliability of SAC-based alloys. Two representative solder materials (SAC305 and SAC-Q) are assembled on the test boards with CABGA208 components. Both OSP surface finish and ENIG surface finish were reflowed on the solder mask-defined copper pads to study the effect of surface finish on the drop shock performance. The effect of temperature on varying surface finishes and solder alloys will also be studied. The test boards were tested at two temperatures: 25°C (room temperature) and 75°C. The drop shock tests were conducted at a peak acceleration of 1500G and pulse width of 0.5ms, per JEDEC drop test standard B.

For each of the testing conditions, eight test boards were tested. The test matrix is given in Table 4.6. Weibull and ANOVA analysis was performed to analyze the failure data. Subsequently, characteristic life ($N_{63}$) and β10 life were determined. Microstructure analysis was performed to determine each test condition's failure mode and location.

Table 4.6 Study III test matrix

| Solder Alloy | Surface Finish | Temperature (°C) | #Boards |
|---|---|---|---|
| **SAC305** | OSP | 25 | 8 |
| | ENIG | 25 | 8 |
| | OSP | 75 | 8 |
| | ENIG | 75 | 8 |
| **SAC-Q** | OSP | 25 | 8 |
| | ENIG | 25 | 8 |
| | OSP | 75 | 8 |
| | ENIG | 75 | 8 |

# Chapter 5 Comparative Drop Shock Reliability Study of SAC-Based Alloys in BGA Assemblies

## 5.1 Introduction

Recently, there has been exponential growth in the electronics market for portable handheld electronics. This has led the industry to continuously strive for smaller devices with high functionality and smaller form factor. Handheld electronic products are prone to accidental drops, which can cause harm to the internal components. For instance, a solder joint failure due to brittle fracture at the intermetallic compound (IMC) layer. Integrated Circuit (IC) packages are prone to developing cracks in the solder joints due to a combination of mechanical shock and PCB bending during the impact. Repeated drop events can lead to the rupture of solder joints and assembly material due to accumulated damage and fatigue. Drop testing is an experimental method used to design for drop shock reliability.

The primary objective of the study is to conduct a comprehensive comparison between traditional alloys and the more recent Bi-doped SAC alloys, testing them under various acceleration levels. Furthermore, the study aims to evaluate the drop test performance and overall reliability of these alloys when subjected to different impact conditions. In addition, the study aims to develop drop life prediction models for each alloy at different energy levels. Furthermore, it endeavors to conduct hardness tests on each alloy under pristine conditions and establish correlations between the test results and drop life data. It is worth noting that such a comprehensive investigation is currently lacking in the existing literature, which underscores the significance of this study. The study introduces an innovative aspect through its dual approach, which involves comparing Bi-doped SAC alloys with traditional ones and investigating the potential relationship between drop

test performance and hardness characteristics. This study offers valuable insights, contributing to a deeper understanding of the reliability and performance of solder alloys in BGA assemblies.

### 5.2 Test Matrix

This study involved testing five solder alloys (SnPb, SAC305, and three SAC-Bi alloys. For each alloy, testing was conducted at four G-levels and various pulse durations. The test was performed on eight or ten boards at each combination, as indicated in Table 5.1. The test encompassed a spectrum of peak accelerations and pulse widths, spanning from 500G for 0.6ms to 3000G for 0.3ms. As a standardized benchmark, the JEDEC-recommended acceleration profile of 1500G for 0.5ms was employed for all alloy evaluations. The specific acceleration profiles employed during the tests are visually represented in Figure 5.1.

Table 5.1 Test Matrix

| **Solder Alloy** | **G-Level and Pulse width** | | | | | |
|---|---|---|---|---|---|---|
| | 500G, 0.6ms | 1000G, 0.55ms | 1500G, 0.5ms | 2000G, 0.4ms | 2500G, 0.35ms | 3000G, 0.3ms |
| **SnPb** | 8 | 8 | 10 | 10 | | |
| **SAC305** | | 8 | 10 | 10 | 8 | |
| **Cyclomax** | | | 10 | 10 | 8 | 8 |
| **Innolot** | | | 10 | 10 | 8 | 8 |
| **Sabix** | | | 10 | 10 | 8 | 8 |

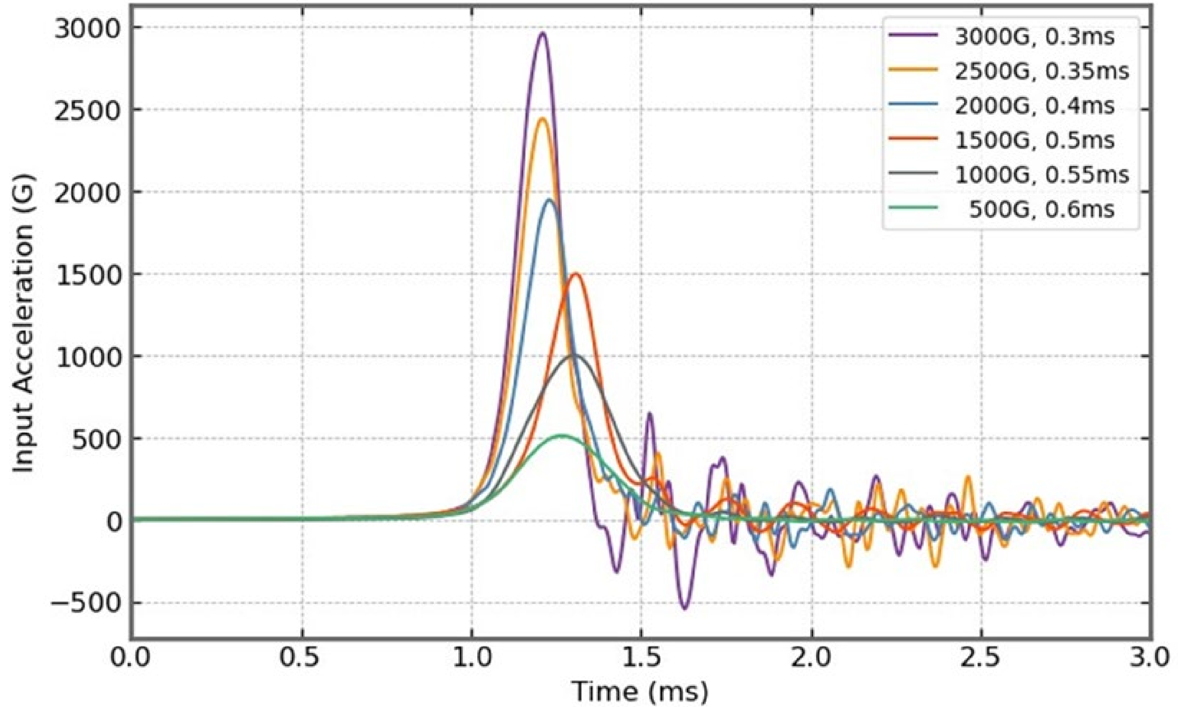



Figure 5.1 Acceleration profiles; 500G -3000G

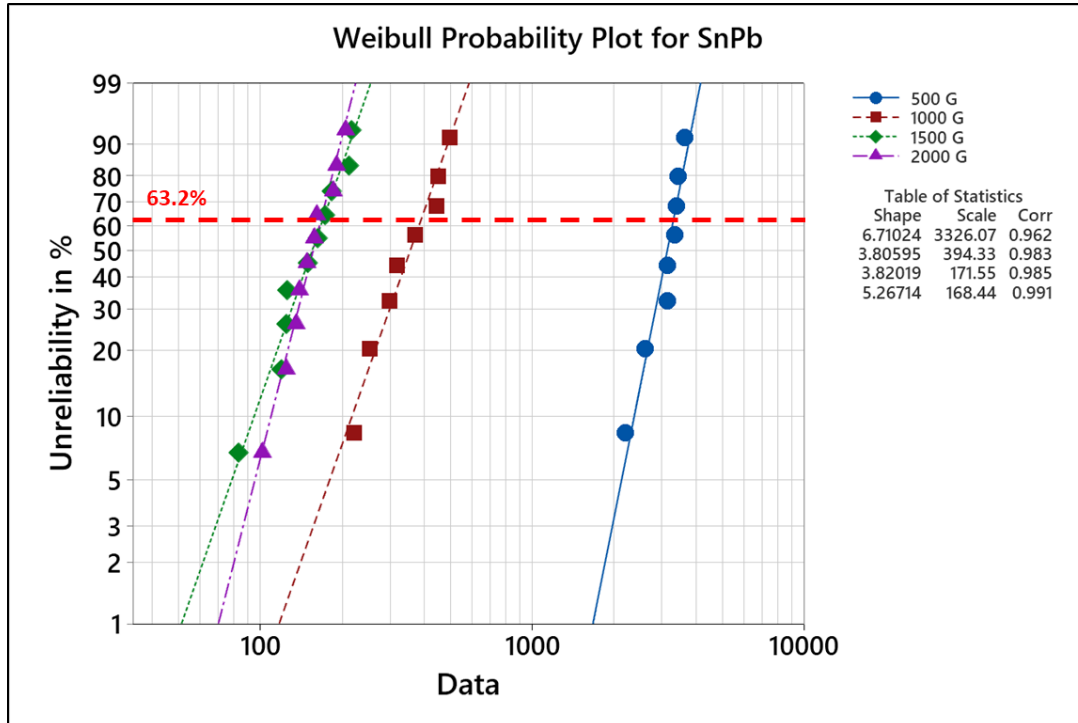
## 5.3 Results and Discussions

The results of this study are organized and discussed in four distinct parts, specifically: Weibull analysis, predictive modeling, microstructure analysis, and a hardness test.

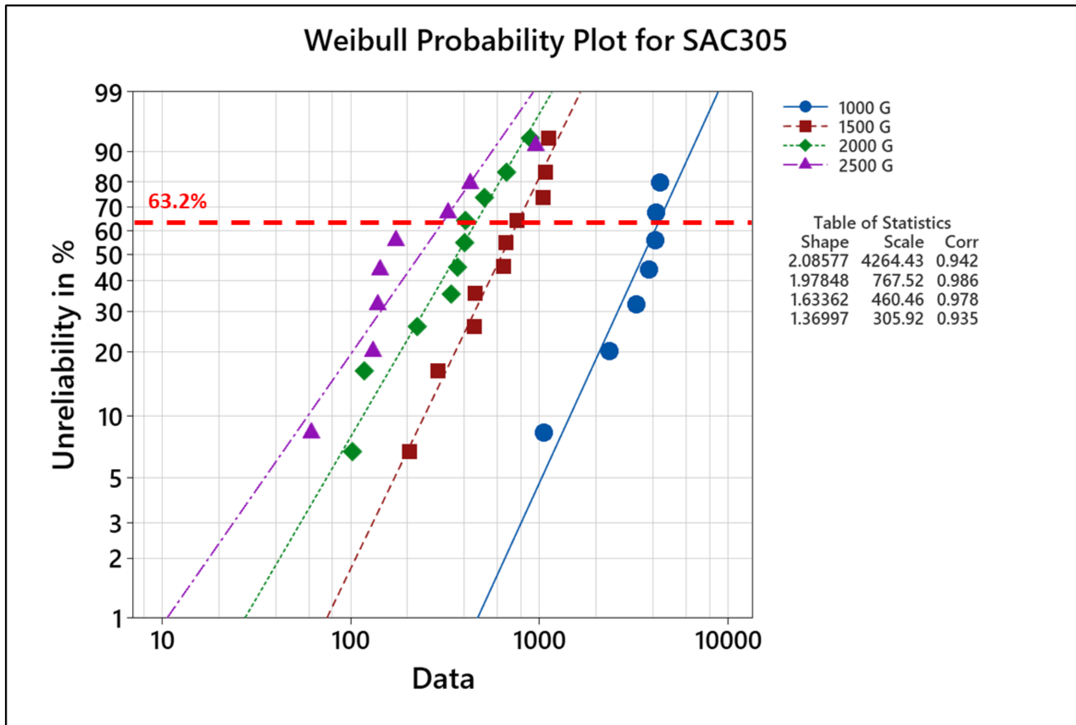
### 5.3.1 Weibull Analysis

Weibull plot of all the alloys for all the four G-Levels is shown in Figure 5.2(a)-(e), while Figure 5.3 and Table 5.2 summarize the characteristic life for all the alloys at various G-Levels. Based on the Weibull analysis, it is evident that Innolot exhibits the best performance among the alloys tested at G-levels of 2000 and below. Subsequently, Cyclomax, Sabix, SAC305, and SnPb follow in that order. However, at 2500 G, SAC305 was observed to outperform the Bi-doped alloys. This difference can be attributed to SAC305 retaining a certain level of ductility, whereas SAC-Bi alloys tend to become more brittle at higher strain rates [124], [125]. As a result, SAC305

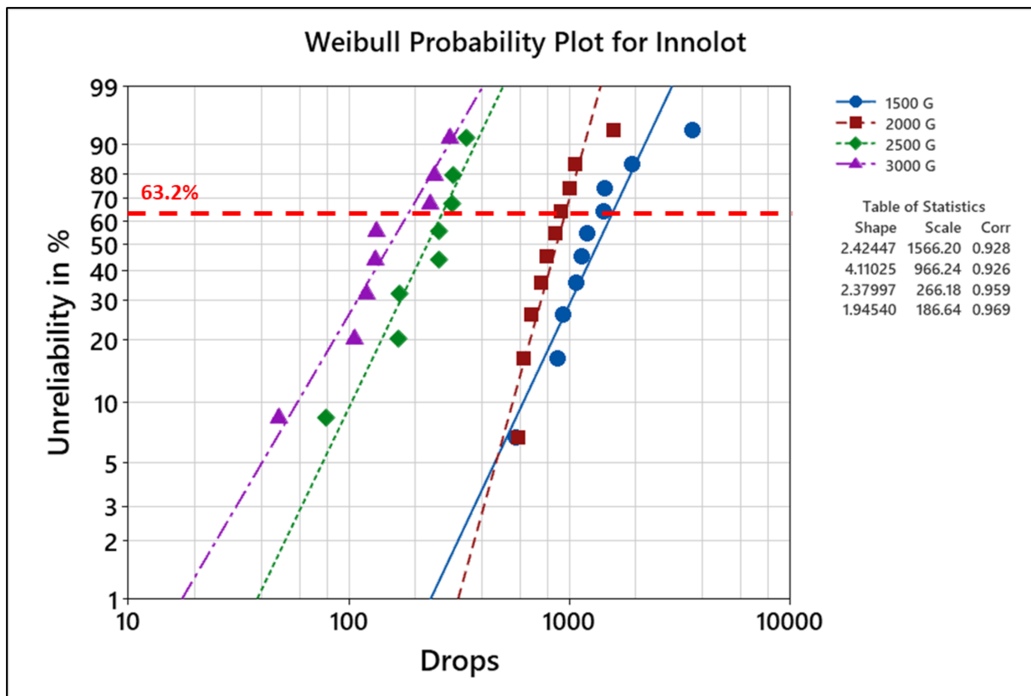
demonstrates higher toughness compared to SAC-Bi alloys. Among the Bi-doped alloys, Innolot exhibited the highest performance, followed by Cyclomax and Sabix consistently across all G-levels.



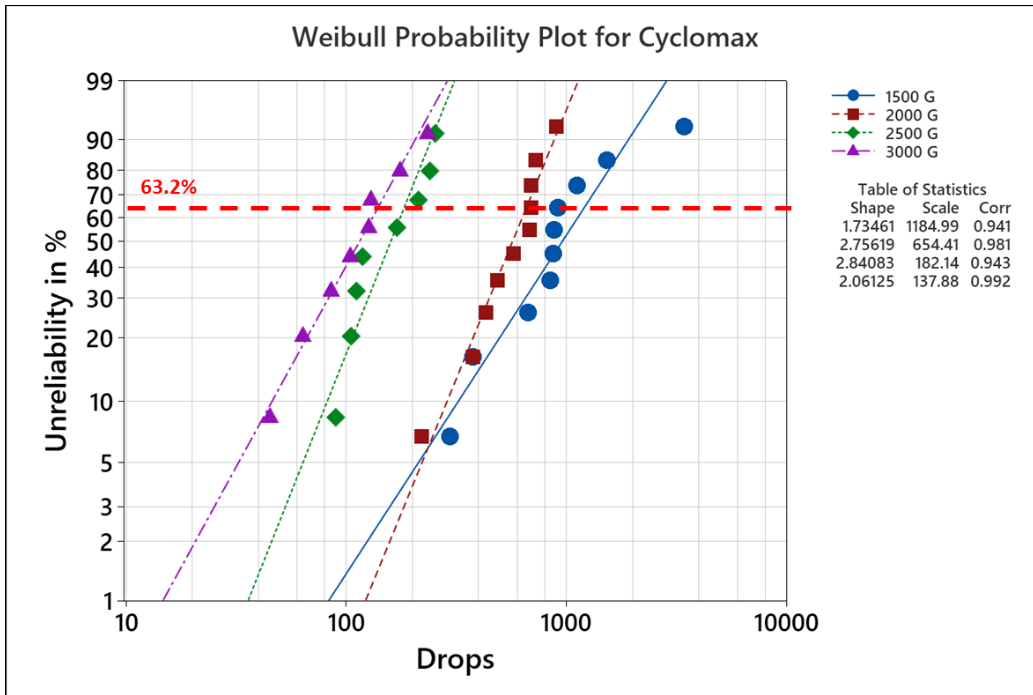

(a) SnPb Weibull plot



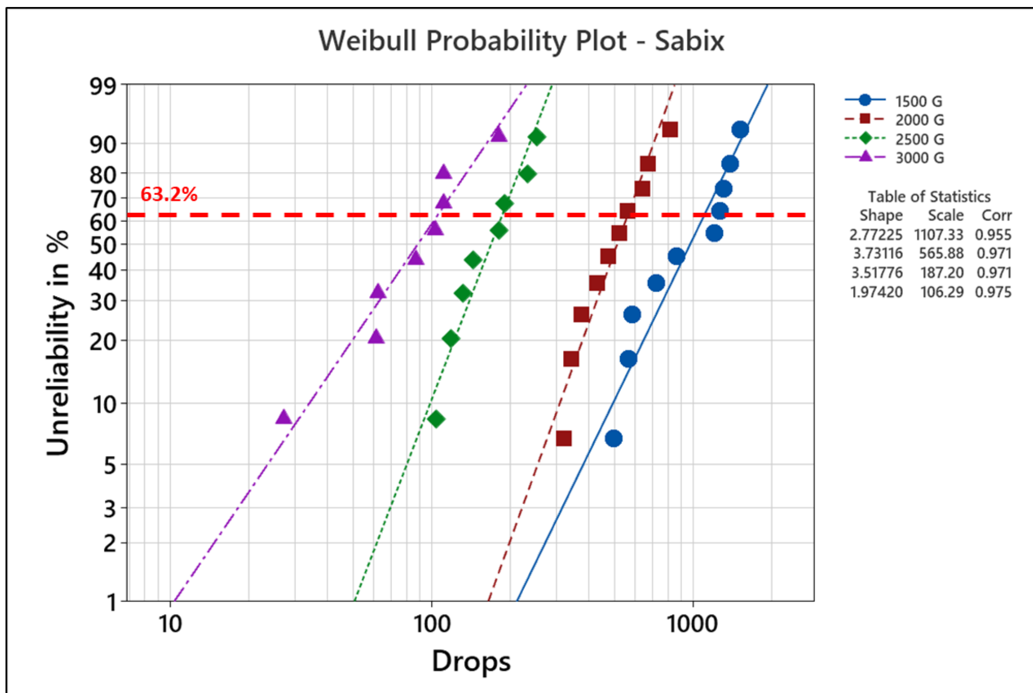

(b) SAC305 Weibull plot




(c) Innolot Weibull plot




(d) Cyclomax Weibull Plot




(e) Sabix Weibull plot

Figure 5.2 Weibull plots for all alloys at all G levels (a) SnPb (b) SAC305 (c) Innolot (d) Cyclomax (d) Sabix

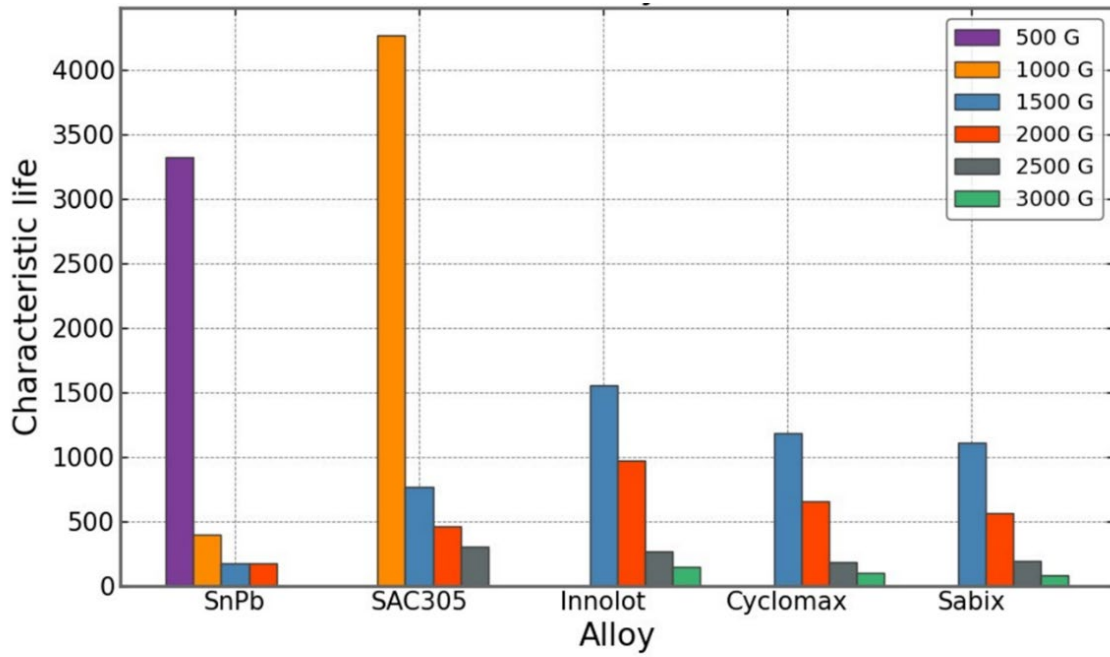



Figure 5.3 Characteristic lives for all alloys

Table 5.2 Comprehensive Weibull analysis summary across all alloys

| Alloy | G-Level | Scale Parameter | Shape Parameter |
|---|---|---|---|
| **SnPb** | 500 | 3326 | 6.71 |
| | 1000 | 394 | 3.805 |
| | 1500 | 172 | 3.82 |
| | 2000 | 168 | 5.267 |
| **SAC305** | 1000 | 4264 | 2.086 |
| | 1500 | 767 | 1.978 |
| | 2000 | 460 | 1.633 |
| | 2500 | 306 | 1.37 |
| **Innolot** | 1500 | 1556 | 0.928 |
| | 2000 | 966 | 0.926 |
| | 2500 | 266 | 0.959 |
| | 3000 | 140 | 0.973 |
| **Cyclomax** | 1500 | 1185 | 0.941 |
| | 2000 | 654 | 0.981 |
| | 2500 | 182 | 0.943 |
| | 3000 | 98 | 0.991 |
| **Sabix** | 1500 | 1107 | 2.772 |
| | 2000 | 565 | 3.731 |
| | 2500 | 187 | 3.518 |
| | 3000 | 79 | 1.32 |

### 5.4 Predictive Modeling

For the predictive modeling of solder interconnect drop shock life, the study focused on the input energy as the key factor influencing damage. When the shock plate strikes the seismic base, the energy is transmitted from the shock table to the standoffs and subsequently to the boards. This leads to flexure in the boards, inducing stress on the interconnects. The study assumes that the force experienced by the board is uniformly distributed across its surface. The input force is expressed as:

$$F(t) = m \times a(t) \tag{5.1}$$

Where, m denotes the board mass, and a(t) represents the input acceleration. The input energy is defined as:

$$E_{input=\frac{1}{2}\times mV^2} \tag{5.2}$$

Where, V represents the velocity change, which is determined by integrating the acceleration curve within the range of ±10% of the G-level, following the JEDEC standards, as illustrated in Figure 5.4.

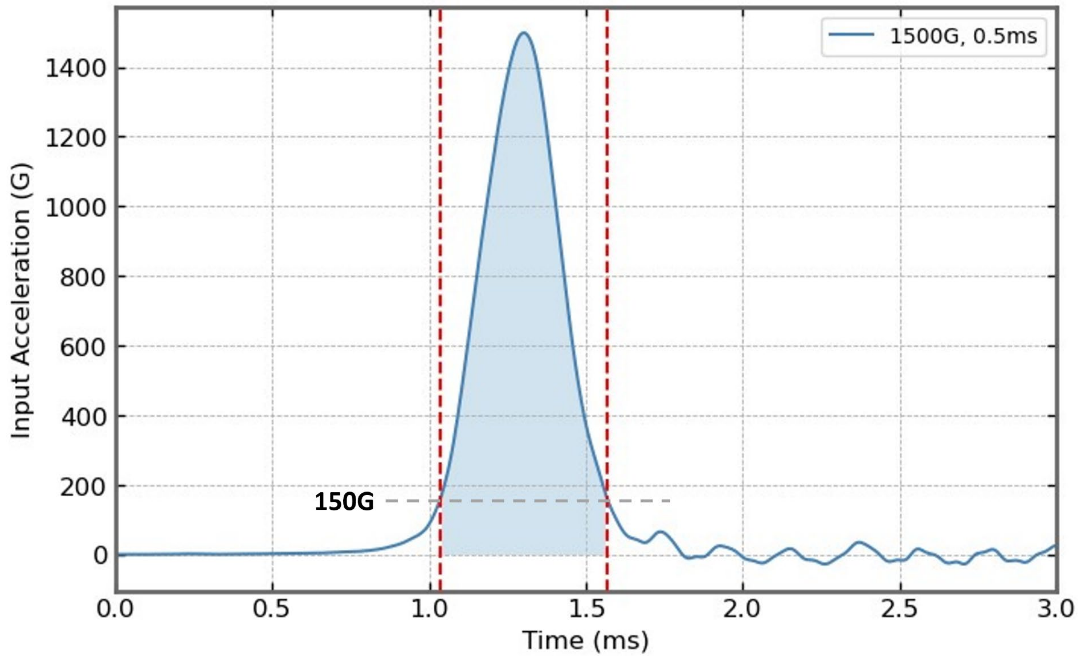



Figure 5.4 Velocity change calculation for 1500G and 0.5 ms pulse based on effective pulse with acceleration ≥ 150G

Equation 5.2 allows for the removal of board mass without substantially affecting results, enabling the calculation of input energy density as shown below:

$$E_{input\ energy\ density=\frac{1}{2}V^2} \tag{5.3}$$

The velocity change for each G-level was determined, and the input energy density was subsequently computed using equation 5.3. Table 5.3 presents the input energy density corresponding to each G-level. A power law was employed to fit the data points and establish the relationship between characteristic life and input energy density. Subsequently, the data points were plotted on a log-log scale, as shown in Figure 5.5. The power law equation can be expressed as [50]:

$$N_{63} = C_1 \times E_{input\ energy\ density}^{C2} \qquad (5.4)$$

Where, $C_1$ and $C_2$ are constants. The table of constants for all the alloys is provided in Table 5.4. The comparison between characteristic life and input energy reveals that SAC-Bi alloys exhibit a similar slope and are clustered together. Similarly, SnPb and SAC305 also demonstrate a comparable pattern. Notably, lower input energy corresponds to a higher characteristic life. However, as the energy density increases, the characteristic life of the Bi-doped alloys declines rapidly compared to the traditional alloys. The Bi-doped alloys outperform the traditional alloys at lower energy levels, while the traditional alloys exhibit better performance at higher energy density levels.

Table 5.3 Input energy at different G-Levels

| **G-level** | **Input Energy Density (Joule/Kg)** |
| --- | --- |
| 500 | 1.3994645 |
| 1000 | 3.7019205 |
| 1500 | 5.800418 |
| 2000 | 6.822818 |
| 2500 | 8.5698 |
| 3000 | 11.2765005 |

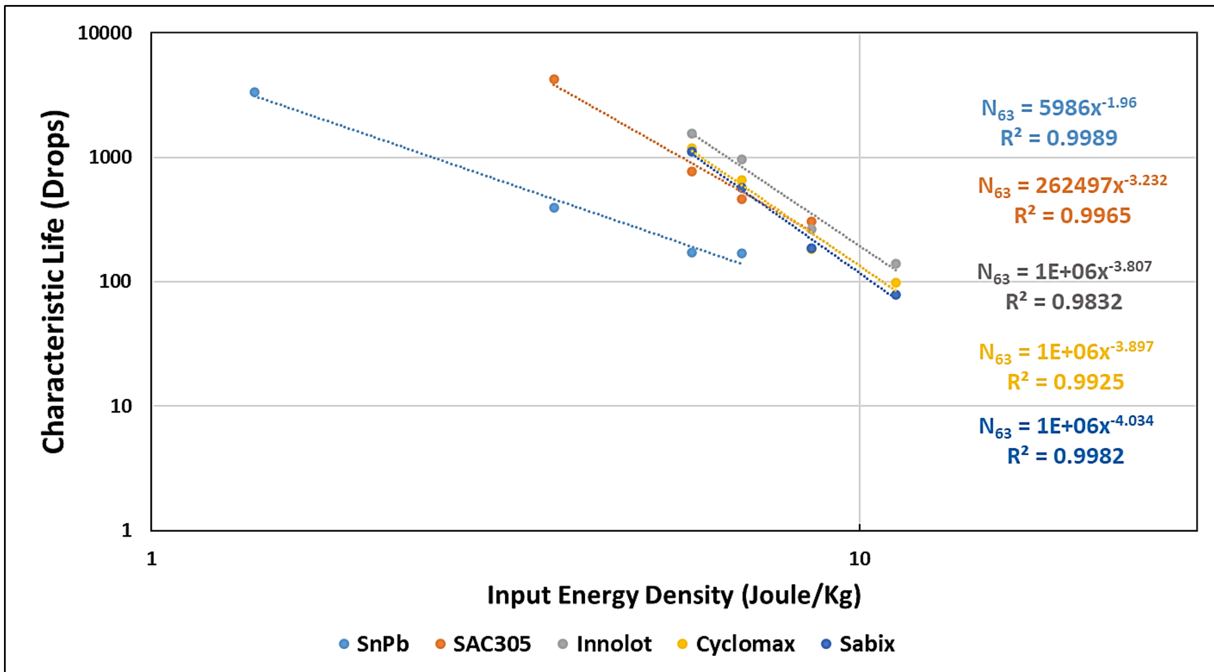



Figure 5.5 Characteristic life vs Input energy

Table 5.4 Table of constants for power law equation ($C_1$ & $C_2$)

| Alloy | $C_1$ | $C_2$ |
|---|---|---|
| SnPb | 5986 | -1.96 |
| SAC305 | 262497 | -3.232 |
| Innolot | 1E+06 | -3.807 |
| Cyclomax | 1E+06 | -3.897 |
| Sabix | 1E+06 | -4.034 |

## 5.5 Microstructure Analysis

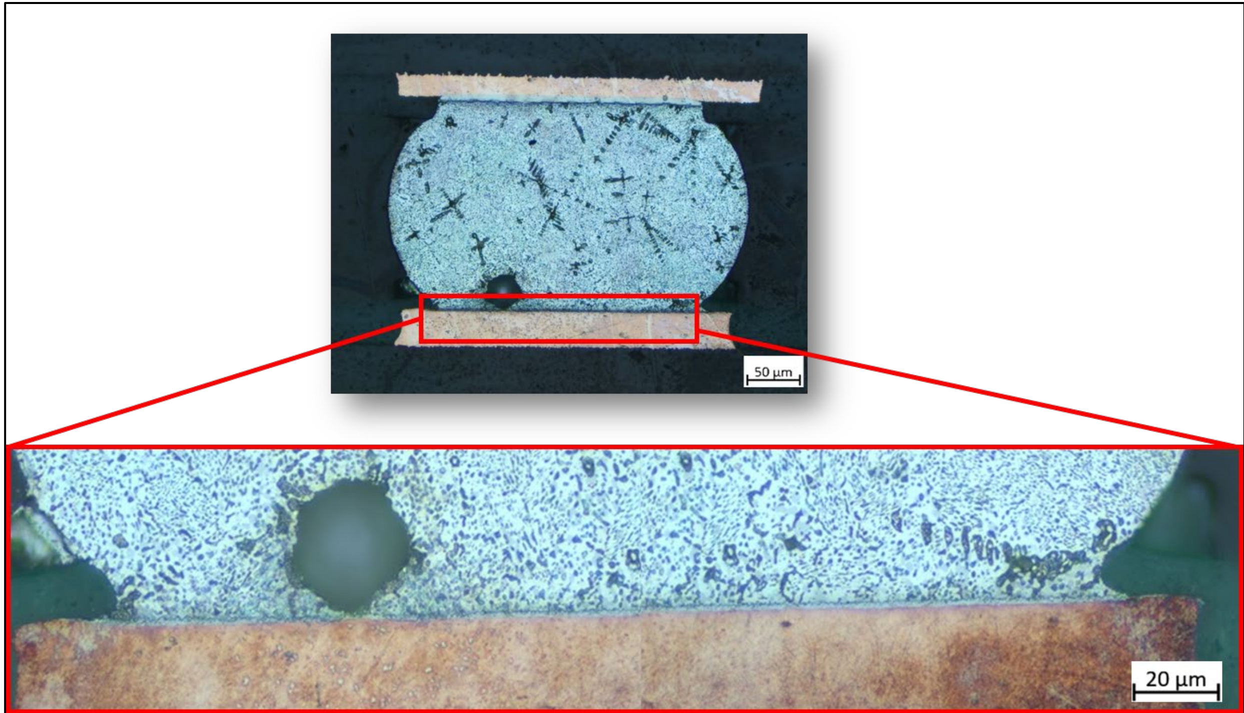
The main objective of the failure analysis was to study the microstructure evolution of the IMC layer in the solder joints, aiming to develop a comprehensive understanding of the reduction in fatigue life of the solder alloys. This analysis involved cross-sectioning the failed samples and

capturing microscopy images to investigate the microstructural changes. Subsequently, the failure modes in the solder joints were identified, providing valuable insights into the factors contributing to the diminished fatigue life of the tested alloys. Several samples underwent cross-sectioning for each condition, and the corresponding representative images are presented in Figures 5.6-5.10. Figures 5.7(b)-(g) illustrate the visual representation of SAC305 solder joint failures across various G-level conditions. Significantly, the crack's behavior and position exhibit variations depending on the specific G-levels. At 1000 G, as displayed in Figure 5.7 (b), the crack is confined exclusively to the bulk solder. In contrast, Figures 5.7 (c) and 5.7 (d) at 1500 G and 2000 G, respectively, exhibit cracks that extend through both the bulk solder and the IMC. At 1500 and 2000 G, the presence of voids near the IMC layer contributed to causing a mixed failure mode. Complete IMC layer failures were observed where there were no voids near the IMC layer, at 1500 and 2000 G. Notably, Figure 5.7 (f) emphasizes a significant transition occurring taking place at 2500 G. At this level, the failure becomes prominently focused within the IMC, with no instances of mixed bulk solder failures being detected. In conclusion, the failure mode of SAC305 shifted from bulk failure at 1000 G to a mixed mode/IMC failure IMC at 1500 G and 2000 G, and eventually transitioned entirely to IMC failure at 2500 G. This transition can be attributed to changes in material properties resulting from increased strain rates. As the G-level increases, the strain rate on the board escalates [36].The solder's viscoplastic characteristics or its dependence on strain rate lead to a heightened ultimate tensile strength and elastic modulus at higher strain rates. Consequently, this effect curtails plastic deformation while promoting brittle fracture [33], [37], [38]. Consequently, a progression from ductile to mixed mode and finally to brittle fracture is observable with an elevation in input energy or G-level.

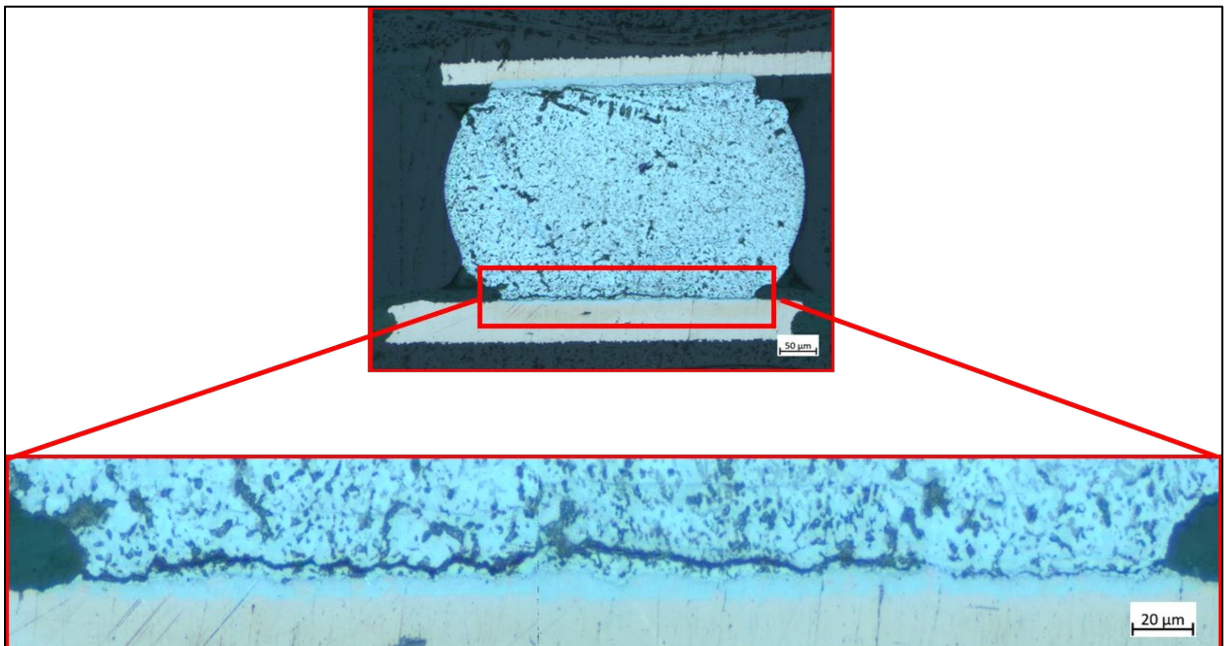
In Figure 5.6(b)-(e) depicting SnPb, cracks were detected within the bulk solder. Conversely, for Innolot, Cyclomax, and Sabix, as indicated in Figures 5.8-5.10, cracks were exclusively observed within the IMC. In conclusion, for SnPb, the crack was observed in the bulk solder at all the G-levels. For Innolot, Cyclomax, and Sabix, cracks were observed in the IMC for all G-levels, and no instances of pad cratering were observed. The cracks were predominantly observed towards the board side in all cases, except for two specific instances of SAC305 at 2000 G and 2500 G. In those instances, cracks were observed at both the board and component side.

### 5.5.1 Microstructure Analysis of Eutectic SnPb

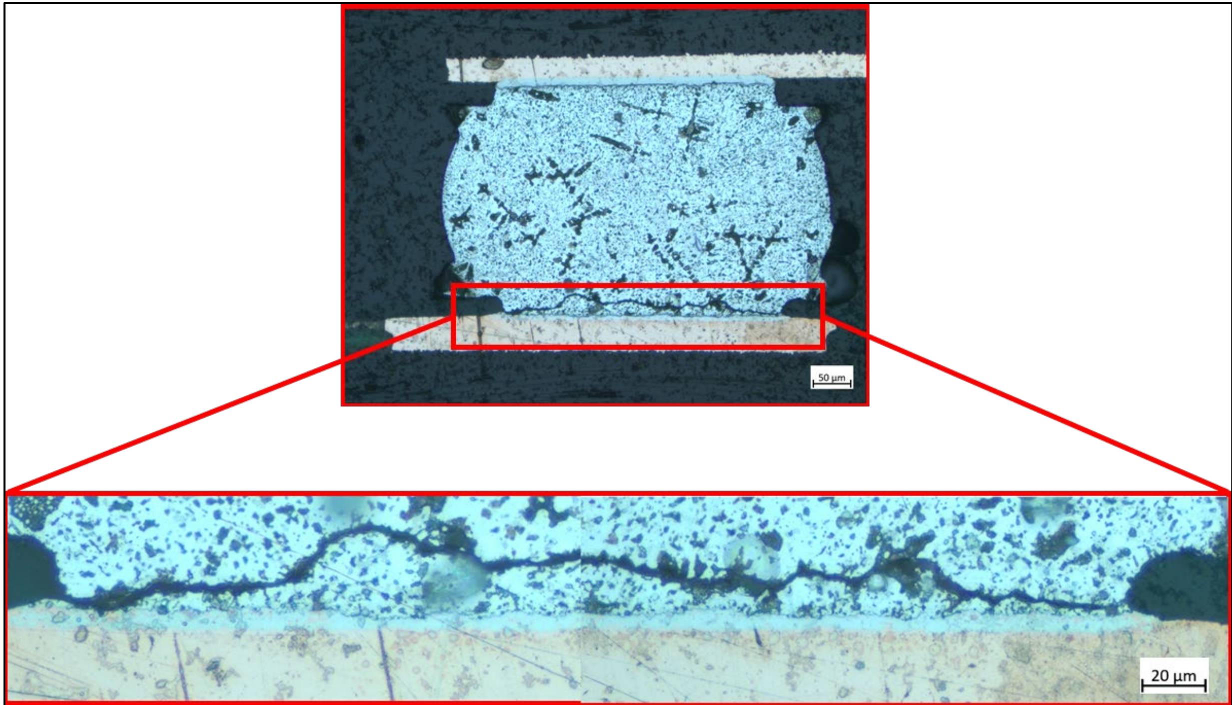
In all the cases, it was observed that the crack was complete in the bulk solder, indicating ductile failure mode. Below are the microscopy images after reflowing failed SnPb solder at 500 G, 1000 G, 1500 G, and 2000 G acceleration. It can also be observed that all the cracks was formed towards the board side.



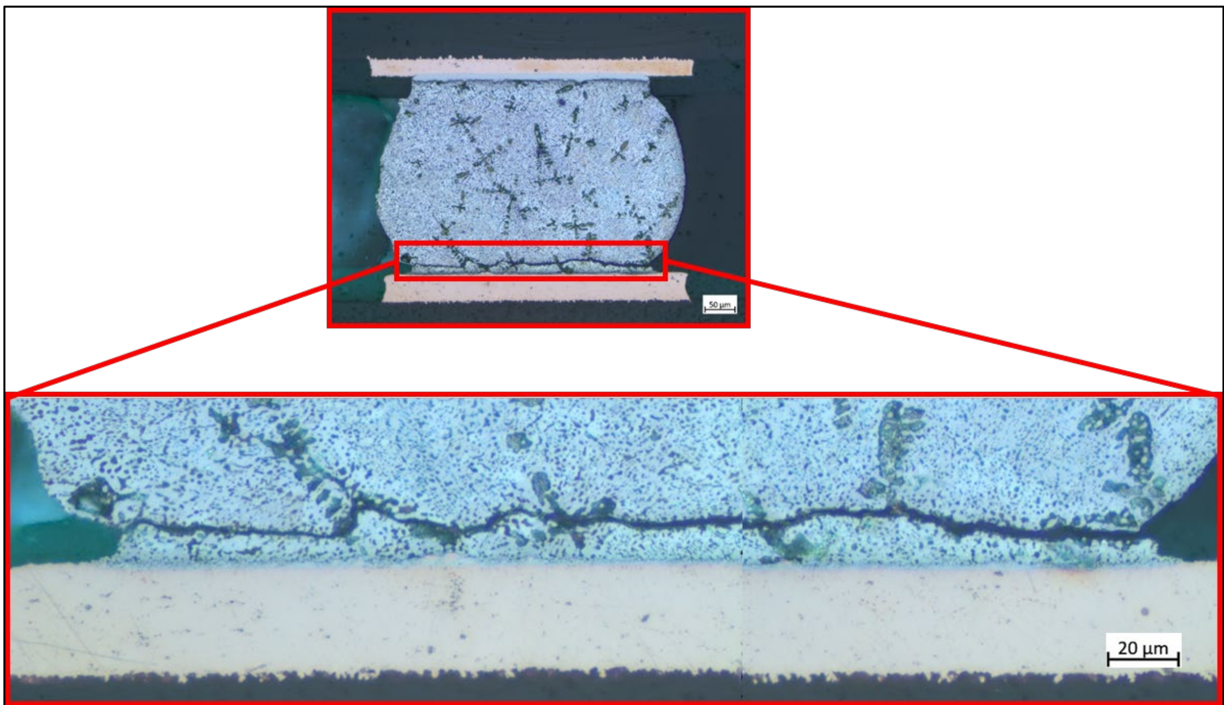

(a) SnPb solder joint after reflow



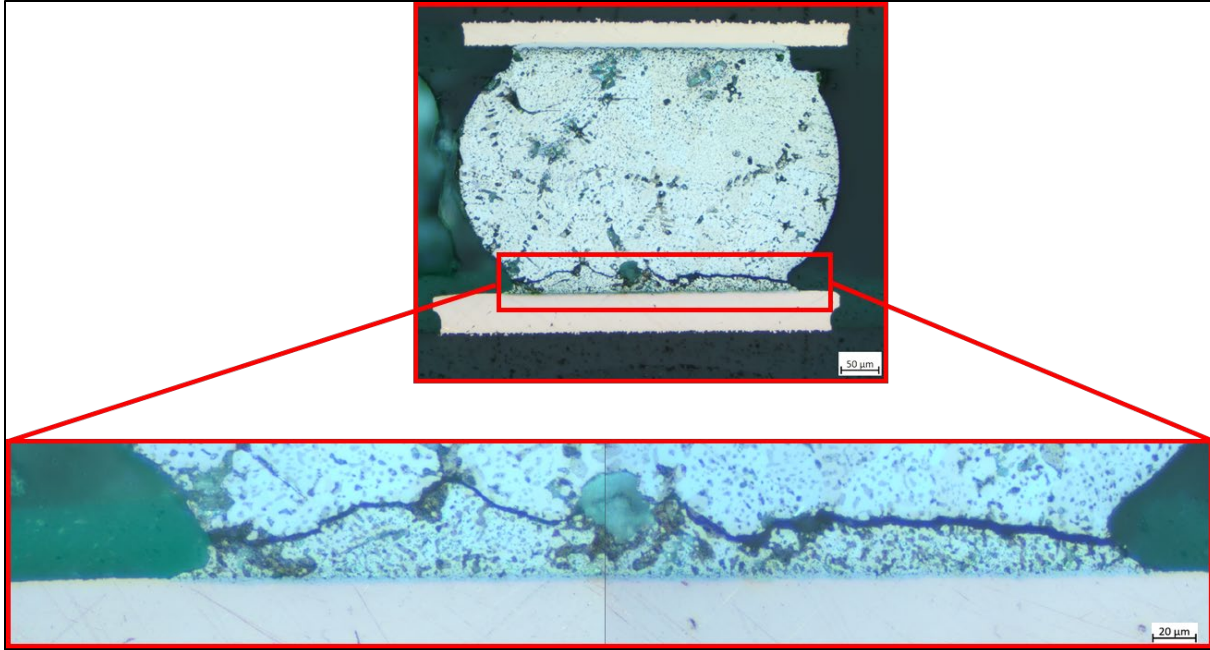

(b) SnPb at 500 G - bulk solder failure




(c) SnPb at 1000G - bulk solder failure




(d) SnPb at 1500 G – bulk solder failure

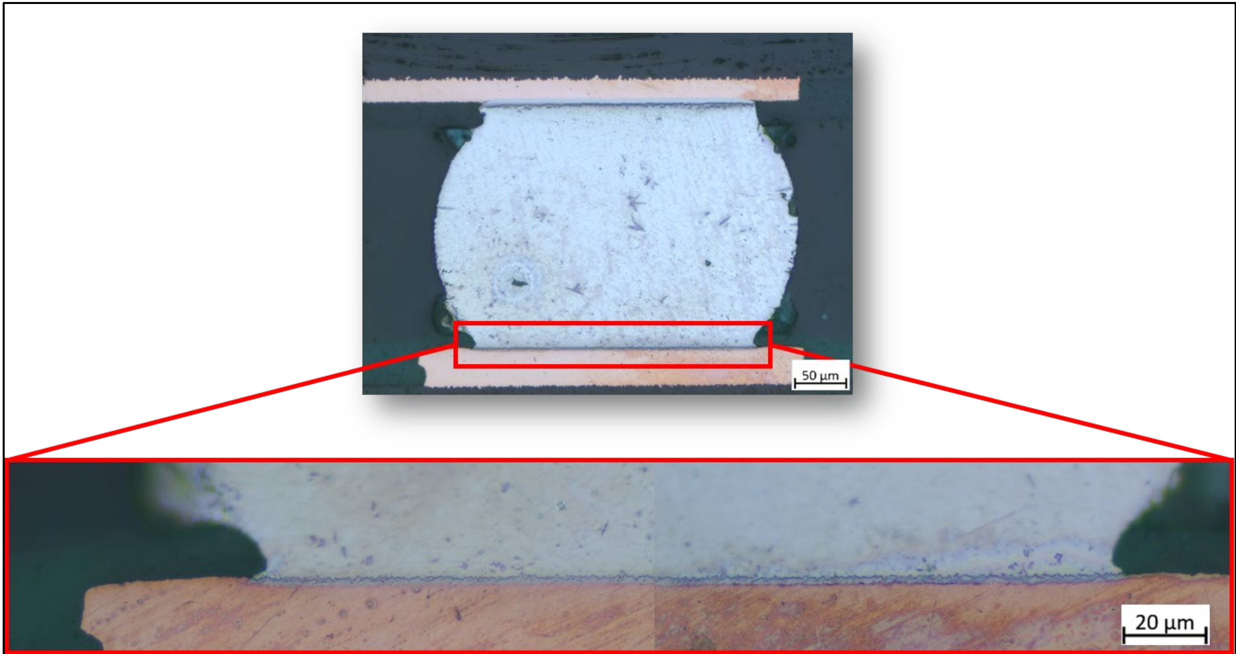



(e) SnPb at 2000G – bulk solder failure

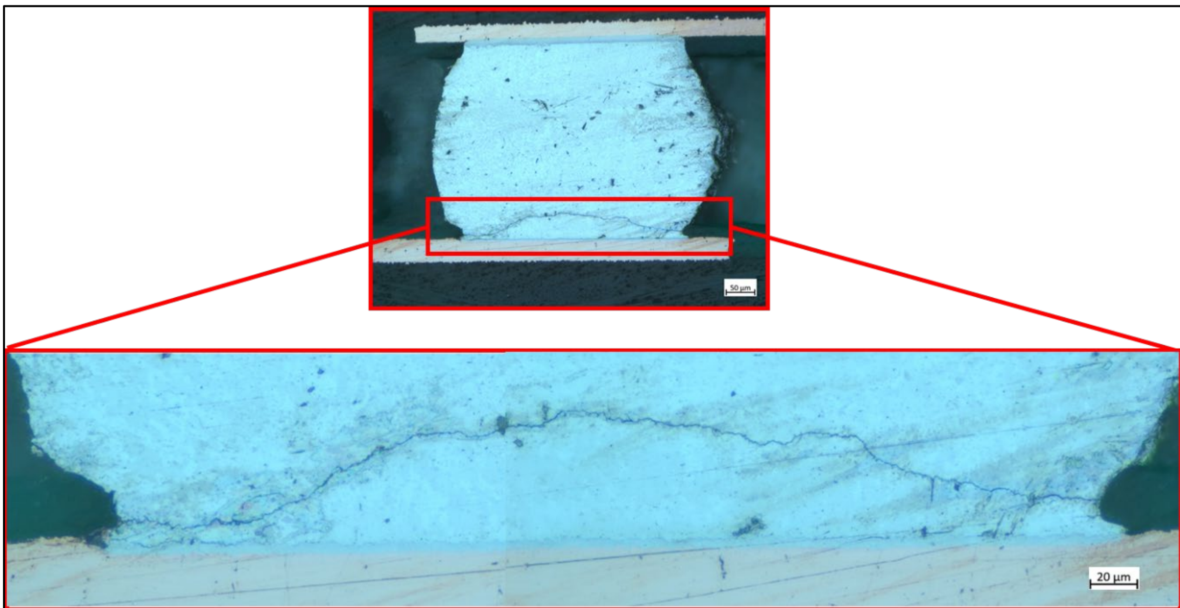
Figure 5.6 SnPb solder joint microstructure after reflow and post failure for all G levels

### 5.5.2 Microstructure Analysis of SAC305

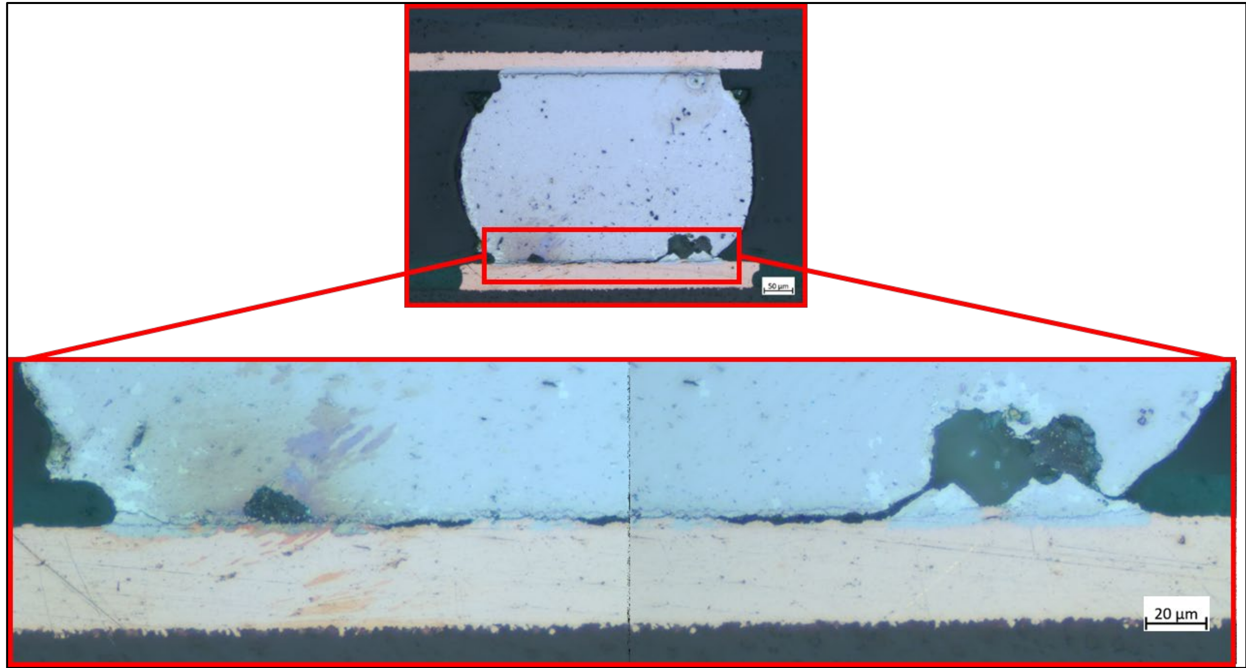
Below are the microscopy images after reflow and failed SAC305 solder joints at 1000 G, 1500 G, 2000 G, and 2500 G acceleration levels. At 1000 G the crack was formed in the bulk solder. At 1500 G, the crack was a combination of bulk crack and IMC layer crack. At 2000 G the crack was mixed (bulk and IMC layer). At 2000 G and 2500 G only IMC layer cracks were observed. It can also be noted that at 2000 G and 2500 G component side IMC layer cracks were observed.



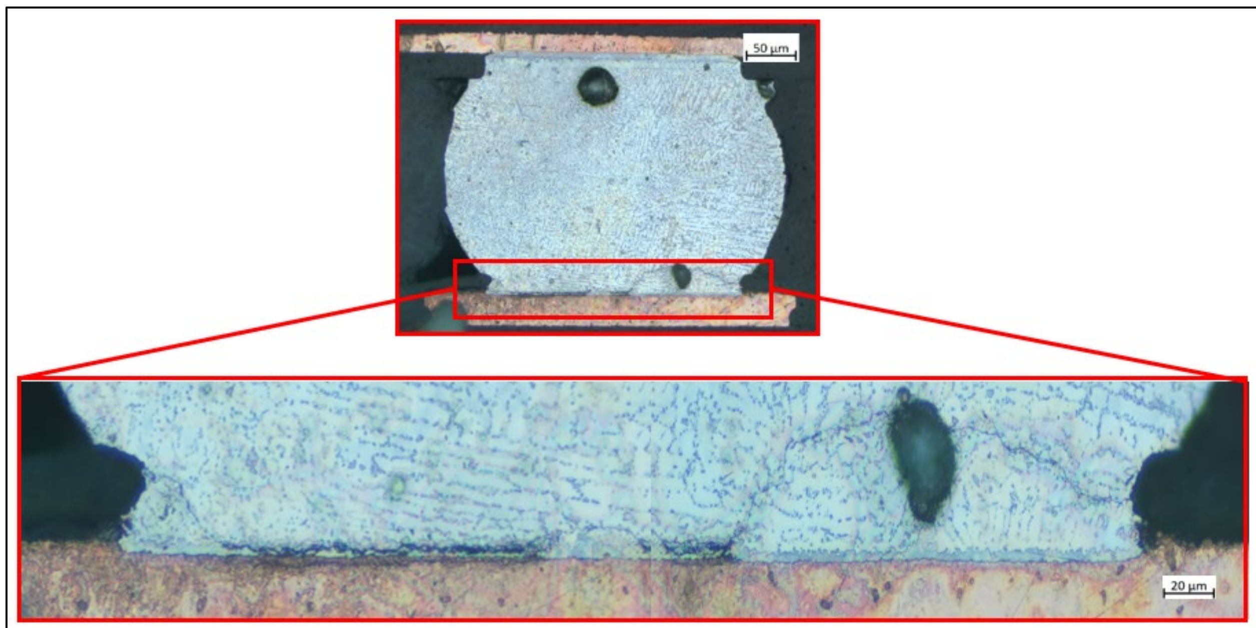

(a) SAC305 solder joint after reflow



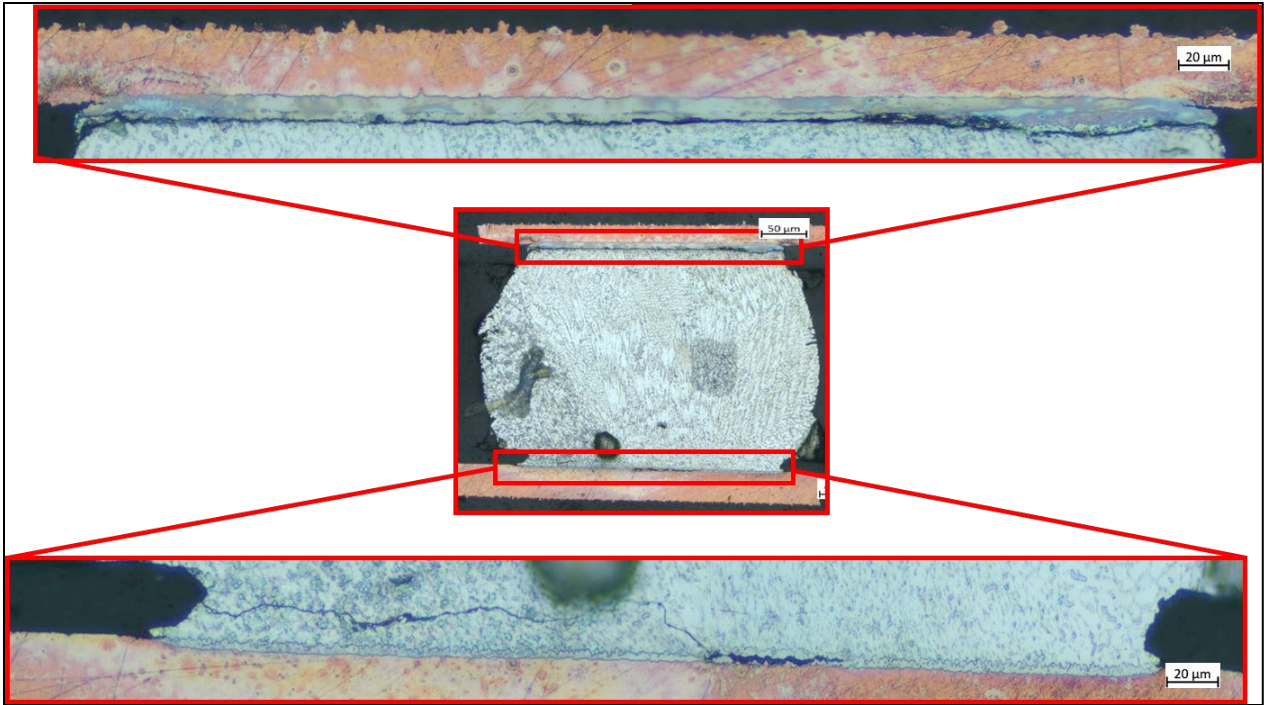

(b) SAC305 at 1000 G - bulk solder failure



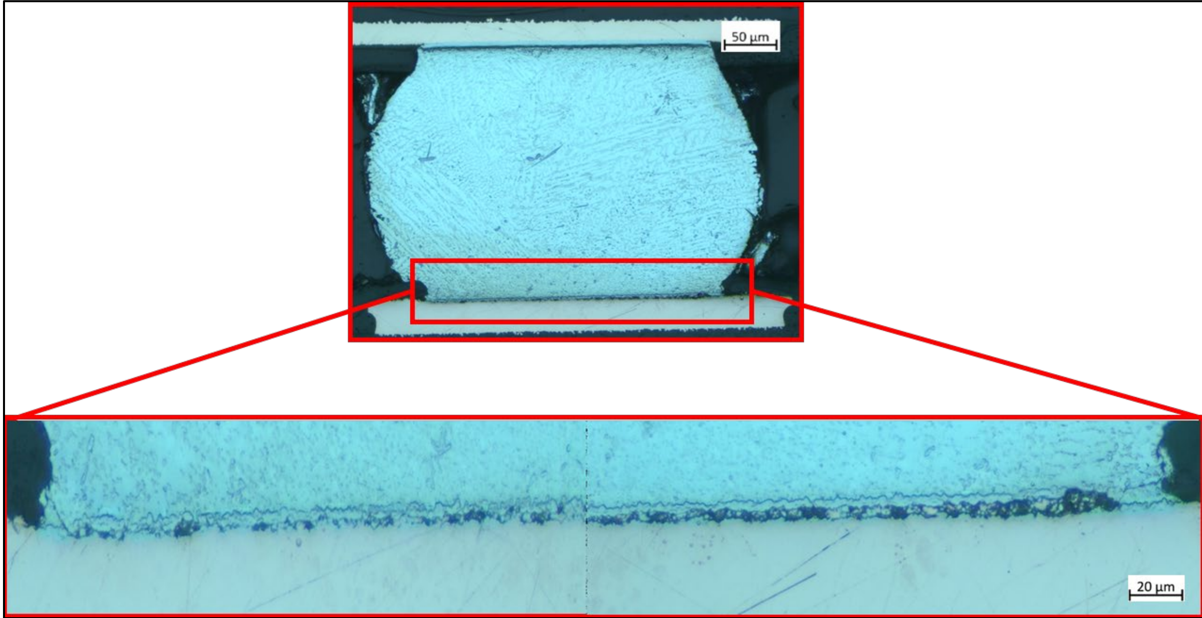

(c) SAC305 at 1500 G – mixed failure pattern



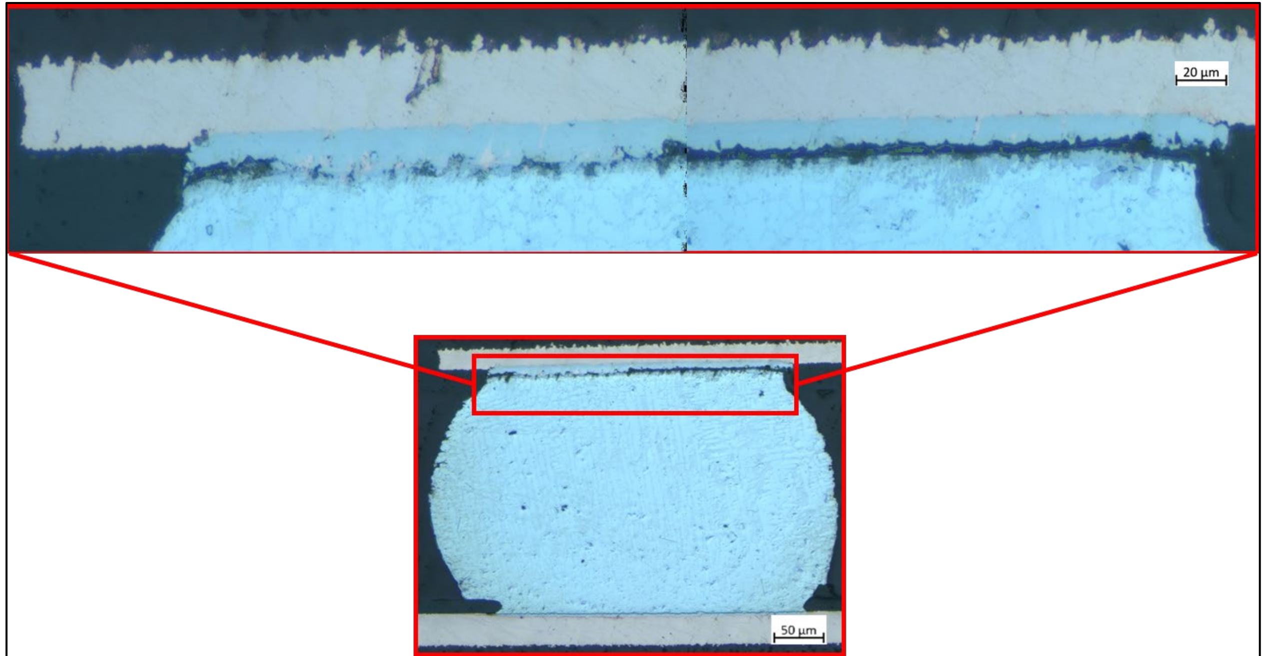

(d) SAC305 at 2000 G - mixed failure pattern




(e) SAC305 at 2000 G – mixed failure at board side and IMC layer failure at component side




(f) SAC305 at 2500 G - IMC layer failure

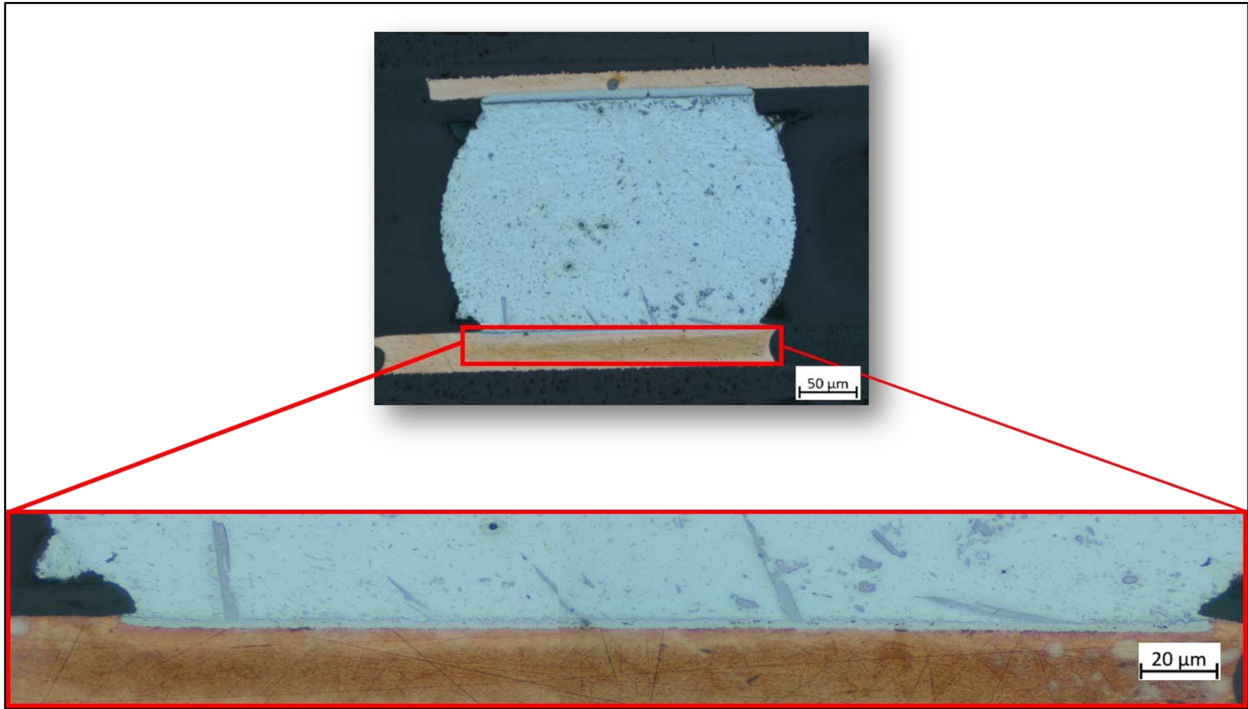



(g) SAC305 at 2500 G - IMC layer failure at component side

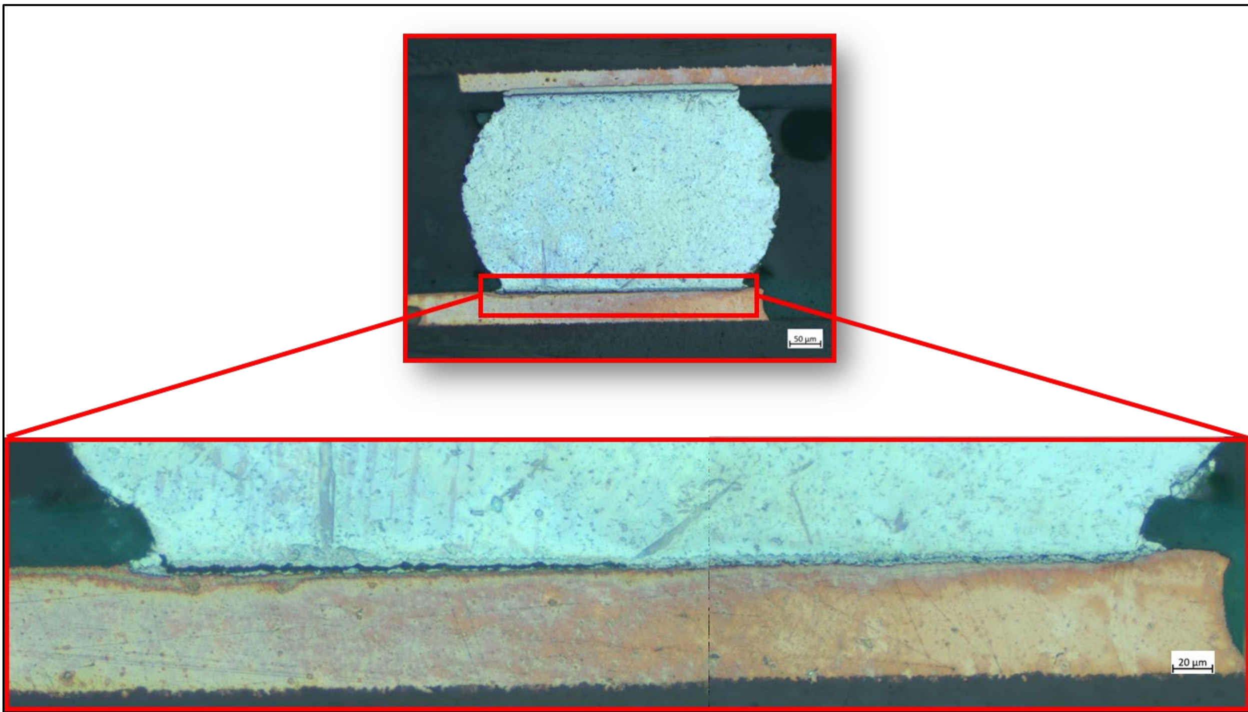
Figure 5.7 SAC305 solder joint microstructure after reflow and post failure for all G levels

### 5.5.3 Microstructure Analysis of Innolot

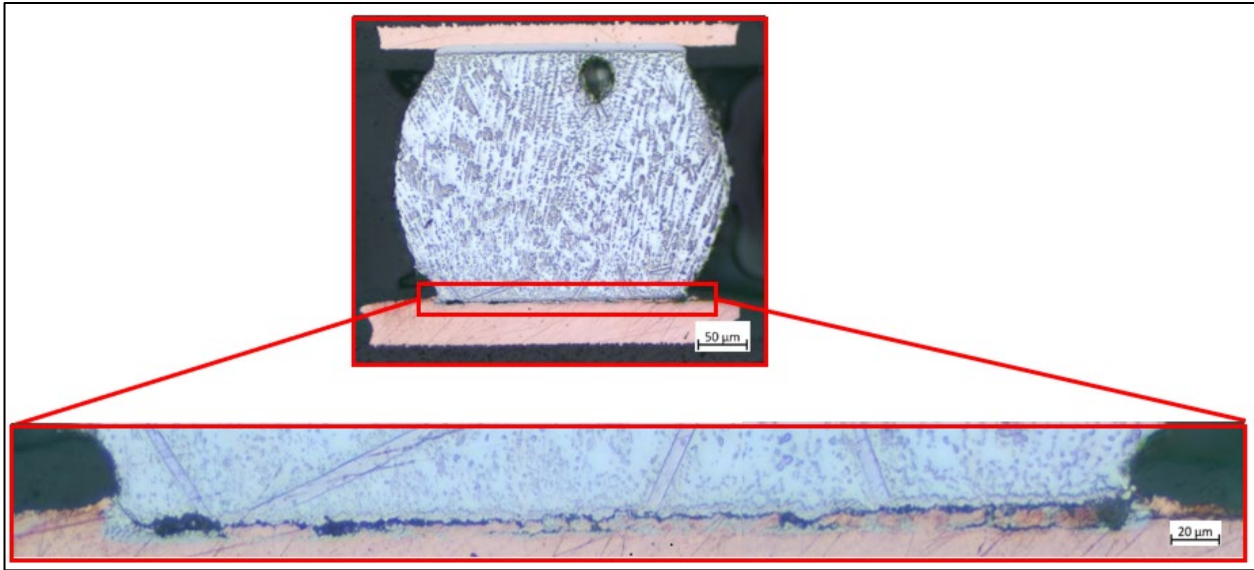
Below are the microscopy images for after reflow failed Innolot solder at 1500 G, 2000 G, 2500 G, and 3000 G acceleration. In all the cases, it was observed that the crack was in the IMC layer, indicating brittle failure mode. All the cracks were observed towards the board side.



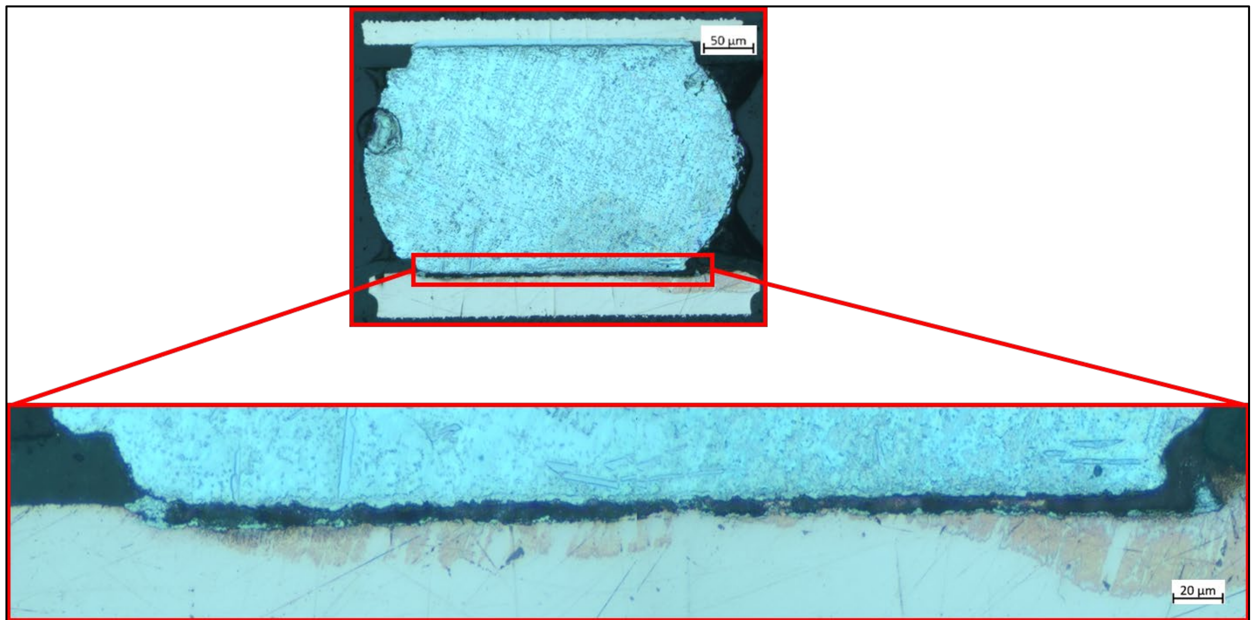

(a) Innolot solder joint after reflow



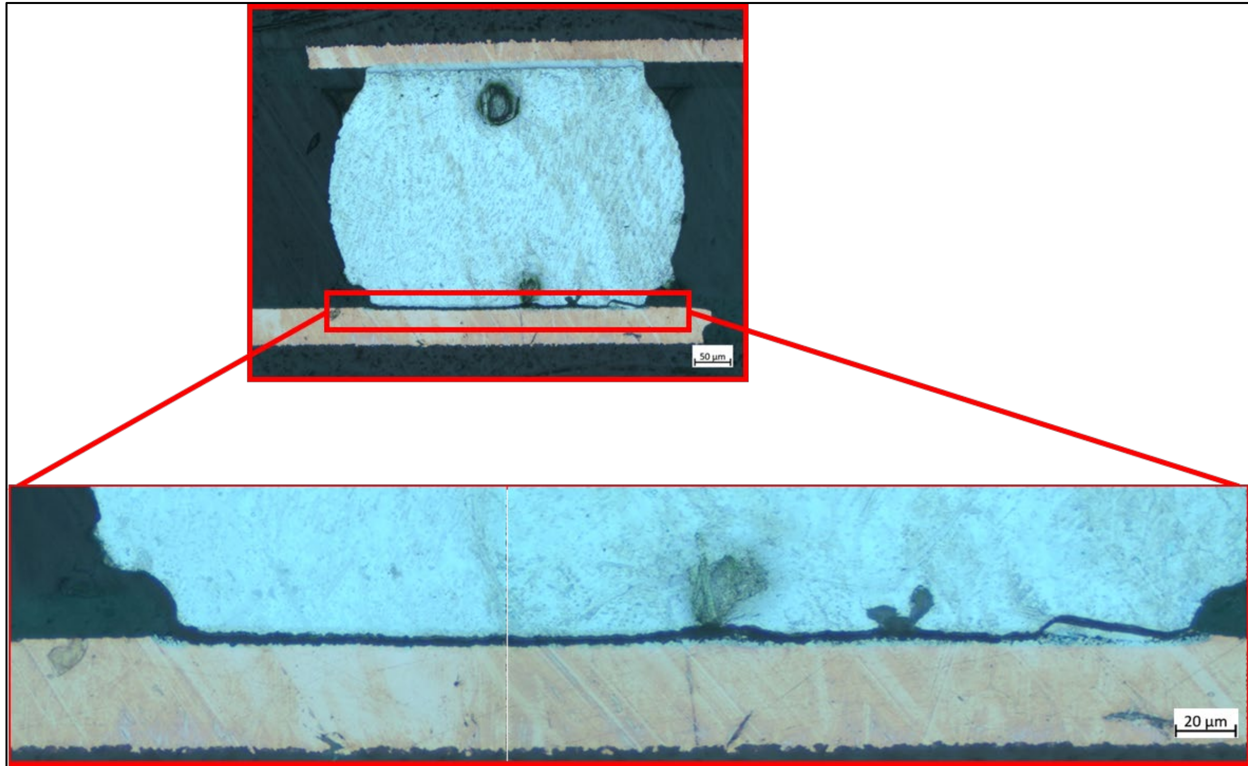

(b) Innolot at 1500 G - IMC layer failure




(c) Innolot at 2000 G - IMC layer failure




(d) Innolot at 2500 G - IMC layer failure

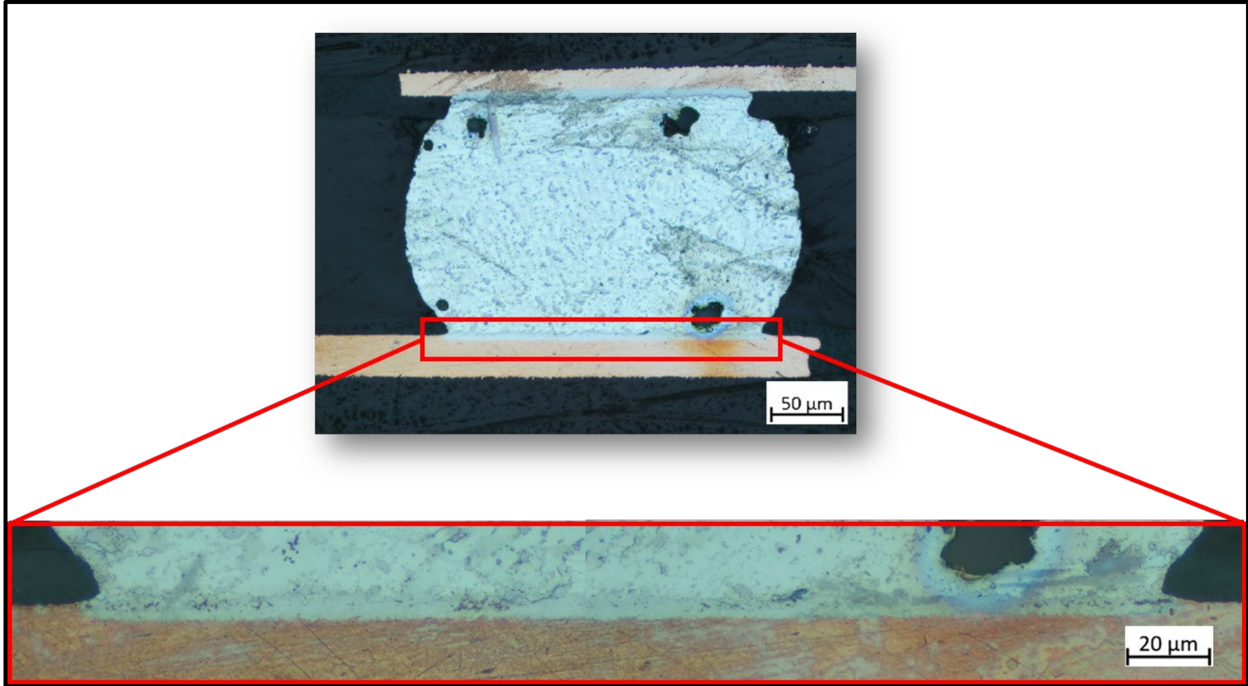



(e) Innolot at 3000 G - IMC layer failure

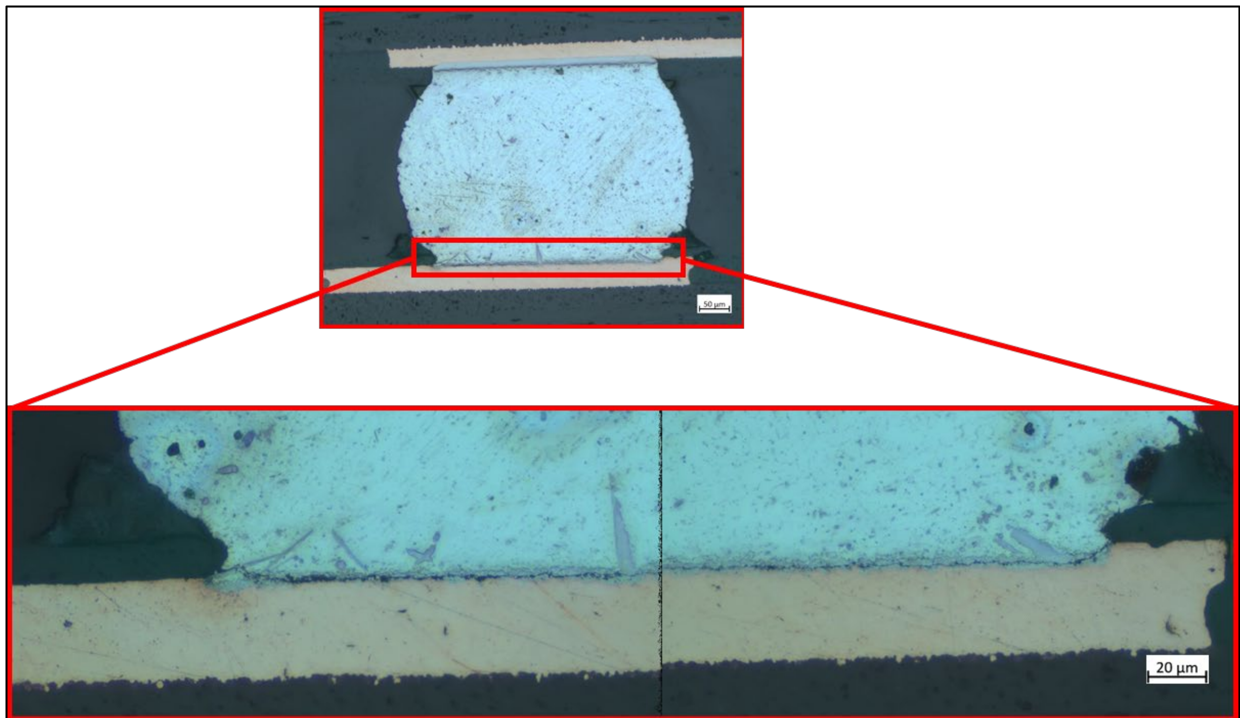
Figure 5.8 Innolot solder joint microstructure after reflow and post failure for all G levels

### 5.5.4 Microstructure Analysis of Cyclomax

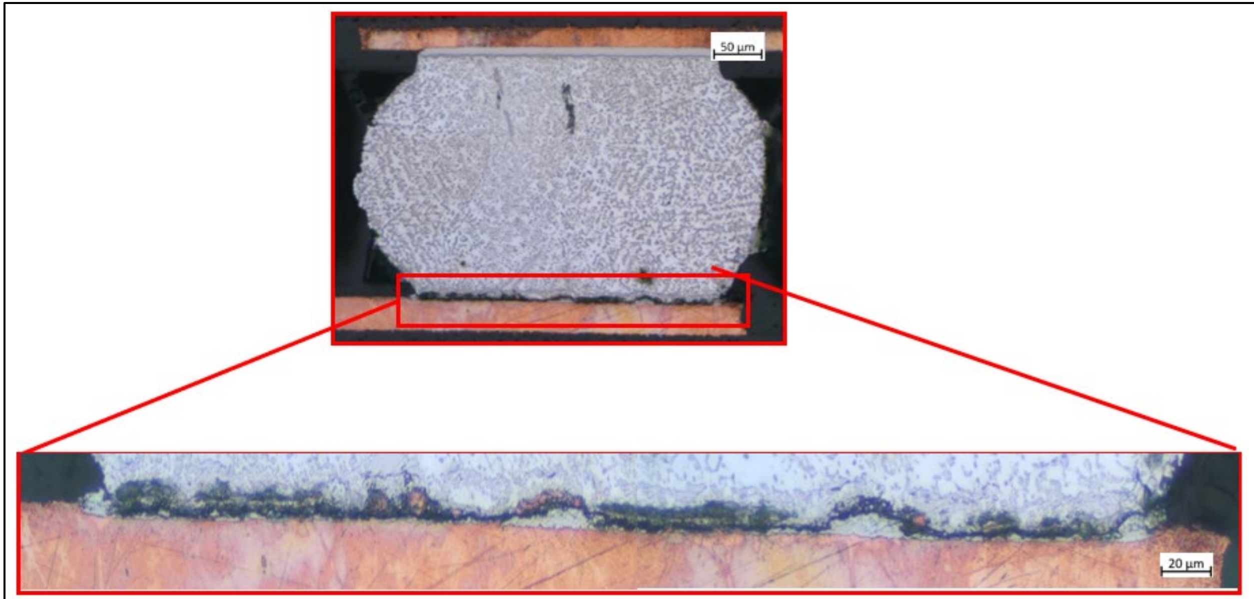
Below are the microscopy images for after reflow and failed Cyclomax (SAC-Q) solder at 1500 G, 2000 G, 2500 G, and 3000 G acceleration. In all the cases, it was observed that the crack was in the IMC layer, indicating brittle failure mode. All the cracks were observed towards the board side.



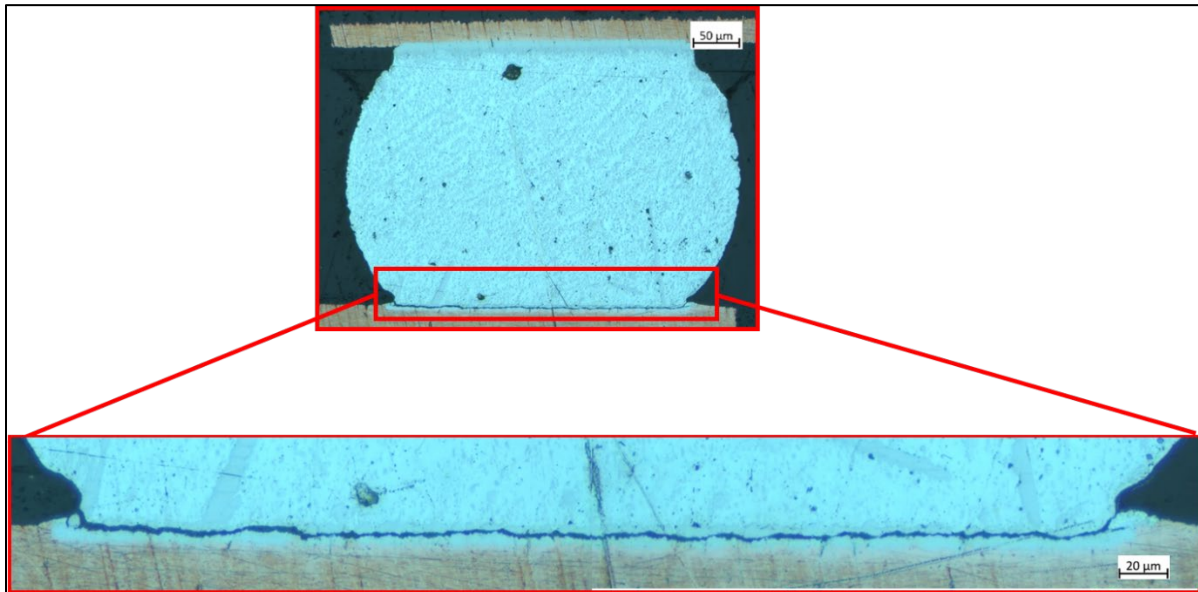

(a) Cyclomax solder joint after reflow



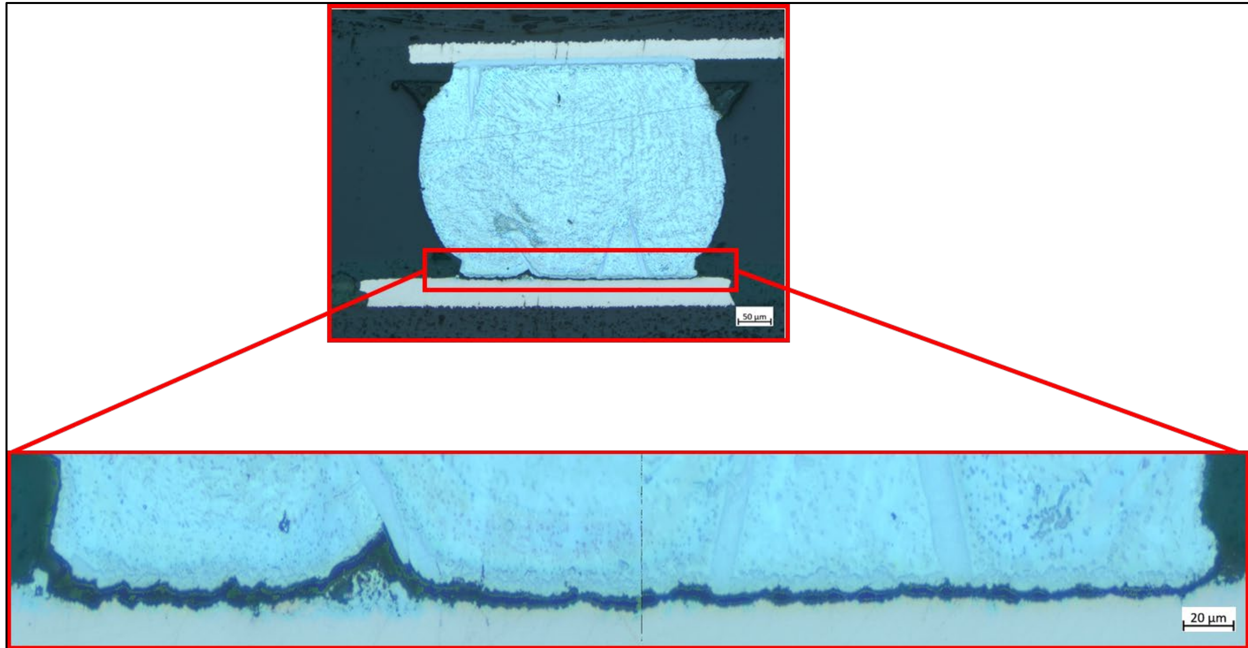

(b) Cyclomax at 1500 G - IMC layer failure




(c) Cyclomax at 2000 G - IMC layer failure




(d) Cyclomax at 2500 G - IMC layer failure

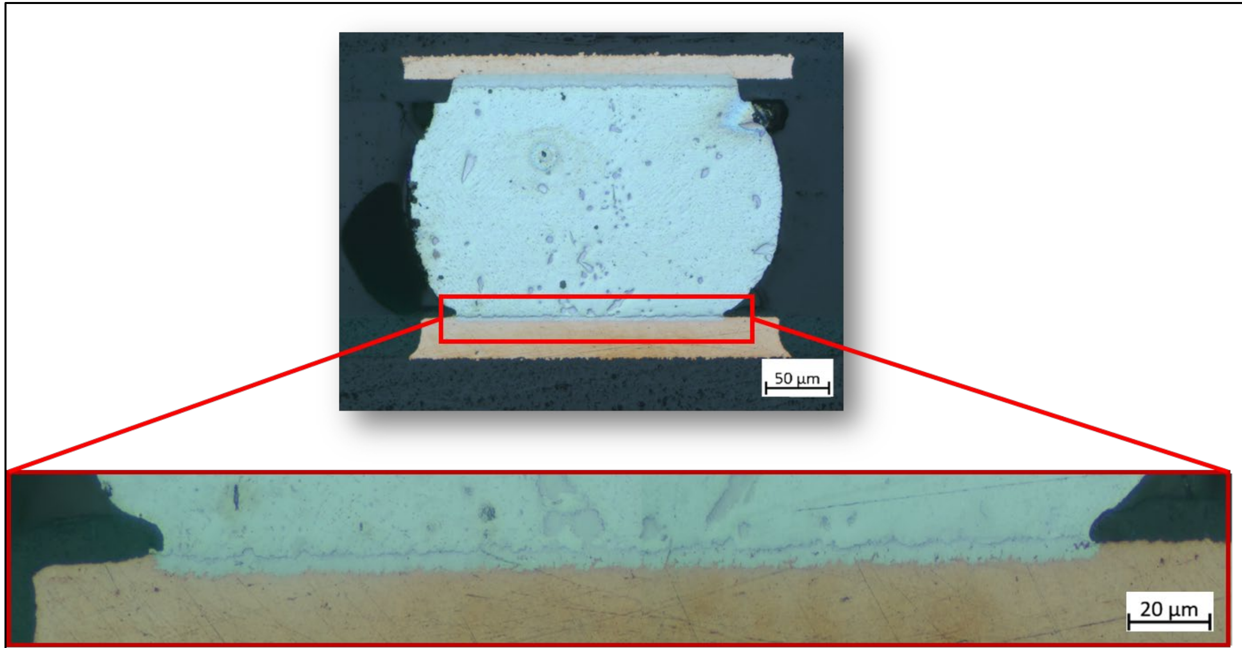



(e) Cyclomax at 3000 G - IMC layer failure

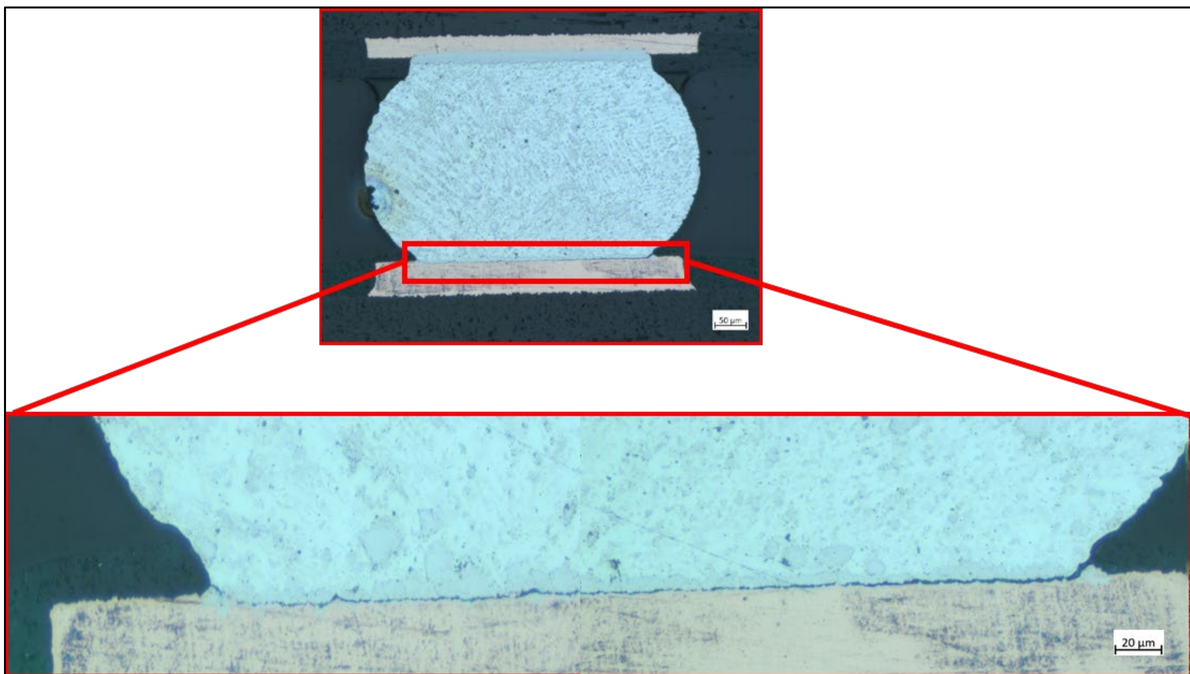
Figure 5.9 Cyclomax solder joint microstructure after reflow and post failure for all G levels

### 5.5.5 Microstructure Analysis of Sabix

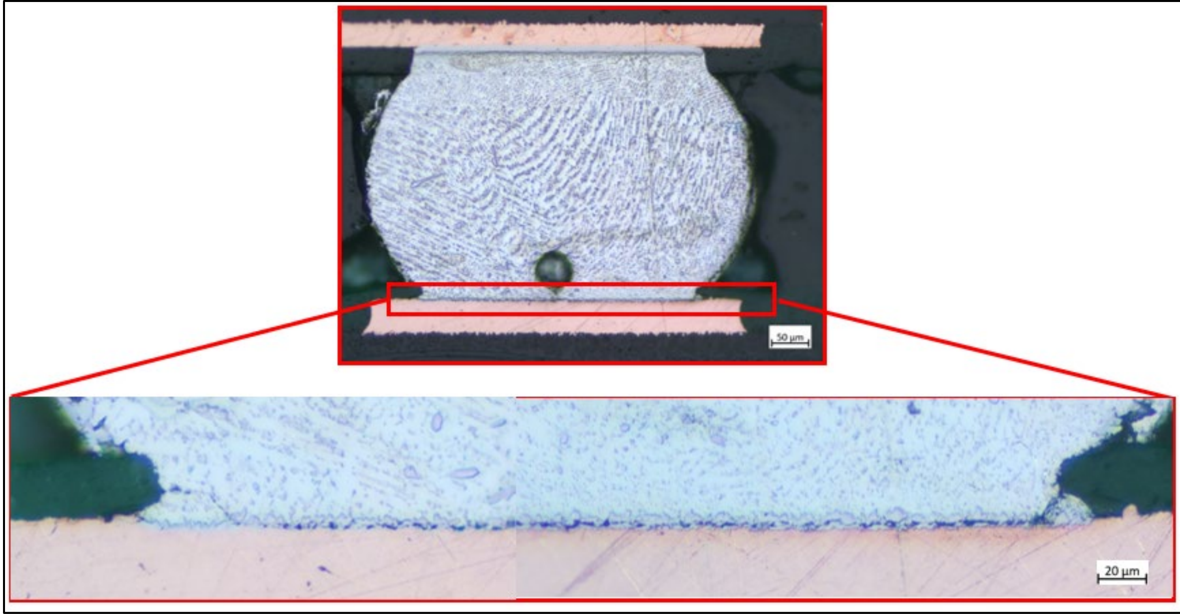
Below are the microscopy images for Sabix (SAC-In) after reflow and failed solder joints at 1500 G, 2000 G, 2500 G, and 3000 G acceleration. In both cases, it was observed that the crack is majorly in the IMC layer. The crack initiation can be claimed to start from the corner of the joint, slightly inside the solder bulk area near the interface. However, the crack penetrates the IMC interface for further propagation. It was also noted that the crack was towards the board side.



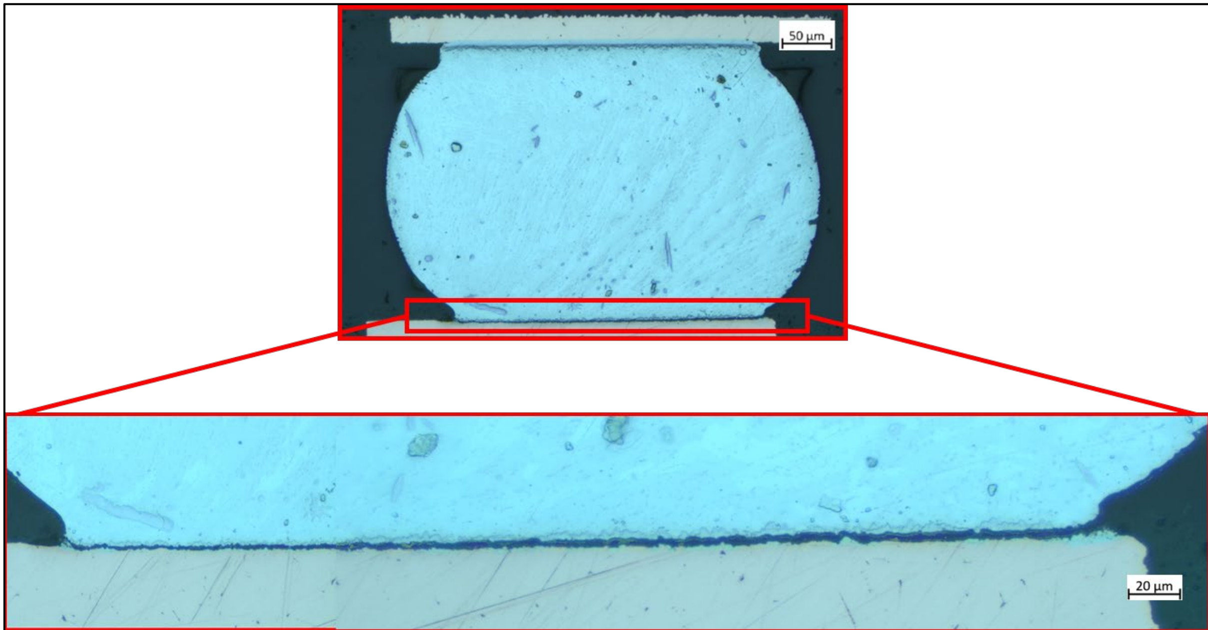

(a) Sabix solder joint after reflow



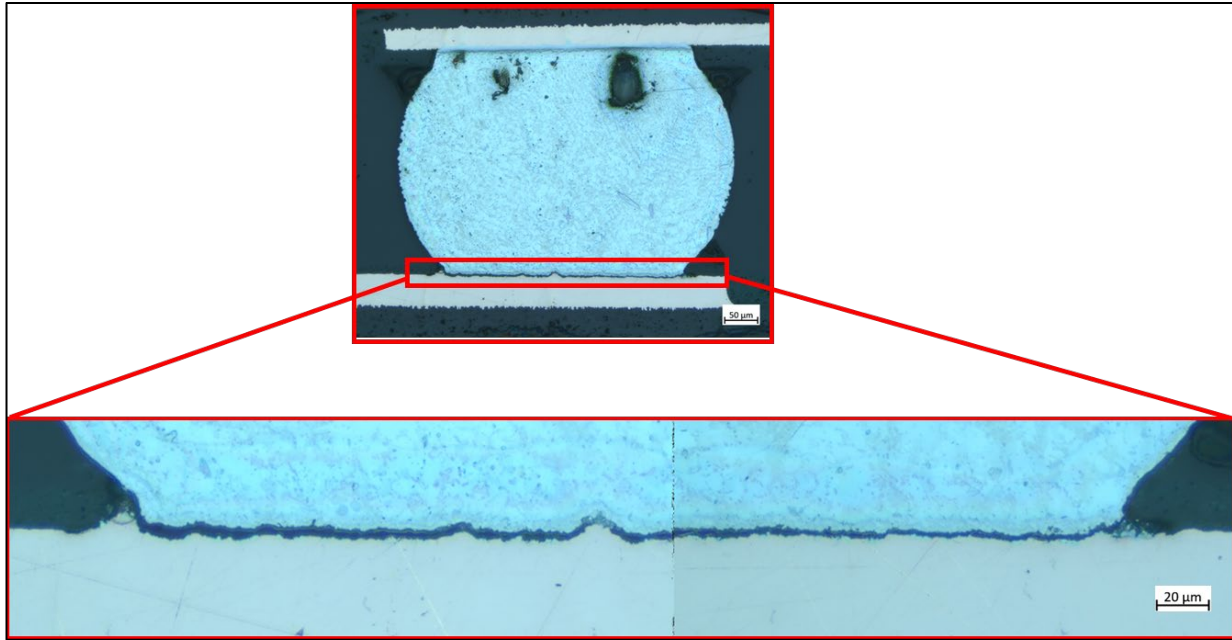

(b) Sabix at 1500 G - IMC layer failure




(c) Sabix at 1500 G - IMC layer failure




(d) Sabix at 2500 G - IMC layer failure




(e) Sabix at 3000 G - IMC layer failure

Figure 5.10 Sabix solder joint microstructure after reflow and post failure for all G levels

## 5.6 Hardness Test

The Vickers hardness test was conducted on all the alloys following the reflow process. Ten samples were tested for each alloy, and the obtained results are illustrated in Figure 5.11. Based on the results, SnPb exhibits the lowest hardness, followed by SAC305 and Sabix, while Innolot and Cyclomax show the highest hardness. A Pearson correlation analysis was conducted to examine the relationship between hardness and characteristic life. The findings revealed a strong positive correlation between the two variables at 1500G and 2000G, with correlation coefficients of 0.914 and 0.897, respectively. This indicates that as hardness increased, characteristic life also increased. The graphical representation of the relationship between characteristic life and hardness at 1500 G and 2000 G is depicted in Figure 5.12.

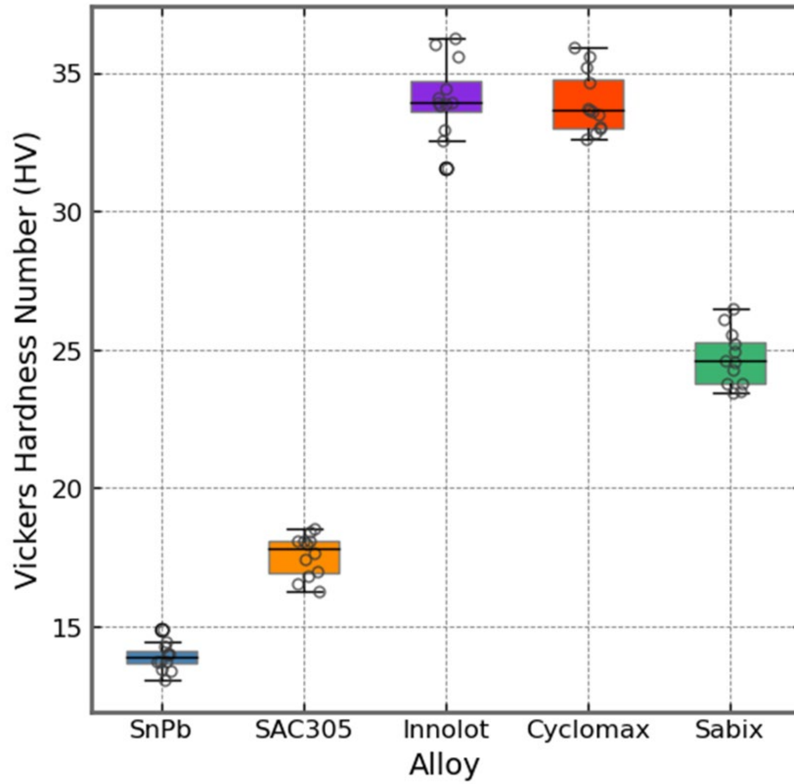



Figure 5.11 Hardness test for all the alloys. Each bubble represents a data point. The lower upper sides of the box represent 25th and 75th percentiles. The bars represent 10th and 90th percentiles.

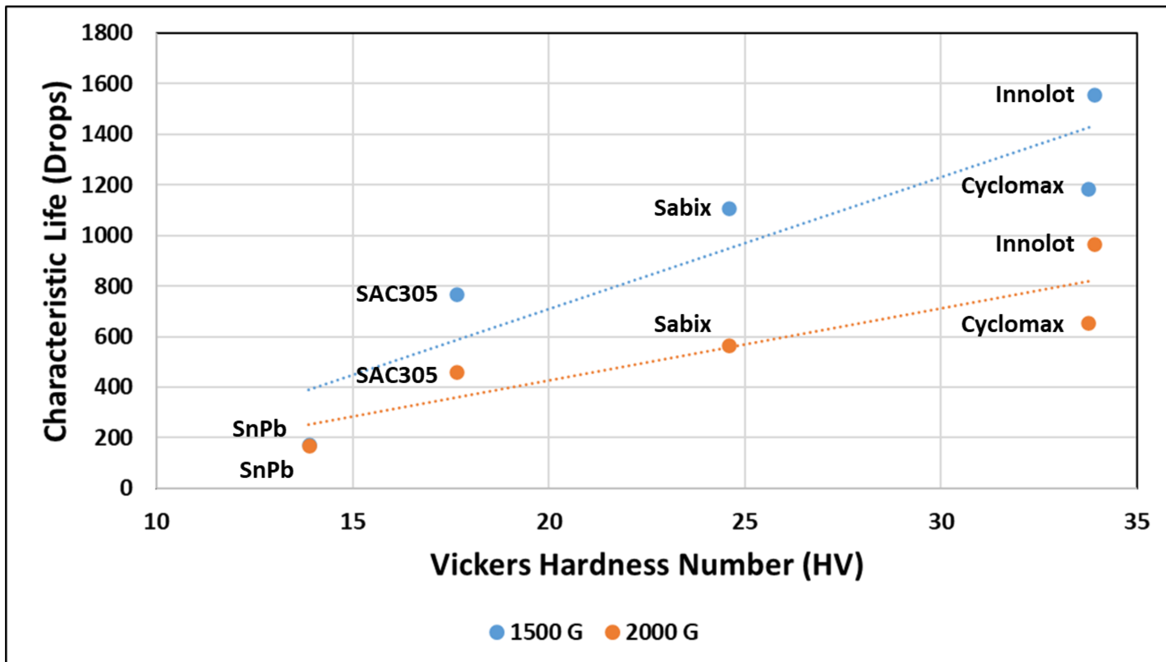



Figure 5.12 Characteristic life vs hardness correlation

### 5.7 Solder Joint Failure Mechanism

Solder joint failure mechanism was determined through the resistance data for failed solder joints. The resistance data was plotted to determine any patterns it would follow. From the plotted data, it was discovered that there are 4 phases to the resistance increase before the solder joint finally fails. These 4 phases are depicted in the figure below (Figure 5.13).

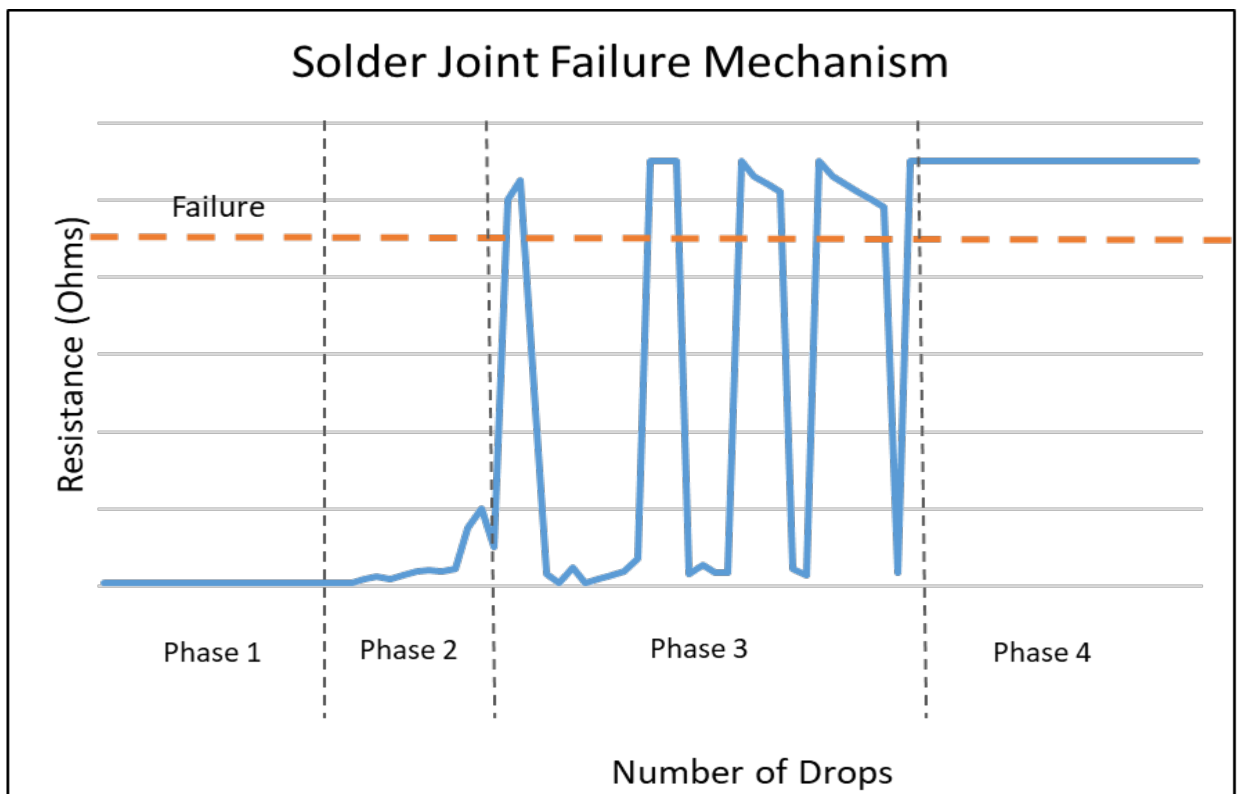



Figure 5.13 Solder joint failure mechanism

Phase 1: In this phase, the resistance at the solder joints remains almost constant and close to the initial value.

Phase 2: The resistance value increases, however, it stays below the threshold resistance, indicating crack initiation.

Phase 3: The resistance value reaches the threshold for a brief amount of time, which is a result of slow crack propagation, however, the resistance falls back, indicating the closure of cracks, this trend continues as the crack propagates through the joint.

Phase 4: The resistance reaches the failure zone and does not fall back, indicating a complete failure of the solder joint.

Below is a representative graph of resistance vs number of drops (Figure 5.14).

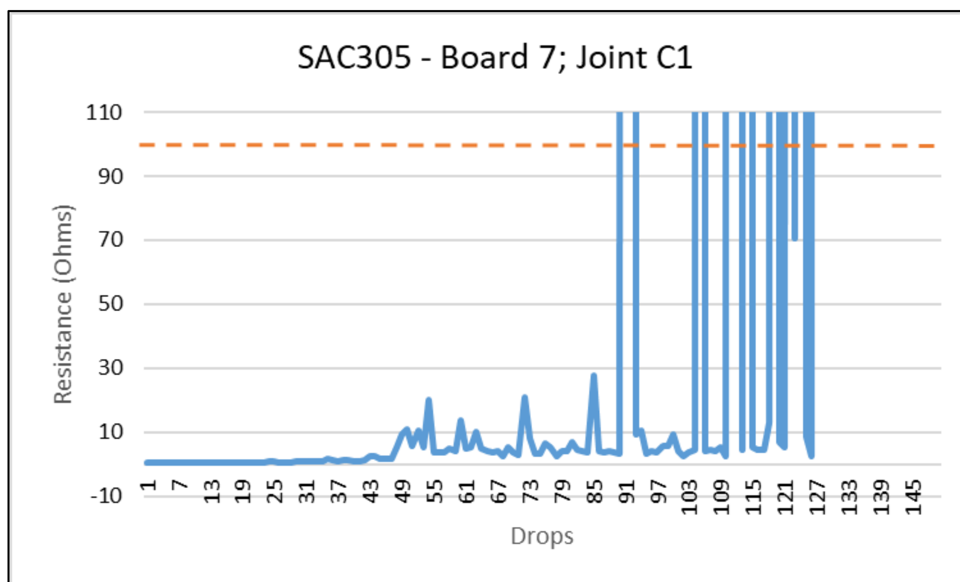



Figure 5.14 SAC305-Board 7, C1 Joint at 2500G

### 5.8 Conclusions

This study conducted a comprehensive examination of the drop shock performance of SnPb, SAC305, and SAC-Bi solder alloys with BGA assemblies and OSP surface finish. The study aimed to explore the influence of different input energies on the performance of these assemblies. Additionally, microstructure analysis was carried out to identify the failure modes for each alloy under various drop shock conditions. The results revealed that Innolot performed the best among

all alloys at 2000 G and below, followed by Cyclomax, Sabix, SAC305, and SnPb. At 2500 G, SAC305 outperformed all other alloys. The superior performance of SAC305 compared to SAC-Bi at higher G-levels can be attributed to SAC305 retaining some ductility, while SAC-Bi alloys become more brittle at higher strain rates (G-levels). As a result, SAC305 exhibits a higher toughness value, leading to an extended drop life. For all G-levels, crack propagation occurred in the bulk solder of SnPb, while in Innolot, Cyclomax, and Sabix, the crack propagation was observed in the IMC layer. For SAC305, crack propagation transitioned from bulk solder at 1000 G to mixed failure at 1500 and 2000 G, and finally to IMC failure at 2500 G. This can be attributed to SAC305 displaying higher ultimate tensile strength and higher elastic modulus at higher strain rates (or G-levels), leading to suppression of plastic deformation and promotion of brittle fracture. Finally, the hardness test results indicated a strong positive correlation between the hardness number and characteristic life at G-levels of 1500 and 2000 G. In forthcoming research, the potential of developing a predictive model for solder joints incorporated into PCBs with varying surface finishes under different G-levels will be explored. Furthermore, conducting drop shock tests at elevated temperatures could be pursued to assess how temperature affects the reliability of various solder joints.

# Chapter 6 Drop Shock Testing Analysis at Elevated Temperature: Assessing SAC305 Solder Alloy Reliability in BGA Assemblies

## 6.1 Introduction

During normal operation, electronic circuits encounter a range of loads, encompassing thermomechanical loads due to temperature variations and mechanical loads from shocks and vibrations. These concurrent loads can significantly impact circuit reliability [126], [127]. Thermomechanical effects manifest from the expansion and contraction of materials due to temperature changes Electronic circuits commonly comprise materials with differing coefficients of thermal expansion (CTE), leading to varying rates of expansion and contraction [128], [129]. This diversity induces stress in the solder interconnects that link circuit board components. Over time, this stress can cause fatigue and failure in these interconnects. In many applications, electronic circuits are subjected to combined exposure to both thermomechanical and mechanical loads. This combined exposure creates a synergistic effect, resulting in more severe damage than either load type would induce independently.

These studies illustrate that the substantial influence of temperature on the drop test reliability of electronic components. This impact is attributed to temperature's impact on the mechanical characteristics of solder interconnects and the materials within the electronic circuit. At higher temperatures, solder interconnects tend to exhibit decreased stiffness and increased ductility, rendering them more prone to failure upon impact. Furthermore, the thermal expansion and contraction in the electronic circuit generate stress, which can also contribute to failure.

Accordingly, the primary aim of this study is to determine the impact of temperature on the drop shock reliability of SAC305 solder alloy. Additionally, the study aims to develop a predictive

model for the drop shock life at elevated temperatures. This study introduces a novel technique of drop testing at elevated temperature through utilizing a heating chamber. This research provides valuable insights, enriching the understanding of the reliability and performance of solder alloys in BGA assemblies.

### 6.2 Test Matrix

The boards underwent testing across a range of temperatures: 25°C, 50°C, 75°C, and 100°C, with eight boards tested at each temperature. These test boards were assembled on CABGA components featuring OSP surface finish. The test matrix details are provided in Table 6.1. Testing adhered to JEDEC drop test standards B, with peak acceleration set at 1500G and a pulse width of 0.5ms.

Table 6.1 Test matrix

| Temperature (°C) | Number of SAC305 Boards |
| --- | --- |
| **25** | 8 |
| **50** | 8 |
| **75** | 8 |
| **100** | 8 |

### 6.2 Graphical Abstract

Figure 6.1 represents a concise overview of the PCB fabrication process, followed by drop testing and reliability assessment. After surface mount assembly, the PCB underwent a 24-hr preconditioning at 100°C. Following preconditioned, the boards were subjected to drop shock testing. After the completion of drop testing, failure data was analyzed using Weibull analysis.

Subsequently, the Arrhenius model was used to model drop life. Finally, failed samples were cross-sectioned, and microscopy analysis was conducted.

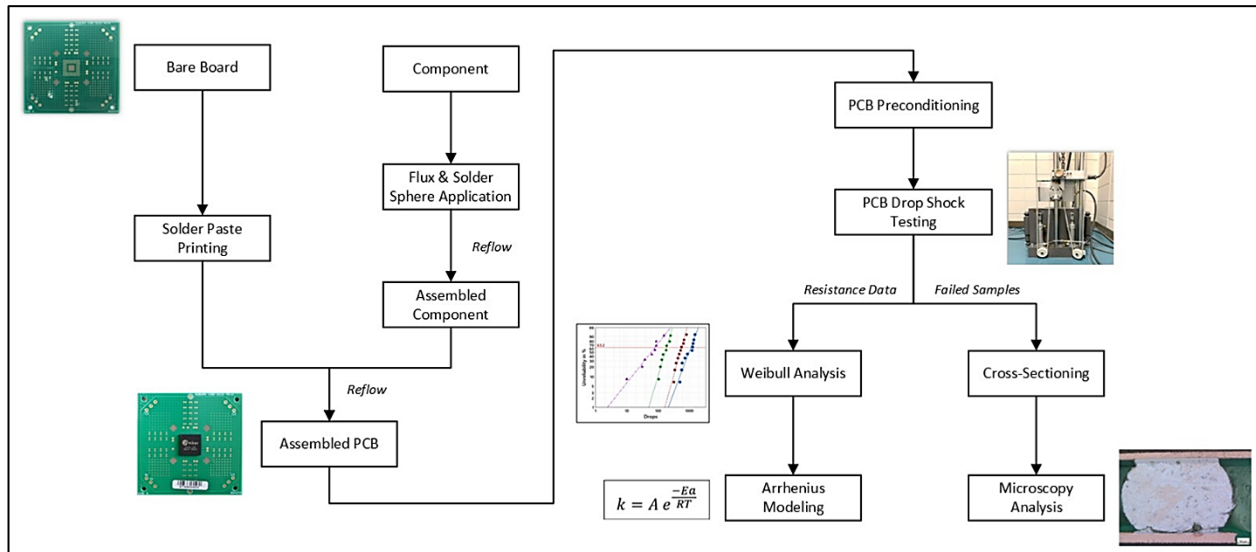



Figure 6.1 PCB Fabrication and reliability testing overview

## 6.3 Results and Discussion

The results of this study are detailed across three sub-sections: Weibull analysis, predictive modeling, and microstructure analysis. Each sub-section provides a comprehensive description of the findings and their implications.

### 6.3.1 Weibull Analysis

The failure data for all tested boards were examined using a 2-parameter Weibull distribution, as the boards were tested until complete failure. The 2-parameter Weibull model is depicted in equation 6.1, where α and β represent the scale and shape parameters, respectively.

$$R(t) = e^{-\left(\frac{t}{\alpha}\right)^{\beta}} \tag{6.1}$$

The shape parameter represents the slope of the regression line, while the scale parameter represents the number of drops at which 63.2% of the population is expected to fail. Additionally, early failure (β10) stands for the number of drops at which 10% of the population is expected to fail. To demonstrate the impact of testing temperature on solder joint reliability, probability plots were generated using fatigue life data at varying temperatures, as displayed in Figure 6.2. According to the Weibull analysis, SAC305 exhibits its best performance at room temperature (25°C). The characteristic life values display a significant reduction in solder joint reliability as the temperature increases. Similarly, the early failures or β10 life exhibited a comparable pattern, with SAC305 displaying optimal performance at room temperature and reduced performance at elevated temperatures °C. Figure 6.3, and Table 6.2 encapsulate the characteristic life and β10 life for SAC305 across all temperatures.

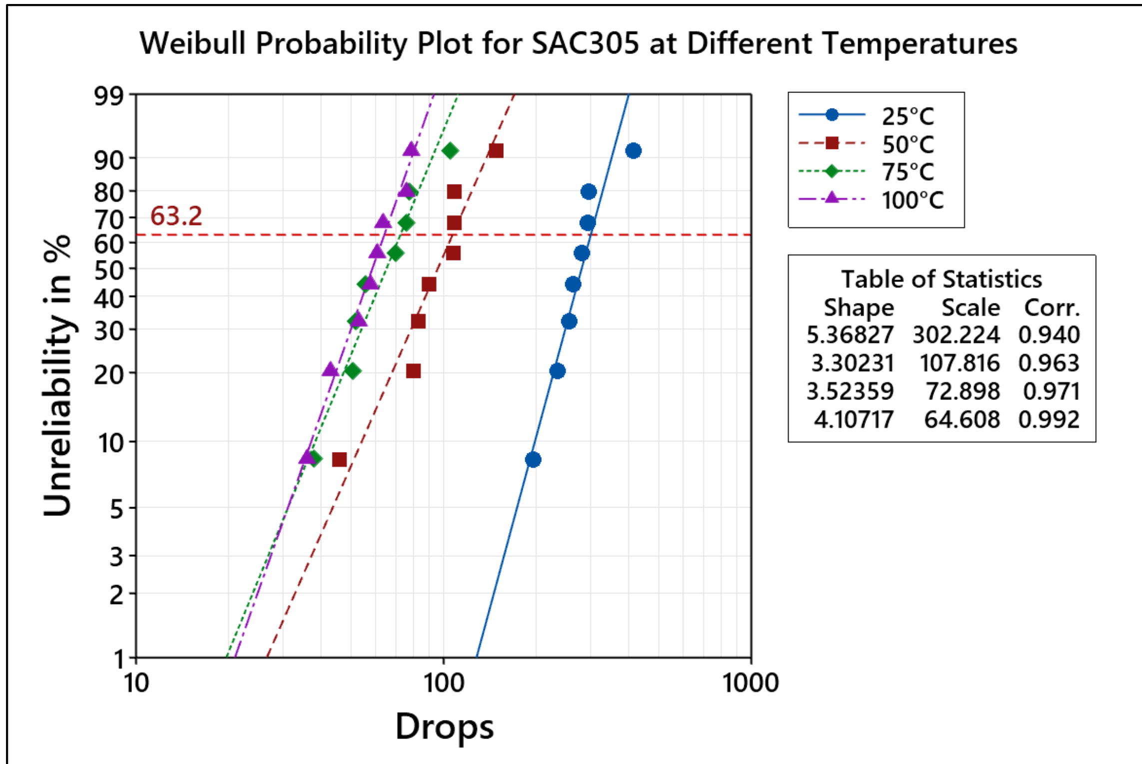



Figure 6.2 Weibull plots for all temperatures

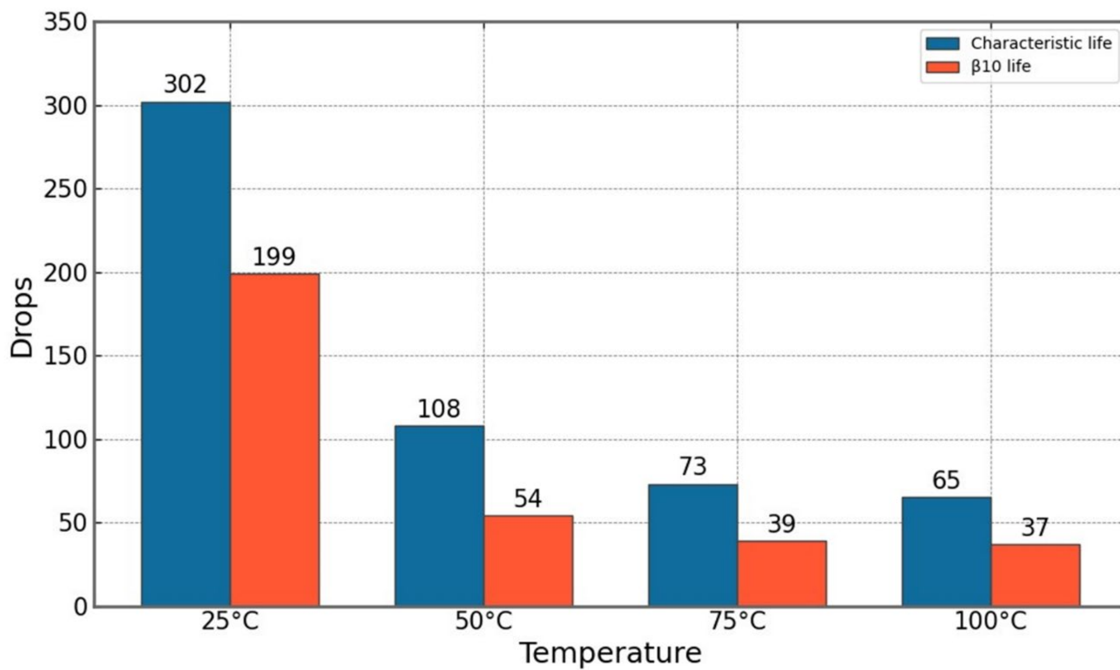



Figure 6.35 Characteristic life and β10 life for all temperatures

Table 6.2 Comprehensive Weibull analysis summary

| **Temperature** (°C) | **Characteristic Life** | **% Reduction** | **β10 Life** | **% Reduction** |
|---|---|---|---|---|
| 25 | 302 | - | 199 | - |
| 50 | 108 | 64.23 | 54 | 72.86 |
| 75 | 73 | 75.82 | 39 | 80.4 |
| 100 | 65 | 78.48 | 37 | 81.4 |

### 6.3.2 Predictive Modeling

The relationship between solder joint drop shock life and temperature was established using the Arrhenius model. The adoption of the Arrhenius model was based on its widespread application as a tool to assess fatigue life in correlation with temperature [130]. The Arrhenius equation is represented as follows:

$$k = A\, e^{\frac{Ea}{RT}} \tag{6.2}$$

Where, k represents the number of drops to failure, A is the pre-exponential coefficient, $E_a$ is the activation energy, R denotes the gas constant (8.314 J $\mathrm{mol}^{-1}$ $\mathrm{K}^{-1}$), and T signifies the testing temperature in Kelvin. The formula can be expressed as follows:

$$\ln(k) = \ln(A) + \frac{E_a}{RT} \tag{6.3}$$

The mathematical average of drops to failure at each temperature was computed and fitted to equation 6.3. Subsequently the constants $E_a$ and A were determined. The fitted plot, along with the fitted equation, is depicted in Figure 6.4. The resulting linear equation can be utilized to ascertain the characteristic life of SAC305 solder joints at any given temperature.

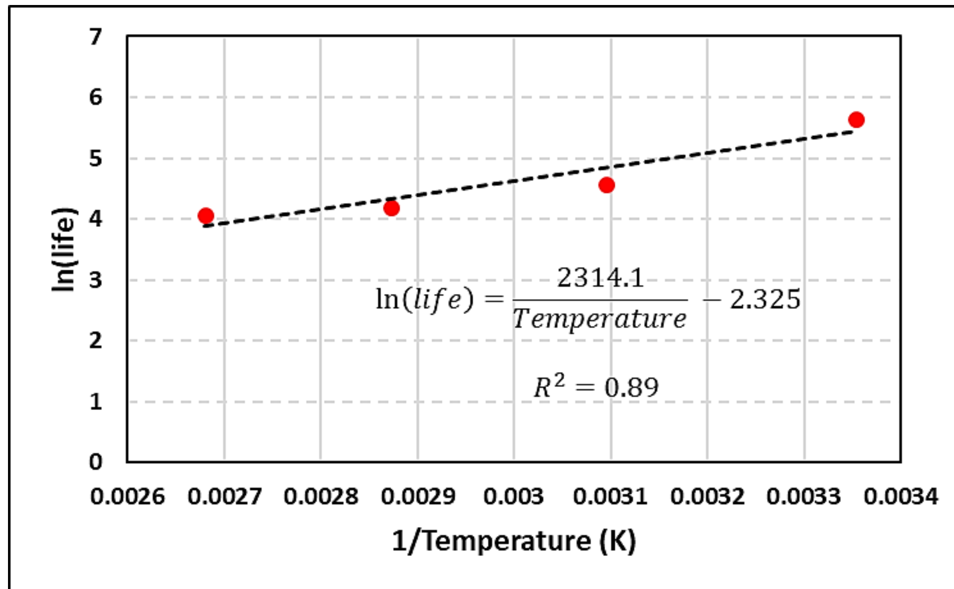



Figure 6.4 Arrhenius model fitting curve

The reliability of the model was confirmed by an R-squared value of 89%, denoting a strong fit. The constants derived from the equation are $E_a$ at 19.4 KJ mol$^{-1}$ and an approximate value of 0.0978 for A.

During a drop shock test, the PCB encounters rapid acceleration and deceleration, prompting vibrations within the board. The acceleration leads to the PCB flexing and transmits the impact to its components. As the PCB decelerates, the stored energy gets released, leading to vibrations in both the board and its components. The highest strain is observed in the corner joints of the component, leading to the fracture of the solder joint. The strain rates experienced by solder joints during drop tests are notably higher compared to thermal cycling, leading to increased yield strength of the solder material [127]. Therefore, the increased solder strength contributes to stresses exceeding the strength of the IMC layer, leading to its brittle fracture. In an elevated temperature environment, fluctuating temperatures affect strains and stresses in testing via three mechanisms: inducing thermally induced stresses, reducing the stiffness of the printed wiring board (PWB), and

diminishing both the yield strength and the elastic modulus of solder interconnections [131]. The decrease in solder strength at elevated temperatures enhances the chance of plastic deformation, resulting in ductile failure. Moreover, the increased strains on the PCB due to reduced stiffness at higher temperatures [132] contribute to the observed decline in reliability as temperature increases.

### 6.3.3 Microstructure Analysis

The main goal of this failure analysis was to examine the failure modes of solder joints at various temperatures. Probable interconnect failure modes in drop shock tests include: (i) IMC layer crack on the package side; (ii) IMC Layer crack on the board side; (iii) bulk solder crack on the package side; (iv) bulk solder crack on the board side; and finally (v) pad cratering. In the failure analysis process, the procedure starts with creating cross-sections of the failed samples. Microscopy is then utilized to capture images for examination and assessment of the failed joints. Afterward, the investigation identified failure modes associated with the reduced fatigue life. The observed failure modes encompass IMC layer failure, bulk solder failure, and mixed failure, visually represented in Figure 6.5.

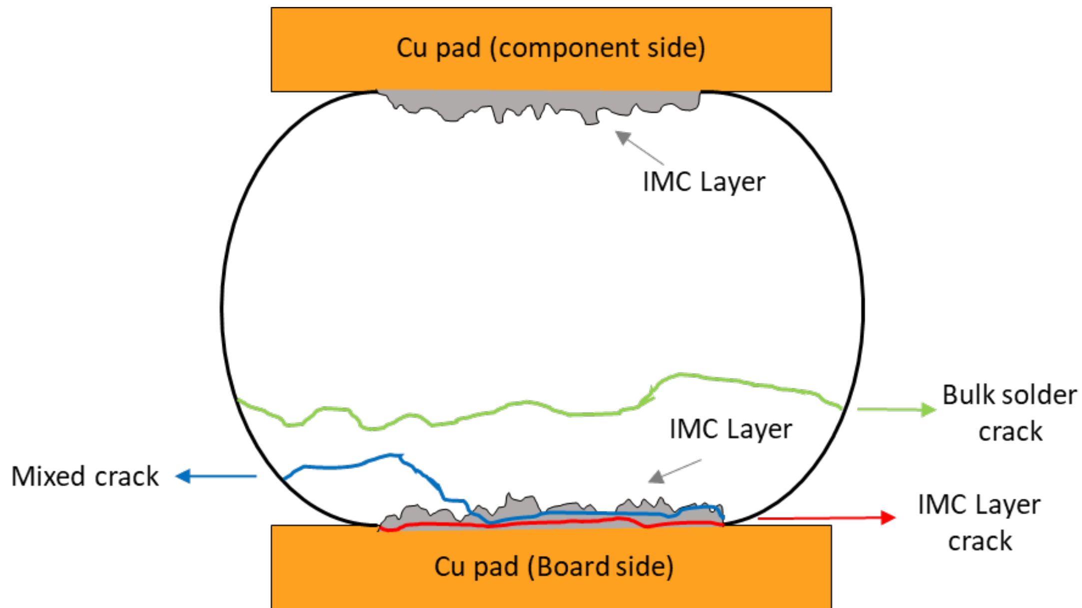
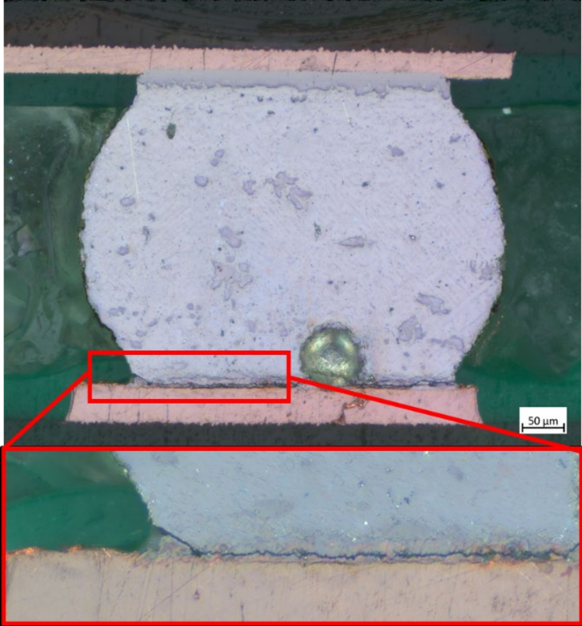



Figure 6.5 Summary of all observed failure modes

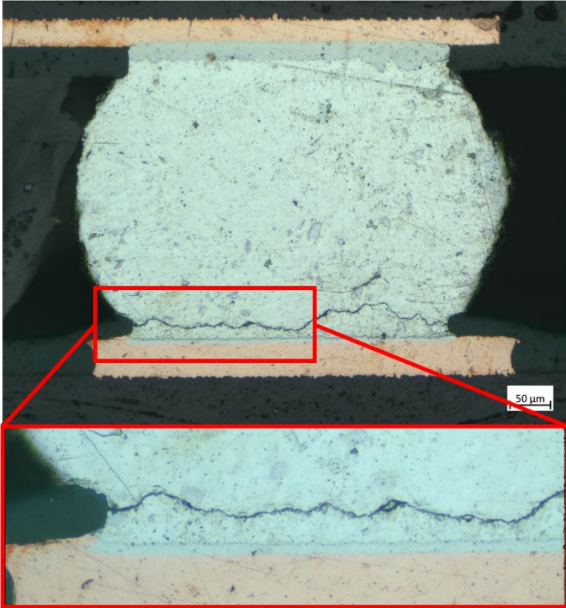
Cross-sectioning was performed on several samples to evaluate each condition. Figures 6.6(a)-(f) depict a visual illustration of SAC305 solder joint failures at different temperatures, showcasing varying crack behaviors with changing temperatures. At 25 °C, illustrated in Figure 6.6(a), a predominant IMC layer failure was observed. The cracks initially form in the bulk solder, then transition to the IMC layer, propagating through it. There were no instances of mixed or complete bulk failure modes observed at 25°C. In Figure 6.6(b), the visual representation highlights a brittle IMC layer failure at 50°C. There were no instances of mixed or complete bulk failure modes observed at 25°C and 50°C. However, when shifting to 75°C as seen in Figure 6.6(c) and (d), a mixed failure pattern emerges, presenting both bulk and IMC layer issues, where the bulk experiences ductile failure. Similarly, at 100°C as observed in Figures 6.6(e) and (f) mixed failures and bulk failures were majorly observed. Although a couple of complete IMC layer cracks were also observed at 75°C and 100°C. The shift observed in these failure modes is likely influenced by altered material properties due to the increase in temperature. As the temperature increases, the

transition from brittle to ductile failure can be attributed to the decrease in the elastic modulus and yield strength for the solder. Predominantly, cracks developed on the board side of the joint, except for a single instance at 25 °C where cracks were detected on the component side. This implies that the board side experiences higher stress levels during drop shock loading.

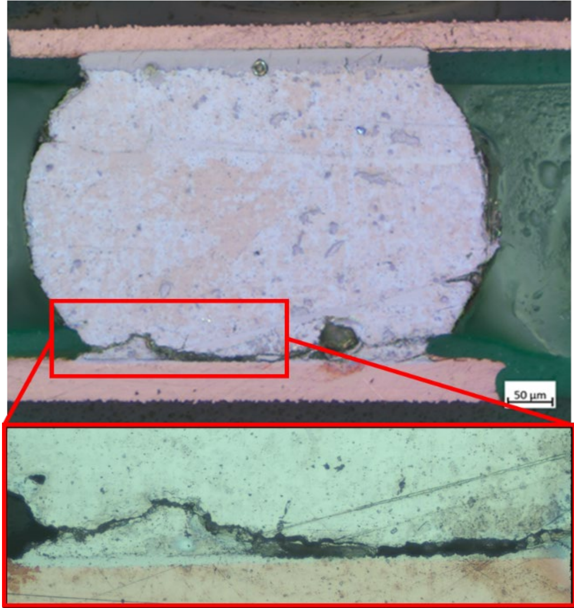
(a) 25°C- IMC layer failure



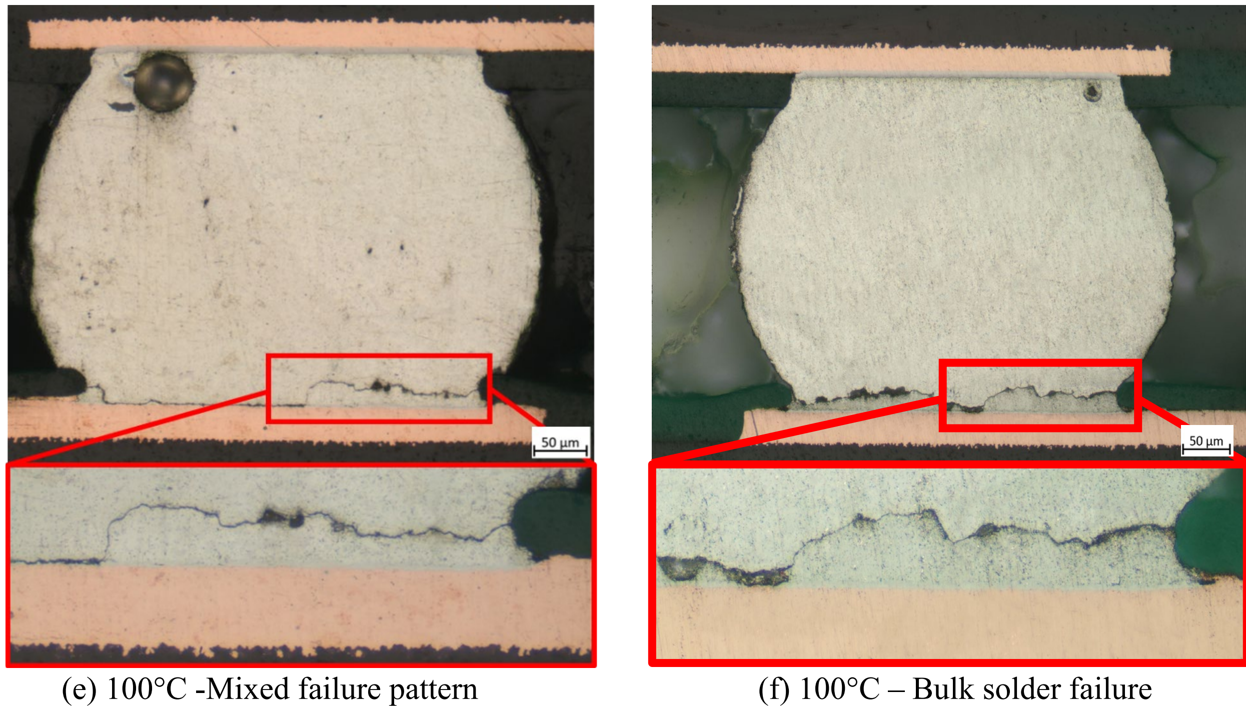

(b) 50°C – IMC layer failure




(c) 75°C – Bulk solder failure




(d) 75°C – Mixed failure pattern




(e) 100°C -Mixed failure pattern (f) 100°C – Bulk solder failure

Figure 6.6 Microstructure Analysis SAC305 solder joints at all temperatures: (a) 25°C- IMC layer failure, (b) 50°C – IMC layer failure, (c) 75°C – Bulk solder failure, (d) d) 75°C – Mixed failure pattern, (e) 100°C, Mixed failure pattern, and (f) 100°C – Bulk solder failure

### 6.4 Conclusions

This comprehensive study extensively investigated the drop shock performance of SAC305 solder alloy BGA assemblies alongside the OSP surface finish. The study involved subjecting SAC305 solder alloy in BGA assemblies to drop shock testing across various temperatures: 25°C (room temperature) and elevated temperatures: 50°C, 75°C, and 100°C. The findings indicated that SAC305 exhibited optimal performance at room temperature. However, as the temperature increased, the reliability of the solder joint notably declined, with characteristic life values decreasing to 108 drops at 50°C, 73 drops at 75°C, and further reducing 65 drops at 100°C. Furthermore, the β10 life showcased a similar trend, emphasizing a consistent reduction in

reliability with increasing temperatures. The Arrhenius model was utilized to construct a predictive relationship between solder joint drop shock life and temperature, offering a comprehensive grasp of the degraded reliability at elevated temperatures. The decrease in life can be attributed to reduced PCB stiffness and the diminished yield strength and elastic modulus of the solder alloy. Microstructure analysis highlighted that at lower temperatures (25°C and 50°C), the dominant failure mode was brittle, with cracks propagating through the IMC layer. As the temperature increased to 75°C and 100°C, the failure mode transitioned towards a more ductile form, with cracks propagating through both the bulk solder and the IMC layer (mixed) and even completely through the bulk. The transition in the failure mode can be attributed to changes in the material properties of the solder joint as the temperature increases. With increasing temperatures, the yield strength and elastic modulus of the solder decrease, causing the solder joint to become more ductile. Future studies could explore the impact of elevated temperatures on doped SAC-based alloys and further investigate the effect of surface finish on drop testing at increased temperatures. For future research, exploring the impact of elevated temperatures on doped SAC-based alloys could be beneficial. Additionally, investigating the influence of surface finish on drop testing at increased temperatures would be an area worth pursuing.

# Chapter 7 Drop Shock Test of SAC-Based Alloys at Elevated Temperature

## 7.1 Introduction

Portable and handheld electronic devices are frequently dropped, experiencing mechanical shock. Understanding how the solder joints perform under such stress helps ensure device reliability in real-world use. These devices often operate at an elevated temperature. Elevated temperatures can accelerate degradation processes, and understanding how solder alloys respond in different temperature environments is essential for predicting real-world performance. SAC305 and SACQ are common lead-free solders, with varying mechanical properties. Research has shown that SACQ displayed better fatigue resistance and improved aging resistance compared to SAC305 in various stress cycles. Firstly, the surface finish of a printed circuit board (PCB) can significantly impact its reliability under mechanical stress, such as drop and shock events. Research has shown that different surface finishes can influence the drop reliability of solder interconnects, making it essential to understand the specific performance of OSP and ENIG.

The study presented highlights the significant impact of temperature on the reliability of electronic components during drop tests. This influence is established to the temperature-induced changes in the mechanical properties of solder interconnects and the materials comprising the electronic circuit. Thus, the primary aim of this study is to determine the impact of temperature, and surface finish on the drop shock reliability of SAC305 and SACQ solder alloy.

## 7.2 Test Matrix

This study involved testing two solder alloys (SAC305 and SACQ) at two temperatures (25°C and 75°C) assembled with two Surface finishes (OSP and ENIG). Eight boards were tested at each test

condition, indicated in Table 7.1. The tests were performed at the peak acceleration of 1500 G and pulse with of 0.5 ms (half-sine) as per the JEDEC drop test condition B.

Table 7.1 Test Matrix

| Solder Alloy | Surface Finish | Temperature (°C) | #Boards |
|---|---|---|---|
| **SAC305** | OSP | 25 | 8 |
| | ENIG | 25 | 8 |
| | OSP | 75 | 8 |
| | ENIG | 75 | 8 |
| **SAC-Q** | OSP | 25 | 8 |
| | ENIG | 25 | 8 |
| | OSP | 75 | 8 |
| | ENIG | 75 | 8 |

### 7.3 Results and Discussion

The findings of this study are presented in three dedicated sections: Weibull analysis, ANOVA analysis, and microstructure analysis. Each section offers a detailed examination of the obtained results and their corresponding implications, providing a comprehensive understanding of the study outcomes.

#### 7.3.1 Weibull Analysis

The influence of testing temperature and surface finish on solder joint reliability was investigated through Weibull analysis of fatigue life data acquired at various temperatures. The results are visualized in the following Weibull probability plots.

Figure 7.1.1 depicts the Weibull probability plots for SAC305 alloy with OSP surface finish at 25°C and 75°C. The characteristics life reduced with an increase in temperature from 302 drops to 73 drops, a drop by 76%.

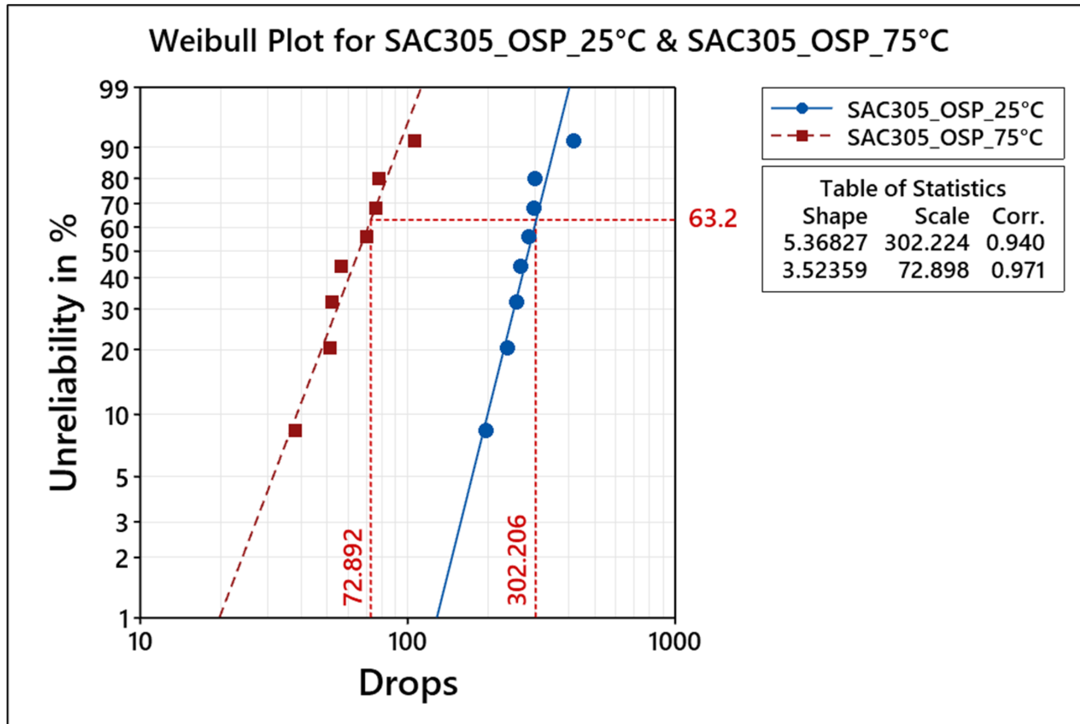



Figure 7.1.1 Weibull plot for SAC305 with OSP Surface finish at 25°C and 75°C. Each data point represents the number of drops to failure for each test vehicle. Scale parameter represents 63.2% of failures and shape parameter represents the slope of the fitted plot.

Figure 7.1.2 depicts the Weibull probability plots for SACQ alloy with OSP surface finish at 25°C and 75°C. The characteristics life reduced with an increase in temperature from 600 drops to 345 drops, a reduction by 43%.

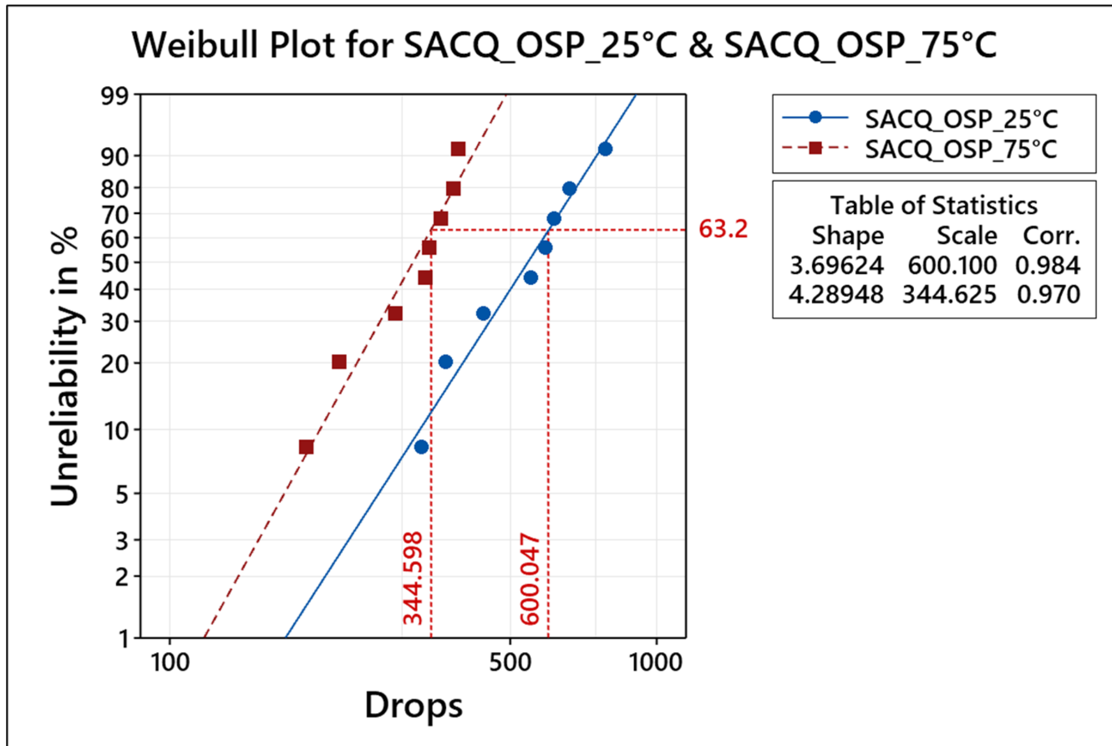



Figure 7.1.2 Weibull plot for SACQ with OSP Surface finish at 25°C and 75°C

Figure 7.1.3 depicts the Weibull probability plots for SAC305 alloy with ENIG surface finish at 25°C and 75°C. The characteristics life reduced with an increase in temperature from 180 drops to 42 drops, a reduction by 77%.

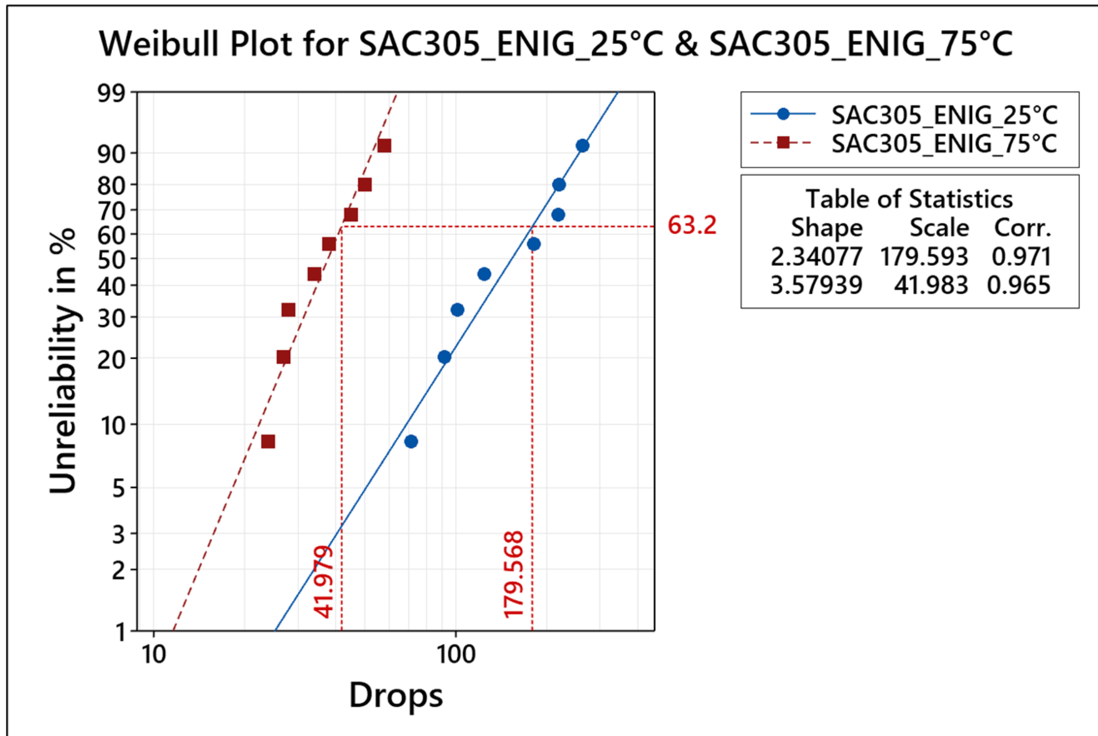



Figure 7.1.3 Weibull plot for SAC305 with ENIG Surface finish at 25°C and 75°C

Figure 7.1.4 depicts the Weibull probability plots for SACQ alloy with OSP surface finish at 25°C and 75°C. The characteristics life reduced with an increase in temperature from 130 drops to 53 drops, a drop by 60%.

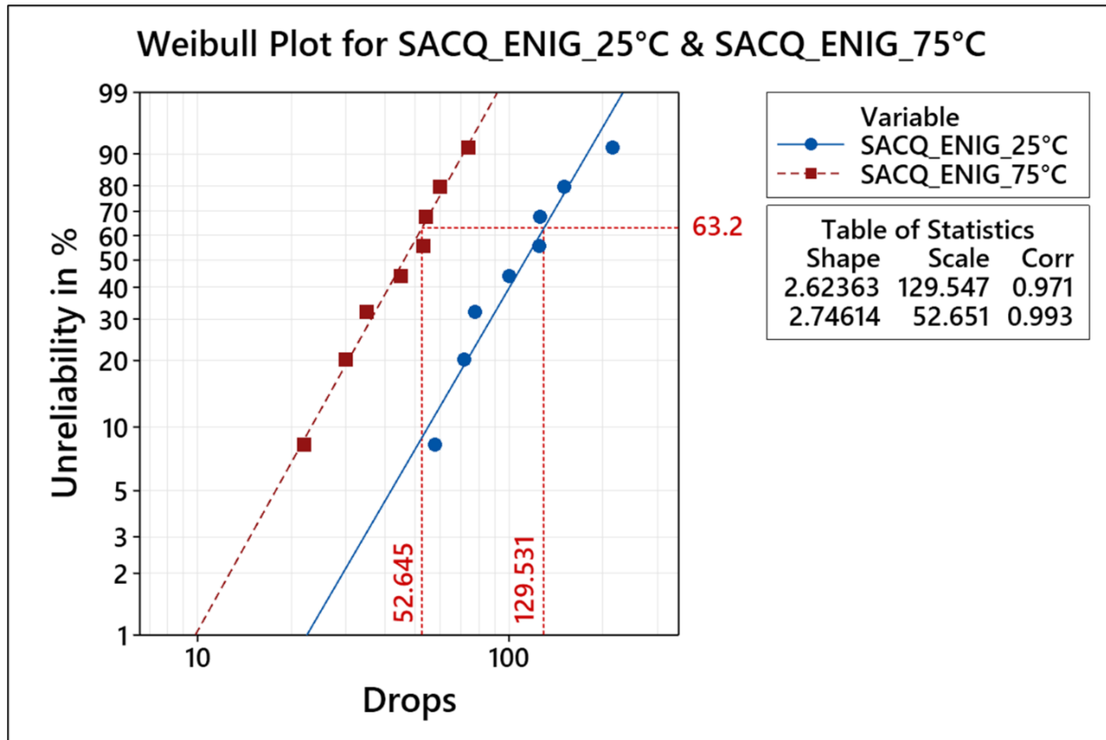



Figure 7.1.4 Weibull plot for SACQ with ENIG Surface finish at 25°C and 75°C

Figure 7.1.5 depicts the combined Weibull plot for all the conditions. Likewise, Figure 7.2, Figure 7.3 and Table 7.2 summarize the characteristic life and B10 life across all conditions. It can be observed that the decrease in characteristic life was more pronounced for SAC305 where the decrease was 76% and 77% for OSP and ENIG surface finish respectively with increase in temperature. Whereas for SACQ the decrease was 43% and 60% for OSP and ENIG surface finish respectively with increase in temperature.

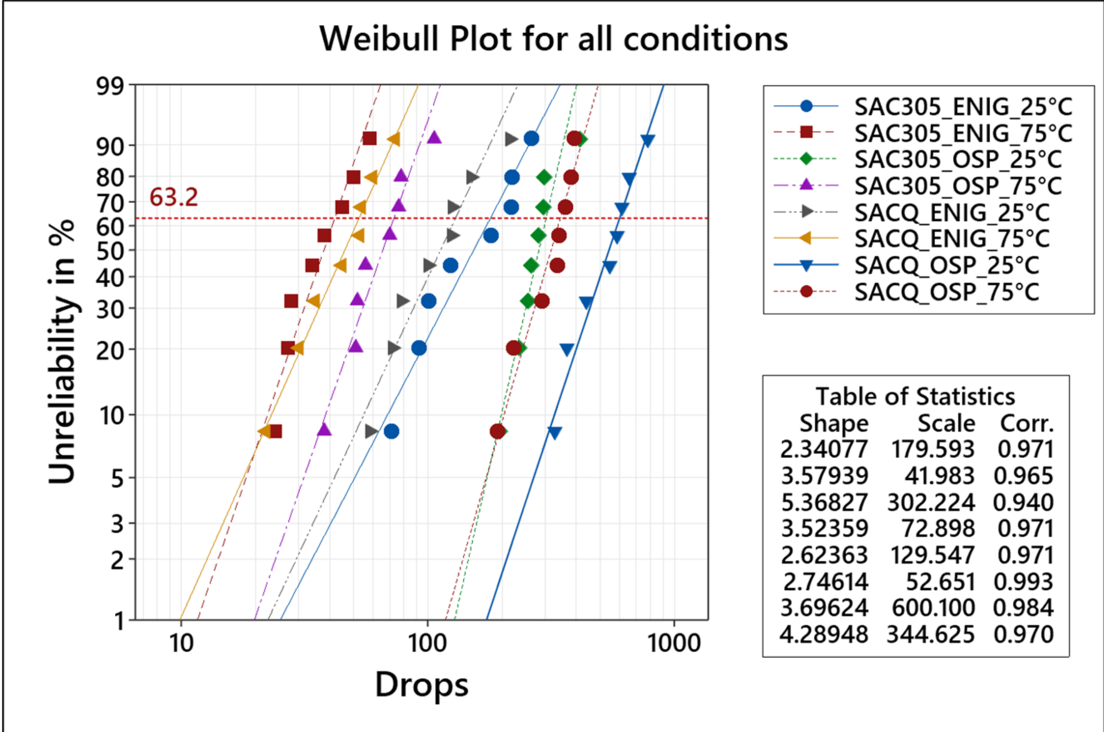



Figure 7.1.5 Weibull plot for all conditions

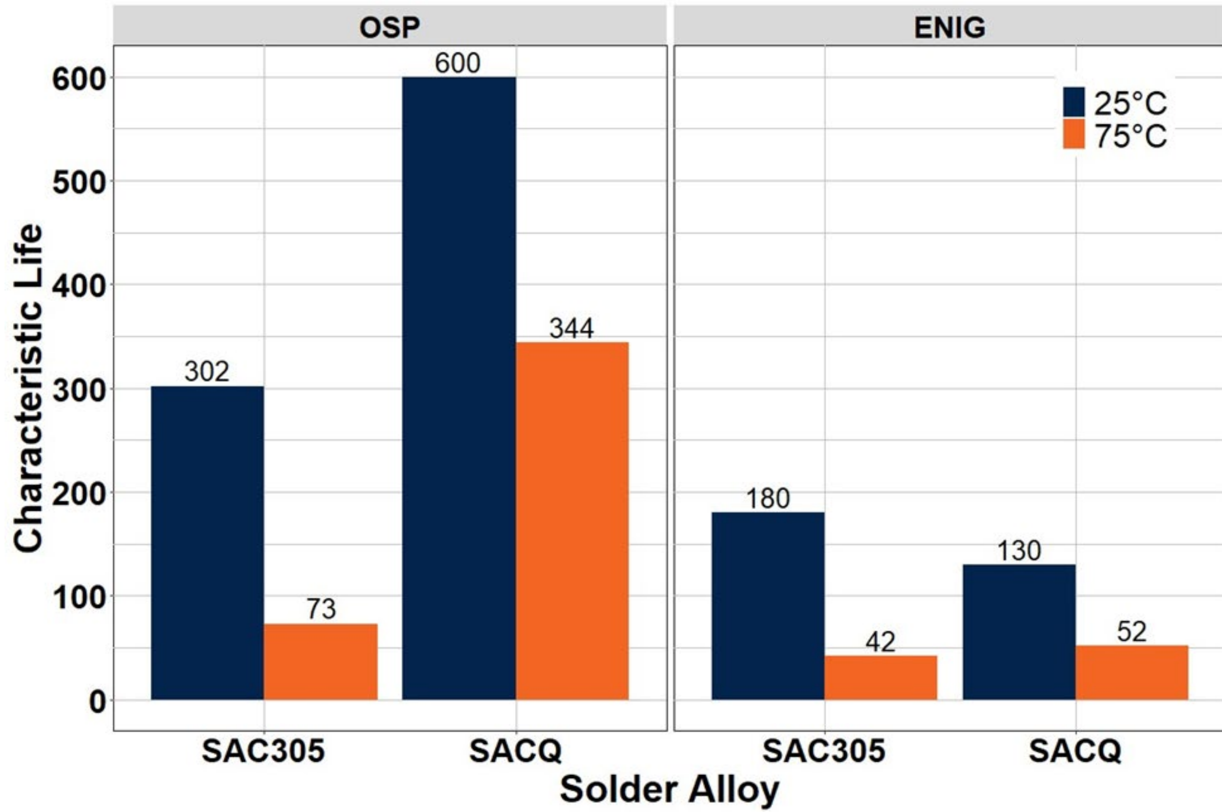



Figure 7.2 Characteristic life for all conditions. SACQ in general exhibited a higher drop shock life compared to SAC305 except for one case at 25°C and ENIG surface finish where SAC305 outperformed SACQ.

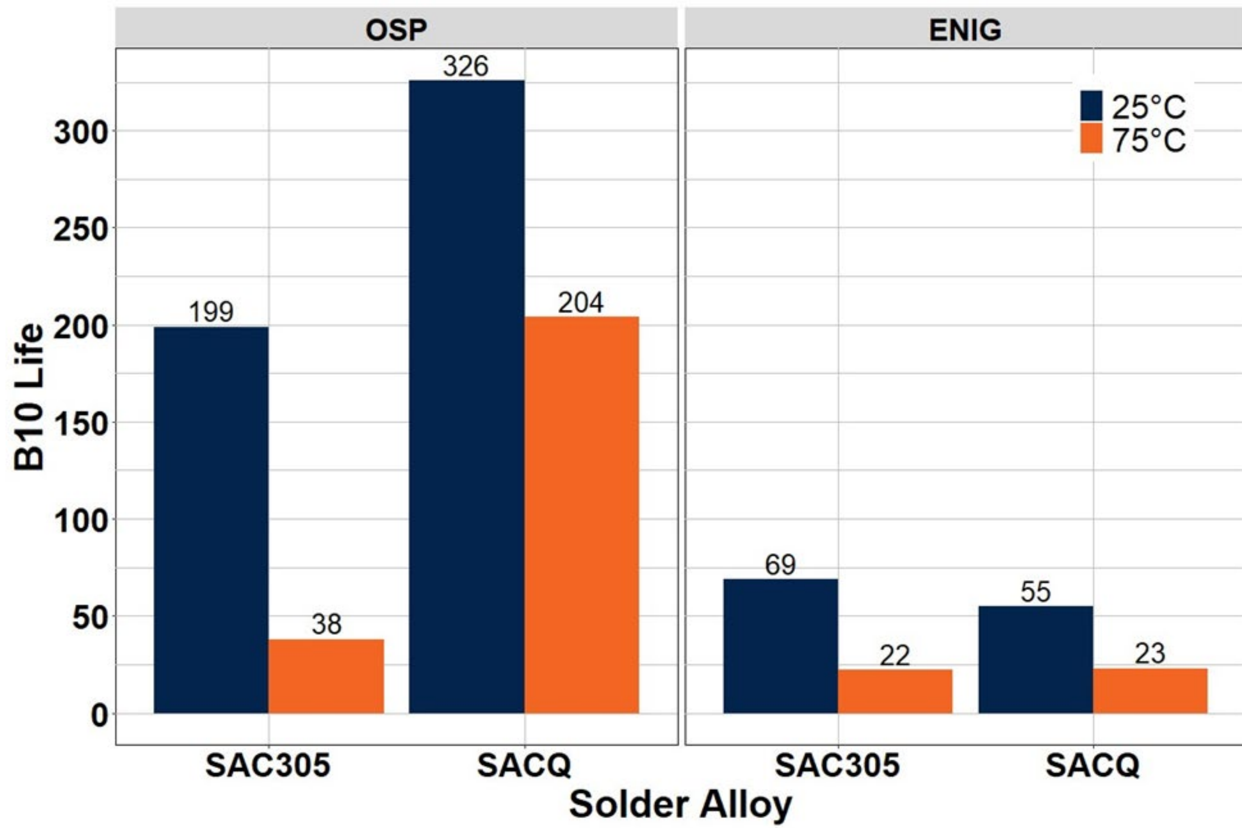



Figure 7.3 B10 life for all conditions

Table 7.2 Comprehensive Weibull analysis summary

| Solder Alloy | Surface Finish | Temperature (°C) | Characteristic Life ($N_{63}$) | % Reduction | B10 Life | % Reduction |
|---|---|---|---|---|---|---|
| **SAC305** | OSP | 25 | 302 | - | 199 | - |
| | | 75 | 73 | 75.83 | 38 | 80.90 |
| | ENIG | 25 | 180 | - | 69 | - |
| | | 75 | 42 | 76.67 | 22 | 68.12 |
| **SACQ** | OSP | 25 | 600 | - | 326 | - |
| | | 75 | 344 | 42.67 | 204 | 37.42 |
| | ENIG | 25 | 130 | - | 55 | - |
| | | 75 | 52 | 60 | 23 | 58.18 |

### 7.3.2 ANOVA Analysis

ANOVA was performed to quantify the contribution of each experimental factor on the life of the solder joints (cycles to failure). All statistical analyses in this study were performed using MINITAB 20 with a 95% confidence level. Table 7.3 represents the ANOVA of the response (drops to failure). Based on the ANOVA results, all main effect variables showed statistically significant effects, with p-values below 0.005. Specifically, the solder alloy, surface finish material, and temperature variables exhibited significant effects. Additionally, we conducted 2-way and 3-way ANOVA analyses to explore potential interactions among the experimental variables. The interaction between solder alloy and surface finish was found to be significant based on the p-value. Furthermore, the interaction between surface finish and temperature was also found

to be significant. However, the 3-way interaction involving all variables was not found to be statistically significant.

Table 7.3 Analysis of variance

| **Source** | **DF** | **Adj SS** | **ADJ MS** | **F-Value** | **P-Value** |
|---|---|---|---|---|---|
| Solder Alloy | 1 | 226338 | 226338 | 43.21 | 0.000 |
| Surface Finish | 1 | 7127758 | 712758 | 136.07 | 0.000 |
| Temperature | 1 | 399740 | 399740 | 76.31 | 0.000 |
| Solder alloy*Surface Finish | 1 | 297025 | 297025 | 56.7 | 0.000 |
| Solder Alloy * Temperature | 1 | 1482 | 1482 | 0.28 | 0.597 |
| Surface Finish* Temperature | 1 | 64009 | 64009 | 12.22 | 0.000 |
| Solder alloy*Surface Finish*Temperature | 1 | 4258 | 4258 | 0.81 | 0.371 |
| Error | 56 | 293346 | 5238 | | |
| Total | 63 | 1998956 | | | |

Below is the Interaction plot of characteristic life at 25°C for both the alloys and surface finishes (Figure 7.4). From the plot, it can be noted that for SACQ has a higher characteristic life compared to SAC305 at OSP surface finish, however, the trend changes for ENIG surface finish where SAC305 performs better. Also, the difference in characteristic life is smaller for ENIG surface finish than for OSP. Similarly, it can also be noted that OSP surface finish give a higher characteristic life regardless of the solder alloy.

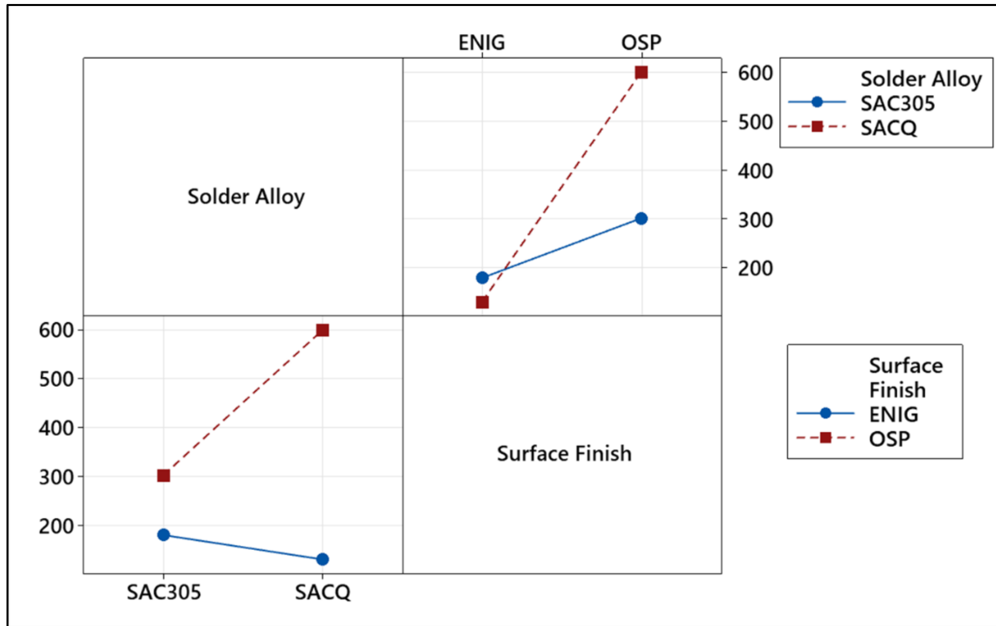



Figure 7.4 Interaction plot of characteristic life at 25°C. Each data point represents the characteristic life at that condition. Bottom left plot represents the change in characteristic life as the alloy changes, for both surface finishes. Top right plot represents the change in characteristic life as the surface finish changes, for both alloys.

Below is the Interaction plot of characteristic life at 75°C for both the alloys and surface finishes (Figure 7.5). From the Interaction plot we can observe that the characteristic life of SACQ is generally higher than the characteristic life of SAC305, regardless of the surface finish. It can also be noted that the increase in characteristic life is more drastic for SACQ as compared to SAC305 when the surface finish is changed from ENIG to OSP. Similarly, OSP surface finish is more reliable compared to ENIG surface finish, regardless of the solder alloy. Also, the increase in characteristic life is more drastic for OSP surface finish when the alloy is changed from SAC305 to SACQ.

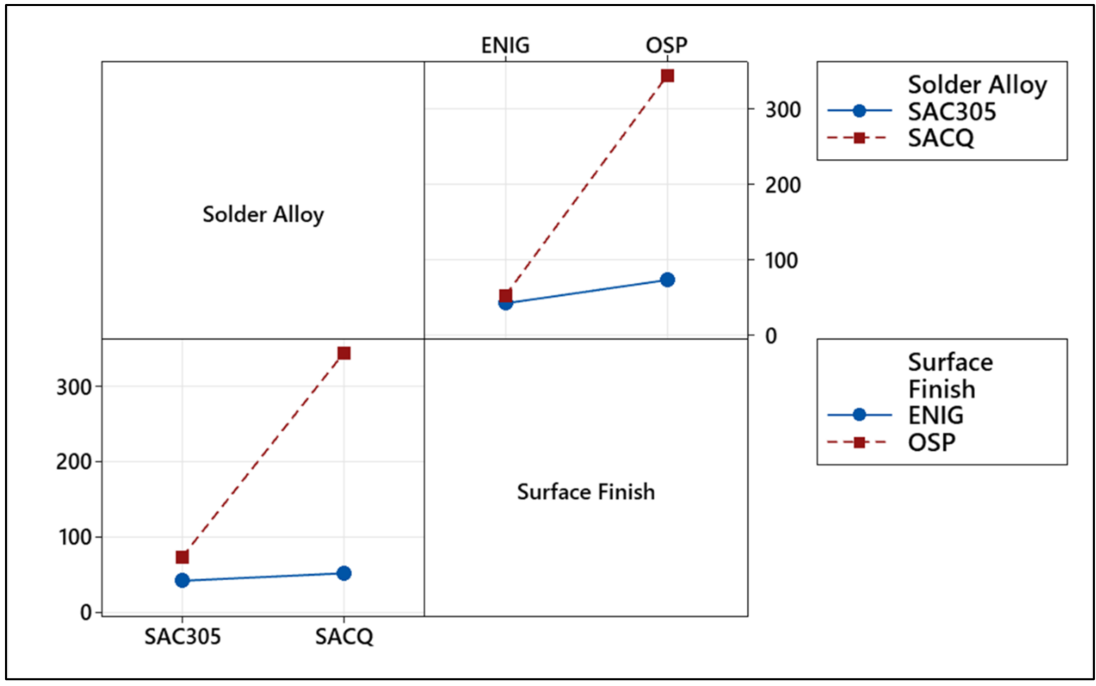



Figure 7.5 Interaction plot of characteristic life at 75°C

Below is the main effect plot for characteristic life for all the variables (Figure 7.6). We can observe that all the variable changes have a significant effect on the characteristic life. In general, SACQ has a higher characteristic life compared to SAC305. OSP surface finish is more reliabile compared to ENIG, and characteristic life decreases with an increase in temperature.

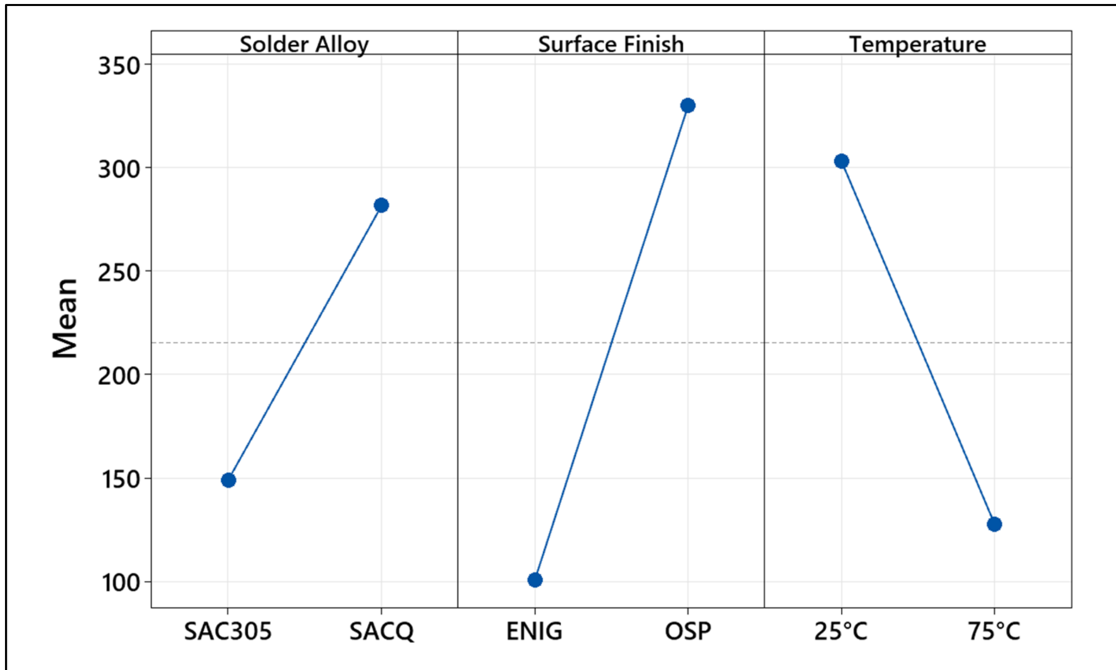



Figure 7.6 Main effect plot of characteristic life. Each data point represents the mean of characteristic life for each condition. The plot represents the trend in characteristic life with variable change.

### 7.3.3 Linear Regression

Multiple linear regression (LR) model was utilized to assess the relationship between the solder alloy, surface finish, temperature, and life (drops to failure for the solder joint). The LR model aims to quantify the strength of correlations between the response variable (life) and the explanatory variables (solder alloy, surface finish, and temperature). The LR model predicts the response by linearly combining the effects from the explanatory variables along with a constant value. The least squares method and gradient descent techniques are employed to minimize the error between the predicted and actual response values. For this analysis, only the interaction terms that exhibited a significant effect on life according to the previously conducted ANOVA model were included in the LR model. The coefficients of the LR model, along with their associated p-

values, are presented in Table 7.4. These coefficients provide insights into the magnitude and direction of the effects of each explanatory variable on the response variable.

Table 7.4 Table of Coefficients

| ***Predictors*** | ***Coefficient*** | ***P-value*** |
|---|---|---|
| **Intercept** | 193.19 | 6.06e-08 |
| **Temperature** | -1.90 | 0.000431 |
| **Solder Alloy (SACQ)** | -17.31 | 0.498016 |
| **Surface Finish (OSP)** | 201.31 | 2.53e-05 |
| **Solder Alloy (SACQ): Surface Finish (OSP)** | 272.50 | 2.99e-10 |
| **Surface Finish (OSP): Temperature** | -2.53 | 0.000839 |

The table presents the estimated coefficients using solder alloy (SAC305) and surface finish (ENIG) as reference values. For instance, the estimated difference between the mean drops to failure of OSP and ENIG is 201.3. The p-value assesses whether there is a significant difference between mean life values compared to SAC305. In the case of SACQ and SAC305, the p-value is 0.498, which exceeds the predefined significance level of 0.05, indicating an insignificant difference in mean life values. The following equation represents this model:

$$L = \beta_\circ + \beta_1 * SA + \beta_2 * SF + \beta_3 * T + \beta_4 * (SA * SF) + \beta_5 * (SF * T) \quad (7.1)$$

Where L represents the drops to failure value, $\beta_\circ$ denotes the intercept and $\beta_1$, $\beta_2$, $\beta_3$, $\beta_4$, $\beta_5$ are the estimated coefficients. SA represents the solder alloy, SA represents the surface finish, and T signifies the temperature.

Moreover, while ANOVA assesses an overall effect, determining whether the means are the same across groups, it does not specify which means differ if they are not the same. In contrast, the

regression model provides a p-value for each mean, promptly identifying the means that deviate from the reference (e.g., SAC305 for solder alloys). This allows for a more detailed examination of the differences between groups. Another advantage of the regression model is that it provides an 'estimate of the effect,' indicating the difference between two averages and a 95% confidence interval. For example, if the testing conditions involve a temperature of 50°C with SAC305 as the solder material and OSP as the surface finish, the predicted drops-to-failure value can be anticipated. In this scenario, the predicted drop-to-failure value is 173.188, with a confidence interval ranging from 137.252 to 209.123. This outcome is deemed acceptable compared to the actual drops-to-failure value of SAC305 at 25°C and 75°C, as illustrated in ANOVA plots.

### 7.3.3 Microstructure Analysis

The primary objective of this failure analysis is to investigate the different failure modes exhibited by solder joints under different conditions. Cross-sectional analysis was conducted on multiple samples to assess each specific condition. In Figures 7.7-7.14, a visual representation is presented, illustrating the failures of solder joints.

Below is the solder SAC305 solder joint with OSP surface finish at 25°C post failure (Figure 7.7).

All the failures observed at this test condition were brittle IMC layer failures on the board side.

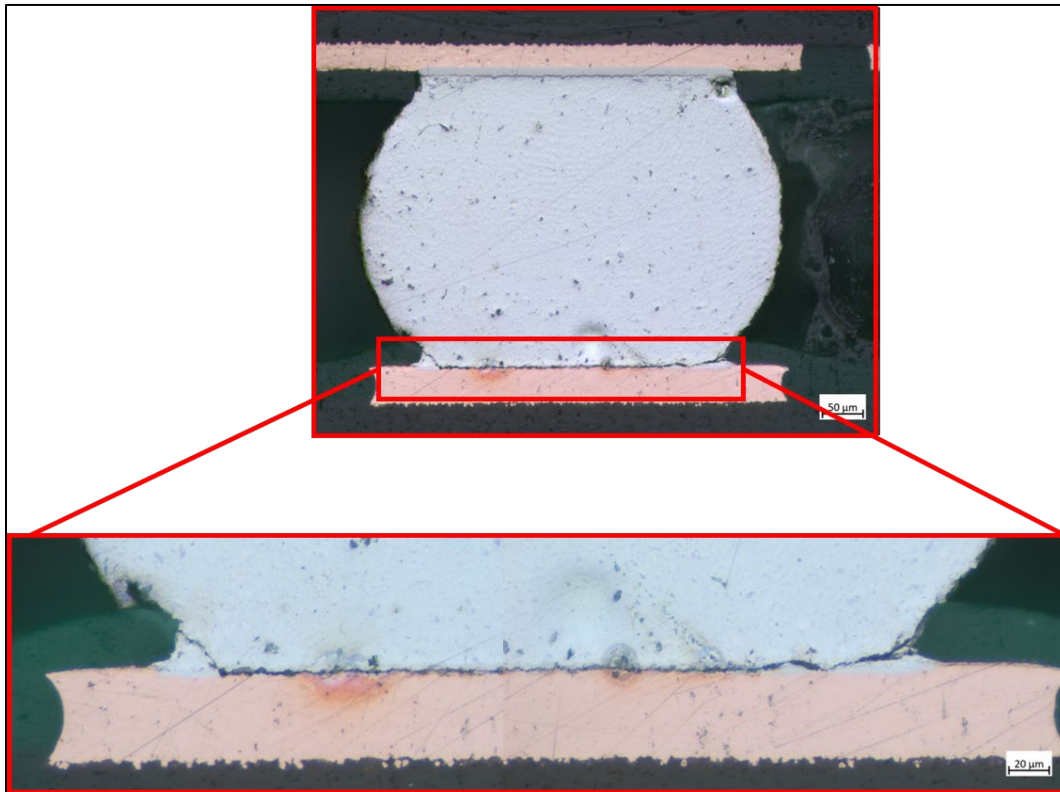



Figure 7.7 SAC305_OSP_25°C – IMC layer failure

Below is the SAC305 solder joint with OSP surface finish at 75°C post failure (Figure 7.8). All the failures observed at this test condition were ductile bulk solder failures on the board side.

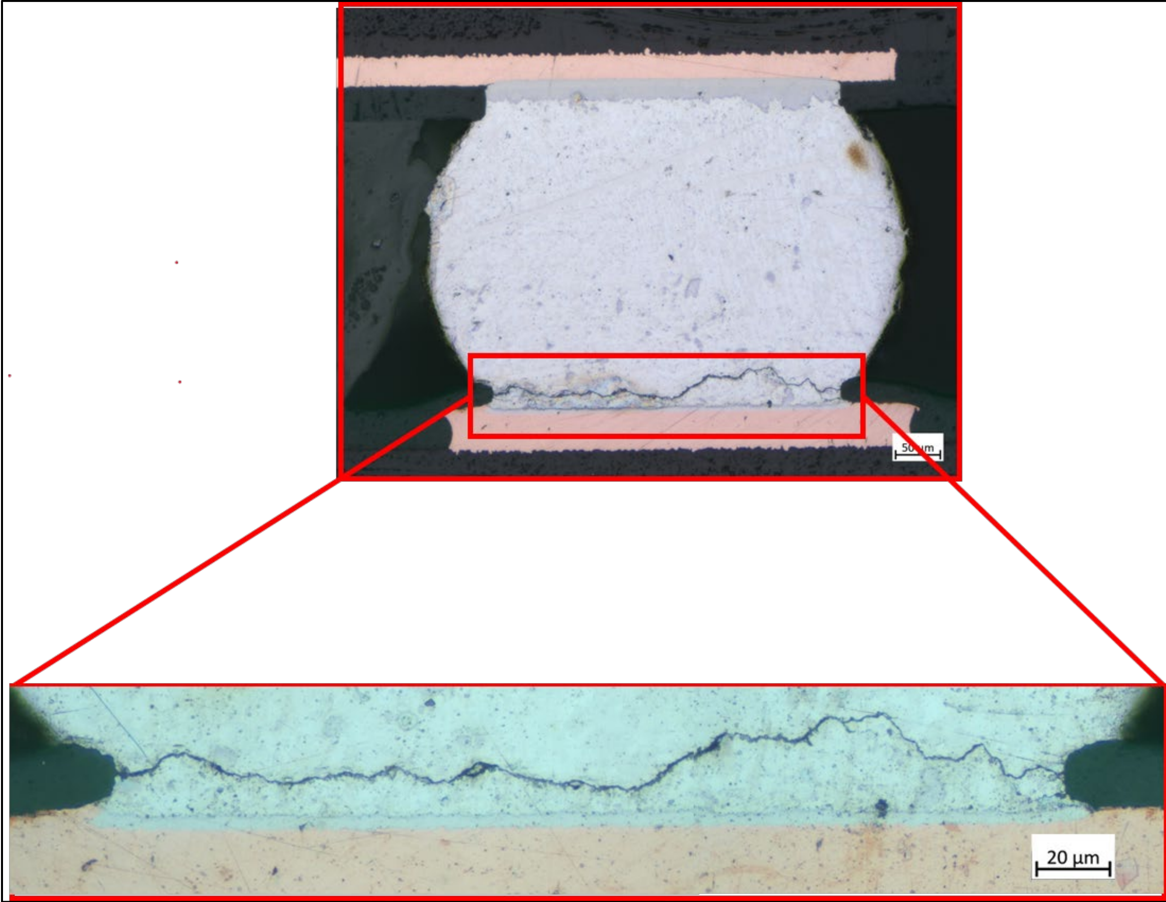



Figure 7.8 SAC305_OSP_75°C – bulk failure

Below is the SAC305 solder joint with ENIG surface finish at 25°C post failure (Figure 7.9). All the failures observed at this test condition were brittle IMC layer failures on the board side.

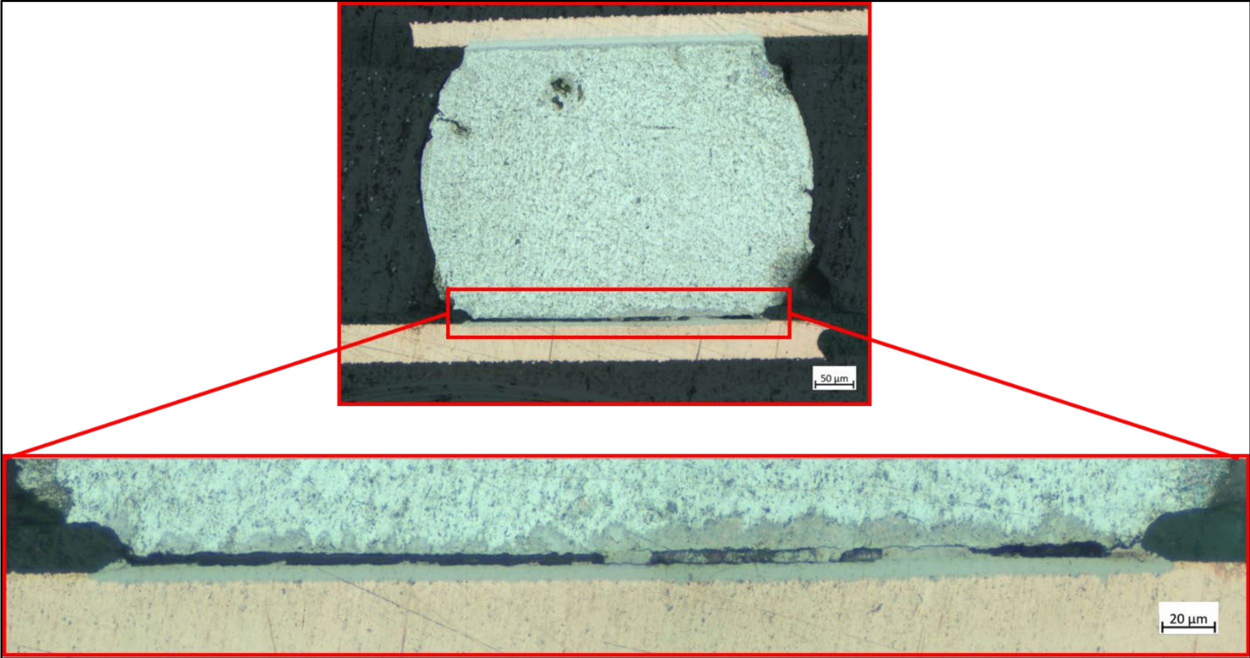



Figure 7.9 SAC305_ENIG_25°C – IMC layer failure

Below is the SAC305 solder joint with ENIG surface finish at 75°C post failure (Figure 7.10). All the failures observed at this test condition were brittle IMC layer failures on the board side.

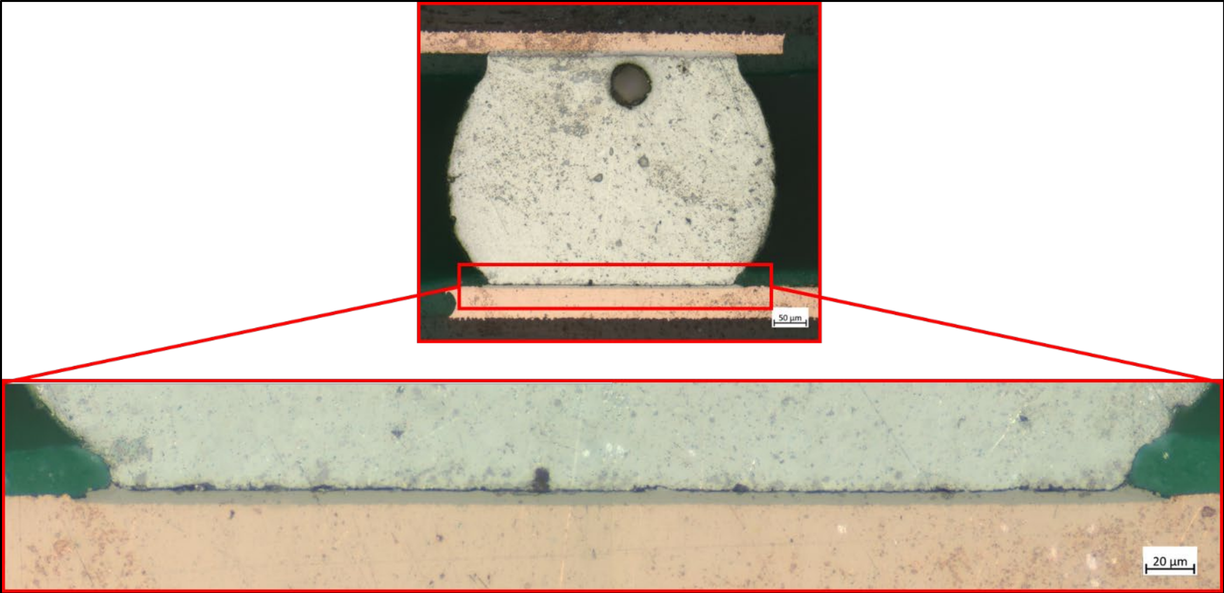



Figure 7.10 SAC305_ENIG_75°C – IMC layer failure

Below is the SACQ solder joint with OSP surface finish at 25°C post failure (Figure 7.11). All the failures observed at this test condition were brittle IMC layer failures on the board side.

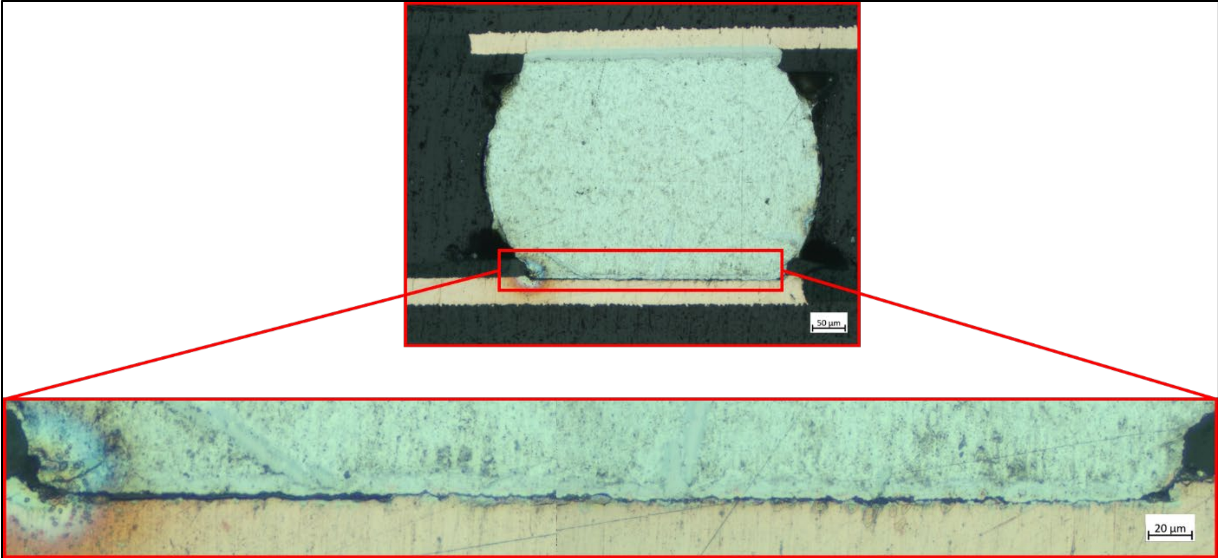



Figure 7.11 SACQ_OSP_25°C – IMC layer failure

Below is the SACQ solder joint with OSP surface finish at 75°C post failure (Figure 7.12). All the failures observed at this test condition were brittle IMC layer failures on the board side.

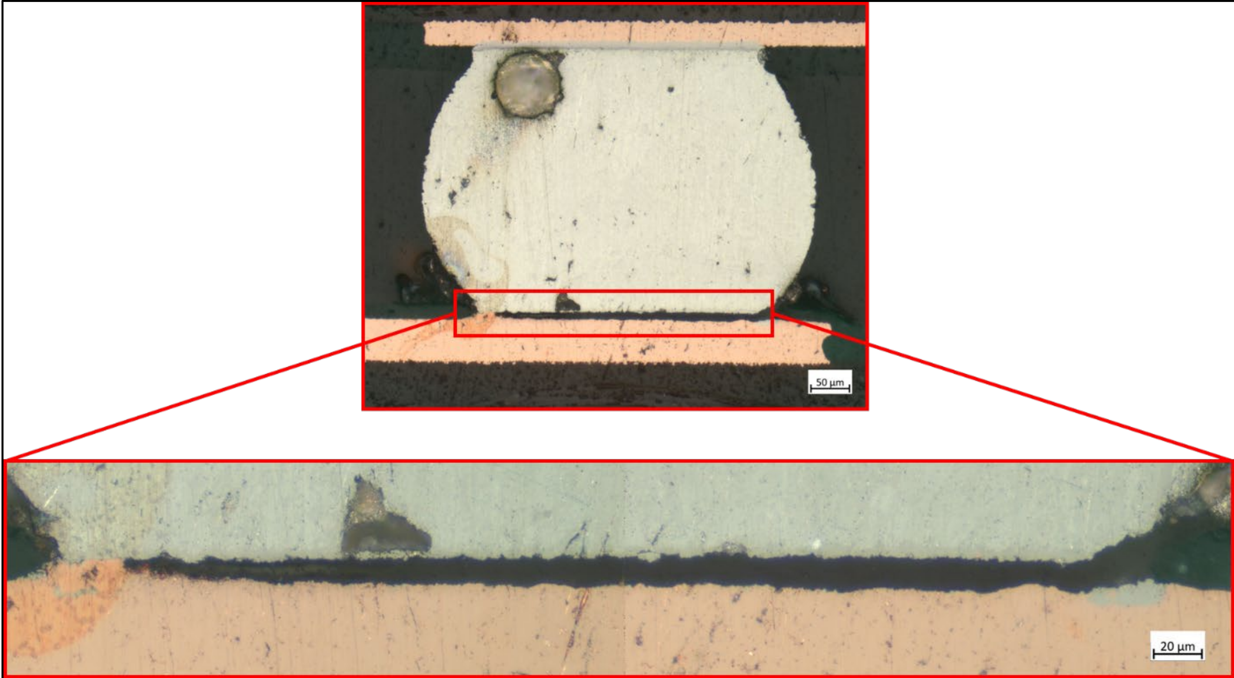



Figure 7.12 SACQ_OSP_75°C – IMC layer failure

Below is the SACQ solder joint with ENIG surface finish at 25°C post failure (Figure 7.13). All the failures observed at this test condition were brittle IMC layer failures on the board side.

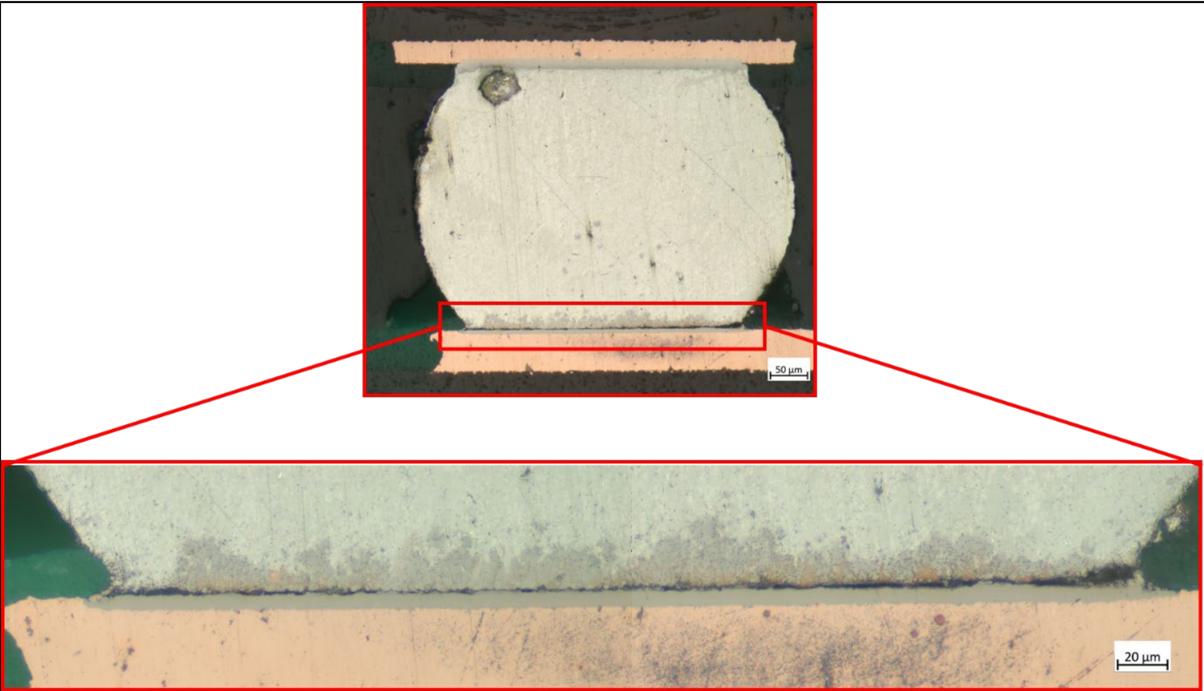



Figure 7.13 SACQ_ENIG_25°C – IMC layer failure

Below is the SACQ solder joint with ENIG surface finish at 75°C post failure (Figure 7.14). All the failures observed at this test condition were brittle IMC layer failures on the board side.

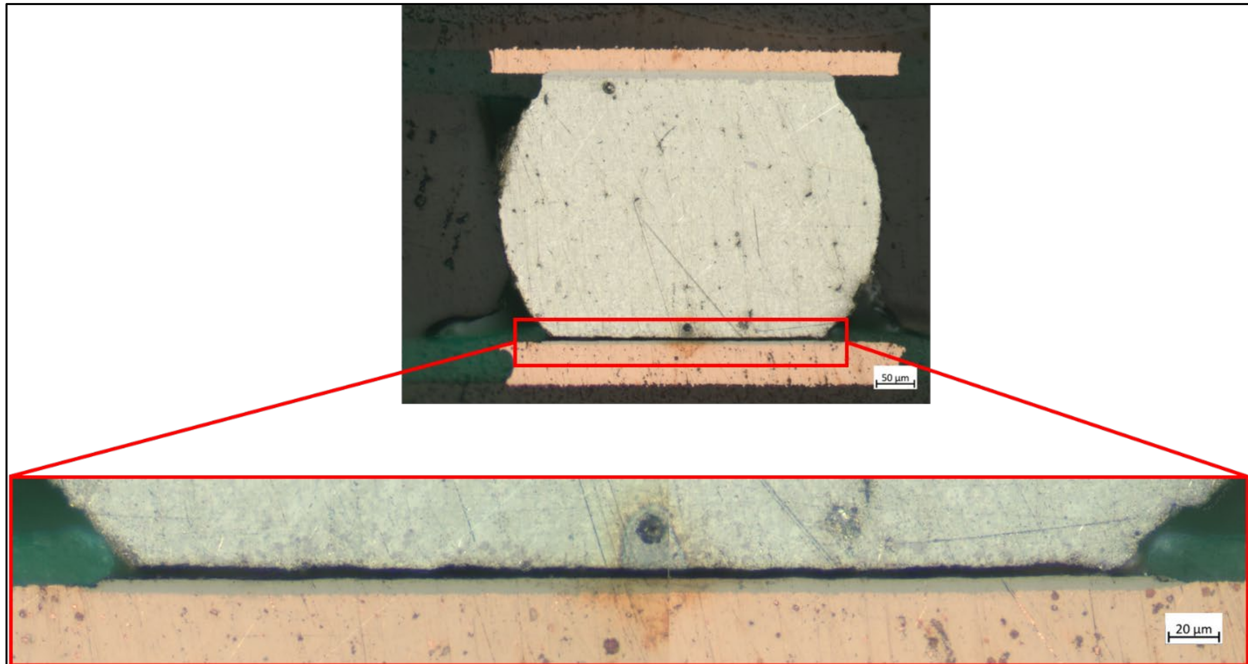



Figure 7.14 SACQ_ENIG_75°C – IMC layer failure

### 7.4 Conclusions

In conclusion, this study aimed to assess the impact of temperature and surface finish on the drop shock reliability of SAC305 and SACQ solder alloys. The investigation involved Weibull analysis, ANOVA analysis, and microstructure analysis, providing a comprehensive understanding of the solder joint behavior under different conditions. Among all test groups, SAC-Q OSP tested at 25°C exhibited the highest drop life, followed by SAC-Q OSP at 75°C. In contrast, SAC305 ENIG at 75°C showed the lowest drop life. Interestingly, SAC-Q generally demonstrated better drop life compared to SAC305, regardless of temperature or surface finish, except for ENIG at 25°C where

SAC305 outperformed SAC-Q. Notably, both alloys exhibited a decrease in drop life with increasing temperature (25°C to 75°C), irrespective of surface finish. Furthermore, ENIG consistently displayed lower drop life compared to OSP for both alloys and temperatures. The results indicated that the choice of solder alloy and surface finish can significantly influence the drop shock reliability of electronic devices. Microscopic analysis of SAC305 OSP revealed a shift in failure mode: at 25°C, failure occurred within the IMC layer, while at 75°C, failure shifted to the bulk solder. For all other test conditions, failure consistently occurred within the IMC layer, and all failures were observed on the board side. Overall, the findings emphasize the importance of considering temperature and surface finish in solder joint performance assessments, providing valuable insights for the electronics industry to enhance the durability of portable and handheld devices in real-world scenarios.

# Chapter 8 Overall Summary, Conclusions, and Future Work

## 8.1 Overall Summary and Conclusions

The first study investigated the drop shock performance of SnPb, SAC305, and three Bi-doped SAC alloys (Innolot, Cyclomax, and Sabix) in BGA assemblies subjected to varying input energies. The primary objective was to evaluate and compare their reliability under different drop shock conditions. Microstructure analysis was employed to elucidate the underlying failure mechanisms. Among the Bi-doped SAC alloys, Innolot exhibited the superior drop shock performance at 2000 G and below, followed by Cyclomax and Sabix. This can be attributed to their optimized compositions leading to improved mechanical properties. However, at 2500 G, SAC305 demonstrated the highest reliability due to its retained ductility at elevated strain rates, translating to greater toughness and resistance to crack propagation. Conversely, SnPb consistently displayed the weakest performance across all energy levels. Failure mode analysis revealed distinct characteristics for each alloy. SnPb exhibited cracks solely within the bulk solder, while Innolot, Cyclomax, and Sabix experienced cracks exclusively in the IMC layer. Notably, SAC305 displayed a unique evolution of failure modes: transitioning from bulk solder cracks at 1000 G to mixed bulk solder and IMC cracks at 1500-2000 G, and finally to complete IMC failure at 2500 G. This phenomenon can be ascribed to the strain-rate dependent material properties of SAC305, where the increased strength and stiffness at higher strain rates suppress plastic deformation and promote brittle fracture within the IMC layer. Furthermore, a positive correlation was established between solder hardness and drop shock performance at specific energy levels (1500 and 2000 G). This suggests that harder alloys offer enhanced resistance to drop shock under these conditions. These findings contribute significantly to the field of portable electronics reliability. This study

highlights the potential of Bi-doped SAC alloys with optimized compositions for surpassing the performance of traditional SnPb and even SAC305 in certain scenarios. Additionally, the identified failure mechanisms provide valuable insights for further materials development and design optimization.

The second study presented a comprehensive investigation into the drop shock performance of SAC305 solder joints in BGA assemblies with an OSP finish across a range of temperatures (25°C, 50°C, 75°C, and 100°C). The results demonstrate a clear correlation between increasing temperature and decreasing drop shock reliability. SAC305 exhibited superior performance at room temperature (25°C), achieving a characteristic life exceeding 300 drops. However, as temperature escalated, reliability deteriorated significantly. Characteristic life progressively decreased to 108 drops at 50°C, 73 drops at 75°C, and a mere 65 drops at 100°C. A similar trend was observed for the β10 life, highlighting the consistent decline in reliability with elevated temperatures. To quantify the relationship between temperature and reliability, the Arrhenius model was employed. This model established a correlation between drop shock life and temperature, enabling the prediction of solder joint performance under diverse thermal conditions. The microstructure analysis revealed a shift in the dominant failure mode as temperature increased. At lower temperatures (25°C and 50°C), brittle failure dominated, characterized by cracks propagating primarily within the IMC layer. However, a distinct transition emerged at elevated temperatures (75°C and 100°C). Ductile failure became more prevalent, with cracks initiating and propagating in both the bulk solder and IMC layer (mixed mode), or only within the bulk solder. This shift can be attributed to the altered material properties of the solder joint at higher temperatures, where decreased yield strength and elastic modulus promote ductile behavior.

The third study investigated the multifaceted relationship between solder alloy, surface finish, and operating temperature on the drop shock reliability of BGA assemblies. By evaluating the performance of SAC305 and SACQ solder alloys on both organic solderability preservative (OSP) and electroless nickel/immersion gold (ENIG) finishes across temperatures 25°C and 75°C. In general, SACQ demonstrated better drop shock resistance compared to its SAC305. Its characteristic and B10 lives, reflecting the predicted number of drops before failure, were notably higher under all investigated conditions. A decrease in drop life was observed for both SAC305 and SACQ as temperature increases from 25°C to 75°C. The impact of surface finish was also a significant factor. OSP consistently outperformed ENIG in terms of drop shock performance for both solder alloys and across all temperatures. For SAC305 with OSP surface finish, At 25°C, the intermetallic compound (IMC) layer within the solder joint exhibited brittle failure due to localized stress concentration. However, as temperature climbed to 75°C, a shift occurred, with the bulk solder becoming the primary site of failure, exhibiting ductile behavior.

## 8.2 Future Work

This work can be extended by conducting drop shock test of various components such as land grid arrays, column grid array etc. Additionally, the effect of underfilling on drop shock performance of solder joint must also be studied. Drop shock performance must be conducted for PCBs mounted at different angles. For elevated temperatures testing, various other high reliability solder alloys must be studied and compared. Additionally, surface finishes such as ENEPIG, ImSn etc. could also provide valuable insights. By understanding these details more thoroughly, researchers and industry experts can help develop better electronic devices for the future. These improved components would not only perform exceptionally well but also be more reliable, leading to progress in different technological fields.

## BIBLIOGRAPHY

[1] J. Lau, C. P. Wong, N.-C. Lee, and R. Lee, *Electronics Manufacturing with Lead-Free Halogen-Free and Conductive-Adhesive*, vol. 17. 2003.

[2] S. K. Kang and A. K. Sarkhel, “Lead (Pb)-free solders for electronic packaging,” *J Electron Mater*, vol. 23, no. 8, pp. 701–707, Aug. 1994, doi: 10.1007/BF02651362.

[3] R. Prasad, *Surface mount technology: principles and practice*. 2013.

[4] R. Lin, E. Blackshear, and P. Serisky, “Moisture induced package cracking in plastic encapsulated surface mount components during solder reflow process,” in *26th Annual Proceedings Reliability Physics Symposium 1988*, IEEE, pp. 83–89. doi: 10.1109/RELPHY.1988.23431.

[5] P. L. Tu, Y. C. Chan, and J. K. L. Lai, “Effect of intermetallic compounds on the thermal fatigue of surface mount solder joints,” *IEEE Transactions on Components, Packaging, and Manufacturing Technology: Part B*, vol. 20, no. 1, pp. 87–93, 1997, doi: 10.1109/96.554534.

[6] “Semiconductor Back-End Process 2: The Roles, Process, and Evolution of Semiconductor Packaging,” *SK hynix Newsroom*. https://news.skhynix.com/semiconductor-back-end-process-episode-2-semiconductor-packaging/, Dec. 05, 2023.

[7] J. H. Saleh and K. Marais, “Highlights from the early (and pre-) history of reliability engineering,” *Reliab Eng Syst Saf*, vol. 91, no. 2, pp. 249–256, Feb. 2006, doi: 10.1016/j.ress.2005.01.003.

[8] M. Thurston, *Practical Reliability Of Electronic Equipment And Products* . New York: Marcel Dekker inc, 2003.

[9] W. Weibull, “A Statistical Distribution Function of Wide Applicability,” *J Appl Mech*, vol. 18, no. 3, pp. 293–297, Sep. 1951, doi: 10.1115/1.4010337.

[10] “Weibull Distribution Characteristics,” *ReliaWiki*.

[11] T.-S. Park and S.-B. Lee, “Low Cycle Fatigue Testing of Ball Grid Array Solder Joints under Mixed-Mode Loading Conditions,” *J Electron Packag*, vol. 127, no. 3, pp. 237–244, Sep. 2005, doi: 10.1115/1.1871192.

[12] C. Kanchanomai and Y. Mutoh, “Effect of temperature on isothermal low cycle fatigue properties of Sn–Ag eutectic solder,” *Materials Science and Engineering: A*, vol. 381, no. 1–2, pp. 113–120, Sep. 2004, doi: 10.1016/j.msea.2004.04.018.

[13] B. Trumble, “Get the lead out! [lead free solder],” *IEEE Spectr*, vol. 35, no. 5, pp. 55–60, May 1998, doi: 10.1109/6.669978.

[14] “https://fctsolder.com/eutectic-solder/,” FCT Solder.

[15] H. Black, “Getting the Lead Out of Electronics,” *Environ Health Perspect*, vol. 113, no. 10, Oct. 2005, doi: 10.1289/ehp.113-a682.

[16] “IPC Roadmap: A Guide for Assembly of Lead-Free Electronics,”,” IPC.

[17] Z. Cai, Y. Zhang, J. C. Suhling, P. Lall, R. W. Johnson, and M. J. Bozack, “Reduction of lead free solder aging effects using doped SAC alloys,” in *2010 Proceedings 60th Electronic Components and Technology Conference (ECTC)*, IEEE, 2010, pp. 1493–1511. doi: 10.1109/ECTC.2010.5490796.

[18] D. A. Shnawah, M. F. M. Sabri, and I. A. Badruddin, “A review on thermal cycling and drop impact reliability of SAC solder joint in portable electronic products,” *Microelectronics Reliability*, vol. 52, no. 1, pp. 90–99, Jan. 2012, doi: 10.1016/j.microrel.2011.07.093.

[19] D. A. Benson, R. T. Mitchell, M. R. Tuck, D. R. Adkins, and D. W. Palmer, “Micro-machined heat pipes in silicon MCM substrates,” in *Proceedings 1996 IEEE Multi-Chip Module Conference (Cat. No.96CH35893)*, IEEE Comput. Soc. Press, pp. 127–129. doi: 10.1109/MCMC.1996.510782.

[20] E. Bradley and K. Banerji, “Effect of PCB finish on the reliability and wettability of ball grid array packages,” *IEEE Transactions on Components, Packaging, and Manufacturing Technology: Part B*, vol. 19, no. 2, pp. 320–330, May 1996, doi: 10.1109/96.496035.

[21] Zequn Mei, M. Kaufmann, A. Eslambolchi, and P. Johnson, “Brittle interfacial fracture of PBGA packages soldered on electroless nickel/immersion gold,” in *1998 Proceedings. 48th Electronic Components and Technology Conference (Cat. No.98CH36206)*, IEEE, pp. 952–961. doi: 10.1109/ECTC.1998.678824.

[22] P. Snugovsky, P. Arrowsmith, and M. Romansky, “Electroless Ni/Immersion Au interconnects: Investigation of black pad in wire bonds and solder joints,” *J Electron Mater*, vol. 30, no. 9, pp. 1262–1270, Sep. 2001, doi: 10.1007/s11664-001-0159-z.

[23] Kejun Zeng, V. Vuorinen, and J. K. Kivilahti, “Interfacial reactions between lead-free SnAgCu solder and Ni(P) surface finish on printed circuit boards,” *IEEE Transactions on Electronics Packaging Manufacturing*, vol. 25, no. 3, pp. 162–167, Jul. 2002, doi: 10.1109/TEPM.2002.801648.

[24] J.-W. Yoon and S.-B. Jung, “Effect of immersion Ag surface finish on interfacial reaction and mechanical reliability of Sn–3.5Ag–0.7Cu solder joint,” *J Alloys Compd*, vol. 458, no. 1–2, pp. 200–207, Jun. 2008, doi: 10.1016/j.jallcom.2007.04.014.

[25] Y.-H. Chen, Y.-Y. Wang, and C.-C. Wan, “Microstructural characteristics of immersion tin coatings on copper circuitries in circuit boards,” *Surf Coat Technol*, vol. 202, no. 3, pp. 417–424, Dec. 2007, doi: 10.1016/j.surfcoat.2007.06.004.

[26] M. Arra, D. Shangguan, D. Xie, J. Sundelin, T. Lepistö, and E. Ristolainen, “Study of immersion silver and tin printed-circuit-board surface finishes in lead-free solder applications,” *J Electron Mater*, vol. 33, no. 9, pp. 977–990, Sep. 2004, doi: 10.1007/s11664-004-0025-x.

[27] Xiang Dai, M. V. Brillhart, and P. S. Ho, “Adhesion measurement for electronic packaging applications using double cantilever beam method,” *IEEE Transactions on Components and Packaging Technologies*, vol. 23, no. 1, pp. 101–116, Mar. 2000, doi: 10.1109/6144.833049.

[28] K. C. Norris and A. H. Landzberg, “Reliability of Controlled Collapse Interconnections,” *IBM J Res Dev*, vol. 13, no. 3, pp. 266–271, May 1969, doi: 10.1147/rd.133.0266.

[29] Dally, J. W, P. Lall, and J. Suhling, *Mechanical design of electronic systems*. College House Enterprises, 2008.

[30] K. J. Puttlitz and P. A. Totta, *Area array interconnection handbook*. Springer Science & Business Media, 2012.

[31] K. Shimohashi, X. Zhou, and J. M. Schoenung, “A test-rework process yield performance model for estimation of printed wiring board assembly cost,” *Int J Prod Econ*, vol. 119, no. 1, pp. 161–173, May 2009, doi: 10.1016/j.ijpe.2009.02.004.

[32] A. Edward, “Characterisation of lead-free solder pastes and their correlation with the stencil printing process performance,” 2012.

[33] “Quality Control,” *Ventura Technology*. https://venturatech.com/quality/inspection/.

[34] “What is a Fiducial Mark?: PCB Knowledge - PCB Manufacturing Information,” *PCBway*. https://www.pcbway.com/blog/PCB_Manufacturing_Information/Fiducial_Mark_PCB_Knowledge_542b3c29.html.

[35] “MK7 Reflow Oven Featured at IPC APEX 2022 Booth 1920,” *Heller*. https://hellerindustries.com/reflow-news/mk7-reflow-oven-featured-at-ipc-apex-2022-booth-1920/, Mar. 30, 2023.

[36] “PCB X-ray Inspection in Real Time,” *Solder.net*. https://www.solder.net/services/pcb-x-ray-inspection/.

[37] “Electronic devices and appliances,” *MECA courses - Home*. https://www.ett.bme.hu/meca/Courses/TEP/7_3.html.

[38] S. Etris *et al.*, “Fatigue Behavior of Solders Used in Flip-Chip Technology,” *J Test Eval*, vol. 1, no. 2, p. 170, 1973, doi: 10.1520/JTE10895J.

[39] “Observation and Measurement of Through Holes and Lands on PWBs,” *KEYENCE*. https://www.keyence.eu/ss/products/microscope/vhx-casestudy/electronics/printed-circuit-board.jsp.

[40] "Practical Components," *www.practicalcomponents.com*. https://www.practicalcomponents.com/home/print-view.cfm?type=pkg&prid=1010.

[41] "Drop & Shock Testing," Shinyei.

[42] "JEDEC, 'Board level drop test method of components for handheld electronic products,' JES22-B111A."

[43] E. H. Wong, K. M. Lim, N. Lee, S. Seah, C. Hoe, and J. Wang, "Drop impact test - mechanics & physics of failure," in *4th Electronics Packaging Technology Conference, 2002.*, IEEE, pp. 327–333. doi: 10.1109/EPTC.2002.1185692.

[44] C. T. Lim, C. W. Ang, L. B. Tan, S. K. W. Seah, and E. H. Wong, "Drop impact survey of portable electronic products," in *53rd Electronic Components and Technology Conference, 2003. Proceedings.*, IEEE, pp. 113–120. doi: 10.1109/ECTC.2003.1216265.

[45] J. Wu, G. Song, C.-P. Yeh, and K. Wyatt, "Drop/impact simulation and test validation of telecommunication products," in *ITherm'98. Sixth Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (Cat. No.98CH36208)*, IEEE, pp. 330–336. doi: 10.1109/ITHERM.1998.689582.

[46] Dongji Xie, M. Arra, Sanuny Yi, and D. Rooney, "Solder joint behavior of area array packages in board level drop for handheld devices," in *53rd Electronic Components and Technology Conference, 2003. Proceedings.*, IEEE, pp. 130–135. doi: 10.1109/ECTC.2003.1216267.

[47] P. Lall, D. Panchagade, Yueli Liu, W. Johnson, and J. Suhling, "Models for reliability prediction of fine-pitch BGAs and CSPs in shock and drop-impact," in *2004 Proceedings.*

*54th Electronic Components and Technology Conference (IEEE Cat. No.04CH37546)*, IEEE, pp. 1296–1303. doi: 10.1109/ECTC.2004.1320280.

[48] P. Lall, D. Panchagade, P. Choudhary, J. Suhling, and S. Gupte, “Failure-Envelope Approach to Modeling Shock and Vibration Survivability of Electronic and MEMS Packaging,” in *Proceedings Electronic Components and Technology, 2005. ECTC ’05.*, IEEE, pp. 480–490. doi: 10.1109/ECTC.2005.1441309.

[49] A. Agrawal, T. Levo, J. Pitarresi, and B. Roggeman, “Board level energy correlation and interconnect reliability modeling under drop impact,” in *2009 59th Electronic Components and Technology Conference*, IEEE, May 2009, pp. 1694–1702. doi: 10.1109/ECTC.2009.5074243.

[50] M. Amagai, Y. Toyoda, T. Ohnishi, and S. Akita, “High drop test reliability: lead-free solders,” in *2004 Proceedings. 54th Electronic Components and Technology Conference (IEEE Cat. No.04CH37546)*, IEEE, pp. 1304–1309. doi: 10.1109/ECTC.2004.1320281.

[51] T.-K. Lee and W. Xie, “Effect of Board Thickness on Sn-Ag-Cu Joint Interconnect Mechanical Shock Performance,” *J Electron Mater*, vol. 43, no. 12, pp. 4522–4531, Dec. 2014, doi: 10.1007/s11664-014-3479-5.

[52] G. Iyer, E. Ouyang, W. Kittidacha, S. Tantideeravit, and L. Suresh, “Pb-free Solder: SAC105 vs SAC305 Drop-Test Reliability Data Comparison,” in *2007 32nd IEEE/CPMT International Electronic Manufacturing Technology Symposium*, IEEE, Oct. 2007, pp. 251–255. doi: 10.1109/IEMT.2007.4417072.

[53] Vickers Nicholas, Rauen Kyle, Farris Andrew, and Pan Jianbiao, “Board Level Failure Analysis of Chip Scale Package Drop Test Assemblies ,” in *41st International Symposium on Microelectronics*, Providence, Nov. 2008.

[54] A. Farris *et al.*, “Drop impact reliability of edge-bonded lead-free chip scale packages,” *Microelectronics Reliability*, vol. 49, no. 7, pp. 761–770, Jul. 2009, doi: 10.1016/j.microrel.2009.05.003.

[55] B. Roggeman *et al.*, “Assessment of PCB pad cratering resistance by joint level testing,” in *2008 58th Electronic Components and Technology Conference*, IEEE, May 2008, pp. 884–892. doi: 10.1109/ECTC.2008.4550081.

[56] A. Farris *et al.*, “Drop test reliability of lead-free chip scale packages,” in *2008 58th Electronic Components and Technology Conference*, IEEE, May 2008, pp. 1173–1180. doi: 10.1109/ECTC.2008.4550124.

[57] S.-W. R. Lee, Y.-L. T. Li, and H.-W. ben Lui, “Experimental Evaluation on Solder Joint Reliability of PBGA Assembly Under Mechanical Drop Test,” in *Electronic and Photonic Packaging, Electrical Systems Design and Photonics, and Nanotechnology*, ASMEDC, Jan. 2002, pp. 181–185. doi: 10.1115/IMECE2002-39493.

[58] G. Heaslip, J. Punch, B. Rogers, C. Ryan, and M. Reid, “A Simulated and Experimental Comparison of Lead-Free and Tin-Lead Solder Interconnect Failure Under Impact Stimuli,” in *Advances in Electronic Packaging, Parts A, B, and C*, ASMEDC, Jan. 2005, pp. 1283–1291. doi: 10.1115/IPACK2005-73366.

[59] G. M. Heaslip, J. M. Punch, B. A. Rodgers, and C. Ryan, “Board Level Drop Tests Comparing Lead-Free and Eutectic Solder Interconnects on a BGA Package for Mobile ICT

Applications," in *Electronic and Photonic Packaging, Electrical Systems Design and Photonics, and Nanotechnology*, ASMEDC, Jan. 2004, pp. 353–362. doi: 10.1115/IMECE2004-59162.

[60] Yi-Shao Lai, P. C. Chen, Chang-Lin Yeh, and J. C. B. Lee, "The Effect of IMC Microstructure of Solder Joint on the Mechanical Drop Performance in SnxAgCu and SnAgCuX CSP Package," in *56th Electronic Components and Technology Conference 2006*, IEEE, pp. 1935–1939. doi: 10.1109/ECTC.2006.1645926.

[61] T. T. Mattila, P. Marjamaki, and J. K. Kivilahti, "Reliability of CSP Interconnections Under Mechanical Shock Loading Conditions," *IEEE Transactions on Components and Packaging Technologies*, vol. 29, no. 4, pp. 787–795, Dec. 2006, doi: 10.1109/TCAPT.2006.885948.

[62] T. C. Chai *et al.*, "Board level drop test reliability of IC packages," in *Proceedings Electronic Components and Technology, 2005. ECTC '05.*, IEEE, pp. 630–636. doi: 10.1109/ECTC.2005.1441335.

[63] Jie Gu, C. T. Lim, and A. A. O. Tay, "Simulation of mechanical response of solder joints under drop impact using equivalent layer models," in *Proceedings Electronic Components and Technology, 2005. ECTC '05.*, IEEE, pp. 491–498. doi: 10.1109/ECTC.2005.1441310.

[64] M.-L. Wu and J.-S. Lan, "Reliability and failure analysis of SAC 105 and SAC 1205N lead-free solder alloys during drop test events," *Microelectronics Reliability*, vol. 80, pp. 213–222, Jan. 2018, doi: 10.1016/j.microrel.2017.12.013.

[65] S. Su *et al.*, “Reliability of Micro-Alloyed SnAgCu Based Solder Interconnections for Various Harsh Applications,” in *2019 IEEE 69th Electronic Components and Technology Conference (ECTC)*, IEEE, May 2019, pp. 2309–2317. doi: 10.1109/ECTC.2019.00318.

[66] S. K. Saha, S. Mathew, and S. Canumalla, “Effect of intermetallic phases on performance in a mechanical drop environment: 96.5Sn3.5Ag solder on Cu and Ni/Au pad finishes,” in *2004 Proceedings. 54th Electronic Components and Technology Conference (IEEE Cat. No.04CH37546)*, IEEE, pp. 1288–1295. doi: 10.1109/ECTC.2004.1320279.

[67] T.-K. Lee, Z. Chen, C. Guirguis, and K. Akinade, “Impact of Isothermal Aging and Testing Temperature on Large Flip-Chip BGA Interconnect Mechanical Shock Performance,” *J Electron Mater*, vol. 46, no. 10, pp. 6224–6233, Oct. 2017, doi: 10.1007/s11664-017-5650-2.

[68] T. T. Mattila, J. Simecek, and J. K. Kivilahti, “Failure Modes of Solder Interconnections under Mechanical Shock Loading at Elevated Temperatures,” in *2006 1st Electronic Systemintegration Technology Conference*, IEEE, Sep. 2006, pp. 195–202. doi: 10.1109/ESTC.2006.279998.

[69] T.-K. Lee, “Impact of External Temperature Environment on Large FCBGA Sn-Ag-Cu Solder Interconnect Board Level Mechanical Shock Performance,” *Journal of Welding and Joining*, vol. 32, no. 3, pp. 53–59, Jun. 2014, doi: 10.5781/JWJ.2014.32.3.53.

[70] C.-L. Yeh and Y.-S. Lai, “Support excitation scheme for transient analysis of JEDEC board-level drop test,” *Microelectronics Reliability*, vol. 46, no. 2–4, pp. 626–636, Feb. 2006, doi: 10.1016/j.microrel.2004.12.021.

[71] A. Bansal, T.-K. Lee, K.-C. Liu, and J. Xue, “Effects of isothermal aging and in-situ current stress on the reliability of lead-free solder joints,” in *2010 Proceedings 60th Electronic Components and Technology Conference (ECTC)*, IEEE, 2010, pp. 1529–1535. doi: 10.1109/ECTC.2010.5490790.

[72] B. T. Lampe, “Room Temperature Aging Properties of Some Solder Alloys,” *Weld J*, vol. 55, pp. 330s–340s, 1976.

[73] A. S. Medvedev, “Aging of Tin-Lead Solders and Joints Soldered by Them,” *Metallovedenie i Obrabotka Metallov*, vol. 7, pp. 16–23, 1956.

[74] C. Key Chung, R. Aspandiar, K. Foo Leong, and Cheng Siew Tay, “The interactions of lead (Pb) in lead free solder (Sn/Ag/Cu) system,” in *52nd Electronic Components and Technology Conference 2002. (Cat. No.02CH37345)*, IEEE, pp. 168–175. doi: 10.1109/ECTC.2002.1008091.

[75] C. Hunt, J. Nottay, A. Brewin, and A. Dinsdale, “Predicting Microstructure of Mixed Solder Alloy System,” 2002.

[76] C. M. Chuang, T. S. Lui, and L. H. Chen, “Effect of aluminum addition on tensile properties of naturally aged Sn-9Zn eutectic solder,” *J Mater Sci*, vol. 37, no. 1, pp. 191–195, 2002, doi: 10.1023/A:1013143218738.

[77] S. J and et.al., “Variations in Thermal Cycling Response of Pb-Free Solder Due to Isothermal Preconditioning,” SMTAI, 2011, pp. 641–654.

[78] S. Su *et al.*, “Effect of Surface Finish on the Fatigue Behavior of Bi-based Solder Joints,” in *2019 18th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena*

*in Electronic Systems (ITherm)*, IEEE, May 2019, pp. 1155–1159. doi: 10.1109/ITHERM.2019.8757419.

[79] H. Ma and J. C. Suhling, “A review of mechanical properties of lead-free solders for electronic packaging,” *J Mater Sci*, vol. 44, no. 5, pp. 1141–1158, Mar. 2009, doi: 10.1007/s10853-008-3125-9.

[80] Young-Bae Kim, H. Noguchi, and M. Amagai, “Vibration fatigue reliability of BGA-IC package with Pb-free solder and Pb-Sn solder,” in *53rd Electronic Components and Technology Conference, 2003. Proceedings.*, IEEE, pp. 891–897. doi: 10.1109/ECTC.2003.1216397.

[81] F. Akkara and et.al., “Effects of Long-term Aging on SnAgCu Solder Joints Reliability in Mechanical Cycling Fatigue,” *SMTA*, 2017.

[82] W. J. Plumbridge and C. R. Gagg, ““‘Effects of Strain Rate and Temperature on the Stress–Strain Response of Solder Alloys,” *Journal of Materials Science: Materials in Electronics*, vol. 10, no. 5/6, pp. 461–468, 1999, doi: 10.1023/A:1008930430875.

[83] M. Date, T. Shoji, M. Fujiyoshi, K. Sato, and K. N. Tu, “Impact reliability of solder joints,” in *2004 Proceedings. 54th Electronic Components and Technology Conference (IEEE Cat. No.04CH37546)*, IEEE, pp. 668–674. doi: 10.1109/ECTC.2004.1319410.

[84] S. Ahat, M. Sheng, and L. Luo, “Microstructure and shear strength evolution of SnAg/Cu surface mount solder joint during aging,” *J Electron Mater*, vol. 30, no. 10, pp. 1317–1322, Oct. 2001, doi: 10.1007/s11664-001-0118-8.

[85] T. T. Mattila, J. Hokka, and M. Paulasto-Kröckel, “The Reliability of Microalloyed Sn-Ag-Cu Solder Interconnections Under Cyclic Thermal and Mechanical Shock Loading,” *J Electron Mater*, vol. 43, no. 11, pp. 4090–4102, Nov. 2014, doi: 10.1007/s11664-014-3298-8.

[86] X. Liu, V. K. Sooklal, M. A. Verges, and M. C. Larson, “Experimental study and life prediction on high cycle vibration fatigue in BGA packages,” *Microelectronics Reliability*, vol. 46, no. 7, pp. 1128–1138, Jul. 2006, doi: 10.1016/j.microrel.2005.09.011.

[87] T. E. Wong, F. W. Palmieri, B. A. Reed, H. S. Fenger, H. M. Cohen, and K. T. Teshiba, “Durability/reliability of BGA solder joints under vibration environment,” in *2000 Proceedings. 50th Electronic Components and Technology Conference (Cat. No.00CH37070)*, IEEE, pp. 1083–1088. doi: 10.1109/ECTC.2000.853304.

[88] Y. L. Zhang, X. Q. Shi, and W. Zhou, “Effect of hygrothermal aging on interfacial reliability of flip chip on board (FCOB) assembly,” in *Proceedings of 6th Electronics Packaging Technology Conference (EPTC 2004) (IEEE Cat. No.04EX971)*, IEEE, pp. 404–409. doi: 10.1109/EPTC.2004.1396642.

[89] Yifei Zhang, Zijie Cai, J. C. Suhling, P. Lall, and M. J. Bozack, “The effects of aging temperature on SAC solder joint material behavior and reliability,” in *2008 58th Electronic Components and Technology Conference*, IEEE, May 2008, pp. 99–112. doi: 10.1109/ECTC.2008.4549956.

[90] Q. J. Yang, G. H. Lim, R. M. Lin, F. F. Yap, H. L. J. Pang, and Z. P. Wang, “Experimental modal analysis of PBGA printed circuit board assemblies,” in *Proceedings of the 1997 1st*

*Electronic Packaging Technology Conference (Cat. No.97TH8307)*, IEEE, pp. 290–296. doi: 10.1109/EPTC.1997.723924.

[91] Q. J. Yang, H. L. J. Pang, Z. P. Wang, G. H. Lim, F. F. Yap, and R. M. Lin, "Vibration reliability characterization of PBGA assemblies," *Microelectronics Reliability*, vol. 40, no. 7, pp. 1097–1107, Jul. 2000, doi: 10.1016/S0026-2714(00)00036-6.

[92] Q. J. Yang, Z. P. Wang, G. H. Lim, J. H. L. Pang, F. F. Yap, and R. M. Lin, "Reliability of PBGA assemblies under out-of-plane vibration excitations," *IEEE Transactions on Components and Packaging Technologies*, vol. 25, no. 2, pp. 293–300, Jun. 2002, doi: 10.1109/TCAPT.2002.1010020.

[93] Q. Yu, H. Kikuchi, S. Ikeda, M. Shiratori, M. Kakino, and N. Fujiwara, "Dynamic behavior of electronics package and impact reliability of BGA solder joints," in *ITherm 2002. Eighth Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (Cat. No.02CH37258)*, IEEE, pp. 953–960. doi: 10.1109/ITHERM.2002.1012559.

[94] K. R. Shah and M. Mello, "Ball grid array solder joint failure envelope development for dynamic loading," in *2004 Proceedings. 54th Electronic Components and Technology Conference (IEEE Cat. No.04CH37546)*, IEEE, pp. 1067–1074. doi: 10.1109/ECTC.2004.1319472.

[95] P. L. Tu, Y. C. Chan, and J. K. L. Lai, "Effect of intermetallic compounds on vibration fatigue of μBGA solder joint," *IEEE Transactions on Advanced Packaging*, vol. 24, no. 2, pp. 197–205, May 2001, doi: 10.1109/6040.928755.

[96] P. Lall, G. Limaye, J. Suhling, M. Murtuza, B. Palmer, and W. Cooper, "Reliability of lead-free SAC electronics under simultaneous exposure to high temperature and vibration," in

*13th InterSociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems*, IEEE, May 2012, pp. 753–761. doi: 10.1109/ITHERM.2012.6231503.

[97] Y.-S. Lai, P.-F. Yang, and C.-L. Yeh, "Experimental studies of board-level reliability of chip-scale packages subjected to JEDEC drop test condition," *Microelectronics Reliability*, vol. 46, no. 2–4, pp. 645–650, Feb. 2006, doi: 10.1016/j.microrel.2005.07.005.

[98] J. Y. Choi, I. S. Kang, B. J. Park, Y. M. Park, and G. J. Jung, "Study on Inter-Metallic Compound (IMC) at Interface of Pb-Free Solder and Nickel UBM for Mobile Application," in *2007 Proceedings 57th Electronic Components and Technology Conference*, IEEE, 2007, pp. 1802–1808. doi: 10.1109/ECTC.2007.374041.

[99] Z. Mei, M. Ahmad, M. Hu, and G. Ramakrishna, "Kirkendall voids at Cu/solder interface and their effects on solder joint reliability," in *Proceedings Electronic Components and Technology, 2005. ECTC '05.*, IEEE, pp. 415–420. doi: 10.1109/ECTC.2005.1441298.

[100] S. K. Kang *et al.*, "Interfacial reactions of Sn-Ag-Cu solders modified by minor Zn alloying addition," *J Electron Mater*, vol. 35, no. 3, pp. 479–485, Mar. 2006, doi: 10.1007/BF02690535.

[101] M. E. A. Belhadi, L. Wentlent, R. al Athamneh, and S. Hamasha, "Mechanical properties of SAC-Bi solder alloys with aging," SMTA, Sep. 2021.

[102] J. Zhao, Y. Mutoh, Y. Miyashita, and S. L. Mannan, "Fatigue crack-growth behavior of Sn-Ag-Cu and Sn-Ag-Cu-Bi lead-free solders," *J Electron Mater*, vol. 31, no. 8, pp. 879–886, Aug. 2002, doi: 10.1007/s11664-002-0199-z.

[103] M. J. Rizvi, Y. C. Chan, C. Bailey, H. Lu, and M. N. Islam, "Effect of adding 1wt% Bi into the Sn–2.8Ag–0.5Cu solder alloy on the intermetallic formations with Cu-substrate during soldering and isothermal aging," *J Alloys Compd*, vol. 407, no. 1–2, pp. 208–214, Jan. 2006, doi: 10.1016/j.jallcom.2005.06.050.

[104] J. H. Lee, S. Kumar, H. J. Kim, Y. W. Lee, and J. T. Moon, "High thermo-mechanical fatigue and drop impact resistant Ni-Bi doped lead free solder," in *2014 IEEE 64th Electronic Components and Technology Conference (ECTC)*, IEEE, May 2014, pp. 712–716. doi: 10.1109/ECTC.2014.6897362.

[105] J. Zhao, L. Qi, X. Wang, and L. Wang, "Influence of Bi on microstructures evolution and mechanical properties in Sn–Ag–Cu lead-free solder," *J Alloys Compd*, vol. 375, no. 1–2, pp. 196–201, Jul. 2004, doi: 10.1016/j.jallcom.2003.12.005.

[106] W. Liu and N.-C. Lee, "The effects of additives to SnAgCu alloys on microstructure and drop impact reliability of solder joints," *JOM*, vol. 59, no. 7, pp. 26–31, Jul. 2007, doi: 10.1007/s11837-007-0085-5.

[107] I. E. Anderson, J. W. Walleser, J. L. Harringa, F. Laabs, and A. Kracher, "Nucleation Control and Thermal Aging Resistance of Near-Eutectic Sn-Ag-Cu-X Solder Joints by Alloy Design," *J Electron Mater*, vol. 38, no. 12, pp. 2770–2779, Dec. 2009, doi: 10.1007/s11664-009-0936-7.

[108] M. Amagai, Y. Toyoda, T. Ohnishi, and S. Akita, "High drop test reliability: lead-free solders," in *2004 Proceedings. 54th Electronic Components and Technology Conference (IEEE Cat. No.04CH37546)*, IEEE, pp. 1304–1309. doi: 10.1109/ECTC.2004.1320281.

[109] R. S. Pandher, B. G. Lewis, R. Vangaveti, and B. Singh, “Drop Shock Reliability of Lead-Free Alloys - Effect of Micro-Additives,” in *2007 Proceedings 57th Electronic Components and Technology Conference*, IEEE, 2007, pp. 669–676. doi: 10.1109/ECTC.2007.373868.

[110] IPC-9703, “Mechanical Shock Test Methods and Qualification Requirements for Surface Mount Solder Attachments (Working Draft),” Apr. 2004.

[111] K. Newman, “BGA brittle fracture - alternative solder joint integrity test methods,” in *Proceedings Electronic Components and Technology, 2005. ECTC ’05.*, IEEE, pp. 1194–1201. doi: 10.1109/ECTC.2005.1441422.

[112] F. Kraemer, S. Wiese, S. Rzepka, W. Faust, and J. Lienig, “A detailed investigation of the failure formation of copper trace cracks during drop tests,” in *3rd Electronics System Integration Technology Conference ESTC*, IEEE, Sep. 2010, pp. 1–6. doi: 10.1109/ESTC.2010.5642938.

[113] T. Y. Tee, H. S. Ng, A. Syed, R. Anderson, C. P. Khoo, and B. Rogers, “Design for board trace reliability of WLCSP under drop test,” in *EuroSimE 2009 - 10th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems*, IEEE, Apr. 2009, pp. 1–8. doi: 10.1109/ESIME.2009.4938518.

[114] N. Li *et al.*, “A novel pin-pull tester and its application on PCB pad cratering assessment,” in *2015 16th International Conference on Electronic Packaging Technology (ICEPT)*, IEEE, Aug. 2015, pp. 1198–1202. doi: 10.1109/ICEPT.2015.7236794.

[115] S. Menon, D. Y. Chen, M. Osterman, and M. G. Pecht, “Copper Trace Fatigue Life Modeling for Rigid Electronic Assemblies,” *IEEE Transactions on Device and Materials Reliability*, vol. 21, no. 1, pp. 79–86, Mar. 2021, doi: 10.1109/TDMR.2021.3055432.

[116] P. Lall, A. Angral, and J. Suhling, “Board trace fatigue models and design guidelines for electronics under shock-impact,” in *2010 12th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems*, IEEE, Jun. 2010, pp. 1–7. doi: 10.1109/ITHERM.2010.5501310.

[117] Liping Zhu and W. Marcinkiewicz, “Drop impact reliability analysis of CSP packages at board and product system levels through modeling approaches,” in *The Ninth Intersociety Conference on Thermal and Thermomechanical Phenomena In Electronic Systems (IEEE Cat. No.04CH37543)*, IEEE, pp. 296–303. doi: 10.1109/ITHERM.2004.1318296.

[118] C.-L. Yeh, Y.-S. Lai, and C.-L. Kao, “Evaluation of board-level reliability of electronic packages under consecutive drops,” *Microelectronics Reliability*, vol. 46, no. 7, pp. 1172–1182, Jul. 2006, doi: 10.1016/j.microrel.2005.09.002.

[119] Tz-Cheng Chiu, Kejun Zeng, R. Stierman, D. Edwards, and K. Ano, “Effect of thermal aging on board level drop reliability for Pb-free BGA packages,” in *2004 Proceedings. 54th Electronic Components and Technology Conference (IEEE Cat. No.04CH37546)*, IEEE, pp. 1256–1262. doi: 10.1109/ECTC.2004.1320275.

[120] Jing-en Luan, Tong Yan Tee, Xueren Zhang, and E. Hussab, “Solder joint failure modes, mechanisms, and life prediction models of IC packages under board level drop impact,” in *2005 6th International Conference on Electronic Packaging Technology*, IEEE, pp. 382–388. doi: 10.1109/ICEPT.2005.1564714.

[121] K. Herrmann, “Hardness Testing: Principles and Applications,” *ASM International*, 2011.

[122] W. C. Oliver and G. M. Pharr, “Measurement of hardness and elastic modulus by instrumented indentation: Advances in understanding and refinements to methodology,” *J Mater Res*, vol. 19, no. 1, pp. 3–20, Jan. 2004, doi: 10.1557/jmr.2004.19.1.3.

[123] N. A. Sakharova, J. V. Fernandes, J. M. Antunes, and M. C. Oliveira, “Comparison between Berkovich, Vickers and conical indentation tests: A three-dimensional numerical simulation study,” *Int J Solids Struct*, vol. 46, no. 5, pp. 1095–1104, Mar. 2009, doi: 10.1016/j.ijsolstr.2008.10.032.

[124] P. Lall, V. Mehta, J. Suhling, and K. Blecker, “Effect of Evolution of High Strain Rate Properties on Plastic-Work of SAC305 Alloy with 100° C Aging for Periods up to 240-days,” in *2022 21st IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (iTherm)*, IEEE, 2022, pp. 1–16.

[125] M. E. A. Belhadi, S. Hamasha, and A. Alahmer, “Effect of Bi content and aging on solder joint shear properties considering strain rate,” *Microelectronics Reliability*, vol. 146, p. 115020, 2023.

[126] P. Lall, V. Mehta, J. Suhling, and D. Locker, “Study of Sustained High-Temperature on the Reliability of Lead-Free Solder Joint Assemblies Under Vibration,” in *ASME 2023 International Technical Conference and Exhibition on Packaging and Integration of Electronic and Photonic Microsystems*, American Society of Mechanical Engineers, Oct. 2023. doi: 10.1115/IPACK2023-111984.

[127] T. T. Mattila, J. Li, and J. K. Kivilahti, “On the effects of temperature on the drop reliability of electronic component boards,” *Microelectronics Reliability*, vol. 52, no. 1, pp. 165–179, Jan. 2012, doi: 10.1016/j.microrel.2011.07.085.

[128] F. J. Akkara, S. Hamasha, A. Alahmer, J. Evans, M. E. A. Belhadi, and X. Wei, “The Effect of Micro-Alloying and Surface Finishes on the Thermal Cycling Reliability of Doped SAC Solder Alloys,” *Materials*, vol. 15, no. 19, p. 6759, Sep. 2022, doi: 10.3390/ma15196759.

[129] M. E. A. Belhadi, S. Hamasha, A. Alahmer, Q. Qasaimeh, A. Alakayleh, and S. Alavi, “Investigating the Evolution of Creep Properties during Thermal Cycling of Homogeneous Lead-Free Solder Joints,” *IEEE Trans Compon Packaging Manuf Technol*, pp. 1–1, 2023, doi: 10.1109/TCPMT.2023.3337634.

[130] R. Al Athamneh, D. B. Hani, S. Hamasha, and M. Abueed, “Arrhenius Fatigue Life Modeling for Lead-Free Solder Joints in Accelerated Combined Fatigue and Creep Tests at Different Operating Temperatures,” *IEEE Trans Compon Packaging Manuf Technol*, vol. 13, no. 3, pp. 332–345, Mar. 2023, doi: 10.1109/TCPMT.2023.3256184.

[131] Jue Li, T. T. Mattila, and J. K. Kivilahti, “Computational Assessment of the Effects of Temperature on Wafer-Level Component Boards in Drop Tests,” *IEEE Transactions on Components and Packaging Technologies*, vol. 32, no. 1, pp. 38–43, Mar. 2009, doi: 10.1109/TCAPT.2008.2005401.

[132] T. T. Mattila, R. J. James, L. Nguyen, and J. K. Kivilahti, “Effect of Temperature on the Drop Reliability of Wafer-Level Chip Scale Packaged Electronics Assemblies,” in *2007 Proceedings 57th Electronic Components and Technology Conference*, IEEE, 2007, pp. 940–945. doi: 10.1109/ECTC.2007.373909.