INITIATION AND PROGRESSION OF DAMAGE IN LEADFREE ELECTRONICS UNDER DROP-IMPACT

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INITIATION AND PROGRESSION OF DAMAGE IN LEAD-FREE ELECTRONICS UNDER DROP IMPACT

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INITIATION AND PROGRESSION OF DAMAGE IN LEADFREE ELECTRONICS UNDER DROP-IMPACT

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Signature of Author

Date of Graduation

VITA

Deepti Raju Iyengar, daughter of Mr. S. Raju, Senior Deputy Director, the Automotive Research Association of India (ARAI) and Mrs. Lakshmi Raju Iyengar, Senior Auditor, Central Defense Accounts (Officers) (CDAO), was born on 12th September, 1982, in Pune, Maharashtra, India. Upon graduating from high school, she earned her Bachelor of Engineering (BE) degree in Mechanical Engineering from University of Pune, India in the year 2004. She worked for the University of Pune as an instructor, teaching Machine Design from January 2005 to June 2005. In the quest to augment her academic qualifications and technical experience, she moved to Auburn, Alabama in August 2005. Since her enrollment in the M.S. program at Auburn University, she has worked for the Semiconductor Research Corporation (SRC) as a Graduate Research Assistant in the area of impact reliability of electronic packaging. She has an elder brother Vijay who received his Bachelor of Engineering degree in Electronics and Telecommunication from University of Pune. He is the co-founder and CEO of Embedded Computing Machines (ECM).

THESIS ABSTRACT

INITIATION AND PROGRESSION OF DAMAGE IN LEADFREE ELECTRONICS UNDER DROP-IMPACT

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Electronics may be subjected to shock, vibration, and drop impact during shipping, handling, and normal usage. Measurement of transient dynamic deformation of the electronic assemblies during shock and vibration can yield significant insight in understanding the occurrence of failure modes and the development of failure envelopes. In this work, the transient dynamics of board assemblies in the form of relative displacement, drop angle, velocity, and acceleration were measured with high-speed imaging. In addition, high-speed data acquisition systems with discrete strain gages were used for measurements of transient strain at fixed locations. A new technique called digital image correlation (DIC) using ultra high-speed cameras for full-field measurement of transient strain was investigated. Various board assemblies subjected to shock at different drop orientations were examined. Accuracy of the high-speed optical

measurements was compared with that from discrete strain gages. Explicit finite-element models were developed and correlated with experimental data.

There is a fundamental need for the development of predictive techniques for electronic failure mechanisms in shock and drop-impact. Presently, one of the primary methodologies for assessment of shock and vibration survivability of electronic packaging is the JEDEC drop test method, JESD22-B111 [JEDEC 2003] which tests board-level reliability of packaging. However, packages in electronic products may be subjected to a wide array of boundary conditions beyond those targeted in the test method. Development of damage-equivalency methodologies will be invaluable in correlating standard test conditions to widely varying design-use conditions. In this work, the development of solder-joint stress based relative damage index was investigated to establish a method for damage equivalency.

In practical applications, electronics are subjected not only to drop and shock but to a combination of loads. Thus, effect of overlapping stresses on the deformation behavior of solder interconnects was investigated. The effect of different package architectures and various surface finishes including ImAg, ImSn and ENIG on impact reliability was studied. Life prediction of new lead-free alloy-systems under shock and vibration is largely unexplored. An approach to model drop and shock survivability of electronic packaging is presented for six lead-free solder alloy systems including Sn1Ag0.5Cu, Sn3Ag0.5Cu, Sn0.3Ag0.7Cu, Sn0.3Ag0.7Cu-Bi, Sn0.3Ag0.7Cu-Bi-Ni, and 96.5Sn3.5Ag. The approach is scalable to a wide variety of electronic applications.

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1

INTRODUCTION

1.1 Electronic Packaging

Electronics is the biggest, most dynamic, and rapidly evolving worldwide industry. It is an industry working under the constant pressure to improve, thus reinventing itself endlessly. Electronic systems play an important role today. They are a part of every aspect of life including simple devices like watches to complex devices such as super computers. Electronics are present in every field and are invariably used by everyone.

Electronic Packaging is a major discipline of electronics that includes a wide variety of technologies like materials, design, architecture, process and manufacture. Packaging of electronic system refers to the placement and connection of various electronic and electromechanical components, which are placed in an enclosure that protects the system from the environment. Electronic packaging is conventionally defined as a process that alters bare integrated circuits (IC) into useful products. It not only acts as a bridge between the micron IC world and the macroscopic world of peripheral devices, but also provides electrical signal connections, power supply, a path for heat dissipation and environmental protection.

The co-founder of Intel, Gordon E. Moore observed and stated a very important trend in the history of computer hardware [Moore 1965]. According to Moore, the transistors that can be inexpensively placed on an integrated circuit were increasing exponentially and were doubling approximately every two years. The trend has been maintained for more than 40 years as shown in Figure 1.1 and is expected to continue at least for a decade more. Almost all of the factors used to gauge the capability of digital electronic systems are associated with Moore's Law, all of which have progressed at exponential rates. This progression is one of the key factors that has increased the importance of electronics. Moore's Law was especially responsible for the dynamic technological advancements in electronic packaging in the past half century.

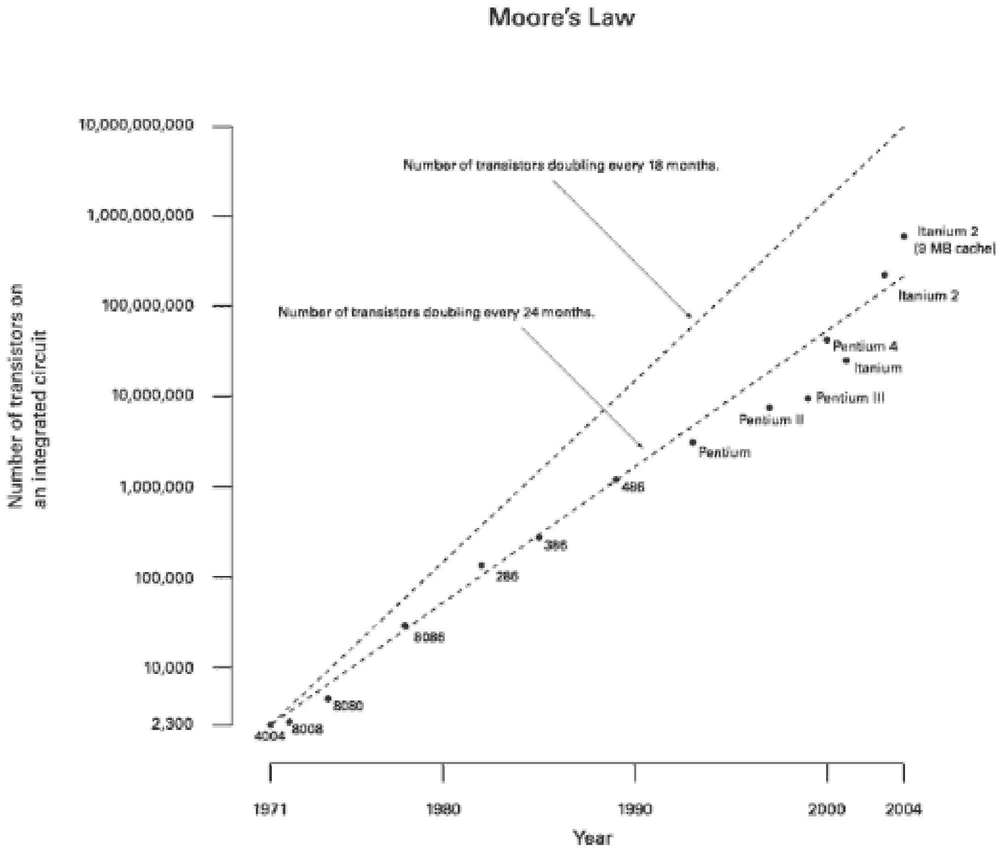


Figure 1.1: Moore's Law

1.2 Categorization of Electronic Packaging

Electronic systems are classified into several levels of packaging with characteristic types of interconnects associated with them. As per the hierarchy shown in Figure 1.2, the silicon wafer is at the zero level. The first level includes chip carriers, underfilled flip chips, chip level interconnect, and passive devices such as resistors. The second level comprises of printed circuit boards (PCB), printed wired boards (PWB) or cards. The third level incorporates the mother board and connections between PCBs and PWBs and the forth level contains connections between two subassemblies. Connections between two physically separated systems such as a computer and a printer are referred to as the fifth or final level of packaging.

The two technologies for printed circuit board assemblies are plated through hole (PTH) and surface mount technology (SMT). The former is out dated as surface mount technology is far more superior. Some of the advantages of the later include more pin count on the same area and lower costs. PTH packages include Dual In Line Package (DIP), Shrink DIP (SH-DIP), Skinny DIP (SK-DIP), Slim DIP (SL-DIP), Zig-zag In Line Package (ZIP) and Pin Grid Array (PGA). The surface mount packages include Small Out-line Package (SOP), Quad Flat Package (QFP), Leadless Chip Carrier (LCC), Plastic Leaded Chip Carrier (PLCC), Ball Grid Array (BGA), Tape Automated Bonding (TAB) and Chip Scale Package (CSP). The progression of chip carriers from chip on board to package on board is shown in Figure 1.3. Some of the different types of packaging technologies are shown in Figure 1.4.

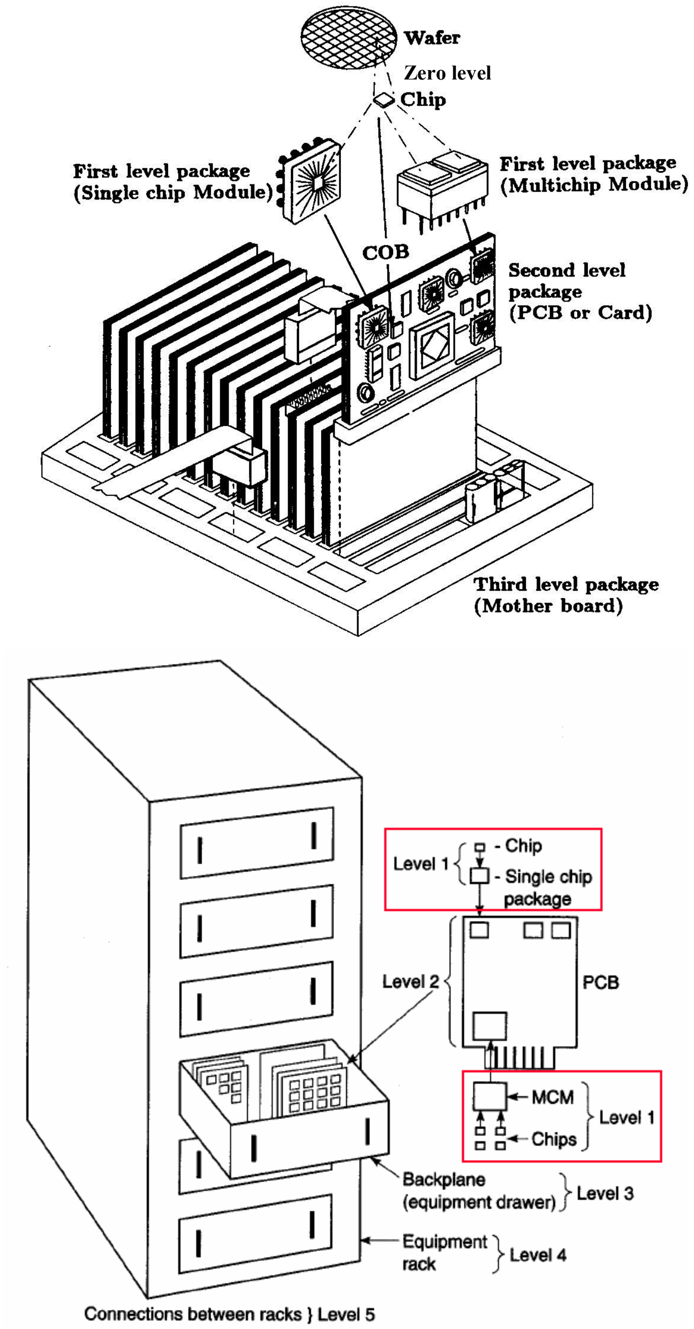


Figure 1.2 : Electronic Packaging Hierarchy [MECH 6310 Course Notes]

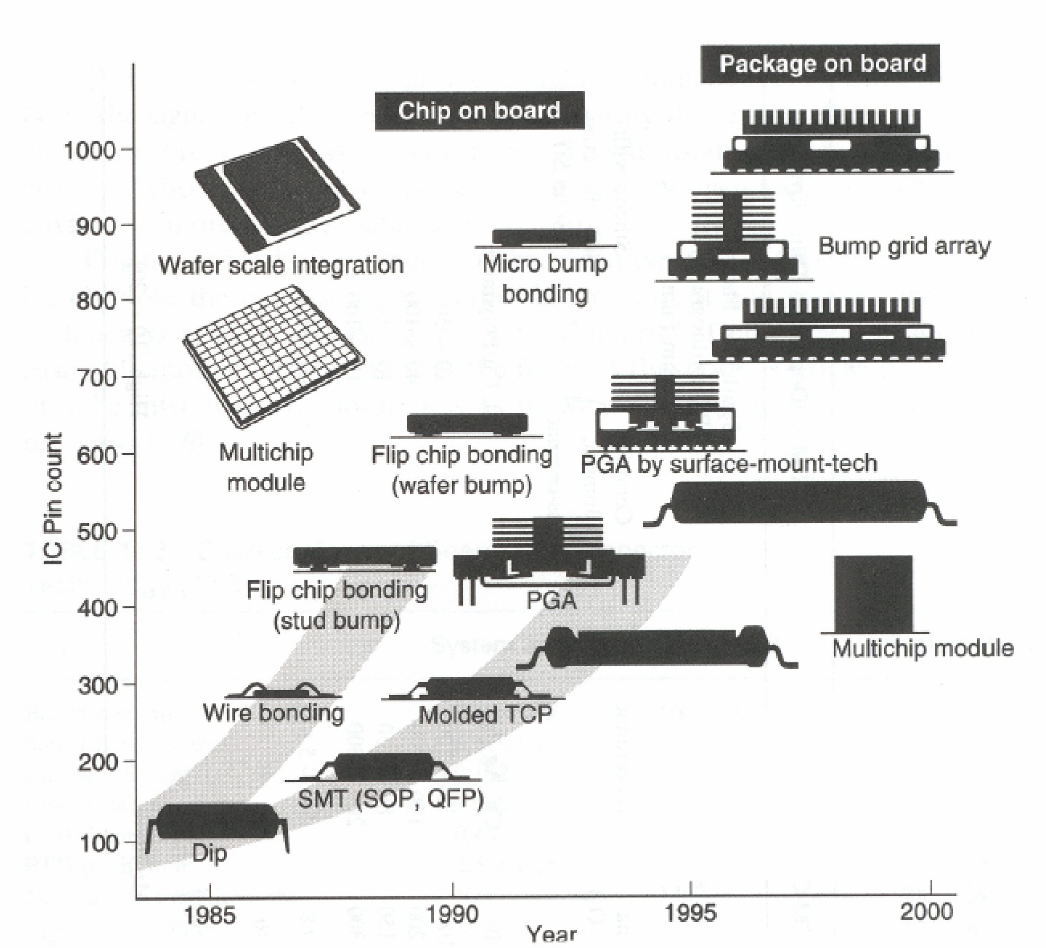


Figure 1.3 : Evolution of Chip Carriers [MECH 6310 Course Notes]

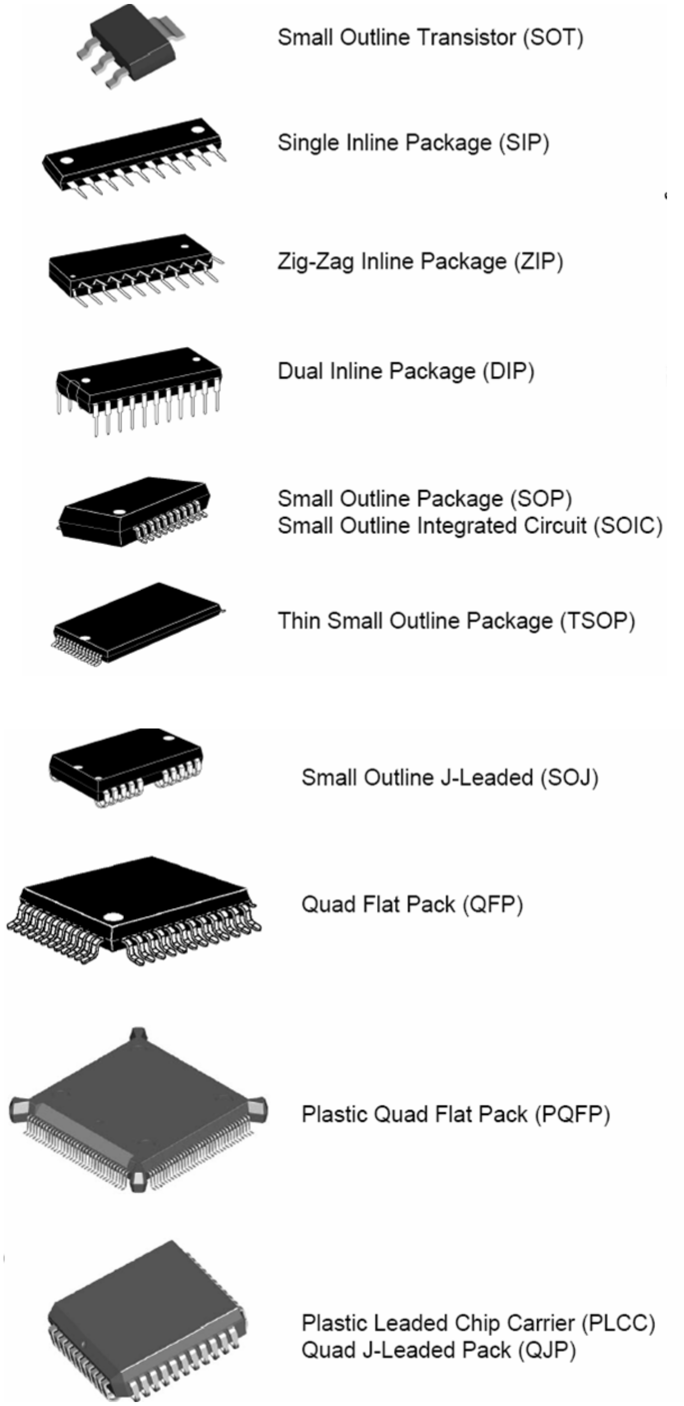


Figure 1.4 : Different Types of Packaging Technology

1.3 Reliability concerns

The current trend in electronic packaging is strongly driven by the market's requirement to lower costs and increase circuit density, enhanced by the necessity to have faster and multi-functional electronic products. These factors give rise to a wide range of mechanical challenges in this field such as extreme operating environments or vibration. The packaging can also be exposed to high temperature changes in high power density devices. Stresses may be induced thermally due to the large mismatch of coefficients of thermal expansion of the various materials in a package, mechanical loading due to the weight of the rest of the product such as the battery or due to shock and drop in its functional life. The challenges are further augmented by the small size of the electronic structure and new materials of interest. These concerns might be responsible for the failures in the packaging through various failure modes like solder joint fatigue, die fracture, severing of interconnects, wire bond failure, delamination, encapsulant cracking, silicon cracking and underfill cracking .

Reliability of electronic packaging is classified into two categories namely thermal reliability and impact reliability. Thermo-mechanical reliability is the process of estimating useful life of electronics subjected to thermal cycling or thermal aging. Reliability studies consist of life predictions of electronics in computers which may undergo thermal cycling during working and shut down modes or in under-the-hood applications of automobiles. Impact reliability deals with the consequences of electronic packaging subjected to drop and shock or vibrations. Mechanical reliability is important in the case of hand-held devices such as cell phones, PDAs and laptops as these devices have high chances of being subjected to drop or in the case of electronics in power tools which are subjected to large vibrations. This thesis essentially deals with impact reliability of electronic packaging when subjected to shock and drop. As in most of the practical situations, one is not independent of the other. The effects of overlapping stress on reliability have also been investigated.

1.4 Shock and Drop Reliability

Emerging trends of portable computing and communication applications towards smaller and lighter form-factors have driven the need for robust-designs under overlapping environments of shock and vibration. Electronic products may be subjected to drop and shock due to mishandling during transportation or normal regular usage. Test methods for drop reliability can be broadly classified into board-level and product-level tests, under constrained and unconstrained or free drop. One such board-level constrained drop test is the Joint Electron Device Engineering Council (JEDEC) test method. The JEDEC test standard [JEDEC 2003] is frequently used to evaluate and compare the drop performance of surface mount electronic components for handheld electronic product applications. Correlation of the board-level tests to product level performance is often challenging. Product-level failures are often influenced by housing design, in addition to drop orientation, which may not always be perpendicular to the board surface [Lim 2002]. Factors such as drop height, mass of the product, impact orientation and the properties of the impacting surface affect the forces and the accelerations that are experienced by the product during impact. Design changes encompass an iterative process for improving the impact resistance of the electronic product. Use of experimental approach to test every possible design variation, and identify the one that gives the maximum design margin is often not feasible because of product development cycle time and cost constraints.

1.5 Digital Image Correlation

Earlier, the measurement of derivatives of field quantities, such as strain, was limited to specific physical locations or discrete target points in an electronic structure. It was not feasible to extract data at a very large number of locations by using discrete targets because of the time consuming process. Techniques such as Moiré Interferometry are an option to get the overall deformation contour, but it is often time consuming and involve expensive grates.

Digital Image Correlation (DIC) is a state-of-the-art method which supercedes the techniques used previously as it consumes less time. This method is used by researchers mainly in the field of thermal reliability. The sample preparation is simple, quick and inexpensive since the test specimens are simply speckle painted with regular paint. The transient deformation is then recorded with the help of high-speed cameras to enable the measurement of full-field strains. This work explores the possible use of DIC to obtain full field strain and displacement contours of a PCB subjected to an impact test to get reliable results.

1.6 Thesis Organization

In this work, impact reliability of electronic devices was investigated by subjecting the test boards to drop tests. An assortment of package architectures that include flex ball-grid arrays, tape array ball-grid arrays (TABGA), chip array ball grid array

(CABGA) and metal lead-frame (MLF) packages was examined. Various test board assemblies were drop tested in 0º JEDEC and 90º vertical drop orientations in order to study the effects of drop angle on the reliability of these packages. The performance of a wide range of alloy systems such as SAC105, SAC305, SAC405, Sn3.5Ag and alloys with impurities like nickel and bismuth were evaluated. Failure analysis was performed on the failed packages to better understand the various failure mechanisms and modes associated with the different factors that affect the reliability of the packages.

Data collection was accomplished with strain gages mounted at discrete locations on the test boards in conjunction with high speed data acquisition systems. Feasibility of the DIC technique to acquire full field strain data on both the board and package side was investigated for electronic assemblies subjected to free drop and constrained drop. Simulations of the drop test were developed and correlated with the experimental data. The drop test was replicated using finite element methods. Models developed include smeared property models and Timoshenko-beam models.

Statistical pattern recognition method (SPR) was implemented to quantify the relative performance based on strain histories obtained from the DIC technique. SPR was used to study the effect of damage progression for various packaging architectures and for various alloy systems. Confidence value of the transient-strain response was computed using Wavelet Packet Energy Decomposition, Mahalanobis distance and Fast Fourier Transform (FFT) approach.

A methodology was developed to identify the damage progression versus number of drops by studying the transient strain history of electronic assemblies from DIC in conjunction with SPR. Manifestation of damage was studied through analysis of failure modes and correlation with degradation in the confidence value. The development of a transient-strain based relative damage index was investigated to establish a method for damage equivalency for the different alloy compositions. The damage proxies developed in this work could be used on strain response from simulations or from experimental data in controlled drop or shock tests.

CHAPTER 2

LITERATURE REVIEW

As the significance of electronics is increasing rapidly, researchers have spent enormous amounts of effort and time to understand the various aspects associated with electronic packaging. Reliability of packaging has become an imperative topic in recent times. Thermal and impact reliability are the two major classifications of this topic. Realistically, these two classifications can not be separated from each other and studies have been conducted on the effect of overlapping stresses on packaging reliability. But for most research purposes, they are investigated individually. Impact reliability at board level as well as product level is considered for applications involving shock and drop during the functional life of the products, such as hand held devices. Factors like drop orientation, surface finish and alloy systems affect drop reliability and researchers have investigated these aspects using tools like failure analysis. Full field strain contours of an electronic system under different loading conditions give important insight into several aspects affecting reliability. Various techniques for acquiring this data for example, interferometry and speckle photography were investigated in the past. Newer techniques like Digital Image Correlation are also gaining importance due to advantages of reduced cost and lower sample preparation time. These techniques are being investigated to be more applicable to this field.

As it is not feasible to experiment and study the influence of different combinations of factors that affect reliability simultaneously, finite element analysis is considered as a valuable instrument in understanding the different aspects causing failure in electronic packaging. Prognostic methods to predict the life of a package when subjected to different types of loading conditions has gained attention in the recent past, especially in critical areas like military applications where the functioning of the electronic devices is crucial.

2.1 Board and Package Level Testing

Reliability of solder interconnects in electronic devices subjected to shock and drop impact is one of the most significant factors in hand held devices since they are more prone to experience these loading conditions. Modern portable devices are equipped with increased number of new and more powerful capabilities causing the components to dissipate more heat. This results in a considerable rise of the local temperatures of the products. As products are most likely to be dropped when they are being used, it is imperative to investigate the effect of drop testing the component boards at different temperatures as done by Mattila et. al. [Mattila 2007]. On the other hand, Lall et. al. [Lall 2006] investigated the effects of overlapping stress on packaging by subjecting them first to thermal loading followed by drop tests.

To keep it simple, the two loading conditions, thermal and impact are analyzed independently. The most realistic shock tests would be product-level tests on the complete product to assess its performance under drop impact. But these tests are very expensive. Package-level tests are simplified real life impact scenarios and serve as an acceptable replacement of board-level drop tests that save cost and time [Yeh 2005, 2006, Ong 2003]. A variety of tests for example, bending impact [Kim 2006], ball impact [Lai 2006], pendulum impact or Charpy [Ratchev 2007], high speed bend [Seah 2006], micro impact [Ou 2005], cold ball pull and high speed shear [Johnson 2007] were investigated as tools to study impact toughness, fracture toughness and other factors contributing to impact reliability of packaging. Results from some of these tests were compared with each other for instance, impact and cold ball pull [Zaal 2007], cold ball pull and high speed shear [Johnson 2007], shear, ball pull and monotonic bend [Geng 2004].

Amongst the mechanical tests mentioned above, the drop test is the most prominent. JEDEC established a standard [JEDEC 2003] for drop tests to specify the drop impact pulse and test board configuration. This generated a common ground for an assortment of semiconductor component manufacturers to compare the solder joint reliability under impact. This standard has been widely accepted and used by researchers to compare their reliability results. However, the JEDEC standard has some limitations. One of the limitations is that it has too many loading conditions, which may be unnecessary, and results in reduced sample sizes of each loading condition for statistical analyses. To overcome this drawback, Zhao et. al. [Zhao 2007] proposed an alternative board design with only one loading condition and a sufficiently large sample size, while Tsai et. al. [Tsai 2007] demonstrated applications of the response spectra to a JEDEC standard drop test board subjected to different JEDEC drop test conditions. In spite of its drawbacks, JEDEC is the most frequently used drop test standard.

The JEDEC standard specifies that the test vehicle should be mounted with the package side facing downwards to create a more critical loading condition [Yeh 2004]. It also states that the drop orientation should be horizontal or at zero degrees during the drop test. But this is not the only angle at which a product might hit the floor. Experiments conducted on cell phones by Liu et. al. [Liu 2005], Seah et. al. [Seah 2002] and Ong et. al. [Ong 2003] have shown that impact reliability is very sensitive to the impact angle of the product. Chong et. al. [Chong 2005] reported that pin-supported vertical drop of PCB generated much lower PCB flexing and impact stress damage to the solder joints compared to the horizontal orientation drop.

2.2 Finite Element Models

With the continuous decrease in the size of electronic devices, it is expensive, time consuming and demanding to carry out drop tests to directly detect failure modes and identify their drop behaviors. Due to the complexities involved in direct measurement of the response variables in solder joint during drop and shock events, simulation is gaining more importance in the present times. Different types of tests such as cold ball pull test [Zaal 2007] were simulated to use it as a prognostic tool and predicted the behavior of electronic packaging subjected to various loading conditions.

Several techniques to simulate electronic packaging subjected to drop test have been developed by researchers. Yeh et. al. [Yeh 2004] used an implicit solver by translating the input acceleration pulse into effective support excitation load on the test vehicle, making the method numerically efficient and accurate. Many scientists have also used the explicit finite element solver to replicate the dynamic drop event [Lall 2004, 2005, Xie 2002, 2003, Wu 1998, 2000]. Other techniques used include implicit global models [Irving 2004, Pitaressi 2004, Syed 2005], the global-local sub model [Wang 2004, Tee

2003, Wong 2003, Zhu 2001, 2003, 2004], smeared models [Jie 2004, Lall 2006], explicit-implicit sequential model [Zhu 2005] and models with solid elements using sub modeling [Wong 2002]. The global-local sub model has detailed models to investigate the.critica1 failure location and components and a corresponding simplified model to simulate the global response and local effects of the system. Smeared models have cluster of solder balls represented by a single column and are modeled with one 3D continual layer to represent the discrete solder joints. Tan et. al. [Tan 2005] modeled the IC package, PCB, and solder interconnects with varying levels of detail to conclude that the range of deviation in the solder stress in the three models used was as much as 40%. Zhu et. al. [Zhu 2005] examined three drop tests models namely, bare board drop, board with fixture drop or shock, and system level phone drop using the sub-modeling and explicit-implicit sequential modeling techniques.

2.3 Alloy compositions and Surface Finish

Due to the implementation of Restriction of Hazardous Substances (RoHS) in electrical and electronical equipment directive, lead-free solder replaced SnPb solder alloy. This execution of banning lead in the electronics industry resulted in adopting lead-free solder in spite of SnPb, which was used as the primary solder alloy world wide in the past, out-performing lead free alloys in impact resistance. Jang et. al. [Jang 2007] reported that the reason for better performance of SnPb under impact loading conditions was due to the lesser strain rate sensitivity of the bulk solder. The most common lead free alloys used today are different compositions of the Sn-Ag-Cu (SAC) alloy. Several researchers proved that SAC alloys with lower silver(Ag) content demonstrate higher resistance to impact [Kim 2006, Zhao 2006, Kim 2007, Masicat 2007, Chen 2007, Pandher 2007]. Lower Ag content implies lower modulus of elasticity which in turn implies lower stiffness giving the solder greater capability to absorb large amounts of shock [Iyer 2007]. Another lead-free alternative, eutectic Sn-Ag (Sn-3.5Ag), is gaining increased recognition as a solder alloy because it provides superior component and board level performance, while not showing the metallurgical deficiencies observed in the SAC materials.

Researchers have also investigated numerous impurities which can be added to the solder alloys to improve properties such as impact resistance and fracture strength in the solder interconnect under shock loading. Addition of some of these elements in SnAgCu based solder can significantly improve the drop performance, primarily because of differences in intermetallic compound (IMC) formation and the strength of solder alloys. Nickel (Ni) [Kim 2006] is one such impurity to improve the reliability of electronic packaging by retarding the formation and growth of the Cu_3Sn intermetallic layer at the pad-solder interface to minimize the potential of void formation and failure at the IMC layer [Syed 2006]. Some of the other elements which have been investigated are Cobalt (Co), Antimony (Sb), Zinc (Zn), Aluminum (Al), Germanium (Ge), Indium (In) and Bismuth (Bi).

Sn-Zn-Al and other alloys were observed to be potential choices for lead-free solder alternatives [Geng 2004]. Addition of Ni softens the SnAgCu alloys to improve shock reliability [Huang 2007] and addition of copper leads to brittle fractures across the solder ball interface [Anand 2004]. Tsai et. al. [Tsai 2005] asserted that SnAg solder demonstrates the highest impact fracture strength, while BiSn solder exhibits the lowest strength when compared with SAC alloys. Lee et. al. [Lee 2005] reported an improvement in impact reliability after adding Nickel and Germanium to SAC alloys. SnAgCu and SnAgCuNi interconnections with a Copper - Organic Solderability Preservative (Cu-OSP) coating prove to be equally reliable and superior to the SnAgCuBi interconnections while with the Electroless Nickel Immersion Gold (ENIG) coating the SnAgCu interconnections were the most reliable. The SnAgCuBi interconenctions were the second most reliable and the SnAgCuNi interconnections were the least reliable as reported by Mattila et. al. [Mattila 2007]. Pandher et. al. [Pandher 2007] concluded that the combination of Ni and Cr offered high drop shock reliability and excellent tarnish resistance, while the combination of Ni and Bi provided over 20% improvement in solder sphere spread on Cu-OSP. The improvement of the solder sphere spread was also maintained for the Bi, Ni, and Cr combination.

Surface finish was investigated as a key player affecting the reliability of packaging. Studies revealed a strong influence of different intermetallic compound formation on soldered assemblies' drop durability. Some of the most commonly used pad finishes include Hot Air Solder Leveling (HASL), Electroless Nickel Immersion Gold (ENIG), Immersion Gold (ImAg), Immersion Tin (ImSn) and Organic Solderability Preservative (OSP). Mattila et. al. [Mattila 2007] examined the combination of surface finishes Cu-OSP and ENIG with SAC alloys doped with Ni and Bi at three different temperatures under impact loading. Results showed that interconnections with the Cu-OSP coating were more reliable than ENIG finish. Other studies [Chai 2005, Kim 2006, Zhao 2006, Zhao 2007^{b}] also reported similar conclusions. ImSn was compared with Direct Solder on Pad (DSOP) to infer that Ball Impact Test (BIT) characteristics are greater for samples with the ImSn substrate pad finish [Lai 2007]. A comparison of OSP, ENIG and ImSn was investigated to conclude that OSP supersedes the performance of the other finishes [Chong 2005]. Not only the individual effect of surface finish, but also a combination with the different solder alloys was investigated. Syed et. al. [Syed 2007] concluded that SAC125Ni solder, with much better performance for Cu-OSP finish, does not show a significant improvement over SAC305 with the ENIG finish.

2.4 Failure Analysis

Failure analysis provides significant insight on mechanisms that cause deterioration in reliability of electronic packaging. Prediction of failure was investigated using fracture mechanics [Shah 2004], von-misses stress [Tee 2004], and board-strain based damage index [Lall 2005]. Failure in the interconnect occurs at the interface close to the device or board side as these are the highest stressed locations in the joint. The extent of damage and failure modes varies for different alloy systems. The impact failure modes of SnPb solder were predominated by bulk failures as the bulk solder deformation absorbs some of the impact strain and cracks through solder rather than through the interfacial intermetallic. Lead-free solder, on the other hand, exhibits a mixture of IMC and bulk failure that occur along the bond interface [Tsai 2005]. The imposed strain in the SnAgCu joints moves away from the bulk solder into the lower strength brittle IMC as the apparent strength of the solder increases at higher strain rates [Jang 2007]. Comparison of the failure modes of SAC alloys indicated that crack propagation through the bulk solder was more in SAC105, due to a lower elastic modulus, than brittle IMC layer in SAC405 [Kim 2007]. Failures at the intermetallic layer on the package side and the laminate beneath the pad location on the board side were predominant in SAC305 [Iyer 2007].

The addition of impurities and different combinations of alloy systems and surface finishes cause variations in failure mechanisms. A comparison of the failure modes in SAC305 and Sn1.2Ag0.5Cu0.05Ni shows an increase in drop reliability and a shift in fracture mode from interface failure to bulk failure [Kim 2006]. Syed et. al. [Syed 2007] compared a number of solder alloys to illustrate that the interfacial failure on the package side was the primary mode of failure for SAC305 with the ENIG surface finish. The failure shifted to board side through the bulk solder for the SAC125Ni solder alloy in combination with Cu-OSP.

2.5 Digital Image Correlation (DIC)

High speed photography is defined as the science of capturing an extremely fast phenomenon with the help of cameras capable of acquiring images at a very high frame rate. Some of the common applications of high speed photography include measurement of deformation and strain in sheet metal forming analysis, automotive crash testing, rail vehicle safety [Kirpatrick 2001], air-plane safety [Marzougui 1999], and modal analysis of blades and disks. Other applications are shearography using laser NDT for rapid honeycomb delamination tests, dynamic fracture phenomenon, tire tests, rotating components, exhaust manifolds, split Hopkinson bar tests and package integrity or hermiticity (MIL-STD-883) tests. High-speed cameras in high speed photography measure impact speed, force, deformation due to shock, and thermal loading. It is also used for quantitative evaluation of in-plane deformation characteristics of geo-materials

[Watanabe 2005] and in medical fields to assess local failure of bone by implementing mechanical compression testing of bone samples [Thurner 2005].

Measurement of full field dynamic responses of a test specimen during events such as impact and vibration was always a challenge. A range of optical methods were used in the past to measure full-field displacement and deformation gradient distributions. These non-contact methods include interferometric techniques and non-interferometric techniques, like speckle photography [Smith 1993], speckle interferometry [Cote 2001], Moiré interferometry [Ho 1997, Wang 2002], holographic interferometry [Petrov 1996], and Twyman-Green and shadow Moiré interferometry [Hartsough 2007]. Researchers have used Twyman-Green and shadow Moiré interferometry to investigate various aspects such as warpage of non-conventional packages subjected to reflow and assembly processes [Hartsough 2007] and out-of-plane deformation of the bi-material specimens during moisture absorption [Tsai 2007[b]]. High precision optical techniques for example, shadow moiré, moiré interferometry, reflection moiré and electronic speckle pattern interferometry were considered as efficient methods to predict warping behavior of bare substrates [Wen 2007]. Optical interferometry was used not only for strain measurement, but also for acquiring 3-D surface height maps [Braunisch 2007] and surface contours of interposer bonded in a package [Marinis 2007].

Digital Image Correlation (DIC) is a new technique based on tracking a geometric point before and after deformation that enables full field strain and displacement measurement during a transient event such as shock and impact. Tracking points on the test vehicle is done by speckle coating the surface of interest. Studies reveal that size, consistency and density of the speckle pattern affect the accuracy of the method [Zhou

2001, Amodio 2003, Srinivasan 2005]. This method is extremely favorable in comparison to the use of strain gage which measure strain only at localized points on the specimen. It is also advantageous over interferometry as this technique is non-contact and has reduced sample preparation time and lower costs. The DIC technique was used in the electronics industry for various applications. Investigating stresses in solder interconnects of BGA packages under thermal loading [Zhou 2001, Yogel 2001, Rajendra 2002, Zhang 2004, Zhang 2005, Xu 2006, Bieler 2006, Sun 2006], stresses and strain in flip-chip die under thermal loading [Kehoe 2006], and monitoring crack propagation and calculating Young's modulus of the underfill at elevated temperatures during four-point bending tests [Park 2007[a], Shi 2007] are some of the areas for which this technique has proven to be valuable. The DIC method applied to high resolution SEM images has also been used to study the stresses released at the component surface before and after ion milling [Vogel 2007]. In addition, DIC technique was used in the study of behavior of materials like polyurethane foams. [Jin 2007], polymer films [Park 2007[b]] and coating materials [Thompson 2007]. It was also used for material characterization at high strain rates [Tiwari 2005]. Although this technique has become popular in the thermal area of electronic packaging, it is fairly new in the field of dynamics. DIC systems integrated with high speed cameras are being examined as helpful tools to acquire and analyze images taken during a drop event to obtain responses such as dynamic deformation, shape and strain over the entire surface of printed circuit boards not only in the horizontal configuration [Lall 2007, Miller 2007, Park 2007[c]] but also in the vertical drop orientation [Scheijgrond 2005].

CHAPTER 3

HIGH SPEED DIGITAL IMAGE CORRELATION AND SIMULATION TECHNIQUES FOR TRANSIENT STRAIN MEASUREMENT IN ELECTRONICS SUBJECTED TO SHOCK AND DROP

3.1 Introduction

Electronic components are subjected to shock, vibration and drop-impact during shipping, handling and normal usage. Measurement of transient dynamic deformation of the electronic assemblies during shock and vibration can yield significant insight into the understanding of development of failure envelopes. In this chapter, measurement of deformation kinematics with the help of ultra high-speed data acquisition and video systems are examined. Various test board assemblies were drop tested in 0^0 JEDEC and 90^0 vertical drop orientations. Electrical continuity was measured for all the daisy chained packages during the transient event. Explicit finite element models were used to assess the reliability and performance of the electronic boards. Experimental data was correlated with the finite element results.

3.2 Experimental Test Vehicle

The test vehicles used in this study included boards - A, B, C, D, and E as shown in Figure 3.1. Test board-A was a bare board which was designed to accommodate 7mm -

32 I/O and 7mm - 44 I/O MLF packages. Test board-B was populated with five packages which included, two 10mm - 144 I/O BGA, two 16mm - 280 I/O BGA and one 6 mm - 56 I/O BGA packages. Test board-C included, 15mm CSP, 16mm C2BGA, 27mm BGA, and PQFN packages. Test board-D was populated with ten 8mm - 0.5mm pitch 132 I/O flex-substrate chip scale packages. Each of the boards was populated only on one side of the printed circuit board. Test board-E was populated with three different packages: 17mm - 256 I/O PBGA, 18mm - 192 I/O CABGA and 6 mm - 56 I/O CABGA packages. Test boards A, B and E were FR – 4 boards with an identical dimension of 8” x 5.5” x 0.06”. For these three test boards, lead-free solder alloy 95.5Sn4.0Ag0.5Cu (SAC 405) was used. The details of all the packages are given in Table 3.1, Table 3.2 and Table 3.3.

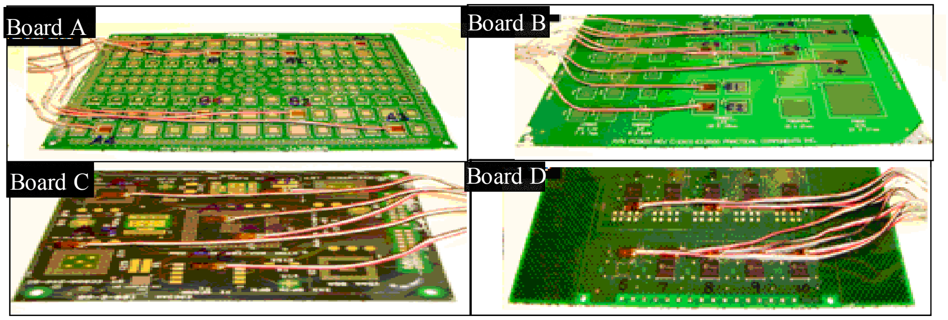


Figure 3.1: Test Boards A, B, C and D

Table 3.1: Package Architecture of 6mm, 10mm and 14mm BGAs

	6 mm, 56 I/O CABGA	**10mm, 144 I/O BGA**	**14mm, 92 I/O CABGA**
Test Vehicle	Board B, E	Board B	Board E
Ball Count	56	144	192
Ball Pitch	0.5 mm	0.8 mm	0.8
Die Size	4 mm	7 mm	6.35 mm
Substrate Thickness	0.36 mm	0.36 mm	0.36 mm
Substrate Pad Diameter	0.28 mm	0.34 mm	0.34 mm
Substrate Pad Type	NSMD	NSMD	NSMD
Ball Diameter	0.32 mm	0.48 mm	0.48 mm

Table 3.2: Package Architecture of 16mm and 17mm BGAs

	16mm, 280 I/O BGA	**17mm, 256 I/O PBGA**
Test Vehicle	Board B	Board E
Ball Count	280	256
Ball Pitch	0.8 mm	1 mm
Die Size	10 mm	6.35 mm
Substrate Thickness	0.36 mm	0.36 mm
Substrate Pad Diameter	0.34 mm	0.34 mm
Substrate Pad Type	NSMD	NSMD
Ball Diameter	0.48 mm	0.5 mm

Table 3.3: Package Architecture of 32 I/O and 44 I/O MLF Packages

	7mm, 32 I/O MLF	**7mm, 44 I/O MLF**
Test Vehicle	Board A	Board A
Lead Count	32	44
Pitch	0.5 mm	0.65 mm
Die Size	2.5 mm	3.25 mm
Substrate Thickness	0.9 mm	0.9 mm
Substrate Pad Thickness	0.1 mm	0.1 mm
Substrate Pad Type	NSMD	NSMD

Three different lead-free surface finishes, namely, ImAg, ENIG and ImSn for test board B were examined. All the packages used in the test configuration were daisy-chained. In all cases, multiple boards were tested in each test configuration. Test boards were exposed to sequential stresses of either thermal cycling or thermal aging, followed by shock impact to determine the effect of cumulative damage of the overlapping stresses on the interconnect reliability. Thermo-mechanical cycling included exposure from -40^{o}C to 125^{o}C for 100 cycles. The duration of each cycle was 90 minutes with 25 minute ramps between temperature extremes and 15 minute dwell periods at each temperature extreme.

The test vehicle F used for this study is shown in Figure 3.2. The board was made up of FR-4 with dimensions of 5.2” x 3.03” x 0.04”. The test vehicles were populated only on one side. Each of the test boards had 15 Chip-Array Ball-Grid Array (CABGA) packages with an I/O count of 100 and a pitch of 0.8mm. Details of the package are shown in Table 3.4. The interconnect array configuration of the 10mm CABGA is shown in Figure 3.3. All the packages used in the test configuration were daisy chained. The surface finish of the test boards was ENIG on the populated side and Cu-OSP on the unpopulated side. Six different alloy compositions including Sn1Ag0.5Cu (SAC105), Sn3Ag0.5Cu (SAC305), Sn0.3Ag0.7Cu (SAC0307), Sn0.3Ag0.7Cu-Bi (SACX), Sn0.3Ag0.7Cu-Bi-Ni (SACX-Plus) and 96.5Sn3.5Ag (SnAg) were examined for this board. The compositions of the various alloy systems are given in Table 3.5.

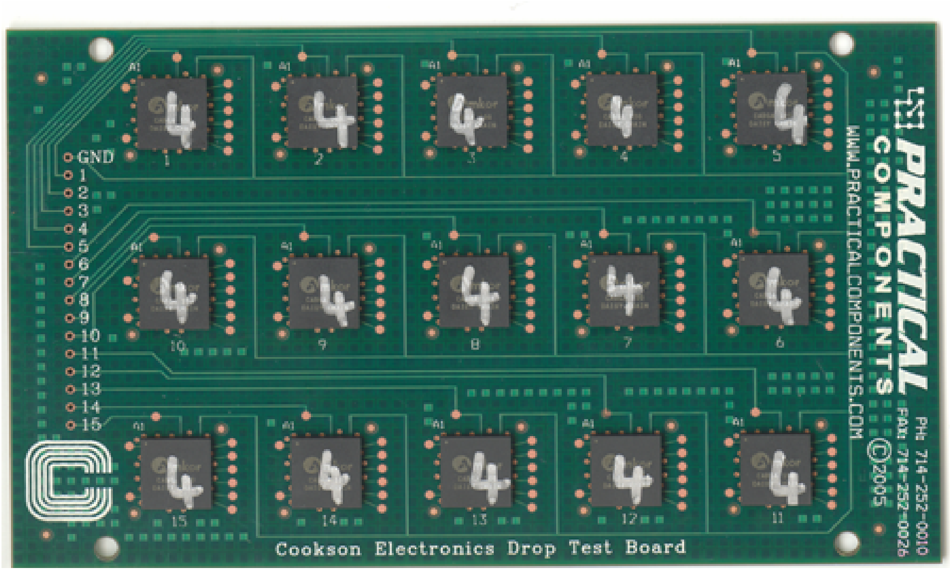


Figure 3.2: Test Vehicle

Table 3.4: CABGA Package Details

Ball Count	100
Ball pitch(mm)	0.8
Die Size(mm)	5.55
Substrate Thickness(mm)	0.232
Substrate Pad Type	NSMD
Ball Diameter(mm)	0.48

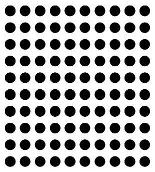


Figure 3.3: Interconnect Array Configuration of the 10mm-100 I/O CABGA Package

Table 3.5 : Lead Free Alloy Compositions

Alloys	**Composition**
SAC105	Sn: 98.5%,Ag: 1%, Cu: 0.5%
SAC305	Sn: 96.5%,Ag: 3%, Cu: 0.5%
SAC0307	Sn: 99%,Ag: 0.3%, Cu: 0.7%
SACX	Sn: 98.9%,Ag: 0.3%, Cu: 0.7%, 0.1% Bi
SACX-PLUS	Sn: 98.8%,Ag: 0.3%, Cu: 0.7%, 0.1% Bi, 0.1%Ni
Sn3.5Ag	Sn: 96.5%,Ag: 3.5%,

3.3 Detection Of Damage Progression

The test boards were subjected to controlled drop. Repeatability of drop orientation is critical while measuring a repeatable response. Significant effort was invested in developing a repeatable drop set-up because small variations in the drop orientation could produce significantly varying transient-dynamic board responses. Repetitive readings were taken to determine repeatability of the controlled drop orientation. Repeatability was characterized and is shown in Figure 3.4, Figure 3.5 and Figure 3.6. Tests were performed in two different drop orientations. The 0^o drop was done in the JEDEC configuration, involving a 1500g, 0.5 millisecond, half-sine input pulse. The 90^o drop was a free drop with a weight attached to the circuit-board assembly to simulate the weight of the battery and the components in a typical product board. For this arrangement, the test vehicle was attached to the drop table with the help of a nylon string.

Weights were added to the printed circuit board F when dropped in the JEDEC drop orientation to simulate the effect of shields. Weights were in the form of two metal strips attached at equal distances from the center of the board. Strain gages were placed on the populated boards on the package side and on the board side at different locations to measure longitudinal strain on the boards. One such arrangement along with the numbering scheme of packages for test structure F has been shown in Figure 3.7. The drop tower along with a test board instrumented with strain sensors is shown in Figure 3.8.

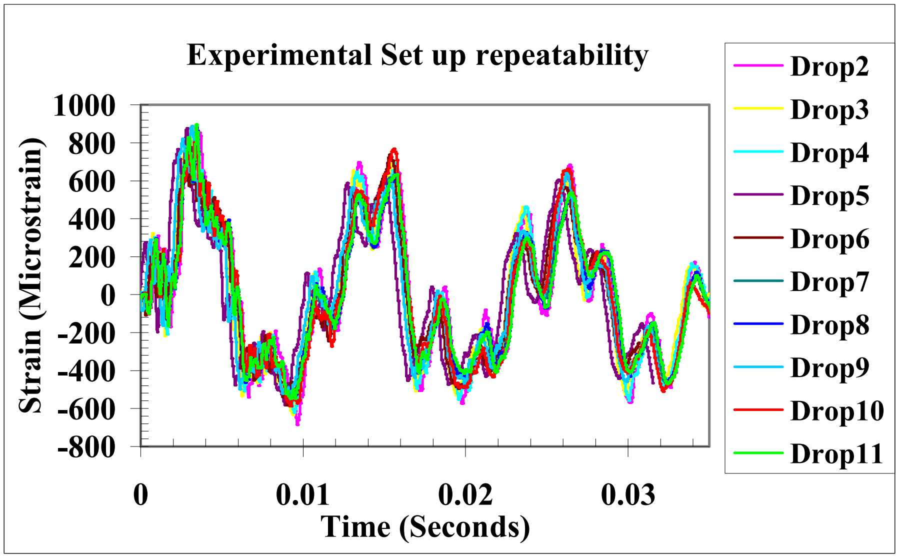


Figure 3.4: Strain Repeatability for Test-Board A

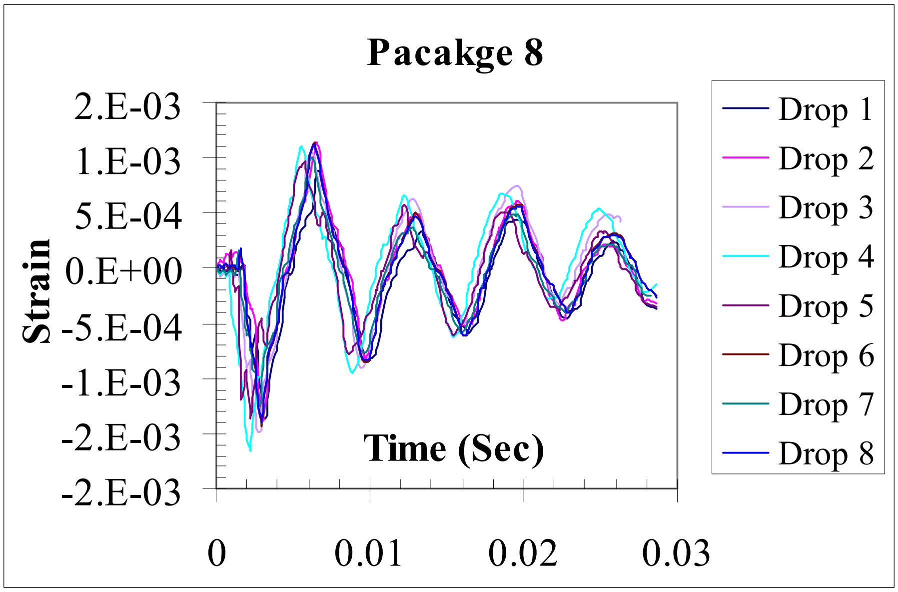


Figure 3.5: Repeatability Plot at Package Location 8 on test board F

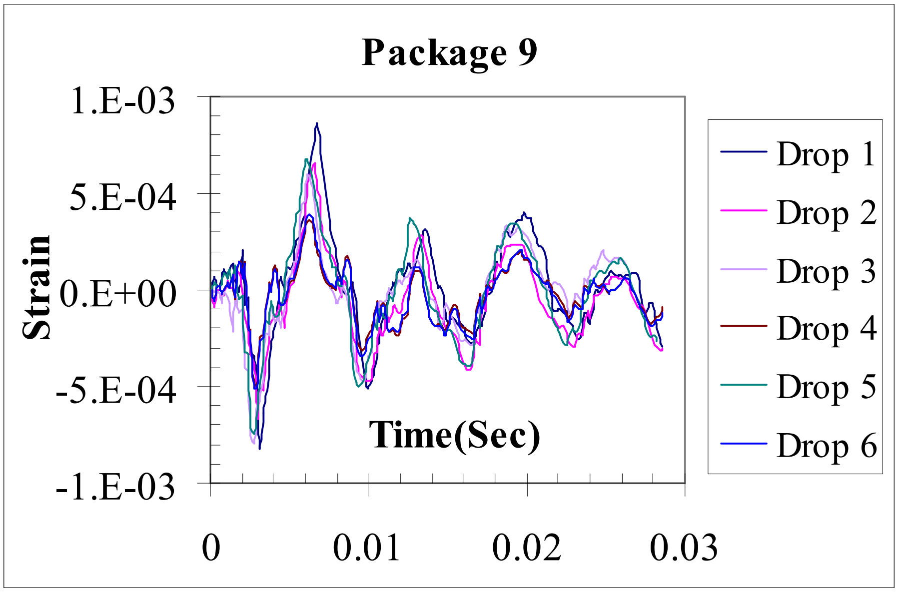


Figure 3.6: Repeatability Plot at Package Location 9 on test board F

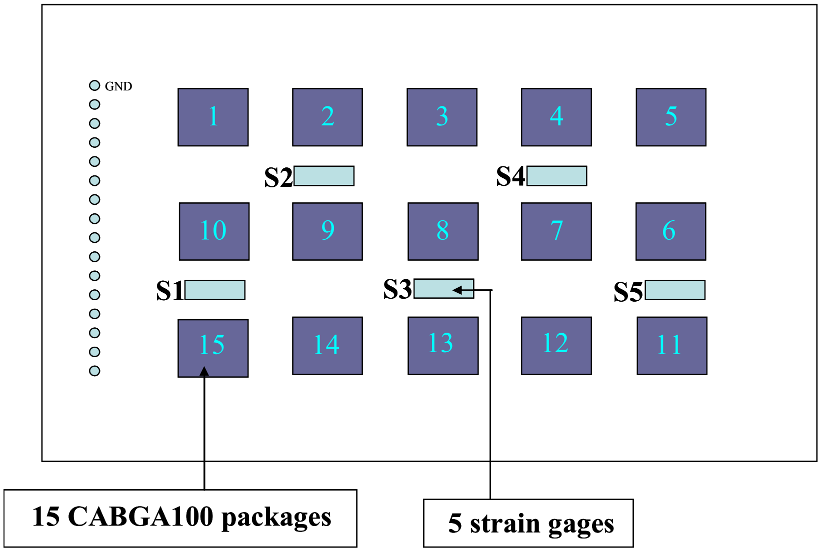


Figure 3.7: Location of Gages and Numbering Scheme of Packages on SAC305 Alloy Specimen Board on Test Board F

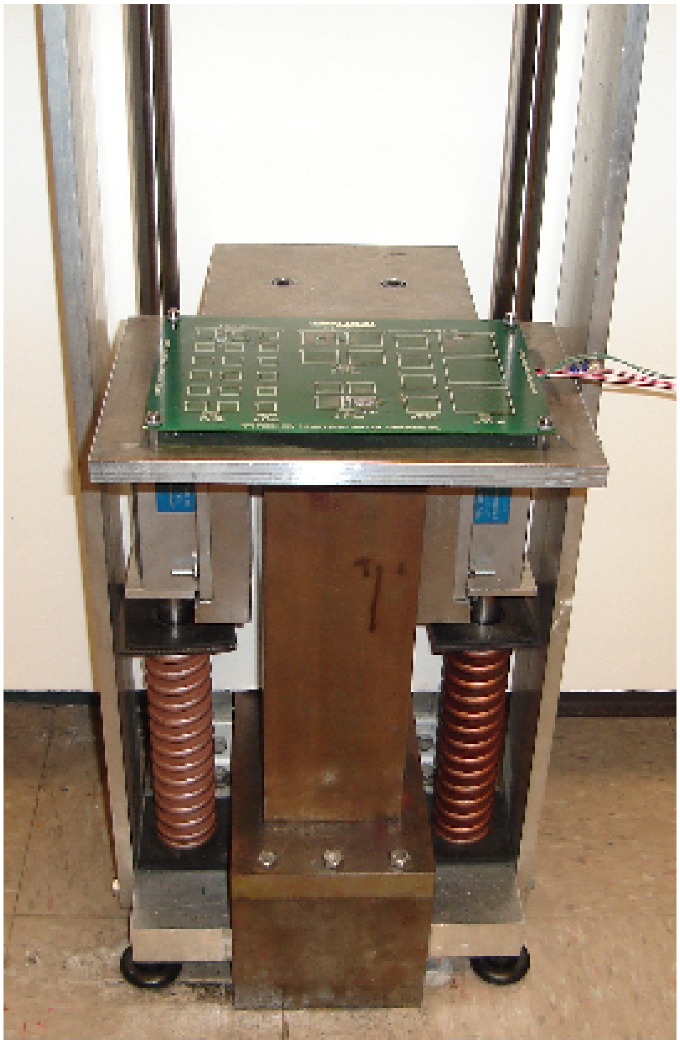


Figure 3.8: Experimental Set-up for Controlled JEDEC Drop of Test Board B

Strain and continuity data were acquired during the drop event using a high-speed data acquisition system operating at 2.5 to 5 million samples per second. The drop-event was simultaneously monitored with an ultra high-speed video camera operating at 30,000 frames per second. Targets were mounted on the edge of the board to allow high-speed measurement of relative displacement during the drop event as shown in Figure 3.9. Responses, namely, strain, displacement, orientation angle, velocity, acceleration, and continuity data were acquired simultaneously. An image tracking software was used to quantitatively measure displacement during the drop event. Figure 3.10 shows a typical relative displacement plot measured during the drop event. The plot trace subsequent to the white scan is the relative displacement of the board targets with respect to a specified reference. In addition to relative displacement, velocity and acceleration of the board prior to impact were also measured.

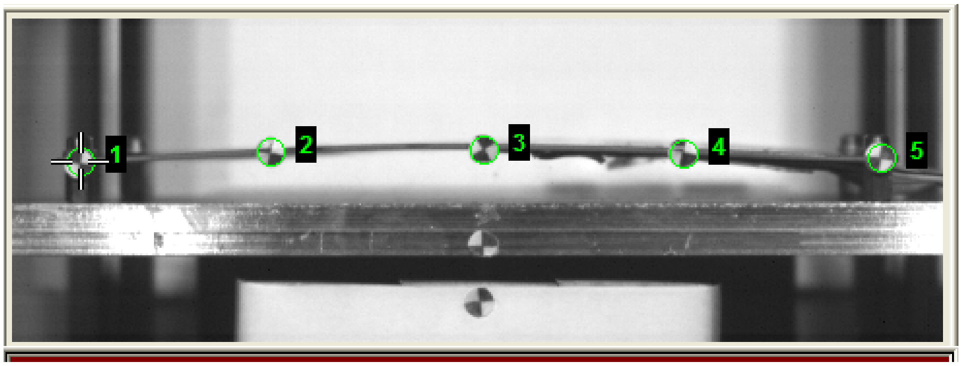


Figure 3.9: Board B Mounted with Targets for Relative Displacement Measurement

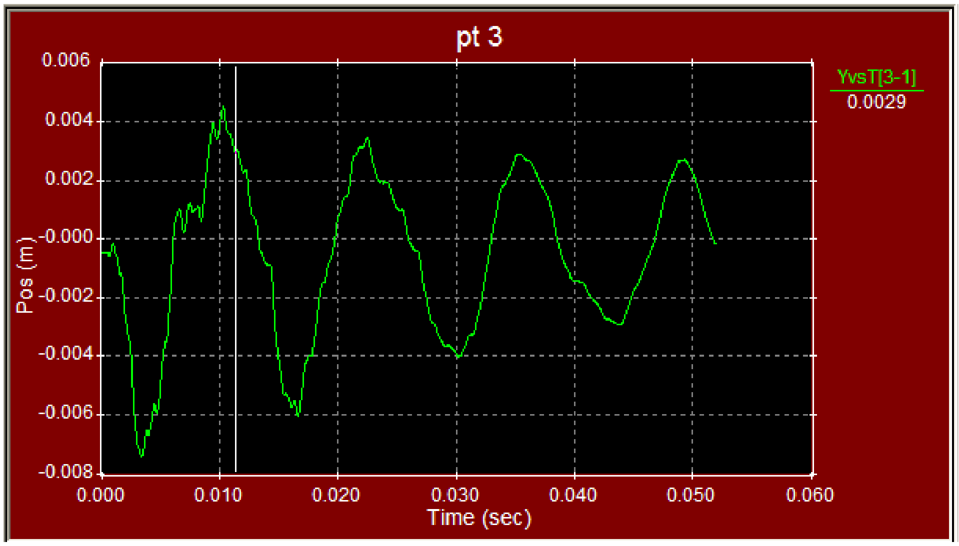


Figure 3.10: Relative Displacement of Test Board B Subjected to JEDEC Drop

Figure 3.11 shows the package-strain history during the impact test of board B in the JEDEC drop orientation at the 16mm - 280 I/O package location. Failure in the device was identified as an increase in voltage drop. Similar plots, Figure 3.12 and Figure 3.13, have been shown for test structure F. Different locations on a particular test board exhibited different strain histories during the same drop. Packages at different locations on a single test vehicle failed at different cycle counts. However, the strain histories were very consistent and repeatable at the same component location on the test board for various drops. The strain history was also very repeatable for the same component location across various test boards.

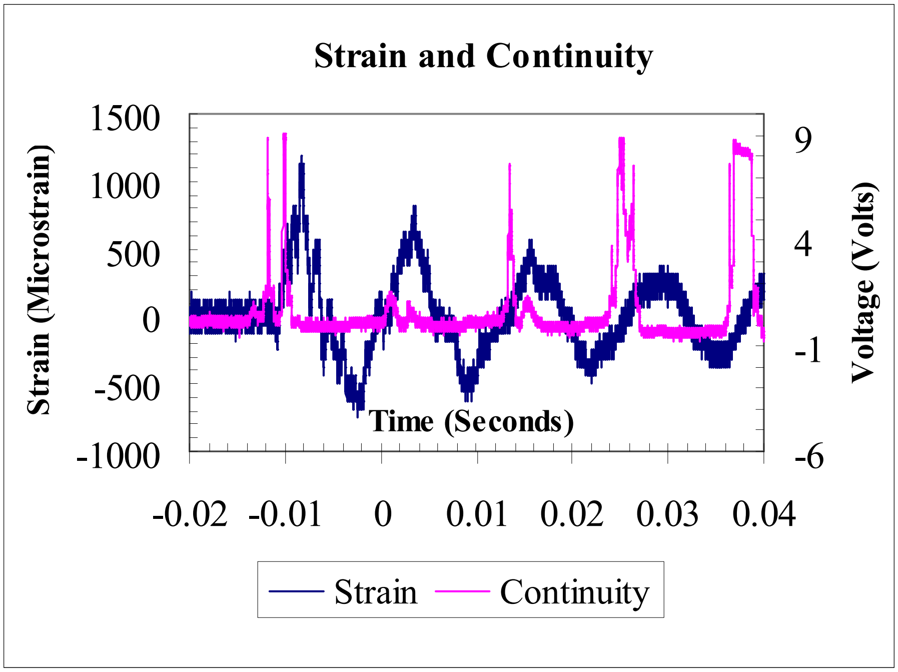


Figure 3.11: Package Strain and Continuity History in JEDEC drop-shock Orientation, for Test board B

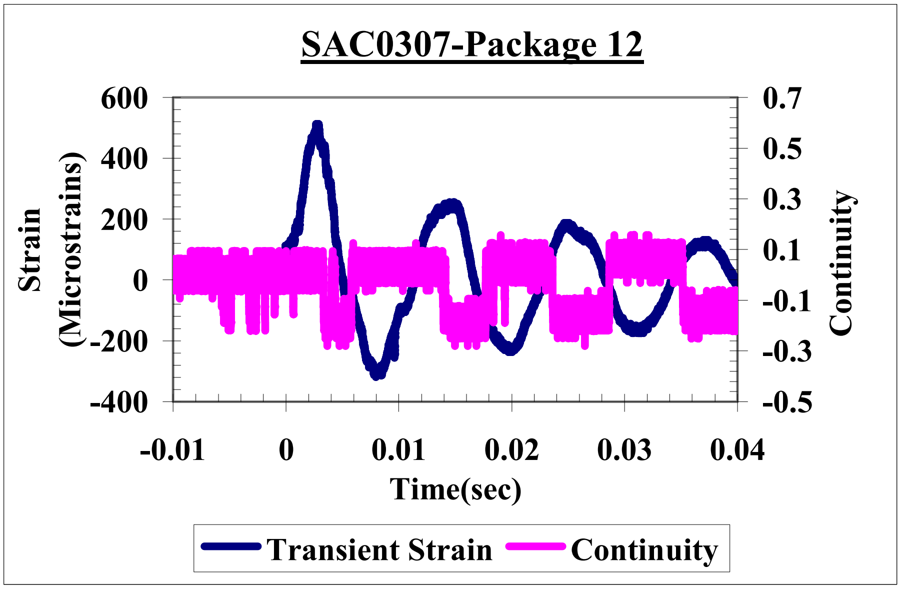


Figure 3.12: Strain and continuity history at Package 12 for SAC0307 alloy system on Test Board F

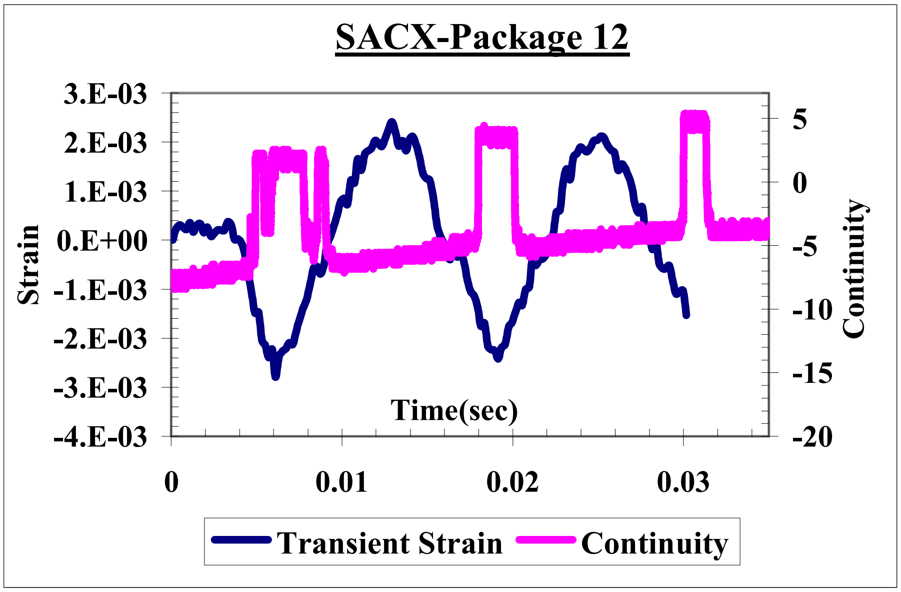


Figure 3.13: Strain and continuity history at Package 12 for SACX alloy system on Test Board F

3.4 Digital Image Correlation (DIC)

Digital image correlation is an optical method to measure full field deformation on the surface of an object. The technique is based on tracking a geometric point before and after deformation and using it to calculate the displacement field. This method has been used in the past for various applications such as for acquiring stress and strain in solder interconnects and for material characterization under thermal loading. However, data is scarce for the behavior of a printed circuit board (PCB) transient dynamics in shock, which is a major reliability issue, to study the failures at the solder interconnects in portable electronics. Board-level reliability of an electronic assembly has never been studied using this technique when subjected to drop in vertical and JEDEC orientations.

In this work, DIC was used for capturing the shock-deformation in electronic assemblies by tracking the speckle pattern in small regions called subsets or sub-images. High speed cameras were used to capture the motion of assemblies before and after deformation. The undeformed and deformed images are called the original image and deformed image respectively. A subset around a reference pixel O in the reference image was then compared with the corresponding subset in the deformed image using a predefined correlation function to describe the difference between the two digital sub-images. The full field displacement contour was obtained by shifting the reference pixel in the original image and applying this method to all the other pixels of the images. Figure 3.14 shows the digital images of the speckle patterns before and after deformation, obtained using high speed cameras.

The relationship between the reference image $I_1(r)$ and the deformed image $I_2(r)$ is given as follows:

$$I_2(r) = I_1[r - U(r)] \tag{3.1}$$

$$I_1(r) = I_2[r + U(r)] \tag{3.2}$$

where U(r) is the displacement vector at pixel r = $(x,y)^T$. An algorithm based on the mutual correlation coefficient or other statistical functions was used to correlate the change in a reference pixel in the original image and the corresponding reference pixel in the deformed image.

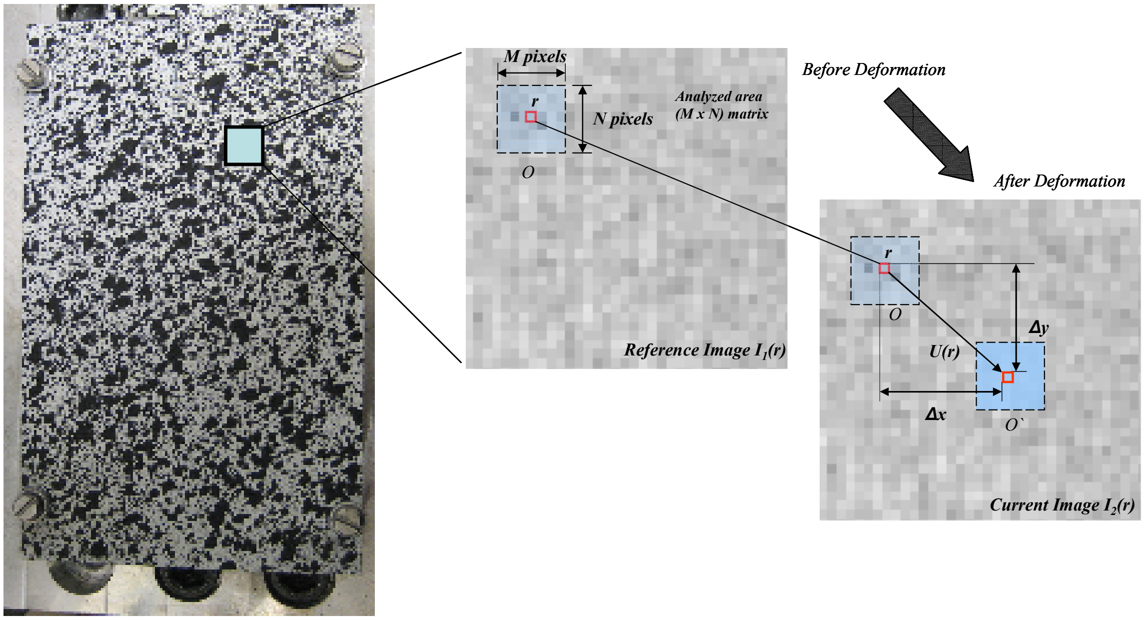


Figure 3.14: DIC Principle

Three such typical correlations are absolute difference, least square and cross correlation. They were defined as follows:

Absolute difference:

$$C_A(r') = 1 - \frac{\iint_\Omega \left| I_2(r+r') - I_1(r) \right| dr}{\iint_\Omega I_1(r) dr} \tag{3.3}$$

Least square:

$$C_L(r') = 1 - \frac{\iint_\Omega [I_2(r+r') - I_1(r)]^2 dr}{\iint_\Omega I_1^2(r) dr} \tag{3.4}$$

Cross-Correlation:

$$C_C(r') = 1 - \frac{\iint_\Omega I_1(r) I_2(r+r') dr}{\left[\iint_\Omega I_1^2(r) dr \iint_\Omega I_2^2(r+r') dr\right]^{1/2}} \tag{3.5}$$

where Ω (M x N) is the area of the sub-image around reference pixel r, r\` is the current pixel, $C_A$(r\`) is the current absolute difference correlation function, C_L(r\`) is the current least square correlation function, and $C_C$(r\`) is the current cross correlation function. The cross-correlation functions provided the correspondence between matching subsets in images of the undeformed and deformed states. It was an iterative spatial domain cross-correlation method. This method maximized the cross-correlation coefficient between a subset in the reference image I_1 and the deformed image I_2. In practice, the absolute and least square correlation functions require less computation since constant brightness is assumed. In order to handle illumination changes, normalized cross-correlation is used, which is computationally demanding.

Correlation functions determine the difference between the current pixel O' and the reference pixel O, by matching the two sub-images. To estimate sub-pixel displacements, U(r) in a sub-image corresponding to a pixel $r_0 = (x_0, y_0)^T$ in the current image $I_2(r)$ is assumed to be constant [Davis 1998].

$$U(r) = U(r_0) = U_0 = (u_0, v_0)^T \tag{3.6}$$

Equations (1) and (2) can then be written as; [Zhou 2001]

$$I_2(r) = I_1(r - U_0) \tag{3.7}$$

$$I_1(r) = I_2(r + U_0) \tag{3.8}$$

Taylor expansion of these two equations yields:

$$\begin{aligned} I_2(r) &= I_1(r)\,U_0^0 - \frac{\partial I_1}{\partial r^1} U_0^1 + \frac{\partial I_1}{\partial r^2} U_0^2 - \frac{\partial I_1}{\partial r^3} U_0^3 + K \\ I_2(r) &= I_1(r) - \nabla I_1(r)\,U_0^1 + \nabla I_1(r)\,U_0^2 - \nabla I_1(r)\,U_0^3 + K \end{aligned} \tag{3.9}$$

After neglecting higher order terms,

$$I_2(r) = I_1(r) - \nabla I_1(r) \cdot U_0 \tag{3.10}$$

$$I_1(r) = I_2(r) + \nabla I_2(r) \cdot U_0 \tag{3.11}$$

where $\nabla I_1(r)$ and $\nabla I_2(r)$ are spatial gradients of two images. Equations (3.10) and (3.11) can be rearranged as [Zhou 2001]:

$$[\nabla I_1(r) + \nabla I_2(r)] \cdot U_0 = 2[I_1(r) - I_2(r)] \tag{3.12}$$

Equation (3.11) holds for M x N pixels in a sub image Ω around r_0 and therefore leads to M x N equations. The least squares approximate solution to these equations is then determined by [Zhou 2001]:

$$U_0 = \left(A^T A\right)^{-1} A^T \cdot b \tag{3.13}$$

where,

$$A = \begin{pmatrix} \cdot \\ \cdot \\ \nabla^T I_1(r) + \nabla^T I_2(r) \\ \cdot \\ \cdot \end{pmatrix}_{M \cdot N \times 2, r \in \Omega} \tag{3.14}$$

$$b = \begin{pmatrix} \cdot \\ \cdot \\ 2[I_1(r) - I_2(r)] \\ \cdot \\ \cdot \end{pmatrix}_{M \cdot N \times 1, r \in \Omega} \tag{3.15}$$

3.5 Experimental Set-up

For this study, strain was measured using two methods. The DIC technique was used to get the full field strain and displacement contours with the help of high speed cameras. Gages were also mounted at different locations on the test boards and strain was measured at these points with the help of high speed data acquisition systems. Data was acquired on the populated as well as the non-populated sides of the test specimens. In conjunction to this, continuity data was also monitored during impact. Figure 3.15 shows the speckle pattern on four of the test boards under investigation. Patterns on the six alloy system on test board F are shown in Figure 3.16. Efforts were taken to get similar and consistent speckle patterns on all the test boards since the speckle size and distribution affect the accuracy of this technique [Zhou 2001, Gu 2006]. The package side and the board side of a speckle coated specimen board mounted with strain gages are shown in Figure 3.17.

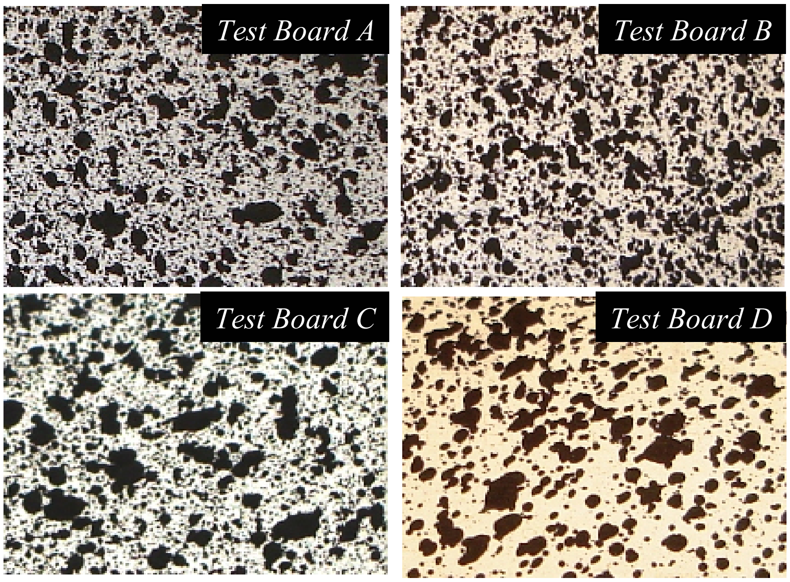


Figure 3.15: Speckle Pattern on Four of the Test Vehicles

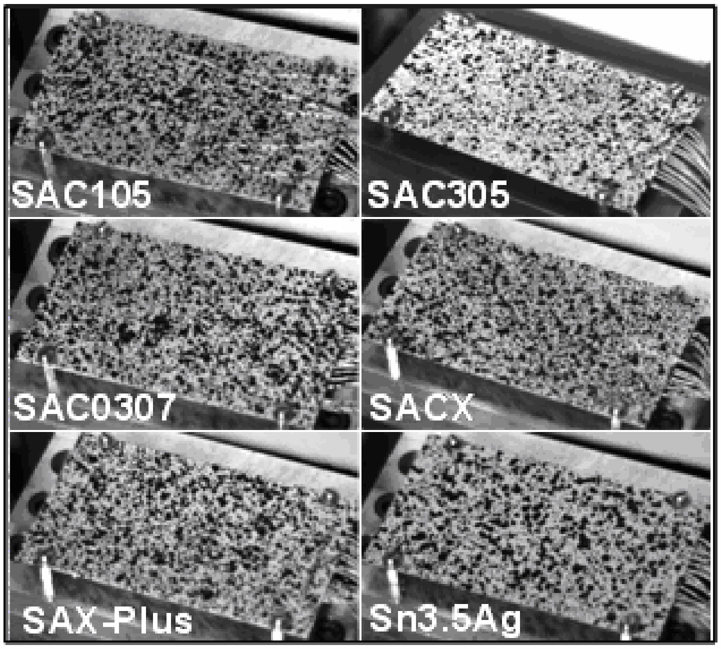


Figure 3.16: Speckle Pattern on the Populated Side of the Six Alloy System Test Vehicles

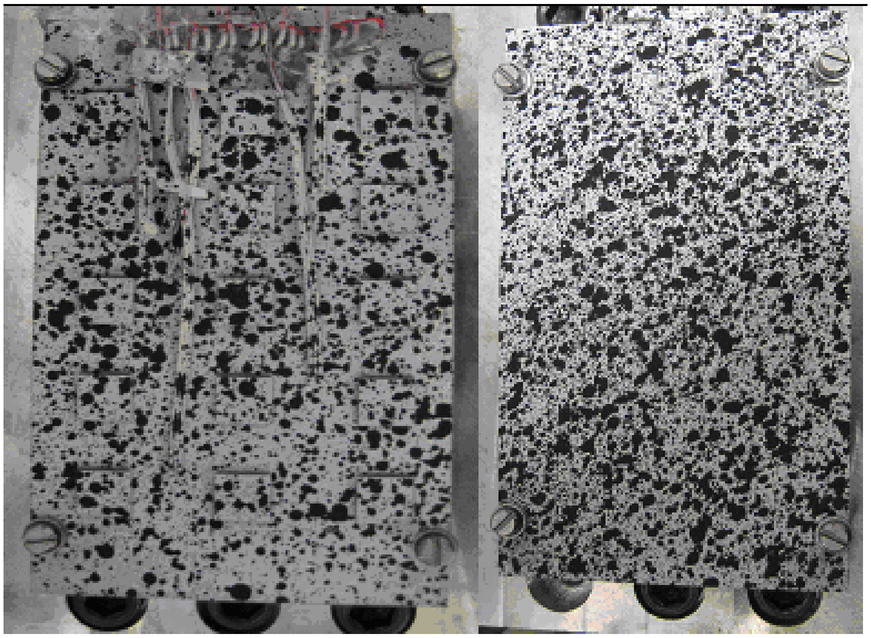


Figure 3.17: Speckle Coated Image of Test Board with Strain Gages (A) Package Side (B) Board Side

The DIC experimental set up consisted of two high speed cameras mounted on two independent tripods on a rigid floor in front of the drop tower so as to make an angle of approximately 30º with the specimen. Previous research has indicated that keeping the angle between the cameras in the range of 20º to 40º gives higher accuracy [Gu 2006, Helm 1996]. The arrangement for both the drop orientations is shown in Figure 3.18. The two CCD cameras were internally synchronized and were manually triggered with an external trigger. Before recording the drop event, the cameras were calibrated. Calibration involved capturing images of the target at different orientations as shown in Figure 3.19. The target used in this study consisted of a 9 x 9 grid of black points on a white background with a 10 mm pitch. 12 to 15 such images were taken so as to get a good calibration, ensuring high accuracy. The test specimen was constraint to the drop table with four screws at the four corners of the board. The drop table was dropped from a height of 9 inches, so as to achieve 1500Gs as per the JEDEC standard. A set of test vehicles were also drop tested from a height of 12 inches. In the vertical drop arrangement, the boards were attached with a nylon string to the drop table and were drop tested from a height of 3 feet. The transient event was captured by the two cameras which were triggered simultaneously and a video clip of the drop was recorded at 50,000 frames per second (fps). The clip was then sampled to get images of the event which were further analyzed using software from Correlated Solutions. The drop test was continued until all the packages on the test board failed.

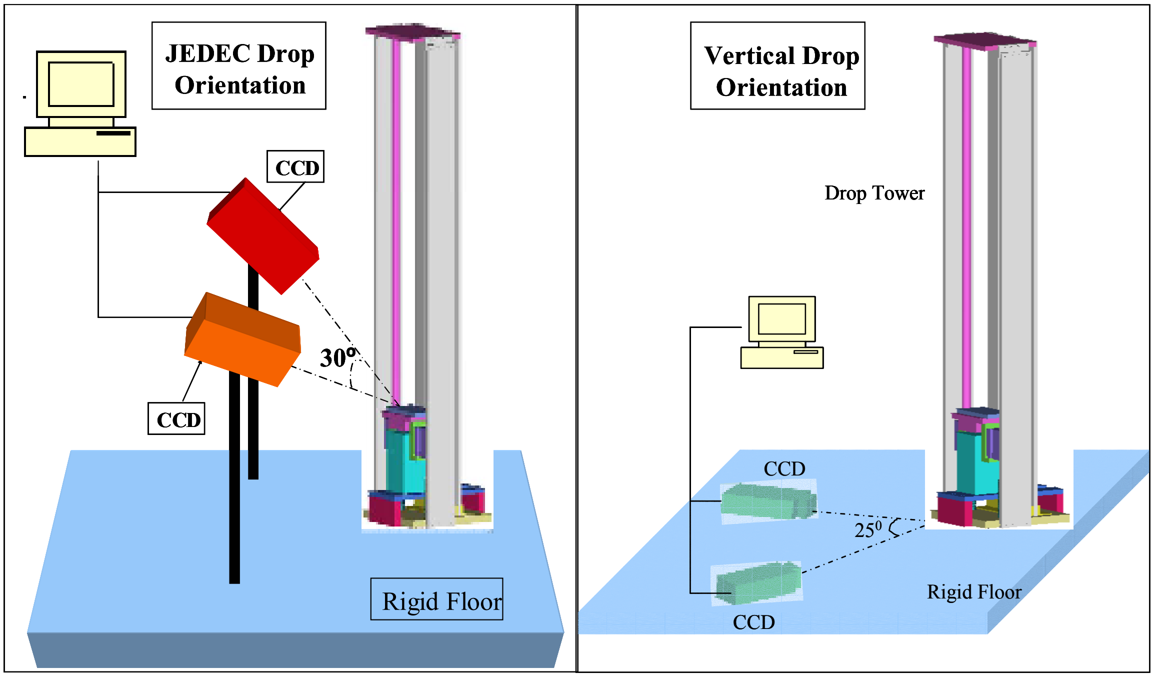


Figure 3.18: Experimental Set-up for DIC in both the Drop Orientations

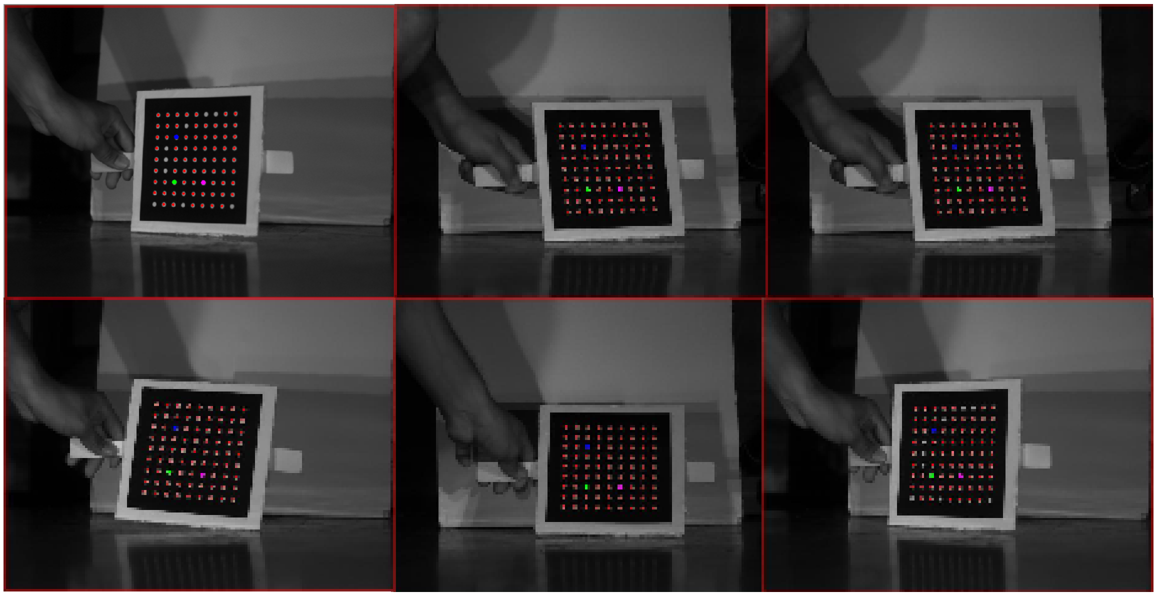


Figure 3.19: Calibration Images

3.6 Correlation of DIC Technique and Strain Gage Data

Strain from DIC technique was correlated with the strain values obtained from strain gages at various locations on the test specimens. Three such comparisons at points A1, A3, and A6 on test vehicle C subjected to drop in the vertical orientation are shown in Figure 3.20, Figure 3.21 and Figure 3.22. Comparison of strain values from DIC and strain gages at three locations on the board F with SAC305 alloy system is also shown in Figure 3.23, Figure 3.24 and Figure 3.25. DIC results obtained were accurate and consistent with the strain gage sensors. 2D strain contours of test boards A, B and C when dropped in the vertical orientation are shown in Figure 3.26. Figure 3.27 corresponds to the DIC 3-D contours of strain in the longitudinal direction at different time instants for test board C drop tested in the vertical drop direction. Although this plot represents the drop test in the vertical drop orientation, the board appears to be horizontal with the ground on the right hand side of the figure. Figure 3.28 shows the 3-D contours of strain for test board A in the 0º JEDEC configuration. Figure 3.29 shows a comparison of a DIC transient-deformation contour with the actual deformation contour of the test specimen. Figure 3.30 shows the 3D strain contours at successive drops during the transient drop event.

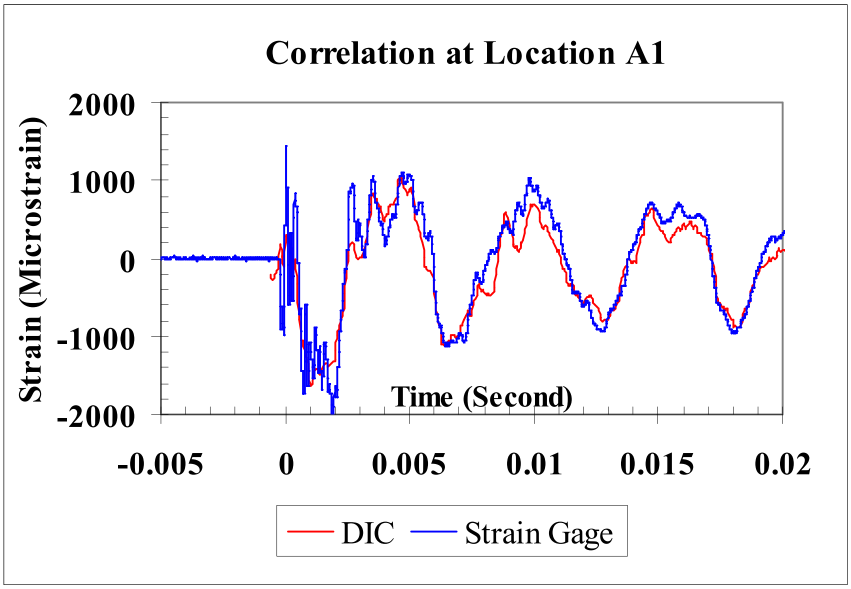


Figure 3.20: Strain Correlation of Test Board-C subjected to Vertical Drop at Location A1

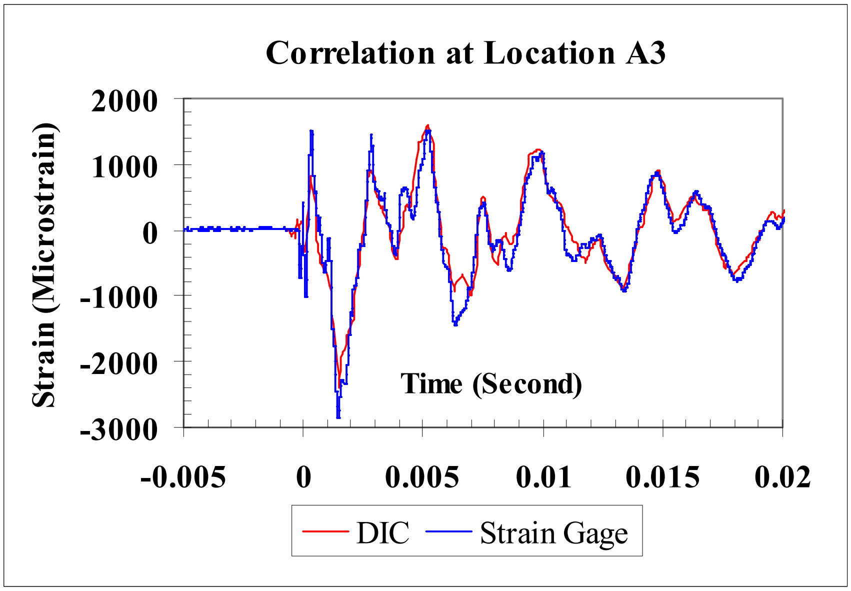


Figure 3.21: Strain Correlation Test Board-C subjected to Vertical Drop at Location A3

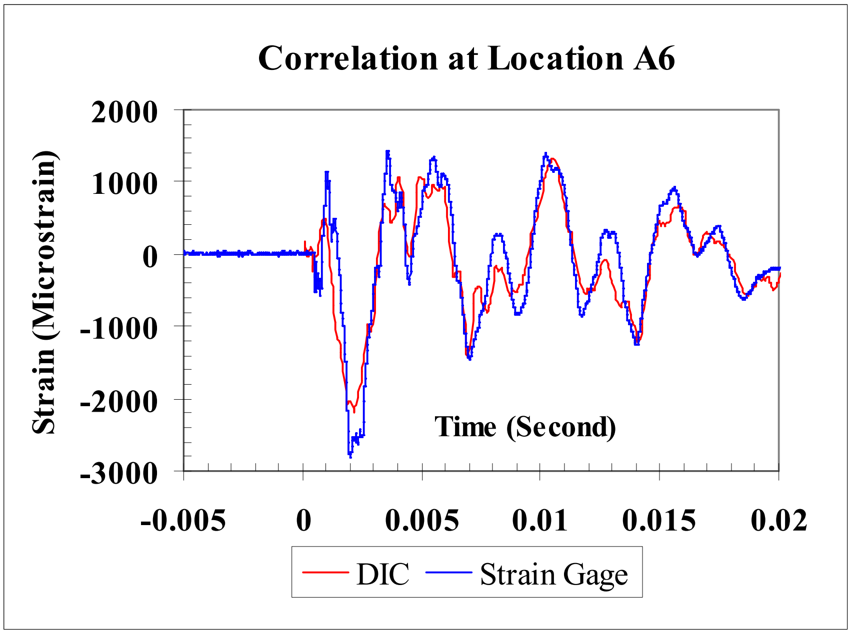


Figure 3.22: Strain Correlation Test Board-C subjected to Vertical Drop at Location A6

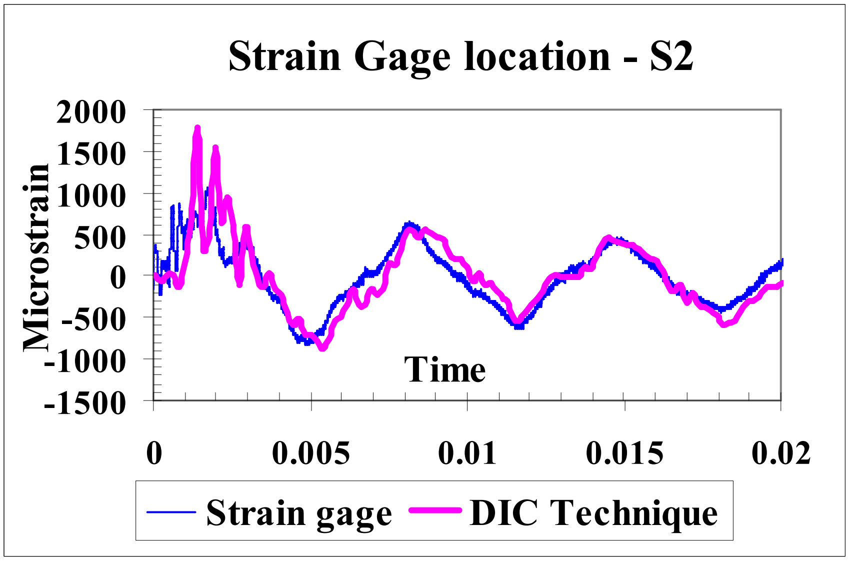


Figure 3.23: Correlation of Strain from DIC and Strain Gages for SAC305 Alloy System at Gage Location S2

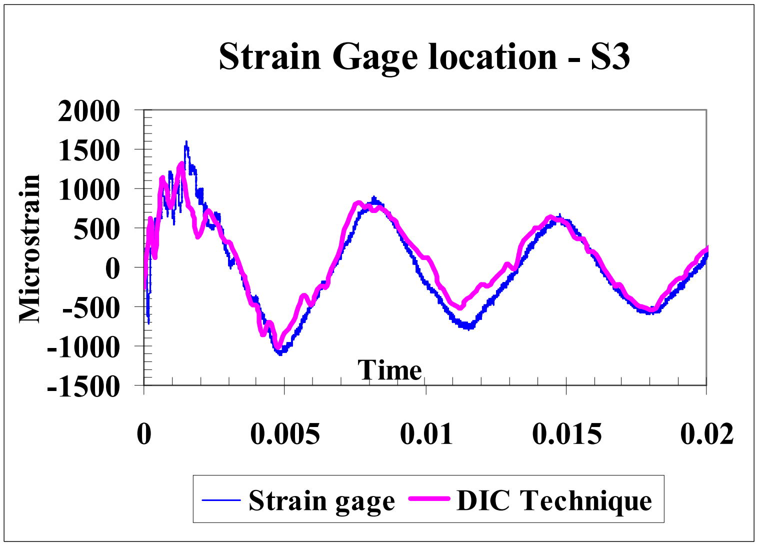


Figure 3.24: Correlation of Strain from DIC and Strain Gages for SAC305 Alloy System at Gage Location S3

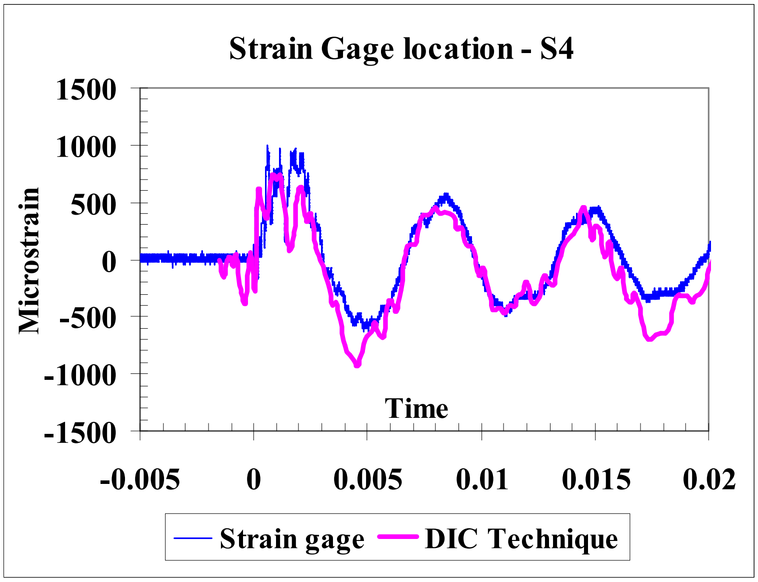


Figure 3.25: Correlation of Strain from DIC and Strain Gages for SAC305 Alloy System at Gage Location S4

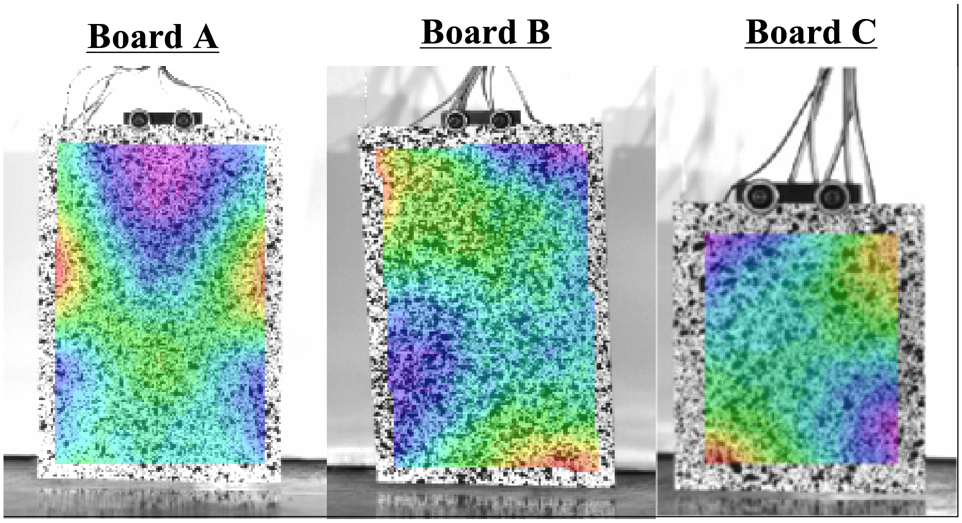


Figure 3.26: 2D Strain Contours of Boards A, B, and C Dropped in Vertical Orientation

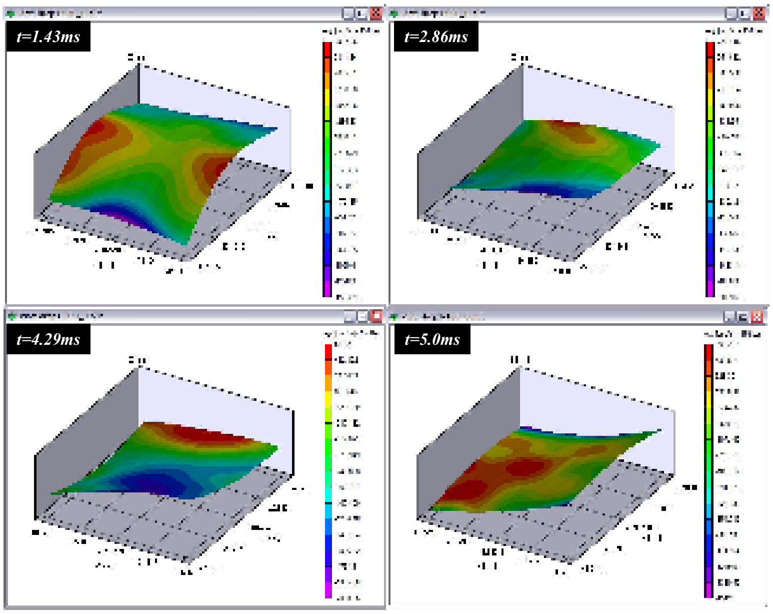


Figure 3.27: 3D Longitudinal Strain Contours from DIC for Test-Board C subjected to 90º Vertical Drop

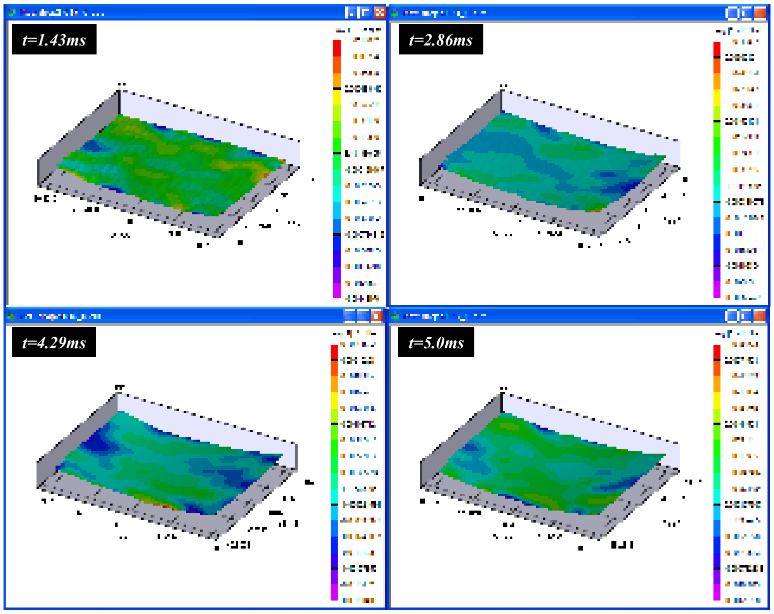


Figure 3.28: 3D longitudinal strain contours from DIC for Test-Board A subjected to 0º JEDEC Drop

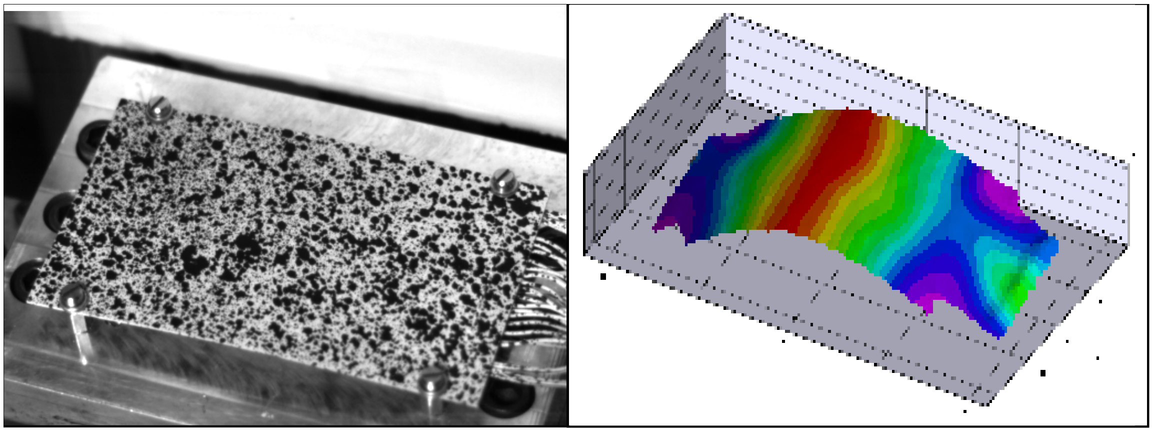


Figure 3.29: Comparison of DIC Strain Contour with the Actual Contour

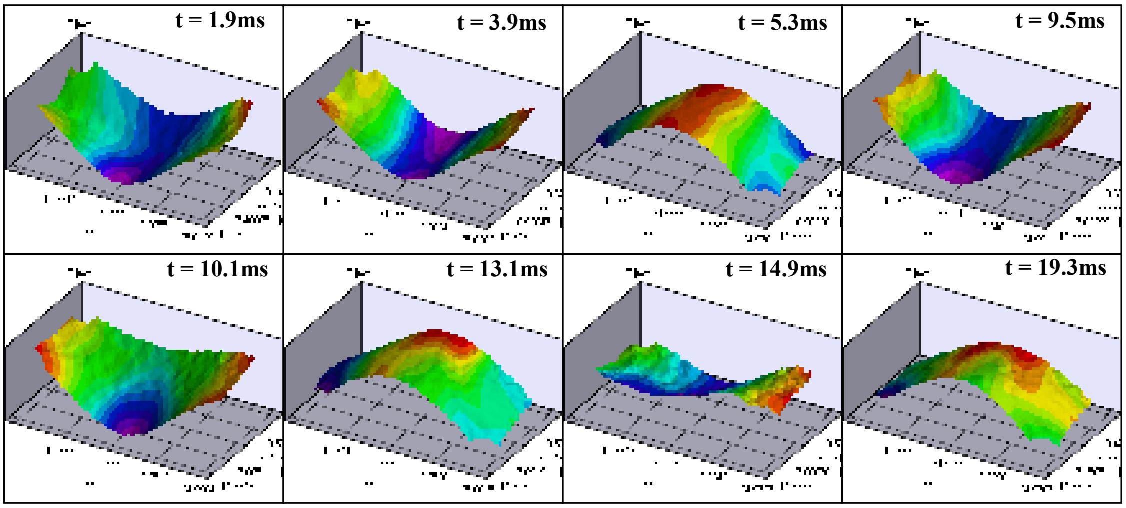


Figure 3.30: 3D Strain Contours at Successive Drops during the Transient Drop Event

3.7 Full-Field Transient Strains for Various Lead-free Alloys

The full-field transient strains for six lead-free alloys, namely, SAC105, SAC305, SAC0307, SACX, SACX-Plus and Sn3.5Ag were measured. The measurements of the strain histories were compared as a function of package locations on the package-side and the board-side. Figure 3.31 and Figure 3.32 show the peak strain values as a function of package location on SACX and SAC0307 test boards. The trend was consistent for various alloy systems examined in the study. Largest PCB peak strain values were observed in the center section of the JEDEC test board, shown as maxima at package locations 2-3, 8-9, and 13-14. Strain values at two different locations, package 2 and package 14, on the PCB just below the package are shown in Figure 3.33 and Figure 3.34. The peak strain values between alloys differed greatly and are plotted in Figure 3.35. It is hypothesized that the difference in the peak strain is due to difference in the elastic modulus of the solder alloys. Figure 3.36 shows failure as a function of package location. The number of drops-to-failure was strongly correlated with the magnitude of peak strain. Packages with the largest peak strain exhibited the smallest cycle count-to-failure. The negative trend between drops-to-failure and peak value of transient strain during a drop event for SAC305 and Sn3.5Ag solders is shown in Figure 3.37 and Figure 3.38. The negative trend was consistent for all the alloys. Data-analysis proved that the PCB transient strain histories were a valid potential indicator of failure progression and failure thresholds for the different lead-free alloy systems.

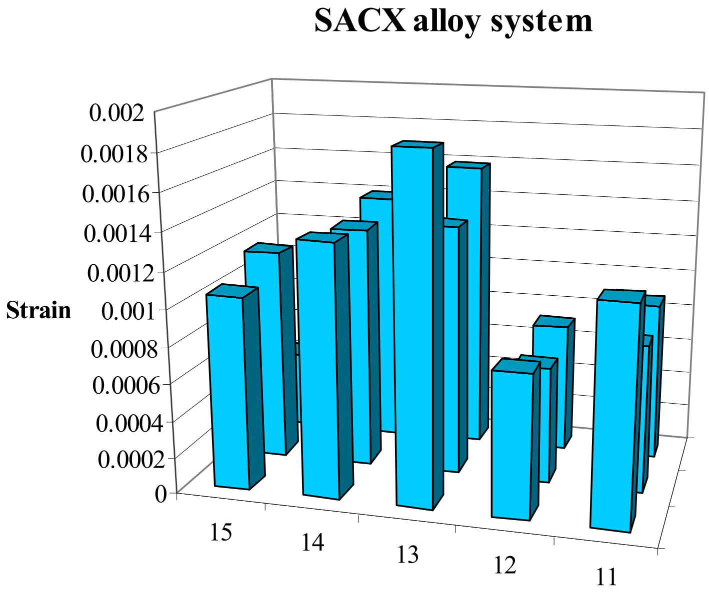


Figure 3.31: Peak PCB Strain Values as a Function of
Package Location on the SACX Solder Alloy System on Board F

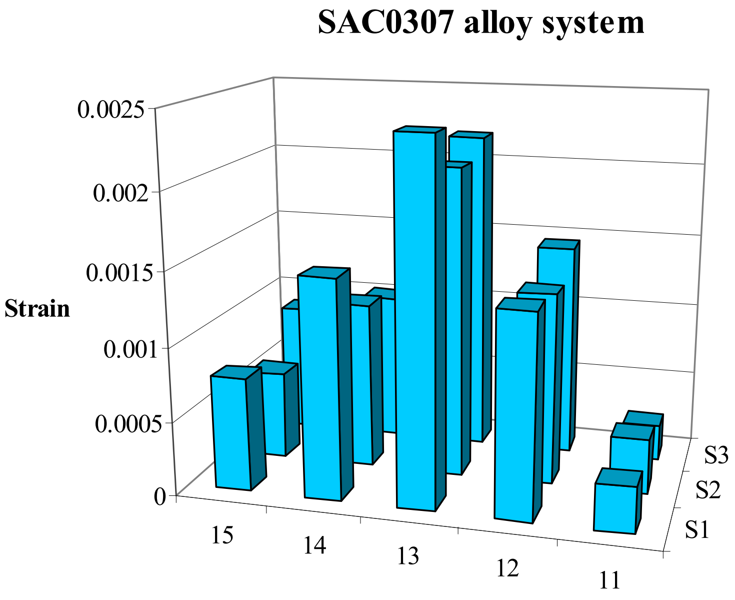


Figure 3.32: Peak PCB Strain Values as a Function of
Package Location on the SAC0307 Solder Alloy System on Board F

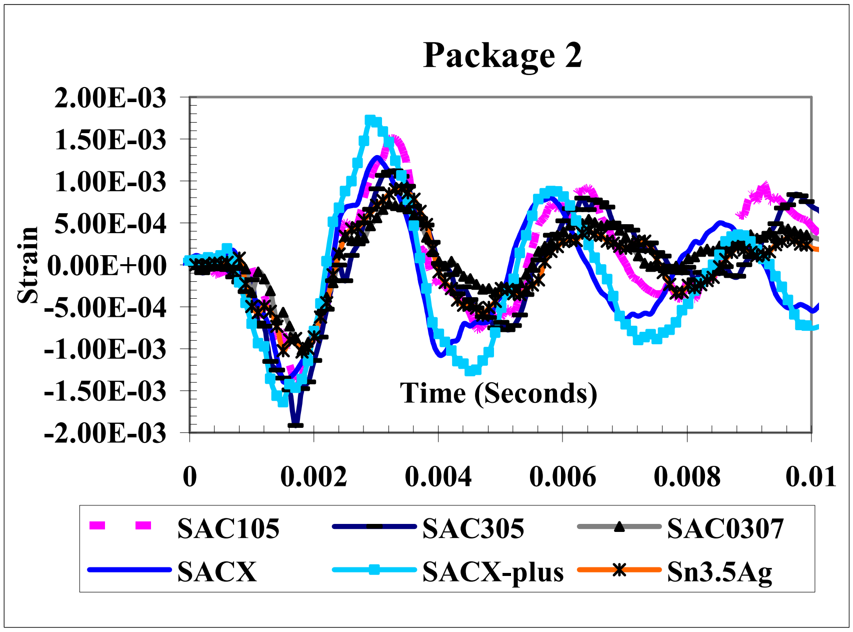


Figure 3.33: Comparison of Strain for the Six Alloy Systems at Package 2 Location on Board F

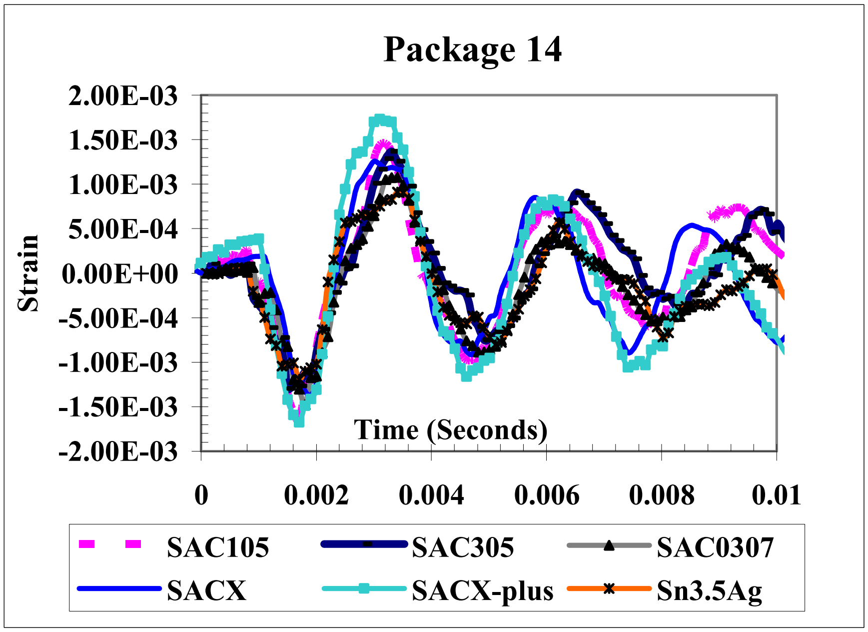


Figure 3.34: Comparison of Strain for the Six Alloy Systems at Package 14 Location on Board F

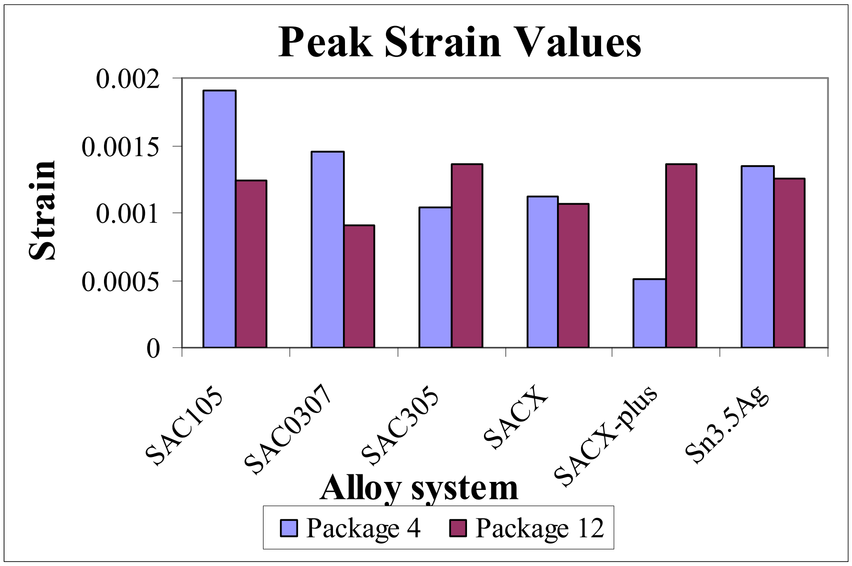


Figure 3.35: Peak Strain Values at Packages 4 and 12 Location for the Various Alloy Systems on Board F

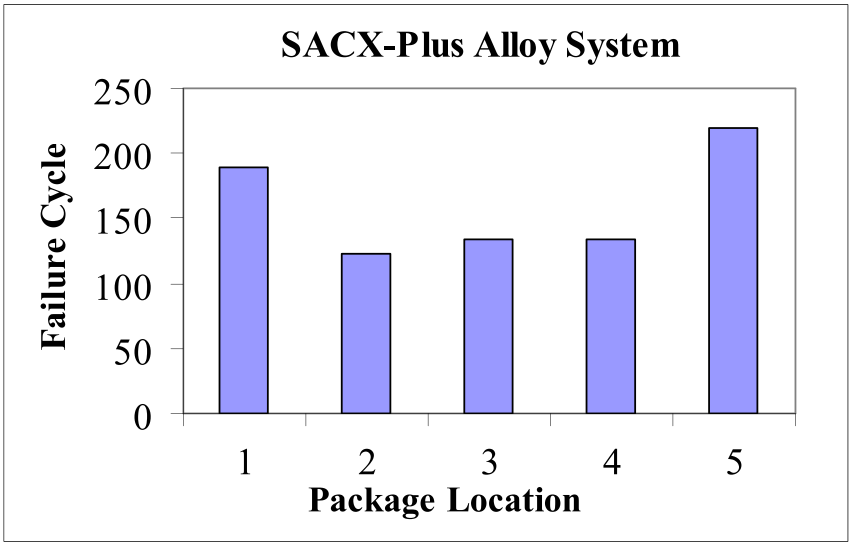


Figure 3.36: Failure Plot for the SACX-Plus Alloy System on Board F

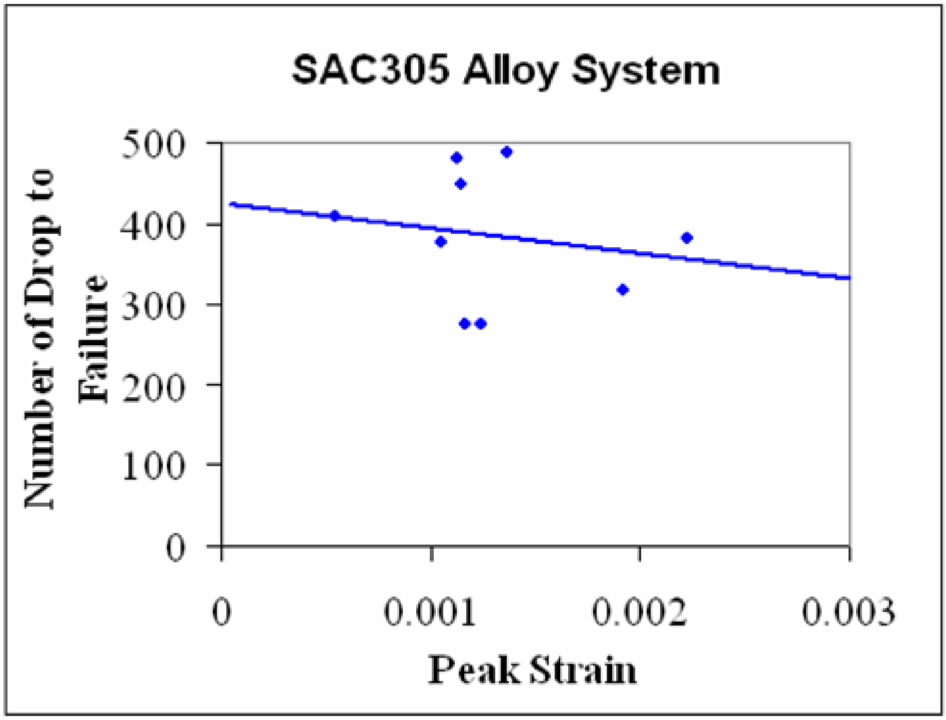


Figure 3.37: Correlation of Peak Strain with Drops-to-Failure for SAC305 alloy on Board F

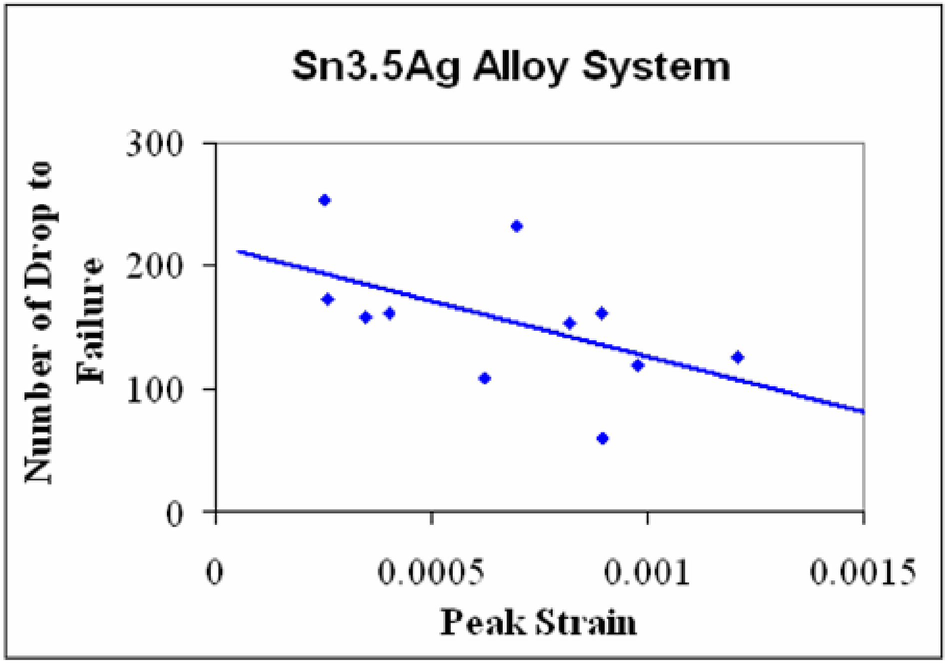


Figure 3.38: Correlation of Peak Strain with Drops-to-Failure for Sn3.5Ag alloy on Board F

The 2D strain state was measured on the top surface of the package during the transient deformation experienced by the board assembly during the shock-impact. The measurements of full-field package strain at various package locations were compared for the various lead-free alloys. Comparison of strain contours for the six alloys at package 12 location has been shown at the same time instant after impact in Figure 3.39. Strain distributions varied with solder alloys at the same location and same instant after impact.

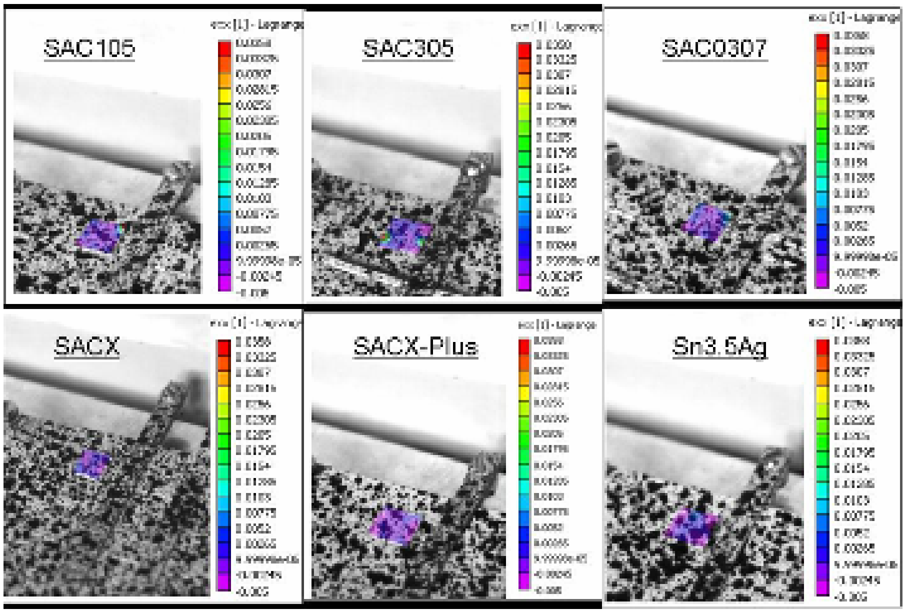


Figure 3.39: Comparison of 2D Contour Plot at Package Location 12 at Same Time Instant for Different Alloy Systems on Board F

3.8 Explicit Finite Element Models

Explicit finite element methods are well suited to simulate high-speed dynamic events which require small increments in order to obtain high resolution solutions. Transient dynamic deformation of the test boards was treated as a wave propagation problem and was modeled using explicit finite element models. Prediction of the response of the test specimen subjected to 0° JEDEC and 90° vertical drop orientations were simulated and results from the simulation were correlated with the DIC measurements.

Previously, the JEDEC JESD22-B111 condition was modeled using the input-G method [Tee 2004]. In this thesis, the use of explicit finite elements has been investigated. The use of this method enables the calculation of response history using step-by-step integration in time without changing the form of dynamic equations as done in modal methods. The modeling effort was focused on the predictions of transient dynamic drop response variables using explicit finite-element theory with reduced integration elements.

An explicit algorithm uses a difference expression of the general form,

$$\{D\}_{n+1} = f\left[\{D\}_n, \{\dot{D}\}_n, \{\ddot{D}\}_n, \{D\}_{n-1}, ...\right] \tag{3.16}$$

where {D} is the degree of freedom vector, the '.' on top of the variable represents time differentiation, and subscript 'n' represents the time-step. The equation contains only historical information on the right hand side. The difference expression is combined with the equation of motion at time step 'n' for the simulation and is given as,

$$\begin{aligned}&\left(\frac{1}{\Delta t^2}[M]+\frac{1}{2\Delta t}[C]\right)\{D\}_{n+1}\\&=\left\{R^{ext}\right\}_n-\left\{R^{\text{int}}\right\}_n+\frac{2}{\Delta t^2}[M]\{D\}_n-\left(\frac{1}{\Delta t^2}[M]-\frac{1}{2\Delta t}[C]\right)\{D\}_{n-1}\end{aligned} \tag{3.17}$$

If [C] in equation (3.16) was either zero or diagonal, each time step was executed very quickly because the solution of simultaneous equations is not required. But

[C]= α [M] + β [K],

such that diagonal [C] corresponds to mass-proportional damping α [M] with diagonal [M], which damps lower modes most heavily. Mass damping was used for the PCB material in the simulation. Hence, there was a small time-lag which was unavoidable since the implementation was to be fully explicit, i.e. the solution of any of the equations was not required. In order to have equation (3.16) to be conditionally stable, we need to have,

$$\Delta t < \Delta t_{cr} = \frac{2}{\omega_{\max}} \tag{3.18}$$

where frequency ω_{max} and its period T_{min} correspond to the highest natural frequency of

$$([K] - \omega^2 [M]) \{D\} = 0 \tag{3.19}$$

It was essential to determine the maximum natural frequency of the system i.e. ω_{max}, as explicit integration fails whenever Δt is very large or Δt is unnecessarily small leading to expensive calculations. The estimation of ω_{max} is provided by the Gerschgorin bound, which may be stated in the following form of lumped (or diagonal) mass matrix,

$$\omega_{\max}^2 \le \max_i \left(\frac{1}{M_{ii}} \sum_{j=1}^{n} \left| K_{ij} \right| \right) \tag{3.20}$$

where, i = 1, 2, 3,….,n, and n is the matrix order of number of degrees of freedom, K and M are the stiffness and mass matrices respectively. Courant number, C_n is used to measure the time step which is defined as,

$$C_n = \frac{\Delta t_{actual}}{\Delta t_{cr}} \tag{3.21}$$

where Δt_{cr} is the maximum time step consistent with the numerical stability. In order to reduce the computation time of the transient dynamic event, reduced integration elements were used in the analysis. These element types use fewer integration points to form the element stiffness matrices. Lower order element performed better when the strain was large or a very high strain gradient was expected during drop impact events. Higher order elements have higher frequencies than the lower order elements and tend to produce noise when stress waves move across a finite element mesh. Lower order elements provided better results than the higher order elements while modeling a shock wave front.

Figure 3.40 correspond to the explicit finite element model for Test Boards B in the JEDEC drop configuration. Reduced integration elements were used to formulate the transient event. Fewer integration points were required as compared to the implicit formulation thus, reducing the computation time to run the models. Shell-elements (S4R), which account for large strains [Abaqus 2007] were used to model the PCB. Solder interconnects were modeled using three-dimensional linear Timoshenko-beam (B31) elements. 3D beams have six degrees of freedom at each node including three translational and three rotational degrees of freedom. The rotational degrees of freedom were constrained to simulate the interconnect behavior. B31 elements also allowed shear deformation. It was assumed that the strain was constant throughout the beam. Various component layers of the packages such as substrate die-adhesive, silicon die, encapsulant and copper pads were modeled with C3D8R solid elements. The concrete floor was modeled as a rigid floor using a rigid R3D4 element.

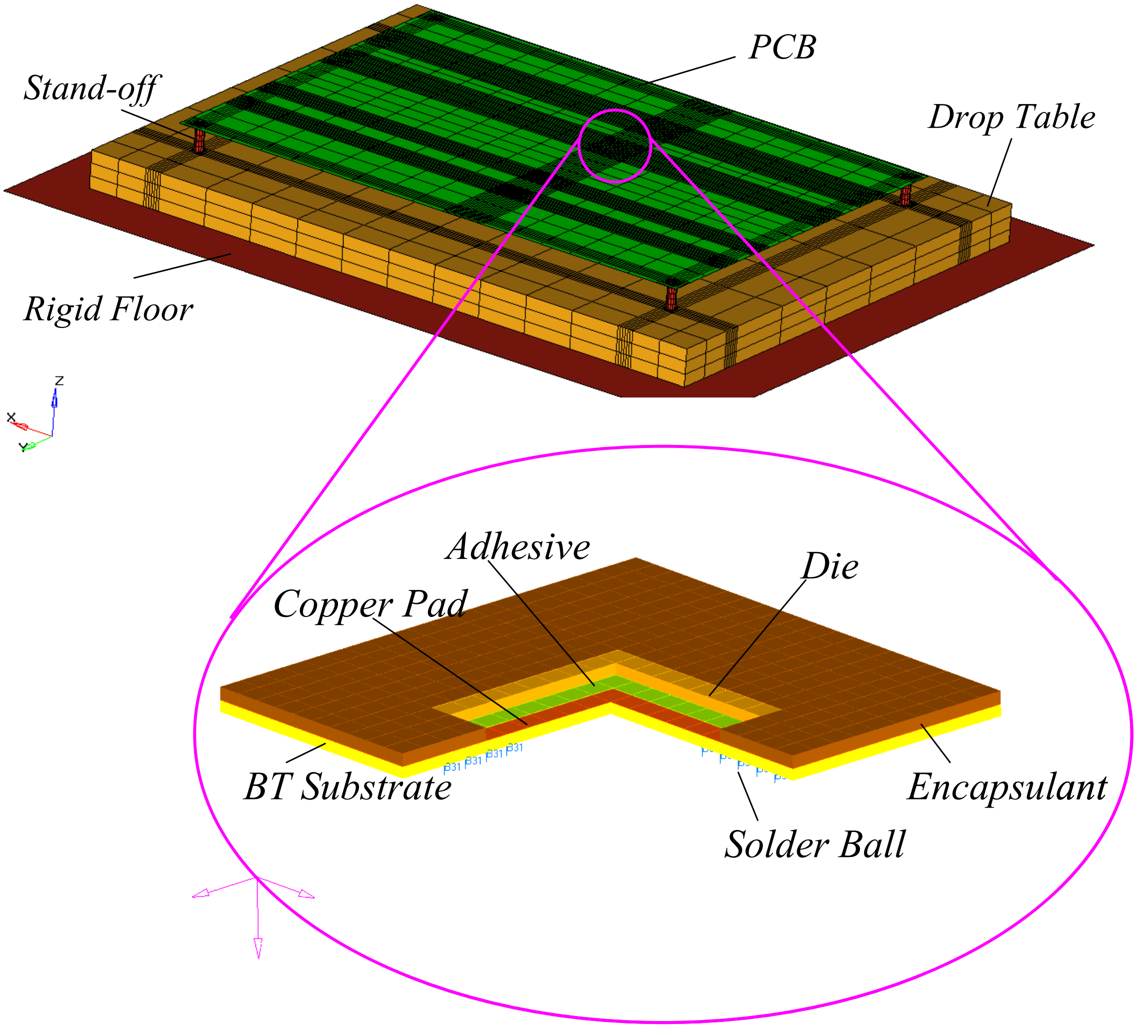


Figure 3.40: Explicit-Finite Element Model for Test Board B in JEDEC Configuration

The cost of a numerical simulation depends on the size of the model and the number, 'N' of time increments that are required to simulate the entire shock event. Possible approaches to reduce the overall CPU time either involves an increase in the size of the time increments, Δt, or a reduction in the total time t of the operation. The first approach known as mass scaling can be easily achieved by increasing the density of the material and thus artificially reducing the speed of the longitudinal wave. The second approach known as load factoring is generally accomplished by changing the rate of loading through an artificial increase in the velocity as compared to the real process speed. This second approach should not be considered when the material is strain-rate sensitive or thermo-mechanical phenomenona are involved. It is worth mentioning that the above mentioned numerical strategies to reduce the CPU time must be sensibly utilized because they may cause the dynamic formulation to provide inaccurate solutions for the deformation as well as for the stress-strain distribution. It should be ensured that parametrization by mass scaling or load factoring approaches prevents the kinetic energy to ascend above 5% of the total strain energy.

The mass of selected element sets or individual elements in Abaqus™ can be scaled so as to control the stable time increment. As the explicit central difference method was used to integrate the equations in time, the discrete mass matrix used in the equilibrium equations played a crucial role in both computational efficiency and accuracy of the transient dynamic response problems. Whenever the non-physical mass was added to increase the time step in the dynamic analysis, F = m * a relation got affected. For cases with an insignificant effect, adding the non-physical mass to just a few small elements in non-critical areas was justifiable. A user defined scale factor was used to scale the mass.

It was observed that mass scaling saved computational time by 2 to 4 times with 1 to 5% change in accuracy. Material deformation was assumed to be linear elastic for FR-4 PCB material, SnAgCu solders, copper pad on package side, BT substrate, silicon die, and encapsulant. The properties of all the materials used in the finite element simulation are given in Table 3.6.

Table 3.6: Material Property for Finite Element Simulation

	Elastic Modulus (GPa)	**Poisson's Ratio**	**Density (Kg/m^3)**
62Sn36Pb2Ag	32	0.35	8400
Mold	23.5	0.25	1650
Die	162	0.28	2329
Die Attach	2.76	0.35	7800
Epoxy Film	0.649	0.35	2100
BT substrate	17.4	0.28	1800
Bare FR-4	16.8	0.39	1800

Smeared property modeling was used to simulate the JEDEC drop phenomenon of the test board F as shown in Figure 3.41. Smeared property was calculated based on volumetric averaging [Lall 2004, 2005]. The material properties used in the finite element simulation are specified in

Table 3.7. Weight of the components in the simulation is comparable to the actual weights as shown in Table 3.8.

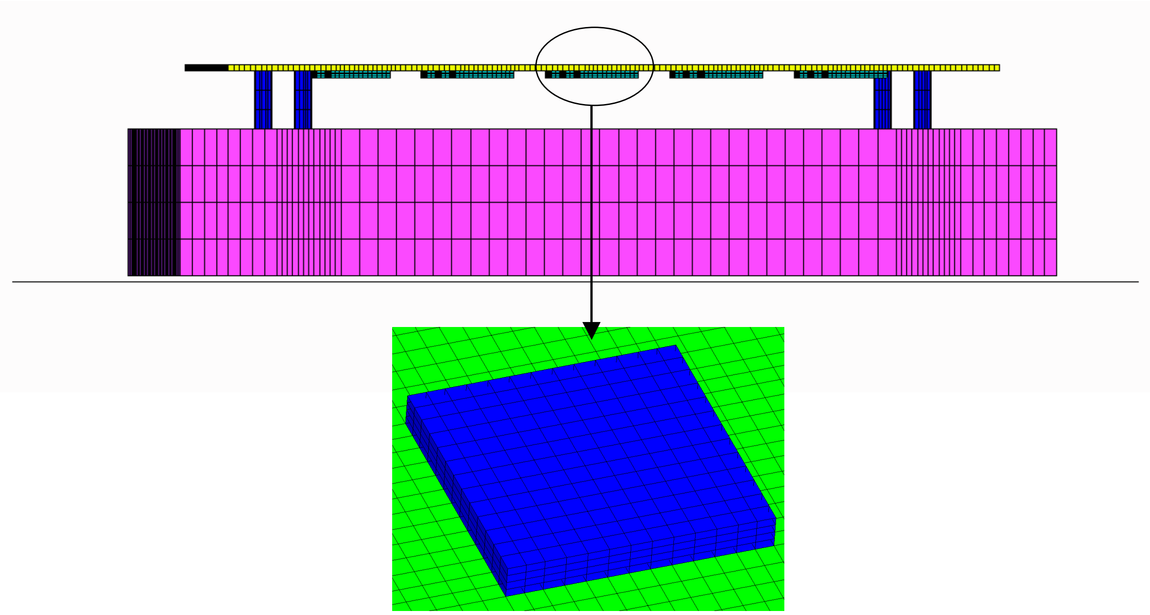


Figure 3.41: Smeared Property Model

Table 3.7: Material Property used in the Finite Element Simulation

	Elastic Modulus (GPA)	Poisson's Ratio	Density (Kg/m3)
PCB	16	0.33	2243
Mold	15.5	0.25	1970
Substrate	24.13	0.33	1400

Table 3.8: Actual and Simulated Component Masses

Components	Actual Mass	Simulated mass
PCB	22.8 gm	22.74 gm
Package	0.23 gm	0.24 gm
Base Plate	11.52 Kg	12 Kg

3.9 Simulation Model Validation

Transient dynamic strain predicted by the explicit finite element models for both the JEDEC and the vertical drop were correlated with the high-speed strain-gage and DIC measurements. Figure 3.42 and Figure 3.43 show strain correlation plots for test board C subjected to drop in the vertical orientation at two locations on the PCB side of the specimen. During impact, the peak deformation occurs within 20 ms, and hence the correlation is shown for this time duration. The values of strain on the PCB side and the package side showed good correlation with the experimental data. The correlation for the strain value obtained from DIC and simulation at location A1 have been calculated and shown to be 0.859. The transient dynamic strain prediction for the JEDEC 0° drop from the DIC technique and from simulation were calculated on the package side as well as the board side. Figure 3.44 shows strain correlation for the SAC305; test board F for the first 20 milliseconds. Transient mode shapes at different time intervals are shown in Figure 3.45 for test board C subjected to drop in the vertical orientation. However, the plot is shown with the board in the horizontal direction moving from left-to-right during the fall, with the ground on the right side of the plot for both the DIC and explicit finite element technique. The board was dropped with a weight attached to the top end of the printed circuit board assembly. Transient mode shapes were plotted at 1.4ms and 2.8ms. Comparisons of the 3D strain contours for test board D subjected to drop in the JEDEC orientation at 1.4ms and 4.29ms are shown in Figure 3.46. The predicted mode shapes showed good correlation with experimental data for both cases.

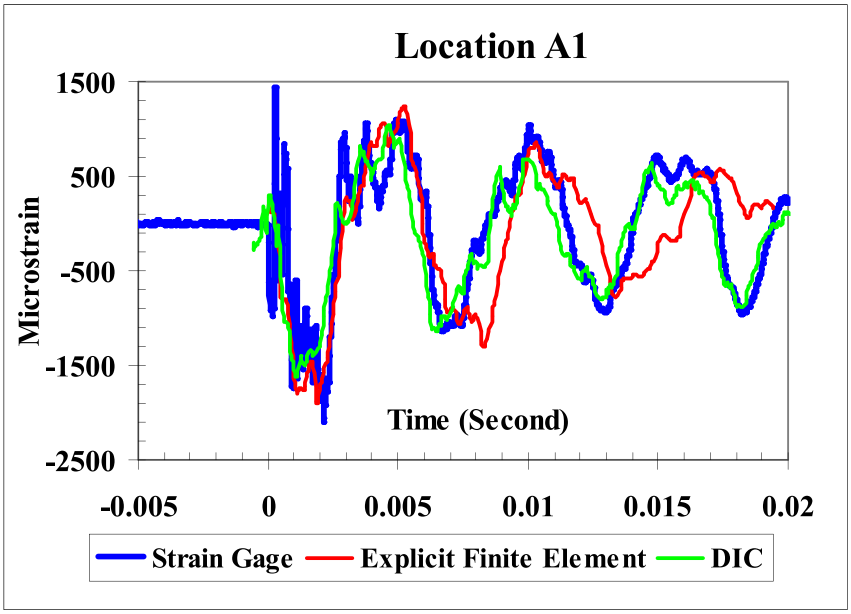


Figure 3.42: PCB Strain correlation of results from experiment, finite element and DIC Technique at location A1 on Test Board C, subjected to Vertical Drop Correlation = 0.859

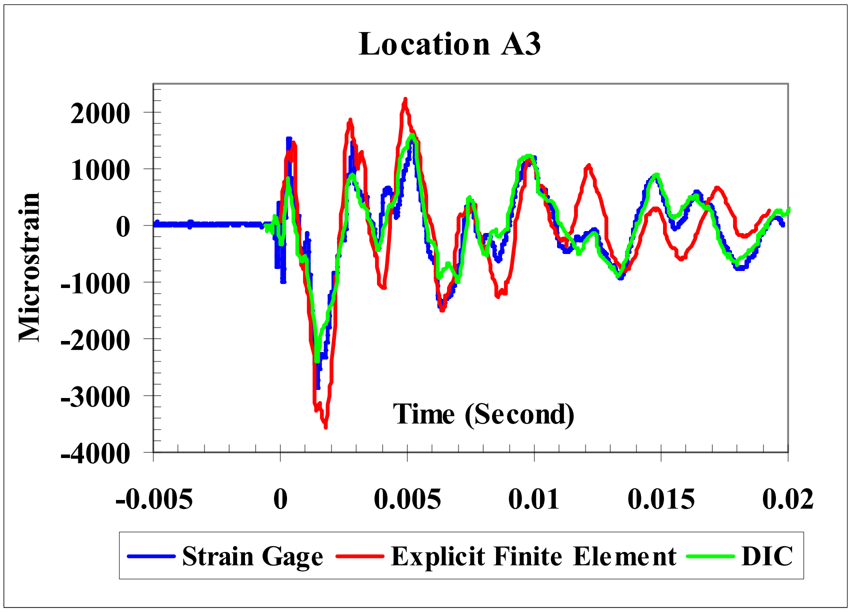


Figure 3.43: PCB Strain correlation of results from experiment, finite element and DIC Technique at location A3 on Test Board C subjected to Vertical Drop

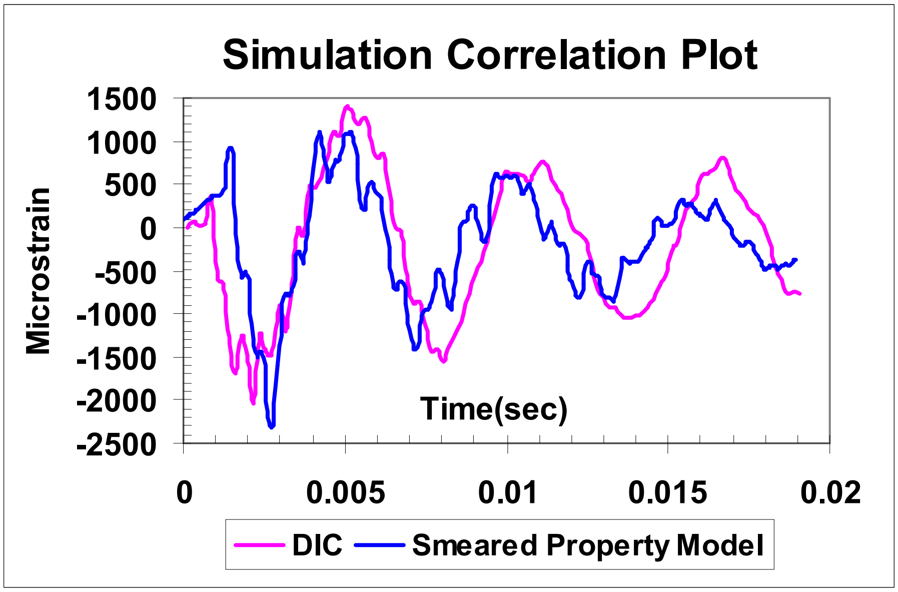
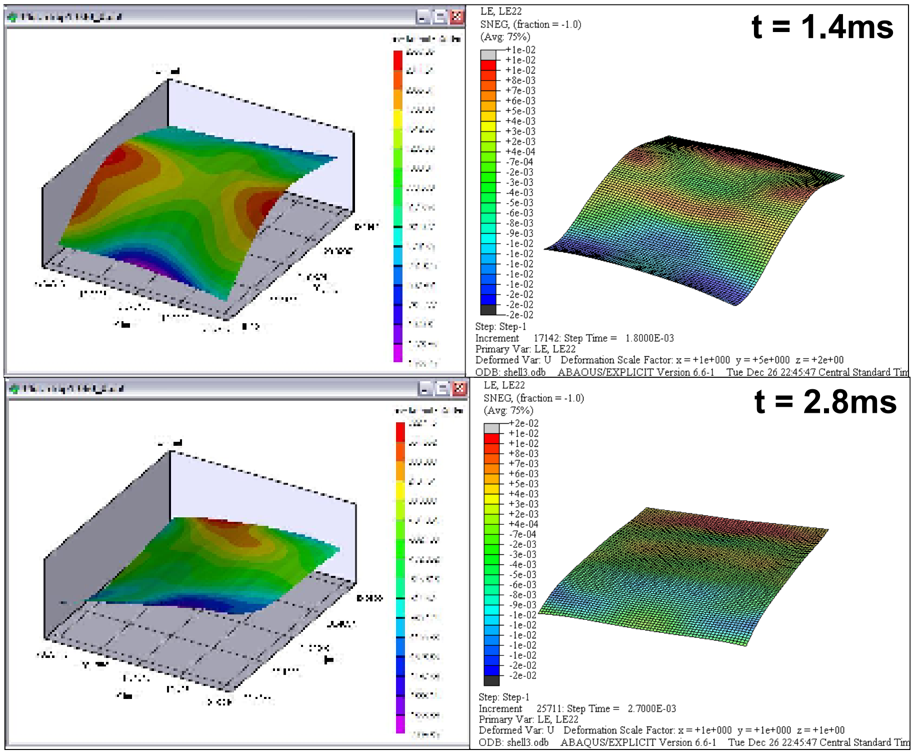


Figure 3.44: Package Strain Correlation between DIC and Finite Element Models at the Package 13 Location on SAC305; Test Board F during 0° JEDEC Drop



```
Step: Step-1
Increment     17142: Step Time =   1.8000E-03
Primary Var: LE, LE22
Deformed Var: U   Deformation Scale Factor: x = +1e+000  y = +5e+000  z = +2e+00
ODB: shell3.odb    ABAQUS/EXPLICIT Version 6.6-1    Tue Dec 26 22:45:47 Central Standard Tim
```

```
Step: Step-1
Increment     25711: Step Time =   2.7000E-03
Primary Var: LE, LE22
Deformed Var: U   Deformation Scale Factor: x = +1e+000  y = +1e+000  z = +1e+00
ODB: shell3.odb    ABAQUS/EXPLICIT Version 6.6-1    Tue Dec 26 22:45:47 Central Standard Tim
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Figure 3.45: Correlation of DIC and FEM Full Field 3D Strain Contours of Test Board C subjected to vertical drop

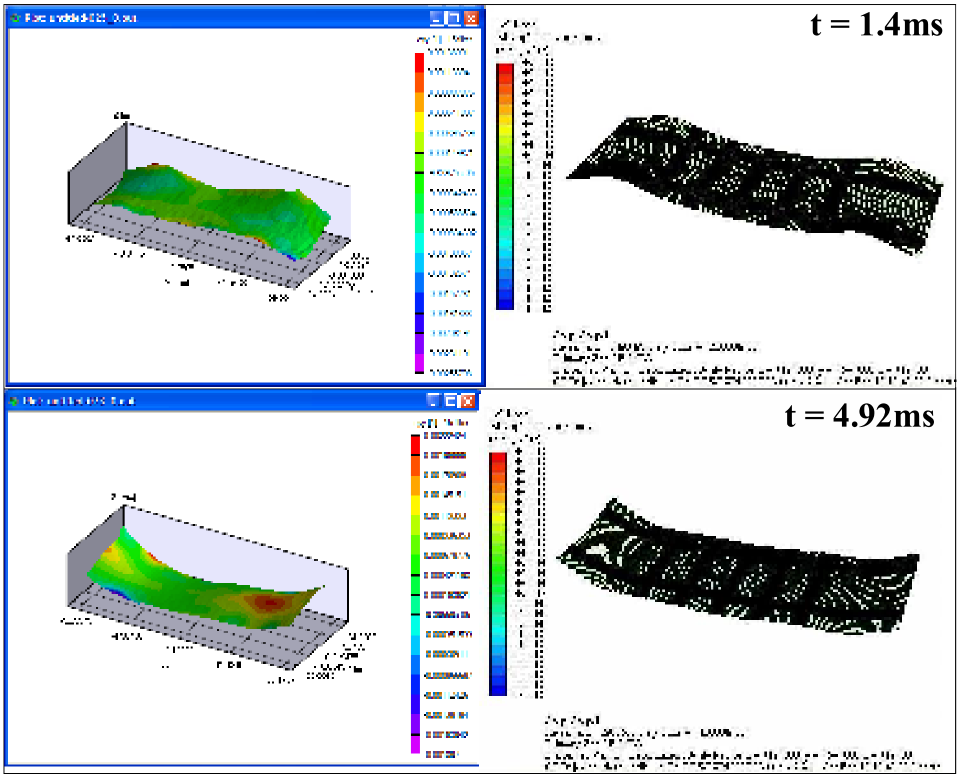


Figure 3.46: Correlation of DIC and FEM Full Field 3D Strain Contour of Test Board D subjected to JEDEC Drop

CHAPTER 4

OPTICAL FEATURE EXTRACTION TECHNIQUES FOR SURVIVABILITY OF LEADFREE PACKAGING ARCHITECTURES UNDER SHOCK AND VIBRATION

4.1 Introduction

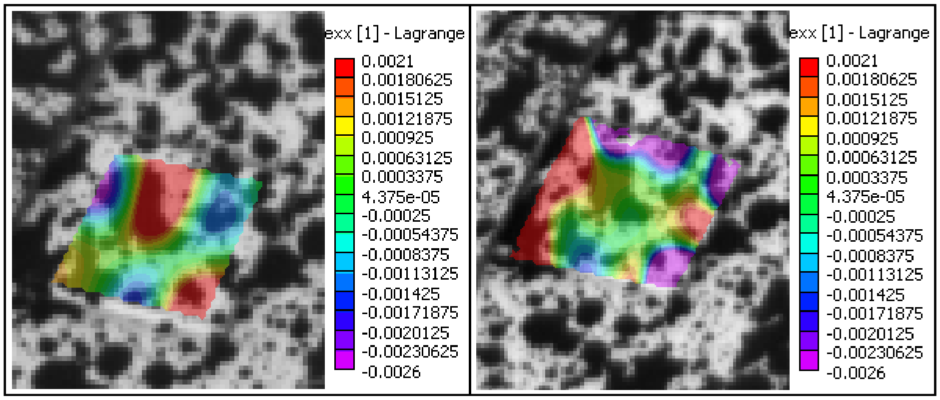
In this chapter, The Statistical Pattern Recognition (SPR) method was implemented to quantify the relative performance based on strain histories obtained from the Digital Image Correlation (DIC) technique. SPR was also used to study the effect of damage progression for various types of packaging architectures. Confidence values of the transient-strain response computed using Wavelet Packet Energy Decomposition, Mahalanobis distance and Fast Fourier Transform (FFT) approach were investigated. A methodology was developed to identify the damage progression with respect to the number of drops, by studying the transient strain history of electronic assemblies from DIC in conjunction with SPR. Manifestation of damage was examined through analysis of observed failure modes and degradation in confidence value. The development of SPR based damage proxies was investigated to establish a method for identification of impending failures. The damage proxies developed could be used on strain response from simulation or from experimental data in controlled drop or shock tests. Damage proxies also provided objective and quantitative failure definitions that accommodate variations in orientation and component location, in addition to load history. These proxies were scalable and could account for recognition of imminent failure in product level applications.

4.2 Transient Mode Shapes from DIC and Strain Gage

Full field package strain measurements also indicated that the 2D strain distributions varied between pristine packages and the packages with incipient damage. Figure 4.1 and Figure 4.2 show a comparison of package strain distribution at package locations 8 and 13 respectively for the SACX-Plus alloy system, before and after failure of the solder interconnects. The package strain state changed significantly after failure of the solder interconnects.

4.3 Leading Indicators for Damage Initiation and Progression

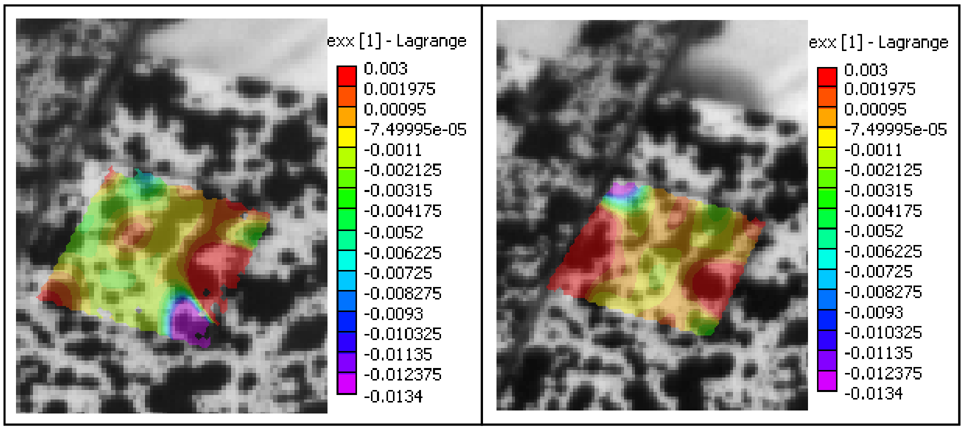
The strain values at the package locations varied before and after failure of the component. Knowledge of how these strain values differ may be used as an indicator to predict failure in packages under dynamic loading conditions. The variation in strain values was different for different alloys. Figure 4.3 and Figure 4.4 show the change in strain values before and after package failure as compared to strain at zero cycles. This assessment was made at package location 12 for two alloy systems. To make the comparison easier, the peak values for the three conditions for two alloy systems are also shown in Figure 4.5 and Figure 4.6. The trend remained the same for the other alloy systems. It can be concluded from these graphs that as the cycle number increases during the test, the strain in the solder interconnects increase up to failure, after which the values plunge.



SACX – plus; Drop 73; t = 1.98ms,

SACX – plus; Drop 141; t = 1.98ms,

Figure 4.1: 2D Strain Contours at Package Location 8 Before and After Failure for the SACX-Plus Alloy System on Test Board F



SACX – plus; Drop 78; t = 1.98ms,

SACX – plus; Drop 430; t = 1.98ms,

Figure 4.2: 2D Strain Contours at Package Location 13 Before and After Failure for the SACX-Plus Alloy System on Test Board F

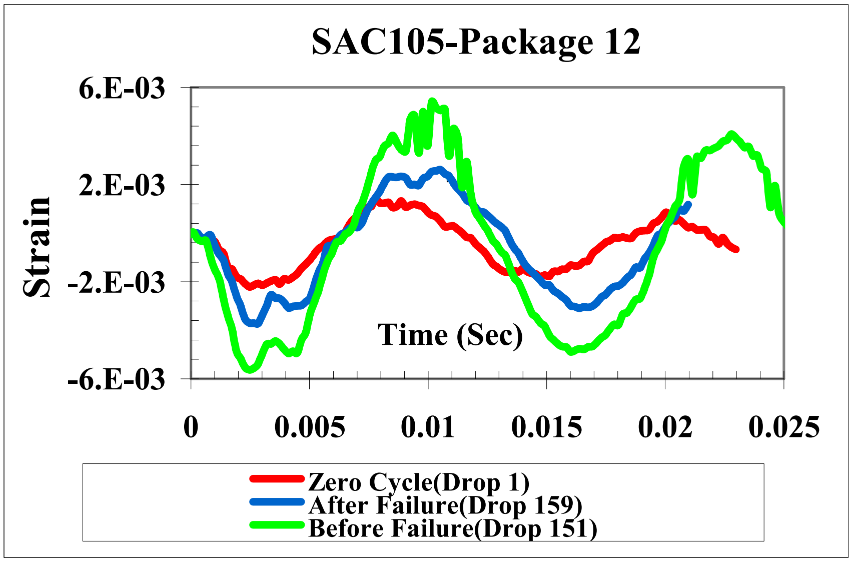


Figure 4.3: Strain Before and After Failure at Package 12 Location for SAC105 Alloy System on Test Board F

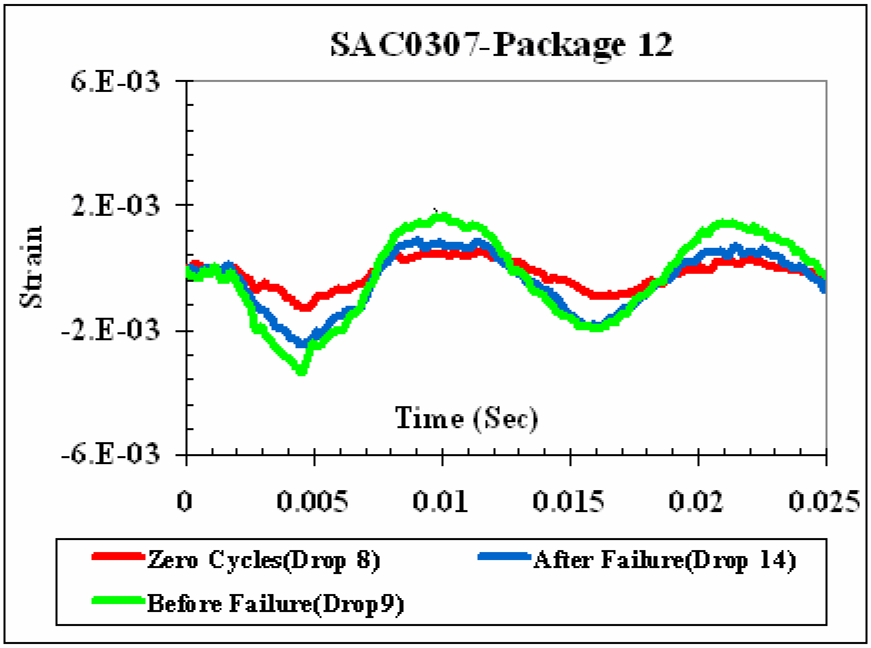


Figure 4.4: Strain Before and After Failure at Package 12 Location for SAC0307 Alloy System on Test Board F

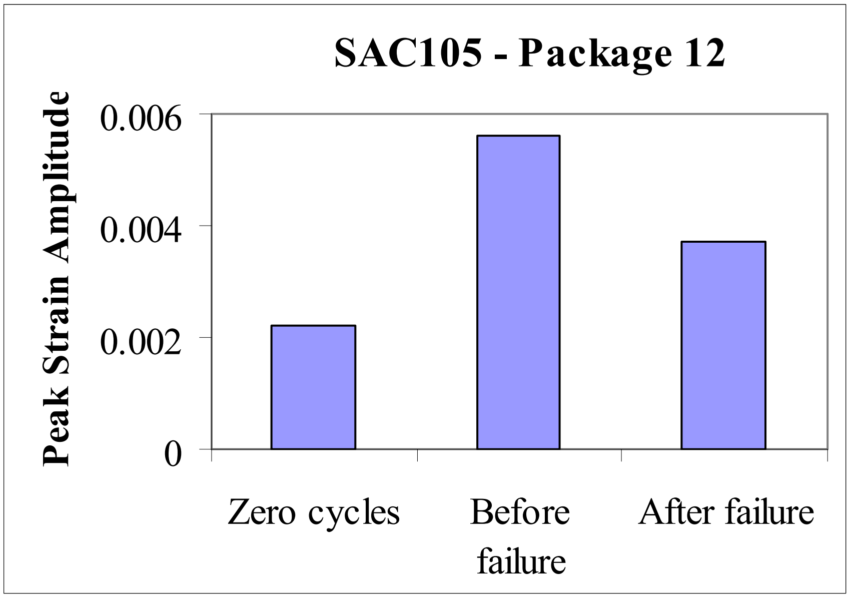


Figure 4.5: Peak Strain Values Before and After Failure at Package 12 Location for the SAC105 Alloy System on Test Board F

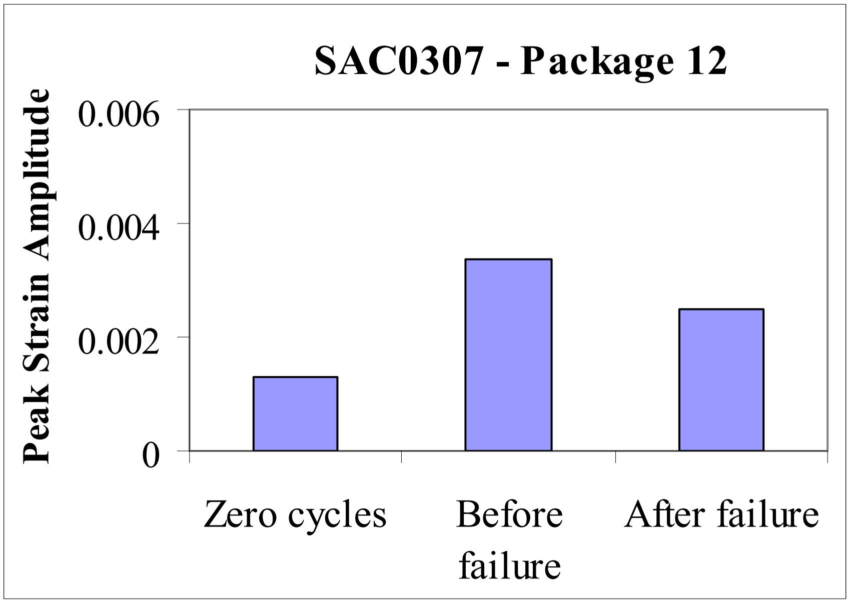


Figure 4.6: Peak Strain Values Before and After Failure at Package 12 Location for the SAC0307 Alloy System on Test Board F

4.4 Statistical Pattern Recognition Techniques

Statistical Pattern Recognition Technique (SPR) refers to the study of algorithms that recognize patterns in data and contains various sub-disciplines like discriminant analysis, feature extraction, error estimation, and cluster analysis. Some important application areas of SPR are image analysis, character recognition, and industrial inspection. In this thesis, statistical pattern recognition is used to study the degradation of reliability in electronic assemblies due to shock and drop. In the presence of multiple failure modes, health monitoring of assemblies was investigated by observing the confidence values computed by applying SPR techniques to the transient-strain response, transient displacement-response, vibration mode shapes, and frequencies of the electronic assembly under shock and drop. Correlation of structural response, damage proxies and underlying damage was accomplished with high-speed digital image correlation and high-speed data-acquisition. Here three SPR techniques, namely, the wavelet packet decomposition approach, the Mahalanobis distance approach and the Fast Fourier Transform (FFT) approach have been investigated.

Wavelet Packet Decomposition Approach

Wavelets have been used in several areas including data and image processing [Martin 2001], geophysics [Kumar 1994], power signal studies [Santoso 1996], meteorological studies [Lau 1995], speech recognition [Favero 1994], medicine [Akay 1997], and motor vibration [Fu 2003, Yen 1999].

The wavelet transform is defined by

$$Wf(u,s) = \langle f, \psi_{u,s} \rangle = \frac{1}{\sqrt{s}} \int_{-\infty}^{+\infty} f(t)\ \psi^{*}\left(\frac{t-u}{s}\right) dt \tag{4.1}$$

where the base atom ψ* is the complex conjugate of the wavelet function which is a zero average function, centered around zero with a finite energy. The function f(t) is decomposed into a set of basis functions called wavelets with the variables s and u, representing the scale and translation factors respectively.

An entropy-based criterion is used to select the most suitable decomposition of a given signal. This implies that at each node of the decomposition tree, the information gained by performing a split is quantified. Simple and efficient algorithms exist for both wavelet packet decomposition and optimal decomposition selection. Adaptive filtering algorithms, allow the Wavelet Packet transform to include the "Best Level" and "Best Tree" features that optimize the decomposition both globally and with respect to each node. For obtaining the optimal tree, a node is split into two nodes, if and only if the sum of entropy of the two nodes is lower than the sum of entropy of the initial node. After the wavelet packet transform, the wavelet packet energy is calculated at each node of the decomposition tree. An energy signature E_n for each sequence of wavelet packet coefficients $C^{p}_{n,k}$, for n = 0, 1, 2….4^{p-1} can be computed by using the formula

$$E_n = \frac{1}{N^2} \sum_{k=1}^{N} \left| C^{p}_{n} \right|^2 \tag{4.2}$$

where N is the total number of points in the signal at a given node in the wavelet packet tree, p is the decomposition depth, and C_i is the wavelet packet coefficients obtained during the wavelet packet transform at the particular node where energy is being calculated. The feature vector of length 4^{p-1} is formed for the signal. The packet energies obtained from the wavelet packet decomposition of the various mode shapes and frequencies of vibration of the electronic assembly are the basis for the computation of confidence values for health monitoring.

Mahalanobis Distance Approach

The Mahalanobis Distance classification is similar to the maximum likelihood classification except for the class co-variances which are all assumed to be equal. Hence this approach is more efficient. It is based on correlations between variables by which different patterns can be identified and analyzed. It is a useful way of determining similarity of an unknown sample set to a known one. It differs from Euclidean distance method in that it takes into account the correlations of the data set. The Mahalanobis distance from a group of values with mean $\mu = (\mu_1, \mu_2, \mu_3, \mu_4, \ldots\ldots, \mu_n)$ and covariance matrix Σ for a multivariate vector $(x = x_1, x_2, x_3, x_4, \ldots\ldots, x_n)$ is,

$$D_M(x) = \sqrt{(x-\mu)^T \Sigma^{-1} (x-\mu)} \tag{4.3}$$

Mahalanobis distance can also be defined as dissimilarity measure between two random vectors x and y of the same distribution with the covariance matrix Σ,

$$\mathbf{d}(\vec{\mathbf{x}}, \vec{\mathbf{y}}) = \sqrt{(\vec{\mathbf{x}} - \vec{\mathbf{y}})^T \boldsymbol{\Sigma}^{-1} (\vec{\mathbf{x}} - \vec{\mathbf{y}})} \tag{4.4}$$

The Mahalanobis distance approach has been chosen over other classification approaches as it considers the variance and covariance of the variables as opposed to only the average value. The distance measured is taken as a basis for the calculation of the confidence values for prognostics.

Fast Fourier Transform Approach

Fourier transform is a widely used tool in real-time signal analysis and has found application in several areas such as speech recognition [Nwe 2003, Polur 2005, Prasanthi 2005, Sakurai 1984, Tin 2005, Wang 1996], biomedical signals [Cesarelli 1990, Clayton 1993, Cote 1988, Pannizzo 1988], image processing [Ahlvers 2003, Zhu 1990, Uzun 2003], solving differential and integral mathematical equations [Branick 2004, Helms 1967, Olejniczak 1990, Qing 2000], geology [Axelsson 1997, Liu 1988], and astronomy [Kulkarni 1995]. The Fast Fourier Transform (FFT) is an efficient algorithm to compute the Discrete Fourier Transform (DFT) and reduce the computation time for N size signal from $O(N^2)$ to $O(N\log_2(N))$ [Cochran 1967, Cooley 1967, Chu 2000]. The FFT algorithms are based on two classes of decimation techniques: decimation in time and the decimation in frequency. The DFT requires the computation of the product of a matrix, called the DFT matrix where the matrix components are the twiddle factors with the signal being transformed represented as a vector. Though the DFT can be applied to any kind of real or complex signal, the computation time required to process large size signals is a limitation. Some of the algorithms available to perform the FFT are the Cooley-Tukey, Prime-factor, Bruun's, Rader's and Bluestein's FFT algorithm. The decimation in time FFT is computed by splitting the data over the odd and even index k of the input signal [Cooley 1965, Cochran 1967]. The decimation in frequency FFT is obtained by decimating the frequency spectrum data into even-indexed and odd-indexed sets. The decimation in frequency algorithm is applied when the data is in the frequency domain.

Frequency band energies were calculated and the vectors of the energies obtained were used as feature vectors to perform prognostics and damage monitoring.

The above mentioned techniques were used to show the degradation in the reliability of the electronic packages when subjected to shock and drop loading. Figure 4.7 shows a very small decrease in the confidence value in Package 8 for the SAC305 alloy system for 6 successive drops before failure. This is consistent with the expectation of having a high level of confidence with repeatable drops. The trend was verified by comparing histograms for package 8 and package 9 of the SAC305 alloy system for 8 successive drops as shown in Figure 4.8 and Figure 4.9 respectively. The repeatable drops were used to develop the training signal for the statistical pattern recognition techniques. Figure 4.10, Figure 4.11 and Figure 4.12 show the degradation observed in confidence values in package 13 for the six alloy systems calculated by the three different techniques. These plots indicate a decrease in reliability in the package with increase in cycle count.

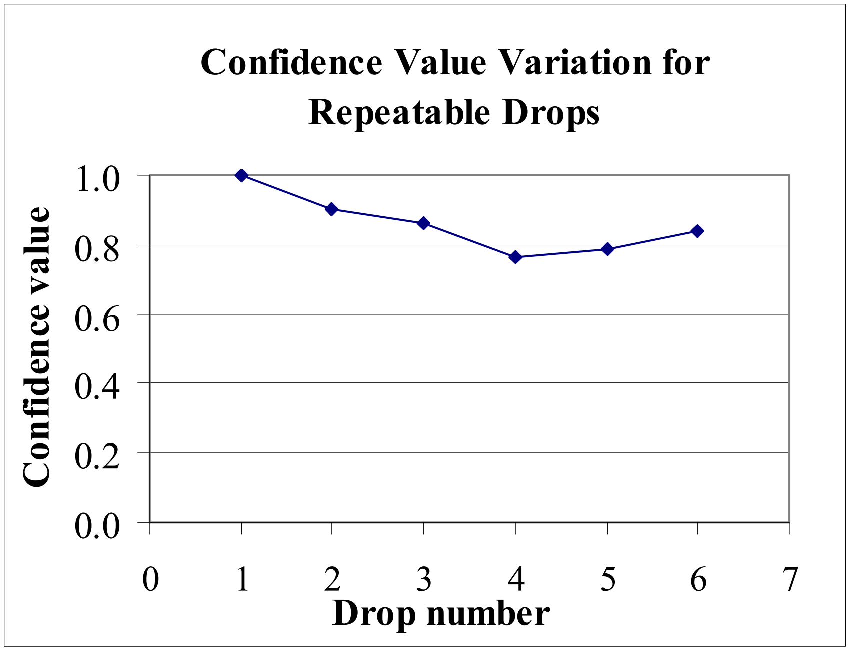


Figure 4.7: Confidence Value for 6 Successive Drops at Package 8 Location for SAC305 Alloy System

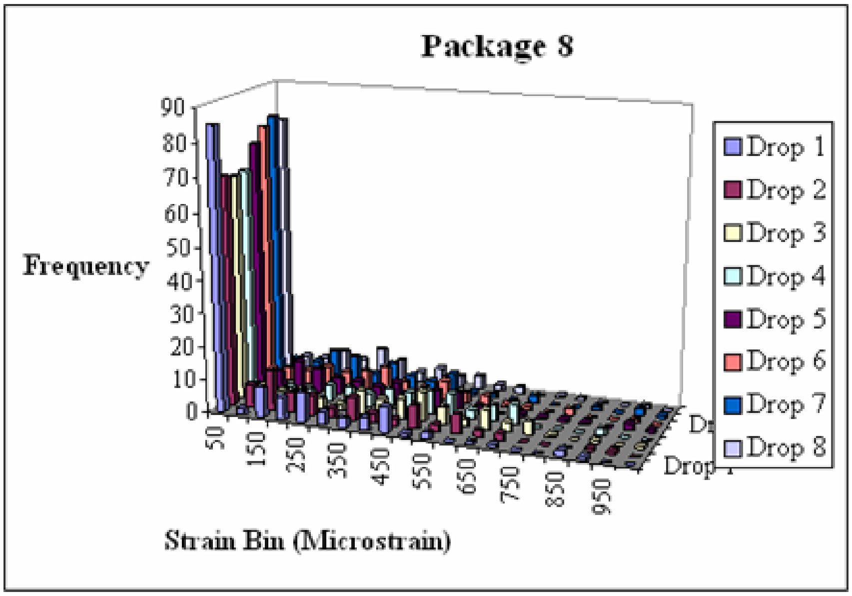


Figure 4.8: Comparison of Histograms for Successive Drops at Packages 8 Location for SAC305 Alloy System

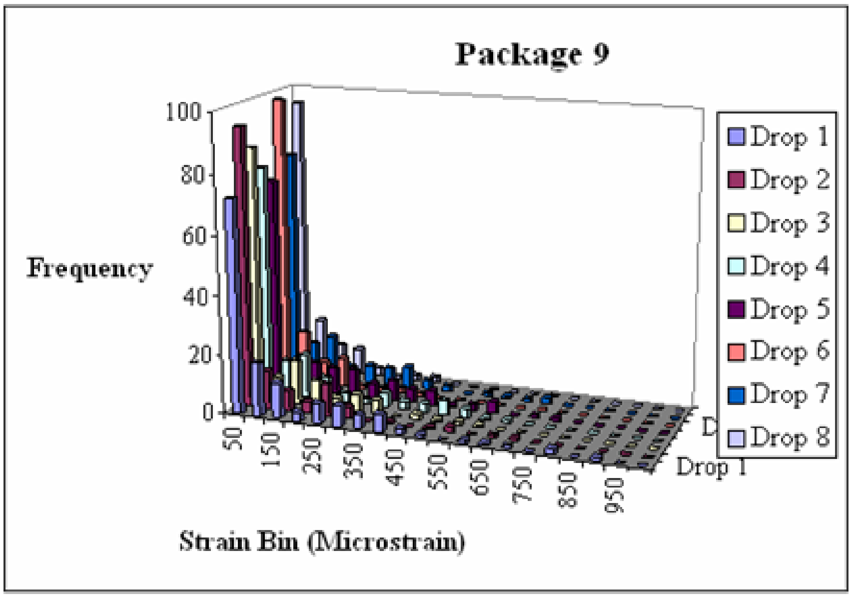


Figure 4.9: Comparison of Histograms for Successive Drops at Packages 9 Location for SAC305 Alloy System

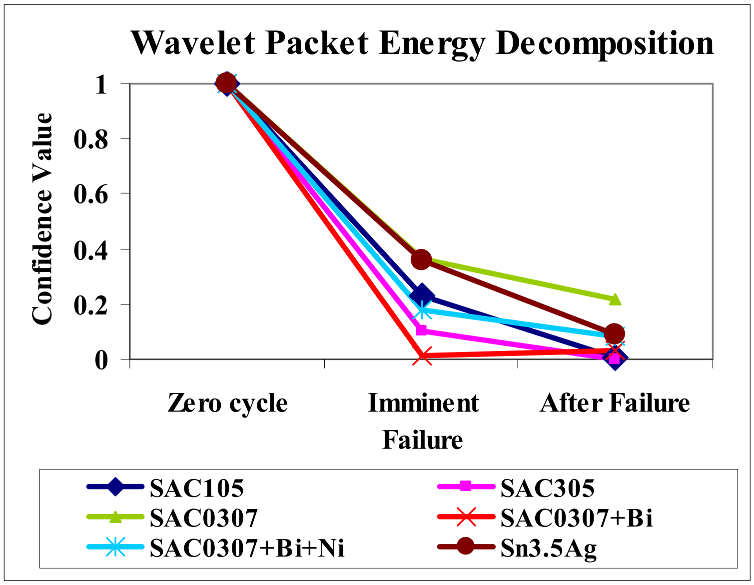


Figure 4.10: Confidence Value Degradation in the Six Alloy Systems using Wavelet Packet Energy Decomposition Approach

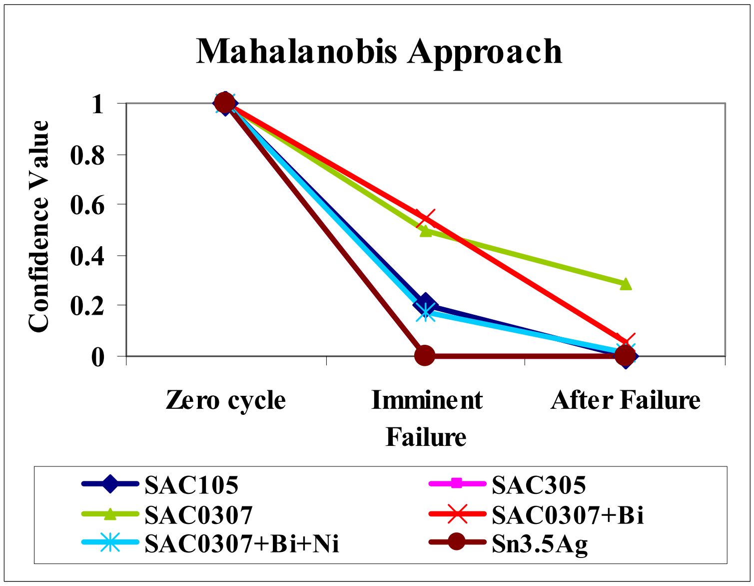


Figure 4.11: Confidence Value Degradation in the Six Alloy Systems using Mahalanobis Approach

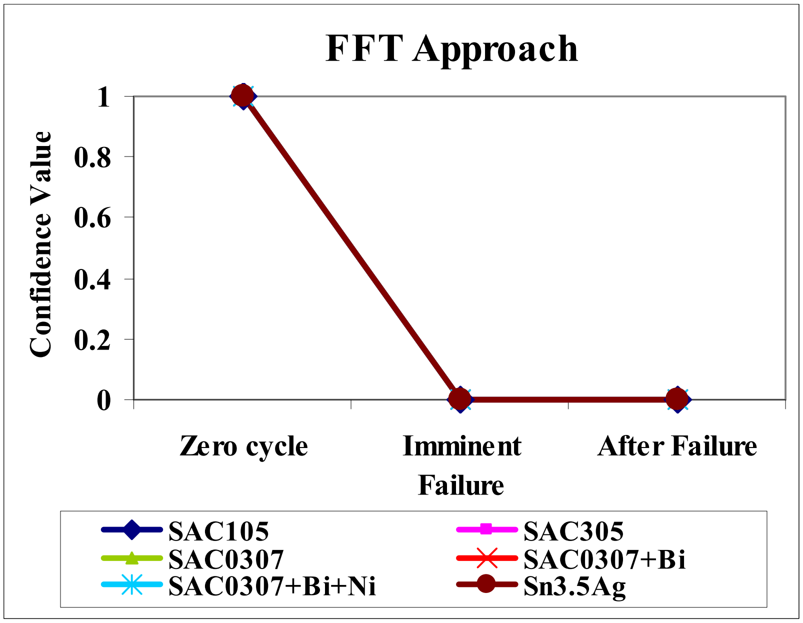


Figure 4.12: Confidence Value Degradation in the Six Alloy Systems using Fast Fourier Transform Approach

CHAPTER 5

SURVIVABILITY ENVELOPE BASED ON RELATIVE DAMAGE INDEX FOR LEADFREE ALLOY COMPOSITIONS

5.1 Introduction

In this chapter, failure modes are examined for the various alloy systems investigated in this study. Weibull plots were used for reliability prediction. Data on identification of damage proxies for competing failure mechanisms at the copper-to-solder, solder-to-printed circuit board, and copper-to-package substrate are presented. Manifestation of damage was examined through analysis of observed failure modes. The damage proxies developed could be used on strain response from simulation or from experimental data in controlled drop or shock tests. The damage accumulation due to progressive drop was also studied.

5.2 Reliability Analysis of Lead-Free Alloy Systems

In this section, the performance of CABGA with the different SAC alloy systems under impact testing according to the JEDEC test standards is discussed. Figure 5.1 shows a Weibull distribution, comparing the reliability of six different SAC alloys with ENIG board finish at room temperature. Results indicate that SAC305, SAC0307, and SAC105 exhibit superior characteristic life amongst the SAC alloy systems and Sn3.5Ag is the least reliable. Investigation of failure modes of lead free SAC solder alloys when subjected to drop tests can give a lot of insight into the various failure mechanisms in these systems. Research has shown that the different combinations of surface finishes and alloy systems can cause varying affects on impact reliability.

In this study, the failed packages were cross-sectioned and Scanning Electron Microscope (SEM) images revealed the different failure modes. Based on the images, failures were classified into five types: mode A, B, C, D and E as listed in Table 5.1 and illustrated in Figure 5.2. The various failure mechanisms observed in these alloys include copper trace failures, copper - solder interconnect failure on the package and board side and bulk solder failures. Higher stresses were developed on the solder-component side compared to solder-board side due to strain hardening effect of SAC alloys under repetitive loading. Figure 5.3 to Figure 5.8 illustrate the prominent failure modes in the six alloy systems. A comparison of the percentage of these different modes observed in the alloy systems is plotted in Figure 5.9. It can be clearly seen from this figure that the prominent failure mode in SAC0307 was copper trace failure, while Sn3.5Ag showed prominent copper-solder interconnect failure on the component side. SAC105 showed mixed failure modes while SAC305 showed cracking at the IMC layer on the package side. Failure modes in SAC alloys with impurities such as Bi included bulk solder cracking while Ni caused failure at IMC on the board side of the interconnect.

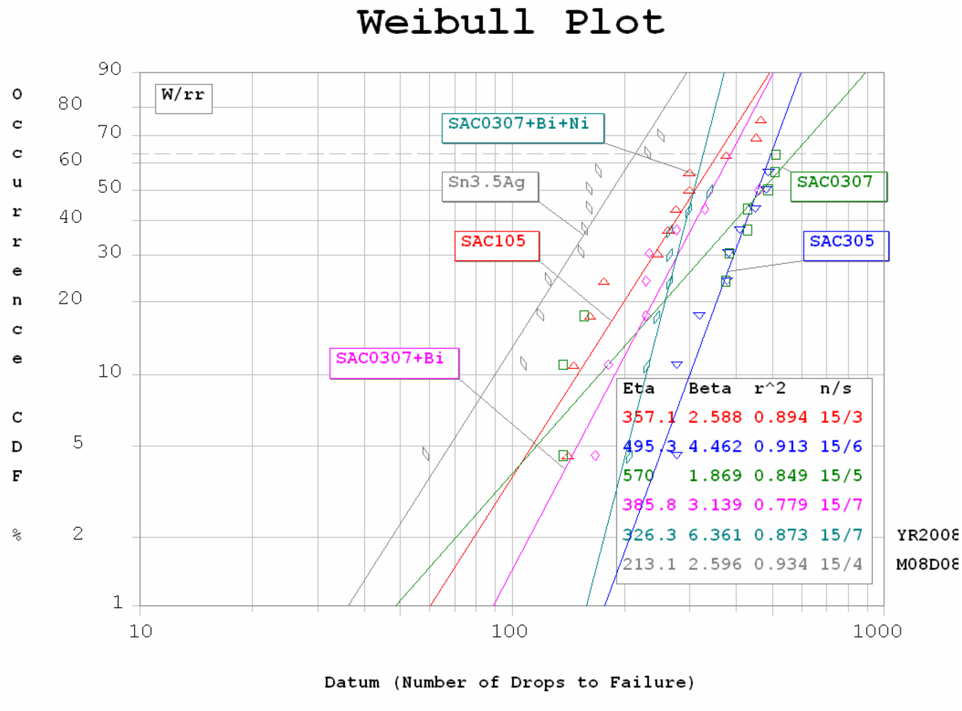


Figure 5.1: Weibull Distribution of 10mm-100 I/O Components for the Various Solder Alloy Systems on Test Board F

Table 5.1: Failure Mode Description

Failure Mode	Description
A	Solder-Copper pad interfacial failure on Package side
B	Solder-Copper pad interfacial failure on PCB side
C	Resin Crack
D	Copper trace failure
E	Copper-PCB failure

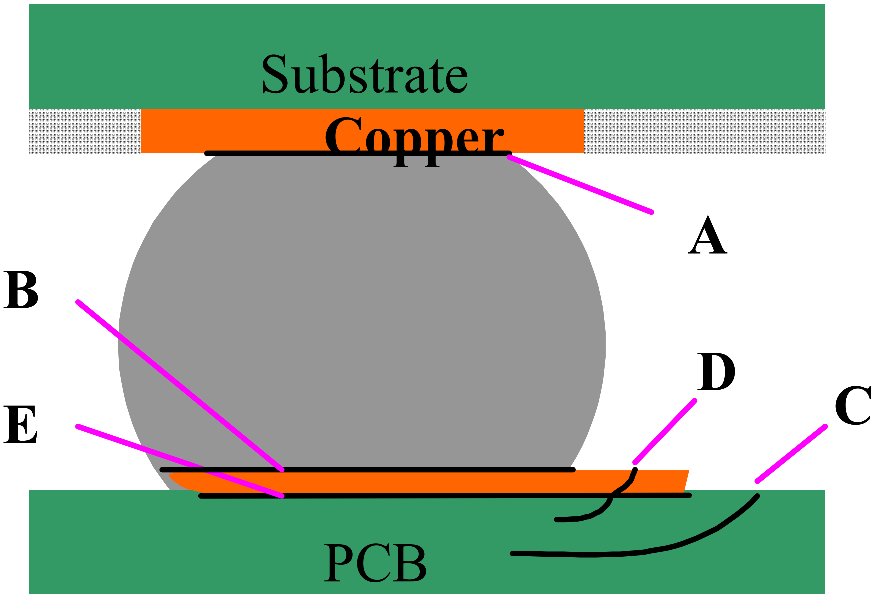


Figure 5.2: Failure Modes

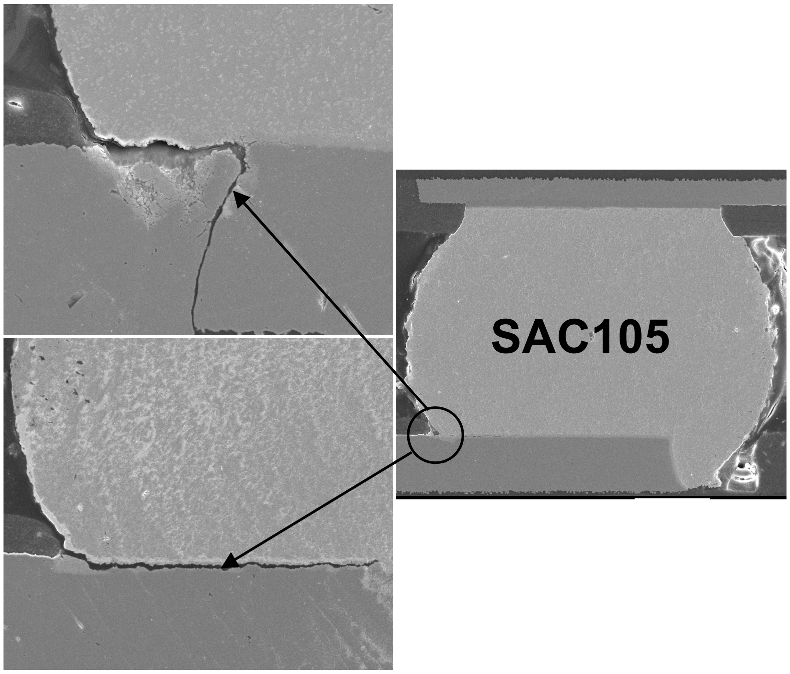


Figure 5.3: Failure Modes observed in SAC105 Solder Joints

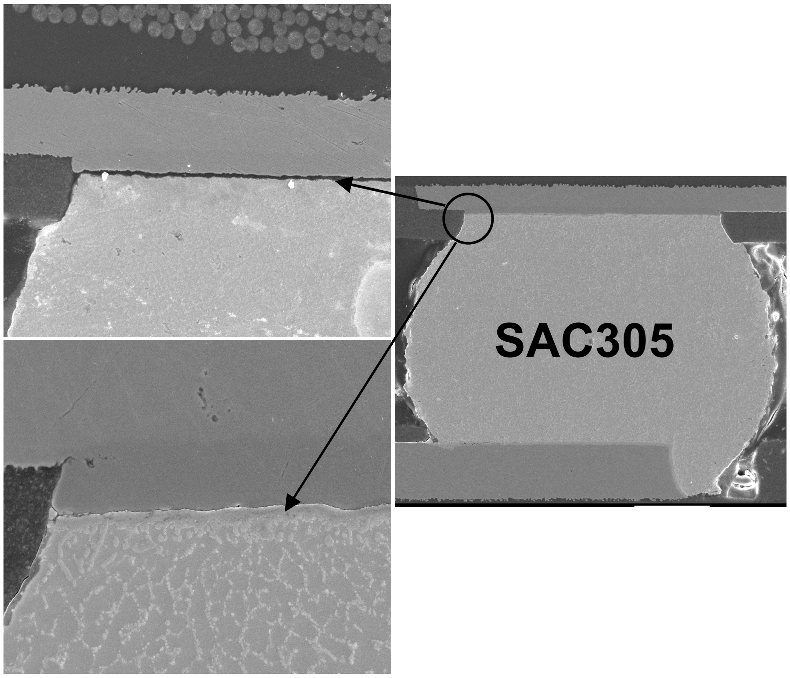


Figure 5.4: Failure Modes observed in SAC305 Solder Joints

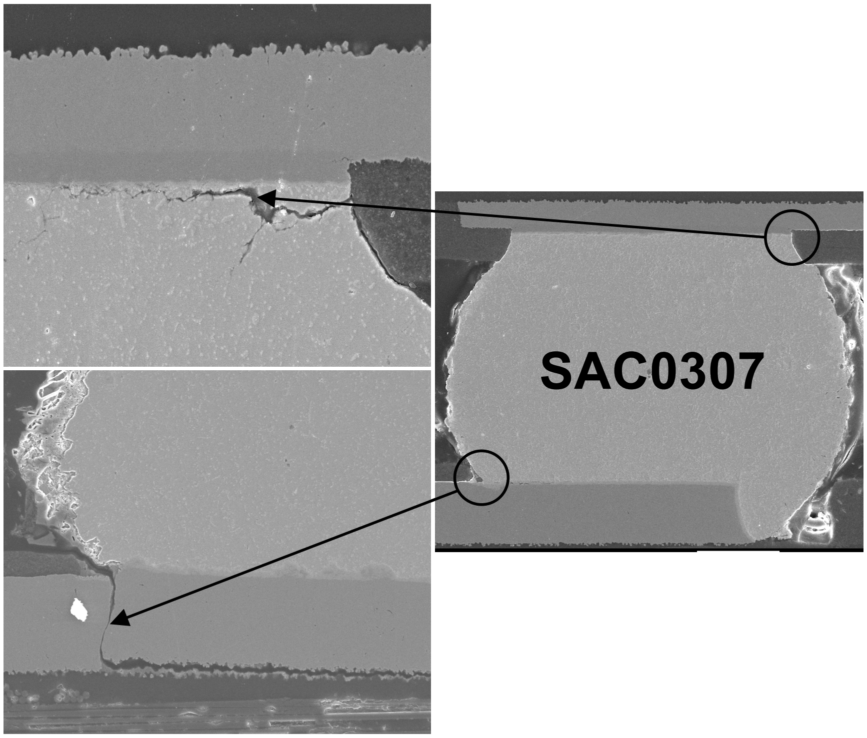


Figure 5.5: Failure Modes observed in SAC0307 Solder Joints

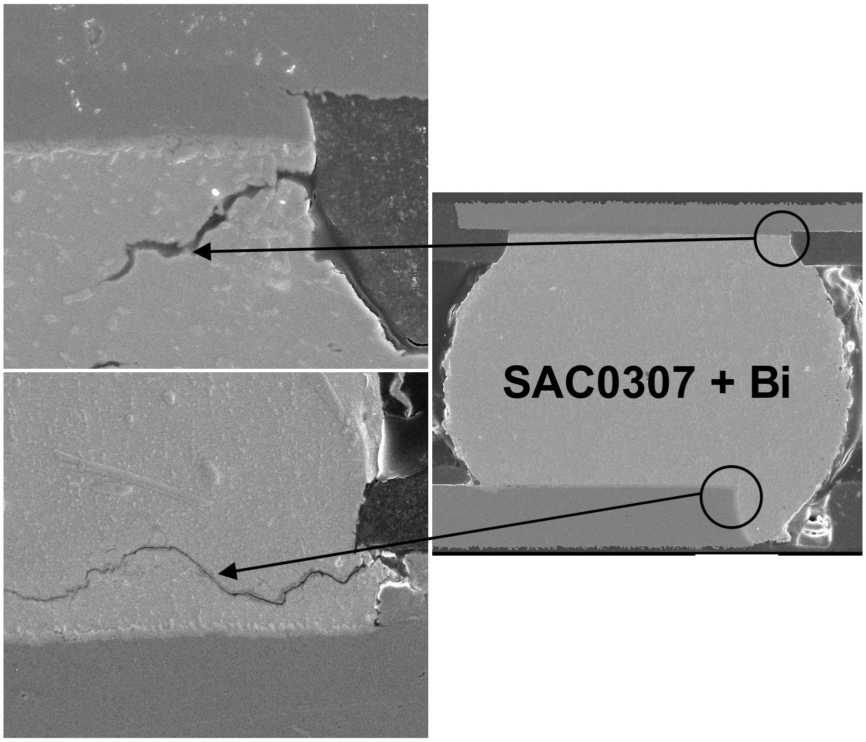


Figure 5.6: Failure Modes observed in SACX Solder Joints

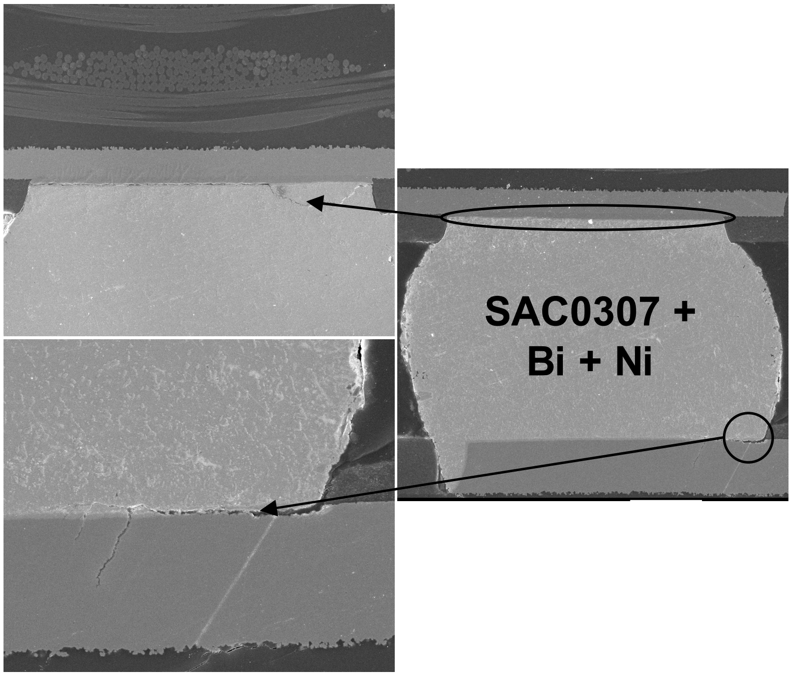


Figure 5. 7: Failure Modes observed in SACX-Plus Solder Joints

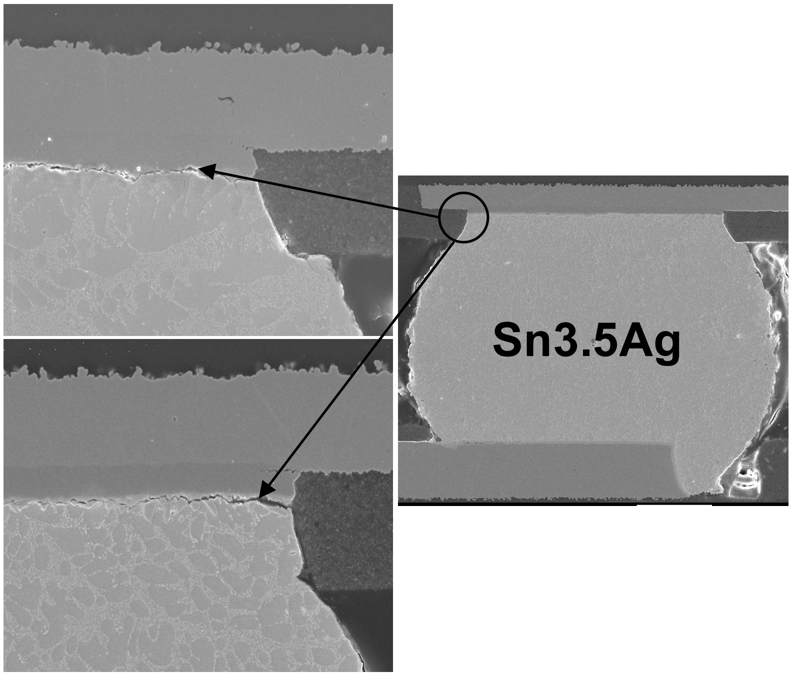


Figure 5.8: Failure Modes observed in SnAg Solder Joints

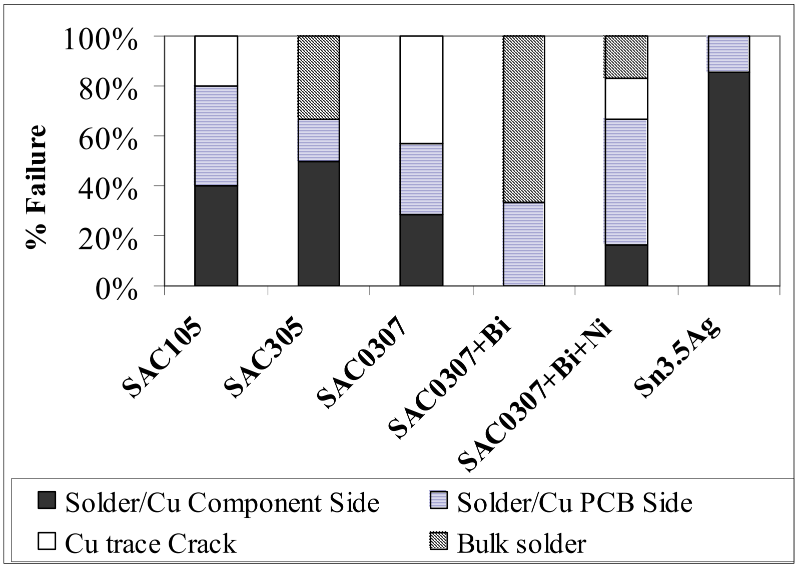


Figure 5.9 : Comparison of Failure Modes in the Six Different Alloy Systems

5.3 Damage Index based Survivability Envelope

An electronic assembly subjected to shock-impact, may experience loads which vary in both amplitude and frequency. The Daubechies, D10 wavelet with 12-level decomposition was used to investigate the transient strain response acquired at specific points on the test vehicle. Rainflow analysis was then used as the cycle-counting algorithm for which the second approximation, A2 was used as input. Histograms of load cycle amplitudes and number of cycles were calculated from this transient dynamic data in the time domain. The transient strain signal analyzed, had a large number of very small strain amplitude cycles and very few large strain amplitude cycles. Damage from repeatable and non-repeatable drops was investigated. The strain histograms for repeatable drops as seen in the previous section were very similar. Damage was computed for each component, till failure. All information about the sequence of the individual strain variation was lost during counting. The resulting cumulative frequency distribution histogram gave the overall number of load cycles for each of the load amplitudes. A relative damage index was defined such that the damage magnitude at failure is “1”. Linear superposition of damage was assumed in this study. Based on the assumed logarithmic relationship between strain and number of cycles given by the Coffin-Manson Relationship, the equation can be rewritten as follows:

$$\sum_{k=1}^{M} \frac{D_k}{D} = 1 \tag{5.1}$$

$$\sum_{k=1}^{M} \frac{N_k}{A\left(\frac{\Delta\varepsilon_k}{2}\right)^n} = 1 \tag{5.2}$$

where, k is the bin-index for the histogram, $\Delta\varepsilon/2$ is the strain amplitude, M is the total number of bins in the histogram, N is the number of cycles subjected on the sample in the k^{th} histogram bin during all the drops until failure of the device, and D is the damage index. For solving, consider the following equations,

$$\left(\sum_{k=1}^{N} \frac{N_k}{A\left(\frac{\Delta\varepsilon_k}{2}\right)^n} \right)_i = 1, \qquad \left(\sum_{k=1}^{N} \frac{N_k}{A\left(\frac{\Delta\varepsilon_k}{2}\right)^n} \right)_{i+1} = 1 \tag{5.3}$$

where the index i indicates the drop number. Each data set included test vehicles which were dropped-to-failure; therefore the cumulative relative damage index is 1. The load histories were differed by varying the angle of impact by a small magnitude. Subtracting the two equations, we get,

$$\left(\sum_{k=1}^{N} \frac{N_k}{\left(\frac{\Delta\varepsilon_k}{2} \right)^n} \right)_i - \left(\sum_{k=1}^{N} \frac{N_k}{\left(\frac{\Delta\varepsilon_k}{2} \right)^n} \right)_{i+1} = 0 \tag{5.4}$$

Solution of the difference equation for the electronic assemblies for each alloy, gives the exponent, n and coefficient A over the complete data-set. Average values of the exponent, n and coefficient A were computed over the complete data. The model predictions of PCB strain were correlated with the measurement from DIC. The strain history was then extracted from the simulation model. The relative damage in any particular drop was computed based on total damage at failure. The advantage of the proposed approach is that it can be used to calculate damage in the test structures of interest, instead of an idealized test specimen. The test samples were cross-sectioned after failure, and the test data was sorted based on failure modes. Solder joint failure were predominant in the test samples examined in this study, however, other failures modes including copper-trace cracking and printed-circuit board resin cracks were also encountered. It is anticipated that the cumulative damage will be different for different failure modes.

In this thesis, only samples with solder joint failures are examined. The values of the exponent, n and coefficient A were calculated for the six alloy systems. Figure 5.10 and Figure 5.11 show the damage index plots for package 8 on the SAC105 board and package 13 on the SAC305 board. The damage progression can be seen very clearly from these plots with the damage index reaching 1 at failure. The relative damage index was used to predict the number of drops-to-failure for all the six-alloys analyzed. The location for the predictions is different from location at which the experimental data was acquired. Therefore, the transient strain history and the damage progression were also different.

The relative damage index approach outlined in this section provides a method to define the survivability envelope for packaging architectures. The proposed methodology enabled evaluation of the survivability envelope in the application of interest and for the packaging architecture in question. Damage during the life of the product should not exceed “1” for the design to have good survivability in drop and shock applications. The constants used for damage progression were specific to the solder alloy. The proposed methodology is amenable to implementation not just at board-level but also at system-level.

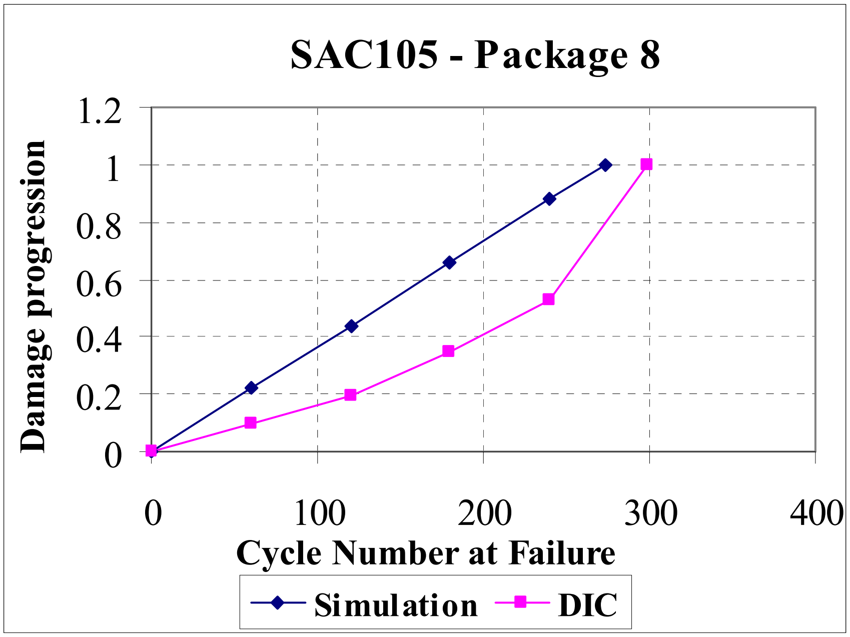


Figure 5.10: Damage Index Progression for SAC105 Alloy System

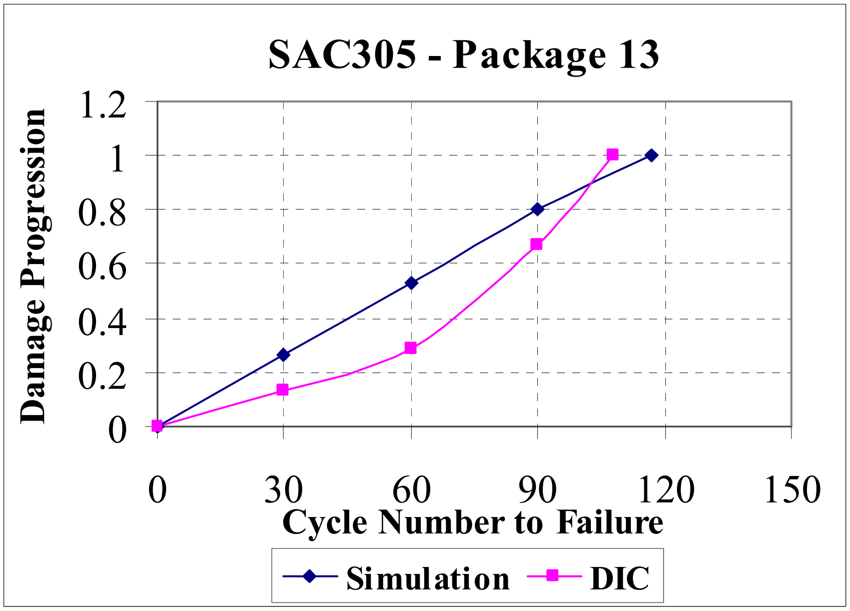


Figure 5.11: Damage Index Progression for SAC305 Alloy System

CHAPTER 6

SUMMARY AND CONCLUSION

Measurement of transient dynamic deformation kinematics can offer essential information in understanding the failure mechanisms of electronic assemblies subjected to impact. In this work, full-field strain measurement using Digital Image Correlation (DIC) was investigated for shock and vibration of electronic assemblies as an advantageous alternative to strain measurements at discrete locations with the help of strain gages. This work shows that accurate full-field measurements can be made using DIC in conjunction with high-speed imaging for electronic assemblies with various packaging architectures, including Flex-BGA, Tape array BGA, C2BGA, PQFN and PBGA. Transient impact strain histories were measured in two orientations, namely, 0º JEDEC and the 90º vertical drop orientations. Repeatability of the setup was characterized, as it is critical to the measurement of repeatable responses. Full field strain data from DIC was correlated with high speed strain measurements with the help of strain gages at different locations on the specimen test vehicles. Six-different lead-free alloy systems were investigated, namely, Sn1Ag0.5Cu, Sn3Ag0.5Cu, Sn0.3Ag0.7Cu, Sn0.3Ag0.7Cu-Bi, Sn0.3Ag0.7Cu-Bi-Ni, and 96.5Sn3.5Ag. Results indicated that SAC105, SAC0307, and SAC305 showed better performance amongst the SAC alloy systems and Sn3.5Ag was the least reliable.

Explicit finite element models were constructed for all the electronic assemblies to simulate transient-impact. Different modeling methods such a smear property models and Timoshenko beam model were investigated. Model predictions, including strain and deformation contours, showed good correlation with experimental strain gage and DIC data. The potential of damage recognition and tracking for various solder alloys was investigated. Data on identification of damage proxies for competing failure mechanisms at the copper-to-solder, solder-to-printed circuit board and copper-to-package substrate were presented. Failure modes for the various alloys were compared and reported. A damage-index based survivability envelope was developed for the lead-free alloy systems. Life prediction for the alloy systems using strain histories from simulation and experiment was correlated for the JEDEC configuration. Strain histories were also compared at various stages of the experiment to conclude that as the cycle number increases during the test, the strain in the solder interconnects increases up to failure, after which the values plunge.

Statistical Pattern Recognition (SPR) was used to analyze the transient strain measurements and the ability to monitor in-situ health of the electronic assemblies was examined. SPR was also used to study the effect of damage progression for various types of packaging architectures. Confidence values of the transient-strain response were computed using Wavelet Packet Energy Decomposition, Mahalanobis distance and FFT approach. Results showed that the confidence value degradation of the transient strain feature vector from DIC can be used as a leading indicator of failure. Damage accumulation due to progressive drop was studied. Degradation of confidence values prior to failure were correlated with the occurrence of failure.

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APPENDIX

LIST OF SYMBOLS

D	Degree of Freedom Vector
n	Time Step
M	Mass Matrix
Δt	Time Increment
C	Damping Matrix
Δt_{cr}	Critical Time Increment
ω_{max}	Maximum Natural Frequency
K	Stiffness Matrix
C_n	Courant Number
Δt_{actual}	Actual Time Increment
F	Force
a	Acceleration
ψ	Wavelet Transform Function
s	Scale Factor

u	Translation Factor
ψ^*	Complex Conjugate of Wavelet Function
E_n	Energy Signature
N	Number of points in a signal at a given node in a wavelet packet tree
C_i	Wavelet Packet Co-efficient
p	Decomposition Depth
μ	Mean
Σ	Covariance Matrix
D_M	Mahalanobis Distance
I_1	Reference Image
I_2	Deformed Image
$U(r)$	Displacement Vector
r	Pixel
C_A	Absolute Difference Correlation
C_L	Least Square Correlation
C_C	Cross Correlation
k	Bin Index

$\Delta\varepsilon/2$	Strain Amplitude
i	Drop Number
A, n	Constants
R_{int}	Internal force-vector
R_{ext}	External force-vector