DESIGN OF MEMS-BASED TUNABLE ANTENNAS, ORGANIC TRANSISTORS

AND MEMS-BASED ORGANIC CONTROL CIRCUITS

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DESIGN OF MEMS-BASED TUNABLE ANTENNAS, ORGANIC TRANSISTORS AND MEMS-BASED ORGANIC CONTROL CIRCUITS

Madhurima Maddela

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DESIGN OF MEMS-BASED TUNABLE ANTENNAS, ORGANIC TRANSISTORS

AND MEMS-BASED ORGANIC CONTROL CIRCUITS

Madhurima Maddela

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Signature of Author

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Date of Graduation

VITA

Madhurima Maddela, daughter of (Late) Dr. M. S. Venkateswarlu and (Late) Dr. M. Sundaramma, was born on June 25, 1981 in Tirupathi, India. She graduated with a Bachelor's of Electronics and Communications Engineering in July 2002 from Osmania University, Hyderabad, India. She then joined the Electrical and Computer Engineering department of Auburn University as a graduate student in January 2003. The focus of her graduate research was on designing antennas for radio frequency identification systems and the realization of a wireless mobile sensor platform for the detection of pathogens in food products. After receiving her master's degree, she has been working on (Microelectromechanical systems) MEMS devices, employing them for different applications like developing MEMS-based tunable antennas and integration of MEMS devices with organic transistors.

DISSERTATION ABSTRACT

DESIGN OF MEMS-BASED TUNABLE ANTENNAS, ORGANIC TRANSISTORS AND MEMS-BASED ORGANIC CONTROL CIRCUITS

Madhurima Maddela

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The advent of precision three-dimensional micromachining technologies in the last couple of decades has seen the birth of an exciting and potentially revolutionary field called Microelectromechanical Systems (MEMS). Predictions about the far-reaching implications and widespread prevalence of such miniaturized, smart, integrated systems and sub-systems have been made and yet as of today only modest market presence and commercial success has been attained. Having arisen out of the silicon IC microfabrication technology in academic and research environment, the initial developments in MEMS were driven mainly by technical curiosity and demonstrability. Like in any emerging field, most of the developments have therefore been an array of new fabrication techniques, new materials, and new device structures for a host of sensor

and actuator applications. However, the commercial viability and success of MEMS devices in the industrial and academic communities require tackling some of the daunting technical and commercialization issues impeding the market presence of such systems.

This dissertation explores two varied and vital applications of MEMS devices. One application involves the development of MEMS-based tunable antennas and the other explores the integration of MEMS sensors with organic transistors.

Tunable antennas are drawing interest because instead of having multiple antennas switched into multiple transceiver chains covering different frequency ranges, a single multi-band tunable antenna assembly would provide size advantages and minimize product packaging complexity. This dissertation demonstrates a coplanar patch antenna made tunable by the use of a MEMS varactor.

The second application explored was to develop a ‘Polymer Microsystem’ by the integration of a Polymer MEMS device and Organic Electronics. Traditionally, microsystems have been fabricated using silicon-like semiconductor substrates by micromachining techniques. Silicon (or thin-film in general) may be the ideal substrates for semiconductor devices, but they may not be suitable for all microsystem applications. In particular, silicon based wafer level technology may not be suitable for cost effective manufacturing and packaging of microsystems for large area and large volume applications. The proposed work was to demonstrate a plastic microsystem using low cost fabrication techniques. As a proof-of-concept of the proposed plastic microsystem, this project demonstrated the integration of a Polymer MEMS pressure sensor with an organic field effect transistor.

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A special mention goes to my husband, Subramanian Nambi, the wind beneath my wings, and my in-laws and extended family, who have enthusiastically supported the pursuit of my doctoral program.

I would like to dedicate this dissertation to my late parents, Dr. M. S. Venkateswarlu and Dr. M. Sundaramma whose lives will always inspire me to be the best that I can be.

Style manual of journal used Graduate School Guide to preparation and submission of theses and dissertation

Computer software used Microsoft Office XP

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER I: INTRODUCTION

In recent years, miniature electromechanical components suitable for Microsystem applications have been developed by Micro-electro-mechanical Systems (MEMS) technologies. A MEMS system involves the fabrication of mechanical elements, sensors, actuators, and electronics on a common substrate through the utilization of micro-fabrication technology. Typical sizes for MEMS components range from nanometers to millimeters (100 nm to 1000 μm). The characteristics of MEMS components are low-cost, high functionality, and small size and light weight. MEMS devices can sense, control and actuate on micro-scale, and function individually (or in combination with other devices) to generate macro-scale effects. MEMS devices are already in mass use in applications ranging from inertial sensors for automobile airbags to monitoring patient blood pressure at the bedside [1]. Microsystems/MEMS have proved to be a revolutionary technology in many application arenas, including accelerometers, pressure sensors, displays, inkjet nozzles, optical scanners, and fluid pumps. Typical examples for commercial MEMS devices/Microsystems include ADXL series accelerometers from Analog Devices Inc., pressure sensors and accelerometers from FreeScale Semiconductor Inc., DLP displays from Texas Instruments Inc., SiSonic MEMS microphone from Knowles Electronics Inc., etc. But, issues like the reliability and lifetime of MEMS

devices, and their packaging difficulties have given cause for skepticism about the growth of this industry.

1.1 Tackling MEMS Issues

For several years, reliability and packaging issues have prevented the insertion of MEMS switches in military and commercial systems. Ohmic contact MEMS switch reliability issues, such as failure due to stiction and contact degradation, have been observed to be the key failure modes. Stiction is the unintentional adhesion of the movable and fixed parts in MEMS caused by surface adhesion forces. In capacitive contact type MEMS switches, reliability issues such as stiction due to charge accumulation in the dielectric layer and downstate capacitance degradation with actuation are commonly encountered failure modes.

The typical lifetime requirement for military applications is in the range of 100-500 billion cycles. Over the past five years, steady progress has been made in improving both the reliability and packaging of RF MEMS switches. Many successful MEMS switches have been demonstrated with lifetimes in excess of 100 million cycles. Reliable MEMS switches are commercially available from TeraVicta Technologies and Radant MEMS Inc. Radant MEMS Inc. has demonstrated 900 billion cycles of operation for their ohmic contact switches. MEMtronics Corporation demonstrated over 100 billion cycles of switch lifetime for capacitive MEMS switches. TeraVicta switches have been tested up to 100 million cycles over the 0° to 70° C operating range of the device. Radant MEMS Inc. has developed a high-power MEMS switch with power handling in the range of 1 to 4 watts and is developing MEMS switches capable of handling up to 20 watts. Advantest

produces electro-thermally activated relays for use in Automated Test Equipment (ATE). The expected lifetime is greater than 20 million cycles. The Packaging issue is resolved by hermetic sealing of MEMS switches after completion of the micromachining process. Recent improvements in reliability and packaging make MEMS switches attractive for reconfigurable antenna applications [2].

1.2 Biasing considerations

MEMS devices typically require higher voltages than conventional semiconductor devices and thus would require high voltage DC sources in the antenna assembly. In spite of the high bias voltage requirements, the power consumption is low when compared to their semiconductor counterparts. MEMS devices integrated with RF circuits and antennas can be biased using resistive bias lines between the DC power supply and the MEMS devices. The resistive bias line allows a DC current flow from the DC power supply to the MEMS device. The resistance of the bias lines is designed to provide a high impedance path (> 10 kΩ for 0.1λ) from the MEMS device to the DC power supply and thus preventing the leakage of RF signal into the supply [2].

1.3 Frequency agile antennas

With the advent of RF MEMS switches, there has been a considerable interest in the development of multi-band reconfigurable antennas. Multi-mode, multi-band, and multi-standard mobile devices create the need to simplify RF front ends. Instead of having multiple antennas switched into multiple transceiver chains covering different frequency ranges, a single multi-band tunable antenna assembly would provide size advantages and

minimize product packaging complexity. Multi-band antenna technology can be fully utilized for seamless mobility of next generation wireless devices. Multi-band antennas can be created to cover combinations of existing law enforcement bands, Homeland Security applications, cellular bands, Wireless Local Area Network (WLAN) bands, Bluetooth, 3G applications, Ultra Wide Band (UWB), for both voice, video, and high-data-rate wireless communications with tunable performance, high RF power handling, and low power consumption. Two important characteristics parameters of an antenna are: 1) the operating frequency, and 2) the radiation pattern. RF MEMS devices can be integrated with antennas for altering the operating frequency (tunable/switchable antennas) and/or the radiation pattern (phase shifters). Chapter 2 describes a MEMS-based tunable antenna made tunable in the range 5.185 GHz to 5.545 GHz.

1.4 Organic electronics

An Organic Field Effect Transistor (OFET) belongs to a new class of electronics that can be fabricated directly on plastic films at ambient temparatures; therefore it is mechanically flexible, light-weight, very thin, shock resistant and easy to transport compared to their silicon-based counterparts. Weak Van der walls forces hold the organic semi-conductor molecules together. Low charge hopping from molecule to molecule is the major factor limiting the mobility of the semi-conductor. The main disadvantages of organic transistors are the low mobilities and slow switching times. But unlike traditional FETs, OFETs can handle much high voltages of the order of about 100 V. Some successful applications of organic electronics are Organic Light Emitting Diodes (OLEDs). Chapter 3 presents an all organic polymer transistor made using

BenzoCycloButene (BCB), a promising, moisture resistant dielectric and Pentacene, an aromatic compound from the Benzene family as the p-type semi-conductor. Integration of an OFET and OLED completes the need for controlling circuitry for the operation of the OLED, making it an independent all polymer micro-system. A similar integration of a MEMS-based pressure sensor and an OFET is presented in Chapter 4. This field is drawing a lot of interest now as some experiments have shown that bulk Silicon is susceptible to fatigue [3].

Chapter 5 presents the conclusions and suggests possible avenues for future work.

CHAPTER II: MEMS-BASED TUNABLE COPLANAR PATCH ANTENNA

In recent years, there has been a considerable interest in the development of tunable antennas because of the increasing number of global wireless standards in close proximity to one another. A single tunable antenna would eliminate the need for multiple antennas operating in various frequency bands. Several tunable printed antennas using varactor diode(s) were reported in [4]-[10]. The operating frequency of the antenna was altered by varying the DC bias applied to the varactor diode(s). With the advent of MEMS technology, there have been considerable research efforts in the development of frequency tunable and reconfigurable (or switchable) antennas using RF MEMS devices [1]-[21]. In [13], a patch antenna operating at 25 GHz was made tunable over a range of 1.6 %, i.e., 400 MHz. In [14], a tunable MEMS patch antenna using an electrostatic actuator with a wrapped metallization was reported. The area of the wrapped metallization was changed to obtain operating frequencies at 23.8 GHz and 12.4 GHz for 0 V and 150 Volts, respectively. In [15],[16], dual-band frequency reconfigurable planar antennas integrated with RF MEMS switches were reported. In [17], a triple-band reconfigurable microstrip antenna that employs two RF MEMS switches was reported. The antenna resonates at 1.8 GHz, 2.4 GHz, and 1.9 GHz with return losses better than 10 dB when both the switches are OFF, only one switch is ON, and both the switches are ON, respectively. In [18], a quadruple-band reconfigurable mini-nest patch antenna was

developed using half u-slots integrated with RF MEMS switches to achieve frequency bands like GSM (0.9 GHz), GPS (1.57 GHz), DCS (1.8 GHz) and WLAN (2.4 GHz and 5.2 GHz). The return losses were reported to be in the range of 14 dB to 22 dB. RF MEMS switches were also used in conjunction with fractal antenna structures to obtain a reconfigurable array antenna structure. In [19], a multi-band frequency reconfigurable modified sierpinski gasket type fractal antenna was reported. Different configurations of the fractal antenna were achieved using RF MEMS switches to obtain operation in multiple frequency bands ranging from 0.6 GHz to 1.95 GHz.

Recently, printed circuit board (PCB) process compatible MEMS-based frequency tunable and reconfigurable antennas have been reported in [20][21]. The advantages of PCB compatible MEMS technology include low cost, compatibility with organic laminate substrates, ease of integration with surface mount components, suitability for batch fabrication in large panels, and high volume manufacturing [22]. In [20], monolithic integration of RF MEMS switches with a diversity antenna on a PCB substrate was reported. In [21], a MEMS-based tunable circular microstrip patch antenna fabricated on a flexible Kapton polyimide film using printed circuit processing techniques was reported by our group. A 6 mm diameter circular patch antenna was reported that was tunable from 16.91 GHz at 0 V to 16.64 GHz at 165 V, for a tuning range of 270 MHz.

2.1 Tunable Antenna Design and Simulation

A Coplanar Patch Antenna (CPA) made tunable using a MEMS varactor fabricated using printed circuit processing techniques is investigated in this chapter. CPAs have

many advantages like low radiation loss, low dispersion, and uni-planar configuration. Due to their uni-planar configuration, CPAs facilitate integration with coplanar feed lines that enable shunt and series mounting of active and passive components. They also exhibit wider bandwidth and lower cross-polarization radiation as compared to microstrip patch antennas [4]. The concept of a coplanar antenna structure was first introduced by J. W. Greiser [23]. The antenna consists of a patch surrounded by a closely spaced ground conductor, and is suitable for being fed using Coplanar lines. Electromagnetic (EM) field simulations of the structure revealed that the antenna behaves more like a microstrip patch antenna than a loop slot antenna. Particularly, the resonant frequency of the antenna is primarily determined by the patch length (L) of about a half guide-wavelength instead of the total loop size. Electromagnetic simulations also show that the electric field distributions around the slots of the CPA resemble that of the microstrip patch edges. The variation of the input impedance of the CPA with the length of the patch exhibits a behavior similar to that of a microstrip patch. This characteristic allows impedance matching of the CPA to the feed line by only adjusting the width, W of the patch. In the following sections, design, simulation, fabrication, and experimental results for the PCB MEMS based tunable coplanar patch antenna are discussed.

2.1.1 Antenna Configuration

A Coplanar Patch Antenna (CPA) is based on the concept of a half-wavelength, open-ended coplanar waveguide (CPW) resonator. It consists of an open-ended CPW resonator section (along the y direction) fed by a CPW feed line as shown in Figure 2.1.

The characteristic parameters of the CPA are: length L, width W, and slot S. The field distributions in the slots of the half-wavelength resonator section (along y-direction) are out-of-phase and hence these slots behave as Non-Radiating Edges (NRE). On the other hand, the field distributions in the slots at the open-ends (along x-direction) are in-phase and therefore these slots are referred as Radiating Edges (RE). The CPA is fed by a 50 Ω CPW line connected to one of the radiating edges of the CPA.

An initial design for the CPA is obtained by choosing the length, L of the non-radiating edges to be $\lambda_g/2$ at the required operating frequency, where λ_g is the guide-wavelength of the CPW line that forms the resonator section. The antenna was designed on a 30-mil thick RT/Duroid 6002 substrate (ε_r = 2.94) with 1/4 ounce copper metallization. For a chosen operating frequency (f_r) of 4 GHz, the approximate length, L of the patch is calculated using $\varepsilon_{eff} \approx \varepsilon_r$ [10].

$$L = \frac{\lambda_g}{2} = \frac{c}{2 f_r \sqrt{\varepsilon_{eff}}} \approx \frac{c}{2 f_r \sqrt{\varepsilon_r}} = 21mm \tag{2.1}$$

The patch width W and slot S were chosen to be 30 mm and 2.2 mm, respectively. Using LineCalc (a transmission line calculator available in [24]), the dimensions of a 50Ω CPW feed line were calculated to be g = 0.1 mm and s = 1.642 mm. It should be pointed out that the designed CPA would resonate at a frequency slightly lower than 4 GHz due to fringing-field effect at the radiating edges. An effective length L_{eff} can be defined to account for the fringing fields at the radiating edges. The expected resonant frequency can be estimated using an approximate value for the effective length $L_{eff} \approx L + S$ and $\varepsilon_{eff} \approx \varepsilon_r$ as given below.

$$f_r = \frac{c}{2L_{eff}\sqrt{\varepsilon_{eff}}} \approx \frac{c}{2(L+S)\sqrt{\varepsilon_r}} \tag{2.2}$$

For a chosen slot dimension S = 2.2 mm, the expected resonant frequency of the designed CPA is calculated to be 3.8 GHz. For this design, the simulated return loss is 43dB at a resonant frequency of 3.526 GHz as shown in Figure 2.2. The simulated input impedance, Z_{in} is 50.73 + j0.21Ω which provides for good matching. A varactor diode MA46H200 has been mounted at top of the radiating edge of the antenna as shown in Figure 2.2. The photograph of the fabricated antenna along with the varactor diode is shown in Figure 2.3. The return loss of the antenna has been measured using an Agilent 8510C vector network analyzer. The return loss results of the antenna for various bias voltages in the range of 0 to 19.5 V applied to the varactor diode are shown in Figure 2.4. It can be seen that the operating frequency of the antenna is tunable from 4.92 GHz at 0 V with a return loss of 14 dB to 5.40 GHz at 19.5 V with a return loss of 56 dB. It should be pointed out that in the tunable frequency range of 5.16 to 5.40, the return loss is better than 32 dB. The radiation patterns were measured at the operating frequency of the antenna for various tunable states. Whereas the nominal shape of the pattern remains the same, there is a very slight tilt in the beam. This is due to the phase change across the structure due to the new operating frequency. As the resonance of the antenna changes from the design frequency, it will match less and less due to the fixed physical length of the antenna. In the following sections, MEMS varactor design and frequency tuning characteristics of the antenna are discussed.

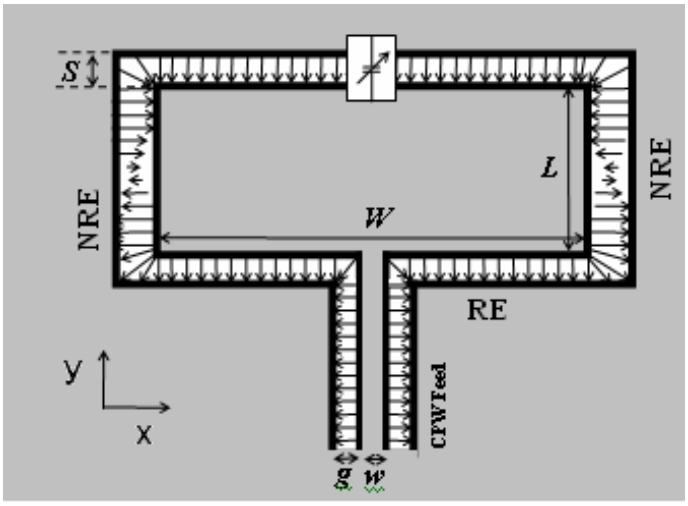

Figure 2.1. Coplanar patch antenna with CPW feed at the bottom Radiating Edge (RE) and varactor diode mounted at the top RE.

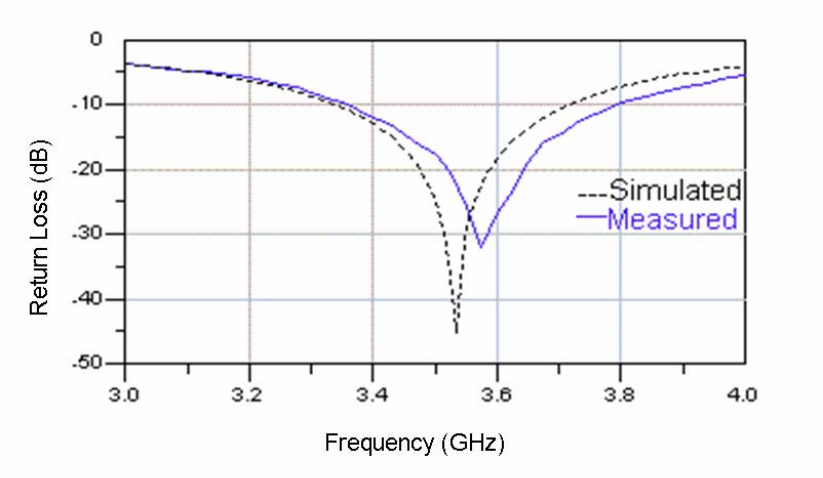

Figure 2.2. Simulated and measured return loss for the coplanar patch antenna without the varactor diode.

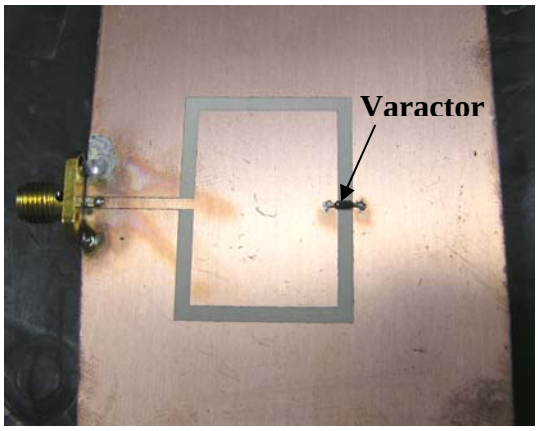

Figure 2.3. Photograph of the fabricated CPA with varactor diode mounted at the center of the top RE.

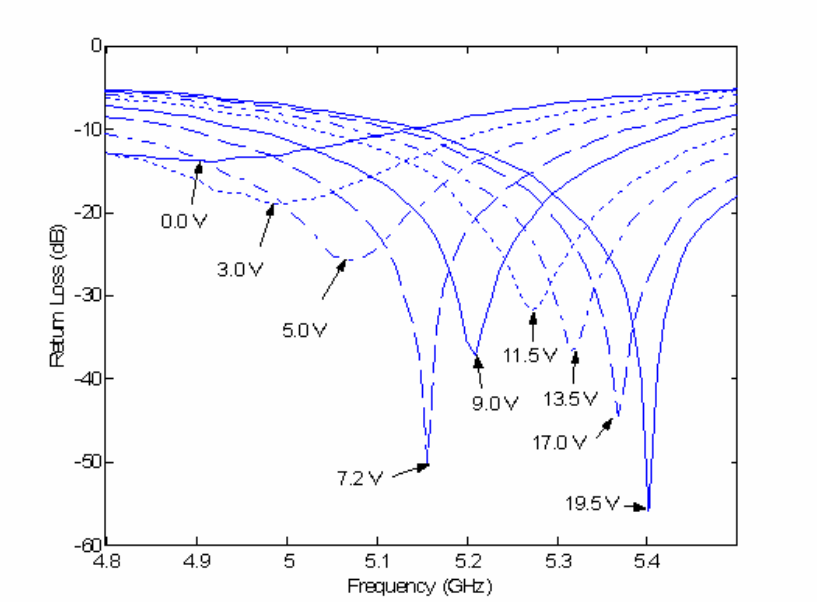

Figure 2.4. Measured return loss results of the CPA for various bias voltages applied to the varactor diode.

2.1.2 MEMS Varactor

A Tunable Coplanar Patch Antenna (TCPA) has been demonstrated in [10] by using a pin diode at one of the radiating edges. In this chapter, a MEMS based TCPA has been designed by integrating a MEMS varactor at one of the radiating edges as shown in Figure 2.5. Figure 2.6(a) illustrates the detailed cross sectional view of the MEMS varactor and Figure 2.6(b) shows the top view of the MEMS varactor on the antenna. An actuation pad is included in the antenna metallization layer to facilitate electrostatic actuation of the MEMS varactor. An air gap is present between the MEMS varactor membrane and the actuation pad on the antenna. The MEMS varactor is controlled by a DC bias voltage. As the DC bias is increased, the movable MEMS varactor membrane is pulled towards the actuation pad due to electrostatic force of attraction caused by the applied DC bias voltage. The deflection of the varactor membrane decreases the air gap

thereby increasing the capacitive load at the radiating edge of the CPA. The increase in the loading capacitance increases the effective length of the CPA and hence results in a downward shift in the resonant frequency of the CPA.

The close-up view of the MEMS varactor configuration on the antenna is shown in Figure 2.6(b). The dimensions of the suspension beams are L_A = 1.4 mm, L_B = 0.75 mm, L_C = 1.4 mm, L_D = 1 mm and the flexure width is 0.2 mm. From Figure 2.7, the capacitance of the MEMS varactor is given by

$$C_{MEMS}^{u,d} = \frac{C_1^{u,d} C_2^{u,d}}{C_1^{u,d} + C_2^{u,d}} \tag{2.3}$$

where C_1 is the capacitance between pad 1 and the MEMS electrode and C_2 is the capacitance between pad 2 and the MEMS electrode. Superscripts *u* and *d* represent the up and down states, respectively.

By ignoring the fringe effects, the MEMS varactor capacitance in the up and down states are given by

$$C_{MEMS}^{u,d} = \frac{\varepsilon_0 \varepsilon_{u,d}}{h_{u,d}} \left(\frac{A_1 A_2}{A_1 + A_2} \right) \tag{2.4}$$

where $A_1 = w_e l_1$ is the area of overlap between the MEMS electrode and pad 1, $A_2 = w_e l_2$ is area of overlap between the MEMS electrode and pad 2, ε_u (=1) is the relative dielectric constant of air, ε_d (=2.65) is the relative dielectric constant of the BCB dielectric layer, h_u is the air gap measured from the top surface of the dielectric to the MEMS electrode, and h_d is the dielectric thickness of the BCB layer.

The capacitance ratio between the down state capacitance, C_d, and the up state capacitance, C_u, can be written as

$$\varsigma = \frac{C^d_{MEMS}}{C^u_{MEMS}} \tag{2.5}$$

Using Eqn. (2.4) and Eqn. (2.5), the capacitance ratio can be expressed as

$$\text{i.e. } \varsigma = \frac{\varepsilon_d h_u}{h_d} \tag{2.6}$$

From Figure 2.6(a), the thickness of the spacer film is 2 mils (~ 50 μm). It can be noted that the sum of h_u + h_d + copper thickness (3 μm) should be equal to the spacer thickness. If the dielectric thickness h_d is chosen to be 7 μm, the air gap h_u can be calculated to be 40 μm. In this case, using Eqn. (2.6), the capacitance ratio can be calculated to be 15.

Using Eqn. (2.3), the MEMS varactor capacitance in the down state is given by

$$C^d_{MEMS} = \frac{C^d_1 C^d_2}{C^d_1 + C^d_2} \tag{2.7}$$

For design purposes, C^d_2 is assumed to be smaller than C^d_1. In this case, from Eqn. (2.4), the capacitance in the down state is given by

$$C^d_{MEMS} \approx \frac{\varepsilon_0 \varepsilon_d A_2}{h_d} \tag{2.8}$$

For a chosen MEMS electrode width w_e = 1 mm and overlap length l_2 = 0.45 mm, the capacitance C^d_{MEMS} can be calculated to be 1.5 pF. Using Eqn. (2.5), C_u can be estimated to be 100 fF.

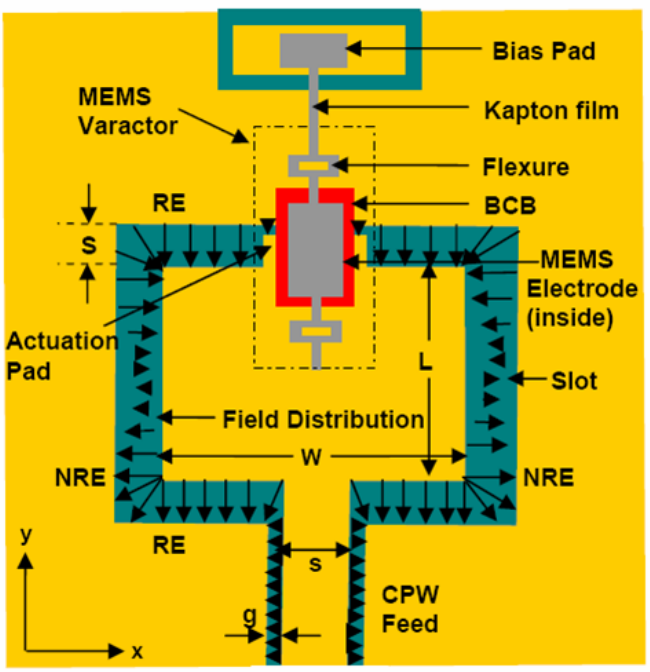

Figure 2.5. Coplanar patch antenna with CPW feed at the bottom radiating edge and a MEMS varactor mounted at the top radiating edge.

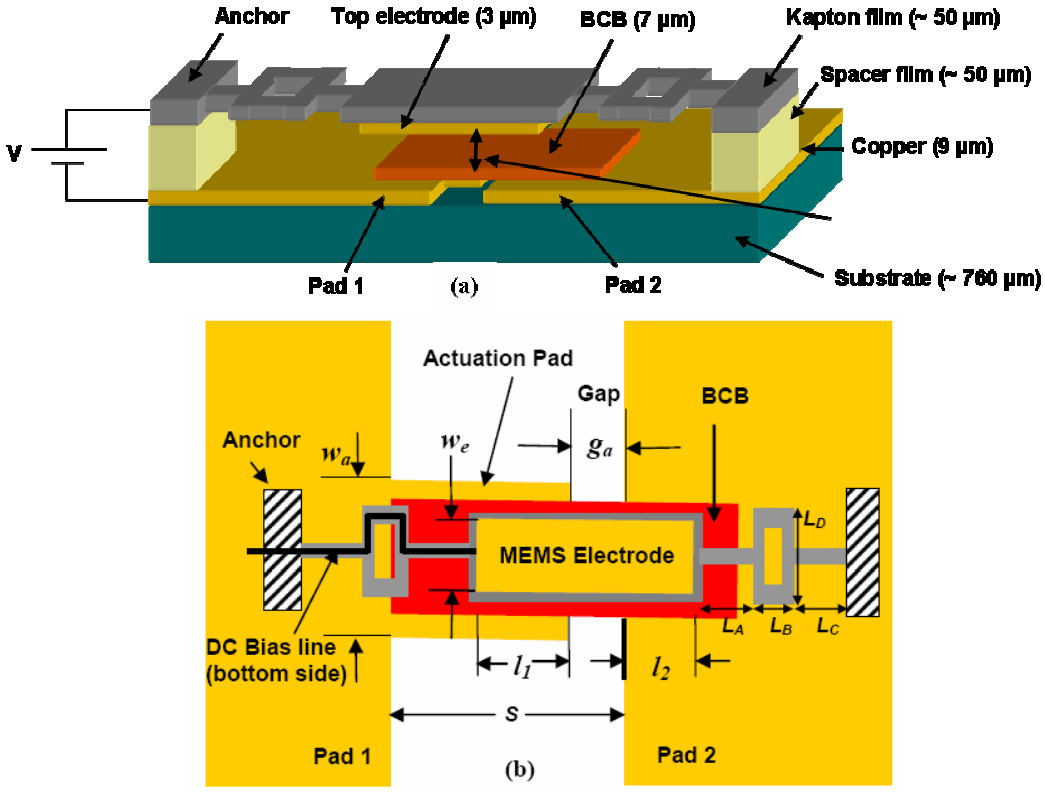

Figure 2.6. MEMS Varactor configuration on the antenna (a) Schematic view, and (b) Top view (Figure not to scale).

2.1.3 Equivalent Transmission Line Model

The equivalent transmission line model for the tunable CPA capacitively loaded by the MEMS varactor (along with the parasitic gap and open capacitances) is shown in Figure 2.7. It should be noted that this model ignores discontinuity reactances at the feed junction. From the model, the total capacitance can be expressed as

$$C_T^{u,d} = C_{MEMS}^{u,d} + C_{gap} + C_{open} \tag{2.9}$$

where C_{gap} is the capacitance between the actuation pad and pad 2, and C_{open} is the capacitance between pad 1 and pad 2. Superscripts u and d represent the up and down states, respectively.

The total capacitance loading the transmission line can be modeled as an equivalent open-circuited line section of length Δl. By equating the impedance of the capacitive load to an open circuited line section of length Δl, we obtain

$$Z_{OC} = \frac{-j}{\omega C_T} = -jZ_0 \cot(\beta \Delta l) \tag{2.10}$$

The equivalent line length extension Δl can be expressed as

$$\Delta l = \frac{1}{\beta} \cot^{-1}\left(\frac{1}{\omega C_T Z_0}\right) = \frac{c}{2\pi f \sqrt{\varepsilon_{eff}}} \cot^{-1}\left(\frac{1}{Z_0 2\pi f C_T}\right) \tag{2.11}$$

For a chosen slot width of S = 2.2 mm, the capacitance C_{gap}, was obtained using CoventorWare [25] for various gap widths (g_a) in the range of 0.1 mm to 2.1 mm. In order to generously account for any misalignment between the MEMS electrode and the actuation pad, the width of the actuation pad, w_a was chosen to be 2 mm. Figure 2.8 shows a plot of the variation of the gap capacitance, C_{gap} as a function of the gap width,

g_a. The gap value was chosen to be g_a = 0.1 mm so as to obtain a long actuation pad that would provide high actuation force and hence a reasonably low actuation voltage for PCB MEMS varactors. The corresponding C_{gap} is 2.04 fF. Using CoventorWare [25], C_{open} was estimated to be around 9 fF. Substituting these values into Eqn. (2.7), the total capacitances in the up and down states of the MEMS varactor are calculated to be 111 fF and 1.5 pF, respectively. Using the afore mentioned design parameters, an antenna model including an actuation pad but without a MEMS varactor was built in Agilent ADS [24] and Electromagnetic (EM) simulation was carried out. The simulated return loss of the antenna is shown in Figure 2.9. From Figure 2.9, it can be seen that the antenna resonates at 5.583 GHz with a return loss better than 45 dB. Also, using the *LineCalc* tool (*a transmission line calculator*) in Agilent ADS [24] for the antenna parameters yielded Z_0 = 66.26 Ω and ε_{eff} = 1.198. After substituting all these values in (2.11), the equivalent line length extension (Δl), in the up and down states are calculated to be 2.1 mm and 10 mm, respectively.

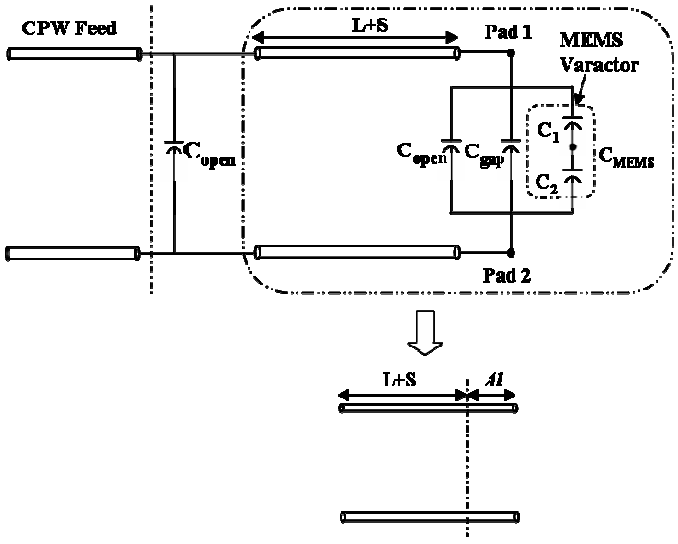

Figure 2.7. Transmission line model for the tunable CPA with the MEMS varactor.

2.1.4 Frequency Tuning Characteristics

The effective length of the transmission line, L_{eff} can be expressed as $L_{eff} = L + S + \Delta l$ where Δl is the equivalent line length extension that accounts for the capacitive loading. The resonant frequency of the antenna can be expressed as a function of the effective length, L_{eff} as

$$f = \frac{c}{2L_{eff}\sqrt{\varepsilon_{eff}}} \tag{2.12}$$

Assuming ε_{eff} remains constant; the ratio of the antenna resonant frequencies in the down and up states of the MEMS varactor can be obtained from Eqn. (2.12) as

$$\frac{f_d}{f_u} = \frac{L + S + \Delta l_u}{L + S + \Delta l_d} \tag{2.13}$$

The frequency ratio (*FR*) is defined as the ratio of the change in the antenna resonant frequency to the up state resonant frequency.

$$FR = \frac{f_u - f_d}{f_u} \tag{2.14}$$

Using these design parameters, a MEMS varactor model was created and included on top of the rectangular patch antenna for EM simulation in Agilent ADS [24]. The return losses of the antenna for the up and down states are shown in Figure 2.9. We can observe that as the air gap between the MEMS varactor membrane and the substrate decreases, the capacitance increases and hence the resonant frequency decreases. This antenna design is expected to be tunable in the frequency range from 4.94 GHz (down state) to 5.44 GHz (up state). The return loss values are 28.85 dB and 44.67 dB at 4.94 GHz and 5.44 GHz, respectively. From the simulated results, the frequency ratio was calculated to

be 0.09. The radiation patterns shown in Figure 2.10 were simulated in Ansoft HFSS [26]. In the following sections, fabrication and experimental characterization of this antenna design are discussed.

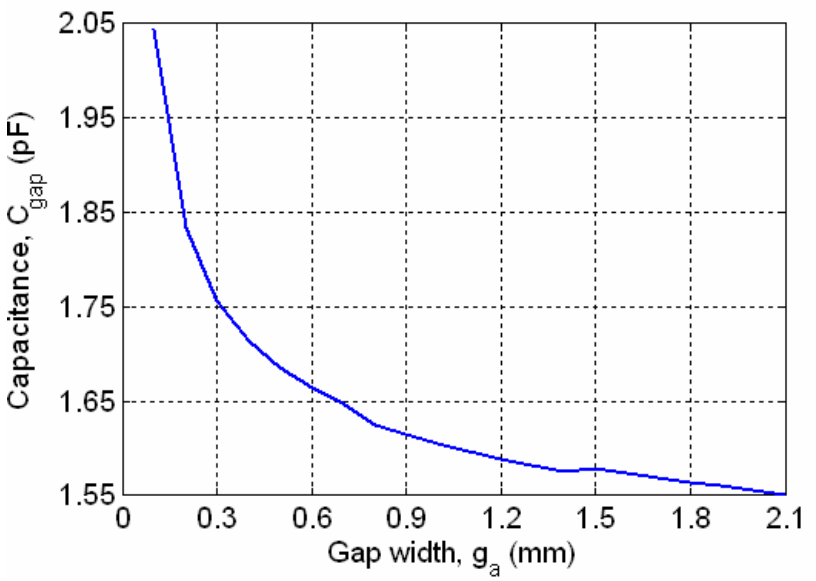

Figure 2.8. Simulated gap capacitance (C_{gap}) between the actuation pad (pad 1) and the ground plane (pad 2) for various gap widths (g_a).

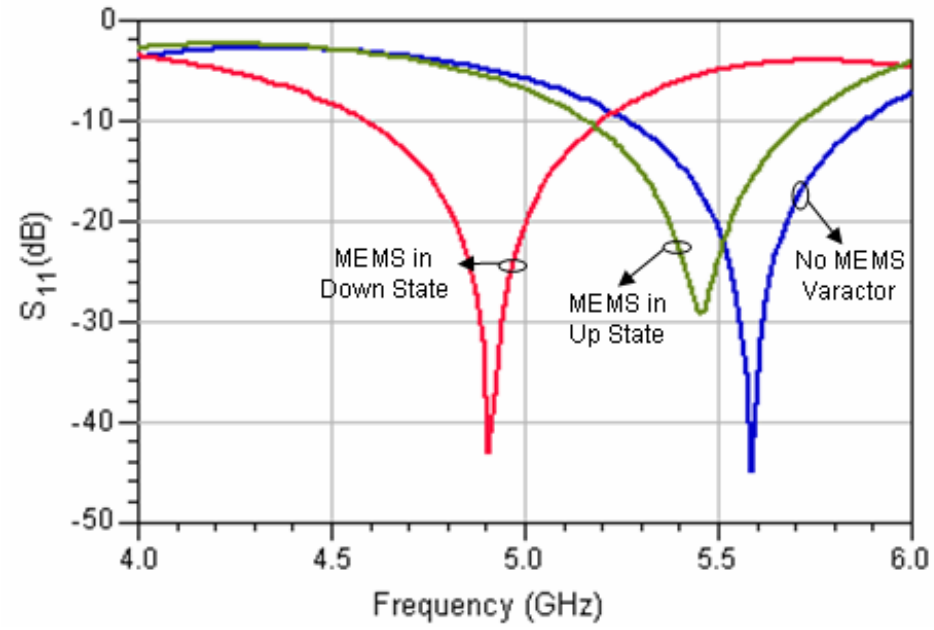

Figure 2.9. Simulated return loss of the coplanar patch antenna without and with the MEMS varactor (up and down states).

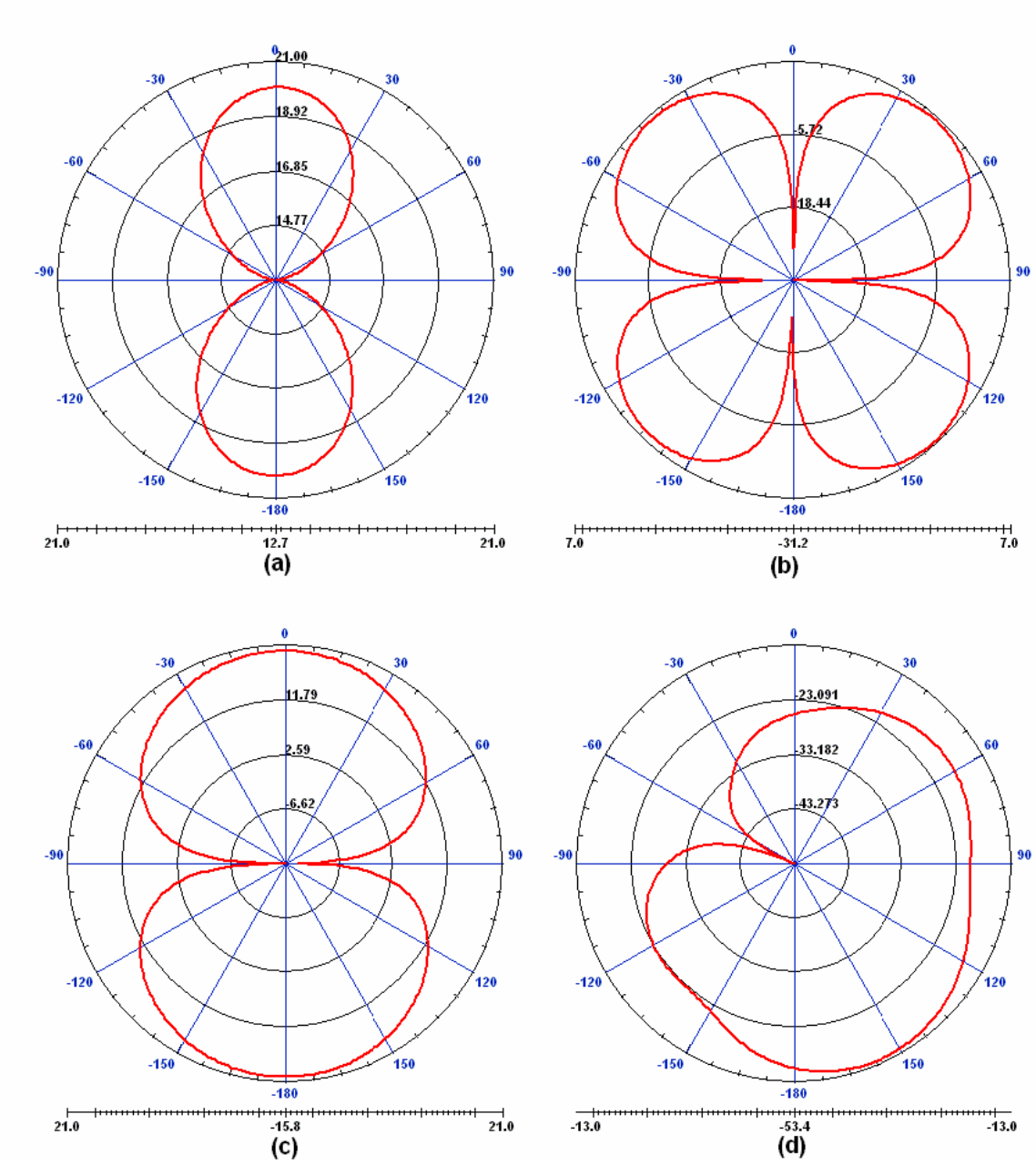

Figure 2.10. Measured radiation patterns of the MEMS tunable antenna for various applied voltages: (a) H-plane Co-polarization, (b) H-plane Cross-polarization, (c) E-plane Co-polarization, and (d) E-plane Cross-polarization.

2.2 Fabrication and Assembly

The three layers that make up the configuration of the tunable coplanar patch antenna are: substrate, spacer, and a polyimide film.

2.2.1 Substrate

A 2" x 2" RT/Duroid 6002 (30 mils thick with 9 μm copper cladding, $\varepsilon_r = 2.94$) substrate was used. Coplanar Waveguide (CPW) lines are defined on the metallization layer on the substrate by photolithography and etching processes. Photosensitive BenzoCycloButene (BCB) is spin-coated on the substrate and patterned to form the dielectric layer on the bottom electrode metallization. Figure 2.11(a) shows a photograph of the substrate with the patterned antenna, CPW line, and BCB dielectric layer.

2.2.2 Spacer

The spacer layer provides the required spacing between the substrate and the polyimide layer. Hence, the thickness of the spacer film determines the up-position gap height. A 2 mil thick polyflon bonding film is used as the spacer film. This film is machined using a milling machine to create openings for the contact pads and the MEMS varactor in the polyimide film. A milling machine processed spacer film is shown in Figure 2.11(b).

2.2.3 Polyimide film

A 2 mil thick flexible Kapton E polyimide film ($\varepsilon_r = 3.1$) with 100 Å -150 Å nichrome seed layer and 3 micron thick copper cladding is used. The Kapton film is used as the MEMS structural layer because of its ability to withstand millions of mechanical

flexing cycles. First, the electrode is defined on the 3 micron thick copper cladding on the Kapton film by photolithography and etching processes. Then, the film is machined using Deep Reactive Ion Etching (DRIE) to create slot openings required for the formation of a movable membrane. These flexures separate the membrane from its adjacent area and thus reduce the stiffness of the movable membrane. The equipment used for the DRIE process is an STS AOE (Advanced oxide etcher). The configuration of the gases used for this etch in our facility is 8 sccm CF4 and 35 sccm oxygen with 500 Watts of RF power. These processing parameters take about 70 minutes to etch a 2 mil thick Kapton film. Finally, resistive bias lines are defined in the nichrome seed layer for DC biasing of the MEMS varactor. These bias lines prevent leakage of the RF signal from the MEMS varactor to the DC supply. Figure 2.11(c) shows the photograph of a processed Kapton film.

2.2.4 Thermo-Compression Bonding

Thermo-compression bonding is performed using a Carver Press consisting of two platens. The platens are heated using heaters, which are controlled by a thermocouple. The fixture consists of two steel plates with alignment holes at four corners. The substrate forms the bottom most layer, the spacer is the middle layer and the Kapton film forms the top most layer in this structure. The different layers are aligned by aligning the marks created on the three layers during the fabrication process described earlier. This unit is now placed between the press platens. The bonding is performed at a pressure of 65 psi (a load of 165 lbs.) and a temperature of 130°C. Both pressure and temperature are maintained for 5 min during bonding. Before pressure is released, the assembly is cooled

down to the room temperature. A detailed traveler of the fabrication process is provided in Appendix A.

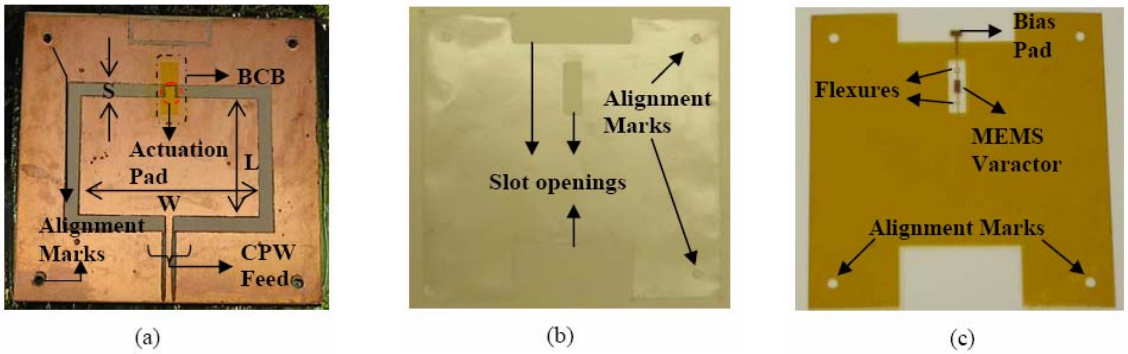

Figure 2.11. Three layers of the MEMS tunable CPA (a) Substrate layer coated with BCB, (b) Milled polyflon bonding film, and (c) Kapton film layer after DRIE.

2.3 Experimental Characterization

A photograph of the fabricated tunable coplanar patch antenna is shown in Figure 2.12. Figure 2.13 shows the biasing arrangement for the MEMS based tunable coplanar patch antenna. A bias-T (Picosecond Model No. 5542-203) with a maximum DC bias voltage rating of 100 V was used. The bias-T ensures that the applied DC voltage does not leak into the RF input thereby providing proper isolation between the RF test equipment and the DC power supply. An SMA launcher was soldered to the CPW feed line for RF testing. To ensure rigidity of the MEMS devices during testing, the substrate was mounted on a Lucite frame. Two types of measurements were taken to characterize the antenna: MEMS varactor profile and RF measurements.

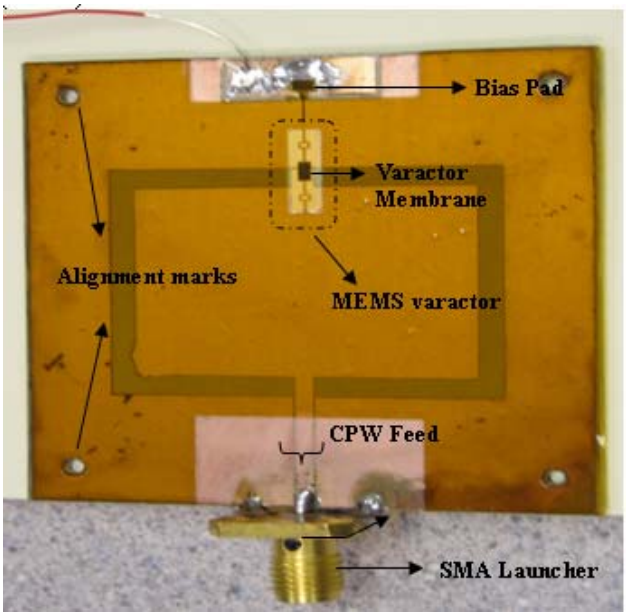

Figure 2.12. Photograph of the fabricated MEMS tunable coplanar patch antenna.

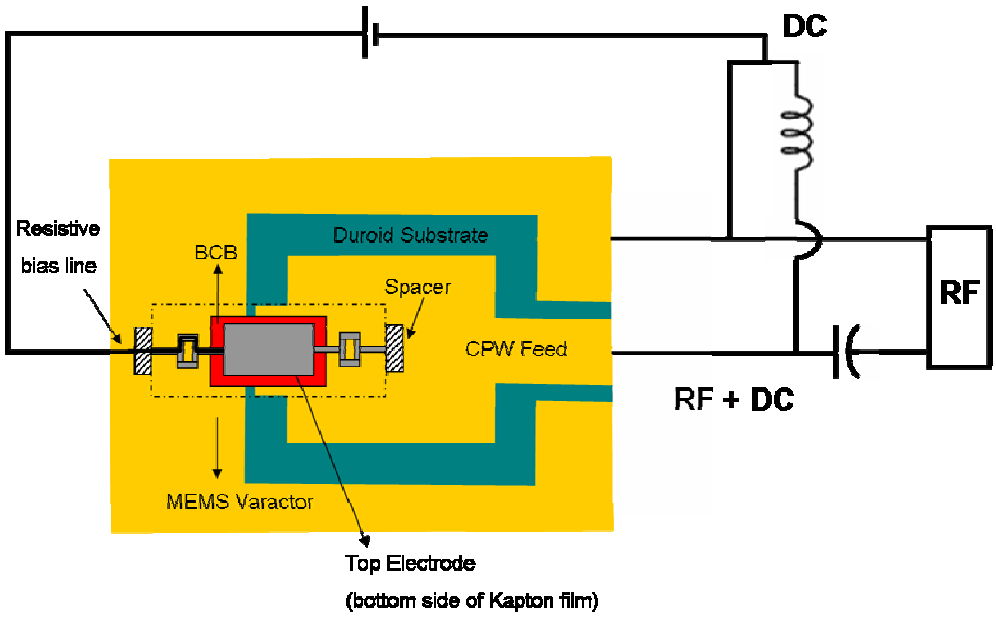

Figure 2.13. Biasing arrangement used for RF testing of the tunable CPA.

2.3.1 MEMS Profile Characterization

The WYKO optical profilometer was used to measure the profile of the MEMS varactor in the CPA and the measured profile is shown in Figure 2.14. The procedure to

use this equipment is provided in Appendix B. Profile measurements of the initial design yielded the height of the MEMS varactor above the ground plane when measured at the center of the MEMS varactor to be about 100 microns and the variation of the height from the edge to the center to be around 50 microns. In order to reduce this warpage, during lamination of the final design, spare Kapton pieces were placed in the air gap between the BCB on the bottom electrode (plate 1 and plate 2) and the Kapton membrane. This helped in bringing down the warpage to about 5 to 10 microns across the MEMS varactor plate. The slight warpage could be attributed to the thermal coefficient of expansion mismatch between the copper patch (17 ppm) and Kapton (16 ppm) polyimide film.

2.3.2 RF Measurements

The return loss of the MEMS patch antenna was measured using an HP 8510C Vector Network Analyzer (VNA). A DC bias voltage was applied to the patch and return loss measurements were taken for a various bias voltages in the range of 0 to 116 V, at 5 or 10 V increments. Figure 2.15 shows the plot of the return loss measurements for various applied voltages. It can be observed that the resonant frequency of the antenna shifts downward with increasing bias voltage. At 0 V, the MEMS varactor is in the "up" state and the antenna resonates at 5.545 GHz with a return loss of 40 dB. When the applied voltage is below 80 V, no significant frequency shift was observed. The antenna provides a downward shift in the resonant frequency as the applied DC bias is increased to 110 V. When the DC bias voltage is increased to 116 V, the MEMS varactor reaches the "down" state and the antenna resonates at 5.185 GHz with a return loss of 41.12 dB.

The tunable frequency range of the antenna between the up and down states of the MEMS varactor is 360 MHz. The measured frequency ratio is 0.065.

The radiation patterns of the antenna have been measured using a Diamond Engineering 6000 Series Desktop Antenna Measurement system (DAMS) (available from Diamond Engineering [27]). Measured radiation patterns for various bias voltages of 0, 110, 113, 115 and 116 V are shown in Figure 2.16. The null along the broad-side direction in the E-field co-polarization patterns can be attributed to the asymmetry caused by the presence of the MEMS varactor and the feed line at the center of the radiating edges. It can be noted that there is no significant change in the overall patterns throughout the tuning range for various applied voltages.

Table 2.I shows the comparison of the simulated and measured resonant frequencies in the up and down states. The simulated results were obtained by EM simulation of the CPA (including the MEMS varactor) in the HP-Momentum available in the Agilent's Advanced Design System (ADS) [24]. In the up state, the real part of the input impedance obtained from the simulated and measured return losses are 47.51 Ω and 49.53 Ω, respectively. Hence the antenna exhibits a better impedance match to the 50 Ω feed line in the measured case when compared to the simulated case. From Table 2.I, it can be noted that the simulated tuning range is about 9 % whereas the measured tuning range is about 6.5 % [28]. The lower measured tuning range can be attributed to a slight decrease in the down state capacitance caused by factors like the surface roughness of the RT/Duroid substrate and fabrication tolerances. Typical surface roughness for RT/Duroid

substrate is in the range of 1-2 μm. A similar trend was observed in [29] for RF MEMS switches fabricated on RT/Duroid substrates.

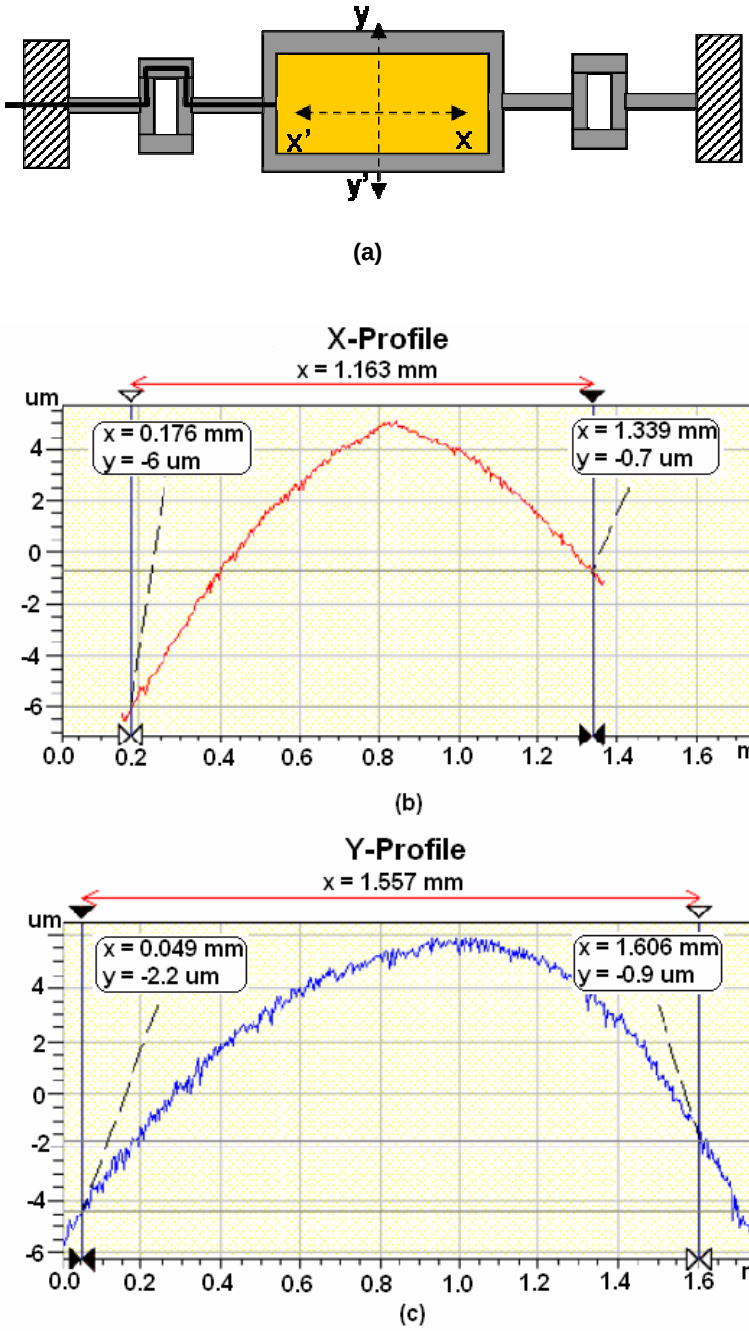

Figure 2.14. 2D profile of the MEMS varactor in the CPA measured using WYKO NT 2000 optical profiler (a) top view of the MEMS varactor membrane showing xx' and yy' reference planes, (b) xx' profile of the MEMS varactor membrane, and (c) yy' profile of the MEMS varactor membrane.

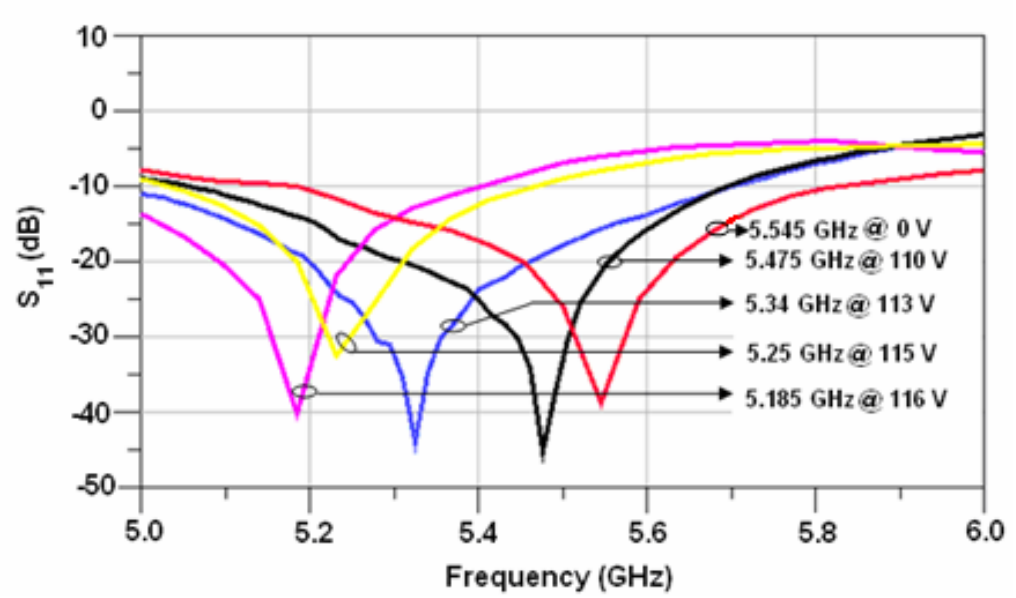

Figure 2.15. Return loss results of the tunable MEMS antenna for various applied DC bias voltages.

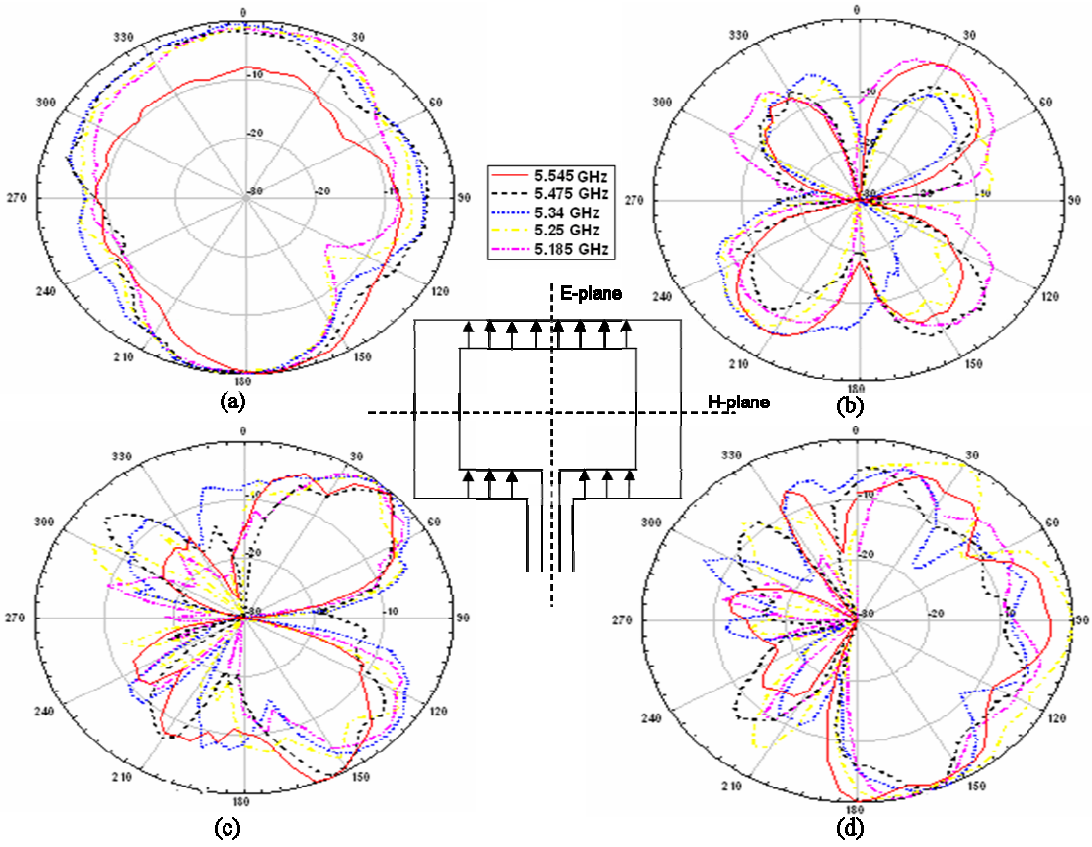

Figure 2.16. Measured radiation patterns of the MEMS tunable antenna for various applied voltages: (a) H-plane Co-polarization, (b) H-plane Cross-polarization, (c) E-plane Co-polarization, and (d) E-plane Cross-polarization.

Table 2.I: Simulated and measured resonant frequencies and return losses for the antenna in the up and down states of the MEMS varactor

	Simulated			Measured		
	Frequency (GHz)	S_{11} (dB)	Z_{in} (Ω)	Frequency (GHz)	S_{11} (dB)	Z_{in} (Ω)
Up State	5.44	-28.85	47.51-2.486i	5.545	-40	49.53-1.045i
Down State	4.94	-45	49.97-0.583i	5.185	-41	50.43-0.88i

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CHAPTER III: ORGANIC FIELD EFFECT TRANSISTORS

The last three decades have seen an explosive growth in silicon-based microelectronics. The rapid growth in mass-scale manufacturing has been possible due to reduction of dimensions of the transistors, reduction of the power consumption, and yet maintaining a high degree of reliability. Though the cost of setting up new manufacturing plants has steadily increased over the years, the cost per transistor for logic, memory, application specific circuits, and other related applications has been decreasing for every generation of semiconductor products [30]. Thus, the continuous progress in the design, process and testing has made it possible to achieve higher performance, yields, and reliability; making the semiconductor industry one of the important drivers of economical growth. In search of flexible and low-cost substrates, organic semi-conductor-based integrated circuits (ICs) have been suggested as an alternate to silicon ICs [31]. The discovery that the electrical conductivity of some polymers can be increased from insulator to semiconductor range or metallic range by doping has been a driving force for research in this area [32],[33]. Over the last two decades, there has been a tremendous interest in the electrically conducting polymers [34],[35],[36]. The main processing techniques employed in the deposition of polymer films on glass or silicon substrates are electro-polymerization, solution-processed deposition by casting, and vacuum evaporation [37],[38]. These techniques are relatively less complicated and cheaper

compared to the techniques used in the traditional semiconductor industry [39],[40],[41]. Ebisawa et al. fabricated the first polymer-based transistor in 1983 [42]. Since then, a great deal of research work has been done in the area of organic material-based transistors. The driving force for developing organic field effect transistor (OFET) or organic thin-film transistor (OTFT)-based electronics is the fact that they are flexible, light weight and have the prospect of low-cost manufacturing. Major barriers in the practical realization of OTFT-based electronic systems are the need for larger power supplies, lower gain, lower switching speeds and reliability problems. New directions leading to changes in the design of transistors, materials used in the fabrication, and processing techniques are warranted for developing processes and equipment that can lead to the manufacturing of OTFT-based electronics. OTFTs are being investigated in this chapter to lay the ground work for future utilization of OTFTs to control Polymer MEMS actuators like the ones discussed in the earlier chapters. They are currently controlled manually. Silicon based transistors do not have the capability to withstand the high actuation voltages.

3.1 Choosing a semi-conductor Polymer

Large varieties of organic compounds have been tested for making OFETs and there are many new materials being synthesized for this purpose. Currently, most organic materials used in OFETs are π-conjugated organic oligomers and polymer-based organic semiconductors. Conjugated polymers present the advantage of being amenable to specific deposition techniques that have been developed for conventional polymers. Their

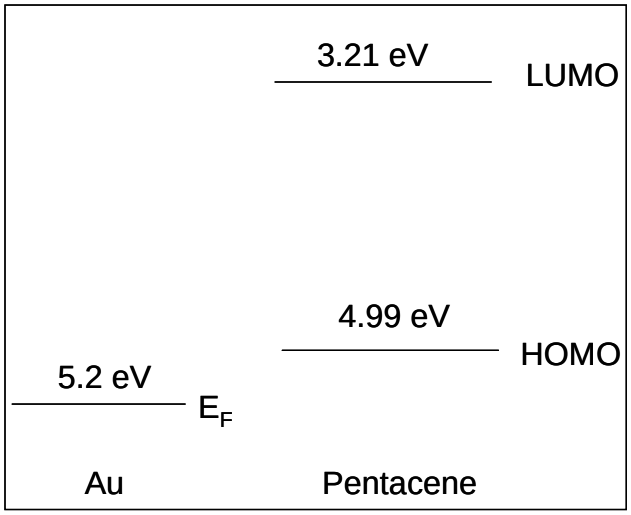
main drawback is that their performance is still lower than that of small-moleculed organic oligomers.

Depending on the type of charge carriers, the organic semiconductors can be classified as p-type and n-type. In p-type semiconductors, the majority carriers are holes, while in n-type semiconductors, the majority carriers are electrons. Both type materials have been used in OFETs. N-type materials are mainly characterized by their high electron affinity and p-type materials, by their low ionization potential. In most applications, the investigated organic semiconductor materials are p-type. Because of their sensitivity to air and moisture, most n-type semiconductors are not suitable for OFETs. Also, n-type materials have relatively low field effect mobilities. Recently, Chua has discussed n-type materials in Nature [45]. Commonly used organic semiconductors include Phthalocyanine (PC) [46],[47], Pentacene [48], α-Sexithiophene [49], poly(3-hexylthiophene), 3,4,9,10-Perylenetetracarboxylic dianhydride (PTCDA) [50], Hexadecahalo-genated metallophthalocyanines (F_{16}CuPc) [51], etc.

At present, almost all devices are made of small molecule semiconductors, especially Pentacene, Oligothiophenes, and their derivatives. These two materials possess the best electronic characteristics by offering high charge carrier mobilities, the mobilities can reach 6 cm^2/V-s for Pentacene [48] and 1 cm^2/V-s for α-Sexithiophene [49].

Pentacene is an aromatic compound with five condensed benzene rings and has been widely studied for its application in OFETs. Due to the poor solubility of Pentacene, it is mainly used in its polycrystalline thin film form and deposited by vacuum evaporation. The characteristics of Pentacene have been described in many reviews [52],[53],[54].

Molecules have similar energy band levels as atoms. The valance band energy level of an atom is analogous to the energy level of Highest Occupied Molecular Orbital (HOMO). Similarly, the conduction band energy level of an atom is analogous to the energy level of Lowest Unoccupied Molecular Orbital (LUMO). The LUMO and HOMO energy levels are in the vicinity of 3.21 eV and 4.99 eV respectively as shown in Figure 3.1 [55]. The Fermi level of gold is 5.2 eV. Hence, it can be seen that the HOMO energy level of Pentacene and the Fermi level of Pentacene are in good agreement. So, it can be inferred that when sufficient reverse bias is provided at the Gold-Pentacene interface, there will be a current flow due to the holes in the valence band.



HOMO: Highest Occupied Molecular orbital ~ E_V

LUMO: Lowest Unoccupied Molecular orbital ~ E_C

Figure 3.1. Energy level comparison of Gold and Pentacene.

3.2 Different Configurations

Three different configurations (shown in Figure 3.2) used for designing an OFET are discussed below.

(i) **Top contact configuration:** Here, the gate electrode is defined first and then surrounded by the gate dielectric. The semiconductor polymer is then deposited/coated followed by the source and drain contacts as the top-most layer.

(ii) **Bottom contact configuration:** This formation varies from the above one in that the upper two layers are interchanged.

(iii) **Co-planar configuration:** In this configuration, the gate, source and drain are defined in the same layer. The gate dielectric isolates the gate while the semiconductor polymer forms the top-most layer.

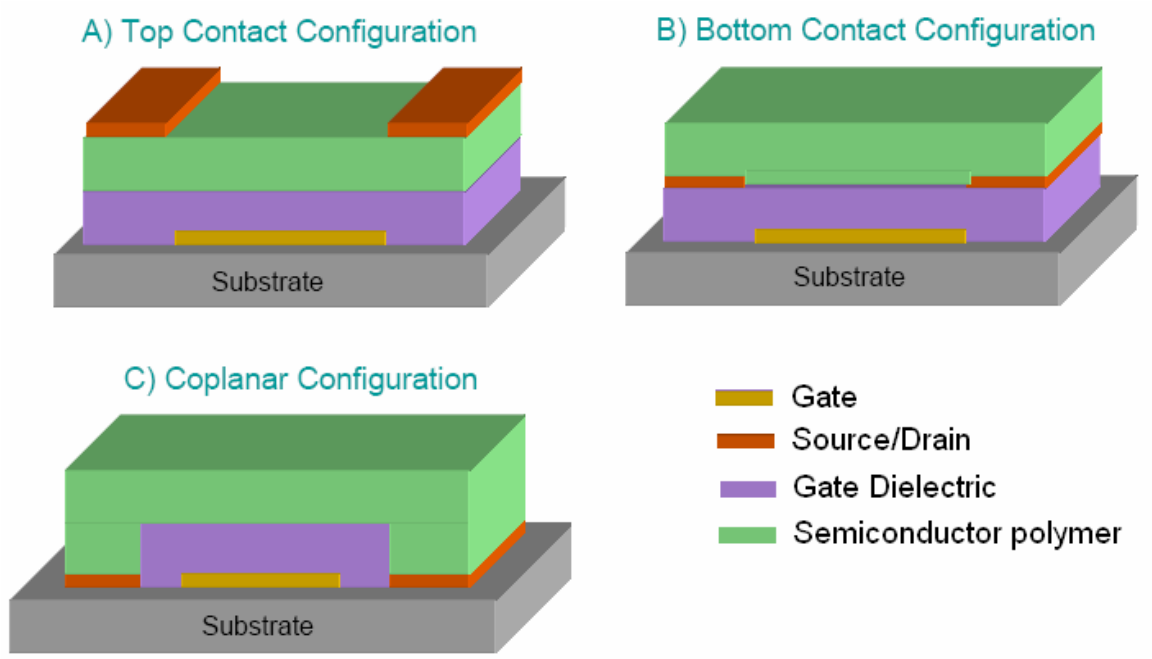


Figure 3.2. Three different configurations used for the OFET.

In this experiment, the organic gate dielectric used is BenzoCycloButene (BCB). Table 3.I shows the various parameters chosen for this design. Masks were made with the channel widths ranging from 25-100 μm and channel lengths from 100-200 um for a coplanar configuration.

Table 3.I: Organic thin film transistor parameters

Layers	Material	Thickness
Source, Drain and Gate Electrodes	Gold ($\sigma = 4.1 \times 10^7$ S/m)	~100 nm
Gate Dielectric	BCB ($\varepsilon_i = 2.65$)	~500 nm
Semiconductor Polymer	Pentacene (μ_s = 0.8e-4 cm^2.V/S)	~700 nm

3.3 Fabrication

Gold electrodes are deposited on a plain oxidized silicon wafer through Chemical Vapor Deposition (CVD) and photolithography techniques. BCB is then spin-coated and patterned on top of the gate. In order to obtain a thin BCB coating of 500 nm, 1 part of BCB was diluted using 1 part of T1100 solvent and the mixture was spin-coated at 2700 rpm. The final step is to deposit Pentacene through thermal evaporation. The electrode pads are covered before Pentacene can be deposited so that they are available for probe testing. Figure 3.3 shows the different steps involved in the fabrication process.

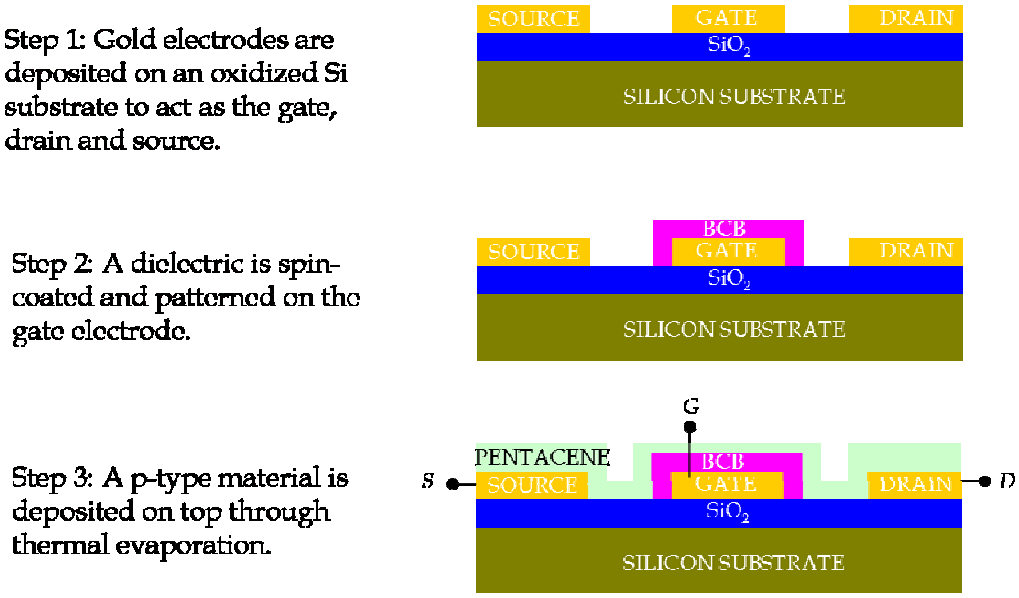


Figure 3.3. Fabrication process of the preliminary design for the Coplanar OFET.

3.4 Testing and modifications

When this device was tested by varying the output and input voltages while measuring the output current, it was observed that the gate voltage did not have any significant impact on the device performance. It was suspected that the field effect generated by this device might not be sufficient to function as an FET. In order to confirm this suspicion, the device was modified so that the silicon on the wafer now acted as the gate while the silicon oxide layer acted as the gate dielectric. This configuration is shown in Figure 3.4. Figure 3.5 and Figure 3.6 show the electrical characteristics of the above modified OFET. It can be observed that the device performance resembled that of a FET. From these experiments, it was gathered that the masks needed to be modified to allow for a wider gate and that the bottom contact configuration would be better suited in order for the field effect to take place. Hence a new configuration was developed while maintaining Pentacene as the top layer in order to prevent any interaction with other chemicals. Figure 3.7 shows the different fabrication steps involved. Detailed travelers for the fabrication of the transistor in the coplanar and bottom contact configurations are provided in Appendix C and Appendix D respectively.

The devices were fabricated through photolithography, CVD and thermal evaporation techniques and the experiment was repeated. Figure 3.8 shows the photograph of a device with width, W = 1000 μm and length, L = 50 μm. The fabricated OFET was characterized using an HP 4156A semiconductor parametric analyzer. Figure 3.9 shows a plot of the output characteristics of the aforementioned device while Figure 3.10 shows the transfer characteristics [56]. It can be seen from these characteristics that this device behaves like

a p-type FET albeit with a lower drain current which causes a drop in the mobility. It is also shown that the device can handle high voltages of ~70 V.

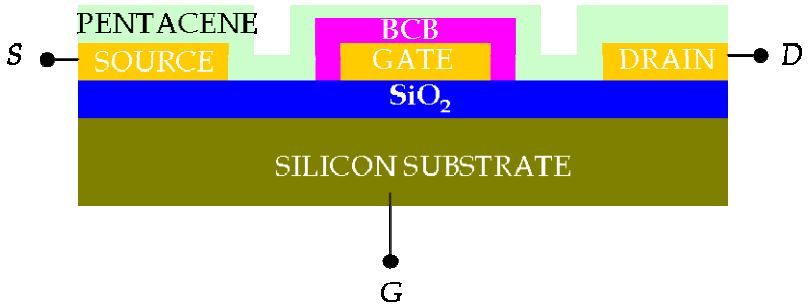


Figure 3.4. Crosssectional view of the modified design for the OFET.

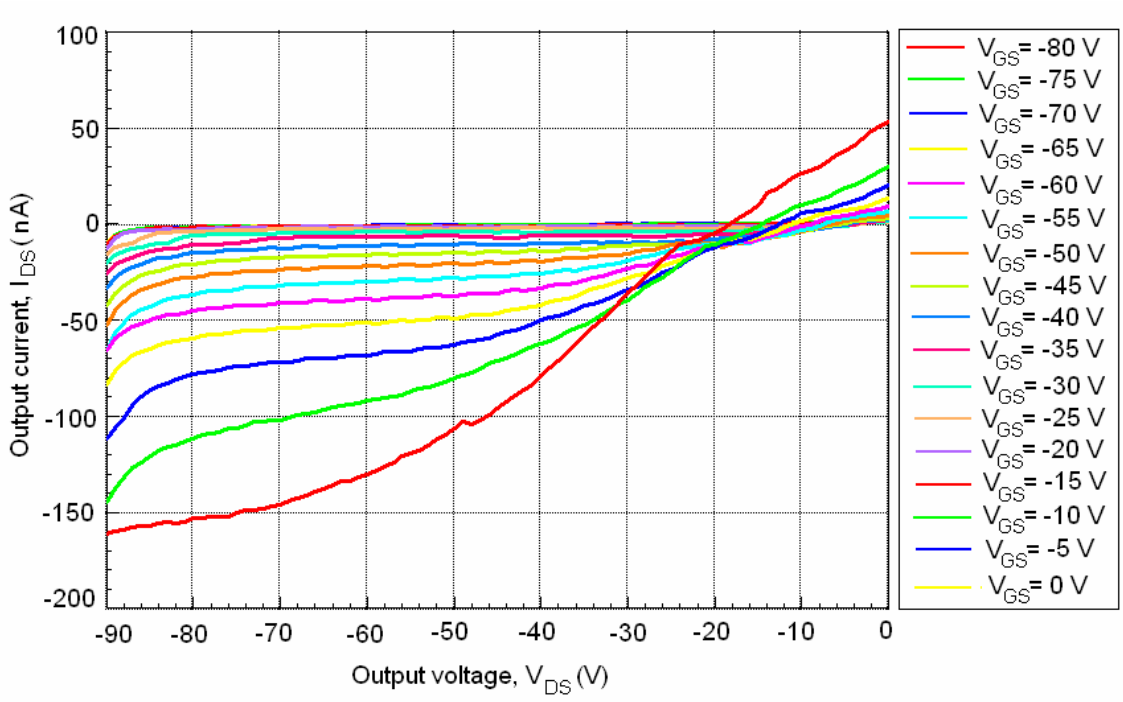


Figure 3.5. Output characteristics of the modified design for the OFET.

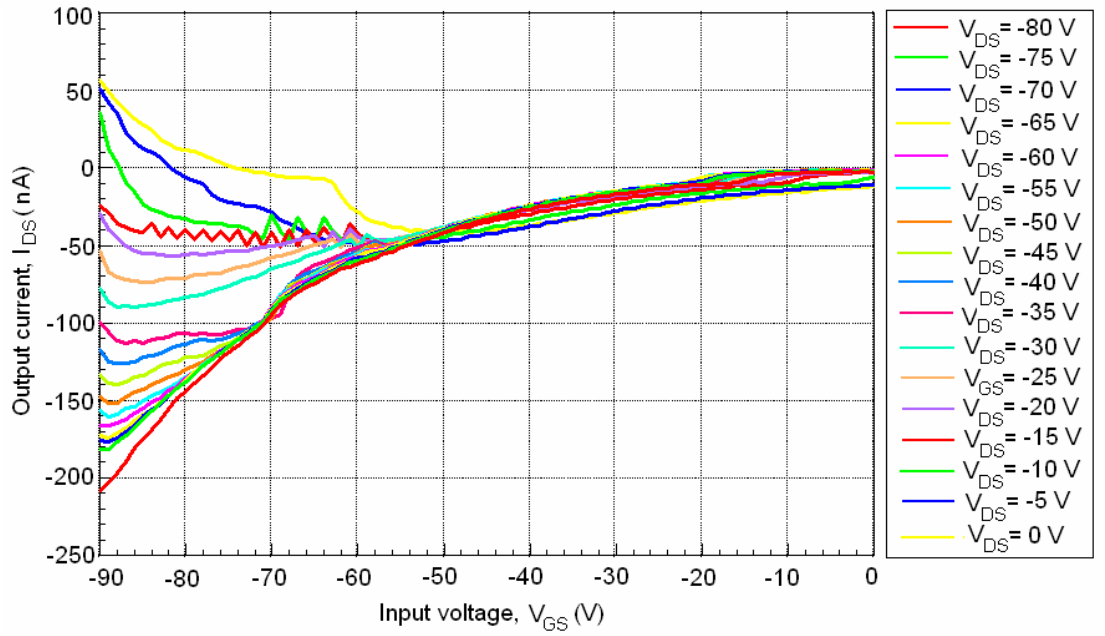


Figure 3.6. Transfer characteristics of the modified design for the OFET.

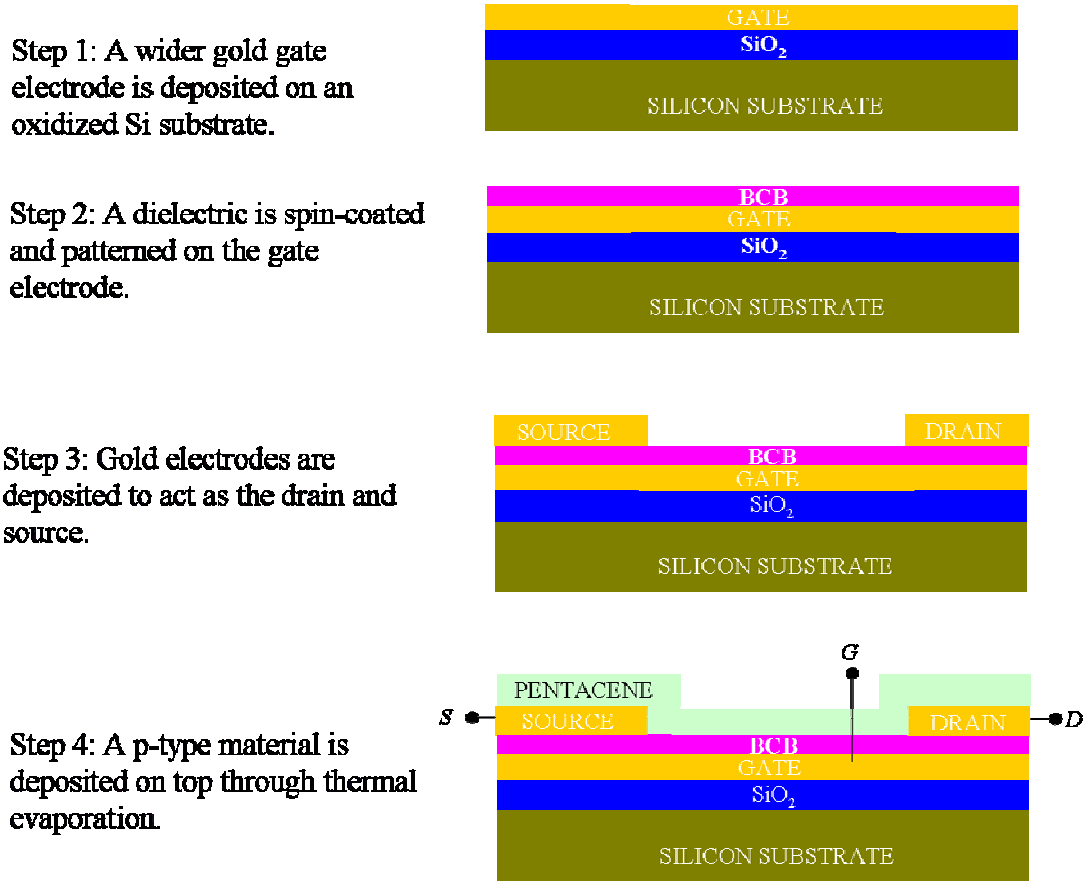


Figure 3.7. Fabrication process of the finalized design for the OFET.

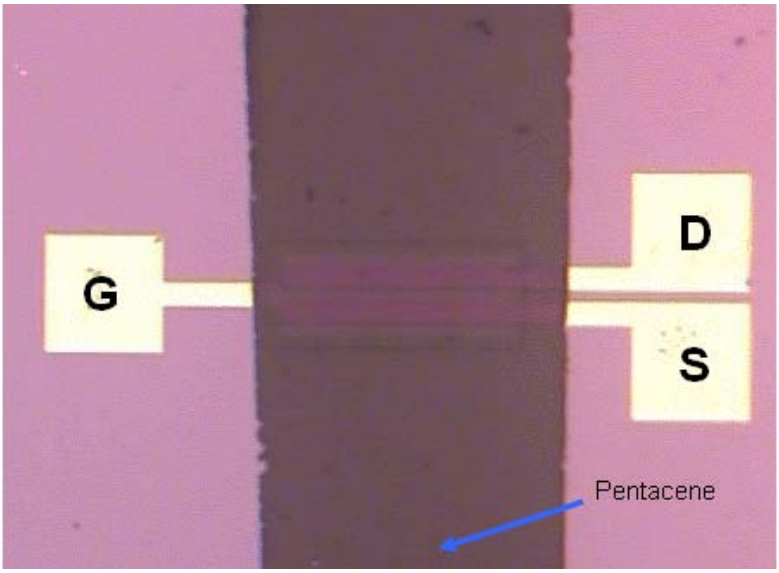


Figure 3.8. A photograph of a 1000 μm (*W*) X 50 μm (*L*) OFET.

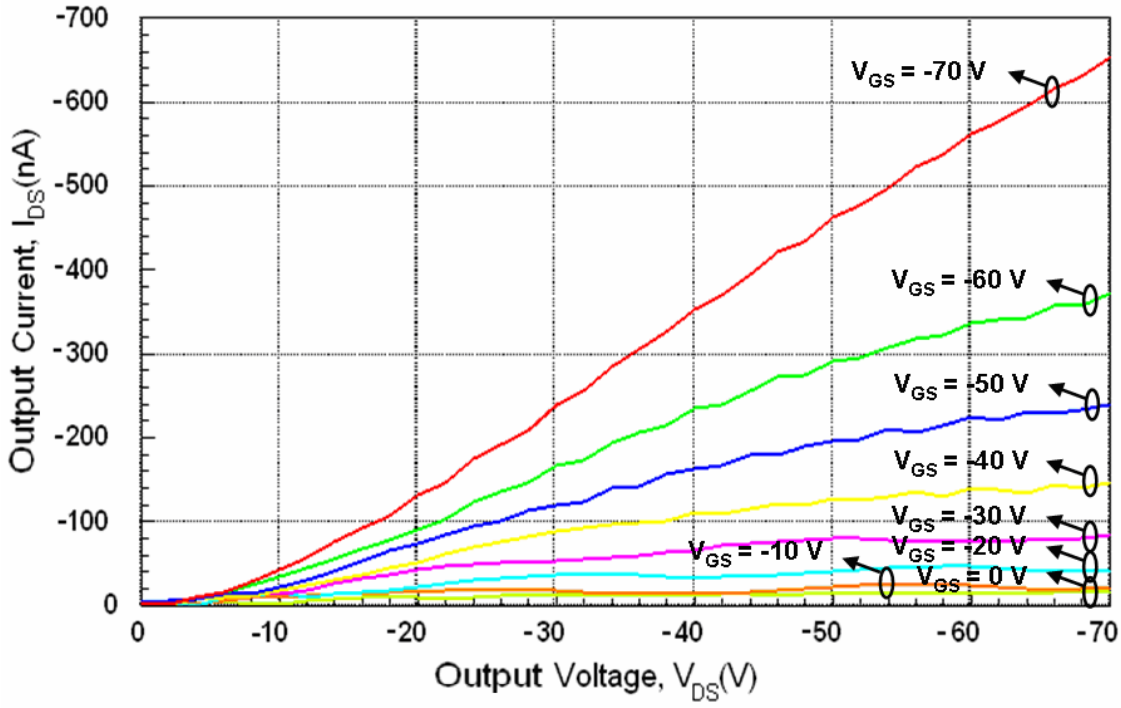


Figure 3.9. Output Characteristics of the OFET.

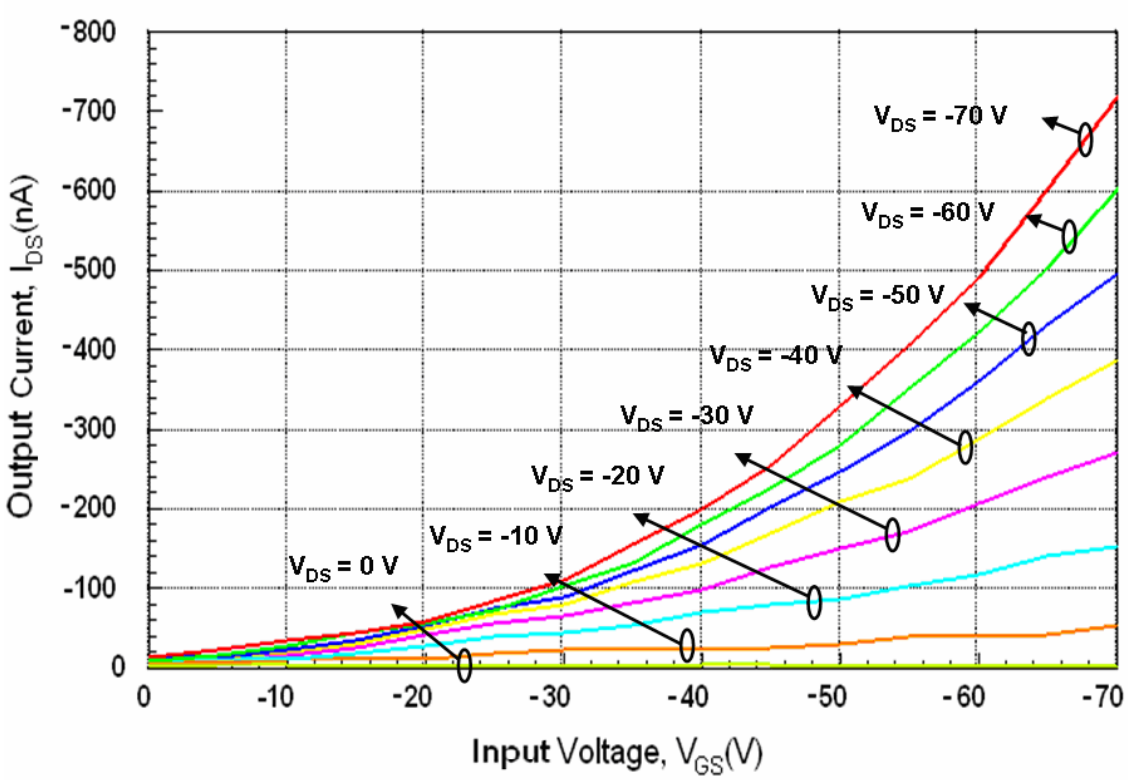


Figure 3.10. Transfer Characteristics of the OFET.

In conclusion, this chapter presents the design, fabrication and measured characteristics of an organic transistor. The highlight of this work is the use of a thin BCB layer (500 nm) as the gate dielectric for Pentacene based organic transistors. The mobility of the transistor is not as high, but it can handle higher voltages than a silicon transistor.

CHAPTER IV: INTEGRATION OF AN ORGANIC FIELD EFFECT TRANSISTOR WITH A POLYMER MEMS-BASED PRESSURE SENSOR

By the end of 20th century, semiconductor based micro-systems were omnipresent in everyday life. Microsystems are very "small systems" or "systems made of very small components" [57]. Microsystems perform special functions by manipulation of electrons, photons, phonons, atoms, molecules etc. Microsystems are realized by integration of mixed-domain components such as electrical, electronic, optical, mechanical, thermal, chemical and fluidics. We are now facing a new electronics revolution that has become possible due to the development and understanding of a new class of materials, commonly known as Organic (or Polymer) conductors, semiconductors, and insulators [58]-[64]. Interest in plastic electronics stems from the ability to deposit organic films on a wide variety of very low-cost substrates such as glass, plastic or metal foils. The most advanced organic electronic systems already in commercial production are high-efficiency, very bright and colorful thin displays based on organic light-emitting devices (OLEDs). Significant progress is also being made in the realization of organic thin-film transistors (OTFTs) and organic photovoltaic devices (OPVs) for low-cost solar energy generation. The enormous progress in this field has been driven by the expectation to realize new applications, such as large area, flexible displays, sensors arrays, disposable

low-cost integrated circuits or plastic solar cells. Also, almost all Microsystems and MEMS devices manufactured today are fabricated on silicon substrates using traditionally expensive semiconductor equipment and facilities. Silicon-based MEMS technology may not be the ideal technology for large area sensor array applications. Also, recent experiments showing that bulk silicon is susceptible to fatigue [3]. So, integration of polymer MEMS with organic electronics has been drawing considerable interest in the recent years [65]-[68]. Integration of an OFET and an OLED or another organic device completes the need for controlling circuitry for the operation of the OLED making it an independent all polymer micro-system. For demonstration of one such integration with the OFET, a polymer MEMS pressure sensor is chosen. The pressure sensor changes the input voltage applied to the gate of the OFET and thereby controls the output drain current corresponding to the sensing movement for various pressures.

4.1 Principle of operation

In this section, the principle of operation of the polymer MEMS pressure sensor integrated with the OFET is discussed. Figure 4.1 shows a capacitive type MEMS pressure sensor connected in series with the gate terminal of an OFET.

The equivalent electrical circuit of this series combination is shown in Figure 4.2. For a series combination of capacitors, the charge on both the capacitors becomes the same.

$$Q = C_{MEMS} V_{MEMS} = C_g V_{gs} \Rightarrow V_{MEMS} = \frac{C_g V_{gs}}{C_{MEMS}} \tag{4.1}$$

Also, using Kirchoff's Voltage Law, we can see that,

$$V_{GS} = V_{MEMS} + V_{gs} \tag{4.2}$$

Substituting Eqn. (4.1) in Eqn. (4.2), we have,

$$V_{GS} = \frac{C_g V_{gs}}{C_{MEMS}} + V_{gs} = \left(\frac{C_g}{C_{MEMS}} + 1 \right) V_{gs} \qquad \Rightarrow V_{gs} = \frac{V_{GS}}{\left(1 + \frac{C_g}{C_{MEMS}} \right)} \tag{4.3}$$

In the linear region, drain to source current, I_{DS} can be expressed as

$$I_{DS} = \mu_s \left(\frac{\varepsilon_0 \varepsilon_i}{t_i} \right) \left(\frac{W}{L} \right) \left[\left(V_{gs} - V_t \right) V_{DS} - \frac{V_{DS}^2}{2} \right] \tag{4.4}$$

Substituting Eqn. (4.3) in Eqn. (4.4), we have,

$$I_{DS} = \mu_s \left(\frac{\varepsilon_0 \varepsilon_i}{t_i} \right) \left(\frac{W}{L} \right) \left[\left(V_{GS} \frac{C_{MEMS}}{C_{MEMS} + C_g} - V_t \right) V_{DS} - \frac{V_{DS}^2}{2} \right] \tag{4.5}$$

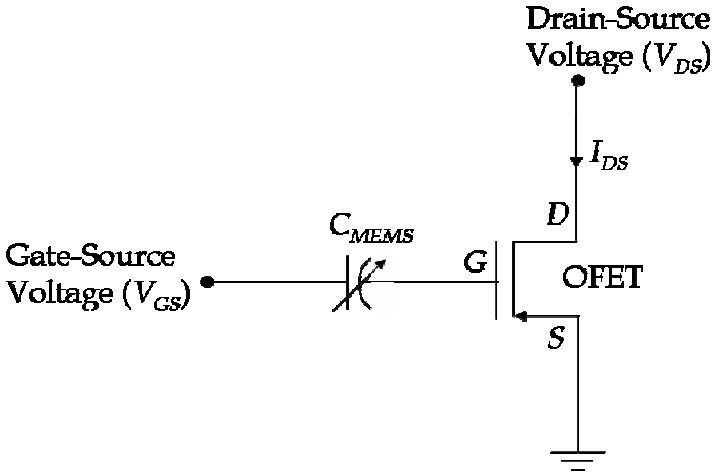


Figure 4.1. A capacitive type MEMS pressure sensor connected in series with the gate of the OFET.

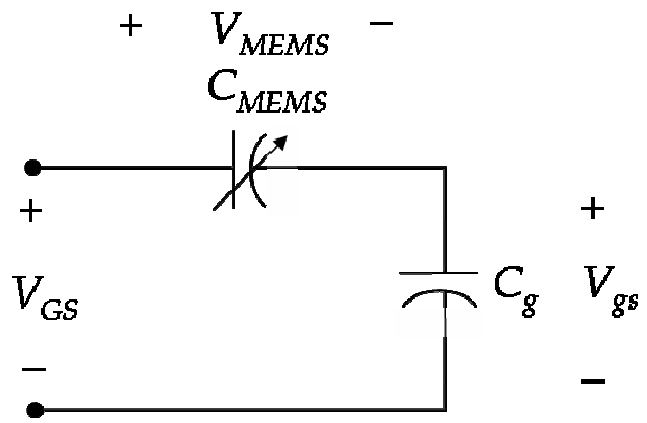


Figure 4.2. Equivalent electrical circuit for the Polymer MEMS pressure sensor integrated with an OFET.

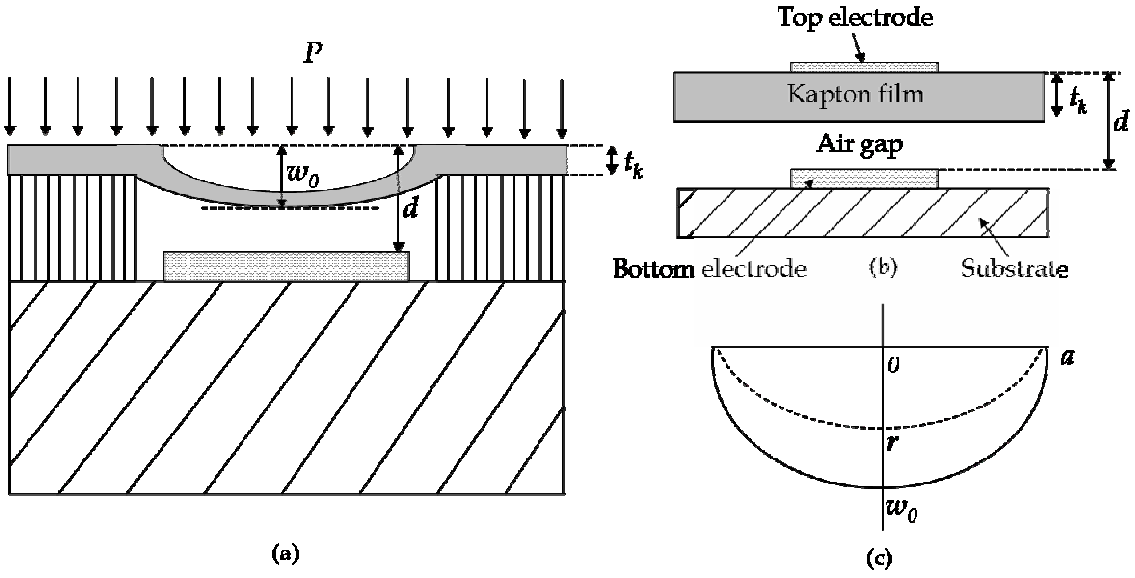


Figure 4.3. (a) Cross-sectional view of the MEMS pressure sensor with a circular membrane, (b) Close-up view of the MEMS varactor area, (c) Close-up view of the circular membrane.

Using the equations of the pressure sensor, the MEMS pressure sensor capacitance can be expressed as [69]

$$C_{MEMS} = C_0\left[1+\frac{1}{3}\left(\frac{w_0}{d}\right)+\frac{1}{5}\left(\frac{w_0}{d}\right)^2+\ldots\right] \tag{4.6}$$

where w_0 is the deflection from the center of the membrane,

d is the gap between the top and bottom electrodes as shown in Figure 4.3(a), and

C_0 is the capacitance of the sensor when no pressure is applied.

From Figure 4.3(b), it can be seen that,

$$C_0 = \frac{\varepsilon_0 \left(\pi a^2\right)}{\left(\left(d - t_k\right) + \frac{t_k}{\varepsilon_k}\right)} \tag{4.7}$$

where a is the radius of the circular membrane as shown in Figure 4.3(c).

The deflection profile of the circular membrane for an applied pressure is given by,

$$w_r = P\frac{\left(a^2 - r^2\right)^2}{64D} \tag{4.8}$$

where r is the radial distance from the center of the membrane, $0 \le r \le a$;

P is the applied pressure, and

D is the flexural rigidity/spring constant given by

$$D = \frac{Et^3}{12\left(1 - v^2\right)} \tag{4.9}$$

where E is the Elastic modulus of the membrane,

t is the thickness of the membrane, and

v is the Poisson's ratio of the membrane.

So from Eqn. (4.8), for radial distance, r = 0, $w_0 = \frac{Pa^4}{64D}$ (4.10)

Substituting Eqn. (4.10) in Eqn. (4.6), we have,

$$C_{MEMS} = C_0\left[1 + \frac{1}{3d}\left(\frac{Pa^4}{64D}\right) + \frac{1}{5d^2}\left(\frac{Pa^4}{64D}\right)^2 + \ldots\right] \tag{4.11}$$

Neglecting the higher order terms, (11) can be reduced to

$$C_{MEMS} = C_0\left[1+\frac{1}{3d}\left(\frac{Pa^4}{64D}\right)+\frac{1}{5d^2}\left(\frac{Pa^4}{64D}\right)^2\right] \tag{4.12}$$

Using these expressions, the capacitance-to-pressure variation and drain current-to-pressure variation can be estimated. Table 4.I shows the different parameters employed and their values.

Table 4.I. Different parametric values employed to determine the variations of the MEMS capacitance and drain current with applied pressure.

Parameter	**Value**
Permittivity of free space, ε_0	8.854e-12 F/m
Young's modulus of elasticity of Kapton, E	5.38 MPa
Poisson's ratio of Kapton, ν	0.32
Relative permittivity of Kapton, ε_k	3.1
Thickness of Kapton, t_k	50e-06 m
Relative permittivity of the dielectric, BCB, ε_i	2.65
Thickness of BCB, t_i	0.4e-06 m
Gap between the top and bottom electrodes, d	100e-06 m
Radius of the circular membrane, a	1e-03 m
Width of the OFET, W	1000e-06 m
Length of the OFET, L	50e-06 m
Gate-to-source voltage, V_{GS}	-70 V
Drain-to-source voltage, V_{DS}	-70 to 0 V
Estimated threshold voltage, V_t	-20 V
Estimated mobility of the OFET, μ_s	0.8e-08 m^2/V-s

The gate-to-channel capacitance, C_g was calculated to be about 36 pF by connecting the OFET as shown in Figure 4.4. Figure 4.5 shows the plot of the MEMS capacitance as the pressure is varied from 0 to 160 kPa. The code for this plot, which was generated using MATLAB, is provided in Appendix E. From the plot, it can be gathered that the capacitance of the MEMS pressure membrane varies from 0.42 pF to about 0.49 pF causing a 70 fF variation overall.

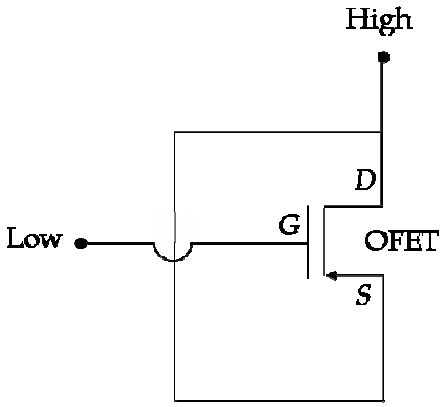


Figure 4.4. The electrical circuit connections of the OFET to obtain the gate-to-channel capacitance.

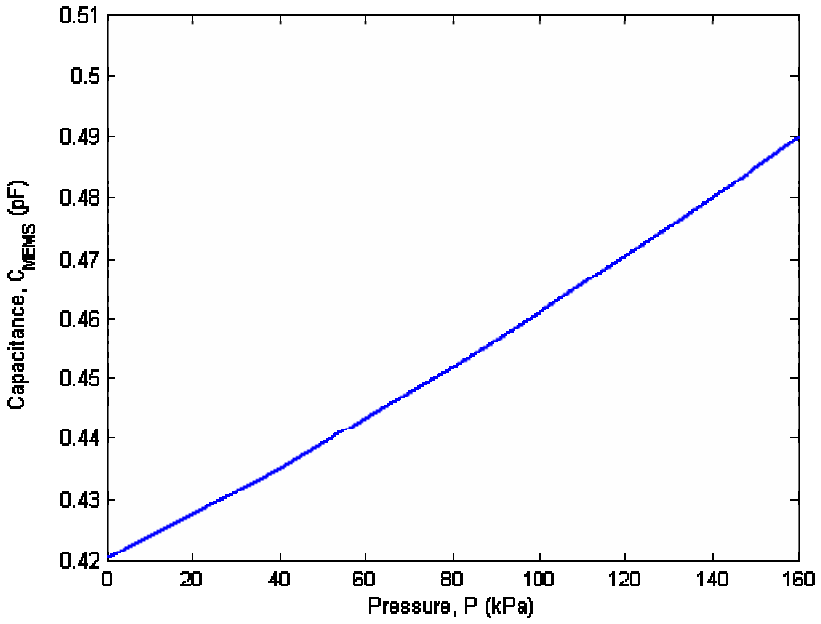


Figure 4.5. A plot of the capacitance of the MEMS pressure sensor with varying pressure.

In order to obtain a relation between the drain current, I_{DS} and applied pressure, P, we can substitute Eqn. (4.12) in Eqn. (4.5) which yields

$$I_{DS} = \mu_s \left(\frac{\varepsilon_0 \varepsilon_i}{t_i} \right) \left(\frac{W}{L} \right) \left[\left(V_{GS} \left(\frac{C_0 \left[1 + \frac{1}{3d} \left(\frac{Pa^4}{64D} \right) + \frac{1}{5d^2} \left(\frac{Pa^4}{64D} \right)^2 \right]}{\left(C_0 \left[1 + \frac{1}{3d} \left(\frac{Pa^4}{64D} \right) + \frac{1}{5d^2} \left(\frac{Pa^4}{64D} \right)^2 \right] \right) + C_g} \right) - V_t \right) V_{DS} - \frac{V_{DS}^2}{2} \right] \tag{4.13}$$

Eqn. (4.13) draws a complex relation between the variation of the drain current, I_{DS} with applied pressure, P. When the pressure outside the sensor cavity is increased above the atmospheric level, the pressure sensor membrane deflects downward toward the bottom electrode and increases the sensor capacitance, C_{MEMS} between the top and bottom electrodes. When C_{MEMS} is small compared to C_g, an increase in the sensor capacitance decreases the voltage drop across the sensor and increases the gate voltage, V_{gs} applied to the OFET. In the OFET, the increase in the gate voltage, V_{gs} increases the drain current, I_{DS}. Thus, the mechanical movement of the pressure sensor in response to an applied external pressure is used to modulate the OFET drain current. Figure 4.6 is a plot of I_{DS} generated using MATLAB with the parameters mentioned in Table 4.I as the pressure is varied from 0 to 200 kPa. This plot shows that there is a steady increase in current as the pressure applied on the membrane is increased. A detailed MATLAB code is provided in Appendix E.

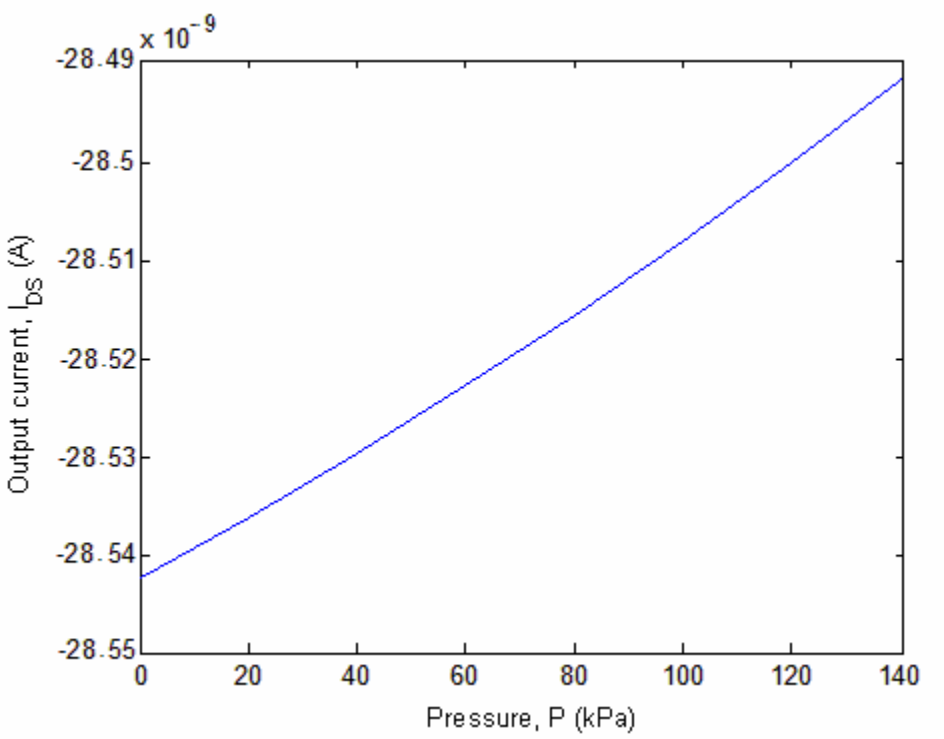
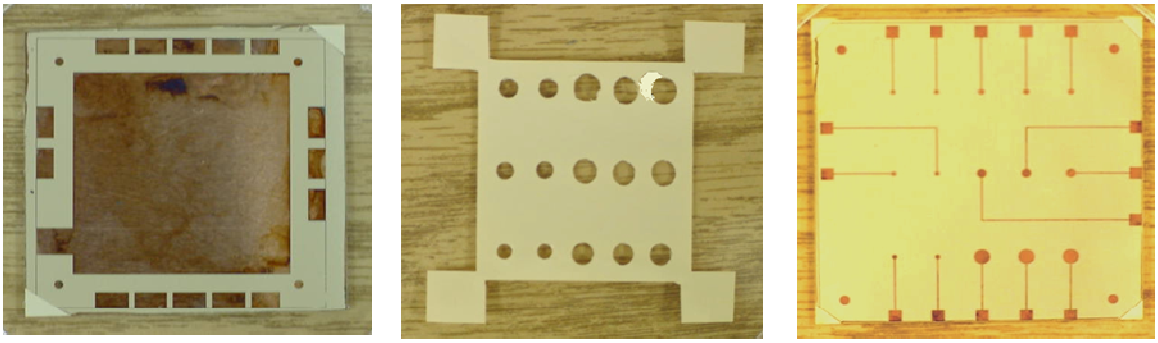


Figure 4.6. A graph of the drain current, I_{DS} to the pressure, P applied on the MEMS sensor.

4.2 MEMS Pressure Sensor

The MEMS pressure sensor described in this section has been developed by our research group [70]. It was fabricated using printed circuit processing techniques. The MEMS pressure sensor consists of a cylindrical cavity formed by a sandwich of a 30 mil thick Liquid Crystal Polymer (LCP) substrate, a 2 mil thick LCP spacer film (with circular holes) and a 2 mil thick LCP MEMS layer. The photographs of the three layers are shown in Figure 4.7. The bottom electrode of the sensor is defined on the substrate by photolithography and wet etching processes. The top electrode of the sensor is defined on the bottom side of the LCP MEMS layer by photolithography and wet etching processes. In the spacer layer, circular holes are defined by mechanical machining. These three layers are laminated by thermo-compression bonding at normal atmospheric pressure

using a press. After bonding, the sealed cavity of the pressure sensor is at atmospheric level. A photograph of the fabricated MEMS pressure sensor is shown in Figure 4.8.



(a) (b) (c)

Figure 4.7. The three layers of the polymer MEMS pressure sensor: (a) Bottom electrode, (b) Spacer Film and (c) Top Electrode.

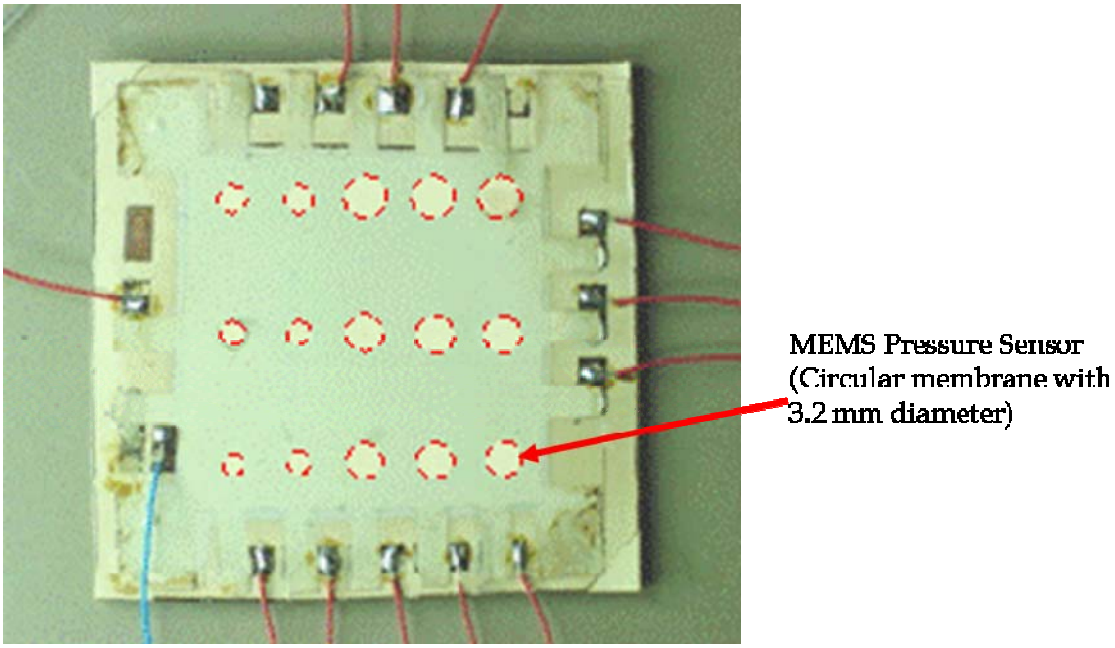


Figure 4.8. Photograph of the MEMS pressure sensor after thermo-compression bonding.

The MEMS pressure sensor was placed in a sealed pressure chamber and the capacitance variation with a change in the pressure applied was recorded. Figure 4.9 shows the plot of the measured capacitance of the MEMS pressure sensor as the pressure

was varied from 0 to 160 kPa [56]. The capacitance with no pressure applied was measured to be 3.52 pF. It was observed that as the pressure increased, the capacitance increased steadily and settled at 3.59 pF. Hence the variation is about 70 fF.

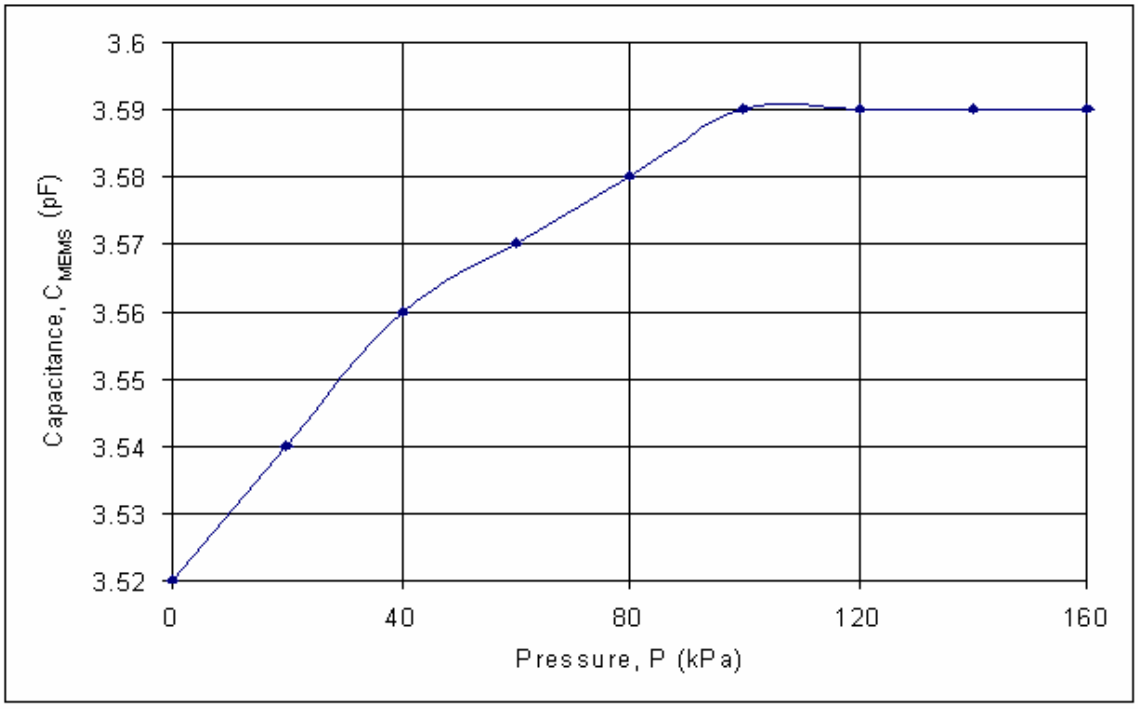


Figure 4.9. A graph showing the variation of the measured MEMS capacitance with applied pressure.

4.3 Integration of MEMS Pressure Sensor and the OFET

Experiments were conducted by simply connecting the MEMS pressure sensor and the OFET demonstrated in the previous chapter through wires. Figure 4.10(a) shows the cross-sectional view and Figure 4.10(b) shows the top view of the connections. The experimental setup employed for the testing of these devices is shown in Figure 4.11. It consists of a probe station, a semi-conductor parametric analyzer, and a pressure chamber. The MEMS pressure sensor is placed inside the chamber and the OFET drain current is measured at various pressures. Figure 4.12 shows the generated pressure vs. the

drain current characteristics. This plot was generated for a gate source voltage, V_{GS} = -65 V. From the plot, it can be observed that for a drain voltage, V_{DS} = -50 V, the drain current increases from -103 nA to -282 nA when the pressure is increased from 0 to 50 kPa. Hence, we can see that there is a considerable increase in the drain current of the OFET when pressure is applied to the MEMS pressure sensor.

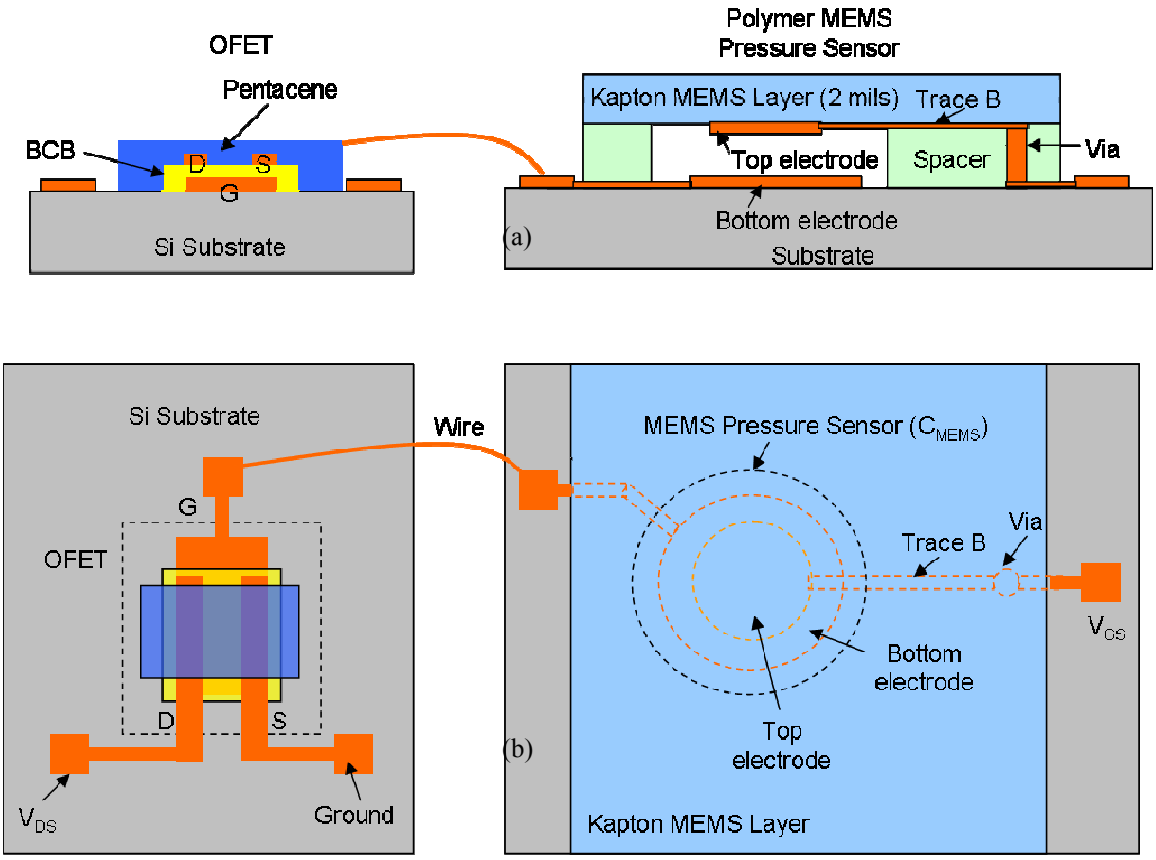


Figure 4.10. Schematic diagram of the wire integration of the MEMS pressure sensor and the OFET: (a) Cross-sectional view and (b) Top view.

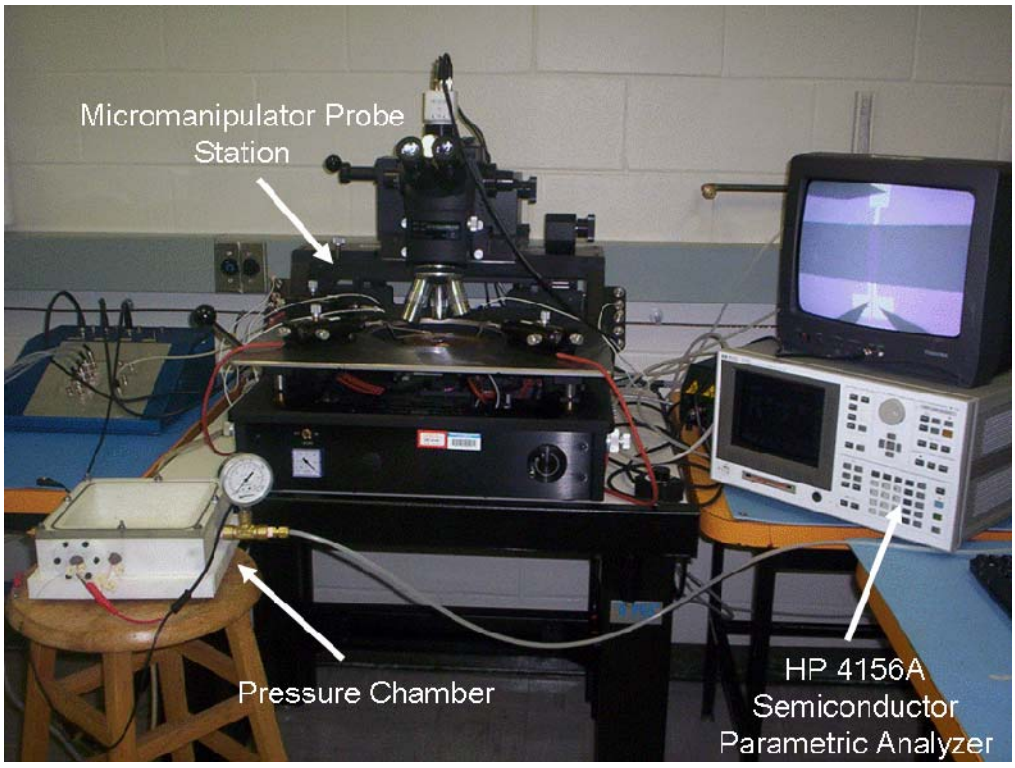


Figure 4.11. The experimental setup used for obtaining the pressure sensor vs. the drain current characteristics.

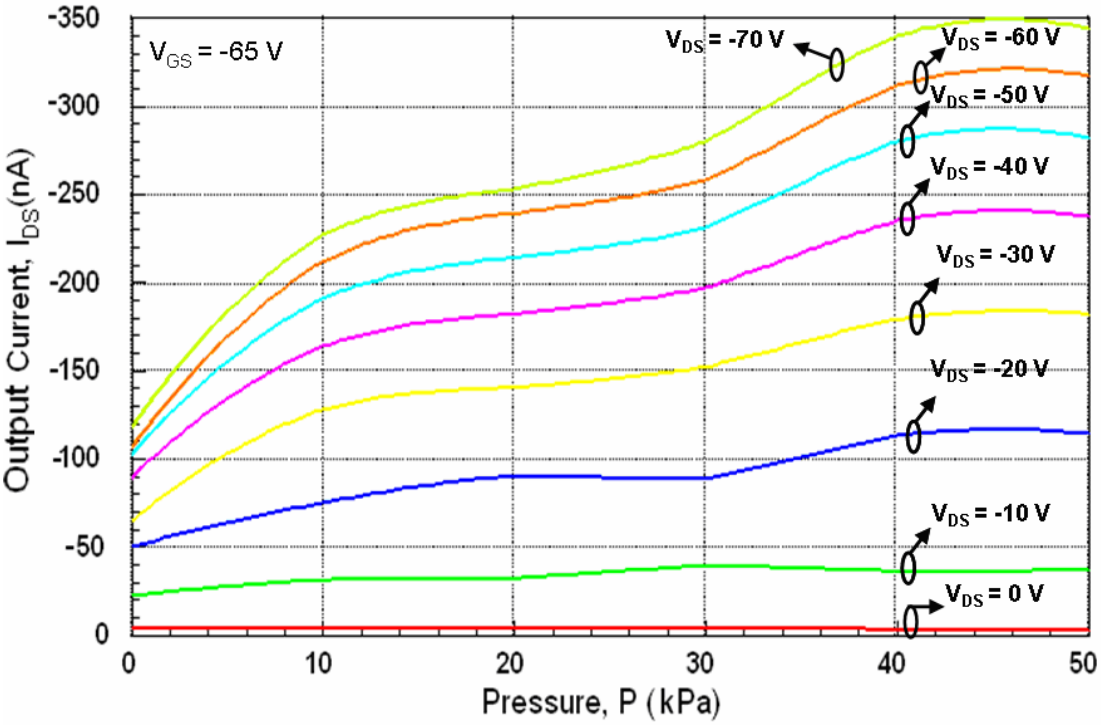


Figure 4.12. Pressure Versus Drain Current Characteristics for the Polymer MEMS sensor.

4.4 Monolithic Integration of MEMS Pressure Sensor and the OFET

The ultimate goal of this project is to develop a monolithic all polymer integration of the MEMS pressure sensor and the OFET. Figure 4.13 shows the schematic diagram of one such integration.

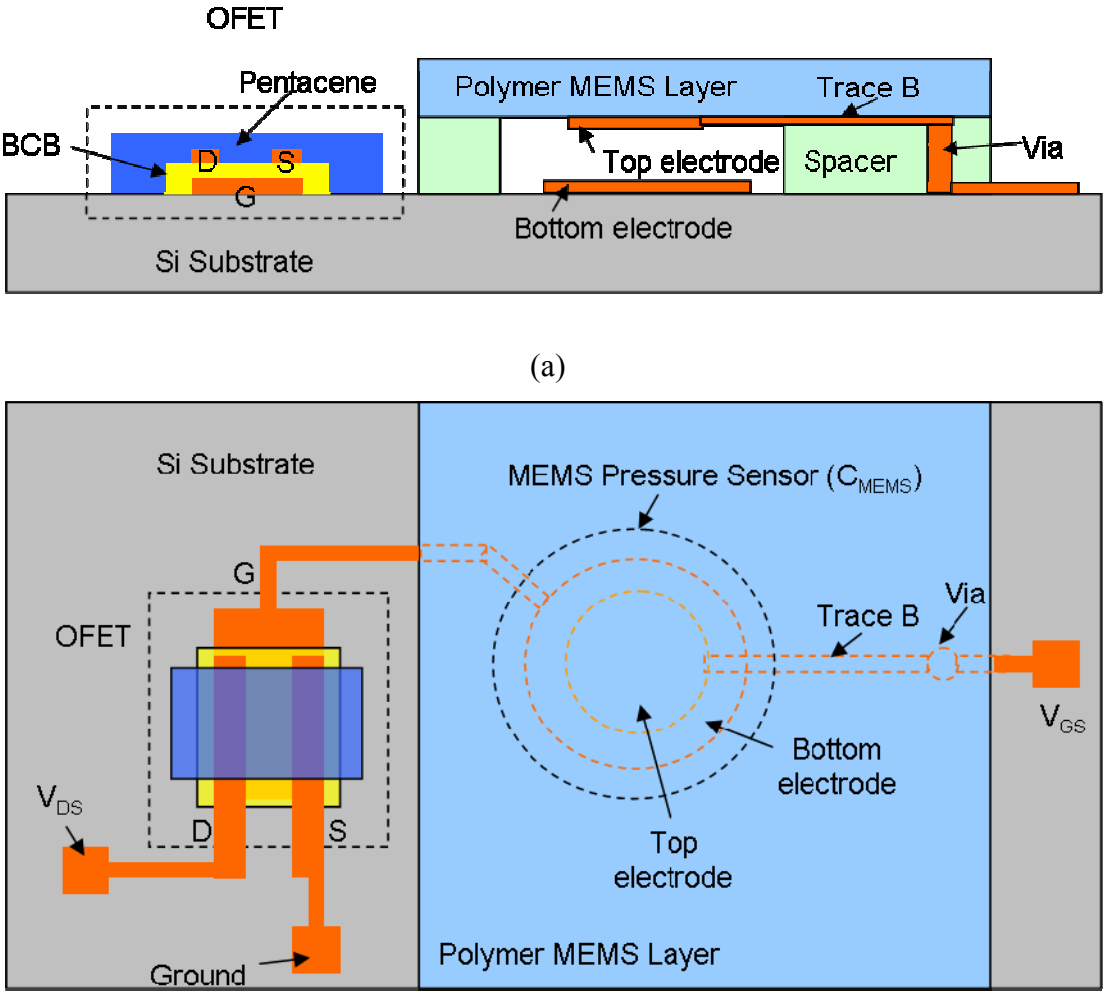


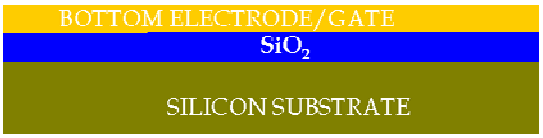
Figure 4.13. Schematic configuration of the Polymer MEMS pressure sensor monolithically integrated with an OFET: (a) Cross-sectional view and (b) Top View.

Based on the capacitance measurements and the range of the pressure sensor, a new design was developed where in both the pressure sensor and OFET would be fabricated

on the same substrate. This design was then fabricated using printed circuit processing techniques. Kapton film was employed as the top MEMS layer and polyflon film was cut through mechanical machining to form the spacer film. A step-by-step account of the fabrication process is provided in Figure 4.14. A traveler detailing the fabrication process is provided in Appendix F. A photograph of the fabricated device is shown in Figure 4.15.

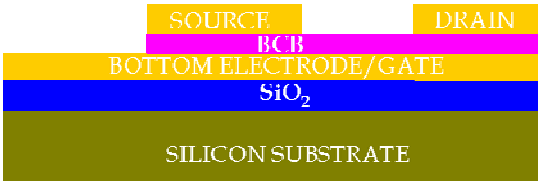
Before tests can be run on the integrated device, the organic field effect transistor and the MEMS pressure sensor were tested separately. The OFET was tested using a HP 4145A parametric analyzer. The output and transfer characteristics of the transistor are shown in Figure 4.16 and Figure 4.17, respectively. It can be observed that the OFET exhibits characteristics similar to a traditional FET. Also, the pressure sensor variation was tested in a sealed pressure chamber. The capacitance variation to the change in pressure is plotted in Figure 4.18. It can be seen that the capacitance varies about 250 fF from 7.7 to 7.95 pF. This test was repeated about 4-5 times with less than 1% tolerance error. The 250 fF capacitance variation is almost thrice as much as the previous MEMS pressure sensor employed for the wire integration. In addition to this, the OFET employed in the previous section is connected in series with the new sensor and the sensing mechanism is tested. A plot of the measured drain current of the OFET with changes in the applied pressure is shown in Figure 4.19. It can be noted that as the pressure increases, the drain current also increases. It can also be seen that the drain current is lower as is the change in the drain current when compared to the results of the wire integration.

Step 1: A modified gold gate electrode is deposited on an oxidized Si substrate.



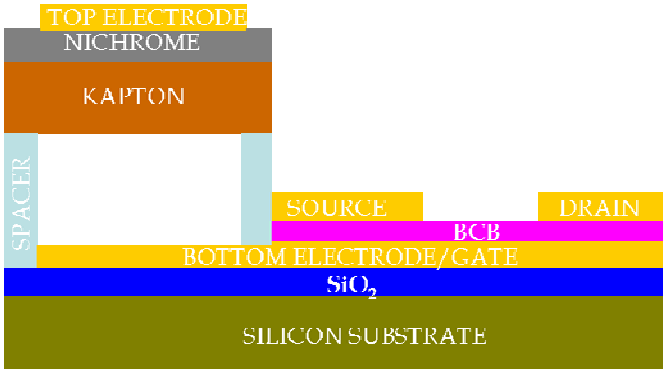
Step 2: A dielectric is spin-coated and patterned on the gate electrode.

Step 3: Gold electrodes are deposited to act as the drain and source.



Step 4: Top layer of MEMS electrode is defined on a Kapton film

Step 5: Thermo-compression bonding of the substrate and Kapton film using a spacer film.



Step 6: A p-type material is deposited on top through thermal evaporation. The pads and the top electrode are protected from this deposition by the use of a tack film.

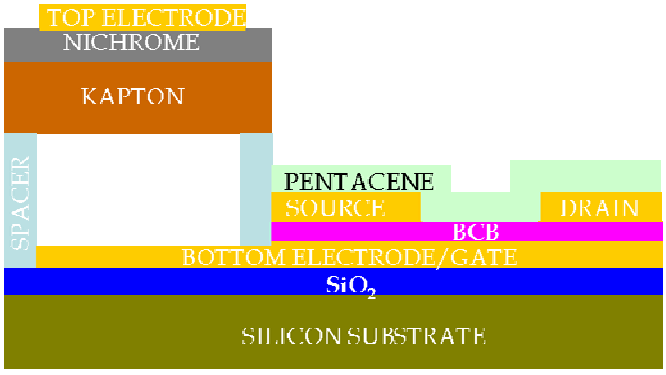


Figure 4.14. Fabrication process for the monolithically integrated OFET and MEMS pressure sensor.

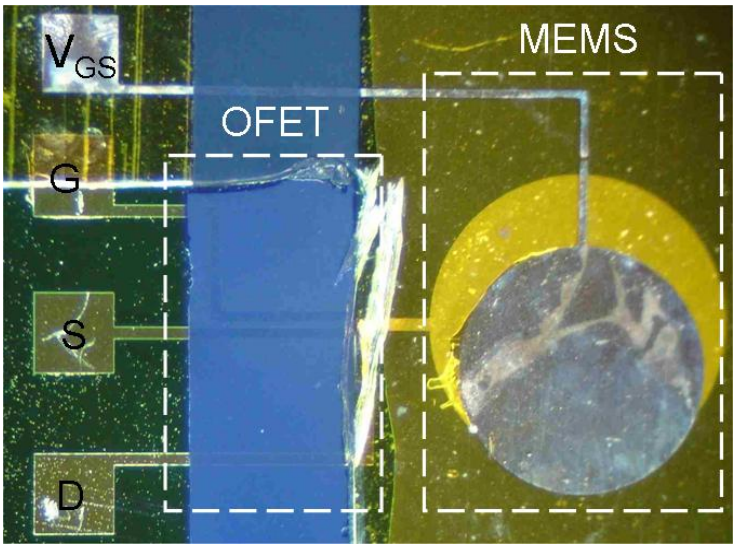


Figure 4.15. Photograph of the fabricated MEMS pressure sensor monolithically integrated with an OFET.

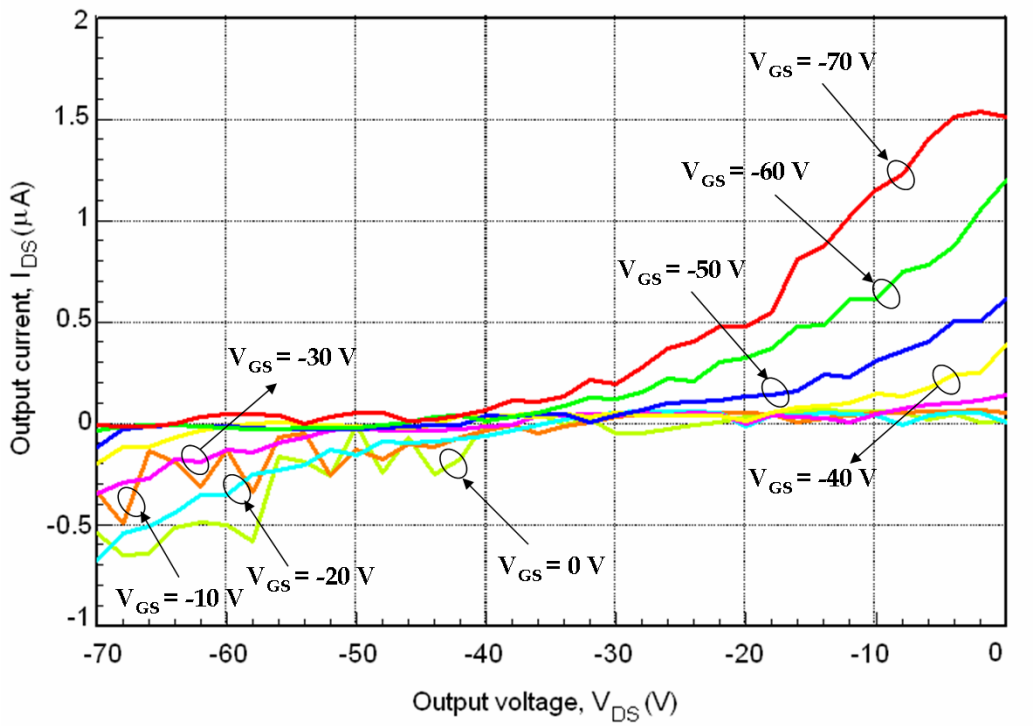


Figure 4.16. Output characteristics of the OFET monolithically integrated with a MEMS pressure sensor.

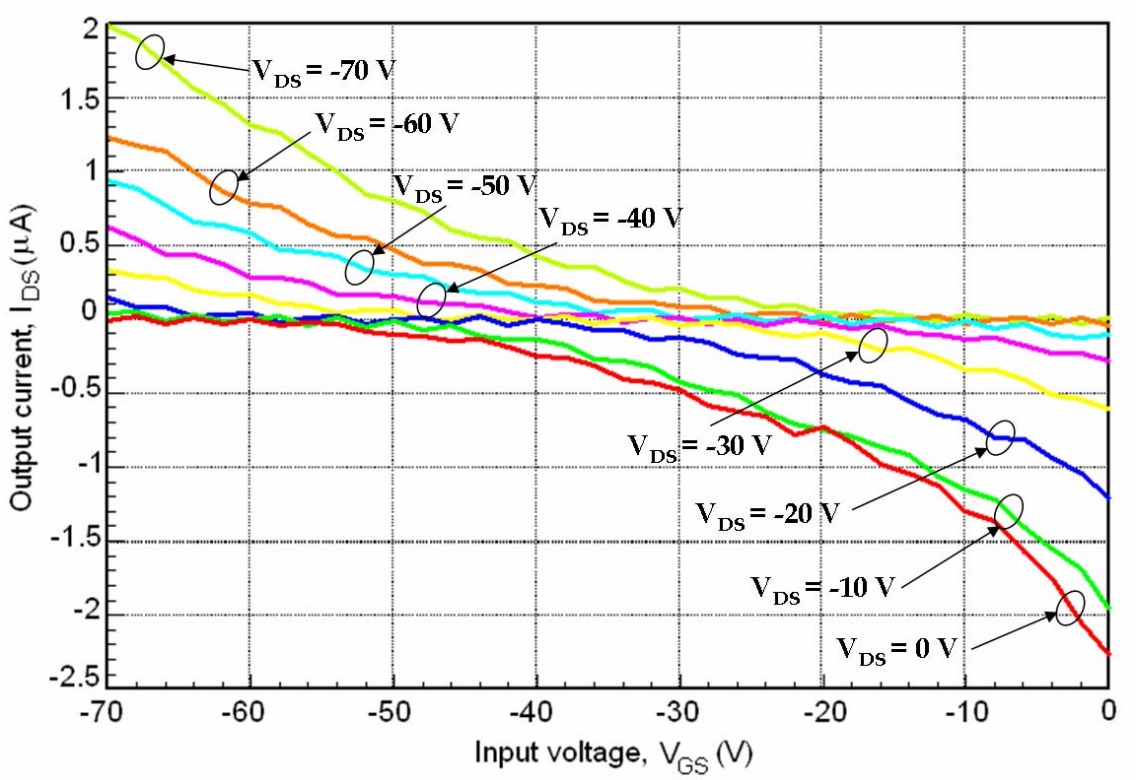


Figure 4.17. Transfer characteristics of the OFET monolithically integrated with a MEMS pressure sensor.

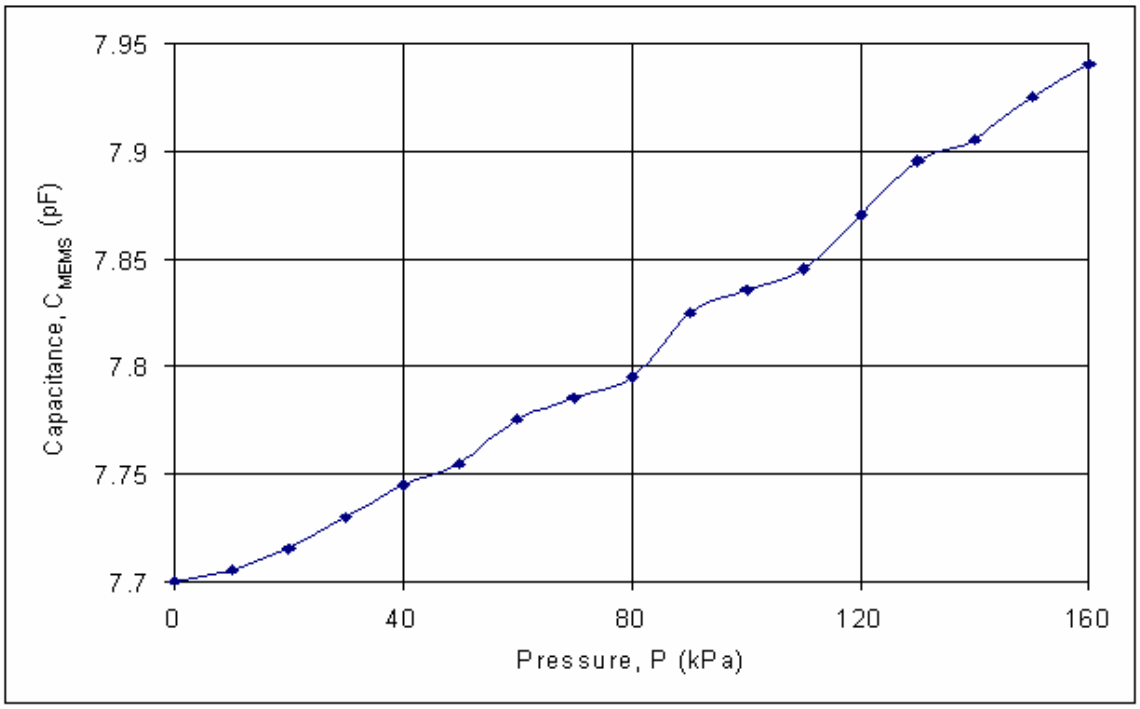


Figure 4.18. A graph of the capacitance of the pressure sensor to the pressure applied.

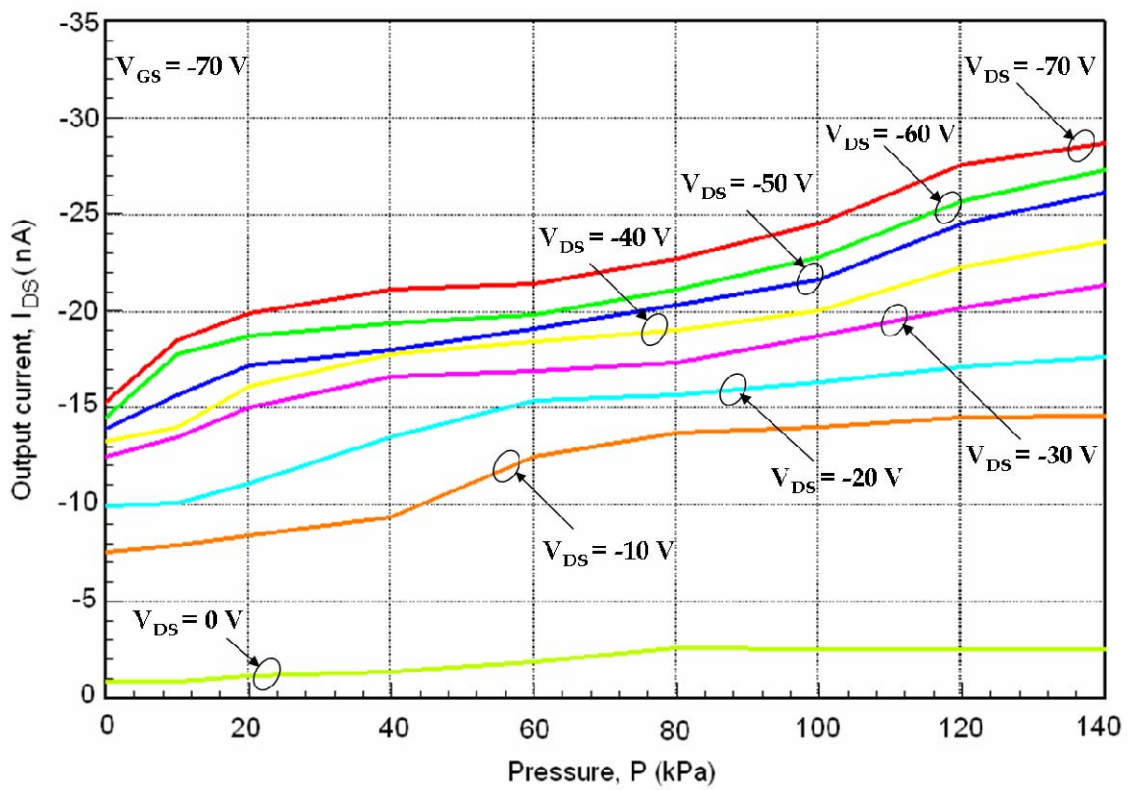


Figure 4.19. A graph of the drain current of the OFET discussed in chapter 3 tested in conjunction with the new Kapton-based MEMS pressure sensor.

Since both the devices were shown to be working well, the monolithically integrated OFET and MEMS pressure sensor were analyzed as a series combination. Figure 4.20 shows the graph of the drain current of the OFET plotted against the applied pressure. From the plots, it can be gathered that the drain current does not change significantly with the change in applied pressure. Some of the factors contributing to this phenomenon could be that the gate capacitance, C_g of the MEMS pressure sensor and OFET series combination is about 7.6 pF, which is quite higher than the design value of about 0.8 pF. This change could have been brought about by the parasitics in the connecting wires. Also, the p-type material, Pentacene is known to degrade in performance under prolonged exposure to light and moisture.

This chapter has presented the design, fabrication and testing of a series integration of a MEMS pressure sensor and an OFET. The wire integration results have successfully demonstrated that an increase in pressure on the MEMS pressure sensor manifests itself as an increase in the drain current. However, the monolithic integration did not replicate these results although the OFET and the MEMS pressure sensor were tested individually and were found to be functioning adequately.

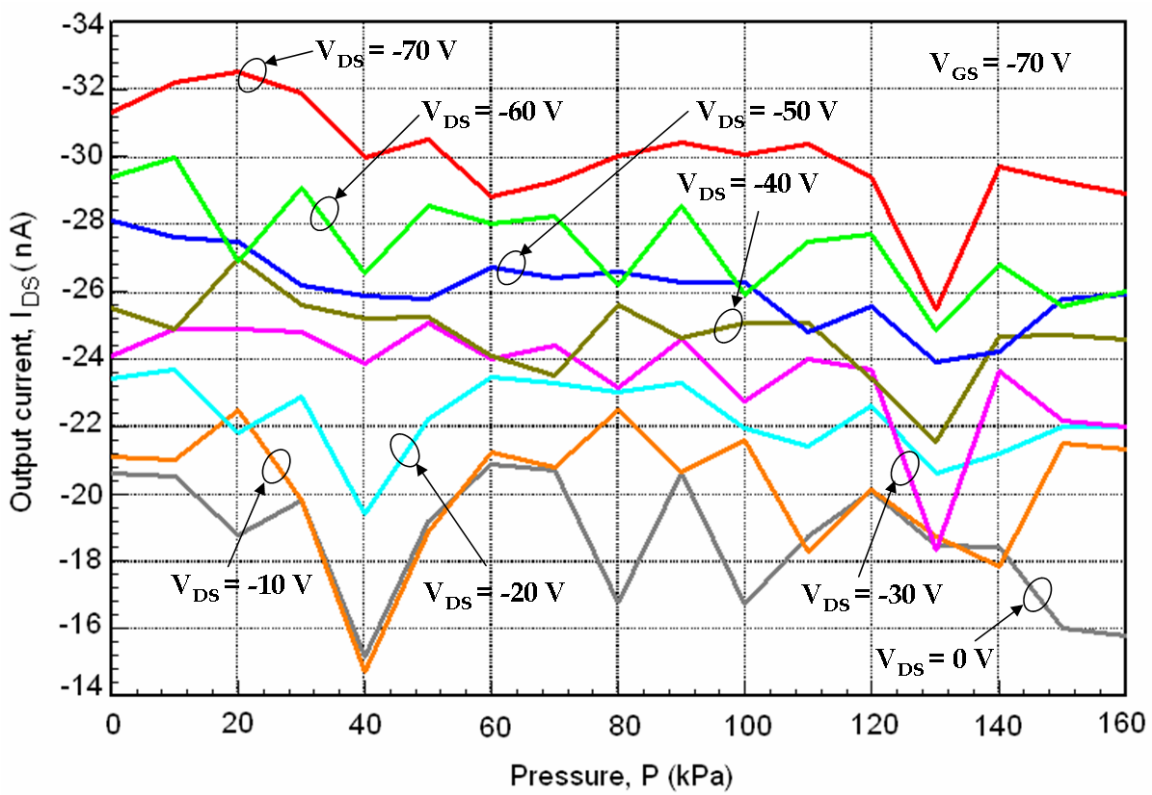
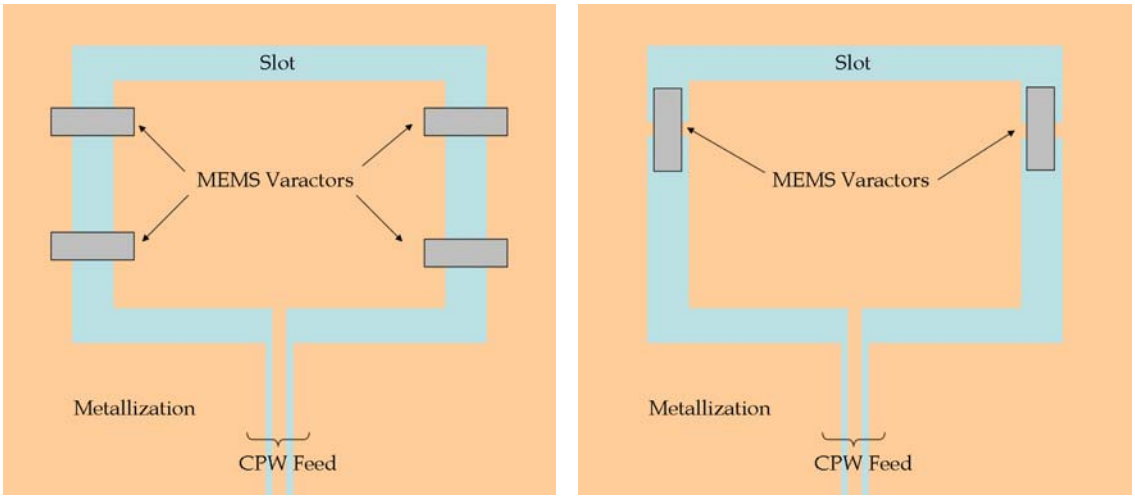


Figure 4.20. A graph of the drain current of the monolithically integrated OFET tested with the new Kapton-based MEMS pressure sensor.

CHAPTER V: CONCLUSIONS AND FUTURE WORK

5.1 MEMS-based Frequency agile antennas

Chapter 2 described a MEMS-based tunable coplanar patch antenna. The patch antenna was made tunable in the range of 5.185 GHz to 5.545 GHz, achieving a 330 MHz bandwidth. The return loss was better than -20 dB. Although the patch antenna was originally designed to operate at 3.5 GHz, adding an actuation pad caused a frequency shift to 5.5 GHz. There was a MEMS varactor warpage problem. It was overcome by readjusting the bonding fixture and placing Kapton pieces in the air gap between the MEMS electrode and the antenna. The next step would be to explore the idea of increasing the number of MEMS varactors on the antenna in order to elicit a larger bandwidth. Also, reconfigurable antennas can be modeled to be integrated with RF MEMS switches to achieve frequency bands like GSM (0.9 GHz), GPS (1.57 GHz), DCS (1.8 GHz) and WLAN (2.4 GHz and 5.2 GHz). Figure 5.1 shows two configurations where multiple MEMS varactors are placed along the non-radiating edges to help the antenna tune in a wider frequency range. These models need to be explored further.



(a) (b)

Figure 5.1. (a) and (b): Possible configurations of MEMS-based frequency agile antennas.

5.2 Organic electronics and micro-systems

Chapter 3 presented an Organic Field Effect Transistor (OFET) with Pentacene, a p-type semi-conductor polymer, BenzoCycloButene (BCB) as the gate dielectric and gold was used for the metal pads. Although, the design was unresponsive initially, widening the gate electrode supplied the required field effect. The electrical characteristics of this transistor were observed to be similar to that of silicon-based transistors. Some key advantages of the OFET include no gate leakage current and the ability to handle high voltages. Low mobility and slow switching times are some of the drawbacks.

Chapter 4 illustrated a wire integration of a MEMS-based pressure sensor with the OFET discussed in Chapter 3. It was observed that the pressure variation in the pressure sensor brought about a change in the output drain current of the transistor. So, the sensing movement was able to control the output of the transistor. However, the monolithic integration of the MEMS pressure sensor and the OFET could not replicate the same results. The reasons behind that are currently being probed. First, the measured

capacitance of the pressure sensor was 10 times the design value. So, it can be seen that a lot of parasitics are involved that are degrading the performance of the integrated FET. When the OFET discussed in Chapter 4 was tested separately, the device was found to be in working condition and exhibiting FET characteristics. The measured drain current of the OFET was a big improvement compared to the OFET presented in Chapter 3. The current increased from hundreds of nA to tens of μA which also boosted the mobility of the new OFET. The performance of the MEMS pressure sensor was also evaluated separately and found to be satisfactory. When the MEMS pressure sensor and the OFET were tested together, a big drop was noticed in the output current of the transistor. A better design that will reduce the affect of parasitics needs to be developed. Also, the performance of Pentacene is affected by exposure to light and moisture [71]. In the future processes, one way to overcome this is to coat a passivation layer like poly-chloro-para-xylylene (parylene) on top of Pentacane to protect it from atmospheric affects [72]. Also, other conjugated polymers that have better alignment of organic molecules leading to lower band gaps and higher mobilities need to be explored. Also, dipping the drain and source metal layers in alkane thiols can improve carrier injection between the p-type semiconductor polymer and the metal [73].

The project was able to develop a 'Polymer Microsystem' by integration of a Polymer MEMS device and Organic Electronics. Traditionally, microsystems have been fabricated using silicon-like semiconductor substrates by micromachining techniques. Silicon (or thin-film in general) may be the ideal substrates for semiconductor devices, but they may not be suitable for all microsystem applications. In particular, silicon based wafer level

technology may not be suitable for cost effective manufacturing and packaging of microsystems for large area and large volume applications. The proposed work was to demonstrate a plastic microsystem using low cost fabrication techniques. As a proof-of-concept of the proposed plastic microsystem, this project demonstrated the integration of a Polymer MEMS pressure sensor with an organic field effect transistor.

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APPENDIX A

TRAVELER FOR FABRICATING A TUNABLE COPLANAR PATCH ANTENNA

I. Substrate:

The substrate to be used should have been cut to the right dimensions and should have 4 holes drilled that are spaced 42 mm from every adjacent hole and have a diameter of $1/16^{th}$ inch + 1mil (for clearance).
The substrate must first be cleaned with acetone, methanol and water; then dried off with a nitrogen gun. The substrate must subsequently be dipped in a weak sulphuric acid solution (a couple of drops of sulphuric acid in a regular bowl filled with water) for a couple of minutes to remove any oxidation.

1. **Etching copper off of the backside**: This process can either be done prior to any processing or after defining the antenna.

Step 1 **Photoresist application** on the side to be used to define the antenna. Stick blue tack film on the other (back) side so that no photo resist sticks to that side.

Photoresist	S1813
Spin Speed	2500 rpm
Spin Ramp	500 rpm
Spin Time	30 secs

Step 2 **Soft bake** (Remove the tack film as it will wrinkle under high temperatures)

Temperature	110 ^{0}C
Time	60 secs

Step 3 **Etching**

Etchant	CE-200
Time	4 mins

Step 4 **Acetone/Methanol Cleaning**

Cleaner	First Acetone then Methanol
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until the substrate is completely dry

2. Defining the antenna: Take the side that has copper on it.

Step 1 Acetone/Methanol Cleaning

Cleaner	First Acetone then Methanol
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until the substrate is completely dry

Step 2 Photoresist application

Photoresist	S1813
Spin Speed	2500 rpm
Spin Ramp	500 rpm
Spin Time	30 secs

Step 3 Soft bake

Temperature	110 ^{0}C
Time	60 secs

Step 4 Photoresist Exposure

Mask used	ANTENNA_TCPA
Exposure Time	45 secs

Step 5 Post-exposure bake

Temperature	110 ^{0}C
Time	60 secs

Step 6 Photoresist Develop

Developer	CD-30
Time	45 secs
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until the substrate is completely dry

Step 7 Acetone/Methanol Cleaning

Cleaner	First Acetone then Methanol
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until the substrate is completely dry

3. Spincoating BCB: A mask having the pattern of the BCB should be available as a glass mask for this process. **Note:** Do not use film mask for this process.

Step 1 Adhesion promoter application (AP3000)

Spin Speed	3000 rpm
Spin Ramp	1000
Spin Time	30 secs

Step 2 Soft Bake

Temperature	120 ^{0}C
Time	30 secs

Step 3 BCB (Cyclotene 4024-40) application for a thickness of ~ 7 µm). Let BCB spread on the substrate for a minute.

Spread Speed	500 rpm
Ramp	500
Time	5 secs
Speed	1500 rpm
Ramp	1000
Time	30 secs

Step 4 Soft Bake

Temperature	95 ^{0}C
Time	90 secs

Step 5 Photoresist Exposure

Mask used	BCB_MASK
Exposure Time	15 secs

Step 6 Pre Develop Bake

Temperature	80 ^{0}C
Time	30 secs

Step 7 Puddle Develop Process: The spinner is used for this process.

Developer	DS2100 (Pour it on the wafer and let it sit for 75 secs.)
Rinse Speed	500 rpm
Ramp	500
Rinse Time	5 secs
Speed	2500 rpm
Ramp	1000
Time	30 secs

Step 8 Post Develop Bake

Temperature	70 ^{0}C
Time	60 secs

Step 9 Curing BCB: The BCB coated substrate is cured in a nitrogen oven for 2-3 hours by letting the temperature ramp up to 200 ^{o}C.

II. Kapton film:

1. Kapton film cleaning

Step 1 Acetone/Methanol Cleaning

Cleaner	First Acetone then Methanol
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until film is completely dry

Step 2 Oxidation Removal

Remover	250 ml DI water + 2 drops of H_2SO_4 using a pipette
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until film is completely dry

Step 3 Acetone/Methanol Cleaning

Cleaner	First Acetone then Methanol
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until film is completely dry

2. Etching the backside of the Kapton film

Step 1 Copper Etching (Cover the front side using blue tack squares)

Etchant	CE-200
Time	8 secs
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until film is completely dry

Step 2 Nichrome Etching

Etchant	250 ml DI water + 10 gm $KMnO_4$ + 5 gm NaOH
Time	60 secs
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until film is completely dry

Step 3 Acetone/Methanol Cleaning

Cleaner	First Acetone then Methanol
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until film is completely dry

3. Gluing the film on a wafer

Step 1 4" Wafergrip application

Peel wafergrip and put it on a clean and smooth wafer

Step 2 Heat wafer on hot plate

Temperature	110 ^{0}C
Time	till wafergrip melts and sticks to the wafer

Step 3 Stick film on wafer

While the wafer gel is still in molten state, stick the Kapton film starting with one edge and smoothing the entire film on the gel without any unevenness

4. Defining the electrode

Step 1 Photoresist application

Photoresist	S1813
Spin Speed	2500 rpm
Spin Ramp	500 rpm
Spin Time	30 secs

Step 2 Soft bake

Temperature	110 ^{0}C
Time	60 secs

Step 3 Photoresist Exposure

Mask used	ELECTRODE_TCPA
Exposure Time	15 secs

Step 4 Photoresist Develop

Developer	CD-30
Time	45 secs
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until film is completely dry

Step 5 Post Develop Bake

Temperature	110 ^{0}C
Time	60 secs

Step 6 Copper Etching

Etchant	CE-200
Time	8 secs
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until film is completely dry

Step 7 Photoresist Removal

Photoresist Remover	First Acetone then Methanol
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until film is completely dry

Step 8 Nichrome Etching

Etchant	250 ml DI water + 10 gm $KMnO_4$ + 5 gm NaOH
Time	60 secs
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until film is completely dry

Step 9 Acetone/Methanol Cleaning

Cleaner	First Acetone then Methanol
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until film is completely dry

5. Aluminum deposition

Step 1 Oxidation Removal

Remover	250 ml DI water + 2 drops of H_2SO_4 using a pipette
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until film is completely dry

Step 2 Acetone/Methanol Cleaning

Cleaner	First Acetone then Methanol
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until film is completely dry

Step 3 Aluminum deposition

Process	E-beam
Thickness	5000 ^{0}A

Step 4 Acetone/Methanol Cleaning

Cleaner	First Acetone then Methanol
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until film is completely dry

6. Patterning Aluminum for Deep Reactive Ion Etching

Step 1 Photoresist application

Photoresist	S1813
Spin Speed	2500 rpm
Spin Ramp	500 rpm
Spin Time	30 secs

Step 2 Soft bake

Temperature	110 ^{0}C
Time	60 secs

Step 3 Photoresist Exposure

Mask used	DRIE_TCPA
Exposure Time	15 secs

Step 4 Photoresist Develop

Developer	CD-30
Time	45 secs
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until film is completely dry

Step 5 Post Develop Bake

Temperature	110 ^{0}C
Time	60 secs

Step 6 Aluminum Etching

Etchant	PAE
Time	15 mins

7. Deep Reactive Ion Etching (DRIE)

The machine used for performing the DRIE etching of the Kapton film is an STS AOE (Advanced oxide etch) .The configuration of the gases used for this etch in our facility is 8 sccm CF4 and 35 sccm Oxygen with 500 Watts of RF power. The ratio of the gases is the most important part and not the exact quantity of the gases. These processing parameters take about 75-85 minutes to etch a 2 mil thick Kapton layer. Before starting this process, it is extremely important to check if the Kapton film is stuck properly to a silicon substrate with the thermally conductive gel without any air bubbles. If air bubbles are present between the substrate and the film, it results in inconsistent etching of the Kapton film. A simple procedure to check for any trapped air bubbles in the Kapton film after it is glued to the silicon wafer is to put the wafer in the wafer holder of the STS system and hit “Pump + Map” on the software screen. This feature will cause the Kapton film to be put under some pressure thereby revealing the hidden air bubbles. Once the bubbles are located, the wafer should be put on a hot plate. After giving the gel adequate time to melt again, all the bubbles should be nudged out through the corners of the Kapton film with the help of a small clean tissue (the clean room certified ones) which is rolled up to form a hard edge. After the film has been flattened out, it should be checked again for bubbles in the STS system. This process may be repeated until the film is satisfactorily flat.

Now,

- Place the wafer on a wafer holder in the STS system.
- Hit “Pump+Map” on the software screen. (Assuming that there are no bubbles, proceed to next step.)
- Hit “Load” on the software screen.

- To create a Kapton recipe program for the STS system:
  Click on "Recipe". Then click on "New".
  Any new recipe opens with two default steps- Gas Line Purge and Standby step.
  1. Gas Line Purge
     No of cycles: 1

  2. Standby Step

Standby Gas:	Argon
Flow Rate:	0 sccm
Base Pressure:	1 mTorr
Pressure Tip:	94 mTorr
Pump Down Time:	00:00:20 hh:mm:ss
Purge Time:	00:00:10 hh:mm:ss
Pump Out Time:	00:00:30 hh:mm:ss

1. Add New Step. This step can be renamed as desired. It comes with 6 tabs.
   General
   Pressure
   Gases
   R.F.
   HBC and
   HeLUR

General:

Recipe Process Mode:	Θ Discrete O Continuous
Pump Down Time:	00:00:20 hh:mm:ss
Gas Stabilization:	00:00:20 hh:mm:ss
Process Time:	00:05:00 hh:mm:ss
Pump Out Time:	00:00:30 hh:mm:ss

The total process time required for a 2 mil Kapton film is around 75-85 minutes.

Process:

APC Mode:	O Manual Θ Automatic
Process Pressure	
Pressure:	60 mTorr
Tolerance:	25 %
Base Pressure:	0 mTorr
Pressure Tip:	94 mTorr

Gases:

Gas	Flow (sccm)	Tolerance

O_2	35 sccm	10 %
CF_4	8 sccm	5 %
Active Gases:		O_2 and CF_4
Illegal Combination:		H_2

R.F.:
O 13.56 MHz on Platen Only
O 13.56 MHz on Coil Only
Θ Simultaneous

13.56 MHz Generator connected to Coil

Power:	500 W
Tolerance:	25 %

Matching Auto

Match Load:	50 %
Match Tune:	50 %

13.56 MHz Generator connected to Platen

Power:	100 W
Tolerance:	25 %

Matching Auto

Match Load:	50 %
Match Tune:	50 %

All the other options are left unaltered.

- Save and close this recipe.
- In order to ensure that this recipe is selected, click on "Select" and select this recipe from the list.

Hit "Process". Each cycle will have a process time of 5 minutes. Repeat the process until the process time reaches a total of about 75-85 minutes. The process time can be started at 5 minutes at first and increased to a suitable no. depending on the machine.

8. Post-DRIE Aluminum Etching

Step 1 Aluminum Etching

Etchant	6 gm NaOH + 200 ml DI water
Time	3 mins

Step 2 Acetone/Methanol Cleaning

Cleaner	First Acetone then Methanol

DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until film is completely dry

9. Defining the bias lines

Step 1 Photoresist application

Photoresist	S1813
Spin Speed	2500 rpm
Spin Ramp	500 rpm
Spin Time	30 secs

Step 2 Soft bake

Temperature	110 ^{0}C
Time	60 secs

Step 3 Photoresist Exposure

Mask used	BIAS_LINES_TCPA
Exposure Time	60 secs

Step 4 Photoresist Develop

Developer	CD-30
Time	45 secs
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until film is completely dry

Step 5 Post Develop Bake

Temperature	110 ^{0}C
Time	60 secs

Step 6 Copper Etching

Etchant	CE-200
Time	8 secs
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until film is completely dry

Step 7 Photoresist Removal

Photoresist Remover	First Acetone then Methanol
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until film is completely dry

10. Final film cleaning

Step 1 Wafer gel Cleaning

Cleaner	Amyl Acetate
Temperature	150 ^{0}C
Time	until film lifts off the wafer with no residual wafer gel on it

Step 2 Acetone/Methanol Cleaning

Cleaner	First Acetone then Methanol
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until film is completely dry

Chemical Incompatibilities:

1. Copper etchant, CE-200 removes Aluminum faster than it removes copper.
2. Photoresist Developer, CD-30 attacks Nichrome while H_2SO_4 does not.
3. Nichrome etchant reacts with photoresist, S1813.
4. Aluminum etchant, NaOH reacts with photoresist, S1813.
5. Aluminum etchant, PAE etches copper too.
6. BCB process:
    a. Do not rinse the substrate in acetone/methanol after the deposition of BCB.
    b. BCB is very viscous. Any bubbles that may arise are hard to put out. So, proper care should be taken when handling BCB.
    c. A dab of T1100 on a swab can be used to remove residual BCB, if any.

APPENDIX B

MEASUREMENTS WITH THE WYKO OPTICAL PROFILOMETER

A picture of the WYKO measurement system is shown in Figure 1. As can be seen from Figure 1, the WYKO measurement system consists of an objective microscope, a field of vision microscope (controlled through software), a stage, and microscope movement controlling joystick all interfaced to the software Vision 32. The procedure to make measurements using this system will be explained in the following sections.

1. To start measurements, open the software Vision 32 (Shortcut to V32 on desktop) on the interfaced computer. Once the software is opened, *Hardware → Intensity*. The Intensity and Focus window should open up and the software screen it should look like in Figure 2.

2. Place the device or sample to be measured under the microscope in the light beam and reduce the intensity to about 50% (use the sliding bar under the intensity and focus window to do this). The screen should look something like what is shown in Figure 3 (predominantly grey).

3. To adjust the focus of the microscope on the device, we need to select a suitable objective lens. To do this, go to *Hardware → Measurement options.*
    a. In the options tab, change the resolution to half (this is sufficient for our measurement purposes).
    b. In the measurement mode, select ***VSI.***
    c. In the objective drop down menu, select 5X or whatever is suitable and select 1X from the FOV dropdown menu.
    d. Now, in the VSI options tab, check 3X speed in the scan options, uncheck the high speed/large memory checkbox, set backscan and length to 10 um and 30 um respectively. (Backscan is the scan distance in the negative z axis from the focused surface and length is the scan distance in the positive z axis.)

4. **Focusing:** We are ready to focus the interferometer on the desired surface. The coarse and fine movement of the microscope is controlled by two knobs shown in Figure 4.

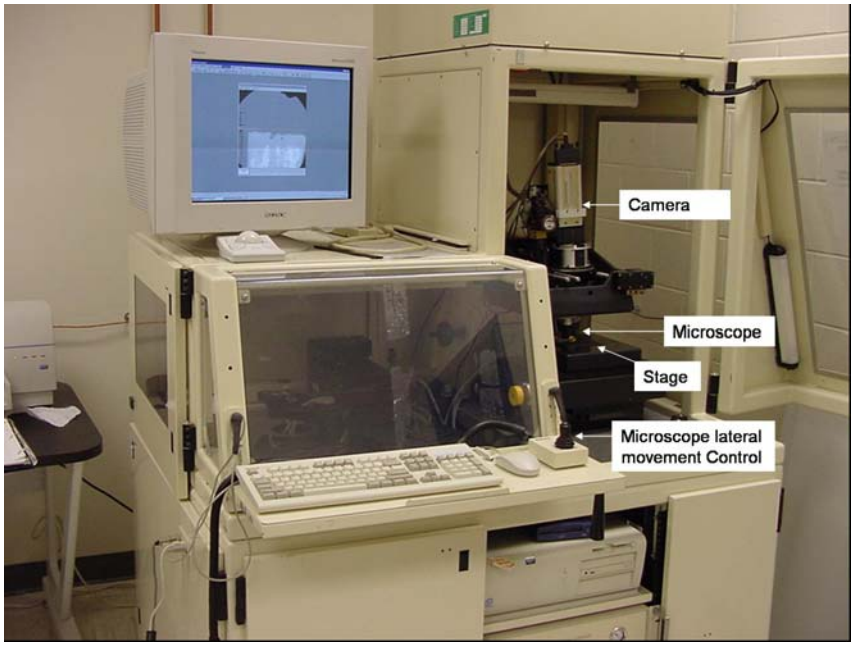

Figure 1. The WYKO Measurement system.

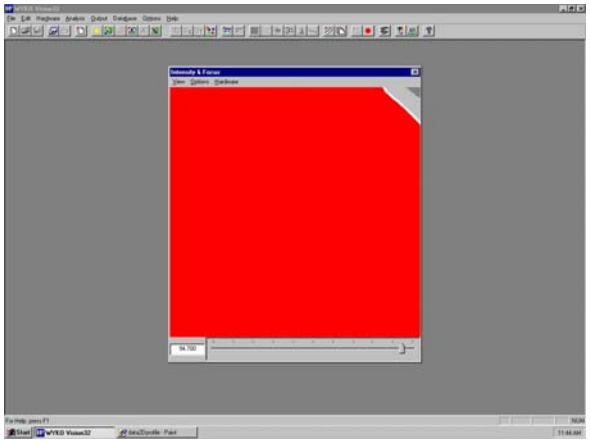

Figure 2. Initial Intensity and Focus window.

Use the coarse knob until you see fringe lines on the target surface. The fringe lines on a certain region on the surface signify that the microscope is focused on that region of the surface. We'd like the focus to be on the whole surface to make a consistent measurement throughout the field of view. To make the fringe lines focus on the whole surface in the field of view (spreading the fringes), we'll need to tilt the microscope using the microscope lateral movement control knob and use the fine adjustment knob shown in Figure 4. A close up of the lateral movement control is shown in Figure 5.

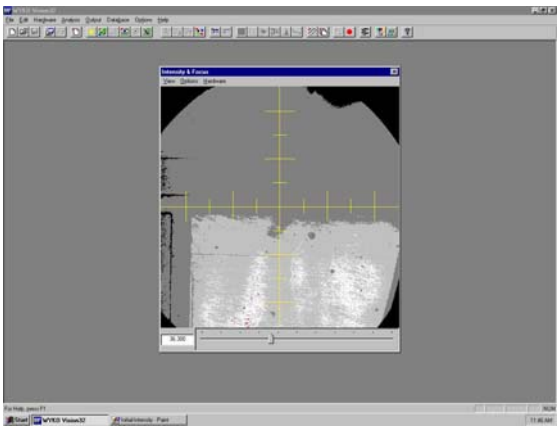

Figure 3. Adjusting Image intensity.

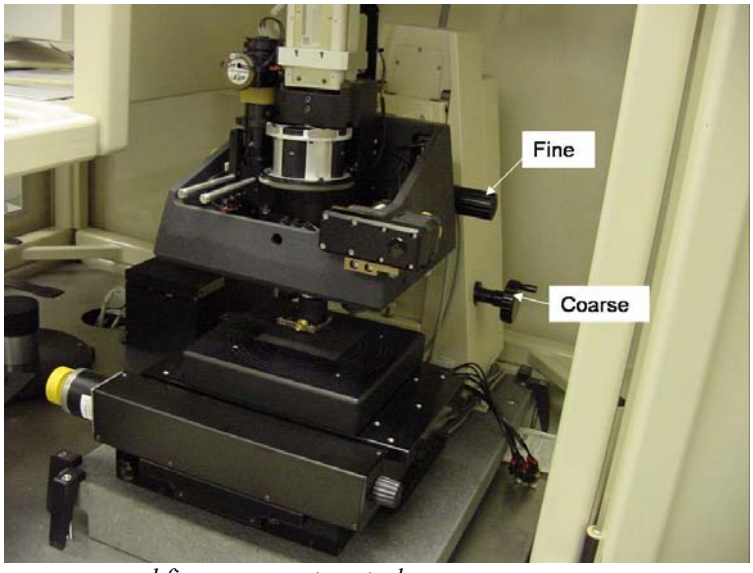

Figure 4. Microscope coarse and fine movement control.

As was explained earlier, once the fringes are seen on the intensity and focus window, we need to tilt the microscope and use the fine focus adjustment to spread the fringes. The joystick shown in Figure 5 is used for the movement along with the tip/tilt button. Moving the joystick without pressing the Tip/Tilt button moves the stage in the x and y directions and movement of the joystick when the Tip/Tilt button is pressed tilts the microscope. The movement speed control button on top of the joystick is an extremely important part of this system since it reduces the speed with which the microscope tilts. There is a very high probability of the microscope hitting the substrate if the tilting of the microscope is not handled extremely carefully.

Figure 5. Lateral movement control of microscope.

5. **Measurement:** When the fringes are spread over the target surface in the field of view, File→ New to perform measurement. Do not touch anything on the system during the measurement process.

6. **Analysis:** After the measurement is done, Analysis→ 2D. The 2D analysis window is shown in Figure 6.

7. **Interpretation of results:** Let us assume for example that going from left to right in the field of view, there is a cantilever and hence is at an elevation. The height from the substrate (assuming the fringes were focused on the substrate) is depicted by the y-axis difference between a point on the substrate and a point on the cantilever shown in the X profile. In other words, a step is shown in the X-profile measurement and the height of the step is the height of the cantilever. To position the profile lines as required in the field of view, click on the required point on the field of view. Intersection of the X-profile line (red) and the Y-profile line (blue) is depicted. Position the markers to obtain a measurement of the height difference. Markers simultaneously move in the profile plot and the field of view. The profile lines in the field of view can be moved by dragging them on the field of view or clicking at a different point.

8. **Saving the results:** File→Save to save the data. If another measurement is to be performed, close the 2-D analysis window and reopen the Illumination window and follow the procedure outlined in these instructions.

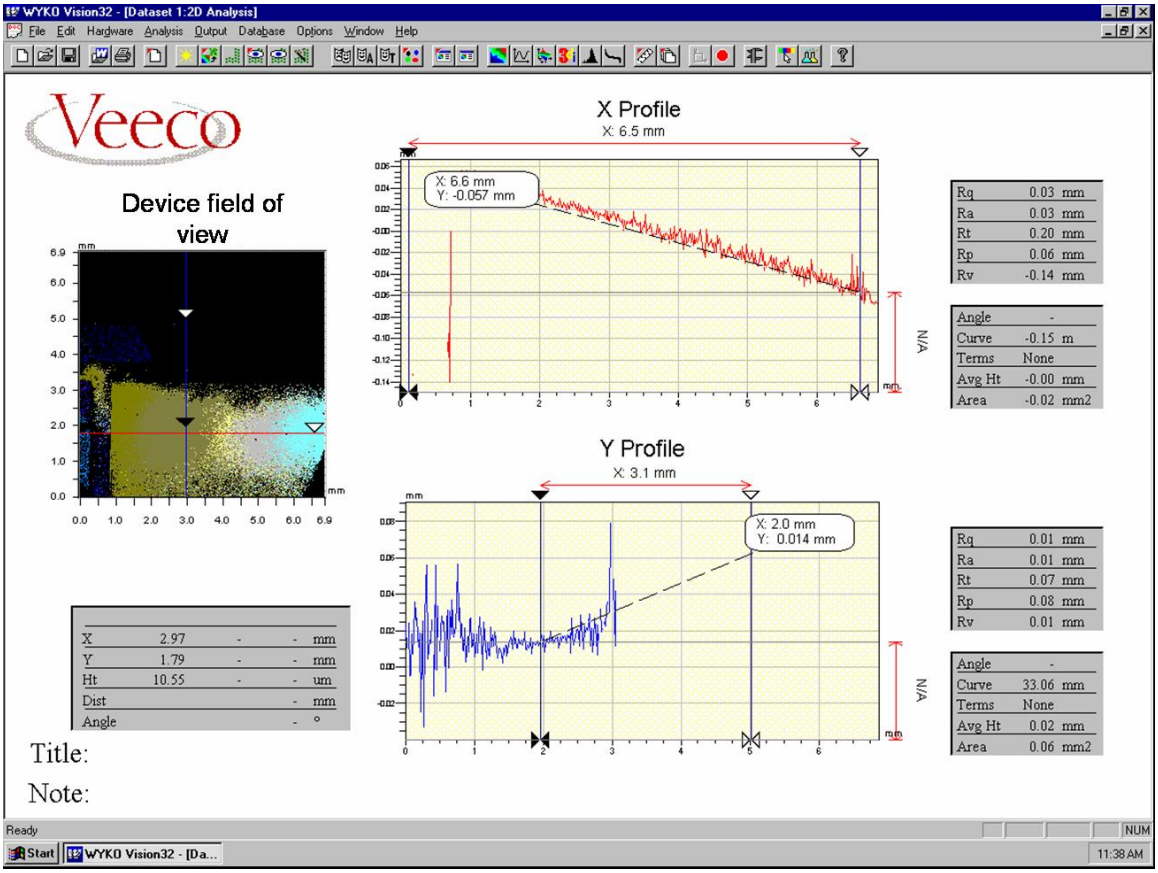

Figure 6. The x- and y- profiles of the test device.

Important note: Before shutting the system down, make sure the illumination is set to zero or else when the system is restarted, the illumination bulb will be damaged.

APPENDIX C

TRAVELER FOR FABRICATING AN OFET IN THE COPLANAR CONFIGURATION

1. **Defining the gate, drain and source electrodes:** Choose a smooth oxidized silicon wafer.

Step 1 Acetone/Methanol Cleaning

Cleaner	First Acetone then Methanol
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until wafer is completely dry

Step 2 Photoresist application (~ 2 microns thick)

Photoresist	nLOF 2035 negative photoresist
Spin Speed	3500 rpm
Spin Ramp	500 rpm
Spin Time	30 secs

Step 3 Soft bake

Temperature	110 ^{0}C
Time	60 secs

Step 4 Photoresist Exposure

Mask used	ELECTRODES_MASK
Exposure Time	15 secs

Step 5 Post-exposure bake

Temperature	110 ^{0}C
Time	60 secs

Step 6 Photoresist Develop

Developer	AZ-300 MIF
Time	90 secs
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until wafer is completely dry

Step 7 Post Develop Bake

Temperature	110 ^{0}C
Time	60 secs

Step 8 Gold deposition

Process	E-beam
Thickness	1000 ^{0}A

Step 9 Defining the gold electrodes through photoresist removal

Process	Lift-off
Developer	Acetone
Time	~ 30 mins

Step 10 Acetone/Methanol Cleaning

Cleaner	First Acetone then Methanol
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until wafer is completely dry

2. **Spincoating BCB:** A mask having the pattern of the BCB should be available as a glass mask for this process. **Note:** Do not use film mask for this process.

Step 1 Adhesion promoter application (AP3000)

Spin Speed	3000 rpm
Spin Ramp	1000
Spin Time	30 secs

Step 2 Soft Bake

Temperature	120 ^{0}C
Time	30 secs

Step 3 BCB (Cyclotene 4024-40) application for a thickness of ~ 0.5 µm). Prepare a mixture of 1:1 solution of BCB and T1100. Let this spread on the wafer for a minute.

Spread Speed	500 rpm
Ramp	500
Time	5 secs
Speed	2700 rpm
Ramp	1000
Time	30 secs

Step 4 Soft Bake

Temperature	95 ^{0}C
Time	90 secs

Step 5 Photoresist Exposure

Mask used	BCB_MASK
Exposure Time	15 secs

Step 6 Pre Develop Bake

Temperature	80 ^{0}C
Time	30 secs

Step 7 Puddle Develop Process: The spinner is used for this process.

Developer	DS2100 (Pour it on the wafer and let it sit for 75 secs.)
Rinse Speed	500 rpm
Ramp	500
Rinse Time	5 secs
Speed	2500 rpm
Ramp	1000
Time	30 secs

Step 8 Post Develop Bake

Temperature	70 ^{0}C
Time	60 secs

Step 9 Curing BCB: The BCB coated substrate is cured in a nitrogen oven for 2-3 hours by letting the temperature ramp up to 200 ^{o}C.

Note:

2. Do not rinse the substrate in acetone/methanol after this process.
3. BCB is very viscous. Any bubbles that may arise are hard to put out. So, proper care should be taken when handling BCB.
4. A dab of T1100 on a swab can be used to remove residual BCB, if any.

3. **Deposition of Pentacene:** Before this step, all the contact pads to be utilized for probe testing should be covered with a blue tack film in order to prevent deposition of Pentacene on the pads.

Process	Thermal evaporation
Deposition time	~ 30 mins

Note: Remove the tack film carefully before testing.

APPENDIX D

TRAVELER FOR FABRICATING A BOTTOM CONTACT OFET

1. Defining a gate electrode: Choose a smooth oxidized silicon wafer.

Step 1 Acetone/Methanol Cleaning

Cleaner	First Acetone then Methanol
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until wafer is completely dry

Step 2 Photoresist application (~ 2 microns thick)

Photoresist	nLOF 2035 negative photoresist
Spin Speed	3500 rpm
Spin Ramp	500 rpm
Spin Time	30 secs

Step 3 Soft bake

Temperature	110 ^{0}C
Time	60 secs

Step 4 Photoresist Exposure

Mask used	GATE_ELECTRODE
Exposure Time	15 secs

Step 5 Post-exposure bake

Temperature	110 ^{0}C
Time	60 secs

Step 6 Photoresist Develop

Developer	AZ-300 MIF
Time	90 secs
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until wafer is completely dry

Step 7 Post Develop Bake

Temperature	110 ^{0}C
Time	60 secs

Step 8 Gold deposition

Process	E-beam
Thickness	1000 ^{0}A

Step 9 Defining the gold electrode through photoresist removal

Process	Lift-off
Developer	Acetone
Time	~ 30 mins

Step 10 Acetone/Methanol Cleaning

Cleaner	First Acetone then Methanol
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until wafer is completely dry

2. Spincoating BCB: A mask having the pattern of the BCB should be available as a glass mask for this process. **Note:** Do not use film mask for this process.

Step 1 Adhesion promoter application (AP3000)

Spin Speed	3000 rpm
Spin Ramp	1000
Spin Time	30 secs

Step 2 Soft Bake

Temperature	120 ^{0}C
Time	30 secs

Step 3 BCB (Cyclotene 4024-40) application for a thickness of ~ 0.5 µm). Prepare a mixture of 1:1 solution of BCB and T1100. Let this spread on the wafer for a minute.

Spread Speed	500 rpm
Ramp	500
Time	5 secs
Speed	2700 rpm
Ramp	1000
Time	30 secs

Step 4 Soft Bake

Temperature	95 ^{0}C
Time	90 secs

Step 5 Photoresist Exposure

Mask used	BCB_MASK
Exposure Time	15 secs

Step 6 Pre Develop Bake

Temperature	80 ^{0}C
Time	30 secs

Step 7 Puddle Develop Process: The spinner is used for this process.

Developer	DS2100 (Pour it on the wafer and let it sit for 75 secs.)
Rinse Speed	500 rpm
Ramp	500
Rinse Time	5 secs
Speed	2500 rpm
Ramp	1000
Time	30 secs

Step 8 Post Develop Bake

Temperature	70 ^{0}C
Time	60 secs

Step 9 Curing BCB: The BCB coated substrate is cured in a nitrogen oven for 2-3 hours by letting the temperature ramp up to 200 ^{o}C.

Note:

5. Do not rinse the substrate in acetone/methanol after this process.
6. BCB is very viscous. Any bubbles that may arise are hard to put out. So, proper care should be taken when handling BCB.
7. A dab of T1100 on a swab can be used to remove residual BCB, if any.

3. Defining the drain and source electrodes:

Step 1 Cleaning

DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until wafer is completely dry

Step 2 Photoresist application (~ 2 microns thick)

Photoresist	nLOF 2035 negative photoresist
Spin Speed	3500 rpm
Spin Ramp	500 rpm
Spin Time	30 secs

Step 3 Soft bake

Temperature	110 ^{0}C
Time	60 secs

Step 4 Photoresist Exposure

Mask used	D_S_ELECTRODES
Exposure Time	15 secs

Step 5 Post-exposure bake

Temperature	110 ^{0}C
Time	60 secs

Step 6 Photoresist Develop

Developer	AZ-300 MIF
Time	90 secs
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until wafer is completely dry

Step 7 Post Develop Bake

Temperature	110 ^{0}C
Time	60 secs

Step 8 Gold deposition

Process	E-beam
Thickness	1000 ^{0}A

Step 9 Defining the gold electrodes through photoresist removal

Process	Lift-off
Developer	AZ 300 MIF
Time	~ 30 mins

Step 10 Cleaning

DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until wafer is completely dry

4. **Deposition of Pentacene:** Before this step, all the contact pads to be utilized for probe testing should be covered with a blue tack film in order to prevent deposition of Pentacene on the pads.

Process	Thermal evaporation
Deposition time	~ 30 mins

Note: Remove the tack film carefully before testing.

APPENDIX E

MATLAB CODE FOR GENERATING PLOTS SHOWING THE VARIATION OF MEMS CAPACITANCE AND DRAIN CURRENT WITH APPLIED PRESSURE

```
%Parameter assignment
mu=5e-7;%Estimated mobility of the OFET in m^2/V.s
ebcb=2.65; %Permittivity of BCB
tbcb=0.5e-6; %Thickness of BCB in Meters
Vgs=-60; %Gate-to-Source voltage in Volts
Vt=-20; %Estimated threshold voltage in Volts
Cg=36e-12; %Measured Gate-to-Channel capacitance in Farads
W=1000e-6; %Width of the OFET in Meters
L=50e-6; %Length of the OFET in Meters
e0=8.854e-12; %Permittivity of free space
d=100e-6;%Spacing between the top and bottom electrodes in Meters
a=1e-3; %Radius of the circular membrane in Meters
tkap=50e-6;%Thickness of the Kapton membrane in Meters
ekap=3.1; %Permittivity of Kapton
E=780e3*6.898; %Young's modulus of Kapton in kPa
v=0.32;%Poisson's ratio of Kapton

Co=e0*(pi*(a^2))/((d-tkap)+(tkap/ekap)); %Capacitance of the circular membrane
 D=E*(tkap^3)/(12*(1-(v^2))); %Flexural Rigidity

%Variation of the MEMS capacitance with Pressure
 m=0;
for P=0:20:160 %Pressure range is in kPa
m=m+1;
Pr(m)=P;
C(m)=Co+(Co*P*(a^4)/(192*D*d))+(((P*(a^4)/(D*d))^2)*Co/20480); %Expression for the MEMS
capacitance, Equation 12 from Chapter 4
Pr(m)=P;
Cmems(m)=1e12*C(m);
end
plot(Pr,Cmems)
figure

%Variation of the drain current, I_DS with Pressure
 for Vds=-60:10:0 %Voltage range is in Volts
m=0;
for P=0:20:160 %Pressure range is in kPa
m=m+1;
Pr(m)=P;
```

```
C(m)=Co+(Co*P*(a^4)/(192*D*d))+(((P*(a^4)/(D*d))^2)*Co/20480); %Expression for the MEMS capacitance, Equation 12 from Chapter 4
C1=Vgs*C(m)/(C(m)+Cg);
Ids(m)=mu*e0*(ebcb/tbcb)*(W/L).*(((C1-Vt).*Vds)-0.5*(Vds^2)); %Expression for the drain current, I_DS, Equation 5 from Chapter 4
end
plot(Pr,Ids)
hold on;
end
```

APPENDIX F

TRAVELER FOR FABRICATING A BOTTOM CONTACT OFET INTEGRATED WITH A PRESSURE SENSOR

I. Organic Transistor

1. Defining a gate electrode: Choose a smooth oxidized silicon wafer.

Step 1 Acetone/Methanol Cleaning

Cleaner	First Acetone then Methanol
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until wafer is completely dry

Step 2 Photoresist application (~ 2 microns thick)

Photoresist	nLOF 2035 negative photoresist
Spin Speed	3500 rpm
Spin Ramp	500 rpm
Spin Time	30 secs

Step 3 Soft bake

Temperature	110 ^{0}C
Time	60 secs

Step 4 Photoresist Exposure

Mask used	MODIFIED_GATE_ELECTRODE
Exposure Time	15 secs

Step 5 Post-exposure bake

Temperature	110 ^{0}C
Time	60 secs

Step 6 Photoresist Develop

Developer	AZ-300 MIF
Time	90 secs
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until wafer is completely dry

Step 7 Post Develop Bake

Temperature	110 ^{0}C
Time	60 secs

Step 8 Gold deposition

Process	E-beam
Thickness	1000 ^{0}A

Step 9 Defining the gold electrode through photoresist removal

Process	Lift-off
Developer	Acetone
Time	~ 30 mins

Step 10 Acetone/Methanol Cleaning

Cleaner	First Acetone then Methanol
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until wafer is completely dry

2. **Spincoating BCB:** A mask having the pattern of the BCB should be available as a glass mask for this process. **Note:** Do not use film mask for this process.

Step 1 Adhesion promoter application (AP3000)

Spin Speed	3000 rpm
Spin Ramp	1000
Spin Time	30 secs

Step 2 Soft Bake

Temperature	120 ^{0}C
Time	30 secs

Step 3 BCB (Cyclotene 4024-40) application for a thickness of ~ 0.5 µm). Prepare a mixture of 1:1 solution of BCB and T1100. Let this spread on the wafer for a minute.

Spread Speed	500 rpm
Ramp	500
Time	5 secs
Speed	2700 rpm
Ramp	1000
Time	30 secs

Step 4 Soft Bake

Temperature	95 ^{0}C
Time	90 secs

Step 5 Photoresist Exposure

Mask used	BCB_MASK
Exposure Time	15 secs

Step 6 Pre Develop Bake

Temperature	80 ^{0}C
Time	30 secs

Step 7 Puddle Develop Process: The spinner is used for this process.

Developer	DS2100 (Pour it on the wafer and let it sit for 75 secs.)
Rinse Speed	500 rpm
Ramp	500
Rinse Time	5 secs
Speed	2500 rpm
Ramp	1000
Time	30 secs

Step 8 Post Develop Bake

Temperature	70 ^{0}C
Time	60 secs

Step 9 Curing BCB: The BCB coated substrate is cured in a nitrogen oven for 2-3 hours by letting the temperature ramp up to 200 ^{o}C.

3. Defining the drain and source electrodes

Step 1 Cleaning

DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until wafer is completely dry

Step 2 Photoresist application (~ 2 microns thick)

Photoresist	nLOF 2035 negative photoresist
Spin Speed	3500 rpm
Spin Ramp	500 rpm
Spin Time	30 secs

Step 3 Soft bake

Temperature	110 ^{0}C
Time	60 secs

Step 4 Photoresist Exposure

Mask used	D_S_ELECTRODES
Exposure Time	15 secs

Step 5 Post-exposure bake

Temperature	110 ^{0}C
Time	60 secs

Step 6 Photoresist Develop

Developer	AZ-300 MIF
Time	90 secs
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until wafer is completely dry

Step 7 Post Develop Bake

Temperature	110 ^{0}C
Time	60 secs

Step 8 Gold deposition

Process	E-beam
Thickness	1000 ^{0}A

Step 9 Defining the gold electrodes through photoresist removal

Process	Lift-off
Developer	AZ 300 MIF
Time	~ 30 mins

Step 10 Cleaning

DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until wafer is completely dry

II. Kapton film processing for MEMS top layer

1. Kapton film cleaning

Step 1 Acetone/Methanol Cleaning

Cleaner	First Acetone then Methanol
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until film is completely dry

Step 2 Oxidation Removal

Remover	250 ml DI water + 2 drops of H_2SO_4 using a pipette
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until film is completely dry

Step 3 Acetone/Methanol Cleaning

Cleaner	First Acetone then Methanol
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until film is completely dry

2. Etching the backside of the Kapton film

Step 1 Copper Etching (Cover the front side using blue tack squares)

Etchant	CE-200
Time	8 secs
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until film is completely dry

Step 2 Nichrome Etching

Etchant	250 ml DI water + 10 gm $KMnO_4$ + 5 gm NaOH
Time	60 secs
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until film is completely dry

Step 3 Acetone/Methanol Cleaning

Cleaner	First Acetone then Methanol
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until film is completely dry

3. Gluing the film on a wafer

Step 1 4" Wafergrip application

Peel wafergrip and put it on a clean and smooth wafer

Step 2 Heat wafer on hot plate

Temperature	110 ^{0}C
Time	till wafergrip melts and sticks to the wafer

Step 3 Stick film on wafer

While the wafer gel is still in molten state, stick the Kapton film starting with one edge and smoothing the entire film on the gel without any unevenness

4. Defining the electrode

Step 1 Photoresist application

Photoresist	S1813
Spin Speed	2500 rpm
Spin Ramp	500 rpm
Spin Time	30 secs

Step 2 Soft bake

Temperature	110 ^{0}C
Time	60 secs

Step 3 Photoresist Exposure

Mask used	ELECTRODE_MEMS
Exposure Time	15 secs

Step 4 Photoresist Develop

Developer	CD-30
Time	45 secs
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until film is completely dry

Step 5 Post Develop Bake

Temperature	110 ^{0}C
Time	60 secs

Step 6 Copper Etching

Etchant	CE-200
Time	8 secs
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until film is completely dry

Step 7 Photoresist Removal

Photoresist Remover	First Acetone then Methanol
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until film is completely dry

Step 8 Nichrome Etching

Etchant	250 ml DI water + 10 gm $KMnO_4$ + 5 gm NaOH
Time	60 secs
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until film is completely dry

Step 9 Acetone/Methanol Cleaning

Cleaner	First Acetone then Methanol
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until film is completely dry

5. Final film cleaning

Step 1 Wafer gel Cleaning

Cleaner	Amyl Acetate
Temperature	150 ^{0}C
Time	until film lifts off the wafer with no residual wafer gel on it

Step 2 Acetone/Methanol Cleaning

Cleaner	First Acetone then Methanol
DI Rinse	30 secs in a bowl of slightly agitated DI water
N_2 dry	until film is completely dry

III. Integration of the MEMS pressure sensor and the organic transistor

1. **Lamination:** The Silicon wafer needs to be cut using a diamond scribing tool to fit the bonding jig shown in Figure 1. A spacer film was hand-cut and lamination of the MEMS Kapton layer and the organic transistor was performed by thermo-compression bonding at a pressure of 150 psi and a temperature of 130° C.

2. **Deposition of Pentacene:** Before this step, all the contact pads to be utilized for probe testing should be covered with a blue tack film in order to prevent deposition of Pentacene on the pads. Also, all the pressure sensors are covered with the tack film as thermal evaporation takes place in a vacuum chamber which might burst the pressure sensor.

Process	Thermal evaporation
Deposition time	~ 30 mins

   Note: Remove the tack film carefully before testing.

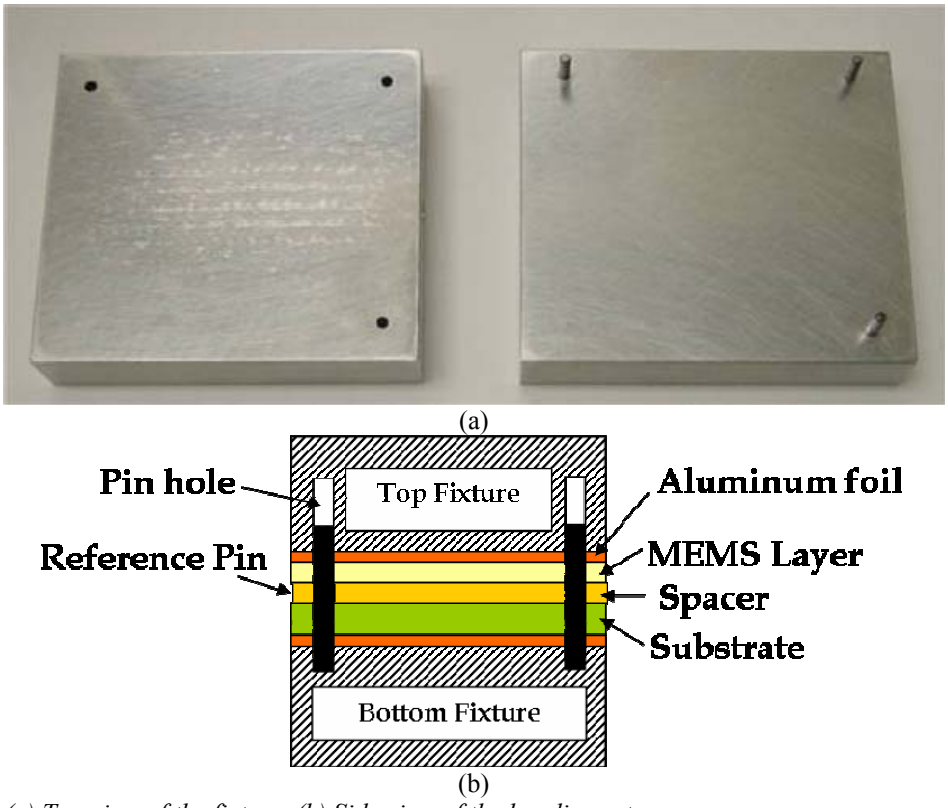

Figure 1. (a) Top view of the fixture, (b) Side view of the bonding setup.