A Linear CMOS Tunable Active Resistor

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A Linear CMOS Tunable Active Resistor

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Thesis Abstract

A Linear CMOS Tunable Active Resistor

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The demand for fast, inexpensive, and accurate sensors is increasing at a staggering rate. Deciding whether to use analog of digital signal processing for these sensors has become a challenge. Even though digital systems have become very fast, often the delay associated with digital signal processing cause stability issues in the systems. Analog circuitry is still needed for these types of systems. The challenges of using on-chip passive components are described as well as so techniques of overcoming the issue. A Linear Tunable Active resistor, proposed by Dr. Bogdan M. Wilamowski, is described in this thesis that attempts to overcome some of the shortcomings that on-chip passive components have. The design, operation, and simulation results of the active resistor are presented, as well as the use of the active resistor as replacements for passive resistors in simple filters and a Proportional-Integral-Derivative controller.

Acknowledgments

I would like to thank the members of my advisory committee for providing much help and having much patience with me during my graduate studies. I would like to thank in particular Dr. Bogdan M. Wilamowski for providing the circuits described in this thesis. I would also like to thank Dr. Michael E. Greene for giving me a job at Archangel Systems and being flexible to work around my class schedule.

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Chapter 1

Introduction

With the demand for inexpensive, fast, and accurate sensors, the need to integrate multiple systems on one chip while reducing costs is increasing. The pros and cons of analog versus digital signal processing must be weighed against one another to determine the type of ASIC to be produced. The main performance advantage that analog signal processing has over digital signal processing for these sensors is less delay and high dynamic ranges for high frequency signals [1]. Making devices smaller has lead to the ability to increase the speed of these devices and fit more dies per wafer, which lowers the manufacturing cost per device. Using on-chip passive components avoids the parasitic inductance of leads and decreases printed circuit board area, while lowering the cost of the system. While processing technology has been able to decrease the minimum feature size of active devices, on-chip passive components have not been able to keep up with their active device counterparts. However, when dealing with analog signals active components would be nothing without these passive components, so finding ways to overcome the challenges of creating high quality and high density on-chip passive components is the obvious objective.

In order to understand the impact the limitations of on-chip passive components have on the design of circuits, the design constraints of the circuit must be considered. In equation (1.1), f_c represents the corner frequency of an RC circuit, e.g., low-pass filter or high-pass filter.

$$f_c = \frac{1}{2 \cdot \pi \cdot R \cdot C} \tag{1.1}$$

With a corner frequency of $1000Hz$ the RC time constant of the circuit would be $1ms$. Table (1.1) shows the capacitance between each layer of the AMIS C5 process provided by MOSIS Integrated Circuit Fabrication Service [2].

CAPACITANCE PARAMETERS	N+	P+	POLY	POLY2	M1	UNITS
AREA (substrate)	439	752	101			$\frac{aF}{\mu^2}$
AREA (N+active)			2411			$\frac{aF}{\mu^2}$
AREA (P+active)			2328			$\frac{aF}{\mu^2}$
AREA (poly)				929	61	$\frac{aF}{\mu^2}$

Table 1.1: Capacitance Parameters for AMIS C5 process

The most commonly used capacitor is the polysilicon to polysilicon capacitor because of its manufacturability. The capacitance value for a poly-poly capacitor in this process is $\approx 1\frac{fF}{\mu m^2}$. Allowing a maximum of $1000\mu m^2$ for a capacitor yields a capacitor value of $1pF$. Substituting $1pF$ for C and $1000Hz$ for f_c back into equation (1.1) and solving for R gives

$$R = \frac{1}{2 \cdot \pi \cdot 1000 \cdot 10^{-12}} \approx 160M\Omega \tag{1.2}$$

Table (1.2) shows the resistor value of each layer per unit area.

PROCESS PARAMETERS	N+	P+	POLY	PLY2HR	M1	UNITS
Sheet Resistance	80.7	103.8	22.8	949	0.09	$\Omega/\square$
Contact Resistance	61.6	158.8	19.3			Ω
Gate Oxide Thickness	143					angstroms

Table 1.2: Resistor Parameters for AMIS C5 process

Due to cost constraints, resistors are made of either low doped polysilicon or source drain diffusion areas, which are susceptible to circuit coupled noise [3]. High resistance polysilicon provides $\approx 1000\frac{\Omega}{\square}$. Equation (1.3) calculates the area of high resistance polysilicon needed to realize a resistance of $160M\Omega$, with one $\square = 1\mu m^2$ then

$$Area = 160e^6\Omega \cdot \frac{1\mu m^2}{10^3\Omega} = 160000\mu m^2 \tag{1.3}$$

The resulting calculation produces an area 160 times the maximum allowable size, and therefore impractical.

Not only is a resistor of this magnitude not practical due to the area it will consume, but also the noise generated by large resistances starts to be a concern. The Johnson noise generated from a resistor is defined by equation (1.4). Substituting the correct values for the variables gives

$$V_t = \sqrt{4 \cdot k \cdot T \cdot R} = \sqrt{4 \cdot 1.38 \cdot 10^{-23} \cdot 300 \cdot 160 \cdot 10^6} = \frac{1.62\mu V}{\sqrt{Hz}} \tag{1.4}$$

A resistor with this magnitude will generate noise of $\frac{1.62\mu V}{\sqrt{Hz}}$. In sensors, since accuracy is the key objective, any source of noise must be eliminated. Since this thermal noise is

proportional to the resistance value, a way to lower the resistance value must be found [4]. Fortunately, some clever techniques have been developed in order to ease the limitations of on-chip passive components.

1.1 Increasing Capacitance

The only way to lower the resistance needed, while maintaining the same RC time constant is to increase the capacitance. The parallel plate capacitance, equation (1.5) is used. There are three methods to increase capacitance in parallel plate capacitors,

1. Increase area of electrodes
2. Increase the permativity, ϵ, of the dielectric between electrodes
3. Decrease distance between electrodes

$$C = \frac{\epsilon A}{d} \tag{1.5}$$

1.1.1 Increasing Electrode Area

Increasing electrode area is a subject well documented. There are several methods of increasing electrode area and all are equally clever in their approaches. The first that is discussed in detail, in [5] as well as [6], is using three dimensional capacitors utilizing not only plates stacked on top of one another but also those adjacent to each other. In [5], a method of using vertical parallel plates is discussed. This method uses metal plates in a parallel fashion by stacking metal levels. Vertical parallel plates are also discussed in [6].

Figure 1.1 from [6] shows in more detail what is suggested, using multiple metal layers with oxide between them as a dielectric, in a Metal Insulator Metal (MIM) configuration. These parallel plates stacked vertically are wired in parallel to effectively double the electrode area.

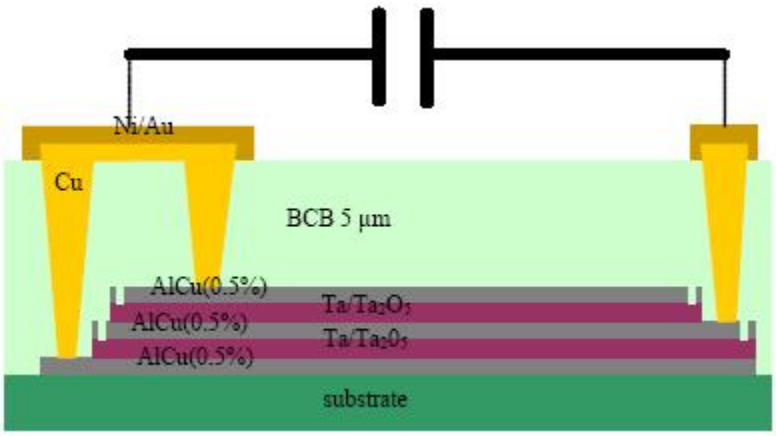

Figure 1.1: Architecture of a double stacked MIM capacitor

Another means of making three dimensional capacitors is discussed in [7]. This method uses the sides of interdigitated metal lines and interlayer vias maximize capacitor density. Figure 1.2 shows a clear illustration of the three dimensional capacitor in [7].

The authors of [7] claim capacitive densities of $2.18\frac{fF}{\mu m^2}$ while the authors of [6] claim densities of $30\frac{fF}{\mu m^2}$.

In [8], yet another method of increasing capacitance is discussed. This method utilizes deep trenches etched into the silicon to create capacitors. Locally doped substrate provides a connection to the bottom electrode. Chemical Vapor Deposition (CVD) is used to deposit a nitride or oxide to serve as the dielectric and finally the pores are filled in with poly-silicon to complete the top electrode. Aluminum is used as an interconnect for the capacitor. Figure 1.3 shows a detailed drawing of the high density trench capacitors. The authors have found

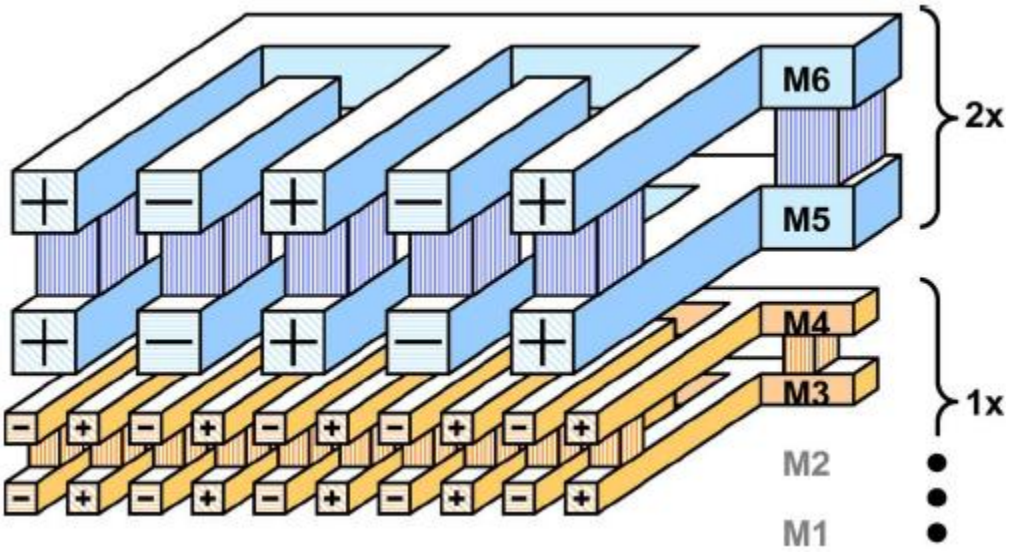

Figure 1.2: VPP capacitor layout diagram.

that using trenches to make high density capacitors can yield densities of $\approx 25\frac{fF}{\mu m^2}$. Not only do the trenches serve to increase the surface area, but the paper also suggests using a separate die to include the passives for a circuit. Vias are etched through the passive die to form the interconnects. Figure 1.4 shows a detailed drawing of the proposed configuration. The separate die integration platform alleviates some of the physical size restraints that are put on passive components.

With capacitive densities of $2.18\frac{fF}{\mu m^2}$, $25\frac{fF}{\mu m^2}$, and $30\frac{fF}{\mu m^2}$ the resistance needed for an RC time constant of $1mS$ would be decreased significantly and thus the area would also. Equation (1.6) gives the area needed for passive resistors with capacitive densities of $2.18\frac{fF}{\mu m^2}$, $25\frac{fF}{\mu m^2}$, and $30\frac{fF}{\mu m^2}$ respectfully. Unfortunately, with complex techniques for constructing these three dimensional structures the cost of processing increases, which may make these methods impractical.

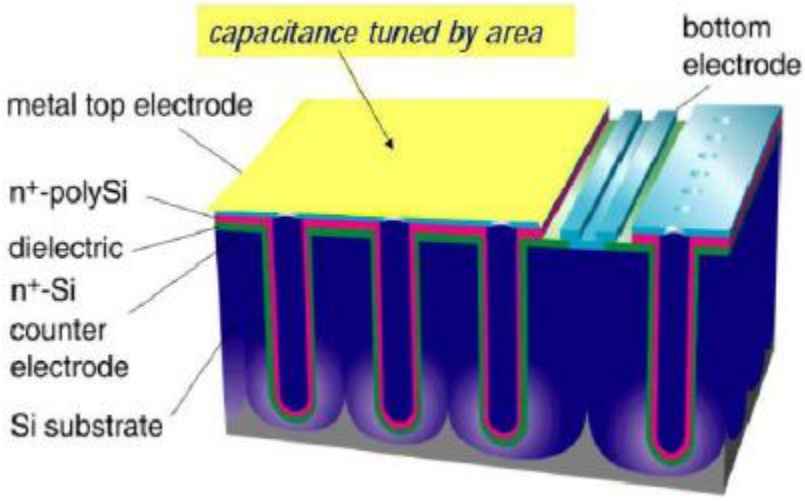

Figure 1.3: High Density Trench Capacitor

$$
\begin{aligned}
Resistor\ Area &= \frac{1}{2\pi \cdot 1000 \cdot 2.18e^{-12}} \cdot \frac{1\mu m^2}{1000\Omega} \approx 73000\mu m^2 \\
Resistor\ Area &= \frac{1}{2\pi \cdot 1000 \cdot 25e^{-12}} \cdot \frac{1\mu m^2}{1000\Omega} \approx 6400\mu m^2 \qquad (1.6) \\
Resistor\ Area &= \frac{1}{2\pi \cdot 1000 \cdot 30e^{-12}} \cdot \frac{1\mu m^2}{1000\Omega} \approx 5300\mu m^2
\end{aligned}
$$

1.1.2 Increasing the Permativity of the Dielectric

Increasing capacitance, by means of a higher permativity dielectric, is as easy as using a different material between the electrodes. This method of increasing capacitance is discussed in [9], [20], and [14]. The authors in [9] suggest that using Hafnium Oxide (HfOx) or Tantalum Oxide (TaOx) capacitor densities of $5\frac{fF}{\mu m^2}$ can be achieved. While the authors of

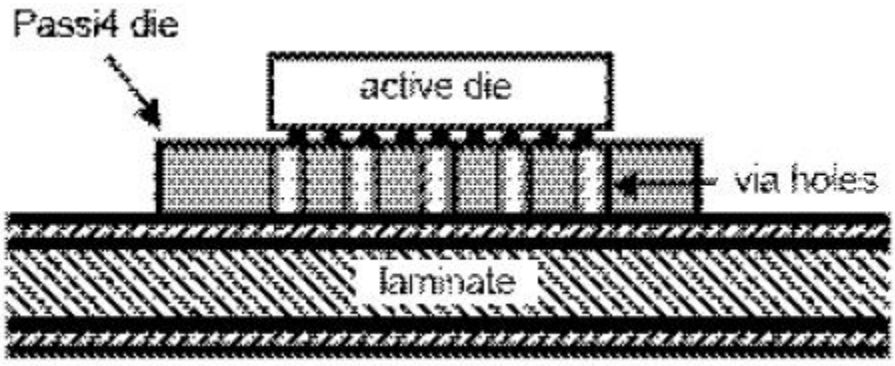

Figure 1.4: Separate Die Integration Platform

[20] suggest that by using Aluminum Oxide (Al_2O_3) as a dielectric the capacitive density can be increased to $\approx 10\frac{fF}{\mu m^2}$. However, the most impressive is in [14], where the authors claim that they have developed a capacitor film deposited on a silicon substrate that has a dielectric constant of 1000 which is roughly 250 times higher than SiO_2 and would yield a density of $\approx 250\frac{fF}{\mu m^2}$. As impressive as these numbers seem, the fact is that they do not make up for the orders of magnitude that must be overcome in order to have an achievable on-chip passive resistor. With capacitive densities of $5\frac{fF}{\mu m^2}$, $10\frac{fF}{\mu m^2}$, and $250\frac{fF}{\mu m^2}$ this method can also achieve a significant reduction in resistance needed for a $1mS$ RC time constant. Equation (1.7) gives the area needed for a passive resistor with $1000\frac{\Omega}{\mu m^2}$. The special techniques for achieving these densities may not be cost effective enough for use in a low cost application.

$$\begin{aligned} Resistor\ Area &= \frac{1}{2\pi \cdot 1000 \cdot 5e^{-12}} \cdot \frac{1\mu m^2}{1000\Omega} \approx 32000\mu m^2 \\ Resistor\ Area &= \frac{1}{2\pi \cdot 1000 \cdot 10e^{-12}} \cdot \frac{1\mu m^2}{1000\Omega} \approx 16000\mu m^2 \end{aligned} \tag{1.7}$$

$$Resistor\ Area \quad = \quad \frac{1}{2\pi \cdot 1000 \cdot 250e^{-12}} \cdot \frac{1\mu m^2}{1000\Omega} \approx 636\mu m^2$$

1.1.3 Decreasing the Distance Between the Electrodes

In an attempt to increase capacitive density by decreasing the thickness of the dielectric, undesirable traits form in the capacitors. As the dielectric becomes thinner, the leakage current of the capacitor increases largely, because of direct tunneling through the dielectric [9]. This increase of leakage current no longer meets the requirement for the voltage levels that will be used and thus other solutions to the problem must be found.

1.2 Active Resistors

Although significant strides have been made in increasing capacitive densities, these are still not large enough to offset the need for very large value resistors. Since traditional poly-silicon and diffused resistors can not meet the performance needs, different techniques have been used to synthetically produce active devices that fulfill the need of a large value resistor. These active resistors yield many advantages over traditional resistors. First, although they do introduce noise into the system, it is not caused directly by the value of resistance that they represent. Second, they take up much less silicon area versus regular resistors. Finally, they are not a fixed resistance value, so they can be tuned to compensate for variations in capacitance values in the circuit.

The simplest of these active resistors used for tuning and consists of using a MOS transistor in parallel with a regular poly-silicon resistor. This allows the parallel combination of the resistors to be varied based on the value of the resistance of the transistor. However,

this will only allow for a resistance value from $400\Omega - 1600\Omega$ which is quite small but shows how easily it is to implement a tunable resistor [10]. There are several different approaches to making an active resistor. In [12], a highly linear CMOS floating gate resistor is proposed. This active resistor is a single MOS transistor with programming circuitry around it. It utilizes a voltage feedback to the well in order to overcome the nonlinear nature MOS transistor. This provides tunable resistance values from $\approx 1400k\Omega - 660k\Omega$.

Another approach of creating high value controlled floating resistors is to use two current controlled conveyors. The current is transferred from port X to port Z in the current conveyor. The system uses two current conveyors coupled together with current divider circuits in order to create the proper resistance. The authors suggest that an active resistor with this configuration can create resistances from $93\Omega - 60k\Omega$ with a bandwidth of $100MHz$ [17]. Although these examples do drastically increase resistance values, the ability to make active resistors with values on the order of megaohms to overcome the limitations of on-chip capacitors, is still not achievable by these methods.

Described in this thesis is a linear active CMOS resistor, proposed by Dr. Bogdan M. Wilamowski, for use in a control system for a MEMS gyroscope. The Active CMOS Resistor(ACR) can achieve values up to $600M\Omega$ with a bandwidth over $100KHz$. The ACR uses $\pm 2.5V$ supply rails and has an input voltage swing of $\pm 1.5V$ and an output voltage swing of $\pm 2V$. It can serve as a drop in replacement for a passive resistor in most applications as long as the input and output voltage and bandwidth of the system are within its range.

Chapter 2

Design and Simulation of Active CMOS Resistor(ACR)

2.1 Design of CMOS Resistor

The described ACR is implemented using the AMIS C5 process. Being that this is a $5V$ process, and the desired use for the resistor is in a PID controller working with positive and negative error voltages the resistor uses $\pm 2.5V$ supply rails for operation. The input voltage swing is $\pm 1.5V$ and the output voltage swing is $\pm 2V$.

The ACR can be viewed as two separate yet interrelated parts, the input amplifier stage and output stage. The input amplifier stage feeds the output stage while utilizing the output for feedback to remain balanced. Figure 2.1 is a schematic of the ACR showing the relationship between the input and output stages. The small signal model for the ACR is given in Figure 2.2.

2.1.1 Input Stage

The input stage is a five transistor differential amplifier. There is a simple long tailed differential pair with a NMOS current mirror providing bias current and a PMOS current mirror serving as the load. For ease of calculations the source voltage of the differential pair transistors, M_1 and M_2, is assumed to be constant, as well as the drain current of the bias current mirror transistor I_{D12}, I_{S1}.

The purpose of the input amplifier stage is to translate the input voltage to the output stage in order to adjust the output current by using feedback from the output stage. It

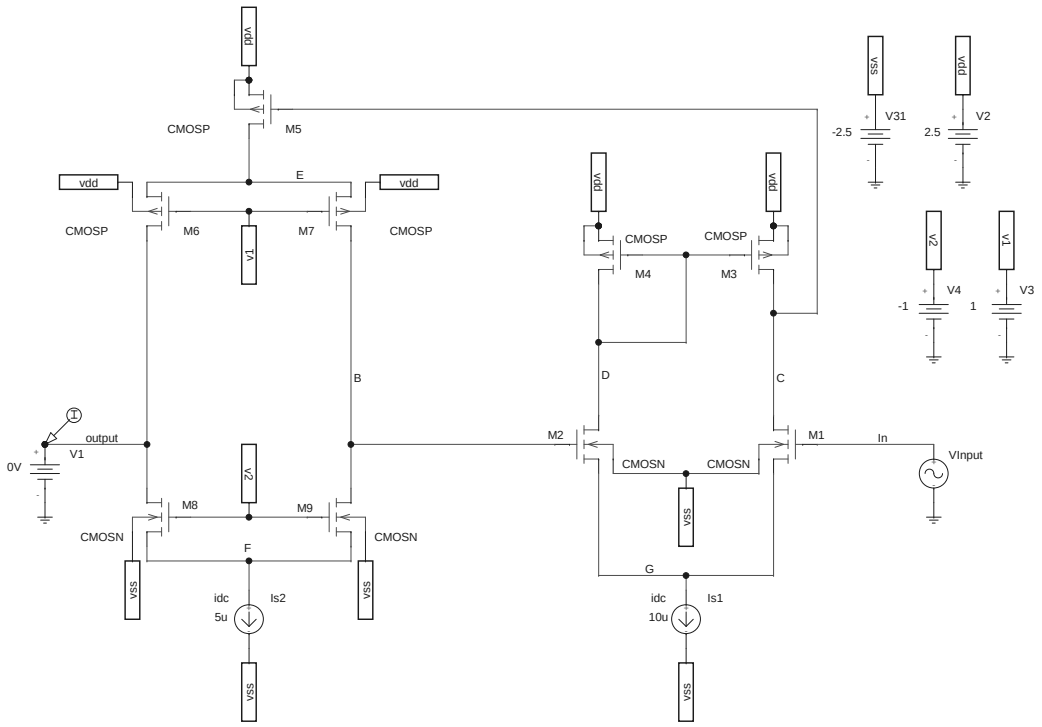

Figure 2.1: Schematic of ACR

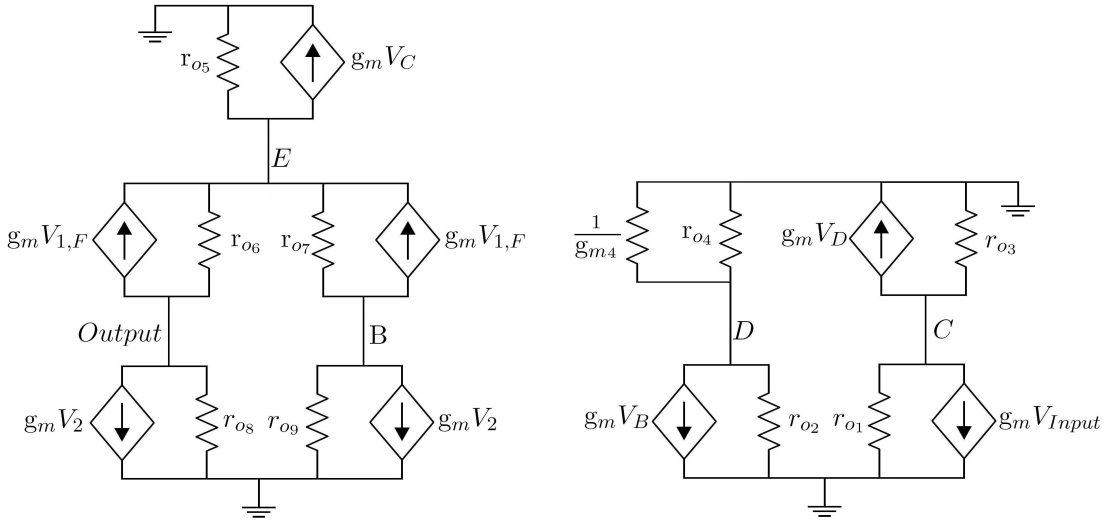

Figure 2.2: Small Signal Model for ACR

takes the difference between the input and feedback voltages, and applies gain. The gain of the input stage is found using equation (2.1).

$$A = g_{m1}(r_{o1}||r_{o3}) = \frac{\mu_{f1}}{1 + \frac{r_{o1}}{r_{o3}}} \cong \frac{\mu_{f1}}{2} \tag{2.1}$$

Where,

$$\frac{\mu_{f1}}{2} = \frac{g_{m1} \cdot r_{o1}}{2} \tag{2.2}$$

$$g_{m1} = \frac{2I_{D1}}{V_{GS} - V_{TN}} \cong \sqrt{2K_n I_D} \tag{2.3}$$

$$r_{o1} = \frac{1 + \lambda V_{DS}}{\lambda I_D} \cong \frac{1}{\lambda I_D} \tag{2.4}$$

The voltage change of the output of the amplifier stage, node C, can be written as

$$\begin{aligned} \Delta V_C &= \Delta(V_{Input} - V_B) \cdot A \\ &= \Delta(V_{Input} - V_B) \cdot \frac{\sqrt{2K_n I_{D1}}}{2\lambda I_{D1}} \\ &= \Delta(V_{Input} - V_B) \cdot \frac{\sqrt{K_n}}{\lambda\sqrt{2I_{D1}}} \\ &= \Delta(V_{Input} - V_B) \cdot \frac{\sqrt{K_n}}{\lambda\sqrt{I_{S1}}} \end{aligned} \tag{2.5}$$

2.1.2 Output Stage

The output current is controlled by the difference between the voltage on node B and the voltage on the output node. When node B is lower than the output node the V_{DS} of M_8 is larger than the V_{DS} for M_9, so the drain current of M_8 is larger than the drain current for M_9. Also, the V_{DS} of M_7 is larger than the V_{DS} for M_6, so the drain current of M_7 is larger than the drain current for M_6. If $I_{D8} > I_{D7} > I_{D6}$, then I_{Output} will be negative. Likewise, when node B is greater than the output node the V_{DS} of M_8 is smaller than the V_{DS} for M_9, so the drain current of M_8 is smaller than the drain current for M_9. Also, the V_{DS} of M_7 is smaller than the V_{DS} of M_6, so the drain current of M_7 is smaller than the drain current for M_6. If $I_{D8} < I_{D7} < I_{D6}$, then I_{Output} will be positive.

The output stage contains six transistors. The top PMOS, M_5, translates the difference between the input and feedback voltages in to a current that keeps the input amplifier stage in balance. Since M_5 has to source twice the current as the others in this stage, it has a

width to length ratio that is twice that of the other transistors in order to accommodate the extra current. The biasing current is provided by a NMOS current mirror, M_{10}. For ease of calculations the source voltage of the source of M_8 and M_9 will be considered constant, as well as, the bias current I_{D10}, I_{S2}.

The output current is the difference between I_{D5} and I_{S2}.

$$I_{Output} = I_{S2} - I_{D5} \tag{2.6}$$

The change in the drain current of M_5, ΔI_{D5}, can be written as

$$\Delta I_{D5} = \Delta V_C \cdot g_{m5} \tag{2.7}$$

where,

$$g_{m5} = \sqrt{2K_p I_D} \tag{2.8}$$

Substituting equations (2.5) and (2.8) into equation (2.7) and making $I_{S1} = 2 \cdot I_{S2}$ yields

$$\begin{aligned} \alpha = \Delta I_{D5} &= \Delta(V_{Input} - V_B)\frac{\sqrt{K_n}}{\lambda\sqrt{I_{S1}}} \cdot \sqrt{2K_p I_D} \\ &= \Delta(V_{Input} - V_B)\frac{\sqrt{2K_1 K_5 I_{S2}}}{\lambda\sqrt{I_{S1}}} \\ &= \Delta(V_{Input} - V_B)\frac{\sqrt{K_1 K_5}}{\lambda} \end{aligned} \tag{2.9}$$

Equation (2.9) is not dependent on the bias current, I_{S2}, so it is considered a constant. The drain current of M_5 can also be thought of as

$$I_{D5} = I_{S2} + \alpha I_{S2} \tag{2.10}$$

where αI_{S2} is the output current and α is defined as equation (2.9). The equivalent resistance of the ACR can be written as

$$R = \frac{V_{Input} - V_{Output}}{I_{Output}} \tag{2.11}$$

Setting $V_{Input} - V_{Output}$ equal to one and substituting for I_{Output} yields

$$R = \frac{1}{\alpha I_{S2}} \tag{2.12}$$

Equation (2.12) shows that the resistance value is inversely proportional to the tuning current I_{S2}. With this current, the resistance can be tuned to achieve the value that is desired.

2.2 DC Analysis

A DC analysis was performed on the ACR to determine the maximum input and output voltage swings and to determine resistance value for any given tuning current. The DC analysis was performed using $\pm 2.5V$ supply rails, the input voltage was fixed at zero volts with an voltage source, and the current through the output voltage source was plotted.

Figure 2.3 shows the output current as the output voltage is swept from $\pm 500mV$ and the tuning current is stepped from $1\mu A$ to $5\mu A$ in steps of $1\mu A$. As shown in Figure 2.3, the output current is positive when the input voltage is higher than the output voltage and negative when it is lower than the output voltage, passing through zero amperes when the input and output voltages are equal.

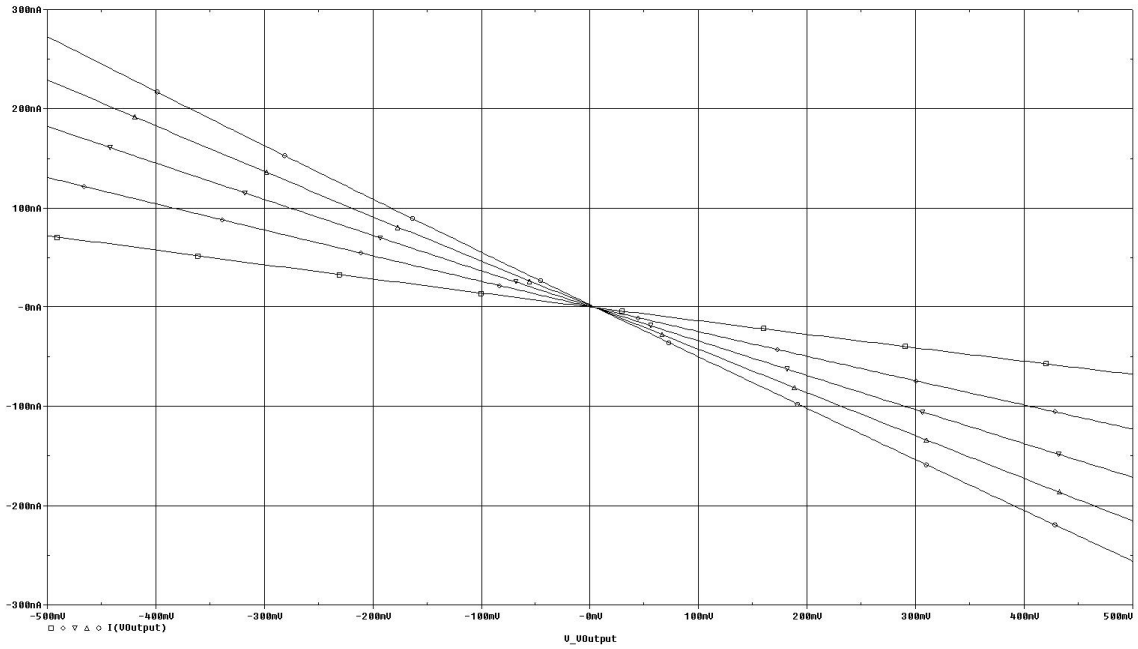

Figure 2.3: Output Current vs Output Voltage

Figure 2.4 shows a plot of $R = \frac{V_{Input} - V_{Output}}{I_{Output}}$. The plot shows the resistance value as a function of voltage difference and tuning current. The resistance is flat across the range.

The most important information can be gathered from a plot of resistance versus the tuning current. A sweep of the tuning current shows how the resistance changes with tuning current directly. The input voltage was set at a constant $250mV$, while the output voltage was set at a constant $-250mV$. With these two voltages fixed, the tuning current of the ACR was swept from $10nA$ to $10\mu A$. The same calculation $R = \frac{V_{Input} - V_{Output}}{I_{Output}}$ was performed and

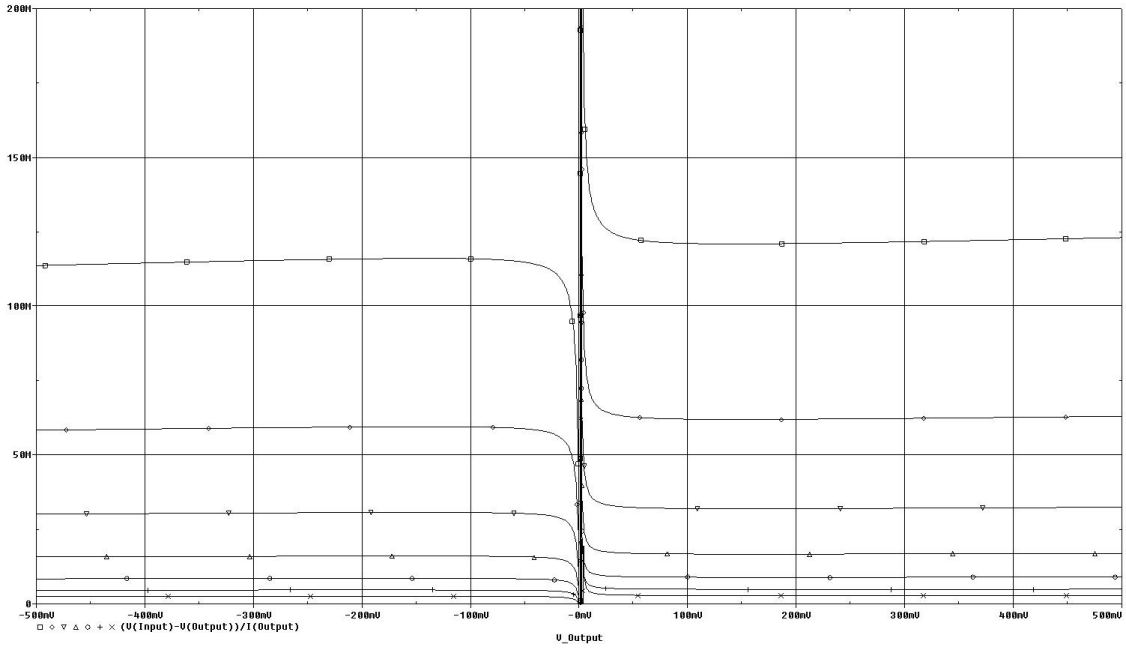

Figure 2.4: Resistance vs Output Voltage

plotted. The a curve was fit to the data from Figure 2.5 in order to find an equation that describes the relationship between the tuning current and the resistance. Equation (2.13) can be used in order to find the proper tuning current for a chosen resistance.

$$\begin{aligned} R &= \frac{25.774}{(I_{S2})^{0.909}} \\ I_{S2} &= \left(\frac{25.774}{R}\right)^{\left(\frac{1}{0.909}\right)} \end{aligned} \tag{2.13}$$

The curve fit equation (2.13) shows that the resistance is inversely proportional to the tuning current and fairly linear through the range.

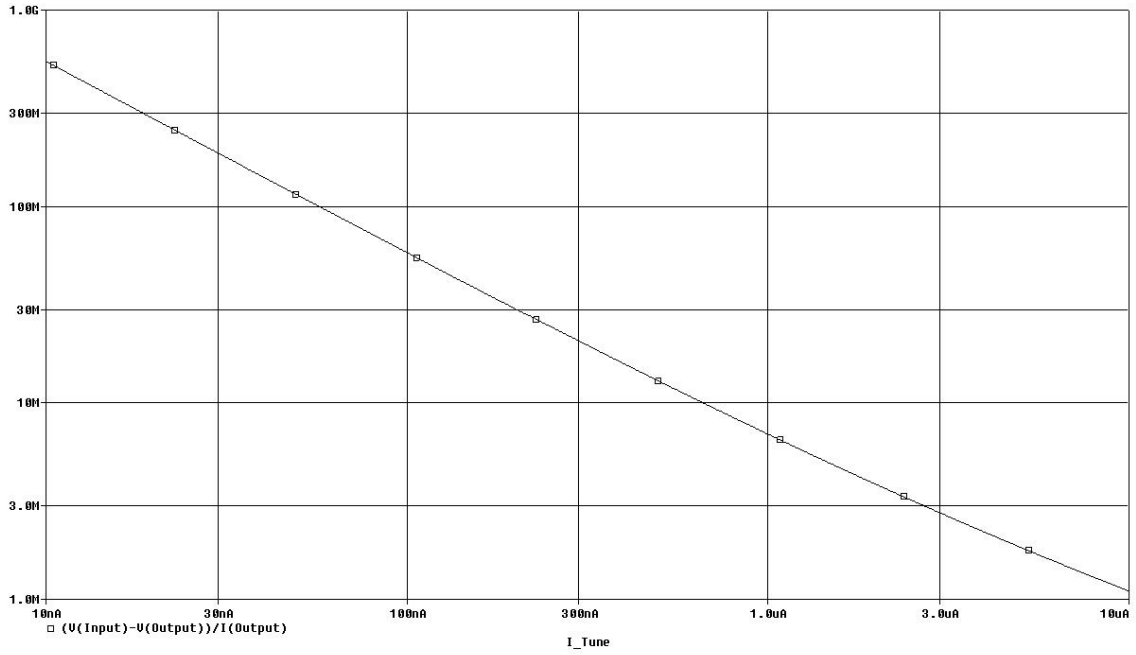

Figure 2.5: Resistance vs Tuning current

2.3 AC Analysis

The AC analysis will show the frequency response of the ACR and show the operational bandwidth. An AC voltage source, swept from $10Hz$ to $10MHz$, drives the input of the circuit while the output voltage is kept at zero volts. The tuning current is stepped from $50nA$ to $3.2\mu A$ doubling with each step. The current through the output voltage source is plotted versus the frequency of the input signal. Figure 2.6 shows how tuning current effects the bandwidth of the circuit. As the frequency increases so does the output current, which effectively lowers the resistance of the circuit. The bandwidth of the circuit is $200KHz$ with a tuning current of $50nA$ and $10MHz$ with a tuning current of $3.2\mu A$. The phase of the output current is plotted in Figure 2.7. In the operational bandwidth of the ACR the

phase is 0°. The resistance versus frequency is plotted in Figure 2.8. It is clear that the bandwidth of the resistor is a function of tuning current.

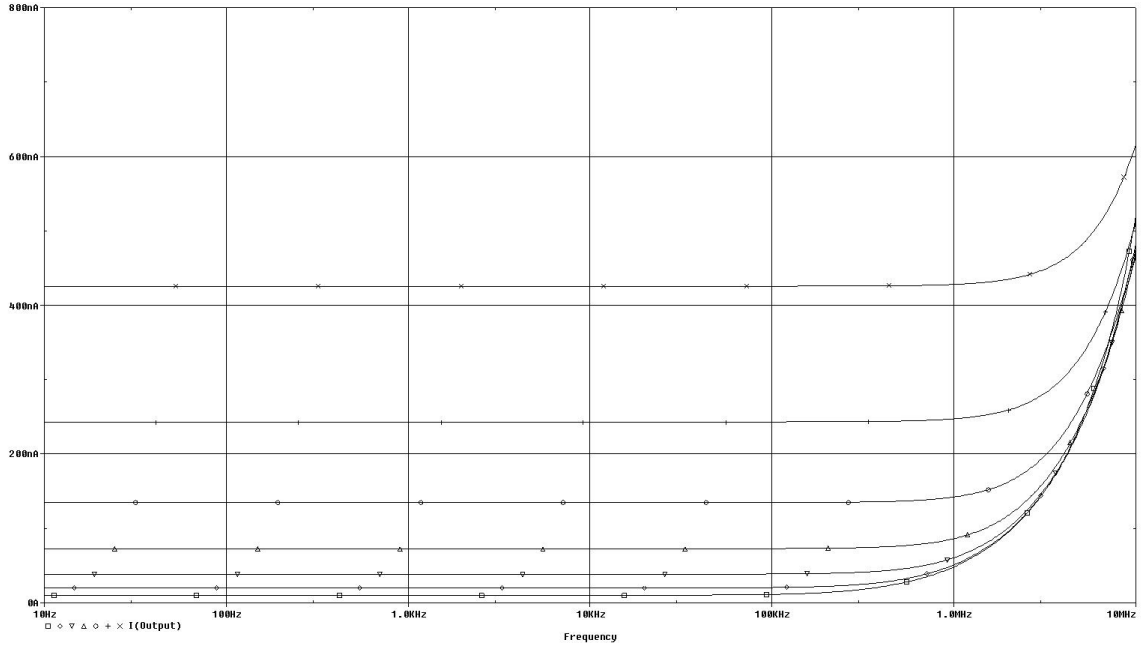

Figure 2.6: Output Current vs Input Voltage Frequency

2.4 Transient Analysis

A transient analysis was performed on the circuit to determine its real time response to an input. For the simulation, a sinusoidal voltage source was used to drive the input of the circuit. This sinusoidal signal was run at a frequency well below that of the bandwidth of the ACR, $3KHz$. The output of the circuit is held at zero volts and the output current through the output voltage source is plotted. The tuning current was stepped from $50nA$ and $3.2\mu A$ doubling with each step. Figure 2.9 how shows the current follows the sinusoidal input. Figure 2.10 shows the resistance of the circuit versus the sinusoidal input voltage.

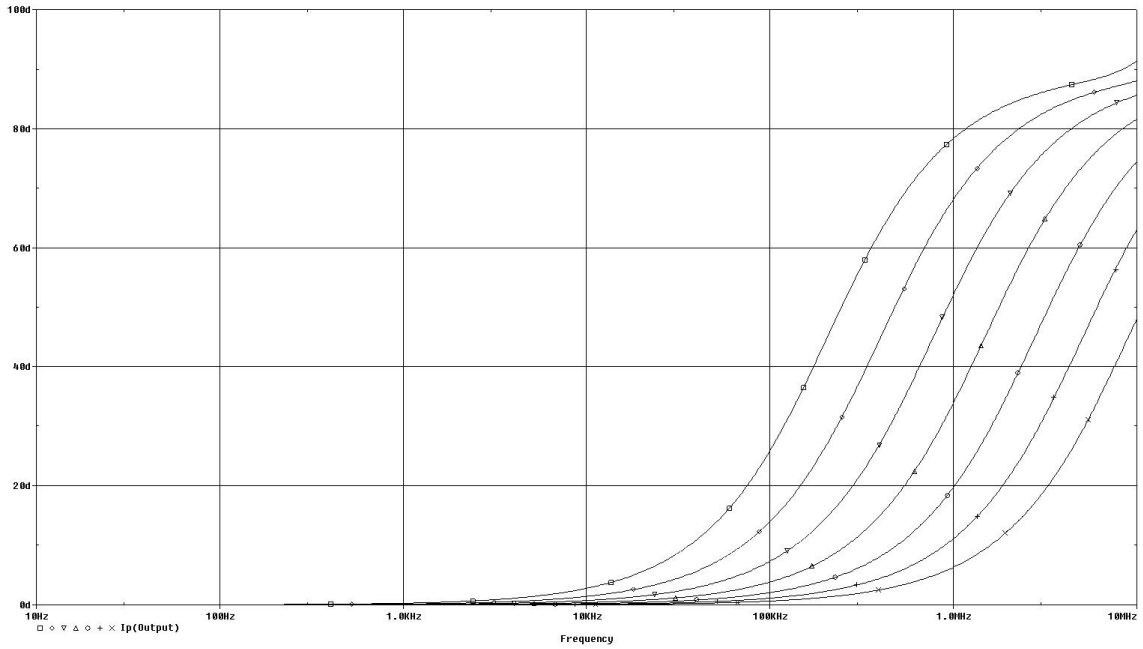

Figure 2.7: Phase of Output Current vs Input Voltage Frequency

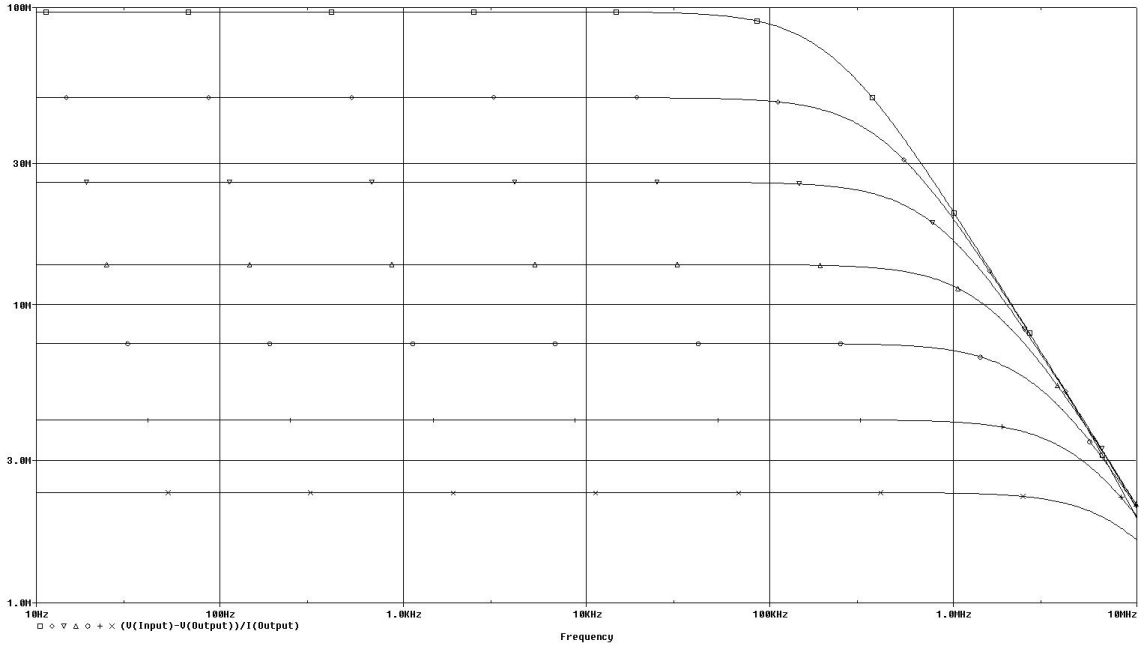

Figure 2.8: Resistance vs Input Frequency

As with the other simulations, the equivalent resistance increased as the tuning current decreased.

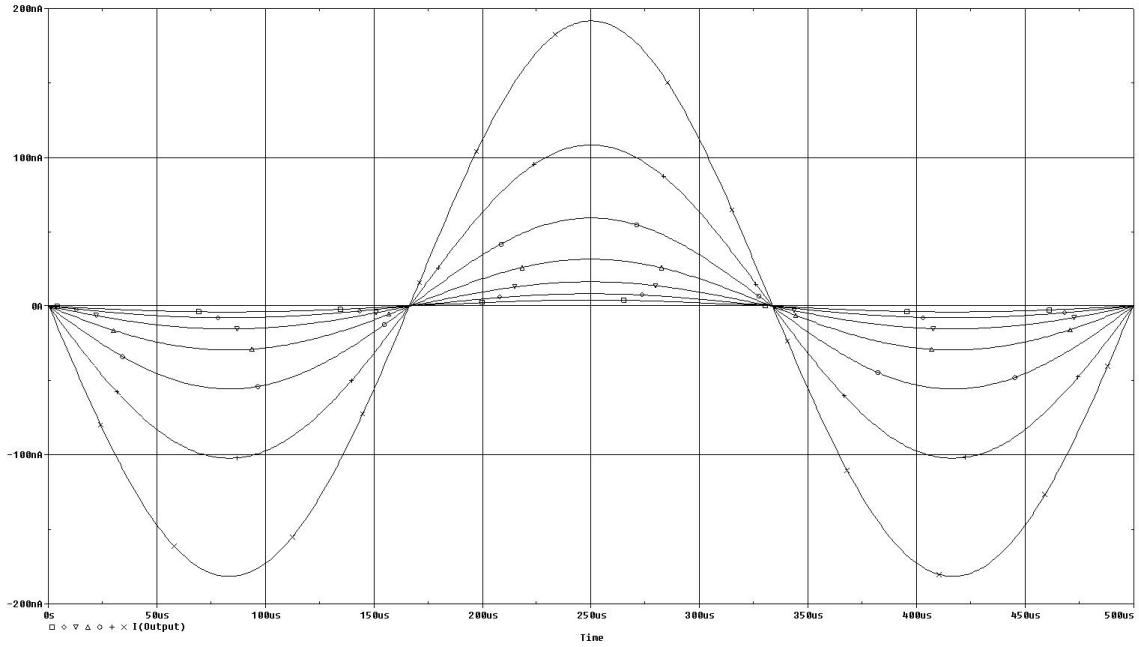

Figure 2.9: Output Current with Sinusoidal Input Voltage

2.5 Noise Analysis

Because of its unpredictable nature, noise is a main contributor to the inaccuracy of a sensor. The main source of noise in a MOSFET is thermal noise due to thermal agitation of electrons in the resistive channel [21]. Equation (2.14) gives the current noise of a MOSFET where $k = 1.38e^{-23}$, $T = 300$, and g_m is the transconductance of the transistor.

$$\overline{i^2} = \frac{8}{3} \cdot k \cdot T \cdot g_m \frac{A^2}{Hz} \tag{2.14}$$

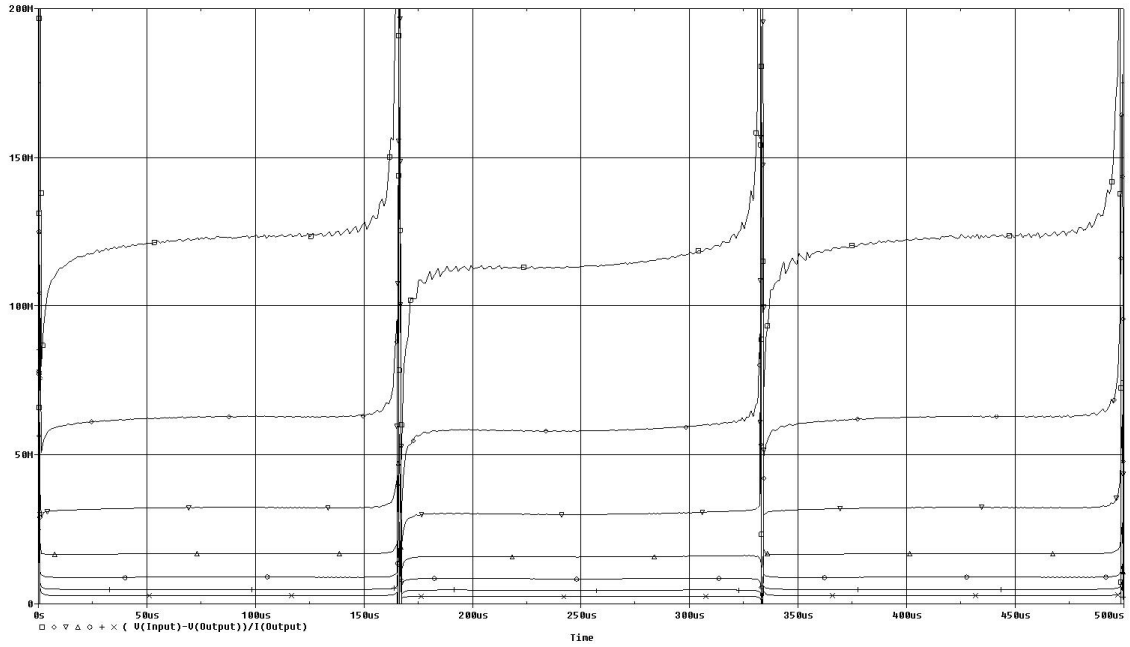

Figure 2.10: Resistance vs Sinusoidal Input Voltage

In order to obtain the voltage noise, $\overline{V^2}$, equation (2.14) is multiplied by the output resistance of the transistor, r_o.

$$\overline{V^2} = \frac{8}{3} \cdot k \cdot T \cdot g_m \cdot r_o^2 \frac{V^2}{Hz} \tag{2.15}$$

Equation (2.15) clearly shows the relationship between the voltage noise of a MOSFET and its output resistance. The output resistance is proportional to the drain current of the transistor, therefore, the noise is proportional to the tuning current of the ACR.

A noise analysis was performed on the ACR in SPICE. In order to obtain the voltage noise, the ACR is connected to a grounded passive resistor of equal value. The noise contribution of the passive resistor will be subtracted off the noise voltage to yield that

which is contributed by the ACR. Table 2.1 gives the noise contributions of each transistor to the total output voltage noise. At $167.778M\Omega$ the total output noise for the ACR is $13.8\frac{\mu V}{\sqrt{Hz}}$. The main contributors to the total output noise are the four output transistors M_6, M_7, M_8, and M_9, due to the fact that any fluctuation of their output current will directly affect the output current and output voltage.

The square root of equation (2.15) must be taken in order to compare the noise result of the simulation to the noise calculation of equation (2.16). Comparing the simulation results for the thermal noise of an ACR tuned to $167.778M\Omega$, $13.8\frac{\mu V}{\sqrt{Hz}}$, and a passive resistor with a value of $167.778M\Omega$, $1.667\frac{\mu V}{\sqrt{Hz}}$, the ACR has approximately and a factor of 8 greater noise.

$$V_t = \sqrt{4 \cdot k \cdot T \cdot R} = \sqrt{4 \cdot 1.38 \cdot 10^{-23} \cdot 300 \cdot 167.778 \cdot 10^6} = \frac{1.667\mu V}{\sqrt{Hz}} \tag{2.16}$$

	M1	M2	M3	M4	M5	M6
ID	5.773E-16	5.658E-16	4.987E-16	4.744E-16	5.964E-19	4.372E-11
	M7	M8	M9	M10	M11	M12
ID	4.373E-11	5.147E-11	5.146E-11	1.437E-19	1.519E-18	6.497E-20
Total	1.904E-10 $\frac{V^2}{Hz}$					
Total	13.8 $\frac{\mu V}{\sqrt{Hz}}$					

Table 2.1: Noise Sources of ACR

Chapter 3

Resistor Substitution

The beauty behind the ACR circuit is its simplicity and the way it can replace a passive resistor in complex applications. Because the output node is allowed to float to the necessary voltage, the circuit performs just as a high value resistor would as it interacts with other passive components. All the previous simulations were performed with specified output and input voltages. However, to truly gage whether the circuit will perform like a passive resistor, the circuit must be put in actual applications that allow the output to drive something other than an ideal voltage source.

3.1 Single Pole Filter

The simplest application for the resistor circuit is a single pole low-pass or high-pass filter. These filters involve one resistor either driving or being driven by a capacitor. As stated before the main challenge with using on-chip capacitors for filtering functions is their inherently low values. A capacitor with just one picofarad of capacitance has a significant footprint and is as large as the proposed ACR itself. The maximum on-chip capacitance that will be used in any of these applications will be approximately one picofarad.

3.1.1 Low-Pass Filter

Figure 3.1 shows the configuration of a simple one pole RC low-pass filter. The input of the ACR is driven by a sinusoidal voltage source while the output node of the ACR serves

as the output of the filter. A one picofarad grounded capacitor is connected to the output node to form the filter. The transfer function for this single pole low-pass filter is

$$H(s) = \frac{1}{sRC + 1} \tag{3.1}$$

with the pole located at

$$f_c = \frac{1}{2\pi RC} \tag{3.2}$$

The frequency response of the low-pass filter can seen in Figures 3.2 and 3.3. The tuning current is stepped from $50nA$ to $3.2\mu A$ doubling with each step. The plot of the magnitude starts at $0dB$ and continues flat until reaching the pole of the filter where it decreases with a slop of $-20dB$ per decade, while the phase starts at 0° in the passband and turns down toward -90° beyond the pole. It is clearly shown in the plots that as the tuning current of the ACR is increased the resistance is decreased, thereby increasing the frequency of the filter's pole. The plots also show that the filter behaves just as a passive resistor low-pass filter would, which demonstrates the ease at which a tunable single pole low-pass filter can be implemented on chip. Because there is very little offset, this configuration can easily be daisy chained in order to form higher order low-pass filters.

From Figure 3.2, the pole of the low-pass can be found. For the middle trace, corresponding to a tuning current of $400nA$, the pole of the low-pass filter, read from the plot,

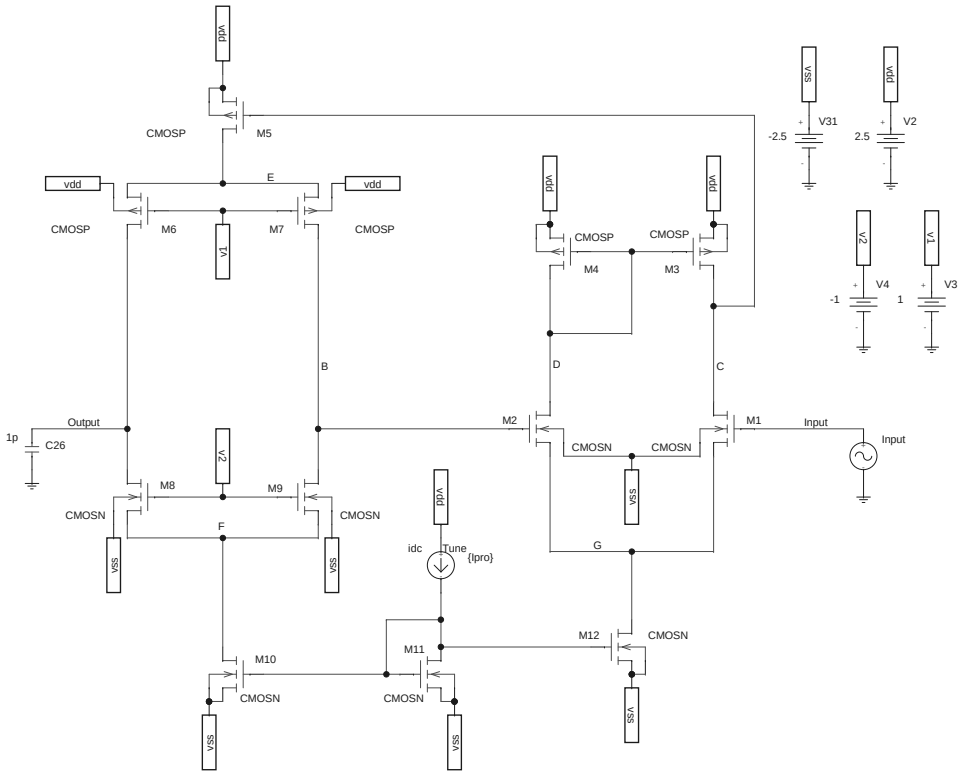

Figure 3.1: Single Pole Low-Pass Filter Configuration

is located at $9723Hz$. Substituting $9723Hz$ for the cutoff frequency and one picofarad for C in equation 3.2 and solving for R yields equation (3.3).

$$R = \frac{1}{2 \cdot \pi \cdot 9723 \cdot 1e - 12} = 16,368,913.2\Omega \tag{3.3}$$

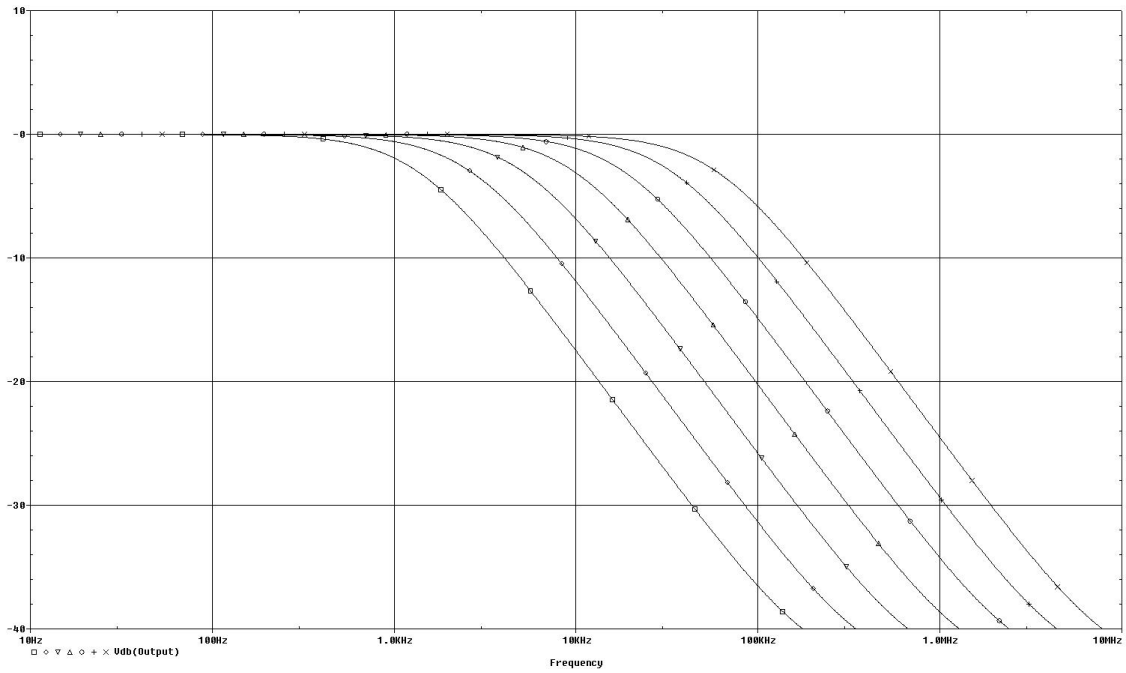

Figure 3.2: Low-Pass Filter Output Magnitude vs Frequency

To see how well the circuit will perform with an actual sinusoidal signal, a transient analysis was performed on the circuit in the low-pass filter configuration. The input is driven by a sine wave voltage source at the frequency that is the $-3dB$ point of the filter with a tuning current of $400nA$, $9723Hz$, to see if the filter will perform as it should, attenuating and phase shifting the signal more as the tuning current is decreased. The tuning current is stepped through the same range, $50nA$ to $3.2\mu A$ doubling with each step. Figure 3.4 is a

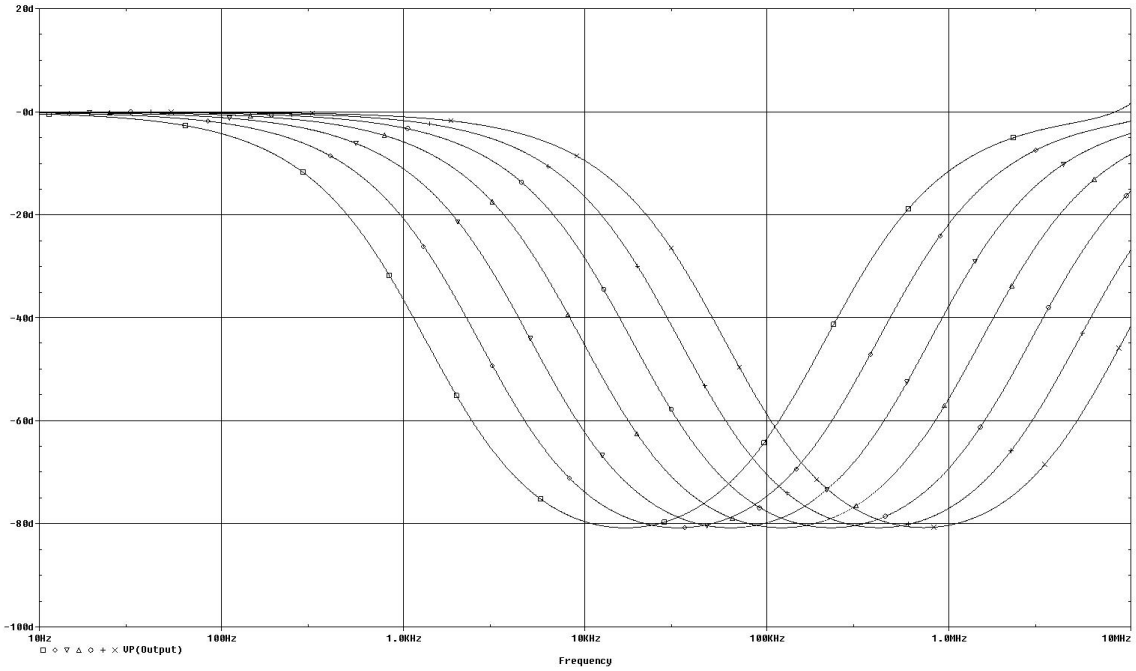

Figure 3.3: Low-Pass Filter Output Phase vs Frequency

plot of the output voltage of the filter with an input frequency of $9723Hz$ and magnitude of $1V$. Clearly from the plot it can be seen that the filter is functioning properly. If a closer look is taken at the filter tuned with its $f_c = 9723Hz$, Figure 3.5, the output is 70.7% of the input and is phase shifted 45° with a very small DC offset. These output results are very similar to a passive resistor filter with the same resistance value.

The total harmonic distortion is defined as the

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} V_n^2}}{V_1} \tag{3.4}$$

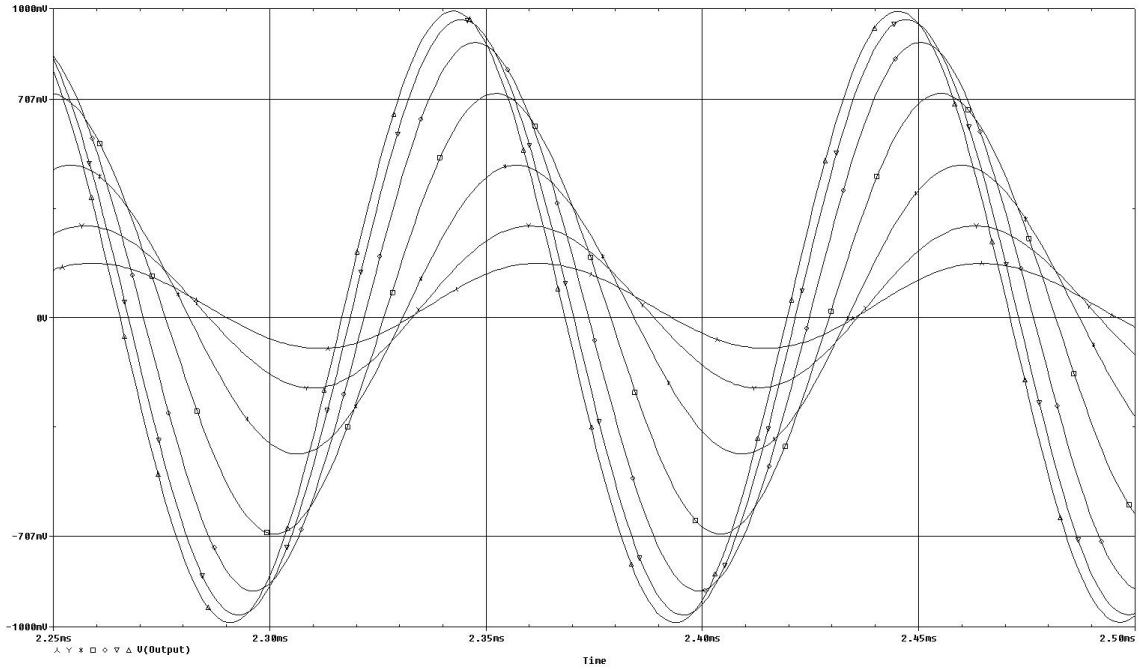

Figure 3.4: Low-Pass Filter Transient with Stepped Tuning Current

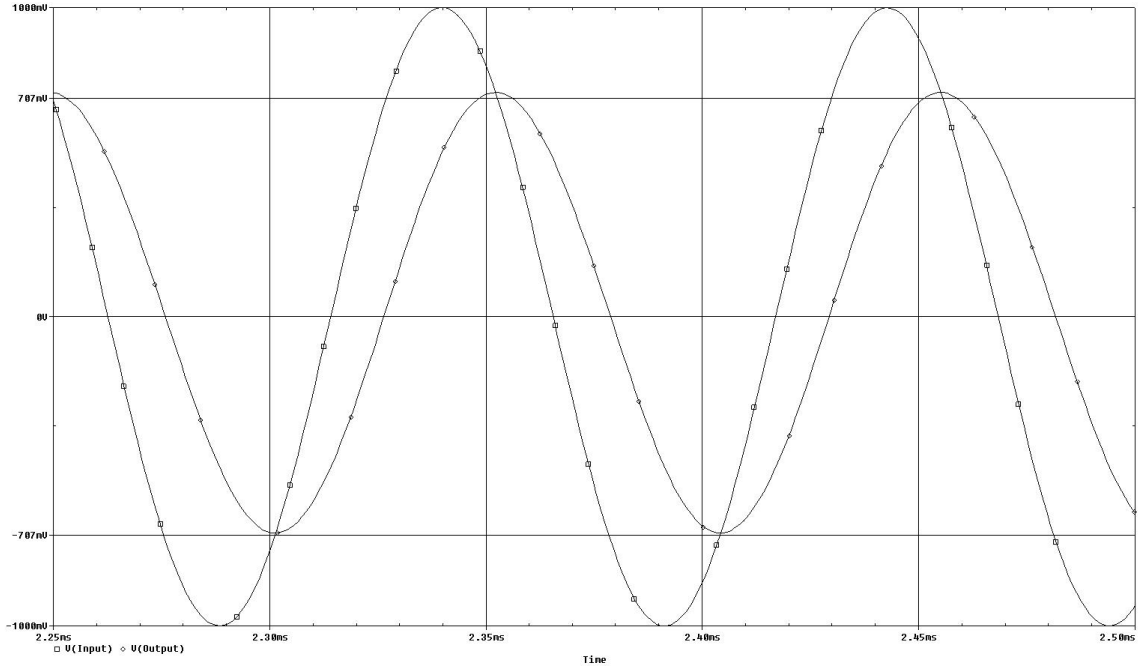

Figure 3.5: Low-Pass Filter With 9723 Hz Input Signal

Harmonic NO	Frequency (Hz)	Fourier Component	Normalized Component	Phase (deg)	Normalized Phase (deg)
1	9.72E3	2.48E-1	1.000	-7.71E1	0.00
2	1.95E4	1.59E-5	6.41E-5	-4.53E1	1.09E2
3	2.92E4	3.55E-5	1.43E-4	3.12E+1	2.63E2
4	3.89E4	1.38E-5	5.56E-5	-8.80E1	2.21E2
5	4.86E4	1.21E-5	4.89E-5	-1.38E2	2.48E2

Table 3.1: Total Harmonic Distortion Low-Pass Filter

3.1.2 High-Pass Filter

The other single pole filter that can be designed using this ACR is a single pole high-pass filter. Figure 3.6 shows the configuration of the single pole RC high-pass filter. The input of the ACR is grounded while the output is connected to a one picofarad capacitor. A sinusoidal voltage source drives the capacitor and the output of the ACR is the output of the filter. The transfer function of the filter is given in equation (3.5).

$$H(s) = \frac{sRC}{sRC + 1} \tag{3.5}$$

The pole of the filter is located at

$$f_c = \frac{1}{2\pi RC} \tag{3.6}$$

The frequency response of the high-pass filter is shown in Figures 3.7 and 3.8, as with the low-pass filter, the tuning current was stepped from $50nA$ to $3.2\mu A$ doubling with each step. The plot of the magnitude increases with a slop of $20dB$ per decade until reaching

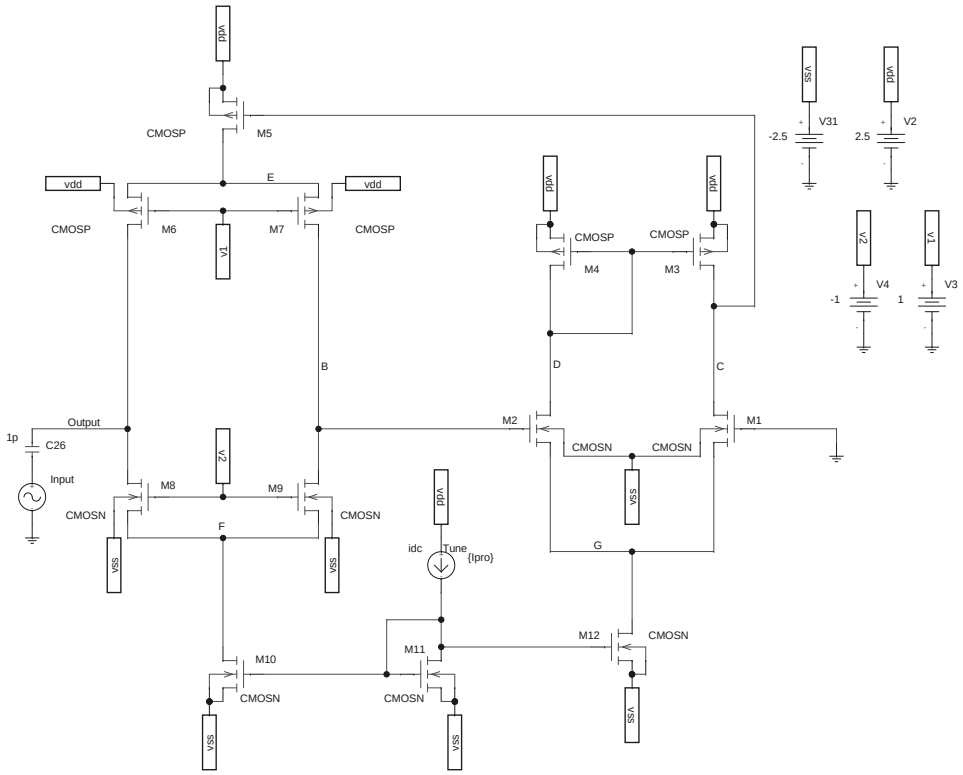

Figure 3.6: Single Pole High-Pass Filter Configuration

the pole of the filter and turning over to be flat, while the phase starts at 90° and goes down to 0° in the pass band of the filter. Figure 3.7 also clearly shows the pole of the filter moving toward dc as the tuning current decreases. The f_c of the high-pass filter with a tuning current of $400nA$ is $9723Hz$, and the phase at that point is 45°.

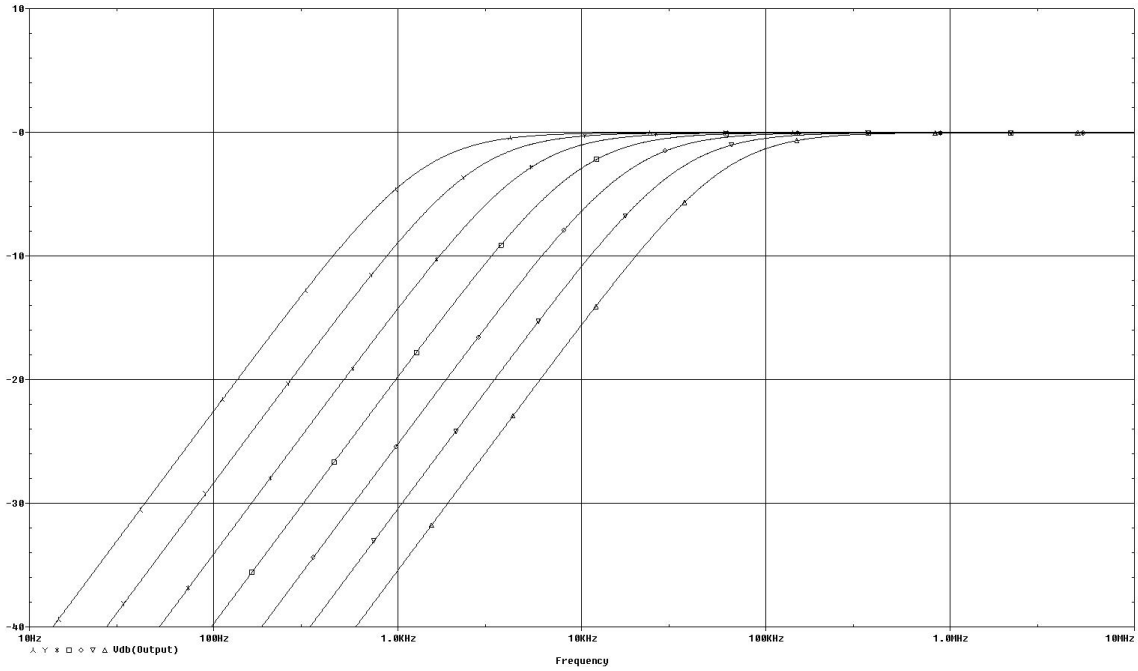

Figure 3.7: High-pass Filter Output Magnitude vs Frequency

Good performance in the time domain is the main objective, thus a transient analysis is performed to determine the performance of the filter with sinusoidal a sinusoidal input. The sinusoidal input voltage source drives the capacitor with a $1V$ sine wave at the $-3dB$ point of the filter which has a $400nA$ tuning current, $9723Hz$. Figure 3.9 shows the sinusoidal output of the filter as the tuning current is stepped from $50nA$ to $3.2\mu A$ doubling with each step. With each step it is clear there is more attenuation of the signal, as well as, a much larger phase shift.

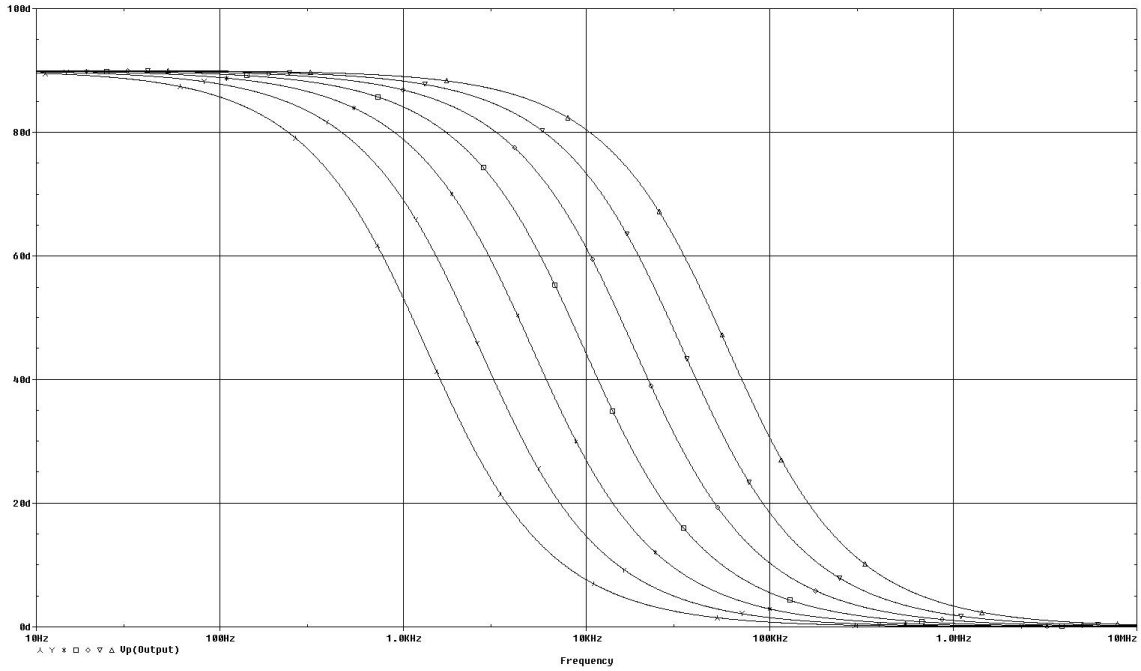

Figure 3.8: High-pass Filter Output Phase vs Frequency

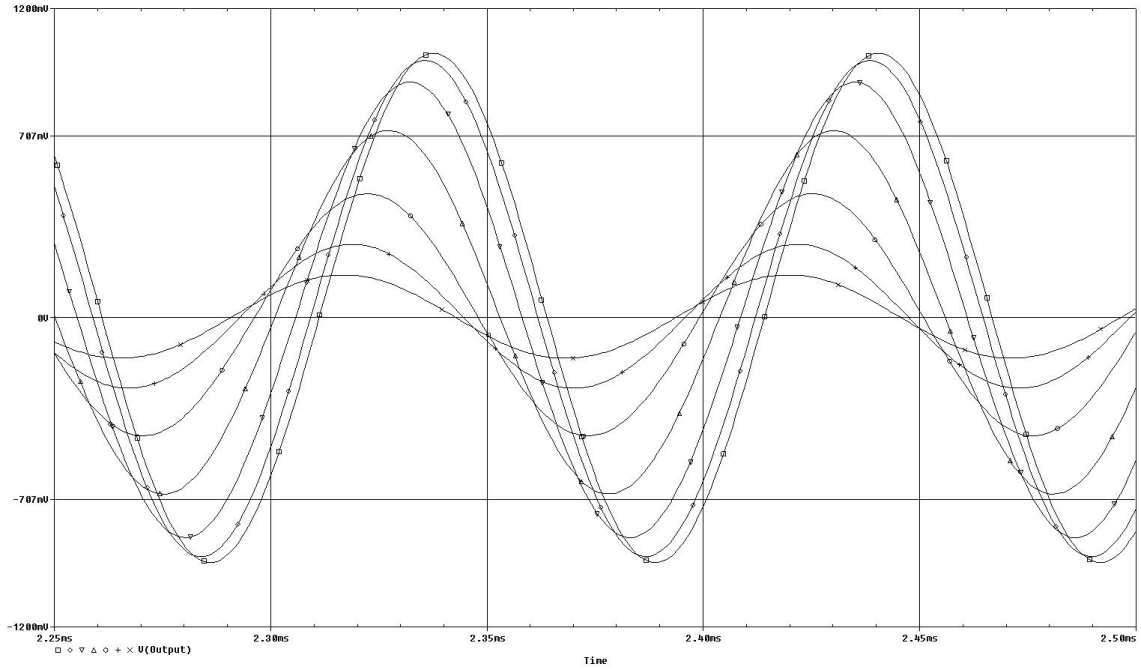

Figure 3.9: High-Pass Filter Transient with Stepped Tuning Current

To show in more detail the operation of the filter, the tuning current is set to $400nA$. The output voltage is shown in Figure 3.10. The output amplitude is only 70.7% of the input and phase shifted by 45° with a small dc offset. Just as it was predicted in the frequency plot, the time domain simulation of the circuit indicates that the ACR filter circuit performs similarly to a passive resistor filter circuit. As long as the input and output voltage ranges and frequencies are within the operating range of the ACR, it can replace a passive resistor and have still have a very similar performance.

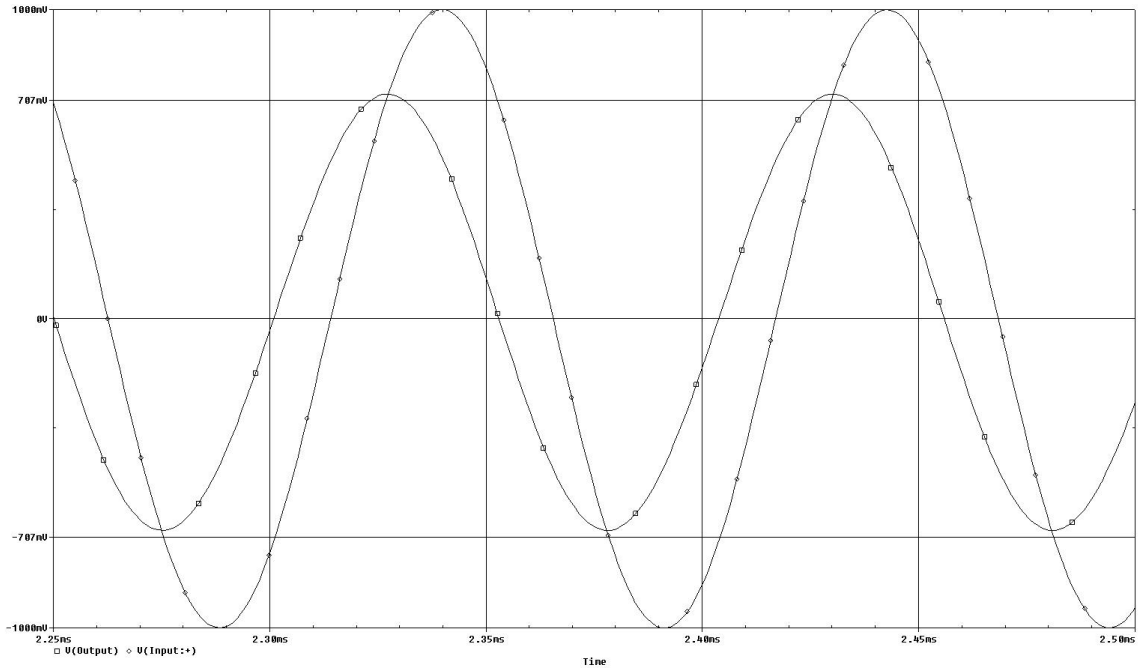

Figure 3.10: High-Pass Filter Transient

3.2 PID

The intended use for the ACR is in an analog control ASIC. The control ASIC contains a traditional Proportional-Integral-Derivative (PID) controller. The ACR is a great solution

Harmonic NO	Frequency (Hz)	Fourier Component	Normalized Component	Phase (deg)	Normalized Phase (deg)
1	1.00E5	2E-1	1.00	-1.46E2	0.00
2	2.00E5	1.25E-3	6.25E-3	-8.29E1	2.08E2
3	3.00E5	1.01E-3	5.03E-3	-8.41E1	3.53E2
4	4.00E5	9.74E-4	4.87E-3	-8.63E1	4.96E2
5	5.00E5	9.29E-4	4.65E-3	-8.84E1	6.39E2

Table 3.2: Total Harmonic Distortion high-pass Filter

for this application, not only does it provide the high resistance needed for the desired RC time constant, it also allows the controller gains to be adjusted to meet the demands of the system. The error, V_{err}, is the input to all stages. A folded cascode amplifier was used in conjunction with the ACR in all the stages of the PID controller. The power supply rails of the op amp are the same as the ACR, $\pm 2.5V$.

3.2.1 Proportional Stage

The proportional stage is an inverting gain stage utilizing two resistors and an operational amplifier. More than having a large value, the main attraction of using the ACR in this application is its adjustability. An ACR with a fixed value is included as the input resistor, while another ACR with variable resistance is used as the feedback resistor so the gain of the stage can be adjusted. The mathematical operation performed by the proportional stage is given by equation (3.7).

$$V_P = K_P \cdot V_{err} \tag{3.7}$$

The gain of the proportional stage is like that of any inverting gain stage given by equation (3.8).

$$V_P = \frac{-R_f}{R_i} \cdot V_{err} \tag{3.8}$$

Figure 3.11 shows the proportional stage of the controller. To see how the gain responds to input voltage frequency and tuning current of the feedback resistor, an AC simulation was performed. The feedback resistor tuning current was stepped from $50nA$ to $3.2\mu A$, doubling with each step, while the tuning current of the input resistor was held constant at $3.2\mu A$. Figure 3.12 shows the magnitude of the output voltage as the frequency of the input voltage was swept from $10Hz$ to $100MHz$. The magnitude stays the same across frequencies until the frequency limitations of the resistor are met. The plot shows the circuit working properly with the gain increasing as the tuning current of the feedback resistor is decreased. Figure 3.13 shows how the phase of the output is affected by the frequency of the input voltage and the tuning current of the feedback resistor. The phase starts at 180° because of the inverting configuration of the op amp, while at higher frequencies the internal poles and zeros of the ACR and op amp change the phase.

The simulations have shown the ACR can replace a passive resistor in an inverting gain stage in order to increase the flexibility of the circuit by allowing the gains to be changed with an adjustment to the tuning current of the feedback resistor.

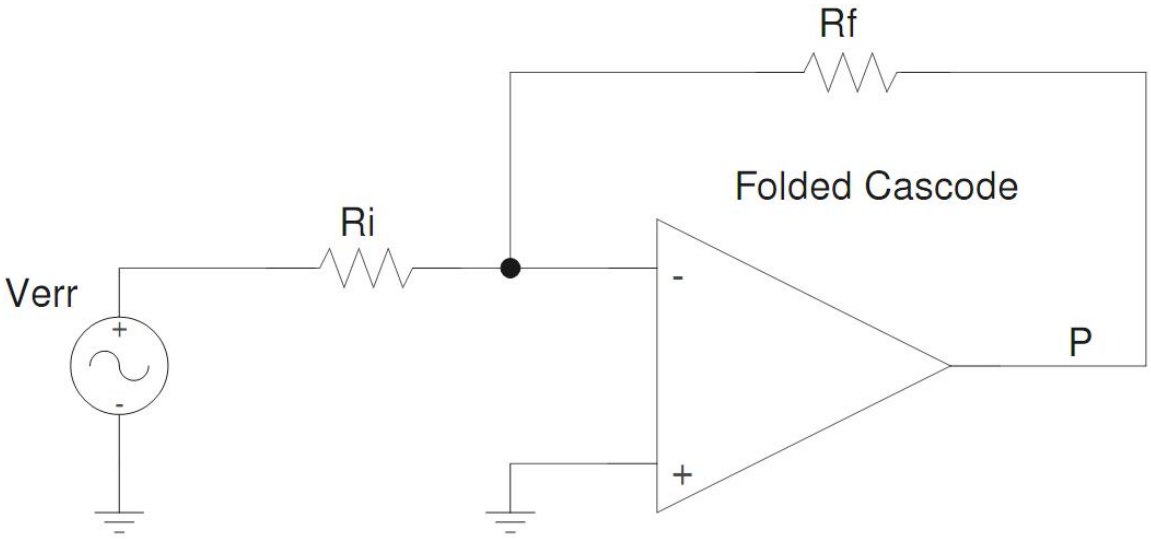

Figure 3.11: Proportional Stage of Controller

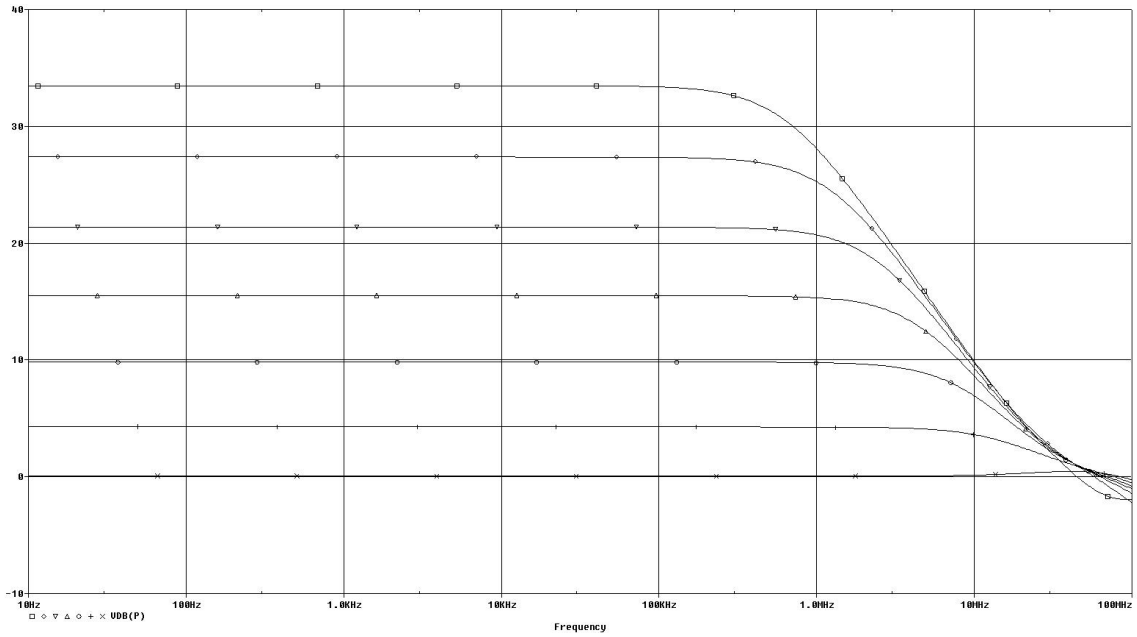

Figure 3.12: Proportional Stage Output Magnitude vs Input Voltage Frequency

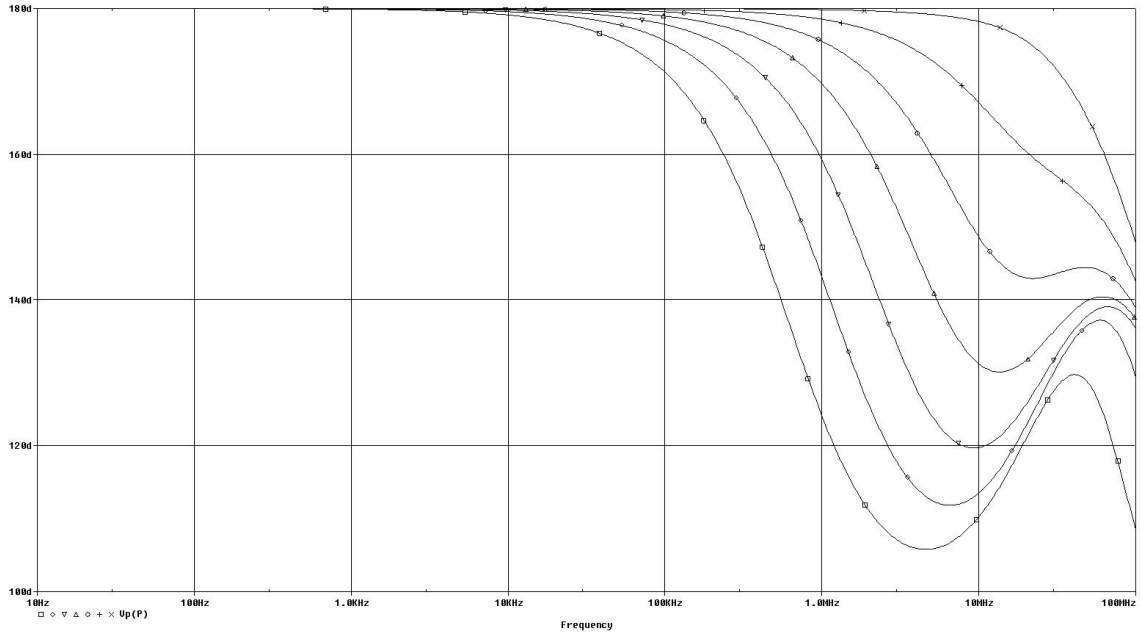

Figure 3.13: Proportional Stage Output Phase vs Input Voltage Frequency

3.2.2 Integral Stage

The integral stage uses a resistor connected between the input and inverting terminal of the op-amp and a feedback capacitor connected between the output and inverting terminal of the op-amp. Due to the feedback capacitor's small capacitance, $1pF$, the input resistor must have a large value to obtain the desired RC time constant. The main attraction the ACR has is its high resistance. The integral stage is arranged as shown in Figure 3.14.

The integral stage performs the following mathematical operation.

$$V_I = K_I \cdot \int_0^{\tau} V_{err} \cdot d\tau \tag{3.9}$$

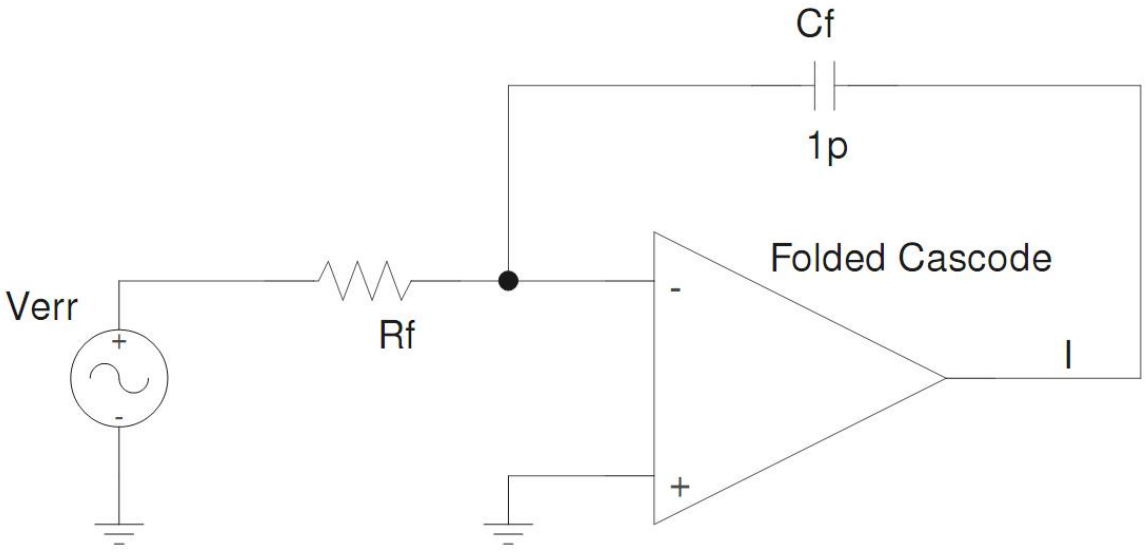

Figure 3.14: Integral Stage of Controller

The transfer function for the integrator is given in equation (3.10).

$$H(s) = \frac{-1}{sCR} \tag{3.10}$$

An AC simulation was performed on the integrator circuit to determine its performance and judge whether it is a suitable integrator. The input voltage frequency was swept from $10Hz$ to $100MHz$ while the tuning current was stepped from $50nA$ to $3.2\mu A$, doubling with each step. From the transfer function, equation (3.10), at very low frequencies the gain should be nearly infinite, however, as can be seen in Figure 3.15, the output is limited by the open loop gain of the op-amp. The magnitude plot has a slope of $-20dB$ per decade. It can be seen that with each step of the tuning current the gain and frequency response of the integrator changes. Along with the magnitude plot, the phase plot, Figure 3.16, of the output voltage starts at 180°, because of the inverting configuration of the integrator,

and moves toward 90° at the frequencies that the circuit integrates. The integrator circuit, with a CMOS input resistor, behaves in much the same way as an integrator circuit with a passive input resistor. Not only can the ACR provide the high resistance needed, but it also affords the designer the flexibility of adjusting the integrator to perform the way that is optimal.

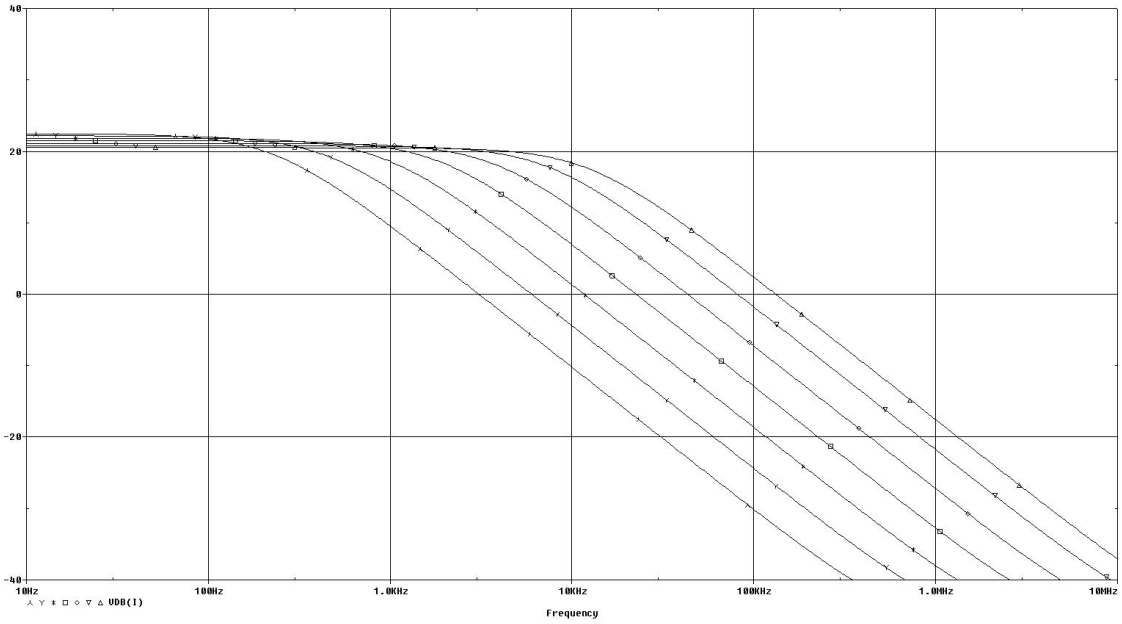

Figure 3.15: Integral Stage Output Magnitude vs Input Voltage Frequency

3.2.3 Differential Stage

The configuration of the differential stage, shown in Figure 3.17, is an inverting op amp with a input capacitor and a feedback resistor. As with the integrator, the input capacitor has a very small capacitance. To combat this the feedback resistor must be very large, which makes the ACR ideal for this application as well. The differential stage performs the mathematical operation in equation (3.11).

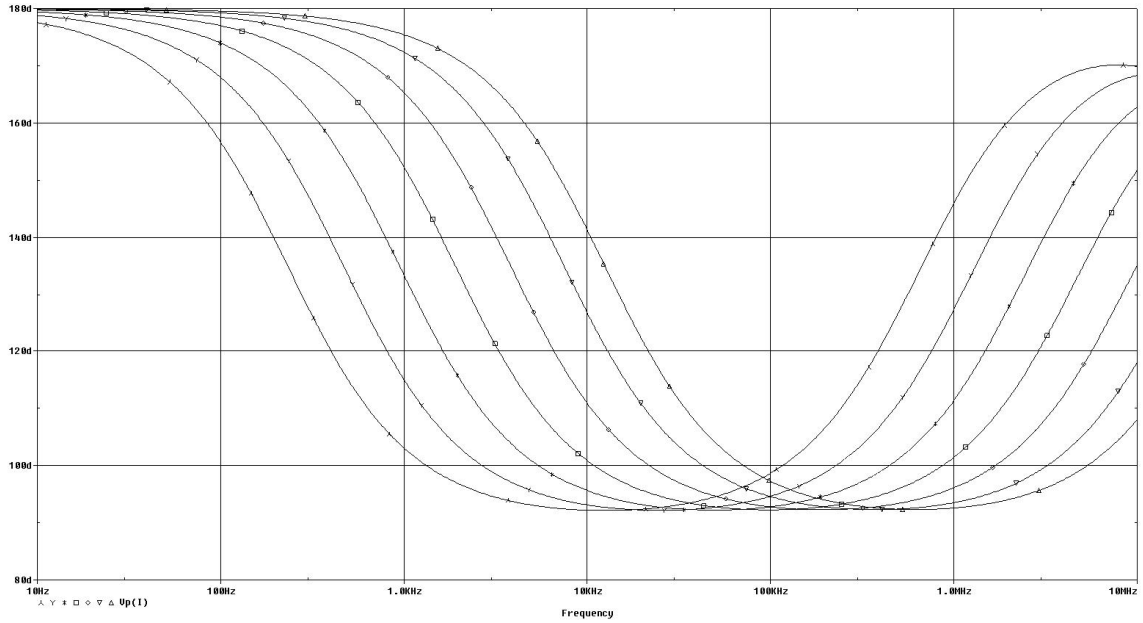

Figure 3.16: Integral Stage Output Phase vs Frequency

$$V_D = K_D \cdot \frac{dV_{err}}{d\tau} \tag{3.11}$$

The transfer function for the differential stage is give in equation (3.12).

$$H(s) = -sCR \tag{3.12}$$

To maintain stability in the differentiator, the high frequency gain of the circuit must be limited. To do this, a capacitor with the same value as the input capacitor, is placed in parallel with the feedback resistor, to provide a high frequency pole. The transfer function of the new circuit is given in equation (3.13).

$$H(s) = \frac{-sCR}{sCR + 1} \tag{3.13}$$

The differential stage frequency response plot, Figure 3.18, shows how feedback resistor tuning current changes affect the response of the circuit. The output voltage magnitude increases at $20dB$ per decade until it reaches the pole of the circuit, caused by the parallel combination of the feedback R and C. As the tuning current of the feedback resistor is decreased the pole of the differentiator decreases in frequency. The phase plot of the output voltage, Figure 3.19, shows that in the frequencies of differentiation the phase of the output is $-90°$ and drops to $-180°$ when reaching the pole. Both plots also show how the frequency response changes with changes to the tuning current of the feedback resistor. The pole of the RC parallel combination changes as well as the gain of the circuit. The plots show that the ACR behaves in the same manner as a passive resistor would in the differentiator with the advantage of high resistance values and tuning capability.

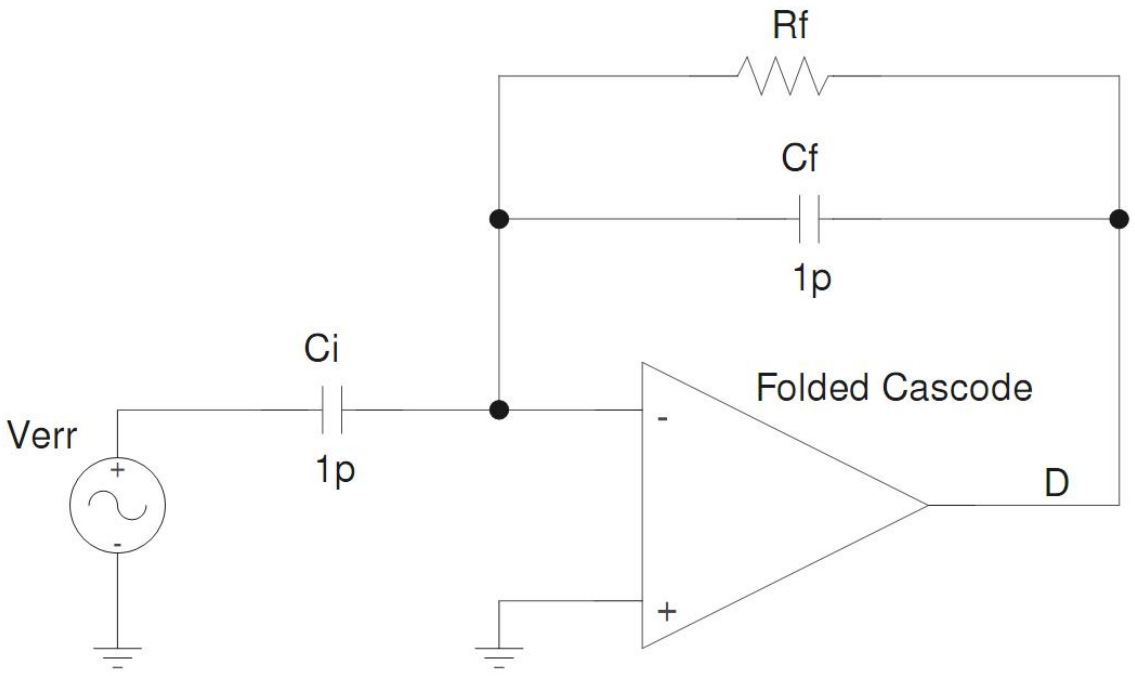

Figure 3.17: Derivative Stage of Controller

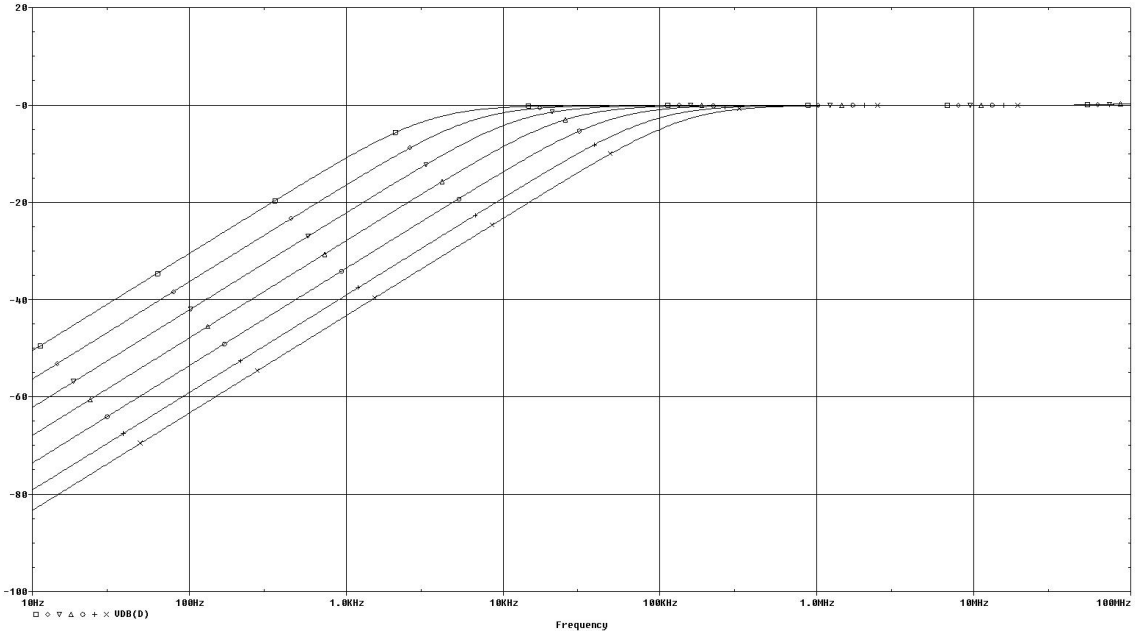

Figure 3.18: Differential Stage Output Magnitude vs Input Voltage Frequency

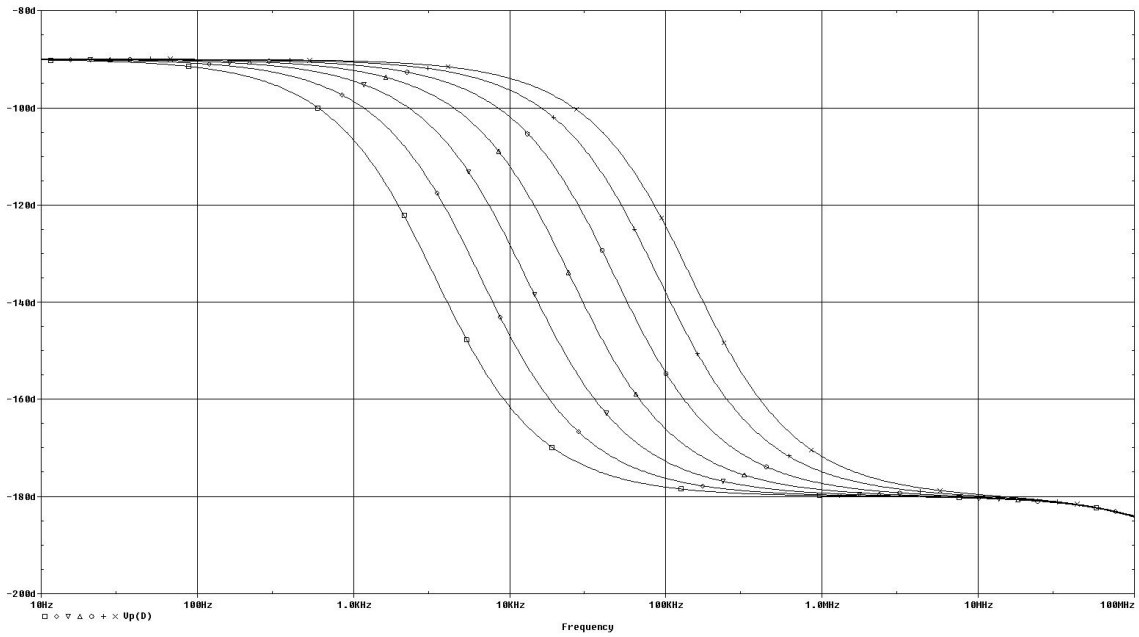

Figure 3.19: Differential Stage Output Phase vs Input Voltage Frequency

Chapter 4

Conclusion

Described in this thesis are the limitations of on-chip passive components in integrated circuits due to their inherent flaws. Many solutions have been attempted to try and overcome these limitations with limited success. A linear active CMOS resistor using the AMIS C5 process has been described that meets the limitations of on-chip capacitors by means of a very high synthesized resistance. It has been shown through simulation that as long as the bandwidth and input and output voltage levels are within range the CMOS resistor is a drop in replacement for a passive resistor in many applications. It performs well in single pole filters as well as more complex circuits such as a PID controller. Not only does the circuit provide very high resistance values, but it also yields flexibility through its ability to be tuned to a wide range of resistance values.

The CMOS resistor runs off of $\pm 2.5V$ supply voltage rails, to meet the requirements of the technology. The input voltage swing is $\pm 1.5V$ and the output voltage swing is $\pm 2V$. The bandwidth is more than $100KHz$ for the highest resistance value. These are more than adequate for the given application of a PID controller.

The CMOS resistor can be scaled with technology. It has very low quiescent power, on the order of microwatts. The signal voltage swing limitations can be addressed with higher voltage rails. The CMOS resistor introduces more noise into the system than a passive component of the same value, however, since device size makes passive components impractical and the difference in noise is not that great, about a factor of 8 difference, the CMOS resistor still provides an good alternative.

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Appendices

Appendix A

Transistor Models

```
* DATE: Jun 14/07
* LOT: T74S                  WAF: 8103
* Temperature_parameters=Default
.MODEL CMOSN NMOS (                              LEVEL   = 7
+VERSION = 3.1          TNOM    = 27            TOX     = 1.43E-8
+XJ      = 1.5E-7       NCH     = 1.7E17        VTH0    = 0.6174975
+K1      = 0.8876598    K2      = -0.0951675    K3      = 20.9151529
+K3B     = -9.6382243   W0      = 1.020585E-8   NLX     = 1.08112E-9
+DVT0W   = 0            DVT1W   = 0             DVT2W   = 0
+DVT0    = 0.8186693    DVT1    = 0.3372827     DVT2    = -0.4471971
+U0      = 449.7033083  UA      = 1E-13         UB      = 1.481183E-18
+UC      = -4.35408E-13 VSAT    = 1.750272E5    A0      = 0.6637676
+AGS     = 0.1269501    B0      = 2.281394E-6   B1      = 5E-6
+KETA    = -2.932031E-3 A1      = 7.951274E-7   A2      = 0.319673
+RDSW    = 1.044541E3   PRWG    = 0.1113887     PRWB    = 0.0124254
+WR      = 1            WINT    = 2.035444E-7   LINT    = 9.118243E-8
+XL      = 1E-7         XW      = 0             DWG     = -6.76768E-10
+DWB     = 2.626198E-8  VOFF    = -8.709001E-4 NFACTOR = 0.3274632
+CIT     = 0            CDSC    = 2.4E-4        CDSCD   = 0
+CDSCB   = 0            ETA0    = 2.542626E-3   ETAB    = -9.003453E-4
```

```
+DSUB    = 0.1345826    PCLM    = 2.7474125    PDIBLC1 = 0.673548
+PDIBLC2 = 3.953974E-3  PDIBLCB = 0.0676693    DROUT   = 0.8884749
+PSCBE1  = 7.0944E8     PSCBE2  = 5.636482E-4  PVAG    = 0
+DELTA   = 0.01         RSH     = 81.6         MOBMOD  = 1
+PRT     = 0            UTE     = -1.5         KT1     = -0.11
+KT1L    = 0            KT2     = 0.022        UA1     = 4.31E-9
+UB1     = -7.61E-18    UC1     = -5.6E-11     AT      = 3.3E4
+WL      = 0            WLN     = 1            WW      = 0
+WWN     = 1            WWL     = 0            LL      = 0
+LLN     = 1            LW      = 0            LWN     = 1
+LWL     = 0            CAPMOD  = 2            XPART   = 0.5
+CGDO    = 2.22E-10     CGSO    = 2.22E-10     CGBO    = 1E-9
+CJ      = 4.258295E-4  PB      = 0.9372076    MJ      = 0.4456534
+CJSW    = 3.076063E-10 PBSW    = 0.8          MJSW    = 0.181535
+CJSWG   = 1.64E-10     PBSWG   = 0.8          MJSWG   = 0.181535
+CF      = 0            PVTH0   = 0.0162776    PRDSW   = 278.4786758
+PK2     = -0.0814166   WKETA   = -7.283165E-3 LKETA   = -4.020995E-3)
*
.MODEL CMOSP PMOS (                              LEVEL   = 7
+VERSION = 3.1          TNOM    = 27           TOX     = 1.43E-8
+XJ      = 1.5E-7       NCH     = 1.7E17       VTH0    = -0.9152268
+K1      = 0.553472     K2      = 7.871921E-3  K3      = 53.4949014
+K3B     = -3.7856731   W0      = 6.738971E-6  NLX     = 2.795695E-7
```

```
+DVT0W   = 0             DVT1W   = 0             DVT2W   = 0
+DVT0    = 1.3395264     DVT1    = 0.267458      DVT2    = -0.0568881
+U0      = 201.3603195   UA      = 2.408572E-9   UB      = 1E-21
+UC      = -1E-10        VSAT    = 1.272242E5    A0      = 0.7748807
+AGS     = 0.0598168     B0      = 6.64175E-7    B1      = 5E-6
+KETA    = -4.865785E-3  A1      = 1.799339E-4   A2      = 0.4844663
+RDSW    = 3E3           PRWG    = -0.0304277    PRWB    = -0.0443398
+WR      = 1             WINT    = 2.824041E-7   LINT    = 1.186971E-7
+XL      = 1E-7          XW      = 0             DWG     = -1.16725E-9
+DWB     = -1.237634E-8  VOFF    = -0.0735326    NFACTOR = 0.6345367
+CIT     = 0             CDSC    = 2.4E-4        CDSCD   = 0
+CDSCB   = 0             ETA0    = 9.767795E-4   ETAB    = -0.2
+DSUB    = 1             PCLM    = 2.2583753     PDIBLC1 = 0.0394748
+PDIBLC2 = 3.705722E-3   PDIBLCB = -0.0320804    DROUT   = 0.212888
+PSCBE1  = 2.49175E10    PSCBE2  = 2.457905E-9   PVAG    = 0
+DELTA   = 0.01          RSH     = 109           MOBMOD  = 1
+PRT     = 0             UTE     = -1.5          KT1     = -0.11
+KT1L    = 0             KT2     = 0.022         UA1     = 4.31E-9
+UB1     = -7.61E-18     UC1     = -5.6E-11      AT      = 3.3E4
+WL      = 0             WLN     = 1             WW      = 0
+WWN     = 1             WWL     = 0             LL      = 0
+LLN     = 1             LW      = 0             LWN     = 1
+LWL     = 0             CAPMOD  = 2             XPART   = 0.5
```

```
+CGDO    = 2.89E-10     CGSO    = 2.89E-10     CGBO    = 1E-9
+CJ      = 7.243769E-4  PB      = 0.9580741    MJ      = 0.4957715
+CJSW    = 2.398685E-10 PBSW    = 0.99         MJSW    = 0.3331245
+CJSWG   = 6.4E-11      PBSWG   = 0.99         MJSWG   = 0.3331245
+CF      = 0            PVTH0   = 5.98016E-3   PRDSW   = 14.8598424
+PK2     = 3.73981E-3   WKETA   = 6.989253E-3  LKETA   = -7.31204E-3)
*
```