CHARACTERIZATION OF DIE STRESSES IN LARGE

AREA ARRAY FLIP CHIP PACKAGES

Except where reference is made to the work of others, the work described in this thesis is
my own or was done in collaboration with my advisory committee. This thesis does not
include proprietary or classified information.

_____
Jordan Christopher Roberts

Certificate of Approval:

_____   _____
Richard C. Jaeger, Co-Chair   Jeffrey C. Suhling, Co-Chair
Distinguished University Professor   Quina Distinguished Professor
Electrical and Computer Engineering   Mechanical Engineering

_____   _____
Robert L. Jackson   George T. Flowers
Assistant Professor   Interim Dean
Mechanical Engineering   Graduate School

CHARACTERIZATION OF DIE STRESSES IN LARGE

AREA ARRAY FLIP CHIP PACKAGES

Jordan Christopher Roberts

A Thesis

Submitted to

the Graduate Faculty of

Auburn University

in Partial Fulfillment of the

Requirements for the

Degree of

Master of Science

Auburn, Alabama
August 9, 2008

CHARACTERIZATION OF DIE STRESSES IN LARGE

AREA ARRAY FLIP CHIP PACKAGES

Jordan Christopher Roberts

_____
Signature of Author

_____
Date of Graduation

VITA

Jordan Christopher Roberts was born December 14, 1980 to Bobby E. and Jesca G. Roberts in Guntersville, Alabama. He graduated from Sardis High School as Salutatorian in 1999. He graduated from the University of Alabama at Birmingham in 2003 with a Bachelor of Science in Mechanical Engineering. While working towards his degree, he worked at Southern Ductile Casting Company, now known as Citation Bessemer. He began his graduate studies at Auburn University in January 2004.

THESIS ABSTRACT

CHARACTERIZATION OF DIE STRESSES IN LARGE

AREA ARRAY FLIP CHIP PACKAGES

Jordan Christopher Roberts

Master of Science, August 9, 2008
(B.S.M.E., University of Alabama at Birmingham, 2003)

212 Typed Pages

Directed by Jeffrey C. Suhling and Richard C. Jaeger

Microprocessor packaging in modern workstations and servers often consists of one or more large flip chip die that are mounted to a high performance ceramic chip carrier. The final assembly configuration features a complex stack up of area array solder interconnects, underfill, ceramic substrate, lid, heat sink, thermal interface materials, second level solder joints, organic PCB, etc., so that a very complicated set of loads is transmitted to the microprocessor chip. Several trends in the evolution of this packaging architecture have exacerbated die stress levels including the transition to larger die, high CTE ceramic substrates, lead free solder joints, higher level of power generation, and larger heat sinks. Die stress effects are of concern due to the possible degradation of

silicon device performance (mobility/speed) and due to the possible damage that can occur to the copper/low-k top level interconnect layers.

In this work, test chips containing piezoresistive sensors have been used to measure the stresses induced in microprocessor die after various steps of the assembly process as well as to characterize stresses induced by various mechanical clamping scenarios. The utilized (111) silicon test chips were able to measure the complete three-dimensional stress state (all 6 stress components) at each sensor site being monitored by the data acquisition hardware. The test chips had dimensions of 20 x 20 mm, and 3600 lead free solder interconnects (full area array) were used to connect the chips to the high CTE ceramic chip carriers. Before packaging, the sensor resistances were measured by directly probing the stress test die. The chips were reflow soldered to the ceramic substrate, and then underfilled and cured. Finally, a metallic lid was attached to complete the ceramic LGA package. After every packaging step (solder reflow, underfill dispense and cure, lid attachment and adhesive cure), the sensor resistances were re-measured, so that the die stresses induced by each assembly operation could be characterized. The build-up of the die stresses was found to be monotonically increasing, and the relative severity of each assembly step was judged and compared. Such an approach allows for various material sets (solders, underfills, TIM materials, lid metals, and lid adhesives) to be analyzed and rated for their contribution to the die stress level. Baseline resistance changes with temperature were determined for the test packages. Finally, mechanical and thermal characterizations of the utilized underfill material were performed.

ACKNOWLEDGEMENTS

First, I would like the thank the Lord for giving me the ability to perform this work; for comforting me when I was down, and for resolving issues that I thought were irresolvable. I thank my mother from the bottom of my heart for her love, patience, and encouragement throughout my life and especially during my graduate studies. I thank my father for the examples he set for me, and the love he showed me. I wish he could see this work completed.

Thanks go to my church family at Sardis Baptist Church in Sardis City, Alabama, and my church home in Auburn, Lakeview Baptist Church. They have supported me with prayer every step of the way.

Thanks go to my committee co-chairs Dr. Jeff Suhling and Dr. Richard Jaeger for their patience and invaluable guidance and teaching throughout this experience. I would also like to thank Dr. David Dyer and Dr. Roy Knight for guidance and encouragement during my graduate career.

Thanks to Kaysar Rahim, a great friend and co-worker for all he taught me and for four-point bending results. Thanks to Hecham Abdel-Hady for Labview programming, and also Chang Lin for micro-tester training and underfill testing. Thanks to John Marcell for things too numerous to mention. Thanks to Asa Vaughan for friendship, advice, and DSC testing. Thank you to the many friends not mentioned here.

Guide to Preparation and Submission of Theses and Dissertations

Microsoft Office 2003, Solid Edge, ANSYS, MathCAD, LabView, and SigmaPlot

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1

INTRODUCTION

1.1   Area Array Components for Microprocessor Packaging

Microprocessor packaging in modern high performance workstations and servers often consists of one or more large flip chip die that are mounted to a high density ceramic chip carrier. Figure 1 illustrates a typical configuration with an air-cooled heat sink. Over the past few years, the flip chip solder interconnects have transitioned to full area arrays and lead free composition, while the size of the processor die has grown dramatically. In addition, the utilized Ceramic Ball Grid Array (CBGA) substrates are now typically constructed from "high CTE" glass ceramic materials [1-7]. Relative to the older alumina ceramic technology that used tungsten based conductors, these new ceramics have significantly higher coefficients of thermal expansion (10-12 ppm/C) and much lower stiffness (70-80 GPa). They are also formed at much lower co-firing temperatures, which allows processing with higher performance copper-based conductors.

Elements completing the basic processor package are the underfill between the chip and the chip carrier, and a metal lid (AlSiC) adhered to the top of the ceramic carrier with an adhesive and to the back of the die through a thermal interface material (TIM1). The processor package can be used as a Land Grid Array (LGA) in a socket, or as a

TIM2

Lid
Adhesive

TIM1

Heat Sink

Die

Lid

Ceramic BGA Substrate

PCB Laminate
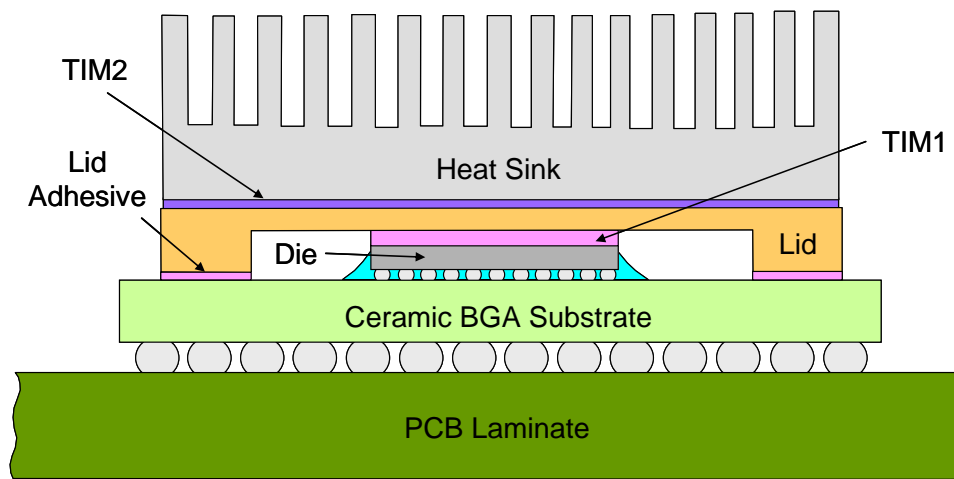
Figure 1.1 - Typical Packaging Architecture for a High Performance Flip Chip
Microprocessor

Ceramic Ball Grid Array attached to a high density PCB if an additional set of second level solder interconnects are added to the bottom of the ceramic chip carrier. In either case, a heat sink is normally bonded (TIM2) and mechanically clamped to the metallic lid on the chip carrier.

The packaging architecture described above and newer variations under development transmit a complicated set of loads to the microprocessor chip. While the high CTE ceramic substrate technology helps to increase the reliability of the second level (board level) interconnects, the larger CTE mismatch with the silicon chip reduces the flip chip solder ball reliability and causes transmission of larger loads to the die.

The transition to use of stiffer lead free flip chip solder interconnects has further exacerbated die stress levels. Other sources of mechanically and thermally induced die stresses include the clamped heat sink and high levels of power generation. Finally, the presence of power cycling further complicates the analysis of package reliability. All of these die stress effects are of concern due to the possible degradation of silicon device performance (mobility/speed) and due to the possible damage that can occur to the copper/low-k top level die interconnect layers.

On-chip piezoresistive stress sensors represent a unique approach for characterizing stresses in silicon die embedded within a complicated packaging architecture such as described above. Die stress measurements in flip chip assemblies have been performed by several investigators using test chips [8-14]. Variations of the (100) silicon Sandia ATC04 test die have been utilized to examine device side die stresses and compare stress levels with different underfills [8-10]. In previous flip chip studies, the mechanical stresses present on the backside (top side) [11] and the device

side (bottom side) [12-14] of the die at each stage of the flip chip assembly process were investigated. In these investigations, (111) silicon test chips were utilized that were able to measure all of the die stress components including the interfacial shear stresses. Die stress variations were observed during underfill curing, and the room temperature die stresses in the final cured assemblies have been compared for several different underfill encapsulants.

In this work, test chips containing piezoresistive sensors have been used to measure the stresses induced in microprocessor die after various steps of the assembly process as well as to characterize stresses induced by various mechanical clamping scenarios. The test chips were also used to study the effects of temperature on large microprocessor package, and to perform preliminary power cycling studies. The utilized (111) silicon test chips were able to measure the complete three-dimensional stress state (all 6 stress components) at each sensor site being monitored by the data acquisition hardware. The utilized test chips had dimensions of 20 x 20 mm, and 3600 lead free solder interconnects (full area array) were used to connect the chip to the high CTE ceramic chip carrier. Before packaging, the sensor resistances were measured by directly probing the stress test die. The chips were reflowed to the ceramic substrate, and then underfilled and cured. Finally, a metallic lid was attached to complete the ceramic LGA package. After every packaging step (solder reflow, underfill dispense and cure, lid attachment and adhesive cure), the sensor resistances were re-measured, so that the die stresses induced by each assembly operation could be characterized. The build-up of the die stresses was found to be monotonically increasing, and the relative severity of each assembly step was judged and compared. Such an approach also allows for various

material sets (solders, underfills, TIM materials, lid metals, and lid adhesives) to be analyzed and rated for their contribution to the die stress level. The final test package configuration, with lid attachment, was also used to determine baseline resistance changes with temperature. Finally, mechanical and thermal characterizations of the utilized underfill material were performed.

CHAPTER 2

LITERATURE REVIEW

2.1 **Review of Electronic Package Issues**

2.1.1 Introduction

The integrated circuit (IC) industry continually strives for faster, denser, larger, and more powerful chips. This push has increased industry consciousness to reliability concerns, and the need for continued study of the structural reliability of electronic packages. An assortment of different materials comprises an electronic package, each with different mechanical properties. The driving property in regards to stress generation and package failure has historically been the coefficient of thermal expansion (CTE), more specifically the mismatches of the CTEs within an electronic package. Each stage of fabrication typically adds another dissimilar material to a package. Thus, an obvious need arises for the characterization of stress levels caused by each stage of packaging.

2.1.2 Historical Packaging Issues

In their work, Dale and Oldfield [15] discussed stresses due to package manufacturing processes. They included stresses produced by oxidation, diffusion, metallization, and even wafer preparation. Also named as stress producers were the actual die attachment, wire bonding, and encapsulation. Lau [16] addressed many of these causes as well as discussing different surface mounting processes and die bending during

mounting or bonding. The results of thermally-induced stresses have been widely studied. Lau also discussed package cracking, wire damage, and passivation cracks on die. Inayoshi [17] showed the effect of stresses on the passivation layer of silicon chips. Lesk, et al. [18] and Edwards, et al. [19] studied damage and metal shift caused by thermally induced stresses. The authors of [18] also studied problems related to packages containing large die. Nishamura and co-workers [20, 21] showed that cracks in the package induced by thermal cycling also greatly affect die stress levels. In addition, encapsulated packages face additional problems caused by the encapsulant. The effects of die attachment, among other manufacturing processes were shown by van Kessel, et al. [22, 23]. In addition, it was noted that stresses have great effect on packages with certain die surface finishes.

2.2   Stress Determination in Electronic Packaging

Failure of IC electronic packages has been a problem since their inception. Researchers have used various methods to measure, characterize, and otherwise understand stress levels in integrated circuit packages. Suhir [24, 25] and Liew, et al. [26] saw parallels between bimetal thermostats and interfacial stresses in electronic packages; developing an analytical approach with elementary beam theory. Tay and Lin [27-29] used an analytical approach to model delamination during solder reflow, and then correlated their predictions with experimental data.

Historically, analytical methods have been difficult to implement due to the complex nature of electronic package geometries. Many well known analytical methods, such as the Distance to Neutral Point (DNP) approach and the Coffin-Manson theory, are crude and based on over-simplified models with extensive assumptions. As with many other problems within the field of solid mechanics, this has given rise to the popularity of

7

experimental methods, especially when correlated with some form of computer simulation, such as finite element analysis (FEA).

2.2.1   Experimental Methods

Moiré interferometry is a powerful experimental method for measuring displacements of a mechanical object. Researchers such as Bastawros and Voloshin [30], Han and Guo [31], and Liu, et al. [32, 33] have employed moiré techniques to measure thermally-induced deformations of electronic packages. Stiteler and Ume [34], and Wang and Hassell [35] used shadow moiré to study warpage of packages. Voloshin, et al. [36] used Digital Image Analysis Enhanced Moiré Interferometry (DIAEMI) to characterize in-situ out-of-plane die displacements during die attachment. Displacement data were recorded and mapped across the die, and then compared with stress data obtained using a hybrid FEA technique. Additional experimental techniques have been discussed by Guo and Sarihan [37].

Silicon is a piezoresistive material which exhibits a change in resistivity upon application of a mechanical stress. This feature has lead to the development of silicon stress sensing integrated circuit chips. In the 1950s, the concept of using piezoresistive semiconductors as tools to measure stress and strain was introduced by Smith [38]. Later, the temperature dependencies of the piezoresistive coefficients of silicon, as well as germanium, were studied by Tufte and Stetzer [39], as well as Suhling, et al. [40, 41]. The nonlinear nature of the piezoresistive effect was discussed by Yamada and co-workers [42], while the piezoresistive coefficients were represented graphically by Kanda [43]. A full discussion of semiconductor strain gages was given by Dally and Riley [44]. The detailed

8

theory of silicon piezoresistive sensors was derived by Bittle, et al. [45-46], while Kang [47] expanded and applied this theory to various wafer planes for silicon and silicon carbide.

In the use of piezoresistive silicon stress sensors, the need for calibration of the piezoresistive coefficients of the silicon chip is widely accepted. Traditionally, some form of four-point bending method is used for calibration. This method has been discussed in detail by Beaty, et al. [48], Bittle, et al. [45-46], Suhling, et al. [40, 41, 49], Jaeger, et al. [50-53], and van Gestal [54]. A method of calibration employing application of a hydrostatic state of stress to a chip in a pressure vessel was devised by Kang, et al. [55]. The four-point bending and hydrostatic methods are performed on sliced silicon wafer strips and diced silicon chips, respectively. Cordes [56] and Suhling, et al. [57-58] have alternatively devised a calibration technique applied at the wafer level. Lwo, et al. [59-61] also discussed the design and fabrication of stress sensors, and designed and fabricated a calibration apparatus.

Piezoresistive stress sensors have been used by many researchers to study die stress levels in electronic packages. In early work, Edwards, et al. [19], Groothuis, et al. [62], and van Kessel, et al. [22] used chips fabricated from (100) silicon wafers to examine small packages. These early test chips contained two-element sensor rosettes, with the sensors oriented at 0 and 90 degrees to the wafer flat. Early work was aimed at material evaluation, reliability testing, and process control. Later, Gee, et al. [63] used four element rosettes to map stresses during thermal cycling. Van Gestal and co-workers [64] also used these same chips to study dual inline packages.

Miura, et al. [65-69] also used (100) chips to study die stresses in dual inline packages. The chips used in their study employed sensors fabricated with both n-type and p-type doping, where the n-type sensors were oriented at 0° and 90°, and the p-type sensors were oriented at ±45°. This chip was notable, as it was the first test chip able to measure out-of-plane normal stresses on the die. Zou, et al. [70-72] also used (100), four element test chips. The chips used the same sensor orientations as the Miura chips, but the doping of the sensor pairs was reversed. The Sandia ATC-04, a (100) silicon test chip, was used to study die mounted on ceramic substrates by Sweet [73]. The Sandia chip used a sensor rosette with eight resistors, including four n-type sensors at orientations of 0°, ±45°, and 90°, and four p-type sensors of the same orientations. The third generation of Sandia test chips has also been studied [74]. Bossche, et al. [75-76] and Lo, et al. [77-78] designed, fabricated, and calibrated stress sensing chips with similar capabilities to prior studies.

Suhling and his co-workers [79-82] have demonstrated the advantages of stress sensors fabricated from (111) silicon wafers as opposed to (100) wafers. When optimized, rosettes on (111) silicon can measure the complete state of stress at a point. In addition, optimized (111) rosettes can measure four temperature compensated stress components, as opposed to (100) rosettes, which can measure two. Suhling, et al. [80, 82] used these advantages to be the first to measure the complete state of stress at a point on the surface of a die with test chips designated BMW-1. This chip used an eight sensor rosette containing n-type and p-type sensors oriented at 0°, ±45°, and 90°, with respect to the wafer flat. The BMW-1 chips were mounted to organic substrates, and then used to measure stress in chip on board packages at room temperature. These studies were the

first to measure out-of-plane shear stresses at the interface of the die and encapsulant. Zou, et al. [70-72] used a second iteration of the BMW chip to measure stresses in different packages. Schwizer, et al. [83-84], described a new test chip package that uses a flip chip micro sensor, capable of measuring forces on solder balls in three directions.

Jaeger, et al. [85-89] and others [90-92] have utilized other silicon devices such as transistors and van der Pauw structures to develop stress sensor chip technology. In these studies, relationships between applied mechanical stress and transistor performance were developed. Mian, et al. [93-94] developed and used van der Pauw structures to characterize stress. Mayer, et al. [95-96] also used test chips with MOS technology.

Piezoresistive stress sensors have also been used to characterize stress levels during and after different stages of package assembly. Stresses due to die attachment and encapsulation were studied by Natarajan, et al. [97] using chips fabricated from n-doped (100) silicon wafers. Integrated piezoresistive stress sensors were also employed by Bjorneklett, et al. [98] to measure stress induced by die attachment. Ducos, et al. [99] measured stress levels during package assembly in-situ. Thomas and co-workers [100] measured the resistances of sensors on chips assembled into various ball grid array packages. Recently, Rahim [101] measured stress levels on both sides of a flip chip die during each stage of assembly. Peterson, et al. [8, 102] used test chips to study flip chip ball grid array packages. Zou and co-workers [103] also used test chips to evaluate die attachment adhesives in ceramic Pin Grid Array (PGA) packages. Palaniappan, et al. [9-10] used test chips to study curing parameters of flip chip assemblies.

It should be noted that use of piezoresistive stress sensors requires foreknowledge of errors expected in their calibration and use. Aside from error in any data acquisition

11

system or the physical wiring of a test setup, there are several ways inappropriate use or calibration may affect results. A discussion of optimized rosette design has been give by Suhling, et al. [81], and a complete discussion of design and calibration errors was presented by Jaeger, et al. [104-105].

2.2.2 Numerical Methods

The finite element method is powerful tool that has risen to prominence due to its inherent time and cost savings. Many problems in electronic packaging have been successfully modeled using this technique. It allows for the implementation of the wide variety of geometric, material, and environmental conditions seen by IC packages. In early work, FEA techniques were used to study the effects of different materials and geometry on dual inline packages by Groothuis, et al. [62], and Pendse [106]. Kelly, et al. [107-108] studied thermal stresses in plastic packages numerically. Van Gestel [64] used simulation techniques to study delamination in plastic packages. Sweet, et al. [109-110] used a viscoplastic material model in a study of die surface stresses.

2.2.3 Correlation of Experimental and Numerical Methods

Although finite element analysis is a powerful tool, it may not always be a reliable predictor of mechanical events. For this reason, researchers have relied on correlation of experimental methods and numerical methods. Skipor, et al. [111] used moiré interferometry to measure displacements of two different packages, then measured stresses in the packages with test chips, and compared both results with finite element predictions. Ducos, et al. [99] also correlated their results with FEA data. Slattery, et al. [112] used

both piezoresistive stress chips and finite element analysis to characterize stress levels in packages. Chen, et al. [113] studied the effects of underfill in two types of packages with the use of two-dimensional finite element analysis and experimental techniques. Analytical, numerical, and experimental results were also correlated in the work of Peterson, et al. [8]. Zou [70, 72, 103] related stress data from PGA and chip on board packages to finite element simulations. More recently, Rahim [101] showed graphical correlation between measured die stress levels at various stages of assembly and the corresponding predictions from FEA models. Y. Chen [114] mapped die stress levels using CMOS stress sensors and also graphically showed agreement with finite element data.

2.3   High End Microprocessor Issues

Several investigations have been performed on the thermal-mechanical reliability of the second level CBGA solder joints when using high CTE ceramic substrates. Pendse, et al. [2] demonstrated order of magnitude type improvements in the thermal cycling reliability using both thermal cycling tests and finite element simulations. Dai, et al. [3] and Pan and co-workers [4] have examined the effects on reliability of 52.5 x 52.5 mm CBGAs (2533 I/O) with various solder alloys (SnPb and SAC), ceramic substrate thicknesses, lid configurations, and lid materials (AlSiC compositions). Their results suggest that reliability is increased significantly when using the SAC solder alloy, a lid-less configuration (not practical if a heat sink is needed), and a lid material with lower SiC content. The ceramic substrate thickness had little effect on reliability due to the fact that the new ceramic materials are more compliant (lower stiffness) than traditional alumina compositions, as well as they provide a better CTE match between the ceramic

13

substrate and PCB laminate. Enhanced solder joint reliability has also been demonstrated

for 42.5 x 42.5 mm and 45 x 45 mm CBGAs [5-6], and for Ceramic Column Grid Arrays

(CCGAs) [5, 7] when using the higher CTE ceramic substrates. Xu, et al. [8] have

explored the heat transfer characteristics and air cooling limits of the packaging

configuration in the previous chapter (Figure 1.1).

Using finite element simulations, Tosaya et al. [6] have predicted a 2X increase in

the die normal stress levels for a flip chip mounted on a high CTE ceramic carrier

(relative to the analogous configuration on an alumina carrier). In addition, the stresses at

the die to underfill interface were significantly higher with the high CTE ceramic carrier,

complicating underfill selection and raising concerns relative to damage of fragile

Interlayer Dielectric (ILD) layers.

CHAPTER 3

REVIEW OF PIEZORESISTIVE THEORY

3.1   General Resistance Change Equations

The term piezoresistive refers to a material that undergoes a change in electrical resistance under the application of a mechanical load. The application of a load to silicon changes its resistivity behavior from isotropic to anisotropic. The relation between the anisotropic second order resistivity tensor of silicon and the second order stress tensor can be modeled using the equation [46]

$$\rho_{ij} = \rho\delta_{ij} + \pi_{ijkl}\sigma_{kl} \tag{3.1}$$

where π is the fourth order piezoresistivity tensor, σ is the second order stress tensor, ρ is resistivity, and δ_{ij} is the Kronecker delta. Equation (3.1) can also be can be written for an arbitrary rotated orthogonal coordinate system as

$$\rho'_{ij} = \rho\delta_{ij} + \pi'_{ijkl}\sigma'_{kl} \tag{3.2}$$

where π' is the fourth order piezoresistivity tensor in the rotated system, and σ' is the second order stress tensor in the rotated system. Using reduced index notation, eq. (3.2) becomes

$$\rho'_{ij} = \rho\delta_{ij} + \pi'_{\alpha\beta}\sigma'_{\beta} \tag{3.3}$$

At this point, the development is specialized to the filamentary silicon conductor shown in Figure 3.1. The conductor is oriented arbitrarily in an orthogonal (x_1, x_2, x_3) coordinate system, where the unprimed axes $x_1 = [100]$, $x_2 = [010]$, and $x_3 = [001]$ are the principal crystallographic directions of the m3m silicon crystal. The normalized resistance change of the conductor can be expressed as [46]

$$\frac{\Delta R}{R} = (\pi'_{1\alpha}\sigma'_{\alpha})l'^2 + (\pi'_{2\alpha}\sigma'_{\alpha})m'^2 + (\pi'_{3\alpha}\sigma'_{\alpha})n'^2$$

$$+ 2(\pi'_{4\alpha}\sigma'_{\alpha})l'n' + 2(\pi'_{5\alpha}\sigma'_{\alpha})m'n' + 2(\pi'_{6\alpha}\sigma'_{\alpha})l'm' \qquad (3.4)$$

$$+ [\alpha_1 T + \alpha_2 T^2 + ... \quad]$$

where α_1, α_2 ... are temperature coefficients of resistance, l', m', and n' are direction cosines of the conductor orientation with respect to the primed system. In this equation, T is the temperature change

$$T = T_m - T_{ref} \qquad (3.5)$$

where T_m is the temperature of the silicon when the final resistance measurement is made, and T_{ref} is the reference temperature of the silicon when the initial unstressed resistance R is measured. Equation (3.4) follows the summation convention for repeated indices, and stress components are given in reduced index notation:

$$\sigma'_1 = \sigma'_{11}, \sigma'_2 = \sigma'_{22}, \sigma'_3 = \sigma'_{33}$$
$$\sigma'_4 = \sigma'_{13}, \sigma'_5 = \sigma'_{23}, \sigma'_6 = \sigma'_{12} \qquad (3.6)$$

The off-axis piezoresistive coefficients $\pi'_{\alpha\beta}$ can be related to the 3 unique on-axis coefficients $\pi_{11}, \pi_{12}, \pi_{44}$, which are evaluated in the original coordinate system aligned
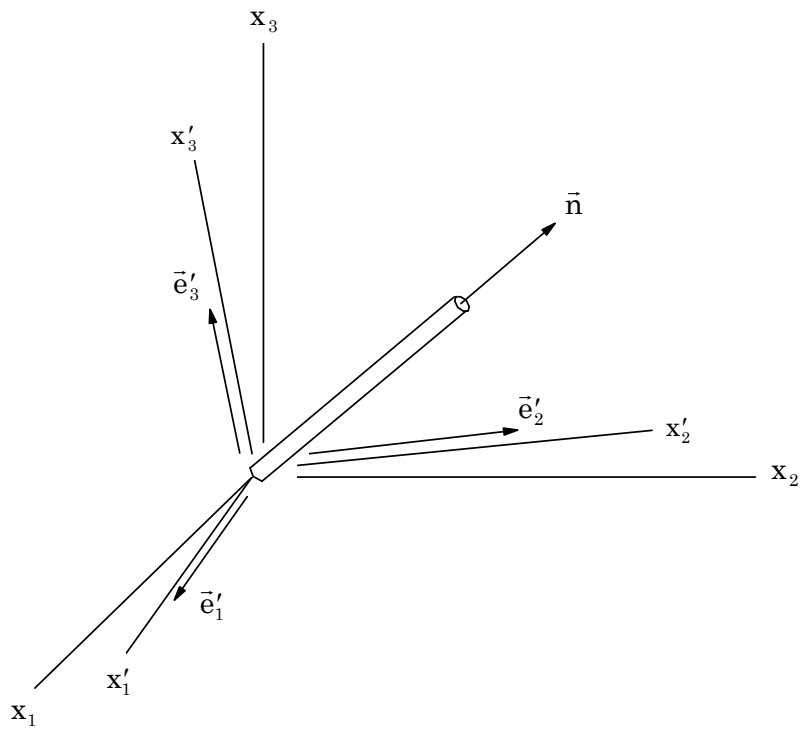
Figure 3.1 - Filamentary Silicon Conductor

with the principal crystallographic axes. Using tensor transformations, this relationship

can be expressed as

$$\pi'_{\alpha\beta} = T_{\alpha\gamma}\,\pi_{\gamma\delta}\,T^{-1}_{\delta\beta} \tag{3.7}$$

where

$$[\pi_{ij}] = \begin{bmatrix} \pi_{11} & \pi_{12} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{11} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{12} & \pi_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & \pi_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & \pi_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & \pi_{44} \end{bmatrix} \tag{3.8}$$

is the on-axis piezoresistive coefficient matrix, and

$$[T_{\alpha\beta}] = \begin{bmatrix} l_1^2 & m_1^2 & n_1^2 & 2\,l_1\,n_1 & 2\,m_1\,n_1 & 2\,l_1\,m_1 \\ l_2^2 & m_2^2 & n_2^2 & 2\,l_2\,n_2 & 2\,m_2\,n_2 & 2\,l_2\,m_2 \\ l_3^2 & m_3^2 & n_3^2 & 2\,l_3\,n_3 & 2\,m_3\,n_3 & 2\,l_3\,m_3 \\ l_1\,l_3 & m_1\,m_3 & n_1\,n_3 & l_1\,n_3+l_3\,n_1 & m_1\,n_3+m_3\,n_1 & l_1\,m_3+l_3\,m_1 \\ l_2\,l_3 & m_2\,m_3 & n_2\,n_3 & l_2\,n_3+l_3\,n_2 & m_2\,n_3+m_3\,n_2 & l_2\,m_3+l_3\,m_2 \\ l_1\,l_2 & m_1\,m_2 & n_1\,n_2 & l_1\,n_2+l_2\,n_1 & m_1\,n_2+m_2\,n_1 & l_1\,m_2+l_2\,m_1 \end{bmatrix} \tag{3.9}$$

This transformation matrix in eq. (3.9) relates the piezoresistive coefficients in the rotated

coordinate system, to those in the crystallographic coordinate system.

The direction cosines l_i, m_i, and n_i in eq. (3.9) are given by

$$\begin{bmatrix} l_1 & m_1 & n_1 \\ l_2 & m_2 & n_2 \\ l_3 & m_3 & n_3 \end{bmatrix} = \begin{bmatrix} a_{11} & a_{12} & a_{13} \\ a_{21} & a_{22} & a_{23} \\ a_{31} & a_{32} & a_{33} \end{bmatrix} = [a_{ij}] \tag{3.10}$$

18

where

$$a_{ij} = \cos(x'_i, x_j) \tag{3.11}$$

The inverse of the matrix in eq. (3.9) is needed for calculation of the off-axis piezoresistive coefficients in eq. (3.7). It can be evaluated as:

$$[T_{\alpha\beta}]^{-1} = \begin{bmatrix} l_1^2 & l_2^2 & l_3^2 & 2\,l_1\,l_3 & 2\,l_2\,l_3 & 2\,l_1\,l_2 \\ m_1^2 & m_2^2 & m_3^2 & 2\,m_1\,m_3 & 2\,m_2\,m_3 & 2\,m_1\,m_2 \\ n_1^2 & n_2^2 & n_3^2 & 2\,n_1\,n_3 & 2\,n_2\,n_3 & 2\,n_1\,n_2 \\ l_1\,n_1 & l_2\,n_2 & l_3\,n_3 & l_1\,n_3 + l_3\,n_1 & l_2\,n_3 + l_3\,n_2 & l_1\,n_2 + l_2\,n_1 \\ m_1\,n_1 & m_2\,n_2 & m_3\,n_3 & m_1\,n_3 + m_3\,n_1 & m_2\,n_3 + m_3\,n_2 & m_1\,n_2 + m_2\,n_1 \\ l_1\,m_1 & l_2\,m_2 & l_3\,m_3 & l_1\,m_3 + l_3\,m_1 & l_2\,m_3 + l_3\,m_2 & l_1\,m_2 + l_2\,m_1 \end{bmatrix} \tag{3.12}$$

If the arbitrary primed coordinate system coincides with the crystallographic axes, the matrices in eqs. (3.9, 3.12) become the 6 x 6 identity matrix, and eq. (3.7) simplifies to

$$\pi'_{\alpha\beta} = \pi_{\alpha\beta} \tag{3.13}$$

Additionally, when the two coordinate systems are aligned, Equation (3.4) simplifies to

$$\begin{aligned} \frac{\Delta R}{R} &= [\pi_{11}\sigma_{11} + \pi_{12}(\sigma_{22} + \sigma_{33})]l^2 + [\pi_{11}\sigma_{22} + \pi_{12}(\sigma_{11} + \sigma_{33})]m^2 \\ &\quad + [\pi_{11}\sigma_{33} + \pi_{12}(\sigma_{11} + \sigma_{22})]n^2 + 2\,\pi_{44}[\sigma_{12}\,lm + \sigma_{13}\,ln + \sigma_{23}\,mn] \\ &\quad + [\alpha_1 T + \alpha_2 T^2 + ...] \end{aligned} \tag{3.14}$$

where l, m, and n are the direction cosines of the conductor orientation with respect to the crystallographic axes. Equation (3.14) describes the normalized resistance change of an arbitrarily oriented silicon conductor as a function of all six stress components in the crystallographic coordinate system.

3.2 Piezoresistivity in the (111) Silicon Plane

A generalized schematic of a (111) silicon wafer is shown in Figure 3.2. A wafer plane is defined by the direction normal to its surface. Therefore, a (111) silicon wafer has the [111] crystallographic direction as its normal. The principal unprimed crystallographic axes mentioned previously are not found in the (111) plane. In this plane, the rotated coordinate system has been chosen so that the x_1' direction is parallel to the wafer flat, and the x_2' direction is perpendicular to the flat. In order to find resistance changes of a conductor in this plane using eq. (3.4), the direction cosines must be found between the rotated, primed coordinate system of the wafer plane, and the unprimed coordinate system formed by the principal crystallographic axes. The appropriate matrix of direction cosines for the (111) wafer plane can be found to be [46]

$$[a_{ij}] = \begin{bmatrix} \dfrac{1}{\sqrt{2}} & -\dfrac{1}{\sqrt{2}} & 0 \\[2mm] \dfrac{1}{\sqrt{6}} & \dfrac{1}{\sqrt{6}} & -\dfrac{2}{\sqrt{6}} \\[2mm] \dfrac{1}{\sqrt{3}} & \dfrac{1}{\sqrt{3}} & \dfrac{1}{\sqrt{3}} \end{bmatrix} \tag{3.15}$$

Using these values in eqs. (3.9, 3.10 3.11), the off-axis piezoresistive coefficients $\pi'_{\alpha\beta}$ found in Equation (3.7) can be calculated. These coefficients can be substituted in eq. (3.4) to produce

$$\begin{aligned} \frac{\Delta R}{R} = {}& [B_1 \sigma'_{11} + B_2 \sigma'_{22} + B_3 \sigma'_{33} + 2\sqrt{2}(B_3 - B_2)\sigma'_{23}]\cos^2\phi \\ & + [B_2 \sigma'_{11} + B_1 \sigma'_{22} + B_3 \sigma'_{33} - 2\sqrt{2}(B_3 - B_2)\sigma'_{23}]\sin^2\phi \\ & + [2\sqrt{2}(B_3 - B_2)\sigma'_{13} + (B_1 - B_2)\sigma'_{12}]\sin 2\phi \\ & + [\alpha_1 T + \alpha_2 T^2 + \ldots] \end{aligned} \tag{3.16}$$
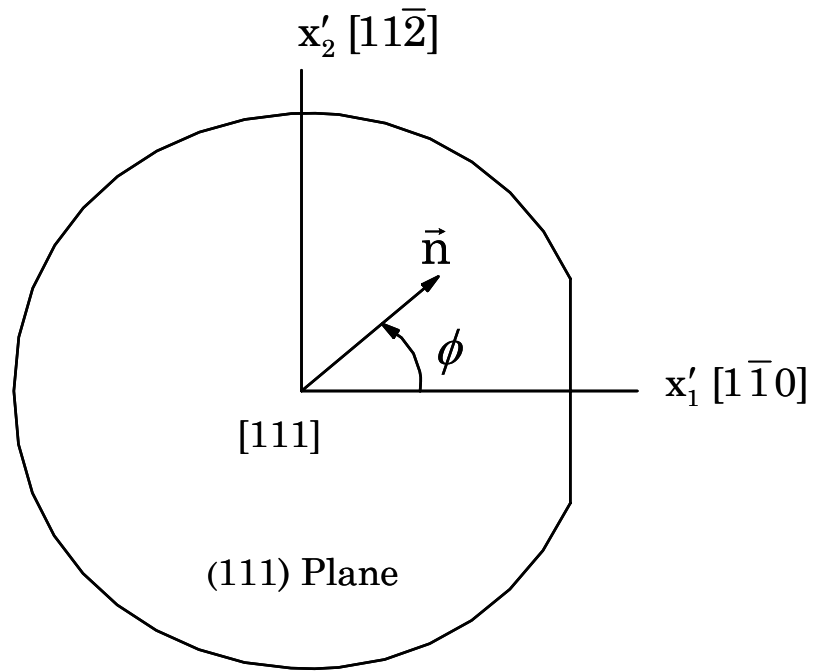
20

Figure 3.2 - (111) Silicon Wafer

where ϕ is the angle between the x_1'-axis and the conductor orientation. The coefficients B_i (i = 1, 2, 3) are linearly independent constants comprised of a combination of the piezoresistive coefficients evaluated in the unprimed crystallographic coordinate system, and are expressed as

$$B_1 = \frac{\pi_{11} + \pi_{12} + \pi_{44}}{2}$$
$$B_2 = \frac{\pi_{11} + 5\pi_{12} - \pi_{44}}{6} \qquad (3.17)$$
$$B_3 = \frac{\pi_{11} + 2\pi_{12} - \pi_{44}}{3}$$

It is important to note that these constants are temperature dependant and must be calibrated prior to measurement of resistance changes for use in stress calculations.

Equation (3.16) shows that the resistance changes of a silicon conductor in the (111) wafer plane is a function of all six components of the stress tensor. This feature of the (111) plane has been utilized to create sensor rosettes for measurement of the complete state of stress at a point. It will also be shown in the next chapter that rosettes made using (111) wafers can be designed to measure four stress quantities that can be evaluated without measurement of the temperature change T. It has been shown that errors in temperature measurement have a great effect on the calculated stress values, and the ability to measure stress components directly from resistance values is invaluable [72].

CHAPTER 4

(111) SILICON TEST CHIPS

4.1   Rosette and Test Chip Designs

4.1.1   Optimized Eight- Element Rosette

The eight-element (111) silicon rosette shown in Figure 4.1 has been developed at

Auburn University to measure the complete state of stress on the surface of a packaged

semiconductor die. The rosette is dual polarity, meaning that it uses both n-type and p-

type serpentine silicon sensors. Only three unique resistance change measurements can be

made for a group of sensors of one doping type and doping level combination in a single

plane [45]. This fact brings about the need for two doping types present in one sensor

rosette. It is also noted that only six resistors are required for measurement of the state of

stress using (111) silicon. The sensors oriented at -45° are not necessary, but aid in

making bridge measurement easier and in localizing stress measurement [81].

The complete rosette is comprised of eight elements, four of each doping type

oriented at $\phi = 0°$, $\pm 45°$, and 90° with respect to the x_1'-axis. Applying eq. (3.16) to each

of the sensors leads to the following equations for the normalized resistance change of

each sensor as a function of the stress components:
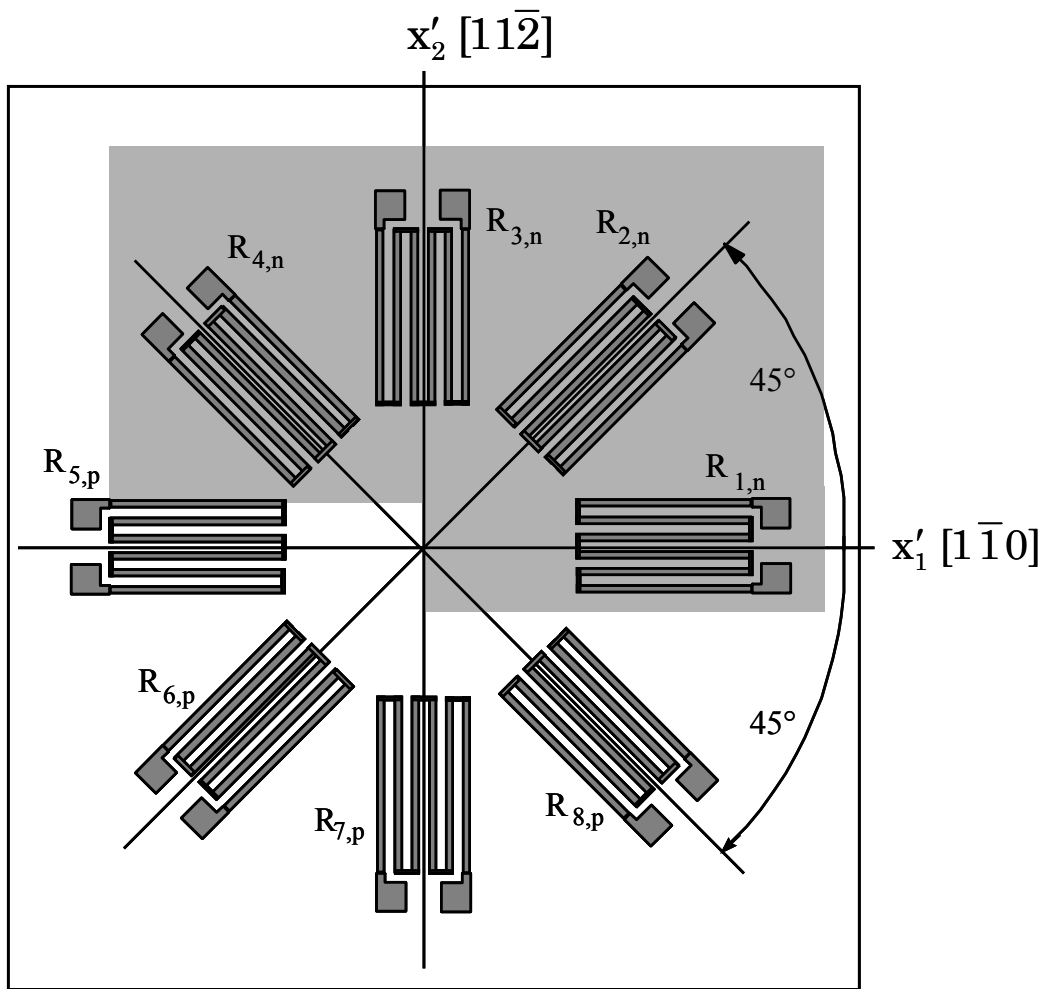
Figure 4.1 - Optimized Eight-Element Rosette

$$\frac{\Delta R_1}{R_1} = B_1^n \sigma'_{11} + B_2^n \sigma'_{22} + B_3^n \sigma'_{33} + 2\sqrt{2}(B_3^n - B_2^n)\sigma'_{23}$$
$$+ [\alpha_1^n T + \alpha_2^n T^2 + ...]$$

$$\frac{\Delta R_2}{R_2} = \left(\frac{B_1^n + B_2^n}{2}\right)(\sigma'_{11} + \sigma'_{22}) + B_3^n \sigma'_{33} + 2\sqrt{2}(B_3^n - B_2^n)\sigma'_{13}$$
$$+ (B_1^n - B_2^n)\sigma'_{12} + [\alpha_1^n T + \alpha_2^n T^2 + ...]$$

$$\frac{\Delta R_3}{R_3} = B_2^n \sigma'_{11} + B_1^n \sigma'_{22} + B_3^n \sigma'_{33} - 2\sqrt{2}(B_3^n - B_2^n)\sigma'_{23}$$
$$+ [\alpha_1^n T + \alpha_2^n T^2 + ...]$$

(4.1)

$$\frac{\Delta R_4}{R_4} = \left(\frac{B_1^n + B_2^n}{2}\right)(\sigma'_{11} + \sigma'_{22}) + B_3^n \sigma'_{33} - 2\sqrt{2}(B_3^n - B_2^n)\sigma'_{13}$$
$$- (B_1^n - B_2^n)\sigma'_{12} + [\alpha_1^n T + \alpha_2^n T^2 + ...]$$

$$\frac{\Delta R_5}{R_5} = B_1^p \sigma'_{11} + B_2^p \sigma'_{22} + B_3^p \sigma'_{33} + 2\sqrt{2}(B_3^p - B_2^p)\sigma'_{23}$$
$$+ [\alpha_1^p T + \alpha_2^p T^2 + ...]$$

$$\frac{\Delta R_6}{R_6} = \left(\frac{B_1^p + B_2^p}{2}\right)(\sigma'_{11} + \sigma'_{22}) + B_3^p \sigma'_{33} + 2\sqrt{2}(B_3^p - B_2^p)\sigma'_{13}$$
$$+ (B_1^p - B_2^p)\sigma'_{12} + [\alpha_1^p T + \alpha_2^p T^2 + ...]$$

$$\frac{\Delta R_7}{R_7} = B_2^p \sigma'_{11} + B_1^p \sigma'_{22} + B_3^p \sigma'_{33} - 2\sqrt{2}(B_3^p - B_2^p)\sigma'_{23}$$
$$+ [\alpha_1^p T + \alpha_2^p T^2 + ...]$$

$$\frac{\Delta R_8}{R_8} = \left(\frac{B_1^p + B_2^p}{2}\right)(\sigma'_{11} + \sigma'_{22}) + B_3^p \sigma'_{33} - 2\sqrt{2}(B_3^p - B_2^p)\sigma'_{13}$$
$$- (B_1^p - B_2^p)\sigma'_{12} + [\alpha_1^p T + \alpha_2^p T^2 + ...]$$

Superscripts n and p are used on the combined piezoresistive coefficients, B_i (i =1, 2, 3), to denote n-type and p-type resistors, respectively.

For an arbitrary state of stress, inverting these equations allows the six stress components to be calculated in terms of the measured resistance and temperature changes:

$$\sigma'_{11} = \frac{(B_3^p - B_2^p)\left[\frac{\Delta R_1}{R_1} - \frac{\Delta R_3}{R_3}\right] - (B_3^n - B_2^n)\left[\frac{\Delta R_5}{R_5} - \frac{\Delta R_7}{R_7}\right]}{2[(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n]}$$
$$+ \frac{B_3^p\left[\frac{\Delta R_1}{R_1} + \frac{\Delta R_3}{R_3} - 2\alpha_1^n T\right] - B_3^n\left[\frac{\Delta R_5}{R_5} + \frac{\Delta R_7}{R_7} - 2\alpha_1^p T\right]}{2[(B_1^n + B_2^n)B_3^p - (B_1^p + B_2^p)B_3^n]}$$

$$\sigma'_{22} = -\frac{(B_3^p - B_2^p)\left[\frac{\Delta R_1}{R_1} - \frac{\Delta R_3}{R_3}\right] - (B_3^n - B_2^n)\left[\frac{\Delta R_5}{R_5} - \frac{\Delta R_7}{R_7}\right]}{2[(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n]}$$
$$+ \frac{B_3^p\left[\frac{\Delta R_1}{R_1} + \frac{\Delta R_3}{R_3} - 2\alpha_1^n T\right] - B_3^n\left[\frac{\Delta R_5}{R_5} + \frac{\Delta R_7}{R_7} - 2\alpha_1^p T\right]}{2[(B_1^n + B_2^n)B_3^p - (B_1^p + B_2^p)B_3^n]}$$

$$\sigma'_{33} = \frac{-(B_1^p + B_2^p)\left[\frac{\Delta R_1}{R_1} + \frac{\Delta R_3}{R_3} - 2\alpha_1^n T\right] + (B_1^n + B_2^n)\left[\frac{\Delta R_5}{R_5} + \frac{\Delta R_7}{R_7} - 2\alpha_1^p T\right]}{2[(B_1^n + B_2^n)B_3^p - (B_1^p + B_2^p)B_3^n]} \quad (4.2)$$

$$\sigma'_{13} = \frac{\sqrt{2}}{8}\left[\frac{(B_1^p - B_2^p)\left[\frac{\Delta R_4}{R_4} - \frac{\Delta R_2}{R_2}\right] - (B_1^n - B_2^n)\left[\frac{\Delta R_8}{R_8} - \frac{\Delta R_6}{R_6}\right]}{(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n}\right]$$

$$\sigma'_{23} = \frac{\sqrt{2}}{8}\left[\frac{-(B_1^p - B_2^p)\left[\frac{\Delta R_1}{R_1} - \frac{\Delta R_3}{R_3}\right] + (B_1^n - B_2^n)\left[\frac{\Delta R_5}{R_5} - \frac{\Delta R_7}{R_7}\right]}{(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n}\right]$$

$$\sigma'_{12} = \frac{-(B_3^p - B_2^p)\left[\frac{\Delta R_4}{R_4} - \frac{\Delta R_2}{R_2}\right] + (B_3^n - B_2^n)\left[\frac{\Delta R_8}{R_8} - \frac{\Delta R_6}{R_6}\right]}{2[(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n]}$$

In order to calculate the normal stress components $\sigma'_{11}, \sigma'_{22}, \sigma'_{33}$, the normalized resistance changes and the temperature change T of the resistors must me measured. The piezoresistive coefficients and temperature coefficients of resistance for each doping type

must also be known.   Calibration of the piezoresistive coefficients and of the Temperature Coefficients of Resistance (TCR) will be discussed later in this chapter.

Upon examination of eqs. (4.2), it can be seen that the shear stresses $\sigma'_{12}, \sigma'_{13}, \sigma'_{23}$ can be evaluated from only the resistance change measurements, and that it is not necessary to know the temperature change T.   Such measurements are referred to as being temperature compensated.   In addition to the three shear stresses, another temperature compensated stress quantity can be determined by subtracting the expressions for the in-plane normal stresses σ'_{11} and σ'_{22} in eqs. (4.2):

$$\sigma'_{11} - \sigma'_{22} = \frac{(B_3^p - B_2^p)\left[\dfrac{\Delta R_1}{R_1} - \dfrac{\Delta R_3}{R_3}\right] - (B_3^n - B_2^n)\left[\dfrac{\Delta R_5}{R_5} - \dfrac{\Delta R_7}{R_7}\right]}{[(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n]} \tag{4.3}$$

In all cases where temperature compensation occurs, it has been assumed that the TCRs for sensors of the same doping type are well matched.

The use of temperature compensated stress quantities has been encouraged by Jaeger, et al. [53], due to the difficulties in measuring temperature changes accurately over any extended period of time.   These authors further showed that the errors in the calculated stresses could be substantial given a temperature measurement error of as little as 0.25 °C.

4.1.2   Area Array Stress Test Chip

The (111) silicon test chips utilized in this thesis contained piezoresistive sensor rosettes that were capable of measuring the complete state of stress at the die surface. The test chips were 20 x 20 x .625 mm in size, and contained an area array of 3600 SAC387 lead free solder bumps on a 300 micron pitch. A photograph of one of the test chips is shown in Figure 4.2. Each of the 20 x 20 mm area array stress test chips used in this work contained
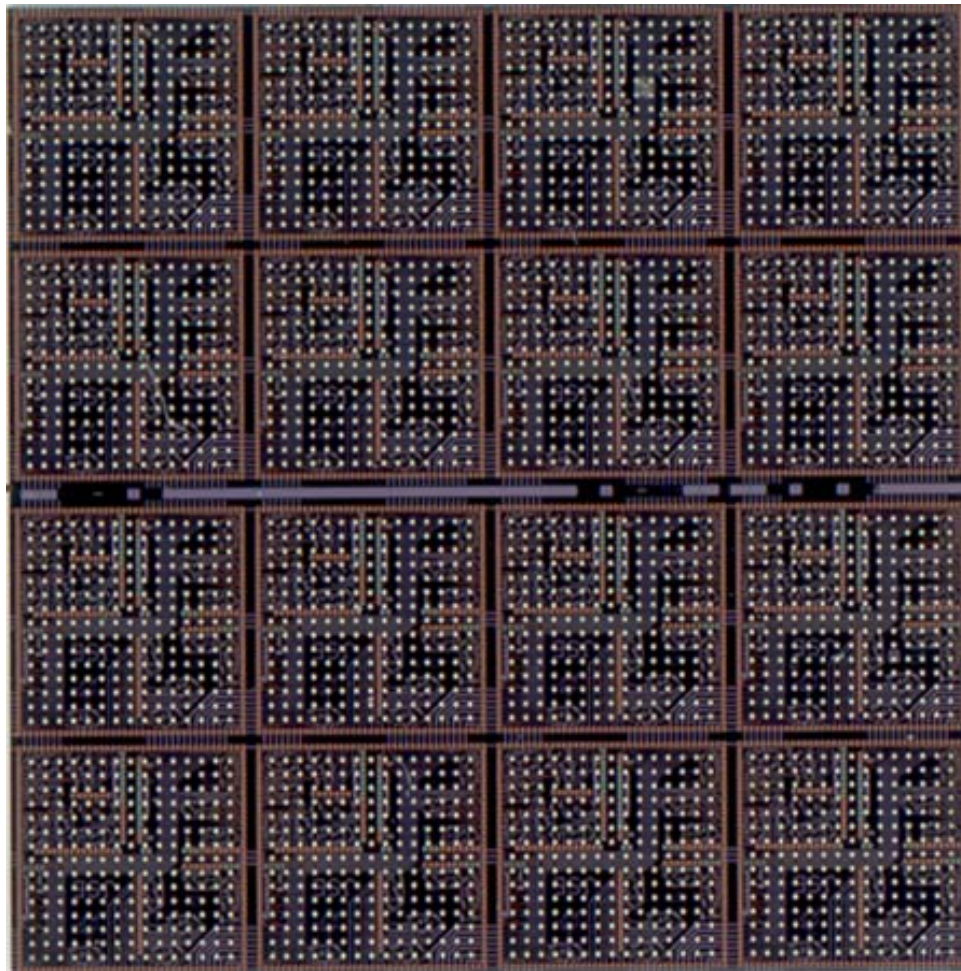
Figure 4.2 – Area Array Flip Chip Stress Test Chip [20 x 20 mm, 3600 I/O]

16 (4 x 4 array) of identical 5 x 5 mm regions as shown in Figure 4.3. The area array flip chip test chip wafers were obtained by redistributing an existing set of wirebond stress test chip wafers, and then subsequently bumping the topside metal layers of the redistributed wafers. The basic 5 x 5 mm wirebond stress test chip design (JSE WB200) found on the original wafers is shown in Figure 4.4. These test chips were designed specifically for wire bonding applications with 4 x 4 mil (100 x 100 μm) perimeter pads on a 5 mil (125 μm) pitch. Each WB200 test chip contains 16 optimized eight-element resistor rosettes for stress characterization, diodes for temperature measurement, a sub-surface heater across the full die area, and a fuse ID. All of the measurement functionality of the original test chip design is routed to the perimeter pads, and the redistribution procedure transferred this to an area array flip chip bond pad configuration. The details of the redistribution routing and solder bump placement over the same 5 x 5 mm region are shown in Figure 4.5. Figure 4.6 illustrates the 20 x 20 mm test chip before redistribution, and Figure 4.7 shows the redistribution metal layer that was added as well as the solder bump pad locations.

The eight stress sensor rosette elements are routed to the die bond pads in a manner that allows them to be configured as four two-element half-bridges in order to simplify the resistance change measurements. A fully ion-implanted bipolar process has been used in the original semiconductor device fabrication to balance the n- and p-type sheet resistances and resistor values, while maintaining high sensitivity to stress. Figure 4.8 illustrates an optical microscopy photograph of some sensor rosette sites and neighboring solder balls (black circles) on one of the final test chips. Figure 4.9 shows a close-up photograph of one of the eight-element sensor rosettes (no solder balls). It can be seen that the resistor sensors in this work are fairly large compared to the spacing of the solder balls. Thus, averaging of the
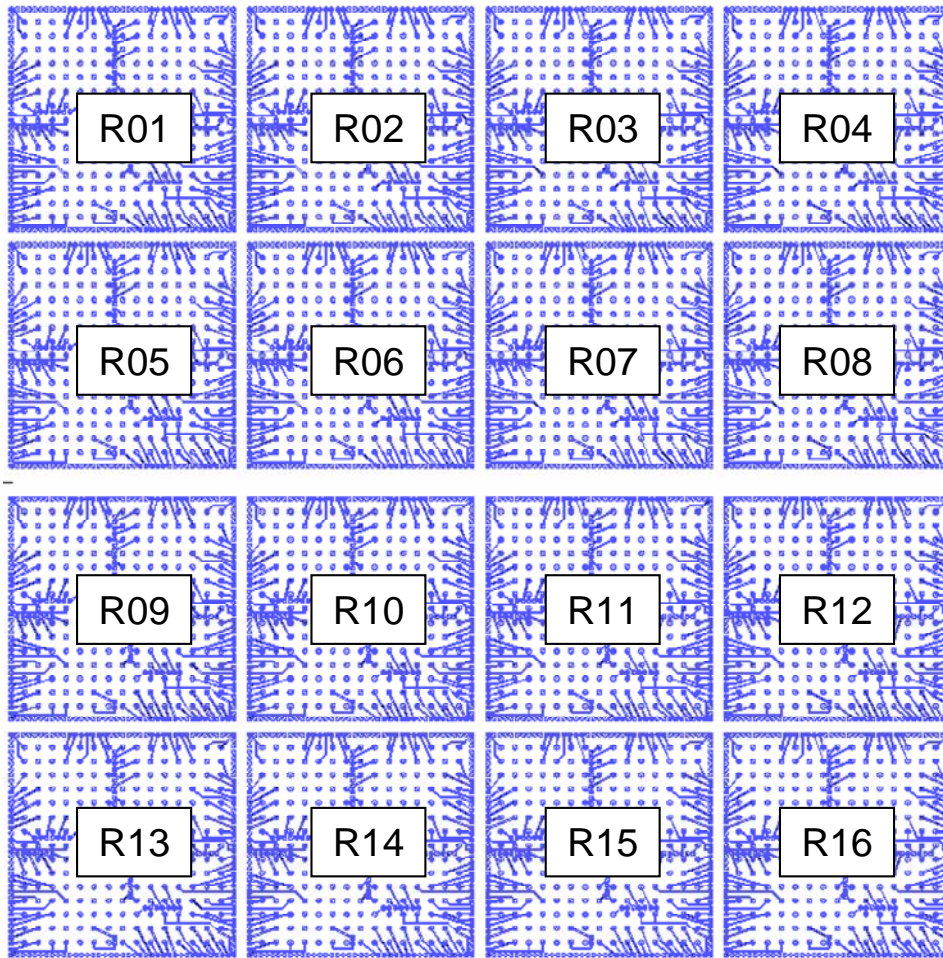
Figure 4.3 – Array of Identical 5 x 5 mm Regions
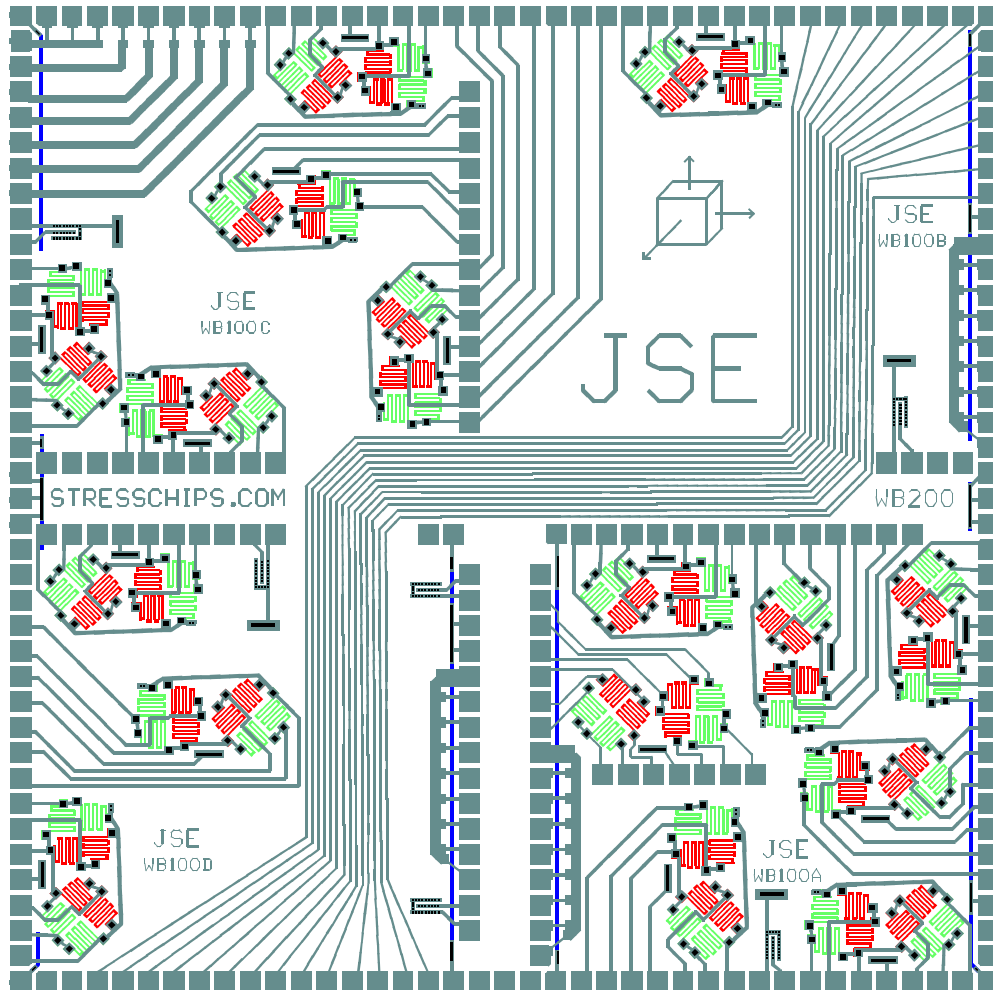
Figure 4.4 – Wirebond Stress Test Chip (JSE WB200)
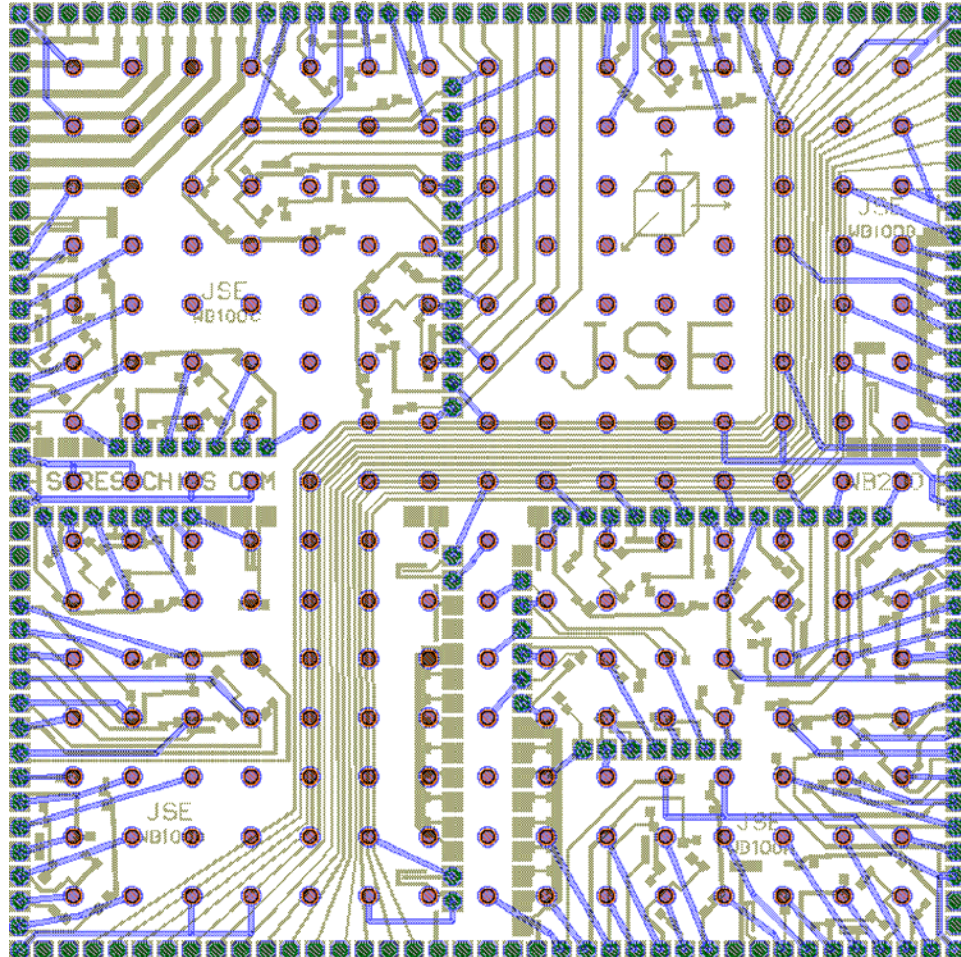
Figure 4.5 – Redistribution Pattern on each 5 x 5 mm Region

Figure 4.6 – 20 x 20 mm Test Chip Before Redistribution
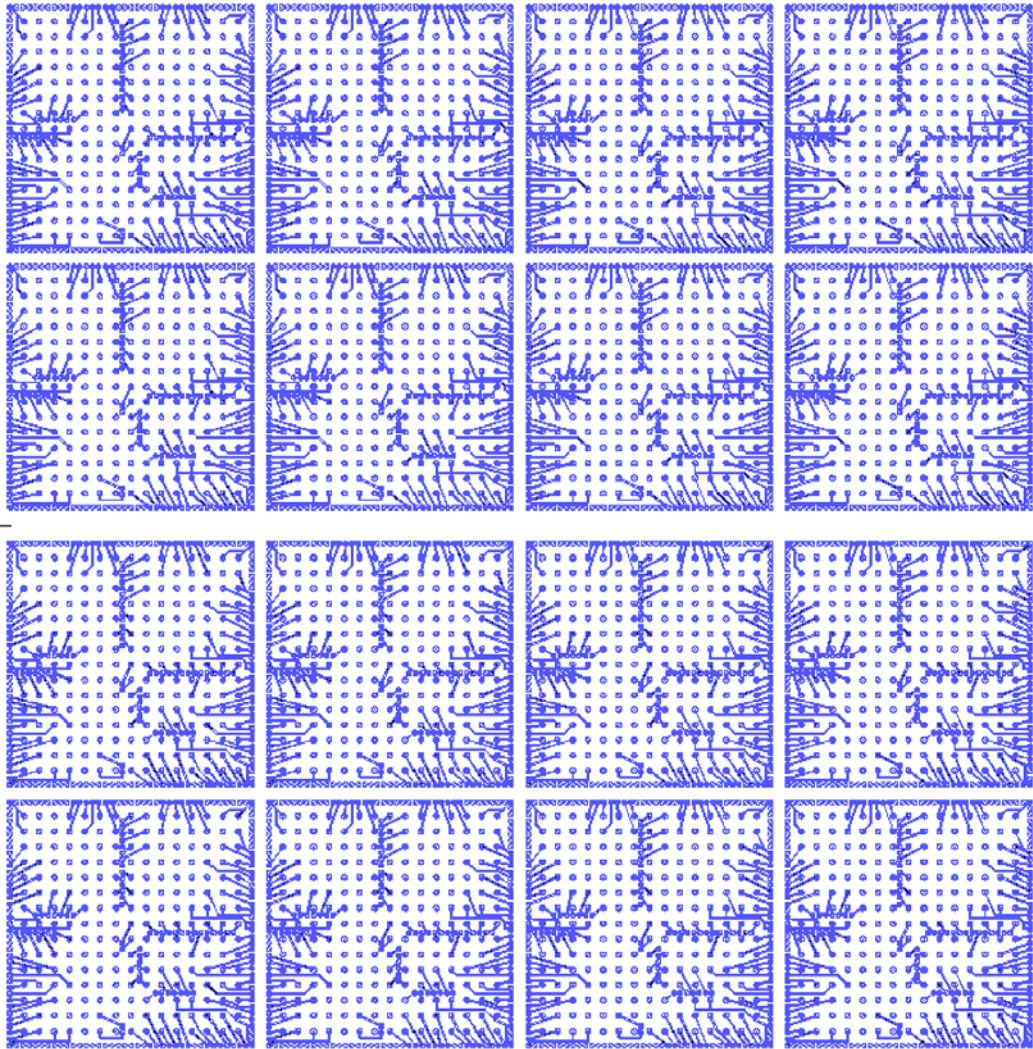
Figure 4.7 – Redistribution Metal Layer for 20 x 20 mm Test Chip
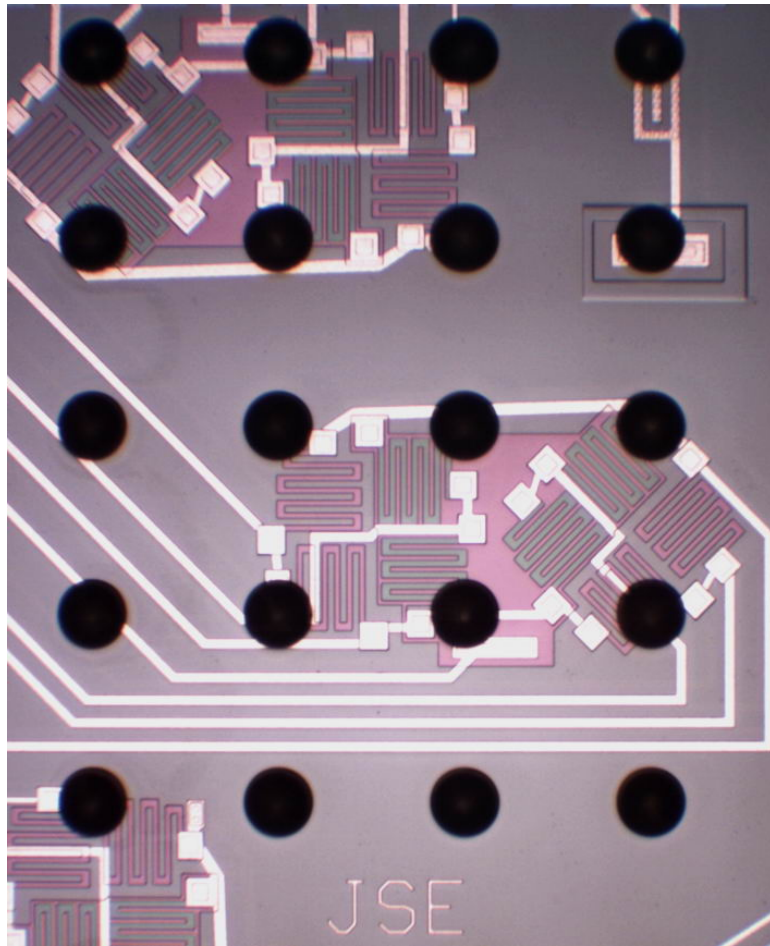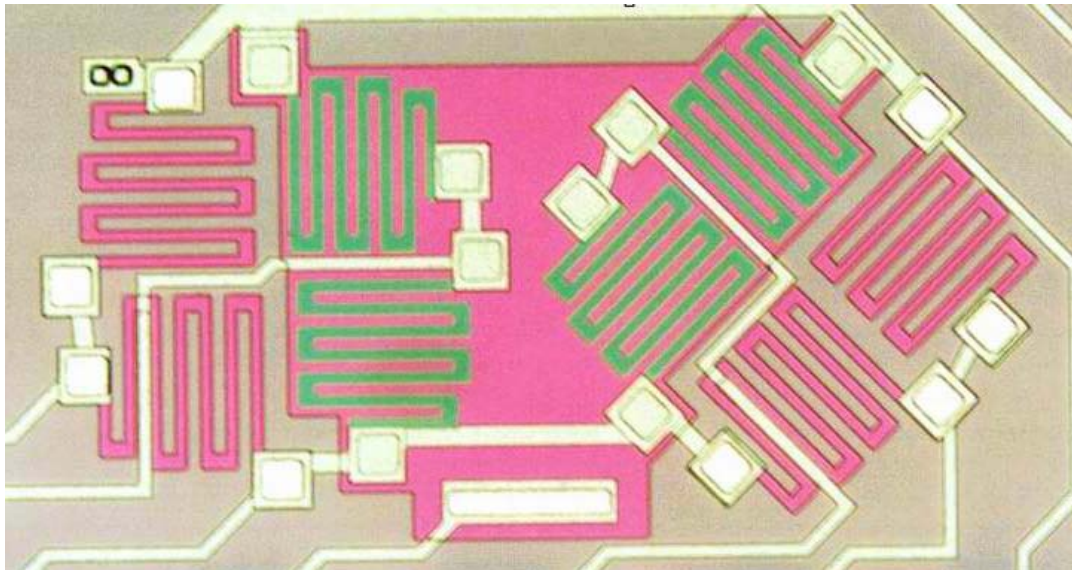
Figure 4.8 – Photograph of the Sensor Rosettes

Figure 4.9 – Close-Up Photograph of a Fabricated Rosette

stress distributions occurs over the rosette area and the sensors in this work will not be able to resolve any stress gradients that exist between solder balls. Ueta and Miura [114] have performed some initial measurements of this effect by placing 5 sensors elements between a pair of solder balls at the corner of a flip chip die.

4.2   Test Chip Calibration

4.2.1   Introduction

As noted earlier, the combined piezoresistive constants B_i (i =1, 2, 3) must be determined by a calibration procedure before the sensors can be used for measurement. To calibrate the six parameters, three for each doping type, both uniaxial and hydrostatic pressure tests are needed.

4.2.2   Four-Point Bending Calibration

The most common configuration for loading the device surface of a silicon test chip in uniaxial tension is four-point bending as shown in Figure 4.10 [46, 48]. A silicon wafer is cut into strips to generate the silicon beams. For the geometry shown in Figure 4.10, a uniaxial tensile state of stress is applied to the top surface of the beam given by:

$$\sigma = \frac{3F(L-d)}{t^2 h} \tag{4.4}$$

When the wafer strips are sliced perpendicular to the wafer flat so that the length of the beam coincides exactly with the x_1' direction of the wafer, the applied stress is by definition σ_{11}'. Using eq. (4.1), application of a known stress $\sigma = \sigma_{11}'$ leads to the following resistance changes in the 0-90° oriented sensors:

37
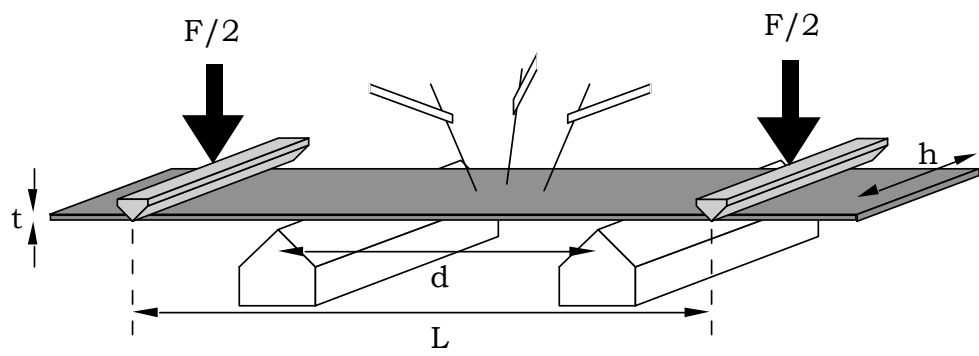
Figure 4.10 – Four-Point Bending Geometry

$$\frac{\Delta R_1}{R_1} = B_1^n \sigma + \alpha_1^n T \qquad \frac{\Delta R_3}{R_3} = B_2^n \sigma + \alpha_1^n T$$

$$\tag{4.5}$$

$$\frac{\Delta R_5}{R_5} = B_1^p \sigma + \alpha_1^p T \qquad \frac{\Delta R_7}{R_7} = B_2^p \sigma + \alpha_1^p T$$

Therefore, the combined piezoresistive constants B_1^p, B_2^p, B_1^n, B_2^n can be determined by applying uniaxial stress to wafer strip in a temperature controlled environment (T=0) and measuring the resulting resistance changes of the sensor rosettes.

As part of this study, strips were sliced along the x_1'-axis from the JSE-WB wafers. The strips measured 0.2 x 6.0 inches, and were stressed in the four-point bending fixture shown in Figure 4.11. The average piezoresistive coefficients B_1^p, B_2^p, B_1^n, B_2^n are shown in Table 4.1. The detailed calibration data are reported in Appendix A.

4.2.3   Hydrostatic Calibration and TCR Measurement

As discussed above, the piezoresistive coefficients B_1 and B_2 were calibrated by uniaxial testing using the four-point bending method. The third combined piezoresistive coefficient, B_3, was calibrated by applying hydrostatic pressure to a silicon chip. Under the application of hydrostatic state of pressure $(\sigma_{11}' = \sigma_{22}' = \sigma_{33}' = -p)$, eq. (4.1) can be used to show that the normalized resistance change on any sensor can be written in terms of piezoresistive coefficients and temperature change as:

$$\frac{\Delta R}{R} = -(B_1 + B_2 + B_3)p + \alpha_1 T = -(\pi_{11} + 2\pi_{12})p + \alpha_1 T = \pi_p p + \alpha_1 T \tag{4.6}$$

where π_p is the pressure coefficient defined by:

$$\pi_p = -(B_1 + B_2 + B_3) = -(\pi_{11} + 2\pi_{12}) \tag{4.7}$$
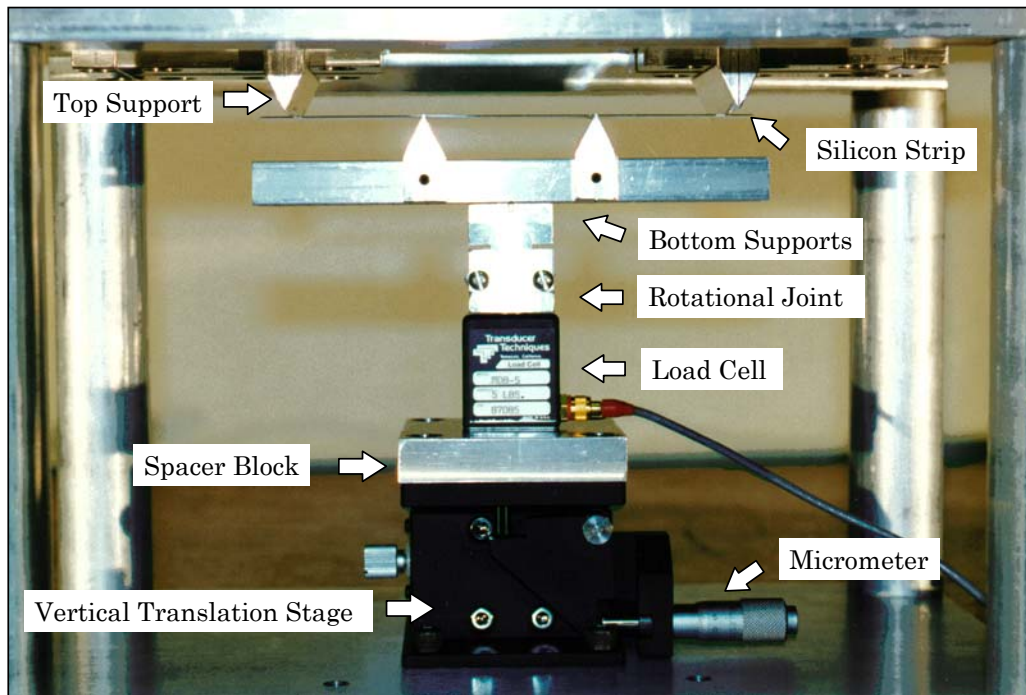
Figure 4.11 – Four-Point Bending Fixture

Test Chip	Piezoresistive Coefficients (1/TPa)					
	B_1^p	B_2^p	B_3^p	B_1^n	B_2^n	B_3^n
JSE - WB	368 (12)	-92 (7)	-452	-131 (11)	91 (16)	-76

Table 4.1 – Average Piezoresistive Coefficient Values and Standard Deviations

and the normalized resistance change is

$$\frac{\Delta R}{R} = \frac{R(\sigma,T) - R(0,0)}{R(0,0)}$$

(4.8)

Here, $R(\sigma,T)$ is the resistance measured during application of stress, and $R(0,0)$ is the resistance of the sensor in an unstressed condition. The pressure coefficient π_p can be obtained by applying hydrostatic pressure to a sensor and simultaneously measuring the resulting resistance and temperature changes.

For hydrostatic calibration, the high capacity pressure vessel shown in Figure 4.12 was employed to test several WB100 (2.5 x 2.5 mm) die. Each die was used in conjunction with a specially designed hydrostatic test Printed Circuit Board (PCB), as shown in Figure 4.13. A small dot of adhesive is placed on the PCB in a position where one corner of the WB100 chip would rest. The adhesive dot serves a dual purpose. First, it raises the chip off the PCB, allowing fluid to reach, and therefore apply pressure to every surface of the die. Second, the dot gives stability to the chip while it is wire-bonded to the PCB. After the adhesive dot is applied, the chip is set in place, and the assembly is cured, per the adhesive instructions. A bonded WB100 die on a hydrostatic PCB is shown in Figure 4.14. In this case, the glue dot is located in the lower left hand corner.

Before pressurizing the test die, TCR measurements are made. Equation 4.6 shows the dependence on temperature during hydrostatic measurements. It has previously been observed that the upper range of pressure applied in hydrostatic testing causes a temperature change of 0.8 °C [55]. Therefore, before the pressure coefficient π_p can be accurately evaluated, the temperature coefficient of resistance α_1 must also be

42
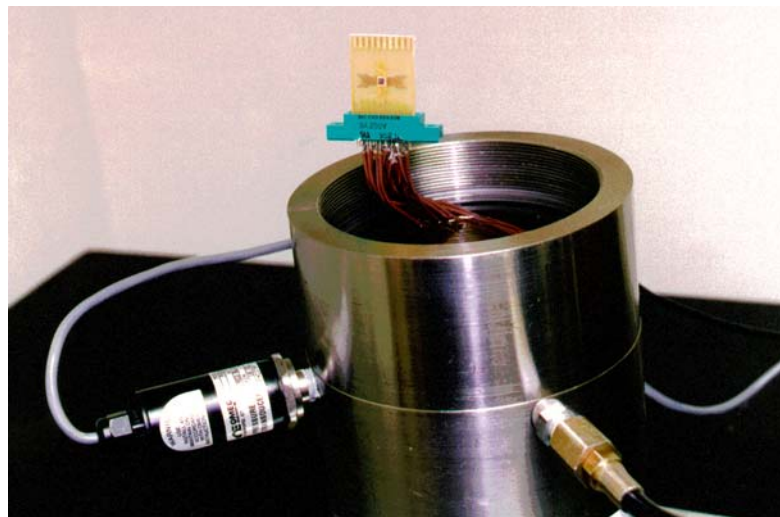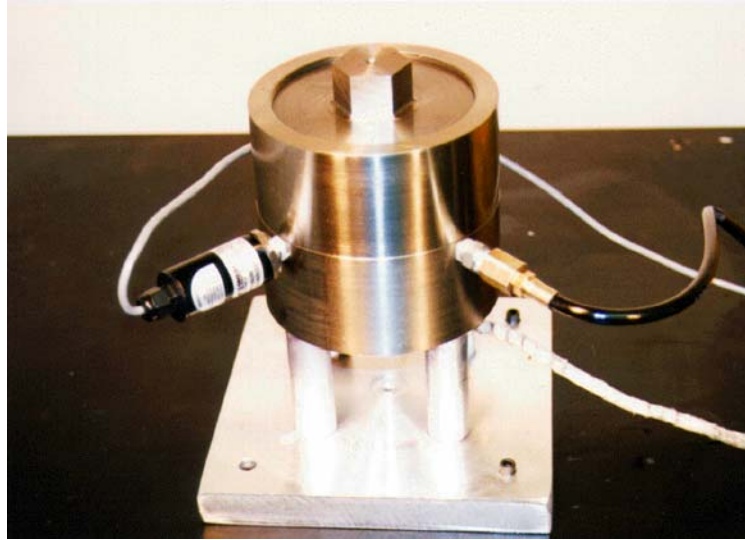
Figure 4.12 – Hydrostatic Pressure Vessel
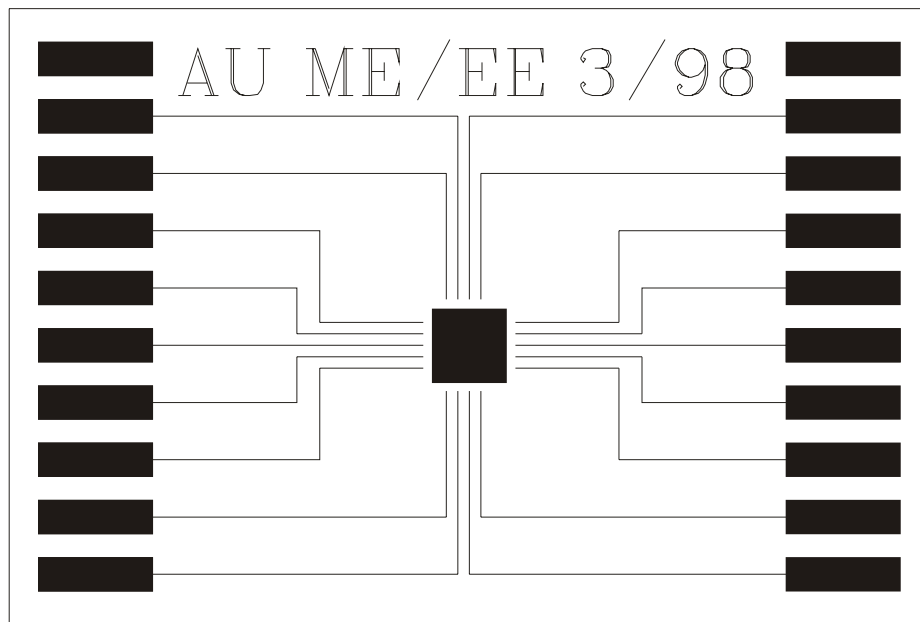
Figure 4.13 – Schematic of Hydrostatic PCB
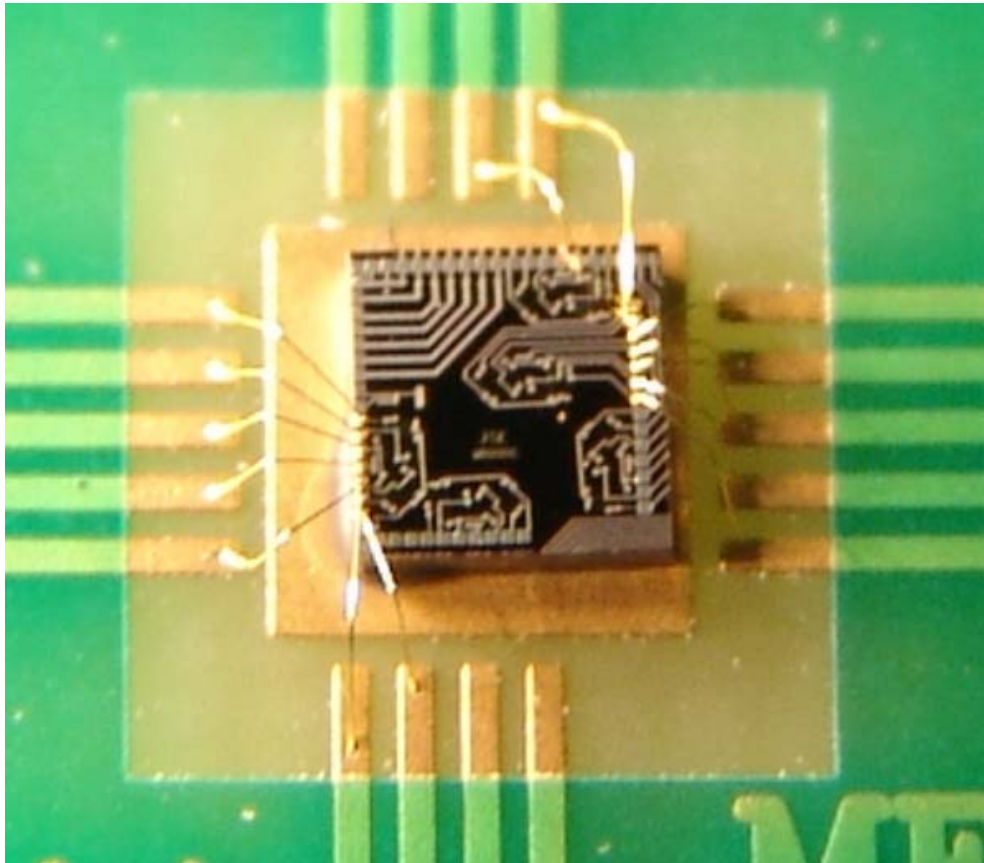
Figure 4.14 – Wire-Bonded WB100 Die for TCR and Hydrostatic Tests

measured. TCR measurements must be made on sensors when they are stress free, so that the resistance change is solely due to temperature effects:

$$\frac{\Delta R}{R} = \alpha_1 T \qquad (4.9)$$

The corner bonded chip, shown in Figure 4.14, satisfies the stress free requirement. The chips were placed in an environmental chamber and electrically connected to a data acquisition system. LabView software was used to control the chamber as well as measure temperature and resistance. Once electrically connected and in the chamber, the software lowered the temperature several degrees below room temperature, and then raised the temperature incrementally to well above room temperature while measuring resistance and temperature. Typical TCR data are shown in Figure 4.15. The slopes of the resistance change versus temperature change plots are the desired TCR = α_1 values.

When TCR measurements were completed for each sensor, the packages were placed in the pressure vessel shown in Figure 4.12. This configuration was developed by Kang, et al. [47, 55]. The complete hydrostatic setup is shown in Figure 4.16. After placing the bonded test die in the pressure vessel, the vessel was sealed. A Teflon gasket ensured that the liquid in the vessel did not leak and pressure was retained. Pressure was then applied using a mechanical hand pump. The resistance changes of all sensors were then recorded as well as the fluid temperature using a data acquisition system and LabView software. Typical hydrostatic data are shown in Figure 4.17. The top graph shows the raw resistance change versus pressure data as well as the calculated contribution due to temperature change. The difference of these two effects is plotted in the bottom graph, and represents only the contribution of pressure on the resistance

46

Normalized Resistance Change
Board #1, Site #1
Type - N, Orientation - 0°
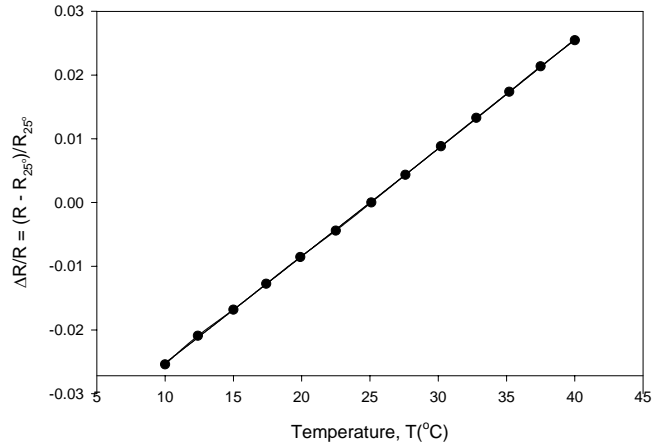
Normalized Resistance Change
Board #1, Site #2
Type: N, Orientation: 0°
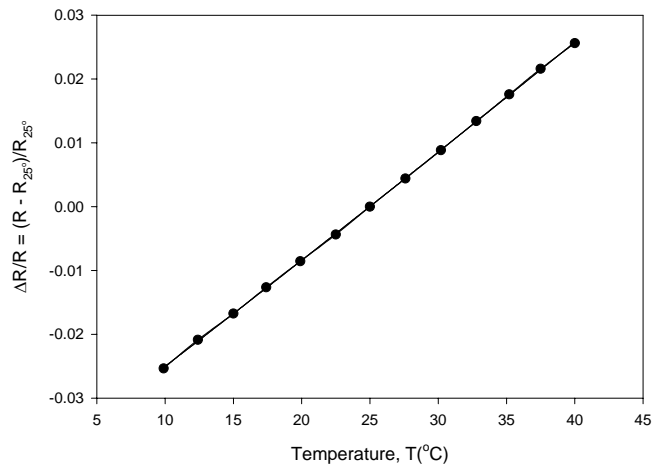
Figure 4.15 – Typical TCR Data
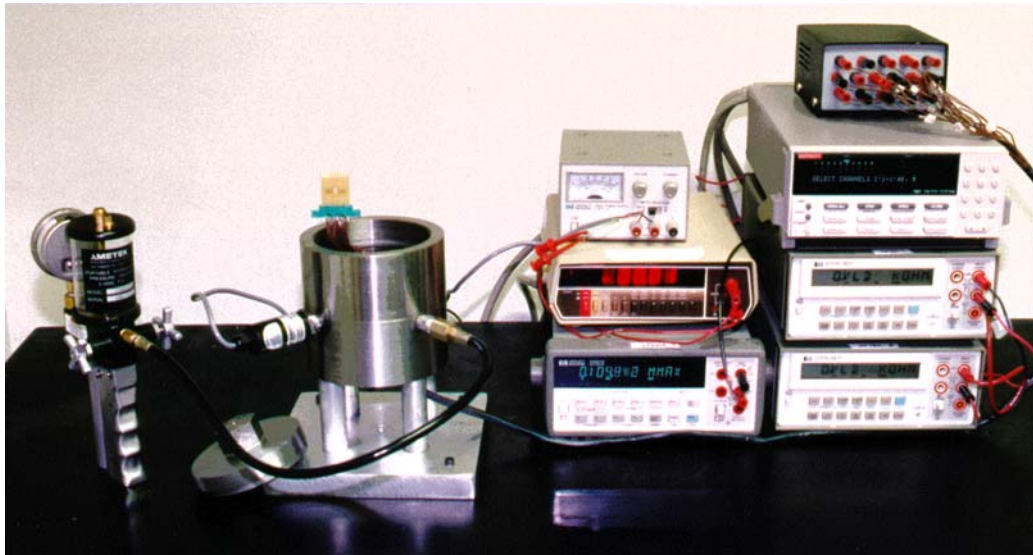
Figure 4.16 – Hydrostatic Test Setup

Hydrostatic Calibration Data
Resistance Change and Temperature Variation
N - Type Resistor, Orientation : 45 ^{0}
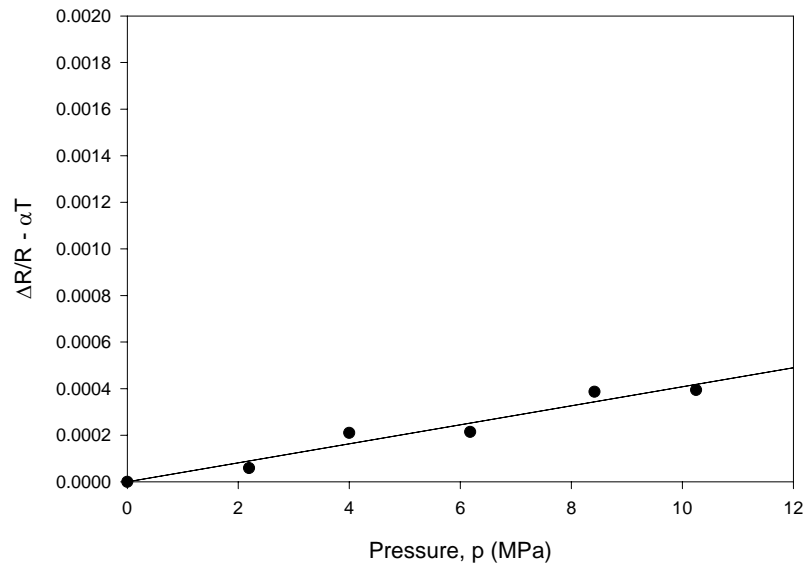Board # 1, Site # 1
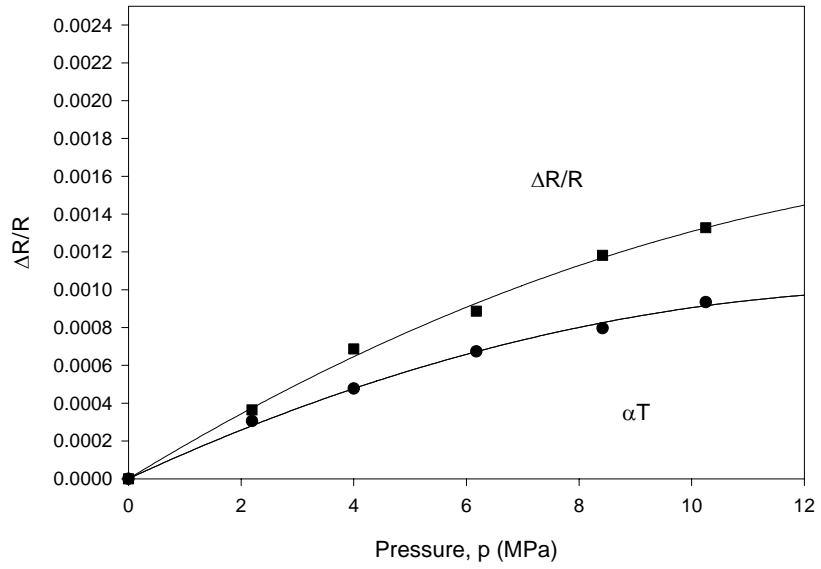
Adjusted Resistance Change

Figure 4.17 – Typical Hydrostatic Test Results

change of the sensors. The slope of the bottom graph is the desired pressure coefficient, which can be used to calculate coefficient B_3 using eq. (4.7). Average values for coefficients B_3^p and B_3^n are given in Table 4.1. Detailed hydrostatic calibration data are reported in Appendix B.

4.3 Resistance Measurement Procedure

4.3.1 Introduction

The (111) silicon test chips used in this study were fabricated using six inch wafers and a bipolar process. The wafers were passivated using silicon nitride, and then redistributed and solder bumped. The resistances of sensors on each 20 x 20 mm test chip were characterized at several different points including as bare die, and after various packaging steps including die attachment, underfill application, and lid attachment. The hardware and software used to make resistance measurements were designed by several previous Auburn University students including Zou [70], Rahim [101, 115], and H. Abdel-Hady. The utilized methods are briefly discussed below.

4.3.2 Resistance Measurements

The Test Chip Software utilizes GPIB interface technology to control the data acquisition system used for resistance measurement of sensor rosettes. In this study, initial resistance measurements were made at the chip level by probing, and subsequent measurements were made by inserting the packaged die into a test socket as discussed in the next chapter.

4.3.3 Test Measurement Equipment

The following is a list of equipment used for test measurement, as well as a description of how each item was used.

- Computer

A PC-based computer and a custom National Instruments LabView software program were used to control the data acquisition process. A logic chart and the program interface are shown in Figures 4.18 and 4.19 respectively.

- Keithley 7002 Switch System

Upon prompting from the control program, the switch turns on or off multiple channels in order to measure the resistance of successive resistors. Nine scanner cards were required for measurement of all of the devices on the test chip in this work.

- HP Multimeter #1

This multimeter measures current through a resistor.

- Power Supply

During measurement of sensors, the power supply provides voltage to the measured resistors, and also provides bias in the circuit to prevent current leakage. For ease of resistance measurement, the voltage used is 1V. Figure 4.20 illustrates the proper biasing on n-type and p-type resistors.

- HP Multimeter #2

This multimeter measures the exact voltage across each resistor. A side advantage of using a second multimeter is that by comparing this voltage to the bias voltage, one can check the circuit. The voltage measured by this meter is used in the calculation of resistance.

51
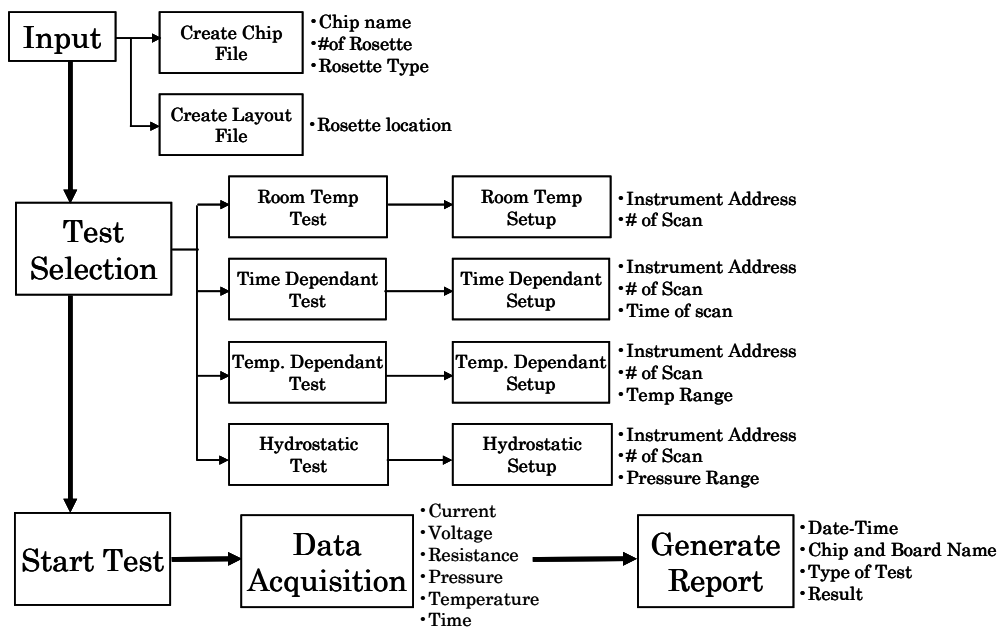
Figure 4.18 - Test Chip Software Logic
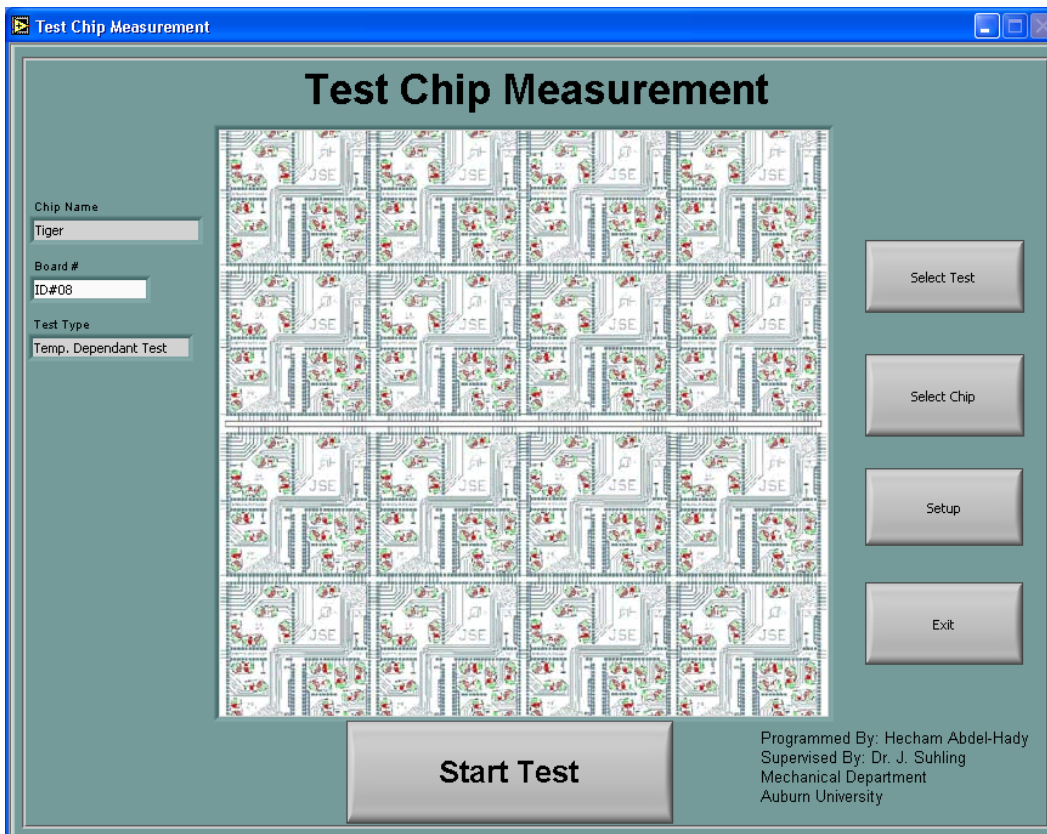
Figure 4.19 - Test Chip Measurement Software Interface
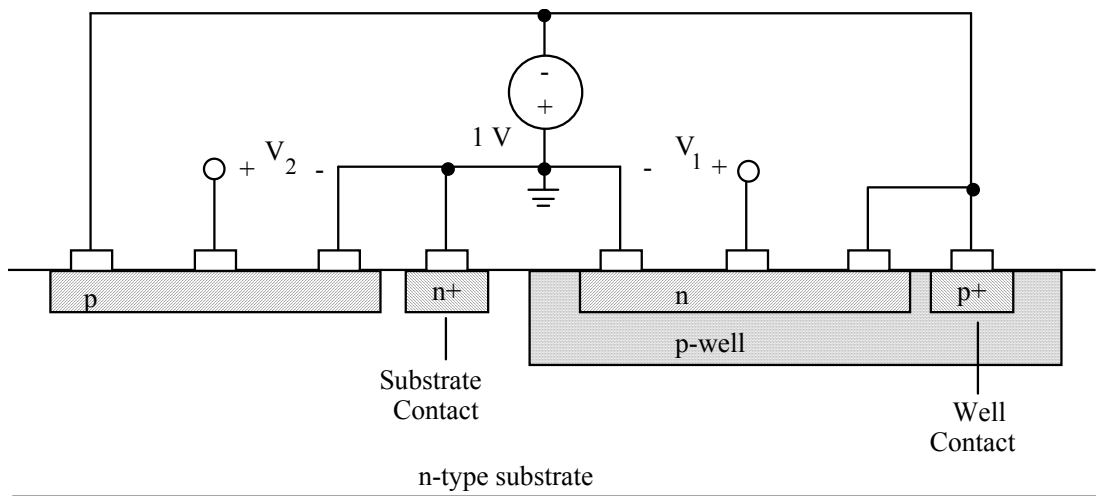
Figure 4.20 – Proper Biasing of Sensors

- HP Multimeter #3

This meter measures the resistance value from a resistance thermometer, otherwise referred to as a thermistor. The thermistor is placed on the die to measure temperature changes needed for stress and TCR measurements.

- Delta Design 9010 Environmental Chamber

As with the other equipment, the chamber is controlled through the Test Chip Software. During TCR calibration experiments, it is used to expose the chips to a range of temperatures in order to measure resistance over that range and calculate TCR. The chamber is also used to submit assembled packages to various temperature changes while measuring the sensor resistances.

- Accessories

For TCR measurements, two edge connectors were used to connect the PCB shown in Figure 4.13 to the data acquisition system electronically. For all other measurements, a special socket attached to a test board was used to electrically connect to the packages test chips. A package clamp was developed to secure the packages and ensure proper electrical contact. This arrangement is discussed in detail in the following chapter.

As discussed earlier, each rosette has eight sensors, four of each doping type. Figure 4.21 shows the two unique wiring configurations of sensor rosettes used in the test chip. The sensors are at angles of 0°, 90°,+45°, and -45° from the x_1'-direction. The resistors are denoted P1 (0°), P2 (90°), P3 (+45°), P4 (-45°), N1 (0°), N2 (90°), N3 (+45°), and N4 (-45°). Analogous sensors in the so-called Type 1 (horizontal) and Type 2 (vertical) rosettes are at different orientations. When comparing the two configurations, the

(Type 1)

(Type 2)
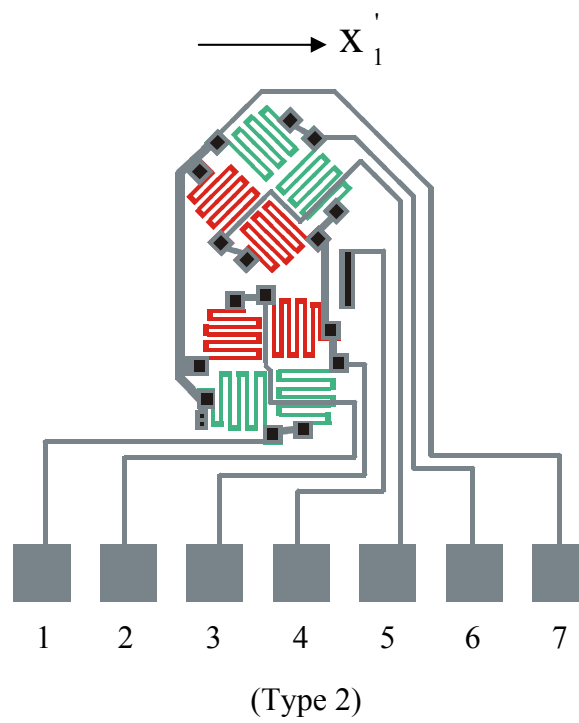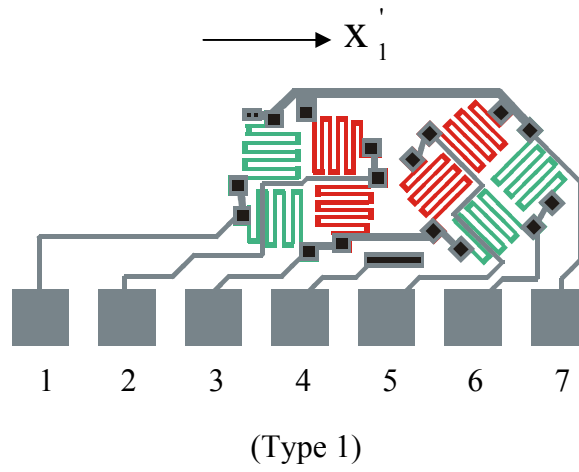
Figure 4.21 - Rosette Types 1 and 2

orientation of a particular rosette element will switch from 0° to 90°, or from +45° to -45°.

Using the resistor orientations defined above, Figure 4.22 shows a wiring schematic for each type of rosette. The numbers 1, 2, …,7 refer to the bond pad locations in the circuit. A voltage of 1 volt is applied across pads 3 and 7. In Figure 4.21, the methods utilized for measuring the resistances of sensor P1 in a Type 1 (horizontal) rosette and sensor P2 in a Type 2 (vertical) rosette are given. Referring to Figure 4.21, the multimeter (ammeter) serves as a shunt to prevent current from entering the lower sensor. Thus, the resistance of the upper sensor is simply the applied voltage of 1 V divided by the measured current.

The Keithley switch system is used to sequentially access various sensors on the test chip. This system uses interchangeable cards to connect to various devices. In this work, Keithley 7011S screw terminal cards were used to connect the wires from the test board and socket to the measurement equipment. Each scanner card has four banks, and each bank can measure one sensor rosette. Table 4.2 shows the connections between bonding pads, shown in Figure 4.21, and channels of the scanner card.

As shown in Figure 4.22, the 8 sensors in a rosette are configured as the parallel connection of four two-element half bridges. In this particular work, the individual resistor changes were measured directly utilizing the techniques shown in Figures 4.23 and 4.24, and as described above and shown in Figure 4.22. For the case in Figure 4.23, an ammeter is used to force the current in upper resistor R_U to bypass lower resistor R_L and flow through the ammeter. The ammeter must force the voltage across R_L to be zero

57
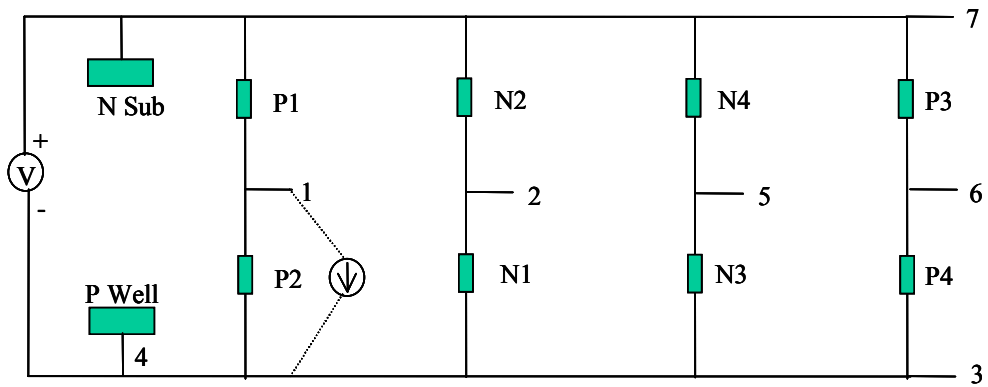
Wiring to Evaluate Sensor P1 in a Horizontal (Type 1) Rosette
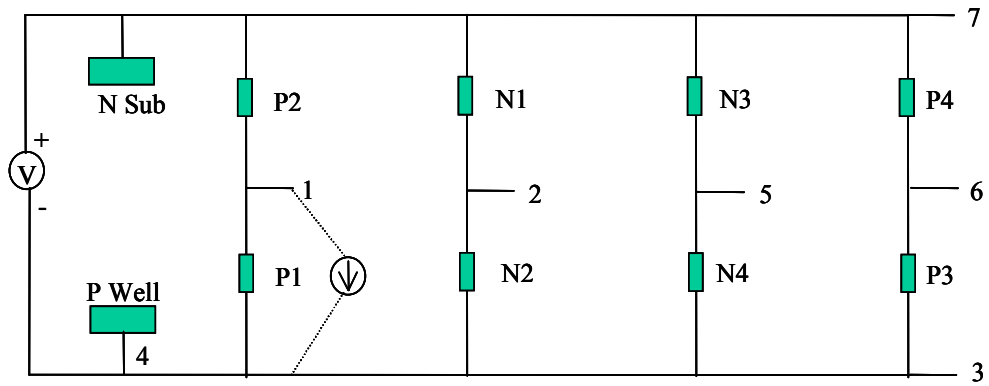
Wiring to Evaluate Sensor P2 in a Vertical (Type 2) Rosette

Figure 4.22 - Typical Wiring Diagram of Sensors used in JSE-WB Test Chips

Pad Number	Channel Status	
	H	L
7	1	
1	2	3
2	5	6
3, 4		4
5	7	8
6	9	10

Table 4.2 - Bonding Pad and Scanner Card Connections

and should be implemented using a high quality digital multimeter or an electrometer (such as the Keithley 6512). The circuit in Figure 4.24 functions in a similar manner. In this case the ammeter forces current in resistor R_U to be zero, and the measured current is due to resistor R_L acting alone.
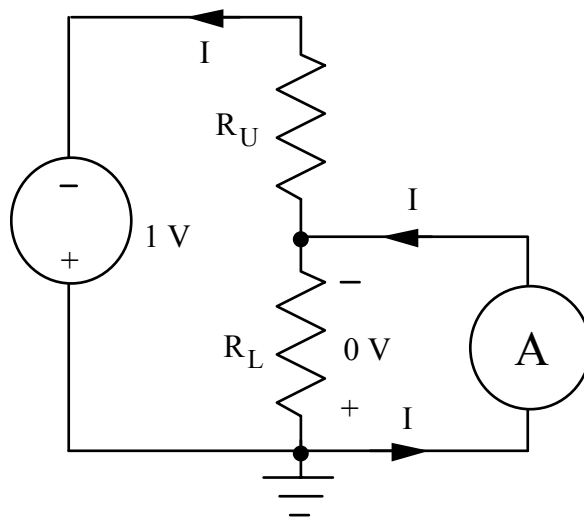
Figure 4.23 – Bias for Resistance Measurements – Upper Arm of Half Bridge
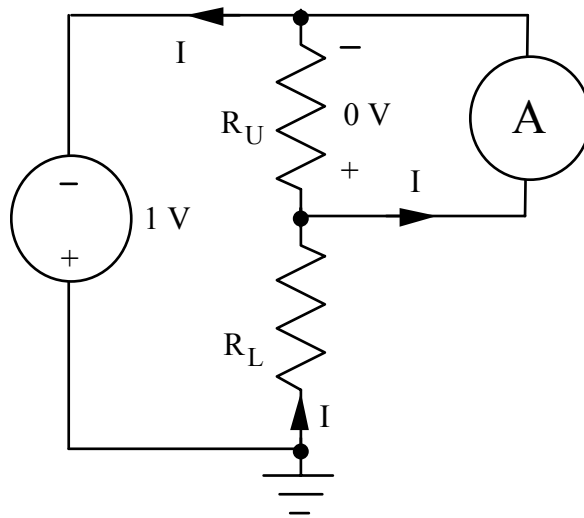
Figure 4.24 – Bias for Resistance Measurements – Lower Arm of Half Bridge

CHAPTER 5

DIE STRESS CHARACTERIZATION OF LARGE

AREA ARRAY FLIP CHIP PACKAGES

5.1　CBGA Package and Assembly Procedure

A total of 40 of the 20 x 20 mm flip chip stress test chips were assembled onto Ceramic Ball Grid Array (CBGA) substrates mimicking those used in high performance microprocessor packaging architectures (Figure 1.1). The manufacturing process was done in several steps including die attachment (flip chip solder joint reflow to the CBGA substrate), underfill dispense and cure, and lid attachment. Cross-sectional schematics of a test specimen at various stages in the assembly process are shown in Figure 5.1. Photographs of actual samples after the various steps in the manufacturing process are illustrated in Figure 5.2. The utilized high CTE ceramic substrates had in-plane dimensions of 51 x 51 mm, and a thickness of 2 mm.

Before packaging, the sensor resistances were measured by directly probing singulated chips from the test chip wafers. In the work of Rahim [101, 116], relatively small flip chip die were assembled to laminate substrates and it was found that the die stress states after solder joint reflow were universally small (e.g. 0-2 MPa). These stresses were then neglected and the initial "zero stress" resistance values were measured after the die were reflowed to the substrate. This had the advantage of avoiding the
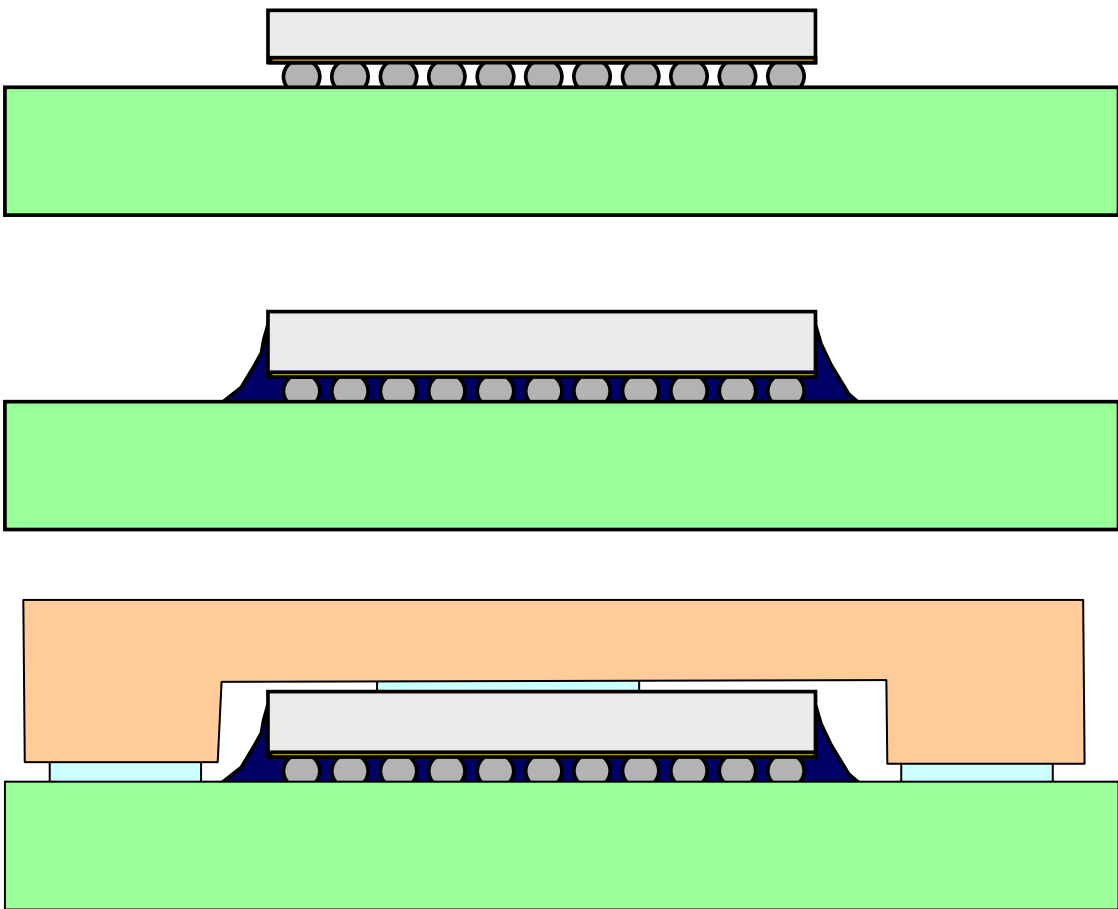
Figure 5.1 – Schematics of the CBGA Package at Various Points in the Assembly Process
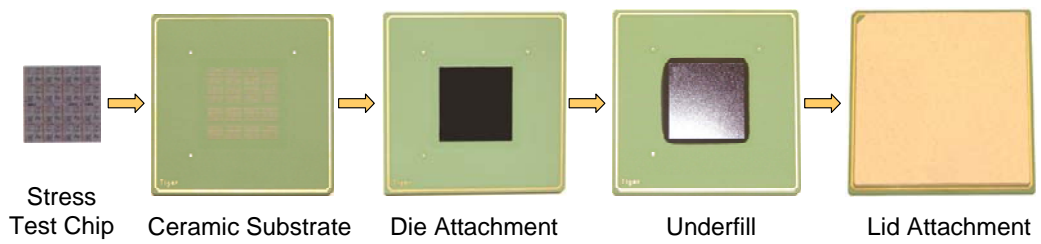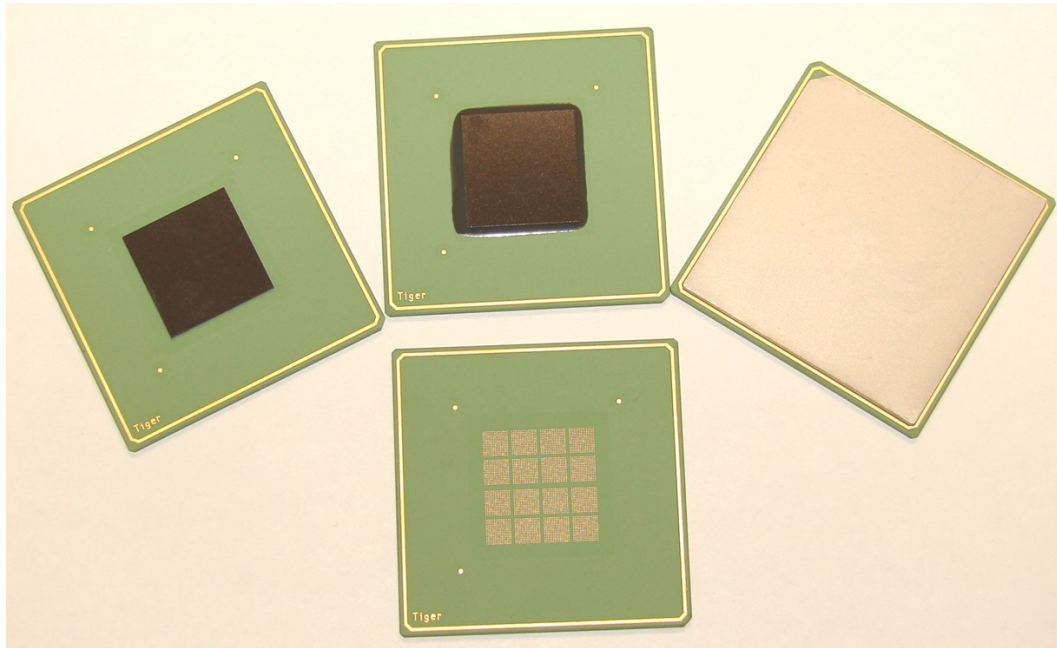
Figure 5.2 – CBGA Flip Chip Test Assemblies and Packaging Process Steps

complicated and tedious die probing procedure. However, for the large die and lead free solder bumps considered in this work, the die stresses induced by the solder reflow process were not negligible (see results in later sections). Thus, it was necessary to characterize the sensor resistances of each sensor element of the bare (unpackaged) die. The individually characterized chips were then reflowed to the ceramic substrates, and then subsequently underfilled and cured. Finally, a metallic lid (AlSiC) was attached to complete the ceramic LGA component. After every packaging step (solder reflow, underfill dispense and cure, lid attachment and adhesive cure), the sensor resistances were re-measured, so that the die stresses induced by each assembly operation could be characterized. In this work, all measurements were made at room temperature (22 $^{\circ}$C)

A total of 256 sensor rosettes (2048 piezoresistive sensor elements) were available for measurement on each 20 x 20 mm test chip. The total number of solder ball connections was 3600, and 2384 of them were used to access the piezoresistive sensors, diodes, heaters, and fuse IDs on the chip. In each of the 16 identical sub regions (see Figure 4.3), there were 149 active solder ball connections including 118 to access the piezoresistive sensors, 4 to access the diode temperature sensors, 18 to access the buried layer heater, and 9 to access a fuse ID. For this study, a subset of 36 rosettes was used for stress measurements. In addition, electrical access was maintained to the on-chip buried heater layer (for future power cycling measurements) and to an eight-bit fuse style chip-ID (for chip identification). The ceramic substrate was designed to only route 308 of the 2384 useful chip connections from its top (where the chip is attached) to its bottom (where it is connected to a PCB). These 308 active connection included 265 pads for piezoresistive sensors, 8 pads for diodes, 26 pads for connection to the heater, and 9 pads for the fuse ID. Figure 5.3 illustrates the
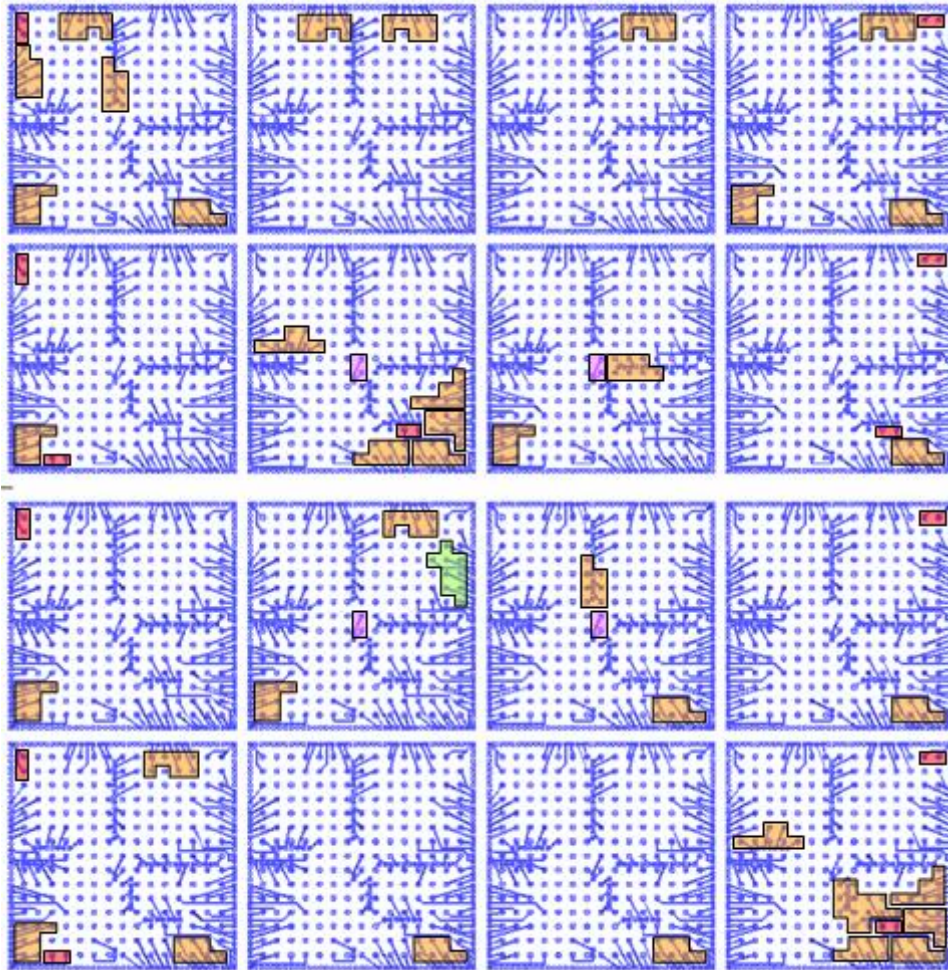
Figure 5.3 – Active Pads on the Packaged Test Chips

active pads on the packaged test chips including the rosette sites and solder bump locations that were interrogated after each packaging step. These sites were chosen so that measurements could be made at the die center and die corners, where several of the stress components typically have their maximum values. In addition, other sites were chosen to verify the symmetry of the observed stress distributions.

The integrity of the assembly processes were evaluated after each manufacturing step. Micro-focus x-ray inspection (see Figure 5.4) was utilized on each sample after solder joint reflow to identify any mis-alignment of the die to the ceramic substrate, as well as to locate poorly formed or missing solder joints. In addition, CSAM imaging (see Figure 5.5) was utilized after underfill dispense and cure to locate voids at the die to underfill interface. With the exception of a small number of missing solder balls on a few parts, the quality of the assemblies was quite high.

5.2   Socket Clamping Effects on Die Stresses

In a field application, a microprocessor package would be assembled to the next level of packaging by means of solder balls in a ball grid array (see Figure 5.6). For ease of measurement, the packages in this study were not soldered to a test board. Instead they were placed in a socket that allowed electrical connection to a PCB test board, representing the next packaging level in field applications. Connectors on the test board served as a means for the final connection of the assembly to a data acquisition system. All socket systems require some amount of mechanical force to achieve electrical connection to the PCB. In this study, several clamping options were applied to find the solution that induced the least amount of mechanical stress on the die. The options used
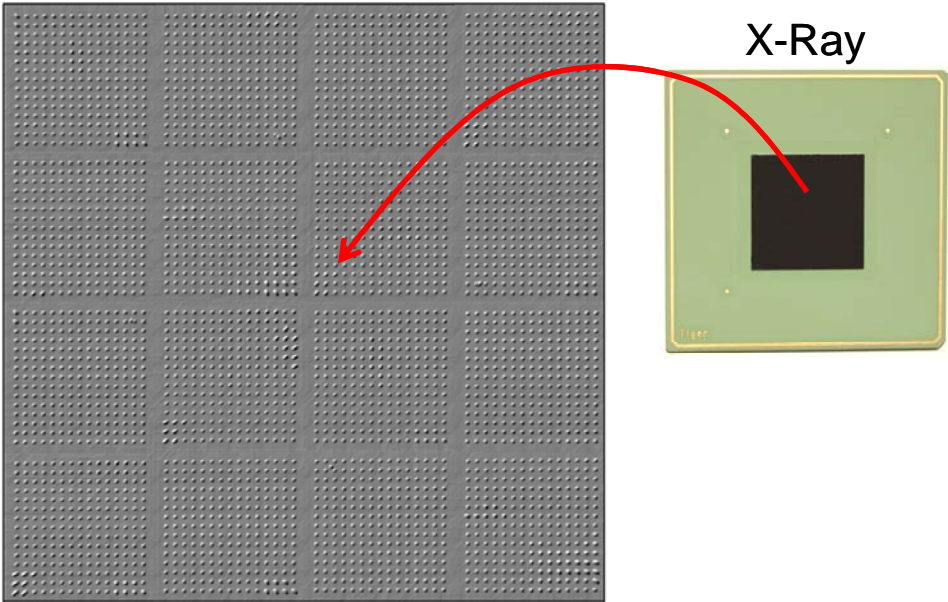
Figure 5.4 – X-Ray Verification of Solder Bumps
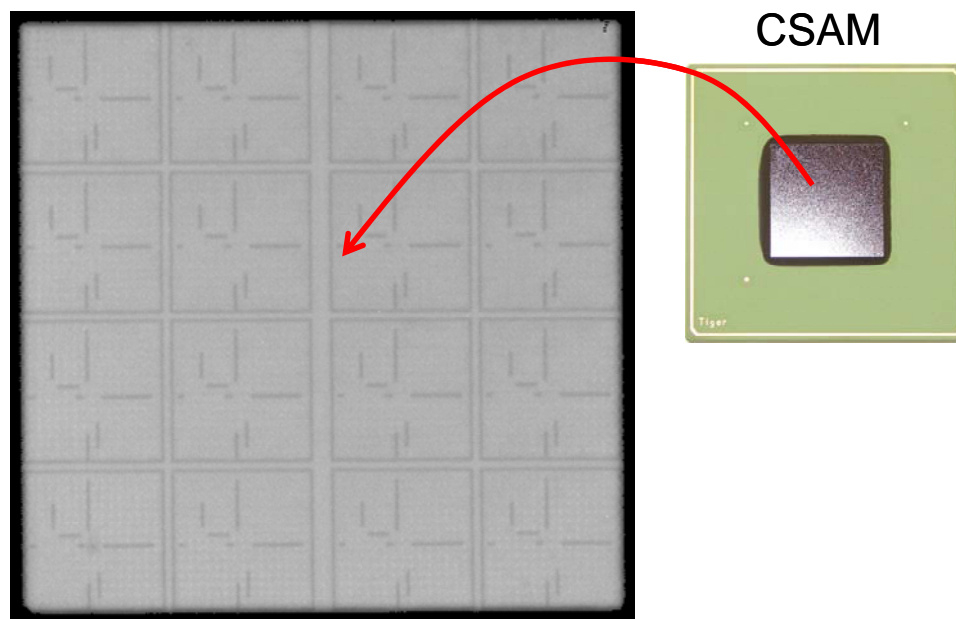
Figure 5.5 – CSAM Verification of Die-Underfill Interface
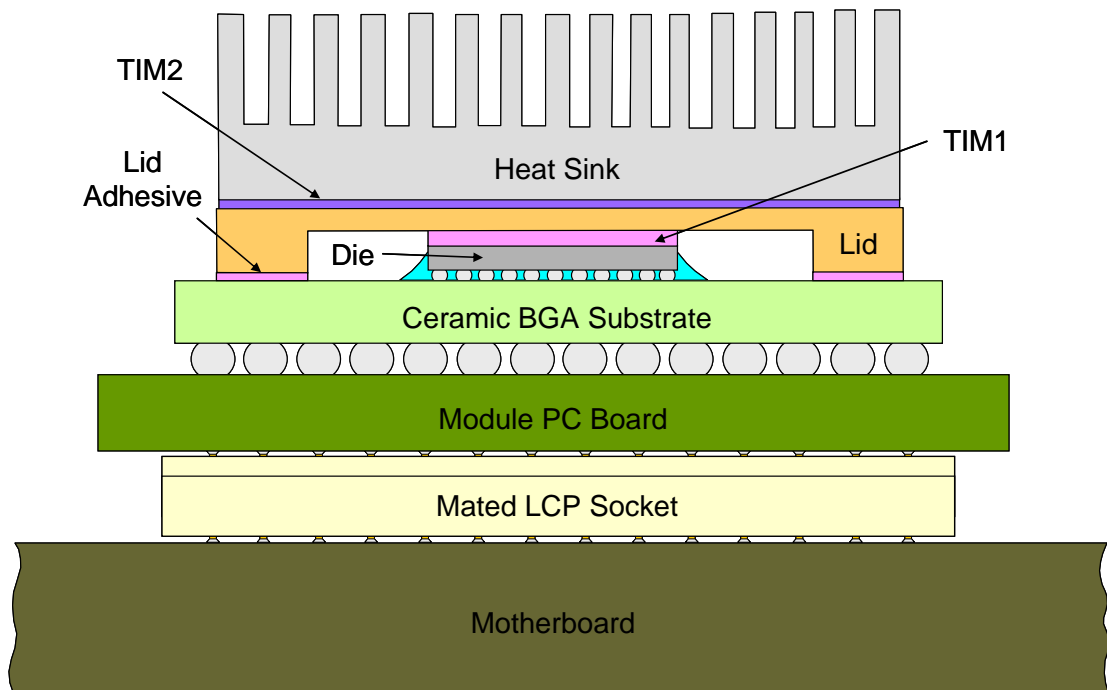
Figure 5.6 – Schematic of Real World Application

will be discussed in the order they were used, by assembly steps, as this was the natural progression of the study.

5.2.1   Clamping of Packages after Die Attachment

The first step of the packaging process was die attachment, and the packages consisted of the ceramic substrate with a central silicon chip (see Figures 5.1-5.2).   A mechanical clamp fitted specifically to the test PCB was first used to clamp these packages into the socket.   This clamping configuration is referred to as Clamp "A" (Figure 5.7).   Upon application of this clamp, warpage of the test PCB was observed.   A second observation on this method was that it directly applied force to the backside of the die (see Figure 5.8).   These two factors caused the disqualification of Clamp "A" as a suitable fixture for testing the packages.   To avoid inducing warpage to the test PCB, a localized clamping fixture was preferred.   Other clamp designs were tested that applied force on the substrate at a distance from the die, but were rejected due to asymmetry and warping issues along with lack of electrical connectivity.   To lessen these effects, a local clamp was designed that applied force to the full exposed surface of the ceramic BGA substrate with a 1 mm relief around the edge of the die.   This design is referred to as Clamp "B" and is shown in Figures 5.9–5.10.   The disassembled stack up of the package, clamp, and test board assembly is shown in Figure 5.11.

The application of force over the outside area of the ceramic substrate provided good electrical contact to the socket and test PCB, with the exception of the contacts at the center of the socket.   Upon examination of the clamped assembly, it was determined that the flexibility of the test socket, combined with the localized clamping scenario,

Figure 5.7 – Clamp Configuration A

Raised Section
Applies Direct
Mechanical Force
To the Die!

The Die Stresses
Change as the
Clamp is
Tightened!

Clamp Top

Die

Underfill

Socket

Ceramic Substrate

PCB

Clamp Base
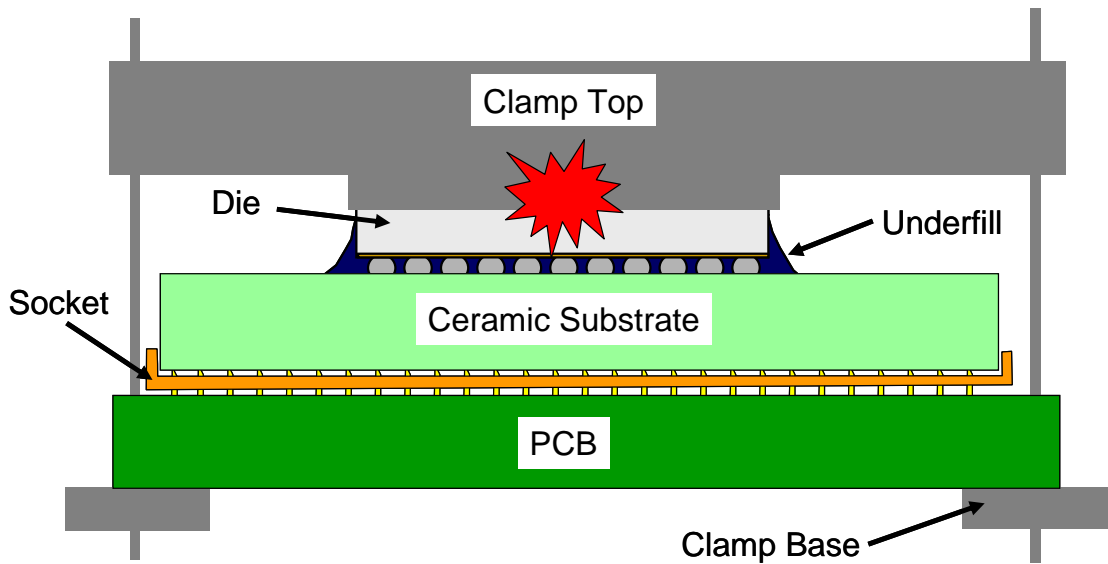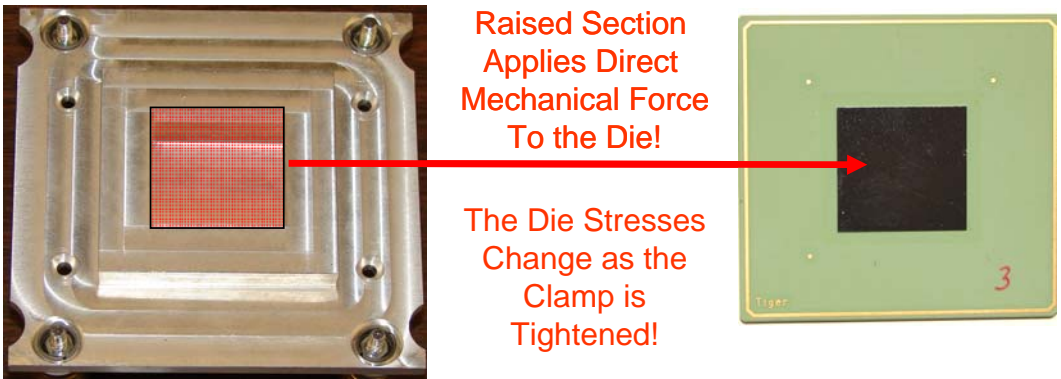
Figure 5.8 – Direct Application of Force to the Die Using Clamp Configuration A
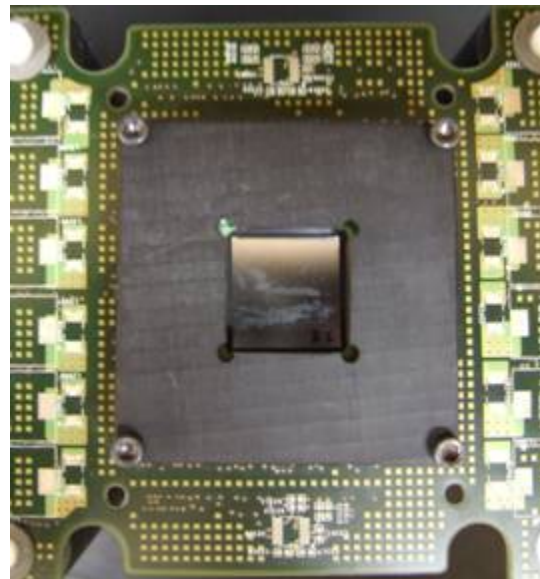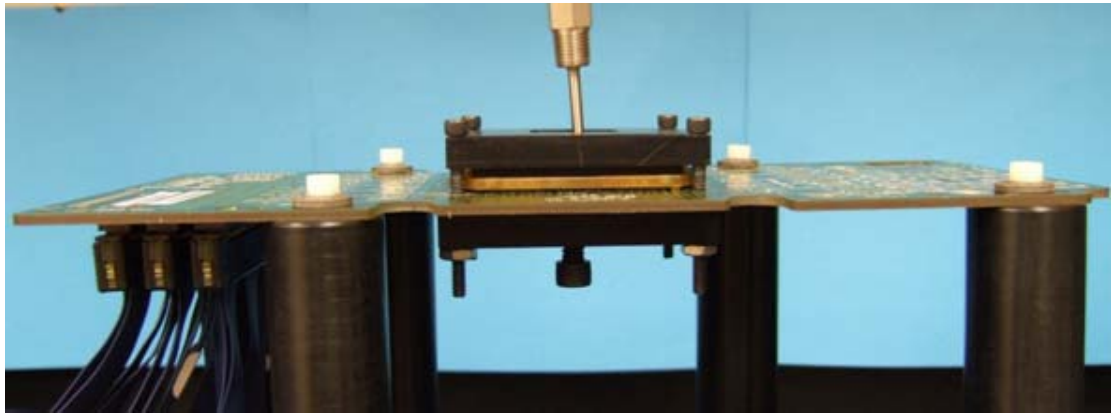
Figure 5.9 – Clamp Configuration B

Applies NO Direct
Mechanical Force
to the Die!

The Die Stresses
Do Not Change as
the Clamp is
Tightened!

Figure 5.10 – Contacting Piece in Clamp Configuration B
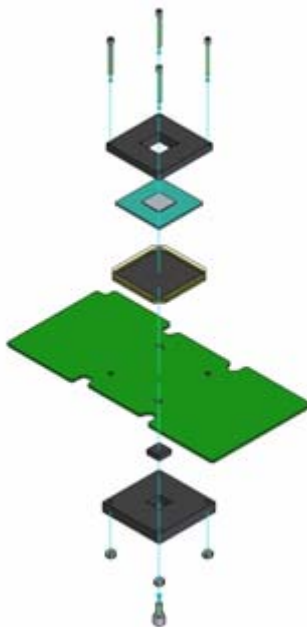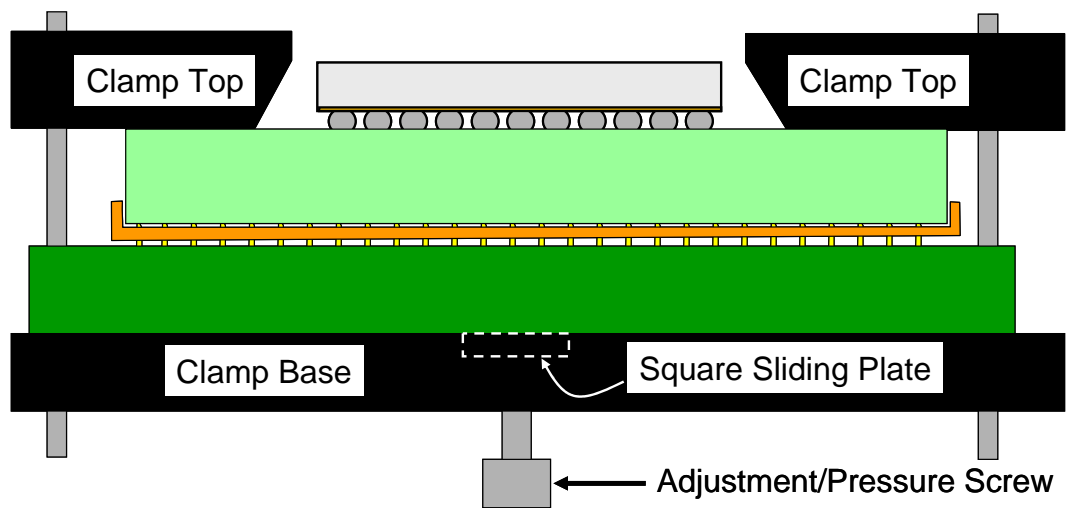
Figure 5.11 – Test Stack Up for Clamp Configuration B

contributed to a slight lifting effect on the socket. To compensate for this, a small cutout was made in the backing plate, and a sliding block adjusted by a screw was used to induce localized shifts in the test PCB in order to obtain full electrical contact throughout the assembly (see Figures 5.9 and 5.11). Readings taken with this clamping assembly were compared with measurements by hand probing the substrate, and the difference was found to be negligible. Thus, clamping configuration B was viewed as appropriate for measurement of the packages after die attachment.

5.2.2   Clamping of Underfilled Packages

In the second manufacturing step, underfill was applied and cured. The only physical and geometrical changes to the packages, once underfilled, was a small fillet at the perimeter of the die (see Figure 5.2). A slight change was necessary to the top piece in clamp design B to avoid any contact with the underfill fillet. After this change was made, it was found that the modified clamp B configuration had negligible influence on the die stress levels.

5.2.3   Clamping of Lidded Packages

As shown in Figures 5.1-5.2, a metallic lid was added to the packages at the third and final stage of assembly. An adhesive (TIM1) was applied to bond the lid to the ceramic substrate (Clamp A) and to the back of the die. Thus, the adhesive serves as a thermal interface material to conduct heat away from the die. The lidded packages were then clamped using clamping configuration B, and the resistances and temperatures of the sensors were measured. However, it was discovered that this configuration was

inappropriate, because it caused additional undesired loading of the lidded packages. Thus, it was disqualified for testing lidded packages. In initial attempts to find a solution, clamping configuration B was modified, as shown in Figure 5.12, to include a solid top piece, which provided a more even load distribution on the lid. The packages were measured again using this clamping scenario. The results showed an improvement, but were still unsatisfactory since they did not agree with those obtained by probing of the ceramic package. Similar results were obtained using clamp configuration A, so it was disqualified for lidded packages.

A third fixture referred to as clamping configuration C was then developed to apply force to the substrate only over the small region not covered by the lid. This approach is shown in Figure 5.13 and removed any force application to the lid, and therefore any possibility of force transmission through the lid attachment adhesive or TIM1 to the die. The lidded packages were measured using clamping configuration C, and stress values were extracted. Clamping configuration C showed statistically identical stress levels to manual probing of the lidded packages, and was thus concluded to be satisfactory.

5.2.4   Summary of Clamping Study

In this study, it has been shown that for a large area array microprocessor die on a high CTE ceramic substrate, that a localized clamp transmitting force through the substrate induced a negligible amount of stress on the die in reflowed condition. The same clamping scenario induced a negligible amount of stress on the die in an underfilled package. A combination of lid warpage and force transmission through the TIM1
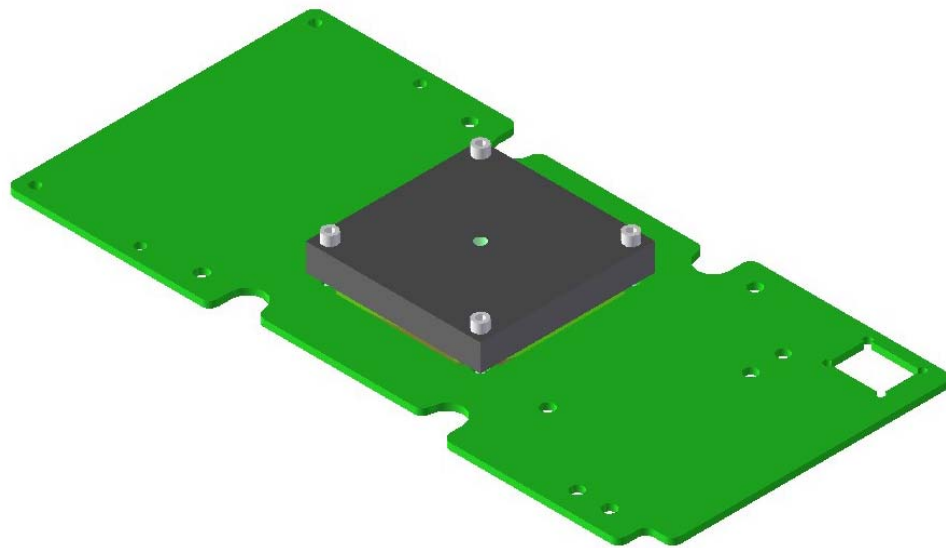
Figure 5.12 – Modified Clamp Configuration B
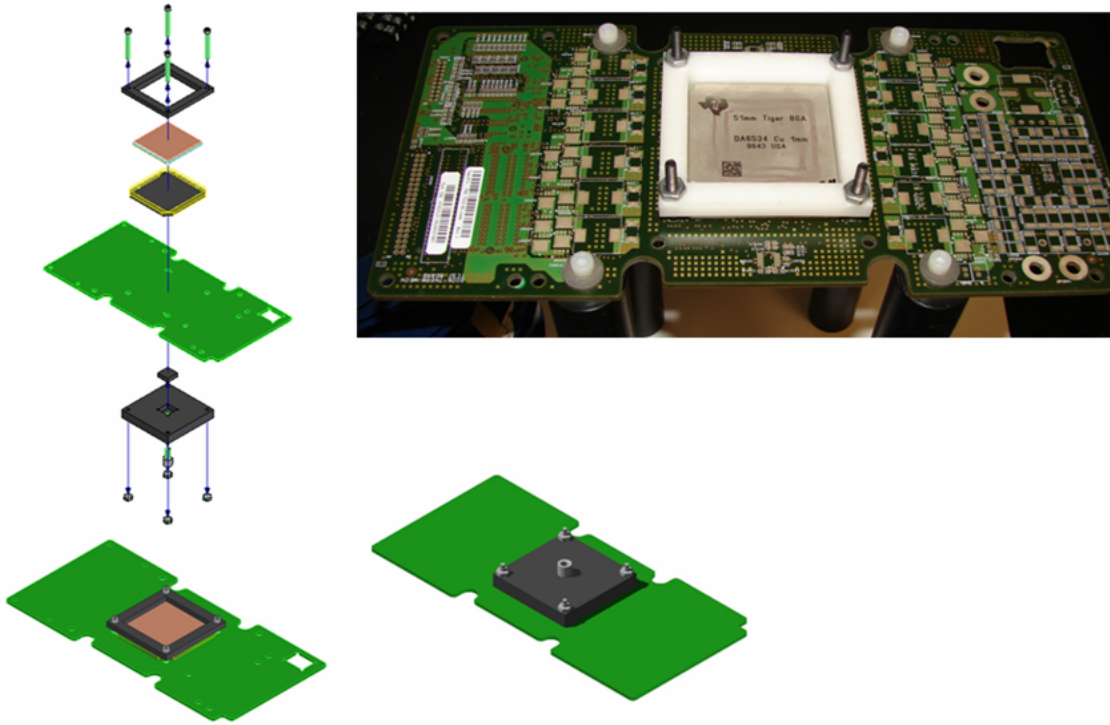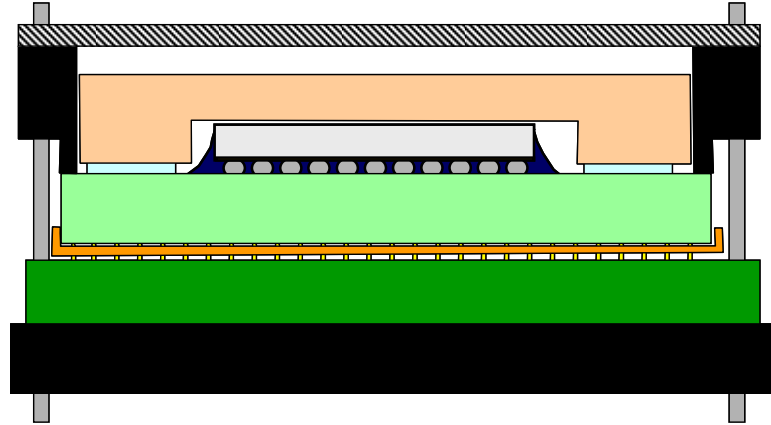
Figure 5.13 - Clamp Configuration C

material to the die resulted in large undesirable forces being transmitted to the die surface by the same clamp. This led to the design of a clamp transmitting force only on the periphery of the substrate, resulting in very low impact of the clamping on the die stress state. Example numerical results from the clamping study on the lidded packages are shown in Figure 5.14.

5.3   Experimental Stress Evaluation of Packaging Induced Stresses

The first step in measuring stress components in a piezoresistive stress sensor chip, once the chip has been calibrated, is to characterize the initial resistances of the individual sensors on the chip. This process was performed using a manual probe station as shown in Figure 5.15. In Equations 4.2, several terms appear as ΔR_i, i=1,2,…8. Here, ΔR is defined as the initial stress free resistance of the sensor subtracted from the current resistance of the sensor. Therefore, stress values can be extracted at any time if the initial and current resistances are known for each sensor as well as the temperature. In this study, the sensor resistances measured at the bare die stage were considered to be the initial stress free resistances. The sensor resistances measured after each stage of assembly are then considered to be the current resistances.

After the flip chip die were reflow soldered to the ceramic substrates, resistances of the sensors on the test die were measured again using the data acquisition system and test board fixture in Figure 5.9. A typical package at this stage is shown in figure 5.16. The results of the measurements agreed with historical data in several ways. First, the largest in-plane normal stresses (compressive) were observed at the center of the die. Correspondingly, the lowest values of in-plane normal stress were observed at the corners
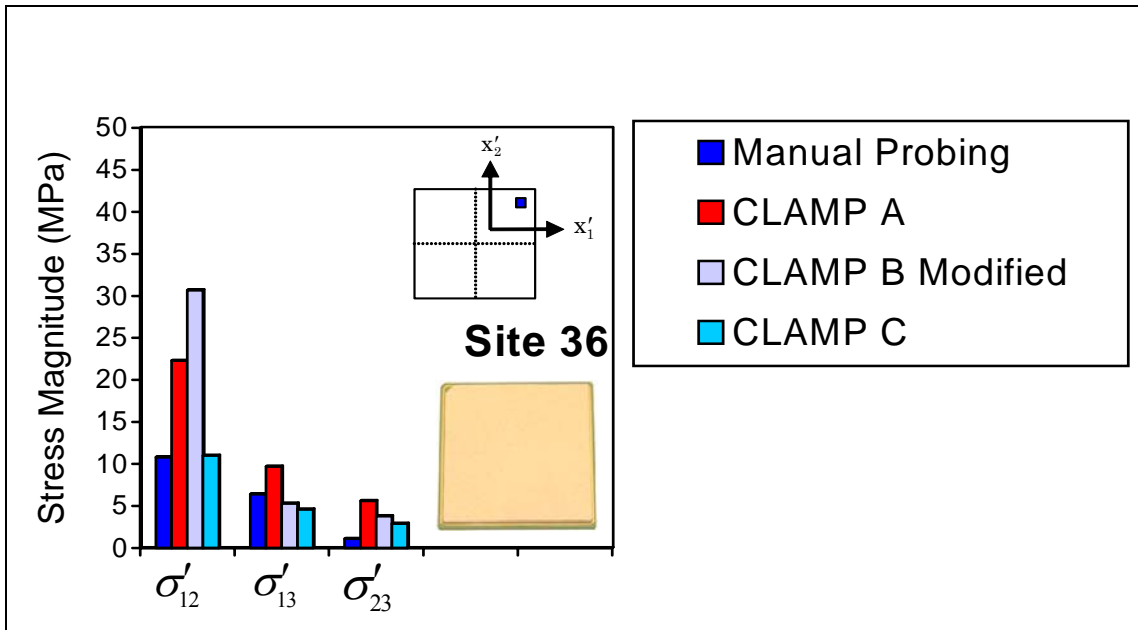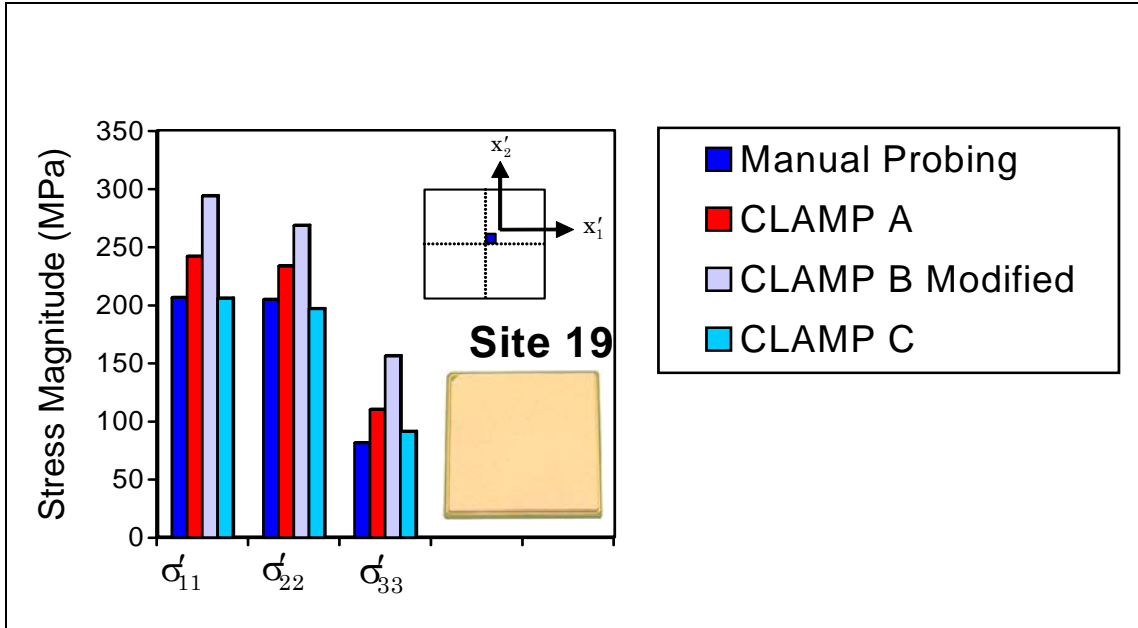
Figure 5.14 – Socket Clamping Study Summary
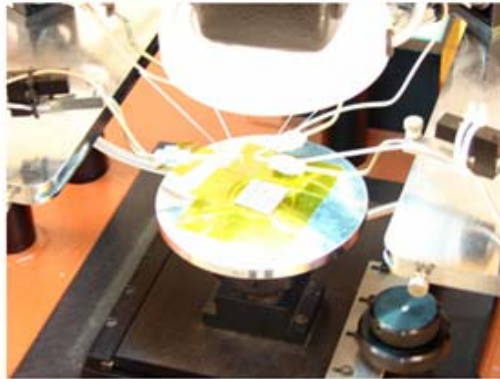
Figure 5.15 – Manual Probe Station
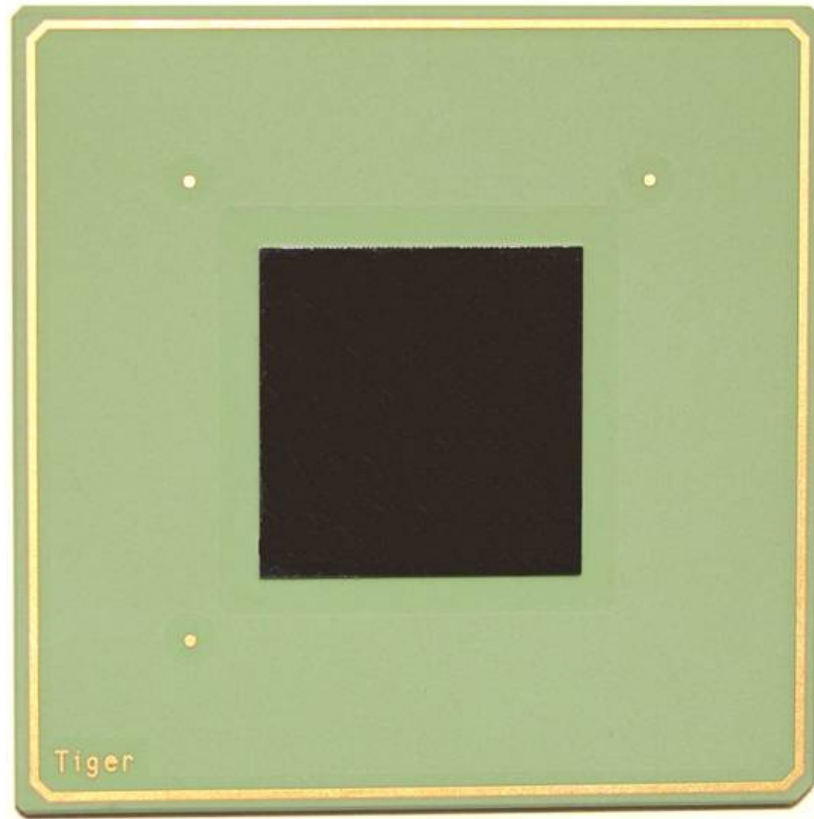
Figure 5.16 – Typical Package After Die Attachment

of the die. Also, the in-plane shear stress values were largest at the corners of the die. It is noted that the normal stress magnitudes were over 10X larger than the shear stress values, and were much larger than observed in previous flip chip studies [101, 116]. It is also noted that out-of-plane shear stress values were small as expected and in the range of 2-4 MPa. In comparison to previous studies, the value of the out-of-plane normal stress was found to be large. Numerical stress results at the die center and one corner are shown in Figure 5.17

The packages were then underfilled. A typical package at this point in the assembly process is shown in Figure 5.18. Stress values extracted from the resistance and temperature data showed that the underfilled packages held to the same trends noted for the die attached packages. However, the stress magnitudes all increased dramatically. The central normal stress magnitudes more than doubled, while the in-plane shear stress at the corners of the die increased by 25 percent. The normal stress difference at the center of the die was statistically unchanged, while it doubled at the corner of the die. The out-of-plane shear stress values remained very low with only very small changes. Numerical stress results for the underfilled packages are shown in Figure 5.19.

The third and last packaging step was lid attachment. A photograph of a typical sample and a schematic of a lidded assembly are shown in Figure 5.20. The attachment of the lid caused relatively small additional changes in the die stress levels. The in-plane normal stress magnitudes at the center of the die increased by an additional 10 percent, while the in-plane shear stresses at the die corners increased by almost 5 percent. The largest changes were observed in the normal stress difference values at both the center and corner of the die. The magnitude of the normal stress difference at the center

86

Site: R16_S15		
Stress Components	Values (MPa)	St. Dev
σ'_{11}	-54.3	9.7
σ'_{22}	-58.3	11.1
σ'_{33}	-24.0	3.9
σ'_{12}	-10.5	4.8
σ'_{13}	-4.3	1.8
σ'_{23}	2.6	2.5
$\sigma'_{11} - \sigma'_{22}$	4.0	1.4

Site: R7_S13		
Stress Components	Values (MPa)	St. Dev
σ'_{11}	-78.6	9.8
σ'_{22}	-73.5	11.3
σ'_{33}	-22.4	8.6
σ'_{12}	-7.4	3.1
σ'_{13}	-4.5	1.3
σ'_{23}	-2.8	2.1
$\sigma'_{11} - \sigma'_{22}$	-5.1	1.6
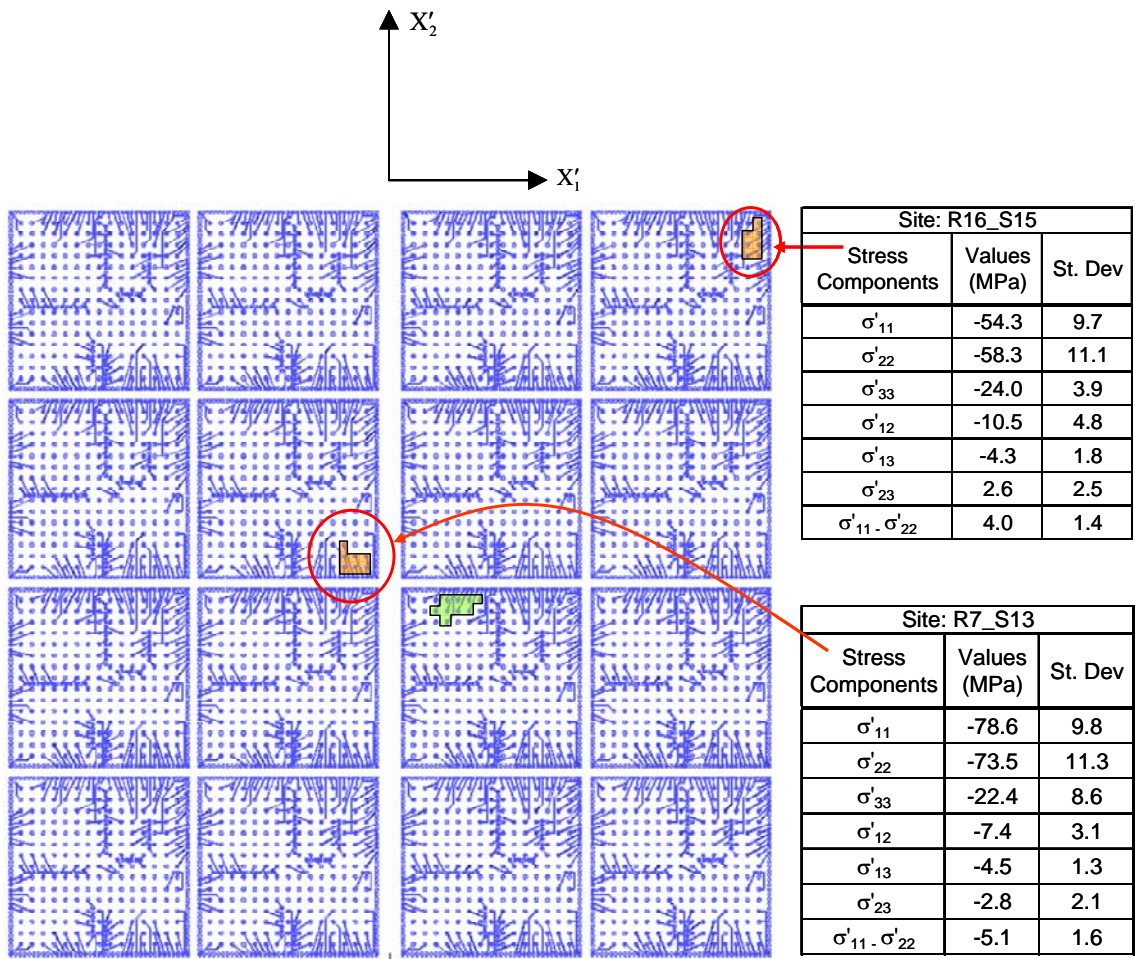
Figure 5.17 - Stress Results After Die Attachment
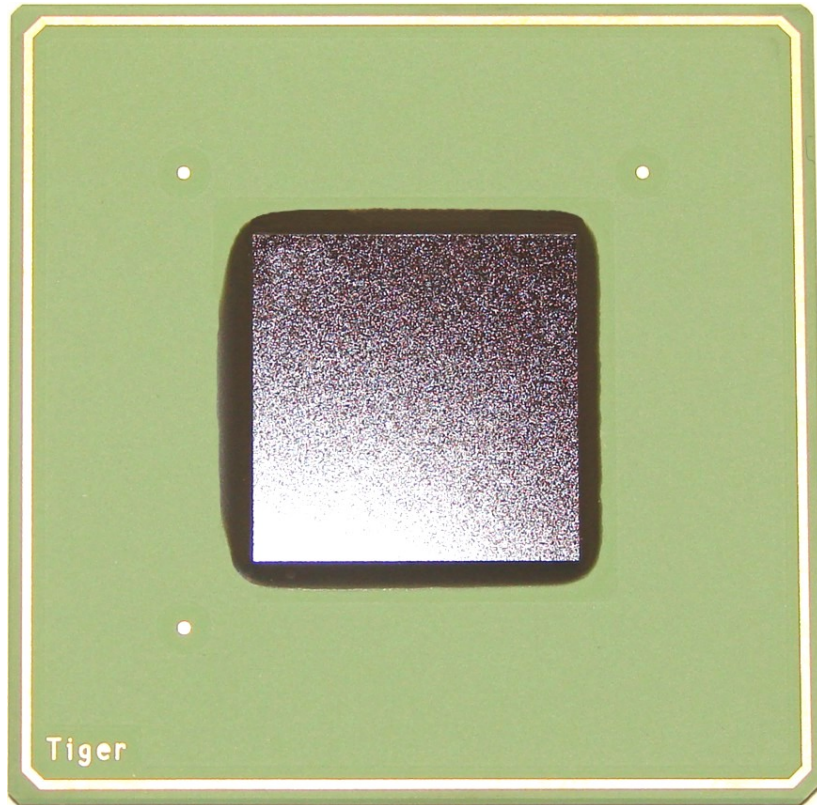
Figure 5.18 – Typical Underfilled Package
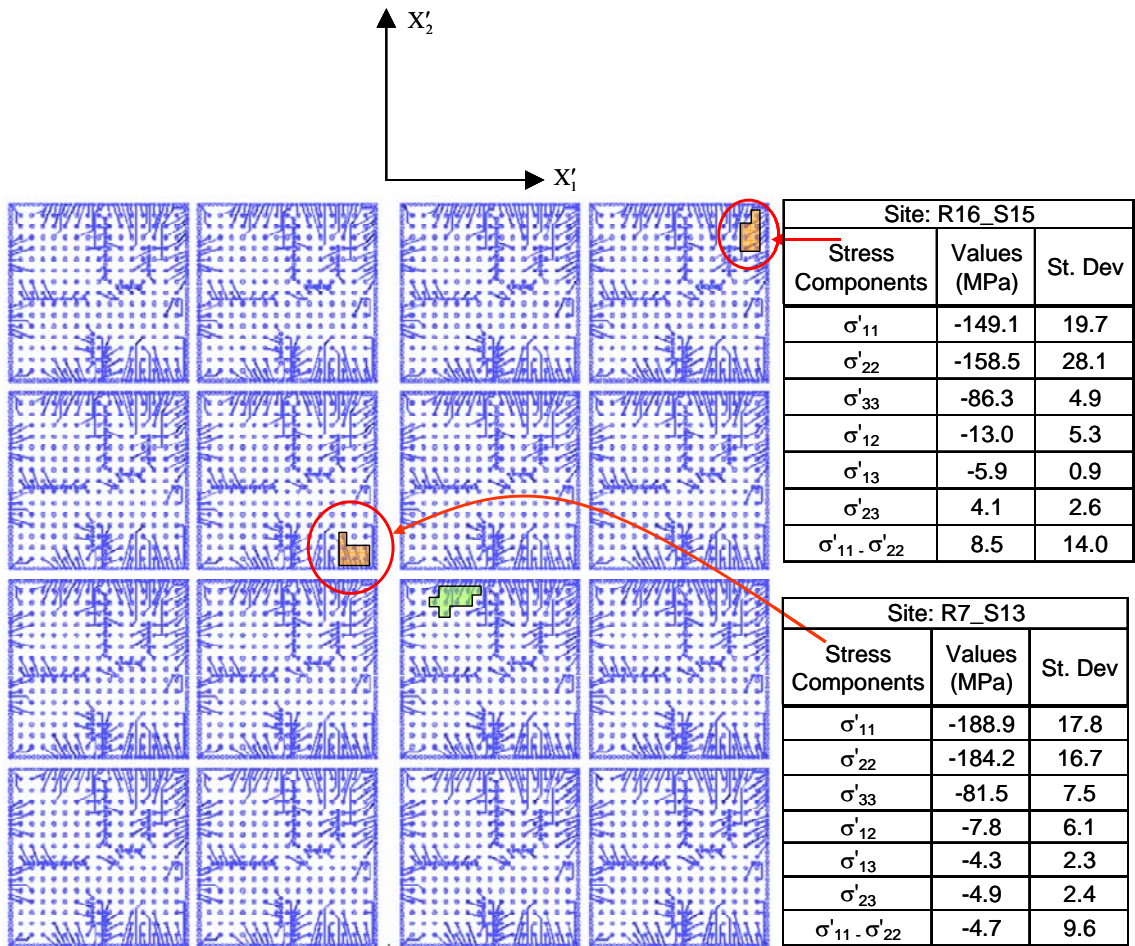
Figure 5.19 - Stress Results After Underfill Application

Site: R16_S15		
Stress Components	Values (MPa)	St. Dev
σ'_{11}	-149.1	19.7
σ'_{22}	-158.5	28.1
σ'_{33}	-86.3	4.9
σ'_{12}	-13.0	5.3
σ'_{13}	-5.9	0.9
σ'_{23}	4.1	2.6
$\sigma'_{11} - \sigma'_{22}$	8.5	14.0

Site: R7_S13		
Stress Components	Values (MPa)	St. Dev
σ'_{11}	-188.9	17.8
σ'_{22}	-184.2	16.7
σ'_{33}	-81.5	7.5
σ'_{12}	-7.8	6.1
σ'_{13}	-4.3	2.3
σ'_{23}	-4.9	2.4
$\sigma'_{11} - \sigma'_{22}$	-4.7	9.6
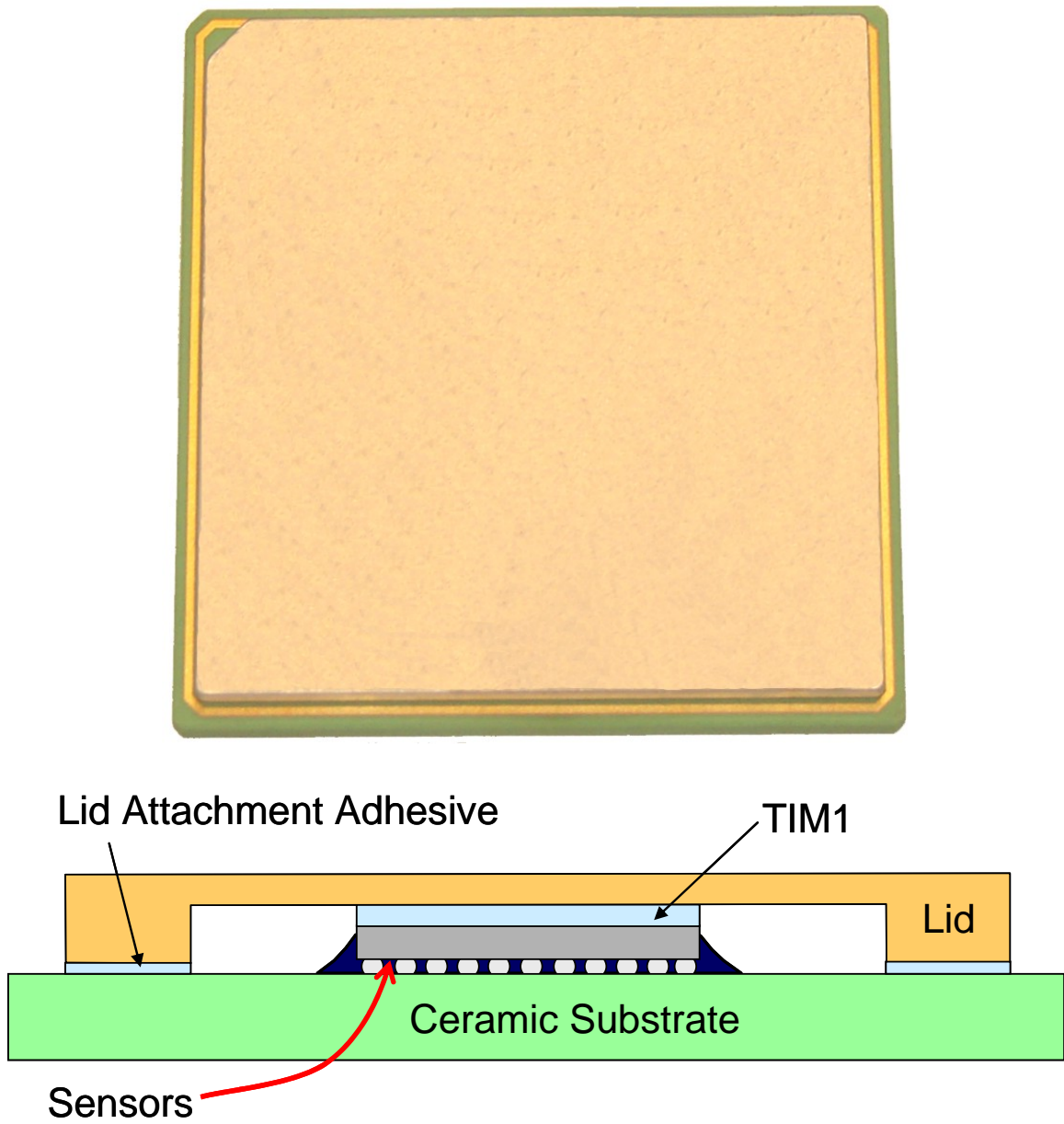
Figure 5.20 – Typical Lidded Packages

decreased by approximately 25 percent, and the value at the corner almost doubled. Numerical stress results for the lidded packages are shown in Figure 5.21. Figures 5.22-5.24 graphically illustrate the evolution of the die stresses during the manufacturing process.

Site: R16_S15		
Stress Components	Values (MPa)	St. Dev
σ'_{11}	-153.1	13.6
σ'_{22}	-169.0	19.5
σ'_{33}	-96.2	10.8
σ'_{12}	-13.5	2.2
σ'_{13}	-6.5	0.2
σ'_{23}	5.5	2.2
$\sigma'_{11} - \sigma'_{22}$	15.9	6.2

Site: R7_S13		
Stress Components	Values (MPa)	St. Dev
σ'_{11}	-210.3	17.0
σ'_{22}	-206.7	15.4
σ'_{33}	-89.4	13.2
σ'_{12}	-7.9	5.1
σ'_{13}	-4.2	2.1
σ'_{23}	-4.4	2.6
$\sigma'_{11} - \sigma'_{22}$	-3.6	10.1
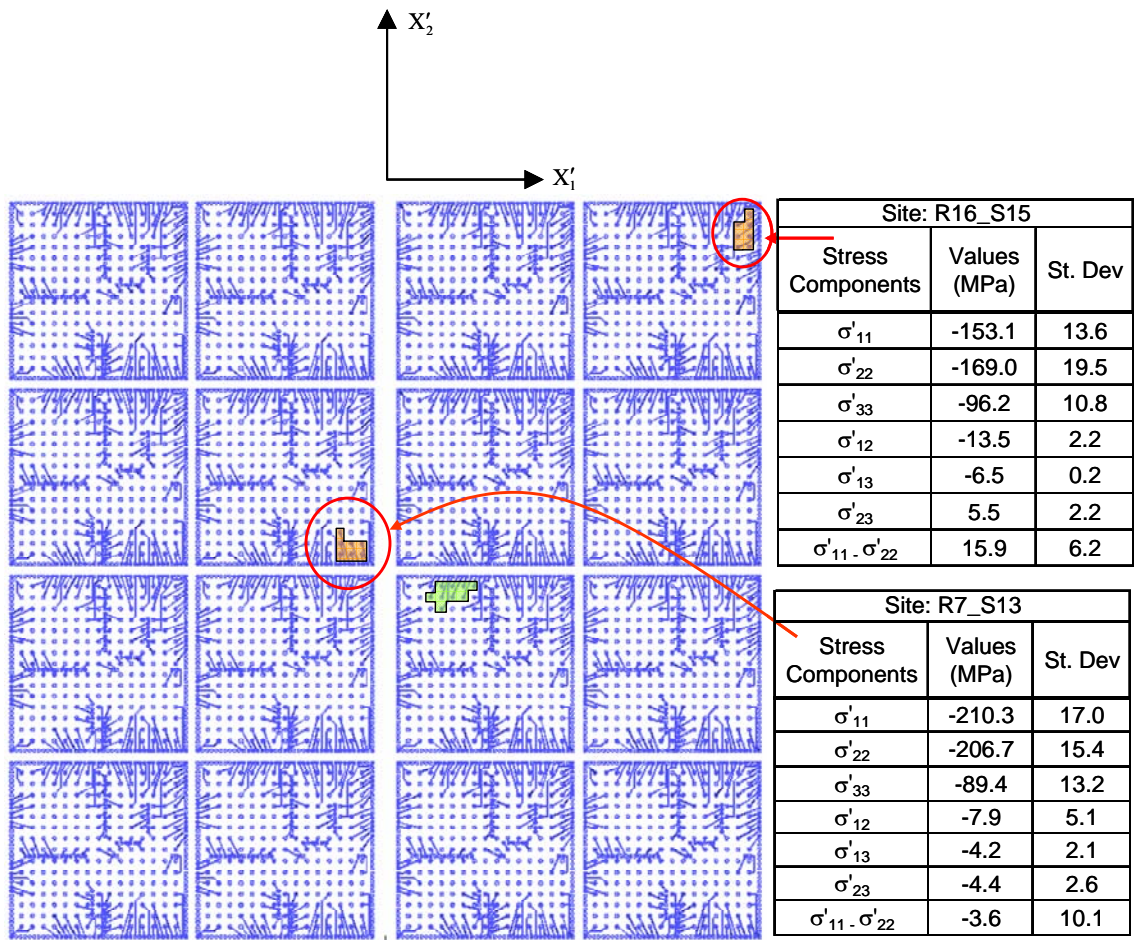
Figure 5.21 – Stress Results after Lid Attachment
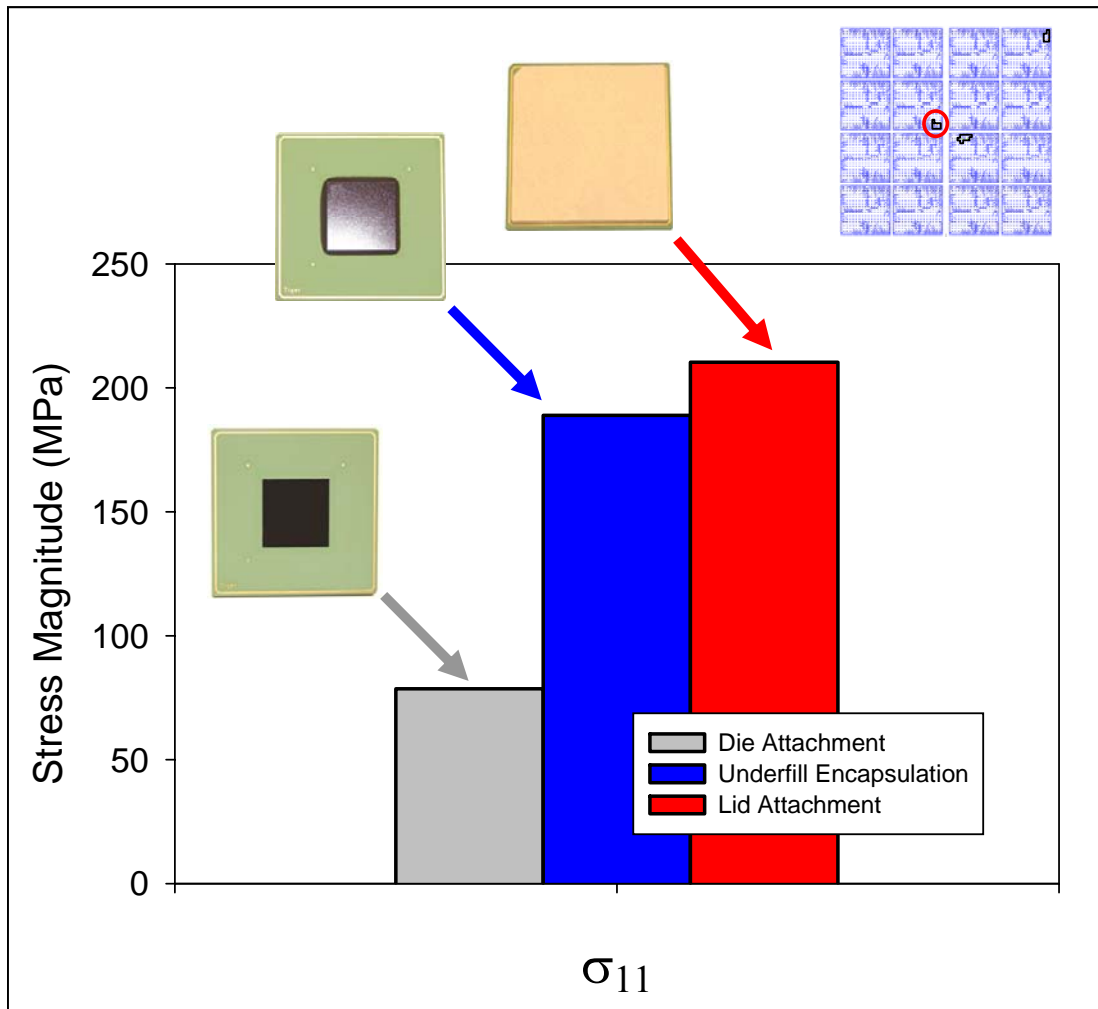
Figure 5.22 - Evolution of In-Plane Normal Stress at the Center of the Die
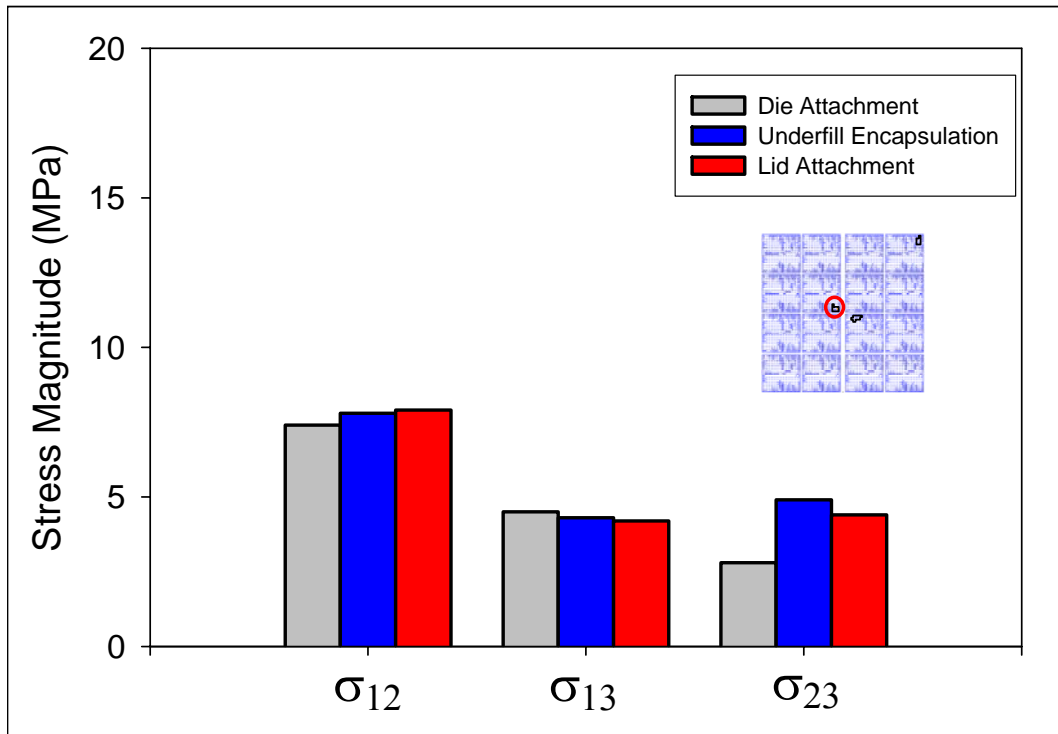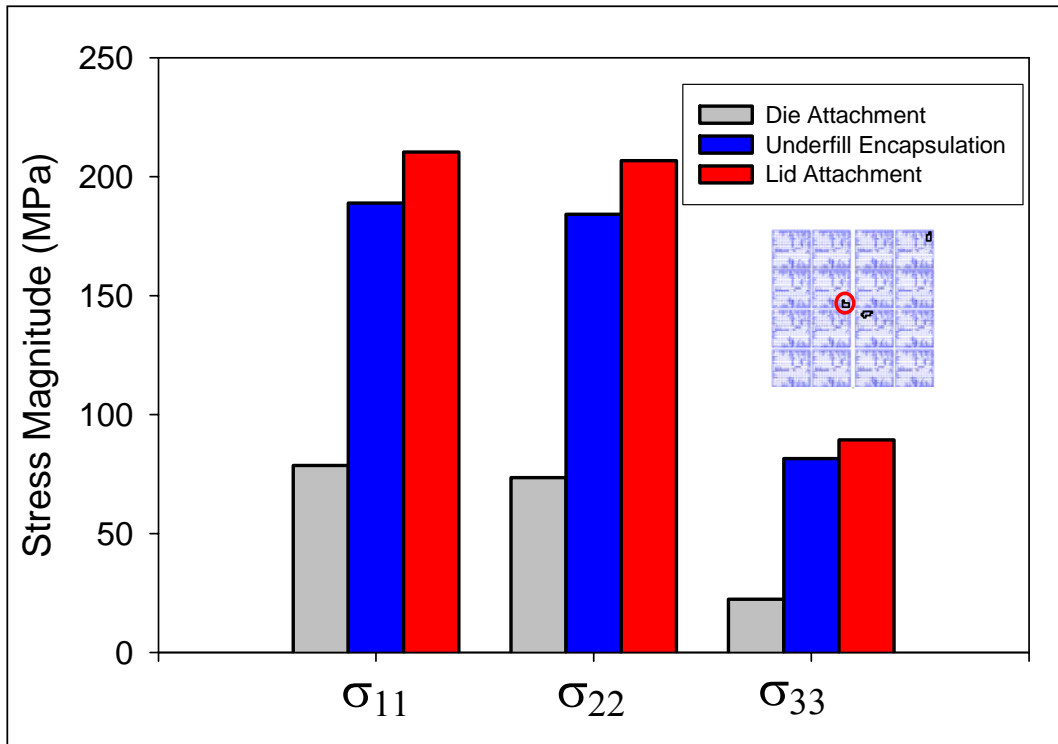
Figure 5.23 - Evolution of the Six Die Stress Components at the Center of the Chip
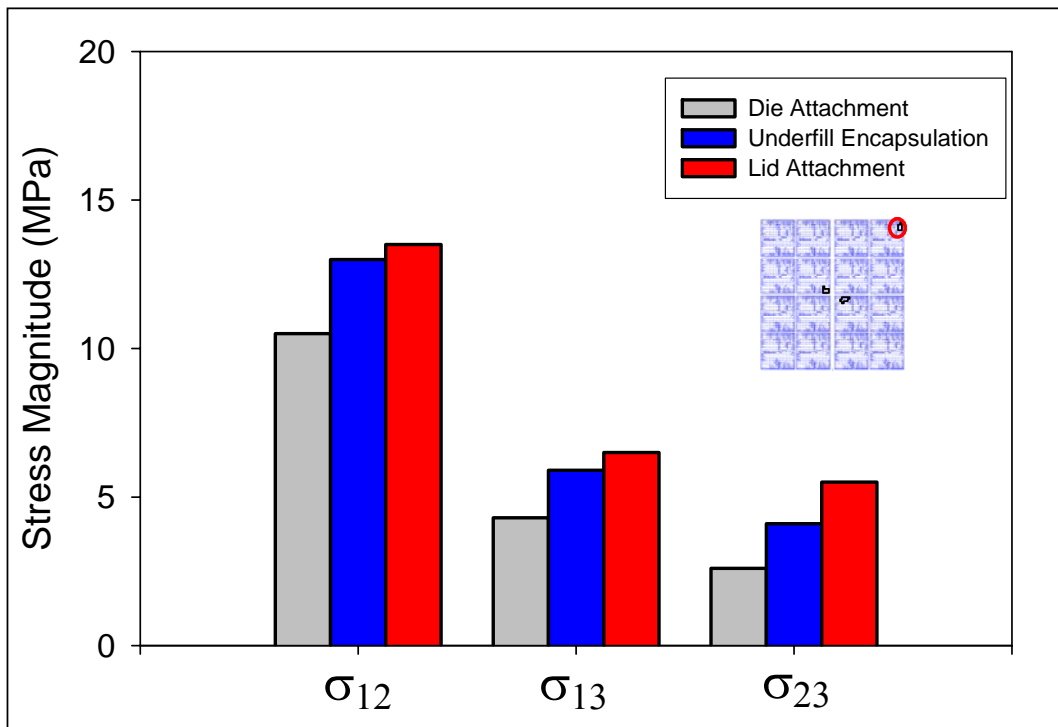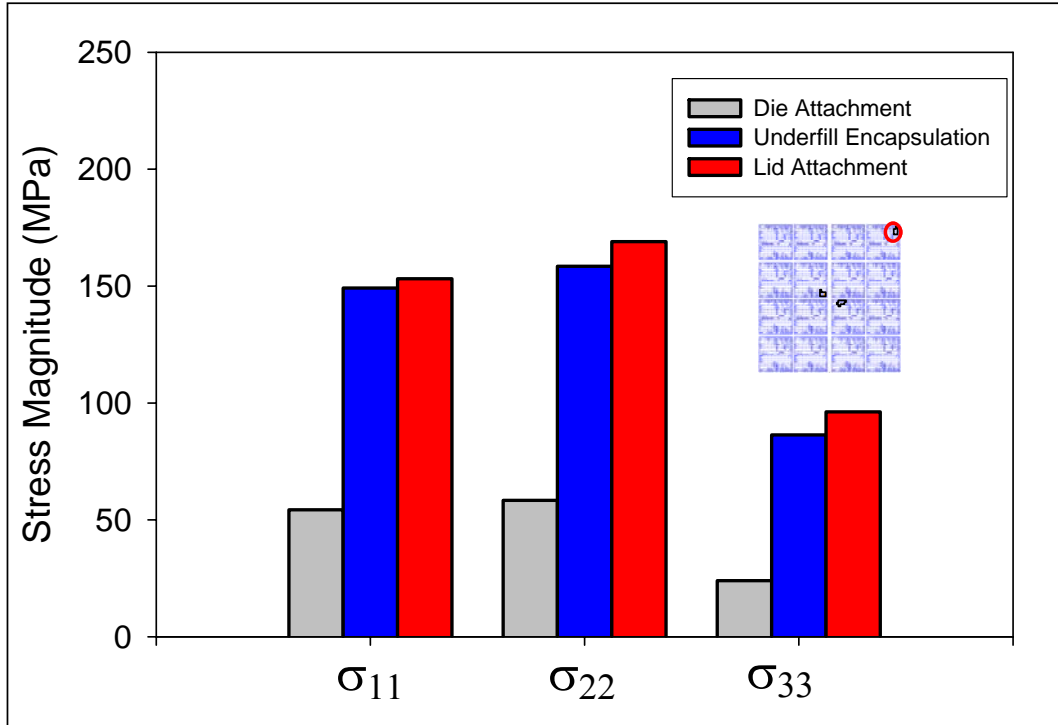
Figure 5.24 - Evolution of the Six Die Stress Components at the Corner of the Chip

CHAPTER 6

DIE STRESS VARIATION WITH TEMPERATURE

6.1   Die Stress Variation with Temperature

Electronics packages rarely if ever operate at room temperature.   All stress

measurements in this study up to this point have been made at room temperature. A basic

understanding of the effects of temperature on die stress levels in the CBGA test package

is needed.   After the complications with clamping of the test packages onto the test

boards (see Chapter 5), the necessity of eliminating a clamp as a source of induced die

stress was apparent. While the clamp used to characterize the lidded packages was found

to induce little to no stress on the die surface at room temperature, the assumption could

not be made that the same clamp would continue to have no effect as the temperature

changes. In this chapter, an initial attempt was made to make temperature dependent die

stress measurements. An interconnection system was developed that avoided using the

previously discussed test board and clamping fixtures.

The test package carrier shown in Figure 6.1 was developed for temperature

dependent measurements. The carrier allowed the package to "float" without restriction

of deformations, while also providing electrical routing to the data acquisition system.

Specific pads on the bottom of the CBGA ceramic substrate necessary to access the

central and corner sensor rosettes were identified. Small strips of a PCB designed for
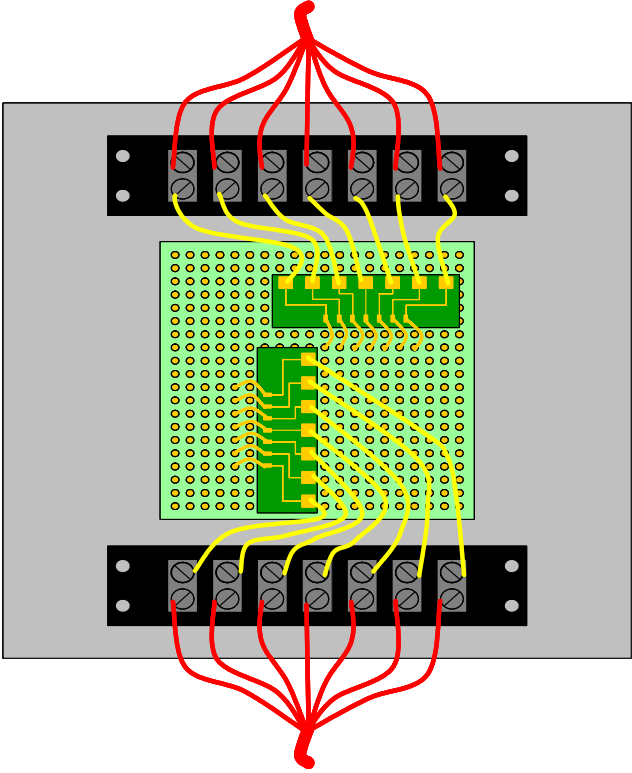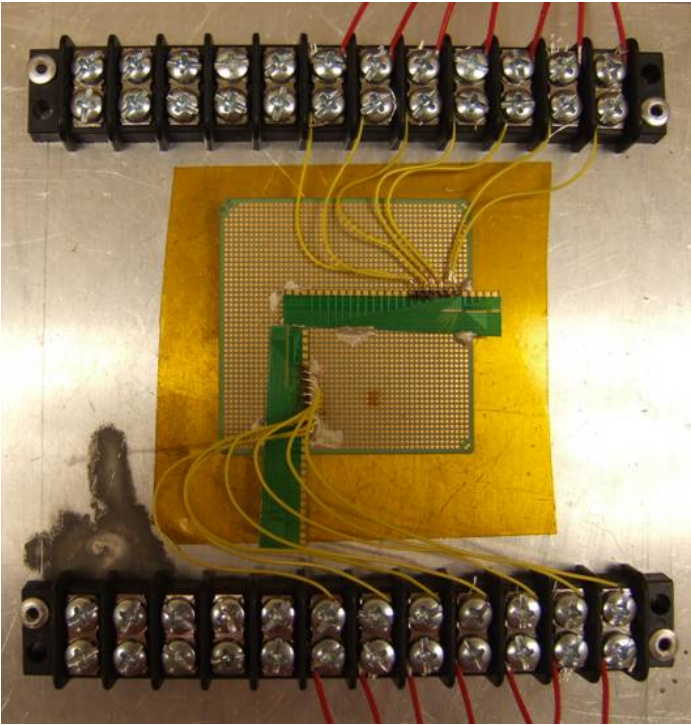
Figure 6.1 – Test Package Carrier

wirebonding were mounted to the back of the package using a non-conductive adhesive. The strips fanned out from the wirebond pads to larger pads that were big enough to accept soldered wires. Wirebonds were made from the pads on the ceramic package to the wirebond pads of the PCBs. Small, 36 AWG wires were then soldered to the larger pads on the PCB and connected to screw terminal blocks on the carrier base. Connections were made to the data acquisition system from the terminal blocks.

The package and carrier assembly were then placed into the test oven and connected to the data acquisition system shown in Figure 6.2. Software was used to control the oven temperature and also make sensor resistance measurements. The package was subjected to temperatures from 10 ˚C (slightly below room temperature) to 105 ˚C. This temperature range was chosen based on the temperatures a microprocessor package might see in field use. The temperature of the oven was varied in 5 ˚C degree increments, and the package was allowed to reach steady state before sensor measurements were taken. The temperature versus time profile is shown in Figure 6.3, and the corresponding in-plane normal stress results at the die center are shown in Figure 6.4. As expected, the stress level decreased with increased temperature. It is noted that the normal stress at 100 ˚C is not close to zero. Stress levels in IC packages typically relax as they get closer to their assembly temperature and the glass transition temperatures of the assembly materials. As discussed in the next chapter, the glass transition temperature of the underfill used in the CBGA packages was 80 ˚C. The stress magnitude tended towards zero up to 100 ˚C, but was still relatively high. Solder is a relatively stiff material when compared to underfill. The SAC387 solder used in the CBGA test packages has a reflow temperature of approximately 220 ˚C, and retains 75%

Figure 6.2 - Data Acquisition and Oven
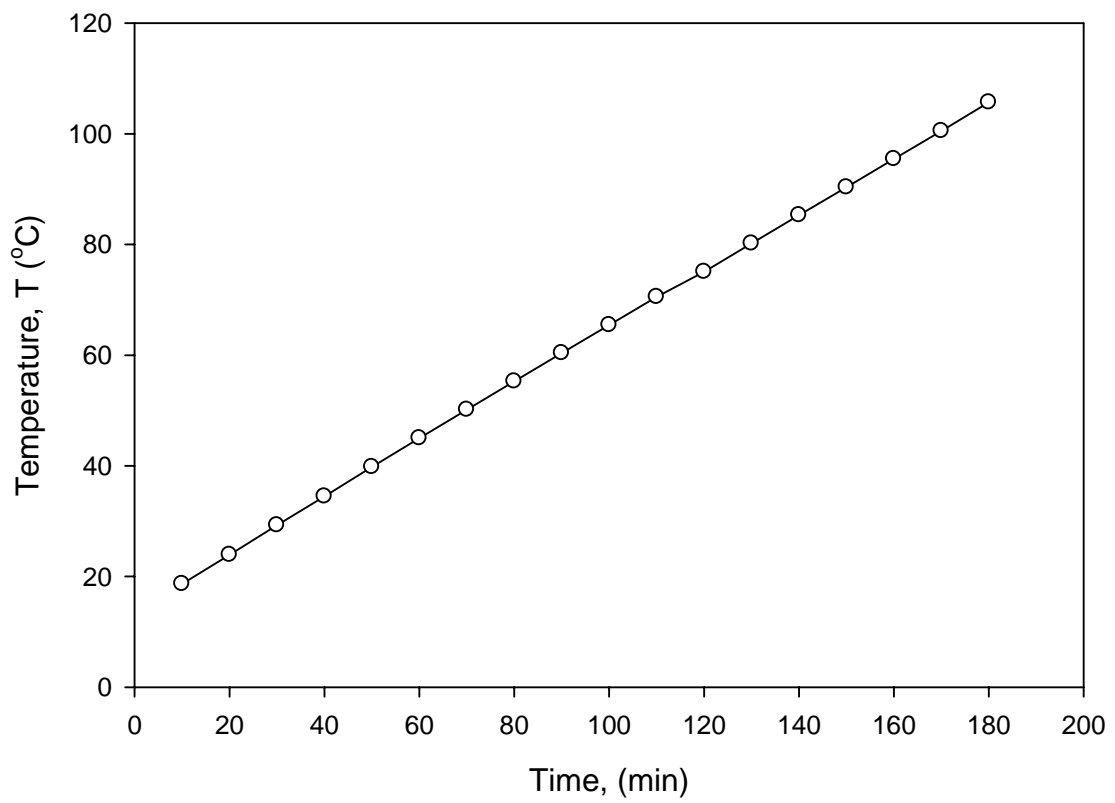
Figure 6.3 - Temperature Profile
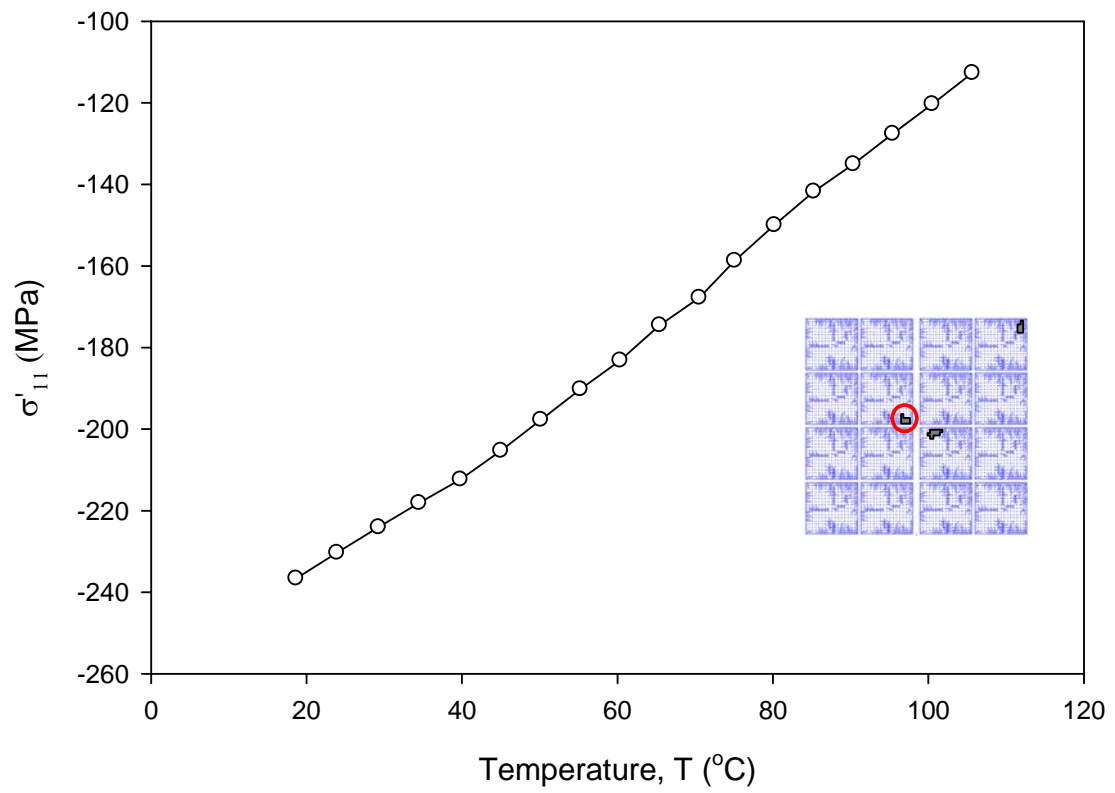
Figure 6.4 - Normal Stress vs. Temperature

101

of its stiffness and strength at 100 °C [117]. Since the test chips are large area array die with relatively stiff solder bumps, it is very reasonable to expect non-zero stress levels at 100 °C even though the underfill has negligible stiffness at that temperature.

6.2   Summary and Conclusions

A preliminary study on the effects of temperature on the die surface stresses has been completed for the CBGA test packages. A fixture was designed to eliminate sources of clamping stress. Test packages were subjected to temperatures from 10 °C to 105 °C. The die central normal stress magnitude was observed to decrease with increased temperature. It was noted that stress levels were not at zero near the high end temperature of 105 °C. This has been attributed to the fact that the flip chip solder bumps were made from relatively stiff lead free solder. At 105 °C, the solder is still partially contracted compared to its state at its reflow temperature, and it still has high stiffness to pull the die toward its neutral axes.

CHAPTER 7

CHARACTERIZATION OF UNDERFILLS

FOR MICROPROCESSOR PACKAGING

7.1   Characterization of Underfills

7.1.1   Introduction

Underfills have become an extremely important element of modern microprocessor packages. In the context of this study, it has been shown that underfill can have an extreme effect on die surface stress levels. It has been deemed necessary to further study the underfill used in the CBGA microprocessor packages in order to further understand experimental results and to facilitate future finite element verification of the experimental results.

To fully characterize an underfill for application in experimental and finite analysis, several quantities must be known. First, tensile properties must be known over a temperature range that exceeds what the package would see in a working environment, and above the range of any foreseen environmental testing on the package. A full set of temperature dependant stress-strain curves will result from this testing. Elastic modulus, ultimate tensile strength, and failure strain should be known as a function of temperature. Creep tests should also be performed over a range of strain rates and as a function of different stress levels. Finally, coefficient of thermal expansion and glass transition

different stress levels. Finally, coefficient of thermal expansion and glass transition temperature, T_g, must also be determined experimentally.

7.1.2   Specimen Preparation

For tensile and creep tests, a standard specimen was used. The specimens are 90 mm in length, 3 mm in width, and 0.125 mm thick. They are prepared by using the Teflon coated plates in Figure 7.1. The plates are separated with shims by 0.125 mm. The plates are then placed in a CAM/ALOT 3700 underfill dispense machine, shown in Figure 7.2. A needle dispenses the underfill along the crossbars of the top plate. The underfill moves under the crossbars by capillary action, and forms a specimen the size and shape of the crossbars. The underfill is then cured in an oven according to the manufacturer's specifications, shown in Table 7.1.

To obtain coefficient of thermal expansion (CTE) data and T_g for the underfill, a different sample size and dimension was needed. A small square of cured underfill was called for in this phase of testing. The square was limited to 5 mm on a side and a minimum thickness of 1.5 mm was required. For these specimens, two of the solid Teflon coated plates were shimmed to the appropriate thickness, and underfill was applied by hand using a syringe. The samples were then cured in an oven according to the manufacturer's specifications. A large sheet of cured underfill was produced by this method. The sheet was then dry sawn into the desired squares by a Buehler Isomet 1000 High Precision Saw, shown in Figure 7.3.

Out of Cold Storage Time	1 hr
Substrate Temperature	70-80 °C
Cure Temperature	150 °C
Cure Time	60 min

Table 7.1 - Cure Conditions of Underfill
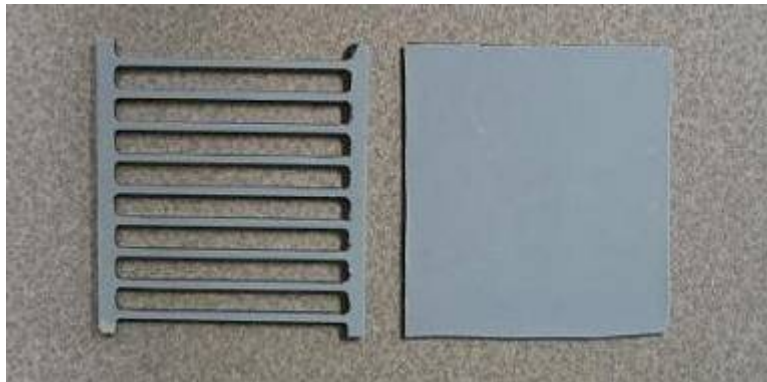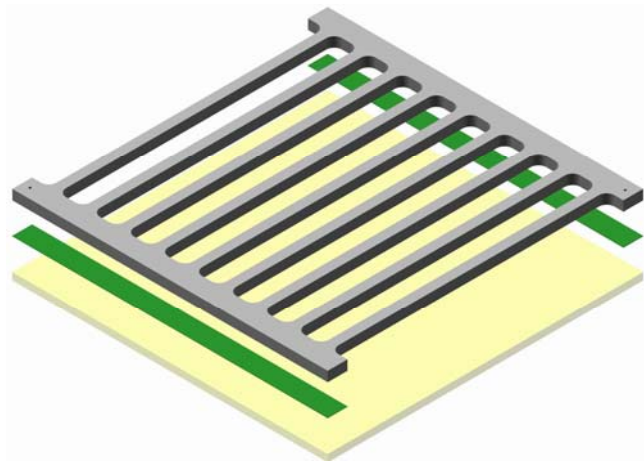
Figure 7.1 - Teflon Coated Plates Used in Underfill Specimen Preparation

Figure 7.2 - CAM/ALOT 3700 Underfill Dispense Machine

Figure 7.3 - Buehler High Precision Saw

7.1.3   Testing Methods

To obtain stress-strain curves for the underfill studied here, a precision tensile tester, or micro-tester is employed (Figure 7.4).   The micro-tester is fitted with a precision stepper motor and load cell. With attachments, also shown in Figure 7.4, the micro-tester is capable of testing materials from -185 to +300 ˚C.   Variables in the controller software include strain rate, constant load, force-displacement, and stress strain, making it capable of performing both stress-strain tests and creep tests. To obtain CTE and T_g values for the underfill, a DuPont Instruments Thermomechanical Analyzer (TMA) was used in conjunction with an Omnitherm controller and Instrument Specialists software, and is shown in Figure 7.5. A schematic of the TMA is shown in Figure 7.6.

7.2   Properties of Underfills

7.2.1   Stress-Strain Curves

A typical stress-strain curve with visual explanation of physical properties is shown in Figure 7.7. Samples are fixed to the grips of the micro-tester and pulled at a constant rate until failure. The data is recorded by the software real time. To accommodate for any variance in samples, 10 different tests were performed at each temperature. After the specimen yields it is still subject to plastic deformation. The response of an underfill after it yields can be noisy especially at elevated temperatures. The data for each specimen tested between 50˚C and 90˚C were smoothed by fitting a line through only the data past the yield point. The data for each temperature are then fitted with a model that averages the results from the data of the ten tests. An example of this fitting is shown in Figure 7.8. The fits to the data sets at various temperatures
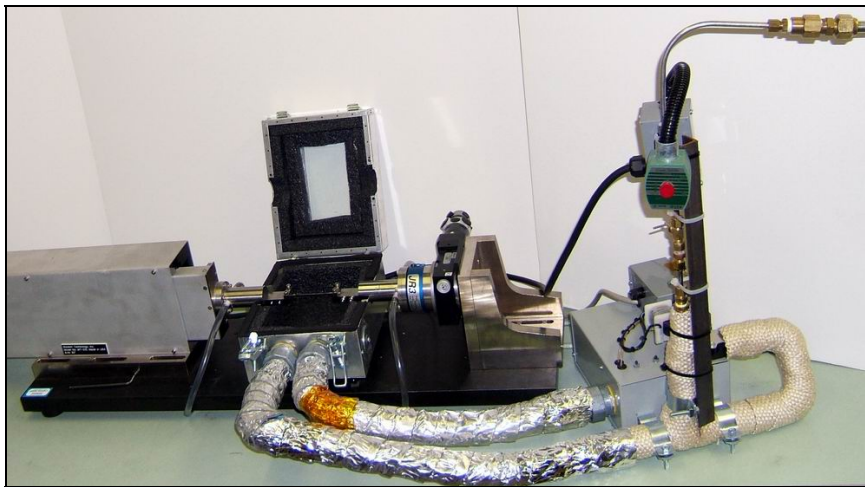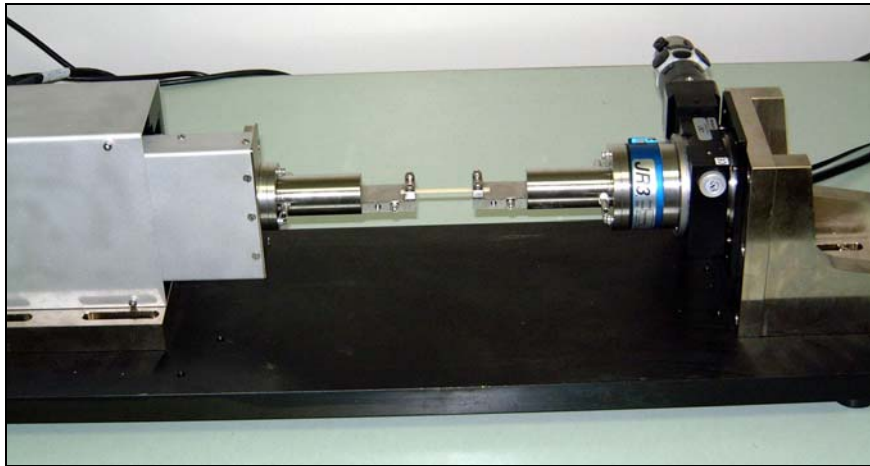
Figure 7.4 - Micro-Tester (top), Cooling Attachment (middle),
Heating Attachment (bottom)

Figure 7.5 – DuPont Instruments 942 Thermomechanical Analyzer
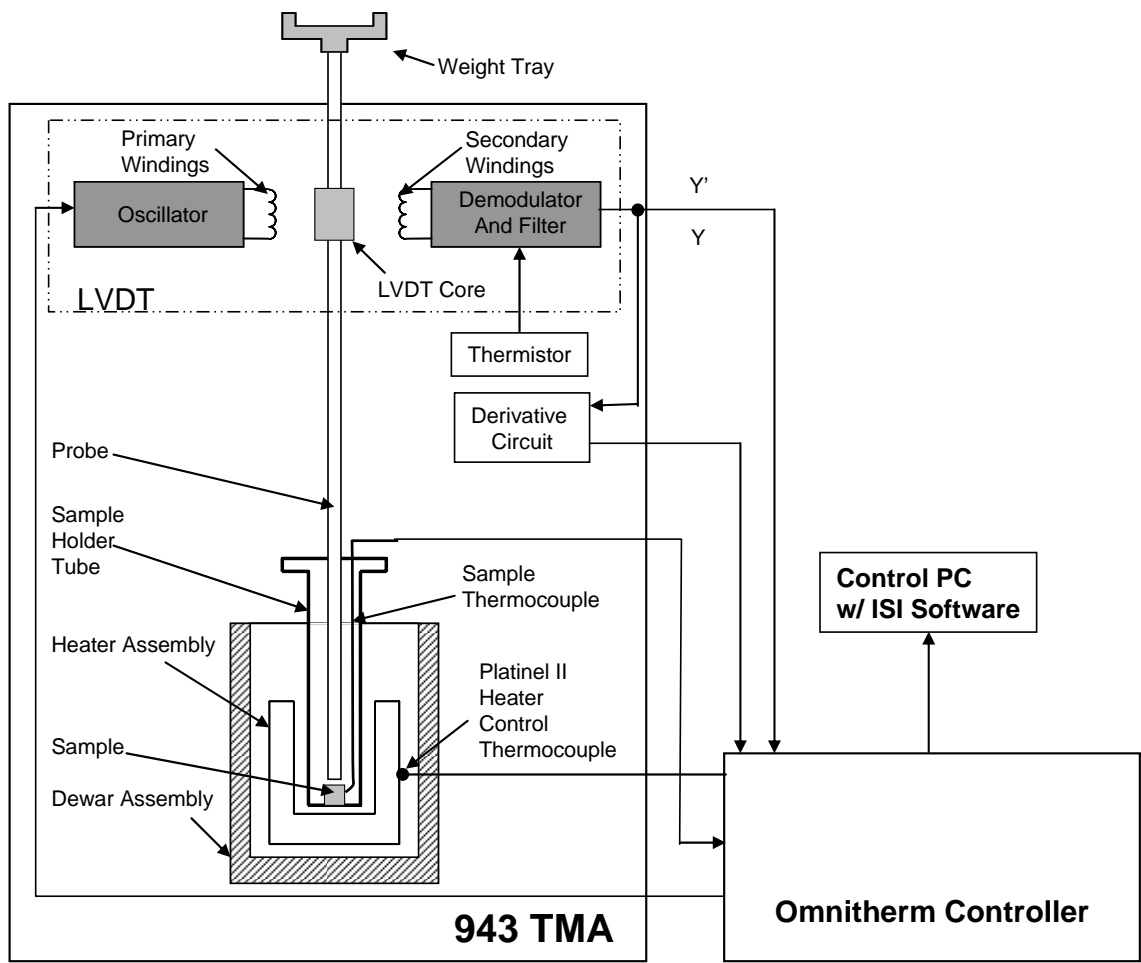
Figure 7.6 - Schematic of TMA Setup
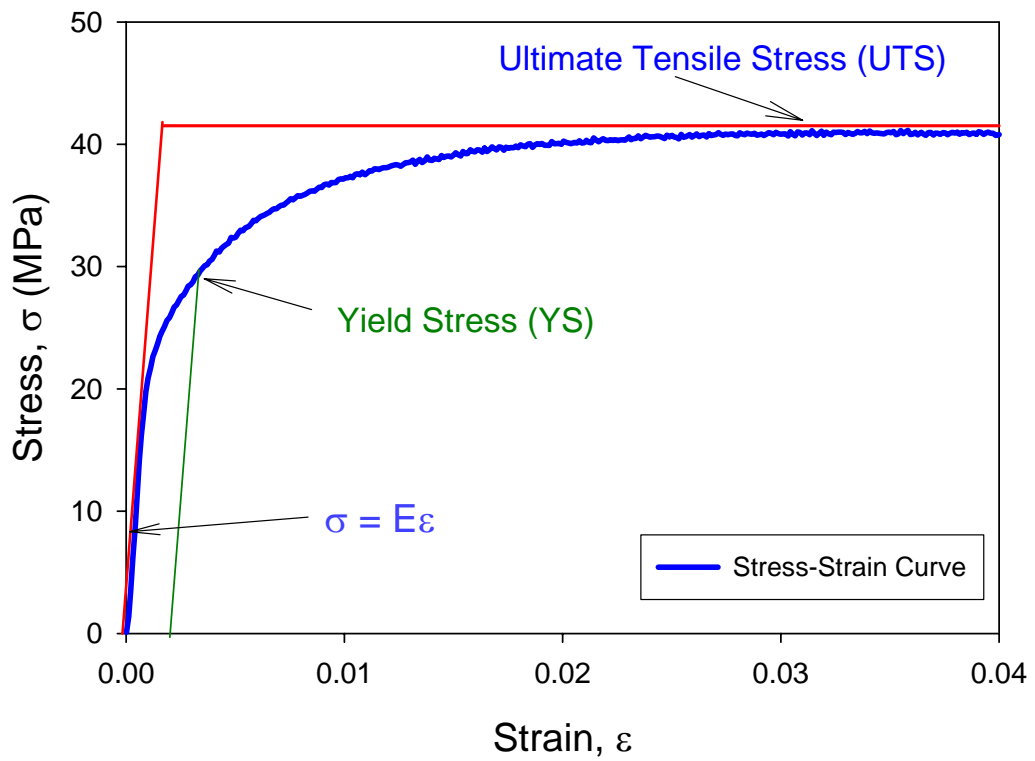
Figure 7.7 - Typical Stress-Strain Curve

are shown in Figure 7.9. The raw stress-strain data for various temperatures are given in Appendix C.

7.2.2 Creep Testing of Underfills

Creep is time dependent deformation of a material caused by application of constant stress. Higher temperatures tend to elevate creep deformation [118]. In an electronics packaging context, creep is an accepted failure mechanism of many packages subjected to thermal or power cycling. Discussions of creep deformation in the context of IC packaging usually begin with creep of solder joints. Figure 7.10 shows a classical representation of a creep curve. Most notable in the case of underfill, is the secondary creep region. In an electronics package, most of the creep deformation occurs here.

To fully characterize the underfill material, creep tests were performed using the micro-tester associated chambers. The tests were performed as a function of both applied stress and temperature. Figure 7.11 shows creep curves grouped by temperature and shown as a function of stress level. Figure 7.12 shows the results at different temperatures with applied stress kept constant.

7.2.3 CTE and Tg of CBGA Test Package Underfill

As part of an electronics package, underfill must expand and contract with temperature in such a way that is compatible with the other components of the package such as the solder balls and substrates. An underfill provides both a thermal path from the chip and aids structural rigidity of the solder balls. The glass transition temperature, Tg, is the temperature where a polymer transitions between glass-like behavior and
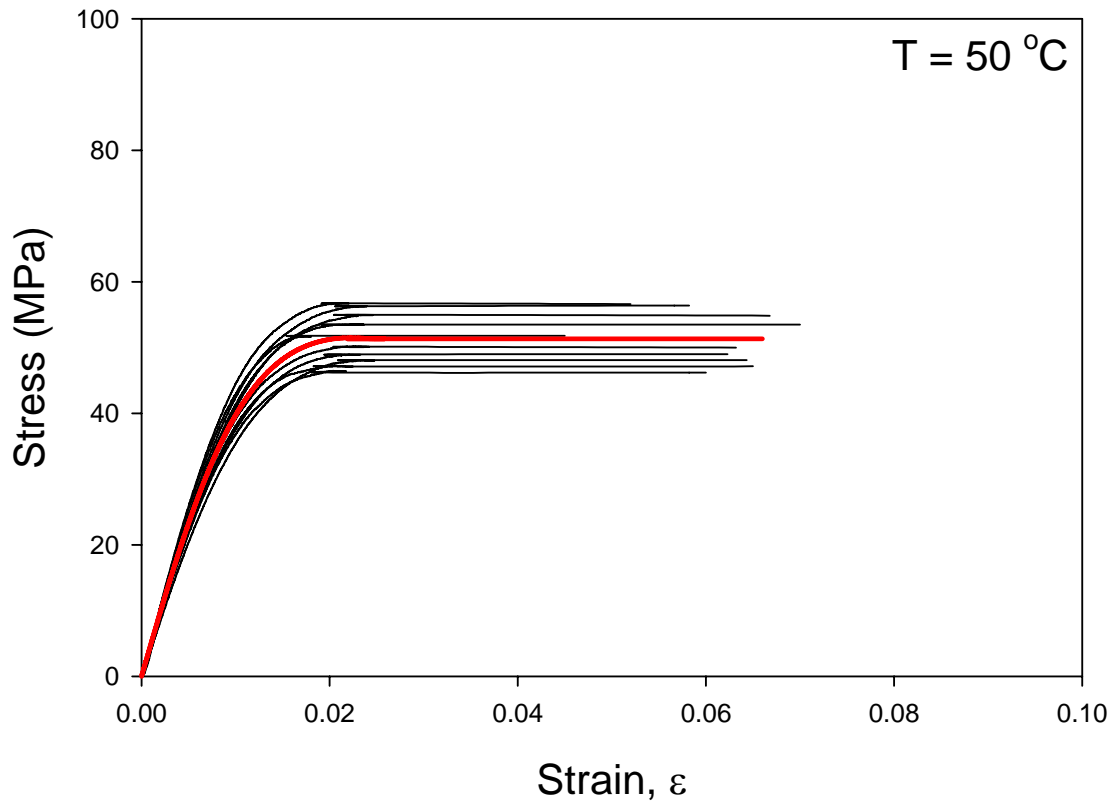
Figure 7.8- Example of Isothermal Stress-Strain Data and Fit (RED)
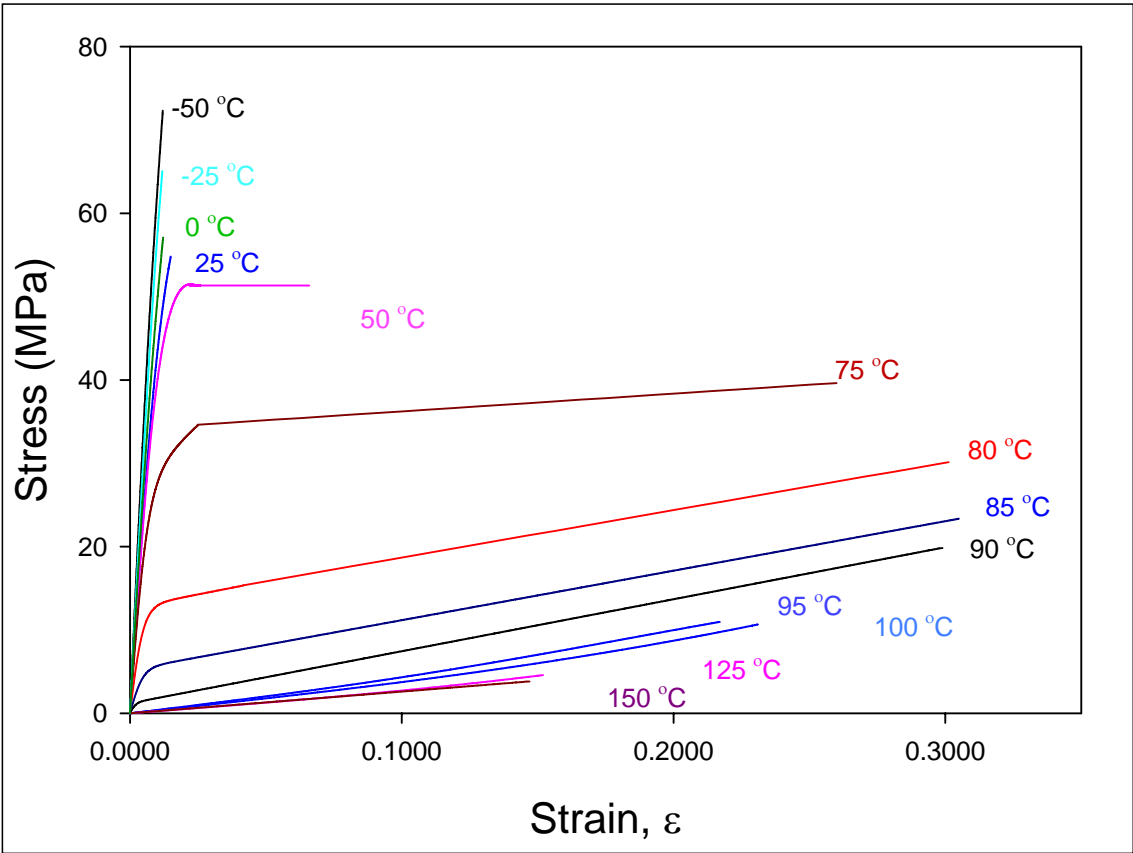
Figure 7.9 - Underfill Stress-Strain Curves as a Function of Temperature
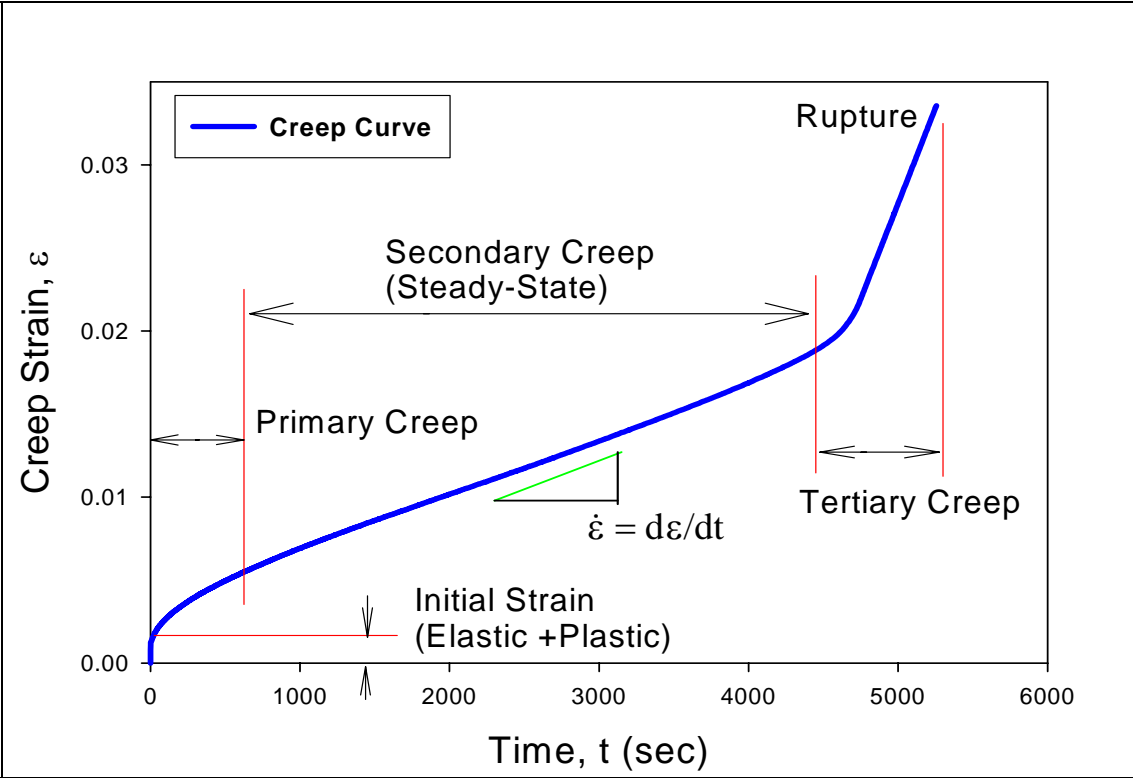
Figure 7.10 - Classical Creep Curve
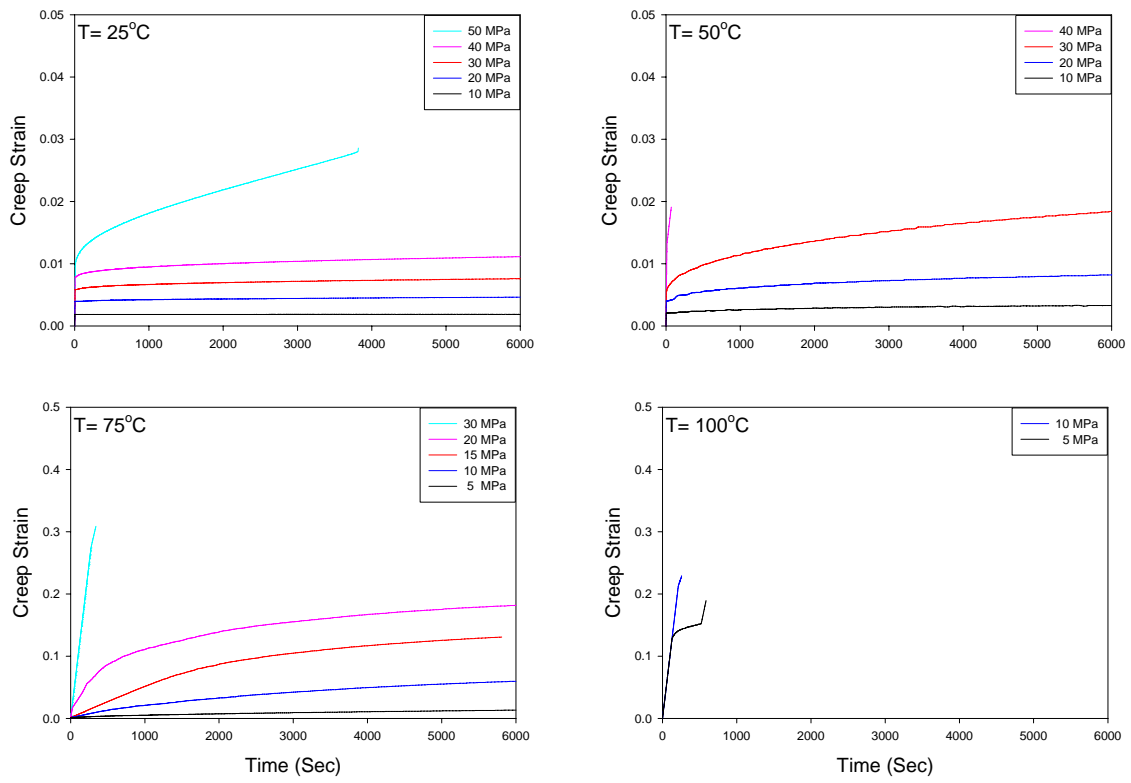
Figure 7.11 - Creep Curves for CBGA Package Underfill
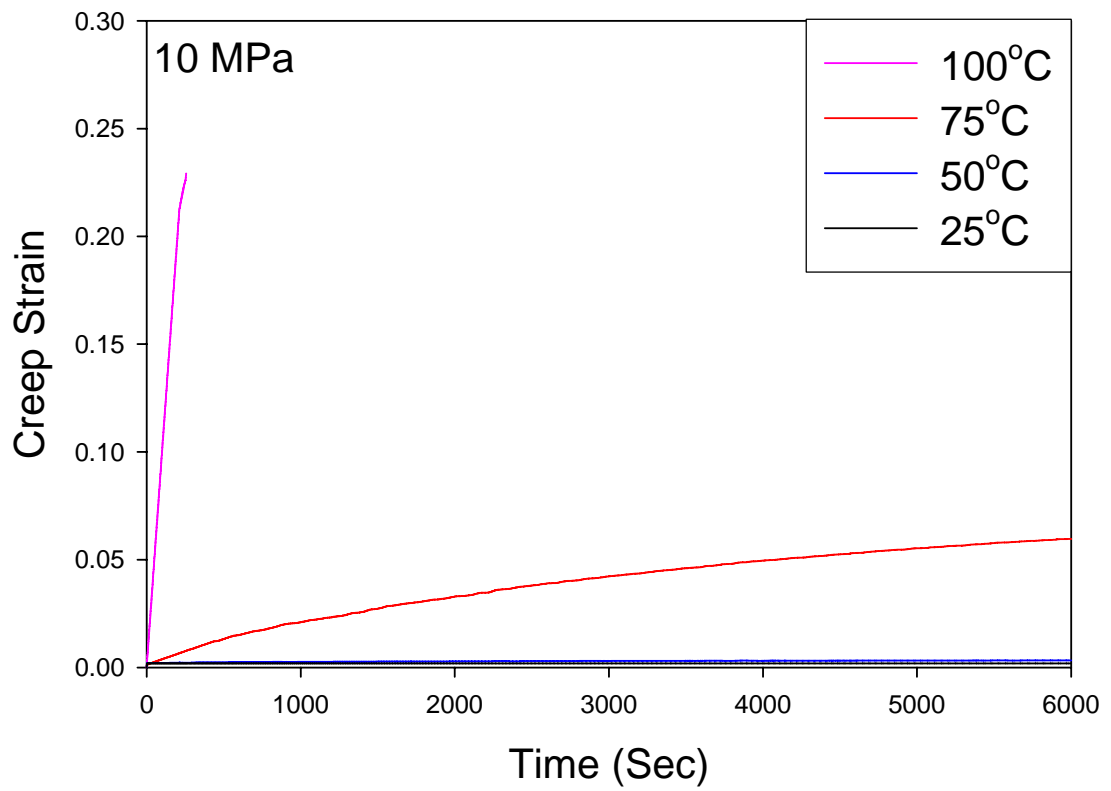
Figure 7.12 - Creep Strain at Constant Applied Stress with Varied Temperature

119

rubbery behavior. It is essentially a measure of the temperature at which the underfill stops lending structural support to the package. A DuPont Instruments Thermomechanical Analyzer was used to measure the glass transition temperature of the underfill samples by monitoring the displacement of the samples as they were heated. Coefficients of thermal expansion and glass transition temperatures for the samples were extracted using Instrument Specialists Thermal Analysis software. Underfill is typically a filled epoxy. Fillers can be glass, rubber, or organics. The material expands with temperature at a certain rate, then moves through a smooth transition, ultimately expanding at a different, higher rate after passing through the glass transition temperature. A typical curve is shown in Figure 7.13. Material properties supplied by the underfill manufacturer are shown in Table 7.2.

Initial testing revealed results not typical for a polymer. The initial region and the final region of the temperature versus displacement plots showed matching CTE results with the vendor values. However, near the glass transition temperature, a region of very high CTE was observed as shown in Figure 7.14. The TMA was recalibrated and the sample was retested. The results were similar, and the glass transition temperature matched the vendor value. The sample was then subjected to testing by a differential scanning calorimeter (DSC), to validate the results from the TMA and to eliminate the TMA apparatus as a source of perceived error. A DSC measures heat flow vs. temperature, but not displacement. The DSC results verified that the glass transition temperature measured by the TMA was accurate. In addition, an underfill supplied from a different vendor was also tested using the TMA, and the results were normal. Thus, the TMA was eliminated as a source of error.

Property		Value
T_g		90 °C
CTE	$< T_g$	44 ppm/°C
	$> T_g$	137 ppm/°C
Elastic Modulus		6.8 GPa

Table 7.2 – Manufacturer Supplied Mechanical Properties
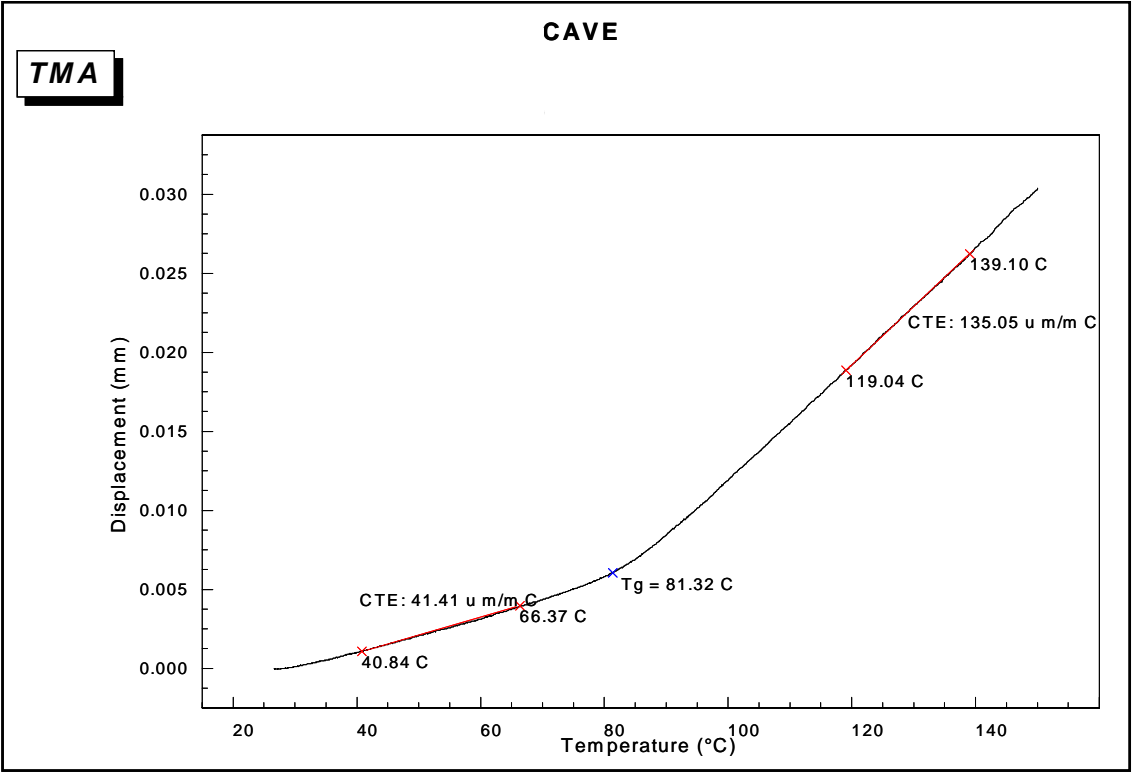
Figure 7.13 - Typical Underfill TMA Data

122

Figure 7.14 - High CTE Behavior of Underfill

At this point, the study shifted from an instrument investigation to a study to determine the root cause of the high CTE region exhibited by the underfill. Several samples were used to perform a repeatability study. Results for the same sample were found to be repeatable as shown in Figure 7.15. Based on advice from a survey of underfill makers, 5 samples were then thermally aged at 100 °C for five hours; slightly above the glass transition temperature of 90 °C, but well below the prescribed cure temperature of 150 °C. An example of the results is shown in Figure 7.16. In the region of previously observed high CTE, a negative CTE, or contraction of the material, was observed. CTE values before and after the glass transition temperature still matched well with previous tests and vendor supplied values. Table 7.3 shows the full results of the testing after the thermal aging exposure.

A second set of samples was then thermal cycled from 0 to 100°C for five cycles. The cycle time was forty minutes with approximately 15 minute dwells at each extreme. The samples were then evaluated using the TMA. Results were similar to those found with thermal aging at 100°C. Results from this thermal cycling exposure experiment are shown in Table 7.4.

A third set of samples was then thermally cycled from 25°C to 150 °C for five cycles. The upper limit of this exposure is equal to the cure temperature prescribed by the vendor. The samples were then evaluated using the TMA. After this thermal exposure, the displacement vs. temperature curves exhibited classic polymer trends and agreement with vendor supplied CTE values and glass transition temperature, as shown in Figure 7.17. Complete results of this elevated temperatures cycling exposure are shown in Table 7.5.

First Measurement

Second Measurement
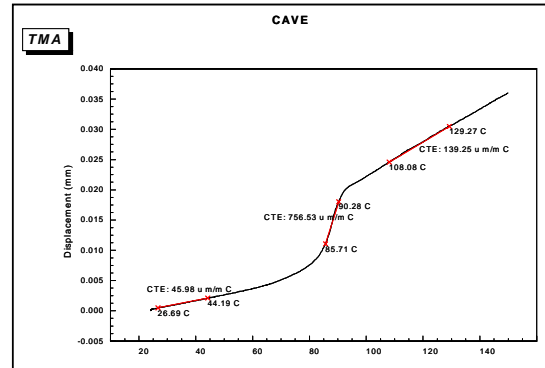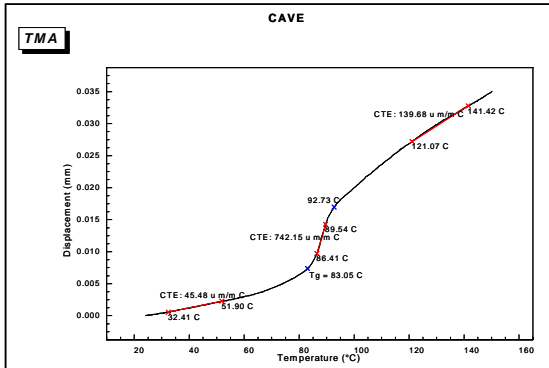
SAMPLE 1
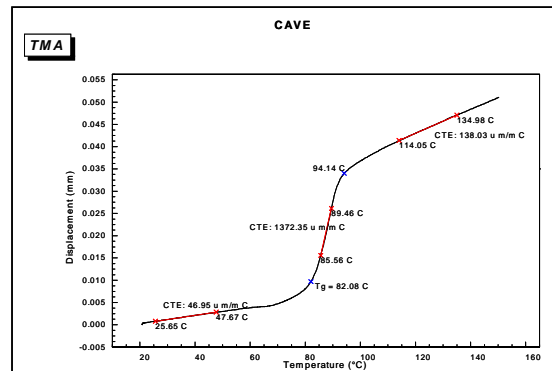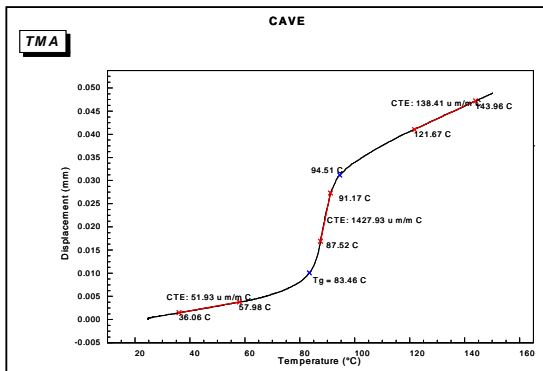
SAMPLE 2

Figure 7.15 - Repeatability of TMA Measurement of Underfill
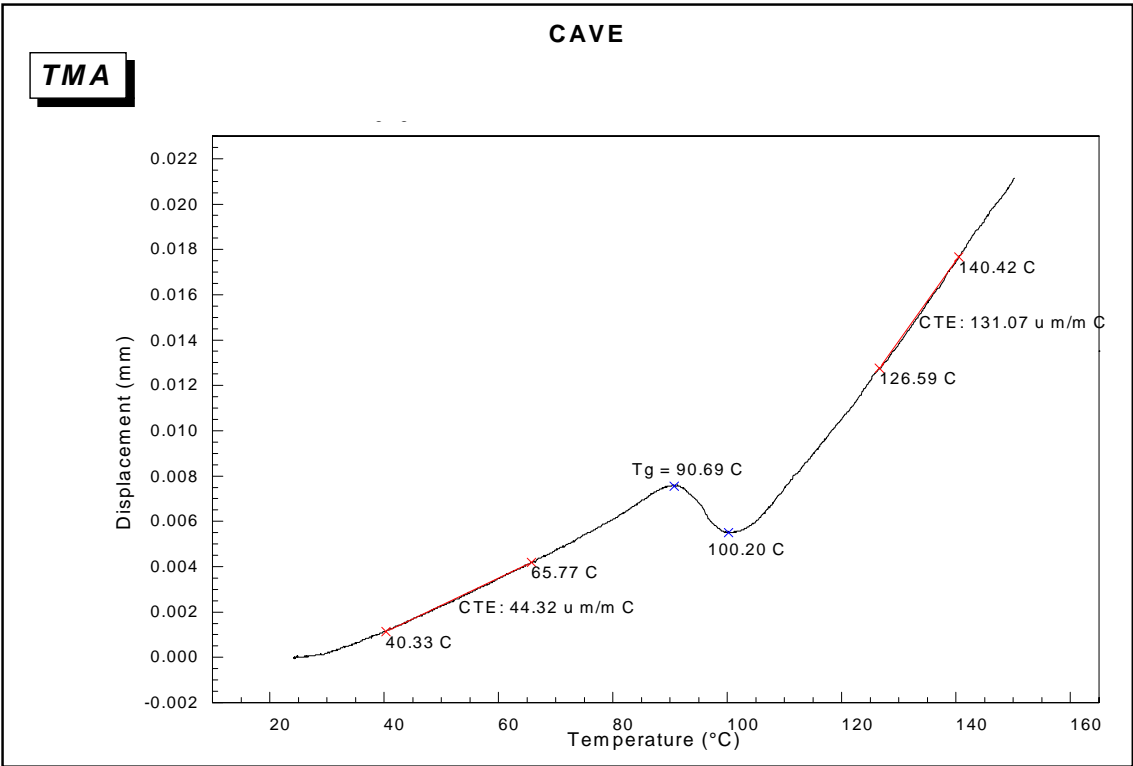
Figure 7.16 - Effect of Thermal Aging & Negative CTE

Underfill Sample	Tg (^{o}C)	CTE (ppm/^{o}C) (25 to 80°C) (Before Tg)	CTE (ppm/^{o}C) (80 to 100°C) (After Tg)	CTE (ppm/^{o}C) (100 to 150°C) (After Tg)
1	81.9	43.0	##	130.8
2	90.7	44.3	##	131.1
3	86.9	46.0	##	133.1
4	85.4	45.3	##	135.7
5	83.9	45.3	##	133.0
Average	85.8	44.8	##	132.7
St. Dev	3.3	1.2	##	2.0

CTE Values were Negative

Table 7.3 - Expansion Results After Thermal Aging

Underfill Sample	Tg (^{o}C)	CTE (ppm/^{o}C) (25 to 80°C) (Before Tg)	CTE (ppm/^{o}C) (80 to 100°C) (After Tg)	CTE (ppm/^{o}C) (100 to 150°C) (After Tg)
1	80.6	45.9	##	137.2
2	83.5	53.2	##	129.5
3	87.6	41.3	##	126.6
4	81.4	46.1	##	130.3
5	81.9	46.8	##	122.1
Average	83.0	46.7	##	129.1
St. Dev	2.8	4.3	##	5.5

CTE Values were Negative

Table 7.4 - Expansion Results After Thermal Cycling

Underfill Sample	Tg (^{o}C)	CTE (ppm/^{o}C) (Before Tg)	CTE (ppm/^{o}C) (After Tg)
1	82.7	44.0	137.4
2	83.9	40.4	130.5
3	80.1	43.0	138.4
4	81.7	43.7	142.4
5	81.3	41.4	135.1
Average	81.9	42.5	136.8
St. Dev	1.4	1.5	4.4

Table 7.5 - Expansion Results After Elevated Thermal Exposure
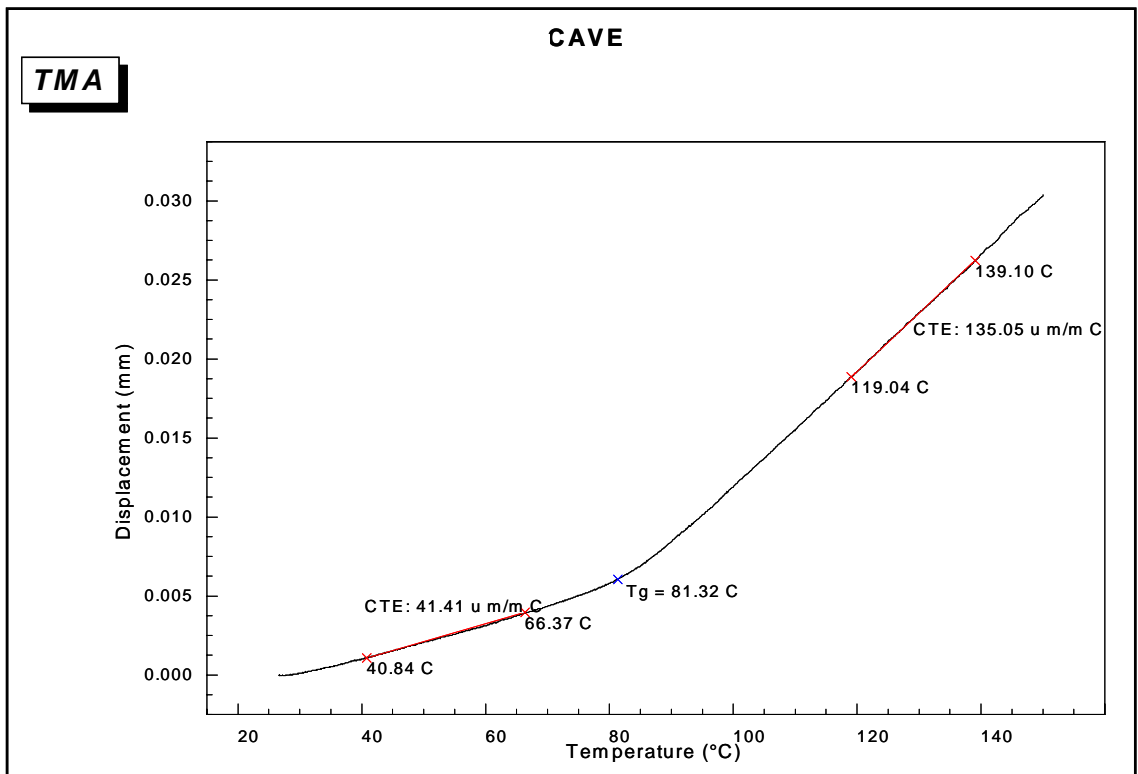
Figure 7.17 - Correct Expansion Properties After Elevated Thermal Exposure

7.3   Summary and Conclusions

The underfill used in the microprocessor packages in this study has been characterized. Temperature dependant stress-strain curves have been recorded and some creep tests have been performed. Elastic modulus and ultimate tensile strength have been found for the underfill, as shown in Figure 7.18. Numerical material property data are also tabulated in Table 7.6. The underfill was found to have strange expansion behavior when tested in the as-cured condition. Various forms of thermal exposure were applied to underfill samples to eliminate this behavior. It was found that when heated to the cure temperature five times, that the odd expansion behavior was eliminated and the underfill exhibited classic polymer thermal expansion response. It is hypothesized that the cure conditions specified by the vendor are incorrect in regard to length of cure.
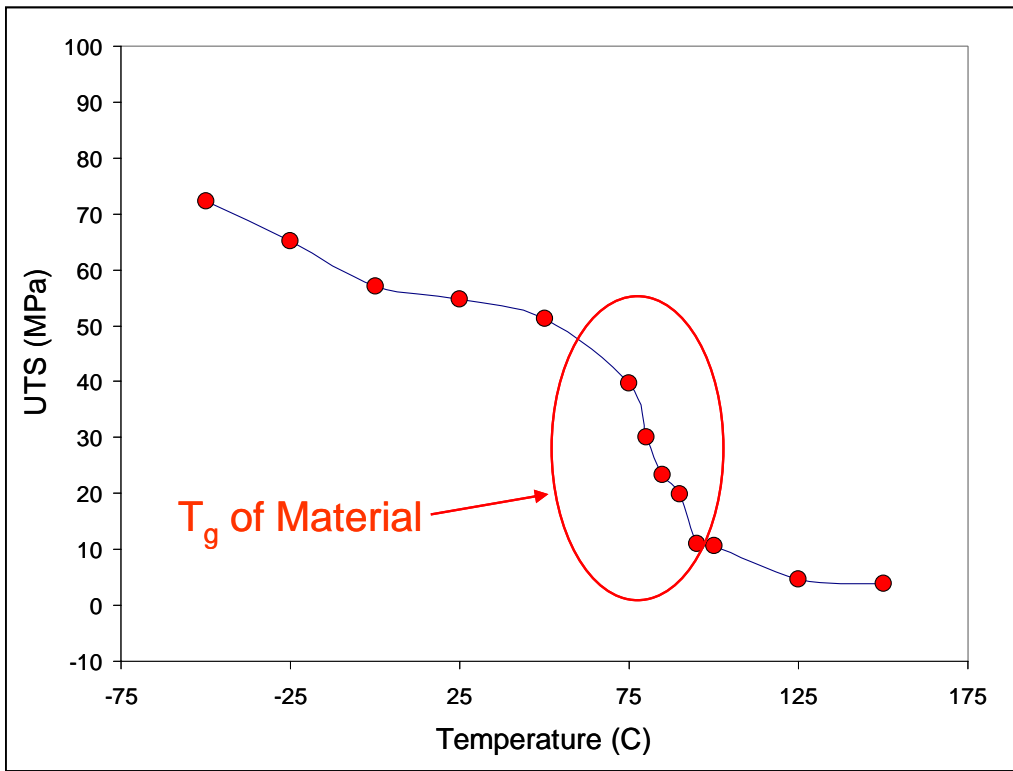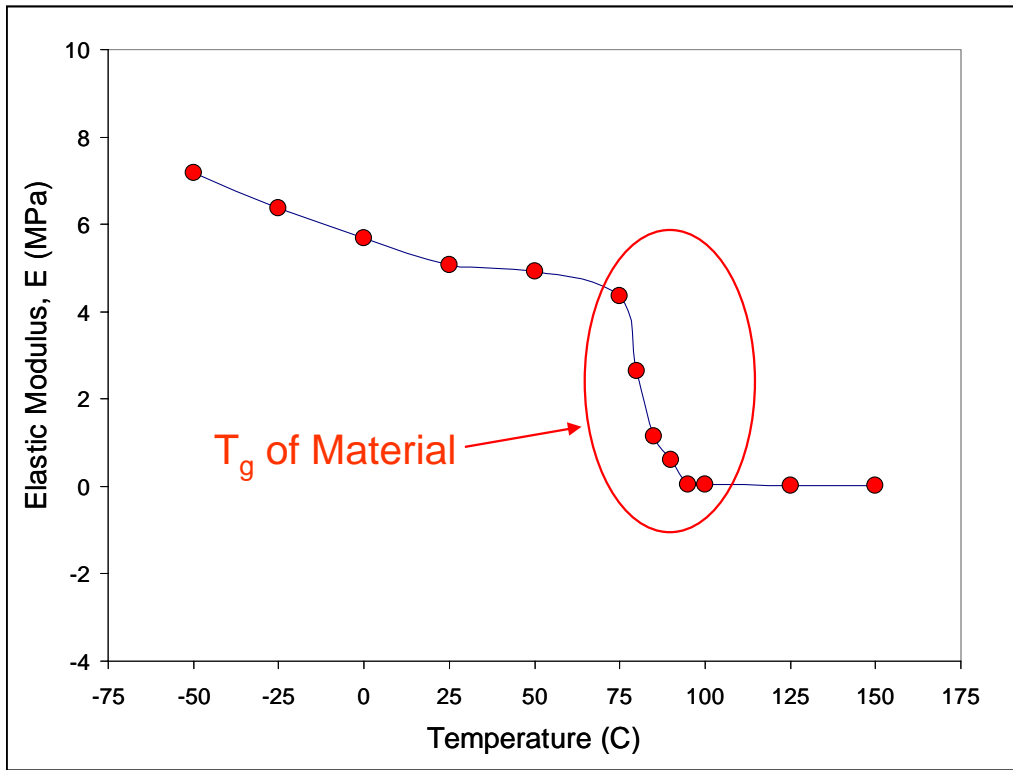
Figure 7.18 - Elastic Modulus and Ultimate Tensile Strength vs. Temperature

Temperature (°C)	Elastic Modulus (MPa)	Ultimate Tensile Strength (MPa)	Failure Strain
-50	7.18	72.20	0.01
-25	6.38	65.10	0.01
0	5.69	57.00	0.01
25	5.06	54.80	0.07
50	4.93	51.33	0.02
75	4.37	39.63	0.07
80	2.65	30.13	0.3
85	1.16	23.34	0.31
90	0.6	19.83	0.3
95	0.04	10.96	0.22
100	0.04	10.66	0.26
125	0.03	4.58	0.23
150	0.03	3.81	0.15

Table 7.6 - Summary of Tensile Properties

BIBLIOGRAPHY

1. Maeda, K., Higashi, M., Kokubu, M., and Nakagawa, S., "The Application of HITCE ceramic material for LGA-type Chip Scale Package, <u>Proceedings of the 50th Electronic Components and Technology Conference</u>, pp. 358-363, 2000.

2. Pendse, R., Afshari, B., Butel, N., Leibovitz, J., Hosoi, Y., Shimada, M., Maeda, K., Maeda, M., and Yonekura, H., "New CBGA Package with Improved 2nd Level Reliability, <u>Proceedings of the 50th Electronic Components and Technology Conference</u>, pp. 1189-1197, 2000.

3. Dai, X., Pan, N., Castro, A., Culler, J., Hussain, M., Lewis, R., and Michalka, T., "High I/O Glass Ceramic Package Pb-Free BGA Interconnect Reliability," <u>Proceedings of the 55th Electronic Components and Technology Conference</u>, pp. 23-29, 2005.

4. Pan, N., Henshall, G. A., Billaut, F., Dai, S., Strum, M. J., Benedetto, E., and Rayner, J., "An Acceleration Model for Sn-Ag-Cu Solder Joint Reliability Under Various Thermal Cycle Conditions," <u>Proceedings of the 2005 SMTA International Conference</u>, pp. 876-883, 2005.

5. Teng, S. Y., and Brillhart, M., "Reliability Assessment of a High CTE CBGA for High Availability Systems," <u>Proceedings of the 52nd Electronic Components and Technology Conference</u>, pp. 611-616, 2002.

6. Tosaya, E., Ouimet, S., Martel, R., and Lord, R., "Router Flip Chip Packaging Solution and Reliability," <u>Proceedings of the 54th Electronic Components and Technology Conference</u>, pp. 1153-1160, 2004.

7. Butel, N., "Comparison of the Level 2 Characteristics of HITEC Substrate Assembled with SAC and High Lead Balls," <u>Proceedings of the 2007 SMTA International Conference</u>, pp. 1-10, 2007.

8. Peterson, D. W., Burchett, S. N., Sweet, J. N. and Mitchell, R. T., "Calculation and Validation of Thermomechanical Stresses in Flip Chip BGA Using the ATC4.2 Test Vehicle," <u>Proceedings of the 49th Electronic Components & Technology Conference</u>, pp. 1241-1248, San Diego, CA, June 1-4, 1999.

9. Palaniappan, P., Selman, P., Baldwin, D., Wu, J. and Wong, C. P., "Correlation of Flip Chip Underfill Process Parameters and Material Properties with In-Process Stress Generation," <u>IEEE Transactions on Electronics Packaging Manufacturing</u>, Vol. 22(1), pp. 53-62, 1999.

10. Palaniappan, P. and Baldwin, D. F., "In Process Stress Analysis of Flip Chip Assemblies During Underfill Cure," <u>Microelectronics and Reliability</u>, Vol. 40(7), pp. 1181-1190. 2000.

11. Suhling, J. C., Johnson, R., Mian, A.K.M., Rahim, M., Zou., Y., Ellis, C., Ragam, S., Palmer, M., and Jaeger, R., "Measurement of Backside Flip Chip Die Stresses using Piezoresistive Test Die," <u>32nd International Symposium on Microelectronics</u>, IMAPS, pp. 298-303, Chicago, IL, October 26-28, 1999.

12. Rahim, M. K., Suhling, J. C., Copeland, D. S., Islam, M. S., Jaeger, R. C., Lall, P., Johnson, R. W., "Die Stress Characterization in Flip-Chip Assemblies," <u>IEEE Transactions on Components and Packaging Technologies</u>, Vol. 28(3), pp. 415-429, 2005.

13. Rahim, M. K., Suhling, J. C., Copeland, D. S., Islam, M. S., Jaeger, R. C., Lall, P., Johnson, R. W., "Measurement of Thermally Induced Die Stresses in Flip Chip on Laminate Assemblies," <u>Proceedings of ITHERM 2004</u>, pp. 1-12, Las Vegas, NV, June 1-4, 2004.

14. Rahim, M. K., Suhling, J. C., Jaeger, R. C., and Lall, P., "Fundamentals of Delamination Initiation and Growth in Flip Chip Assemblies," <u>Proceedings of the 55th IEEE Electronic Components and Technology Conference</u>, pp. 1172-1186, Orlando, FL, June 1-3, 2005.

15. Dale, J. R., and Oldfield, R. C., "Mechanical Stresses Likely to be Encountered in the Manufacture and Use of Plastically Encapsulated Devices," <u>Microelectronics and Reliability</u>, Vol. 16, pp. 255-258, 1977.

16. Lau, J., <u>Thermal Stress and Strain in Microelectronics Packaging</u>, Van Nostrand Reinhold, 1993.

17. Inayoshi, H., "Moisture-Induced Aluminum Corrosion and Stress on the Chip in Plastic Encapsulated LSI's," <u>Proceeding of 17th Annual Reliability Physics Symposium</u>, IEEE, pp. 113-119, 1979.

18. Lesk, L. A., Thomas, R. E., Hawkins, G., Remmel, T. P., and Rugg, J., "Progression of Damage Caused by Temperature Cycling on a Large Die in a Molded Plastic Package," <u>Proceedings of the 40th Electronic Components and Technology Conference</u>, IEEE, pp. 807-812, Las Vegas, NV, May 20-23, 1990.

19. Edwards, D. R., Heinen, K. G., Martinez, J. E., and Groothuis, S., "Shear Stress Evaluation of Plastic Packages," <u>Proceedings of the 37th Electronic Components Conference</u>, IEEE, pp. 84-95, 1987.

20. Nishimura, A., Kawai, S., and Murakami, G., "Effect of Lead Frame Material on Plastic-Encapsulated IC Package Cracking Under Temperature Cycling," <u>IEEE Transactions on Components, Hybrids, and Manufacturing Technology</u>, Vol. 12(4), pp. 639-645, 1989.

21. Nishimura, A., Tatemichi, A., Miura, H., and Sakamoto, T., "Life Estimation for IC Plastic Packages Under Temperature Cycling Based on Fracture Mechanics," <u>IEEE Transactions on Components, Hybrids, and Manufacturing Technology</u>, Vol. 10(4), pp. 637-642, 1987.

22. van Kessel, C. G. M., Gee, S. A., and Murphy, J. J., "The Quality of Die-Attachment and Its Relationship to Stresses and Vertical Die-Cracking," <u>IEEE Transactions on Components, Hybrids, and Manufacturing Technology</u>, Vol. 6(4), pp. 414-420, 1983.

23. van Kessel, C. G. M., and Gee, S. A., "The Use of Fractography in the Failure Analysis of Die Cracking," in <u>Proceeding of the International Symposium for Testing and Failure Analysis</u>, Los Angeles, CA, 1984.

24. Suhir, E., "Die Attachment Design and Its Influence on Thermal Stresses in the Die and the Attachment," <u>Proceedings of 37th Electronic Components Conference</u>, pp. 508-517, 1987.

25. Suhir, E., "Analytical Modeling in Electronic Packaging Structures. Its Merits, Shortcomings and Interaction with Experimental and Numerical Techniques," <u>Journal of Electronic Packaging</u>, Vol. 111(2), pp. 157-161, 1989.

26. Liew, H. L., Yasir, A. Q., Hassan, A. Y., and Seetharamu, K. N., "Engineering Model for Thermal Mismatch Stresses at the Interface of a Non-Uniformly Heated Two Layer Structure," <u>International Journal of Microcircuits and Electronic Packaging</u>, Vol. 21(2), pp. 186-190, 1998.

27. Tay, A. A. O., and Lin, T. Y., "Moisture Diffusion and Heat Transfer in Plastic IC Packages," <u>IEEE Transactions on Components, Hybrids, and Manufacturing Technology</u>, Part A, Vol. 19(2), pp. 186-193, 1996.

28. Tay, A. A. O., and Lin, T. Y., "Effects of Moisture and Delamination on Cracking of Plastic IC Packages during Solder Reflow," <u>Proceedings of 46th Electronic Components and Technology Conference</u>, pp. 777-782, Orlando, FL, 1996.

29. Tay, A. A. O., and Lin, T. Y., "Moisture-Induced Interfacial Delamination Growth in Plastic IC Packages during Solder Reflow," <u>Proceedings of 48th Electronic Components and Technology Conference</u>, pp. 371-378, Seattle, WA, 1998.

30. Bastawros, A. F., and Voloshin, A. S., "Transient Thermal Strain Measurements in Electronic Packages," <u>IEEE Transactions on Components Hybrids & Manufacturing Technology</u>, Vol. 13(4), pp. 961-966, 1990.

31. Han, B., and Guo, Y., "Thermal Deformation Analysis of Various Electronic Packaging Products by Moiré and Microscopic Moiré Interferometry," <u>Journal of Electronic Packaging</u>, Vol. 117(3), pp. 185-191, 1995.

32. Liu, S., Zhu, J., Zou, D., and Benson, J., "Study of Delaminated Plastic Packges by High Temperature Moiré and Finite Element Method," <u>IEEE Transactions on</u>

Components, Hybrids, and Manufacturing Technology, Part A, Vol. 20(4), pp. 502-512, 1997.

33. Liu, S., Hsu, S. C., and Tung, Y. C., "Thermal Deformation Analysis of a Plastic Quad Flat Packages by Hybrid Moiré and Finite Element Method," Thermo-Mecanical Characterization of Evolving Packaging Materials and Structures, ASME, EEP-Vol. 24, pp. 51-58, 1998.

34. Stiteler, M., and Ume, C., "System for Real-Time Measurements of Thermally Induced Warpage in a Simulated Infrared Solding Environment," Journal of Eletronic Packaging, Vol. 119, pp. 1-7, 1997.

35. Wang, Y., and Hassell, P., "On-Line Measurement of Thermally Induced Warpage of BGAs with High Sensitivity Shadow Moiré," International Journal of Microcircuits and Electronic Packaging, Vol. 21(2), pp. 191-196, 1998.

36. Voloshin, A. S., Tsao, P., Polak, A., J., and Baker, T., L., "Analysis of Environment Induced Stresses in Silicon Sensors," Proceedings of InterPACK '95, EEP Vol. 10(1), pp. 489-492, 1995.

37. Guo, Y., and Sarihan, V., "Testing and Measurment Techniques Applied to Electronic Packaging Development," Applications of Experimental Mechanics to Electronic Packaging, ASME, EEP-Vol. 22, pp. 85-90, 1997.

38. Smith, C. S., "Piezoresistance Effect in Germanium and Silicon," Physical Review, Vol. 94, pp. 42-49, 1954.

39. Tufte, O. N., and Stezer, E. L., "Piezoresistive Properties of Silicon Diffused Layers," Journal of Applied Physics, Vol. 34(2), pp. 313-318, 1963.

40. Suhling, J. C., Beaty, R. E., Jaeger, R. C., and Johnson, R. W., "Piezoresistive Sensors for Measurement of Thermally-Induced Stresses in Microelectronics," Proceedings of the 1991 Spring Conference of the Society for Experimental Mechanics, pp. 683-694, Milwaukee, WI, June 10-13, 1991.

41. Suhling, J. C., Carey, M. T., Johnson, R. W., and Jaeger, R. C., "Stress Measurement in Microelectronic Packages Subjected to High Temperature," in Manufacturing, Processes and Materials Challenges in Microelectronic Packaging, ASME, EEP-Vol. 1, pp. 143-152, 1991.

42. Yamada, K., Nishihara, M., Shimada, S., Tanabe, M., Shimazoe, M., and Matsouka, Y., "Nonlinearity of the Piezoresistance Effect of P-Type Silicon Diffused Layers," IEEE Transactions on Electron Devices, Vol. 29(1), pp. 71-77. 1982.

43. Kanda, Y., "A Graphical Representation of the Piezoresistance Coefficients in Silicon," IEEE Transactions on Electron Device, Vol. 29(1), pp. 64-70, 1982.

44. Dally, J. W., and Riley, W. F., Experimental Stress Analysis, 4th Edition. McGraw-Hill, 2001.

45. Bittle, D. A., <u>Piezoresistive Stress Sensors for Integrated Circuits</u>, M.S. Thesis, Auburn University, Auburn, AL, 1990.

46. Bittle, D. A., Suhling, J. C., Beaty, R. E., Jaeger, R. C., and Johnson, R. W., "Piezoresistive Stress Sensors for Structural Analysis of Electronic Packages," <u>Journal of Electronic Packaging</u>, Vol. 113(3), pp. 203-215, 1991.

47. Kang, Y., <u>Piezoresistive Stress Sensors for Advanced Semiconductor Materials</u>, Ph.D. Dissertation, Auburn University, Auburn, AL, 1997.

48. Beaty, R. E., Suhling, J. C., Moody, C. A., Bittle, D. A., Johnson, R. W., Butler, R. D., and Jaeger, R. C., "Calibration Considerations for Piezoresistive-Based Stress Sensors," <u>Proceedings of the 40th Electronic Components and Technology Conference</u>, IEEE, pp. 797-806, 1990.

49. Suhling, J. C., Jaeger, R. C., and Ramani, R., "Stress Measurement Using 0-90 Piezoresistive Rosettes on (111) Silicon," <u>Proceedings of the 1994 International Mechanical Engineering Congress and Exposition.</u> Chicago, IL, AMD-Vol. 195, pp. 65-73, 1994.

50. Jaeger, R. C., Suhling, J. C., Carey, M. T., and Johnson, R. W., "A Piezoresistive Sensor Chip for Measurement of Stress in Electronic Packaging," <u>Proceedings of the 43th Electronic Components and Technology Conference</u>, IEEE, pp. 686-692, 1993.

51. Jaeger, R. C., Suhling, J. C., and Anderson, A. A., "A (100) Silicon Stress Test Chip with Optimized Piezoresistive Sensor Rosettes," <u>Proceedings of 44th Electronic Components and Technology Conference</u>, pp. 741-749, Washington, DC, May 1-4, 1994.

52. Jaeger, R. C., Suhling, J. C., Carey, M. T., and Johnson, R. W., "Off-Axis Piezoresistive Sensors for Measurement of Stress in Electronic Packaging," <u>IEEE Transactions on Components, Hybrids, and Manufacturing Technology (CHMT- Advanced Packaging)</u>, Vol. 16(8), pp. 925-931, 1993.

53. Jaeger, R. C., Suhling, J. C., and Ramani, R., "Thermally Induced Errors in the Application of Silicon Piezoresistive Stress Sensors," <u>Advances in Electronic Packaging 1993 - Proceedings of the 1993 ASME International Electronic Packaging Conference</u>, pp. 457-470, Binghamton, NY, September 29-October 2, 1993.

54. van Gestel, R., <u>Reliability Related Research on Plastic IC-Packages: A Test Chip Approach</u>, Ph.D. Thesis, Delft Technical University, Delft University Press, 1994.

55. Kang, Y., Mian, A. K. M., Suhling, J. C., and Jaeger, R. C., "Hydrostatic Response of Piezoresistive Stress Sensors," <u>Application of Experimental Mechanics to Electronic Packaging - 1997</u>, ASME, EEP-Vol. 22, pp. 29-36, 1997.

56. Cordes, R. A., <u>Wafer Level Calibration Of Piezoresistive Stress Sensors</u>, M.S. Thesis, Auburn University, Auburn, AL, 1995.

57. Suhling, J. C., Jaeger, R. C., Kang, Y. L., and Cordes, R. A., "A New Wafer-Level Calibration Procedure for Piezoresistive Stress Sensors," <u>Proceedings of the 1993 SEM Spring Conference on Experimental Mechanics</u>, pp. 977-987, Dearborn, MI, June 7-9, 1993.

58. Suhling, J. C., Cordes, R. A., Kang, Y. L., and Jaeger, R. C., "Wafer-Level Calibration of Stress Sensing Test Chips," <u>Proceedings of the 44th Electronic Components and Technology Conference</u>, pp. 1058-1070, 1994.

59. Lwo, B., and Wu, S., "Calibrate Piezoresistive Stress Sensors through the Assembled Structure," <u>Journal of Electronic Packaging</u>, Vol. 125(2), pp. 289-293, 2003.

60. Lwo, B., Chen, T., Kao, C., and Lin, Y., "In-plane Packaging Stress Measurements through Piezoresistive Sensors," <u>Journal of Electronic Packaging</u>, Vol. 124(2), pp. 115-121, 2002.

61. Lwo, B., Kao, C., Chen, T., and Chen, Y., "On the Study of Piezoresistive Stress Sensors for Microelectronic Packaging," <u>Journal of Electronic Packaging</u>, Vol. 124(1), pp. 22-26, 2002.

62. Groothuis, S., Schroen, W. H., and Murtuza, M., "Computer Aided Stress Modeling for Optimizing Plastic Package Reliability," <u>Proceeding of 23th Annual Reliability Physics Symposium</u>, pp. 182-191, 1985.

63. Gee, S. A., van den Bogert, W. F., and Akylas, V. R., "Strain-Gauge Mapping of Die Surface Stresses," <u>IEEE Transactions on Components, Hybrids, and Manufacturing Technology</u>, Vol. 12(4), pp. 587-593, 1989.

64. van Gestel, H. C. J. M., van Gemert, L., and Bagerman, E., "On-Chip Piezoresistive Stress Measurement and 3D Finite Element Simulations of Plastic DIL 40 Packages using Different Materials," <u>Proceedings of the 43th Electronic Components and Technology Conference</u>, pp. 124-133, Orlando, FL, June 1-4, 1993.

65. Miura, H., Nishimura, A., Kawai, S., and Nishi, K., "Development and Application of Stress-Sensing Test Chip for IC Plastic Packages," <u>Transactions of the Japan Society of Mechanical Engineers</u>, Vol. 53(493-A), pp. 1826-1832, 1987.

66. Miura, H., Nishimura, A., Kawai, S., and Nishi, K., "Residual Stress in Resi-Molded IC Chips," <u>Transactions of the Japan Society of Mechanical Engineers</u>, Vol. 55(516-A), pp. 1763-1770, 1989.

67. Miura, H., Nishimura, A., Kawai, S., and Murakami, G., "Structural Effect of IC Plastic Package on Residual Stress in Silicon Chips," <u>Proceedings of the 40th Electronic Components and Technology Conference</u>, IEEE, pp. 316-321, Las Vegas, NV, May 20-23, 1990.

68. Miura, H., and Nishimura, A., "Device Characteristic Changes Caused by Packaging Stress," <u>Mechanics and Materials for Electronic Packaging</u>, ASME, AMD-Vol. 195, pp. 101-109, 1994.

69. Miura, H., Kitano, M., Nishimura, A., and Kawai, S., "Thermal Stress Measurement in Silicon Chips Encapsulated in IC Plastic Packages under Thermal Cycling," <u>Journal of Electronic Packaging</u>, Vol. 115(1), pp. 9-15, 1993.

70. Zou, Y., <u>Application of Silicon Piezoresistive Stress Test Chips in Electronic Packages</u>, Ph.D. Dissertation, Auburn University, Auburn, AL, 1999.

71. Zou, Y., Suhling, J. C., Jaeger, R. C., Lin, S. T., Nguyen, L., and Gee, S., "Characterization of Plastic Packages Using (100) Silicon Stress Test Chips," <u>Application of Experimental Mechanics to Electronic Packaging - 1997</u>, ASME, EEP-Vol. 22, pp. 15-21, 1997.

72. Zou, Y., Suhling, J. C., Johnson, R. W., and Jaeger, R. C., "Complete Stress State Measurements in Chip on Board Packages," <u>Proceedings of MCM '98</u>, IMAPS, pp. 425-435, Denver, CO, April 15-17, 1998

73. Sweet, J. N., "Die Stress Measurement Using Piezoresistive Stress Sensors," in <u>Thermal Stress and Strain in Microelectronics Packaging</u>, Edited by J. Lau, Von Nostrand Reinhold, 1993.

74. Sweet, James N., Peterson, David W., and Hsia, Alex H., "Design and Experimental Evaluation of a 3rd Generation Addressable CMOS Piezoresistive Stress Sensing Test Chip," <u>Proceeding of InterPACK '99</u>, pp. 205-213, Lahaina, HI, June 13-19, 1999.

75. Bossche, A., "On-Chip Stress, Metal Deformation and Moisture Measurements," <u>Microelectronics and Reliability</u>, Vol. 32(11), pp. 1633-1637, 1992.

76. Bossche, A., and Mollinger, J. R., "Calibration Procedure for Piezoresistance Coefficients of Polysilicon Sheets and Application to a Stress Test Chip," <u>Sensors & Actuators A-Physical</u>, Vol. 62(1-3), pp. 475-479, 1997.

77. Lo, T. C. P., Chan, P. C. H., and Tang, Z., "Design And Characterization of a Micro Strain Gauge," <u>Proceedings of the 1995 IEEE Region 10 International Conference on Microelectronics and VLSI, TENCON '95</u>, pp. 36-39, Hong Kong, 1995.

78. Lo, T. C. P., and Chan, P. C. H., "Design and Calibration of a 3-D Micro-Strain Gauge for In Situ on Chip Stress Measurements," <u>Proceedings of the 1996 IEEE International Conference on Semiconductor Electronics</u>, ICSE, pp 252-255, Penang, Malaysia, 1996.

79. Suhling, J. C., and Jaeger, R. C., "Silicon Piezoresistive Stress Sensors and Their Application in Electronic Packaging," <u>IEEE Sensors Journal</u>, Vol. 1(1), pp. 14-30, 2001.

80. Suhling, J. C., Jaeger, R. C., Lin, S. T., Moral, R. J., and Zou, Y., "Measurement of the Complete Stress State in Plastic Encapsulated Packages," Proceedings of InterPACK '97, pp. 1741-1750, Kohala, HI, June 15-19, 1997.

81. Suhling, J. C., Jaeger, R. C., Wilamowski, B. M., Lin, S. T., Mian, A. K. M., and Cordes, R. A., "Design and Calibration of Optimized (111) Silicon Stress Sensing Test Chips," Proceedings of InterPACK '97, pp. 1723-1730, Kohala, HI, June 15-19, 1997.

82. Suhling, J. C., Lin, S. T., Moral, R. J., Johnson, R. W., and Jaeger, R. C., "Measurement of Die Stress in Advanced Electronic Packaging for Space and Terrestrial Applications," Proceedings of STAIF-97, American Institute of Physics Conference Proceedings #387, pp. 819-824, Albuquerque, NM, January 26-30, 1997.

83. Schwizer, J., Mayer, M., Bolliger, D., Paul, O., and Baltes, H., "Thermosonic Ball Bonding: Friction Model Based on Integrated Microsensor Measurements," Proceedings of the IEEE/CPMT International Electronics Manufacturing Technology (IEMT) Symposium, pp. 108-114, Austin,TX, October 18-19, 1999.

84. Schwizer, J., Song, W. H., Mayer, M., Brand, O., and Baltes, H., "Packaging Test Chip for Flip-Chip and Wire Bonding Process Characterization," Proceedings of the 12th International Conference on Transducers, Solid-State Sensors, Actuators and Microsystems, pp. 440-443, Boston, MA, June 8-12, 2003.

85. Jaeger, R. C., Ramani, R., and Suhling, J. C., "Effects of Stress-Induced Mismatches on CMOS Analog Circuits," Proceedings of the International Symposium on VLSI Technology, Systems, and Applications, pp. 354-360, Taipei, Taiwan, 1995.

86. Jaeger, R. C., Ramani, R., Suhling, J. C., and Kang, Y., "CMOS Stress Sensor Circuits Using Piezoresistive Field-Effect Transistors (PIFET's)," Proceedings of 1995 Symposium on VLSI Circuit Design and Technology, pp. 43-44, Kyoto, Japan, 1995.

87. Jaeger, R. C., and Suhling, J. C., "Advances in Stress Test Chips," Application of Experimental Mechanics to Electronic Pakcaging-1997, ASME, EEP-Vol. 22, pp.1-5, Dallas, TX, 1997.

88. Jaeger, R. C., Suhling, J. C., Bradley, A. T., and Xu, J., "Silicon Piezoresistive Stress Sensors Using MOS and Bipolar Transistors," Proceeding of InterPACK '99, pp. 219-226, Lahaina, HI, June 13-19, 1999.

89. Jaeger, R. C., Suhling, J. C., Ramani, R., Bradley, A. T., and Xu, J., "CMOS Stress Sensors on (100) Silicon," IEEE Journal of Solid-State Circuits, Vol. 35(1), pp. 85-95, 2000.

90. Ramani, R., Piezoresistive Behavior of MOSFET and FET-Based Stress Sensor Circuit, Ph.D. Dissertation, Auburn University, 1996.

141

91. Bradley, A. T., <u>Piezoresistive Behavior of MOSFETs and MOS Circuits</u>, Ph.D. Dissertation, Auburn University, 1999.

92. Xu, J., <u>CMOS Piezoresistive Stress Sensors on (111) Silicon</u>, Ph.D. Dissertation, Auburn University, 2000.

93. Mian, A. K. M., Suhling, J. C., and Jaeger, R. C., "Sensitivity of Van der Pauw Sensors to Uniaxial Stress," <u>ASME Advances in Electronic Packaging</u>, EEP-Vol. 26, No 1, pp. 195-203, Jun 13-Jun 19 1999.

94. Mian, A. K. M., <u>Application of the Van der Pauw Structure as a Piezoresistive Stress Sensor</u>, Ph.D. Dissertation, Auburn University, 2000.

95. Mayer, M., Schwizer, J., Paul, O., Bolliger, D., and Baltes, H., "In-situ Ultrasonic Stress Measurements During Ball Bonding Using Integrated Piezoresistive Microsensors," <u>Proceeding of InterPACK '99</u>, pp. 973-978, Lahaina, HI, June 13-19, 1999.

96. Mayer, M., Paul, O., and Baltes, H., "Complete Set of Piezoresistive Coefficients of CMOS n Plus-diffusion," <u>Journal of Micromechanics and Microengineering</u>, Vol. 8(2), pp. 158-160, 1998.

97. Natarajan, B., and Bhattacharyya, B., "Die Surface Stresses in a Molded Plastic Package," <u>Proceedings of the 36th Electronic Components Conference</u>, IEEE, pp. 544-551, 1986.

98. Bjorneklett, A., Tuhus, T., Halbo, L., and Kristiansen, H., "Thermal Resistance, Thermomechanical Stress and Thermal Cycling Endurance of Silicon Chips Bonded with Adhesives," <u>Proceedings of the Ninth Annual IEEE Semiconductor Thermal Measurement and Management Symposium</u>, pp. 136-143, Austin, TX, 1993.

99. Ducos, C. S., Christophe, E., Fremont, H., Kaoua, G., Pellet, C., and Danto, Y., "Evaluation of Stresses in Packaged ICs by In Situ Measurements with an Assembly Test Chip and Simulation," <u>Microelectronics and Reliability</u>, Vol. 37(10-11), pp. 1795-1798, 1997.

100. Thomas, C. E., Bright, W. T., and Kenyon, E. A., "Stress Comparison of TBGA, MBGA, and ViperBGA Using the PAQC Chip," <u>Proceedings of MCM '98</u>, IMAPS, pp. 399-404, Denver, CO, April 15-17, 1998.

101. Rahim, M., <u>Measurement of Stress in Electronic Packages using Piezoresistive Sensors</u>, M.S. Thesis, Auburn University, Auburn, AL, 2004.

102. Peterson, D. W., Sweet, J. N., Burchett, S. N., and Hsia, A., "Stresses from Flip-Chip Assembly and Underfill: Measurements with the ATC4.1 Assembly Test Chip and Analysis by Finite Element Method," <u>Proceedings of 47th Electronic Components and Technology Conference</u>, pp. 134-143, 1997.

103. Zou, Y., Lin, S. T., Suhling, J. C., Jaeger, R. C., Benoit, J. T., and Grzybowski, R. R., "Die Surface Stress Variation During Thermal Cycling and Thermal Aging

Reliability Tests," <u>Proceedings of the 49th Electronic Components and Technology Conference</u>, pp. 1249-1260, San Diego, CA, June 1-4, 1999.

104. Jaeger, R. C., Suhling, J. C., and Ramani, R., "Errors Associated with the Design and Calibration of Piezoresistive Stress Sensors in (100) Silicon," <u>Proceedings of the ASME/JSME Joint Conference on Electronic Packaging</u>, ASME, EEP-Vol. 1-1, pp. 447-456, Milpitas, CA, April 9-12, 1992.

105. Jaeger, R. C., Suhling, J. C., and Ramani, R., "Errors Associated with the Design, Calibration of Piezoresistive Stress Sensors in (100) Silicon," <u>IEEE Transactions on Components, Packaging, and Manufacturing Technology - Part B: Advanced Packaging</u>, Vol. 17(1), pp. 97-107, 1994.

106. Pendse, R. D., "A Comprehensive Approach for the Analysis of Package Induced Stress in IC's Using Analytical and Empirical Methods," <u>IEEE Transactions on Components, Hybrids, and Manufacturing Technology</u>, Vol. 14(4), pp. 870-873, 1991.

107. Kelly, G., Lyden, C., Mathuna, C. O., and Campbell, J. S., "Investigation of Thermo-Mechanically Induced Stress in a PQFP 160 Using Finite Element Techniques," <u>Proceedings of 42nd Electronic Components and Technology Conference</u>, IEEE, pp. 467-472, San Diego, CA, 1992.

108. Kelly, G., Lyden, C., Mathuna, C. O., Slattery, O., and Hayes, T., "Correlation Of Shear Stress And Metal Shift: A Modeling Approach," <u>Proceedings of 43rd Electronic Components and Technology Conference</u>, IEEE, pp. 264-269, 1993.

109. Sweet, J. N., Burchett, S. N., Peterson, D. W., Hsia, A. H., and Chen, A., "Piezoresistive Measurement and FEM Analysis of Mechanical Stresses in 160L Plastic Quad Flat Packs," <u>Proceedings of InterPACK '97</u>, pp. 1731-1740, Kohala, HI, June 15-19, 1997.

110. Sweet, J. N., Peterson, D. W., Emerson, J. A., and Burchett, S. N., "Experimental Measurements and Finite Element Calculation for Liquid Encapsulated ATC04 Assembly Test Chips," <u>Applications of Experimental Mechanics to Electronic Packaging</u>, ASME, EEP-Vol. 13, pp. 79-94, 1995.

111. Skipor, A F., Baird, J., Jeffery, D., Ommen, D., and Westlake, M., "Experimental Validation and Finite Element Simulation of a 64 Lead TQFP and a 68 Lead PLCC," <u>Sensors in Electronic Packaging</u>, ASME, MED-Vol. 3, pp. 1-9, San Francisco, CA, 1995.

112. Slattery, O., Hayes, T., Lawton, W., Kelly, G., Lyden, C., Barrett, J., and O'Mathuna, C., "Methods of Analysing Thermomechanical Stress in Plastic Packages for Integrated Circuits," <u>Journal of Materials Processing Technology</u>, Vol. 54(1-4), pp. 199-204, 1995.

113. Chen, L., Zhang, Q., Wang, G., Xie, X., Cheng, Z., "The Effects of Underfill and its Material Models on Thermomechanical Behaviors of a Flip Chip Package," <u>IEEE Transactions on Advanced Packaging</u>, Vol. 24(1), pp. 17-24, 2001.

114. Chen, Y., <u>CMOS Stress Sensor Circuits</u>, Ph.D. Dissertation, Auburn University, Auburn, AL, 2006.

115. Ueta, N., and Miura, H., "Dominant Structural Factors of Local Residual Stress in Three Dimensional Stacked LSI Chips Mounted Using Flip Chip Technology," <u>Proceedings of InterPACK '07</u>, Paper IPACK2007-33402, pp. 1-7, 2007.

116. Rahim, MD. S., <u>Die Stress Characterization And Interface Delamination Study In Flip Chip On Laminate Assemblies</u>, Ph.D. Dissertation, Auburn University, Auburn, AL, 2005.

117. Schubert, A., Walter, H., Dudek, R., Michel, B., Lefranc, G., Otto, J. and Mitic, G., "Thermomechanical Properties and Creep Deformation of Lead-containing and Lead-free Solders", Proceedings, <u>International Symposium on Advanced Packaging Materials</u>, pp. 129-134, 2001.

118. Garofalo, F., <u>Fundamentals of Creep and Creep-Rupture in Metals</u>, The Macmillan Company, 1966.

APPENDIX A

CALIBRATION RESULTS: FOUR POINT BENDING

P -TYPE SENSORS

Sample	$B_1^{\,p}$ (1/Tpa)	$B_2^{\,p}$ (1/Tpa)	$B_1^{\,p} - B_2^{\,p}$ (1/Tpa)
W1S1P1	376.8	-92.8	469.6
W1S1P2	368.8	-95.5	464.3
W1S1P3	354.1	-88.7	442.8
W1S1P4	349.1	-91.8	440.9
W1S1P5	348.3	-93.6	441.9
W1S2P6	373.8	-88.5	462.3
W1S2P7	363.1	-98.5	461.6
W1S2P8	374.9	-80.8	455.7
W1S3P9	375.0	-90.8	465.8
W1S3P10	377.0	-107.6	484.6
W2S1P1	373.1	-84.0	457.1
W2S1P2	366.4	-89.4	455.8
W2S1P3	376.3	-96.9	473.2
W2S1P4	366.8	-99.7	466.5
W2S2P5	382.3	-89.5	471.8
W2S2P6	364.8	-85.4	450.2
W2S2P7	364.1	-93.6	457.7
W2S2P8	361.5	-81.1	442.6
W2S2P9	392.8	-92.5	485.3
W2S2P10	350.4	-88.1	438.5
Average	368.0	-91.4	459.4
St. Dev.	11.6	6.4	13.9

JSE-WB Stress Chip
W1S1P1
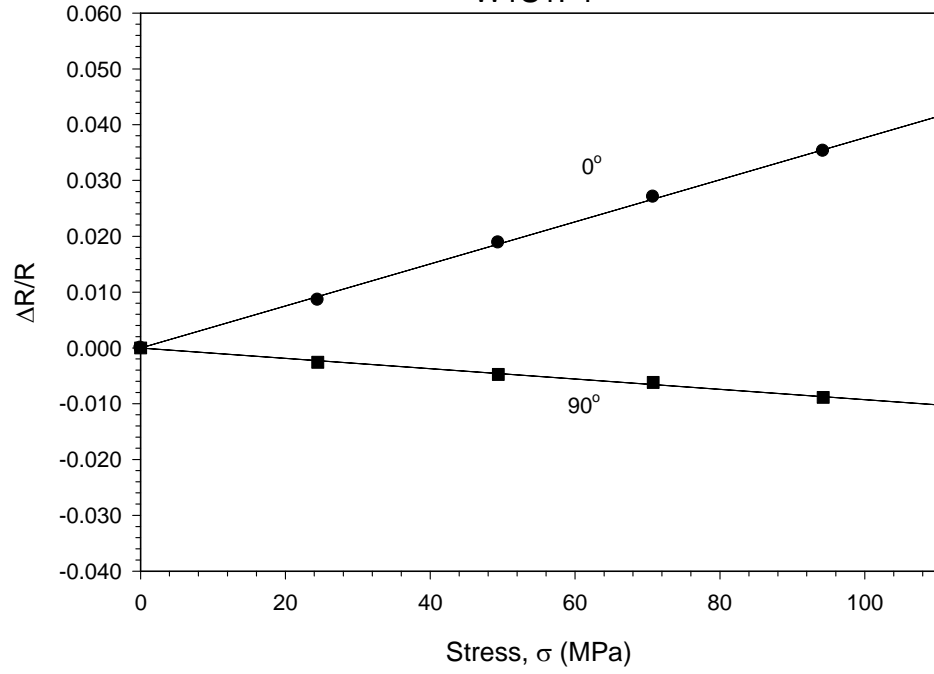
JSE-WB Stress Chip
W1S1P2
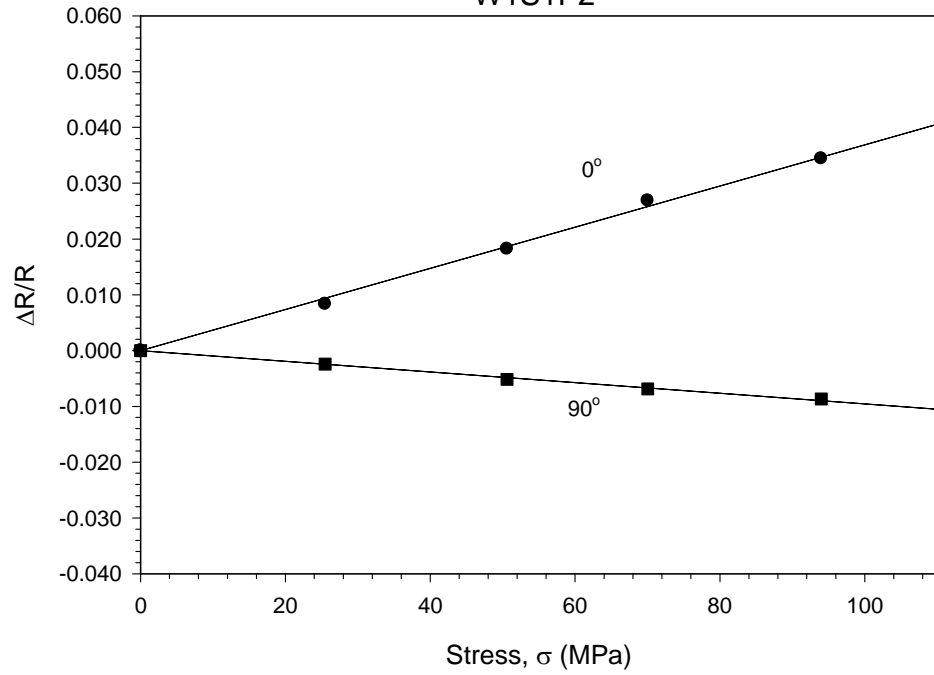
JSE-WB Stress Chip
W1S1P3
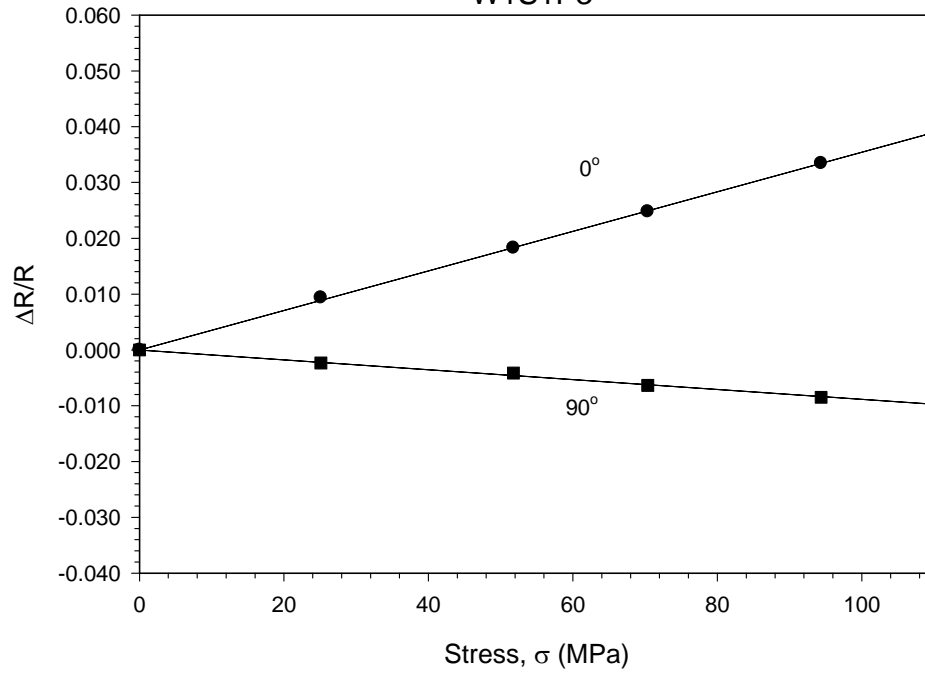
JSE-WB Stress Chip
W1S1P4

148
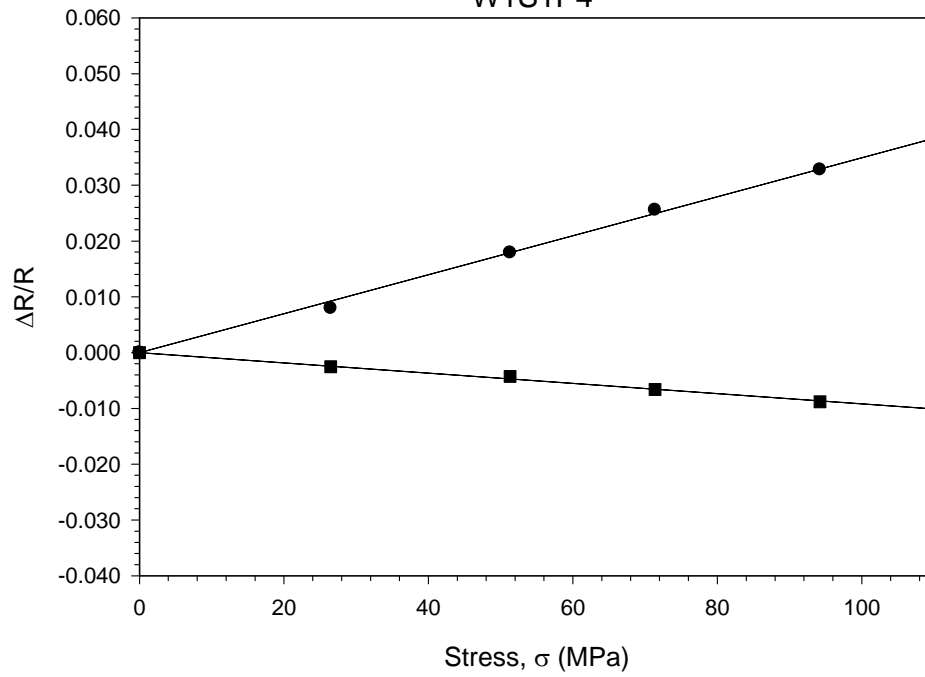
JSE-WB Stress Chip
W1S1P5
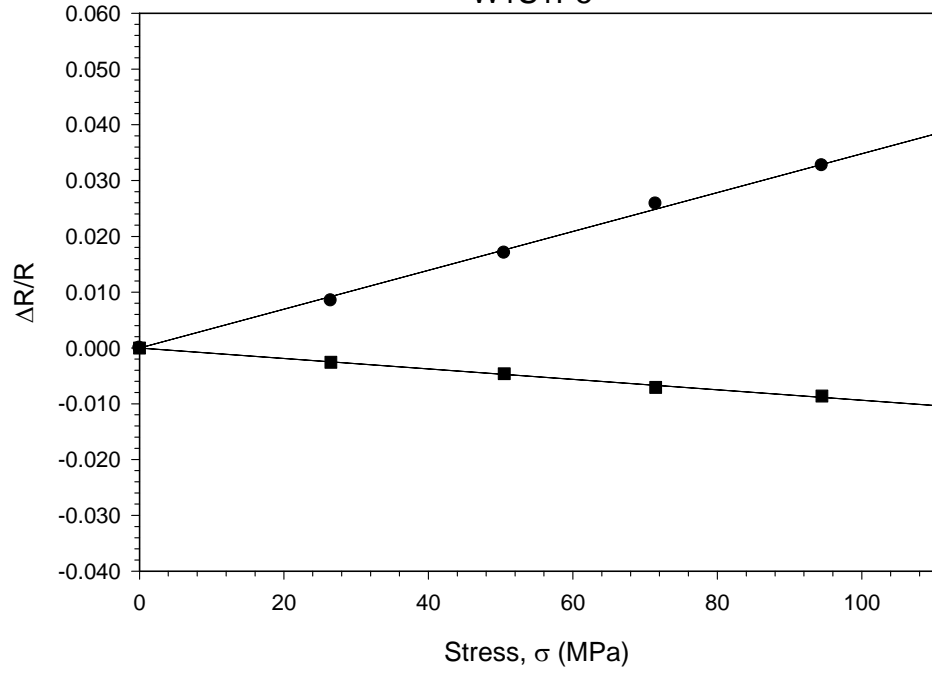
JSE-WB Stress Chip
W1S2P6

149
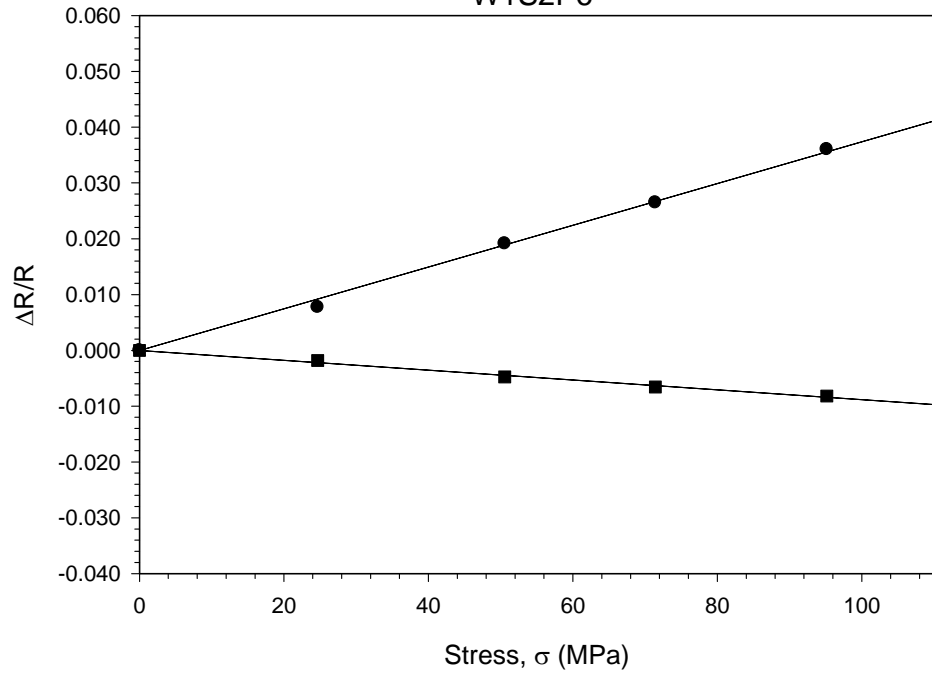
JSE-WB Stress Chip
W1S2P7
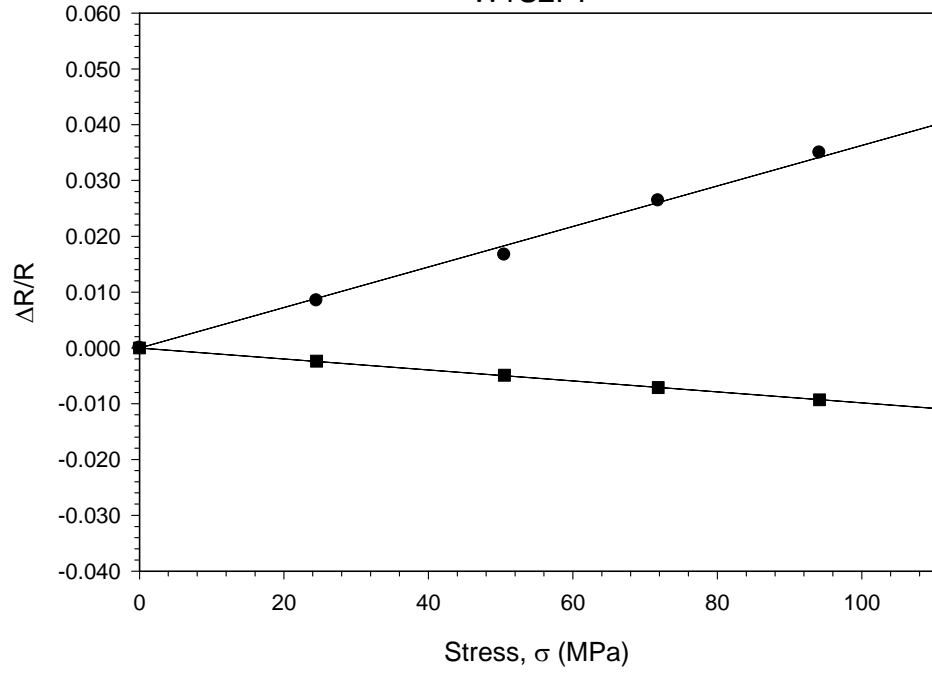
JSE-WB Stress Chip
W1S2P8
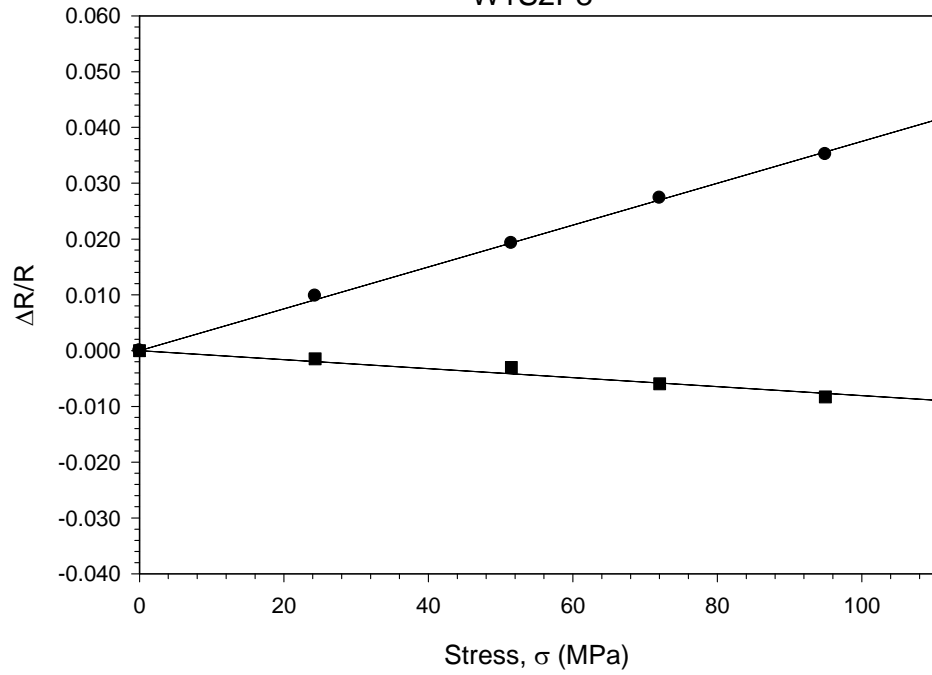
JSE-WB Stress Chip
W1S2P9
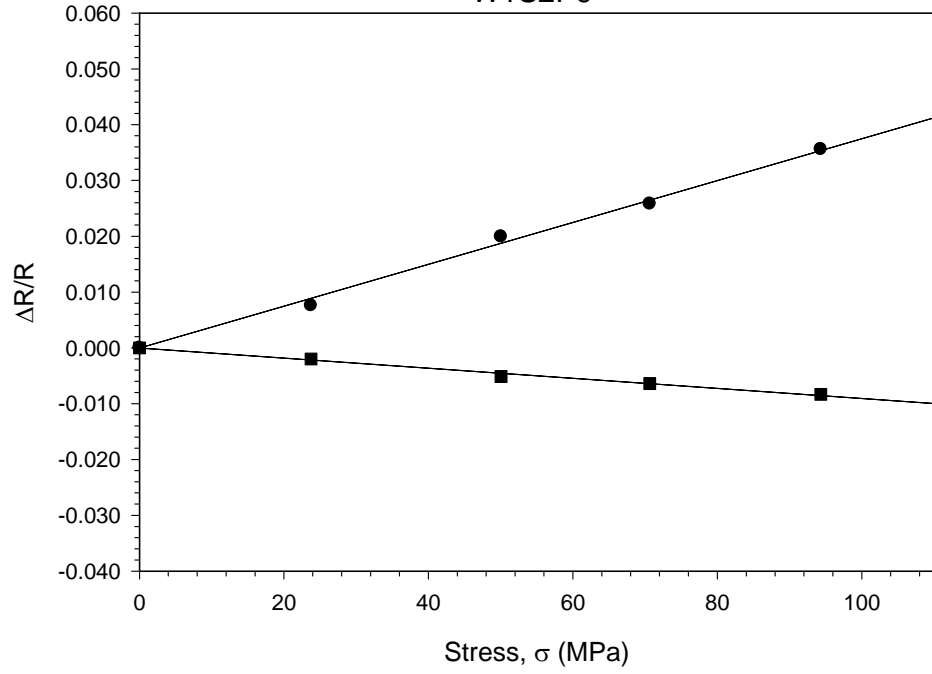
JSE-WB Stress Chip
W1S2P10

151
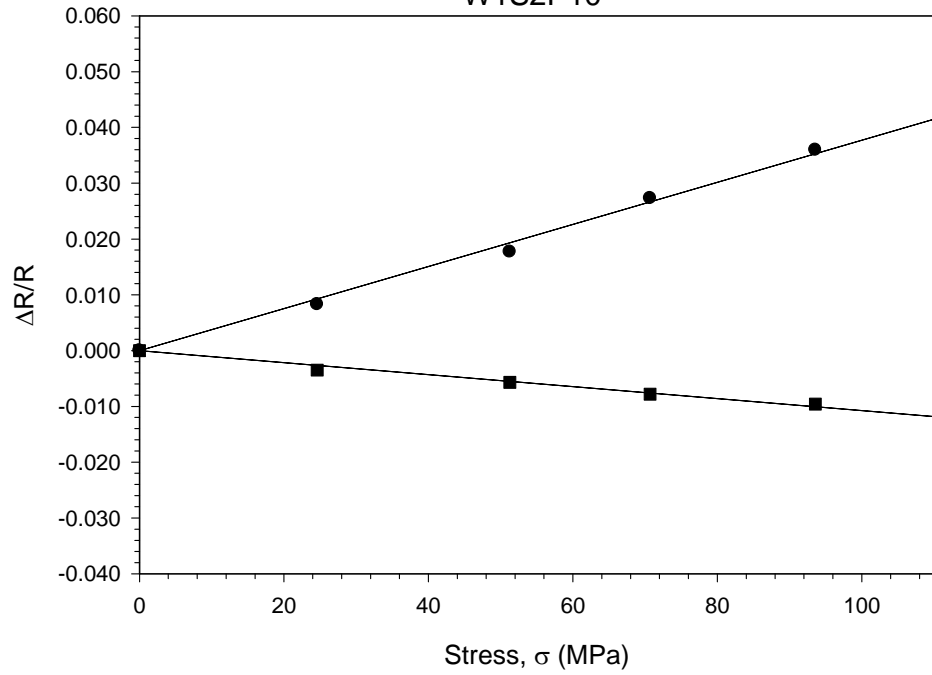
JSE-WB Stress Chip
W2S1P1
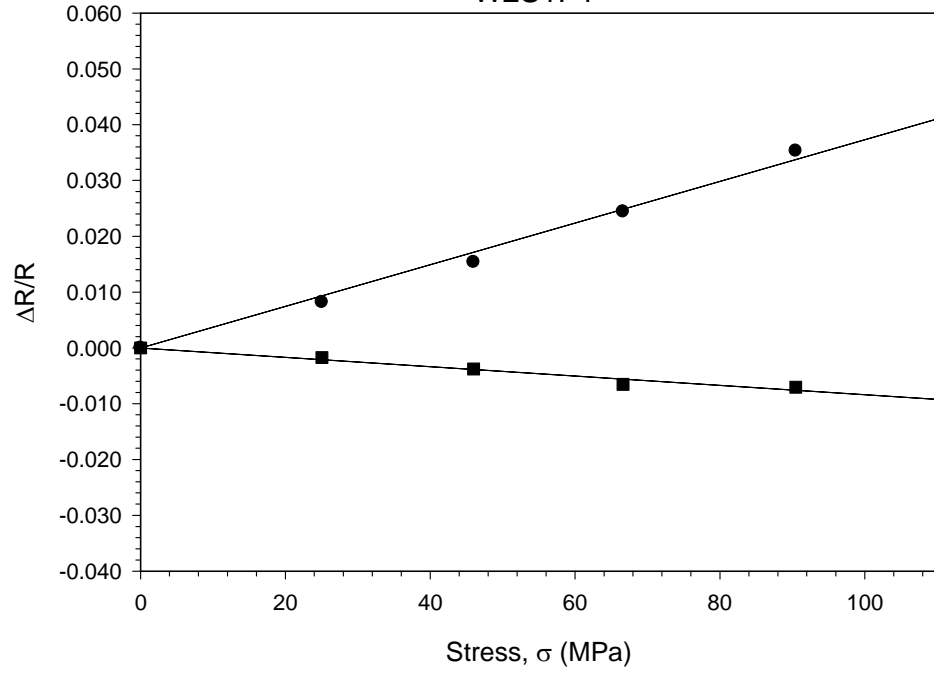
JSE-WB Stress Chip
W2S1P2

152
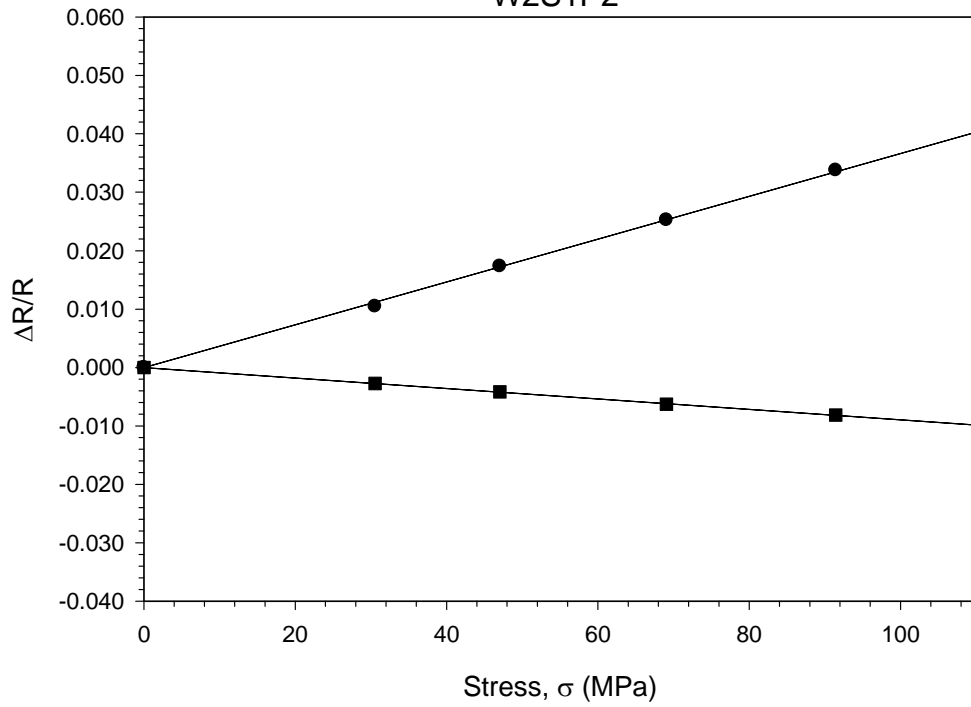
JSE-WB Stress Chip
W2S1P3
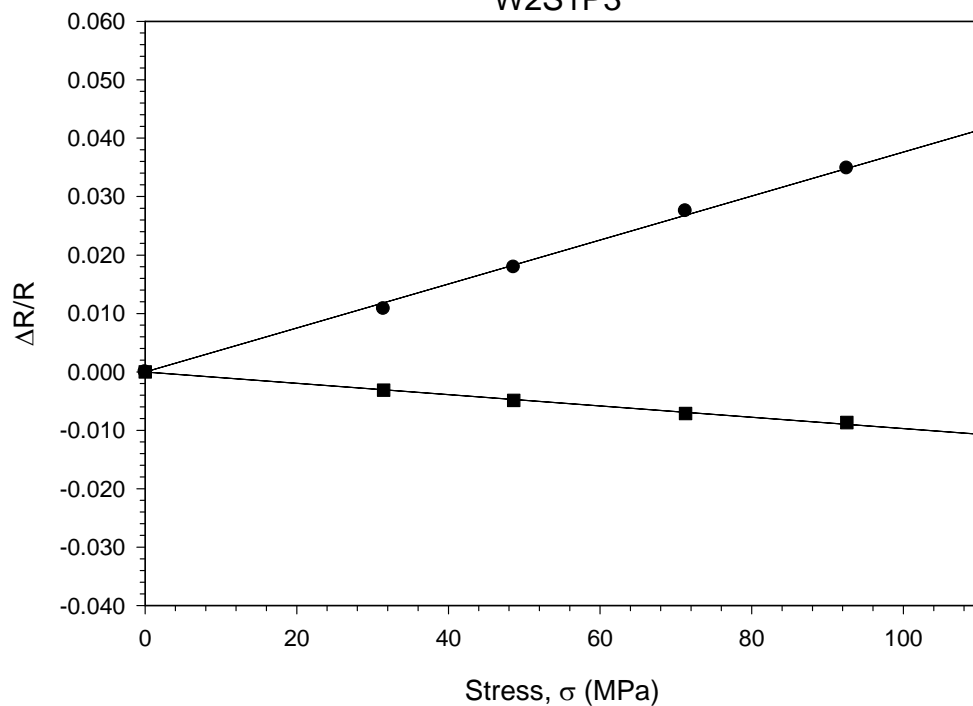
JSE-WB Stress Chip
W2S1P4
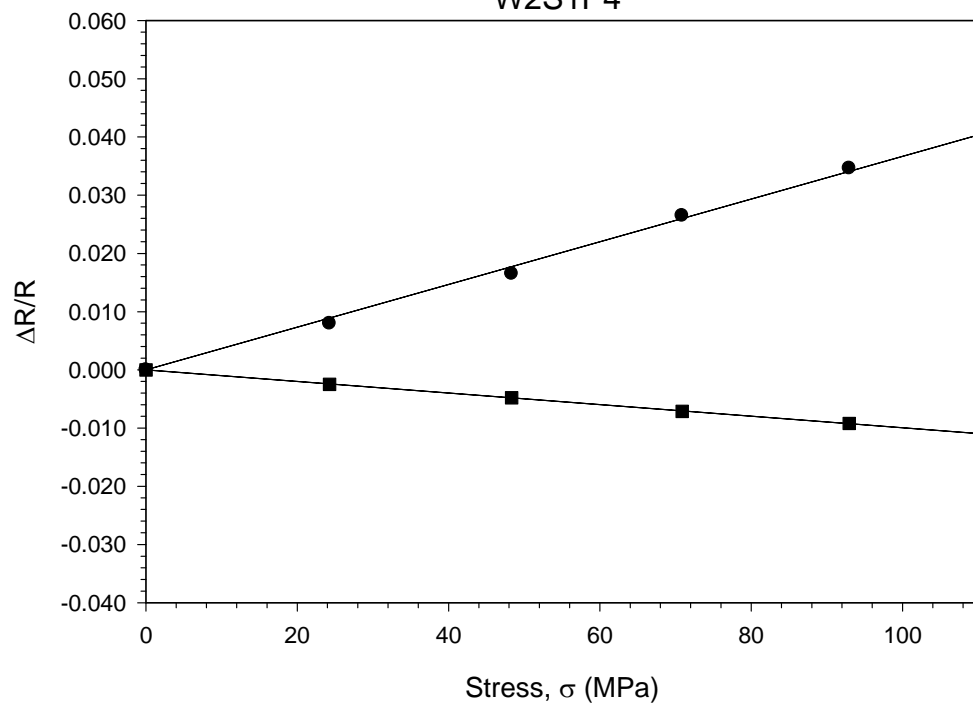
JSE-WB Stress Chip
W2S2P5
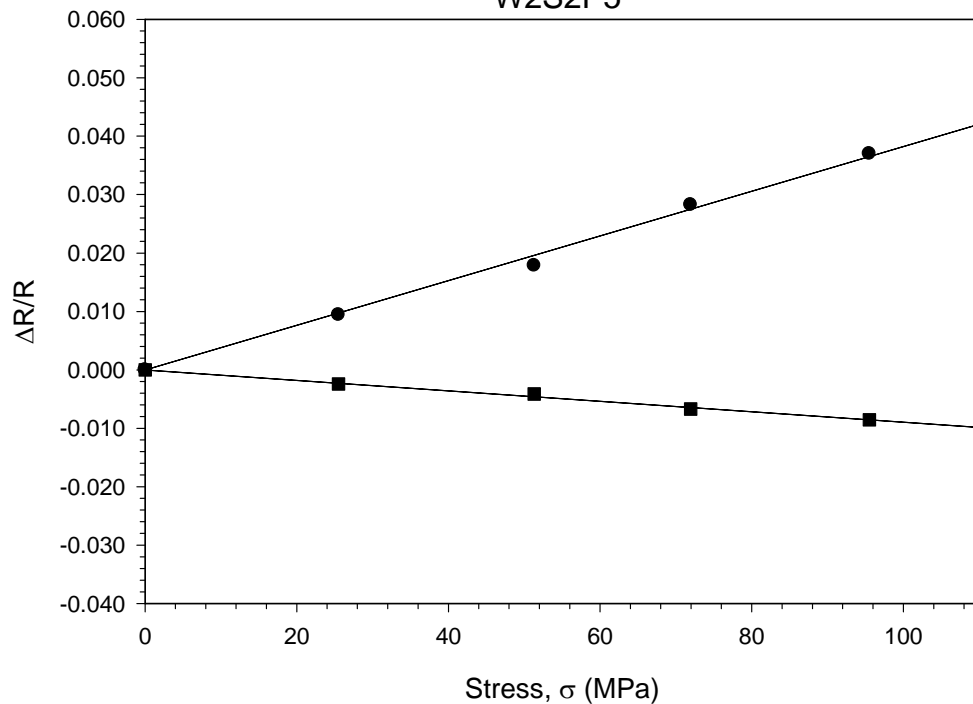
JSE-WB Stress Chip
W2S2P6

154
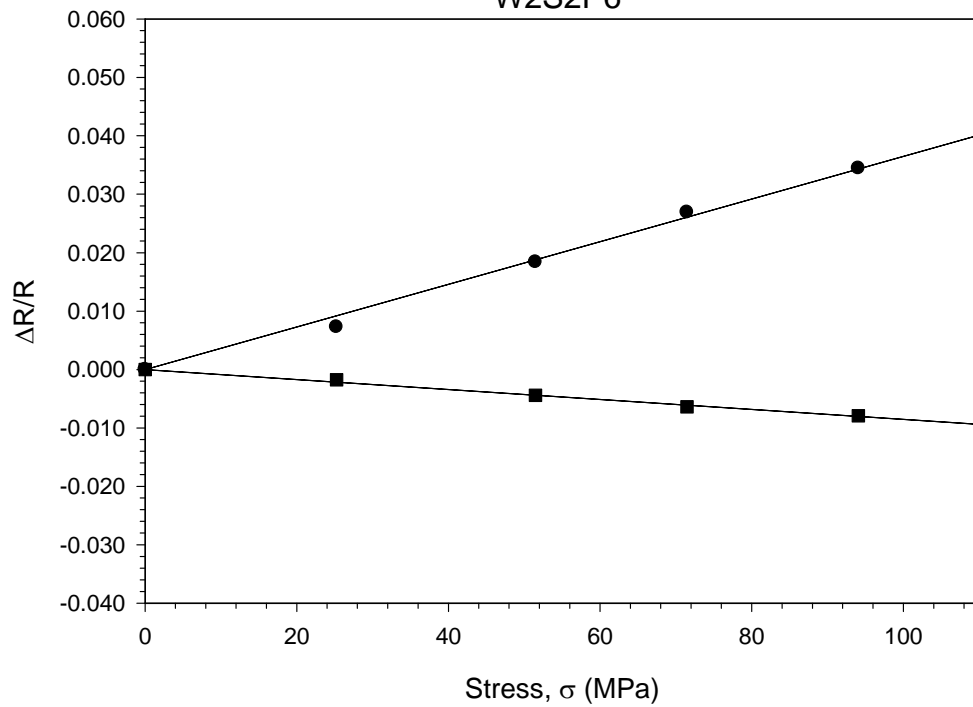
JSE-WB Stress Chip
W2S2P7
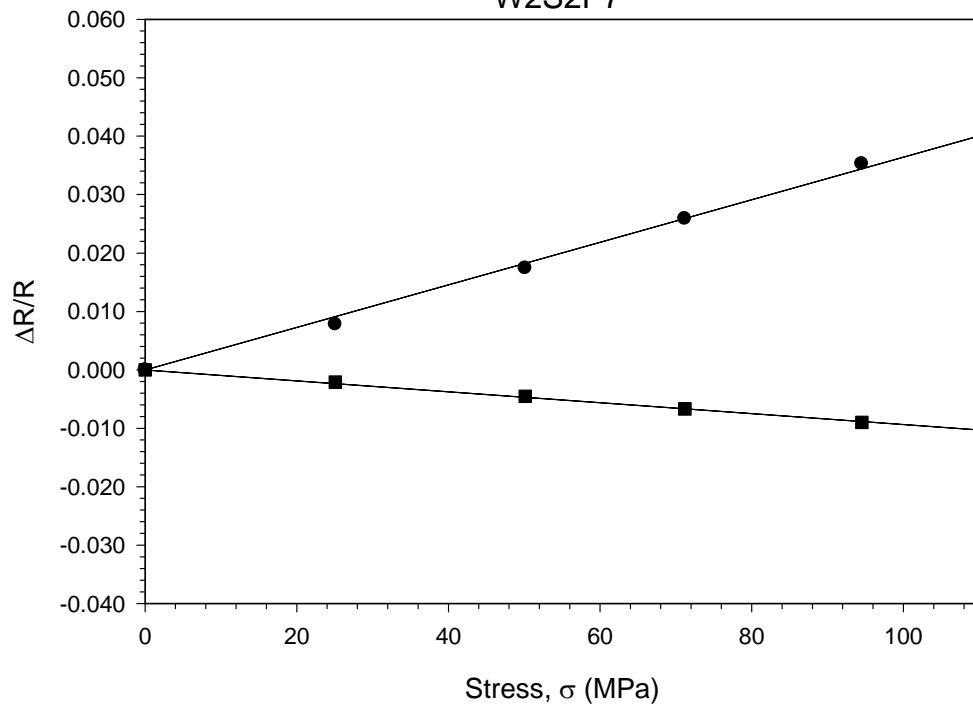
JSE-WB Stress Chip
W2S2P8
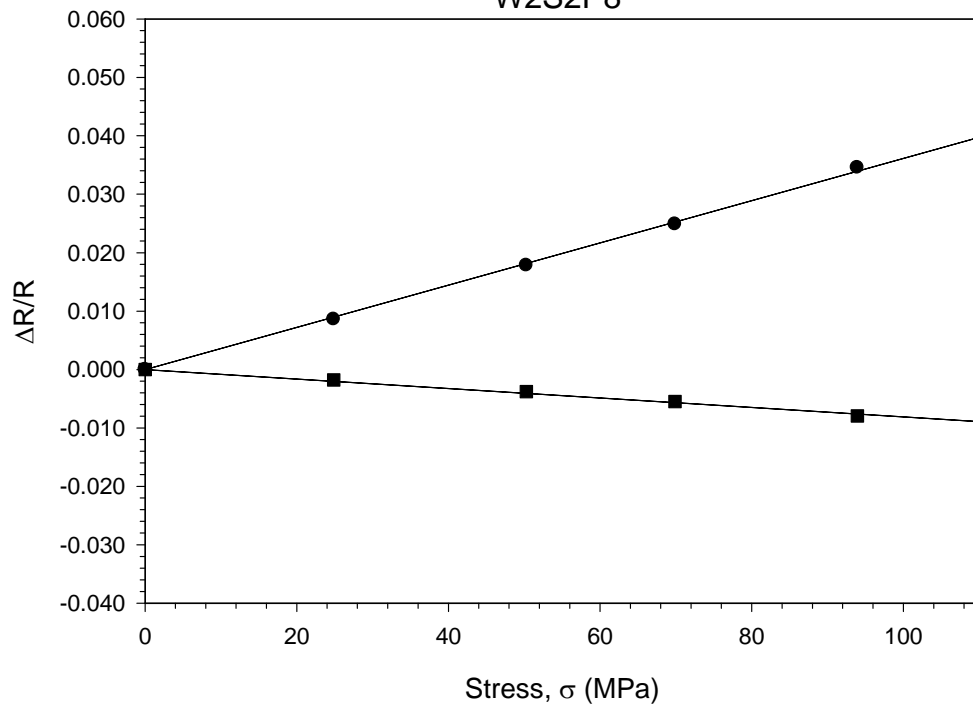
JSE-WB Stress Chip
W2S2P9
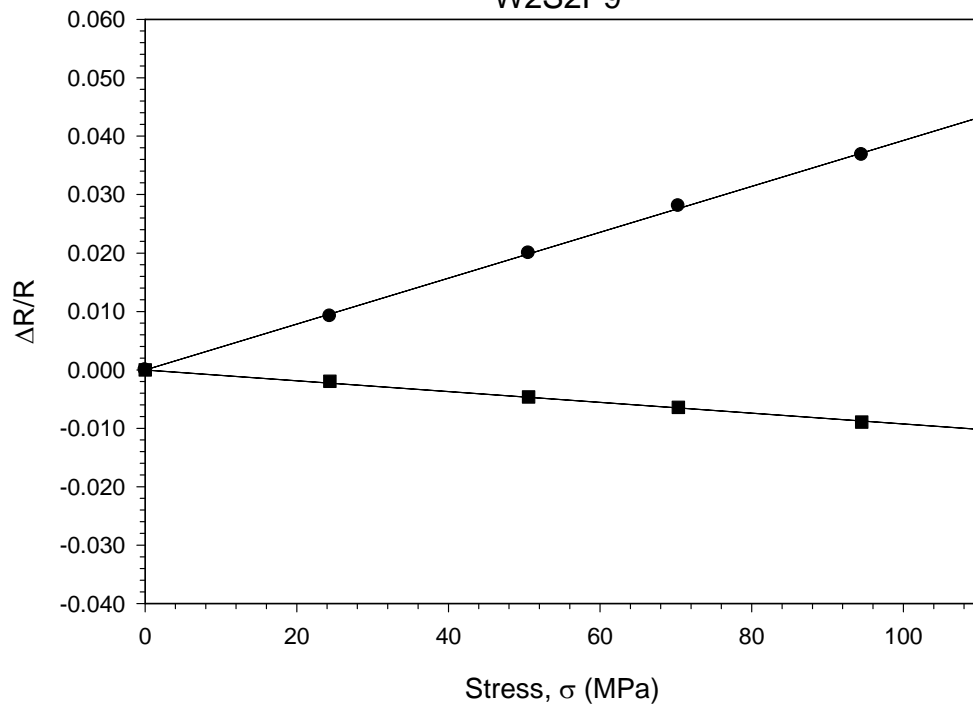
JSE-WB Stress Chip
W2S2P10
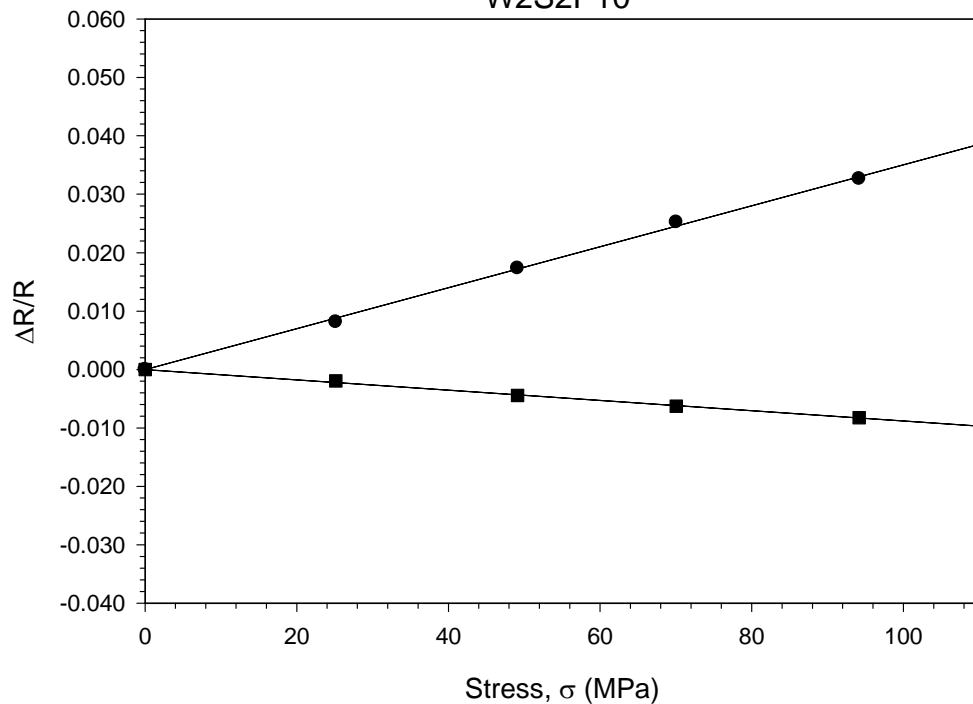
N -TYPE SENSORS

Sample	B_1^n (1/Tpa)	B_2^n (1/Tpa)	$B_1^n - B_2^n$ (1/Tpa)
W1S1N1	-118.4	110.3	-228.7
W1S1N2	-131.8	85.0	-216.8
W1S1N3	-135.2	93.3	-228.5
W1S1N4	-124.9	70.9	-195.8
W1S1N5	-133.4	71.6	-205.0
W1S2N6	-140.5	83.3	-223.8
W1S2N7	-126.1	114.5	-240.6
W1S2N8	-121.5	88.4	-209.8
W1S3N9	-141.1	101.1	-242.2
W1S3N10	-131.2	103.9	-235.1
W2S1N1	-119.9	90.7	-210.6
W2S1N2	-136.3	73.2	-209.5
W2S1N3	-152.7	85.7	-238.4
W2S1N4	-140.7	120.1	-260.8
W2S2N5	-139.7	85.8	-225.5
W2S2N6	-123.6	79.3	-202.9
W2S2N7	-104.8	113.6	-218.4
W2S2N8	-129.5	75.8	-205.3
W2S2N9	-144.9	101.0	-245.9
W2S2N10	-127.4	72.5	-199.9
Average	-131.2	91.0	-222.2
St. Dev	10.9	15.6	17.7

JSE-WB Stress Chip
W1S1N1
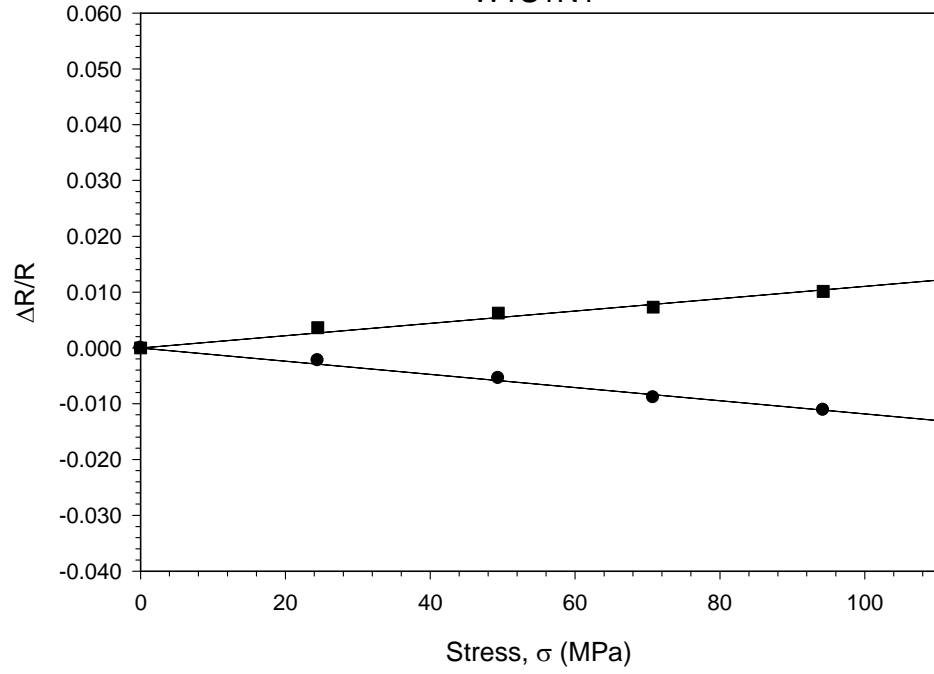
JSE-WB Stress Chip
W1S1N2
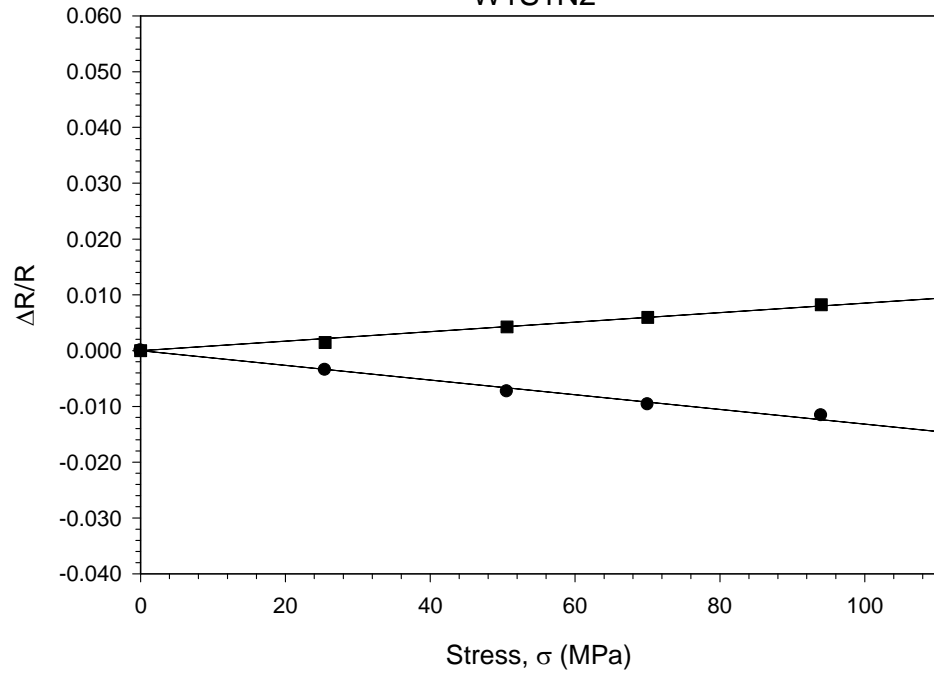
JSE-WB Stress Chip
W1S1N3
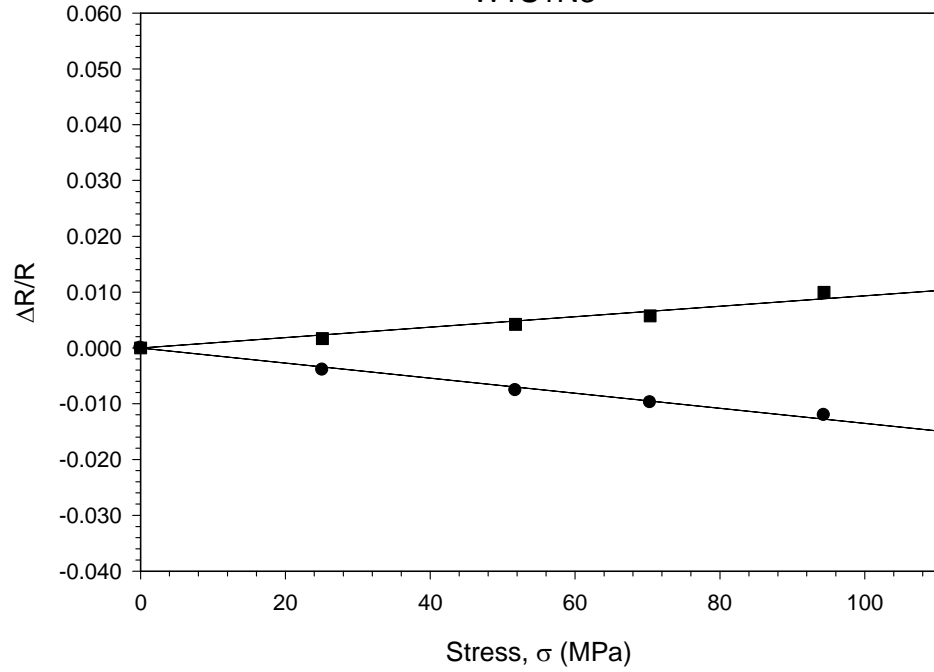
JSE-WB Stress Chip
W1S1N4

159
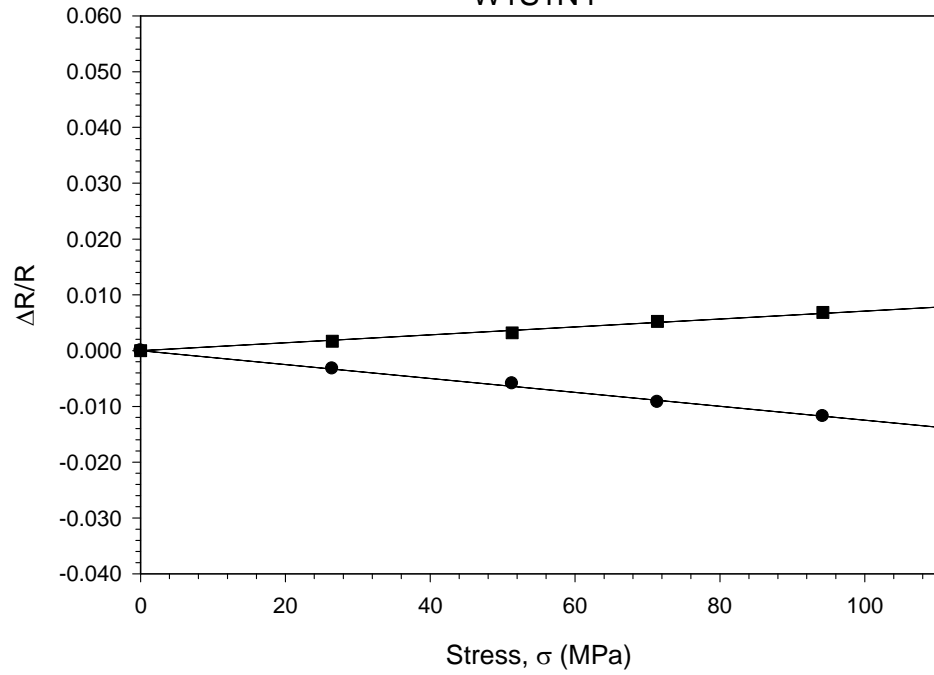
JSE-WB Stress Chip
W1S1N5
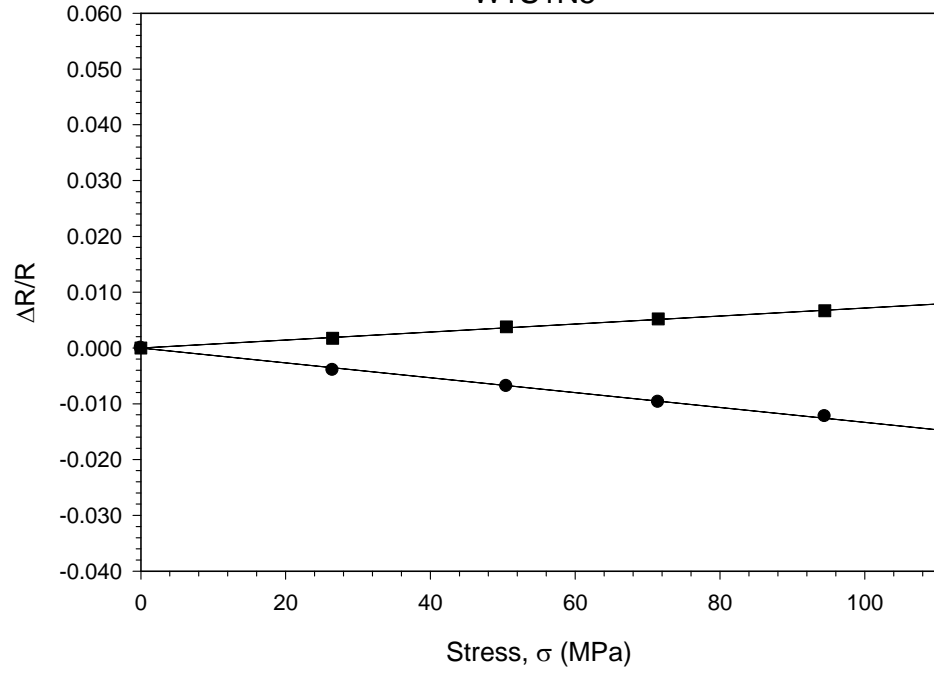
JSE-WB Stress Chip
W1S2N6

160
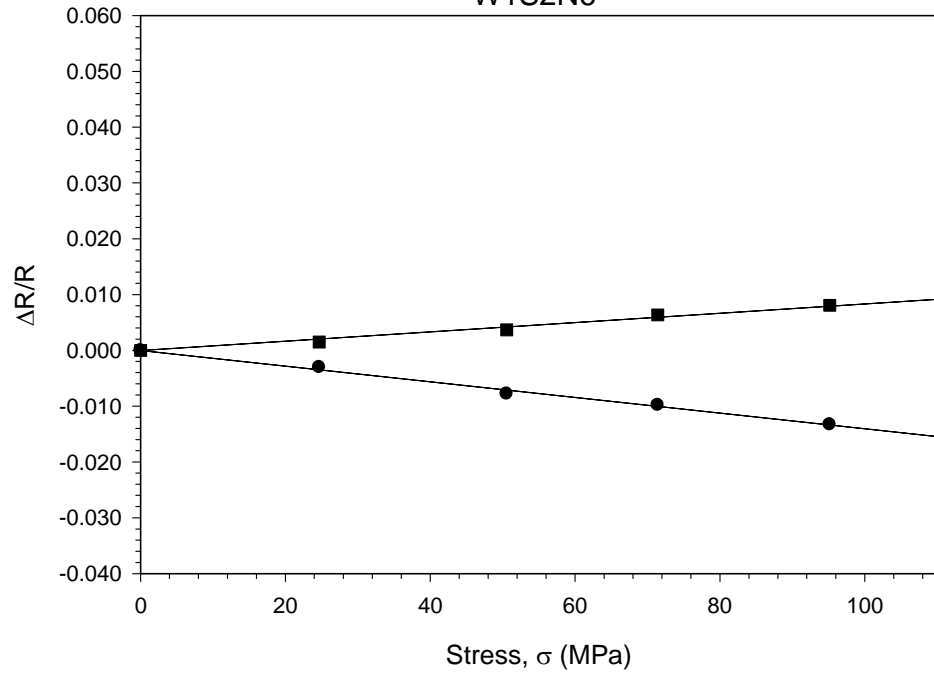
JSE-WB Stress Chip
W1S2N7
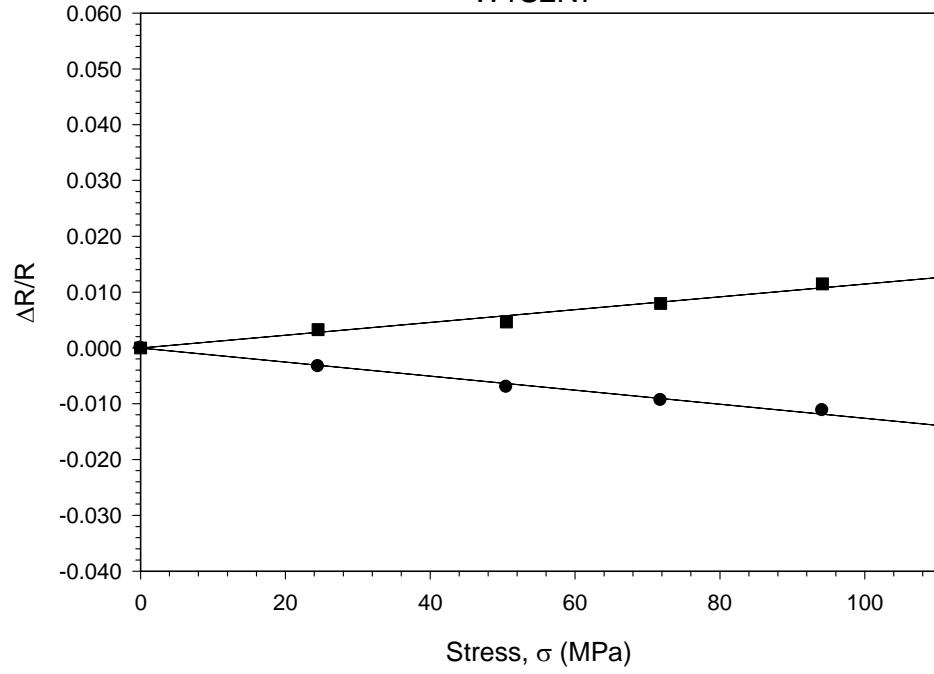
JSE-WB Stress Chip
W1S2N8

161
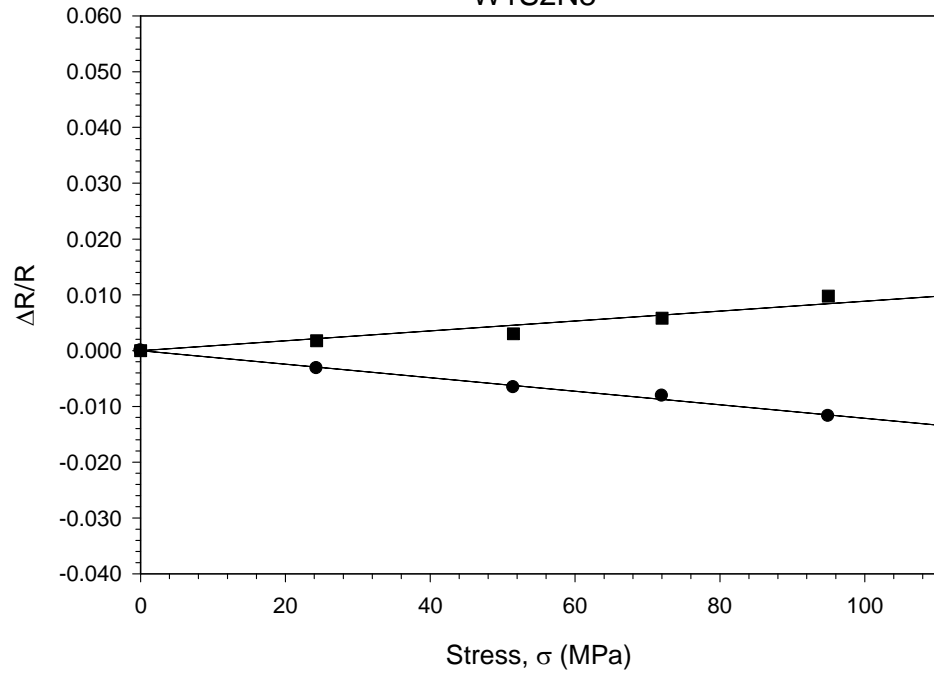
JSE-WB Stress Chip
W1S2N9
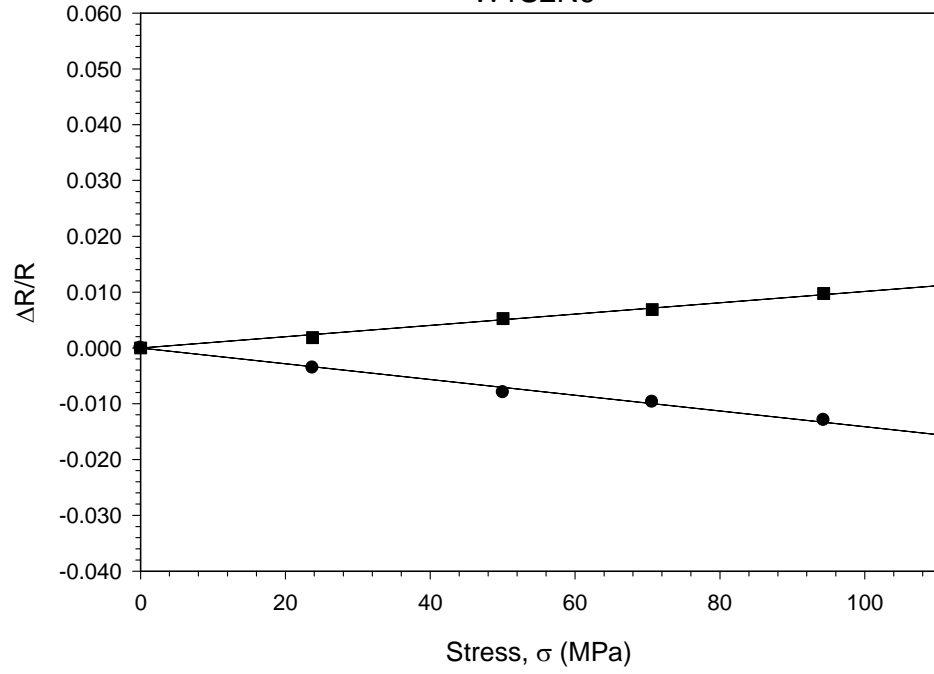
JSE-WB Stress Chip
W1S2N10

162
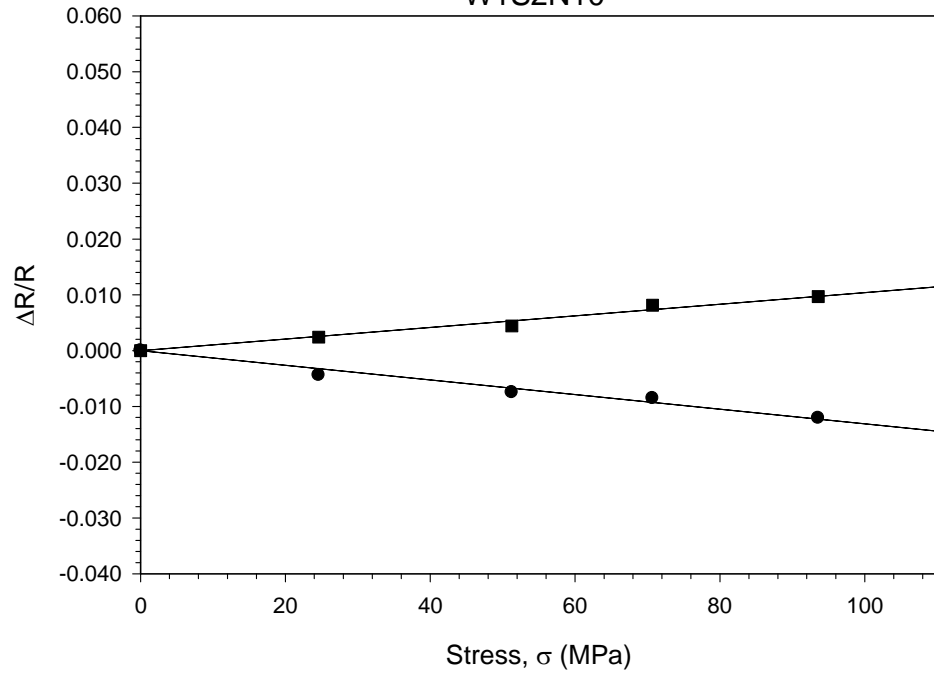
JSE-WB Stress Chip
W2S1N1
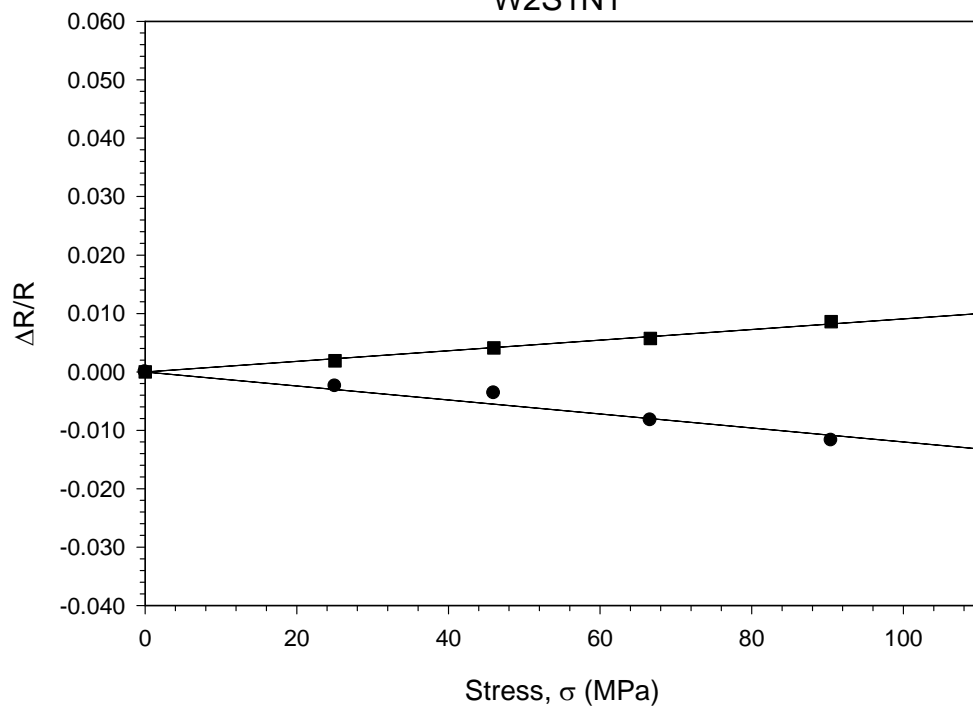
JSE-WB Stress Chip
W2S1N2

163
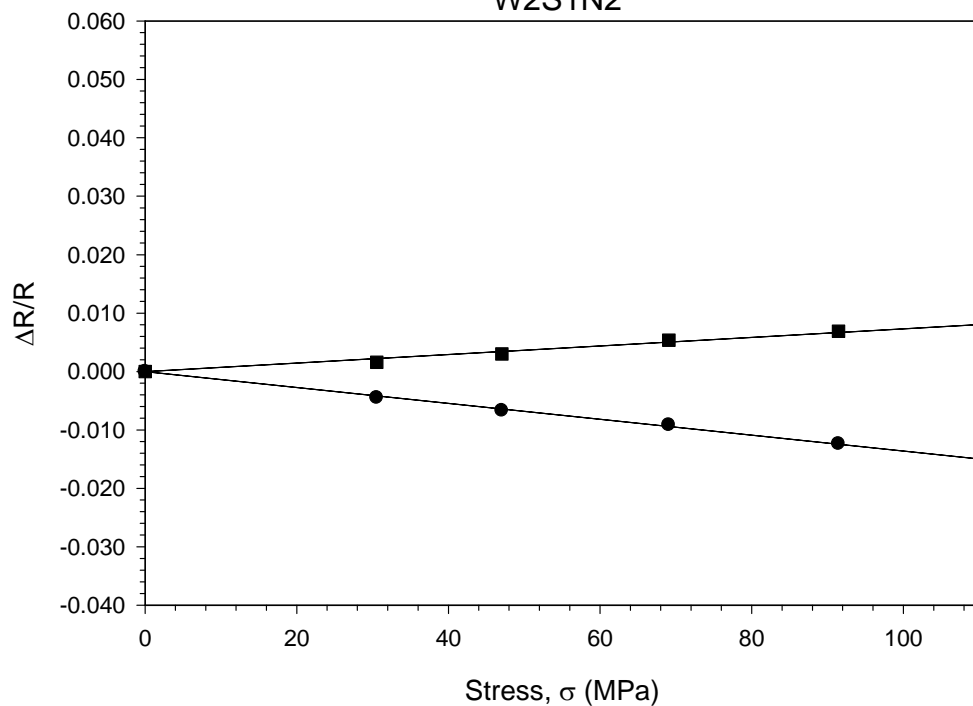
JSE-WB Stress Chip
W2S1N3
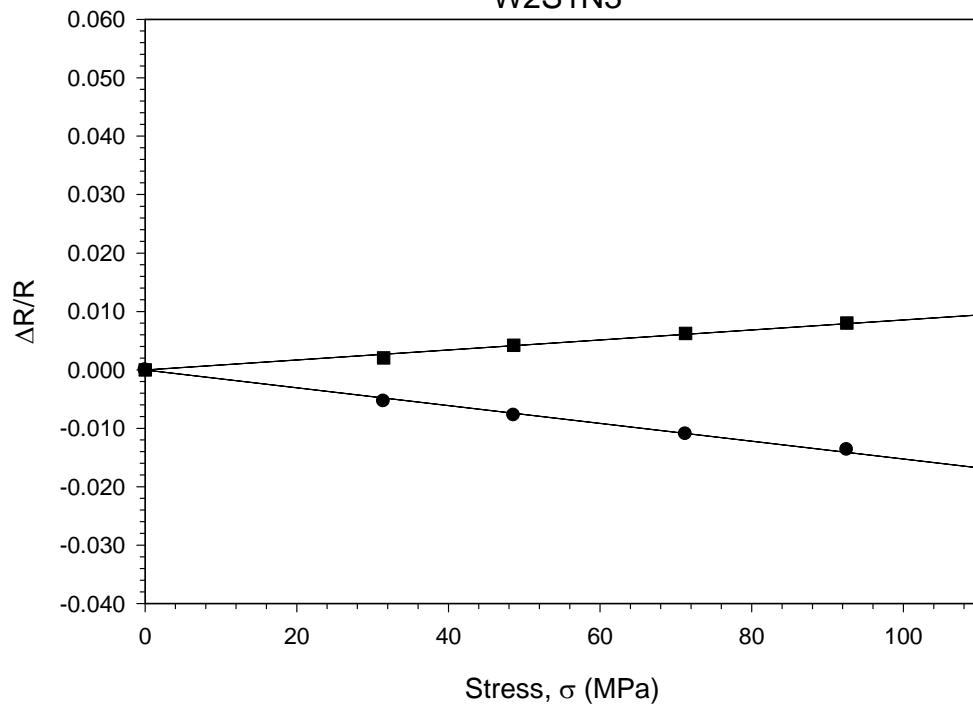
JSE-WB Stress Chip
W2S1N4

164
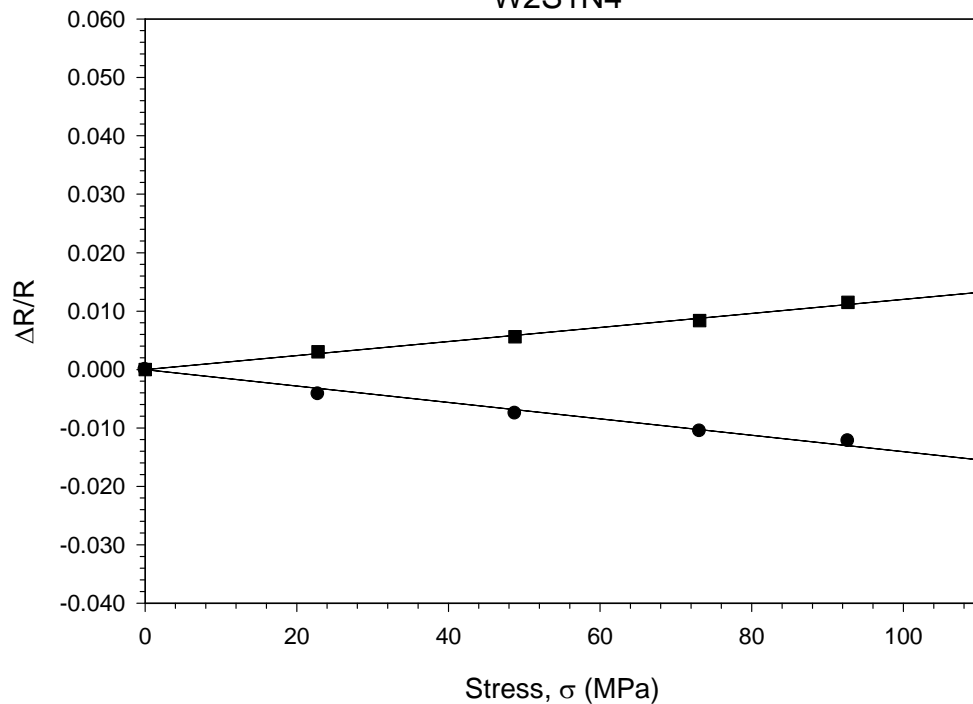
JSE-WB Stress Chip
W2S2N5
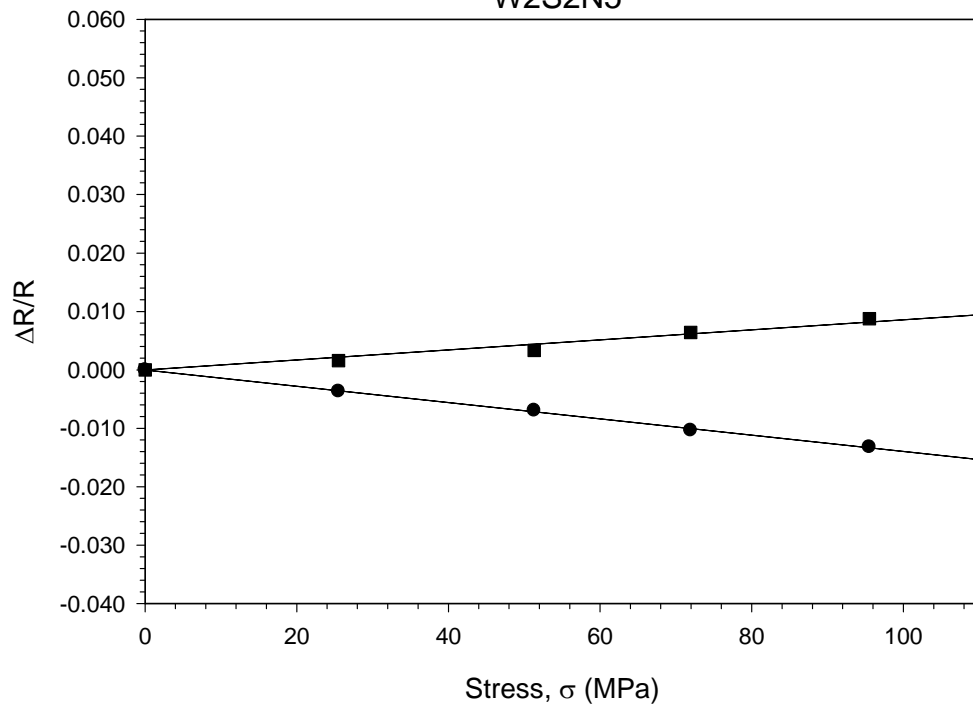
JSE-WB Stress Chip
W2S2N6

165
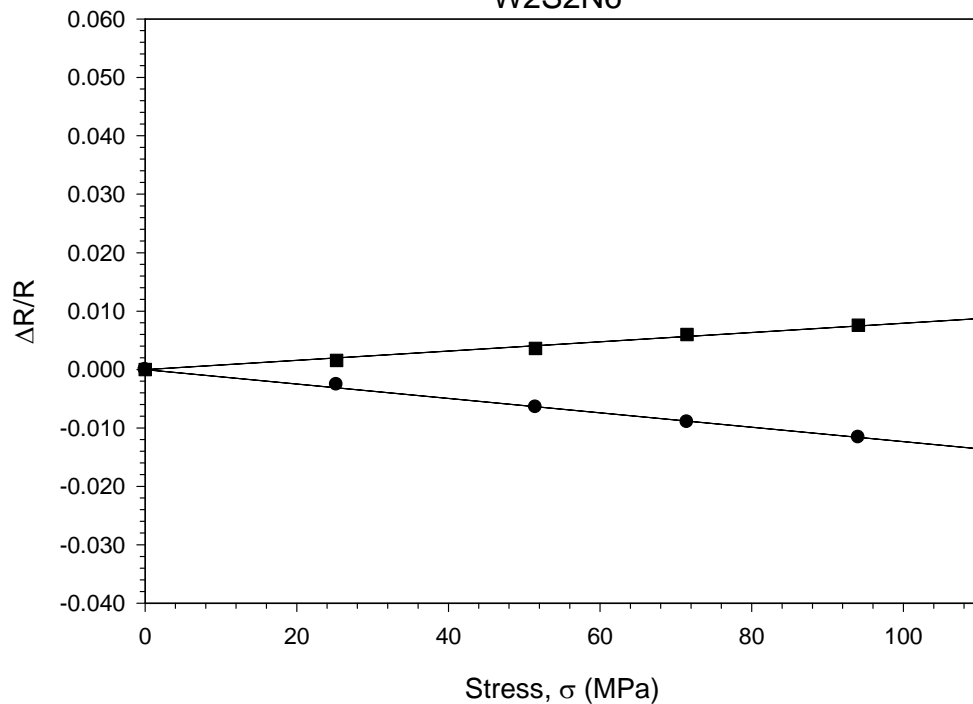
JSE-WB Stress Chip
W2S2N7
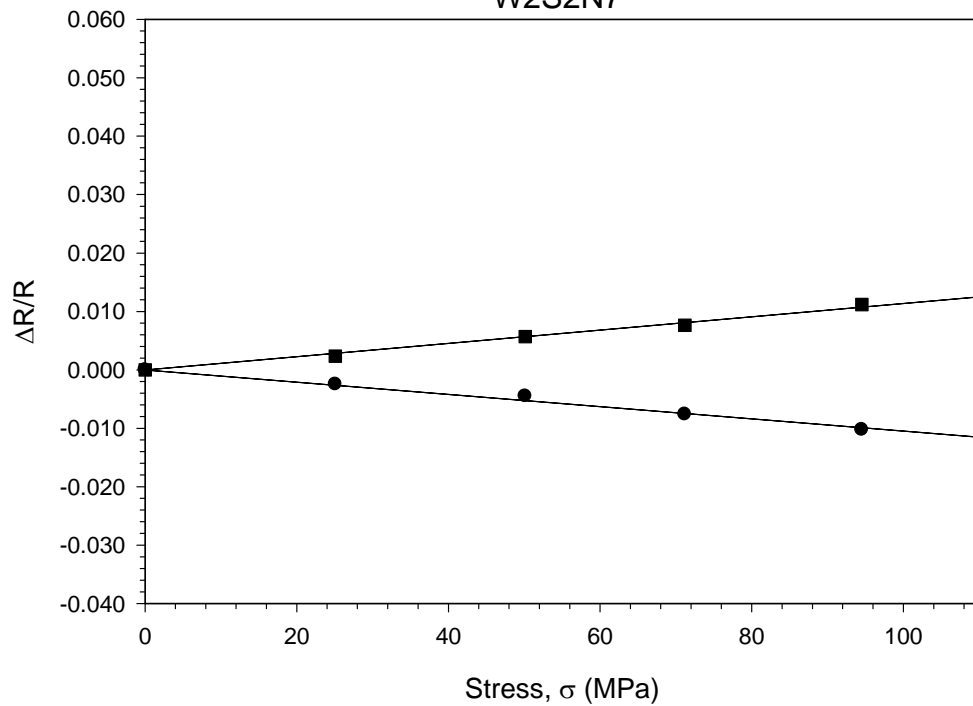
JSE-WB Stress Chip
W2S2N8
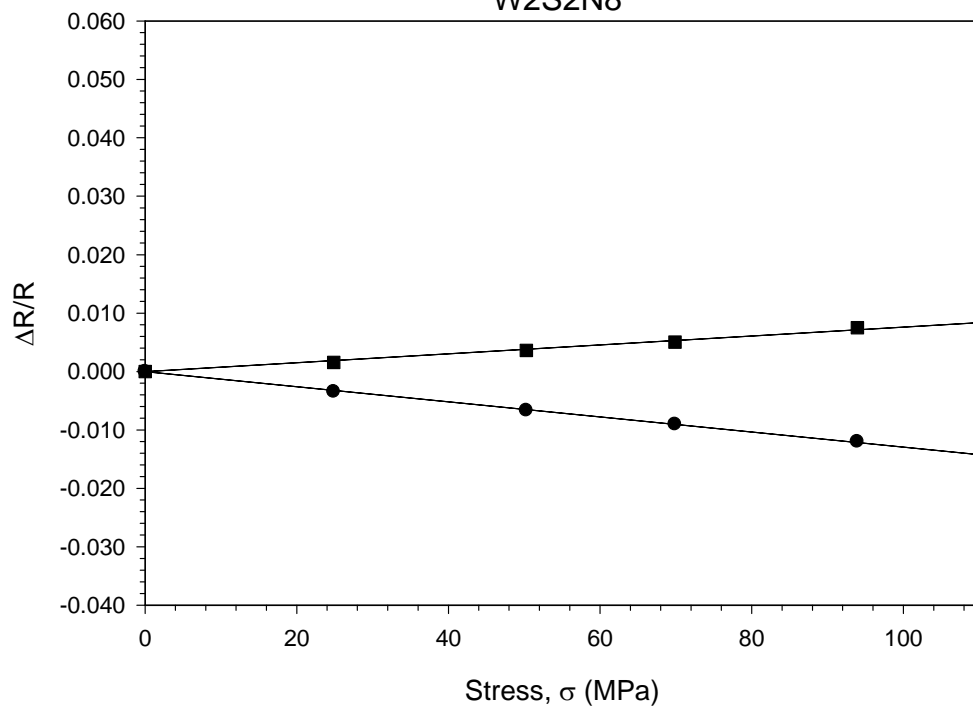
JSE-WB Stress Chip
W2S2N9
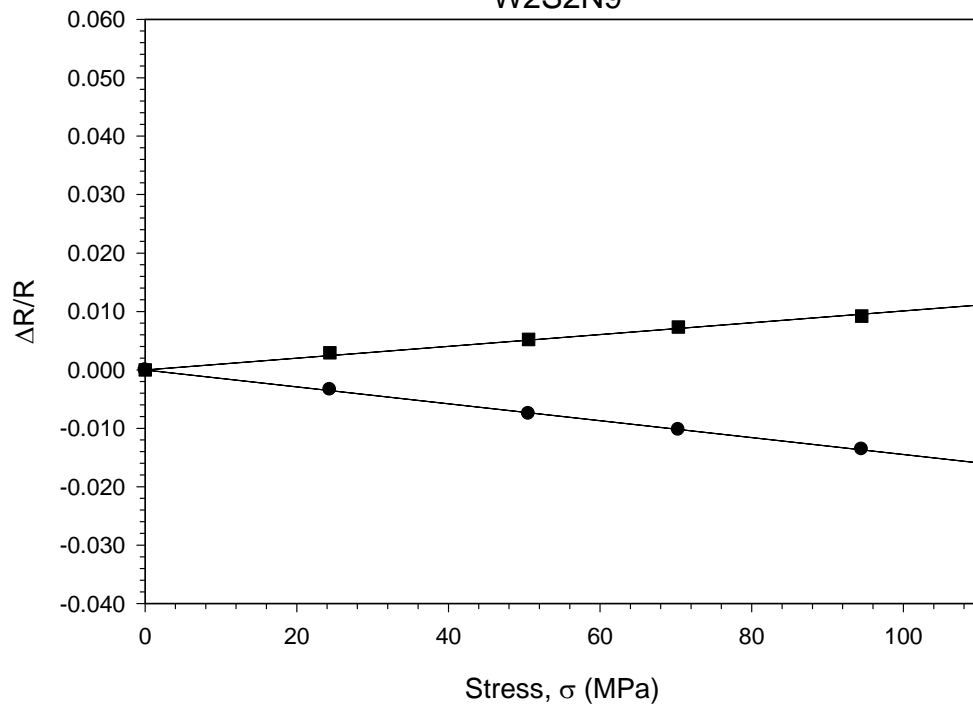
JSE-WB Stress Chip
W2S2N10
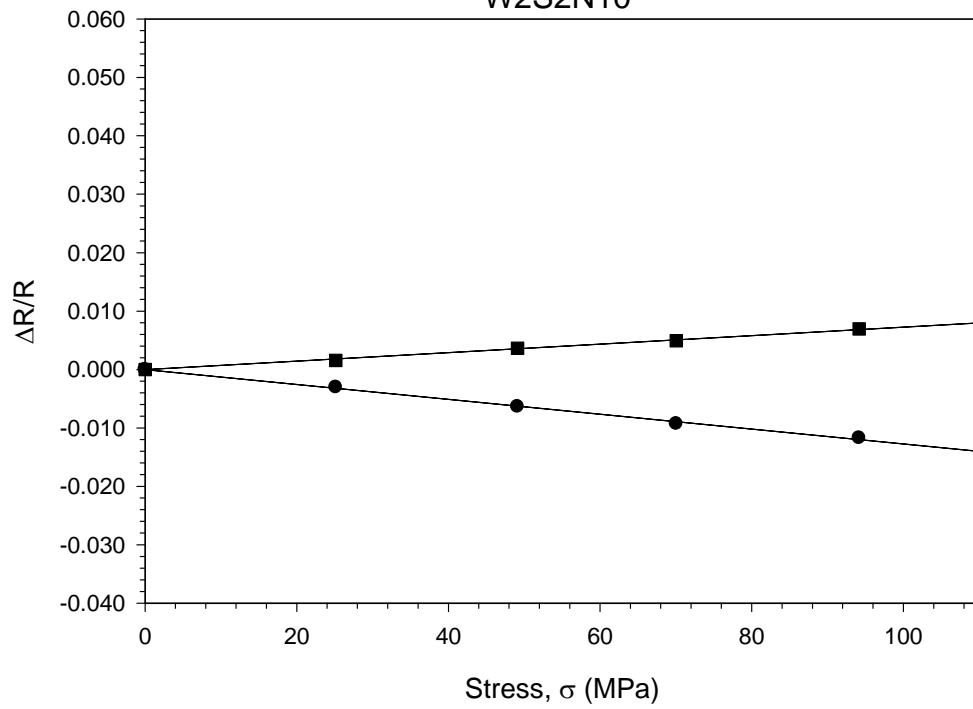
APPENDIX B

CALIBRATION RESULTS: HYDROSTATIC

N-Type Sensors

Sample	π_p(1/TPa)	TCR (x 10-6 1/^{o}C)
B1S1N0	74.8	1537
B1S1N-45	67.3	1548
B1S1N90	71.4	1558
B2S1N-45	70.2	1630
B1S1N0	77.6	1537
B1S1N-45	60.6	1548
B1S1N90	83.9	1558
B2S1N-45	77.5	1630
B6S1N-45	67.1	1647
B6S1N90	108.5	1675
Average	75.9	1586.7
St. Dev.	13.2	52.5

Hydrostatic Calibration Data
Resistance Change and Temperature Variation
N - Type Resistor, Orientation : 0°
Board #1 , Site # 1

Adjusted Resistance Change

Hydrostatic Calibration Data
Resistance Change and Temperature Variation
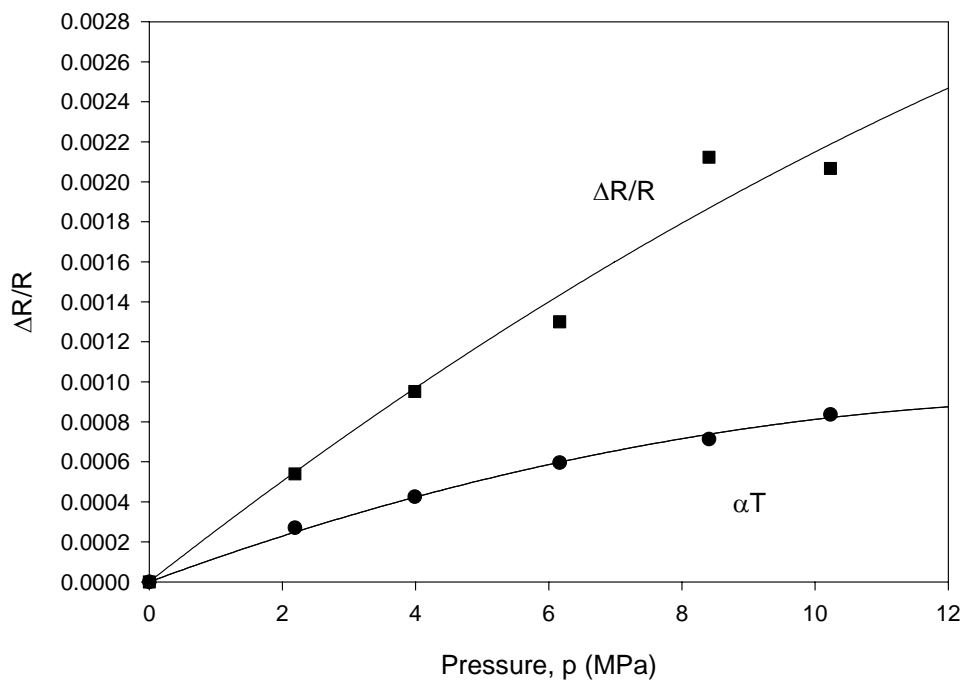## N - Type Resistor, Orientation : 90 [0]
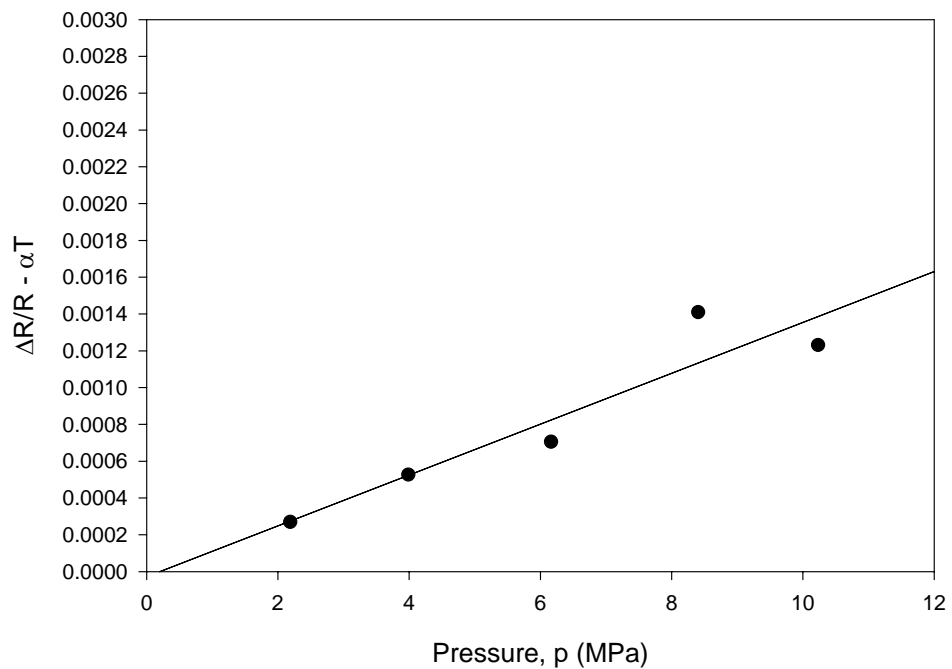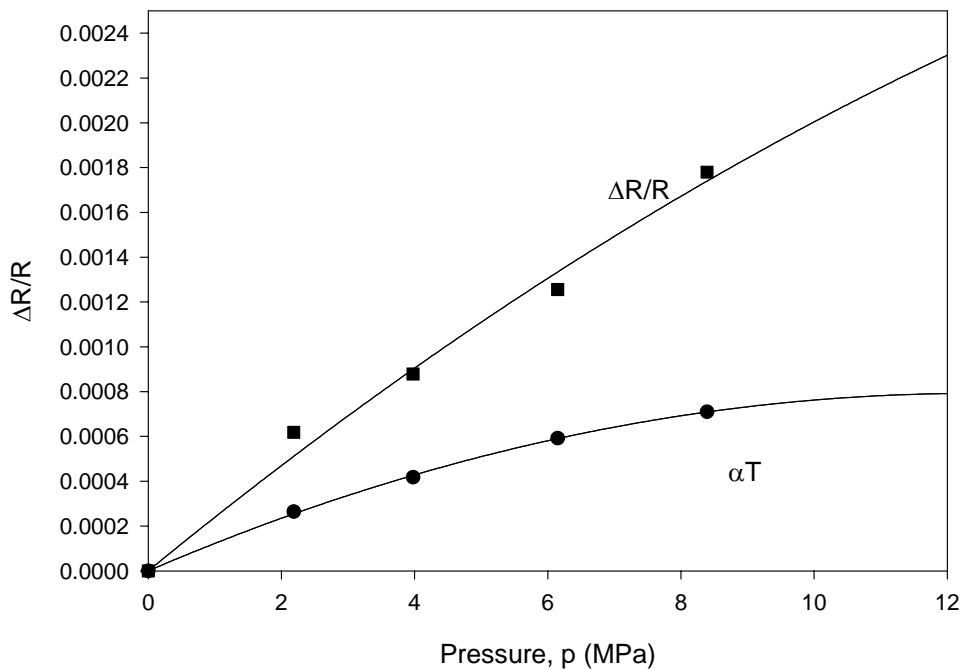## Board # 1, Site # 1

Adjusted Resistance Change

Hydrostatic Calibration Data
Resistance Change and Temperature Variation
N - Type Resistor, Orientation : -45°
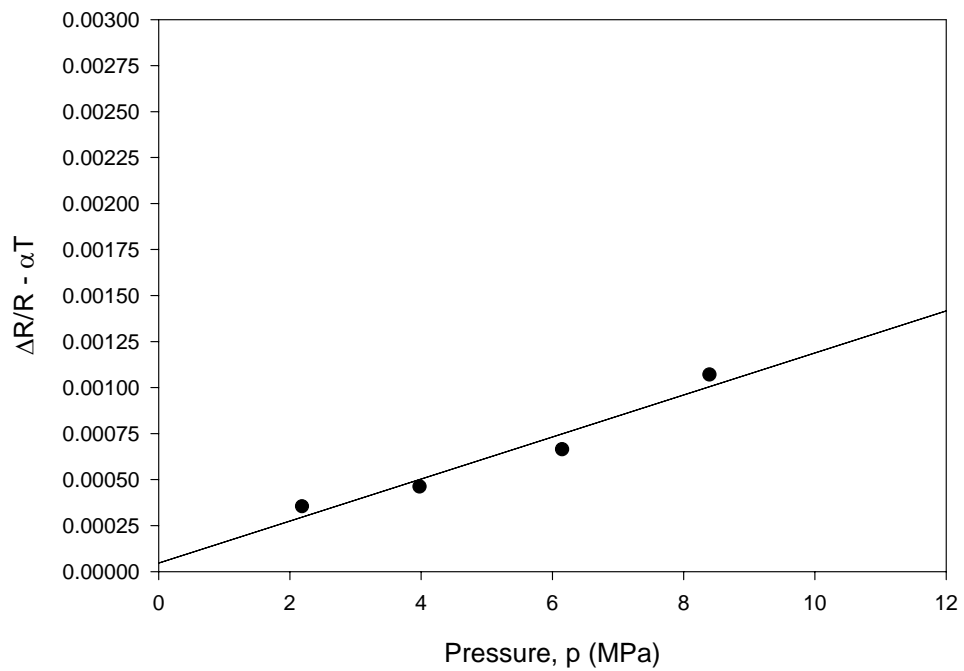## Board # 1, Site # 1

Adjusted Resistance Change

Hydrostatic Calibration Data
Resistance Change and Temperature Variation
N - Type Resistor, Orientation : -45°
Board # 2, Site # 1

ΔR/R

αT

Pressure, p (MPa)
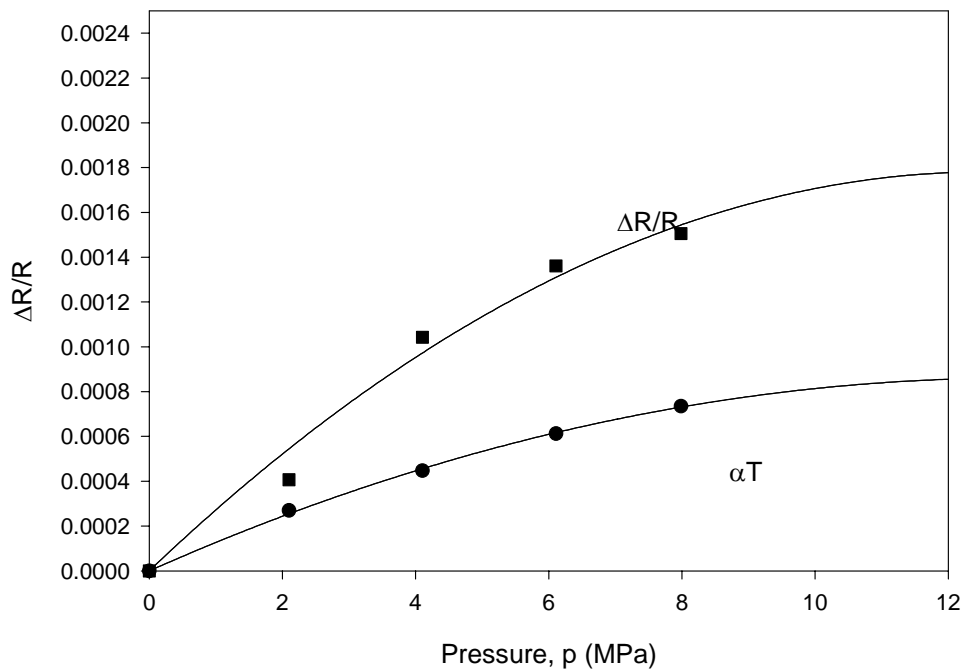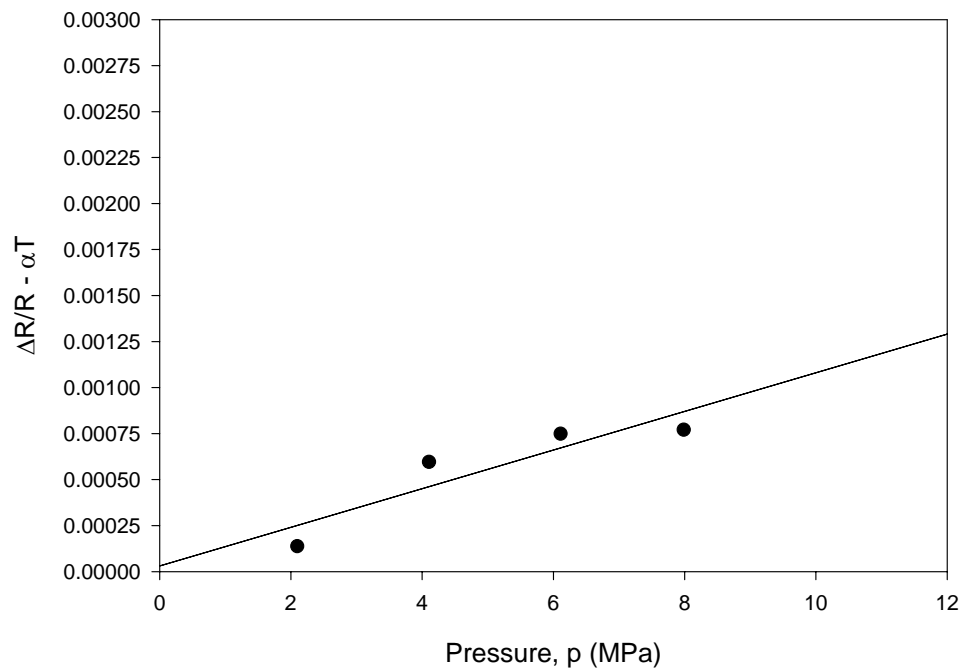
Adjusted Resistance Change

Pressure, p (MPa)

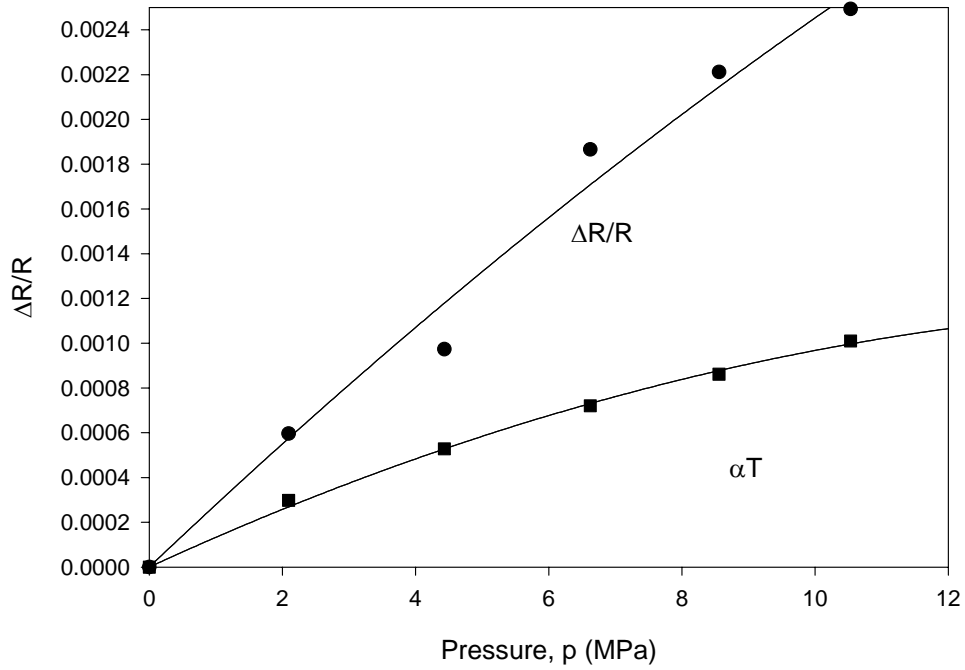# Hydrostatic Calibration Data
Resistance Change and Temperature Variation
N - Type Resistor, Orientation : -45°
Board # 6, Site # 1

Adjusted Resistance Change

Hydrostatic Calibration Data
Resistance Change and Temperature Variation
N - Type Resistor, Orientation : 90^{0}
Board # 6, Site # 1

$\Delta R/R$

αT

Pressure, p (MPa)

Adjusted Resistance Change

$\Delta R/R - \alpha T$

Pressure, p (MPa)

Hydrostatic Calibration Data
Resistance Change and Temperature Variation
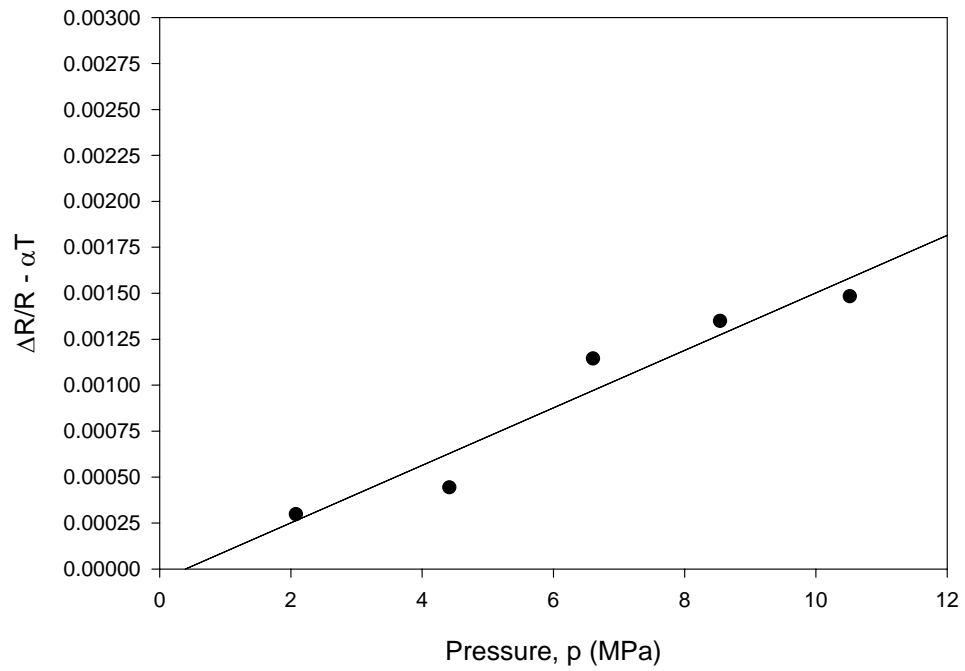## N - Type Resistor, Orientation : 0°
Board #1 , Site # 1

Adjusted Resistance Change

Hydrostatic Calibration Data
Resistance Change and Temperature Variation
N - Type Resistor, Orientation : 90 ^{0}
Board # 1, Site # 1

Adjusted Resistance Change

Hydrostatic Calibration Data
Resistance Change and Temperature Variation
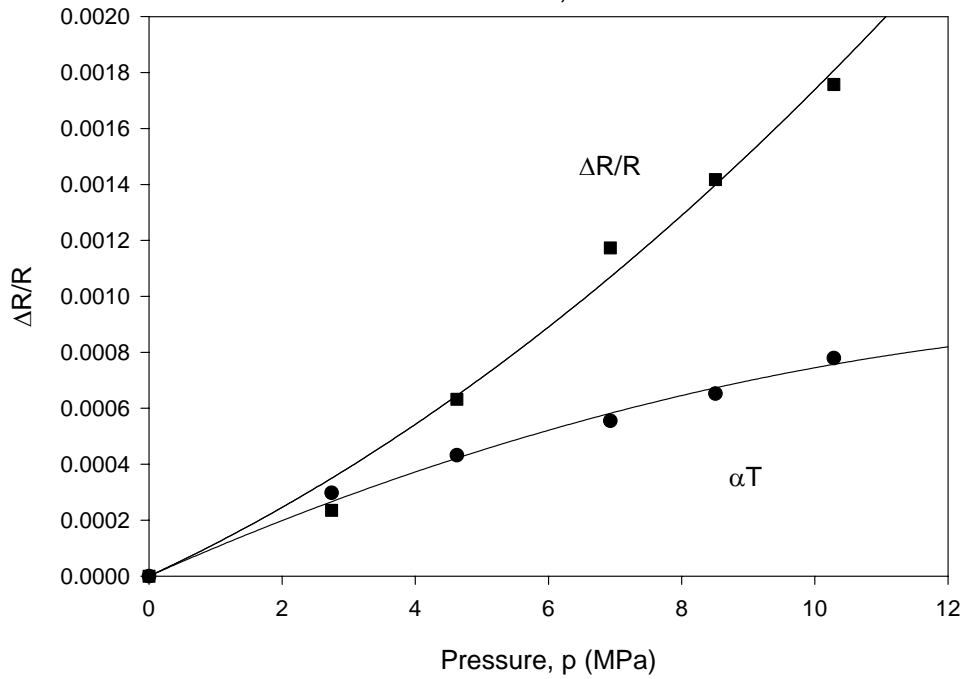## N - Type Resistor, Orientation : -45°
Board # 1, Site # 1

Adjusted Resistance Change

Hydrostatic Calibration Data
Resistance Change and Temperature Variation
N - Type Resistor, Orientation : -45°
## Board # 2, Site # 1

Adjusted Resistance Change

P-Type Sensors

Sample	π_p(1/TPa)	TCR (x 10-6 1/^{o}C)
B1S1P45	193.8	1404
B2S1P-45	121.9	1515
B4S2P0	161.7	1418
B1S1P45	138.2	1404
B1S1P-45	114.2	1409
B3S2P0	184.8	1457
B4S1P0	156.4	1568
B4S2P0	182.4	1418
B5S2P90	140.4	1438
B6S1P45	123.4	1577
Average	151.7	1460.6
St. Dev.	28.6	67.7

Hydrostatic Calibration Data
Resistance Change and Temperature Variation
P - Type Resistor, Orientation : 45 ^{0}
Board # 1, Site # 1

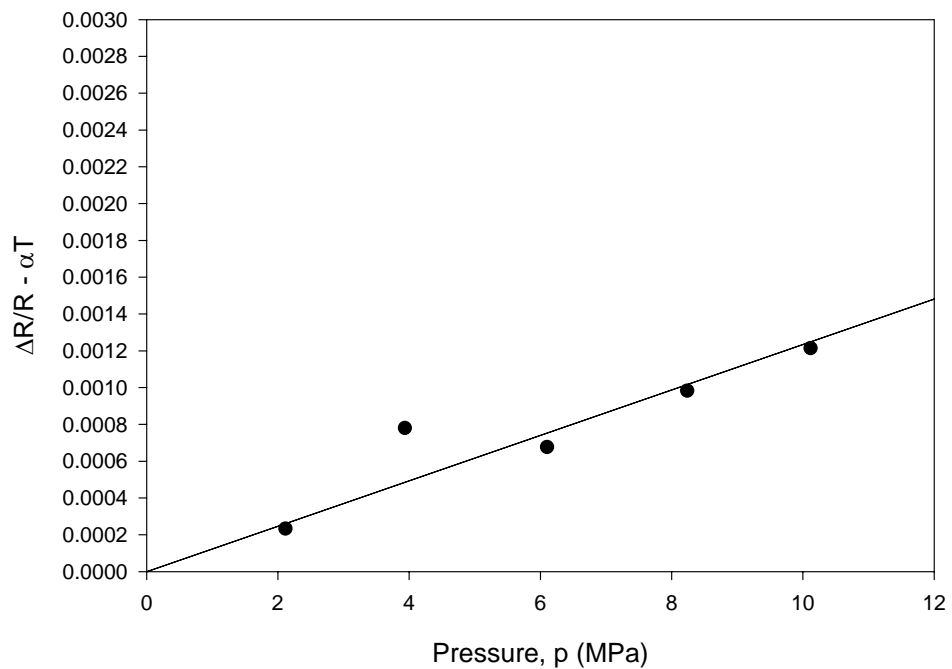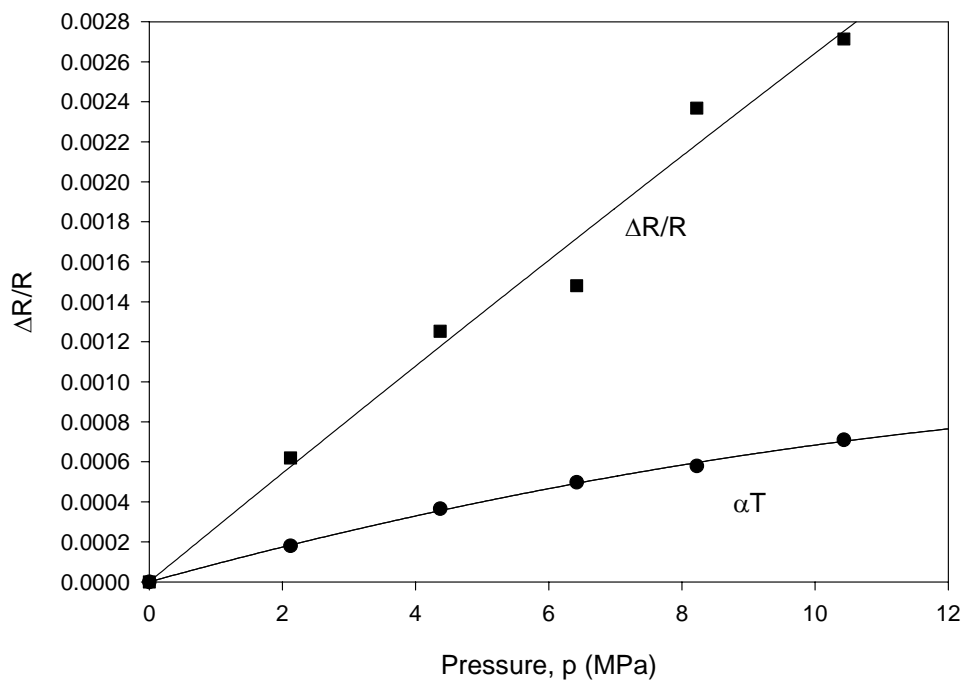## Adjusted Resistance Change

Hydrostatic Calibration Data
Resistance Change and Temperature Variation
P - Type Resistor, Orientation : -45°
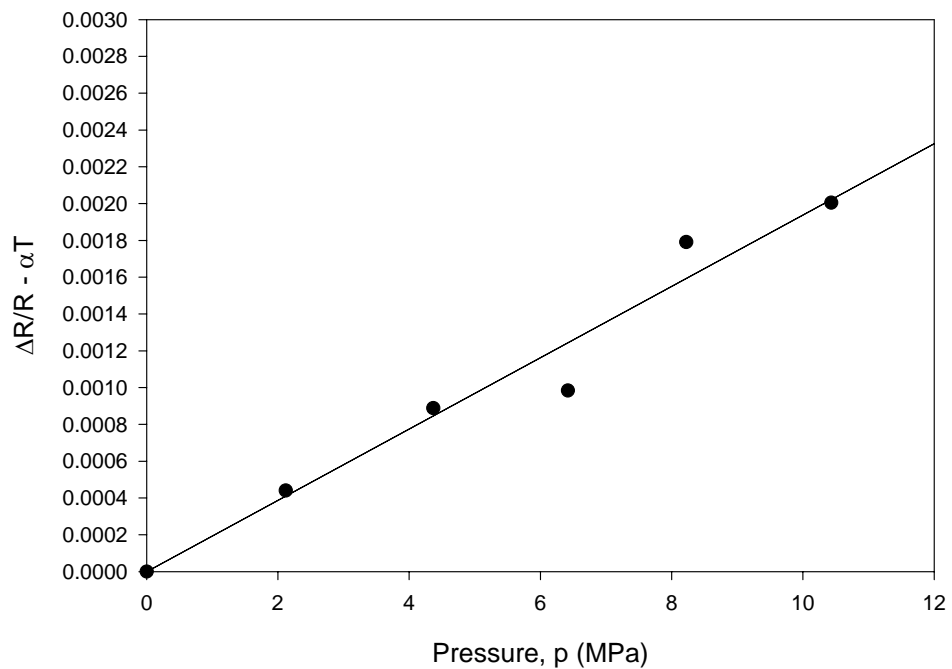## Board #1 , Site # 1

$\Delta R/R$

αT

Adjusted Resistance Change

Hydrostatic Calibration Data
Resistance Change and Temperature Variation
P - Type Resistor, Orientation : -45°
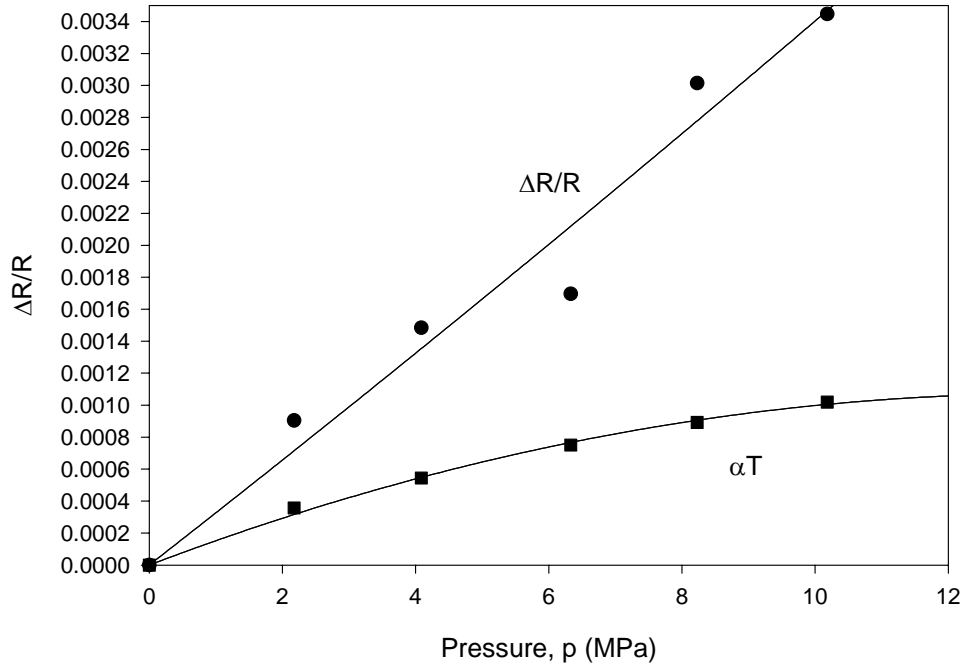## Board # 2, Site # 1

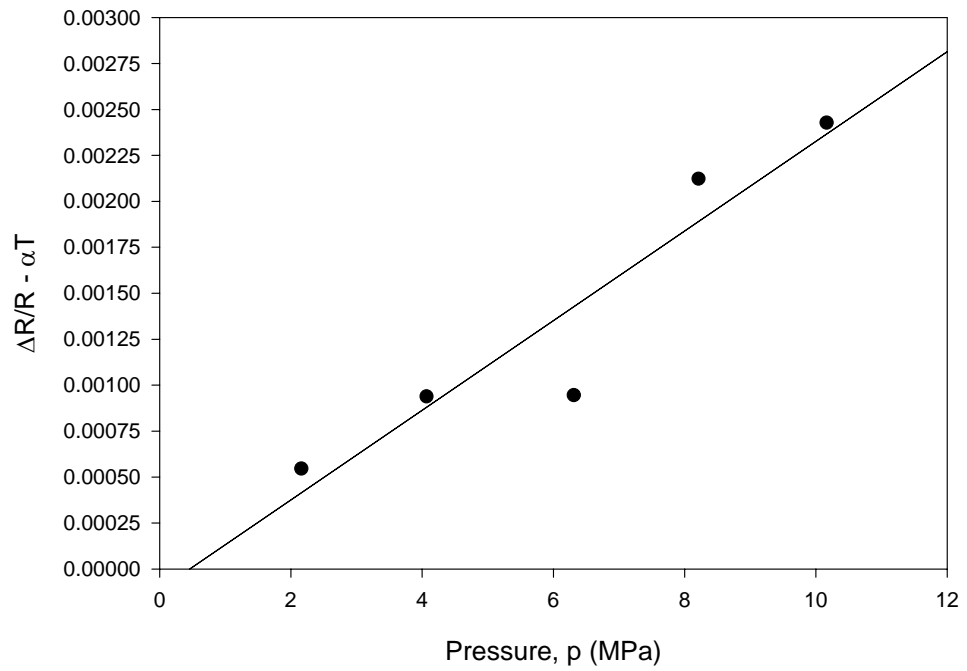## Adjusted Resistance Change

Hydrostatic Calibration Data
Resistance Change and Temperature Variation
P - Type Resistor, Orientation : 0°
Board # 4, Site # 1

Adjusted Resistance Change

Hydrostatic Calibration Data
Resistance Change and Temperature Variation
P - Type Resistor, Orientation : 90°
Board # 5, Site # 2

Adjusted Resistance Change
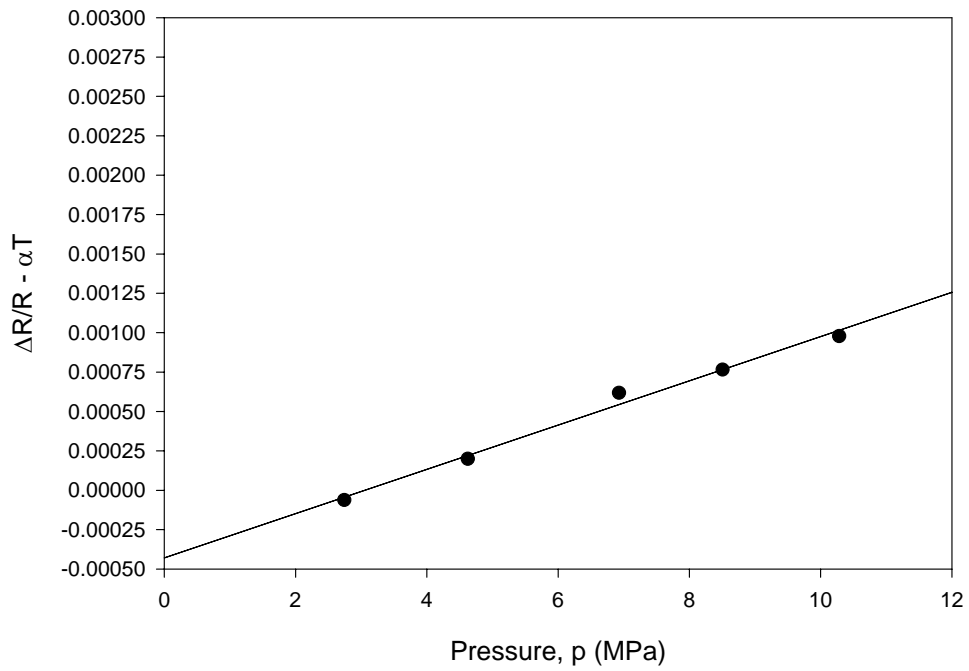
Hydrostatic Calibration Data
Resistance Change and Temperature Variation
P - Type Resistor, Orientation : 45 ^{0}
Board # 6, Site # 1
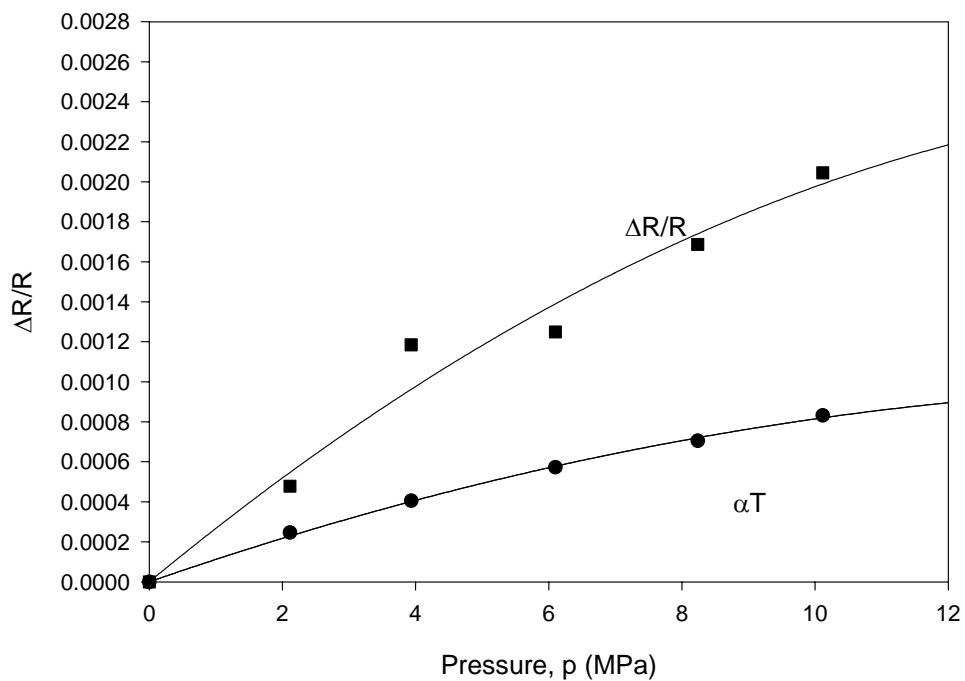
Adjusted Resistance Change

Hydrostatic Calibration Data
Resistance Change and Temperature Variation
P - Type Resistor, Orientation : 45 ^{0}
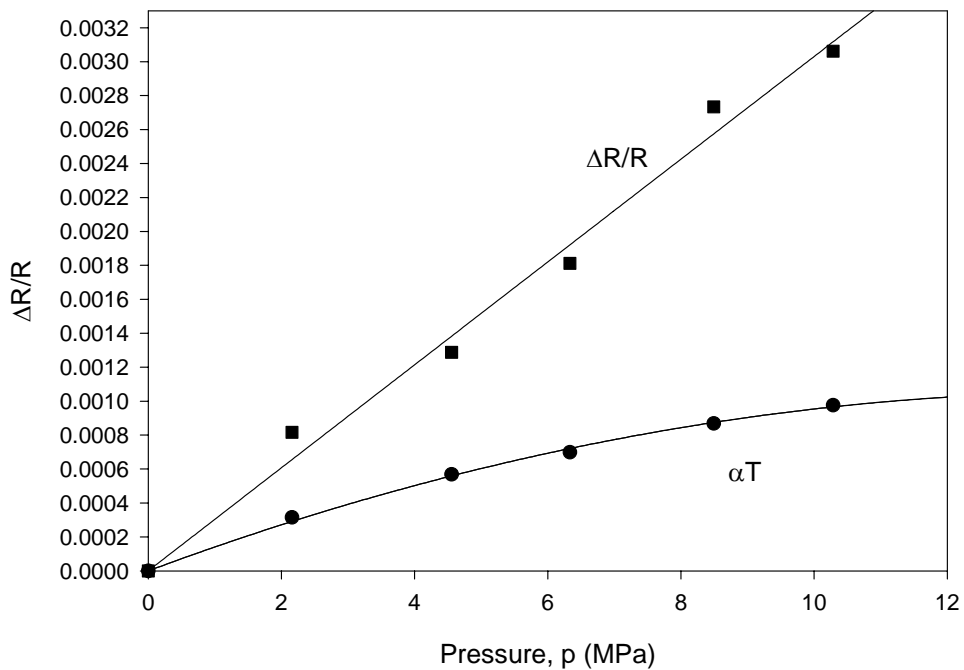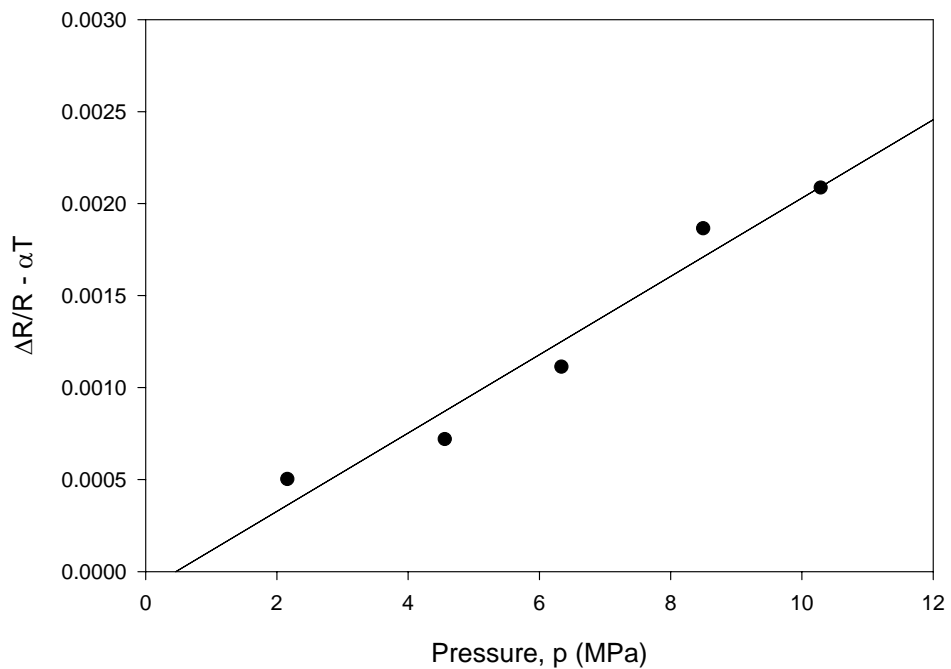Board # 1, Site # 1

Adjusted Resistance Change

Hydrostatic Calibration Data
Resistance Change and Temperature Variation
P - Type Resistor, Orientation : 0°
Board # 4, Site # 2

Adjusted Resistance Change

Hydrostatic Calibration Data
Resistance Change and Temperature Variation
P - Type Resistor, Orientation : 0 ^{0}
Board # 3, Site # 2

Adjusted Resistance Change

Hydrostatic Calibration Data
Resistance Change and Temperature Variation
P - Type Resistor, Orientation : 0^0
Board # 4, Site # 2
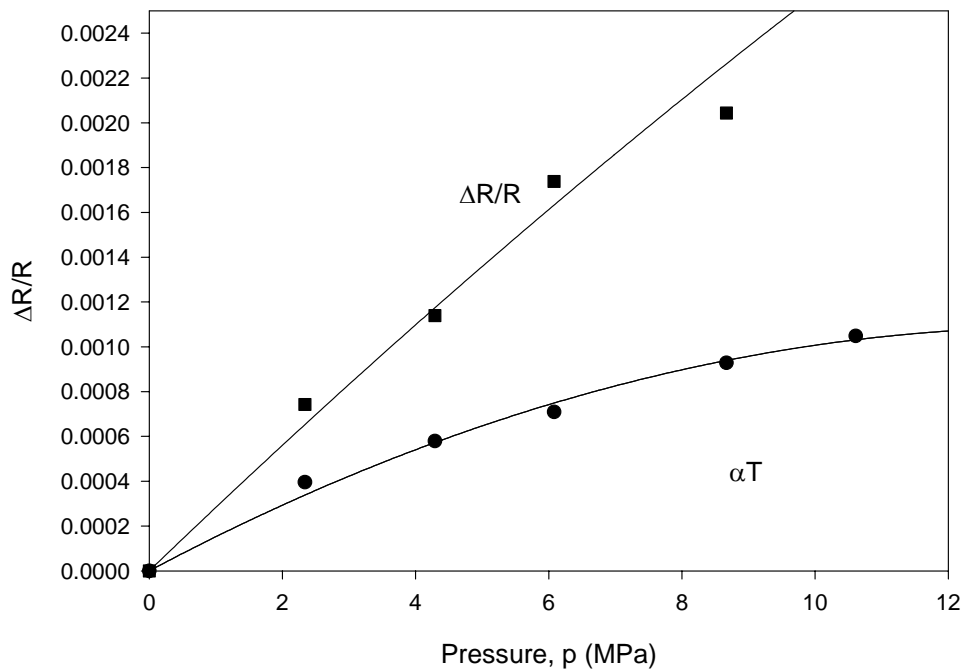
Adjusted Resistance Change
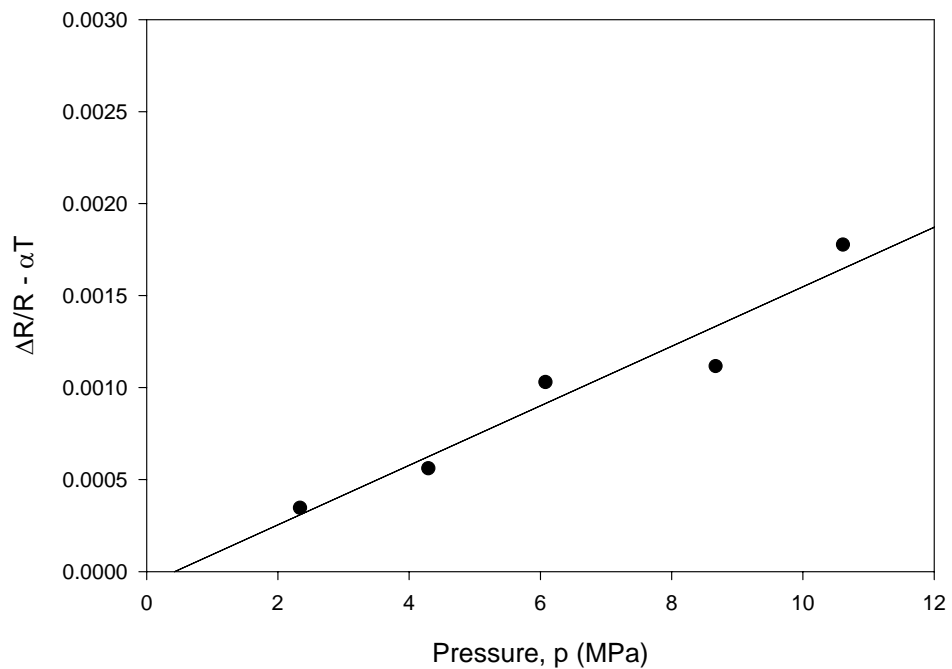
APPENDIX C

UNDERFILL STRESS STRAIN CURVES