FREQUENCY SYNTHESES WITH DELTA-SIGMA MODULATIONS AND THEIR

APPLICATIONS FOR MIXED SIGNAL TESTING

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FREQUENCY SYNTHESES WITH DELTA-SIGMA MODULATIONS AND THEIR APPLICATIONS FOR MIXED SIGNAL TESTING

Dayu Yang

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FREQUENCY SYNTHESES WITH DELTA-SIGMA MODULATIONS AND THEIR APPLICATIONS FOR MIXED SIGNAL TESTING

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VITA

Dayu Yang, son of Shangda Yang and Meilin Yao, was born in April 02, 1977 in Shanghai, P. R. China. He attended Shanghai Jiao Tong University in May 1995 and graduated with a Bachelor of Engineering degree in Communication Engineering in July 1999. He entered the Graduate School, Shanghai Jiao Tong University in September 1999 and received the Master of Science degree in Circuits and Systems in March 2002. Then he worked at Pericom Technology (Shanghai) Co. Ltd. as a mixed signal circuit design engineer. In January 2003, he joined Ph.D. program of the Department of Electrical and Computer Engineering, Auburn University.

DISSERTATION ABSTRACT

FREQUENCY SYNTHESES WITH DELTA-SIGMA MODULATIONS AND THEIR APPLICATIONS FOR MIXED SIGNAL TESTING

Dayu Yang

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This dissertation presents design and application of two popular frequency synthesizers, namely, the direct digital frequency synthesis (DDS) and phase lock loop (PLL) synthesis.

DDS is a digital technique for frequency synthesis, waveform generation, sensor excitation, and digital modulation/demodulation in modern communication systems. DDS provides many advantages including fine frequency-tuning resolution, continuous-phase switching and accurate matched quadrature signals. DDS can directly generate and modulate signal at microwave frequencies. A high-speed DDS can be significantly simplified the transceiver architecture. Thus the cost of radio and radar systems can be reduced considerably.

High speed DDS over GHz is demanding for wireless communication systems. This research proposes work on designing a high speed DDS chip with nonlinear DAC in Silicon Germanium (SiGe) process and using DDS as test pattern generator for analog circuitry built-in self test.

Nonlinear DAC is needed for high speed DDS for it replaces conventional ROM and linear DAC. The structure and system performance are analyzed with experimental data for a DDS with nonlinear DAC. Tradeoffs should be made to gain the best performance with feasible hardware implementation.

Spurious components in the DDS output spectrum introduced by the phase truncation are problems and delta-sigma modulators can be used either in phase or frequency domain to suppress in-band spurs. The formula deductions of delta-sigma modulation in both phase and frequency domain are presented and various delta-sigma modulators such as MASH, feed-forward, feedback and error feedback have been implemented in both phase and frequency in a CMOS DDS chip and their performances are compared.

Circuit and layout designs using SiGe technology of DDS building blocks such as current mode logic (CML), 11-bit pipe-lined accumulator, 12-bit carry look-ahead accumulator, 1-1-1 Mash type delta-sigma modulator and a nonlinear DAC are discussed.

A DDS-based built-in-self-test (BIST) is presented for analogy circuit test. It uses DDS for test pattern generator (TPG) and a multiplier and accumulator as output response analyzer (ORA) and thus avoids traditional FFT-based spectrum analysis. Detail methods of frequency response and linearity test are introduced and verified by a field programmable gate array (FPGA) experimental results.

PLL is another important frequency synthesis for its small area and power consumption. Fractional-N type PLL can have a wide loop bandwidth and fast settling time. The fractional spurs are reduced by delta-sigma modulators with new coefficients that have less out-band noise in order to suppress the modulators output bit pattern. A 2.5 GHz fractional-N PLL is designed in silicon on insulator (SOI) technology for its full dielectric device isolation, less junction capacitances, lower average device threshold voltages and less body effect and source follower effect.

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CHAPTER 1 INTRODUCTION

1.1 **RFIC Design**

Radio frequency integrated circuit (RFIC) design becomes challenging with the growing demand of wireless and communication market. The competence resides in high performance, high compatibility [1], lower cost and low power dissipation. In addition, high levels of integration, which may include all of the analog and digital functions related to transceiver and built-in self-test (BIST) are the design goals to achieve better performance. The thesis presents research work on one of the building blocks of RFIC--frequency synthesizer design and its application for analog circuit build-in-self-test (BIST).

Device technology plays an important role in RF IC design. Bipolar device takes its advantages in high speed, high trans-conductance (g_m), low noise of its npn transistor, but it has a slow pnp transistor and high power consumption [2].

CMOS technology is gaining its popularity in RF circuits [3][4]. It's preferred for low quiescent power dissipation, complementary transistors, low cost and easy scaling. Its disadvantage is its low speed and large noise, the limited set of available passive devices. The modeling for the CMOS technology is mainly optimized for digital design and it needs accurate model for RF design [5].

Bipolar complementary metal-oxide-semiconductor (BiCMOS) technology can provide high integration capability of both digital and analog circuitry as well as high performance

levels. BiCMOS IC technology is viewed as a good candidate for implementing the relatively complex digital functions because the high current-drive capability of the bipolar transistors greatly facilitates driving large capacitive loads. The hetero-junction bipolar transistor uses two different materials such as Si and Ge to form a pn junction inside the transistor to reach higher unity gain-bandwidth product (f_T), low noise, good linearity and low power consumption compared to BJT. Mature SiGe technology [6] that has many generations provides a full device suite for RF IC design, including a trench isolated, highly planar SiGe hetero-junction bipolar transistor (HBT), n-MOS and p-MOS devices, poly-silicon and diffused resistors, high-density MOS and high quality-factor metal-insulator-metal (MIM) capacitors, varactor diodes, and spiral inductors. It makes it possible to achieve full mixed-signal design and high levels of integration in RF IC design.

Silicon-On-Insulator (SOI) CMOS circuits differentiate from conventional bulk CMOS for its device is built on a thin silicon layer placed upon an insulator. Circuits fabricated in a SOI process can operate with higher speed and lower power consumption than circuits fabricated with bulk CMOS because the reduced parasitic capacitances intrinsic to the device structure is isolated from the substrate. The buried insulator layer allows the use of a high resistance substrate, which significantly reduces the device capacitance and the loss of passive components, such as inductors, that are commonly used in analog and RF circuits. Thus, SOI provides an advantage over bulk MOS to realize complete systems on a chip by integrating high speed digital devices with high performance analog and RF devices.

1.2 **Frequency Syntheses**

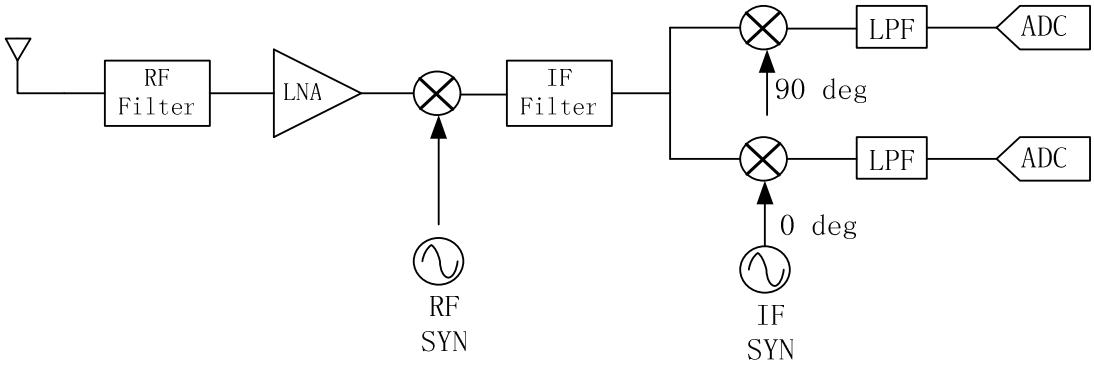


Figure 1-1 Frequency synthesizer in a super-heterodyne receiver.

In a RF transceiver, a frequency synthesizer is needed to generate the local oscillation (LO) frequency to mix with the received RF signal and down-convert it to IF and base band. A typical super-heterodyne receiver is shown in Figure 1-1, two frequency synthesizers are used to provide different local oscillation signals. Quadrant signals from the IF synthesizer are used to get rid of the image signal from the mixers. Ideal frequency synthesizer generates a pure sinusoidal wave form for frequency translation. Its purity is highly demanded such that no image signal caused by synthesizer after mixer. But due to systematic design, repetitive pattern disturbance and noise from circuits, the synthesizer output's amplitude and phase varies from the desired design values, the output spectrum is never an ideal single tone. It usually contains of unwanted spurious frequency components and phase noise and it could mix with the input signal and produce side bands and noise in the desired channel. This reduces the sensitivity and selectivity of a receiver. So the main frequency synthesizer design goal is to get low spurious tones and low phase noise in the output spectrum with minimum power and area consumption. On other aspects, fine channel spacing in transceivers require high frequency resolution as low as Hz and quick

frequency toggling needs fast frequency switching speed as high as GHz. Besides generating pure local oscillation frequency, synthesizers need to combine modulation techniques to realize a modulated transmitter.

There are mainly two types of frequency synthesizer, namely, the phase locked loop (PLL) and direct digital synthesizer (DDS). PLL is a conventional way to realize low phase noise and low spurious tone frequency synthesizer. But the need of high-Q passive component and off chip components makes it a hard for a full integration. Besides, narrow bandwidth of the integer-N type PLL makes it relatively low frequency switching speed of the system. Fractional-N type PLL achieves fine step size since the output frequency can vary by a fraction of the input reference frequency. As a result, the fractional-N PLL can have high reference frequency and low division ratio, which leads to lower in-band noise. However, it also generates fractional spurs in the output spectrum due to periodic switching of the divider ratio.

DDS can provide fast frequency switching, fine resolution and wide tuning range in frequency-agile communication systems and it is suitable for integration for no need of off-chip components. It can also provide various direct modulations such as chirp, MSK, FSK and GMSK. DDS is also flexible as a test pattern generator in testing area and addresses an application in BIST for RF circuits. Its drawback is that high speed and high resolution is usually achieved at the cost of big area and huge power consumption.

These two types of frequency synthesizers both suffer from unwanted spurs in the vicinity of the main output frequency. These spurs are caused by the periodic disturbance due to their own mechanisms. Delta-sigma modulation technique is used to decrease the

periodic disturbance without affecting the synthesizer's function. Various types of delta-sigma modulators in frequency synthesizers can have different effects in spur reduction.

1.3 **Dissertation Organization**

In Chapter 2, the fundamentals of direct digital synthesis including the spurs and quantization noises introduced by phase and amplitude truncation are reviewed. Nonlinear DAC is introduced to DDS to replace the speed bottle neck ROM lookup table and linear DAC. Top level structure and system performance are analyzed and design tradeoffs are evaluated.

In Chapter 3, the basics of delta-sigma modulation are introduced and its white noise linear model is examined. The effectiveness of various types of delta-sigma modulators in both frequency domain and phase domain of DDS is verified by math deduction and real implementation in a CMOS chip. Their performances including spur reduction effect, area, speed and stability are compared.

In Chapter 4, the RF circuit designs of DDS building blocks such as CML digital circuits, phase accumulators, delta-sigma modulator and nonlinear DAC are discussed

In Chapter 5, a DDS-based BIST approach for analog frequency response and linearity test is proposed.

In Chapter 6, a fractional-N type wide-band PLL in SOI technology is presented.

Chapter 7 concludes the thesis with a summary.

CHAPTER 2 DIRECT DIGITAL SYNTHESIS

2.1 Introduction

In this chapter, basic ROM-based the direct digital synthesis(DDS) and its mechanism are first reviewed in section 2.2. Phase truncation after the accumulator and DAC's amplitude quantization can cause unwanted the spurs and noise in the output spectrum. The location and strength of the spurs can be determined by the phase accumulator's length *L* and phase word *W* that addresses the ROM. Increasing the *W* and DAC bits *D* can lead to reduction of spur and noise but may cause bigger area and power consumption. Standard Sine ROM compression technique stores only first quadrant amplitude value to reduce 75% the ROM.

In section 2.3, a nonlinear DAC replaces the conventional ROM lookup table and linear DAC in DDS to reach high speed. In section 2.4, the structure and system performance such as SNR and SFDR of DDS with a nonlinear DAC are analyzed. An experimental structure design is given in section 2.5.

2.2 DDS Fundamentals

2.2.1 Conventional ROM-based DDS

Figure 2-1 shows a conventional ROM-based DDS, The output frequency of the DDS depends on the input *L*-bit word named frequency control word (FCW). At each positive

edge of the reference clock cycle the FCW is added to an accumulator. At any instant, the value in the accumulator represents the phase of the output sinusoid, so it is referred as phase accumulator register. The value in the phase accumulator register is used to address the ROM storing the values of the sinusoid in digital domain. The DAC and filter are used to reconstruct the waveform in analog domain. The frequency resolution is determined by the word length of the phase accumulator which is *L*.

$$f_{out} = f_{clk} \cdot \frac{FCW}{2^L} \tag{2.1}$$

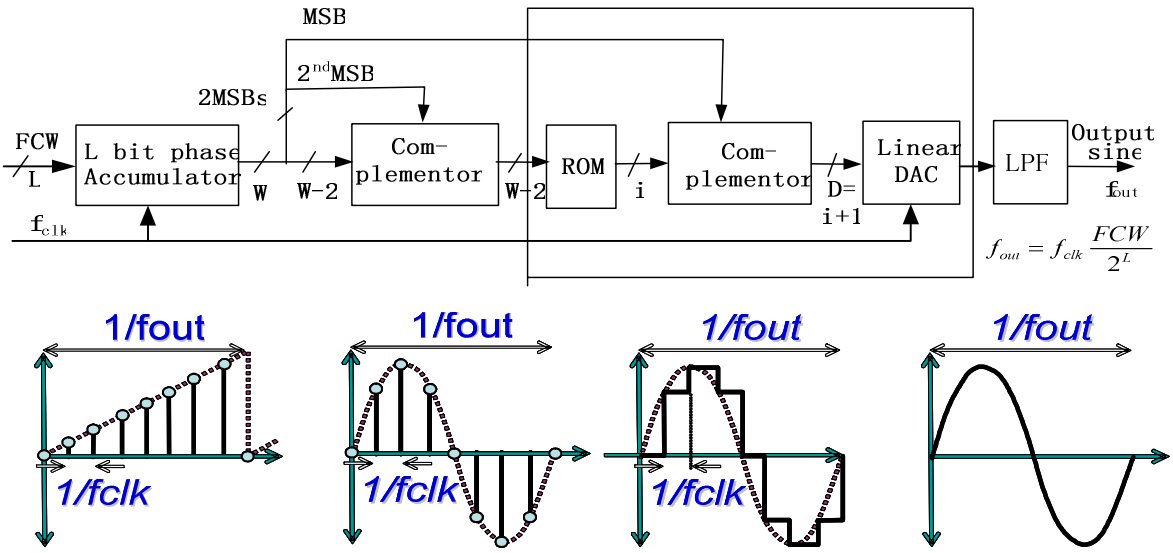


Figure 2-1 Conventional ROM-based DDS.

Finite phase word length and amplitude word length will cause quantization errors and thus lead to unwanted spurs and noises in the output wave form. The actual word length of the phase information in the sine ROM will determine the phase quantization error, while the number of the bits in the digital-to-analog converter (DAC) will determine the amplitude quantization error. Therefore, it is desirable to increase the resolution of the ROM and DAC. Unfortunately, larger ROM and DAC resolutions mean larger area, higher power consumption, lower reliability, lower speed, and greatly increased costs. Some

memory compression techniques can be used to alleviate the problem and will be introduced later. However, the truncation of the phase accumulator bits dressing the sine ROM is necessary. This "phase truncation error" corrupts the output sinusoid and it's periodic and results in spurs in output spectrum of DDS as shown in Figure 2-2(a). The location and magnitude of these spurious spurs have been calculated by Nicholas and Samueli[7]. Knowing that FCW is the input frequency control word, *L* is the accumulator's size, *W* is the number of bits addressing the ROM. *B=L-W* is the truncated phase word bits. The number of spurs is:

$$N = \frac{2^{B-1}}{(FCW, 2^{L})} \tag{2.2}$$

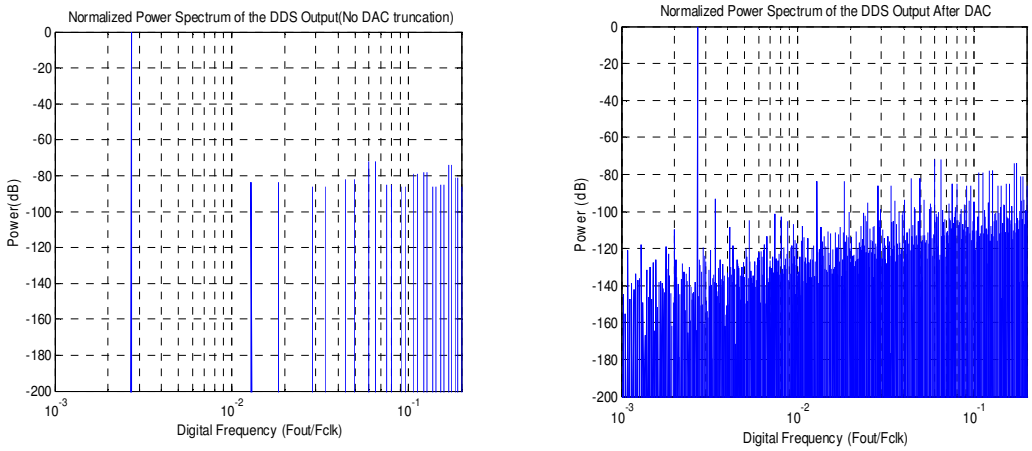
where (FCW, 2^L) represents the greatest common divisor of the FCW and 2^L.

These spurs are equally spaced between 0 and $f_{clk}/2(FCW, 2^L)$ in the spectrum. The magnitude of the largest spur in the spectrum is given by:

$$\zeta_{worst} = 2^{B-L} \frac{\pi(FCW, 2^{B})/2^{B}}{\sin(\pi(FCW, 2^{B})/2^{B})} \tag{2.3}$$

There is something important between the magnitude of the largest spur and (FCW, 2^B). The magnitude of the worst case spur in the spectrum is a decreasing function of (FCW, 2^B) with the maximum value provided by (FCW, 2^B) = 2^{B-1}. If (FCW, 2^B) =1, the worst case spur would be 3.933dB lower than the spur caused by same *B*, but unrestricted values of FCW. Nicholas has proposed an architecture to force the (FCW, 2^B)=1 to get the half bit improvement in worst case spur [7]. Under this situation, when *B* is bigger than 4, the magnitude of the worst case spur can be approximately estimated as 2^{-W}.

Similarly, the amplitude truncation of ROM to DAC can also introduce quantization to the output. The spurious spurs caused by the quantization effects both in phase and amplitude are shown in Figure 2-2(b), the locations of the spurs are mainly determined by phase truncation. ROM and DAC would affect the magnitudes of the spurs and also increase the noise power density in band by 6dB per bit. The in-band noise plus spurs close to the main signal cannot be filtered by the low pass filter afterward.



(a) Spurs caused by pure phase quantization

(b) Spurs and noise caused by both phase and amplitude quantization

Figure 2-2 Spurs and noise in output spectrum caused by phase, amplitude quantization (L=16, W=10, D=12).

2.2.2 **Quadrant Compression of ROM**

The size of the ROM can be reduced by more than 75 percent by taking advantage of the fact that only one quadrant of the sine wave form needs to be stored. As shown in Table 2-1 [8], the second, third and fourth quadrants of a sine waveform can be constructed by using the phase to amplitude information of first quadrant and the two MSBs of the phase information *W*.

Table 2-1 Quadrant table of a sine wave in one period

Phase	MSB	MSB-1	Sine
0<A<90	1	0	sinA
90<A<180	1	1	sin(90-A)
180<A<270	0	0	-sinA
270<A<360	0	1	-sin(90-A)

Thus, given a sin(A) over only the first quadrant, the operations necessary to flip to the other quadrants are as shown in Table 2-2.[8]:

Table 2-2 Flipping Operations from first quadrant to other quadrants

Quadrant I	0.5+0.5sin(k) (k is running index from 0 to 2^{W-2}-1)
Quadrant II	0.5+0.5sin(k) (k is complemented running index from 0 to 2^{W-2}-1)
Quadrant III	0.5-0.5sin(k) (k is running index from 0 to 2^{W-2}-1)
Quadrant IV	0.5-0.5sin(k) (k is complemented running index from 0 to 2^{W-2}-1)

Figure 2-3 shows the hardware implementation of a quadrant compressed sine ROM, the second MSB of the phase word is used to switch on and off the 1's complement of the rest phase word. The inverse of the first MSB of the phase word is used to switch on and off the 1's complement of ROM output. The first MSB of the phase word is also the MSB of the final digital amplitude output.

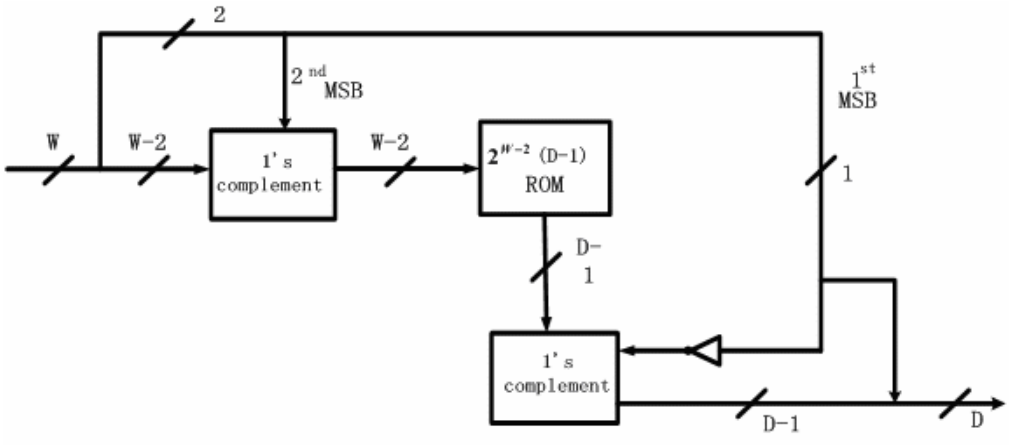


Figure 2-3 Quadrant compression of sine ROM.

2.3 **DDS with Nonlinear DAC**

In conventional ROM-based digital frequency synthesizer, it's not easy to achieve output frequency bigger than 2GHz because of the time and area consumed by ROM look up table. At present, ROM-less DDS gains popularity because it uses a nonlinear DAC to replace the ROM lookup table and the linear DAC and thus can generate much higher output frequency [9][10].

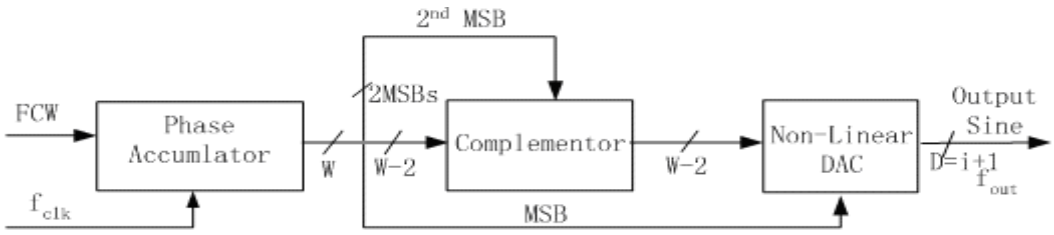


Figure 2-4 High-speed DDS with a nonlinear DAC.

The function of a nonlinear DAC in DDS is to convert the linear phase information *W* at the output of the accumulator directly into analog sine waveform as shown in Figure 2-4. The truncated phase information *W* is divided into several parts. The first two MSBs are used to select different quadrants of the sine wave. The rest bits are segmented into a, b two parts. The whole phase $0 \sim \pi/2$ in the first quadrant is divided equally into $2^{(a+b)}$ phase steps. With the corresponding DAC bits $D=i+1$, each phase step corresponds to a DAC output magnitude. The difference of each phase step magnitude forms basic DAC cells and each cell's output value is O_K given as [11]

$$O_{k=}\begin{cases}\text{int}\left[(2^{i}-1)\sin\dfrac{\pi(0.5)}{2\left(2^{a+b}-1\right)}\right], & for \quad k=0\\ \text{int}\left[(2^{i}-1)\sin\dfrac{\pi(k+0.5)}{2\left(2^{a+b}-1\right)}-\sum_{n=0}^{k-1}O_{n}\right], & for \quad 1\le k\le 2^{a+b}-1\end{cases} \tag{2.4}$$

A switching matrix with row and column thermo-meter decoders is used to switch on and off each DAC cell according to the phase information *W*. The DAC output is the sum of all the DAC cells that the output of thermo-decoder turns on. As shown in Figure 2-5, the value of sine wave at phase step k is formed by summing the outputs form DAC $cell_0$ to DAC $cell_k$.

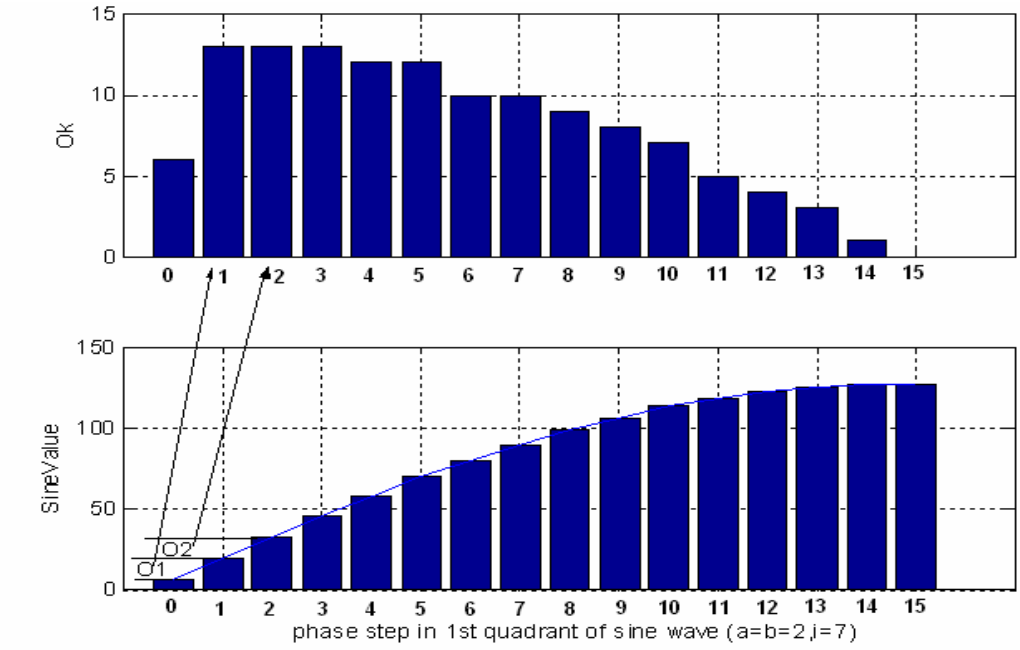


Figure 2-5 First quadrant sine wave construction using nonlinear DAC cells.

The first the quadrant sine wave form thus can be reconstructed by switching on and off different DAC cells with different values. Same as the ROM storing the first quadrant sine value, the other quadrants of sine wave form can be built by flipping the phase and output waveforms as shown in Figure 2-3. The MSB output of the phase accumulator is used to provide the proper mirroring of the sine waveform at the π phase point. The second MSB is used to invert the remaining bits for the second and fourth quadrant of sine wave.

In next section, structure parameters of a DDS with nonlinear DAC such as the accumulator length *L*, nonlinear DAC's input phase word *W*, DAC's output resolution *D* are evaluated according to the tradeoffs between system performance and hardware implementation.

2.4 **Optimization of DDS Structure Parameters**

DDS structure parameters directly impact its speed, area, power consumption and its output performance. Spurious free dynamic range (SFDR) is defined as the difference in decibels between the *root-mean-square* (*rms*) power of the fundamental and the largest spurious signal within a specified frequency band. SINAD is the difference in decibels between the rms power of the fundamental and the noise and distortion that falls within the Nyquist frequency.

There are several ways to improve these two targets. One is to increase the phase bit *W* to reduce spurs and Nonlinear DAC bit ($D = i+1$) to decrease the quantization noise effect. However, increase the *W* and *D* will also increase the complexity of the implementation. The other way is to add a delta-sigma modulator to shape the quantization noise and this will be discussed in next chapter. Higher order delta-sigma modulator has higher noise shaping effect of the quantization noise. But it also leads to bigger circuit implementation and may cause un-stability. So there is a tradeoff between the output performance and the complexity.

Different *W* and *D* combinations are compared in simulations to test the magnitude of the worst case spur and the result is shown in Figure 2-6. It plots the decibel difference

between the largest spurious (the worst case spur) and the fundamental signal versus the number of phase bits *W* and the number of nonlinear DAC output bits. It's shown that the worst-case spur decreases as the number of DAC bits or the number of phase bit *W* increase.

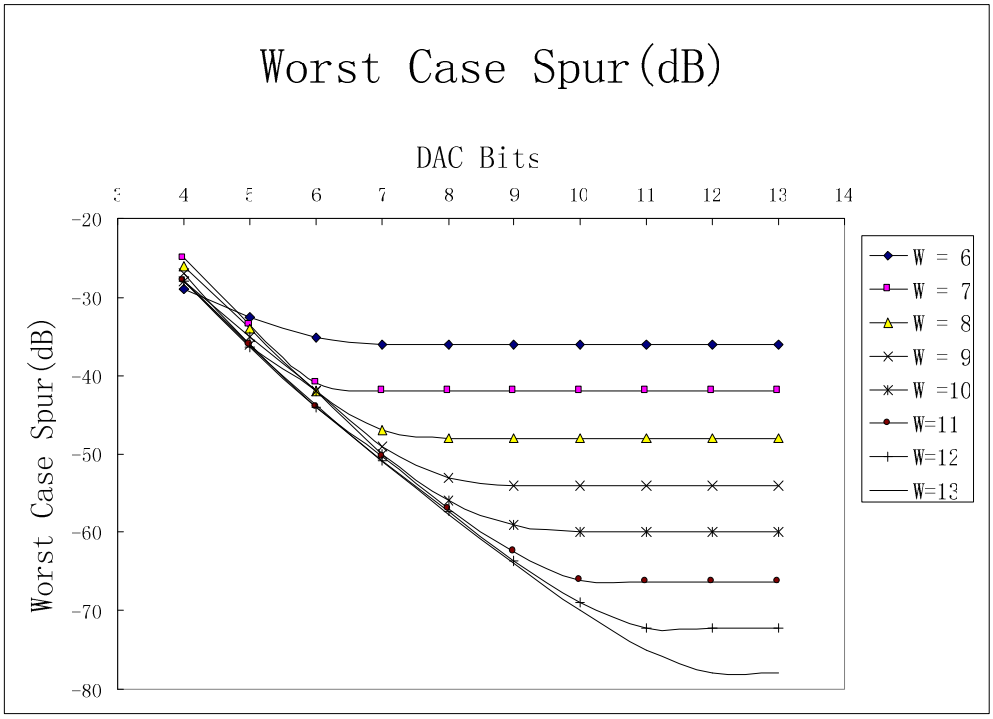


Figure 2-6 Worst case spur versus phase bit W and output bits D of nonlinear DAC.

From Figure 2-6 we can see that when the DAC bit *D* is bigger than the phase bit *W*, the Worst case spur is mainly determined by the DAC bit *D* and the phase bit W has little effect on it. When the phase bit *W* is bigger than DAC bit *D*, the increase of the phase bits *W* will decrease the worst spur.

When nonlinear DAC bit *D* and phase bit *W* are all bigger than 10, the worst case spur in dB with respect to carrier can be restricted below the -60dB.

From the viewpoint of the implementation, it's needed to keep DAC output bits *D*

small for less power consuming. Besides, the total current output will double with one bit increase in *D* and this will bring to the headroom design problem of the circuit. SINAD is used to determine the DAC output bits *D*. The SINAD at the output with different nonlinear DAC bits *D* and phase bits *W* is shown in Figure 2-7. The band of interest is $0.25 \cdot f_{clk}$.

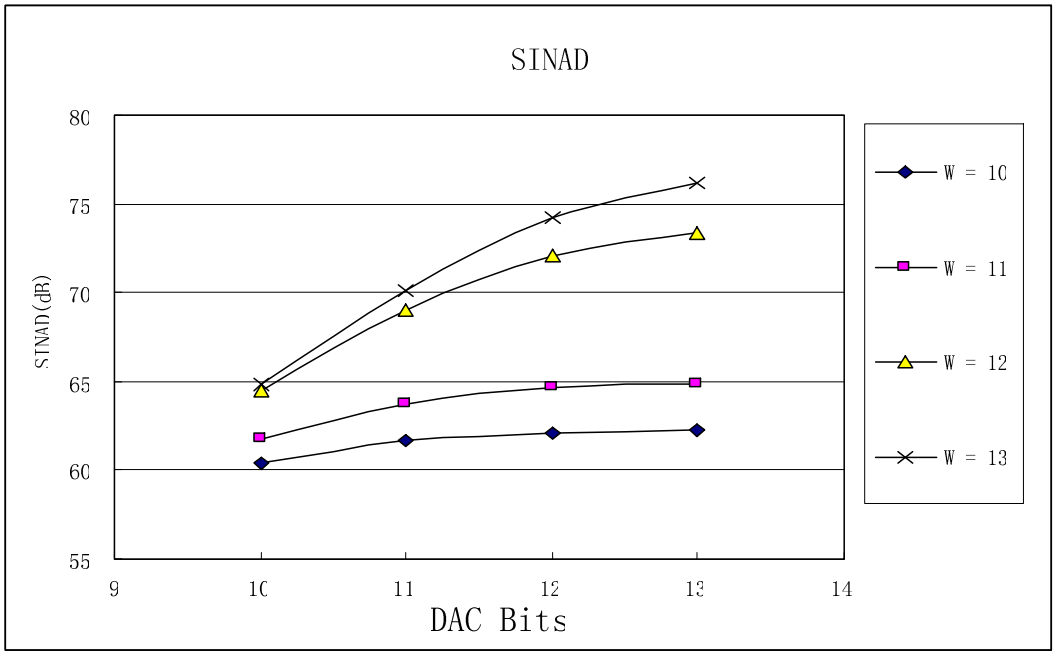


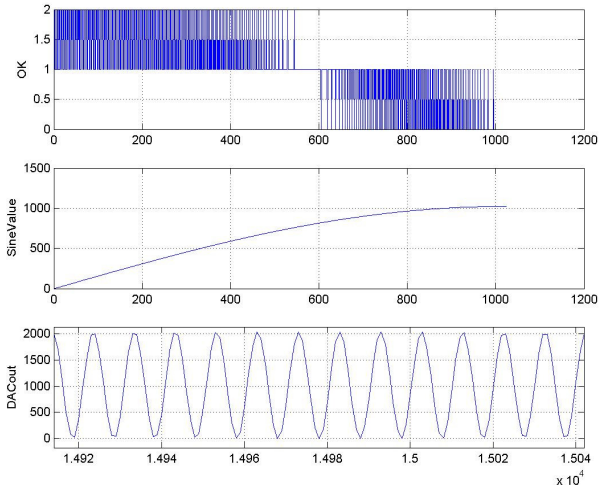
Figure 2-7 SINAD with different DAC bits *D* and phase bits *W* (BW=$0.25 \cdot f_{clk}$).

SINAD increases with the increase of the DAC bits *D* and phase bits *W*. Normally, the number of phase bits *W* is chosen slightly larger than that of the DAC output bits such that the overall quantization noise is dominated by the number of DAC bits *D*.

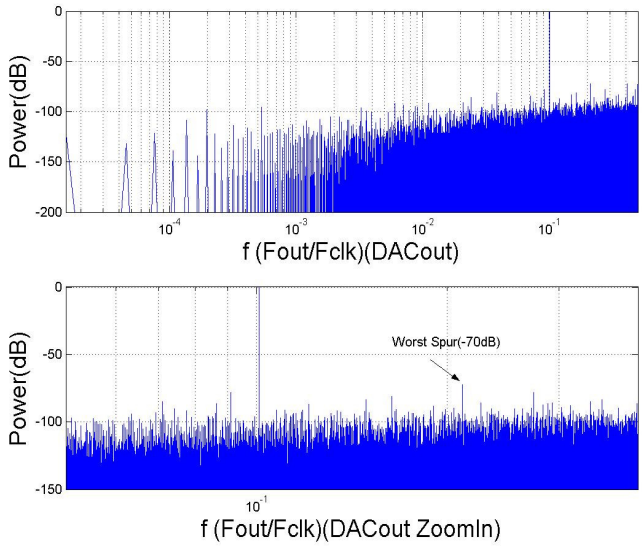
According to the discussion of tradeoffs between SFDR, SNR and hardware implementation, the phase bits *W* is first determined by the in-band worst case spur requirement. Then the DAC output is determined using the SINAD within the band.

2.5 **Experimental Structure Design and Results**

Figure 2-8 shows a design example with parameters *L*=16, *W*=12, *D*=11 of the nonlinear DAC. The basic DAC cells values, first quadrant waveform and whole time domain waveform is shown in Figure 2-8 (a)and the output spectrum is shown in Figure 2-8 (b)



(a) The output sine wave form (*L*=16, *W*=12, *D*=11)



(b)Output power spectrum (*L*=16, *W*=12, *D*=11)

Figure 2-8 Structure design of DDS with nonlinear DAC with *L*=16, *W*=12, *D*=11

In this design, the SINAD would be 68dB in a relative wide band-with which is $0.25 \cdot f_{clk}$ and the worst case spur can reach -70dB.

CHAPTER 3 DELTA-SIGMA MODULATION IN DIRECT DIGITAL SYNTHESIS

3.1 Introduction

Delta-sigma modulation has been used in high-performance ADC, DAC and fractional-N frequency synthesizer and begins to appear in the DDS recently [12][13]. Section 3.2 first reviews the basic concepts of delta-sigma modulator. Section 3.3 discusses its linear white noise model. Based on the linear model, formula deductions of delta-sigma modulation in both phase and frequency domain for DDS are presented. Section 3.4 presents comparisons of various delta-sigma modulations in DDS. Delta-sigma modulators such as MASH, feed-forward, feedback and error feedback have been implemented in both phase and frequency domains in a CMOS DDS. The DDS prototype is fabricated in a 0.35μm CMOS technology with core area of 1.7x2.1 mm^2 and total 75 mA current. Measured DDS output demonstrates that frequency domain delta-sigma modulation achieves better SFDR and SINAD than phase domain delta-sigma modulation.

3.2 Delta-Sigma Modulation Basics

A common linear model of delta-sigma modulator is shown in figure 3-1 [14].

It consists of a quantizer and feedback loop. The system transfer function obtained from Figure 3-1 is given as follows

$$V(z)=G(z)U(z)+He(z)E(z) \quad (3.1)$$

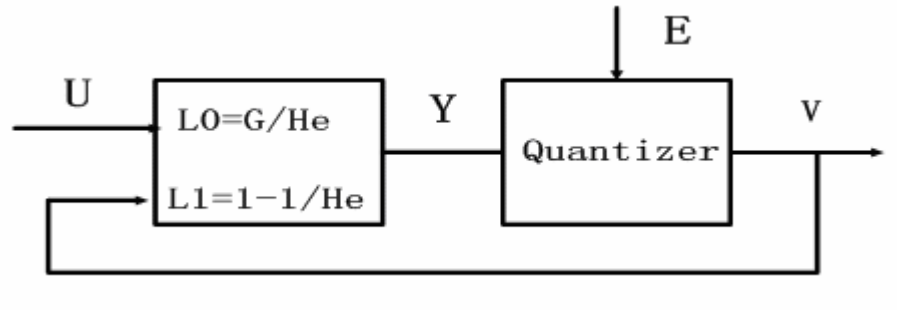


Figure 3-1 Linear model of delta-sigma modulator.

In equation (3.1), U(z) is the input signal，V(z) is the output signal, E(z) is the quantization noise，H(z) is *Noise Transfer Function* (NTF), G(z) is *Signal Transfer Function* (STF). STF can pass the base-band signal from input to output directly. NTF is usually a high-pass filter (HPF), it can restrain the base-band noise and let the high frequency noise pass. In this way, the quantization error is shaped away for the band of interest. For an L^{th} order MASH type, feedback, and error-feedback type delta-sigma modulator, their noise transfer function is given by

$$He(z)=(1-Z^{-1})^{L} \tag{3.2}$$

Assuming the quantization error e[n] is an additive white noise, its power is evenly distributed through the whole bandwidth:

$$\sigma_e^2=E[(e(n))^2]=\frac{1}{2\pi}\int_{-\pi}^{\pi} P_e(\omega)d\omega \tag{3.3}$$

Using transformation $z=e^{j\omega}$ and $\omega=2\pi f/f_s$, the modulated quantization noise from the L_{th} modulator is

$$P_L(\omega)=(2\sin\frac{\omega}{2})^{2L}\delta_e^2 \tag{3.4}$$

The sampling clock f_s, the baseband f_b and the frequency of the signal satisfy over-sampling condition, namely, $f_s>>f_b\geq f$:

$$P_L(f)=\frac{2P_L(\omega)}{f_s}=2(\sin\frac{\pi f}{f_s})^{2L}\delta_e^2/f_s\approx 2^{2L+1}(\frac{\pi f}{f_s})^{2L}\delta_e^2/f_s \tag{3.5}$$

The total quantization noise in the band of interest [0， f_b] is:

$$\varepsilon_L^2 = \int_0^{f_b} P_L(f)df = \frac{\pi^{2L}}{2L+1}\,\delta_e^2\left(\frac{2f_b}{f_s}\right)^{2L+1} = \frac{\pi^{2L}}{2L+1}\,\delta_e^2\left(\frac{1}{R}\right)^{2L+1} \tag{3.6}$$

For an input sine wave form with power $\sigma_x^2=E^2/2$, the signal to noise ratio (SNR) and dynamic range (DR) of L^{th} order delta-sigma modulator are:

$$SNR_L = \sigma_x^2/\varepsilon_L^2 = \frac{3\cdot 2^{2n-1}}{\pi^{2L}}(2L+1)R^{2L+1} \tag{3.7}$$

$$DR_L = E^2/\varepsilon_L^2 = \frac{3\cdot 2^{2n}}{\pi^{2L}}(2L+1)R^{2L+1} \tag{3.8}$$

$$SNR(dB) = 10\lg 3+10(2n-1)\lg 2+10\lg(2L+1)+10(2L+1)\lg R-20L\lg\pi \tag{3.9}$$

From above deductions, increasing the modulator order *L* can increase the in-band SNR. When the order L is fixed, doubling the over-sampling ratio *R* will increase the SNR a value of 3(2*L*+1).

If the quantizer inside the modulator is multi-bit (n>2), the SNR can be improved by 6dB with one more bit increase in quantizer.

In practice, the modulator's order *L* cannot be increased without limit for it would introduce instability and cause the modulator to oscillate. Usually, *L* is less than 3 to make sure the stability of the modulator.

3.3 **Linear Model of Delta-Sigma Modulator**

The above deductions are based on the linear model of the delta-sigma modulator. The question remains that under what condition does the linear model of the delta-sigma modulator holds. The function of the quantizer inside a delta-sigma modulator is to

truncate its input into quantized signal which represent the input signal. The quantization process is an inherently non-linear operation and introduces errors to the conversion. In order to make the analysis tractable, the quantizer is often linearized by using an input-independent additive white noise model.

In this white noise model, a number of assumptions are traditionally made on the error process and its statistics. They follow:

1. The quantization error sequence e[n] is statistically independent of the input sequence.

2. The Probability Density Function (PDF) of e[n] is uniform over the range of half the bin width.

3. The random variables of the error process are uncorrelated.

If all the above assumptions hold, the linear model of delta-sigma modulator holds.

In order to get the delta-sigma modulator which is capable of complying with the signal-independent white noise assumption, the characteristics of the quantization error e[n] introduced inside the delta-sigma modulator is studied. Most of all, the input to the delta-sigma modulator is preferred to be DC so that math equations of the e[n] and its statistical performance can be derived.

On the other hand, MASH type delta-sigma modulator (Figure 3-2 [23]) is a widely used for its easy implementation and stability. A rigorous analysis of MASH delta-sigma modulators with DC input and initial values of each accumulator have been proposed in [15]. It mainly examines the statistics of the quantizer error sequences.

First of all, the quantization error from different stage is derived:

$$e_l[n]=\frac{1}{2}-\left\langle\frac{V_{l,0}}{2b}+\sum_{Kl=0}^{n-1}\left(\frac{V_{l-1,0}}{2b}+\cdots+\sum_{K_2=0}^{K_3-1}\left(\frac{V_{1,0}}{2b}+\sum_{Kl=0}^{K_2-1}\beta\right)\right)\right\rangle \tag{3.10}$$

In (3.10), l represents MASH type modulator's order. $\pm b$ is the output levels of the single-bit (or binary) quantizer. $V_{i,0}(i=1\cdots l)$ are the initial values in each stage's accumulator. β is the normalized the DC input to the delta-sigma modulator.

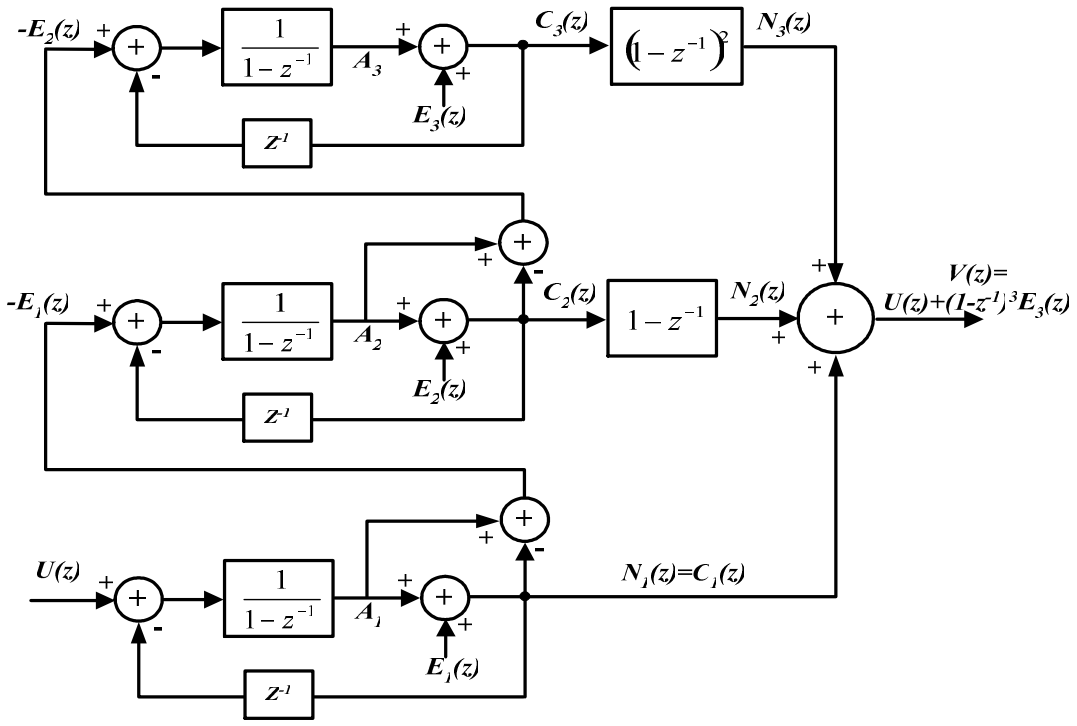


Figure 3-2 MASH delta-sigma modulator with quantization noise e[n] at each stage.

Assume $e_l[n]$ is a stationary ergodic random process, its sample mean, average power and auto-correlation are evaluated below.

$$\text{Sample mean: } M\left(\hat{x}\right)=\lim_{N\to\infty}\frac{1}{N}\sum_{n=0}^{N-1}\hat{x}[n] \tag{3.11}$$

$$\text{Average power: } M\left(\hat{x}^2\right)=\lim_{N\to\infty}\frac{1}{N}\sum_{n=0}^{N-1}\hat{x}^2[n] \tag{3.12}$$

$$\text{Auto-correlation: } r_{\hat{x}}(r)=\lim_{N\to\infty}\frac{1}{N}\sum_{n=0}^{N-1}\hat{x}[n]\,\hat{x}[n+r] \tag{3.13}$$

Let the $V_{1,0}$ be an irrational number, the following results are important. [15]

(1) For modulator's order l > 2, the sample mean and average power of the binary quantizer error from the last stage are :

$$M(\varepsilon_l) = 0 \tag{3.14}$$

$$M(\varepsilon_l^{\,2}) = \frac{1}{12} \tag{3.15}$$

The autocorrelation is different from second order MASH with higher order MASH type modulators. For second order MASH type, the autocorrelation of the binary quantizer error from the second stage is found:

$$r_{\varepsilon 2}(r) = \begin{cases} \frac{1}{12}, r = 0 \\ \frac{1}{2\pi^2\mu^2}\left(\frac{1}{4}(\gamma - \pi)^2 - \frac{1}{12}\pi^2\right), r \neq 0 \end{cases} \tag{3.16}$$

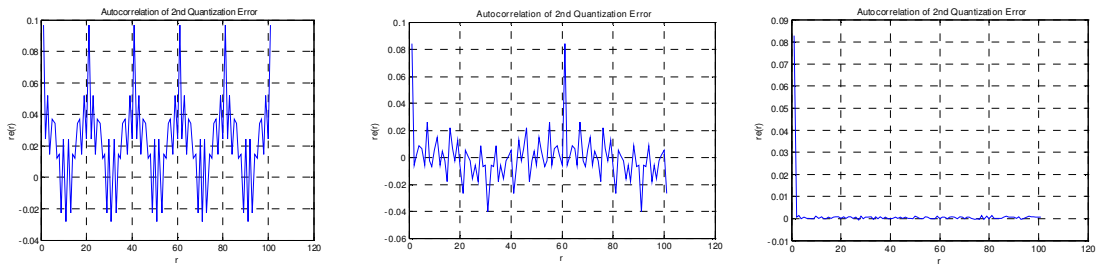
(2) For third or higher order MASH type, the autocorrelation of the binary quantizer error from the last stage is found:

$$r_{\varepsilon l}(r) = \begin{cases} \frac{1}{12}, r = 0 \\ 0, r \neq 0 \end{cases} \tag{3.17}$$

From all the math equations, a conclusion is drawn that an irrational initial condition imposed in the 1st accumulator guarantees a linear white noise model for a third or higher order MASH delta-sigma modulator. The real implementation for the irrational number is based on the fact that a rational number, which is represented by a ratio of two relatively prime integer numbers, will tend to an irrational number when the number in the denominator is made very large. Usually, it is desirable to utilize the minimum odd number "1" in the first accumulator as the initial seed. This is accomplished by setting "1" LSB in the first accumulator each time the circuit is reset [15].

(3) For second order MASH type delta-sigma modulator, the autocorrelation is not zero and the linear model does not hold. However, dithering can be added to the LSB of the first accumulator to dither the autocorrelation effect in (3.16) and thus to make its linear model hold.

We used a second order MASH type delta-sigma modulator to test initial seed and dithering effect. We set L=30, Fr=3. First initial values of all accumulators in the modulator are set to be zero and the autocorrelation of the second MASH type modulator's quantization error is shown in Figure 3-3.



(a) Normal autocorrelation of quantization error

(b) With initial seed '1' added to the 1st accumulator

(c) With dithering added to the LSB of 1st accumulator

Figure 3-3 Autocorrelation of second order MASH type modulator's quantization error.

First initial values of all accumulators in the modulator are set to be zero and the autocorrelation of the second order MASH type modulator's quantization error is shown in Figure 3-3 (a). Next an initial seed "1" is added to the first accumulator in the modulator and the result is shown in Figure 3-3 (b). There're some improvements in the quantization error autocorrelation in (b) but it's still not a white noise. So a 16-bit pseudo random series is added to dither the LSB of the 1st accumulator and the result is shown in (c).This is almost a white noise and the linear model of delta-sigma modulator holds. For higher order delta-sigma modulator, the results are even better.

In this section, a MASH type delta-sigma modulator with DC input is studied and the quantization errors for its quantizers are examined using the math autocorrelation to verify the effectiveness of linear model of delta-sigma modulator. Modulator with order higher than 3 satisfies the linear white noise model. Lower order modulator needs dithering to approach the linear model. The linear model of delta-sigma modulator is the basis of its use in DDS in next section.

3.4 **Delta-sigma Modulation in DDS**

3.4.1 **Introduction**

As illustrated in Figure 3-4, a conventional direct digital synthesizer (DDS) consists of a numerically controlled oscillator (NCO) and a digital-to-analog converter (DAC). The NCO further includes a phase accumulator and a lookup table that transforms digital phase information to digital amplitude information. The DDS output spectrum contains spurious components mainly due to phase word truncation before the ROM lookup table. The periodic truncated phase error sequence causes spurs in its output spectrum. Delta-sigma modulators have been implemented in both frequency [16] and phase [17] domains in DDS to reduce the spurs, their noise shaping effects and design tradeoffs have been compared [18]. In this section, we go details of comparison and implementation of eight different delta-sigma modulators including MASH, feed-forward, feedback and error feedback in both frequency and phase domains in a CMOS DDS chip. The noise shaping effects, in-band SFDR, SINAD, operation speeds, area and stability are compared according to measured results.

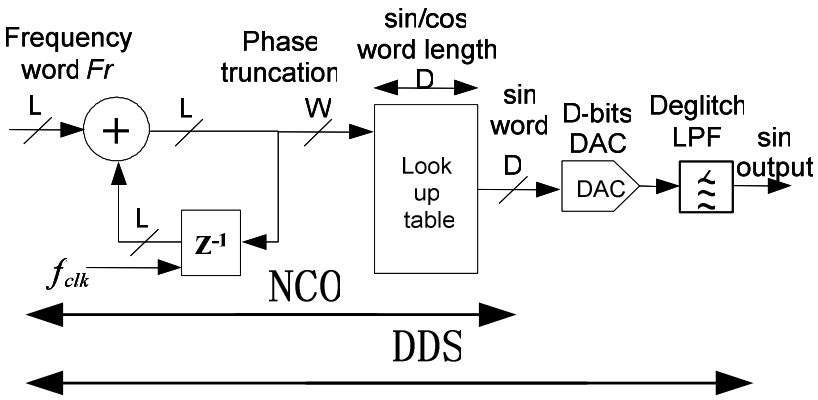


Figure 3-4 DDS with NCO and DAC.

3.4.2 **Phase Domain Modulation**

In an ideal DDS without phase truncation ($L = W$) and with infinite amplitude precision, the output sequence of the NCO is given by

$$S(n) = \sin\left(2\pi \frac{Fr}{2^L} n\right) \tag{3.18}$$

where F_r is the input frequency control word with L bits and W is the length of phase word to address the accumulator.

In order to reduce the ROM size, one can either truncate the phase accumulator output from L bits to W bits. With a phase word truncation, we define B to be the number of bits truncated such that L-W=B. The output of the DDS becomes

$$S_t(n) = \sin\left(2\pi \frac{2^B}{2^L}\left[\frac{Fr}{2^B} n\right]\right) \tag{3.19}$$

where the operator [] represents truncation to integer values. Equation (3.19) can alternatively be expressed as

$$S_t(n) = \sin\left(\frac{2\pi}{2^L}\left[Fr \cdot n - \varepsilon_p(n)\right]\right) \tag{3.20}$$

where $\varepsilon_p(n)$ represents the phase error sequence. Applying trigonometric identities, Equation (3.20) can be rewritten as

$$S_t(n) = \sin\left(2\pi\frac{Fr\cdot n}{2^L}\right)\cos\left(2\pi\frac{\varepsilon_p(n)}{2^L}\right) - \cos\left(2\pi\frac{Fr\cdot n}{2^L}\right)\sin\left(2\pi\frac{\varepsilon_p(n)}{2^L}\right) \tag{3.21}$$

Assuming $\varepsilon_p(n) << 2^L$, we get

$$S_t(n) = \sin\left(2\pi\frac{Fr\cdot n}{2^L}\right) - 2\pi\frac{\varepsilon_p(n)}{2^L}\cdot\cos\left(2\pi\frac{Fr\cdot n}{2^L}\right) \tag{3.22}$$

Therefore, the output spectrum of the DDS is composed of a sine wave at the desired output frequency corrupted by the cosine modulated harmonics of the phase error $\varepsilon_p(n)$. The periodic sequence $\varepsilon_p(n)$ can be expressed as Fourier series. Thus, the conventional DDS with phase truncation ends up with spurs at different places in its output spectrum.

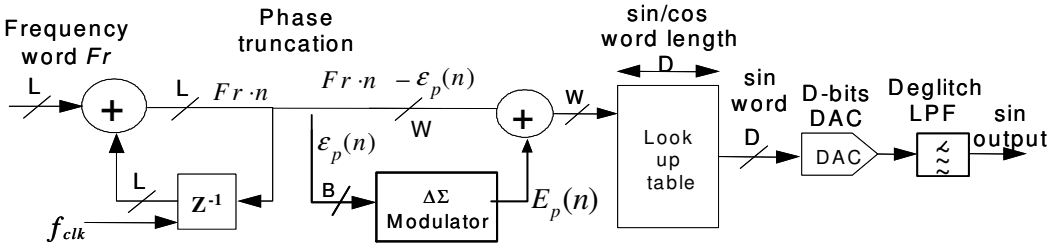


Figure 3-5 Phase domain delta-sigma modulation in DDS.

In order to reduce spurs due to phase truncation, we apply delta-sigma modulation in phase domain. There are two ways of adding delta-sigma modulator in phase domain. One is shown in Figure 3-5. The phase word $Fr\cdot n$ after the accumulator is truncated into $Fr\cdot n - \varepsilon_p(n)$ (W bits) and $\varepsilon_p(n)$ (B bits). The phase error $\varepsilon_p(n)$ is fed into a delta-sigma modulator. The modulator's output $E_p(n)$ is expressed as a single-bit or multi-bit word and added back to the truncated phase.

Using a linear model for delta-sigma modulators, we get

$$E_p(z) = \varepsilon_p(z) + Q(z)(1-z^{-1})^k = \varepsilon_p(z) + Noise(z) \tag{3.23}$$

where $Q(z)$ is the quantization noise from the quantizer inside the modulator and k is the order of the modulator. We can rewrite (3.23) as

$$E_p(n) = \varepsilon_p(n) + Noise(n) \tag{3.24}$$

where the modulated quantization noise, $Noise(n)$, is the inverse Z-transform of $Q(z)(1-z^{-1})^k$.

The DDS output is thus given by

$$\begin{aligned} S_t(n) &= \sin\left(\frac{2\pi}{2^L}\left[Fr \cdot n - \varepsilon_p(n) + Ep(n)\right]\right) \\ &= \sin\left(\frac{2\pi}{2^L}\left(Fr \cdot n + Noise(n)\right)\right) \end{aligned} \tag{3.25}$$

Assuming $Noise(n) << 2^L$, we obtain

$$S_t(n) = \sin\left(2\pi \frac{Fr \cdot n}{2^L}\right) - 2\pi \frac{Noise(n)}{2^L} \cdot \cos\left(2\pi \frac{Fr \cdot n}{2^L}\right) \tag{3.26}$$

The second type of delta-sigma modulation in phase domain is phase error feedback as shown in Figure 3-6:

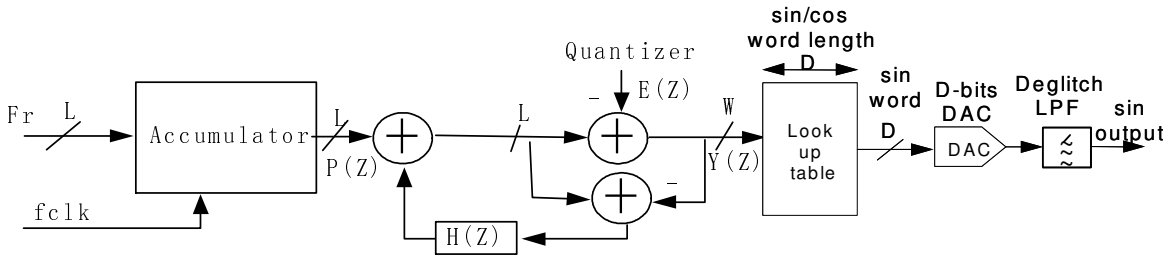


Figure 3-6 Error feedback modulator in phase domain.

From the linear model of error feedback delta-sigma modulator shown in Figure3-6, we can write the modulator's transfer function:

$$Y(z) = P(z) + (1 - H(z))E(z) \tag{3.27}$$

Error feedback delta-sigma modulator actually has a single bit quantizer and the output $Y(z)$ represents the input $P(z)$ added with the modulated quantization noise $(1-H(z))E(z)$. The order of the modulator can be changed with different transfer function $H(z)$.

In DDS application, the input *L*-bit phase is truncated to *W*-bit. It is a single bit quantization except that the remaining is *W*-bit in word length.

Shown in Figure 3-6, the error feedback modulator's input is the phase information $Fr \cdot n$ but not the phase error $\varepsilon_p(n)$ as the case in the type phase domain modulation shown in figure3-5.

The modulator's output is $Fr \cdot n + Noise(n)$ .where *Noise(n)* is the modulated quantization noise which has high frequency shaping effect. In this way we can get DDS's output S_t(n) that is same as (3.25) and (3.26).

$$S_t(n) = \sin\left(\frac{2\pi}{2^L}(Fr \cdot n + Noise(n))\right)$$
$$= \sin\left(2\pi\frac{Fr \cdot n}{2^L}\right) - 2\pi\frac{Noise(n)}{2^L} \cdot \cos\left(2\pi\frac{Fr \cdot n}{2^L}\right) \quad (3.28)$$

In equation (3.28), the modulated quantization *Noise(n)* takes place of the original phase error $\varepsilon_p(n)$. Thus, spurs introduced by the phase truncation are reduced, and modulated quantization noise with high frequency shaping shows up in the spectrum. Delta-sigma modulators with different noise transfer functions thus lead to different DDS output spectra.

3.4.3 **Frequency Domain Modulation**

Delta-sigma modulation can also be implemented in the frequency domain of a DDS. For frequency word truncation, the frequency word *Fr* is truncated from *L* bits to *W* bits

before the phase accumulator. The discarded frequency bits $B=L-W$, and the output sequence of the DDS ROM become

$$\begin{aligned} S(n) &= \sin\left(2\pi \frac{Fr}{2^L} n\right) = \sin\left(2\pi \frac{(Fr/2^B)}{2^W} \cdot n\right) \\ &= \sin\left(2^{1-W}\pi\left(\left[\frac{Fr}{2^B}\right] \cdot n + \left(Fr - \left[\frac{Fr}{2^B}\right] \cdot 2^B\right) \cdot n \Big/ \left(2^B\right)\right)\right) \\ &= \sin\left(2\pi\left(\left[\frac{Fr}{2^B}\right] n + pe \cdot n\right) \Big/ 2^W\right) \end{aligned} \tag{3.29}$$

where the operator [] represents truncation to an integer and the frequency error due to frequency word truncation is

$$\left(\left(Fr - \left[\frac{Fr}{2^B}\right] \cdot 2^B\right) \Big/ 2^B\right) = pe \tag{3.30}$$

As shown in (3.29), the phase accumulator size can be reduced to W bits if the input frequency word Fr is truncated to $[Fr/2^B]$.

The frequency word truncation will also cause a phase error $(pe \cdot n)$ which is periodic in nature and thus leads to spurs at the DDS output. If the input word $Fr \leq 2^B$, then $[Fr/2^B] = 0$, there will be no DDS output due to frequency word truncation. However, to avoid losing frequency information, the constant frequency error pe needs to be modulated and added back to the accumulator.

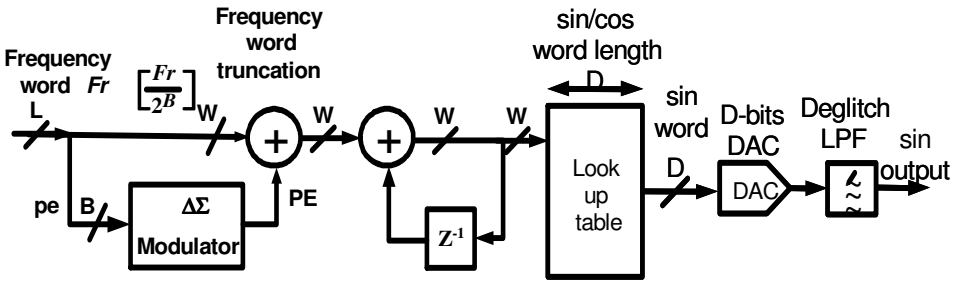


Figure 3-7 Proposed DDS with frequency domain delta-sigma modulation.

As shown in Figure 3-7, the modulated frequency error pe is added back to the truncated Fr that is represented by $[Fr/2^B]$. Note that in Figure 3-7, the delta-sigma modulator's input pe is constant, which benefits the modulator design with improved stability, input range and speed. The noise shaped frequency error is thus a series of numbers and is given by

$$PE(z) = pe(z) + Q(z)(1 - z^{-3}) = pe(z) + Noise(z) \tag{3.31}$$

where $Q(z)$ is the quantization noise introduced by the delta-sigma modulator.

With the frequency domain delta-sigma modulation, the DDS output is given by

$$\begin{aligned} S_t(n) &= \sin\ 2\pi\left(\left[\frac{Fr}{2^B}\right]n + PE\ (n)\cdot n\right)\Big/2^W \\ &= \sin\ 2\pi\left(\left[\frac{Fr}{2^B}\right]n + pe\ \cdot n + Noise\ \ (n)\cdot n\right)\Big/2^W \\ &\approx \sin\left(2\pi\ \frac{Fr\ \cdot n}{2^L}\right) - \cos\left(2\pi\ \frac{Fr\ \cdot n}{2^L}\right)\cdot\left(2\pi\ \frac{Noise\ \ (n)\cdot n}{2^W}\right) \end{aligned} \tag{3.32}$$

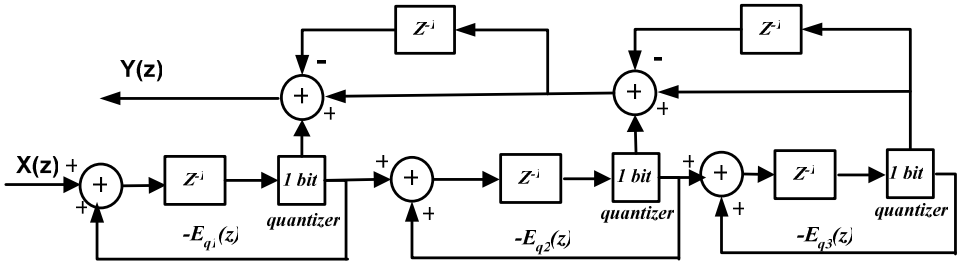
Thus, the DDS output spectrum is composed of a sine wave at the desired output frequency and a cosine wave that is modulated by the quantization noise shaped by the delta-sigma modulator. Based on the linear model of a delta-sigma modulator, the periodic phase error due to frequency word truncation is reduced. Instead, the modulated quantization noise from the modulator occurs at the DDS output.

3.4.4 **Comparison of Measured NCO Output Spectra for Various Delta-sigma Modulators**

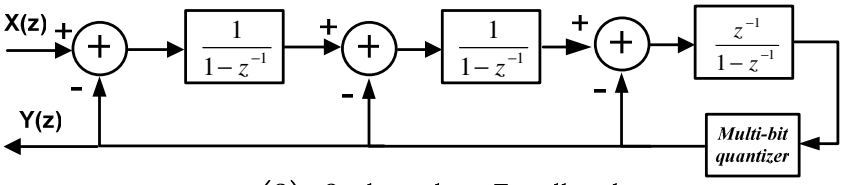
Although various delta-sigma modulators in both the phase domain and frequency domain can move the spurs and quantization noise to a high frequency band, their performances on noise shaping are different. To compare various delta-sigma modulator performances, we consider factors such as the modulator topology, the order of the modulator, the modulator input, the in-band spurious tones, the number of quantizer bits, the modulator speed and area, etc. We first implemented an NCO with several types of delta-sigma modulators in both frequency and phase domain in FPGA as shown in Figure 3-8. The NCO output is captured into a PC for analysis. First we analyze the output characteristics such as the spurious-free-dynamic-range (SFDR), defined as the ratio between the fundamental signal and the highest spurs and the signal-to-noise-and-distortion ratio (SINAD) shown in (3.33).

$$SINAD = 20 \cdot \log\left(\frac{Signal}{SUM\ (Noise + Harmonics)} \right) \tag{3.33}$$

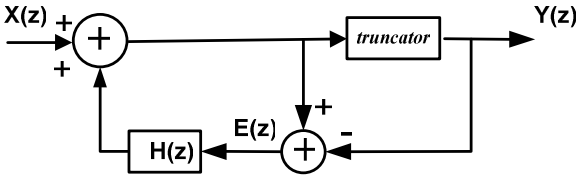
The oversampling ratio (OSR) of the delta-sigma modulator is chosen as 64 and the band of interest is from zero to 1/64 of the clock frequency. The measured in-band SINAD and SFDR of the NCO output with various delta-sigma modulators are given in Figure 3-9. The measurements show that without delta-sigma modulation, direct phase truncation has a low SFDR and SINAD. With delta-sigma modulation, in-band SFDR and SINAD increase. In phase domain modulation, the phase error *pe* (*L*-*W* bits LSBs) has different repeating periods with respect to different Fr, which leads to a varying the input to the modulator. In contrast, frequency domain modulators have constant dc input.



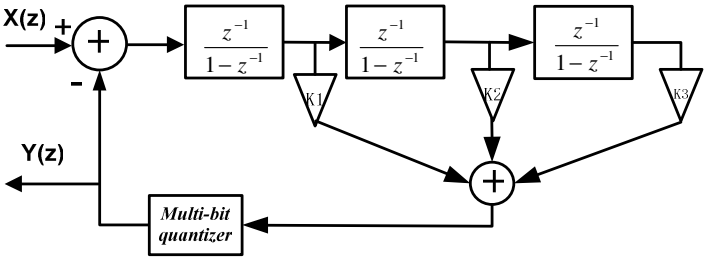
(1) MASH111



(2) 3rd order Feedback



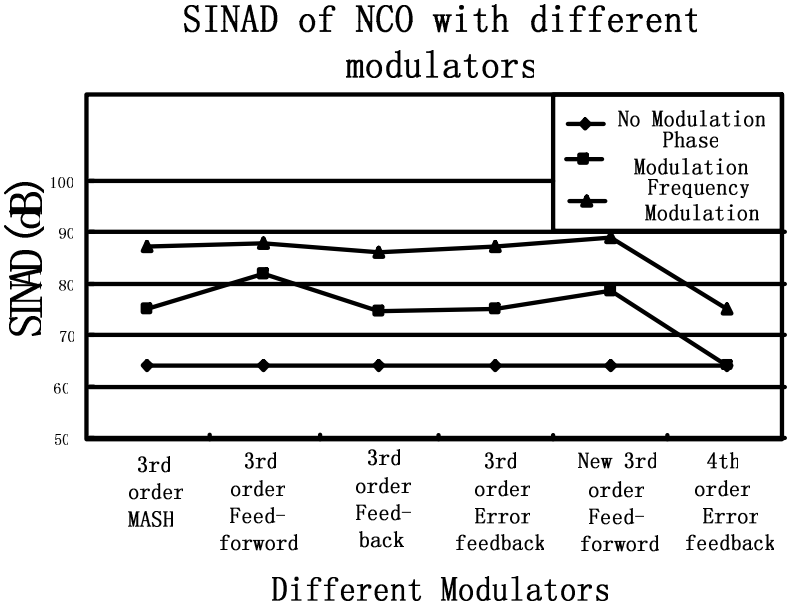
(3) Error Feedback, H(z) determines the order



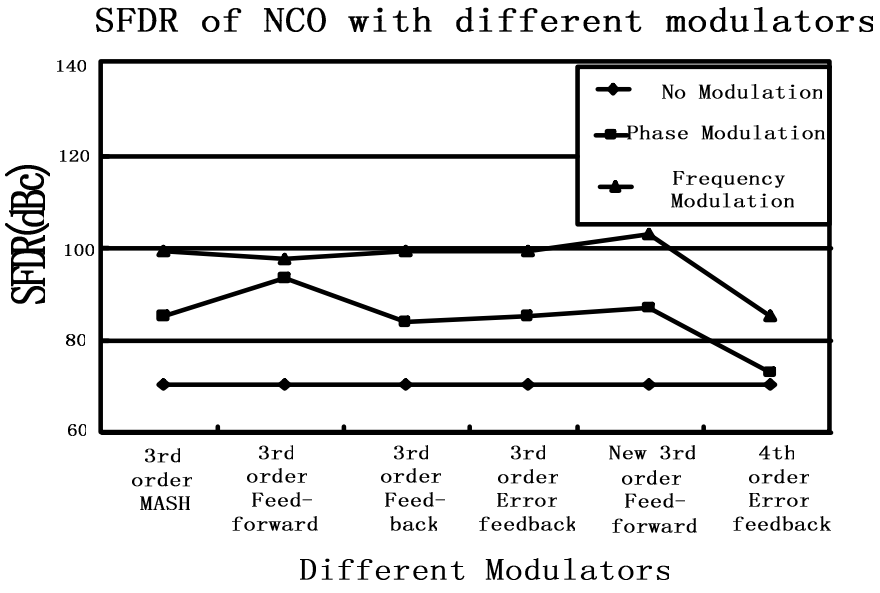
(4) 3rd order feedforward

Figure 3-8 Four types delta-sigma modulators implemented in a DDS and NCO for comparison.

As a result, the frequency domain delta-sigma modulation has higher SFDR and SINAD than phase domain. Although using a high-order delta-sigma modulator results in sharper noise shaping effect, it suffers from degraded SFDR and SINAD.



(a) SINAD of NCO with different modulators



(b) SFDR of NCO with different modulators

Figure 3-9 Measured in-band SINAD and SFDR of the NCO output with various delta-sigma modulators in frequency and phase domains.

Since the modulated quantization noise dominates the DDS output spectrum, its noise transfer function *He(Z)* can greatly affect the DDS output. We implemented four types of delta-sigma modulators, i.e., MASH, feedforward, feedback and error feedback as shown

in Figure 3-8. MASH, feedback and error feedback type delta-sigma modulators have the same noise transfer function of $He(Z)=(1-Z^{-1})^k$, where k is the order of the modulator. MASH-111 has three 1-bit quantizers, while the feedback type modulator has a multi-bit quantizer and the error feedback delta-sigma modulator has one single-bit quantizer. A feedforward type delta-sigma modulator is first presented in the frequency domain in [16]. It's a second order feedforward type with a multi-bit quantizer. The modulator's order can be increased by adding more accumulators in cascade and different noise transfer functions can be obtained by varying the feedforward coefficients k_1, k_2, k_3. We propose a *feedforward2* delta-sigma modulator with coefficients of $k_1 = 2.5$, $k_2 = 2.5$, $k_3 = 1$.

Figure 3-10 compares the noise transfer function of MASH, *feedforward1* [19], and the proposed *feedforward2* modulator. It's clear that MASH has much sharper noise shaping effect in-band. But it has high out-of-band noise that requires a high-order LPF for noise rejection. The *feedforward2* modulator has lower in-band noise compared with existing *feedforward1* modulator and has flat out-of-band noise compared with MASH type.

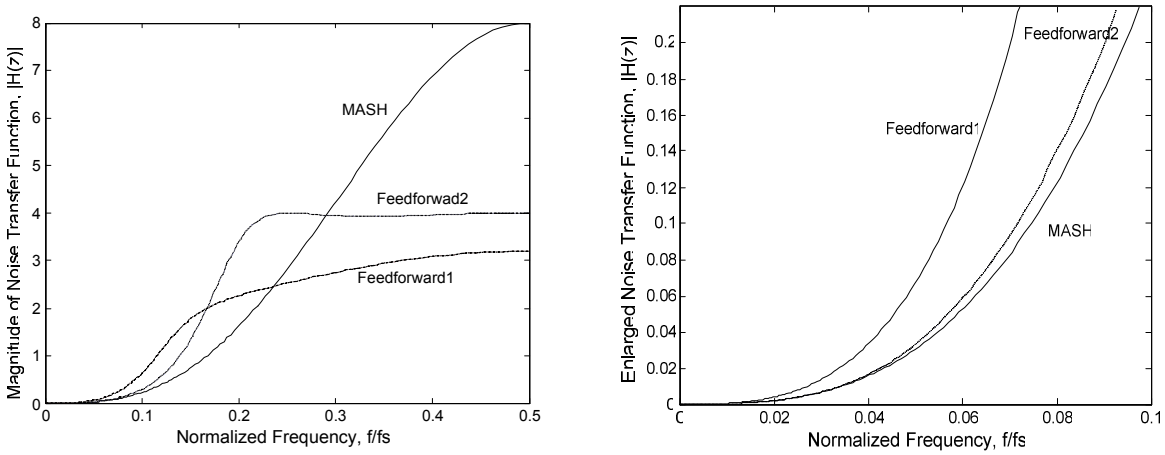
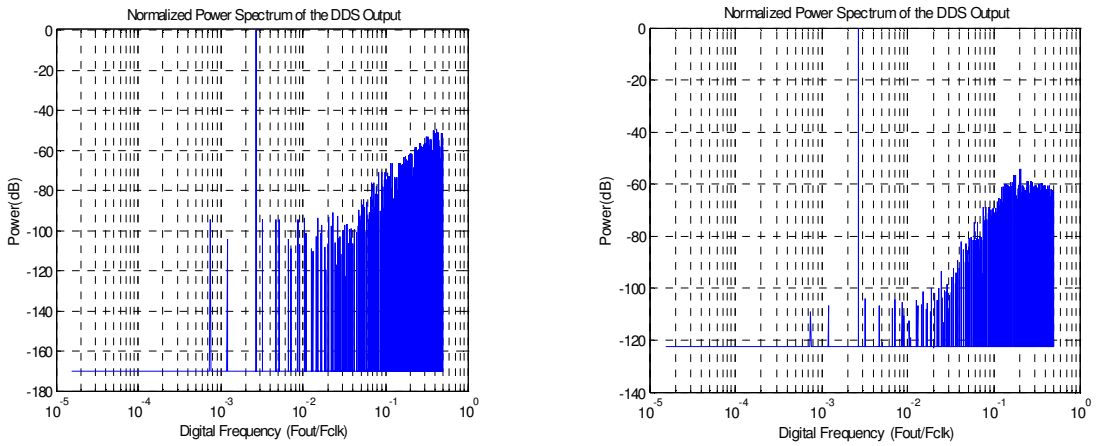


Figure 3-10 simulated noise transfer function of MASH and feedforward delta-sigma modulators.

Figure 3-11 gives the measured NCO output spectrum for two types of delta-sigma modulators. The measured spectra of the two delta-sigma modulators are almost identical with the modulated noise. Multi-bit quantizer inside the modulator can make feedback signal match input signal more accurately and make the quantization noise more random, which better fits the liner model for delta-sigma modulators.

Although feedforward modulator can increase in-band SINAD by a few dB, it has drawback of instability. In contrast, a MASH type modulator is good for its high speed, sharp slope and full input dynamic range, and it is always stable. The drawback of a MASH modulator lies on its fixed number of output bits. The error feedback has the same noise transfer function as that of MASH except for its lower speed. However, error feedback modulator can flexibly choose the number of output bits. Feedback modulator also has the same noise transfer function as MASH and it also has an advantage of a multi-bit quantizer, but it has stability problem.



(a) NCO output spectrum with 3rd order MASH type delta-sigma modulation in frequency domain(1-bit quantizer)

(b) NCO output spectrum with frequency domain 3rd order *feedforward2* delta-sigma modulation (multi-bit quantizer)

Figure 3-11 Comparison of measured NCO output spectrum with different noise shaping effects.

The proposed *feedforward2* delta-sigma modulator is good in both in-band and out-of-band performances, but its implementation requires more hardware and its speed is lower.

3.4.5 **Implementation of DDS with Various Delta-sigma Modulators in 0.35μm CMOS Technology**

To compare the DDS performance with various delta-sigma modulations, we designed delta-sigma modulators including MASH1-1-1, 3rd order feedforward, feedback and error feedback delta-sigma modulators and error feedback delta-sigma modulator as shown in Figure 3-8 in both frequency and phase domains. Different delta-sigma modulators can be selected individually while other delta-sigma modulators are turned off.

The proposed DDS with frequency domain and phase domain delta-sigma modulator was implemented in 0.35μm CMOS technology with two poly and four metal layers. A 16-bit accumulator is designed, and 8 phase bits are used for addressing the look-up ROM. The 12-bit current steering DAC is integrated to convert the ROM output to an analog signal. For 12-bit amplitude resolution in a conventional DDS without a delta-sigma modulator, at least 12 phase bits should be used, which requires a look-up ROM with 2^{12}x12 bits. The use of a delta-sigma noise shaper effectively reduces the required number of phase bits. Thus, we use only 8 phase bits to address the ROM, which reduces the ROM size by a factor of 2^4 or 16 times compared to that of a conventional DDS without a delta-sigma modulator.

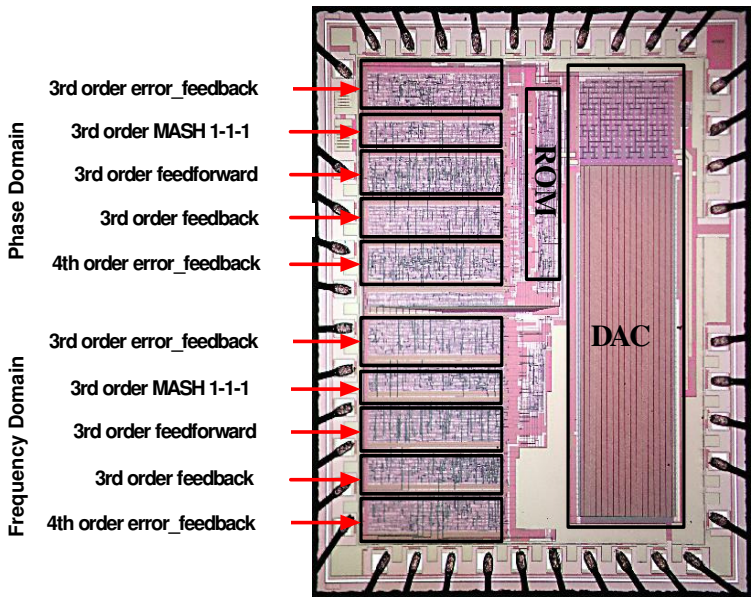
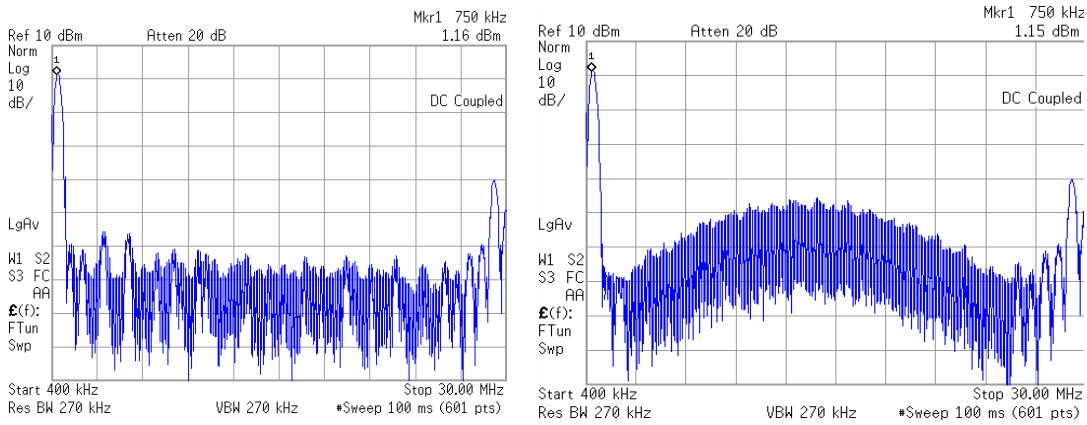


Figure 3-12 Die photo of the CMOS DDS prototype chip with various delta-sigma modulators in frequency and phase domain.

The die photo of the fabricated CMOS delta-sigma DDS prototype chip is shown in Figure 3-12. The total die area is 2x2.5mm^2, in which the DDS active core area is 1.7 x 2.1mm^2 including the DAC, and the rest of the die area is used for pads and ESD diodes. The 16-bit phase accumulator and ten delta-sigma modulators occupy 0.7x2.1mm^2 die area. The 2^8x12-bit ROM occupies only 0.1x0.8mm^2, which would be 16 times larger without the delta-sigma noise shaper. In a conventional DDS, the ROM normally takes the majority of the die area, whereas the ROM takes only a small portion of the total area in this DDS implementation, which clearly demonstrates the advantage of using delta-sigma noise shaping in DDS designs. The measured DDS output spectra with and without delta-sigma modulators are shown in Figure 3-13(a). It's clear that the in-band spurs shown in figure3-13(a) are reduced in Figure 3-13(b).



(a) without delta-sigma modulator

(b) with frequency domain 3rd order MASH delta-sigma modulator

Figure 3-13 Comparison of the measured output spectra for (a) conventional DDS without delta-sigma modulation and (b) proposed DDS with frequency domain delta-sigma modulation, f_o=750KHz, F_{clk}=30MHz.

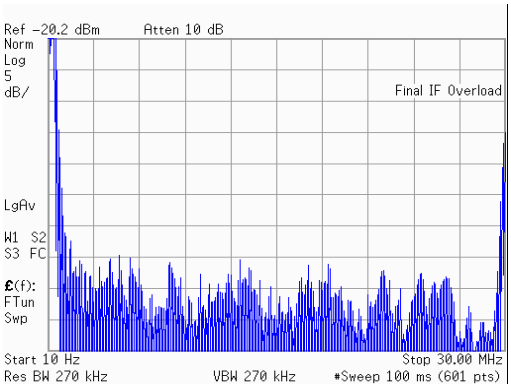
We have implemented various delta-sigma modulators in both frequency and phase domains in a CMOS DDS chip. The measured data demonstrates that frequency domain modulations have better SFDR and SINAD than their phase domain counterparts. Measurements results of output spectrum with different delta-sigma modulators either in frequency domain and phase domain are shown in Figure 3-14 ~Figure 3-18. For clear comparison , they all have a same frequency control word FCW=00000000,11111111. We have also compare factors such as input range, quantizer bits, speed and stability for different type of delta-sigma modulators (Table 3-1).

Table 3-1 Performance comparison of delta-sigma modulators in frequency and phase domains of DDS. (In-band SFDR and SINAD are measured from NCO)

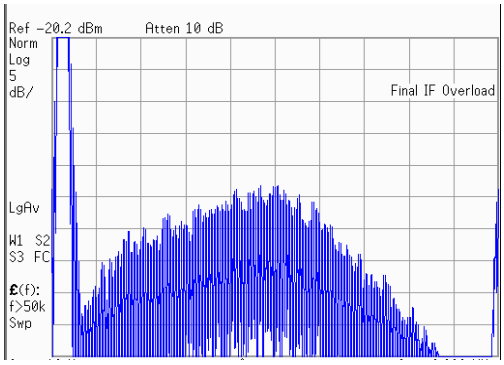
Frequency domain	High freq noise	No. of output bits	In-band SFDR (dBc)	In-band SINAD (dB)	Stability	Area (mm^2)	Speed (MHz)
3rd order MASH 111	poor	3	99.5	87.23	*ABSOLUTELY STABLE*	*0.112*	*180*
3rd order Feedback	fair	≥ 3	99.4	86.11	*FAIR*	*0.126*	*140*
3rd order Feedforward	good	≥ 3	103	89.03	*POOR*	*0.161*	*150*
3rd order EF	poor	≥ 3	99.5	87.23	*GOOD*	*0.147*	*140*
4th order EF	poor	≥ 4	85.4	75.15	*GOOD*	*0.148*	*160*
Phase domain							
3rd order MASH 111	poor	3	85.4	75.15	*ABSOLUTELY STABLE*	*0.112*	*180*
3rd order Feedback	fair	≥ 3	84	74.57	*FAIR*	*0.126*	*140*
3rd order Feedforward	good	≥ 3	87	78.59	*POOR*	*0.161*	*150*
3rd order EF	fair	≥ 3	85.4	75.15	*GOOD*	*0.147*	*140*
4th order EF	poor	≥ 4	73	64.10	*GOOD*	*0.148*	*160*

3.4.6 **Conclusions**

Mash 1-1-1 delta-sigma modulator in frequency domain provides a good noise shaping means for DDS application with optimal speed, stability and input dynamic range. Feed-forward delta-sigma modulator can provide both good in-band noise shaping and flat high frequency performance. Error-feedback takes advantage in its flexible output bit numbers.

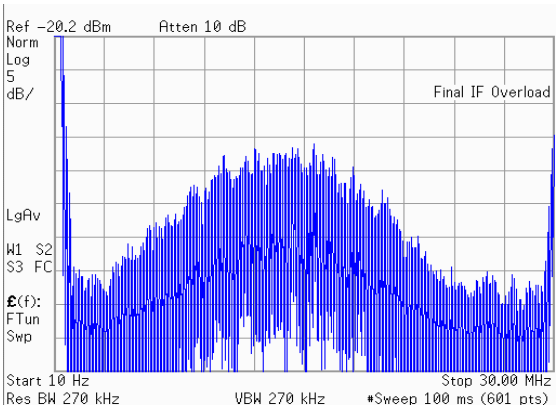


(a) Without modulation

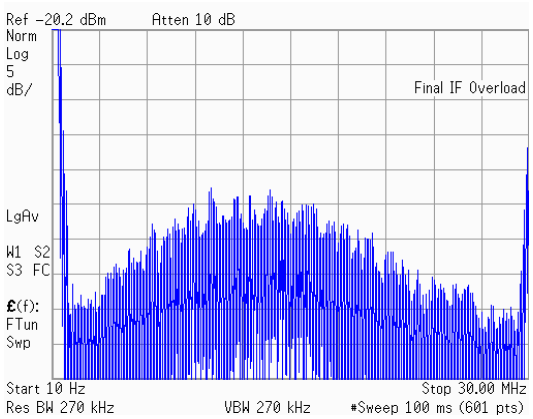


(b) Third order feedforward type delta-sigma modulation in phase domain

Figure 3-14 Measured DDS output spectra (FCW=00000000,11111111).

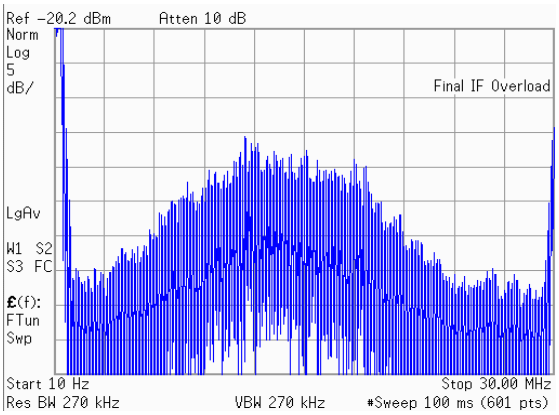


(a) Phase domain

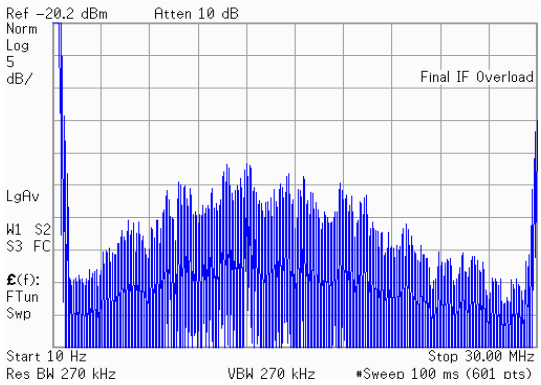


(b) Frequency domain

Figure 3-15 Measured DDS output spectra with third order MASH type delta-sigma modulation.

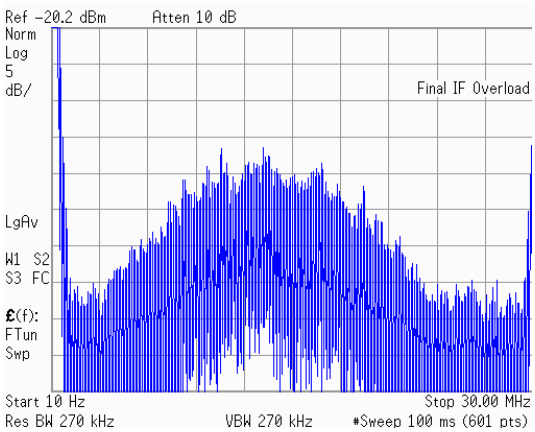


(a) Phase domain

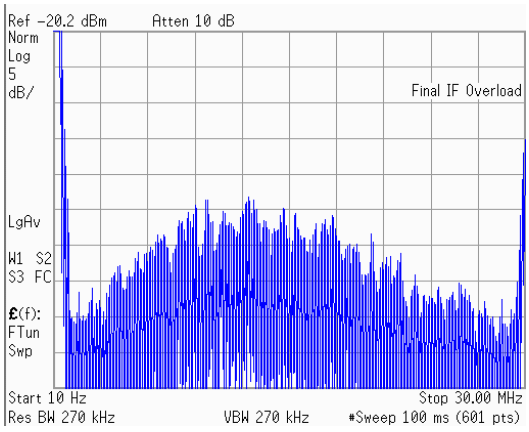


(b) Frequency domain

Figure 3-16 Measured DDS output spectra with third order feedback type delta-sigma modulation.

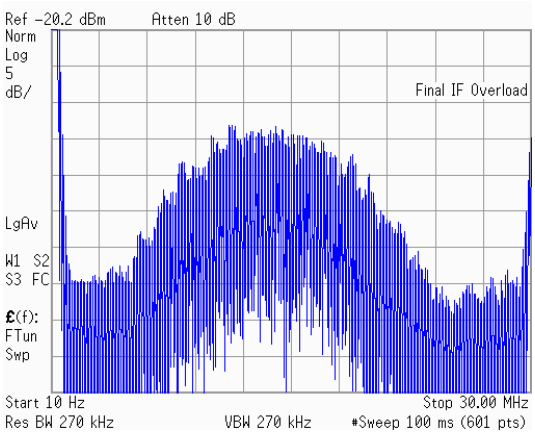


(a) Phase domain

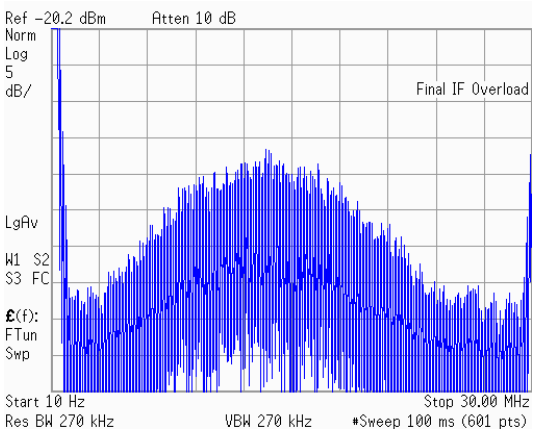


(b) Frequency domain

Figure 3-17 Measured DDS output spectra with third order error feedback type delta-sigma modulation.



(a) Phase domain



(b) Frequency domain

Figure 3-18 Measured DDS output spectra with fourth order error feedback type delta-sigma modulation.

CHAPTER 4 HIGH SPEED DDS DESIGN

4.1 Introduction

This chapter discusses the RF circuit design of high speed DDS basic building blocks such as current mode logics, pipelined and carry look-ahead phase accumulators, delta-sigma modulator and a nonlinear DAC that have been discussed in previous chapters. SiGe BiCMOS technology is adopted for its high speed and low noise performance.

4.2.SiGe BiCMOS

In contrast to conventional Si bipolar transistors, SiGe bipolar transistor [20] is formed by adding some germanium to its base. The SiGe compound in base has a narrower band-gap compared to the pure silicon one. The relatively large band gap in the emitter can be used to increase the potential barrier to holes that can be injected from the base back to the emitter. Therefore, the emitter doping is can be decreased which leads to the increase of the base-emitter width and hence to reduce the C_{je}. Meantime, the base doping can be increased which lead to reduction of base width and base-collector depletion region. All these changes bring to higher operating frequency f_T, higher gain, increased early voltage VA and lower base resistance r_b which are needed for RF circuit design.

4.3 **CML Digital Blocks**

Current mode logic (CML) has been employed in the high-speed digital systems for it very fast switching property. The circuit topology is composed of several single current switch pairs which are tied together either in series or parallel with a common current source at the bottom. A current switch pair consists of two bipolar transistors with common emitter connected together. The digital signal in CML circuits is differential and switches on and off each current switch pair at one time. The current is flowing through only one branch from power (VDD) to ground. Figure 4-1 shows a four level 3-input 'AND' circuit. One of the two resistors pulls down the output voltage from VDD to VDD-$I_{Bias}R_L$ when bias current flowing through it. The output differential swing is thus $2I_{Bias}R_L$ which many range from 100mv~400mv [21]. So the resistance of R_L mainly depends on the swing requirement when the bias current is determined.

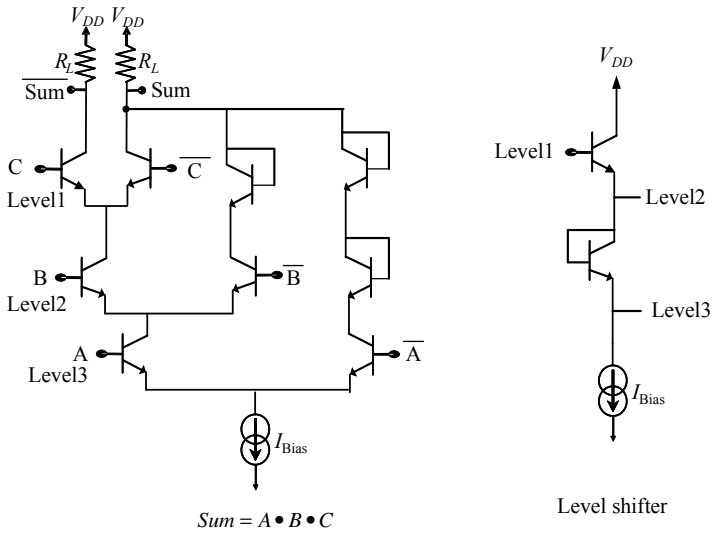


Figure 4-1 A four-level AND CML logic.

The four-level CML logic (with one current source level) has up to 3 different inputs levels and 3~4 current branches to realize complex combinational logic with less hardware

and power compared to ECL logics. The input level voltage of A, B, C under a 3.3V supply is 1.3V, 2.2V and 3.1V so as to make sure the transistors not work in saturation mode. Additional transistors are connected as diode to let each current branch have same voltage drop at each input level. It is necessary for high speed SiGe bipolar transistor has a relatively low BV_{CEO}. A level shifter made of emitter follower buffer to shift down the output voltage level 1 to level2 or level3 to the next stage CML logics.

CML circuit's speed is mainly determined by its propagation delay which is contributed by the base-emitter capacitance, the Miller effect on the intrinsic base-collector capacitance, the inner collector node parasitic such as the collector-substrate capacitance C_s and parasitic resistance r_c and of course the load capacitance C_L and resistance R_L at the output node. SiGe technology has taken its advantages in reducing the parasitics such as r_b , C_{je} and so to C_π and high current gain. Transistor's unity current gain-bandwidth product f_T is the frequency at which the short-circuit current gain β is equal to 1.

$$f_T = \frac{g_m}{2\pi(c_\pi + c_u)} \tag{4.1}$$

In order to achieve maximum speed, it's a good decision to make the bias current as large as possible by setting it to peak f_T. Next, simulations are made to get tradeoff between power consumption and the minimum propagation delay of the CML circuits. For each 3-input AND circuit with minimum transistor size in 0.18um and 0.12um, the bias current is biased at near 70% to its peak f_T. With the same AND circuit as load, the propagation delays is 10ps and 5ps.

When the emitter follower stage inside the level shifter is running at very high speed,

its output impedance would increase with increasing frequency and appear to be inductive [22].

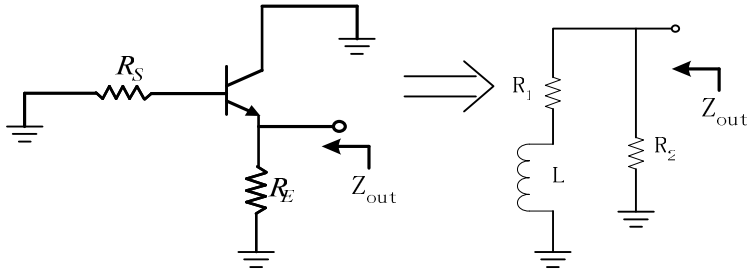


Figure 4-2 Output resistance of emitter follower at high bias and high frequency.

For the quite large DC biasing condition: $\frac{1}{gm} < R_s + r_b$

The output impedance can be approximated by the equivalent circuit of Figure 4-2, where:

$$R_1 = \frac{1}{gm} + \frac{Rs + r_b}{\beta_0} \tag{4.2}$$

$$R_2 = R_s + r_b \tag{4.3}$$

$$L = \frac{1}{\omega_T}(R_s + r_b) \tag{4.4}$$

Because there are inductive components in the output resistance, when the level shifter is to drive the next stage with quite large capacitive load, it may cause peaking or instability in the overall circuit response as shown in Figure 4-3.

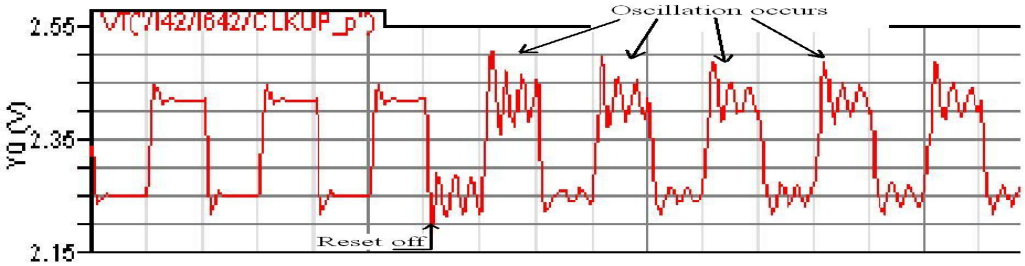


Figure 4-3 Oscillation caused by emitter followers inductive output.

The edge of the clock signal starts to oscillate when the reset is turn off and circuit begins to work. That's one reason normally the transistor with minimum size used. Meantime, we need to shrink the load capacitance as small as possible and thus try not let level shifter drive too much loads.

4.4 **Pipeline and Carry Look-Ahead Accumulators**

Accumulator is a major block in the DDS. Phase accumulator in DDS adds up a frequency control word FCW at each clock cycle and generates a phase word of a sine wave at the output. Therefore, accumulator output 0 refers phase 0 and output 2^L-1 refers 2π. The accumulator's size L determines the final output frequency resolution. The output frequency resolution doubles with one bit increase in accumulator's length. As discussed in Chapter 2, the phase bits L is truncated to W bits before it goes to ROM or nonlinear DAC and this combined with FCW also determines the spurious spurs. With DAC output bits D, the truncated phase bits W which is connected to ROM determined the quantization noise floor. As a rule of thumb in practical applications, the number bits at the ROM input W should be bigger than or equal to D+2.

In high speed DDS design, the accumulator's speed, area and power consumption would influence the whole DDS performance. The speed is mainly limited by the critical path between the flip-flop registers.

4.4.1 **Pipeline Accumulator**

A pipeline accumulator is known for its highest speed. The delay is its critical path is dominated only by a full adder delay.

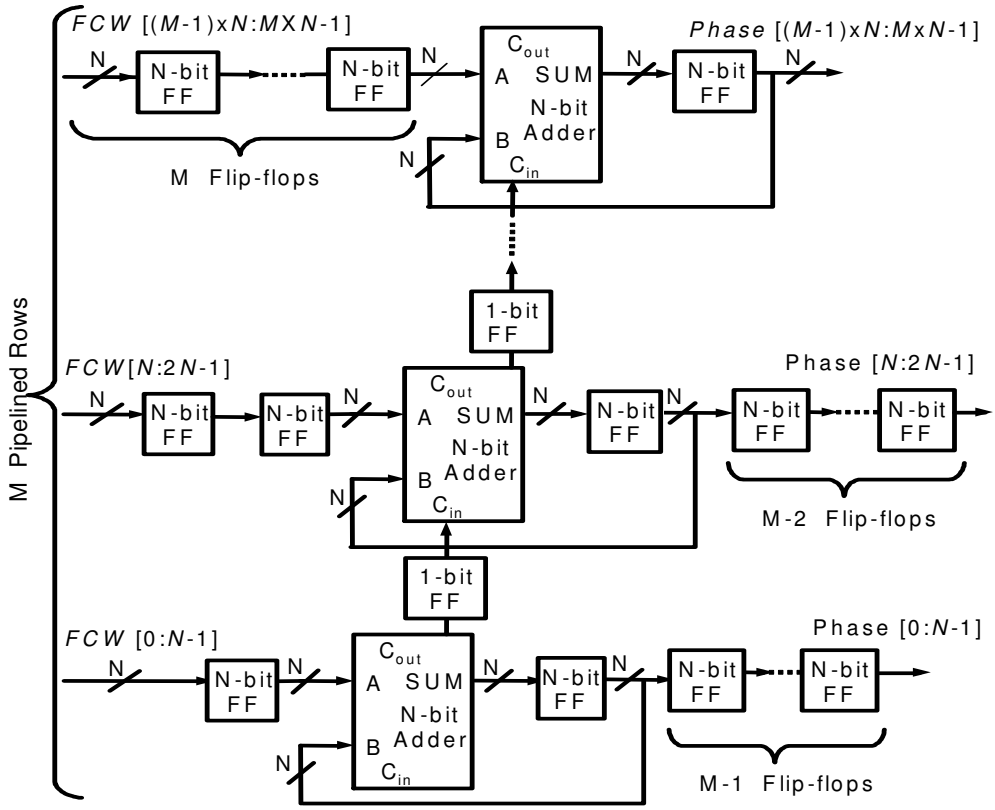


Figure 4-4 A generic architecture of an N×M pipelined accumulator.

If the accumulator input is time invariant, each bit of the input word and the adder output bits can be delayed properly such that an N-bit accumulator can operate at the speed of a 1-bit full adder. This type of accumulator, called a pipelined accumulator, uses the most hardware, but achieves the highest speed. Figure 4-4 [23] illustrates a generic architecture of an N×M pipelined accumulator with an N-bit input FCW and a total of M pipelined rows [23]. In the figure, Verilog notation is used to represent the location of the bits. For instance, FCW[N:2N – 1] denotes bits of FCW from the N^{th} bit to the $(2N – 1)^{th}$ bit. Each row has a total of M delay stages placed at the input and output of an N-bit adder.

Obviously, an N×M pipelined accumulator has a latency period equal to the propagation delay of M – 1 clock cycles. Note that an accumulator needs at least one delay stage even without any pipelined stages. The illustrated pipelining accumulator allows the N×M bit accumulator to operate at the speed of an N-bit accumulator, a speed-up of M times. When the number of adder bits is set to one (N = 1), the 1×M bit accumulator can operate at the same speed as a 1-bit adder. To realize an 11-bit accumulator, we can set N = 1 and M = 11. Thereby, an 11-bit accumulator runs at the speed of a 1-bit accumulator consisting of a full-adder and a flip-flop.

The sum and carry-out of a full adder can be expressed as:

$$\begin{cases} \text{Sum} = A \oplus B \oplus C \\ C_{\text{out}} = A \cdot B + B \cdot C + C \cdot A \end{cases} \tag{4.5}$$

where A and B are the input bits and C is the carry-in of the adder.

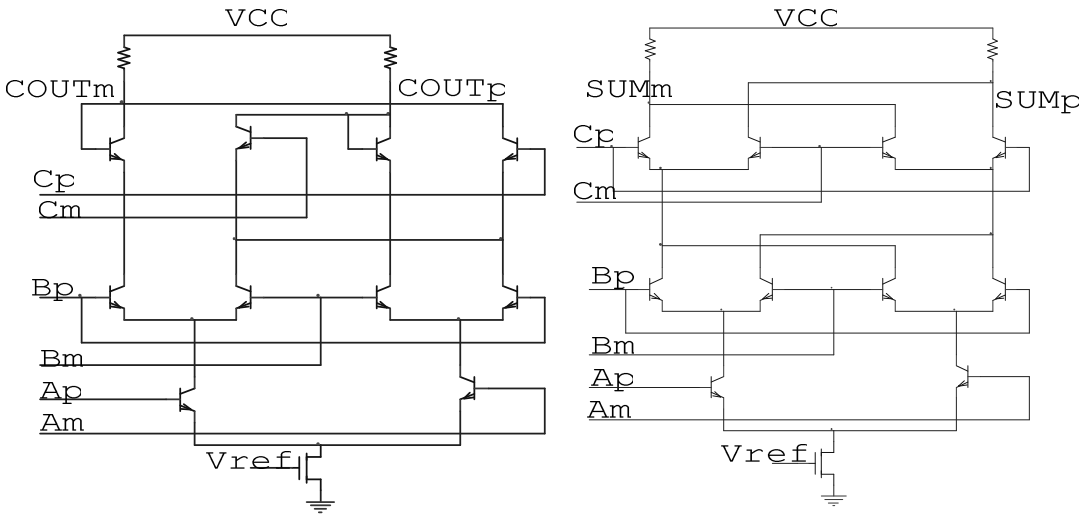


Figure 4-5 1-bit CML full adder.

The CML circuit for a 1-bit adder is illustrated in Figure 4-5 with four-level transistors. The sum circuit reduces the number of transistors by two and the capacitance load on the

output as well, compared to the conventional 3-level logic topology. The simulation results confirmed that the speed of the full adder increases 20% using the four-level logic and the propagation delay is 10ps in SiGe 200GHz technology. For 3.3V supply voltage, four levels of bipolar transistors cannot be vertically stacked without saturating the top level transistors. It is rather critical for high-speed circuit to keep all the transistors from saturation. Therefore the current source for the CML circuit is replaced by an NMOS transistor which can attain low overdrive voltage with large W/L ratio.

The clock tree design is very critical for the equal driving capability of the clock signal at each DFF's input. Clock tree layout is important to make equal phase delay form the original input to each end clock. Due to the fact that the load capacitance is proportional to the bias current, we designed a clock tree with present current to total next stages' current to 1:4. In order to make the clocks have equal delay, the N×M accumulator is split in half and the whole clock tree is inserted inside to make the equal clock path to each DFF. A 20GGz 11-bit pipeline accumulator in 200GHz SiGe technology has been implemented in a DDS tape-out.

4.4.2 **Carry Look-Ahead Adder**

When modulation is implemented using DDS, the pipeline accumulator is no longer suitable for its input is a constant. The intuitive way to construct a N-bit adder with variable input is to place *N* 1-bit adders in a chain starting with a 1-bit half adder followed by *N*–1 1-bit full adders with the carry-in of the full adder connected to the carry-out of the

previous bit. The most significant bit of the sum must wait for the sequential evaluation of all N-1 1-bit adders. It's very low for high-speed circuits.

The delay of an N-bit ripple adder is hence simply Delay=$(N-1)T_{carry}+T_{sum}$, where T_{carry} is the time for carry generation and T_{sum} is the time for sum generation in a 1-bit adder.

Carry look-ahead adders use methods to reduce the carry propagation delay by adding additional logic. It divides the full adders into subgroups and employs the carry look-ahead logic to speed up the carry propagation process. For the most 3 input levels for our CML logic, we use a 3-bit adder as a single building block to form a 12-bit adder.

For a full adder with inputs A_i and B_i and a carry-in C_{i-1} from previous adder, the carry out c_i

$$c_i=a_i\cdot b_i+(a_i+b_i)\cdot c_{i-1}$$

Let the generate $gi= a_i\cdot b_i$ and propagate $pi=(a_i+b_i)$, we can calculate all the gi and pi by using the existing a_i and b_i. and the c_{i+1} can be get by initial c_{in} and combination of pi and gi at each stages. For a 3-bit adder, the carry out of each stage can be calculated as:

$$\begin{cases} c_1 = g_0 + p_0 \cdot c_{in} \\ c_2 = g_1 + p_1 \cdot g_0 + p_1 \cdot p_0 \cdot c_{in} \end{cases} \tag{4.6}$$

After getting each carry-in, we can use 3 half-adders to calculate the 2 output sum bits. This single block can be used to construct 3~12bit carry look ahead adder by using 2nd and 3rd level of abstraction logic to calculate the carry-ins between the basic 3-bit adder blocks .

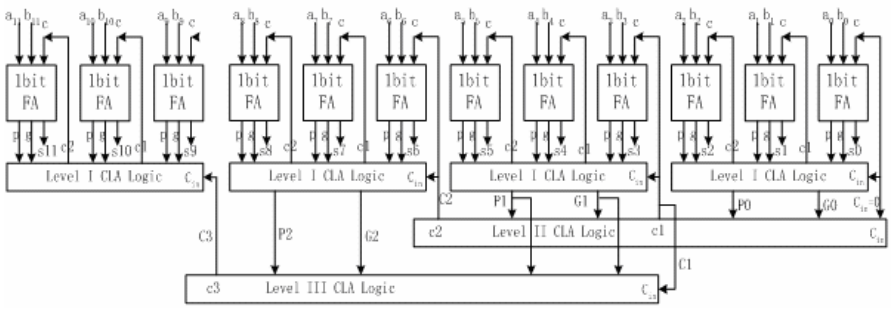


Figure 4-6 A 12-bit carry look-ahead adder using CML logics.

The level II and III CLA logic is same as level I CLA logic and only one CLA is need to be built.

$$\begin{cases} C_1 = G_0 + P_0 \cdot C_{in} \\ C_2 = G_1 + P_1 \cdot G_0 + P_1 \cdot P_0 \cdot C_{in} \\ C_3 = G_2 + P_2 \cdot G_1 + P_2 \cdot P_1 \cdot C_1 \end{cases} \tag{4.7}$$

The combinational logic of level II and III carry generate Gi and propagate Pi are also same and reusable.

$$\begin{cases} G_0 = g_2 + p_2 \cdot g_1 + p_2 \cdot p_1 \cdot g_0 \\ G_1 = g_5 + p_5 \cdot g_4 + p_5 \cdot p_4 \cdot g_3 \\ G_2 = g_8 + p_8 \cdot g_7 + p_8 \cdot p_7 \cdot g_6 \\ P_0 = p_2 \cdot p_1 \cdot p_0 \\ P_1 = p_5 \cdot p_4 \cdot p_3 \\ P_2 = p_8 \cdot p_7 \cdot p_6 \end{cases} \tag{4.8}$$

The schematic of the 12-bit CLA adder is shown in Figure 4-16. The longest critical path in this carry look-ahead adder is a path that starts from inputs a_i b_i ->G_0-> C_1-> C_3 ->c_{10}. This path uses 8 AND(OR) gates and assuming each AND(OR) has 10ps propagation delay with same load. The 12-bit CLA adder can run at over 10GHz speed in 200GHz SiGe.

4.5 **Nonlinear DAC**

Nonlinear digital-to-analog converter converts the digital phase from accumulator directly into its analog form. It's most important and hard to realize very high speed DDS. A SiGe cosine-weighted nonlinear DAC [24] with 10GHz sampling rate is presented in this section. It takes the advantage of high switching speed of SiGe current switches and uses the current mode logic (CML) circuits to realize the digital control logics. The DAC is designed using a 47GHz SiGe technology and achieves a maximum 5GHz output frequency with 10GHz clock. The DAC only consumes about 1W power, which is much smaller than that of a prior art cosine-weighted DAC implemented in InP [25].

The total output current doubles when DAC bit increases by one bit and the number of DAC cells also doubles when phase bit W increases by one bit. Thus, the DAC bit and the phase bit W should be chosen as small as possible to minimize the area and power consumption. Moreover, the DAC output using an open collector resistor may encounter headroom problem if the total output current is too large. For low power application, we first choose a reasonable number of DAC output bits based on the required SFDR. Then, we choose the number of phase bits slightly larger than that of the DAC output bits such that the overall quantization noise is dominated by the number of DAC bits. For example, if the SNFR is required to be below -45dB, then according to Figure 2-6, the DAC bit is at least 8. This result is obtained under the assumption that that the phase bit W is equal or greater than the DAC bit. Having known the output DAC bit, the value of phase bit W can be obtained by the SINAD requirement in the band. By adding a delta-sigma modulator in DDS, the quantization noise can be pushed away from the Nyquist band and thus increase

the in-band SINAD. So the phase bit W can be reduced using sigma-delta modulation, which further reduces the decoder size and thus increases the circuit speed.

The architecture of the nonlinear DAC in DDS is shown in Figure 4-7. The phase bit W from the phase accumulator is fed into a 1's complementor. The complementor output bits (W-2 in length) are separated into MSBs (a bits in length) and LSBs (b bits in length) and passed to the row and column control blocks using thermometer-decoding scheme.

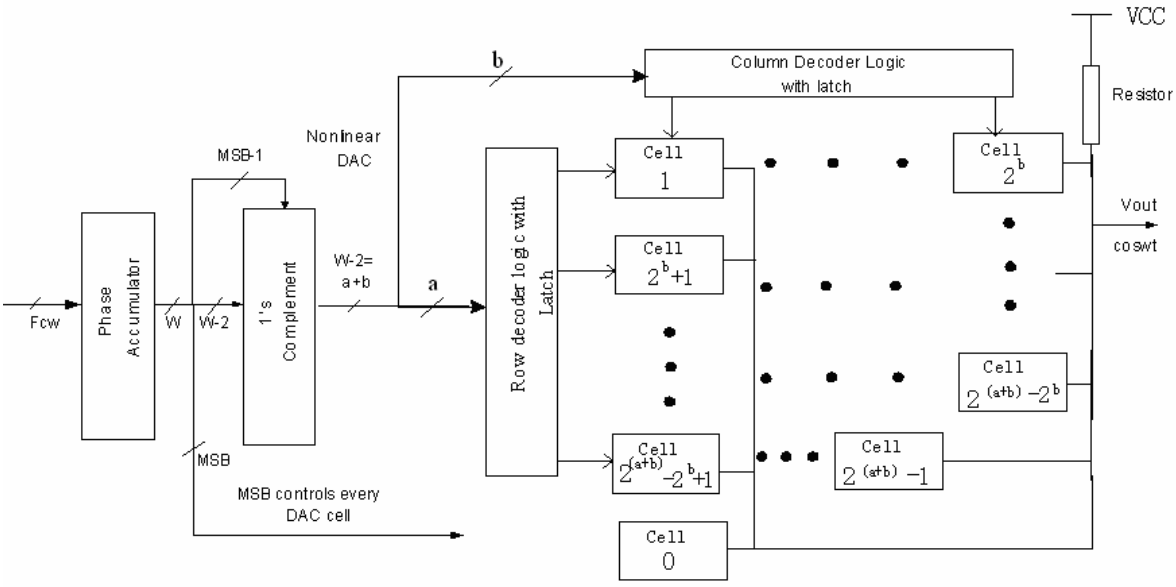


Figure 4-7 Architecture of the nonlinear DAC in DDS.

These blocks translate the binary input into thermometer code and pass the values to the control logic in each DAC cells for the selection of the current–cell matrix. The sine wave output is obtained by summing the output currents from all the selected current cells. The thermometer decoding reduces dynamic errors by ensuring that the minimum number of cells switches simultaneously. The number of current sources that are turned on should be equal to the value of the thermometer input code. Let the W=6 and a=b=2, the thermometer decoder logic function is shown in table 4-1.

Table 4-1 Thermometer-code representation of 2-bit binary values

Phase step(k)	Binary (a or b) a1(b1)	a2(b2)	Thermometer decoder output R1(C1)	R2(C2)	R3(C3)
0	0	0	0	0	0
1	0	1	1	0	0
2	1	0	1	1	0
3	1	1	1	1	1

Note that a value of 0.5 introduces a 1/2 LSB amplitude offset in equation (2.4) such that XOR gates **c**an be used as 1's complementor. During the negative region that is from π to 2π, the sine wave amplitude is generated by the complementation of the amplitude values in positive region (0 to π). If there is no 1/2 LSB offset, the amplitude in the last phase step of positive region and the amplitude in the first phase step of negative region would be both zero. This would destroy the symmetry of the output sine wave form. As shown in Figure 4-8:

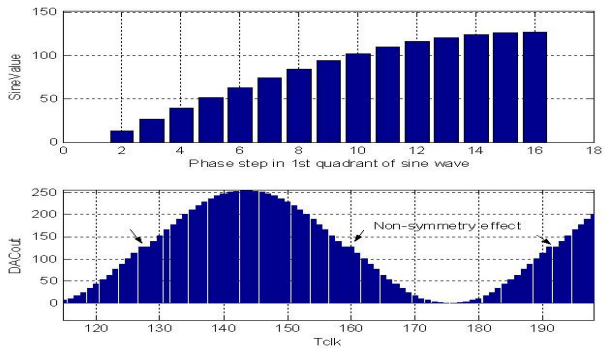


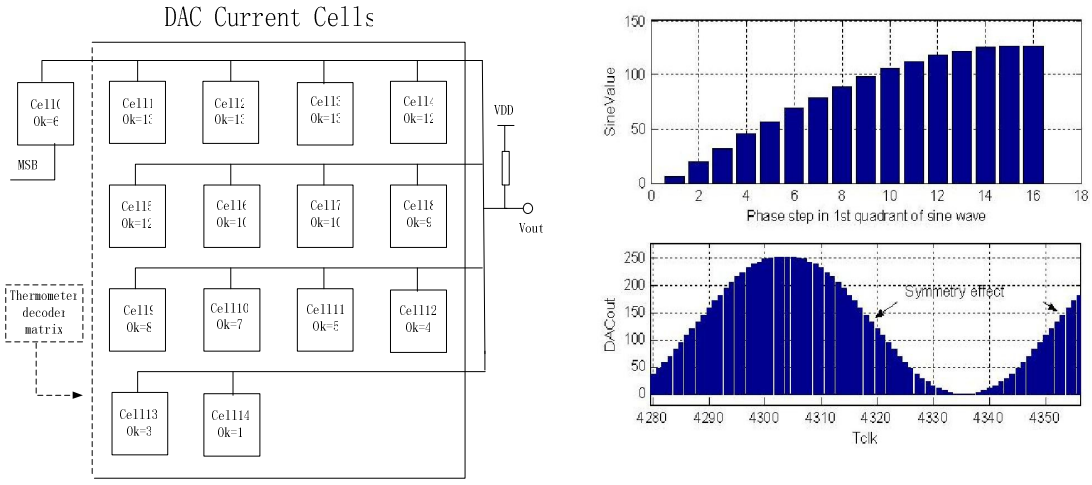
Figure 4-8 Non-symmetry effect of sine waveform.

Therefore, the 1/2 LSB is introduced to offset the sine output from value 0 when K equals 0. Yet, this offset conflicts with thermometer decoding. Thus, in this design the first DAC cell 0 is placed out of the thermometer decoder cell matrix and is separately controlled by the MSB. When MSB is low (positive region of sine wave), it turns on and vise versa. The proposed DAC architecture can reduce the glitches in thermometer decoder

and meanwhile keep the amplitude symmetry of the output sinusoidal wave. The rest DAC cells from 1 to 2^{a+b}-1 are placed in the DAC cells matrix as shown in Figure 4-9 (a). For the nonlinear DAC with W=6 and a=b=2, the output currents of DAC cells from 0 to 15 are given as follows:

O_k= 6 13 13 13
12 12 10 10
9 8 7 5
4 3 1 0

The first DAC cell O_0=6 is moved out of the cell matrix and is separately controlled by MSB. Because the last DAC cell O_{15} =0, this DAC cell is neglected in the DAC cell matrix. The structure leads to the symmetry effect as shown in Figure 4-9 (b).



(a) DAC cell matrix with W=6(a=b=2) (b)Symmetry effect of sine waveform

Figure 4-9 DAC cell matrix structure and its symmetry effect.

The DAC cell with different current source O_k is shown in Figure 4-10, where *n* represents the number of duplicated minimum current tails that form the desired current value O_k. The CML circuits are used to implement the current switches and the differential transistors both operate in the forward-active region with 400uA bias current. Although higher bias current can speed up the circuit slightly, it's not preferable because the total

power consumption increases and the output pull-up resistor value decreases in order to keep the same full-scale output voltage. A differential input voltage of 400mV is used to switch the current cells.

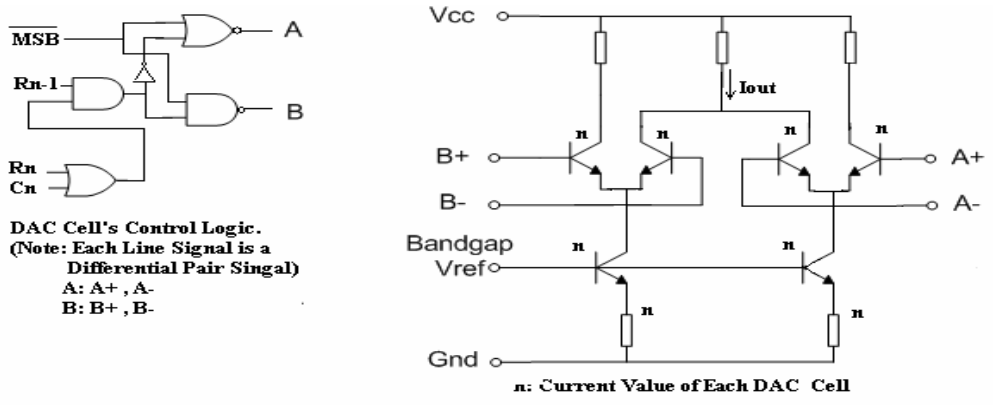
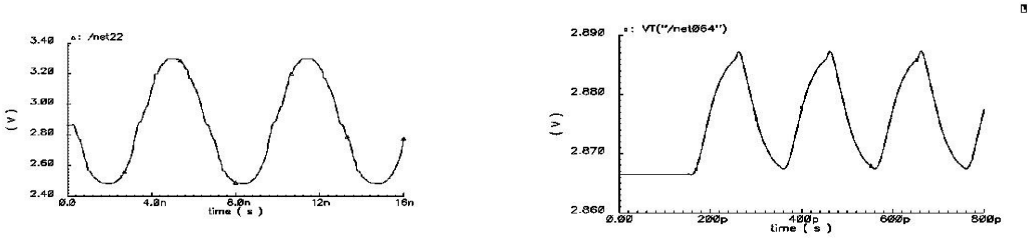


Figure 4-10 DAC current cell circuit.

Moreover, during a sampling period, the current is held constant. The two pairs of current switches A and B are used for producing the positive and negative regions of the sine wave outputs, respectively. For the positive region, the signal MSB is low, and the current switch pair A in all the DAC cells are turned on. The thermometer-code decoders will turn on the pair B according to cell control logic. For the negative region, the signal MSB is high and all the current switch pair B are turned off. The thermometer code decoder will turn on each cell's switch pair A according to the logic control circuit shown in Figure 4-10.

We have designed the proposed nonlinear DAC in a 47GHz SiGe technology. Simulations were run with 6-bit phase input W (a=b=2) and 8-bit DAC output under f_{clk}=10GHz. There are total $2^{(a+b)}$=16 phase steps in one quadrant and the output frequency is set as 10GHz/(16*4)=125.25MHz. The 125.25MHz output waveform is shown in Figure 4-11 (a). Figure 4-11(b) gives the simulated DAC output waveform with the maximum

output frequency of 5GHz with clock frequency of 10GHz. Using the minimum size transistor with 1um emitter length, the total nonlinear DAC power consumption is 0.57 W, including the DAC cells and decoders.



(a) Output at 125.25MHz (b) Output at frequency 5GHz

Figure 4-11 Simulated DAC output waveform at 10GHz.

4.6 **Ultra High Speed DDS with MASH Delta-sigma Modulation**

A 16b direct digital frequency synthesizer in 120G HBT technology is presented in this section. Its top level schematic is shown in Figure 4-12.

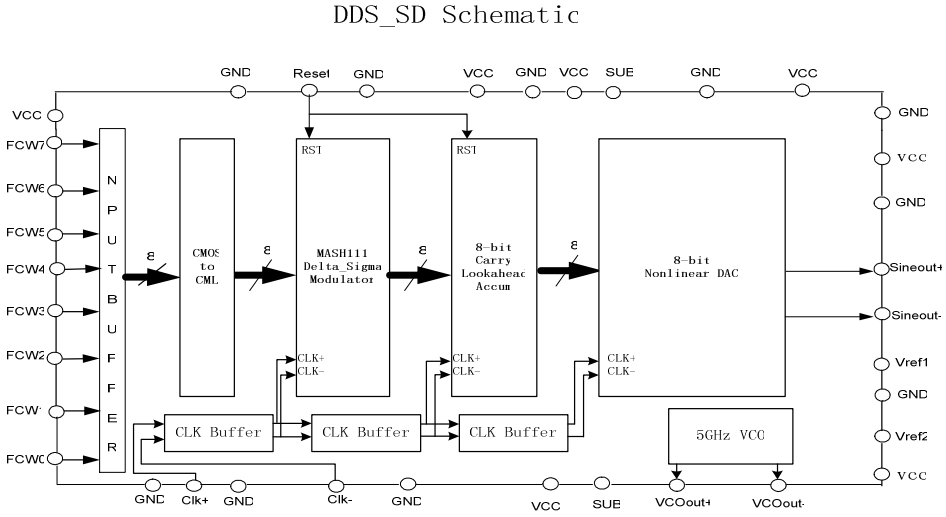


Figure 4-12 Schematic of DDS with delta-sigma modulation.

It consists of a 7GHz 3rd order MASH delta-sigma modulator in frequency domain, a 8-bit carry look ahead accumulator and a 10 GHz nonlinear current-steering DAC.

Differential CML is used in circuit implementation to reach high speed and low power consumption. The prototype IC die area is 3mm×3mm and it consumes 4W with 3.3V supply.

It's better to truncate less phase bits and make the left phase bit W big to keep more phase information. But if the phase input bit W is increased more by 1 bit, the decoder size of the nonlinear DAC would double and would cause more unwanted switch glitches. On the other hand, the total current output of the DAC is proportional to 2^D (D is the DAC resolution bits) which is proportional to the DAC power consumption. Considering these tradeoffs, the phase is truncated to W=8 bits before it goes to the nonlinear DAC and the DAC output bits R is chosen to be 8.

With DAC input and output both be 8 bits, the spurs generated by the phase truncation become dominant. In this case, the worst case spur in DDS output spectrum is -48dBc. A delta-sigma modulator is used to modulate the truncated B bits (B=L-W) and add them back to the frequency word before it goes to the accumulator as shown in Figure 3-7. With this effort, the worst case spur can be furthermore decreased. It also shows that frequency domain modulation has its advantages due to modulator's constant input and shrinkage of phase accumulator's size. The phase accumulator's size is also decreased from 16 bits to 8 bits. There're several delta-sigma modulator types that can be implemented and different modulator type would lead to different DDS output spectrum.

A 3rd order MASH Delta-Sigma is chosen for its high speed, stability and easy implementation. The accumulator size is fixed to 8bit and no multiplier is needed. 4-level CML is used to realize basic logic gates such as a 1-bit full adder shown in Figure 4-5. Bias

current of current switch pair is 400uA. To speed up the circuit, Carry Look-ahead adders are used. Adjacent 3 bits of each input are grouped into a 3-bit CLA cell to match the 3 input levels of basic logic cells. DFFs are inserted into data flow to buffer each adder's outputs. Two's complemented format is used to realize the constant minus one. Because each digital bit is realized by differential pair, the opposite value of one bit is simply the reverse of the differential pair.

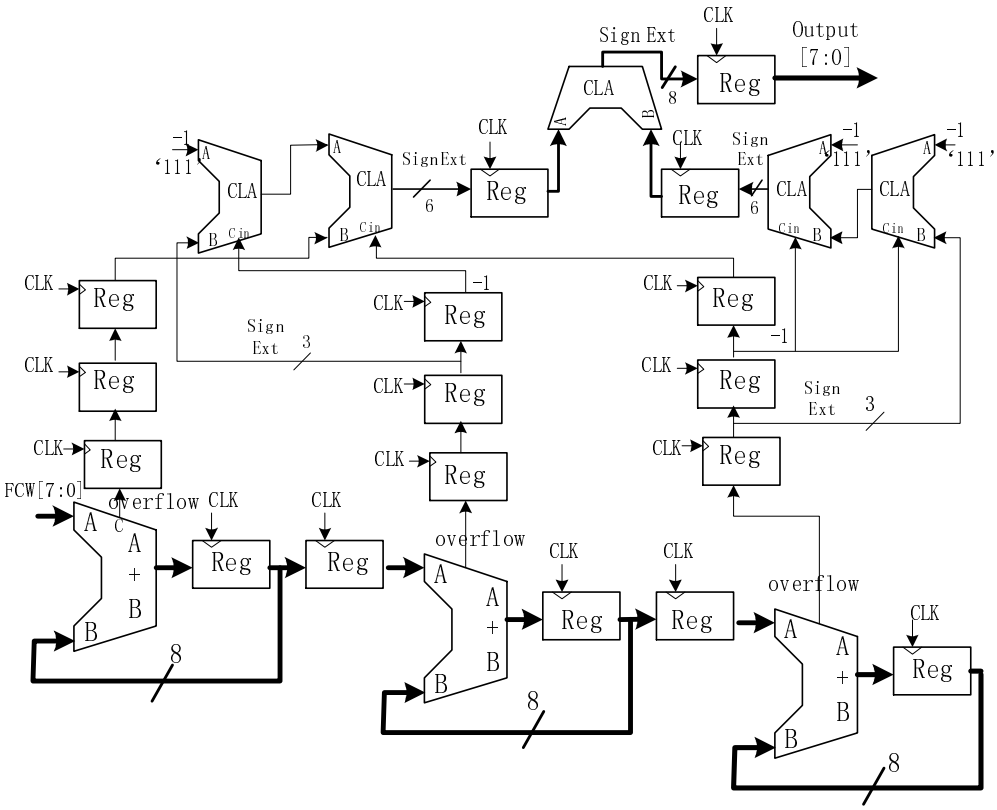


Figure 4-13 Third order MASH delta-sigma modulator architecture.

Figure 4-13 shows the whole architecture of the 3rd order MASH delta-sigma modulator. It is composed of 3-bit CLA adders and DFFs. Its inputs are the truncated 8-bit frequency word *B* from FCW and its output 8 bits are added back to the frequency word *W* and go to phase accumulator.

Figure 4-14 shows the simulation result of the third order MASH type delta-sigma modulated accumulator's output running at 7GHz. Its functionality is verified using Matlab test pattern.

The output of delta-sigma modulated accumulator goes to a 10GHz current-steering 8-bit nonlinear DAC and this forms the whole DDS. The DDS current outputs are converted to differential voltages by a pair of off-chip 15Ω pull-up resistors.

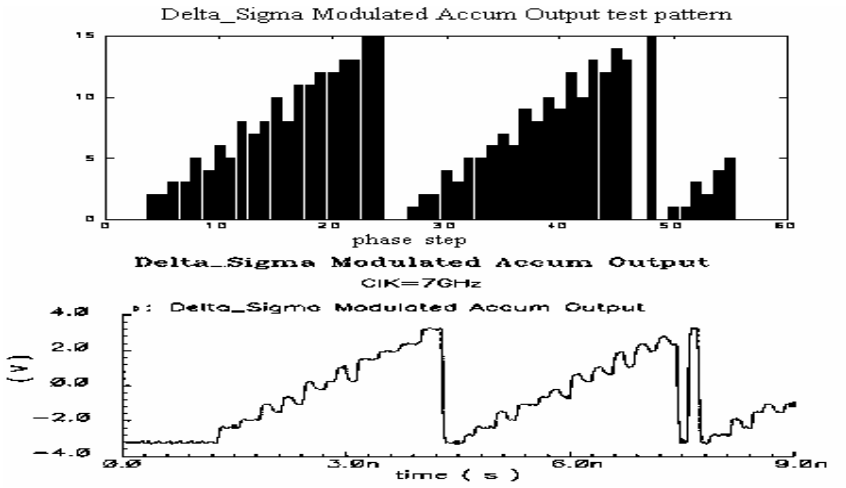
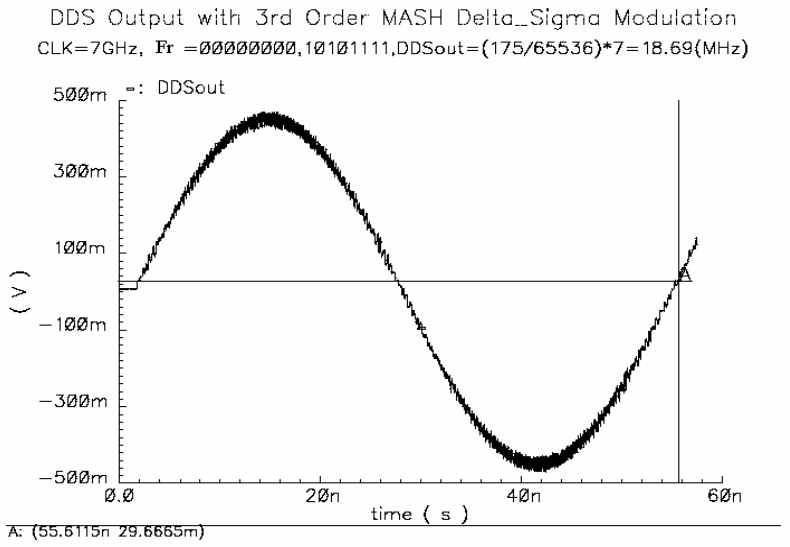


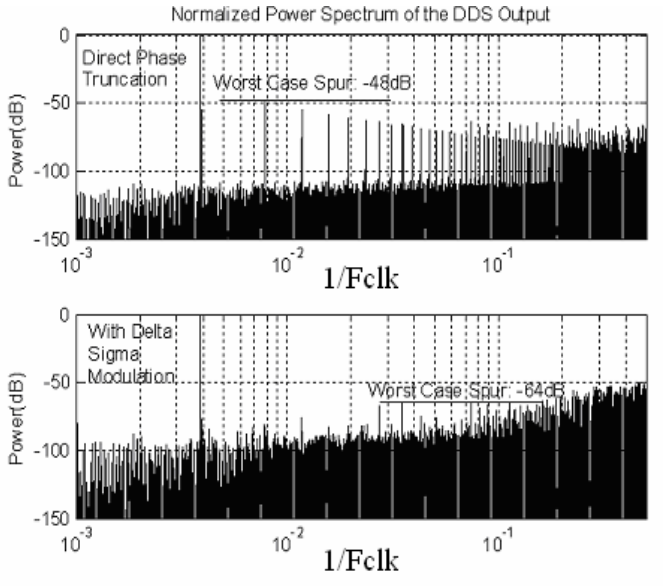
Figure 4-14 Delta-sigma modulated accumulator output running at 7GHz.

Figure 4-15 shows the whole DDS simulation output at a clock frequency f_{clk} =7GHz. The input frequency control word is set as 00000000,10101111(175d). The generated output frequency is thus (175/65536)*7=18.69(MHz).

The output spectrum is shown in figure 4-15(b). The upper picture shows the output spectra of DDS with direct phase truncation from 16bits to 8 bits. The frequency range is from 0 to 0.5*f_{clk}. The lower picture is the output spectra of DDS with delta-sigma modulation. The worst case spur has been reduced from –48dB to –64dB by employing the third order MASH type delta-sigma modulation in the frequency domain of the DDS.



(a)Sine output at 7GHz clock



(b) Worst case improvement in spectrum

Figure 4-15 Delta-sigma modulated DDS output waveform and spectrum (F_{clk}=7GHz).

The DDS die diagram is 3×3 mm^2 die size. It includes a third order MASH type delta-sigma modulator, 8bit phase accumulator, 8bit nonlinear DAC and VCO. The VCO is used to drive the chip with its output so the whole chip does not need the outside driving

clock. The power consumption of the pure DDS with delta-sigma modulation is 2.5W under 3.3V supply.

4.7 **Conclusions**

This chapter introduces the RF circuit design of high speed DDS building blocks such as CML running over 20GHz, pipelined phase accumulators running at 20GHz, Carry look-ahead accumulator running at 10GHz, MASH 1-1-1 delta-sigma modulator running at 7GHz and a nonlinear DAC running at 10GHz.

CHAPTER 5 DDS BASED BUILT-IN SELF TEST

5.1 Introduction

As discussed in previous chapters, direct digital frequency synthesizer (DDS) can switch its output frequency instantly by changing its frequency control word. It is also capable of generating various waveforms with changeable output amplitude. Moreover, the hardware area and power consumption of DDS can be minimized by adding delta-sigma modulation either in frequency or phase domain [27]. All these characteristics benefit DDS a good test signal source for on-chip analog circuit test.

In this chapter, a built-in self-test (BIST) approach based on DDS for analog circuitry test in mixed-signal systems is presented. The BIST can do on chip analog circuitry functional measurement of linearity and frequency response including both phase and gain. The approach has been implemented in Verilog and synthesized into a field programmable gate array (FPGA) where it was used for testing of an actual device under test (DUT) and the measurement is compared to theoretical simulation results and real outside spectrum analyzer measurement. In section 5.2, the theory and application of the proposed BIST approach to linearity test are introduced. In section 5.3, a method for analog frequency response and linearity tests will be presented. Finally, conclusions will be given in section 5.4.

5.2 **Linearity Test Using DDS**

Linearity is a critical performance of analog amplifiers and mixers. Third-order intercept point (IP3) is a figure-of-merit for linearity for the fact that the third-order inter-modulation (IM3) distortion products are close in frequency to the fundamental signal in the output spectrum and they cannot be removed easily by filtering. The third-order inter-modulation products can be measured by of mixing two-tone input signals to the DUT. By sweeping the amplitude of the two-tone input signal, we can reach a point that the IM3 product equals the ideal linear amplified fundamental signal. At this point, the input signal level is named as input referred IP3 (IIP3) for the amplifier. Higher IIP3 means better linearity and less distortion. The two-tone test signal contains frequencies ω_1 and ω_2 for IIP3 test can be generated by DDS embedded on chip. DDS as a test pattern generator can also sweep its test tone amplitude by changing the effective bits that fed into the DAC. With the two-tone inputs, the device under test (DUT) generates the output that contains fundamental signals ω_1, ω_2, two IM3 tones, $2\omega_2-\omega_1$, $2\omega_1-\omega_2$ and other inter modulation frequencies. Usually, the IM3 are measured by outside equipment such as frequency analyzer to analyze its spectrum directly.

For on chip measurement, traditional way is to convert the DUT output to digital sampling points by an ADC and use FFT to analyze its power spectrum. As shown in the Figure 5-1, the input two tones are added after look up tables in sampled domain and fed into the DAC. The analog output from the DAC is the combination of the two-tone test input. Moreover, by gradually addressing the least significant input bits to most significant bits of the DAC, the test tone amplitude can be swept from small to big. The combination

of two-tone test signal is filtered by a LPF on the DAC board and then fed into the DUT (analog amp or filter).

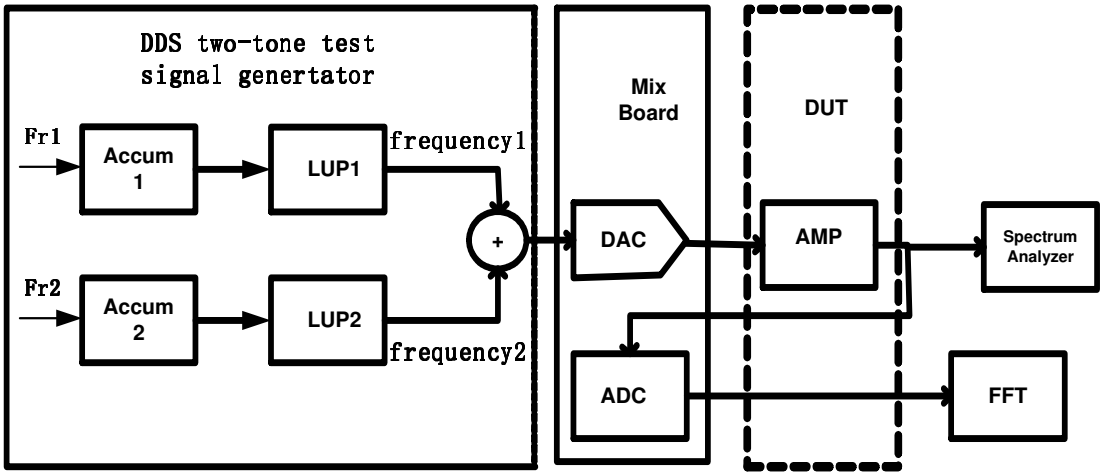


Figure 5-1 Two-tone test using DDS for linearity test.

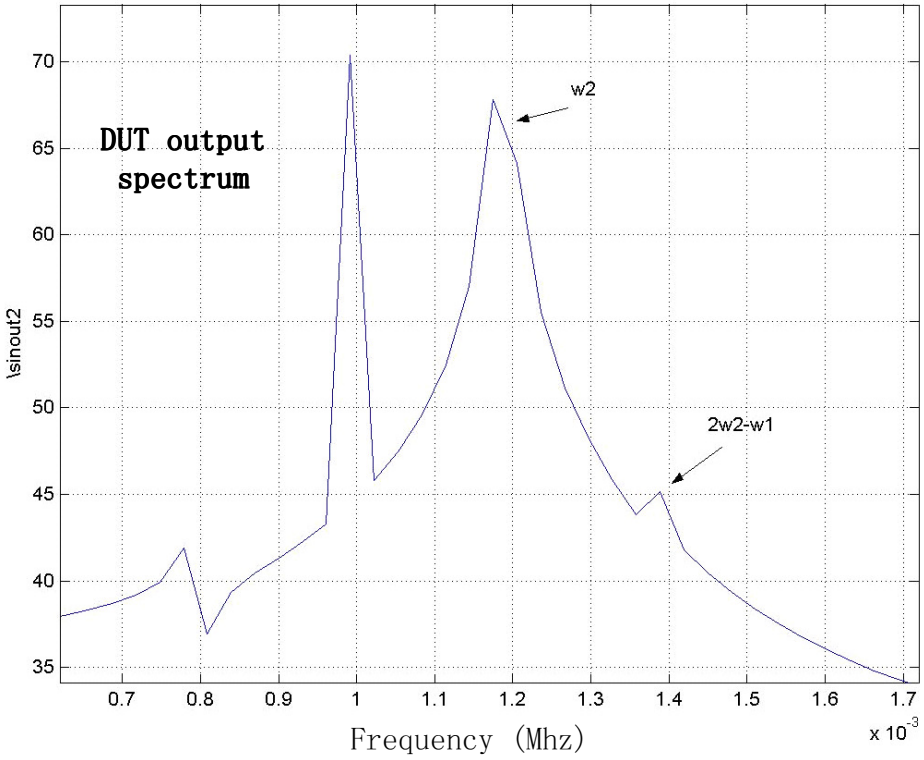


Figure 5-2 DUT output spectrum measured by FFT.

On chip spectrum analysis using FFT requires a big amount of hardware implementation. Its accuracy depends on the frequency sampling points calculated by FFT. For the 1024*64 points FFT of the DUT output spectrum analysis is shown in Figure5-2, the frequency resolution is still not good enough to get the accurate values of two IM3. The two IM3 values are not equal and ω_2 is missed for it is between two consecutive frequency sampling points. Increasing the sampling points of FFT would cause more complexity of implementation.

The proposed method uses a BIST-based measurement to get the IIP3 of a DUT automatically and accurately with much less hardware compared with usual FFT approach. In this method, an on-chip digital multiplier is used as a down converter that can selectively capture the frequency components ω_2 and $2\omega_2-\omega_1$ in DUT output. It down-converts them into two DC signals. The DC values can be further compacted for evaluation of IIP3 by using an accumulator.

5.2 BIST-based measurement of linearity

The DDS based BIST for automatic linearity test is shown in Figure 5-3. Total three lookup tables are used to generate test signals with two fundamental frequency1(ω_1) and frequency2(ω_2) and one third order frequency3($2\omega_2-\omega_1$). The two-tone input test signal is formed by adding the DDS output signals ω_1 and ω_2. The basic signal ω_2(or ω_1) and third order test tone $2\omega_2-\omega_1$ are accurately generated by setting the frequency control word *Fr1*(=*Fr2*) and 2*Fr2-Fr1* from DDS. They are also used for capturing the correspond components in the DUT output spectrum. This is done by the two simple additional digital

multipliers and accumulators that form the output response analyzer to generate tow DC signatures DC1 and DC2 whose values are proportional to the power level of fundamental component and IM3 component in the output spectrum. In this way, the power different of first order component and IM3 in output can be easily got from equation below:

Delta_P=20log (*DC1*)-20log (*DC2*) (5-1)

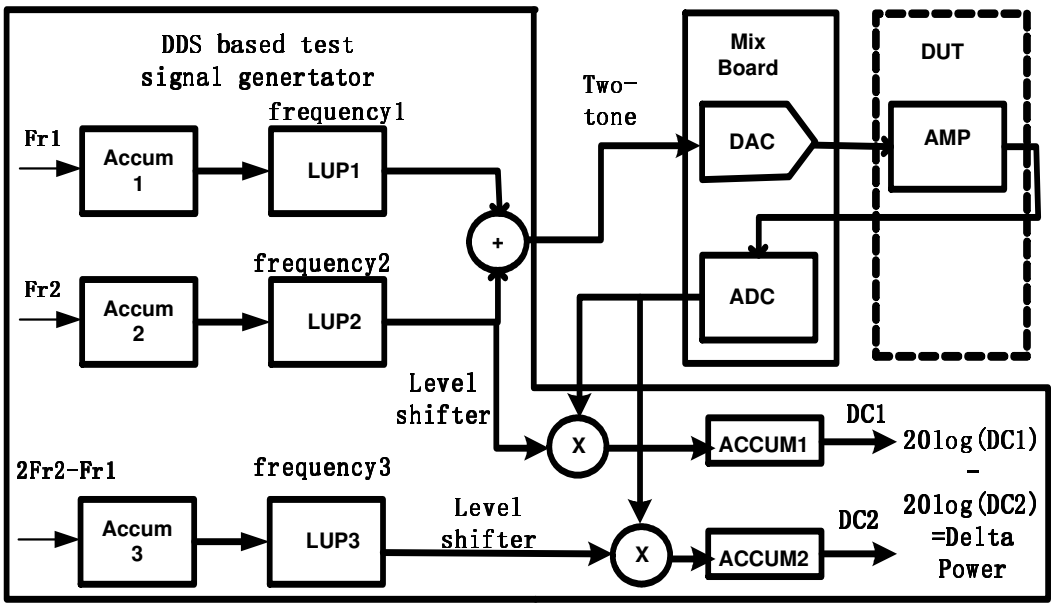


Figure 5-3 Automatic Linearity (IP3) Test using DDS.

Delta_P (ΔP) represents the power difference of the IM3 component between the fundamental signal in output spectrum at a certain input level. The good linearity performance can be proved by measurement of ΔP. As discussed below, under some circumstance, the IIP3 can be directly measured by ΔP and input signal power lever.

First of all, the DUT is represented by a nonlinear function *f(u)* for analysis. For more intuitive understanding and a preparation for matlab simulation, let's look at the nonlinear function *f(u)* of the model of a BJT:

$$ic = Is\exp(\frac{V_{BE}}{V_T})\exp(\frac{v_{be}}{V_T}) = Ic\left[1+(\frac{v_{be}}{V_T})+\frac{1}{2}(\frac{v_{be}}{V_T})^2+\frac{1}{6}(\frac{v_{be}}{V_T})^3+...\right]$$

$$= Ic(1+a1\times v_{be}+a2\times v_{be}{}^2+a3\times v_{be}{}^3) \quad (5\text{-}2)$$

where *a1*=1/0.026; *a2*=1/(2*0.026*0.026); *a3*=1/(6*0.026*0.026*0.026). The input two tones are from DDS and have same amplitudes *A*. After normalization, we can get *a1*=1, *a2*=20, *a3*=246, the *a2* and *a3* are set according to the same proportion to the BJT. In order to comply with the DDS output, the sine waves from ω_1 and ω_2 both have DC bias *A*.

For small input amplitude *A* and satisfies the equation below [29][30] :

$$a1\cdot A >> (9/4)\cdot a3\cdot(A^3) \quad (5\text{-}3)$$

The input referred IP3 (IIP3) can be calculated by:

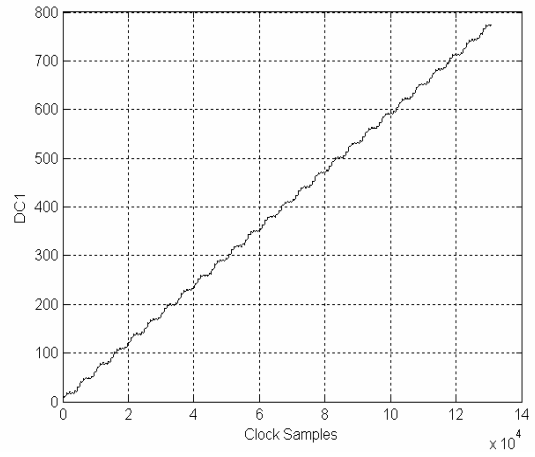
$$IIP_3[dBm] = \frac{\Delta P[dB]}{2} + P_{in}[dBm] \quad (5\text{-}4)$$

where ΔP is the difference between fundamental and IM3 components in DUT output spectrum and *Pin* is the signal power at the input.

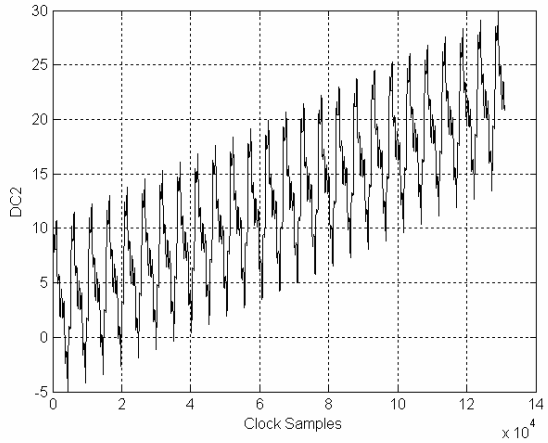
For the input test signal power level is already known, the problem is focused on how to measure the ΔP more accurately and directly in output spectrum between frequency components ω_2 and $2\omega_2$-ω_1.

Shown in Figure 5-3, a third DDS in introduced to produce the test waveform with frequency3 ($2\omega_2$-ω_1). Frequency3 and original basic signal frequency2 (ω_2) are level shifted downwards in level *A* to make the waveform symmetrical with the X-axis. This is in order to use accumulator to get rid of other frequency components the DUT output other than these two. Digital multipliers are used to down convert the two frequencies components ω_2 and $2\omega_2$-ω_1 in DUT output to DC values. The output DC series are accumulated to get DC1 and DC2.

The DC1 and DC2 from the accumulator in a matlab simulation with BJT nonlinear model are shown in Figure 5-4 and Figure 5-5.



(a) DC1

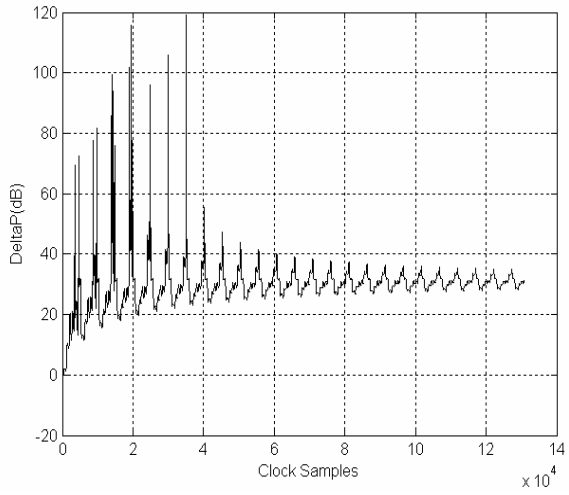


(b) DC2

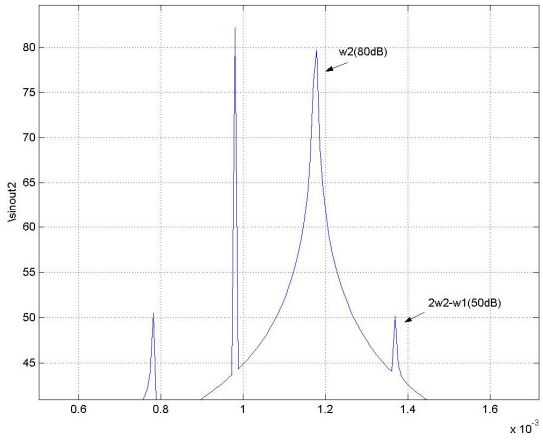
Figure 5-4 DC from the accumulator at different sampling points.

We can see from the accumulator output in Figure 5-4(a) that value of output frequency component ω_2 can be picked up by the multiplier. But there are some sine-wave-form disturbs along the DC1. In Figure 5-4(b), these disturbs are more obvious because the IM3 component ($2\omega_2-\omega_1$) is far less than the main output frequency component (ω_2). These disturbs are further amplified by the dc components in the output of the DUP.

So it's very necessary to deal with sample data that ends at the biggest period of all the disturbances and this will not need very long sampling data. For both DC1 and DC2, the common period is given by $\frac{2\pi}{\omega_2 - \omega_1}$.



(a) ΔP (30dB) with different sample points



(b) ΔP (30dB) measurement with spectrum analysis

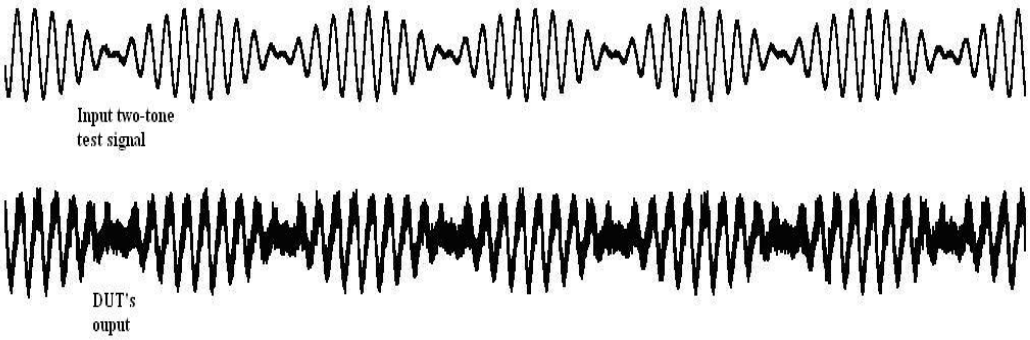
Figure 5-5 ΔP (30dB) measurement.

From Figure 5-5(a), we can see the change of ΔP with different sample points in BIST. It's clear that we need to sample at a period that is the integer times of $\frac{2\pi}{\omega_2 - \omega_1}$ in order to get the correct ΔP which is 30dB that matches well with the result got from spectrum analysis in Figure 5-5(b). The dc component in the output of DUP is enlarged and it would cause the increase of the disturbance amplitude in DC signatures. On the other hand, when we take longer time to reach a relatively stable ΔP and use mean value of the ΔP in this period, we can also get a pretty accurate value of ΔP. In practical implantation, we need to choose long accumulation time (such as 2^16 accumulation steps).

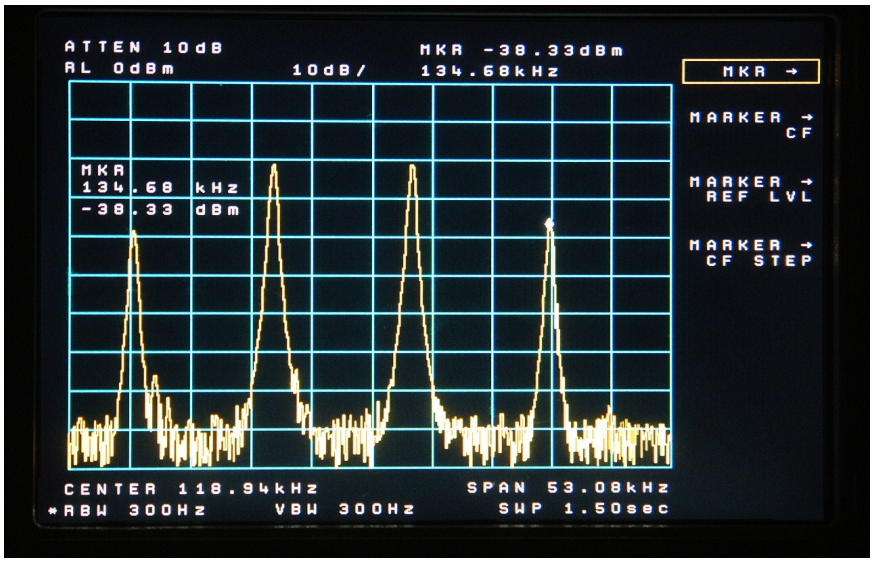
5.3 **Implementation and Test Results**

We use FPGA, a DAC&ADC board to test the nonlinearity of the DUT generated by a field programmable analog array (FPAA). The nonlinearity of the DUT is tuned by

lowering FPAA's power supply from 5v to 3v. We first measured the ΔP between the fundamental signal and IM3 by a spectrum analyzer. Then we used the BIST method to calculate the ΔP on chip automatically. The experiment results are shown below.



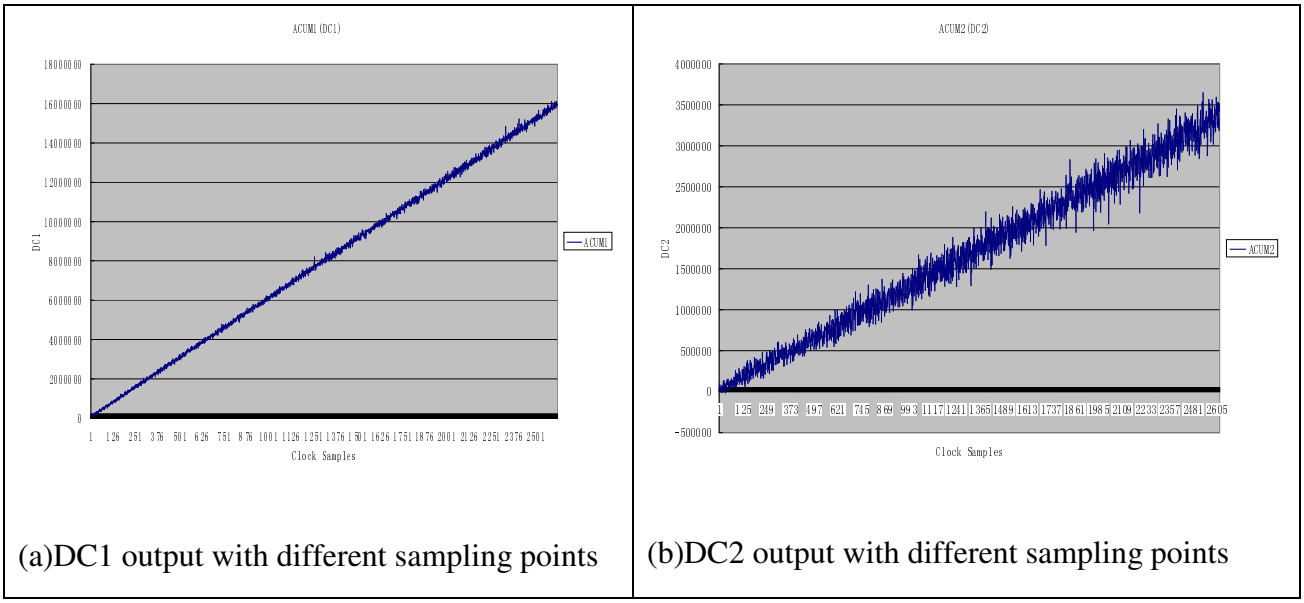
(a) Input two-tone signal the DUT output with nonlinearity



(b) Measured DUT output spectrum

Figure 5-6 Hardware measurements of two-tone test at the DUT output.

Next, we use the BIST method to measure the DUT's linearity performance. The period of $\omega_2-\omega_1$ in our experiment T=1024*$Tclk$. We use a common period Tc= 1024*110*$Tclk$ which is the integer times of T to get the ΔP without disturbances. The measured two DC signatures DC1 and DC2 are shown in figure 5-7 and they match well with the theoretical matlab simulations in figure 5-4.

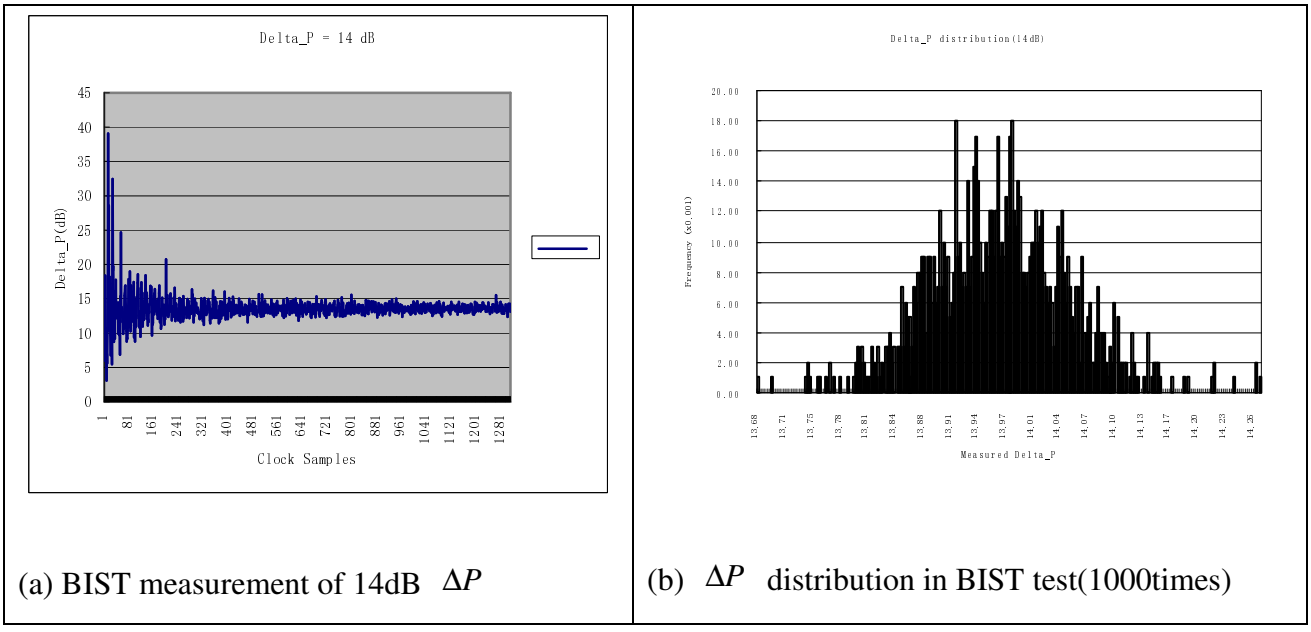


(a)DC1 output with different sampling points

(b)DC2 output with different sampling points

Figure 5-7 Hardware measurements of DC1 and DC2.

We run the experiment for 1000 times and each time the stop time is T and get the BIST result and result's distribution of a 14dB ΔP measurement.



(a) BIST measurement of 14dB ΔP

(b) ΔP distribution in BIST test(1000times)

Figure 5-8 ΔP measurement per 100 points and its distribution.

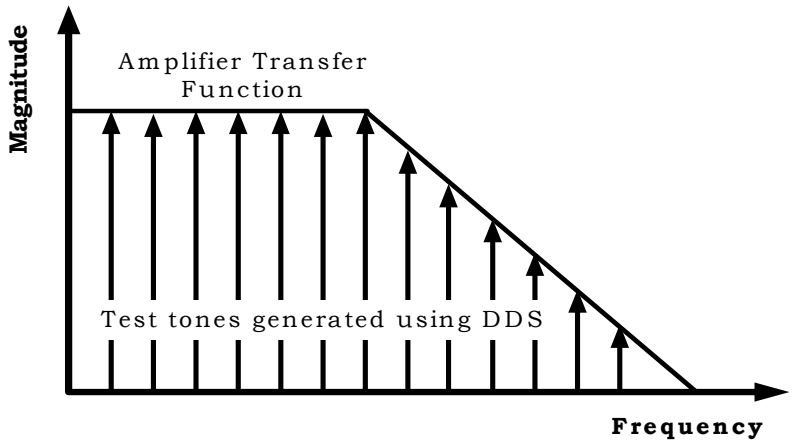
DDS based BIST ΔP measurement matches well with the result obtained using a spectrum analyzer as shown in figure 5-8(a). The measured ΔP distribution in figure

5-8(b) shows deviation 0f 0.0055 and variance of 0.0003 for the value 14dB ΔP measurement in 1000 BIST runs.

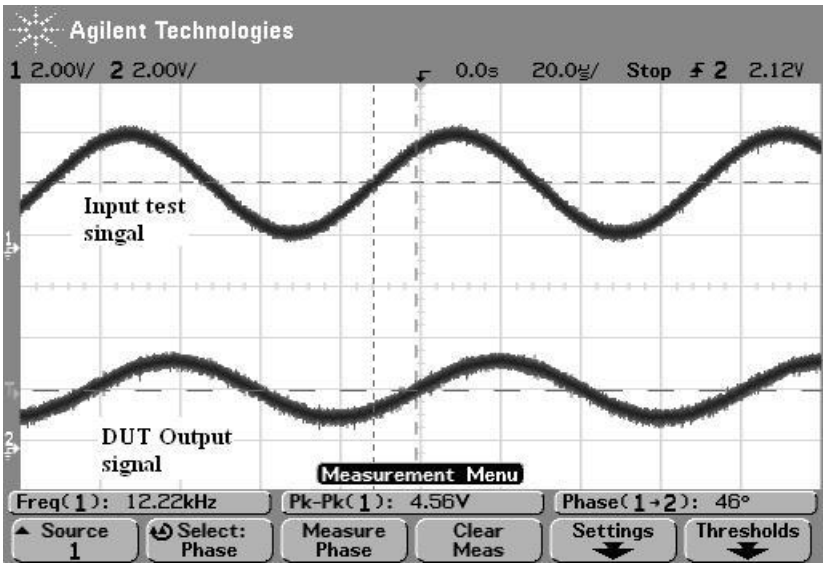
But this method also has dynamic range limitations mainly due to the ADC/DAC on the mixed signal board. For this hardware test, the ADC and DAC are both 8 bits and it limits the ΔP measurement range to within 30dB.

5.4 **Frequency Response Test Using DDS**

Frequency response including amplitude and phase response [28][31] is also critical for analog integrated filters and amplifiers. The commonly interested cut-off frequency of the filters and amplifiers can be found by measuring the pass-band and stop-band amplitude response, while the group delay can be determined from the phase response. To test the analog filter and amplifiers, the DDS generates frequency tones with fine resolution. A DDS-based test pattern generator and output response analyzer can scan the pass and stop bands of the device with fine step size and can thus measure the frequency and amplitude responses of the device, as shown in Figure 5-9(a).



(a) Frequency scan through passband and stopband



(b) Input and output signal of a DUT at frequency 12.22KHz and a phase delay=46°

Figure 5-9 Frequency response test using DDS.

In Figure 5-9 (b), when an input test tone is at 12.22KHz, the amplitude of the DUT output is degraded and there is a phase delay of 46° between the input test tone and the output. This is normally a phase difference between the external path through the DUT (amplifier) and the internal path from the test generator to the test analyzer. Phase correction needs to be done prior to the frequency magnitude measurement.

The BIST based on DDS approach to measure the phase difference between the input and output of DUT is shown in Figure 5-10. Note that in Figure 5-10 that DDS1 generates a fine-toned sine wave *T1* with a DC bias *k1*. After the test signal *T1* passes through the analog device, both its amplitude and phase will change. The signal output of the DUT is given by $D=A_2\cos(\omega_1 t+\vartheta)+k2$. A second DDS (DDS2) is used to generate test signal *T2* that has the same frequency and amplitude as *T1*. A level shifter is used to shift the *T2* signal such that it symmetrical to X-axis (from $-A1/2$ to $A1/2$). During the frequency sweep, if all the test

signals *T2* start from phase 0, namely $T2=A_1 \cos \omega_1 t$, the signal after the multiplier is hence given by:

$$MUL = A_1 \cos(\omega_1 t) \cdot (A_2 \cos(\omega_1 t + \theta) + k_2)$$
$$= \frac{A_1 A_2}{2}\left[\cos\theta + \cos(2\omega_1 t + \theta)\right] + A_1 k_2 \sin \omega_1 t \qquad (5.5)$$

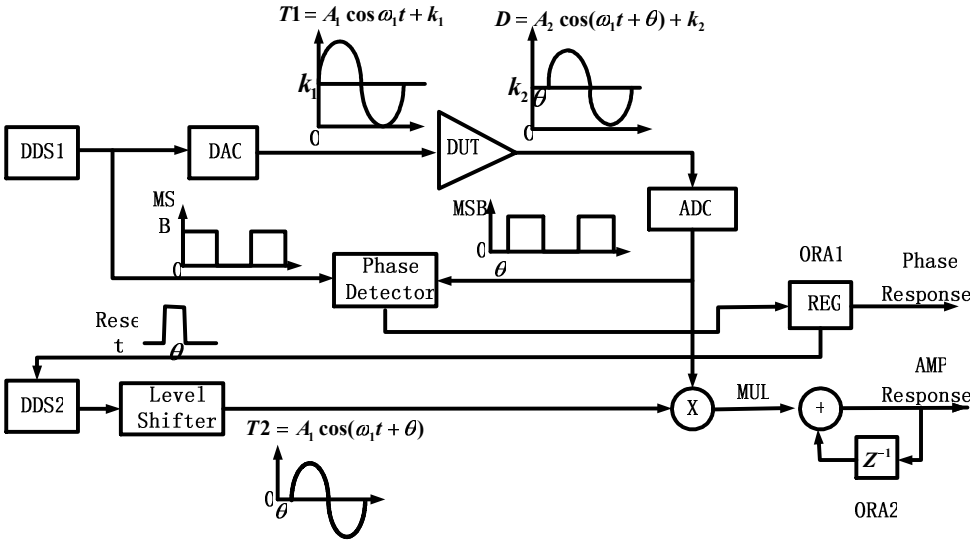


Figure 5-10 BIST of frequency response of an analog circuit.

We use an accumulator to obtain the above result and to end the accumulation on a common period of all the test sine multiplication. The period of the different test signal is:

$$T_p = \frac{1}{\frac{FCW}{2^L} \cdot F_{clk}} = \frac{2^L}{FCW} \cdot T_{clk} \qquad (5.6)$$

By setting the step of input frequency control word to be a power of 2, we can get a same period for all the test signals. In our case, the biggest period of the test signal is when *Fr*=2 which is 2^{L-1} *Tclk*, so we set the time of calculation to be 2^L*Tclk*. The phase step is set to 2 to achieve the finest frequency resolution which is $2/2^L$. The accumulator translates the output to a constant:

$$ORA = \frac{A_1 A_2}{2} \cos\theta . 2^L \tag{5.7}$$

If there is no phase shift, θ=0, the degradation of A_2 compared with A_1 will be shown in the ORA. When the ORA value decreases to 0.707 times its initial value, we have reached the 3dB amplitude point of the analog circuit. Unfortunately, analog circuits always have phase shift θ. Therefore, we need to measure θ first and make adjustments to the test signal to achieve the same phase shift.

The MSB of the test signal *T1* and the MSB of the signal *D* from the ADC are square waveforms with the same frequency and phase as their sine waveforms. Therefore, we can get the phase difference with a phase detector and record the phase shift θ corresponding to this frequency in a register and output it to the computer. For the next test frequency the register will record another phase shift and after the whole frequency sweep, we will get the frequency response of the analog device. Before the change to next test frequency, the BIST circuitry also performs the amplitude response test. When the amplitude test begins, the DDS2 will be reset and thus delayed for a phase θ that is stored in the phase register. In this way, its output *T2* would have the same frequency and amplitude as *T1* but has a phase shift θ as *D* does. That is:

$$T2 = A_1 \cos(\omega_1 t + \theta) \tag{5.8}$$

With this modified *T2* to be one input to the multiplier, the ORA1's output in equation (5.7) will have no effect of phase shift θ and we can get both the correct frequency response and amplitude response of the analog device. This idea in this approach is to measure the frequency delay with an additional phase detector and compensate phase delay in the test

pattern generator.

5.5 **BIST Measurement of Frequency Response**

We have used the proposed BIST scheme to measure the frequency response of a low pass filter (LPF). As discussed, the built-in DDS generates the test tones that scan over the frequency from 0 to ½ f_{clk} with a frequency step $(1/2^{L-1})f_{clk}$. A first order low pass filter was used as a device under test to test our BIST method which automatically applied the test tones at the input of the filter and measured its output magnitude response from ORA2. The cutoff frequency of the amplifier and LPF modules, which is 3dB below the pass-band magnitude, can thus be found at 46 kHz from figure 5-11.

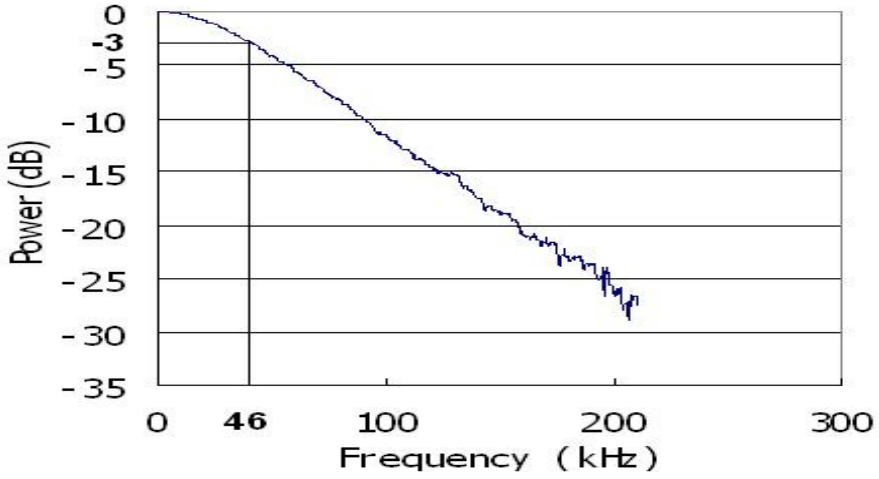


Figure 5-11 BIST measured frequency response of a low pass filter.

The DDS-based TPG, test controller, and multiplier accumulator-based ORA were modeled in Verilog along with an interface to allow PC control of the BIST circuitry and retrieval of the BIST results. The complete Verilog model is approximately 510 lines of non-commented code. The Verilog code can be parameterized to facilitate easy adaptation of the BIST circuitry for different size DAC and ADC for synthesis into standard cell based

ASICs or into FPGAs. In our implementation, we used an 8-bit DAC and ADC and synthesized the BIST circuitry into a Xilinx Spartan XC2S50 FPGA. The synthesized circuit required less than 25% of the total logic resources in the Spartan 2S50 and, as a result could easily fit into the smallest Spartan II FPGA. This means that the BIST-based frequency response measurement circuitry can be efficiently implemented in the digital portion of an ASIC with little area overhead.

5.6 **Conclusions**

In this chapter, a BIST approach using DDS is developed for analog circuit functional testing measurement of analog circuitry's linearity and frequency response including both phase and gain. The DDS-based test pattern generator is used to generate two frequency tones required in the two-tone linearity test as well as single tones for frequency response measurements. The efficient output response analyzer consisting of a multiplier and accumulator avoid using traditional FFT-based spectrum analysis which consumes much more power and die area. We have implemented the BIST approach in Verilog which was subsequently synthesized into an FPGA and verified on actual hardware with close agree to traditional measurement techniques and simulations.

CHAPTER 6 PHASE LOCKED LOOP FREQUENCY SYNTHESIZER

6.1 Introduction

Phase-locked loop(PLL) is another frequency synthesis technique that has a long history. Different from DDS that generates the output frequency directly by setting input frequency control word, PLL frequency synthesizer uses an oscillator to generate desired output frequency. The oscillator is constantly adjusted by a feedback control loop in order to match in phase and thus lock on the frequency of an input reference signal. A typical PLL structure is shown in Figure 6-1:

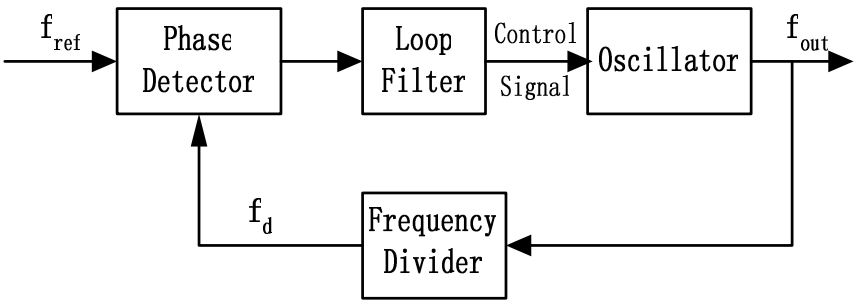


Figure 6-1 Typical PLL frequency synthesizer.

The oscillator is initially tuned to a frequency close to the desired receiving or transmitting frequency. A circuit called phase detector causes the oscillator to seek and lock onto the desired frequency, based on the output of a crystal-controlled reference oscillator. This works by means of a feedback scheme shown in Figure 6-1. If the oscillator frequency departs from the selected crystal reference frequency, the phase detector

produces a control signal to bring the oscillator back to the reference frequency. A loop filter is used to stabilize the loop by introducing zeros and poles into the loop. The loop filter, oscillator, reference oscillator, phase detector and feedback frequency divider together comprise a PLL frequency synthesizer.

The accuracy, channel spacing, phase noise, side bands and lock time are main performance parameters of a PLL frequency synthesizer and require careful considerations throughout the system, circuit and layout designs.

6.2 Charge Pump PLL

Charge pump PLL frequency synthesizer is widely used for its simple structure and good performance. Compared with conventional multiplier PLL or XOR phase detector PLL, it has three main advantages: (1) The output of voltage controlled oscillator determines the lock range of charge pump PLL and its lock range is wide and no mis-lock phenomenon;(2) If the mismatches and offsets of the two branches currents are neglected, the static phase error is zero when in lock mode; (3) The certain amount of time to lock on the frequency of an incoming signal is short and the synthesizer's switching speed is fast. Moreover, the open-loop transfer function of it has two poles at the origin and root locus shows that more stability of the PLL is achieved with the increasing loop gain. [32]

A charge pump PLL is composed of a phase and frequency detector (PFD), charge pump, loop filer and VCO as shown in figure 6-2.

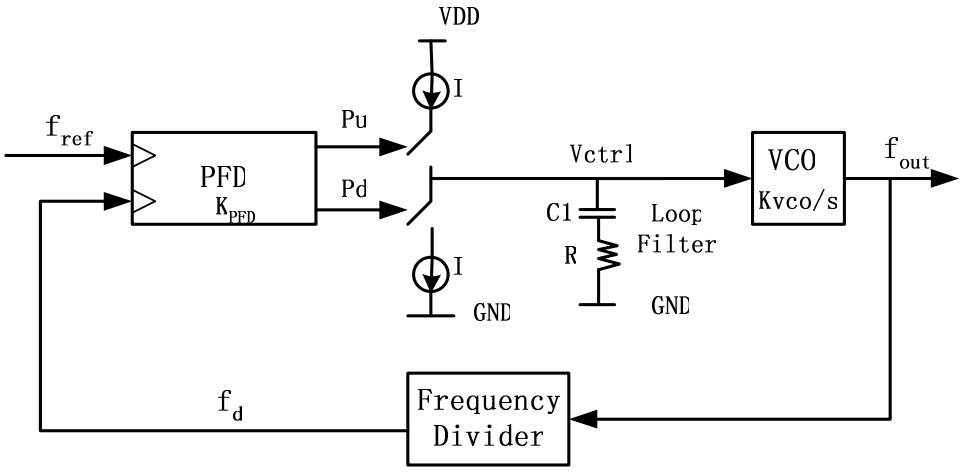


Figure 6-2 Charge pump PLL.

The basic work theory of charge pump PLL is that tow current sources controlled by the outputs of PFD charges and discharges the loop filter capacitors to generate the voltage control signal to VCO. The PFD transforms the phase or frequency error signal to two switching signal Pu and Pd with corresponding pulse width. For example, when the VCO frequency is lower than reference signal, Pu is high and the up switch is closed for the current source charges the capacitor and make the voltage control signal go high. In the way, VCO frequency is tuned higher. It works vise versa.

The whole loop dynamics can be analyzed by the linear mode of each component inside the PLL. The PFD has a gain of K_{PFD}, the loop filter has a transfer function F(s), and the VCO has a gain of Kvco(Hz/V). For the fact that phase is the integration of frequency, an integrator 1/s is included to the VCO transfer function so that VCO has a gain of Kvco/s. Suppose the loop has a phase error ϕ_{ref}-ϕ_d=ϕ_e. The average current charging the capacitor is given by $I\phi_e/(2\pi)$. The average change in the control voltage after the loop filter is:

$$V_{ctrl}(s) = I\phi_e(R + 1/sC_1)/2\pi \qquad (6.1)$$

The output phase from VCO is thus:

$$\phi_{out}(s) = V_{ctrl}(s) Kvco / s \tag{6.2}$$

$\phi_{out}(s)$ is also the open loop transfer function and it has two poles at the origin.

The closed-loop transfer function of the PLL is

$$H(s) = \frac{\phi_{out}(s)}{1 + \phi_{out}(s)} = \frac{I \cdot Kvco(RC_1 s + 1)/(2\pi C_1)}{s^2 + I \cdot Kvco \cdot R \cdot s/(2\pi) + I \cdot Kvco/(2\pi C_1)} \tag{6.3}$$

The loop transfer function has a zero at $\omega_z = -1/(RC_1)$.

The second order system has two parameters;

$$\omega_n = \sqrt{I \cdot Kvco/(2\pi \cdot C_1)} \tag{6.4}$$

$$\zeta = (R/2) \cdot \sqrt{I \cdot C_1 \cdot Kvco/(2\pi)} \tag{6.5}$$

Suppose the divider modulus changes form M to M+k and k<<M, the frequency settling time inside the loop is:

$$t_s \approx (1/\zeta \cdot \omega_n) \ln(k/(M|\alpha|\sqrt{1-\zeta^2}) \tag{6.6}$$

In which the decay time constant is $(1/\zeta \cdot \omega_n) = 4\pi/(R \cdot I \cdot Kvco)$ and it is independent of C_1.

Increasing the ω_n can lead to the increase of loop bandwidth and thus shorten the settling time. This can be achieved by increasing the pump current I and VCO's coefficient Kvco as shown in 6-4. However, loop would become unstable when the ω_n becomes comparable with the input reference frequency. Usually, loop bandwidth ω_n should meet equation (6.7) for the stability of the loop. [33]

$$\omega_n^2 < \omega_{ref}^2 / (RC_1 \omega_{ref} \pi + \pi^2) \tag{6.7}$$

The loop filter in figure 6-2 indicates that the loop is a second order system. In practice, another capacitor C_2 is added in parallel to the R and C_1. C_1 produces the first pole for the

loop filter and this is the largest capacitor. C_2 is used to smooth the control voltage ripples and to generate the second pole. This modification leads the system to a third order system. [34]

6.3 Fractional-N Frequency Synthesizer

Replacing the integer-N divider with fractional frequency divider in the feedback of PLL, we can get fractional-N type frequency synthesizer as shown in Figure 6-3. The fractional divider is usually a multi-modulus divider (MMD). A modulus control signal is used to toggle different modulus at each reference period.

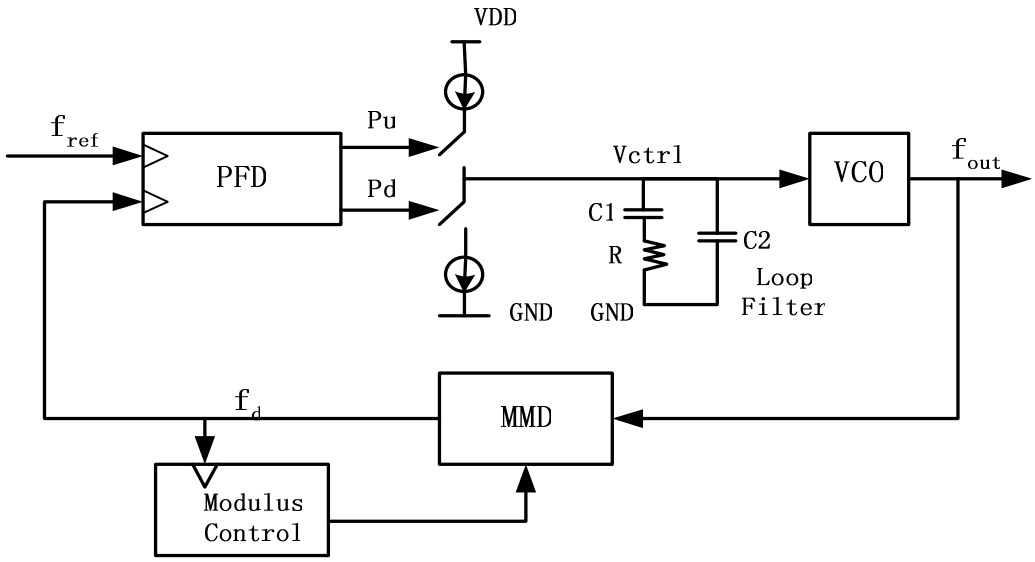


Figure 6-3 Fractional-N PLL frequency synthesizer.

For a two modulus divider case, the divider can divide the input signal form VCO by *N* or *N*+1. Assume that the divider divide By *N* for *L* reference cycles and *N*+1 for *M* reference clock cycles. The N_{avg} is defined as the average division ratio:

$$(L+M)/f_{ref} = (N \cdot L + (N+1) \cdot M)/f_{out} \tag{6.8}$$

$$N_{avg} = f_{out} / f_{ref} = N + M /(L + M) \quad (6.9)$$

The fractional division ratio makes the frequency step be a fractional of reference signal. A fractional-N synthesizer can have a higher reference frequency and hence higher loop bandwidth without stability problem. Thus it decreases the settling time of the PLL, the noise contributed by the VCO, and the in-band portions of the noise contributed by the reference source, the PFD, the charge pump, and the divider.

Under this condition: $N>>1$ and $\alpha<<1$, $N+\alpha=N$, The delta-sigma fractional-N PLL loop dynamics and stability issues are identical in delta-sigma fractional-N PLL and integer-N PLL. This is because that each phase noise transfer function in an integer-N PLL is same as the corresponding phase noise transfer function in a delta-sigma fractional-N PLL.

In phase-locked loop, the divider output positive edge is separated from the VCO edge by a phase offset (propagation delay). Ideally, this propagation delay is constant if it is independent of the corresponding divider modulus and it does not contribute to the phase noise. Delta-sigma fractional-N PLL has a multi-modulus divider. The modulus dependent divider delays and the nonlinearity introduced by multi-level delta-sigma modulator's output would increase the PLL's phase noise.

One solution is to use a delta-sigma modulator with single-bit quantization. But as discussed before, this would cause decreased nose shaping effect of the modulator. Higher order modulator works but still needs to meet required dynamic range.

One solution is to resynchronize the divider output to the nearest VCO edge or at least a higher-frequency edge obtained from within the divider circuitry [35][36].This can get rid

of the modulus dependent delays but it takes more power consumption.

6.4 Fractional Spurs

The alternation modulus of the divider cause the output frequency to vary between $N \cdot f_{ref}$ and $(N+1) \cdot f_{ref}$ and during each reference period the difference between the actual divider modulus and the average represents error that gets injected into the PLL and results in increased phase noise. The error is periodical and can generate spurious tones at the fractional offset frequency. If the fractional frequency is low and falls inside the loop bandwidth, large spurious tones appear. One way to suppress these tones is have a very small PLL bandwidth, which negates the potential benefit of the fractional-N technique.

There are several methods to suppress these spurs and one is known as the “fractional compensation”. If the divider's alternating modulus is deterministic, the current generated by the charge pump can be compensated by another current pulses that with the same alternating process but an opposite sign. [37] This technique depends on highly accuracy of the compensation currents.

The other way to eliminate fractional spurs is to randomize the sequence of the modulus so as to break up their periodicity. With the randomness of the modulus, the average division modulus can still be achieved and the fractional spurs are converted into white noise. The white noise inside the PLL’s bandwidth is integrated by the PLL transfer function and introduces phase noise contribution no mater what PLL bandwidth is.

Delta-sigma fractional-N PLL can solve this problem by shaping the noise spectrum to higher frequency offsets. It generates the sequence of modulus such that the quantization

noise has most of its power in a frequency band well above the desired bandwidth of PLL.

Chapter3 has discussed the details of the work mechanism of delta-sigma modulator. With a linear model of delta-sigma modulator, the input sequence of delta-sigma modulator x[n] is coarsely quantized into integer-valued y[n] that has the form:

$$y[n]=x[n]+eq[n] \tag{6.10}$$

where eq[n] is the quantization noise introduced inside the modulator and has most of its power at high frequency offset.

In order to make white noise of quantization noise model hold, a pseudo-random sequence is usually added to the modulator as described in chapter 3. Its amplitude should be small so it does not appreciably increase the phase noise of the PLL.

Suppose x[n] represents an average modulus $N+\alpha$, y[n] thus represents the $N+\alpha+eq$. Writing them in continuous time domain, therefore:

$$f_d(t) = f_{out}(t)/(N+\alpha+eq(t)) \tag{6.11}$$

The noise in f_d is thus:

$$\begin{aligned} n_f(t) &= f_{out}(t)/(N+\alpha) - f_{out}/(N+\alpha+eq(t)) \\ &= (f_{out}(t)/(N+\alpha)) \cdot (eq(t)/(N+\alpha+eq(t))) \end{aligned} \tag{6.12}$$

By making use of the approximation, $eq(t) \ll N+\alpha$, we can rewrite (6.12) to (6.13):

$$n_f(t) = (f_{out}(t)/(N+\alpha)) \cdot (eq(t)/(N+\alpha)) \tag{6.13}$$

Assume $\alpha \ll N$ the power spectrum density of the noise is :

$$S_{nf}(f) = {f_{out}}^2/(N+\alpha)^2 \cdot |Q(f)|^2 / N^2 \tag{6.14}$$

where Q(f) is the spectrum of eq(t) which has high noise shaping effect and the noise in the synthesizer has the same spectral shape as quantization noise Q(f) can be filtered by the

PLL system transfer function.

Different types of delta-sigma modulators with different order have different effects on the phase noise performance of the PLL output.

6.5 Delta-sigma Modulation in Fractional-N PLL

For fractional-N frequency synthesis, several types of delta-sigma modulators have been used such as MASH, feed-forward and error feedback. Feedforward modulators are most often used for it can have a single-bit or a multi-bit output depending on the quantizer inside the loop. Besides, the in-band and out-band noise shaping effect can be tune with different feed forward coefficients. Higher order modulator can have much sharper in-band noise shaping effect but it also has a higher out-band quantization noise. Extra poles are needed in loop to suppress the noise at high frequencies.

6.5.1 Dynamic Range of Modulator

From the viewpoint of the dynamic range requirement of delta-sigma modulator, it needs high over-sampling ratio for a fixed modulator's order. The loop bandwidth of PLL determines the over-sampling ratio.

$$OSR = f_{ref} /(2 f_{loop}) \tag{6.15}$$

Thus the loop bandwidth has an upper bound limit.

In [19] , it gives an approximate upper bound of the bandwidth:

$$f_{loop} < \left[\left(\frac{\theta_{rms}}{\sqrt{2}} \right)^2 \cdot \frac{L+0.5}{(2\pi)^{2L}} \right]^{(1/2L-1)} \cdot f_{ref} \tag{6.16}$$

where L is the order of the delta-sigma modulator, θ_{rms} is the integrated phase error [rms rad] for synthesizer.

From equation (6.16), we can see that high order L of delta-sigma modulator is necessary for the loop bandwidth can be increased.

6.5.2 Multibit Quantizer

A high-order modulator with single-bit quantizer has a dead-band problem due to the limited input range of the quantizer in synthesizer. For a fixed input range, the quantization noise decreases with the increase of quantization bits in the quantizer. One additional bit in the quantizer reduces the noise lever by 6dB. Moreover, the performance of the modulator with multibit quantizer follows the linear model more closely than that of the single bit modulator. Hence, delta-sigma modulator with multi-bit quantizer tends to be more stable. With the number of quantizer levels increases, the maximum pass-band gain of the noise transfer function (NTF) can be increased without causing any nonlinear stability problem. As the maximum pass-band gain of the NTF increases, the corresponding corner frequency increases. The quantization noise of the third-order modulator can be further suppressed by 16 dB with a 2-bit quantizer, 22 dB with a 3-bit quantizer, and 25 dB with a 4-bit quantizer. [38]

6.5.3 NTF Optimization

The third-order feed-forward delta-sigma modulator takes its advantage in moving its poles inside the unit circle in the z-domain by changing its feed-forward coefficients. For

hardware implementation, these coefficients are chosen to be the multiples of 0.25 for easy implementation using shift operations.

The NTF design goal is to get more shaper noise shaping in-band to be close as MASH, feedback which has the sharpest noise shaping effect. Meantime, it needs to constrain the out-band noise so as to suppress the output bit pattern. Due to its high out-band noise, MASH has the widest the bit pattern which ranges for N-3 ~ N+4. Wide spread output bit pattern makes the synthesizer more sensitive to the substrate noise coupling since the modulated turn-on time of the charge pump in the locked condition increases.

We propose new feedforward coefficients $k_1 = 2$, $k_2 = 1.75$, $k_3 = 0.5$ for third order feed-forward delta-sigma modulator (figure 6-4). It has sharper in-band noise and less out-band noise compared with the existing feedforward type [19] and MASH type (Shown in figure 6-5).

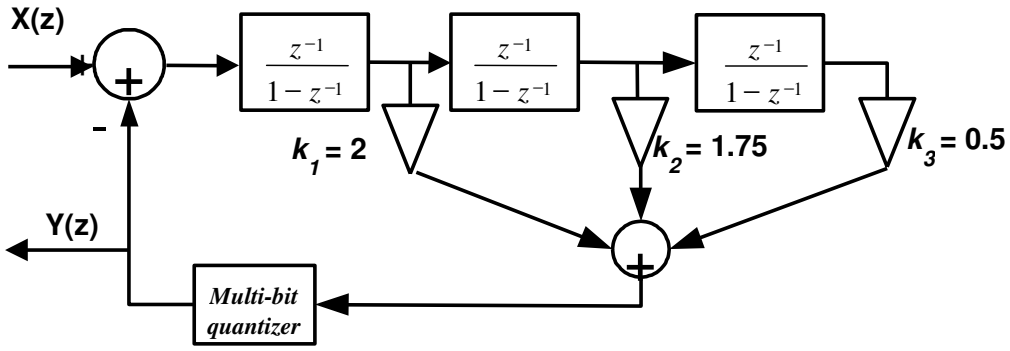


Figure 6-4 Block diagrams illustrating the proposed 3rd order feedforward delta-sigma modulators in PLL.

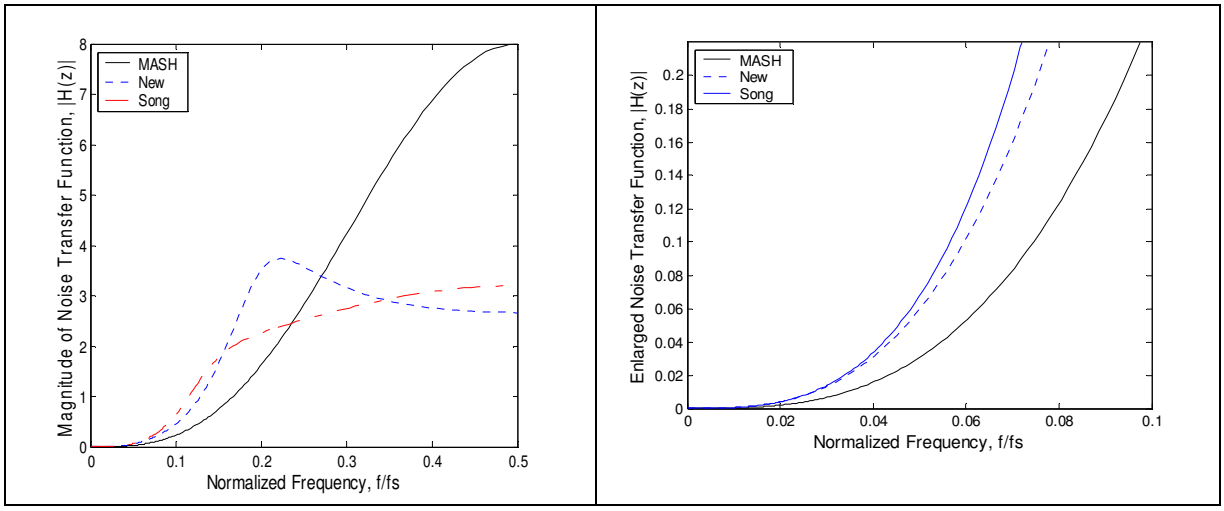


Figure 6-5 Simulated noise transfer function of MASH and feedforward delta-sigma modulators ($k_1 = 2$, $k_2 = 1.75$, $k_3 = 0.5$).

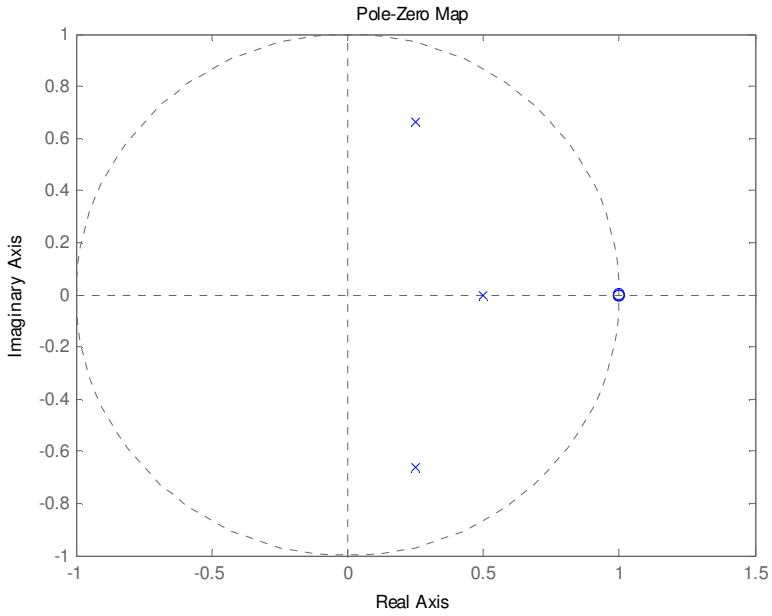


Figure 6-6 The PZ map of the new transfer function (Stable).

Another design example shown in figure 6-7 by setting k_1=1.75, k_2=1, k_3=0.25, It has much more less power in high frequency and leads to less output bit pattern.

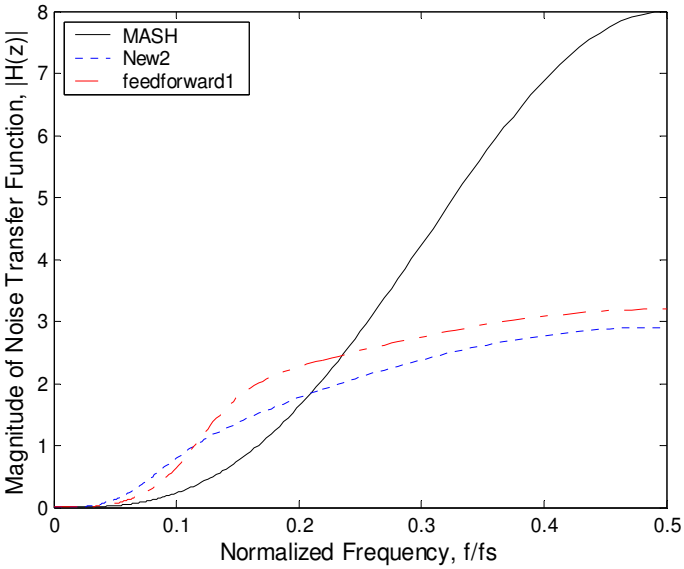


Figure 6-7 Simulated noise transfer function of MASH and new feedforward delta-sigma modulators (k_1 = 1.75, k_2 = 1, k_3 = 0.25).

6.6 Digital Modulations in PLL and Band-Widening Techniques

Conventionally, digital modulated signals can be converted into analog baseband signal using a DAC. The analog signal can be up-converted to IF an RF signal by mixed with frequency synthesizer's output. This approach requires high performance of DAC and filters and not easy for integration (shown in figure 6-8).

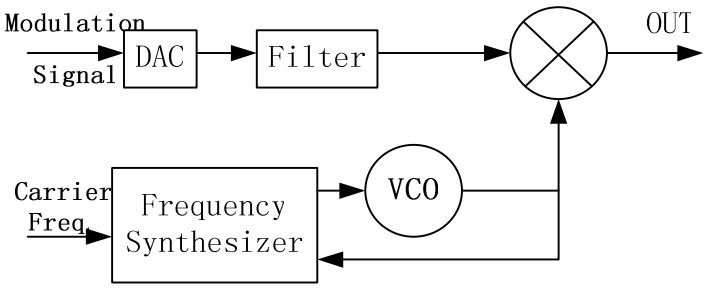


Figure 6-8 Modulation frequency up-conversion using mixer.

Digital modulation can be combined into frequency synthesizers. Many kinds of modulation techniques such as FSK, GMSK have been implemented in DDS in either

frequency or phase domain. [23]

For PLL type frequency synthesizer, the modulated signal can be generated by modulating VCO to eliminate the need of conventional up-conversion stages.

There're two ways so far published to realize this idea. One is to use the open-loop VCO modulation which is presented in [39] for a DECT (Figure 6-9).

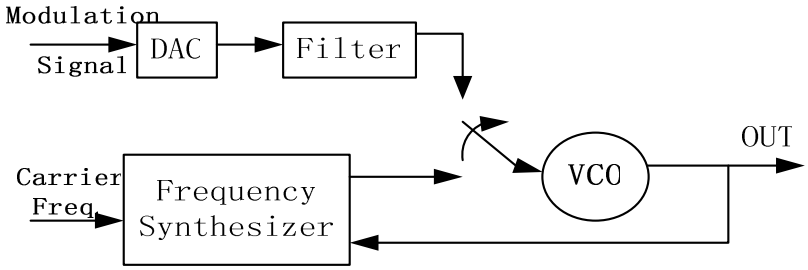


Figure 6-9 Modulation frequency up-conversion using direct modulation of VCO.

The accurate frequency is set to a reference frequency by enclosing the VCO within a PLL loop. During the signal transmission step, the VCO is disconnected from PLL and the modulation is fed directly into its input. This technique does not need mixers and only one DAC is needed to produce the analog modulation signal. Components reduction leads to power reductions. The limitation of this technique is the VCO frequency drift because of leakage current during inactive mode. In addition, it is highly sensitive to noise and perturbations from other circuits and thus shift the output frequency. The required level of isolation excludes the possibility of a one-chip solution.

The indirect modulation of VCO through delta-sigma fractional-N synthesizers can overcome these problems caused by direct modulation of VCO. The digital modulation signal such as GMSK is summed with the common divider and fed into the delta-sigma modulator which controls the instantaneous divide value of the PLL. The common divider

value sets the carrier frequency, and variation of the divide value causes the output frequency to be modulated according to the input modulation signal. (shown in figure 6-10)

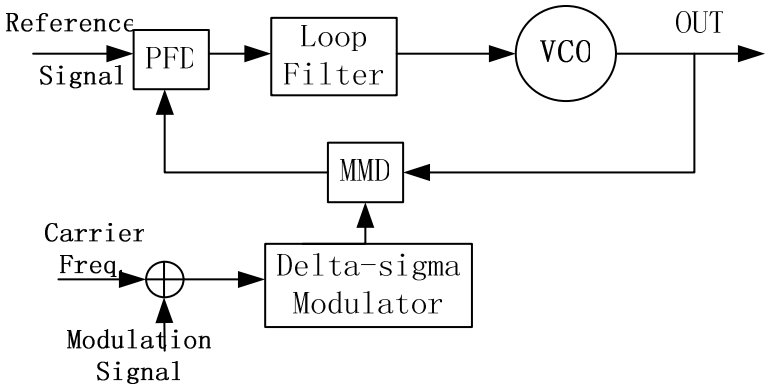


Figure 6-10 Modulation frequency up-conversion using indirect modulation of VCO.

The synthesizer has a digital input and conventional DAC is no longer needed. Since the VCO is always control by the synthesizer, the problem of frequency drift during modulation is solved. The primary limitation of transmission rate of modulation signals due to the bandwidth of PLL itself. An enough bandwidth is needed for modulation signal to pass and big bandwidth allows for high transmission rate. On the other hand, the bandwidth of the PLL should be narrow enough to suppress the quantization noise from the delta-sigma modulator to reach the requirement of phase noise.

Several solutions have been proposed to widen the PLL loop bandwidths. One is the digital compensation method to the digital modulation signal prior to the delta-sigma modulator [40]. The compensation filter has a high-pass filter response that is cascoded with the low-pass loop filter. The transfer function seen by the modulation date can be made flat by setting the compensation transfer function the inverse of the closed loop filter. However, due to the analog dynamics of the PLL, mismatches would occur between the

compensation filter and PLL loop filter. Another solution is increasing the order of delta-sigma modulator to reduce in-band quantization noise [41]. This allows the loop bandwidth to be increased without increasing the total phase noise. But the out-band quantization noise would be higher. One way to solve it is to design the noise transfer function of the delta-sigma modulator to achieve both reduced noise in-band and out-band. The other way is to increase the order of loop filter to increase the attenuation of out-of-band quantization noise. The third method [42] proposed is to keep the loop bandwidth low, but modulate the VCO both through delta-sigma modulator and through an auxiliary modulation port at the VCO input. This is to apply the low-frequency modulation signal to the delta-sigma modulator while high frequency components to the VCO.

6.7 Circuit Design of a Fractional-N PLL in SOI

6.7.1 SOI Technology

Silicon on insulator (SOI) technology has come into being for more than 30 years. Compared with bulk CMOS, it takes advantages in full dielectric device isolation, less junction capacitances, lower average device threshold voltages, less body effect and source follower effect. The insulator layer reduces the thermal conductivity in SOI leading to possible reliability issues. Meantime, it keeps the easy scalability of bulk CMOS and can achieve high packing density. For RF circuit design, substrate-coupled noise has been a persistent noise problem and it limits the integration in mixed signal circuits that has both analog and digital circuits. SOI is well suited to solve this problem for its intrinsic body isolation.

6.7.2 SOI Devices

SOI devices are built on a thin silicon layer placed upon an insulator. This is the main difference from bulk CMOS. Almost same bulk CMOS process can be used to fabricate devices such as FETs, diodes and resistors. A cross-section of an SOI NMOS is shown in Figure 6-11 [43].

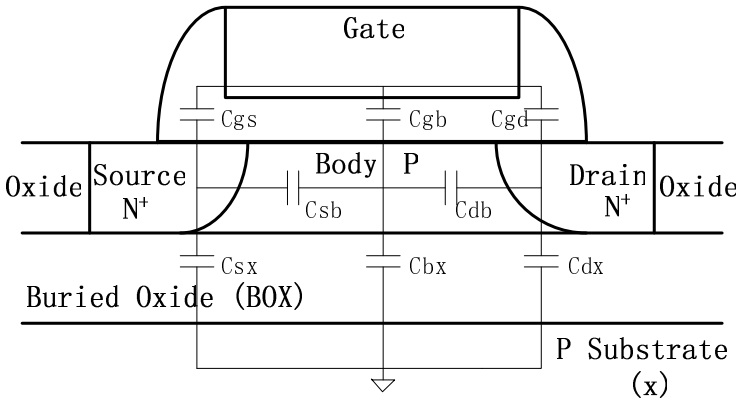


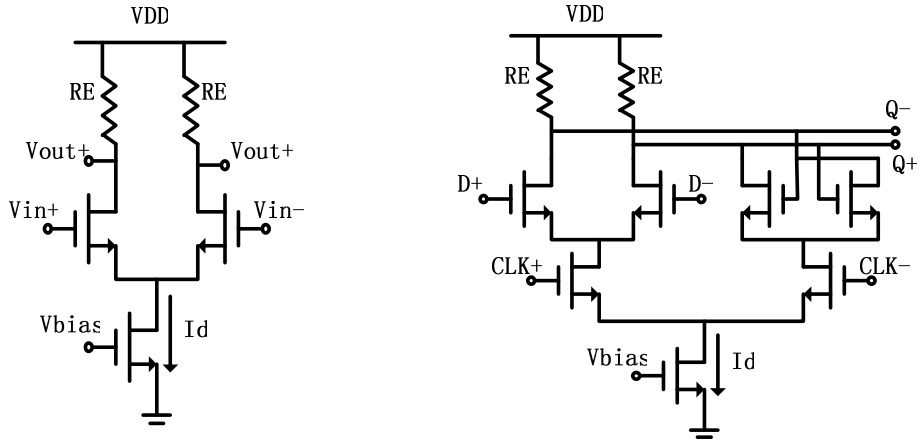
Figure 6-11 Cross-section of SOI NMOS.

An insulating region that is made of silicon dioxide is formed beneath the devices. Usually, a technique named Separation by the Implantation of Oxygen (SIMOX) is performed on an epitaxial wafer. It forces a large dose of oxygen deep beneath the surface of wafer and creates the BOX after annealing shown in Figure 6-11. After that, silicon layer is placed on the buried oxide and insulated with silicon dioxide on both sides. Depending on the thickness of the silicon layer, two major approaches, differentiating the manufacturing process and the circuit characteristics, are distinguished. One is partially depleted structure and the other is fully depleted structure. For partially depleted (PD) SOI the depletion region extends into the body of a FET under the gate at the source-body and drain-body junctions, It does not deplete the all of the charge in the body. The silicon layer

is around 150nm. The fully depleted (FD) SOI exhibits a very thin (<50nm) silicon layout, so that the depletion region extends through the entire layer. In this way, it minimize the floating body effect and allows the depletion regions from the source to body and from the drain to body regions to fully deplete the body of mobile charge under all bias conditions. The thickness of a FD device determines the threshold voltage of the device and is a manufacturability issue. As in bulk CMOS, a MOS device is defined by the intersection of active and poly. In SOI, the active area corresponds to a thin silicon island, which is doped with a threshold adjust implant NMOS or PMOS device, respectively. The source and drain extension implants and the source and drain degenerate implants are both controlled using the N and P implantation. An issue addressing SOI is the floating body effect which can be controlled by "Special Purpose MOS Structures" such as T, H type to make good body contacts. However, all these special structure are at a cost of increasing area. There're two kinds of resistors in SOI, one is the buried resistor which is a depletion MOS device with its gate tied to the source. The resistance is determined by the channel region of the device. The other is the poly-silicon resistor. Diode is made in SOI just like FET, the diffusions that would normally be the source and the drain of the FET are now the anode (P+) and the cathode (N+). Decoupling capacitor provides accumulation capacitance using the thin oxide of the FET. The source and drain are grounded and hence the NWELL is grounded and the gate is tied to VDD. For the poly-bounded diode, the resistance of body is large and the distance between the source and drain should be kept small to alleviate this problem.

6.7.3 MOS Current Mode Logic

MOS Current Mode Logic (MCML) circuits are able to operate with lower signal voltage and higher operating frequency at lower supply voltage. The speed bottleneck PMOS is no longer needed.



(a) Buffer (b) Latch

Figure 6-12 MOS Current Mode Logic.

Figure 6-12 shows the base logic buffer and latch used in the logic cells design. It contains common source NMOS current switching pairs and a tail current source. The pull up resistor *RE* and tail current *Id* determines the swing range of the differential signal which is 400mV. So *RE*=200mv/*Id* when Id is determined. The supply voltage is 1.5V and Vbias voltage is 0.6V for NMOS with 0.2um length. Different biasing current is got by changing the width of transistor from 1.2um to 8um. The biasing current ranges from 85uA to 400uA respectively.

Trans-conductance *gm* in forward-active operation region

$$g_m = \mu C_{ox} \frac{W}{L}(V_{GS} - V_t) = \sqrt{2 I_D \mu C_{ox} \frac{W}{L}} \tag{6.16}$$

The delay between the logic cells can be approximately as $0.69RE \cdot C_{eff}$ [45]and C_{eff} is a

combination the load capacitance which includes C_{gs}, C_{gd} and C_{g}b of NMOS transistors. The transition frequency which is the frequency of unit current gain is a mark of the transistor's speed.

$$f_T = \frac{1}{2\pi} \cdot \frac{g_m}{C_{gs} + C_{gd} + C_{gb}} \tag{6.17}$$

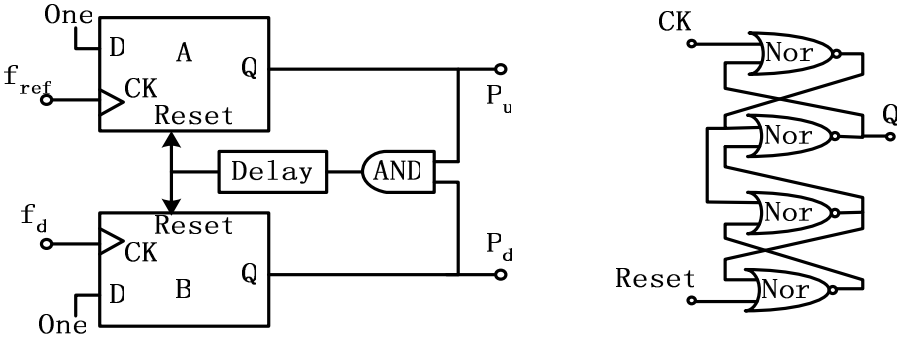
SOI technology takes it advantages in reduced these parasitic capacitance and for an AND gate it delay is below 0.1ns. Besides, the ripple effect caused by the inductive output of a level-shifter is also greatly reduced in SOI for its small parasitic capacitance.

Basically, if one logic cell needs to drive the next stage, the current ratio between first stage and all the next stage is around 1:4.

6.7.4 Phase Frequency Detector

The phase-frequency detector (PFD) is to detect both the phase and frequency differences of the reference signal and the divided VCO signal. It employs two employs two edge-triggered, re-settable D flip-flops with their D inputs connected to logic high. Reference signal fref and the divided VCO sign fd act as the clock input of the two flip-flops. In MOS technology, a simple realization of this kind of D flip flop is shown in figure 6-13. The outputs QA and QB are called the UP and DOWN signals to drive the nest stage. If QA=QB=0, a low-to-high transition on f_{ref} would cause QA to go high. Subsequent transitions on fref would have not effect on QA. when B goes from low to high, the AND gate activates the Reset of both flip-flops. QA and QB are both high for a duration of the total delay of AND gate and reset path of D flip flops. The advantages of

the PFD are the improved acquisition range and clock speed as it detects both the frequency and phase. Meanwhile, it has a constant over the phase error range -π~+π. The PFD suffers from a dead zone problem when the delay between UP and DOWN signals becomes comparable to their switching delay in the vicinity of the lock condition and this would cause jitter in the output.



(a) PFD (b) DFF

Figure 6-13 PFD and its D flip-flop implementation.

In order to solve this problem additional delays (buffers) are added into the reset path to make the delay time bigger. A Simulation the PFD output with input frequency of A_{in} is faster than that of B_{in} is shown in figure 6-14.

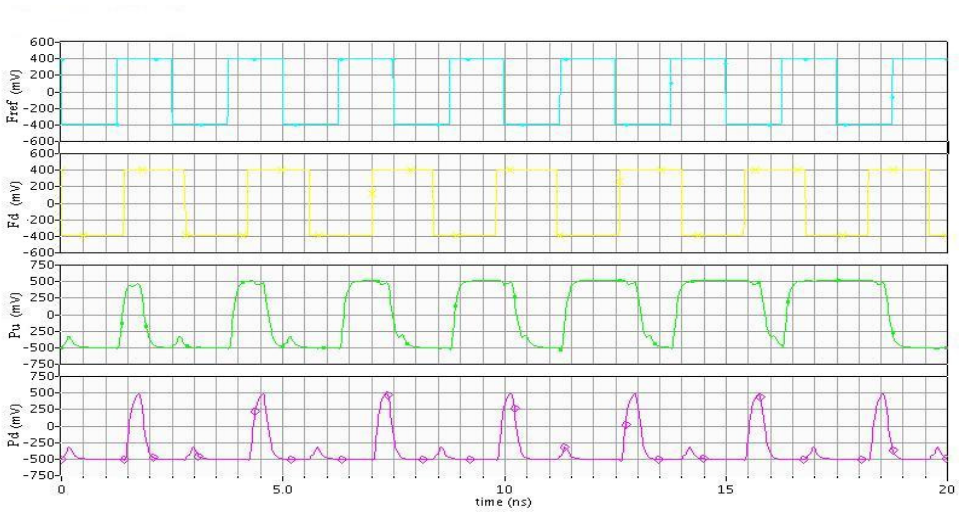


Figure 6-14 PFD simulation results.

6.7.5 Charge Pump and Loop Filter

The function of charge pump and loop filter is to convert the output of PFD into the DC control signal for the VCO. The average of the PFD output is obtained by depositing or decaying charge onto a capacitor during each phase frequency comparison.

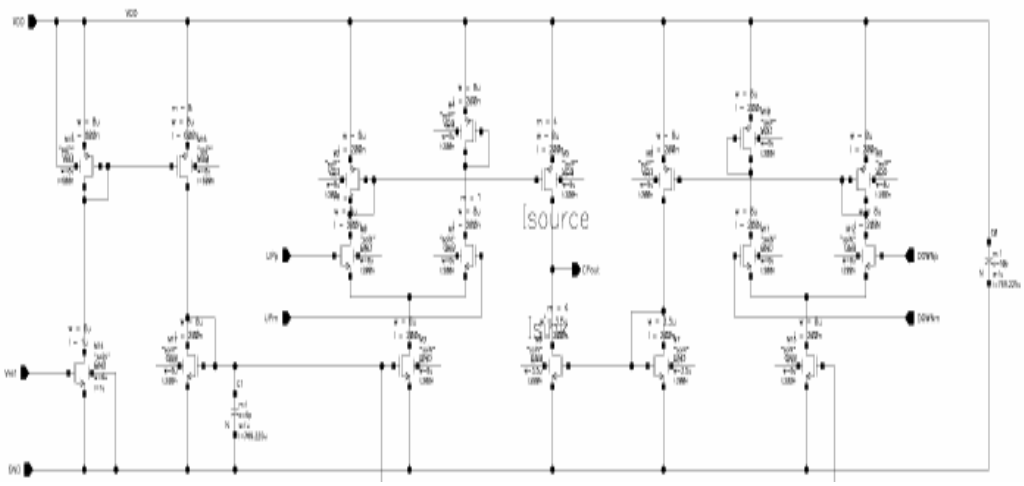


Figure 6-15 Charge pump schematic.

Shown in Figure 6-15, two differential switch pairs Pu and Pd form PFD are used to switch on and off the two current sources *Isource* and *Isink* to charge and discharge the capacitor. In PLL lock condition, the switches Pu and Pd turn on at every phase comparison instant. Any mismatches between their magnitudes, duration or absolute timing results in a net current that is drawn from the loop filter.

The low output impedance of M1 and M2 in Figure 6-15 also can cause ripples in the control voltage especially when *Vcont* is below few hundred millivolts [46] This effect creates additional mismatch between the up and down currents as a function of Vcont and lead to larger reference sidebands. Cascode structure can enhance the output resistance and alleviate this problem.

As discussed before, an additional capacitor C_2 is added in parallel with C_2 and R in

order to suppress the unwanted ripples. The loop filter's transfer function is

$$H_{loop} = \frac{1}{C_1 + C_2} \cdot \frac{1 + sRC_1}{s[1 + sRC_1C_2/(C_1 + C_2)]} \tag{6.18}$$

The frequency response has one zero at $1/RC_1$ and this make the circuit act like an integrator at low frequency. The pole that determined the loop bandwidth is $1/RCs$ where $Cs=C_1C_2/(C_1+C_2)$. The value of C_2 is usually less than 1/5 of the C_1 for not increasing the loop settling time. For a 20MHz crystal input reference, the loop bandwidth should keep around 1/10 to guarantee the loop stability. Here, we pick R=100, C_1=5.66nF, C_2=566pF to get a loop bandwidth 2.5MHz. The whole PFD, charge pump simulation is shown in Figure 6-16.

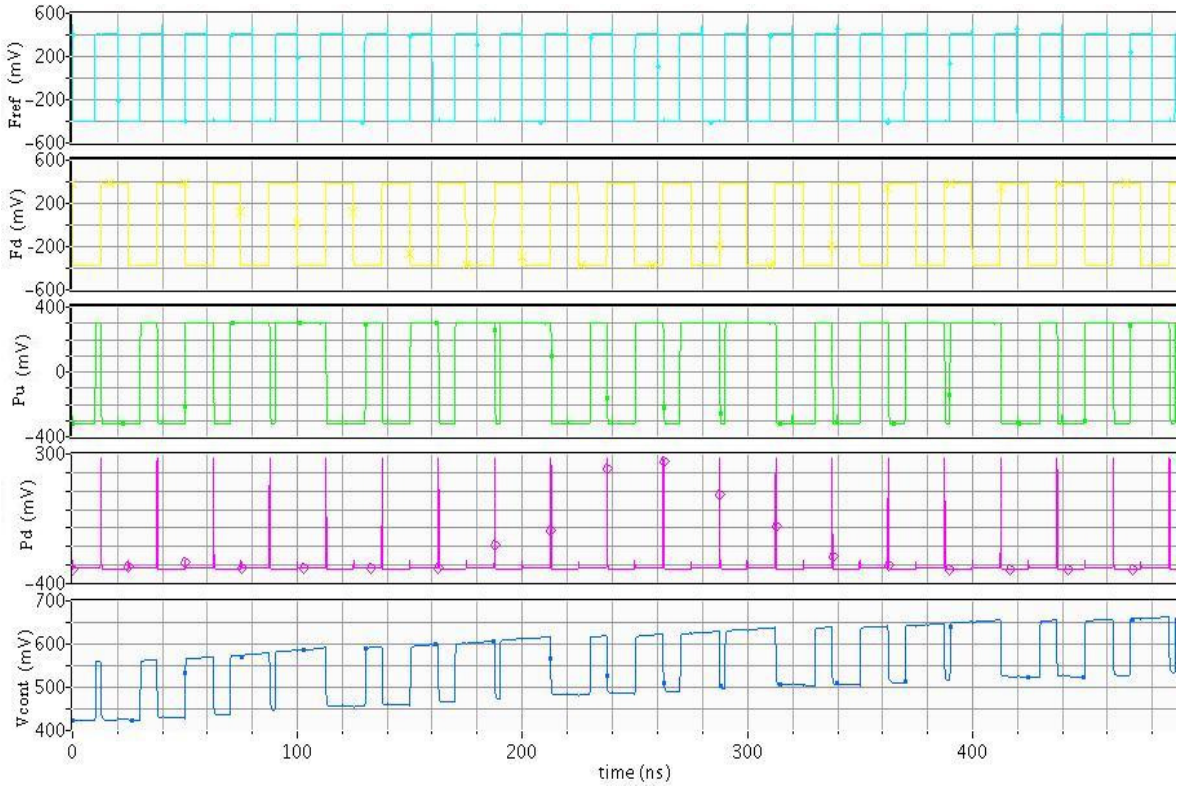


Figure 6-16 Charge pump simulation results.

6.7.6 Multi-Modulus Divider

The multi-modulus divider (MMD) is capable of supplying programmable modulus to divide the output of VCO. The modulus is determined by its control bits and the division range becomes wider as the control bits increase. The flexibility of changing modulus with input control bits also an interesting attribute for delta-sigma modulation in fractional-*N* PLLs so that multi-bit modulator's output can directly feed into the control bits of MMD. Meantime, speed and power consumption are important design issues we have to consider.

The MMD structure we use contains a chain of 2/3 divider cells as shown in Figure 6-17 [47].

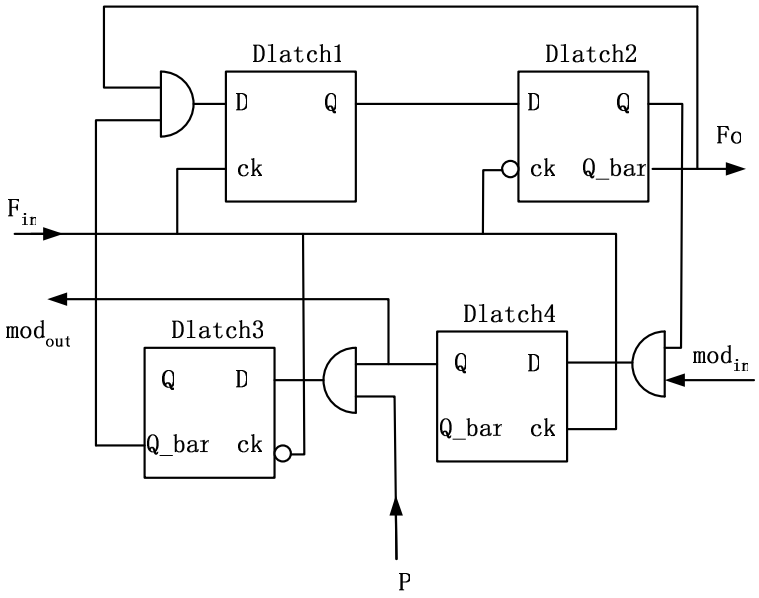


Figure 6-17 Divider by 2 or 3 cell.

The 2/3 divider comprises of 4 Dlatches and 3 AND gates. It has 3 inputs F_{in}, mod_{in}, P and 2 outputs Fo, mod_{out}. When input mod_{in} is zero the Fo is the Fin divided by 2. When mod_{in} becomes active, the state of the P input is checked, and if P=1, the Dlatch3, Dlatch4 and two down AND gates force the Dlatch1, Dlatch2 to swallow one extra period of the

input signal. In this way the cell divides the Fin by3. If P=0, the cell stays in division by 2 mode. Meantime, the mod_{in} signal is relocked by the F_{in} (faster clock) and outputs as mod_{out} to the preceding 2/3 divider cell. The basic logic cells such as Dlatch and AND are built in MCML logic as described in section 6.7.3. A simulation with input F_{in} running at 5GHz is shown in Figure 6-18.

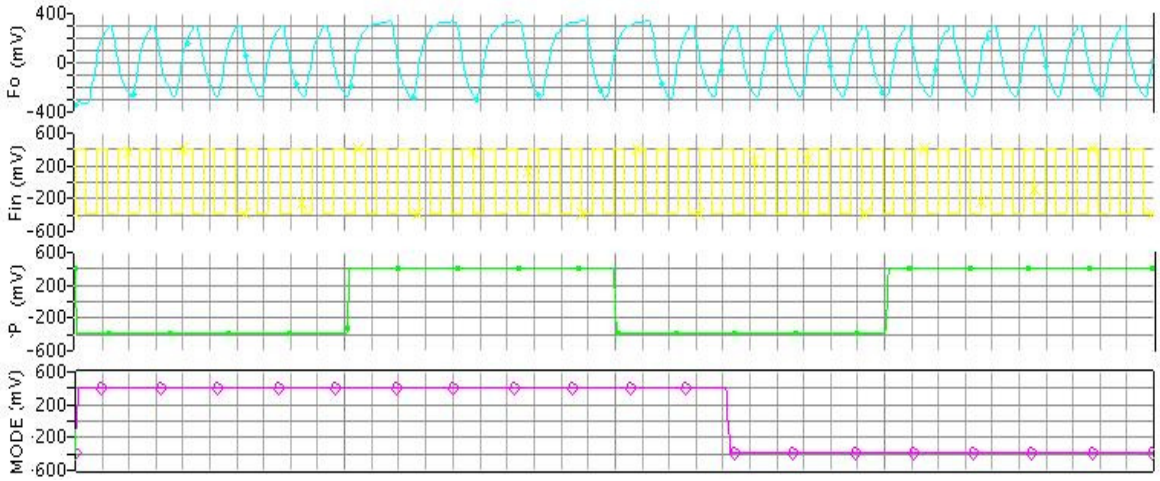


Figure 6-18 Simulation result of Divider by 2 or 3 cell.

The whole MMD structure that consists of same 2/3 divider cells is shown in Figure 6-19 [47]. The feedback signal mod is only between adjacent cells and this allows simple optimization of power dissipation. The work mechanism of MMD is as follows. Once in a division period, the last cell in the chain generates the signal mod_{out} which propagates back to the previous cell in the chain as its input mod_{in}. The mod signals between adjacent cells are reclocked by a faster Fin signal in each cell. Once a cell's input mod signal and P are both high, cell is to divide its input Fin by 3. Division by 3 adds one extra period of each cell's input signal to the period of the output signal. Hence, a chain of n 2/3 divider cells provides an output signal with a period of [47]

$$T_{out} = 2^n \cdot T_{in} + 2^{n-1} \cdot T_{in} \cdot P_{n-1} + 2^{n-2} \cdot T_{in} \cdot P_{n-2} + \cdots + 2 \cdot T_{in} \cdot P_1 + T_{in} \cdot P_0$$
$$= (2^n + 2^{n-1} \cdot P_{n-1} + 2^{n-2} \cdot P_{n-2} + \cdots + 2 \cdot P_1 + P_0) \times T_{in} \quad (6.19)$$

In equation (6.19), we can see that the MMD's division ratios range from 2^n (all P_n=0) to 2^{n+1}-1(all P_n=1).A control logic can be added to the MMD to extend the division range as shown in Figure 6-15. The control logic includes OR gates and it is to shorten the effective control bits length. For a 7-bit MMD design case, when P6 and P7 are zero, the effective bit length is shortened to 5. The division range is from 32~63. When P6 is one and P7 is zero, the effective bit length is 6 and the division range is from 64~127. When P6 and P7 are both ones, the effective bit length is 7 and division range is from 128~255.

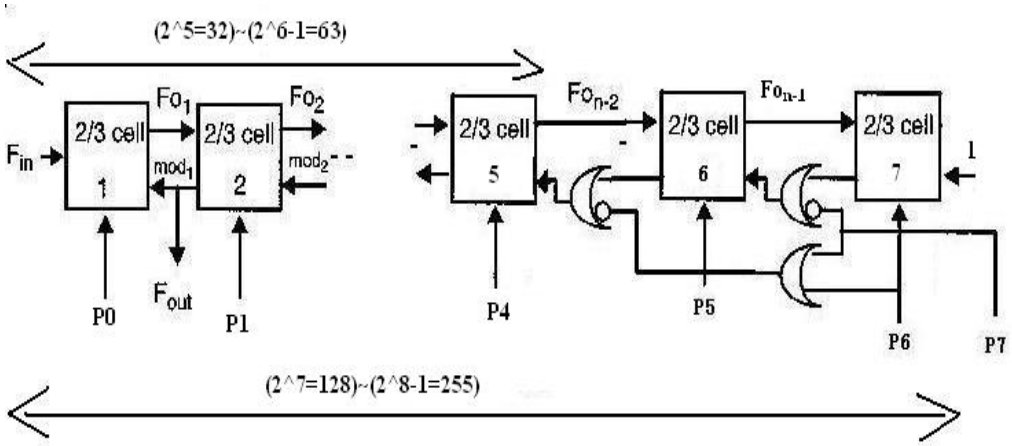


Figure 6-19 Multi-modulus divider.

Notice that the Fo signal from each cells runs at different frequency we can set different biasing current to each 2/3 divider cells to save power consumption. For the fastest cell1~cell4, the biasing current is set to be maximum 400uA. The rest cells that run at lower frequency have the biasing current 100uA. The whole MMD simulation is shown in Figure 6-20.

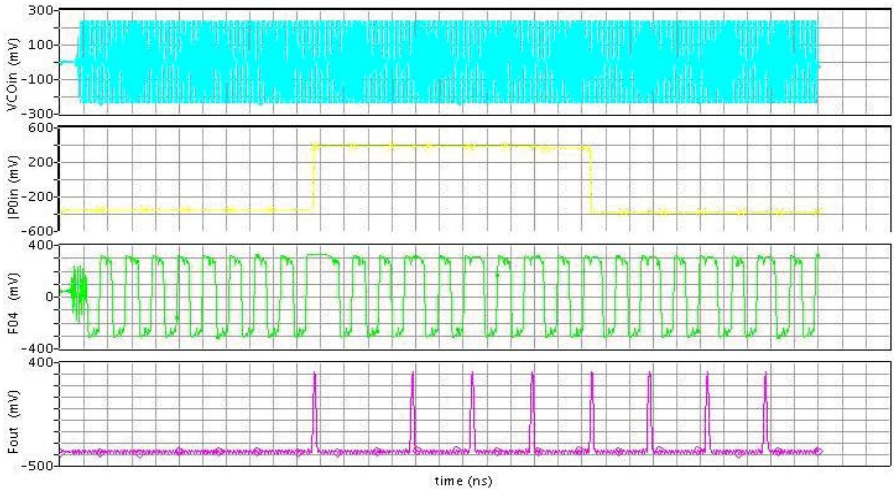


Figure 6-20 MMD simulation result.

6.7.9 Die Photo

The whole chip die photo is shown in Figure 6-21. It takes 2×2.3mm^2 and consumes 100mw (without VCO) under 1.5V power supply. It's under testing and measurement.

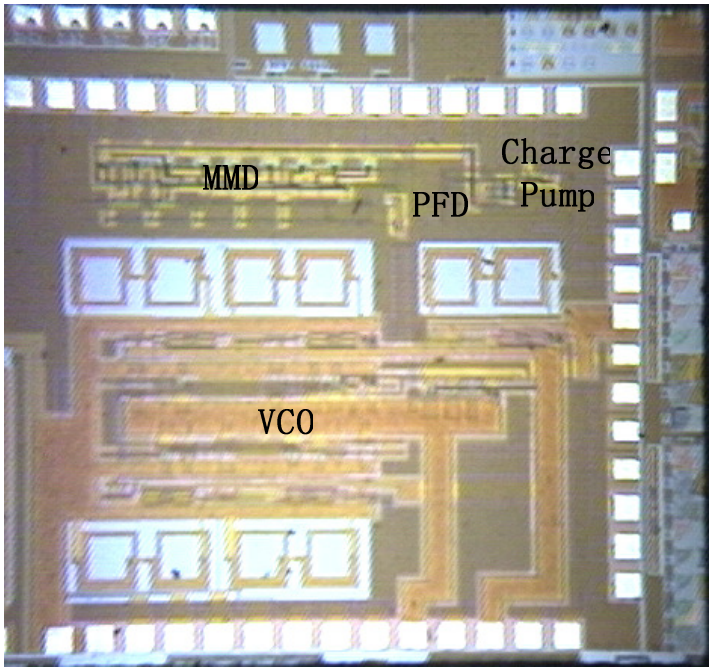


Figure 6-21 Die photo of the PLL in SOI.

6.8 Conclusion

This chapter presents a phase locked loop frequency synthesizer design. It uses the fractional-N type structure to get a relatively wide loop bandwidth of 2.5MHz. Third order feedforward type delta-sigma modulator with new feedforward coefficients k_1 = 2, k_2 = 1.75, k_3 = 0.5 are implemented. The noise transfer function of the modulator has constrained out-band noise in order to suppress the output bit patterns. SOI technology is employed due to the full dielectric device isolation, less junction capacitances, lower average device threshold voltages and less body effect and source follower effect. MOS Current Mode Logic (MCML) circuits are used to operate with lower signal voltage and higher operating frequency 5GHz at lower supply voltage 1.5 V.

CHAPTER 7 CONCLUSIONS

This dissertation is mainly focused on frequency synthesizer with delta-sigma modulations to get high quality output spectra.

For high speed DDS with nonlinear DAC. Structure selection is done for optimal SINAD and SFDR performance. With a phase bit L=16, truncation bit W=12 and nonlinear DAC bit D=11, the DDS can reach a 68dB SINAD in a band-with of $0.25f_{clk}$ and a SFDR of 70dB.

Delta-sigma modulators such as MASH, feed-forward, feedback and error feedback have been implemented in both phase and frequency domains in a CMOS DDS. The DDS prototype is fabricated in a 0.35μm CMOS technology with core area of 1.7x2.1 mm^2 and total 75 mA current. Measured DDS output demonstrates that frequency domain delta-sigma modulation achieves better SFDR and SINAD than phase domain delta-sigma modulation. A delta-sigma modulator which is a third order feedforwad type and with feedforward coefficients k_1=2.5, k_2=2.5 and k_3=1 is proposed. It has sharp in-band noise performance and flat out–of-band noise shaping effect. The in-band signal to noise and distortion ratio has 5dB increase with the claimed feedforward structure compared with the exiting structure [19].

RF circuit designs of high speed DDS building blocks in SiGe technology are presented. They include digital CML running over 20GHz, pipelined phase accumulators

running at 20GHz, carry look-ahead accumulator running at 10GHz, MASH 1-1-1 delta-sigma modulator running at 7GHz and a nonlinear DAC running at 10GHz.

A BIST approach using DDS is developed for analog circuit functional testing measurement of analog circuitry's linearity and frequency response including both phase and gain. The DDS-based test pattern generator is used to generate two frequency tones required in the two-tone linearity test as well as single tones for frequency response measurements. The efficient output response analyzer consisting of a multiplier and accumulator avoid using traditional FFT-based spectrum analysis which consumes much more power and die area. We have implemented the BIST approach in Verilog which was subsequently synthesized into an FPGA and verified on actual hardware with close agree to traditional measurement techniques and simulations.

In the end, a fractional-N phase locked loop frequency synthesizer is implemented in a 90nm SOI technology. It uses third order feedforward type delta-sigma modulator with new feedforward coefficients $k_1 = 2$, $k_2 = 1.75$, $k_3 = 0.5$. The noise transfer function of the modulator has constrained out-band noise in order to suppress the output bit patterns. MOS Current Mode Logic (MCML) circuits are for high operating frequency 5GHz at lower supply voltage 1.5 V.

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