

AREA-ARRAY PACKAGE RELIABILITY MODELS FOR NO-CORE PCB
ASSEMBLIES IN EXTREME THERMO-MECHANICAL ENVIRONMENTS

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ASSEMBLIES IN EXTREME THERMO-MECHANICAL ENVIRONMENTS

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Timothy Dale Moore

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VITA

Timothy Dale Moore, son of Mr. Tim and Mrs. Carolyn Moore, was born on January 26, 1982 in Ashland, KY. He graduated in 2005 with a Bachelor of Science in Mechanical Engineering from the University of Louisville's Speed Scientific School in Louisville, KY. During his pursuit of his baccalaureate degree he was hired for three co-op internships at United Parcel Service headquarters beginning in 2002. He worked on various aircraft engine optimization, aircraft weight and balance, and aircraft performance projects in the department of Aircraft Performance Engineering. In the pursuit of enhancing his academic qualification he joined the M.S. program at Auburn University in the Department of Mechanical Engineering in Fall 2005. During the M.S. program at Auburn University, he has worked under the guidance of Professor Pradeep Lall, in the Department of Mechanical Engineering as a Graduate Research Assistant in the area of harsh environment electronic packaging reliability.

THESIS ABSTRACT

AREA-ARRAY PACKAGE RELIABILITY MODELS FOR NO-CORE PCB ASSEMBLIES IN EXTREME THERMO-MECHANICAL ENVIRONMENTS

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The trends in the electronic packaging industry are to design smaller packages that have higher complexity, and to improve package reliability while reducing costs. These needs in the packaging industry have lead to a newer generation of chip architectures, such as: Chip Scale Packages, Plastic Ball Grid Arrays, and Flip Chips. The ability of these package types to process faster information, and have high degrees of wiring complexity, while taking up minimal space, has made them very appealing to the automotive, space, and military industries. However, despite the increased performance capabilities of these leading-edge package types, their thermo-mechanical reliability is a concern for harsh environment applications.

In this work, risk-management models for reliability prediction of BGA packages on NO-CORE assemblies in harsh environments have been presented. The models presented in this paper provide decision guidance for selection of component packaging technologies. In addition, qualitative parameter interaction effects, which are often ignored in closed-form modeling, have been incorporated in this work. Previous studies have focused on deterministic prediction of reliability. There is need for a turnkey approach for making trade-offs between geometry and materials, and quantitatively evaluating the impact on reliability.

The presented statistics based approach targets a probabilistic life prediction for component wear-out under thermo-mechanical stresses. Models developed have been correlated with experimental data and non-linear finite element models. Factor effects for geometry, materials, and architectures based on statistical models, and FEA models have been developed. Convergence of statistical, failure mechanics, and FEA based model sensitivities with experimental data has been demonstrated. Validation of model predictions with accelerated test data has been presented.

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CHAPTER 1

INTRODUCTION

Electronic packaging is the process of interconnecting electronic and electromechanical components, devices, and modules between the various layers of the electronic system [Suhling, et.al. 2004]. The package provides protection from the environment, such as protection from moisture, and from external loads and stresses; removes heat from the silicon chip; provides wiring for a power supply to the chip; and provides the wiring for the I/O information to and from the chip. With the growth and advances in the electronic packaging industry, and the trends of packages to become smaller, faster, and have more circuit density, electronics reliability is a critical concern. Damage do to thermal cycling fatigue is a major concern for electronic devices that operate in harsh environments, with the solder joint interconnects being the primary failure component.

1.1 Test Parameters

An extensive amount of test packages were monitored in this research, with a multitude of test variables and conditions to consider. Among the package architectures were: Plastic BGAs, Ceramic BGAs, Flex Grid Arrays, CSPs, and Flip Chips, with I/O counts ranging from 49 to 900. Other test variables include: solder alloy (eutectic and

SAC305), PCB with and without a copper core, board surface finish, and four different temperature conditions. For this research, 45 No-Core PCB test boards were monitored (5 groups of 9 boards), with each test board being populated on both sides with packages. Figures 1.1 through 1.10 shows the front and back of a typical test board from each of the five test groups.



Figure 1.1. CCA's 091-099 (TC2: -55C to 125C). Side A of test board.

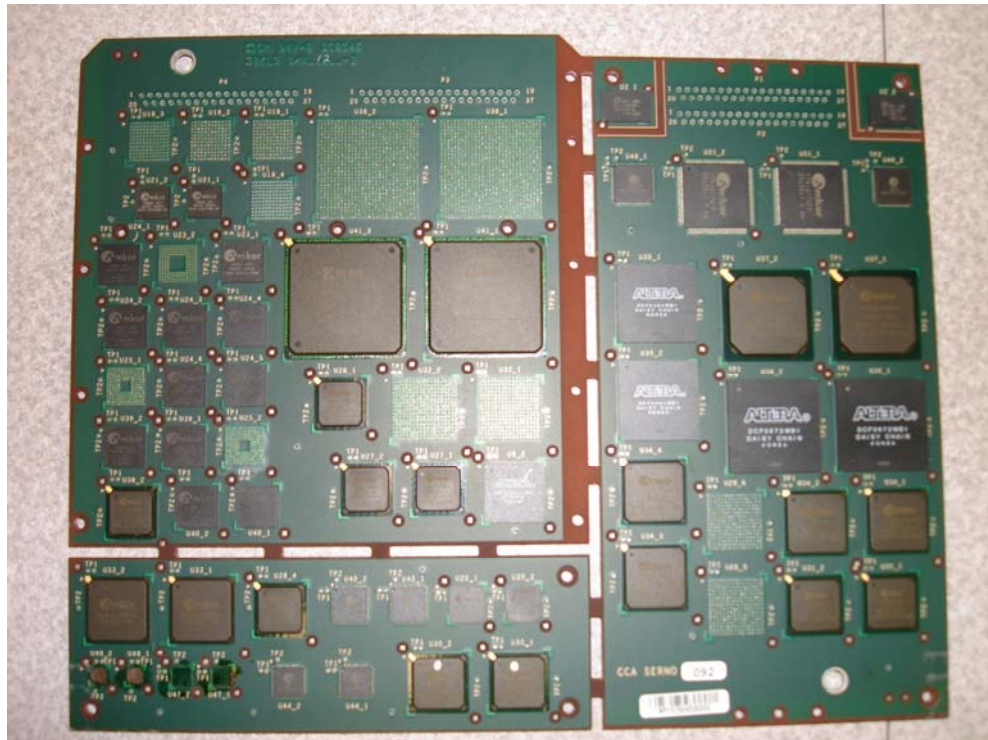


Figure 1.2. CCA's 091-099 (TC2: -55C to 125C). Side B of test board.

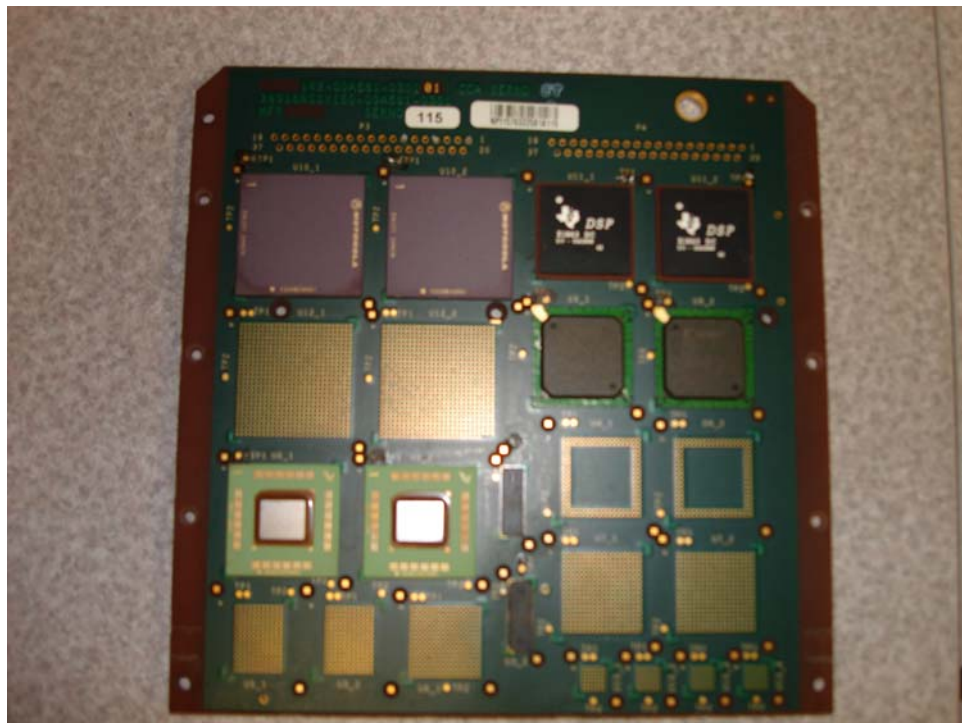


Figure 1.3. CCA's 109-117 (TC2: -55C to 125C). Side A of test board.

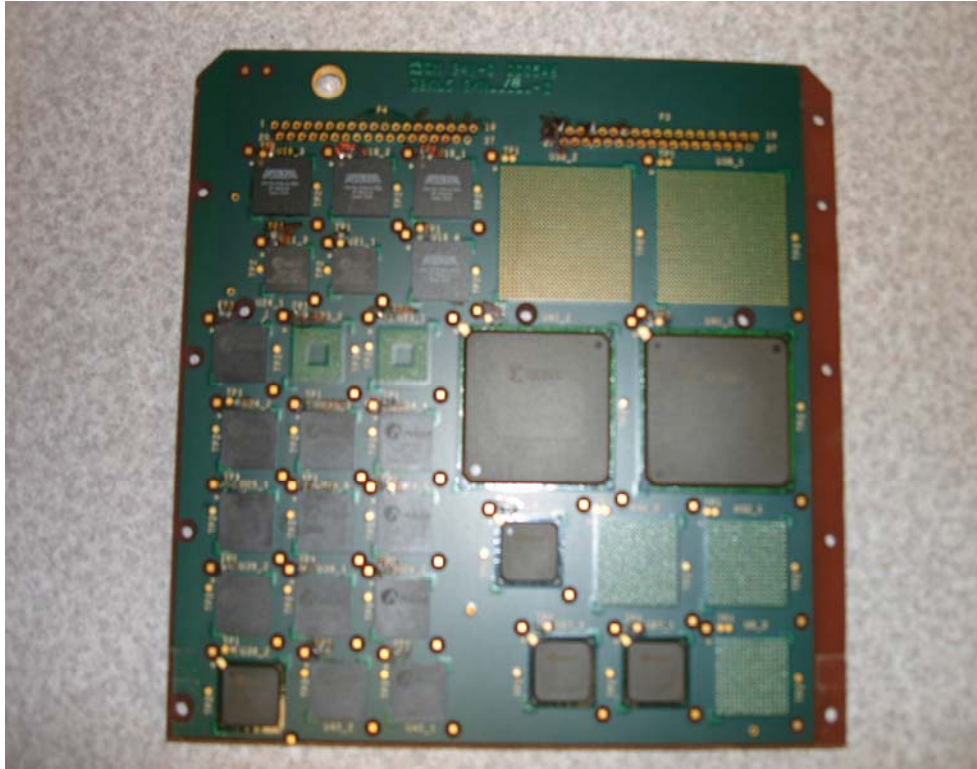


Figure 1.4. CCA's 109-117 (TC2: -55C to 125C). Side B of test board.

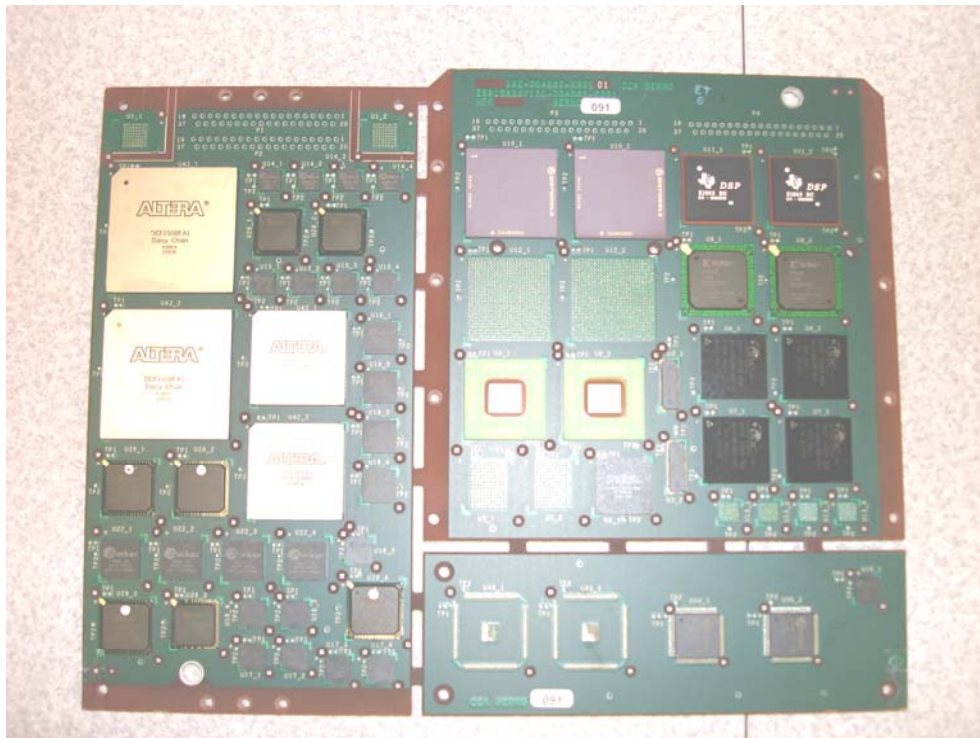


Figure 1.5. CCA's 127-135 (TC2: -55C to 125C). Side A of test board.



Figure 1.8. CCA's 136-144 (TC3: 3C to 100C). Side B of test board.

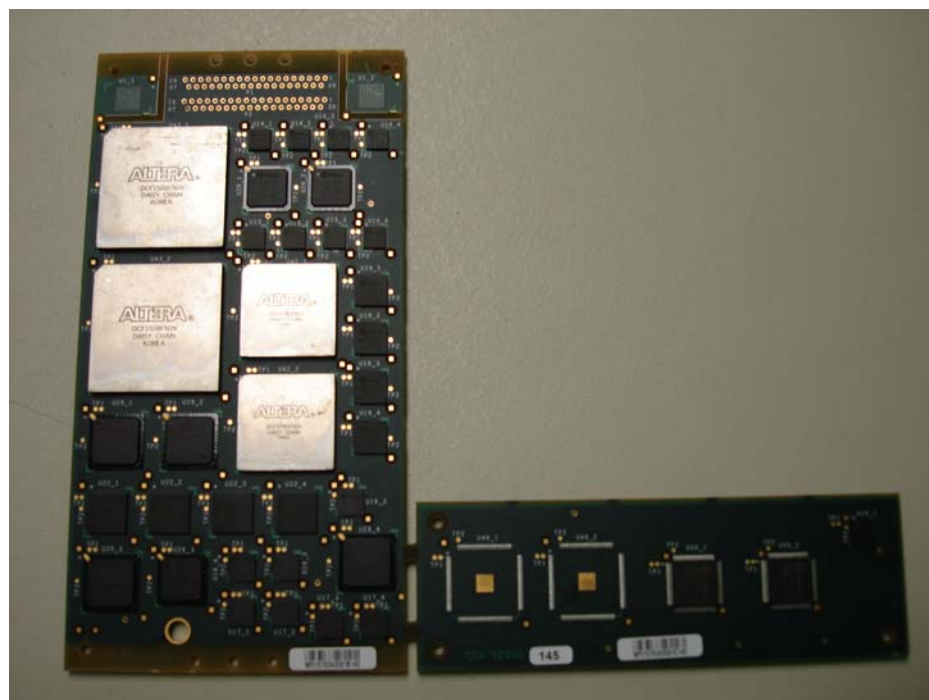


Figure 1.9. CCA's 145-154 (TC4: -20C to 60C). Side A of test board.

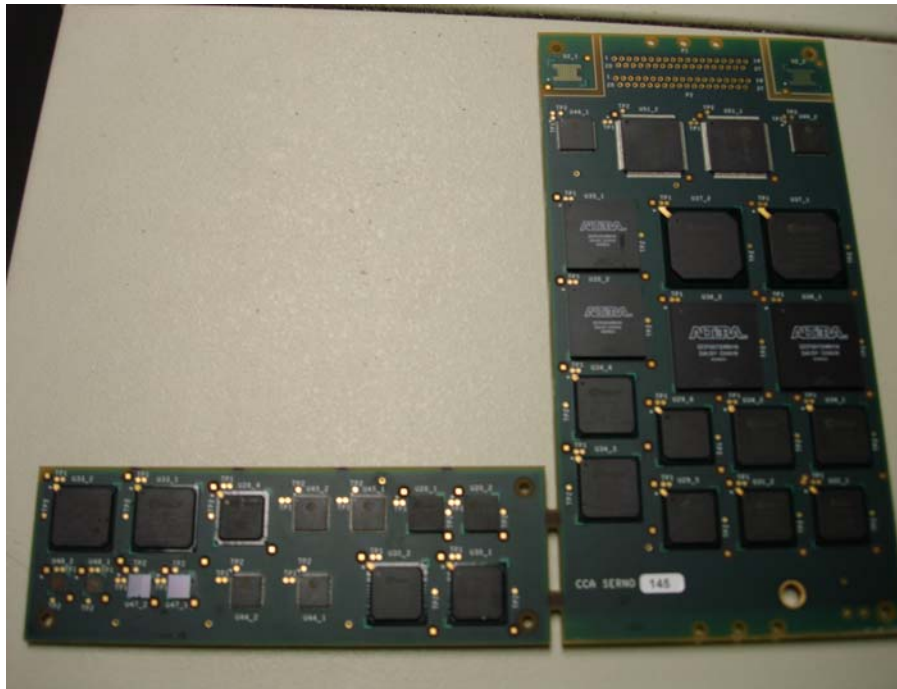


Figure 1.10. CCA's 145-154 (TC4: -20C to 60C). Side B of test board.

Each of the test boards contained between 61 and 120 packages. The total electronic package count for the scope of the research was approximately 4500 packages. The various types of packages included in this research are shown below in figures 1.11 through 1.13.

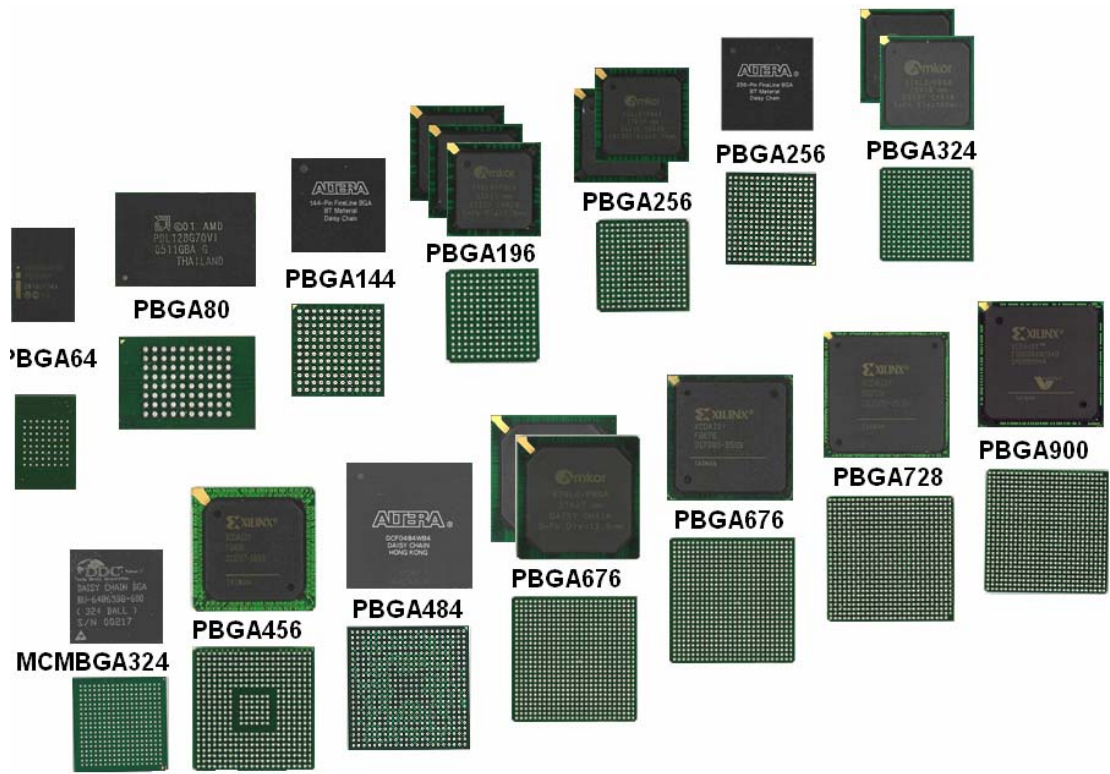


Figure 1.11. Various packages of accelerated test.

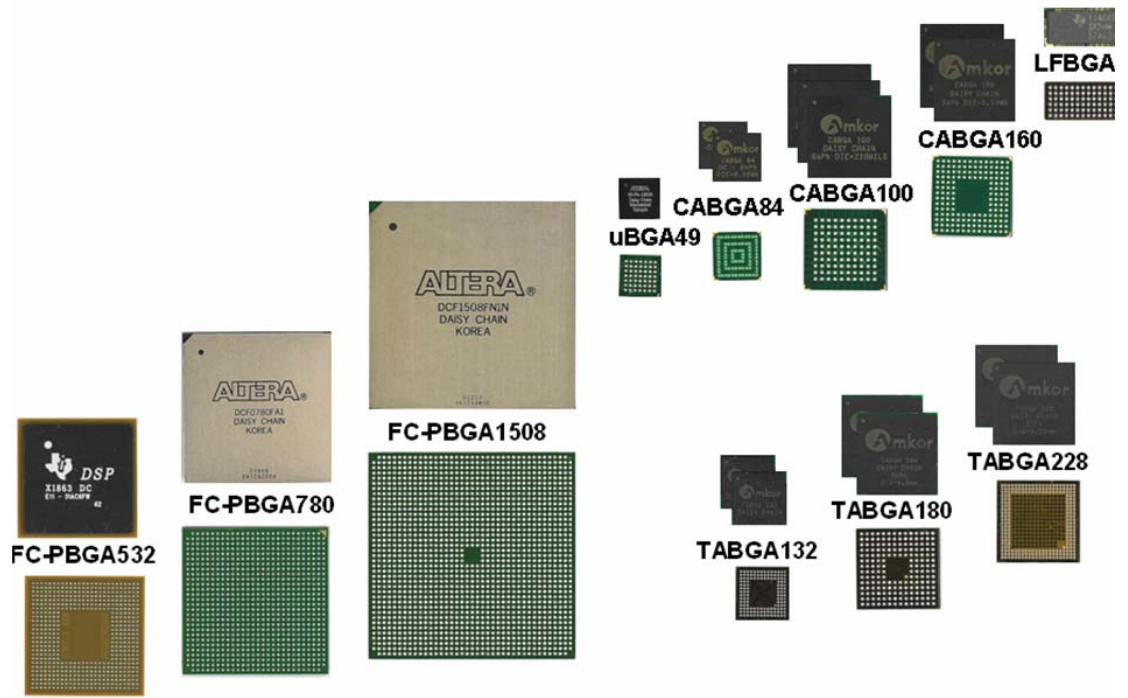


Figure 1.12. Various packages of accelerated test.

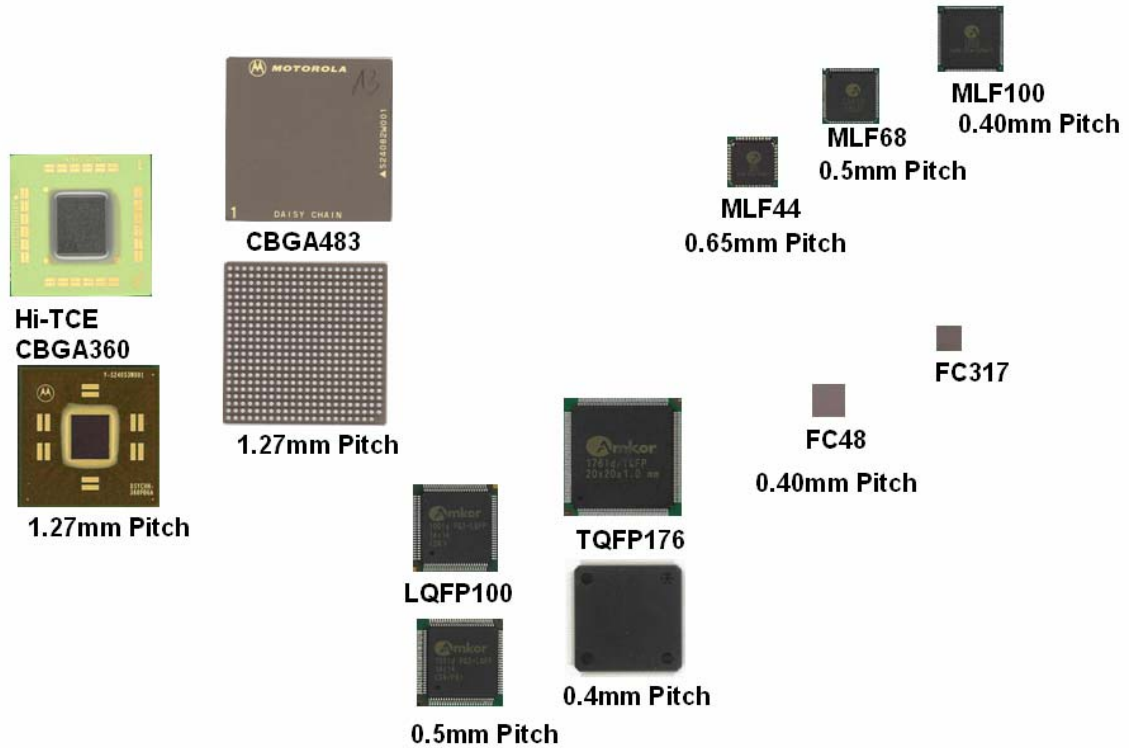


Figure 1.13. Various packages of accelerated test.

Four different temperature cycling conditions were also applied, three of which were monitored by this research, while the remaining temperature range was monitored by the sponsoring company. The four thermal cycling temperature conditions are shown in Table 1.1.

Table 1.1. Temperature conditions for accelerated test.

Profile	Low Temp (°C)	High Temp (°C)	Ramp Rate (°C/min)	Low Dwell (min)	High Dwell (min)
TC1	-40	95	3	30	30
TC2	-55	125	3	30	30
TC3	3	100	3	30	30
TC4	-20	60	3	30	30

The temperature profiles for TC2, TC3, and TC4 are shown in Figures 1.14, 1.15, and 1.16 respectively.

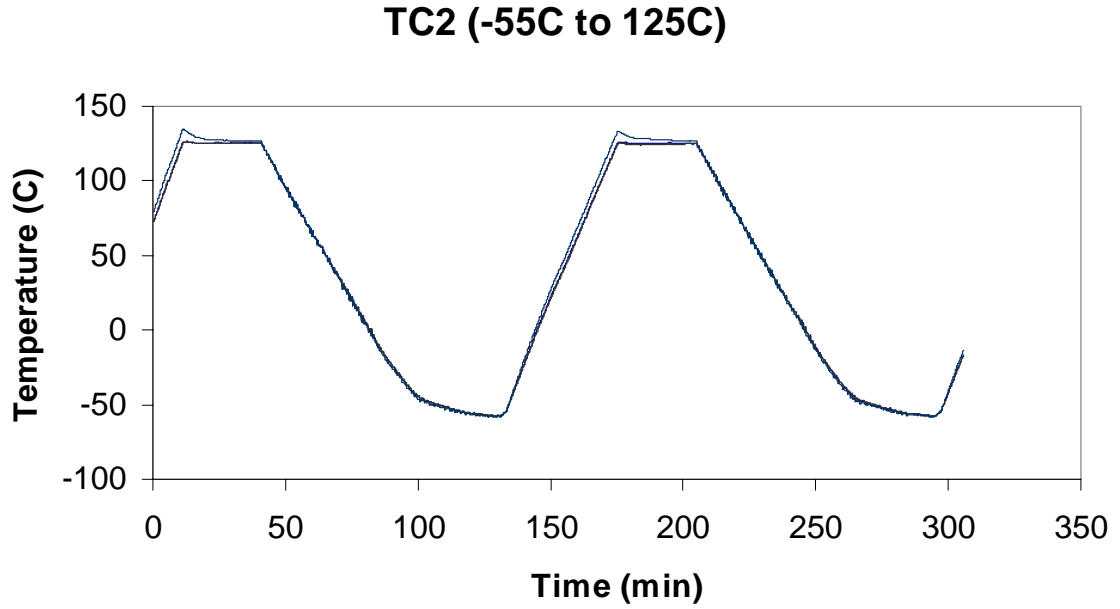


Figure 1.14. TC2 thermal cycling temperature profile.

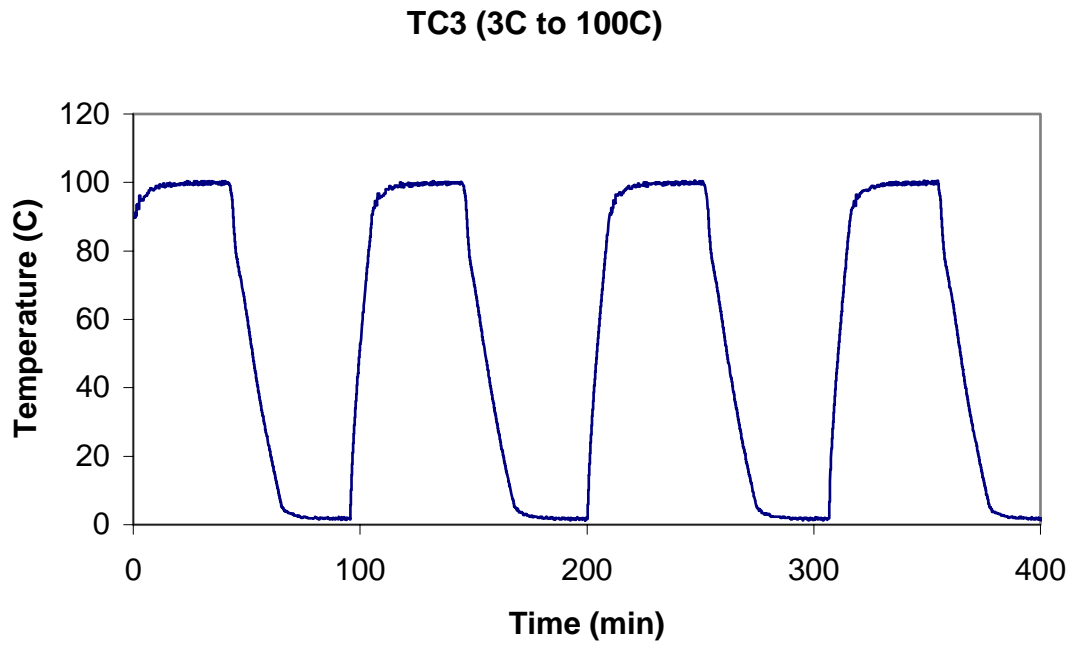


Figure 1.15. TC3 thermal cycling temperature profile.

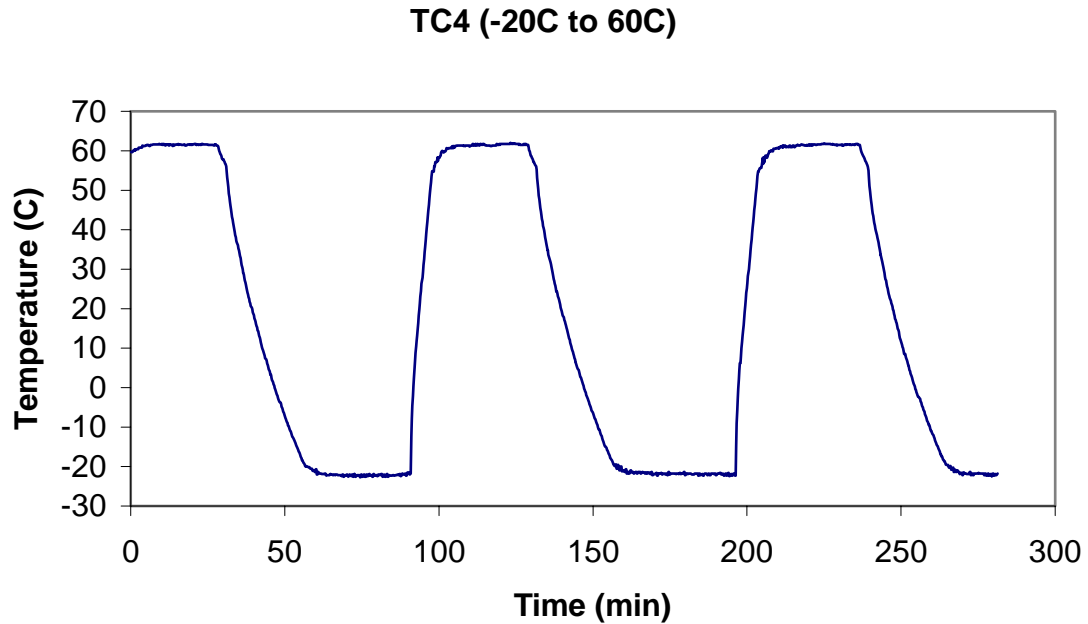


Figure 1.16. TC4 thermal cycling temperature profile.

1.2 Failure Monitoring

The reliability of the electronic test packages was monitored by periodically probing the resistivity of the packages, both manually and with data acquisition software, while subjected to thermal cycling temperature environments. The failure monitoring records of certain package types in specific environments allow for algorithms to be developed for use of package reliability and prognostics. By developing accurate life prediction models, significant cost reduction can be achieved by reducing downtime inspections and non-necessary component replacement, as well as reducing the risk of component failure during system operation.

1.3 Thermo-mechanical Reliability

Whenever an electronic device is operating, the device will generate heat. With Technology increases in electronic packaging making the IC chips of higher wiring density and increased complexity, the amount of heat generation and subsequent thermal damage is of high concern for the electronic packaging industry. When a device is powered on, which causes heat generation causing the components to heat up, and then powered off, allowing the components to cool back down to their environmental temperatures, a thermal cycle has occurred. Accelerated thermal cycling tests have been performed in this research to simulate the operational life of various components in harsh environments. The thermal cycling of devices leads to thermal fatigue damage, and eventually failure, due to mismatches in coefficients of thermal expansion (CTE) between the different materials in an electronic package. Table 1.2 shows typical values for CTE values among the different materials of an electronic package.

Table 1.2. Typical CTE values for package materials.

Material	CTE (1/K)
Copper Pad	16.3E-6
Solder Mask	30.0E-6
BT Substrate	12.42E-6 (XY) 57.0E-6 (Z)
Die Adhesive	52E-6
Silicon Die	2.50E-06
Ceramic	7.40E-06
Solder - 62Sn36Pb2Ag	24E-6
Solder - 96.5Sn3.0Ag0.5Cu	25E-6
Mold Compound	15E-6
PCB	14.5E-6 (XY) 67.2E-6 (Z)

This difference in CTE values causes stresses in the various components, with the most detrimental effects taking place at the interface of two components. The repetitive temperature cycling will accrue thermal plastic fatigue damage, and will lead to failure of the device.

1.4 Finite Element Modeling

The FEA (Finite Element Analysis) methodology is a very useful tool in simulating stresses on a device. For the purposes of electronic packaging reliability in this study, finite element analysis uses a physics of failure approach to analyze solder joint fatigue life under thermal cycle loading conditions. The measured amount of thermal fatigue damage that a solder joint accumulates is helpful in life prediction model validation, in which values can be compared to actual experimental values, as well as statistical models that have been developed. FEA analysis can be very useful; however, care must be taken by the user in modeling, meshing, boundary condition selection, and other assumptions in order to yield accurate results.

1.5 Statistical Modeling

Multivariate regression analysis has been used to assess the relative influence of parameters on the thermal reliability of electronic packages. Statistical models have been developed for Plastic BGA packages under various temperature environments, solder alloys, and various other package parameters. Parameters investigated for thermal reliability of the BGAs include: die size, die to package ratio, solder ball composition,

solder ball diameter, ball pitch, pad size, and temperature cycle conditions such as ΔT and the inverse of mean temperature.

CHAPTER 2

LITERATURE REVIEW

The thermo-mechanical fatigue that electronic packages are subjected to is considered to have the most critical effect on their life and reliability. The primary region of the thermal-induced failure occurs in the solder joint. Because of the high mismatch in CTE of the various materials that make up electronic packages, much of the accumulated stress is transferred to the solder joint causing de-lamination or fatigue crack initiation and growth. An abundance of published works exists on the effects of thermal loading and reliability. Numerous test methodologies have also been used to demonstrate results for thermal loading damage effects such as: accelerated thermal cycling tests, failure and damage relationship models, statistical based regression models, and finite element analysis (FEA) models.

2.1 Experimental Techniques

Researchers have conducted many types of experimental tests in the past to better understand and address solder joint fatigue life. Examples of such tests are accelerated thermal cycling, thermal shock loading, and vibration testing. These diverse testing procedures have been used by researchers to analyze solder joint fatigue life under different applications.

Syed [1996] conducted thermal fatigue reliability tests of plastic ball grid array packages for four design parameters: ball pitch, substrate thickness, array configuration, and pad size. It was found that thicker BT substrates (0.76 mm), using perimeter array configurations, 0.635 mm pads, and 1.27 mm ball pitch could improve solder joint fatigue life approximately 5X, allowing PBGAs to meet the harsh-environment reliability specifications of the automotive industry.

Suhling, et.al. [2004] presented research on the thermal cycling reliability of lead free solder joints for use in the automotive industry. Four solder compounds were tested: 95.5Sn3.8Ag0.7Cu and three variations of lead free SAC solder that incorporate small additions of bismuth and indium to enhance fatigue resistance. These solder joint compounds were thermally cycled under two test conditions: -40 C to 125 C, and -40 C to 150 C.

Results from this study showed that the eutectic SAC alloy 95.5Sn3.8Ag0.7Cu gave comparable reliability results to standard 63Sn37Pb solder alloy during the -40 C to 125 C temperature condition, but differed greatly, demonstrating much lower reliability relative to the 63Sn37Pb alloy, when subjected to the more harsh -40 C to 150 C temperature range. It was also shown that adding trace amounts of bismuth and indium can enhance the -40 to 150 C thermal cycling fatigue resistance relative to 95.5Sn3.8Ag0.7Cu.

A second set of thermally cycled test samples were cross-sectioned in order to examine crack growth, changes in microstructure, and intermetallic growth at the solder interfaces. It was observed that voiding and spheroidizing was present in all of the lead

free alloys, with spheroidizing clearly present after only 500 cycles. This was one proposed explanation for the variations and low beta values seen in the Weibull data.

Another observed difference came from the intermetallic layers. The layers in the two SnAgCuBi alloys and the 95.5Sn3.8Ag0.7Cu alloy were fine (typically around 1-3 mm thick) and continuous, while the SnAgCuIn alloy had rather large (10-20 mm thick) and uneven layers. It was proposed that these variations in the intermetallic layers could be responsible for the differences in harsh temperature reliability of the alloys.

2.2 Statistical Analysis

Statistical methods have often been used in research to analyze results of experimental test failure data. Most commonly, the choices of linear regression analysis and Weibull distributions are used. Liu, et al. [2005] conducted thermal reliability tests on anisotropic conductive adhesive (ACA) flip-chip joining technology for electronic packages. In this study, nine types of ACA and one nonconductive film (NCF) were used, totaling nearly 1000 single joints which were subjected to reliability tests of temperature cycling between 40 C and 125 C. A four-parameter Weibull parameter was developed and shown that in optimized conditions, high reliability flip-chip anisotropically conductive adhesive joints on low-cost substrate can be achieved.

Tee, et al. [2006] conducted solder joint reliability tests, comparing five different designs of thermally enhanced ball grid array packages: conduction cooled BGA (C²BGA), metal-core BGA, exposed-die land grid array (LGA), slug LGA, and spreader LGA. For this study, the solder joint reliability performances of the thermally enhanced BGAs were benchmarked with the conventional thin-profile fine-pitch ball grid array

(TFBGA). It was found that the C²BGA has better solder joint performance compared to conventional TFBGAs, and that solder joint reliability of C²BGAs can be enhanced by having smaller die, thinner mold compound and die, thicker substrate, smaller solder ball diameter, and a mold compound with higher CTE and a lower modulus. In his research, Tee also concluded that die-attach and slug-attach materials have little effect on fatigue life, and that thermal solder joints help to reduce the thermal resistance and enhance the solder joint reliability. A good correlation was also found between solder joint fatigue life and package warpage for both TFBGA and C²BGA: smaller package warpage leads to longer fatigue life.

Lall, et al. [2005] presented research on prognostics methods developed from statistical analysis from data on leading indicators of failure of electronic packages. Some leading indicators of failure are: micro structural evolution characterized by average phase size and correlated to time and equivalent creep strain rate, and stresses at interface of silicon structures. All predictive models to this point have only been able to predict the life of an electronic package from a known good state starting from a pristine, unused condition. The overall goal of this research was to develop a prognostics model that can predict the remaining useful life of a package based on examination of the current material state and prior stress histories.

The test components for this research include I/O counts in the range of 193 to 388, I/O pitch in the range of 0.8 to 1 mm, and package sizes in the range of 15 to 27 mm. The test board contained two 15 mm BGAs, one 27 mm BGA, and two 16 mm C²BGAs. All BGAs had Sn63/Pb37 solder balls, and the substrates used were standard HASL finished high temperature glass epoxy laminate (FR4-06) attached to 2.54-mm-

thick aluminum plate. The thermal cycling test was conducted at a profile from -40 C to 125 C.

It was concluded from experimental data that the rate of change of the phase growth parameter correlates well with several existing macro indicators of damage. A mathematical relationship was found between phase growth rate and time-to-1-percent failure. This allowed the computation of damage, and a forward estimate of residual life.

2.3 Finite Element Based Numerical Techniques

The FEA (Finite Element Analysis) methodology is a widely used and valuable instrument in the testing and understanding of solder joint fatigue life and reliability [Seyd 1996, Zahn 2002, Lall, et.al. 2004, Darveaux 2002]. Darveaux, et.al. [1992] conducted accelerated life tests on five types of alloy solder: 62Sn36Pb2Ag, 60Sn40Pb, 96.5Sn3.5Ag, 97.5Pb2.5Sn, and 95Pb5Sn. It was found that the 60Sn40Pb and the 62Sn36Pb2Ag solder alloys accumulate less strain before failure than the 97.5Pb2.5Sn and 96.5Sn3.5Ag alloys, and the 95Pb5Sn solder was the least yielding of all the alloys tested. It was also discovered that all of the test alloys reacted about the same amount under the accelerated thermal cycle conditions; however, under actual use conditions, the 96.5Sn3.5Ag and 97.5Pb2.5Sn solder alloys accumulated significantly less strain.

Zahn [2002] examined the solder joint reliability of same die, stacked, chip scale, ball grid array packages that were subjected to thermal cycling (-40C to 125C). ANSYS finite element analysis software (an industry standard) was used for the study, specifically Anand's Viscoplasticity model for solder plastic strain that combines plasticity and creep phenomenon. Of the two configurations of boards tested (one with

0.1143 mm spacer die with 0.7 mm mold cap and the other having a 0.1397 mm spacer die with a 0.8 mm mold cap), the thinner board configuration was found to have approximately 2X the characteristic life of the thicker board design. This was believed to be a result of the thinner board's greater flexibility, which would lessen the damage of plastic strain on the solder joint.

Novotny, et al. [2005] presented work on improving the reliability and durability of SMD components. Finite element analysis models were simulated to determine time-dependent solder joint fatigue under accelerated temperature cycling conditions (-40 C to 125 C), and to determine the maximum stress deformation in the solder joint during shear. Three types of SMDs were modeled using ANSYS finite element software: SMD 0805, 1206, and 1812. All model analyses were at constant temperature of 100°C.

It was shown that after the comparison of thermo-mechanical stress and shearing, the stress values for shearing were higher than that of thermo-mechanical stress. Of the three SMDs tested, 1812 reported the best reliability, having a predicted lifetime of 20% higher than the other two test configurations.

2.4 Constitutive Behavior of Solder Material

The material properties and behavior of materials is an important facet of modeling parameters, and ultimately, life prediction. Since finite element models require the input of material models and parameters that make up the components of the assembly, developing and classifying constitutive behavior accurately is vital to the modeling process.

A constitutive model is the mathematical representation of the material response to one or more variables [Vandevelde, et.al. 2002]. These constitutive models serve as input into larger computational models for stress analysis to approximate the thermal and mechanical loading a component will experience. Grossmann [1999] presented findings on the activation of deformation mechanisms in Sn62Pb36Ag2 solder alloy. Two deformation phenomena were observed (Grain Boundary Sliding and Dislocation Climb), each activated by a certain thermal test parameter, and associated to a particular stress-strain curve.

Darveaux, et al. [1992] conducted research on several solder alloys (62Sn36Pb2Ag, 60Sn40Pb, 96.5Sn3.5Ag, 97Pb3Sn and 95Pb5Sn) to collect and compare the stress-strain data. The testing parameters were for shear and tensile loading of the solder joint, over a wide range of strain and temperature rates. Darveaux found in his experiment that all of the data could be fit to the same constitutive model, where only the constant terms of the equation were dependent upon the solder alloy.

Pang, et al. [2004] compared his modified Ramberg-Osgood model to Anand's constitutive model for lead-free solder. His modified version of the Ramberg-Osgood model was derived from the fitted stress strain curves for lead-free (95.5Sn3.8Ag0.7Cu) solder alloy.

2.5 Objectives and Scope of the Thesis

The reliability of electronic packages can be analyzed by a physics of failure based and a statistical failure based approach. The research presented here has been done to further understand the reliability of various electronic packages subjected to harsh

environments, and to further understand the parameter effects that geometry and materials have on harsh environment package reliability. The field of electronic packages that were tested covered a multitude of variable parameters such as: solder joint diameter, solder joint pitch, package architecture, material properties, temperature conditions for accelerated thermal cycling, and board characteristics. The research presented here uses a physics-of-failure based finite element modeling approach to measure the accumulated strain energy density within components of a package. From these values of strain energy density, fatigue damage equations can be applied to predict the life for ball grid array packages. Also, statistical models were used to identify the critical factors in reliability performance of the tested electronic packages. These critical factors were found from the collection of experimental data, and then quantified through use of regression analysis.

CHAPTER 3

TEST EQUIPMENT

Given the large scope of the research presented in this work, a multitude of equipment was needed to perform, monitor, and collect useful information from the tests. It would be tedious and superfluous to list all tools, devices, hardware, and software that were needed to complete the research for this thesis; however, the author finds it appropriate to discuss essential equipment that was used to accomplish this research.

3.1 Experimental Test Equipment

Several fundamental equipment devices were needed to set up the experimental testing portion of the research. The major components of the data acquisition and testing used for this research were: thermal cycling environmental chambers, high density switching systems, and multiplexer cards, chamber profile calibrating equipment, digital multimeters, and Lab View software.

3.1.1 Keithley Model 7002 High Density Switch Systems

The switching systems used for this research were Keithley Model 7002 High Density Switch Systems. These switching systems allowed for programmable resistance monitoring of the test boards while cycling in the thermal chamber. The Model 7002

switching system is a ten card system, with 40 channels per card. A front panel and back panel view of this switching system is shown in Figures 3.1 and 3.2 respectively [Keithley 7002 Owner's Manual].

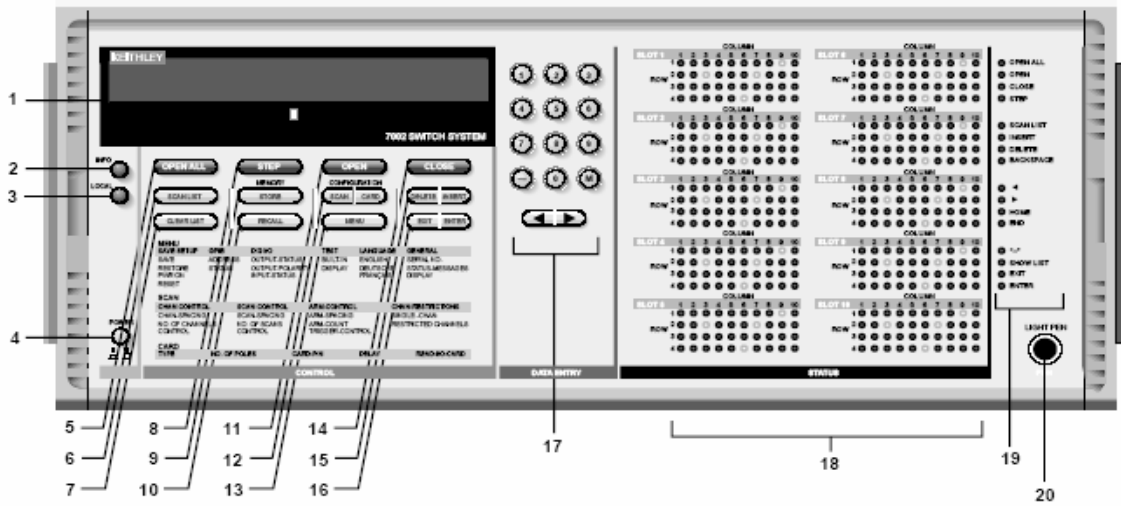


Figure 3.1. Front view of Keithley Model 7002 High Density Switch System.

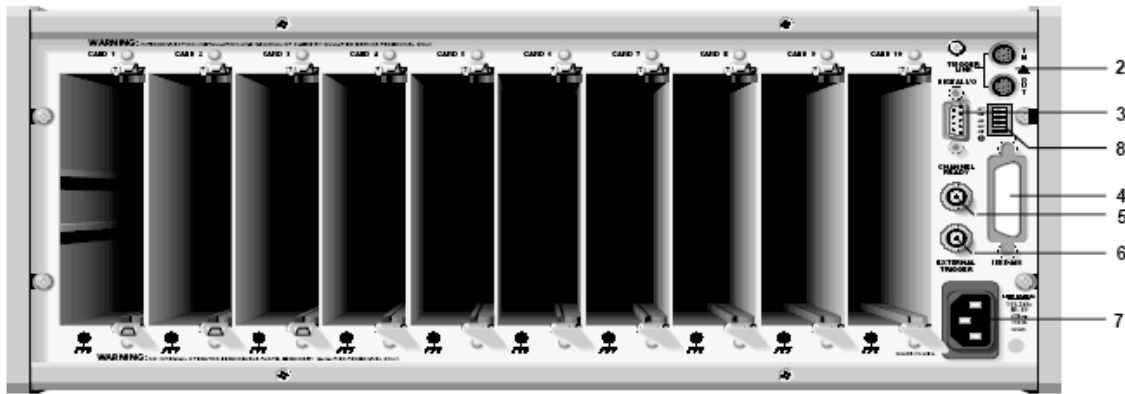


Figure 3.2. Back view of Keithley Model 7002 High Density Switch System.

3.1.2 Keithley 7011-C Quad 1 x 10 Multiplexers

The cards used within this model switching system were Keithley 7011-C Quad 1 x 10 Multiplexers. The 7011 is a low voltage, two-pole, quad, 1 x 10 multiplexer card [Keithley 7011 Owner's Manual]. These multiplexer cards consist of a multi-pin (mass termination) connector card and a relay card. External test circuit connections to the multiplexer are made through the 96-pin male DIN connector on the connector card. The Keithley 7011-C multiplexer card is shown in Figure 3.3. Figure 3.4 shows an actual test setup of 96-pin ribbon cables connected to the 7011-C multiplexer cards in the back of a Keithley 7002 switch system.

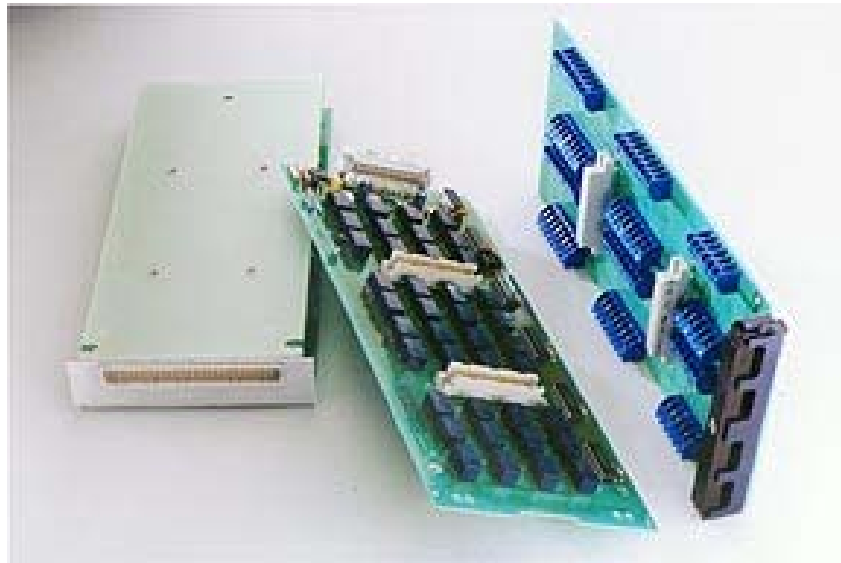


Figure 3.3. Keithley 7011-C multiplexer card.



Figure 3.4. Wiring setup of Keithley Model 7002 High Density Switch System.

3.1.3 Keithley Model 2000 Multimeter

The multimeters that were used to measure the test package resistance values were Keithley Model 2000 Multimeters. These 6.5 digit digital multimeters can take fifty triggered rdgs/s over the IEEE-488 bus, with a max speed of 2000 rdgs/s [Keithley 2000 Owner's Manual]. The model 2000 multimeter has a resistance sensitivity of $100 \mu\Omega$, and a maximum reading of 120 M Ω . The Keithley 2000 digital multimeter is shown in Figure 3.5.



Figure 3.5. Keithley Model 2000 Multimeter.

3.1.4 Fluke 73 Series III Multimeter

The portable digital multimeters that were used for this research were the Fluke 73 Series III Digital Multimeter. This model multimeter possesses 0.3% basic accuracy with 3200-count resolution. The full statistics are presented in Table 3.1, and a picture is displayed in Figure 3.6.

Table 3.1. Specifications of the Fluke 73 Series Multimeter.

Fluke Digital Multimeter Specifications		
DC Voltage	Maximum Voltage:	600 V
	Basic Accuracy:	0.30%
	Maximum Resolution:	0.1 mV
AC Voltage	Maximum Voltage:	600 V
	Basic Accuracy:	2%
	Maximum Resolution:	1 mV
DC Current	Maximum Current:	10 Amp
	Basic Accuracy:	1.50%
	Maximum Resolution:	0.01 mA
AC Current	Maximum Current:	10 Amp
	Basic Accuracy:	2.50%
	Maximum Resolution:	0.01 mA
Resistance	Maximum Resistance:	32 Ω
	Basic Accuracy:	0.50%
	Maximum Resolution:	0.1 Ω



Figure 3.6. Fluke 73 Series III Digital Multimeter.

3.1.5 SlimKIC 2000 Thermal Profiler

The thermal cycle temperature profile hardware and software used was the SlimKIC 2000. The basic components of the system are shown in Figure 3.7, consisting

of a receiver, data processor, and K type thermocouples. The specifications for the SlimKIC 2000 system are shown in Table 3.2 from the SlimKIC owner's manual.

Table 3.2. Specifications of the SlimKIC 2000 Thermal Profiler.

SlimKIC Specifications	
Accuracy	$\pm 1.2^{\circ}\text{C}$
Resolution	0.1°C to 0.3°C
Internal Operating Temp.	0°C to 105°C
Thermocouple Compatibility	Type K
Temperature Range	-150°C to 1050°C
Dimensions	10.5"L x 3.0"W x 0.75"H
Power Requirements	9V alkaline battery
Thermal Receiver	433.92 MHz



Figure 3.7. SlimKIC 2000 thermal profile system.

3.1.6 Environmental Chambers

Three temperature conditions were monitored by the author; those being TC2 (-55C to 125C), TC3 (3C to 100C), and TC4 (-20C to 60C). An environmental chamber

was needed for each different temperature condition. For the TC2 condition, the Blue M VRC was used. The Blue M, as shown in Figure 3.8.



Figure 3.8. Blue M VRC environmental chamber.

The second thermal cycling chamber employed was the Thermotron S-1.2 Mini-Max, shown in Figure 3.9. This chamber has a maximum temperature range of -73°C to $+180^{\circ}\text{C}$, with interior chamber dimensions of $40.6\text{cm} \times 27.9\text{cm} \times 30.5\text{cm}$.



Figure 3.9. Thermotron S-1.2 Mini-Max environmental chamber.

For the TC4 temperature condition, the chamber that was used was the Tenney Jr. bench top thermal chamber, shown in Figure 3.10. The Tenney Jr. chamber has both set point and actual temperature display with 0.1°C or 0.1°F resolution. The Tenney Jr. also features a control tolerance of $\pm 0.3^{\circ}\text{C}$ after stabilization.



Figure 3.10. Tenney Jr. environmental chamber.

3.2 Lab View Data Acquisition Program

The program used for data acquisition was a Lab View data acquisition program. This program was built to monitor test boards specifically for thermal cycling test environments by monitoring resistivity in packages as the thermal cycle test chamber is cycling. Information about the setup of this software was obtained from a procedural document written by former Auburn University engineering graduate Charles Mitchell. Figure 3.11 displays a screenshot of the Lab View graphical user interface (GUI).

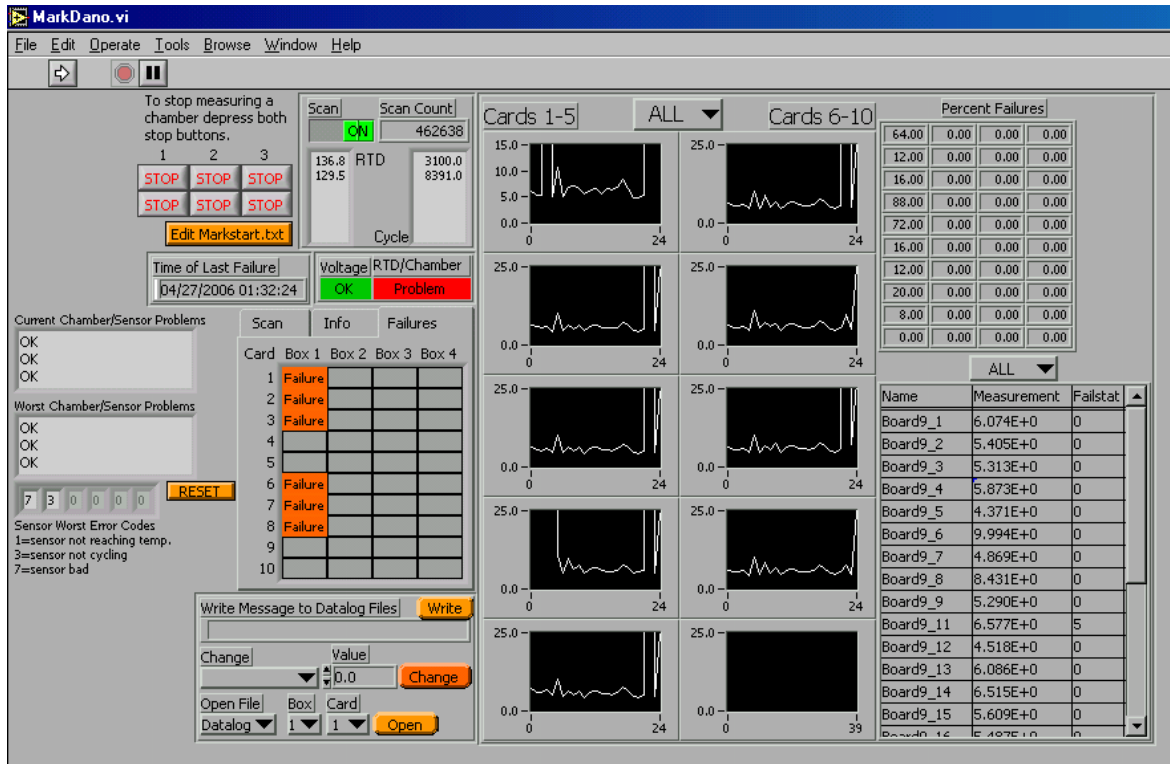


Figure 3.11. Screenshot of the Lab View data acquisition system software.

This program performs by utilizing two types of text files: configuration files and data files.

3.2.1 Configuration Files

The configuration text files are manually set up by the user, and are necessary for the program to function correctly. There are six different configuration files, but for the research conducted in this thesis, only five were necessary. The five file were: Markstart.txt, Rlogset.txt, Rtd.txt, bBfval.txt, and bBnameC.txt.

3.2.1.1 Markstart.txt

The first configuration file is titled: Markstart.txt. An example of this file is shown below. The numbers along the left column are not present in the actual file; however, numbered rows allow for easier explanation. It is important to note that on all of the configuration text files, no extra spaces or blank lines must be present after the entered text commands, or the system may not operate correctly.

Markstart.txt

Example file:

```
1.   Run
2.   c:\Connector_Test
3.   1
4.   1     0     0
5.   5400  0     0
6.   1
7.   0
8.   6.000 4.000
9.   1
10.  TCgrey/Connector   hsgale@eng.auburn.edu;menorris@ieee.org
11.  6341
```

The markstart.txt file is essential for the measurement program to initialize and run. This file is to be placed in the directory: c:\windows\desktop, with a shortcut of the measurement software placed in the Windows Startup folder so it will start when booted. The first line in the Martkstart.txt file is “Run” so the program will initialize and begin taking measurements when the computer is booted. The second line of text displays the directory in which all other configuration files, with the exception of Rlogset.txt, are located. This is also the directory where the data files will be created and store the

measured results. Line three of the text selects the scan speed or integration time in number of power line cycles per measurement (NPLC). This scanning speed is automatically reduced if filters are used, but one is the most adequate. Line four selects the temperature measurement option to be used for the test. Values of (0) through (3) can be entered and represent in order: no temperature sensors, 2-wire resistance of RTDs, 2-wire resistance of mechanical switches, and temperature in degrees C using 4-wire RTDs with the 2001 multimeter. Up to three values can be entered, and are tab delimited. The mechanical switch option can be used in place of the temperature sensors. If done, it looks for resistance values below 97 Ohms when the chamber is cold and resistance values above 125 Ohms when the chamber is hot. However, with this setting, the program will not report errors if the switch reaches zero or infinite resistance. Line five lists cycle times for up to three test chambers, and is also tab delimited. This setting is used to determine if the chamber is cycling within the appropriate amount of time. The sixth line lists the switching system number that the temperature sensors (RTDs) are connected to. A value of (0) indicates using the 2000-SCAN with the 2001 multimeter, and values (1) through (4) signify using the first through fourth Keithley 7002 switching system. *Note: the numbered order of the switching systems refers to the box address number. For checking or changing the box address numbers, refer to the Keithley 7002 operations manual. The seventh line can be either (0) or (1). Choose a value of (1) if one or more bias voltages are to be monitored, otherwise choose (0). Line eight signifies the range of bias voltages that are considered appropriate, with the upper limit first, and then the lower limit separated by a tab. The ninth line decides the type of measurement log setting to be used. A value of (0) results in every data measurement being recorded, (1)

results in data measurements being logged two times per cycle, and (2) will record data measurements every 30 minutes. Line ten gives a name to the test chamber, which is used in e-mail notices and web page status reports. After the chamber name, separated by a tab, e-mail addresses are listed to which error messages will be sent when they arise. Multiple e-mail addresses can be separated by a semicolon. The eleventh line lists the TCP port on the server to which the computer will send information.

3.2.1.2 Rlogset.txt

The next configuration file is Rlogset.txt. An example of this file is shown below.

Rlogset.txt

Example File:

1.	1	1	1	1
2.	1	1	1	1
3.	1	1	1	1
4.	1	1	1	1
5.	1	1	1	1
6.	1	1	1	1
7.	1	1	1	1
8.	1	1	1	1
9.	1	1	1	1
10.	1	1	1	1

This setup file designates which multiplexer cards in each of the switching systems will have measurement logs recorded for them. It should be noted that the Lab View software is programmed to monitor a maximum of four switching systems. Additional switching systems would require additional computers running the Markdano.dll software.

In this file four columns are present, each representing a Keithley 7002 switching system (in order by box address number from left to right). Also, ten rows are listed, each representing a multiplexer card with the designated switching systems. All columns are tab delimited, and rows are carriage return delimited. Each value within the matrix represents a multiplexer card which the switching system is capable of measuring. An example of how to read this matrix would be: the value in the fifth row and third column represents the fifth multiplexer card in the third switching system. Each value can either be a (1) or a (0), with a (1) designating a measurement log to be recorded for that multiplexer card, and a (0) designating that no measurement log will be recorded for that card. *Note: It is commonality not to change any of the values in this file, even if only one switching system is being used.

3.2.1.3 Rtd.txt

The next configuration file is the Rtd.txt file. An example of this file is shown below.

Rtd.txt

Example File:

1.	3	40
2.	4	40

The Rtd.txt file is responsible for the channel information of the temperature sensors. Each of the two rows assign the number of the multiplexer card that the

temperature sensor is connected to, then a tab, then the channel number that the temperature sensor is connected to for that card. One sensor is listed per line, with two sensors per chamber. Two additional values must be added after the channel number when using 4-wire RTDs, each tab delimited. These third and fourth values represent upper and lower temperature range values of the test respectively. These upper and lower limit values are used to determine if the chamber is cycling properly. The chamber temperature must reach at least 0.4 multiplied by these upper and lower limit values or an error will occur. *Note: All temperature sensors must be on the same Keithley 7002 switching system or 2000-SCAN system for the software to run properly. *Note: If the 2000-SCAN system with the 2001-multimeter is used for data measurement, the card number spot in the text file can be disregarded, and only the channel number is used.

3.2.1.4 bBfval.txt

The fourth type of configuration file is the bBfval.txt file, which is the failure value file. An example of this file is shown below.

bBfval.txt (Failure Value File)

Example File:

1.	150	2000	80	1
2.	150	2000	80	1
3.	150	2000	80	1
4.	150	2000	80	1
5.	150	2000	80	1
6.	150	2000	80	1
7.	150	2000	80	1
8.	150	2000	80	1
9.	150	2000	80	1

10. 150 2000 80 1

This file designates the settings to be used during the measurement scans. The name of the file follows this format: `bBfval.txt`, where B represents the switching system number (one through four). Each row represents a multiplexer card for that switching system, and can contain up to nine values, which are tab delimited. The first value stands for the upper resistance limit. The other eight values are optional, and are in order as follows: meter range, channels per scan, digital filter, lower limit, meter function, integration time divisor, temperature sensor pair, and close first list. The meter range is typically 1000 to 2000 ohm, depending on the meter used. The channels per scan option defaults to 40, but can be set to 80 allowing a consecutive odd and even numbered multiplexer card with the same scan settings to be scanned together, reducing overall measurement time. The integration time divisor is a division factor number by which the integration time is divided for a scan, reducing the scan time for a test with a large number of channels. The defaults for all of these options are: 100 ohm upper failure limit, 1000 or 2000 ohm meter range (depending on meter used), 40 channels per scan, digital filter off, negative infinity ($-\infty$) for lower failure value, 2-wire ohm meter function, integration time divider of 1, first temperature sensor pair (0 indexed), and no close first list.

3.2.1.5 bBnameC.txt

The fifth configuration file is `bBnameC.txt`. An example of this file is shown below.

bBnameC.txt (Naming File)

Example File:

```
1.   Board1_1   1
2.   Board1_2   2
3.   Board1_3   3
.
.
.
40.  Board1_40  40
```

This file contains channel and test component information of components that are being monitored during thermal testing. The name of the file follows this format: bBnameC.txt, where B is the switching system number (one through four), and C represents the multiplexer card number (one through ten). There needs to be one name file for each multiplexer card that is being scanned. Each row of the file designates a test device or component to be monitored, and is tab delimited. The first value is the name of the component being tested, and can be any name the user desires to identify the component. These component names will be used in the data files to record failures, which will be discussed later. The second value in the row represents the channel number that the device is connected to, on that particular card (C) and switchbox (B). The other two values are optional, and are: upper limit and lower limit. The upper and lower limits are the resistance range values that can be used to determine if the component has failed. When the upper and lower limits are present in this file, they will be used as failure criteria instead of the values in the failure value file. This option is useful when each device has its own separate resistance failure limit requirements.

3.2.2 Data Files

The data files are files that the Lab View program creates automatically when it begins the monitoring process of the experimental test. These files are used to record the various test information. There are four types of data files that the LabView program creates: Count files, Failure Status files, Data files, and Log files.

3.2.2.1 Counta.txt

The first group of data files is the Count files (counta.txt, countb.txt, and scount.txt). Examples of two of these files are shown below. The numbers along the left column are not present in the actual file; however, numbered rows allow for easier explanation.

Counta.txt

Example file:

1. 388.0

This file, along with the countb.txt file, records the measurement cycle count number of the thermal chamber when the program is monitoring an experiment. These two files are created in the /count subdirectory folder, which the LabView program creates as well. There exists one count file for each temperature sensor in the thermal chamber, and both the counta and countb text files contain only one number, the cycle count number, which automatically starts at zero when the program initiates.

Scount.txt

Example file:

1. 1128285

The Scount.txt file is similar to the other two count files, except instead of recording the number of thermal cycles that the test has experienced, this file records the total number of scans executed by the measurement software. This file is created in the same directory as the other two count files.

3.2.2.2 bBfailC.txt

The second type of data file is the failure status file. An example of this file is shown below.

bBfailC.txt (Failure Status File)

Example file:

1. 0
2. 0
3. 0
4. 0
5. 0
6. 0
7. 0
8. 0
9. 0
10. 5
11. 1
12. 1
13. 0
14. 0
15. 0

16. 0
17. 5
18. 0
19. 0
20. 5
.
.
.
400. 0

This file monitors how many times each test device has been reported as a failure (the number of times each device has been measured to be beyond the allowable range set in either the bBfval.txt file or the bBnameC.txt file). This file is in the format bBfailC.txt, where B is the switching system number, and C designates the multiplexer card number. There is one file created for each multiplexer card being used in the test, and they are found in the /failstat subdirectory. These files contain many rows of numbers, where each row designates a channel number. Every time a device “fails,” the value of that channel number increases by one. Once the device is measured to be outside of the set allowable range five times, the test device is considered to have failed, and a record of this is logged in the data file. *Note: once a channel value has reached five, the value will not increase since the test device is considered to have already failed. The user can manually reset this number.

3.2.2.3 bBdataC.txt

Next is the data file. An example of this text file is shown below.

bBdataC.txt (Data File)

Example File:

Name	Date	Time	Value	Cycle A	Cycle B	RTD A	RTD B	Scan #	% Failure
G19	06/06/2006	15:39:45	99.000000E+36	139.5	139.5	114.55	118.09	1124125	4.76
G5	07/05/2006	21:46:32	2.130781E+3	383.0	383.0	121.10	121.06	1128163	14.29

The rows were not numbered in this example file since the rows would have been too wide to properly display. This file records the failure information for each test device. The file has the format bBdataC.txt, where B represents the switching system number, and C stands for the multiplexer card number. These files are saved in the \datalog subdirectory. Each row contains ten values which are all tab delimited. The first four values represent the name, date, time, and measured resistance value at which the test device failed. The fifth and sixth values represent the values of the counta.txt and countb.txt text files respectively at the time of failure. The seventh and eighth values in the row correspond to the temperatures of the tow temperature sensors at the time of failure. The ninth value displays the scout.txt value at the time of failure, and the last column lists the percent failure.

3.2.2.4 bBlogC.txt

The last data file is the log file. No example file is shown for this file since it can grow very large depending on the type of log file recording preference that was selected

in the markstart.txt configuration file. This file has the format bBlogC.txt, where B represents the switching system number, and C designates the multiplexer card number. This file records the resistance values for every channel on the multiplexer card that is being monitored, as well as information such as: the time, date, temperature sensor values, and cycle count number when the resistance values were logged.

3.2.3 Executing Lab View Software

Once all configuration files have been set up to the desired test specifications, the program is now ready to begin monitoring and recording the test data. To begin the program, restart the computer, then immediately power off all switching systems and multimeters. The program is set to automatically begin upon reboot. Now wait until the windows screen appears during the computer reboot process. When the windows screen appears, begin powering on the switching systems in order of their box address number, lowest to highest. For checking or changing the box address numbers, refer to the Keithley 7002 operations manual. Once all switching systems have been powered on, power on the multimeter. All of these devices must be on before the computer is fully rebooted and tries to start the program; else the user must stop the program, and repeat this process. Figure 3.12 shows an excerpt of the experimental data failure record catalog system.

	A	B	C	AC	AD	AE	AF	AG	AH	AI	AJ	AK
1												
2	Date			7/28/06	8/21/06	9/6/06	9/13/06	9/21/06	9/28/06	10/13/06	10/19/06	10/24/06
3	Cycle		151	508	691	822	866	940	1001	1123	1175	1219
76	U26_3			fail	fail	fail	fail	fail	fail	fail	fail	fail
77	U26_4			1.8	1.1	1.1	1.1	1.1	1.2	1.2	1.2	10.4
78	U27_1			1.2	1.0	1.0	1.0	1.1	1.2	1.2	1.2	1.2
79	U27_2			1.1	1.0	1.0	1.0	1.0	1.2	1.2	1.2	1.2
80	U28_1			1.1	3.9	fail	fail	fail	fail	fail	fail	fail
81	U28_2			1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2
82	U29_1			fail	fail	fail	fail	fail	fail	fail	fail	fail
83	U29_2			1.5	fail	fail	fail	fail	fail	fail	fail	fail
84	U29_3			fail	fail	fail	fail	fail	fail	fail	fail	fail
85	U29_4			1.5	1.7	4.6	fail	fail	fail	fail	fail	fail
86	U29_5			1.2	1.2	1.2	1.2	1.2	1.4	1.4	1.4	1.4
87	U29_6			1.2	1.5	1.5	1.5	11.7	11.7	11.7	15.5	20.0
88	U30_1			1.3	1.3	1.3	1.3	8.0	8.1	8.1	8.1	8.1
89	U30_2			1.2	1.2	1.2	1.2	1.3	1.3	1.3	1.3	6.5
90	U31_1			fail	fail	fail	fail	fail	fail	fail	fail	fail
91	U31_2			fail	fail	fail	fail	fail	fail	fail	fail	fail

Figure 3.12. Experimental data failure record catalog system.

3.3 Package Cross-Sectioning Technique

For the finite element based modeling approach previously discussed, proper dimensioning for each of the packages modeled had to be obtained. For some of the electronic packages that were modeled, package cross sectioning had to be done to obtain these component dimensions. Information about the process of cross-sectioning electronic packages was obtained from a procedural document written by former Auburn University engineering graduate Charles Mitchell [2006]. The procedure used for cross sectioning and preparing the package will be discussed in this section.

The first step of the cross-sectioning procedure should be to develop a cutting scheme that will give the desired cross section. An example of a cutting scheme is shown

in Figure 3.13; however, each cutting scheme is application specific and should be determined on a case-by-case basis.

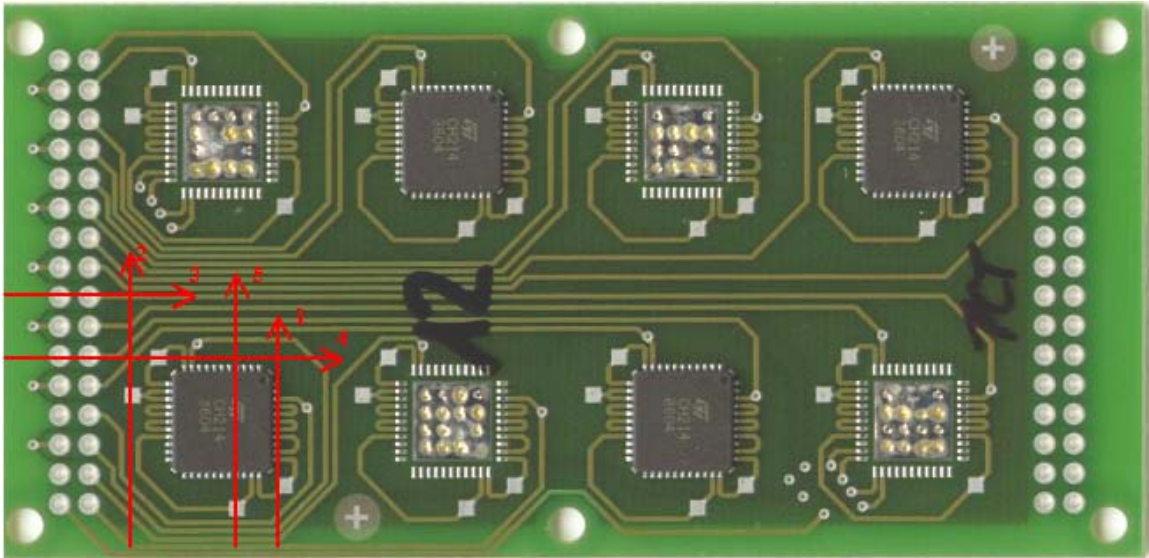


Figure 3.13. Example of cross-sectioning cutting scheme.

The cutting procedure is delicate, so care must be taken to make a straight, precise cut. A fine-tipped permanent marker is used to mark the area of interest of the electronic package. Once the mark identifying the location of the cut is made, preparation of the cutting saw must be done to ensure a clean, accurate cut to the package, and to ensure proper care of saw. For cross-section cutting, the Isomet 1000 (Figure 3.14) wet saw was used to make the cuts.



Figure 3.14. The Isomet 1000 wet saw.

In preparing the wet saw for use, the coolant must be checked. If the coolant appears to be clean and at the proper level, then the saw is ready for cross sectioning; however, if the coolant appears dirty or below the proper level, it must be replaced before use. The manufactures' specified coolant ratio is 1 part coolant to 9 parts water (ratio 1:9). Also, the appropriate coolant level is measured to cover the bottom of the saw with 3/8 inch of coolant solution. This ensures heat dissipation of the saw blade generated by cutting the electronic packages, and wets the blade to prevent sawdust or chipping of the package. After the coolant is at the specified level, the saw can be turned on. Dress the saw blade with coolant before starting any package cross sectioning. This is done by setting the saw at 250 rpm and allowing the blade to make two complete revolutions through the coolant. For the cross sections cut in this research, the blade speed was typically set at 200 rpm, but this can be varied to meet the application. After each section cut, label and clean the components. After all cuts have been made, empty and replace the coolant.

Once all cuts have been made, they each must be sealed in epoxy resin so they can be handled and polished. Supplies used for encasing the cross sections are displayed

in Figure 3.15. These supplies consist of epoxy resin, hardener, molds, stabilizing clips, stirs, and a mixing cup. An accurate scale will also be needed to measure the appropriate ratio of epoxy.



Figure 3.15. Materials used for epoxy coating cross-sectioned samples.

For all samples of interest, place stabilizing clips on them with the cross-sectioned area facing down and flush in the holder. Once all samples have been placed in holders, the epoxy resin can be prepared. Place a clean mixing cup on the scale and record the dry tare weight. Now the resin can be very slowly and delicately poured into the mixing cup, making as few air bubbles as possible. This is made easier if the resin is poured smoothly onto an angled stir that is sitting in mixing cup. After the resin has been poured in, calculate how much hardener must be added based on how much resin was used. The proper ratio of resin to hardener is 2:1, and must be exact. Now the hardener can be added to the resin in the same manner that the resin was added. Once the appropriate amount of hardener has been added, use a gentle “scooping” motion with the stir while leaning the mixing cup at an angle to ensure proper mixing of the resin and hardener, and

to eliminate any remaining air bubbles. It is important to remove as many air bubbles as possible so they do not disrupt the view of surface of interest. The mixture should appear clear when fully mixed.

Once the epoxy has hardened, each sample can be pushed out of the mold. Make sure that each sample is labeled on top of its epoxy for proper identification later. For the research done in this research, the Ecomet 6 polisher (Figure 3.16) was used.



Figure 3.16. The Ecomet 6 polisher.

The polishing can be done on either wheel. Take the metal clamp off of the wheel to be used and put on the appropriate grit sandpaper. The process of polishing is to incrementally adjust sandpaper sheets, using progressively finer grit sheets the more you polish. The grit types used in sequential order are as follows: 120, 240, 320, 400, 600, 800, and 1200. The grit size from 120 to 40 is used to remove the excess bulk material until the solder joints can just be seen. The more fine sheets – 600 through 1200 – are used to gently grind to the solder joints and to reduce surface scratches.

Once the paper is clamped on the wheel, turn on the water and direct the stream to the center of the wheel. The wheel can be turned on now at approximately 200 rpm. With the wheel turning and wet, the sample can be held against the wheel with reasonable pressure for intervals of 3 to 5 seconds. After each interval, lift the sample, rotate it 90°, and repeat. The sample can be checked every complete revolution to see the progress. To check the progress, clean the sample under the water valve, and look under a microscope. When finished, turn off the water valve, and dry the sample with compressed air – never wipe the sample with anything, as scratches will result.

By this point the sample should have a reasonably polished surface; however, to obtain an ultra clear surface for detailed view under a microscope, the samples need to be polished with diamond paste. Remove the grinding wheel from the machine, and exchange it with the polishing wheel with the white cover. Put the covered wheel on the machine, and do not use water. Now retrieve the 3-micron alumina diamond paste (green colored) and the Extender spray bottle. Apply dots of diamond paste around the white wheel, and spray the Extender spray on it as well. The machine can now be turned on to 150 rpm, and with modest pressure, polish the sample in the same manner as previously explained. To check the sample, wash and air dry them, and look under a microscope. When finished, wipe the white cover with a clean wipe, spraying additional Extender spray if needed.

Finally, for master prep of the samples, remove the white covered wheel and replace it with the black covered polishing wheel. Turn on the water and wet the wheel, and then turn the water flow off. Now the polisher can be turned on to 100 rpm. While the wheel is turning, take the 0.05-micron master prep solution (white colored), shake it

well, and apply it to the wetted wheel by a few drops every few seconds. Now put the sample on the polishing wheel the same way as before. To check the sample, clean the surface with water only, and check under a microscope. Everything should now appear clear and scratch free. When finished, turn the water on to rinse off the black cover and allow to air dry by setting the polisher to 300 rpm, and let run for 5 minutes. Wash of the samples with water and used only compressed air to dry; never use a cloth or towel to wipe.

CHAPTER 4

FINITE ELEMENT ANALYSIS

The use of finite element analysis (FEA) to model deformation and failure caused by thermal cycle testing is common in the industry of electronic packaging [Pang, et.al. 2001]. These analytical models have several practical uses in the field of engineering, examples of which are: rapid design optimization during the development of a product, predicting application use limits of the product, and failure analysis of the product returned from field use or a failed quality control test [Darveaux 2002]. For the use of accelerated thermal cycle testing, the FEA analysis presented in this research has been used to evaluate the stress and strain distributions within the modeled electronic package by calculating the accumulated plastic work within the solder joints. This volume averaging of the plastic work accumulation is useful in applying damage relationships to predict the N1% life for a package.

For the process of analyzing thermal cycling conditions in FEA, the initial temperature, or stress free state temperature, can be modeled at different temperature values; for instance: room temperature (25 °C), the underfill epoxy cure temperature (140 °C), or at the eutectic solder joint melting temperature (183 °C) [Pang, et.al. 2001, Rahim, et.al. 2006]. It is known that electronic packages have less initial stress at the assembly temperature – typically above 150 C – than at cooler temperatures. This is due

to the fact that as the assembly cools with all of the materials bonded together, the CTE mismatch of the different materials cause stresses at the mating surfaces of the bonded materials within the package. As the assembled components of the package cool below room temperature, the temperature difference between the applied temperature and the package stress-free temperature becomes larger. This large ΔT value causes large stresses and deformations in the package layers due to component CTE mismatches. In this research a room temperature reference temperature was chosen to more accurately match the experimental package conditions that were being modeled.

ANSYS V 9.0 finite element simulation software was used as the comparative theoretical test method for predicting solder joint fatigue failure. The models were built from empirical data gained from each individual package that was modeled. This method makes the FEA modeling process very specific to the conditions of each application.

4.1 Geometry

The geometry used for ANSYS modeling was a half-symmetry diagonal slice of the total package, which is shown in Figures 4.1 and 4.2. The stress and strain calculated was derived from the amount of plastic work that accumulated over the thermal cycling test conditions. A vast number of packages types were tested in the experimental portion of this research; however, only a certain number of package types were selected for modeling in ANSYS.

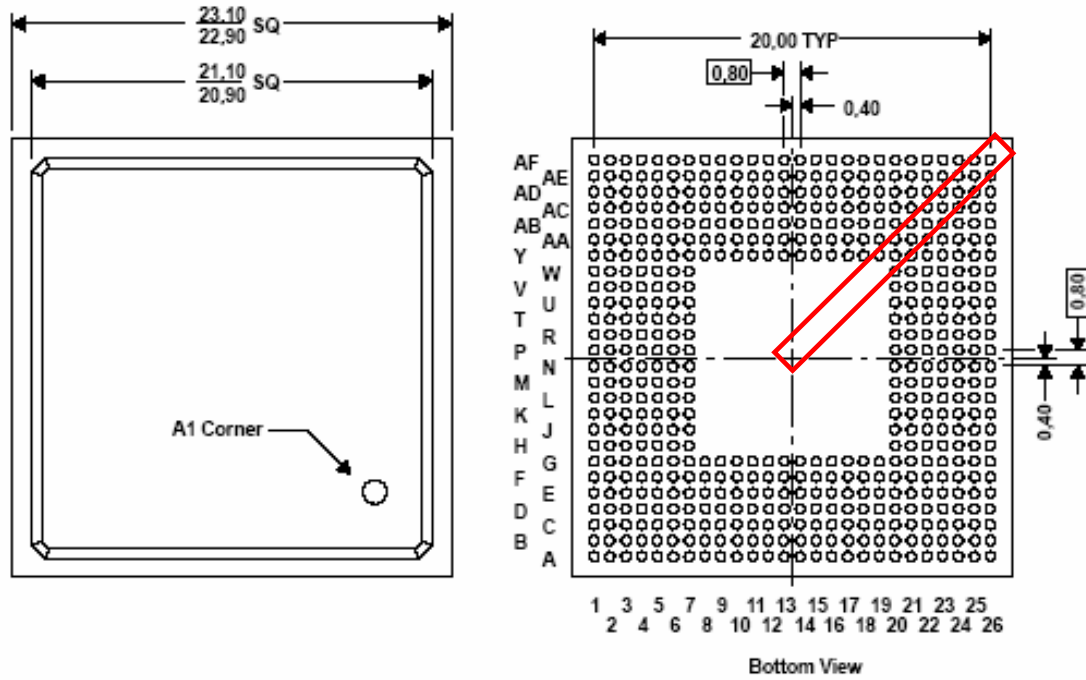


Figure 4.1. Diagram of slice model geometry.

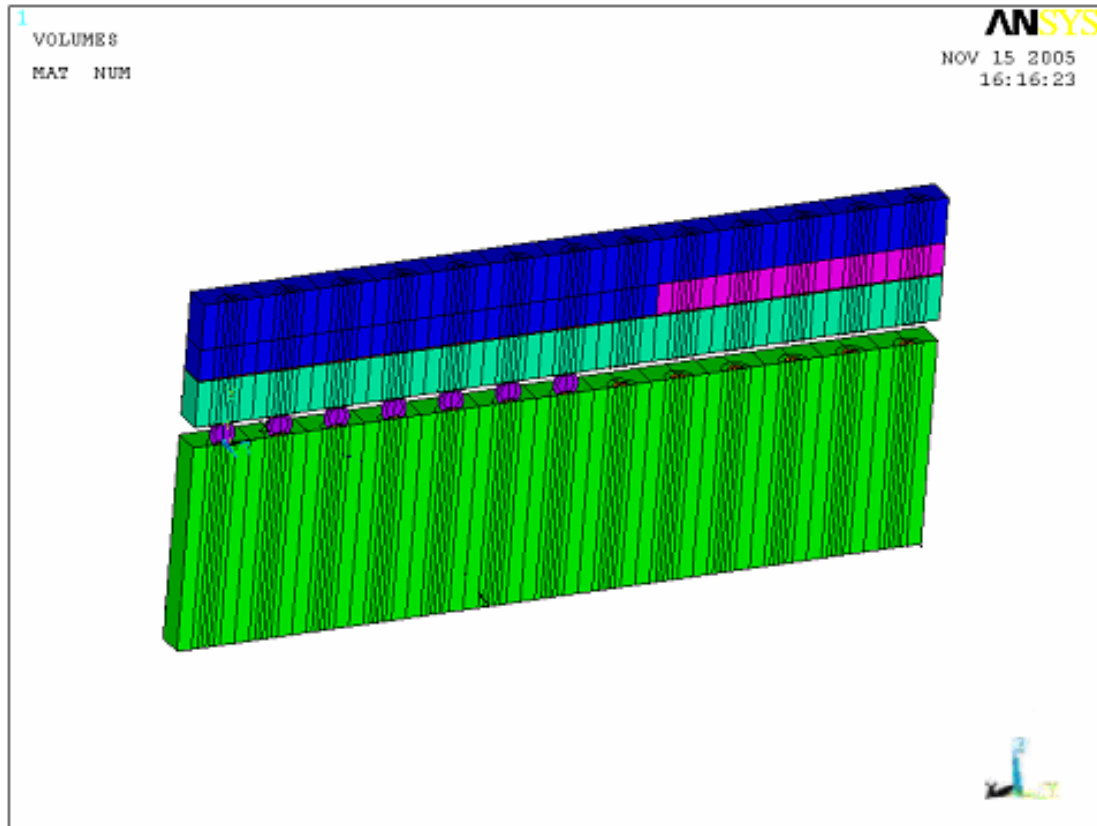


Figure 4.2. Isometric view of a slice model.

The geometries were programmed into ANSYS by using ANSYS Parametric Design Language (APDL). This approach allows the user to key in all appropriate dimensions and properties into a text file and select ANSYS to read from the file and build the model to the user's specifications. The option certainly exists to use the GUI to manually build and mess models; however, this process can be very time consuming and difficult. Once the input file is created, the user can easily change values parametrically by simply keying in a new value in place of an existing one, and have ANSYS build the new model. This parametric modeling code has been omitted from this thesis due to proprietary rights of the research sponsor.

4.2 Material Properties

Several different materials make up an electronic package. Each material has its own material properties that are critical to the accuracy of FEA modeling. Some materials can be modeled accurately as linear elastic, while others, solder for example, require more complex material models. The Printed Circuit Board (PCB) FR4 material was modeled as linear elastic orthotropic. Many layers can exist in a PCB, as well as a large number of vias and circuit wiring throughout. For the purpose of model simplification, the PCB was modeled as a homogenous material. Also, Bismaleimide Triazine (BT) substrate material was modeled as linear elastic orthotropic. Like the PCB board, many layers can exist in the BT substrate, as well as a large number of vias and circuit wiring throughout. For the purpose of model simplification, the BT substrate was modeled as a homogenous material as well.

Two types of solder were used in the research presented: eutectic tin-lead solder (62Sn36Pb2Ag) and lead-free SAC305 (96.5Sn3.0Ag0.5Cu). Eutectic solder is the most popular choice for solder alloy; however, legislation has been passed and is being increasingly enforced banning the use of leaded solder alloys for important environmental and health concerns [Suhling, et.al. 2004]. Of the lead-free solder that have since been developed as a suitable replacement for eutectic solder; the SAC alloy has become the most popular choice. Since solder has a more complex material behavior than other board-level components, the modeling approach required more complexity. Solder alloy demonstrates time dependent and time independent behavior. A comprehensive list of all material properties used in the FEA models is shown in Table 4.1.

Table 4.1. Material Properties Used in Finite Element Model.

	E (Mpa)	Poisson's Ratio	CTE (1/K)	G (Mpa)
Copper Pad	129000	0.34	16.3E-6	
Solder Mask	3100	0.3	30.0E-6	
BT Substrate	17890 (XY) 7846 (Z)	0.39 (XZ & YZ) 0.11 (XY)	12.42E-6 (XY) 57.0E-6 (Z)	8061 (XY) 2822 (YZ & XZ)
Die Adhesive	6769	0.35	52E-6	
Silicon Die	163000	0.28	2.5E-06	
Ceramic	37000	0.22	7.40E-06	
Eutectic - 62Sn36Pb2Ag	30546	0.35	24E-6	
SAC305 – 96.5Sn3.0Ag0.5Cu	51000	0.35	25E-6	
Mold Compound	23520	0.3	15E-6	
PCB	27924-37T (XY) 12204-16T (Z)	0.39 (XZ & YZ) 0.11 (XY)	14.5E-6 (XY) 67.2E-6 (Z)	12600-16.7T (XY) 5500-7.3T (YZ & XZ)

4.3 Finite Element Modeling Approach

Linear, nonlinear, elastic, plastic, temperature, time-dependent, and time-independent material properties have been incorporated in the finite element models. It is known that solder is above half its melting point at room temperature [Darveaux 1992]. Because of this, time-dependent creep is the dominant factor in solder joint fatigue. The combined plastic deformation and creep of solder joints is the greatest contributor to thermal solder joint fatigue failures. The Anand Viscoplasticity model, which is a widely used to model the constitutive behavior of solder, and has been used in this study. The modeling methodology utilizes finite element analysis to calculate the viscoplastic strain energy density that is accumulated per cycle during thermal cycling. The strain energy density is then utilized with crack growth data to calculate time to crack initiation and propagation-to-failure. The Anand Viscoplasticity constitutive law has been used by

Darveaux [1996, 2000], and several other researchers, toward the development of damage relationships. Flow and evolution equations from Anand's model, shown in Equations 4.1-4.4, describe the strain hardening or softening of the materials [Brown, et. al., 1989]. Table 4.2 shows the constants used for Anand's model [Chang 2006, Darveaux 1996, 2000].

Flow Equation:

$$\frac{d\varepsilon_p}{dt} = A \left(\sinh(\xi\sigma/s_0) \right)_m^{\frac{1}{m}} \exp\left(\frac{-Q}{kT}\right) \quad (4.1)$$

Evolution Equations:

$$\frac{ds_0}{dt} = \left\{ h_0 (|B|)^a \frac{B}{|B|} \right\} \frac{d\varepsilon_p}{dt} \quad (4.2)$$

$$B = 1 - \frac{s_0}{s^*} \quad (4.3)$$

$$s^* = \hat{s} \left[\frac{\frac{d\varepsilon_p}{dt}}{A} \exp\left(\frac{Q}{kT}\right) \right]^n \quad (4.4)$$

Table 4.2. Anand's Constants for Solder Alloy.

Anand's constants for Solder Alloys				
SAC305	Eutectic			
96.5Sn3.0Ag0.5Cu [Chang 2006]	62Sn36Pb2Ag [Darveaux 1996, 2000]	ANSYS Input	Model Parameter	Definition
45.9	12.41	C1	So (MPa)	Initial Value of Deformation Resistance
7460	9400	C2	Q/k (1/K)	Activation Energy/Boltzmann's Constant
5.87E+06	4.00E+06	C3	A (1/sec)	pre-exponential factor
2.0	1.5	C4	ξ	multiplier of stress
0.0942	0.303	C5	m	stain rate sensitivity of stress
9350	1378.95	C6	ho (MPa)	hardening constant
58.3	13.79	C7	\hat{s} (MPa)	coefficient for deformation resistance saturation value
0.0015	0.07	C8	n	Strain rate sensitivity of saturation (deformation resistance) value
1.5	1.3	C9	a	strain rate sensitivity of hardening

Several researchers have established inelastic strain energy density (ISED) to be the damage proxy for solder joint thermo-mechanical reliability of electronic packages. Damage relationships correlating the solder joint life with the ISED accumulated per thermal cycle by the solder joint have also been developed. These relationships can be used for the life prediction of the electronic packages with solder joint cracking as the failure mode. The ISED can be calculated from the simulation. In ANSYSTM VISCO107 element has plastic work (PLWK) as a standard output, ISED has been calculated in the present study by volume averaging PLWK over the interface layers of the solder bump volume. Plastic work accumulated in the solder joint over the complete thermal cycle has been found to be stabilized after the first cycle. Consequently the simulation is run for

only two cycles and the ISED is calculated based on the plastic work accumulated during the second thermal cycle. ISED for the solder joint is given by:

$$\Delta W_i(\text{ISED}) = \frac{\left(\sum_{n=1}^{\text{total_elements}} \Delta W^{(n)} \times V_n \right)}{\left(\sum_{n=1}^{\text{total_elements}} V_n \right)} \quad (4.5)$$

where $\Delta W^{(n)}$ is plastic work accumulated by n^{th} element during the second thermal cycle of the simulation and it is standard output in ANSYSTM for VISCO107 element in form of PLWK and V_n volume of the n^{th} element. Damage relationships are shown in equations 4.6 through 4.8. The characteristic life of the component, α_{Joint} , is given by [Darveaux 1992, 1996]:

$$\alpha_{\text{Joint}} = N_0 + \frac{a}{\frac{da}{dN}} \quad (4.6)$$

$$N_0 = K_1 (\Delta W)^{K_2} \quad (4.7)$$

$$\frac{da}{dN} = K_3 (\Delta W)^{K_4} \quad (4.8)$$

Where “a” is the joint diameter at the interface, N_0 is the number of cycles for crack initiation, and $\frac{da}{dN}$ is the crack propagation rate. Once the value of ΔW is calculated from the FEA result, it can be applied in the above equations to predict the characteristic life of the package. The constants K_1 through K_4 are given in Table 4.3.

Table 4.3. Crack Initiation and Propagation Constants.

	K_1 (cycles/psi ^{K_2})	K_2	K_3 (in/cycle/psi ^{K_4})	K_4
Darveaux, et.al. [2000]	14.148	-1.64	1.704E-03	1.040
Lall, et.al.[2004]	14.062	-1.53	6.967E-04	0.7684

4.3.1 Anand Viscoplasticity

Viscoplasticity is the effect on a material over time from rate-dependent plasticity. It is known that rate-independence of plastic response is only a reasonable approximation at low temperatures. In actuality, this plastic flow is not truly rate-independent at lower temperatures either, but it is accepted and commonly used. The Anand Viscoplasticity model is a rate-dependent model and unlike the elasto-plastic model, it has no specific yield point. The plastic flow of this model is assumed to occur at all non-zero stress locations, and the equivalent plastic strain rate must be set by a suitable constitutive function.

4.3.2 ANSYS Element Types

The element types used for the 3D ANSYS slice models were the SOLID45 brick element, and the VISCO107 brick element. The SOLID45 element was used to model all materials and parts of the package slice model, except for the solder joint. The VISCO107 element was used to mesh the solder joints.

4.3.2.1 SOLID45 Element

The SOLID45 element is an 8-node brick element having three degrees of freedom at each node: translations in the nodal x, y, and z directions. The element has plasticity, creep, swelling, stress stiffening, large deflection, and large strain capabilities built into it. The geometry, node locations, and the coordinate system for this element are shown in Figure 4.3 [ANSYS 9.0 Tutorial].

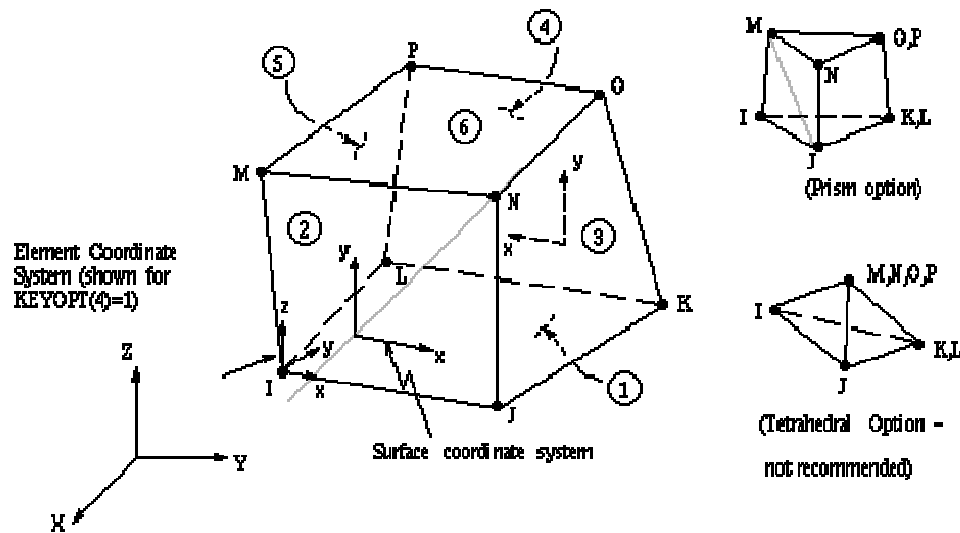


Figure 4.3. SOLID45 3-D Structural Solid

The element is defined by eight nodes, and the orthotropic material directions correspond to the element coordinate directions. Figure 4.4 shows the output stress for the SOLID45 brick element [ANSYS 9.0 Tutorial]. The element stress directions are parallel to the element coordinate system, and the surface stress outputs are in the surface coordinate systems, and are available for any face.

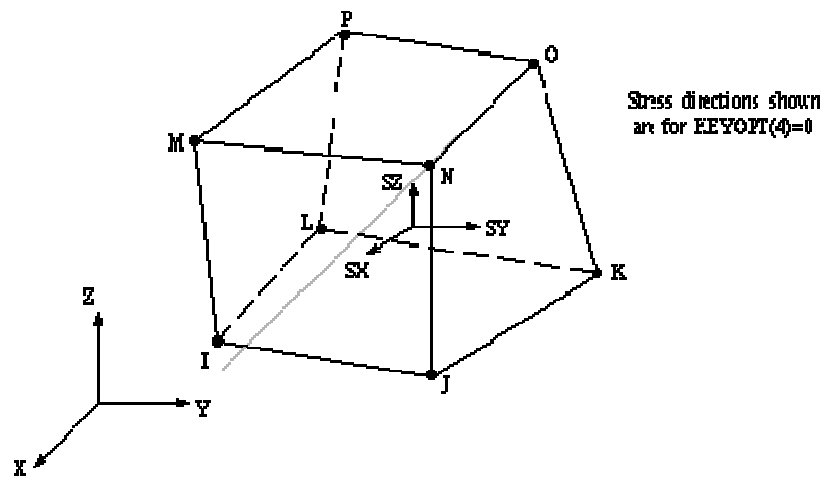


Figure 4.4. SOLID45 Stress Output

4.3.2.2 VISCO107 Element

The VISCO107 element is a more complex and application specific element than that of the SOLID45 for modeling 3-D solid structures. It is defined by eight nodes having three degrees of freedom at each node: translations in the nodal x, y, and z directions, and it is designed to solve both isochoric (volume preserving) rate-independent and rate-dependent large strain plasticity problems. Iterative solution procedures must be used with VISCO107 since it is used to represent highly nonlinear behavior. Also, large deflections must be active in order to update the geometry after

each sub-step. The geometry, node locations, and the coordinate system for the VISCO107 element are shown in Figure 4.5 [ANSYS 9.0 Tutorial].

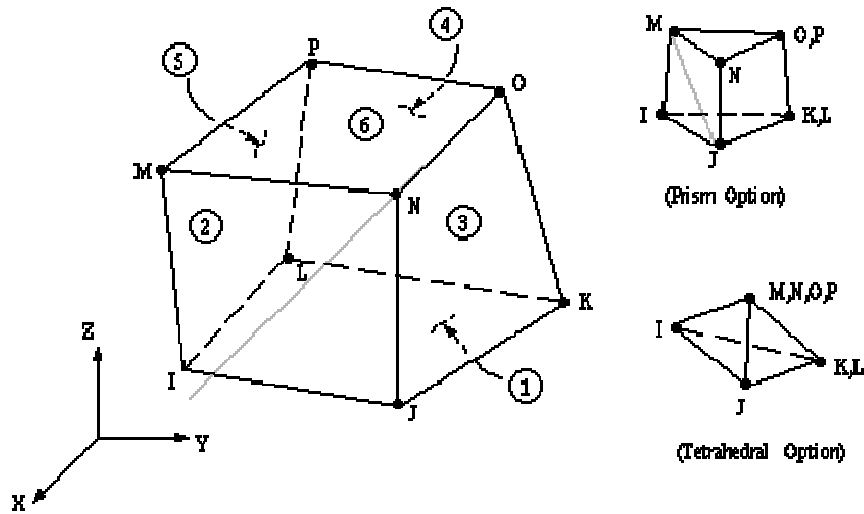


Figure 4.5. VISCO107 3-D Large Strain Solid

The element is defined by eight nodes having linear and nonlinear material properties. Figure 4.6 shows the output stress for the VISCO107 brick element [ANSYS 9.0 Tutorial]. The element stress directions are parallel to the rotated element coordinate system.

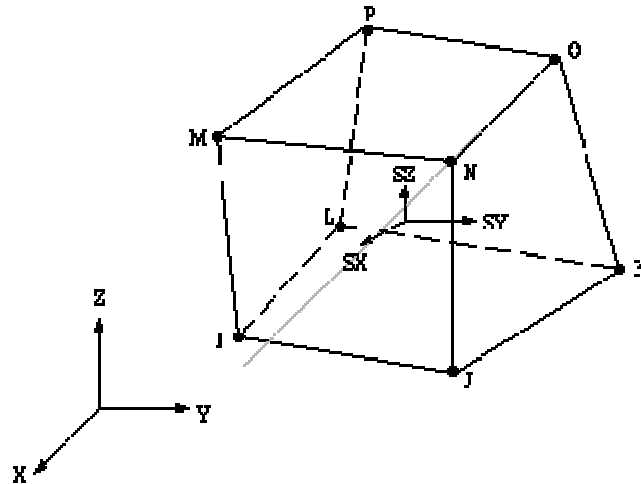


Figure 4.6. VISCO107 Default (No ESYS) Element Coordinate System

4.3.3 Modeling Assumptions

Finite element modeling is a very useful tool for analyzing complex stress and strain results; however, for an answer to be accurate, knowledge of modeling methods and assumptions is needed. Several assumptions were made in modeling electronic packages. Due to memory limits and computational time, and to very complex geometries, intelligent simplifications can be made to advance the modeling process. One simplification made was to model the BT Substrate and PCB board as a homogeneous material. In reality, these two components many have several layers of board layering, adhesive, and circuit wiring. These very small features require extensive time to model, and due to their extremely small size relative to the package structure, they cannot be meshed in a useful manner. Meshing objects such as these would be very difficult for the user and would add enormous extra computational time, as well as jeopardizing analysis results due to the increased risk of element shear locking.

Similar to the homogeneity of the board materials, the solder joints are assumed to be homogeneous. In reality, the solder joints are not perfectly blended, and often contain air bubble gaps within them called voids. These voids can add or hinder the thermal reliability of the solder joint. Also, stress and strain near the interface of the solder joint due to thermal cycling can alter the chemical composition and grain structure of the alloy. This condition is unfortunately impossible to effectively model with today's technology.

This assumption of homogeneity is also applied to the mold compound. Similar to voids in solder joints, mold compound contains tiny spheres of glass silica that are used as a filler material to lessen the processing cost of the epoxy, and the most important feature, to reduce the compound CTE to more closely match the silicon chip. Other main assumptions are in choosing boundary conditions.

4.3.4 Boundary Conditions

There are three main types of finite element modeling options: full model, quarter symmetry model, and diagonal slice model. Diagonal slice modeling was chosen for modeling in this research due to reduced computational time and memory. The diagonal slice model extends from the center of a package out to the outermost corner solder joint. In this modeling approach, all materials are included through the thickness of the package, and the model captures a full row of solder joints from the center joints to the outermost joints. When the model itself is simplified, the boundary condition choices become more important on the effect of analysis. This slice plane is neither a true symmetry plane nor a free surface [Zahn 2002]. A compromise between the two options is to couple the surface. For the slice plane surface, a coupling boundary condition of UY

on all nodes on the surface was chosen, and allows the plane to move freely in the Y direction, but is restricted in that plane. All boundary conditions applied for slice models in this research are displayed in Figure 4.7.

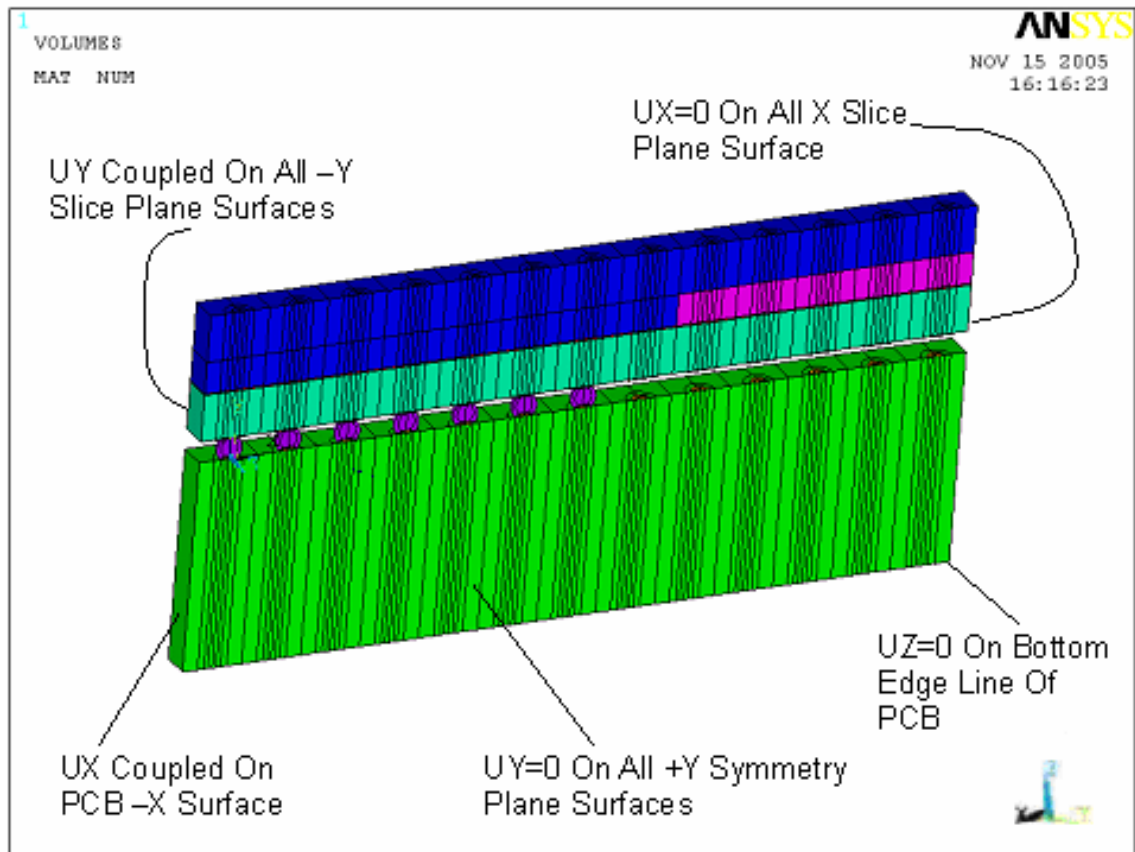


Figure 4.7. Boundary conditions used for typical slice models.

4.4 Non-Linear Finite Element Model for 532 I/O BGA

The Flip Chip Ball Grid Array (FCBGA) package was modeled in ANSYS 9.0 for thermal cycling plastic work accumulation in order to determine accelerated test dwell time parameters, particularly whether 30 minute dwell times added any significant increase in the amount of damage accumulation versus 20 minute dwells. Figure 4.8 shows the footprint of the 532 I/O package, along with a highlighted area designating the slice model area. Table 4.4 displays dimensions for this package.

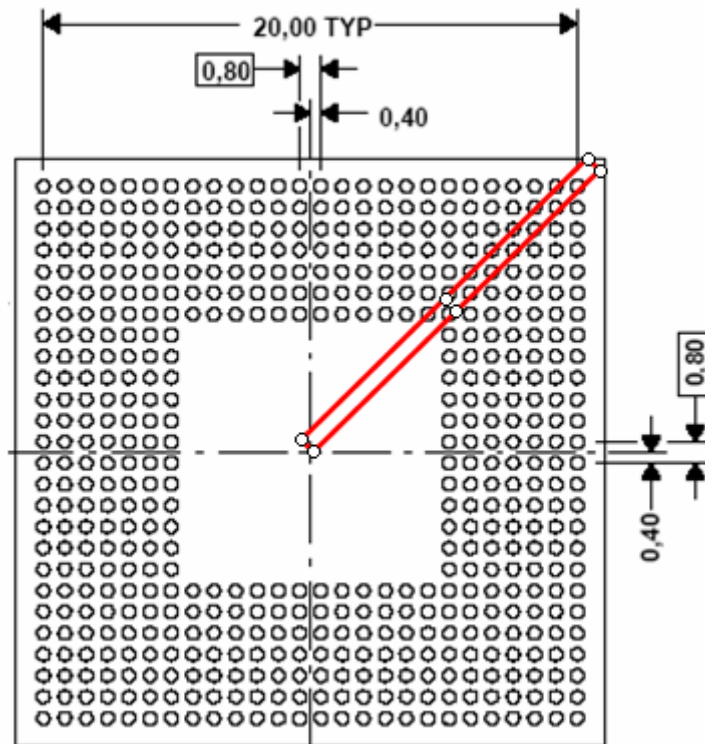


Figure 4.8. Footprint of the 532 I/O BGA package.

Table 4.4. Dimensions for FCBGA 532.

Package	Ball Count	Ball Pitch (mm)	Package Size (mm)	BT Thickness (mm)	Ball Diameter (mm)
FCBGA532	532	0.8	23x23	0.56	0.49

The meshing of the finite element slice model was done using a mapped mesh technique that provides a uniform mesh over the volume. VISCO107 elements were used to mesh the solder balls, whereas all other volumes were meshed with SOLID45 brick elements. Only a slice of the entire package was needed to run an accurate analysis because of the internal symmetry of the components. By using a diagonal slice (from the center of the package to the outer-most corner) to model the effects of the whole package, the worst-case scenario is simulated since the perimeter solder joint represents the furthest solder joint from the package center [Zahn 2003].

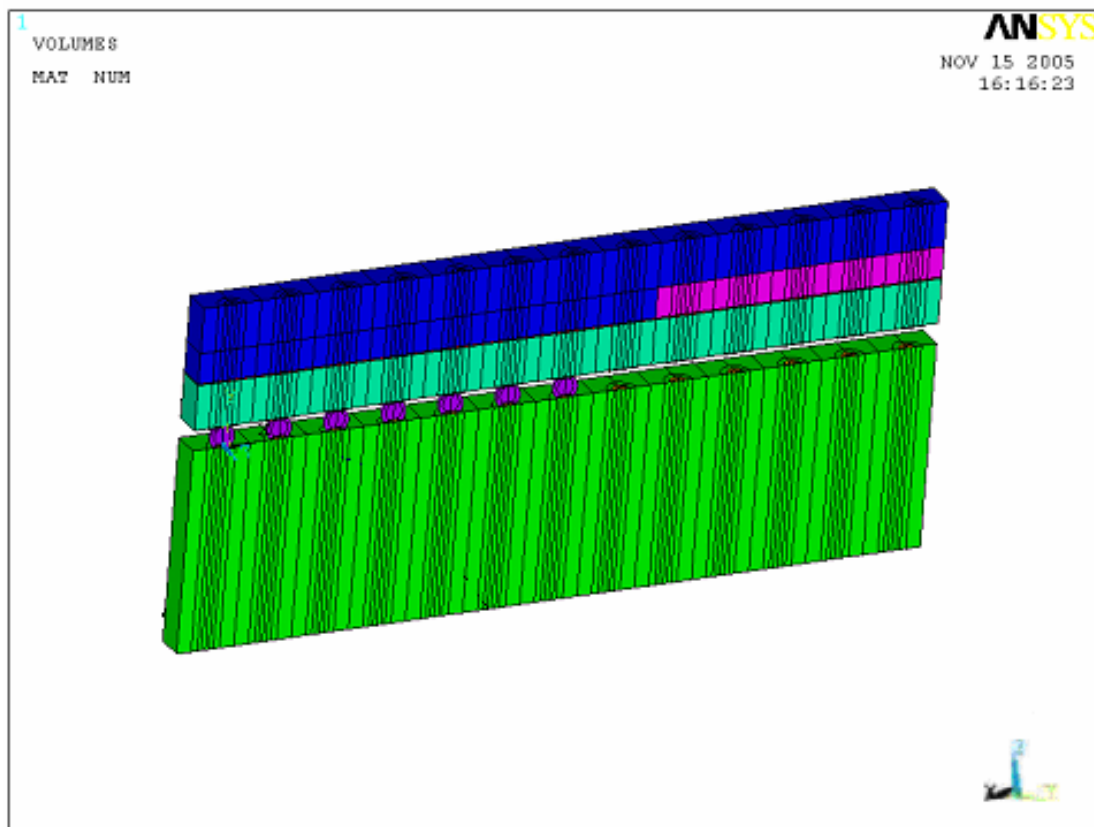


Figure 4.9. Isometric volumetric plot of the 532 I/O slice model.

Figure 4.10 displays the contour plot of plastic work accumulation over all of the solder joints. Figure 4.11 show a close-up contour plastic work plot of the most critical solder joint.

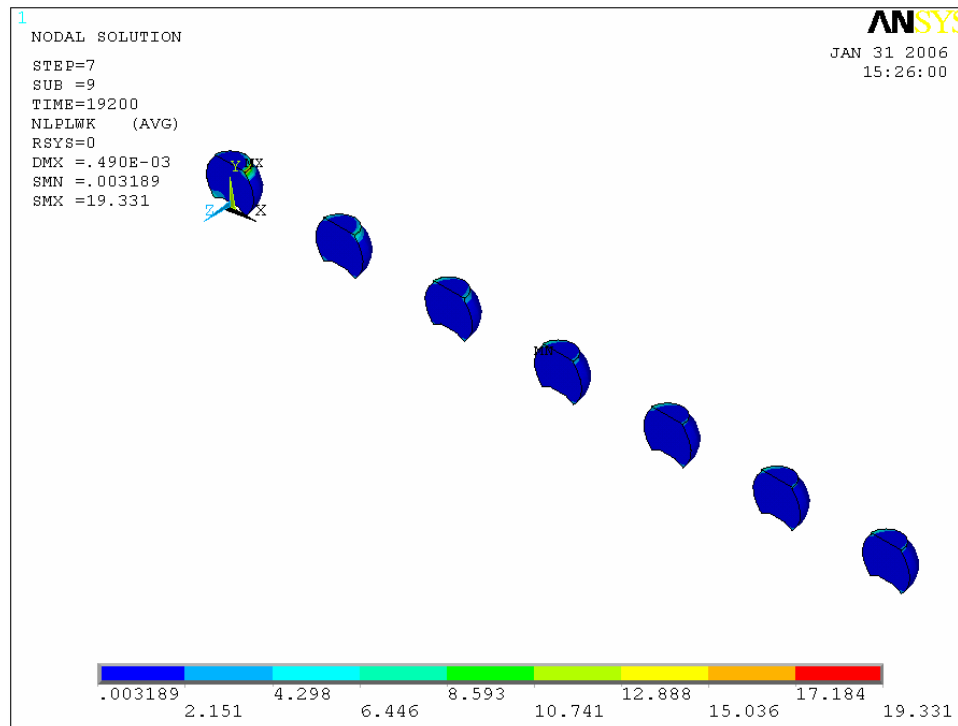


Figure 4.10. Contour plot of accumulated plastic work on the solder joints.

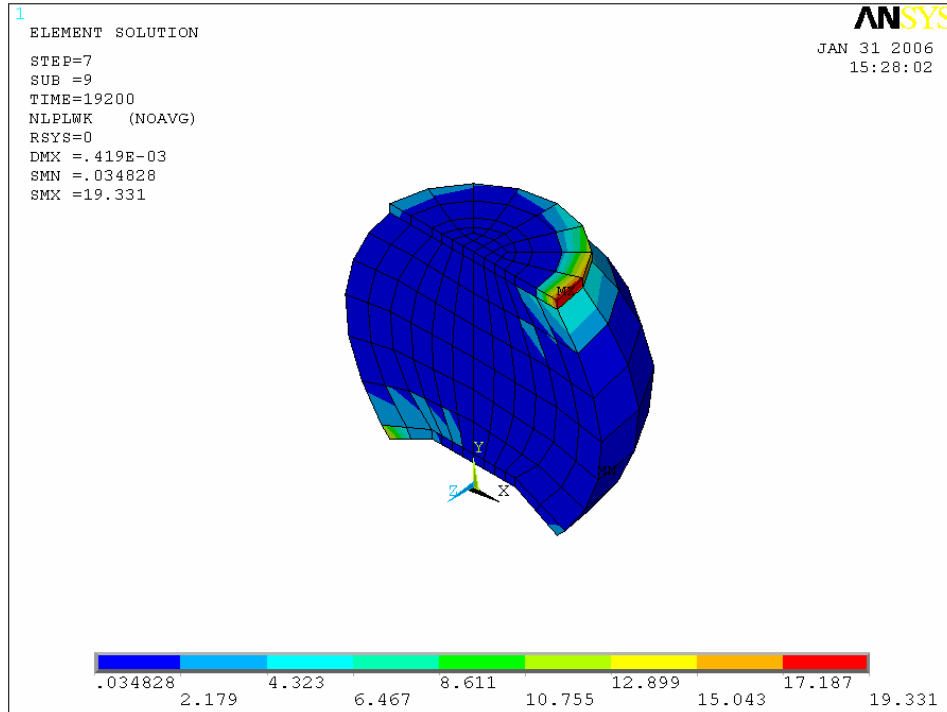


Figure 4.11. Contour plot of accumulated plastic work on the critical solder joint.

This package was model was analyzed for 20 minute dwell times and 30 minute dwell times for a temperature cycling condition of -55 °C to 125 °C. The stress, strain, and hysteresis loop plot results for the models are shown in figures 4.12 through 4.17 respectively.

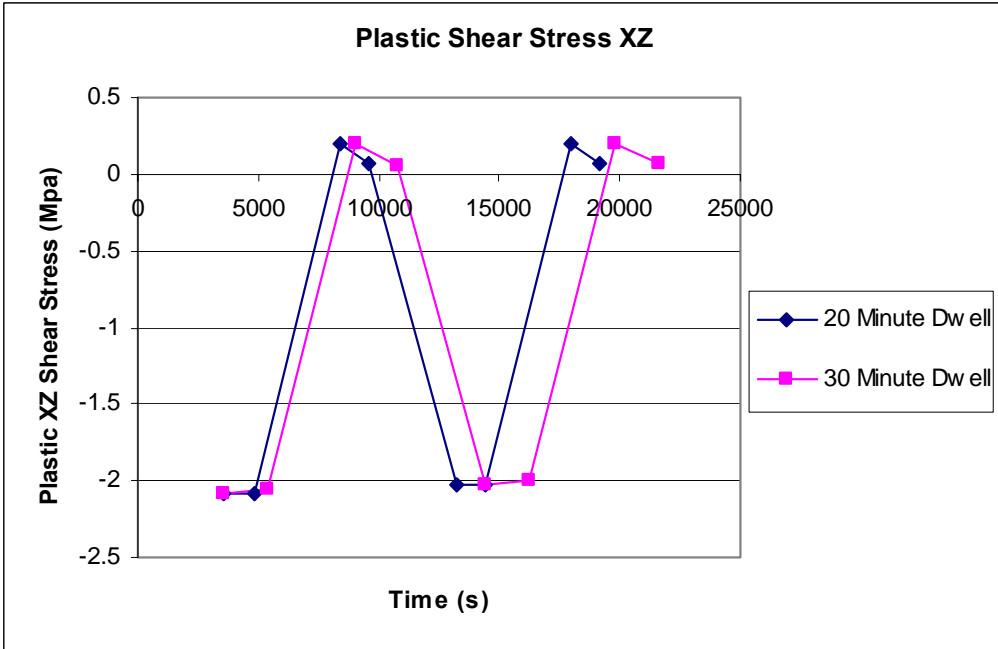


Figure 4.12. Plastic shear stress plot results for the XZ plane.

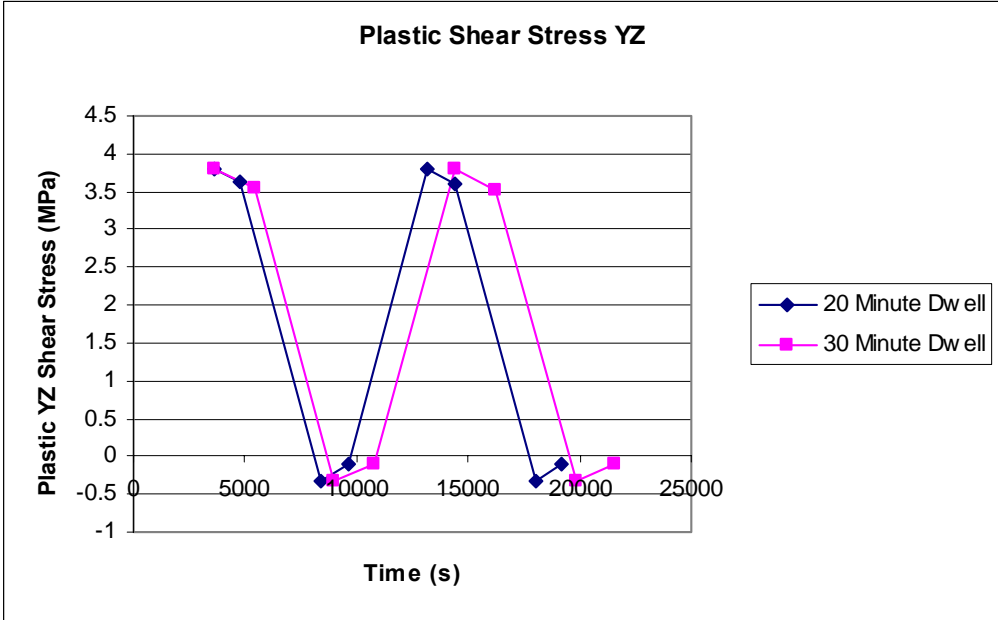


Figure 4.13. Plastic shear stress plot results for the YZ plane.

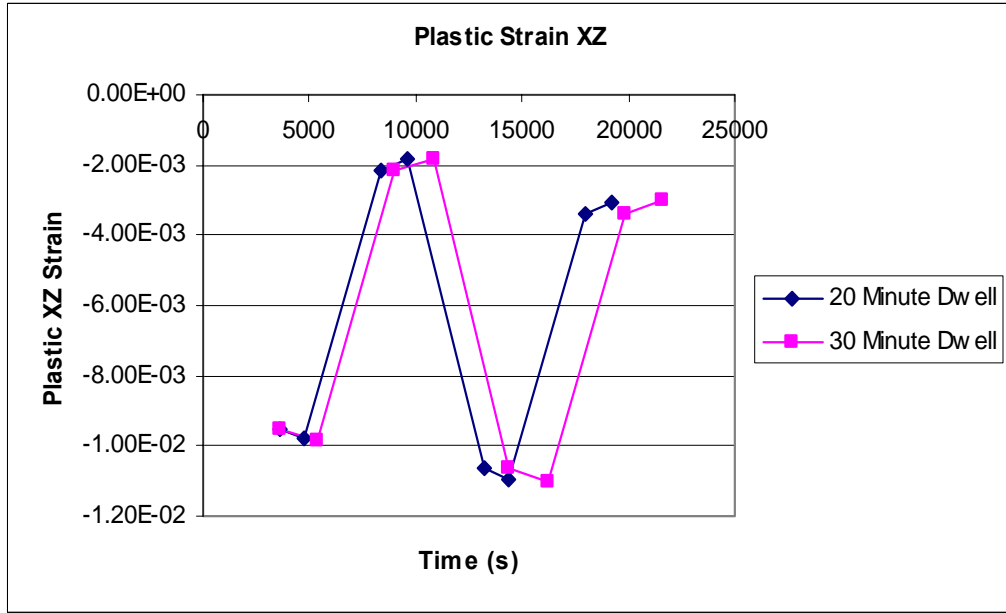


Figure 4.14. Plastic shear strain plot results for the XZ plane.

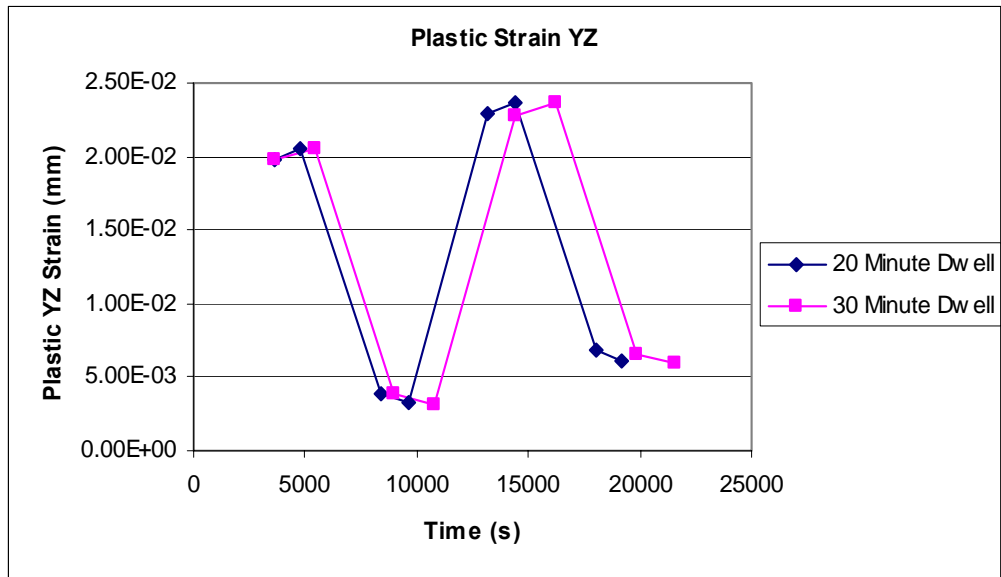


Figure 4.15. Plastic shear strain plot results for the YZ plane.

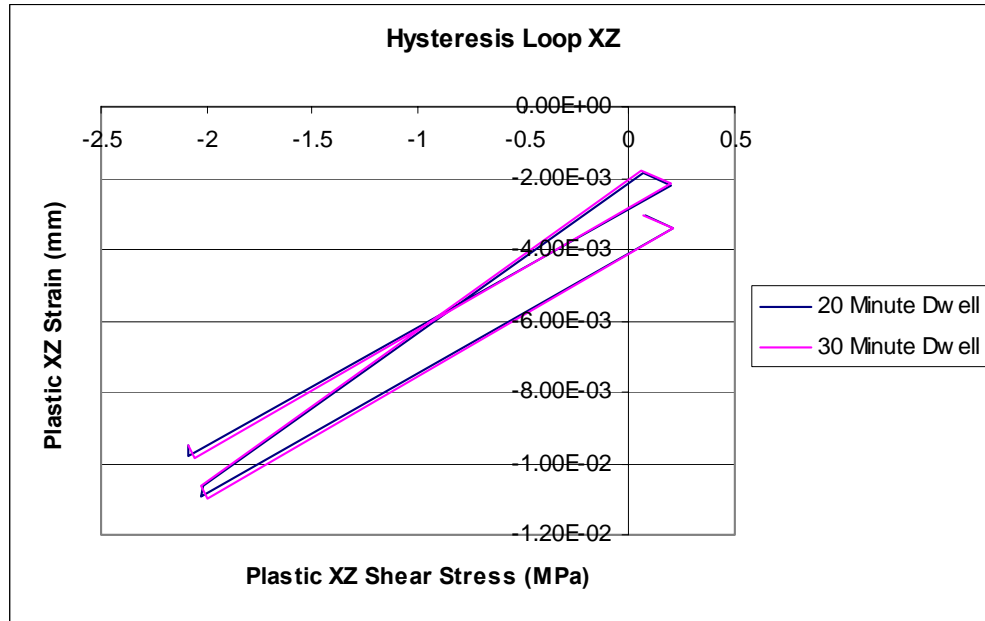


Figure 4.16. Hysteresis loop plot results for the XZ plane.

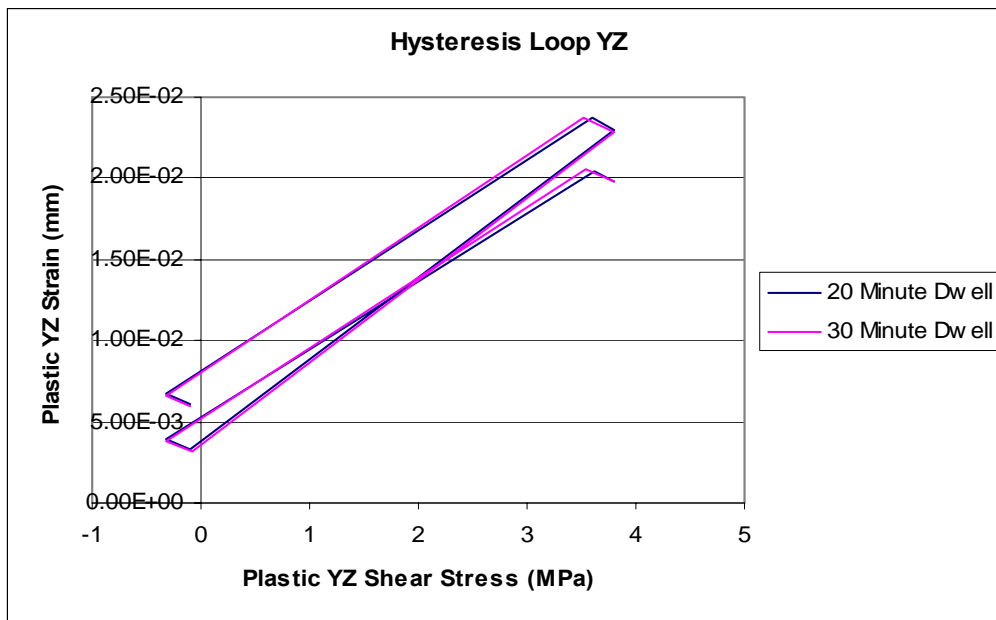


Figure 4.17. Hysteresis loop plot results for the YZ plane.

From the results it was determined that no significant additional damage was accumulated from the longer 30 minute dwell times, and therefore the 20 minute dwell

times could be chosen for the accelerated test conditions to reduce testing time. From Figures 4.16 and 4.17, it is shown that the hysteresis loops are virtually overlapping, and thus illustrating that nearly identical plastic work damage is being accumulated from the 20 and 30 minute dwell time conditions. Despite this, 30 minute dwell times were chosen for the accelerated thermal cycle testing at the sponsor's request.

4.5 Non-Linear Finite Element Model for 49 I/O BGA

The Altera 49-Pin Ultra Fine Line Ball-Grid Array (UBGA) package was modeled in ANSYS 9.0 for thermal cycling plastic work accumulation. The complete model was meshed with a mapped meshing technique that involved 203,752 nodes and 194,952 elements. The typical computer solution processing time was 27 hours (Dual Processor, 2.8 GHz Pentium IV).

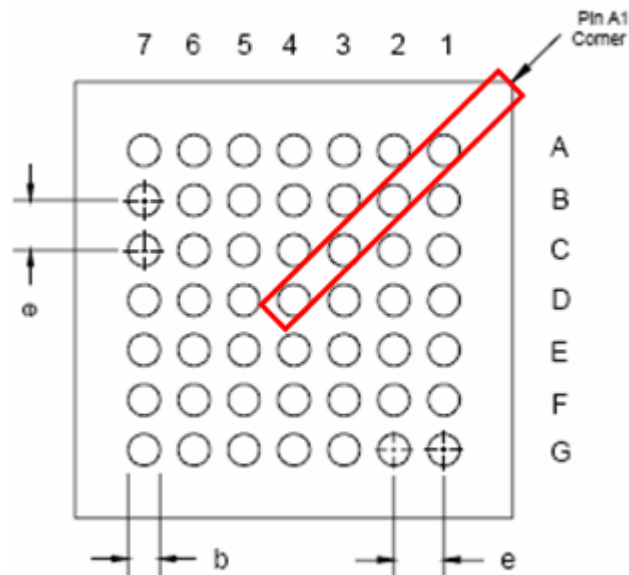


Figure 4.18. Footprint of UBGA 49 package.

The meshing of the finite element slice model was done using a mapped mesh technique that provides a uniform mesh over the volume. VISCO107 elements were used to mesh the solder balls, whereas all other volumes were meshed with SOLID45 brick elements. Only a slice of the entire package was needed to run an accurate analysis because of the internal symmetry of the components. By using a diagonal slice (from the center of the package to the outer-most corner) to model the effects of the whole package, the worst-case scenario is simulated since the perimeter solder joint represents the furthest solder joint from the package center [Zahn 2003].

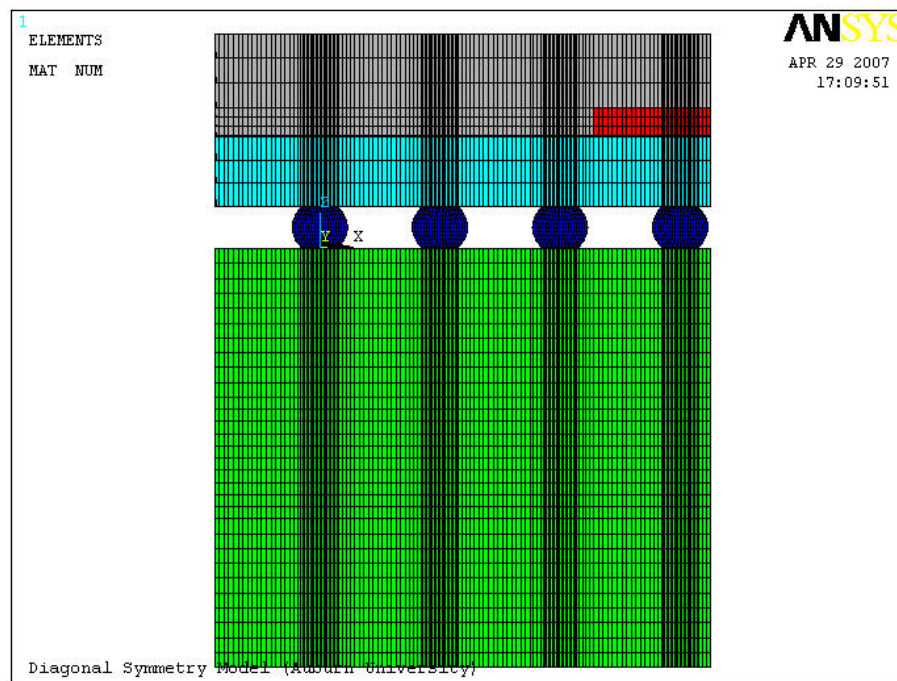


Figure 4.19. Front view of UBGA 49 Finite Element Model.

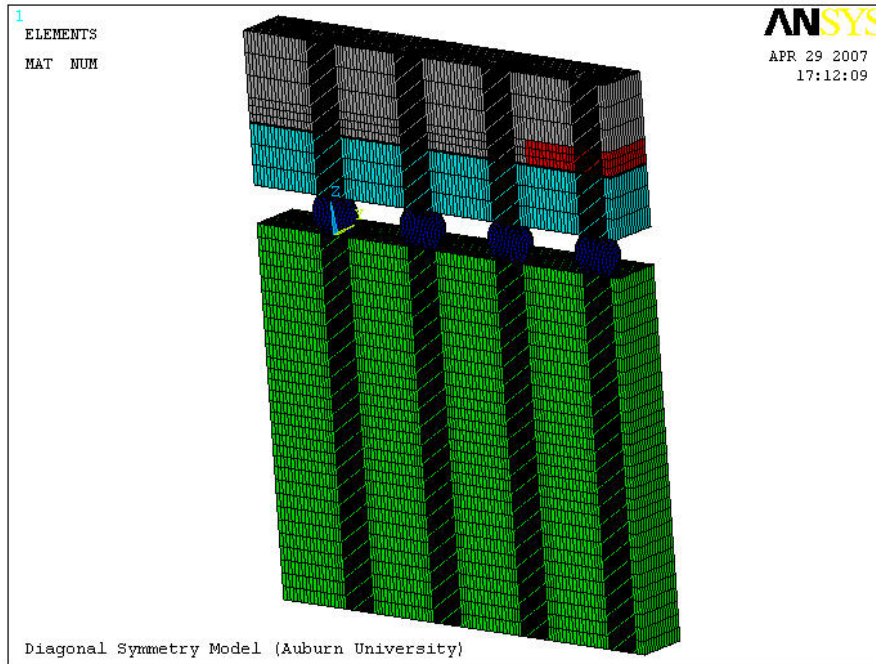


Figure 4.20. Isometric view of UBGA 49 Finite Element Model

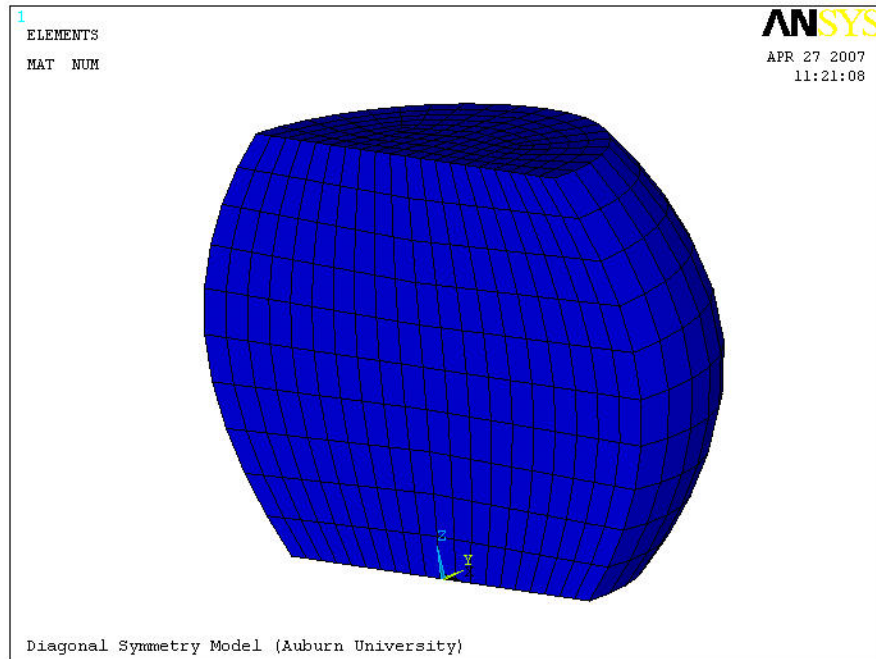


Figure 4.21. Isometric view of solder joint.

The UBGGA 49 model was analyzed for a variety of conditions: -55C to 125C (TC2), 3C to 100C (TC3), and -20C to 60C (TC4). For all temperature conditions, eutectic (62Sn36Pb2Ag) and SAC305 solder alloy models were analyzed.

4.5.1 Eutectic Solder

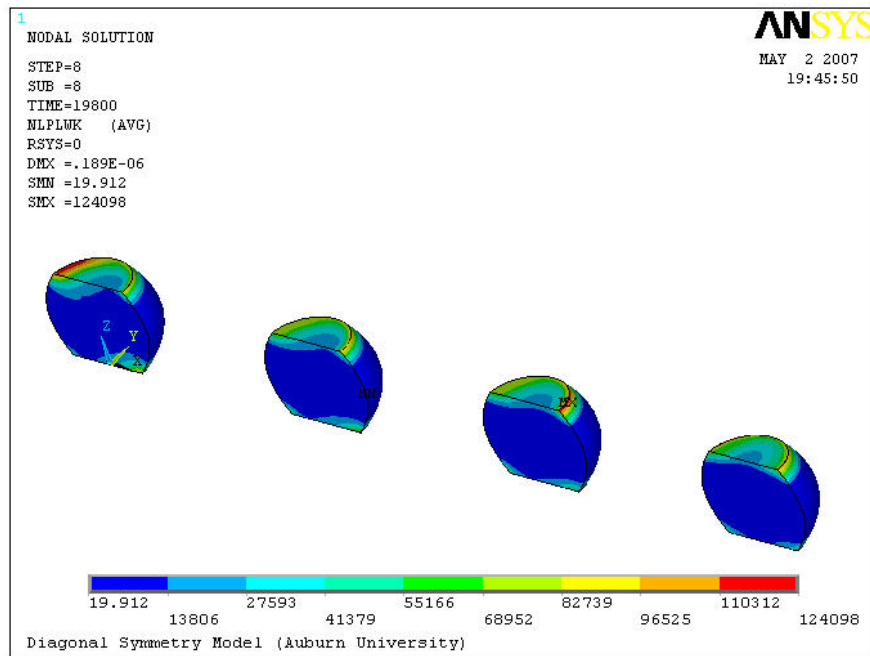


Figure 4.22. Plastic work plot of all eutectic solder joints subjected to TC2 condition.

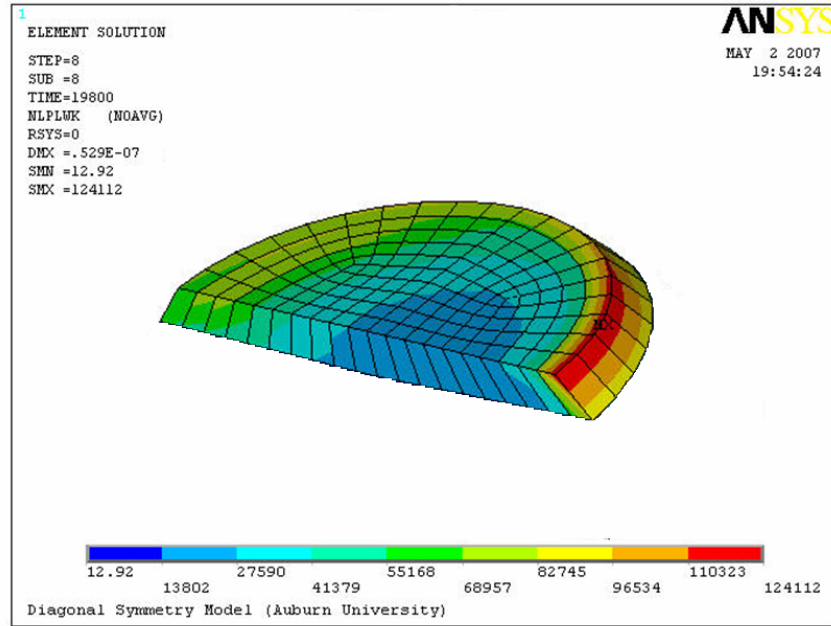


Figure 4.23. Plastic work plot of most critical solder joint interface surface subjected to TC2 condition.

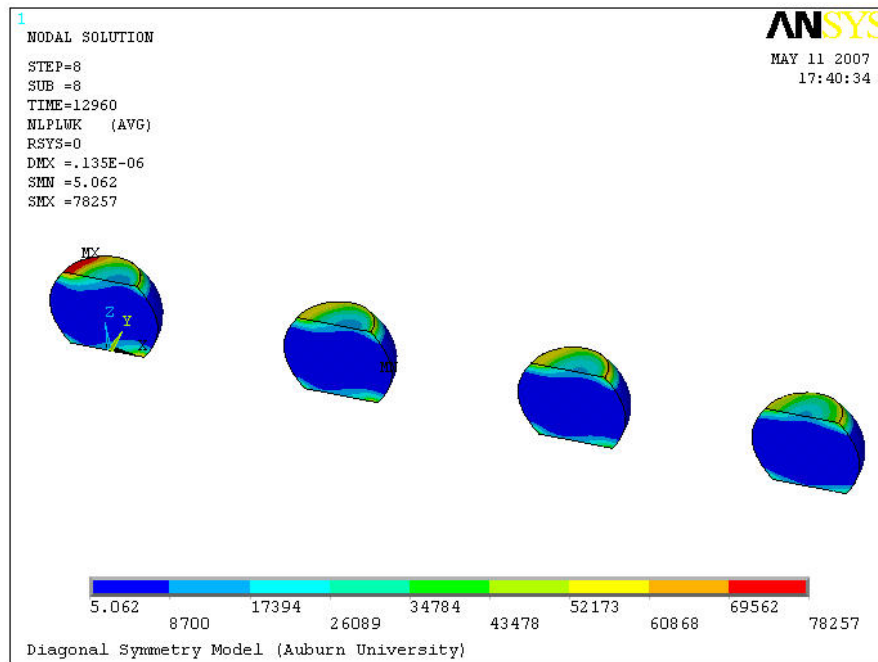


Figure 4.24. Plastic work plot of all eutectic solder joints subjected to TC3 condition.

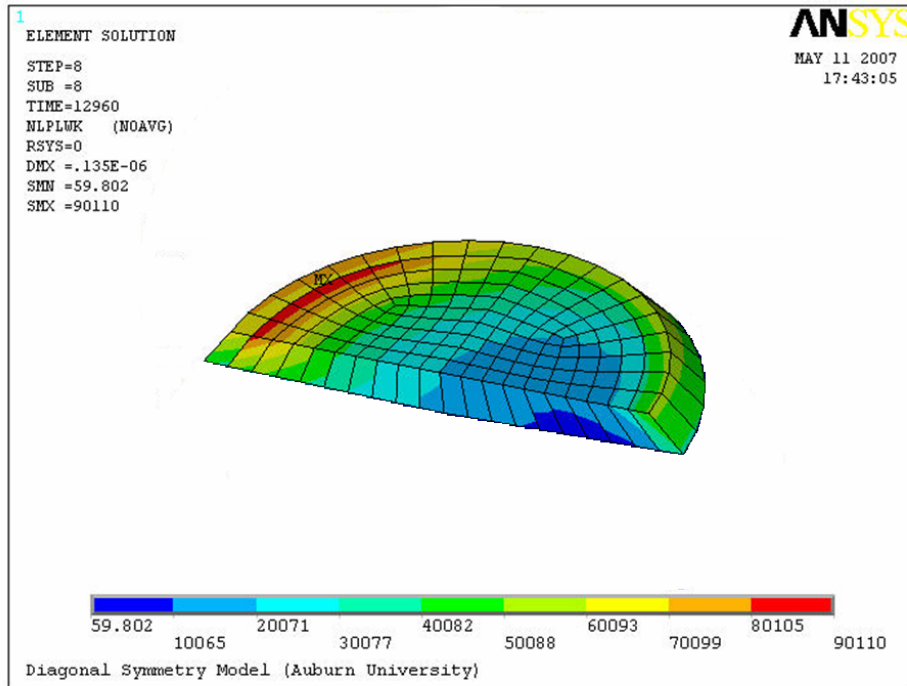


Figure 4.25. Plastic work plot of most critical solder joint interface surface subjected to TC3 condition.

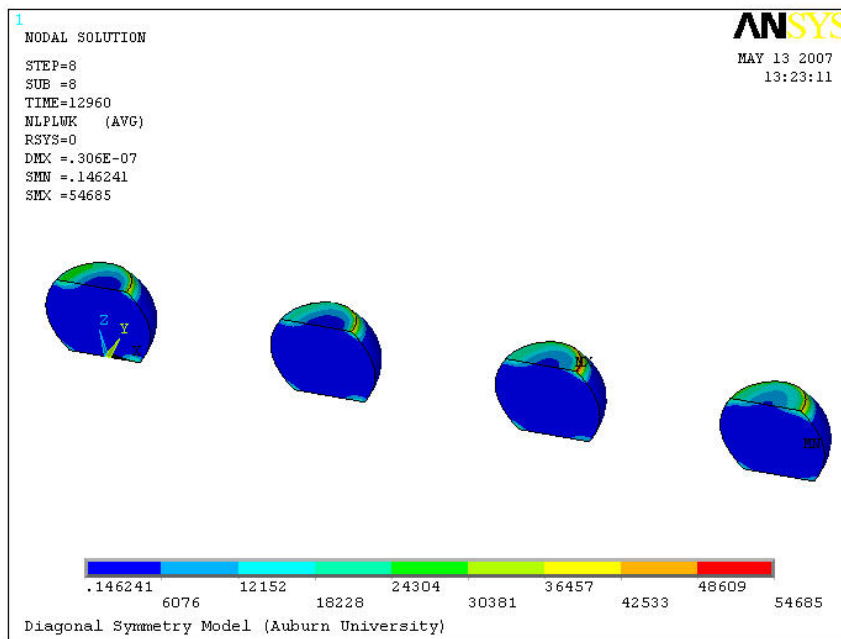


Figure 4.26. Plastic work plot of all eutectic solder joints subjected to TC4 condition.

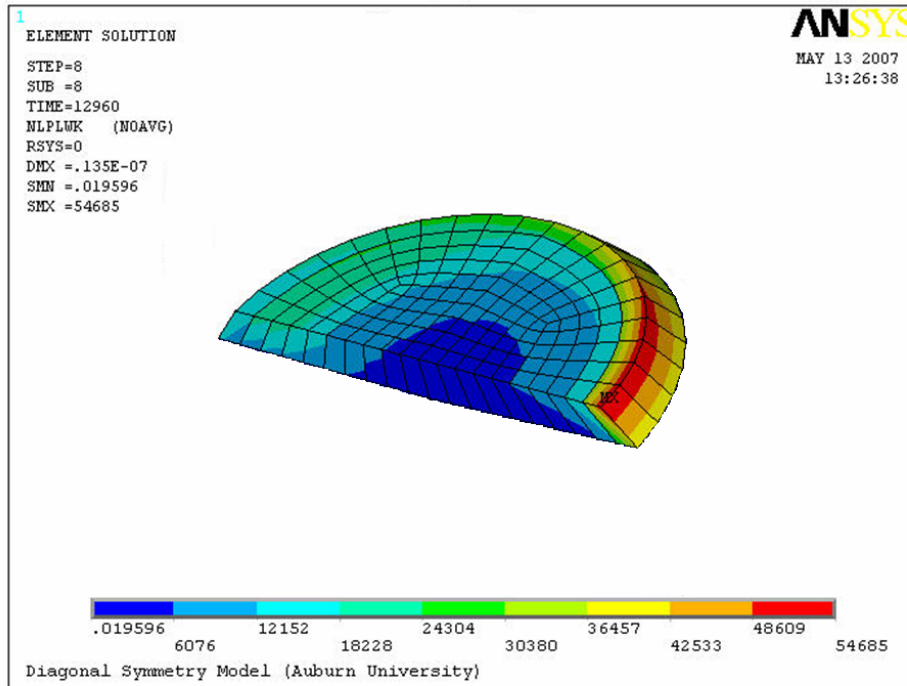


Figure 4.27. Plastic work plot of most critical solder joint interface surface subjected to TC4 condition.

Figures 4.28 through 4.33 display the XY and YZ shear stress plots of eutectic solder for temperature conditions TC2, TC3, and TC4. To properly display the high stress regions of some solder joint plots, the joints were rotated 180 degrees about the x-axis.

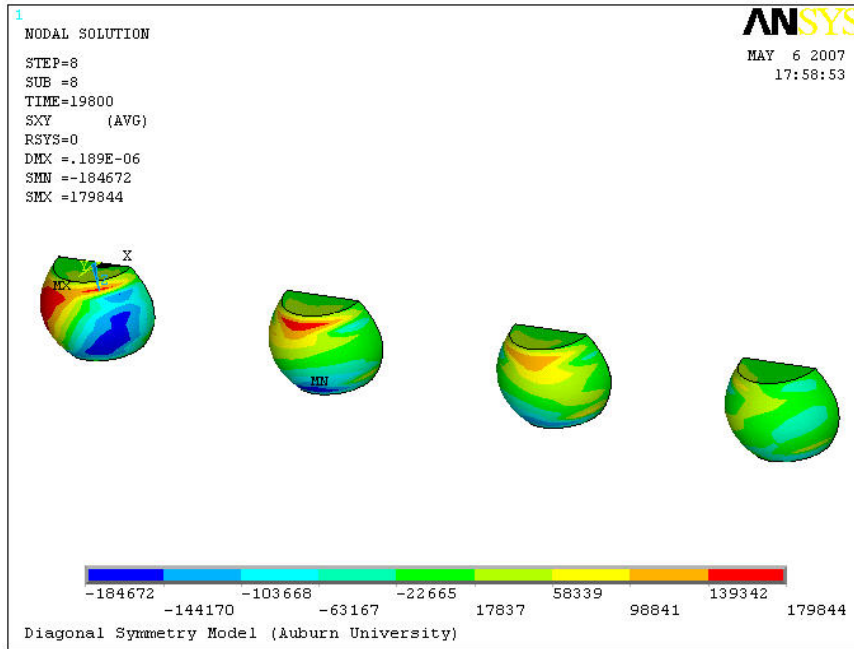


Figure 4.28. XY Shear Stress plot of all eutectic solder joints subjected to TC2 condition.

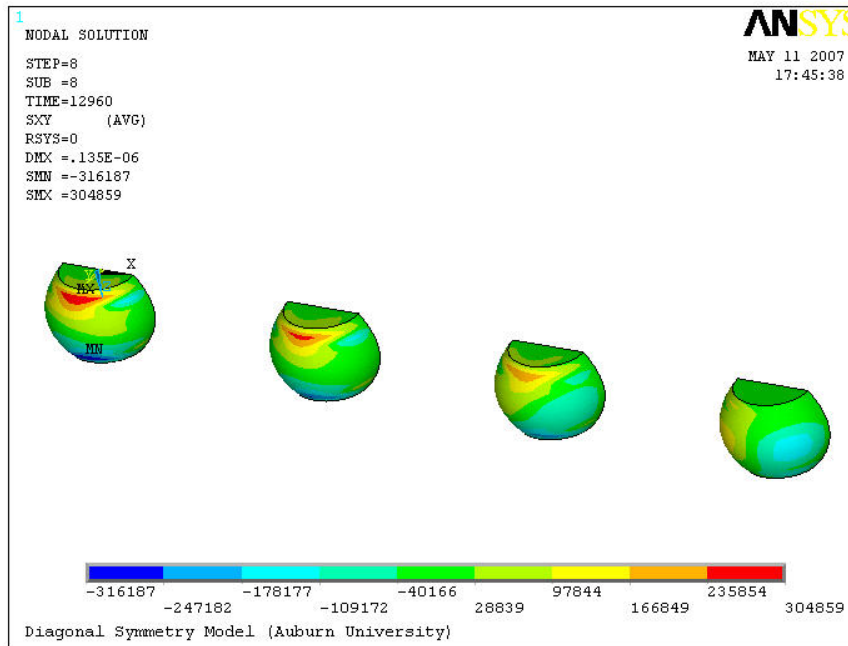


Figure 4.29. XY Shear Stress plot of all eutectic solder joints subjected to TC3 condition.

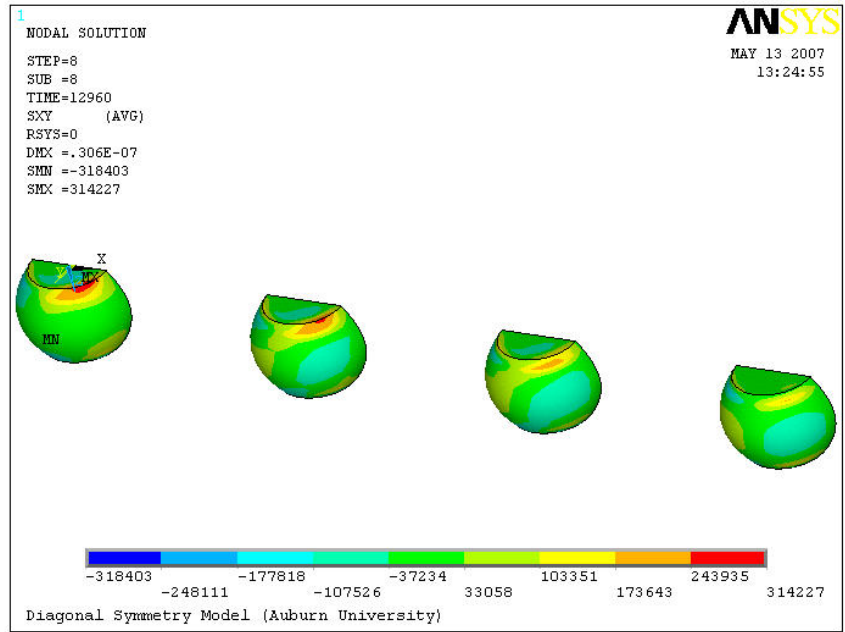


Figure 4.30. XY Shear Stress plot of all eutectic solder joints subjected to TC4 condition.

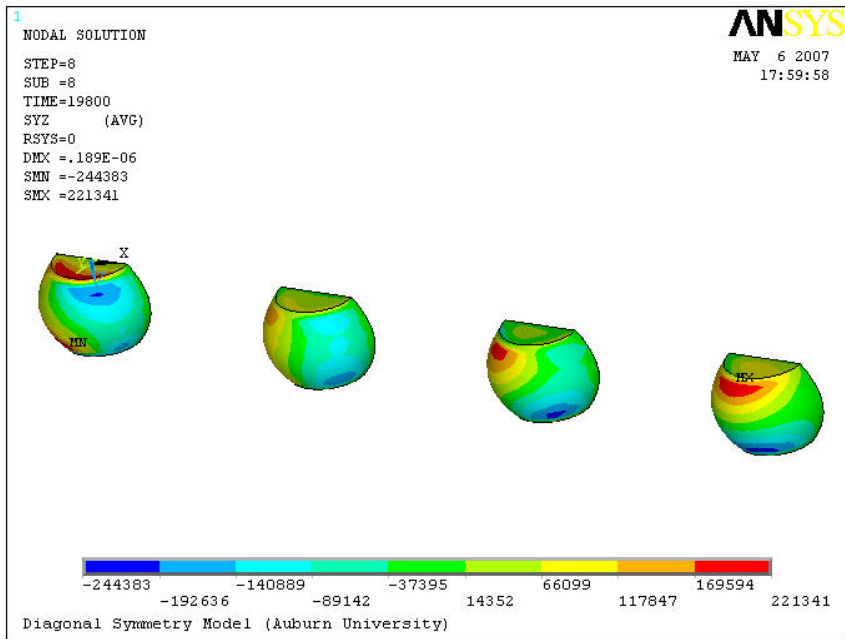


Figure 4.31. YZ Shear Stress plot of all eutectic solder joints subjected to TC2 condition.

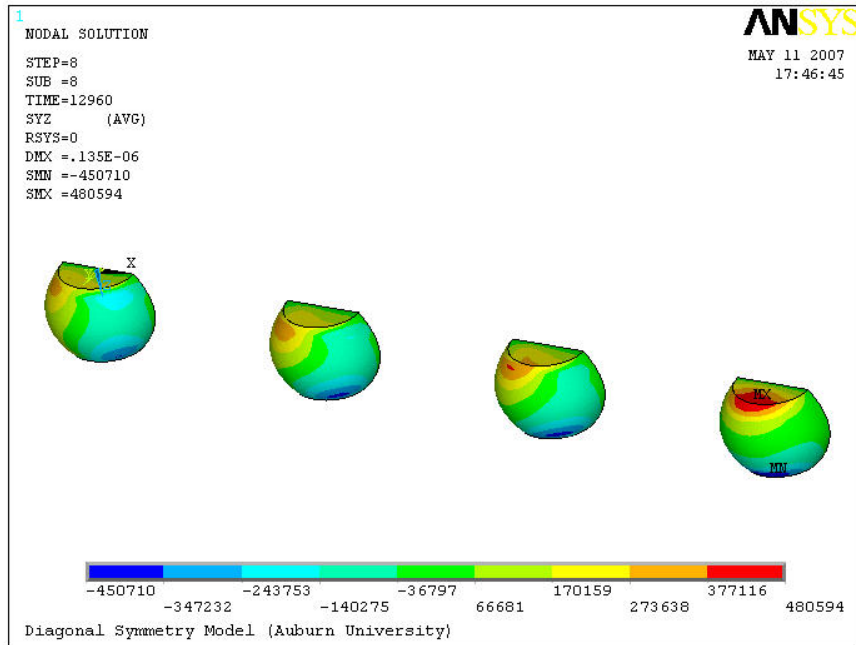


Figure 4.32. YZ Shear Stress plot of all eutectic solder joints subjected to TC3 condition.

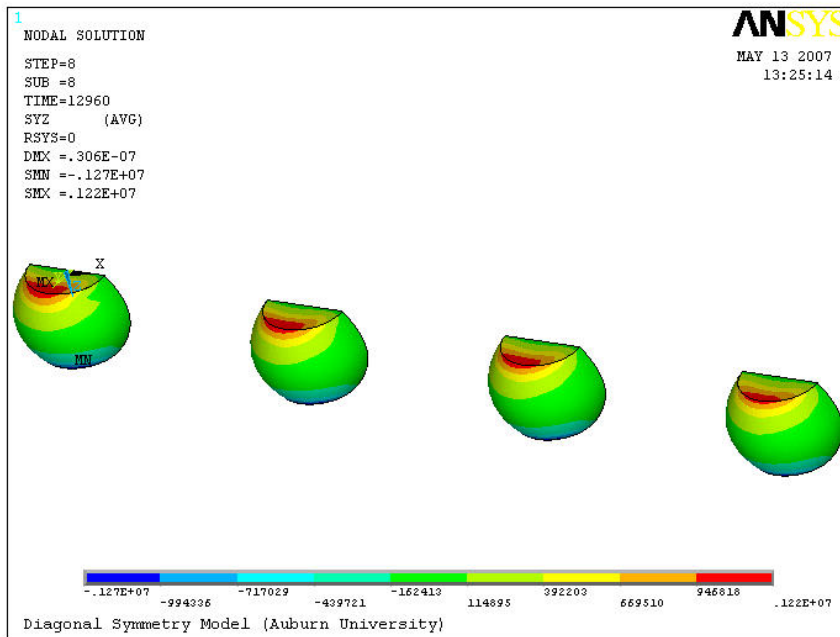


Figure 4.33. YZ Shear Stress plot of all eutectic solder joints subjected to TC4 condition.

4.5.2 SAC305 Solder

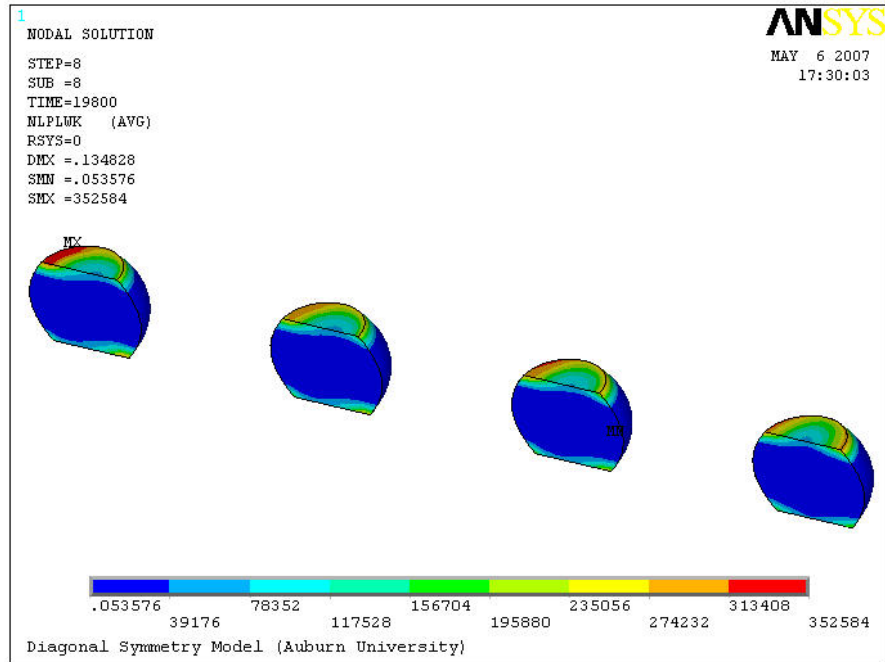


Figure 4.34. Plastic work plot of all SAC305 solder joints subjected to TC2 condition.

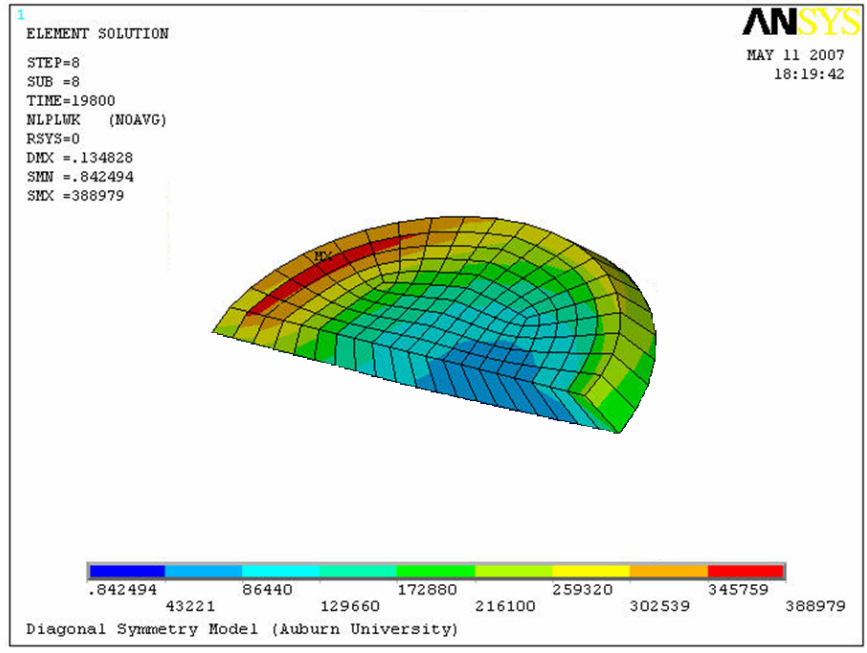


Figure 4.35. Plastic work plot of most critical solder joint interface surface subjected to TC2 condition.

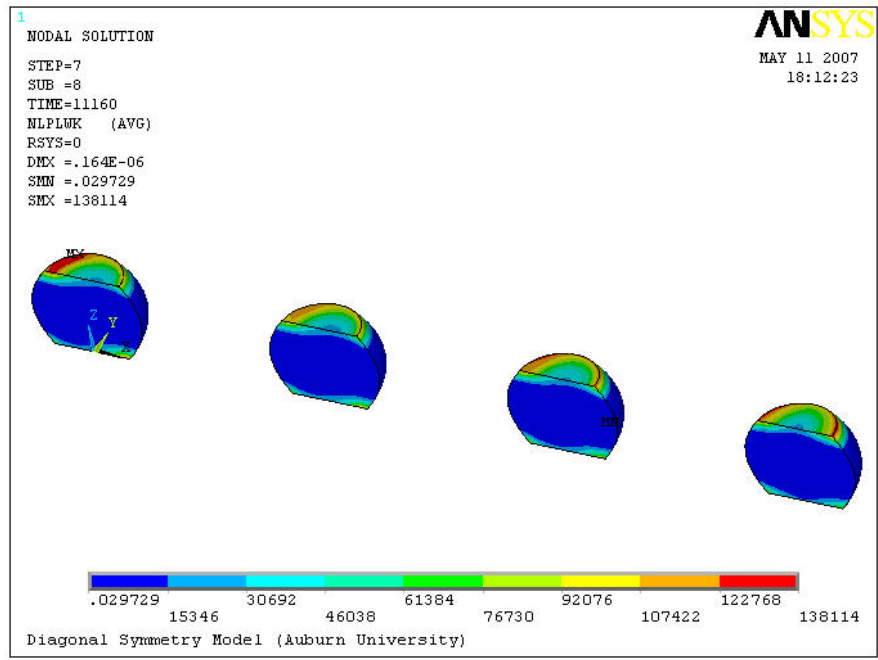


Figure 4.36. Plastic work plot of all SAC305 solder joints subjected to TC3 condition.

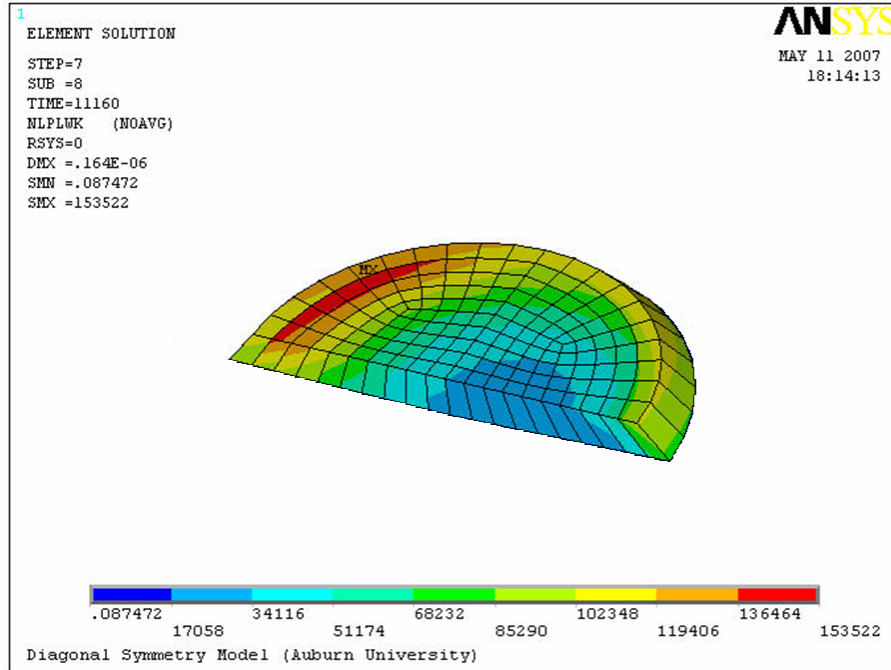


Figure 4.37. Plastic work plot of most critical solder joint interface surface subjected to TC3 condition.

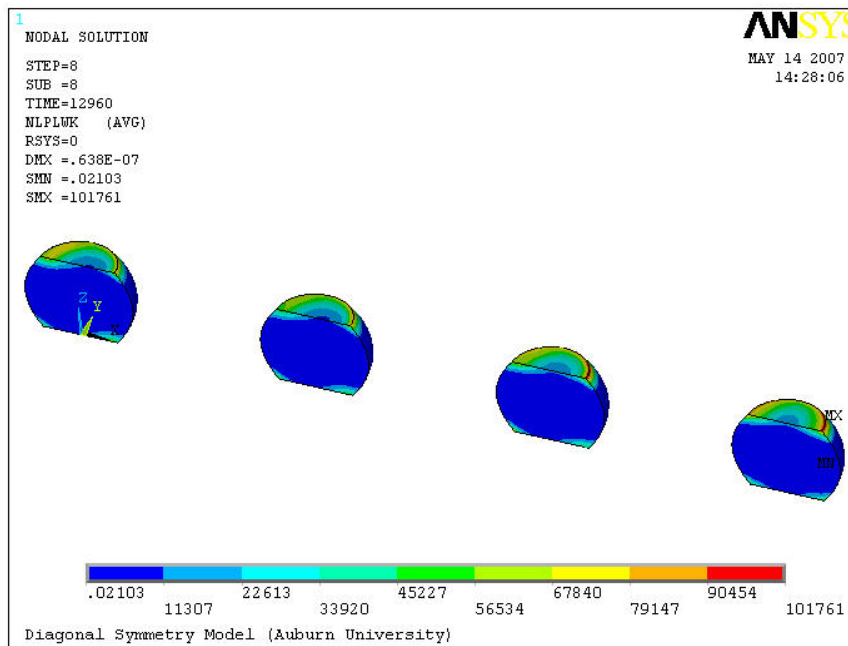


Figure 4.38. Plastic work plot of all SAC305 solder joints subjected to TC4 condition.

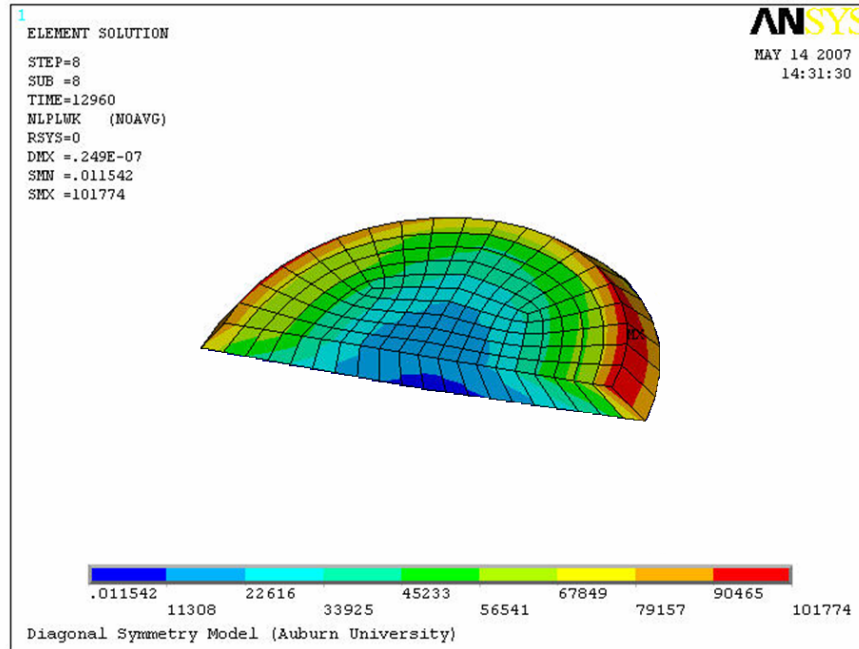


Figure 4.39. Plastic work plot of most critical solder joint interface surface subjected to TC4 condition.

Figures 4.40 through 4.45 display the XY and YZ shear stress plots of SAC305 solder for temperature conditions TC2, TC3, and TC4. To properly display the high stress regions of some solder joint plots, the joints were rotated 180 degrees about the x-axis.

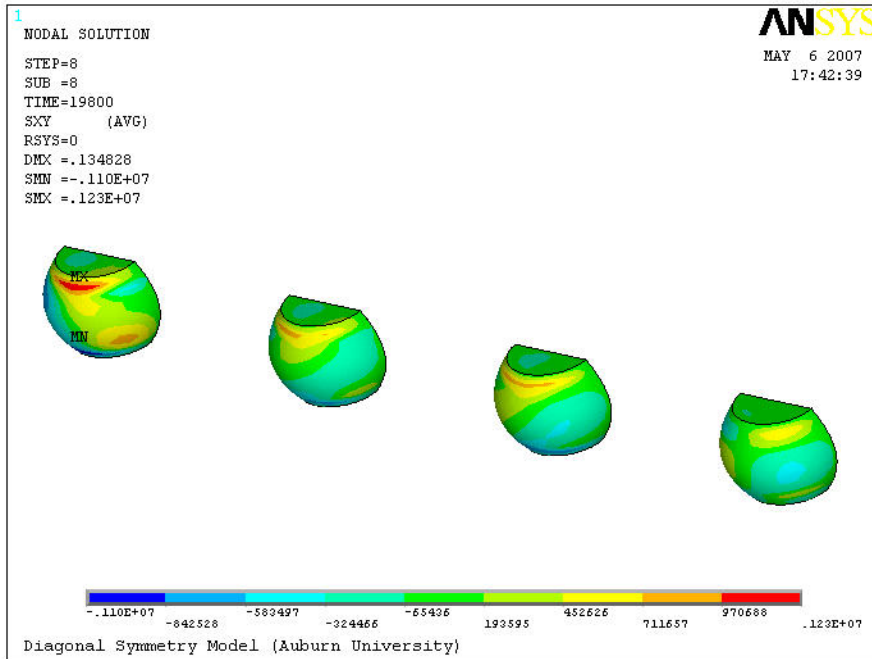


Figure 4.40. XY Shear Stress plot of all SAC305 solder joints subjected to TC2 condition.

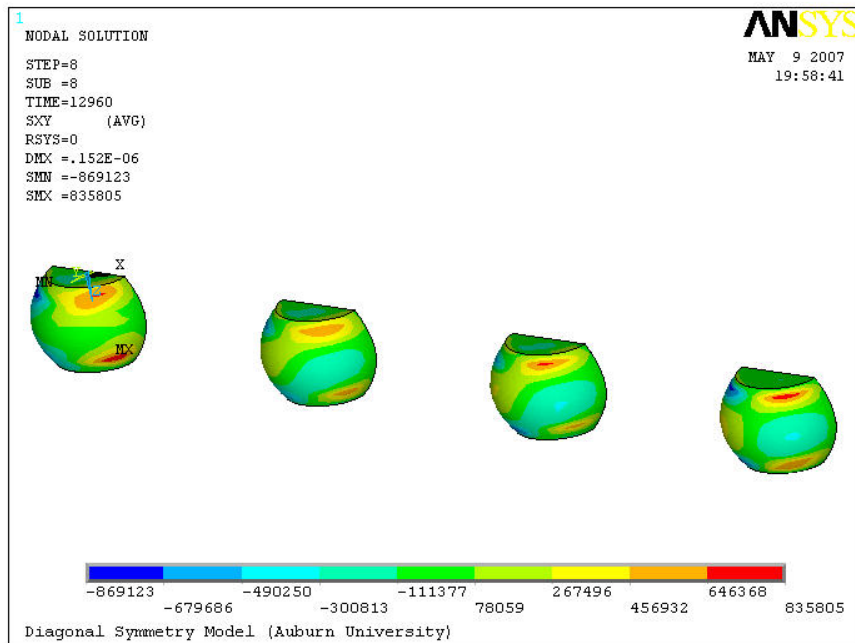


Figure 4.41. XY Shear Stress plot of all SAC305 solder joints subjected to TC3 condition.

condition.

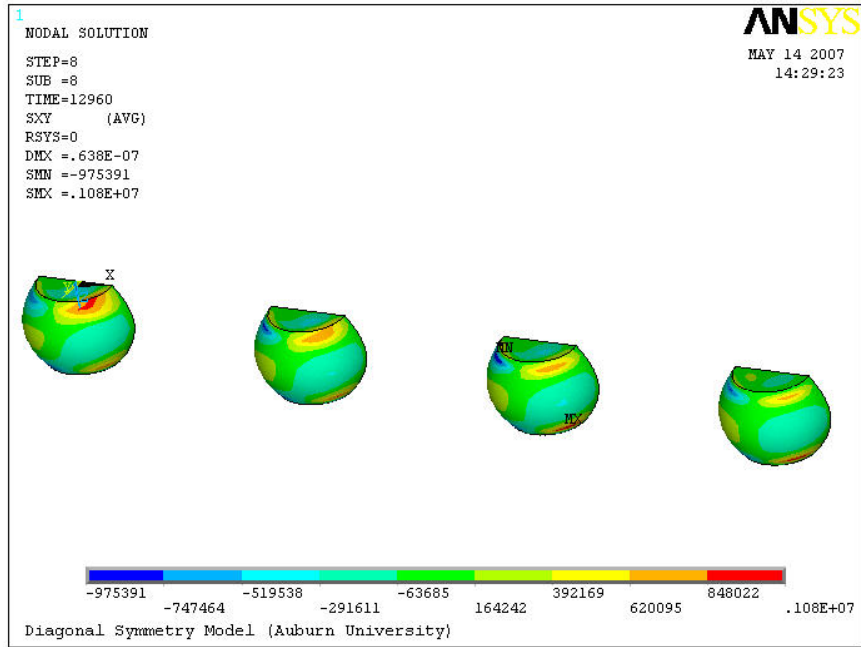


Figure 4.42. XY Shear Stress plot of all SAC305 solder joints subjected to TC4 condition.

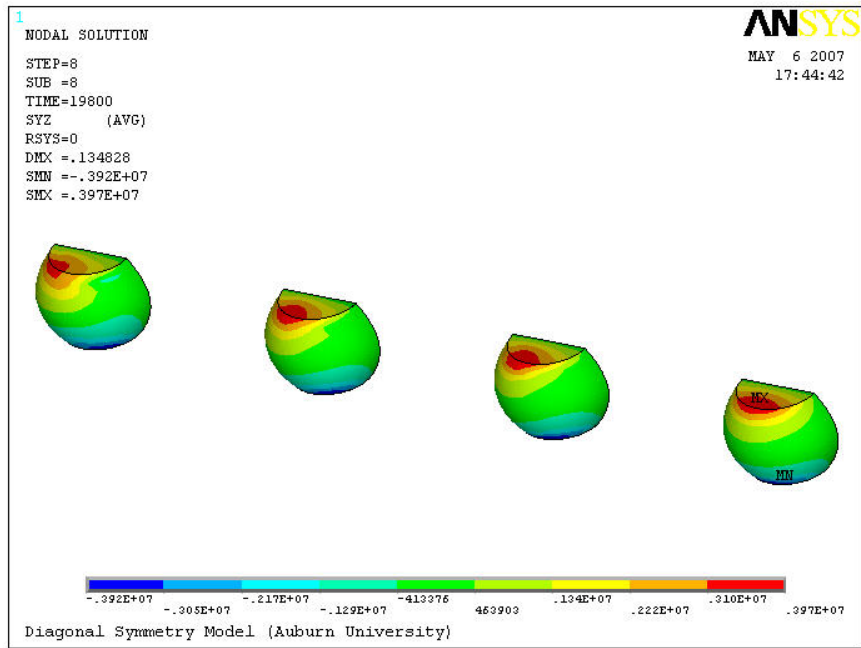


Figure 4.43. YZ Shear Stress plot of all SAC305 solder joints subjected to TC2 condition.

condition.

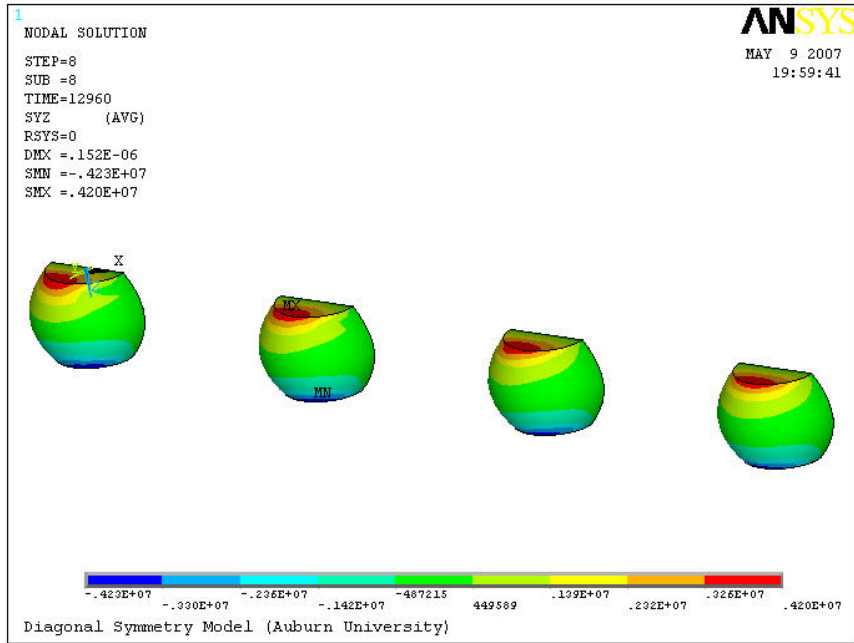


Figure 4.44. YZ Shear Stress plot of all SAC305 solder joints subjected to TC3 condition.

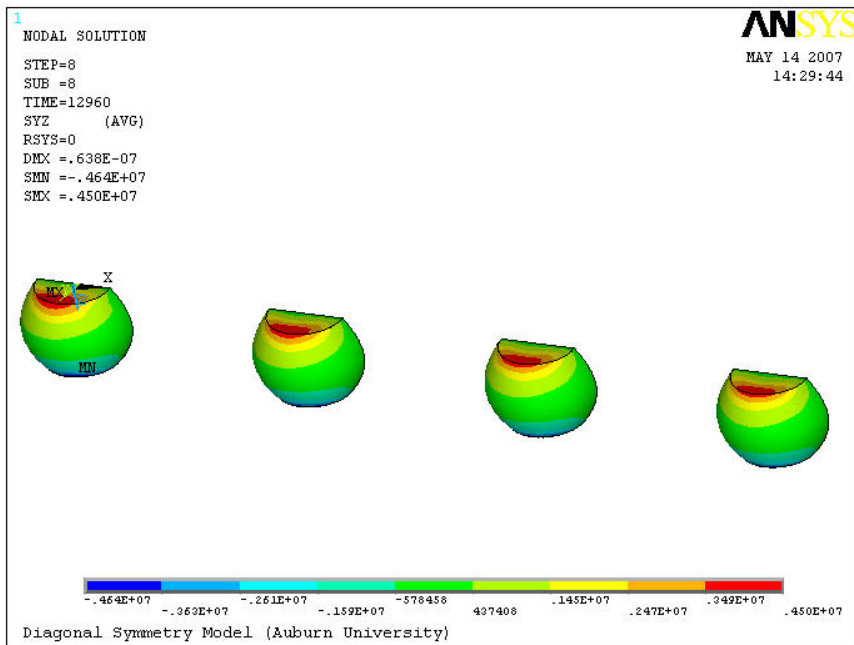


Figure 4.45. YZ Shear Stress plot of all SAC305 solder joints subjected to TC4 condition.

4.6 Time History Post Processing of 49 I/O BGA Model

Time history post processing is a results subset of ANSYS that can be used to plot the desired stress and strain values over cycle time. For purposes of the research presented in this work, stress vs. time, strain vs. time, and hysteresis loops were plotted to show trends in the accumulated damage to the critical solder joint caused by thermal cycling. Figures 4.46 through 4.53 show stress vs. time and strain vs. time plots for the BGA 49 model.

4.6.1 Eutectic Solder

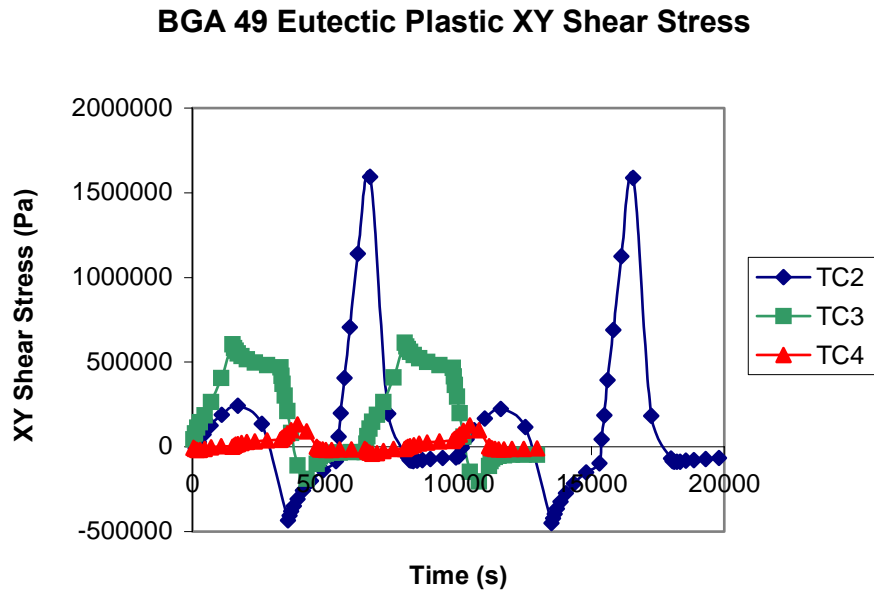


Figure 4.46. XY Stress vs. Time plot for eutectic solder.

BGA 49 Eutectic Plastic YZ Shear Stress

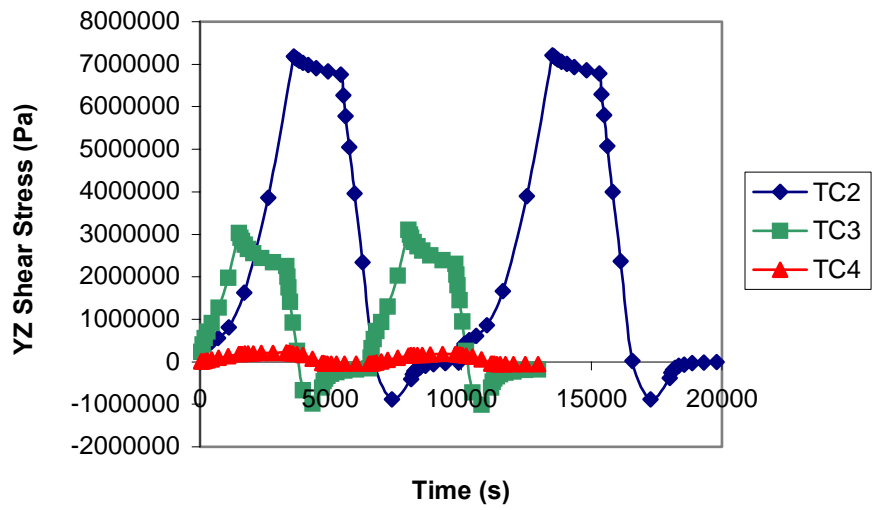


Figure 4.47. YZ Stress vs. Time plot for eutectic solder.

BGA 49 Eutectic Plastic XY Shear Strain

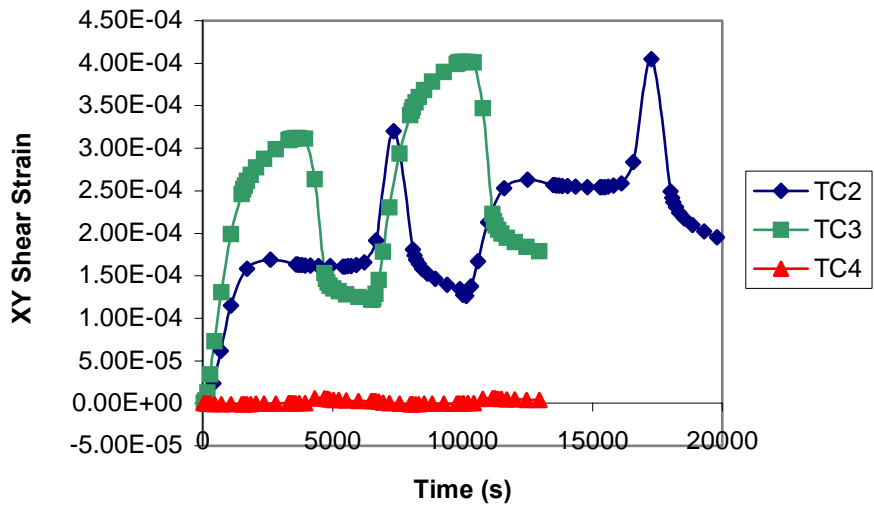


Figure 4.48. XY Strain vs. Time plot for eutectic solder.

BGA 49 Eutectic Plastic YZ Shear Strain

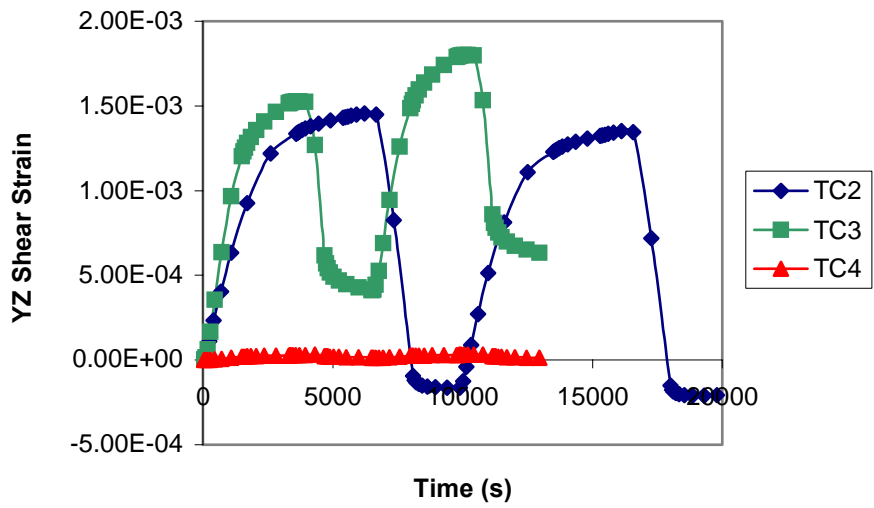


Figure 4.49. YZ Strain vs. Time plot for eutectic solder.

4.6.2 SAC305 Solder

BGA 49 SAC305 Plastic XY Shear Stress

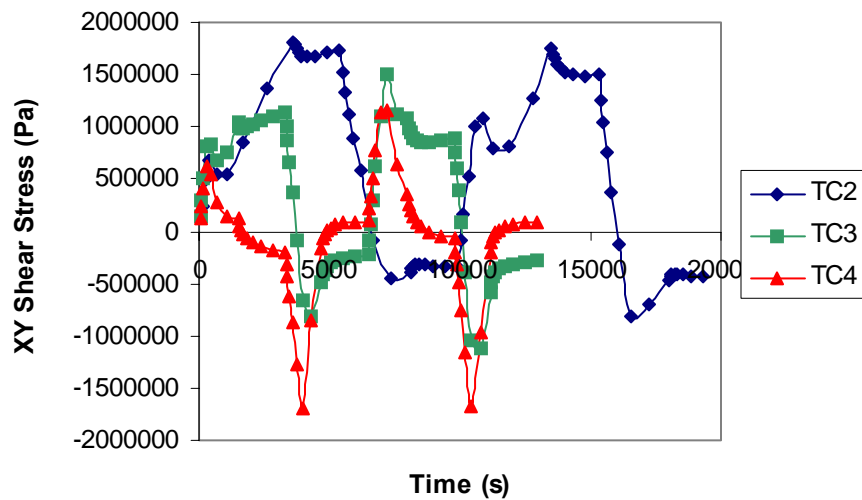


Figure 4.50. XY Stress vs. Time plot for SAC305 solder joint.

BGA 49 SAC305 Plastic YZ Shear Stress

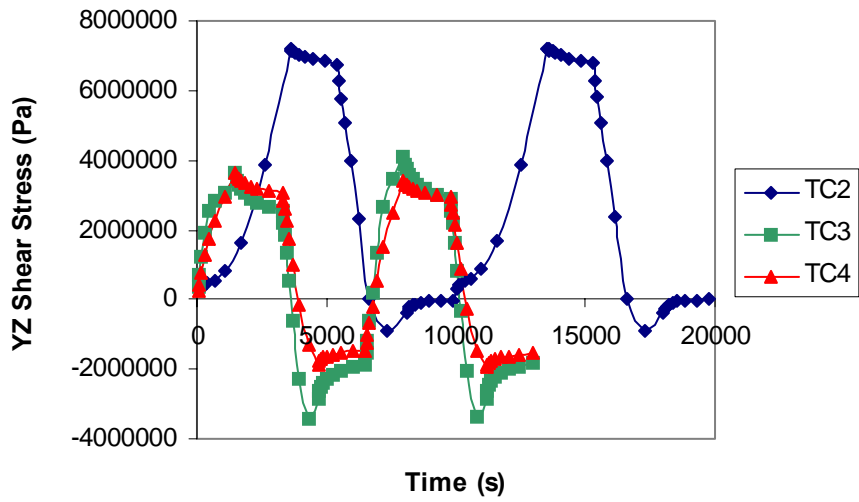


Figure 4.51. YZ Stress vs. Time plot for SAC305 solder joint.

BGA 49 SAC305 Plastic XY Shear Strain

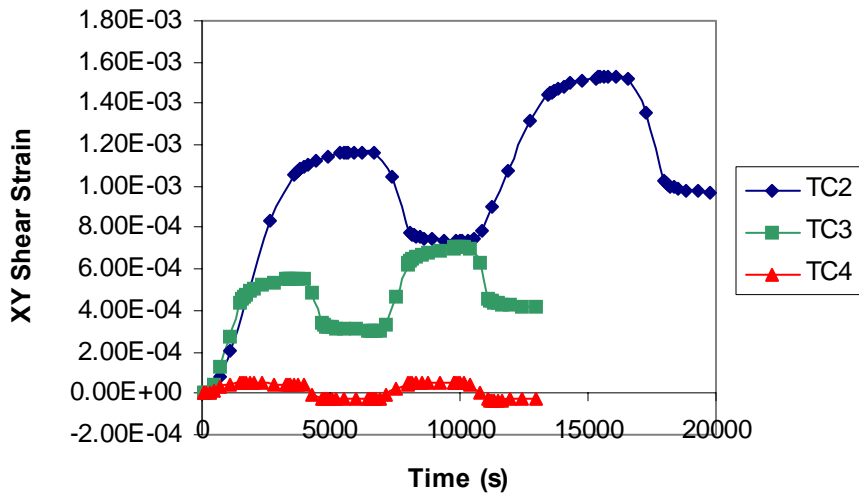


Figure 4.52. XY Strain vs. Time plot for SAC305 solder joint.

BGA 49 SAC305 Plastic YZ Shear Strain

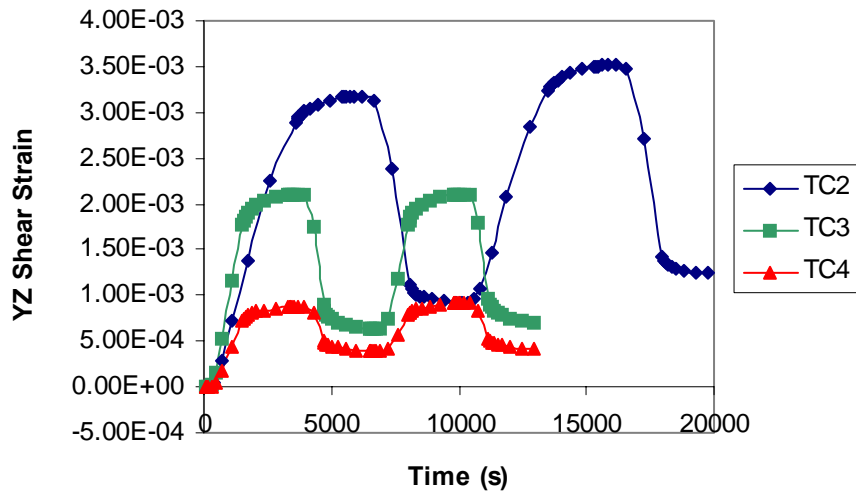


Figure 4.53. YZ Strain vs. Time plot for SAC305 solder joint.

4.7 Plastic Work Calculation

The inelastic strain energy density can be seen visually as a graph of the stress vs. strain over the time that the solder joint was subjected to thermal cycling. This stress vs. strain representation is known as the hysteresis loop. Figures 4.54 through 4.57 show the hysteresis plot results for each model.

4.7.1 Eutectic Solder Results

BGA 49 Eutectic XY Hysteresis Loop

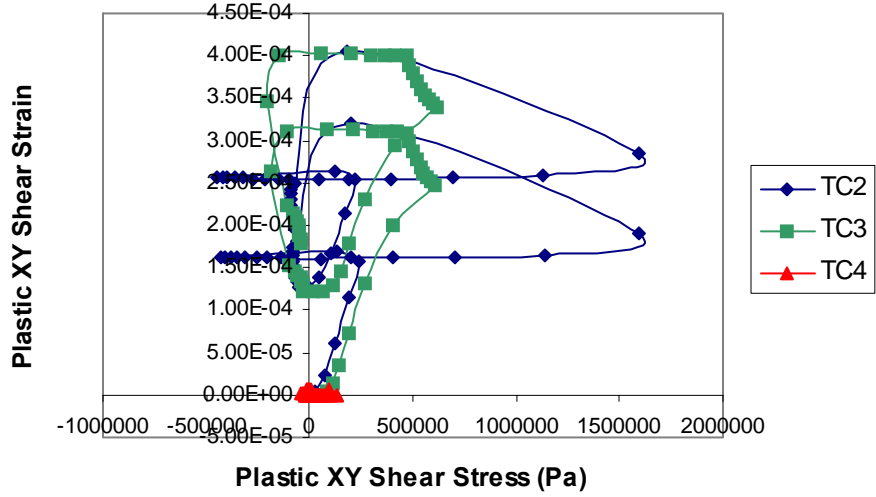


Figure 4.54. XY Hysteresis plot of eutectic solder for TC2, TC3, and TC4 conditions.

BGA 49 Eutectic YZ Hysteresis Loop

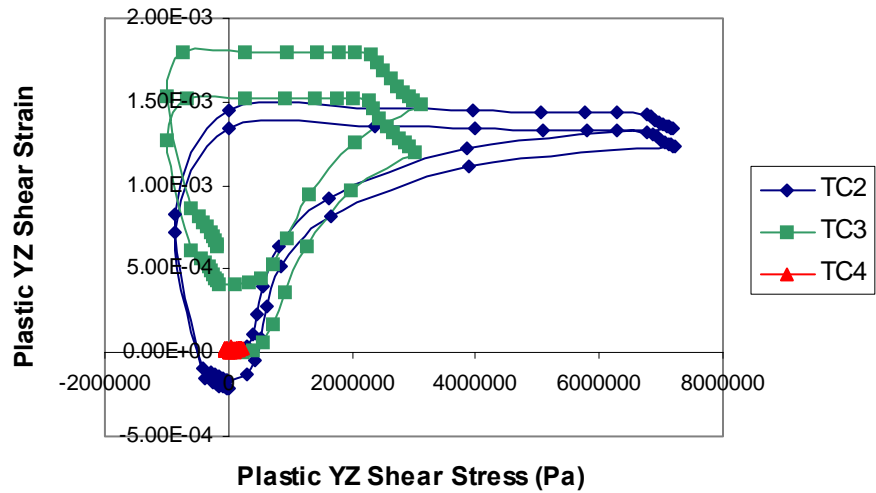


Figure 4.55. YZ Hysteresis plot of eutectic solder for TC2, TC3, and TC4 conditions.

4.7.2 SAC305 Solder Results

BGA 49 SAC305 XY Hysteresis Loop

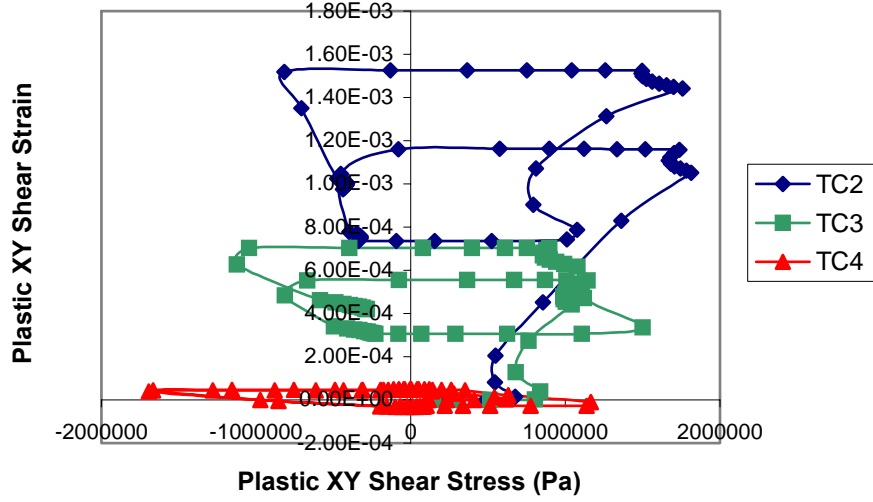


Figure 4.56. XY Hysteresis plot of SAC305 solder for TC2, TC3, and TC4 conditions.

BGA 49 SAC305 YZ Hysteresis Loop

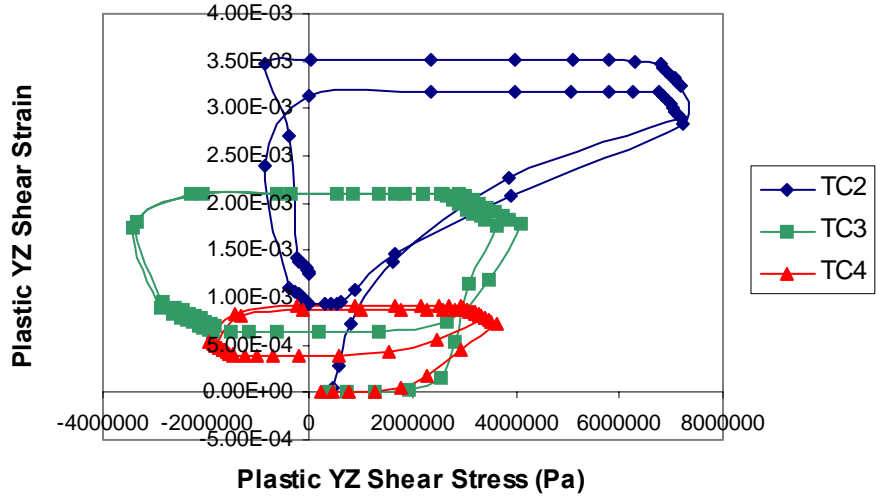


Figure 4.57. YZ Hysteresis plot of SAC305 solder for TC2, TC3, and TC4 conditions.

When the most critical solder joint was determined, the plastic work simulation could be initiated. Because of the highest stress accumulating near the interface layer between the solder joint and the solder pads, the two interference layers were isolated from the remaining body of the critical solder joint in order to determine the accumulated damage averaged over the most critical surface of the solder joint.

$$\Delta W_i(\text{ISED}) = \frac{\left(\sum_{n=1}^{\text{total elements}} \Delta W^{(n)} \times V_n \right)}{\left(\sum_{n=1}^{\text{total elements}} V_n \right)} \quad (4.9)$$

The inelastic strain energy density (ΔW) is calculated from the converged hysteresis loop. The damage relation proposed by Darveaux, et al. [1996], [2000], and Lall, et al. [2003] has been used to calculate the characteristic life (α_{joint}) for life prediction of the component. The characteristic life of the component is given by

$$\alpha_{\text{joint}} = N_0 + \frac{A}{\left(\frac{da}{dN} \right)} \quad (4.10)$$

$$N_0 = K_1 (\Delta W)^{K_2} \quad (4.11)$$

$$\frac{da}{dN} = K_3 (\Delta W)^{K_4} \quad (4.12)$$

Table 4.5. FEA Life Prediction for UBGA49.

	TC2	TC3	TC4
ΔT	180	97	80
Tin-Lead Solder	1162	2194	2414
SAC305 Solder	511	1237	1409

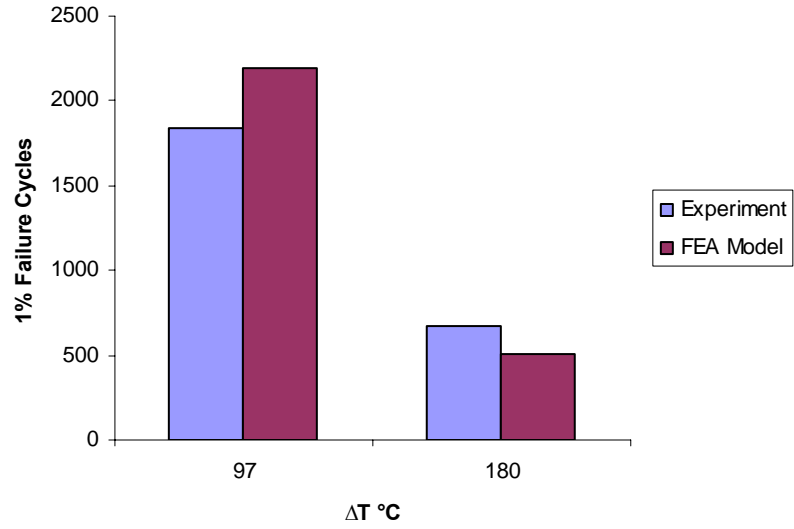


Figure 4.58. Correlation between experimental vs. FE predicted N1% failure cycles.

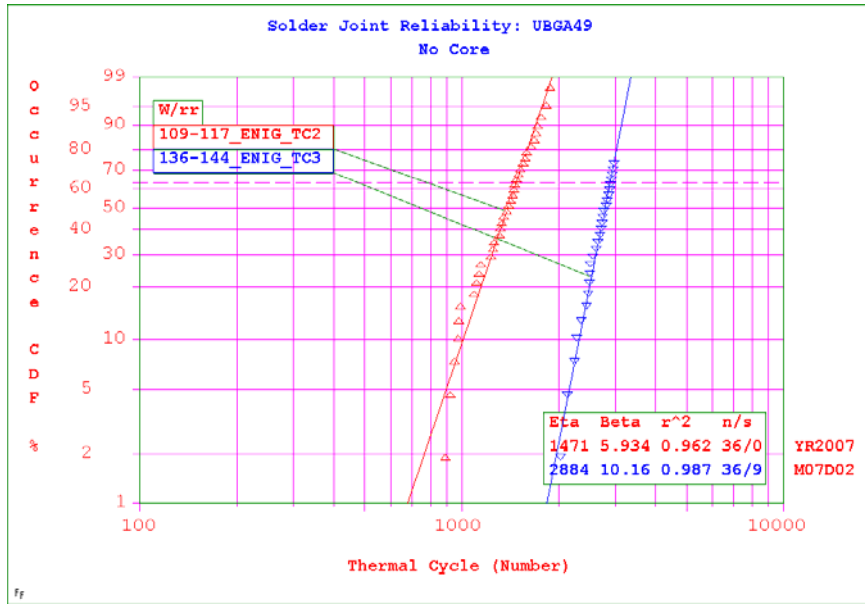


Figure 4.59. Weibull distribution for 49 I/O package.

CHAPTER 5

STATISTICAL MODELING

In this paper, non-copper core PCB boards were used for the accelerated thermal cycling experiment, as well as for the statistical and finite element models. The data in this paper was collected using non-core printed circuit boards. The no-core PCBs are made up of FR-4 printed circuit boards of thickness 2.286mm (.090 in.). All electronic packages tested and modeled in this paper are plastic ball grid array (PBGAs).

5.1 Hybrid Approach

A combination of statistics-based and finite element methodology has been used to identify the critical parameters and their sensitivity on the thermal reliability of the BGA packages. Sensitivities of reliability to design, material, architecture, and environment parameters have been developed from statistics and finite element models and validated versus experimental data. Parameters investigated for thermal reliability of the BGAs include: die size, die to package ratio, solder ball composition, solder ball diameter, ball pitch, pad size, local CTE mismatch between mold compound, global CTE mismatch between component and PCB board, PCB thickness, board finish (HASL and ENIG), PCB material, substrate material and temperature cycle conditions such as ramp rate, dwell time, and temperature extremities.

The relative influence of these parameters on the thermal reliability has been determined by using multivariate regression and analysis of variance techniques. MINITAB has been used for statistical analysis. Statistics-based models have been developed based on experimental data. The scope of the accelerated test database is shown in Table 5.1. A model library has been developed to address common package architectures. Accelerated life-test data in harsh thermal environments, for various formats of ball-grid packages, has been accumulated and used for analysis. Package sizes targeted include 7 mm, 8 mm, 12 mm, 15 mm, 17 mm, 19 mm, 23 mm, 25 mm, 27 mm, and 29 mm PBGAs. Multivariate regression techniques have been used to develop mathematical equations for parameter sensitivities.

Table 5.1. Scope of Accelerated Test Database.

Parameter	PBGA
Package/Body Size	7mm to 29mm
Number of I/O	49 to 900
Die Size	2.9mm to 15.24mm
Ball Diameter	0.32mm to .8026mm
Ball pitch	0.5mm to 1.0mm
PCB Type	No Copper Core FR-4
PCB Thickness	2.286mm
Surface Finish	ENIG
Solder Type	Eutectic and SAC305

5.2 Model Library

Linear, Log-linear, and log-log statistical models were iteratively developed. Accelerated test response data including number of cycles to 1% failure, and characteristic life over four temperature cycle conditions and for major package and PWB level variables was used for the development and validation of the models. These models in their present form, can be used for the reliability prediction and design trade-offs of package thermo-mechanical reliability. Examples include a linear-regression model (Equation 5.1) and log-log model (Equation 5.2).

$$\text{Linear: } t_f = a_0 + \sum_{k=1}^n b_k f_k \quad (5.1)$$

$$\text{Log: } t_f = a_0 \prod_{k=1}^n (f_k)^{b_k} \quad (5.2)$$

The parameter t_f on the left hand side of the equation represents the time-to-1% failure or characteristic life (time to 63.2% failure) of three-parameter Weibull distribution for the package when subjected to accelerated thermo-mechanical stresses. The parameters on the right hand side of the equation are the predictor variables of the various parameters that influence the reliability of the package. The coefficient of each of the parameters is the indicator of the relative influence of that parameter on the characteristic life of the package. A model library has been developed for various

packaging configurations. Parameter dimensions are indicated at the end of the parameter, e.g. $\ln \text{DiagLenMM}$ represents the diagonal die size in “mm”. The prefix “ln” indicates that the logarithm of the data was used in the regression analysis.

5.2.1 Log-Log Model for No Copper Core PCBs

Lead-free solder alloy PBGA packages were analyzed for the no-copper core group. The maximum number of predictor variables (parameters) and data points has been included in the linear model to analyze the effect of each variable on the reliability of the pbga packages. Test packages using SAC305 lead-free solder alloy were analyzed for the no-core statistical models. The statistical model in the form of mathematical equation is given by

$$\begin{aligned} \ln(N_{1\%}) = & A_0 + A_1(\ln \text{DiagLenMM}) + A_2(\ln \text{BallCount}) \\ & + A_3(\ln \text{PkgPadDiaMM}) + A_4(\ln \text{SolderComp}) \\ & + A_5(\ln \text{BallDiaMM}) + A_6(\ln \text{DeltaT}) \end{aligned} \quad (5.3)$$

Where A_0 through A_6 are generalized degree of freedom in the problem definition. The various predictors used in this model are $\ln \text{DiagLenMM}$ (measurement of the diagonal length of the package), $\ln \text{BallCount}$ is the number of I/O, $\ln \text{PkgPdDiaMM}$ (PCB pad diameter), $\ln \text{BallDiaMM}$ (solder ball diameter), and $\ln \text{DeltaT}$ is the change in temperature °C. Model parameters for No Copper Core PBGA package architecture is shown in Table 5.2. The initial linear regression analysis returned sub-standard R-Sq values for the model. Solder Composition shows a lower statistical significance with a p-value of 10.2%, but from failure mechanics theory we know that solder composition has a

significant effect on the package reliability. Since this statistical insignificance may be attributed to the multi-collinearity among the predictor variables in the reliability data, the correlation coefficient matrix of the predictor variables was plotted to check the correlation coefficients for any multi-collinearity.

Table 5.2. Multiple Regression Log-Log Model for PBGAs on No-Core PCBs

Predictors (ln a_0, f_k)	Coeff (b_k)	SE Coeff	t	p-Value
Constant	24.057	2.064	11.66	0.000
lnDiagLenMM	-0.876	0.2744	-3.19	0.002
lnBallCount	-0.6183	0.1504	-4.11	0.000
lnPkgPadDiaMM	6.088	1.01	6.03	0.000
SolderComp	0.2727	0.1642	1.66	0.102
lnBallDiaMM	-1.6781	0.5845	-2.87	0.006
lnDeltaT	-1.4929	0.3095	-4.82	0.000

Since the regression is based on the assumption of normal distribution, the nature of the distribution of the residuals has been verified. Residual plots of the statistical model are shown in Figure 5.1. Plotting the residuals against the normal score of residuals yields a perfectly normal distribution represented by a straight line at 45° on the normal plot of the residuals. The normal plot of residuals for this model indicates a fairly normal distribution of the residuals as it is quite close to a straight line at 45° (Figure 5.2). The histogram plot of residual versus frequency also exhibits a nearly symmetrical bell-shape pattern, which is consistent with a sample from a normal distribution. The I-

chart of individual observations reveals that the residuals for all the observations are within the three sigma limits of (245.6, -245.6) which implies that all the data points in the analysis are fitted within the control limits of three standard deviations. We can see fairly random distribution of the residuals in the residual versus fits plot, which demonstrates the linear relationship between the predictors and the response variable in the model. If the relationship is not linear than the residuals follow some curved pattern distribution. The plot also holds the assumption of constant variance in the data as the residuals do not fan out or show any pattern as we go from the lower fits to the higher fitted values.

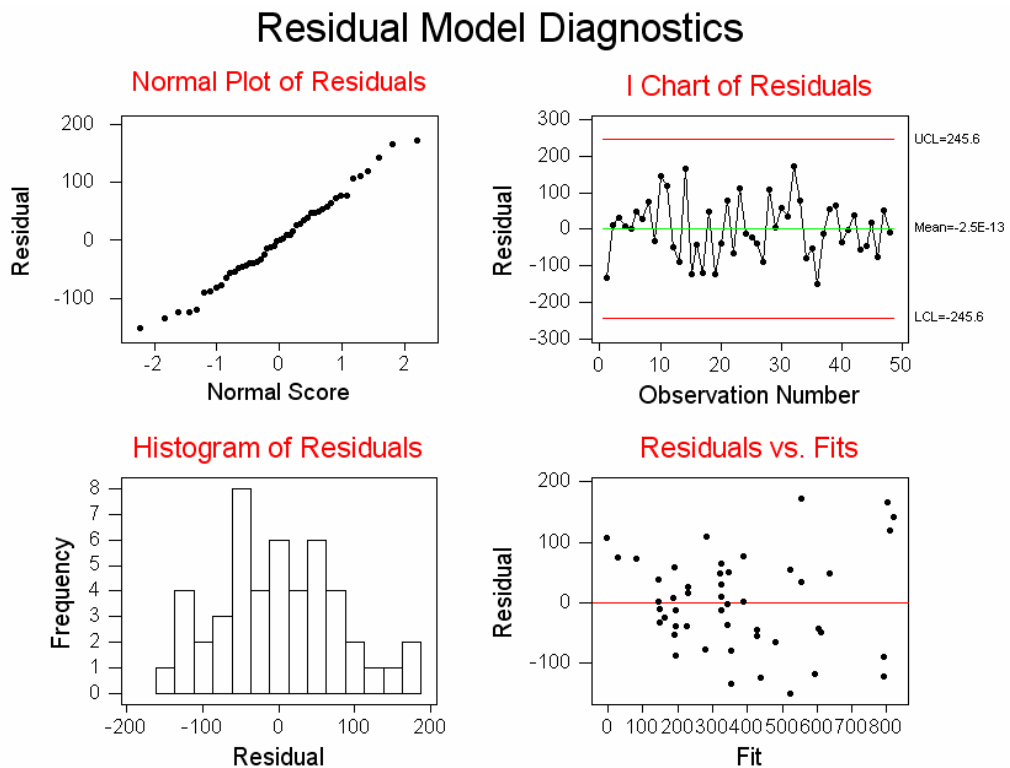


Figure 5.1. Residual plots for the statistical model.

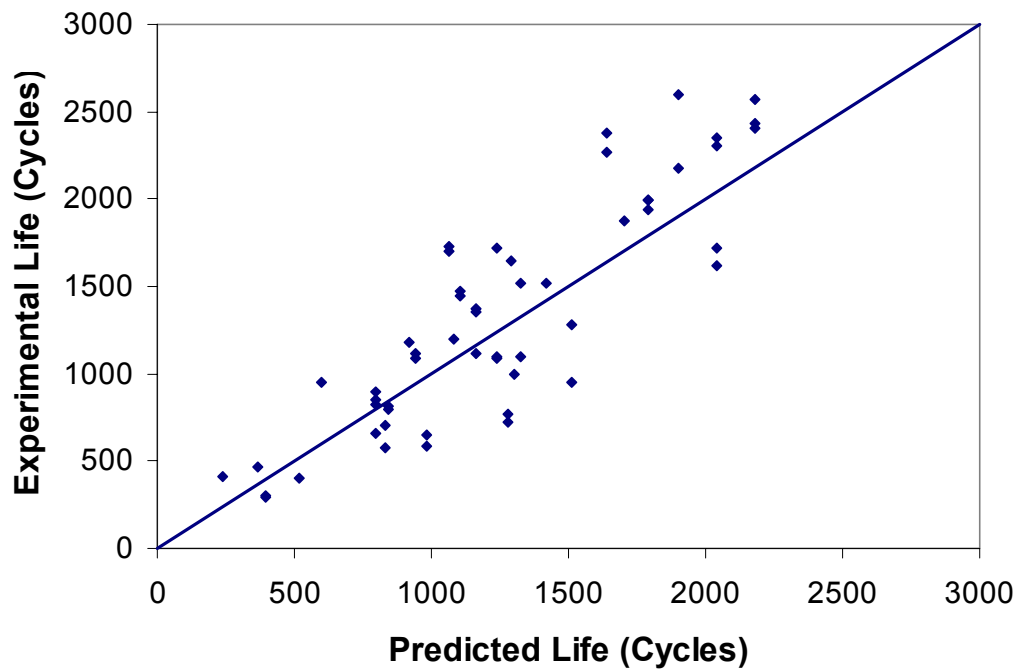


Figure 5.2. Actual versus predicted 1% failure cycles plot for modified linear model.

One-percent failure cycle values predicted by the statistical model have been plotted against the actual values from the experimental database to assess the integrity of fit from the model. The straight line at approximately 45° in Figure 5.2 represents the near-perfect fit of the predicted values. After comparing the various statistical models for the fit of the predicted values with that of actual 1% failure cycles values from the experimental data, the model with the best fit has been finally selected. The plot in Figure 4 for the model shows that the predicted values are consistent with the experimental values within close tolerance.

5.2.2 Log-Linear Model for No Copper Core PCBs

Log-linear models have been developed based on a truncated sub-set of parameters from a global set. The statistical model in the form of mathematical equation is given by

$$\begin{aligned} \ln N_{CharLife} = & A_0 + A_1(\ln \text{DiagLengthMM}) + A_2(\ln \text{DieToBodyRatio}) \\ & + A_3(\ln \text{BallPitchMM}) + A_4(\ln \text{PkgPadDiaMM}) \\ & + A_5(\text{SolderComp}) + A_6(\ln \text{BallDiaMM}) + A_7(\text{TinvK}) \\ & + A_8(\ln \text{DeltaT}) \end{aligned} \quad (5.4)$$

The individual form of the model may differ depending on the parameters selected from the global set for particular package architectures. Certain data points were identified as outliers as a result of high residual absolute values of three standard deviations from the mean, and from large values of Cook's Distance. The general equation for determining Cook's Distance is given by

$$D_i = \frac{(\hat{\beta}_{(i)} - \hat{\beta})' X'X (\hat{\beta}_{(i)} - \hat{\beta})}{pMS_E}, \quad i=1,2,\dots,n \quad (5.5)$$

Where D_i is Cook's Distance, X is an n -by- p matrix of regressors, $\hat{\beta}$ is the least squares estimate, p is the confidence interval, and MS_E is the residual mean square [Montgomery, et.al. 1992].

Log-linear model parameters for No Copper Core PBGA package architecture are presented in Table 5.3. Analysis of the log-linear model results allow for higher R-Sq

values and better explains the variation in the reliability data. The p-values show high statistical significance for all predictor variables. It should be noted that the p-value for $\ln\text{DieToBodyRatio}$ (6.6%) is still greater than the significance level of 5%, which means it is statistically significant at a lower confidence level. SolderComp was assigned a dummy value of 1 for eutectic solder and a value of 2 for SAC305 solder alloy.

Table 5.3. Multivariate Linear Regression Model for PBGAs.

Predictor	Coeff	SE Coeff	T	P
Constant	29.531	1.835	16.09	0.000
$\ln\text{DiagLengthMM}$	-2.567	0.189	16.09	0.000
$\ln\text{DieToBodyRatio}$	-5.897	3.136	-1.88	0.066
$\ln\text{BallPitchMM}$	-1.052	0.480	-2.19	0.034
$\ln\text{PkgPadDiaMM}$	4.135	0.868	4.77	0.000
SolderComp	0.343	0.122	2.81	0.007
$\ln\text{BallDiaMM}$	2.445	0.594	4.12	0.000
T_{invK}	-4.183	1.794	-2.33	0.024
$\ln\Delta T$	-1.431	0.221	-6.48	0.000

$$S = 0.211524 \quad R\text{-Sq} = 87.8\% \quad R\text{-Sq}(\text{adj}) = 85.7\%$$

Since the regression is based on the assumption of normal distribution, the nature of the distribution of the residuals has been verified. Residual plots of the statistical model are shown in Figure 5.3. Plotting the residuals against the normal score of

residuals yields a perfectly normal distribution represented by a straight line at 45° on the normal plot of the residuals. The normal plot of residuals for this model indicates a fairly normal distribution of the residuals as it is quite close to a straight line at 45° (Figure 5.3). The histogram plot of residual versus frequency also exhibits a nearly symmetrical bell-shape pattern, which is consistent with a sample from a normal distribution. The I-chart of individual observations reveals that the residuals for all the data points in the analysis are fitted within the control limits of three standard deviations. We can see fairly random distribution of the residuals in the residual versus fits plot, which demonstrates the linear relationship between the predictors and the response variable in the model. If the relationship is not linear than the residuals follow some curved pattern distribution. The plot also holds the assumption of constant variance in the data as the residuals do not fan out or show any pattern as we go from the lower fits to the higher fitted values.

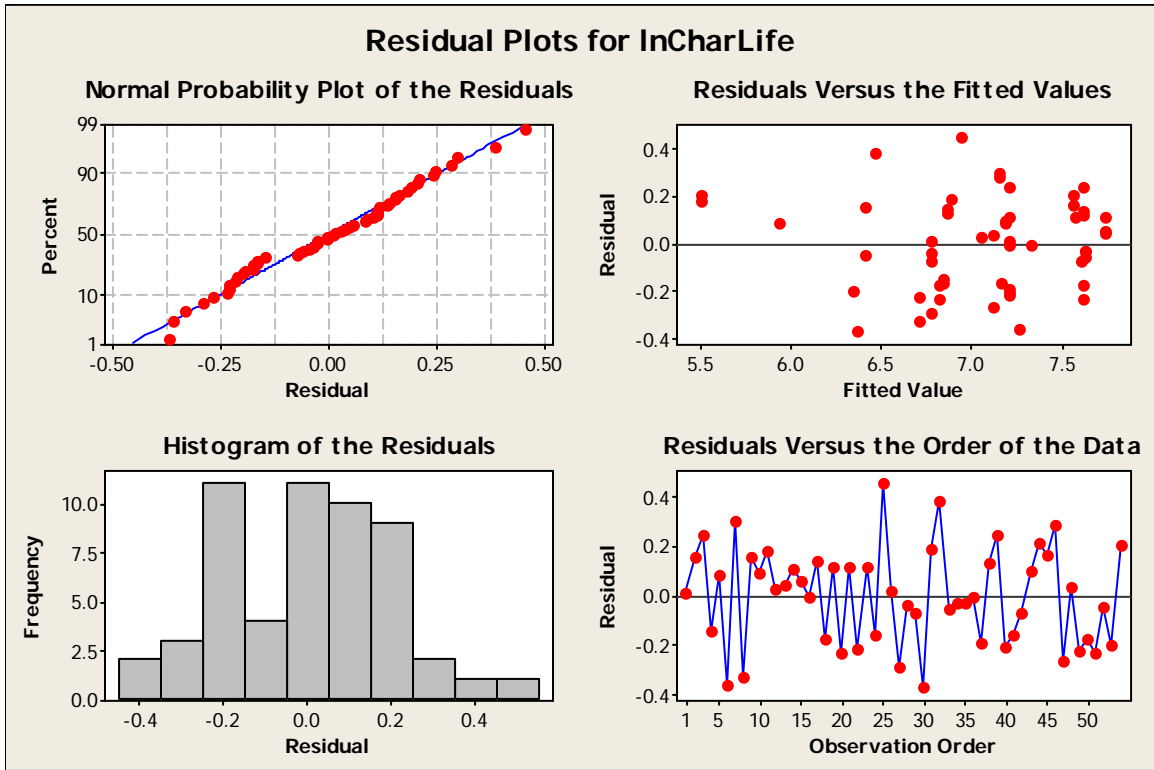


Figure 5.3. Residual plots for the statistical model.

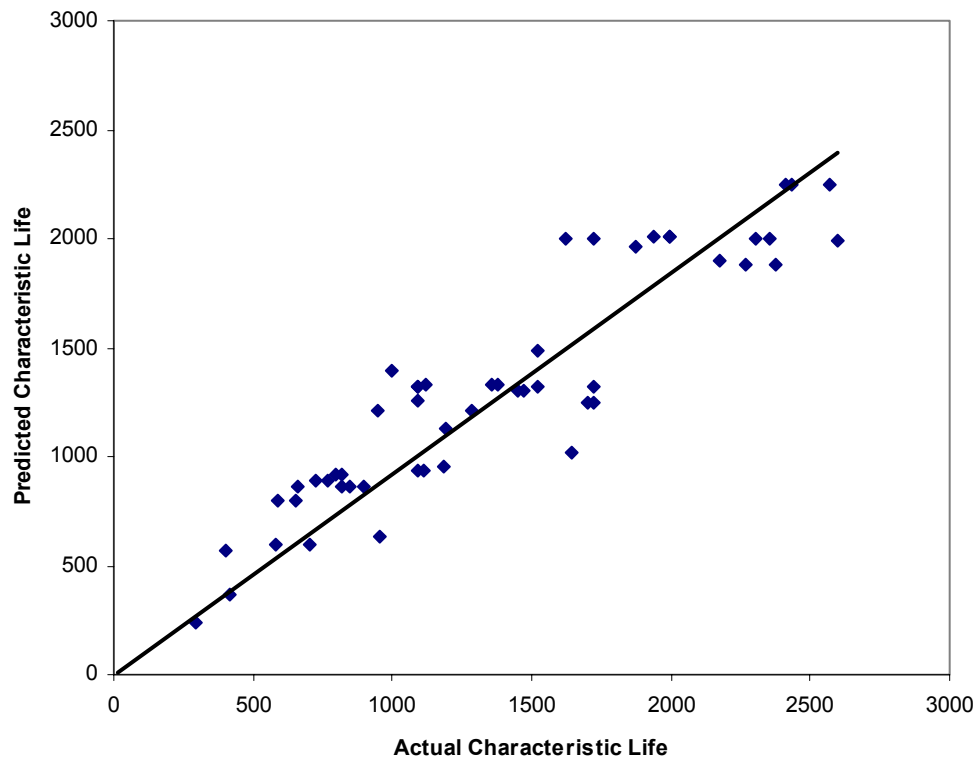


Figure 5.4. Actual versus predicted characteristic life failure cycles plot.

Characteristic life failure cycle values predicted by the statistical model have been plotted against the actual values from the experimental database to assess the integrity of fit from the model. The straight line at approximately 45° in Figure 5.4 represents the near-perfect fit of the predicted values. After comparing the various statistical models for the fit of the predicted values with that of actual characteristic life failure cycles values from the experimental data, the model with the best fit has been finally selected. The plot in Figure 5.4 for the model shows that the predicted values are consistent with the experimental values within close tolerance.

5.2.3 Log-Log Model for No Copper Core PCBs

Log-log models have been developed based on a truncated sub-set of parameters from a global set. The statistical model in the form of mathematical equation is given by

$$\begin{aligned} \ln N_{CharLife} = & A_0 + A_1(\ln DiagLengthMM) + A_2(\ln BallPitchMM) \\ & + A_3(\ln PkgPadDiaMM) + A_4(SolderComp) \\ & + A_5(\ln BallDaiMM) + A_6(\ln DeltaT) \end{aligned} \quad (5.6)$$

Log-log model parameters for No Copper Core PBGA package architecture are presented in Table 5.4. This model illustrates the difference in coefficient values when the inverse of mean temperature variable (T_{invK}) and $\ln DieToBodyRatio$ are removed from the model. The p-values show high statistical significance for all predictor variables.

Table 5.4. Multivariate Linear Regression Model for PBGAs

Predictor	Coeff	SE Coeff	T	P
Constant	24.992	1.808	13.82	0.000
lnDiagLengthMM	-2.174	0.1997	-10.88	0.000
lnBallPitchMM	-1.966	0.5557	-3.54	0.001
lnPkgPadDiaMM	4.001	0.9086	4.40	0.000
SolderComp	0.332	0.1514	2.19	0.033
lnBallDiaMM	2.653	0.7071	3.75	0.000
lnDelta T	-1.562	0.2728	-5.72	0.000

5.3 Model Validation

The effect of the various design parameters on the thermal reliability of the package has been presented. Log-linear regression model validation plots are presented. Statistics and finite element analysis based sensitivity factors quantifying the effect of design, material, architecture, and environment parameters on thermal fatigue reliability, have been used to compute life. The sensitivity factors have been computed by perturbing only the desired parameter or in conjunction with other geometry and material parameters and evaluating its effect on reliability. The predictions from the statistical model have also been compared with the experimental data.

5.3.1 Temperature Cycle Condition

Temperature cycle condition affects BGA packages reliability immensely. The sensitivity of the package thermal reliability to the thermal cycling temperature range has been quantified using the multivariate regression analysis in the statistical model. ΔT is the thermal cycling temperature magnitude. The cycles for characteristic life failure for 180 I/O BGA with Die/Body ratio of 0.5814 predicted by the statistical model have been plotted (Figure 5.5) with the experimental data. Two different temperature cycle conditions used for the comparison are:

1) -40 C to 95 C (TC1).

2) -55 C to 125 C (TC2).

This model prediction validates the thermal sensitivity of the package seen in the experimental data.

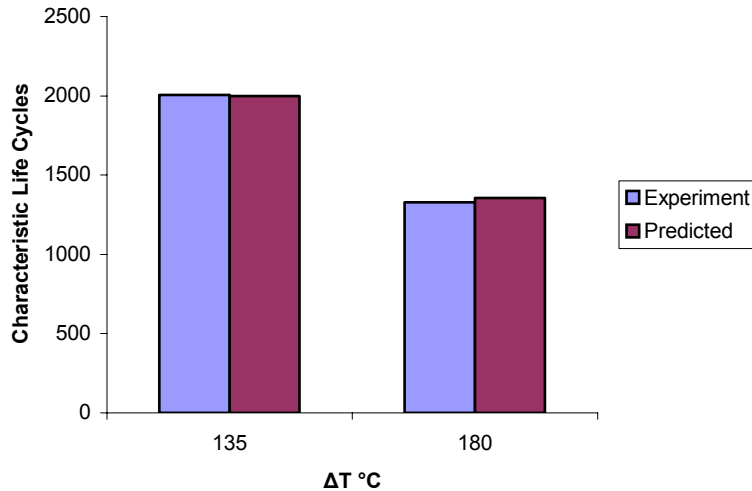


Figure 5.5. Effect of temperature cycling range on 196 I/O BGA coupled with Die Area, Ball Pitch, Ball Diameter, and Die to Body Ratio.

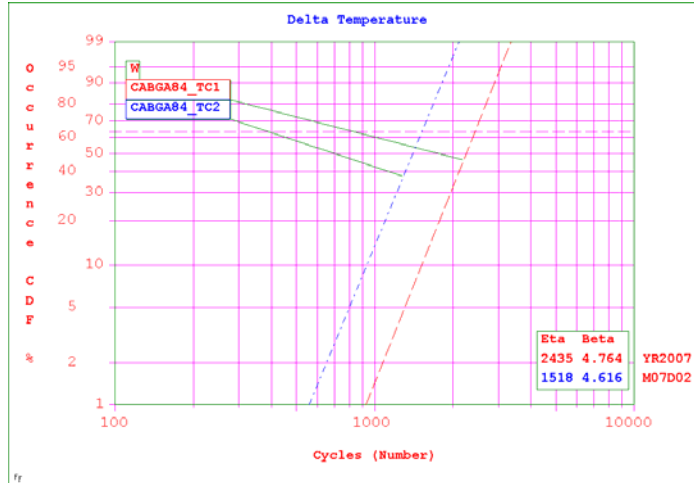


Figure 5.6. Weibull plot of packages used for ΔT graph.

5.3.2 Die to Package Ratio

The reliability of a ball-grid array package generally decreases with the increase in the die-to-package ratio. Experimental data on reliability effect of die-to-body ratio on the solder joint thermal fatigue life of different sizes of BGA packages has been evaluated. Figure 5.7 shows the experimental vs. predicted correlation of the thermal fatigue reliability variance that occurs from various die to package ratios. The packages were all subjected to a thermal cycle of -55°C to 125°C for package die to body ratios of 0.5 mm and 0.7401 mm. The cycles for characteristic life failure from the experimental data and the statistical model have been plotted against the die to body ratio of the various packages. The predicted follow the experimental values quite accurately and show the same trend.

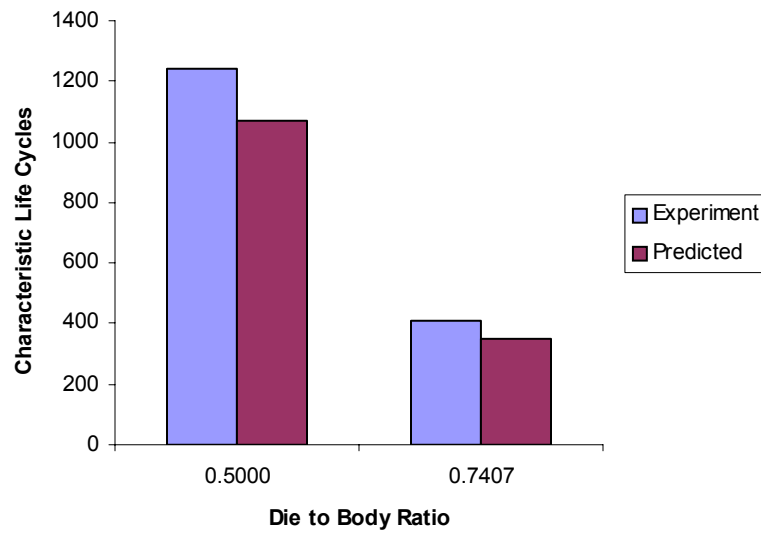


Figure 5.7. Effect of Die to Body Ratio on 196 I/O BGA coupled with Die Area, Ball Pitch, Ball Diameter, and ΔT .

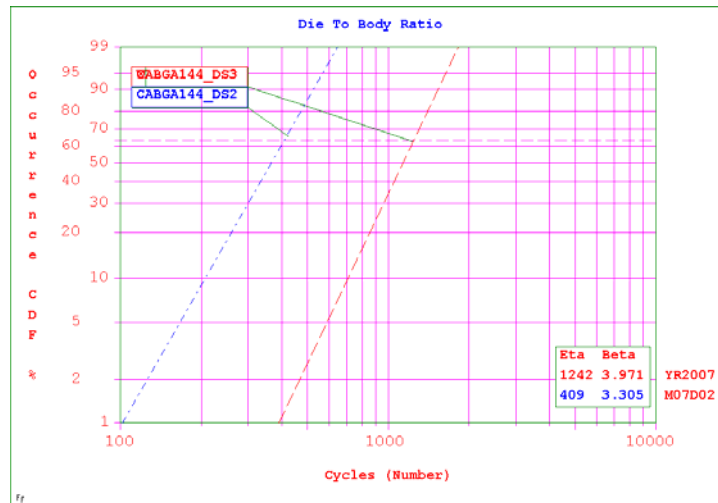


Figure 5.8. Weibull plot of packages used for Die to Body Ratio graph.

5.3.3 Ball Diameter

The solder joint ball diameter has a prominent effect on the thermal reliability of the PBGA packages. Experimental thermal reliability data has been compared with the

statistical model predictions. BGA packages evaluated include solder ball diameter of 0.541 mm, 0.50 mm, and 0.48 mm. Experimental data indicates that the increase in the ball diameter leads to improved thermal reliability of the package, which is shown in Figure 5.9. This trend is in compliance with the theory of failure mechanics as the increase in the solder ball diameter increases the crack area resulting in higher thermal fatigue life.

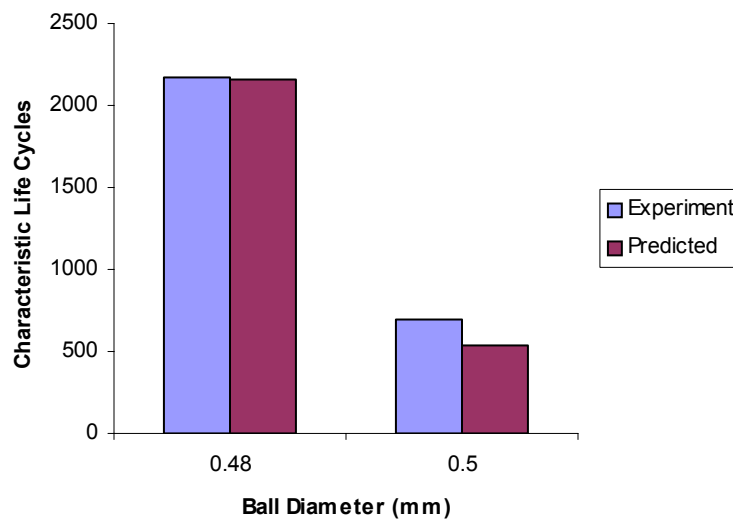


Figure 5.9. Effect of Ball Diameter on 100 I/O BGA coupled with Package Pad Area, Ball Pitch, and ΔT .

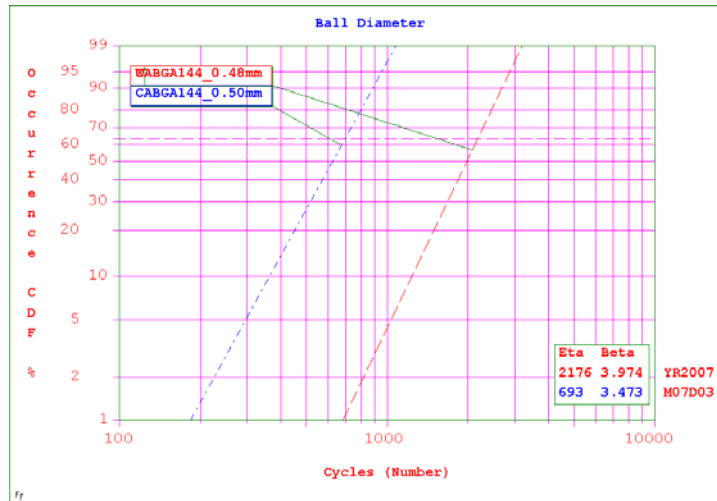


Figure 5.10. Weibull plot of packages used for Ball Diameter graph.

5.3.4 Model Validation

Correlation of experimental, finite element, and statistical models is shown in Figure 5.11 for a 7mm PBGA package. Model convergence was shown using the parametric variable of temperature range. Comparison of experimental data with that of predicted values for 1% failure cycles from both statistics and failure mechanics model shows good agreement, and follows the same trend pattern of decreasing package reliability when temperature range increases.

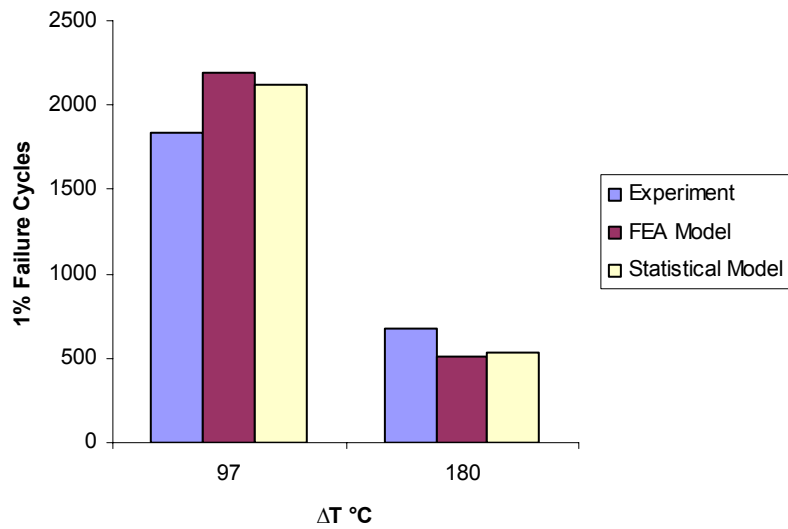


Figure 5.11. Effect of ΔT on thermal reliability of 7 mm PBGA package.

Table 5.5. FEA N1% Life Prediction.

I/O Count	BT Pad Dia (mm)	ΔW (Mpa)	BT Thick (mm)	CDF	N(i) Cycles	da/dN	N(o) Cycles	N1% Fail
49	0.355	0.1069	0.65	0.01	553	0.0002	1342	2195
49	0.355	0.3498	0.65	0.01	79	0.0006	350	511

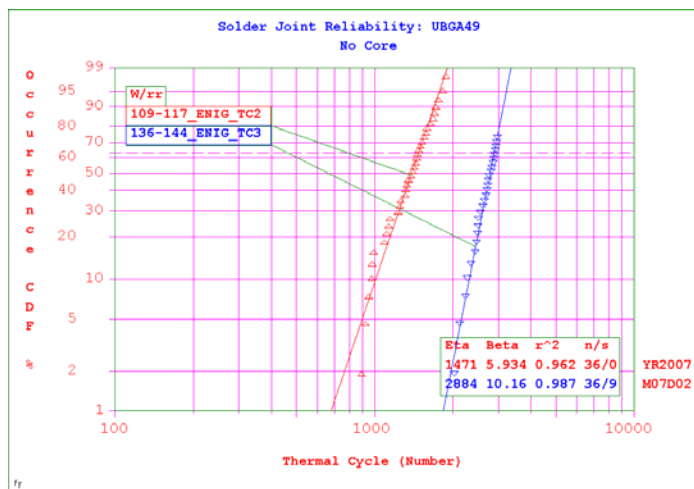


Figure 5.12. Weibull plot of packages used for correlation graph.

Life prediction cycle counts have been predicted for several packages. A list of actual package failures compared to statistical model life prediction is displayed in Table 5.5.

Table 5.6. Predicted vs. Actual N1% Failure Data.

Package Type	Predicted CharLife	Experiment CharLife
PBGA_196_A_DS1	1329.71	1376
PBGA_196_A_DS3	921.50	815.4
PBGA_196_A_DS3	1298.54	1449
PBGA672_Altera	370.06	415.1
PBGA728	1129.72	1194
CABGA -84_A_DS1	2245.45	2408
CABGA -84_A_DS1	2245.45	2572
CABGA -84_A_DS1	2245.45	2435
CABGA -84_A_DS1	1488.11	1518
CABGA -84_A_DS2	1996.46	1720
CABGA -84_A_DS2	1996.46	2307
CABGA -84_A_DS2	1323.10	1518
CABGA -144_A_DS1	1901.89	2176
CABGA -160_A_DS1	858.14	896
CABGA -160_A_DS1	858.14	849
CABGA -160_A_DS1	858.14	819
PBGA_196_A_DS1	2006.43	1940
PBGA_196_A_DS1	2006.43	1995
PBGA_196_A_DS1	2006.43	1998
PBGA_196_A_DS1	1329.71	1356
PBGA_196_A_DS3	921.50	800
PBGA_196_A_DS3	1959.40	1874
PBGA_196_A_DS3	1298.54	1471
PBGA256_A_DS3	1208.65	1285
PBGA324_A_DS2	592.72	580

CHAPTER 6

SUMMARY AND CONCLUSIONS

In this work, risk-management and decision-support models for reliability prediction of BGA packages in harsh environments have been presented. Plastic ball Grid Array packages on non-copper core PCB boards were used for the accelerated thermal cycling experiment, as well as for the statistical and finite element models. The models developed in this effort provide decision support tools for packages subjected to harsh environment conditions. Models described in this work are able to be used with confidence in forecasting the useful life of PBGA packages, and in determining reliability tradeoffs between geometry and materials.

FEA models were tested to measure the effect that dwell time had on damage accumulation within the solder joint. Plotting of the hysteresis loops demonstrated a non-significant change in the amount of damage accumulation between 20 and 30 minute dwell times. Finite element analysis was also used for life prediction in examining the amount of damage caused by thermal cycling fatigue, and the relative resistance to that fatigue damage for the two solder alloys tested. A life prediction method has been developed by calculating the accumulated strain energy density of the solder joint as an indicator of solder joint reliability under harsh conditions.

Statistical models have also been developed in this work, providing a means of package selection reliability that can be parametrically adjusted to meet a variety of environmental, geometrical, and material selection conditions. Convergence between the experimental and statistical model results validates the application of these models to compare the reliability of the different package configurations with different parametric variations.

Convergence of model predictions from statistics and finite element modeling has been investigated. Figure 5.11 shows the effect of temperature range on package reliability of 7 mm PBGA package. Comparison of experimental data with that of predicted values for 1% failure cycles from both statistics and failure mechanics model shows good agreement. All three values for both temperature ranges show a same trend of decreased thermal reliability with the increase in temperature range. The correlation is especially important, if one considers the vastly different approaches used in arriving at predicted life.

It can be suggested that due to the large scope of this overall project, additional research could be done on the many other package architectures that were studied, but omitted from this thesis. Furthermore, this specific research study on PBGA packages could be carried to full conclusion given a long enough timeline to where all packages fail, thus improving model accuracy even further.

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APPENDIX A

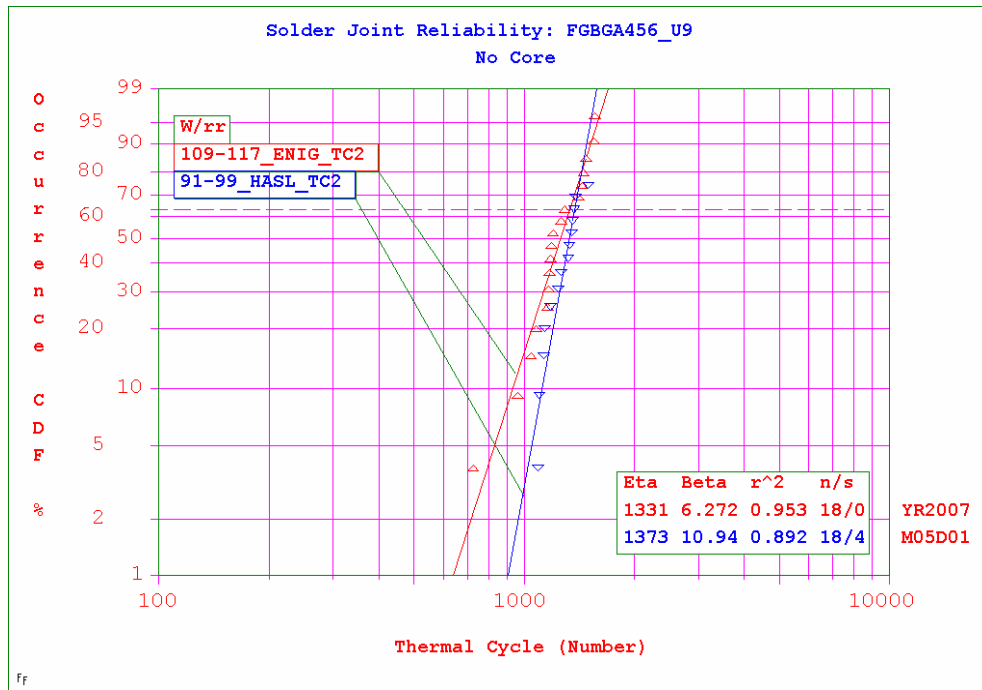


Figure A.1. Weibull plot results for FGBGA456.

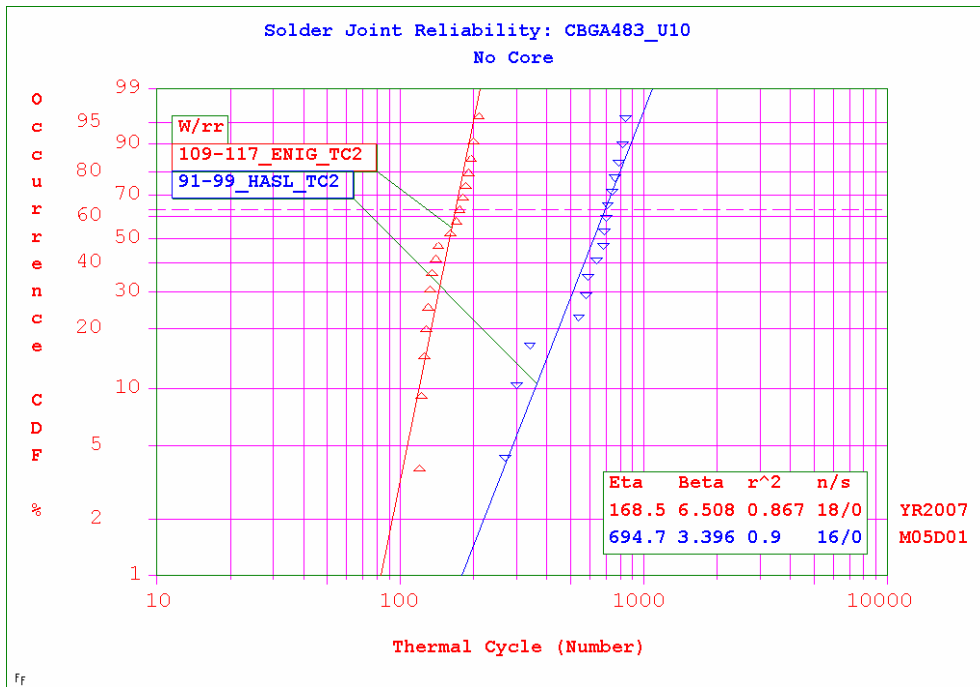


Figure A.2. Weibull plot results for CBGA483.

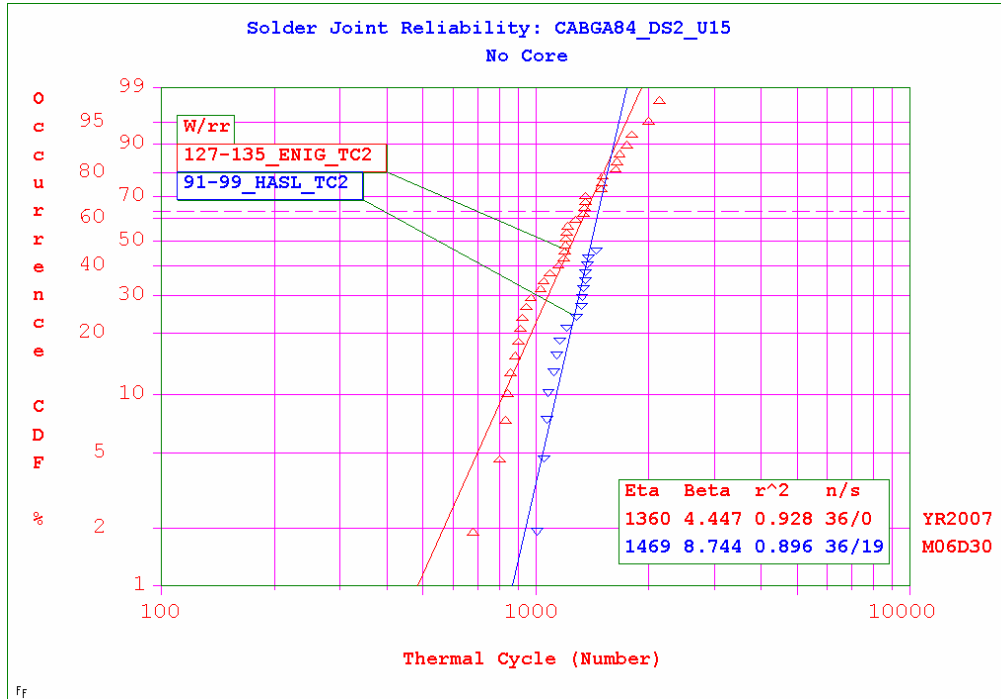


Figure A.3. Weibull plot results for CAGA84.

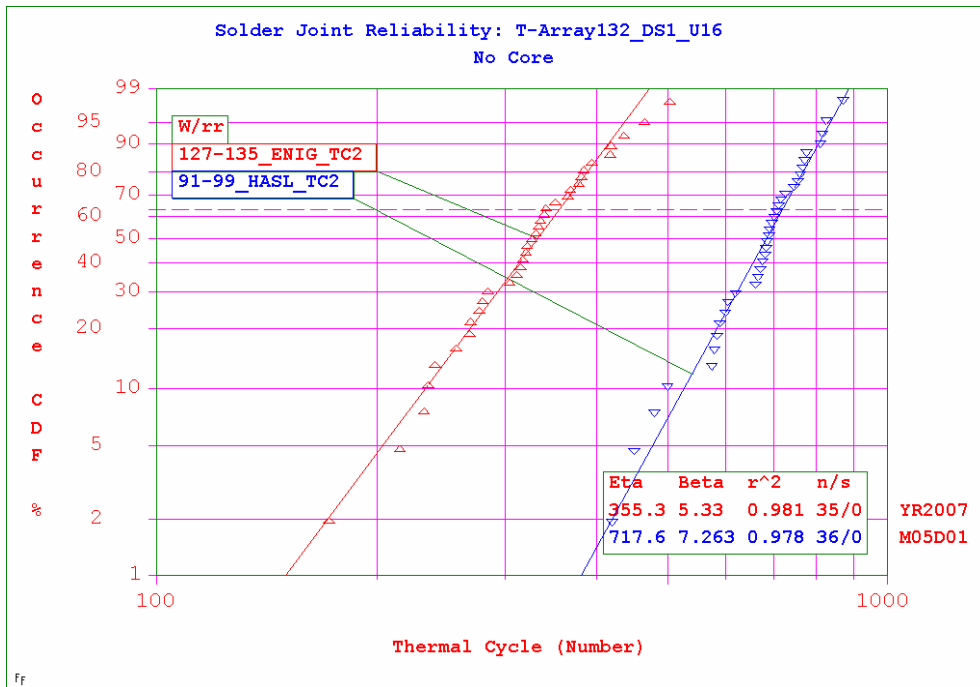


Figure A.4. Weibull plot results for T-Array132_DS1.

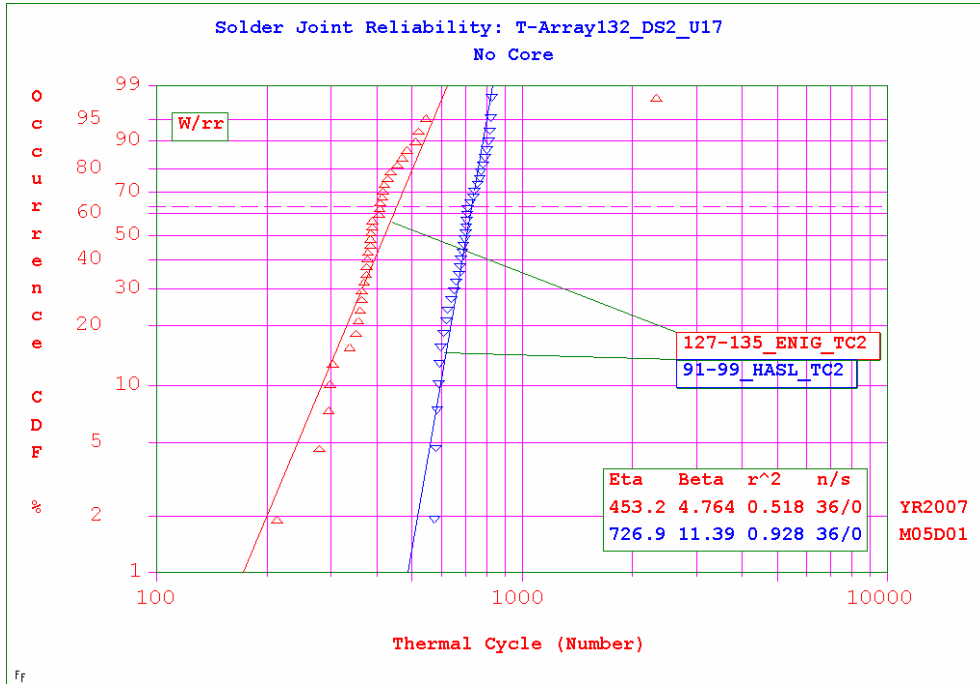


Figure A.5. Weibull plot results for T-Array132_DS2.

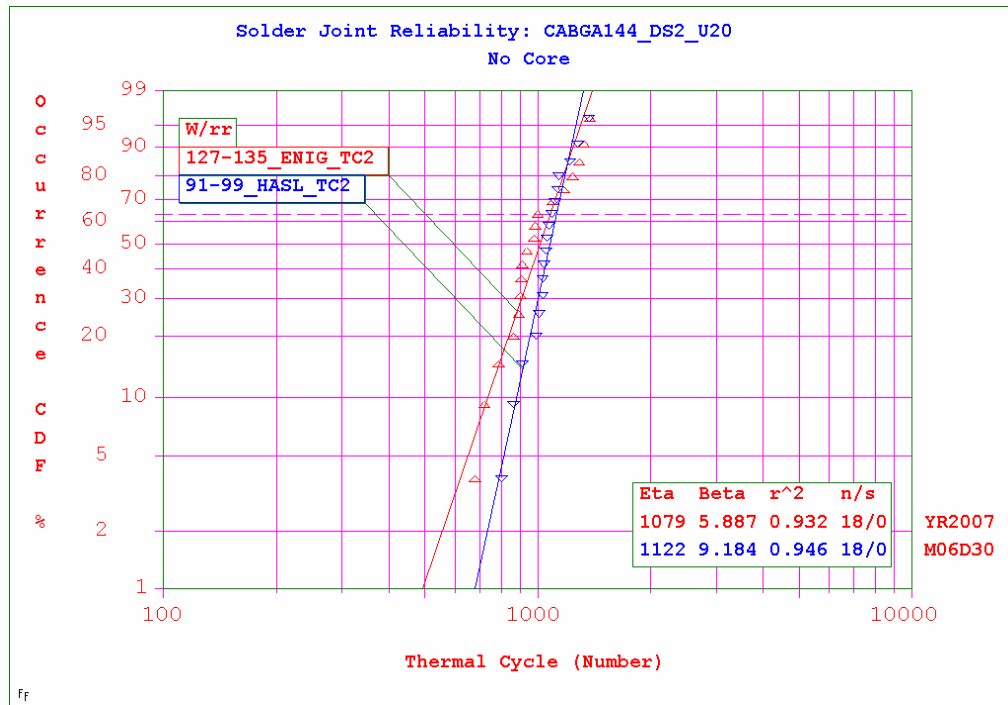


Figure A.6. Weibull plot results for CABGA144_DS2.

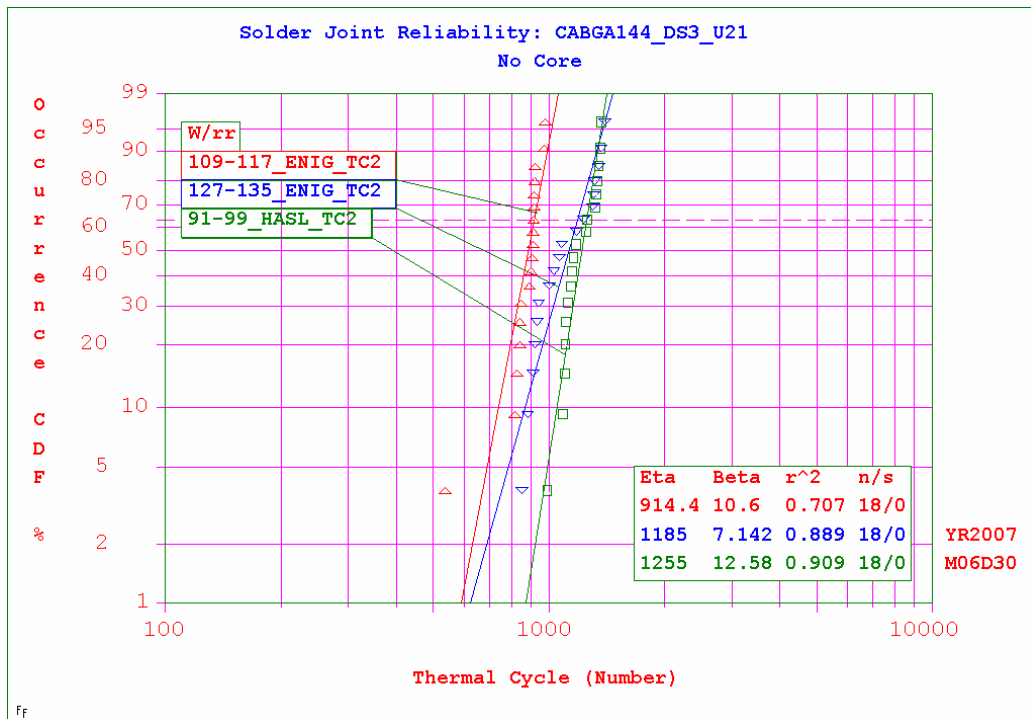


Figure A.7. Weibull plot results for CABGA144_DS3.

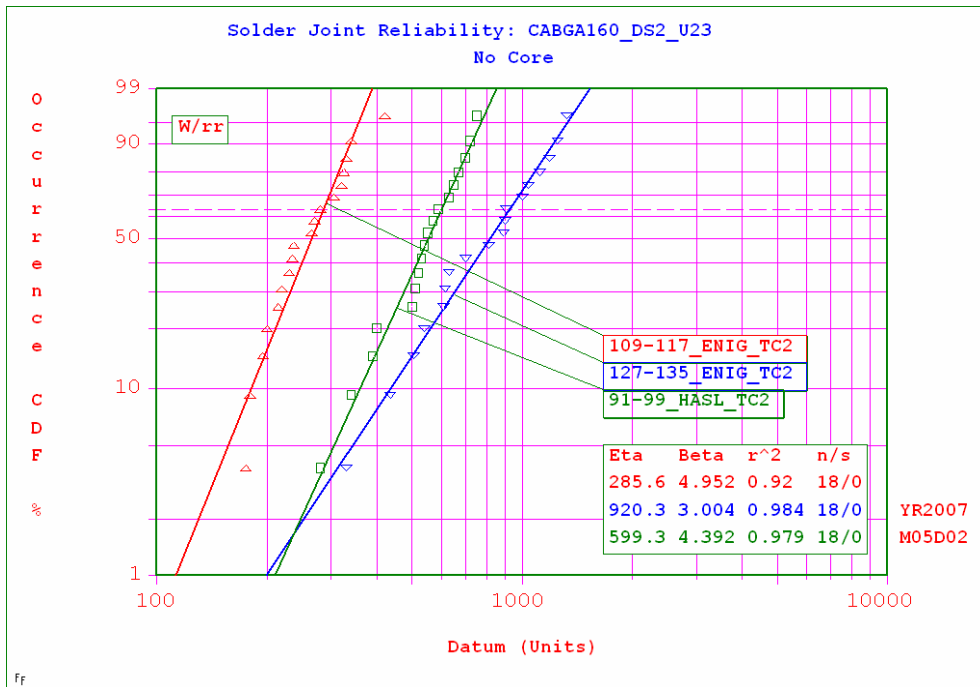


Figure A.8. Weibull plot results for CABGA160.

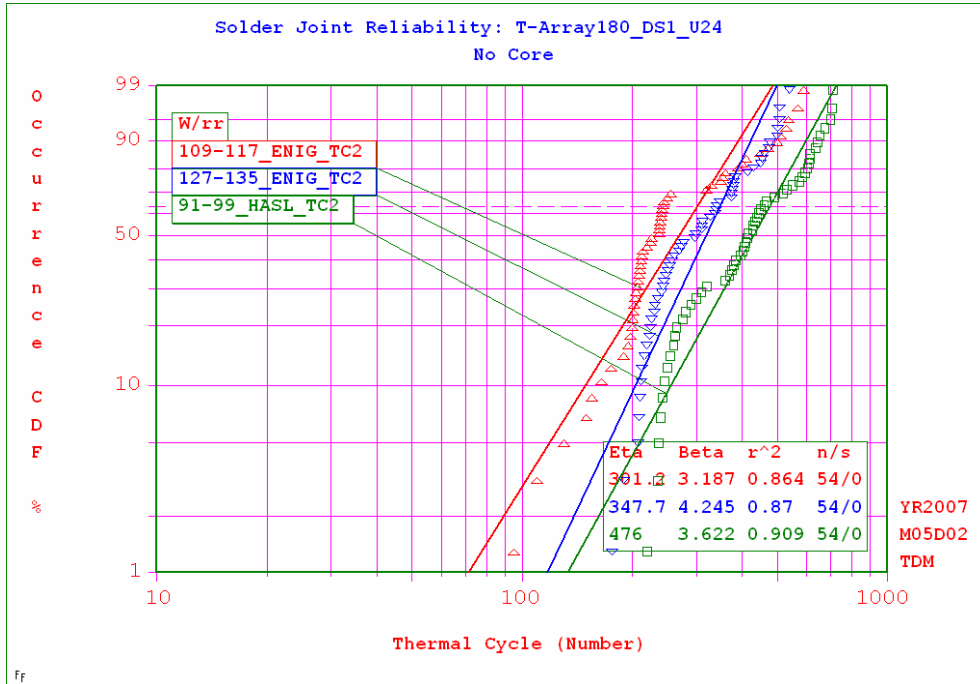


Figure A.9. Weibull plot results for T-Array180_DS1.

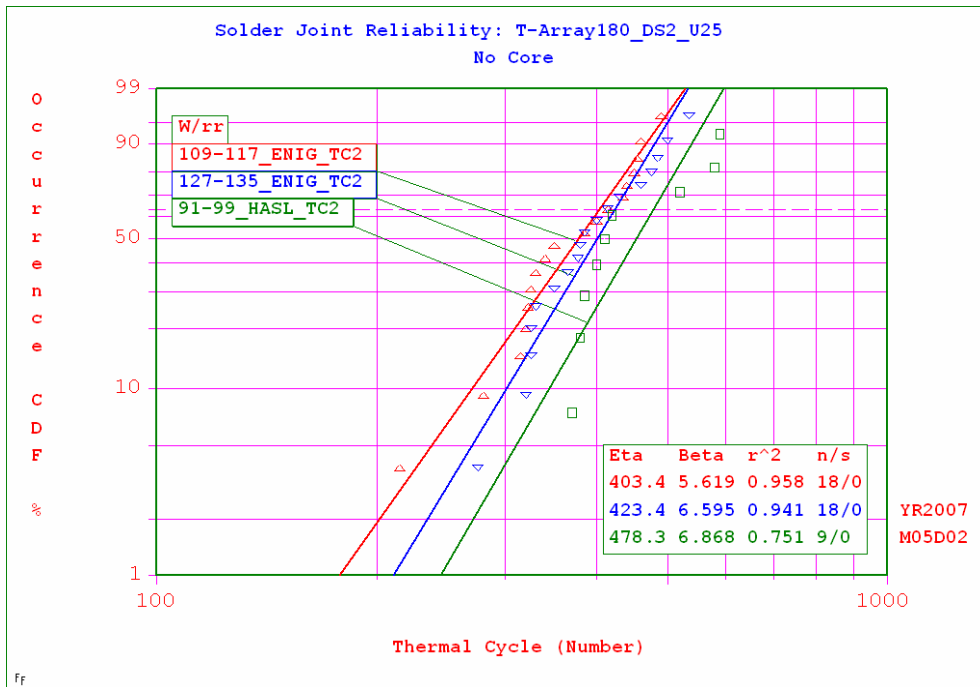


Figure A.10. Weibull plot results for T-Array180_DS2.

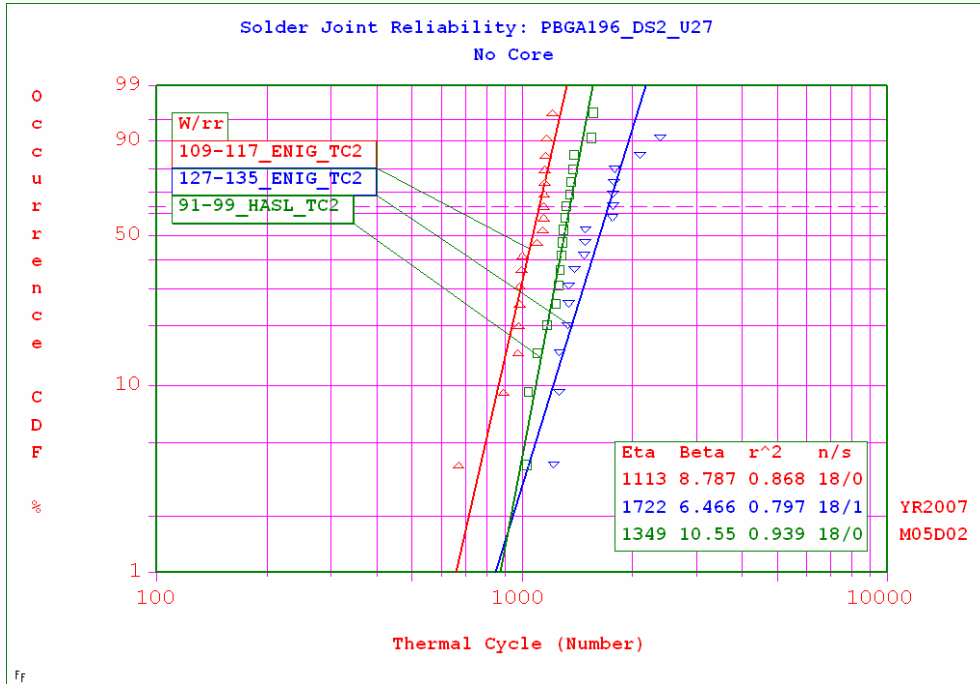


Figure A.11. Weibull plot results for PBGA196_DS2.

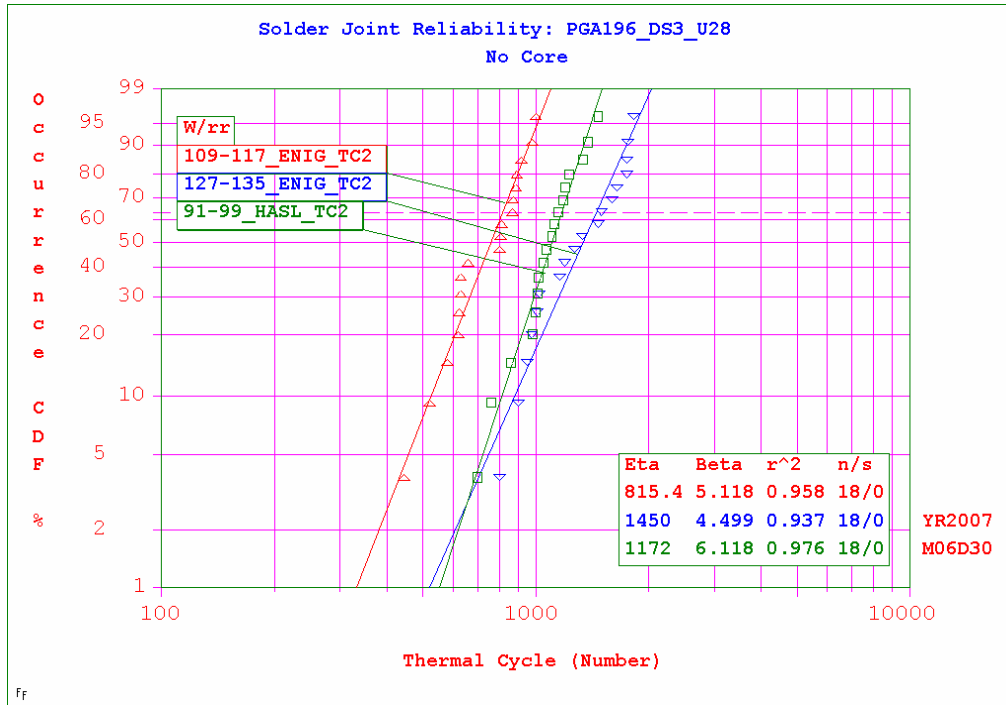


Figure A.12. Weibull plot results for PBGA196_DS3.

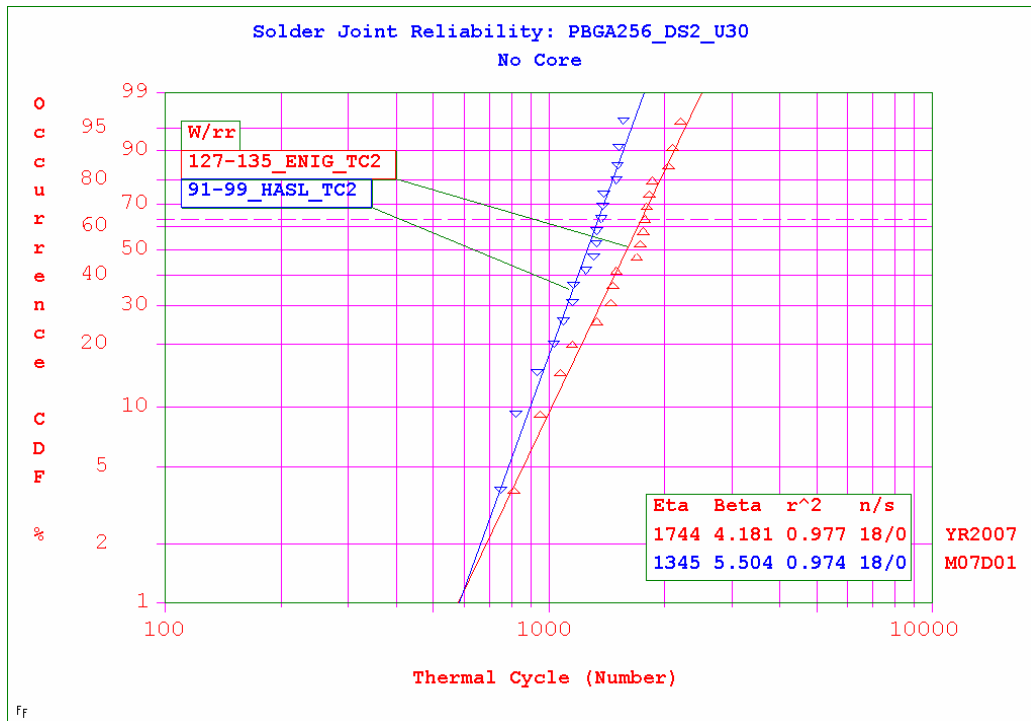


Figure A.13. Weibull plot results for PBGA256_DS2.

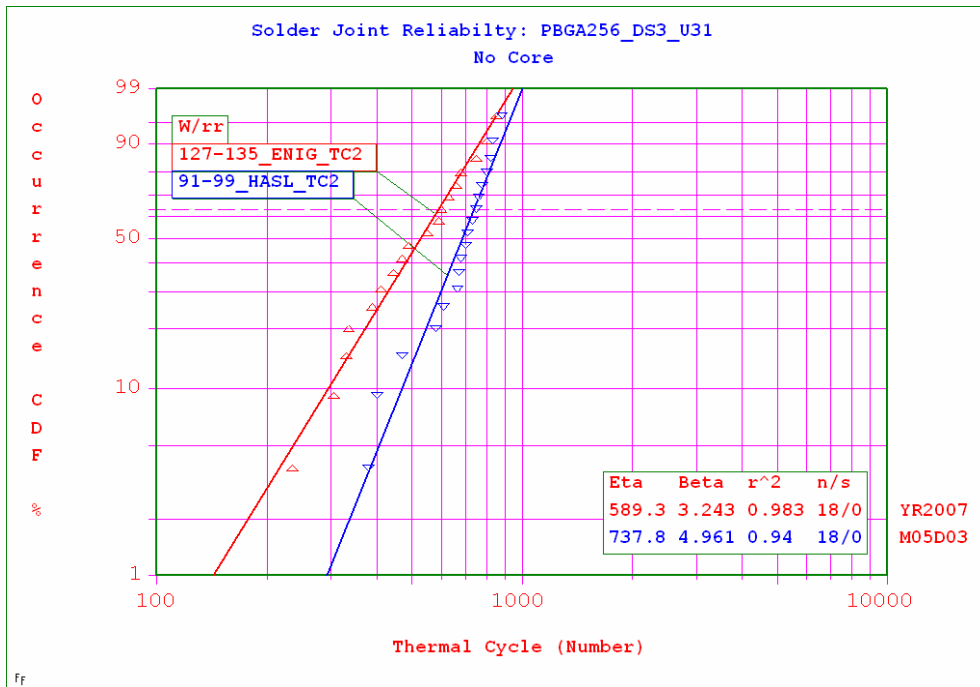


Figure A.14. Weibull plot results for PBGA256_DS3.

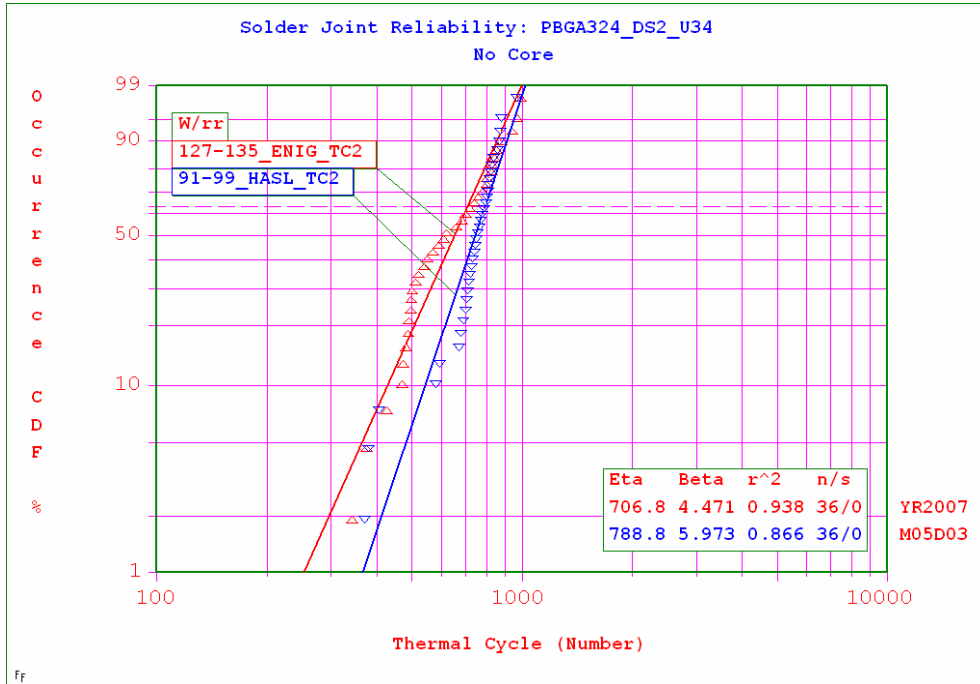


Figure A.15. Weibull plot results for PBGA324.

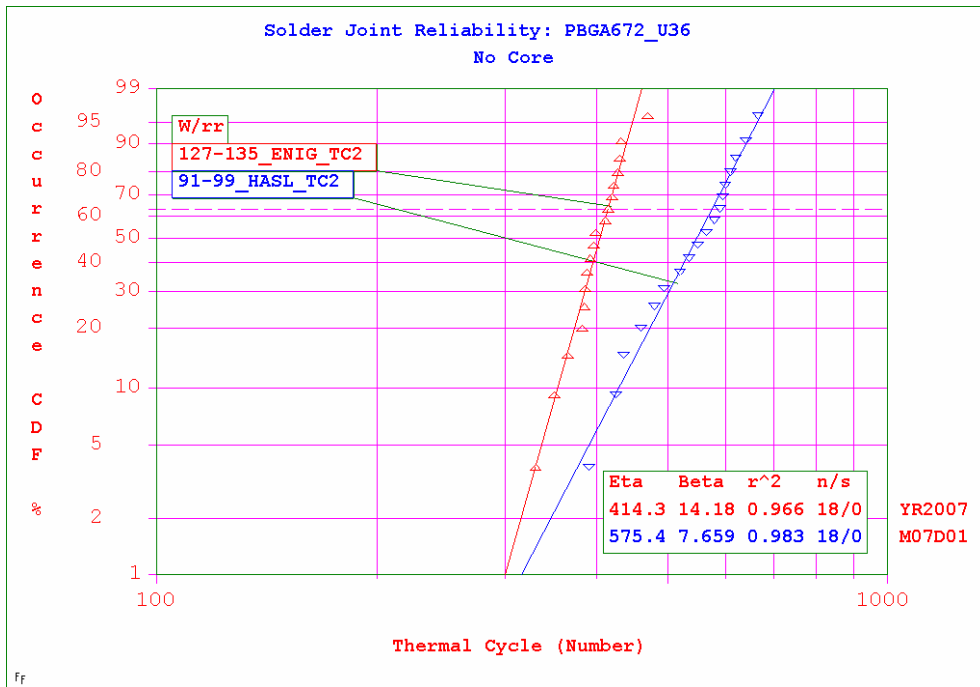


Figure A.16. Weibull plot results for PBGA672.

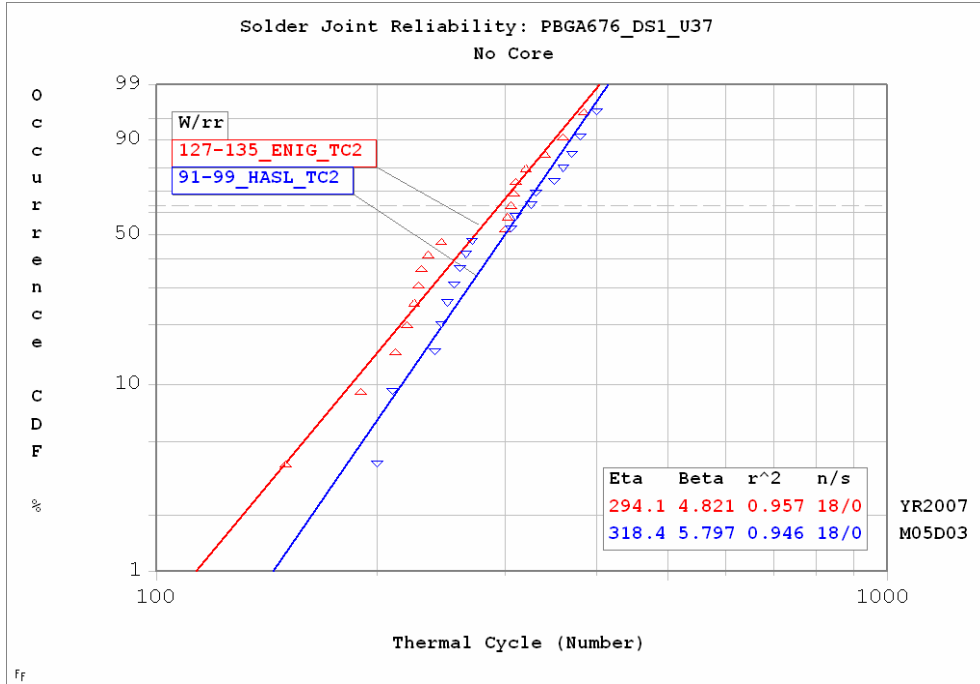


Figure A.17. Weibull plot results for PBGA676.

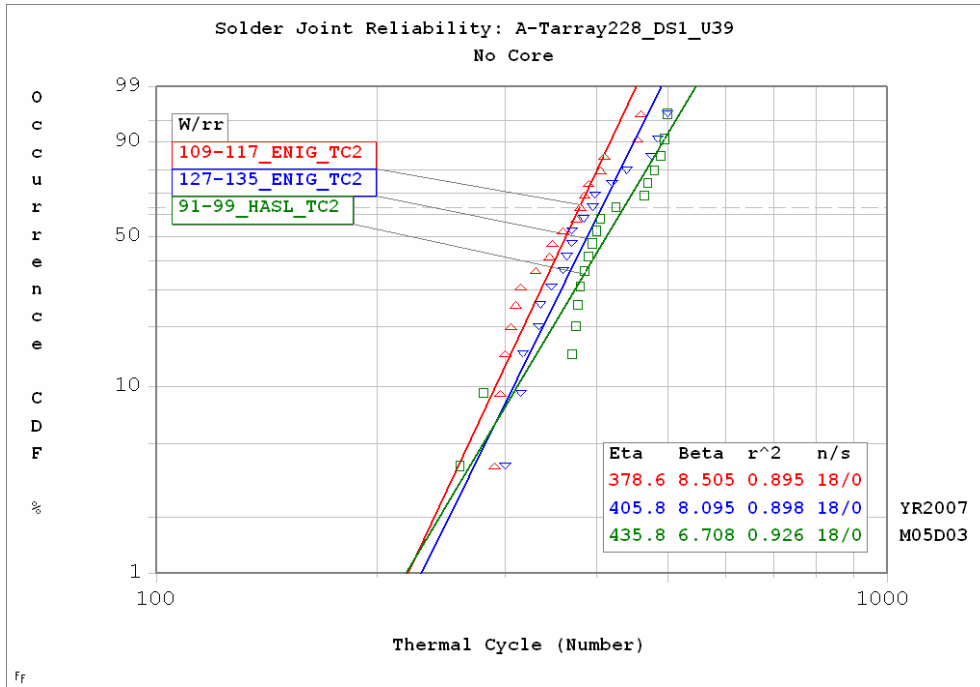


Figure A.18. Weibull plot results for A-Tarray228_DS1.

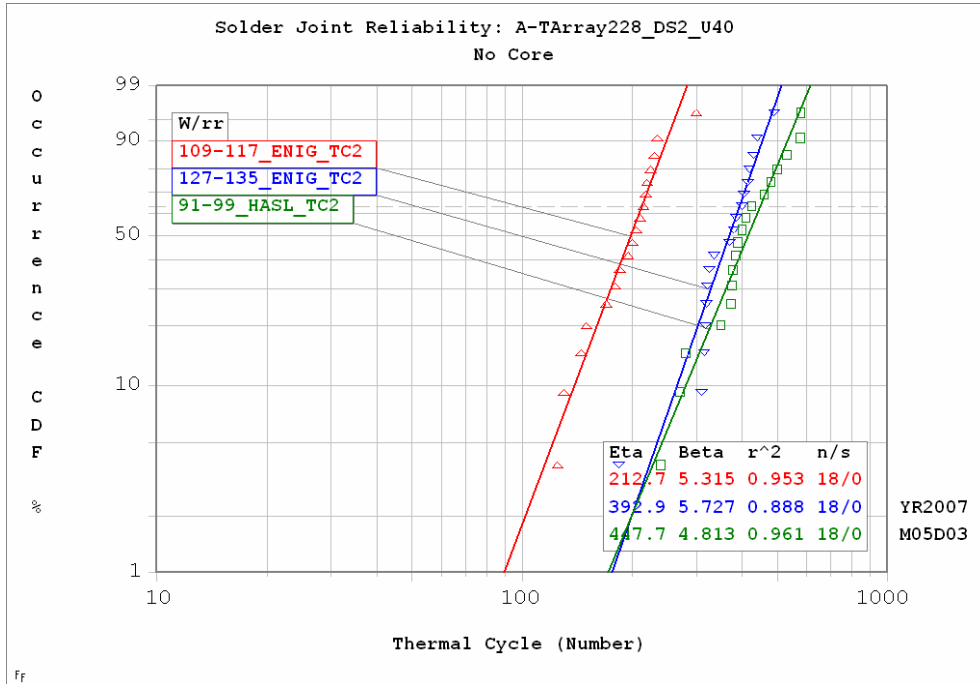


Figure A.19. Weibull plot results for A-Tarray228_DS2.

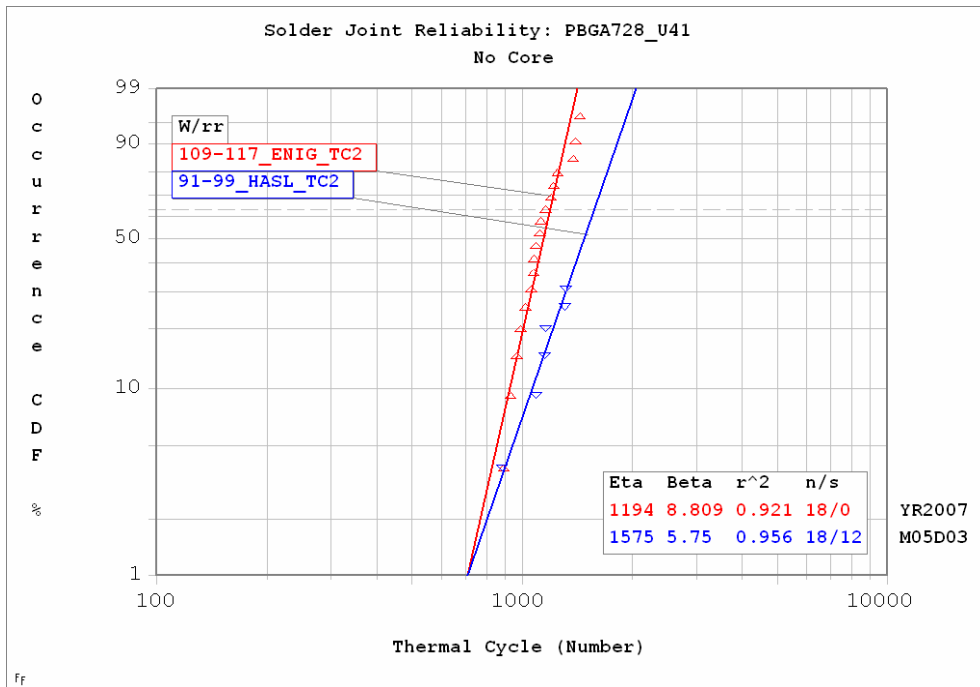


Figure A.20. Weibull plot results for PBGA728.

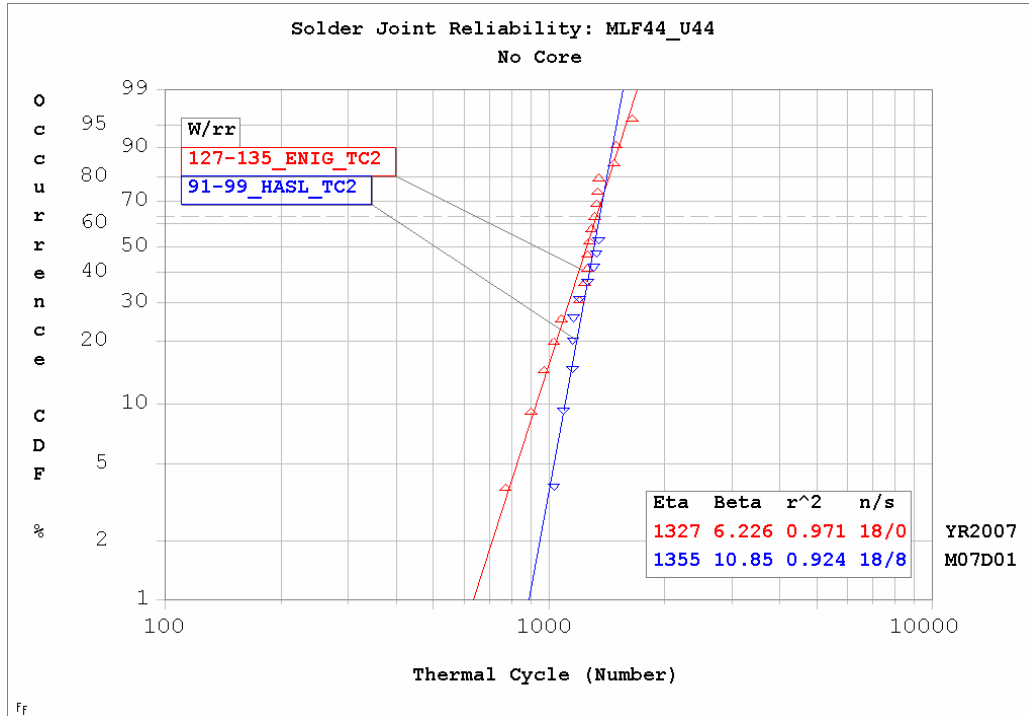


Figure A.21. Weibull plot results for MLF44.

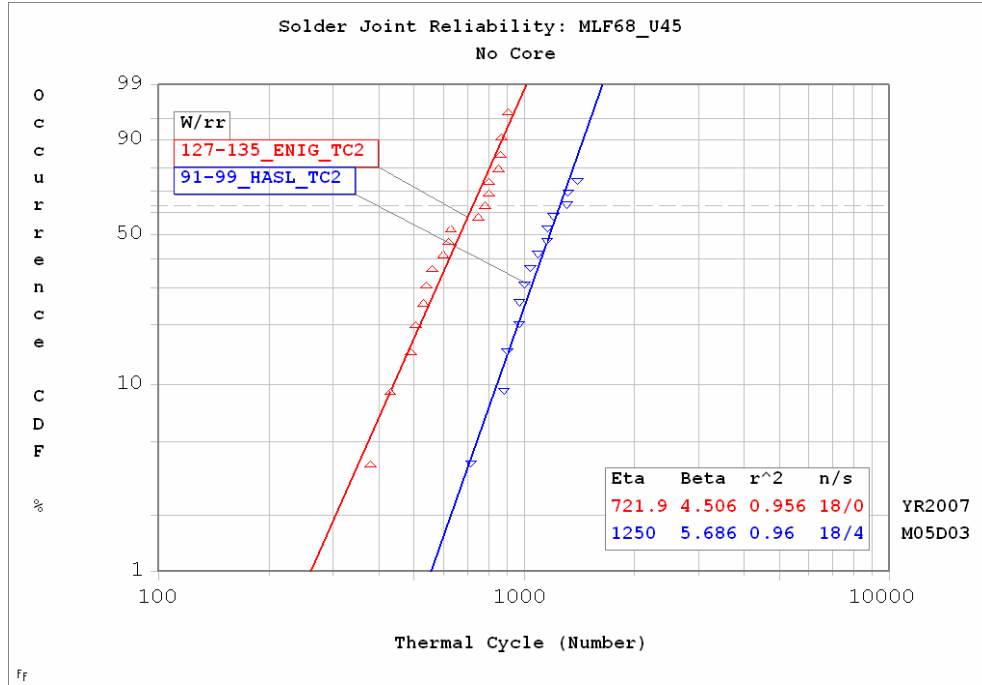


Figure A.22. Weibull plot results for MLF68.

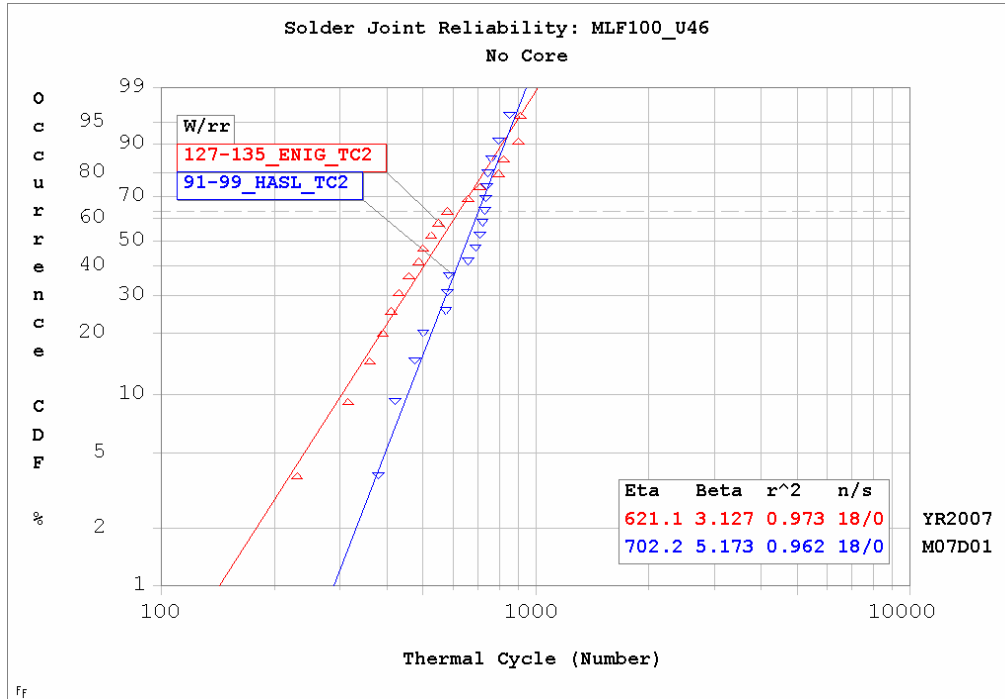


Figure A.23. Weibull plot results for MLF100.

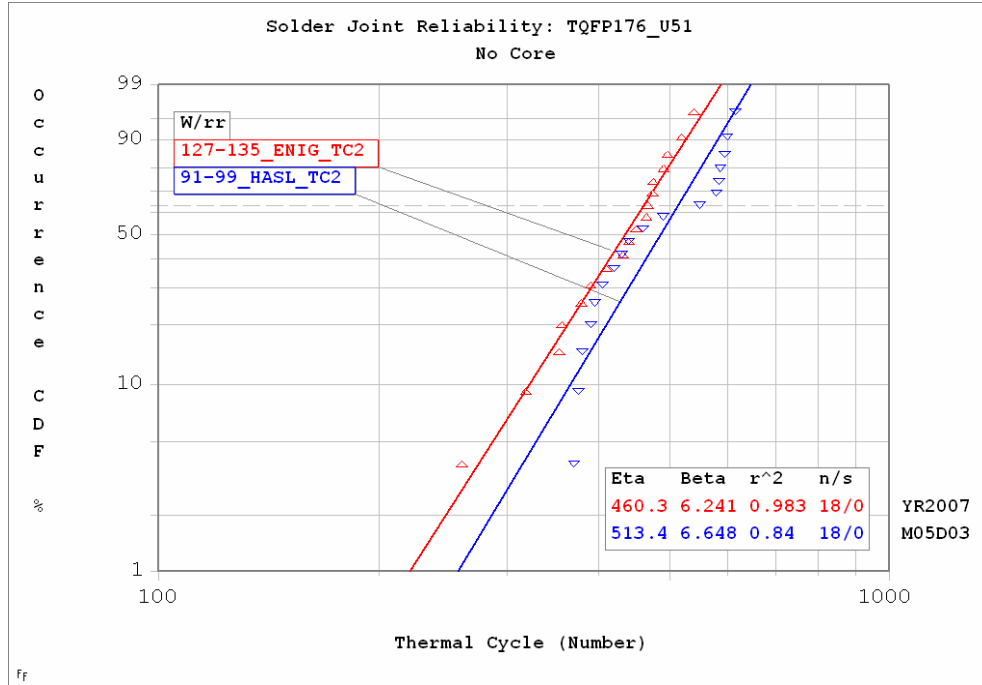


Figure A.24. Weibull plot results for TQFP176.

APPENDIX B

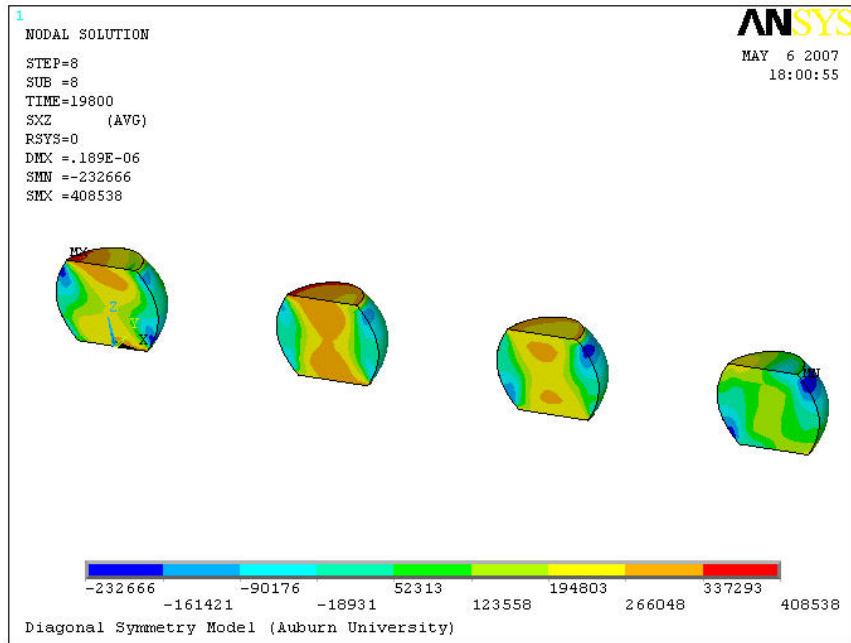


Figure B.1. XZ Shear Stress plot of all eutectic solder joints subjected to TC2 condition.

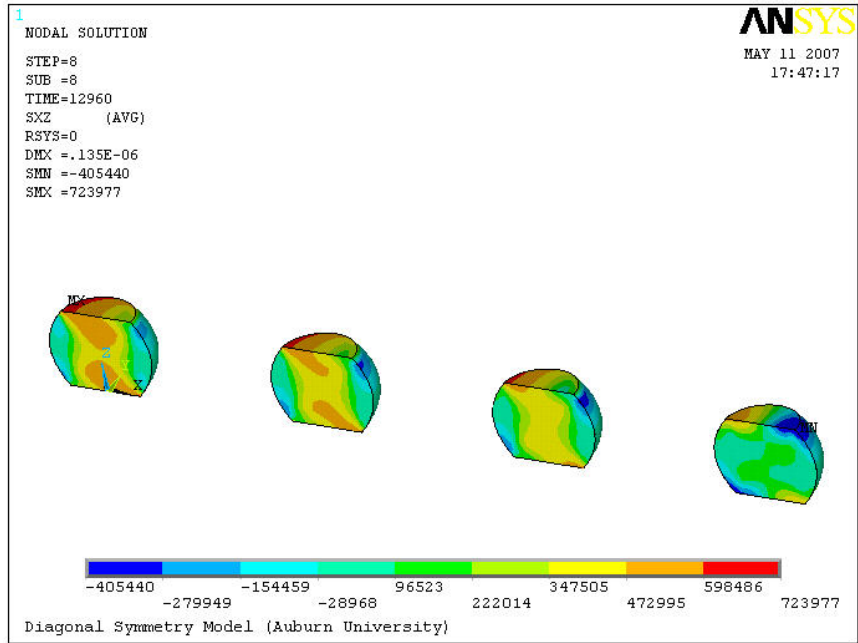


Figure B.2. XZ Shear Stress plot of all eutectic solder joints subjected to TC3 condition.

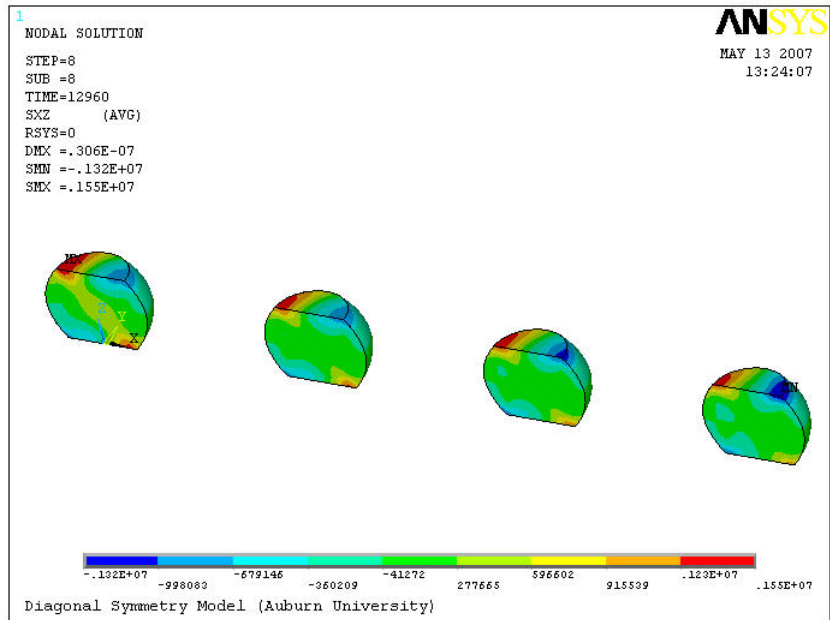


Figure B.3. XZ Shear Stress plot of all eutectic solder joints subjected to TC4 condition.

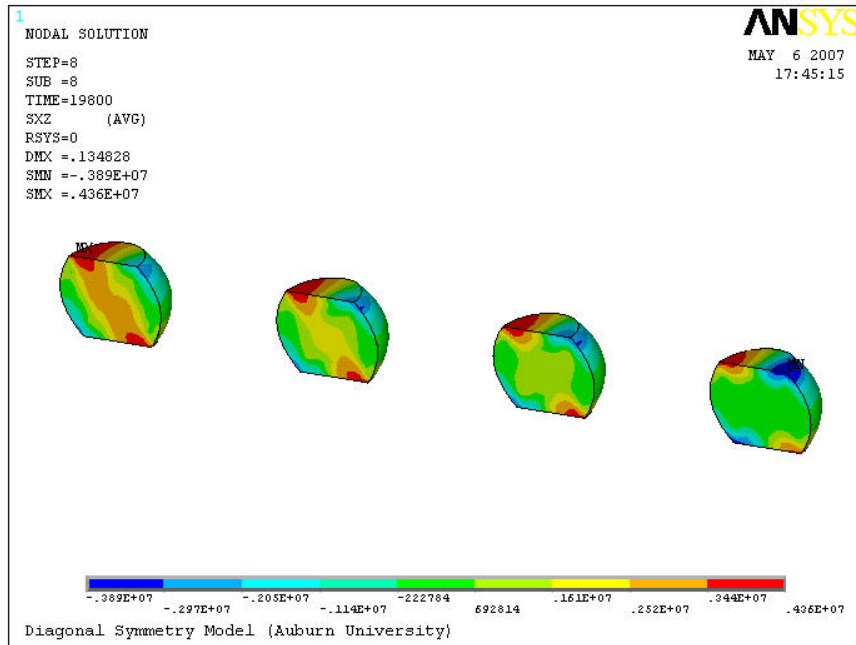


Figure B.4. XZ Shear Stress plot of all SAC305 solder joints subjected to TC2 condition.

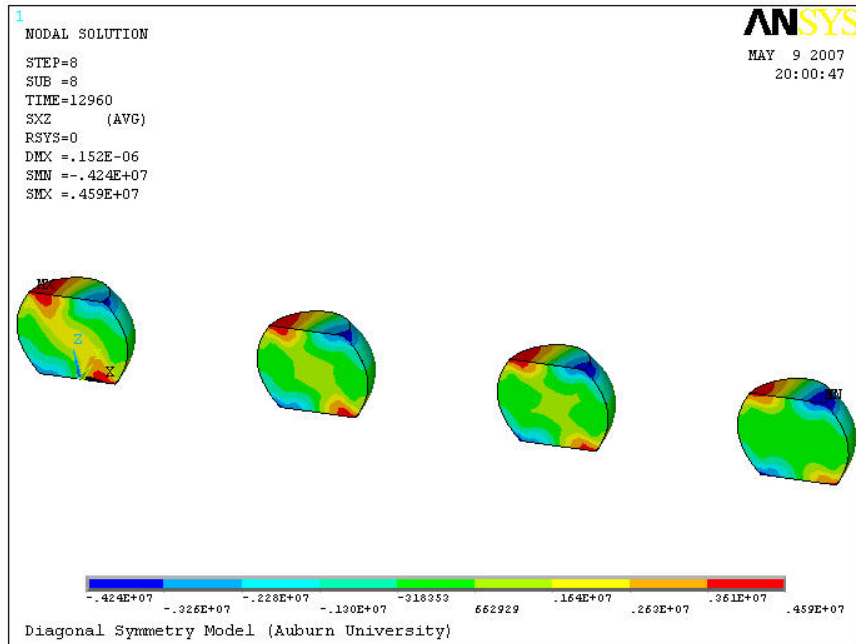


Figure B.5. XZ Shear Stress plot of all SAC305 solder joints subjected to TC3 condition.

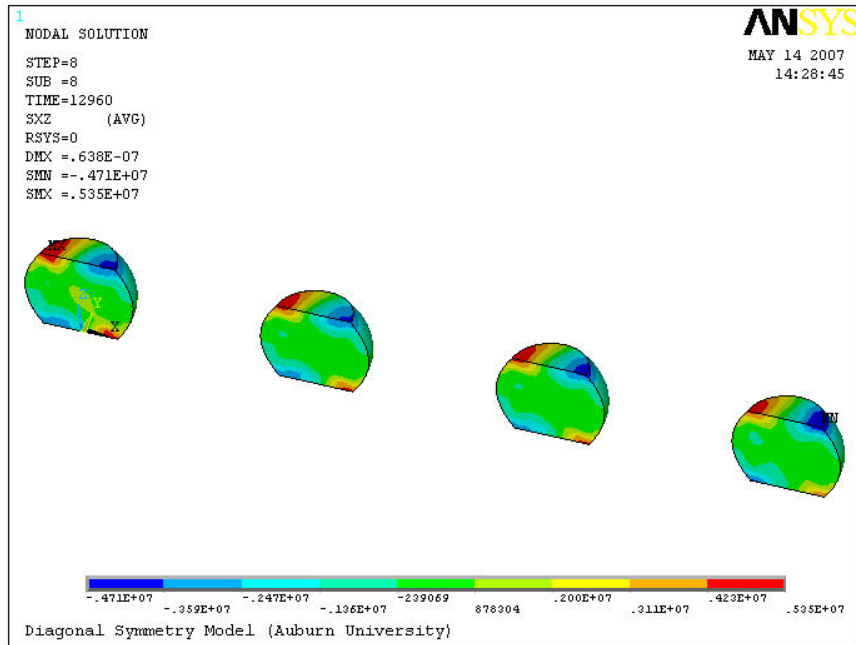


Figure B.6. XZ Shear Stress plot of all SAC305 solder joints subjected to TC4 condition.

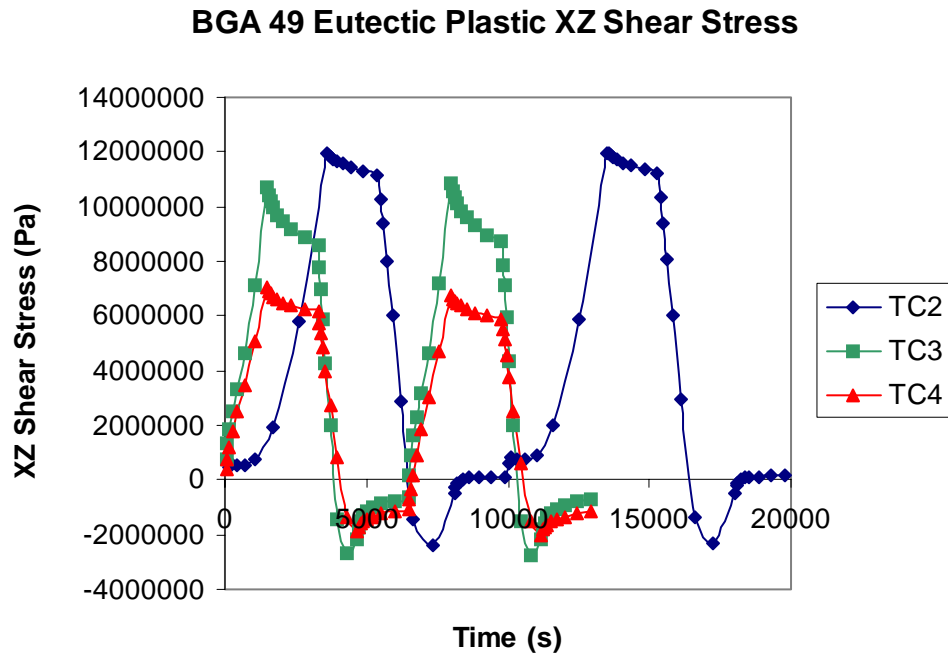


Figure B.7. XZ Stress vs. Time plot for eutectic solder.

BGA 49 Eutectic Plastic XZ Shear Strain

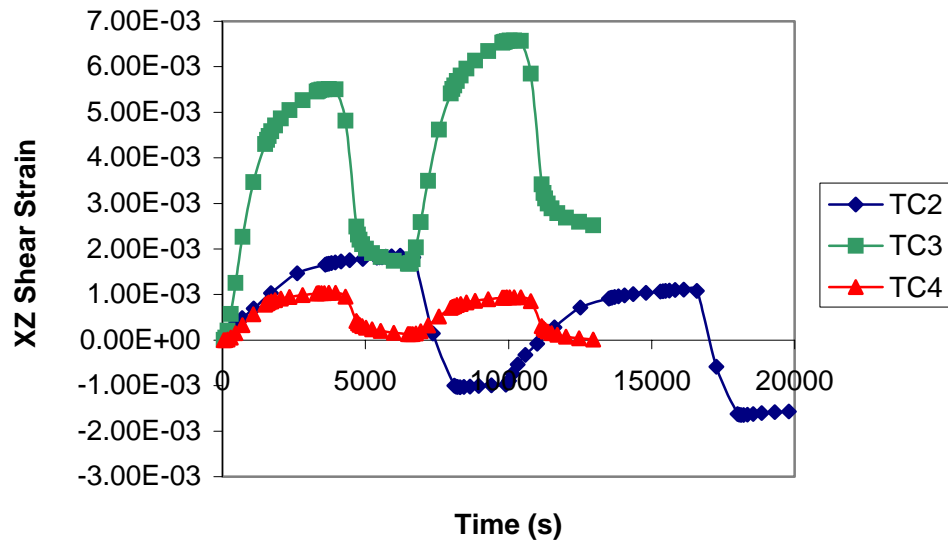


Figure B.8. XZ Strain vs. Time plot for eutectic solder.

BGA 49 SAC305 Plastic XZ Shear Stress

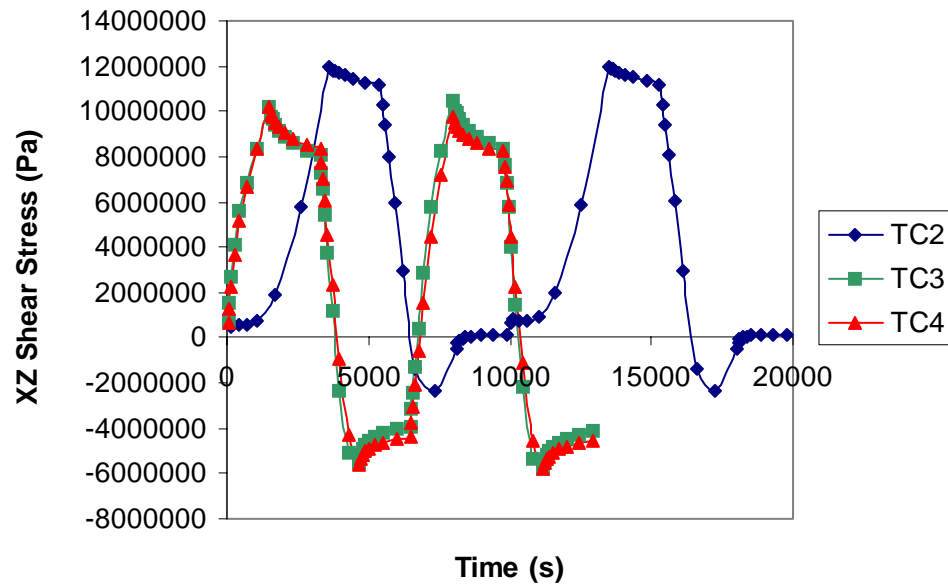


Figure B.9. XZ Stress vs. Time plot for SAC305 solder.

BGA 49 SAC305 Plastic XZ Shear Strain

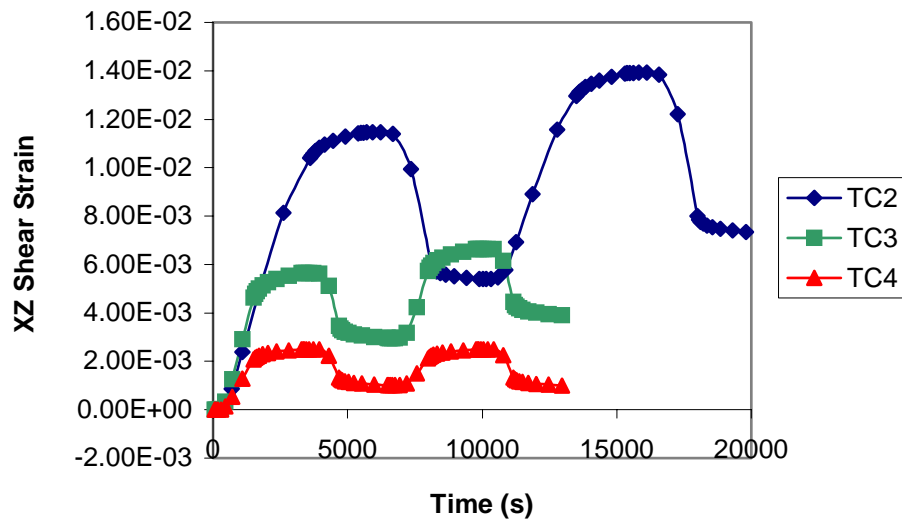


Figure B.10. XZ Strain vs. Time plot for SAC305 solder.

BGA 49 Eutectic XZ Hysteresis Loop

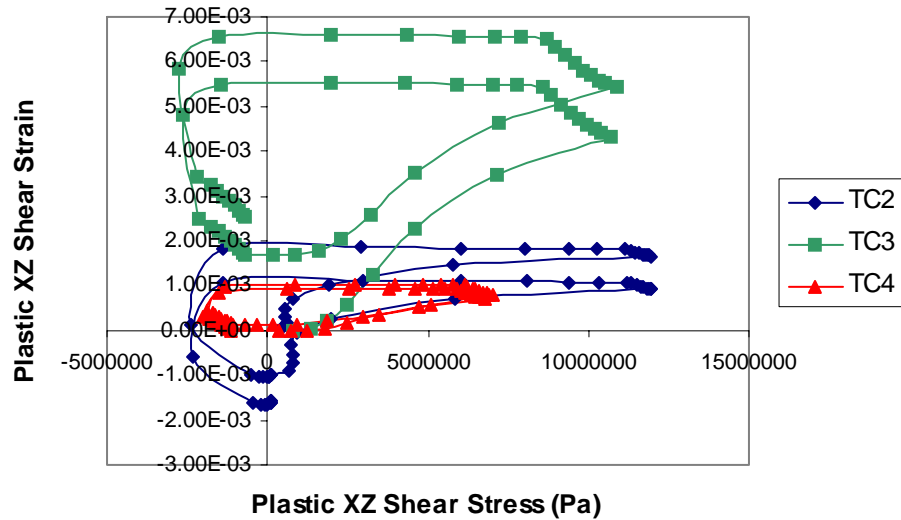


Figure B.11. XZ Hysteresis plot of eutectic solder for TC2, TC3, and TC4 conditions.

BGA 49 SAC305 XZ Hysteresis Loop

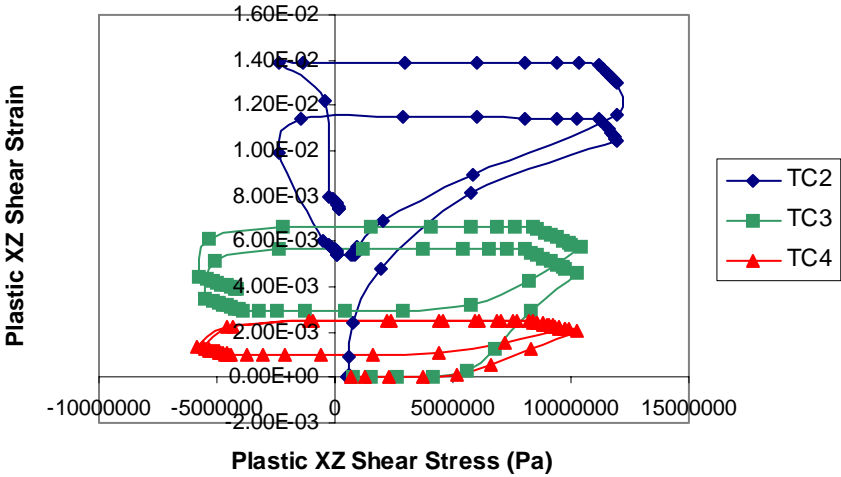


Figure B.12. XZ Hysteresis plot of SAC305 solder for TC2, TC3, and TC4 conditions.