THERMO-MECHANICAL RELIABILITY MODELS FOR LIFE PREDICTION OF BALL GRID ARRAYS ON CU-CORE PCBs IN EXTREME ENVIRONMENTS

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Date of Graduation

VITA

Jonathan Luke Drake, son of Richard and Joe Anne Drake, was born on August 26, 1982 in Phoenix, Arizona. He graduated in May of 2004 with a Bachelor's Degree in Mathematics from East Tennessee State University. After obtaining his Bachelor's Degree, he attended the University of Alabama at Huntsville from May 2004 through August 2005 where he continued his education and completed all of the engineering coursework needed to enter the Master's program in Mechanical Engineering at Auburn University. Since entering the M.S. program at Auburn, he has worked under the guidance of Professor Pradeep Lall, in the Department of Mechanical Engineering as a Graduate Research Assistant in the area of harsh environment electronic packaging reliability. While working under Dr. Lall, he was doing research for Northrop Grumman in Chicago, IL through Auburn University. He has also completed internships at Ford Motor Company in Detroit, MI and Shaw Group Inc. at Browns Ferry Nuclear Plant in Athens, AL.

THESIS ABSTRACT

THERMO-MECHANICAL RELIABILITY MODELS FOR LIFE PREDICTION OF BALL GRID ARRAYS ON CU-CORE PCBs IN EXTREME ENVIRONMENTS

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In this work, thermo-mechanical models for reliability prediction of BGA packages mounted on Cu-core printed circuit assemblies in harsh environments have been developed. The models have been developed based on thermo-mechanical reliability data acquired on copper-core assemblies in four different thermal cycling conditions. Solder alloys examined include SnPb and SAC alloys. The models presented in this paper provide decisions guidance for smart selection of component packaging technologies and perturbing product designs for minimal risk insertion of new packaging technologies. In addition, qualitative parameter interaction effects, which are often ignored in closed-form modeling, have been incorporated in this work.

Multivariate linear regression and non-linear finite element models have been developed for prediction of geometry and material effects. MLR approach uses the potentially important variables from stepwise regression. The statistics models are based on accelerated test data acquired as part of this thesis, in harsh environments, while finite-element models are based on damage mechanics and material constitutive behavior. Sensitivity relations for geometry, materials, and architectures based on statistical models, and FEA models have been developed. Convergence of statistical, failure mechanics, and FEA based model sensitivities with experimental data has been demonstrated. Validation of model predictions with accelerated test data has been presented.

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CHAPTER 1

INTRODUCTION

Electronics has become the largest industry, surpassing agriculture, automotive, and heavy metal industries [Tummala. et al. 1997]. Over the past three decades, there have been dramatic advances in the area of microelectronics. Today's trend in the electronic packaging industry is to make products that are smaller, faster, and lighter but at the same time they want to make them more reliable, powerful, and affordable. The continuous drive toward high density and low profile integrated circuit (IC) packaging has led to the growing application of ball-grid array (BGA) assemblies. BGA packages with area-array configurations offer many advantages over their predecessors. Smaller footprint, faster signal transmission, lower thermal resistance between the package and the printed circuit board (PCB), and ease of handling are only a few of the advantages that BGAs have over quad flat package (QFP), dual inline packages (DIP), and leadless chip carriers (LCC).

1.1 Functions of Electronic Packaging

In this day of age, almost every electrical device that is used, calculators, cell phones, computers, televisions and ipods, contain numerous forms of electronic packages. Electronic packaging is defined as the art of establishing interconnections between various levels of electronic devices, components, modules and systems. These packages contain various electrical components which include transistors, resistors, capacitors, diodes, as well as other devices. In turn, all of these devices must be interconnected to one another to perform a specific function or multiple functions. The connection of multiple devices to perform a function is called a circuit. As this level of integration increases, these multiple circuit connections are moving towards integrated circuit (IC) chips. Mechanical support and environmental protection are required for the ICs and their interconnections. To function properly, electrical circuits must be supplied with electrical energy, which is consumed and converted into heat. In order for these circuits to operate at their peak performance, they must maintain a certain operating temperature. Thus packaging serves four main functions:

- Power Distribution
- Heat Dissipation
- Signal Distribution
- Mechanical, chemical, and electromagnetic protection of components and interconnections

These functions are illustrated in figure 1.1 In addition to providing the four functions listed, the package must function at its specified performance level as decided by the requirements of the electronic product of system.

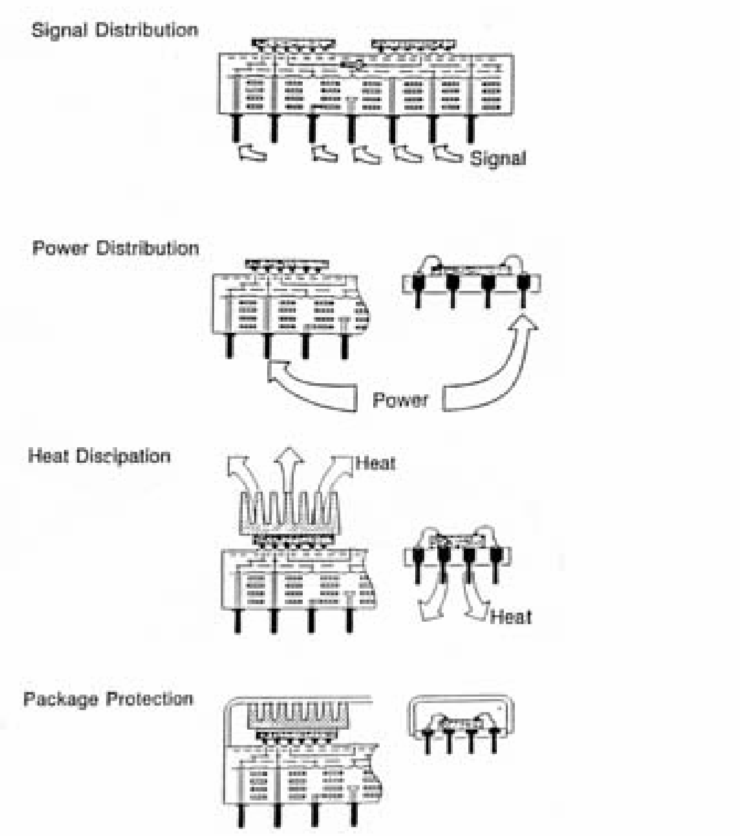
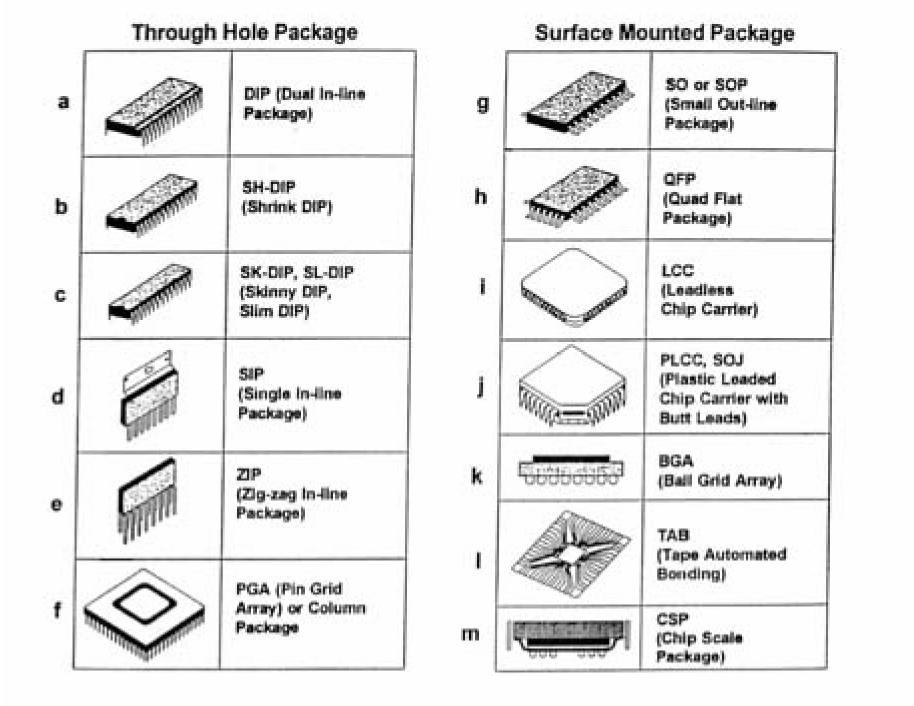


Figure 1.1 Four Main Functions of Electronic Packaging [Tummala 1997]

1.2 Evolution of Electronic Packaging

Throughout the past few decades, chip carrier technology has drastically evolved to keep up with the rising demand for higher input/output (I/O) connections per chip, higher I/O density, lower weight, faster signal speed, and lower cost. See Table 1.1 for the various packaging technologies used over the years. The original packaging devices were typically large. In the 1970's most packaging technologies were plated through-hole (PTH) Dual In-Line Packages (DIPs). With DIPs, the I/Os are aligned along each side of the chip carrier in the form of pins, or leads, which were plated with tin and lead (Sn/Pb). In order to create more I/Os, more leads had to be added, which in turn, caused the overall package size to increase dramatically. DIP packages have an upper limit of 64 pins, after which the package simply becomes too large for any practical application. In order to solve this problem and attain higher I/O connections, manufacturers began to build Pin Grid Array (PGA) packages where the I/Os were arranged in an area array underneath the package. PGA packages typically have an upper limit of 200 pins. The Quad Flat Package (QFP) was created as an extension to the small outline package. QFPs have higher I/O connections compared to the small outline packages, but still occupied too much space. However, the main problem with through-hole devices is their size. The trend for manufacturers was to increase density while decreasing the amount of space used on the printed circuit board (PCB).



Through Hole Package	
a	DIP (Dual In-line Package)
b	SH-DIP (Shrink DIP)
c	SK-DIP, SL-DIP (Skinny DIP, Slim DIP)
d	SIP (Single In-line Package)
e	ZIP (Zig-zag In-line Package)
f	PGA (Pin Grid Array) or Column Package

Surface Mounted Package	
g	SO or SOP (Small Out-line Package)
h	QFP (Quad Flat Package)
i	LCC (Leadless Chip Carrier)
j	PLCC, SOJ (Plastic Loaded Chip Carrier with Butt Leads)
k	BGA (Ball Grid Array)
l	TAB (Tape Automated Bonding)
m	CSP (Chip Scale Package)

Table 1.1 Various Packaging Technologies [Tummala 1997]

In the 1980's, through-hole technology began to phase out and a new type of technology, called Surface Mount Technology (SMT) became the main emphasis. With this technology, there was no longer a need to drill holes through the PCB. Instead, the leads from these packages mounted directly to copper plated pads on the surface of the printed circuit board in the form of solder balls. This allowed the width of the leads to become smaller, the spacing, or pitch, between them was drastically decreased, and also allowed a package with the same number of pins as a traditional through-hole device to be significantly smaller in area. Ball Grid Array (BGA) packages are an example of this type of surface mount technology. Figure 1.2 shows the evolution of the various packing technologies.

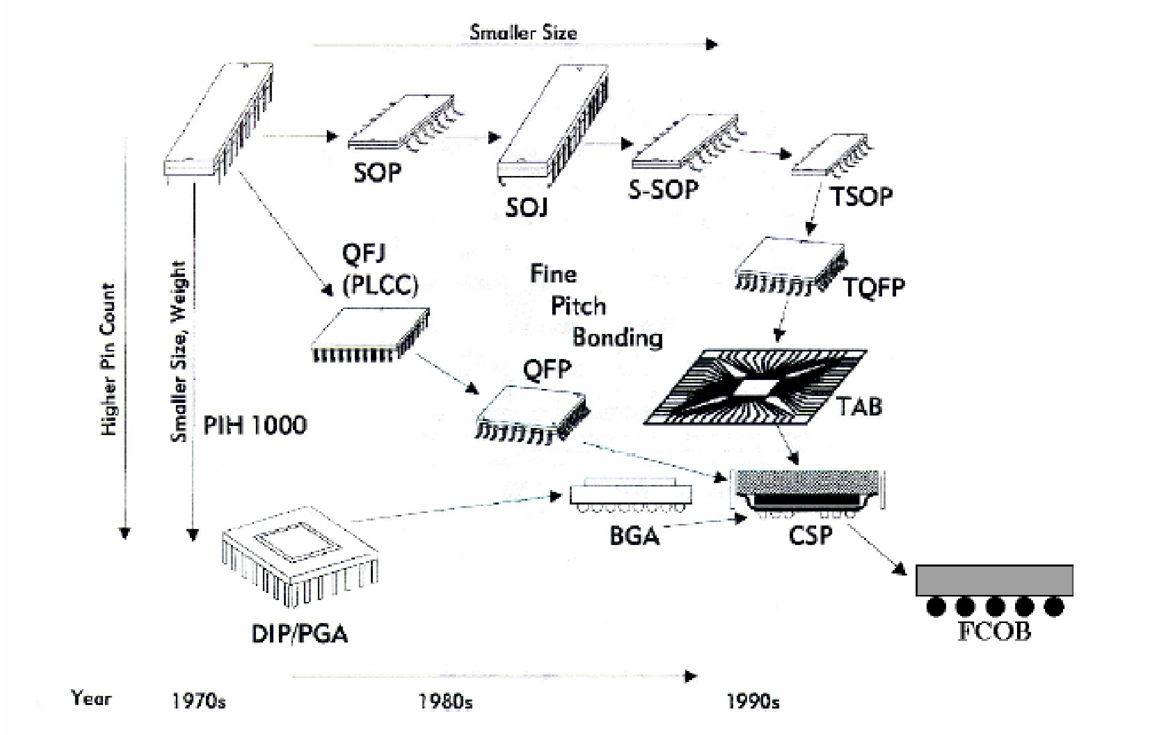


Figure 1.2 Evolution of Various Packaging Technologies [Tummala 1997]

1.3 Ball Grid Array Packages

The IC packaging technology [Suhling, 2003] in the past has evolved from the inline and peripheral array packages such as single inline package (SIP), dual inline package (DIP), plastic leaded chip carrier (PLCC), quad flat package (QFP) or leadless ceramic chip carrier (LCCC) to an area array packaging such as ball grid array (BGA). The BGA is a solution to the problem of producing a miniature package for an integrated circuit with many hundreds of pins. Pin grid arrays, BGAs' predecessors, were being produced with more and more pins which resulted in lowering the pitch between pins.

Creating larger PGAs with more pins seemed like a good idea, until the pitch became small enough that it began to create soldering issues. Bridging between solder joints during the soldering process became a major concern. BGAs do not have this problem because the solder is factory-applied to the package in the exact volume needed.

In a typical BGA package, the pins have been replaced by spheres of solder which are applied to the bottom of the package. It is then placed on a PCB which carries copper pads arranged in the same grid pattern that matches the solder balls on the package. The entire assembly is then heated by an infrared heater or in a reflow oven which causes the solder balls to melt. The molten solder balls are held in place by surface tension while the solder cools and solidifies to the printed circuit board. The composition of the solder alloy and the soldering temperature are carefully chosen so that the solder does not completely melt, but stays semi-liquid, allowing each ball to stay separate from its neighbors. Figure 1.3 shows a schematic drawing of a typical PBGA package.

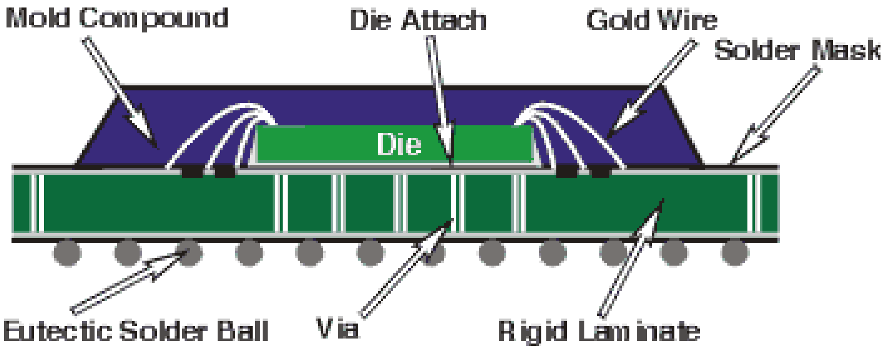


Figure 1.3 Cross-Sectional View of typical PBGA on PCB

Advantages: Ball Grid Arrays allow for a higher number of interconnects in a much more compact space, thus maximizing available space on the PCB. BGAs also allow computerized robots on assembly lines to pickup and move these packages much easier than leaded chips which have very fragile leads. As stated above, one of the main advantages to BGA packages is that during the soldering process, the manufacturers do not have to worry about bridging of solder joints. Another advantage over leaded packages is it lowers the thermal resistance between the package and the printed circuit board. This keeps the chip from overheating by allowing heat that was generated from the integrated circuit inside the package to flow more easily to the PCB. Since the pins and peripheral arrays have been replaced by solder balls, thus creating a shorter electrical conductor, the inductance of the package is also lowered. The short distance between the package and the PCB creates a lower inductance which leads to better electrical performance compared to leaded devices.

Disadvantages: Although, there are many advantages to BGAs compared to leaded chip carriers, there are still a few drawbacks. One of the big disadvantages is that the solder balls can not flex the same way that longer leads can. In previous packages, the mismatch in thermal expansion coefficients between the PCB, the silicon die, the epoxy over-mold, and the Bismaleimide-Triazine substrate, or BT substrate was not as much of an issue as it is in BGAs. With BGAs, the bending and thermal expansion of the PCB is transmitted directly to the package. This, in turn, places great amounts of shear strain on the solder joints and causes them to fracture under high thermal and mechanical stresses, which will be covered more in depth throughout this paper.

However, this problem of mismatched CTEs can be overcome at a cost by matching the mechanical and thermal characteristics of the PCB to those of the silicon die and other materials of the BGA package more closely. Another disadvantage of the BGA is that it is very hard to analyze the package for soldering faults, such as voids or cracks, once the package has been soldered to the PCB.

1.4 Design Factors

The trend of electronic products is moving towards further miniaturization and improved performance. Today, manufacturing companies as well as consumers, such as cellular companies, computer, automotive, military, and aerospace companies have many factors determining which type of commercial off the shelf IC package to choose. Not only do they have a wide variety of package architectures to choose from, but they also must decide what the product will be used for, what their budget is, how reliable they want the package to be, as well as how much space they have allotted for the particular application. For instance, a military company may need the package to be sealed off from the elements as well as be capable of handling extreme temperature from -55C all the way up to 125C from one day to the next. Not only would this particular application need a package that has proven its reliability in this temperature extreme, but it would also have to be cost effective as well as use a minimal amount of space. Other applications may require only high reliability, in which the component could be fairly large and weigh twice as much as another product and be less costly. It all depends on the individual's or company's needs.

Cost: One of the most important factors in any industry in this day and age is the ability to design a product and offer it to the consumer at a reasonable price. Over the past few years, there have been many engineering advances in materials used which are all aimed at getting the same performance, but reducing the cost at the same time. If one manufacturer can build PBGAs cheaper than another and still produce around the same performance and reliability numbers as another, that manufacturer is going to prosper and the other, high priced company, will be short lived. Also, certain packages are more expensive than others. Ceramic packages and hermetically sealed packages cost much more than PBGAs and DIPs. Not only are the manufacturers trying to reduce costs, but each particular application must fully research which particular architecture is needed before a decision is made and thousands or even millions of dollars are spent.

Exposure: Electronic packaging is becoming more widely used in various technological applications and thus each particular application requires a different type of protection from environmental, mechanical, and even chemical exposures. Obviously the type of electronic package used in automotive[Lall 2004], aerospace, and military conditions is going to be subjected to much harsher thermal cycling, shock, and vibrations and need better protection from the elements than applications used in personal computers, office equipment, and cellular phones[Sillanpaa 2004].

Size: Aside from cost and exposure, the miniaturization of electronic devices has become the predominant design factor throughout the industry. Cellular phones, personal Global Positioning Satellites (GPS), personal computers, and many other military, aerospace, and automotive applications demand electronic devices to occupy minimal amounts of space. However, the overall size of the product depends on the application which it is used. For instance, and desktop computer, for use at home or in the office, can have larger electronic packages designed to occupy a larger area on the PCB than computer chips and their packaging used underneath the hood of an automobile inside an electronic controller where limited space is available.

Life and Reliability: A product's life, or number of cycles until failure, has become a critical factor for electronic packaging over the past decade. Millions of dollars are being spent each year to design products with higher reliability and increased life. However, from a design perspective, one must choose a product with the correct life span for the application. If the consumer decides to purchase an electronic package with a higher life than the application is needed, the company will be wasting money by purchasing a device with more life than is needed. On the other hand, if the consumer or company purchases a packaging device which has a shorter life span than needed and also begins production of components, premature failures will occur and there will be many unsatisfied customers to deal with.

When selecting which electronic package is right for certain applications, all of these design factors must be analyzed and taken into consideration first. There are many ways to simplify and decide which factors are important and which applications will optimize performance. One way in which this can be done, is to conduct accelerated experimental testing, such as thermal cycling, and to compare the results with actual field tested results. However, this task is very time consuming as well as tedious and costs to conduct the experiment are high as well, which could possibly delay estimated arrival of the product to the public or personal consumer. Another method is to use Finite Element Analysis (FEA) computational simulation to design the product and test it using a computer to build and conduct the analysis of the individual components. This method takes highly trained individuals to conduct and analyze what is needed and can yield false information if used by an untrained individual. No matter which methods a company uses, one must take into consideration that there is a fine balance between these four design factors when deciding which component to use in each individual application.

1.5 Thermo-Mechanical Reliability

Reliability is defined as the ability of a system or component to perform its required functions under stated conditions for a specified period of time. The operation of any electronic device generates heat and with the increasing device density of the IC chips the amount of heat flux generated by the integrated circuit chips has gone to a level of 100-200 $\frac{W}{cm^2}$ [Nimkar, et al. 2005]. Each time a device is powered up, the individual components heat up and cool down. This heating and cooling leads to thermal cycling of the electronic components which causes many problems, such as shear deformation, due to the mismatch in coefficients of thermal expansion (CTE) of each material. Figure 1.4 shows the varying CTEs for a typical PBGA package in this research.

Thermal cycling requirements pose one of the greatest reliability challenges for BGA style packages. Under severe operating conditions or applications that require a high level of reliability, a large number of thermal cycles must be sustained without fracturing solder balls [Galloway, et al 2005]. Since the different packaging components have different coefficients of thermal expansion (CTE), as shown, there is a differential in expansion of varying components. This differential in expansion causes stresses to occur throughout the different components, and over repeated thermal cycling, causes failures to occur throughout the package. These failures in each electronic device can occur in various modes and locations [Viswanadham and Singh 1998], as seen in figure 1.5

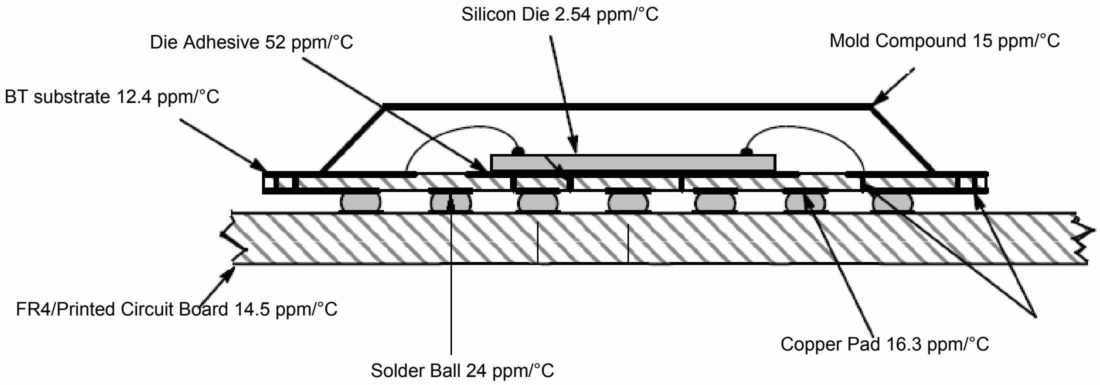


Figure 1.4 Typical PBGA package with corresponding Coefficients of Thermal Expansion (CTE) values

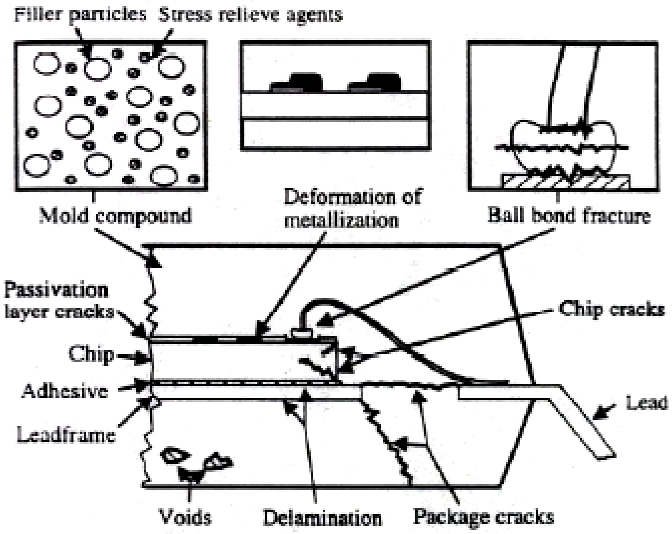


Figure 1.5 Failure Sites, Modes, and Mechanisms on a Plastic Encapsulated Package [Nguyen 1995]

During the solder joint reflow process, one of the most common failure modes in electronic packaging, known as the ‘Popcorn Failure’, occurs. A disadvantage of plastic molding compounds is that they are hydrophilic and absorb moisture when exposed to a humid environment [Nguyen, et. al. 1995]. This popcorn-like explosion happens when moisture that is trapped inside the molding compound becomes heated and vaporized during the solder joint reflow process and the only way for it to escape is to expand the molding compound until it cracks and the vapor is released. Ilyas and Roberts [1993] investigated the moisture sensitivity in several surface mount packages that included SOJ, PLCC, TQFP, and PQFP packages. Yip, et al. [1996] studied the moisture induced failures of Ball Grid Array packages such as PBGA and TBGA. They showed that baking the chips at 115°C for sixteen hours essentially removes most of the moisture content from the package, and reduces the possibility of the interfacial delamination and popcorn cracking of the package. By encountering this popcorn cracking, Lee [1996] studied and proposed a new lead frame design for improved reliability of these packages.

The cracking of the silicon die is another failure mode due in part to thermal stresses developed in the chip. These stresses could be caused from either the assembly stage or from the CTE mismatches within the package. Adhesives and molding compounds are the two key components which result in the highest CTE mismatches around the silicon die. From figure 1.4, one can see that the typical coefficient of thermal expansion for the molding compound is 15, the die adhesive is 52, and the silicon die is 2.54. These drastic differences in CTEs account for the majority of the cracks found in the silicon die after thermal cycling.

Edwards, et al. [1987] evaluated shear stresses during thermal cycling and thermal shock tests in the plastic packages and found that the shear stresses are heavily concentrated at the corners and edges of the silicon die. Okikawa [1987] analyzed plastic molded LSI packages subjected to thermal cycling and found that thermal stresses cause passivation film cracks in the package. Lau [1993] also studied and addressed the stresses due to the assembly stage of the package. He studied such aspects as wafer preparation, oxidation, diffusion, metallization, die and wire bonding, encapsulation, and the re-flow and curing processes. Lau [1993] also discussed several problems associated with stress, including package cracking, wire damage, and thin film cracking on the die. Suhling.[1999] measured flip chip die stresses using piezoresistive test die, and Zou [1999] analyzed the die surface stress variation during thermal cycling and thermal aging raliability tests.

Electronic packages are comprised of dissimilar materials which expand and contract at different rates upon heating and cooling. The differential expansion, or thermal mismatch, must be accommodated by the various structural elements of the package. The structural elements that absorb most of this mismatch in expansion coefficients are the leads and solder balls. These stresses developed during the package assembly or due to thermal cycling can lead to interfacial delamination and fracturing which could lead to decreased functionality or failure. Zou, et al. [1998] analyzed the effect of delamination on the die surface stresses and conducted the stress measurements of delaminated and non-delaminated plastic packages.

Clech [2000] studied the CTE mismatches of CSPs and BGAs with 1.27mm pitch using accelerated thermal conditions from -55 to 125ºC with 10 to 15ºC/min. ramps, 20-minute dwells, and a cycle duration of 68 minutes.

As the trend towards miniaturization continues, the size of the interconnect becomes smaller, and the solder joints become the weakest link in a packages overall reliability. In this study, structural and thermal reliability of ball grid array packages, mainly the shear stresses and strains of critical solder balls, have been investigated using accelerated life testing. Many studies and failure analyses have been conducted [Lall, et al 1997, 2004, 2005, Suhling, et al 2004, Clech 2000, Zbrzezny, et al. 2006, Syed 1996] showing that interconnect failures due to mismatches of CTE during thermal cycling is the most critical mode of failure in leaded and SMT packages such as BGAs. Figure 1.6 shows a schematic of what happens to the solder joints during thermal cycling due to mismatches in CTEs. It shows that at a stress free temperature, the two components, silicon and the PCB, are relaxed. Then, as the temperature increases, the PCB wants to expand at a higher rate since the PCB's CTE is 14.5 ppm/°C and the CTE of the silicon is 2.54 ppm/°C. As the temperature drops, the PCB wants to contract much quicker than the silicon. Looking at the schematic, one can see that the solder joints are having to flex and deform due to the mismatch in CTE between the two materials. Over time, these shear stresses and strains cause the solder joints to become fatigued, then cracks begin to propagate and the package will ultimately fail once a certain number of thermal cycles have been reached.

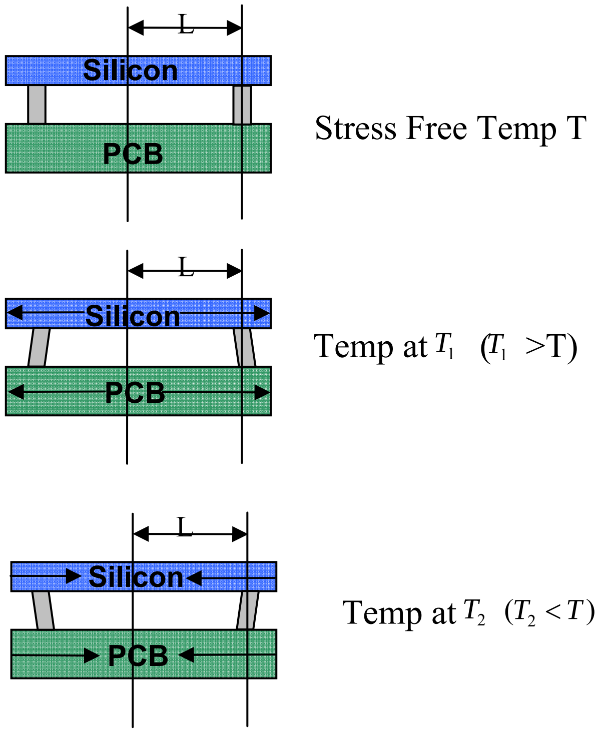


Figure 1.6 Schematic of CTE Mismatches and Solder Joint Failure due to Thermal Cycling

CHAPTER 2

LITERATURE REVIEW

It has been recognized that thermal loading is one of the major causes to the failure of electronic devices, especially surface mount packages. Chip delamination, solder joint cracking, and cracking of the silicon chip are only a few of the major problems due to the mismatch of the coefficients of thermal expansion (CTE) in the various layers that make up each individual package. This makes the solder joint reliability analysis one of the most important and focused issue as far as the reliability and life of the electronic packages is concerned [Harper, 2004]. There is a plethora of published literature available addressing solder joint reliability and life prediction. Within these literatures, there is a multitude of methodologies used for the solder joint fatigue life prediction of area array packages. Some of the methodologies used include experimental techniques using accelerated thermal cycling tests and closed form models based on the theory of failure mechanics, finite element analysis, and statistics based multivariate regression analysis.

2.1 Experimental Techniques

There are several experimental tests which are performed in order to study the reliability of electronic devices and are designed to operate under certain environmental conditions. Extreme temperatures, high humidity levels, and vibration are a few of the environmental conditions that are tested experimentally. Researchers have applied various test conditions such as the accelerated thermal cycling, thermal shock, HAST (highly accelerated stress test) and vibration tests, to analyze the reliability of the packages for various applications.

Syed [1996] conducted accelerated thermal cycling to determine the effects of four design parameters on the thermal fatigue life of solder joints in automotive under-the-hood environment. The four parameters considered were: substrate thickness, array configuration, ball pitch, and pad size. After conducting the experiment on three BGA configurations, standard, perimeter array, and thicker BT substrate BGA's, he discovered that the CTE mismatch between the board and the package, and the load bearing area of the solder joints are the two main drivers of solder fatigue. For the levels considered in his experiment, the results from the combined design of experiment and validated life prediction model indicated that one could improve the life of the solder joints up to five times by using perimeter array, 0.76mm BT substrate, 0.635mm pads, and 1.27mm pitch.

Lall, et.al [2006] conducted thermal cycling tests, from -40°C to 125°C, to determine the effect of metal-backed boards on the interconnect reliability. In this study 15mm C2BGAs, 27mm BGAs, and 1225 chip resistor solder joints were cross sectioned at every 125cycles to measure crack propagation. It was reported that the addition of metal backing increases the CTE of the substrate and creates potential reliability issues for many electronic packages. It was shown that the crack propagation rate on metal back boards is approximately 1.7 times faster than nonmetal-backed boards, and that BGAs on metal backed boards exhibit a lower number of cycles-to-crack initiation that packages on nonmetal-backed boards for any inelastic strain energy density.

Darveaux, et.al. [1998, 2000] conducted several board level thermal cycling reliability tests using FBGAs (flex BGA's), TABGAs (tape array BGAs), PBGAs, and μBGA packages. Multiple package and board variables were tested, and it was found that fatigue life increased up to 6X as dies size was reduced. Also shown that for a given die size, fatigue life was up to two times longer for larger packages, and solder joint fatigue life was 20% longer for 0.9mm thick test boards compared to 1.6mm thick test boards. He also showed that there was a 1.6 times greater acceleration factor between thermal cycling profiles of -40°C to 125°C and 0°C to 100°C.

Knight, et.al. [2006] studied the effect of thermal cycling of ball grid array packages on die size, thermal ball, number of perimeter balls, the use of underfills, and printed circuit board heat spreader and thermal via design. He showed that as a result of thermal cycling from -40°C to 125°C, the thermal resistance of the packages with large die size increased significantly, with thermal degradation preceding electrical failure by several hundred cycles. His study also showed that the critical thermal balls cracked before the critical perimeter ball, which is a contradiction in conventional electronic packaging. Normally, the ball furthest from the package's center, the perimeter ball, would crack first, due to the distance to neutral point (DNP) formula. However, in this study, the cracking of the critical thermal ball can be attributed to the fact that the thermal balls were mounted on a relatively thick copper heat spreader. This lead to a mismatch in

CTE of $\frac{13.8\times10^{-6}}{K}$ between the die and the PCB near the thermal balls, where as th mismatch near the perimeter balls was only $\frac{12\times10^{-6}}{K}$.

2.2 Failure Mechanics Based Analytical Modeling

Clech, et. al [1993] discovered that some predictive tools, like AT&T's Figure of Merit, contained many errors when they were applied to different surface mount packages. After discovering this, he developed a comprehensive surface mount reliability (CSMR) model which was based on the correlations of 28 accelerated tests in the surface mount reliability database and was validated by nine accelerated test data sets. This model uses one-dimensional structural models to estimate solder joint stress/strain hysteresis due to global and local CTE mismatches during thermal cycling. He found that when it was exercised over the entire database, the new model had a correlation coefficient of 0.97 compared to the 0.40 or less for earlier models. The CSMR model was further extended to another Design-for-Reliability Tool, the Solder Reliability Solution (SRS) moded, which was used for the reliability of predictions of leadless ceramic chip carriers (LCCC's) and area array assemblies. He validated the SRS model for a variety of BGA, flip chip, and CSP assemblies as well [Clech, 2000].

Lall, et. al. [2005] used a hybrid approach between failure mechanics based and statistics based methodology to identify critical parameters and their sensitivities on the thermal reliability of certain BGA packages. This study used a combination of Timoshenko beam theory [1925], and its application to tri-material assemblies [Suhir 1990], calculation of time-independent plastic deformation, calculation of stress relaxation, hysteresis loop calculation [Clech 1996], and life prediction [Darveaux 1992]. Bartelo, et. al. [2004] used failure mechanics methods to study the thermo-mechanical fatigue behaviors of Sn-Ag-Cu solder joints in terms of their Ag content, cooling rate, and ATC test condition. This studied showed that 2.1Sn-0.9Ag-0.9Cu solder joints assembled at a slow cooling rate have the best thermal fatigue life over the high silver content joints for the ATC test of 0°C to 100°C with a 120 minute cycle time.

2.3 Statistical Modeling

Regression analysis and Weibull distribution are the two most common methods of statistical analysis being used by researchers to display trends and analyze failure data in electronic packaging today. Lall, et. al. [2005, 2006] used a combination of statistics-based and failure-mechanics based methodology to identify the critical parameters and their sensitivity on the thermal reliability of BGA packages. Sensitivities of reliability to design, material, architecture, and environment parameters were developed from both statistical and failure mechanics and then validated with experimental data. Multivariate regression and analysis of variance techniques were used to determine the relative influence of these parameters on thermal reliability. Montgomery, et. al. [2002] used traditional multivariate regression methods to analyze trends in the large amounts of data produced by probe testing following wafer fabrication. Clustering analysis was the preferred method for analyzing this data, however this method of analysis proved useless in this study. Linear regression analysis was also used in this study and they were able to obtain some interpretable results. The method of Classification and Regression Trees (CART), based on a recursive partitioning algorithm, proved to be the model-building approach that worked best for their data. This study highly recommends using this method when applicable as it was able to explain 91.9% of their data.

Lall, et. al [2006] used statistics-based closed-form models based on multivariate regression, analysis of variance, and principal components to analyze flip-chip assemblies subjected to thermo-mechanical stresses. The study investigated the material properties and the geometric parameters such as die thickness, die size, ball count, ball pitch, bump metallurgy, underfill types, underfill glass transition temperature (T_g), solder alloy compostion (SnAgCu, SnPbAg), solder joint height, bump size, and printed circuit board thickness. Model input variables were selected by defining all predictors that were known, and then selecting a subset of predictors to optimize a predefined goodness-of-fit function. The appropriateness of the model was checked by using any one combination of the several of the features of the model, such as linearity, normality, or variance which may be violated. The statistical model methodology provided in this study was validated against the experimental accelerated test failure data from the Center for Advanced Vehicle Electronics (CAVE). This studied showed that there is a direct correlation between what the statistical models predicted and what the experimental data actually showed for each of the geometric parameters and their effects.

2.4 Finite Element Modeling

Finite element modeling is an important tool for analyzing complex systems, such as chip-scale packages. FEA (Finite Element Analysis) has been a widely used methodology for solder joint reliability [Darveaux 1996, Syed 2001, Zahn 2000, 2003] analysis and life prediction of various electronic packages. By providing a more thorough understanding of the complex behavior associated with chip-scale packages and their constituent materials, it is possible to create and optimize designs that can take advantage of variable material properties such as CTE and elastic modulus. Moreover, computer simulations of mechanical behavior help to identify design issues early in the design cycle and minimize the number of prototypes needed for tests. Thus, finite element modeling is a cost-effective method for rapidly moving products from concept to production while minimizing risk and increasing understanding of the overall system. FEA is a tool and a technique that should not be ignored if one hopes to keep pace in today's competitive electronics market.

Zahn [2000] used viscoplastic finite element simulation methodologies to predict ball and bump solder joint reliability for a silicon based five-chip multi-chip module package under accelerated temperature cycling conditions of 0°C to 100°C with five minute ramp and dwell times. For this portion of the study, ANSYS sub-modeling methodology was utilized by which global model simulation results were applied as boundary conditions. Further into this study, finite element analysis (FEA) was also used to evaluate the steady-state thermal performance of the multi-chip system. For this model, ANSYS was utilized to create a full-symmetry , three-dimensional FEA model of the 40x40mm, 697 ball 1.0 mm pitch because the structure was not symmetric. Zahn

[2003] also used 3-D slice and symmetry models for the purpose of deriving life prediction equations in order to determine the fatigue response of microelectronic package structures using both eutectic, 63Sn37Pb, and lead-free, 95.5Sn4Ag0.5Cu, solder materials. As a result of this study, it was shown that a combination of minimum true symmetry global modeling and straight slice symmetry global modeling may be the best approach to accurately and efficiently predict accelerated temperature cycling solder fatigue in large microelectronic package structure models such as the 15x15mm 196-lead PBGA and a 35x35mm 388-lead PBGA packages used here.

Pang, et. al. [2001] used finite element analysis to simulate thermal cycle loadings for solder joint reliability in electronic assemblies, namely flip-chip packages. This study was conducted to investigate different methods of implementing thermal cycling analysis, mainly using the dwell creep and full creep methods since there are significant differences between the analysis results for the flip chip solder joint strain responses and the predicted fatigue life of the two methods. A three dimensional slice model of the flip chip on board (FCOB) assembly was created using ANSYS software and used for analysis. After simulation was completed, it showed that the viscoplastic analysis using the 3-D slice model and Darveaux's [2000] model for solder joint fatige life prediction gave even more conservative fatigue life compared to the full creep analysis results observed in a previous study.

Darvaeux [2000] analyzed the effect of simulation methodology on solder joint crack growth correlation and fatigue life prediction using ANSYS 5.6 to run the simulation . Solder joint material was modeled with Anand's viscoplastic constitutive model [Anand 1985, Brown, et al. 1989], which is a standard option in ANSYS. Johnson

[1999] extended Darveaux's approach and implemented it for the finite element simulation of BGA solder joint reliability, Gustafsson et al., [2000] also used finite element modeling for the life prediction of BGA packages.

Lindley, et al. [1995] and Lall, et al. [2003] conducted solder joint reliability study on BGA and CSPs for the automotive underhood application. Yeh, et al. [1996] and Lu, et al. [2000] did parametric analysis of flip chip reliability based on solder joint fatigue modeling, via computer simulation. Time independent plastic behavior [Wiese, et al. 2002] of SnPb and SnAgCu solder alloy has been modeled and it's effect on the FEM (Finite Element Method) simulations of electronic packages.

Lau, et al. [2004] developed a thermal fatigue life prediction equation for lead-free (Sn4.0Ag0.5Cu) bumped WLCSP (wafer level CSP) on lead-free FR-4 PCB with ENIG (electroless nickel-immersion gold) surface finish. FEA simulation based solder joint fatigue life model methodology for both 63Sn37Pb and 95.5Sn4Ag0.5Cu solder alloy has been presented by [Zahn, 2002, 2003, Kim et al. 2003, Schubert et al. 2002]. The effect of underfill on solder strains and susceptibility to delamination in SBGA (Super BGA) was studied [Pyland, et al. 2002] and it was reported that underfill does not always enhance super ball grid arrays.

2.5 Composition of Solder Alloy

Darveaux et.al. [1992] studied various solder compositions, 62Sn36Pb2Ag, 60Sn40Pb, 96.5Sn3.5Ag, 97.5Pb2.5Sn, 95Pb5Sn, in order to determine the effects of grain size and intermetallic compound distribution due to tensile and shear loading with a temperature range between 25°C and 135°C. He observed that the 96.5Sn3.5Ag and 97.5Pb2.5Sn alloys absorbed more strain before the onset of failure than the 60Sn40Pb and 62Sn36Pb2Ag alloys, and that the 95Pb5Sn was the least ductile. He also observed that the thermal cycle simulations indicated that all the alloys tested responded about the same under accelerated test conditions, but the 96.5Sn3.5Ag and 97.5Pb2.5Sn alloys undergo considerably less strain under field use conditions.

Zbrzezny et.al.[2006] studied the effect of different reflow profiles on the reliability of lead-free Sn-3.0 Ag-0.5 Cu (SAC305) ball grid array devices assemble with SnPb eutectic paste. These packages were subjected to 1500 cycles of accelerated thermal cycling with temperature profiles of 0°C to 100°C. The thermo-mechanical testing revealed that assemblies with the mixed alloy, lead-free, assemblies failed much earlier than the SnPb assemblies. It was found that cracks, or fractures, occurred on the board side, between the intermetallic layer and solder. They believe that the interfacial failures resulted from Pb redistribution at the interface and from high tensile stresses that were due to the accelerated thermal cycling.

In the past few years, lead-free solders have received a lot of attention. The National Center for Manufacturing Sciences (NCMS) and the National Electronics Manufacturing Initiative (NEMI) have published multiple year studies on lead free solders. Although it depends strictly on application, there have been many reports of increased solder joint reliability using lead-free solders, such as SnAgCu, instead of the conventional SnPb solders. Bartelo, et. al. [2004] studied the thermo-mechanical fatigue behaviors of Sn-Ag-Cu solder joints in terms of their Ag content, cooling rate, and ATC test condition. This studied showed that 2.1Sn-0.9Ag-0.9Cu solder joints assembled at a slow cooling rate have the best thermal fatigue life over the high silver content joints for the ATC test of 0°C to 100°C with a 120 minute cycle time.

2.6 Objective and Scope of Thesis

In this thesis, risk-management and decision-support models for reliability prediction of BGA packages in harsh environments have been presented. The models presented in this paper provide decision guidance for smart selection of component packaging technologies and perturbing product designs for minimal risk insertion of new packaging technologies. In addition, qualitative parameter interaction effects, which are often ignored in closed-form modeling, have been incorporated in this work. Previous studies have focused on development of modeling tools at sub-scale or component level. The tools are often available only in an offline manner for decision support and risk assessment of advanced technology programs. There is need for a turn key approach, for making trade-offs between geometry and materials and quantitatively evaluating the impact on reliability.

Multivariate linear regression and robust principal components regression methods were used for developing these models. The first approach uses the potentially important variables from stepwise regression, and the second approach uses the principal components obtained from the eigen values and eigen vectors, for model building.

Principal-component models have been included because of their added ability in addressing multi-collinearity.

The statistics models are based on accelerated test data in harsh environments, while failure mechanics models are based on damage mechanics and material constitutive behavior. Statistical models developed in the present work are based on failure data collected from the published literature and extensive accelerated test reliability database in harsh environments, collected by the author at Auburn University. Sensitivity relations for geometry, materials, and architectures based on statistical models, failure mechanics based closed form models, and FEA models have been developed. Validation of statistical, failure mechanics, and FEA based model sensitivities with experimental data have been demonstrated.

The objective of this research is to develop a fundamental understanding of damage initiation and progression in copper-core electronic assemblies constructed with leaded solder interconnects and development of methodologies for predicting thermal reliability, or $N_{1\%}$ values, under thermal cycling loads. The fundamental knowledge will be used for development of predictive models and prognostication techniques. Prognostication refers to the ability to determine residual life in deployed electronics without knowledge of prior stress history. Leading indicators of failure will be developed to determine the probability of impending failure in electronics. The research results have wide applicability in extreme environment electronic applications.

2.7 Thesis Layout

In Chapter 3, the methods for which the experimental data was acquired, cross-sectioned, and set up are discussed. Chapter 4 talks about the failure mechanics based models and the equations used to develop them for PBGA packages. Chapter 5 deals with finite element modeling steps for PBGA packages while Chapter 6 deals with the specific models that were built and analyzed in this research. Chapter 7 shows the development of statistics based closed form models and Chapter 8 validates them.

Chapter 9 deals with life predictions and field life correlations.

CHAPTER 3

EXPERIMENTAL SETUP AND DATA ACQUISITION

This research was conducted for Northrop Grumman in order to develop a fundamental understanding of damage initiation and progression in copper-core electronic assemblies constructed with leaded solder interconnects and development of methodologies for interrogation of material state under thermal-cycling loads. In this chapter, the accelerated thermal cycling experiment will be explained in great detail. The test boards, the thermal chambers and their temperature profiles, the data acquisition system, the cross-sectioning process, and the microscopes used for taking measurements are all explained.

3.1 Test Boards

The test boards were provided by Northrop Grumman and wired up by Auburn University. This experiment utilized 4 sets of 9 copper core test boards each containing electronic packages mounted on the front and rear side of the boards. Figures 3.1-3.6 show the various test boards, CCA073-081, CCA010-018, CCA028-036, and CCA019-027. The test boards used were 254mm x 190.4mm (10in x 7.5in) with various electronic packages on each side. The electronic packages mounted to these test boards were all

BGA's. They contained ceramic ball grid arrays (CBGA), chip array ball grid arrays (CABGA), tape ball grid arrays (TBGA), flex ball grid arrays (FBGA), and primarily PBGA's. The electronic packages ranged from 64 to 900 I/O counts, 0.80 mm to 1.27mm pitch, and package sizes ranging from 5.5mm x 16mm all the way up to 31mm x 31mm.

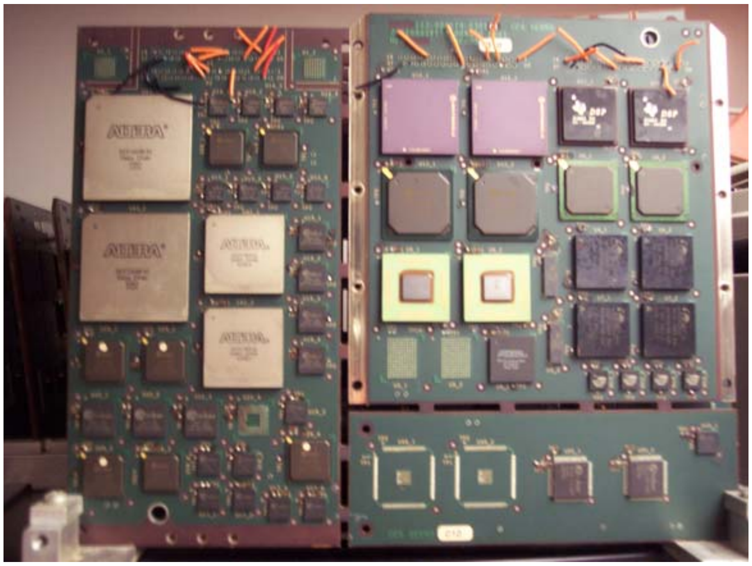


Figure 3.1 Front Side of Test Boards CCA010-018

Figure 3.2 Back Side of Test Boards CCA010-018

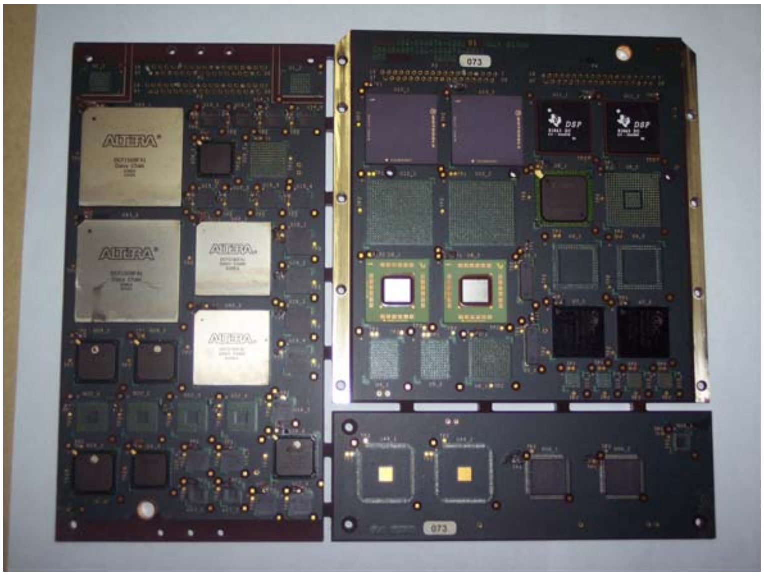


Figure 3.3 Front Side of Test Boards CCA 073-081

Figure 3.4 Back Side of CCA 073-081

Figure 3.5 Front Side of Test Boards CCA 028-036

Figure 3.6 Back Side of Test Boards CCA 028-036

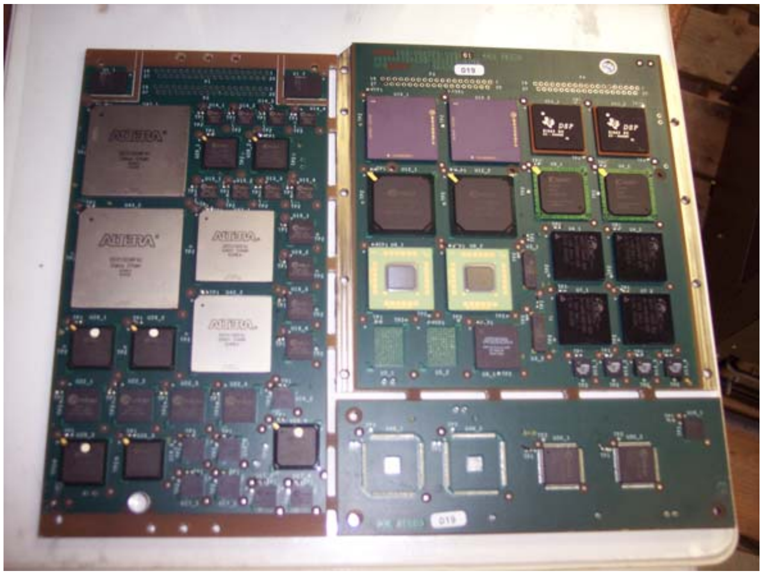


Figure 3.7: Front Side of Test Boards CCA 019-027

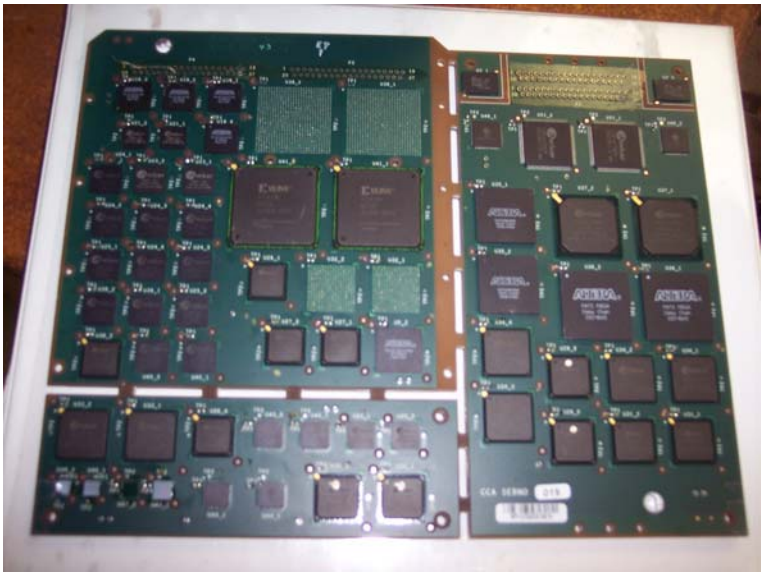


Figure 3.8: Back Side of Test Boards CCA 019-027

3.2 Chamber Profiles

In order for these tests to be carried out, three thermal chambers were used. Each of the three chambers were to be set up with different temperature profiles, -55°C to 125°C (TC2), 3°C to 100°C (TC3), and -20°C to 60°C (TC4). In order to make sure the thermal chambers' profiles were accurate, a thermal profiler was used. The thermal profiler used for all three chambers was the Slim KIC-II Thermal Profiler by KIC Innovations. (see Figure 3.9). Each chamber contained three thermal couples during the profiling. The KIC software allows the user to watch the temperature vs. time plot over the entire thermal cycle.

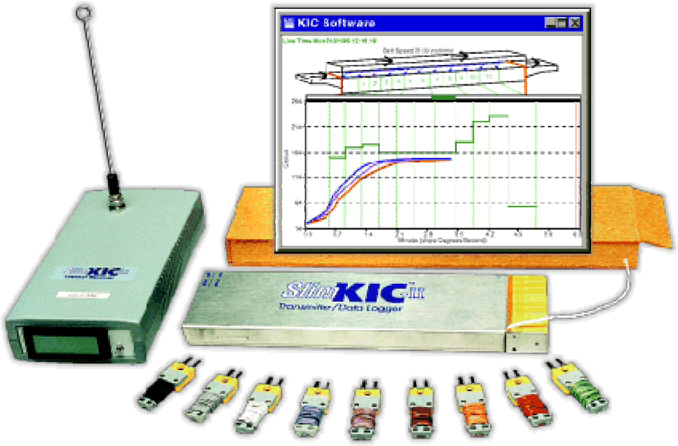


Figure 3.9: Slim KIC-II Thermal Profiler and Software

TC2 Thermal Cycle: The thermal profile shown in figure 3.10 has been used for test boards CCA010-018 and CCA 073-081 in order to experimentally determine solder joint reliability in various electronic packages in harsh environments, -55°C to 125°C. This temperature range is used for military and defense companies and is deemed "harsh environment" for electronic packaging. This cycle starts at room temperature (25°C) and has a 30 minute dwell at the extreme temperatures of -55°C and 125°C and the ramp rate is 3°C/min from the hot extreme to the cold extreme, and 4°C/min. from the cold extreme to the hot. The reason for this difference is that the particular thermal chamber used, Figure 3.11, has a maximum ramp rate of 4°C/min. The total cycle time is 165 minutes.

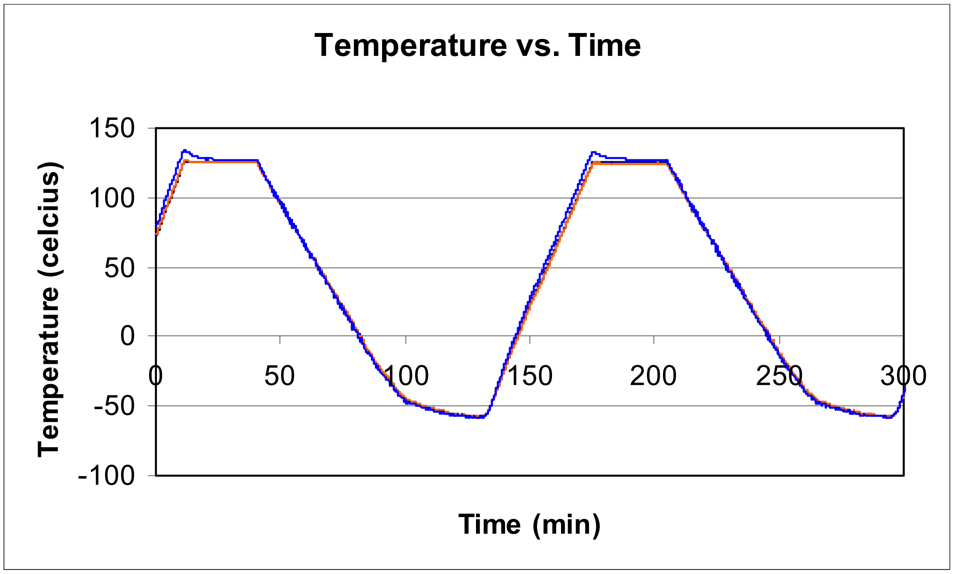


Figure 3.10: TC2 Profile

Figure 3.11: Thermal Chamber used for TC2 Temperature Profile

TC3 Thermal Cycle: The thermal profile shown in figure 3.12 has been used for test boards CCACCA-019-027 in order to experimentally determine solder joint reliability in various electronic packages from 3°C to 100°C. This cycle starts at room temperature (25°C) and has a 30 minute dwell at the temperatures of 3°C and 100°C and the ramp rate is 3.2°C/min from the hot extreme to the cold extreme, and 6.5°C/min. from the cold extreme to the hot. The reason for this difference is that the particular thermal chamber used for TC3 and TC4 is much smaller and can ramp up much faster than the larger chamber used for the TC2 temperature conditions.

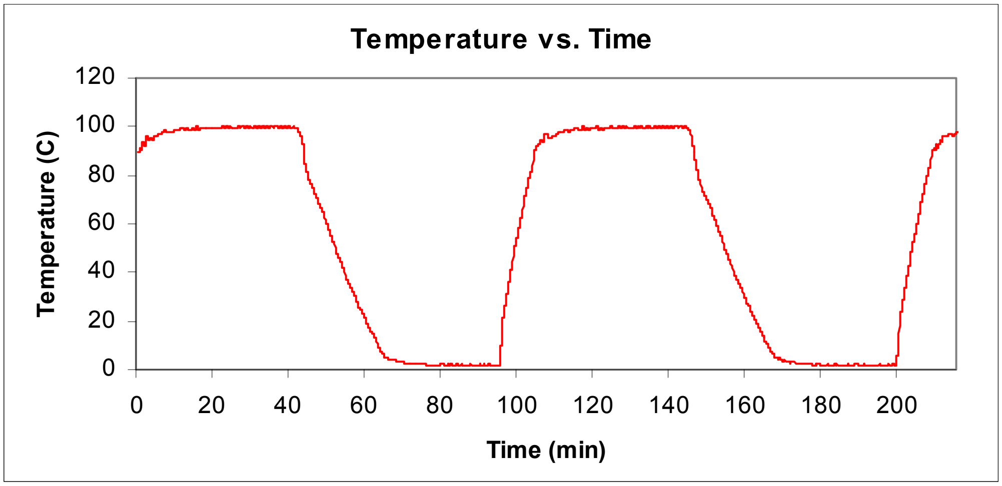


Figure 3.12: TC3 Profile

TC4 Thermal Cycle: The thermal profile shown in figure 3.13 has been used for test boards CCACCA-028-036 in order to experimentally determine solder joint reliability in various electronic packages from -20°C to 60°C. This cycle starts at room temperature (25°C) and has a 30 minute dwell at the temperatures of -20°C and 60°C and the ramp rate is 2.6°C/min from the hot extreme to the cold extreme, and 5.3°C/min. from the cold extreme to the hot.

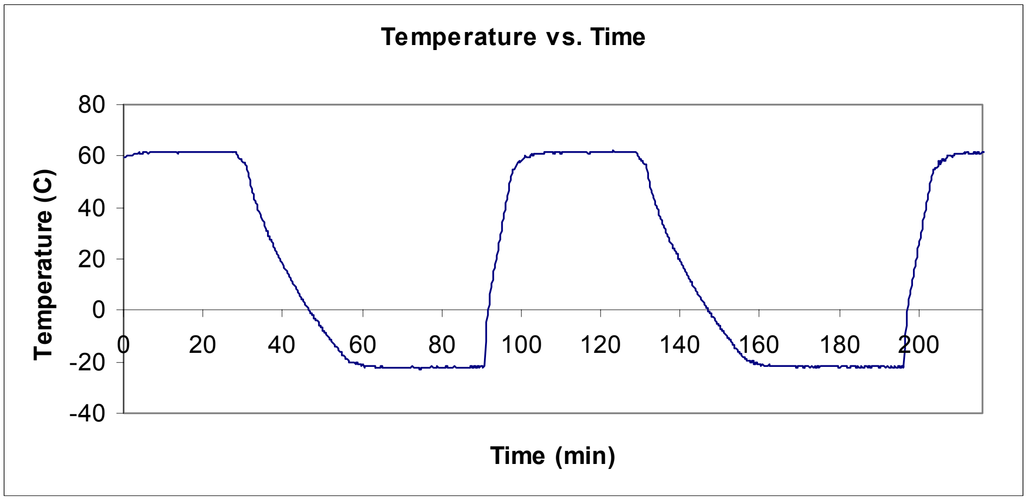


Figure 3.13: TC4 Profile

3.3 Data Acquisition

Setup**:** After each of the chambers have been profiled and set up accordingly, the boards are then placed into their aluminum carriers, as seen in Figure 3.14, which were designed by Northrop Grumman. These carriers allowed each of the test boards to be stood up vertically, as well as maintaining equal distance from each of the other boards.

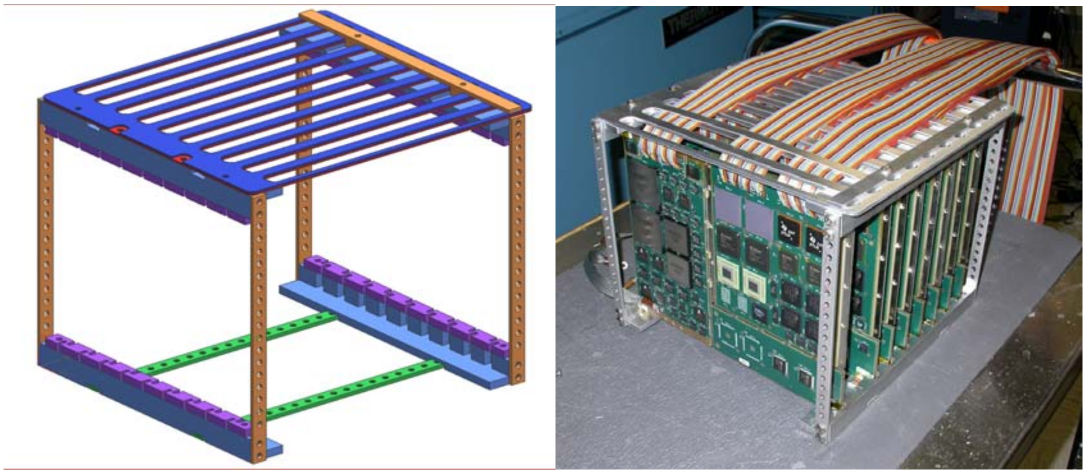


Figure 3.14: Test Board Holders

Once all of the boards are placed into the holders, each test vehicle is then wired up and their corresponding wires are passed through the access holes in the side of the chamber as shown in Figure 3.14. The wires from each of the boards are then wired to an interface board constructed by Auburn University Center for Advanced Vehicle Electronics (CAVE). These interface boards have four 10-pin connectors at the bottom which are for the wires coming directly from the test boards inside the chamber. The single 10-pin connector on the left hand side is for the ground wires. Each test board only requires one ground, however, in order for the interface board to work properly, each pin must have a ground. One ground was run from the test board, and then short wires were used for “jumpers” to connect the remaining pins to a ground. The two holes in the upper left hand corner of the interface boards are for the ceramic resistance temperature detector (RTD). The two small holes on the right hand side of the board are for the multi-meter connections, and the large 96-pin connector in the middle of the interface board is for the ribbon cable which runs to the back of the scan boxes.

Switching Systems: The digital switching system used to monitor the test boards was the Keithley Model 7002 Full Rack Switch Mainframe System, see Figure 3.15. This particular model is capable of high density switching with up to 400 channels per mainframe while using only two switching cards in the CARD1 and CARD2 locations. For the accelerated thermal cycling done in this experiment, two of these switching systems were used with the TC2 temperature cycling.

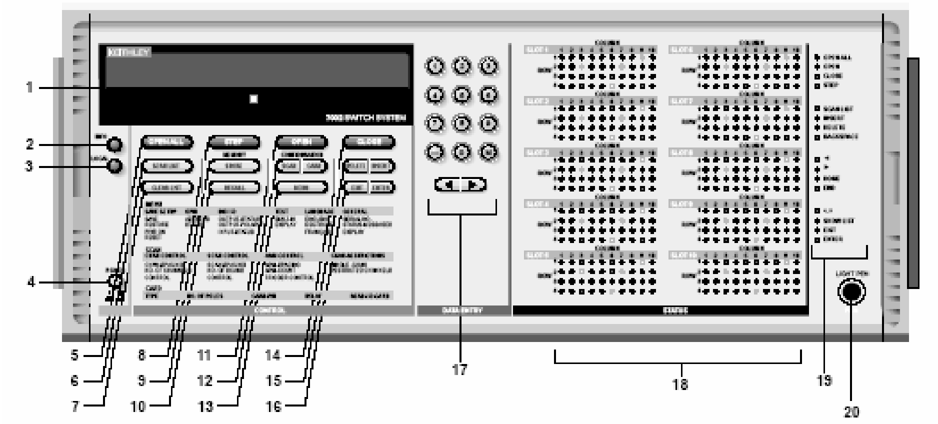


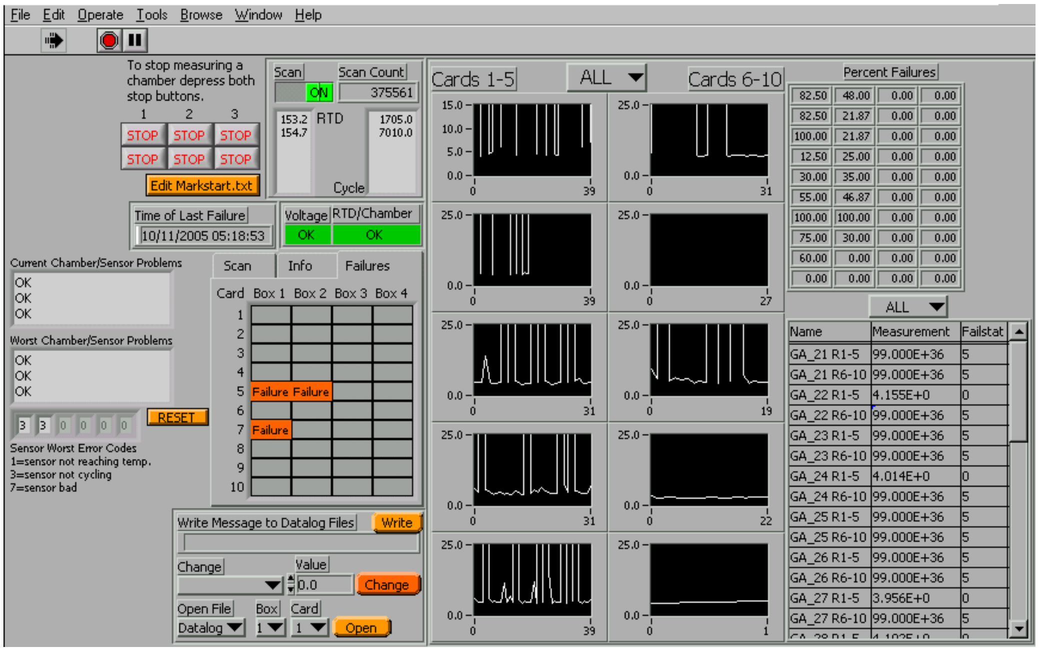
Figure 3.15: Keithley Model 7200 Digital Switching Mainframe

Multimeters: The multimeters used in this experiment were the Keithley Model 2000 61/2-digit Digital Multimeter, Figure 3.16. It combines broad measurement ranges with superior accuracy specifications – DC voltage from 100nV to 1kV (with 0.002% 90-day basic accuracy) and DC resistance from 100μΩ to 100MΩ (with 0.008% 90-day basic accuracy). This multimeter worked in conjunction with two of the digital switching systems above to accurately switch between channels, as seen in Figure 3.16, and record vitally accurate data and results in conjunction with the LabView software and MarkDano file which will be explained next.

Figure 3.16: Keithley 2000 Digital Multimeter

Figure 3.17: Data Acquisition Setup in Dungeon Lab

Software: LabView Data Acquisition Software was the software package used to interface with the digital switching systems, the interface boards, the boards inside the chamber, and the PC. It allows the user to view a live feed of what is actually going on with the boards inside the thermal chambers. Figure 3.18 shows a screen capture of the LabView software while it is running and what the user sees displayed on the screen.



To stop measuring a chamber depress both stop buttons.

Scan: ON

Scan Count: 375561

RTD: 153.2, 154.7

Cycle: 1705.0, 7010.0

Time of Last Failure: 10/11/2005 05:18:53

Voltage: OK

RTD/Chamber: OK

Current Chamber/Sensor Problems:
OK
OK
OK

Worst Chamber/Sensor Problems:
OK
OK
OK

3 3 0 0 0 0

Sensor Worst Error Codes
1=sensor not reaching temp.
3=sensor not cycling
7=sensor bad

Scan | Info | Failures

Card	Box 1	Box 2	Box 3	Box 4
1				
2				
3				
4				
5	Failure	Failure		
6				
7	Failure			
8				
9				
10				

Write Message to Datalog Files

Change

Value: 0.0

Open File: Datalog

Box: 1

Card: 1

Percent Failures

82.50	48.00	0.00	0.00
82.50	21.87	0.00	0.00
100.00	21.87	0.00	0.00
12.50	25.00	0.00	0.00
30.00	35.00	0.00	0.00
55.00	46.87	0.00	0.00
100.00	100.00	0.00	0.00
75.00	30.00	0.00	0.00
60.00	0.00	0.00	0.00
0.00	0.00	0.00	0.00

ALL

Name	Measurement	Failstat
GA_21 R1-5	99.000E+36	5
GA_21 R6-10	99.000E+36	5
GA_22 R1-5	4.155E+0	0
GA_22 R6-10	99.000E+36	5
GA_23 R1-5	99.000E+36	5
GA_23 R6-10	99.000E+36	5
GA_24 R1-5	4.014E+0	0
GA_24 R6-10	99.000E+36	5
GA_25 R1-5	99.000E+36	5
GA_25 R6-10	99.000E+36	5
GA_26 R1-5	99.000E+36	5
GA_26 R6-10	99.000E+36	5
GA_27 R1-5	3.956E+0	0
GA_27 R6-10	99.000E+36	5

Figure 3.18: LabView Software Screen Capture

As seen in the figure above, the Labview software allows the user to interface with the boards inside the chamber. It shows current resistances in each of the ten black and white graphs. Each graph is a live feed of cards 1-5 and 6-10. This allows the user to see the exact resistance values for the particular electronic package that is being monitored. Card 10 shows a straight line, which tells the user that the board still has a steady resistance, hence all solder joints are still in “working” order and have not failed. The orange boxes on the screen shot that have the words “failed” written in them, tell the user if a board has failed. The spreadsheet in the upper right hand corner of the screen shot shows the percentage failure of each individual board. In this screen capture, after 1000 cycles, box 2 card 9, still has 0.0% failure. The software also gives up-to-date temperature readings from the RTD, shows failure that have occurred (shown by the orange flags in the figure), as well as percent failures for each of the cards/channels that are being monitored. In order for this software to run, a program file by the name of MarkDano.llb, must be explained in order to fully understand how this software works and where the resistance values are input in order to result in a failure. Each individual text file within the MarkDano.llb serves as a place to store data while the software is running. It can record things such as time failure occurred and what temperature the chamber was at when it failed, as well as many other parameters set by the user prior to starting the tests.

MarkDano Program File: This file contains two types of files that must be setup in order for the LabView software to record data needed for accelerated thermal cycling tests. First, the configuration files, Markstart.txt, Rlogset.txt, Rtd.txt, Voltage.txt, bBfval.txt, bNameC.txt, must be setup in order for the software to run properly.

Markstart.txt

Example file:

```
1.      Run
2.      c:\Connector_Test
3.      1
4.      1       0       0
5.      5400    0       0
6.      1
7.      0
8.      6.000   4.000
9.      1
10.     TCgrey/Connector      drakejl@eng.auburn.edu
11.     6341
```

Figure 3.19: Markstart.txt File Example

Configuration Files:

Markstart.txt: Figure 3.19 above shows an example code written in a text file and will help understand the following explanation. The markstart.txt file contains information necessary for the measurement software to begin. The file is located in the directory: c:\windows\desktop. A shortcut to the measurement software is placed in the startup folder for Windows so it will start when the computer boots. The first line of this file is “run” if the program is to start making measurements when the computer boots. If the first line contains “networkserver”, the computer starts the e-mail notification and web interface program. Note that the web server built into LabView must be enabled for the status web page to be available. The second line of this file contains the directory in which all other configuration files, except rlogset.txt, are located. This directory is also used to store test data. The third line consists of the scan speed or integration time in NPLC, or number of power line cycles per measurement. When using filters this is automatically reduced, but one is most adequate. The fourth line contains the temperature measurement type to be used for the test. Up to three can be specified and are tab delimited. Values of zero (0) through three (3) are valid and represent in order: no temperature sensors, 2 wire resistance of RTDs, 2 wire resistance of mechanical switches, and temperature in degrees Celsius using 4 wire RTDs with the 2001 multimeter. The mechanical switch option can be used instead of temperature sensors, this looks for a resistance less than 97 Ohms when the chamber is cold and resistance above 125 Ohms when the chamber is hot, but will not give errors if the switch reaches zero or infinite resistance.

The fifth line gives cycle times for each chamber, tab delimited. This is used to determine if the chamber does not cycle in an appropriate amount of time.

The sixth line gives the box number, or switching system number of the temperature sensors (RTD's) and bias voltages. A zero (0) signifies using the 2000-SCAN with the 2001 multimeter, while one (1) through four (4) represent using the first through fourth 7002 switching system. The seventh line is one (1) if one or more bias voltages are to be monitored, and zero (0) otherwise. The eighth line gives the range of values the bias voltage is considered good, with the upper limit followed by a tab and then lower limit. The nineth line determines the type of measurement log to be used, a value of zero (0) will result in every measurement being logged, while a value of one (1) will result in measurements being logged twice per cycle and a value of two (2) will record measurements approximately every 30 minutes. The tenth line specifies a name for the test and chamber. This is used in e-mail notification and web page status to designate different chambers. On the same line with the computer name and separated by a tab is a list of e-mail address to which messages will be sent when errors occur. Multiple e-mail addresses may be separated by a semicolon (;). The eleventh line of this file gives the TCP port on the network server to which this computer will send status packets. This also determines the location of this chamber's status on the web status page, and the file name it will use on the network backup device.

Rlogset.txt

```
1.    1    1    1    1
2.    1    1    1    1
3.    1    1    1    1
4.    1    1    1    1
5.    1    1    1    1
6.    1    1    1    1
7.    1    1    1    1
8.    1    1    1    1
9.    1    1    1    1
10.   1    1    1    1
```

Figure: 3.20: Rlogset.txt File Example

Rlogset.txt: Figure 3.20 above, shows an example of the Rlogset.txt file and will help with the following explanation. This file determines which cards will have a measurement log kept for them. There are four columns, each representing a 7200 switching system, and ten rows, each representing a 7011 card within the 7200 switching system. Columns are tab delimited and rows are carriage return delimited. Each position within the matrix of rows and columns represents a different card which the switching system is capable of measuring, with the first row and fourth column representing the first card in the fourth switching system. The tenth row in the fourth column would likewise represent the tenth card of the fourth switching system. The positions contain a one (1) or zero (0), with a one a measurement log will be kept for that card, with a zero a measurement log will not be kept. When setting up this file it is very important that none of the values are changed, even if only one switchbox is used.

Rtd.txt

```
1.      1       40
2.      2       40
```

Figure 3.21: Rtd.txt Example File

Rtd.txt: The rtd.txt file contains the channel information for the temperature sensors. This information consists of the card number of a temperature sensor followed by a tab and the channel number of the sensor. Two additional values after the channel number are used for 4 wire RTD measurement of real temperature. These values are also tab delimited; the third and fourth values of each line are upper and lower temperature. One sensor is listed on each line with two sensors per chamber. In the case of using the 2000-SCAN with the model 2001 multimeter the card number is ignored and only the channel number is used. All temperature sensors must be on the same 7200 switching system or the 2000-SCAN.

With 4 wire measurement of RTDs, an upper and lower temperature of the test must be given. These will be used to determine when the chamber cycles, the chamber must reach 0.4 multiplied by these values to be counted as a cycle. If the chamber does not reach at least the temperatures given, an error will be generated based on the fact that the chamber is not reaching the desired temperatures. This error as well as the chamber not cycling error will cause front panel notification as well as an e-mail.

Voltage.txt: The channel information for bias voltages to be monitored is placed in this file. This file is formatted similar to rtd.txt file with the card number and channel number. All bias voltage measurements must be on the same 7002 switching system. There is no limit to the number of voltages that can be monitored; however, the number should be limited to an amount which can be scanned in a short length of time. However, since this file is only used for humidity testing, it was not used in this experiment.

bBfval.txt

```
10	2000	80	1
10	2000	80	1
10	2000	80	1
10	2000	80	1
```

Figure 3.22: bBfval.txt File Example

bBfval.txt: Figure 3.22 shows an example of this text file. This file's purpose is to store settings to be used during the measurement scans. One file exists per 7200 switching system used and the name of the file follows the following format: bBfval.txt, where B represents the switching system number, one (1) through four (4). The file contains one line per card, each line contains up to nine elements which are tab delimited. The first element of each line is the upper limit, followed by the optional values: meter range, channels per scan, digital filter, lower limit, meter function, integration time devisor, temperature sensor pair, and close first list. The integration time devisor here is a number by which the integration time is divided for a scan. This can be used to speed the scan speed for a large number of channels.

The channels per scan defaults to 40, but can be set to 80 which allows a consecutive odd and even numbered card with the same scan settings to be scanned together to reduce overall measurement time. Most of the options are optional and the defaults are: 100 ohms for upper failure value 1000 or 2000 ohm meter range (depending on meter used), 40 channels per scan, digital filter off, -Inf for lower failure value, 2 wire ohms meter function, integration time divider of 1, first temperature sensor pair (0 indexed), and no close first list.

bBnameC.txt

```
1.      Board1_1      1
2.      Board1_2      2
3.      Board1_3      3
              .
              .
              .
4.      Board_40      40
```

Figure 3.23: bBnameC.txt File Example

bBnameC.txt: Figure 3.23 should be referenced during this file's explanation. The name file contains channel information and a device specific name for devices to be measured during environmental reliability testing. One file exists for each card to be scanned. The name of the file follows this format: bBnameC.txt, where B is the switching system number, one (1) through four (4) and C represents the card number, one (1) through ten (10). The file contains one line per device to be measured. Each line contains the following tab delimited information: name, channel (40 channels per card, 400 channels per box), upper limit, lower limit, and card. The name is used to identify the devices that fail in the data files.

The channel and card number determine to which channel on a switchbox the device is connected. When the upper and lower limits are present here they are used instead of the values in the failure value file. All but the name and channel information are optional. Empty lines should be removed from the bottom of this file.

Data Files:

Count Files: The count files are used to store the current cycle count when the measurement system is monitoring thermal cycling chambers. There are two files containing the cycle count, counta.txt and countb.txt in the /count subdirectory. Each file contains the cycle count for one temperature sensor per chamber. The files contain one number per line and are created automatically to start at cycle zero by the measurement software.

In addition to the cycle count files there is a scan count file in the same directory. This file, scount.txt, contains the total number of scans performed by the measurement software. The scan count file is used for the watchdog function and can also be used as a sorting index for data files.

Failure Status Files: The failure status files contain the number of times each device has been outside the allowable range. One of these files is kept for each card being measured, and all are located in the /failstat subdirectory. The name of these files has the format bBfailC.txt, where B represents the switching system number and C represents the card number. The files contain many lines of numbers, with each number representing the number of times a device has been outside the allowed range.

When the number reaches five the device is considered to have failed and a record is written to the data file. These numbers do not exceed five after a device has failed, but will remain unchanged unless reset by users.

Data Files: Data files contain records of failures, with one file for each card. These files are located in the /datalog subdirectory and their names follow the format bBdataC.txt, where B represents the switching system number and C represents the card number. These files contain the device names, times, dates, cycle numbers and values at which devices fail.

Log Files: The measurement log files can periodically save measurements of all devices. These files are also in the /datalog subdirectory and have the filename format bBlogC.txt, where B represents the switching system number and C represents the card number. Although the log files do not contain the most important data recorded throughout the test, they can be referenced for events that affect all devices being monitored. When the log files are set to save measurements twice every cycle they will stop saving measurements when the environmental simulation chamber stops cycling, this giving an estimate of the time which the chamber stopped [Mitchell 2006].

3.4 Cross-Sectioning

Various electronic packages needed to be cross-sectioned before the accelerated thermal cycling tests were started, for package measurements, as well as after the ATC tests in order to see crack initiation as well as failures due to cracking in the solder balls. The entire cross-sectioning and polishing process contains five steps: underfill the electronic package, coating the plastic containers, cutting/cross-sectioning the package, pouring/mixing the epoxy resin, and polishing/buffing the sample for measurements.

Step I: Underfill the Electronic Package: The current underfill that has been used is the CSPM 12J00 or Cookson SC3080. This chemical must be stored in a refrigerator and in order to use it, the underfill must thaw for approximately thirty minutes. In order for it to become viscous and flow underneath the electronic packages, it must then be heated to 110°C. After heating the underfill, a suitable syringe is used to dispense the underfill on the desired electronic component. For BGAs, the underfill is dispensed in one corner of the package and it will disperse throughout the solder balls. After the underfill is allowed to flow underneath the package and through all the solder balls, it then needs to be baked at 165°C for 20-25 minutes.

Step II: Cutting the Electronic Package: Before cutting the test board and package needed for cross-sectioning, a fine-tipped permanent marker is used to mark the area of interest of the electronic package. An example of how the package is marked up before cutting is shown in Figure 3.24. This picture shows a previous student's PCB with

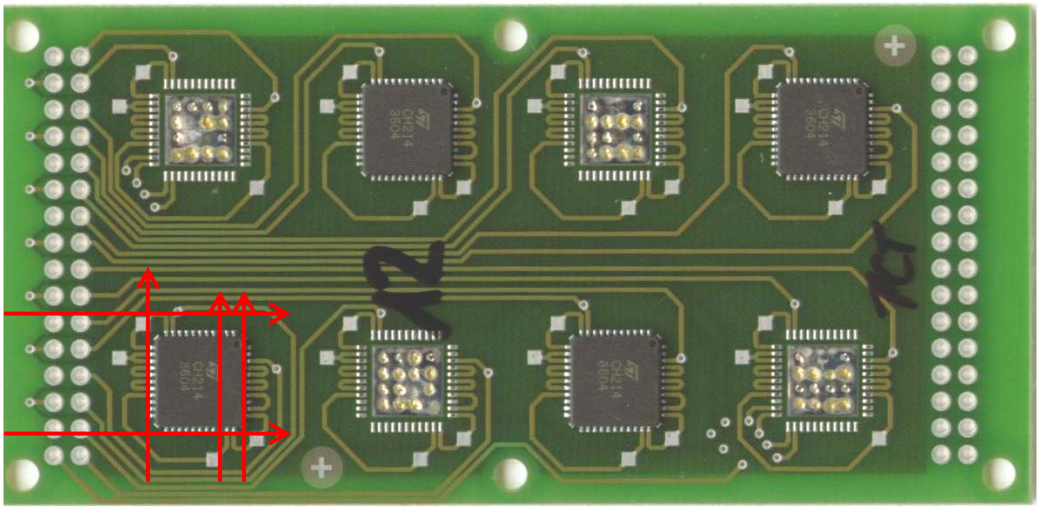


Figure 3.24 Test Board Ready for Cross-Sectioning

various quad flat packages (QFP's), with one package marked up and ready for cutting. Before cutting the test board, coolant must be added to the saw's reservoir. The coolant is mixed with a 1:9 ratio 1 part coolant and 9 parts water. In order for the saw to cut without overheating and warping the blade, 3/8 of the saw blade must be submerged into the coolant solution. Once the cutting scheme has been determined, and the coolant is added, the Isomet 1000 wet saw, Figure 3.25, can be powered up and the cutting blade can be set at ~250rpm in order to dress the cutting blade and prepare it for cutting. Next, the cutting speed is lowered to 200rpm, depending on the board and package type, and the cutting scheme is followed. Once finished, the cross-sections are labeled set aside for the next step.

Figure 3.25: Isomet 1000 Wet Saw

Figure 3.26: Various Chemicals and Tools used for Cross-Sectioning

<u>Step III</u>: <u>Coating the Plastic Holders</u>: After the packages are cross-sectioned, they are placed in the blue cylindrical plastic holders as seen in Figure 3.26. A silicon release agent, Buehler Release Agent, must then be applied liberally to the inside of these holders and allowed to dry for approximately five minutes. This release agent is applied so that

once the epoxy hardens and “sets up,” the sample can be easily removed form the container.

<u>Step IV</u>: <u>Mixing and Pouring the Epoxy Resin</u>: First each cross section must have a clip, Sampl-Klip, placed on it. This keeps the cross-section in place and in the desired position while the epoxy is poured over it. The area of interest is placed face down (flush) in the blue holder. The epoxy resin in mixed in a cup with a ratio of 2:1. This mix must be exact 100 parts resin to 50 parts hardener, or it will not set up and will yield a soft, flexible cross-section which can not be polished. In order to be precise, the resin and hardener are measured on a scale, then mixed together. To keep air bubbles from forming, the resin and hardener are both poured over and angled tongue depressor and then mixed. The two chemicals are mixed very slowly and when they are thoroughly mixed, the mixture should turn clear. Once mixed, the epoxy is poured onto the samples with a very fine stream until the samples are completely covered. The samples are then labeled and left to sit for 24 hours at room temperature for hardening.

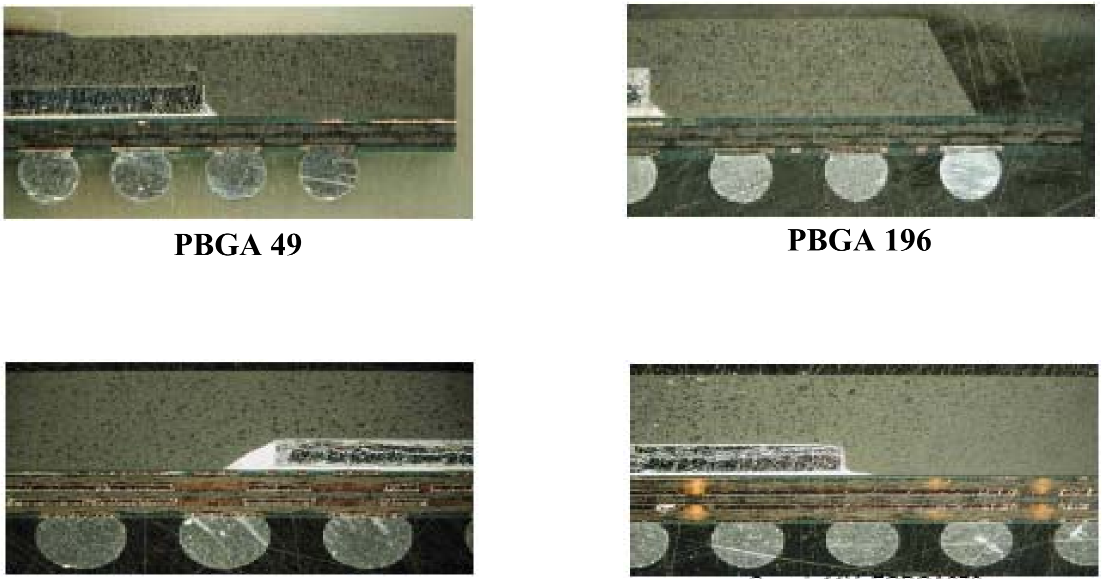
Step V: Polishing the Cross-Sections: After the samples have hardened, they are pushed out of their containers and ready for polishing as seen in Figure 3.27.

Figure 3.27: Cross-Sectioning Samples and Polisher

Once the samples are removed, they are taken over to the Ecomet 6 surface grinder/polisher for polishing, Figure 3.27. Buffing and polishing the samples is a very long and tedious procedure. Various grits of sand paper are grouped into two groups for sanding and buffing. Group 1 corresponds to grits 120-400, and group two corresponds to grits 600-1200. The first group is used to remove the bulk of the material until the solder balls become visible. The second group is sued to fine tune the solder balls and reduce the appearance of scratches from the epoxy. Water is continuously flowing onto the polishing wheels while sanding takes place. The wheels are set between 150-200 rpm for this procedure. Moderate pressure is applied to the sample on the spinning wheel and it is moved back and forth for 3-5 seconds. Then the sample is rotated 90° and placed back on the spinning wheel. This is done for each of the grits of sand paper used in group one and two. Once this is completed, the water is turned off, and the sample is lifted off, ran under water, and then blasted with a few shots of compressed air to remove any particle. It can not be wiped with a towel, as this could scratch the sample.

When all the grinding is finished, the polishing wheel is installed and a small bead of the 3-micron alumina diamond paste is spread onto the wheel and the extender is sprayed onto the wheel as well. The wheel is turned on to 150 rpm and with moderate pressure, the sample is pressed onto the polishing wheel and moved back and forth for 3-5 seconds, then lifted and rotated 90º and placed back onto the polisher. The progress of the buffing is checked by placing the sample underneath a microscope and checking for visible scratches. The more the cross-section is polished, the scratches will begin to fade and the image will become sharper.

After the diamond paste has been used to reduce the scratches, another polishing disc is placed onto the polishing wheel and the .05 micron masterprep solution is used. The polishing wheel is set to 100 rpm this time and the same method as stated previously is used to polish the sample to a crystal clear finish. Once this step is complete, the cross-section is ready for taking measurements of the various layers of the electronic package. Various cross-sections, like the ones shown in figure 3.28, are used for taking package dimensions [Mitchell 2006].



PBGA 49

PBGA 196

PBGA 728

PBGA 676

Figure 3.28: Various cross-sections used for package dimensions

CHAPTER 4

FAILURE MECHANICS BASED MODELS FOR PBGA PACKAGES

Some literatures refer to failure mechanics as mathematical or analytical models. Failure mechanics based models are based on the strength of materials analysis for a given package configuration with known geometry and material properties. The package life is considered to be a function of the damage due to the inelastic strain energy that a solder joint interconnect accumulates while the device undergoes thermal cycling. The accumulation of the inelastic strain energy initiates a crack in the solder joint and this crack propagates with the accumulation of the inelastic strain energy as the component keeps on undergoing thermal cycling. The component finally fails when either the solder joint cracks completely or when the crack is sufficient enough to prevent the flow of required current through the solder joint interconnection. The inelastic strain energy accumulated per unit volume per cycle, also referred to as inelastic strain energy density (ISED), is given by the area enclosed within the hysteresis loop of the solder joint. The inelastic strain energy density calculation for any given package depends on various factors such as: the geometry and architecture of the package, material properties, assembly stiffness, local and global thermal mismatch, hysteresis loop approximation methodology, creep and other material constitutive relations.

4.1 Failure Mechanics Methodology

Figure 4.1 shows a flow chart which describes the main steps involved in the formulation and application of failure mechanics based models. In the first step, the maximum shear strain in the solder joint is determined which is required as an initial guesstimate for initializing the hysteresis loop iteration. The second step involves hysteresis loop determination for both local and global thermal mismatch using various material constitutive relations. Once the hysteresis loops are determined for both of these cases then in the next step inelastic strain energy is calculated from the area enclosed within the loops. After all this has been done, the sum of the inelastic strain energy density due to both local and global thermal mismatch is used in the damage relationship for calculating, predicting, the characteristic life of the package.

4.2 Calculating Maximum Shear Strain

The maximum shear strain in the solder joint can be calculated by the simplified distance to neutral point, DNP, formula. The DNP formula is based on several assumptions due to which it gives the upper bound of the maximum shear strain value. Since the maximum shear strain value is used as the primary input for initiating the hysteresis loop iteration, in order to determine the hysteresis loop for both local and global mismatch, the accuracy of the hysteresis loop is significantly impacted by the initial input of the maximum shear strain value.

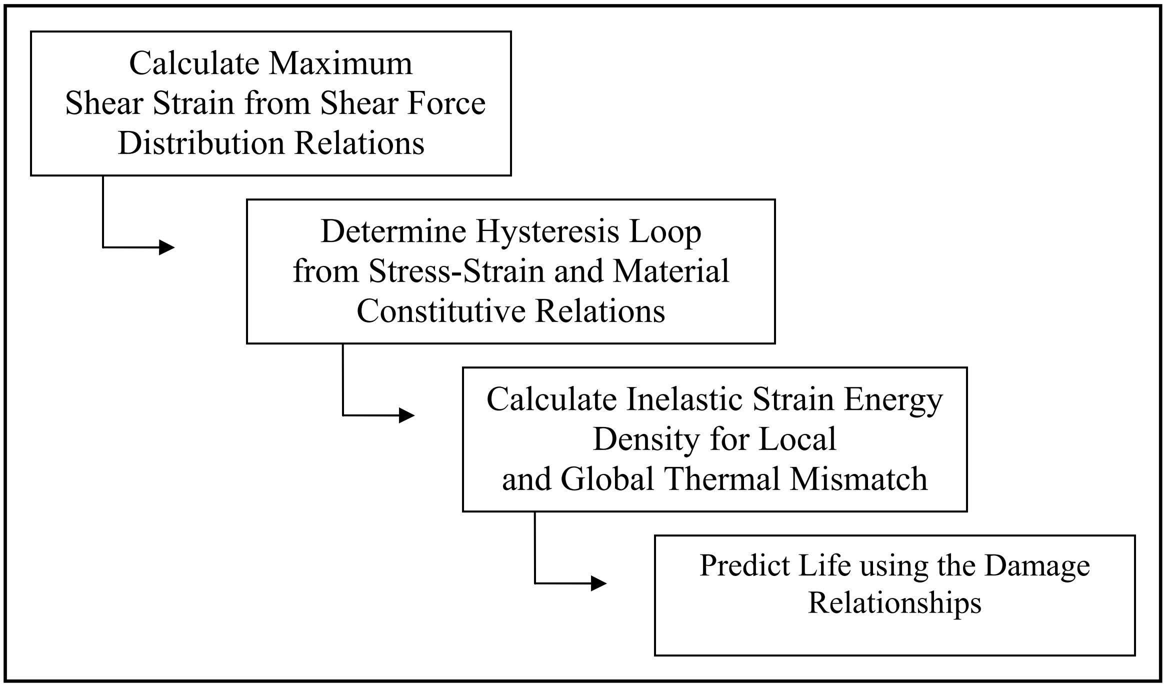


Figure 4.1: Flow Chart of the Methodology behind failure mechanics based modeling

In the case of area array packages, the shear forces generated due to the thermal mismatch during thermal cycling of the component is shared by all the solder joints so the DNP formula, which does not consider the shear force distribution among the solder joints, gives a highly unrealistic value. Vandevelde, et al. [1998] proposed an analytical thermo-mechanical model to calculate thermally induced shear force in the solder balls of an area array package. In this research, Vandevelde's [1998] approach has been used to determine γ_{max} instead of the DNP formula. Since the shear force distribution among all the solder balls for different area array configurations is taken into account in this methodology so it gives a better estimate of the γ_{max} than the DNP formula. The shear force experienced by the solder balls in an area array with 2n x 2n balls can be calculated by solving a set of n linear equations from (4.1) for i = 1 to n [Vandevelde, et al. 1998].

$$(\alpha_b - \alpha_c)(\Delta T)(P)(i) = \left\{ (\phi) \sum_{k=1}^{i} \sum_{q=k}^{n} F(q) \cdot (P) \right\} + F(i) \cdot \chi \qquad (4.1)$$

where

F(i) is the shear force due to thermal mismatch in the i_{th} solder joint from the center [Vandevelde, et al. 1998].

$$\varphi = \frac{\left(\frac{h_c}{2} + h_s + \frac{h_b}{2} \right)^2}{E_C I_C + E_b I_b} + \frac{1}{E_C I_C} + \frac{1}{E_b I_b} \qquad (4.2)$$

$$\chi = \frac{h_c}{6 G_c P b_c} + \frac{h_b}{6 G_b P b_c} + \frac{h_s}{A_s G_s} + \frac{h_s^3}{12 E_s I_s} \qquad (4.3)$$

The shear strain is then calculated for the ball with the maximum value of shear force F(i) using Equation (4.2) [Vandevelde, et al. 1998].

$$\gamma_{\max} = \frac{2(1+\upsilon_s)F_{\max}(i)}{E_x A_s} \tag{4.4}$$

4.3 Hysteresis Loop

To calculuate the hysteresis loop, the thermal cycle must be divided into 4 sections:

1. Ramp up from low temperature to high temperature
2. Dwell at high temperature
3. Ramp down from high temperature to low temperature
4. Dwell at low temperature

The solder joint response during the temperature ramps is approximated by a time independent plastic deformation relation (4.5) [Knecht and Fox 1991].

$$\gamma_B - \gamma_A = \left(\frac{\tau_B}{\tau_p}\right)^2 \tag{4.5}$$

where

subscript A denotes the condition before ramp, B denotes condition after ramp and τ_p is the plasticity parameter obtained from linear curve fitting of data in [Knecht, et al. 1991]:

$$\tau_p(\text{MPa}) = 50588.5\text{-}300.23{*}T(°\text{C}) \tag{4.6}$$

The constitutive relation (4.6) given by Hall [1991] has been used for stress relaxation during the dwell period. The creep relation (4.8) given by Wong [1988] has been used for time and temperature dependent creep during the dwell period.

$$\gamma + \frac{\tau}{\kappa} = \gamma_{\max} \qquad (4.7)$$

$$\overset{o}{\gamma}_{\text{creep}} = A(T)\tau^3 \qquad (4.8)$$

where

$$\kappa = \frac{(K \times h_s)}{A_s} \qquad (4.9)$$

K is the effective assembly stiffness calculated from the formulation given by Hall[1984] for both global and local thermal mismatch creep $\overset{\circ}{\gamma}_{creep}$ is strain rate or the time derivative of creep strain A(T) is temperature dependent factor derived from the data by Wong [1988] and is given by:

$$A(T) = 7.298 \times 10^{13} \left(\frac{1}{E^3(T)} \right) \times e^{\frac{-5412}{T(K)}} \qquad (4.10)$$

where

E(T) is the temperature dependent Young's modulus of the eutectic tin-lead solder.

The first iteration is started with initial value of shear strain, $\gamma_A = \gamma_{max}/2$ and zero shear stress. The iteration is continued each time starting with the shear strain equal to the mean of residual strain, γ_F, and γ_A, of the previous iteration. The loop is stabilized and closed when the point residual strain overlaps the initial strain, which means that the value of γ_F lies in the vicinity of γ_A. The loop closure is defined by the parameter %e, given by Equation (4.11), and the loop is considered to be closed and stabilized when %e is equal to or less than 1%.

$$\%e = \frac{|\gamma_A - \gamma_F|}{\gamma_D - \gamma_A} \times 100 \tag{4.11}$$

4.4 Calculating Inelastic Strain Energy Density

The hysteresis loop is determined for both the global and local thermal mismatch separately using the procedure discussed in section 4.3. Once the stabilized loops are determined than the area enclosed within the loops, which represents the amount of inelastic strain energy density accumulated by the solder joint during one complete thermal cycle, is determined using the trapezoidal rule in Calculus. According to the trapezoidal rule, the area under any curve given by a function f(x), as shown in the Figure 4.2, can be approximated as the summation of the ‘n’ trapezoids used to divide the area, [Suli, et al. 2003] (change to my Calculus Book)

$$\int_a^b f(x)dx \approx \sum_{i=1}^{n} \frac{h}{2}\big(f(a+(i-1)h\big) + f(a+ih) \tag{4.12}$$

The total inelastic strain energy per unit volume per cycle (ΔW) is given by the sum of the inelastic strain energy density per cycle due to global thermal mismatch (ΔW_G) and due to local thermal mismatch (ΔW_L) [Clech 1996].

$$\Delta W = \Delta W_G + \Delta W_L \tag{4.12}$$

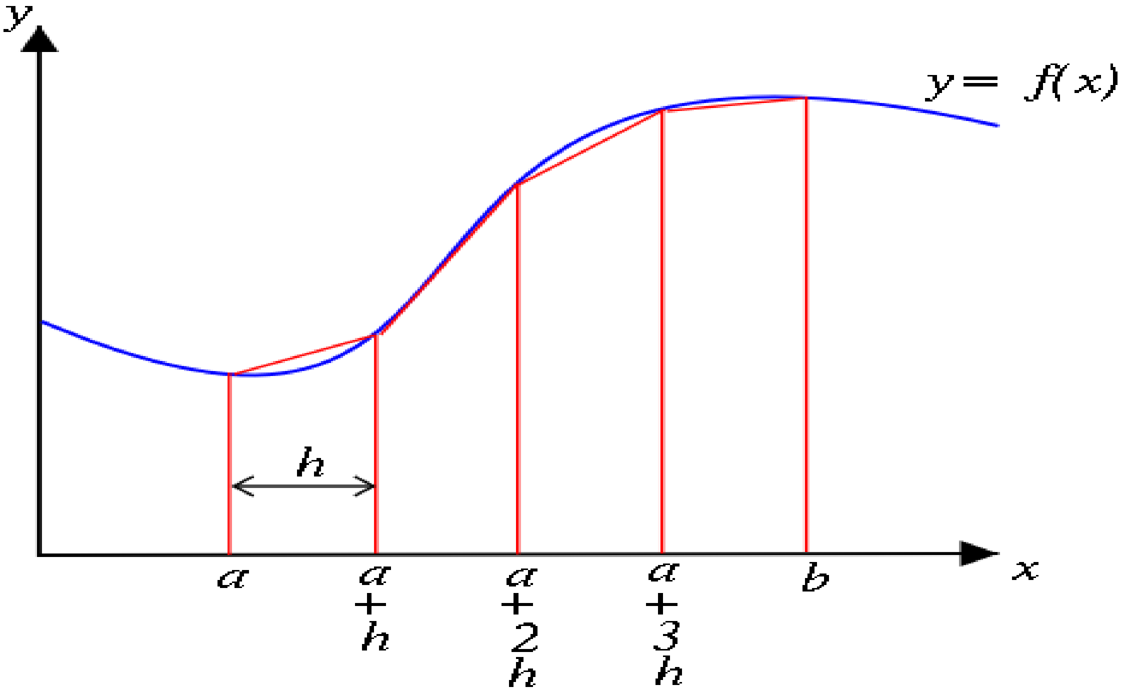


Figure 4.2: Example of calculating the area under a curve using the Trapezoidal Rule

CHAPTER 5

FEM ANALYSIS OF PBGA PACKAGES

In the past, FEM (Finite Element Method) has been widely used for the reliability assessment and analysis of the various electronic components in the electronic packaging industry. Several modeling methodologies have been developed and used over the period of time [Lindley 1995], each having its own merits and demerits. Both 2-D (two dimensional) and 3-D (three dimensional) models have been used for the analysis. Usually 3-D models have been shown to give better accuracy and more realistic results as compared to the

2-D models. Depending upon the geometric and material symmetry of the actual package different configurations of 3-D models like full-scale models 1/4th or 1/8th symmetry models and diagonal slice models [Syed 1996] and [Darveaux 1996]. Use of 3-D diagonal slice model configuration is preferred over the other configurations for the fully symmetric packages due to its computational efficiency and ability to capture true boundary conditions. In the present study, 3-D diagonal slice models have been used for all of the FEA purposes. Various other parameters such as material non-linearity, element type, shape and size also affect the simulation accuracy. The finite element models used in the current work have been checked for their element shapes (aspect ratio and angles) and a finer mesh in the region of solder bump has been employed for better accuracy. In order to capture the true nature of solder bump, time and temperature dependent non-linear constitutive models have been employed for the simulation.

Exhaustive research has been done on the solder joint reliability of various electronic packages subjected to thermal cycling. It has been established by many researchers that the fatigue life of the solder interconnect is dependent on the amount of inelastic strain energy density (ISED) accumulated by the solder joint during each thermal cycle. A correlation between the solder joint reliability and the ISED output from FEA has also been developed in the past for both leaded [Gustafsson 2000] and lead-free [Clech 1996] interconnects. The ISED calculations done from the simulations run for different configuration and various thermal cycles have been used in the current work for the solder joint reliability prediction using the life prediction correlations.

In the current work, 3-D diagonal slice models for various plastic ball grid array packages have been developed. Both linear and non-linear material properties have been used for analyzing the effect of various parametric variations on the reliability of the package. The parametric variations include both design parameters (geometry and material) and the thermal cycling parameters. The failure mode analyzed for the relative comparison of reliability due to the various parametric variations is solder joint failure. Failure modes such as silicon die cracking and delamination have not been analyzed in the present study.

5.1 Model Description

3-D diagonal slice models incorporated with time and temperature dependent non-linear and linear material properties have been developed in ANSYS^{TM}. Four different geometries have been modeled and simulation has been run using various temperature cycles TC1 (-40 to 95°C), TC2 (-55 to 125°C), TC3 (3 to 100°C), and TC4 (-20 to 60°C).

5.2 Geometry

The variations in the geometry considered in the FEA analysis include: die size, die thickness, solder joint height, solder joint diameter, mold compound, pitch, ball count, substrate thickness, die attach layer, copper pad diameter and thickness, package thickness, and package margin. The exact geometric dimensions for the model construction were either provided by the Northrop Grumman or were measured from the cross-sectioning images of the plastic ball grid arrays at Auburn University's Center for Advance Vehicle Electronics (CAVE). The dimensions of the fixed parameters are given in the Table 5.1 and the dimensions of variable parameters will be given in each individual PBGA's modeling section. The packages that were modeled, with numbers corresponding to ball count (I/O count), and used for life predictions are PBGA 49, PBGA196, PBGA 256, PBGA 676, and PBGA 728. PBGA 728 was an early prototype model used to determine the amount of dwell time, whether 20 minute or 30 minute dwells were to be used for this research. However, it was also used for life prediction analysis as will be shown later.

Table 5.1: Dimensions of fixed parameters used for the finite element models

Parameter	Dimension (mm)
Top Layer (FR-4) Thickness	1.397
Cu Core Thickness	1.143
Bottom Layer (FR-4) Thickness	1.397
Total PCB Thickness	3.937

5.3 Modeling Elements

All FEA models have been map meshed using brick shaped 8 noded hexahedral isoparameteric elements (Figure 5.1). Since the 8 noded hexahedral element provides higher accuracy as compared to the tetrahedral elements so the hexahedral elements have been used for meshing the entire model. 2x2x2 Gaussian quadrature integration option has been used for the solution.

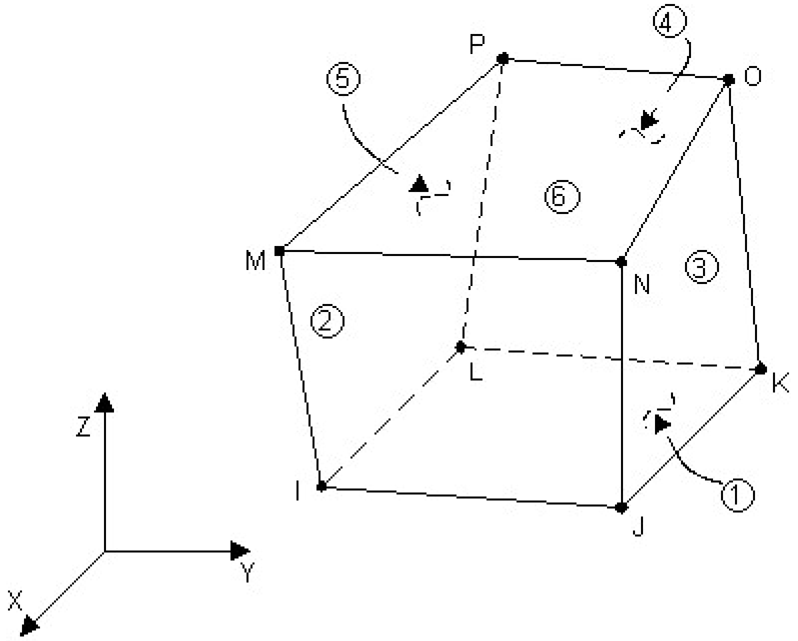


Figure 5.1: Eight-noded hexahedral isoparametric element [ANSYS^{TM}]

VISCO107 elements have been used for the solder bump and SOLID45 elements for all other materials. VISCO107 was used because it has rate-dependent large strain plasticity capabilities and is used to represent non-linear behavior of visco-plastic materials. Another advantage of using VISCO107 for solder is to facilitate the constitutive modeling of the solder material using Anand's model. The SOLID45 element in ANSYS^{TM} also has large strain capabilities.

5.4 Mesh and Boundary Conditions

Figure 5.2 shows a schematic of the boundary conditions that are applied, in this case PBGA49, to all FEM slice models used in this research. It shows that the displacement in the x-direction is zero, UX=0, on all -X slice plane surfaces. Displacement in the z-direction equals zero, and the displacement UY=0 on all +y symmetry plane surfaces. It also shows that there are two couples applied to each slice model. UY is coupled on all –Y slice plane surfaces, and UX is coupled on the PCB only for the +X vertical surface. The boundary conditions have been applied on the nodes. The coupled boundary condition applied on the symmetry plane implies that the nodes on that surface are constrained to remain coplanar. One node on the bottom left corner of the model has been fully constrained in order to prevent the rigid body motion.

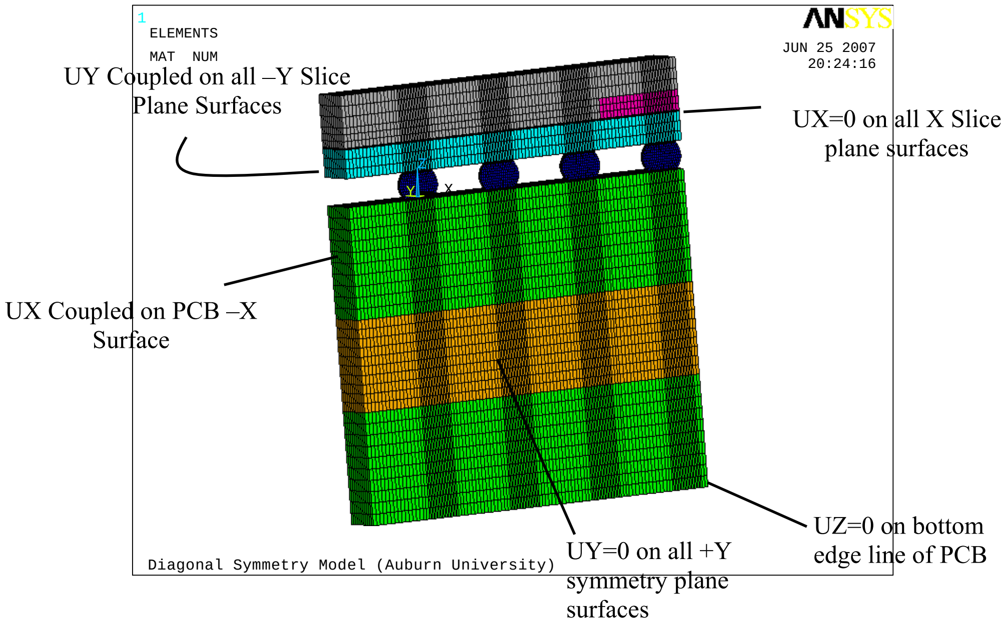


Figure 5.2: Schematic of boundary conditions applied to PBGA49 slice model for simulations.

5.5 Material Properties

Linear Material Properties

Linear isotropic material properties have been assigned to all the elements except for the solder bump elements. The solder bump elements have been modeled with both linear and non-linear constitutive relations. The linear isotropic material properties assigned in the model have been listed in the Table 5.2. The non-linear constitutive relations for the solder bump will be discussed in the next section.

Non-Linear Material Properties

Solder alloy is a viscoplastic material which means that it exhibits both time dependent creep and plasticity. Thus it is essential to use time and temperature dependent non-linear material model for the solder bump. Widely used and established Anand's model which is also a standard feature in ANSYS^{TM} has been used to model both eutectic (62Sn36Pb2Ag) [Darveaux et. al 2000] and lead-free [Amagai, et. al. 2002], SAC305, solder material. In the Anand's model both creep and plasticity have been coupled together with the help of flow and evolutionary equations [Brown 1989]:

Flow equation
$$\frac{d\varepsilon_p}{dt} = A(\sinh(\varsigma\sigma / s_o)^{\frac{1}{m}} \exp\left(\frac{-Q}{kT}\right)$$

Evolutionary equation $$\frac{ds_o}{dt} = \left\{ h_o (|B|)^a \frac{B}{|B|} \right\} \frac{d\varepsilon_p}{dt}$$

where $$B = 1 - \frac{s_o}{s^*}$$

$$s^* = s^{\wedge} \left[\frac{d\varepsilon_p / dt}{A} \exp\left(\frac{Q}{kT} \right) \right]^n$$

The constants of the Anand's model for the simulation have been assigned through the standard input for VISCO107 element in ANSYS^{TM}. The value of the constants used for modeling both the eutectic and lead-free solder material have been listed in the Tables 5.3 and Table 5.4.

Table 5.2: Linear isotropic material properties

Material Properties				
	E (Mpa)	**Poisson's Ratio**	**CTE (1/K)**	**G (Mpa)**
Copper Pad	128932	0.34	16.3E-6	
Solder Mask	3100	0.3	30.0E-6	
BT Substrate	17890 (XY)	0.39 (XZ & YZ)	12.4E-6 (XY)	8061 (XY)
	7846 (Z)	0.11 (XY)	57.0E-6 (Z)	2822 (YZ & XZ)
Die Adhesive	6769	0.35	52E-6	
Silicon Die	162716	0.28	2.54E-06	
Ceramic	37000	0.22	7.40E-06	
Mold Compound	23520	0.3	15E-6	
PCB	27924-37T (XY)	0.39 (XZ & YZ)	14.5E-6 (XY)	12600-16.7T (XY)
	12204-16T (Z)	0.11 (XY)	67.2E-6 (Z)	5500-7.3T (YZ & XZ)

Table 5.3: Values of the constants of Anand's viscoplastic model for Eutectic 63Sn36Pb2Ag Solder [Darveaux 1996, 2000]

Parameter	**Value**	**Definition**
S_o (MPa)	12.41	Initial Value of Deformation Resistance
Q/k (1/K)	9400	Activation Energy / Boltzmann's Constant
A (1/sec)	4.00E+06	Pre-Exponential Factor
ξ	1.5	Multiplier of Stress
M	0.303	Strain Rate Sensitivity of Stress
h_o (MPa)	1378.95	Hardening Constant
s^ (MPa)	13.79	Coefficient of Deformation Resistance Saturation Value
N	0.07	Strain Rate Sensitivity of Saturation Value
A	1.3	Strain Rate Sensistivity of Hardening

Table 5.4: Values of the constants of Anand's viscoplastic model for Sn3Ag0.5Cu – Lead Free Solder [Chang 2006]

Parameter	**Value**	**Definition**
S_o (MPa)	45.9	Initial Value of Deformation Resistance
Q/k (1/K)	7460	Activation Energy / Boltzmann's Constant
A (1/sec)	5.87E+06	Pre-Exponential Factor
ξ	2.00	Multiplier of Stress
m	0.0942	Strain Rate Sensitivity of Stress
h_o (MPa)	9350	Hardening Constant
s^ (MPa)	58.3	Coefficient of Deformation Resistance Saturation Value
n	0.015	Strain Rate Sensitivity of Saturation Value
a	1.50	Strain Rate Sensistivity of Hardening

5.6 Inelastic Strain Energy Density

Several researchers have established inelastic strain energy density (ISED) to be the damage proxy for solder joint thermo-mechanical reliability of electronic packages. Damage relationships correlating the solder joint life with the ISED accumulated per thermal cycle by the solder joint have also been developed. These relationships can be used for the life prediction of the electronic packages with solder joint cracking as the failure mode. The ISED can be calculated from the simulation. In ANSYS™, VISCO107 element has plastic work (PLWK) as a standard output, ISED has been calculated in the present study by volume averaging PLWK over the few layers in the vicinity of the interface. Plastic work accumulated in the solder joint over the complete thermal cycle has been found to be stabilized after the first cycle. Consequently the simulation is run for only two cycles and the ISED is calculated based on the plastic work accumulated during the second thermal cycle. ISED for the solder joint is given by:

$$\Delta W_i (\text{ISED}) = \frac{\left(\sum_{n=1}^{\text{total\_elements}} \Delta W^{(n)} \times V_n \right)}{\left(\sum_{n=1}^{\text{total\_elements}} V_n \right)}$$

where $\Delta W^{(n)}$ is plastic work accumulated by nth element during the second thermal cycle of the simulation and it is standard output in ANSYS™ for VISCO107 element in form of PLWK and V_n volume of the nth element.

5.7 Using Damage Relationships to Predict Life and Package Reliability

The damage relationship relates the characteristic life of the component in terms of number of thermal cycles to the total inelastic strain energy density per cycle. This damage relationship is valid only if the failure mode of the package is solder joint cracking due to thermal cycling fatigue. The damage relationship is established from the experimental accelerated thermal cycling failure data. This relationship depends on the solder composition and the package architecture. So, one has to be very careful while using the damage relationships while predicting failure cycles for any particular component. In the current work the damage relationships proposed by Lall, et al. [2004] and Darveaux [2000] have been used to calculate the characteristic life (α_{joint}) for life prediction of the component. The characteristic life of the component is given by Equation,

$$\alpha_{jo\,int} = N_O + \frac{A}{\left(\frac{da}{dN}\right)}$$

where 'A' is the joint diameter at the interface

$N_0 = K_1(\Delta W)^{K_2}$ is the number of cycles for crack initiation

$\frac{da}{dN} = K_3(\Delta W)^{K_4}$ is the crack propagation rate

Table 5.5: Crack Initiation and Propagation Constants

	K_1 (cycles/psi^{K_2})	**K_2**	**K_3 (in/cycle/psi^{K_4})**	**K_4**
Lall et al. [2004]	28769	-1.53	$6\text{x}10^{-7}$	0.7684
Darveaux [2000]	48300	-1.64	$3.8\text{x}10^{-7}$	1.04

CHAPTER 6

FINITE ELEMENT MODELS OF PBGA PACKAGES

This chapter shows each individual plastic ball grid array (PBGA) finite element model created for the vendor. As it was discussed in Chapter 5, the use of 3-D diagonal slice model configuration is preferred over the other configurations for the fully symmetric packages due to its computational efficiency and ability to capture true boundary conditions. In the present study, 3-D diagonal slice models have been used for all of the FEA purposes. These models include: 728, 49 196, and 256 I/O count PBGA packages from two different vendors. Each model is discussed in great detail and gives the electronic packages' exact dimensions and geometries. It also discusses contour plots of both shear stresses and plastic shear strains as well as shows graphical representations of XY, XZ, YZ shear stresses and plastic shear strains versus time for each individual package. Hysteresis loops and inelastic strain energy density values for each package will be shown here, however, they will not be discussed thoroughly until chapter 9 (life prediction chapter).

6.1 728 I/O PBGA

This electronic package is a full array of 26x28 solder interconnects yielding a 728 I/O count, which can be seen in figure 6.1. Table 6.1 also shows the packages dimensions for die size, ball height, ball diameter, mold compound thickness, substrate thickness, die attach thickness, package thickness, ball pitch, package margin, Cu pad thickness, and the die thickness. Figure 6.2 shows a volumetric view and 6.3 shows the package modeled and fully meshed in ANSYS^{TM}. PBGA 728 was an early prototype model that was modeled for the vendor, Northrop Grumman. It was not modeled with a Cu core because, at the time, the vendor was unsure whether or not it was going to be attached to a Cu core or non-core PCB. Figures 6.4-6.6 show contour plots of the total plastic work accumulated by the solder joints during thermal cycling of the TC2 temperature profile (-55°C to 125°C). The plots have been rotated about the y-axis and flipped about the x-axis to show the locations of maximum shear. The last two solder joints, the ones furthest from the center of the package, display the maximum values of the plastic work as can be seen via the contour plots.

As with all the other finite element models that will be discussed later, this model was created for life prediction using damage relationships and failure mechanics from the inelastic strain energy density obtained during simulation. It was also created to determine the affects of dwell time, whether there is a huge difference in the amount of shear stress, plastic shear strain, and inelastic strain energy density, ΔW, that the package would accumulate in a 20 minute or 30 minute dwells during thermal cycling. Figures 6.7-6.13 show the difference in these parameters described above for thermal cycle TC2 (-55°C to 125°C).

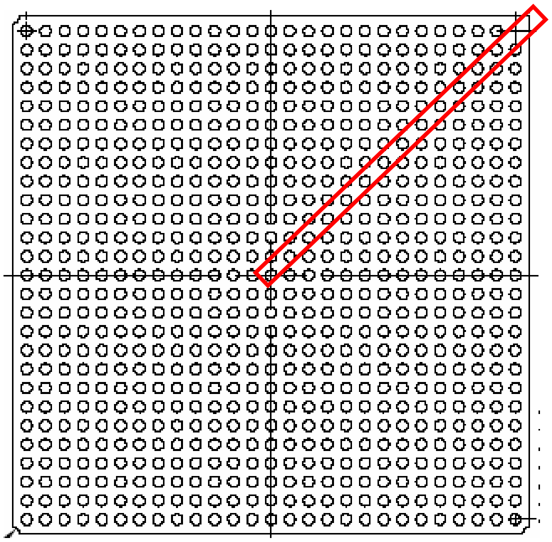


Figure 6.1: Footprint of 728 I/O PBGA with diagonal slice shown in red

Table 6.1: Dimensions of variable parameters for PBGA 728

Parameter	Dimension
Die length	19.70 mm
Die width	17.62 mm
Package Size	35 x 35
Package Height	2.33 mm
Diagonal Length	24.75 mm
Ball Count	728
Ball Pitch	1.26 mm
Ball Diameter	0.80 mm
Ball height	0.59 mm
Cu Pad thickness	0.001 mm
Die Thickness	0.36 mm
MC Thickness	1.97 mm

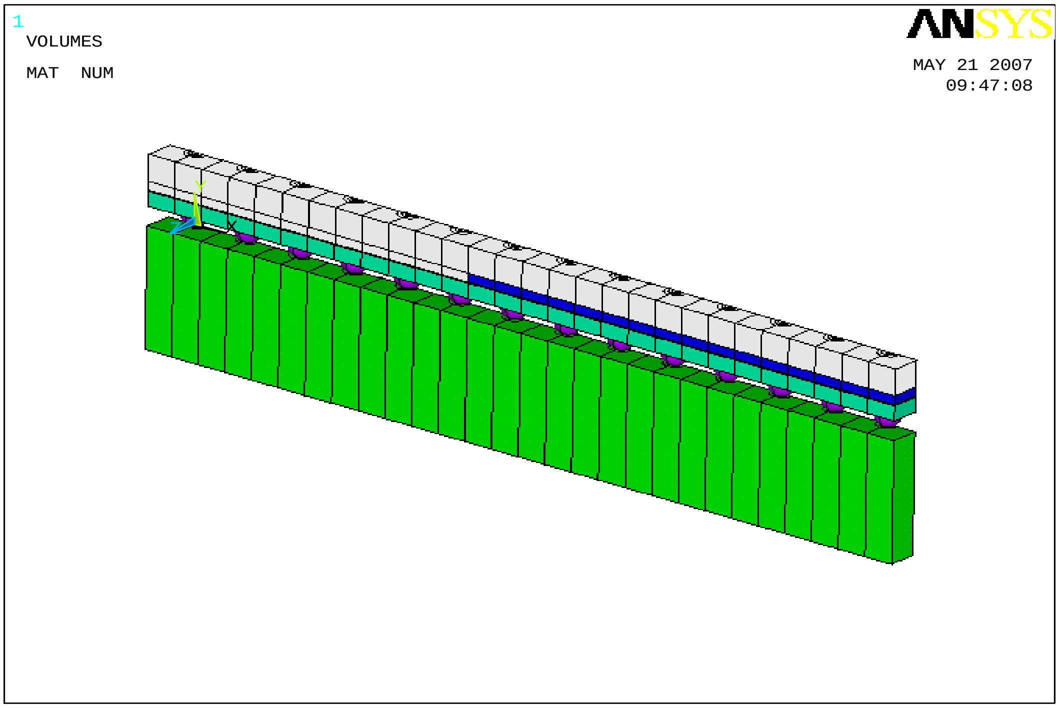


Figure 6.2: Volumetric view of PBGA 728 slice model

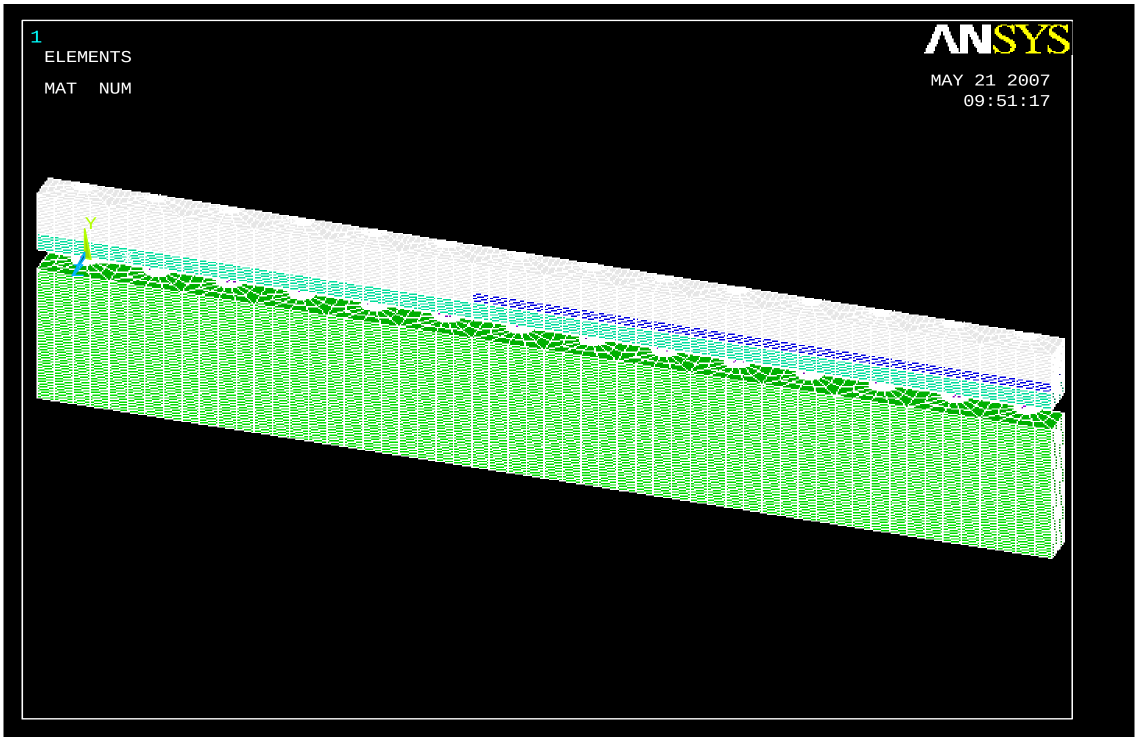


Figure 6.3: Fully Meshed view of PBGA 728 slice model

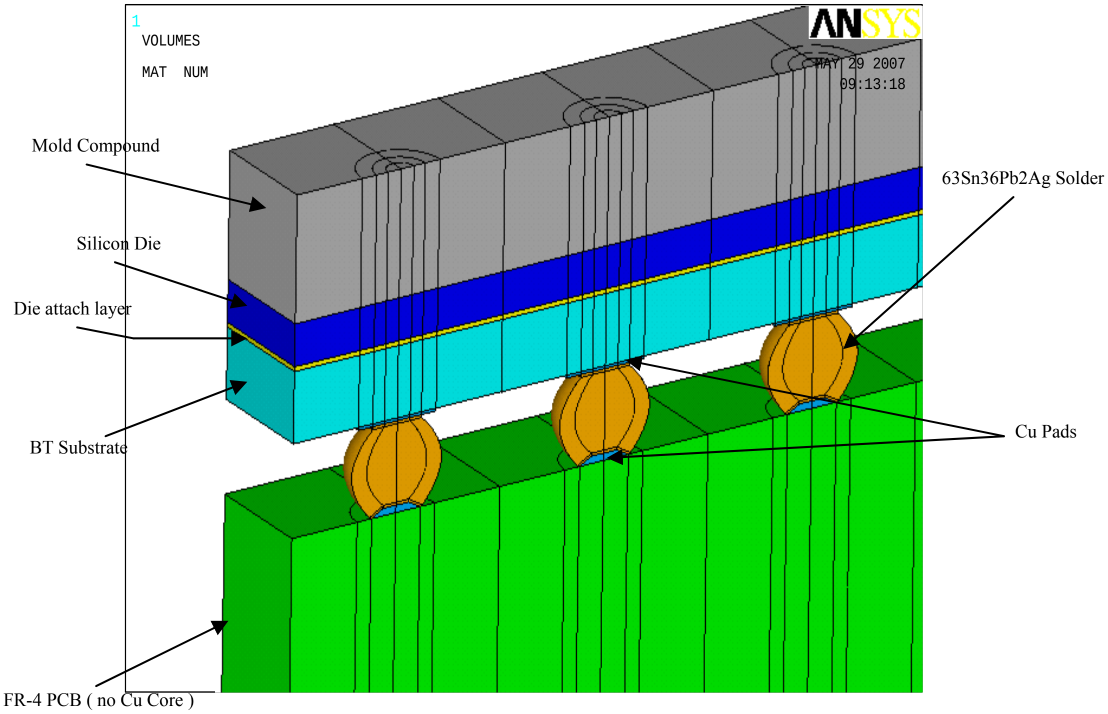


Figure 6.4: PBGA 728 Schematic showing various layers of the diagonal slice model

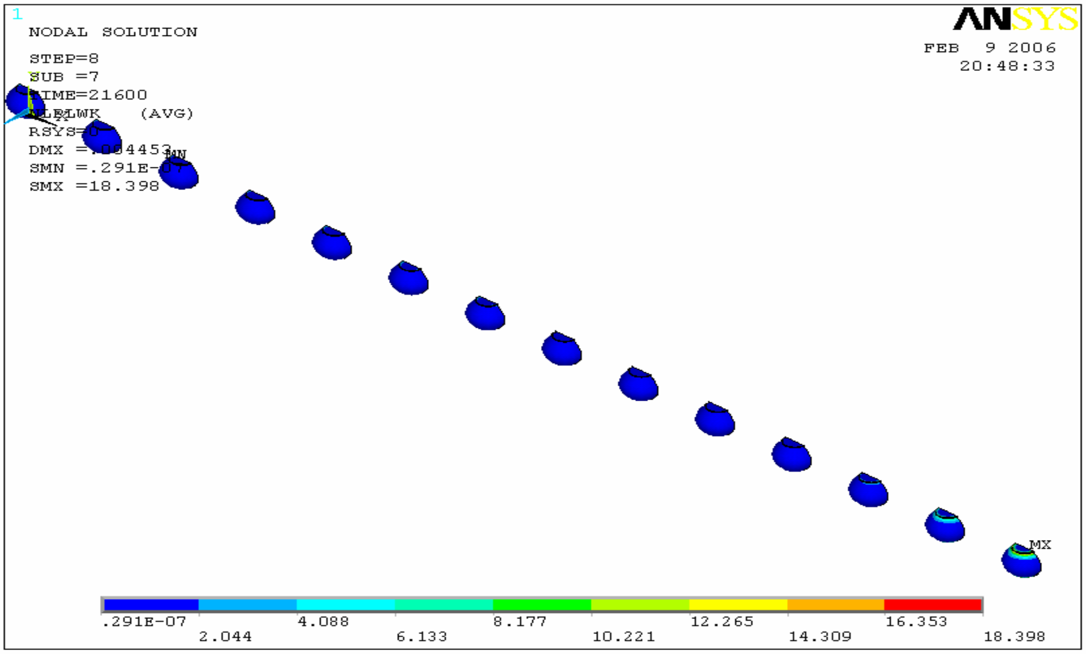


Figure 6.5: Contour plot of accumulated plastic work on the solder balls

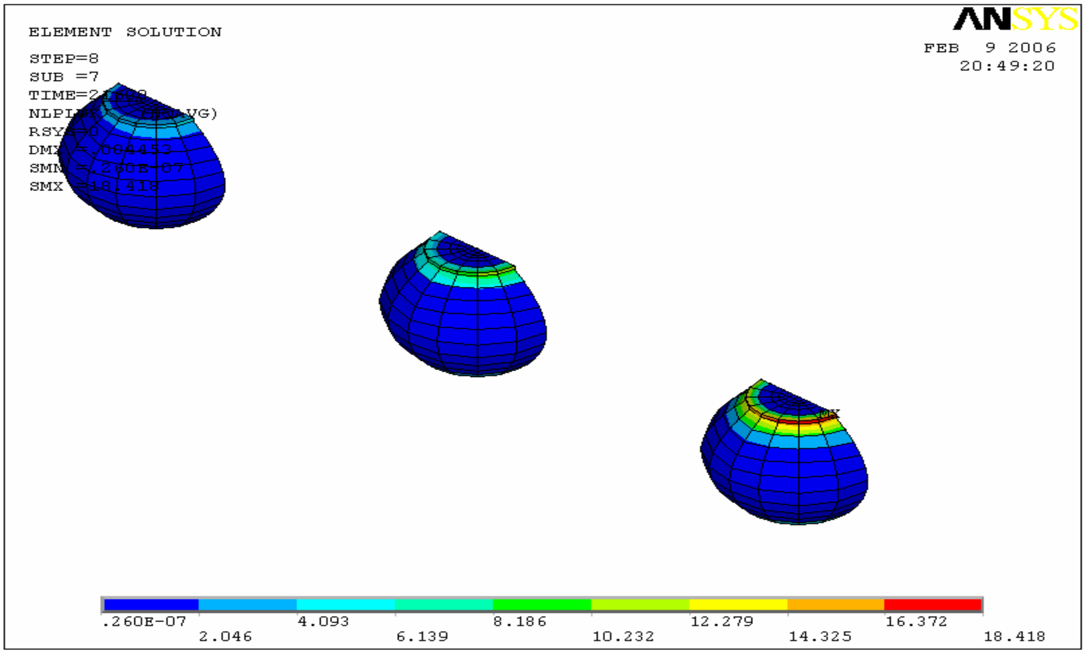


Figure 6.6: Close up of the last three solder balls showing the total plastic work of the last solder ball which is the furthest from the center of the package

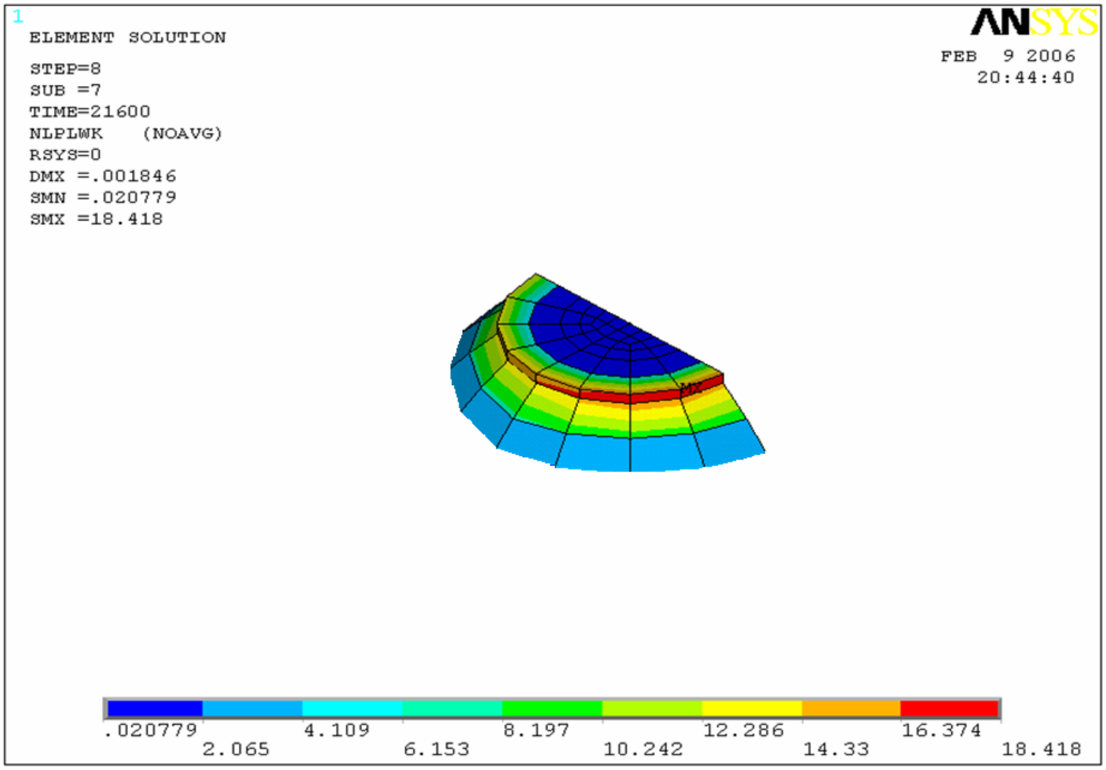


Figure 6.7: Close-up total plastic work contour plot of top few interface layers on the furthest solder ball (DNP)

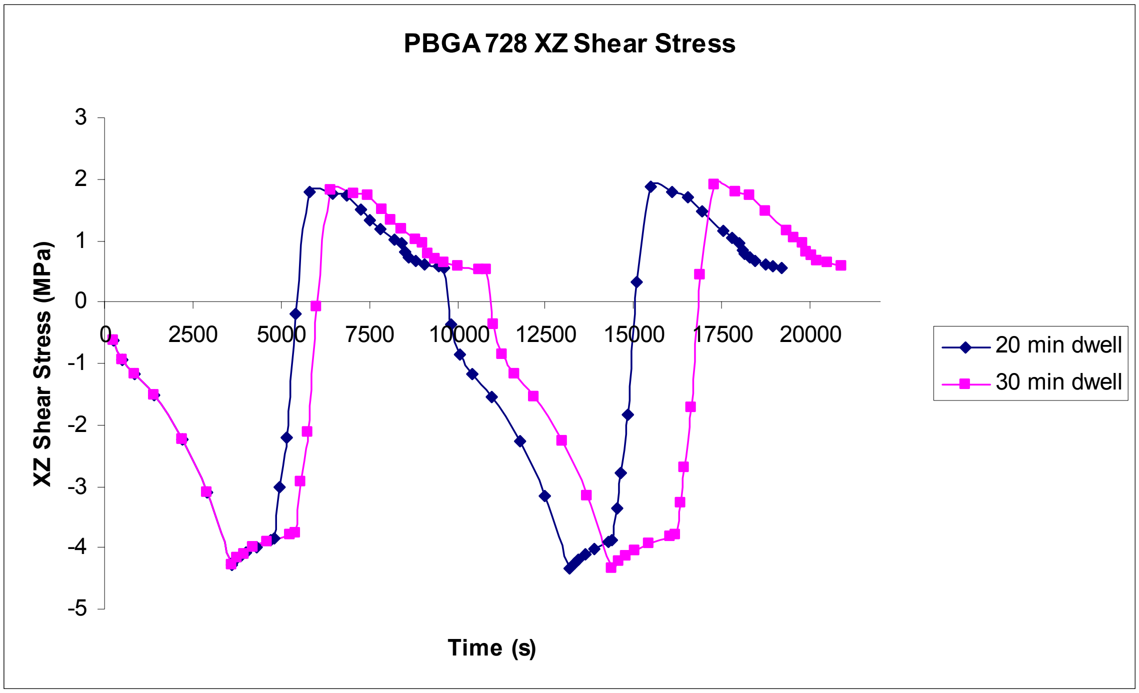


Figure 6.8: Plot of XZ Shear stress with different dwell times

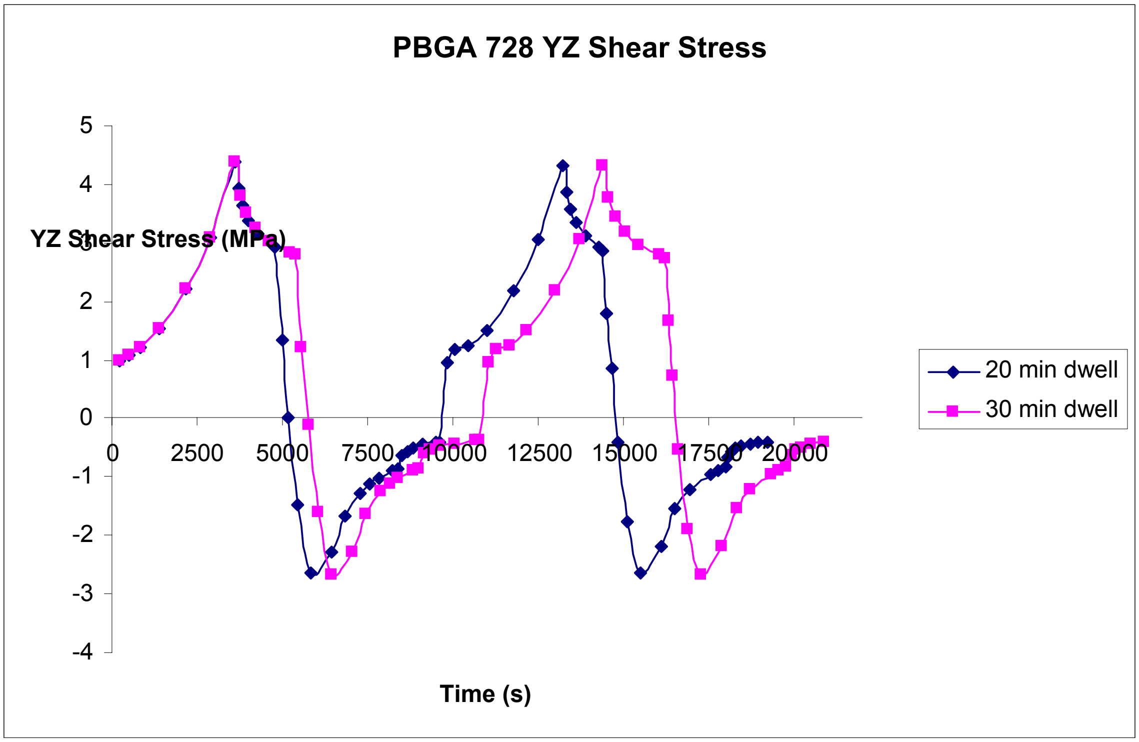


Figure 6.9: Plot of YZ Shear stress with different dwell times

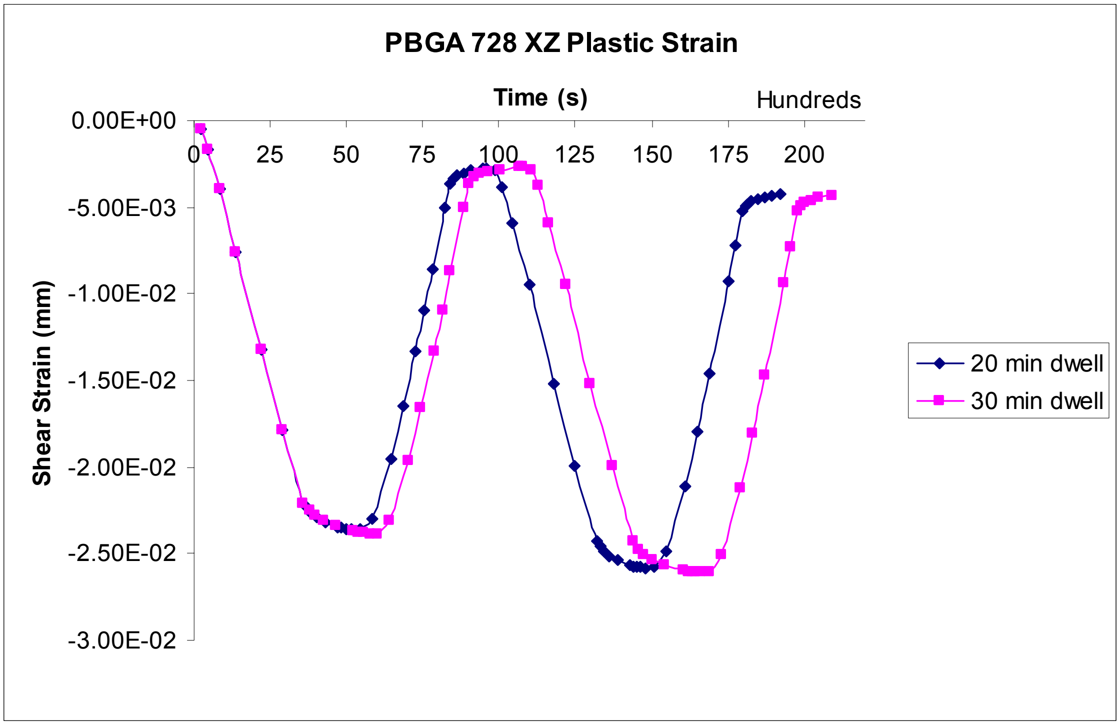


Figure 6.10: Plot of XZ Plastic shear strain with different dwell times

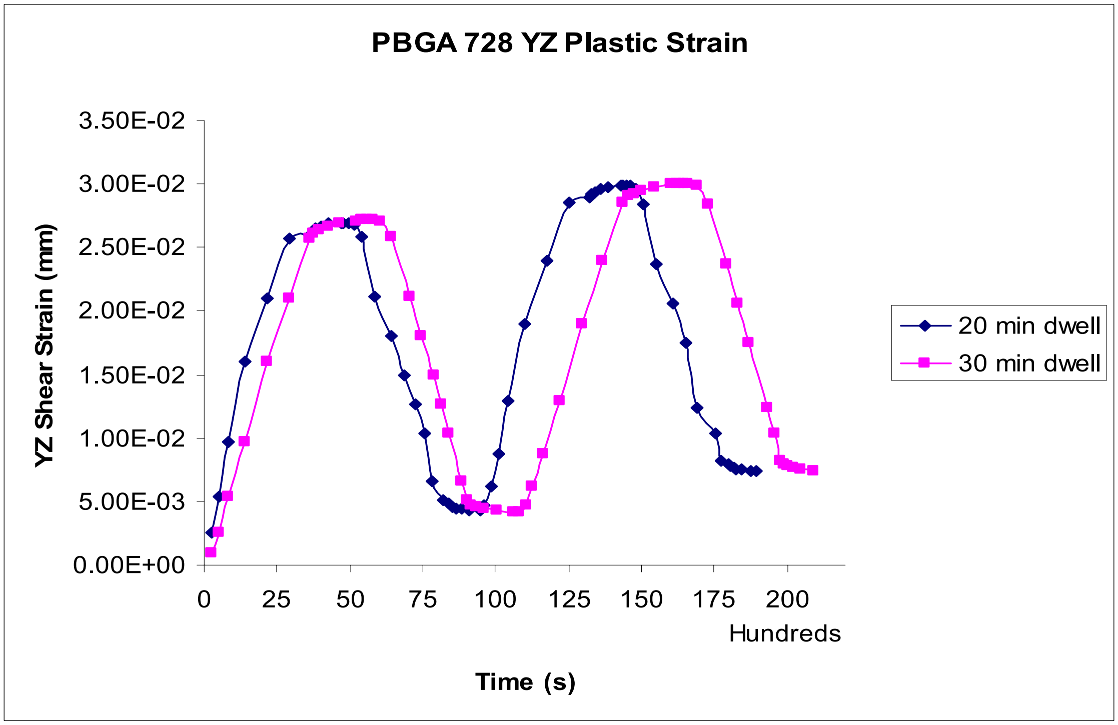


Figure 6.11: Plot of YZ Plastic shear strain with different dwell times.

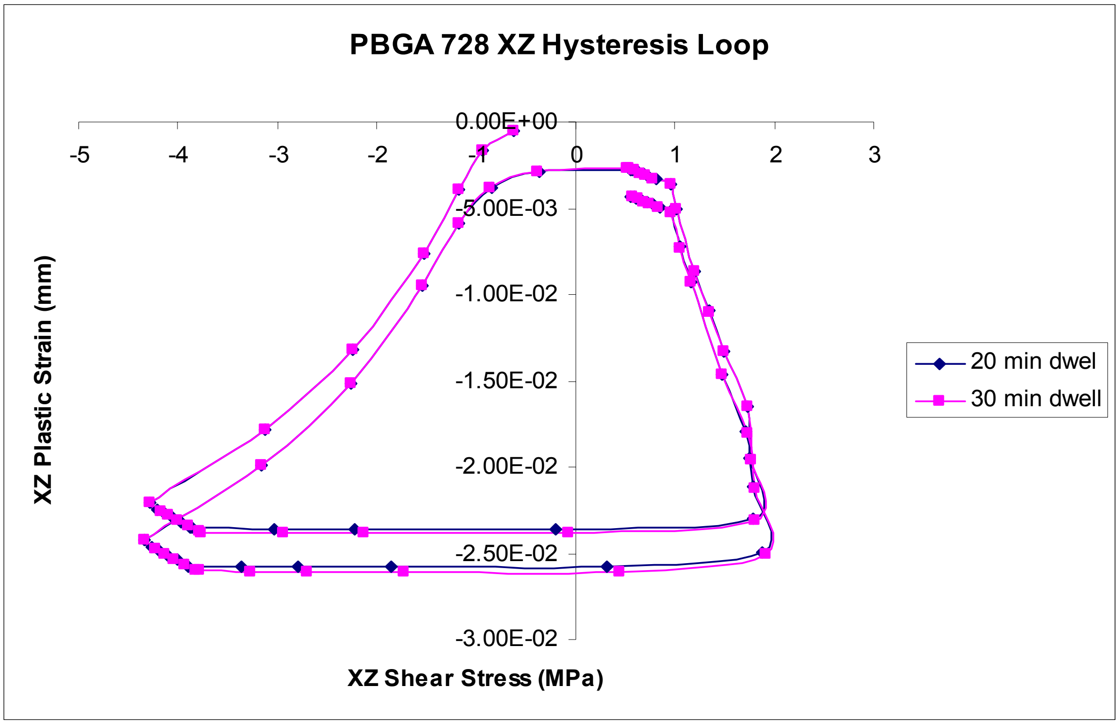


Figure 6.12: Plot of XZ Hysteresis loop with different dwell times

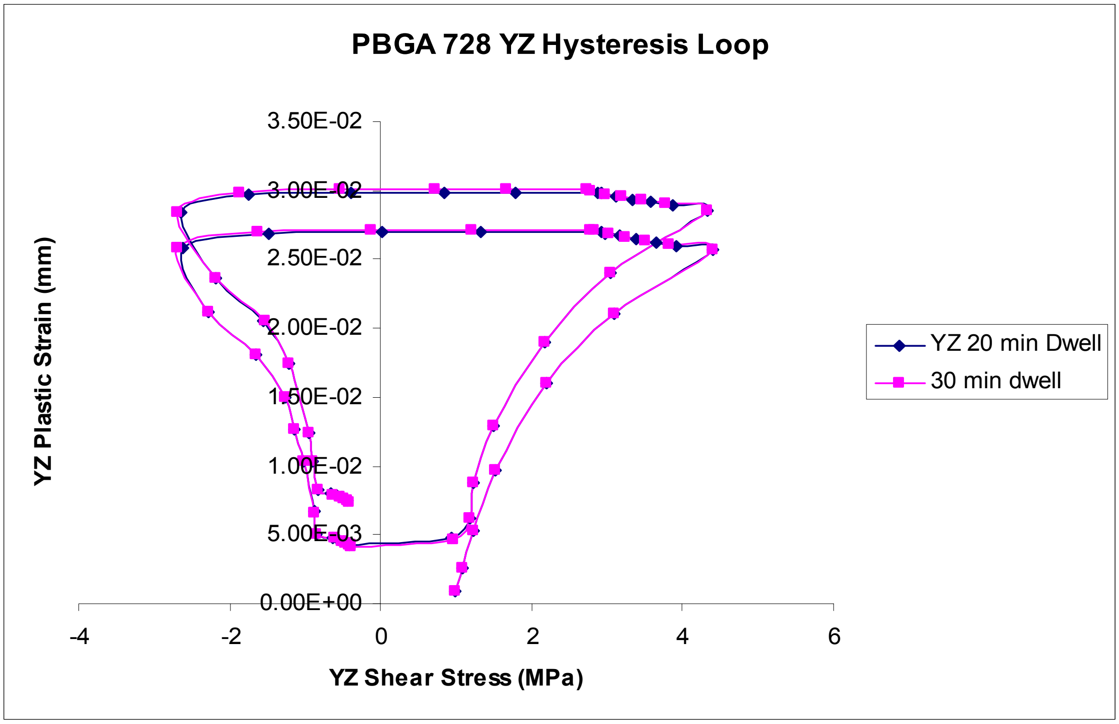


Figure 6.13: Plot of YZ Hysteresis Loop with different dwell times

Dwell Time Conclusion:

After running two separate simulations on PBGA 728 and plotting the data for XZ and YZ shear strain and shear stresses, it can be seen from the graphs that the difference between 20 minute and 30 minute dwell times is not very significant. The plastic strains, both YZ and XZ, have the exact same magnitude of strain, however, they occur at a slightly different time, about 20 to 25 seconds apart. The shear stresses, both XZ and YZ, are very similar to the plastic strains, in that they have the same magnitudes, they occur at a slightly later time with 30 minute dwells. The hysteresis loops show that the inelastic strain energy density (ΔW), the area inside the hysteresis loops, are almost exactly the same. This shows that 30 minute and 20 minute dwell times at this particular thermal cycle, produce the same value for ΔW. Twenty minute dwell times would allow for a slightly quicker simulation time however, the vendor chose to run simulations on all models for 30 minute dwells anyways. For all the finite element models shown in this research, dwell times are 30 minutes at the high and low temperatures.

6.2 49 I/O PBGA

This electronic package is a full array of 7x7 solder interconnects yielding a 49 I/O count, which can be seen in figure 6.14. Table 6.2 also shows the packages dimensions for die size, ball height, ball diameter, mold compound thickness, substrate thickness, die attach thickness, package thickness, ball pitch, package margin, Cu pad thickness, die thickness, and a few other variable parameters. Figure 6.15 shows the fully meshed diagonal slice FE model of PBGA 49 in ANSYS^{TM}. PBGA 49 was modeled for the vendor, Northrop Grumman, with a copper core PCB. Simulations have been run in ANSYS^{TM} for all four temperature conditions, TC1-TC4. Figures 6.16-6.21 show contour plots of the total plastic work accumulated by the solder joints during thermal cycling of the TC1 temperature profile (-40°C to 95°C). The last solder joint, the one furthest from the center of the package, accumulated the maximum values of the plastic work as can be seen via the contour plots.

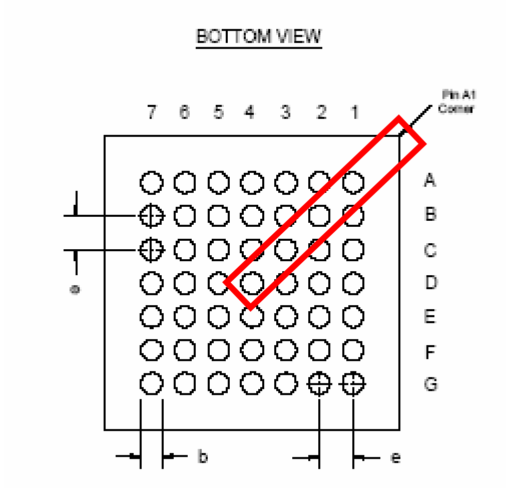


Figure 6.14: Footprint of 49 I/O PBGA with diagonal slice shown in red

Table 6.2: Dimensions of variable parameters of PBGA 49

Parameter	**Dimension**
Die Length	2.9
Die Width	3.0
Die Thickness	0.254
Package Size	7x7
Diagonal Length	4.173
Ball Count	49
Ball Pitch	0.800
Ball Height	0.305
Ball Diameter	0.521
Cu Pad Thickness	0.025
BT Thickness	0.356
MC Thickness	0.400
Die Attach Thickness	0.018
Die to Body Ratio	2.370

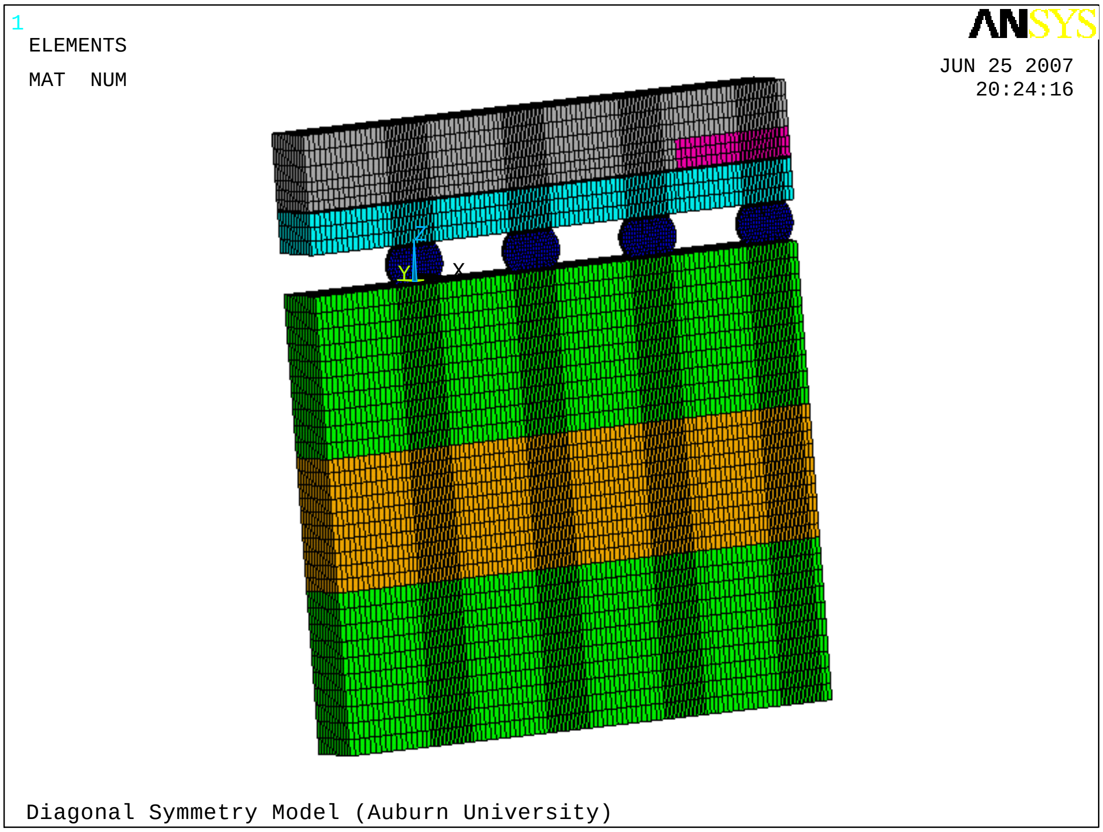


Figure 6.15: Fully Meshed FEA Model of the 49 I/O PBGA

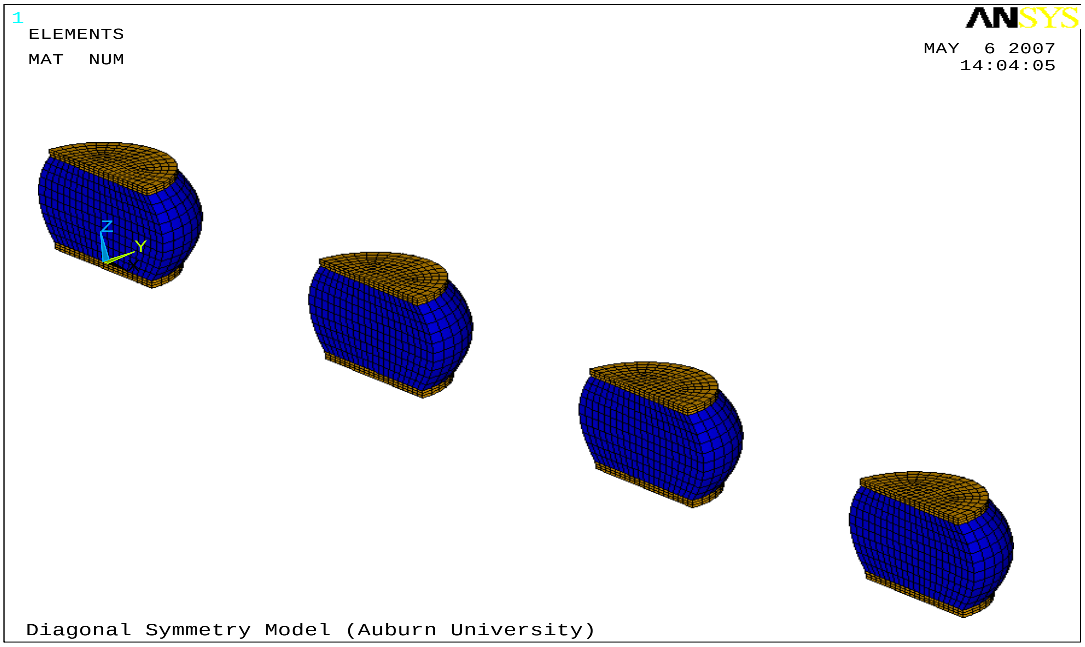


Figure 6.16: Screen capture showing meshed solder balls and copper pads

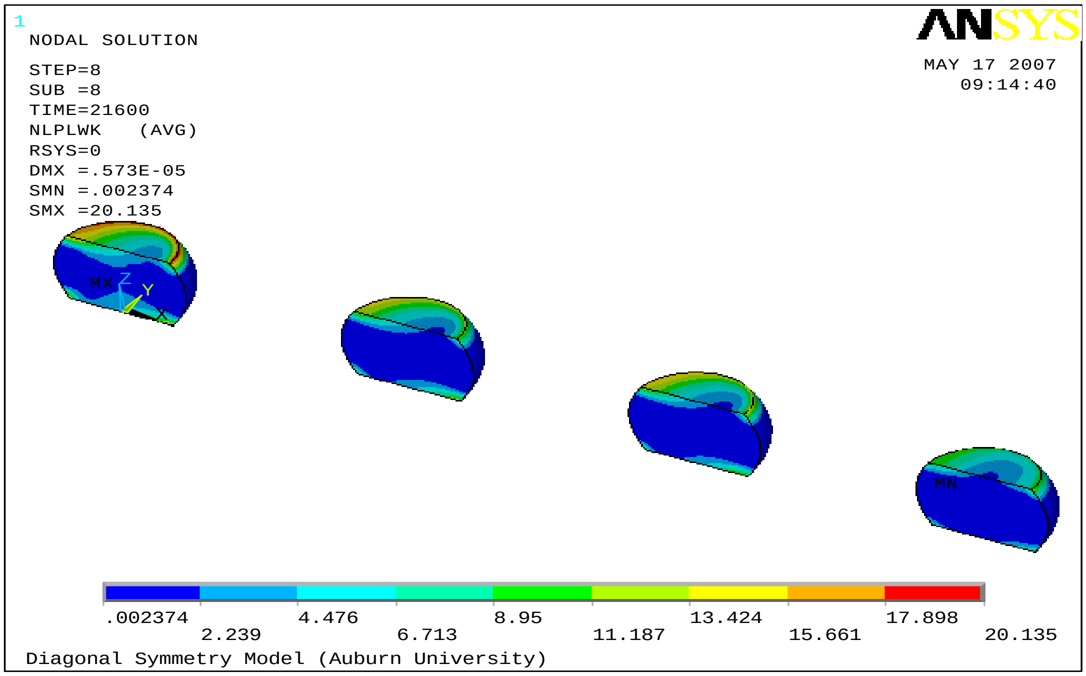


Figure 6.17: Contour plot of accumulated plastic work of PBGA 49 solder balls (TC1)

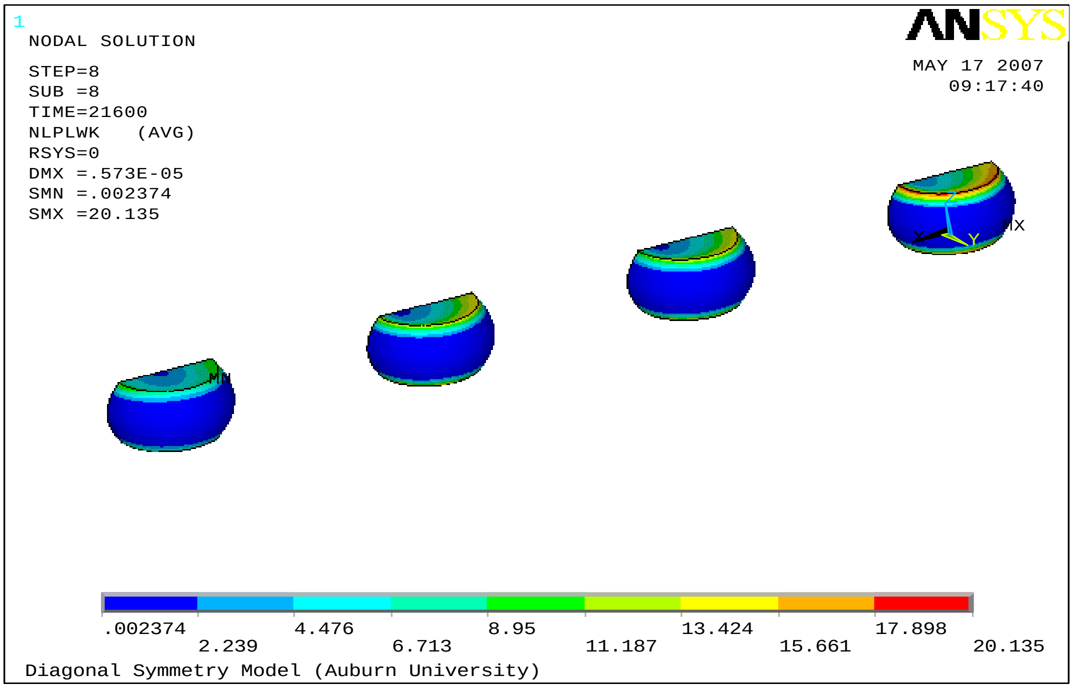


Figure 6.18: Rotated view of contour plot for accumulated plastic work (TC1)

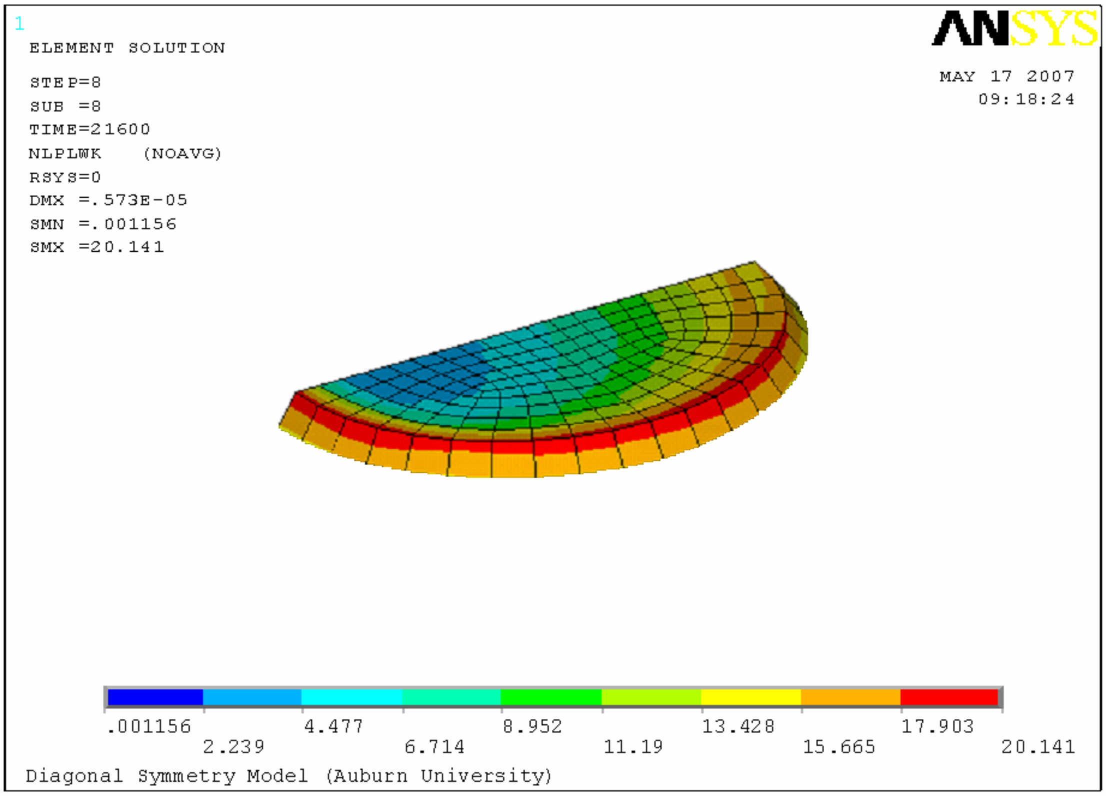


Figure 6.19: Solder ball interface layers with maximum accumulated plastic work (TC1)

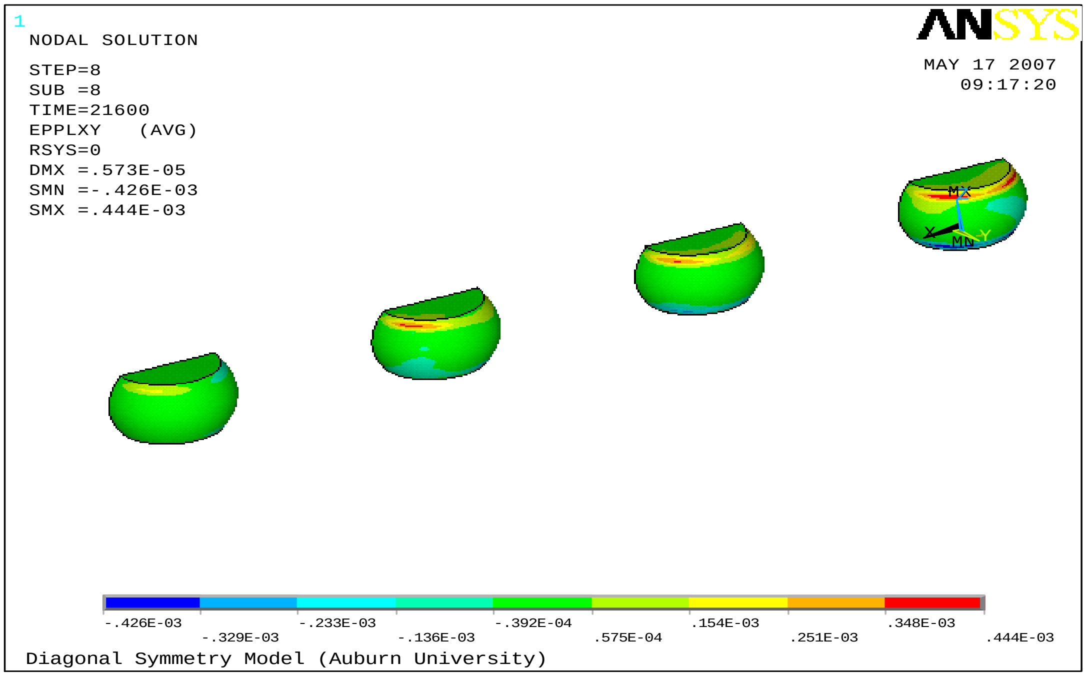


Figure 6.20: Contour Plot of accumulated XY plastic shear strain (TC1)

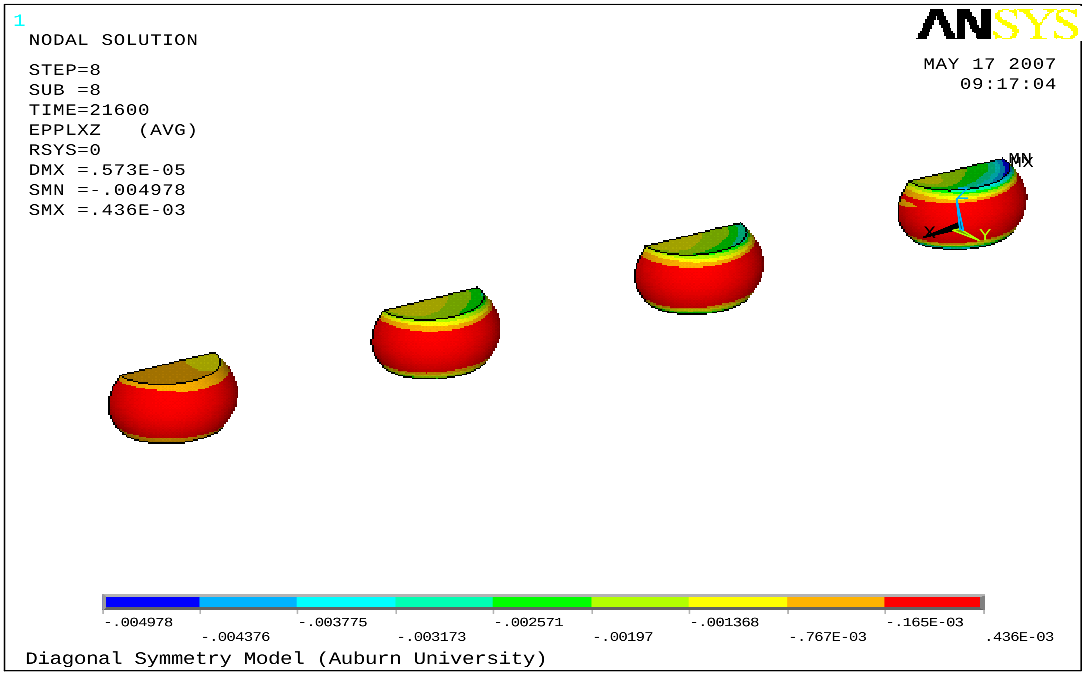


Figure 6.21: Contour Plot of accumulated XZ plastic shear strain (TC1)

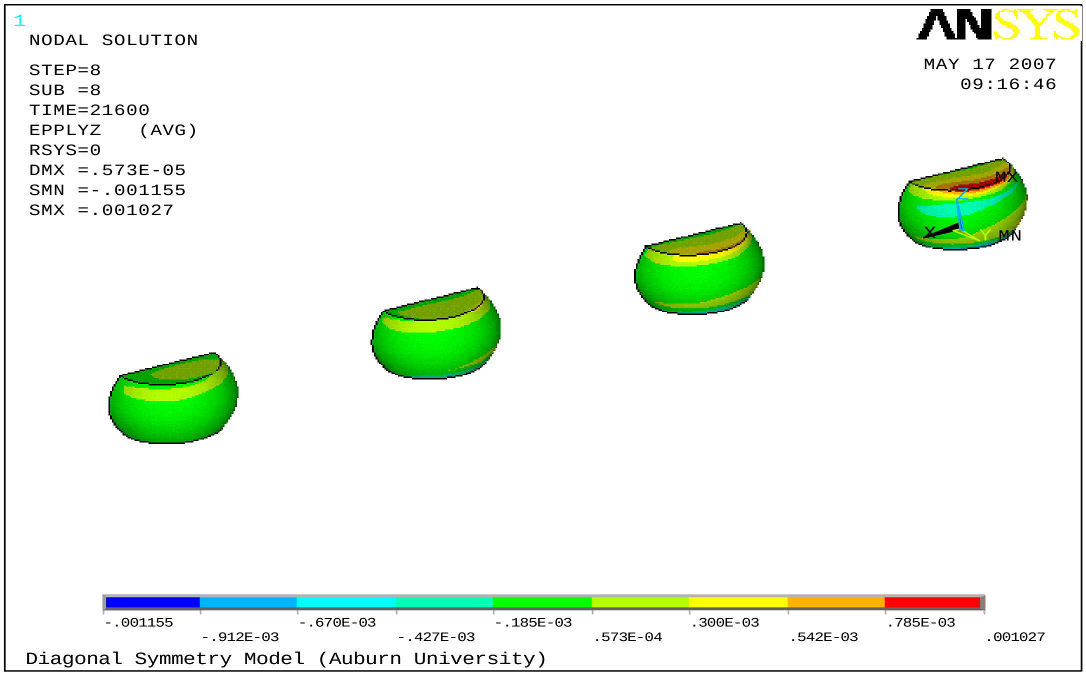


Figure 6.22: Contour plot of accumulated YZ plastic shear strain (TC1)

Figures 6.23-6.26 show contour plots of the total plastic work accumulated by the solder joints during thermal cycling of the TC2 temperature profile (-55°C to 125°C).

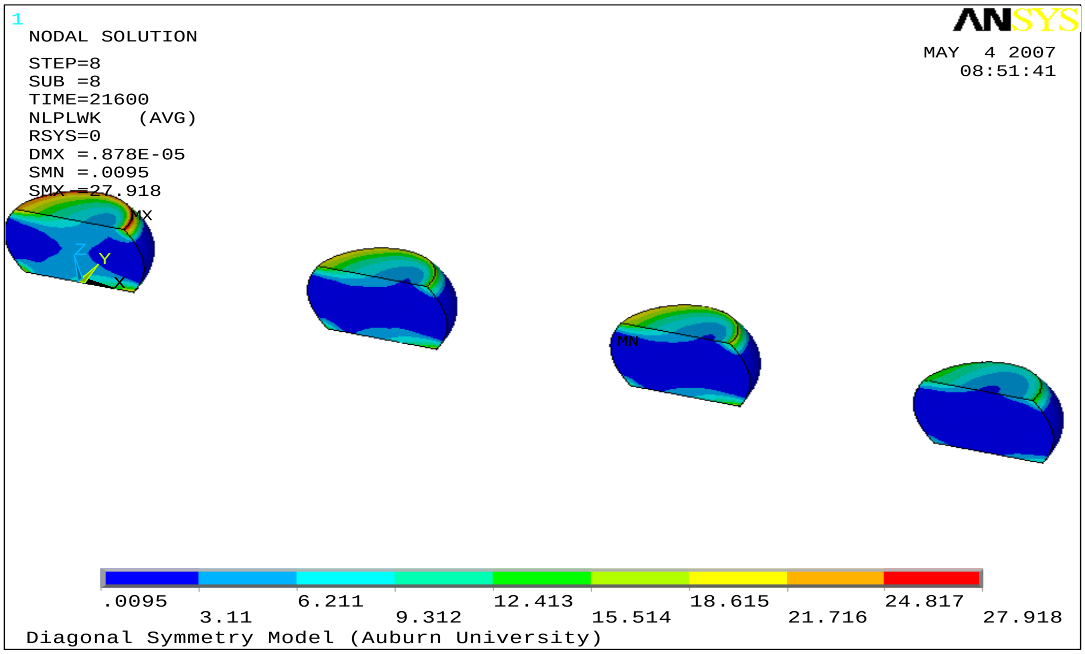


Figure 6.23: Contour plot of accumulated plastic work of PBGA 49 solder balls (TC2)

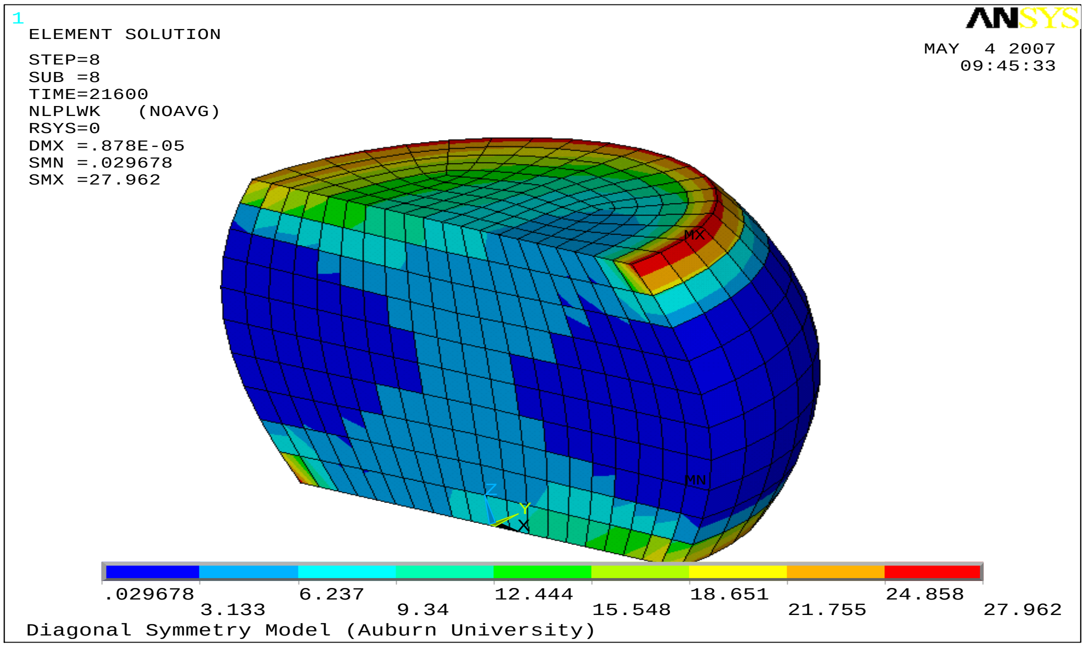


Figure 6.24: Solder ball with maximum accumulated plastic work (TC2)

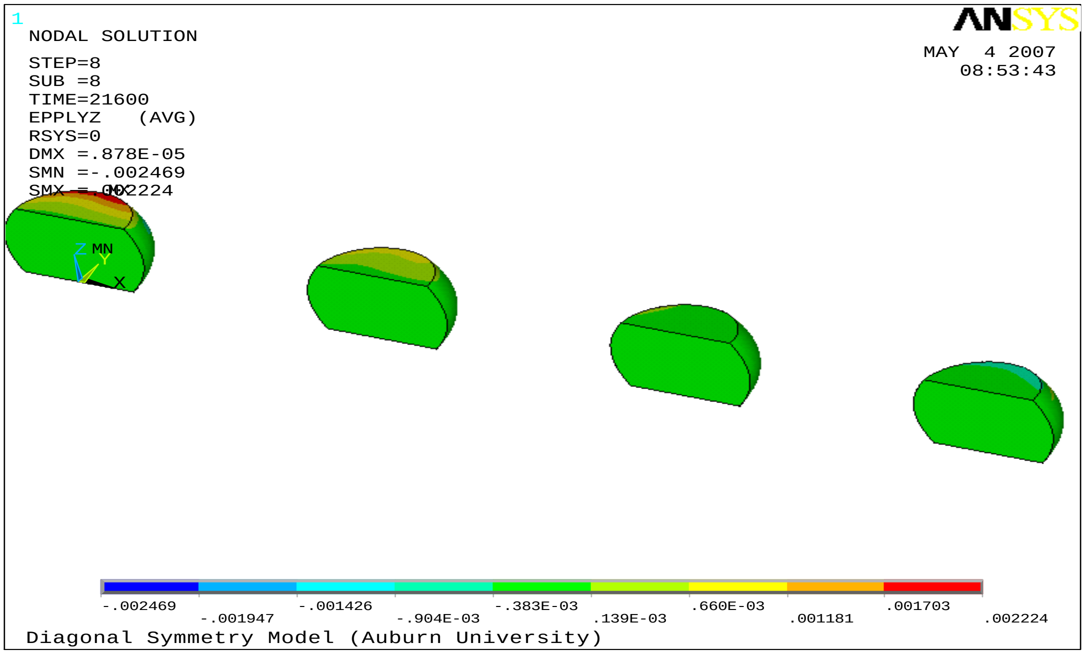


Figure 6.25: Contour plot of accumulated YZ plastic shear strain (TC2)

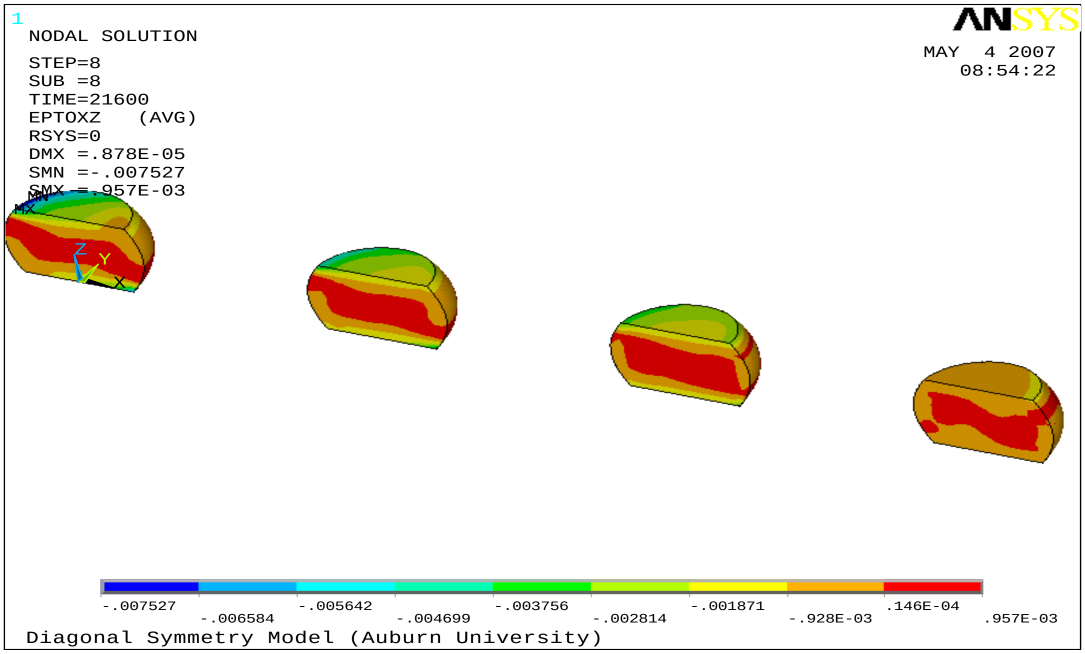


Figure 6.26: Contour Plot of accumulated XZ plastic shear strain (TC2)

Figures 6.27-6.31 show contour plots of the total plastic work accumulated by the solder joints during thermal cycling of the TC3 temperature profile (3°C to 100°C)

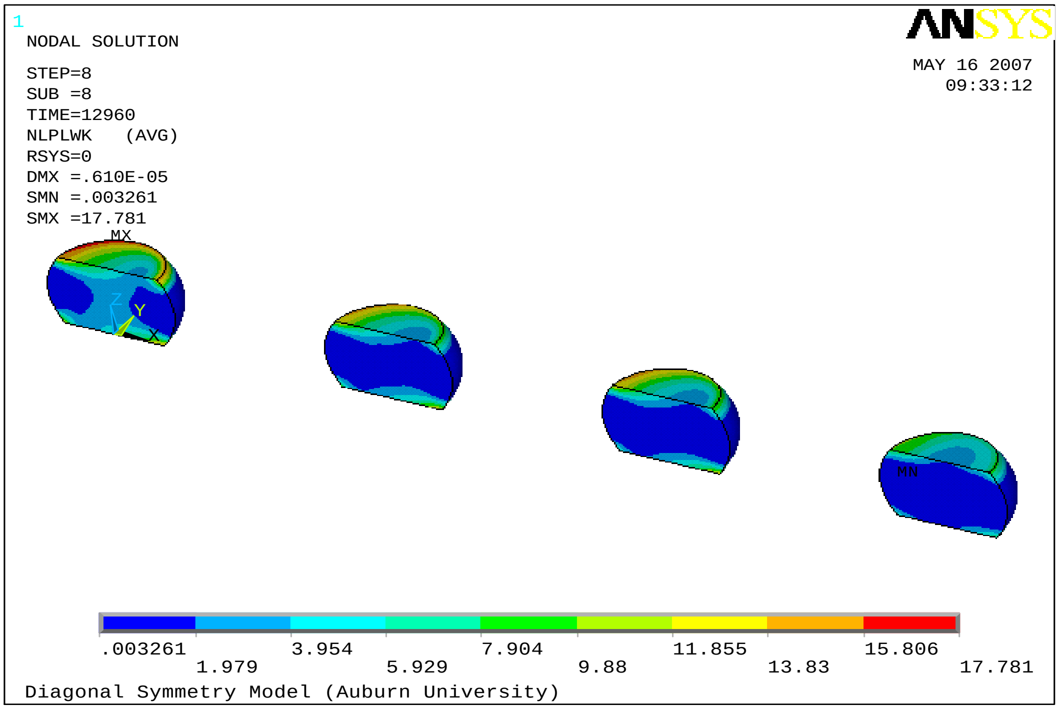


Figure 6.27: Contour plot of accumulated plastic work of PBGA 49 solder balls (TC3)

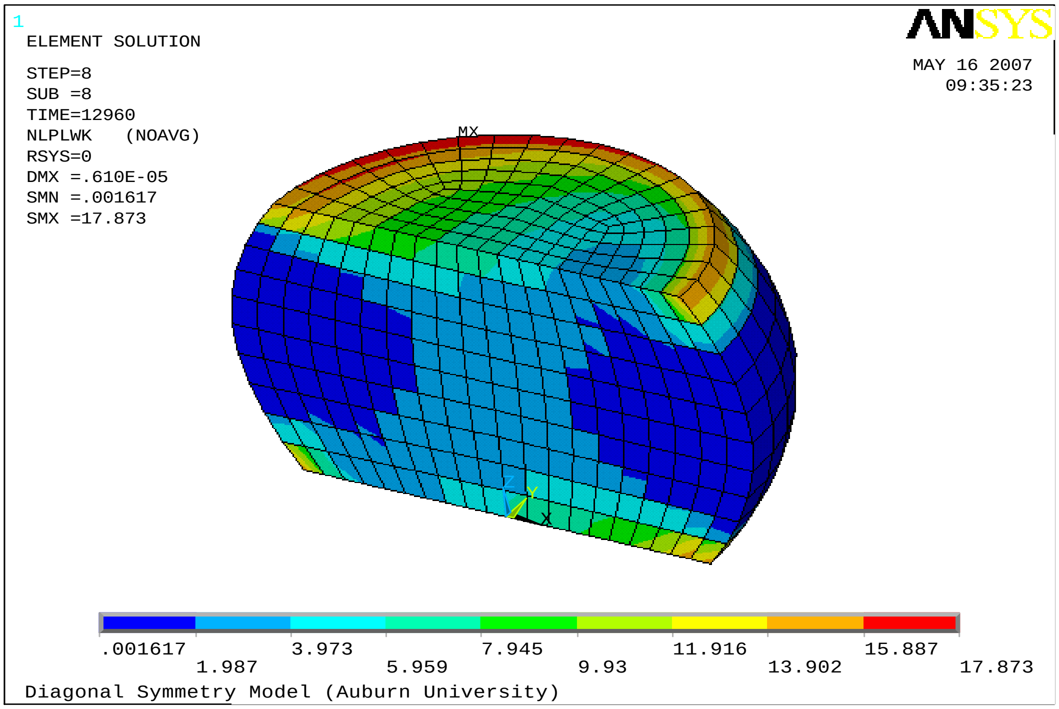


Figure 6.28: Solder ball with maximum accumulated plastic work (TC3)

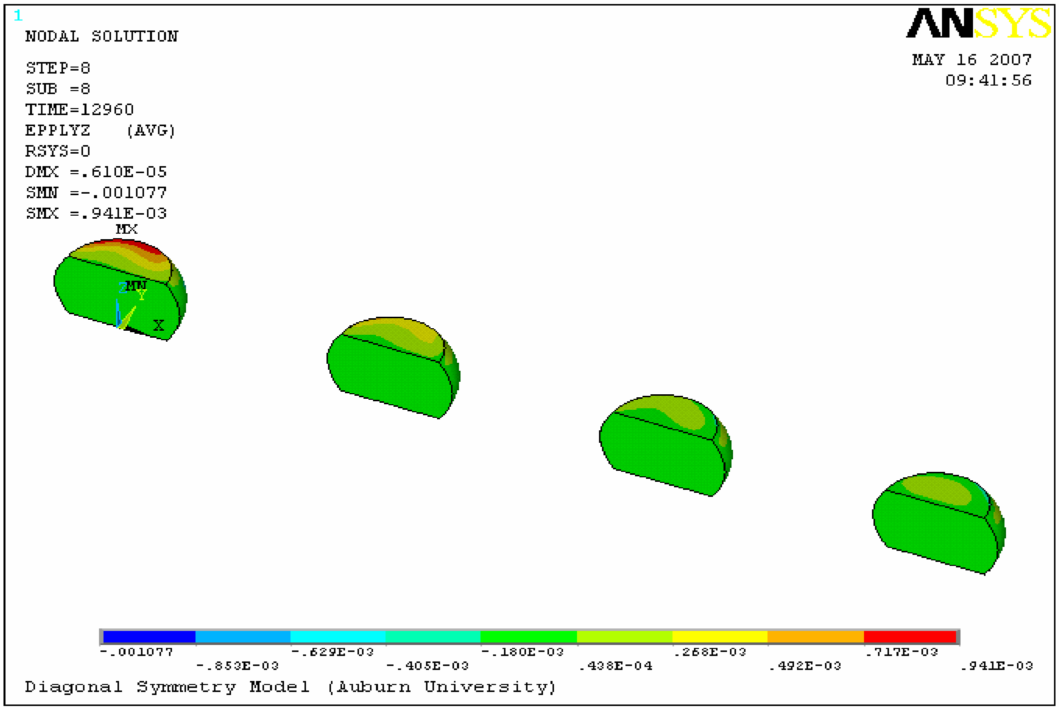


Figure 6.29: Contour plot of accumulated YZ plastic shear strain (TC3)

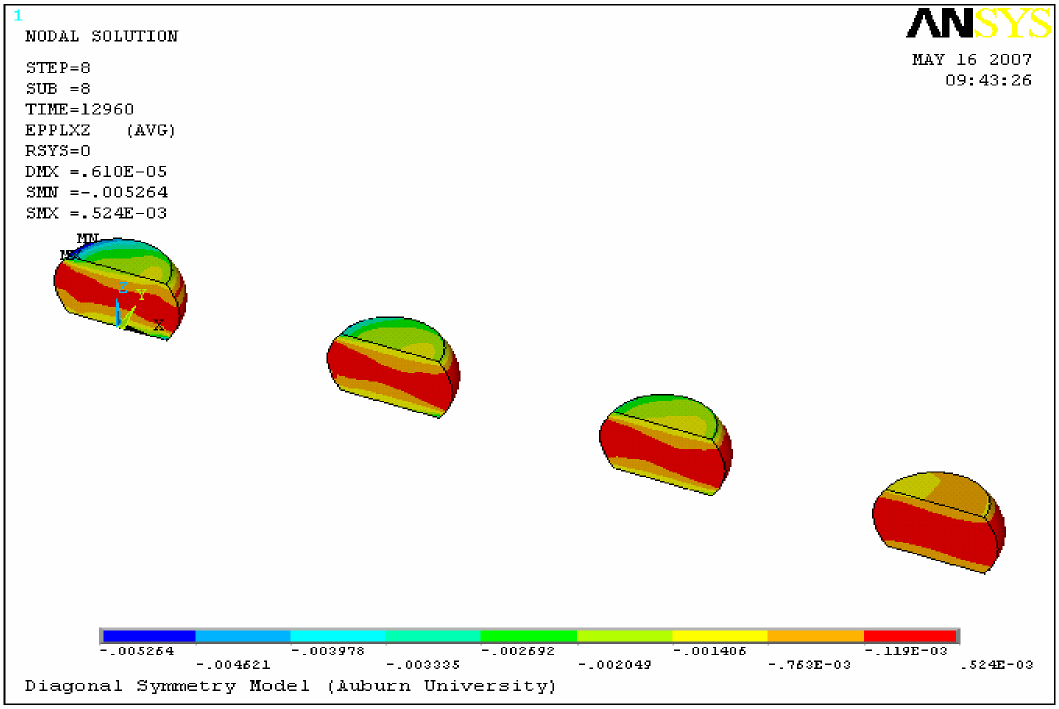


Figure 6.30: Contour Plot of accumulated XZ plastic shear strain (TC3)

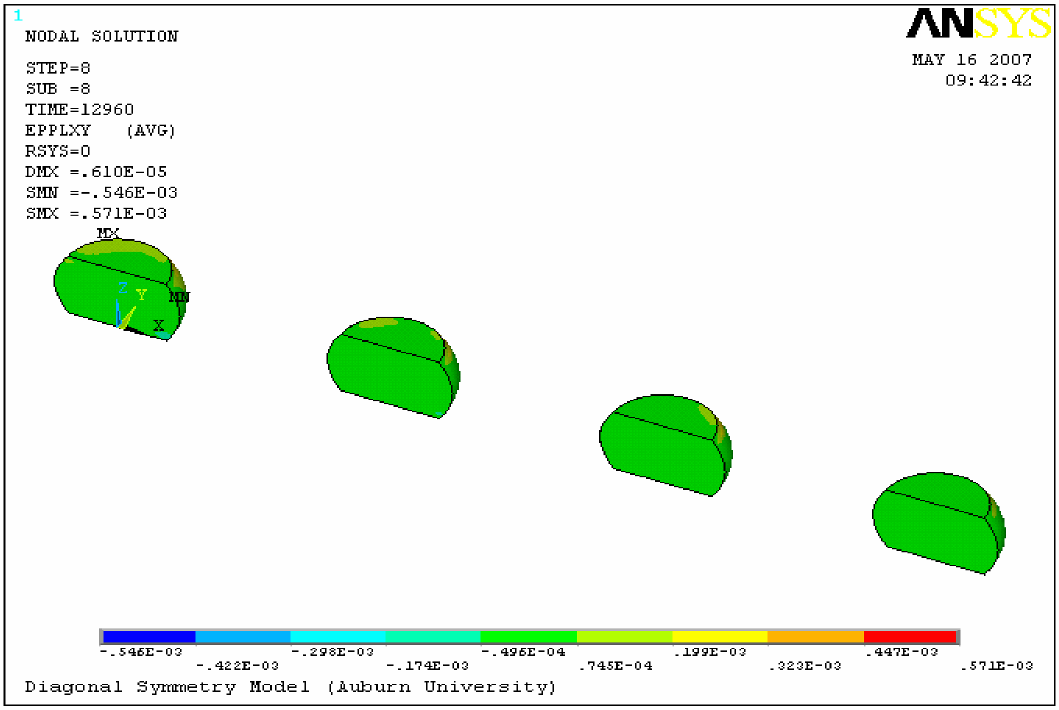


Figure 6.31: Contour Plot of accumulated XY plastic shear strain (TC3)

Figures 6.32-6.33 show contour plots of the total plastic work accumulated by the solder joints during thermal cycling of the TC4 temperature profile (-20°C to 60°C).

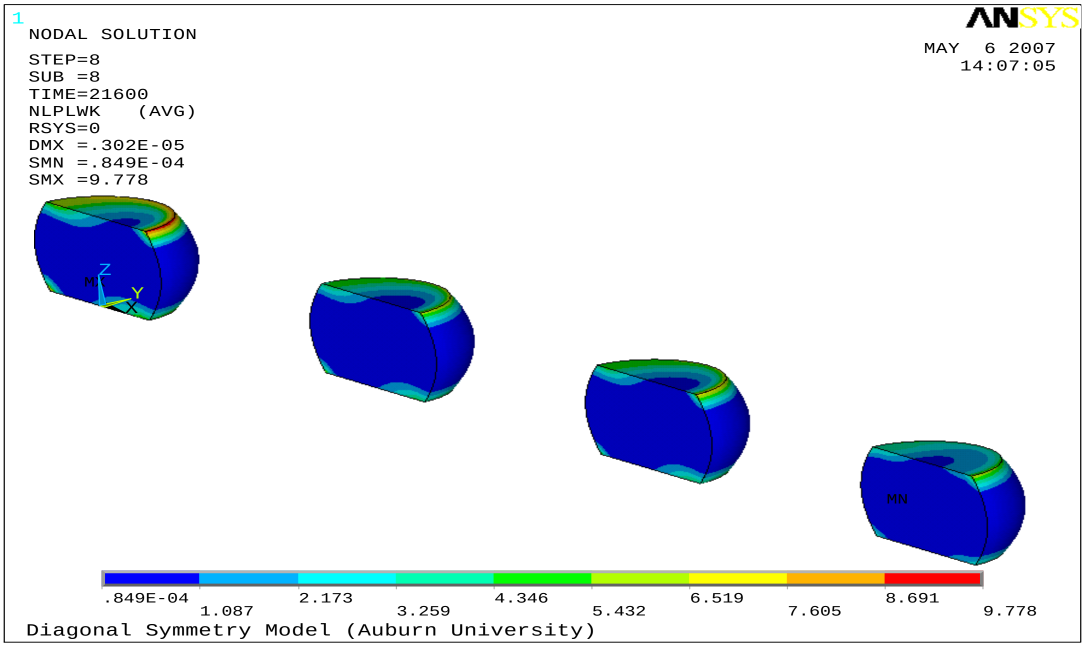
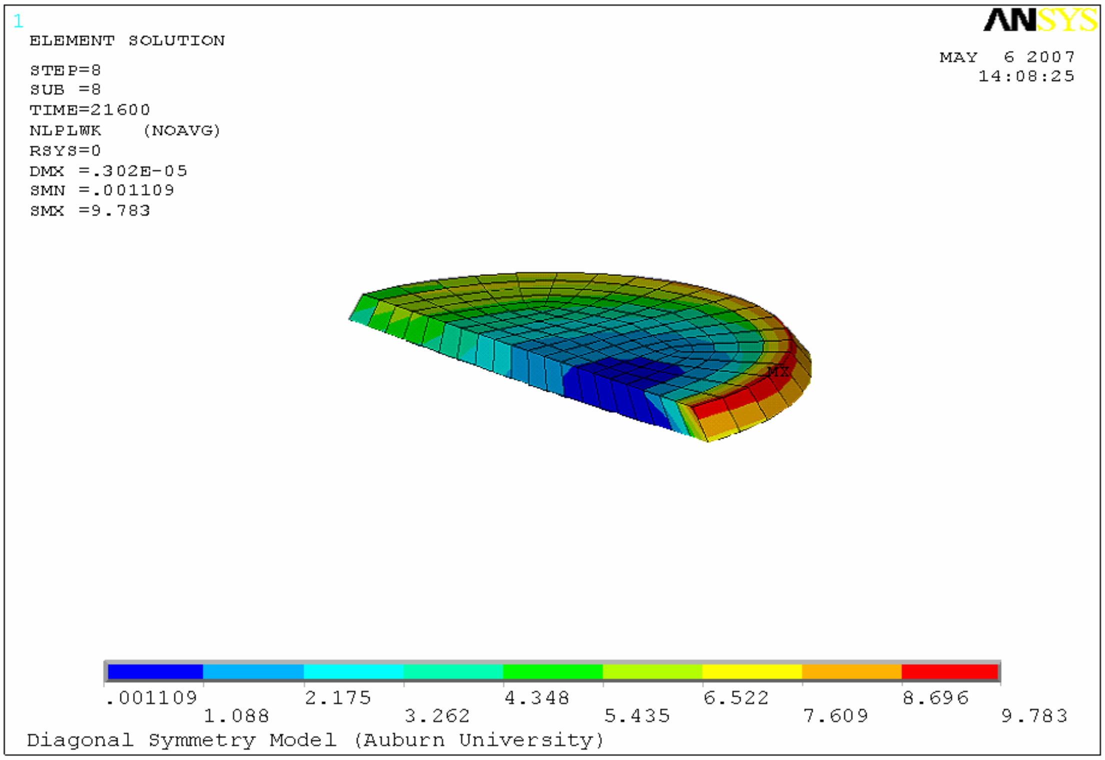


Figure 6.32: Contour plot of accumulated plastic work of PBGA 49 solder balls (TC4)



6.33: Solder ball top interface layer with maximum accumulated plastic work (TC4)

6.3 Shear Stress and Plastic Shear Strain Plots for PBGA 49

Figures 6.34-6.40 show plots of various shear stresses as well as plastic shear strain plots. Each graph shows plots of PBGA 49 under TC1, TC2, and TC4 temperature profiles. These profiles are simulated and analysis is run with the exact same profiles that are used for the experimental data, so that the simulations can be correlated in Chapter 9 to validate the FEA models. In figure 6.34 and 6.36, one can see that the XY and XZ plastic shear strains are greatest for temperature profiles TC2. This is because TC2 has the largest ΔT value (135°C), and hence causes the greatest amount of inelastic strain energy density, or ΔW value. Figure 6.38 shows the same thing for the XZ shear stress, showing that TC2 has the greatest amount of shear stress. The same could be shown fro figure 6.37 if TC2 were plotted against TC1 and TC3. However, the computers that this work was being simulated on, crashed and this data was unrecoverable. However, if it were plotted, one can speculate to say that TC2 would have the greatest amount of XY shear stress as well.

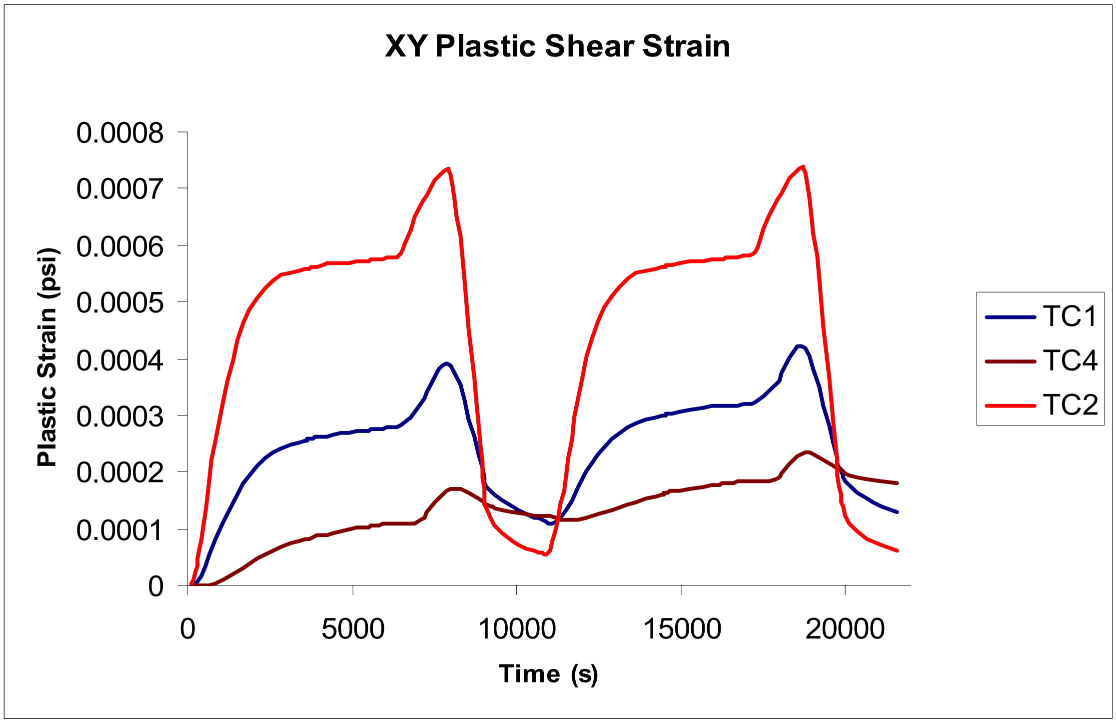


Figure 6.34: XY Plastic shear strain plot of PBGA 49 under TC1, TC2, and TC3 temperature profiles

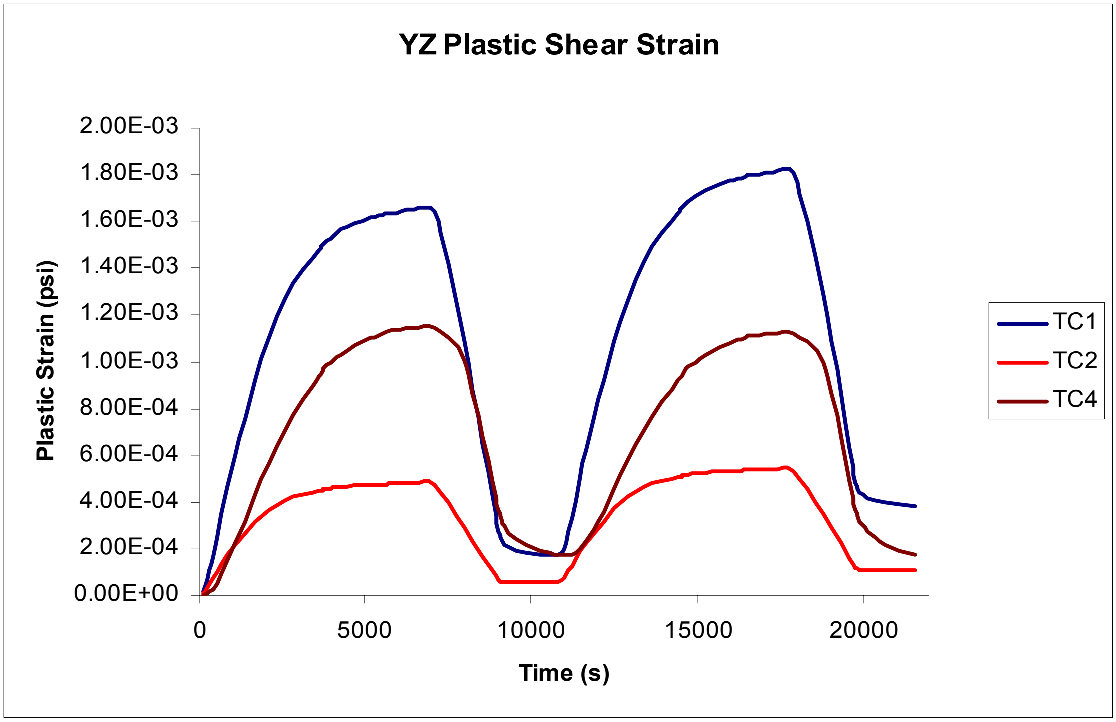


Figure 6.35: YZ Plastic shear strain plot for PBGA49 under TC1, TC2, and TC4 thermal cycles

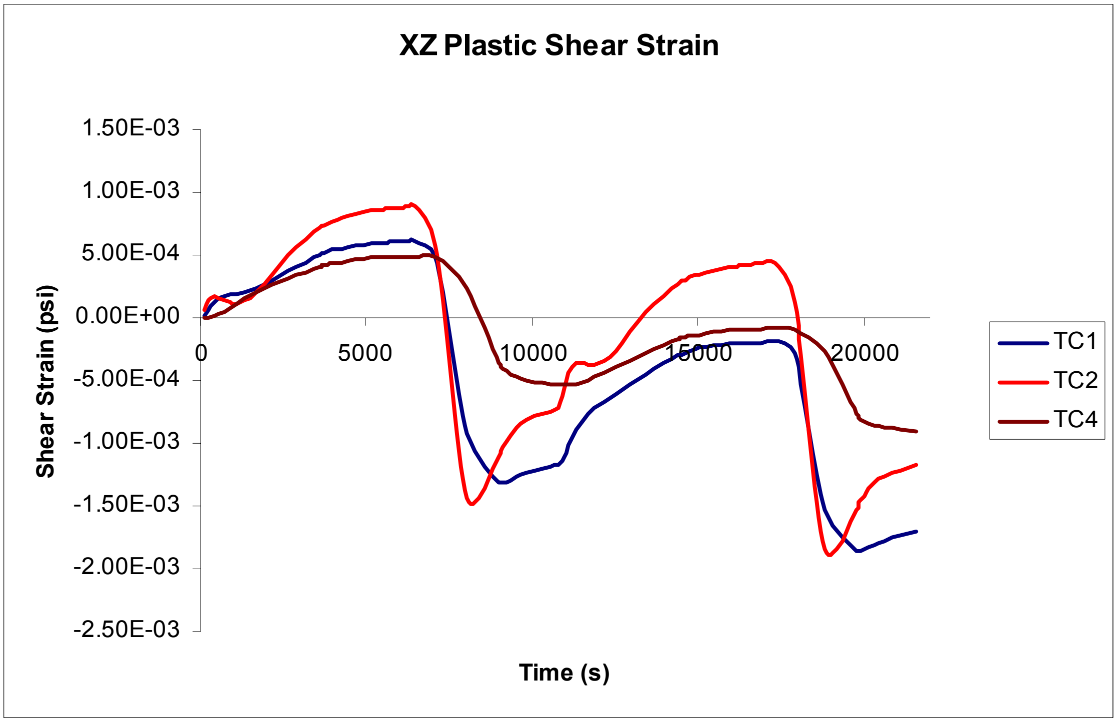


Figure 6.36: XZ Plastic shear strain plots of PBGA49 under TC1, TC2, and TC4 thermal profiles

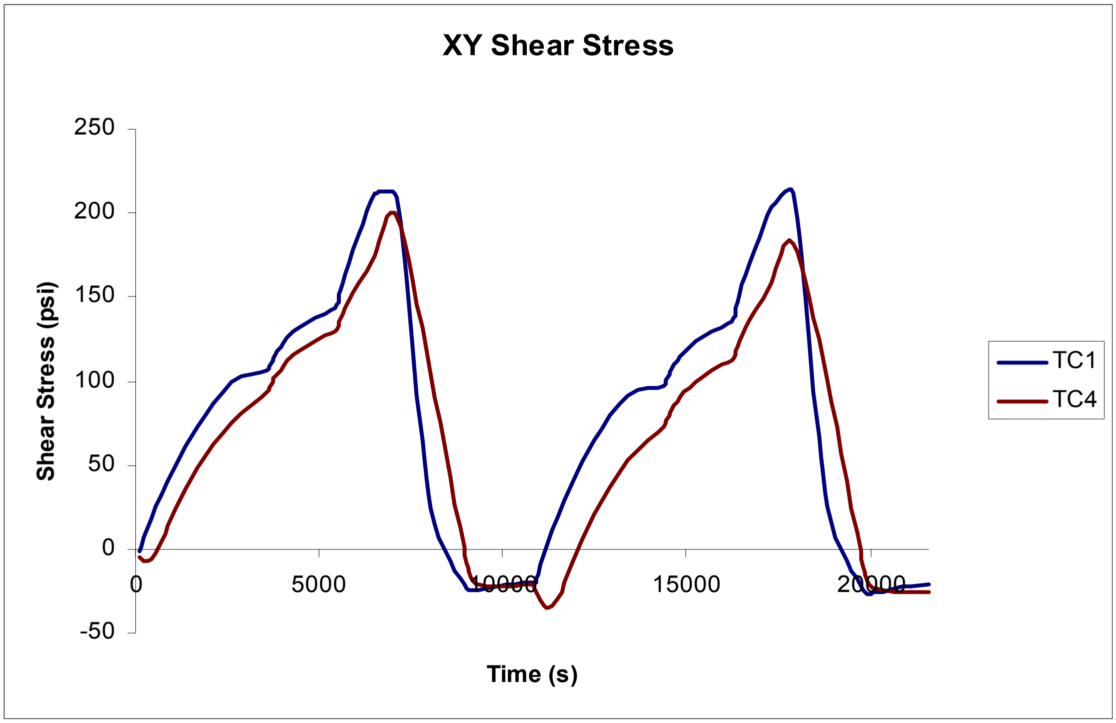


Figure 6.37: XY Shear stress plots of PBGA49 under TC1 and TC4 thermal profiles

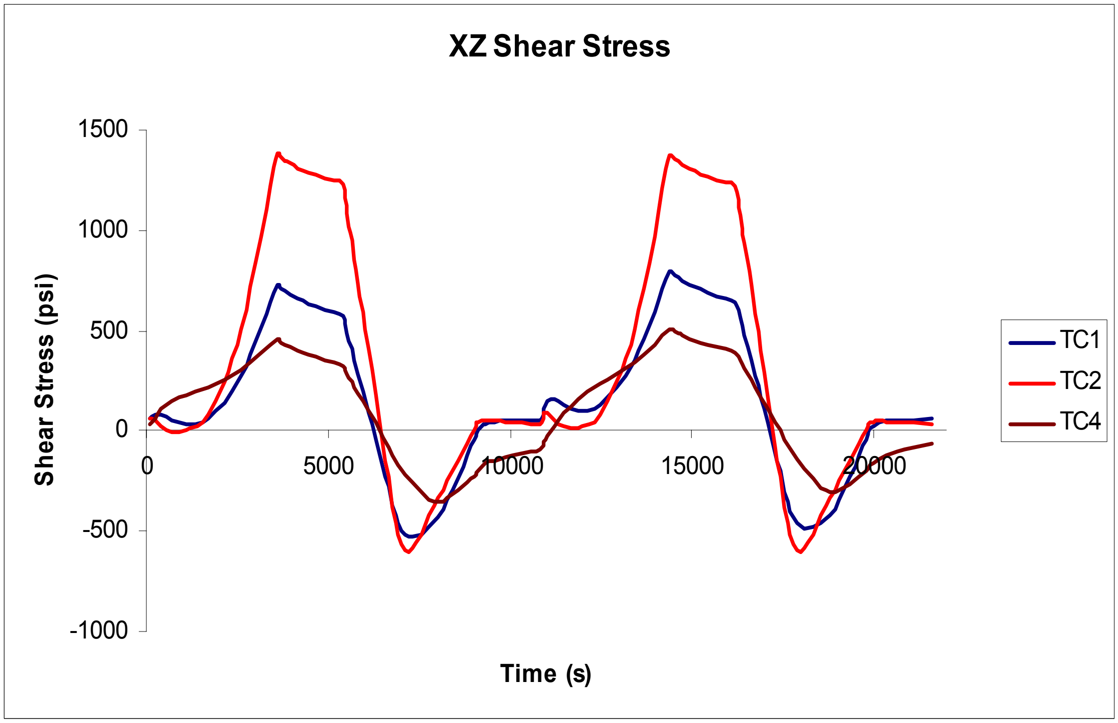


Figure 6.38: XZ Shear stress plots of PBGA49 under TC1, TC2, and TC4 thermal Profiles

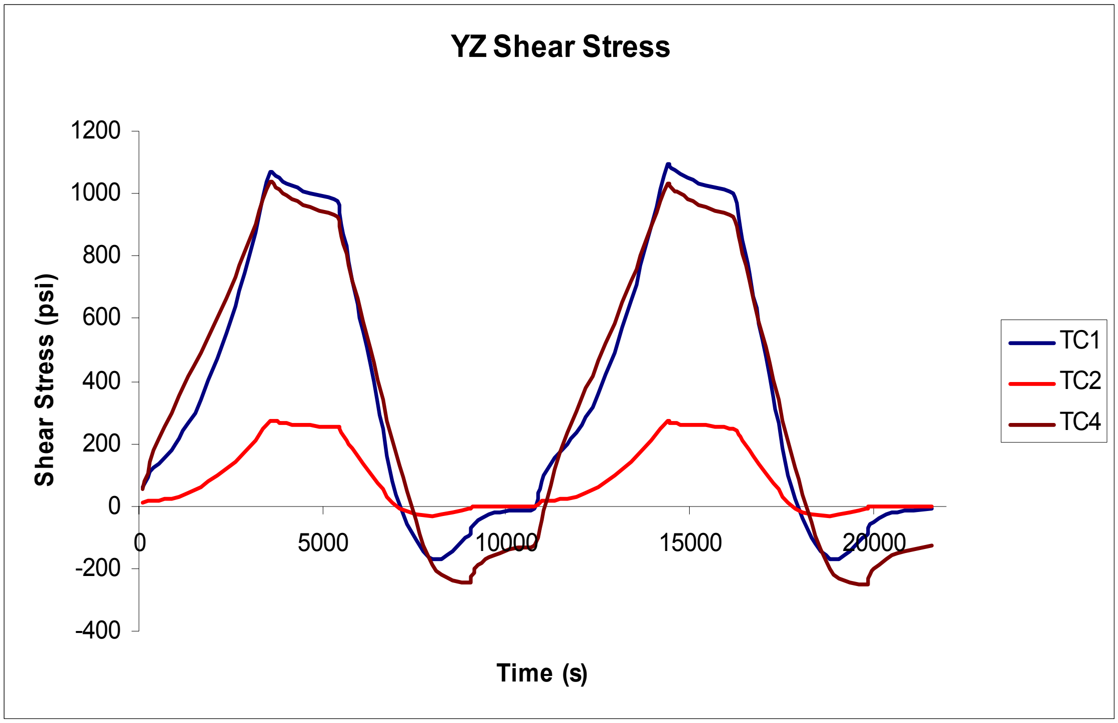


Figure 6.39: YZ Shear stress plots of PBGA49 under TC1, TC2, and TC4 thermal profiles

6.4 Hysteresis Loops

In figure 6.40, the shear stress and shear strain data from the simulation has been plotted against each other in order to analyze the hysteresis loops for the solder joints in PBGA 49. The hysteresis loop shows the amount of the non-linear plastic work accumulated by the solder joint during the thermal cycle. The inelastic strain energy density (ISED) accumulated by the solder ball during the thermal profiles can be calculated by finding the area enclosed within the hysteresis loop for a particular thermal cycle. The hysteresis loops also show how the solder joint acts when it is subjected to different thermal cycles. Vertical lines in hysteresis loops show the stress relaxation taking place during the dwell periods of the cycle. It is in this region where creep occurs within the solder ball. The regions where there are horizontal lines shows the plastic deformation happening during the ramps.

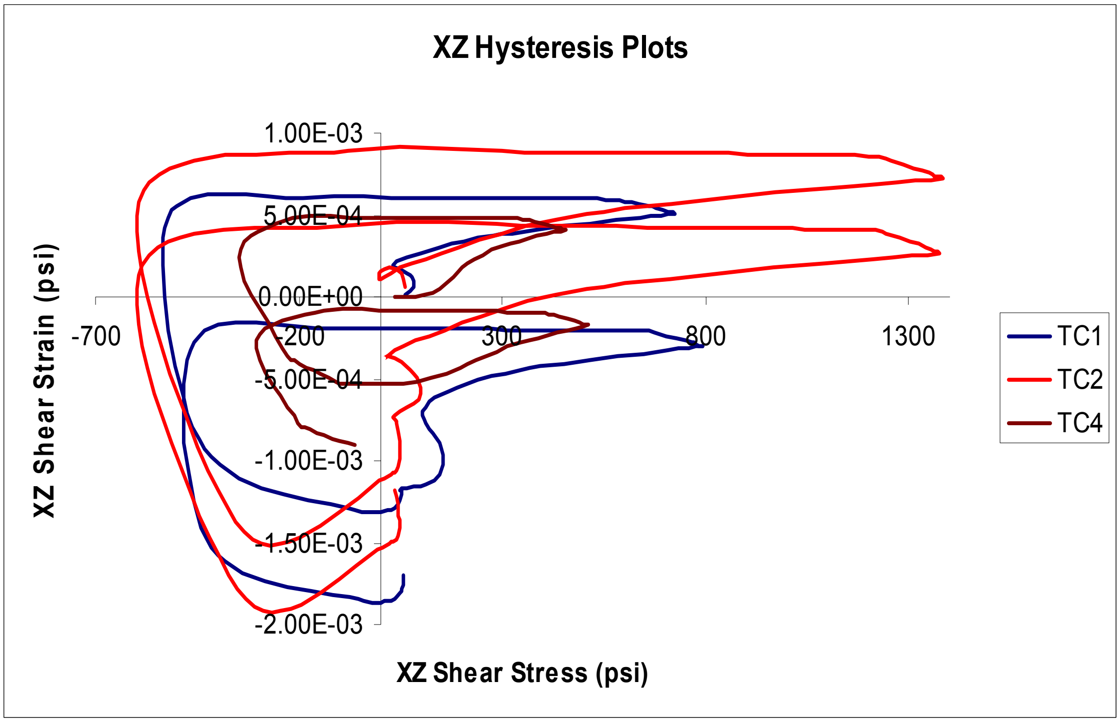


Figure 6.40: XZ Hysteresis Plots of PBGA 49 under TC1, TC2, and TC4 temperature Profiles

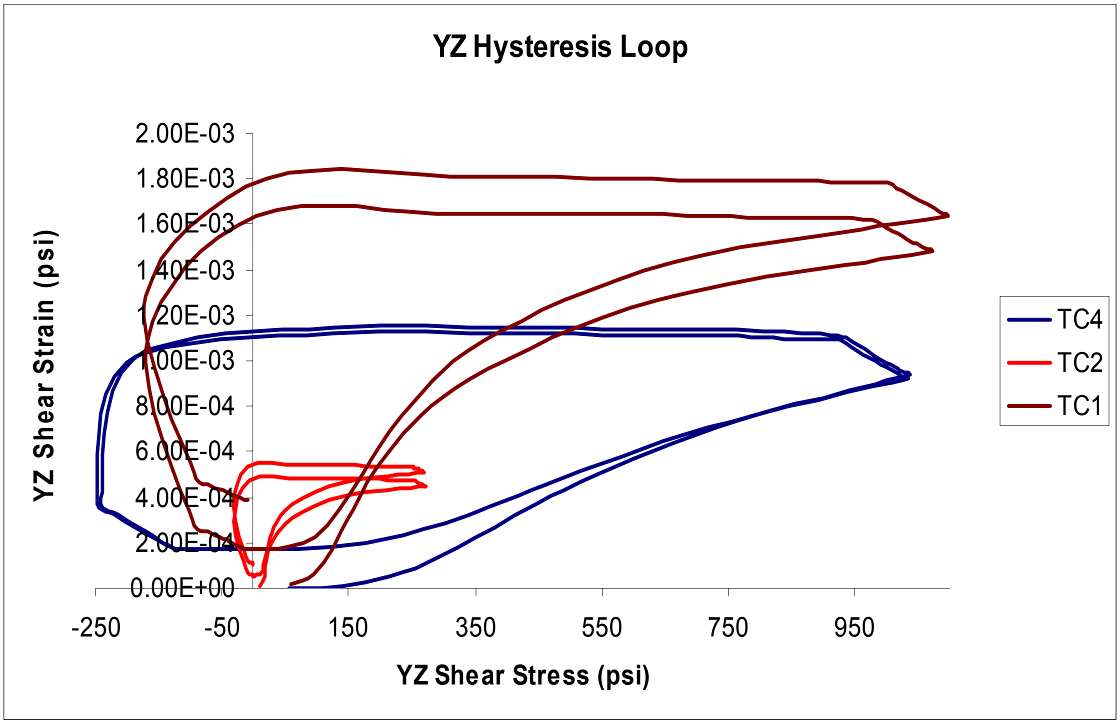


Figure 6.41: YZ Hysteresis loop TC1, TC2, and TC4

CHAPTER 7

STATISTICS BASED CLOSED FORM MODELS FOR PBGA PACKAGES

In this chapter, multi-variable regression and analysis of variance are used to analyze and quantify the effects that multiple independent variables have on a single dependent variable. This has been a very powerful, as well as an extremely useful, statistical technique for engineers in the past. It's been used to establish a mathematical relationship between an independent variable, such as characteristic life or number of cycles to 1% failure for a specific electronic package, and dependent variables, which affect the reliability of the package. It presents a methodology based on statistics of multi-variable regression for assessing and predicting the reliability of area array packages under harsh environments. The biggest advantage of this methodology, over finite element analysis, is that it allows the user to incorporate the effect of non-conventional predictor, or dependent, variables such as board finish, which can not be modeled using FEM, on the thermal reliability of the package. The results have been analyzed and correlated with FEM life predictions to develop meaningful closed form statistical models for application to area array package reliability. The results of these models have also been correlated and compared with the actual experimental failure data so that acceptable confidence levels can be gained in order to apply these models elsewhere.

7.1 Perturbation Methodology

The current work has been developed using a perturbation approach based on the statistical models developed from multivariate regression techniques. The first step of this methodology is to gather actual experimental failure data of various PBGA packages under accelerated thermal cycling tests. This data was gathered using numerous test boards as well as PBGA packages as described in Chapter 3. Weibull software, as described in chapter 9, was used to plot the failures for each package and board type, and the experimental data (number of cycles to 1% failure, β, and ή values) was gathered from these Weibull plots. It was then arranged in a large excel spreadsheet in the form of several datasets. The reliability criterion used for these models were the number of cycles for 1% of the total components to fail. This value, also referred to as N1%, has been used because it is a standard rule of thumb commonly followed in the automotive and aerospace industries for assessment and comparison of thermal reliability of the electronic components. Many conventional, as well as non-conventional predictor variables that are known to have an impact on the component reliability have also been included in the datasets. Die size, die to body ratio, package size, solder ball diameter, solder ball height, ball pitch, solder volume, board finish (HASL or ENIG), and ΔT are some of the parameters used.

In the second step of the perturbation methodology, statistical analysis of the entire datasets has been accomplished using MINITAB^{TM}, statistical analysis software. With this software, multi-variable regression and analysis of variance techniques have been used to quantify and analyze the relative influence that the predictor variables have on the thermal reliability of the electronic package. The output of the regression analysis and variance is then used to develop a mathematical equation which correlates the sensitivities of the predictor variables with the number of cycles until1% failure occurs. The final equation retains only the significant variables after analyzing the sensitivities of the predictor variables. Since multi-collinearity does exist between a few of the variables, the reliability data has been analyzed using the Pearson correlation coefficient matrix of the predictor variables. In statistics, a sequence or a vector of random variables is heteroscedastic if the random variables have different variances. The residuals have also been analyzed and verified for heteroscedasticity in the data, which can be shown in the residuals vs. fit plots. One of the basic assumptions for regression analysis is the normal distribution of the residuals, and this has been ensured as well.

After the mathematical equation is established and validated with the actual failure data with a significant level of confidence, only then can it be used for perturbing a select few, or all, parameters against the existing datasets for evaluation of various design options. This allows the user to analyze the various effects that each parameter has on the reliablity of the package. Then, the model can also be used to perform trade-offs with confidence within the frame of given datasets in order to achieve a specified level of thermo-mechanical reliability for any package under a given thermal cycling condition, or ΔT. Therefore, this methodology gives the user a "turn-key" approach, or tool, in making a final decision on the various package design parameters such as package size, die size, ball count, board finish, package size, ball pitch, ball count, and PCB thickness.

7.2 Model Library

This work includes several different types of statistical models to predict the thermal reliability of PBGA electronic packages. Both linear and non-linear models have been studied in order to determine the best model to use for predicting life with various component parameters. Both the linear and non-linear models are shown in equations 7.1

$$\text{Linear:} \qquad t_{63.2\%} = a_0 + \sum_{k=1}^{n} b_k f_k \qquad (7.1)$$

$$\text{Log:} \qquad t_{63.2\%} = a_0 \prod_{k=1}^{n} (f_k)^{b_k} \qquad (7.2)$$

and 7.2. The number of cycles for 1% failure to occur for different package parameters of PBGA packages has been used to predict, as well as to compare, the thermo-mechanical reliability of the various package configurations subjected to various temperature extremes.

7.3 Linear Models

After running the diagonal slice models using finite element analysis, the vendor for this work wanted another type of model they could use in order to compare various parameters of electronic packaging and predict their reliability. Multi-variable regression analysis was used on the collected data sets to generate a linear relationship between the cycles to 1% failure and the predictor variables. In order for this to be done, a mathematical equation must be used in which the user can input various parameters and output the number of cycles to 1% failure. Using linear statistical models for this assumes that the life of the electronic package is linearly related to the various design parameters. For linear statistical models, the mathematical relation is shown in the form of equation 7.3

$$N_{1\%} = a_0 + a_1(\text{Param1}) + a_2(\text{Param2}) + \ldots + a_N(\text{ParamN}) \qquad (7.3)$$

where,

'$N_{1\%}$' is the number of cycles until 1% failure occurs, also referred to as the response or dependent variable.

'Param1', 'Param2'… 'ParamN' are the design parameters which influence the package's life, also referred to as the predictor or independent variables.

'a_0' is constant and 'a_1', 'a_2', … 'a_N' are the coefficients of the design parameters, also referred to as the generalized degrees of freedom in the problem definition.

7.4 Log-Linear Model-1

The first log-linear model created was developed with the maximum number of predictor variables, or parameters, in order to analyze the effect of each variable on the reliability of the package. The statistical model represented by the mathematical equation is given by equation 7.4

$$\begin{aligned}\ln\left(N_{1\%}\right) = {} & A_0 + A_1(\ln \mathrm{BrdFinish}) + A_2(\ln \mathrm{DiagLenMM}) \\ & + A_3(\ln \mathrm{BallCount}) + A_4(\ln \mathrm{PkgPadDiaMM}) \\ & + A_5(\ln \mathrm{BallDiaMM}) + A_6(\ln \mathrm{DeltaT})\end{aligned} \qquad (7.4)$$

Where, A_0, A_1, …, A_6 are generalized degrees of freedom in the problem definition. The prefix ln indicates a natural log of the value. The various predictors used in this model are lnBrdFinish (HASL or ENIG), lnDiagLenMM (measurement of the diagonal length of the package), lnBallCount is the number of I/O, lnPkgPdDiaMM (PCB pad diameter), lnBallDiamMM (solder ball diameter), and lnDeltaT is the change in temperature (°C). LnBrdFinish switches between the two different board finishes that were studied in these statistical models.

Values of 1 and 2 were used because the ln(0) is undefined. The coefficient of each of the variables shown in equation (7.4) defines the sensitivity of that parameter on the thermal reliability of the electronic package. If there is a negative sign in front of the design parameter, or variable, this indicates a decrease in the number of cycles to 1% failure with an increase in value of that variable. The numerical values of these coefficients, or generalized degrees of freedom, for this model are listed in the 'Coefficients' column of Table 7.1.

Table 7.1: Model Parameters and Analysis of Variance for Multi-variable Regression Log-linear Model-1

Predictors ($\ln a_0, f_k$)	**Coeff** (b_k)	**SE Coeff**	**t**	**p-Value**
Constant	17.363	1.039	16.71	0
lnBrdFinish	0.07868	0.05153	1.53	0.13
lnDiagLenMM	-0.5135	0.12	-4.28	0
lnBallCount	-0.19368	0.06709	-2.89	0.005
lnPkgPdDiaMM	2.3317	0.4298	5.43	0
lnBallDiaMM	-0.6917	0.256	-2.7	0.008
lnDeltaT	-1.2862	0.1595	-8.06	0

S = 0.2538 R-Sq = 61.4% R-Sq(adj) = 59%

7.4.1 Model Diagnostics of Log-Log Model-1

The model parameters for the log-linear model-1 have been shown in table 7.1. However, after further analysis of the model parameters, the model's R-Sq and R-Sq(adj) values indicate that only 59-61.4% of the variation in the reliability data is explained by the model. This is lower than the 75-90% goal that was trying to be reached. For a prediction model, target R-Sq values of 75% or better are a must. This model indicates that 62.1% of variation in the reliability data is explained by the regression model. From failure mechanics theory we know that board finish has a significant effect on the package reliability. Therefore the predictor variable has been retained in the regression even though it is statistically significant at a lower confidence level of 87%. Various model forms have been developed based on multicollinearity considerations to enable specification of different predictor variable sets and measure their response on reliability.

Figure 7.1 shows the residual plots for the log-linear model-1. Since the linear regression is based on the assumption of normal random distribution of the residuals, it is extremely important to look at the distribution of the residuals in order to make sure that the basic assumption is not violated. It is also important to check if there is any heteroscedasticity in the data. This means that the standard deviation in the distribution of the dependent variable varies with the value of the independent variable. The residual plots, shown in the Figure 7.1, help check whether the model complies with all these.

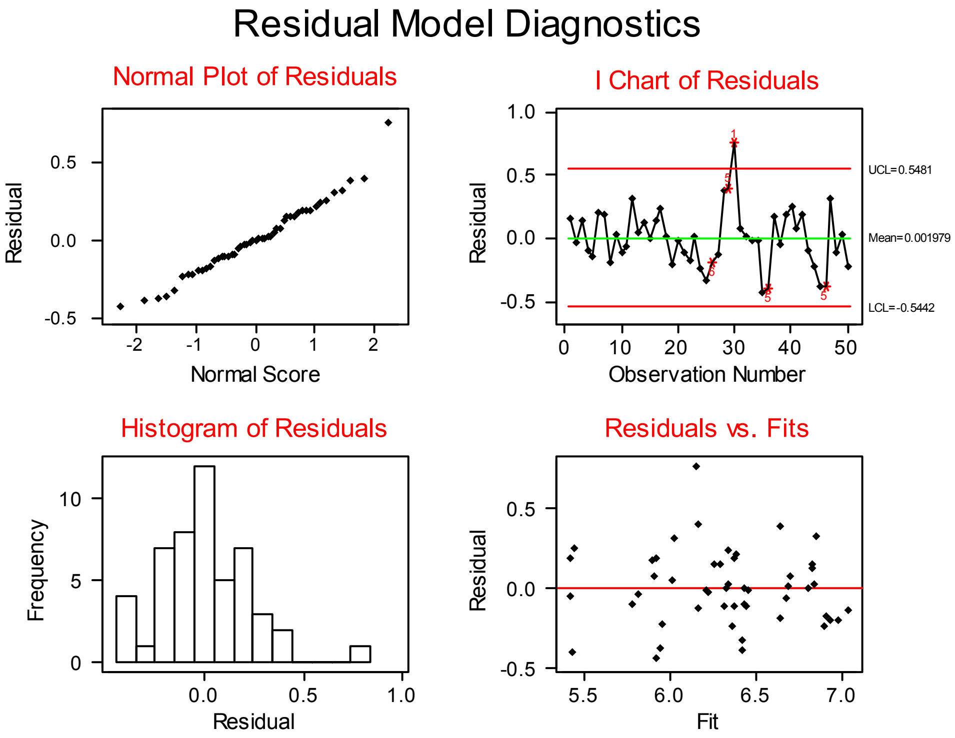


Figure 7.1: Residual plots for the log-log model-1

assumptions. The normal plot of the residuals shows the residuals plotted against the normal score. This plot should be a straight line at an angle of approximately 45°. The histogram of the residuals should be a symmetrical bell-shaped curve if the residual distribution is normal. In the plot for the log-linear model-1, it is bell-shaped, however it is not very symmetrical. The I-chart of the residuals is used to verify that the residuals for all the predicted values of the model are within the control limits of 3 sigma. All but one point in these plots for this model are within the limits. The residual-vs-fit plot is used to check if the failure data holds the assumption of homoscedasticity (constant variance). In case there is any heteroscedasticity than the residuals either fan out or follow some pattern as we go from the lower fits to the higher fitted values. Analyzing the residual plots of the log-linear model-1 it can be concluded that the distribution of the residuals is not very close to normal, and there is some heteroscedasticity in the data, also all the residuals are not within the control limits of 3-sigma. These findings led to the log-linear model-2.

7.5 Log-Log Model-2

Modified log models have been developed based on a truncated sub-set of parameters from the global set. However, the high p-values and poor model efficiency, low R-Sq and R-Sq(adj) values, can be attributed to multi-collinearity between other predictor variables in the reliability data. So the correlation coefficient matrix of the predictor variables was plotted and the correlation coefficients were checked for any multi-collinearity. It was found that lnPkgWtG was highly correlated with lnDieSqMM and lnBallHgtMM. Also, lnBallPitchMM and lnBallCount were found to be highly correlated as well. These findings led to the modified log-linear model, log-linear model-2.

Cook's Distance

Modified linear models have been developed based on a truncated sub-set of parameters from the global set. Certain data points were identified as outliers as a result of high residual absolute values of three standard deviations from the mean, and from large values of Cook's Distance. To help aid in truncating the data, Cook's distance was used to eliminate outlying data sets. In statistics, the Cook's distance is a commonly used estimate of the influence of a data point when doing least squares regression. Data values which are outliers and leverage points may distort the outcome and accuracy of a regression. The general equation for determining Cook's Distance is given by

$$D_i = \frac{(\hat{\beta}_{(i)} - \hat{\beta})' X'X(\hat{\beta}_{(i)} - \hat{\beta})}{pMS_E}, \quad i = 1,2,..n \tag{7.5}$$

where D_i is Cook's Distance, X is an n-by-p matrix of regressors, $\hat{\beta}$ is the least squares estimate, p is the confidence interval, and MS_E is the residual mean square [Montgomery 1992]. Points with a Cook's distance of 1 or more are considered to merit closer examination in the analysis.

Pearson Correlation Coefficient

In statistics, the Pearson product-moment correlation coefficient (sometimes known as the PMCC) (*r*) is a measure of the correlation of two variables *X* and *Y* measured on the same object or organism, that is, a measure of the tendency of the variables to increase or decrease together. It is defined as the sum of the products of the standard scores of the two measures divided by the degrees of freedom. The equation for determinging the Pearson Correlation Coefficient is given by

$$r = \frac{\sum XY - \frac{\sum X \sum Y}{N}}{\sqrt{\left(\left(\sum X^2 - \frac{\sum X^2}{N}\right)\left(\sum Y^2 - \frac{\sum Y^2}{N}\right)\right)}} \qquad (7.6)$$

where X and Y are two variables being compared and N is the sample size[Montgomery 1992]. Equation 7.6 can be simplified by turning the numbers into z scores to get

$$r = \frac{\sum Z_x Z_y}{n-1} \qquad (7.7)$$

The statistical model in the form of mathematical equation is given by equation 7.8.

$$
\begin{aligned}
\ln\left(N_{1\%}\right) = A_0 &+ A_1\left(\ln \text{BrdFinish}\right) + A_2\left(\ln \text{DiagLenMM}\right) \\
&+ A_3\left(\ln \text{DietoBodyRatio}\right) + A_4\left(\ln \text{BallCount}\right) \\
&+ A_5\left(\ln \text{PkgPadDiaMM}\right) + A_6\left(\ln \text{BallDiaMM}\right) \\
&+ A_7\left(\ln \text{SdrVol}\right) + A_8\left(\ln \text{DeltaT}\right)
\end{aligned}
\tag{7.8}
$$

The parameters in equation 7.8 begin with ‘ln’ showing that the natural log of each parameter was used in this equation. Also, the parameters in equation 7.8 ending with MM indicate that these parameters lengths are measured in millimeters. The various predictors used in this model were BrdFinish (HASL or ENIG), DiagLenMM(measurement of the diagonal length of the package), DietoBodyRatio (ratio of die size to body size), BallCount, PkgPadDiamMM (PCB cu pad diameter that solder ball mounts to), BallDiamMM (solder ball diameter), SdrVol (volume of the solder paste in cu mils), and DeltaT (change in temperature °C).

LnBrdFinish switches between the two different board finishes that were studied in these statistical models. Values of 1 or 2 were used to switch between HASL and ENIG finishes. Values of 1 and 2 were used because the ln(0) is undefined. The coefficient of each of the variables shown in equation (7.8) defines the sensitivity of that parameter on the thermal reliability of the electronic package. If there is a negative sign in front of the design parameter, or variable, this indicates a decrease in the number of cycles to 1% failure with an increase in value of that variable. The numerical values of these coefficients, or generalized degrees of freedom, for this model are listed in the ‘Coefficients’ column of Table 7.2.

Table 7.2: Model Parameters and Analysis of Variance for Multi-variable Regression Log-Linear Model-2

Predictors (ln a_0,f_k)	**Coeff** (b_k)	**SE Coeff**	**t**	**p-Value**
Constant	17.539	1.182	14.83	0
lnBrdFinish	0.12444	0.04518	2.75	0.007
lnDiagLenMM	-0.3209	0.2092	-1.53	0.129
lnDieToBodyRatio	-0.3441	0.2192	-1.57	0.121
lnBallCount	-0.39305	0.09465	-4.15	0
lnPkgPdDiaMM	2.2066	0.432	5.11	0
lnBallDiaMM	-0.517	0.3376	-1.53	0.13
lnSdrVol	0.04716	0.08042	0.59	0.559
lnDeltaT	-1.4292	0.1387	-10.31	0

S = 0.2007 R-Sq = 75.90% R-Sq(adj) = 73.40%

Table 7.3: Pearson correlation coefficient matrix for the predictor variables of the log-linear model-2

	lnBrdFinish	lnDieSqM	lnDiagLe	lnDieToB	lnBallCo	lnBallDi	lnBallHg	lnSdrVol
lnDieSqMM	0.015							
lnDiagLength	0.006	0.954						
lnDieToBody	-0.14	-0.038	0.005					
lnBallCount	0.097	0.824	0.806	-0.405				
lnBallDiamMM	0.056	0.778	0.821	-0.311	0.706			
lnBallHgtMM	0.096	0.745	0.815	-0.311	0.714	0.938		
lnSdrVol	0.098	0.718	0.734	-0.446	0.8	0.871	0.88	
lnDeltaT	-0.083	0.041	0.044	-0.115	0.072	0.065	0.037	0.091

7.5.1 Model Diagnostics of Log-Linear Model-2

The model parameters for the log-linear model-2 have been shown in table 7.2. Analysis of the modified log-linear model results shows that this model allows for higher values and better explains the variation in the reliability data. The trends in the coefficients column make sense. The negative sign in front of the coefficient in the DeltaT column says that as ΔT increases, the life, or reliability, of the package decreases. Also, looking at PkPadDiam, the lack of a negative sign tells us that as the package pad diameter increases, the life, or reliability, of the electronic package increases. From failure mechanics theory we know that these variables have significant effect on the package reliability. These trends help solidify this statistical model's relevance.

Analysis of this modified log linear model also shows that there is a huge improvement in the p-values (from Table 7.2) of the predictor variables lnBrdFinish, lnBallCount, lnDiagLenMM, lnDietoBodyRatio, lnPkgPdDiam, lnBallDiamMM, lnSdrVol, and lnDeltaT. The *p*-values for lnBallDiam and lnSdrVol are still greater than the significance level of 5%, which means they are statistically significant at a lower confidence level.

Figure 7.2 shows the residual plots for the log-linear model-2. Since the regression is based on assumption of normal distribution, the nature of distribution of the residuals has been verified. Residual plots of the statistical model are shown in Fig. 1. If we plot the residuals against the normal score of the residuals then a perfectly normal

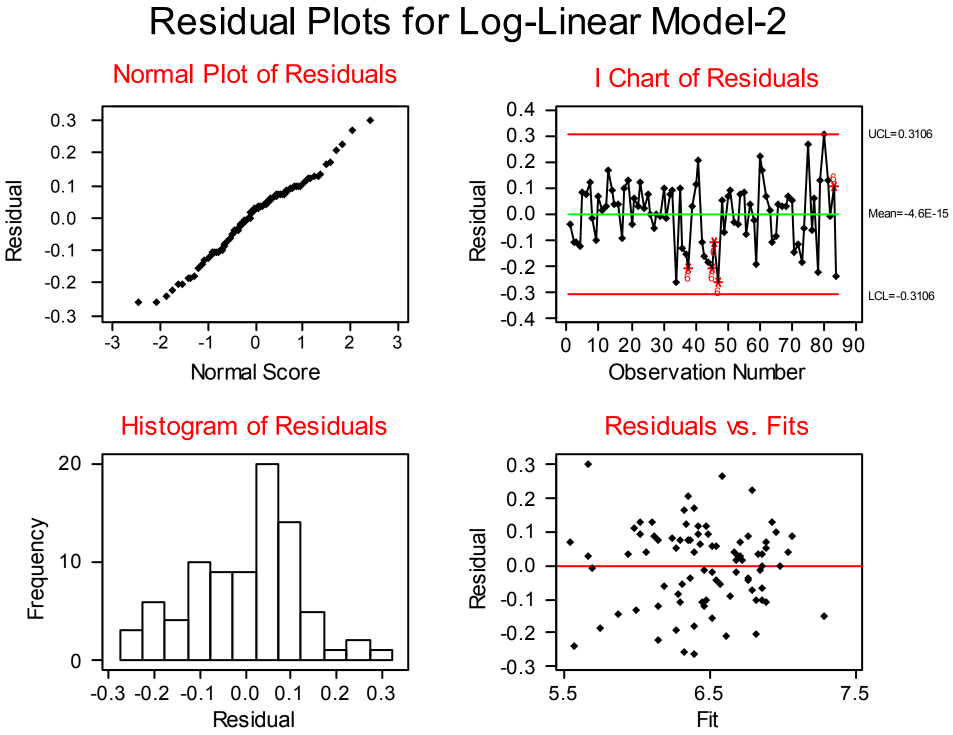


Figure 7.2: Residual plots for log-log model-2

distribution is represented by a straight line at 45 on the normal plot of the residuals. The normal plot of residuals for this model indicates a fairly normal distribution of the residuals as it is quite close to a straight light at 45° (Figure 7.2). The histogram plot of residual versus frequency also exhibits a nearly symmetrical bell-shape pattern, which is consistent with a sample from a normal distribution. The I-chart of individual observations reveals that the residuals for all the observations are within the three sigma limits of (0.2175, 0.2175) which implies that all the data points in our analysis are fitted within the control limits of 3 sigma. We can see fairly random distribution of the residuals in the residual versus fits plot, which demonstrates the linear relationship between the predictors and the response variable in the model. If the relationship is not linear than the residuals follow some curved pattern distribution. The plot also holds the assumption of constant variance in the data as the residuals do not fan out or show any pattern as we go from the lower fits to the higher fitted values.

7.6 Correlation of Statistical Model with Experimental Data

The number of cycles until one percent failure values that are predicted by the statistical model have been plotted against the actual values obtained from the experimental data in order to assess the "goodness of fit" of the statistical model. The best fit linear model was used for the comparison of the accuracy of the prediction of these models. Figure 7.3 shows the plot for the log-linear model-2. The straight line at 45° in this figure represents the local of points for which the predicted values match exactly to the experimental values. In other words, the closer the data points are scattered to this line, the more accurate the model predictions.

Looking at figure 7.3, one can see that the data points are all either on the line or hovering right around the line at 45°. Therefore, the log-linear model-2 is an accurate model and can be used for analyzing the sensitivity of the various design parameters on the PBGA packages and even for life prediction.

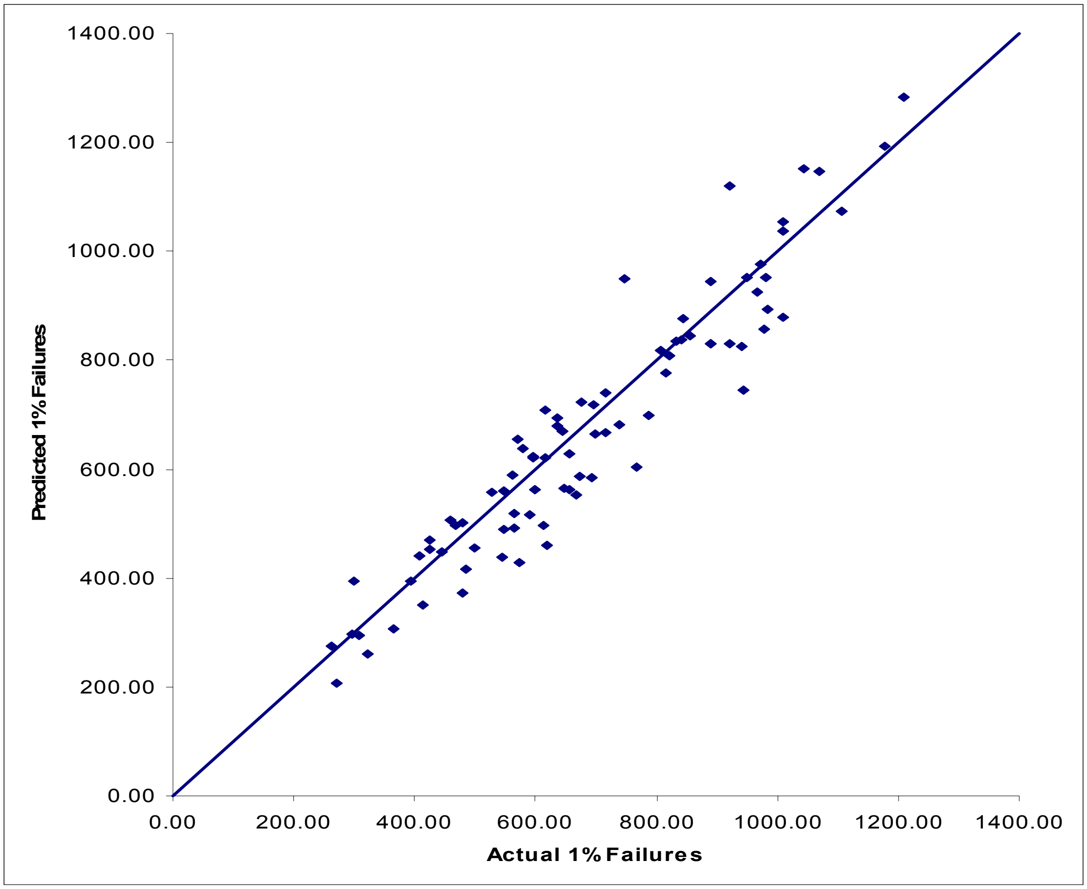


Figure 7.3: Plot of experimental vs. predicted 1% cycles to failure for the Log-Log Model-2

CHAPTER 8

STATISTICAL MODEL VALIDATION FOR PBGA PACKAGES

Experimental data has been correlated with the statistical model in order to develop confidence in the accuracy of the model presented in chapter 7. In this chapter, sensitivity factors for various design parameters from the statistics based models have been validated against the sensitivity factors from the actual accelerated test failure data for various configurations of plastic ball grid array packages subjected to harsh environments. Various design parameters have been shown to have a major impact on the reliability of particular electronic packages. This chapter analyzes and quantifies these effects and creates guidelines for future vendors to use when designing and selecting package architectures and board attributes for applications in these temperature conditions such as aerospace, automotive under-hood, and military applications.

8.1 Model Validation

The effects of various design parameters on the thermal reliability of the package has been used for validating the model as well as for comparing the model predictions to the actual accelerated thermal cycling failure test data. Failure mechanics and statistics based sensitivity factors quantifying the effects of design, material, architecture, and environmental parameters on thermal fatigue reliability, have been used to predict, or, compute, life. Predictions of sensitivities have been validated against the experimental test data. The Log-Linear Model-2 from Chapter 7 has been used for perturbation of the failure data for validation of the predicted values.

8.1.1 Ball Count

The effect of ball count, or number of I/O interconnects, has been investigated in this section. Experimental data shows that thermal reliability decreases with the increase of ball count in PBGA electronic packages. The experimental data used for the correlation includes 196, 324, and 672 ball count PBGA packages. Figure 8.1 shows that there is a close correlation between experimental and the statistics-based model predictions. The sensitivity of the package reliability to the ball count has also been shown, table 8.1, and the number of cycles to 1% failure for the different packages predicted by the model along with the actual failure data.

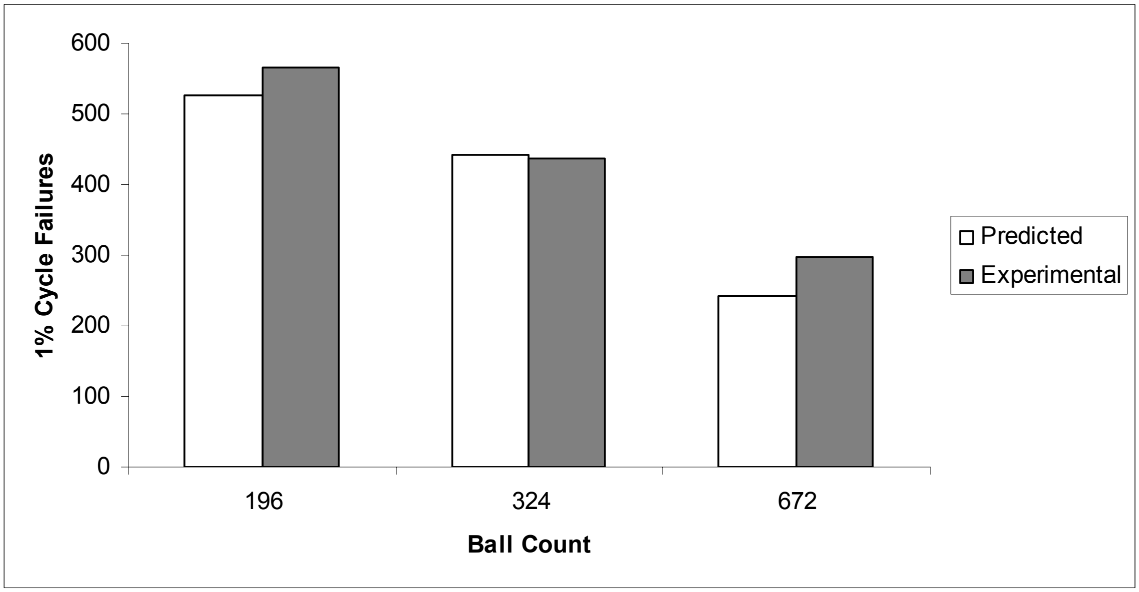


Figure 8.1: Effect of ball count on thermal reliability of PBGA packages subjected to -55°C to 125°C thermal cycle

Table 8.1: Sensitivity of package reliability of ball count and comparison of statistical model predictions to actual experimental data.

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Ball Count	**Model**	**Experimental**	**Sensitivity Factor for Ball Diam.**
196	527	567	-0.393
324	443	438	
672	242	297	

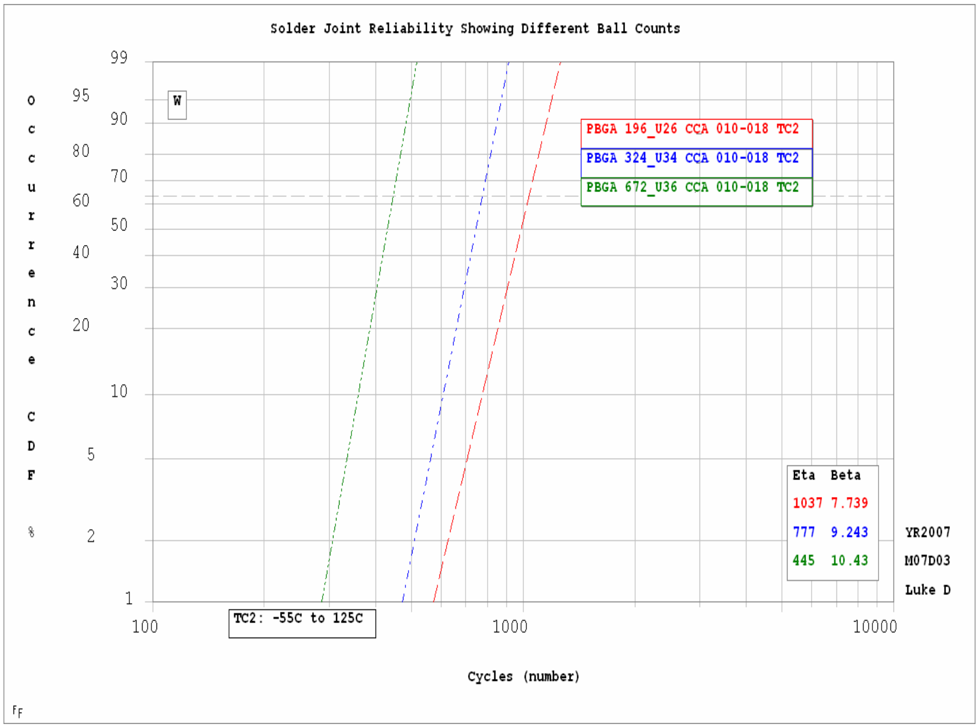

Figure 8.2: Weibull Distribution showing experimental data correlation with model predictions

8.1.2 Die to Body Ratio

The die-to-body ratio, also known as the packaging density, of an electronic package is defined as the ratio of the die size to the package body size. The general trend for this parameter is that the reliability of a ball grid array package generally decreases with the increase in the die-to-package ratio. This effect has been demonstrated in both rigid substrate as well as flex substrate packages. Die to body ratio of experimental thermal reliability data of PBGA packages from -55°C to 125°C (TC2) with 30 minute dwells has been correlated with the statistical model predictions for 7mm 12mm 15mm, and 17mm with varying die sizes. The cycles for 1% failure from the experimental data and the statistical model have been plotted against the die to body ratio of the various packages. Figure 8.3 shows that there is a close correlation between experimental and the statistics-based model predictions. Also, the general trend of increase in the ball die to body ratio of a package decreases the thermal reliability of the package can be seen from the plot in figures 8.3 through 8.6, which is also in agreement with the failure mechanics theory. The sensitivity of the package reliability to the die to body ratio has also been shown, table 8.2, and the number of cycles to 1% failure for the different packages predicted by the model along with the actual failure data. This helps solidify the model's validation in that the trends, showing a negative sign in front of the sensitivity factor, match what has been previously observed in earlier studies.

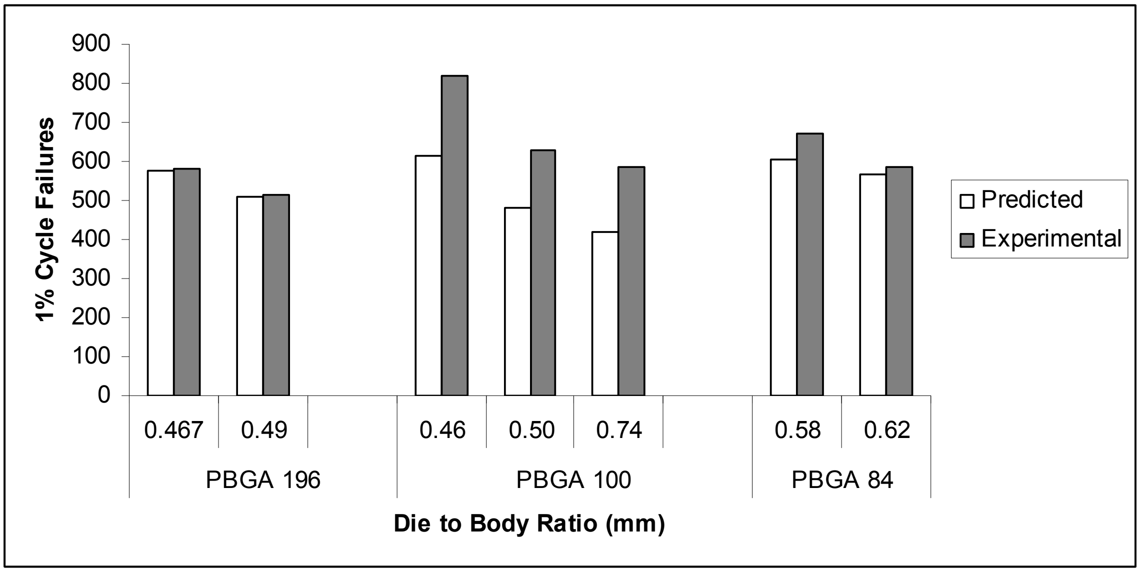

Figure 8.3: Effect of die-to-body ratio on thermal reliability of PBGA packages coupled with package type, ball count, surface finish, package size, and TC2 thermal cycle

Table 8.2: Sensitivity of package reliability of die to body ratio and comparison of statistical model predictions to actual experimental data

Package	Die to Body Ratio	Model	Experimental	Sensitivity Factor for Die to Body Ratio
PBGA 196	0.467	574	583	-0.3441
	0.49	508	515	
PBGA 100	0.46	615	818	
	0.50	480	629	
	0.74	419	588	
PBGA 84	0.58	603	670	
	0.62	567	587	

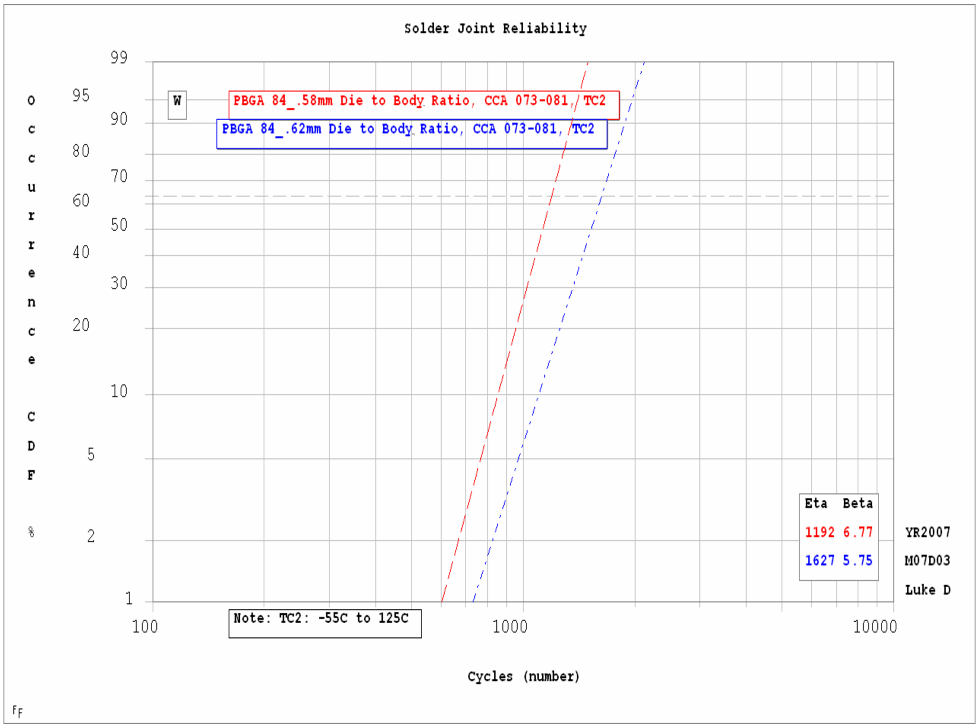

Figure 8.4: Weibull distributions of PBGA 84 with various die sizes

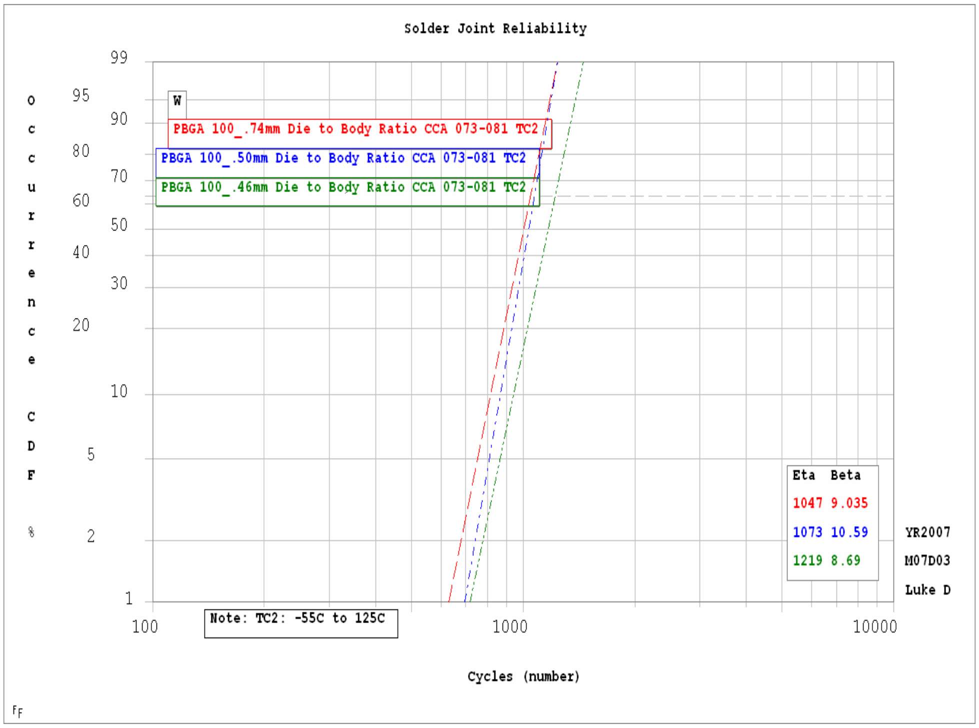

Figure 8.5: Weibull distributions of PBGA 100 with various die sizes

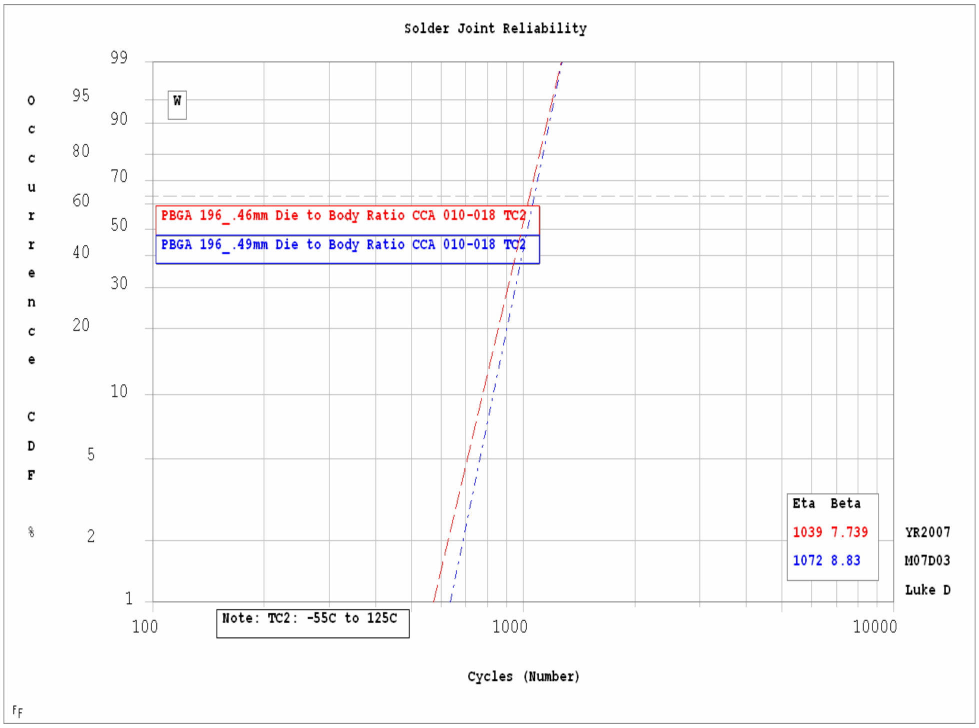

Figure 8.6: Weibull distributions for PBGA 196 with varying die sizes.

8.1.3 Ball Diameter

The solder joint diameter has a pronounced effect on the thermal reliability of the PBGA packages. Experimental thermal reliability data has been compared with the statistical model predictions. PBGA packages evaluated include solder ball diameters of 0.48 mm, 0.54 mm, and 0.80mm. The plot in figure 8.7 shows the correlation of 1% failure cycles for PBGAs with variable ball diameters. Experimental data shows that the increase in the ball diameter leads to a decrease in the thermal reliability of the package. This has been studied in the past, especially with column grid arrays (CGA) where the solder joint is made as tall as possible in a column shape, as opposed to a ball shape. This trend is in compliance with the theory of failure mechanics as the increase in the solder joint diameter decreases the distance between the substrate and the PCB, allowing for less flexibility, or more rigidity, in the joint for thermal expansion, resulting in decreased thermal reliability. The sensitivity of the package reliability to the solder joint height has also been shown, table 8.3, and the number of cycles to 1% failure for the different packages predicted by the model along with the actual failure data.

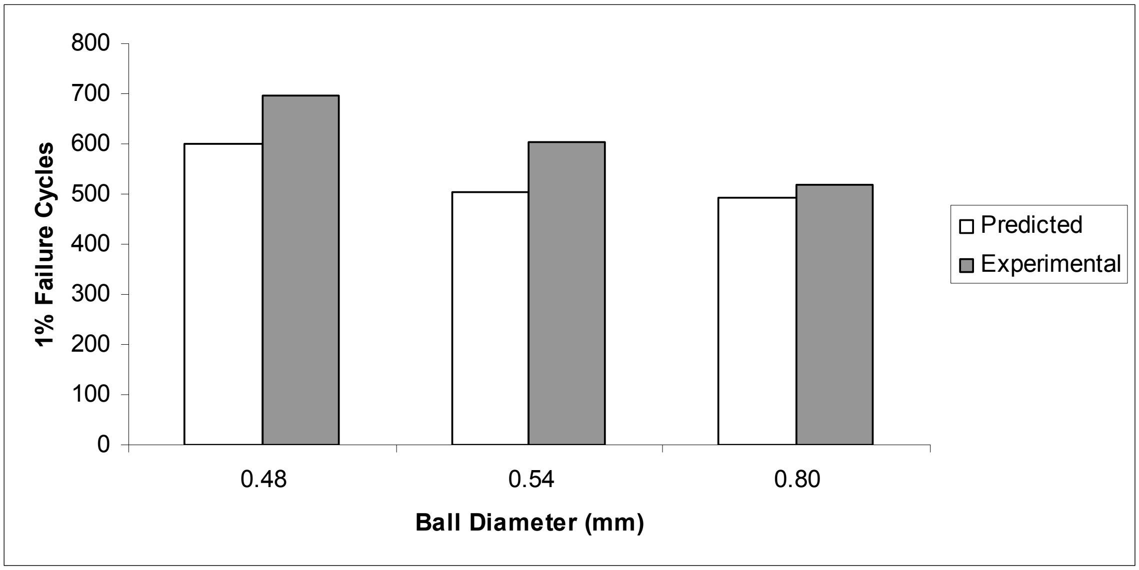

Figure 8.7: Effect of ball height on thermal reliability of PBGA packages subjected to -55°C to 125°C thermal cycle

Table 8.3: Sensitivity of package reliability of ball diameter and comparison of statistical model predictions to actual experimental data

Ball Diam (mm)	**Model**	**Experimental**	**Sensitivity Factor for Ball Diam.**
0.48	601	698	-0.517
0.54	503	605	
0.80	493	519	

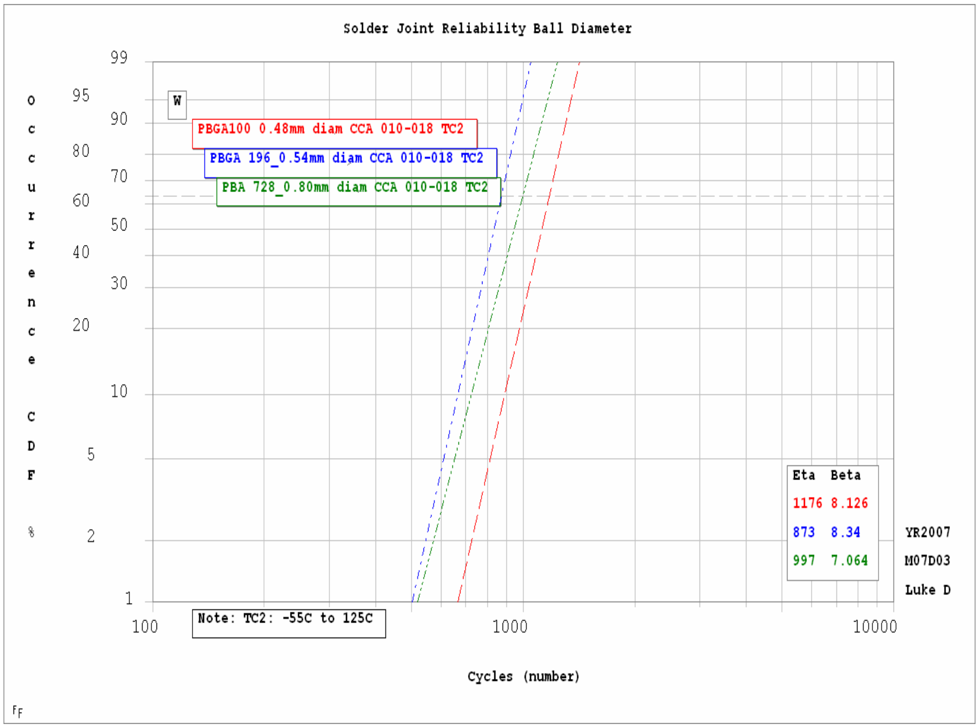

Figure 8.8: Weibull distribution for varying solder ball diameters under TC2 thermal Cycle

8.1.4 Board Finish

The most commonly used board finishes for PCB surfaces these days are Eletroless Nickel Immersion Gold (ENIG), Organic Solder Protection (OSP), and Hot Air Solder Leveled (HASL). In this study, only HASL and ENIG surface finishes were used on the PBGA packages. Experimental data from previous studies, as well as Auburn's MECH6310 Mechanics of Electronic Packaging course, have shown that there is not really a huge difference in the thermal reliability for these two surfaces, however the ENIG surface finish tends to be slightly more reliable. Figure 8.9 shows a plot comparing the two surface finishes. For this plot, ΔT (TC2), ball count, die size, ball diameter, and ball height were all coupled in order to make a more accurate comparison of the two surface finishes. Figure 8.10 shows a weibull plot validating this trend. The main cause for the slight difference in the two finishes can be attributed to the different inter-metallic system formation for different board finishes. These inter-metallic systems induce different failure modes thus having a slightly different impact on the thermal reliability of the component. Figure 8.9 shows a close agreement between the experimental data and the predicted values from the statistical model. The sensitivity of the package reliability to the different types of board finishes has also been shown, table 8.4, and the number of cycles to 1% failure for the different packages predicted by the model along with the actual failure data.

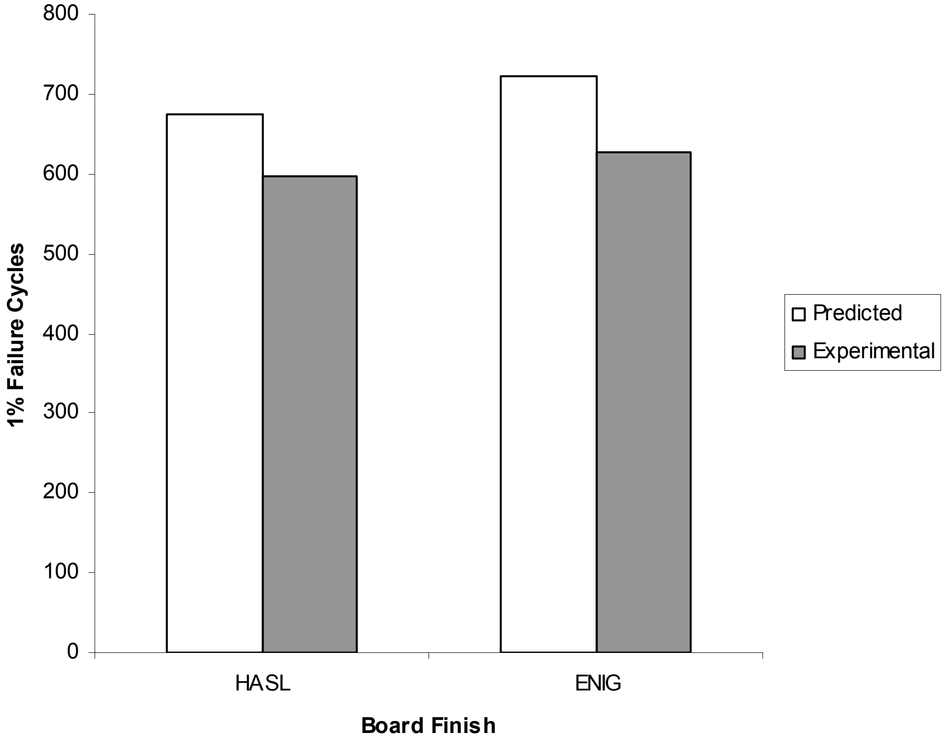

Figure 8.9: Effect of board finish on thermal reliability of PBGA packages coupled with ΔT (TC2), ball height, ball count, ball diameter, and die size

Table 8.4: Sensitivity of package reliability of different board finishes and comparison of statistical model predictions to actual experimental data

Board Finish	**Model**	**Experimental**	**Sensitivity Factor for Board Finish**
HASL	675	722	0.175
ENIG	598	626	

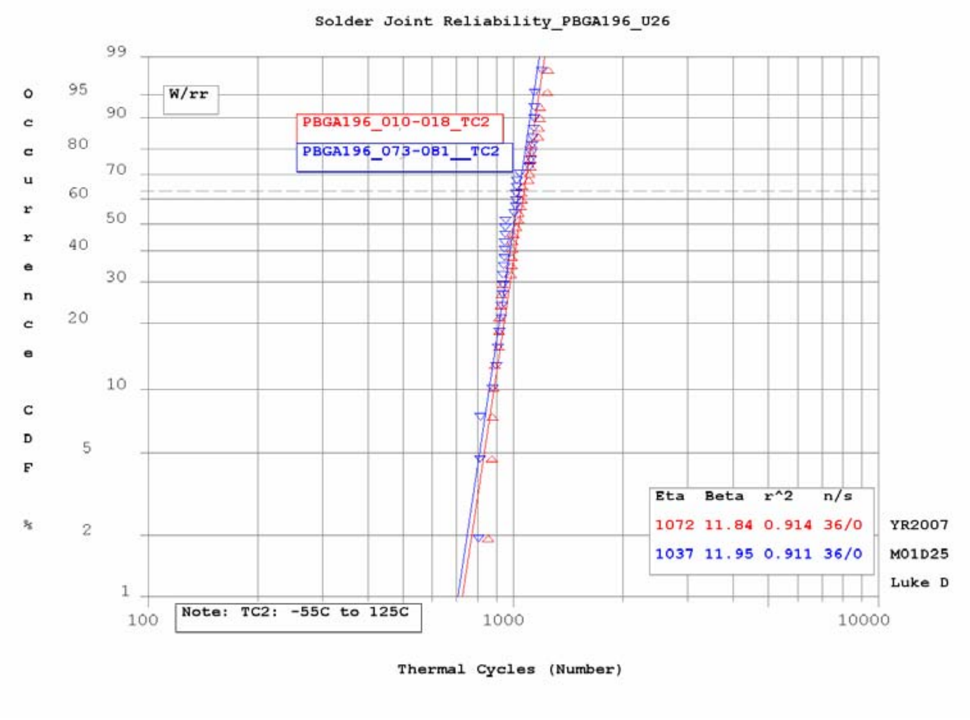

Figure 8.10: Weibull plot validating model with ENIG and HASL finishes under TC2 temperature profile

8.1.5 Temperature Cycle Condition (ΔT)

One of the largest determining factors in thermal cycle reliability is how large, or small, the ΔT value is for the thermal cycling profiles. From the use of multivariate regression analysis in MINITAB^{TM}, the sensitivity factor of the package's thermal reliability to the thermal cycling temperature range is able to be quantified. The theory behind why this is so important can be seen from failure mechanics. As was described in the introduction, thermal cycling causes varying coefficients of thermal expansions throughout the package to relax and contract at various rates causing large amounts of shear stress and strain through the electronic package. The three different temperature cycles used for comparisons are:

1. TC1: -40°C to 95°C (ΔT = 135)
2. TC2: -55°C to 125°C (ΔT = 180)
3. TC4: -20°C to 60°C (ΔT = 80)

From failure mechanics theory, we know, that as ΔT increases, the thermal reliability of the package greatly begins to decrease. This trend can be seen from the plot in figure 8.11. The plot also shows a close agreement between the experimental data and the predicted values from the statistical model. The sensitivity of the package reliability to the change in ΔT has also been shown, table 8.5, and the number of cycles to 1% failure for the different packages predicted by the model along with the actual failure data. This solidifies the trend that as ΔT increases, the reliability of the package decreases, as can be seen by the negative sign in front of the sensitivity factor in table 8.5

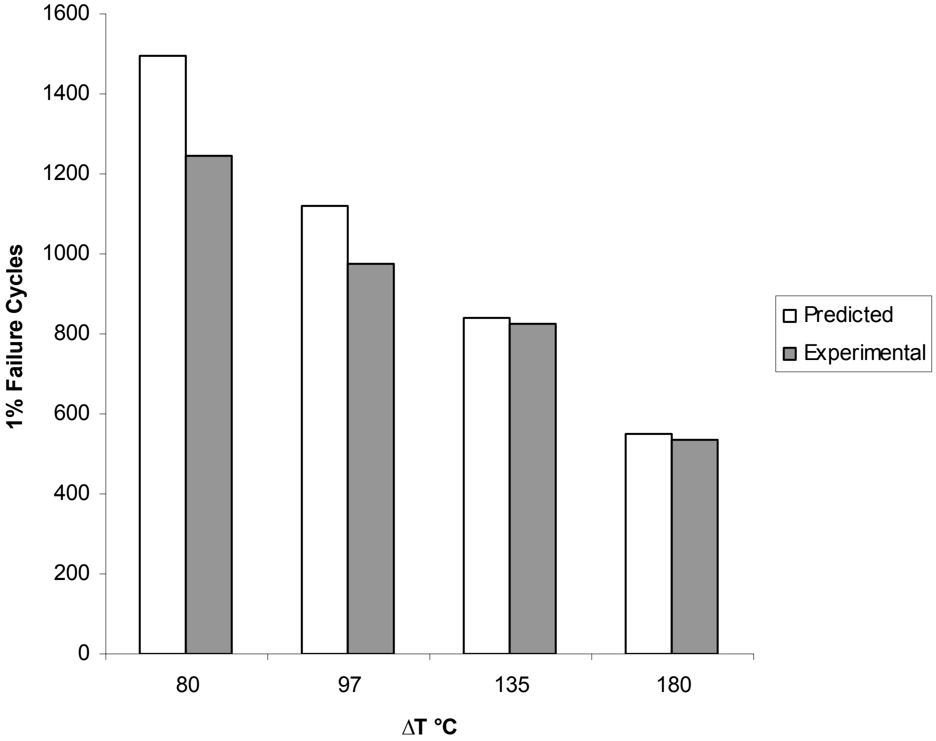

Figure 8.11: Effect of ΔT on thermal reliability of PBGA packages

Table 8.5: Sensitivity of package reliability of ΔT and comparison of statistical model predictions to actual experimental data

Package Parameters	**ΔT**	**Model**	**Experimental**	**Sensitivity factor for ΔT**
12mm 160 I/O Plastic BGA	80	1497	1246	-1.400
	97	1122	977	
	135	840	823	
	180	552	536	

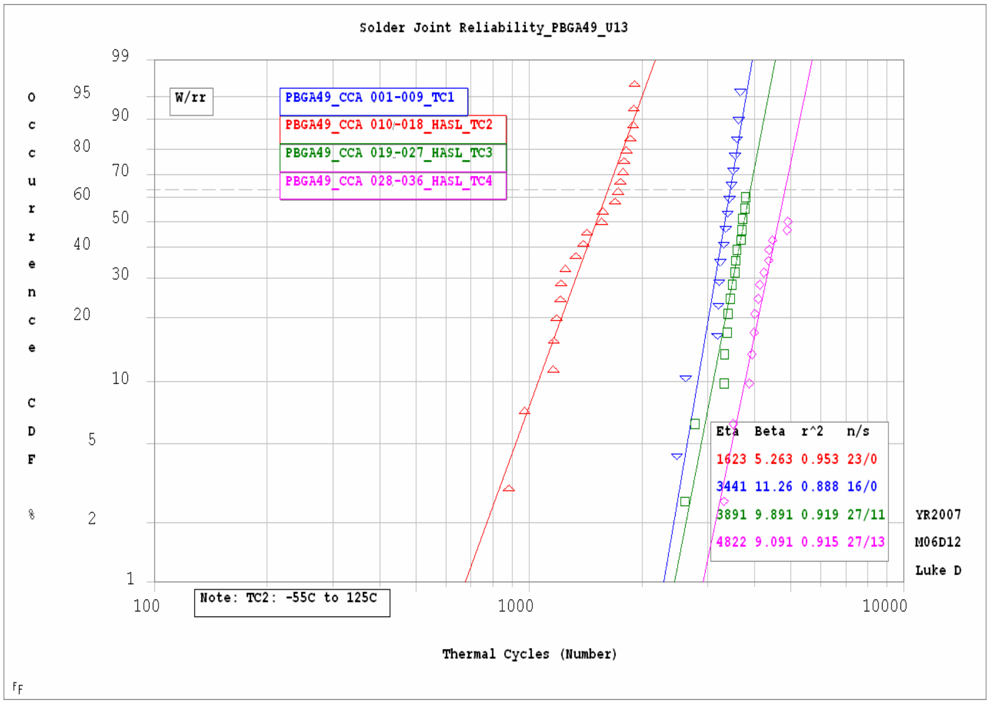

Figure 8.12: Weibull plot validating model under varying ΔT thermal conditions

8.2 Parameter Selection and Packaging Construction Process

The coefficients, or sensitivities, that were derived from the multivariable regression statistics model have been used to study the effects of various electronic packaging parameters on the solder joint reliability of the plastic ball grid array packages. The coefficients that were validated in this chapter and derived in the previous one, can be used for packaging companies to help design and determine various trade offs during planning and build stages of various applications. This model can be used as a "turn key" approach to see various trends at a glance and determine which parts or materials and the size and shape that will work best for plastic ball grid array applications. Table 8.6 shows the overall correlation between actual experimental data and the life predictions based on the statistical model The following trends have been discussed in detail and will help manufacturers decide which components to add and which to leave out in order to increase thermal reliability:

- An increase in the solder joint's height increases the thermal reliability of the solder joint in the PBGA package.
- The thermal reliability of the solder joint in a plastic ball grid array package generally decreases with the increase in the die-to-body ratio. It has been shown to hold for both the statistical model as well as the experimental data.
- Increasing the ball count for a particular PBGA package increases the over thermal reliability of the electronic package.

- HASL and ENIG surface finishes generally tend to offer the same amount of thermal reliability, however, ENIG finishes seem to be slightly better as both the statistical model predicts and the experimental data tend to support.
- The temperature cycle magnitude is inversely proportional to the thermal reliability of plastic ball grid array packages. Which says, as ΔT increases for thermal cycles, the reliability of the package, as for all ball grid arrays (not just PBGAs), greatly diminishes as a general rule of thumb.

CHAPTER 9

LIFE PREDITICION AND FIELD LIFE CORRELATION WITH ATC DATA

Life prediction and reliability assessment of an electronic package play an essential role in the product design and manufacturing processes. In order to build a more reliable product, manufacturers and engineers must be able to determine the life of the product prior to installing it into a certain component. This chapter goes into great detail explaining how life predictions can be made after a particular package has been modeled in ANSYS^{TM}. The general equations used, correlations with accelerated thermal cycling data, as well as thermal reliability life predictions of PBGA49, for three different thermal cycles, and PBGA728 have been analyzed here.

9.1 Theory

Life prediction models can be developed after several preliminary, and time consuming, steps have been completed. First, one must determine an accelerated thermal cycle in order to simulate the field conditions and the same failure mechanisms as encountered in the field. After this step, acquisition of the actual test data on the various components subjected to the ATC is completed. Then, the constitutive equations and material properties for the applicable range of stress/strain conditions are determined. In this study's case, the constitutive equations from the published literature and the material properties measured at Auburn University have been used in the present study. After these steps have been completed, the simulations for calculating the ISED for the life predictions of the solder joints must be run in ANSYS^{TM} using 3-D diagonal slice models as described in Chapter 5. Once all of this has been done, only then can the life prediction models be created.

9.2 Eutectic Solder Life Prediction Models

Life prediction models published in the literatures and used in the past are given below:

- Engelmaier's [1983] model which was based on total shear strain range

$$N_f = \frac{1}{2}\left[\frac{\Delta\gamma_T}{0.65}\right]^{-\left(\frac{1}{c}\right)}$$

where the ductility exponent, c = -0.442 -6×10-4(T) +1.72×10-2(Ln(1+ν))

T is the mean temperature, and ν is the cycling frequency.

- Solomon's [1986] low cycle fatigue model was based on plastic shear strain range

$$N_p = \left[\frac{1.36}{\Delta\gamma_p}\right]^{\left(\frac{1}{0.5}\right)}$$

- Knecht's and Fox's[1991] model was based on creep shear strain range

$$N_C = \left(\frac{8.9}{\Delta\gamma_C}\right)$$

- Pang's [1997] model was based on Miner's superposition rule of creep-fatigue

  interaction $$N_T = \left[\left(\frac{1}{N_C} \right) + \left(\frac{1}{N_p} \right) \right]^{(-1)}$$

- Morrow's energy-based fatigue model modified by Spraul, et al. [2004]

  $$N_f = C_1 (\Delta W)^{C_2}$$

  where $C_1 = 537.15$ and $C_2 = -1.0722$

- Darveaux's [2000] energy based model with CAVE modified constants

  $$N_e = N_0 + \left(\frac{a}{da/dN} \right)$$

  where 'a' is the joint diameter at the interface

  $N_0 = K_1 (\Delta W)^{K_2}$ is the number of cycle for crack initiation

  $\frac{da}{dN} = K_3 (\Delta W)^{K_4}$ is the crack propagation rate

  and the values of K_1, K_2, K_3, and K_4 are given in table 9.1.

Table 9.1: Damage relationship constants

	K_1 (cycles/psi^{K_2})	K_2	K_3 (in/cycle/psi^{K_4})	K_4
Lall et al. [2004]	28769	-1.53	6×10^{-7}	0.7684
Darveaux [2000]	48300	-1.64	3.8×10^{-7}	1.04

9.3 Weibull Distribution

Weibull distribution analysis was used to plot the experimental data obtained from the accelerated thermal cycling tests. This software plots the number of thermal cycles (x-axis) versus the percentage of occurrence of the cumulative distribution of failures (CDF). Figure 9.1 shows the Weibull distribution plot of PBGA 196 with two different surface finishes, HASL and ENIG.

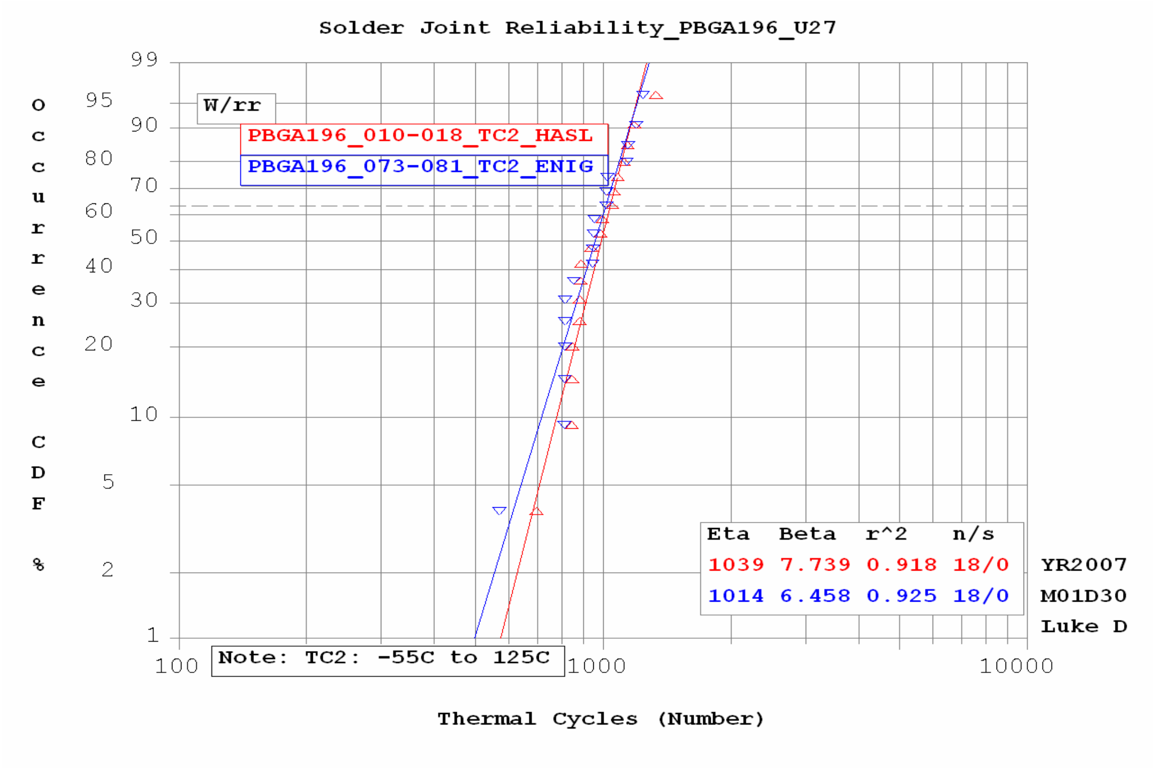

Figure 9.1: Weibull Distribution plot of PBGA 196 with various surface finishes under TC2 temperature cycle.

The basic equations that this software uses for the distributions are given in equations 9.1 and 9.2:

$$R(N) = 1 - F(N) = e^{-\left[\frac{N}{\eta}\right]^{\beta}} \qquad (9.1)$$

$$F(N) = 1 - R(N) = 1 - e^{-\left[\frac{N}{\eta}\right]^{\beta}} \qquad (9.2)$$

where "N" is the number of cycles (time until failure occurs), "R" is the percentage of parts remaining (not failed) $0 \le R \le 1$, "F" is the percentage of parts failed $0 \le F \le 1$, "η" is the characteristic life(where 63.2% of the parts have failed), and "β" is the Weibull slope.

Then, to calculate the number of cycles until failure occurs, the equation can be rearranged into

$$N = \eta\left[\ln\left(\frac{1}{1 - F(N)}\right)\right]^{\frac{1}{\beta}} \qquad (9.3)$$

In order to solve for $N_{1\%}$ failures, which will be used for FEM life predictions and was used in the statistical models, set F = .01 (1% of samples have failed) and one is left with the equation

$$N_{1\%} = \eta[.0100503]^{\frac{1}{\beta}} \qquad (9.4)$$

Appendix A contains other weibull graphs that are relevant to this research.

9.4 Crack Growth Correlations and Fatigue Life Predictions

As it was shown in Chapter 5, ANSYS was used to simulate the thermal cycle experiments for two PBGA packages, 49 I/O and 728 I/O. The diagonal slice model was used with mapped finite element mesh techniques. Solder ball materials were meshed with VISCO 107 elements and all other package materials were meshed with SOLID 45 elements.

A volume averaging technique was used to reduce this sensitivity to meshing. The volume of the element normalizes the strain energy value at each element

$$\Delta W_{AVE} = \frac{\sum \Delta W \cdot V}{\sum V} \qquad (9.5)$$

where $\Delta W_{AVE,}$ the average viscoplastic strain energy density, is accumulated per cycle at the interface elements. ΔW is the viscoplastic strain energy density accumulated per cycle of each element, and V is the volume of each element.

The difference in the viscoplastic strain energy density has been correlated with the measured crack growth data. Initially the viscoplastic strain energy density values were averaged over entire worst solder ball to minimize the mesh density effect on the finite element simulation. However, extensive analysis of this technique, Lall, et. al [2004], proved that fatigue life results are way off the experiment. The viscoplastic strain energy density values have been averaged over the interface elements. The typical interface layer varies from 1.5 to 3 mils.

In the current work, the life prediction model used to predict N1% failures was the Darveaux [2004] energy based model with CAVE-modified constants. This model presents the “best fit” model for life prediction of PBGA49 and PBGA728 models created for this study.

When comparing the various component reliabilities, the value of N1% has been used for correlation purposes. The cumulative distribution of failures (CDF) for the Weibull Distribution is given by

$$\mathrm{CDF} = 1 - e^{-\left(\frac{N - N_0}{\alpha_W - N_0}\right)^{\beta_W}} \qquad (9.6)$$

where N is the number of cycles, N_0 is the failure free life, α_W is the characteristic life at which 63.2% of the population has failed, and β_W is the weibull slope or shape parameter which indicates the class of failure modes.

Since the crack growth rate is constant during the thermal cycling, as seen from Lall’s et. al [2004] studies, the fatigue life of a joint can be calculated by adding the number of cycles to grow the cracks across the joint interface. The characteristic life can be expressed as

$$\alpha_W = N_i + \left(\frac{a}{da/dN}\right) \qquad (9.7)$$

where ‘a’ is the joint diameter at the interface. Darveaux et. al. [1995] found that the maximum crack length in the population was approximately one half of the characteristic length. The characteristic crack length can be defined as the propagation length of the primary interface, which may be the board or package pad depending on the crack interface being examined. Typically, the pad diameter is equivalent to the characteristic crack length. Therefore, one would expect the failure free life to be approximately one half of the characteristic life as expressed in equation 9.8.

$$N_0 = \left(\frac{\alpha_W}{2}\right) \tag{9.8}$$

In order to calculate the number of cycles until 1% failure occurs from the failure equation, it has been assumed that the sample size being predicted is 100 samples. Therefore, the 1% failure time and time until the first failure occurs are the same value. If the data is used for a sample size of less than 100, such as in this study's case, the prediction should only be interpreted as 1% failure. The number of cycles until the first failure occurs is given by equation 9.9.

$$N = N_0 + (\alpha_W - N_0)\left[-\ln(1 - \mathrm{CDF})\right]^{(1/\beta_W)} \tag{9.9}$$

where CDF is calculated in terms of median rank

$$\mathbf{C}\mathrm{DF} = \left(\frac{1 - 0.3}{S_S + 0.4}\right) \tag{9.10}$$

where S_S is the sample size.

Fatigue Life Predictions (FEM)

Solder joint fatigue life predictions have been done for PBGA 728 under temperature profile TC2 and PBGA 49 life predictions have been done under temperature profiles TC1-TC4. Figure 9.2 shows the Weibull distributions for PBGA 49 under the four temperature cycles. Figure 9.3 shows the weibull distribution for PBGA 728 under thermal cycling condition TC2. These weibull distributions were used to create table 9.4 as well as to compare the FEM predicted $N_{1\%}$ values to the actual experimental $N_{1\%}$ values and to generate Figure 9.4. Table 9.2 and 9.3 show the values that were used for the FEM life predictions which were plugged into equations 9.5-9.10.

Looking at Figure 9.4, one can see the comparisons of the FEM predicted $N_{1\%}$, as well as the statistics model's predicted $N_{1\%}$ values to the actual experimental $N_{1\%}$ values. The life predictions based on the finite element and multivariate linear regression analysis are very close to the actual experimental values. This shows that the models work and hence validates the diagonal slice modeling methods that were implemented in ANSYS^{TM}.

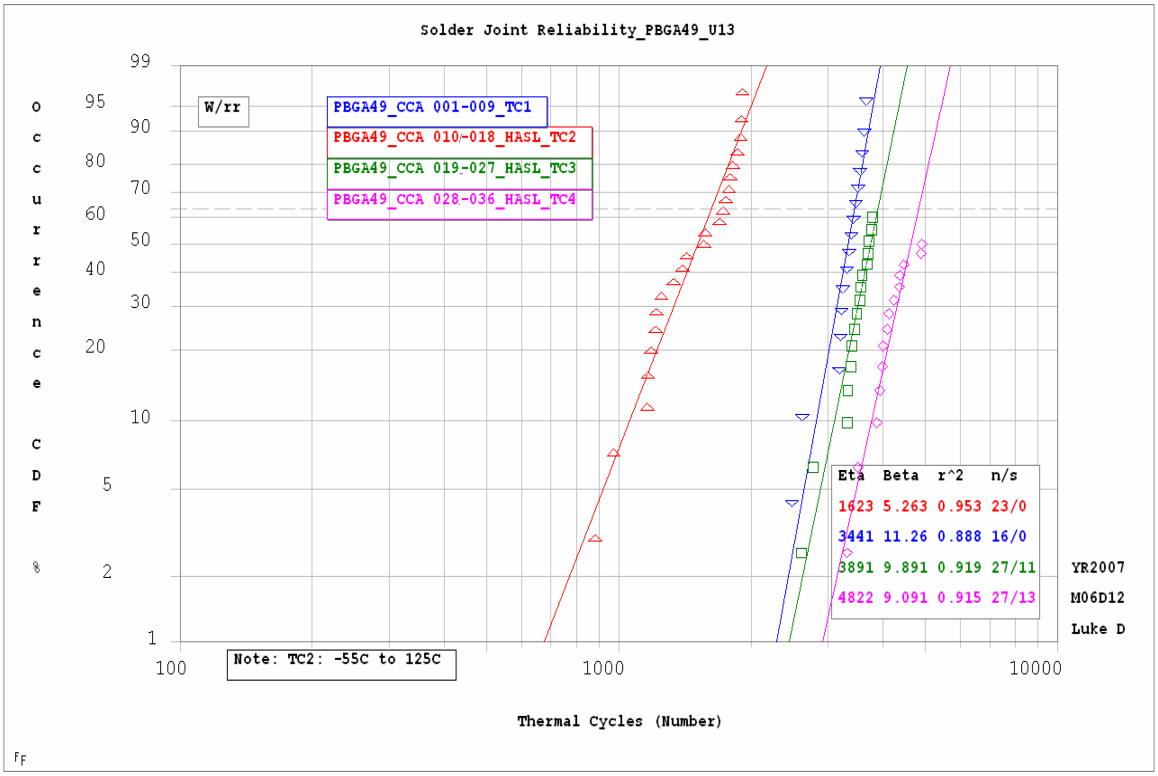

Figure 9.2: Weibull Distribution for PBGA 49 under temperature cycles TC1-TC4

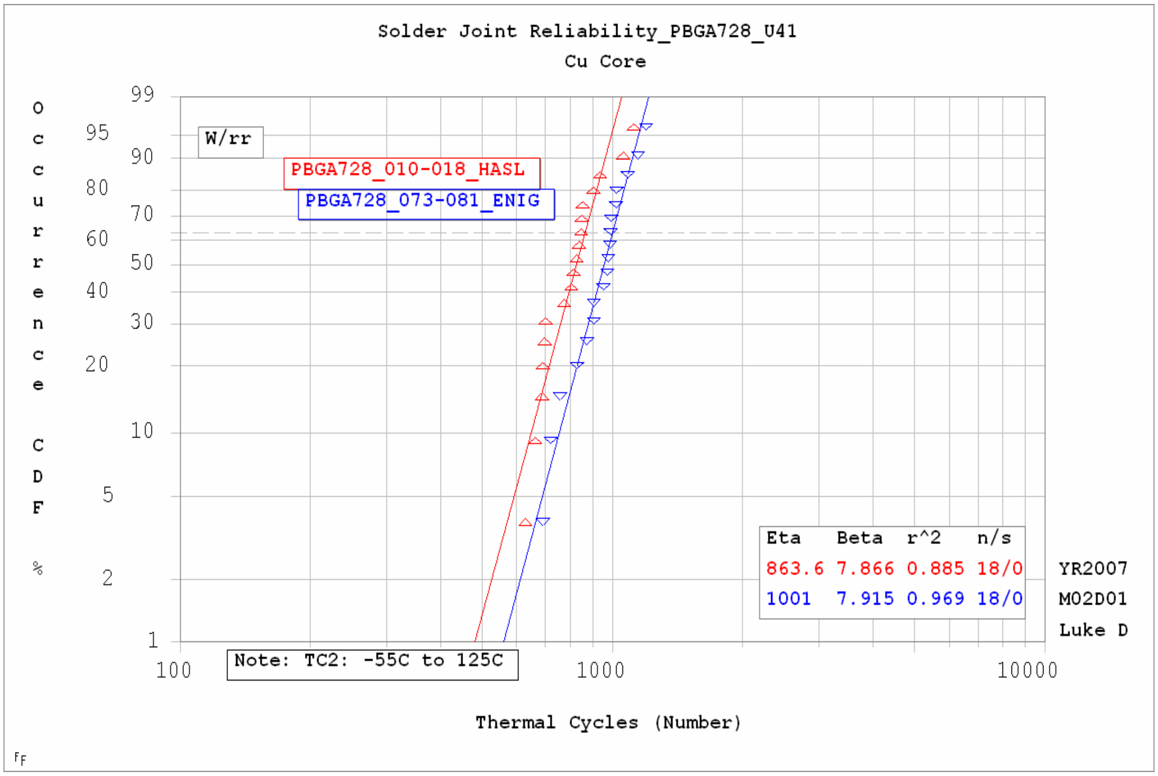

Figure 9.3: Weibull Distribution for PBGA 728 under temperature cycle TC1

Table 9.2: FEM life prediction parameters

Reference Number	I/O Count	a BT Pad Diameter (inch)	Temperature Cycle	ΔW (psi)	Package Size (BT Thickness) (in)	CDF	N(i) Cycles
U41 (Eutectic)	728	0.0160	TC2	36.152	0.019	0.01	134
U13 (Eutectic)	49	0.0093176	TC1	13.301	0.045	0.01	693
U13 (Eutectic)	49	0.0093176	TC2	32.200	0.045	0.01	163
U13 (Eutectic)	49	0.0093176	TC3	11.346	0.045	0.01	899
U13 (Eutectic)	49	0.0093176	TC4	9.034	0.045	0.01	1307

Table 9.3:FEM life prediction results from equations 9.5 - 9.10

da/dN (inch/Cycle)	η (Cycle)	N(o) (Cycle)	N(1%) Failure (Cycle)
0.0000158	1142	571	889
0.0000056	2355	1178	1960
0.0000141	825	413	584
0.0000048	2860	1430	2325
0.0000037	3792	1896	3039

Table 9.4: Experimental data and results from ATC testing

Experimental Data					
I/O Count	**Temperature Cycle**	**β Slope**	**Sample Size**	**η (Cycle)**	**N(1%) Failure (Cycle)**
728	TC2	7.866	18	1205	739
49	TC1	11.26	16	3441	2287
49	TC2	5.263	23	1623	677
49	TC3	9.81	27	3891	2444
49	TC4	9.09	27	4822	2907

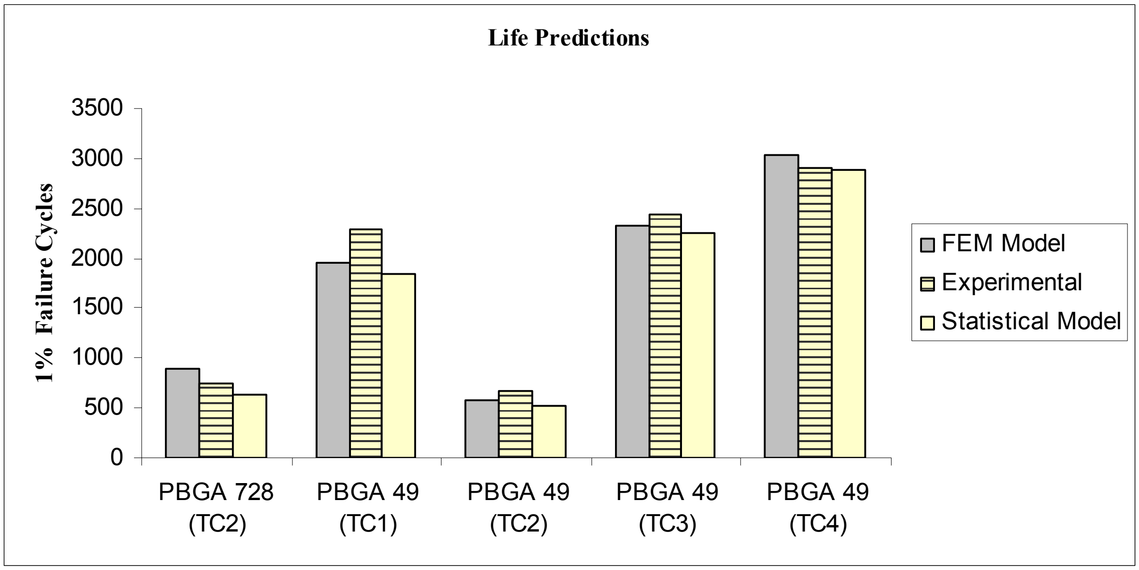

Figure 9.4: FEM and Statistical Model life predictions plotted next to actual experimental data for PBGA 728 and PBGA 49

CHAPTER 10

SUMMARY AND CONCLUSIONS

The work presented in this thesis has been used to create decision support models for package construction, design, and deployment of ball grid area array devices under various thermal conditions. These thermal conditions ranged from harsh environments, -55°C to 125°C (TC2), to not so harsh thermal environments, -20°C to 60°C (TC4). Whatever the case may be, even thermal conditions not described here, the two sets of models created throughout this research, can be used to design, develop, analyze, and reduce costs for many electronic devices which use PBGA electronic packages. The sensitivities of reliability to design, material, architecture and environment parameters have been developed and validated with the experimental data. The model predictions for multiple parametric variations show the similar trends in the effect on reliability of the package of various configurations. The sensitivity factors that were developed in the statistical modeling section, Chapter 8, can be used to analyze the quantitative impact that various design parameters have on the actual thermal reliability of plastic ball grid array packages in harsh thermal environments.

The hybrid modeling methodology that is presented in this paper provides companies with a technique to perturb accelerated test data and evaluate what happens when certain parameters are changed without having to run the tedious, time consuming accelerated thermal cycling processes at their own facilities. These models presented are a valuable asset to electronic companies looking to design electronic components with plastic ball grid array electronic packages. It presents an extremely cost effective and time saving solution for the thermo-mechanical reliability assessment of the PBGA devices subjected to extreme environments. First order models that are generally used for this "turn-key" approach can not achieve the accuracy that these finite element and multivariate regression analysis models are capable of. These models allow the user to quantitatively determine the various impacts that changing parameters can have on the overall thermal reliability of these electronic packages.

The overall conclusions that can be made for plastic ball grid array electronic packages from this research are:

- The increase in the temperature range, ΔT, of a given thermal cycle decreases the thermal reliability of the package greatly.
- An increase in the solder ball's diameter increases the thermal reliability of the package
- An increase in the solder ball height increases the thermal reliability of the ball grid array
- The thermo-mechanical reliability of an electronic package increases as the ball count , or number of I/O's, increase
- The die-to-body ratio of an electronic package greatly effects the thermo-mechanical reliability. As the die-to-body ratio increases, the thermo-mechanical reliability decreases for ball grid array packages.

Finite element analysis was conducted on two different plastic ball grid array electronic packages with different die sizes, ball counts, and various other packaging parameters. PBGA 49 was constructed and simulated in all four temperature cycling conditions and PBGA 728 was constructed and simulated in the most extreme thermal environment, TC2. Eutectic tin-lead, (62Sn36Pb2Ag), solder and its appropriate material properties were used in the analysis and simulation of these models. These models led to some interesting conclusions as well:

- For temperature cycling condition TC2, -55°C to 125°C, the inelastic strain energy density, ΔW, was considerably higher than it was for the other three temperature cycling conditions.

- For temperature cycling conditions TC1, TC3, and TC4 the inelastic strain energy densities were relatively close to one another. Each temperature condition resulted in ± 4 psi of one another.

Multivariate regression analysis was also conducted on a large database of experimental data for various plastic ball grid array packages. Analysis of variance and sensitivity factors were analyzed and developed in order to produce a statistical model which accurately predicts life for these PBGA packages. The statistical model conclusions were:

- An increase in the solder joint height increases the thermal reliability of the electronic package.

- Increasing the number of I/O's , or ball count, increased the thermal reliability of the electronic package.

- Increasing the temperature range, ΔT, of the accelerated thermal cycling decreases the thermal reliability, or life, of the package at hand.

- As the die-to-body ratio increases, the thermo-mechanical reliability of the package decreases. It has an inverse effect on the package life.
- Surface finishes were analyzed, both HASL and ENIG, and it was shown that both finishes produce relatively close results for thermo-mechanical reliability. However, in this study, ENIG had the better life and reliability results.

These models, both statistical and FEA, have produced some really exciting results that have not been produced or shown before. For instance, the statistical models let the user analyze different surface finishes on the copper pads, such as HASL and ENIG. This is an element that can not be modeled using finite element analysis. Also, finite element analysis lets the user analyze the inelastic strain energy density, stresses, and both elastic and plastic strains which can not be seen in statistical models. Each of these model have their own positives and limits to their abilities. However, when they are used in conjunction to one another, as they are in this research, very exciting results can be seen at a glance. These results allow manufacturers to have a “turn-key” approach for designing, analyzing, and predicting what will happen when these plastic ball grid array packages are used on copper core printed circuit boards. These models are not 100% accurate and should not be used for absolute solder joint life prediction. However, they are great tools for helping decide which packages to use and what kind of reliability can be expected from each.

There are a few things that could use improvement in these models. For one, finite element models need to be developed for various I/O count packages, such as PBGA 196, PBGA 676, PBGA 256, etc. Also, the finite element models in this research are only slice models with boundary conditions imposed on them. For more accurate results, full scale models need to be run and analyzed for life predictions. However, full scale models of these packages would take a great deal of time to construct and even more time for simulation to be run on the computer. All in all, these models are great tools to help manufactures decide which components will work best for given situations as well as save a great deal of time and money trying to figure out which packages to use.

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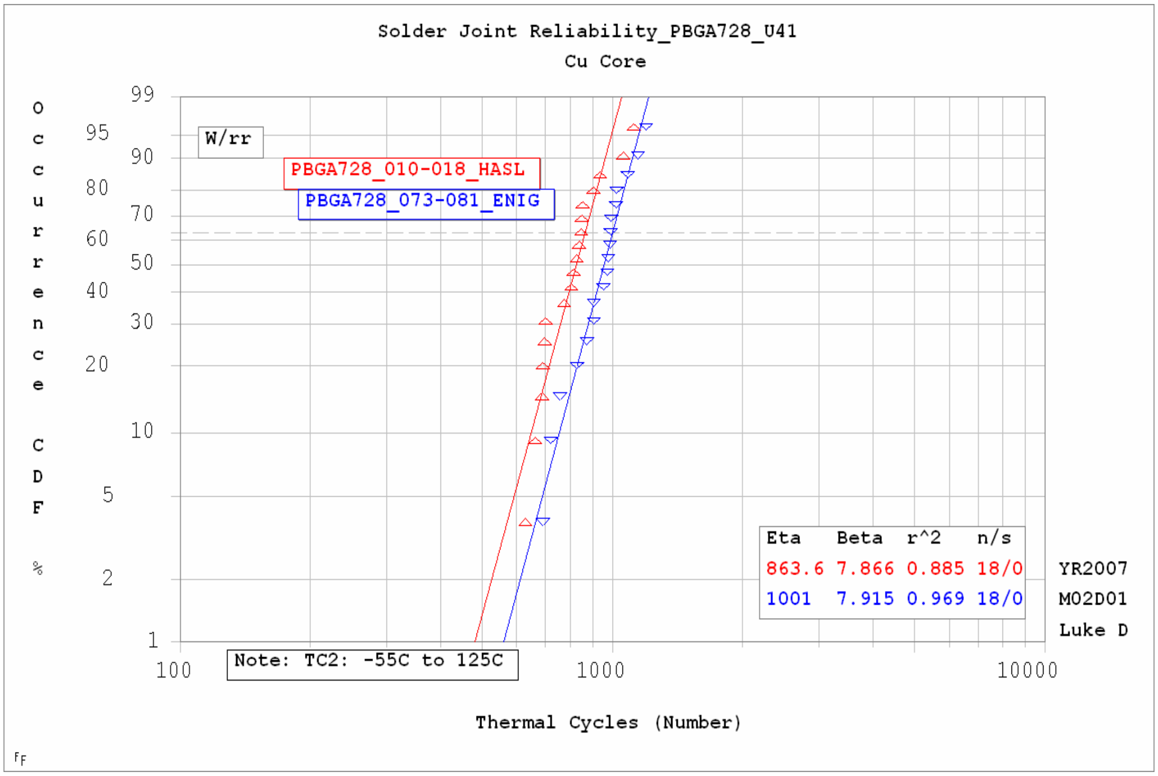
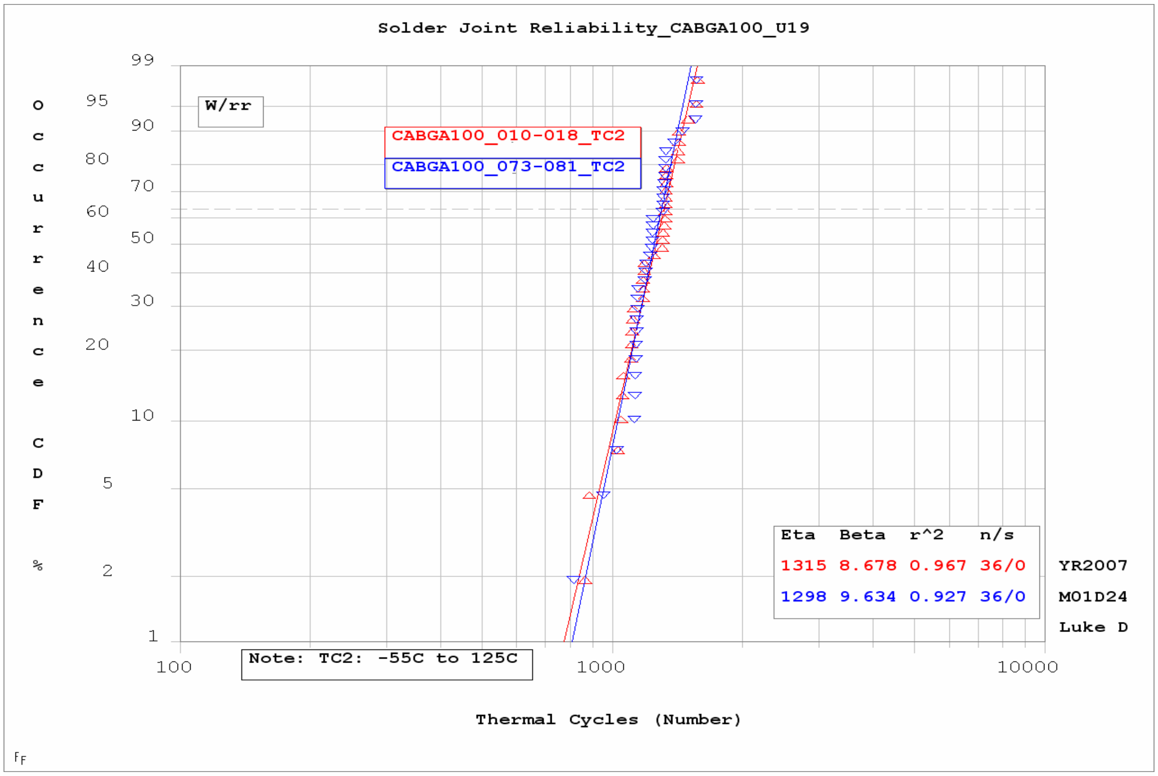
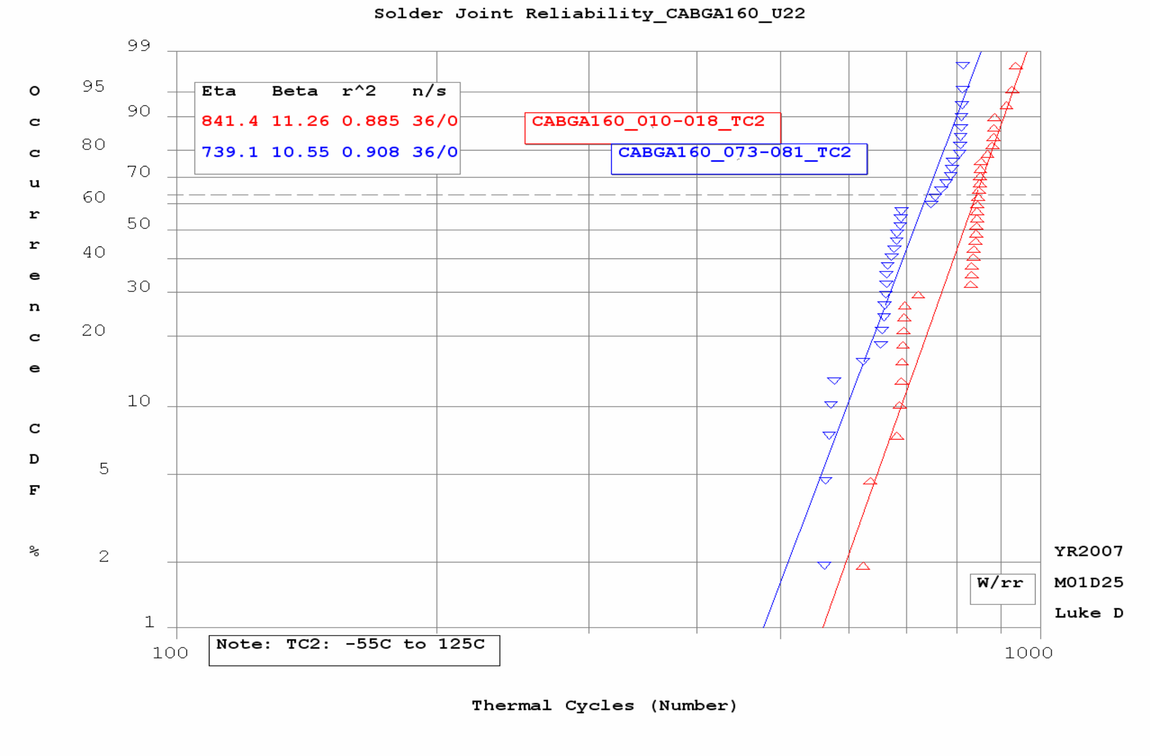
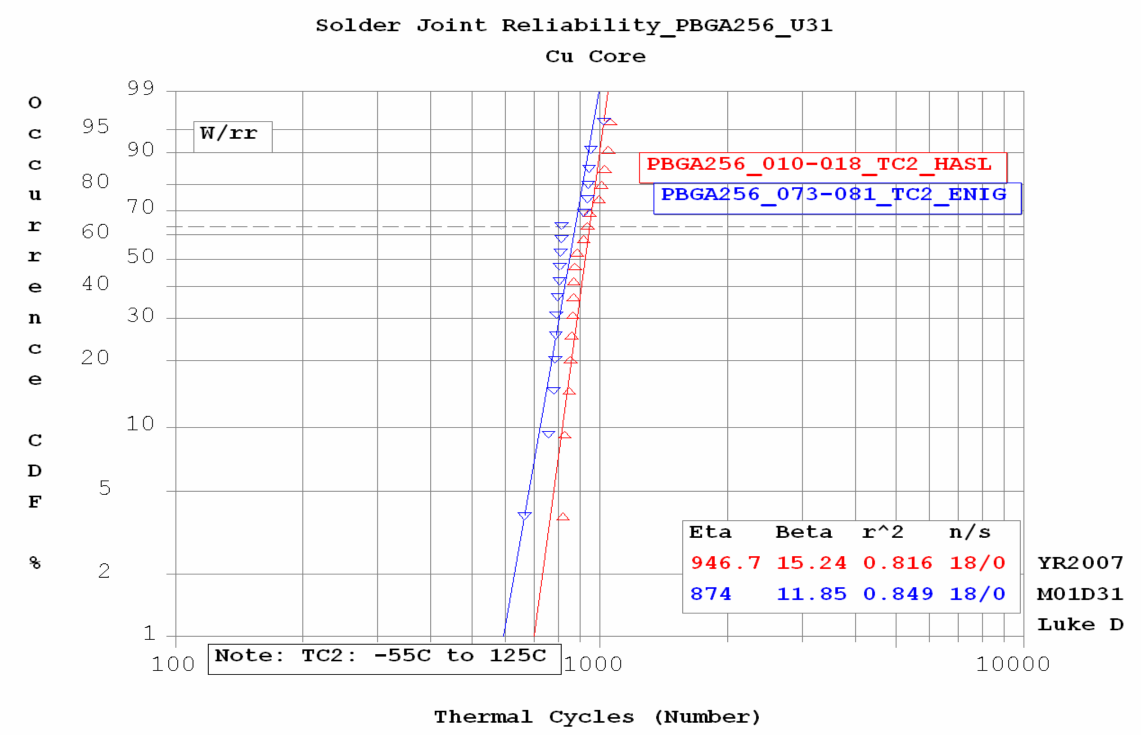
APPENDIX-A

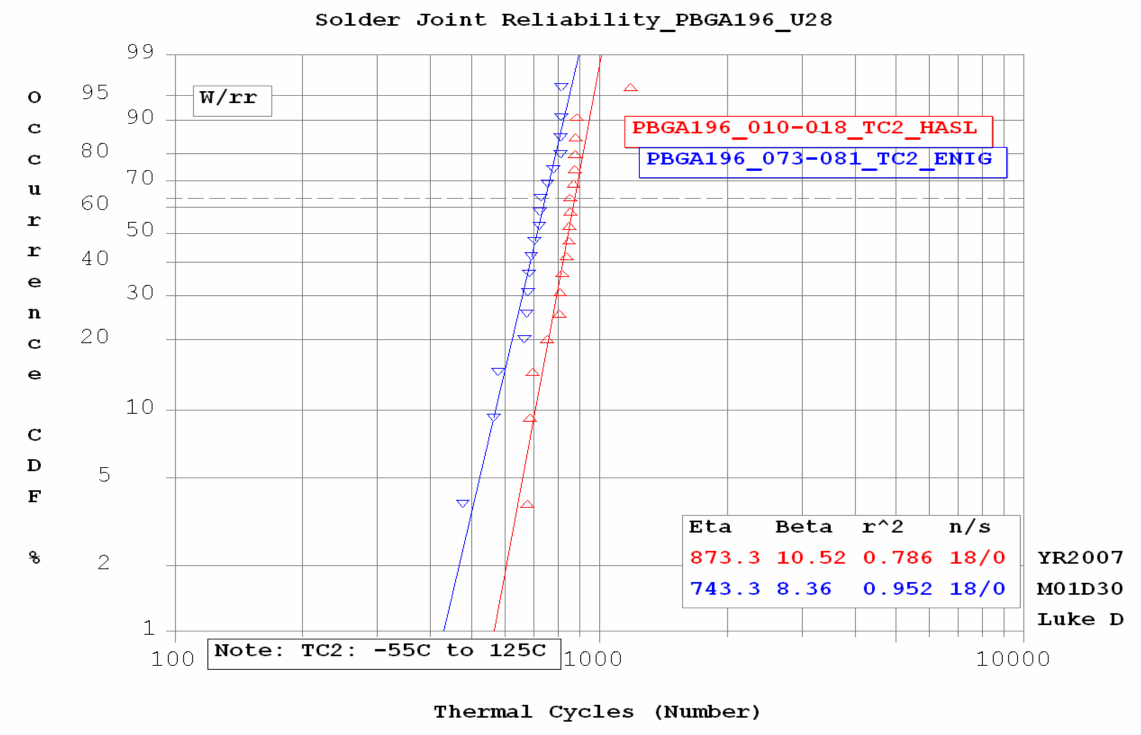
WEIBULL DISTRIBUTION PLOTS FOR VARIOUS PBGA PACKAGES

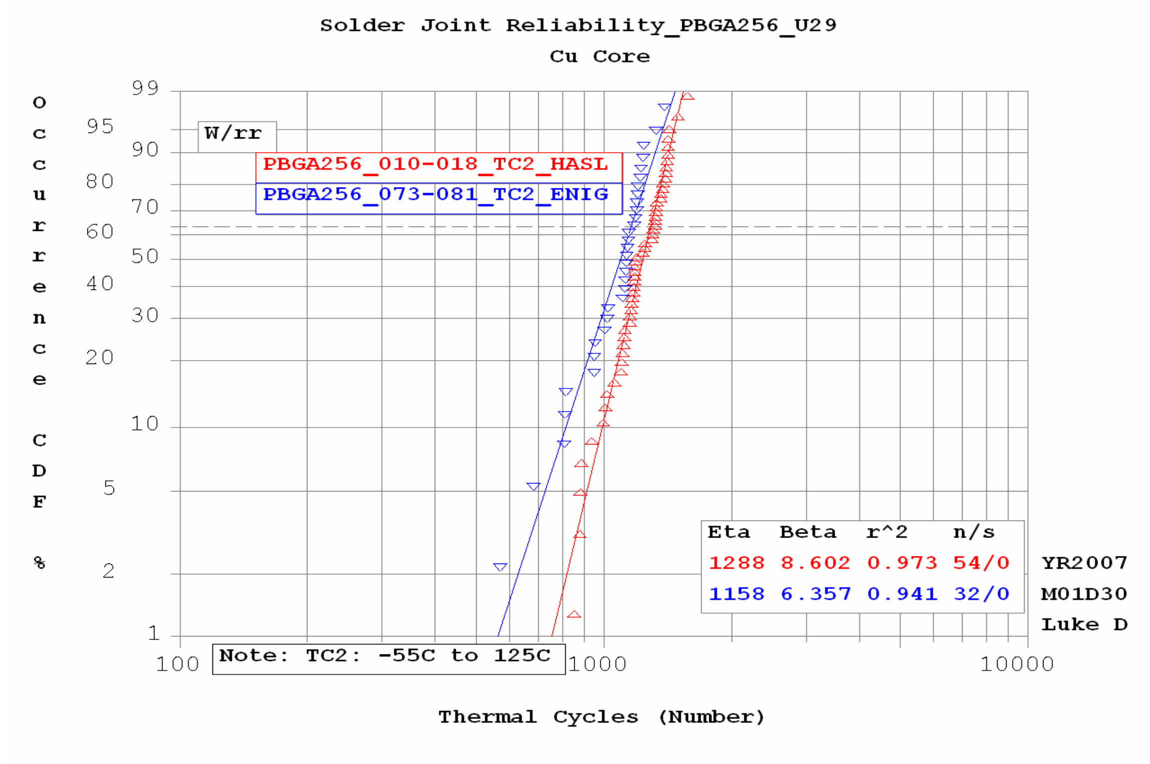



Solder Joint Reliability_CABGA100_U19
Occurrence CDF %
99
95
90
80
70
60
50
40
30
20
10
5
2
1
W/rr
CABGA100_010-018_TC2
CABGA100_073-081_TC2
Eta Beta r^2 n/s
1315 8.678 0.967 36/0
1298 9.634 0.927 36/0
YR2007
M01D24
Luke D
100
1000
10000
Note: TC2: -55C to 125C
Thermal Cycles (Number)


Solder Joint Reliability_CABGA160_U22
Occurrence CDF %
99
95
90
80
70
60
50
40
30
20
10
5
2
1
Eta Beta r^2 n/s
841.4 11.26 0.885 36/0
739.1 10.55 0.908 36/0
CABGA160_010-018_TC2
CABGA160_073-081_TC2
W/rr
YR2007
M01D25
Luke D
100
1000
Note: TC2: -55C to 125C
Thermal Cycles (Number)


Solder Joint Reliability_PBGA256_U31
Cu Core
W/rr
PBGA256_010-018_TC2_HASL
PBGA256_073-081_TC2_ENIG
Eta Beta r^2 n/s
946.7 15.24 0.816 18/0
874 11.85 0.849 18/0
YR2007
M01D31
Luke D
Note: TC2: -55C to 125C
Occurrence CDF %
99
95
90
80
70
60
50
40
30
20
10
5
2
1
100
1000
10000
Thermal Cycles (Number)


Solder Joint Reliability_PBGA196_U28
W/rr
PBGA196_010-018_TC2_HASL
PBGA196_073-081_TC2_ENIG
Eta Beta r^2 n/s
873.3 10.52 0.786 18/0
743.3 8.36 0.952 18/0
YR2007
M01D30
Luke D
Note: TC2: -55C to 125C
Occurrence CDF %
99
95
90
80
70
60
50
40
30
20
10
5
2
1
100
1000
10000
Thermal Cycles (Number)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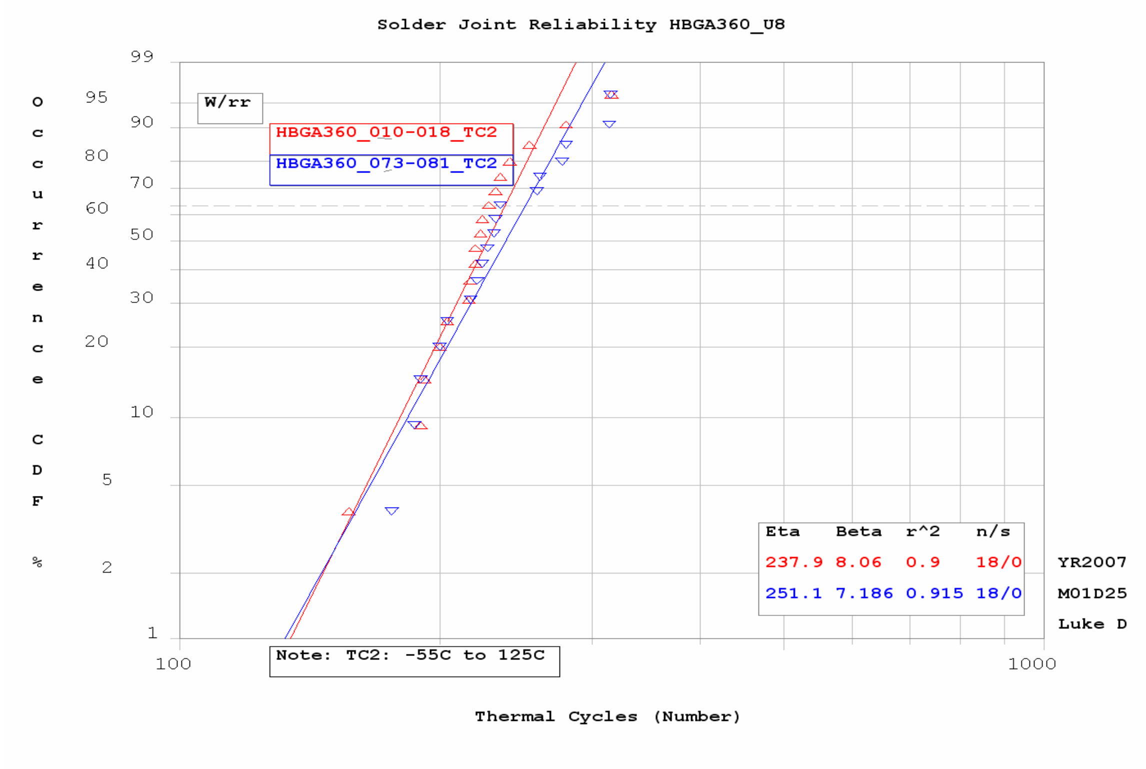
Cu Core
Occurrence CDF %
99
95
90
80
70
60
50
40
30
20
10
5
2
1
W/rr
PBGA256_010-018_TC2_HASL
PBGA256_073-081_TC2_ENIG
Eta Beta r^2 n/s
1288 8.602 0.973 54/0
1158 6.357 0.941 32/0
YR2007
M01D30
Luke D
100
1000
10000
Note: TC2: -55C to 125C
Thermal Cycles (Number)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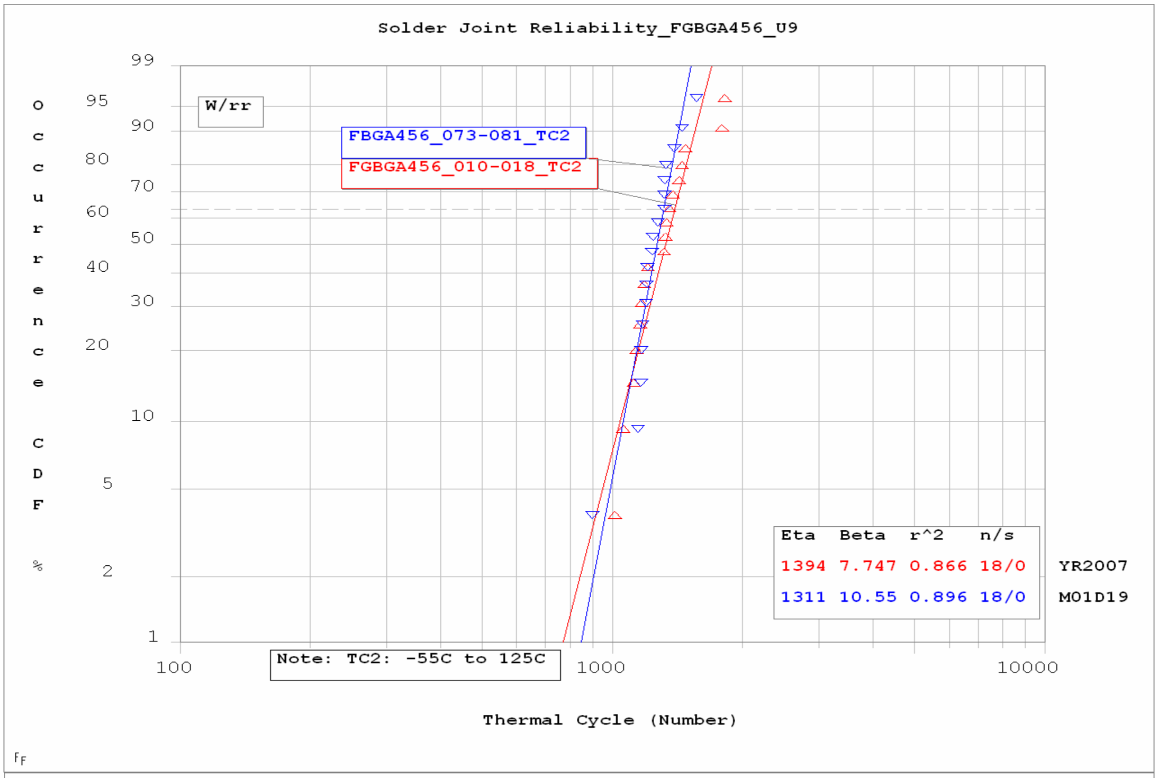
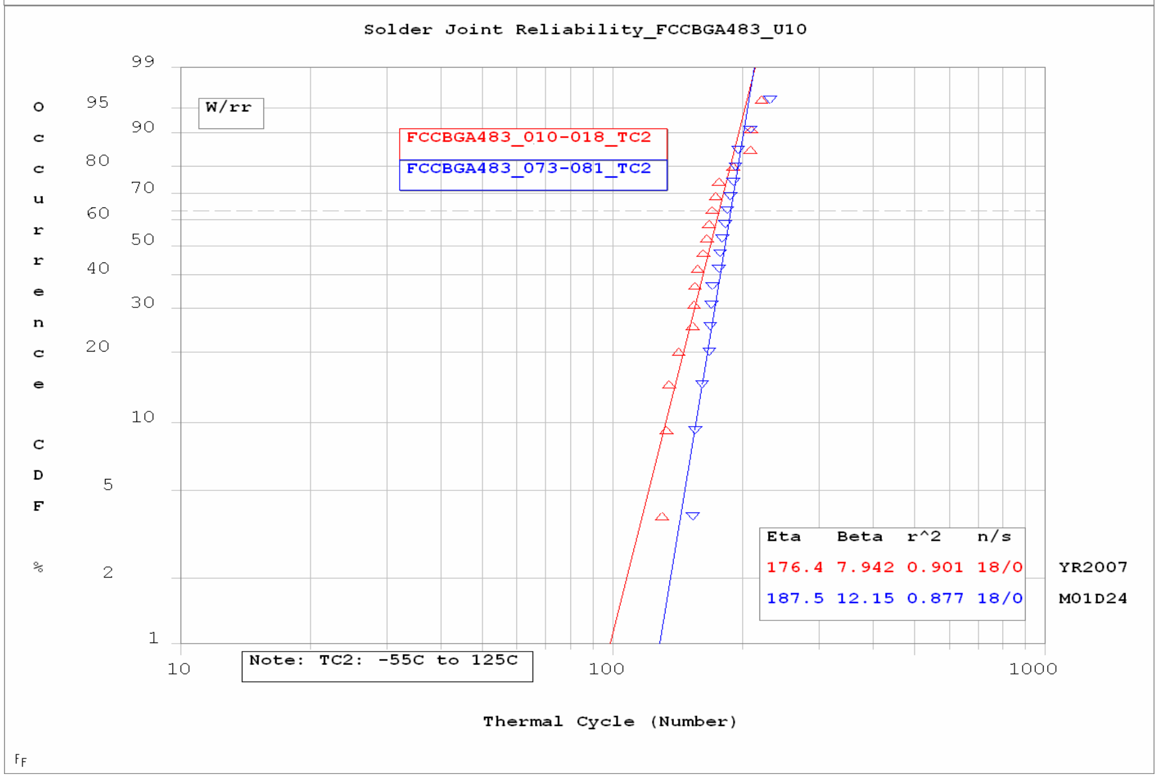
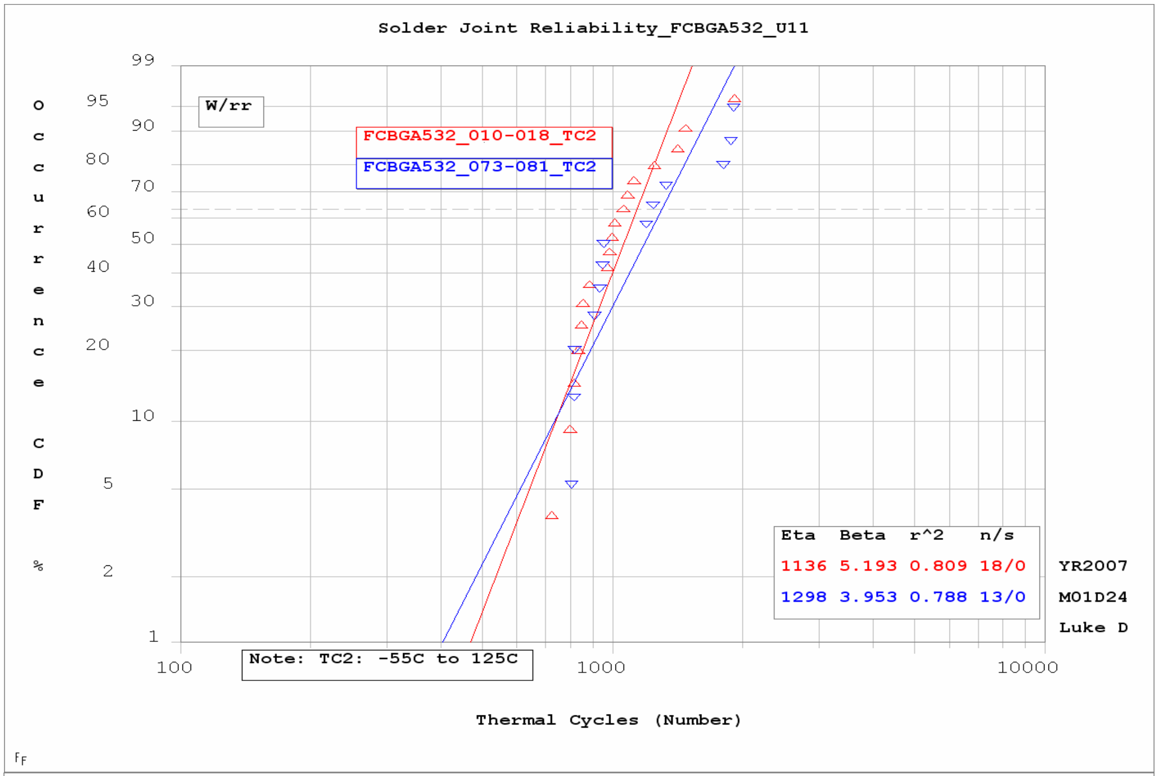
Occurrence CDF %
99
95
90
80
70
60
50
40
30
20
10
5
2
1
W/rr
HBGA360_010-018_TC2
HBGA360_073-081_TC2
Eta Beta r^2 n/s
237.9 8.06 0.9 18/0
251.1 7.186 0.915 18/0
YR2007
M01D25
Luke D
100
1000
Note: TC2: -55C to 125C
Thermal Cycles (Number)


Solder Joint Reliability_FGBGA456_U9
Occurrence CDF %
99
95
90
80
70
60
50
40
30
20
10
5
2
1
W/rr
FBGA456_073-081_TC2
FGBGA456_010-018_TC2
Eta Beta r^2 n/s
1394 7.747 0.866 18/0
1311 10.55 0.896 18/0
YR2007
M01D19
Note: TC2: -55C to 125C
100
1000
10000
Thermal Cycle (Number)
fF


Solder Joint Reliability_FCCBGA483_U10
Occurrence CDF %
99
95
90
80
70
60
50
40
30
20
10
5
2
1
W/rr
FCCBGA483_010-018_TC2
FCCBGA483_073-081_TC2
Eta Beta r^2 n/s
176.4 7.942 0.901 18/0
187.5 12.15 0.877 18/0
YR2007
M01D24
Note: TC2: -55C to 125C
10
100
1000
Thermal Cycle (Number)
fF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W/rr
FCBGA532_010-018_TC2
FCBGA532_073-081_TC2
Occurrence CDF %
99
95
90
80
70
60
50
40
30
20
10
5
2
1
100
1000
10000
Note: TC2: -55C to 125C
Thermal Cycles (Number)
Eta Beta r^2 n/s
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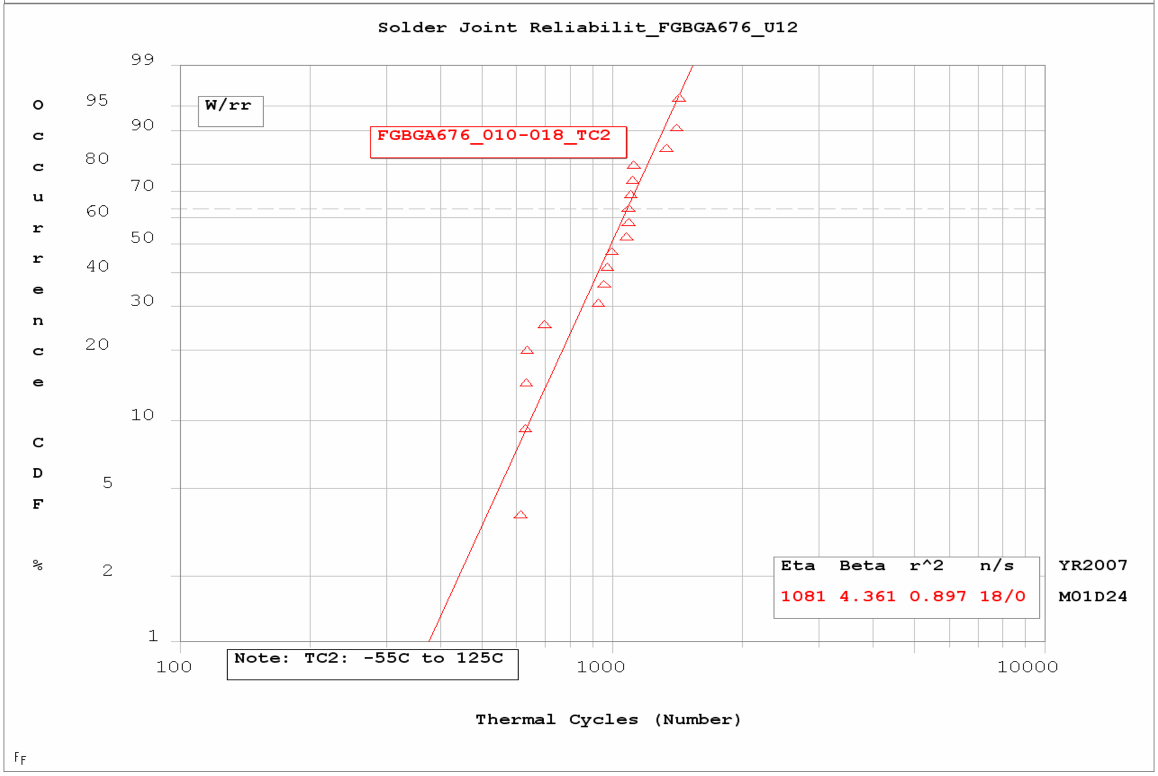
1298 3.953 0.788 13/0
YR2007
M01D24
Luke D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W/rr
FGBGA676_010-018_TC2
Occurrence CDF %
99
95
90
80
70
60
50
40
30
20
10
5
2
1
100
1000
10000
Note: TC2: -55C to 125C
Thermal Cycles (Number)
Eta Beta r^2 n/s
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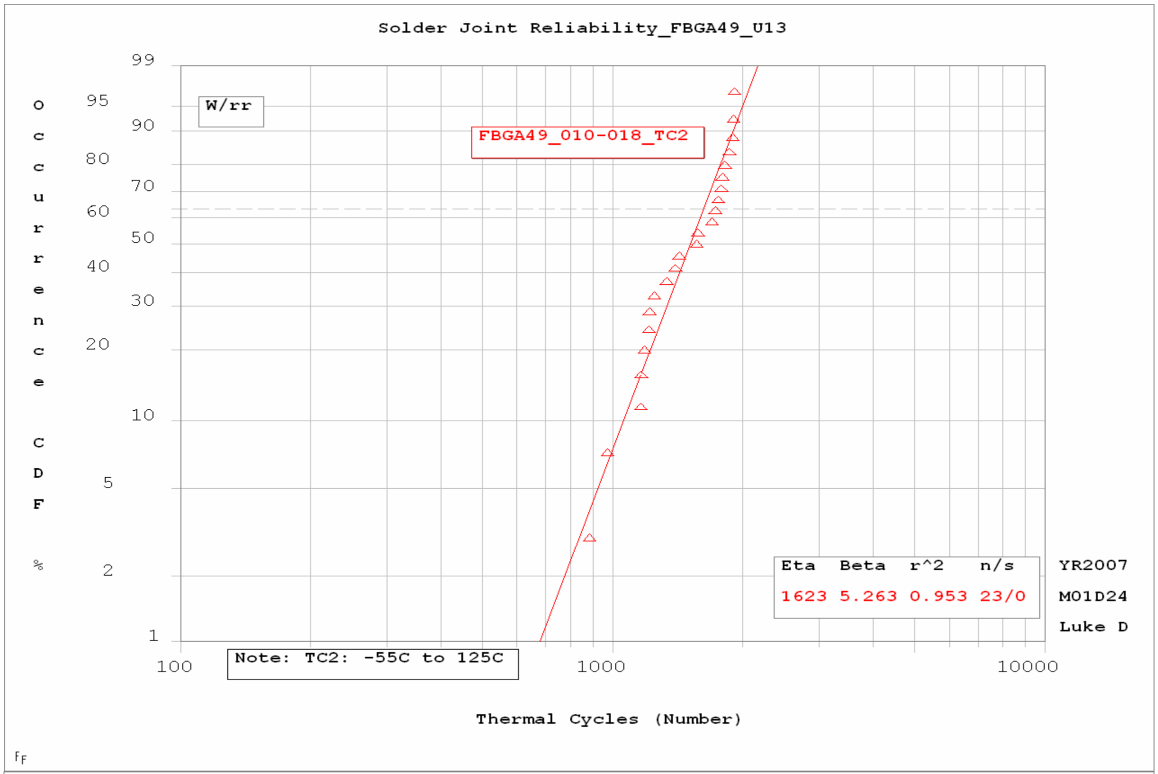
YR2007
M01D24


Solder Joint Reliability_FBGA49_U13
W/rr
FBGA49_010-018_TC2
Occurrence CDF %
99
95
90
80
70
60
50
40
30
20
10
5
2
1
100
1000
10000
Note: TC2: -55C to 125C
Thermal Cycles (Number)
Eta Beta r^2 n/s
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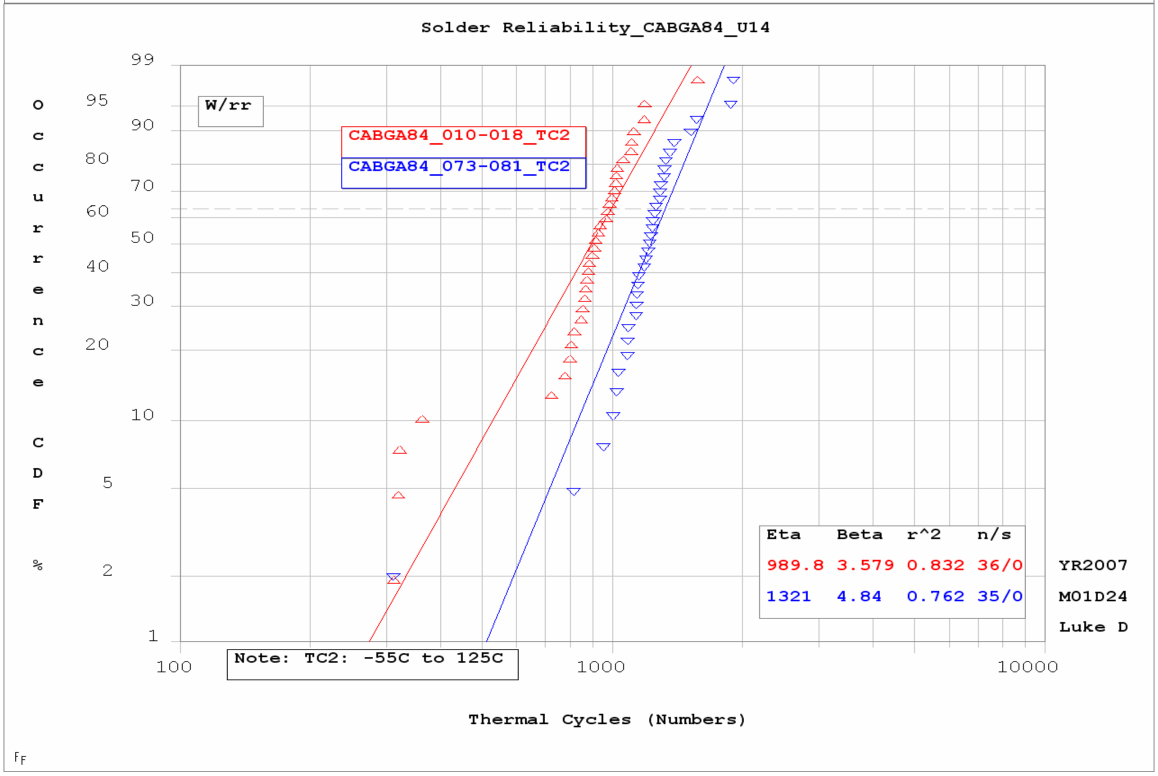
YR2007
M01D24
Luke D
fF


Solder Reliability_CABGA84_U14
W/rr
CABGA84_010-018_TC2
CABGA84_073-081_TC2
Occurrence CDF %
99
95
90
80
70
60
50
40
30
20
10
5
2
1
100
1000
10000
Note: TC2: -55C to 125C
Thermal Cycles (Numbers)
Eta Beta r^2 n/s
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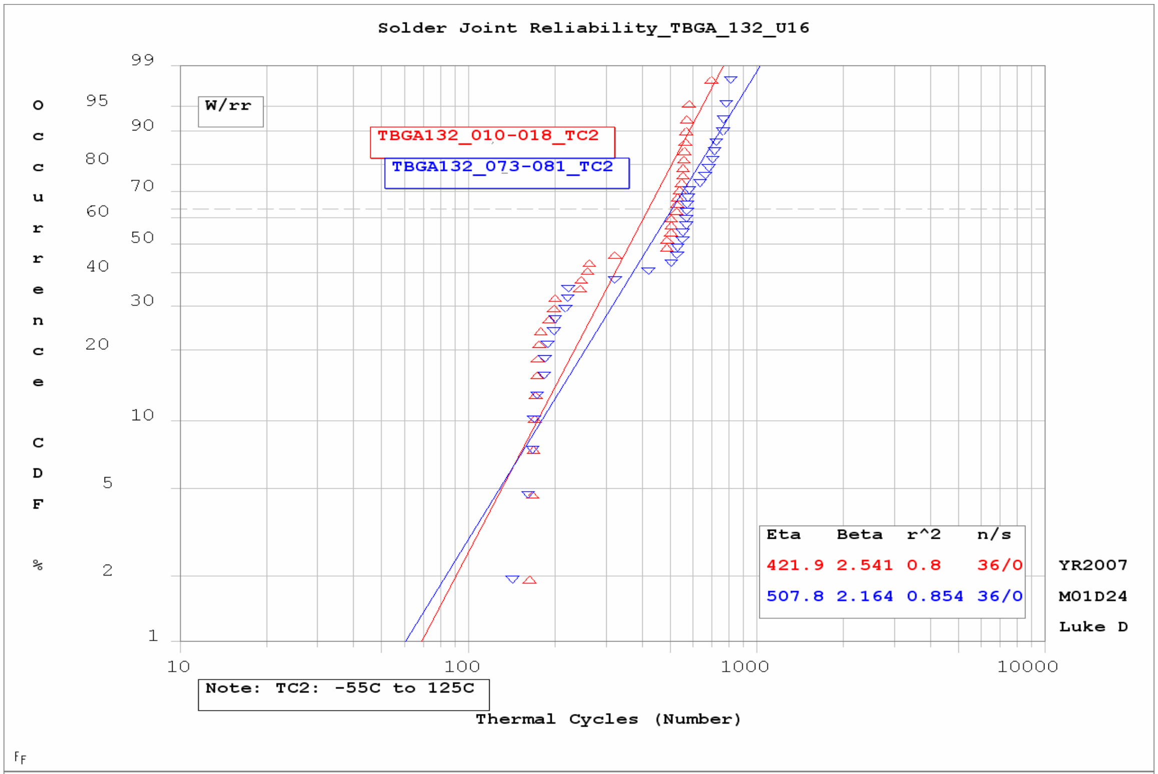
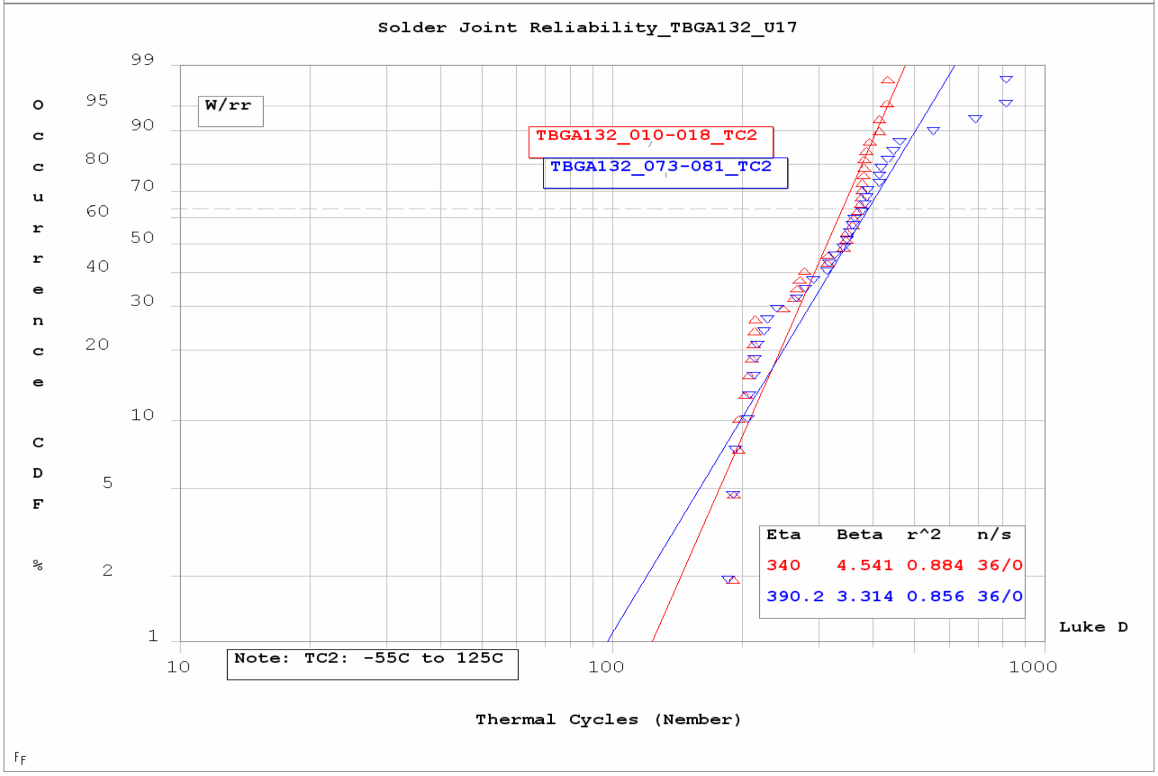
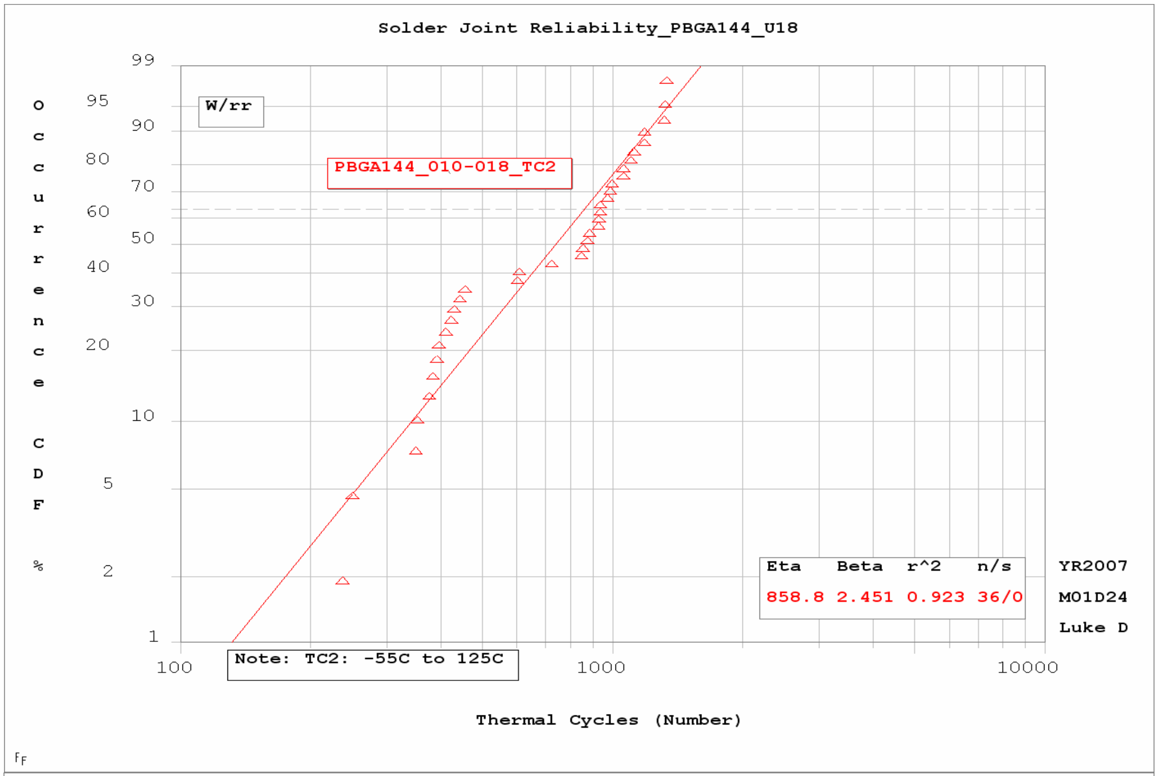
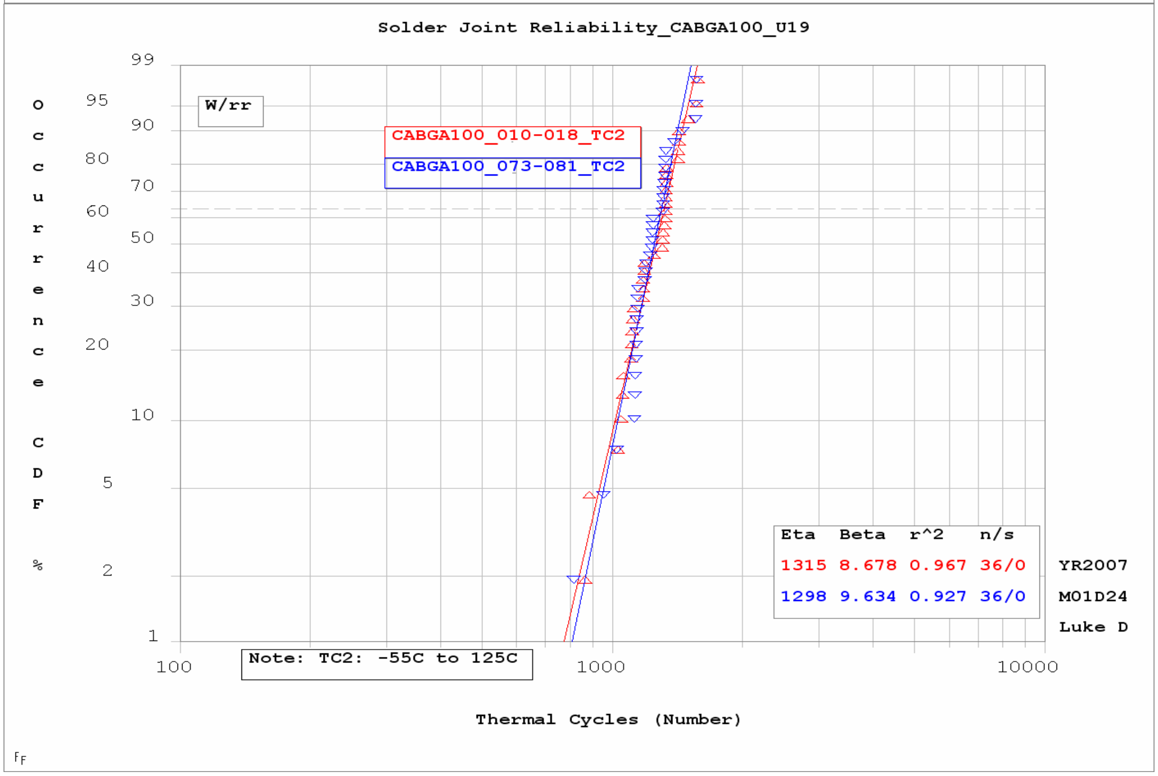
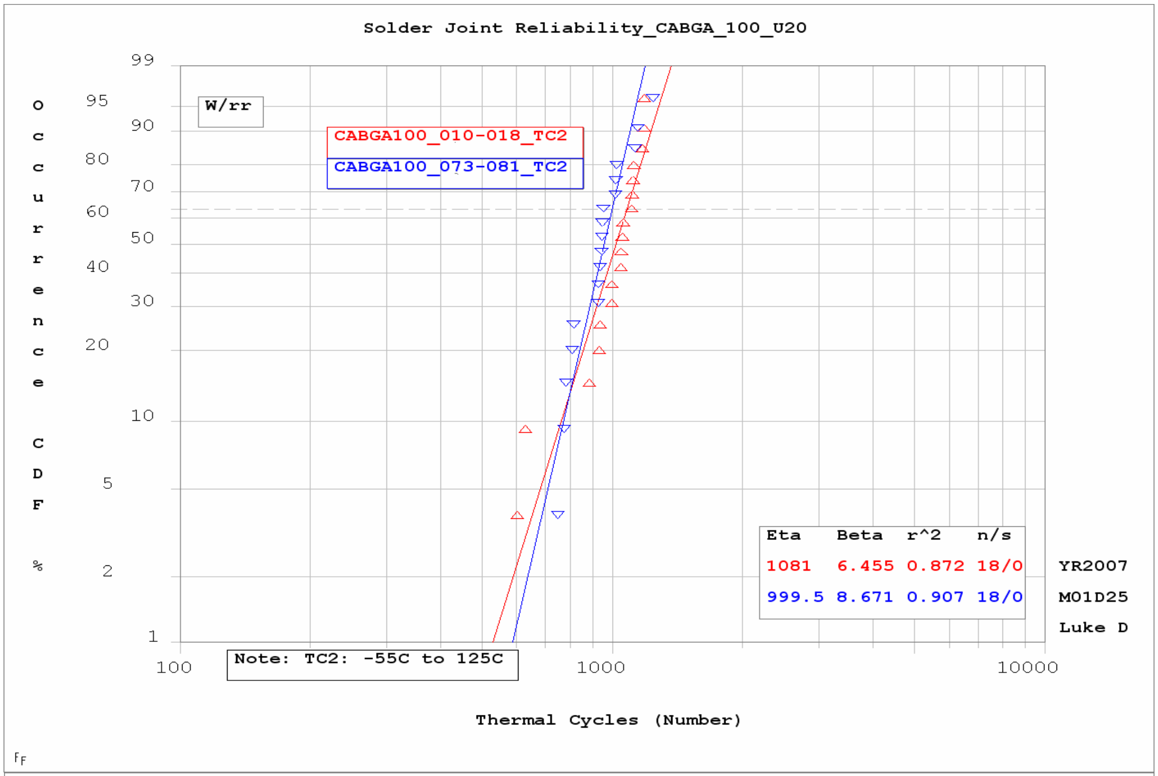
1321 4.84 0.762 35/0
YR2007
M01D24
Luke D
fF

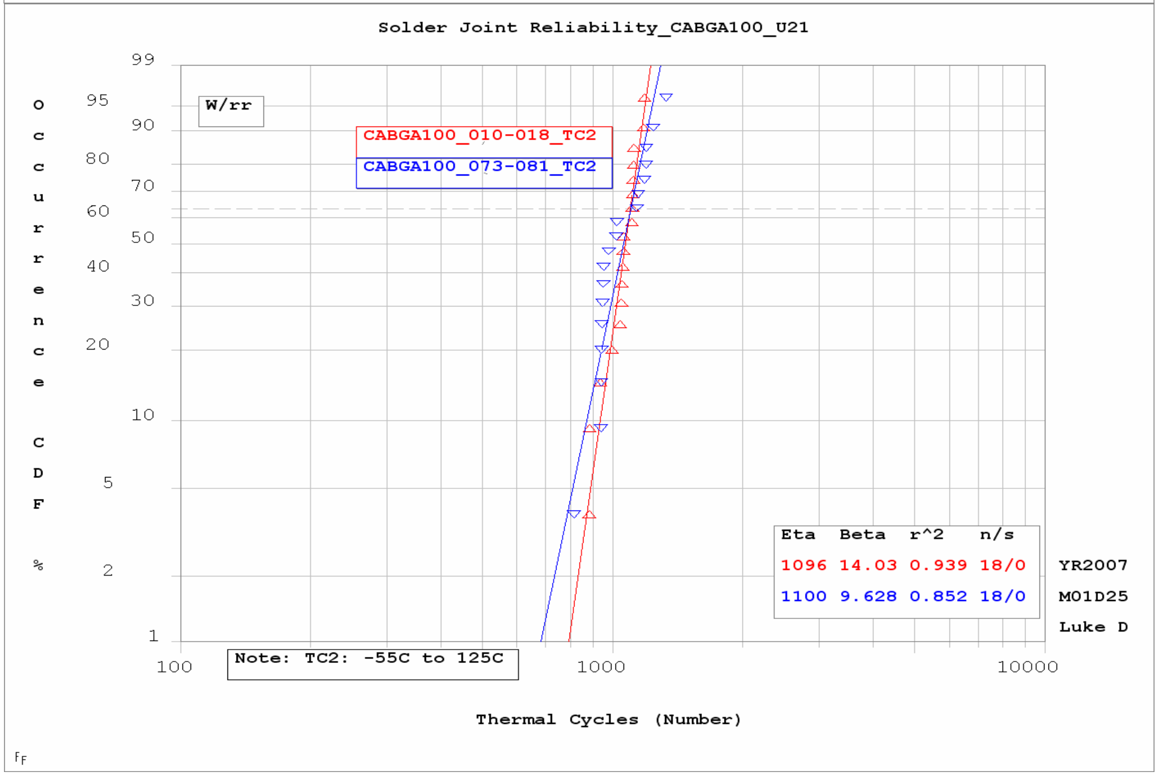

Solder Joint Reliability_TBGA_132_U16
W/rr
TBGA132_010-018_TC2
TBGA132_073-081_TC2
Occurrence CDF %
99
95
90
80
70
60
50
40
30
20
10
5
2
1
10
100
1000
10000
Eta Beta r^2 n/s
421.9 2.541 0.8 36/0
507.8 2.164 0.854 36/0
YR2007
M01D24
Luke D
Note: TC2: -55C to 125C
Thermal Cycles (Number)
fF

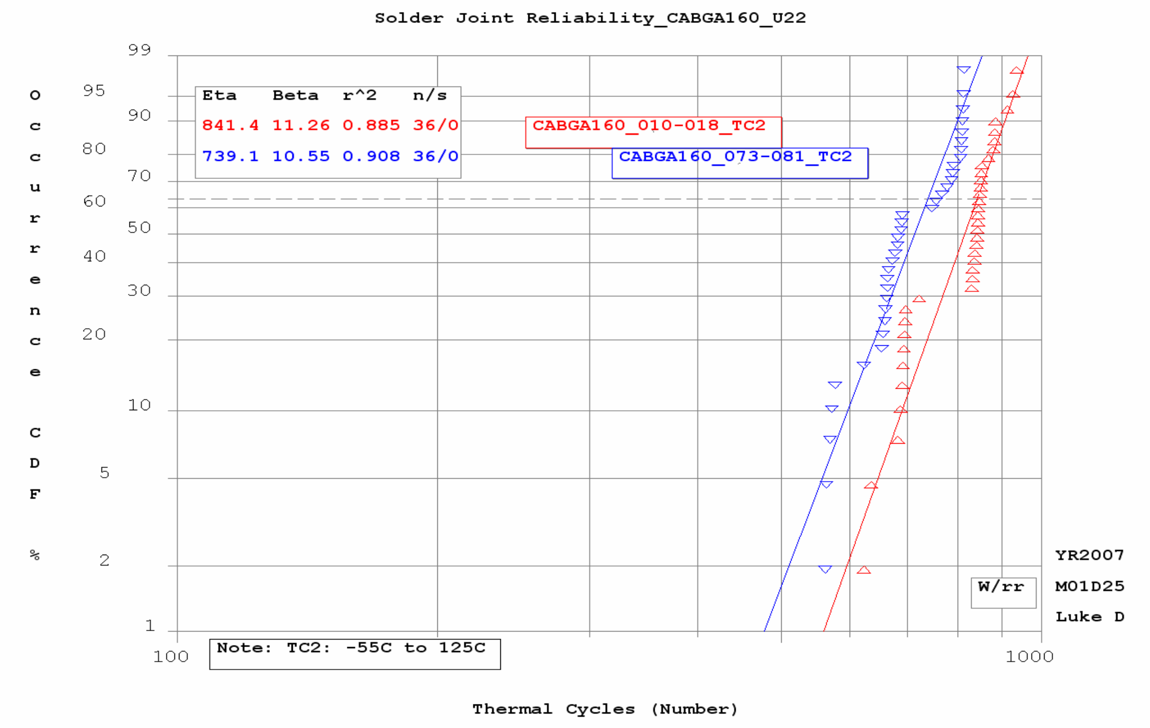

Solder Joint Reliability_TBGA132_U17
W/rr
TBGA132_010-018_TC2
TBGA132_073-081_TC2
Occurrence CDF %
99
95
90
80
70
60
50
40
30
20
10
5
2
1
10
100
1000
Eta Beta r^2 n/s
340 4.541 0.884 36/0
390.2 3.314 0.856 36/0
Luke D
Note: TC2: -55C to 125C
Thermal Cycles (Nember)
fF

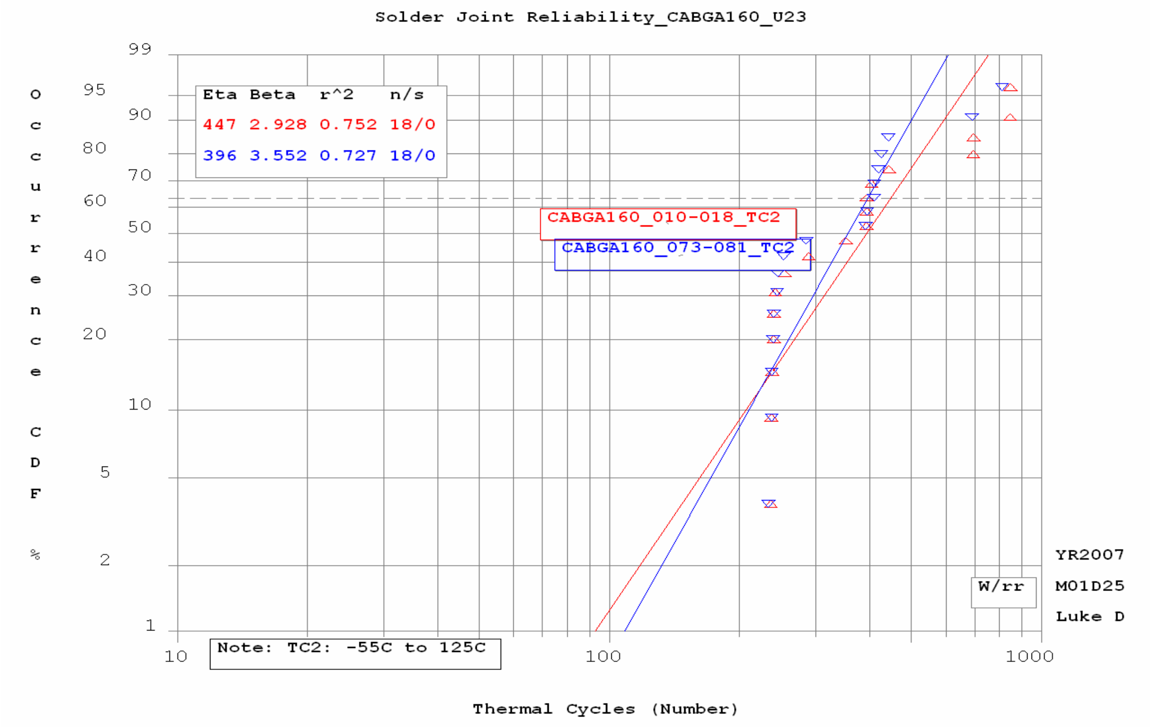

Solder Joint Reliability_PBGA144_U18
W/rr
PBGA144_010-018_TC2
Occurrence CDF %
99
95
90
80
70
60
50
40
30
20
10
5
2
1
100
1000
10000
Eta Beta r^2 n/s
858.8 2.451 0.923 36/0
YR2007
M01D24
Luke D
Note: TC2: -55C to 125C
Thermal Cycles (Number)
fF

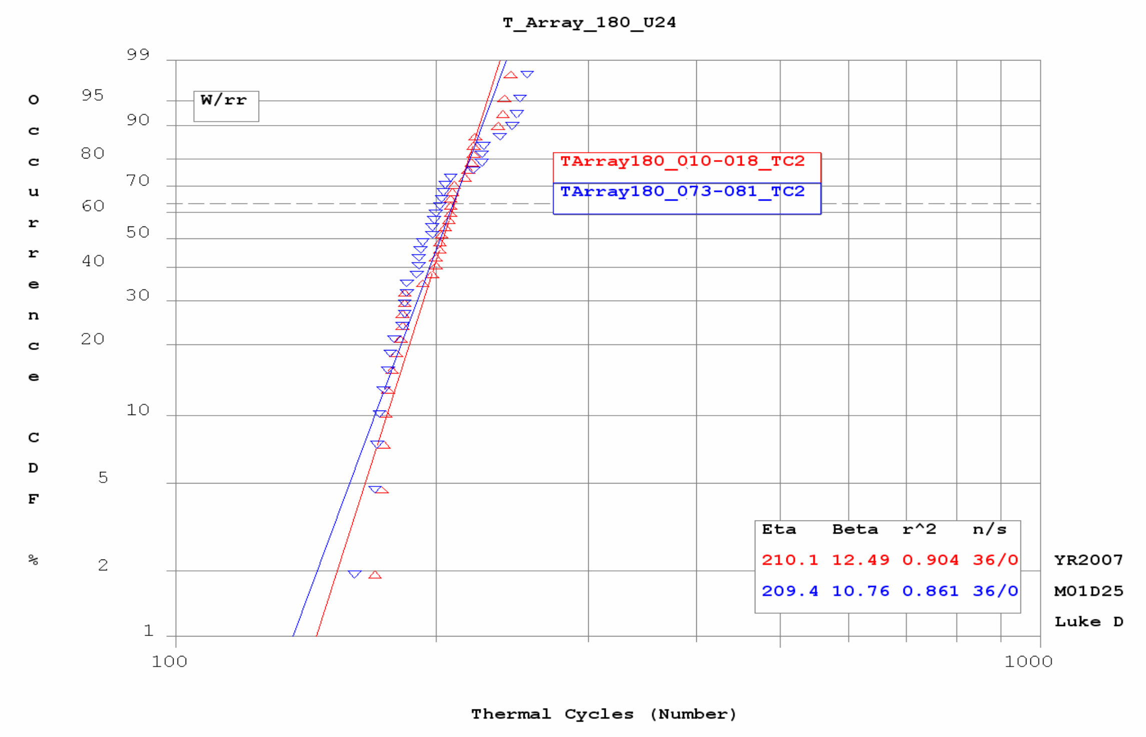

Solder Joint Reliability_CABGA100_U19
W/rr
CABGA100_010-018_TC2
CABGA100_073-081_TC2
Occurrence CDF %
99
95
90
80
70
60
50
40
30
20
10
5
2
1
100
1000
10000
Eta Beta r^2 n/s
1315 8.678 0.967 36/0
1298 9.634 0.927 36/0
YR2007
M01D24
Luke D
Note: TC2: -55C to 125C
Thermal Cycles (Number)
fF

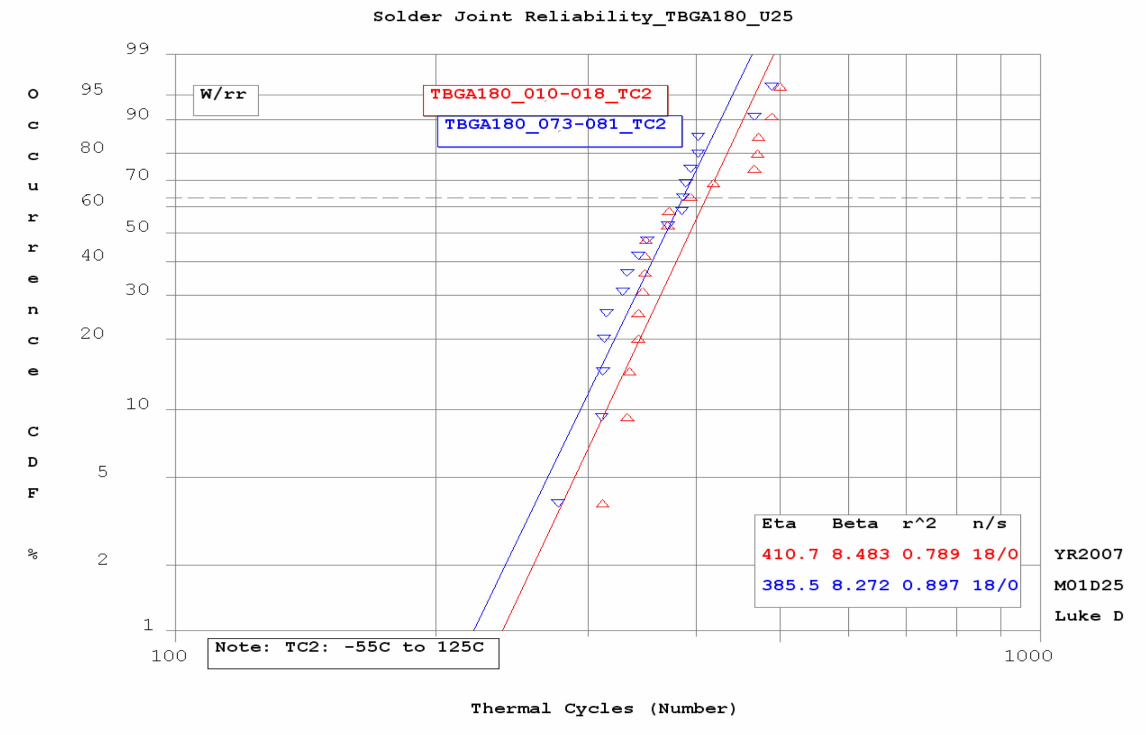

Solder Joint Reliability_CABGA_100_U20
W/rr
CABGA100_010-018_TC2
CABGA100_073-081_TC2
Occurrence CDF %
99
95
90
80
70
60
50
40
30
20
10
5
2
1
Eta Beta r^2 n/s
1081 6.455 0.872 18/0
999.5 8.671 0.907 18/0
YR2007
M01D25
Luke D
100
1000
10000
Note: TC2: -55C to 125C
Thermal Cycles (Number)

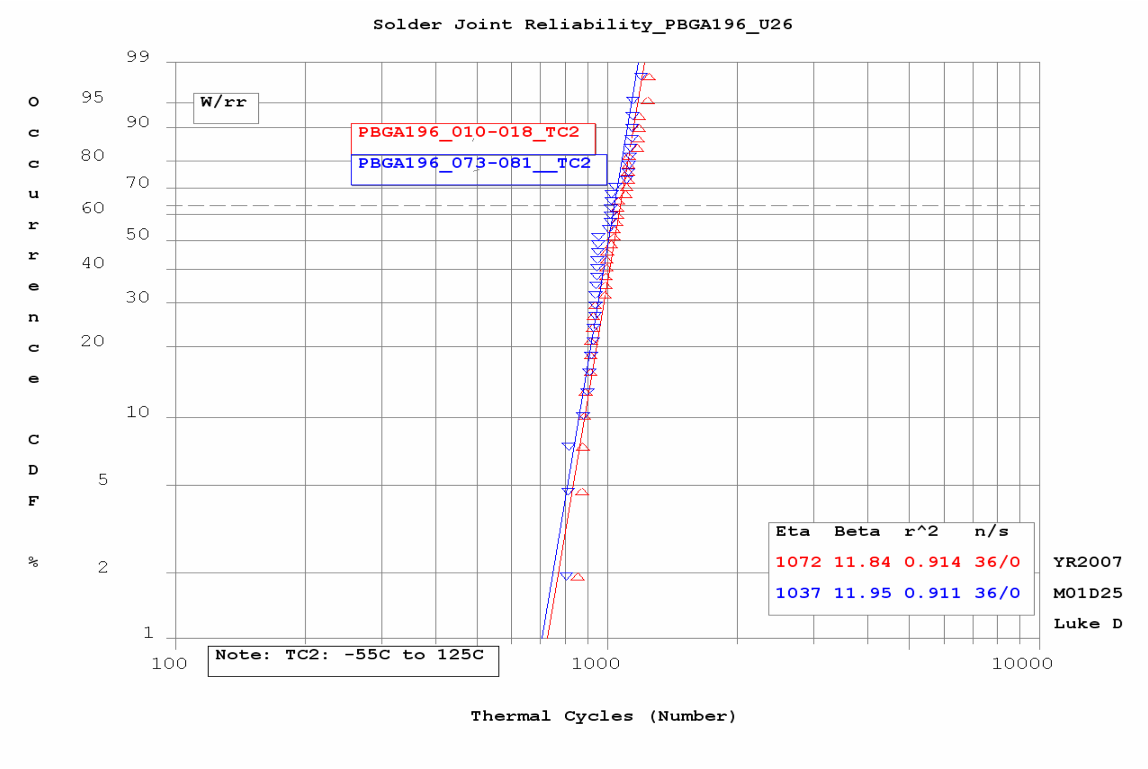

Solder Joint Reliability_CABGA100_U21
W/rr
CABGA100_010-018_TC2
CABGA100_073-081_TC2
Occurrence CDF %
99
95
90
80
70
60
50
40
30
20
10
5
2
1
Eta Beta r^2 n/s
1096 14.03 0.939 18/0
1100 9.628 0.852 18/0
YR2007
M01D25
Luke D
100
1000
10000
Note: TC2: -55C to 125C
Thermal Cycles (Number)


Solder Joint Reliability_CABGA160_U22
Occurrence CDF %
99
95
90
80
70
60
50
40
30
20
10
5
2
1
Eta Beta r^2 n/s
841.4 11.26 0.885 36/0
739.1 10.55 0.908 36/0
CABGA160_010-018_TC2
CABGA160_073-081_TC2
YR2007
M01D25
Luke D
W/rr
Note: TC2: -55C to 125C
100
1000
Thermal Cycles (Number)


Solder Joint Reliability_CABGA160_U23
Occurrence CDF %
99
95
90
80
70
60
50
40
30
20
10
5
2
1
Eta Beta r^2 n/s
447 2.928 0.752 18/0
396 3.552 0.727 18/0
CABGA160_010-018_TC2
CABGA160_073-081_TC2
YR2007
M01D25
Luke D
W/rr
Note: TC2: -55C to 125C
10
100
1000
Thermal Cycles (Number)


T_Array_180_U24
W/rr
TArray180_010-018_TC2
TArray180_073-081_TC2
Occurrence CDF %
99
95
90
80
70
60
50
40
30
20
10
5
2
1
100
1000
Thermal Cycles (Number)
Eta Beta r^2 n/s
210.1 12.49 0.904 36/0
209.4 10.76 0.861 36/0
YR2007
M01D25
Luke D


Solder Joint Reliability_TBGA180_U25
W/rr
TBGA180_010-018_TC2
TBGA180_073-081_TC2
Occurrence CDF %
99
95
90
80
70
60
50
40
30
20
10
5
2
1
100
1000
Note: TC2: -55C to 125C
Thermal Cycles (Number)
Eta Beta r^2 n/s
410.7 8.483 0.789 18/0
385.5 8.272 0.897 18/0
YR2007
M01D25
Luke D


Solder Joint Reliability_PBGA196_U26
W/rr
PBGA196_010-018_TC2
PBGA196_073-081__TC2
Occurrence CDF %
99
95
90
80
70
60
50
40
30
20
10
5
2
1
100
1000
10000
Thermal Cycles (Number)
Note: TC2: -55C to 125C
Eta Beta r^2 n/s
1072 11.84 0.914 36/0
1037 11.95 0.911 36/0
YR2007
M01D25
Luke D