ALTERNATIVE GROWTH AND INTERFACE PASSIVATION TECHNIQUES FOR SiO_2 ON 4H-SiC

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ALTERNATIVE GROWTH AND INTERFACE PASSIVATION TECHNIQUES FOR SiO_2 ON 4H-SiC

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ALTERNATIVE GROWTH AND INTERFACE PASSIVATION TECHNIQUES FOR SiO_2 ON 4H-SiC

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DISSERTATION ABSTRACT

ALTERNATIVE GROWTH AND INTERFACE PASSIVATION TECHNIQUES FOR SiO_2 ON 4H-SiC

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Silicon Carbide is a novel wide band gap semiconductor material with excellent thermal, chemical and electrical properties. It also shares its natural oxide SiO_2 with Si, which has been widely studied and optimized for decades. These properties make it a perfect candidate for applications in high-temperature, high-power MOS devices. Of over 200 polytypes, 4H-SiC is most commonly used, because it is among the only few commercially available polytypes that are known to be electrically and thermo-dynamically stable for making microelectronic devices. Unfortunately, the performance of such devices is limited by the poor SiO_2/SiC interface quality after the standard dry O_2 oxidation process. By far, the atomic understanding of the true physical structure and schematic of this interface still remains mystery. After applying most of the conventional passivation techniques such as NO anneal and H_2 anneal, improvements on the device performances can be clearly observed, however, the results are still far from satisfactory.

In this work, two alternative passivation techniques are applied, in order to obtain better understanding of the interface properties and achieve improved electrical characteristics and higher performance. The first technique is the alumina enhanced oxidation, which by introducing metal impurities via the ceramic alumina during the oxidation, a decreased interface-trap density (D_{IT}) and drastic increase in field effect channel mobility can be observed, however, this is also accompanied by a large amount of mobile ions inside the oxide. The results from electrical measurement of the devices as well as the possible cause and effect of those ions on the interface are discussed. Few other passivation techniques are also applied after this process for potential improvement and optimization, and the results are discussed.

Another passivation technique is the nitrogen plasma anneal, which successfully creates atomic nitrogen by microwave induced plasma to achieve an oxygen-free nitridation annealing condition. This helps for further and better understanding of the passivation effect by the sole presence of nitrogen. All the electrical results obtained are discussed in detail and also compared with standard NO results.

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CHAPTER 1

Introduction

1.1 General Introduction

The silicon-based microelectronic industry has played an essential role in the development of modern technology for the last 50 years. The major reasons that silicon is still the dominant material for most of the electronic devices are the excellent quality of its natural oxide, SiO_2 and the SiO_2/Si interface. Besides, it is also a great semiconductor material with well-developed processing technology. With the rapid evolution of modern technology, Si can no longer satisfy the demanding requirements for higher power, higher temperature devices due to its own limitations. As a result, a few wide band-gap materials have begun to draw more and more interest in this area. Among them, Silicon Carbide (SiC) is the most developed and the only material that shares the same natural oxide with Si, which enables it to utilize most of the mature fabrication techniques from Si industry, especially for Metal-Oxide-Semiconductor (MOS) electronic devices. In addition, some of its impressive properties also make it superior to others, such as the wide band-gap, high critical field, low dielectric constant, and high thermal conductivity, make SiC superior to other materials. The details are introduced in the later part of Chapter 1. All of these qualities make SiC a perfect candidate for high power, high temperature electronic devices, especially for power MOS devices, which is the main focus of this work.

The detailed structures and parameters of two MOS devices, MOS capacitor and Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) will be discussed in Chapter 2, along with the characterization and testing of these devices. A few non-ideal characteristic such as work function difference, various oxide charges and mobile ions as well as how they affect the device parameters are also discussed.

Many of the fabrication techniques for these devices do not differ significantly from Si-based devices. The equipments for fabrication and testing as well as some major fabrication processes are introduced in Chapter 3, Discussion of processing techniques will include photolithography, sputtering, rapid thermal annealing, and reactive ion etching. The test equipment will be described in detail including the capacitance-voltage (C-V) system, the current-voltage (I-V) system and the MOSFET mobility measurement system.

MOS devices have a wide range of applications, such as power switching for electric utilities, industrial motor control, hybrid and electric vehicles, as well as other industrial and military applications. Replacing Si-based power devices with SiC devices in these areas will result in higher efficiency, significant cost reduction, reduced size and weight, simpler system design, and improved reliability and durability.

However, the performance for the SiC MOS devices is hampered by the poor quality of the SiO_2/SiC interface, which is the major obstacle for the production of SiC based MOS devices currently. The standard dry oxidation yields poor performances in terms of high interface trap density and low effective channel mobility. By applying a few traditional passivation techniques, such as the nitric oxide (NO) anneal[1] and the hydrogen anneal, the performance is raised to a barely acceptable level, but is still far below expectation. Details are further discussed in Chapter 4

The major part of this work consists of studying alternate oxidation and passivation techniques on 4H-SiC MOS devices, which will be discussed in Chapter 5 and 6. In Chapter 5, the main focus is alumina enhanced oxidation (AEO)[2]; basically oxidizing samples with sintered alumina inside the furnace. These samples demonstrate lower interface traps density and drastically increased effective channel mobility. However, a huge number of mobile ions are detected inside the oxide, and it is reported that these ions is quite possibly the major cause for all the improvements to D_{IT} and mobility.[94] In this part of study, detailed results after the AEO process will be introduced, followed by the discussion of the possible cause, and the results for other anneal techniques following this AEO process will also be examined.

Chapter 6 is focused on the nitrogen plasma anneal process, which successfully introduces active nitrogen into the oxide through microwave induced plasma in an oxygen free environment. Compared with other nitridation annealing techniques such as NO or N_2O, This process allows the detailed study of the passivating effect of solely nitrogen on the SiO_2/SiC interface. And the results indicate that the passivating effects of NO or N_2O are most likely caused by the presence of nitrogen at the interface. With less amount N at the interface, this anneal efficiently reduces interface trap density (D_{IT}), especially near mid-gap and significantly increases effective channel mobility. Besides, this technique allows for more precise control of the amount of N introduced, and is also potentially capable of creating other gaseous plasmas in order to study their effect on the oxide reliability.

Lastly, a summary of all the work is presented in Chapter 7, and a discussion of possible improvements and future work is also offered.

1.2 General Information for SiC

1.2.1 Historical Review

Silicon Carbide is a compound of silicon and carbon with a 1:1 atomic ratio. The material mostly man made and rarely seen in nature where it is called moissanite - having been first discovered in a meteorite by Moissan in 1893 and named after him in 1905[3]. The first study of SiC was made in 1824 by Jöns Jacob Berzelius[4], where he mentioned a possible bond between Si and C. It was not long after the invention of the electric smelting furnace by E. H. & A. H. Cowles in 1885[5], that E.G. Acheson started manufacturing the material which was called Carborundum[6]. The crystalline products Acheson found after the process were found to have a great hardness, refractabiliy and chemical inertness. The invention had a great impact with material produced abrasion and cutting applications for a while.

Years later people also started taking interest in the electronic properties of SiC. The first Light Emitting Diode (LED) made from SiC dates way back in 1907[7]. In 1955, Lely developed a new process for growing high quality crystals[8]. However, interest in SiC waned due to the success and rapid development of Si technology. In 1978, a new procedure for substrate growth using a seeded sublimation process was introducesd by by Tairov and Tsvetkov[9]. Their discovery helped refocus attention on SiC technology development. The growth of single crystal SiC on Si was demonstrated by Matsunami et al[10] in 1981. Shortly thereafter, Cree Research was founded in 1987, and the company has become a leader in SiC growth technology and device development.

Currently, SiC is widely used for applications as both a structural material and a semiconductor material. In addition to being a favorite for abrasives and cutting materials, SiC is also used for heating elements, armor and ceramic membrane and mechanical parts. As a semiconductor material, crystalline SiC has or is being developed for blue light emitting diodes (LED) and high voltage, high temperature power electronics (ultra-fast Schottky diodes and transistors – particularly metal-oxide-semiconductor field effect transistors (MOSFET). Silicon carbide is also used as a substrate for other semiconductor materials such as gallium nitride to take advantage of its wide band gap and good thermal conductivity. Furthermore, well-known limitations set by basic material parameters for Si and the III-V compound semiconductors have further increased interest in SiC. With its excellent physical and electrical properties, especially wide bandgap, SiC is superior to Si for high temperature, high power and radiation-tolerant devices, and device development expanding rapidly, owing to the recent commercial availability of high quality substrates.

Nevertheless, results obtained for SiC MOSFETs to date are still far from satisfactory. Silicon dioxide SiO_2 is SiC's native oxide which is a great advantage considering all of the previous development work over the last 60 years for SiO_2 on Si. However, the poor quality and performance of the SiC/SiO_2 interface has hampered the development of SiC MOS power transistors. For example, there is a thin transition layer (~ 1-5nm) that exists between SiO_2 and SiC (compared to an abrupt interface for SiO_2/Si), an extra carbon as well as other defects contribute to a high interface trap density that lowers channel mobility. Details will be discussed in the later chapters, but at present, efforts are underway worldwide by scientists and engineers to solve these problems. The focus of this dissertation is the improvement of the quality and reliability of the SiO_2 layer and SiC/SiO_2 interface.

1.2.2 Polytypism

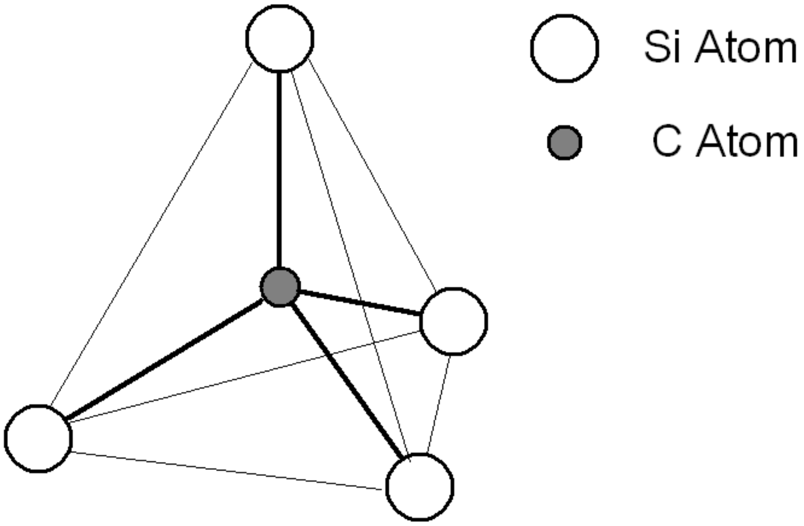


Figure 1.2.1 Tetragonal structure of the SiC crystal.

Silicon carbide occurs with different crystal structures. However, all have the Si-C bond tetragonal structure similar to diamond, with one carbon atom in the center surrounded by four silicon atoms or vice versa, as shown in Figure 1.2.1. The distance between two neighboring silicon or carbon atoms is approximately 3.08 Å for all structures[11].

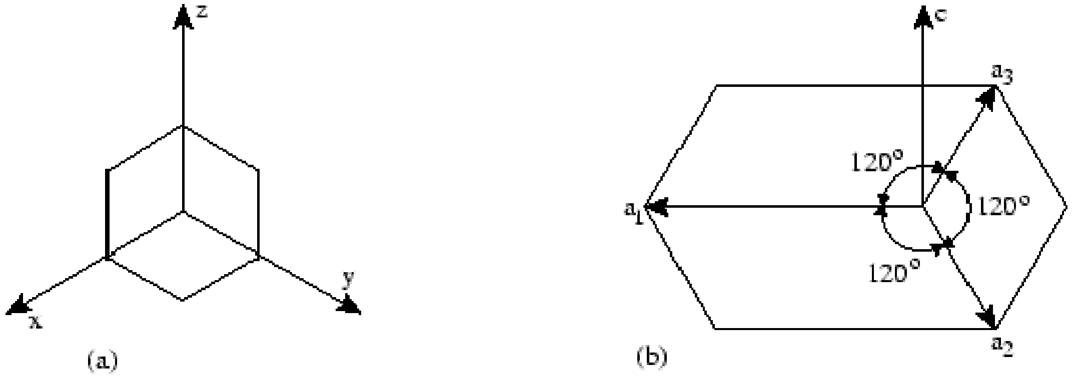


Figure 1.2.2 Unit cell for different crystal structures of SiC: (a)cubic; (b)hexagonal.

Figure 1.2.2 shows the different crystal structures for SiC. For cubic crystals, three Miller indices, *h, k, l*, are used, which are integers with the same ratio as the reciprocals of the intercepts with the x, y, z axes, respectively. For hexagonal structures four principal axes a_1, a_2, a_3 and *c* are commonly used. These three *a*-axes (with 120^o angles between them) are all in the close-packed plane called *a*-plane, whereas the *c*-axis is perpendicular to this plane.

One of the most remarkable features of silicon carbide crystal structure is its polytypism. The study of polytypism in crystals began nearly 90 years ago, and the word "polytype" was first used by Baumhauer around 1912[12] in an attempt to describe materials that crystallize with structural characteristics that differ only along one crystallographic direction. From optical studies, Baumhauer discovered two new crystal structures for silicon carbide in addition to the commonly known 6-layered hexagonal type, both differing in their stacking along the c-axis. Their existence was later confirmed by X-ray diffraction[13]. Several more new polytypes were revealed by morphological and structural studies in the 1940's and 1950's. Schneer[14] called it "polymorphism in one dimension" in order to emphasize that two dimensions of the unit cells of different polytypes are identical, while the third is a variable integral multiple of a common unit. The polytype structures are considered as stacked layers with repeat sequences ranging from 2 layers to many hundreds of layers. For the extreme case of no finite repeat, the polytype can be called a one-dimensionally disordered layer. At present, the number of known SiC polytypes exceedes 200, all with a different stacking sequence of bi-atom layers but without any variation in stoichiometry.

Physical and electrical properties vary distinctively among different polytypes. Therefore, only a few are commonly grown and developed as electronic semiconductors. Among these, the most popular polytypes are cubic SiC (3C), the hexagonal SiC (4H and 6H) and rhombohedral SiC (15R).

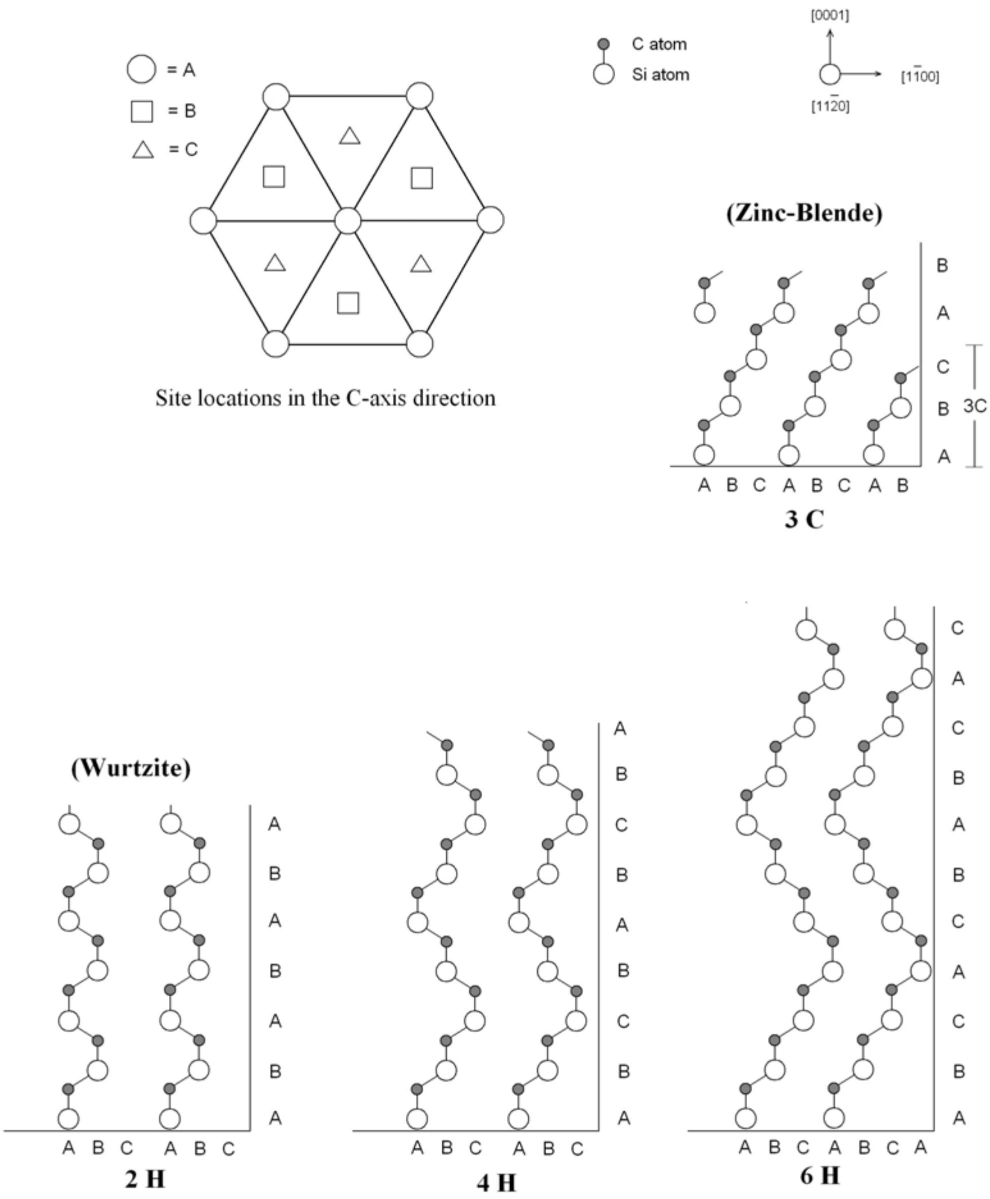


Figure 1.2.3 Stacking sequence for different SiC crystalline polytypes.

The polytypes are mainly characterized by the stacking sequence of bi-atom layers. This stacking layout can be explained as follows: As shown in the tetragonal structure of Figure 1.2.3 one carbon atom lies at the center of a triangle formed by three adhering silicon atoms below. The top silicon atom forms a bi-layer with the carbon atom, and has the same projection as the carbon atom. Let us label the locations of the atoms of this hexagonal structure bi-layer as "A" the Figure 1.2.3. The atoms of the next carbon - silicon bi-layer may either occupy a position having its bi-layer projection on "A", the same as the first layer, or on the center of the triangle not covered by the projections of the atoms of the first bi-layer, i.e., “B” and “C” in Figure 1.2.3. Different structures arise as a consequence of the fact that through successive of alterations of tetrahedral layers, a repeating unit is formed. For some polytypes, it is possible to stack up to few hundreds of bi-atom layers without repeating.

Among the most used polytypes, the cubic (a.k.a. zinc-blende) and hexagonal (a.k.a. wurtzite) crystalline structures are most commonly encountered. 3C-SiC is the only known form of SiC with a cubic crystal lattice structure. For this polytype, each bi-atom layer projects into one of those lattice positions labeled A, B and C in Figure 1.2.3. With the stacking sequence ABCABC ... The number 3 refers to the number of layers needed for periodicity, and this arrangement is also referred to as β-SiC.

The rest of the polytypes are hexagonal, and are sometimes referred to as α-SiC. For the hexagonal structure, the most common polytypes are 2H, 4H, and 6H. 2H-SiC has the bi-layer stacking sequence ABAB ..., and only this type is the simple hexagonal structure (a.k.a. wurtzite). Most of other polytypes are mixtures of the cubic and wurtsite stacking types, and may occur in complex, intermixed forms, yielding a wide range of ordered structures with large stacking period. The most widely used polytype, 4H-SiC for example, consists of an equal number of cubic and hexagonal bonds with a stacking sequence of ABCB…. Similarly, 6H-SiC is composed of 2/3 cubic bonds and 1/3 hexagonal bonds with a stacking sequence of ABCACB…. The overall symmetry, however, is hexagonal for both polytypes, despite the cubic bonds that present for each. In the same manner, 15R-SiC has a rhombohedral structure which is composed of 3/5 cubic bonds and 2/5 hexagonal bonds.

The stacking sequence can also be better visualized in the way demonstrated in Figure 1.2.3, the stacking of few common polytypes is depicted in the figure. The same A, B, C notation mentioned earlier is used here as well. For all the polytypes, the stacking of the bi-layers is always along *C*-direction. There are some 200 polytypes proven known to exist. As mentioned previously, some polytypes have a stacking period of several hundred double layers, and, in principle, an infinite number of possible stacking variants may exist. However the structures of even the highest period polytypes can be considered as combination sequences of one or more of the smaller period units such as 4H, 6H, 15R, 21R.[15]

Among the large number of polytypes of SiC, only a few are known to be electrically and thermodynamically stable. These are 2H, 3C, 4H, 15R, and 6H which are the forms of SiC currently in use. For different stacking sequences, the physical and chemical properties of these polytypes vary significantly.

1.2.3 Bulk Crystal and Epitaxial Growth

The semiconductor electronics industry requires high quality crystals for device fabrication, and SiC wafers are grown at high temperature using a high quality SiC seed sample. Epitaxial growth (from the Greek root "epi = above" and "taxis = in ordered manner") is a replicating thin film growth technique that is subsequently used with a wafer to grow SiC layers specifically tailored for a particular device.

Historically, SiC material has been produced through the Acheson process[6,16] which is still used for production of poly-crysralline SiC that is suitable for grinding and cutting applications. Some of the material produced by the Acheson process is also of adequate quality for electronic grade material growth. This Acheson process uses a mixture of silica, carbon, sawdust and common salt (e.g. 50% silica, 40% coke, 7% sawdust and 3% common salt) heated in an electric furnace to a maximum temperature of approximately 2700°C[17]. Before heating, a graphite and coke mixture is placed in the furnace with the mixture of reactants placed around this mixture. During growth, a pure graphite core layer forms in the center of the mixture, and near the core, useful SiC is found, in the form of threads of crystallites radiating from the core. The size of these crystallites decreases with increasing distance from the core, due to the temperature gradient in the furnace. Further from the core, the SiC is amorphous.

A major improvement to the Acheson process is the non-seeded process developed by Lely in 1955[8]. The Lely process is similar to the Acheson process, and growth takes place in an Ar ambient at approximately 2500°C. Lely grown material is sometimes used as a substrate for small area epitaxial growth due to the high crystalline quality of these substrates. However, Lely growth is a slow process that yields small substrate platelets with irregular sizes and shapes, and though the crystalline form is normally hexagonal, there is no real polytype control. The purity of the crystals is largely governed by the quality of the starting materials which must be obtained in a high purity form. As a result, of these problems, the non-seeded Lely method has never been considered an important technique for commercial electronic material production.

Tairov and Tsvetkov introduced a modified Lely process in 1978[8] by adding a seed crystal for sublimation growth. Their process has proved most successful, allowing good polytype control during SiC growth. Cree Research Inc. (founded in 1987) has become a leading supplier of SiC wafers grown using the modified Lely technique in which SiC powder is placed inside a cylindrical graphite crucible. The crucible is closed with a graphite lid onto which a seed crystal is attached. The crucible is heated to approximately 2200° C in an induction furnace, normally in Ar at a pressure between 1 and 100 Torr. A temperature gradient is created over the length of the crucible in such a way that the SiC powder at the bottom of the crucible is at a higher temperature than the seed crystal at top. The temperature gradient is typically kept on the order of 20 - 40°C/cm. During growth, the SiC powder sublimes, and the crucible is filled with a vapor mixture of different carbon and silicon compounds (Si_2C, SiC_2, Si_2 and Si). Since the seed is coldest part of the crucible the vapor condenses on the seed and the crystal will start to grow. The growth rate is largely governed by the temperature, pressure and the temperature gradient which determines the diffusion rate of the various species from the source to the seed. It has also been experimentally confirmed that different growth temperatures and seed crystal orientations give rise to different polytypes.[18]

The two most commonly seen defects in bulk SiC material nowadays are Micropipes and Low-Angle Grain Boundaries.

Dislocations and Micropipes: The origin and details of the micropipe formation are still topics of discussion. The first description of the formation of micropipes is F.C. Frank's theory,[19] which states that micropipes are caused by superscrew dislocations that possess a large Burgers vector, several times the unit cell dimension. The high stress along the center core of the screw dislocation causes preferential sublimation during the growth process, which consequently opens a hollow core. These hollow core screw dislocations typically run parallel to the growth direction through the entire SiC boule. The screw dislocation content of micropipes has been observed experimentally by various groups.[20,21]

Low-Angle Grain Boundaries: Low-angle boundaries tend to form near the crystal periphery during the growth of large diameter crystals. They appear as void-like linear crystallographic features extending radially inward from the wafer edge and generally follow low-index crystallographic planes. They can sometimes extend through the entire thickness of the wafer. Despite the fact that the source of these defects is still uncertain, commercial SiC wafers have seen a steady increase in size (now up to 100cm) and steady reductions in the micropipe and grain boundary defect densities.

Compared with Si, dopant species have extremely low diffusion coefficients for SiC (negligible below 1800^{o}C). Therefore, for SiC device fabrication, it is not feasible to achieve doping using diffusion techniques. The main methods currently used are either ion implantation/activation or doping during epitaxial growth. Ion implantation can introduce damage that results in reduced performance; however, one is left with no other choice when selective area doping is required. Another factor is that substrate wafer quality is not comparable to Si. For this reason, almost all the SiC electronic devices nowadays are not fabricated directly on sublimation-grown bulk wafers, but are instead fabricated on thinner, higher quality epitaxial SiC layers that are grown on modified Lely wafer. Well-grown SiC epilayers have improved electrical properties which allow more control and reproducibility. The controlled growth of high quality epilayers is important for high performance SiC devices and the technique can also be used to growth SiC on other substrates (hetero-epitaxy) including sapphire, AlN and Si.[22,23] Only homo-epitaxial growth on SiC substrates is used for high power devices.

There are several techniques available for the epitaxial growth, each with different advantage and disadvantages. Some of the most common techniques (not just for SiC) are chemical vapor deposition (CVD)[24], low pressure CVD, metalorganic CVD, molecular beam epitaxy (MBE)[25], vapor phase epitaxy, liquid-phase epitaxy, hot-wall epitaxy and sublimitation epitaxy.

Many impurities and crystallographic defects found in sublimation-grown SiC wafers do not propagate into SiC homo-epitaxial layers. For example, basal-plane dislocation loops emanating from micropipes and screw dislocations are generally not observed in SiC epilayers. However, some screw dislocations (both micropipes and closed-core screw dislocations) present in commercial c-axis wafers do replicate themselves in the epilayers. Currently, there are many observable defects in the best SiC homo-epilayers. These defects are affected by substrate defects, non-ideal substrate surface finish, surface cleaning, contamination, and/or epitaxial growth conditions. Despite these imperfections, electrical properties are generally much improved with greater device yields and improved performance.

For SiC, n-type dopants are nitrogen and phosphorus, and the common p-type dopants are Al, and B. Typical doping concentrations range from 9E+14 to 1E+19 cm^{-3}. For CVD growth, the doping concentration is governed primarily by varying the flow of the dopant gas. Additionally, the “site-competition” doping methodology[26] provides a broader range of doping concentration as well as improved repeatability. This technique is based on the fact that many dopants of SiC will preferentially incorporate into either Si lattice sites (p-type dopants) or C lattice sites (n-type dopants). If epitaxially SiC is grown under a carbon-rich environment, nitrogen incorporation in restricted. Similarly, by introducing a carbon-deficient environment during growth, the incorporation of nitrogen can be enhanced to form very heavily-doped epilayers for ohmic contacts. The same methods can be applied for p-type dopants which prefer the Si lattice sites.

1.2.4 Physical and Electrical Properties

For comparison, the major physical and electrical properties of the common polytypes of SiC along with Si and GaAs are summarized in Tables 1.2.1 and 1.2.2.

Table 1.2.1 Mechanical properties of SiC, Si and GaAs.

	Si	**GaAs**	**3C-SiC**	**6H-SiC**	**4H-SiC**	**Diamond**
Lattice a[Å]	5.43	5.65	4.36	3.08	3.08	3.567
Lattice c[Å]	n.a.	n.a.	n.a.	10.05	15.12	n.a.
Bond length [Å]	2.35	2.45	1.89	1.89	1.89	1.54
TEC [10^{-6}/K]	2.6	5.73	3.0	4.5	-	0.8
Density [gm/cm^3]	2.3	5.3	3.2	3.2	3.2	3.5
Ther.cond.[W/cmK]	1.5	0.46	3.2	4.9	3.7	20
Melting point [°C]	1420	1240	2830	2830	2830	4000
Mohs hardness	7.0	5.0~5.5	9	9	9	10

TEC = thermal expansion coefficient

Table 1.2.2 Comparison of the electrical properties of SiC, Si and GaAs.[27,28,29,30]

	Si	**GaAs**	**4H-SiC**	**6H-SiC**	**3C-SiC**
Bandgap energy [eV]	1.12	1.43	3.26	3.03	2.4
Relative dielectric constant	11.9	13.1	9.7	9.66	9.72
Breakdown Field E_B [MV/cm] (For 1KV operation)	0.25	0.4	∥c-axis:2.2	∥c-axis:2.4 ⊥c-axis:>1	>1.5
Thermal Conductivity κ[W/cmK]	1.5	0.5	3.0-3.8	3.0-3.8	3.2
Intrinsic Carrier Concentration n_i**[cm^{-3}]**	1.45E+10	1.79E+6	5E-9	1.6E-6	1.5E-1
Electron Mobility μ_n@ $N_D=10^{16}$cm^{-3} [cm^2/Vs]	1430	8500	∥c-axis: 900 ⊥c-axis: 800	∥c-axis: 60 ⊥c-axis: 400	800
Hole Mobility μ_p@ $N_A=10^{16}$cm^{-3} [cm^2/Vs]	480	400	115	90	40
Saturated Electron Velocity v**[10^{7}cm/s]**	1	1	2	2	2.5
Donors & Ionization Energy ΔE_d**[meV]**	P: 45 As: 54		N: 50, 92 P: 54, 93	N: 85, 140 P: 80, 110	N: 50
Acceptors & Ionization Energy ΔE_a **[meV]**	B: 45 Al: 67		Al: 200 B: 285	Al: 240 B: 300	Al: 270
2007 Commercial Wafer Diameter [inches]	12	6	3	3	?

The physical and electronic properties of SiC make it a superior and promising semiconductor material for electronic devices that is applicable for high power / high temperature applications for the following reasons[30]:

i) SiC's large bandgap energy translates to low intrinsic concentration even at extremely high temperatures. This permits SiC devices to operate at elevated temperatures without suffering from intrinsic conduction effects, resulting in devices that are more stable and reliable during high power / high temperature operation.

ii) A high breakdown (~x3 Si) electric field allows SiC devices to be smaller with thinner drift regions that contribute significant less drift resistance to the total on-resistance.

iii) High thermal conductivity provides much faster heat dissipation compared to Si and GaAs, potentially resulting in higher power delivery at higher frequency.

iv) High saturated electron drift velocity permits SiC devices to operate normally at higher frequencies (RF and microwave).

v) Small dielectric constant provides low parasitic capacitance and higher operating speed for MOS devices.

vi) Crystalline SiC is chemically inert, thermally stable (high melting point) with better radiation tolerance which make SiC devices suitable for operation in hostile environments.

Collectively, these properties promise SiC devices that offer tremendous benefits compared to power semiconductors (mostly Si) currently used for industrial and military applications.

CHAPTER 2

Characteristic and Theoretical Parameters for 4H-SiC MOS Devices

2.1 MOS Structures

For modern MOS (metal-oxide-semiconductor) device fabrication, the metal layer is commonly replaced by heavily doped polycrystalline silicon for better performance, although the MOS jargon is still used for historical reasons. For more general applications, an insulator layer other than SiO_2 can be used on Si or even some other semiconductor with the nomenclature metal-insulator-semiconductor (MIS). Although semiconductor technology is evolving rapidly, MOS structures still form the core structure for modern microelectronics circuit design. One of the major advantages of SiC compared with other wide band gap semiconductors is that many circuit design and device structures can be borrowed from Si since the two semiconductors have the same native oxide SiO_2. In order to take advantage of the situation, one of the major tasks at present is to improve the performance and reliability of SiC-based MOS structures. The performance of these devices is currently limited by SiO_2/SiC interface quality.

Two MOS device structures have been used for the work described herein - the MOS capacitor and MOSFET (metal-oxide-semiconductor field effect transistor). The two terminal MOS capacitor is the simpler structure. Fabricating the capacitor is straightforward, and essential information related to characteristics and properties of all MOS devices device can be obtained from MOS capacitor studies, especially information about interfacial trap density, transition layer formation and oxide breakdown. MOSFETs on the other hand, are three terminal devices that are more often used in actual circuits. For example, the Si MOSFET-based IC circuit is still the most pervasive technology in semiconductor industry. At present, there are already hundreds of different MOSFET designs available, each tailored for a specific application. However, in this work, we only focus on the simple lateral MOSFET structure in order to determine basic device characteristics such as inversion channel mobility. Lower than expected channel mobility is still one of the major obstacles that limits the performance of 4H-SiC inversion-mode MOSFETs.

2.2 MOS Capacitor

2.2.1 General Introduction

The metal-oxide-semiconductor capacitor (MOS CAP) is the most basic device of all the MOS structures. It has four modes of operation, accumulation, flatband, depletion and inversion. Studying the MOS capacitor provides important information about the oxide, the oxide-semiconductor interface and even the semiconductor substrate. Also, most MOS CAP parameter relate directly to MOSFET performance, which make the capacitor an important tool for process/quality control. Another major advantage of studying the MOS CAP is the simplicity of the fabrication process for this simple structure. Hence, the MOS CAP is the most popular device for MOS characterization.

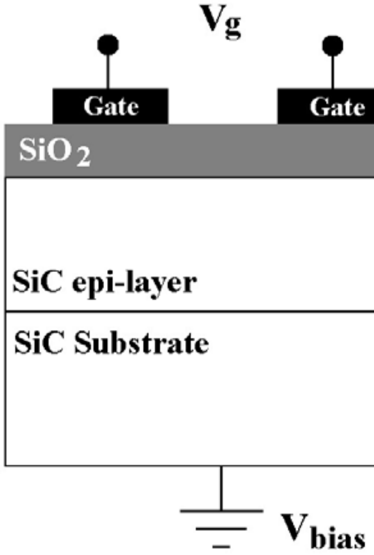


Figure 2.2.1 Two dimensional diagram for a MOS capacitor.

Figure 2.2.1 shows the two dimensional diagram for a MOS capacitor. The top circular metal contact is defined by photolithography and metal deposition mentioned in Chapter 1, with circular patterns that have varying radii. On SiC, materials commonly used as gate contacts are molybdenum, aluminum, and highly doped polycrystalline silicon. For the back side contact, a metal forming Ohmic contact is typically used; however, for all the MOS capacitor studies in this work, colloidal silver paint was used to form a broad area (5mm×5mm minimum) back side contact. Though the backside contact was not annealed, the large area provided a reasonably low MOS capacitor series resistance that was typically $< 100\Omega$.

The ideal MOS structure[31] has the following characteristics. (1) the metallic gate is thick enough to be considered at equipotential surface; (2) the oxide is a perfect insulator with no current flowing under all static biasing conditions; (3) there are no charge located at the interface or through the oxide; (4) the substrate is uniformly doped; (5) the semiconductor bulk is thick enough so that a field-free region encountered before reaching the back contact for any gate bias; (6) an Ohmic contact is used for back contact; (7) all the variables can be treated in a one dimensional structure; (8) at equilibrium, the Fermi levels E_F on metal and semiconductor sides are at the same energy, which also can be expressed as:

$$\Phi_M = \chi + (E_C - E_F)_\infty \quad \text{(Eq 2.2.1)}$$

Where Φ_M is the metal work function, χ is the semiconductor electron affinity, and E_C and E_F are the energies of the semiconductor conduction band edge and the Fermi level, respectively (see Figure 2.2.2). In real devices however, while some of the above assumptions hold, others often do not. For example, oxide leakage current and charge at interface and in the oxide are still problems that greatly limit the performance and reliability of SiC MOS devices. Our studies of SiC MOS capacitors are aimed at identifying non-ideal properties and attempting improvements.

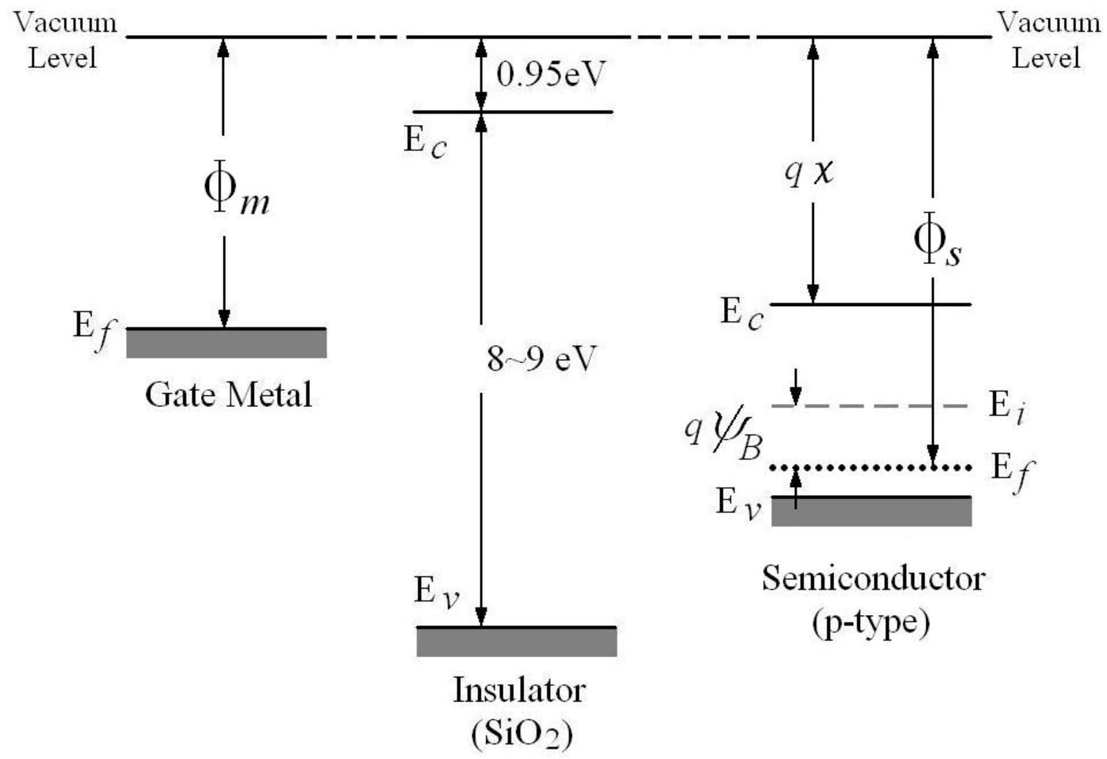


Figure 2.2.2 Energy band diagram of a MOS capacitor on a p-type semiconductor.[32,33]

Figure 2.2.2 shows band diagrams for the energy levels of the different components of a p-type MOS capacitor. The reference potential for energy band diagram is usually set at the *Vacuum Level*, which is defined as the energy level of an electron at rest after it is removed from the crystal lattice. On the metal side, the energy difference between the Fermi level and vacuum level is called the *Work Function* of the metal Φ_M which varies for different metals. SiO_2 is an insulator with a large energy gap E_C-E_V ~ 8-9eV. The energy difference between the vacuum level and the oxide conduction band edge is around 0.95eV. Lastly, on the semiconductor side, the energy difference between E_C and vacuum level is the *Electron Affinity* (χ) which is the minimum energy necessary to remove an electron with energy E_C from the semiconductor. For Si, χ is 4.05eV while for 4H and 6H-SiC, χ is around 3.9eV and 3.65eV, respectively[34]. In other words, the potential barrier between the conduction bands of the semiconductor and the SiO_2 is 4.05eV−0.95eV = 3.1eV for Si, while for 4H-SiC, it is 2.7eV. This parameter is important when one considers oxide reliability and electron/hole injection under different bias conditions.

2.2.2 Operating Modes and Surface Potential under Gate Bias

As mentioned previously, when under a gate bias, a typical MOS capacitor will have four operating modes, accumulation, flatband, depletion and inversion. As shown below, Figure 2.2.3 & Figure 2.2.4 are the band diagrams of both p-type and n-type ideal MOS capacitor under different bias conditions. We will discuss the details of the four modes of operation taking the ideal n-type MOS capacitor as an example.

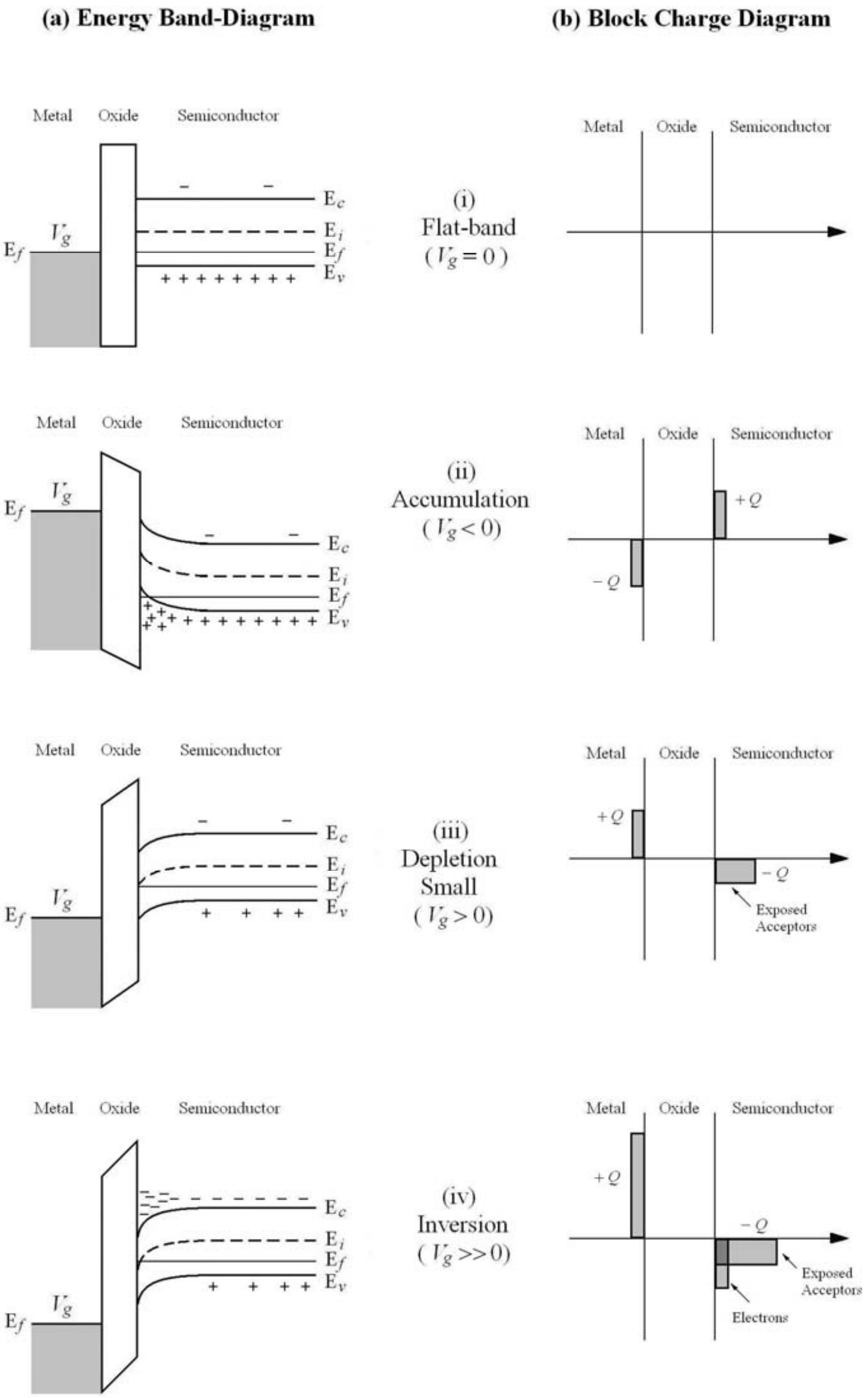


Figure 2.2.3 Band diagram and corresponding block charge diagrams of p-type ideal MOS capacitor under different static bias condition.[31,35]

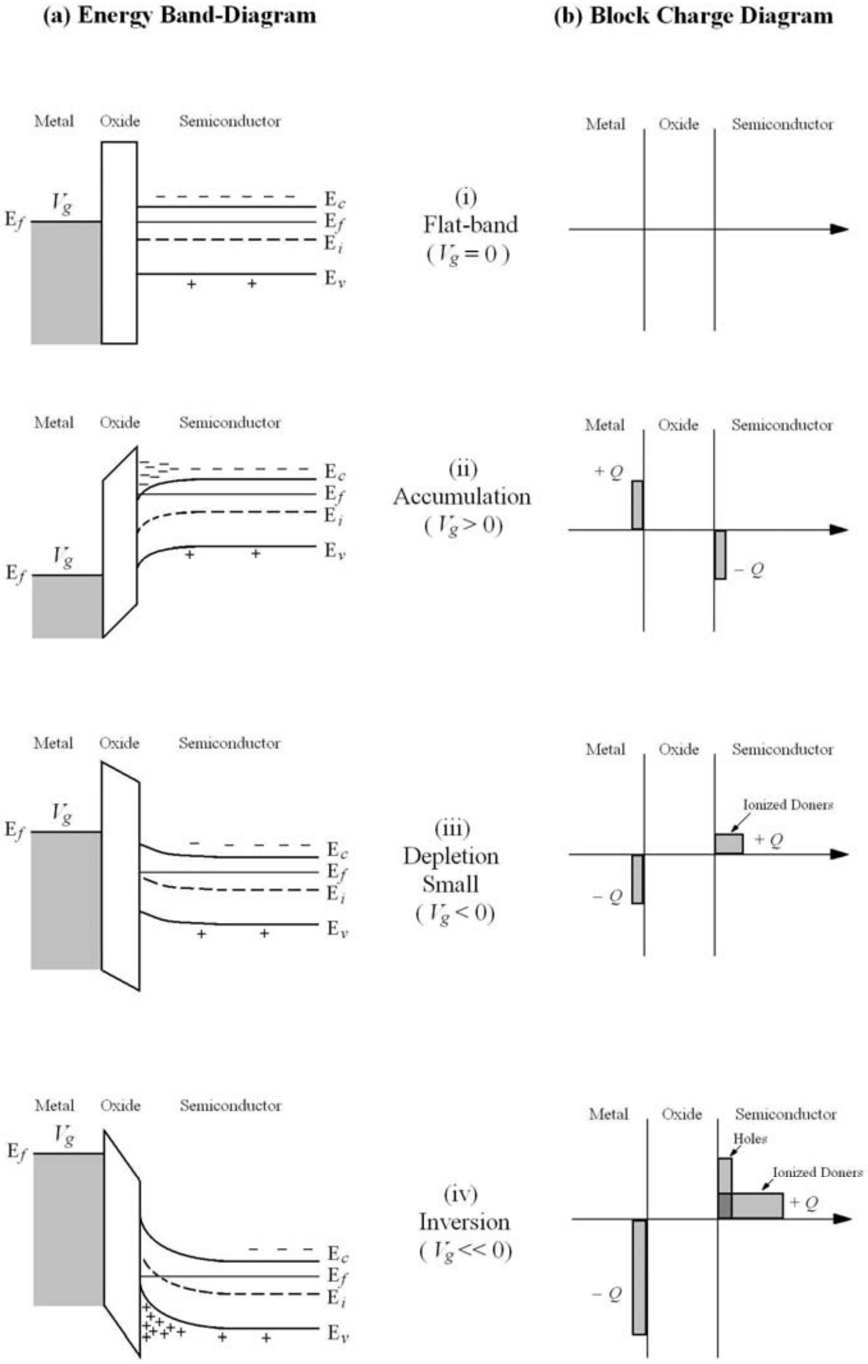


Figure 2.2.4 Band diagram and corresponding block charge diagrams of n-type ideal MOS capacitor under different static bias condition.[31,35]

i) Flatband

For simplicity, we are assuming the metal work function Φ_M and electron affinity χ in semiconductor are related following Eq.2.2.1. When there is no applied voltage between the metal and semiconductor, their Fermi levels must to line up, and in the ideal case, their vacuum levels line up as well. All the bands in both the oxide and semiconductor are flat. Hence there is no charge, no field and no current flow. This is called the *flat-band condition*. However, in non-ideal cases, as mentioned in section 2.2.4, the difference between Φ_M and Φ_S, and the presence of different types of charges at the interface and throughout the oxide layer, require that an initial gate bias voltage be applied to achieve the flat-band condition. This voltage is called the *flat-band voltage*, V_{FB}.

ii) Accumulation

Let us take an n-type semiconductor as an example, and consider the situation when a positive gate voltage is applied. The gate bias V_G lowers the Fermi level E_F on the metal side relative to E_F in the semiconductor and causes a positive sloping of the energy bands in both the insulator (SiO_2) and semiconductor, as shown in Figure 2.2.4(ii). Due to this field, the bands inside the semiconductor will bend downward toward the oxide interface, although the Fermi level will stay flat when there is no current flow. The potential at the semiconductor surface is called the *surface potential*. Because of this bending, the Fermi level at the surface is much closer to the conduction band than is the Fermi level deep into the bulk. As a result, the electron concentration inside the semiconductor which is given by $n = n_i \exp[(E_F\text{-}E_i)/kT]$, increases when approaching the oxide/semiconductor interface. This situation, where the majority carrier concentration is greater near the oxide/semiconductor interface than in the bulk of the semiconductor, is called *accumulation*.

Another way to look at this situation is from the block charge diagram. When a gate bias V_G>0 is applied. Positive charges will be induced at the metal/oxide interface. Inside of the bulk semiconductor, negatively charged electrons will be drawn toward the oxide/semiconductor interface by the field. At equilibrium, the charges at both interfaces will reach a charge balance.

iii) Depletion

Under the same assumptions, consider next a small negative voltage V_G applied to the gate. The metal Fermi level E_F rise slightly towards E_F in the semiconductor, and the energy bands in both the oxide and semiconductor bend with a negative slope, as shown in Figure 2.2.4 (iii). Due to the field induced by the gate voltage, the bands bend upward toward the oxide/semiconductor interface. Since the conduction band at the interface now is farther away from the Fermi level than deeper into the bulk, the majority carrier concentration, in this case the electron concentration, will be lower at the interface than into the bulk semiconductor. This situation is known as *Depletion*. Similarly from the charge distribution point of view, when gate voltage $V_G<0$ is applied, negative charge will be induced on the metal side. As for the semiconductor side, electrons are repelled away from the oxide/semiconductor interface, leaving only positive donor sites. Both electron and hole concentrations at the oxide-semiconductor interface are very low, or *depleted*. This near-interface region is therefore known as the *depletion region*.

iv) Inversion

Now consider depletion, but instead with a larger negative gate bias V_G applied to the metal gate. The bands at the oxide/semiconductor will further bend up, resulting in a wider depletion region and more depletion charge. The bending continues with larger negative bias until the intrinsic level (~mid-gap energy) at the interface becomes higher than the Fermi level, as shown in Figure 2.2.4 (iv). After this point, the semiconductor will behave like p-type material near the oxide/semiconductor interface. In other words, the field is so large that all the electrons are depleted from the interface, and the surface potential is such that it is energetically favorable for holes to populate the conduction band. The positive charge in the semiconductor consists of both the ionized donors and the thermally generated holes driven by the electric field to populate the interface region. Driven by the large applied field instead of doping, the minority carrier concentration at the oxide/semiconductor interface exceeds the bulk majority carrier concentration, and this situation is referred to as i*nversion*. From the band diagram, this situation happens when[31,36]

$$E_i\text{ (surface)} - E_i\text{ (bulk)} = 2[E_F - E_i\text{ (bulk)}] \quad \text{(Eq 2.2.2)}$$

The gate voltage V_G during the dividing of the depletion and inversion is simply called the depletion-inversion transition point. This equation applies to both n-type and p-type devices. Eq 2.2.2 can also been written as

$$\phi_S = 2\phi_F \quad \text{(Eq 2.2.3)}$$

Here, $\phi_S = \frac{1}{q}[E_i(bulk) - E_i(surface)]$ ……………….……..……... (Eq 2.2.4a)

$$\phi_F = \frac{1}{q}[E_i(bulk) - E_F] \quad \text{(Eq 2.2.4b)}$$

Here, ϕ_S is defined as the potential evaluated at the oxide/semiconductor interface, also known as the surface potential, measured with the potential in the field-free region deep into the substrate as a reference point. ϕ_F is simply defined by Eq 2.2.4b, and it is an important material parameter for determining substrate material type and doping concentration. A graphic depiction of ϕ_S and ϕ_F is shown in Figure 2.2.5.

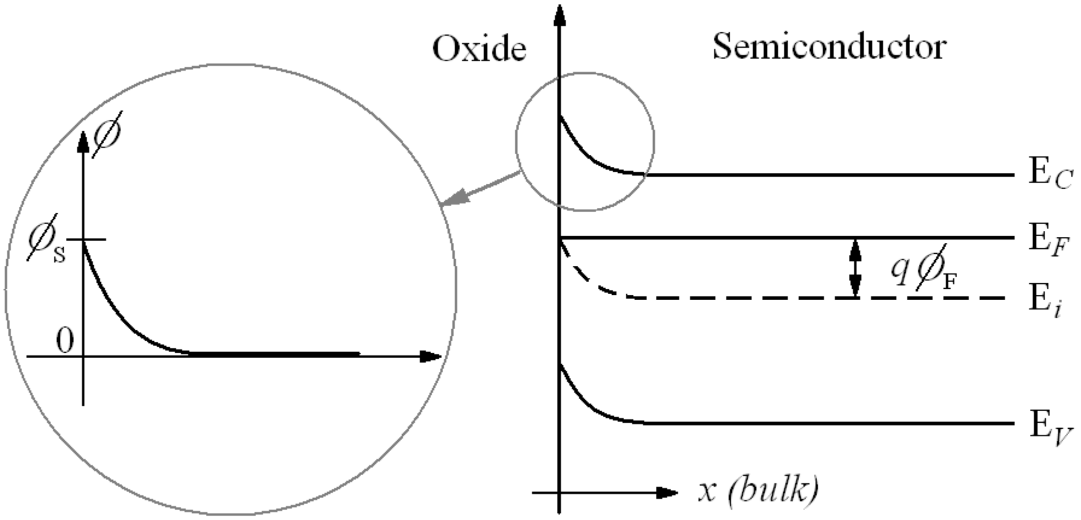


Figure 2.2.5 Graphical definition of parameters ϕ_S and ϕ_F on the band diagram.

2.2.3 High-Low Frequency Capacitance-Voltage Measurement

Since the insulating layer sandwiched in an MOS capacitor structure blocks DC current flow, AC measurements must be used to measure the characteristics of the capacitor. One AC techniques is capacitance measurement with changing gate voltage. This method is known as Capacitance-Voltage (C-V) measurement.[109] As discussed previously, there are four operating modes for a MOS capacitor. Therefore, the measured capacitance will change according to the operating mode. Most of the non-ideal characteristics of the device will have some effect on the measured C-V curve. So studying of the C-V characteristics can reveal lots of information about the nature of the oxide and the oxide-semiconductor interface.

All the C-V data are extracted using the simultaneous high-low frequency C-V probe station mentioned in Chapter 3. The measurement process is done automated to sweep from the accumulation to depletion with a slowly changing DC voltage to obtain a continuous quasi-static C-V curve. Simultaneously, a high frequency AC signal (100KHz in our case) is also applied between the gate and back contact. This AC signal adds and subtracts a small charge ΔQ for each applied DC bias. Please refer to Chapter 3 for further details about the actual measurement. Now taking an n-type MOS capacitor as an example, let us look at its capacitance behavior under different bias modes:

i) In accumulation, the majority carriers inside the bulk semiconductor (electrons in this case) will be piling up at the oxide/semiconductor (O-S) interface due to the energy band bending. The AC signal will then be adding and subtracting a small charge ΔQ to the charges on both sides of the oxide layer. The accumulated MOS capacitor can be approximated as a single parallel-plate capacitor. That is:

$$C(acc) \cong C_O = \frac{K_O \varepsilon_0 A_G}{x_0} \qquad \text{(Eq 2.2.5)}$$

where A_G is the area under the gate metal, x_o is the thickness of the oxide layer, and K_O is the dielectric constant of oxide.

ii) The depletion situation is a totally different picture. Under a negative DC gate bias, as shown in Figure 2.2.4 (iii), the field created will push the majority carriers away from the O-S interface and create a depletion region. The width of this depletion region, W, will respond very rapidly to the AC signal which results in the small variation of the depletion width while the signal is still adding and subtracting a small ΔQ on the gate. This situation can approximated as two layers of insulator, one the oxide, and the other the depletion region with depth W. In other words, they can be treated as two parallel plate capacitors in series. Take C_O as the capacitance of oxide layer, C_S as the capacitance of semiconductor due to the depletion region, they are expressed as:

$$C_O = \frac{K_O \varepsilon_0 A_G}{x_o} \qquad \text{(Eq 2.2.6 a)}$$

$$C_S = \frac{K_S \varepsilon_0 A_G}{W} \qquad \text{(Eq 2.2.6 b)}$$

Here A_G, x_o, and K_O are the same as defined in Eq 2.2.5, K_S is the dielectric constant for the semiconductor and W is the width of the depletion region.

The total capacitance C(depl) between the gate and back contact is then:

$$C(depl) = \frac{C_O C_S}{C_O + C_S} = \frac{C_O}{1 + \frac{K_O W}{K_S x_o}} \qquad \text{(Eq 2.2.7)}$$

In Eq 2.2.7, the only variable that changes with gate bias is W, which will increase when the negative gate bias increases in magnitude, As a result, C(depl) continuously decreases slightly when the device is bias deeper into depletion.

iii) When the MOS capacitor is further biased into inversion, the depletion layer will stop at its maximum width which depends on the doping concentration of the bulk semiconductor. Because the bands are bending up due to the field, E_F moves closer to E_V, and this results in the piling up of the minority carriers (holes at the oxide-semiconductor interface. However, the effect of the AC signal depends on the signal frequency.

If the AC frequency is very low ($\omega \to 0$), the situation can be treated as one of quasi-equilibrium for the generation-recombination process for minority charges. A small charge ΔQ will be added and subtracted at both edges of the oxide layer, similar to accumulation situation, therefore, the capacitance should be:

$$C(inv) \cong C_O \qquad \text{when } \omega \to 0 \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \text{(Eq 2.2.8 a)}$$

On the other hand, if the AC frequency is very high ($\omega \to \infty$), the comparatively large delay constants for the generation and annihilation of charges will make this process unable to respond to the applied AC signal. However, the depletion width W will then start to respond and fluctuate according to the signal. This will result in the similar situation as depletion, the device can be considered as two parallel plate capacitors in series:

$$C(inv) = \frac{C_O C_S}{C_O + C_S} = \frac{C_O}{1 + \dfrac{K_O W}{K_S x_o}} \qquad \text{when } \omega \to \infty \quad \ldots\ldots\ldots\ldots\ldots \text{(Eq 2.2.8 b)}$$

Also worth mentioning here is that this effect can be easily observed for silicon-based MOS capacitors. However for SiC, due to its wide energy band gap and the 100KHz AC signal that we are using, it is nearly impossible to bias into deep inversion and see this effect under normal measurement conditions. According to the equipment manual[37], the optimum voltage range should be chosen such that depletion region covers about 1/3 to 2/3 of the whole voltage range, which in our case, means the stop voltage will still be in depletion region. In other words, all our C-V measurements only sweep from accumulation to depletion (or depletion to accumulation), and never into inversion. We thus focus on the analysis and discussion of the C-V characteristics from accumulation to depletion.

2.2.4 Non-ideal Characteristic of MOS Capacitor

All the previous discussions treated the device as an ideal MOS capacitor, following the assumptions listed in section 2.2.1. However, all real MOS devices rarely meet the idea conditions. The main goal of this work is to improve the performance and quality of SiC MOS devices by reducing or minimizing the non-idealities which limit device performance. So it is important to study and understand the physical origin of non-ideal characteristics and the effect they have on the important device parameters such as V_{FB} (flat band voltage), D_{IT} (interface trap density), V_{Th} (threshold voltage) and channel mobility.

2.2.4.1 Metal-Semiconductor Work Function Difference

The definition of the work function on an energy-band diagram is the energy (or potential) difference between the vacuum level and the Fermi level. As shown on Figure 2.2.5, the work function of the metal is Φ_M, and the work function of the semiconductor is Φ_S, For ideal case with Eq 2.2.1, $\Phi_M = \chi + (E_C - E_F)_\infty$, in other words, $\Phi_M = \Phi_S$, meaning vacuum and Fermi levels on both the metal side and semiconductor side line up perfectly under flat band conditions.

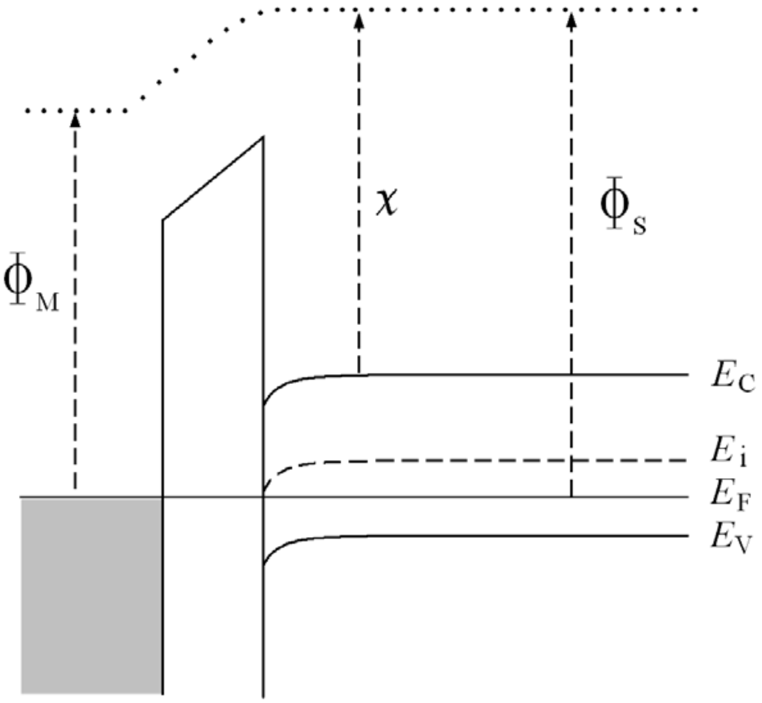


Figure 2.2.6 Energy band diagram of real MOS capacitor of $\Phi_M \neq \Phi_S$,
under no gate bias (V_G=0).

However, in most cases, Φ_M is not equal to Φ_S. Consider the situation in Figure 2.2.6, when metal, oxide, and semiconductor are brought together to form a MOS capacitor. After reaching the equilibrium state, all their Fermi levels must align. In other words, E_F for both metal and semiconductor are at the same energy. However, $\Phi_M \neq \Phi_S$, and as a result, their vacuum level will at deferent energies as shown on Figure 2.2.6. The energy bands inside the semiconductor bend due to the energy difference on the two sides of the oxide layer. In order to reach the flat band condition, a gate bias voltage is necessary to introduce a field that bends the bands in the other direction, correcting this built-in potential difference, which is noted as ϕ_{MS}. From Figure 2.2.6, it is obvious that the built-in energy difference is the work function energy difference for the metal and semiconductor. To get the value of ϕ_{MS}, the factor of 1/q is placed in the equation in order to express this energy difference (in eV) in volts. Therefore, ϕ_{MS} can be expressed as

$$\phi_{MS} = \frac{1}{q}(\Phi_M - \Phi_S) \text{ .... (Eq 2.2.9)}$$

For n-type 4H-SiC MOS capacitors, this value of ϕ_{MS} is typically not large, around 0.87Volts. Due to this build-in offset potential (and not just the flat-band condition, but also for any point on the ideal C-V curve), one must always add ϕ_{MS} (in volts) into the applied gate voltage to achieve the same degree of band bending, resulting in a shift of ϕ_{MS} of the C-V curve of an real device compared from its ideal characteristic along the voltage axis.[31] This shift in applied gate voltage ΔV_G can be expressed as:

$$\Delta V_G = (V_{G(real)} - V_{G(ideal)})|_{same\,\phi_S} = \phi_{MS} \text{ .... (Eq 2.2.10)}$$

2.2.4.2 Oxide Charges and V_{FB}

In addition to the work function difference, another major factor responsible for the shift of the applied gate voltage ΔV_G is various types of charges at the oxide/semiconductor interface and throughout the oxide. Sometimes these charges can result in a very large voltage shift which poses a severe problem for MOS device performance.

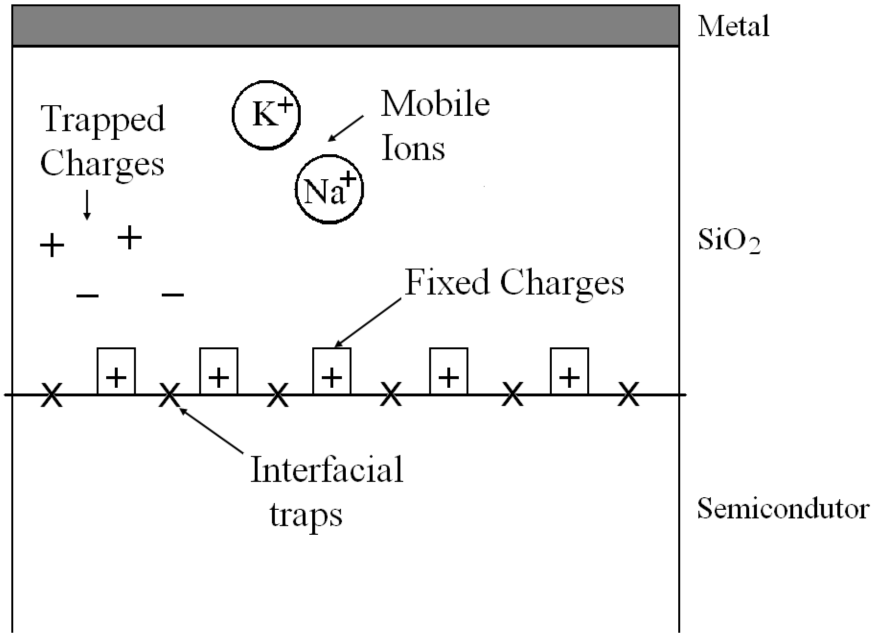


Figure 2.2.7 Nature and location of different oxide charges in thermally grown SiO_2. (Adapted from Deal, B.E., 1980)[39]

Experience over decades of research worldwide[38] has shown that major types of oxide charge inside a thermally grown SiO_2 layer include Fixed Charges, Q_F; Mobile Ion Charges, Q_M; and Interfacial Trap Charges, Q_{IT}[39]. Their locations in the oxide are shown in Figure 2.2.7. The total shift of the applied gate voltage due to these charges and including the ϕ_{MS} term mentioned in the previous section can be expressed as:[31]

$$\Delta V_G = (V_{G(real)} - V_{G(ideal)})|_{same\,\phi_S} = \phi_{MS} - \frac{Q_F}{C_O} - \frac{Q_M \gamma_M}{C_O} - \frac{Q_{IT}(\phi_S)}{C_O} \ldots\ldots\ldots\ldots\ldots \text{(Eq 2.2.11)}$$

The first charge term Q_F corresponds to the fixed charges inside the oxide. This term stands for those positive charges inside the oxide near the O-S interface usually introduced during fabrication process. These charges do not move under bias-temperature stressing (BTS). These charges are independent of oxide thickness, gate bias, temperature variance and all the other conditions that may affect other oxide charges. The shift of ΔV_G due to this constant charge distribution therefore is fixed and stable. However, the ΔV_G shift that they produce is still undesirable, even though the total concentration of these charges is relatively reproducible for a given certain fabrication process. This situation will be discussed further when passivation techniques are discussed for the removal of Q_{IT} (negative interface trapped charges).

Q_M represents mobile ionic charge. These charges can be introduced either during the oxidation process or afterwards during subsequent device processing, and mobile ions move rapidly under bias-temperature stress. The detail nature of these charges and γ_M will be discussed in later sections, but these mobile charges and the unstable shift of ΔV_G they introduce is a severe problem. Much effort throughout the semiconductor industry has been directed towards eliminating these ions.

Q_{IT} is the charge trapped in interface states, and this charge which will be discussed in detail in the following section. Note that the Q_{IT} term is a function of the surface potential ϕ_S, meaning that the value of Q_{IT} varies with applied gate voltage V_G. For an n-type MOS capacitor measured at accumulation, the Q_{IT} term is usually negative, correspond to an in positive ΔV_G shift.

Flat-Band Voltage (V_{FB}) expression

Because of the non-ideal properties of a real MOS capacitor, there will be a "build-in" potential across the device in equilibrium, and the energy bands will be bent at the O-S interface. In order to make this real device reach flat-band the condition, an initial gate bias voltage is needed. This voltage is known as flat-band voltage, V_{FB}. As mentioned in section 2.2.2, V_{FB} for the ideal case is 0V. Now taking into account for the non-idealities mentioned in this section, Eq 2.2.11 becomes:

$$V_{FB(real)} = (V_{FB(ideal)} + \Delta V_G)|_{same\,\phi_S} = \phi_{MS} - \frac{Q_F}{C_O} - \frac{Q_M \gamma_M}{C_O} - \frac{Q_{IT}(\phi_S)}{C_O} \text{ .... (Eq 2.2.12a)}$$

The V_{FB} measured for a real n-type 4H-SiC MOS capacitor experimentally for example, is usually positive, indicating the sum of all these kinds oxide charges is negative. For a p-type capacitor, the measured V_{FB} is typically negative, indicating a positive net charge.

According to Eq 2.2.12a, V_{FB} is determined by all the non-idealities of the MOS capacitor. This makes V_{FB} a very important parameter for a real MOS capacitor because it is a very good indication of all the non-ideal properties of that device. By studying and analyzing V_{FB} and its behavior under different conditions (i.e. gate bias, temperature, etc.), valuable information can be obtained about device quality and the nature of the O-S interface and the oxide layer.

Note that Eq 2.2.12 can also be written as:

$$V_{FB(real)} = \phi_{MS} - \frac{1}{C_O}[Q_F + Q_M\gamma_M + Q_{IT}(\phi_S)] = \phi_{MS} - \frac{1}{C_O}[Q_{eff}] \ldots\ldots\ldots\ldots.. \text{(Eq 2.2.12b)}$$

Here $Q_{eff} = [Q_F + Q_M\gamma_M + Q_{IT}(\phi_S)] \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots..$ (Eq 2.2.12c)

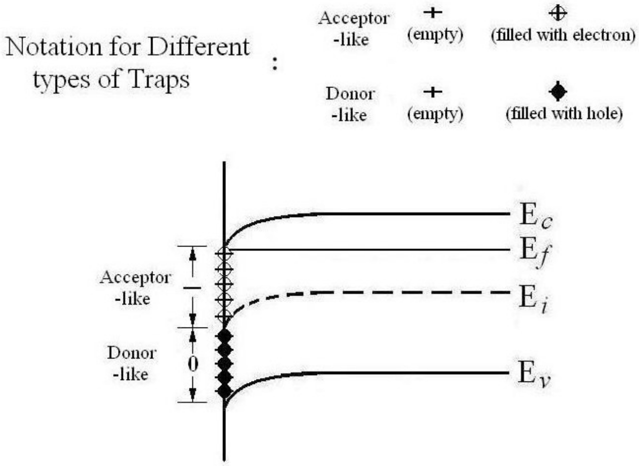
An important fact about V_{FB} measurement in real devices is that what can be extract from the measured values of V_{FB} and C_O is the Q_{eff} term in Eq 2.2.12b. Q_{eff} represents the sum of all the charges in the oxide layer. It will be much more helpful if one could obtain the value for each term separately; however, the complexities of the measurement process prevent this. For example, there is no efficient way of separately measuring the fixed oxide charge Q_F because for Q_{IT} with the wide band gap of SiC, it is not possible to sweep (i.e., separate) the deep traps located around mid-gap. However, there are some other methods such as BTS that can be applied to have a rough estimate of some individual types of oxide charge. For Q_F and deep Q_{IT} however, the only way to study them is by looking into the combined total charge Q_{eff} term.

2.2.4.3 Interface Traps and D_{IT}

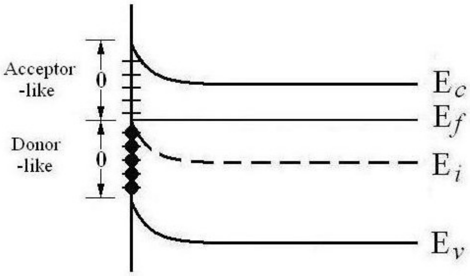
Among all the non-idealities for a real MOS capacitor, oxide-semiconductor interface traps is considered one of the most important and a major obstacle that limits the performance of MOS transistors. These interfacial traps are localized energy levels that can occur throughout the forbidden band gap. These interface states form potential wells located near or at the O-S interface, and these wells trap either electron of holes to produce a localized, charged site. By creating a localized coulomb field, these sites contribute to the scattering of carriers in the inversion channel of a MOSFET, which reduces mobility drastically. Moreover, these charges will create a field that bends the bands and varies the flat-band voltage, V_{FB}. Traps near the band edges can rapidly capture and release carriers under different gate bias, thus affecting the charge and field distributions and making the device characteristic complex and sometimes unpredictable. Removing, or at least minimizing the concentration of interface traps is very important, and much effort and study by the MOS R&D community has been directed towards this end.

The physical origin of these interface traps always remains mysterious and attracts great interest of researcher and scientist. In Si-based devices, it has been shown that these traps are mainly due to the Si dangling bonds that remain at the Si/SiO_2 interface[31, 38], when the silicon lattice is terminated abruptly after the oxidation. Oxidation does not tie up all the Si bonds left at the surface, and these untied chemical bonds, i.e., "dangling bonds", are the source of the interface traps. The Si industry nowadays already handles this problem by using different oxidation condition and annealing technique. The most popular method is either a wet-oxidation or post-oxidation H_2 anneal. Atomic hydrogen ties up most of the Si dangling bonds at the interface and reduces the interface trap to an acceptable level[40] (from ~10^{12}cm^{-2}eV^{-1} after oxidation to ~10^{10}cm^{-2}eV^{-1} following passsivation).

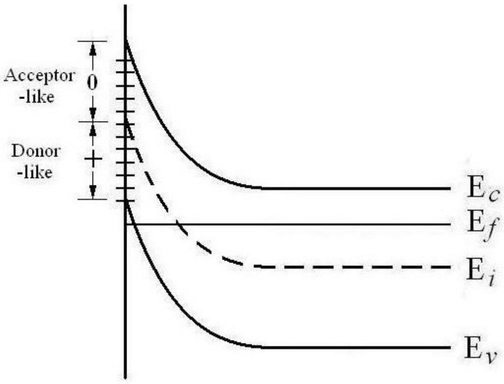
In the case of SiC-based MOS devices however, interfacial traps are a much more serious problem. Compared with Si, where the density of interface traps ($D_{IT} = Q_{IT}/q$)) is ~10^{10}cm^{-2}eV^{-1}, the D_{IT} for SiO_2/4H-SiC is widely reported to be above to 10^{13}cm^{-2}eV^{-1} close to the conduction band edge E_C. This much higher trap density does not mainly originate from Si dangling bonds[41]. It is widely accepted that instead of an abrupt interface (as is the case for SiO_2/Si) there is a several nm thick transition layer at SiO_2/SiC interface.[42,43,44] Our understanding of this layer to date is limited at best. Unlike Si, the oxidation of SiC releases carbon which contributes to the formation of the transition layer to make the SiO_2/SiC interface more complicated, troublesome and interesting. The physical origins of these traps still remains mostly unknown and still a subject for debate, though a number of theoretical works have sought to provide explanations. It is been frequently reported that the excess carbon cluster is one of the factors that contribute to interfacial traps.[38,41,103,104] Possible reasons could also be unknown vacancy sites, other carbon related defects, and intrinsic defects in the oxide due to oxygen vacancies.[38,103] Although the physical picture of the transition layer and the origins of the interface traps remains unclear, a fact that we are certain of is that, if we apply common oxidation and annealing methods to SiC (e.g., wet oxidation, H_2 anneal, nitridation anneal, etc.), devices do show a reduced number of interface traps. However, even with the best combination of post-oxidation annealing techniques, results are still far from satisfactory compared with SiO_2/Si. The D_{IT} measured for SiC is two orders of magnitude higher, and the channel mobility for SiC MOSFETs remains just barely acceptable for commercial device fabrication. Further study and improvement is still required – both experimentally and theoretically.



(a)
Accumulation



(b)
Depletion



(c)
Inversion

Figure 2.2.8 Band diagram of the filling of different types of interface traps under (a) accumulation, (b) depletion, (c) inversion for an n-type MOS capacitor.

Now let us use model of these interfacial traps on the band diagram to discuss their behavior as a function of gate bias and how they affect the measured flat-band voltage. As mentioned previously, the interface states introduce energy levels throughout the whole band gap, as shown in Figure 2.2.8. For SiC, it is proposed by various authors that the interface states near the conduction band appear to be acceptor-like traps (electron traps), and those close to the valence band appear to be donor-like (hole traps).[31,109] Acceptor-like traps behave like acceptors, meaning that they are neutral when empty and negatively charged when filled with an electron. Similarly, donor-like traps are positively charged when empty and neutral when filled with an electron. Consider an n-type MOS capacitor with the Fermi level close to E_C. To first order, all the energy levels above E_F will be empty, and all the energy levels below E_F will be filled. The energy levels of the interface traps is fixed relative to band edges E_C and E_V, meaning they will shift on the band diagram with the bending of the bands due to different gate bias situations. It is obvious from the Figure 2.2.8 that at accumulation, almost all the interface states are below Fermi level. They are all filled, with all the acceptor-like traps charged negatively and the donor-like traps neutral. Since D_{IT} is higher above mid-gap than below, the total net charge due to interface states, Q_{IT}, will be negative. When this device is biased into inversion, the acceptor-like traps moves above the Fermi level and release their electrons, and Q_{IT} will decrease and eventually become positive. Lastly, when the device is further biased into inversion (actually deep depletion), E_F will be close to E_V. All traps above E_F

will empty and the donor-like traps will become positively charged. Q_{IT} becomes even more positive in this situation. For these reasons, Q_{IT} is usually expressed as a function of surface potential ϕ_s, noted as $Q_{IT}(\phi_s)$. As with other charges, the effect of the total interfacial trapped charge $Q_{IT}(\phi_s)$ on the observed gate voltage shift is then:[31]

$$\Delta V_G \begin{pmatrix} \text{interrfacial} \\ \text{traps} \end{pmatrix} = -\frac{Q_{IT}(\Phi_S)}{C_O} \text{ ....…........... (Eq 2.2.12)}$$

Note that here Q_{IT} varies with ϕ_s, which makes the shift of ΔV_G unstable and hard to predict. This is a very serious problem for SiC MOS devices. According to Nicollian and Brews,[109] For Si-based device, as mentioned earlier, the density of interface traps can be reduce to an acceptable level $\sim 10^{10} \mathrm{cm}^{-2}\mathrm{eV}^{-1}$, and the variance of $Q_{IT}(\phi_s)$ is small enough (<0.1V) that the resulting shift ΔV_G is also acceptable. However, in case of SiC, D_{IT} is still around two orders of magnitude larger, which translates into a much larger $Q_{IT}(\phi_s)$ (~10V). The ΔV_G is no longer negligible and poses a serious obstacle. This is the reason it is important to minimize and remove these interface traps for SiC.

It is possible to sweep the interface states at different energy levels by applying different gate biases. The trap density (D_{IT}, with unit of $\#/\mathrm{cm}^2 \cdot \mathrm{eV}$), is defined as the real trap concentration per unit energy in the band-gap. According to Section 3.7, and APPENDIX C,[37] D_{IT} is calculated from interface trap capacitance C_{IT} which is calculated from the capacitance change that occurs when traps empty during the sweep from accumulation to depletion[45]:

$$C_{IT} = \left(\frac{1}{C_Q} - \frac{1}{C_{OX}}\right)^{-1} - \left(\frac{1}{C_H} - \frac{1}{C_{OX}}\right)^{-1} \quad \text{(Eq 2.2.14)}$$

Then, $$D_{IT} = \frac{(1\times 10^{-12})C_{IT}}{A} \quad \text{(Eq 2.2.15)}$$

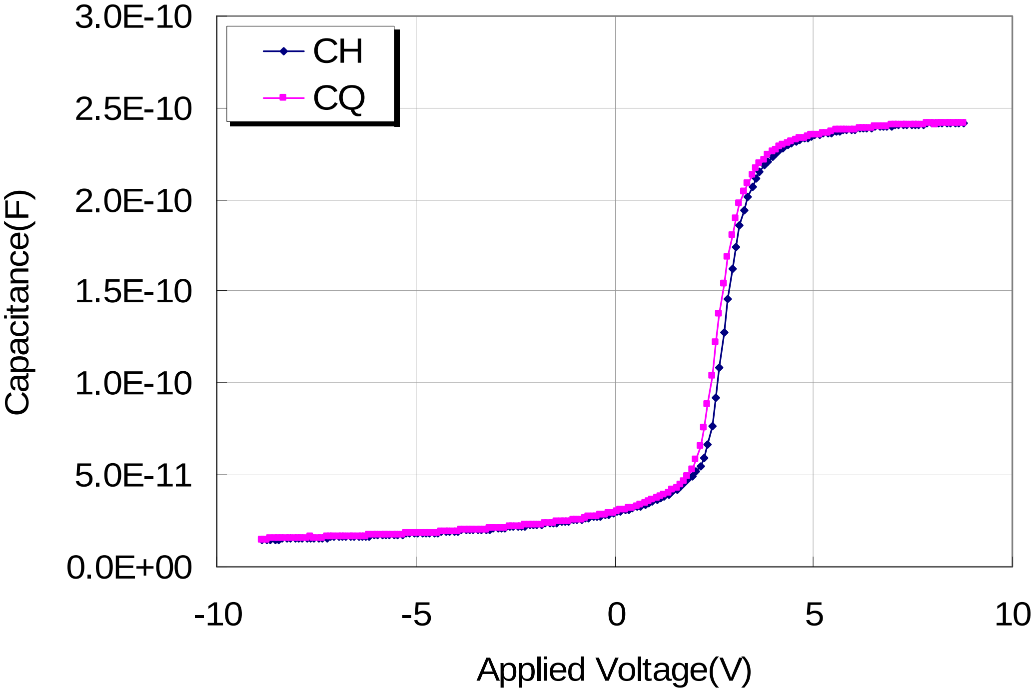


Figure 2.2.9 Room-temperature (23°C) C-V measurement on an n-4H-SiC MOS capacitor with dry O_2 oxidation followed by standard NO anneal.

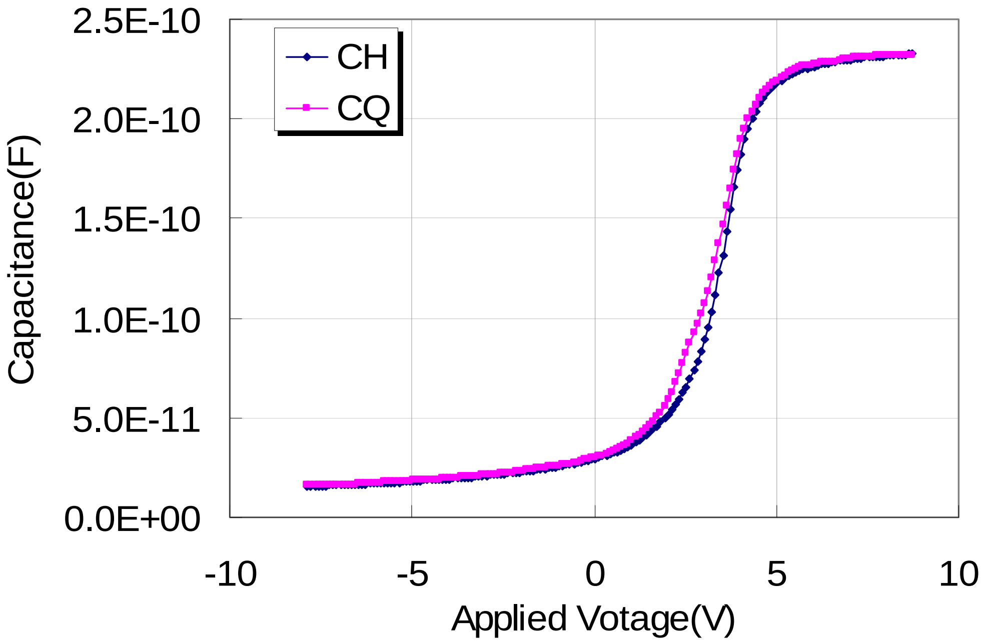


Figure 2.2.10 High-temperature (300°C) C-V measurement on an n-4H-SiC MOS capacitor with dry O_2 oxidation followed by standard NO passivation anneal.

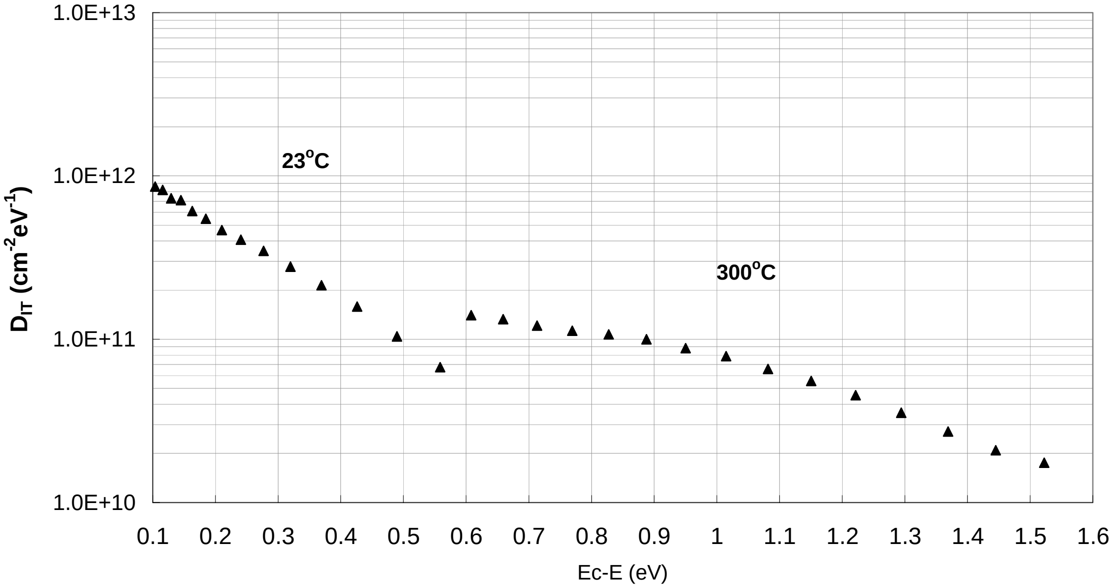


Figure 2.2.11 The D_{IT} extracted from room-temperature (23°C) and high-temperature (300°C) C-V measurements on an n-4H-SiC MOS capacitor with dry O_2 oxidation followed by standard NO anneal.

Note that this calculation is only relatively accurate, because the equations become inaccurate when D_{IT} is of order 10^{12}~10^{13} $cm^2 \cdot eV$.[45,46] For SiO_2/Si interface traps, it is feasible to sweep the whole band-gap using different gate bias at room temperature. However, because of SiC's larger band-gap, traps near mid-gap do not respond at room temperature. D_{IT} near E_C and E_V can be measured using n-type and p-type MOS capacitors. The measurements are usually made from accumulation to depletion, sweeping traps close to both band-edges to deeper into the band. Taking an n-type capacitor for example, D_{IT} of the upper half of the band-gap is plotted using C-V measurement at both room-temperature (23°C) and high-temperature (300°C),[47] as shown in Figure 2.2.11. Shallow traps close to E_C can fill and emit easily for the quasi-static measurement but not for the high frequency at room temperature,[48] causing the gap between C_Q (quasi-static or low frequency capacitance) and C_H (high frequency capacitance). Deeper traps more than 0.6eV below E_C usually have larger emission times and do not respond (i.e., fill and empty) to either the low or high frequency measurement at room temperature.[47, 49] Figure 2.2.9 is an example of the room temperature C-V result. On the other hand, under higher temperature (300°C), the trapped electrons/holes have more energy to overcome the barrier to emission, enabling those deep traps to empty during measurement. However, high temperature cause the shallow traps to respond to the high frequency measurement as well, and this makes the quasi-static curve almost overlap the high-frequency curve near the accumulation, as demonstrated in Figure 2.2.10. Because of this, 1MHz is used for the high frequency measurement to make it more accurate. But still, high temperature is only accurate for measuring the deep traps.[50] D_{IT} at 0.1eV~0.6eV below E_C are extracted from the room-temperature C-V curves, while D_{IT} at 0.6 eV~1.6eV below E_C are extracted from the high temperature C-V curves. Additionally, the measurements are less accurate in strong accumulation and deep depletion where the differences between C_Q and C_H are smaller. Noise in the system can make the results unreliable in these cases. More accurate values can be obtained using other measurement techniques. For example, traps very near E_C can be measured at low-temperature (~80K), which is practically very difficult and expensive; traps around 0.6eV can be measured at 100^oC or 150^oC; the traps near mid-gap can be measured at higher temperature. Nevertheless, accurate trap densities very close to E_C and near mid-gap remain difficult to determine.

Also worth mentioning for n-type capacitors, is that only traps near E_C are swept during a room temperature measurement, and according to Figure 2.2.8 for at accumulating and shallow depletion, the net charge in these states will be negative, resulting in a positive V_{FB} shift, according to Eq 2.2.12. A similar situation applies for p-type capacitors with charge polarities simply reversed, and V_{FB} shifting more negative relative to ideal value. This can result in an inaccurate estimation of the MOSFET threshold voltage as discussed in section 2.3.3.

2.2.4.4 Mobile Ion and Bias Temperature Stressing (BTS)

Among all the oxide charge problems, the mobile ion problem is the most troublesome and unpredictable. The reason is that these ions shift inside the oxide easily under various conditions of gate bias and temperature. Depending on the total concentration of these ions inside the oxide, the gate voltage shift ΔV_G can be anywhere from few volts to tens of volts, which results in unacceptable performance instabilities. This effect is particularly troublesome for the threshold voltage of MOSFET, possibly changing the devices operating characteristics from “normally-off” to “normally-on” in a device that is vulnerable to effects of heat and field.

The physical source of these mobile ions is believed to be alkali ions, such as Na^+ and K^+ ions. These ions along with some other metal ions can easily diffuse through SiO_2 at elevated temperatures, and can even sometimes change the structure of the SiO_2 layer. For many years in the semiconductor industry, great care has been taken to avoid contaminations from these ions by using clean rooms, avoiding direct wafer handling, using high purity quartz and metals for all processing and the adoption of fabrication procedures developed specifically for the removal of these ions.

Mobile ions are mostly positively charged metal ions.[38] Thus the total charge per unit area under the gate, Q_M, is usually a positive number. Take $\rho_{ion}(x)$ to be the number of mobile ions per unit volume as a function of distance measured moving into the oxide from the metal-oxide interface. Then Q_M is simply:

$$Q_M \equiv \int_0^{x_0} \rho_{ion}(x)dx \text{ ……………………………………..…….. (Eq 2.2.16a)}$$

According to[31], the shift in the applied voltage ΔV_G caused by these mobile ions is:

$$\Delta V_G \begin{pmatrix} \text{mobile} \\ \text{ions} \end{pmatrix} = -\frac{1}{K_O \varepsilon_O} \int_0^{x_0} x\rho_{ion}(x)dx \text{ ………………………..…. (Eq 2.2.16b)}$$

In order to express ΔV_G as a function of total mobile ion charge Q_M, we define a unitless parameter γ_M, defined by Eq 2.2.17a, which weights the spatial distribution of the ions inside the oxide:

$$\gamma_M = \int_0^{x_0} \frac{x\rho_{ion}(x)dx}{x_0 \int_0^{x_0} \rho_{ion}(x)dx} \text{ ……………………………….………….. (Eq 2.2.17a)}$$

At the M-O and O-S interfaces, γ_M is 0 and 1, respectively. Eq 2.2.16b can be re-written as:

$$\text{Then, } \Delta V_G \begin{pmatrix} \text{mobile} \\ \text{ions} \end{pmatrix} = -\frac{Q_M \gamma_M}{C_O} \text{ ………………………….……… (Eq 2.2.17b)}$$

From Eq 2.2.17b, ΔV_G is quite sensitive to the value of γ_M – i.e., to the position of the mobile ions in the oxide. As mentioned earlier, the ions can move easily under the influence of temperature and bias, and this characteristic makes them unwelcome infabricated devices. If all the mobile ions are present at the O-S interface, $\gamma_M = 1$, likewise, if the mobile ions are all at M-O interface, $\gamma_M = 0$ (Figure 2.2.12). Otherwise, γ_M is always a number between 0 and 1, depending on the actual position of ions inside the oxide layer.

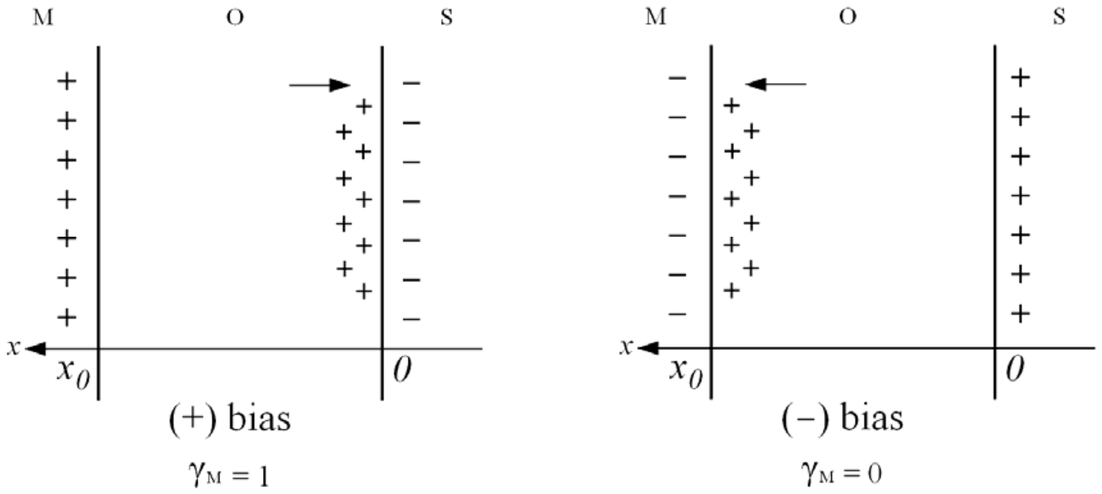


Figure 2.2.12 Two hypothetical mobile ion distribution inside the oxide layer under (+) and (-) bias-temperature stressing (BTS).

It is clear that by forcing the ions into the $\gamma_M = 0$ and 1 situations, an estimate of the total mobile ion areal density Q_M can be made using observed shifts in the measured C-V curves. The bias-temperature stress (BTS) measurement technique is based on the observation of these shifts. The BTS procedures used in this work are the following: a room temperature simultaneous high-low C-V measurement is made on the sample as fabricated to obtain all the initial parameters and an estimate of the voltages needed for fields to be applied. Then sample is heated to 250°C and a positive field of 1.5~2 MV/cm is applied for 5~10 min. The sample is cooled to room temperature under the same bias, after which a second C-V measurement is made. A shift of the flat band voltage to a lower value (i.e., a left shift) is usually seen if the sample is contaminated with mobile ions. Following this room temperature measurement, a negative bias is applied at 250°C for 5-10min. A final C-V curve is generated after the sample is cooled to room temperature under negative bias. The positive bias – negative bias shift of measured flat-band voltage ΔV_{FB} can be calculated from the BTS results, assuming all the ions are pushed into the two situations described in Figure 2.2.12. The total mobile ion charge Q_M can be calculated using Eq 2.2.17b

$$\text{Since}\quad \Delta V_{FB}\begin{pmatrix}\text{mobile}\\ \text{ions}\end{pmatrix} = |V_{FB}(\gamma_M = 0) - V_{FB}(\gamma_M = 1)| = \frac{Q_M}{C_O} \quad \text{.................... (Eq 2.2.18a)}$$

$$\text{Then}\quad Q_M = C_O \times \Delta V_{FB}\begin{pmatrix}\text{mobile}\\ \text{ions}\end{pmatrix} = C_O \times |V_{FB}(-\text{bias}) - V_{FB}(+\text{bias})| \quad \text{..........(Eq 2.2.18b)}$$

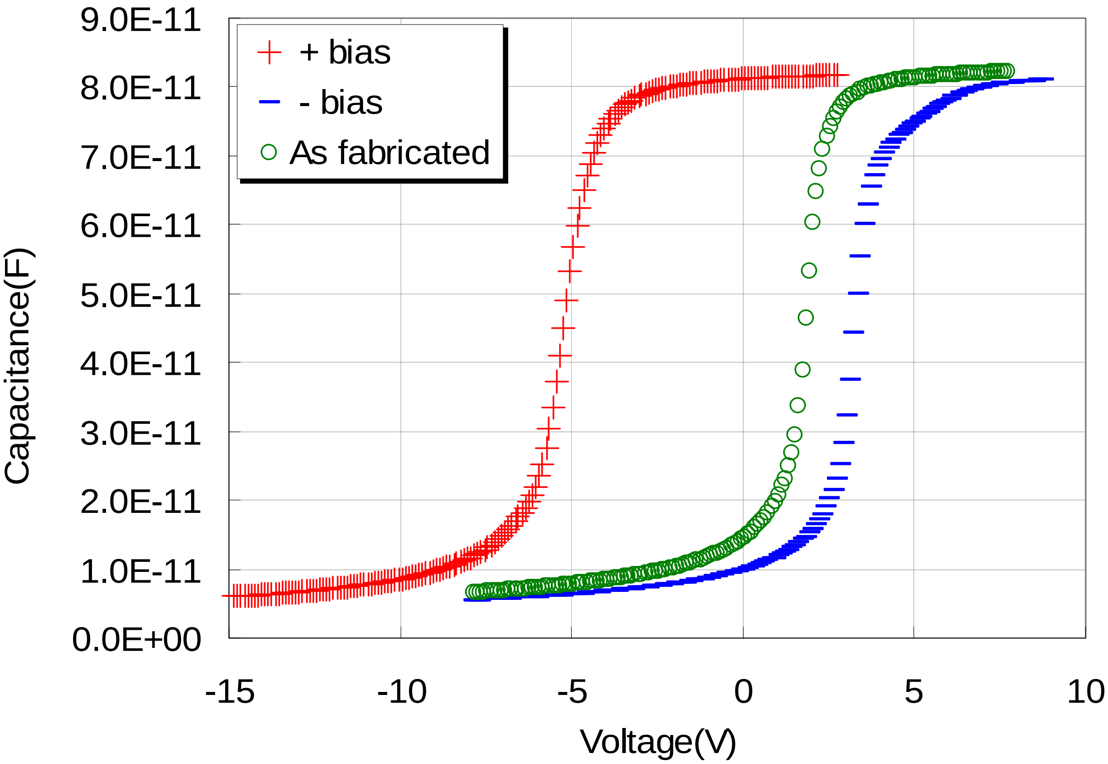


Figure 2.2.13 BTS result of an n-type 4H-SiC MOS capacitor with oxide grown by alumina enhance oxidation process.

The mobile ion concentration of the MOS capacitor shown in Figure 2.2.13 is about $6\times10^{12}/cm^2$. In some cases, for example alumina enhanced oxides[2] (described in Chapter 3), the concentration can be higher than$10^{13}/cm^2$, resulting in a V_{FB} shift of tens of volts. This is the major factor that makes this kind of oxide not applicable for device fabrication. The typical acceptable mobile ion concentration of an "uncontaminated" oxide layer is less than $10^{11}/cm^2$. However, due to the abundance of the sources of these ions gate metals, sputter system and sometimes even the oxidation furnace, it is very possible that the fabricated MOS devices will have mobile ion contamination. Checking the devices by BTS measurement is an important way to determine the quality of device performance.

BTS method also has a limitation, especially on SiC MOS devices. This is due to the effect known as electron/hole injection. Consider an n-type 4H- MOS capacitor, for example. Because of its wide band gap, the electron affinity χ of 4H-SiC is relatively small compared with that of Si. In other words, the energy barrier between the oxide layer and the SiC, which is mainly the difference in the electron affinities of the oxide and the SiC, is much smaller compared with that between SiO_2 and Si. As a result, the probability for the electron to cross the barrier and be injected from the SiC into the oxide is much larger in SiC MOS devices under positive gate bias. Putting negatively charged electrons into the oxide shifts V_{FB} in the positive direction.[51,52] Similarly, on the p-type SiC, hole-injection can be easily observed under negative bias. Therefore, during the BTS measurement, the electron or hole injection will always result in a small shift of V_{FB} in direction opposite the shift produced by the mobile ions. For a device with low concentration of mobile ions (less than ~ $1\times10^{11}/cm^2$) this effect will become dominate, and the true shift of V_{FB} due to the mobile ion charges will be shielded by it. So for SiC based devices, the BTS method is only safe for accurately measuring mobile ion concentrations of heavily contaminated samples. However, the method is very useful for checking whether the sample might have mobile ions.

2.3 MOSFET

2.3.1 General Introduction

"MOSFET" is short for Metal-Oxide-Semiconductor Field-Effect Transistor. The MOSFET is one of the most fundamental and important devices for modern circuit designers. There are literally thousands of MOSFET-based devices for almost any conceivable application. Improvements in MOSFET performance directly link to the improvements in the operating efficiency of the circuits of which the devices are a part.

Silicon carbide's wide band-gap and other physical and chemical properties make it a promising candidate for MOSFETs that can tolerate high power and high temperature. However, compared to Si-based devices, the performance of SiC MOSFETs is far from satisfactory. As matter of fact, SiC MOSFETs are not currently available for commercial use. One of the main obstacles is channel mobility, which is mainly limited by the poor quality of the oxide/semiconductor interface. Therefore, in order to improve the performance of SiC MOSFETs and promote commercialization, it is imperative that we understand how oxide non-idealities affect the device operating characteristics.

2.3.2 Basic Structure of MOSFET

There are dozens of different MOSFET structure available in modern VLSI design, each designed mostly for applications in specific areas or for certain functions. Since our interest is mainly focused on the oxide/semiconductor interface and its effect on the channel mobility, in our research work, we will mainly focus on the very basic structure of an n-channel, p-bulk lateral MOSFET.

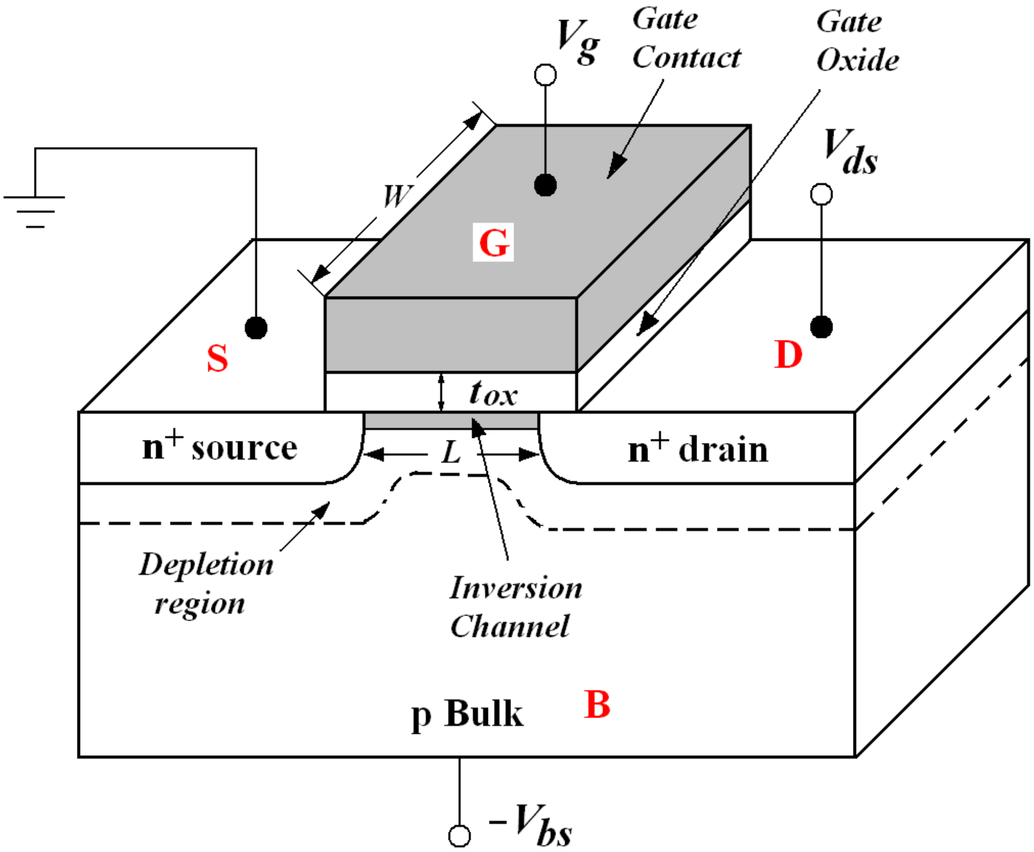


Figure 2.3.1 Cross-section diagram of an inversion mode, n-channel lateral MOSFET.

The schematic cross section diagram of this MOSFET is shown in Figure 2.3.1. The device consists of four regions which are the Gate (G), the Source (S), the Drain (D) and the Bulk or Substrate (B).[53] The gate is in the form of a thin oxide layer overlaid with a metal layer or heavily doped poly-silicon. The source and drain consist of two highly doped n^+ regions with low resistances. In our devices, the n^+ regions are formed by ion implantation using nitrogen at 700°C, due to the fact that it is almost impossible to dope SiC bulk by diffusion at reasonable temperatures. The ohimc source and drain contacts are realized by depositing Ni on the n^+ regions and annealing at ~870 ^{o}C to forming nickel silicide (Ni_2Si).[54,55,56]

The operation of MOSFET can be explained by recalling the operation of the MOS capacitor. A small voltage is applied across source and drain. Ideally, when gate bias voltage is zero, there will be no current flow due to the natural p-n junction barriers. The device is in the Off state. When a positive gate voltage is applied, the semiconductor surface under the gate area will be biased first into depletion, then eventually into inversion, as discussed previously. In the inversion state, an n-type inversion channel is formed under the gate, connecting the n+ source and drain regions so that current flows between them. And at this point, the device is On. In another words, an ideal MOSFET operates like a current switch control by the gate voltage V_G.

The fabrication process for the MOSFET is described in the Appendix B, please refer to it for further details. For device characterization and parameter extraction, two Keithley Instruments measurement units (Mod. Nos. 4200 and 4210) are connected to a high temperature probe station. One unit measures source-drain current I_{SD} for a constant source-drain voltage V_{SD}, while the other is used to supply the gate voltage V_G.

2.3.3 Threshold Voltage V_T

The threshold voltage V_T, is one of the most important parameters for a MOSFET, and there are a number of ways to define threshold voltage. The most straightforward and popular way is to extrapolate a tangent line on the I_D-V_G curve to zero drain current. The zero current intercept on the gate voltage axis is the threshold voltage V_{on}.[32] The advantage of this definition is that V_{on} is easily measured. All the threshold voltage data presented in this work were measured by this method. The method is also widely used in the literatures as a result of the convenience of extracting V_{on} from the experimental data. However, one should keep in mind that this V_{on} is different from V_T. Theoretically, V_{on} is typically (2~4)*kT/q* higher than the V_T, due to the inclusion of the inversion-layer capacitance and other mobility degradation effects.[32] In real devices, the difference is usually much less than 1 volt, and for a first-order approximation, one can treat $V_{on} \approx V_T$.

Another popular method to define threshold voltage is through the sub-threshold current, using the following Equation[32]:

$$I_{ds}(V_g) = \mu_{eff} C_{ox} \frac{W}{L}(m-1)(\frac{kT}{q})^2 \exp[q(V_g - V_t)/mkT] \ldots\ldots\ldots\ldots \text{(Eq 2.3.1a)}$$

Here *m* is the body-effect coefficient, defined by[32]:

$$m = 1 + \frac{\sqrt{\varepsilon_s qNa/4\psi_B}}{C_{ox}} \ldots\ldots\ldots\ldots \text{(Eq 2.3.1b)}$$

For a given constant current level I_0, The threshold voltage V_t^{sub} in this case, can be solved from Eq 2.3.1a by setting $I_{ds}(V_g = V_t^{sub}) = I_0(W/L)$. It is not very difficult to extract an accurate threshold voltage from experimental data using this method for long-channel MOSFET. However, the problem with this method is that an precise value of channel length hard to obtain, especially for short-channel MOSFETs, not to mention real cases where V_T is also subject to change under various conditions such as temperature, substrate bias, and imperfections and defects.

For an ideal MOSFET, the most commonly used theoretical definition can be described as follows:[32,109] The first part of the threshold voltage corresponds to the application of a depletion-inversion gate voltage that makes the surface potential equal to $2\phi_F$. As previously, under inversion, there is also a depletion region in the semiconductor. The charge in this depletion region is given by $Q_D = -qN_a X_{\text{dmax}}$ (for n-channel) at $\varphi_S(\text{inv})=2\varphi_F$, where $X_{\text{dmax}} = \sqrt{\frac{2\varepsilon_s(2\phi_F)}{qN_a}}$, putting these contributions together, the theoretical V_T of an n-channel ideal MOSFET is then:

$$V_T = 2\phi_F + \frac{K_S X_O}{K_O}\sqrt{\frac{4qN_a(\varphi_F)}{K_S\varepsilon_O}} \quad \text{……………………………………..….. (Eq 2.3.2a)}$$

Similarly, for a p-channel MOSFET,

$$V_T = 2\phi_F - \frac{K_S X_O}{K_O}\sqrt{\frac{4qN_D(-\varphi_F)}{K_S\varepsilon_O}} \quad \text{…………………………………..…….. (Eq 2.3.2b)}$$

Now the effect of non-ideal oxide characteristics discussed in section 2.2.4 shifts V_T by an amount ΔV_T,

$$V_{T(real)} = (V_{\mathrm{T}(ideal)} + \Delta V_T) = V_{\mathrm{T}(ideal)} + \phi_{MS} - \frac{Q_F}{C_O} - \frac{Q_M\gamma_M}{C_O} - \frac{Q_{IT}(2\phi_F)}{C_O} \quad \text{……… (Eq 2.3.3)}$$

Recall that the flat band voltage of a real MOS capacitor from Eq 2.2.12a is that:

$$V_{FB(real)} = (V_{FB(ideal)} + \Delta V_G)\big|_{\phi_S=0} = \phi_{MS} - \frac{Q_F}{C_O} - \frac{Q_M\gamma_M}{C_O} - \frac{Q_{IT}(0)}{C_O} \quad \text{…………..… (Eq 2.2.12a)}$$

Under the flat band conditions, $\phi_S = 0$ and $V_{FB(ideal)} = 0$. little during band bending from $\phi_S = 0$ to $\phi_S = 2\phi_F$, (including Q_{IT} which is a function of the surface potential) the V_{FB} shifts caused by interface traps when the Fermi level is close to E_C and E_V are actually reversed, as explained in section 2.2.4.3. This approximation holds for well made Si devices; however for SiC, this assumption is questionable, due to its large trap density. Even for passivated n-type and p-type 4H-SiC MOS capacitors, the Q_{IT} alone during the band bending can cause a several Volts V_{FB} change,[109] and the V_T shift is always larger than the V_{FB} shift due to interface imperfections such as Q_{IT}.[57] The complete expression for the threshold voltage V_T for an n-channel MOSFET is:

$$V_T = V_{FB} + 2\phi_F + \frac{K_S X_O}{K_O}\sqrt{\frac{4qN_a(\varphi_F)}{K_S\varepsilon_O}} \quad \text{………………………..……... (Eq 2.3.2a)}$$

Similarly, for a p-channel MOSFET,

$$V_T = V_{FB} + 2\phi_F - \frac{K_S X_O}{K_O}\sqrt{\frac{4qN_D(-\varphi_F)}{K_S\varepsilon_O}} \quad \text{……………………..…….. (Eq 2.3.2b)}$$

As a key design parameter in MOSFET devices, threshold voltage is always carefully considered and tailored during the design of the MOSFET as well as during the fabrication process.

2.3.4 Channel Mobility

The most important parameter currently limiting the performance of SiC MOSFETs is no doubt the channel mobility. In the semiconductor industry, Si MOSFETs can achieve a maximum channel mobility at about half of silicon's bulk mobility. For SiC MOSFETs on the other hand, the highest reported channel mobility is still around 40~50 $cm^2/V{\cdot}s$[58] (higher peak channel mobility is reported in reference [59] using alumina enhanced oxidation; however, this method is not applicable for commercial devices due to problems with mobile ion contamination). Compared with its bulk mobility, which is above 800 $cm^2/V{\cdot}s$ for 4H-SiC (Table 1.2.2), channel mobility is still far from satisfactory. It is widely believe that one of the major reasons for this low mobility is the poor oxide/SiC interface (high interface traps, physical carbon containing transition layers). The main goal of our research is to optimize the oxidation process and to apply and improve different post-oxidation annealing methods in order to further reduce the interfacial defect concentrations boost the channel mobility.

It is possible to extract channel mobility and threshold voltage from experimentally measured data. In order to do this, a model describing the behavior of that MOSFET is necessary. Depending on the structure and function of the MOSFET, there are number of models available. For the lateral n-channel MOSFET described here, the most common models are the linear model, the quadratic model and the variable depletion layer model.

2.3.4.1 The Linear Model

All the mobility values reported in this work were extracted from the I_D-V_G curves using the linear model. The idea of this model, as suggested by its name, is to treat the MOSFET as a linear device or as a variable resistor controlled by the gate-to-source voltage V_{GS}. This model is relatively accurate when the MOSFET is biased with a small drain-to-source voltage, and it can be explained as follows. The source-drain current I_D can be simply treated as the total charge in the inversion layer divide by the travel time for the carriers flowing from source to drain. Taking Q_{inv} as the total inversion charge per unit area, t_r as the miniority carrier travel time, and W and L as the width and length of the inversion channel, the drain current this can be written as:

$$I_D = -\frac{Q_{inv}WL}{t_r} \quad \text{(Eq 2.3.3)}$$

Assuming the velocity of those carriers stays constant, t_r is then simply:

$$t_r = \frac{L}{v} \quad \text{(Eq 2.3.4)}$$

Again, assuming the field is uniform in the inversion layer,

$$v = \mu\varepsilon = \mu\frac{V_{DS}}{L} \quad \text{(Eq 2.3.5)}$$

Here, μ is the mobility of the minority carriers in the channel, and $\varepsilon = \frac{V_{DS}}{L}$ is the electric field (assumed uniform) induced by the source-drain voltage V_{DS}.

As for calculation of Q_{inv}, this device can be treated as a capacitor, with total charge Q_{inv} (per unit area) on the sides of the oxide layer. This charge equals to the product of net voltage across the oxide layer (V_{GS}-V_T) (where V_T also takes into account of non-ideality), and the capacitance of the oxide layer per unit area C_{ox}. It is written as:

$$Q_{inv} = -C_{ox}(V_{GS} - V_T) \quad \text{for } (V_{GS} > V_T) \ldots\ldots\ldots\ldots \text{(Eq 2.3.6)}$$

Now combining all the equations above (Eq 2.3.3 to Eq 2.3.6), we can write the expression for I_D as a function of V_{GS},

$$I_D = \mu C_{ox} \frac{W}{L} V_{DS}(V_{GS} - V_T), \quad \text{valid for } |V_{DS}| << (V_{GS} - V_T) \ldots\ldots\ldots\ldots \text{(Eq 2.3.7)}$$

In order to extract the channel mobility μ experimentally, the I_D-V_{GS} curve is measured and plotted. Now define transconductance $g_m = \left.\frac{d(I_D)}{d(V_{GS})}\right|_{V_{DS}}$, which can be calculated easily from the I_D-V_{GS} plot by automated software, Eq 2.3.7 becomes:

$$\mu = \frac{L}{W} \frac{1}{C_{ox} V_{DS}} g_m, \text{ valid for } |V_{DS}| << (V_{GS} - V_T) \ldots\ldots\ldots\ldots \text{(Eq 2.3.8)}$$

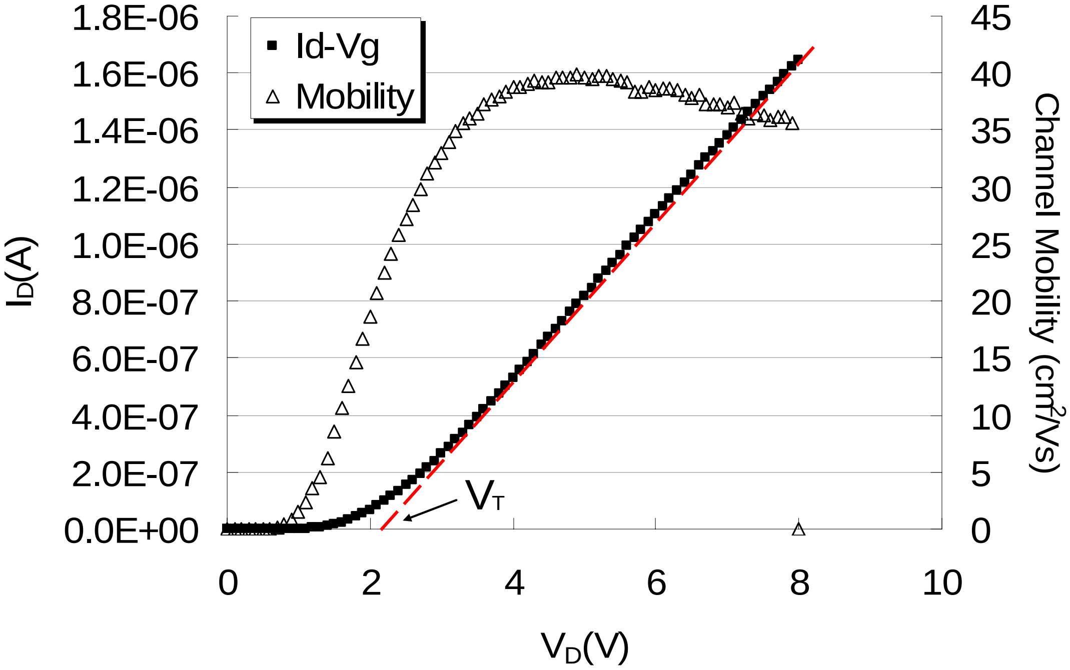


Figure 2.3.2 I_D-V_G (solid square) and channel mobility (hollow triangle) extracted from a 4H-SiC MOSFET, with gate oxide grown in dry O_2 and annealed by NO.

As an example, Figure 2.3.2 shows the I_D-V_G characteristic of a 4H-SiC MOSFET fabricated with a dry oxidation followed by a standard NO anneal. According the linear model, the channel mobility μ is extracted by Eq 2.3.8 from the I_D-V_G curve. This mobility agrees with the data reported in the literatures, which is 35~40 cm^2/V-s, as reported in reference 58.

The Linear Model is popular and widely used for its simplicity and convenience. This method is easy to understand, and all the parameters needed are accessible or can be easily measured. Extracting the mobility using the Linear Model is simple and fast, and introduces little error.

The primary problem with this model is that non-linear effects are not considered. These effects can sometimes be important. Linear Model results are less accurate when V_{DS} gets larger. However in our case, V_{DS} is usually set at 0.025V, while V_{GS} is usually few volts to tens of volts, which meets the requirements for this approximation. Furthermore, for the purpose of comparing the effects on channel mobility of different oxidation and annealing techniques, this method is more than sufficient.

2.3.4.2 *The Quadratic Model*

Compared with the Linear Model, the Quadratic Model is relatively more complicated. This model starts with the same assumptions as the linear model. However, it further assumes that the inversion charge varies along the channel according to the potential change along the channel. The model also assumes a steady continuous current flowing through the channel with the channel voltage increasing linearly 0 to V_{DS}. Now taking the *y*-axis from source to drain along the channel, for a small segment *y* to *y*+d*y*, the channel voltage at this point is V_C, the charge distribution inside this segment can be considered uniform, so Eq 2.3.7 in Linear Model is valid.

$$I_D = \mu C_{ox} \frac{W}{dy} (V_{GS} - V_T - V_C) dV_C \quad \text{……………………………………. (Eq 2.3.9)}$$

Assuming the rest of the parameters don’t vary along the channel, Eq 2.3.9 can be integrated on both sides:

$$\int_0^L I_D dy = \mu C_{ox} W \int_0^{V_{DS}} (V_{GS} - V_T - V_C) dV_C \text{ .... (Eq 2.3.10)}$$

As a result, Eq 2.3.10 becomes:

$$I_D = \mu C_{ox} \frac{W}{L} [(V_{GS} - V_T) V_{DS} - \frac{{V_{DS}}^2}{2}] \quad \text{for } |V_{DS}| < (V_{GS} - V_T) \text{ .... (Eq 2.3.11)}$$

The drain current first starts increase almost linearly. Then due to the quadratic term, the rate of increase lessens, and I_D eventually saturates at a maximum value $I_{D,Saturate}$. After that point, what happens in real device is that instead of decreasing, as predicted by Eq 2.3.11, the source-drain current stays at its maximum value even for increasing V_{DS}. A depletion layer located at the drain end of the gate accommodates the additional drain-to-source voltage. This behavior is referred to as drain current saturation. According to Eq 2.3.11, this saturation occurs when $|V_{DS}| = (V_{GS} - V_T)$, and I_D becomes:

$$I_{D,Saturate} = \mu C_{ox} \frac{W}{L} \frac{(V_{GS} - V_T)^2}{2} \quad \text{for } |V_{DS}| \geq (V_{GS} - V_T) \text{ .... (Eq 2.3.12)}$$

The quadratic model explains another important current-voltage characteristic of the MOSFET, which is the source-drain current I_D plotted as a function of source-drain voltage V_D. These plots are normally made for several different gate-source voltages. An example is shown in Figure 2.3.3:

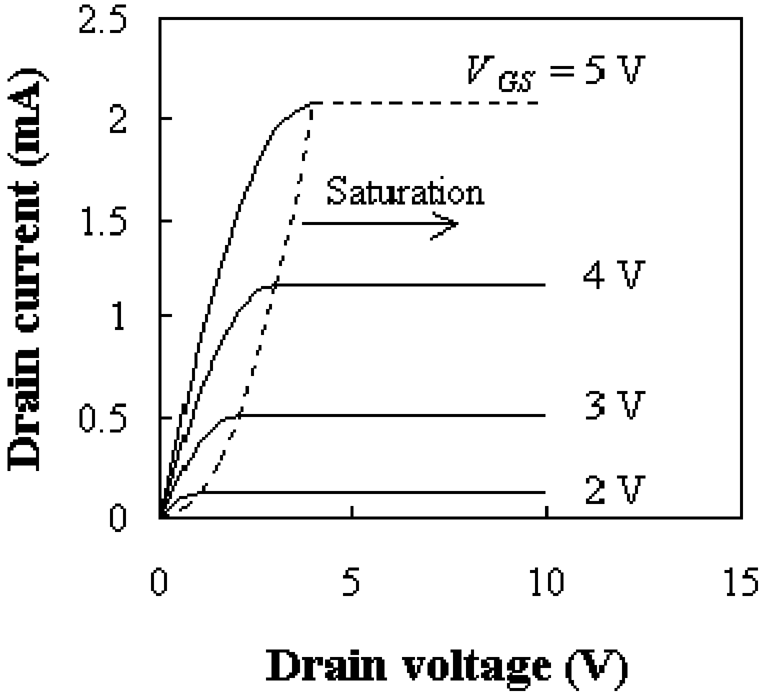


Figure 2.3.3 Typical I_D-V_D behavior of a MOSFET under different V_{GS}.

This is a typical I_D-V_D plot of a MOSFET for different values of fixed V_{GS}. The saturation occurs to the right of the dotted line which is defined by $I_D = \mu C_{ox} \frac{W}{L} V_{DS}{}^2$. At saturation, the maximum value of the current I_D follows Eq 2.3.12. This provides another way to extract channel mobility. By measuring $I_{D,saturate}$ from the I_D-V_D plot, and using additional parameters, the channel mobility can be calculated by:

$$\mu = \frac{L}{W} \frac{2}{C_{ox}(V_{GS} - V_T)^2} I_{D,Saturate} \quad \text{……………………………….…………….. (Eq 2.3.13)}$$

For a well-made device, the channel mobility calculated using the Quadratic Model should agree closely with the effective mobility extracted with the Linear Model.

We should also mention that the measured drain current in saturation does not behave strictly as predicted by the Quadratic M – that is, the drain current in saturation is not constant. The saturated current slowly increases with V_{DS} due to other reasons, such as channel length modulation, drain induced barrier lowering or two-dimensional field distributions. Considering these effects, this model can be modified for better accuracy by adding a fitting parameter λ into Eq 2.3.12:

$$I_{D,Saturate} = \mu C_{ox} \frac{W}{L} \frac{(V_{GS} - V_T)^2}{2} (1 + \lambda V_{DS}) \text{, for} |V_{DS}| \geq (V_{GS} - V_T) \ldots\ldots\ldots \text{(Eq 2.3.12)}$$

2.3.4.3 Depletion Layer Model and Other Models

The Variable Depletion Layer Model is more complicated. It further considers charge density variations in the depletion layer. Instead of assuming that V_T remains constant, it incorporates V_C (as defined for the Quadratic Model) into the equation for V_T.

$$V_T = V_{FB} + V_C + 2\phi_F + \frac{\sqrt{2\varepsilon_s q N_a (2\phi_F + V_{SB} + V_C)}}{C_{ox}} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \text{(Eq 2.3.13)}$$

Using the same idea as the Quadratic Model, substituting Eq 2.3.13 into Eq 2.3.9, and integrating on both sides over d*y* and dV_C, as a result, one can get:

$$I_D = \frac{\mu_n C_{ox} W}{L} (V_{GS} - V_{FB} - 2\phi_F - \frac{V_{DS}}{2}) V_{DS} - \frac{2}{3} \frac{\mu_n W}{L} \sqrt{2\varepsilon_s q N_a} [(2\phi_F + V_{DB})^{3/2} - (2\phi_F + V_{SB})^{3/2}]$$

$$\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \text{(Eq 2.3.14)}$$

Due to its complexity, this expression is not a preferable way to extract channel mobility experimentally. However, this method is more accurate under some circumstances and is useful sometimes in theoretical calculations. With the rapid development of technology and computer capacity, more and more complex and sophisticated models have been proposed and studied.

Compared to the simple long-channel lateral MOSFET structure we use to determine effective mobility, actual power device structures are much more complicated. For example, a field oxide and an etched isolation trench for better insulation and protection, various types of contact shapes and lay-outs for specific purposes, and variable doping profile for the p-well channel region. Full details describing the performance of these devices are beyond the scope of this work. Even for the simple MOSFETs used here, threshold voltage, contact resistance, channel mobility are not the only parameters that are important for device performance. However, for 4H-SiC MOSFET, these parameters are primarily those that limit the device performance, and it is widely believed that the poor SiO_2/SiC interface is mostly responsible for low mobility. The main goal of the experimental work described in the following chapter is to improve characteristics of the interface by using different oxidation conditions and annealing methods, and to observe their effects on threshold voltage and channel mobility.

CHAPTER 3

Equipments and Processes

3.1 Furnaces

All the oxidation and annealing processes were performed in one of the furnaces shown below. The furnaces in Figure 3.1.1, Figure 3.1.2 & Figure 3.1.3 were used for all the regular oxidation and anneal processes, and were connected with a full range of gas outlets including Ar, O_2, N_2, NO, and HCl for this research, while the furnace shown in Figure 3.1.2 is also capable of wet-reox process when linked with a vapor bubbler. The furnace in Figure 3.1.3 was specifically designated for the alumina enhanced oxidation related experiments discussed in Chapter 5, as in these experiments, various contaminations were intentionally brought into the furnace. The furnaces tubes were all made from fused GE224 low sodium quartz tubes, each about 16~18 inches long, and with a diameter of either 2.5 inches or 3.5 inches. The heating units with temperature controllers were supplied by Thermcraft. All the furnaces are capable of reaching a maximum temperature close to 1200°C with an adjustable temperature ramping rate, and maintaining a hot-zone with an acceptably uniform temperature profile extending at least 12 inches in the center of the furnace tube.

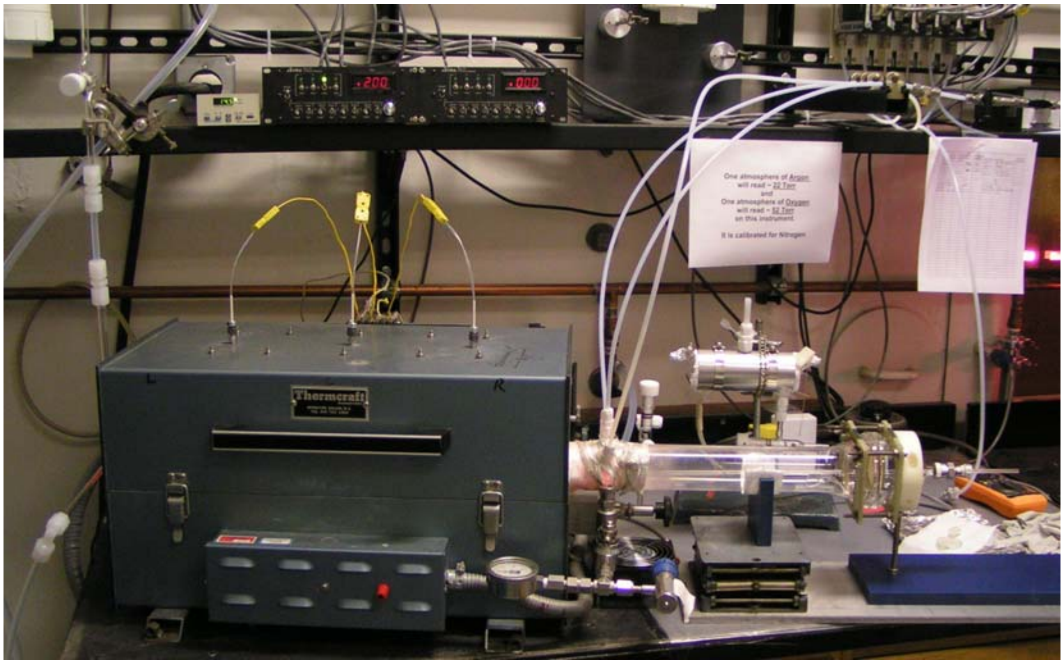


Figure 3.1.1 Furnace used for standard oxidation and few annealing process.

Figure 3.1.2 Furnace used for standard oxidation and few annealing process.

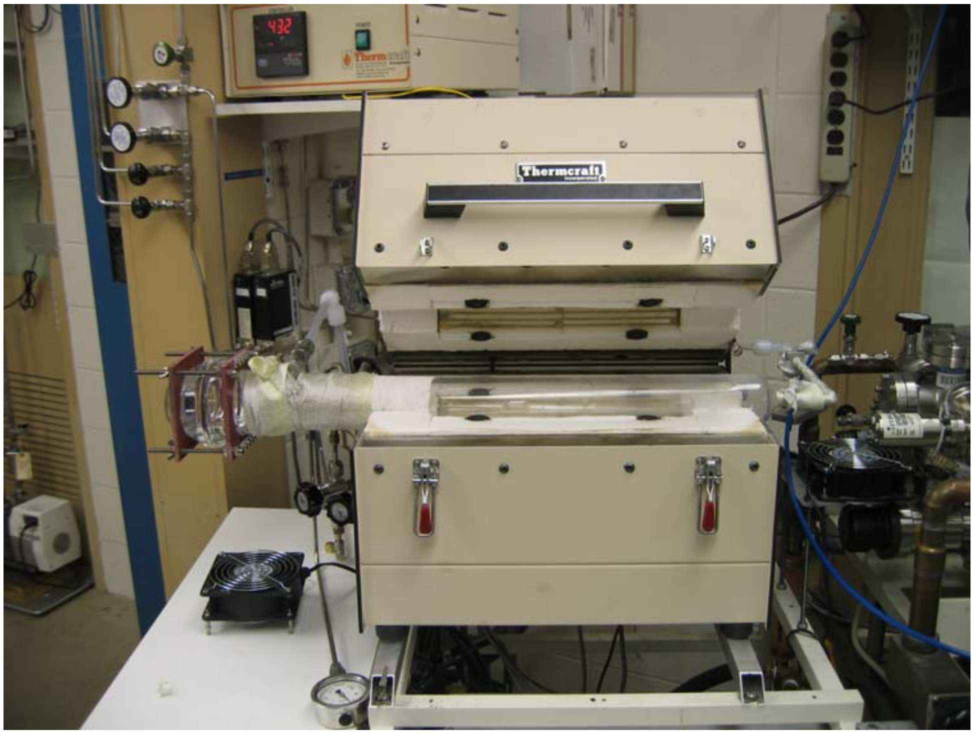


Figure 3.1.3 Furnaces designated for alumina enhanced oxidation.

3.2 Photolithography

All the sample patterns were prepared using photolithographic techniques. Due to their small size (usually 5mm×5mm), to facilitate handling most samples were adhered to a pre-cleaned 4 inch Si wafer by silver paste or a drop of photoresist. The photoresist used for the majority of the samples was Shipley AZ5214E, which is a positive resist where the exposed portion dissolves in the developer. The photoresist is spun onto the sample at 4,000 revolutions per minute for 30 seconds to create a layer approximately 1.5 μm thick, followed by a soft bake at 105^{o}C for 1 minute on an electrical hot plate in order to remove residual solvent and prepare the sample for the exposure step. A Cr coated glass mask were used for patterning on the mask aligner, after which the samples were exposed to a 160 W UV light source for 30 seconds. Without performing a hard bake, the sample was then immersed in the developing solution for around 1~2 minutes until the exposed photoresist dissolved completely. 400K developer was used here, with a volume ratio of 1 part developer to 3~4 parts de-ionized water. The sample was then rinsed in de-ionized water and dried under a nitrogen stream, ready for metal sputtering. This technique was used for most of the MOS capacitor and TLM samples patterned with a dark mask.

Some MOSFET samples required the use of a negative photoresist, where the unexposed portion dissolves in the developer. In the reversed photolithographic technique, AZ5214E was initially deposited using the same spinning conditions described above, followed by a soft bake at 105^{o}C for 1 minute to remove the residual solvents in the photoresist. After aligning on the mask aligner, generally utilizing a clear mask in order to more easily locate the alignment marks, the sample was exposed to the UV light source for 30 seconds, as with the previous samples, followed immediately by a hard bake at 110 ^{o}C which was performed in order to harden the exposed portion. The full area of the sample was then once again exposed to the UV light for about 1 minute without the mask, after which the same developer was used to remove the photoresist from the undesired areas. As a result of the second bake, in this method the portion initially exposed is dissolved much more slowly than the unexposed portions, producing the same effect as a negative photoresist. Because the exposed part also dissolves to some extent, this usually results in a thinner and less uniform photoresist layer. Moreover, this technique requires a more highly skilled operator and is extremely sensitive to temperature and developing time compared to the more widely used positive photoresist methods.

3.3 Sputtering System

Physical sputtering is widely used to deposit thin films of metal onto the substrate in fabricating semiconductors and is driven by the momentum exchange that takes place during the collision between the ions in the beam and the atoms in the target material.[60,61] When such cascades recoil and reach the target surface with the energy above the surface binding energy, an atom can be ejected. The average number of atoms ejected from the target per incident ion is called the sputter yield and depends on the ion incident angle, the energy of the ion, the masses of the ion and target atoms, and the surface binding energy of atoms in the target. The primary particles for the sputtering process can be supplied in a number of ways, for example by plasma, an ion source, an accelerator or by a radioactive material emitting alpha particles.

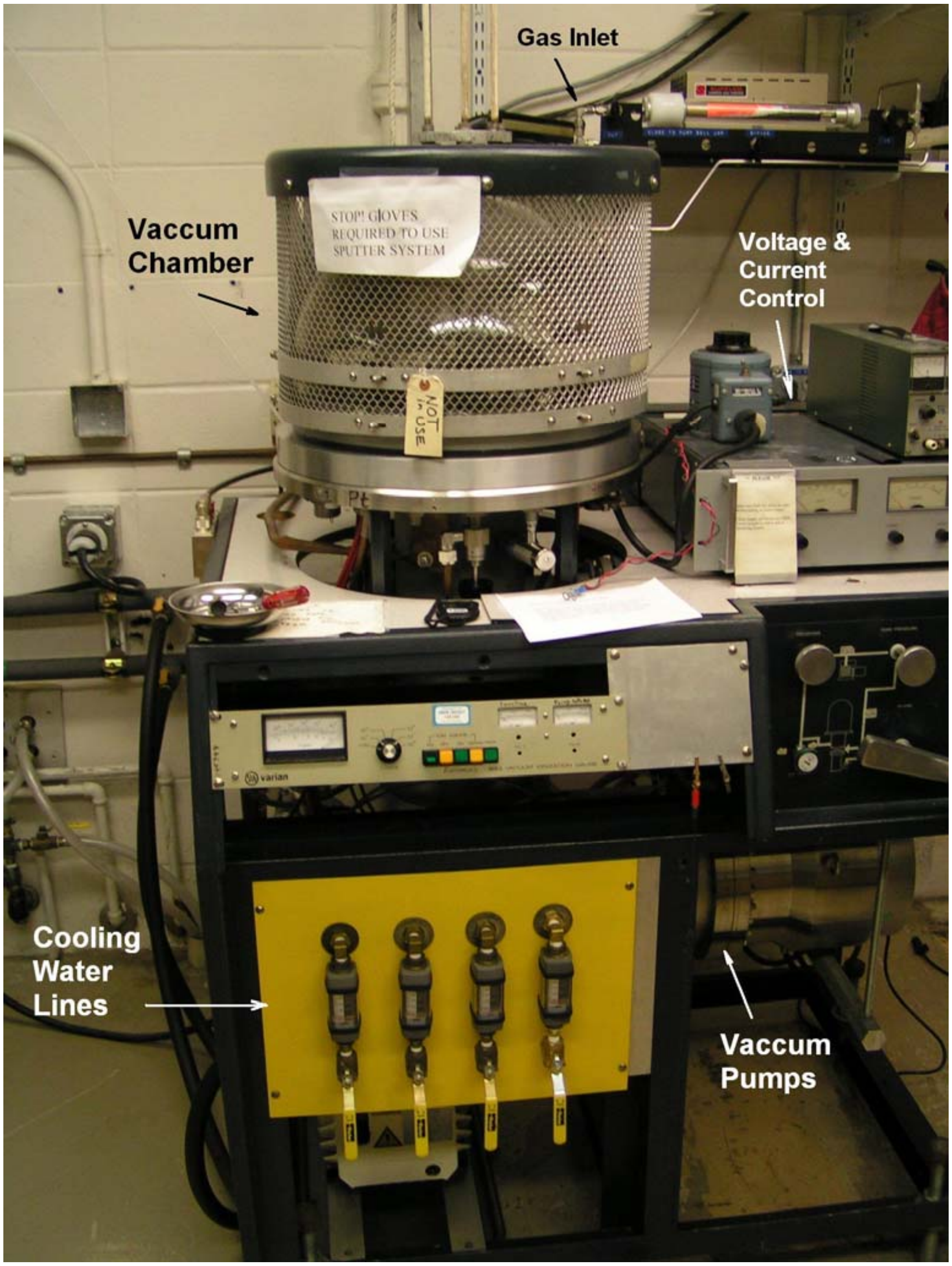


Figure 3.3.1 The sputtering system with all the components labeled.

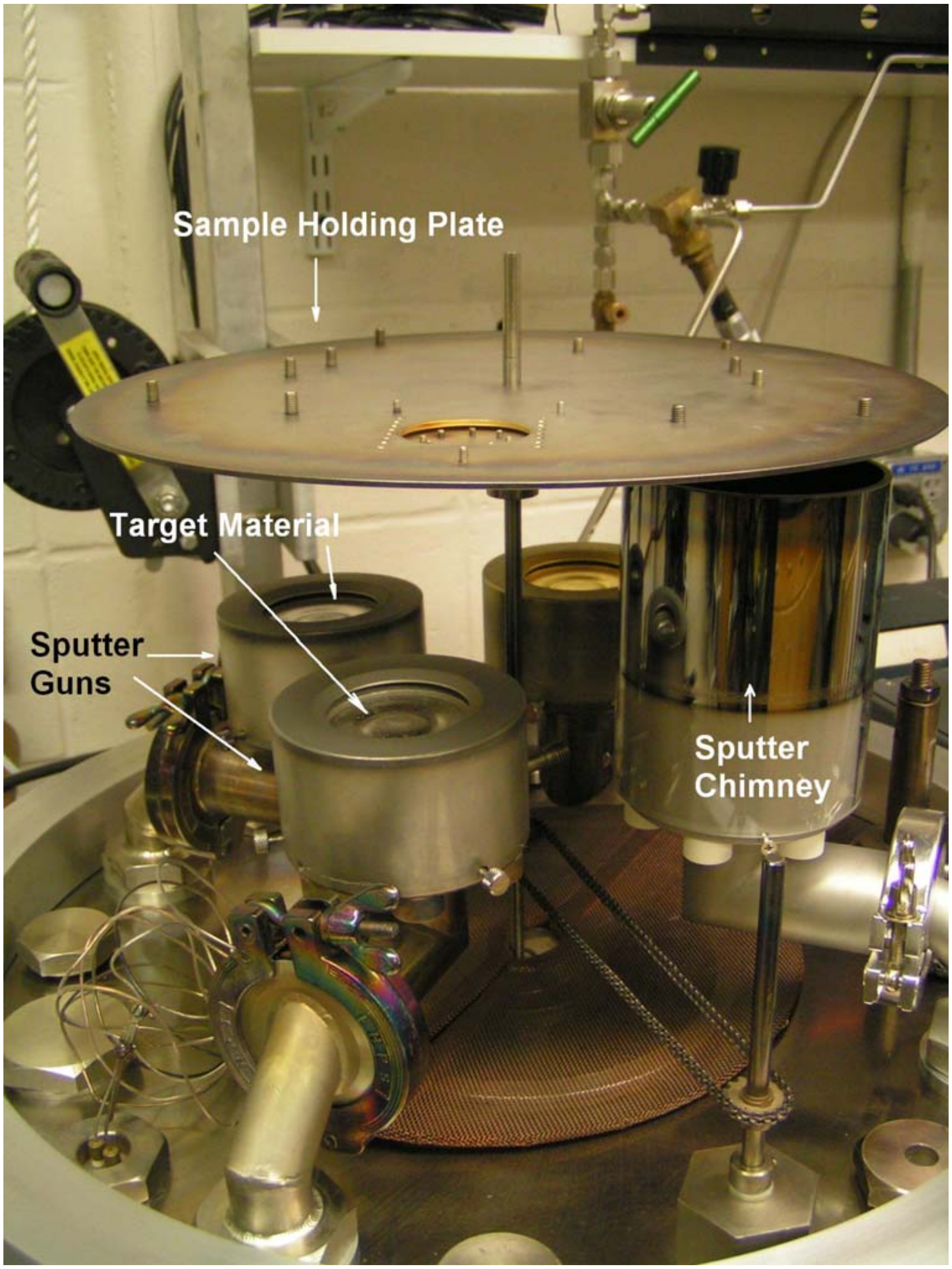


Figure 3.3.2 The inside of the sputtering system's vacuum chamber.

Figure 3.3.1 & Figure 3.3.2 shows the sputtering system used for metal deposition in this research. The following procedure was used:[62] the sample was loaded onto the metal plate on top of the sputtering gun facing towards the target material inside the vacuum chamber. This chamber achieved a vacuum of $2\sim5\times10^{-7}$ torr using a two-step pumping process composed of a roughing pump followed by the diffusion pump. Ar was then introduced into the chamber and the pressure of chamber maintained at 20 mTorr.

In a sputtering system, a gaseous plasma is created by applying a high voltage (300~400V) and the free electrons accelerate away from the cathode with enough momentum to eject the outer electrons from neutral Ar atoms to form Ar Ions (e.g. Ar^+) when collisions occur. The Ar ions are accelerated towards the cathode by the electric field, impacting the surface of the target material at the cathode with sufficient energy to eject some of the target material, either as single atoms or clusters of atoms or molecules, as neutral particles and free additional electrons to feed into the system. Unless affected by other particles, most of the ejected particles are deposited on the first surface they encounter, which in this experiment was a quartz chimney placed around the sputter gun to prevent the target material from depositing anywhere except the area at the top of the chimney where the sample was located. A magnet installed beneath the target material was used to generate a strong magnetic field immediately above the surface of the target in order to trap as many as possible of the free electrons in the vicinity and concentrate them along the magnetic field lines near the surface. This greatly increases the probability of ionizing the Ar atoms, enabling them to expel more particles from the target, and enhancing the deposition rate. Moreover, by trapping most of the free electrons near the target, fewer electrons are available to bombard the sample surface, resulting in less structural damage and reducing overheating.

It is important to note that the sputtering system used for this experiment was suitable only for depositing small areas, since most of the samples were smaller than 1 cm^2; for whole wafers or commercial fabrication, the system would require improvement and modification to achieve better uniformity and a faster sputtering rate. However, such systems have been developed for commercial applications. For example, in a confocal sputtering system multiple magnetron sputtering guns are arranged in a circular pattern, with the substrate located at the focal point and rotated on its own axis. This enables highly uniform single layers, multi-layers and co-deposited alloy films to be produced rapidly. For some systems, the angle of the guns and the working distance can be adjusted for better flexibility. Another approach uses a single gun for direct sputtering but ensures the target material diameter is at least 20%~30% larger than the substrate in order to retain reasonable uniformity. Although this tends to be relatively expensive, it allows sputtering target material to be swiftly deposited onto larger substrates.

3.4 Lift Off Process

Photolithographic techniques are primarily used for selectively depositing metal on desired areas by first covering the undesired areas with photoresist to protect them, although a photoresist may also be used either as the blocking layer for Reactive Ion

Etching (RIE) or to form a carbon cap. When forming the gate metal on MOS devices, a lift-off process to remove the protective layer of photoresist is therefore usually required after the metal has been deposited by the sputtering system. Here, soaking the sample in an organic solvent such as acetone removed both the photoresist and the metal deposited on top of it, leaving metal only on the areas not previously covered by photoresist. The sample was then soaked in methanol to remove residual acetone and rinsed in de-ionized water before being blown dry. For some devices, removing oxide that had built up on the backside was also necessary, in which case the sample was fully covered with crystal bond on the front surface and then dipped into BOE (Buffered Oxide Etchant) solution for 10 minutes. After rinsing off the residue with de-ionized water, the crystal bond was removed using acetone followed by methanol. After once more rinsing with de-ionized water and attaching the sample with silver paint onto a metal plate or gold plated ceramic as the back contact, the sample was ready for electrical measurement.

3.5 Rapid Annealing System

Figure 3.5.1 shows a photograph of the rapid annealing system used for this research. Due to its high vacuum level and fast heating capability, this system can perform multiple tasks during the MOSFET fabrication process. It consists of a vacuum chamber and a two vacuum pump system similar to that used in the sputtering system that enables it to achieve a vacuum of $1\sim3\times10^{-7}$ torr. A heating unit consisting of two carbon strips is located at the center of the chamber and an adjustable current source used to control the temperature. An optional carbon foam box, shown in Figure 3.5.2, was used to cover the whole heating unit for better temperature uniformity. An OMEGASCOPE OS1100 infrared pyrometer on top of the chamber and a thermocouple inside were used to monitor the temperature. For MOSFET fabrication this system was used for two processes, namely *implant activation* and *contact annealing*.

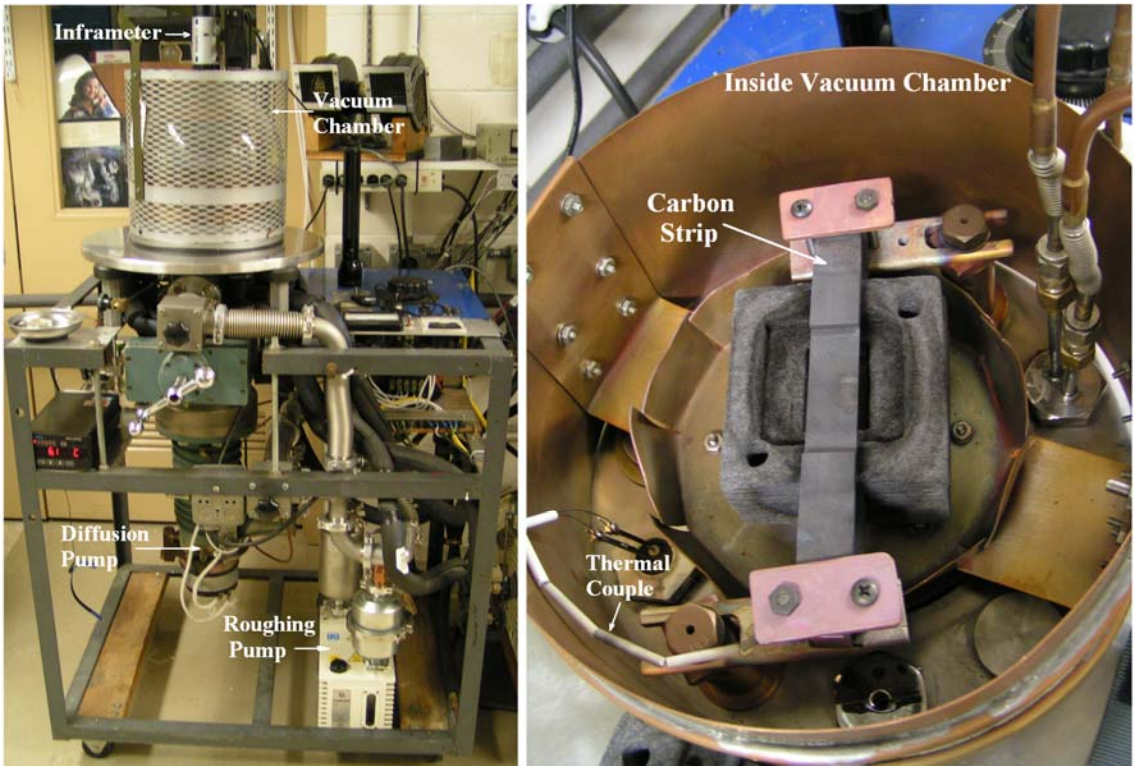


Figure 3.5.1 Fast annealing system and inside of vacuum chamber.

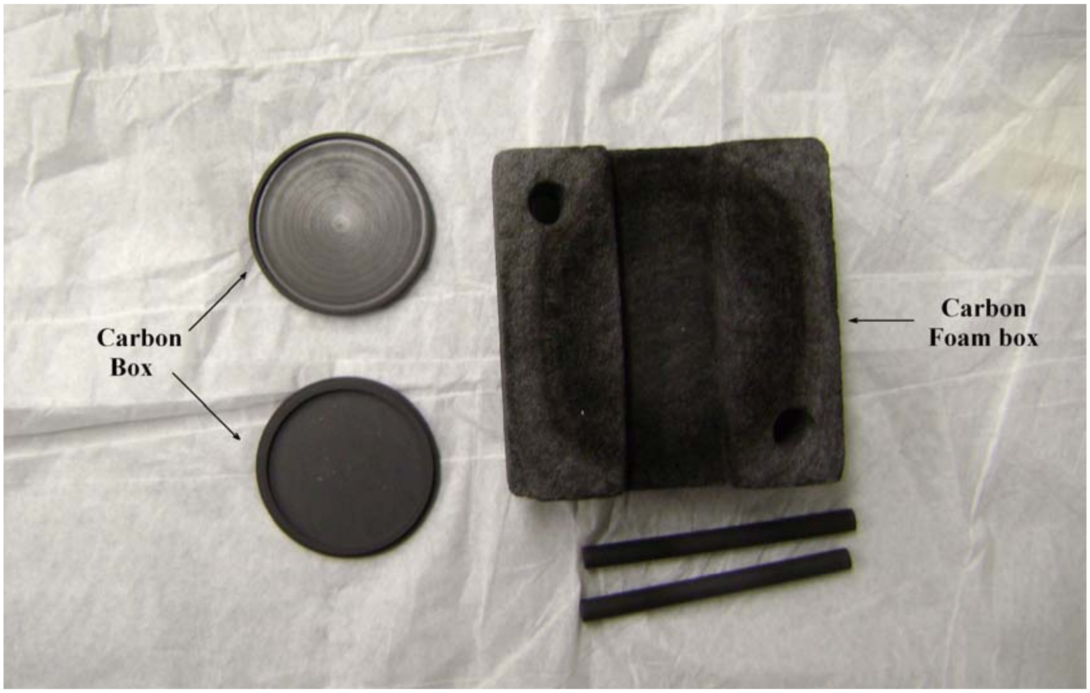


Figure 3.5.2 Circular carbon boxes and carbon foam box used for implant activation.

Two steps are involved in implant activation: the formation of the carbon cap and activation annealing. Here, samples were placed facing up in a circular carbon box to ensure uniform heating and placed between two carbon strips, covered with the carbon foam box. As this blocked the pyrometer, temperature was monitored through a thermocouple placed close to the carbon box. The samples had previously been coated with a ~1.5 μm spin-on layer of photoresist. The system was pre-pumped to the base pressure for 1~2 hours, and then filled with Ar. The current was adjusted to maintain a temperature of 900°C for 30 minutes to allow the photoresist to form a protective carbon cap and thus keep the surface of the substrate from evaporating during the high temperature anneal. Once the carbon cap forming step was complete, the samples were removed, placed face down in another carbon box, and loaded into the system, pre-pumped in the same manner. After the base pressure was reached, the box was gradually heated to the desired temperature to anneal the implantation in an Ar atmosphere.

The temperature required for activation varies depending on the implanted material, for example 1550°C for Nitrogen and 1650°C for Aluminum. Boron and Phosphorus are also commonly used for SiC doping. During this step, the ions that have been implanted diffuse into the crystalline lattice to form either p-type or n-type doped material. At the same time, the surface and crystal lattice damage caused by the ion bombardment during implantation are also partially annealed. It is important to note that not all the ions that have been implanted can be activated; for the samples used in this research the estimated activation percentage was about 80% ~100% for Nitrogen and 50% for Aluminum. Finally, the carbon cap on the annealed sample was removed in the RIE system by an O_2 plasma.

The rapid annealing system was also used in this research to perform contact annealing on the MOSFET samples. A layer of Ni (7%V) was sputtered onto the samples to form the source and drain contacts. However, if a metal is in direct contact with an n-type semiconductor with a lower work function than its own ($\phi_m > \phi_s$), in order to balance the Fermi levels on both sides at thermal equilibrium the bands at the semiconductor bend upwards and charge starts to accumulate at the metal/semiconductor interface. This creates a depletion region in the semiconductor surface and forms a natural energy barrier, causing the contact to behave as a diode, known as a Schottky diode.[63,64,65] Heating samples to a high temperature causes Ni to chemically react with SiC to form Nickel Silicide (Ni_2Si), which results in an Ohmic contact (like a common resistor, V-I will behave linearly). As the remaining area is already covered by oxide and some parts will be used as gate oxide, in order to minimize damage to and evaporation of the SiO_2 layer, a rapid thermal anneal is necessary. In the semiconductor industry, the mostly commonly used equipment for rapid anneals is the ion lamp, which heats up extremely rapidly and also offers precise temperature control and good uniformity. A few alternative methods are also available. Although the performance of the carbon strip heater used here is not as good as that of an ion lamp, it is still adequate for the contact annealing needed for this research.

The procedure used was as follows: a 1500 μm thick Ni(7%V) layer was first deposited on the sample, which was then loaded onto the carbon strip held directly by tungsten clips. The vacuum chamber was evacuated by the two step pumping system, taking 1~2 hours. After reaching the desired base pressure ($<5E\times10^{-7}$ torr), the chamber was filled with Ar. The contact annealing condition used here was 4 minutes at around $900^{o}C$. By supplying current through the carbon strip, this temperature could be reached in about 1~2 minutes, as monitored by the infrared pyrometer. After the desired time was complete, the current was cut off and the chamber cooled down in an Ar atmosphere.

3.6 Reactive Ion Etching (RIE) System

In the semiconductor industry, the two major methods used commercially for etching patterns on a substrate are wet chemical etching and reactive ion etching. The former method proceeds as follows: the sample is first patterned with a mask layer, which may be either a photoresist or a metal template, leaving the designated area exposed. The whole substrate is then immersed into a chemical solution that dissolves the exposed area until the desired amount of etching is achieved. This method is simple, inexpensive and quick and is especially suitable for etching a thin film on a substrate or removing a thin layer of the substrate itself, given an efficient etchant solution and a reliable mask material. It is often used, for example, for removing the patterned SiO_2 layer on top of an SiC or Si substrate on MOS devices using Buffered Oxide Etchant (BOE).

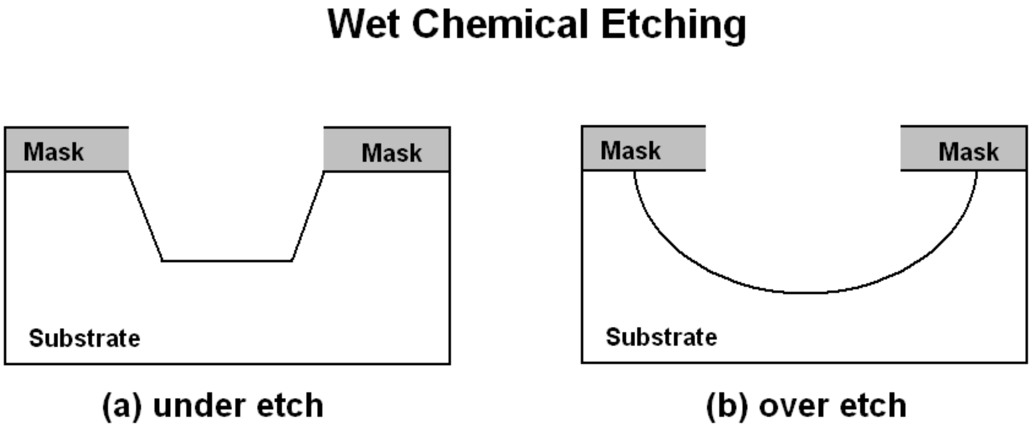


Figure 3.6.1 Diagram for wet etching: (a) under etching (b) over etching.

However, this approach suffers from two major problems, shown in Figure 3.6.1 (a) & (b), namely under etching and over etching. Particularly during anisotropic processes, the etchant is less efficient when the sidewalls are vertically deep, leading to under etching. In contrast, mostly happened in isotropic processes, the etchant significantly undercuts the masked layer, in some cases by the same distance as etching depth, leaving a cavity underneath the mask and compromising the performance of the device, which is known as over etching. In addition, due to the chemical inertness of SiC, it is very difficult to find a chemical solution for efficient SiC substrate etching.

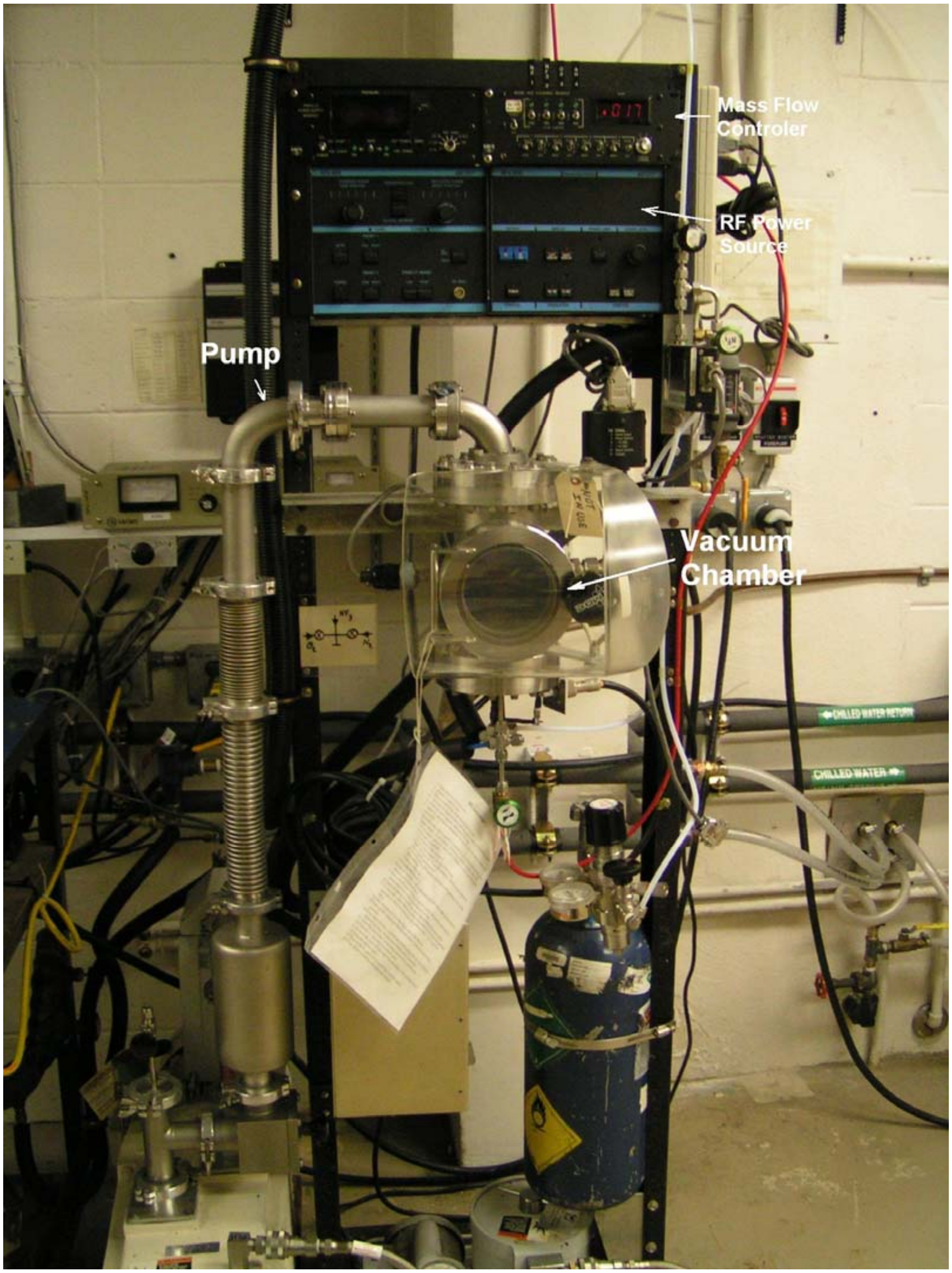


Figure 3.6.2 Reactive Ion Etching (RIE) system.

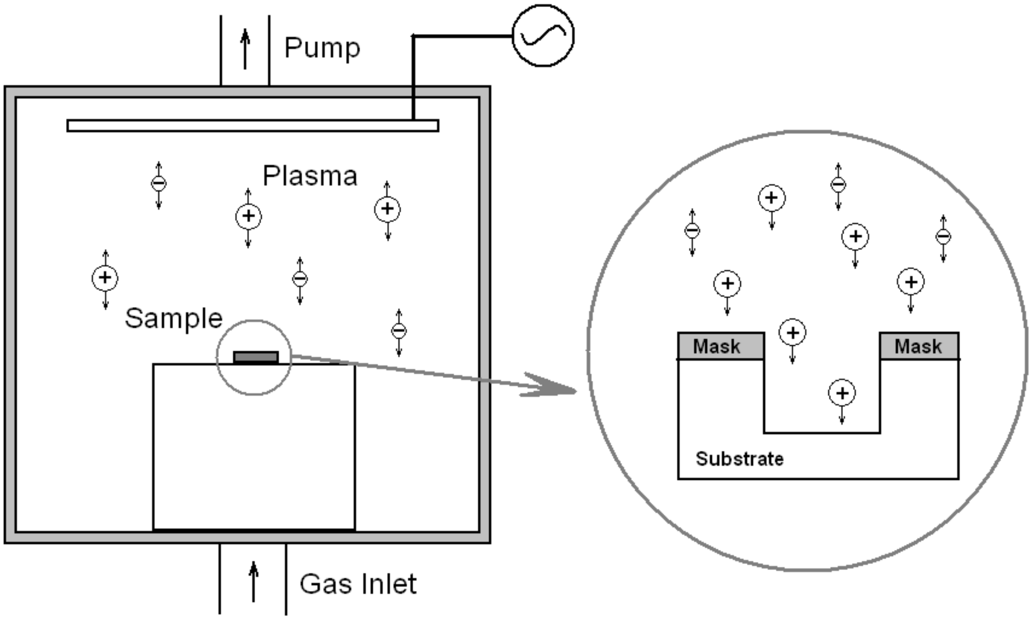


Figure 3.6.3 Diagram of the Vacuum Chamber in the RIE system.

An alternative approach, Reactive Ion Etching (RIE), avoids these issues and offers a useful method for etching SiC samples. It has become the preferred method for small size, high requirement devices due to its excellent resolution and precision. Figure 3.6.2 shows the RIE system used in this research, and Figure 3.6.3 provides a diagram of the inside of its vacuum chamber. This RIE system consists of a cylindrical vacuum chamber with a wafer platter located in the bottom portion of the chamber. The wafer platter, which holds the sample, is electrically isolated from the rest of the chamber. Gas enters through a small inlet at the bottom of the chamber, and exits to the vacuum pump through the outlet on top. The vacuum chamber can be pumped down to about 10 mTorr. The types and amount of gas used varies depending upon the etching process to be conducted, but the most commonly used are SF_6, NF_3, O_2, and N_2. NF_3 is commonly used for etching SiC, and in the work reported here the flow rate was set to 9 sccm at a pressure of around 40 mTorr. An RF power source is used to generate a plasma by dissociating the active gases and an AC voltage is then applied across the top plate and wafer platter, causing electrons and ions to start vibrating vertically. Here, the RC power was set at 18 watts.

Some of the etching takes place during this step, as the ions in the plasma are accelerated towards, and then react with, the surface of the substrate being etched to form further gaseous material and leave the surface. This is referred to as the chemical part of reactive ion etching. There is also a physical part that is similar in nature to the sputtering process: when the ions have a high enough energy, they may knock atoms out of the substrate surface physically with no chemical reaction. For etching SiC by NF_3, the possible reactions are thought to be as follows:[66]

$NF_3 = N + 3F$

$Si + 4F = SiF_4$

$C + xF = CF_x$

$C + xO = CO$ or CO_2

The etching rate achieved in this research was 2 microns per 15 minutes, and the masking of the pattern utilized an Ni (7%V) layer for most samples, with varying thicknesses depending on the desired etching time. In some cases a photoresist was used as the mask material. The major advantage of RIE is that as the reactive ions are primarily delivered vertically, the etching profile can be significantly anisotropic, forming very sharp vertical sidewalls. The ions in the plasma are also more chemically active, so the etching rate of RIE can be much higher than that for a wet etching process using a solution of the same etchant.

A popular modified RIE process is Deep RIE, also known as the Bosch Process, which was originally proposed and patented by a German company, Robert Bosch.[67] During this process, two different gas compositions are alternately introduced into the reactor chamber, with each phase lasting for a few seconds. The first gas composition reacts with the substrate to form a chemically inert passivation layer that covers the entire sample. For instance, using C_4F_8 as a source gas with Si yields a substance similar to Teflon. The second gas composition then etches the substrate vertically. In the case of Si, SF_6 is often used in this step. The passivation layer at the bottom of the trench can be immediately sputtered away by the physical part of the etching, exposing the substrate to the chemical etchant, but not the sidewalls. Since the passivation layer dissolves very slowly in the chemical part of the etching, it builds up on the sidewalls and protects them from etching. These etch/deposit steps are repeated many times during the process and as a result, etching aspect ratios of 50 to 1 can be achieved. The process can easily be used to etch completely through a silicon substrate, and etch rates are 3~4 times higher than can be achieved by wet etching. Consequently, this process is now widely used in the fabrication of micro-electro-mechanical systems (MEMS). It has also found many applications in micro-electronic device processes, especially for opening deep trenches.

3.7 Simultaneous High-low Frequency C-V Probe Station

Simultaneous high-low frequency Capacitance-Voltage (C-V) measurement is the most commonly used method for characterizing MOS capacitors, which are both very important and the simplest MOS structure. A detailed discussion of these MOS devices were provided in Chapter 2.

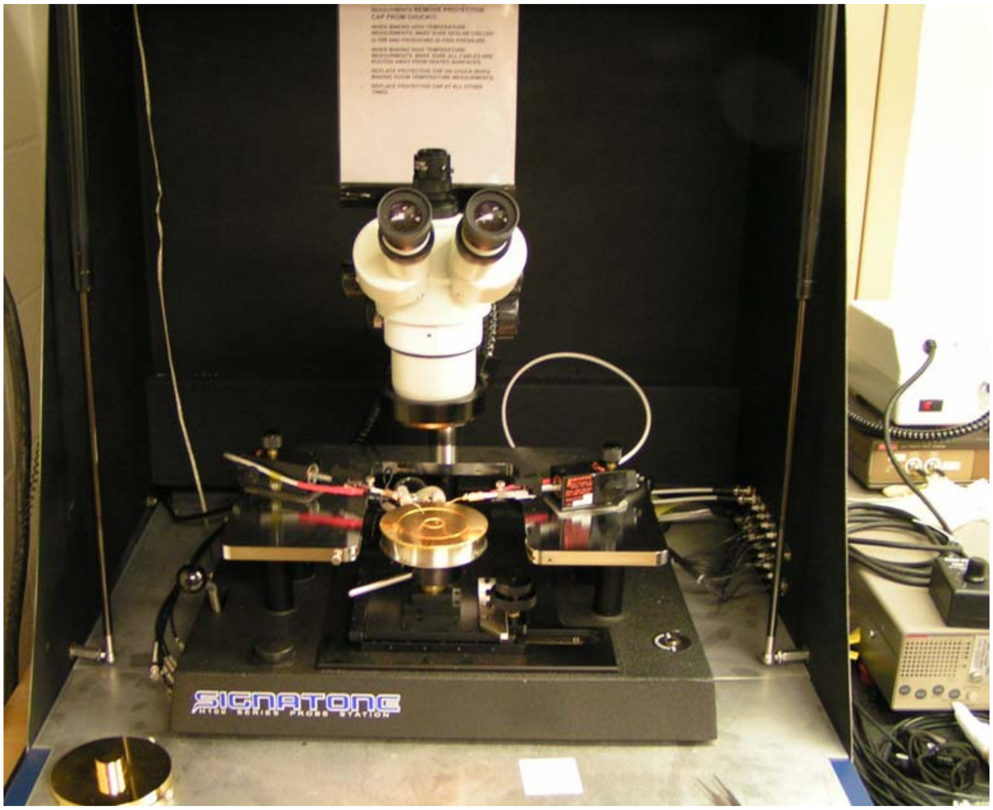


Figure 3.7.1 Probe Station for room temperature and high temperature C-V measurement.

Figure 3.7.2 Keithley CV analyzers and temperature controller for C-V measurement.

Figure 3.7.1 shows a photograph of the probe station used for all the C-V measurements in this research. The station was placed inside a grounded black box for better insulation from electrical and magnetic fields and light, all of which can interfere with the measurements. In most cases the sample was placed on the gold plated sample holder, which was then heated or cooled to the desired temperature by the temperature controller shown in Figure 3.7.2. The probes were located on adjustable bases and were connected to the sample using gate and backside contacts. An adjustable optical microscope was incorporated and used to locate devices and operate probes.

As shown in Figure 3.7.2, the equipment used for the simultaneous high-low frequency C-V measurements were a Keithley 590 Quasi-static C-V Meter for the quasi-static part, and a Keithley 595 C-V Analyzer for the high-frequency part. The voltage for the measurements was provided by a Keithley 230 Programmable Voltage Source. These components were controlled using the *Interactive Characterization Software* (ICS) package supplied by Metric Technology, Inc, which automatically ran the measurements, recorded the raw data, extracted parameters, and then plotted, exported and printed the final data. In addition to room-temperature measurements, elevated temperatures were possible using a SIGNATONE S-1060 Series Temperature Controller with Active Cooling, which was capable of rapidly heating the sample to 300^{o}C. Although higher temperatures were possible, they were not needed for this research.

Measurements of actual devices using the pre-stored profile in ICS was conducted and the data extracted automatically. During the measurement, the device was swept from accumulation to depletion using a slowly changing DC voltage to obtain a continuous quasi-static C-V curve. A high frequency signal (100KHz for room temperature, and 1MHz for high-temperature measurements) was simultaneously applied between the gate and back contact, adding and subtracting a small ΔQ all the time. Since most of the interface traps (discussed in the next chapter) and other possible defects typically do not have time to respond to such high frequencies, the charges due to them will mostly remain unchanged and their effect on parameters such as flat-band voltage will not vary with time.[47] This produces a very good approximation to an ideal curve and the high-frequency behavior of the device can therefore be assumed to be the theoretical ideal curve in calculations. For example, the separation between the high frequency and quasi static C-V curve provides an indication of the number of interface traps. More details are available in the ICS manual,[68] but a few points regarding the choice of the actual measurement parameters are addressed below:

i) In all the measurements reported here, the top probe as the gate voltage was kept grounded, while the backside bias voltage was varied during the measurement. This was done to minimize background noise by grounding the gate contact;

ii) The start and stop voltages were carefully selected, as according to the User's Guide [69], due to the fact that most of the parameters were extracted from the steep transition or depletion region, it was important that the depletion region should make up about 1/3 or 2/3 of the voltage range of the C-V curve. Moreover, as some parameters were extracted form the accumulation region, for example C_{ox}, it was also necessary for the start or stop voltage to bias the device into strong accumulation;

iii) The choice of the step voltage was also critical as it determined the number of data points during the sweep. Too few data points would have given poor results, but too many data points would have increased the noise more than the resolution for the measurements and would also have considerably increased the time needed for each sweep.

iv) The sweep direction was set to sweep from accumulation to depletion for most samples in order to measure deeper into the semiconductor to achieve deep depletion-profiling. This also made it faster and easier to reach equilibrium at accumulation before measurement.

v) Not only did the samples have different gate metals, such as Molybdenum or highly doped Poly-Silicon, but also the gate contacts varied considerably in size, with the most commonly used being 300 μm and 600 μm diameter circles. It was therefore important to remember to change parameters such as W_{MS} (metal-semiconductor work function) and the contact area appropriately before taking the measurements.

In addition to the C-V measurements, extracting the parameters from the data obtained was performed using the pre-loaded C-V Libraries from Keithley. All the detailed parameters were later exported to Excel for further analysis and plotting. For further details of all the equations used to extract the major parameters of a typical C-V measurement, please refer to Appendix C of this dissertation. The physical origin and explanation of these parameters were discussed in Chapter 2.

3.8 I-V Probe Station and Measurement

The I-V characteristic and breakdown field are important parameters for oxides on MOS devices, especially power MOS devices. This character can be measured on a MOS capacitor with the I-V station.

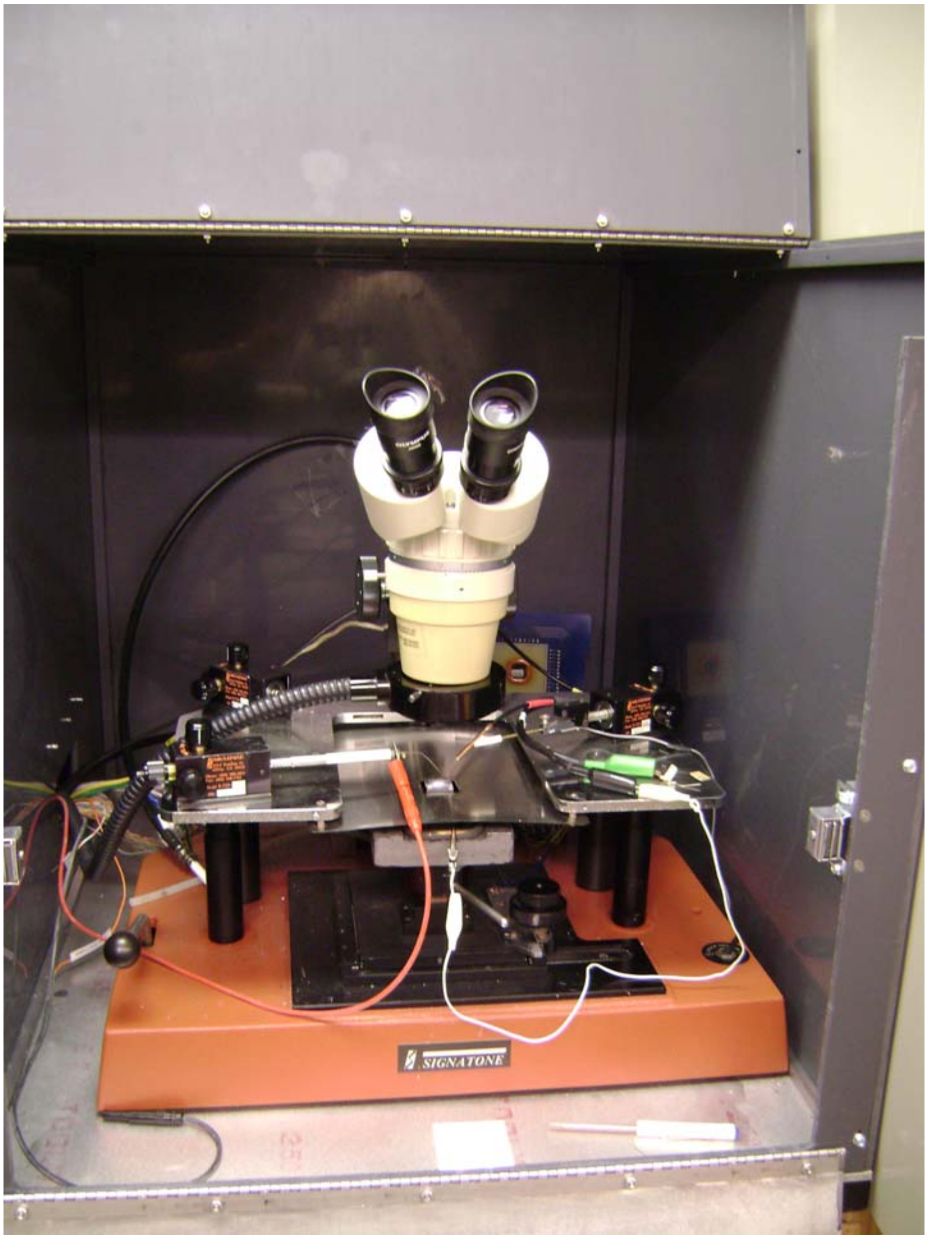


Figure 3.8.1 Probe station used for I-V measurements.

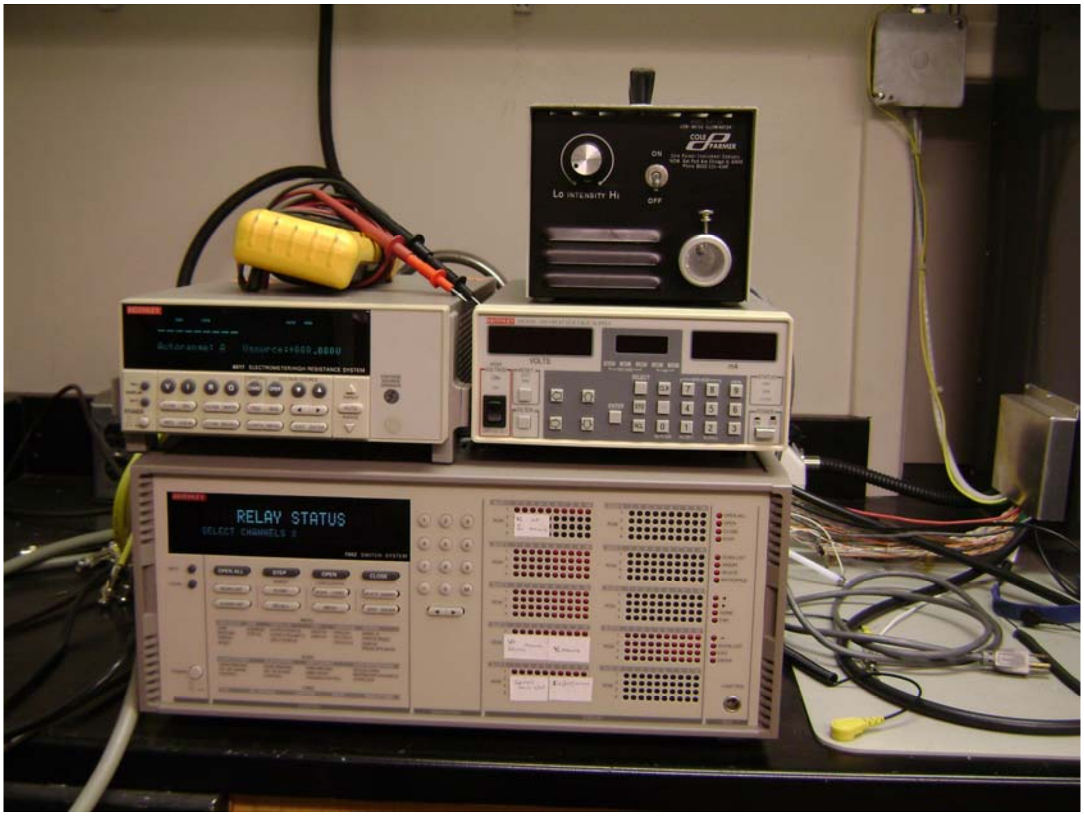


Figure 3.8.2 Equipments used for I-V measurements.

The probe station used for this measurement is shown in Figure 3.8.1. As with the C-V probe station, it is located in a grounded black box in order to block light, external fields and interference. The optical microscope on top of the probes is used to locate the sample and apply the two needles used as probes, one of which is grounded for the backside contact, and the voltage on the other can be varied for the gate contact. This probe station is also capable of high temperature measurements at 200~300°C. As shown in Figure 3.8.2, this probe station is connected to a Keithley 6517 electrometer and a Keithley 248 Voltage Source, both of which are controlled by a Labview program that simultaneously measures the applied gate voltage and the current. Data is later exported and processed by Excel.

Before the I-V measurement was performed on each sample, the C-V measurements were conducted in order to characterize most of its parameters, as devices are usually destroyed by I-V measurement. During these measurements, a gate bias is applied and swept from 0V to high voltage, usually tens of volts, with current monitored until breakdown occurs. The data obtained is usually plotted as current density (*A/cm*^{2}) vs. oxide field (*MV/cm*). The breakdown field for a device is usually considered as the point on the plot where a drastic increase in the current density is seen. Otherwise, it is taken to be the point at which the current density reaches 1E + 5 *A/cm*^{2}.

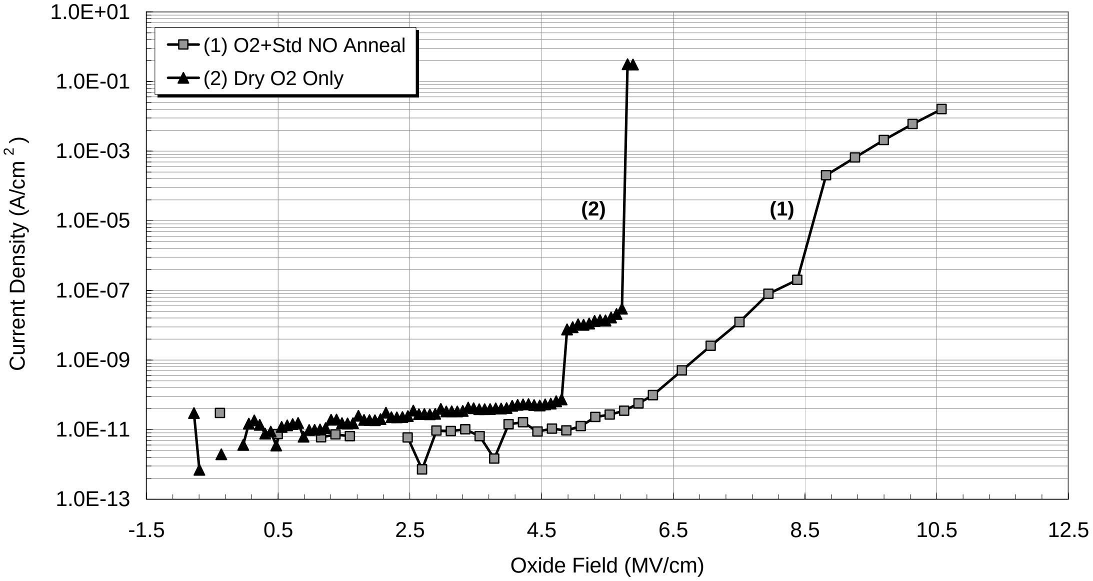


Figure 3.8.3 I-V characteristic of MOS capacitors with oxide grow with standard dry O_2 and standard dry O_2+standard NO anneal.

To illustrate this, Figure 3.8.3 shows the current density vs. oxide field plot of two MOS capacitors with different gate oxides, one oxidized using the standard dry O_2 procedure and the other grown with standard dry O_2 followed by the standard NO anneal. The breakdown field for these two devices, according to the plot, is ~6 *MV/cm* for the sample oxidized with dry O_2, and ~8.5 *MV/cm* for dry O_2 followed by NO anneal. Both the current density and oxide field are calculated from other measured parameters. Current density is defined by Current (A)/Area (cm^2), while the calculation of the oxide field is more complicated. Theoretically, for an ideal device the oxide field simply equals applied voltage (V)/oxide thickness (cm), but as mentioned in Chapter 2, due to other non-ideal factors in a real device the flat band condition is not at 0V but shifted by ΔV. In order to incorporate this into more accurate field calculation, the oxide field must be calculated using the information in Table 3.8.1.

Note that the oxide field calculated in this manner is still an estimate and it is important to be very careful when taking these values as the actual field. However, as a comparison between breakdown fields for different oxides using different oxidation and annealing conditions, using the same method to calculate all the oxide fields should be a reasonable approximation.

Table 3.8.1 Formulas for oxide electric field calculation in accumulation.

Doping	Oxide field for negative fixed charge	Oxide field for Positive fixed charge
n-type	$\frac{V-\varphi_{MS}}{t_{ox}}\hat{i}$	$\frac{V-V_{FB}}{t_{ox}}\hat{i}$
p-type	$\frac{V-V_{FB}}{t_{ox}}-\hat{i}$	$\frac{V-\varphi_{MS}}{t_{ox}}-\hat{i}$

* Table provided by Dr. Sarit Dhar, Vanderbilt University, Nashville,TN.

V = applied voltage;   *ϕ_{MS}= Work function Difference;*
V_{FB}= Measured flat-band,   *t_{ox}= Oxide thickness*

- *Direction convention : + i indicates electric field from metal to semiconductor*
- *Formulas independent of whether $\phi_{MS} > 0$ or $\phi_{MS} < 0$*

3.9 MOSFET Mobility Measurement

In addition to the MOS capacitors used in this research, another very important MOS device tested was the lateral n-channel MOSFET. Although many parameters are important for a MOSFET device, this study focused primarily on the I_D-V_G data and the mobility values that can be extracted from it.

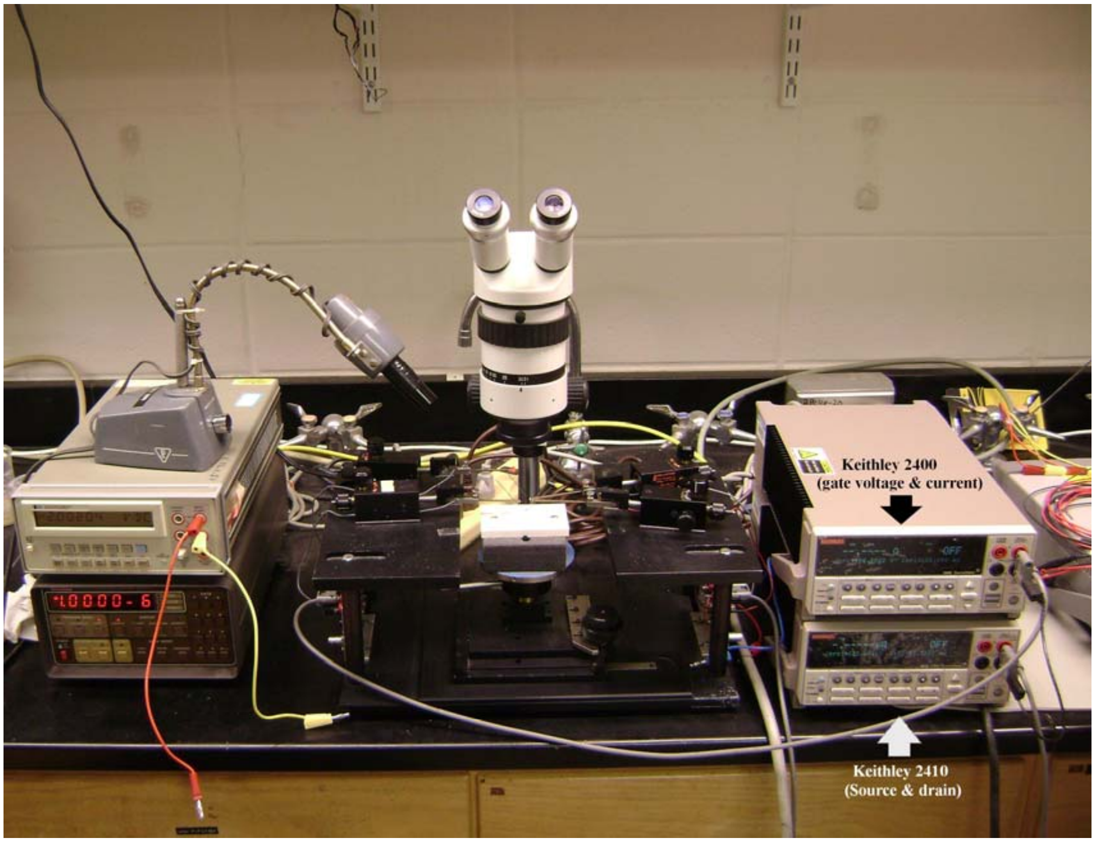


Figure 3.9.1 Probe station for mobility measurements.

The probe station shown in Figure 3.9.1 was used for the mobility measurements conducted for this research. As the photograph shows, two source measurement units, a Keithley 4100 and a Keithley 4210, were used, both of which are capable of applying voltage and measuring current at the same time: the Keithley 4100 measures gate voltage V_G and gate current I_G, while the Keithley 4210 measures source and drain voltage V_D and current I_D, with source and backside grounded. A Labview program was used to control them and automatically extract the data. Generally, the applied gate voltage on the device was swept from 0V to about 5~8V, and the I_D-V_G data obtain and plotted.

According to the linear model section 2.2.3 in Chapter 2, their relation can be expressed by Eq 2.3.7:

$$I_D = \mu C_{ox} \frac{W}{L} V_{DS} (V_G - V_T), \quad \text{valid for } |V_{DS}| << (V_{GS} - V_T)$$

Channel Mobility μ can then be calculated by the slope g_m on the I_D-V_G curve using Eq 2.3.8:

$$\mu = \frac{L}{W} \frac{1}{C_{ox} V_{DS}} g_m, \quad \text{with } g_m = \left. \frac{d(I_D)}{d(V_G)} \right|_{V_{DS}}$$

Here, for all of the MOSFET devices,

I_D: drain current (I)

V_G: gate voltage (V)

L: channel length = 150 μm

W: channel width = 290 μm

V_{DS}: drain-source voltage = 0.025 V

C_{ox}: capacitance per area (F/cm^2), varies with different oxide thickness. Typical values for the gate oxide (usually 35~75nm thick) were of the order of 10^{12} F/cm^2

Another important parameter is the threshold voltage V_T. There are many ways to define V_T, but the method applied here is $V_T \approx V_{on}$, which is defined by the interception of the tangent line of I_D curve at its maximum slope with the V_G axis, from the I_D-V_G curve.

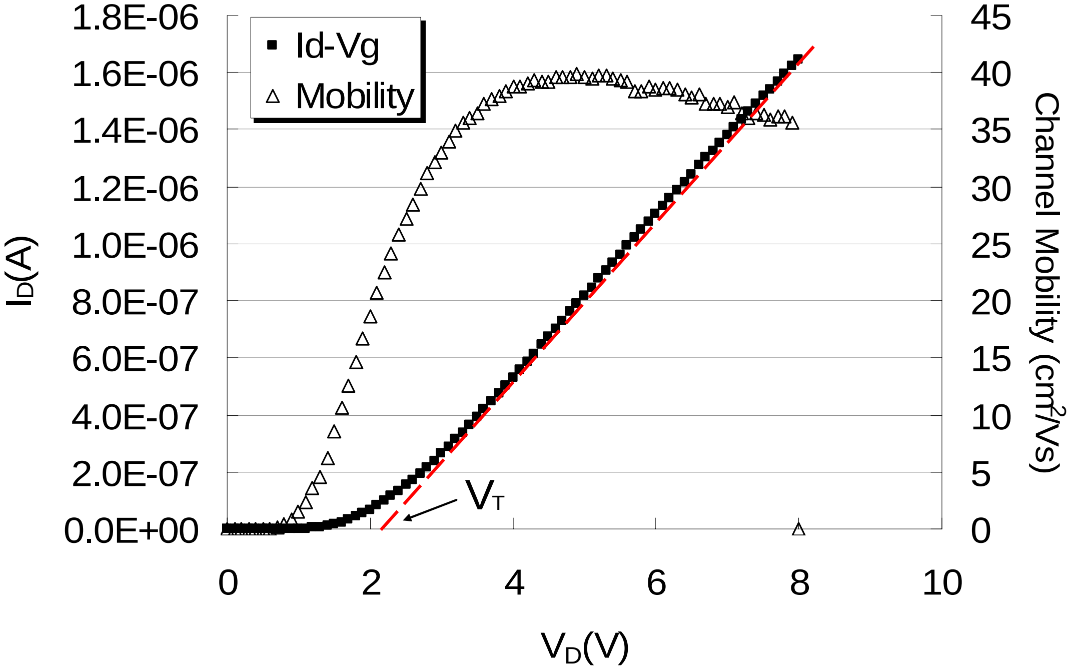


Figure 3.9.2 Typical V_T, I_D-V_G and channel mobility measured from an n-channel 4H-SiC MOSFET, with gate oxide grown in dry O_2 followed by NO anneal.

As an example, Figure 3.9.2 shows a typical value of the threshold voltage V_T, I_D-V_G curve and channel mobility μ measured from an n-channel 4H-SiC MOSFET, with the gate oxide grown in dry O_2 followed by a standard NO anneal.

Details concerning the properties of this MOSFET structure, the physical interpretation and the derivation of the equations and methods mentioned above were explained and discussed in Section 2.3 of Chapter 2.

CHAPTER 4

Current Oxidation and Passivation Procedures

4.1 General Introduction

As mentioned previously, SiO_2, the natural oxide of SiC, is commonly used as the insulator in SiC devices. As in the fabrication of Si based materials, the most straightforward and common approach used is oxidation in a dry O_2 environment inside a quartz furnace. However, compared to directly forming SiO_2 from Si as $Si+O_2 = SiO_2$, forming an oxide on SiC under the same conditions is more complicated and difficult. Before the oxide can be formed an Si-C bond must first be broken in an O_2 rich environment, allowing SiO_2 to form and releasing the excess carbon atoms as CO or CO_2 gas.[70,103] This reaction proceeds relatively slowly, and it is believed that there are several intermediate chemical reactions and transforming steps.

Aside from the dangling bond created by the oxygen deficiency at the interface, the most important difference between the SiC/SiO_2 and Si/SiO_2 interfaces is that during the oxidation process, rather than the chemically abrupt interface seen in Si/SiO_2, the

SiC/SiO_2 interface has a transition layer several nm thick,[71] as revealed by techniques such as HRTEM and EELS[72]. However, due to the limitations of current technology the physical structure and chemical composite of this layer remains unclear. The other major problem with the SiC/SiO_2 interface arises due to the fact that carbon is continuously released during the oxidation process, resulting in excessive free carbon at the interface that tends to form carbon clusters with various sizes and other possible structures.[73,103,104] forming defects at the interface and throughout the oxide, and introducing traps at and near the interface.

These two factors are believed[87,103,104] to be mostly responsible for the high interface trap densities at the SiC/SiO_2 interface and in order to reduce the number of traps and improve the quality of the oxide and the SiC/SiO_2 interface an effective passivation procedure following the termination of oxidation has been found to be useful. Many passivation methods first developed for the silicon industry have been tested over the past few years, such as NO and H_2 anneals, and these will be introduced and their effectiveness discussed in the following sections.

4.2 Standard Dry O_2 Oxidation

4.2.1 General Procedure for Standard Dry Oxidation

The quartz furnace described in Chapter 3 was used for this oxidation. The samples generally consisted of 5×5 mm n-type or p-type 8^{o} off 4H-SiC, with a 10μm thick epi-layer with a typical doping concentration of about 5~7×10^{15}cm^{-3}. Samples were slowly loaded into the furnace using a quartz paddle in an Ar atmosphere at 900^{o}C. The temperature was then increased to 1150^{o}C at a rate of 5 ^{o}C/min with Ar flowing at 500 sccm. Dry O_2 gas was introduced into the furnace at 500 sccm once the furnace reached the desired temperature. The oxidation process usually required 5~6 hours, depending on the desired thickness of oxide, after which the O_2 was switched off and Ar gas flowed over the sample at 500 sccm at 1150 ^{o}C for 30 minutes to flush out residual O_2 and complete the oxidation. Finally, the temperature was ramped down to 900 ^{o}C and the sample removed with the Ar flowing.

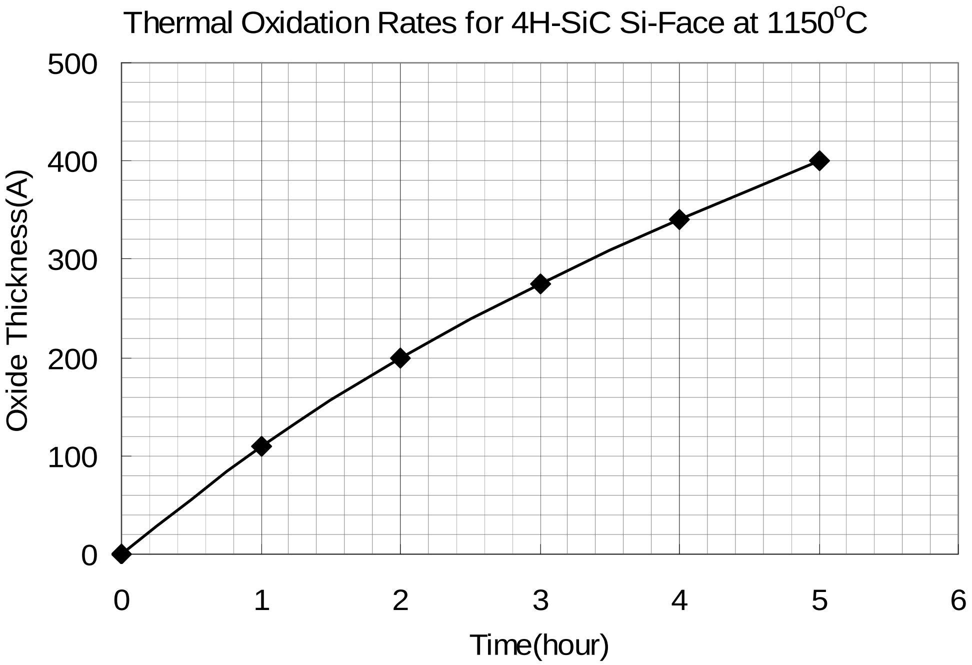


Figure 4.2.1 Measured growth rate using standard dry O_2 oxidation process.

The measured growth rate of a typical sample using the standard dry oxidation process described above is shown in Figure 4.2.1. Note that this rate is necessarily an estimate; the presence of low levels of contamination inside the furnace, residual gas from previous runs (e.g. O_2, NO, H_2, H^+), and small variations in the temperature means that the actual oxidation rate always varies slightly from run to run. This growth rate will also vary for different furnaces.

After the oxidation was completed, the sample was patterned using dark masks with circular patterns in various sizes. AZ5214E photoresist and 400K developer were used for the lithography. Samples were then sputtered with 1000 Å thick high purity Molybdenum as the gate contact using the sputtering system described in Chapter 3. In early runs a layer of gold was then sputtered on to the Mo as a cover metal, since Mo oxidizes easily when exposed to atmosphere, but in later runs this was discontinued due to the potential for mobile ion contamination and the diffusion of these impurities into the sample. After the lift-off process, the backside oxide was removed by BOE wet-etch and the front side covered with crystal bond. Finally, the sample was pasted onto a metal plate using silver paint as the backside contact for ease of handling, after which the electrical parameters were measured by the C-V station described in Chapter 3 using simultaneous high-low C-V measurement.

4.2.2 Electrical Characteristics of Standard Dry Oxidation

4.2.2.1 C-V Measurements and D_{IT} for MOS Capacitors

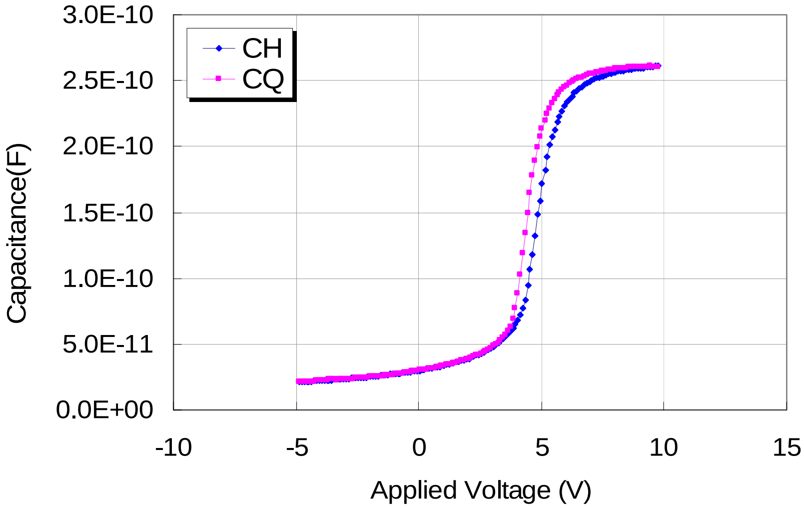


Figure 4.2.2 Room-temperature (23^{o}C) C-V curve for an n-type 4H-SiC MOS capacitor with oxide grown by standard O_2 oxidation.

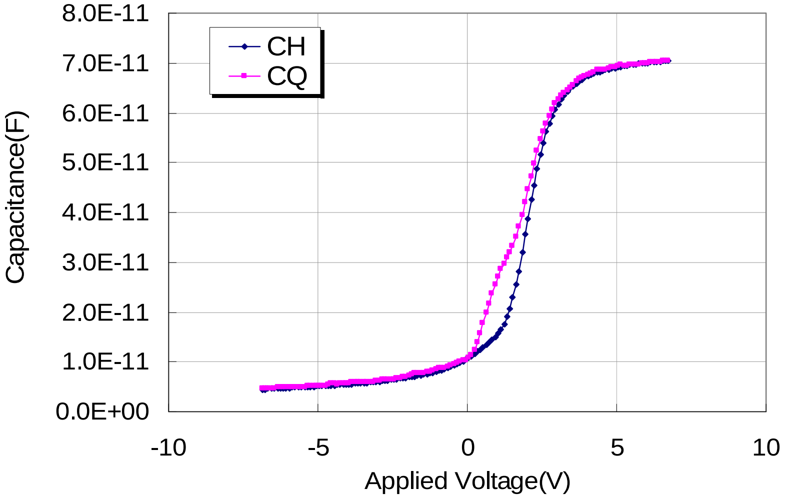


Figure 4.2.3 High-temperature (300^{o}C) C-V curve for an n-type 4H-SiC MOS capacitor with oxide grown by standard O_2 oxidation.

Figure 4.2.2 & Figure 4.2.3 shows the room-temperature and high-temperature (300^{o}C) C-V characteristic of a typical n-type 4H-SiC MOS capacitor fabricated using the procedure outlined above. CH represents the adjusted high frequency (100KHz for 23^{o}C and 1MHz for 300^{o}C) capacitance curve, and CQ represents the adjusted quasi-static capacitance curve. This sample had 300 um diameter contacts and the thickness extracted from the C-V curve was around 39 nm, with V_{FB} at 3.9V. The value for measured V_{FB} under similar conditions is typically around 3V, which gives the effective oxide charge Q_{eff} a value of 2~3E-7 *C/cm^{2}*.

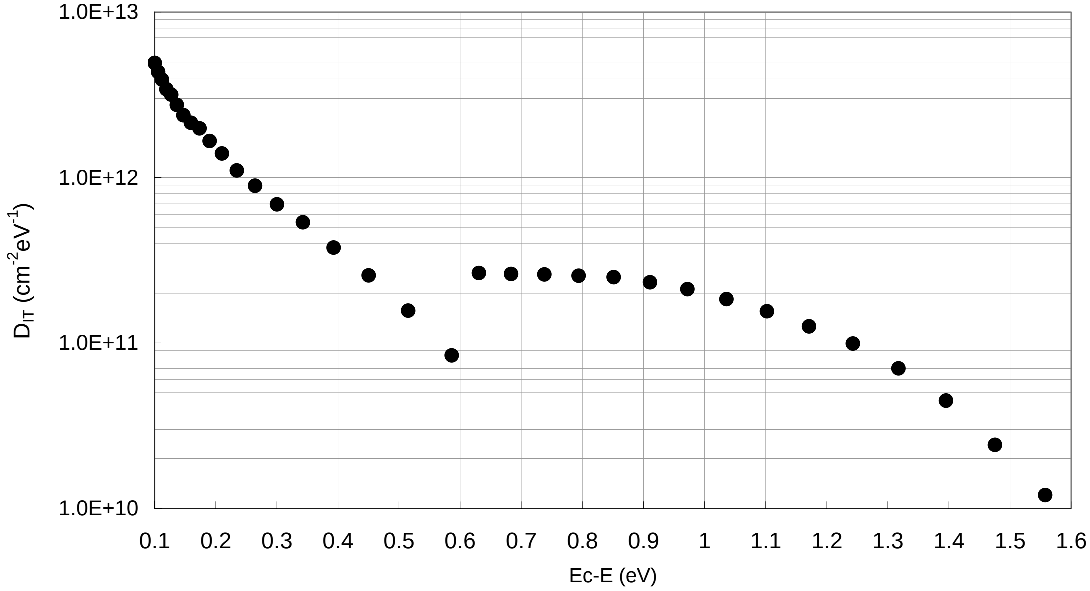


Figure 4.2.4 Density of Interface-Traps (D_{IT}) extracted from C-V curve in Figure 4.2.2 & Figure 4.2.3.

Figure 4.2.4 shows the D_{IT} curve extracted from the C-V curves in Figure 4.2.2 and Figure 4.2.3, which starts from 0.1eV below the conduction band and extends to around mid-gap. Note that as mentioned in previous chapters, the accuracy of a D_{IT} curve extracted from the C-V depends on the temperature and energy level. The D_{IT} in the range of 0.1~0.6eV below E_C was extracted from the room-temperature C-V measurement, while the D_{IT} at 0.6eV~1.6eV below E_C was extracted from the high-temperature (300^{o}C) C-V measurement. Consequently, the discontinuity in the D_{IT} curve at around 0.6eV below E_C is due to the fact that the two parts of the curve actually represent different C-V measurements at different temperatures. An in-depth discussion of the procedure used to extract D_{IT} curves and the equation used are given in Section 2.2.4.3 and Appendix C.

From the curve, at 0.1eV below E_C the value of D_{IT} is about 5~6x10^{12} cm^{-2} eV^{-1}, but as explained earlier the equations become increasingly inaccurate at high D_{IT} values. However, the number of interface traps measurement by other methods agrees with this value, which indicates that it is close to the actual D_{IT} values for the device. Also, as most of these values are for comparison purposes only, this will not affect the conclusions reached. Typically, for well-made Si based devices the D_{IT} is about 1x10^{10} to 1x10^{11} $cm^{-2}eV^{-1}$ near the conduction band, indicating that the D_{IT} of SiC based device is much higher than similar Si base devices. This suggests a far greater number of interfacial traps and defects are present at the interface, which is likely to be one of the main factors causing low channel mobility, reduced conductance and eventual poor performance of SiC based MOS devices. The mechanism by which channel mobility is affected is believed to be as follows: 1) defects trap free electrons as carriers, reducing current and leading to a slower response time for the device; 2) by trapping electrons, these traps become negatively charged, thus further reducing the current by creating a coulomb field and scattering other free electrons nearby.[74]

4.2.2.2 V_T and Channel Mobility for N-channel MOSFETs

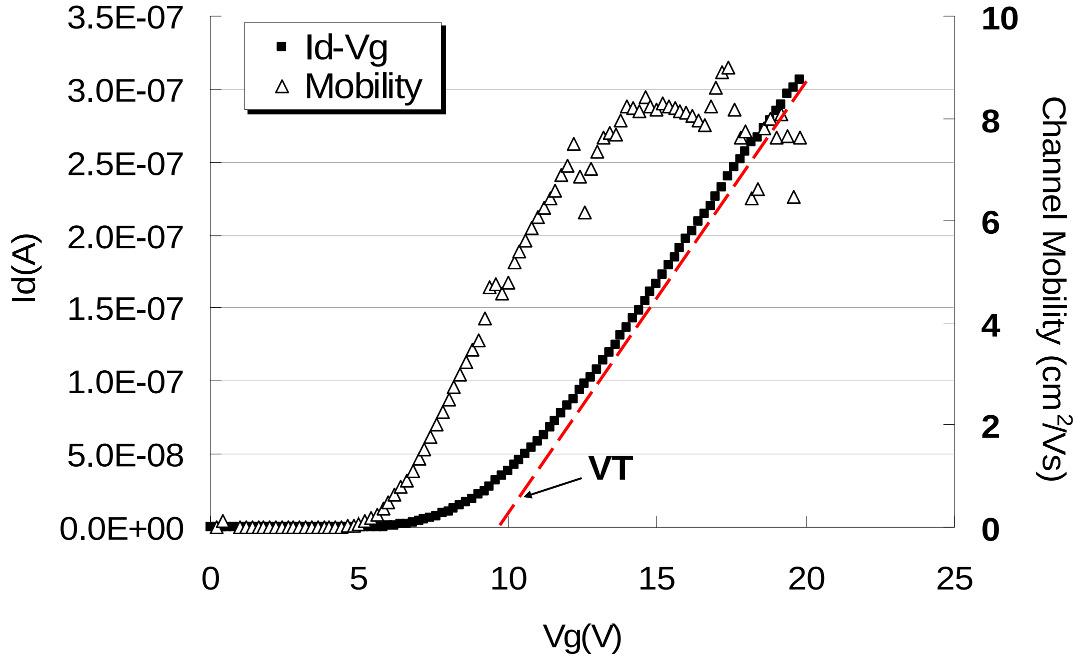


Figure 4.2.5 Channel mobility μ of n-channel MOSFET with gate oxide grown under standard dry O_2 oxidation.

In order to measure effective channel mobility, an n-channel MOSFET was fabricated according to the procedure in Appendix B. The gate oxide was grown under similar conditions to those used for the MOS capacitor discussed above. Figure 4.2.5 shows a typical mobility curve for this type of MOSFET, with the parameters mentioned in Section 3.9, with a gate oxide thickness of around 40 nm. The peak value of measured mobility in this sample was around 8 cm^2/Vs, which agrees with widely reported values for the channel mobility of standard dry O_2 gate oxide MOSFETS. However, this value is far below the bulk mobility of 4H-SiC, which is around 800 cm^2/Vs, and is especially striking when compared with that of Si based devices, which can achieve almost half of the bulk mobility. The threshold voltage V_T in this plot was around 8V.

4.2.2.3 I-V Characteristics and Breakdown Field

What is more, the I-V characteristic of the standard dry O_2 oxide is shown in Figure 4.2.6 below.

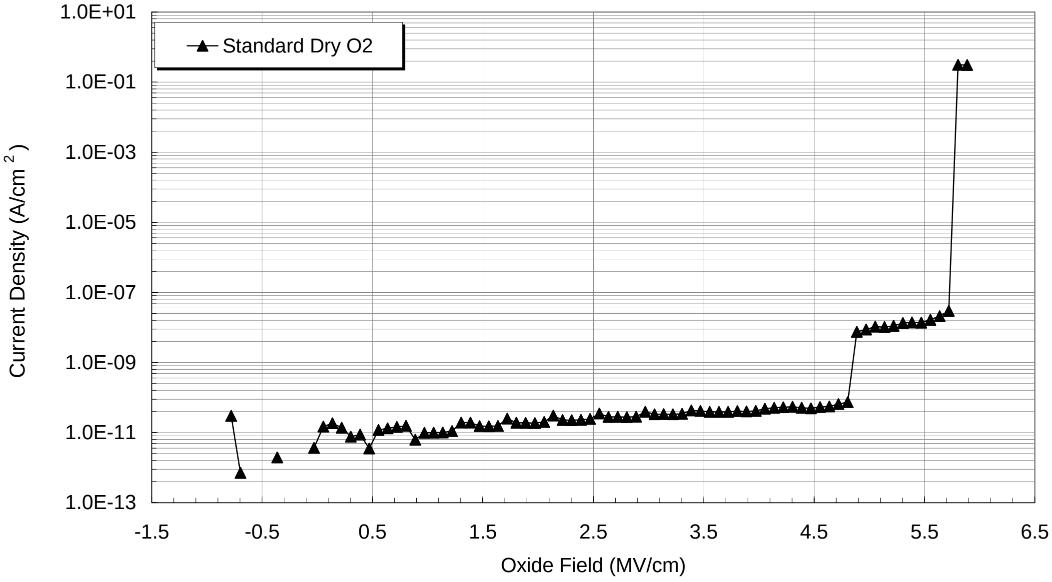


Figure 4.2.6 I-V characteristic for an MOS capacitor with oxide grown by standard O_2.

The value for the breakdown field for this oxide is typically 5~6 MV/cm. Details of the measurement and calculation of the field are given in Section 3.8. Note that the calculated field is an estimate, and may differ from the actual field inside the oxide. For high-voltage power MOS devices, the main application area for SiC based devices, the value of this breakdown field requires further improvement, which can be realized by using a post-oxidation anneal, as discussed in the next section.

4.2.3 Summary for Standard Dry Oxidation

The use of SiO_2, the naturally occurring oxide on SiC, as the insulator on MOS devices provides some promising properties and appears to offer a useful approach. However, compared with similar Si based devices, the quality of SiO_2/SiC is far below expectations, which severely limits the reliability and performance of devices. In order to address this, the use of a post-oxidation anneal is necessary.

4.3 Nitric Oxide (NO) Anneal

4.3.1 General Introduction and Procedure for Standard NO Anneal

One of the most widely used types of anneal in the silicon industry is a Nitric Oxide (NO) anneal. This was first reported by Li et al[75] on 6H-SiC and Young et al[1,76] on 4H-SiC. For 4H-SiC, especially n-type, it has been observed that introducing a NO gas anneal after the standard dry O_2 oxidation process significantly reduces the interface trap density, increases mobility, and raises oxide reliability and performance.[1,76,77,78] The mechanism by which this anneal proceeds and how it affects the transition region at the SiO_2/SiC interface is not clear, but a possible explanations is that at around 1100~1120°C the NO gas molecules break up into N atoms and O atoms. The N atoms at the interface then chemically react and fill some of the dangling bonds and also bond with the excess C atoms and C clusters[75], hence decreasing the number of interface traps. However, it has certainly been widely observed that this anneal successfully reduces D_{IT} by an order of magnitude close to the E_C, increases channel mobility from less than 10 $cm^2/V\cdot s$ to 35~40 $cm^2/V\cdot s$, and improves the interface quality, making this an essential step for most current 4H-SiC MOS device fabrication processes.[1,75,76]

4.3.2 Nitrogen Profile from Standard NO Anneal

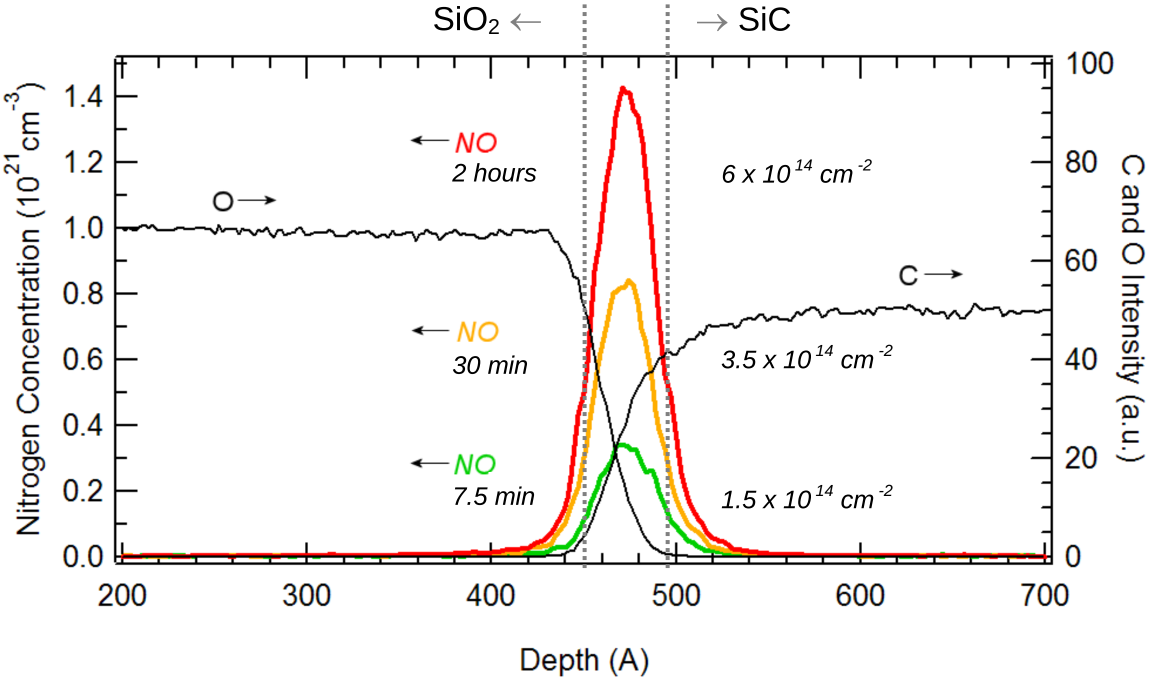


Figure 4.3.1 SIMS profile of nitrogen concentration at the SiO_2/SiC interface after an NO anneal with different annealing time.[79]

The nitrogen concentration inside the oxide after the NO anneal can be detected in various ways and there are many reports in the literature. For example, Figure 4.3.1 shows the SIMS profile of the nitrogen concentration at the SiO_2/SiC interface after an NO anneal at 1175°C with different annealing time reported by J.Rozen.[79] From this plot it is obvious that most of the nitrogen has accumulated at the SiO_2/SiC interface. Note that this plot only includes the part of the oxide layer that lay near the interface, while at the oxide surface there was a further accumulation of nitrogen not shown in this plot. The figure also indicates that the total nitrogen concentration at the interface varied according to the annealing time.

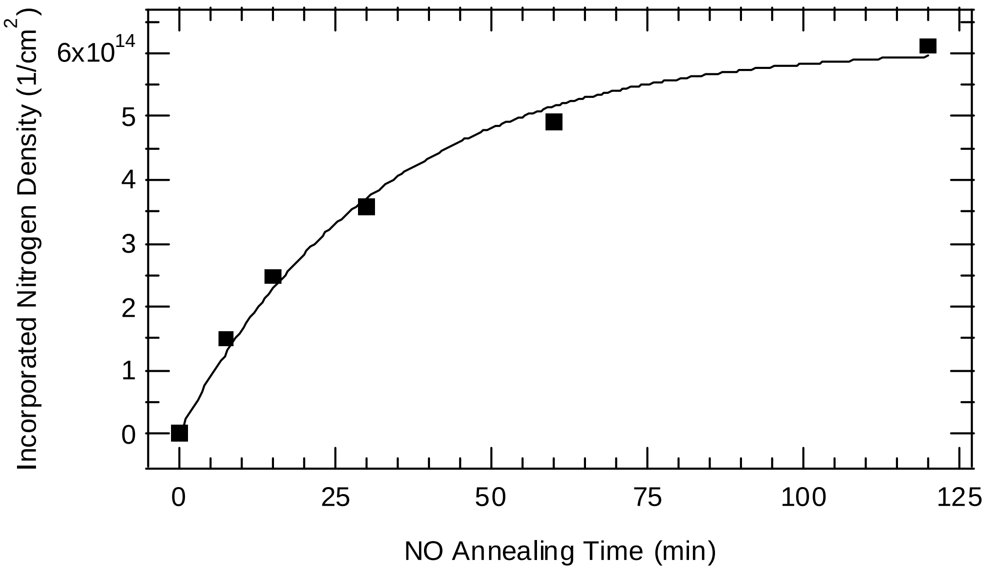


Figure 4.3.2 Nitrogen concentration at the SiO_2/SiC interface vs. annealing time of the NO anneal (reported by Rozen).[80]

This trend is also demonstrated in Figure 4.3.2, which plots the nitrogen concentration at the SiO_2/SiC interface vs. annealing time of the NO anneal reported by J.Rozen[80]. This plot shows the good fit between the experimental results and the exponential equation and reveals that the total concentration of Nitrogen at the interface saturates at $\sim 6\times10^{14}$ /cm^2 for an annealing time of 2 hours.

In the work reported here, for the NO anneal similar 5×5 mm samples were oxidized through the standard dry O_2 oxidation process described previously after which they were loaded into the furnace in an Ar atmosphere and heated to 1175°C. Once the desired temperature was reached, NO was flowed into the furnace at 577 sccm for 2 hours and then the furnace was again flushed with Ar to terminate the annealing while cooling down to 900°C. The samples were then processed into MOS capacitors using the same process as that used in the previous section, and measured using the simultaneous high-low C-V station at both room temperature and 300 °C.

4.3.3 Electrical Characteristics Following Standard NO Anneal

4.3.3.1 C-V Measurements and D_{IT} of MOS Capacitors

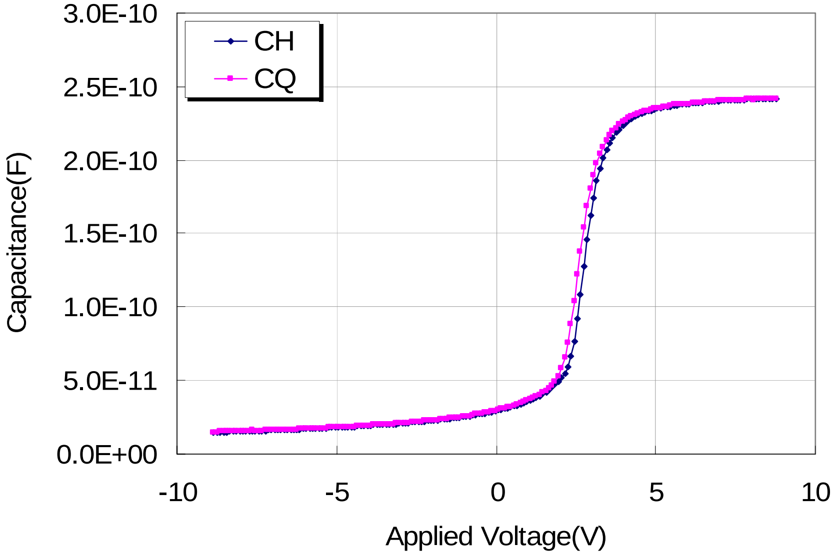


Figure 4.3.3 Room-temperature (23°C) C-V curve for an n-type 4H-SiC MOS capacitor with oxide grown by standard O_2 oxidation followed by standard NO anneal.

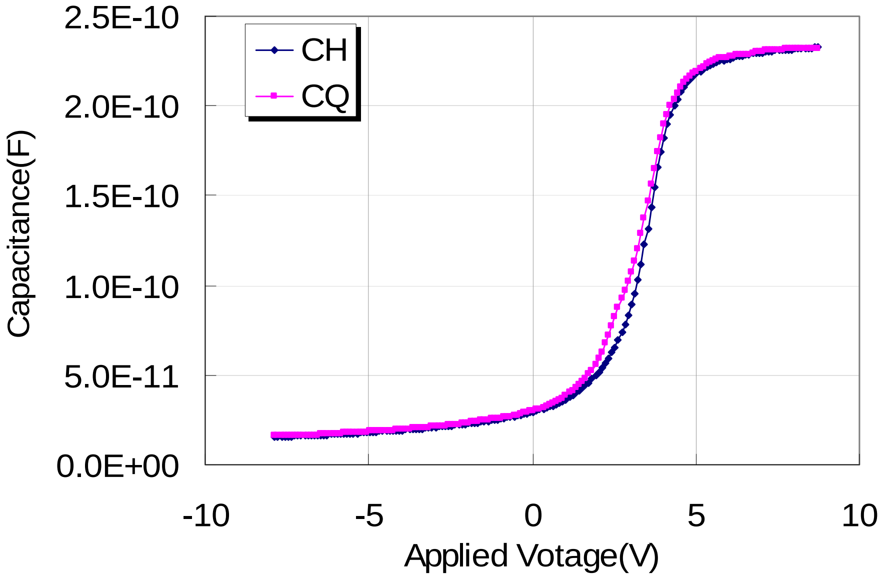


Figure 4.3.4 High-temperature (300°C) C-V curve for an n-type 4H-SiC MOS capacitor with oxide grown by standard O_2 oxidation followed by standard NO anneal.

Figure 4.3.3 & Figure 4.3.4 shows the room-temperature and high-temperature (300^{o}C) C-V curves for a MOS capacitor using n-type 4H-SiC. As in the previous section, CH represents the adjusted high frequency (100KHz for 23^{o}C and 1MHz for 300^{o}C) capacitance curve, and CQ represents the adjusted quasi-static capacitance curve. This sample also had 300 um diameter contacts and the thickness extracted from the C-V curve was around 36 nm, with V_{FB} at 2.93V. Once again, compared with similar samples with oxide grown by standard dry O_2 oxidation such as the previous example, the V_{FB} was usually about 1V smaller and the Q_{eff} calculated from the V_{FB} was about 1~2E-7 *C/cm²*, which is typically a smaller negative number compared with standard dry O_2 oxidation, Recall that:

$$Q_{eff} = [Q_F + Q_M\gamma_M + Q_{IT}(\phi_S)] \quad \text{.. (Eq 2.2.12c)}$$

where the fixed charge term Q_F is usually a positive number and the interface trap charges Q_{IT} is usually a negative number. Because of the deep bandgap in SiC, there is as yet no method that can measure these two terms separately. However, the significant reduction in D_{IT} as well as the decreased Q_{eff} is a good indication of the actual decrease in the number of interface traps and hence the interface trap charges. This also implies that the Q_F term changes little after the annealing. As mentioned earlier, the reduction in D_{IT} is advantageous, although the lower V_{FB} of the MOS capacitor, along with a lower threshold voltage V_T of the MOSFET using the same oxide as gate insulator, causes problems for devices that need to be able to sustain a larger field before turning on.

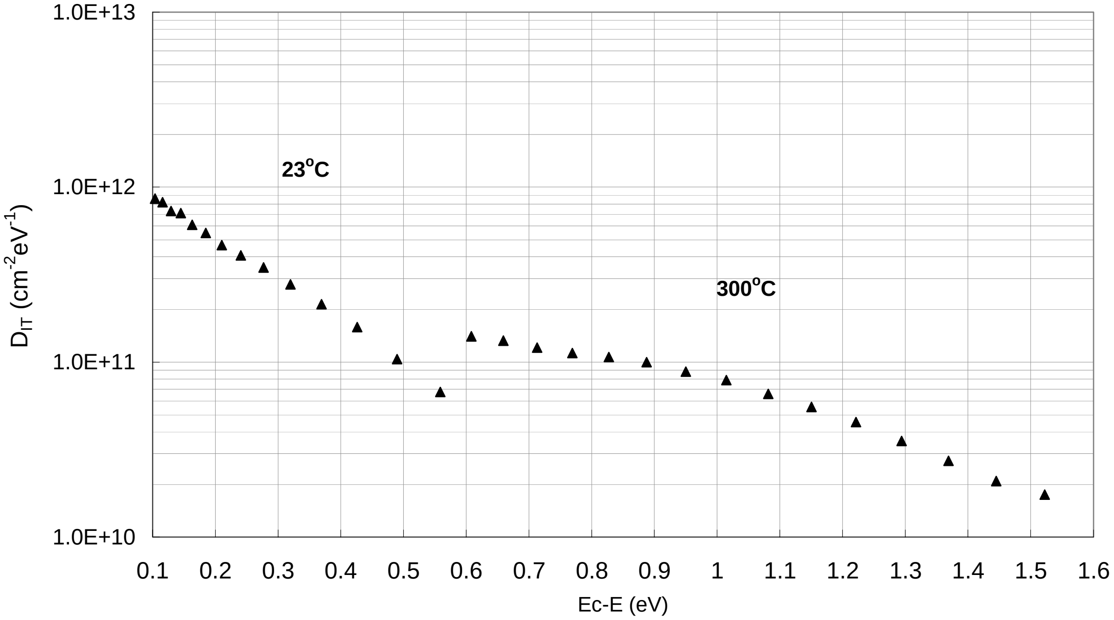


Figure 4.3.5 Density of Interface-Traps (D_{IT}) extracted from C-V curve in Figure 4.3.3 & Figure 4.3.4.

Figure 4.3.5 shows the D_{IT} of an n-type 4H-SiC MOS capacitor with oxide grown by dry O_2 oxidation followed by the standard NO anneal. As for the previous dry O_2 oxidation sample, this was extracted from both the room-temperature measurement (0.1eV~0.6eV below Ec) and high-temperature (300°C) measurement (0.6eV~1.6eV). As shown in the figure, there was a significant decrease in the trap density both near the interface and deeper below the conduction band. Typical measured values of the D_{IT} of samples annealed by NO at 1175 °C for 2 hours were about 1.0E+12 $cm^{-2}eV^{-1}$ at 0.1eV below E_C,[1,76,77] which is almost an order of magnitude smaller than the D_{IT} of the standard dry O_2 sample discussed above. It has been reported that this effect has also been observed on the deposited oxide,[81] which reduces the D_{IT} to a similar value and indicates that approximately same number of interface traps are present near the Ec after the anneal. Deeper into the band gap, this anneal also efficiently reduces the D_{IT} by a factor of 2~3 compared with the D_{IT} of the standard O_2 oxidation sample, with the number of traps generally being below 1.0E+11 $cm^{-2}eV^{-1}$.

It is worth noting that there have been reports that D_{IT} value also changes according to the different N concentration at the interface by varying the annealing time of the NO anneal.[80] This effect is especially obvious for traps near the E_C, while those traps that are located deeper in the gap are passivated much faster. As indicated by Figure 4.3.6 and Figure 4.3.7, which is the D_{IT} of each N concentration value at different NO annealing time from Figure 4.3.1, both at 0.1eV and 0.6 eV, the lowest D_{IT} were achieved for a 2 hour NO anneal. Both curves also saturated at this point.

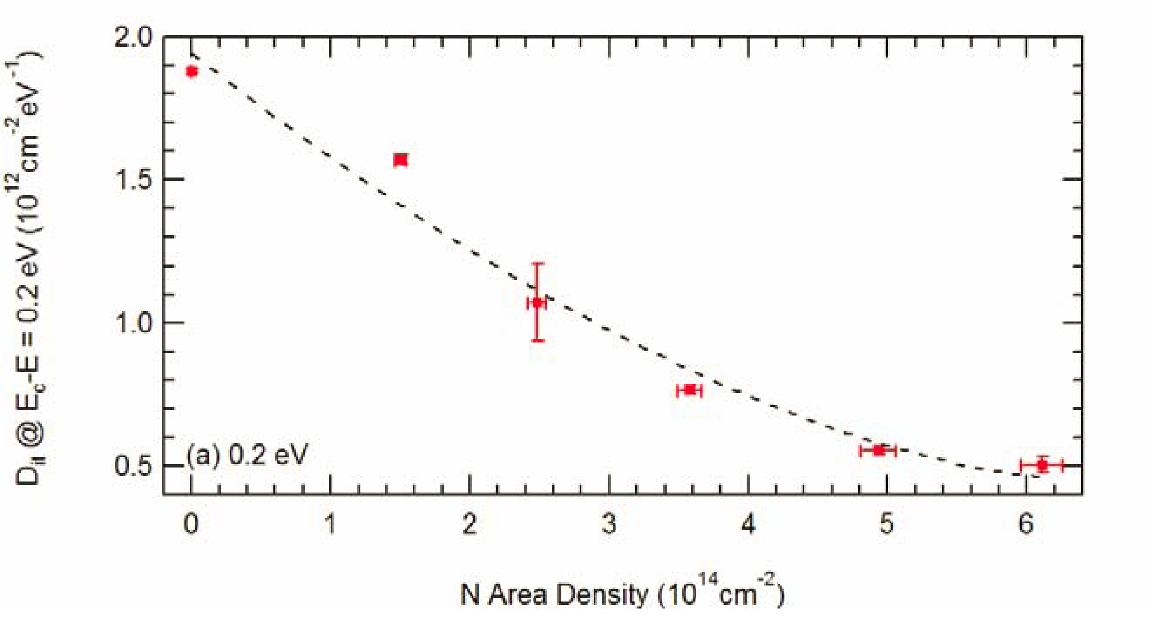


Figure 4.3.6 D_{IT} at 0.2eV below E_C of different N concentrations at the interface by varying NO annealing time (reported by Rozen).[80]

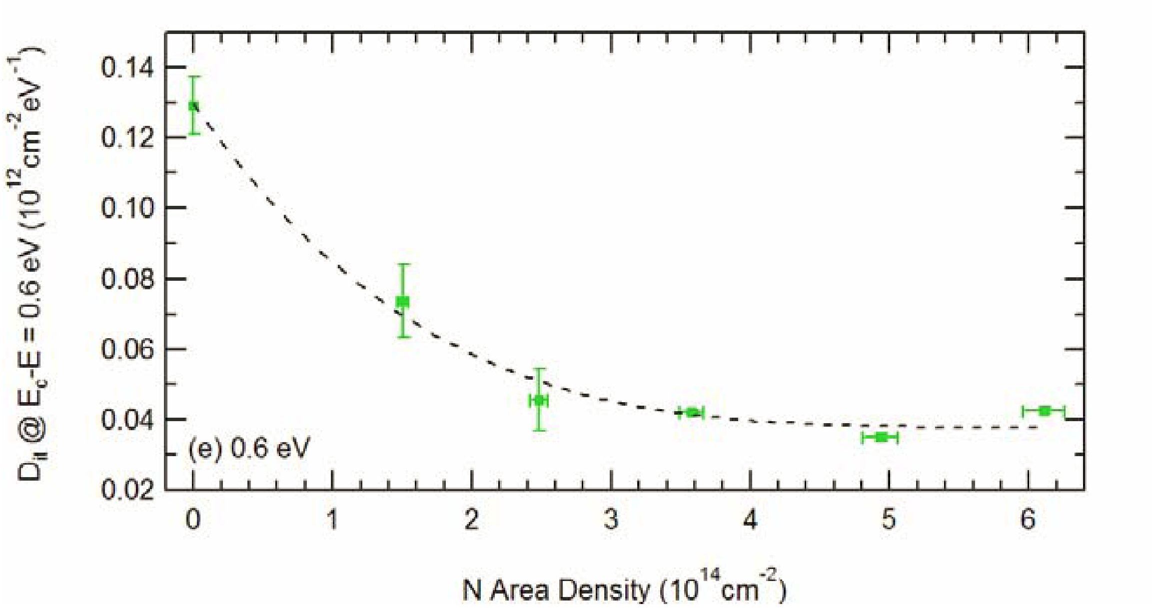


Figure 4.3.7 D_{IT} at 0.6eV below E_C of different N concentrations at the interface by varying NO annealing time (reported by Rozen).[80]

4.3.3.2 V_T and Channel Mobility for N-channel MOSFETs

This large reduction in the number of interface traps directly links to a significant increase of the channel mobility. To examine this issue, N-channel 4H-SiC lateral MOSFETs were made according to the process in Appendix B. The gate oxide was grown on the 10*um* thick 5×10^{15} cm^{-2} p-epi material by the standard dry oxidation process followed by the standard NO anneal at 1175°C for 2 hours. Ni was deposited and annealed at 870°C as the contact on a highly doped source and drain, after which Molybdenum was evaporated on as the gate metal.

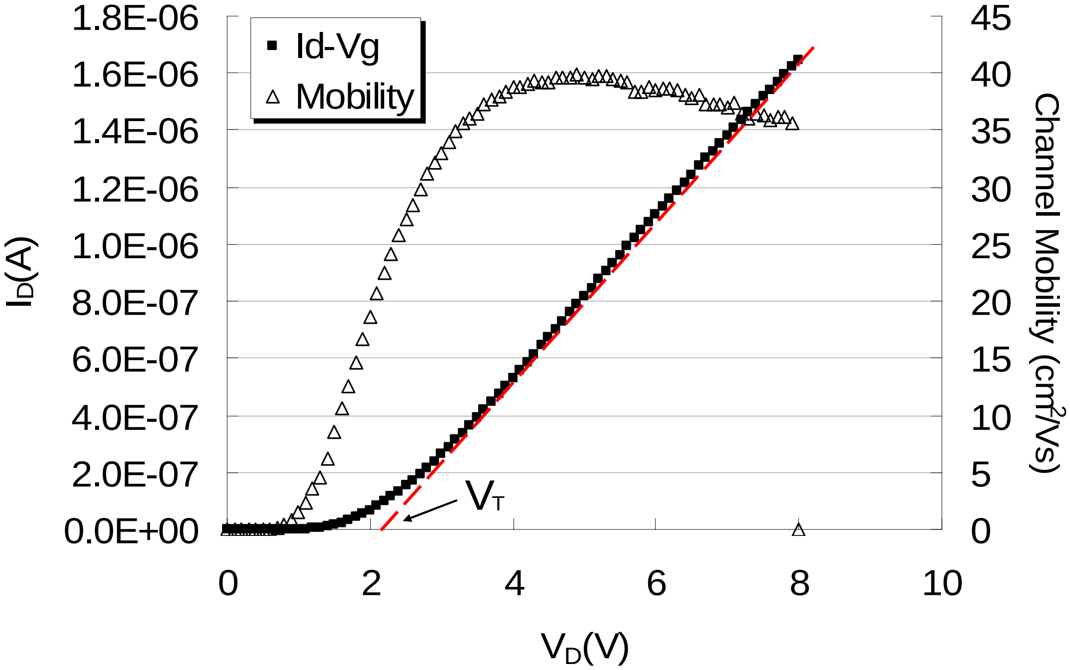


Figure 4.3.8 Channel mobility μ of n-channel MOSFET with gate oxide grown under standard dry O_2 oxidation followed by standard NO anneal.

Figure 4.3.8 shows the I_D-V_G curve measured at room temperature of the MOSFET described above and the field-effect channel mobility extracted from it using the linear relation Eq 2.3.8. The typical measured peak value of the mobility was around 35~40 $cm^2/V{\cdot}s$, which agrees with the widely reported value for n-channel 4H-SiC MOSFETs with NO annealed gate oxide.[1,76,77,78] This is significantly higher than the values for the standard dry O_2 oxide, which are usually less than 10 $cm^2/V{\cdot}s$. The reason for this increase is still under debate, but it has been suggested that it is partly because of the reduction in the number of interface traps caused by the standard NO anneal and possibly also some change of structure and smoothing of the SiO_2/SiC interface. As for the threshold voltage, V_T, is about 2.3V for this example, comparable to a typical V_T of 2~3V for a gate oxide thickness of around 50 nm. For this thickness, V_T is relatively smaller than the typical V_T value for a standard dry O_2 oxide MOSFET by 1~2V, which may be due to the reduction in the trap charges mentioned earlier.

4.3.3.3 I-V Characteristics and Breakdown Field

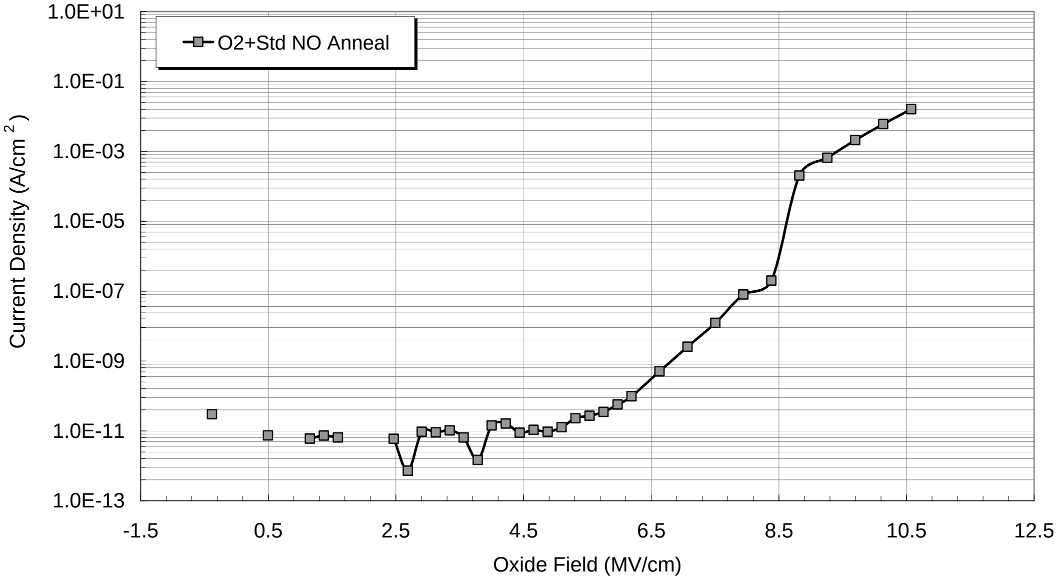


Figure 4.3.9 I-V characteristic for an MOS capacitor with oxide grown by standard O_2 followed by standard NO anneal.

The I-V characteristic of an oxide with standard dry O_2 followed by the standard NO anneal is shown in Figure 4.3.9. The value for the breakdown field for this type of oxide is typically ~8 MV/cm. As the previous section, details of the measurement and calculation of the field are provided in Section 3.8. Compared with the standard dry O_2 oxide mentioned previously, the breakdown field improves by about 2 MV/cm, which can easily translate into a gain of ~10V in gate bias for a 50*nm* thick oxide, and this difference can be even greater for a thicker gate oxide. The breakdown field of an oxide with the standard NO anneal is the best known so far, which is one of the main reasons that most currently available high-voltage power MOS devices now use this type of gate oxide. Although the precise mechanism is still unknown, the I-V results indicate the possibility that NO may chemically react with the oxide layer and thus change the electrical characteristics of the whole layer. A similar theory proposed by Maeyama, et al.[82] suggests that the dielectric constant of the oxide may be changed by the NO anneal, possibly explaining the improved breakdown field.

4.3.4 Summary for Standard NO Anneal

In conclusion, the NO annealing process results in a much lower D_{IT} for MOS capacitors and increased channel mobility for MOSFETs. This indicates a significant reduction in the number of interface traps and improved oxide reliability. Currently, almost every SiC related MOS devices developer uses this anneal as one of their standard fabrication steps. However, the devices suffer from an undesirably lower threshold voltage due to the reduction in the number of negatively charged traps at the interface. Further, even with a drastically increased channel mobility, the peak value is still only about 5% of the bulk mobility of n-type 4H-SiC, which is far from satisfactory compared with Si base devices that can achieve up to about half of its bulk mobility.

Furthermore, this method also suffers from several serious limitations. Firstly, the excess O atoms around the sample always tend to continuously grow additional layers of new oxide at the interface while annealing. An increase of oxide thickness can always be observed after the standard NO anneal used for the work reported here, with a growth rate of approximately 2 nm/hour. This may lead to thickness control problems in commercial device fabrication processes, although it did not pose a serious problem here as for the standard 2 hour anneal the thickness increase was consistently 2~4 nm. Also, during the additional oxidation, dangling bonds, free C clusters and other defects and traps were continuously being created even as the N atoms were attempting to passivate the surface. This competing effect inevitably limited the overall effectiveness of the passivation process, thus posing the question of whether the concentration of N atoms at the interface would be sufficient to passivate all the traps created during the additional oxidation in time? This issue can be answered by nitrogen plasma anneal, which will be discussed later in this work.

Secondly, another disadvantage of this annealing method is that while it reduces the number of interface traps, which are usually negatively charged for n-type semiconductors as discussed in Section 2.2.4.3, it also reduces the total interface charges

Q_{IT} to a less negative number. Assuming all the other charges remain unchanged, Eq 2.2.12b and 2.3.2a become:

$$V_{FB(real)} = \phi_{MS} - \frac{1}{C_O}[Q_F + Q_M \gamma_M + Q_{IT}(\phi_S)] = \phi_{MS} - \frac{1}{C_O}[Q_{eff}] \ldots\ldots\ldots\ldots \text{(Eq 2.2.12b)}$$

$$V_T = V_{FB} + 2\phi_F + \frac{K_S X_O}{K_O}\sqrt{\frac{4qN_a(\varphi_F)}{K_S \varepsilon_O}} \quad \text{(n-channel MOSFET)}\ldots\ldots\ldots\ldots \text{(Eq 2.3.2a)}$$

This change will result in a shift of V_{FB} and V_T towards the negative direction. This effect has been confirmed by experimental observation, with a comparatively smaller V_{FB} and V_T being observed for similar MOS devices that have the gate oxide but with and without NO anneal. Using ICS (refer to Section 3.7 and Appendix C), the Q_{eff} calculated from the measured V_{FB} of the C-V characteristic of a MOS capacitor with an NO anneal also gives a smaller number compared with a standard dry O_2 device. For practical device designs, this effect corresponds to a smaller turn on voltage for the MOSFET devices, which is very undesirable for high-voltage application MOS power devices. Other Nitric based compound such as N_2O and NH_3 have been tested with similar results, and the best results are still achieved by NO under similar conditions.[77]

4.4 Hydrogen Passivation

4.4.1 General Introduction and Procedure for H_2 Anneal

Traditionally, in Si/SiO_2 interface, most of the interface traps can be related to Si dangling bond. And Hydrogen anneal is a well-known method which is very effective at passivating these traps, by forming Si-H bonds at the interface.[83,84,85] Hence, Hydrogen passivation techniques are widely used as the standard fabrication procedure in the Si industry. However, in case of SiC/SiO_2 interface, it is believed that the large amount of interface traps do not primarily originate from the silicon dangling bonds, while carbon clusters and other defects are suspected to be more dominant[41,86,87,103] Similar as the effect and role of N, the behavior of H on interface defects also lacks theoretical models and remains elusive so far.

Hydrogen passivation techniques have also been applied onto SiO_2/SiC interface.[100] As for the detailed process, it has been proved that directly introduce H_2 gas during the oxidation at moderate temperature does not show any measurable effect, similar as introducing N_2 directly. However, there are a few techniques can be applied in practice. One of the feasible methods is to use a metal layer, working as a catalyst, in order to crack H_2 into atomic H during anneal. Few metals such as Pt, Ni are known to have this effect. The standard annealing process used in Auburn is as follows: samples are prepared by standard dry O_2 oxidation initially, sometimes followed by a standard NO anneal. Pt is sputtered as gate metal prior to the annealing process. This step is essential for the effectiveness of the process. Afterward, samples are annealed in the quartz furnace with pure H_2 flowing at 500sccm for 1 hour at 500°C. Then, backside oxide is removed and samples are prepared into MOS capacitors for electrical characterization.

4.4.2 Electrical Characterizations of Standard H_2 Anneal

4.4.2.1 C-V Measurements and D_{IT} for MOS Capacitors

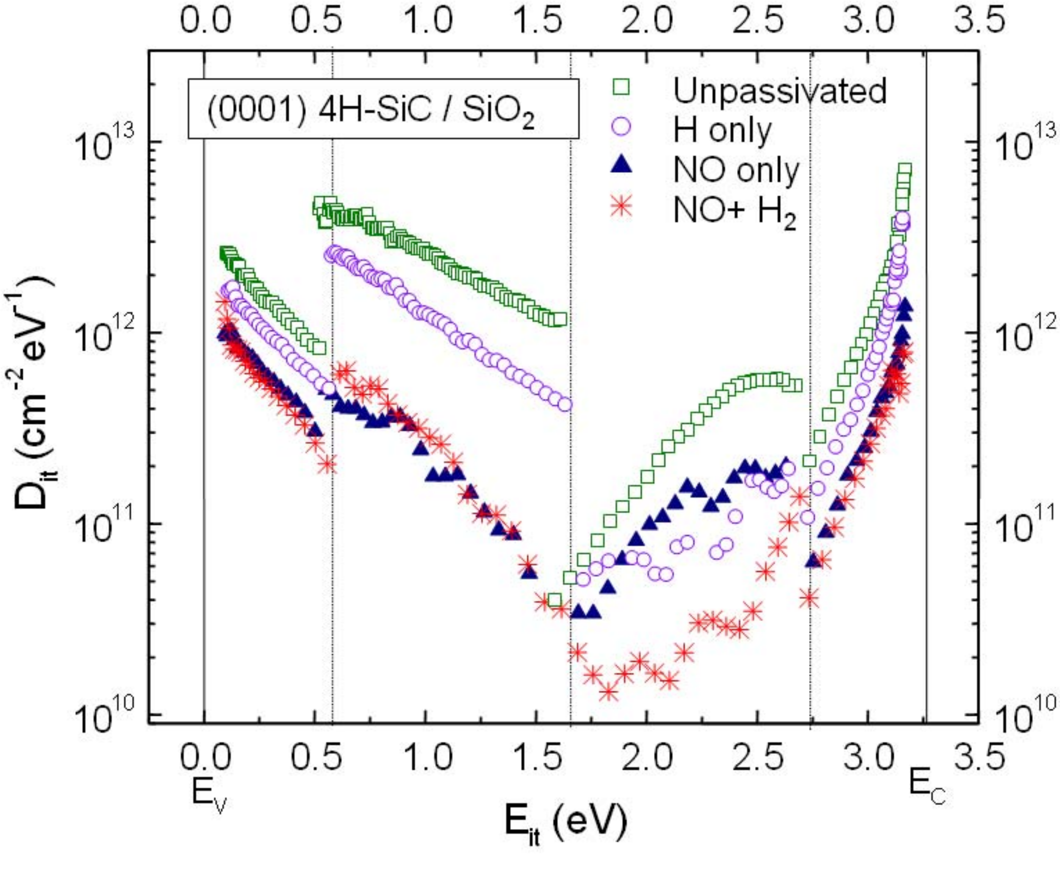


Figure 4.4.1 The D_{IT} of 4H-SiC MOS capacitors with oxides after different passivations.

First of all, after the anneal, presence of H inside the oxide is confirmed by SIMS result,[88] with a peak distribution near the interface at the concentration of $\sim 2.5\times10^{14}cm^{-2}$. Note that D_2 is used instead of H_2 for better sensitivity.

As a comparison, full band-gap D_{IT} of 4H-SiC MOS capacitors with oxides after different types of passivation techniques are shown in Figure 4.4.1. They are characterized from room-temperature and high-temperature C-V from both n-type and p-type. Similar results were previously reported by [100]. Compared with the unpassivated as-oxidized sample, the sample with only H_2 anneal does not show significant decrease in D_{IT}, which is also an reinforcement of the fact that the Si dangling bond may not be the dominant contributor for the interface traps. NO anneal however, effectively reduces D_{IT} throughout the whole band-gap. And the last sample in the chart with NO anneal followed by the H_2 anneal with Pt gate leads to the best result. The D_{IT} indicates H_2 is capable of further reducing the D_{IT} significantly at deeper into the gap, especially at about 1.6eV~2.7eV above E_V (or 0.6eV~1.6eV below E_C), although it is not as effective at the rest of the band-gap. Similar as NO, the reduction of D_{IT}, translates into a reduction in Q_{IT}, and the measured V_{FB} also further shifts toward the negative direction. For an n-type MOS capacitor, the typical value for calculated total Q_{eff} is even positive.

4.4.2.2 V_T and Channel Mobility for N-channel MOSFETs

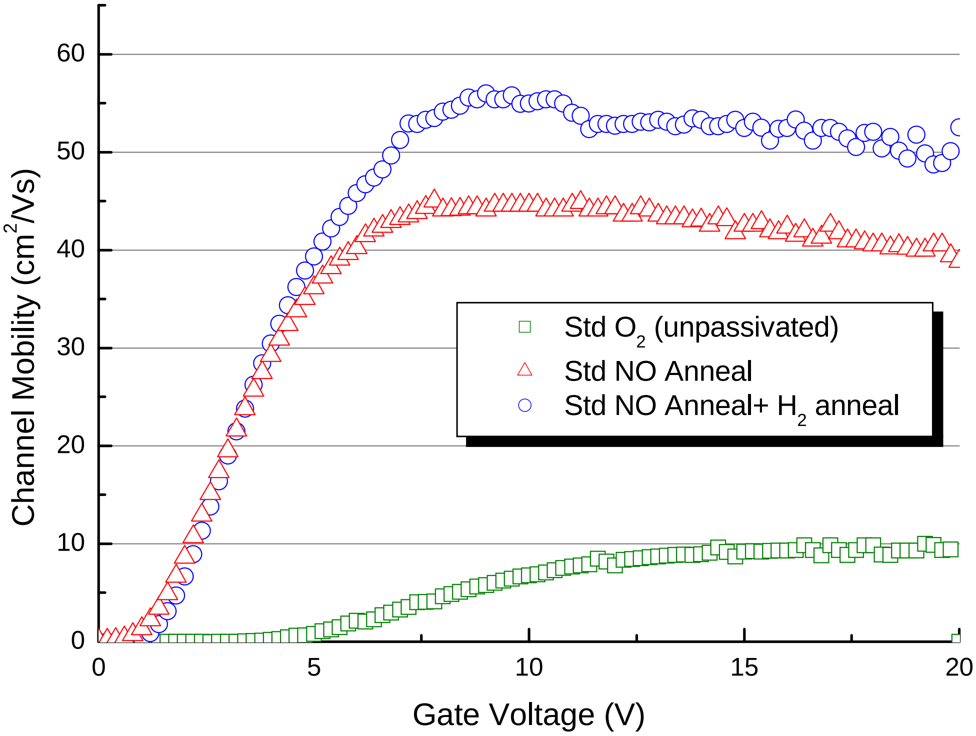


Figure 4.4.2 Channel mobility μ of 4H-SiC MOSFET with gate oxides after different passivations.

N-channel 4H-SiC lateral MOSFETs are made according the process in Appendix B, same as other samples. The gate oxides of few samples are grown on the 10*um* thick 5×10^{15} cm^{-2} p-epi materials with standard dry oxidation process followed by the standard NO. For comparison purpose, one sample is further annealed by the standard H_2 anneal process, with Pt deposited as gate contact prior to the annealing.

Figure 4.4.2 is the field-effect channel mobility of those MOSFETs extracted by the linear relation Eq 2.3.8. From the plot, it is very clear that the H_2 anneal after standard NO anneal results in a small increase in the peak mobility. The typical measured peak value of the mobility after this process is around 50 $cm^2/V \cdot s$, which accords with the observed reduction of the D_{IT} in the deeper region. As for the threshold voltage, V_T, typically is close to the value of standard NO anneal only, but usually a little smaller, which might possibly due to the further lowering of the trap charges as mentioned earlier.

4.4.2.3 I-V Characteristics and Breakdown Field

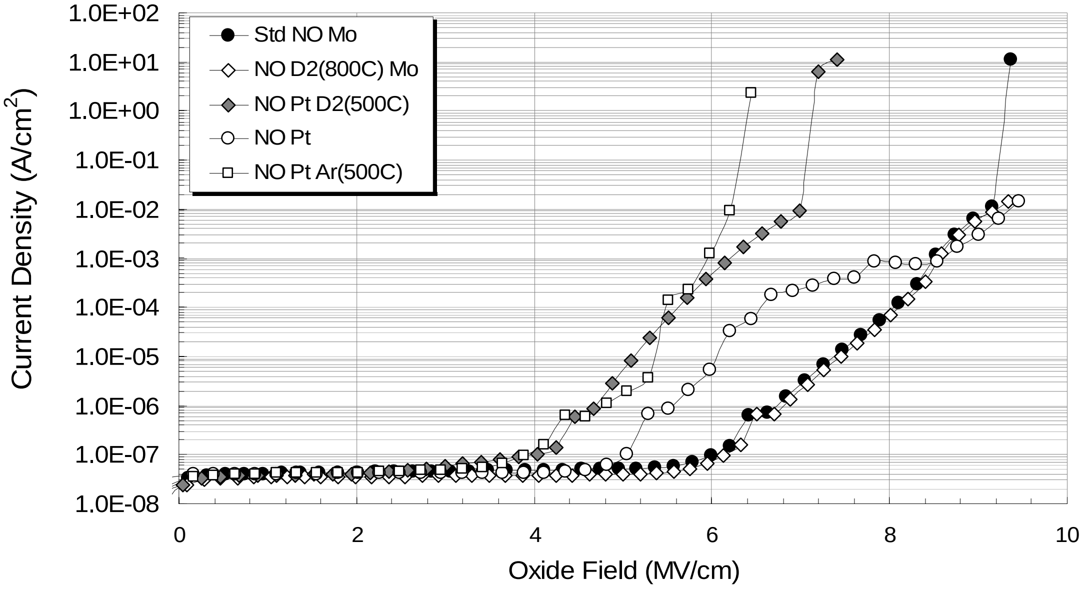


Figure 4.4.3 I-V characteristic for the MOS capacitor with oxide after different process.

The typical I-V characteristic and the breakdown field of the oxide after this process is surprisingly lowered by ~2 MV/cm. This significant reduction in the breakdown field is suspected to be caused by H during anneal. A series of samples each with a different process is tested in order to find out the actual cause: 1) Standard NO anneal with Mo gate; 2) Standard H_2 anneal (D_2 is used instead) with Mo gate; 3) Standard NO anneal with the Pt deposited followed by the H_2 anneal; 4) Standard NO anneal only with the Pt deposited; 5) Standard NO anneal with the Pt deposited followed by annealing in Ar at 500^{o}C. As indicated by Figure 4.4.3, two samples with Mo gate do not show any decrease in their breakdown field, while with the Pt deposition, a noticeable reduction in the breakdown field is observed regardless of the presence of H. And the last sample which used Ar instead of H_2 to mimic all the rest of the conditions results in the same breakdown field. Therefore, these results indicate that the reduction in the breakdown field is most possibly due to the damage caused by Pt deposition. Besides, Pt is very easy to peel off from the surface during post deposition processes such as lift off, causing more difficulties during fabrication. Also, using Pt gate during fabrication in mass production can be very expensive. Currently, other techniques are applied for hydrogen anneal in industry, such as atomic hydrogen anneal[89,90] and wet re-oxidation.[91,92] The former process introduces atomic hydrogen radicals by following H_2 through catalyzer at high temperature prior to the anneal, while the latter process mainly introduces water-vapor into re-oxidation by burning H_2 with O_2 inside the furnace. For both processes, similar results as H_2 anneal with Pt with improved breakdown field are observed.

4.4.3 Summary for Standard H_2 Anneal

In summary, H_2 anneal is proven to be capable of further improving the D_{IT} after NO, especially at deeper energy levels. Hence, this results in a small increase of the peak channel mobility to ~ 50 $cm^2/V\cdot s$. Also, a smalle decrease in the breakdown field is seen however it is later proved that this is mostly caused by the Pt depositing instead of H_2 anneal. This could be improved by using alternative H anneal methods such as wet re-oxidation. As a matter of fact, H anneal is now a standard process in the industry, and most of the current SiC MOS power devices are fabricated using NO anneal followed by H passivation. However, similar to NO anneal, an increase and better controllability in threshold voltage V_T is required. In addition, in order to surpass and replace Si based devices in some field, further improvement of the mobility and other device performance is still necessary to meet the demanding standard.

CHAPTER 5

Alumina Enhanced Oxidation (AEO) Process

5.1 General Introduction

Alumina enhanced oxidation was first reported around 2003 by researchers at Chalmers University,[59] who found that introducing metallic impurities through placing sintered alumina into the furnace during oxidation resulted in an oxide with lower D_{IT} and higher channel mobility.[2,59] This process has since attracted a great deal of attention and been intensively studied worldwide. The main characteristics of this process are that it provides a fast growth rate, significantly low interface trap density and increased peak channel mobility. However, it also introduces a huge mobile ion concentration throughout the oxide layer, which makes it unusable for device fabrication. This issue was therefore addressed in the work reported here.

Different types of alumina were used during the oxidation process initially in this work. Although some of the alumina samples exhibited none of these effects, the ceramic alumina pieces supplied by International Ceramic Engineering (ICE) clearly showed all the effects mentioned above. Interestingly, the listed contaminants in these samples included several metal oxides, including MgO, CaO, Fe_2O_3, Cr_2O_3.[93] This and the large mobile ion content indicates that the observed characteristics may all be due to the impurities contained in the alumina rather than the alumina itself. This is widely supported by other reports.[2,94,95] Based on these preliminary findings, all the alumina enhanced oxidation discussed in this chapter used this type of ceramic alumina.

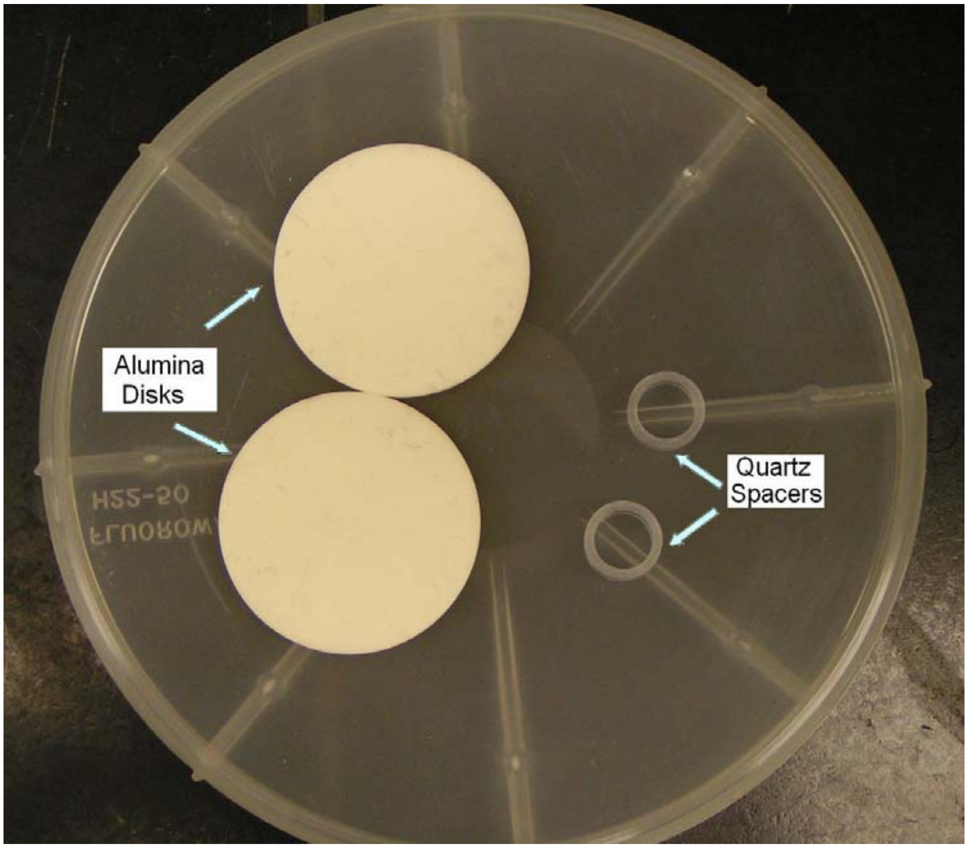


Figure 5.1.1 Ceramic alumina disks and quartz spacers used for the alumina enhanced oxidation.

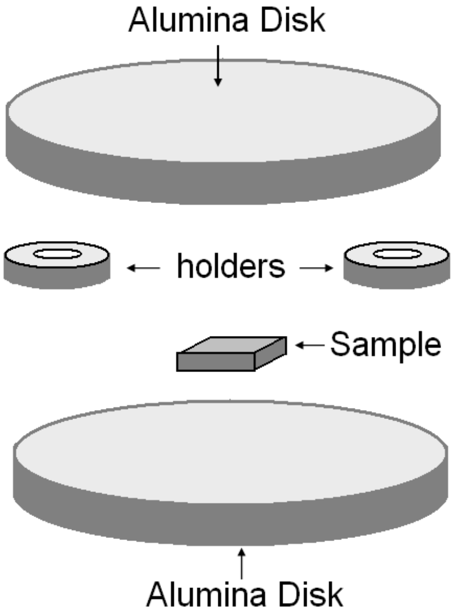


Figure 5.1.2 Diagram of the sandwich-like set up for alumina enhanced oxidation.

Figure 5.1.1 is a photograph of the two actual ceramic alumina disks and spacers used for the oxidation. These alumina disks have a diameter of approximately 1.5 inches and weigh about 10.5 grams. Two small alumina washers were used as spacers initially, but were later replaced by quartz spacers the same shape, as shown in the photograph. Figure 5.1.2 shows a diagram of the set up for the alumina enhanced oxidation. Here, two alumina disks were stacked separated by two spacers, with the samples sandwiched between them and sitting on the bottom disk. The stack was then loaded into a quartz furnace filled with Ar and the sample oxidized for 20~30 minutes in O_2 flowing at 500 sccm at 1150^{o}C, followed by Ar for 30 min at the same temperature to flush the residual

O_2 and terminate the oxidation before cooling to 900°C and removing the samples. The samples were then made into MOS capacitors using the same process described in previous sections.

5.2 Characteristics of Oxides Following Alumina Enhanced Oxidation

8° off, 11.1um of 5.01E+15cm^{-2} N epi on N^{-}, 0001 face 4H-SiC samples were used for this experiment. After oxidation, a 300 *μm* diameter circular pattern was used for photolithography, and Mo sputtered as the gate oxidation, then the backside oxide removed by wet BOE etching, and silver paint used for the back contact.

5.2.1 Growth Rate

The first non-traditional property of this oxidation process is its significantly fast growth rate. The thickness of oxide was extracted from the accumulation capacitance as the oxide capacitance from the C-V curve. It is well known that for Si-face 4H-SiC, the oxidation rate is typically very slow. However, in an alumina environment this rate increases to about 8~10 times higher than that normally seen under the same conditions. Table 5.2.1 shows the average growth rate under different conditions.

Table 5.2.1 Average growth rate for different oxidation conditions on Si-face 4H-SiC.

Process	Dry	NO	Alumina*	Alumina*
Temperature	1150^{o}C	1175 ^{o}C	1150 ^{o}C	1050 ^{o}C
Avg.growth rate	8nm/hour	2nm/hour	210~270nm/hour	50~80nm/hour

*: Due to wide variations in the concentration of impurities in the alumina, the growth rate varies considerably for different alumina pieces.

It is believed that this fast growth rate is mainly caused by the metal impurities inside the alumina, which may catalyze the oxidation process.[94] Although several metal impurities appear to have a similar effect on the growth rate, ceramic alumina itself seems to have little effect. As mentioned previously, this effect was strongly visible in the contaminated alumina selected for use in this experiment, and was much less evident in some of the other alumina samples tested.

5.2.2 C-V Characteristics and Interface Trap Density (D_{IT})

The high growth rate that is one of the main effects of this process is of little importance for the fabrication and quality of the oxide layer. The Interface Trap Density, on the other hand, is one of the most important parameters and directly determines the quality and performance of the device. It is also a critical factor that limits the value of inversion channel mobility. Although the physical mechanism is still uncertain, a significant decrease in the D_{IT} is observed after this type of oxidation process, which may relate to the effect of the impurities inside the alumna. [59,94~96]

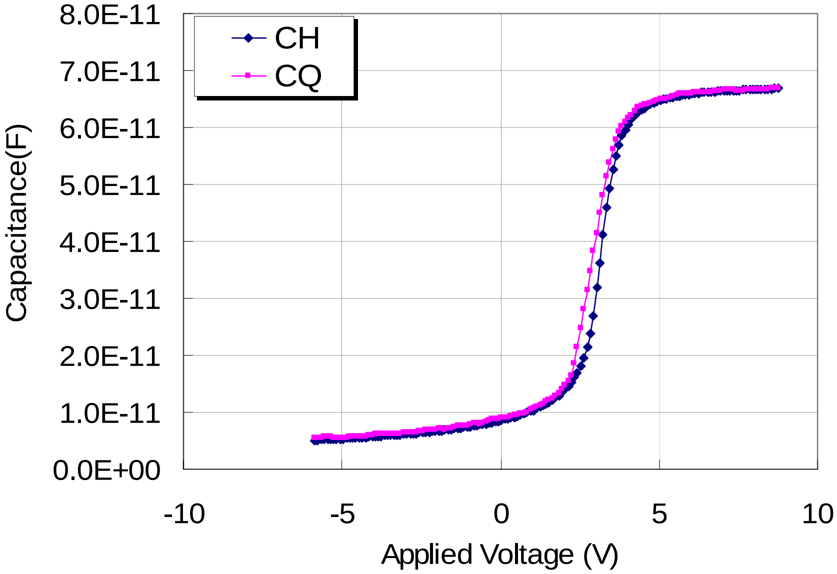


Figure 5.2.1 Room-temperature (23°C) C-V curve for an n-type 4H-SiC MOS capacitor with oxide grown in the alumina environment.

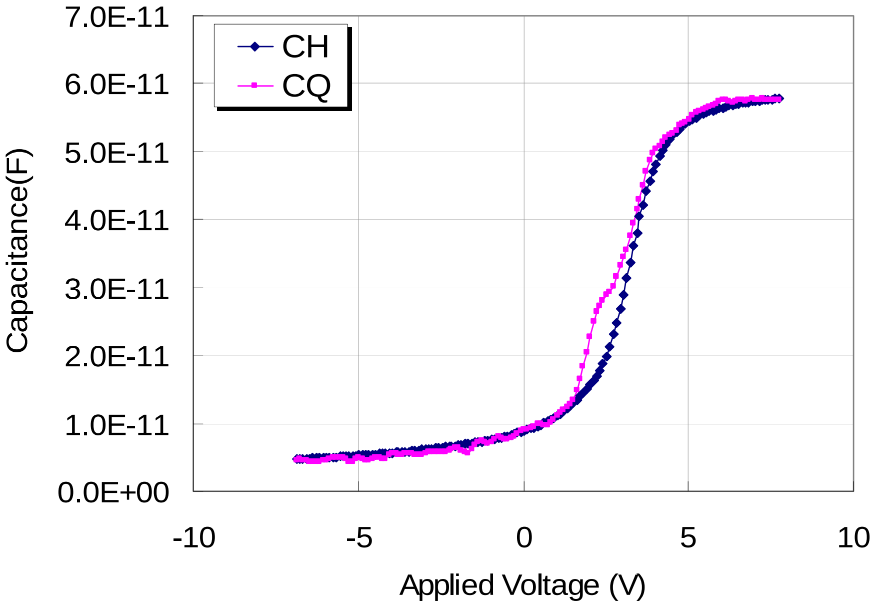


Figure 5.2.2 High-temperature (300°C) C-V curve for an n-type 4H-SiC MOS capacitor with oxide grown in the alumina environment.

Figure 5.2.1 & Figure 5.2.2 shows the room-temperature and high-temperature (300^{o}C) C-V curves for MOS capacitors obtained using alumina enhanced oxidation. As before, CH represents the adjusted high-frequency (100 KHz for 23^{o}C and 1 MHz for 300^{o}C) capacitance curve, and CQ represents the adjusted quasi-static capacitance curve. The oxide thickness extracted from the C-V curve was around 36 nm, with V_{FB} at ~3V. However, due to the huge number of mobile ions inside the oxide, the V_{FB} produced by this process varied continuously, so the total effective charge Q_{eff} calculated from this process was unpredictable. As a result, the parameters for MOS devices fabricated by this process suffered from considerable uncertainty and poor controllability.

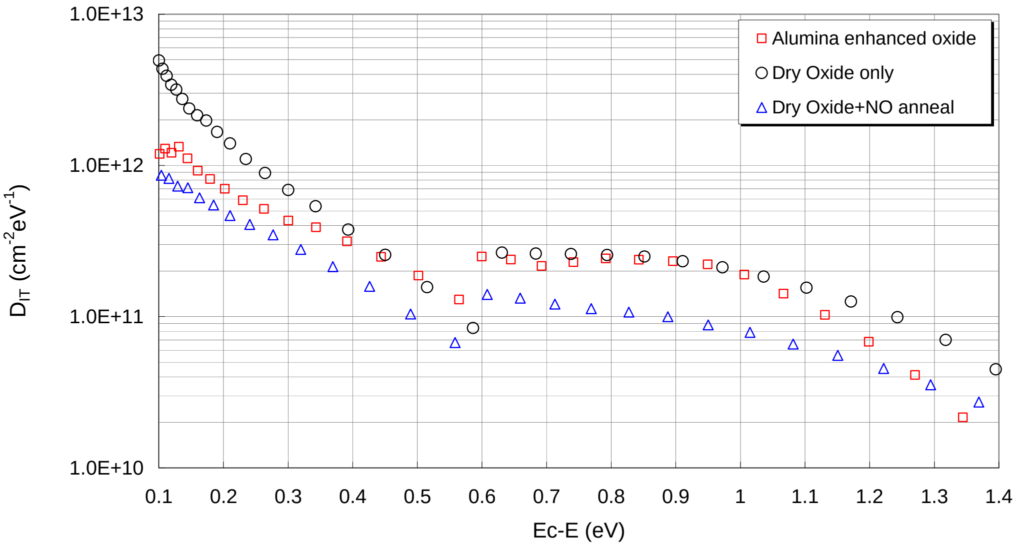


Figure 5.2.3 Density of Interface-Traps (D_{IT}) extracted from C-V curve in Figure 5.2.1 & Figure 5.2.2.

Extracting D_{IT} from the C-V curves, as before, the alumina enhanced oxidation process efficiently lowered D_{IT} throughout the band gap. It was most effective near the conduction band, as shown in Figure 5.2.3, with a typical D_{IT} of 0.1eV below E_C at about 1.0E+12 $cm^{-2}eV^{-1}$, close to the value for samples with a standard NO anneal. However, the passivating effect on D_{IT} of this process appeared to weaken deeper into the band gap. The D_{IT} value of 0.6eV~1.6eV extracted from the high-temperature C-V measurement indicates that although a reduction was observed, this value was still close to the D_{IT} of a standard dry O_2 sample. This may indicate that this process is not able to reduce most traps at deep energy levels closed to the mid-gap. Also worth noting is that although the huge number of mobile ions inevitably led to unpredictable variation in many parameters, they appeared to have little effect on the D_{IT} values. The measured D_{IT} values of samples fabricated by this process were very consistent and agreed with the values reported by other researchers worldwide.[2,94~97]

5.2.3 BTS Measurement and Mobile Ion Concentration

In order to estimate the quantity of mobile ions introduced by the alumina enhanced oxidation process, samples were measured using the Bias-Temperature Stressing (BTS) method, a popular way to determine mobile ion concentration. Details concerning this method are provided in Section 2.2.4.

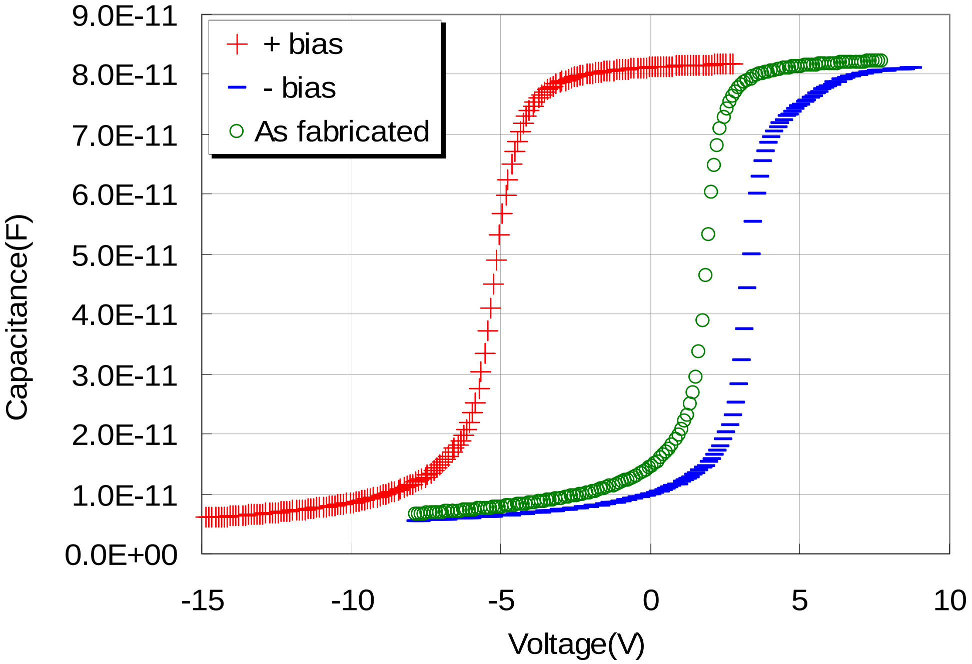


Figure 5.2.4 BTS result for an n-type 4H-SiC MOS capacitor with oxide grown by alumina enhance oxidation process.

The BTS result for an oxide grown by this process is shown in Figure 5.2.4. Here, an n-type 4H-SiC sample was oxidized using the alumina enhanced oxidation process. The oxide thickness on the resulting sample was about 30 nm. Molybdenum was used as the gate contact. For the BTS measurement, the sample was heated to 250^{o}C and a gate bias of ±1.5 MV/cm applied for 10 minutes. The sample was cooled under bias and the low-high frequency C-V curve measured as soon as it reached room-temperature. The resulting plot yielded a shift in the flat-band voltage ΔV_{FB} of ~8.4V, according to Eq 2.2.18b, which corresponds to a mobile ion concentration inside the oxide layer of 6.13×10^{12} cm^{-2} or 2.10×10^{18} cm^{-3}. Note that the total concentration of mobile ions varies with each sample, and the typical value of an oxide with similar thickness will be of the order of 10^{12} cm^{-2} to 10^{13} cm^{-2}, which agrees with the reported results.[2,94] Of particular importance for device manufacture, the concentration of these mobile ions can correspond to a voltage shift ranging from several volts to tens of volts, depending on the oxide thickness.

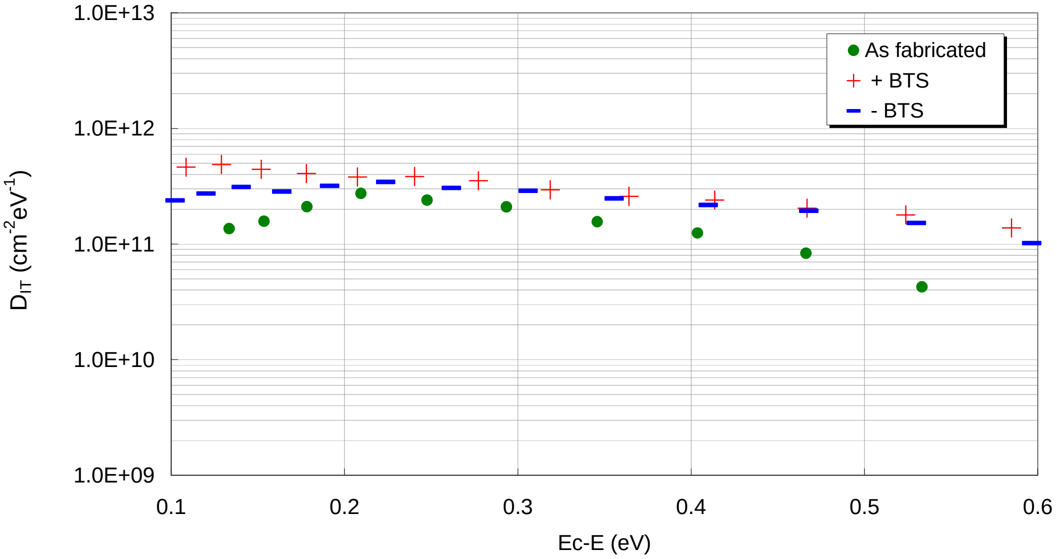


Figure 5.2.5 D_{IT} extracted from the BTS measurements in Figure 5.2.4.

Figure 5.2.5, shows that under +/- BTS conditions, although the mobile ions are moving inside the oxide layer and causing the flat-band voltage to shift, D_{IT} varies only slightly, suggesting that the mobile ions away from the interface have little effect on D_{IT}. This D_{IT} behavior conflicts with the D_{IT} results obtained for HCl anneal and –BTS with wet-etching presented in later sections, which indicate that removing the mobile ions from the oxide increases D_{IT}. Whether the position of mobile ions inside the oxide affects D_{IT} is therefore still open to question.

5.2.4 Channel Mobility for N-channel MOSFETs

The effective inversion channel mobility of lateral MOSFETs with gate oxide grown by the alumina enhanced oxidation process is the main reason for the widespread interest in this process.

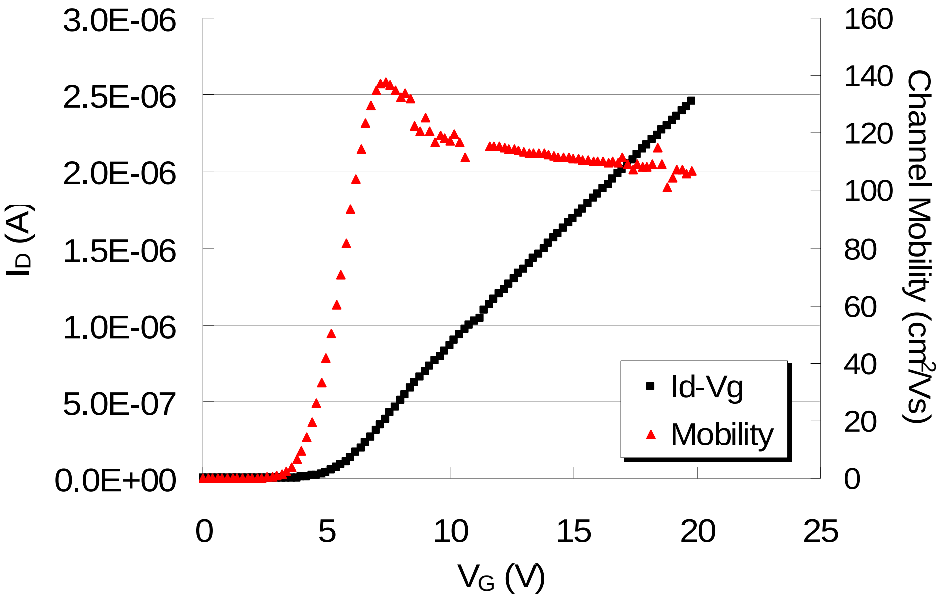


Figure 5.2.6 Channel mobility μ of n-channel MOSFET with gate oxide grown under alumina enhanced oxidation process.

As with the previous mobility results, the sample shown in Figure 5.2.6 was fabricated using the process described in Appendix B, with the gate oxide grown by alumina enhanced oxidation. Due to its fast oxidation rate, there is some difficulty controlling the oxide thickness, and the thickness of the gate oxide of this sample was around 112 nm. The peak mobility shown on the plot is more than 120 cm^2/V·s, while the typical mobility obtained for samples fabricated by this process was generally well above 100 cm^2/V·s. Note that this device has a relatively thick gate oxide layer; in devices fabricated using a similar method but with a relatively thin gate oxide layer, the mobility curve drops off very rapidly with increasing gate voltage, as demonstrated by other publications.[95,97] This result is very promising for applying into actual devices, although as yet there are few practical applications due to the instability caused by the mobile ions.

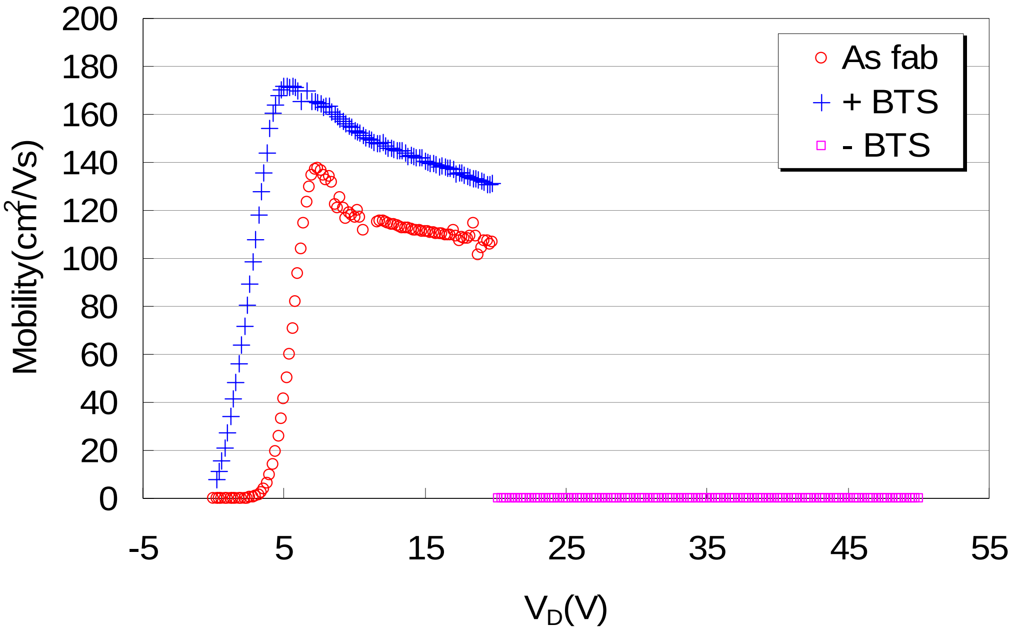


Figure 5.2.7 Channel mobility behavior after +/- BTS on the device from Figure 5.2.6.

As for the Bias-Temperature Stress (BTS) measurements on the MOS capacitors, measurement were conducted under the same conditions (250^{o}C, ±1.5MV/cm, 10 minute) for the MOSFET device shown in Figure 5.2.6, and the results are shown in Figure 5.2.7. As mentioned in the previous section, just as with the flat-band voltage shift the heavy mobile ion contamination shifts the threshold voltage V_T drastically under +/- BTS. For the mobility after +BTS, with the mobile ions mostly at the SiO_2/SiC interface, V_T shifts towards the negative direction and an increase in the peak mobility is seen. However, this increase in mobility occurs mainly near the low field region and is not obvious in the high field region, although this trend is not clearly shown on Figure 5.2.6 due to the relatively thick gate oxide layer. This behavior can also be seen in other MOSFETs with different types of gate oxides and mobile ion contaminants. Under –BTS on the other hand, with the mobile ions mostly near the metal/SiO_2 surface V_T shifts towards the positive direction and a decrease in mobility is usually seen. Unfortunately, in MOSFETs fabricated by this process the shift of the V_T is so great that it is impossible to turn on the device before the gate oxide breaks down. Similar mobility behaviors of devices made from this process have been confirmed by other researchers.[96, 97]

A possible explanation is that at low field, Coulomb scattering is the dominant effect limiting the mobility, so the positively charged mobile ions present at the interface neutralize the fields exerted by negatively charged interface traps and hence reduce the scattering of the inversion carriers in the channel. These positive ions may also induce more minority carriers in the channel, which will be electrons in the case of an n-channel device, further boosting the mobility. However, at higher field, the channel becomes much narrower and the physical roughness of the interface plus other effects become more dominant. Meanwhile, due to the fact that the mobile ions and traps are not at exactly the same location, when the electron gets closer the field cannot be completely shielded and will thus also scatter electrons.

As most 4H-SiC devices are targeting for high field / high temperature applications, this huge shift of V_T and instability under bias and temperature causes a serious problem for the application of this process in the fabrication of practical devices. To date, it is still not possible to remove all the mobile ions while preserving high mobility. Unless a satisfactory solution to this problem can be found, this process continues to languish, with few commercial applications.

5.2.5 I-V Characteristics and Breakdown Field

The breakdown field and I-V characteristic for an MOS capacitor with oxide grown by alumina enhanced oxidation is shown in Figure 5.2.8. For this particular sample, the oxide thickness was about 78 nm and the breakdown field in the region of 5.5 MV/cm. Repeating these measurements on samples oxidized by the same process but with different oxide thicknesses (35 nm~78 nm) indicated the typical breakdown field for this process to be around 5~6 MV/cm. Thus, samples fabricated using alumina enhanced oxidation show no improvement regarding the breakdown field compared with those made using standard dry O_2 oxidation. In conclusion, the mobile ion contamination may affect the interface trap density and channel mobility, and may even change the quality of the transition layer at the interface, but the I-V results indicate that unlike an NO anneal, this process is not likely to be able to change the properties of the entire oxide layer significantly.

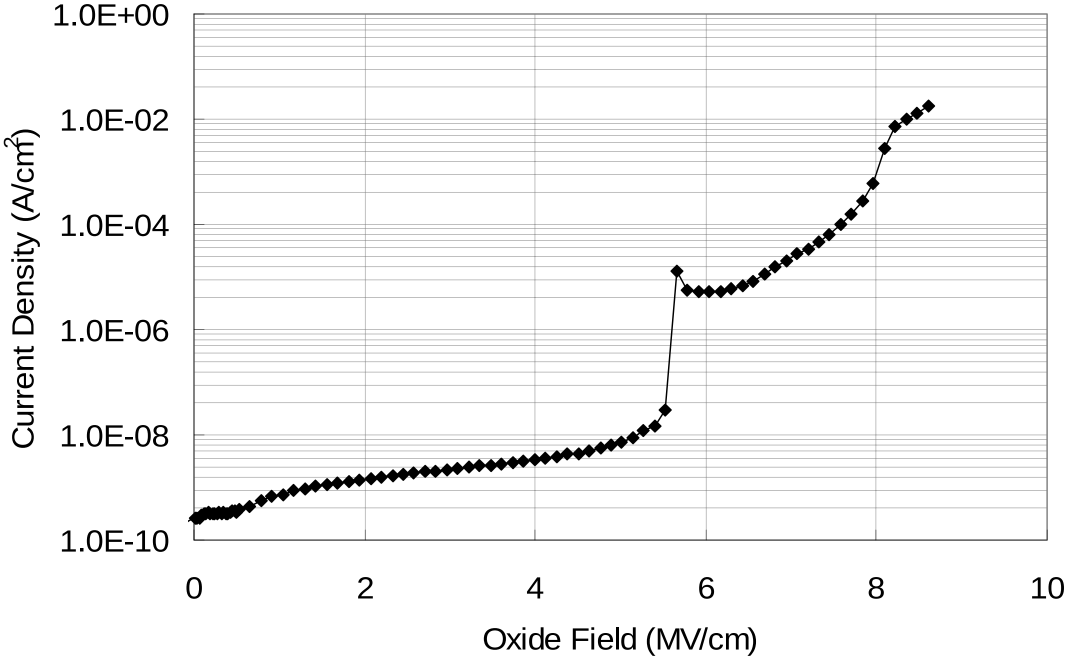


Figure 5.2.8 I-V characteristic for an MOS capacitor with oxide grown by alumina enhanced oxidation.

5.3 Oxidation with Intentional Metal Contamination

5.3.1 Introduction

Most fabrication procedures currently used to produce ceramic alumina are based on the Bayer Process, invented by Karl Josef Bayer in 1887.[98] This process mainly uses sodium hydroxide to dissolve and refine bauxite, a mineral typically containing 30-54% of alumina, Al_2O_3, with the rest being a mixture of silica, various iron oxides, and titanium dioxide. After the fabrication process, all the metal impurities inside the final product are likely to be in their oxide form and metal oxides such as MgO, CaO, Fe_2O_3, and K_2O are reported in chemical analysis sheet provided by ICE,[93] the producer of the ceramic alumina used in this work. Similar contamination in the ceramic alumina was also revealed by Rutherford backscattering (RBS), shown in Figure 5.3.1. Other researchers have reported that SIMS analysis confirms a high concentration of various metals inside the oxide using alumina enhanced oxidation.[94,97] In order to identify which of the contaminants are of interest for this study, the following experiments examined the effects of different impurities intentionally introduced during the oxidation process.

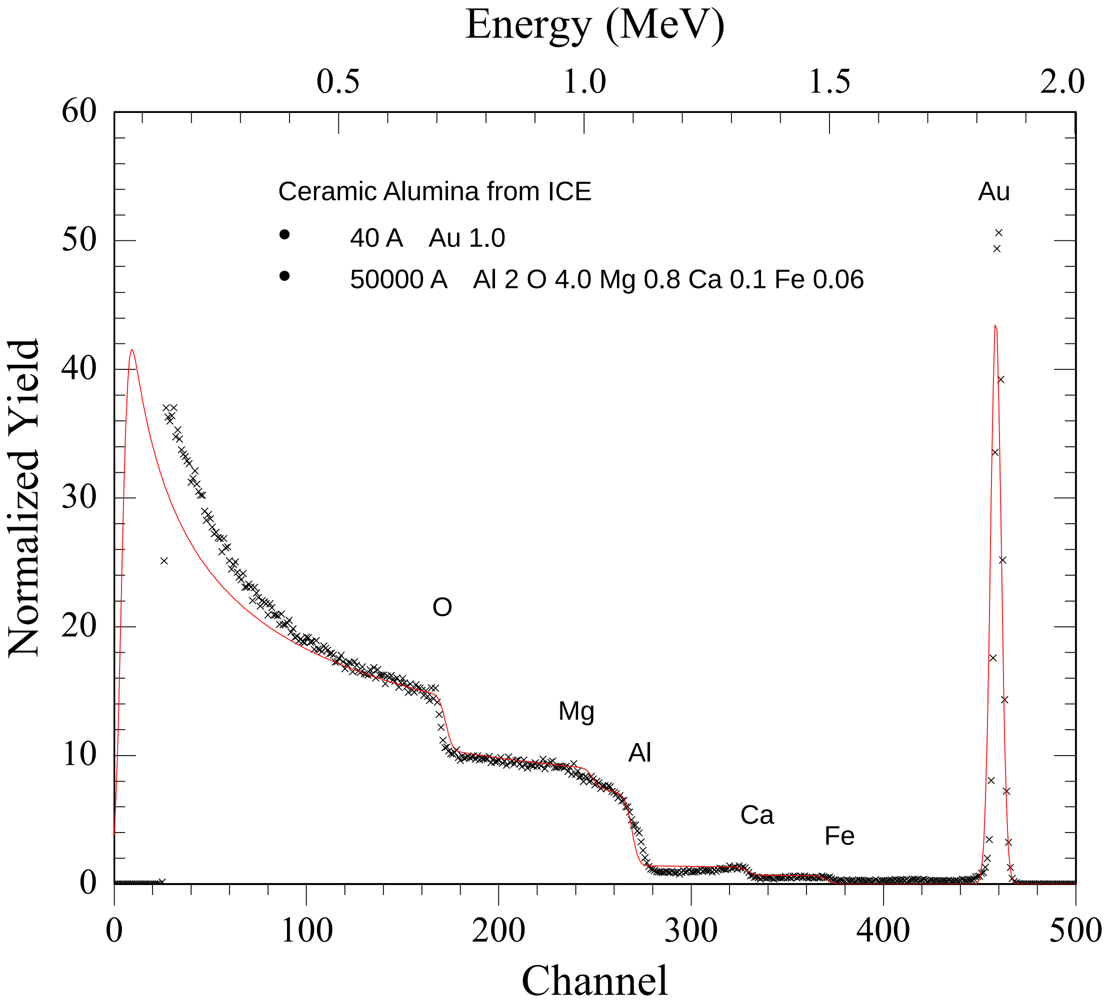


Figure 5.3.1 Rutherford backscattering (RBS) result for alumina used for this work.

5.3.2 Oxidation with Different Metal Oxide Compounds

5.3.2.1 Growth Rate

Three different metal oxides were tested for this research, namely MgO, CaO, and Fe_2O_3. For each, a small amount of the metal oxide powder was loaded into a quartz boat and the sample placed on top. The assembly was then loaded into a furnace and oxidized for 4 hours at 1150°C. Note that the amount of the impurity introduced into the oxide during oxidation was effectively random, as it is very difficult to control.

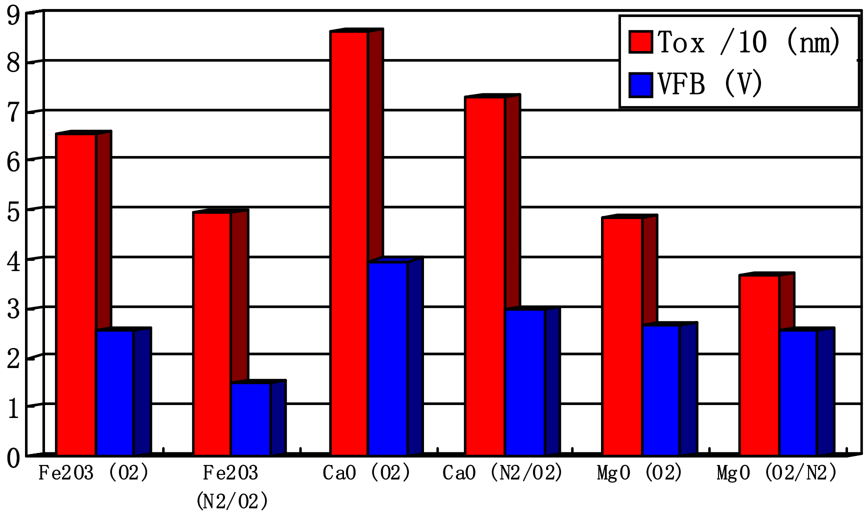


Figure 5.3.2 Comparison of T_{OX} and V_{FB} after oxidization with different metal oxides.

Figure 5.3.2 reveals that all of the metal oxides tested increased the oxidation rate, although it was noted earlier that high purity Al_2O_3 itself cannot. The V_{FB} as fabricated produced typical results, each according to its T_{OX}. Therefore, the rapid growth rate of the alumina enhanced oxidation could safely be ascribed to the presence of one or more metal oxide impurities inside the ceramic alumina.

5.3.2.2 Electrical Characteristics and Discussion

After oxidation with different metal oxide impurities, Figure 5.3.3 shows that the D_{IT} from all the samples was similar to that for the standard dry O_2 oxidation and no significant reduction due to alumina enhanced oxidation was seen. There were also no improvements in other electrical properties. There was, however, a reduction in both the yield and the breakdown field.

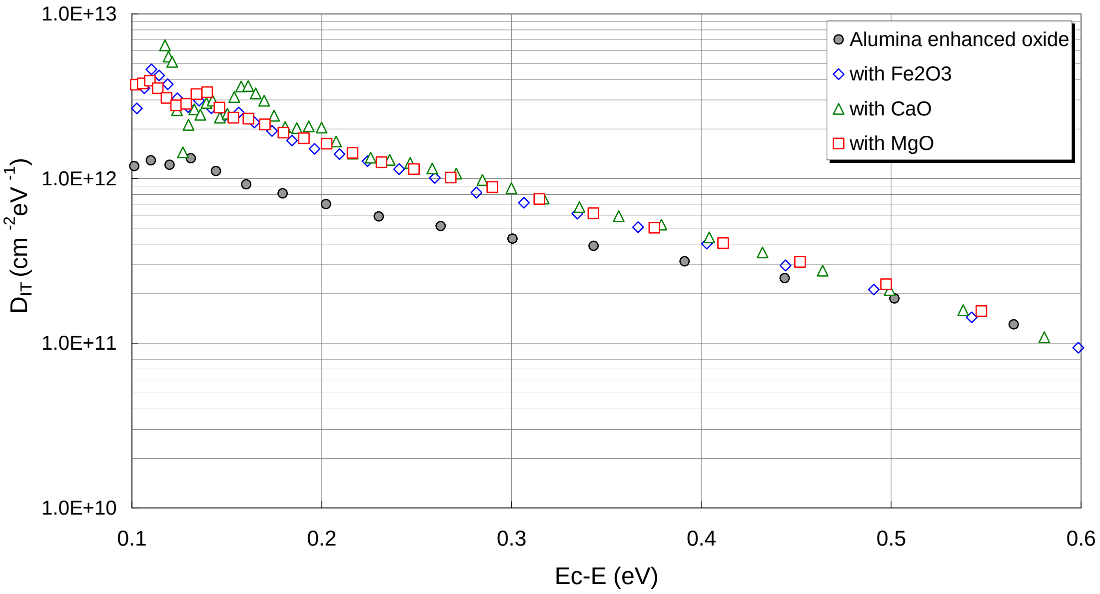


Figure 5.3.3 D_{IT} of sample oxidized in different metal oxide environments.

These results imply that either these metal oxides do not affect the electrical properties or the amount of the impurities introduced during oxidation is insufficient to show any distinct effect. However, as mentioned earlier, controlling the amount of impurities in the oxide is very hard in practice and some of the impurities were found to cause damage to the quartz furnace tube and paddle.

5.3.3 Oxidation with Alkali Metal Compounds

Historically, alkali metals such as Na and K have always been a very common contaminant in semiconductors due to their abundance in nature, and they were also present in the ceramic alumina used here. It has been reported recently by the group that first reported the efficacy of alumina enhanced oxide,[94] that intentionally introducing sodium into the oxide successfully produces a similar effect. The method they used to introduce Na was by boiling the sample with oxide in an NaCl solution before additional oxidation. This method was been widely used in Si-related research in the 1980s to study the effect of Na^+ on the oxides.[31,99]

Here, a similar method was used with different Alkali Chlorides, in this case NaCl and KCl. As mentioned earlier, the contaminants inside the ceramic alumina were mostly in the oxide form, so in order to mimic the alumina enhanced oxidation process an Alkali Oxide was also used, namely Na_2O_2.

5.3.3.1 Results with Alkali Metal Chlorides

Here, samples were pre-oxidized with a 4 hour standard O_2 oxidation. They were then boiled in the solution with various molar concentrations, after which they underwent a further oxidation in the quartz furnace. The results from the C-V measurements are shown in Figure 5.3.4, Figure 5.3.5 and Figure 5.3.6. Solution concentrations of 0.002 mol/L of NaCl and 0.05 mol/L of KCl were used for the results reported here, but other concentration were also tried and similar results were obtained.

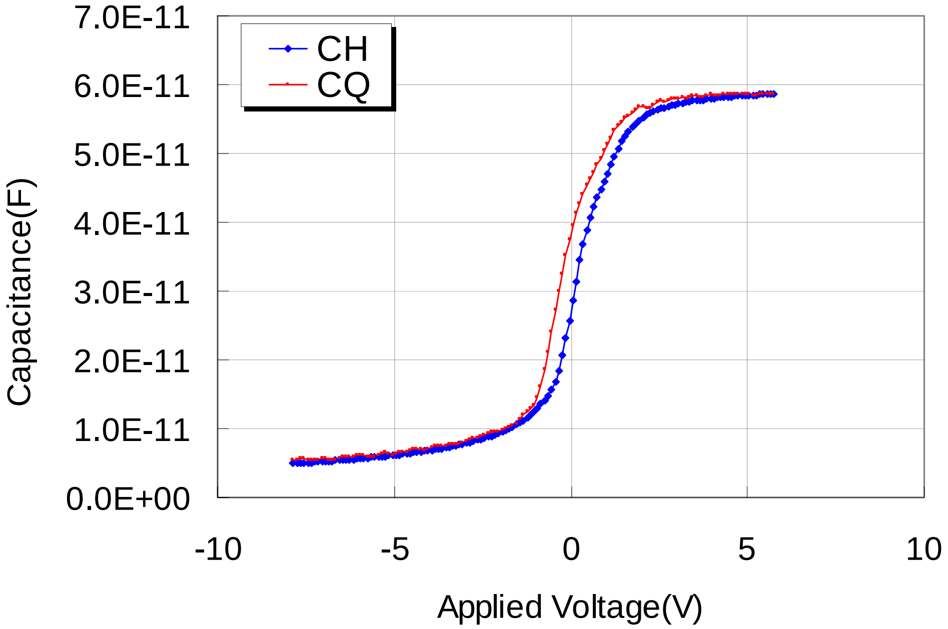


Figure 5.3.4 C-V curves for sample contaminated with NaCl.

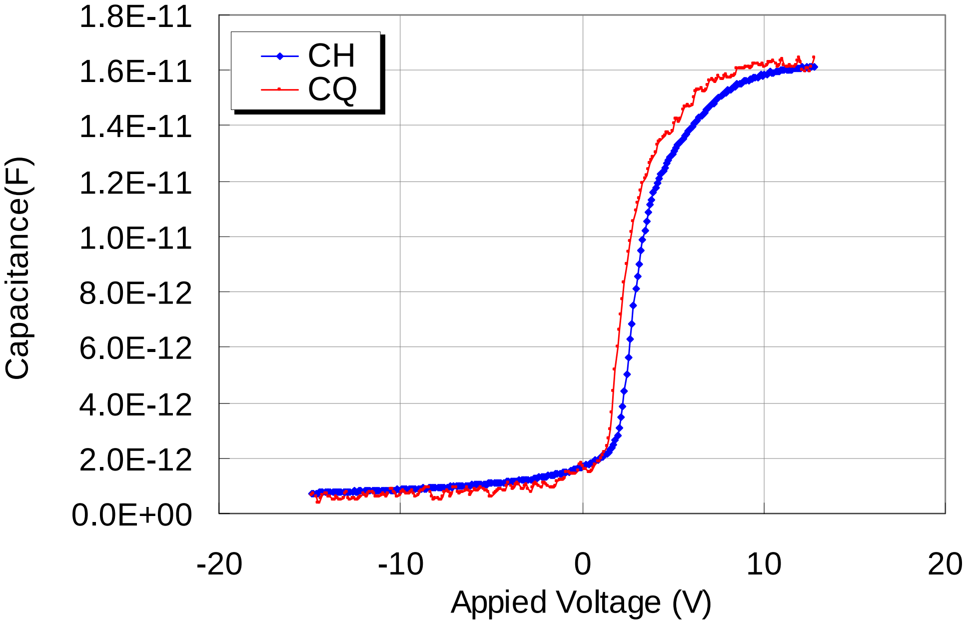


Figure 5.3.5 C-V curves for sample contaminated with KCl.

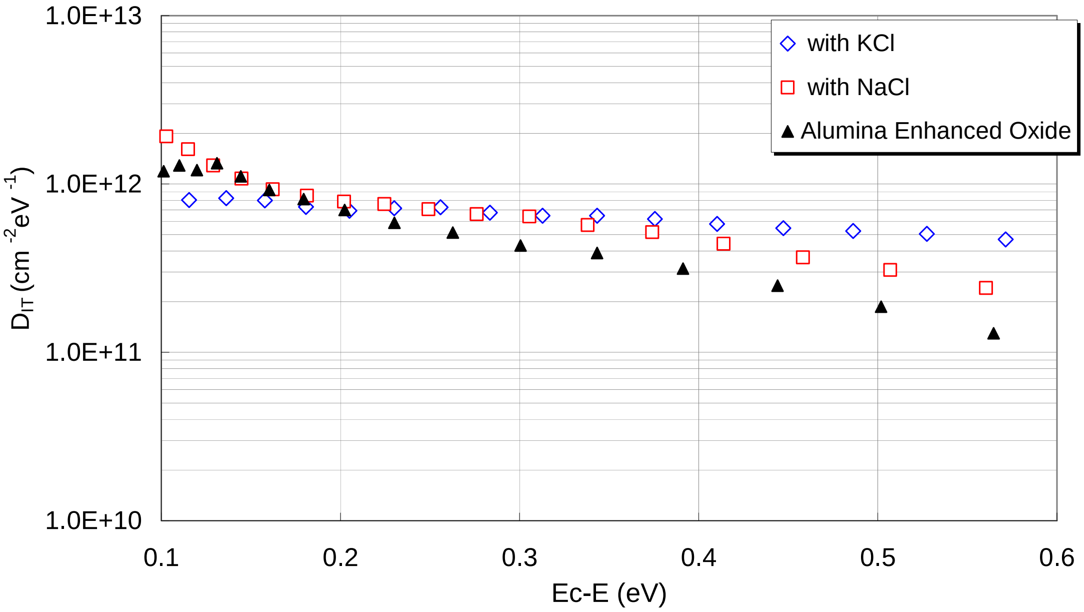


Figure 5.3.6 D_{IT} of samples contaminated by NaCl, KCl, and AEO for comparison.

The first noticeable result is that all the oxides after this experiment were very leaky, with poor device yields and breakdown fields. The reason for this result is still uncertain. As for the I-V characteristic, the V_{FB} of both devices were very small, indicating that positive charges were present at the interface. The BTS results for the sample contaminated with NaCl indicated a mobile ion concentration of $2.31\times10^{12}cm^{-2}$; unfortunately, the corresponding BTS for the sample contaminated with KCl could not be measured because the oxide was too weak to sustain the same bias and temperature conditions.

As for the D_{IT}, it is important to note that the D_{IT} values shown in Figure 5.3.6 are less accurate due to the following reasons: (1) a high leakage current was observed, and the quasi-static C-V was very shaky especially on the sample with KCl. The D_{IT} calculated will be affected by those errors. (2) For both samples, it was very hard to bias them into deep accumulation before oxide breakdown, so the D_{IT} close to E_C will be inaccurate, especially for 0.1eV~0.2eV below E_C. As a result, the D_{IT} from 0.2~0.6eV below E_C demonstrates a noticeable reduction, indicating these ions do have some effect in lowering the D_{IT}. However, the result is still not as substantial as for alumina enhanced oxidation, especially deeper into the bandgap.

5.3.3.2 Results with Na_2O_2

As for the other metal oxides, a small amount of the Na_2O_2 was loaded into a quartz boat and the sample placed on top. The whole assembly was then loaded into the furnace and oxidized for 10~20 minutes at 1150°C. Na_2O_2 is extremely chemically active, and the extremely fast growth rate observed meant that controlling the amount of Na_2O_2 and oxide thickness was very difficult. Na_2O_2 is also corrosive, aggressively reacting with the quartz furnace and boat and transforming them into Na-enriched glass. This not only contaminated the equipment, but also rendered them vulnerable to high temperature and pressure by changing their physical properties.

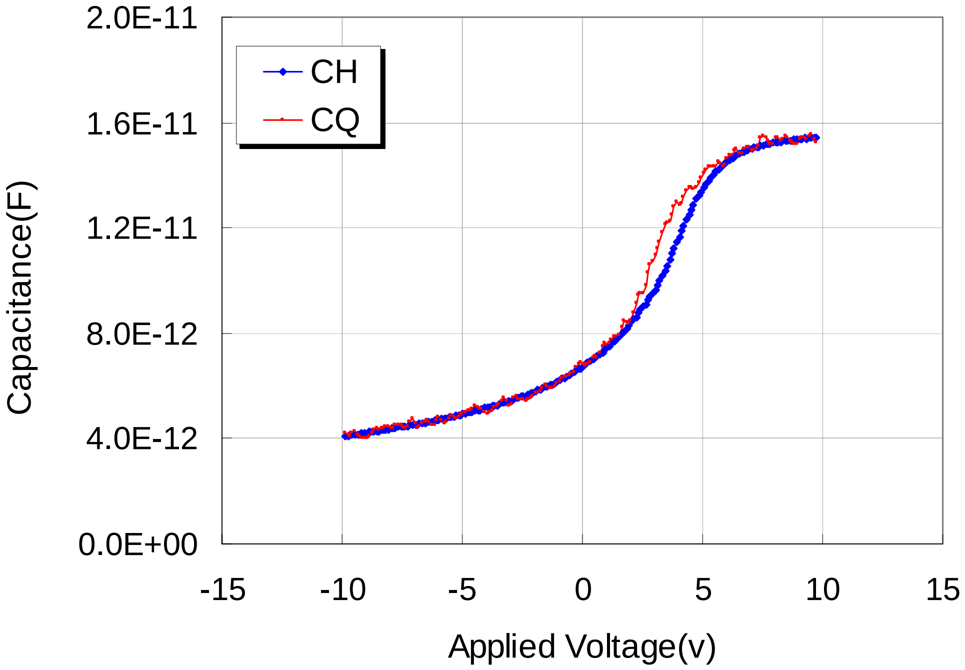


Figure 5.3.7 C-V curves of sample oxidized with Na_2O_2.

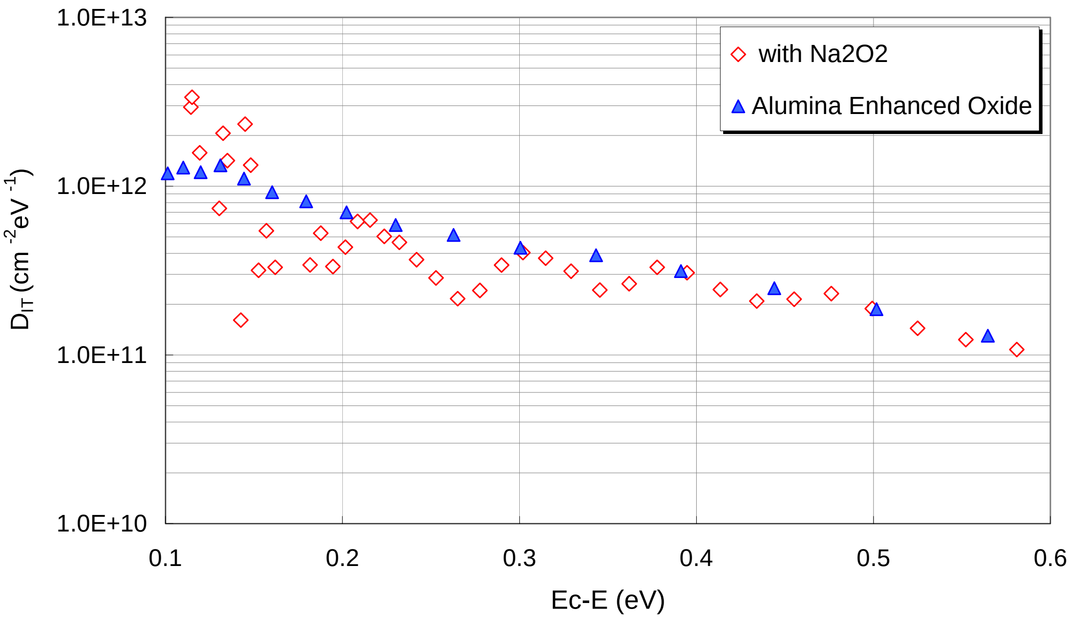


Figure 5.3.8 D_{IT} of sample oxidized with Na_2O_2 extracted from Figure 5.3.7.

The results from C-V measurements revealed that the device yield and breakdown field were both very poor. The oxide thickness was about 155nm because of the difficulty with thickness control, so the quasi-static curve was shaky due to the smaller capacitance and comparatively larger noise and leakage current. Similarly, the D_{IT} was very variable for the same reasons as for the previous results with NaCl and KCl. However, Figure 5.3.8 indicates a clear trend of reduction in D_{IT} similar to that seen for alumina enhanced oxidation. Unfortunately, the high-temperature C-V was also not measured due to the poor oxide quality.

5.3.4 Summary

Besides the experiments discussed above, several alternative methods were also tried, such as using less aggressive Alkali Hydroxides such as NaOH and KOH, implanting Na into the oxide and thermally driven-in toward the interface. However, no satisfactory results were obtained for any of these methods.

In summary, the presence of one or multiple types of metal oxides inside the alumina is likely to be primarily responsible for the fast growth rate, for example CaO, Fe_2O_3, and alkali oxides. A reducing trend in D_{IT} can be produced by introducing metal ions into the oxide, especially alkali metal ions such as Na^+ and K^+. However, the results are not sufficient to confirm that whether all the effects of alumina enhanced oxidation are entirely caused by the presence of Na^+ and K^+ at the interface. Moreover, if the presence of these alkali ions is the dominant cause for those effects, then using these impurities as a method to improve device performance is not applicable and strongly unadvisable for the following reasons: (1) the amount of the impurity introduced into the oxide varies randomly, leading to difficulties in controlling the thickness, V_{FB} and other parameters during fabrication; (2) most of those metal ions are mobile under certain bias and temperature conditions, which could cause unwanted and unpredictable shifts in V_{FB} and V_T, and result in device malfunction; (3) some of the compounds, such as CaO, NaO, Na_2O_2, and K_2O, are known to be naturally extremely reactive and are consequently aggressively corrosive to quartz and other equipment, potentially causing damage to the furnace and even resulting in accidents. Thus, because of the reasons listed above, intensive future experiments using those metal impurities are not recommended, especially with regard to their potential damage to the furnace and other equipment.

5.4 Effect of Other Anneal Methods on Alumina Enhanced Oxidation

Except for the heavy mobile ion contamination inside the oxide, alumina enhanced oxidation on Si-face 4H-SiC is a promising oxidation process that effectively reduces D_{IT}, especially near E_C, and dramatically increases n-channel MOSFET channel mobility to a peak value over 100 $cm^2/V \cdot s$. However, based on the results in the previous section, there is still potential for further improvements in the quality of the oxide, for example by reducing the D_{IT} in the deeper gap further using other annealing methods such as NO, and reducing the excess mobile ions using annealing methods such as HCl. Therefore, several of the possible annealing methods were tested for this study after the alumina enhanced oxidation and their effect on the oxide and other results are discussed in the following sections.

5.4.1 HCl Anneal on Alumina Enhanced Oxidation

5.4.4.1 Experimental Process

HCl anneal has been used in the semiconductor industry for some time as one of the annealing steps used to reduce the mobile ions introduced during the fabrication process. This is because chlorine is known for its ability to remove mobile ions such as Na^+ and K^+ by chemically reacting with these ions during the anneal, forming NaCl and KCl, and then evaporating away from the oxide. This property of the HCl anneal makes it the perfect candidate for removing the unwanted mobile ions that remain inside the oxide after alumina enhanced oxidation.

Two Si-face n-type 4H SiC samples were initially oxidized simultaneously by alumina enhanced oxidation at 1150°C for 20 minutes for comparison. One was then annealed by a standard HCl anneal procedure, using 300 sccm of mixed 10% HCl and 90% Ar at 600°C for 2 hours. Both samples were then processed into MOS capacitors for electrical measurement.

5.4.4.2 Results and Discussion

The oxide thickness extracted by C-V measurement was around 94 nm. The BTS results for both samples are shown in Figure 5.4.1 and Figure 5.4.2 as an indication of the mobile ions inside the oxide; the conditions used were +/- 1MV/cm at 250°C for 4 minutes. For the sample using alumina enhanced oxidation without HCl anneal, Figure 5.4.1, a ΔV_{FB} shift of ~28V was observed, indicating a mobile ion concentration of about 6.47×10^{12} cm^{-2}, which agrees with the previous alumina enhanced oxidation result. For the similar sample using alumina enhanced oxidation followed by a standard HCl anneal, Figure 5.4.2, no significant mobile ions were detected. Clearly, the HCl anneal successfully removed the excess mobile ions in the oxide introduced by the alumina enhanced oxidation.

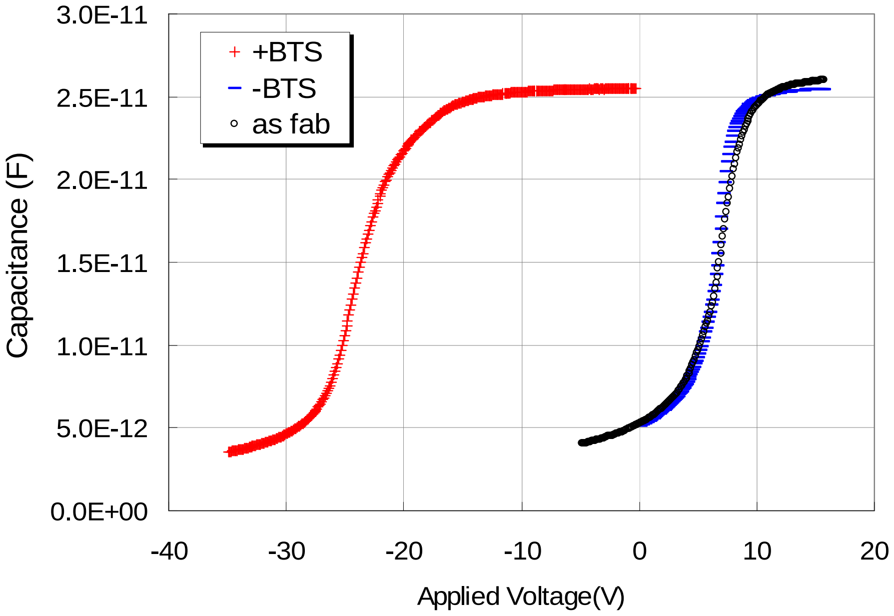


Figure 5.4.1 BTS result for sample using alumina enhanced oxidation without HCl anneal.

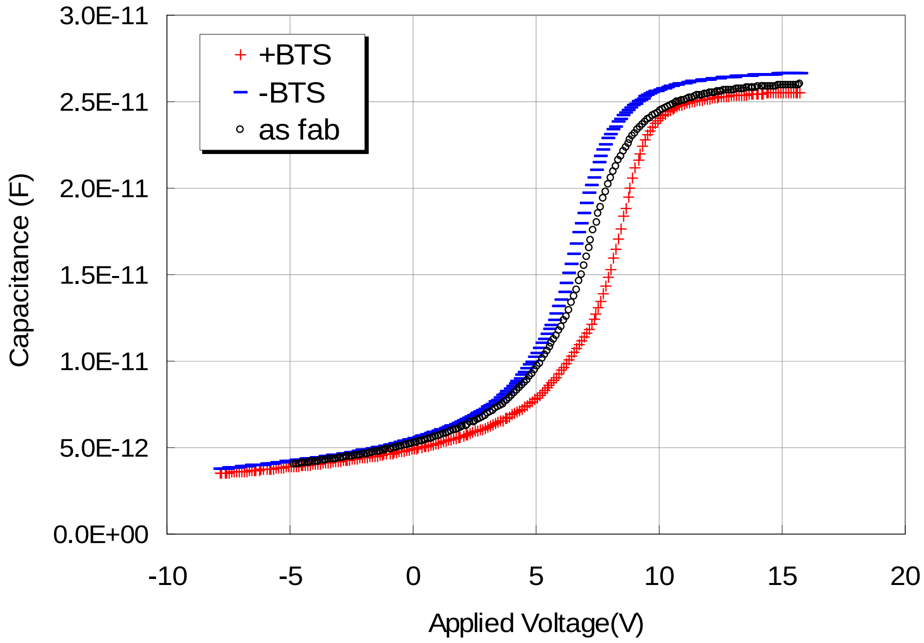


Figure 5.4.2 BTS result for sample using alumina enhanced oxidation followed by standard HCl anneal.

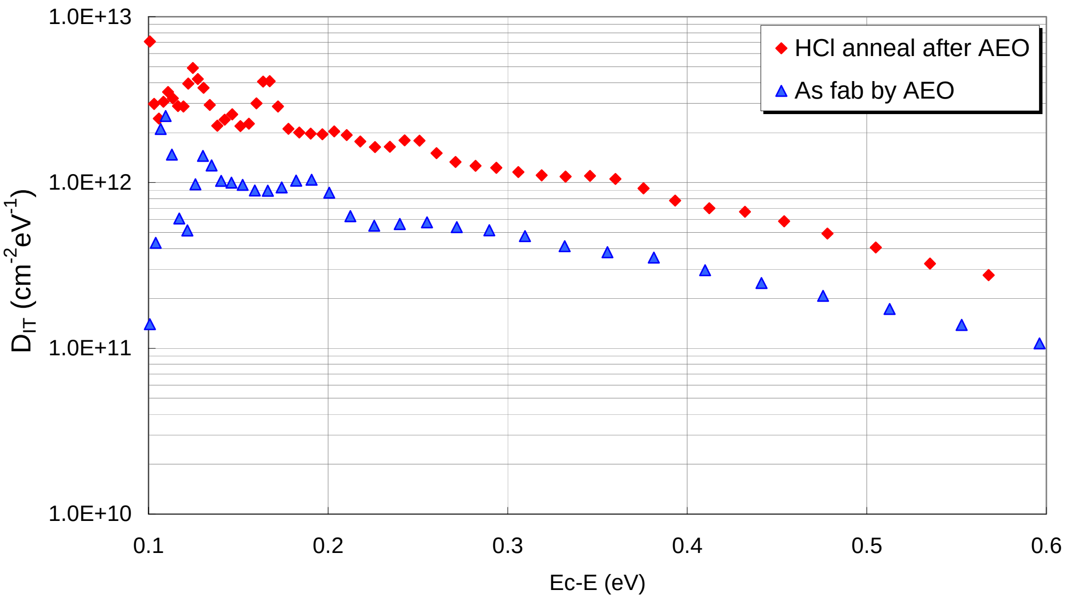


Figure 5.4.3 D_{IT} of the samples using alumina enhance oxidation with and without HCl anneal.

The D_{IT} values for these two samples are plotted in Figure 5.4.3. Note that their oxide layer is thicker than usual, meaning the oxide capacitance is relatively smaller. In this case, the system noise noticeably affected the measured quasi-static C-V curve, introducing some uncertainty into the D_{IT} value extracted from the C-V. However, by comparing the number of traps at 0.2eV~0.6eV below E_C with previous data, these results still clearly indicate that without the HCl, the D_{IT} is similar to the typical data for alumina enhanced oxidation, but when HCl removes most of the mobile ions the D_{IT} is very close to the typical data for standard O_2 oxidation without any passivation. This is therefore a good indication that the effect of reducing D_{IT} may be primarily due to the presence of mobile ions at the interface and that this can be reversed by removing the mobile ions by HCl. As yet, however, the effect of this anneal on channel mobility has not been measured; future work on this topic will be very interesting.

5.4.2 NO Anneal Following Alumina Enhanced Oxidation

In order to further improve D_{IT} and channel mobility, a standard 2-hour NO anneal was applied to the sample using alumina enhanced oxidation. The results are plotted in Figure 5.4.4. Somewhat surprisingly, NO seems to have very little effect on further improving the D_{IT} from 0.1eV below E_C to mid-gap, and the results after the NO anneal are very comparable to the data for alumina enhanced oxidation only. There are no results available for p-type material, and whether this approach might improve the other half of the band-gap is therefore unknown.

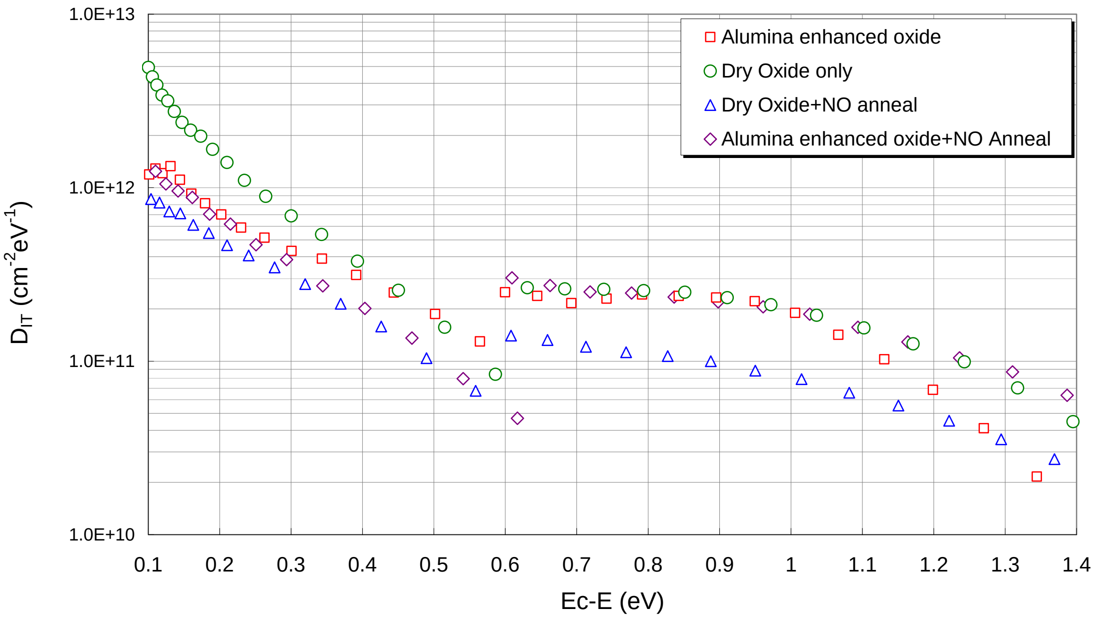


Figure 5.4.4 D_{IT} of oxides with different oxidation and annealing methods.

The I_D-V_G curve and the channel mobility extracted from the MOSFET with the same process are shown in Figure 5.4.5. The thickness of the gate oxide was around 40nm. Due to the variation in mobile ion concentration, the peak mobility also varied from 100~180 cm^2/V·s, which still agrees with the mobility values obtained from alumina enhanced oxidation alone.

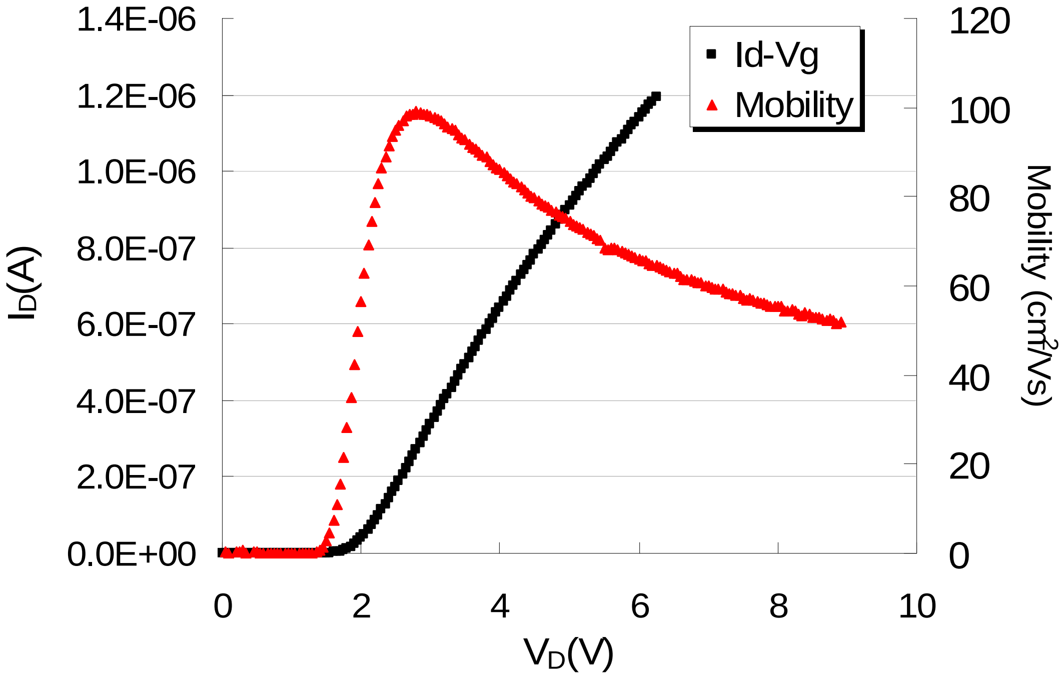


Figure 5.4.5 I_D-V_G curve and channel mobility from Si-face 4H-SiC MOSFET with alumina enhanced oxidation followed by standard NO anneal.

Based on the above results, the use of an NO anneal after alumina enhanced oxidation appears to yield no further improvement, though the reason for this is unclear.

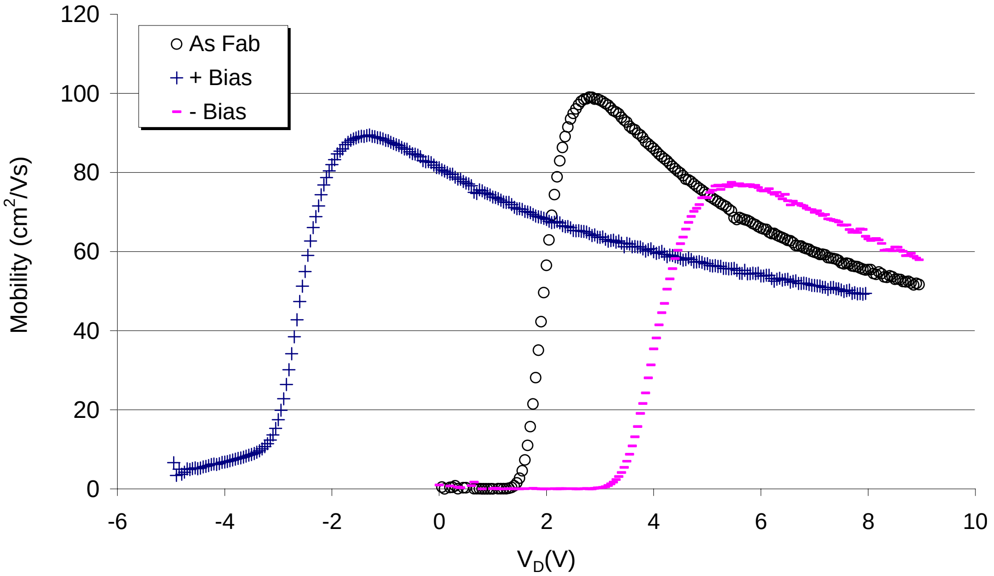


Figure 5.4.6 Channel mobility μ after +/- BTS on the MOSFET in Figure 5.4.5.

One interesting finding is that a much smaller mobile ion concentration was observed on both the MOS capacitor and the MOSFET after +/-BTS for 1MV/cm, at 250°C for 10 minutes. A small V_{FB} shift was observed in the MOS capacitor sample, while on the MOSFET shown in Figure 5.4.6 the mobile ion concentration calculated from ΔV_T was only 3×10^{12}cm^{-2}. However, it is important to be careful drawing any conclusions from this. This ΔV_T shift cannot be directly compared with previous MOSFET data with alumina enhanced oxidation due to differences in the oxide thicknesses used, as the previous samples were about 2~3 times thicker. With the alumina enhanced oxidation, the mobile ion concentration introduced during the oxidation was also very variable and uncertain. It is possible that the small mobile ion concentration is just coincidence. Finally, some of the MOSFET fabrication steps could also introduce mobile ions to a concentration of $2\sim5\times10^{12}\text{cm}^{-2}$, for example the contact anneal step. The mobile ions inside the gate oxide of that MOSFET could therefore originate from the fabrication steps rather than the oxidation process. If that were indeed the case, it is possible that the NO anneal successfully “immobilized” most of the ions. Therefore, further investigation into these issues is necessary before drawing any firm conclusions.

5.4.3 Effect on D_{IT} of Mobile Ion Removal by +/- BTS on AEO

In addition to the HCl anneal discussed earlier, another method of removing the mobile ions from the oxide layer is +/- BTS followed by BOE wet-etching. The concept is very simple. As shown in Figure 5.4.7, after oxidizing the sample using an alumina enhanced oxidation process, a broad area metal contact was deposited initially by applying +/- bias (1.5MV/cm) at 250°C for 10 minutes, as for a BTS measurement, causing mobile ions inside the oxide to move towards the interfaces driven by the field. Afterwards, the top oxide layer was removed by BOE wet-etching for ~20 seconds. The sample was then fabricated into an MOS capacitor for C-V measurement.

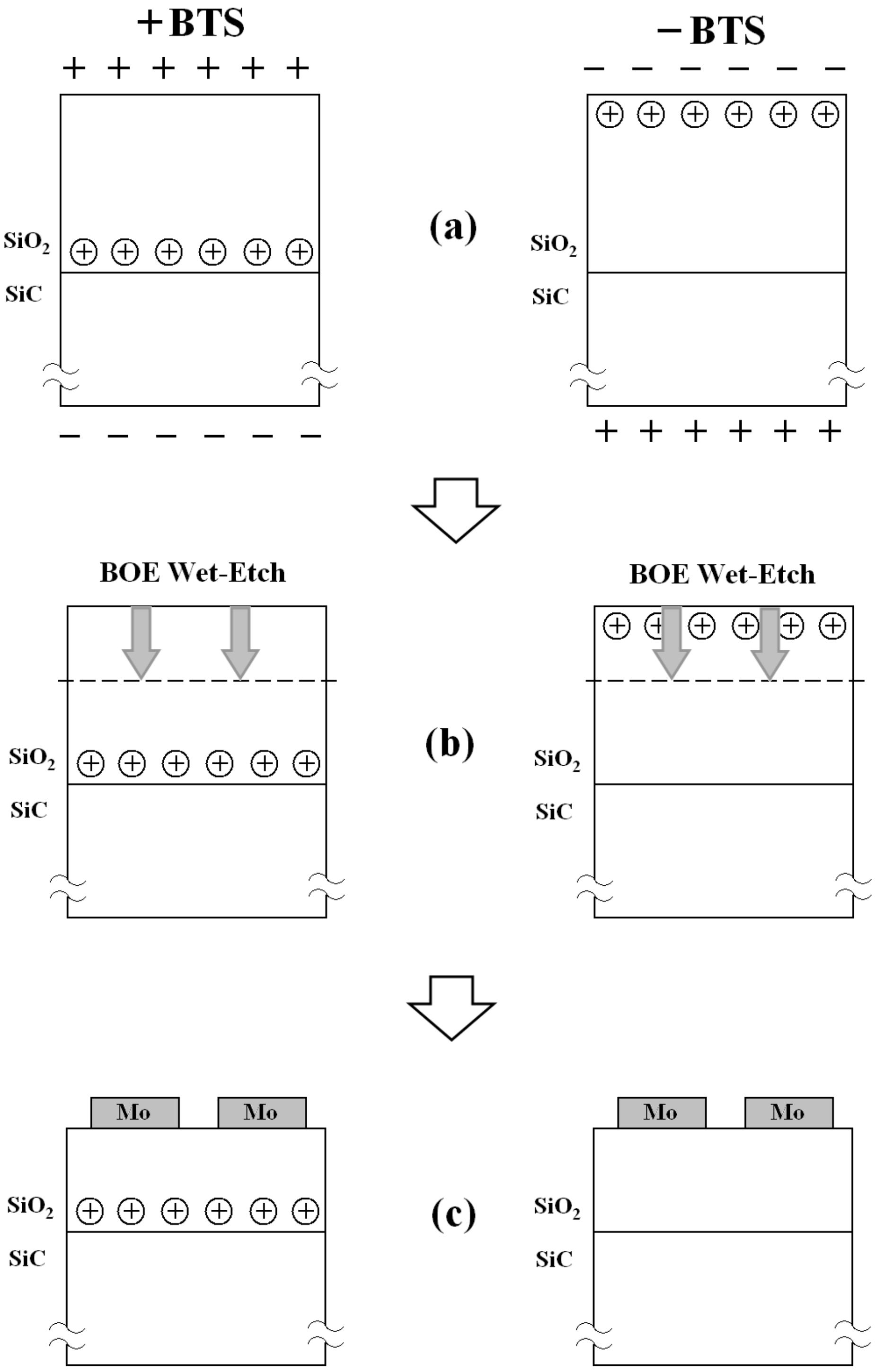


Figure 5.4.7 Diagram of reposition and removal of mobile ions by +/- BTS and wet-etch.

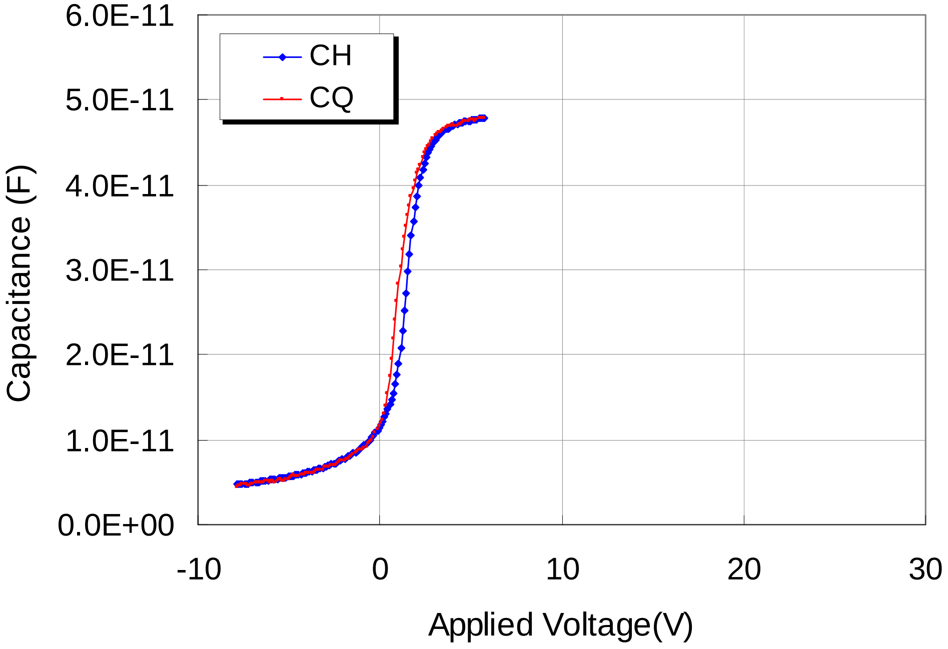


Figure 5.4.8 C-V characteristic of sample after +BTS and wet etch.

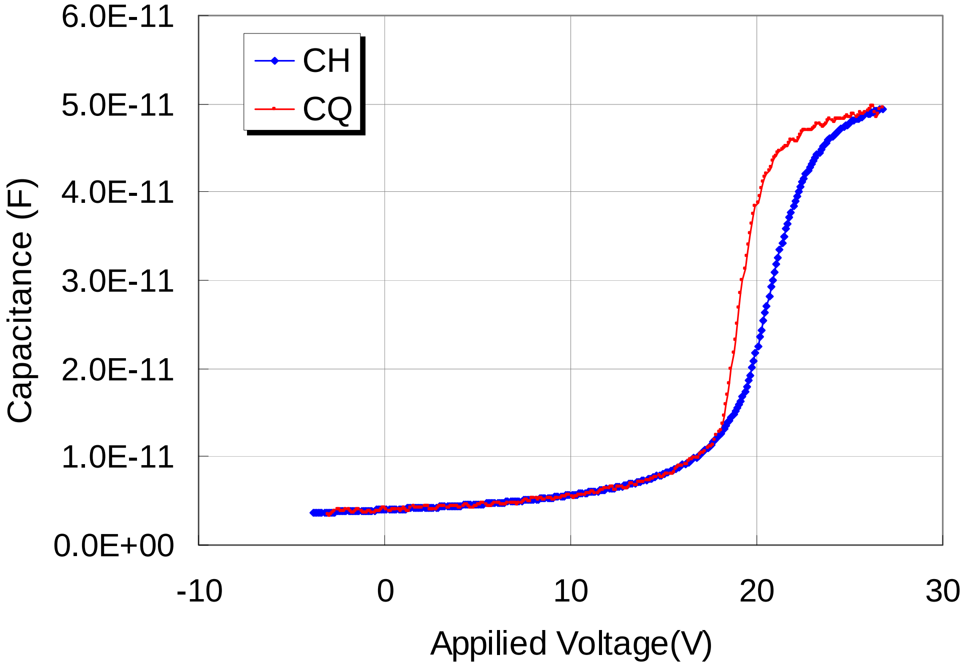


Figure 5.4.9 C-V characteristic of sample after -BTS and wet etch.

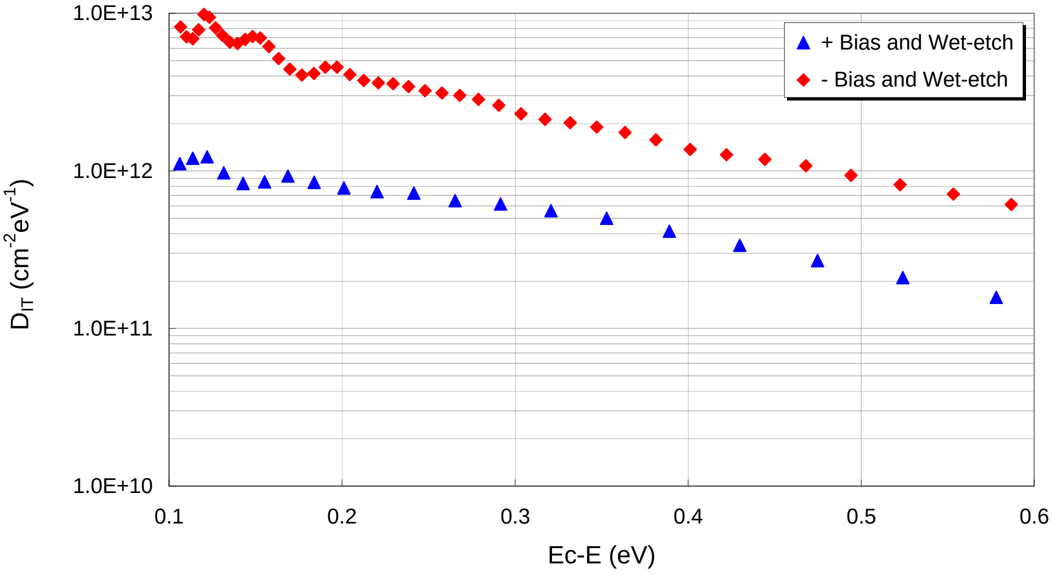


Figure 5.4.10 D_{IT} extracted form C-V curves in Figure 5.4.8 & Figure 5.4.9.

The results of this experiment are shown in Figure 5.4.8, Figure 5.4.9 and Figure 5.4.10. After the +BTS followed by wet-etching, a smaller V_{FB} is shown in Figure 5.4.8, indicating more mobile ions were present at the interface, while no further improvement in D_{IT} is visible in Figure 5.4.10, which may indicate that the initial mobile ions piled up at the interface were sufficient for reducing D_{IT}. After the –BTS followed by wet-etching, V_{FB} increased dramatically to ~20V, as shown in Figure 5.4.9, indicating most of the mobile ions were some distance from the interface, and the D_{IT} values shown in Figure 5.4.10 also increased markedly. Note that a high leakage current was observed during C-V measurement, probably due to the etching process and high voltage applied. In this case, the C-V curves and D_{IT} extracted are consequently less accurate and the increase in

D_{IT} may also be partly due to the error caused by current leakage. However, there is still a clear trend indicating that D_{IT} worsens with the removal of mobile ions.

The results from this experiment raise two questions: (1) The D_{IT} behavior contradicts the D_{IT} results after +/- BTS presented in Section 5.2.3. Further experimental confirmation about whether the reduction of the D_{IT} is caused solely due to the presence of mobile ions at the interface is therefore needed. (2) After removing the mobile ions by –BTS and wet-etching, a very large V_{FB} is shown in Figure 5.4.9, and the Q_{eff} calculated from V_{FB} is -1.45×10^{-6} C/cm^2, 2~3 times larger than the typical value, indicating a large number of negative charges are also present inside the oxide. It is possible that these negative radicals could be introduced along with the mobile ions during oxidation in order to obtain charge neutrality in chemical reaction. More experiments to resolve these issues and improve our understanding of these results are needed.

5.4.4 Summary for Annealing Methods on Alumina Enhanced Oxidation

In addition to the methods listed above, several other techniques were also tested, including H_2 anneal with Pt gate and the phosphorous stabilizing method for removing mobile ions. However, the results from all the post-oxidation methods on alumina enhanced oxidation are far from satisfactory. It is technically very difficult to eliminate the unwanted V_{FB} and V_T shift under bias and temperature while maintaining all the positive benefits from the process. The results did, however, provide evidence that the effect on the D_{IT} and mobility may arise primarily due to the presence of mobile ions in the oxide and at the interface. If that is the case, then the only way to make alumina enhance oxide commercially viable is to find a way to immobilize the ions without removing them, or to identify substitute elements that are less mobile under the same conditions.

5.5 Conclusion

As a conclusion, for the first time, this process demonstrates that it is potentially possible to increase the channel mobility of the 4H-SiC based MOSFET to a satisfying level. Unfortunately, although promising, huge amount of mobile ions are making this process unusable. For further details and recommended future work, please refer to Chapter 7.

CHAPTER 6

Nitrogen Plasma Anneal Process

6.1 General Introduction and Motivation

The previous chapters discussed the fabrication of 4H-SiC based MOS devices using its natural oxide, SiO_2, by the standard dry O_2 process, but found that this process was far from satisfactory, primarily due to the poor quality of the interface. In order to lower D_{IT} and improve the performance of SiC based MOS devices, a number of different post-oxidation anneal methods have been examined. However, apart from alumina enhanced oxidation, which is impractical due to mobile ion contamination, the most effective applicable method remains the widely used Nitric Oxide anneal. The results reported in Chapter 5 revealed a tremendous decrease in the number of interface traps both near E_C and deeper in the bandgap. A significant increase in the channel mobility was also observed for the n-channel MOSFETs, with values up to ~40 cm^2/Vs. Although the physical structure of the Si-C-O transition layer between SiO_2 and SiC remains unclear, it is possible that the passivation effect is mainly due to the N atoms bonding with Si atoms and forming Si≡N at the interface, removing C clusters, reducing C dangling bonds and forming Si-C-O-N bonds at the transition layer during the process.[100,103] However, a direct anneal of the oxide in nitrogen gas at high temperature yielded no improvement in the oxide quality because N_2 is chemically inert. In order to create this passivation effect, the addition of oxidizers such as NO or N_2O to the nitrogen is necessary, but this inevitably introduces Oxygen during the process, resulting in the continuous growth of additional SiO_2 layers at the interface. As discussed in Section 4.3, this leads to two problems: 1) competition between the creation of new oxide with new traps and the simultaneous annealing of these traps, which is suspected to be the limiting factor in the nitrogen passivation efficiency; and (2) the introduction of positive fixed oxide charges $+Q_F$ that is mostly believed to occur during the oxidation process. The presence of $+Q_F$ in the final few-nm layers closest to the interface is most important and has a major effect on all the electrical parameters, even if nitrogen reduces these charges during passivation the growth of additional oxide always creates more. Thus, with the additional oxidation created during an NO anneal, the N that accumulates at the interface may not be sufficient to passivate all the traps and counteract the $+Q_F$ created by the additional growth in time. If some of the traps and $+Q_F$ created during the additional growth time remain in the material after the passivation, then further removal of those traps and $+Q_F$ may lower D_{IT} further and reduce the unwanted negative shift of V_{FB} and

V_T after the NO anneal. This question can only be answered by conducting an experiment in which active N is introduced in an oxygen-free environment.

In order to accomplish this objective, several annealing methods were tried. These included implanting N into the deposited oxide and thermally diffusing them to the interface at high-temperature, similar to the work reported in Moscatelli et al.[101] Alternatively, chemically active NH_3 can be used as the annealing gas at a similar temperature. Unfortunately, all the methods tried were far from satisfactory, and further improvements and efforts are in progress. However, a microwave generated Nitrogen plasma is found to be a very successful and effective method of introducing chemically reactive nitrogen into the oxide in an oxygen free environment. By applying this annealing process, a similar passivating effect on D_{IT} and an increase in the channel mobility comparable to that seen in an NO anneal was observed. This finding agrees with the similar effect observed by Maeyama, et al.[82] on the D_{IT} of 6H- and 4H- SiC MOS capacitors, although they reported no accompanying increase in the mobility. Further details of the N plasma anneal process used here are presented below.

6.2 Nitrogen Plasma Anneal System and Standard Annealing Process

6.2.1 Plasma Annealing Furnace

Figure 6.2.1 shows the microwave plasma furnace system for this research. It consists of a GE 224 low sodium quartz tube, 33 inch in length, 1 inch in diameter on one end and 2.5 inch in diameter on the other end, and a Thermcraft furnace with temperature controller, similar as those used on other oxidation furnaces. It is capable of reaching temperatures about 1160°C. A 1000 Watts microwave source from a commercial microwave oven was attached to the top of the waveguide for this experiment, and the microwave radiation transmitted through the waveguide to create a plasma inside the furnace. A dampener was placed at the other end of the waveguide to dissipate any remaining microwave energy. Different gas outlets were connected at the narrow end of the furnace while a mechanical pump capable of evacuating the furnace to a base pressure of 40~50 mTorr was connected at the other end.

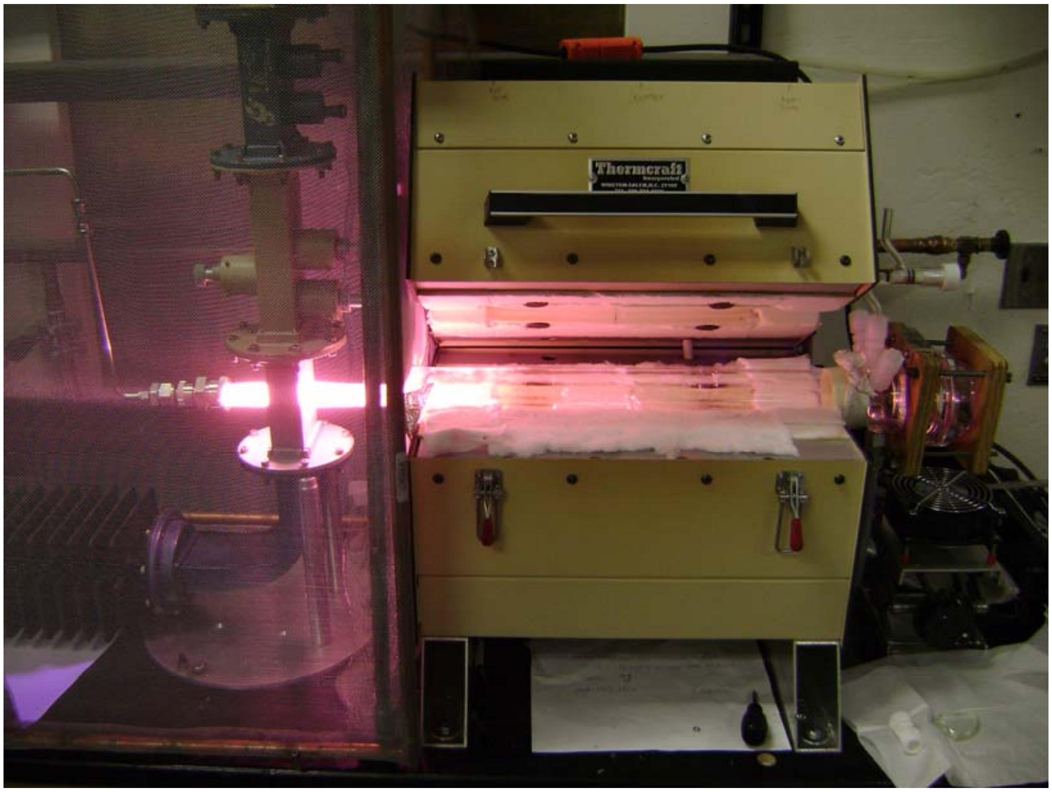


Figure 6.2.1 The plasma furnace system.

6.2.2 Nitrogen Plasma Anneal Process

A schematic diagram of the Nitrogen Plasma Anneal process is shown in Figure 6.2.2. The furnace was initially flushed with N_2 gas, then samples with oxide already grown were loaded into the furnace through a quartz paddle, with the furnace at $800^oC\sim 900^oC$ and N_2 gas flowing. The furnace was then heated to 1160^oC in an N_2 environment. Once the desired temperature was reached, the flow rate of N_2 gas was kept at 200 sccm while the chamber simultaneously was evacuated at the other end to achieve a dynamic equilibrium at a constant gas pressure of 2.75 Torr. The Nitrogen plasma created with the microwave source was then turned on for various annealing time. Due to the inefficiency of the plasma, which suffered from a very low N atom/molecule ratio, 20 hours was used as the standard N plasma annealing time in order to demonstrate the effect sufficiently. After the annealing step was complete, a post-plasma anneal was added, leaving the sample in the furnace at 1160°C in the N_2 environment for 30 minutes with the microwave and plasma turned off. This step was included to help repair the electron and ion bombardment damage to the oxide and other damage caused by the plasma and the microwave, hence improving the reliability of the oxide while retaining the benefit of the N plasma anneal. This will be discussed in more detail later in this chapter. The furnace was then cooled to 800°C and the sample was removed and fabricated into MOS devices for electrical measurement.

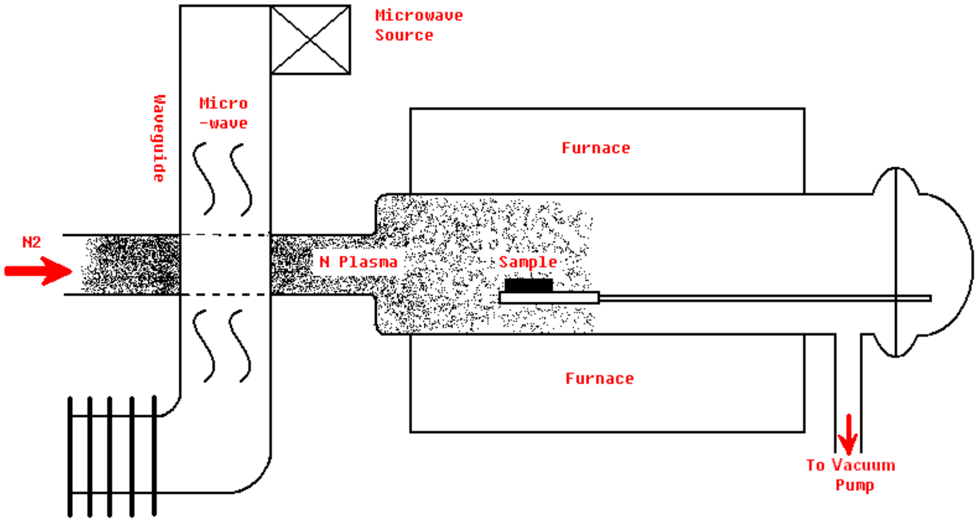


Figure 6.2.2 Schematic diagram of the microwave plasma furnace system used for nitrogen plasma anneal.

The relative inefficiency of the plasma system meant that long annealing times were needed in order to obtain acceptable results, however, this prolonged exposure to temperatures close to the softening point for quartz and the pressure imbalance due to the near vacuum inside the furnace posed a severe threat to the integrity of the quartz furnace tube. Consequently, optimizing the annealing time was very necessary. Figure 6.2.3 shows the D_{IT} of samples with different oxide thicknesses annealed for different lengths of time. Values for D_{IT} at 0.1eV below E_C (near the conduction band) and 0.9eV below E_C (deeper in the gap) are plotted for comparison. For the 20 nm oxide samples, the best annealing result was achieved after 20 hours, but for thicker oxide layers longer times were needed, especially for passivating traps near E_C. This also indicates that traps near the E_C are more resistant to N plasma anneal. As the annealing effect of the current plasma system saturates at about 20 hour according to the plot, this annealing time was chosen as the standard nitrogen plasma anneal condition for the work reported here.

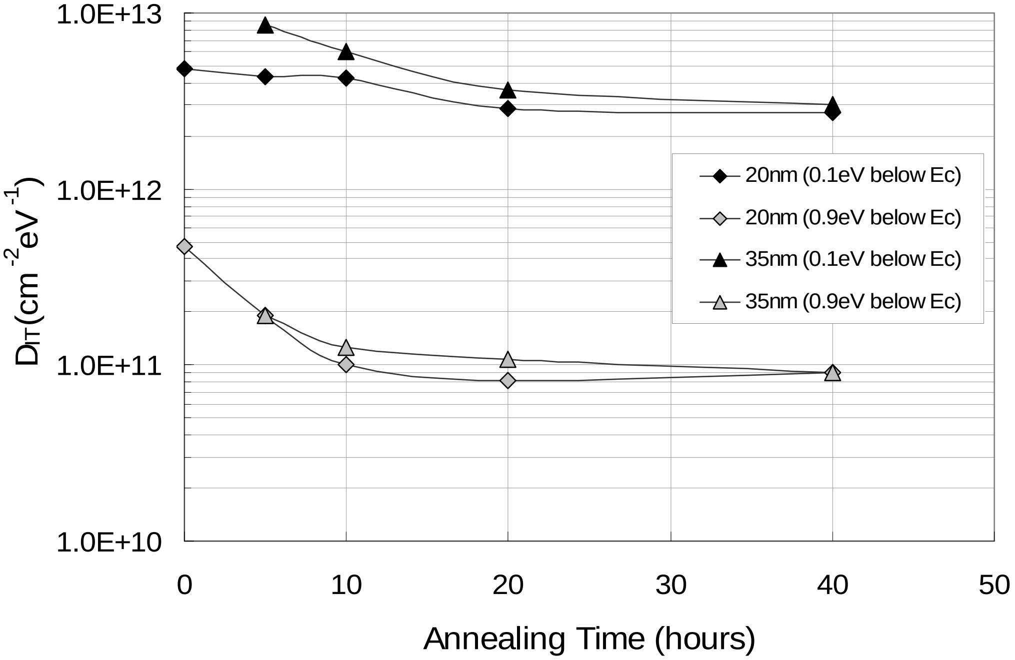


Figure 6.2.3 D_{IT} at different energy levels for samples with different oxide thicknesses after the nitrogen plasma anneal vs. annealing time.

6.2.3 System Efficiency and Optimization

This system was optimized using an Ocean Optics USB2000 Spectrometer, and the optical spectrum of the nitrogen plasma inside the furnace under low pressure was taken. On the spectrum, 589nm peak is a possible indicating of the recombination rate of the N atoms into N_2, indicating the number of nitrogen atoms that was excited initially in the plasma.[102] In this furnace, plasma can be created under pressure conditions ranging from mTorr to tens of Torrs, directly proportional to the flow rate of the N_2. Increasing the pressure and flow rate also increases the total number of gas atoms present, however, the dissociation rate also decreases dramatically. The conditions used here were optimized to maximize the number of excited nitrogen atoms present, measured to an accuracy within the limitations of the sensitivity of the spectrometer. Figure 6.2.4 shows a typical optical spectrum of the nitrogen plasma inside of the furnace taken under standard nitrogen plasma annealing conditions (N_2 flow at 200 sccm, pressure at 2.75 Torr).

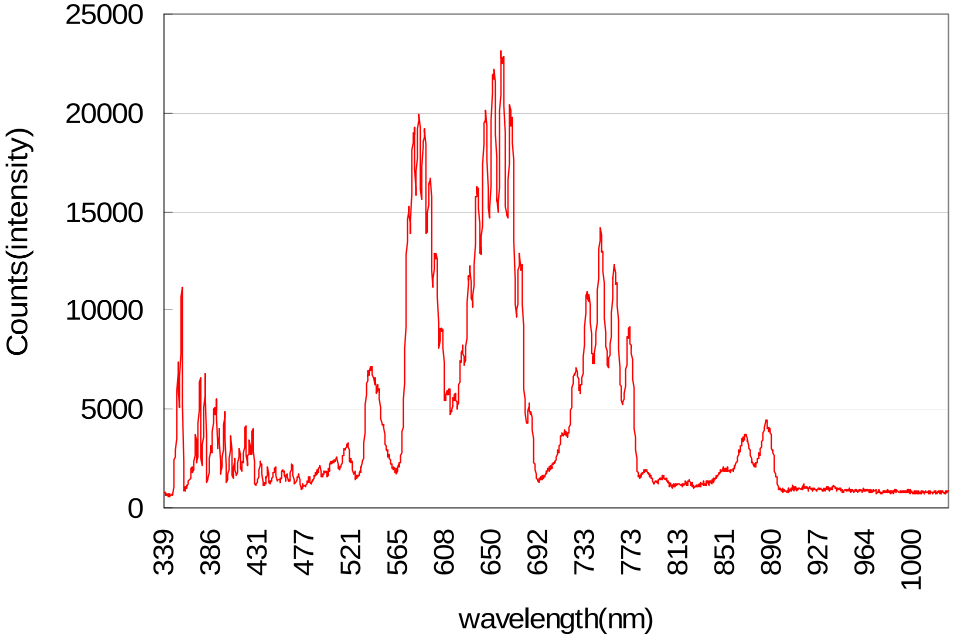


Figure 6.2.4 Optical spectrum of the nitrogen plasma inside the furnace.

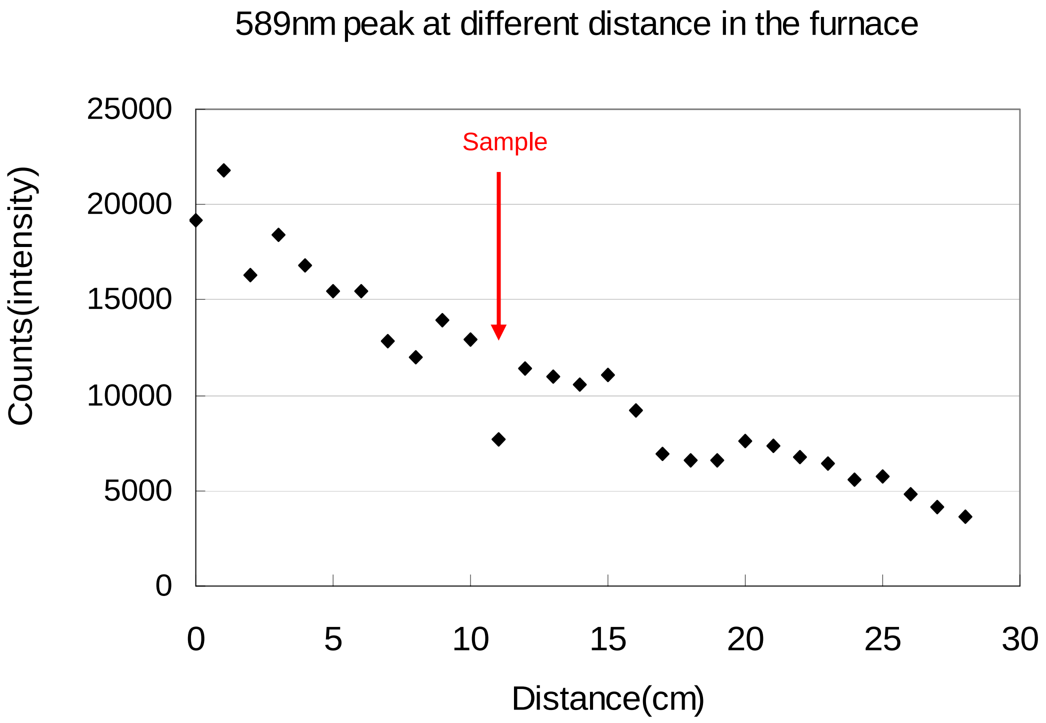


Figure 6.2.5 Intensity of 589 nm peak of the plasma spectrum inside the furnace.

For this plasma system, the life time of the excited atoms or ions was relatively short and the plasma decayed very fast. Figure 6.2.5 plots the intensity of the 589nm peak of the nitrogen plasma inside the furnace under standard nitrogen plasma anneal conditions, with the origin of the x-axis at the left outside wall of the furnace. Because the heat-zone of the furnace commenced 8~10cm from the outside wall, the sample was already placed as close to the plasma as possible, but due to the rapid decay of the plasma, the intensity of the plasma had already dropped to less than 1/2 the intensity at the wall by the time it reached the sample location. It is also important to note that the total concentration of N atoms present in the furnace during the plasma anneal was hundreds to thousands times less than the concentration of NO molecules during a standard NO anneal, although the ratio of dissociation of NO during the annealing process is also uncertain.

6.3 Electrical Characteristics of Oxides with Nitrogen Plasma Anneal

6.3.1 N Profile by Nitrogen Plasma Anneal

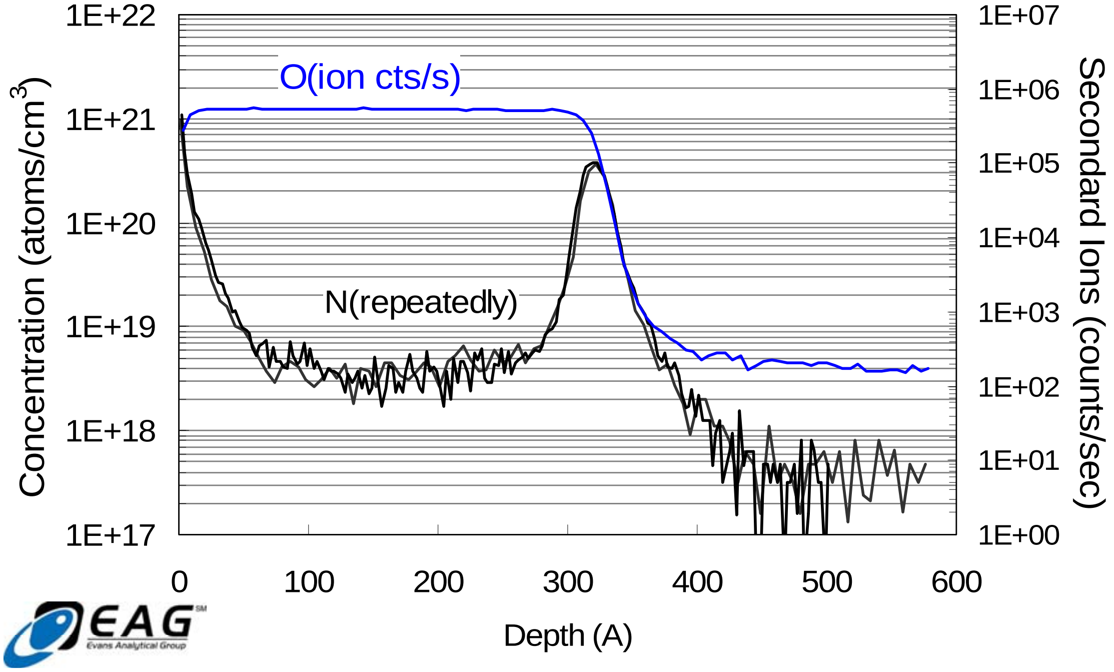


Figure 6.3.1 SIMS profile of the N concentration inside the N plasma annealed sample.

Similar to the nitrogen profile inside the NO annealed oxide depicted in Figure 4.3.1, the SIMS profile of the N concentration inside the oxide after the N plasma anneal process is shown in Figure 6.3.1. The plot is a composite of multiple measurements which overlap perfectly. As these results show, the nitrogen profile in the N plasma annealed sample is identical to that for the NO annealed oxide, with most of the nitrogen atoms accumulating at the two interfaces. As a possible explanation, this may be because the diffusion rate of nitrogen inside the oxide at $1160^{o}C$ is very high, and it is therefore able to diffuse through the oxide in minutes, but it is relatively hard to diffuse into SiC at this temperature so the excess nitrogen tends to pile up at the interface.

The concentration of the N peak at the interface of the 20-hour N plasma annealed sample is about $1\times10^{14}cm^{-2}$, which is 5~6 times smaller than the concentration obtained from a standard NO anneal, according to Figure 4.3.1. The D_{IT} result presented later in this chapter indicates that this N concentration may be the maximum value the current nitrogen plasma system can achieve in the oxide. However, by modifying and improving the system, increasing the N concentration that this annealing process can introduce into the oxide should be possible.

6.3.2 I-V Characteristics and Breakdown Field

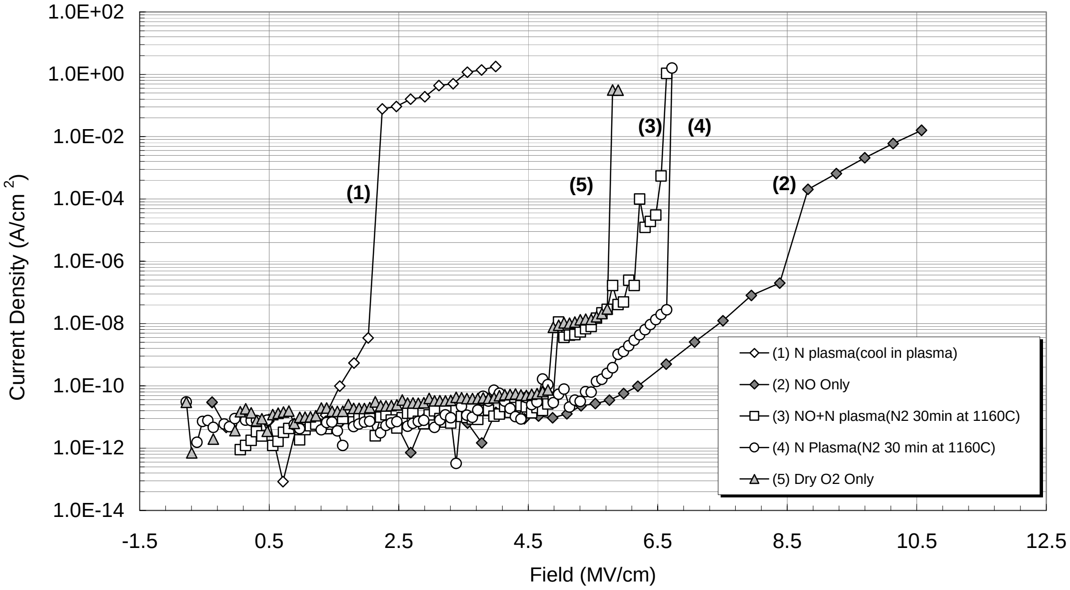


Figure 6.3.2 I-V characteristic of oxides after different annealing process.

This section presents the I-V and breakdown characteristic of the oxide after the nitrogen plasma process. Initially, plasma annealed samples were cooled down immediately after the annealing time with the plasma on, but it was found that this led to significantly decrease in the reliability of the oxide, in particular very low yields and low breakdown fields. As shown in Figure 6.3.2, curve (1) is a typical I-V data for this process, and breakdown field is less than 2.0 MV/cm. This is mainly due to the active ions and electrons in the plasma and the impact damage they cause as they are driven by the oscillating field. It was found that by passivating the oxide in an N_2 environment at 1160^{o}C, significantly improved the breakdown characteristics, while the beneficial plasma effects on interface traps were preserved. Furthermore, curve (4) is a typical I-V curve for a sample that was annealed in the N plasma, followed by the post-plasma annealing described earlier, namely 30 minutes at 1160^{o}C with N_2 gas flowing at 500 sccm before cooling down. The breakdown field of the resulting device was markedly better, at about 6 MV/cm. A similar I-V characteristic is also seen on the sample which is annealed by N plasma following a standard NO anneal. Curves (2) and (3) show the I-V data of before and after the 20hr N plasma annealing, respectively, on the same sample that is grown by dry O_2 oxidation followed by the NO anneal. As the figure shows, the breakdown field of the NO annealed sample (2) is initially at ~8.5 MV/cm, while after the plasma anneal, (3) drops to ~6.5 MV/cm, similar to (4). Based on these results, the microwave and plasma does appear to cause damage to the oxide layer and compromise the samples' I-V characteristic, however, this can be mostly ameliorated by passivating with a post-plasma anneal, which improves the breakdown field to a satisfactory level that is even slightly better than that achieved by a standard dry O_2 oxidation (5). But this approach cannot yet match the results that can be obtained using an NO anneal.

6.3.3 C-V Characteristics and Interface Trap Density (D_{IT})

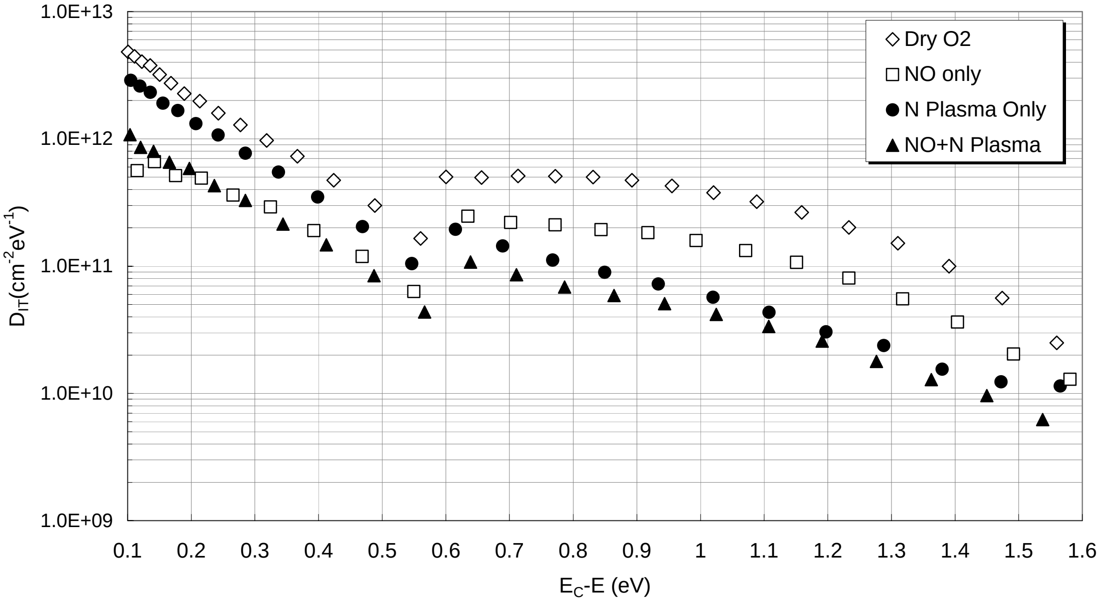


Figure 6.3.3 D_{IT} in the upper half of the 4H-SiC band-gap for different annealing methods: (1) standard dry O_2 oxidation only; (2) NO only: standard post-oxidation NO anneal; (3) N Plasma Only: 20hr N plasma anneal following standard dry oxidation; (4) NO+N Plasma: standard post-oxidation NO anneal followed by 20hr N plasma anneal.

The D_{IT} extracted from the High-Low frequency C-V measurements for n-type 4H-SiC MOS capacitors following different annealing methods is shown in Figure 6.3.3. All the oxide layers were oxidized using the standard dry O_2 procedure before anneal. The oxide thickness of all the samples was controlled at ~20 nm for better comparison. The standard 20-hour process described earlier was used for the nitrogen plasma anneal. As in all the previous results, the D_{IT} plot, 0.1~0.6eV below E_C was extracted from the room-temperature C-V measurement, while 0.6 below E_C ~ midgap was extracted from the high-temperature (300°C) measurement. As Figure 6.3.3 shows, near the E_C, the "N plasma anneal Only" curve exhibited only a small reduction in the D_{IT} compared to the sample treated with dry O_2, and it is still a factor of 2~3 higher than the sample after the standard NO anneal process. However, for the energy level deeper into the band-gap, N plasma seems to be particularly effective at annealing the traps, resulting in a D_{IT} similar to and even slightly lower than the typical D_{IT} value for a standard NO anneal. Overall, the best result was achieved by the "NO+N plasma anneal", with the beneficial effect of the NO anneal being preserved near the E_C after the nitrogen plasma anneal, it also further reduced the D_{IT} deeper in the gap. Different oxide thicknesses and annealing times were also tested in an attempt to determine the optimum values for these parameters, as shown in Figure 6.2.3.

Interestingly, the D_{IT} values obtained from the plasma anneal process closely matched the results from NO anneal. As suggested previously by Rozen,[80] with NO anneal, D_{IT} after passivation also varied in direct proportion to the total nitrogen concentration at the interface. On the plot of D_{IT} with different N concentrations by varying NO annealing times given in Figure 4.3.6 and Figure 4.3.7, the D_{IT} at 0.2eV and 0.6eV below E_C extracted from room temperature C-V measurement at N concentration of $1\times10^{14}\text{cm}^{-2}$ is around $1.5\times10^{12}\ \text{cm}^{-2}\text{eV}^{-1}$ and $8.5\times10^{10}\ \text{cm}^{-2}\text{eV}^{-1}$, respectively. This is in perfect agreement with the D_{IT} curve shown in Figure 6.3.3 for the nitrogen plasma anneal process at the same interfacial nitrogen concentration.

In conclusion, the N plasma annealing process seems to be very efficient at annealing the traps deeper in the gap and the D_{IT} obtained may even be slightly lower than that obtained using the standard NO anneal. However, although there is a noticeable reduction in the D_{IT} near E_C, it is still less effective at passivating those traps, and consequently the NO anneal is still the most efficient method of annealing those traps so far.

As the schematic still remains largely unclear, it is difficult to fully understand exactly how this annealing process passivates interface traps. However, above results suggest that possible explanations could be as follows: (1) in an as-oxidized sample, the number of interface traps at 0.6eV~1.6eV below E_C are far smaller, being 1~2 orders of magnitude less than the number of traps with energy levels close to E_C. Consequently, for annealing with small N amounts, the N contents in the oxide may be sufficient to passivate most of the traps in the deep level but not near E_C, while interface traps are far more numerous; (2) there is both theoretical and experimental evidences to indicate that traps at different parts of the band gap correspond to different types of imperfections and mechanisms. For example, it is proposed[41,103,104] that excess carbon clusters of different sizes are responsible for majority of the traps at deeper part of the band gap but few close to E_C, while intrinsic oxide defects (possibly correlated with excessive Si in SiO_2, i.e. oxygen deficiency center) near the interface and throughout the whole oxide layer are mostly likely to contribute to the high D_{IT} values near the conduction band. As a possible explanation, this model agrees well with the results reported here. The main impact of nitrogen, by forming Si≡N bonds, is very effective at suppressing the formation of excessive carbon clusters and reducing the number of carbon related traps, and this effect can be achieved both by N plasma and NO anneal. However, as for chemically annealing oxide defect related traps, NO or N_2O are still the most effective methods and the presence of O is likely to assist this process.

6.3.4 Channel Mobility for N-channel MOSFETs

As for the mobility, n-channel 4H-SiC lateral MOSFETs were made according the process in Appendix B. The gate oxide was grown separately on the 10*um* thick 5×10^{15} cm^{-2} p-epi materials by standard dry O_2 oxidation process initially. Sample in Figure 6.3.4 was then annealed by the N plasma annealing process, with the gate oxide about 41 nm thick. While sample in Figure 6.3.5 was annealed using the standard NO anneal at 1175^{o}C for 2 hours, then followed by the N plasma anneal, with the gate oxide thickness of about 50 nm. For both samples, Ni was then deposited and annealed at 870^{o}C as the contact on the highly doped source and drain, while finally Molybdenum was evaporated on as the gate contact.

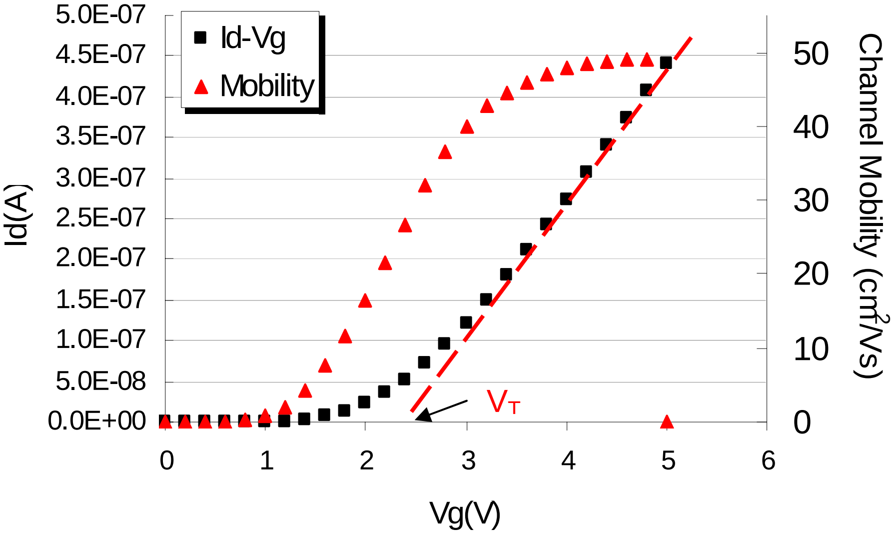


Figure 6.3.4 Channel mobility μ of n-channel MOSFET with gate oxide grown by standard dry O_2 followed by N plasma anneal.

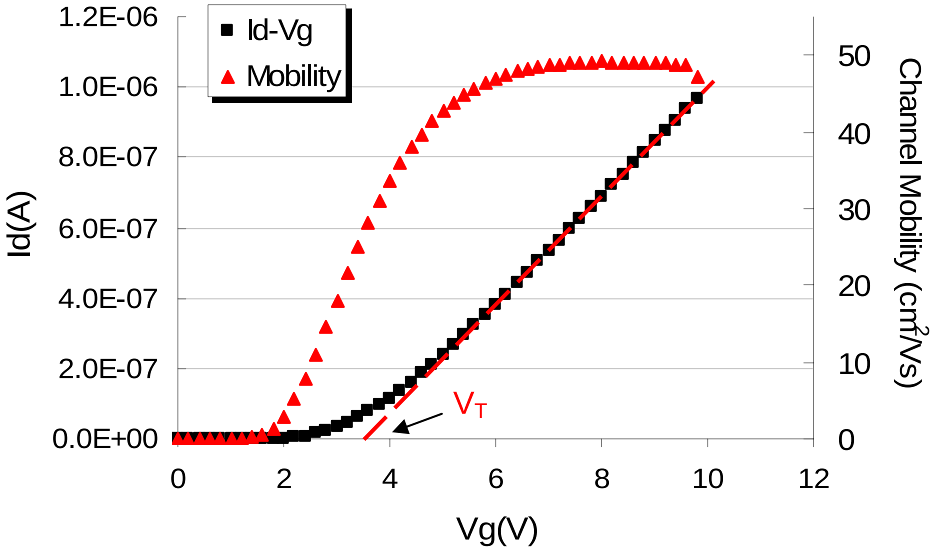


Figure 6.3.5 Channel mobility μ of n-channel MOSFET with gate oxide grown by standard dry O_2 followed by standard NO anneal then followed by N plasma anneal.

Figure 6.3.4 and Figure 6.3.5 shows the I_D-V_G curves measured at room temperature of the two MOSFETs described above, and the corresponding field-effect channel motilities were extracted from the I_D-V_G curves using the linear relation Eq 2.3.8. Interestingly, the measured peak value of the mobility of both processes is around 50 $cm^2/V \cdot s$, which is very similar to, or even slightly better than the value for the sample with standard NO annealed shown in Figure 4.3.8. When attempting to assess the threshold voltage V_T, caution is needed when directly using the values for comparison, due to the variance in the gate oxide thickness on each sample and other factors during the fabrication process which may also influence V_T, as each sample was fabricated separately. However, taking into account of the difference in thickness, Figure 6.3.4 Figure 6.3.5 and Figure 4.3.8 indicate that the V_T for samples after the N plasma annealing process is similar to the value for samples with standard NO annealed, although there may be a slight improvement by less than 1V, this is still not enough to make a practical difference for most applications.

The underlying electrical and physical mechanism governing this mobility behavior is still uncertain. However, one possible explanation is as follows: as explained in previous sections, compared with the standard NO anneal, the number of interface traps after N plasma anneal is slightly smaller in the deeper part of the band-gap, but 2~3 times greater at near the E_C compared with standard NO annealed sample. As described in Chapter 2, for an non-ideal n-channel p-type MOSFET operating from the “off” state at

0V gate bias to the “on” state under a few-Volt gate bias, the band bending is from accumulation or depletion to inversion, similar to Figure 2.2.4. During this operation, the Fermi level E_F in the semiconductor will be sweeping mostly from below the mid-gap E_i to above the mid-gap, but it may still reach as far as few tenth of eV below E_C. According to Figure 2.2.8 about interface traps, those traps at near E_C are mostly accepter-like and will remain neutral when above the E_F. As a result, they will stay uncharged all the time and are unlikely to be major contributors to the mobility at lower field. However, those traps near the mid-gap will switch from uncharged to negatively charged after the band-bending, hence affecting the mobility. Since N plasma anneal seems to be slightly more efficient at passivating those traps, this may explain why there is a slight increase in the peak mobility. Note that although the interface traps near the E_C may not be major concern for peak mobility at low field, they are still very important as most of the SiC based MOS devices are designed for high-field applications where the band-bending is much harder toward E_C and may even be above E_C. Consequently, these traps can start to affect the performance of the device.

6.4 Conclusion

In conclusion, as a novel process, prior to this research the idea of nitrogen plasma anneal has seldom been reported or used and its effects has also been studied very little, which made this work both interesting and challenging. For further details and recommended future work, please refer to Chapter 7.

CHAPTER 7

Conclusions and Recommendations for Future work

In summary, the key to industrial applications of SiC based MOS devices is to increase the performance and reliability by improving the SiO_2/SiC interface and oxide quality. In this work, all the current oxidation and passivation techniques have been examined, and results have been discussed in detail in the previous chapters. Various alternative oxidation and passivation techniques have been studied, among which, some techniques have demonstrated great potential for further improvements of device performance. However, these techniques are still too immature for industrial application, additional investigation is required for further development.

7.1 Conventional Oxidation and Passivation Techniques

SiC as a wide band gap semiconductor material has excellent physical, chemical and electrical properties for applications in high temperature, high power MOS devices. However, the performance of SiC based devices is hampered by its poor SiO_2/SiC interface quality. The main problems at the interface include: 1) existence of a thick transition layer;[71,72] 2) defects such as excessive carbon clusters for example.[73,103,104] In all, these problems can result in a high interface-trap density (D_{IT}) and low field-effect inversion channel mobility. For example, MOS devices from standard dry oxidation will yield a D_{IT} of $\sim 5\times10^{12}$ $cm^{-2}eV^{-1}$ at 0.1eV below E_C and an n-channel mobility less than 10 $cm^2/V\cdot s$.

The NO anneal process can effectively reduce D_{IT} significantly throughout the band-gap, as well as increase channel mobility on MOSFETs to about 35~40 $cm^2/V\cdot s$,[1,76~78] approximately 4 times higher than unpassivated standard dry oxidation. But even with this improvement, the performance is still far below expectation.

An important limitation of this method is the constant growth of the addition growth of oxide layer at the interface while annealing, which is continuously creating more traps and defects while being passivated at the same time. This competing effect eventually limits the effectiveness and total outcome of this process.

Another disadvantage of this method is that with the $+Q_F$ remains nearly unchanged, it lowers Q_{IT} by reducing the number of interface traps, resulting in a less negative Q_{eff}, leading to a comparatively smaller V_{FB} and V_T for similar MOS devices, and a smaller than desired turn-on voltage for the MOSFET devices.

Another commonly used passivation technique, the hydrogen anneal, is capable of further reducing the D_{IT} after NO, especially at deeper energy levels, and causing a small increase in the peak channel mobility to ~ 50 $cm^2/V{\cdot}s$.[83~85] Also, a larger decrease in the V_T is observed.

The results of all the conventional passivation techniques on SiC make the current SiC-based MOS device performance barely acceptable for commercial production. However, compared with Si-based devices, with D_{IT} at the order of 10^{10} $cm^{-2}eV^{-1}$ and channel mobility reaches up to half of its bulk mobility, the SiC device performance is still inadequate to meet all the demanding expectation for high power, high temperature applications.

7.2 Alumina Enhanced Oxidation

7.2.1 Conclusion and Discussion

In conclusion, the use of alumina enhanced oxidation on Si-face 4H-SiC effectively reduces the density of interface traps, especially those located near the conduction band. Moreover, this process increases the channel mobility of the MOSFET to a peak value of more than 100 $cm^2/V \cdot s$, which is the highest mobility ever reported[2,59] on Si-face 4H-SiC MOSFETs for any oxidation or annealing techniques. However, a large concentration of mobile ions was found to be present inside the oxide layer and they tend to move throughout the oxide under bias and temperature. As a result, it causes unpredictable and unacceptable shifts in both V_{FB} and V_T of MOS devices, limiting the application of this process for device fabrication.

The physical and chemical mechanisms of alumina enhanced oxidation process still remain unclear. As possible explanations, the fast growth rate and the improvement in electrical properties is probably caused by metal ion impurities introduced during the oxidation, most likely due to alkali metals such as Na^+ and K^+, which demonstrate similar effects while introduced into the oxide.[94] Removing the contaminants by different techniques such as HCl anneal or negative BTS with wet-etching after this process also removes most of the improvements from AEO process on D_{IT}, and possibly also the mobility. The BTS results for MOSFETs revealed that the positions of the mobile ions relative to the interface cause a large change on both V_T and mobility. These mobile ions impurities introduced into the oxide during the oxidation are most likely to accumulate at both interfaces, since their diffusivity in SiO_2 should be very large at oxidation temperatures but they cannot diffuse into SiC. A similar profile has been observed before by Nicollian & Brews[109] with Si/SiO_2 interface. The presence of these excess mobile ions at or near the interface is at least a major cause, if not the only cause, of the further reduction in D_{IT} and the dramatic increase in mobility observed here. In addition, the fact that these effects are reversible after removing the ions from the oxide by HCl anneal or negative BTS with wet-etching, indicates that the reduction in D_{IT} may simply arise because most of the trap charges are "shielded" or temporarily bonded instead of "passivated" by the mobile ions present at the interface, while the increase in the channel mobility may also be caused by those ions shielding the trap charges and/or inducing more carriers in the inversion layer.

In other samples with different gate oxides, such as with unpassivated dry O_2 oxidation or oxidation followed by a standard NO anneal, which were then intentionally contaminated by the addition of large amounts of mobile ions, a similar effect was seen after positive BTS, but the value of the peak mobility was still below that achieved by alumina enhanced oxidation. Moreover, it is interesting that after +/- BTS on MOS capacitors, D_{IT} remained almost unchanged according to the movement of mobile ions. This indicates the possibility that a very small amount of contamination may assist the removal of the excess carbon and fill the dangling bonds. It is even possible that the contaminants may react with SiO_2 chemically and form a SiO_2/SiC interface with different properties, as some alkali compounds naturally react with SiO_2 and introduce new energy levels throughout the band-gap, as proposed by Rosencher and Coppard.[99] However, even if this is in fact the case, the traps it can passivate and other effects it causes are still relatively insignificant. A large number of ions at the interface may still be necessary in order to boost the beneficial effects to a satisfactory level.

7.2.2 Future Work

To use alumina enhanced oxidation as part of the standard device fabrication process, further work and improvement is necessary. Based on the results reported here, since positive ions at the interface seems to be inevitable and essential for the improvements in the device performance, possible solutions to the problem will be a process either capable of "immobilize" the Na^+, K^+ ions, or using substitute elements which are less mobile. Based on this concept, few feasible experiments can be performed in the future:

1) Grow a thin oxide (<10 nm) at the interface using the alumina enhanced oxidation, introduce a dopant such as phosphorus to transform this layer into phosphorus silicate glass, with low diffusion constant for ions like Na^+ and K^+. In other words, most of the mobile ions may be "trapped" near the interface and become "immobile" under normal device operation condition.
2) Introduce heavier ions with similar chemical properties into the oxide and interface, which could mimic all the effects of Na^+ and K^+ on device performance such as low D_{IT} and high channel mobility in the similar manner, but less mobile under desired operating temperature and field for the device. Therefore, alkali metal ions such as Rb^+ or Cs^+ would be the best candidate. Introducing them into the oxide and

interface may be realized by either boiling the sample in their chloride solution or oxidized with their oxide compounds. However, close monitoring for furnace and equipment damage is required.

7.3 Nitrogen Plasma Anneal

7.3.1 Conclusion and Discussion

As mentioned previously, nitrogen plasma anneal has rarely been reported or used before. Compared with other nitridation passivations such as NO or N_2O process, it is the only oxygen-free method and allows a feasible way to examine and study the passivation effect of nitrogen alone. All the results have been discussed in Chapter 6, and a few conclusions can be drawn from those:

1) This process successfully introduces active nitrogen into the oxide layer during anneal. All the results indicates that the passivating effects of NO or N_2O are most likely caused by the presence of nitrogen at the interface.
2) Even with a lower nitrogen concentration at the interface, the N plasma anneal efficiently reduces the number of interface traps especially deeper traps, while for traps near E_C, it is still not as effective as standard NO anneal.

3) For 4H-SiC MOSFET devices, the channel mobility after this process is increased significantly, with the peak value similar to standard NO process, even slightly better.

Additionally, compared with other nitridation methods, the nitrogen plasma anneal also has a few advantages and great potential:

4) Unlike NO anneal, this process will not introduce the additional oxidation during the annealing process, providing a simpler and direct way to study the passivation effect of nitrogen.
5) NO anneal saturates after 2 hours, which is probably limited by the factors such as additional oxidation and dissociate rate of NO into nitrogen and oxygen atoms near the interface during anneal, which indicates there might be little room for further improvements to this anneal. In the contrary, the N plasma process still has the potential for major improvements in the efficiency by further equipment optimization, which should allow more nitrogen to be introduced into the interface than with the NO anneal, potentially resulting in better passivation effects.
6) This process is capable of more precise control on the amount of nitrogen introduced into the oxide during passivation. In addition, for mass production, this new process can be as effective as NO anneal but with a much lower cost.
7) This plasma system is potentially capable of creating other gaseous plasmas such as O_2, H_2 (special pumping and venting system is required), disassociating gas

molecules into atoms. Therefore, this system can be also used for studying the effect of other elements on the interface and oxide quality.

However, the current nitrogen plasma anneal system for this work has its own limitations as follows:

8) The efficiency of this system is very low due to the limitation of the current equipments, long annealing time is needed and the total N concentration at the SiO_2/SiC interface saturates at ~1×10^{14} cm^{-2}, about 5~6 time less than the standard NO anneal.
9) The yield and breakdown field decreased by approximately 2MV/cm compared to that with an NO anneal, which arises as a result of the damages from plasma and microwave during the anneal.
10) The threshold voltage V_T seems to have no significant increase compared with NO anneal. This indicates the nitrogen plasma anneal may have little effect on reducing $+Q_F$, same as NO anneal.

7.3.2 Future Work

As mentioned earlier, further improvement of the current plasma system is substantial. Plasma systems with similar structures has been used by other researchers,[105,106,107] who used similar spectrometer measurements to determine the ratio of active N atoms produced. Although precise numbers are still hard to obtain due to the limitations of our equipments, fortunately, the estimated dissociate rate achieved by those reported[105,106,107] is much greater than current plasma system, indicating that this system still has great potential for further improvement.

Possible improvements are as follows:

1) The current source can be replaced by a more powerful microwave source, adjustable for both frequency and power output, to enable better coupling and efficiency control.
2) A magnetic field can be added parallel with the furnace, with microwave adjusted to couple the plasma electrons to reach electron cyclotron resonance (ECR), which can drastically increase the dissociation rate of the plasma, for example as demonstrated by McCullogh et al.[105,106,107]
3) A faster pump would increase the flowing speed of the particles, enabling the plasma radicals to project deeper into the furnace. Also, special pumping and venting equipments can be installed for potential use of hydrogen, which is flammable and may cause explosion and personal injury if used under normal environment.
4) Biased electric field and /or electron traps may be placed at the vicinity of the sample holder to minimize the oxide damage caused by charged particles inside the plasma driven by the microwave.

5) Further experiments with the nitrogen plasma anneal may be conducted after the system upgrade, in hope of demonstrating increased improvement in the device performance such as D_{IT} and mobility. In addition, experiments using other gas plasmas can also be performed, For example, oxidation in the O_2 plasma at lower temperature, or hydrogen anneal with H_2 plasma.

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APPENDIX A

Sample Cleaning Procedure

All the samples mentioned in this paper are cleaned through the following procedure, firstly invented by Radio Corporation of America (RCA).[108]

I) Organic Cleaning (removal of the organic contaminants)

i) Ultrasonic in acetone for 5 minutes

ii) Ultrasonic in TCE (trichloroethane) for 5 minutes

iii) Ultrasonic in acetone for 5 minutes

iv) Ultrasonic in methanol for 5 minutes

v) Ultrasonic in methanol for 5 minutes

vi) Rinse well in de-ionized water (>18MΩ)

II) Oxide Strip (removal of existing oxide layer)

i) BOE (Buffered Oxide Etchant) for 10~20 minutes

ii) Rinse well in de-ionized water (>18MΩ)

III) Ionic Cleaning (removal of ionic contamination)

i) In $H_2SO_4 : H_2O_2$ (1:1) solution for 15 minutes

Rinse in de-ionized water for 1 minute

BOE (Buffered Oxide Etchant) for 1 minute

Rinse well in de-ionized water (>18MΩ)

ii) Boil in $NH_4OH : H_2O_2 : H_2O$ (1:1:3) solution for 15 minutes

Rinse in de-ionized water for 1 minute

BOE (Buffered Oxide Etchant) for 1 minute

Rinse well in de-ionized water (>18MΩ)

iii) Boil in $HCl : H_2O_2 : H_2O$ (1:1:3) solution for 15 minutes

Rinse in de-ionized water for 1 minute

BOE (Buffered Oxide Etchant) for 1 minute

Rinse well in de-ionized water (>18MΩ)

IV) Rinse well in de-ionized water and blow dry with N_2 gas

APPENDIX B

MOSFET Fabrication Procedure

There are totally 4 photomasks for fabricating SiC MOSFETs

#1 for mask-alignment marks etch

#2 for source and drain implantation

#3 for source and drain contacts

#4 for gate contact

i) RCA clean samples; photolithography using #1 mask; then sputter Ni (7%V) for 14 minutes (~250 nm) as mask for etching alignment marks; Lift-off; Reactive-ion etching on SiC (using NF_3), 3~4 minutes, etching depth ~300 nm

ii) Remove Ni (7%V) using HCl solution, and RCA clean; grow oxide (~40 nm) for implantation of source and drain; then photolithography using #2 mask, sputter thick Mo for 30~40 minutes (1000~1200 nm depending on ion source and energy) and lift-off to completely protect from implantation for the rest of area, and then sputter thin layer Mo 4~5 minutes (~100 nm for nitrogen, ~40 nm for Aluminum, also depending on ion source and energy) to bring the peak concentration to the surface at source and drain area.

iii) Implant at 700°C, using 4~6 different energy and doses to achieve a box distribution, doses are calculated by SRIM, with junction depth ~400 nm and concentration at the order of $\times 10^{19} \sim \times 10^{20} cm^{-3}$.

iv) Remove Mo and oxide by H_2O_2 and BOE, RCA clean for implantation activation. This activation is divided into two steps: 1) spin-on photoresist (~1.5 μm), put samples face up in the carbon box forming carbon cap to protect the surface (600°C for 30 minutes in Ar); 2) put samples face down in the carbon box for implantation activation (for Nitrogen: 1550°C, 30~40 minutes in Ar; for Aluminum: 1650°C, 30~40 minutes in Ar). Normally it will take about 20 minutes to reach desired temperature; after activation, cool down gradually and remove samples from anneal chamber when below 60°C.

v) Reactive-ion etching (using O_2) for 1~2 hours to remove carbon cap; then RCA clean, and grow sacrificial oxide (30~40 nm) to remove damaged SiC surface.

vi) Remove sacrificial oxide by BOE; RCA clean; Grow gate oxide using desired oxidation and annealing methods.

vii) Photolithography using #3 mask for contacts of source and drain (reversal technique required). After developing, hard bake photoresist 30 minutes at ~105°C, BOE etch on patterned oxide for 50~90 seconds (depending on the thickness of gate oxide) to open source and drain contact.

viii) Sputter Ni (7%V) for 7 minutes (100~120 nm) on source and drain. Lift-off using acetone, methanol, and de-ionized water. Check the contact resistance to confirm complete removal of oxides at source and drain region.

ix) Ohmic contact anneal: Rapid thermal anneal in Ar, raise temperature rapidly to 870~900^{o}C (usually take 60~90 seconds to reach desired temperature), hold ~4 minutes at 870~900^{o}C; decrease temperature quickly afterwards; wait until chamber temperature drop below 60^{o}C to takeout samples.

x) Photolithography using #4 mask for gate contacts (reversal technique required), sputter Mo as gate metal; Lift off using acetone, methanol, and de-ionized water.

xi) Remove backside oxide with BOE while covering the front surface by crystal bond; rinse well with de-ionized water; Remove crystal bond also using acetone, methanol, and de-ionized water; paste sample onto the metal plate using silver paint to form back contact.

xii) Label the sample properly and wait for at least 1~2 hours for sliver paint to dry completely. Sample is then ready for electrical measurement.

APPENDIX C

Equations Used For Major Parameter Extracted From Simultaneous C-V Measurement

As mentioned in Section 3.7, all the parameters are extracted by automated software Interactive Characterization Software (ICS) from simultaneous high-low frequency C-V data measured by Keithley instruments. Some of the important parameters are discussed in Section 2.2 of Chapter 2. According to the user's guide,[69] few major parameters are calculated using the following equations:

Oxide Capacitance

The oxide capacitance, C_{ox}, in Model 82-WIN, is taking the maximum value of the high-frequency capacitance of the device when biased in strong accumulation. The unit is pF.

Oxide Thickness

The oxide thickness t_{ox} is calculated from the C_{ox} and gate area A:

$$t_{ox} = \frac{A\varepsilon_{ox}}{(1\times 10^{-19})C_{ox}} \quad \text{…………………………………………………...… (Eq C.1)}$$

Here,

t_{ox}: oxide thickness (nm)

A: gate area (cm^2)

ε_{ox}: permittivity of SiO_2 (F/cm)

C_{ox}: oxide capacitance (pF)

Flatband Capacitance and Flatband Voltage

Based on (Nicollian and Brews 487-488),[109] the ideal flatband capacitance C_{FB} of the device is calculated using the Debye length:

$$C_{FB} = \frac{C_{ox}\varepsilon_s(1\times 10^{-4})(\lambda)}{(1\times 10^{-12})(C_{ox}) + \varepsilon_s A/(1\times 10^{-4})(\lambda)} \quad \text{………………………………… (Eq C.2)}$$

Here:

C_{FB}: flatband capacitance (pF)

C_{ox}: oxide capacitance (pF)

ε_s: permittivity of substrate (F/cm)

A: gate area (cm^2)

λ: extrinsic Debye lengh = $(1\times 10^{4})\left(\frac{\varepsilon_s kT}{q^2 N_x}\right)^2$

N_x: bulk doping, by default, N at 90% W_{MAX} is chosen, or could be input by user

The value of flatband voltage V_{FB} is interpolated from the closest V_{GS} value that gives the ideal C_{FB} on the C-V curve. Note that this method is not accurate when interface trap density becomes very large (10^{12}~10^{13} or greater), however, for comparison purpose among different devices in this paper, this algorithm should not affect any conclusions.

Threshold Voltage

The threshold voltage V_{TH} in the Model 82-WIN is calculated using the same equation as Eq 2.3.2a and Eq 2.3.2b, in Section 2.3.2 of Chapter 2, it is using the theoretical onset of the inversion when surface potential $\phi_S=2\phi_B$, and plus the V_{FB} which takes into account of most of the non-ideal factors already. However, for 4H-SiC devices, one should be careful that this equation uses the assumption that all the non-ideal charges changes very little under the band bending, from $\phi_S = 0$ to $\phi_S = 2\phi_F$, especially Q_{IT}, which is a function of surface potential. This approximation holds for a well made Si based device, but it is truly questionable for SiC based devices, due to its large interface trap density.

V_{TH} is calculated as follows:

$$V_{TH} = \left[\pm \frac{A}{10^{12} C_{ox}} \sqrt{4\varepsilon_s q \,|\, N_{BULK} \,||\, \phi_B \,|} + 2\,|\,\phi_B\,| \right] + V_{FB} \text{ ……..………………… (Eq C.3)}$$

Here,

V_{TH}: threshold voltage (V)

V_{FB}: flatband voltage (V)

C_{ox}: oxide capacitance (pF)

ε_s: permittivity of substrate (F/cm)

A: gate area (cm^2)

N_{BULK}: bulk doping (cm^{-2})

ϕ_B: (also know as ϕ_F) bulk potential (V)

$$\text{Where } \phi_B = \left(\frac{kT}{q}\right)\ln\left(\frac{N_{BULK}}{n_1}\right)(\text{dope type}) \qquad \left(\text{dope type} = \begin{cases} +1 \text{ for p-type} \\ \text{-1 for n-type} \end{cases}\right)$$

Metal Semiconductor Work Function Difference

Metal-semiconductor workfunction difference W_{MS} (also know as ϕ_{MS}) is defined as the difference of the metal work function Φ_M and the semiconductor workfunction Φ_S, both are potential difference from the vacuum level to the Fermi level in the material. Details are discussed in Chapter 2. According to (Nicollian and Brews, P462-477)[109] and (Sze, P395-402)[28], mathematically, W_{MS} can be expressed as:

$$W_{MS} = W_M - [W_S + \frac{E_G}{2} - \phi_S] \quad \text{(Eq C.4)}$$

Here,

W_M: metal work function (V)

W_S: substrate material work function (a.k.a. electron affinity χ) (V)

E_G: substrate material band-gap (V)

ϕ_B: (also know as ϕ_F) bulk potential (V)

$$\text{Where } \phi_B = \left(\frac{kT}{q}\right)\ln\left(\frac{N_{BULK}}{n_1}\right)(\text{dope type}) \qquad \left(\text{dope type} = \begin{cases} +1 \text{ for p-type} \\ \text{-1 for n-type} \end{cases}\right)$$

Effective Oxide Charge

The effective oxide charge, Q_{eff}, represents the sum of all the charges inside the oxide layer. As discussed in Section 2.2.4, Q_{eff} includes fixed oxide charge, Q_F, mobile ion charge, Q_M, interface trap charge Q_{IT}, oxide trapped charge, Q_{OT}, and other possible types of charges. And the value of Q_{eff} can be estimated from the measured V_{FB} from the C-V (Nicollian and Brews, P424-429)[109] and (Sze, P390-395)[28]:

$$Q_{eff} = 10^{-12} \frac{C_{OX}(W_{MS} - V_{FB})}{A}$$

Here,

Q_{eff} : effective oxide charge per unit area (C/cm^2)

C_{OX} : oxide capacitance (pF)

W_{MS}: metal semiconductor work function (V)

A: gate area (cm^2)

Interface Trap Capacitance C_{IT} and Density D_{IT}

The interface trap density D_{IT} is calculated from interface trap capacitance C_{IT}, while C_{IT} is extracted from the quasi-static—high-frequency C-V measurement. According to (Nicollian and Brews, P322)[109], C_{IT} can be expressed as:

$$C_{IT} = \left(\frac{1}{C_Q} - \frac{1}{C_{OX}}\right)^{-1} - \left(\frac{1}{C_H} - \frac{1}{C_{OX}}\right)^{-1} \text{…………………..………………….. (Eq C.5)}$$

Therefore,

$$D_{IT} = \frac{(1\times10^{-12})C_{IT}}{A} \quad \text{(Eq. C.6)}$$

Here,

C_{IT}: interface trap capacitance (pF)

D_{IT}: interface trap density ($cm^{-2}eV^{-1}$)

C_Q: quasi-static capacitance (pF)

C_H: high-frequency capacitance (pF)

C_{ox}: oxide capacitance (pF)

A: gate area (cm^2)

q: electron charge (1.06219×10^{-19} C)

Note that for room temperature measurement on n-type 4H-SiC MOS capacitor, the D_{IT} extracted by Eq C.6 is more accurate from 0.1eV~0.6eV below E_C, while at 300°C, the D_{IT} is more accurate from 0.6eV~1.4eV below E_C.[47]