# Soft Error Rate Determination for Nanometer CMOS VLSI Circuits

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# Soft Error Rate Determination for Nanometer CMOS VLSI Circuits

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# SOFT ERROR RATE DETERMINATION FOR NANOMETER CMOS VLSI CIRCUITS

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# THESIS ABSTRACT

## SOFT ERROR RATE DETERMINATION FOR NANOMETER CMOS VLSI CIRCUITS

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Nanometer CMOS VLSI circuits are highly sensitive to soft errors due to environmental causes such as cosmic radiation and high-energy particles. These errors are random and not related to permanent hardware faults. Their causes may be internal (e.g., interconnect coupling) or external (e.g., cosmic radiation). Nowadays, the term soft errors, also known as Single Event Upsets (SEU), specifically defines radiation errors caused in microelectronic circuits when high energy particles strike at sensitive regions of the silicon devices. The soft error rate (SER) estimation analytically predicts the effects of cosmic radiation and high-energy particle strikes in integrated circuit chips by building SER models. An accurate analysis requires simulation using circuit netlist, device characteristics, manufacturing process and technology parameters, and measurement data on environmental radiation. Experimental SER testing is expensive and analytical approaches are, therefore, beneficial.

We model neutron-induced soft errors using two parameters, namely, occurrence rate and intensity. Our new soft error rate (SER) estimation analysis propagates occurrence rate and intensity as the width of single event transient (SET) pulses, expressed as a probability and a probability density function, respectively, through the circuit. We consider the entire linear energy transfer (LET) range of the background radiation which is available from measurement data specific to the environment and device material. Soft error rates are calculated for ISCAS85 benchmark circuits in the standard units, failure in time (FIT, i.e., failures in $10^9$ hours). In comparison to the reported SER analysis results in the literature, our method considers several more relevant factors including sensitive regions, circuit technology, etc., which may influence the SER. Our simulation results for ISCAS85 benchmark circuits show similar trend as other reported work. For example, our soft error rate results for C432 and C499 considering ground-level environment are $1.18 \times 10^3$ FIT and $1.41 \times 10^3$ FIT, respectively. Although no measured data are available for logic circuits, SER for $0.25\mu$ and $0.13\mu$ 1M-bit SRAMs have been reported in the range $10^4$ to $10^5$ FIT, and for $0.25\mu$ 1G-bit SRAM around $4.2 \times 10^3$ FIT. We also discuss the factors that may cause several orders of magnitude difference in our results and certain other logic analysis methods. The CPU time of our analysis is acceptably low. For example, for C1908 circuit with 880 gates, the analysis takes only 1.14 second. The fact that we propagate the error pulse width density information to primary outputs of the logic circuit would allow evaluation of SER reduction schemes such as time or space redundancy.

This thesis also proposes a possible soft error reduction technique by hardware redesign involving circuit board reorientation. The basic idea is that the particles with LET smaller than the critical LET will not be able to cause an error if the angle of incidence is smaller than some critical angle. A proper orientation of hardware circuit boards will possibly reduce the soft error rate.

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# Chapter 1

# Introduction

From the beginning of the recorded history, man has believed in the influence of heavenly bodies on the life on Earth. Machines, electronics included, are considered scientific objects whose fate is controlled by man. So, in spite of the knowledge of the exact date and time of its manufacture, we do not draft a horoscope for a machine. Lately, however, we have started noticing certain behaviors in the state of the art electronic circuits whose causes are traced to be external and to the celestial bodies outside our Earth. The *Single Event Upset* (SEU) phenomenon, as this non-permanent (i.e., random or soft) error behavior is termed, in digital systems affects the modern nanotechnology electronic devices. We believe SEU will assume greater importance in the future [113]. We begin this introduction with a definition:

> "**Single Event Upset (SEU):** Radiation-induced errors in microelectronic circuits caused when charged particles (usually from the radiation belts or from cosmic rays) lose energy by ionizing the medium through which they pass, leaving behind a wake of electron-hole pairs". ··· *NASA Thesaurus* [13]

Continuous downscaling of CMOS technologies has resulted in clock frequencies reaching multiples of GHz range, supply voltage decreasing below one volt level and load capacitances of circuit nodes dropping to femtofarads. Consequently, microelectronics systems are more vulnerable to noise sources in the working environment. Nanotechnology therefore makes the meeting of reliability requirements highly challenging. Well-known noise

Table 1.1: Commodity flash memory reliability requirements (ITRS).

| Year | 2007 | 2010 | 2013 | 2016 |
|---|---|---|---|---|
| Density (megabit) | 1024 | 2048 | 4096 | 8192 |
| Maximum Data Rate (MHz) | 166 | 200 | 250 | 300 |
| MTTF (hours) | 4020 | 4654 | 5388 | 6237 |
| FIT=$10^9$/MTTF | $2.487\times10^5$ | $2.149\times10^5$ | $1.856\times10^5$ | $1.603\times10^5$ |

sources include power supply fluctuations, lightning and electrostatic discharge, interconnect coupling capacitance and inductance, and thermal radiation from the galaxy, radio-emitting stars and atmospheric gases. A recent study shows that among the effect of the soft failure sources, hard failure mechanisms exhibit product failure rates on the order of 1$\sim$100 FIT [186] (failures in $10^9$ hours; see Appendix B for definition of FIT). However, the soft error rate of a low-voltage embedded SRAM can easily be 1000 FIT/Mbit [28]

Electronics applications continue to demand higher reliability levels [79]. The 2002 International Technology Roadmap for Semiconductors (ITRS), in its difficult test challenges report (*www.itrs.net/Links/2002Update/2002UpdateTest.pdf*), gives the reliability requirements in mean time to failure (MTTF) for commodity flash memory as shown in Table 1.1. We notice that the maximum data rate and density are expected to increase, stressing the reliability requirements. Getting sufficient information on modern microchip reliability, especially with respect to soft errors due to alpha particles or cosmic rays, before the chip is manufactured has become more important for chip designers these days. Most integrated circuits are tested at particle accelerators for their susceptibility to single event effects (SEE). The soft error rate represents the circuit susceptibility and estimating the soft error rate can be typically done by accelerated testing. The purpose of accelerated life tests is not to expose defects, but to identify and quantify the failures and failure mechanisms which cause products to wear out before the end of their useful life [52]. Unfortunately, accelerated life testing is always time consuming because multiple runs are normally needed to get a sufficient number of samples under test to fail for data to be statistically meaningful. The test time may typically vary from few weeks to few months. The SER results will not be available until almost a year after the first chips start coming out of the fab. This long delay is generally unacceptable. One alternative method is the costly path of testing many more chips with a bigger test facility. Another is to test the chips in a more sensitive state deviated from the nominal conditions, i.e., at reduced voltage. With reduced voltage microchips are more sensitive to radiation. However, low-voltage testing has too many pitfalls to be used with confidence [199, 204].

Soft error is defined as a faulty signal state in a microelectronic circuit caused by charged particles striking at sensitive regions in silicon devices [164]. The soft errors in memories (SRAM and DRAM) were extensively studied at the end of the twentieth century [62]. Because memories have high density of components integrating a large number of storage elements, they are more sensitive to soft errors than logic circuits. Soft error rates in logic and processors are increasing along with the feature downscaling technology trend [73, 105]. In addition, if other circuit noises such as interconnect coupling and ground bounce are considered as soft errors, the logic FIT rate is expected to increase faster and finally the FIT rate in logic is likely to become comparable to the FIT rate in memories [94].

The SER due to high-energy neutrons has been studied in SRAM cells, latches, and logic circuits for feature sizes from 600nm to 50nm. SER per chip for logic circuits is expected to increase by nine orders of magnitude from 1992 to 2011, becoming comparable to the failure rates in unprotected on-chip memories [169].

## 1.1 Problem Statement

It is very costly to determine the SER of a real chip by accelerated life testing. Experimental results on measurement of neutron flux data at sea level over the past half century have shown a big variance. The neutron flux varies based on the location of the test and time-dependent solar activity [60, 141]. The buildings in which these experiments are located pose another difficulty because different mixtures of concrete will have different shielding affects on cosmic rays. These difficulties can make the measurement of the SER of a SRAM or DRAM vary up to 100X, even when tested at the same location.

Until 2002, there was no comprehensive model to reliably evaluate soft error rate of a device [202]. An accurate prediction of SER needs SER simulation using actual chip circuit models, which include device, process, and technology parameters. Current SER estimation methods are not well developed for logic circuits. Logic circuits, different from memories devices, have specific masking effects on SETs (soft error transients) that depend on the circuit properties. These masking factors are electrical masking, logic masking and temporal masking [133]. Accurate estimation of logic circuit SER continues to be a major challenge as rapid advancement in nanotechnology keeps increasing the circuit sensitivity.

In our SER analysis approach, the inputs to the analysis are (1) circuit characteristics: circuit netlist, technology and node sensitive region data, and (2)background environment data: LET distribution and neutron flux. The output of our analysis is the neutron caused logic circuit soft error rate in standard FIT (failure in time) units.

## 1.2 Contribution of Research

In this research, we model neutron-induced soft errors using two parameters, namely, occurrence rate and intensity. Our soft error rate estimation analysis propagates occurrence rate (expressed as a probability function) and intensity as the width of single event transient (SET) pulse expressed by a probability density function through the logic circuit. We develop an algorithm to compute the SER of a logic circuit based on this soft error model. We consider such issues as circuit technology and the altitude, which may influence the SER results, and use a vector-less statistical approach. We consider the entire linear energy transfer (LET) spectrum of the terrestrial background that is available from measurement data specific to environment and device materials.

Soft error rates are calculated for ISCAS85 benchmark circuits in the standard unit, failures in time (FIT, i.e., failures in $10^9$ hours). In comparison to the reported SER analysis work by Rao et al. [156], our method considers many more relevant factors, including sensitive regions, circuit technology, etc., which may influence logic SER. Our simulation results for ISCAS85 benchmark circuits differ from those reported by Rao et al. For example, our estimated soft error rates at ground level for C432 and C499 are $1.18 \times 10^3$ FIT and $1.41 \times 10^3$ FIT, while Rao et al. reported $1.73 \times 10^{-5}$ and $6.26 \times 10^{-5}$, respectively. We discuss the factors that could have caused several orders of magnitude difference between these results. Our CPU time is acceptably low. For example, for C1908 with 880 gates our analysis takes just 1.14 seconds on a Sun Fire 280R workstation.

With our novel soft error model, we are able to accurately model electrical masking factors in logic circuits. Also, the error pulse width density information at the primary outputs of the logic circuit allows evaluation of SER reduction schemes such as time redundancy and space redundancy.

An extensive discussion on soft error considerations for contemporary computer web servers is also presented. We propose a possible soft error rate reduction method that considers the cosmic ray striking angle to redesign the circuit board layout in server systems.

Four papers based on the work reported in this thesis have been authored: (1) a tutorial paper that covers broad topics on SEU was presented at the *21st IEEE International Conference on VLSI Design* [186], (2) the new soft error model and logic SER estimation algorithm was presented at the *40th IEEE Southeastern Symposium on System Theory* [187], (3) the logic SER estimated by our algorithm and that reported in other related work are compared and a detailed discussion is given in a paper presented at *17th IEEE North Atlantic Test Workshop* [185], and (4) a manuscript on SER in web servers with a proposal for its reduction is still unpublished.

## 1.3 Thesis Organization

This thesis is organized as follows. In Chapter 2, we provide the basic background on soft errors. Definitions of terms in this field, the mechanisms of how soft errors occur in silicon, and some widely used soft error mitigation techniques are discussed. In Chapter 3, previous soft error rate estimation strategies are broadly discussed. Our attempt is to include the essentials of the existing work related to soft error rate estimation in this chapter. The traditional experimental SER testing methodology is also discussed. In Chapter 4, the novel soft error model is proposed and an algorithm to compute logic SER is developed. In Chapter 5, the new results are compared with those available in the literature. Our extended work that proposes a possible soft error rate reduction method in computer web servers by considering the hardware orientation, is presented in Chapter 6. The thesis is concluded with insights on future work in Chapter 7.

# Chapter 2

# Background

## 2.1 What is Soft Error

An electronic circuit, that bears no permanent hardware fault, may display unexplained events resulting in spontaneous single bit changes in the system such that there is no way to repeat such failures. In the computer industry such phenomenon is known as a "soft fail", to differentiate from the "hard or permanent fail", which may be repairable [117, 203]. After observing a soft error, there is no implication that the system hardware is any less reliable than before because the soft fail is completely random. These soft fails may be caused by either well-known electronic noise sources such as a power supply fluctuations, lightning, and electrostatic discharge (ESD) [103], or the thermal radiation from the galaxy, such as radiation-emitting stars and atmospheric gases. A soft or non-permanent fault is a non-destructive fault and falls into two categories [180]:

1. Transient faults [38], caused by environmental conditions like temperature, humidity, pressure, voltage, power supply, vibrations, fluctuations, electromagnetic interference, ground loops, cosmic rays and alpha particles.

2. Intermittent faults caused by non-environmental conditions like loose connections, aging components, critical timing, power supply noise, resistive or capacitive variations or couplings, and noise in the system.

With advances in design and manufacturing technology, non-environmental conditions may not affect sub-micron semiconductor reliability. However, the errors caused by cosmic rays and alpha particles remain a dominant factor causing errors in electronic systems.

## 2.2 A Historical Note on Soft Errors

Soft errors have been studied by electrical, aerospace [33], nuclear and radiation engineers for almost half a century. In the period 1954 through 1957 failures in digital electronics were reported during the above-ground nuclear bomb tests. These were originally treated as electronic anomalies in the monitoring equipment because they were random and their cause could not be traced to any hardware fault [199]. Perhaps the first paper concerning the role of cosmic rays on electronics was by Wallmark and Marcus [183]. As quoted in the recent literature [123], these authors predicted that cosmic rays would start upsetting microcircuits due to high energy particle strikes and radiation when feature sizes become small enough. Through 1970s and early 1980s, the effects of radiation received attention and more researchers examined the physics of these phenomena. Also starting around 1950, theories of fault tolerant and self-repairing computing system have been developed due to the increased reliability requirements of critical applications like the space-mission [21, 22, 23, 24, 115, 181].

May and Woods of Intel Corporation [119, 120] determined that intermittent errors were caused by the alpha particles emitted by the radioactive decay of uranium and thorium present just in few parts-per-million levels in package materials. Their papers represent the first public account of radiation-induced upsets in electronic devices at sea level and these errors were referred to as “soft errors”. The term soft error was used to differentiate from the repeatable errors traceable to permanent hardware faults.

Table 2.1: Measured failure rate on SRAM-based FPGA applications due to neutron effects in 130nm technology (Actel) [6].

| Application Example | Altitude (feet) | Neutron Flux (relative) | FPGAs/ System | #upsets/ 1M-gate/ FPGA/day | MTBF (hours) | FIT (million) |
|---|---|---|---|---|---|---|
| (1) Ground-based Communication Network | 5000 | 1 | 512 | $4.19 \times 10^{-4}$ | 112 | 8.92 |
| (2) Civilian Avionics System | 30,000 | ~40 | 4 | $1.85 \times 10^{-2}$ | 324 | 3.09 |
| (3) Military Avionics System | 60,000 | >160 | 16 | $8.33 \times 10^{-2}$ | 18 | 55.56 |

Table 2.2: Projected failure rate on SRAM-based FPGA applications due to neutron effects in 90nm technology (Actel) [6].

| Application Example | Altitude (feet) | Neutron Flux (relative) | FPGAs/ System | MTBF (hours) | FIT (million) |
|---|---|---|---|---|---|
| (1) Ground-based Communication Network | 5000 | 1 | 512 | 58 | 17.24 |
| (2) Civilian Avionics System | 30,000 | ~40 | 4 | 162 | 6.17 |
| (3) Military Avionics System | 60,000 | >160 | 16 | 9 | 111.11 |

Guenzer and Wolicki [74] reported that the error causing particles came not only from uranium and thorium but that nuclear reactions generated high energy neutrons and protons, which could also cause upsets in circuits. Following the title of their paper, “Single Event Upset of Dynamic RAMs by Neutrons and Protons”, the term “SEU” has been in use ever since [74, 123]. In 1979, Ziegler and Lanford from IBM [203] predicted that cosmic rays could result in the same upset phenomenon in digital electronics (not only memories) even at sea level.

Recent *Soft Error Rate* (SER) testing results for SRAM-based FPGAs from Actel [6] show a significant and growing risk of functional failures due to the corruption of configuration data, especially when the system has higher densities. Table 2.1 and Table 2.2 show measured failure rates for 130nm technology and projected failure rates for 90nm technology, respectively, for different applications without using any error protection. The error rates are shown in units of MTBF (Mean Time Between Failures) and FIT (Failures in Time). The number of upsets per 1 million gates per day increases for cases

(1) through (3) because of the altitude dependent increase in neutron flux density. It is expected that neutron-induced soft errors will get worse by a factor of two as we move from 130nm to 90nm technology. Note that this table ignores alpha particle effects, which are also expected to be significant for nanometer technologies and will further increase the system failure rate.

Radiation induced soft errors have become one of the most important and challenging failure mechanisms in modern electronic devices. SER for commercial chips is controlled to within 100–1000 FIT. Compared to most hard failure mechanisms that produce failure rates on the order of 1–100 FIT, the SER of a low-voltage embedded SRAM can easily be 1000 FIT/Mbit. Therefore, a four-phase approach to deal with them is in progress [162]:

1. Methods to protect chips from soft errors (prevention).
2. Methods to detect soft errors (testing).
3. Methods to estimate the impact of soft errors (assessment).
4. Methods to recover from soft errors (recovery).

## 2.3 Radiation Environment Overview

### 2.3.1 Radiation Types

Radiation is kinetic energy in the form of high speed particles and electromagnetic waves. In general, radiation mechanisms can be classified as either ionizing radiation or non-ionizing radiation [89, 174, 175, 176].

1. Ionizing radiation is radiation with enough energy, so that during interaction with an atom it can remove tightly bound electrons from their orbits, thus causing the atom to become charged or ionized. Examples are gamma rays and neutrons.
2. Non-ionizing radiation is radiation without enough energy to remove tightly bound electrons from their orbits in atoms. Examples are microwaves and visible light.

Common types of radiation include: alpha particles, beta radiation, gamma rys, and X-rays. Neutron particles are also encountered in nuclear power plants, high-altitude flights and are also emitted from some industrial radioactive sources. In some types of atoms, the nucleus is unstable and spontaneously decays into a more stable form after releasing energy as radiation. The major types of radiation are summarized as follows [89]:

**Gamma rays and X-rays** are short-wavelength photons or electromagnetic radiation. The two names come from their discoveries at different times. Gamma rays have their origin in nuclear interaction while X-rays originate from electronic or charged-particle collisions. Their interaction mechanisms with matter are identical. The photons are lightly ionizing, highly penetrating, and leave no activity in the irradiated material. Gamma rays have a comparatively higher penetrating power, and it takes a thick sheet of metal such as lead or concrete to attenuate them significantly.

**Alpha Particles** are the nuclei of helium atoms consisting of 2 protons and 2 neutrons. They have an identical mass as a helium nucleus and a positive charge of $2e$, where $e$ is the magnitude of charge on an electron, $e = 1.6 \times 10^{-19}$ coulomb. They normally have high energy in the MeV range (see Appendix A). They interact strongly with matter and are heavily ionizing. They have low penetrating power and travel in straight lines. They are easily stopped even by a sheet of paper. A typical alpha particle energy is 5 MeV with a typical range of 50mm in air and $23\mu$ in silicon.

**Beta Particles** have the same mass as an electron but they may be either negatively or positively charged. Because they have small mass and charge, they can penetrate matter more easily than alpha particles but are easily deflected. They have high velocity normally approaching that of light. They produce weak ionization. Beta particles are stopped by a sheet of aluminum or plastic such as perspex.

**Neutron** has the same mass as proton but has no charge, thus it is difficult to deflect. The capture of a neutron can cause the emission of gamma rays. Neutron rays (streams of neutrons) are classified according to their energy as thermal neutrons (energy $< 1$ eV) [60], intermediate neutrons (1 ev $<$ energy $<$ 100 KeV), and fast neutrons (energy $>$ 100KeV). Water is an effective shield for neutrons.

**Proton** is the nucleus of a hydrogen atom and carries a positive charge of 1 unit, i.e., $+e$. The proton has a mass thousands of times that of an electron, and consequently is more difficult to deflect. The proton has a typical range of several centimeters in air, and tens of microns in aluminum at energies in the MeV range.

The particle masses, charges and radii of interest for radiation effects are listed in Table 2.3, derived from experiment data [70].

The ionizing radiation effects in electronics, such as space vehicle electronics, can be separated into two types: total ionizing dose (TID) and single event effects (SEE) [106].

- **Total Ionizing Dose (TID)** causes long term degradation of electronics through cumulative energy deposited in a material. Effects include parametric failures,

Table 2.3: Mass, charge and radius of particles of interest in radiation effects [70].

| Particle | Mass (kg) | Charge (C) | Radius (m) |
|---|---|---|---|
| Proton | $1.672\times10^{-27}$ | $1.672\times10^{-19}$ | $1.535\times10^{-18}$ |
| Neutron | $1.674\times10^{-27}$ | 0 | $6.317\times10^{-18}$ |
| Electron | $9.109\times10^{-31}$ | $1.602\times10^{-19}$ | $2.817\times10^{-15}$ |

variations in device voltage and functional failures. Significant sources of TID exposure in the space environment include trapped electrons, trapped protons, and solar flare protons.

- **Single Event Effect (SEE)** occurs when a single particle strikes the material and deposits sufficient energy in the device to cause an upset. Here, SEE includes soft errors (SEU, SEFI) and hard errors (SEL, SEB, SEGR[1]).

Parametric and permanent functional failures are the principal failure modes associated with the TID environment. Since TID is a cumulative effect, the total dose tolerances of devices are MTTF (mean time to failure, see Appendix B) numbers, where the time-to-failure is the amount of mission time until the device has encountered enough dose to cause failure [106].

The progression in manufacturing processes to ever deeper sub-micron technologies is increasing the risk from system reliability issues. Due to neutron effects the manufacturers of telecommunications and networking systems are developing qualification tests to identify components that are susceptible to soft errors. The main sources of radiation environment within the interest of avionics and electronics have been listed as follows [50]:

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[1] for definitions of TID, SEU, SEE, SEL, SEFI and SEGR, see Appendix A

- Trapped Belts: Protons and electrons trapped in the Van Allen[2] belt.
- Heavy ions trapped in the magnetosphere.
- Cosmic ray protons and heavy ions.
- Protons and heavy ions from solar flares.

### 2.3.2 Terrestrial Radiation Environment

When galactic cosmic rays traverse the earth's atmosphere, they collide with atomic nuclei and create cascades of interactions and reaction products like neutrons. Some of these neutrons reach the ground and become a source of single event upsets (SEU) in microelectronics. Neutrons produce SEU only when they collide with the nucleus of an atom in a device or its packaging, causing the nucleus to recoil and release densely ionizing nuclear fragments [72]. The probability of a neutron producing a nuclear recoil and fragments to which a particular device may be sensitive depends on the neutron's kinetic energy.

It has been discovered that cosmic rays impinging on the Earth's atmosphere have almost 90% of the particles as protons, about 9% as helium nuclei (alpha particles) and about 1% as electrons. They are influenced by the Earth's magnetic field and other factors like colliding with atmospheric molecules. The initial particles originating from the outer space (also called "primaries"), have a shower of about 1600 particles

---

[2] The radiation belts are regions of high-energy particles, mainly protons and electrons, held captive by the magnetic influence of the Earth. They have two main sources. A small but very intense "inner belt"(some call it "The Van Allen Belt" because it was discovered in 1958 by James Van Allen of the University of Iowa) lies within 4000 miles or so of the Earth's surface. It mainly consists a high-energy protons (10-50 MeV) and is a by-product of the cosmic radiation, a thin drizzle of very fast protons and nuclei which apparently fill all our galaxy [13].

per square meter per second, with a mean energy of ~7 GeV and an energy spectrum that falls off at the rate of energy$^{-5/2}$. The particles with energies below ~1 GeV are deflected by the earth's magnetic field and do not cause showers. The incident particles are protons, helium ions, and heavier ions [198, 200, 201, 203]. These heavy ions interact like individual nucleons. Ziegler et al. [201] report the incident flux as 87% protons and 13% neutrons from measurement. Almost all of the primaries effectively disappear by altitudes of 20,000m. The secondary particles produced by interaction of the primaries with the gas atoms of the atmosphere include nucleons, electrons and photons. The secondaries are either stopped within the atmosphere from producing further cascades of particles or spontaneously decay into other particles. Finally, the remnants of the cascade strike the earth.

The hit rates of different particle types, such as alpha particles or neutrons, are available from experimental results [72, 203]. It is, however, necessary to note that there are large variations in the documented measured fluxes. These may due to the effects attributed to magnetic latitude, solar cycles, time of day, season, and so on.

The natural radiation levels strongly depend on the activity of the sun and the average solar cycle is eleven years, with approximately four years of solar minimum and seven years of solar maximum shown in Figure 2.1 [9]. Neutrons, created by cosmic ray interactions with $O_2$ and $N_2$ in the air, reach a peak flux value at around $60,000$ feet. At $30,000$ feet the neutron flux is about 1/3 of the peak value and on the ground the neutron flux is 1/400 of its peak value [140] (Figure 2.2). Solar flare protons, together with electrons and alpha particles in smaller quantities, are emitted by the sun periodically during solar storms. These particles with high energy during a solar storm can cause

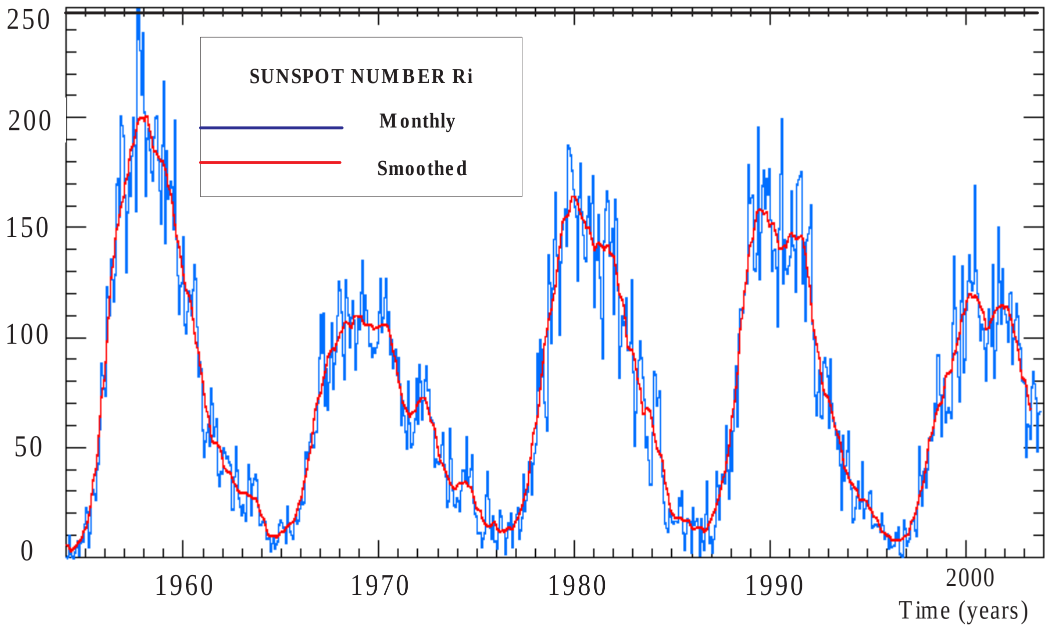

Figure 2.1: Sunspot numbers (y-axis) during solar cycles 19 through 23 recorded by Solar Influences Data Center (SIDC) in Belgium [9].

significant damage to spacecraft solar arrays [71] and produce SEU in electronics [90, 179]. The particle hit rate $R_{PH}$ is given by the equation [200].

$$R_{PH} = \int_{E_{n,min}}^{E_{n,max}} F_n(E_n) dE_n \cdot A_t \tag{2.1}$$

where $F_n(E_n)$ is the altitude and location dependent neutron flux [200] defined between neutron energies $E_{n,min}$ and $E_{n,max}$, and $A_t$ is the total silicon area of a logic circuit. Figure 2.3 [4] illustrates the neutron flux at a variety of altitudes and latitudes. Note that the flux density is more three times higher in Denver than it is in New York, even though both cities are on approximately the same latitude, but Denver is located at a much higher altitude [6].

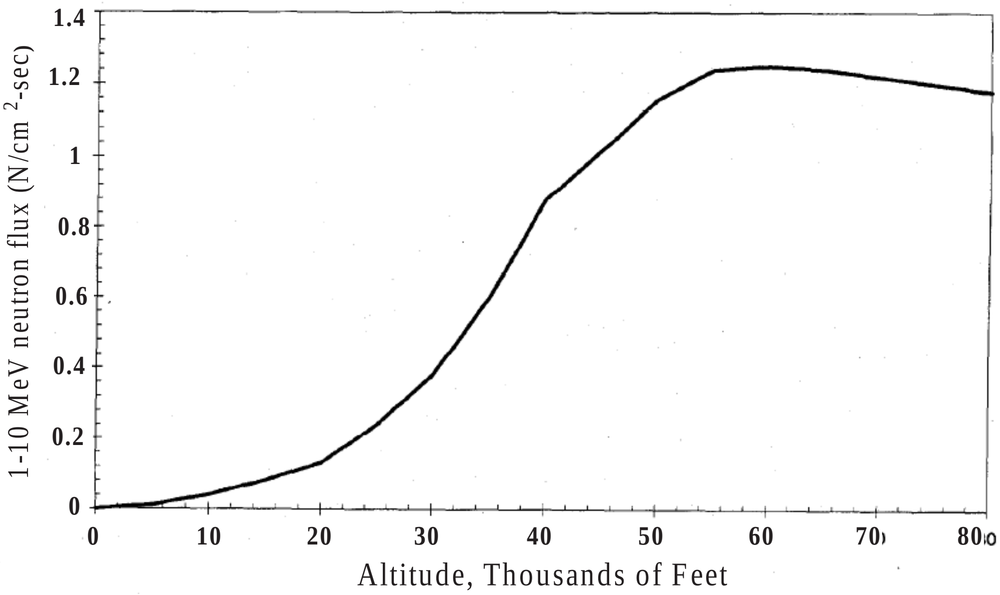

Figure 2.2: Neutron flux versus altitude showing peak at about 60,000 ft [139].

In the terrestrial environment, another significant source of ionization in packaged devices is alpha particle coming from the radioactive impurities in the package materials. This radiation mechanism will be discussed in the next section.

## 2.4 How Soft Error Occurs in Silicon

This section discusses the soft errors caused by radiation and particle strikes.

### 2.4.1 Radiation Mechanisms in Semiconductors

Three principal radiation sources cause soft errors in advanced semiconductor devices [30]:

1. Alpha particles are emitted when the nucleus of an unstable isotope decays to a lower energy state. The particles contain kinetic energy in the range of 4 to 9

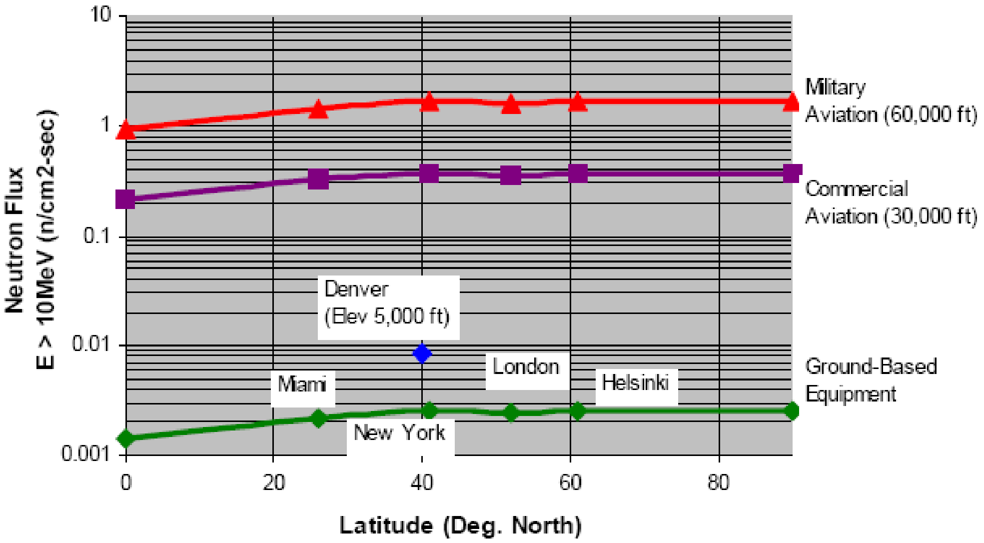

Figure 2.3: Neutron flux as a function of altitude and latitude [4].

MeV. There are many radioactive isotopes. However, uranium and thorium have the highest activity among naturally occurring materials. In the terrestrial environment, major sources of alpha particles are radioactive impurities such as lead-based isotopes in solder bumps of the flip-chip technology, gold used for bonding wires and lid plating, aluminum in ceramic packages, lead-frame alloys and interconnect metalization [50].

2. High-energy ( $> 1$ MeV) neutrons from cosmic radiation can induce soft errors in semiconductor devices via secondary ions produced by the neutron reaction with silicon nuclei. Cosmic rays that are of galactic origin react with the Earth's atmosphere to produce complex cascades of secondary particles. Less than 1% of the primary flux reaches ground level and the predominant particles include muons, neutrons, protons, and pions. Because pions and muons are short-lived and proton

and electrons are attenuated by Coulombic interaction with the atmosphere, neutrons are the most likely cosmic radiation sources to cause SEU in deep-submicron semiconductors at the terrestrial altitudes. The neutron flux is dependent on the altitude above the sea level, the density of the neutron flux increases with the altitude.

3. The third significant source of ionizing particles in electronic devices is the secondary radiation produced from the interaction of cosmic ray neutrons and boron [31]. This radiation is induced by low-energy cosmic neutrons, interacting with the isotope *boron-10* or $^{10}B$. Boron is extensively used as $p$-type dopant in silicon and is also specifically used in formation of BPSG (*Borophosphosilicate glass*) dielectric layer [31]. Boron has two isotopes: $^{10}B$ and $^{11}B$ of which $^{10}B$ is unstable. The reaction scheme is shown in Figure 2.4 [26]. In the $^{10}B(n,\alpha)$ Li reaction the lithium nucleus is emitted with a kinetic energy of 0.84 MeV 94% of the time and with 1.014 MeV 6% of the time. The gamma photon has energy of 478 KeV, while the alpha particle is emitted with an energy of 1.47 MeV [26]. This mechanism has recently been found to be the dominant source of soft errors in $0.25\mu$ and $0.18\mu$ SRAMs fabricated with BPSG. Modern microprocessors use highly purified package materials and this radiation mechanism is greatly reduced, leaving the high-energy cosmic rays as the major reason for soft errors.

The SEU due to activation of $^{10}B$ can be mitigated by removing BPSG material from the process flow. For future deep-submicron DRAM generations a greater suppression of soft error rate is expected for devices made with silicon-on-insulator (SOI) technologies [132].

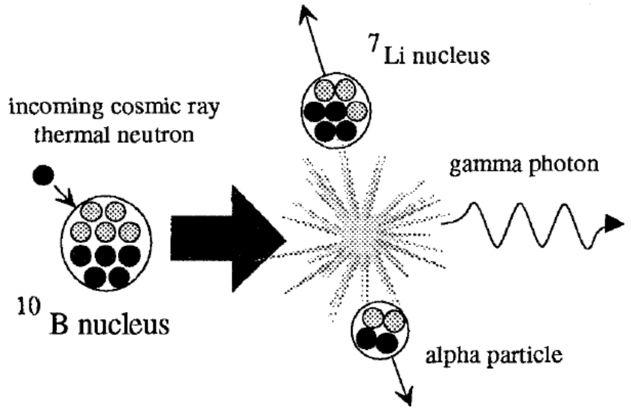

Figure 2.4: Fission of $^{10}B$ induced by the capture of a neutron (commonly happened in SRAMs) [26].

### 2.4.2 Sensitive Regions in Silicon Devices

A *single event transient* (SET) is caused by the generation of charge due to a single particle (proton or heavy ion) passing through a sensitive node in the circuit [157]. SET in linear devices differs significantly from other types of *single event effects* (SEE) like SEU in a memory. Each SET has its unique characteristics like polarity, waveform, amplitude, duration, etc. These characteristics depend on particle impact location, particle energy, device technology, device supply voltage and output load. In CMOS circuits, the "off" transistors struck by a heavy ion in the junction area are most sensitive to SEU by particles with LET (*linear energy transfer*; see Appendix) of around 20 MeV-cm$^2$/mg. When these particles hit the silicon bulk, minority carriers are created and, if collected by the source/drain diffusion regions, a change in the voltage value of the signal node occurs [144].

A particle can induce SEU when it strikes at the channel region of an off nMOS transistor or the drain region of an off pMOS transistor. The ionization induces a current

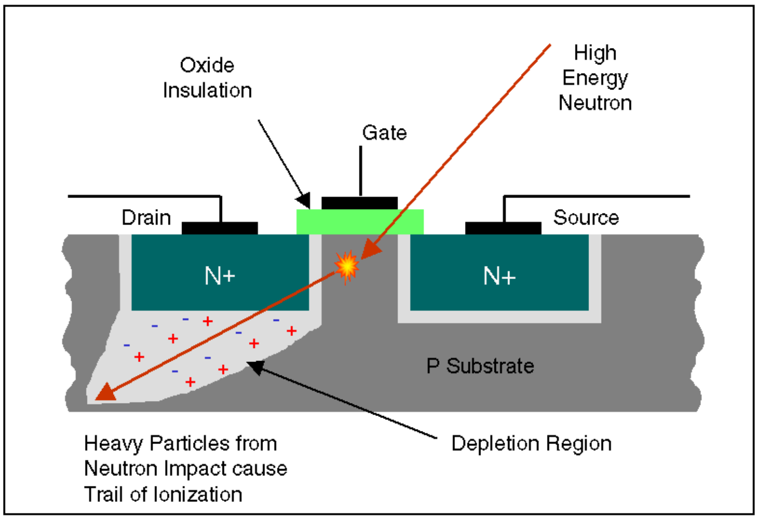

Figure 2.5: Interaction of a high energy neutron and a silicon integrated circuit [6].

pulse in a p-n junction. Conceptually, when the charge injected by the current pulse at a sensitive node exceeds a critical charge ($Q_{crit}$), a SET is generated at the affected junction. In Figure 2.5 [6], interaction of a high energy neutron and a silicon integrated circuit is shown.

### 2.4.3 Single Event Transient (SET)

In Figure 2.6, a SET is produced after a high-energy ionizing particle strikes a silicon device near a sensitive node [29]. Along the traversed path, the particle produces a dense radial distribution of electron-hole pairs as illustrated in Figure 2.6(a). If the resultant ionization track traverses the depletion region, carriers are rapidly collected by the electric field, thus compensating the charge stored in the junction. Outside the depletion region the non-equilibrium charge distribution induces a temporary funnel-shaped potential distortion along the trajectory of the event, further enhancing charge

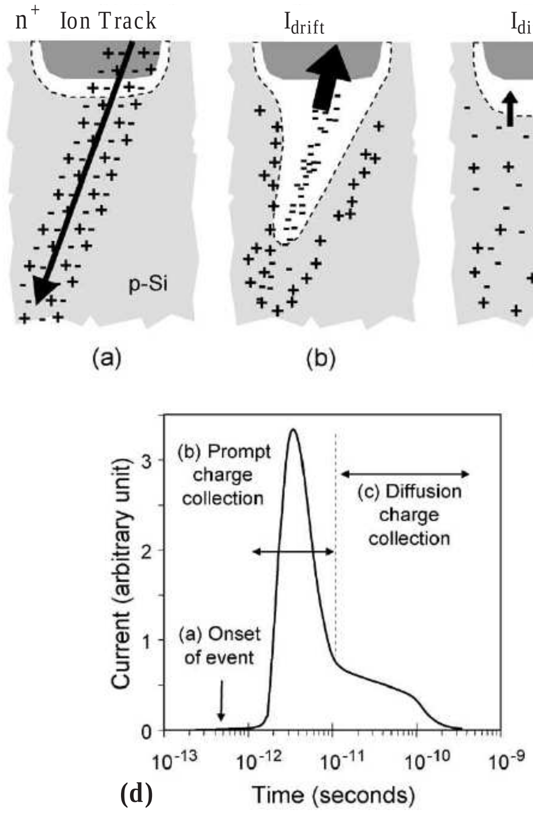

Figure 2.6: Schematic representation of charge collection in a silicon junction immediately after (a) an ion strike, (b) prompt (drift) collection, (c) diffusion collection, and (d) the junction current induced as a function of time [29].

collection by drift (Figure 2.6(b)). A "prompt" collection phase typically follows for several tens of picoseconds. As the funnel collapses, diffusion then dominates the collection process (Figure 2.6(c)) until all excess carriers have been collected, recombined, or diffused away from the junction area (about nanoseconds). The transient charge collected from the radiation event produces a current pulse at the junction as illustrated in Figure 2.6(d) [29].

Figure 2.7 [149] shows the mechanism of the current pulse generation. The cur-

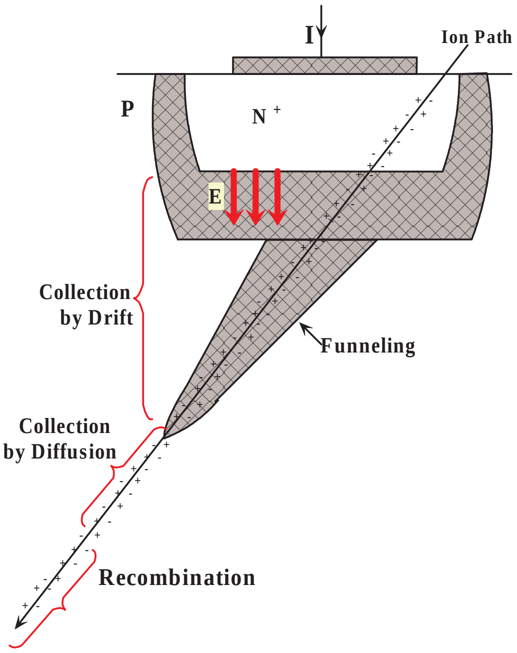

Figure 2.7: Schematic of the charge collection mechanism when an ionizing particle strikes an electronic junction [149].

rent transient typically lasts for 200 picoseconds, with the bulk of the charge collection occurring within 2∼3 microns of the junction region for modern submicron CMOS technologies. The time constant depends strongly on the type of particle, its initial energy and the properties of the specific device technology [29]. If enough charge is collected by a node its logic state may change. The collected charge ($Q_{coll}$) is a function of the ionizing particle's energy and trajectory, silicon substrate structure and doping, and the local electric field [29].

A commonly used approximate analytical model for the induced transient current waveform for ion track charge collection has a double-exponential form [122] with a rapid rise time and a gradual fall time:

$$\begin{cases} I(t) = \frac{Q_{coll}}{\tau_\alpha - \tau_\beta}\left(e^{-\frac{t}{\tau_\alpha}} - e^{-\frac{t}{\tau_\beta}}\right) & \text{(a)} \\ Q_{coll} = 10.8 \times L \times LET & \text{(b)} \end{cases} \tag{2.2}$$

where $Q_{coll}$ is the collected charge (in femtocoulomb) in the sensitive region, $\tau_\alpha$ is a process-dependent collection time constant of the junction, and $\tau_\beta$ is the ion-track establishment time constant, which is relatively independent of the technology. Typical values are approximately $1.64 \times 10^{-10} sec$ for $\tau_\alpha$ and $5 \times 10^{-11} sec$ for $\tau_\beta$ [43]. In bulk silicon, a typical *charge collection depth* ($L$ in microns) is $2\mu$ for every linear energy transfer ($LET$) of 1 MeV-cm$^2$/mg, and an ionizing particle deposits about $10.8fC$ charge along each micron of its track.

*Linear energy transfer* (LET) is a measure of the energy transferred to material as an ionizing particle travels through it. The unit of LET is MeV-cm$^2$/mg of material for electronic devices. It is derived from a combination of the energy lost by the particle to the material per unit path length (MeV/cm) divided by the density of the material (mg/cm$^3$).

The induced transient voltage pulse may propagate through several levels of logic gates. Because a particle can induce an SEU when it strikes either the channel region of an off nMOS transistor or the drain region of an off pMOS transistor, we will consider the strike at an off pMOS drain area as an illustrative example. The critical charge depends on the total charge collected at the sensitive node as well as on the temporal shape of the current pulse and the device supply voltage. A parameter called “switching time ($t_{th}$)” or “feedback time” is defined as the interval starting when the particle strikes and continuing until the affected node voltage exceeds the threshold voltage. The charge on the output capacitor of the gate containing the transistor equals $Q_{crit}$ at that time. $Q_{crit}$ can be calculated by integrating the current that flows at the sensitive node after the strike [57]. The condition for the SEE to propagate is that output node voltage follows Equation 2.3.

$$V \geq \frac{Q_{crit}}{C} = \frac{1}{C}\int_{0}^{t_{th}} I_{induced}(t)dt \tag{2.3}$$

The width of the voltage pulse depends on the value of the capacitance and the $RC$ time constant of the discharging path. For example, in AMI12 technology, when the output load capacitance is $100fF$ and the cumulative collected charge is $0.65pC$, the amplitude of the voltage pulse is,

$$0.65pC/100fF = 0.65 \times 10^{-12}C/100 \times 10^{-15}F = 0.65V$$

We observe that for the same charge collected in the sensitive area a smaller load capacitance will have a larger amplitude of the SEE-induced voltage pulse. The discharge process can be modeled by a simple $RC$-circuit. Then, the voltage as a function of time is $v(t) = v(0)^{\frac{-t}{RC}}$. Clearly, smaller the $RC$ value, faster is the discharge process. A schematic view of how the SEE-induced current pulse translates into an SEE-induced voltage pulse is given in Figure 2.8. With technology scaling, *multiple* transient faults may become an issue for next generation ICs [161].

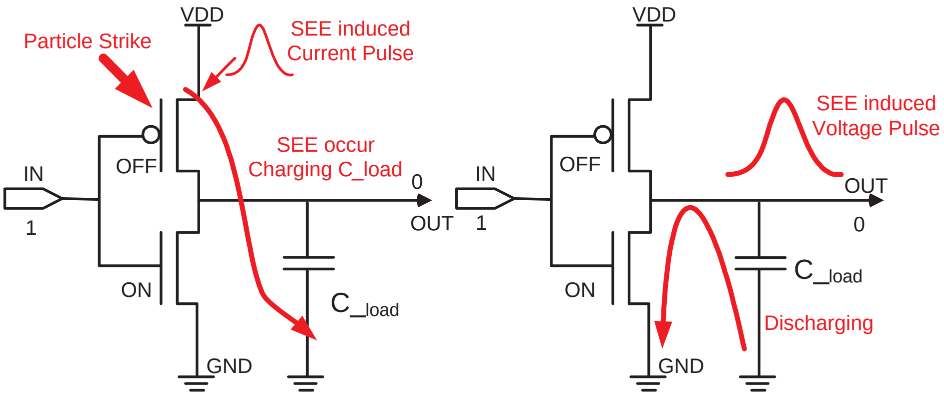

Figure 2.8: A schematic view of how SEE-induced current pulse translates into a voltage pulse in a CMOS inverter.

## 2.5 An Overview of Soft Error Mitigation Techniques

Soft error tolerant design techniques can be classified into two types: prevention and recovery. The methods to protect microchips from soft-errors are the prevention methods [186]. They are used during the chip design and development. The recovery methods include on-line recovery mechanisms from soft-errors in order to achieve the chip robustness requirement. These include fault tolerant computing, Error Correcting Code (ECC) and parity, online-testing [66, 97, 99, 101, 137, 138] and redundancy [151, 163]. One should note that soft error is not the only reason why computer systems need to resort to a recovery procedure. Random errors due to noise, unreliable components, and coupling effects may also require recovery mechanisms [162]. The need for a recovery mechanism stems from the fact that prevention techniques may not be enough for contemporary microchips, because the supply voltage keeps reducing, feature size keeps shrinking, and the clock frequency keeps increasing. Also, the cost of prevention techniques for a fault tolerant design may be too high. Representing the broad area of the error-tolerant computing, here we give a few examples of techniques used for soft error mitigation. In addition, a built-in soft error resilience (BISER) technique for correcting radiation-induced soft errors in latches and flip-flops may be found [192]. In that work, the error-correcting latch and flip-flop designs are power efficient, can correct both flip-flop errors and combinational logic errors, and reuse the on-chip scan design-for-testability hardware for cell-level error recovery.

### 2.5.1 Prevention Techniques

#### Purify the Fabrication Material

A significant reduction in the soft error rate of microelectronics can be achieved by eliminating or reducing the sources of radiation. To reduce the alpha particle emission in packaged ICs, high purity materials and processes are employed. Uranium and thorium impurities have been reduced below one hundred parts per trillion for high reliability. Going from the conventional IC packaging to an ultra-low alpha packaging materials, the alpha emission is reduced from 5$\sim$10 particles/cm$^2$-hr to less than 0.001 particles/cm$^2$-hr. To reduce the SER induced by the $^{10}B$ activation by low energy neutrons, BPSG is replaced by other insulators that do not contain boron. In addition, any processes using boron precursors are carefully checked for $^{10}B$ content before introducing them to the manufacturing process [29]. When these measures are employed the SER of the IC is reduced dramatically, but the SER caused by the high-energy cosmic neutron interactions cannot be easily shielded.

### Radiation Hardened Process Technologies

SER performance can be greatly improved by adapting a process technology either to reduce the collected charge ($Q_{coll}$) or increase the critical charge ($Q_{crit}$) [197]. One approach is to use additional *well* isolation (triple-well or guard-ring structure) to reduce the amount of charge collected by creating potential barriers, which can limit the efficiency of the funneling effect and reduce the likelihood of parasitic bipolar collection paths [40].

Another approach replaces bulk silicon well-isolation with silicon-on-insulator (SOI) substrate material. The direct charge collection is significantly reduced in SOI devices because the active device volume is greatly reduced (due to thin silicon device layer on the oxide layer) [132]. Recent work shows a 10X reduction in SER achieved over conventional bulk devices when a fully depleted SOI substrate is used. Unfortunately, SOI substrates are more expensive than conventional bulk substrates and phenomena like parasitic bipolar action limit further reduction of SER [29, 76, 132]. Circuit-level solutions such as the addition of cross-coupled resistors and capacitors to decrease the bit-line float time are also employed [172].

### 2.5.2 Recovery Techniques

Fault-tolerant computing methods have been reported in the literature for quite some time [181] but have seen renewed interest due to the SEU phenomenon. On-line testing techniques are frequently used as recovery solutions for soft error mitigation. Specific techniques include self-checking design [136], concurrent error detection for finite state machines (FSM) by signature monitoring [46, 48], error detection and correction (EDAC) codes [75], and redundancy [21].

### Redundancy

The basic idea of redundancy in design is to gain higher system reliability by sacrificing the minimality of time or space, or both. The classic triple modular redundancy (TMR) [21, 42, 47, 69, 110, 115, 168, 182] with a majority voter continues to be widely used.

Mitra *et al.* [127] combine a self-checking design with time redundancy based on the C-element gate to compare two samples of the output signal from a combinational circuit at times $t_0$ and $t_0 + d$, where $t_0$ is the clock sampling time and $d$ is finite amount of delay. The C-element has the ability to eliminate glitches at combinational outputs. Their error correction structure is illustrated in Figure 2.9 [127]. In this design, if there is an error pulse of width smaller than $d$ that occurs in the combinational logic in Figure 2.9(b), this error pulse will generate different values at clocking edges $t_0$ and $t_0 + d$. Because the output of the C-element will retain the correct value, the error will be corrected. Space redundancy and time redundancy are often combined together to meet high fault-tolerance requirements with reduced hardware overhead, such as duplication and comparison instead of TMR.

### Error-Correcting Code and Parity

Memories have a significant role in modern systems. Because of very high density of storage cells, a large memory is more sensitive to ionizing particles than logic. A simple solution for protecting a memory is to add parity bits to each memory word.

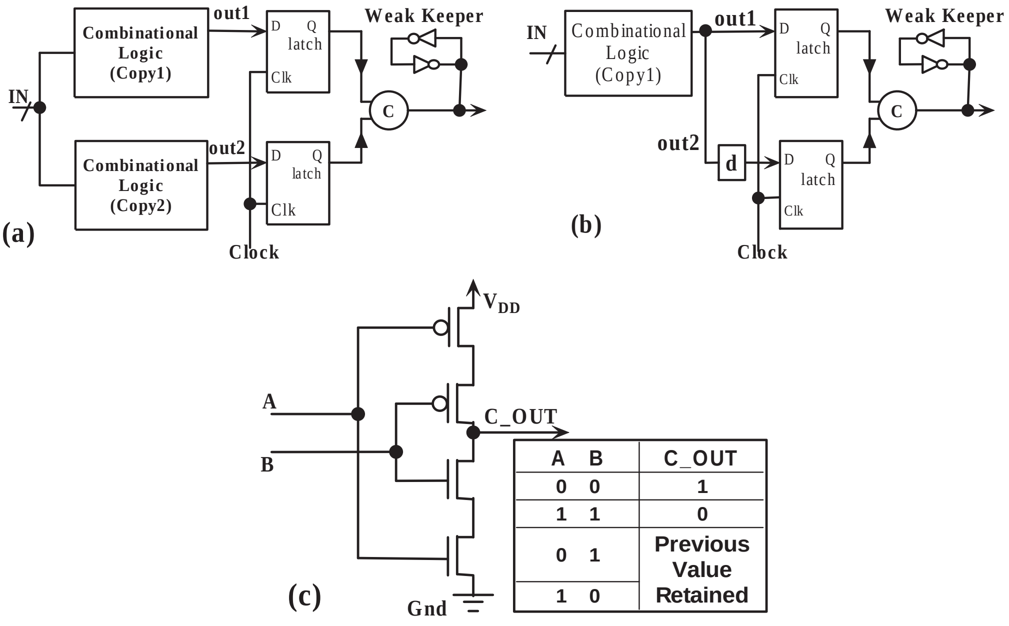

Figure 2.9: Error correction using duplication, (a) space redundancy structure, (b) time redundancy structure, and (c) C-element [127].

During the write operation, a parity generator computes parity bits for the data to be written. The parity bits are written into memory along with the data. If a particle strike alters the state of a single bit of a memory word, now including the parity bits, the error can be discovered by checking the parity code during the read operation. Depending on the number of parity bits used, this scheme can detect errors, and correct them as well. Such schemes are often combined with system-level approaches for error recovery [136]. In most situations, however, the error recovery in a memory is more complex so protection of the memory by means of codes like error correcting code (ECC) is preferable. Table 2.4 [106] summarizes sample error detection and correction (EDAC) methods for memory, data and systems [106].

Table 2.4: Sample EDAC methods for memory or data devices [106].

| EDAC Method | EDAC Capability |
|---|---|
| Parity | Single Bit Error Detect |
| Hamming Code | Single Bit Error Correct, double bit detect |
| RS Code | Correct consecutive and multiple bytes in error |
| Conventional Encoding | Corrects isolated burst noise in a communication stream |
| Overlying Protocol | Specific to each system implementation |

## 2.6 IBM eServer z990 – A Case Study

The IBM eServer z990 system is designed to detect and recover from both soft and permanent errors [121]. System z990 contains up to four pluggable nodes connected through a planar board in a daisy chain interconnect structure. Each node contains up to 64 GB physical memory and a 32 MB L2 cache for a system capacity of 256 GB memory and 126 MB L2 cache.

In IBM z990 system, microarchitecture-level SEU mitigation features include: extensive use of ECC and parity with retry on data and controls; full SRAM ECC and parity protection; operational retries; microprocessor mirroring, checkpointing and rollback, and some hardware derating techniques. These approaches may be useful for future mainframe, general purpose, and application-specific computing systems.

## 2.7 Traditional SER Testing Methods

Soft-error testing seeks to reproduce and then accelerate the die's real-life environment [93, 118]. Typically a neutron beam accelerator is used to conduct this testing. Because each neutron beam has a specific and complex set of neutron properties, the beams must be carefully qualified to correlate the resulting data with real-time results. Beam qualification includes factors such as energy, spectrum, fluency, and tail-effect correction [39].

A schematic overview of the accelerated test setup is shown in Figure 2.10 [86]. The results of this accelerated test are soft error rate. A general test plan for alpha or neutron accelerated SER testing contains multiple runs for the following specifications [86, 92]:

- Supply voltage ($V_{DD}$)
- Input patterns (All 1s, All 0s, or checkerboard)
- Operational frequency (static or dynamic)
- Temperature

The standard procedures and requirements for terrestrial SER testing of ICs should follow the semiconductor industry's accelerated testing methods. The JEDEC (*Joint Electron Device Engineering Council*) standard includes JESD89, JESD89-A [4, 5, 10] and JESD89-2. In JESD89 [4], the standard specifications cover soft errors due to alpha particles and atmospheric neutrons. Also, the standard requirements and procedures for terrestrial SER testing of integrated circuits, and the standardized methodology for reporting the results of the tests are defined. For example, these standards specify that, the SER data obtained from accelerated alpha SER tests should be extrapolated to

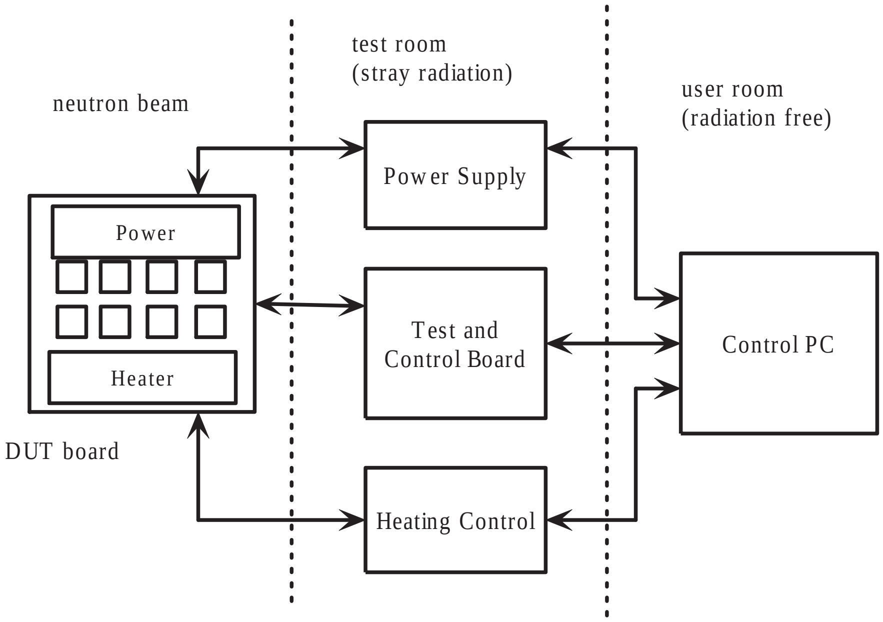

Figure 2.10: Typical test setup (hardware) for neutron-accelerated SER testing [86].

an alpha flux of 0.001 particles/hr-cm$^2$ and the accelerated neutron SER ($ASER$) test results to the typical neutron flux observed at New York City. For that location, the reported data shows that for an energy range from 10 to 10000 MeV, the neutron flux is $3.9\times10^{-3}$ N/cm$^2$-s; and for energy range from 1 to 10 MeV the neutron flux is $4.0\times10^{-3}$ N/cm$^2$-s [86, 4]. Primarily, the procedures apply to memory devices like DRAMs and SRAMs, and with some adjustments they may be used for logic devices [4].

Real-time testing offers another means for soft-error rate detection. However, given that neither single-event upsets nor soft-error-induced latch-ups occur frequently, testers employ environmental acceleration, such as testing at high altitudes where the neutron flux is stronger while the spectrum remains similar to that at ground level. For example, the test facility at the Jungfraujoch Lab in Switzerland, located at 11,000 feet, can accelerate sea-level test times by a factor of 11. In testing conducted at this lab, iRoC

Table 2.5: Accelerated testing versus real-time testing [128].

| Test Type | Logistics | Time | Accuracy | Devices Under Test |
|---|---|---|---|---|
| Accelerated | Complex: Require qualified beams access;<br>expert team required | Average: 2 to 3 months | Good | Memories, SoC, FPGA<br>system level |
| Real-Time | Reasonable | Average: 4 to 6 months | Excellent | All Types |

Technologies obtained a statistically significant number of soft errors on several devices over a period of 4 to 6 months and the tests for soft-error rates covered several different phenomena, including multibit upsets [128]. Table 2.5 [128] shows the advantages of accelerated testing over real-time testing.

The test results show that, the average FIT per megabyte slightly decreases at each process node. From 130nm down to 90 nm, the FIT per megabyte in memory begins to stabilize. Silicon test results show that the average soft-error rate hovers around 1,000 FIT per megabit (neutron and alpha).

Field test is the measurement of the soft error rate of chips due to natural background radiation [142]. This type of testing is frequently used in the evaluation of chip SER by using a tester containing hundreds of chips and evaluating their fail rate at nominal conditions. Field testing is very expensive and may take up to a year to obtain reliable results, but it is used to validate modeling and used in accelerated testing [150]. The traditional SER test needs the parameters shown in Figure 2.11, in which cross section (see Appendix A) is the corresponding interaction probability in the process of computing the interactions of particles of interest with pertinent materials. The fail cross section specifies the sensitivity of a circuit [78]. For a memory, it is determined

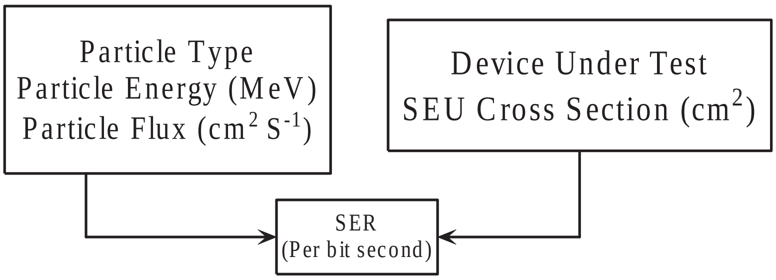

Figure 2.11: Traditional SER field test parameters.

by loading the memory with a known bit pattern and measuring the number of flipped bits when the device is exposed to a beam of neutrons or charged particles. For particle energy $E$, the bit fail cross section, $\delta(E)$, is the measured number of bit flips (or fails) per bit per beam fluence (particles per unit area) [72]:

$$\delta(E) = \frac{fails}{bits \times fluence} \tag{2.4}$$

The soft-error rate (SER) is then determined by integrating the product of the bit cross section and the differential flux over the energy range where the circuit is susceptible to fail when $\Phi$ is beam fluence:

$$SER = \int \delta(E)(\frac{d\Phi}{dE})dE \tag{2.5}$$

At different altitudes, different particles play major roles. Also, the particle flux and energy spectra differ. SER can also be obtained by computer simulation. In a typical SER simulator, radiation environment can be described by either an alpha or a neutron energy spectrum. Neutrons do not possess electrical charge so the only way to cause an SEU is by a nuclear reaction with nuclei of $Si$, $B$, or some other element. The probability

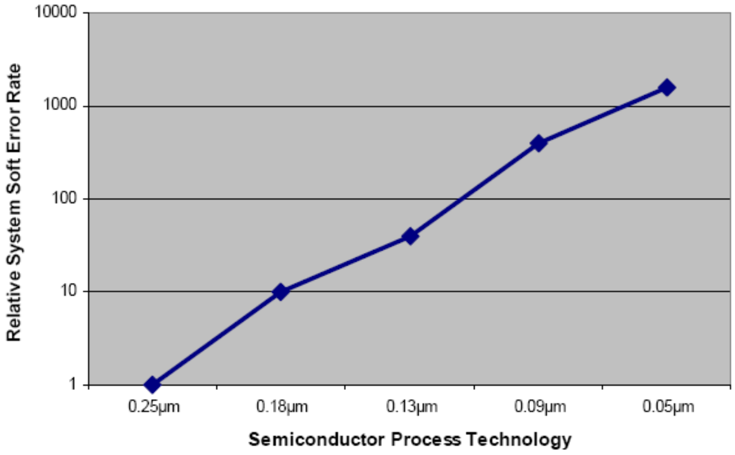

Figure 2.12: Soft error rates as a function of IC process technology [7].

of a neutron producing a nuclear recoil or fragment to which a particular device is sensitive depends on the neutron's energy. Also, the critical charge (see Appendix A) [68, 83, 102] for the circuit node should be measurable.

The sensitivity of an integrated circuit to an upset also depends on the process technology. As semiconductor processes advance to smaller feature sizes, the amount of charge required to cause an upset decreases. The relationship between the process technology and the upset rate is illustrated in Figure 2.12 [7]. Note that this chart includes alpha particle effects as well as neutron effects.

## 2.8 Collected SER Field Test Data

In Table 2.6 [3], recent SER test results are collected from the published literature [11] and some other relevant sources. It can be concluded that from 1000 to 5000 FIT per Mbit for memory would be a reasonable error rate for modern memory devices.

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[3] The question marks in this table mean the relevant data is not available.

Table 2.6: Recently reported data on soft error rates.

| **Type of Memory** | **Reported SER** | **Error per bit-hour** | **FIT/Mbit** | **Source** |
|---|---|---|---|---|
| Goal for new Cypress products | 200 FIT | ? | ? | [3] |
| SRAM (quoted by vendors) | 200 to 2,000 FIT | ? | ? | [2] |
| “typical” | 1,000 FIT | ? | ? | [3] |
| DRAM at full speed | Few hundred to few thousand FIT | ? | ? | [8] |
| SRAM at 0.25 micron and below | 10,000 to 100,000 FIT | ? | ? | [8] |
| Commercial CMOS memory | 1E-5 to 1E-7 per bit-day | 4E-7∼4.2E-9 | 4 million<br>400 million | [3]<br>[170] |
| “some”0.13-micron technologies | 10,000 or 100,000 FIT/Mbit | 1E-11∼1E-10 | 10,000∼100,000 | [3] |
| 1 Gbit memory in $0.25\mu$m | One error per week | 6E-12 | 6,000 | [88] |
| 4M SRAM | <1E-10 upset/bit-day | <4.2E-12 | 4,200 | [140] |
| 1 Gbit of DRAM (Nite Hawk) | 2.3E-12 upset/bit-hour | 2.3E-12 | 2,300 | [1] |
| SRAM and DRAM | 1∼2E-12 upset/bit-hour | 1∼2E-12 | 1,000∼2,000 | [1] |
| ∼8.2 Gbits of SRAM (CRAY YMP-8) | 1.3E-12 upset/bit-hour | 1.3E-12 | 1,300 | [1] |
| SRAM | 1,000 FIT/Mbit | 1E-12 | 1,000 | [77] |
| 256 MBytes | One error per month | 7E-13 | 700 | [44, 8] |
| 160 Gbits of DRAM (Fermilab) | 2.5 errors per day | 7E-13 | 700 | [1] |
| 32 Gbits of DRAM (CRAY YMP-8) | 6E-13 upset/bit-hour | 6E-13 | 600 | [1] |
| MoSys 1T-SRAM (no ECC) | 500 FIT/Mbit | 5E-13 | 500 | [98] |
| Micron estimate, 256 MBytes | 2–4 error per day | 1.2∼2.4E-13 | 120∼240 | [8] |
| “ultra-low” failure rate | 50 to 100 FIT/Mbit | 5E-14∼1E-13 | 50∼100 | [45] |

# CHAPTER 3

# PREVIOUS WORK

The soft error rate estimation predicts the soft-error rates (SER) due to cosmic and high-energy particle radiation in integrated circuit chips by building up accurate SER models [114]. Single event upset phenomenon is a complex process. When neutrons strike silicon, any of more than 100 different nuclear reactions can be generated [128]. Accurate measurement of the neutron flux [72] and its energy distribution are the first considerations in estimating neutron-induced SER. The existing basic concepts and methodologies to estimate cosmic ray induced SER for a given circuit are summarized in this chapter.

## 3.1 Figure of Merit Model for Geosynchronous SER

As discussed in the previous chapter, the error rate $E_r$ is proportional to the integral of the product of the appropriate incident particle flux and the SEU cross section. For spacecrafts in geosynchronous orbits, the appropriate flux $\Phi$ is due to galactic cosmic ray ions. The altitude of these spacecrafts is at the outer fringes of the Van Allen Belt, so their proton-SEU interactions are assumed to be negligible [123]. The Figure of Merit (FOM) Model expressions are obtained by using the chord distribution function for the cross section. Suppose $\Phi(L)$ is the integral SEU flux expressed as number of particles $cm^{-2}day^{-1}$, then the error rate is:

$$E_r \sim \int_{LET_{min}}^{LET_{max}} \Phi(L) d\sigma_u(L) = \int_{LET_{min}}^{LET_{max}} \Phi(L) \frac{d\sigma_u(L)}{dL} dL \; errors \; per \; day \qquad (3.1)$$

where E$_r$ is error rate and $LET_{min}$ and $LET_{max}$ are minimum and maximum linear energy transfer values for the given environment.

The figure of merit (FOM) method provides a single number to roughly estimate the device SEU rate in almost all orbits. After a complex mathematical derivation (for details, see [123]), the figure of merit formula for estimating geosynchronous SEU is given as [25, 148]:

$$E_r = 5 \times 10^{-10} \frac{\sigma_{sat}}{L_c^2} = 5 \times 10^{-10} \frac{abc^2}{Q_{crit}^2} \tag{3.2}$$

where $\sigma_{sat}$ is the saturation device cross section and *a, b* and *c* are dimensions of the approximated parallelepiped sensitive area. The $Q_{crit}$ is the critical charge (see Appendix A for its definition), and $L_c = Q_{crit}/c$, where c is the flat-plate capacitance of the sensitive region. The dimension of SEU error rate $E_r$ is per sensitive region per unit time, where *a, b,* and *c* are given in microns and $Q_{crit}$ in *picocoulomb*. Additional numerical expressions for proton-based, neutron-based and alpha-particle-induced SEU error rate can be found in [123].

**Example: SER Estimation from Figure of Merit Method** [123]

For a particular 1K SRAM, from experiment data the individual SEU sensitive region has dimensions approximately 3×10×10 $\mu$m$^3$ and it is modeled as a $0.05pf$ flat plate capacitor. From manufacturer's specification sheet for this SRAM, the cell $V_{OH} = 5.5V$ and $V_{OL} = 2.5V$. Calculate SEU error rate per cell-day for this SRAM by figure of merit equation.

**Solution:** The cell critical charge is $Q_{crit} \approx C \cdot \Delta V = 0.05 \times 10^{-12} \times (5.5 - 2.5) = 0.15pC$. From figure of merit we can get $E_r = 5 \times 10^{-10} \times \frac{abc^2}{Q_{crit}^2} = 5 \times 10^{-10} \times \frac{(10)\times(10)\times(3)^2}{0.15^2} =$

$2 \times 10^{-5}$ errors per cell per day. For this SRAM, suppose on an average half of the cells are biased so as to be SEU susceptible at a given time, then $\frac{1}{2} \times (1.024 \times 10^3) \times (2 \times 10^{-5}) = 1.024 \times 10^{-2}$ errors per device per day.

Due to the lack of accuracy in the FOM formula and the fact that the sensitive region data for electronic devices is hard to obtain, computer programs have been developed for higher orders of accuracy.

### 3.2 Computer-Based Programs

Some commonly used computer models [172, 173] for calculating soft error rate are SEMM, CHIME and CREME96.

**SEMM** is Soft-Error Monte Carlo Modeling program developed by IBM. It calculates the soft-error rate of semiconductor chips due to ionizing radiation, primarily for determining whether chip designs meet SER specification requirements. The inputs are detailed circuit layout and process information and circuit $Q_{crit}$ values [172].

**CHIME** (CRRES/SPACERAD Heavy Ion Model of the Environment) is a significant tool mainly supported by U.S. Air Force and Office of Naval Research grants. CHIME was developed for the calculation of single event effects due to interplanetary heavy ions, and a set of relevant models to calculate energy deposit (LET) spectra to resulting single event upset rates. This model incorporates the most accurate and up-to-date database currently available for galactic cosmic rays over the past two solar cycles. Also, it provides a predictive model for these fluxes through the next two solar activity minima, to the year 2010 [49].

**CREME96** (Cosmic Ray Effects on Micro Electronics 1996 version) is a widely-used design tool in the aerospace industry. It was developed by Naval Research Laboratory [178]. Its main purposes include:

- Creating numerical models of the ionizing radiation environment in near-Earth orbits;
- Evaluating the radiation effects on electronic systems in spacecrafts and in high-altitude aircrafts;
- Estimating the high LET radiation environment within manned spacecrafts.

The CREME96 program takes advantage of the exact multi-term expression for the chord distribution by numerically integrating without proceeding to FOM Equation 3.2. Also, this program contains up to a dozen environment options [123].

## 3.3 Analytical Models

A circuit level SER analysis can be performed at many levels, from the numerical device simulation level to the abstractions of architectural derating [85, 112, 131, 189]. Accurate estimation of nominal SER is important for circuit level SER estimation and this step lies in the middle of a variety of levels of SER simulation, ranging from device characterization to system level analysis [184]. The SER of a design is defined in terms of the nominal soft-error rates of individual elements such as SRAMs, sequential elements such as flip-flops and latches, and combinational logic, that depend on the circuit design and the architecture [128]:

$$SER^{design} = \sum_{i} SER_i^{nominal} \times \text{Prob(error in ith circuit produces a system error)} \quad (3.3)$$

where the $SER_i^{nominal}$ refers to soft error rate of the $i_{th}$ element in the circuit when all inputs and outputs of the element are constant. For example, it can be a node or an SRAM cell in the circuit; $SER_i^{nominal}$ is independent of the input vectors that activate this element [128]. Generally, the $SER_i^{nominal}$ value can be obtained by the soft error testing method illustrated in Section 2.7.

We define the following terms [133, 134]:

**Nominal SER** is the probability of a SEU occurring at a specific node. It depends on circuit technology, transistor sizing, node capacitance, $V_{DD}$ value, and temperature. It is independent of the state of input vectors that drive the node.

**Timing Derating** is the fraction of time in which the circuit is susceptible to SEU that propagates the SEE-induced pulse through the flip-flops. The susceptibility of the timing window will be discussed later in this section. The timing derating increases with increasing clock frequency. The timing vulnerability factors of sequential elements have been examined in [165].

**Logic Derating** (LD) is a measure of how the device logically reacts to a particle strike. LD depends on the design architecture and input stimulus causing an activated path for error propagation to primary outputs without logical masking of the error pulse.

**Electrical derating** is the electrical property of a device that degrades the error pulses passing through it. An SEU is electrically masked if the signal is attenuated by the electrical properties of gates on its propagation path such that the resulting pulse is of insufficient magnitude or width to be latched [133]. Electrical masking plays an important role in soft error rate estimation for combinational logic. In experimental results on a small circuit having a logic depth of five gates, ignoring electrical masking effects is known to cause an overestimation of the SER by 138% [67].

The main factors that influence the scaling of nominal FIT are as follows [134]:

1. Diffusion area: The probability of SEU on a specific node is roughly proportional to the area of the diffusion region for that node since the charge separation occurs near the diffusion areas.

2. Charge scaling: Keeping up with the technology trend, the capacitance per node and the supply voltage are decreasing, hence less charge is needed for the state of the node to flip. Charge scaling dominated the SER trend in the old process to make the SER sensitivity increase every generation. However, in recent deep submicron technologies, many circuits such as memory cells are flux limited or saturated. In such cases, process scaling reduces the diffusion area but does not increase the circuit sensitivity.

3. Voltage scaling: Voltage scaling has historically contributed to a trend of increasing soft error sensitivity with process evolution. But in recent process generations voltage scaling has lagged process dimension scaling contributing to decline in FIT per bit for 90nm and 65nm memory technologies [134].

4. Process advances: Such as SOI or similar partial or fully depleted layers significantly reduce the charge collection volume and efficiency leading to reduced sensitivity to soft errors. SER sensitivity is also impacted by details of doping profiles and doses. IBM reported a five times improvement in FIT rate for partially depleted SOI for SRAM cells at 90nm [76]. No data has been reported for latches.

5. Flux of alpha particles: The flux of alpha particles strongly depends on the amount of radioactive residues and placement of metal layers in the package. Cleaner materials and more metal layers tend to reduce the flux, thus alpha particles become less of an issue in modern processes. However, alpha articles do impact nodes with very small charge, so the sensitivity to alpha particles increases every generation except for flux-limited circuits.

In a real case, the combinational SEU error rate estimation is complex because it is related to gate types and paths the SEU propagates through. A comparative study has been presented between the $Q_{crit}$ method and the simulation method for estimating the circuit level SER [112]. In that work it is shown that for small circuits with uniformly distributed output values (e.g., flip-flop, binary counter), both methods provide similar estimates for SER.

SER analysis for logic circuits poses a challenge for electronic reliability analysis. Unlike memories, the soft errors occurring inside the logic circuit may be filtered out by the circuit itself and thus may not effect the circuit performance as discussed in previous sections. Analytical methods are widely used to model soft errors probabilistically. Asadi *et al.* [16, 17, 18] present a soft error rate estimation technique based on error probability propagation. Rejimon and Bhanja [159, 160] give a single event fault model based on probabilistic Bayesian networks, which captures spatial dependencies. Hayes *et al.* [80] present a framework for modeling transient-error tolerance in logic circuits. However, these approaches do not take the electrical masking into account and characteristics of transient pulses like pulse width are ignored.

An improvement was provided by Zhao *et al.* [194, 195]. They proposed a constraint-aware robustness insertion methodology that protects the sequential elements in digital circuits to suppress various noise effects. Their noise probability density function represents the distribution of noise that has survived circuit masking effects at internal nodes to reach the flip-flops as determined by a probability matrix mapping. However, in that work the authors did not include the environmental factors like the error rate. Besides, their propagation method requires tabulating all pulse width and height data for each logic gate. It would thus take enormous amount of memory for large logic circuits.

A closed-form model for simulation and analysis of voltage transients caused by SEU in logic circuits provides an accuracy within 5% of the result obtained from SPICE with over 100X improvement in computational speed [129]. Ramanarayanan *et al.* [155] analyze soft error rate in flip-flops and scannable latches. Hazucha *et al.* [81, 84] proposed an empirical model for estimation of SER induced by neutrons. The dynamic behavior of a circuit with massive critical paths in the presence of an SET has been studied and a novel flip-flop architecture to mitigate the effects of such SETs in combinational circuits proposed [91]. Logic circuit SER estimation systems include SEAT-LA [153], SERA [193] and that described by Rao *et al.* [156].

A recent paper [124] proposes an approach using symbolic analysis based on binary decision diagrams (BDD), algebraic decision diagrams and a probabilistic model for sequential SER analysis. Rewriting, extensively used for optimizing the area and power consumption, has been found to also reduce the soft error rate [14]

The production and propagation of single-event transients in scaled CMOS digital logic circuits have been widely examined in [51, 61, 63]. In [63], Three-dimensional mixed-level simulation is used to study both bulk CMOS and silicon-on-insulator (SOI) technologies for scaling trends to the 100nm technology node.

The impact of variations, such as variations in device parameters caused by static process variations, dynamic variations in power supply, temperature and slow degradation of individual devices due to phenomena like hot carrier injection (HCI) and negative bias temperature instability (NBTI) on soft error vulnerability for nanometer VLSI circuits is studied in [152, 154]. The increasing variability not only affects the behavior of contemporary ICs but also their vulnerability to transient error phenomena, especially radiation induced soft errors. The device threshold voltage can also play a significant role in soft error rate estimation [56].

The algorithmic techniques of formal verification, used for design debugging [166], can also be used to estimate vulnerability to reliability problems and to reduce overheads of circuit mechanisms for soft error resilience. One technique for synthesizing multilevel circuits with concurrent error detection is presented in [177].

Timing redundancy and space redundancy based soft-error tolerance techniques for nanometer technologies have been presented [15, 126, 127, 128, 135]. Timing redundancy based scan flip-flops are reused to reduce the SER of combinational logic, thus approaching the goal to minimize the area overhead of radiation hardening [64].

FPGAs have become prevalent in critical applications where transient faults can seriously affect the system operation. The fault tolerance techniques for transient and permanent faults in SRAM-based FPGAs have been presented in [55, 96]. A good summary of fault tolerant techniques for FPGAs can be found in [100]. Besides FPGA systems, radiation hardened micro-controller techniques are presented [54, 108, 143, 188].

Soft-error/noise tolerant techniques are necessary for maintaining the signal-to-noise ratio (SNR) in critical DSP applications. The checksum-based probabilistic error correction method uses the value indicated by the checksum variable to probabilistically correct the error and achieves up to 5 dB improvement in SNR [19, 20]. System level self-checking and self-diagnosing techniques are proposed in [191] for 32-bit microprocessor and multipliers.

A cost effective radiation hardening technique, which exploits the hardening gates that have lowest logical masking probability to achieve tradeoffs between overhead and soft error failure rate reduction, is presented in [196, 197]. More hardening techniques can be found in [53, 116]. Gate sizing may be another possible approach to increase the transient error tolerance as illustrated in [59].

An approach to minimize the impact of soft errors in domino logic by using complementary pass transistors and an additional weak keeper to selectively isolate the logic gates struck by cosmic rays is studied in [104]. This error suppression approach comes with no extra power consumption and with modest area (2.6%) and delay (13.6%) overheads.

A cost effective approach to design logic circuits with concurrent error detection by exploring the asymmetric soft error susceptibility of nodes has been described [130]. Combinational logic error analysis and protection schemes are studied in [138].

Inspired by the principles of immunology, a hardware immune system has been demonstrated. This hardware immune system runs in real-time and continuously monitors a finite state machine (FSM) architecture for errors [36, 37].

The impact of technology scaling on soft error rates can be found in [27, 169]. Effects of CMOS technology scaling and the atmospheric neutron caused soft error rates have been investigated [82].

# CHAPTER 4

# ENVIRONMENT-BASED PROBABILISTIC SOFT ERROR MODEL

This chapter is an original contribution of the present research. Distinct from memories, in a logic circuit a single event effect (SEE) exists as a single event transient (SET) pulse. An SET has unique characteristics like polarity, waveform, amplitude and duration, and these characteristics depend on particle impact location, particle energy, device technology, device supply voltage and output load. A single event upset (SEU) does not occur unless the SET can survive the circuit masking effects and is captured by a clock edge into a sequential element. The SET can be eliminated by electrical masking, logic masking and temporal masking [128, 133].

Environmental neutrons, the principal cause of these transients, come from cascaded interactions when galactic cosmic rays traverse through earth's atmosphere. These neutrons reach the ground with finite probabilities. The neutron flux is usually in units of $N/cm^2$-$s$, where $N$ is the number of neutron particles. The intensity of cosmic-ray induced neutron flux in the atmosphere varies with altitude, geomagnetic field, and solar magnetic activity. The flux data are available from observations accumulated over decades [123, 199]. One often cites the JEDEC standard [4].

Each neutron has a unique energy when it arrives at the ground. The particle does not induce an error itself, it is the interaction that causes the error in electronic materials. The neutron energy is one of the key properties here; we neglect the effects of angle of incidence of the particle strike. Not every particle hits on the sensitive silicon area to induce an error. An SEU occurs with certain probability for each high-energy

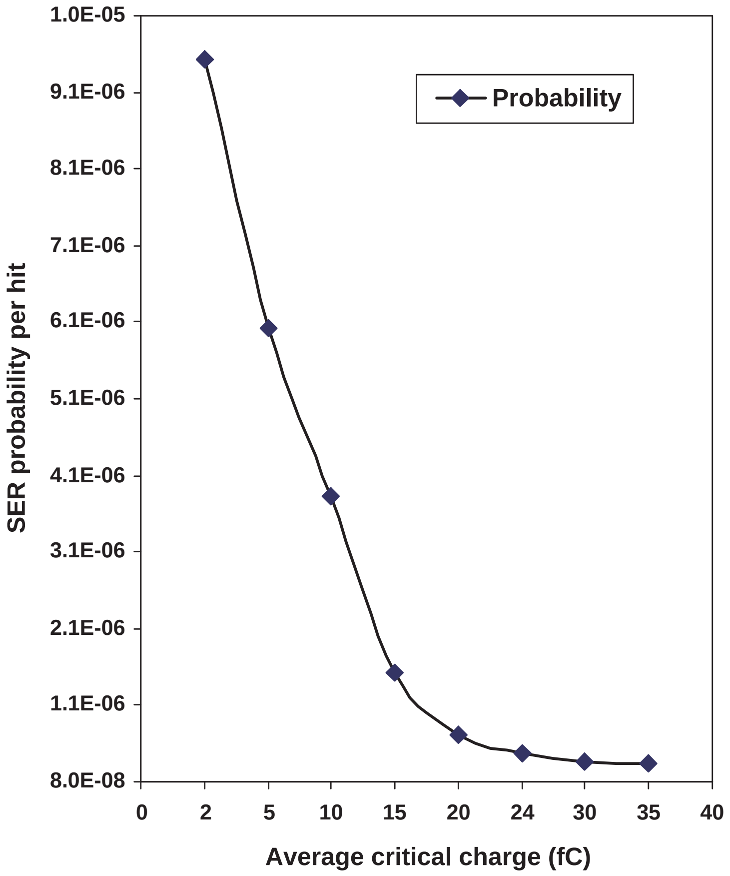

Figure 4.1: Probability of soft error for each collision of a 30MeV neutron as a function of the average critical charge for an SRAM chip (from SEMM program [172]).

particle hit. Such probability can be obtained from existing computer programs, for example, IBM's SEMM. Figure 4.1 [172] shows the result when a CMOS SRAM chip was simulated for 30-MeV neutron hits. The probability of SEU is a function of the particle energy and the critical charge. In the circuit design process, once a circuit is laid out, the critical charge for each cell is defined. Although we did not use the SEMM program in our experiment on logic circuits, we mention it to illustrate how the error probability can be derived.

To consider all energy components in our proposed soft error model, we average the error probability over different energies and assign each circuit node a unique error probability value. The particle energy distribution under specific locations for specific technology nodes can be obtained from experimental results. For example, the cosmic particle strikes were simulated using a heavy ion beam at the Twin Tandem Van de Graaff accelerator at Brookhaven National Laboratory and the results suggest that in the natural environment of space the probability distribution of high-energy particles falls rapidly with increasing $LET$. For both $0.5\mu$ and $0.35\mu$ CMOS technology processes at the ground level, the largest population has a linear energy transfer ($LET$) of $20MeV$-$cm^2/mg$ or less and the particles with $LET$ greater than $30MeV$-$cm^2/mg$ are exceedingly rare [78]. The $LET$ of a striking particle multiplied by a characteristic length of the material gives the charge accumulated due to the strike. These results are used in our experiments in Section 4.2.

In addition, from the statistical energy distribution we are able to model the statistical SET widths in logic circuit by applying the $LET$ values to the commonly used transient current double-exponential model [122]:

$$\begin{cases} I(t) = \frac{Q_{coll}}{\tau_\alpha - \tau_\beta}(e^{-\frac{t}{\tau_\alpha}} - e^{-\frac{t}{\tau_\beta}}) & \text{(a)} \\ Q_{coll} = 10.8 \times L \times LET & \text{(b)} \end{cases} \tag{4.1}$$

where $Q_{coll}$ is the collected charge in the sensitive region, $\tau_\alpha$ is the collection time constant, which is a process-dependent property of the junction, and $\tau_\beta$ is the ion-track establishment time constant, which is relatively independent of the technology. In bulk silicon, a typical charge collection depth ($L$) is $2\mu$ for every 1 $MeV$-$cm^2/mg$, and an

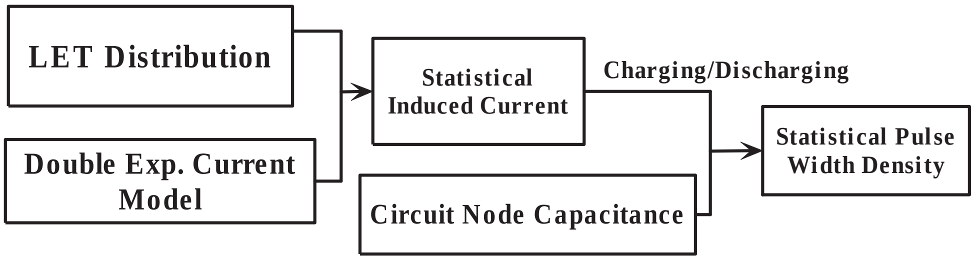

Figure 4.2: Transforming statistical neutron energy spectrum to SET width statistics.

ionizing particle deposits about $10.8fC$ charge along each micron on its track. Typical values are approximately $1.64 \times 10^{-10} sec$ for $\tau_\alpha$ and $5 \times 10^{-11} sec$ for $\tau_\beta$ [43, 194].

From Equation (4.1), the transient current pulse created by a particle strike for each given LET can be calculated. By charging and discharging the circuit node capacitance, the single event transient current pulse is converted into a transient voltage pulse in Figure 4.2. Following the preceding discussion, Figure 4.3 gives a neutron-induced soft error model for logic circuits. Because the probability per hit is related to the neutron flux which is location dependent, we can easily get the circuit SER in units of $FIT$ for different locations if the corresponding neutron flux data are available.

In summary, this probabilistic soft error model is based on two considerations: (1), the occurrence of SEUs, presented as the soft error frequencies and (2), once an SEU occurs, it exists in the logic circuit as SETs with different pulse width densities represented as probability density functions. Note that the pulse width is not the pulse duration between its half peak-peak values, but is the half of the power supply value in the logic circuit.

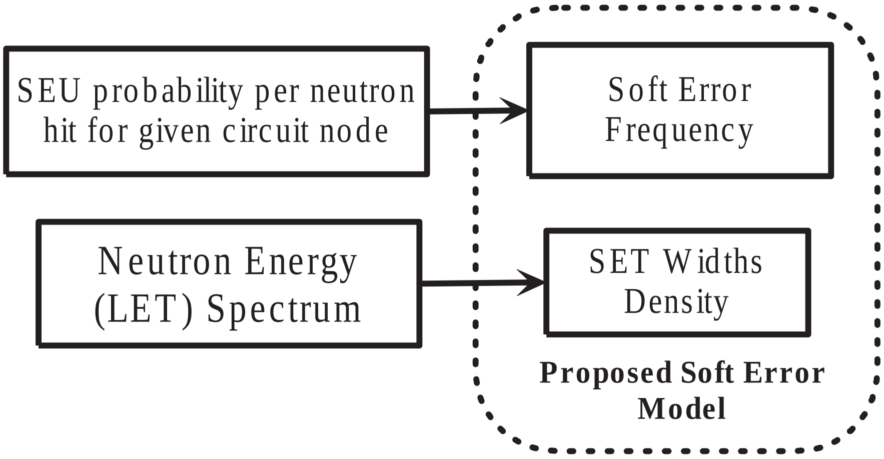

Figure 4.3: Proposed probabilistic neutron induced soft error model for logic.

## 4.1 Gate-Level SET Propagation

Having discussed the modeling of soft errors by two factors (occurrence rate and density), we will now discuss the propagation of errors through a logic gate.

### 4.1.1 Pulse Widths Probability Density Propagation

Assume that the input SET width is a random variable $X$ with probability density function $f_x(X)$, the SET pulse width density function $f_y(Y)$. Suppose the function $g$ expresses the relationship between variable $X$ and variable $Y$: $Y = g(X)$. Given the probability density function of the input pulse width $X$ and the propagation function $g(X)$, we need to find the probability density function of the output pulse width $Y$. In the following derivation, we use the theory of random functions [146].

The pulse width propagation function $g$ for each individual gate is obtained as follows:

$X$ and $Y$ are random variables

$X$: input pulse width, $Y$: output pulse width

$f_X(x)$: probability density function of $X$

$f_Y(y)$: probability density function of $Y$

Given function $g$: $Y = g(X)$, and more specifically,

$g$: $Y = g\{X,\ p : W/L,\ n : W/L,\ C_{load},\ technology\}$

Assume $g$ is differentiable and an increasing function, so $g^{'}$ and $g^{-1}$ exist. Then,

$$\int_{x}^{x+\Delta x} f_X(s)ds = \int_{y}^{y+\Delta y} f_Y(t)dt$$

$\Longrightarrow \qquad f_X(x)\Delta x = f_Y(y)\Delta y$

$$\begin{aligned} \text{i.e., } f_Y(y) &= \lim_{\Delta x \to \infty} f_X(x)\frac{\Delta x}{\Delta y} \\ &= \lim_{\Delta x \to \infty} f_X(x)\frac{1}{\Delta y/\Delta x} \\ &= \frac{f_X(x)}{g^{'}(x)} \end{aligned}$$

$\Longrightarrow \qquad f_Y(y) = f_X(x)/g'(x)$

The pulse width propagation depends on the load capacitance and the induced soft error pulse at the input of the gate will propagate only if the affected node is on a sensitized path of the circuit. Load capacitances are generally determined from the layout. Since, we did not have the physical layouts of benchmark circuits, we used a wire-load capacitance model [171, 190]. Wire-load models estimate capacitance of a net by its pin-count and the technology data. In its simplest form, the load capacitance of a gate can be estimated as the technology-dependent nominal gate delay multiplied by $(1 + number\ of\ fanouts)$. Our analysis, however, is not limited to using wire-load models and more accurate capacitance data, if available, can be readily used.

First consider a CMOS inverter as an example. Suppose we have a positive glitch (0 to 1 and 1 to 0 transitions separated by a glitch-width interval) at the input. We evaluate the output and, as expected, there will be a negative glitch there. The output width will, however, vary depending on load capacitance and the technology-dependent transistor characteristic, which provide inertial delay to the inverter.

For a general multiple input logic gate, a glitch at an input may propagate to the output only if the affected node is sensitized to the gate output. For example, for a NAND gate with a glitch of certain width on one of its inputs, if any other input is at logic 0 then no matter how wide the input glitch is it will not get through the gate because there is no sensitized path. Even when all other inputs are at 1, the input glitch should be wide enough to overcome the inertia of the gate and propagate to its output. Moreover, unless the glitch can propagate through all gates on a path to a primary output, it will not affect the correct operation of the circuit.

We should remember that in our analysis, single event transient pulses are randomly induced at gates. The probability of a pulse being induced at a gate output depends on the probability of a neutron strike at sensitive regions in that gate. The width of the pulse is then a random variable whose probability density is determined from the $LET$ distribution of the striking neutron, technology-dependent gate characteristics and the output node capacitance. Next, given a pulse is induced, its propagation to next gate toward the primary output will depend on signal values. Thus, signal probabilities will determine the probability of pulse propagation. In addition, the transfer functions of gates (denoted as $g()$) will determine the probability density function for the propagated pulse width.

From HSPICE simulation we find that the function $\boldsymbol{g}$ is a nonlinear transmission function. However, a piecewise-linear "3-interval" propagation model can give a good approximation. Given a sensitized path of a generic gate, depending on the input pulse width ($D_{in}$) and the gate input-output delay there are three intervals of possible input glitch durations that can be identified [32, 144].

Thus, for a generic logic gate, the pulse width propagation model is:

1. Propagation with no attenuation, if $D_{in} \geq 2\tau_p$.
2. Propagation with attenuation, if $\tau_p < D_{in} < 2\tau_p$
3. Non-propagation, if $D_{in} \leq \tau_p$.

Where

- $D_{in}$: input pulse width. Also represented by random variable $X$
- $D_{out}$: output pulse width (to be determined). Also represented by random variable $Y$
- $\tau_p$: gate input to output delay

We validate this propagation model by simulating a CMOS inverter using HSPICE. The results are shown in Figure 4.4. This CMOS inverter is in TSMC035 technology with nMOS W/L ratio = $0.6\mu/0.24\mu$ and pMOS W/L ratio = $1.08\mu/0.24\mu$. At the gate output, rising delay

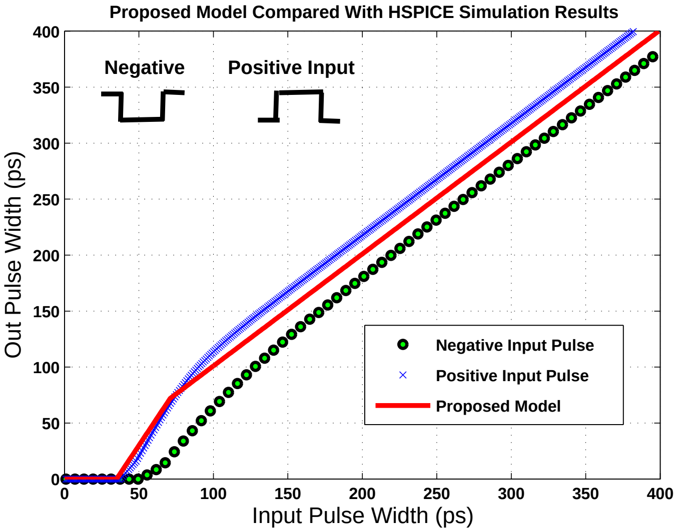

Figure 4.4: Comparison of proposed model and HSPICE simulation for CMOS inverter with $10fF$ load capacitance.

was $41.5ps$ and falling delay was $30.8ps$ for load capacitance of $10fF$. We use an average gate delay of $\tau_p = 36.0ps$ in the proposed propagation model. The mathematical expression is given in Equation (4.2). In Figure 4.4, the x-axis is the input pulse width and the y-axis is the output pulse width. We observe that when input pulse width is greater than $72ps$, i.e., $2\tau_p$, the output pulse width can be either greater or smaller than the input pulse width, depending on the input pulse type. These differences are caused by different rising and falling delays. Thus, the proposed model is a good approximation to the HSPICE simulation.

$$D_{out} = \begin{array}{ll} 0 & \text{if } D_{in} \leq 36.0ps \\ (D_{in} - 36.0) \times \frac{72.0}{36.0} & \text{if } 36.0ps < D_{in} < 72.0ps \\ D_{in} & \text{if } D_{in} \geq 72.0ps \end{array} \tag{4.2}$$

For this CMOS inverter with an output load capacitance of $10fF$, an illustration of the monotonic mapping of probability density $f_y(Y)$ is given in Figure 4.5. The characteristics of the three regions in this figure are: the input pulse width in regions 1, 2 or 3 will be filtered,

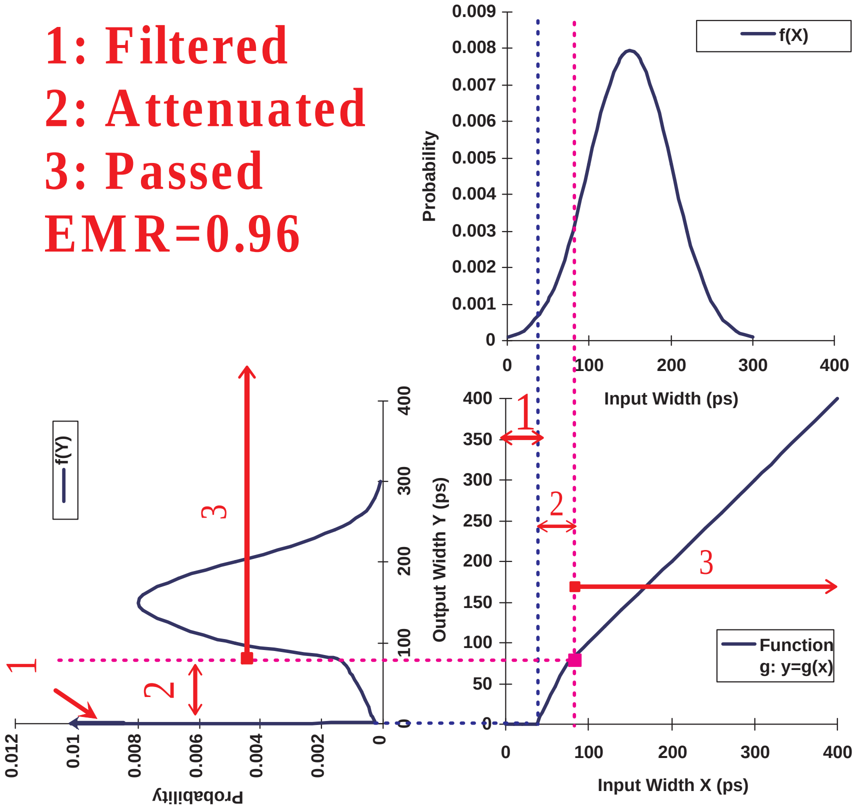

Figure 4.5: Pulse width density propagation through a CMOS inverter with $10fF$ load.

attenuated, or pass without attenuation, respectively. A pulse being filtered actually assumes the shape of a delta function. Similarly, we simulated all gates by HSPICE to extract the gate delays and build the propagation model $\boldsymbol{g}$. Similar agreement as in Figure 4.4 was observed for all other logic gates.

### 4.1.2 Logic SEU Probability Propagation

Because all pulse widths must be greater than or equal to 0, we have

$$\int_0^\infty f_Y(y)dy = \int_0^\infty f_X(x)dx = 1 \tag{4.3}$$

Table 4.1: Output 1 probability calculation for $n$-input Boolean gates.

| Gate | Probability (output = 1) |
|---|---|
| AND | $P_1(out) = \prod_{i=1}^{n} [P_1(in(i))]$ |
| NAND | $P_1(out) = 1 - \prod_{i=1}^{n} [P_1(in(i))]$ |
| OR | $P_1(out) = 1 - \prod_{i=1}^{n} [1 - P_1(in(i))]$ |
| NOR | $P_1(out) = \prod_{i=1}^{n} [1 - P_1(in(i))]$ |

In $f_X(x)$ to $f_Y(y)$ conversion, there is a fraction of pulses that is filtered out or attenuated due to electrical masking (i.e., suppression by gate inertia). We define electrical masking ratio (EMR) as the fraction of pulses that survives propagation in Equation (4.4):

$$EMR = \frac{\int\limits_{y>0} f_Y(y)dy}{\int\limits_{x>0} f_X(x)dx} \tag{4.4}$$

We assume that all signal probabilities are known. This can be done in several ways. If a set of input vectors is given, then a zero-delay logic simulation [41] can easily determine all signal probabilities. Alternatively, signal probabilities can be determined from a static analysis of the primary input probabilities [167]. When no vectors are given, one often assumes equiprobable 0s and 1s at primary inputs. Because signal probability calculation has high complexity, often a simple approximation that ignores correlations between signals at gate inputs may be used. In that case, logic 1 probability calculation rules for $n$-input logic gates are given in Table 4.1. Here, $P_1(in)$ and $P_1(out)$ denote 1-probabilities of input and output signals of the gate. Logic 0 probabilities are obtained simply by complementing logic 1 probabilities. Our SER analysis works with signal probabilities irrespective of how those probabilities were obtained. For the benchmark circuit results we report, we assumed no given vectors and equiprobable inputs. This corresponds to random input vectors. Signal probabilities were calculated in a single input to output pass using the formulas of Table 4.1.

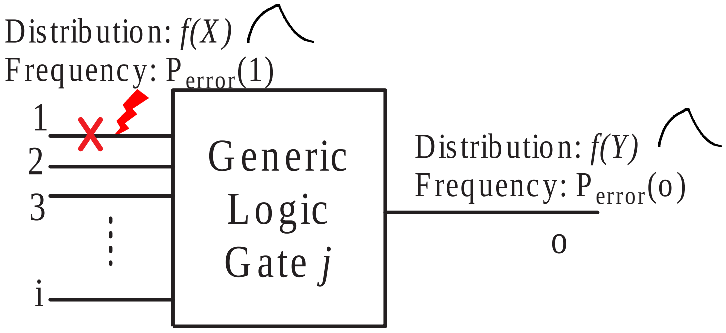

Figure 4.6: A generic gate with particle strike on node 1.

If SEU occurs on input 1 of logic gate $j$ in Figure 4.6 then the output soft error probability is calculated by Equation (4.5):

$$P_{SEU}(o) = P_{SEU}(1) \cdot \underbrace{EMR_j}_{\substack{Electrical\\ Masking}} \cdot \underbrace{\prod_{2}^{i}[P_{non-controlling}(i)]}_{Logic\ Masking} \tag{4.5}$$

Here again, we have assumed that all inputs of the gate are statistically independent. This is an approximation that can be improved [95]. However, we believe that uncorrelated signal assumption will give reasonable accuracy and low computation complexity.

## 4.2 Experimental Results

We analyzed ISCAS85 benchmark circuits and inverter chains of varying lengths by a simulator developed in C programming language. For simplicity, we assume that all the circuits are working at the ground level and the probability of SEU per particle hit is $10^{-4}$. For ground level we use the neutron energy statistics discussed in previous chapters. We assume the SET width density per circuit node follows the *normal* distribution with mean $\mu = 150$ and standard deviation $\sigma = 50$. These assumptions are justified for relatively small value of particle flux and small chip area. From [200], the total neutron flux at sea level is $56.5m^{-2}s^{-1}$. For a CMOS circuit in TSMC035 technology, we assume the sensitive region area is $10\mu m^2$ for each

Table 4.2: SER results for ISCAS85 benchmark circuits.

| Circuit | # PIs | # POs | # Gates | CPU s | FIT/gate /output |
|---|---|---|---|---|---|
| c17 | 5 | 2 | 6 | 0.01 | 0.3679 |
| c432 | 36 | 7 | 160 | 0.04 | 1.0563 |
| c499 | 41 | 32 | 202 | 0.14 | 0.2188 |
| c880 | 60 | 26 | 383 | 0.08 | 0.3882 |
| c1908 | 33 | 25 | 880 | 1.14 | 0.7427 |
| c2670 | 233 | 140 | 1193 | 0.77 | 0.2882 |
| c5315 | 178 | 123 | 2307 | 2.78 | 0.5572 |
| c7552 | 207 | 108 | 3512 | 10.82 | 0.6652 |

Table 4.3: SER results for inverter chains.

| Circuit | # PIs | # POs | # Gates | CPU s | FIT /gate |
|---|---|---|---|---|---|
| inv2 | 1 | 1 | 2 | 0.00 | 0.2819 |
| inv5 | 1 | 1 | 5 | 0.00 | 0.5388 |
| inv10 | 1 | 1 | 10 | 0.00 | 0.9654 |
| inv20 | 1 | 1 | 20 | 0.00 | 1.8185 |
| inv50 | 1 | 1 | 50 | 0.00 | 4.3780 |
| inv100 | 1 | 1 | 100 | 0.04 | 8.6473 |

circuit node. For a circuit with $n$ primary outputs and $m$ gates, the SER per gate per output is $\frac{1}{n}\Sigma_{i=0}^{n}(\frac{1}{m}\Sigma_{j=0}^{m}SER_{i\_caused\_by\_j})$. From Table 4.3 we see that SER increases almost linearly with increasing inverter chain length. That is because in the inverter chain, there is no logic masking and there will always be a portion of SEUs under the current environmental condition that will survive through inverters no matter how long the chain is. But in Table 4.2 for logic circuits, the SER does not increase with the number of gates. The logic masking in these circuits seems to increase with increased number of gates. Field test data for logic circuits is largely unavailable, but actual neutron experiments on a test chip would help to validate our analysis in the future. The CPU times for these results are for a Sun Fire 280R workstation.

## 4.3 Conclusion

In this chapter, we presented a novel soft error model based on two parameters, occurrence rate and single event transient pulse width density for combinational circuits. We developed an algorithm to propagate these parameters through logic and calculate soft error rate in the FIT units. In the next chapter, we will discuss the relevancy of our approach and compare our method with other logic soft error rate estimation methods.

# Chapter 5

# Results Comparison and Discussion

In this chapter, we compare our experimental results with the relevant published work and discuss various key factors that may influence logic SER. Some of those factors have not been considered in the existing logic SER estimation work.

## 5.1 Experimental Results

For the detailed algorithms that propagate soft errors through elementary logic gates and calculate the SER for a circuit, the reader should refer to the previous chapter. Here, we compare our experimental results with previous publications [17, 153, 156, 159, 193].

We simulated ISCAS85 benchmark circuits by a simulator developed in C programming language. For simplicity, we assume that all circuits are working at the ground level and the probability of SEU per particle hit is $10^{-4}$. Here we neglect the polarity of SETs and the temporal masking factor. For ground level we use the neutron energy statistics assuming the SET width density per circuit node follows a *normal* distribution with mean 150 and standard deviation 50. These assumptions are justified for relatively small values of particle flux and small chip area. From [200], the total neutron flux at sea level is $56.5m^{-2}s^{-1}$. For a CMOS circuit in TSMC035 technology, we assume the sensitive region to be $10\mu m^2$ for each circuit node.

For a circuit with $n$ primary outputs and $m$ nodes, the SER is $\Sigma_{i=0}^{n}(\Sigma_{j=0}^{m}SER_{i\_caused\_by\_j})$ which is different from [187] that uses the formula $\frac{1}{n}\Sigma_{i=0}^{n}(\frac{1}{m}\Sigma_{j=0}^{m}SER_{i\_caused\_by\_j})$. Rao et al. [156] and Rajaraman et al. [153] calculated total logic SER. In Table 5.1, we compare our SER results for selected benchmark circuits with available results; not all benchmark circuit SER results have been published. We see our results have large differences when compared with the results from Rao et al.

Table 5.1: Experimental results for ISCAS85 benchmark circuits.

| Circuit | # | # | # | Our approach | | Rao et al. [156] | | Rajaraman et al. [153] | |
|---|---|---|---|---|---|---|---|---|---|
| | PI | PO | Gate | CPU s | FIT | CPU s | (FITs) | CPU min. | Error Prob. |
| c432 | 36 | 7 | 160 | 0.04 | $1.18\times10^{3}$ | <0.01 | $1.75\times10^{-5}$ | 108 | 0.0725 |
| c499 | 41 | 32 | 202 | 0.14 | $1.41\times10^{3}$ | 0.01 | $6.26\times10^{-5}$ | 216 | 0.0041 |
| c880 | 60 | 26 | 383 | 0.08 | $3.86\times10^{3}$ | 0.01 | $6.07\times10^{-5}$ | 102 | 0.0188 |
| c1908 | 33 | 25 | 880 | 1.14 | $1.63\times10^{4}$ | 0.01 | $7.50\times10^{-5}$ | 1073 | 0.0011 |

The order of magnitude differences between results in Table 5.1 need investigation. The published data for SRAMs (see previous chapters) shows SER around 1000 FIT for both analysis and measurement. That is in the same range as our analysis of benchmark circuits. Field test data for logic circuits is largely unavailable and the actual neutron experiments on a test chip in the future will help validate our analysis.

The CPU times for our results are for a Sun Fire 280R workstation. The results in [156] were for a Pentium 4 2.4GHZ machine and those in [153] were for a Sun Fire v210 machine. The run times for our approach are comparable [156] or better [153].

## 5.2 Discussion of Results

In Table 5.2, various methods of analysis are compared. Many factors are listed that influence the calculation of logic SER. However, each of the existing approaches includes only few of them. We make the following observations:

1. The physics of the SEU phenomena seems involved. For example, the analysis of the funneling and the angle of incidence are not considered. We take the energy of neutrons to be the main source that induces the SEU. However, in real cases, it is the physics of interaction between neutrons and silicon that produces the SEU. Simpler modeling and assumptions may influence the SER estimation accuracy.
2. The sensitive region of a transistor is defined as the channel region of an off nMOS transistor or the drain region of an off pMOS transistor. For a CMOS circuit, the "on" or "off" status of transistors is determined from inputs. In our approach, we statically assume that each

Table 5.2: Comparison of our work with other SER estimation methods.

| Authors and Reference | Factors considered | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | LET Spectrum | Re-conv. Fanout | Sensitive Regions | SEU prob. | Vectors Applied | Location Altitude | Circuit Tech. | SET Degradation |
| Our work | yes | no | yes | yes | no | yes | yes | yes |
| Rao et al. [156] | yes | no | no | no | yes | yes | yes | yes |
| Rajaraman et al. [153] | no | no | no | no | yes | no | no | yes |
| Asadi-Tahoori [17] | no | no | no | yes | no | no | no | no |
| Zhang-Shanbhag [193] | yes | no | yes | yes | yes | yes | yes | no |
| Rejimon-Bhanja [159] | no | no | no | yes | yes | no | no | no |

circuit node's sensitive region is $10\mu m^2$. This may bias the SER results. Also, although we have considered the sensitive area of the circuit node, the strikes on pMOS or nMOS influence the polarity of SETs. So, the dynamic state of the circuit may further affect the SER.

3. Compared to the earth surface, the size of the sensitive region of a single transistor or a circuit board is trivially small and is getting smaller with the technology trend. At the surface of the earth we take the probability of a particle strike at a sensitive node simply by taking the ratio of the number of particles strikes/$\mu m^2$-s to strikes/$m^2$-s. Theoretically, it seems correct because note that 1 m$^2$ equals $10^{12}$ $\mu$m$^2$. To imagine this event in real cases, most probably there will be no strike on the sensitive regions but such low probability events can not be neglected. Once the SEU occurs, the circuit SER may easily be several orders of magnitude higher compared to the case of no strike at all.

4. For logic circuits, fan-out details should be considered. In our experiment we only considered the worst case error rate for re-convergent fan-outs. For example, if a re-convergent

fanout has two paths, and one passes through more gates compared to the other, our program only takes the path that has fewer gates because it is likely to give the worst SER. Timing and logic simulation may be needed for better accuracy [58]. In a real circuit, two situations can arise:

- When an SET goes through a large fan-out node the large load capacitance can eliminate the SET through node inertia.
- Or if the SET is not canceled by the fan-out node, it goes through multiple fan-out paths. If all paths have equal length, the SET might cancel itself at the merging point depending on path inversions. However, if paths have different lengths, one SET on the affected node can cause several propagating SETs to further increase the SER of the circuit.

The path delays may also influence logic SER.

5. It is highly recommended to have more field tests for logic circuits. Also, we suggest that the SER results from field tests for the same circuit, even in the same working environment, may be widely different at different times. Still, with field test data, the logic circuit SER results can be validated. A comparison with measurement may be the only way to determine which factors can be really neglected and which assumptions and approximations are justified.

6. We compared [153] and [156] for their HSPICE simulation results. In [156], the SER for the C432 circuit was reported as a FIT rate of $2.42\times10^{-5}$, while for the same circuit, the HSPICE simulation result in [153] was reported in probabilities. For 5,000 iterations it takes 108 minutes and SER is computed as 0.0725, which equals a FIT rate of $2\times10^{11}$. So, the two studies differ by a factor of $10^{16}$. We conclude that, without a proper understanding of SEU phenomena, any results can at best be misleading.

7. None of these SER estimation approaches considered process variation effects on SER, which may also be a factor in the vulnerability to transient errors. It is reported that, intra-die process variation of threshold voltage may result in SER variation of 41% in a small circuit [154].

## 5.3 Conclusion

In real cases, with actual signal values, some paths may not be activated. Temporal masking by clock sampling would further increase the masking. From our discussion, the logic SER may be highly sensitive to factors like sensitive region calibration, process variation and circuit characterization, making soft error estimation for logic circuits a complex problem. In the next chapter, we extensively study soft error effects on modern computer web server systems.

# Chapter 6

# Soft Error Considerations in Computer Web Servers

Generally speaking, a computer that is used as a web server by an Internet Service Provider (ISP) with basic mailing and customer site hosting services should have at least the following characteristics (Online source: http://theos.in/windows-server/computer-server-configuration-for-an-isp):

- Dual Intel XEON or AMD Dual core processor.
- RAID 5 1/2 TB disk.
- 4 GB Error-Correcting Code (ECC) RAM.
- Linux or FreeBSD UNIX operating system.

Services such as a Firewall, Web, FTP, RADIUS (an AAA - authentication, authorization, and accounting - protocol for controlling access to network resources) server, gaming, etc., may be supported, so the actual requirements for an ISP server will be more stringent than what is mentioned above. SEU induced errors can be categorized into four types for an electronic system depending on how the system responds to the error [134]: 1) masked error, i.e., the error is tolerated by the system; 2) correctable error, i.e., the error is detected and successfully corrected; 3) detected uncorrectable errors (DUE); and 4) silent data corruption (SDC), i.e., a non-detectable error that corrupts the system. A typical server system data corruption target is around 1000 years MTBF, as shown in Table 6.1 [34], but it is very hard to achieve this goal in a cost-effective way.

## 6.1 Soft Error Reduction in Industrial Servers

Server system designs from different manufacturers vary in their architectures. However, traditional error checking mechanisms including error correction codes (ECC) or error detection

Table 6.1: Typical server system reliability goals [34].

| Error Type | System MTBF Goal |
|---|---|
| SDC (Silent Data Corruption) | 1000 years (114 FIT) |
| DUE for system crash | 25 years |
| DUE for application crash | 10 years |

and correction (EDAC) codes, parity, and redundancy, e.g., triple modular redundancy (TMR), are extensively used for reliability, availability and serviceability (RAS) [35, 65].

We consider an industrial product, HP Integrity Non-Stop NS16000 server, as an example to show how the design for reliability concept is embodied in each component within the server. This server has the capability to grow with linear scalability from 2 to 4,080 processors and up to 65 TB of main memory. With an announced seven 9s (99.99999%) level of availability [12], the server's fault tolerant hardware techniques are summarized below:

- ServerNet: High bandwidth and low latency optical fabric connection with error detection and isolation capability. The routers are self-diagnosing and data are subjected to a 32-bit cyclic redundancy code (CRC).
- Parity checks and error-correcting code (ECC) are used in the main memory and cache and parity checks are employed in buses and caches on the logic board.
- For the disk subsystem, parity checks and end-to-end checksum are employed.

We may point out that these techniques combat both hard errors and soft errors.

Next, we focus on the error tolerance of storage devices in servers because of their extensive usage and high sensitivity to soft errors.

**Memory** The soft errors caused by alpha particles or cosmic rays are not generally repeatable because they are caused by erroneous charge storage rather than by permanent hardware faults. So, soft errors in a memory, if detected, may be corrected by rewriting the erroneous memory cells with correct data. Otherwise, a failure to correct a soft error in memory may potentially cause a serious system crash. Memory errors are categorized as either single-bit or multi-bit errors. A single bit error can be detected and corrected by standard error correction codes (ECC). However, in the case of multi-bit errors, when more bits than one are affected simultaneously by cosmic rays, standard ECC may not be sufficient. ECC may be able to detect multi-bit errors, but would have limited ability to correct them in many instances. In some instances, ECC may not even be sufficient to detect the errors.

**RAID** The needs of modern computer server systems for extensive data storage require large capacity mass data storage devices. A web server computer system provides text, graphics, sound and video on demand, and typically such a server system requires access to databases stored on rotating rigid magnetic disk drives. The volume of data required for a web server may need a considerable number of disk drives. This increases the probability that any single device might fail. For maintaining data on multiple disk drives in a redundant form a RAID (Redundant Arrays of Inexpensive Disks [87]) disk drive is commonly used. RAID has the capability to reconstruct data stored on any single disk drive, if there is a failure of that disk, from the data stored on other disk drives [145]. The disk drive has on-board soft error recovery procedures for recovering data if a soft error occurs. Because different data types stored on a disk drive have different characteristics, for example, for alphanumeric data every bit is potentially of critical importance; while for multimedia data like audio and video the corruption of a single bit or even that of several bits is likely to be acceptable because the consequences may not be potentially severe. So each disk can independently allocate, for data of different types, different data redundancy strategies. For example, if a disk drive is selected to store multimedia data, the soft error recovery can be disabled [145].

## 6.2 A Proposed Direction

It is inevitable that technology scaling and emerging materials will lead to more transient and soft failures of signals, logic values, devices and interconnects in electronic server systems. Given that the RAS requirements for high performance computer servers are stringent, the existing techniques may not be sufficient for the server requirements. Besides, the cost of high reliability may become too high to be acceptable. For example, extensive use of triple modular redundancy (TMR) can lead to excessive cost. Certain techniques, specifically those targeting soft errors, deserve more research to make the next generation servers practical.

For an ECC protected memory, because the testing of the data in a memory sector occurs only when a "read" command is issued for that sector, seldom-accessed sectors may remain untested. Harmless single-bit errors may accumulate over time and result in uncorrectable multi-bit errors. Once a "read" request is finally issued to a seldom-accessed sector, previously correctable errors may have evolved into uncorrectable multiple errors, thereby causing data corruption or system failure [111]. Recovery of memory from multi-bit errors will require more complex means. However, longer error correction codes may be too complex to implement and alternative approaches would be needed [147].

The evolution of the technology brings a new dimension of soft error effects in logic circuits. The SEU-induced transient pulse duration may span more than one clock cycle of operation, and new fault tolerance solutions working at the system level must be devised [109]. For a microprocessor, a long duration fault will cause errors in two adjacent bits at the circuit outputs, thus posing a catastrophic threat. Hard errors are distinguishable from soft errors through the "error log" reports because hard errors are repeatable. More field test results are needed for web servers. It is necessary to find out the exact causes of the so-called "soft errors" detected and recorded in the server "error log", although it is a tough task. To distinguish the soft errors caused by non-environmental factors and cosmic rays, experiments of testing identical servers at different altitudes, like at ground level and at 6,000 feet altitude, are necessary to find out how severe cosmic ray effects on the system are. Thus, SEU-specific protection techniques for complex server systems can be devised. However, such results at this time are largely unavailable.

In [107], preliminary measurements were carried out on the *ask.com* search engine and a set of office desktop computers. These results suggest that the memory SER in real production systems are much lower than those reported by previous studies. The reason cited for the low SER is that the memory DIMMs (dual in-line memory modules) in the system were plugged perpendicular to the horizontal plane, and the main source of soft errors, cosmic rays, come straight from above. This result provides a possible SER reduction method based on the hardware layout. The rack-mounted server is the most popular layout style for contemporary server systems. A rack is a metal frame that contains bays designed to hold parts of the server computer. The vertical rack spaces between stacks are defined as rack units ("U-space"); a "U" is equivalent to 1.75 inches. These rack-mounted server systems are ubiquitous. A SEU reliability-oriented hardware layout server system is discussed next and may be an SER reduction technique of the future.

First, we will evaluate the sea level cosmic ray characteristics. At sea level, the particle flux contains 94% neutrons, 4% pions, and 2% protons. There are variations in neutron flux with latitude, altitude, diurnal time, earth's sidereal position, and solar cycle. The earth's magnetic field plays a role of providing a shield against charged particles everywhere except for particles entering vertically at poles. As galactic cosmic ray particles near earth, the magnetic field interacts with the particle's charge and bends the particle's trajectory [201]. Therefore, at sea level, the particles potentially causing SEU strike the electronics with varying angles to the horizontal plane.

There is a minimum required distance that a particle with given LET must travel before sufficient energy is transferred to cause an SEU. So the particle's angle of incidence on the device is important. This phenomenon is similar to the refraction of a beam when traversing from one material to another. As the incidence angle deviates from the normal, the path length traversed by the radiation increases. The angle of incidence at which upsets occur for a given particle LET is known as the critical angle $\theta$ [88]:

$$cos(\theta_c) = LET/LET_c \tag{6.1}$$

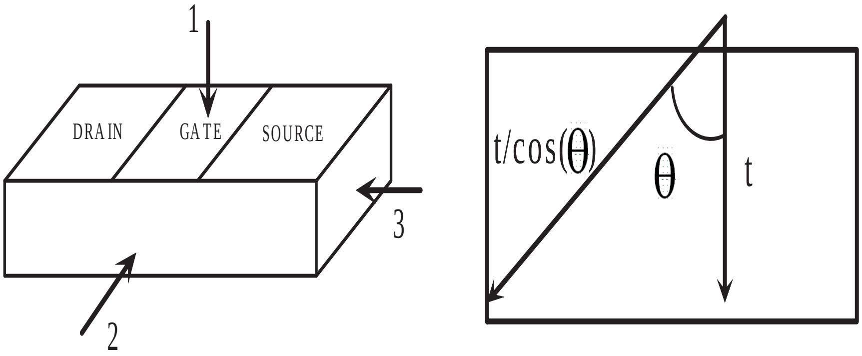

Figure 6.1: Three perpendicular orientations for exposing a transistor and particle angle of incidence [158].

where $LET_c$ is critical $LET$ and $LET_c < LET_{th}$. The particles that produce upset are between incidence angles $\theta_c$ and $\pi/2$. Thus, two potential cases exist:

1. LET > $\text{LET}_c$: all striking incident angles will produce upset.
2. LET < $\text{LET}_c$: there is a critical angle, $\theta_c$, above which upsets occur.

Figure 6.1 is a schematic view of an MOS transistor. It shows three mutually perpendicular directions of exposure to cosmic rays. The direction labeled 1 is traditionally considered for SEU testing at normal incidence. Directions 2 and 3 represent exposures at grazing incidences and their path lengths through the sensitive volume tend to be longer when protons are incident parallel to the longest dimension of the sensitive volume for proton induced SEU [158]. Particles incident at an angle ($\theta$) have a path that is $1/\cos(\theta)$ longer than the path at normal incidence. They are hence likely to produce more ionization charge.

## 6.3 Conclusion

We conclude that with a proper understanding of local ground level particle orientation and energy distribution, if the circuit boards of the server system are appropriately oriented, then the SEU caused by particles with $LET$ smaller than the critical $LET$ would be greatly reduced. However, re-arranging and placing the circuit board may not be able to totally eliminate SEU.

# Chapter 7

# Conclusion

With the continuous downscaling of CMOS technologies, reliability is bound to become a major bottleneck for the next generation systems. To meet the system reliability requirements it is necessary for both circuit designers and test engineers to get the basic knowledge of the soft errors causing those reliability problems.

In this thesis, we first present a tutorial study of the single event upset phenomenon that is one of the root causes of soft errors. The basic physics of single event upset, and basic radiation types that cause it are presented. We summarize the concepts of the basic radiation mechanisms, i.e., the error producing interactions, in silicon. An overview of the natural terrestrial environment is presented as necessary information to help build an accurate soft error analysis model. Also, soft error mitigation techniques like time and space redundancy, cell hardening and EDAC are illustrated. An industrial design example, the IBM eSerer z990 system, shows how the industry is dealing with soft errors these days.

In the second half of this thesis, we present a novel environment-dependent soft error model for logic circuits, based on two parameters: error occurrence rate and soft error transient pulse width density. An error propagation scheme through logic gates is developed that takes electrical masking into account. The SEU pulse width information at the primary outputs can help analyze the effectiveness of time and space redundancy schemes.

Our analysis requires signal probabilities. For any given set of input vectors or signal statistics, these can be obtained either from logic simulation or from static analysis of the circuit topology. For simplicity, we ignore correlations among reconverging signals. If those correlations were considered, some paths may not be activated. Similarly, temporal masking by clock sampling may further increase the masking. Future extensions may incorporate this analysis in logic simulators. That will take signal correlations and temporal effects into consideration.

The SEU transient has two parameters, the probability of error pulse generation and the random width of the pulse if one is generated. The pules width is represented by a probability density function. Logic gates are modeled with inertial delays. The probability of transmitting an SEU pulse through a gate is determined from the probabilities of other input signals. If transmitted, the SEU pulse width at the output of the gate is a function of the input pulse width and the inertial delay, and is determined from the theory of random functions. A single pass of the circuit determines the SEU statistics of all nodes in the circuit. This analysis is, however, static and is applicable to combinational circuits. It should be extended to sequential circuits in the future.

According to our results, the SER may be highly sensitive to factors like accuracy of finding sensitive regions in silicon, process variation and circuit technology. Comprehensive studies on them should provide better insights in the future. We suggest that circuit topologies will also have a significant effect on SERs. For example, a narrow circuit like an inverter chain and a wide circuit like a ripple-carry adder will have quite different soft error rates. Effective soft error control requires new cost effective techniques for soft error protections because classical fault-tolerance techniques are very expensive [125].

In addition, we have presented some essential features of soft error considerations for modern web servers and summarized the commonly used industrial fault tolerant techniques. We have proposed a possible SER reduction technique for conventional hardware server systems by considering the angle of incidence when particles strike at the circuit. Software based fault tolerance and techniques for network communications, not discussed here, are also important for web server reliability. They require future studies.

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# APPENDICES

# APPENDIX A

## TERMS AND DEFINITIONS

These miscellaneous definitions and terms are collected from JEDEC standard [4, 5] and relevant papers cited in the bibliography.

**AAA** authentication, authorization, and accounting – protocol for controlling access to network resources.

**BPSG** Borophosphosilicate glass. BPSG is a type of silicate glass that includes additives containing boron and phosphorus. Silicate glass such as PSG and borophosphosilicate glass are commonly used in semiconductor device fabrication for intermetal layers, i.e., for insulating layers deposited between successive metal or conducting layers.

**Collected Charge** The charge collected by a particular device node during the passage of a particle. The collected charge is dependent on the geometry and doping of the node, the particle properties like mass, energy and trajectory, and the density and type of material being penetrated by the incident radiation.

**Cross Section ($\sigma$)** the device SEE response to ionizing radiation. Normally, the unit for cross section is $cm^2/device$ or $cm^2/bit$ .

**Critical Charge ($\mathbf{Q}_{crit}$)** The minimum amount of charge that when collected at any sensitive node will cause the node to change state. The critical charge is usually generated by incident radiation and its value is dependent on the effective linear energy transfer, which is usually a function of the angle of incident of the particle radiation.

**Differential Flux** The time rate of fluence per unit energy, the rate of quantity of radiation, particle fluence, per unit area incident on a surface per unit energy. The differential flux is usually expressed number ($N$) of particles per unit area per unit energy per unit time, like $N/cm^2 - MeV - hr$. The term differential flux in JEDEC standard is synonymous with spectral flux density used in other publications.

**ECC** Error correction code, sometimes called Error Detection And Correction (EDAC).

**Fluence** The total amount of particle radiant energy incident on a surface in a given period of time, divided by the area of the surface. Fluence is usually expressed number ($N$) of particles per unit area, e.g., $N/cm^2$.

**Flux Density** The time rate of flow of particle energy emitted from or incident on a surface, divided by the area of that surface. The flux density is usually expressed number ($N$) of particles per square centimeter second ($N/cm^2 - s$) or particles per square centimeter hour ($N/cm^2 - h$).

**Hard Error** An irreversible change in operation that is typically associated with permanent damage to one or more elements of a device or circuit.

**LET** Linear Energy Transfer. $LET$ is a measure of the energy transferred to the device per unit length as an ionizing particle travels through a material. The commonly used unit is $MeV - cm^2/mg$ of material (Si for MOS devices).

**LET**$_{th}$ $LET$ threshold ($LET_{th}$) is the minimum $LET$ to cause an effect at a given particle fluence.

**MEU** Multiple Event Upsets.

**MBU** A multiple-bit upset in which two or more error bits occur in the same word. An MBU in memory can not be corrected by a simple single-bit ECC.

**Radiation** Energy emitted in the form of electromagnetic waves or moving nuclear particles. In the present research, the primary concern is the ionizing radiation that includes protons, electrons, alpha particles and nuclear reaction products.

**RAID** Redundant Arrays of Inexpensive Disks. RAID is a technology that supports the integrated use of two or more hard-drives in various configurations for the purposes of achieving greater performance, reliability through redundancy, and larger disk volume sizes through aggregation.

**SEB** Single Event Burnout. Damage of burnout of power transistor or other high voltage devices due to a single energetic particle. SEB includes burnout of n-channel power MOSFETs and it can be triggered in a power MOSFET biased in the OFF state when a heavy ion passing through deposits enough charge to turn it on. Both SEL and SEB susceptibilities decrease at higher temperature.

**SEE** Single Event Effect. Any measurable or observable change in state or performance of a microelectronic device, component, subsystem or system resulting from a single energetic particle strike. SEE include SEU, SEL, SEB and SEFI.

**SEFI** A energetic particle caused functional interrupt, malfunctions in more complex parts sometimes as lockup, hard error, etc.

**SEL** Single Event Latchup. The SEL is defined as a condition that causes loss of device functionality due to single event induced current. SEL results in a high operating current. It may drag down the node voltage or damage the power supply. The latch-up is caused by heavy ions as well as protons in the sensitive area in semiconductor devices. SEL can be cleared by the power off-on reset.

**Sensitive Volume** A region, or multiple regions affected by SEE-induced radiation. The sensitive volume is determined by the angle of the incident radiation, the mass and energy of the incident particles and the density, type of the material in the volume being penetrated by the incident radiation. It is not easy to know the geometry of the sensitive volume of the device but some information can be gained from the test cross section data.

**SET** Single Event Transient. A current or voltage transient pulse caused by SEE.

**SEU** Single Event Upset. Radiation-induced errors in microelectronic circuits caused when charged particles (usually from the radiation belts or from cosmic rays) lose energy by ionizing the medium through which they pass, leaving behind a wake of electron-hole pairs.

**SEGR** Single Event Gate Rupture. SEGR is the destructive burnout of a gate insulator in a power MOSFET.

**Soft error, static** A soft error in a memory that cannot be corrected by repeated reading but can be corrected by rewriting without the removal of power.

**Soft error, transient** A soft error that can be corrected by repeated reading without rewriting or without the removal of power.

**SER** Soft error rate.

**SOI** Silicon on insulator.

**TID** Total ionizing dose.

# Appendix B

## Units and Conversion Factors

**MTTF** Mean Time to Failure.

**MTTR** Mean Time to Repair.

**MTBF** Mean Time Between Failures. MTBF = MTTF + MTTR. The concept of Availability is defined as MTTF/MTBF.

**FIT** Failure in Time; the number of failures per $10^9$ device hours. 1 year MTTF = $10^9/(24\times365)$FIT = 114,155 FIT.

**Gray (Gy)** 1 gray = 1 joule per kilogram.

**rad** rad is a unit of radiation dose. 1 rad = 0.01 gray (Gy) = 0.01 joule of energy absorbed per kilogram of matter.

**Hadron** Particles which have strong interaction. Also called nuclear force.

**Energy Units**

1. Electron Volt (eV). One eV is the energy gained by an electron when accelerating through a potential difference of 1 volt. Energy of radiation is usually in MeV ($10^6$eV) or KeV ($10^3$eV).
2. Joule (J). 1 eV = $1.6\times10^{-19}$ J, 1MeV = $1.6\times10^{-13}$ J.
3. erg. 1 erg = $10^{-7}$ Joules.

**Electronic charge** $e = 1.602 \times 10^{-19}$ coulomb.

**$\mu$Acm$^{-2}$** 1 $\mu Acm^{-2}$ = $6.241\times10^{12}$ electrons $cm^{-2}s^{-1}$