SOLDER JOINT RELIABILITY & PROGNOSTICATION OF LEAD FREE ELECTRONICS IN HARSH THERMO-MECHANICAL ENVIRONMENTS

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SOLDER JOINT RELIABILITY & PROGNOSTICATION OF LEAD FREE ELECTRONICS IN HARSH THERMO-MECHANICAL ENVIRONMENTS

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SOLDER JOINT RELIABILITY & PROGNOSTICATION OF LEAD FREE

ELECTRONICS IN HARSH THERMO-MECHANICAL

ENVIRONMENTS

Chandan Bhat

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THESIS ABSTRACT

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The trends in the electronic packaging industry are to design smaller packages that have higher complexity, and to improve package reliability while reducing costs. These needs in the packaging industry have lead to a newer generation of chip architectures, such as: Chip Scale Packages, Plastic Ball Grid Arrays, and Flip Chips. However, despite the increased performance capabilities of these leading-edge package types, their thermo-mechanical reliability is a concern for harsh environment applications. In this study, the thermo-mechanical reliability of a new architecture (D-Pack^{TM}) has been studied using finite element methods. Life prediction relationships based on damage accumulation principles have been used to calculate the characteristic life, and has been compared with thermal shock data. Failure analysis of the tested assemblies has been conducted to correlate failure locations with predictions from FEM.

While reliability analysis of any component is critical, it is also important to monitor the condition / state of the system from time to time in order to improve the system availability and upkeep. So far, traditional health monitoring methodologies have relied on reactive methods of failure detection often providing little on no insight into the remaining useful life of the system. Detection of system-state significantly prior to catastrophic failure can significantly impact the reliability and availability of electronic systems. Previously, Lall [2004, 2005] have developed methodologies for health management and interrogation of system state of electronic systems based on leading indicators for eutectic Sn-Pb & 95.5Sn4.0Ag0.5Cu solders. Examples of damage pre-cursors include micro-structural evolution, intermetallics. In this study, a mathematical approach for interrogation of system state under cyclic thermo-mechanical and iso-thermal stresses has been developed for 4-different lead-free solder alloy systems. Data has been collected for leading indicators of failure for alloy systems including, SnAgCu, SnAgCuBi, SnAgCuBiNi, SnAg second-level interconnects under the application of thermo-mechanical loads. Methodology presented resides in the pre-failure space of the system in which no macro-indicators such as cracks or delamination exist. Systems subjected to thermo-mechanical damage have been interrogated for system state and the computed damage state correlated with known imposed damage. The approach involves the use of condition monitoring devices which can be interrogated for damage proxies at finite time-intervals. Interrogation techniques are based on non-linear least-squares methods. Various techniques including the Levenberg-Marquardt Algorithm have been investigated. The system's residual life is computed based on residual-life computation algorithms.

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CHAPTER 1

INTRODUCTION

The rapid evolution in microelectronic technology is a well known phenomenon. The decreasing feature sizes on IC's enable the integration of a huge number of transistors on a given area of silicon. In addition to the increase in complexity and size, the pin count of the die is increasing with time. The fast evolution in microelectronic technology has also enabled the circuits to run at higher speeds. Such high frequencies require special design of the IC's and packaging interconnections.

Electronic packaging is the process of interconnecting electronic and electromechanical components, devices, and modules between the various layers of the electronic system [Suhling, et.al. 2004]. Single-Chip packaging has evolved during the last 3 decades, starting with Dual-Inline Packages (DIPs) and wire bond in the 1970s, Quad Flat Packs (QFPs) and Surface-Mount Technologies (SMT) in the 1980s, and Ball-Grid Arrays (BGAs) in the 1990s. In the last two decades area-array packages, e.g., BGA, Chip Scale Package (CSP) have become more popular packaging alternatives as compared to their earlier counterparts.

BGA packages offer a lot of benefits over their leaded counterparts (QFPs / PQFPs) by providing increased functionality for the same package size while being compatible with existing surface mount technology infrastructure. BGAs fit ICs into a smaller footprint, decreasing pitch spacing, by utilizing an array of solder ball

connections. This allows for a higher density of I/O connections than QFPs, along with a high yield. The result is a considerably smaller finished package size. BGAs also offer better electrical performance due to reduced lead inductance. They also have an improved design-to-production cycle time and can be used in flip-chip-package (FCPs) and multi-chip modules (MCMs) configurations.

We know that electronics forms an integral part of most systems that we use, in the form of a simple alarm clock or the circuitry that controls the fuel injection under the hood of a vehicle. Failure of an electronic sub-system to perform reliably can sometimes, depending on the application, lead to catastrophic consequences. Reliability testing is therefore a very important criterion for any electronic system before it is being deployed in the field.

The work presented in this study mainly deals with the reliability of electronics subjected to harsh thermo-mechanical environments. The operation of any electronic device generates heat and with the increasing device density of the IC chips the amount of heat flux generated by the IC chips has gone to a level of 100-200 W/cm^2 [Nimkar, et al. 2005]. An electronic package like BGA (shown in Figure 1) is essentially an assembly of different materials sets (die, BT substrate, molding compound, etc) attached together using various processes. Each material set has unique properties like Coefficient of Thermal Expansion (CTE), Young's Modulus (E), poisons ratio (ν), etc. When this assembly is subjected to a change in temperature, either on account of Joule heating or change in ambient temperatures, these unique materials tend to expand / contract at different rates resulting in cyclic shear strains and shear stresses, which over a period of time lead to fatigue.

The fatigue failure of the device can occur in various different modes [Viswanadham and Singh, 1998]. A summary of common failure modes is shown in Table 1 below

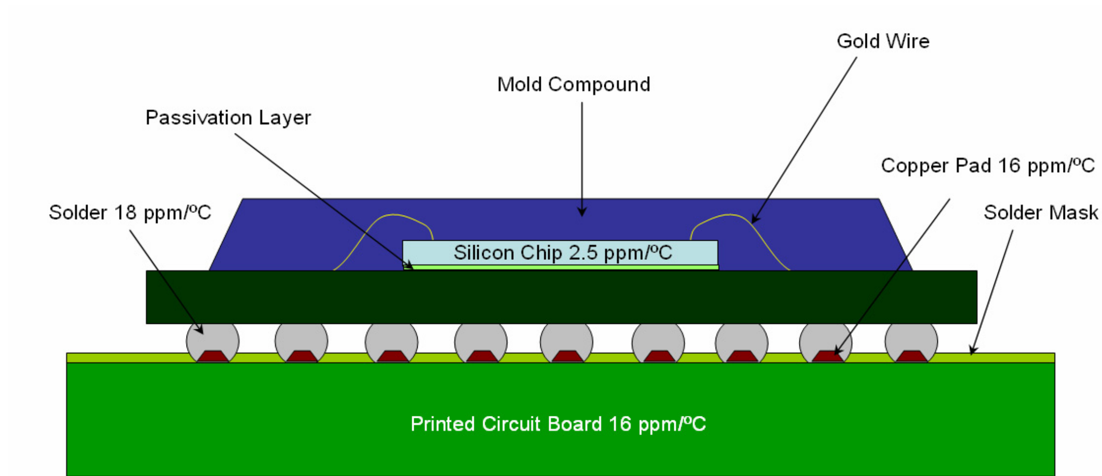


Figure 1: Various components of a BGA package with the corresponding approximate coefficients of thermal expansion (CTE) values.

Table 1 : Common Failure Modes in Electronic Packages

Failure Mode	Reason
Pop-Corn Failure	Occurs during the re-flow of the component due to moisture absorbed by the molding compound.
Chip / Die Cracking	Occurs due to thermal stresses developed in the chip during package assembly or during the thermal cycling of the component due to the CTE mismatch within the package.
Delamination between Interfaces	Occurs due to thermal stresses developed in the chip during the thermal cycling of the component due to the CTE mismatch within the package.
Solder Joint Failure	The expansion and contraction of material sets due to Joule heating / change in ambient temperature introduces shear strains and shear stresses in the solder joint. The repeated heating and cooling can eventually cause fatigue of the solder joints.

It has been established from various studies and failure analyses [Harmon 1974, Engelmaier 1984, Katlowitz 1986, Hwang 1988, Solomon 1989, Tien, et al. 1989, Lau 1991, Lall, et al. 1997, 2003, 2005, Suhling, et al. 2004] that the interconnect failure due to the thermal cycling is the most critical mode of failure in various leaded and SMT packages such as BGAs and flip-chips. Solder joint fatigue failure being a dominant failure mode contributing to 90% of all structural and electrical failures [Tummala 1997] demands greater focus for improving the mechanical reliability of the package.

1.1 Reliability of Novel 3-D Architectures (D-PACK^{TM})

Moving forward, miniaturization with increased functionality continues to be an important trend in all electronics products [Mallik, et al. 2005]. An example of miniaturization trend is also seen in the ever improving functionality of mobile handsets. Over the last five years or so, 2D games, and even more demanding 3D games, have become available in these devices. The increased functionality (music, video, gaming, etc) integration with each handheld product generation adds to the complexity of the baseband and power management units, which in turn requires more passive components (especially resistors and capacitors) for baseband power supply and management. The number of passive components in a typical cell phone has more than tripled in the last few years. This increase in passive counts leads to increase in assembly costs and reliability issues.

Capacitors are used to decouple the system-level power supply from individual electrical devices of an electronic package. Decoupling of an electronic device from the power supply reduces the overall noise in the power distribution network of the electronic package [Geissenger, et al. 2006]. However, due to increase in the speed and electrical current associated with high-speed electronic devices, traditional capacitor structures do not provide adequate performance because the inductance associated with these types of capacitors inhibits their operation at high speeds. Interconnect inductance in an electronic package chokes the capacitor, preventing the high-speed transfer of electrical current to and from the capacitor. Embedding capacitors directly into the electronic packages provides significant decoupling capacitance with very low interconnect inductance. This

approach facilitates very high-speed operation of electronic devices within an electronic package.

Kemet Corporation has patented a technology to embed capacitor in a Ceramic Ball Grid Array Package, called a D-PACK^{TM}. The capacitors are embedded in the second-level interconnects of the package. In the present work, the thermo-mechanical reliability of two configurations of D-PACK^{TM} (full interposer & partial interposer) in harsh environments has been studied using finite element simulations. Failure analyses of failed packages were carried out to investigate the failure modes and mechanisms.

1.2 Prognostics of Lead Free electronics in Harsh Environments

There is a growing need to develop and demonstrate technologies that can monitor and predict the remaining service life of key elements in our national civil infrastructure [Bond 1999]. Maintenance has evolved over the years from simply reacting to machinery breakdowns (corrective maintenance), to performing time-based preventive maintenance, to today's emphasis on the ability to detect early forms of degradation in predictive maintenance practices. The incentive for each incremental step has been a clear reduction in the cost of operating and maintaining (O&M) almost any process facility [Jarell, et al. 2002].

Health Monitoring (HM) refers to the broad concept of assessing the ongoing, in-service performance of a system using a variety of measurement techniques. Prognostics refer to interrogation of material state of a system based on computation of certain proxies, stressors, and to predict the Residual Life (RL) of the system for the intended environment. PHM application areas include fatigue crack damage in mechanical structures such as those in aircraft [Munns 2000], surface ships [Baldwin 2002], civil

infrastructure [Chang 2003], railway structures [Barke 2005] and power plants [Jarrell 2002].

Wear and degradation in electronics is very difficult to detect and inspect compared to most other mechanical systems and structures due to complex and tiny structure. Methods like Built-In-Self-Test (BIST), embedding fuses and pre-calibrated canaries within circuits have been used to provide advance warning of failure in electronics due specific wear out failure mechanism.

A Prognostics & Health Management (PHM) approach has been presented in this study. The approach is different from the current state-of-art diagnostics and resides in the pre-failure space of the electronic-system, in which no macro-indicators such as cracks or delamination exist. The presented PHM methodologies enable the estimation of prior damage in deployed electronics by interrogation of the system state.

Data has been collected for leading indicators of failure for two separate test vehicles, with different area array packages soldered with various lead free alloys (SAC 405, SnAgCuBi, SnAgCuBiNi, 96.5Sn3.5Ag) under both single and sequential application of cyclic and isothermal thermo-mechanical loads.

CHAPTER 2

LITERATURE REVIEW

It is only natural that any major system used these days comprises several sub-systems, each containing myriad components and elements. Since system-level reliability depends on the reliability of these individual components, it becomes critical to analyze the reliability of any component during design phase or before deployment in the field. Concurrent with the rapid progress in IC technology, packaging of an electronic system with high reliability is posing an ever increasing challenge. Whether the result of power transients or changes in ambient temperature, a solder joint must withstand repeated strain reversals caused by non-uniform thermal expansion of the carrier, the solder, and the board [Wong et. al. 1988]. Because of the cyclic nature of this loading, this type of failure has been called fatigue.

Although historically fatigue studies have been concerned with conditions of service in which failure occurred at more than 10^4 cycles of stress, there is growing recognition of engineering failures which occur at relatively high stress and low numbers of cycles to failure [Coffin 1979]. Low cycle fatigue conditions frequently are created where the repeated stresses are of thermal origin [Manson 1960]. Since thermal stresses arise from the thermal expansion of the material, it is easy to see that in this case fatigue results from cyclic strain rather than from cyclic stress [ASTM Standard 1969].

Solder joint fatigue failure being a dominant failure mode, contributing to 90% of all structural and electrical failures [Tummala 1997] demands greater focus for improving the mechanical reliability of the package. As newer packages and architectures continue to evolve with improvements in IC technology, there is a need to develop efficient predictive methodologies for maintaining high levels of package reliability. Over the years, this reliability problem has been approached using combination of experimental measurements and numerical simulations. There exist numerous life-prediction methods for solder fatigue. This section briefly discusses the evolution of various approaches used for solder joint reliability prediction, including inelastic strain or total strain based models, energy based models, physics of failure based models, statistical models and finite element models.

Coffin [1954] & Manson [1964] developed relationship between low-cycle fatigue life (cycles to failure) and plastic strain range ($\Delta\varepsilon_p$). Norris and Landzberg [1969] studied the effect of cycling frequency and maximum temperature of cycling on fatigue failure of solder joints and added an empirical correction factor for time dependent and temperature dependent effects for the thermal fatigue model.

Engelmaier [1982] developed a methodology to determine shear strains from in-plane expansion mismatches. Further Engelmaier [1984] proposed that cyclic fatigue damage is directly proportional to the area circumscribed by the cyclic hysteresis loop in a stress-strain diagram. Engelmaier [1990] developed a surface mount solder joint reliability prediction model containing all the parameters influencing the shear fatigue life of a solder joint due to shear displacement caused by thermal expansion mismatch between component and substrate. The parameters of the model include effective solder

joint area, solder joint height, diagonal flexural stiffness, distance from neutral point and thermal coefficient mismatch, thermal cycling conditions, degree of completeness of stress relaxation and slope of weibull distribution.

Solomon [1989] analyzed the fatigue failure of 60Sn/40Pb solder for various temperatures and developed an isothermal low cycle fatigue equation that correlated number of cycles to failure with applied plastic shear strain range. Solomon also studied the influence of factors like frequency of loading, temperature changes on the fatigue life, and added exponents to the fatigue equation to account for them.

Shine and Fox [1987] proposed a model correlating the number of cycles to failure with matrix creep shear strain $\gamma_{mc.}$ This correlation was achieved using a steady-state creep law with different, experimentally determined coefficients for each sample considered; the matrix creep was then integrated over the actual measured stress history. Subsequently, Knecht and Fox [1990] proposed a constitutive equation for a typical Sn-Pb eutectic solder joint based on empirical data in shear strain. It was shown that the constitutive equation together with the matrix creep failure indicator gave an estimate of fatigue life which matched reasonably well with independent failure datasets.

Wong et al. [1988] developed an analytical framework to predict the failure of solders under creep conditions, based on micromechanics and fracture mechanics approach. This method assumed the presence of a pre-existing crack within the solder, and proposed a theory about nucleation of cavities, their subsequent interlinking around the local second phase particles in the vicinity of crack tip stress field. Based on cavity-crack inter-linkage, equation for crack growth was developed. The time to failure was calculated by assuming that a pre-existing crack grows by creep cavitation until it reaches

a critical length when instantaneous fracture occurs. Yamada [1989] showed that the concept of fracture mechanics could be suitably applied to solder joint cracking and that the fracture toughness of the solder is an important parameter to compare the influence of many variables on the strength relevant to soldering of electronic packages. The theory of strain energy release, and fracture toughness was applied to a 60Sn-40Pb soldered joint of beryllium copper to beryllium copper.

Subrahmanyan et al. [1989] proposed a damage integral calculation providing a numerical accounting of fatigue damage in solder joints. Using a simplistic crack propagation law, crack growth parameters were derived from isothermal fatigues tests and successfully applied to thermo-mechanical fatigue tests through the damage integral approach.

Dasgupta et al. [1992] proposed an energy partitioning approach that considered the complete stress-strain hysteresis response of the solder. The energy stored and dissipated during each cycle (determined by the hysteresis curve) was partitioned into elastic (recoverable) energy, plastic (instantaneous, irrecoverable) work and creep (time-dependent, irrecoverable) work. This energy partitioning information was obtained from visco-plastic analysis such as finite element methods. Three independent power-law expressions relating the partitioned energy to the damage (or cycles to failure) were obtained from experimental data in the literature for eutectic Pb-Sn solder. The total damage incurred in each thermal cycle was calculated using a simple linear superposition of damage due to each of the three partitioned energy terms.

Syed [1995] presented an engineering approach to the life prediction of solder joints in thermal cycle environment. A damage mechanism based on creep crack growth

model incorporating multiaxiality and time, temperature dependence of the solder joint in thermal cycling environments was proposed. The creep deformation mechanisms viz. grain boundary sliding and matrix creep phenomenon were treated separately in this approach. A three-dimensional finite element approach was used to accurately separate the contribution of each mechanism to the total damage. It was shown that creep crack growth rate was a function of temperature, dissipation rate of creep strain energy density and some material and crack growth parameters. For the same damage mechanisms, this model was capable of predicting the fatigue life for any loading profile, frequency and temperature range.

Pao [1992] proposed a crack growth model in terms of both C* integral based creep mechanisms (nucleation, growth and coalescence of cavities along grain boundaries) and J integral based fatigue mechanisms (applied stress in the solder joint acting as the driving force in the propagation of initial crack leading to fracture). In addition to the capability of predicting thermal fatigue life of solder joints, this method could also be used to design accelerated thermal tests.

Clech [1996] developed a solder reliability solutions model for leadless and leaded eutectic solder assemblies and extended it to area array and CSP packages. Clech obtained the inelastic strain energy density from area of solder joint hysteresis loop and developed a prediction equation correlating inelastic strain energy density with number of cycles to failure.

Darveaux et al. [1992] conducted shear and tensile loading experiments on various solders (60Sn40Pb, 96.5Sn3.5Ag, 97.5PbSn2.5, 95Pb5Sn) and presented the deformation behavior of these alloys by the same set of constitutive relations. Also,

numerical simulations were conducted to predict the solder joint response for these alloys under thermal cycling conditions, based on hysteresis loop calculations.

Darveaux [1996] developed a strain energy based methodology to predict the solder joint reliability. A three-dimensional finite element model of the package was created where the solder joints were modeled as visco-plastic material, printed circuit board as orthotropic linear elastic and rest of the material as linear elastic. Symmetric boundary conditions were imposed on the model to coincide with true symmetry plane. The energy-based method linked the fatigue life to the inelastic strain energy dissipation of solder joints. Based on extensive test of BGA solder joints and FE modeling, Darveaux proposed empirical equations to calculate the solder fatigue life [1996, 1997, and 2000].

In Darveaux's model, the total fatigue life consists of the life before crack initiation and the life after it. The constant terms are derived by curve fitting the FEA prediction with the test data. Because the inelastic strain energy depends strongly on the finite element mesh of the solder joints, different constants values were given according to the element size. The extracted plastic work accumulated per unit volume per thermal cycle was used for crack growth correlations. Volume averaging was applied to reduce the sensitivity of strain energy to meshing.

Hariharan [2006] presented models based on multiple linear regression, principal components regression and power law based methodologies for developing prediction models to enable higher-accuracy prediction of characteristic life by perturbing known accelerated-test data-sets using models, using factors which quantify the sensitivity of reliability to various design material, architecture and environmental parameters.

Of all these methodologies, Darveaux's seems to be the most popular due to the ease in its implementation. Also, methodology has been previously presented in the successful analyses of various electronic assemblies from multiple industry sources. Darveaux's energy based model has been used in this thesis to evaluate the thermo-mechanical reliability of 2nd level interconnects for capacitor embedded in a Ceramic Ball Grid Array Package.

While reliability analysis of any component is critical, it is also important to monitor the condition / state of the system from time to time in order to improve the system availability and upkeep. Majority of systems being used these days, e.g., nuclear power plant machinery, aircrafts engines / avionics, gas turbine systems, are expected to remain operational for lengthy periods of time and usually have an elaborately drawn maintenance / overhaul schedule. Also, maintenance techniques have evolved over the years from simply reacting to machinery breakdowns (corrective maintenance), to performing time-based preventive maintenance, to today's emphasis on the ability to detect early forms of degradation in predictive maintenance practices. The incentive for each incremental step has been a clear reduction in the cost of operating and maintaining (O&M) almost any process facility [Jarell, et al. 2002].

New advances in sensor technology and failure analysis are instigating a revolution in the way large electromechanical systems such as aircraft, helicopters, ships, power plants, and many industrial operations will be maintained in the future. For industry and the armed services, the 21st century will bring the age of PHM — Prognostics and Health-Management [Becker et al. 1998]

Health Monitoring refers to the broad concept of assessing the on-going, in-service performance of a system using a variety of measurement techniques. Prognostics means predictive diagnostics, which includes determining the remaining life or time span of the operational life of a component. Prognostics & Health Management (PHM) refers to the methodology of interrogation of material state of a system based on computation of certain proxies and to predict the Remaining Useful Life (RUL) of the system for the intended environment.

PHM methodology application areas include aircraft structures [Munns 2000], surface ships [Baldwin 2002], civil infrastructure [Chang 2003], gas turbines. This section briefly discusses the various applications where PHM methodology has been applied.

In case of mechanical systems like propulsion systems, compressors, gears, etc damage progresses mainly due to wear (prolonged usage), or imbalance condition in one of the rotating elements, or from misalignment of the shafts of the rotating components which leads to changes in the vibration signature of the equipment. By comparing the vibration signals from the defective equipment with those from sound equipment, the performance degradation can be characterized [Dyne 1992].

PHM of mechanical structures has been done by dynamic analysis based on natural frequencies, mode shapes, damping factors, and static analysis based on deformation or changes in structure orientation due to load or unexpected damage, using innovative signal processing, new sensors, and control theory. Transducers along with a wireless data acquisition system can enable the possibility of achieving long distance monitoring [Kok 2005].

Greitzer et al. [1999] has developed prototype diagnostic / prognostic system for main Battle Tank's (MBTs) engine health based on Artificial Neural Networks (ANNs) to diagnose and predict faults. This approach uses approximately thirty onboard sensors to measure temperature, pressure, RPM, vibration to construct a detailed thermodynamic picture of the engine's state. This data is then conveyed via telemetry to the command / control and maintenance support so that battle readiness and maintenance needs can be assessed immediately.

Smeulers et al. [2002] applied a model based PHM methodology to an aircraft hydraulic system using measurable condition parameters like valve port timing, internal leakage using two pressure transducers. The health of the system was monitored by means of signature analysis of pulses produced by pump at sensors. Similar concepts can be applied for health monitoring of other aircraft sub-systems like fuel system, lubrication system of main engine.

The technique of detecting specific faults by interrogating sensors placed along the sides of railway tracks is referred to as wayside detection. Barke [2005] has reviewed various types of wayside detection techniques used in the railway industry to provide extensive information about vehicle performance. The information generated is often recorded in an extensive database, providing information on the vehicle condition and performance over an extended period of time. This database can be interrogated with respect to certain critical performance parameters over time to provide information on condition of in-service railway vehicles.

Most of the PHM methodologies listed above operate by collecting precursor data from sensors, mounted on or near the components, which collect for data in the form of

signals, pulse, etc. Signal feature analysis is performed to detect abnormalities that are related to an impending failure indication by an inference engine / system using an historical database [Hess 2001, 2002]. This approach can provide warning of failure but is inherently incapable of attaching a confidence interval to the remaining life prediction [Wilkinson et al. 2004]. In contrast, electronic systems cannot generally provide such kinds of precursor data.

Wear and degradation in electronics is very difficult to detect and inspect compared to most other mechanical systems and structures due to complex and tiny structure. Some examples of health monitoring in electronic circuits are discussed below.

It has been common practice to implement error detection and sometimes error correction, in dynamic RAM arrays. DRAMS are subject more than any other type of component to single event upsets arising from cosmic rays and alpha particles. Error may be detectable, or with increased hardware overhead, correctable for single bit errors. Similarly, due to their regular structure, the operating system can to keep track of 'bad sectors', analogous to the bad sector mapping applied to disk drives and map out the failed locations. Electronic part manufacturers apply a similar technique to DRAMS. They selectively laser-cut redundant cells into the array to replace those found to be defective on final test. These techniques rely upon precursors to indicate declining health and are very limited in the types of failure that can be predicted and in the warning period provided [Wilkinson et al. 2004].

Built- In-Self Test (BIST) circuit, which includes onboard hardware and software diagnostic, has been used for error detection and fault location [Drees 2004]. BIST is a methodology that embeds additional functionality in the product to give it the ability to

test and diagnose itself with minimal interaction from external test equipment [Williams 1983, Hassan 1992, Zorian 1994, Chandramouli 1996].

BIST controllers are typically used for reactive failure detection, to output failure data that can be correlated to show exactly when the failure occurred. This data can then be interpreted by diagnostic software to analyze the cause of failure. For example, Pseudo-Random Binary-Sequence (PRBS) test pattern generators, apply input vectors to digital or analog [Al-Qutayri 1992] modules. Self-Checking circuit designs provide on-line test for digital [Lala 1985] as well as for analog circuits [Kolarik 1993]. The obtained output is then compared with a "golden response". The results obtained from BIST functions can generate diagnostic information which in turn provides additional confidence in the measurement result and confirm the device availability.

BIST helps in minimizing the interaction with external automated test equipment (ATE) as well as provides the advantage of a more robust “at-speed” test of the circuitry. However, the current form gives little insight about the system level reliability or the remaining useful life of the system. Several studies conducted [Allen 2003, Drees 2004, Gao 2002, Rosenthal 1990] have shown that BIST can be prone to false alarms and can result in unnecessary costly replacement, re-qualification, delayed shipping, and loss of system availability.

Fuses and Canaries have been used to provide advance warning of failure in electronics due to specific wear out failure mechanism [Vichare 2006]. Fuses within circuits and thermostats, can be used to sense the abnormal conditions like voltage transients, critical temperature limit and to make adjustment to restore normal condition [Ramakrishnan 2000].

Canary devices like pre-calibrated cells which are located with the actual circuitry on the same chip experience similar stresses as the actual component, this leads to same damage mechanism. The cells are designed to fail faster by scaling the stress which is been experienced to avoid the catastrophic failure of actual component. The failure of the canary devices can be used to estimate the time to failure of actual product [Mishra 2002]. Similarly canary components created on printed circuit board is been used for prognostication by failing before the actual component [Anderson 2004].

However, replacement of fuses and canaries impacts the maintenance, repair and part replacement making it difficult to integrate these systems with the host system. In addition, fuses provide limited insight into the remaining use life prior to fuse-failure.

These approaches may be best described as health monitoring approaches. They do not (and cannot) address the prognostic side of the problem. PHM approach presented in this paper is different from state-of-art diagnostics and resides in the pre-failure space of the electronic-system, in which no macro-indicators such as cracks or delamination exist. The presented PHM methodologies enable the estimation of prior damage in deployed electronics by interrogation of the system state.

CHAPTER 3

THERMO-MECHANICAL RELIABILITY OF 3-D PACKAGES

Microelectronic packages continue to undergo significant changes to keep pace with the demands of the high performance silicon. From the traditional role of space transformation and mechanical protection, packages have evolved to be a means to cost-effectively manage the increasing demands of power delivery, signal distribution, and heat removal. In the last decade or so, increasing frequency and power levels coupled with lower product costs have been driving new package technologies [Mallik, et al. 2005].

Because of current flow during the simultaneous switching of the circuits of digital systems, voltage fluctuations are generated across power supply buses. The magnitude of these fluctuations depends on the amount of current, its rise time, and the effective chip and package inductances [Humenik et al.1992]. This noise can couple through a quiet logic circuit driver and appear as a spurious voltage signal on the input terminals of a logic receiver circuit, sometimes causing switching [Davidson 1982, Ho 1982]. On-chip decoupling capacitors (decaps) are widely used to mitigate the power-supply-noise problem. By charging up during the steady state, decaps can assume the role of the power supply and provide the current needed during the simultaneous switching of multiple functional blocks [Wong 2007]. Alternatively, decoupling capacitors can be used to reduce the impedance of power delivery systems operating at high frequencies.

However, due to increase in the speed and electrical current associated with high-speed electronic devices, traditional capacitor structures do not provide adequate performance because the inductance associated with these types of capacitors inhibits their operation at high speeds [Geissinger 2006]. Interconnect inductance in an electronic package chokes the capacitor, preventing the high-speed transfer of electrical current to and from the capacitor. Since the inductance scales poorly [Mezhiba 2004], the location of the decoupling capacitors significantly affects the design of the power / ground (P/G) networks in high performance ICs such as microprocessors. With increasing frequencies, a distributed system of on-chip decoupling capacitors is needed.

3.1 *D-Pack™*: Capacitor Construction

Embedding capacitors directly into the electronic packages provides significant decoupling capacitance with very low interconnect inductance. This approach facilitates very high-speed operation of electronic devices within an electronic package [Geissinger 2006]. The decoupling capacitors are placed on the PCB, package, and chip levels, respectively [Kim 2001] as shown in Figure 2:. In case of on-chip decaps, the costs associated with layer count in substrates, and other additional processes to facilitate the connection (traces) between decaps and operating device, drive the overall package costs upwards, making them uneconomical.

Kemet Corporation has patented a technology to make monolithic multi-layer capacitors with improved lead-out structure [Prymak 2005]. The individual monolithic multi-layer capacitors *D-Sticks*™ are assembled into a matrix structure called as *D-Pack*™ as shown in Figure 3. The top and bottom sides of *D-Pack* have metal layers

(including a thin layer of solder) deposited so that it can be attached to both the package as well as the Printed circuit Board (PCB).

The *D-Pack* serves as a physical interconnection between the substrate and the PCB, and also serves a decoupling capacitor performing the functions of reducing signal noise and inductance. Figure 2 and Figure 3 show the conventional configuration of decoupling capacitors vis-à-vis the configuration proposed by Kemet.

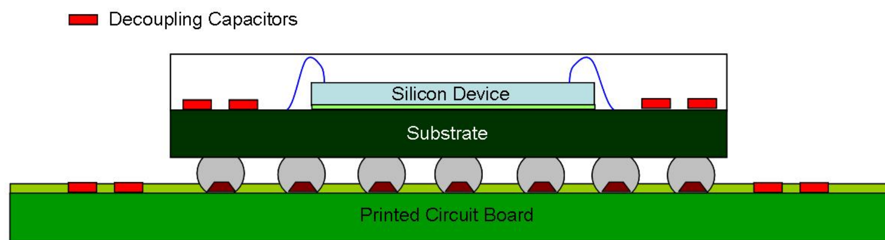


Figure 2: Decoupling capacitors placed on PCB and Package level (Conventional Configuration)

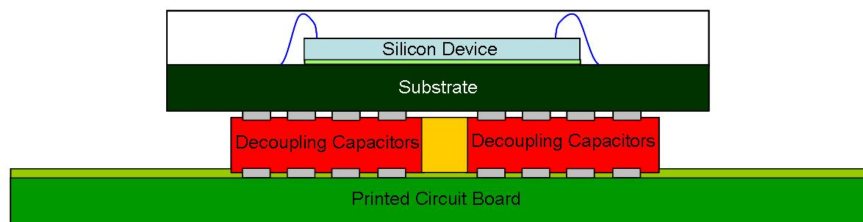


Figure 3: Matrix of decoupling capacitors embedded as a part of second level interconnects structure [Prymak 2005].

Two configurations of *D-Pack*™ have been assembled and subjected to thermal shock experiments at the Center of Advance Vehicle Electronics (CAVE) at Auburn University. The first configuration was called as Partial Interposer, where the *D-Pack*™ is sandwiched between the LTCC Ceramic package and the FR-4 PCB such that solder terminations on the top and bottom surface of the *D-Pack*™ (at package center) form the electrical and mechanical interconnections. This configuration did not have the solder balls on the outer periphery of the package. Figure 4 shows the partial interposer configuration.

The second configuration was called as Full Interposer, where in addition to the *D-Pack*™ capacitor matrix at the central core, the package was assembled with the PCB using an intermediate layer of FR-04 PCB with two rows of spherical solder ball forming the electrical and mechanical connections between package and the PCB.

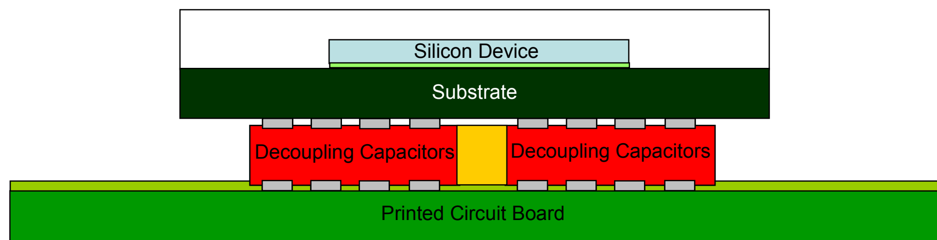


Figure 4: Partial Interposer Configuration D-Pack™.

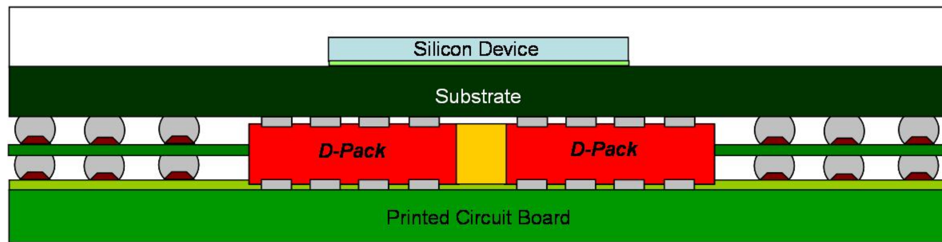


Figure 5: Full Interposer Configuration: *D-Pack*™ (Solder Joints at the periphery).

The objective of this chapter is to evaluate the thermo-mechanical reliability of these interconnect configurations using finite element simulations in ANSYS® and present the failure analysis report of the failed specimens. Life prediction calculations based on Inelastic Strain Energy Density (ΔW) have also been included in the report in order to compare results predicted from finite element models with experimental results. Table 2 shows the *D-Pack*™ configurations that were tested at the Center of Advance Vehicle Electronics (CAVE), Auburn University. The table also includes the details of the solder used in each configuration, the duration of the test as well as the hot / cold dwell times.

Table 2 : Configurations Tested for Thermal Shock Experiments

Configuration	Solder Type	Temperature Range	Dwell Times (Hot / Cold)
Partial Interposer	Sn63-Pb37	0ºC to 100ºC	20 mins. / 20 mins.
Partial Interposer	Sn3.0Ag0.5Cu	0ºC to 100ºC	20 mins. / 20 mins.
Full Interposer	Sn3.0Ag0.5Cu	0ºC to 100ºC	20 mins. / 20 mins.

Figure 6 and Figure 7 figure show actual photographs of the D-Pack assemblies tested.

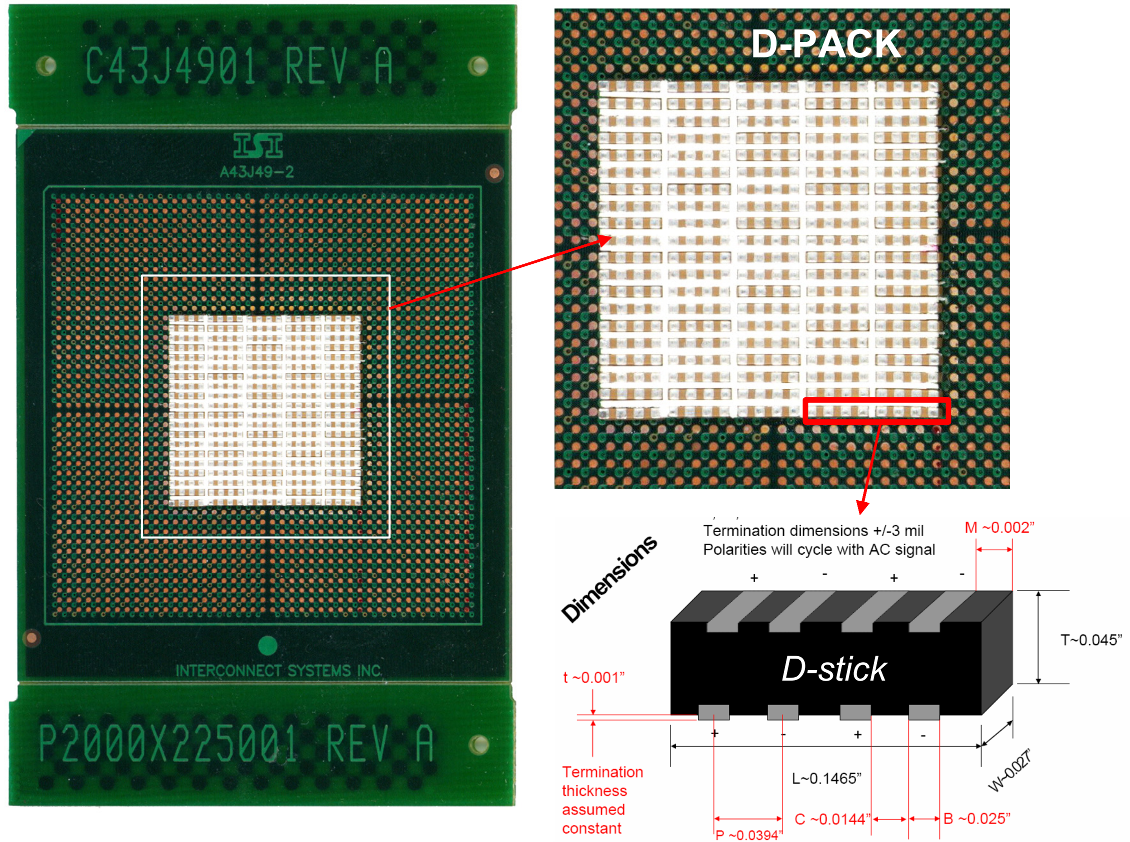


Figure 6: *D-Pack*™ assembled onto test PCB (without LTCC package on top). *D-Pack*™ is a matrix of individual *D-sticks* assembled together. Figure also shows the geometry / dimensions of *D-stick*.

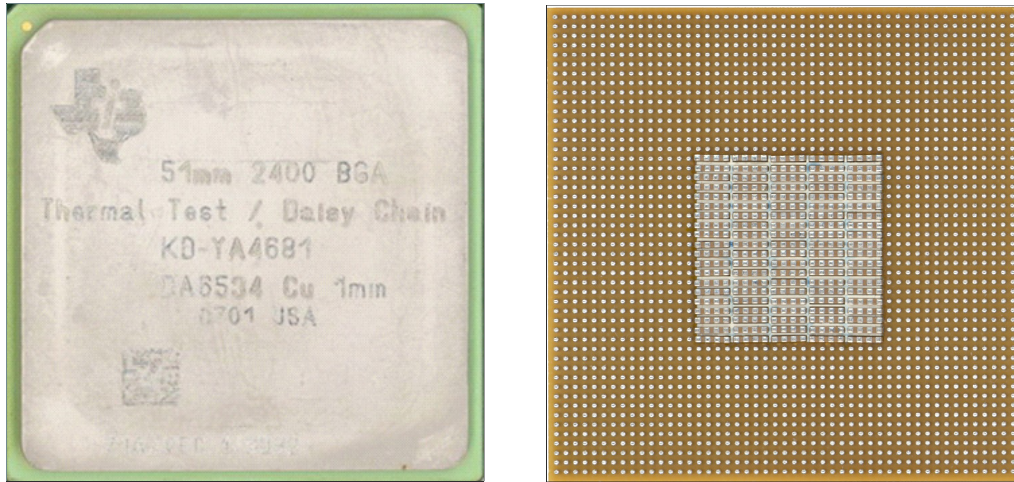


Figure 7: LTCC Package (Top and Bottom View) with D-Pack Assembled onto the Package Land.

In order to capture the true symmetry of the package, quarter symmetry finite element models for both configurations were constructed. Figure 8 and Figure 9 show the quarter symmetry finite element model for partial interposer and full interposer configuration respectively. However, it was observed that the number of nodes in both models exceeded 1 million. Therefore, in view of the file size and the associated computational time for non-linear simulation, it was decided to study the thermo-mechanical reliability using slice models. Figure 10 and Figure 11 show the quarter symmetry finite element model for partial interposer and full interposer configuration respectively.

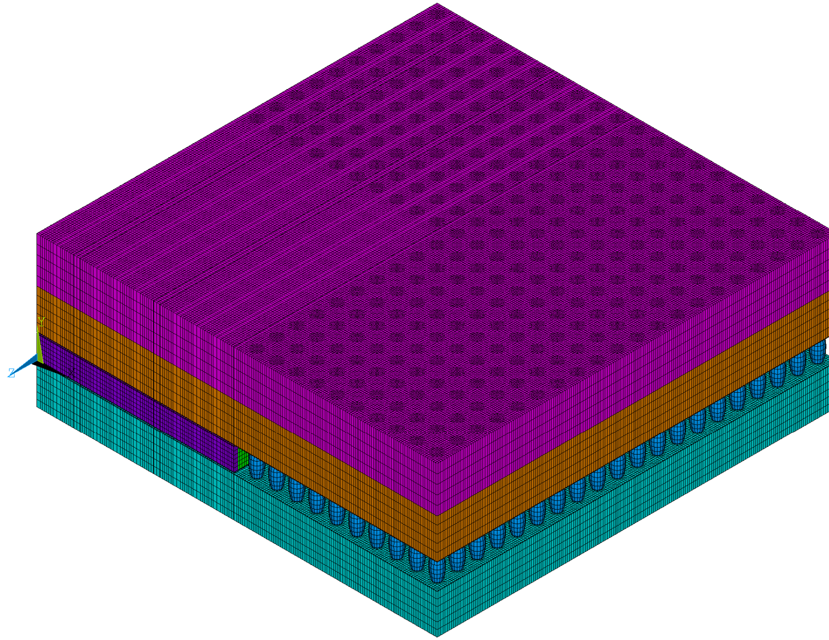


Figure 8: Quarter Symmetry Finite Element Model for *D-Pack*^{TM} Partial Interposer Configuration.

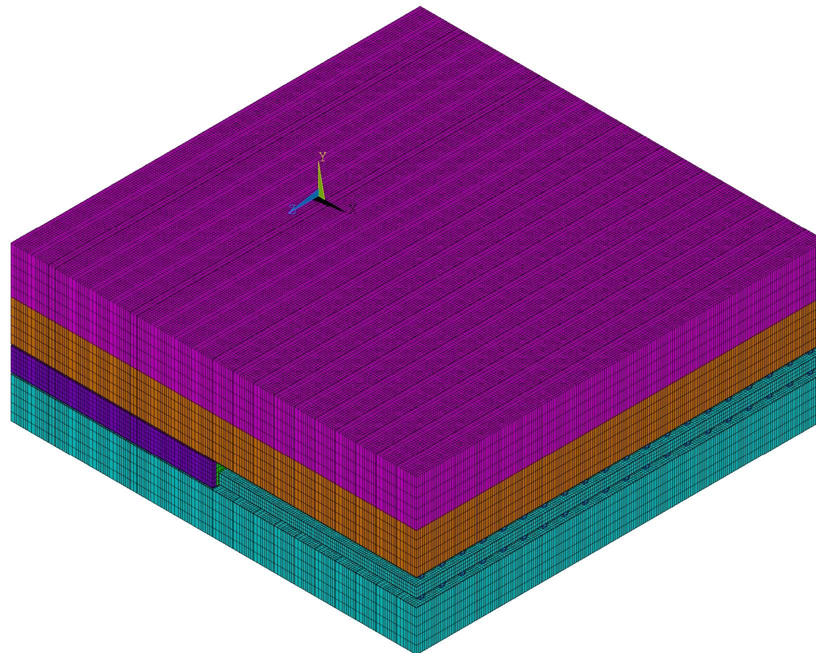


Figure 9: Quarter Symmetry Finite Element Model for *D-Pack*^{TM} Full Interposer Configuration.

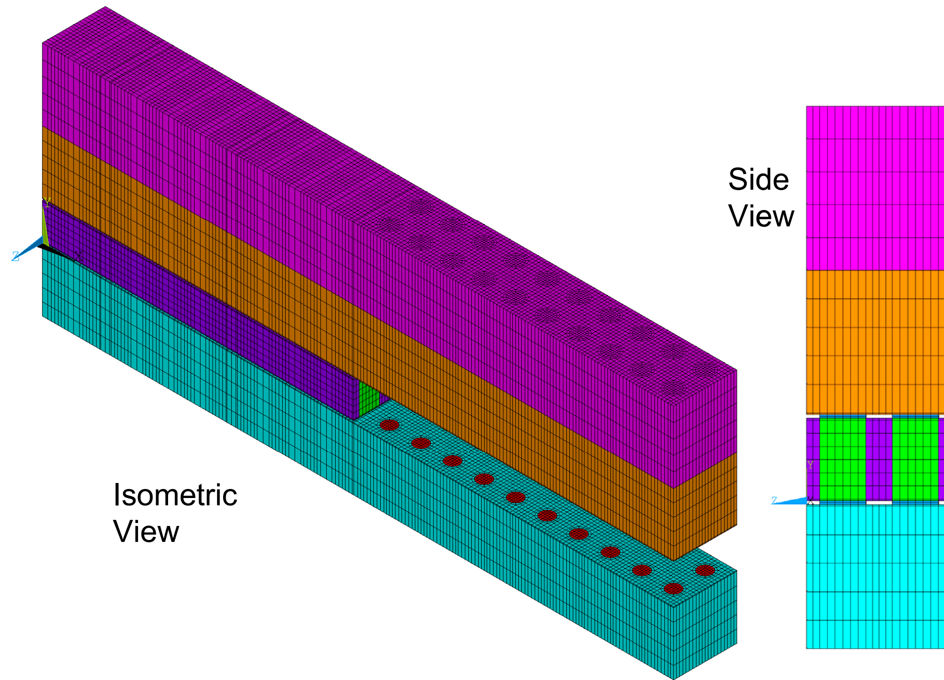


Figure 10: Finite Element Slice Model for *D-Pack*^{TM} Partial Interposer Configuration.

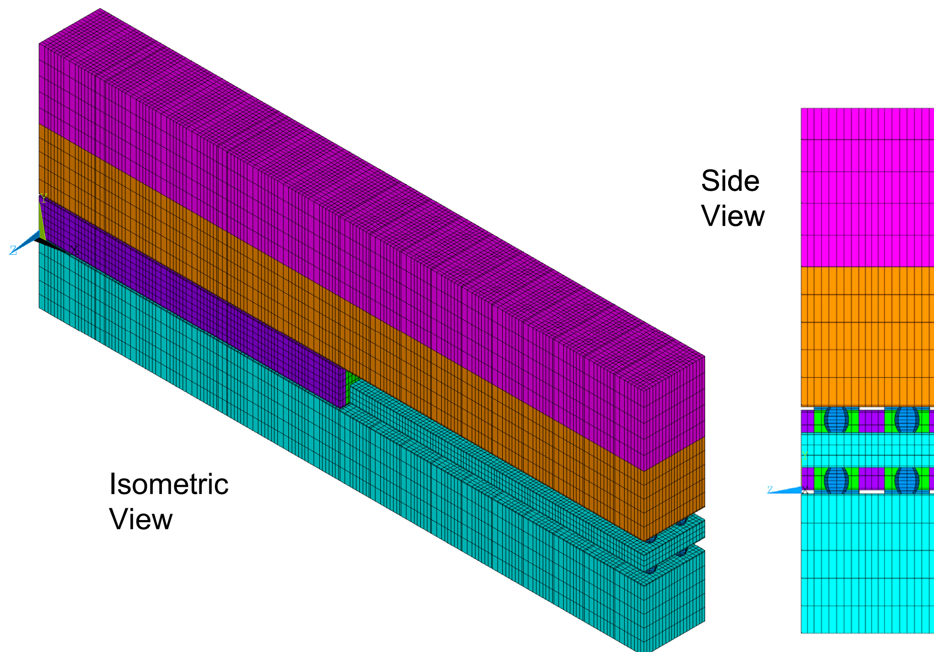


Figure 11: Finite Element Slice Model for *D-Pack*^{TM} Full Interposer Configuration.

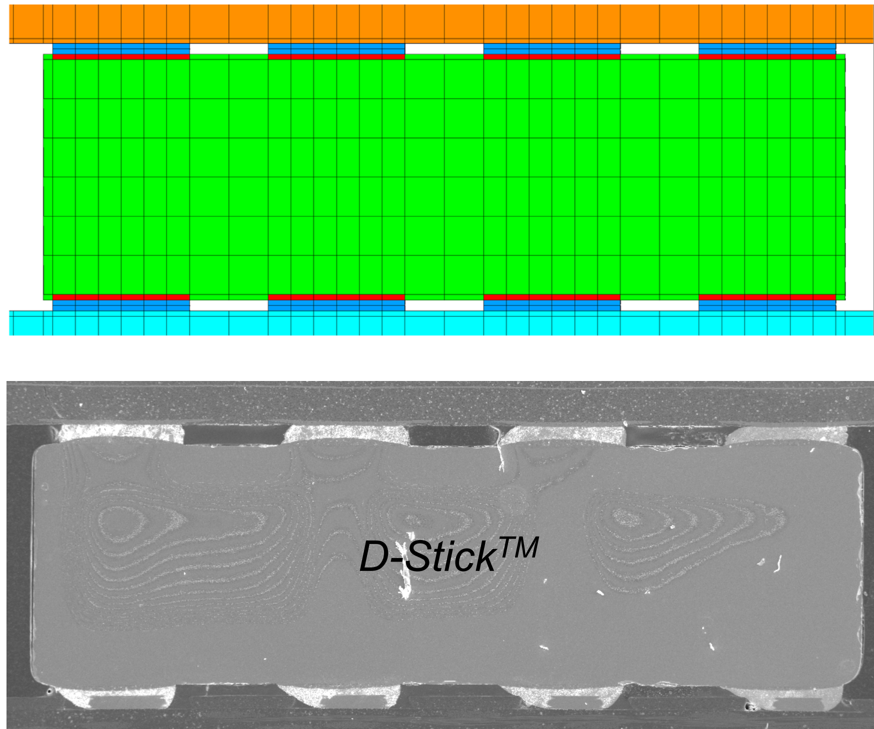


Figure 12: Close up view of *D-Stick*^{TM} (Finite Element mesh) and comparison with actual SEM picture for a pristine assembly.

3.2 Material Models : Constitutive Relationships

In general, a change in temperature causes the mechanical properties and performance of materials to change. Some properties and performance, such as elastic modulus and strength decrease with increasing temperature. Others, such as ductility, increase with increasing temperature. Therefore, in the material modeling of the various materials in the package, constitutive relations that predict strain as a function of stress, temperature, and time should be taken into consideration.

Linear and non-linear, elastic, plastic, creep, temperature, time dependent and time independent material properties have been incorporated in the finite element model. Most of the package materials are considered as linear elastic with no temperature

dependency except solder. It is known that solder is above half its melting point at room temperature and therefore time-dependent creep phenomena dominates the solder joint fatigue life.

The thermal fatigue of electronic packages is associated with combined plastic-deformation and creep of solder joints. The Anand Viscoplasticity model (a standard material in ANSYS library) has been used by several researchers to model the constitutive behavior of the solder. The modeling methodology utilizes finite element analysis to calculate the viscoplastic strain energy density that is accumulated per cycle during thermal cycling. The Anand Viscoplasticity constitutive law has been used by Darveaux [1996, 2000], Zahn [2003] and several other researchers, toward the development of damage relationships. These relationships can be used for the life prediction of the electronic packages with solder joint cracking as the failure mode.

Anand's model [1985] is split into a flow equation and three evolution equations that describe the strain hardening or softening of materials.

Flow Equation:

$$\frac{d\varepsilon_p}{dt} = A(\sinh(\xi\sigma / s_0)^{1/m} \exp\left(\frac{-Q}{kT}\right)$$

Evolution Equations:

$$\frac{ds_0}{dt} = \left\{h_0(|B|)^a \frac{B}{|B|}\right\}\left(\frac{d\varepsilon_p}{dt}\right)$$

$$B = 1 - \frac{s_0}{s^*} \qquad s^* = s^\wedge \left[\frac{\frac{d\varepsilon_p}{dt}}{A} \exp\left(\frac{Q}{kT}\right)\right]^n$$

The nomenclature and the material constants used for simulation are listed in Table 3. Also thermo-mechanical properties used for other material sets are listed in Table 3 below. The solder joints were meshed using element VISCO107, where as the other materials were meshed using SOLID45 in the ANSYS element library.

Table 3: Anand's Constant for SAC105, SAC305 and SAC405

Definition	Sn63-Pb37 [Darveaux 2000]	SAC 305 [Chang 2006]
Initial Value of Deformation Resistance s_0 (MPa)	12.41	45.9
Activation Energy *Q/R* (°K)	9400	7460
Pre-Exponential Factor *A* (sec-1)	4.00×10^6	5.87×10^6
Multiplier of Stress ξ	1.5	2
Strain Rate Sensitivity of Stress *m*	0.303	0.0942
Hardening Constant h_0 (MPa)	1378.95	9350
Coefficient of Deformation Resistance Saturation Value *S^* (MPa)	13.79	58.3
Strain Rate Sensitivity of Saturation Value *n*	0.07	0.015
Strain Rate Sensitivity of Hardening *a*	1.3	1.5

Table 4: Material Properties used for finite element modeling [Zahn 2003]

Material	Modulus of Elasticity (E) MPa	CTE (ppm/°C)	Poisson's ratio
Copper Pad	128,932	16.30	0.34
Solder Mask	3,100	16.3	0.30
Solder (SAC 305)	47,572	25	0.35
Solder (Sn63-Pb37)	30,550	24	0.35
Silicon	162,716	25.4	0.28
Die Adhesive	6,769	52.5	0.25
Substrate	17,890 (X & Z) 7846 (Y)	12.4 (X & Z) 57 (Y)	0.39 (XY & YZ) 0.11 (XZ)
PCB	16,898 (X & Z) 7,436 (Y)	14.50 (X & Z) 67.20 (Y)	0.39 (XY & YZ) 0.11 (XZ)
Mold	23,520	15	0.3

In ANSYS™, VISCO107 element has plastic work (PLWK) as a standard output. Temperature cycling was simulated until total plastic strain energy density accumulated per cycle for the critical solder joint stabilizes. Inelastic work per volume per cycle was calculated for the elements at the interface of the solder interconnect with package pad and board pad. In order to overcome the stress singularity effects, volumetric averaging of inelastic strain-energy density (accumulated per cycle) across a layer of critical elements was done using the following formula:

$$\Delta W_{avg} = \frac{\sum_{k=1}^{N} \Delta W_k V_k}{\sum_{k=1}^{N} V_k}$$

Where ΔW_k is the plastic work for each element, V_k is the volume of each element.

3.3 Finite Element Models: Boundary Conditions

In order to save the computational time and effort, it is more practical to exploit the symmetry of the package. Some of the modeling options used includes quarter symmetry model, 1/8th model, diagonal slice, straight slice, etc. In order to compromise on the computational time, it was decided to explore the diagonal slice symmetry. However, on account of D-Pack™ geometry being unsymmetrical along the diagonal, it was decided to create a straight slice model. The straight slice model extends from the center of a package out to the outermost solder joint (as shown in Figure 13). In this modeling approach, all materials are included through the thickness of the package, and the model captures a full row of solder joints from the center joints to the outermost joints. When the model itself is simplified, the boundary condition choices become more important on the effect of analysis. This slice plane is neither a true symmetry plane nor a free

surface [Zahn 2003]. A compromise between the two options is to couple the surface. For the slice plane surface, a coupling boundary condition of UZ on all nodes on the surface was chosen, and allows the plane to move freely in the Z direction, but is restricted in that plane. All boundary conditions applied for slice models in this research are displayed in Figure 13.

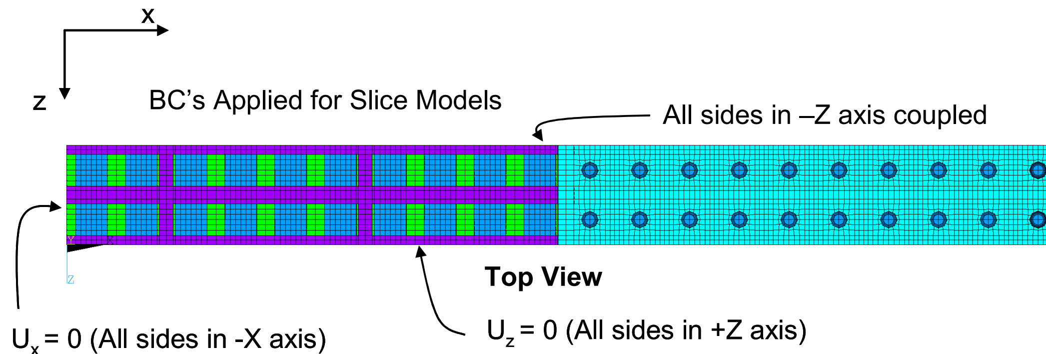


Figure 13: Boundary Conditions applied on the Straight Slice FE model.

3.4 Finite Element Models: Modeling Assumptions

Several assumptions were made in modeling electronic packages. Due to memory limits and computational time, and very complex geometries, intelligent simplifications had to be made to advance the modeling process. The LTCC package used in this study was a Flip Chip BGA (Ceramic Package). It would have been very tedious to incorporate the geometry effects of layers like underfill, solder bumps, thermal insulation material, adhesive between copper lid and substrate, etc. Moreover, in view of the objective to study the thermo-mechanical reliability of the 2nd level interconnects, these layers were not modeled explicitly. However, the physical effects of these layers have been included in the analysis using a smeared property [Clech 1996, 1998] / effective material approach

[Li 2003]. All layers above ceramic substrate were replaced by a single layer of material termed as 'smeared package'. The following equations were used to calculate the effective material properties:

$$h_{eff} = \sum_{k=1}^{n} h_i$$

$$E_{eff} = \frac{\sum_{k=1}^{n} E_i V_i}{\sum_{k=1}^{n} V_i}$$

$$\upsilon_{eff} = \frac{\sum_{k=1}^{n} h_i \upsilon_i}{\sum_{k=1}^{n} h_i}$$

$$(CTE)_{eff} = \frac{\sum_{k=1}^{n} (CTE)_i E_i V_i}{\sum_{k=1}^{n} E_i V_i}$$

where

E = Modulus of Elasticity

υ = Poisson's ratio

h = Layer Thickness

V = Volume

Subscript '*eff*' indicates effective material property

Subscript '*i*' indicates individual layer

Another simplification used in the finite element model was the geometry of solder joints formed at the package / PCB interface with the D-Pack^{TM}. From Figure 12 (SEM image of pristine D-Stick^{TM}), we can see that the geometry of the joints at the

package side and the board side are different from one another. The joint is similar to Non-Solder mask Defined (NSMD) at the package side, and similar to Solder Mask Defined (SMD) at the board side. However, in view of the computational time, mesh continuity due to complex NSMD mesh geometry, joints at both interface were modeled as SMD.

Other simplifications include modeling the Ceramic Substrate and PCB board as homogeneous materials. In reality, these two components have several layers, adhesive, and traces. These features require extensive time to model, and due to their extremely small size relative to the package structure, their effect on the simulation results has been safely assumed to be minimal. Therefore these minute details have not been included in the model.

Also, it is known that strains near the solder joint interface (due to thermal cycling) can alter the chemical composition and grain structure of the alloy. However, finite element methodology currently does not offer the convenience of incorporating the changes in microstructure on account of thermal strains. Therefore, the intermetallics and the changes occurring in the solder joint microstructure have not been included in the analysis.

3.5 Post-Processing Results: Partial Interposer (Eutectic Sn-Pb Solder Joints)

The Partial Interposer package was modeled in ANSYS 10.0 with two solders (eutectic Sn-Pb and SAC 305) and subjected to thermal cycling in order to estimate plastic work accumulation to determine the reliability in a finite element simulation framework. In case of Partial Interposer configuration, mechanical and electrical

interconnections between the package and PCB were formed by the solder joints on the top and bottom terminations of the D-Pack^{TM}. Figure 14 shows the finite element slice model used. Two cycles were simulated in order to stabilize the stress – strain hysteresis loop. The area under the hysteresis loop was used to make life prediction calculations.

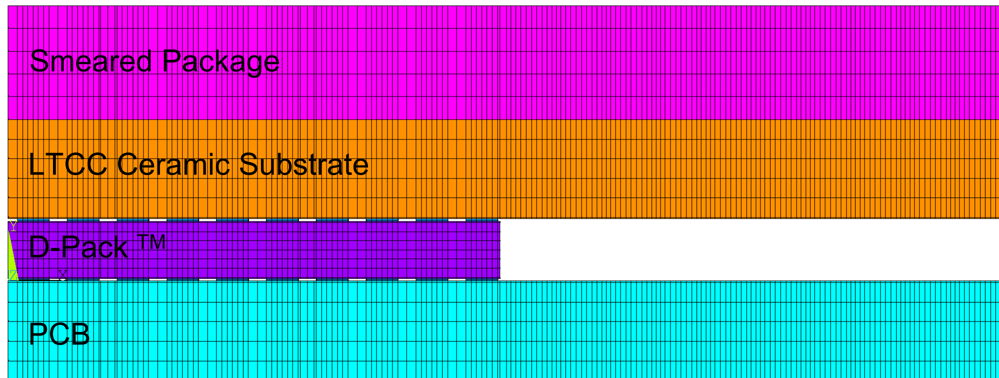


Figure 14: Finite Element Slice Model for Partial Interposer Configuration: Front View (2 Solders Tested: Eutectic Sn-Pb and SAC 305).

Figure 15 and

Figure 16 show the plots for accumulation of plastic work after simulation of two thermal cycles (0ºC to 100ºC, 20 min dwell /ramps) for eutectic Sn-Pb solder. It was seen that the D-Pack^{TM} solder joints farthest from package center were subjected to maximum amount of plastic work. Figure 17 shows the hysteresis loop for the solder element that underwent maximum amount of plastic work accumulation.

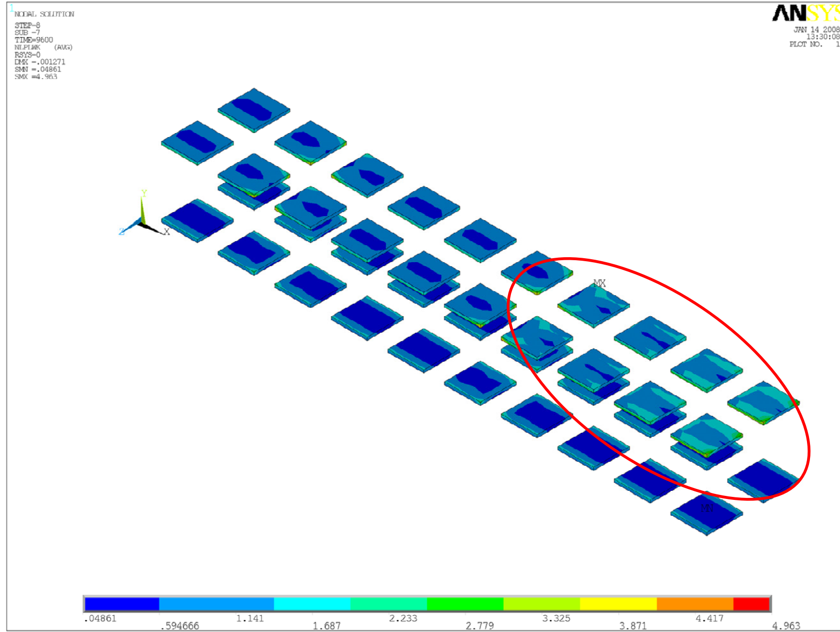


Figure 15: Contour plot of accumulated plastic work on the D-Pack^{TM} solder joints (Partial Interposer with eutectic Sn-Pb solder) at the end of two thermal cycles.

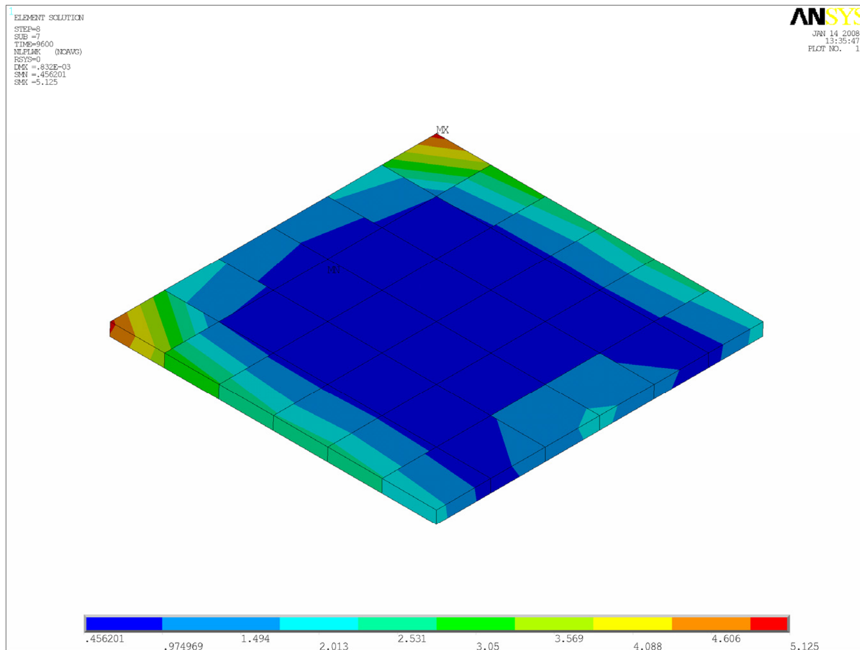


Figure 16: Plastic Work / Volume plot for critical of solder element layer (Partial Interposer with eutectic Sn-Pb solder) that was subjected to maximum plastic damage at the end of two thermal cycles.

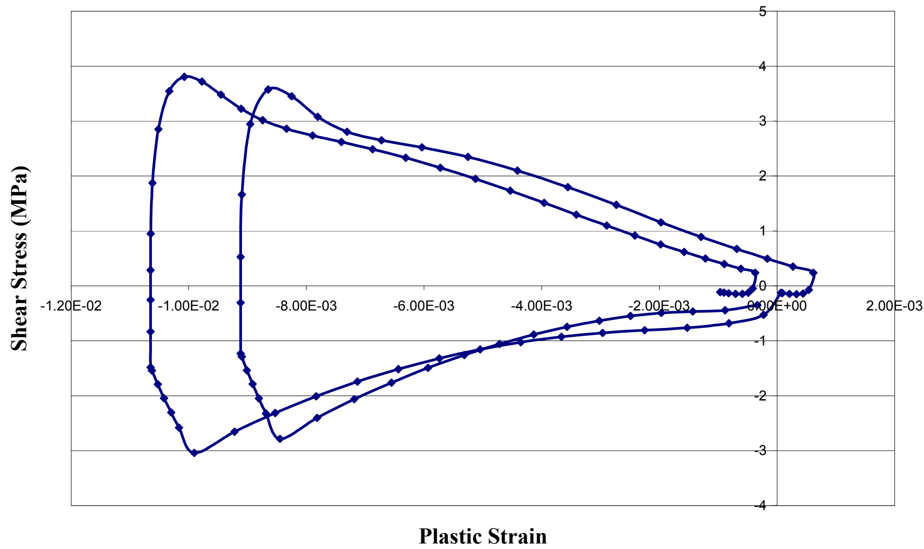


Figure 17: Hysteresis plot (Shear Stress vs. Plastic Strain) for the critical solder joint element (eutectic Sn-Pb) that was subjected to maximum plastic damage at the end of two thermal cycles.

In order to overcome the stress singularity effects, volumetric averaging of inelastic strain-energy density (accumulated per cycle) across a layer of critical solder joint elements was done. The value was found out to be 0.5912 MPa.

Since the D-Pack is a multi-layer capacitor, and dielectric cracking is a very common mode of failure found in multilayer capacitors subjected to high temperatures, the variation of maximum principal stress generated in the dielectric during thermal cycling was also plotted versus time. Figure 18 shows the variation of maximum principal stress in the dielectric vs. time for two thermal cycles. It can be seen that that stress is maximum (~315 MPa) at the lowest temperature.

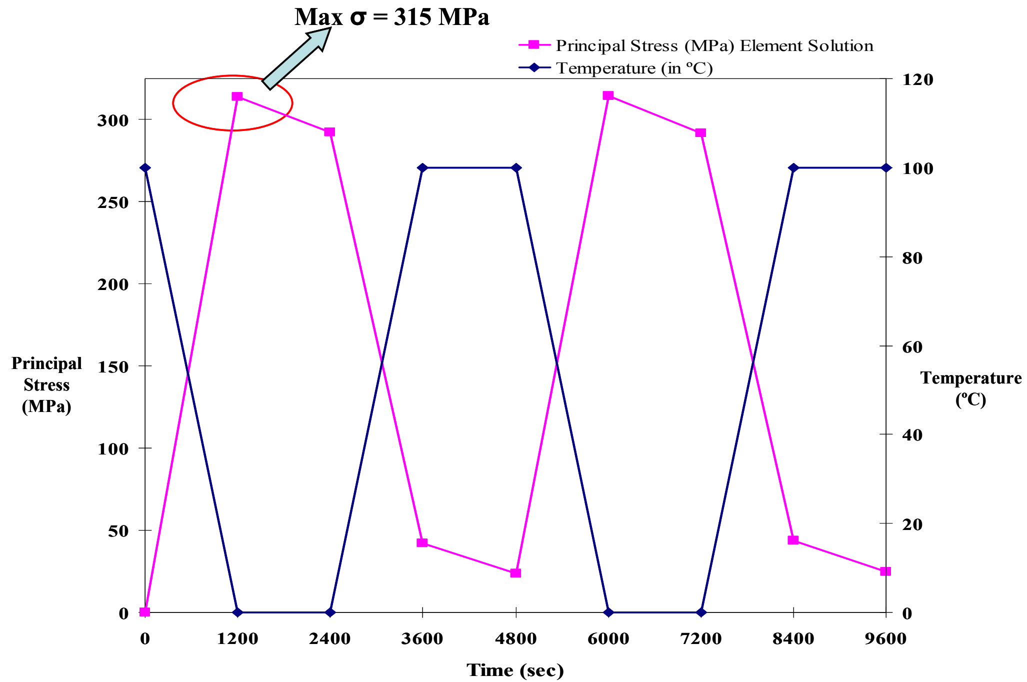


Figure 18: Variation of maximum principal stress in dielectric versus time, temperature.

3.6 Post-Processing Results: Partial Interposer (SAC 305 Solder Joints)

Figure 19 and Figure 20 show the plots for accumulation of plastic work after simulation of two thermal cycles (0ºC to 100ºC, 20 min dwell /ramps) for partial interposer configuration with eutectic SAC solder. Similar to partial interposer with eutectic Sn-Pb joints, it was seen that the D-Pack^{TM} solder joints farthest from package center were subjected to maximum amount of plastic work. Figure 17 shows the hysteresis loop for the solder element that underwent maximum amount of plastic work accumulation.

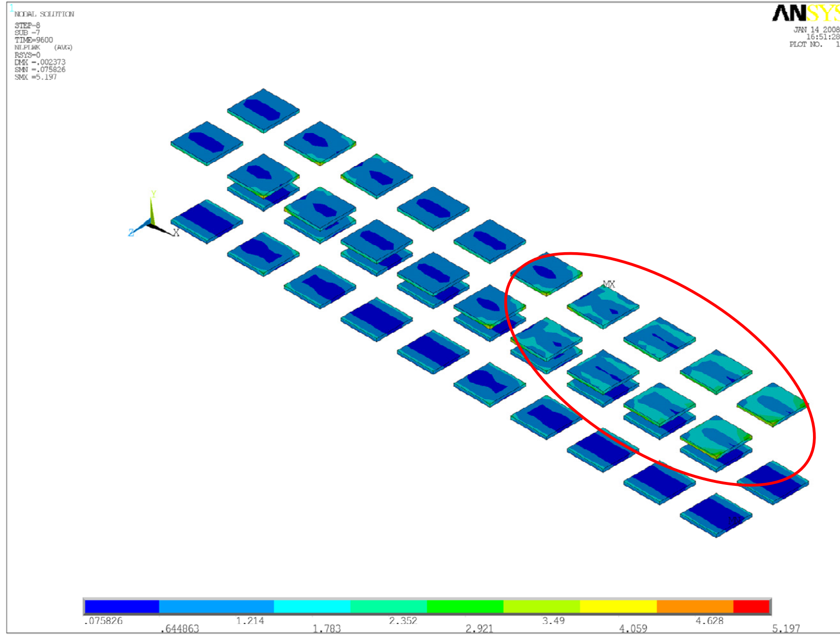


Figure 19: Contour plot of accumulated plastic work on the D-Pack™ solder joints (Partial Interposer with SAC 305) at the end of two thermal cycles.

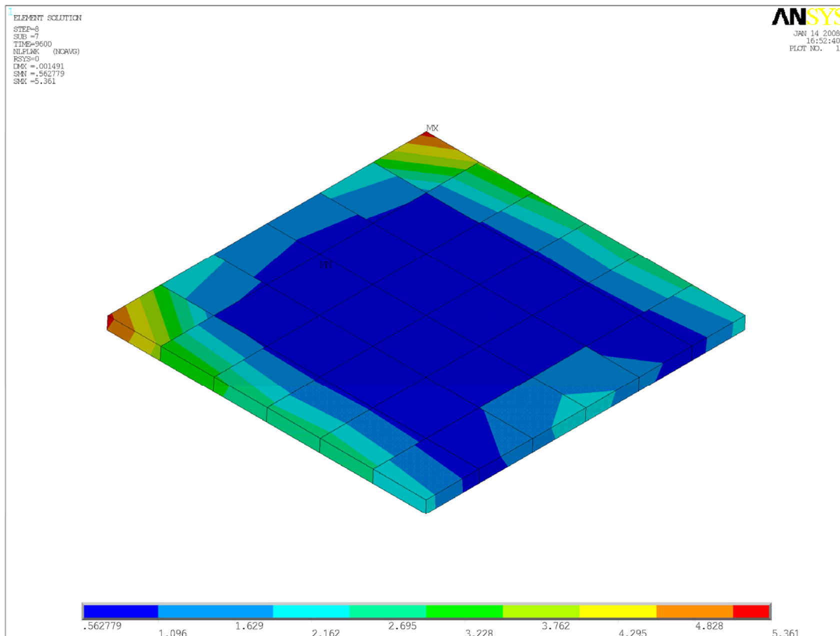


Figure 20: Plastic Work / Volume plot for critical of solder element layer (Partial Interposer with SAC 305 solder joints) that was subjected to maximum plastic damage at the end of two thermal cycles.

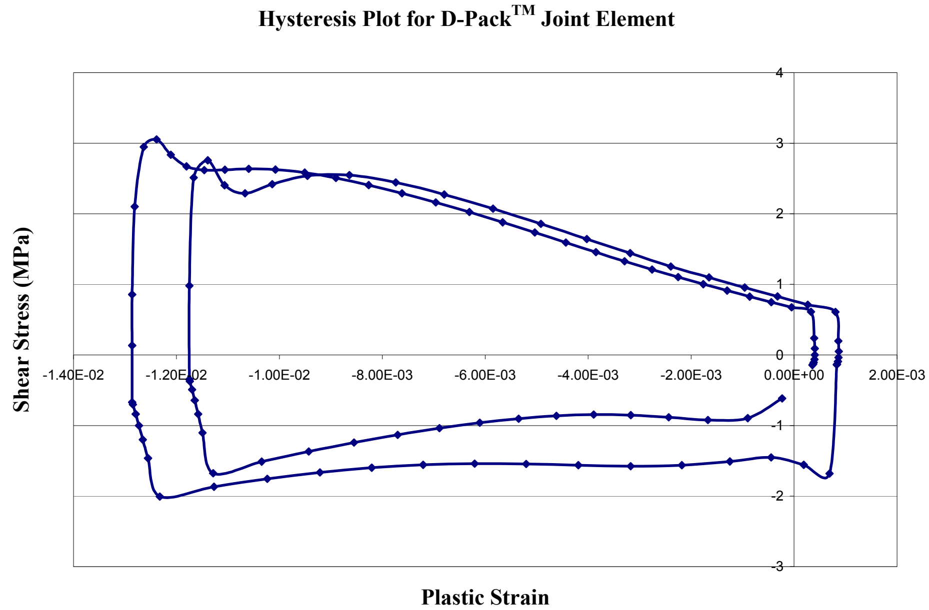


Figure 21: Hysteresis plot (Shear Stress vs. Plastic Strain) for the critical solder joint element (Partial Interposer with SAC 305 solder) that was subjected to maximum plastic damage at the end of two thermal cycles.

In this case, the volumetrically averaged value of inelastic strain-energy density (accumulated per cycle) across a layer of critical solder joint elements was found out to be 0.643 MPa. Figure 22 shows the variation of maximum principal stress in the dielectric vs. time for two thermal cycles. The nature of variation of principal stress was very similar to partial interposer with eutectic Sn-Pb joints, though the magnitude was found to be lower (~291 MPa).

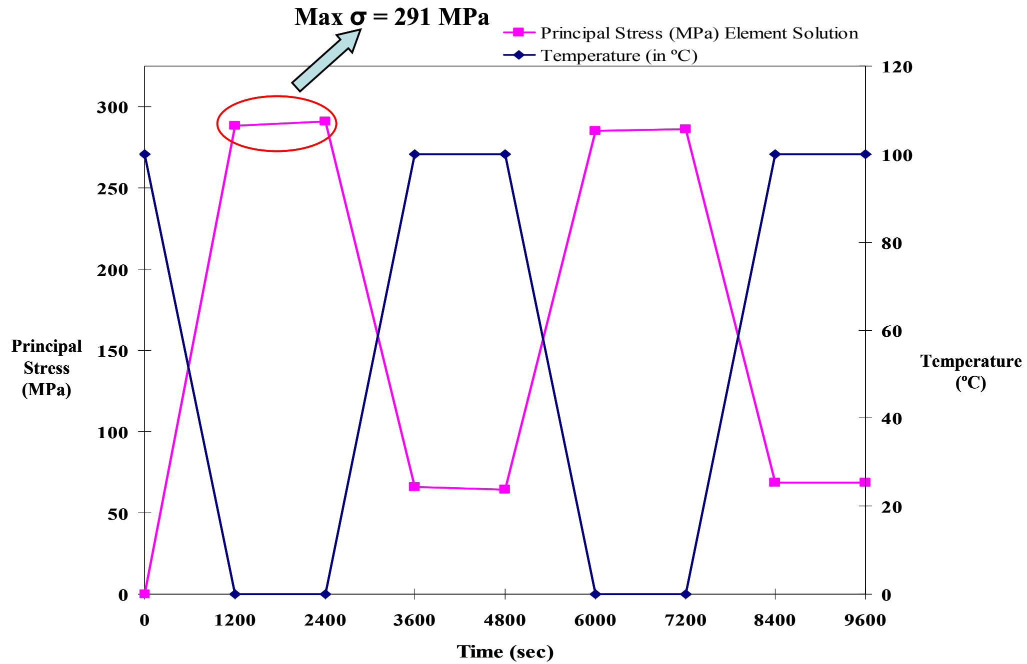


Figure 22: Variation of maximum principal stress in dielectric versus time, temperature.

3.7 Post-Processing Results: Full Interposer (SAC 305 Solder Joints)

For Full Interposer, in addition to the *D-Pack*™ capacitor matrix at the central core, the package was assembled using an intermediate layer of FR-04 PCB with two rows of spherical solder balls forming the electrical and mechanical connections between package and the PCB. Figure 23 shows the slice model used in the analysis.

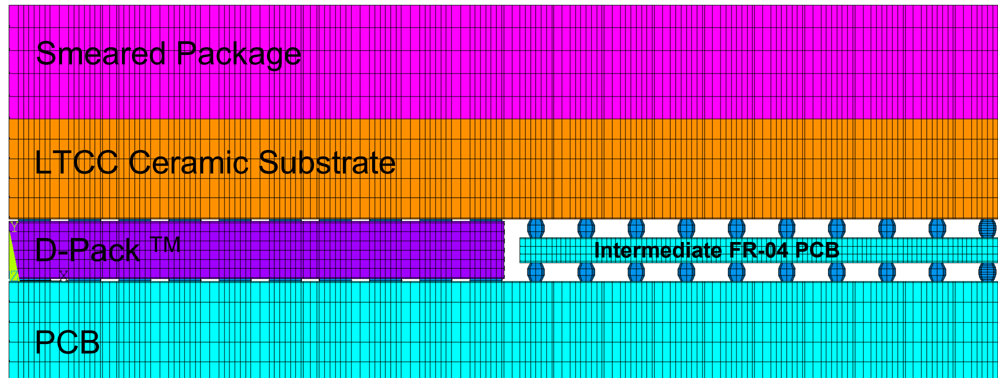


Figure 23: Finite Element Slice Model for Full Interposer Configuration: Front View (SAC 305 solder).

Figure 24 to Figure 27 show the plots for accumulation of plastic work after simulation of two thermal cycles (0ºC to 100ºC, 20 min dwell /ramps) for SAC 305 solder. There were two solder joint geometries that were to be analyzed from the point of view of thermo-mechanical reliability, D-Pack™ joints and the periphery joints (spherical). In both cases it was seen that the solder joints farthest from package center were subjected to maximum amount of plastic work, though the damage accumulation for D-Pack™ was considerably more. Figure 29 and Figure 30 shows the hysteresis loop for the solder element (D-Pack joint and periphery joint respectively) that underwent maximum amount of plastic work accumulation.

In this case, the volumetrically averaged value of inelastic strain-energy density (accumulated per cycle) across a layer of critical solder joint elements was found out to be 0.62 MPa (D-Pack joint) and 0.2233 MPa (spherical periphery joint). Figure 31 shows the variation of maximum principal stress in the dielectric vs. time for two thermal cycles (Max value was ~ 291 MPa).

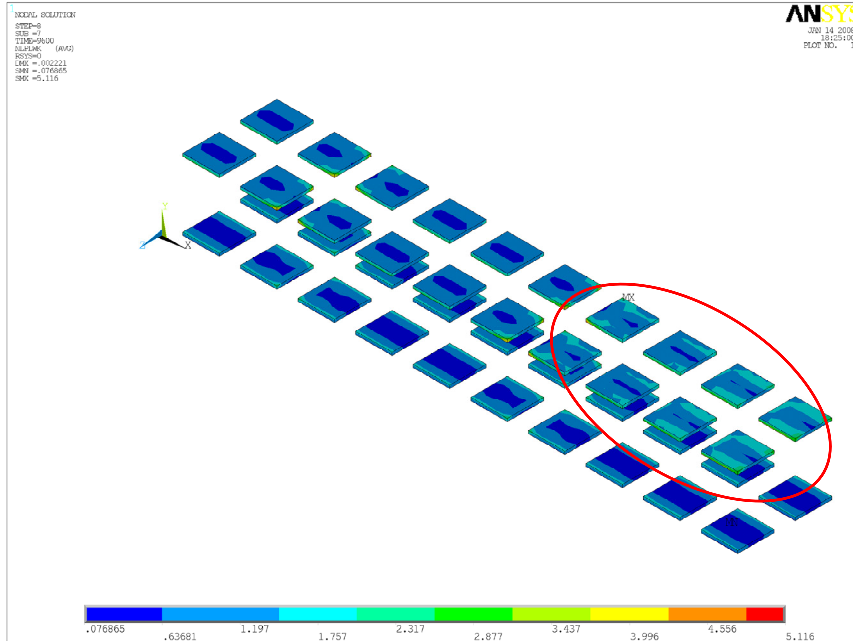


Figure 24: Contour plot of accumulated plastic work on the D-Pack^{TM} solder joints (Full Interposer with SAC 305 solder) at the end of two thermal cycles.

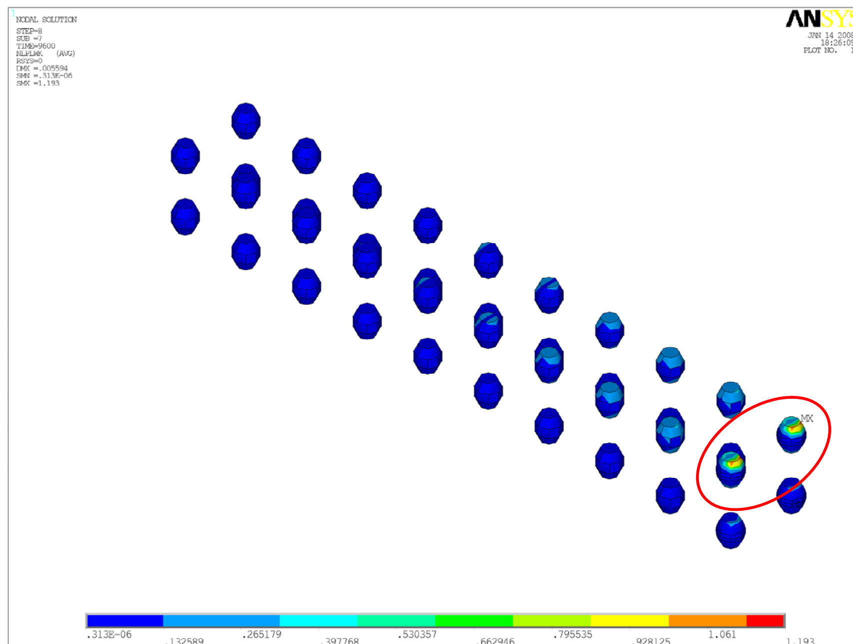


Figure 25: Contour plot of accumulated plastic work on the periphery solder joints (SAC 305 solder) at the end of two thermal cycles.

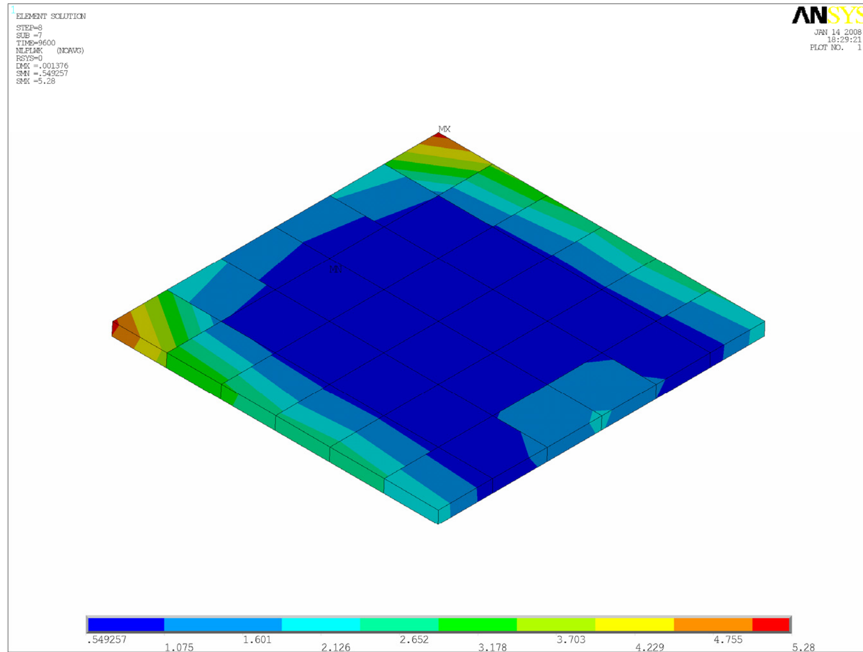


Figure 26: Plastic Work / Volume plot for critical of solder element layer in the D-Pack™ joint (Full Interposer with SAC 305 solder) at the end of two thermal cycles.

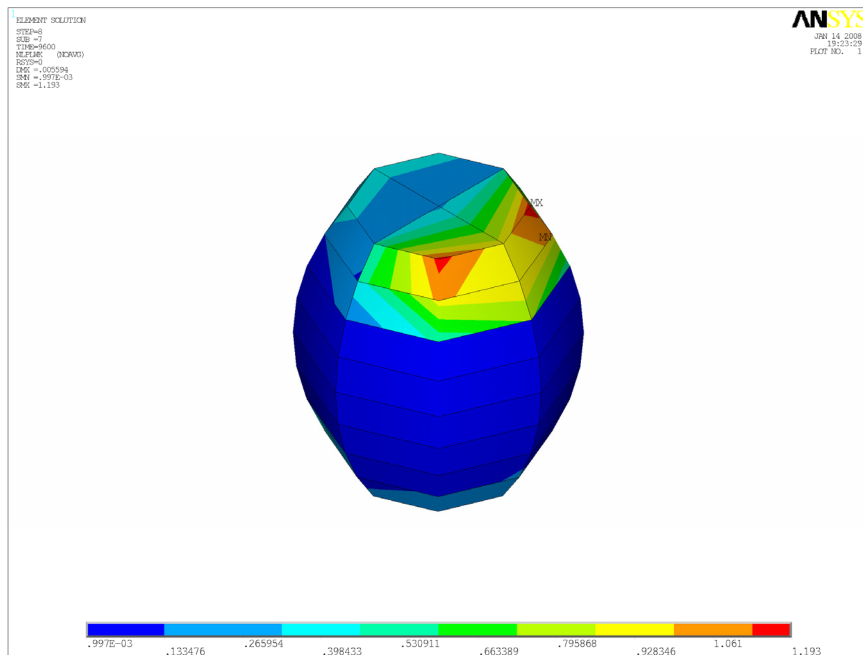


Figure 27: Plastic Work / Volume plot for critical solder ball in the periphery joints (Full Interposer with SAC 305 solder) at the end of two thermal cycles.

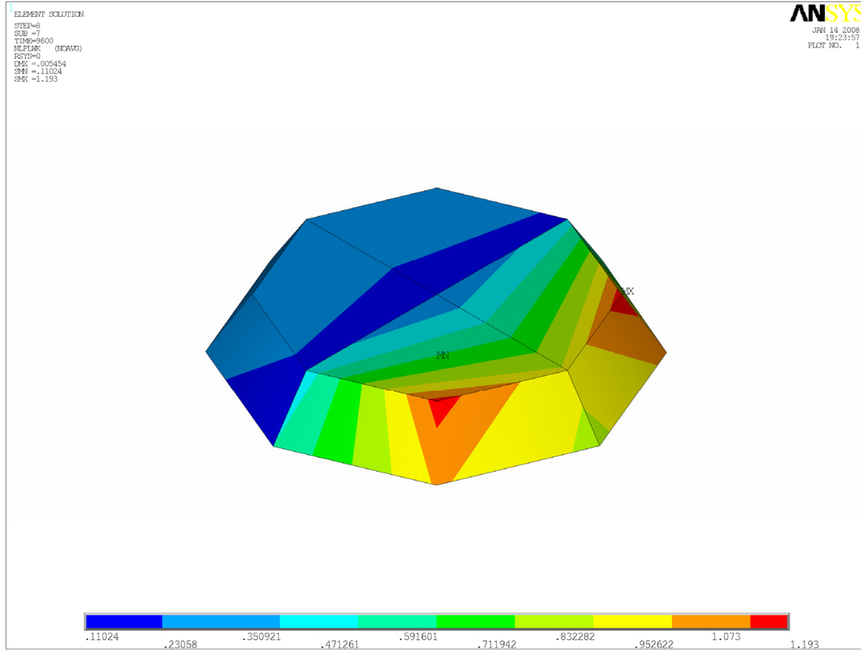


Figure 28: Plastic Work / Volume plot for critical element layer in the periphery solder joints (Full Interposer with SAC 305 solder) at the end of two thermal cycles.

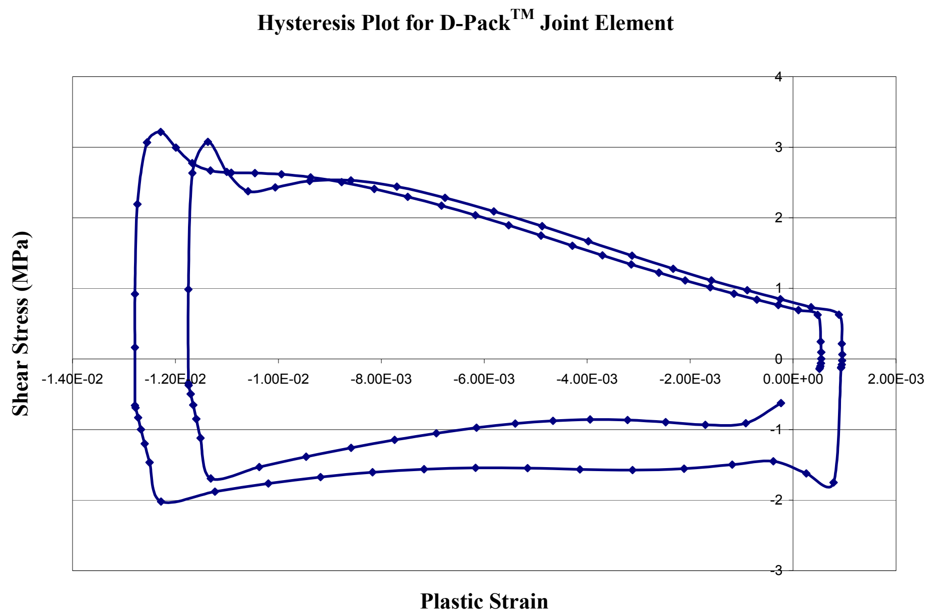


Figure 29: Hysteresis plot (Shear Stress vs. Plastic Strain) for the critical D-Pack™ solder joint element (eutectic Sn-Pb) at the end of two thermal cycles.

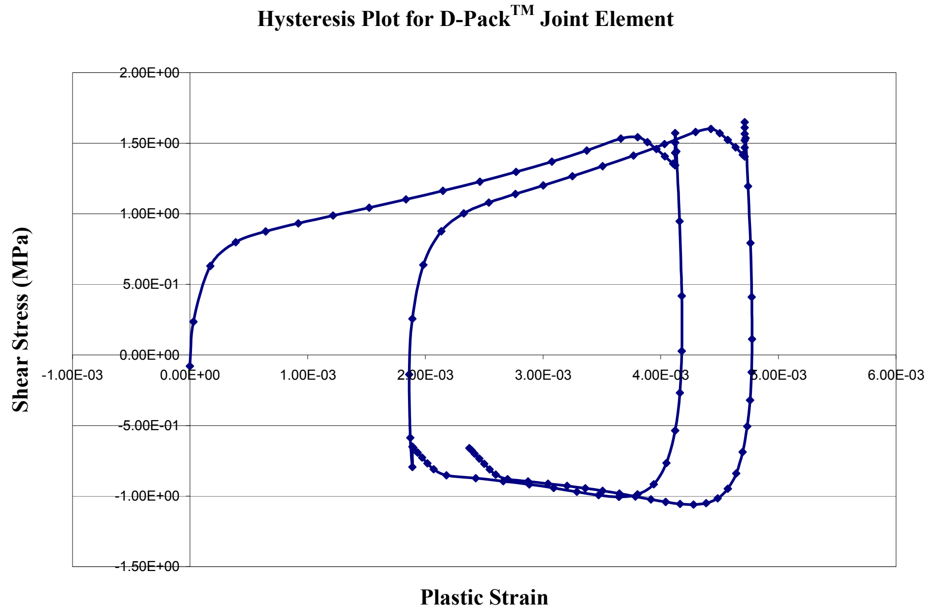


Figure 30: Hysteresis plot (Shear Stress vs. Plastic Strain) for the critical periphery solder joint element (SAC 305) at the end of two thermal cycles.

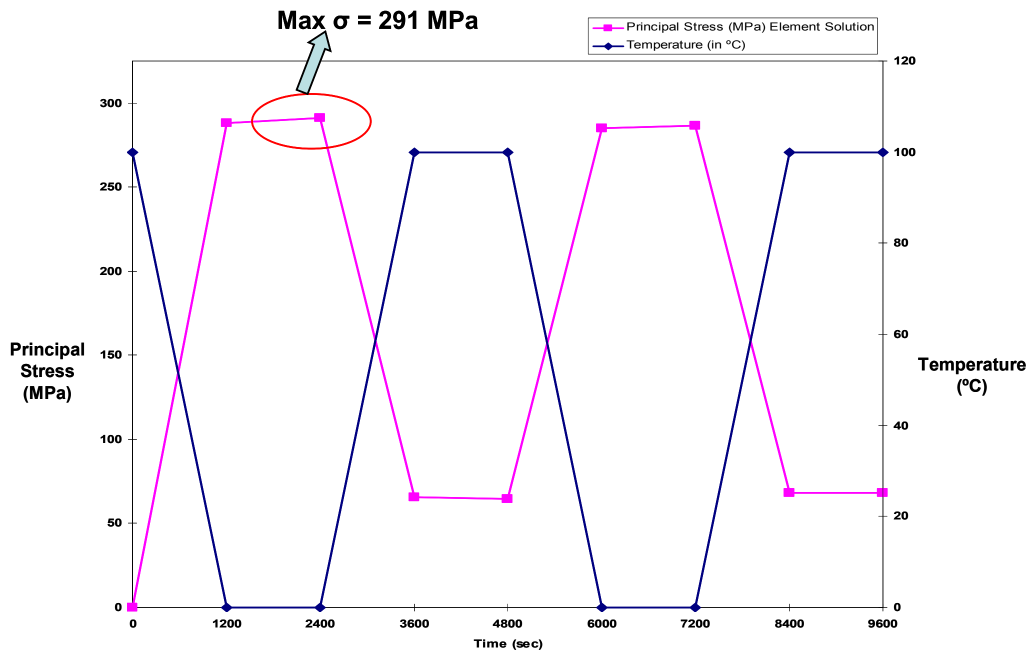


Figure 31: Variation of maximum principal stress in dielectric versus time, temperature.

3.8 Post-Processing Results: Regular BGA (SAC 305 Solder Joints)

In order to compare the reliability of D-Pack configurations with contemporary packages being used, a BGA slice model was created with same material sets, same boundary conditions and subjected to same temperatures and ramp rates. Figure 32 shows the slice model used for analysis.

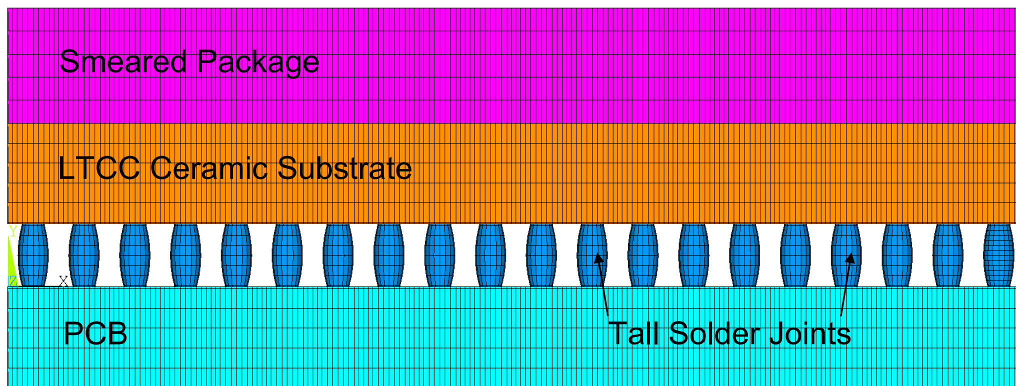


Figure 32: Finite Element Slice Model for BGA Configuration: Front View (SAC 305 solder).

Figure 33 and Figure 35 show the plots for accumulation of plastic work after simulation of two thermal cycles (0ºC to 100ºC, 20 min dwell /ramps) for SAC 305 solder. It was seen that the solder joints farthest from package center were subjected to maximum amount of plastic work. Figure 36 shows the hysteresis loop for the solder element that underwent maximum amount of plastic work accumulation.

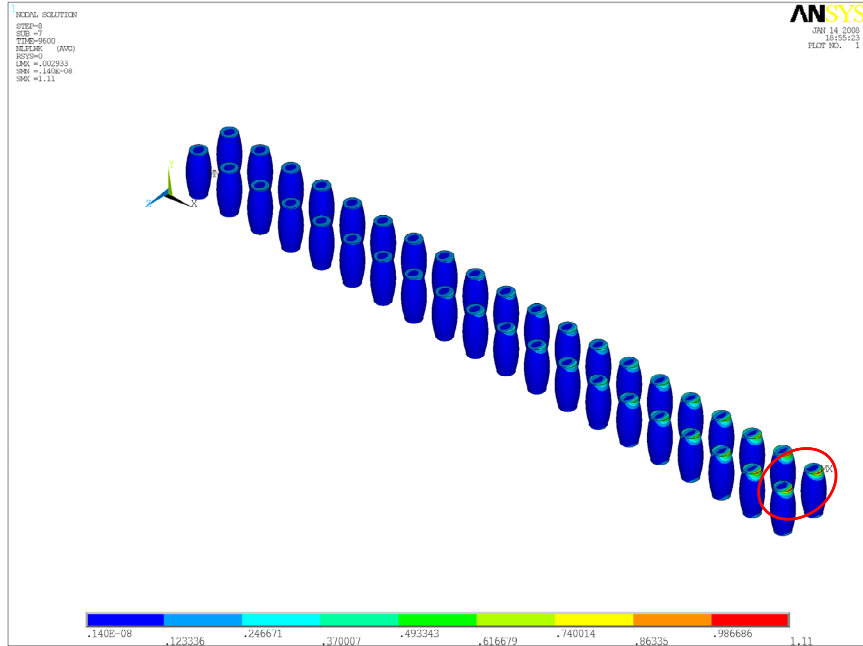


Figure 33: Contour plot of accumulated plastic work on the tall solder joints (Regular BGA with SAC 305 solder) at the end of two thermal cycles.

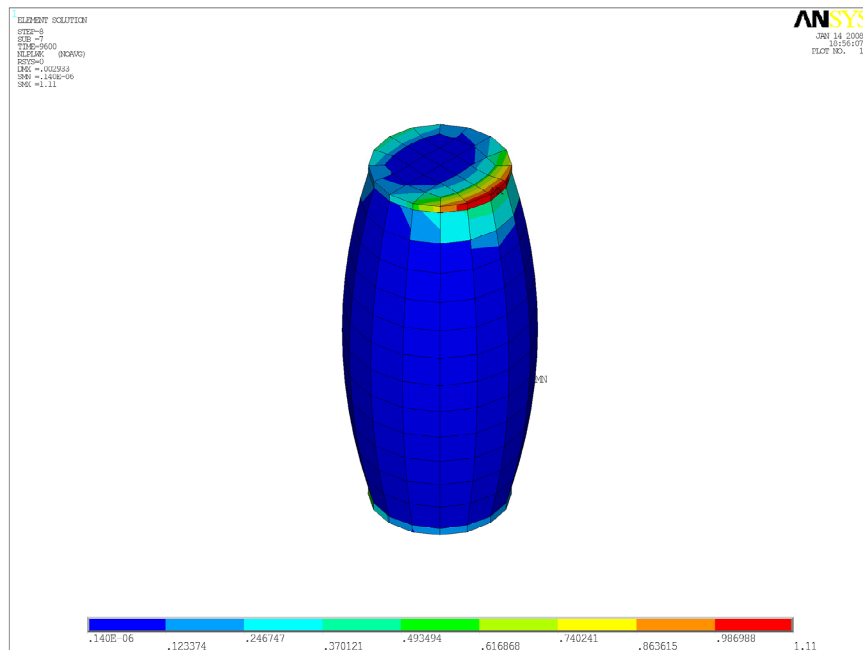


Figure 34: Plastic Work / Volume plot for critical of solder ball (Regular BGA with SAC 305 solder) subjected to maximum plastic damage at the end of two thermal cycles.

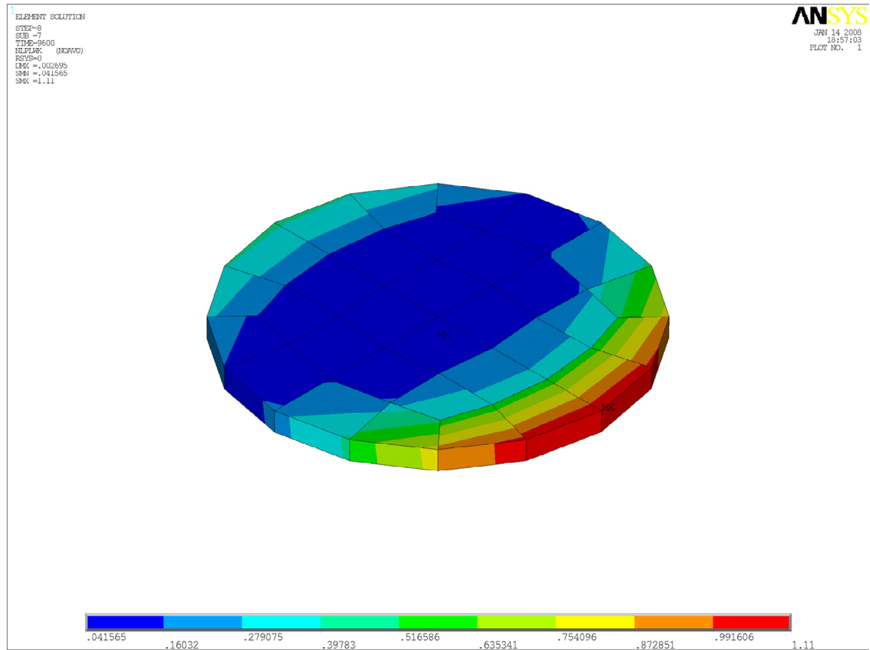


Figure 35: Plastic Work / Volume plot for critical element layer in the tall joint (Regular BGA with SAC 305 solder) at the end of two thermal cycles.

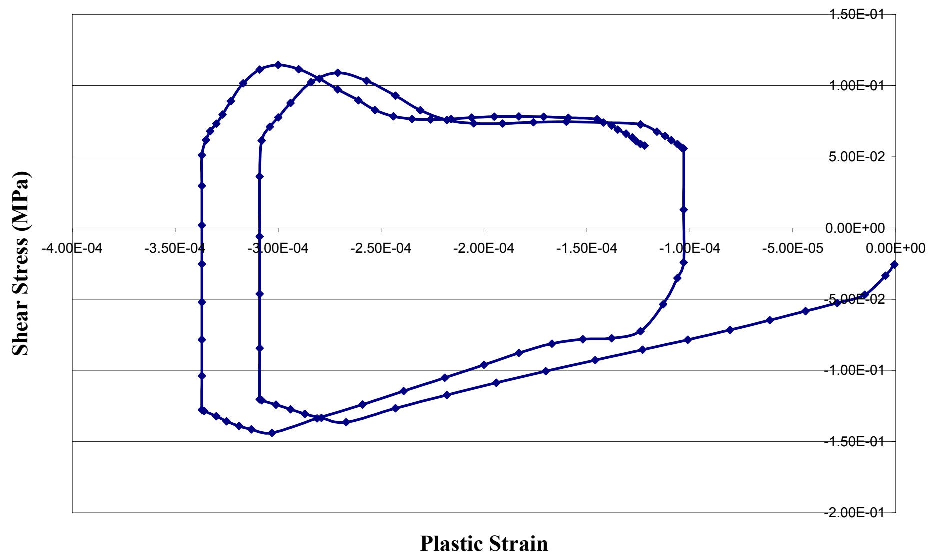


Figure 36: Hysteresis plot (Shear Stress vs. Plastic Strain) for the critical solder joint element subjected to maximum plastic damage at the end of two thermal cycles.

In this case, the volumetrically averaged value of inelastic strain-energy density (accumulated per cycle) across a layer of critical solder joint elements was found out to be 0.1276 MPa.

3.9 Results Summary:

The results obtained for simulation for various configurations are summarized in Table 5 below. Using visco-plastic strain energy density as a metric for life prediction calculations, it can be seen that regular BGA (with tall solder joints) performs considerably better than all the other configurations analyzed. Also, based on the fatigue testing data on $BaTiO_3$ and S-N curves generated [Tanimoto et al. 1992] it can be safely assumed that for a cyclic stress of magnitude 315 MPa, D-Pack^{TM} dielectric would likely crack at approximately 10^6 cycles (well beyond the desired life cycle duration).

Table 5 : Results Summary

Configuration	Solder	Joint Type	Plastic Work (ΔW) MPa	Max Principal Stress (in Dielectric) MPa
Partial Interposer (No Outer Joints)	Sn – Pb	D-Pack	0.591	315
	SAC 305	D-Pack	0.643	292
Full Interposer	SAC 305	D-Pack	0.620	292
		Periphery Solder Ball	0.223	
BGA (Tall Joints)	SAC 305	Tall Solder Ball	0.127	NA

3.10 Life Prediction vs. Experimental data:

Based on simulation and experimental data for several test configurations, different temperatures ranges, different ramp / dwell rates, Darveaux [1996, 2000], Zahn [2003] and several other researchers have developed empirical life prediction relationships. In these studies, Inelastic Strain Energy Density obtained from finite element simulation framework was correlated with the test failure data and empirical relationships were developed to predict the number of cycles to failure. The mode of failure considered for this study was solder joint cracking on account of fatigue.

In this study, empirical relationships presented by Zahn [2003] have been used to calculate the cycles to failure for both eutectic Sn-Pb as well as lead free solder joints. The form of the equation used in this study is as follows:

$$N_{63.2} = C_1 \left(\Delta W \right)^{C_2}$$

Where

ΔW – Averaged inelastic strain energy density at the solder / pad interface.

C_1, C_2 – Constants obtained by correlating the test data with simulation.

Table 6 below summarizes the life prediction calculations based on ΔW calculated for the various D-Pack constructions analyzed above. Figure 39 shows the hysteresis loops (for critical element in solder joint) for various configurations analyzed.

Table 6: Life Prediction Calculations (Summary)

Configuration	Solder	Joint Type	Plastic Work (ΔW) MPa	Characteristic Life $N_{63.2\%}$ (Cycles to failure)
Partial Interposer	Sn – Pb	D-Pack	0.591	2143
	SAC 305	D-Pack	0.643	2814
Full Interposer	SAC 305	D-Pack	0.620	2833
		Periphery Solder Ball	0.223	3322
BGA (Tall Joints)	SAC 305	Tall Solder Ball	0.127	3627

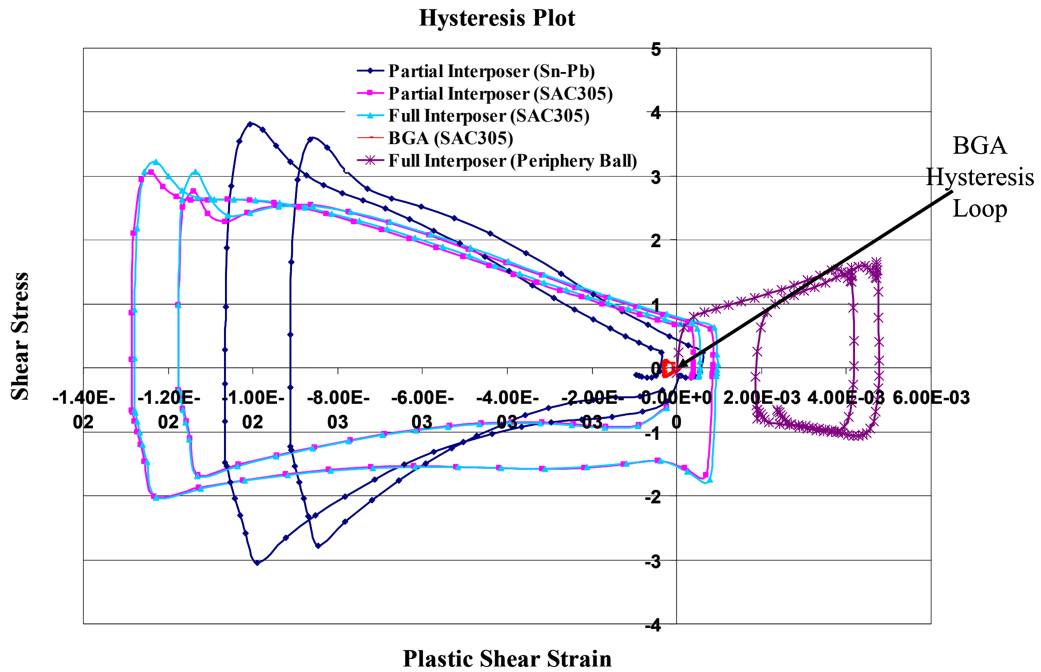


Figure 37: Hysteresis loops (for critical element in solder joints) for various configurations analyzed.

Since the stabilization of hysteresis loop implies a constant rate of damage accumulation with each cycle, it can be reasonably concluded that BGA configuration undergoes least amount of damage/cycle, and therefore would have the largest characteristic life. Figure 38 and Figure 39 show the two-parameter Weibull plots for thermal shock experiments conducted for partial and full interposer configurations.

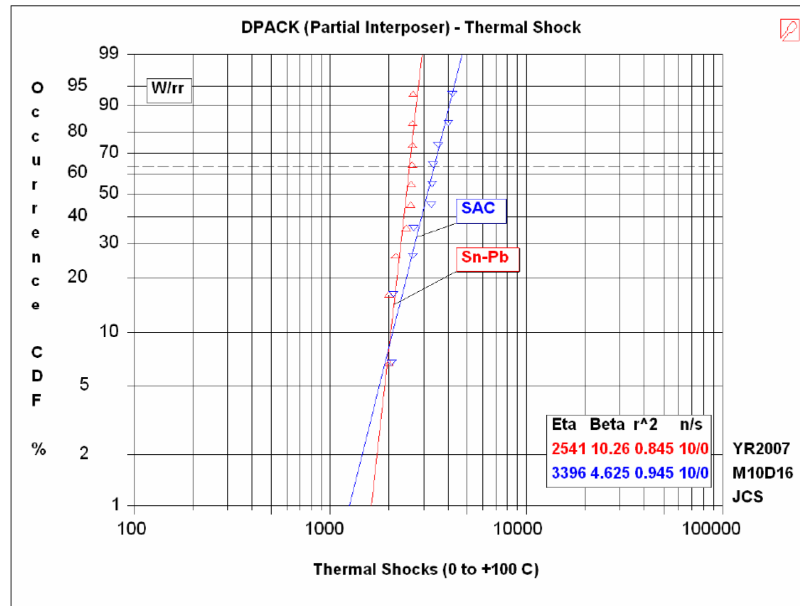


Figure 38: Two parameter Weibull plot for Thermal Shock Experiments (0ºC to 100ºC, 20 min ramp / dwell) on D-Pack Partial Interposer test assemblies (with both Sn-Pb and SAC solder)

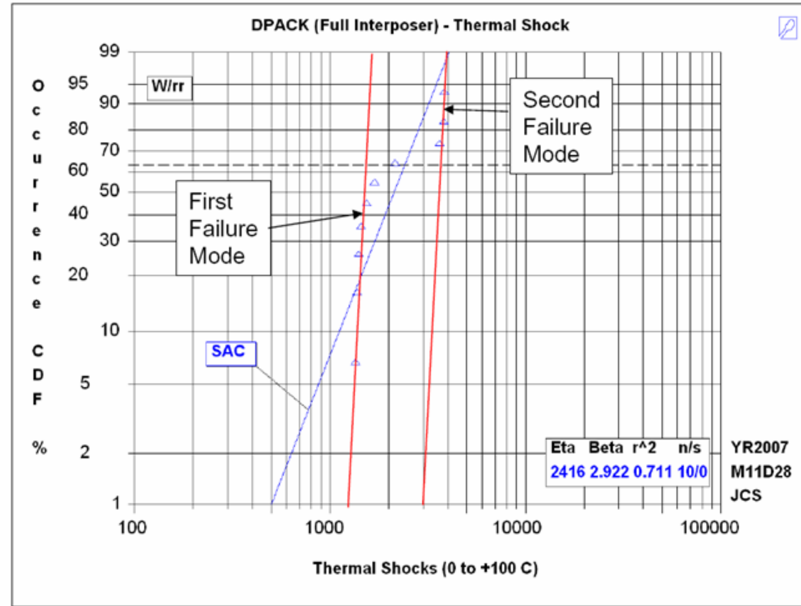


Figure 39: Two parameter Weibull plot for Thermal Shock Experiments (0ºC to 100ºC, 20 min ramp / dwell) on D-Pack Full Interposer test assemblies (with SAC solder)

Figure 40 shows the comparison of life data based on thermal shock experiments with life prediction based on simulations. We see that life predicted from simulations is within ± 20% of the experimental data, which is within the acceptable limits.

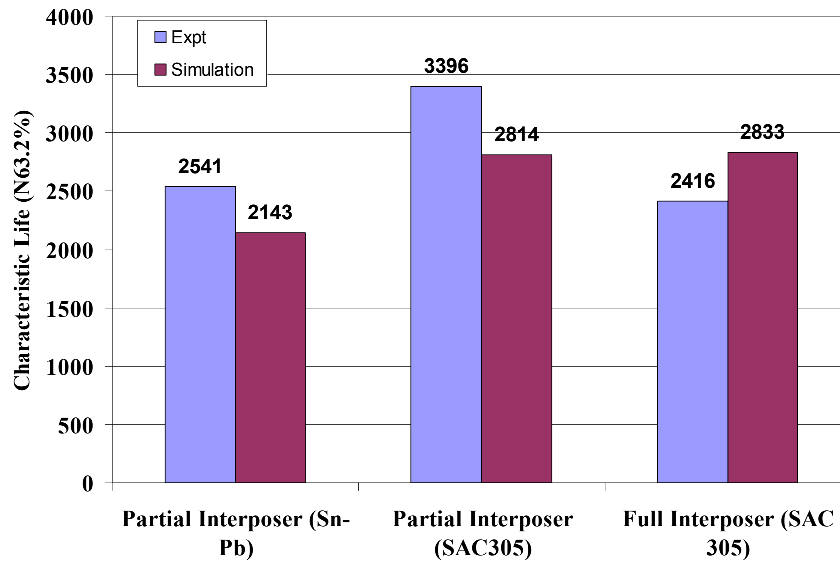


Figure 40: Comparison between life prediction data (based on simulations) with experimental data.

3.11 Failure Analysis:

In order to identify the failure mode, the tested assemblies were cross-sectioned and studied by a Field Emission Scanning Electron Microscope instrument (SEM), JEOL JSM-7000F operated at an accelerating voltage of 20 kV. Most solder joint failures were found on the farthest D-Stick, inline with the finite element model predictions. More solder joint failures were found on the package side than on the board side. The joints on the package side are more like Solder Mask Defined (SMD) while those at the board side are Non-Solder Mask Defined (NSMD). It may be possible to attribute this skewed failure distribution (on the package side) to the fact that NSMD morphology performs better than SMD pads.

In one of the samples, dielectric cracking was also observed. The location of dielectric cracking was also inline with the results predicted from finite element simulations. Representative figures for solder joint failure (package / board side), dielectric cracking, etc for different configurations are shown below.

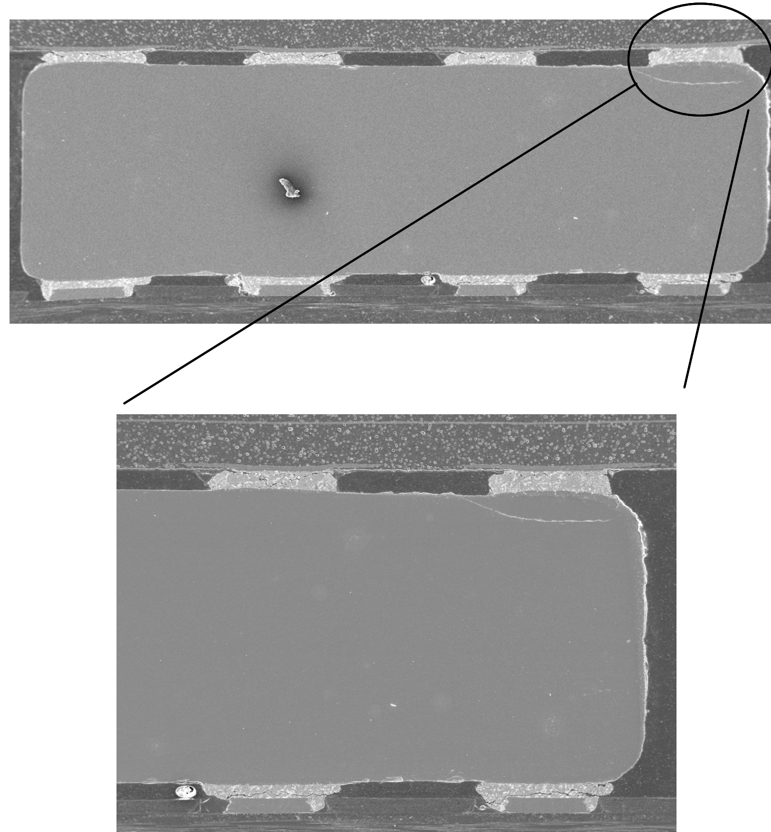


Figure 41: SEM image of failed D-Pack assembly (Partial Interposer with eutectic Sn-Pb solder joints). Dielectric cracking at the package side.

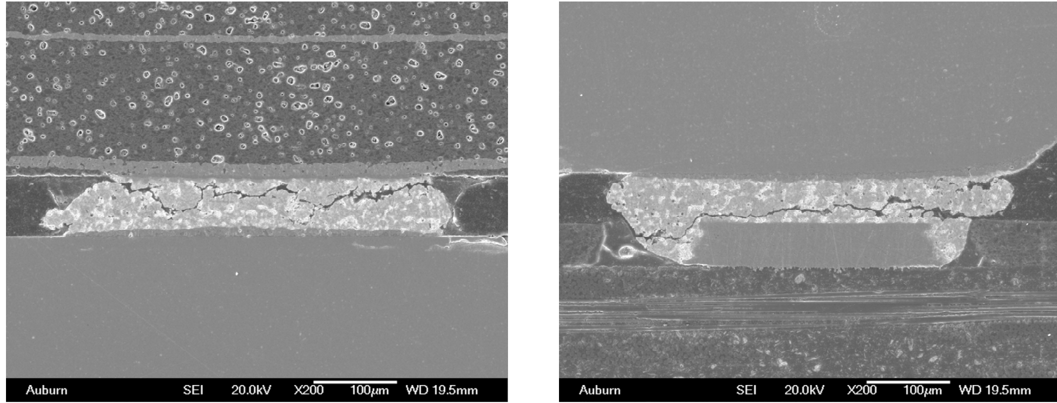


Figure 42: SEM image of failed D-Pack assembly (Partial Interposer with eutectic Sn-Pb solder joints). Solder Joint cracks on package side and board side.

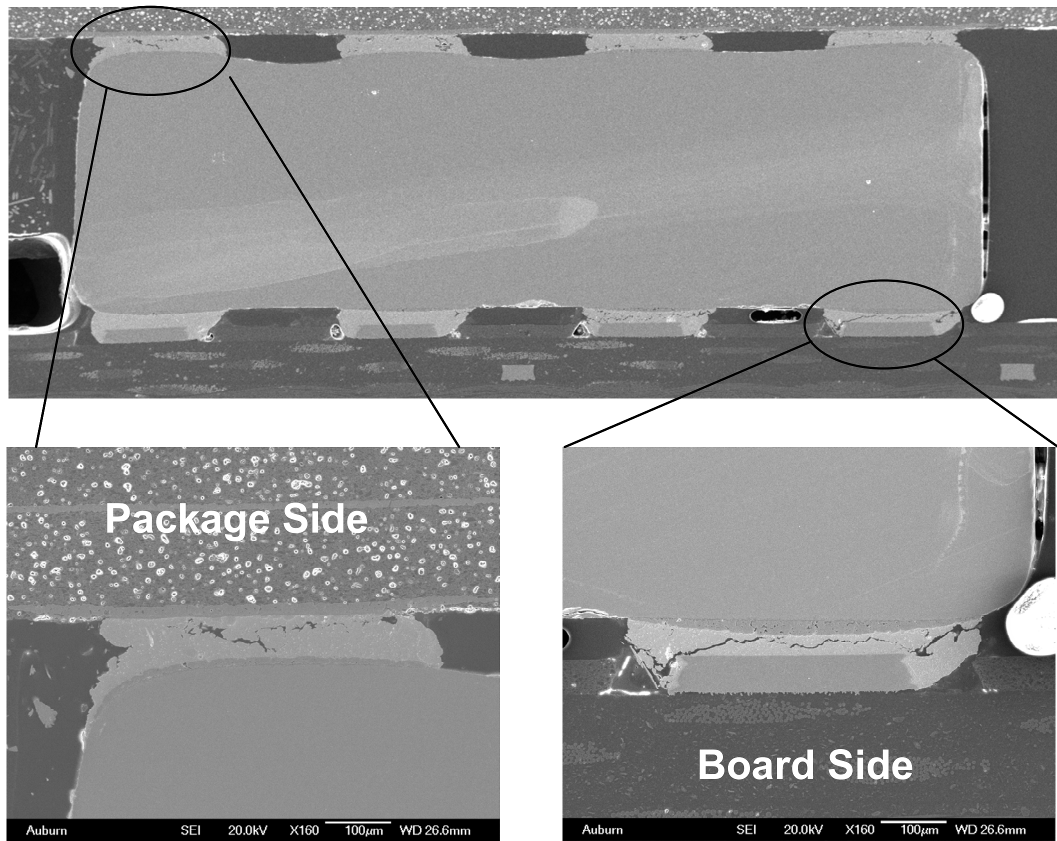
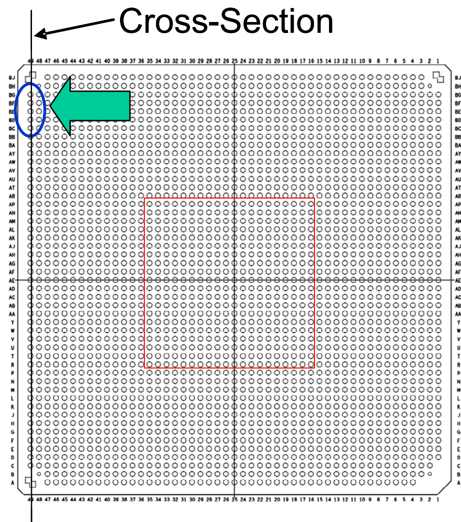


Figure 43: SEM image of failed D-Pack assembly (Partial Interposer with eutectic SAC solder joints). Solder Joint cracks on package side and board side.



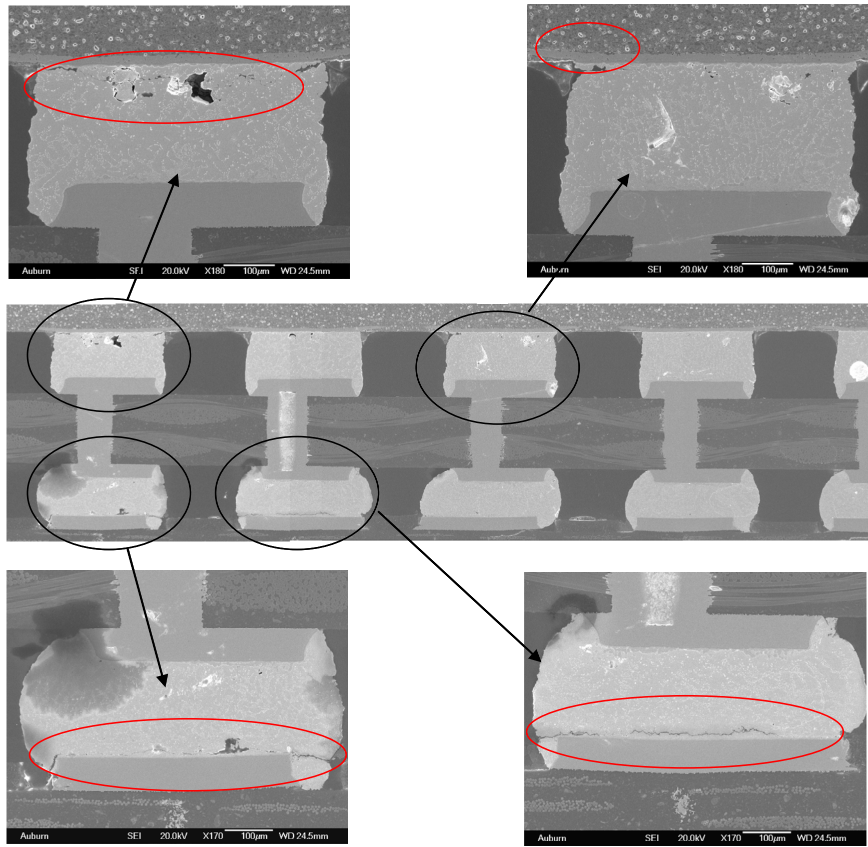


Figure 44: SEM image of failed D-Pack assembly (Full Interposer with SAC solder joints). Outer periphery Solder Joint cracks on top row and bottom row.

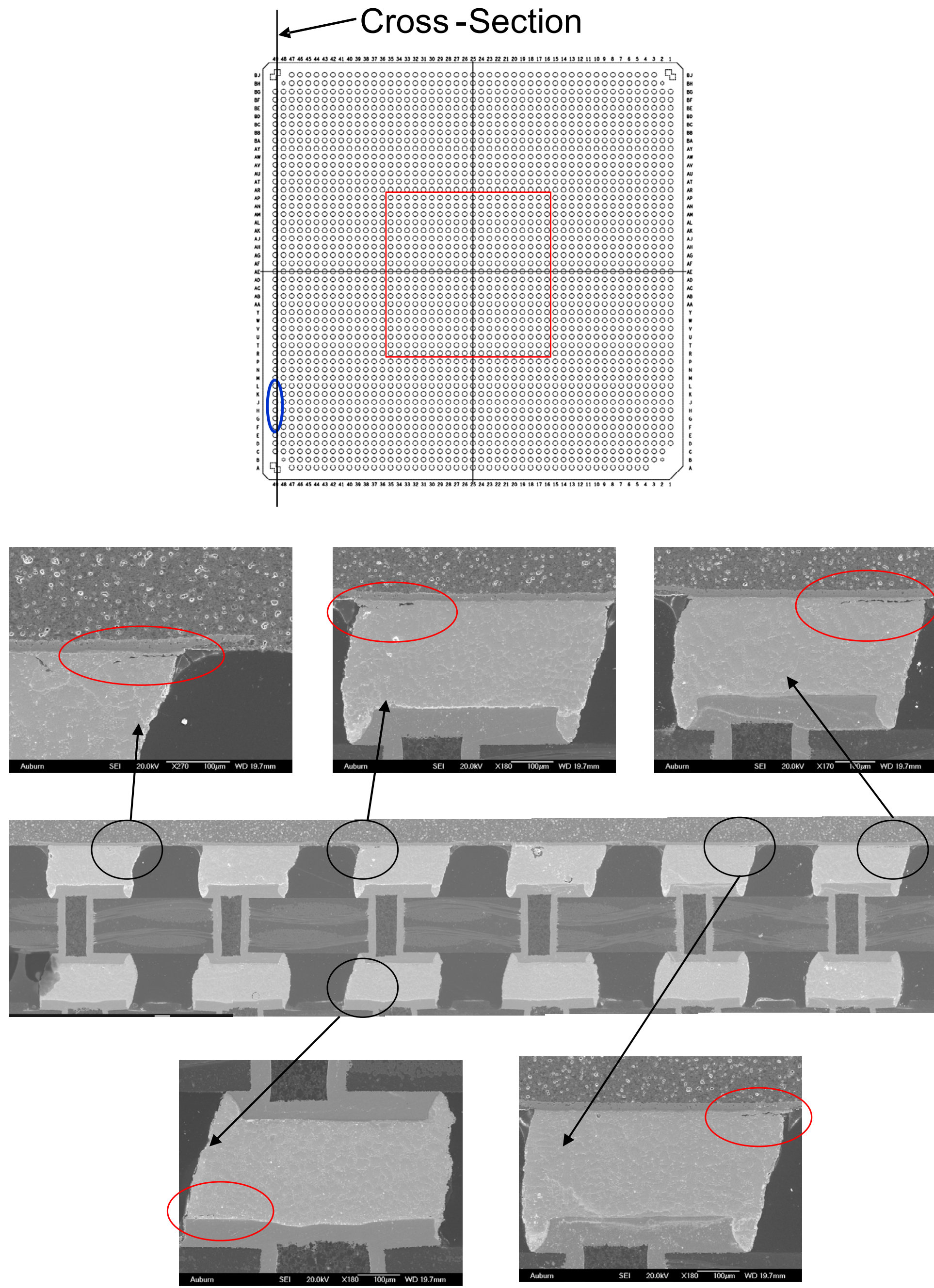


Figure 45: SEM image of failed D-Pack assembly (Full Interposer with SAC solder joints). Outer periphery Solder Joint cracks on top row and bottom row.

3.12 Summary & Conclusion:

The thermo-mechanical reliability of D-Pack has been evaluated using finite element models. Slice models were created for different configurations (Partial Interposer, Full Interposer), solders (eutectic Sn-Pb, SAC) in ANSYS and subjected to two thermal cycles from 0ºC to 100ºC (20 min dwell / ramps). The reliability was assessed from the point of view of fatigue in solder joints as well as capacitor dielectric cracking.

Volumetrically averaged visco-plastic strain energy density (across a layer of critical elements) was used as a metric to calculate the damage in solder joints due to cyclic temperature loading. Based on empirical relations for life prediction available in literature, cycles to failure was calculated using the energy approach and the predictions were compared with experimental data. The predictions based on finite element methodology were in close agreement with the experimental data.

The maximum principal stress generated in the dielectric was also observed during the simulation. Based on the S-N curves available from fatigue testing for $BaTiO_3$ (dielectric in D-Pack), it was concluded that the stresses generated in D-Pack were well within the maximum stress limits.

Also, in order to correlate the failure locations predicted by finite element simulations, the tested (failed) assemblies were cross sectioned and observed under Scanning Electron Microscope (SEM). The solder joint failures and dielectric cracking observed in failed samples were inline with the results shown during the finite element post processing.

CHAPTER 4

PROGNOSTICS HEALTH MANAGEMENT OF SnAgCu SOLDER ELECTRONICS IN HARSH AGING ENVIRONMENTS

There is a growing need to develop and demonstrate technologies that can monitor and predict the remaining service life of key elements including electronics in implantable biological applications [Stanton 2002], automotive applications [Bodensohn 2005], defense [Grietzer 1999], and civil infrastructure applications [Bond 1997]. Health Monitoring (HM) refers to the broad concept of assessing the ongoing, in-service performance of a system using a variety of measurement techniques.

Health Monitoring is aimed at the immediate detection and diagnosis of off-normal system operation, and to take real-time corrective actions to avert the possibility of a system failure. The technical approach here relies on fusion of heterogeneous information derived from physics-based models of fatigue damage and real-time sensor data [Keller 2003]. HM can also provide the Operation and Maintenance (O&M) team with the information necessary to select and follow the optimum asset management path leading to substantial reduction in life cycle cost of the system [Jarrell 2002]. Prognostics refer to interrogation of material state of a system based on computation of certain proxies, stressors, and to predict the Residual Life (RL) of the system for the intended environment.

Pacemakers and implantable cardioverter-defibrillators (ICDs) are among the most critical life-support and complex medical devices in use today. However, several recent high-profile device malfunctions have called into question their safety and reliability. Several database registries including the United Kingdom, Danish and Bilitch Registries have monitored pacemaker and ICD safety performance. In total, hundreds of device malfunctions affecting dozens of pacemaker and ICD models have been reported. A study of pacemaker and ICD advisories, a surrogate marker of device reliability, demonstrated that the number and the rate of pacemakers and ICDs affected by advisory has increased since 1995 [Hauser 2001, Maisel 2001, 2002, Song 1994, Stanton 2002].

Previously, the PHM of mechanical structures has been done by dynamic analysis based on natural frequencies, mode shapes, damping factors, and static analysis based on deformation or changes in structure orientation due to load or unexpected damage, using innovative signal processing, new sensors, and control theory [Kok 2005]. New advances in sensor technology and failure analysis have catalyzed a broadening of application scope for prognostication systems to include large electromechanical systems such as aircraft, helicopters, ships, power plants and many industrial applications. HM application areas include fatigue crack damage in mechanical structures such as those in aircraft [Munns 2000], surface ships [Baldwin 2002], civil infrastructure [Chang 2003], railway structures [Barke 2005] and power plants [Jarrell 2002].

In case of mechanical systems like propulsion systems, compressors, gears, etc damage progresses mainly due to wear (prolonged usage), or imbalance condition in one of the rotating elements, or from misalignment of the shafts of the rotating components which leads to changes in the vibration signature of the equipment. By comparing the

vibration signals from the defective equipment with those from sound equipment, the performance degradation can be characterized [Dyne 1992].

Other examples include, aircraft engines, which start and stop quite frequently and run at high speeds, a model-based method has been used for the on-line identification of cracks in a rotor while it is passing through its flexural critical speed [Sekhar 2003]. Detection of surface corrosion has been used to reduce the maintenance required, and trigger preventive repair for increased aircraft availability and significantly reduced cost of ownership. Fluorescent fiber optic sensors that detect aluminum coating from the early stages of the corrosion process have been used for providing early warning of corrosion in susceptible areas of an aging aircraft [Maalej 2004].

Optical fiber based sensor system has been used on concrete structure to evaluate its performance for health monitoring [Fernando 2003]. Monitoring bridge performance has been done to answer questions on the performance of existing bridges, refine techniques needed to evaluate different bridge components, and develop approaches that can be used to provide a continuous picture of a bridge's structural integrity using structural health monitoring [DeWolf 2002]. Transducers along with a wireless data acquisition system can enable the possibility of achieving long distance monitoring [Kok 2005]. These techniques help in detection of damage of bridges or building to avoid the economic and social effect of aging and deterioration [Chang 2003].

Wayside detection involving fault identification using interrogating sensors placed along the sides of railway tracks has been used in the railway industry for gathering information about vehicle performance. Information on the vehicle condition and performance over an extended period of time is recorded in an online database,

which is interrogated for critical performance parameters to provide information on condition of in-service railway vehicles [Barke 2005]. In other applications, signal feature analysis is used to detect abnormalities related to impending failure indication by an inference system using an historical database [Hess 2001, 2002].

Wear and degradation in electronics is very difficult to detect and inspect compared to most other mechanical systems and structures due to complex and tiny structure. Health management of electronic systems requires knowledge of impending failure. Presently, acquisition of mechanical system-diagnostics has been successfully achieved for automotive applications through an elaborate system of fault codes. The state-of-art health management systems focus on detection and isolation of faults and failures, and are largely reactive in nature, limiting the scope of maintenance decisions.

Built- In-Self Test (BIST) circuit, which includes onboard hardware and software diagnostic, has been used for error detection and fault location [Drees 2004]. BIST is a methodology that embeds additional functionality in the product to give it the ability to test and diagnose itself with minimal interaction from external test equipment [Chandramouli 1996, Hassan 1992, Williams 1983, Zorian 1994]. BIST controllers are typically used for reactive failure detection, to output failure data that can be correlated to show exactly when the failure occurred. This data can then be interpreted by diagnostic software to analyze the cause of failure. For example, Pseudo-Random Binary-Sequence (PRBS) test pattern generators, apply input vectors to digital or analog [Al-Qutayri 1992] modules. Self-Checking circuit designs provide on-line test for digital [Lala 1985] as well as for analog circuits [Kolarik 1993]. The obtained output is then compared with a "golden response".

The results obtained from BIST functions can generate diagnostic information which in turn provides additional confidence in the measurement result and confirm the device availability. BIST helps in minimizing the interaction with external automated test equipment (ATE) as well as provides the advantage of a more robust "at-speed" test of the circuitry; however, the current form gives little insight about the system level reliability or the remaining useful life of the system. Several studies conducted [Allen 2003, Drees 2004, Gao 2002, Rosenthal 1990] have shown that BIST can be prone to false alarms and can result in unnecessary costly replacement, re-qualification, delayed shipping, and loss of system availability.

Fuses and Canaries have been used to provide advance warning of failure in electronics due to specific wear out failure mechanism [Vichare 2006]. Fuses within circuits and thermostats, can be used to sense the abnormal conditions like voltage transients, critical temperature limit and to make adjustment to restore normal condition [Ramakrishnan 2000]. Canary devices like pre-calibrated cells which are located with the actual circuitry on the same chip experience similar stresses as the actual component, this leads to same damage mechanism. The cells are designed to fail faster by scaling the stress which is been experienced to avoid the catastrophic failure of actual component. The failure of the canary devices can be used to estimate the time to failure of actual product [Mishra 2002]. Similarly canary components created on printed circuit board is been used for prognostication by failing before the actual component [Anderson 2004]. However, replacement of fuses and canaries impacts the maintenance, repair and part replacement making it difficult to integrate these systems with host system. In addition, fuses provide limited insight into the remaining use life prior to fuse-failure.

The reliability of electronic control and safety systems in harsh environment applications, such as automotive safety systems, can be significantly impacted through development of methodologies for monitoring the degradation and understanding damage evolution to enable avoidance of system-level failures. Challenges in implementing prognostics can be attributed to the lack of understanding of the underlying component degradation mechanisms.

An electronic component operating in a harsh environment is subjected to both temperature variations as well aging for a finite duration during use-life. Therefore, a time-temperature history of the electronic system ambient would be extremely helpful in using life prediction models and computing life. Continuous capture of time-temperature history would put immense demands on existing system function. Reconstruction of operational profiles is often challenging and future operational profiles often unpredictable. In addition, it may not be always possible to characterize the operational loads under all possible scenarios (assuming they are known and can be simulated). Damage pre-cursors target fundamental understanding of underlying degradations in electronic systems, such a thermo-mechanical interconnect-fatigue, interfacial delamination of underfills, etc. Once identified for specific package elements and failure mechanisms, the pre-cursors are scalable for future package architectures and for application across a broad spectrum of designs.

In this study, a mathematical approach has been presented to calculate the prior damage in electronics subjected to isothermal thermo-mechanical loads. PHM approach presented in this paper is different from state-of-art diagnostics and resides in the prefailure-space of the electronic-system, in which no macro-indicators such as cracks or

delamination exist. The presented PHM methodologies enable the estimation of prior damage in deployed electronics by interrogation of the system state.

In this study, investigation of the changes of the features as well as time-evolution of physical damage, and the relationship between physical damage and feature-set has been established for thermo-mechanical stresses. Comprehensive heath monitoring framework proposed here will facilitate quick assessment of system state and potential for failure of critical electronic systems. A methodology for pre-cursors based computation of residual life of electronic systems has been presented. A damage pre-cursors based residual life computation approach for various package elements has been developed, to prognosticate electronic systems prior to appearance of any macro-indicators of damage (Figure 46).

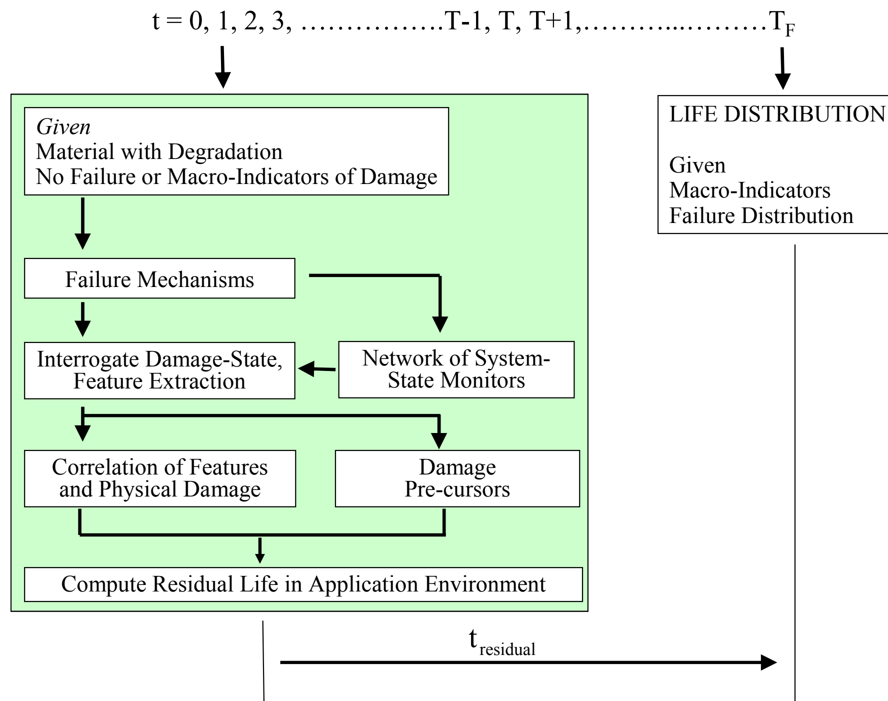


Figure 46: Damage Pre-Cursors Based Methodology for Prognostication of Electronic Systems.

In order to implement the system-health monitoring system, precursor variables or leading indicators-of-failure have been identified for various package elements and failure mechanisms. Model-algorithms have been developed to correlate precursors with impending failure for computation of residual life. The correlations serve a basis for interrogation of damage-state and extraction of features quantifying underlying degradation. Examples of damage pre-cursors include phase-growth, intermetallic thickness, and patterns in interfacial stress distributions. Change in damage pre-cursors are sensed through a network of system-state monitors. Mathematical relationships have been developed for computation of residual life based in terms of damage proxies.

The pre-cursor based damage computation approach eliminates the need for knowledge of prior operational stresses and enables health management of deployed non-pristine electronic systems under unknown prior-loading conditions. The approach is powerful, since it reduces the demands on electronic system field-usage and deployment logistics required for acquisition of prior stress histories. Use of pre-cursors for damage computation addresses the limitation of life-prediction model based prognostication techniques, which target damage estimation for known stress histories imposed on pristine materials. Examples of life prediction models include Paris's Power Law [Paris, et. al 1960 1961], Coffin-Manson Relationship [Coffin 1954; Tavernelli, et. al. 1959; Smith, et. al. 1963; Manson, et. al. 1964] and the S-N Diagram.

4.1 Test Vehicle

Area-array packages with 95.5Sn4.0Ag0.5Cu solder balls assembled on FR4-06 laminates and immersion Ag finish have been studied under isothermal aging at 125°C.

Phase growth data has been gathered and analyzed using image processing. Components analyzed include various packaging architectures including, plastic ball-grid arrays, chip-array ball-grid arrays, tape-array ball-grid arrays, flex-substrate ball-grid arrays, and discrete resistors. Ball counts are in the range of 64 to 676 I/O, pitch sizes are in the range of 0.5 mm to 1mm, and package sizes are in the range of 6mm to 27mm (Table 7). The boards contain six trace layers to simulate the thermal mass of a true production board, though all functional traces were run on the topmost layer.

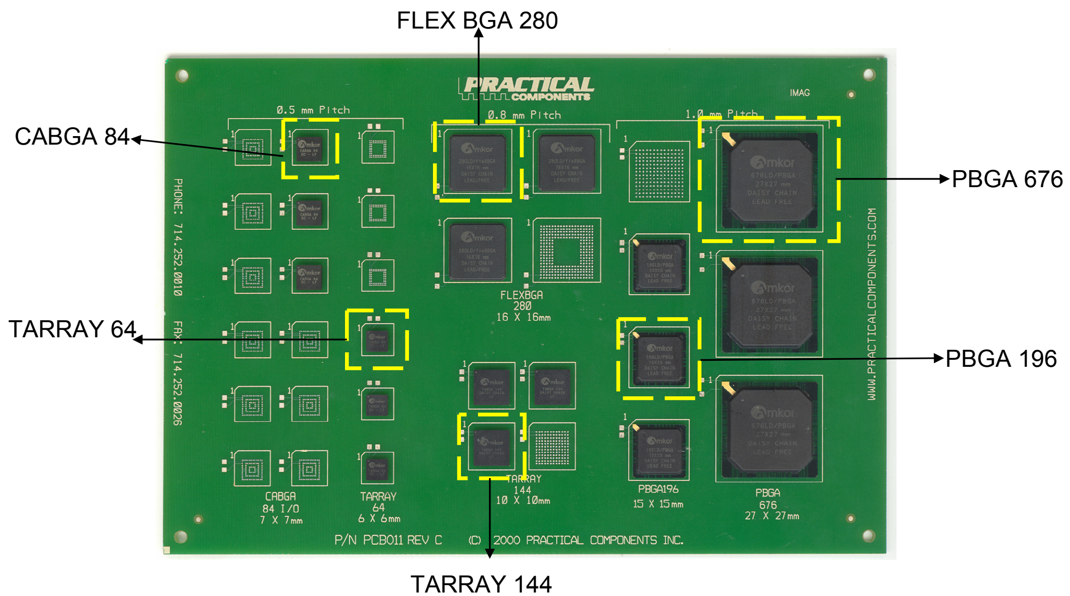


Figure 47: Test Vehicle

Table 7: Experimental Design

Body Size	Package Type	Ball Count	Ball Pitch (mm)	Die Thickness (mm)	Die Size (mm)	BT Thickness (mm)	BT Pad Type	Ball Diameter (mm)
6 mm	TABGA	64	0.5	0.36	4	0.36	NSMD	0.32
7 mm	CABGA	84	0.5	0.36	5.4	0.36	NSMD	0.48
10 mm	TABGA	144	0.8	0.36	7	0.36	NSMD	0.48
15 mm	PBGA	196	1	0.36	6.35	0.36	SMD	0.5
16 mm	FlexBGA	280	0.8	0.36	10	0.36	NSMD	0.48
27 mm	PBGA	676	1	0.36	6.35	0.36	SMD	0.63

Phase growth and intermetallic-growth under steady-state temperature have been identified as pre-cursors for understanding progression of damage in this study. Evolution of solder microstructure and the growth of intermetallic due to thermal fatigue have been reported previously by several researchers.

4.2 Damage Proxies: Lead-Free Solder Grain Coarsening

Electronics deployed in underhood automotive applications is subjected to temperature variations in the neighborhood of -40°C to 125°C. These temperature excursions during operation of a circuit are due to both power-cycling and variations in ambient conditions resulting in thermo-mechanical cyclic stresses and strains induced primarily by thermal expansion mismatch between the package and the board assembly. Micro-structural coarsening during thermo-mechanical deformation is attributed to the generation of excess vacancies caused by the combined effect of local hydrostatic state of stress, and the instantaneous inelastic strain rate [Dutta 2003[a], 2003[b], 2004; Jung 2001].

Previous researchers have examined changes in microstructure occurring in the Sn63/Pb37 and lead-free chip resistor solder joints during thermal cycling [Sayama, et al. 1999, 2003], investigated the grain-size evolution and derivatives of phase growth rate as prognostics parameters on a wide range of leaded devices in underhood applications [Lall, et. al. 2004[b]], correlated thermal fatigue with occurrence of microstructural coarsening in the fatigue damaged region in of 63Sn37Pb solder interconnects [Frear, et. al. 1990, Morris, et al. 1991]. Correlation of grain coarsening with thermal fatigue has also been established for high-lead solders [Bangs, et. al. 1978, Wolverton 1987, Tribula, et. al. 1989]. In this study, prognostics health management methodology has been presented to assess the prior damage is based on solder grain coarsening model. Phase growth under thermal aging has been identified as the damage precursor to compute the residual life.

In this study, changes in solder microstructure and its derivatives have been investigated for use as the leading indicators of failure and interrogation of system state for assessment of damage from prior stress histories. Quantitative metrics of changes in microstructure have been identified and relationships developed to represent damage progression. Data presented covers a wide range of Sn4Ag0.5Cu lead-free packaging architectures and discrete devices in extreme steady-state temperature environments.

The phase growth parameter has been defined as the relative change from phase-state after reflow, instead of the absolute value of phase state. Figure 48 shows Ag_3Sn Grains in 95.5Sn4Ag0.5Cu microstructure. The fundamental reason for selection of phase growth and its derivatives is that, superplastic alloys are usually made of fine grain structure. Therefore a considerable growth of the matrix grains and the second phase

particles frequently occurs during high temperature deformation. The grain growth rate (per unit time) is found to increase with increasing strain rate.

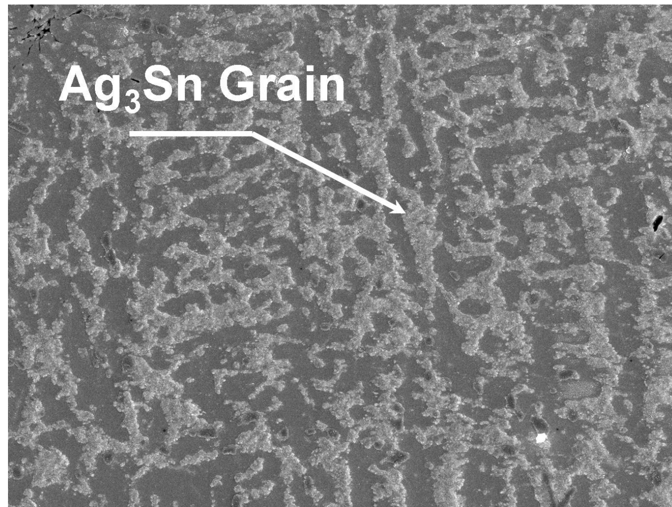


Figure 48: Ag_3Sn Grains in 95.5Sn4.0Ag0.5Cu solder microstructure

Callister [1985] states that for many polycrystalline materials phase size varies with time according to the following relations.

$$g^n - g_0^n = Kt \qquad (1)$$

Where g is the phase size at time t, and g_0 is the initial phase size, and K and n are time independent constants. The value n is generally varies between 2 to 5. The process of the particle growth induced by volume diffusion was theoretically analyzed by Lifshitz, et al. [1961]. It was revealed that the variation of the average particle radius with time is

$$r^3 - r_0^3 = B_1 \frac{\gamma \Omega C_0 D_b}{RT} t \qquad (2)$$

where r is the average particle radius, r_0 is the initial radius of an average particle, B_1 is the parameter related to the volume fraction of the particles, γ is the free energy per unit area of the phase boundary, Ω is the molar volume of the particle phase, C_0 is equilibrium

solute concentration near the phase boundary. D_b is the coefficient of solute diffusion in the phase boundary. R is the gas constant, T is the absolute temperature, and t is time.

Senkov and Myshlev [1986] applied the theory the phase growth process of a superplastic alloy and validated the theory in that of Zn/Al eutectic alloy. They expressed the evolution of the average phase size g with the time as shown below,

$$g^4 - g_0^4 = \frac{B\delta\Omega C_0 D_b}{RT} t \quad (3)$$

Where g_0 is the initial average phase size, B is the phase geometry parameter, δ is the phase boundary width. Dutta [2003[a], 2003[b], 2004] represented the total vacancy concentration at any location within the solder joint at any instant of 't' may be written as the sum of the equilibrium vacancy concentration, and vacancy concentration under applied instantaneous strain rate,

$$n_{total} = n_{eqlm} + n_{strn} \quad (4)$$

$$n_{eqlm} = \exp\left(\frac{-Q_{f,v}}{kT}\right)\exp\left(\frac{\sigma_h \Omega}{kT}\right) \quad (5)$$

$$n_{strn} = \exp\left(\frac{-Q_{f,v}}{kT}\right)\exp\left(\frac{\sigma_h \Omega}{kT}\right) N\dot{\varepsilon}\left[1 - \exp\left(\frac{-t}{\tau_c}\right)\right] \quad (6)$$

Here, $Q_{f,v}$ is the enthalpy of formation of a vacancy, Ω is the molar volume, τ_c is a time constant associated with the decay of a vacancy following formation, and N is a constant that scales the vacancy concentration to $\dot{\varepsilon}$.

Based on Lifshitz-Wagner theory, and assuming a linear time dependence of temperature $(T = T_{min} + \beta t)$ during thermal cycle, Dutta [2003[a], 2003[b], 2004] showed that the final particle size, at any time $r(t)$ can be expressed as,

$$r(t) \approx \left\{ \left[\left(\frac{B_1 \gamma_s V_m C_0}{RT} \right) \overline{D}_{sol} (t + 2N\hat{\gamma} t_{hc} \nu_c \phi) + r_0^3 \right]^{1/3} \right\} \qquad (7)$$

Where,

$$\overline{D}_{sol} = \frac{\int_0^{t_{hc}} D_0^{sol} \exp\left[\left(\frac{\sigma_h \Omega}{k} - \frac{Q_{sol}}{R} \right) \frac{1}{T} \right] dt}{\int_0^{t_{hc}} dt} \qquad (8)$$

and, D_{sol} is the effective solute diffusivity in the matrix, D^0_{sol} and Q_{sol} are the associated frequency factor and activation energy, $\hat{\gamma}$ is the average shear-strain rate during a half cycle, and can be approximated as $\hat{\gamma} \approx \frac{\Delta\alpha (T_{max} - T_{min})}{h t_{hc}}$, where $(T_{max} - T_{min})$ is the temperature range of the cycle, ν_c is the number of thermal cycles, each with a half period of t_{hc}.

In the Equation (7), when $\hat{\gamma} = 0$, value of phase-radius, r, represents the coarsened size caused by isothermal aging only. For $\hat{\gamma} \neq 0$, the value of phase-radius, r, includes contributions caused by both static aging and strain-enhanced (thermal cycling) coarsening.

Samples were subjected to single-stresses of steady-state temperature at 125°C. The stresses were increased gradually in magnitude. The samples were cross-sectioned at various level of stress and exposure length. The cross-sections were studied by a Field Emission Scanning Electron Microscope instrument (SEM), JEOL JSM-7000F operated at an accelerating voltage of 20 kV. The pictures were taken at magnification of 750x. All samples were imaged after polishing and etching to reveal grain structure. The quantitative measure of Ag_3Sn particle size was established from a 60μm x 45μm rectangular region selected from a backscattered SEM image of a highest strain corner

solder ball. The location of the examination region was identical for various samples. Grain size was averaged from various samples for each package architecture and stress exposure. The typical SEM pictures before and after the mapping of phase size using image analysis are shown in Figure 49 and Figure 50.

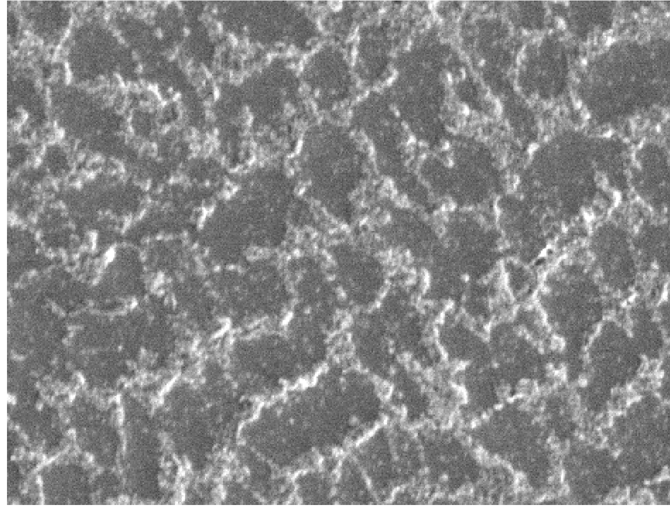


Figure 49: Micrograph from 7 mm BGA showing Tin and Ag_3Sn Phases

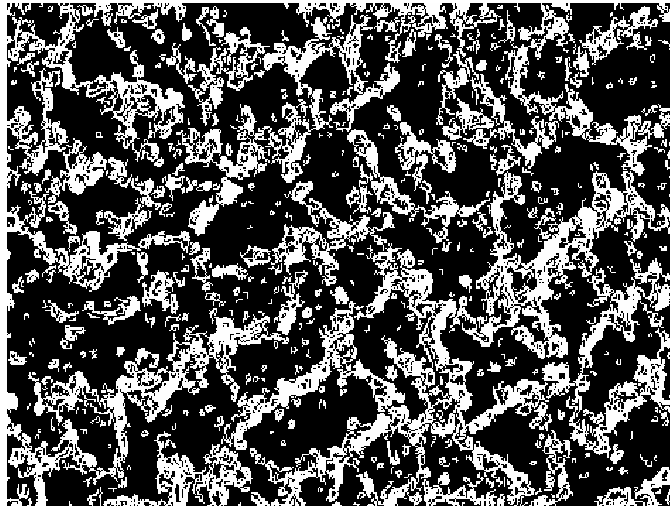


Figure 50: Microstructure mapping using Image Analysis

Error! Reference source not found. Figure 51 to Figure 57 shows SEM backscattered images exhibiting an example of Ag_3Sn phase growth process in different BGA packages during thermal aging test condition.

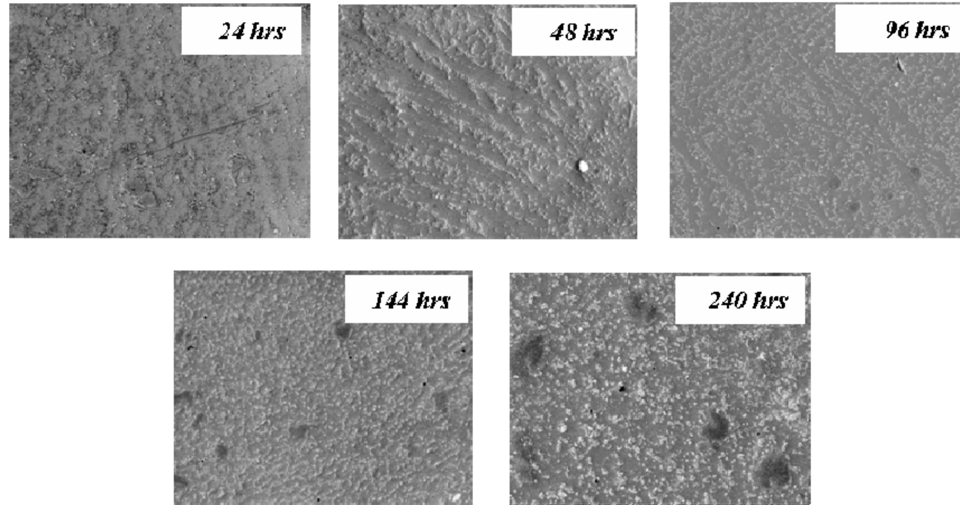


Figure 51: SEM Back-scattered Images of Phase Growth versus Thermal Aging (125°C, 95.5Sn4Ag0.5Cu solder, 16 mm BGA, Magnification: 750x)

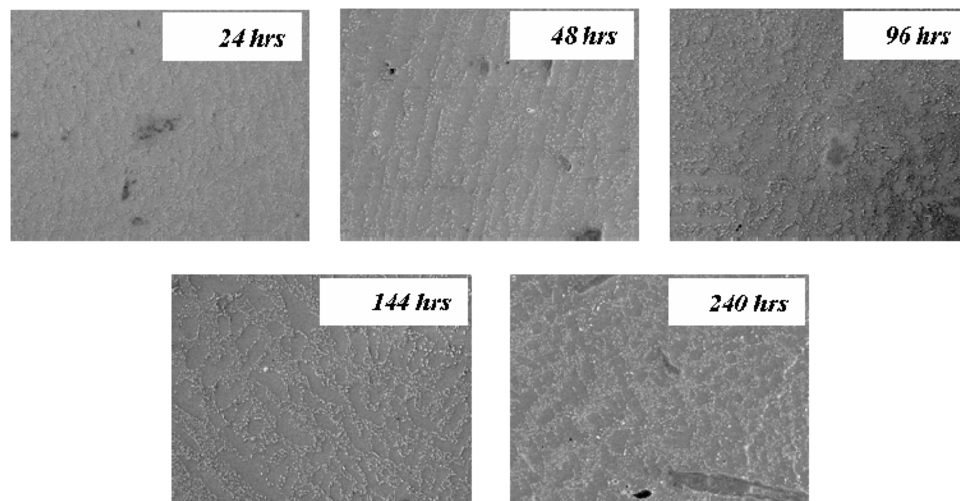


Figure 52: SEM Back-scattered Images of Phase Growth versus Thermal Aging (125°C, 95.5Sn4Ag0.5Cu solder, 27 mm BGA, Magnification: 750x)

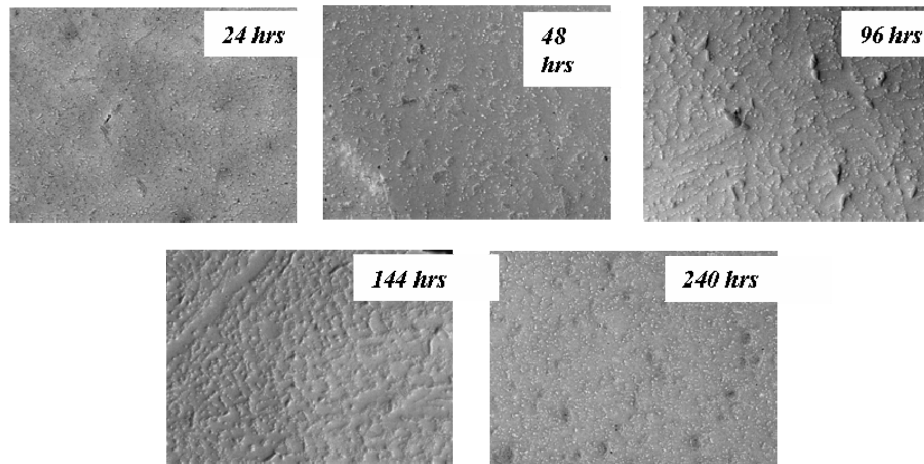


Figure 53: SEM Back-scattered Images of Phase Growth versus Thermal Aging (125°C, 95.5Sn4Ag0.5Cu solder, 15 mm BGA, Magnification: 750x)

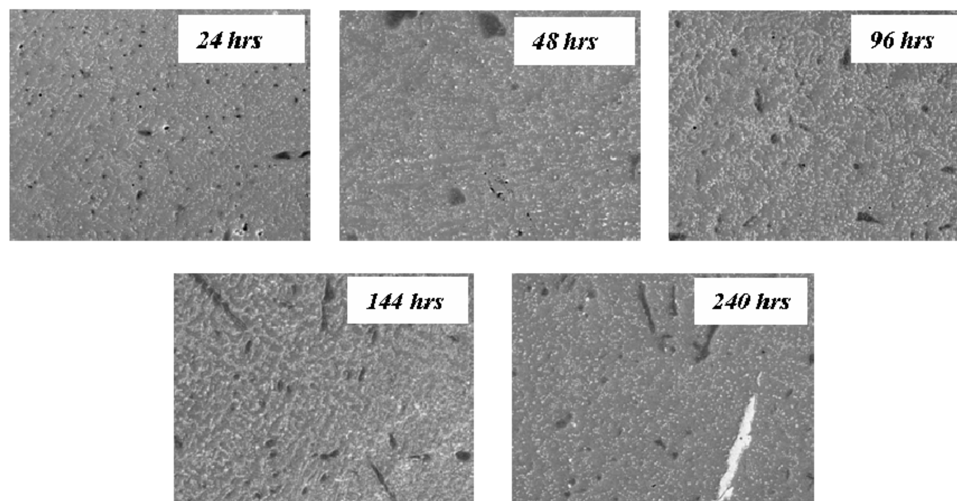


Figure 54: SEM Back-scattered Images of Phase Growth versus Thermal Aging (125°C, 95.5Sn4Ag0.5Cu solder, 15 mm BGA, Magnification: 750x)

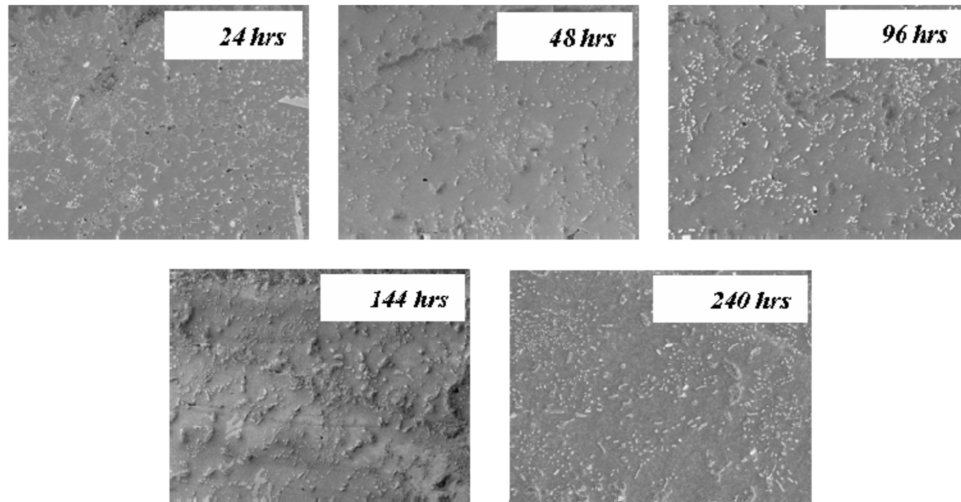


Figure 55: SEM Back-scattered Images of Phase Growth versus Thermal Aging (125°C, 95.5Sn4Ag0.5Cu solder, 10 mm BGA, Magnification: 750x)

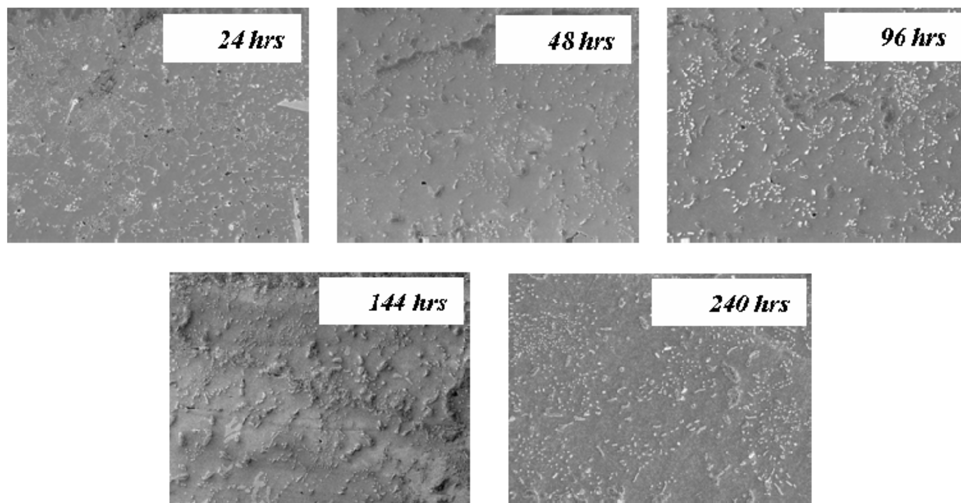


Figure 56: SEM Back-scattered Images of Phase Growth versus Thermal Aging (125°C, 95.5Sn4Ag0.5Cu solder, 7 mm BGA, Magnification: 750x)

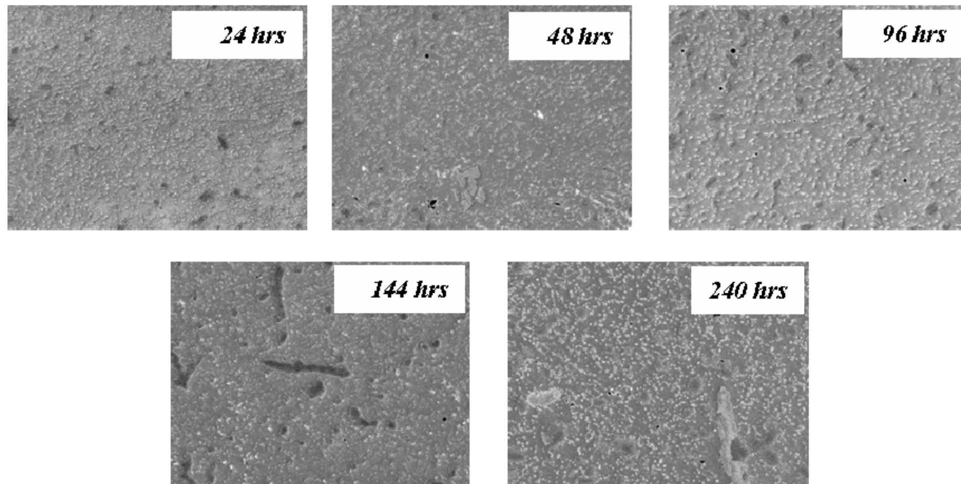


Figure 57: SEM Back-scattered Images of Phase Growth versus Thermal Aging (125°C, 95.5Sn4Ag0.5Cu solder, 6 mm BGA, Magnification: 750x)

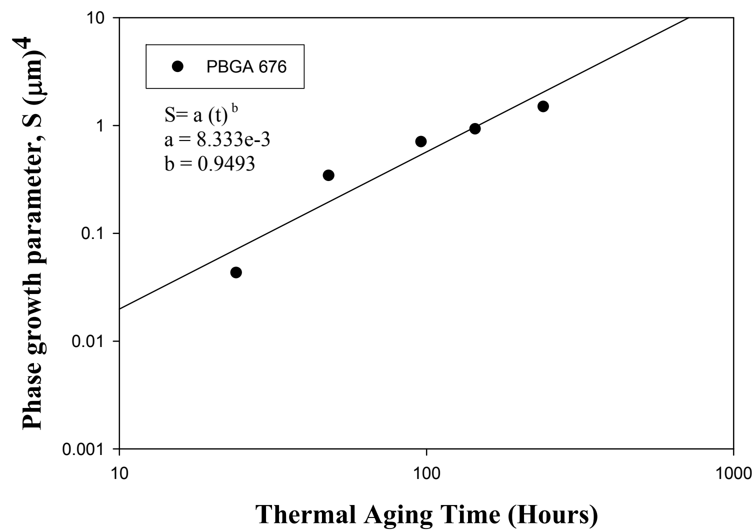


Figure 58: Phase Growth Parameter versus Aging Time at 125°C for PBGA 676 SnAgCu Alloy Solder Interconnects.

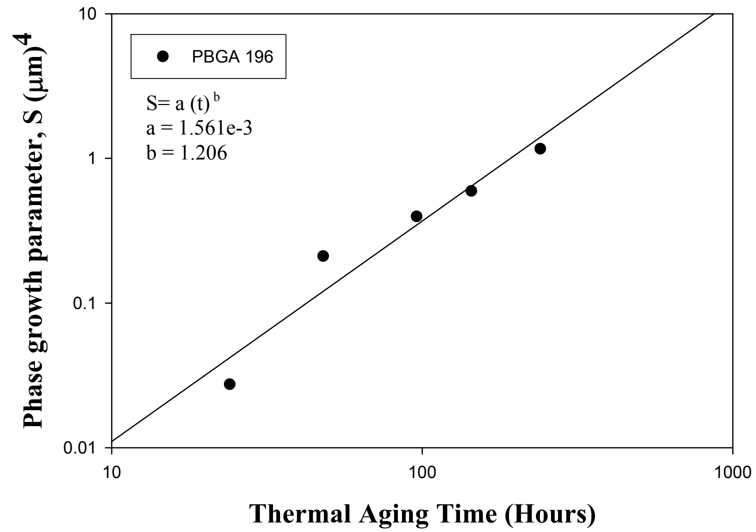


Figure 59: Phase Growth Parameter versus Aging Time at 125°C for PBGA 196 SnAgCu Alloy Solder Interconnects.

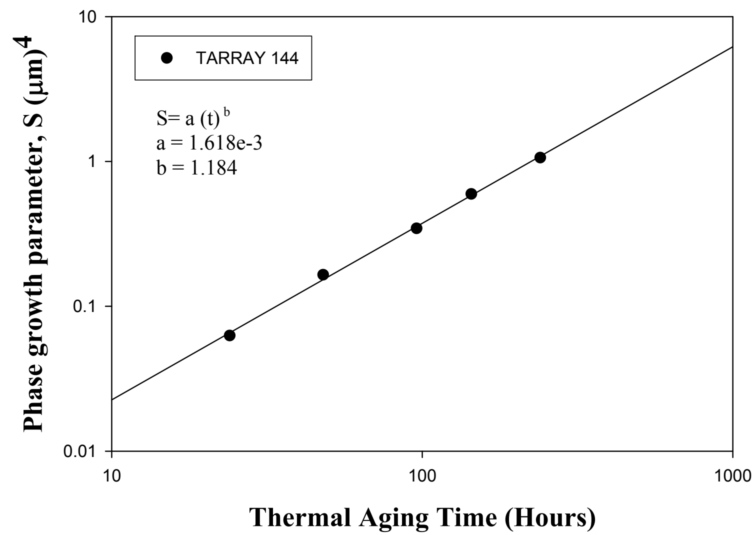


Figure 60: Phase Growth Parameter versus Aging Time at 125°C for TAPE ARRAY 144 SnAgCu Alloy Solder Interconnects.

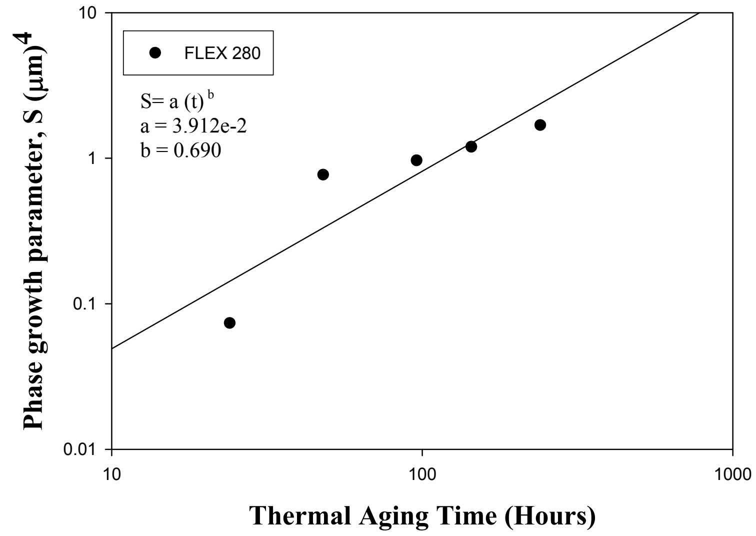


Figure 61: Phase Growth Parameter versus Aging Time at 125°C for FLEX 280 SnAgCu Alloy Solder Interconnects.

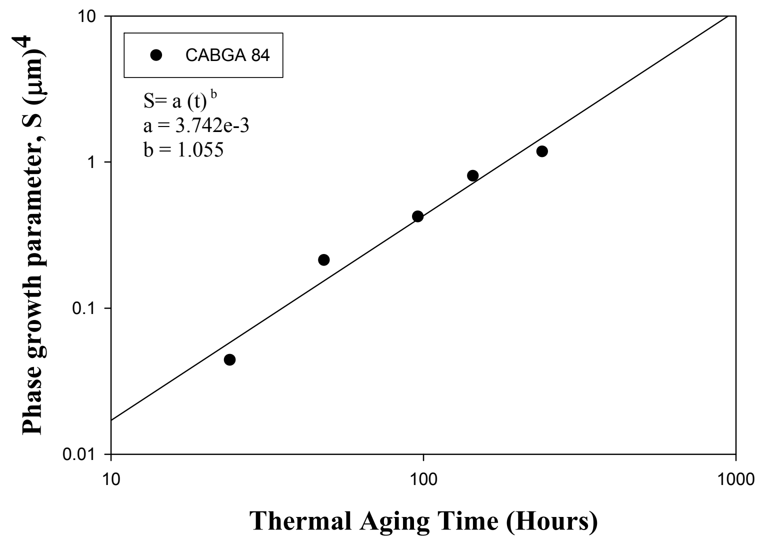


Figure 62: Phase Growth Parameter versus Aging Time at 125°C for CABGA 84 SnAgCu Alloy Solder Interconnects.

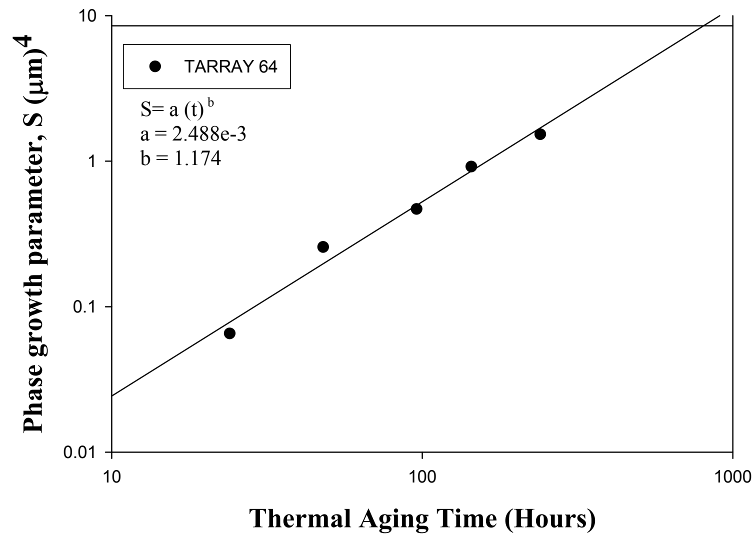


Figure 63: Phase Growth Parameter versus Aging Time at 125°C for TAPE ARRAY 64 SnAgCu Alloy Solder Interconnects.

From this graphs we have found that phase growth rate varies for different components. Figure 58 to Figure 63 shows a comparative study of phase growth rate between various packaging architectures with 95.5Sn4Ag0.5Cu alloys. A correlation between phase growth rate and time can be used as a proxy parameter and evaluation of time at temperature for a deployed part.

4.3 Damage Proxies: Intermetallic Coarsening

Solder joint formation involves wetting and bonding interactions between the solder alloy and the substrate metal. In most cases this interaction manifests itself as reaction between the tin phase and the substrate metal to produce inter-metallic compound (IMC) layers. These are hard, brittle, stoichiometric, metal-metal compounds with high melting points. [Mackay & Levine 1986]. For copper and tin-lead eutectic solder alloy, two such compounds are formed, resulting in a duplex layer consisting of

Cu_3Sn at the copper interface and Cu_6Sn_5 at the tin interface [Unsworth 1976, Kay 1973, --- 1979].

Solid-state IMC layer growth has been investigated for several Sn-containing solders on Cu including the following couples: 63Sn-37Pb/Cu (wt.%), 100Sn/Cu, 96.5Sn-3.5Ag/Cu, 95.5Sn-0.5Ag-4.0Cu/Cu, 95Sn-5Sb/Cu, 91.84Sn-3.33Ag-4.83Bi/Cu, and 58Bi-42Sn/Cu [Vianco 1994[a], 1994[b], 1995, 1999, 2001, 2004 Pang et. al 2001, Tu 1997, Harris 1998, Gupta 2004]. These cited studies and various other researchers have documented the composition and growth kinetics of the IMC layers that develop at the solder/Cu interface.

In this portion of the study, the growth of the intermetallic thickness during thermal aging as leading indicator of failure has been explored. In order to investigate the correlation of interfacial intermetallic thickness growth versus thermal aging, the component has been cross sectioned at various interval of thermal aging. The aged components are sliced periodically to measure the thickness in SEM using 1000x magnification. The mean thickness of IMC layers are measured using commercial image processing software on SEM images. An energy dispersive X-ray (EDX) has been used to examine the morphology and the composition of the intermetallic compound layer at the copper/solder interface. Colloidal silica solution has been applied for the detailed intermetallic compound composition observation and detection.

The interfacial intermetallic layers are formed between solder and copper, and some precipitates appeared near the interface of the IMCs/solder. The intermetallic layers were identified in SEM micrograph and the morphologies are identified by EDX as Cu_3Sn and Cu_6Sn_5 phases. The compositions of the IMC layer are identified as Cu_6Sn_5

for the layer near the Solder Interconnect, and Cu_3Sn, for the layer near the Copper Pad. With the increasing aging time, the IMC layers thicken, and the local irregularities appear to gradually smooth out. Figure 64 shows SEM backscattered images exhibiting an example of intermetallic growth process in the 17 mm BGA solder ball during the thermal aging test condition.

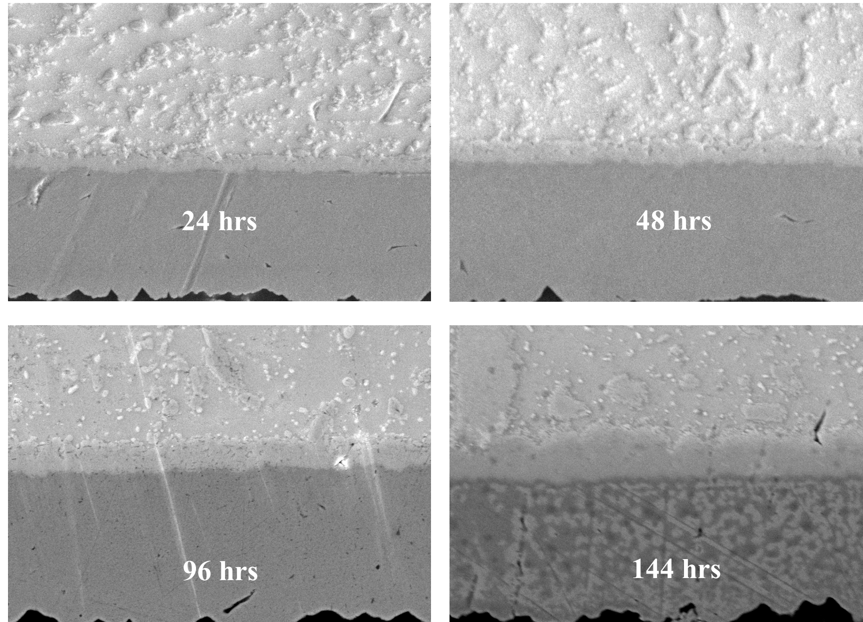


Figure 64: SEM Back-scattered images of IMC Growth versus Thermal Aging for Sn4Ag0.5Cu (Magnification 1000x)

Trend analysis of intermetallic thickness growth on SEM using image processing software, indicates a square root dependence of IMC thickness versus aging time,

$$y = y_0 + kt^n \qquad (9)$$

where $y(t)$ is IMC growth thickness during aging, y_0 is the initial thickness of intermetallic compounds, k is the coefficient standing for the square root of the diffusivity at aging temperature, and t is test time. The exponent value, n = ½ has

been used in Equation (9) above, which reveals a diffusion-controlled mechanism during aging. The IMC growth data in this study indicates that growth rate stays fairly uniform during the thermal aging. It is observed that for both Sn-Ag solder systems, the intermetallic compound thickens roughly as $t^{1/2}$ in a linear manner, where t is the aging time as expected for diffusion-controlled growth.

The average IMC growth measured at each level of test time for each component set cross-sectioned has been shown in Figure 65 to Figure 70.

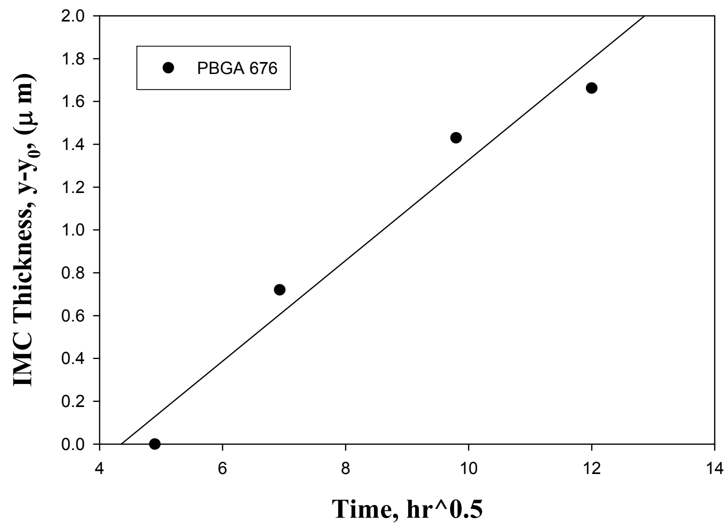


Figure 65: IMC Growth, at Various Levels of time for PBGA 676 with 95.5Sn4Ag0.5Cu Alloy.

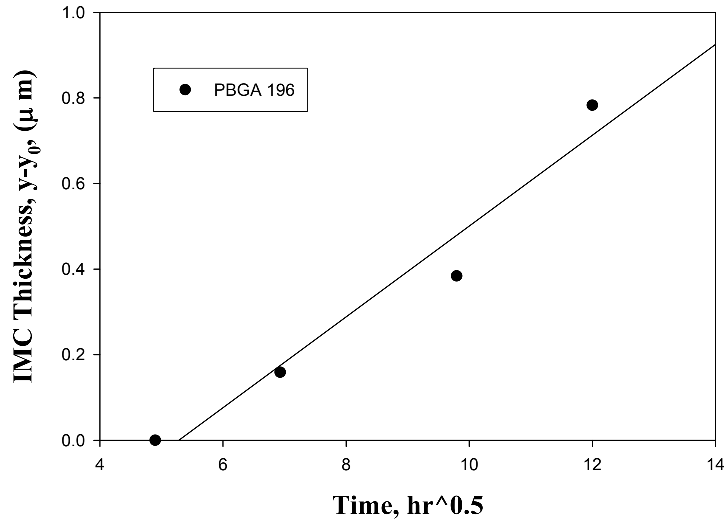


Figure 66: IMC Growth, at Various Levels of time for PBGA 196 with 95.5Sn4Ag0.5Cu Alloy.

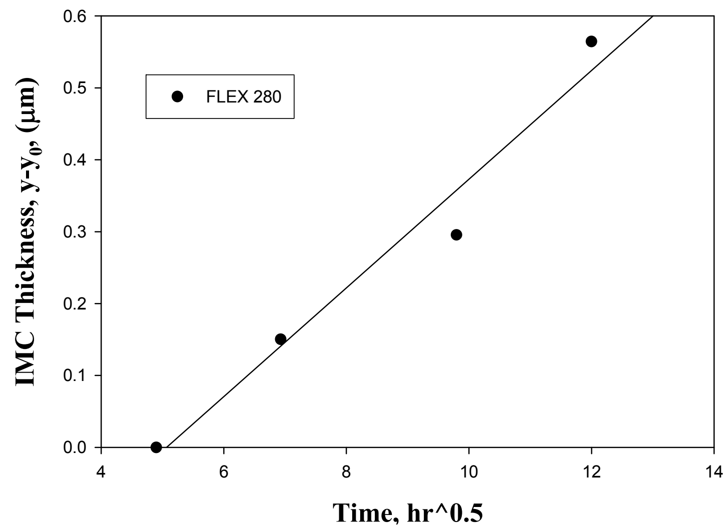


Figure 67: IMC Growth, at Various Levels of time for FLEX 280 with 95.5Sn4Ag0.5Cu Alloy.

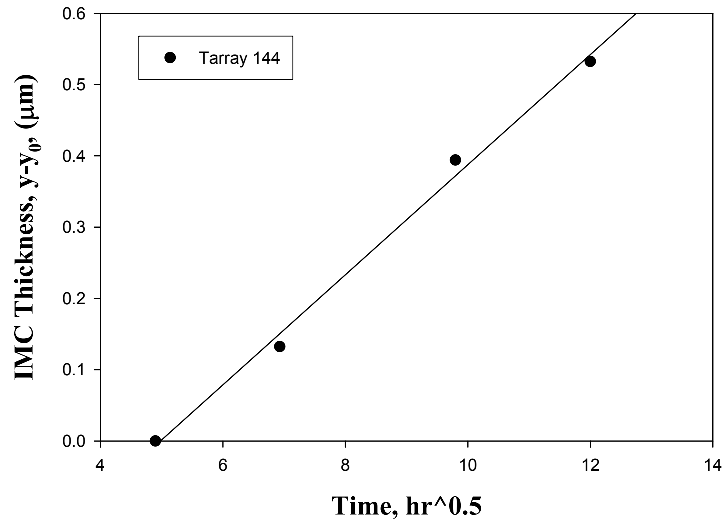


Figure 68: IMC Growth, at Various Levels of time for TAPE ARRAY 144 with 95.5Sn4Ag0.5Cu Alloy.

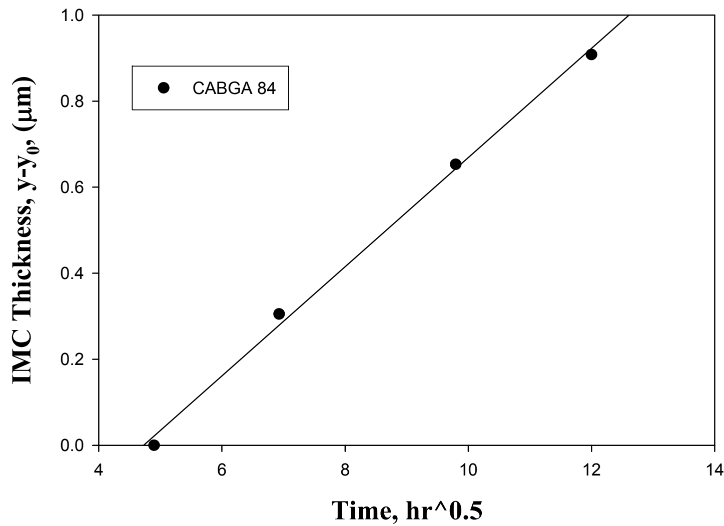


Figure 69: IMC Growth, at Various Levels of time for CABGA 84 with 95.5Sn4Ag0.5Cu Alloy.

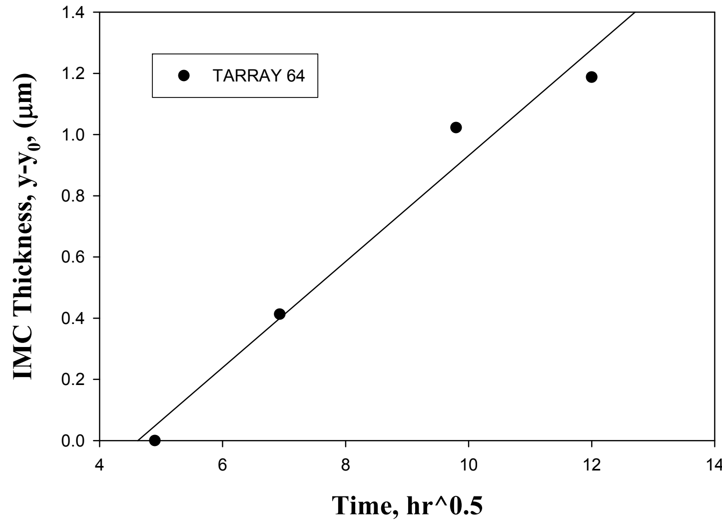


Figure 70: IMC Growth, at Various Levels of time for TAPE ARRAY 64 with 95.5Sn4Ag0.5Cu Alloy.

From this graphs we see that IMC growth rate varies for different components. Figure 65 to Figure 70 shows a comparative study of IMC growth rate between various packaging architectures with 95.5Sn4Ag0.5Cu alloys. A correlation between IMC growth rate and time can be used as a proxy parameter and evaluation of time at temperature for a deployed part.

4.4 Interrogation of System State

We have so far characterized the evolution of damage proxies (phase growth, IMC growth) by subjecting test packages to discrete time intervals of isothermal stress. In this section, a methodology for determining prior damage by interrogating the damage proxies of test structures has been presented. A set of electronic assembly has been subjected to thermal aging (125ºC). The thermal environment is intended to simulate a field application environment. The parts are withdrawn form the application environment for redeployment in a new field environment. The damage proxies have been interrogated

to determine the extent of damage inflicted and also remaining useful life of that assembly if it is to be redeployed. Following sections will explain the prediction of stress history using phase growth and IMC growth in thermal aging environments.

4.5 Levenberg – Marquardt Algorithm

The relationship between the phase growth parameter and time is nonlinear because it contains terms with fourth power. Inverse solution for interrogation of system-state is challenging for damage evolution in such systems. Levenberg-Marquardt (LM) algorithm is an iterative technique that computes the minimum of a non-linear function in multi-dimensional variable space [Madsen 2004, Lourakis 2005, Nielsen 1999]. It has been used successfully for computation of nonlinear least-square solutions. The Levenberg-Marquardt method with a combination of steepest descent using line-search and the Gauss-Newton method has been used for solution of the problem.

Let *f* be an assumed functional relation between a measurement vector referred to as prior-damage and the damage parameter vector, p, referred to as predictor variables. Mathematically, the function, f, which maps a parameter vector p Є Rm to an estimated measurement vector is represented as, x=*f*(p) x Є Rn. The measurement vector is the current values of the leading-indicator of failure and the parameter vector includes the prior system state, and accumulated damage and the damage evolution parameters. An initial parameter estimate p_0 and a measured vector x are provided and it is desired to find the parameter vector p, that best satisfies the functional relation *f* i.e. minimizes the squared distance or squared-error, $\varepsilon^T\varepsilon$ with $\varepsilon = x - f(p)$. Assume that $g(p) = \varepsilon^T\varepsilon$ in the squared error.

The basis of the LM algorithm is a linear approximation to g in the neighborhood of p. For a small δp, a Taylor series expansion leads to the approximation

$$g(p + \delta p) \approx g(p) + J(p)\delta p \qquad (10)$$

Where, J = Jacobian matrix $\partial f(p)/\partial p$. For each step, the value of δp that minimizes the quantity $\varepsilon = x - Jf(p)$, has been computed. Then the minimizer parameter vector, p, for the error function has been represented as,

$$F(p) = \frac{1}{2}\sum_{i=1}^{m}(g_i(p))^2 = \frac{1}{2}\|g(p)\|^2 = \frac{1}{2}g(p)^T g(p)$$

$$F'(p) = J(p)^T g(p) \qquad (11)$$

$$F''(p) = J(p)^T J(p) + \sum_{i=1}^{m} g_i(x) g_i''(x)$$

Where F(p) represents the objective function for the squared error term $\varepsilon^T\varepsilon$, J(p) is the Jacobian, and F'(p) is the gradient, and F"(p) is the Hessian. An initial parameter estimate p_0 and a response-vector "x" are provided and it is desired to find the vector p+, that best satisfies the functional relation x=f(p), while minimizing the squared distance $\varepsilon^T\varepsilon$. The steepest gradient descent method has been used to impose the descending condition, i.e., $F(p_{k+1}) < F(p_k)$. Depending on the starting guess p_0, a given function may have numerous minimizers, not necessarily the global minima. It therefore becomes necessary to explore the whole bounded space to converge to the global minima. The iteration involves finding a descent direction "h" and a step length giving a good decrease in the F-value.

The variation of an F-value starting at "p" and with direction "h" is expressed as a Taylor expansion, as follows:

$$F(p+\alpha h) = F(p) + \alpha h^T F'(p) + O(\alpha^2) \qquad (12)$$

where α is the step-length from point "p" in the descent direction, "h". For a sufficiently small α, $F(p+\alpha h) \cong F(p) + \alpha h^T F'(p)$. If $F(p+\alpha h)$ is a decreasing function of α at $\alpha = 0$, then 'h' is the descent direction. Mathematically, "h" is the descent direction of F(p) if $h^T F'(p) < 0$. If no such "h" exists, then F'(p)=0, showing that in this case the function is stationary. Since the condition for the stationary value of the objective function is that the gradient is zero, i.e. $f'(p+h) = L'(h) = 0$.

Therefore, the descent direction can be computed from the equation,

$$(J^T J) h_{gn} = -J^T g \qquad (13)$$

In each step, Newton method uses α = 1, and $p = p + \alpha h_{gn}$. The value of α is found by line search principle described above. Levenberg-Marquardt algorithm is a hybrid method which utilizes both steepest descent principle as well as the Gauss-Newton method. When the current solution is far from the correct one, the algorithm behaves like a steepest descent method: slow, but guaranteed to converge. When the current solution is close to the correct solution, it becomes a Gauss-Newton method. The LM method actually solves a slight variation of Equation (11), known as the augmented normal equations.

$$(J^T J + \mu I)\, h = -J^T g \qquad (14)$$

The term μ is called as the damping parameter, μ>0 ensures that coefficient matrix is positive definite, and this ensures that h is a descent direction. When the value of μ is large, we get $h \approx -\frac{1}{\mu} J^T g = -\frac{1}{\mu} F'(p)$ implying a short

step in the steepest descent direction, which is beneficial if the iterate is far from the solution. When the value of μ is very small, then the step size for LM and Gauss-Newton are identical. Algorithm has been modified to take the equations of phase growth and inter-metallic growth under both iso-thermal aging loads to calculate the unknowns.

4.6 Phase Growth Prediction

The following phase growth equation [Callister, 1985, Senkov 1986] has been used to for development of the prior stress history,

$$g^4 - g_0^4 = a(t)^b \qquad (15)$$

where b is slope of the equation and a is a constant term. g_0 is the initial grain size, g is the grain size at time t. From the population devices subjected to thermal aging, four condition monitoring devices have been withdrawn and sectioned for four-different isothermal aging durations. The damage proxies have been measured for all the samples. Each following equation represents each interval

$$g_1^{\ 4} = g_0^4 + a(t + \Delta t_1)^b \qquad (16)$$

$$g_2^{\ 4} = g_0^4 + a(t + \Delta t_2)^b \qquad (17)$$

$$g_3^{\ 4} = g_0^4 + a(t + \Delta t_3)^b \qquad (18)$$

$$g_4^{\ 4} = g_0^4 + a(t + \Delta t_4)^b \qquad (19)$$

Since the equations being non-linear in nature, a solution using simultaneous equation approach is very difficult to achieve. Therefore, non-linear least square method has been used for obtaining solution. Variable Solutions differ widely in their magnitudes. In order to find the global minima of error, it is necessary to solve the

equations for a bounded solution of the variables. Based on accelerated test experimental data, acceptable ranges of solutions for the variables a, b and g_0 was developed (See Table 8).

Table 8: Variable Range for Phase-Growth in Thermal Aging (based on Experimental data)

Variables	**Trust Region**
Constant 'a'	0.0002 – 0.005
Constant 'b'	0.60 - 1.50
Initial Grain size 'g_0' (μm)	0.60- 1.00
Aging Time (hrs)	1 - 150

The equations used in LM algorithm for phase growth are of the form x = f(p)

$$g = \sqrt[4]{g_0 + a(t + \Delta t)^b}$$

Where g is the grain size at different time intervals (Δt), and g_0, a, t and b are the parameters to be found. Since the LM method does a linear approximation to the specified function in the neighborhood of parameter to be found, it does so by using a Taylor series expansion for next approximation. Therefore, it is necessary to give the Jacobian with respect to each unknown.

$$\frac{\partial g}{\partial g_0} = \frac{g_0^{\ 3}}{\left(g_0^{\ 4} + a\left(t + \Delta t\right)^b\right)^{3/4}} \tag{20}$$

$$\frac{\partial g}{\partial a} = \frac{(t + \Delta t)^{\ b}}{4\left(g_0^{\ 4} + a\left(t + \Delta t\right)^b\right)^{3/4}} \tag{21}$$

$$\frac{\partial g}{\partial t} = \frac{ab(N + \Delta N)^{\ b}}{4(t + \Delta t)\left(g_0^{\ 4} + a\left(t + \Delta t\right)^b\right)^{3/4}} \tag{22}$$

$$\frac{\partial g}{\partial b} = \frac{a\log(t + \Delta t)(t + \Delta t)^{b}}{4\left(g_0^{\,4} + a\left(t + \Delta t\right)^{b}\right)^{3/4}} \tag{23}$$

Variables g_0, a, t, b, were varied one at a time, while keeping the other three variables constant and were provided as input to the Levenberg-Marquardt algorithm. Schematic illustration of the operation is shown in Figure 71.

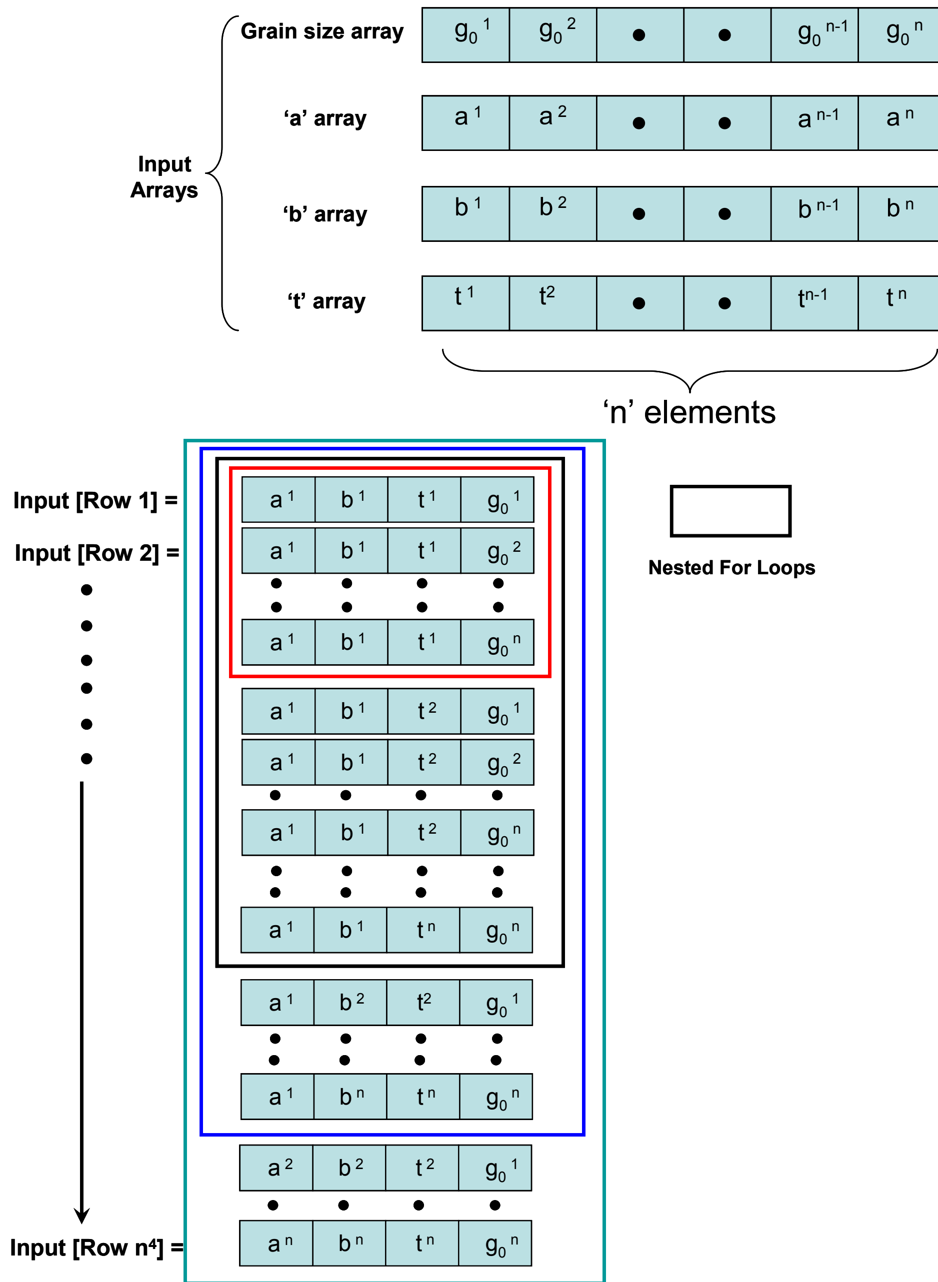


Figure 71: Schematic illustration of input to the LM minimization code

The output from the algorithm, g_0, a, t, b and minimization error was computed for each iteration. Sample row-wise output provided below

0.880941 0.001154379 28.8075 1.13218 0.007383792

The row corresponding to the least minimization error was isolated, and the variables in that row were selected as the final values for g_0, a, t, b. In order to calculate the damage and remaining useful life under isothermal load the phase-growth data were taken for different packages for four different cycle intervals in the time-neighborhood of prognostication of the electronic package, at various thermal aging times. The measured grain size values were given as input to the Levenberg-Marquardt Algorithm. The solution has been identified as the one with minimum error. Show the plots for minimization error versus aging time.

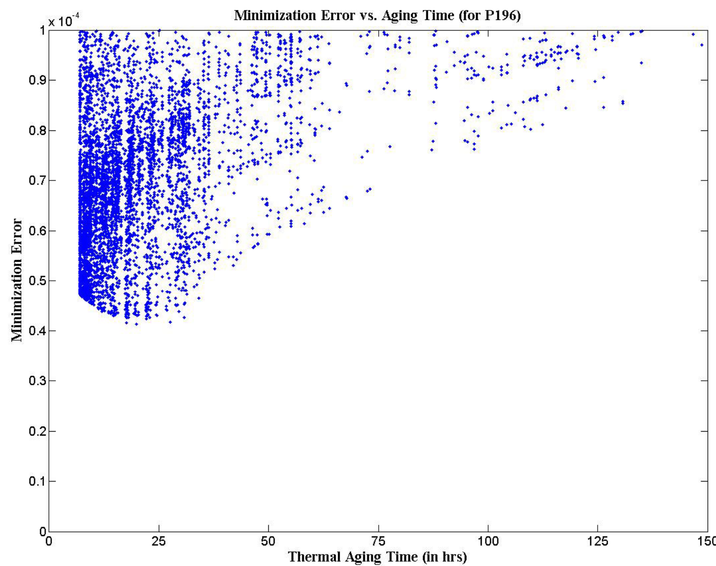


Figure 72: LM algorithm convergence plot for phase growth under aging load for 196 I/O BGA.

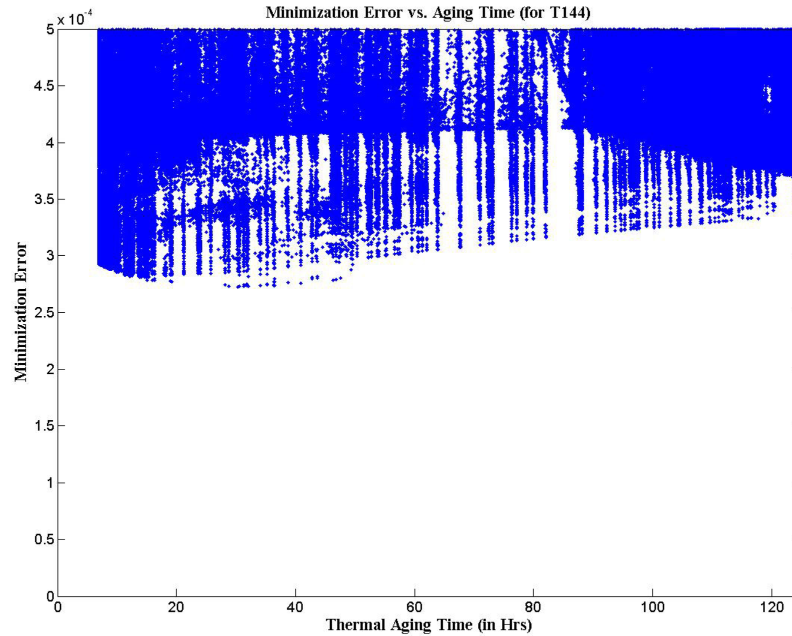


Figure 73: LM algorithm convergence plot for phase growth under aging load for 144 I/O BGA.

In the case of isothermal aging, the values of g_0, a, b and t have been computed. The computed values of g_0, a, b and t have been compared with the experimentally measured values for the same package. The error is minimum in the neighborhood of 19 hours, indicating that prior deployed-life, t = 19 hours is the solution for the 196 I/O BGA. The error is minimum in the neighborhood of 30 hours, indicating that prior deployed-life, t = 30 hours is the solution for the 144 I/O BGA. Both the values correlate well with the actual value of 24 hours from experimental data.

Table 9 shows the g_0, t values and their correlation of computed values with experimental values for the various packages including, 144 I/O Tape Array BGA, 196 I/O Plastic BGA. The packages have been prognosticated in the neighborhood of five experimental data-points including, 24, 48, 96, 124, and 240 hours. The computed phase-

sizes and aging-time have been plotted in Figure 25. The experimental data and the model predictions show good correlation.

Table 9: Results comparison with experiments

Package	Results			
	T (hrs)		g_0 (μm)	
	LM Algorithm	Experiment	LM Algorithm	Experiment
T144	30.29	24	0.832	0.834
P196	19.89	24	0.895	0.899

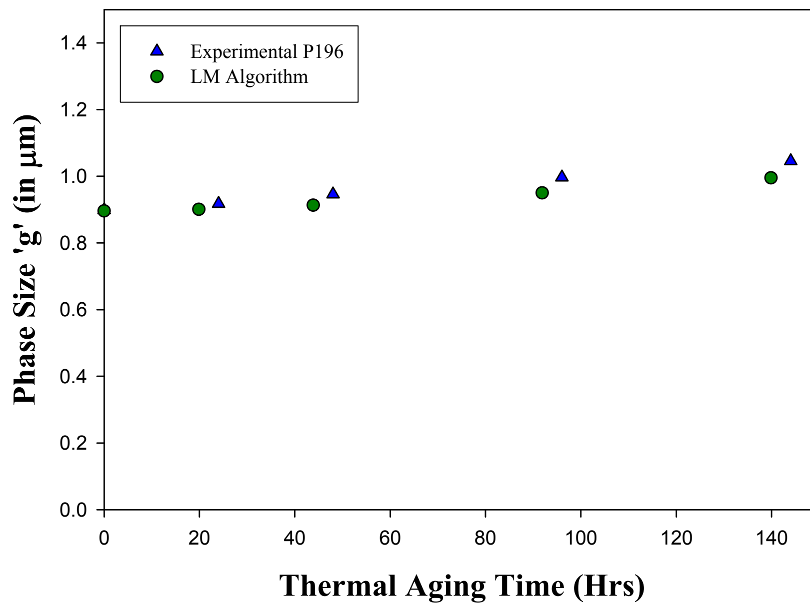


Figure 74: Graphical comparison of final results (PBGA 196).

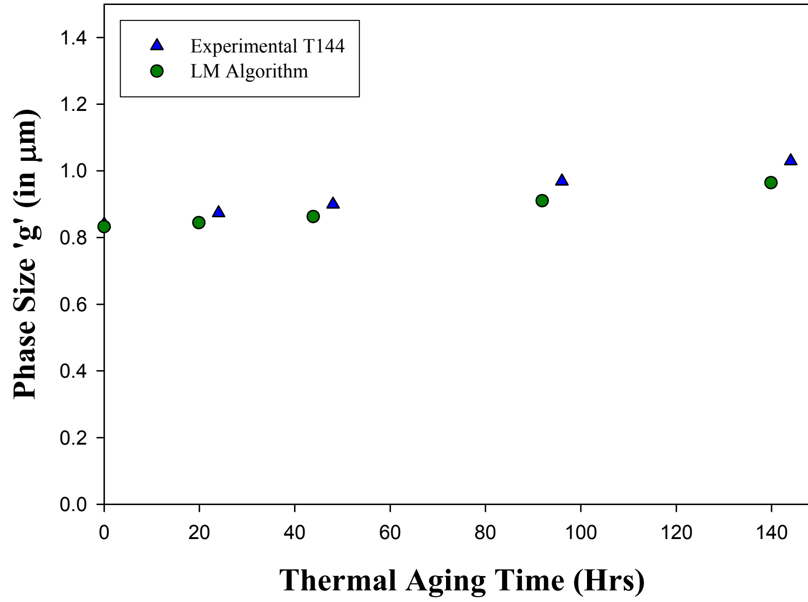


Figure 75: Graphical comparison of final results (T144).

4.7 IMC Growth Prediction

In this portion of the study, a second damage proxy, the growth of the intermetallic thickness during thermal aging as leading indicator of failure, has been measured. The following IC growth equation has been used for the development of the prior stress history is as follows:

$$y(t) = y_0 + k(t)^{0.5} \qquad (24)$$

In order to interrogate the system state using IMC as a damage proxy, three condition monitoring devices have been withdrawn at discrete time intervals, leading to the following equations for the evolution of IMC thickness.

$$y_1(t) = y_0 + k(t + \Delta t_1)^{0.5} \qquad (25)$$

$$y_2(t) = y_0 + k(t + \Delta t_2)^{0.5} \qquad (26)$$

$$y_3(t) = y_0 + k(t + \Delta t_3)^{0.5} \qquad (27)$$

The unknowns in this case are y_0, k and t. Similar to the methodology used for phase growth (explained above), Levenberg – Marquardt Algorithm was used to get the solution. In order to explore the whole design space, acceptable range for each variable, for each alloy was developed. Table 10 shows the range for each variable for each alloy system.

Table 10: Variable Range for IMC growth for various alloys

Variable	Trust Region
Initial IMC 'y_0' (µm)	3.0 – 5.5
Constant 'k'	0.05 – 0.27
Time 't' (hrs)	1 – 100

Similar to the methodology adopted for phase growth, Jacobian(s) with respect to each unknown were also provided as follows:

$$\frac{\partial y}{\partial y_0} = 1 \qquad (28)$$

$$\frac{\partial y}{\partial k} = (t + \Delta t)^{1/2} \qquad (29)$$

$$\frac{\partial y}{\partial t} = \frac{1}{2}\frac{k}{(t + \Delta t)^{1/2}} \qquad (30)$$

Initial guess values for variables y_0, k, t were varied one at a time, while keeping the other three variables constant and were provided as input to the Levenberg-Marquardt algorithm. The output from the algorithm, y_0, k, t and minimization error was computed for each iteration. The row corresponding to the least minimization error was isolated,

and the variables in that row were selected as the final values for y_0, k, t. The computed values of y_0, k and t have been compared with the experimentally measured values for the same package. The error is minimum in the neighborhood of 19 hours, indicating that prior deployed-life, t = 18 hours is the solution for the 196 I/O BGA. The error is minimum in the neighborhood of 22 hours, indicating that prior deployed life, t = 22 hours is the solution for the 84 I/O BGA. Both the values correlate well with the actual value of 24 hours from experimental data.

Table 11 shows the y_0, t values and their comparison with experimental values for the various packages including, 64 I/O Tape Array BGA, 84 I/O Chip Array BGA, 196 I/O Plastic BGA, 280 I/O Flex BGA, and 676 I/O Plastic BGA. The packages have been prognosticated in the neighborhood of five-experimental data points including, 24, 48, 96, 124, and 240 hours. The computed IMC thickness and aging-time have been plotted in Figure 78 to Figure 82. The experimental data and the model predictions show good correlation.

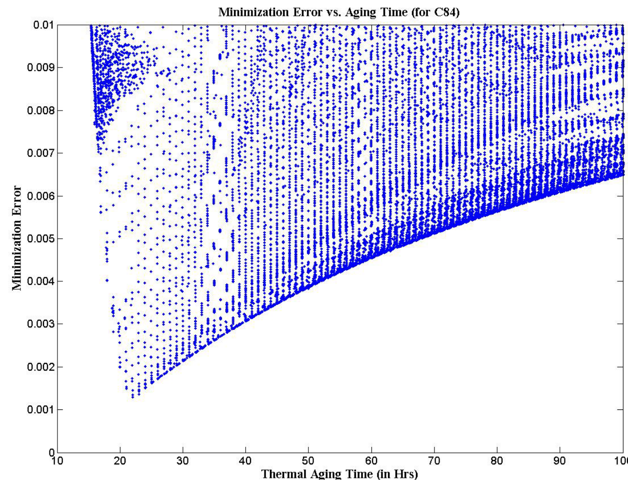


Figure 76: LM algorithm convergence plot - IMC growth under aging for C84 I/O BGA.

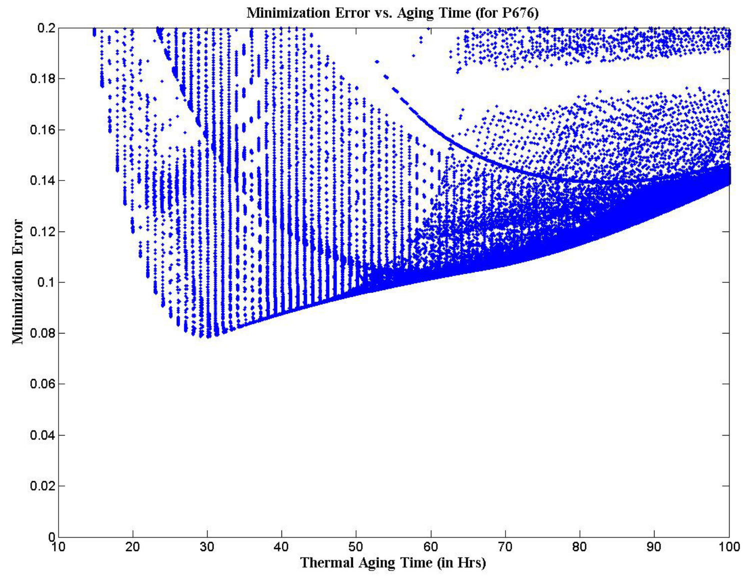


Figure 77: LM algorithm convergence plot for IMC growth under aging load for 676 I/O Plastic BGA.

Table 11: Algorithm Results comparison with experiments

Package	Results			
	T (hrs)		y_0 (μm)	
	LM Algorithm	Experiment	LM Algorithm	Experiment
P676	30.13	24.00	5.499	5.285
P196	17.97	24.00	3.715	4.141
C84	22.00	24.00	5.499	4.311
F280	29.04	24.00	3.388	4.116
T64	23.87	24.00	3.301	3.231

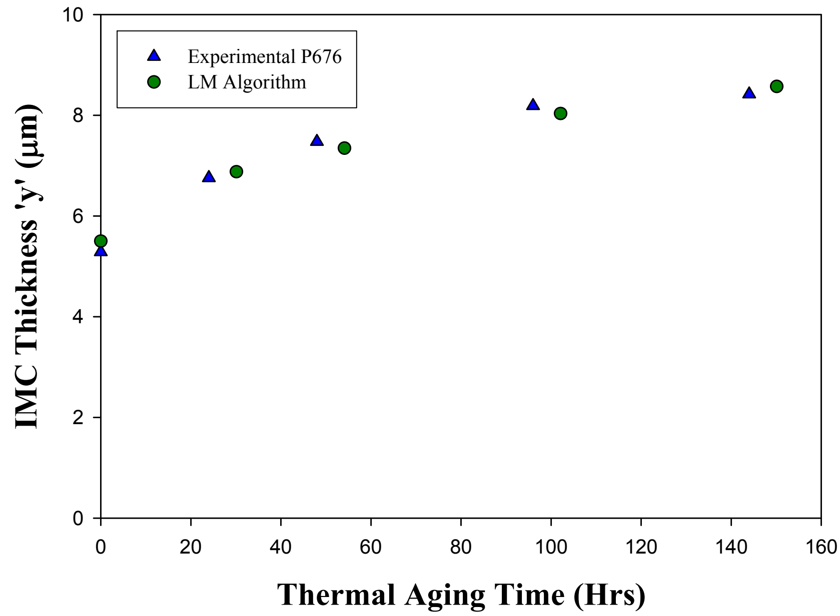


Figure 78: Graphical comparison of final results (P676).

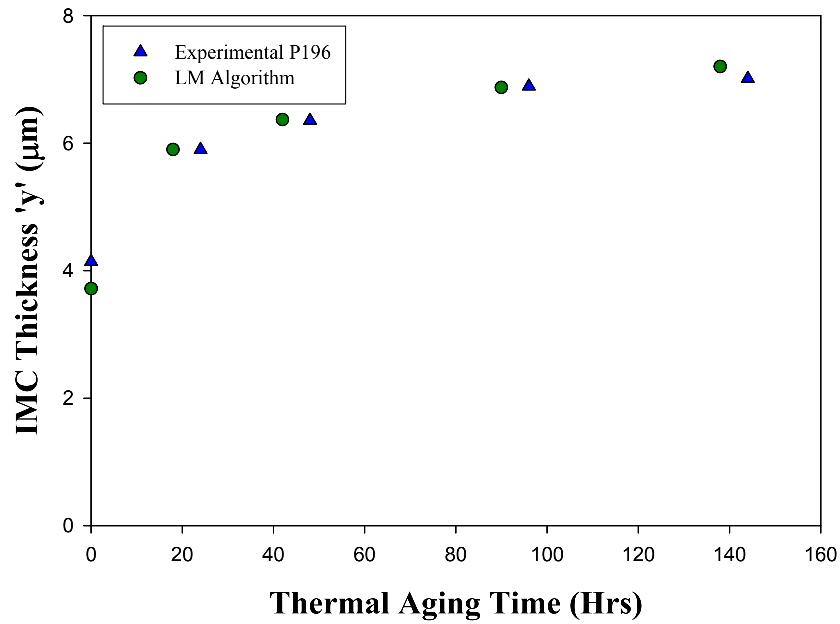


Figure 79: Graphical comparison of final results (P196).

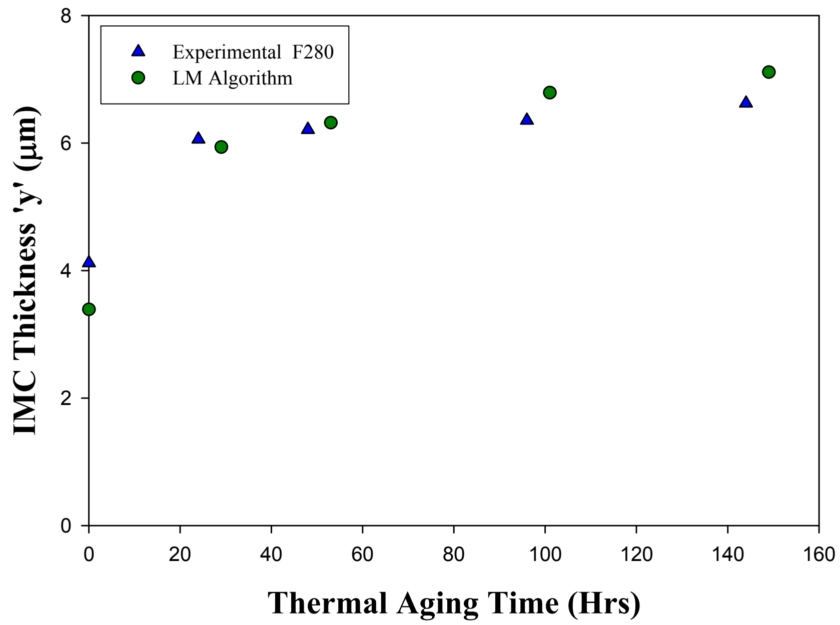


Figure 80: Graphical comparison of final results (F280).

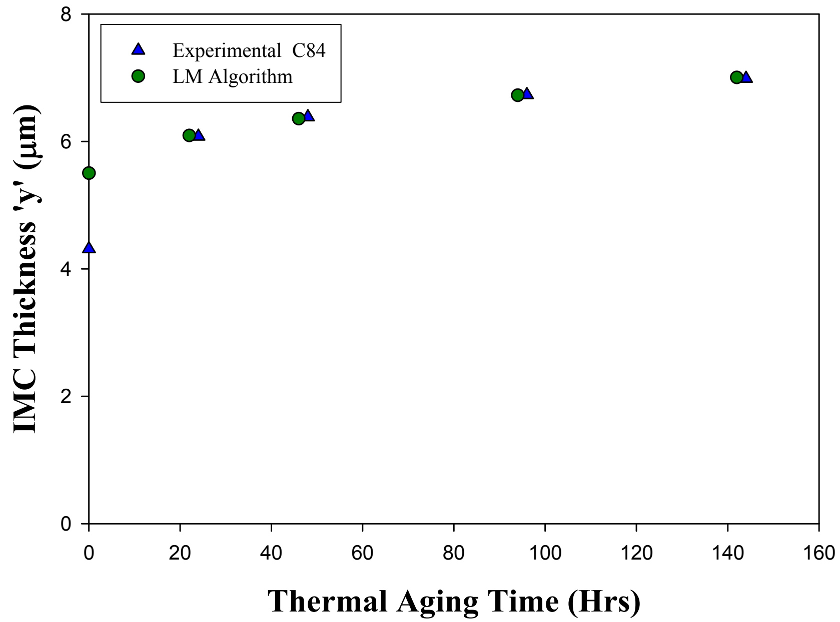


Figure 81: Graphical comparison of final results (C84).

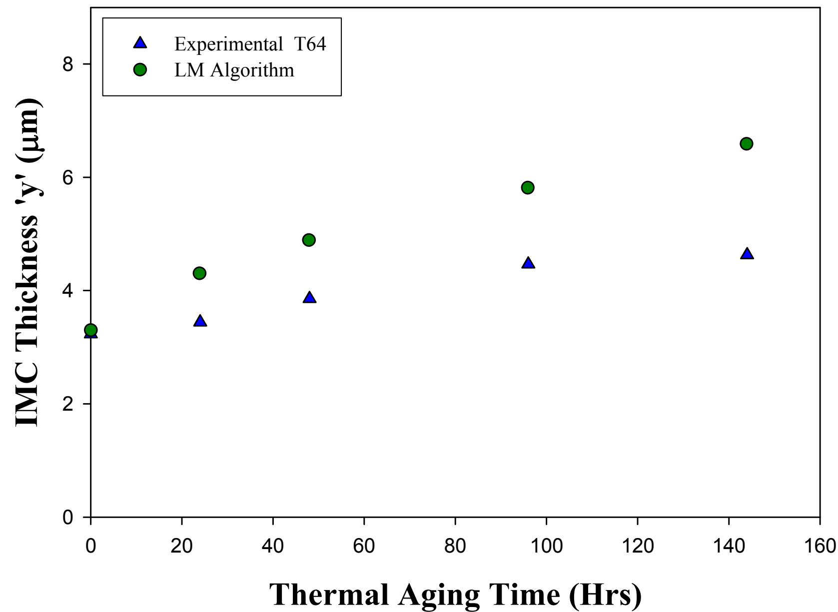


Figure 82: Graphical comparison of final results (T64).

4.8 Implementation of Damage Pre-Cursors Approach

The prognostics approach presented in here may be implemented using sacrificial devices, which can be cross-sectioned to determine the failure progression of the assembly. It is envisioned that the sacrificial devices will be small, low cost devices, such that several of these can be conveniently located along edge of card assemblies to enable cross-sectioning or on a separate card within an electronic module or card cage.

For example, in the case of solder interconnects, chip resistors may be included on the board assembly and serve as sacrificial devices, which can be periodically cross-sectioned. It is not required to assume that all the components mounted on the same board have the same exposure to environmental or operational stresses. However, it is required that the stress variation for the different devices be known and characterized.

The sacrificial components are cross-sectioned when the card assemblies, e.g. avionic card assemblies aboard aircraft, need to be redeployed. The baseline phase-size is then measured. The part assemblies to be deployed in the intended use environment will then be subjected to finite-cycles of controlled environmental temperature exposure characteristic of the intended use environment. Another sample of the sacrificial device is then cross-sectioned to enable calculation of the phase growth rate. The residual life can then be calculated based on knowledge of the accumulated initial damage and the phase growth rate in intended use environment. The sacrificial components include the same mechanisms that lead to failure in standard components. Further, given the damage state of a deployed component, the prior-elapsed time in any thermal environment can be computed based on known phase growth rate, given the initial phase size after reflow. The residual life can then be computed based on the computed phase growth rate for the desired use environment.

4.9 Summary and Conclusions

A damage pre cursors based methodology for prognostication-of-electronics including assessment of residual-life, has been developed and demonstrated under single stresses of thermal cycling and steady-state temperature. The damage pre-cursors enable assessment of system damage-state significantly prior to appearance of any macro-indicators of damage. Phase growth rate and interfacial intermetallic layers growth rate have been identified as valid proxies for determination of residual life in electronic structures. The theoretical basis for the selection of prognostic parameters has been justified based on particle growth induced by volume diffusion. Mathematical

relationships have been developed between phase growth, derivatives of phase growth, intermetallic growth for interrogation of residual life and damage state. A framework for implementation of the prognostication approach has been discussed including, sacrificial devices, which can be examined to determine the damage state of the assembly.

CHAPTER 5

PROGNOSTICS HEALTH MANAGEMENT OF LEAD-FREE Ag BASED SOLDER ELECTRONICS IN HARSH CYCLING ENVIRONMENTS

Requirements for system availability for ultra-high reliability electronic systems such as implantable biological systems are driving the need for advanced heath monitoring techniques for early detection of onset of damage. Traditional health monitoring methodologies have relied on reactive methods of failure detection often providing little on no insight into the remaining useful life of the system. Detection of system-state significantly prior to catastrophic failure can significantly impact the reliability and availability of electronic systems.

Applications for the presented PHM framework include, implantable biological applications such as pacemakers, and implantable cardioverter-defibrillators, consumer applications such as automotive safety systems including front and rear impact protection system, chassis-control systems, x-by-wire systems; and defense applications such as avionics systems, naval electronic warfare systems.

5.1 Introduction

Previously, Lall, et. al. [2004, 2005, 2006, 2007] have developed methodologies for health management and interrogation of system state of electronic systems based on leading indicators. Examples damage pre- cursors include micro-structural evolution,

intermetallics, stressgradients. Pre-cursors have been developed for both eutectic 63Sn37Pb and Sn4Ag0.5Cu alloy systems on a variety of area-array architectures.

In this study, a mathematical approach for interrogation of system state under cyclic thermo-mechanical stresses has been developed for 3-different leadfree solder alloy systems. Thermal cycles may be experienced by electronics due to power cycling or environmental cycling. Data has been collected for leading indicators of failure for alloy systems including, Sn3Ag0.5Cu-Bi, Sn3Ag0.5Cu-Bi-Ni, 96.5Sn3.5Ag second-level interconnects under the application of cyclic thermo-mechanical loads. Methodology presented resides in the pre-failure space of the system in which no macro-indicators such as cracks or delamination exist. Systems subjected to thermo-mechanical damage have been interrogated for system state and the computed damage state correlated with known imposed damage. The approach involves the use of condition monitoring devices which can be interrogated for damage proxies at finite time-intervals. Interrogation techniques are based on non-linear least-squares methods. Various techniques including the Levenberg-Marquardt Algorithm have been investigated. The system's residual life is computed based on residual-life computation algorithms.

5.2 Test Vehicle

In the present study, three lead free solder compositions including, Sn0.3Ag0.7Cu-0.1Bi, Sn0.2Ag0.7Cu-0.1Bi0.1Ni, 96.5Sn3.5Ag on identical ball-grid arrays with FR4-06 laminates have been studied under thermo-mechanical loads. Table 12 shows package parameters for the test vehicles used in this study.

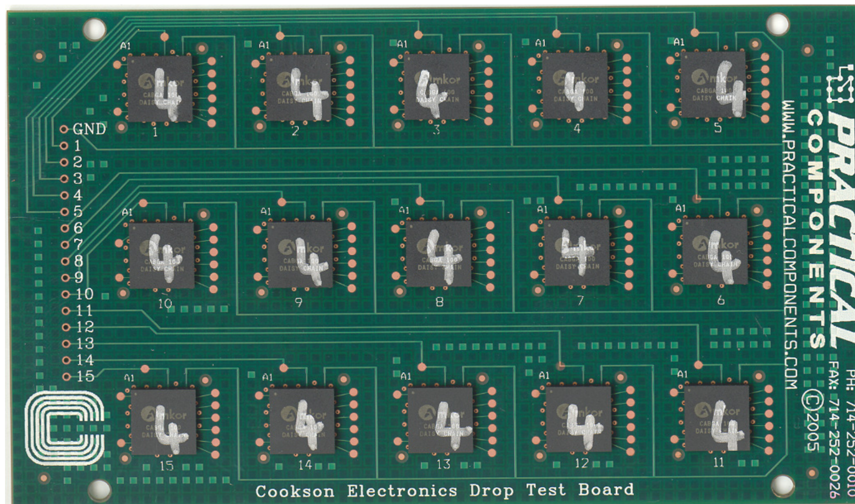


Figure 82: Test Vehicle (15 CABGA 100 I/O Packages)

Table 12 : Package Details

Body Size	Solder	Ball Count	Ball Pitch (mm)	Die Thick (mm)	Die Size (mm)	BT Thickness (mm)	Ball Diameter (mm)
10 mm	Sn0.3Ag0.7Cu0.1Bi	100	0.8	0.26	6.4	0.26	0.50
10 mm	Sn0.2Ag0.7Cu0.1Bi0.1Ni	100	0.8	0.26	6.4	0.26	0.50
10 mm	96.5Sn3.5Ag	100	0.8	0.26	6.4	0.26	0.50

Phase growth and IMC data has been gathered and analyzed using image processing. Components analyzed include chip-array ball grid arrays with I/O counts in of 100, and body size of 10 mm. The boards contain six trace layers to simulate the thermal mass of a true production board, though all functional traces were run on the topmost layer. All pads on the board were non-solder mask defined (NSMD) and had an immersion silver finish. All components were assembled to the electroless nickel gold (ENIG) finish printed circuit board and subjected to -55ºC to 125ºC Cycle, 2.5 hour per cycle. In addition, separate set of board assemblies have been subjected to isothermal

aging at 125°C. All the assemblies were daisy-chained and continuously monitored for failure detection during cycling.

Temperature excursions during operation of a circuit are due to both power-cycling and variations in ambient conditions resulting in thermo-mechanical cyclic stresses and strains induced primarily by thermal expansion mismatch between the package and the board assembly. Previous researchers have studied the micro structural evolution of ternary SnAgCu alloys at elevated temperatures using bulk real solder joints with different designs, geometry and process conditions. The SnAgCu microstructure comprises Ag_3Sn and Cu_6Sn_5 dispersed within the tin matrix. The relatively low percentage of alloying elements, 1-4% for Ag and 0.5% for Cu results in phases which comprise a small percentage of the total volume within the solder joint. The microstructural evolution of SnAgCu alloys over time has been found to effect the thermo-mechanical properties and damage behavior [Ye 2000, Allen 2004a, b, Kang 2004, Xiao 2004, Henderson 2004, Kang 2005, Korhonen 2006, Jung 2001].

5.3 Leading Indicators of Failure:

Micro-structural coarsening during thermo-mechanical deformation is attributed to the generation of excess vacancies caused by the combined effect of local hydrostatic state of stress, and the instantaneous inelastic strain rate [Dutta 2003a, 2003b, 2004; Jung 2001]. Evolution of solder microstructure in 63Sn37Pb and lead-free chip resistor solder joints due to thermal fatigue have been studied previously by previous researchers [Sayama, et al. 1999, 2003] and thermal fatigue correlated with occurrence of microstructural coarsening in the fatigue damaged region in of 63Sn37Pb solder

interconnects [Frear 1990, Morris 1991]. Correlation of grain coarsening with thermal fatigue has also been established for high-lead solders [Bangs 1978, Wolverton 1987, Tribula 1989]. Previously the authors have investigated the grain-size evolution and derivatives of phase growth rate as prognostics parameters on a wide range of leaded and Sn4Ag0.5Cu devices in underhood applications [Lall 2004[b], 2005, 2006[a,b], 2007[a,b]].

In this paper, prognostics health management methodology has been presented to assess the prior damage is based on solder grain coarsening model. Phase growth under thermal cycling and thermal aging has been identified as the damage precursor to compute the residual life. The relation between phase growth parameter and time for polycrystalline material is given by [Callister 1985]

$$g^n - g_0^n = Kt \tag{31}$$

Where g is the average grain size at time t, g_0 is the average grain size of solder after reflow, K and n (varies from 2 to 5) are time independent constants.

Senkov and Myshlev [1986] applied the theory of phase growth process in a super plastic alloy and validated the theory for Zn/Al eutectic alloy. They expressed the phase growth parameter S as:

$$S = g^4 - g_0^4 = Kt \tag{32}$$

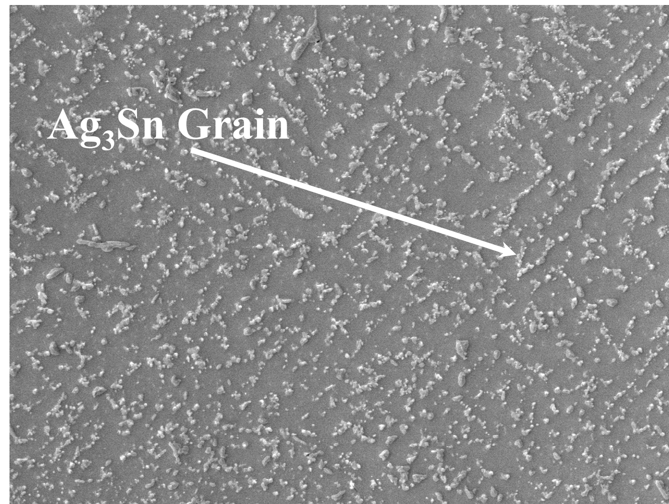


Figure 83: Ag_3Sn Grains in 96.5Sn3.0Ag0.5Cu solder microstructure

In this study, changes in solder microstructure and its derivatives have been investigated for use as the leading indicators of failure and interrogation of system state for assessment of damage from prior stress histories. Quantitative metrics of changes in microstructure have been identified and relationships developed to represent damage progression. Data presented covers a wide range of solder alloys including Sn0.3Ag0.7Cu0.1Bi, Sn0.2Ag0.7Cu0.1Bi0.1Ni, 96.5Sn3.5Ag lead-free area-array packaging architectures in extreme temperature cycling and steady-state temperature environments. The phase growth parameter has been defined as the relative change from phase-state after reflow, instead of the absolute value of phase state. Figure 83 shows Ag_3Sn Grains in solder microstructure.

5.4 Interrogation of System State:

In this section, a methodology for determining prior damage by interrogating the damage proxies of test structures has been presented. Two sets of electronic assemblies has been subjected to thermal cycling (-55°C to 125°C). The thermal environments are

intended to simulate a field application environment. The parts are withdrawn from the application environment for redeployment in a new field environment. The damage proxies have been interrogated to determine the extent of damage inflicted and also remaining useful life of that assembly if it is to be re-deployed. Following sections will explain the prediction of stress history using phase growth and IMC growth in thermal cycling and thermal aging environments respectively.

5.5 Levenberg – Marquardt Algorithm

The methodology presented in Section 4.5 of Chapter 4 has been implemented to interrogate the system state. Mathematical basis of method is not repeated here for the sake of brevity.

5.6 Prognostication of Leading-Indicators

Since the equations governing the phase growth and IMC compound are non-linear in nature, we have used Levenberg-Marquardt Algorithm to interrogate the system state in terms of damage proxies. The LM algorithm has been modified to take the equations for leading indicators of failure (e.g. phase growth and inter-metallic growth) under cycling loads and iso-thermal aging loads. The methodology is as follows:

5.7 Micro-structural Evolution

The following phase growth equation has been used for the development of the prior stress history is as follows:

$$g^4 - g_0^4 = a(N)^b \tag{33}$$

From the population devices subjected to thermal cycling, four condition

monitoring devices have been withdrawn and sectioned for four different thermal cycle durations. The phase size has been measured for all samples. Each of the following equations represents an interval of withdrawal, leading to the following equations.

$$g_1^{\;4} = g_0^4 + a(N + \Delta N_1)^b \quad (34)$$

$$g_2^{\;4} = g_0^4 + a(N + \Delta N_2)^b \quad (35)$$

$$g_3^{\;4} = g_0^4 + a(N + \Delta N_3)^b \quad (36)$$

$$g_4^{\;4} = g_0^4 + a(N + \Delta N_4)^b \quad (37)$$

In equations (34) – (37), we can see that there are four unknowns g_0, a, b and t. In order to compute the damage (no. of thermal cycles), it is necessary to solve this set of non-linear equations using a least squares methodology. In the present case, we have used the Levenberg Marquardt Algorithm (LMA) to obtain the solution. Variable solutions differ widely in their magnitudes. In order to find the global minima of the error, it is necessary to solve the equations for a bounded solution space. Based on the accelerated test experimental data, acceptable range for each variable, for each alloy system was developed. The variable range, for each variable was divided uniformly to form numerous initial guess values to be given as input guesses to the LM algorithm. Table 13 shows the range for each variable for each alloy system.

Table 13: Variable Range for phase growth in thermal cycling for various alloys (based on experimental data)

Alloy System	Constant 'a'	Constant 'b'	Initial Grain size 'g_0'
Sn0.3Ag0.7Cu0.1Bi	0.0001 - 0.002	1.15 - 1.40	1.40 – 1.60

Sn0.2Ag0.7Cu0.1Bi0.1Ni	0.0001 - 0.002	1.50 - 1.70	1.00 – 1.20
Sn3.5 Ag	0.002 - 0.02	1.00 - 1.20	1.35 – 1.55

The form of equation used in LMA for phase growth is

$$g = \sqrt[4]{g_0 + a(N + \Delta N)^b} \qquad (38)$$

Since the method does a linear approximation to the specified function in the neighborhood of the parameter to be found using Taylor series expansion for next approximation, it is necessary to give Jacobian with respect to each unknown.

$$\frac{\partial g}{\partial g_0} = \frac{g_0^{\ 3}}{\left(g_0^{\ 4} + a\left(N + \Delta N\right)^b\right)^{3/4}} \qquad (39)$$

$$\frac{\partial g}{\partial a} = \frac{(N + \Delta N)^b}{4\left(g_0^{\ 4} + a\left(N + \Delta N\right)^b\right)^{3/4}} \qquad (40)$$

$$\frac{\partial g}{\partial N} = \frac{ab(N + \Delta N)^b}{4(N + \Delta N)\left(g_0^{\ 4} + a\left(N + \Delta N\right)^b\right)^{3/4}} \qquad (41)$$

$$\frac{\partial g}{\partial b} = \frac{a\log(N + \Delta N)(N + \Delta N)^b}{4\left(g_0^{\ 4} + a\left(N + \Delta N\right)^b\right)^{3/4}} \qquad (42)$$

Initial guess values for variables g_0, a, N, b, were varied one at a time, while keeping the other three variables constant and were provided as input to the Levenberg-Marquardt algorithm. The output from the algorithm, g_0, a, N, b and minimization error was computed for each iteration. Sample row-wise output provided below

0.68026 0.001154379 228.8075 1.1418 0.006663792

The row corresponding to the least minimization error was isolated, and the variables in that row were selected as the final values for g_0, a, N, b. Variables g_0, a, N, b, were varied one at a time, while keeping the other three variables constant and were

provided as input to the Levenberg-Marquardt algorithm. Schematic illustration of the operation is shown in Figure 84,

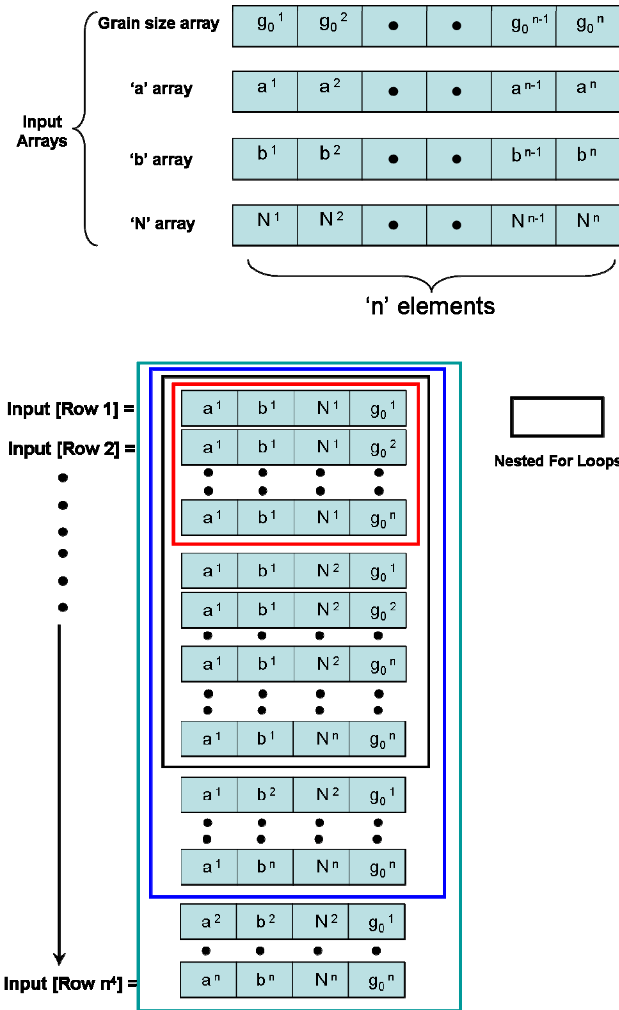


Figure 84: Schematic illustration of input to the LM minimization code

5.8 Intermetallic Compound Growth

The following IC growth equation has been used for the development of the prior stress history is as follows:

$$y(t) = y_0 + k(t)^{0.5} \qquad (43)$$

In order to interrogate the system state using IMC as a damage proxy, three condition monitoring devices have been withdrawn at discrete time intervals, leading to the

following equations for the evolution of IMC thickness.

$$y_1(t) = y_0 + k(t + \Delta t_1)^{0.5} \quad (44)$$

$$y_2(t) = y_0 + k(t + \Delta t_2)^{0.5} \quad (45)$$

$$y_3(t) = y_0 + k(t + \Delta t_3)^{0.5} \quad (46)$$

The unknowns in this case being y_0, k and t. Similar to the methodology used for microstructural coarsening (explained above), LMA was used to get the solution. In order to explore the whole design space, acceptable range for each variable, for each alloy was developed. Table 10 shows the range for each variable for each alloy system.

Table 14: Variable Range for IMC growth for various alloys

Alloy System	Initial IMC 'y_0' (µm)	Constant 'k'	Time 't' (hrs)
Sn0.3Ag0.7Cu0.1Bi	3.66 – 5.41	0.012 - 0.074	200 - 1600
Sn0.2Ag0.7Cu0.1Bi0.1Ni			
96.5Sn3.5Ag			

The form of equation used in LM for IMC growth is,

$$y(t) = y_0 + k(t + \Delta t)^{1/2} \quad (47)$$

The Jacobian with respect to each unknown was also provided as follows:

$$\frac{\partial y}{\partial y_0} = 1 \quad (48)$$

$$\frac{\partial y}{\partial k} = (t + \Delta t)^{1/2} \quad (49)$$

$$\frac{\partial y}{\partial t} = \frac{1}{2} \frac{k}{(t + \Delta t)^{1/2}} \tag{50}$$

Initial guess values for variables y_0, k, t were varied one at a time, while keeping the other three variables constant and were provided as input to the Levenberg-Marquardt algorithm. The output from the algorithm, y_0, k, t and minimization error was computed for each iteration. The row corresponding to the least minimization error was isolated, and the variables in that row were selected as the final values for $y_{0,}$ k and t.

5.9 Characterization of Damage Progression

Two identical sets of test-samples have been subjected to thermal cycling. In this section, the first data-set has been discussed. The first data-set has been used to characterize the progression of leading indicators of failure with the initiation and progression of thermo-mechanical damage. The average phase growth parameter S, which changes with thermal cycling has been measured from SEM back-scattered images. Figure 85 to Figure 87 show the SEM back-scattered images exhibiting examples of Ag_3Sn phase growth process in the 100 I/O Chip Array BGA at different levels of thermal cycle.

Most of the SnAgCu solder is comprised of Sn-phases, so that the growth rate of tin and Ag_3Sn intermetallic crystals are significant. Since Ag atoms have a higher diffusion rate in the molten solder, they can diffuse out of the way and thus allow the Sn dendrites to grow. Particles of Ag_3Sn grow either to spheres or to needles shape

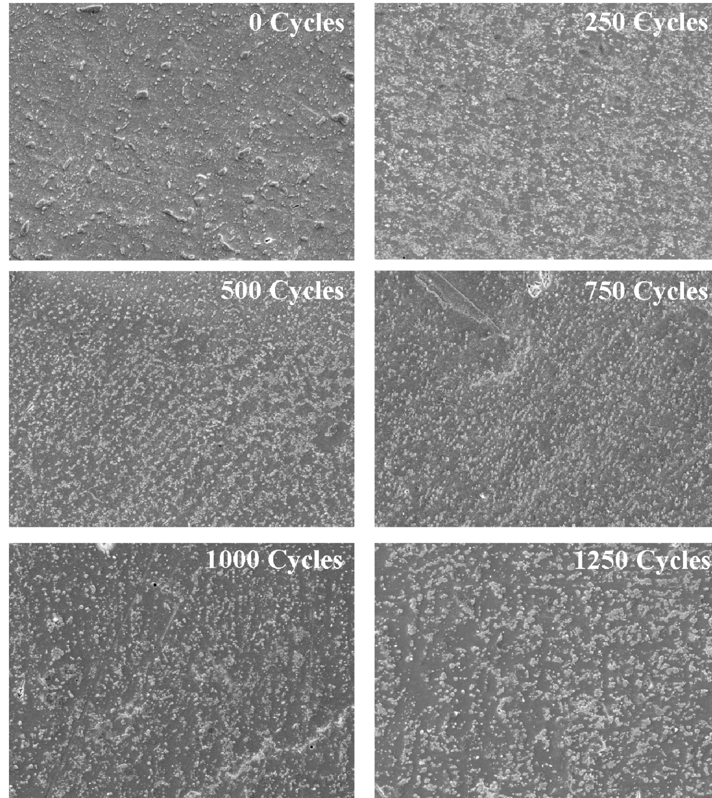


Figure 85: SEM Back-scattered Images of Phase Growth versus Thermal cycling (-55ºC to 125ºC, Sn0.3Ag0.7Cu0.1Bi solder, 100 I/O Chip Array BGA, Magnification 750x)

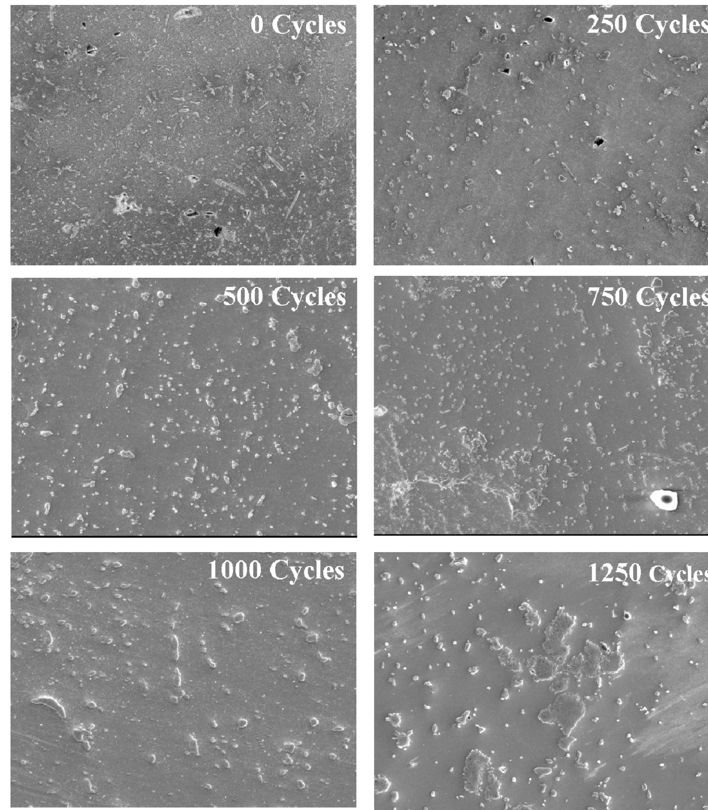


Figure 86: SEM Back-scattered Images of Phase Growth versus Thermal cycling (-55ºC to 125ºC), Sn0.2Ag0.7Cu 0.1Bi0.1Ni solder, 100 I/O Chip Array BGA, Magnification 750x)

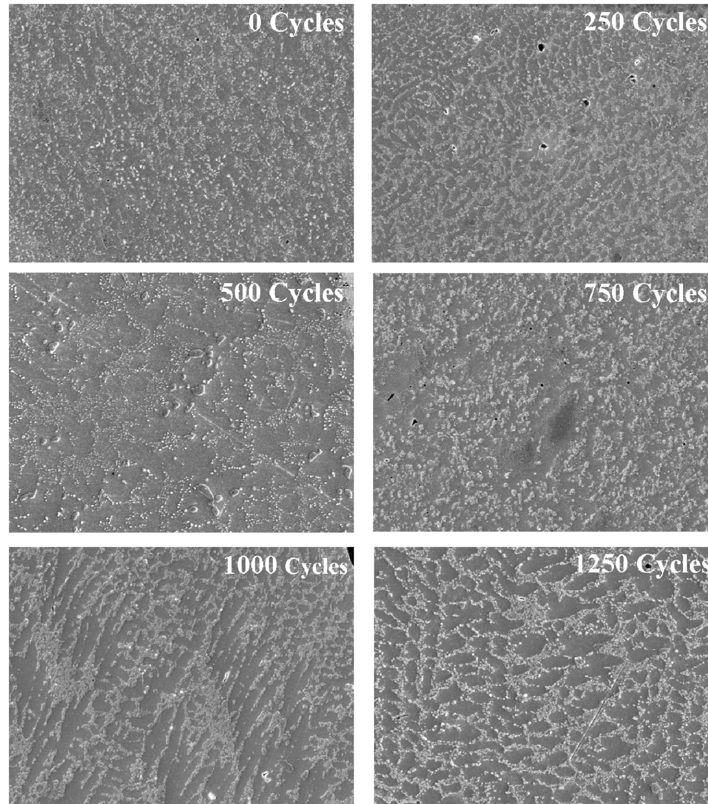


Figure 87: SEM Back-scattered Images of Phase Growth versus Thermal cycling (-55ºC to 125ºC, 96.5Sn3.5Ag plus solder, 100 I/O Chip Array BGA, Magnification 750x)

The average phase growth parameter S measured under thermal cycling and thermal aging for each individual component has been plotted versus cycles in Figure 88 to Figure 90. The phase growth data in this study indicates that phase growth rate stays fairly uniform during the thermal cycle tests. The phase growth also follows a linear pattern under isothermal aging. Since, and electronic system may have variety of material sets and packaging architectures, the linearity of micro-structural evolution depicts the validity of phase growth as a proxy for damage progression. The damage progression can thus be tracked in various devices based on damage proxies.

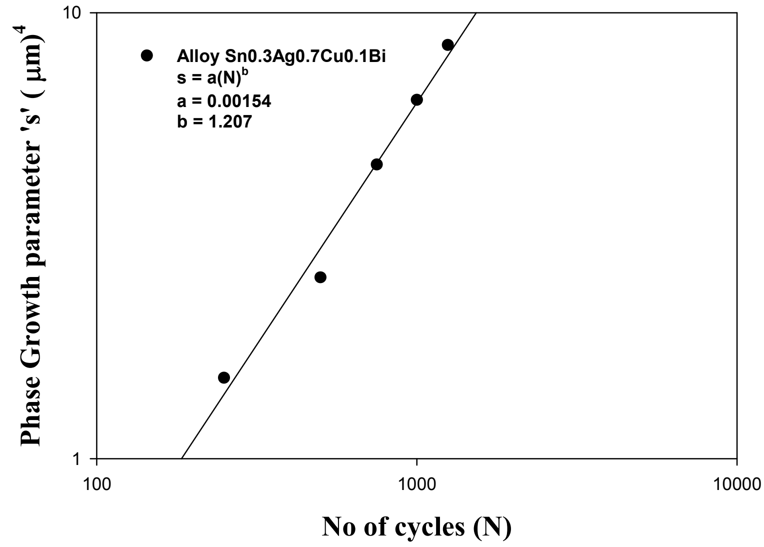


Figure 88: Phase Growth parameter, at various levels of cycles for 100 I/O Chip Array BGA, Sn0.3Ag0.7Cu0.1Bi solder interconnects

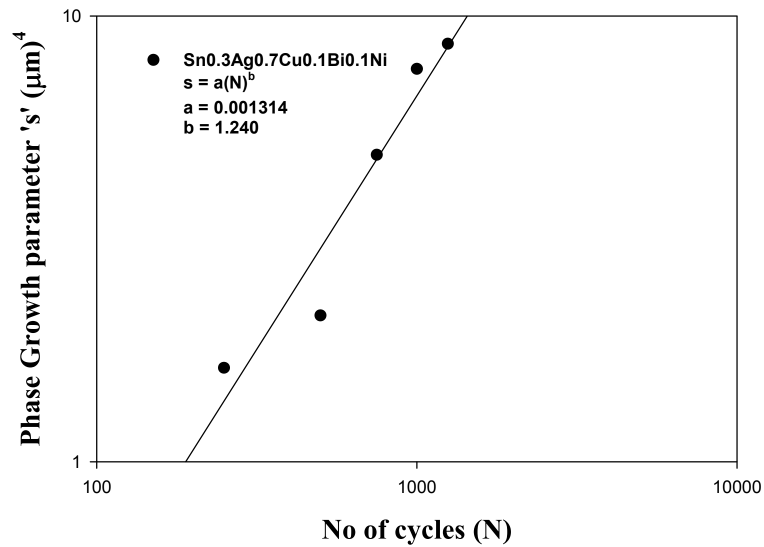


Figure 89: Phase Growth parameter, at various levels of cycles for 100 I/O Chip Array BGA, Sn0.3Ag0.7Cu0.1Bi0.1Ni solder interconnects

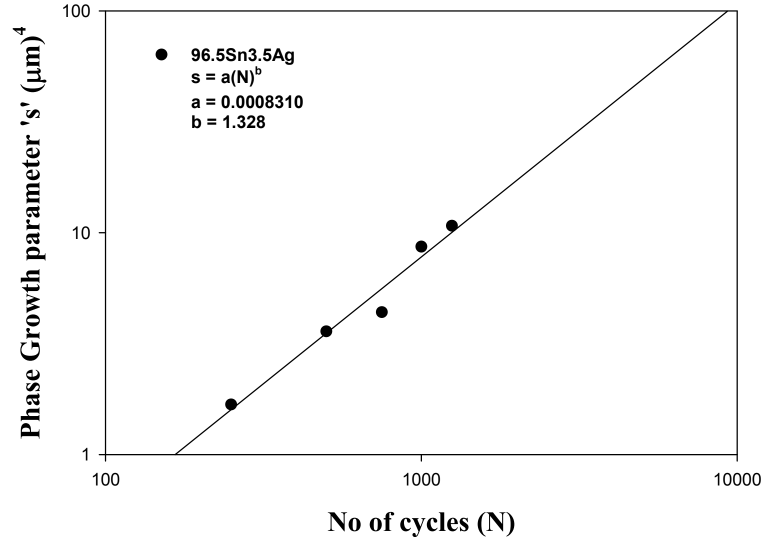


Figure 90: Phase Growth parameter, at various levels of cycles for 100 I/O Chip Array BGA, 96.5Sn3.5Ag solder interconnects

In addition to the phase growth progression, the progression of IMC growth has also been studied. The cycled components have been cross sectioned at various interval of thermal aging. The IMC thickness has been measured in SEM using 1000x magnification using commercial image processing software. An energy dispersive X-ray (EDX) has been used to examine the morphology and the composition of the intermetallic compound layer at the copper/solder interface. Colloidal silica solution has been applied for the detailed intermetallic compound composition observation and detection. Figure 91 to Figure 93 show SEM backscattered images exhibiting examples of IMC growth with aging time for 100 I/O, BGA solder ball for the three-alloys.

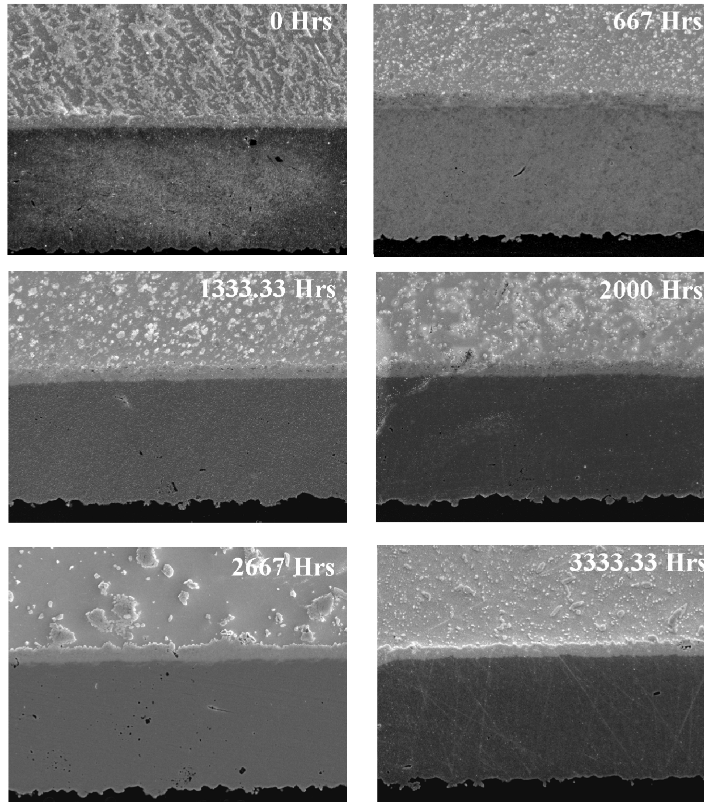


Figure 91: SEM Back-scattered images of IMC Growth versus Thermal Aging for Sn0.3Ag0.7Cu0.1Bi (Magnification 1000x)

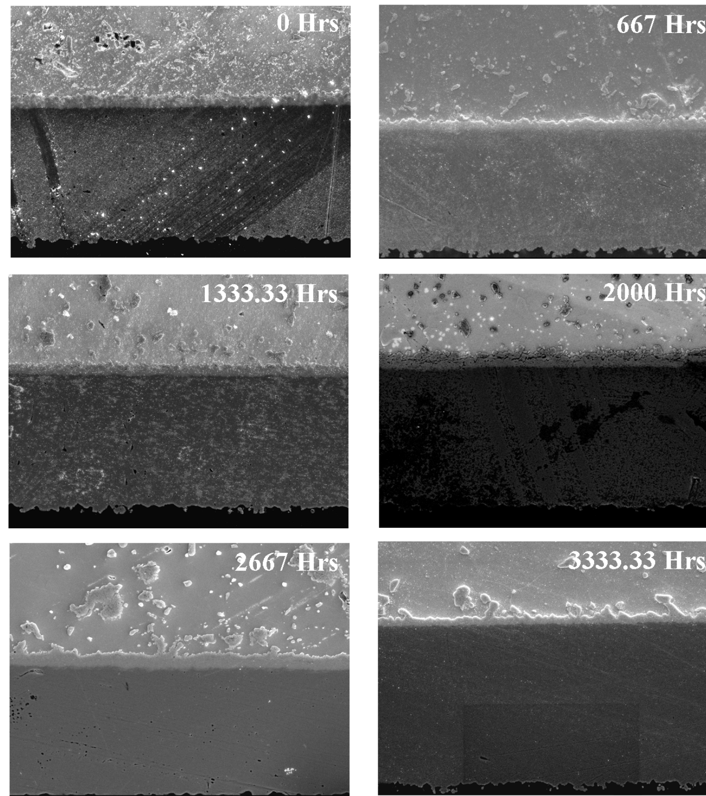


Figure 92: SEM Back-scattered images of IMC Growth versus Thermal Aging Sn0.3Ag0.7Cu0.1Bi0.1Ni (Magnification 1000x)

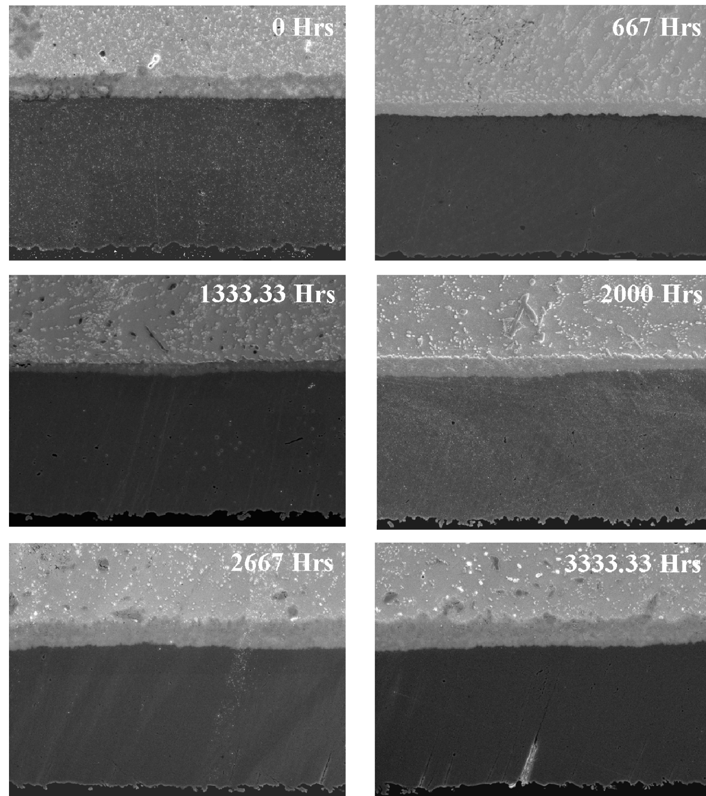


Figure 93: SEM Back-scattered images of IMC Growth versus Thermal Aging for Sn3.5Ag (Magnification 1000x)

Trend analysis of intermetallic thickness growth on SEM using image processing software, indicates a square root dependence of IMC thickness versus aging time,

$$y = y_0 + kt^n \qquad (51)$$

where y(t) is IMC growth thickness during aging, y_0 is the initial thickness of intermetallic compounds, k is the coefficient standing for the square root of the diffusivity at aging temperature, and t is test time. The exponent value, n = ½ has been used in the above equation, which reveals a diffusion-controlled mechanism during aging. The average IMC growth measured at each level of test time has been plotted versus time. (Figure 94 to Figure 96)

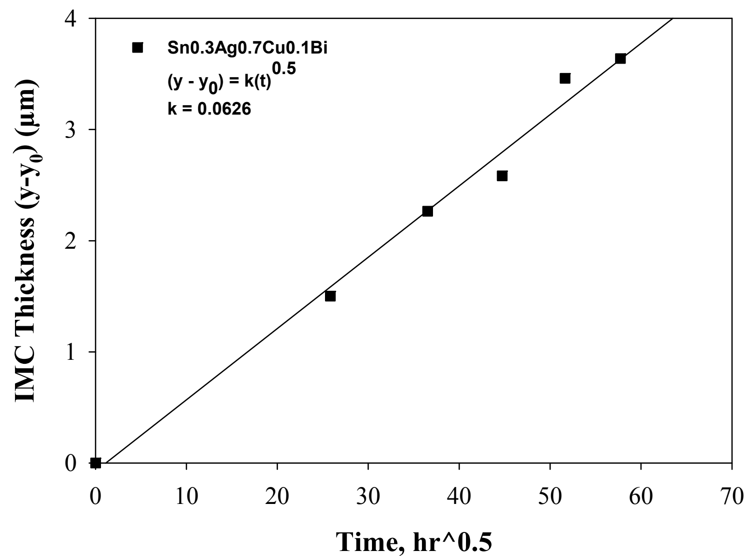


Figure 94: IMC Growth, at various levels of time for CABGA 100 with Sn0.3Ag0.7Cu0.1Bi alloy

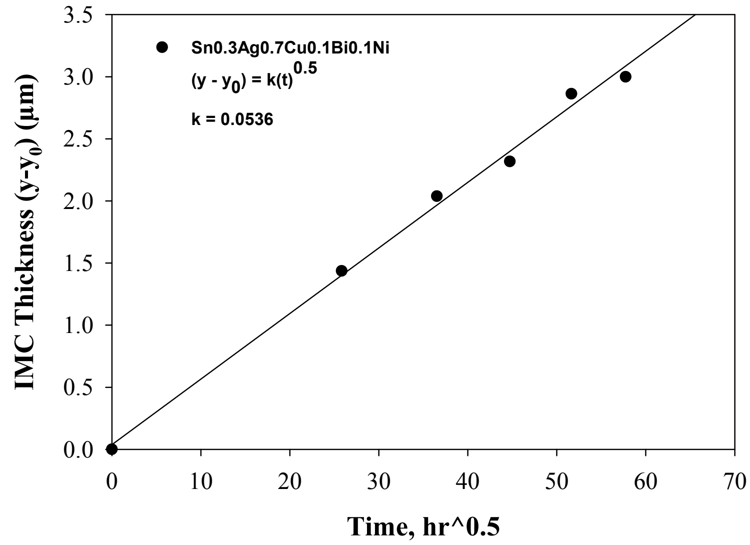


Figure 95: IMC Growth, at various levels of time for CABGA 100 Sn0.3Ag0.7Cu0.1Bi0.1Ni alloy

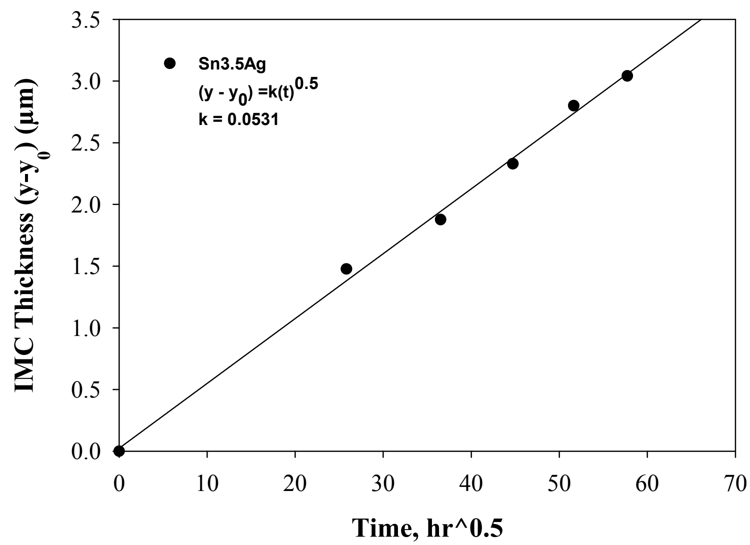


Figure 96: IMC Growth, at various levels of time for CABGA 100 with Sn3.5Ag alloy

5.10 Model Validation: Thermal Cycling

In case of thermal cycling, values of g_0, a, N, b were computed. For example from Figure 97, we can say that the error is minimum in the neighborhood of 177 cycles, indicating that prior deployed life, N = 177 cycles is the solution for CABGA 100 I/O Package with Sn0.3Ag0.7Cu0.1Bi solder interconnects. This correlates well with the actual value of 250 cycles from experimental data. This method was implemented to interrogate the system state for thermal cycling environments in the vicinity of 250 & 500 cycles respectively. Figure 97 to Figure 102 show the plots of error vs. no. of thermal cycles. Table 15 to

Table 18 show the comparison between values from experiment and algorithm

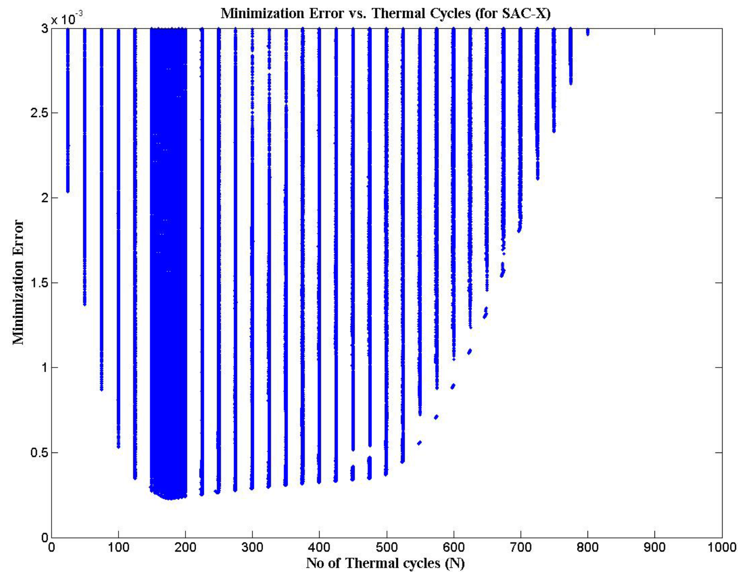


Figure 97: Plot of Error vs. No. of Thermal cycles (N) for 100 I/O CABGA Sn0.3Ag0.7Cu0.1Bi solder interconnects (Error minimum in the vicinity of 177 cycles)

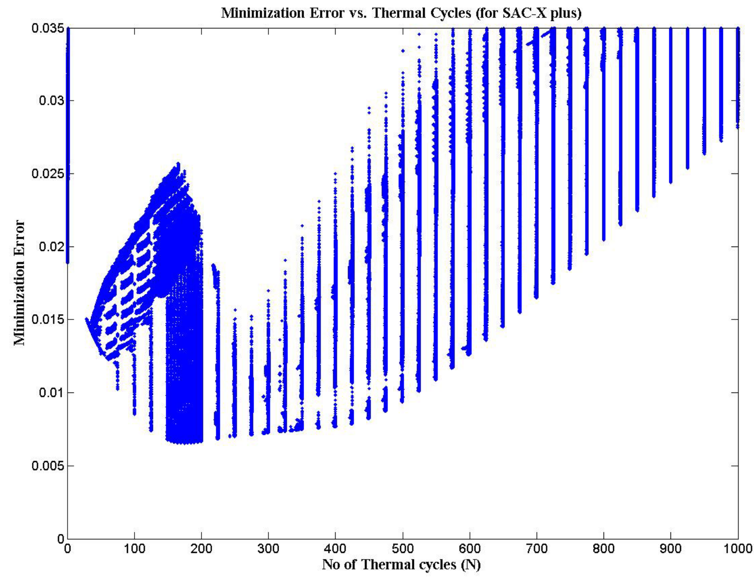


Figure 98: Plot of Error vs. No. of Thermal cycles (N) for 100 I/O CABGA Sn0.2Ag0.7Cu0.1Bi0.1Ni solder interconnects (Error minimum in the vicinity of 175 cycles)

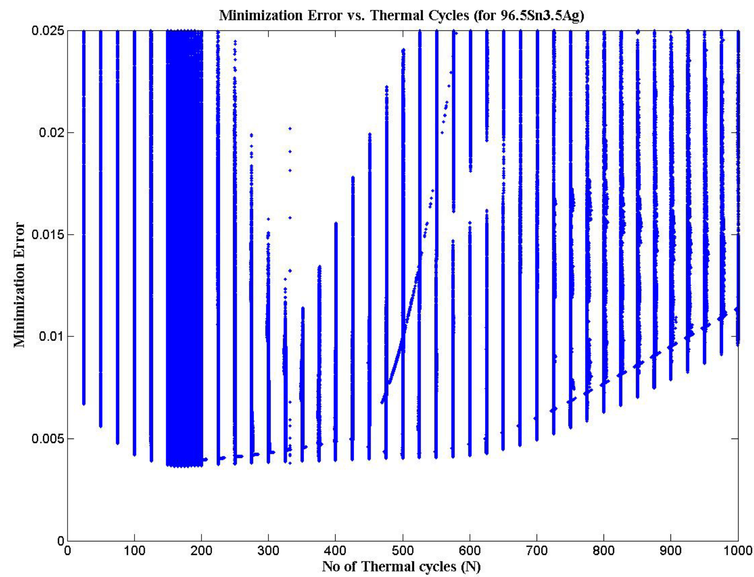


Figure 99: Plot of Error vs. No. of Thermal cycles (N) for 100 I/O CABGA 96.5Sn3.5Ag solder interconnects (Error minimum in the vicinity of 175 cycles)

Table 15: Comparison of computed values of N, g_0, from prognostication model versus experimental result.

Alloy System	Cycles 'N'		Grain Size 'g_0' (μm)	
	Expt Data	LM Algo	Expt Data	LM Algo
Sn0.3Ag0.7Cu0.1Bi	250	177	1.555	1.60
Sn0.2Ag0.7Cu0.1Bi0.1Ni	250	175	1.113	1.20
96.5Sn3.5Ag	250	175	1.429	1.50

Table 16: Comparison of computed values of a and b from Prognostication model versus experimental result.

Alloy System	Constant 'a'		Constant 'b'	
	Expt. Data	LM Algo	Expt. Data	LM Algo
Sn0.3Ag0.7Cu0.1Bi	0.00154	0.0009	1.207	1.280
Sn0.2Ag0.7Cu0.1Bi0.1Ni	0.00131	0.0007	1.240	1.330
96.5Sn3.5Ag	0.00081	0.0006	1.328	1.369

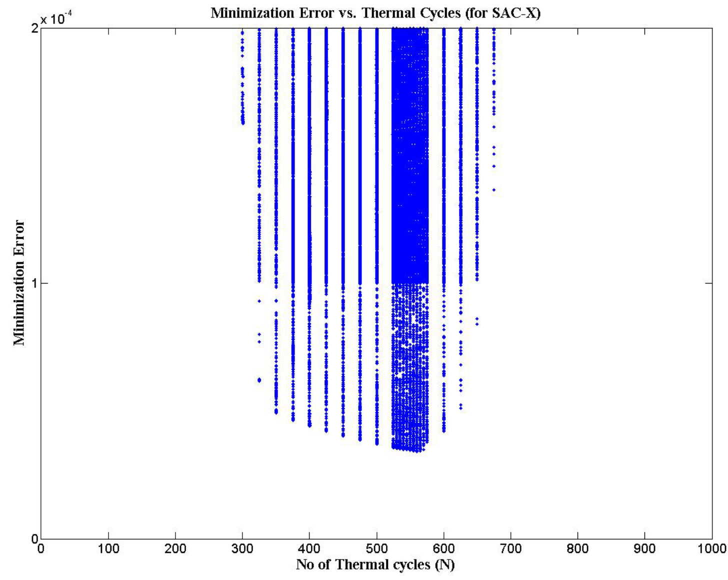


Figure 100: Plot of Minimization Error vs. No. of Thermal cycles (N) for 100 I/O CABGA Sn0.3Ag0.7Cu0.1Bi solder interconnects (Error minimum ~ 559 cycles)

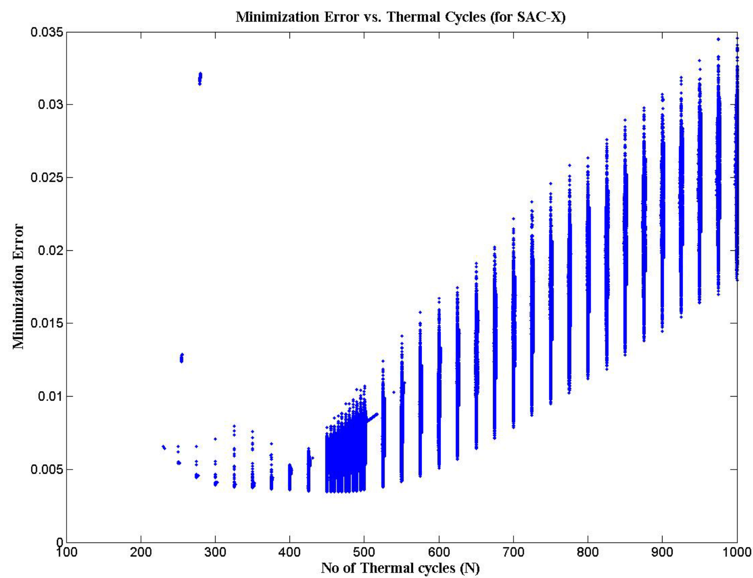


Figure 101: Plot of Minimization Error vs. No. of Thermal cycles (N) for 100 I/O CABGA Sn0.2Ag0.7Cu0.1Bi0.1Ni solder interconnects (Error minimum ~ 460 cycles)

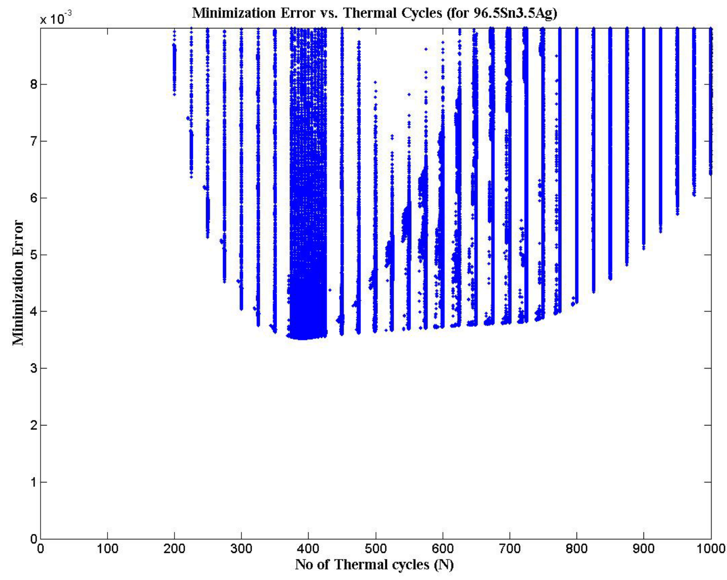


Figure 102: Plot of Minimization Error vs. No. of Thermal cycles (N) for 100 I/O CABGA 96.5Sn3.5Ag solder interconnects (Error minimum in the vicinity of 391 cycles)

Table 17: Comparison of computed values of N, g_0, from prognostication model versus experimental result.

Alloy System	Cycles 'N'		Grain Size 'g_0' (μm)	
	Expt Data	LM Algo	Expt Data	LM Algo
Sn0.3Ag0.7Cu0.1Bi	500	559	1.555	1.60
Sn0.2Ag0.7Cu0.1Bi0.1Ni	500	460	1.113	1.20
96.5Sn3.5Ag	500	391	1.429	1.50

Table 18: Comparison of computed values of a and b from Prognostication model versus experimental result.

Alloy System	Constant 'a'		Constant 'b'	
	Expt Data	LM Algo	Expt Data	LM Algo
Sn0.3Ag0.7Cu0.1Bi	0.00154	0.0018	1.207	1.1909
Sn0.2Ag0.7Cu0.1Bi0.1Ni	0.00131	0.001	1.240	1.2980
96.5Sn3.5Ag	0.00081	0.00064	1.328	1.3700

Based on the values computed from algorithm, it is possible to predict the phase size at different intervals of time. Figure 103 to Figure 105 show the comparison between the predicted versus the experimental values of phase size. The experimental data and model show good correlation.

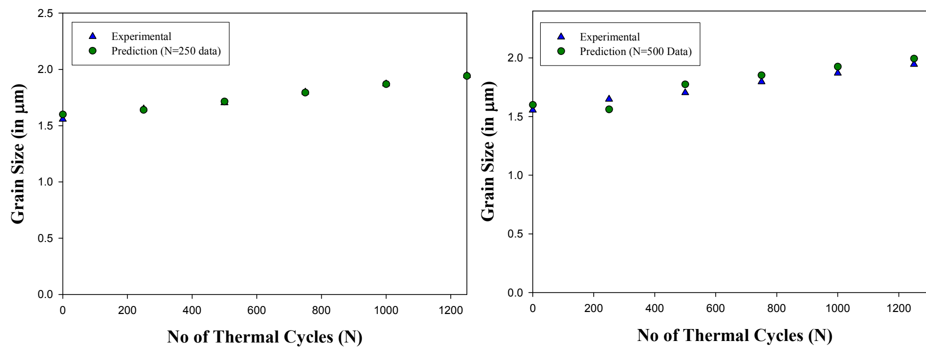


Figure 103: Prognostication of grain size from algorithm (based on g_0, a and b) vs. grain size from experimental values Sn0.3Ag0.7Cu0.1Bi alloy

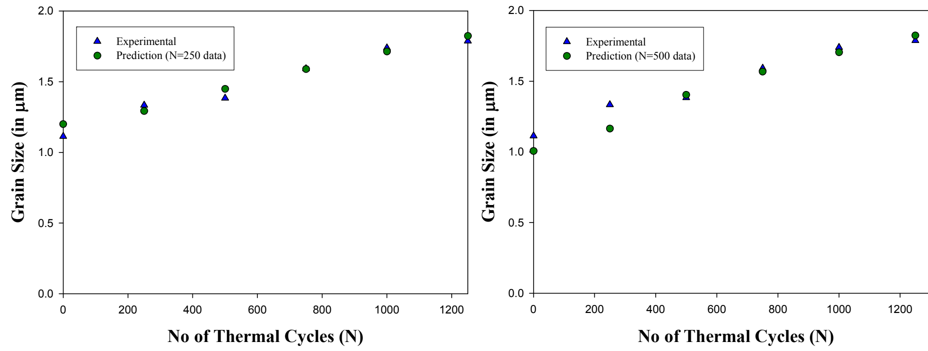


Figure 104: Prognostication of grain size from algorithm (based on g_0, a and b) vs. grain size from experimental values Sn0.2Ag0.7Cu0.1Bi0.1Ni alloy

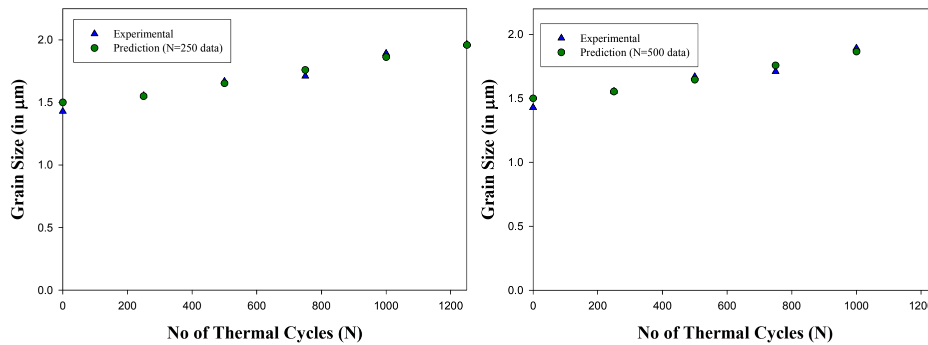


Figure 105: Prognostication of grain size from algorithm (based on g_0, a and b) vs. grain size from experimental values 96.5Sn3.5Ag alloy

5.11 Model Validation: Isothermal Aging

In case of thermal aging, values of y_0, k, *t* have been computed. For example from Figure 106, we can say that the error is minimum in the neighborhood of 830 hrs cycles, indicating that prior deployed life, N = 830 hrs is the solution for CABGA 100 I/O Package with SAC 105 solder interconnects. This correlates well with the actual value of 667 hrs from experimental data. Figure 106 to Figure 111 show the plots of minimization error vs. aging duration.

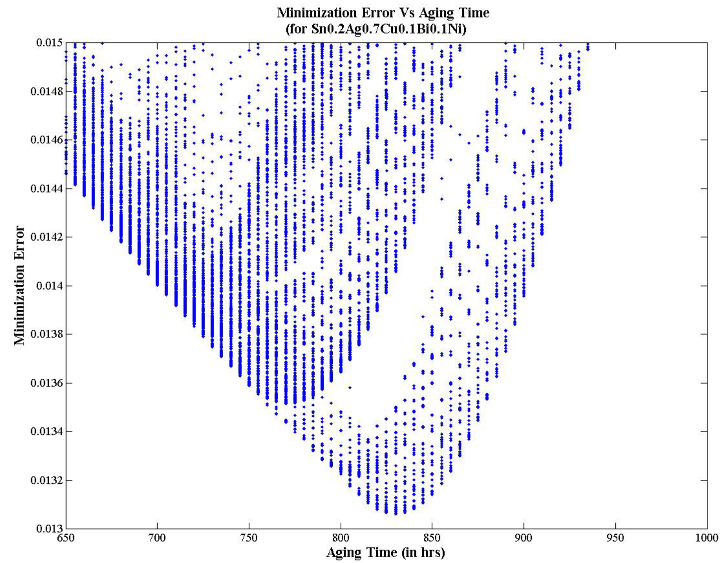


Figure 106: Global Minima for IMC based History Calculation for 100 I/O CABGA, Sn0.3Ag0.7Cu0.1Bi Solder Alloy Interconnects (Error minimum in the vicinity of 830 hrs)

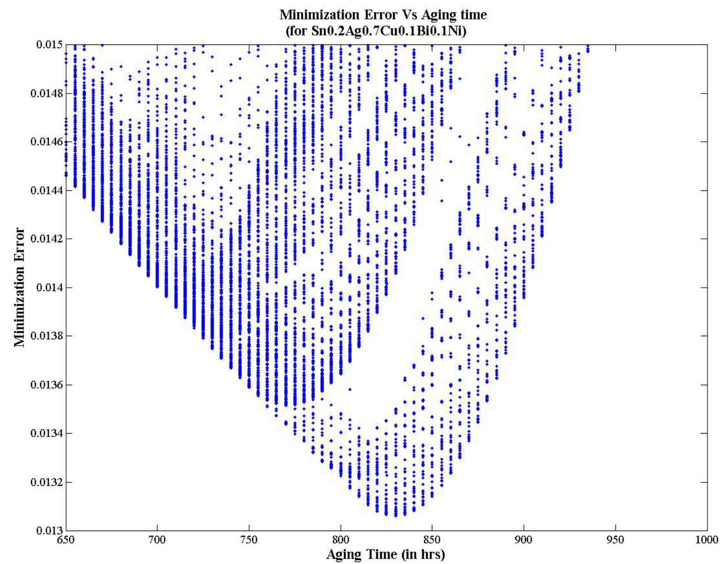


Figure 107: Global Minima for IMC based History Calculation for 100 I/O CABGA, Sn0.2Ag0.7Cu0.1Bi0.1Ni Solder Alloy Interconnects (Error minimum in the vicinity of 830 hrs)

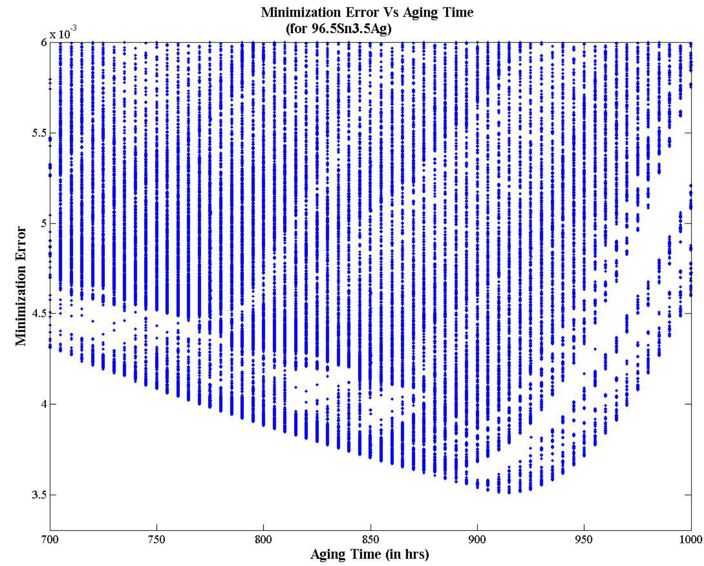


Figure 108: Global Minima for IMC based History Calculation for 100 I/O CABGA, Sn3.5Ag Solder Alloy Interconnects. (Error minimum in the vicinity of 914 hrs)

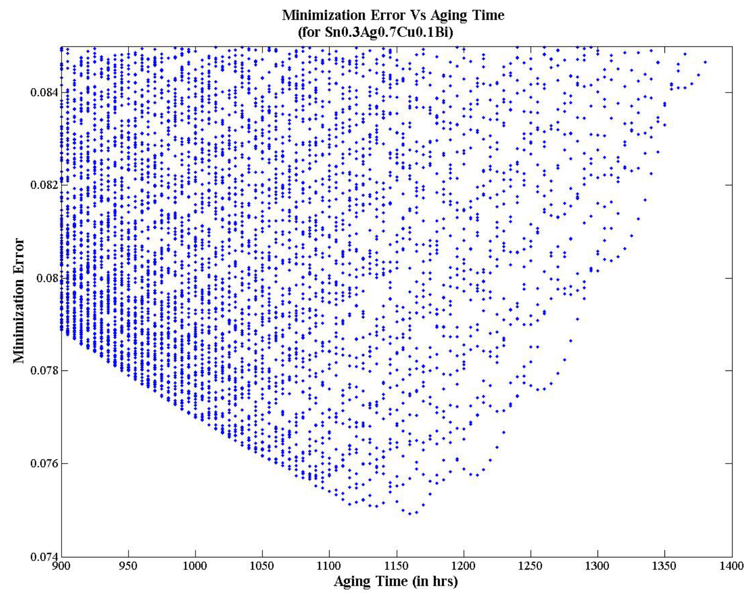


Figure 109: Global Minima for IMC based History Calculation for 100 I/O CABGA, Sn0.3Ag0.7Cu0.1Bi Solder Alloy Interconnects (Error minimum in the vicinity of 1160 hrs).

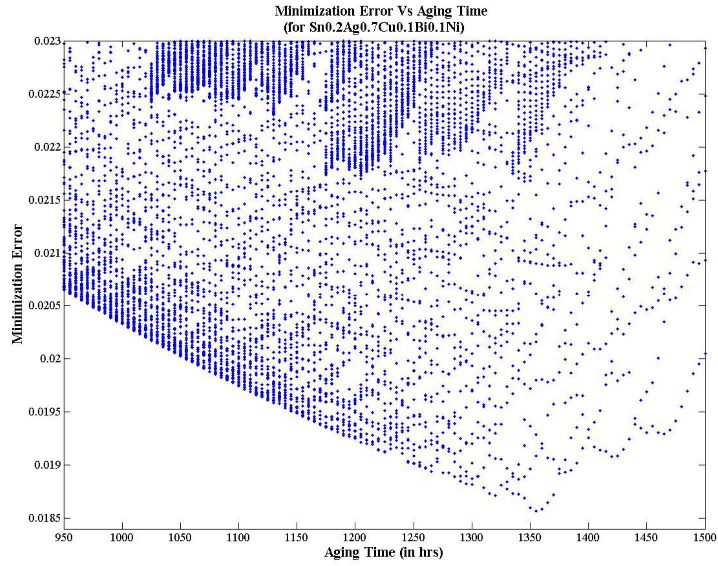


Figure 110: Global Minima for IMC based History Calculation for 100 I/O CABGA, Sn0.2Ag0.7Cu0.1Bi0.1Ni solder Alloy Interconnects. (Error minimum in the vicinity of 1355 hrs).

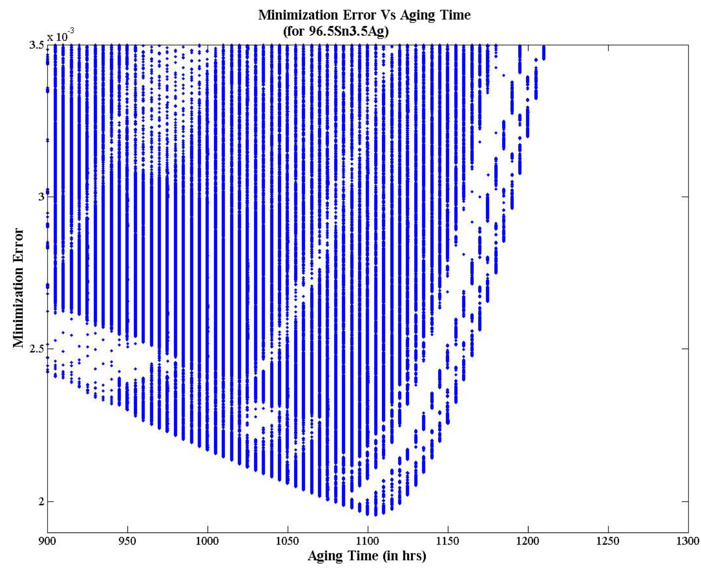


Figure 111: Global Minima for IMC based History Calculation for 100 I/O CABGA, Sn3.5Ag Solder Alloy Interconnects (Error minimum in the vicinity of 1150 hrs).

Computed values of y_0, k, t have been compared with the experimentally measured values for prognostication of 666 hrs (Table 19) and 1334 hrs (Table 20).

Table 19: Comparison of computed values of t, y_0 from prognostication model and experimental result.

Alloy System	Aging Time 't' (hrs)		Grain Size 'y_0' (μm)	
	Expt Data	LM Algo	Expt Data	LM Algo
Sn0.3Ag0.7Cu0.1Bi	667	830	3.93498	3.6610
Sn0.2Ag0.7Cu0.1Bi0.1Ni	667	829.9	3.912	3.912
Sn3.5AG	667	914.9	6.123	6.1

Table 20: Comparison of computed values of t, y_0 from prognostication model and experimental result

Alloy System	Aging Time 't' (hrs)		Grain Size 'y_0' (μm)	
	Expt Data	LM Algo	Expt Data	LM Algo
Sn0.3Ag0.7Cu0.1Bi	1333	1160	3.93498	3.6610
Sn0.2Ag0.7Cu0.1Bi0.1Ni	1333	1355	3.912	3.912
Sn3.5Ag	1333	1150	6.123	6.10

Based on the values computed from algorithm, it is possible to predict the IMC at different intervals of time. Figure 112 to Figure 114 show the comparison between the predicted versus the experimental values of phase size. The experimental data and model show good correlation.

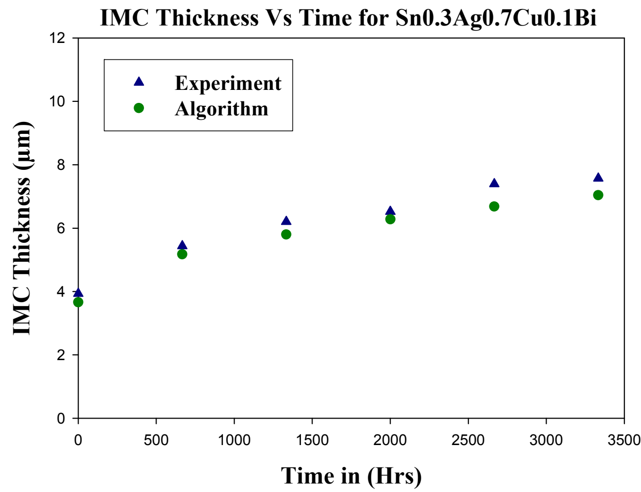


Figure 112: Prognostication of grain size from algorithm (based on g0, a and b) vs. grain size from experimental values Sn0.3Ag0.7Cu0.1Bi alloy

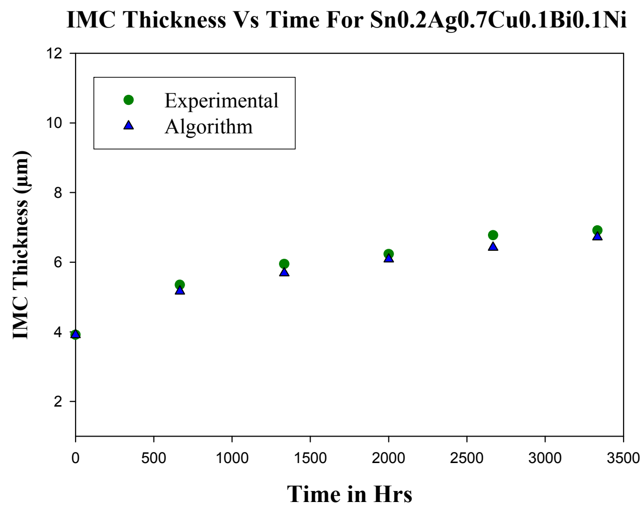


Figure 113: Prognostication of grain size from algorithm (based on g_0, a and b) vs. grain size from experimental values Sn0.2Ag0.7Cu0.1Bi0.1Ni alloy

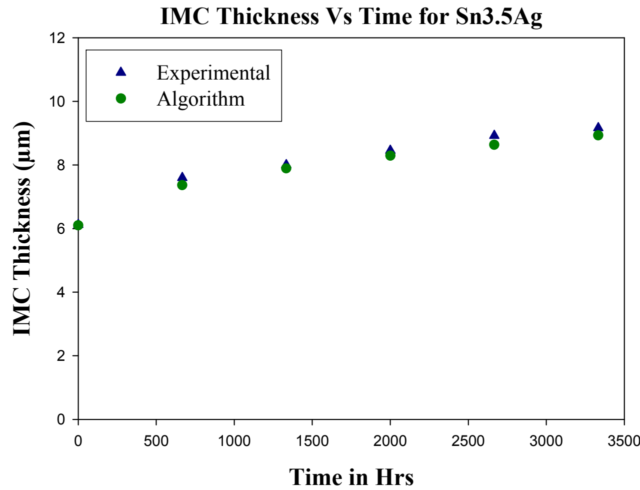


Figure 114: Prognostication of grain size from algorithm (based on g_0, a and b) vs. grain size from experimental values 96.5Sn3.5Ag alloy

5.12 Implementation Of PHM Technique

The PHM technique presented in the study may be implemented using condition monitoring devices, which can be cross-sectioned to interrogate the system state and determine the failure progression of the assembly. Consider an electronic assembly which has been deployed in the field application. The assembly needs to be redeployed in the same environment.

The condition monitoring devices in the system will then, be withdrawn at periodic intervals in the deployed environment. The condition monitoring devices will be cross-sectioned and their grain size data will be extracted. This data will be analyzed using Levenberg's-Marquardt Algorithm and methodologies discussed earlier, to find out the initial grain size (g_0) and the prior time of deployment (N, or t) for which the component has been deployed. The rate of change of phase growth parameter, (dS/dN), will be computed using the computed values of damage proxies or leading indicators-of-

failure. The rate of change of phase growth parameter (dS/dN) can be correlated to time-to-1%-failure [Lall 2004, 2005, 2006]. Residual Life (RL) can be calculated using the equation, $RL = N_{1\%} - N$.

5.13 Summary and Conclusions

A methodology has been presented to calculate the prior damage in electronics subjected to cyclic and isothermal thermo-mechanical loads. The time duration for which the component has been deployed and initial grain size is been estimated using Levenberg-Marquardt Algorithm with Trust Regions. Methodology has been demonstrated using various leading-indicators of failure including, phase growth and intermetallic thickness. The presented approach uses non-linear least-squares based method of estimating prior stress history, and residual life, by interrogating system-state prior to redeployment. The prior stress histories have been calculated for both cyclic thermo-mechanical loads and isothermal loads. Computed results have been correlated with the experimental data for various aging times and thermal cycles for several packaging architectures. The correlations indicate that the leading indicators based PHM technique can be used to interrogate the system state and thus estimate the Residual-Life of a component. The presented approach of computing residual life can be implemented prior to appearance of any macro-indicators of damage like crack. Methodology presented using condition monitoring components to find out the residual life is promising because these components experience the same environment as actual component.

CHAPTER 6
SUMMARY AND FUTURE WORK

6.1 D-PACK: Thermo-Mechanical Reliability

The thermo-mechanical reliability of a new architecture (D-Pack^{TM}) has been evaluated using finite element models. Slice models were created for different configurations (Partial Interposer, Full Interposer), solders (eutectic Sn-Pb, SAC) in ANSYS and subjected to two thermal cycles from 0ºC to 100ºC (20 min dwell / ramps). The reliability was assessed from the point of view of fatigue in solder joints as well as capacitor dielectric cracking.

Volumetrically averaged visco-plastic strain energy density (across a layer of critical elements) was used as a metric to calculate the damage in solder joints due to cyclic temperature loading. Based on empirical relations for life prediction available in literature, cycles to failure was calculated using the energy approach and the predictions were compared with experimental data. The predictions based on finite element methodology have been validated with experimental data.

The maximum principal stress generated in the dielectric was also observed during the simulation. Based on the S-N curves available from fatigue testing for $BaTiO_3$ (dielectric in D-Pack), it was concluded that the stresses generated in D-Pack were well within safety limits to last for more than 10^5 cycles.

On account of relatively small joint height, it was expected that most of the damage would be accommodated by the D-pack joints, which is in line with the finite element predictions, as well as failure analysis of tested assemblies. Based on the examination of hysteresis loop plots (for D-Pack solder joints) from finite element, it can be concluded that partial configuration with SAC solder would perform better than other configurations tested. In order to enhance the thermal reliability it would be worthwhile to explore the effect of increasing the solder joint thickness.

Also, the partial interposer configuration tested during this study was assembled without any joints at the outer periphery. Since it would be reasonable to assume that the intended field application would certainly involve usage of periphery I/Os, it would be interesting to experimentally test assemblies with tall solder joints (for interconnections), and to explore if there is any reliability improvement / degradation over the partial interposer configuration (without any periphery joints).

6.2 Prognostics and Health Management Implementation

A damage pre cursors based methodology for prognostication-of-electronics including assessment of residual-life, has been developed and demonstrated under single stresses of thermal cycling and steady-state temperature. The damage pre-cursors enable assessment of system damage-state significantly prior to appearance of any macro-indicators of damage. Phase growth rate and interfacial intermetallic layers growth rate have been identified as valid proxies for determination of residual life in electronic structures. The theoretical basis for the selection of prognostic parameters has been justified based on particle growth induced by volume diffusion. Mathematical relationships have been developed between phase growth, derivatives of phase growth,

intermetallic growth for interrogation of residual life and damage state. A methodology has been presented to calculate the prior damage in electronics subjected to cyclic and isothermal thermo-mechanical loads.

Components analyzed include various packaging architectures including, plastic ball-grid arrays, chip-array ball-grid arrays, tape-array ball-grid arrays, flex-substrate ball-grid arrays with different pad morphologies, assembled with four different lead-free solder alloys (SAC 405, SnAgCuBi, SnAgCuBiNi, Sn3.5Ag). Packages have been subjected to known levels of thermo-mechanical loads, withdrawn at discrete time intervals and have been cross-sectioned, polished and viewed under a Scanning Electron Microscope. The evolution of damage has been characterized using leading indicators of failure like phase growth and inter-metallic coarsening.

A separate test matrix has been used to interrogate the system state and validate the proposed methodology. The time duration for which the component has been deployed and initial grain size is been estimated using Levenberg-Marquardt Algorithm with trust regions. The presented approach uses non-linear least-squares based method of estimating prior stress history, and residual life, by interrogating system-state prior to redeployment. The prior stress histories have been calculated for both cyclic thermo-mechanical loads and isothermal loads. Computed results have been correlated with the experimental data for various aging times and thermal cycles for several packaging architectures. A framework for implementation of the prognostication approach has been discussed including, sacrificial devices, which can be examined to determine the damage state of the assembly from time to time. The correlations indicate that the leading indicators based PHM technique can be used to interrogate the system state and thus

estimate the Residual-Life of a component. The presented approach of computing residual life can be implemented prior to appearance of any macro-indicators of damage like crack. Methodology presented using condition monitoring components to find out the residual life is promising because these components experience the same environment as actual component.

6.3 Future Work

It is known that high temperature storage of a component prior to field deployment leads to reduction in cyclic life. It would be insightful to conduct an experimental test to quantify the amount of reliability degradation on account of high temperature storage (isothermal aging).

One approach would be to assemble about 15 test boards (each board populated with 15 devices) and to subject them to sequential stress environments (say Treatment I and Treatment II). For example, a test board will be initially subjected to isothermal aging at a given temperature (say 125 °C) and then subjected to thermal cycling (-40°C to 125°C) and failure distribution data be recorded. Table 21 shows a proposed test matrix.

Singh [2006] has developed multivariate regression based models for life prediction of BGA packages. The input data for model building was collected from published literature and accelerated test reliability database based on the harsh environment testing of BGA packages by the researchers at the NSF Center for Advanced Vehicle Electronics (CAVE). The general form of the equation used in this study is

$$N_{1\%} = f \left\{ \begin{array}{l} \text{Die size, die to body ratio, ball count, ball} \\ \text{diameter, pitch, pcb pad diameter, solder mask} \\ \text{definition, pcb finish, encapsulant mold} \\ \text{compound filler content and deltaT} \end{array} \right\}$$

Table 21 : Proposed Test Matrix to quantify the effect of Sequential Stresses

Test Boards (Each Board populated with 15 packages)	**Treatment I** Aging Time (hrs) (@temp)	**Treatment II** Thermal Cycles (-40°C to 125°C)
2 (Two)	No Treatment	Till Failure
2 (Two)	100 hrs (@125 °C)	Till Failure
2 (Two)	200 hrs (@125 °C)	Till Failure
2 (Two)	400 hrs (@125 °C)	Till Failure
2 (Two)	100 hrs (@150 °C)	Till Failure
2 (Two)	200 hrs (@150 °C)	Till Failure
2 (Two)	400 hrs (@150 °C)	Till Failure

Based on the data obtained from the proposed sequential stress experiment, it would be possible to incorporate additional variables (aging temperature and duration) in the multi-variable statistical regression model to compensate for the effects of high temperature storage prior to deployment in a cyclic field environment. The proposed model would be of the form shown below.

$$N_{1\%} = f\left\{\begin{array}{l}\text{Die size, die to body ratio, ball count, ball}\\ \text{diameter, pitch, pcb pad diameter, solder mask}\\ \text{definition, pcb finish, encapsulant mold}\\ \text{compound filler content, deltaT, } \textbf{aging}\\ \textbf{temperature and aging duration}\end{array}\right\}$$

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