FLIP CHIP AND HEAT SPREADER ATTACHMENT DEVELOPMENT

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FLIP CHIP AND HEAT SPREADER ATTACHMENT DEVELOPMENT

Yuquan Li

A Dissertation

Submitted to

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FLIP CHIP AND HEAT SPREADER ATTACHMENT DEVELOPMENT

Yuquan Li

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Signature of Author

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Date of Graduation

DISSERTATION ABSTRACT

FLIP CHIP AND HEAT SPREADER ATTACHMENT DEVELOPMENT

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Flip chip packages offer many advantages over traditional wire bonding based packages. Flip chip packages have high input/output (I/O) handling capability, better electrical performance and smaller size. Proper package design, assembly materials and process integration are needed to build a reliable flip chip package. To reduce package cost, solders are typically used for flip chip interconnection, thus solder joint reliability is critical for flip chip package product application.

Part one of this dissertation was to study the impact of a small amount of Ni on lead free flip chip solder joint thermal shock reliability. Two groups of substrates were used in this study: solder (Sn/1%Ag/0.5%Cu) on pad (as reference) and Sn finished pad bumped with a Ni containing solder (Sn/1%Ag/0.5%Cu/0.05%Ni). Flip chip die bumped with SnAg eutectic solder was used for assembly on the two groups of substrates. The bumped die assembly on bumped (dome shape) substrate was successfully demonstrated. Assembled package thermal shock reliability test and failure analysis were performed. It

was found that the small amount of Ni from the bumping solder paste was concentrated at the substrate site intermetallic (IMC) layer forming $(Ni \sim 1At\%, Cu)_6 Sn_5$, but this did not impact the solder joint thermal shock reliability significantly.

Part two of this dissertation was to study metallization and indium solder based heat spreader attach for flip chip in package applications. For metallization stack selection, it is commonly believed that during soldering and the following solder joint service life time, the solder materials should not consume the underling metallization, otherwise, dewetting or severe solder joint reliability degradation will typically occur, thus a minimum thickness of a barrier metal beneath top anti-oxidization layer (Au typically) is typically used. Ti/Ni/Au flip chip die backside metallization was evaluated in our team before. The Ni layer was used as a barrier metal and the resulting indium solder joint had good reliability. In this study, Ti/Au thin film metallization without the Ni barrier was studied. It was found that the Au thin film was converted to $AuIn_2$ IMC completely during soldering and there was no IMC formation between the In and Ti, however, the indium solder attachment had significant shear and pull strength. The attachment strength was not degraded by multiple lead free reflow or thermal aging testing.

Ti/Au (2000 Å) die based heat spreader attach (24mm x 24mm Cu on 22mm x 22mm Si) showed early delamination compared with Ti/Ni/Au die based assembly after thermal shock cycle testing. The Au thin film thickness effect was further evaluated. The next round assembly with Ti/Au (3000 Å) die did not show early delamination and had similar multiple reflow, thermal aging and thermal shock cycle reliability with Ti/Ni/Au

die. The lower shear strength for Ti/Au (2000 Å) based assembly was correlated to its early failure, since during thermal shock cycle testing, the joint was in shear stress.

Part three of this dissertation was to evaluate adhesive material based heat spreader attach for medium power application. A flat heat spreader was selected for cost reduction. A thermally conductive silicone was used as the thermal interface material. Another co-cure-able non-thermally conductive silicone was applied between the substrate and the heat spreader as a mechanical reinforcement. The manufacturing process was developed and the resulting structure was subjected to sequential assembly and environmental reliability tests. There was no interfacial delamination and no significant pull strength degradation after sequential stress testing.

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CHAPTER 1 FLIP CHIP PACKAGING LITERATURE REVIEW

1.1 Introduction [1-8]

The trend in microelectronic packaging technology is toward miniaturization and high performance. This is driven by the market needs for smaller, faster and higher functionality electronics products, such as hand held cell phones and digital cameras.

Flip chip is a packaging interconnection technology, which can improve electronics package performance and reduce package size. In this technology, the whole die surface area can be used to populate or redistribute chip input and output (I/O) connections. To be able to use this technology, the die metal contact I/O pads must be bumped. The bumps serve as electrical, mechanical and thermal interconnection media between the die and substrate. The bumps are small in size. 50 to 100 μm diameter bumps are common. The bumps can be made with gold studs, electrical conductive adhesives, but most commonly, flip chip die are bumped with low cost solders.

During the flip chip bonding process, the semiconductor die is "flipped" with its active side facing down toward the substrate. For solder bumped flip chip, reflow soldering is used to make interconnections between bumps and substrate pads, during which the solder bumps melt, wet and react with substrate pads to form metallurgy joints with the help of flux. Typically, for flip chip assembly on organic substrates, after chip attach and soldering, epoxy underfill material is used to fill the gap between the die and

the substrate to enhance the solder interconnection thermomechanical reliability (Figure 1.1).

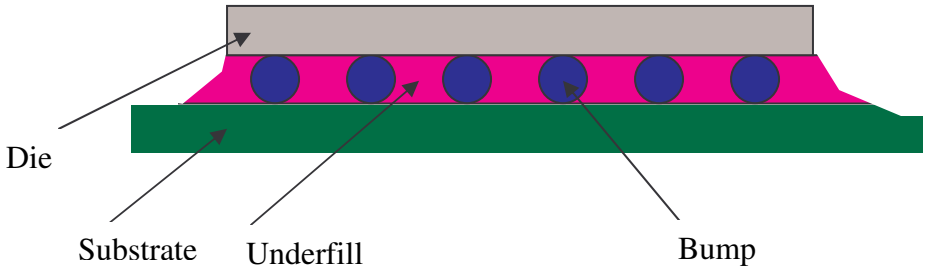


Figure 1.1. Flip chip package schematic.

Flip chip bonding was first introduced by IBM in 1964. It was called controlled collapse chip connection (C4) by IBM, in which the flow of the solder bump during soldering is controlled by the die solder bump volume, area of the solder wettable pad on the substrate, the die weight and the solder surface tension. Compared with wire bonding interconnection, flip chip offers many advantages:

- Flip chip allows designers to use the entire die surface for signal, power and ground pads to accommodate large number of interconnections required by high complexity electronics.
- Flip chip bonding has a shorter interconnection distance and smaller electrical inductance and capacitance. This is ideal for high speed electronics applications, such as networking and communication electronics.
- Flip chip assembly is a mass reflow process, in which all the bumps on the die are joined to the corresponding substrate pads simultaneously in one reflow process.

Flip chip technology has been widely used in high speed network switching electronics, disk drive electronics, cell phones, digital watches, calculators and the application of flip chip is growing very fast in industry (Table 1.1).

Total Flip Chip Demand (in Million Units)					
	2004	2005	2006	2007	2008
Flip Chip in Package	1,763	2,578	3,993	6,147	8,079
Flip Chip on Board	4,053	4,323	5,077	6,200	7,271
Total	5,816	6,901	9,069	12,347	15,350

Table 1.1. Current flip chip consumption and forecasts [3].

1.2 Under Bump Metallization and Die Bumping

For low cost flip chip application, solders are the bumping materials most commonly used. Most integrated circuits (IC) have their final contact pads made with aluminum or copper. To increase flip chip bump interconnection reliability, interface multilayer metallic materials called under bump metallization (UBM) are applied between the die pad and solder bump. The UBM should have the following characteristics [1]:

- Effective solder diffusion barrier.
- Solder wettable top layer/layers.
- Good adhesion to IC final pads.
- Good adhesion to die passivation.

- Low electrical resistance.

Thin film deposition, electroless plating, photolithography and etching process techniques are used to fabricate the UBM stacks. The solder bump will form an intermetallic (IMC) with the UBM top wetting layer after die bumping and this IMC will continue to grow during subsequent flip chip assembly and service time. Excess IMC growth may embrittle the joint or cause solder joint dewetting. The UBM materials used and thickness of each layer need to be engineered to make sure there are no UBM and IMC related reliability issues during the chip's service life.

Currently, there are three main processes for solder bumping flip chip: solder evaporation, solder electroplating and solder paste printing followed by reflow. The E-beam solder evaporation process needs to be carried out in a vacuum chamber. It is a high cost process and can not produce eutectic tin-lead solders due to the tin and lead vapor pressure difference [5]. Electroplating is a low cost process and has the capability for ultra fine pitch bumping. The chemical bath and plating current density control are critical to get uniform solder bump height and solder alloy composition. A binary solder alloy can typically be deposited at one time, but deposition of ternary or quaternary alloys is extremely difficult. For the stencil printing solder paste and reflow bumping process, the solder composition is predetermined by the solder particles in the paste. The major process objective is to deposit uniform solder paste on each pad. This can be accomplished by proper stencil design, stencil type selection and printing process optimization. Stencil printing is cost competitive with electroplating. 150μm fine pitch flip chip solder bumping with stencil printing process has been successfully demonstrated at Auburn University [6].

1.3 The Underfill [9-19]

1.3.1 The Role of Underfill

Historically, flip chip was assembled on ceramic substrates. While there is a coefficient of thermal expansion (CTE) mismatch between the silicon die (~3ppm/ºC) and alumina ceramic (~6.5mm/ºC), which causes shear stress on the solder joint during thermal cycle, flip chip on ceramic built with small die was reliable for under-the-hood environment without the application of underfill [1].

With the die size increasing or switching the substrate to high CTE organic laminate (~17ppm/ºC), the shear stress and strain on the solder joint is increased significantly during thermal cycling, which can cause early failure of flip chip solder joints (Figure 1.2). To overcome this problem, underfill was introduced. Underfill is an adhesive material, typically made with epoxy filled with silica particles. The silica is used to reduce the underfill CTE. Low CTE is a desired underfill property. After the underfill is applied and flows into the gap between the assembled die and substrate and gets cured, the underfill will bond the die and the substrate, forming a tri-layer structure. Under thermal cycling, the tri-layer structure will tend to warp as a unit (Figure 1.3), which will reduce the relative shear deformation on the solder joint to improve solder joint reliability. Typically, with the application of underfill, the flip chip solder joint can have more than ten times longer thermal cycle life compared to no underfill [2]. Underfill can also protect flip chip interconnection from the environment, even though it is not a hermetic seal.

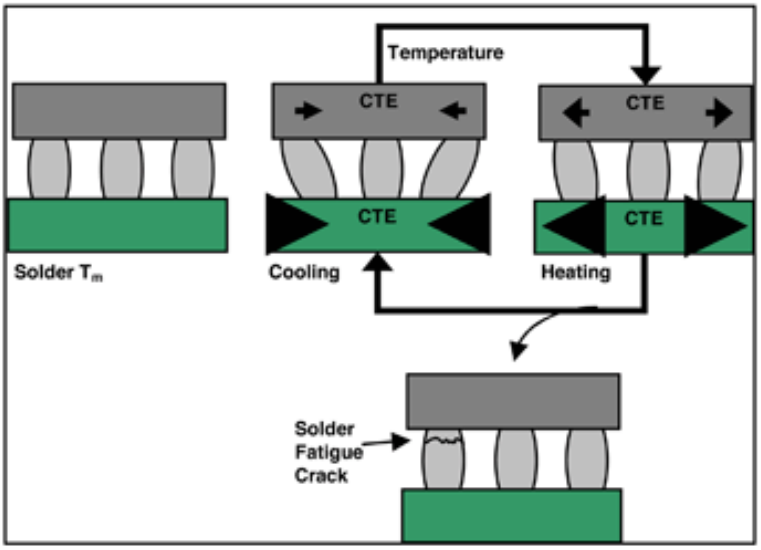


Figure 1.2. Stress on the solder joints during heating or cooling of the package [13].

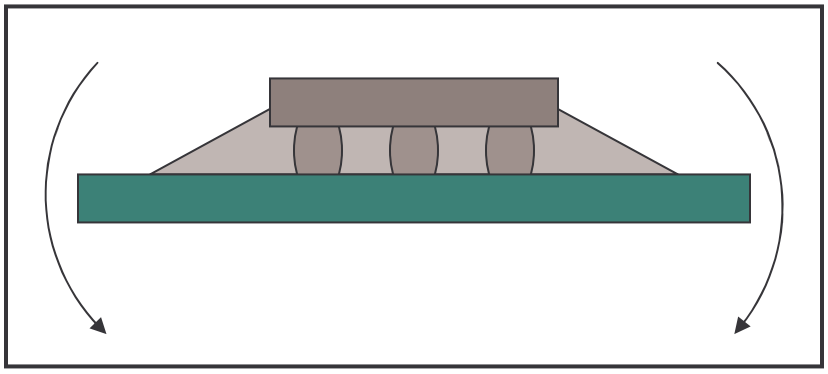


Figure 1.3. Warpage when underfilled package is cooled.

1.3.2 Underfill Selection

The performance of the underfill is highly dependent on its properties and application process quality. In general, the following underfill thermomchanical, environmental and process related properties are desired [13, 15-17].

- Higher glass transition temperature
- Low CTE
- Good dispensability and flowability

- Self fillet capability
- Short cure time
- Low moisture absorption
- Good adhesion to die and substrate surface

The above desired underfill properties are not independent. For example, once the underfill epoxy chemistry is set, lower CTE is accomplished by adding more filler particles, which will degrade the underfill's flow properties. For thin gap flip chip, underfill with small size filler particle is needed, but this will typically increase the particles' total surface area and consequently increase the underfill's viscosity.

High modulus underfill is desired for solder joint reliability, but higher modulus underfill will also stress the die significantly and may even crack the die during thermal cycle reliability testing, especially for bare die packages (package without an integrated heat sink mechanically coupled onto the die)[13]. With the trend of using fragile, low-K dielectric layers in IC backend processing to improve its electrical performance, compliant underfill may be necessary to avoid overstressing the low-k dielectric in the upper routing layers of the die.

1.4 Solder Bumped Flip Chip Assembly Process with Capillary Underfill

The solder bumped flip chip assembly process with capillary underfill includes flux application, die placement, reflow soldering, capillary underfilling and underfill curing (Figure 1.4).

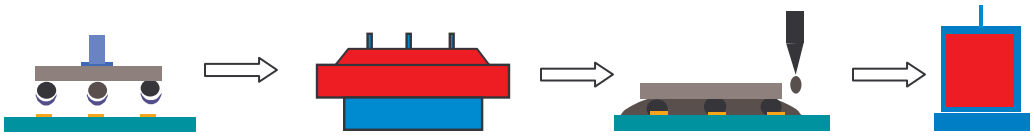


Figure 1.4. Flip chip assembly with capillary underfilling.

The first step is to transfer flux onto the solder bump. The major function of flux is to remove oxide on die bump and substrate pad surface and also to prevent the bump and pad from re-oxidization during reflow soldering, so to achieve good solder wetting. Another function of flux is to hold the die in place before solder reflow with the help of the flux tackiness. Two flux transfer methods are typically used: dip fluxing and spray fluxing. In dip fluxing, the flux is applied on the flux station inside the die pick and place machine. The die is picked up by a vacuum nozzle, inspected and aligned with the help of a look up camera, and then dipped into the flux film. The flux thickness and dip dwell time are used to control the amount of flux transferred onto the die bumps. The thickness of the flux film is controlled by the doctor blade height above the flux station. In spray fluxing, the flux, a low viscosity liquid, is sprayed on the substrate surface. Depending upon the type of solvent used in the flux, a time interval may be needed to allow the volatile solvent in the flux to evaporate before chip placement and soldering.

Chip placement with the bump 20% away from its registration center will still yield good soldering due to the nature of the molten solder during reflow (Figure 1.5).

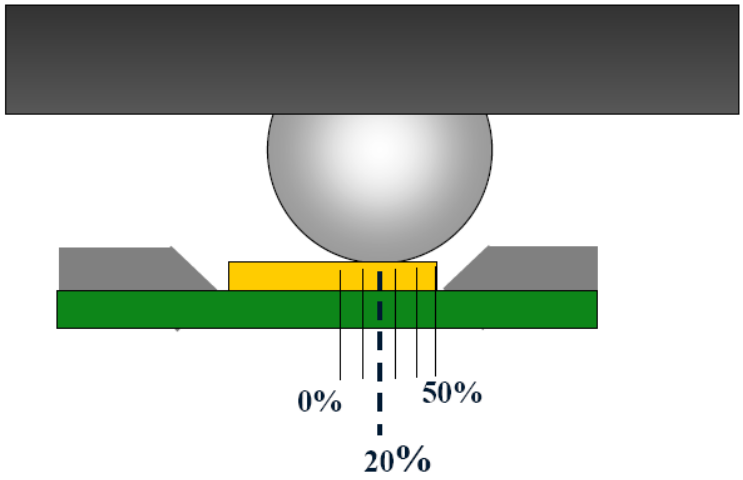


Figure 1.5. Definition of bump placement misalignment [1]

Following chip placement, the assembly is sent through the reflow oven, where the solder melts and forms a metallurgical joint with the substrate pad. The reflow temperature versus time profile is critical to ensure good solder wetting and to form a proper thickness of IMC at the joining interface. The profile should be compatible with the flux activation requirement. It typically has a low ramp rate to avoid board thermal shock and should have a relatively fast cooling rate to get a stronger solder joint. The soldering quality needs to be characterized to make sure there is no solder bridging and excellent solder wetting is accomplished.

After reflow soldering, the assembly will go to the underfilling process. For flip chip on organic substrates, a baking process may be needed before underfilling to eliminate substrate moisture, which can induce underfill voids during underfill cure. A flux residue cleaning process may also be needed depending on the flux type used. During underfilling, the underfill is dispensed near and in contact with die edge. Capillary action will pull the liquid underfill into the gap between the die and the substrate. The substrate is usually heated during the process to reduce the viscosity of the

underfill, increasing underfill flow. If the underfill does not have self-fillet capability, after the underfill fills the gap, a second dispense will be needed to form a fillet around the die edges. Typically, underfill is thermally cured with a temperature profile recommended by its manufacturer.

Schwiebert and Leong [20] presented a simplified parallel plate model and gave the following equation for estimation of underfilling time:

$$T = (3\mu L^2)/(h\gamma\cos\theta) \qquad \text{equation (1)}$$

T: capillary underfilling time

μ: absolute viscosity of the underfill

L: flowing distance

h: gap distance between the parallel plates

γ : the surface tension of the liquid-vapor interface

θ : the wetting angle of the fluid on the plate

From this equation, it can be seen that underfill with low viscosity, better wetting to the contact surfaces and high surface tension takes a shorter time to finish the underfilling process. A thinner underfilling gap and longer underfill travel distance will increase the process time.

Underfilling process quality is critical to fulfill its function after cure. The major process objectives are void free and with good fillet. Absorbed moisture in the organic substrate is a leading cause of voids in underfill after cure. That is why the substrate is typically baked before underfilling. Dispense pattern, such as dot shape, straight line or "L" shape line around two die edges is typically used to reduce the chance of forming air

entrapped voids (Figure 1.6). Underfill dispensing temperature, flux residues and any other contamination on the die and / or substrate also have a strong impact on underfill voiding.

Figure 1.6. Dot, line and "L" shape underfill dispense pattern

C-Mode scanning acoustic microscopy (CSAM), a non-destructive testing technique, is used to detect voids in underfill after cure and delamination of underfill after stress testing. In this technology, an acoustic wave is first generated by a transducer. The wave then propagates and interacts with test samples. Voids or delamination will cause strong reflection of the acoustic signal. The reflected signal is used to map an image, where voids or delamiation region will show significant contrast difference from underfill defect free locations.

1.5 Solder Bumped Flip Chip Assembly Process with Fluxing Underfill

1.5.1 Fluxing Underfill Process

From equation (1), it can be seen that for large die and small standoff gap flip chip assembly, capillary underfilling can take a long time. Capillary underfilled assembly also needs a separate curing step. This will affect the production throughput for high volume manufacturing. One solution is to use fast flow, snap cure capillary underfill. Another solution is to use fluxing underfill.

Fluxing underfill is a polymer system incorporated with a fluxing agent. In assembly with fluxing underfill (Figure 1.7), the underfill is first dispensed on the substrate pads area, and then the die is placed into the dispensed underfill. Proper placement force is needed to squeeze the underfill and make the solder bump contact its corresponding substrate pad. After placement, the assembly is sent through the reflow oven to finish reflow soldering and underfill curing at the same time. During the reflow process, the solder wetting must occur before underfill curing. Otherwise, the cured underfill will stop the die solder bump from collapsing to form a good solder joint. The major process challenges for fluxing underfilling are underfill voiding, die floating and solder non-wetting [14, 25]. Voiding has to do with substrate design, underfill dispense pattern, die placement process [25-26, 29]. A proper design of experiment is needed to minimize voiding. Too much fluxing underfill applied tends to cause die floating due to buoyancy and fillet force from the liquid underfill. It was found that the amount of underfill applied, the placement process and the reflow profile compatibility with underfill cure kinetics and with solder wetting play the key roles to accomplish a good assembly [14, 25].

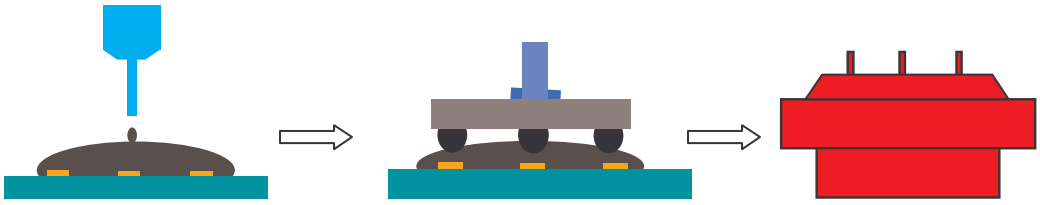


Figure 1.7. Fluxing underfill process.

1.5.2 Fluxing Underfill and Capillary Underfill Comparison

Fluxing underfill can only contain a maximum filler content of about 20% by weight, which is not sufficient to reduce its CTE significantly [30]. This limits fluxing underfill for high reliability flip chip package applications. Compared with capillary underfill, fluxing underfill typically has a high CTE and lower modulus. The following (Table 1.2) shows the comparison between the two underfill systems.

	Conventional Capillary Underfill	Fluxing Underfill
Curing Temperature	< 150 °C	Compatible with solder reflow
Curing Time	< 30 min	
Tg	> 125 °C	Usually lower
Working Life	> 16 hours	Similar
CTE	22-27 ppm/°C	60-80 ppm/°C
Modulus	8-10 GPa	2-3 GPa
Fracture Toughness	> 1.3 MPa·$m^{0.5}$	Typical lower
Moisture Absorption	< 0.25 %	Typical higher
Filler Content	< 70 wt%	None or very low

Table 1.2. Properties of typical capillary underfill and fluxing underfill [14].

1.6 Flip Chip Assembly Process with Wafer Level Applied Underfill

Capillary and fluxing underfill are applied at the individual die level. Researchers are trying to apply underfill at the wafer level to significantly improve flip chip manufacture throughput. Application of wafer level applied underfill on a surface mount production line has several challenges such as:

" 1. Development of a coating process for application of material to wafer
2. Bumping the wafer either before or after material application
3. Singulation of coated die from the wafer after material application
4. Alignment of coated die with covered or partially exposed bumps
5. Tack consideration to hold the coated die in place during reflow [32] "

The strategies for applying underfill at the wafer level can be divided into single and two layer materials systems (Figure 1.8). A single layer material system is desired for cost reduction. This single layer underfill material must also have fluxing capability. Two layer materials system contained separate underfill and fluxing layers. The fluxing layer typically contains no filler to interfere with solder wetting. The underfill coated wafer must leave a clean bump surface for die imaging during placement and for solder wetting during reflow.

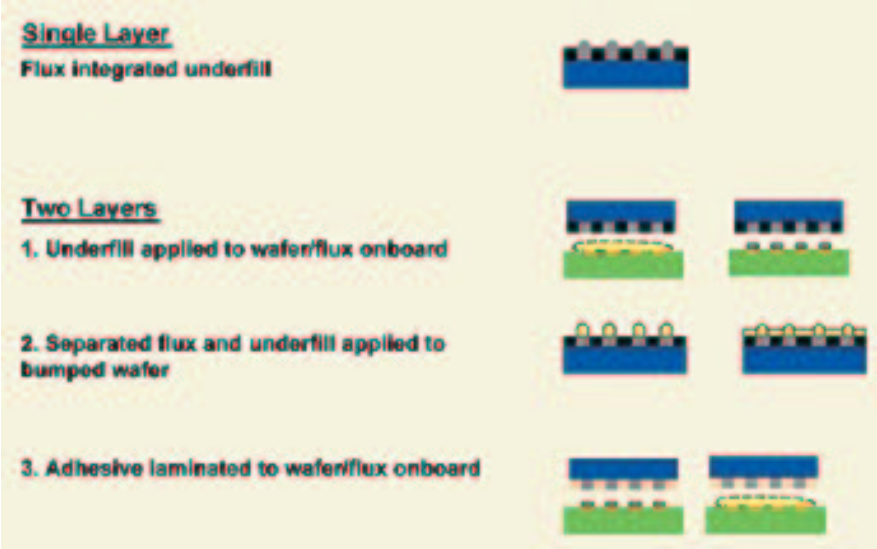


Figure 1.8. Current wafer-applied underfill approaches [32].

A two layer materials system was reported [30 and 33], in which, a stencil design and printing process were developed for coating underfill on a bumped wafer. The wafer was pre-sawn before coating to overcome the incompatibility issue with the sawing water and the underfill. The squeegee was evaluated to get uniform printing with a clean solder bump top surface. The underfill was then B-staged to create a tack free surface for handling. The fluxing layer was dispensed on the substrate pads area. Good flip chip assembly had been accomplished and the assembly had a 1% failure point at 1000 thermal cycles (-55°C to 125°C test condition).

1.7 Lead Free Soldering and its Impact on Flip Chip Assembly

Historically, Sn-Pb eutectic with a melting point of 183ºC is the major soldering material used for electronics assembly due to its low cost, excellent solderability with general surface finishes and well established reliability data through years of application.

The driving force of switching to lead free electronics comes from the fact that lead is a hazardous material to the environment and human body and there is no economical method to recycle the lead from electronics waste. Excessive lead absorption into the human body can damage the kidney, liver and nervous system [18, 35-36]. Lead was used widely in consumer electronics, which constitute about 40% of the lead found in landfills and it is possible for the lead to leach into the soil and drinking water supply system. The Waste Electrical and Electronic Equipment (WEEE) legislation in Europe mandated the elimination of lead in electronic components and subassemblies, starting July, 2006. "In the United States, the ban on lead use has not been formally proposed; however, a change has occurred in reporting the levels of lead [37]."

To convert to lead free electronics, lead free solders are being studied. In terms of manufacturability and long term reliability, there are top three performance criteria for lead free solder: [38]

1. Melting point
2. Intrinsic wettability on typical metal substrate pads/pads surface finish, such as Ni and Cu.
3. Mechanical reliability properties under cyclic strain conditions.

The International Tin Research Institute (ITRI) and the European Department of Trade and Industry (DTI) have recommended tin-silver-copper alloys as lead free solders, which are becoming the mainstream for lead free electronics assembly. The SnAgCu (SAC) eutectic (or near eutectic) alloy has a melting point of ~217°C. The alloy does not wet copper as well as tin lead using commercial flux, however, it has acceptable wetting characteristics with a properly designed flux and reflow profile. Sn-3.5Ag eutectic is also

used for lead free electronics assembly. It has a melting point of 221°C. Under a nitrogen atmosphere during reflow, Sn-3.5Ag has equivalent or superior wettability compared to tin-lead solder [37].

One significant characteristic of current lead free solder is the higher melting point compared with tin-lead eutectic. Lead free solders require peak reflow temperatures of 240-260°C, which is 30-40°C higher than the peak reflow temperature for tin-lead eutectic. New assembly materials, such as components, substrates, flux and underfill need to be redesigned and evaluated to be compatible with lead free high temperature reflow soldering (Table 1.3).

Board assembly items	Effects
Ceramic chip carriers	Little to none
Organic chip carriers	Degradation can be substantial, depends on Tg of material. Increased moisture sensitivity level (MSL).
Specials: electrolytic capacitors, wound components, etc	Susceptible to damage, typically designed for 230℃ maximum temperature, some up to 260℃.
Printed circuit board material	Standard FR4, Tg 140℃, subject to degradation. High Tg materials will survive proposed ~240℃, typically will not survive >=260℃.
Plastic overmold material	Thermal plastic may undergo shrinking or warping or cause critical features to move (creep). Thermal setting compounds, typically not affected by MSL-related effects.
Fluxes	Must be formulated to be active near and at the alloy melting point temperature. Must not create charred masses that hinder soldering, or allow surface reoxidation.

Table 1.3. Effect of higher process temperatures on various microelectronic board assembly [39].

1.8 Flip Chip Solder Joint Reliability

Solder joint reliability is critical for flip chip products. Solder is typically the weaker interconnection in the electronic packaging system. Solder joint reliability depends on packaging system design, materials selection, process quality and application environment.

1.8.1 Coffin-Manson's Solder Joint Thermal Fatigue Life Model

The flip chip solder joint is stressed during thermal cycling due to the CTE mismatch between the die and the substrate. Solder joint fatigue is the major failure mechanism. The Coffin-Manson equation gives an approximate expression for solder joint low cycle fatigue life [2].

$$N_f \text{ Proportional to } \left[\frac{h}{L(\Delta\alpha)\bullet(\Delta T)}\right]^2 \qquad \text{equation (2)}$$

Where N_f : solder joint thermal cycle life time

L : distance from chip neutral point to solder joint center point

h : solder joint standoff height

$\Delta\alpha$: CTE mismatch between the die and substrate

ΔT : temperature variation

This model says that the following actions can improve solder joint fatigue life:

- Reduce die size
- Reduce die and substrate CTE mismatch
- Increase solder joint standoff height

- Reduce temperature variation

1.8.2 Improve Solder Joint Mechanical Properties to Increase its Reliability

Besides conclusions from Coffin-Manson's model, another approach to increase solder joint reliability is to modify solder's microstructure and improve its corresponding mechanical properties.

Yoshiharu et al [40-41] did mechanical shear fatigue test on Sn-1.2%Ag-0.5%Cu-0.05%Ni flip chip solder joints. It was found that the addition of Ni can enhance low cycle fatigue endurance of low silver content SAC alloy (Figure 1.9). The low cycle fatigue endurance of Sn-1.2%Ag-0.5%Cu-0.05Ni% alloy was almost equivalent to that of Sn-3%Ag-0.5%Cu, even though the fatigue life of Sn-1%Ag-0.5%Cu is poor compared with Sn-3%Ag-0.5%Cu. Through microstructure analysis, it was found that the small Ni added to low silver SAC alloy had relatively small Sn grains, which may enhance the mechanical properties of the alloy.

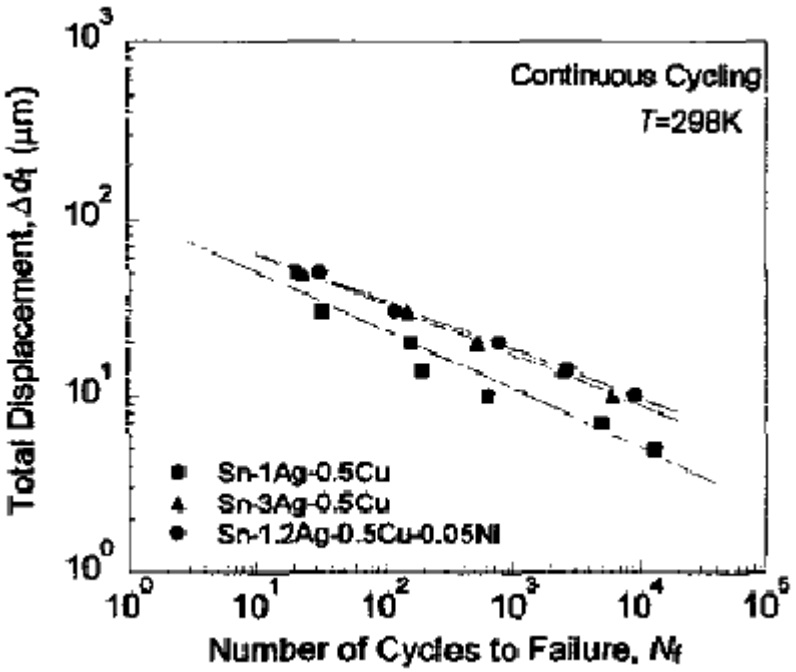


Figure 1.9. Relationship between fatigue life and applied displacement range for each flip chip joint [40].

Masamoto Tanaka et al [42] studied the drop reliability of Sn-1.2%Ag-0.5%Cu-0.05% Ni ball grid array (BGA) interconnections. It was claimed that by a small Ni addition, the drop reliability of low silver SAC solder in the BGA interconnection either on Cu-OSP or Ni/Au substrate surface finish had been improved significantly (Figure 1.10).

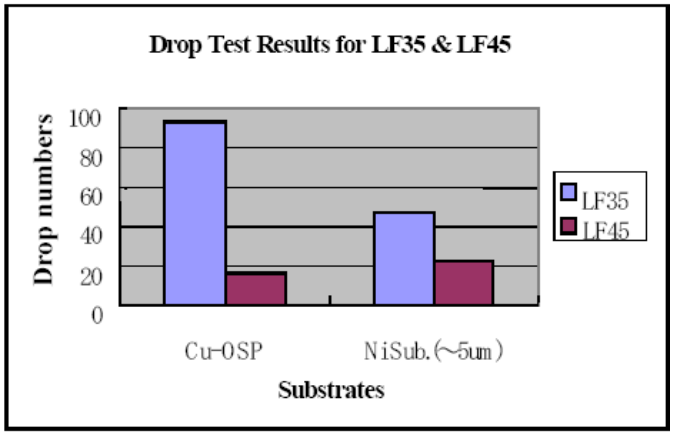


Figure 1.10. Drop shock test results for LF35 (Sn-1.2%Ag-0.5%Cu-0.05%Ni) and LF45 (Sn-3%Ag-0.5%Cu) [42].

Through solder joint microstructure analysis, it was found that the doped Ni was concentrated in the Cu_6Sn_5 IMC and influenced the intermetallic structure. The doped Ni took Cu sites in the Cu_6Sn_5 and the lattice distortions were relaxed due to the smaller atomic size of the Ni compared with Cu. The stress relief model was proposed to explain the drop reliability enhancement of BGA with Sn-1.2%Ag-0.5%Cu-0.05% Ni solder interconnection.

Shinichi et al [43-44] did flip chip solder joint thermal cycle reliability testing. They found the thermal fatigue properties of Sn-1.2%Ag-0.5%Cu solder joint was improved by addition of 0.05%Ni (Figure 1.11).

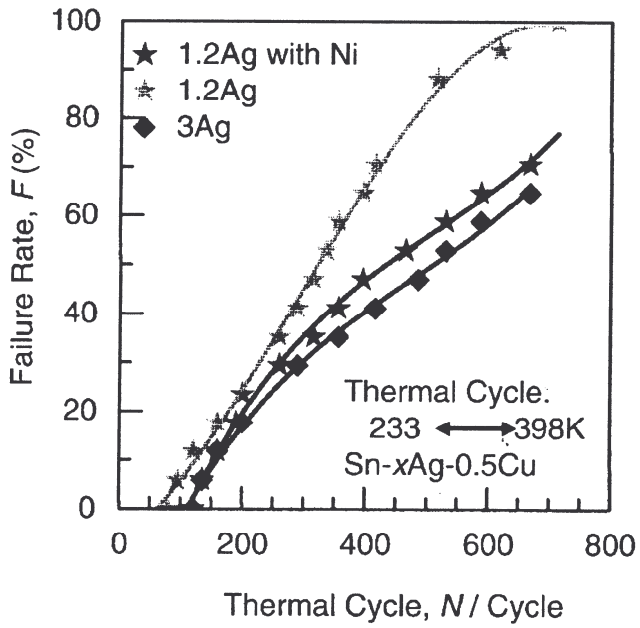


Figure 1.11. Sn-1.2%Ag-0.5%Cu-0.05%Ni and Sn-X%Ag-%0.5Cu (X=1.2 and 3) flip chip solder joint thermal fatigue rate [43].

The authors also found that fine Ag_3Sn and $(Cu,Ni)_6Sn_5$ IMC formed a network around Sn grains in the initial microstructure with Ni added to SAC low silver solder. The Sn-1.2%Ag-0.5%Cu-0.05%Ni solder joint suppressed coarsening of the Sn grains even after thermal fatigue testing. These observations were correlated with longer thermal fatigue life for Ni doped low silver SAC solder.

1.9 Flip Chip in Package Heat Spreader Attach Review

Increase in speed and functionality of high performance microprocessors and application specific integrated circuits (ASICs) results in increased I/O's and power dissipation. For example, the Figure 1.12 shows Intel's microprocessor power density road map.

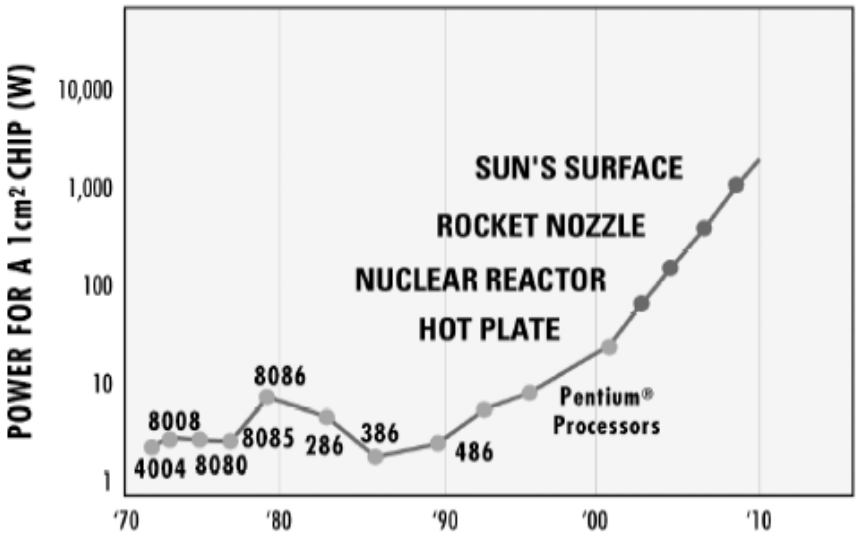


Figure 1.12. Power requirements roadmap for Intel's microprocessors [45].

The International Technology Roadmap for Semiconductors (ITRS) and the International Electronics Manufacturing initiative predicted that "the absolute power levels in microelectronic devices will continue to increase above and beyond 100W [46]."

High power devices generate more heat. If the extra heat is not removed, the device's performance and overall product thermomechanical reliability will be seriously degraded. Flip chip in package is commonly used to address the high I/O counts electronics. This packaging method exposes the backside of the semiconductor die for heat removal. A high thermal conductivity heat spreader significantly larger than the Si die is typically attached to the back of the die to serve as a large area interface to the next level cooling hardware, usually a finned heat sink (Figure 1.13).

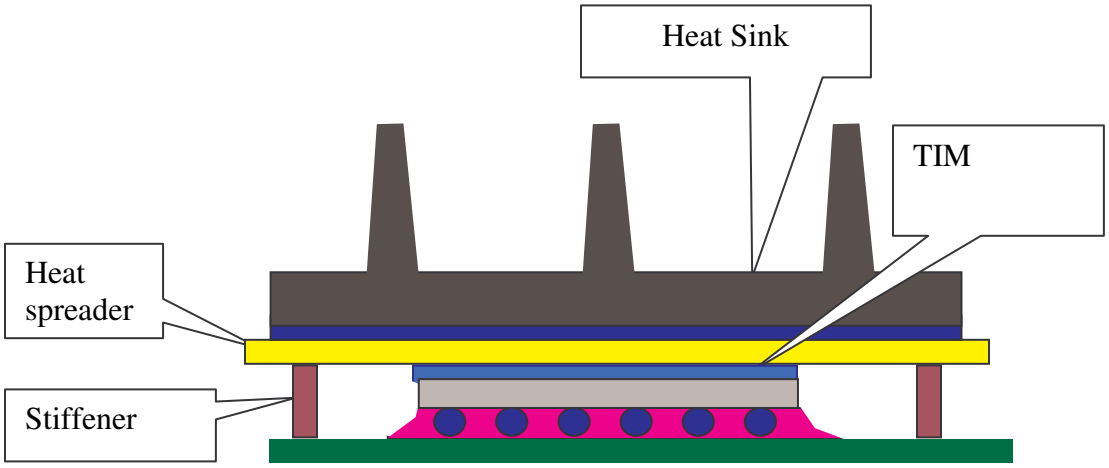


Figure 1.13. Cross section of a typical thermal management system schematic.

To help dissipate heat efficiently, the heat spreader attach system needs to have low thermal resistance, which means large attach area, high thermal conductivity heat spreader and thermal interface material (TIM) and small bond line thickness are preferred. From the attachment joint thermomechanical reliability point of view, a low CTE heat spreader is desired, since the CTE mismatch between the heat spreader (with high CTE) and the silicon die (with low CTE) will cause stress on the TIM attachment joint during temperature cycling. Compliant TIM has better capability to handle this thermomechanical stress.

Copper has often been used as the heat spreader material, since it has high thermal conductivity and low cost. The drawback is that copper has a much higher CTE compared with the silicon die. Aluminum Silicon Carbide (AlSiC) metal-matrix composite is a newly developed heat spreader material, which has a lower CTE and a reasonably high thermal conductivity [47]. The Table 1.4 shows typical heat spreader materials and their properties.

Summary of Microprocessor Heatsink-lid and Semiconductor Materials					
Materials	Average CTE(ppm/°C)	Thermal Conductivity(W/mK)	Density(g/cm^3)	Young's Modulus(Gpa)	Strength(Mpa)
AlSiC9(63vol%SiC)	7.4	200	3.01	188	488
Al	23.6	160	2.72	68	210
Cu	16.9	390	8.94	115	300
CuMo/15-85	6.6	165	10	269	655
CuW/15-85	6.8	175	16.4	225	516
GaAs	6.5	44	5.33	85.9	
Si	4.1	150	2.31	130	

Table 1.4. Heat spreader candidate materials [47]

For high power applications (>100W), indium solder has been used as a TIM [48-49], mainly because:

- It has high thermal conductivity (82W/mK).
- It is a very compliant solder material.
- It has low melting point.
- It is a lead free solder.

Table 1.5 shows the properties of typical solder TIMs.

Solder materials	Melting point (degree C)	Young' Modulus (Gpa)
Indium	156.6	11
SnPb eutectic	183	33
SnAgCu eutectic	217	46

Table 1.5. Solders TIM properties [14].

For medium power application, thermally conductive adhesives are good choices as TIM. Compliant adhesive TIM is preferred for joint thermomechnical stress handling. A silicone adhesive, filled with thermally conductive fillers was used as TIM for AMD's K6 devices [50].

1.10 Chapter Summary and Research Work Introduction

This chapter reviewed flip chip package characteristics and advantages over wire bonding based packages, flip chip bumping, assembly and underfill (capillary, fluxing and wafer level) materials and processes, lead free soldering for flip chip, flip chip solder joint reliability, recent research on Ni doped lead free solder joint reliability and flip chip in package heat spreader attach technology.

In Chapter 2, research results on the impact of a small Ni addition on the lead free solder joint microstructure and on solder joint thermal shock reliability is discussed. In Chapter 3, die backside metallizations for indium solder based heat spreader attachment were studied and the resulting heat spreader attachment reliability was characterized. Adhesives based heat spreader attachment manufacturability and reliability evaluation is documented in Chapter 4. Conclusions and recommendations for future work are presented in Chapter 5.

CHAPTER 2 LEAD FREE FLIP CHIP PACKAGING WITH A SMALL NI CONTAINING SOLDER JOINT

2.1 Introduction

A small amount of Ni added into low silver SAC solder has been claimed to impact solder joint microstructure and reliability as discussed in Chapter 1. This study was to introduce a small amount of Ni into the lead free solder joint and evaluate its impact on solder joint thermal shock reliability. This study included:

1. Introduction of a small amount of Ni into the solder joint by bumping the Sn finished substrate with Ni containing solder paste.
2. Development of the corresponding bumped die assembly on bumped substrate process.
3. Assembled flip chip in package thermal shock reliability test, failure analysis and evaluation of doped Ni impact on solder joint thermal shock reliability.

Two types of substrate finishes were used for this study: solder SAC105 (Sn/1%Ag/0.5%Cu) on pad (Cu) and Sn finished (Table 2.1). A small amount of Ni was introduced through bumping the Sn finished substrate pads with Ni containing solder paste (Sn/1%Ag/0.5%Cu/0.05%Ni). Solder (SAC105) on pad substrate (no Ni) served as

the reference for the Ni impact study. Flip chip die with the same Cu UBM and SnAg eutectic bumps was used for test vehicles assembly on the two groups of substrates.

Substrate finish	Ni status
SAC105 on pad	No Ni (served as reference)
Sn finish bumped with solder (Sn/1%Ag/0.5%Cu/0.05%Ni)	With Ni from bumping paste

Table 2.1. Substrates surface finishes and Ni containing status.

2.2 Substrate Bumping and Ni Introduction

The silicon die (7.9mm x 7.9mm) used had SnAg eutectic solder bumps. The bump pitch ranged from 190µm to 250µm and there were 642 bumps on the die. The organic substrate (23mmx23mm) had 100 µm diameter pads. The optical image of the substrate pads was shown on Figure 2.1.

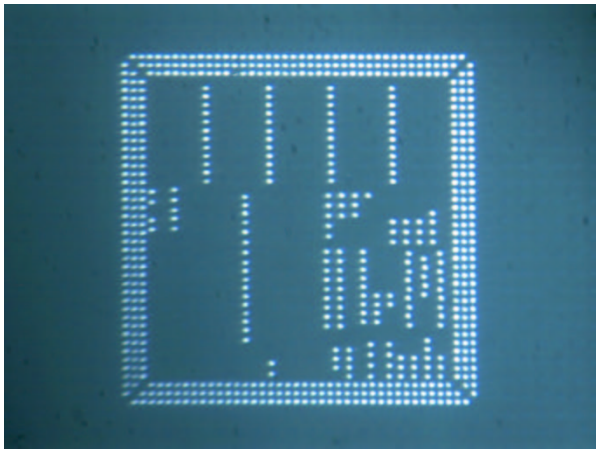


Figure 2.1. Optical image for the substrate pads.

The solder (SAC105) on pad substrate was bumped and flattened by the vendor (Figure 2.2) and there was no Ni on the substrate pad. The Sn finished substrate was bumped with Ni (0.05%) containing solder paste (Sn/1%Ag/0.5%Cu/0.05%Ni). This was a type 6 solder paste with water soluble flux and was supplied by Heraeus Corp. An electroformed Ni stencil from Photo Stencil Corp with 2mil thickness and 5 mil diameter apertures was used for solder paste printing.

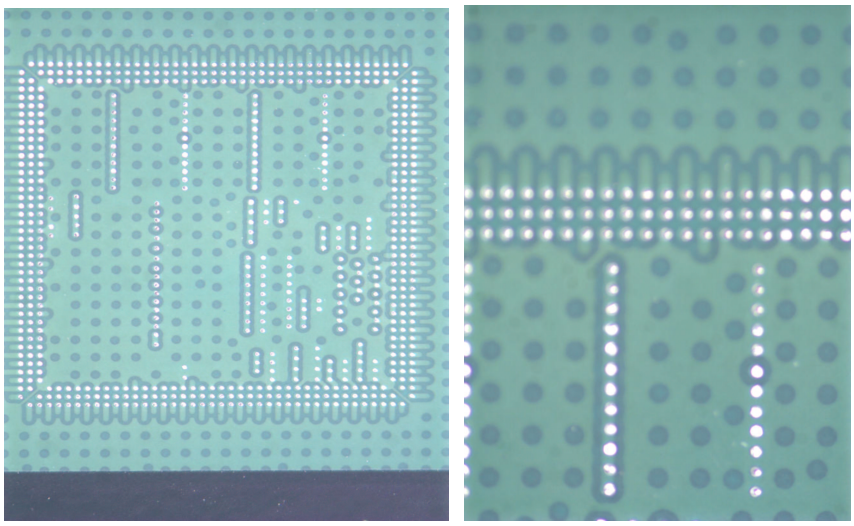


Figure 2.2. Optical image for solder on pad substrate; Right side picture is the enlarged image of the left one.

For the process, before bumping, the substrates were baked at 120°C for four hours to avoid any possible moisture induced pop corning during reflow after paste printing. The MPM stencil printer was used for the printing with a printing force of 8 pounds and a printing speed of 1 inch per second. Contact printing mode was used. After successful printing, the board was sent through reflow to form the bumps. A slow ramp rate lead free reflow profile was used with a peak temperature of 246.6 °C and time

above solder melting point of 65 seconds (Figure 2.3). The reflow process was done in an N_2 atmosphere with O_2 <60ppm to help solder wetting. The Heller reflow oven was used for the reflow process.

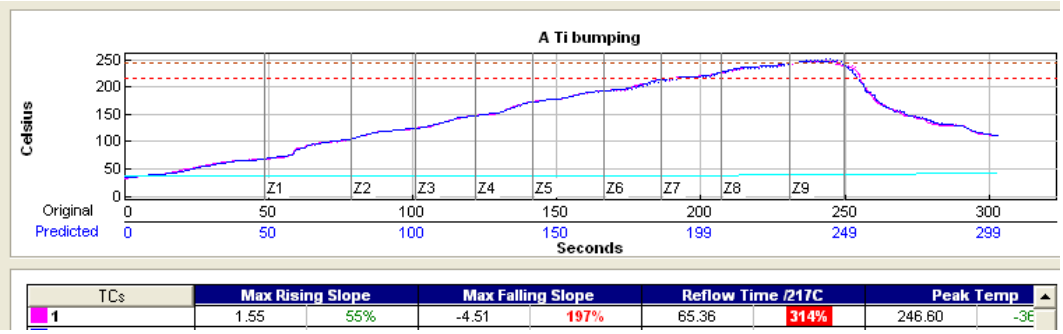


Figure 2.3. Substrate bumping reflow profile.

After reflow, the substrate was cleaned to remove the flux residue. Flux residue is corrosive and is a factor causing underfill voids during the subsequent flip chip underfilling processing. 10% concentration of HYDREX DX aqueous cleaner was used to clean the bumped substrate. HYDREX DX is "a volatile organic compound (VOC) free, high performance alkaline cleaner with exceptional wetting properties and detergency. Used in dilution, HYDREX DX is effective at removing reflowed rosin, no-clean and water soluble flux residues from circuit assemblies" [51]. The diluted HYDREX DX bath was heated and kept at approximately 66 °C during the cleaning process. The bumped substrates were soaked in the HYDREX DX bath for 15 minutes, and then transferred into a DI water bath (66 °C), soaking for 5 minutes. Following the DI water soak, the parts were rinsed with running DI water for 3 minutes and dried with a running fan. Figures 2.4 and 2.5 show the image of the bumped substrate after cleaning.

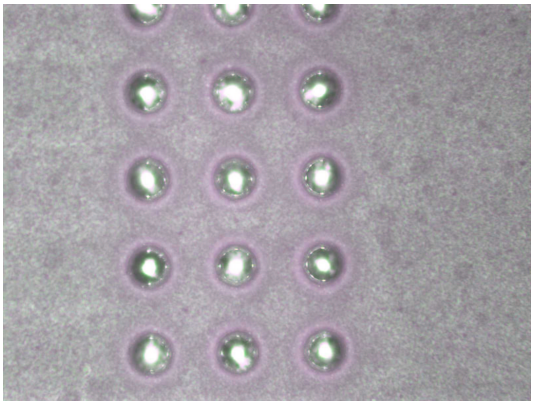


Figure 2.4. Optical image of the bumps after flux residual cleaning (close look).

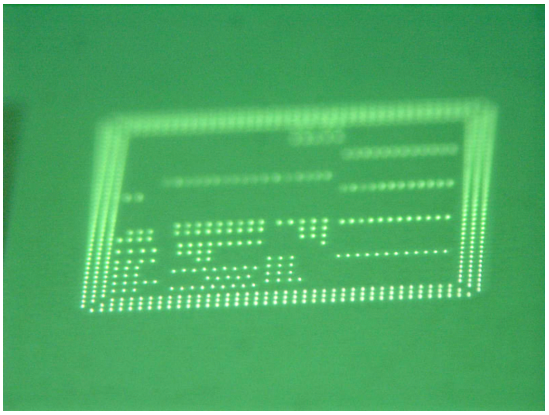


Figure 2.5. Optical image of the bumps after flux residual cleaning.

Cross section and SEM imaging techniques were used to characterize the wetting between the solder bump and substrate surface finish. Figures 2.6 and 2.7 show the uniform bulk solder bump formation and the IMC formed between the bulk solder and substrate pad.

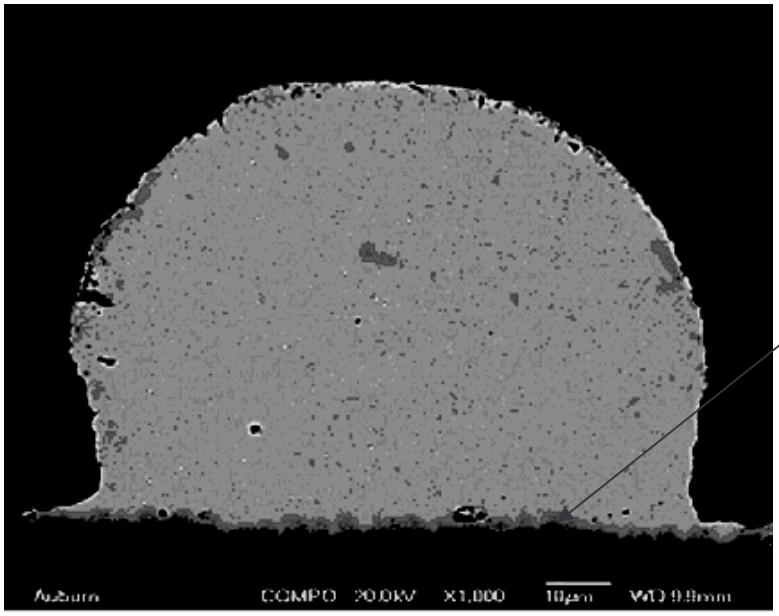


Figure 2.6. Substrate bump SEM image.

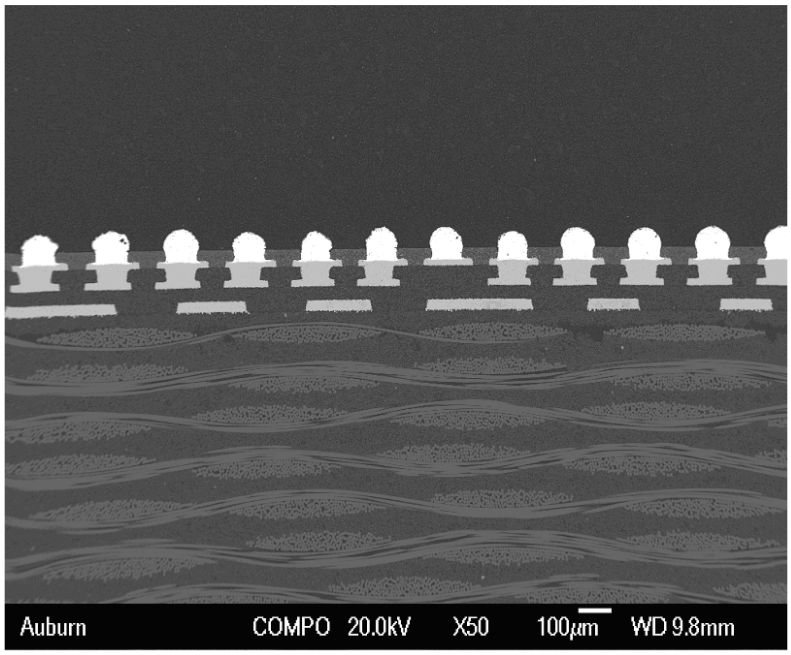


Figure 2.7. Substrate bumps SEM image.

2.3 Flip Chip Test Vehicles Assembly Process

For test chips assembly, there was no die placement issue with the solder on pad substrate, since the solder pads were flattened by the vendor and it was a normal flip chip attach process. For assembly on Sn finish with bumps substrates, there was a challenge to place and assemble bumped die on the bumped substrate as illustrated in Figure 2.8.

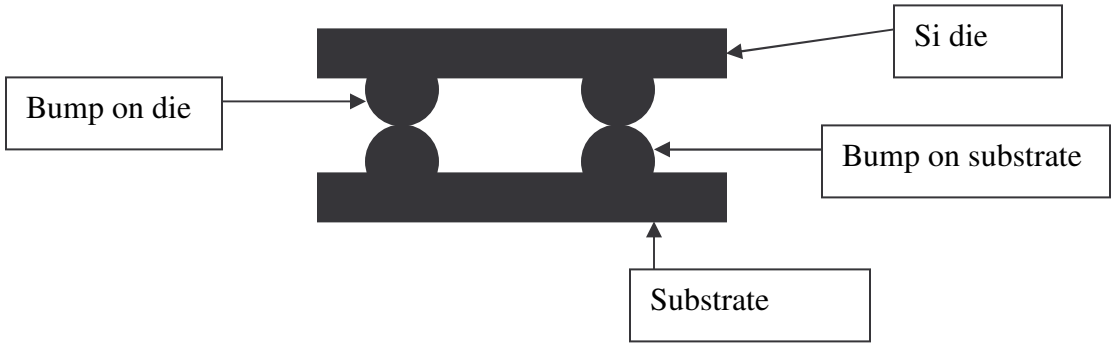


Figure 2.8. Bumped die assembly on bumped substrate schematic.

The initial plan was to develop a process to flatten the dome shaped bump on the substrates before doing normal flip chip attach. However, it was found experimentally that with the tacky flux and low placement force used, direct flip chip attach on the substrate with domed bumps was successful as documented in the following. The tacky, no clean flux, Cobar 2000BT, was used in the assembly. The flux depth was controlled to be 40~50μm. The chip placement force was 1 N. After dip fluxing and die placement, the assembly was sent through the reflow oven. The reflow profile had a peak temperature of 250°C, 54 seconds above the solder melting point, a low ramp rate to reduce the thermal gradient on the assembly and a relatively high cooling rate to get a

stronger solder joint (Figure 2.9). The reflow was done in an N_2 atmosphere with O_2 <60ppm.

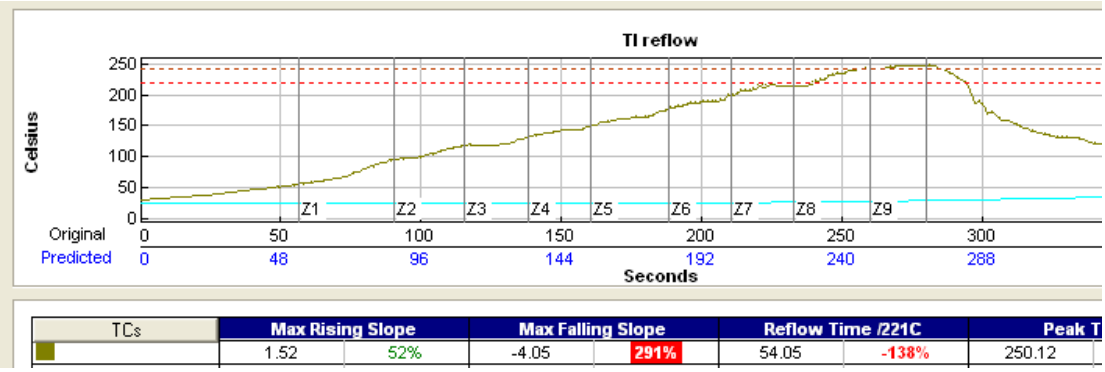


Figure 2.9. Reflow soldering profile for flip chip soldering.

X-ray images were taken right before reflow (Figure 2.10) and after reflow soldering (Figure 2.11). The images showed that the die placement on the bumped substrates had some mis-registration, but after reflow, solder surface tension self aligned the die to the substrate pads. This is similar to what is typically seen with flip chip attachment on flat pad substrates. Cross sectioning and SEM imaging showed that the solder bump on the die and on the substrate formed a good solder joint after reflow (Figure 2.12).

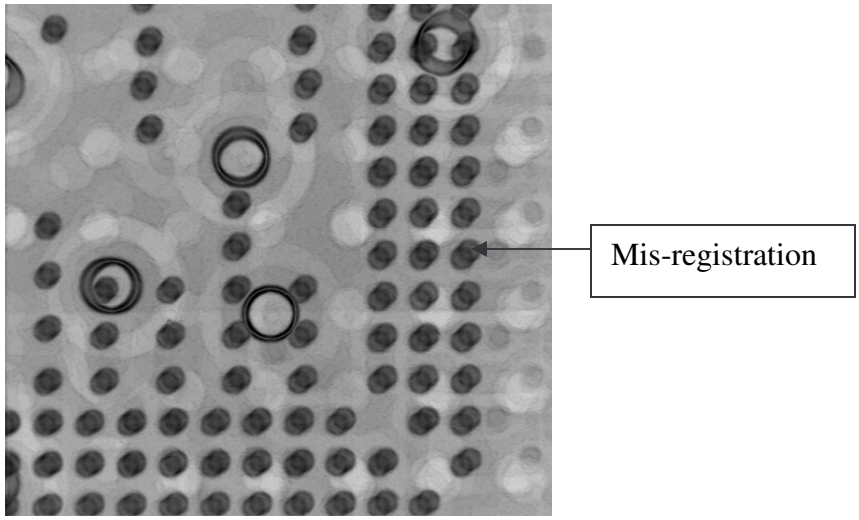


Figure 2.10. After placement and before reflow(X-ray image).

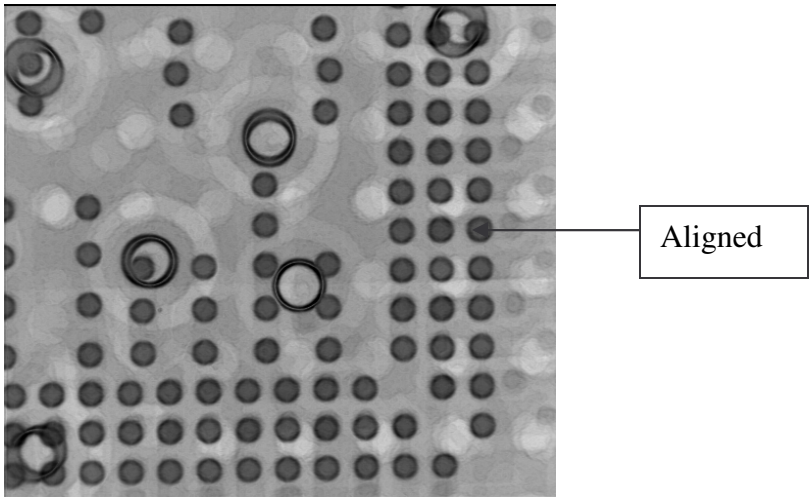


Figure 2.11. After reflow (X-ray image).

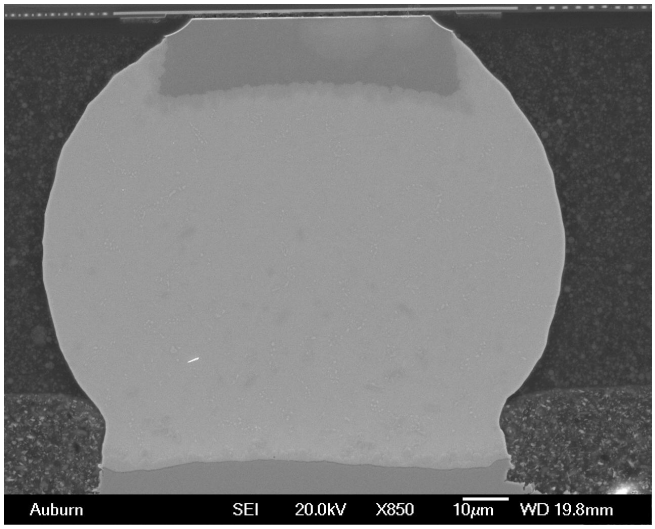


Figure 2.12. Cross section of flip chip assembly on bumped substrate.

For underfilling, a fast flow underfill, UF 8826 from Ablestick, was used, which has been engineered to withstand the 260 °C peak reflow temperature associated with a flip chip BGA second level lead free solder assembly. The underfill also had self-fillet capability. Its key properties are shown in Table 2.2 .

Viscosity at 25°C	Tg	CTE	Modulus
16,000 cP	132 °C	40ppm/°C (below Tg)	5.4 Gpa

Table 2.2. Underfill UF 8826 properties.

The underfilling process was carried out using a CAMALOT dispense machine. Before underfilling, the assembly was baked at 125°C for three hours to drive off any moisture in the substrate. During underfilling, the substrate was heated and kept at 100 °C to help

underfill flow. A line dispense pattern along the die left edge was used and the length of the line was 80 % of the die edge length. Two dispense passes were found to completely fill the gap and produce a good fillet. It took about 15 seconds to finish underfilling one sample. The underfill was cured at 165 °C for 90 minutes. C-SAM was used to inspect the underfill for voids after cure. Figure 2.13 shows a typical void-free flip chip assembly C-SAM image.

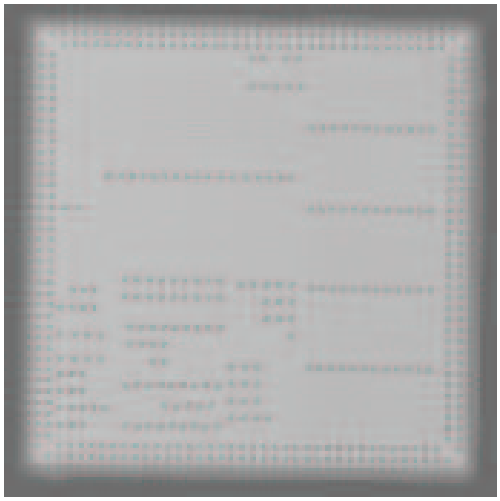


Figure 2.13. C-SAM for underfilled flip chip assembly.

2.4 Thermal Shock Reliability Test, Results, Failure Analysis and Ni Impact Study

2.4.1 Thermal Shock Reliability Test

The two groups of flip chip assemblies were subjected to liquid to liquid thermal shock reliability testing. The test profile was from -55 °C to 125 ºC with 5 minutes dwell time at each temperature extreme and 8 seconds transition time.

The test vehicle die and substrate used were not daisy chain interconnected, so resistance continuity measurements to detect solder joint failure after thermal shock tests was not possible. Samples were removed from each group of assemblies at 100, 400 and 800 thermal shock test cycles and cross sectioned to the second outermost row of solder joints (40 solder joints totally) and SEM imaged for failure analysis. C-SAM was also performed at each designated test cycle to check underfill delimitation status.

2.4.2 Test Results, Failure Analysis and Small Ni Impact Study

At 100 thermal shock cycles, there were no solder joint cracks for the two groups of assemblies. At 400 cycles:

(1) Assemblies on solder (Sn/1%Ag/0.5%Cu/0.05%Ni) bumped Sn substrates had 15 out of 40 solder joints with cracks (Figure 2.14).

(2) Assemblies on solder (Sn/1%Ag/0.5%Cu) on pad substrates had 17 out of 40 solder joints with cracks (Figure 2.15).

To help better identify the solder joint failure mode, ion milling surface preparation was performed on the cross sectioned and polished samples by sponsor Texas Instruments. With SEM analysis, it was found that for both groups of samples, the failure mainly occurred in the bulk solder near the substrate side IMC location, as seen in Figure 2.14 and Figure 2.15.

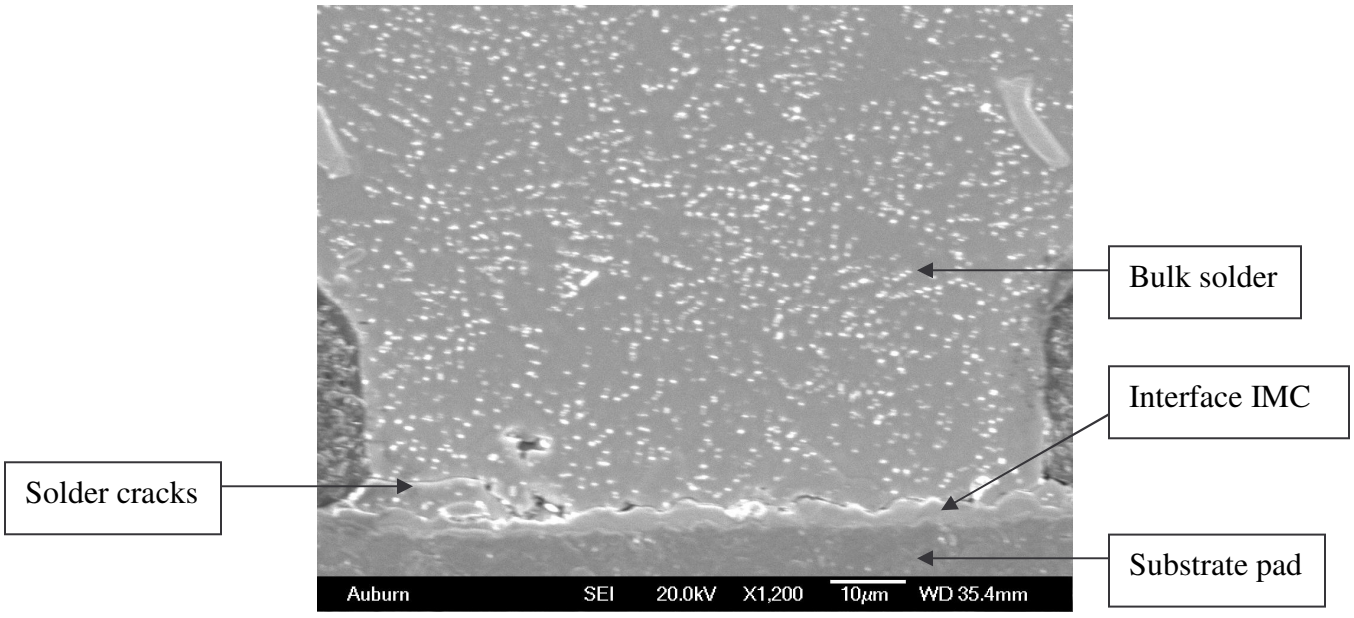


Figure 2.14. Cross section of assembly on bumped Sn substrate (After 400 thermal shock cycles).

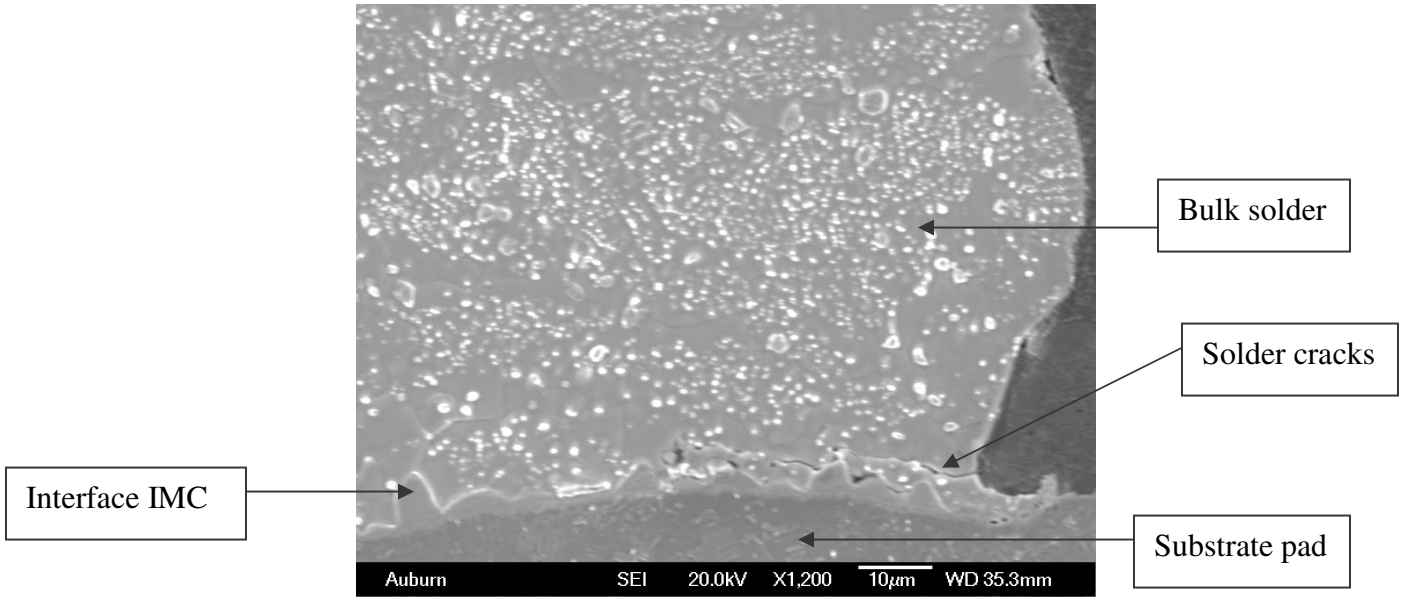


Figure 2.15. Cross section of assembly on solder on pad substrate (After 400 thermal shock cycles).

Comparing the above test results, the conclusion was that small amount of Ni introduced in the solder joint had no significant impact on lead free solder joint thermal shock reliability.

At 800 thermal shock cycles, all solder joints had cracks for each group of assemblies (Figure 2.16). The reliability difference between the two groups at 800 thermal shock cycles could not be determined. There was no underfill delamination in either group of assemblies up to 800 cycles (Figures 2.17-2.18).

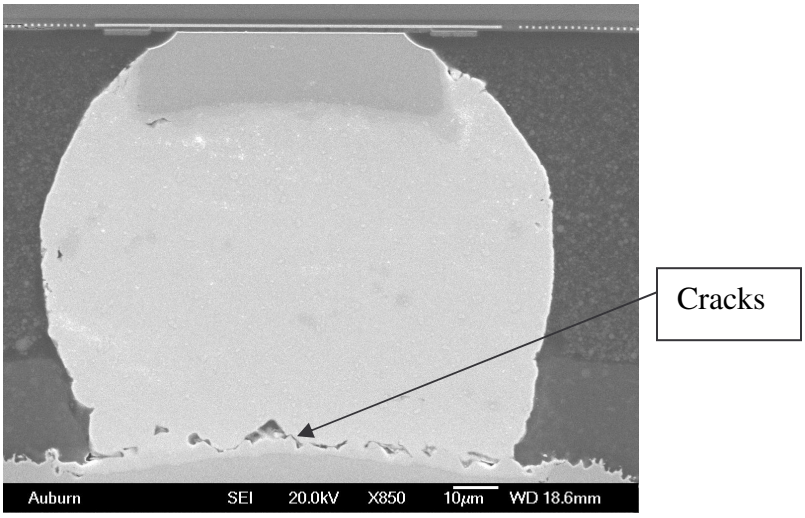


Figure 2.16. Typical failure at 800 thermal shock cycles for the two groups.

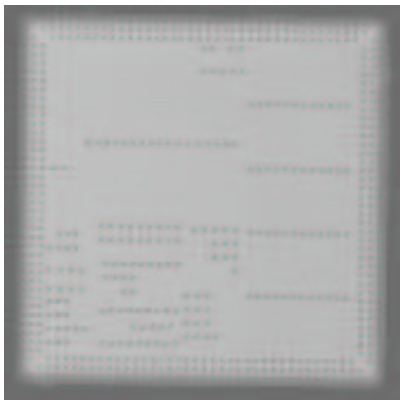


Figure 2.17. C-SAM at zero cycle.

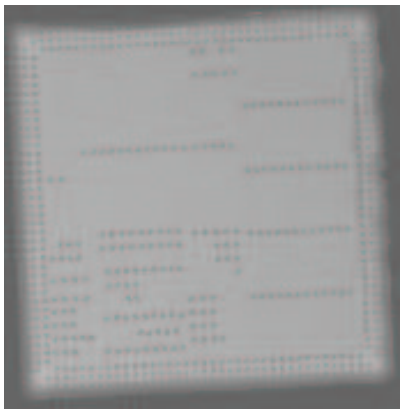


Figure 2.18. C-SAM at 800 cycles.

The following IMC and Ni metallurgy analysis was performed on assemblies with bumped Sn finished substrate. The results showed:

1. 0.05% Ni from the bumping paste was concentrated at the substrate IMC layer (~1At %) (Table 2.3, Figures 2.19-2.20).
2. $(Ni \sim 1\%, Cu)_6 Sn_5$ was the IMC formed at the substrate side (Table 2.3).
3. The die site IMC $Cu_6 Sn_5$ has no Ni (Figures 2.21-2.22, Table 2.4, below EDS 0.1wt% detection limit).
4. The bulk solder has no Ni (Figures 2.23-2.24, Table 2.5, below EDS 0.1wt% detection limit).

5. IMC with Ni concentrated (Figure 2.14) showed more uniform thickness than that without Ni. (Figure 2.15)

Since Ni was only concentrated at the substrate side IMC, it could be inferred that the Ni concentration occurred during substrate bumping instead of the flip chip attach soldering process.

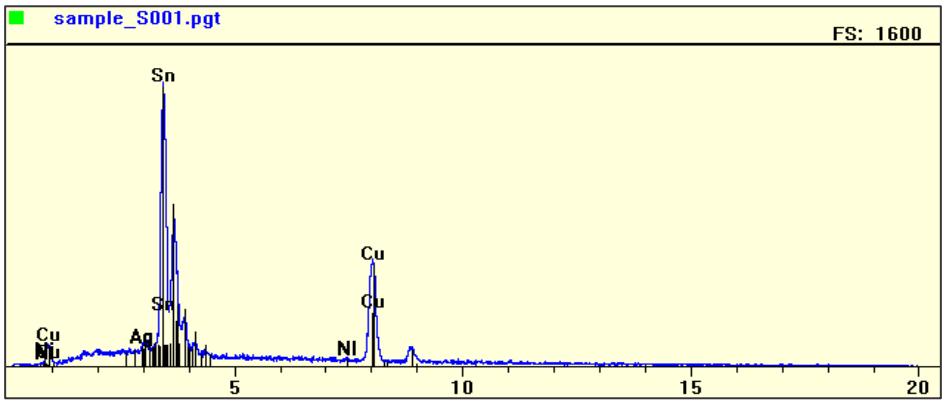


Figure 2.19. EDS for substrate site IMC (assembly on bumped Sn substrate).

Element	Line	keV	KRatio	Wt%	At%
Cu	KA1	8.046	0.4020	37.77	52.85
Ni	KA1	7.477	0.0077	0.68	1.03
Ag	LA1	2.984	0.0002	0.03	0.02
Sn	LA1	3.443	0.5636	61.53	46.09
Total			**0.9736**	**100.00**	**100.00**

Table 2.3. EDS composition map for substrate site IMC (assembly on bumped Sn finished substrate).

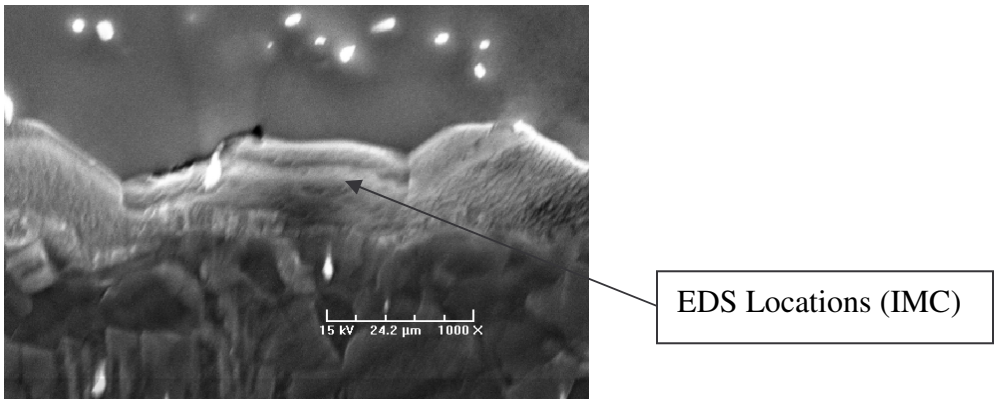


Figure 2.20. SEM image for substrate site IMC (assembly on bumped Sn finished substrate).

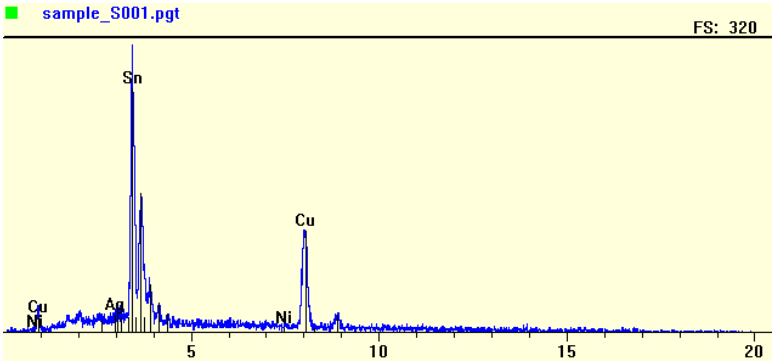


Figure 2.21. EDS for die site IMC (assembly on bumped Sn finished substrate).

Element	Line	keV	KRatio	Wt%	At%
Ag	LA1	2.984	0.0000	0.00	0.00
Cu	KA1	8.046	0.4357	41.04	56.52
Sn	LA1	3.443	0.5390	58.96	43.47
Ni	KA1	7.477	0.0001	0.01	0.01
Total			**0.9747**	**100.00**	**100.00**

Table 2.4. EDS composition map for die site IMC (assembly on bumped Sn finished substrate).

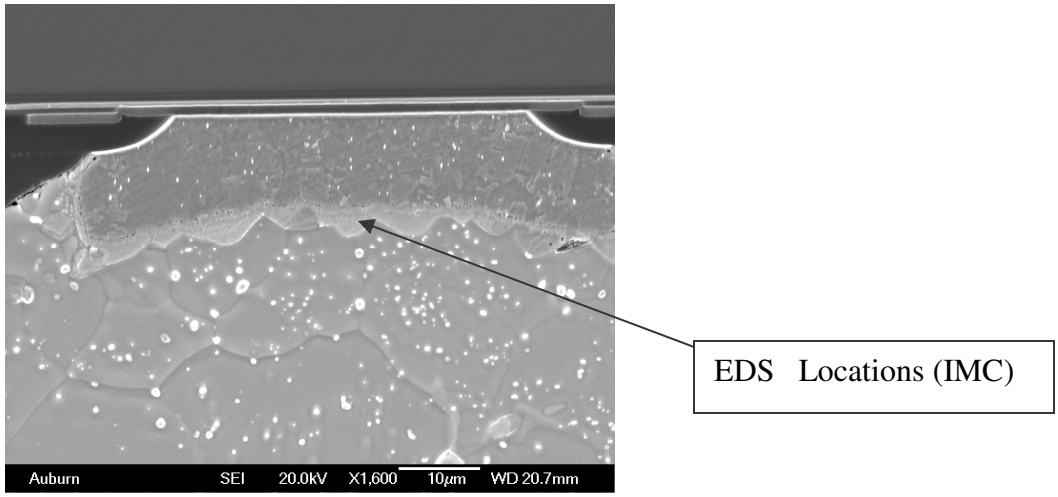


Figure 2.22. SEM image for die site IMC (assembly on bumped Sn finished substrate).

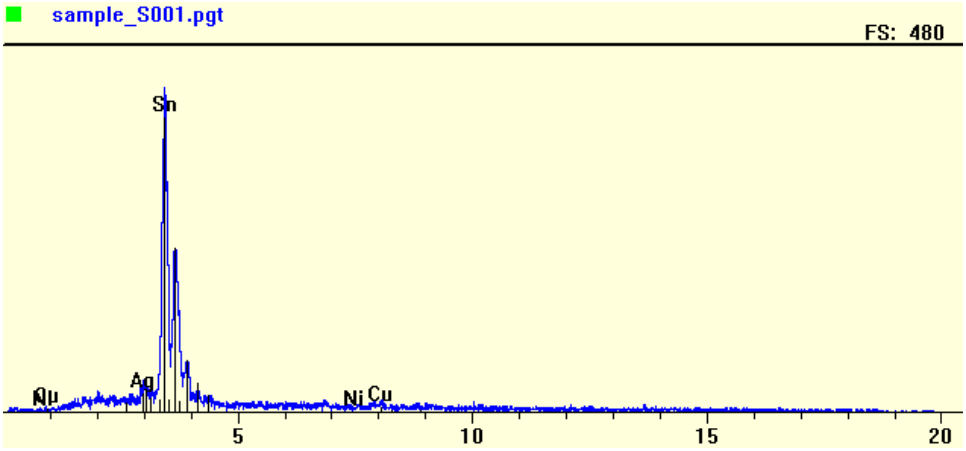
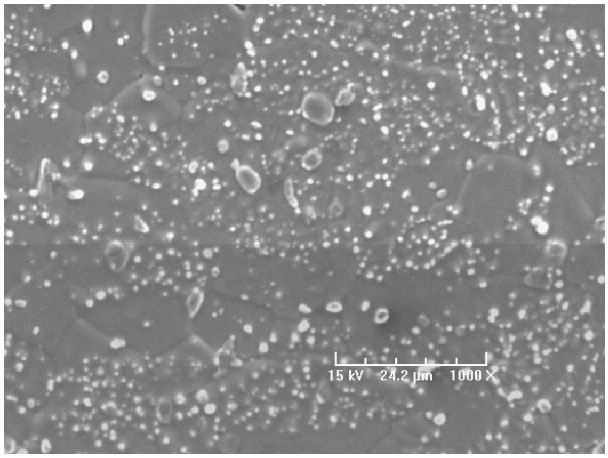


Figure 2.23. EDS for bulk (assembly on bumped Sn finished substrate).

Element	Line	keV	KRatio	Wt%	At%
Ag	LA1	2.984	0.0215	2.21	2.38
Cu	KA1	8.046	0.0263	2.35	4.29
Sn	LA1	3.443	0.9027	95.39	93.23
Ni	KA1	7.477	0.0006	0.05	0.10
Total			**0.9511**	**100.00**	**100.00**

Table 2.5. EDS composition map for bulk solder (assembly on bumped Sn finished substrate).



EDS done on the whole area

Figure 2.24. SEM image for bulk solder joint (assembly on bumped Sn finished substrate).

2.5 Chapter Summary

In this chapter, the impact of a small amount of Ni on lead free flip chip solder joint thermal shock reliability was studied. Two groups of substrates were used in this study: solder (SAC105) on pad (reference) and Sn finished. Solder paste (Sn/1%Ag/0.5%Cu/0.05%Ni) was used to bump the Sn finished substrate and introduce

Ni in the final solder joint system. Flip chip die bumped with SnAg eutectic was used for assembly on the two groups of substrates. The bumped die assembly on bumped (dome shape) substrate was successfully demonstrated. Assemblies thermal shock reliability test and failure analysis were performed. The small amount of Ni from the bumping paste was concentrated at the substrate site IMC, forming $(Ni \sim 1\%, Cu)_6 Sn_5$, but this did not measurably impact the solder joint thermal shock reliability.

CHAPTER 3 METALLIZATION AND INDIUM SOLDER BASED FLIP CHIP IN PACKAGE HEAT SPREADER ATTACH

3.1 Introduction

In this study, indium was used as the TIM, because indium is a highly compliant solder and has high thermal conductivity. Copper was the heat spreader material used. To attach the heat spreader with indium, the die back side and the copper heat spreader surface need to be metallized with indium solderable metal layer/layers. The metallization materials and the subsequent joining process are critical to make the heat spreader attach reliable and achieve low thermal resistance.

Ni/Au layers are commonly used for indium soldering. Indium forms IMC with both Au and Ni. Heat spreader attach with die and Cu heat spreader metallized with Ni/Au has been shown by our team to have good multiple lead free reflow, thermal aging and thermal shock cycle reliability [14]. Intel used Ti/NiV/Au for Si die backside metallization and Ni/Au for Cu heat spreader metallization for its indium based heat spreader attachment [49]. The electroplated gold thickness on the heat spreader and the indium bond line thickness impacts on attachment thermomechanical reliability were evaluated. It was found that the reliability of the attach is “generally improved by decreasing the heat spreader gold metallization thickness and increasing the bond line thickness. However, excessively thin gold must be avoided and slightly, thicker gold

actually performs better in some cases" [49]. TaN/Ru/Au was another metallization used for indium soldering [52]. Si die metallized with TaN/Ru/Au was attached on Si substrates metallized with TaN/Ru/Au. The attachment was evaluated with multiple reflows testing. There was no pull strength degradation after four reflows with a peak reflow temperature at 260 ºC.

The metallization stack for indium soldering typically had a layer of metal between the top Au anti-oxidization layer and the bottom adhesion layer to the die. It is commonly believed that a minimum thickness of this layer is needed to make sure during soldering and the following solder joint service life time, this layer will not be consumed, otherwise, dewetting or severe solder joint reliability degradation will typically occur, however, in this study, it was found that Ti/Au (3000 Å) thin film die without the Ni layer can still yield a similar indium solder joint reliability as that with the Ni layer.

3.2 Objectives of This Study

The objectives of this study were:

- To develop a low voiding heat spreader attachment process.
- To evaluate Ti/Au thin film die backside metallizations for indium soldering based heat spreader attach.
- To characterize the resulting heat spreader attachment thermomechanical reliability.

3.3 Low Voiding Attachment Process Development

Low voiding is desired for heat spreader attachment, since a void is not a good thermal conductor. A void may also degrade the TIM mechanical performance. A 22mm x 22mm sandwich construction of Si (Ti/Ni/Au)/In/Si (Ti/Ni/Au) was used to evaluate different soldering processes (reflow, thermal compression reflow bonding and vacuum soldering). For reflow soldering in a Heller 1800 oven, the profile ramped to 180ºC and was held for 200 seconds. Various weights were evaluated during assembly. An N_2 reflow environment was used with no flux. The resulting assemblies had significant voiding (Figure 3.1). Reflow in air with an indium compatible RA flux applied by dip fluxing was also investigated and the voiding was worse. A Karl Suss thermal compression bonder was evaluated for reflow bonding the assembly. The bonding tool temperature (165, 180 and 200ºC) and bonding force (50, 100, 200 and 400 grams) were varied. The resulting assemblies had significant voiding (Figure 3.2). Vacuum soldering (~$5x10^{-5}$ torr) using a SST vacuum soldering /brazing furnace with a temperature profile dwell at 180ºC for 3 minutes and a 20 gram weight yielded low voiding in the Si on Si assembly (Figure 3.3).

Figure 3.1. X-ray image for assembly with the reflow oven [14].

Figure 3.2. X-ray image for assembly with the thermal compression bonder [14].

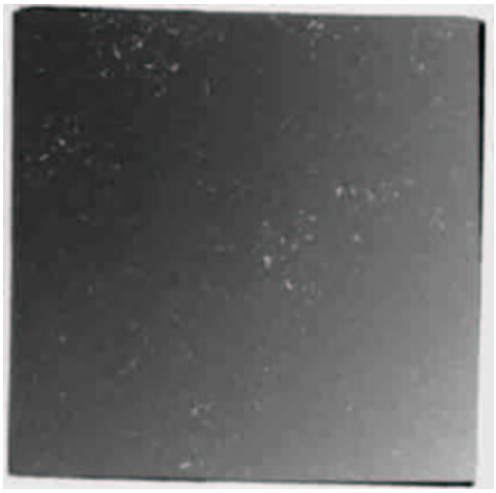


Figure 3.3. X-ray image for assembly with the vacuum furnace [14].

For Ni/Au coated Cu heat spreader attachment, the following vacuum soldering process was developed with good wetting and low voiding (Figures 3.4 to 3.7). For 10mm x 10mm Cu on 5mm x 5mm Si assembly, a 1.5 gram weight was used and for 24mm x 24mm Cu on 22mm x 22mm Si, a 20 gram weight was used. Before assembly, the die and heat spreader were Ar plasma cleaned for five minutes at 0.3KW and 0.6 torr. Figure 3.4 shows the reflow temperature profile. The temperature measured is a reference temperature measured by the vacuum reflow system and not the actual In solder joint temperature. The vacuum was ~$5x10^{-5}$ torr. No flux was needed.

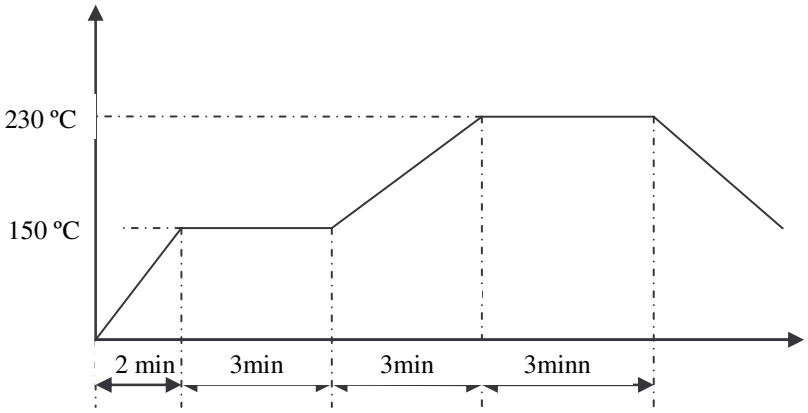


Figure 3.4. Reflow profile.

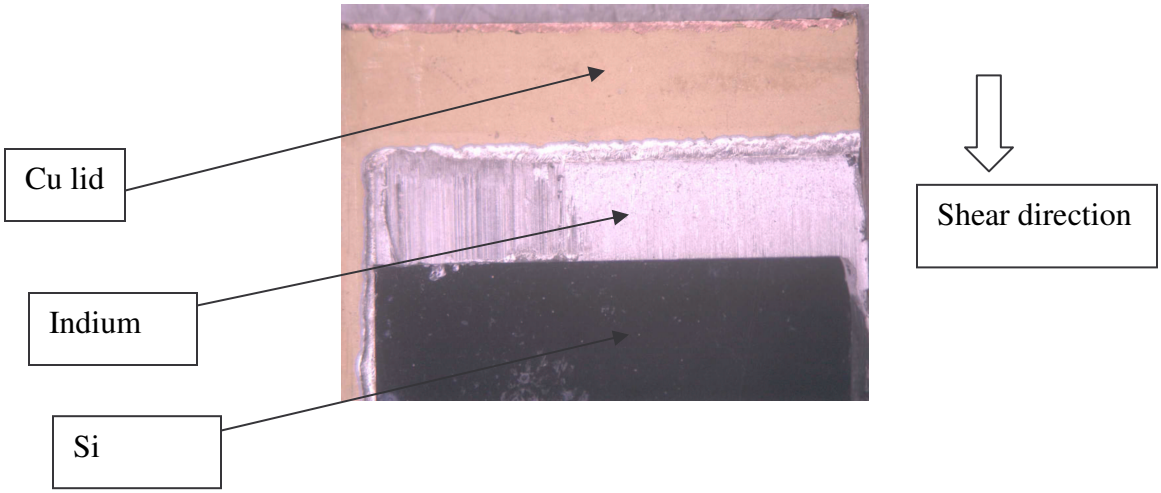


Figure 3.5. Si-Indium-Cu shear failure surface showing good wetting.

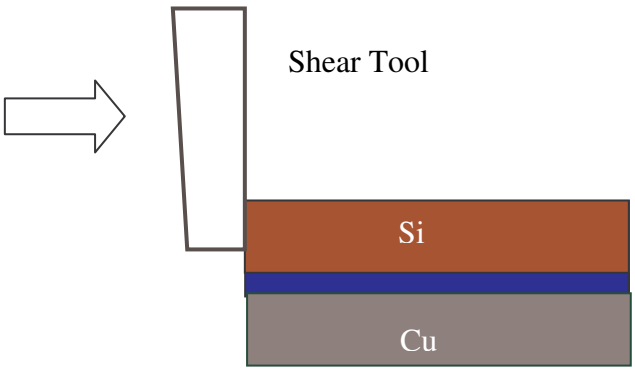


Figure 3.6. Shear test method.

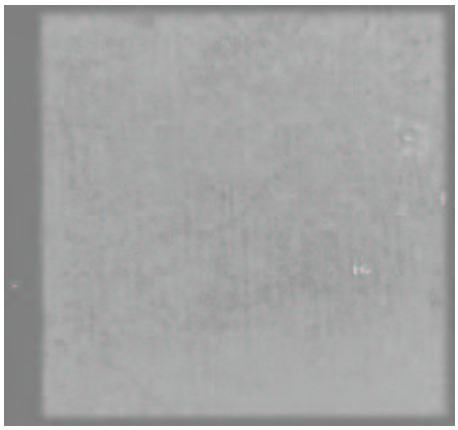


Figure 3.7. C-SAM for Cu on Si assembly showing low voiding.

3.4 Evaluation of Ti/Au (2000 Å) Die Metallization for Indium Based Heat Spreader Attach

3.4.1 Initial Evaluation and the Resulting Joint Structure Analysis

In this experiment, Ti (1000 Å)/Au (2000 Å) was deposited on a Si wafer using the E-beam evaporation process. From the finished wafer, Si (5mm x 5mm)/Indium/Si (10mm x 10mm) test parts were built with vacuum soldering and shear tested. There was significant shear strength, which indicated bond formation during soldering. Further solder joint microstructure study with TEM was performed by Texas Instruments (Figure 3.8). It was found that the gold thin film was consumed after soldering and converted to IMC completely. This agrees with reference [53] (Figure 3.9), however, the depletion of Au did not cause dewetting. The TEM study also showed that $AuIn_2$ was only at the interface. While Ti and In can form an IMC, EDS analysis did not detect any In-Ti IMC.

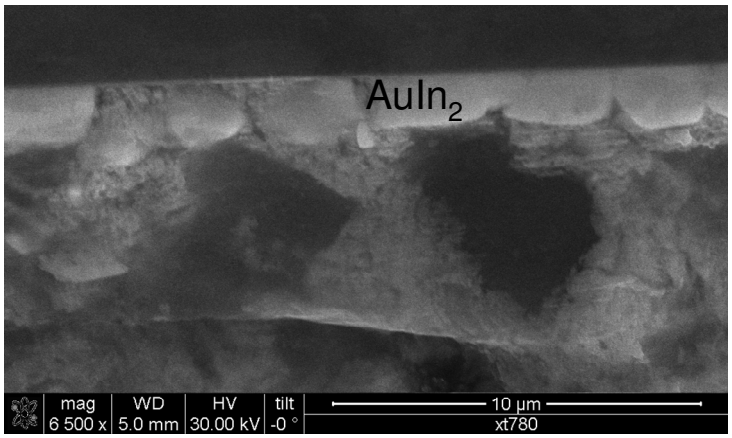


Figure 3.8. Cross section micrograph of Ti/(2000Å) Au assembly showing $AuIn_2$ intermetallic.

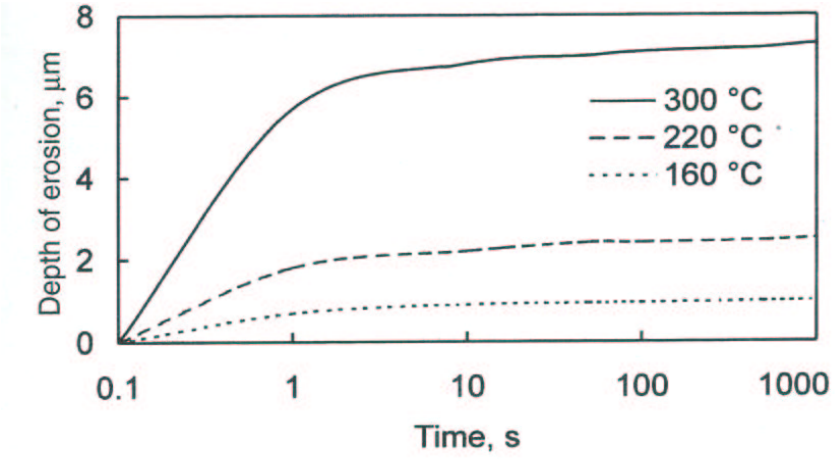


Fig. 2.2 Erosion of a gold metallization by molten indium as a function of reaction time and temperature. Similar results are obtained for indium-base solders, including gold-indium, silver-indium, indium-lead, and indium-tin.

Figure 3.9. Erosion rate of gold by molten indium [53].

3.4.2 Reliability with Ti (1000 Å)/Au (2000 Å) Die

To further evaluate Ti (1000 Å)/Au (2000 Å) metallization for heat spreader attachment, Si (5mm x 5mm) /In (50um)/Si (10mm x 10mm) assemblies were built for multiple reflow and high temperature aging reliability studies. Since a flip chip in

package must survive multiple reflows cycles during subsequent assembly processes, (ball attach to the package, assembly of the package to the next level assembly, etc.) the integrity of the heat spreader attach must be evaluated after multiple reflows. With the move to lead free assembly, the lead free in-air reflow profile shown in Figure 3.10 was used. The peak temperature was 246.5°C and the time above liquidus (221°C) was 64.8 seconds.

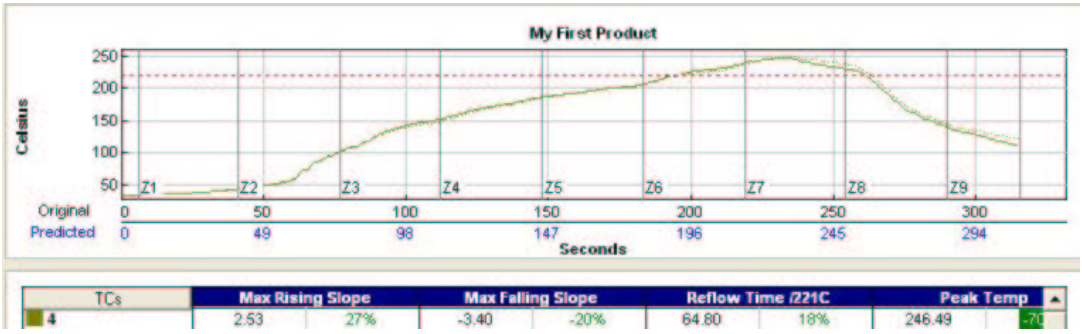


Figure 3.10. Lead free reflow profile.

Figure 3.11 plots shear test results for multiple reflows. After the first reflow, the shear strength increased and there was no significant shear strength change after additional reflows.

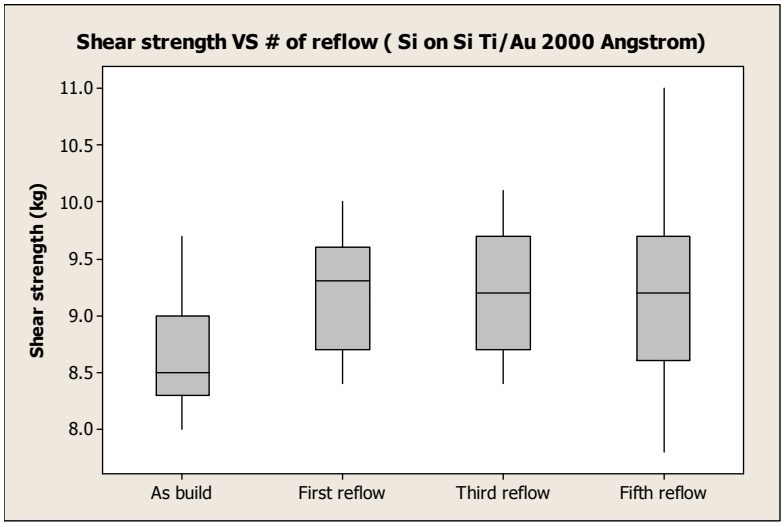


Figure 3.11. Die shear strength as a function of reflows for Si (Ti/Au 2000 Å) die based assembly.

The aging test was at 100 °C for 2000 hours. Figure 3.12 plots the shear test results as a function of aging. The shear strength decreased initially and stabilized after 250 hours aging.

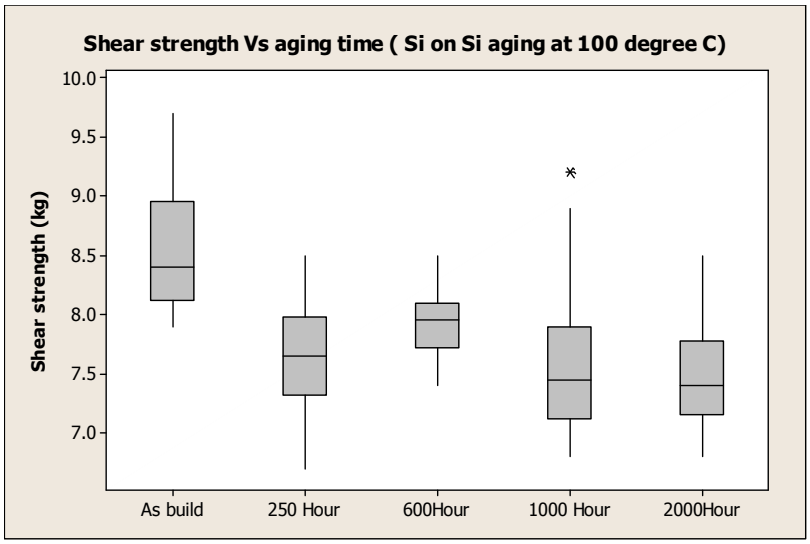


Figure 3.12. Die shear strength as a function of aging for Si (Ti/Au 2000 Å) die based assembly.

Cu (24mm x 24mm x 1mm) on Si (22mm x 22mm) test vehicles were assembled for thermal shock cycle testing. The 1mm thick copper heat spreaders used had a plated Ni (2.5-5µm) finish as-supplied from the vendor. A 1000Å Au layer was subsequently deposited by E-beam evaporation to enhance solderability. Before Au deposition, an in-situ ion milling process was used to remove nickel oxide on the surface of the heat spreader. Indium preforms (50µm thick) purchased from Williams Advanced Materials were used for the assembly. The thermal shock test profile was from -40 °C to +85 °C, with 10 minutes dwell at each temperature extreme and a transition time of 10 seconds. Figures 3.13 to 3.16 show the C-SAM results for the thermal shock cycle test. At 500 cycles, delamination was observed at the indium-to Si interface.

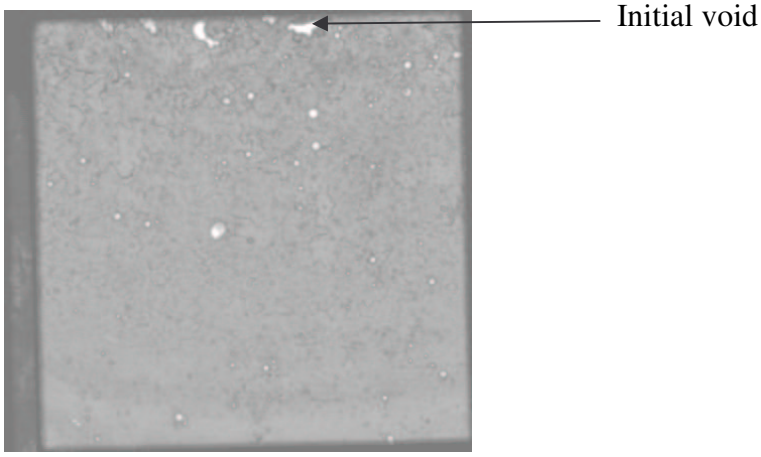


Figure 3.13. C-SAM for assembly with Ti/Au 2000 Å die. (0 cycle).

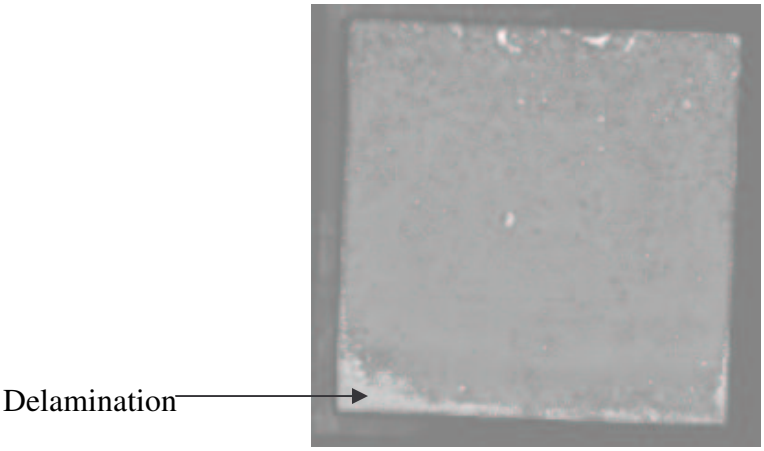


Figure 3.14. C-SAM for assembly with Ti/Au 2000 Å die. (500 cycles).

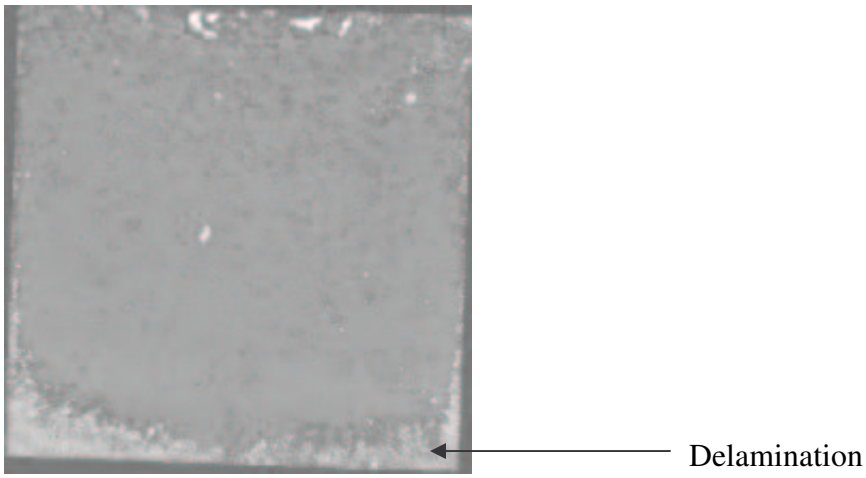


Figure 3.15. C-SAM for assembly with Ti/Au 2000 Å die. (1000 cycles).

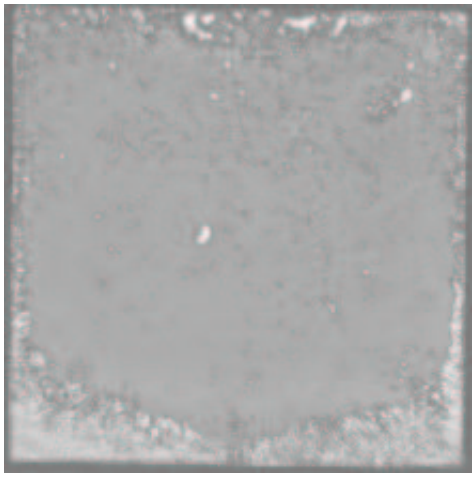


Figure 3.16. C-SAM for assembly with Ti/Au 2000 Å die. (2000 cycles).

For Cu on Si (Ti/Ni/Au) assemblies [14], the thermal shock cycle test had been done from (-55 °C to +80 °C) and there was no significant delamination observed at 1000 cycles. Compared with Cu on Si (Ti/Ni/Au) assembly, Cu on Si (Ti/Au 2000Å) showed early delamination after the thermal shock cycle test.

3.5 Gold Thickness Effect for Attachment with Ti/Au Metalized Si Die

3.5.1 Gold Thickness Effect on Pull Strength

For die with Ti (1000Å)/Au metallization, 5mm x 5mm Si on 10mm x 10mm Si samples were built with different Au thicknesses and pull tested to evaluate the role of Au thickness on strength and failure mode. The pull strength increased with the Au thickness (Figure 3.17). There was significant interfacial (Ti-to-In) failure area for the assemblies with 500Å, 1000Å of Au as shown in Figures 3.18-3.19.

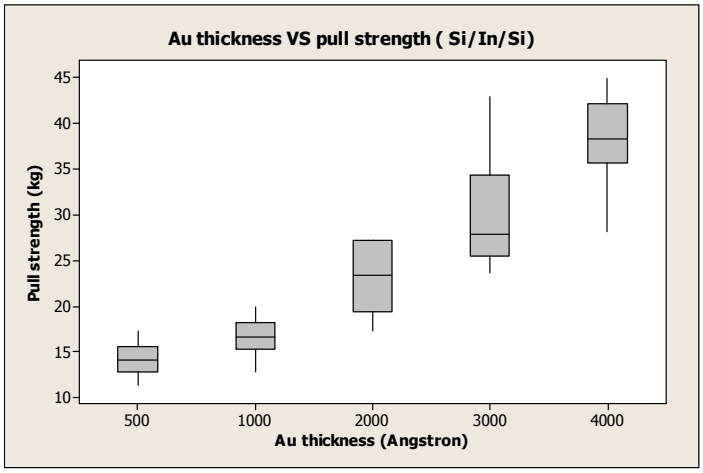


Figure 3.17. Pull strength as a function of Au thickness for Ti/Au metallized Si die.

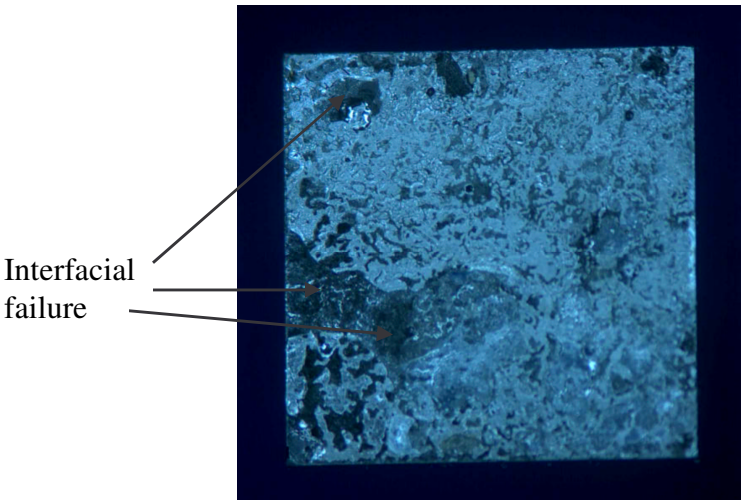


Figure 3.18. Photograph of fracture surface after pull testing for Ti/500Å Au test die.

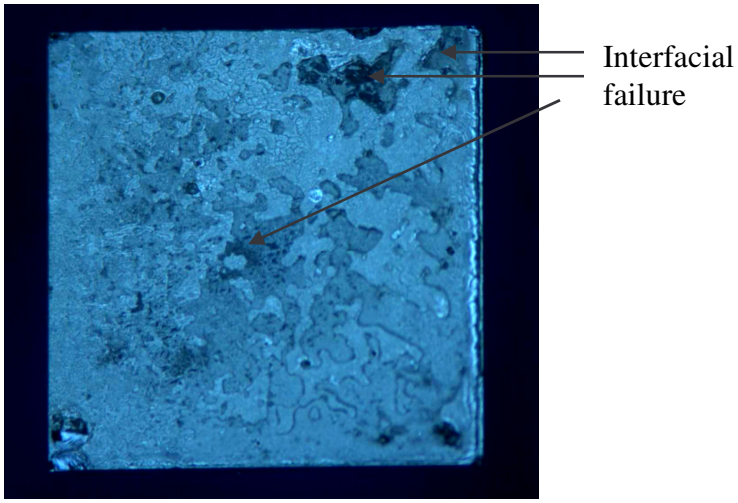


Figure 3.19. Photograph of fracture surface after pull testing for Ti/1000Å Au test die.

For assemblies with 2000Å Au, SEM and EDS were done to see the pull fracture surface and analyze its composition. Figures 3.20 A-C are the pull fracture surface SEM images. Figures 3.20 B and C are the higher magnification images showing certain significant interfacial failure surface (dark surface). EDS "A" (Table 3.1) shows the dark interfacial surface had Ti and had no Au. EDS "B" (Table 3.2) shows the white area was mainly In.

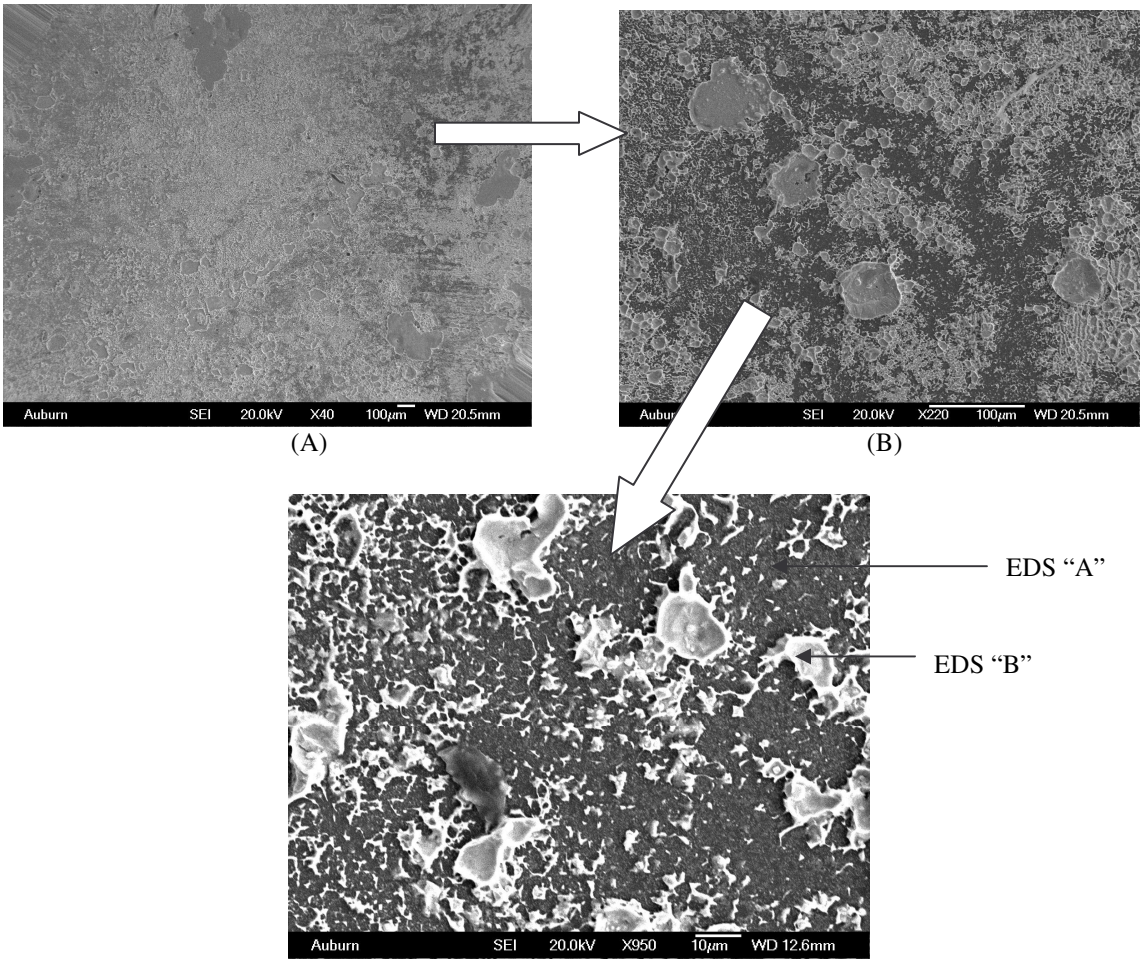


Figure 3.20. SEM Images for Pull Fracture Surface for Assembly with 2000 Å Au die; (A) X40, (B) X220 and (C) X950.

Element	Line	keV	KRatio	Wt%	At%
O	KA1	0.523	0.0027	1.42	2.83
Si	KA1	1.740	0.6966	76.34	86.52
Au	MA1	2.121	0.0000	0.00	0.00
Ti	KA1	4.510	0.0976	11.58	7.70
In	LA1	3.286	0.0817	10.65	2.95
Total			**0.8786**	**100.00**	**100.00**

Table 3.1. EDS "A"

Element	Line	keV	KRatio	Wt%	At%
O	KA1	0.523	0.0002	0.17	1.20
Si	KA1	1.740	0.0022	0.36	1.46
Au	MA1	2.121	0.0062	0.85	0.48
Ti	KA1	4.510	0.0004	0.05	0.12
In	LA1	3.286	0.9338	98.57	96.74
Total			**0.9428**	**100.00**	**100.00**

Table 3.2. EDS "B"

For assembly with 3000Å Au, Figure 3.21 A is the X-ray image before pull and Figure 3.21 B is the pull fracture surface optical image. Corresponding voids were seen from both types of images. Some of the voids were thought the joint seen from pull fracture surfaces. Figures 3.21 C-E are the SEM images. Figures 3.22 D and E are the higher magnification images.

EDS "C" (Table 3.3) shows the void surface had Ti and had no Au. Most of other fracture surface was In as seen from EDS "D" and "E" (Table 3.4-3.5). There was also some micro meter size spot failure surface. Higher Au and Indium composition was found on the spot surface (EDS "F" (Table 3.6)). This surface is close to IMC (significant Au, but more In detected. The Au and In ratio did not correspond to the $AuIn_2$ IMC).

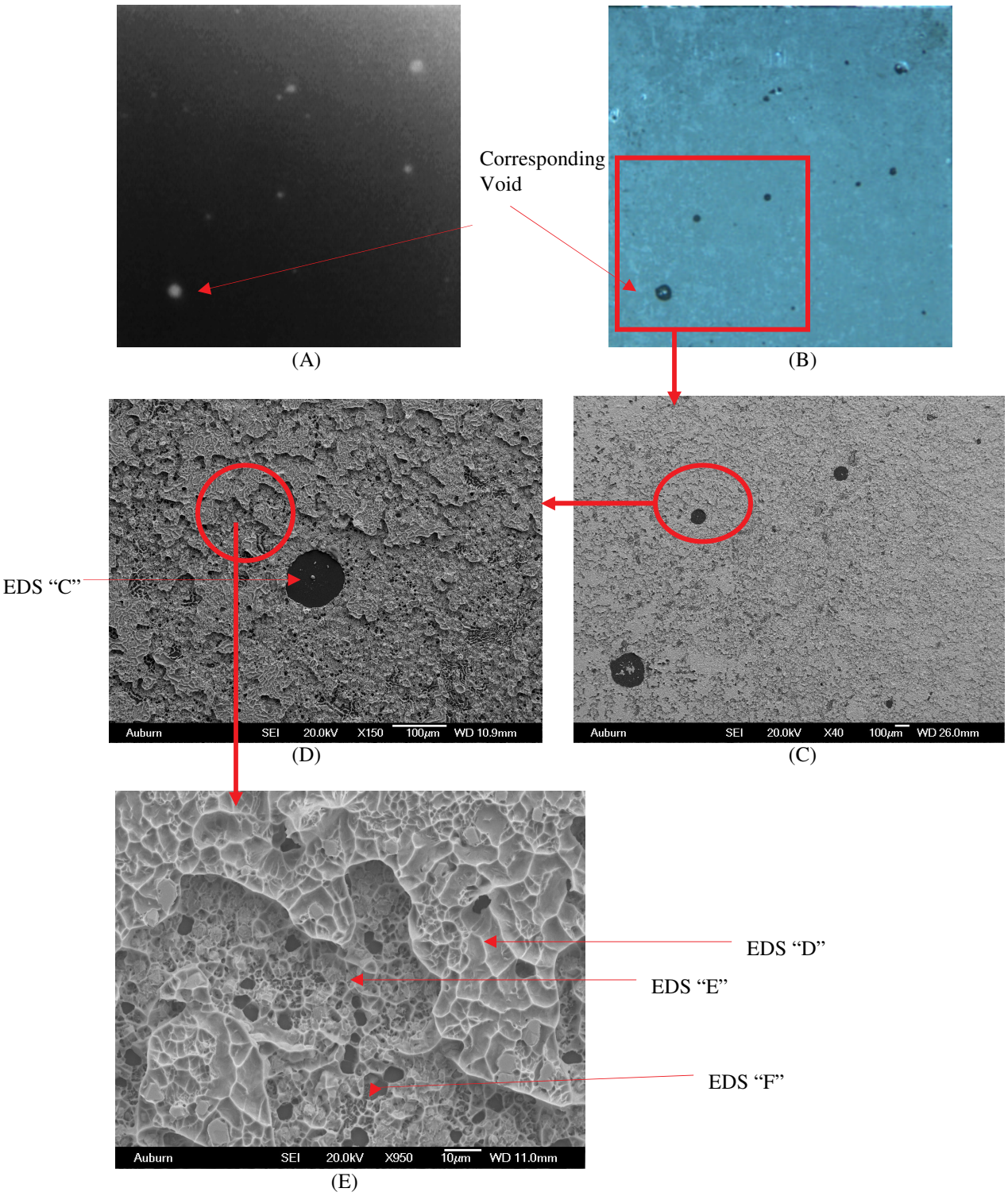


Figure 3.21. (A) X-ray Image for 3000Å Au Assembly; (B) Fracture Surface Optical Image; (C) SEM X40; (D) SEM X150; (E) SEM X950.

Element	Line	keV	KRatio	Wt%	At%
O	KA1	0.523	0.0000	0.01	0.02
Si	KA1	1.740	0.7983	84.47	91.04
Au	MA1	2.121	0.0000	0.00	0.00
Ti	KA1	4.510	0.1112	13.18	8.33
In	LA1	3.286	0.0177	2.34	0.62
Total			**0.9273**	**100.00**	**100.00**

Table 3.3. EDS "C"

Element	Line	keV	KRatio	Wt%	At%
O	KA1	0.523	0.0000	0.02	0.16
Si	KA1	1.740	0.0003	0.04	0.18
Au	MA1	2.121	0.0005	0.07	0.04
Ti	KA1	4.510	0.0000	0.00	0.00
In	LA1	3.286	0.9488	99.86	99.62
Total			**0.9497**	**100.00**	**100.00**

Table 3.4. EDS "D"

Element	Line	keV	KRatio	Wt%	At%
O	KA1	0.523	0.0001	0.07	0.47
Si	KA1	1.740	0.0150	2.41	9.08
Au	MA1	2.121	0.0159	2.18	1.17
Ti	KA1	4.510	0.0098	1.14	2.52
In	LA1	3.286	0.8849	94.19	86.76
Total			**0.9257**	**100.00**	**100.00**

Table 3.5. EDS "E"

Element	Line	keV	KRatio	Wt%	At%
O	KA1	0.523	0.0000	0.00	0.00
Si	KA1	1.740	0.0031	0.49	2.20
Au	MA1	2.121	0.2022	27.06	17.38
Ti	KA1	4.510	0.0029	0.33	0.86
In	LA1	3.286	0.6249	72.12	79.56
Total			**0.8330**	**100.00**	**100.00**

Table 3.6. EDS "F"

Figures 3.22 A-C are the pull fracture surface SEM images for assembly with 4000Å Au. Figures 3.22 B and C are the higher magnification images. There were no voids. Most of the fracture surface was In as seen from EDS "G" (Table 3.7). Other fracture surface (EDS "H") and some tiny spot failure surface (EDS "I") were close to the IMC layer (significant Au, but more In detected. Table 3.8-3.9).

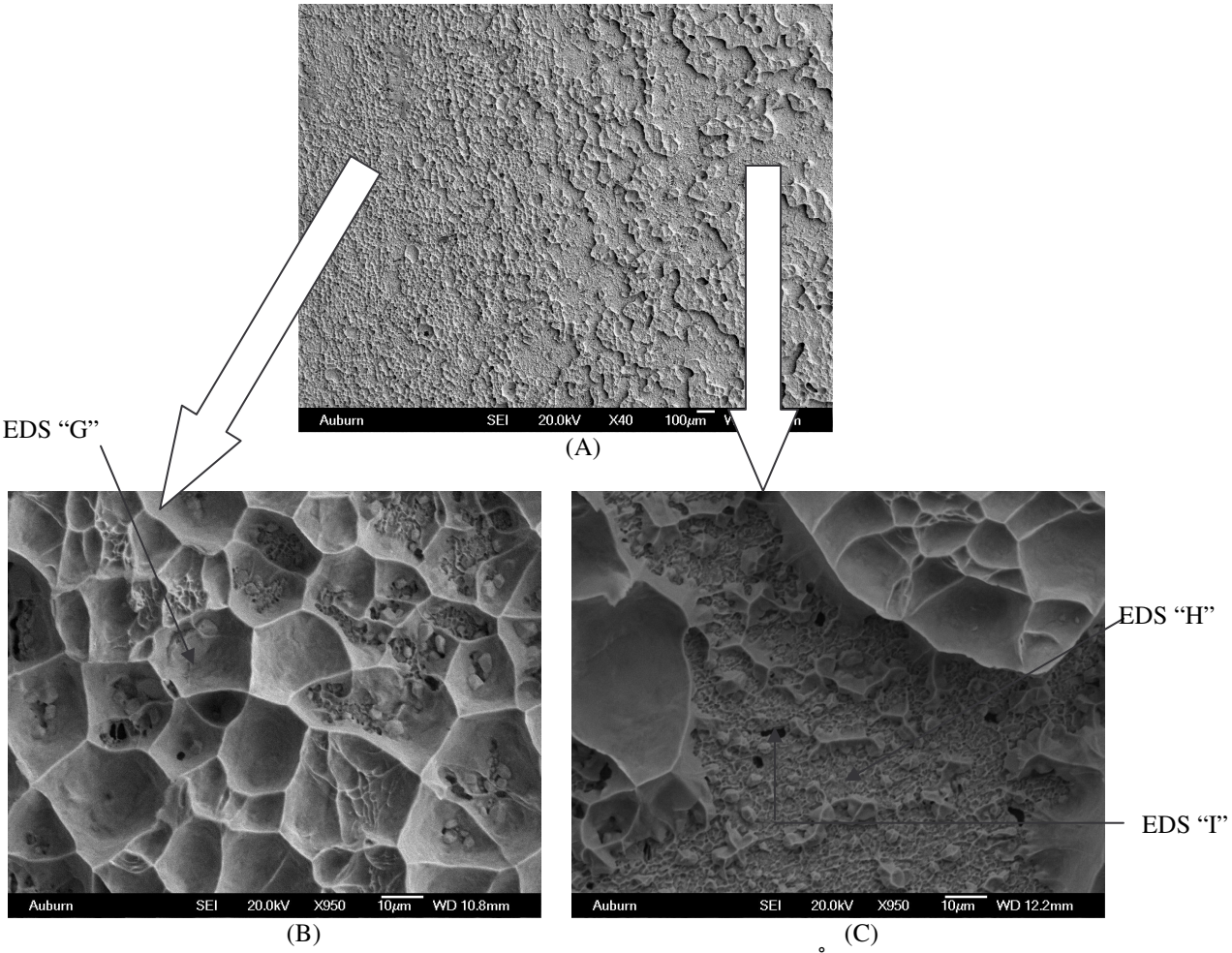


Figure 3.22. SEM image for pull fracture surface for assembly with 4000 Å Au die; (A) X40, (B) X950 and (C) X950.

Element	Line	keV	KRatio	Wt%	At%
O	KA1	0.523	0.0001	0.13	0.91
Si	KA1	1.740	0.0009	0.15	0.60
Au	MA1	2.121	0.0026	0.36	0.20
Ti	KA1	4.510	0.0000	0.00	0.00
In	LA1	3.286	0.9431	99.37	98.29
Total			**0.9468**	**100.00**	**100.00**

Table 3.7. Table EDS "G"

Element	Line	keV	KRatio	Wt%	At%
O	KA1	0.523	0.0000	0.00	0.00
Si	KA1	1.740	0.0006	0.09	0.41
Au	MA1	2.121	0.1963	26.30	17.15
Ti	KA1	4.510	0.0000	0.00	0.00
In	LA1	3.286	0.6403	73.62	82.45
Total			**0.8372**	**100.00**	**100.00**

Table 3.8. Table EDS "H"

Element	Line	keV	KRatio	Wt%	At%
O	KA1	0.523	0.0001	0.08	0.57
Si	KA1	1.740	0.0033	0.53	2.21
Au	MA1	2.121	0.0671	9.13	5.41
Ti	KA1	4.510	0.0003	0.03	0.07
In	LA1	3.286	0.8327	90.23	91.74
Total			**0.9034**	**100.00**	**100.00**

Table 3.9. Table for EDS "I"

4000 Å Au based assemblies had significantly higher median pull strength than assemblies with 3000 Å Au, However, the fracture surface composition analysis of 4000 Å and 3000 Å Au based assembly only showed with the exception of the voids minor differences between them. These voids yielded localized severe non-continuous IMC formation. For the 4000 Å based assembly, the IMC was found by Texas Instruments using TEM to be more continuous than the 3000 Å based assembly. It was also seen that

the pull fracture surface had basically no Ti exposure, even though certain samples showed minor voids under X-Ray and thus, these voids were in the bulk indium, which were different from that of 3000 Å Au based assembly.

For 3000 Å based assembly, void analysis and its relationship with pull strength was evaluated. The assembly was inspected by X-ray for voids (Figure 3.23). An image processing program was used to calculate the void area percentage. It was seen from Figure 3.24 that the pull strength decreased as the void level increased. With minor voiding, the pull strength was close to the 4000 Å based assembly.

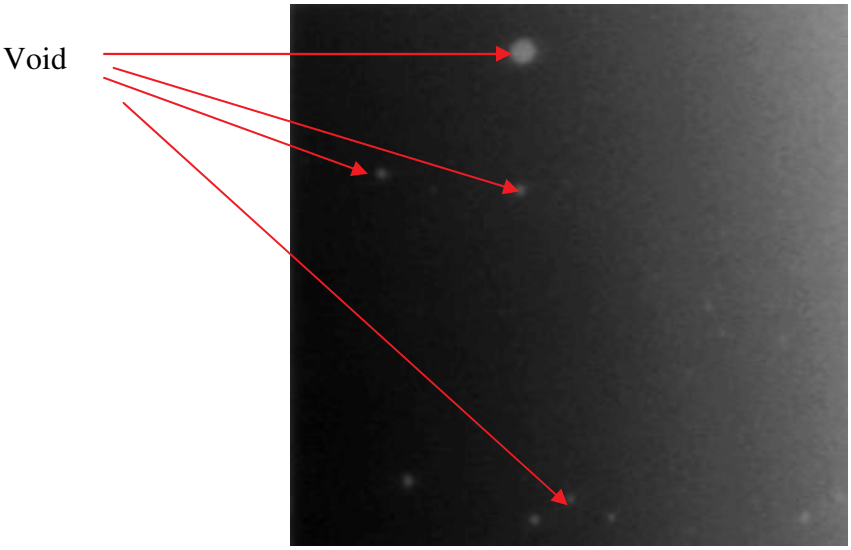


Figure 3.23. X-ray image example showing void

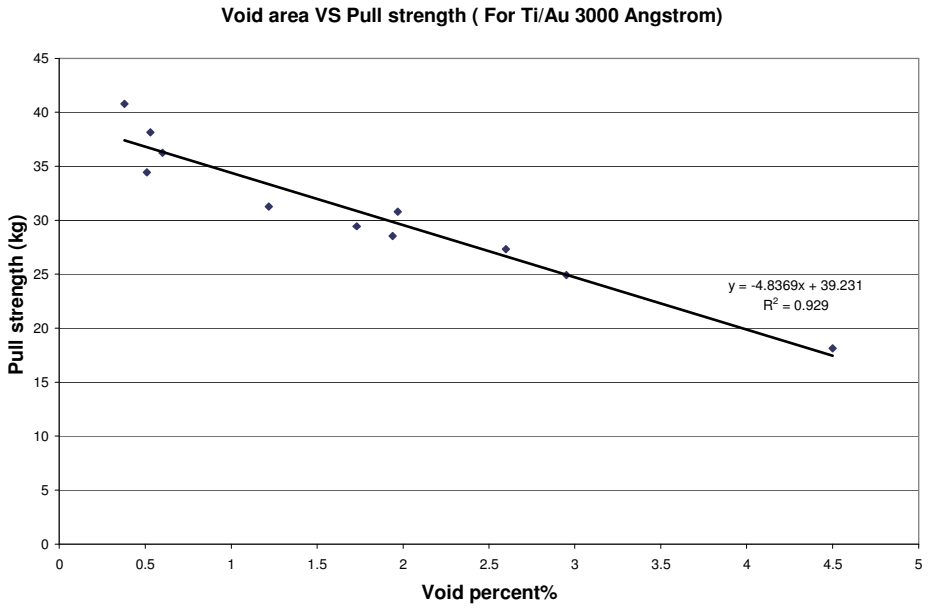


Figure 3.24. Void area VS pull strength (For 3000 Å Au based assembly)

3.5.2 Modeling the Pull Test

Finite element software ANSYS was used to model the pull test. Ideally, indium's true tensile fracture strength, the material's property, was needed to model the pull force required to break the joint, however, this material property was not found from the literature. The tensile strength of indium was found to be 1.6 MPa from Indium Corp [54]. The tensile strength is the stress at which necking begins in a ductile material and it is not the true stress at which the material fractures (the end of necking) in tension. The true fracture strength is higher than the tensile strength. The only related information found was that in reference [55], the author did indium interconnection process optimization with ultrasonic welding method and accomplished an indium joint with tensile fracture strength of 9.21 MPa.

A model was built to see first, the pull force to fracture the indium joint assuming it also failed at 9.21 MPa tensile stress as produced in reference [55] and second, the average tensile stress produced under the 38.2 Kg pull force from the pull test of 4000 Å Au based assembly. The Si material properties and the indium's constitutive relationship used in the model were shown in Table 3.10-3.11 and Figure 3.25. The pull stud used had 4.1mm diameter and the pull force rate was 0.45kg/second as used in the experiment.

Si properties	Modulus E (Gpa)	Density(gcm-3)	Poisson's Ratio
	150	2.329	0.2152

Table 3.10. Si mechanical properties [56-57]

Solder alloy	Material Parameters								
	A	Q/R	ζ	m	s	n	H_0	A	s_0
In	2.33E8	9369.7	49.97	0.30	2.83E7	0	0	1	2.83E7

Table 3.11. Parameters with Anand model of Indium for steady state plastic flow [58].

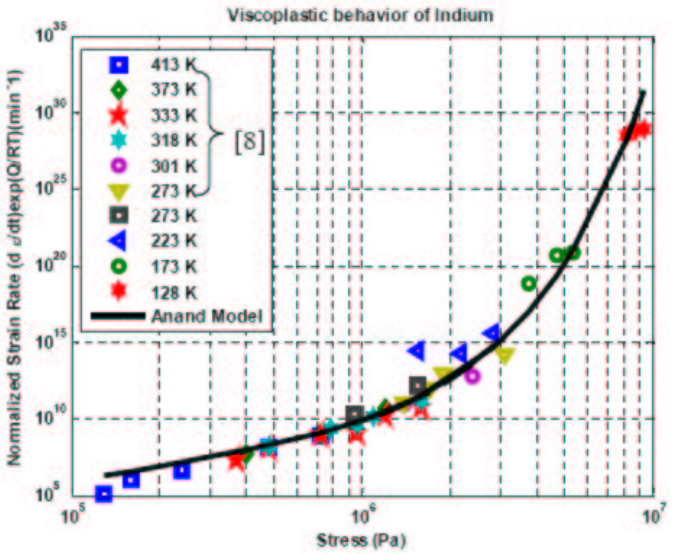


Figure 3.25. Time-temperature dependent materials properties of indium [58]

In ANSYS, SOLID45 element was used for the silicon material and VISCO107 was used for the indium layer. For each time step, the average tensile stress in the indium layer was calculated by averaging the tensile stress on the nodes. The model result (Table 3.12 highlighted) predicts if the joint failed at 9.21 MPa, then the pull force would be 21.6Kg. The model also predicted that a 38.25Kg pull force will produce 16.4 MPa stress in the joint. The conclusion from the model was that the indium joint produced in the experiment had much higher fracture strength than that produced in reference [55].

time (s)	force (kg)	average tensile stress (Pa)
5	2.25	9.14E+05
10	4.5	1.85E+06
15	6.75	2.82E+06
20	9	3.79E+06
25	11.25	4.75E+06
30	13.5	5.72E+06
35	15.75	6.69E+06
40	18	7.66E+06
45	20.25	8.63E+06
48	**21.6**	**9.21E+06**
50	22.5	9.60E+06
52	23.4	9.98E+06
55	24.75	1.06E+07
60	27	1.15E+07
65	29.25	1.25E+07
70	31.5	1.35E+07
75	33.75	1.44E+07
80	36	1.54E+07
85	**38.25**	**1.64E+07**

Table 3.12. Modeling results

3.5.3 Gold Thickness Effect on Shear Performance

Shear performance was evaluated with increasing gold thickness. Cu (10mm x 10mm) on Si (5mm x 5mm) samples were built and shear tested (Figure 3.26). Assembly with 3000Å and 4000 Å Au coated die had similar shear strength with shear failure in the bulk indium layer. Assembly with 2000Å Au coated die had lower shear strength and certain samples showed significant Ti-In fracture surface (Figure 3.27).

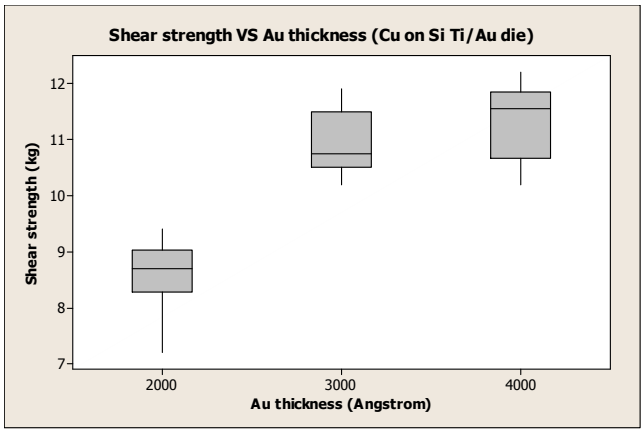


Figure 3.26. Shear Strength as a Function of Au Thickness for Ti/Au Metallized Si Die

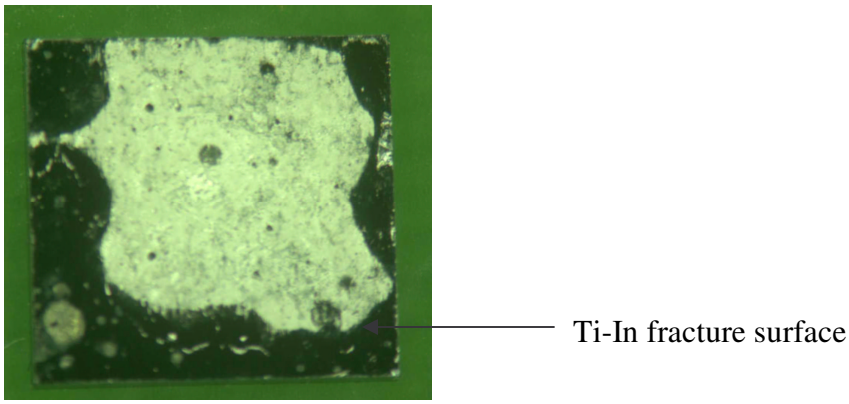


Figure 3.27. Shear Failure Surface (Some Samples) for Cu on Si (Ti/Au2000Å)

For flat Cu heat spreader attachment, during thermal shock cycle test, the solder joint is in shear stress. Since 3000Å Au and 4000Å Au die based assembly had similar shear strength, even though 4000Å Au die had higher pull strength, the decision was made to use 3000Å Au die for the next round evaluation.

3.6 Reliability of Heat Spreader Attach with Ti/Au (3000 Å) and Ti/Ni/Au Die

Ti (1000Å)/Au (3000Å) and Ti (1000Å)/Ni (2700Å)/Au (1000Å) metallized die were prepared. Ti/Ni/Au die based assembly was used as the control. To simulate a real

product application, only Cu on Si was used in this part of the study. Cu (10mm x 10mm) on Si (5mm x 5mm) was used for multiple reflows and aging tests. Cu (24mm x 24mm) on Si (22mm x 22mm) was used for thermal shock cycle tests.

The lead free multiple reflows test profile used was the same as in Figure 3.10. Figure 3.28 plots the die shear strength as a function of multiple reflows for Ti/Ni/Au and Ti/Au metallized Si die. Die pull tests were also performed on the two types of assemblies after multiple reflows (Figure 3.29). There was no reliability degradation after multiple reflows for assemblies with both metallizations. The Ti/Au samples had higher median shear strength after multiple reflows compared to the Ti/Ni/Au. The median pull strength for Ti/Ni/Au was slightly better than for Ti/Au.

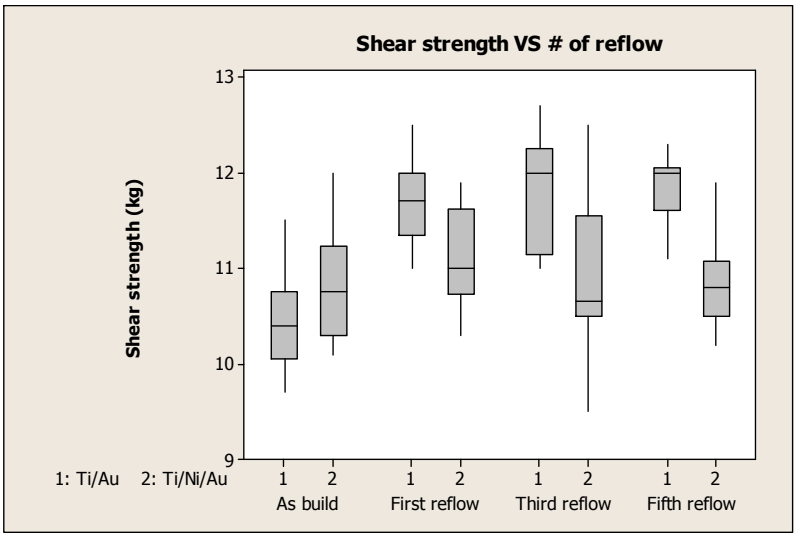


Figure 3.28. Die shear strength as a function of reflows for Ti/Ni/Au and Ti/Au 3000 Å metalized die.

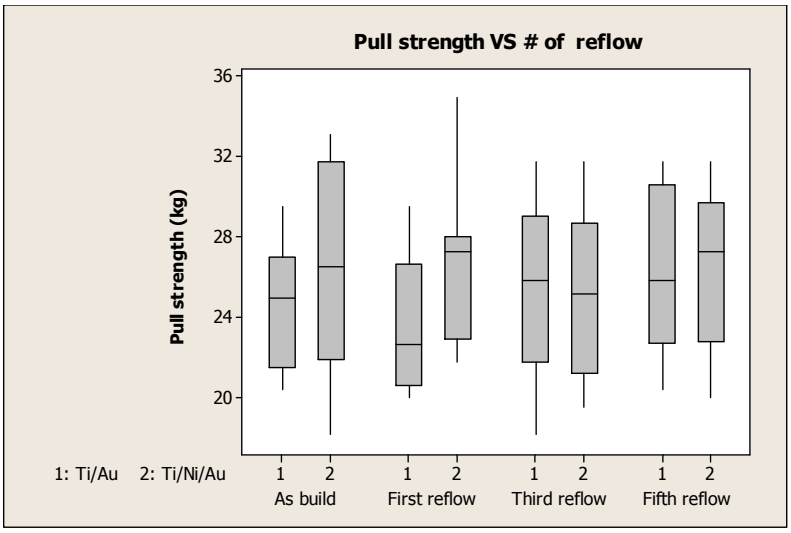


Figure 3.29. Die pull strength as a function of reflows for Ti/Ni/Au and Ti/Au 3000Å metalized die.

The aging temperature was raised to 120°C to accelerate the test. Figure 3.30 plots the shear test results after aging. There was no significant degradation in shear strength after 1000 hours of aging for assemblies with both Ti/Ni/Au and Ti/Au die. Die pull test were also performed as a function of 120 °C aging (Figure 3.31). There was no significant variation in the average pull strength after 1000 hours of aging for assemblies with both metallizations. The median pull strength of Ti/Ni/Au was slightly higher than for Ti/Au.

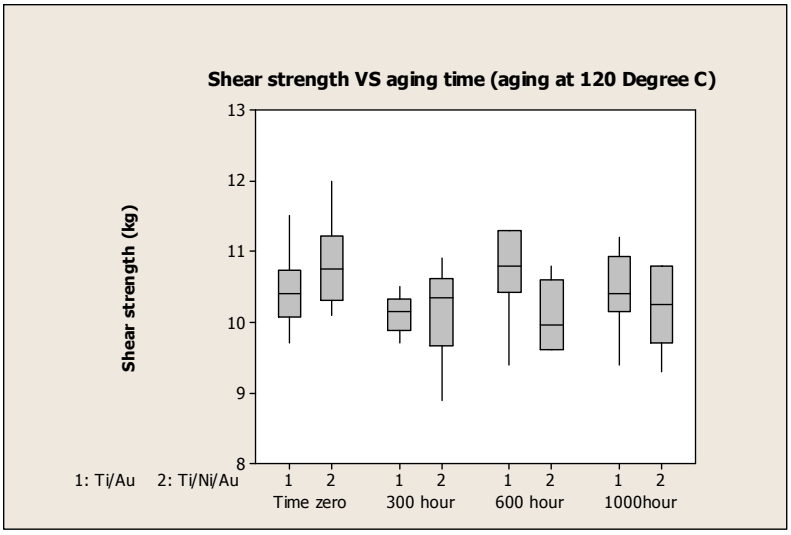


Figure 3.30. Die shear strength as a function of aging at 120°C for Ti/Ni/Au and Ti/Au 3000Å metallized die.

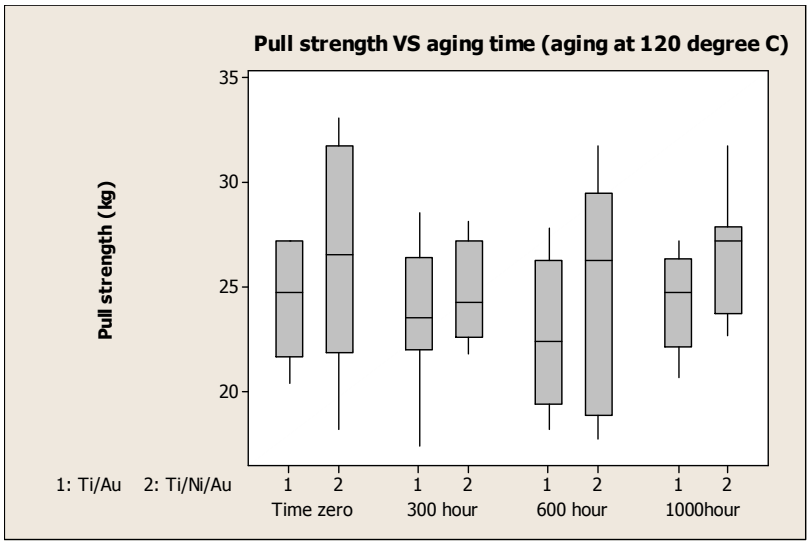


Figure 3.31. Die pull strength as a function of aging at 120°C for Ti/Ni/Au and Ti/Au 3000Å metallized die.

The thermal shock cycle test profile was from -40 °C to +85 °C, with 10 minutes dwell at each temperature extreme and a transition time of 10 seconds. Figures 3.32 to 3.39 shows examples of C-SAM images for assemblies after 2X lead free reflows then

500, 1000 and 2000 air-to-air thermal shock cycles. The assembly was Cu (24mm x 24mm x 1mm) on Si (22mm by 22mm). There was no delamination for both Ti/Au and Ti/Ni/Au based assembly after the initial 2X reflows (Figures 3.32 and 3.33) or after 500 cycles (Figures 3.34 and 3.35). After 1000 cycles, slight edge delamination was observed (Figures 3.36 and 3.37) with both die metallurgies. The edge delamination occurred at the die - indium interface. After 2000 cycles, delamination progressed with both die metallurgies (Figures 3.38 and 3.39). There was no significant thermal shock reliability difference between assembly with Ti/Ni/Au and Ti/Au (3000 Å) die.

Figure 3.32. C-SAM for assembly with Si (Ti/Au) after 2X reflows.

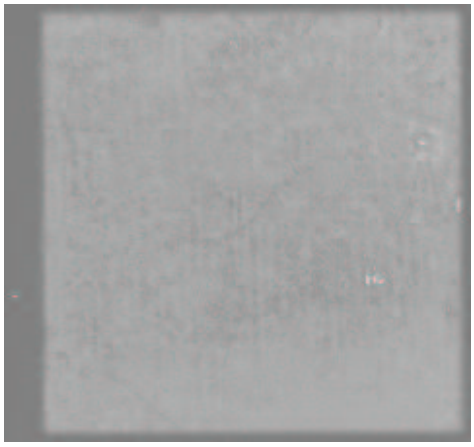


Figure 3.33. C-SAM for assembly with Si (Ti/Ni/Au) after 2X reflows.

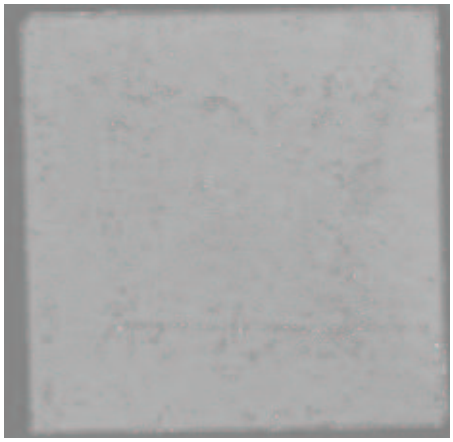


Figure 3.34. C-SAM for assembly with Si (Ti/Au) after 500 thermal shock cycles.

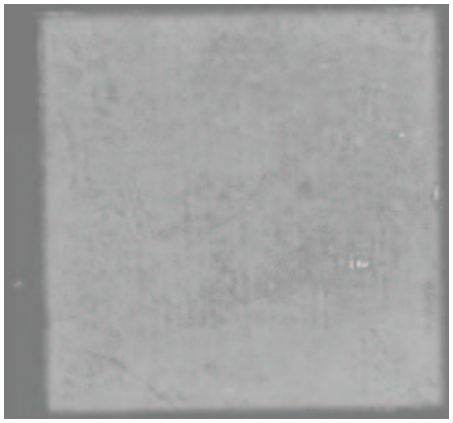


Figure 3.35. C-SAM for assembly with Si (Ti/Ni/Au) after 500 thermal shock cycles.

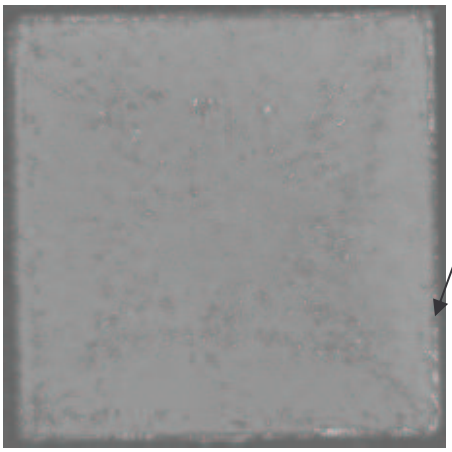


Figure 3.36. C-SAM for assembly with Si (Ti/Au) after 1000 thermal shock cycles.

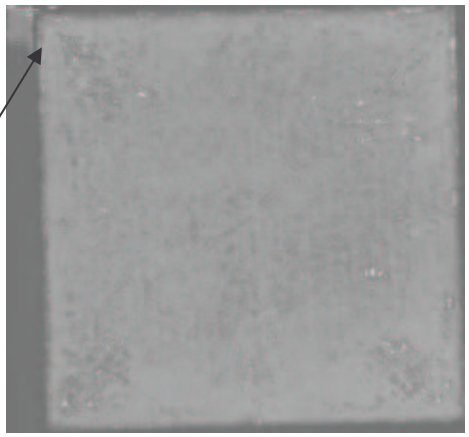


Figure 3.37. C-SAM for assembly with Si (Ti/Ni/Au) after 1000 thermal shock cycles.

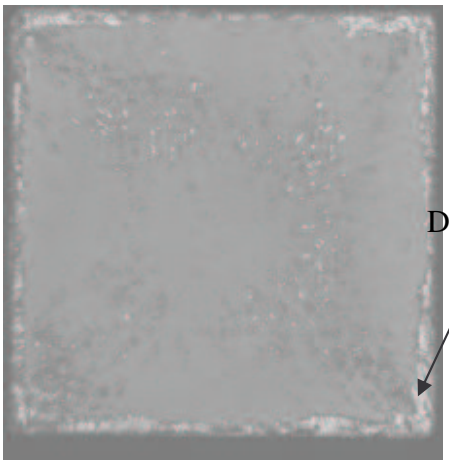


Figure 3.38. C-SAM for assembly with Si (Ti/Au) after 2000 thermal shock cycles.

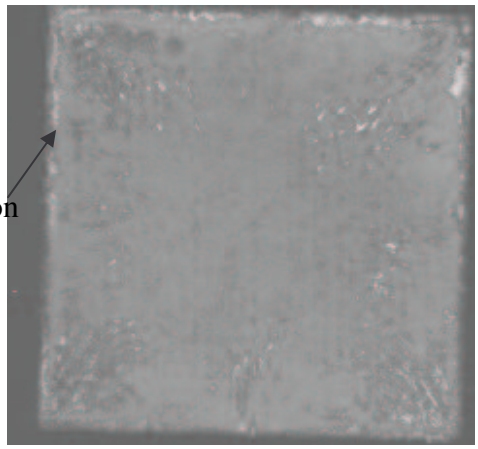


Figure 3.39. C-SAM for assembly with Si (Ti/Ni/Au) after 2000 thermal shock cycles.

3.7 Chapter Summary and Analysis

This chapter first reviewed die metallizations studied in the literature for indium soldering. A layer of barrier metal (Ni, for example) is typically used in between the top anti-oxidization (Au) layer and the bottom adhesion layer to the die. It is commonly believed that a minimum thickness of this layer is needed in order to make sure during soldering and the following solder joint service life time, this layer of metal is not consumed. When it is consumed, dewetting or severe solder joint reliability degradation will typically occur, however, in this study, it was found that Ti/Au (3000 Å) thin film die without the Ni layer can yield a similar indium solder joint reliability as that with the Ni layer.

Die metallization Ti/Au thin film was evaluated with a vacuum soldering process. It was found that during indium soldering, the Au thin film was converted to $AuIn_2$ IMC completely and there was no IMC formation between In and Ti, however, the attachment

had significant shear and pull strength and the attachment strength was not degraded significantly by multiple lead free reflow or thermal aging testing.

Assemblies (Cu on Si) with die Ti/Au (2000 Å) showed early delamination during the thermal shock cycle test. The Au thickness effect was further evaluated. Assemblies (Cu on Si) with Ti/Au (2000 Å) die had lower shear strength compared with Ti/Au (3000 Å) and Ti/Au (4000 Å) die based assemblies. The pull strength (Si on Si) increased with increasing gold thickness. The major difference between assembly (Si on Si) with 3000 Å and 4000 Å Au was that 3000 Å based assembly had a small area fraction of voids. Examination of the pulled fracture surface revealed the void extended to the Si die surface. EDS analysis identified Ti at the void interface to the Si die, indicating the Au was dissolved during the soldering process. The cause of the voids was not determined. For Ti/Au (4000 Å) based assembly (Si on Si), a pull test model was constructed and it was found that the joint produced had much higher pull strength than reported in reference [55].

Ti/Au (3000 Å) die were used for the next round evaluation, since it had similar shear strength to the Ti/Au (4000 Å) die. The test results were that Ti/Au (3000 Å) die had similar multiple lead free reflows, thermal aging and thermal shock cycle reliability with Ti/Ni/Au die. There was no early delamination during the thermal shock cycle test. The higher joint shear strength was believed to be responsible for the improvement of the thermal shock cycle reliability.

CHAPTER 4 ADHESIVE BASED HEAT SPREADER ATTACHMENT

4.1 Introduction

For medium to high (~<100W) power applications, a filled silicone based TIM for large die flip chip package heat spreader attachment was evaluated. The filler was used to improve the silicone's thermal conductivity. Silicone materials are compliant and are good choices for handling stress due to the CTE mismatch between the copper heat spreader and the silicon die. A flat heat spreader was selected, since it costs less than a heat spreader with a flange. To provide additional mechanical support at the corners of the heat spreader, a non-thermally conductive silicone adhesive was dispensed and co-cured with the TIM. The attachment process and reliability were investigated.

4.2 Materials and Process

The test vehicle was a flip chip die (22mm x 22mm) assembled on a multilayer ceramic (50mm x 50mm x 1mm) substrate. The flat Ni coated copper heat spreader was 48mm x 48mm x 1mm in size. The heat spreader also had a layer of Si_xO_y on its top surface, which was found by the sponsor to have better adhesion with the TIM material selected. There were pads for decoupling capacitor mounting on the ceramic substrate. A silicone based thermally conductive adhesive DA6534-X (Table 4.1) was dispensed on the die backside and another non-thermally conductive silicone adhesive GE TSE3212

(Table 4.2) was dispensed at the four substrate corners to provide corner support for the heat spreader.

Viscosity	Thermal conductivity	Moisture uptake (85C/85%RH/72hr)	Lap Shear Strength (Al)	Modulus (25C)
42 Pa.s	6.0W/mK	0.03 wt%	130 N/cm2	70 MPa

Table 4.1. Properties of TIM DA6534-X.

Viscosity	Thermal conductivity	Adhesive Strength	Tensile Strength
280 Pa.S	0.29 W/mK	2.6MPa	3.7MPa

Table 4.2. Properties of reinforcement silicone GE TSE3212.

There were five basic manufacturing requirements for this heat spreader attachment:

1. The substrate corner adhesive standoff should be higher than 1.65mm as-dispensed in order to contact the heat spreader when placed.
2. The width of the substrate corner adhesive should not exceed 7.5mm in order not to contact the chip capacitors.
3. The thermal adhesive should cover the entire die backside surface after heat spreader placement.
4. The thermal adhesive should not bleed or squeeze out from the die beyond 3.5mm in order not to touch the chip capacitors.
5. The attachment process needs to be void free.
6. Bond line thickness of 100µm.

The thermal adhesive was dispensed as one bigger center dot and four smaller corner dots 3mm away from die corners (Figure 4.1). The small dots help to ensure the die corners were completely covered with TIM after heat spreader placement.

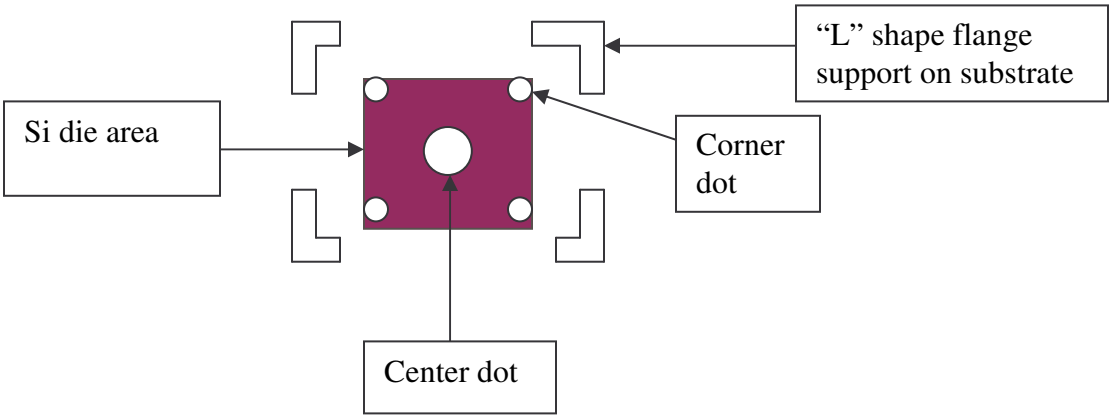


Figure 4.1. Dispense pattern (Drawn not to scale).

The adhesive flow after heat spreader placement was inspected by placing a glass slide and visual inspection. This can help tune the dispense and attachment process parameters to get the proper amount of dispensed material and a void free attachment process. The "L" shaped flange support adhesive was dispensed along the four corners of the substrate, 3.5mm away from the chip capacitor sites. The corner adhesive dispense parameters were set by measuring the resulting adhesive height. The following dispense parameters were set:

Dispense parameters for TIM corner dots:

1. Dispense height: 1mm
2. Dispense time: 1sec
3. Location: 3mm off die edge

Dispense parameters for TIM center dot:

1. Dispense height: 3mm
2. Dispense time: 9 sec

Dispense parameters for flange support:

1. Dispense height: 2mm
2. Dispense speed: 2.5mm/sec
3. Dispense length: 12mm
4. Dispense location: 3.5 mm off chip capacitor pads

Needle size: 1.2 mm diameter

Pressure: 40 PSI

For all dispense patterns

With the dispense parameters established, the two adhesives were dispensed and the Cu heat spreader was placed with a force of 660 grams and a dwell time of 30 seconds. Higher placement forces can be used to achieve shorter placement times. After placement, the adhesives were co-cured at 150°C for one hour. The corner flange support adhesive remained 1-2mm away from the chip capacitor sites after cure. The resulting TIM bond line thickness ranged from 85µm to 100µm measured from cross sectioned samples.

4.3 Reliability Evaluation

Test parts were subjected to a sequential series of assembly and environmental exposures:

- 2X reflow (lead free – Figure 3.10)
- 30° C/60%RH soak for 96 hours
- 3X reflow (lead free – Figure 3.10)
- 500 hours aging at 100°C
- 500 thermal shock (air-to-air) cycles (0ºC to 100ºC, dwell 15 minutes at each temperature with 10 second transition time)

Delamination and pull strength were the two reliability evaluation criteria. Dye penetration followed by heat spreader pull testing was used to check the delamination status as a function of stress testing. The procedure used for dye penetration was:

(1) soak the assembly in the dye (Steel Red Layout Fluids from DYKEM) for eight hours

(2) dry the soaked assembly in air four 24 hours.

JB- weld epoxy was used to mount the assembly for pull testing with the Instron machine.

The test results showed there was only a slight decrease in heat spreader pull strength after sequential assembly and environmental stress exposure (Figure 4.2). Figure 4.3 shows that there was no delamination (no dye penetration into adhesive-to-substrate, adhesive-to-die or adhesive-to heat spreader interfaces) after environmental stressing.

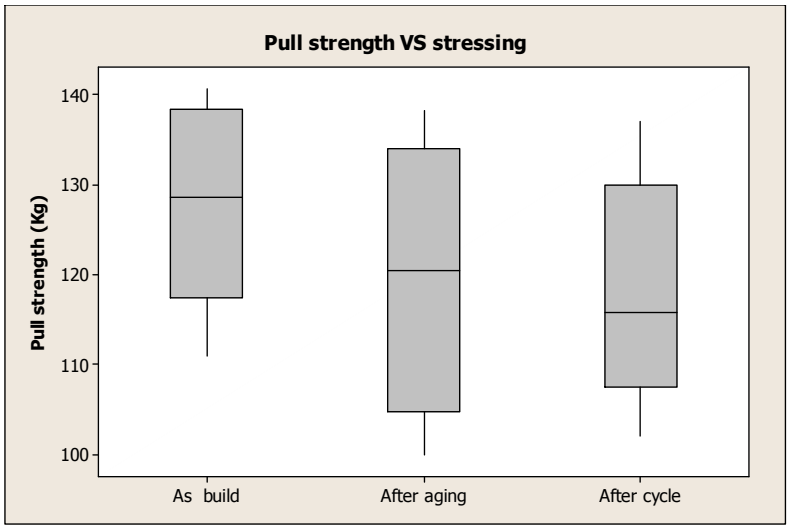


Figure 4.2. Heat spreader pull strength as a function of sequential environmental stress exposures.

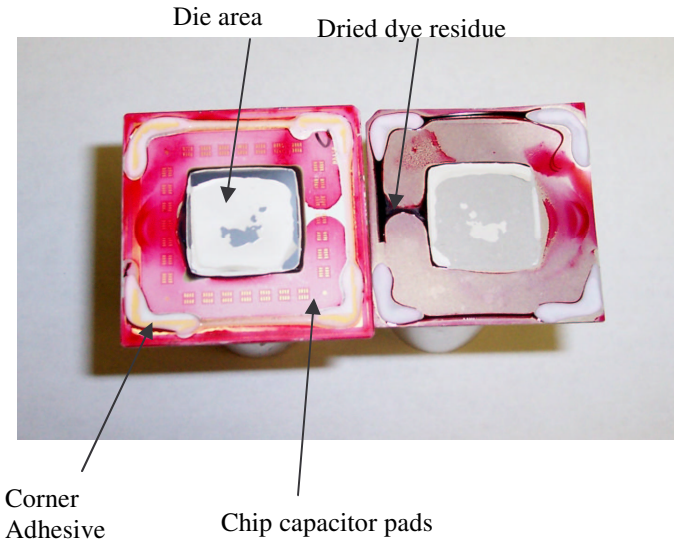


Figure 4.3. Pull test failure surfaces after the complete series of exposures.

4.4 Chapter Summary

In this chapter, a thermal conductive silicone was used as a TIM for large die (22mm x 22mm) flip chip in ceramic package heat spreader attach. Since the heat spreader was selected to be flat for cost reduction, another co-cure-able non-thermally

conductive silicone was applied between the substrate and the heat spreader as flange reinforcement.

The manufacture process was developed and the resulting structure was subjected to sequential assembly and environmental stress tests. There was no interfacial delamination and no significant pull strength degradation after stress testing.

CHAPTER 5 CONCLUSIONS AND FUTURE STUDY RECOMMENDATIONS

5.1 Lead Free Flip Chip Packaging with A Small Ni Containing Solder Joint

A small amount of Ni was introduced into the final flip chip lead free solder joint by bumping the Sn finished substrate pad with Sn/1%Ag/0.5%Cu/0.05%Ni solder paste. Solder on pad (SAC105) was used as control. Flip chip die bumped with SnAg eutectic solder was used for assembly on the two groups of substrates. The bumped die assembly on bumped (dome shape) substrate was successfully demonstrated. Thermal shock reliability test and failure analysis were performed. The small amount of Ni from the bumping paste was concentrated at the substrate side IMC layer, forming $(Cu,Ni)_6Sn_5$, but this did not measurably impact the solder joint thermal shock reliability.

5.2 Metallization and Indium Solder Based Flip Chip in Package Heat Spreader Attach

This part of study first reviewed die metallizations reported in the literature for indium soldering. A layer of metal (Ni, for example) is typically used in between the top Au anti-oxidization layer and the bottom adhesion layer to the die. It is commonly believed that a minimum thickness of this layer is needed in order to make sure during soldering and the following solder joint service life time, this layer of metal is not consumed, otherwise, dewetting or severe solder joint reliability degradation will

typically occur. However, in this study, it was found that Ti/Au (3000 Å) thin film die without the Ni layer can yield a similar indium solder joint reliability as that with the Ni layer.

A low voiding process was developed for indium based heat spreader attachment using vacuum soldering. Die metallized with Ti/Au thin film was studied for indium soldering. It was found that the Au thin film was consumed by the indium during soldering and there was no IMC formation between In and Ti, however, the attachment had significant shear and pull strength and the attachment strength was not degraded by multiple lead free reflow or thermal aging testing.

Ti/Au (2000 Å) die based heat spreader attach (24mm x24mm Cu on 22mm x 22mm Si) showed early delamination compared with Ti/Ni/Au die based assembly after thermal shock cycle test. The effect of Au thickness was evaluated. The major difference between assembly (Si on Si) with 3000 Å and 4000 Å Au was that 3000 Å based assembly had a small percentage voids. Those voids area had Ti pull fracture surface and decreased the assembly pull strength. The cause of the voids was not determined. A model was constructed and it was found that the joint produced with 4000 Å Au die had much higher pull strength than that produced in reference [55].

Ti/Au (3000 Å) die were used for the next round of evaluations, since it had similar shear strength with Ti/Au (4000 Å) die and the solder joint will be in shear stress during the thermal shock cycle testing. The result was that Ti/Au (3000 Å) die had similar multiple lead free reflow, thermal aging and thermal shock reliability to the Ti/Ni/Au die.

5.3 Adhesive Based Heat Spreader Attach

A thermally conductive silicone thermal interface material was selected for large die 22mm x 22mm flip chip in package heat spreader attachment. Since a flat heat spreader was selected for cost reduction, another co- cure-able non-thermally conductive silicone was applied between the substrate and heat spreader as reinforcement.

The manufacture process was developed and the resulting structure was subjected to sequential assembly and environmental tests. There was no interfacial delamination and no significant pull strength degradation after stress testing.

5.4 Recommendations for Future Work

Ti/Au (4000 Å) die showed higher pull strength than the Ti/Au (3000 Å) die, even though both had similar shear strength. It is recommended to further evaluate the reliability of Ti/Au (4000 Å) die for heat spreader attachment, especially for attach with a flange heat spreader, where the joint will experience complex tensile and shear stress during thermal shock cycle testing. The origin of the voids in the 3000 Å Au sample should be explored.

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