Electrical properties of MOS devices fabricated on 4H Carbon-face SiC

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Zengjun Chen

Certificate of Approval:

Jianjun Dong
Associate Professor
Physics

John R. Williams, Chair
Walter Professor
Physics

Minseo Park
Associate Professor
Physics

Chin-Che Tin
Professor
Physics

George T. Flowers
Dean
Graduate School

# Electrical properties of MOS devices fabricated on 4H Carbon-face SiC

Zengjun Chen

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Doctor of Philosophy

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Zengjun Chen



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Signature of Author

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Date of Graduation

# Vita

Zengjun Chen, Son of Mantun Chen and Huyou Wang, was born on August $1^{st}$, 1978, in Linyi, Shanxi Province, People's Republic of China. He entered Xi'an Jiaotong University, Xi'an, Shaanxi Province, P.R.China in September, 1996 and earned a Bachelor of Science degree majoring in Applied Physics from Physics Department in July, 2000. He then entered Fudan University, Shanghai, P.R.China in September, 2000. In July, 2003, he earned a Master of Science degree majoring in General Physics from the Institute of Modern Physics of Fudan University. He entered the graduate program in Physics Department of Auburn University in August, 2003 and worked as a Graduate Teaching Assistant and later as a Graduate Research Assistant in the Silicon Carbide Research Group under the supervision of Professor John R. Williams. He married Yanling Ma in Lucheng, Shanxi Province, P.R.China on December $25^{th}$, 2003, and his daughter, April M. Chen was born on October $2^{nd}$, 2008 in East Alabama Medical Center, Opelika, Alabama.

Dissertation Abstract

Electrical properties of MOS devices fabricated on 4H Carbon-face SiC

Zengjun Chen

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Silicon-based devices are still the mainstay of the electronics industry with applications ranging from small chips in personal computers to large, high power switching devices. However, Si has faced grater and greater challenges for applications at high frequency, high voltage, and in high temperature environments. In order to work under these demanding conditions, silicon-based devices must be used with cumbersome expensive cooling systems and electrical snubbers that add to circuit complexity for switching applications. Solutions for these problems have been sought for years and one potential solution is the replacement of Si with a wide band-gap semiconductor material such as silicon carbide (SiC).

It has been over 20 years since research groups started to investigate SiC as the candidate to replace silicon. Many advantages of SiC over silicon have been well recognized. Its wide band-gap (3.3eV vs. 1.1eV for silicon) allows SiC to operate at higher temperature. The high thermal conductivity (3.7W/cm-K vs. 1.5W/cm-K for silicon) can significantly reduce the amount of cooling power required in a system. In addition, SiC has a high

electric breakdown field (2.1MV/cm vs. 0.3MV/cm for silicon), which enables SiC to block the same voltage as Si with a 7 times thinner layer, thereby providing a much lower drift resistance for drift layer of similar doping concentration. Moreover, among the wide band gap semiconductors, a unique property of SiC is its native oxide is $SiO_2$, which is the same as the native oxide of Si. This implies that the current silicon MOS device technology can be adopted for SiC MOS device fabrication without much effort in the development of new processing methods.

Despite all these advantages, the realistic applications of SiC in industry have been hindered by some of its disadvantages. Silicon carbide's crystal quality is still not as good as that of silicon. Defects like micropipes and dislocations contribute to less than optimum breakdown characteristics SiC-based MOS devices. More importantly, although the bulk electronic mobility of 4H-SiC is comparable to that of silicon (1000$cm^2$/V-s vs. 1400$cm^2$/V-s), MOSFET inversion channel mobility is much lower - currently 50$cm^2$/V-s compared to 700$cm^2$/V-s. This low channel mobility is caused largely by a high trap density at the 4H-SiC/$SiO_2$ interface.

With its advantages and disadvantages, SiC has been widely investigated. Among many polytypes of SiC, 4H-SiC attracts much interest because this polytype has the largest band-gap energy and a high bulk, almost isotropic bulk mobility. The $(000\bar{1})$ or carbon-terminated face 4H-SiC has been much less studied than the (0001) Si-terminated face. However, the carbon face 4H-SiC has a higher oxidation rate ($\times 9$ higher), which can significantly reduce the fabrication time for SiC MOS devices. Furthermore, Fukuda *et al.* reported high

inversion channel mobility on the carbon face 4H-SiC*. Such characteristics would make the carbon face 4H-SiC an ideal candidate of power MOSFETs.

In this dissertation, the basic properties of SiC will be discussed in Chapter 1. The physics of MOS devices will be presented in Chapter 2, and the characteristics of SiC-based MOS devices will be discussed in Chapter 3. The processes and techniques used to fabricate SiC MOS devices will be described in Chapter 4. The results of measurements for MOS capacitors and MOSFETs fabricated on the 4H carbon face will be presented in Chapter 5 to provide an overview of $(000\bar{1})$ characteristics compared to (0001). Both implanted and epitaxial layers are used to build MOSFETs. The oxide layer is grown thermally in furnace at $1150^oC$, followed by post-oxidation annealing to passivate the O-S interface. High-purity Mo is sputtered as the gate metal, and source and drain ohmic contacts for the lateral test MOSFETs are produced by sputtering Ni on heavily implanted regions (nitrogen at $6\times19cm^{-3}$), followed by an anneal at $950^oC$ for 4min in Ar. Hi-lo capacitance-voltage measurements at both $23^oC$ and $300^oC$ are used to obtain the interface trap density ($D_{it}$). Current-voltage measurements at room temperature are used to collect information about oxide leakage and breakdown field ($E_{bd}$). A three-probe I-V system is employed to determine $I_d$-$V_g$ characteristics of the MOSFETs at room temperature, and the inversion channel mobility ($\mu$) is extracted from these characteristics.

Results are compared for different post-oxidation interface passivation anneals, with the combination of nitric oxide (NO) and $H_2$ giving the lowest trap density $D_{it}$ in the upper half of the band gap. Wet-reoxidation plus NO passivation produces the most reliable oxide, but the measured breakdown field of 6MV/cm is still approximately 2MV/cm lower than the

*K. Fukuda, M. Kato, S. Harada, K. Kojima, Mater. Sci. Forum., 527, 1043, (2006)

average field measured for the silicon face. Compared to the values reported by Fukuda, *et al.*, our low field mobility value is not remarkable. However, the high field mobilities are similar. It was observed that the presence of mobile ions can increase our low field channel mobility significantly. For example, after negative bias stress at 250$^o$C to remove possible mobile ions from the O-S interface, the mobility peak value drops from 65cm$^2$/V-s to 35cm$^2$/V-s. These results suggest that the effective channel mobility for the carbon face may not be significantly higher compared to the silicon face.

## Acknowledgments

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Last but not least, the author extends special thanks to his wife Yanling Ma for all her patience, understanding and moral support. The author also wants to thank his daughter, April, for bringing him so many pleasant moments. This dissertation is also dedicated to all his family members and friends.

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# Chapter 1

# Silicon Carbide Properties

Silicon carbide (SiC), also named by moissanite[1], is a compound of silicon and carbon. Compared to silicon, the current dominant semiconductor material in the industry, SiC has shown significant advantages in terms of the electrical properties. The wide band gap of SiC, 3.2eV versus 1.2eV of silicon, enables it to work at higher temperature. The high thermal conductivity of SiC, 3.7W/cm-K compared to 1.5W/cm-K of silicon, makes it an excellent material for heat management application. The high electrical breakdown field of SiC, 2.1MV/cm as opposed to 0.3MV/cm of silicon, can sustain high blocking voltage with employing a much thinner epi-layer. 4H-SiC, one of many polytypes of SiC, has a bulk electron mobility of 1000cm$^2$/V-s, comparable to silicon's bulk mobility (1350cm$^2$/V-s), leaving open the possibility of even high channel mobility. The native oxide of SiC is $SiO_2$, same as that of silicon, enabling the adoption of fabrication techniques from silicon industry. This unique property potentially saves money and effort for developing new procedures for SiC applications. In this chapter, an overview of the relevant properties will be presented and discussed.

## 1.1 Crystal Structure

SiC crystals exist in many polytpes, more than 250 polytypes have been reported. All polytypes share a hexagonal frame with a carbon atom situated above the center of a

triangle of silicon atoms and underneath a silicon atom belonging to the next layer. This framework is shown in figure 1.1. The distance between any two silicon atoms is 3.08Å. From geometrical relations, the distance between silicon atom and carbon atom is around 1.89Å.

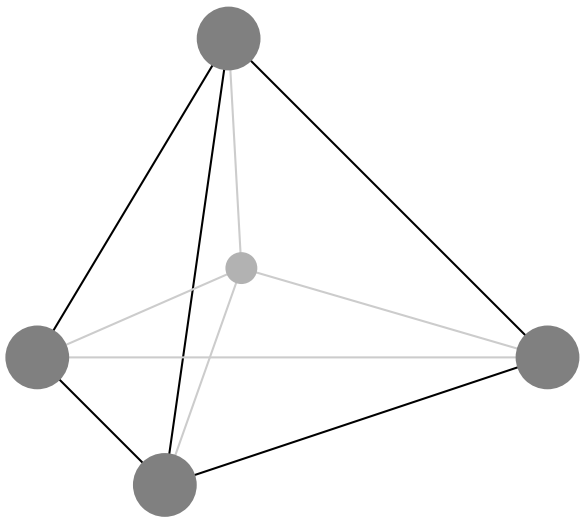

Fig. 1.1: The basic tetrahedron frame of SiC. Dark grey balls represent silicon atoms, light grey ball represents carbon atoms. The distance between silicon atoms and carbon atom is same.

In figure 1.1, a plane is formed by the three base silicon atoms, above this plane, the carbon atoms form another plane. The whole SiC crystal is constructed from silicon-carbon planes. The stacking style of silicon-carbon planes varies, and the variation defines the polytype of SiC crystal. Figure 1.2 shows the stacking sequences of several common polytypes. A, B, and C stand for the different distributions of the silicon-carbon bonds. If the stacking order is ABCABC..., the single crystal structure is named as 3C, where C denotes the cubic structure. For 4H single crystal, the stacking order is ABACABAC..., the H denotes a hexagonal structure. 4H-SiC will be the focus of discussion.

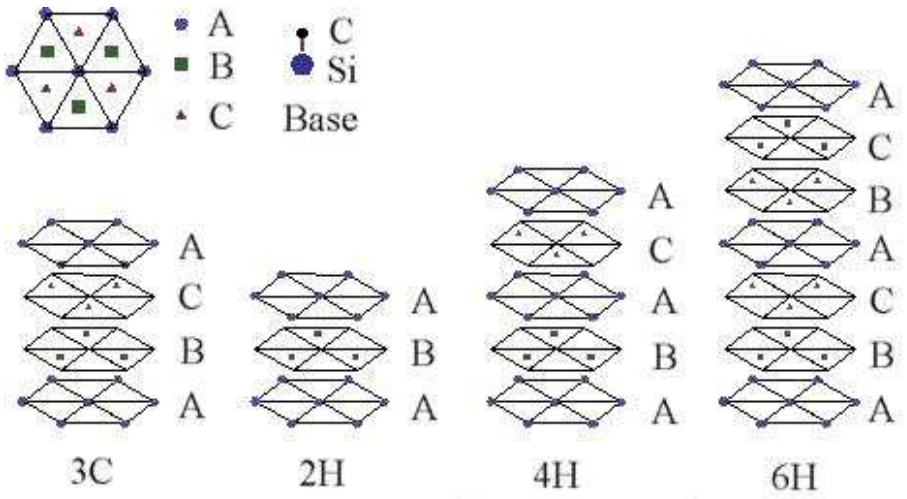


Fig. 1.2: Stacking sequence of several SiC polytypes.

To distinguish the different orientation of SiC crystal, miller indices are employed. 3C crystal uses 3 digits and hexagonal crystal uses 4 digits with the last one defining the direction of c-axis. In figure 1.3, the top surface represents (0001) and the bottom surface $(000\bar{1})$. The shadow surface is $(11\bar{2}0)$. In the surface of $(11\bar{2}0)$, the differences of stacking sequences of various polytypes can be seen, as shown in figure 1.4.

## 1.2 Crystal Growth

The most well-known crystal growth technique today is Czochralski method[2], growth of single crystal from the melt. Most silicon single crystal ingots are produced by this method. In this process, a seed crystal rod is dipped into molten high-purity silicon in a quartz crucible and then pulled up while rotating. A large diameter silicon single crystal ingot will be produced. Single crystal SiC, however, can not be produced by Czochralski method since SiC dose not melt at temperatures above $2000^oC$, but instead gradually sublimes[3]. Thermodynamic analysis of the possibility of single-crystal growth from the

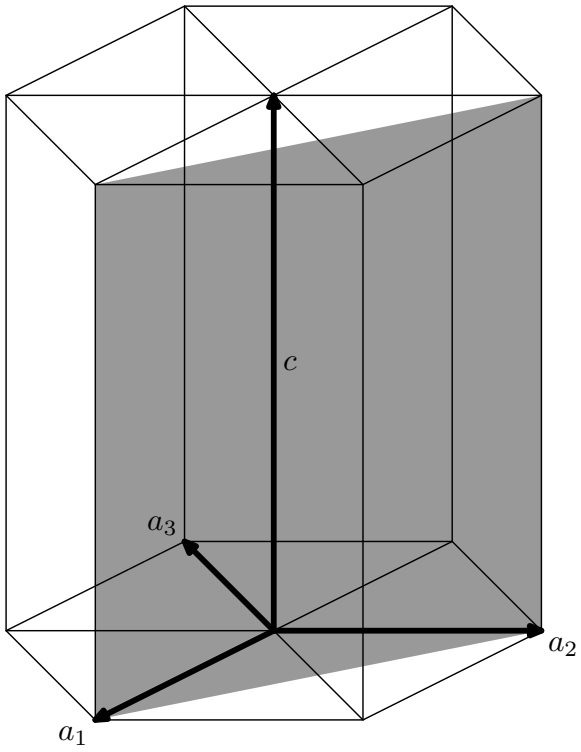


Fig. 1.3: Unit cell of hexagonal structure of SiC.

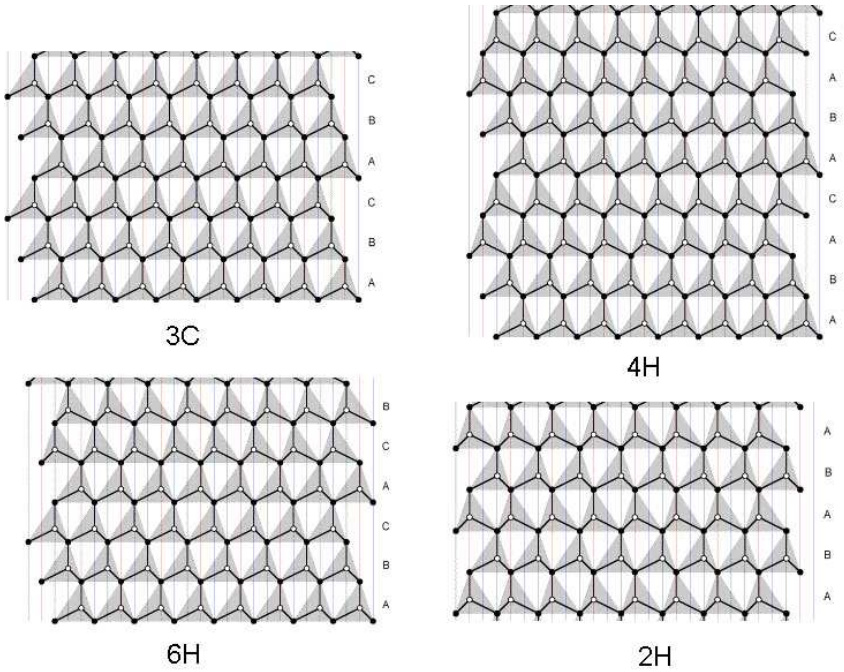


Fig. 1.4: Stacking sequence of several SiC polytypes in $(11\bar{2}0)$ face.

melt indicated that the intrinsic melt of SiC can exist at temperatures greater than 3190$^o$C and pressures greater than 104 MPa, which does not allow the commonly used grow-from-melt techniques for the production of SiC single crystals[4]. For materials with no congruent melting temperature or at least one component having too high a vapor pressure at the melting point, vapor phase growth methods are employed[5].

The first SiC was produced in 1890s by Acheson[5], who let silicon and carbon react at temperature higher than 2500$^o$C. It was Lely who first developed the sublimation method for SiC crystal growth in 1955. The schematic diagram of Lely growth method is shown in figure 1.5. The temperature in the crucible is 2500-2700$^o$C. Under the influence of temperature gradients, SiC or silicon and carbon penetrate through porous graphite and form SiC crystal in the shape of boules on inner walls of graphite. These single crystals are very pure and limited to small size. A large SiC single crystal was finally produced in

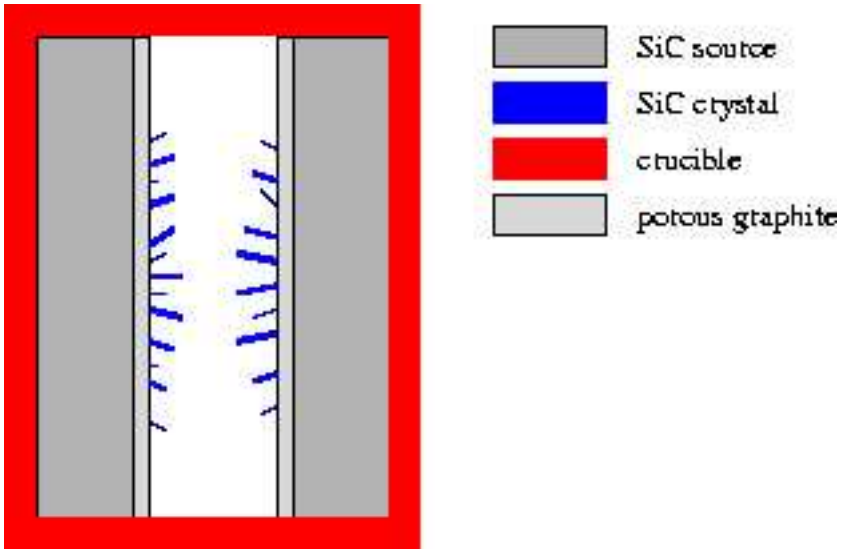


Fig. 1.5: Schematic diagram of Lely growth method[5].

the laboratory by Tairov and Tsvetkov by using seeded sublimation growth method (also

known as modified-Lely growth method)[6]. Their approach is shown in figure 1.6. Seeded sublimation growth places a single crystal seed inside the crucible. An advantage of seeded sublimation growth method over Lely growth method is better control of the nucleation process. Additionally, the crucible is filled with Argon, which helps control the diffusion process of Si-C gas species. The main reactions in the crucible are list below:

$$SiC(s) \leftrightarrow Si(g) + C(s) \tag{1.1}$$

$$2SiC(s) \leftrightarrow SiC_2g + Si(g) \tag{1.2}$$

$$SiC(s) + Si(g) \leftrightarrow Si_2C(g) \tag{1.3}$$

Meanwhile, since the crucible is composed of graphite, the following reactions between the silicon vapor and crucible also exist:

$$C(s) + 2Si(g) \Rightarrow Si_2C(g) \tag{1.4}$$

$$2C(s) + Si(g) \Rightarrow SiC_2(g) \tag{1.5}$$

The letters $g$ and $s$ in the parenthesis stand for gas and solid, respectively. As mentioned in section 1.1, SiC has many polytypes. During the single crystal growth, only the desired polytype is expected to be grown. In reality, many other polytypes may be simultaneously grown and they are considered to be defects in the host polytype semiconductor[5]. Figure 1.7 shows the relationship between the polytpe and the temperature of crystal growth. To achieve single-polytype single-crystal growth, the seed crystal must be pure and of the

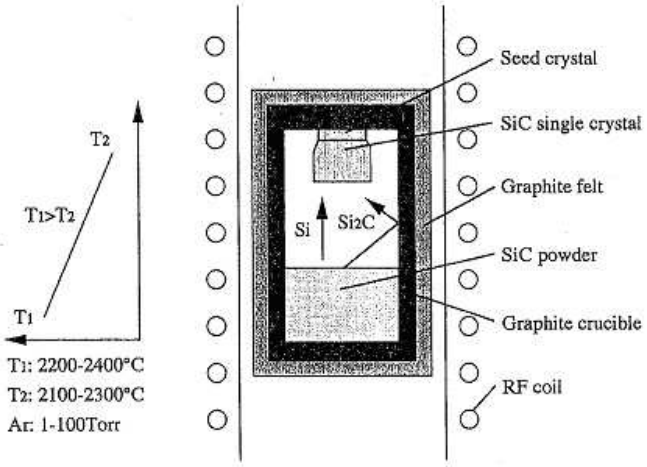


Fig. 1.6: Schematic diagram of seeded sublimation growth method[5].

desired polytype with excellent surface condition. Since polytypes other than that of the seed can easily be formed by phase transitions, the initial stage of crystal growth is critical and very important for polytype control[5]. It has also been shown that using a seed with a slight off-axis from the low-index (0001) plane and growth with a relatively slowly at initial stage improves the polytype control[7]. Another issue in crystal growth is the control

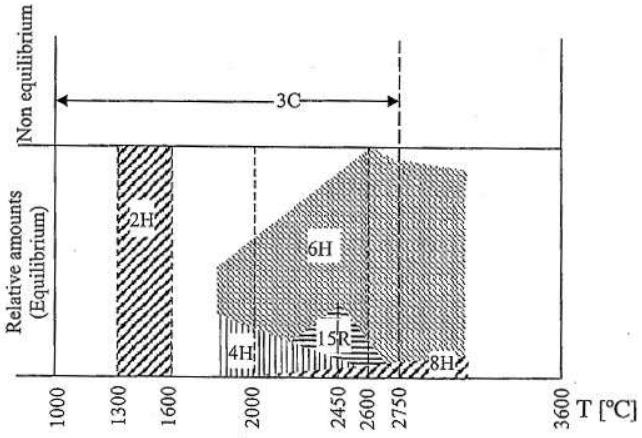


Fig. 1.7: Relationship between the polytype and the temperature of crystal growth[5].

of doping concentration. For SiC bulk doping concentration, which is generally very high, nitrogen and aluminum are used as n- and p-type dopants during the growth. For low-doping concentration, for instance, for an epitaxial layer, precise control is required to achieve accurate doping. Chemical vapor deposition (CVD) is commonly used as the method of epitaxial growth[8–10]. Dopants are added during CVD and diffuse into the epitaxial layer to obtain desired concentration. Other than CVD, molecular beam epitaxy (MBE) and liquid phase epitaxy (LPE) are also used for epitaxial growth[11–13] of compound semiconductors. Since diffusion in SiC is much more difficult than in silicon, ion implantation is also employed to dope epitaxial layer[14, 15].

### 1.3 Band Diagram

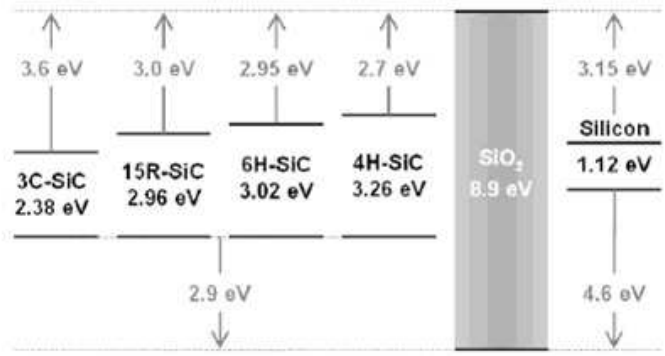


Fig. 1.8: The band gap information of several polytypes of SiC, comparing to that of silicon[16].

SiC is a wide band gap semiconductor material[17, 18]. Figure 1.8 shows the band gaps of the 4 commonly used SiC polytypes. For comparison, $SiO_2$ and silicon are presented.

It should be noted that the band gap depends on temperature and pressure. The values listed in figure 1.8 are measured at liquid helium temperatures. Of the polytypes of SiC,

4H has the widest band gap. Due to this property, devices fabricated on 4H-SiC are able to sustain a higher electric power. This property plus the fact that the native oxide of SiC is silicon dioxide leads to the expectation that 4H-SiC will be a suitable substitute for silicon in the production of power MOSFETs working in the harsh environments. Currently, the poor quality of $SiC/SiO_2$ interface hinders the transition from Si to SiC, which will be discussed later in this dissertation.

## 1.4 Defects in the Crystal

During the crystal growth process, the most easily or commonly produced defects are micropipes[19–22]. Micropipes are hollow tubes propagating the SiC crystal along the growth direction, *i.e.* c-axis. In most cases, the micropipes appear as the super-screw dislocations with a huge Burgers vector[23]. Putting SiC crystal in high-temperature Potassium hydroxide (KOH) liquid allows for visualization of the micropipes[24]. The formation of micropipes is shown in figure 1.9. During the crystal growth process, impurity particles may gather together at the surface of growing crystal, as the next SiC layer grows, the impurity particles will stop Si and C atoms from occupying their lattice sites. As more and more SiC layers are grown, there will be a repulsive force exerted by the edge of the SiC layer on the impurity particles. This force may lift up the impurity particles due to the weak bonding between the impurity particles and the SiC crystal. A hollow tube may be produced under the impurity particles. The moving process of the impurity particles may continue through out the growth. This model explains why most micropipes are along the crystal growth direction and have length equal to the height of the grown crystal[25].

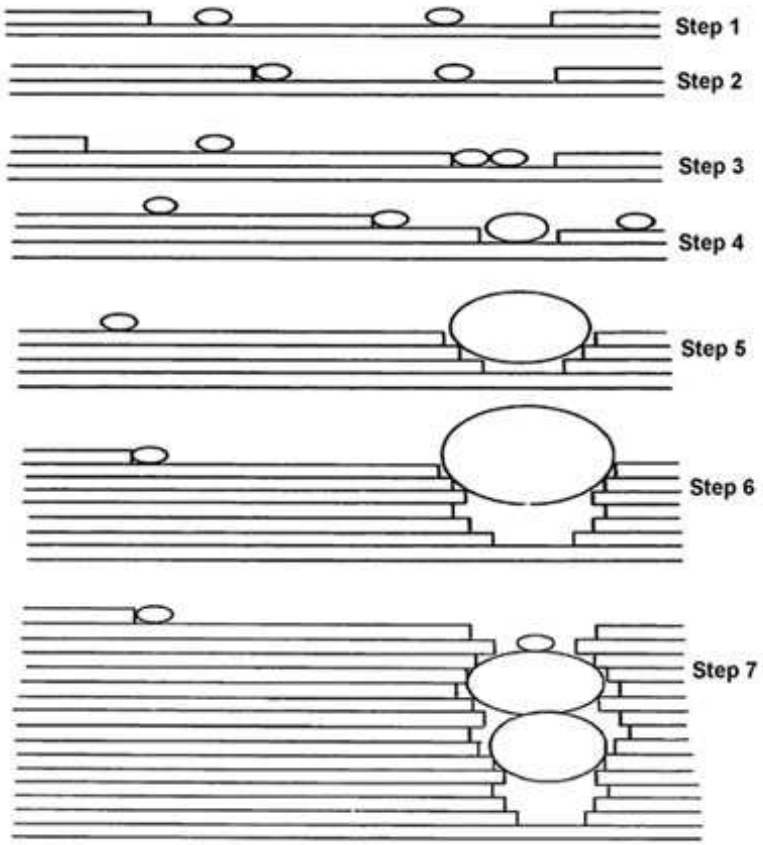


Fig. 1.9: A schematic illustration of the proposed micropipe formation mechanism[25].

The early stage of SiC crystal growth was also investigated to find the relationship between seed condition and micropipe formation in crystal. The micropipes in the seed continue to grow into the crystal, but no new micropipes would be generated[26]. If the seed surface is disintegrated by parasitic sublimation during the preheating stage of growth, micropipes may be generated[27, 28]. The temperature fluctuation in the growth chamber was found to be another cause of generation of micropipes[5].

In addition to micropipes, planar defects, grain boundaries, dislocations and stacking faults are also defects existing in SiC[24, 29–31]. Planar defects are hexagonal voids or tubelike cavities. They are several hundreds microns in width and five to twenty-five microns in thickness along the c-axis[32]. Grain boundaries occur at the places where two polytypes are grown and they appear as line of etch pits after KOH etching. Dislocations are of importance because they are electrically active defects significantly degrading device performance. KOH etching is also used to reveal dislocations. Stacking faults only happen when crystal is grown perpendicularly to the c-axis and they appear as linear etch pits in the basal plane.

## 1.5 Physical and Electronic Properties

SiC has many excellent physical and electrical properties. Table 1.1 shows the relevant parameters. For comparison, the same parameters of several other semiconductor materials are provided.

From table 1.1, the following conclusions may be drawn about SiC.

1. The wide band gap is the most promising characteristics of SiC. This makes it possible for SiC-based devices to sustain a higher working voltage, as required by power MOSFETs.

Table 1.1: Physics properties of several important semiconductors

| Materials | Si | 4H-SiC | 6H-SiC | GaAs | GaN(Wurtzite) |
|---|---|---|---|---|---|
| Lattice $\alpha$[Å] | 5.43 | 3.08 | 3.08 | 5.65 | 3.189 |
| Lattice $c$[Å] | - | 10.07 | 15.12 | - | 5.185 |
| Bond length[Å] | 2.35 | 1.89 | 1.89 | 2.45 | 1.95 |
| Density[gm/cm$^3$] | 2.32 | 3.16 | 3.16 | 5.3 | 6.09 |
| Therm. cond.$[W/cm-K]$ | 1.5 | 3.7 | 3.7 | 0.46 | 2.3 |
| Melting point[$^o$C] | 1420 | 2830 | 2830 | 1240 | 2500 |
| Debye temperature$[K]$ | 640 | 1300 | 1200 | 360 | 600 |
| Young's modulus$[Gpa]$ | 47 | 100-750 | 488 | 85.5 | 330 |
| Band gap$[eV]$ | 1.12 | 3.26 | 3.03 | 1.43 | 3.457 |
| Bulk elec. mob.$[cm^2V^{-1}S^{-1}]$ | 1400 | 1000 | 400 | 8500 | 500 |
| Bulk hole mob.$[cm^2V^{-1}S^{-1}]$ | 480 | 115 | 90 | 400 | 80 |
| Elec. breakd. field$[MV/cm]$ | 0.25 | 2.2 | 2.4 | 0.4 | - |
| Dielectric constant$[\epsilon_s/\epsilon_o]$ | 11.7 | 6.5-6.7 | 6.5-6.7 | 12.5 | 10 |
| Satur. elec. drif. velo.$[cm/s]$ | 1x10$^7$ | 2x10$^7$ | 2x10$^7$ | 1x10$^7$ | 1x10$^7$ |

2. By comparing Young's modulus, SiC is a stiffer material when compared to silicon. Considering carbon atoms are lighter than silicon atoms, it can be implied that the thermal conductivity of SiC is higher than that of silicon[16].

3. High saturated electron drift velocity enables SiC microwave devices to operate at higher cut-off frequencies[33].

4. High thermal conductivity enables devices based on SiC to transfer heat faster than devices based on silicon, therefore reducing the cost on heat management.

5. Significantly high electron breakdown field allows the thinner SiC power devices to handle high blocking voltage. Figure 1.10 shows the cross sectional view of a vertical diffused MOSFET (VDMOSFET). VDMOSFET is a type of power MOSFET, which requires to

handle high blocking voltage, and still have smaller power loss at the same time. A trade-off exists due to the fact that higher blocking voltage needs a thicker epi-layer and lower doping concentration. A thicker epi-layer and lower doping concentration will lead to higher drift resistance $R_{Dr}$, which is one part of on-resistance when power MOSFET is working. The total on-resistance can be approximated by the following equation: $R_{on} \approx R_{ch} + R_{Dr}$, where $R_{ch}$ is the channel resistance. Although several other resistances also contribute to the total on-resistance, for example, contact resistance and access resistance (the resistance when current flows out from channel and changes from horizontal direction to vertical direction), the channel resistance and drift resistance are the two largest components. Consequently the on-resistance will be higher. Because power loss during the operation of MOSFET is $P_{loss} = I_{sd}^2 \times R_{on}$, the power loss will also be higher. This trade-off can be changed when SiC is used to be the substrate. Considering $R_{on}$ is proportional to specific on-resistance $r_{on}$, and $r_{on} = \frac{V_{blocking}^2}{\mu E_c^3}$, where $\mu$ is the bulk electronic mobility of semiconductor. If the blocking voltage does not change, given that bulk electronic mobility of SiC and silicon are comparable and electron breakdown field of SiC is 7 times higher than that of silicon, the specific on-resistance of SiC will be 0.3% of that of silicon. This will make power loss of MOSFET fabricated on SiC much smaller than that fabricated on silicon. This also implies that SiC MOSFET can be much thinner than silicon MOSFET but equally safe.

6. Small dielectric constant provides low parasitic capacitance and higher operating speed for MOS devices[34].

These attractive properties have led to rapid development of SiC as a material and its device technology over the past 10 years[35]. For instance, Schottky diodes have been available commercially for years[36]. According to Cree, power MOSFETs are scheduled to

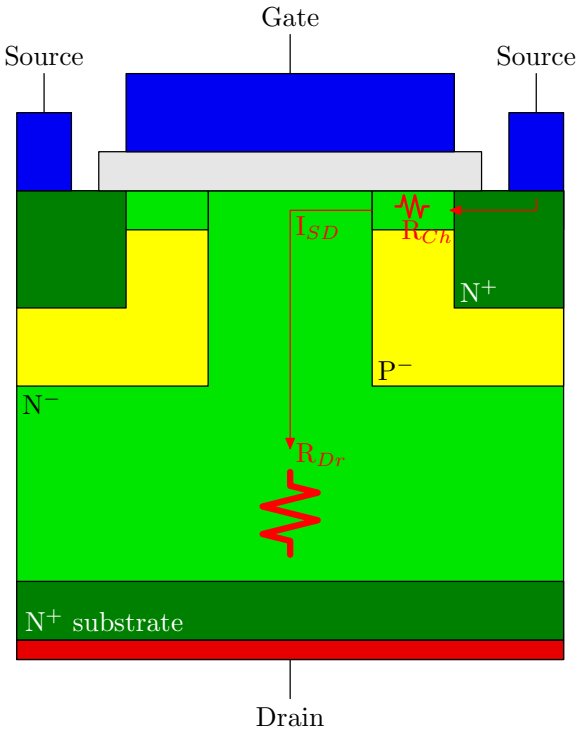


Fig. 1.10: Cross sectional view of a vertical diffused MOSFET.

be introduced in mid-2009. Bipolar transistors are expected to be available in the market within three to seven years. The future of SiC power devices appears bright[36].

# Chapter 2

## Physics of Metal-Oxide-Semiconductor Devices

The metal-oxide-semiconductor or MOS structure is the most important and most commonly used structure in modern microelectronics[37]. A more general definition is MIS or metal-insulator-semiconductor. Since it is used extensively in devices and integrated circuits, the MOS structure has been extensively studied[38]. Although the concept of MOS was proposed in Lilienfeld's patent in 1926[39], the first real working MOS device was demonstrated by Atalla and Kahng in 1959[40, 41]. Today, the most successful, ideal and practical MOS structure is Metal-Si-SiO2 system.

In this chapter, two important MOS devices, the MOS-Capacitor and the MOSFET will be discussed. Ideal devices will be discussed first,and electronic characteristics of real devices will be reviewed as well.

### 2.1 MOS-Capacitors

The MOS capacitor has been the most useful device in the study of oxide-semiconductor surface, which is important for device reliability and stability[38].

#### 2.1.1 Ideal MOS-Capacitors

MOS capacitors refer to the devices with oxide layer sandwiched by a metal layer and a semiconductor layer. The structure of an MOS capacitor is shown in figure 2.1. Another

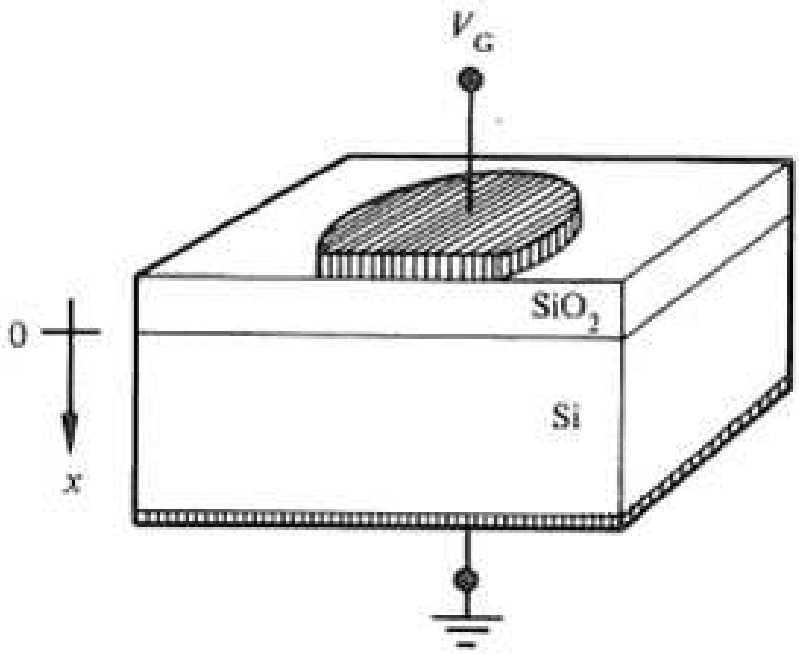


Fig. 2.1: A typical Metal-Oxide-Semiconductor capacitor structure[37]

metal layer, generally grounded, is put on the back of semiconductor material to be annealed as a low resistance ohmic contact. In an ideal MOS-capacitor, the oxide layer is a perfect insulator and has no mobile ions inside. The gate metal layer has to be thick enough to be an equipotential surface.

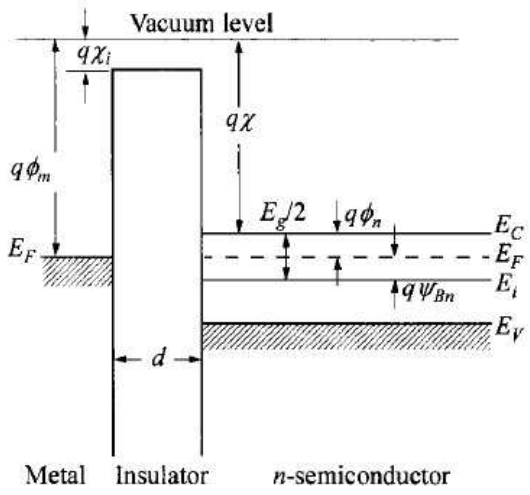


Fig. 2.2: The energy band diagram of an ideal MOS-capacitor.

With no gate voltage, $V_G$, applied, the energy band diagram of an ideal MOS-capacitor is shown in figure 2.2. Since the device must be in equilibrium, the Fermi energy levels of metal layer and semiconductor have to be aligned. If $V_G \neq 0$, Equation 2.1 can be used to describe the relationship between Fermi energy levels of the two sides,

$$E_F(metal) - E_F(semiconductor) = -qV_G \tag{2.1}$$

From Equation 2.1, if $V_G > 0$, Fermi energy level of metal layer will be lower than that of semiconductor; if $V_G < 0$, Fermi energy level of metal layer will be higher than that of semiconductor. For n-type semiconductor material, when $V_G > 0$, the MOS-capacitor will

stay in the accumulation state, and MOS-capacitor will be in depletion when $V_G < 0$. If $V_G$ is lower than a specific value, holes will appear at the interface of semiconductor-oxide. This state is called the inversion state. The situation will be opposite for p-type semiconductor material. Energy band diagrams of the three states for both p-type and n-type materials are shown in figure 2.3.

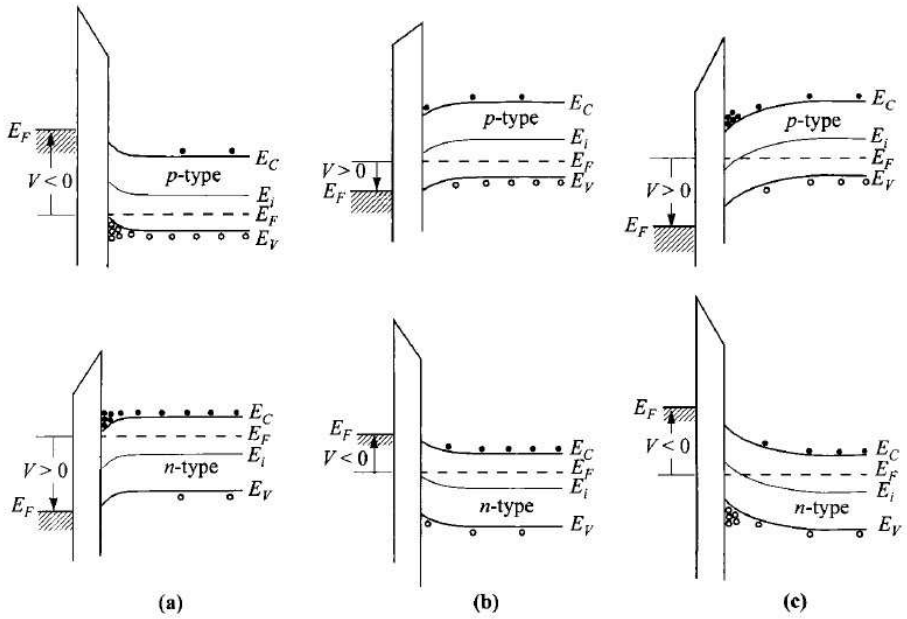


Fig. 2.3: The energy band diagrams of MOS-cpacitors at (a) accumulation, (b) depletion and (c) inversion regions. the upper row is p-type material and the lower row is n-type material[38].

To understand detailed characteristics of MOS-capacitors, capacitance-voltage characteristics are obtained and analyzed. The capacitance of an MOS-capacitor will change with respect to the applied gate voltage. The frequency of an AC probe voltage added to the DC gate voltage affects the measured capacitance, as well. Firstly, we consider the magnitude of the applied gate voltage. When $V_G$ is positive, the device stays in accumulation, which

means that electrons pile up in the semiconductor at the oxide-semiconductor interface. Because electrons are majority carriers in an n-type semiconductor, they can respond quickly with the change of voltage. Therefore, for all applied probe frequencies, the electrons can always follow the changing AC voltage. So the capacitance of the MOS-capacitor in accumulation will be equivalent with that of a parallel-plate capacitor. Equation 2.2 gives the capacitance expression,

$$C_o = \frac{K_0 \varepsilon_0 A}{t} \tag{2.2}$$

where $K_0$ is dielectric constant of the oxide, $\varepsilon_0$ permittivity of free space, $A$ gate area and $t$ thickness of the oxide. Under depletion conditions, $V_G < 0$, electrons disappear from the surface region of the semiconductor near the O-S interface. This region, generally is called depletion layer, whose width depends on how much gate voltage is applied. At the opposite end of depletion layer, electrons will follow the varying gate voltage. The situation will then be like two parallel-plate capacitors in series. One parallel-plate capacitor is the oxide layer, the other is the depletion layer. Equation 2.2 is still valid for oxide layer capacitance, and depletion layer capacitance can be described as equation 2.3,

$$C_s = \frac{K_s \varepsilon_0 A}{W} \tag{2.3}$$

where $K_s$ is dielectric constant of semiconductor and $W$ the width of depletion layer. The total capacitance of the device is

$$C = \frac{C_s C_o}{C_s + C_o} = \frac{C_o}{1 + \frac{K_0 W}{K_s t}}. \tag{2.4}$$

It is easy to find $C$ is a function of width of depletion layer.

When an n-MOS-capacitor is biased more negatively, the inversion state can be achieved. In this state, minority carriers can appear at the O-S interface. The frequency of the AC gate voltage probe may then affect the measured capacitance of the device. Due to the slow response of minority carriers (holes for n-type), high-frequency gate voltage will only drive the electrons in depletion layer, while low-frequency gate voltage will make holes respond. The capacitance of device can be expressed as following,

$$C = \begin{cases} C_o & \omega \longrightarrow 0 \\ \frac{C_o}{1+\frac{K_0 W}{K_s t}} & \omega \longrightarrow \infty \end{cases} \tag{2.5}$$

We use figure 2.4 to explain the capacitance of MOS-capacitor in different regions.

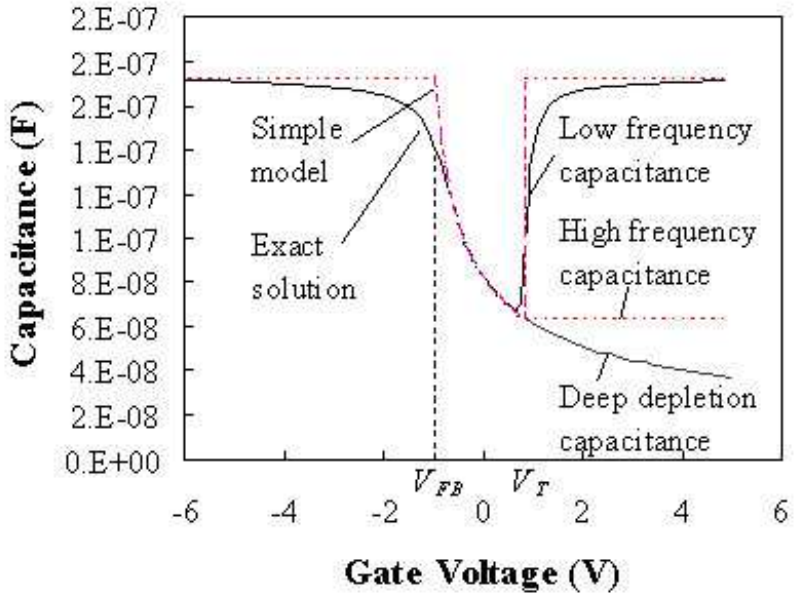


Fig. 2.4: The capacitance of an MOS-capacitor under different bias conditions.

### Electrostatic Analysis

With a knowledge of how energy bands bend with the application of gate voltages, it is necessary to derive the relationships among the potential distribution, the charge density and the electric field inside the semiconductor.

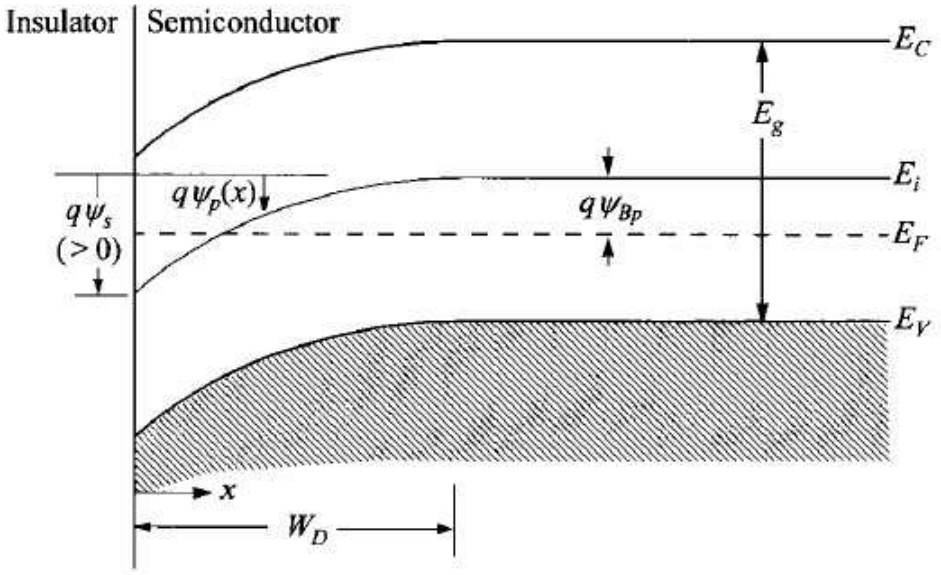


Fig. 2.5: The energy band diagram of a p-type semiconductor under the positive bias[38].

Figure 2.5 shows the energy band diagram of a p-type semiconductor under the positive bias. The potential $\psi$ is a function of distance $x$. In the semiconductor bulk away from the interface, $\psi = 0$. Also, in the 'flat-band state', the surface potential, $\psi_s = \psi(x = 0) = 0$. As functions of $\psi$, the concentrations of electrons and holes can be written as the following equations.

$$n_p = n_{p0} \exp(q\psi/kT) = n_{p0} \exp(\beta\psi) \tag{2.6}$$

$$p_p = p_{p0} \exp(-q\psi/kT) = p_{p0} \exp(-\beta\psi) \tag{2.7}$$

In these equations, $n_{p0}$ and $p_{p0}$ represent the equilibrium densities of electrons and holes in the bulk, and $\beta \equiv q/kT$.

With the help of Poisson's equation, we can describe the relationship between $\psi$ and the charge density.

$$\frac{d^2\psi}{dx^2} = -\frac{\rho(x)}{\epsilon_s} \tag{2.8}$$

$\epsilon_s$ in above equation is the permittivity of the semiconductor material and $\rho(x)$ the charge density, which is given as

$$\rho(x) = q(N_D^+ - N_A^- + p_p - n_p) \tag{2.9}$$

, in which $N_D^+$ and $N_A^-$ are the densities of the ionized donors and acceptors. The boundary conditions are $\rho(x = \infty) = 0$ and $\psi(x = \infty) = 0$. Therefore, when $x = \infty$,

$$N_D^+ - N_A^- = n_{po} - p_{po}. \tag{2.10}$$

Generally,

$$p_p - n_p = p_{po} \exp(-\beta\psi) - n_{po} \exp(\beta\psi). \tag{2.11}$$

The Poisson's equation can be written as follows.

$$\frac{\partial^2\psi}{\partial x^2} = -\frac{q}{\epsilon_s}[p_{po}(e^{-\beta\psi} - 1) - n_{po}(e^{\beta\psi} - 1)]. \tag{2.12}$$

If we integrate the above equation,

$$\int_0^{\partial\psi/\partial x} (\frac{\partial\psi}{\partial x}) d(\frac{\partial\psi}{\partial x}) = -\frac{q}{\epsilon_s} \int_0^{\psi} [p_{po}(e^{-\beta\psi} - 1) - n_{po}(e^{\beta\psi} - 1)] d\psi \tag{2.13}$$

we find the relationship between the electric field and the potential,

$$E^2 = (\frac{2kT}{q})^2(\frac{qp_{po}\beta}{2\epsilon_s})[(e^{-\beta\psi} + \beta\psi - 1) + \frac{n_{po}}{p_{po}}(e^{\beta\psi} - \beta\psi - 1)], \tag{2.14}$$

where $E = \partial\psi/\partial x$. If we define two new variables:

$$L_D \equiv \sqrt{\frac{kT\epsilon_s}{p_{po}q}} \tag{2.15}$$

and

$$F(\beta\psi, \frac{n_{po}}{p_{po}}) \equiv [(e^{-\beta\psi} + \beta\psi - 1) + \frac{n_{po}}{p_{po}}(e^{\beta\psi} - \beta\psi - 1)]^{1/2}, \tag{2.16}$$

the electric field will be

$$E = \pm\frac{\sqrt{2}kT}{qL_D}F(\beta\psi, \frac{n_{po}}{p_{po}}). \tag{2.17}$$

Depending on the sign of $\psi$, $E$ will be either positive or negative. At the surface of semiconductor, $\psi = \psi_s$, the electric field is

$$E_s = \pm\frac{\sqrt{2}kT}{qL_D}F(\beta\psi_s, \frac{n_{po}}{p_{po}}). \tag{2.18}$$

The surface charge density can also be obtained by using the following equation,

$$Q_s = -\epsilon_s E_s = \mp\frac{\sqrt{2}kT}{qL_D}F(\beta\psi_s, \frac{n_{po}}{p_{po}}). \tag{2.19}$$

Knowing the electric field and the surface charge density, we can get the expression of semiconductor capacitance

$$C_D \equiv \frac{\partial Q_s}{\partial \psi} = \frac{\psi_s}{\sqrt{2}L_D} \frac{[1 - e^{-\beta\psi_s} + (n_{po}/p_{po})(e^{\beta\psi} - 1)]}{F(\beta\psi_s, n_{po}/p_{po})}. \tag{2.20}$$

An interesting result is when semiconductor is at flat-band condition, $\psi_s = 0$, the capacitance is

$$C_D = \epsilon_s / L_D. \tag{2.21}$$

We have made an assumption in above analysis that the MOS-capacitors are on silicon substrates. For MOS-capacitors fabricated on SiC, the situation will be slightly different because of SiC's wider band gap compared with silicon. Details describing SiC-based MOS-capacitors will be discussed in next chapter.

### 2.1.2 Real MOS-Capacitors

When dealing with real MOS-Capacitors, we can not avoid defects in semiconductor, traps at O-S, mobile ions in insulator and the effects of the gate metal.

#### Work Function Difference

Since C-V characteristics has been used to describe the electrical properties of ideal MOS-Capacitors, this method will be employed for a better understanding of real MOS-Capacitors. In C-V measurements, flat-band voltage is an important quantity, which refers to the voltage applied on gate to make the electrical potential at the O-S interface equal to that of the bulk semiconductor. In other words, when flat-band voltage is applied, the

conduction and valence bands are horizontal on a band diagram. Theoretically, flat-band voltage can be expressed simply by the following equation

$$V_{fb} = \phi_{ms} - \frac{1}{C_{ox}}[Q_F + \gamma_m Q_{MI} + Q_{IT}] \tag{2.22}$$

where $V_{fb}$ is flat-band voltage, $\phi_{ms}$ is the work-function difference between gate metal and semiconductor, $C_{ox}$ the oxide capacitance of insulator, $Q_F$ the positive fixed charge located near the O-S interface on the insulator side, $Q_{MI}$ the mobile ion charge in insulator, $\gamma_m$ a pure number ranging from 0 to 1 for MIS at the M-O and O-S interfaces respectively, and $Q_{IT}$ the charges located in interface traps.

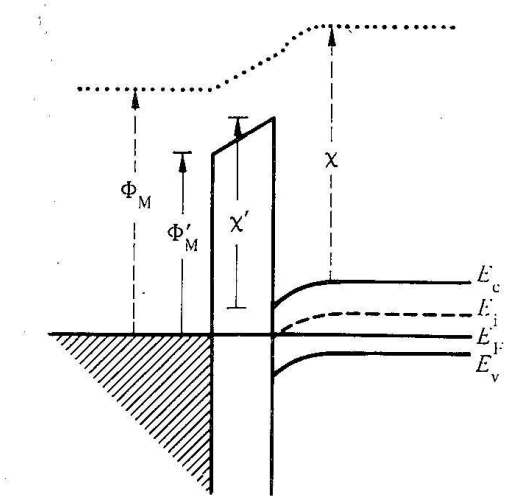


Fig. 2.6: The energy band diagram of a real MOS-capacitor at flat-band state[37].

For the case of ideal devices, insulator layer is clean, interface quality is perfect and the work functions of the gate metal and the semiconductor are the same. Therefore flat-band voltage will be equal to 0. The situation, however, will be different for real MOS-Capacitors. First of all, $\phi_{ms} \neq 0$ due to the fact that the Fermi levels of semiconductor and metal must

be aligned in a device in equilibrium. The Fermi level of semiconductor depends on doping and is unlikely to be at same level as that of metal. This will lead to shift of Fermi level of the metal and to energy-band bending of the semiconductor. Figure 2.6 explains the work function difference in real MOS-Capacitors,

**Oxide Charges**

If we don't consider charges located in device, the gate voltage will be equal to $\phi_{ms}$ in flat-band state. The charges, however, are the most important issues in the real devices. For instance, mobile ions are frequently introduced in fabrication of semiconductor devices. The most commonly seen mobile ions are sodium ions which are introduced from the hands of operators or materials used in fabrication process. A serious problem produced by mobile ions is the flat-band voltage will shift dramatically under electrical bias at elevated temperature. From equation 2.6, the mobile ion concentration can be calculated if one knows the shift of flat-band voltage and the oxide capacitance. Most semiconductor devices need to operate at temperatures as high as $150^oC$, and mobile ions located in the insulator will change the working voltage of a device, which leads to unstable operation. Many methods have been proposed to solve the mobile ion problem. In the phosphorus stabilization method[42], the surface of the oxide layer is infused phosphorus. Heated at high temperature, the mobile ions in the oxide will move everywhere. Once entering the phosphorus layer, they are trapped and immobilized. A similar approach was also used by Miremadi[43] who used thin alumina layers and thin $MoS_2$ films as protective layers.

Another method is called chlorine neutralization[44], in which people introduce a small amount of chlorine, in the form of HCl, $Cl_2$ or TCE, into the oxide growth chamber. A new

material chlorosiloxane will be produced at the O-S interface. The mobile ions in the oxide layer will move into the new material and be trapped. Chlorosioxane is reported to have no effects on the electrical properties of MOS devices.

Other than mobile ions, other kinds of oxide charges exist as well. Unlike mobile ions, these charges don't move with bias and temperature, but rather stay very close to the O-S interface. Because of this property of stability, they are generally called fixed oxide charges. It has been found experimentally, fixed oxide charges don't disappear with improvement of fabrication environment. Furthermore, fixed oxide charges depend on semiconductor surface orientation and oxide conditions such as temperature and gas used, but not on thickness of oxide, semiconductor doping concentration or doping type[37]. Generally speaking, fixed oxide charges are positive in silicon-based oxide, and are believed to result from unoxidized silicon atoms. Based on this information, people have used post-oxidation annealing to reduce the fixed oxide charge concentration.

Equation 2.22 has one more term affecting flat band voltage, which is the interface trap charge, $Q_{IT}$. Interface trap density, however, is the term people use more often to describe the quality of interface of semiconductor and oxide. As an intrinsic property of an MOS device, interface trap density plays a very important role in operating efficiency of whole device. As a result, it has been studied very widely, many approaches have been proposed to improve the interface quality[45–49] by reducing the interface trap density. Currently, the interface trap density for $Si/SiO_2$ is around $10^9 cm^{-2}eV^{-1}$, while the density for 4H-$SiC/SiO_2$ is $10^{11} cm^{-2}eV^{-1}$ at best. Interface trap density for $SiC/SiO_2$ will be discussed in more detail in later chapters.

## 2.2 MOSFETs

The metal-oxide-semiconductor field effect transistor (MOSFET) is a fundamental semiconductor device that is widely applied in both analog and digital circuits. With the dramatic shrinking of chip size, millions of MOSFETs can be integrated into an area as small as 1 $mm^2$.

### 2.2.1 Device Structures

Although various speciality structures can be found in the literature, the basic MOSFET is nothing more than an MOS-capacitor plus two p-n junctions. Figure 2.7 shows the structure of a lateral n-MOSFET. Two $N^+$ zones are called source and drain respectively, where "+" means high doping. Above the oxide layer is a metal gate such as Al or Mo. The source and drain have metal layers, as well, that are annealed at high temperature to form ohmic (i.e., non-rectifying) contacts to the $N^+$ regions of the semiconductor. Another ohmic contact is also formed on the bottom side of the semiconductor. If bottom side of semiconductor is highly doped, annealing is not necessary since the backside ohmic contact is a large area contact. Besides lateral test MOSFETs, other structures are designed for particular applications. For example, vertical geometry MOSFETs handle high power. Lateral test MOSFETs were used in this work.

### 2.2.2 Device Characteristics

The working mechanism of the MOSFETs is not complicated. From figure 2.7, it is easy to see that, if the gate voltage is not applied, no current flows from source to drain, because a reversed biased p-n junction blocks any electron flow no matter the polarity of

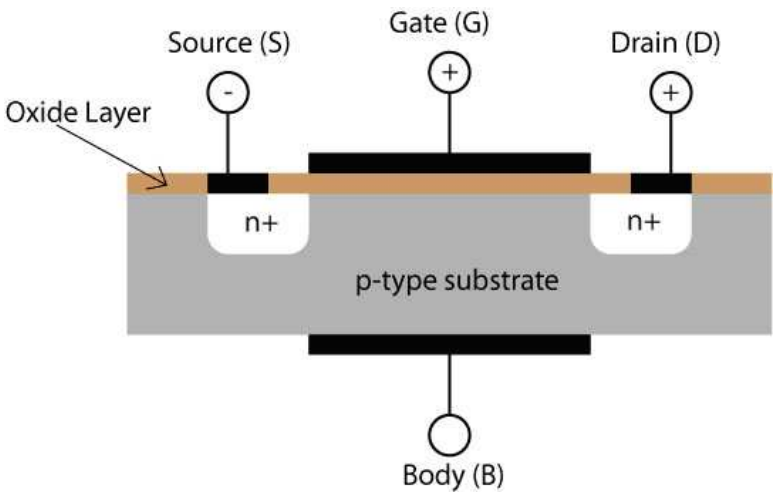


Fig. 2.7: The structure of a lateral n-MOSFET.

the source-drain voltage. However, if gate voltage is not zero, the situation will be different. According to figure 2.7, the substrate is p type semiconductor material; therefore negative gate voltage will make holes accumulate at the O-S interface, and current cannot flow along the interface in the p-type semiconductor. However, when positive voltage is applied on gate, holes are repelled from the O/S and electrons simultaneously will move up to the interface. This movement creates a depletion layer, as described previously. With more positive voltage applied, the surface of the semiconductor inverts to produce an n-type channel that connects the S/D regions of the device. If a voltage exists between the source and drain terminal, current flow will be observed. Generally, the source terminal is grounded and voltage is applied on drain terminal. The voltage and corresponding current are called drain voltage and drain current, respectively, or simply $V_D$ and $I_D$. Gate voltage is noted by $V_G$.

The voltage applied on the gate to create the n-channel is an important quantity, which is called threshold voltage, $V_T$. Simply speaking, the MOSFET will conduct if $V_G > V_T$,

but only when $V_D$ is small compared to $V_G - V_T$. If $V_D$ is positive and large enough, the channel region near the drain will see a modified bias voltage. The result slows the rate of increase in the current flow. When channel near the drain is "pinched-off", the current through the drain will no longer increase, but rather remain constant. Figure 2.8 depicts the above explanation.

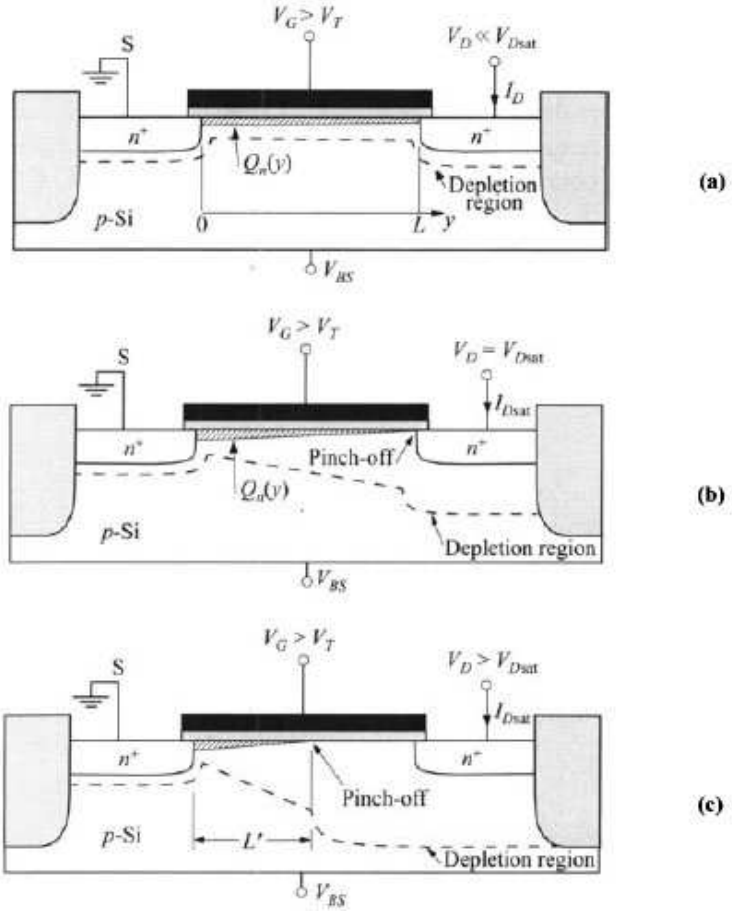


Fig. 2.8: MOSFET operated (a) in the linear region (low $V_D$,), (b) at onset of saturation, and (c) beyond saturation[38].

### Linear and Saturation Regions

In this section, we begin by discussing the ideal MOSFET . By "ideal", we are speaking of several conditions: (1) gate-oxide-semiconductor is similar to that of the MOS-capacitor; (2) only drift current will be considered; (3) there exists a constant carrier mobility in the inversion layer; (4) semiconductor is uniformly doped; (5) reverse leakage current is very small and can be neglected; (6) the transverse field in the channel is much larger than the longitudinal field[38]. Under these idealized conditions, the conductivity of the inversion channel can be written as

$$\sigma(x) = qn(x)\mu_n(x). \tag{2.23}$$

In the above equation, $n(x)$ is the carrier concentration in the channel, and $\mu_n(x)$ the channel mobility. The conductance of the inversion channel will be

$$g = \frac{Z}{L}\int_0^{x_i} n(x)dx, \tag{2.24}$$

in which $Z$ is the channel width, $L$ the channel length and $x$ is measured from the interface into the semiconductor. Assuming the channel mobility is constant, the conductance will be

$$g = \frac{qZ\mu_n}{L}\int_0^{x_i} n(x)dx = \frac{qZ\mu_n|Q_n|}{L}, \tag{2.25}$$

in which $Q_n$ is the total charge in the inversion channel. Let us consider a small element in the channel and assume the length of this element is $dy$. The voltage drop across this element will be

$$dV = I_D dR, \tag{2.26}$$

and

$$dR = \frac{dy}{gL} = \frac{dy}{Z\mu_n|Q_n(y)|}, \tag{2.27}$$

where $I_D$ is the drain current that does not change with location in the channel. It can be shown[38] that the inversion charge in the channel is

$$Q_n(y) = -[V_G - V(y) - 2\psi_B]C_i + \sqrt{2\epsilon_s q N_A[V(y) + 2\psi_B]}, \tag{2.28}$$

where $V_G$ is the applied gate voltage, $V(y)$ is the bias between a specific point $y$ and the source, $\psi_B$ is the bulk potential, and $C_i$ is the capacitance per unit area. If we integrate equation 2.26 from the source to the drain, given that $V(y = 0) = 0$ and $V(y = L) = V_D$, the drain current can be expressed as

$$I_D = \frac{Z}{L}\mu_n C_i\{(V_G - 2\psi_B - \frac{V_D}{2})V_D - \frac{2}{3}\frac{\sqrt{2\epsilon_s q N_A}}{C_i}[(V_D + 2\psi_B)^{3/2} - (2\psi_B)^{3/2}]\}. \tag{2.29}$$

From the above equation, we can infer important characteristics of MOSFET. When $V_G$ is given and $V_D$ is small, by expanding in a Taylor series and keeping only the first-order terms, we can get a simplified expression for $I_D$,

$$I_D \cong (Z/L)\mu_n C_i(V_G - V_T)V_D \tag{2.30}$$

for $V_D \ll (V_G - V_T)$ where $V_T$ is called the threshold voltage, a very important MOSFET parameter

$$V_T = 2\psi_B + \frac{\sqrt{2\epsilon_s q N_A(2\psi_B)}}{C_i}. \tag{2.31}$$

This tells us $I_D - V_D$ is a straight line when $V_D$ is small. This region is called linear region of the MOSFET. By taking derivative of $I_D$ with respect to $V_D$ or $V_G$, we can obtain the expression for the channel conductance and transconductance. They are

$$g_D \equiv \frac{\partial I_D}{\partial V_D}|_{V_G=const} = (Z/L)\mu_n C_i(V_G - V_T) \tag{2.32}$$

$$g_m \equiv \frac{\partial I_D}{\partial V_G}|_{V_D=const} = (Z/L)\mu_n C_i V_D. \tag{2.33}$$

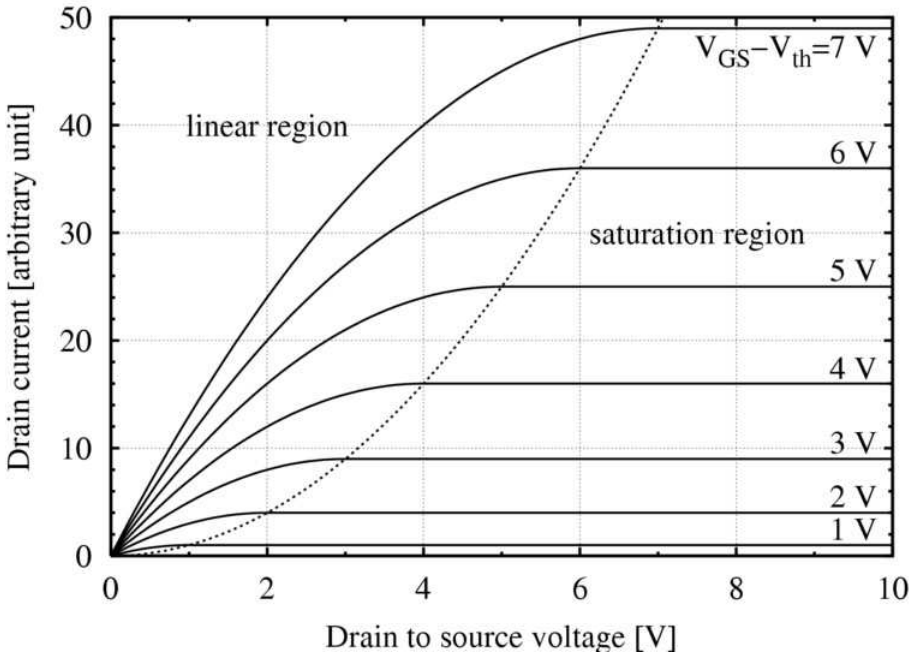


Fig. 2.9: The drain current - gate voltage characteristics of an MOSFET.

If $V_D$ is not small, but instead large enough that $Q_n(y = L) = 0$, the MOSFET enters the saturation region and the point where $V_D$ applied leads to zero charge at $y = L$ is called 'pinch-off'. At this point, we name $V_D$ and $I_D$ as $V_{Dsat}$ and $I_{Dsat}$, respectively. The

complete drain current versus drain voltage plot is shown in figure 2.9. Theoretically, by solving equation for $Q_n(y)$, we can obtain the values of $V_{Dsat}$ and $I_{Dsat}$.

$$V_{Dsat} = V_G - 2\psi_B + \frac{\epsilon_s q N_A}{C_i^2}(1 - \sqrt{1 + 2V_G C_i^2/\epsilon_s q N_A}), \tag{2.34}$$

and

$$I_{Dsat} \cong \frac{mZ}{L}\mu_n C_i (V_G - V_T)^2, \tag{2.35}$$

in which $m$ is a function of doping concentration and roughly equal to 1/2 for light doping. $V_T$ is same as previously stated if doping is low, and the insulator is thin. However, when these two conditions are not satisfied, $V_T$ will be a function of $V_G$. In saturation region, the transconductance is given by

$$g_m = \frac{\partial I_D}{\partial V_G}|_{V_D=const} = \frac{2mZ}{L}\mu_n C_i (V_G - V_T). \tag{2.36}$$

In real measurements, the channel mobility can be calculated using the above equation by measuring drain current as a function of the gate voltage.

The MOSFET device characteristics we have discussed so far describe ideal devices. In the following section, several real issues related to MOSFETs will be discussed, and corresponding adjustments will be made to describe the real devices.

**Work Function Difference**

As with MOS-capacitors, the metal gate - semiconductor work function difference is an unavoidable problem which requires that we introduce the term $\phi_{ms}$ and write the threshold

voltage as

$$V_T = \phi_{ms} + 2\psi_B + \frac{\sqrt{4\epsilon_s q N_A \psi_B}}{C_i}. \tag{2.37}$$

**Fixed Oxide Charges**

Considering the fixed oxide charges $Q_f$, the threshold voltage will be

$$V_T = \phi_{ms} - \frac{Q_f}{C_i} + 2\psi_B + \frac{\sqrt{4\epsilon_s q N_A \psi_B}}{C_i}. \tag{2.38}$$

In addition to the non-idealities discussed above, channel doping uniformity, channel length and temperature affect the MOSFET characterisitics, particularly the threshold voltage, the subthreshold slope and the channel mobility.

# Chapter 3

# SiC-based MOS Devices Properties

## 3.1 Oxidation of SiC

The oxidation of SiC is the most important process of SiC-based MOS devices, since the quality of the oxide layer critically determines the devices' performance[50]. Of many oxidation processes, the thermal oxidation is the most commonly used one due to the fact that thermal oxidation techniques of silicon can be applied directly, and yields a better interface quality than other methods. Other methods for putting an oxide layer over SiC include sputtering, chemical vapor deposition, and pulsed laser deposition. In this thesis, we focus only on thermal oxidation.

The mechanism of thermal oxidation of SiC has been investigated both theoretically and experimentally. First-principle calculations are used to study the atomic-scale mechanisms of the nucleation and growth of $SiO_2$ precipitates in cubic SiC[51, 52]. In his work, Di Ventra *et al.*[51] proposed the mechanisms of the oxidation process on SiC. They found by calculation that oxygen atoms diffused onto the surface of SiC and formed an advance interface of $SiC/SiO_2$. The excess carbon atoms were emitted out of the system in the form of CO, as confirmed experimentally by Tan *et al.*[53]. When thicker $SiO_2$ layer was formed, CO had to diffuse through the oxide layer to take out carbon atoms. Through simulation, they found CO may break up either at the interface of $SiC/SiO_2$ or in the

SiC bulk. The broken oxygen atom would participate in another round of oxidation and carbon atom would remain. This result explained why carbon clusters are found at the interface of $SiC/SiO_2$. Wang *et al.*[52] went further. When CO diffused through the oxide layer, two or more CO molecules might interact and the result was the more complicated structure formed. One of the consequences was the emission of $CO_2$, not just CO. However, no experimental evidence has been reported to support this result yet. Knaup *et al.*[54] reported in their theory work that carbon interstitials and stable carbon pairs grow into the oxide as well as CO molecules. Combined with silicon interstitials, these defects were thought to be the sources of NIT (near-interface traps).

Shenoy *et al.*[55] study experimentally the effect of substrate orientation on thermal oxidation on SiC. They noticed the oxidation rate depended significantly on the crystal orientation of SiC. For instance, *a*-axis planes of SiC oxidize at rates as much as 3-5 times faster than the Si-face *c* axis. Figure 3.1 shows the oxide thickness on (0001) and $(11\bar{2}0)$ orientated 6H-SiC for three different oxidation times.

## 3.2 $SiC/SiO_2$ Interface

Although SiC is superior to silicon in many aspects, a number of improvements need to be made before it can replace silicon as the dominant semiconductor. The problem which impedes the real application of SiC in MOS devices is the quality of the interface between SiC and $SiO_2$. Please note only the interface of $SiC/SiO_2$ produced by thermal oxidation is under discussion.

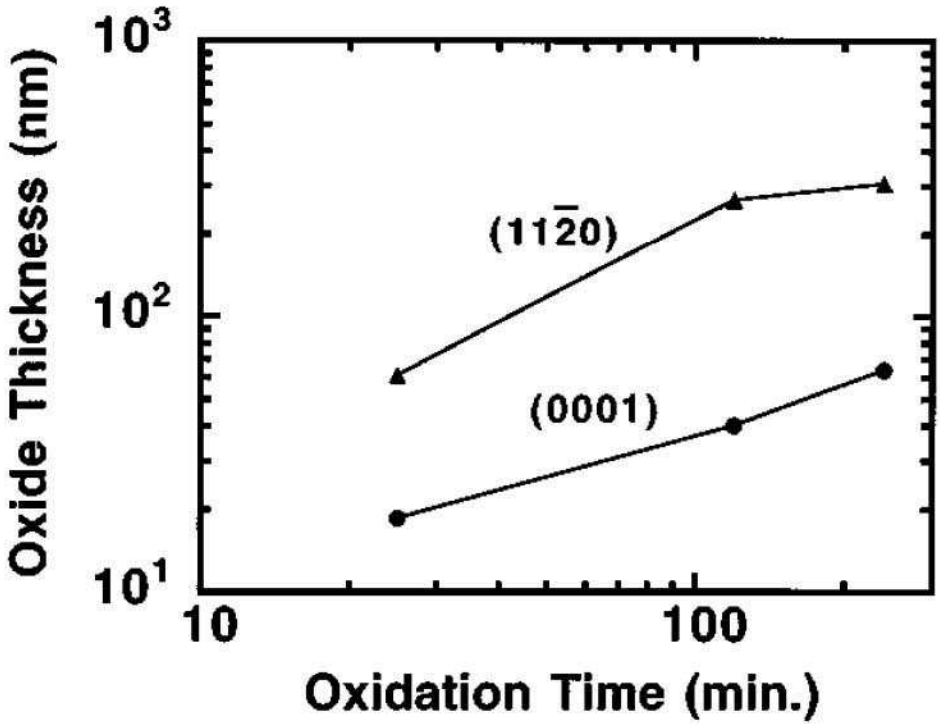


Fig. 3.1: Comparison of oxide thickness on (0001) and (11$\bar{2}$0) oriented 6H-SiC as a function of oxidation time[55].

In order to study the interface states of $SiC/SiO_2$, many experimental methods have been used. Afanasev *et al.*[56] determined the interface state density by admittance spectroscopy. McDonald *et al.*[57] employed SIMS(Secondary Ion Mass Spectrometry) to study how SiC and $SiO_2$ are connected; Chung *et al.*[58] used the simultaneous high-low capacitance-voltage technique to obtain the interface state density of $SiC/SiO_2$. Bardeleben *et al.*[59] studied the $SiC/SiO_2$ interface by EPR (Electron Paramagnetic resonance) [59–61]. Other techniques include AFM (Atomic Force Microscopy)[62], EELS (Electron Energy Loss Spectroscopy)[63], SER (Surface Sensitized Raman)[64], and XPS (X-ray photoelectron spectroscopy)[65]. The effort dedicated by the researchers has created a detailed picture of the interface between SiC and $SiO_2$. In the following sections, the current research on the interface of $SiC/SiO_2$ will be reviewed and the challenges will be discussed.

It has been reported that the interface trap density of $SiC/SiO_2$ ranges from $10^{11}cm^{-2}eV^{-1}$ to $10^{13}cm^{-2}eV^{-1}$[56], while the interface trap density of $Si/SiO_2$ is $10^{9}cm^{-2}eV^{-1}$. The higher interface trap density results in lower inversion channel mobility of MOSFETs[66, 67]. It is unclear whether the worse interface quality comes from the intrinsic $SiC/SiO_2$ system or the thermal oxidation process[68]. However, for the last 10 years, people have been finding a lot of useful information of the $SiC/SiO_2$ interface[67–71].

Shenoy *et al.*[69] used hi-lo capacitance-voltage technique and AC conductance technique at elevated temperatures to characterize the MOS interface of p-type 6H-SiC, because they found only by doing this can they obtain the information of the interface states beyond 0.6eV from the band edge, or the deeper levels of the band gap, which are too stable to be charged and emitted at room temperature and low frequency. Friedrichs *et al.*[70] reported the interface properties of MOS structure of n-type 6H and 4H-SiC. From both theory and

experiments, they showed that the $SiC/SiO_2$ interfaces are more sophisticated than the $Si/SiO_2$ interfaces. Moreover, 6H-SiC showed a better interface quality than 4H-SiC did. To study the interface state very near to the band edges, Saks *et al.*[67] used Gray-Brown C-V technique to obtain profiles of $D_{it}$ close to both band edges of 4H-SiC. In their work, $D_{it}$ increased rapidly close to the conduction band edge. Dhar *et al.*[71] used similar method to reveal the ultrashallow defect states ($E_C$-E$\cong$0.05-0.2eV) at $SiO_2$/4H-SiC interfaces. A $D_{it}$ peak at $\sim$0.1eV below the conduction band edge is found with an energy width of $\sim$0.2eV and a magnitude of $\sim 2 \times 10^{13} \mathrm{cm}^{-2}\mathrm{eV}^{-1}$. Figure 3.2 shows the interface trap density ($D_{it}$) of different polytypes of SiC along the band gap energy[68]. Schörner *et al.*[66] found most interface defects of $SiC/SiO_2$ are located at around 2.9eV above the valence band. Considering the band gap information of several SiC polytypes, 4H-SiC will have more defects in the gap rather than other polytypes like 6H- and 15R-SiC. This also explains why the inversion channel mobility of 4H-SiC is lower than that of other polytypes.

The $SiC/SiO_2$ interface roughness may come from the following: (1) the surface atom density of SiC is larger compared to that of silicon, (2) a transition layer exists instead of a perfect connection of SiC and $SiO_2$[65], (3) carbon cluster accumulates at the interface during the oxidation, (4) the near-interficial oxide traps, and (5) Si- and C- dangling bonds.

While investigating the interface charges of $SiO_2$/Si on different surface orientations, Vitkavage *et al.*[72] found a strongly positive relationship between the silicon surface atom density and the charge density of the Si/oxide interface. Inspired by this article, Afanasev *et al.*[56] suspected the higher surface atom density of SiC contributes to the higher interface trap density of $SiC/SiO_2$, since a higher density of dangling bonds may be produced during the oxidation process. In the same work, Afanasev *et al.* also found the dopant species

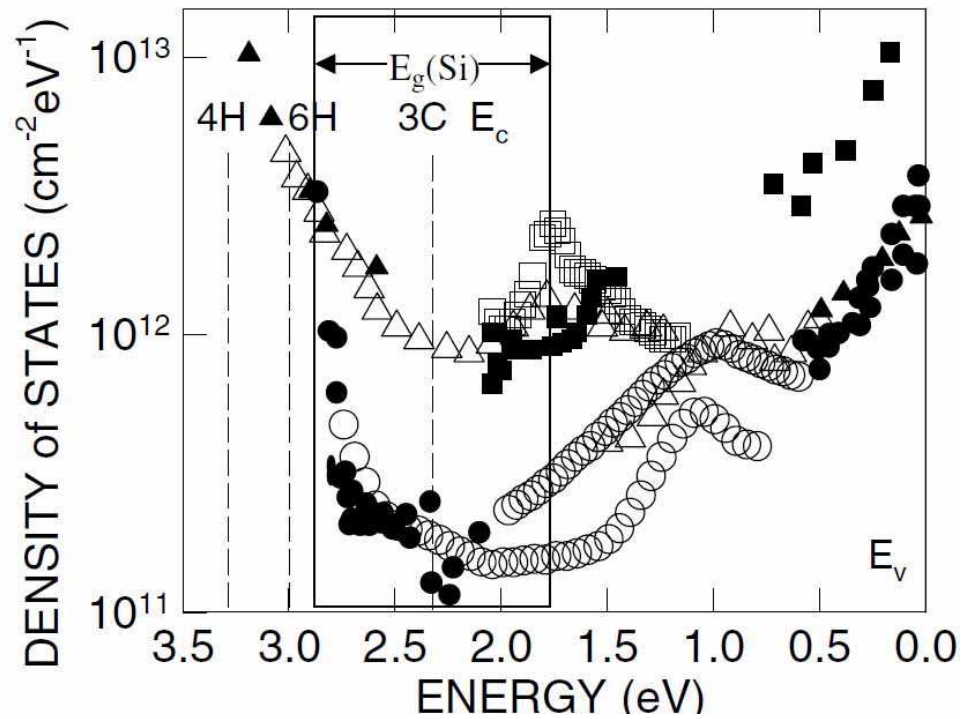


Fig. 3.2: Interface state density $D_{it}$ as a function of energy for 3C-$SiC/SiO_2$ squares, black squares, 6H-$SiC/SiO_2$ circles, bullets, and 4H-$SiC/SiO_2$ triangles, black triangles MOS structures determined from admittance spectroscopy filled symbols and from constant-capacitance deep-level transient spectroscopy open symbols[68].

(N, Al, B) do not affect the magnitude and distribution of the interface trap density ($D_{it}$). They drew the conclusion that $D_{it}$ is dominated by intrinsic defects at the interface. They also noticed the higher interface trap density of carbon face $SiC/SiO_2$ may be attributed to the higher surface carbon atom density of c-face SiC, as compared to Si-face SiC. $\pi$-bonded carbon clusters ($sp^2$- bonded carbon units) were believed to play an important role in the increased interface state density. Electron energy loss spectroscopy (EELS) also showed a high-carbon concentration at the $SiO_2$/6H-SiC(0001) interface[63]. The carbon-rich region is 10-15Å in thickness, and may be produced by the kinetically limited formation and removal of volatile CO molecules. The C- dangling bonds were also found at the interface states around 1.8eV above the valence band maximum (VBM) by Kobayashi *et al.*[73] when they were studying the interface states at silicon face 6H-$SiC/SiO_2$ by using x-ray photoelectron spectroscopy (XPS). Meanwhile they found a broad interface-state peak at around 2eV above the VBM, which they believed was attributable to Si- dangling bonds at the interface. They also noticed that the density of the Si- dandling bonds did not depend strongly on the oxidation temperature and atmosphere, while that of the carbon-related interface states were strongly dependent on them.

The interface state density is also affected by the near-interficial oxide traps (NIT). These traps are those oxide traps located very close to the interface and being able to trap a charge carrier from the semiconductor or to emit it back into the semiconductor[56]. The PST technique (photon stimulated electron tunneling) was used to detect the location of oxide traps relative to the conduction band edge of several semiconductor materials like silicon, 3C-SiC, 4H-SiC and 6H-SiC. It was found that the oxide traps always occur at the same locations relative to the oxide conduction band edge, say 2.77eV below the $SiO_2$

conduction band edge. For silicon, 3C-SiC, 6H-SiC, the traps are still in the oxide layer. But for 4H-SiC, the traps are located at the interface. Therefore, the oxide traps contribute to the interface state of SiC, especially the 4H-SiC. In theoretical work of Knaup *et al.*[74], carbon pairs are believed to contribute to the NIT.

Based on the above review, it is clear that the interface quality of $SiC/SiO_2$ plays a very important role in the function of SiC-based MOS devices. To improve the quality of SiC MOS devices, the first thing to do is improve the interface state of $SiC/SiO_2$. Experimentally, people have found pre-oxidation ultraviolet-ozone cleaning or post-oxidation annealing enhances the quality of the interface[34, 58, 75–77]. The latter will be discussed mainly in this work.

### 3.2.1 Post-Oxidation Annealing

Post-oxidation annealing has been a main technique to enhance the interface quality of $SiC/SiO_2$. Varying gases may be used in this process.

#### Nitridation

Li *et al.*[77] used NO in post-oxidation annealing of 6H-$SiC/SiO_2$ and found the interface state density reduced dramatically. However, the use of $N_2O$ in the post-oxidation annealing increased the interface state density. Figure 3.3 shows the interface trap density after NO and $N_2O$ annealing. Chung *et al.*[58] reported the improvement of the interface quality of 4H-$SiC/SiO_2$ by using NO post-oxidation annealing. This improvement, however, only occurs at the upper half of the gap. They also explained theoretically the NO effect on the interface in figure 3.4, according to which, the carbon clusters will move from near the

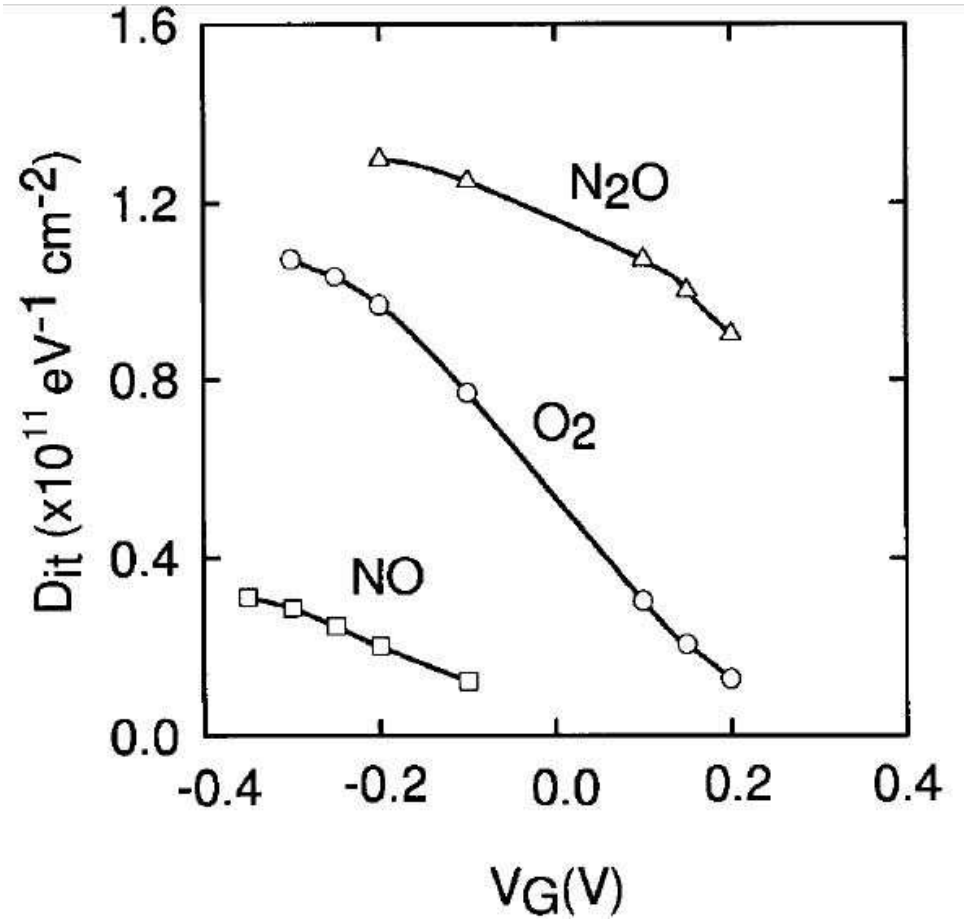


Fig. 3.3: Interface state density versus gate voltage for MOS capacitors with three different types of dielectrics[77].

conduction band downward to near the valence band, and some small carbon clusters even enter the valence band. The consequence is the interface trap density near the conduction band is reduced dramatically. In another article, Chung *et al.*[78] tried another type of gas, ammonia or $NH_3$, in the post-oxidation annealing. Compared to control samples that were not annealed, $D_{it}$ was reduced about 85%. Moreover, $NH_3$ can lower the fixed charge density and effective charges in the oxide since the anneals incorporate an extensive amount of nitrogen throughout the oxide[78]. However, McDonald *et al.*[57] show that $NH_3$ anneals remove oxygen in the oxide, change the oxide stoichiometry, increase the dielectric constant and decrease the breakdown field. They, therefore, conclude that the nitridation in NO is a better technique to reduce the $D_{it}$ in MOSFETs. Nitridation is also used to reduce the interface state of other polytypes of SiC[79].

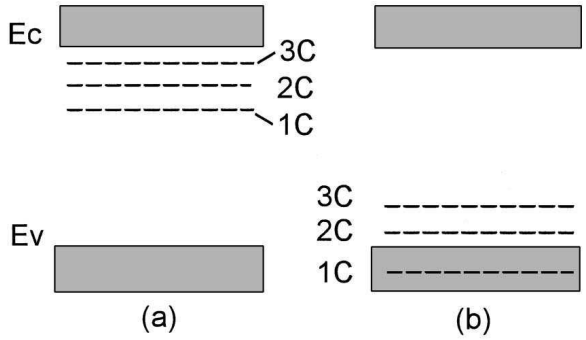


Fig. 3.4: (a) Energy levels for interstitial C and C clusters in SiC.
(b) C and C clusters in SiC following N passivation[58].

Although the experiments have already shown the effectiveness of nitridation on reduction of interface state of $SiC/SiO_2$, the mechanism for the reduction is not clear. However, several theories have been suggested for investigation[80, 81]. X-ray photoelectron spectroscopy after nitridation shows the formation of Si≡N bonds[82], which is also suggested by the observation of the slower oxidation rate. The slower oxidation rate implies the reduction

of the carbon clusters at the interface, considering the fact that $(000\bar{1})$ 4H-SiC has much higher oxidation rate than (0001) does. Gavrikov *et al.*[81] also proposed a mechanism of nitridation that the introduction of N suppresses the lateral moving of the carbon atoms and therefore reduces the possibility of formation of carbon clusters.

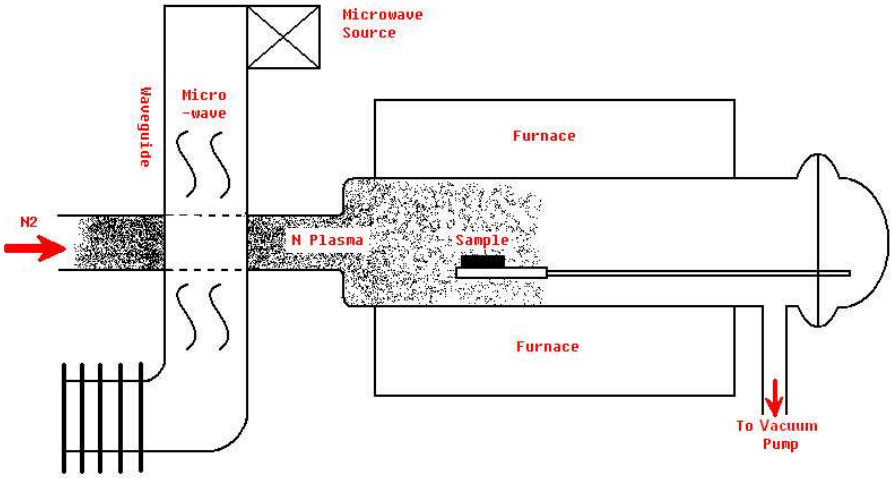


Fig. 3.5: Schematic plot of a plasma nitridation furnace[34].

The above reviews indicate the nitridation is an effective tool to reduce the interface state density of $SiC/SiO_2$. The way they did the nitridation was introducing NO into a heated environment in which $SiC/SiO_2$ structure was loaded. NO post-oxidation annealing introduces oxygen at the same time and creates new interface, which weakens some the effectiveness of nitridation. To solve this problem, some approaches are proposed. Plasma nitridation is one method[34]. Figure 3.5 shows the experimental set-up used in the plasma nitridation. In this process, $N_2$ gas is introduced into the quartz tube and microwave generator breaks $N_2$ into nitrogen atoms. Nitrogen atoms at high temperature will diffuse through $SiO_2$ all the way to the interface of $SiO_2/SiC$ and improve the interface structure.

Figure 3.6 shows the change of $D_{it}$ of (0001) 4H-SiC/$SiO_2$ after plasma nitridation with varying lengths of time[34]. Another approach is nitrogen ion implantation followed by high temperature annealing.

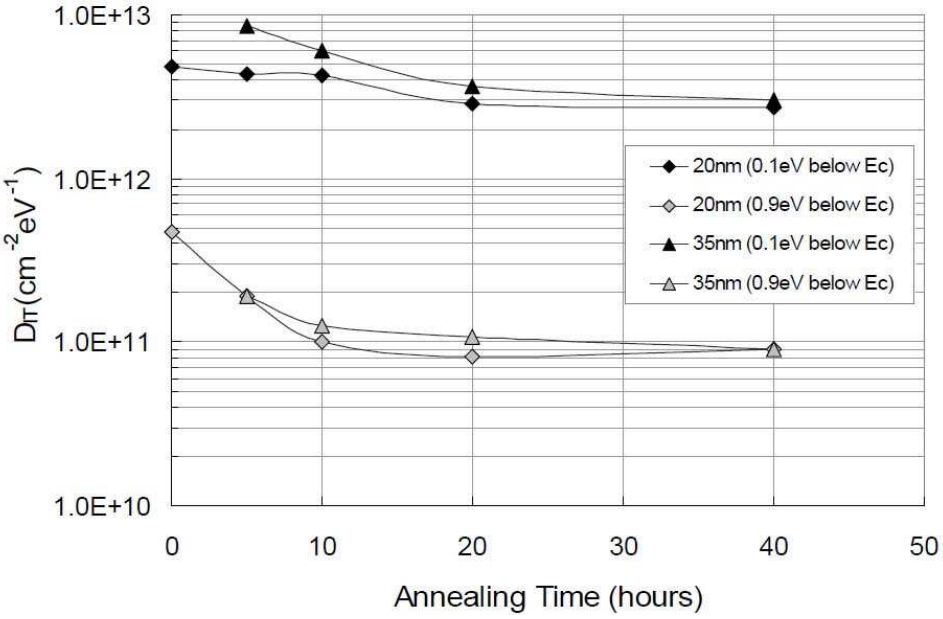


Fig. 3.6: Comparison of $D_{it}$ of silicon face 4H-SiC/$SiO_2$ before and after plasma nitridation[34].

### Hydrogen Passivation

Hydrogen has been known effective to reduce the interface states densities of Si/$SiO_2$[83], because silicon dangling bonds can be reconnected in the form of Si-H. A number of investigations have been conducted to see if the hydrogen passivation enhances the interface quality of SiC/$SiO_2$[56]. The results demonstrate no significant reduction of the interface state of SiC/$SiO_2$. This implies that the silicon dangling bonds are not the main cause of the interface defects and only hydrogen passivation dos not improve the interface quality significantly. The combination of nitridation and hydrogen passivation, however, yields a

lower $D_{it}$ on $SiC/SiO_2$ than simple nitridation does, especially at the deep level[84], as shown in figure 3.7. More specifically, Wang *et al.*[85] conclude that isolated carbon dangling bonds with various backbond combinations have a level in the midgap region and can be passivated by either H or $H_2$, but the different local geometries of correlated carbon dangling bonds can only be passivated by H.

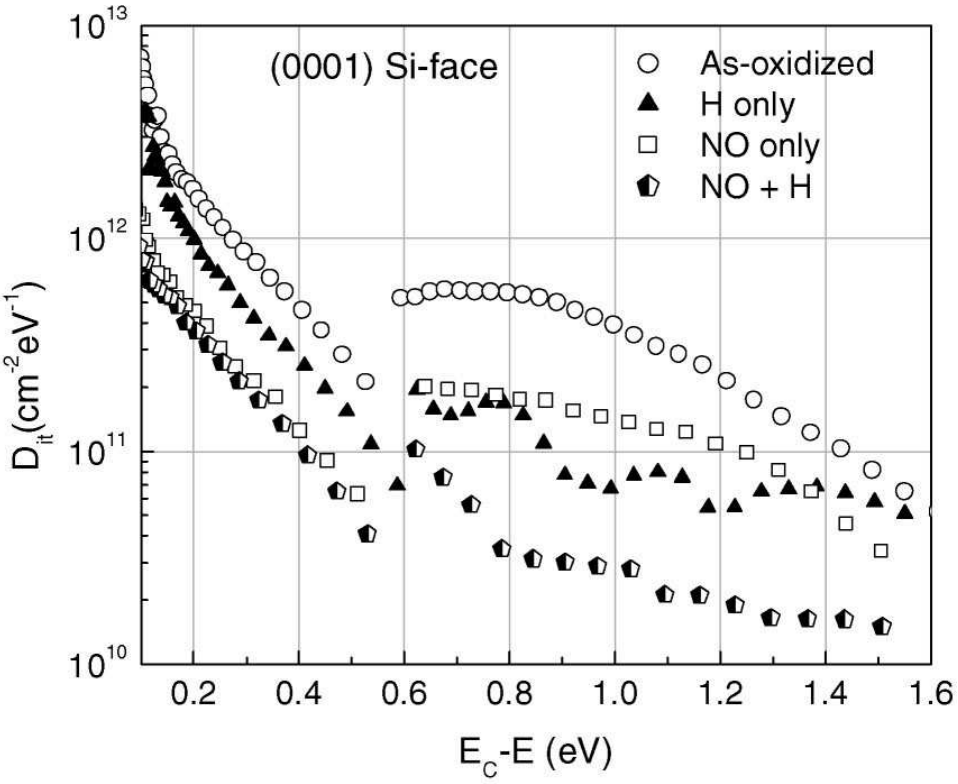


Fig. 3.7: $SiC/SiO_2$ interface state density profiles in the upper half of the 4H-SiC band-gap for the different interface treatments[85].

### 3.3 Oxide Reliability on SiC

The native oxide of SiC is $SiO_2$. This property makes SiC a unique compound semiconductor material, because the fabrication techniques on silicon can be applied on SiC and many experiments on Si-MOS devices will also be used on SiC-MOS devices.

In an MOS device, the oxide is of importance. The role of the oxide is to block the current driven by the voltage applied between the gate and the substrate. When the oxide breaks down, the MOS device is destroyed. Oxide reliability means the ability of the oxide to be stable under operational conditions. When a higher voltage is applied, the oxide tends to break down. Usually, for an oxide of a specific thickness, breakdown electric field is often used to describe the blocking strength of the oxide. To test the reliability of an oxide, current-voltage (I-V) measurements are employed to obtain the breakdown field. In the I-V measurement, applied voltage is increased from 0 to a high value, at which a defined breakdown current goes through the oxide. The value of the gate voltage causing the breakdown of oxide is called breakdown voltage. By simply calculation, the breakdown field can be determined from breakdown voltage.

$$E_{ox} = \frac{V_g - \phi_{ms}}{t_{ox}} \tag{3.1}$$

where $E_{ox}$ is the electric field inside the oxide, $V_g$ is the voltage applied on the gate, $\phi_{ms}$ is the work function difference of gate metal and semiconductor, and $t_{ox}$ is the thickness of the oxide.

### 3.3.1 Oxide Failure Mechanism

It is necessary to understand the physical process to determine the direction for improving the reliability of the oxide. The degradation of oxide is not a short-time process in practical environments. This process always starts with the accumulation of carriers at the interface of oxide and semiconductor. With the presence of different electric fields on oxide,

the carriers will obtain different kinetic energies for attempting to pass over the barrier between oxide and semiconductor. The term of "injection" is used to describe the penetration of carriers. At different levels of electric field, different injection mechanism rules the form of the penetration of carriers: quantum tunneling, thermionic emission, Frankel-pool emission and Fowler-Nordheim tunneling. Of these four injections types, quantum tunneling and thermionic emission are two happening at all time, even without electric field. They actually originate from the nature of probability and temperature, respectively. The relationship of current density and electric field in thermionic emission can be written as:

$$J_{TE} = A^* T^2 \exp(-q\frac{\phi_b - \sqrt{qE/4\pi\epsilon_{ox}}}{K_b T}) \tag{3.2}$$

, where $J_{TE}$ is the current density through the oxide, $A^*$ the effective Richardson constant, $q$ the carrier charge, $\phi_b$ the barrier height, $E$ the oxide electric field and $T$ the temperature. Frankel-pool emission refers to the current generated by electrons trapped in the oxide at high field, and generally is treated as an extrinsic injection mechanism. The corresponding J-E relationship is as follows.

$$J \sim E \exp(\frac{-q(\phi_B - \sqrt{qE/\pi\epsilon_i})}{K_b T}) \tag{3.3}$$

, where the parameters are similarly defined as those in thermionic emission. Fowler-Nordheim tunneling is also called as field emission. It is an injection process in which carriers tunnel into the oxide from either gate or semiconductor under the influence of high

electric field. The F-N tunneling can be expressed by the following equation:

$$J_{FN}(T) = A(T)E_{ox}^2 \exp(-\frac{B(T)}{E_{ox}}), \tag{3.4}$$

where

$$A(T) = \frac{q^3 m}{8\pi\hbar m_{ox}\phi_b}, \tag{3.5}$$

and

$$B(T) = \frac{4\sqrt{2m_{ox}\phi_b^3}}{3q\hbar}. \tag{3.6}$$

In above equations, $q$ is the electron charge, $m$ and $m_{ox}$ are the effective electron mass in the semiconductor and oxide, respectively, $\hbar$ is the Plank constant, $E_{ox}$ is the electric field in the oxide, and $\Phi_b$ is the effective barrier height. Since SiC has a smaller barrier height than silicon (see figure 1.8), it is expected that F-N tunneling is more dominant in the injection of SiC-MOS device.

### 3.3.2 Time Dependent Dielectric Breakdown (TDDB)

TDDB measurement is a kind of method to test the reliability of MOS devices. In the measurement, voltage is applied on devices to keep semiconductor at accumulation region. Elevated temperatures might be used as well. The time it takes before the breakdown current occurs is defined as the lifetime of a MOS device. Tens of devices are measured at the same time, so the statistical result of failure time can be obtained. In TDDB measurement, the electric field in the oxide is generally higher than that used in practical operation, thus

accelerating the measurement. Elevated temperatures might be used for the same goal. The actual lifetime of devices at low field can be extrapolated from the data at high field.

Figure 3.8 shows the schematic of a reliability test circuit. Maranowski *et al.*[86] found from the TDDB measurements that n-type 6H-SiC MOS devices showed a comparable or even better reliability at field lower than 4MV/cm than silicon MOS-devices, but a worse one at high field like 7-9MV/cm. It was concluded that the oxide reliability precluded SiC MOS devices from many high-temperature applications. Reliability of nitrided oxides in 4H-SiC MOS devices was investigated by Krishnaswami *et al.*[87], 100-year Mean Time to Failure (MTTF) was estimated for the oxides working at 175$^o$C and 3MV/cm.

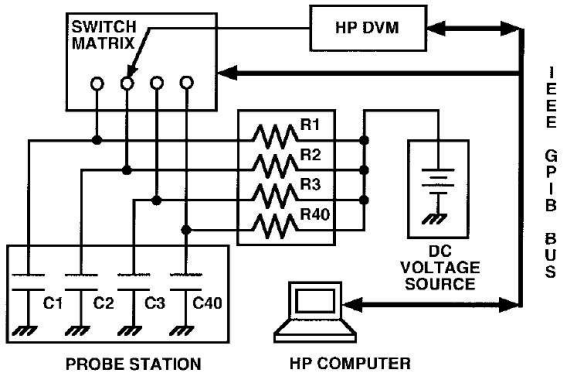


Fig. 3.8: Schematic of the reliability test circuit[86].

Other investigations on the SiC oxide reliability have also been carried out. Alok *et al.*[88] used I-V and C-V measurements to test the quality of thermal oxide grown on n-type 6H-SiC. They found a barrier height of 2.7eV by fitting with Fowler-Nordheim injection mechanism. Combined with information about the interface quality, effective charge density, breakdown field, they concluded that 6H-SiC oxides were comparable to those grown on silicon. Agarwal *et al.*[89] compared the reliability of 4H-SiC MOS devices with 6H-SiC MOS devices. Both polytypes were n-type materials. They obtained data for current densities and

electric fields, computed the effective barrier heights of both polytypes MOS devices from Fowler-Nordheim injection theory. 4H-SiC MOS devices showed a smaller barrier height, which is in agreement with results from experimentalists[90, 91]. Compared with silicon MOS devices, both polytypes did not show a better performance in reliability. P-type 4H-SiC MOS structures were studied by Chanana *et al.*[92]. Fowler-Nordheim hole tunneling was confirmed in their measurements. Using the barrier height of 2.9eV, they obtained the effective hole mass which is $0.35m$ to $0.52m$, where $m$ is the free electron mass.

### 3.3.3 Negative Bias Temperature Instability (NBTI)

It has been demonstrated that a negative gate voltage would degrade channel mobility, causing a threshold voltage shift, and reducing the drain current. NBTI occurs in silicon industry[93], the same problem has been found in SiC-based MOS devices[94]. The investigation on both silicon and SiC MOS devices has led to this conclusion: NBTI effect originates from interface and oxide trap generation. Further studies show this effect occurs only in the presence of negative gate voltage, holes in the semiconductor, and at elevated temperatures.

## 3.4 SiC-Based MOSFETs

SiC, because of its high thermal conductivity, wide band gap, and native oxide of $SiO_2$, has been chosen as a preferable candidate for MOSFET devices, especially those working in an extreme environment. The bulk electron mobility of 4H-SiC is as high as 1000cm$^2$/V-s, which is comparable to that of silicon. However, the inversion channel mobility of SiC MOSFET is very low compared to the bulk mobility. This situation was not observed in the case of silicon, whose typical inversion channel mobility is 800 - 1000cm$^2$/V-s, not

big reduction compared to its bulk mobility of 1400$m^2$/V-s. Much work has been done to understand the reason for the low inversion channel mobility of SiC-MOSFET as well as a method that improves the inversion channel mobility[45, 66, 95–97].

The low inversion channel mobility is attributed to the poor quality of interface of $SiC/SiO_2$. Attempts to enhance the inversion channel mobility have concentrated on reducing the interface states of $SiC/SiO_2$. In this section, a few results concerning the inversion channel mobility of different polytypes SiC MOSFETs will be reviewed.

Schörner *et al.*[66] used 4H-SiC, 6H-SiC and 15R-SiC to build MOSFETs. The low field mobility is significantly higher for both 6H-SiC and 15R-SiC than 4H-SiC, the corresponding $D_{it}$ of $SiC/SiO_2$ is approximately one order of magnitude lower for 6H and 15R polytpes than for the 4H polytype. They believed the oxide defects, which are located at 2.7eV above the valence band, cause the bad interface quality and low channel mobility of 4H, because 4H-SiC has a band gap of 3.2eV and most defects fall in the gap. For 6H and 15R polytypes, those defects will be at the conduction bands because of their narrow bandgap compared to 4H-SiC. Chung *et al.*[95] used NO to anneal the interface of 4H-$SiC/SiO_2$ and successfully reduced the interface trap density. They applied the same passivation process to (0001) 4H-SiC MOSFETs and found the inversion channel mobility could be improved from 3$cm^2$/V-s to 35$cm^2$/V-s[95]. It was the first time that the substantial improvement was observed in the inversion channel mobility for lateral n-channel MOSFETs fabricated with standard thermal oxidation techniques and standard 4H-SiC. A similar improvement of channel mobility on 4H-SiC n-channel MOSFET was also achieved by Schörner *et al.*[96]. The peak value of inversion channel mobility they reported was 48$cm^2$/V-s. An important difference to note it that the temperature Schörner *et al.* used to anneal the source and drain implanted

regions was 1700$^o$C, 150$^o$C higher than that typically used. The effect of implant anneal temperature on the inversion channel mobility was also studied by Lu *et al.*[45]. Only minor influence of temperature on the channel mobility was found. Moreover, they checked the effects of other process variations, such as oxidation procedure, post-oxidation annealing, type of gate material, and ohmic contact annealing. Other than post-oxidation annealing in NO, no process variations show significant improvement to the channel mobility of silicon face 4H-SiC MOSFETs. The roughness of the $SiC/SiO_2$ was investigated by Fukuda *et al.*[98] for improvement of the channel mobility of carbon face 4H-SiC MOSFETs. They found the channel mobility of MOSFETs fabricated on the $(000\bar{1})$ 4H-SiC with 8$^o$ off-angle is approximately 10% higher than that of MOSFETs fabricated on $(000\bar{1})$ 4H-SiC with the vicinal (below 1$^o$) off-angle, although the lower one is already above 80cm$^2$/Vs. Considering the higher off-angle gives the higher roughness, they concluded that the roughness is a main factor affecting the channel mobility. The roughness can be revealed from the $D_{it}$ as obtained from C-V measurement, their conclusion is the same that the inversion channel mobility is determined by the interface quality.

As a summary, the interface quality of $SiC/SiO_2$ is significant in determining the performance of SiC-based MOSFETs. NO post-oxidation annealing not only can reduce the interface trap density, but also improves the inversion channel mobility of MOSFETs. The off-angle of substrate material can affect the performance of MOSFETs, while other factors do not show comparably significant effects on the channel mobility of MOSFETs.

# Chapter 4

## MOS Device Fabrication Techniques and Measurements

In this chapter, the experiment details of MOS devices fabricated on 4H-SiC will be discussed. The performance of a device is determined by the fabrication process. Statistical results for a set of devices depend dramatically on the consistency of the fabrication steps. Therefore, it is very important to methodically apply the key processes of device fabrication and strictly follow proven processing procedures. Careful characterization of the devices is important, as well. The most commonly used measurements for characterization will also be discussed in this chapter.

### 4.1 Oxidation

Oxidation is the most important step in MOS devices fabrication, since the oxide layer is the most critical part of the devices[50]. Different methods of oxidation have been used to improve the oxide reliability, as mentioned in chapter 3. Simply speaking, a layer of $SiO_2$ will be grown on a SiC wafer during the oxidation process. SiC is the only wide band gap semiconductor that has a tavie oxide, and thermal oxidation is the most commonly used method for SiC MOS devices fabrication[99]. There are two types of thermal oxidation: dry oxidation and wet oxidation. It should be noted that careful cleaning prior to oxidation is important for the oxide's quality. Detailed process of cleaning can be found in appendix A.

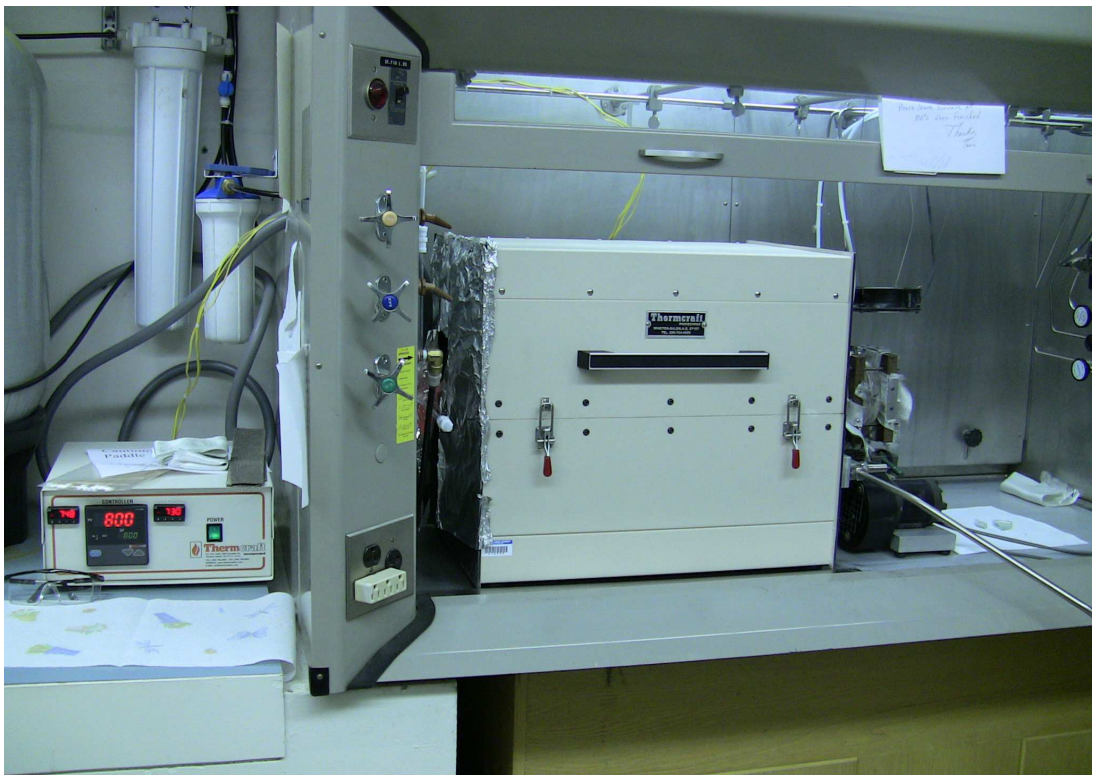


Fig. 4.1: Furnace for dry oxidation.

### 4.1.1 Dry Oxidation

Dry oxidation can be carried out in a quartz tube furnace, which is shown in figure 4.1. The oxygen gas is introduced at one end of the tube and exhausted from the other end. The typical oxidation process is as follows:

(1) Turn on argon gas and flush the quartz tube for 5minutes;

(2) Open the tube and load the wafer;

(3) Close the tube and hold the temperature at $900^oC$ for 30 minutes;

(4) Increase temperature at the step of $5^oC$/minute to $1150^oC$;

(5) Switch Argon to oxygen for oxidation for desired time;

(6) Switch oxygen to Argon;

(7) Decrease temperature at the step of $20^oC$/minute to $900^oC$;

(8) Open the tube and unload the oxidized wafer;

(9) Close the tube and turn off Argon gas and keep Argon at atmosphere pressure in the tube.

In step (1), Argon gas may be substituted by oxygen. The above dry oxidation process is carried out at atmospheric pressure, but lower pressure has also been used to study the relationship between the oxidation rate and pressure[16].

### 4.1.2 Wet Oxidation

The wet oxidation uses the similar facilities compared to dry oxidation. One difference is an additional input gas line added to introduce small flow of oxygen which contains moisture produced by passing the oxygen through deionized water heated to around $95^oC$. Figure 4.2 shows the DI-water container. Wet oxidation is carried out at temperature of

950$^o$C and atmosphere pressure. Since the introduced moisture may stay at the internal wall of the tube and affect future oxidation, the argon flow is usually used to flush the whole system afterward for at least 30 minutes.

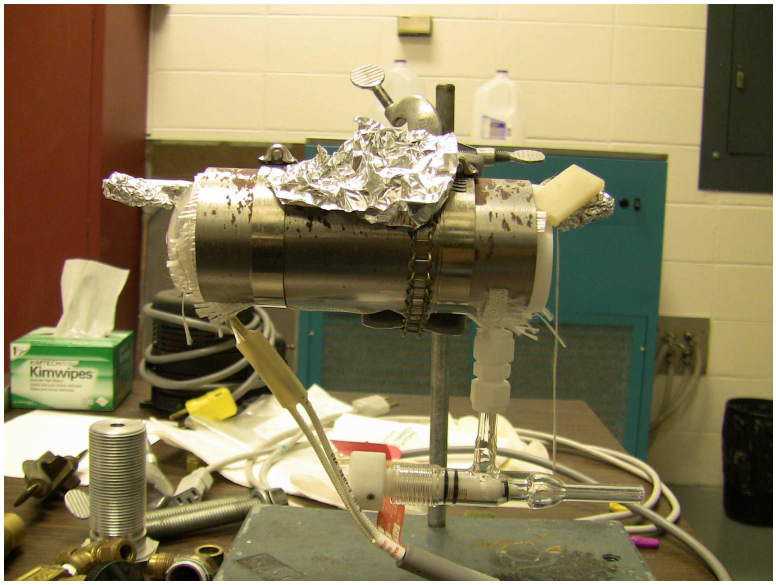


Fig. 4.2: Deionized water container for wet oxidation. The container is heated and two ends are connected to input and output gas lines.

### 4.1.3 Post-Oxidation Annealing

Post-oxidation annealing is an important process that is used to improve the interface quality for SiC/$SiO_2$. The anneal is usually performed in the same quartz tube furnace used for oxidation. The temperature of post-oxidation annealing depends on the type of annealing. For nitric oxide (NO) and ammonia ($NH_3$) post-oxidation annealing, the temperature is 1175$^o$C and the anneal time is 2hr. For $H_2$ post-oxidation annealing, the temperature is 500$^o$C for 1hr, and a thin layer of platinum is put on the surface of $SiO_2$ to

act as a hot catalyst to break the $H_2$ molecules into single atoms. It is noteworthy that $H_2$ molecules, instead of H atoms, are used to anneal $Si/SiO_2$ interface.

## 4.2 Lithography

Lithography is a method for pattern printing that has become an important step in the micro-fabrication process. There are two types of lithography in terms of accuracy requirements: microlithography and nanolithography. In microlithography, photolithography is the most commonly used, especially in the area of semiconductor manufacturing of microchips. Electron beam lithography is one of nanolithography methods. E-beam lithography can define the pattern with higher resolution, but lower speed, compared to photo-lithography. Other lithography methods include nanoimprint lithography, interference lithography, X-ray lithography, extreme ultraviolet lithography and scanning probe lithography. Photo-lithography, the main lithography tool in laboratory, will be discussed in the remainder of this section.

Figure 4.3 can be used to describe the general process of photo-lithography. The equipment that is used is a mask aligner, which is shown in figure 4.4.

There are two types of photoresist: positive photoresist and negative photoresist. The photoresist in figure 4.3 is a positive resist. If negative photoresist is used, the area exposed to ultraviolet light will remain after development and other unexposed areas will be washed. The developing solution is different for negative photoresist.

The photoresist is applied on the surface of sample by using spinner. The spinner sticks the backside of the sample with vacuum and rotates with a specific speed(usually 4000RPM) for a time interval(usually 30 seconds). The photoresist, applied on the center

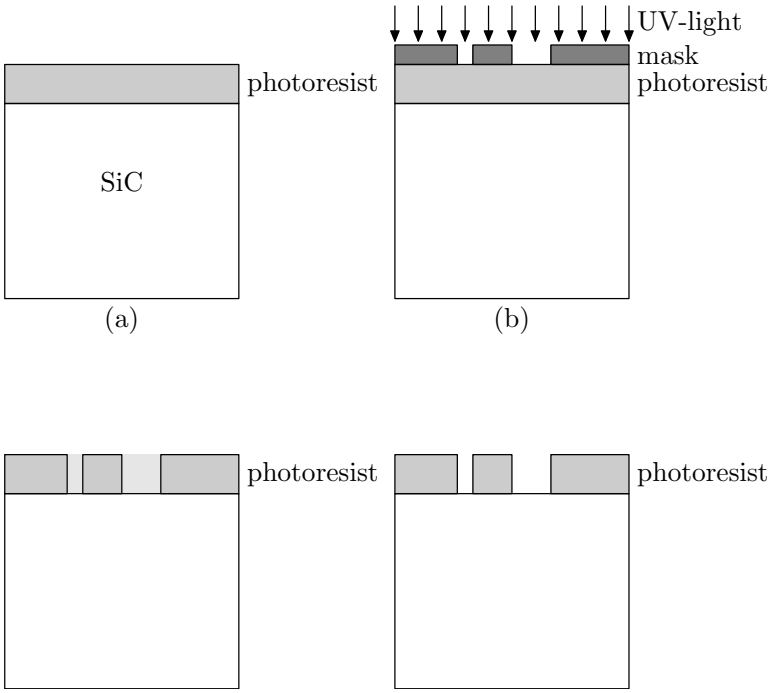


Fig. 4.3: Schematic of a general photo-lithography process. (a) Photoresist is applied on the SiC wafer; (b) The wafer is exposed through a mask to UV light; (c) A chemical reaction takes place in the exposed photoresist; (d) Photoresist after development.

Fig. 4.4: Mask aligner for photo-lithography.

of the sample, will spread out and coat the sample uniformly. The thickness of photoresist on the sample after spinning is greater than 10000Å. If the photoresist is too thin, the lift-off process might be difficult.

The soft baking is needed after spinning to make the photoresist become light-sensitive. The corresponding temperature is around $100^oC$ and baking time is 60 seconds. When exposing photoresist to UV light, it is important to make sample fully contact with the mask. Otherwise, the edge of photoresist will not be clear and the lift-off process may be affected. The power of UV light is 160W and exposing time is 30 seconds.

In the process of development of pattern, avoiding over-development is very important. It is a good habit to check the pattern with microscope several times during the development. If the edge of photoresist is clear and sharp, it means the development is fine.

Double exposing is required when inverse lithography is needed. Between the two exposing processes, there is another baking at the temperature of a little higher than $100^oC$ for 60 seconds. The second exposing process will last 60 seconds and no mask is applied.

### 4.3 Metal Deposition

Metal deposition can be accomplished by various methods. Sputtering deposition is one of them and this technique is used in our laboratory. The sputtering system is shown in figure 4.5 and the working mechanism is explained by figure 4.6.

The sputtering system is usually maintained at high vacuum. When samples are to be coated with a thin film, nitrogen gas is used to fill the chamber atmospheric pressure (760Torr). The samples are held by screws on the underside of substrate mounting plate, which can be rotated when multiple sputter targets are used. Four targets can be installed

Fig. 4.5: DC/RF sputtering deposition system.

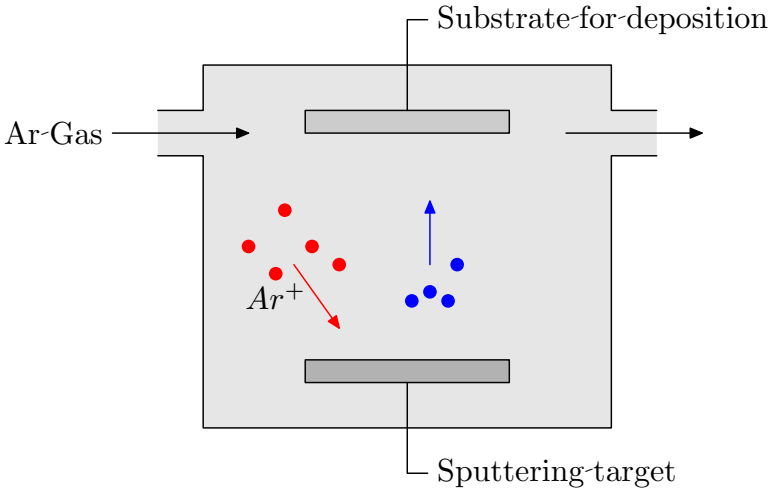


Fig. 4.6: Working mechanism of the sputter deposition process.

in the vacuum chamber at one time. The target to be used will be covered with an open glass chimeny to keep sputtered materials moving only vertically. Each chimney is only used for specific target to avoid cross contamination. When a sputter target is changed, the cooling water to the gun head must be shut off to prevent any water getting into the vacuum chamber. To avoid contamination, high vacuum must be obtained before sputtering. The usual achieved pressure is $4\times10^{-7}$Torr. The sputter gas is Argon.

## 4.4 Implantation

In order to dope a semiconductor sample, thermal diffusion and ion implantation can be used. For SiC however, the diffusion coefficients of most dopants are too low to get appreciable diffusion into crystal except at temperatures approaching the growth temperature of the material. Doping by ion implantation, therefore, has been widely adopted. A flux of ions with certain a energy penetrate to some depth below the SiC surface. Considering the energy loss of ions, the distribution of the single energy dopants in the sample wafer is a near-gaussian curve that has a trailing edge towards the surface of the sample. If a square doping profile is desired, ions with several energies can be implanted. With the help of the simulation software, SRIM, suitable energies and doses can be determined for the profile.

## 4.5 Activation

Implantation put dopants at the desired depth in a sample. However, the dopants remain primarily at interstitial site in the crystal until a high temperature activation anneal is performed. The process of activation will heal implant damage and reorganize the lattice structure of the crystal with implanted dopants moving from interstitial to lattice sites

where they become electrically active. Figure 4.7 shows the chamber used to carry out the activation anneal. In the chamber, two parallel carbon sesistive heaters are installed horizontally and connected to a DC power source. A round carbon box (Figure 4.8) is located between the carbon strips. Samples are located inside the carbon box during the process of activation. A temperature of 1550$^o$C is used to activate nitrogen dopants, and 1650$^o$C is used to activate aluminum dopants. In order to avoid the loss of Si from the SiC surface during the activation anneal, a carbon cap is used to cover the implanted surface. The cap is formed by coating photoresist on the surface of SiC followed by 30min anneal in Argon at 600$^o$C. During the activation anneal, Argon gas at 1atm is flowing through the chamber at all time.

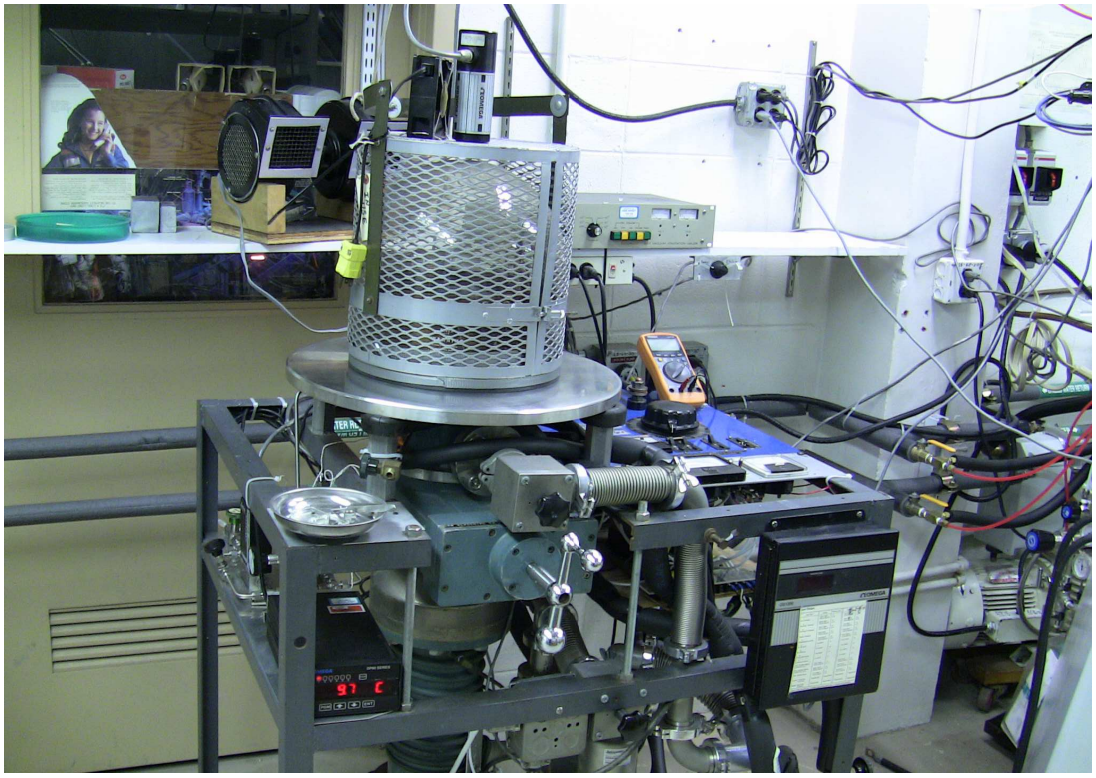

Fig. 4.7: Implant activation anneal chamber.

Fig. 4.8: Sample holder carbon box for implant activation.

## 4.6 Ohmic Contact Annealing

During the fabrication of MOSFETs, the source and drain regions are heavily doped, and Ni is used to make ohmic contacts to the S/D regions. However, the as-deposited metal/semiconductor structure yields a Schottky contact, which is transformed to an ohmic contact with a linear current-voltage characteristic using a short, high temperature anneal. Based on experience, an optimized temperature for our MOSFETs is $\sim 900^{o}$C/4min/Ar(1atm). Figure 4.9 shows the ohmic contact annealing equipment in our laboratory.

## 4.7 Etching

Etching processes are required im many of the steps for MOSFET fabrication. For instance, a buffered oxide etchant (BOE) is used to etch $SiO_2$ and $NF_3$ is used to reactively ion etch SiC. The choice of etching method is important in order to selectively remove layers (oxide, metal, SiC, etc.) during the fabrication process.

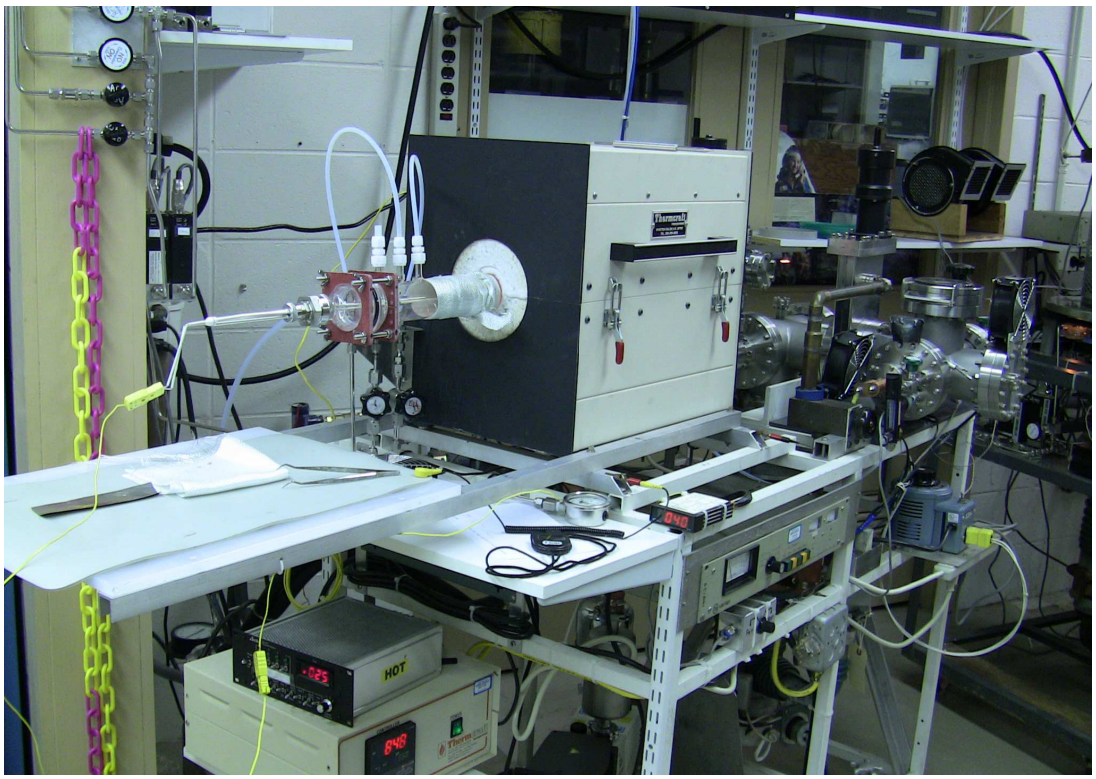


Fig. 4.9: Ohmic contact annealing furnace.

### 4.7.1 BOE Etching

Buffered oxide etchant (BOE) is an excellent etchant for $SiO_2$. BOE does not react with SiC or silicon, and at room temperature, the etch rate of $SiO_2$ by BOE is around 1000Å/min. To protect $SiO_2$, baked or carbonized photoresist is used as the mask. Since the sample must be dipped into the BOE solution during the etching process and the etching is isotropic, the time of etching must be set as precisely as possible to avoid unwanted lateral etching after the $SiO_2$ layer is etched through to the SiC substrate.

### 4.7.2 RIE

RIE is an acronym for reactive ion etching. Figure 4.10 shows the RIE equipment that is used in our laboratory. The plasma is created in a closed chamber filled with a specific gas (e.g., $NF_3$ or $SF_6$). The ions created in the RF plasma can react chemically with the substrate material we wish to remove. Masks have to be used to protect the regions we wish to be keep unetched. In the fabrication of a MOSFET, active areas are protected with nickel, and the devices are fabricated on an isolation mesa with sides etched down a few hundred nanometers using an $NF_3$ plasma.

### 4.7.3 KOH Etching

Another method for etching SiC wafer is KOH etching. The KOH is heated to a molten state, at around $550^oC$. This etching is commonly used to enlarge and observe the defects in a SiC wafer. The KOH technique is very useful when studying the relationship between oxide breakdown and substrate defect density.

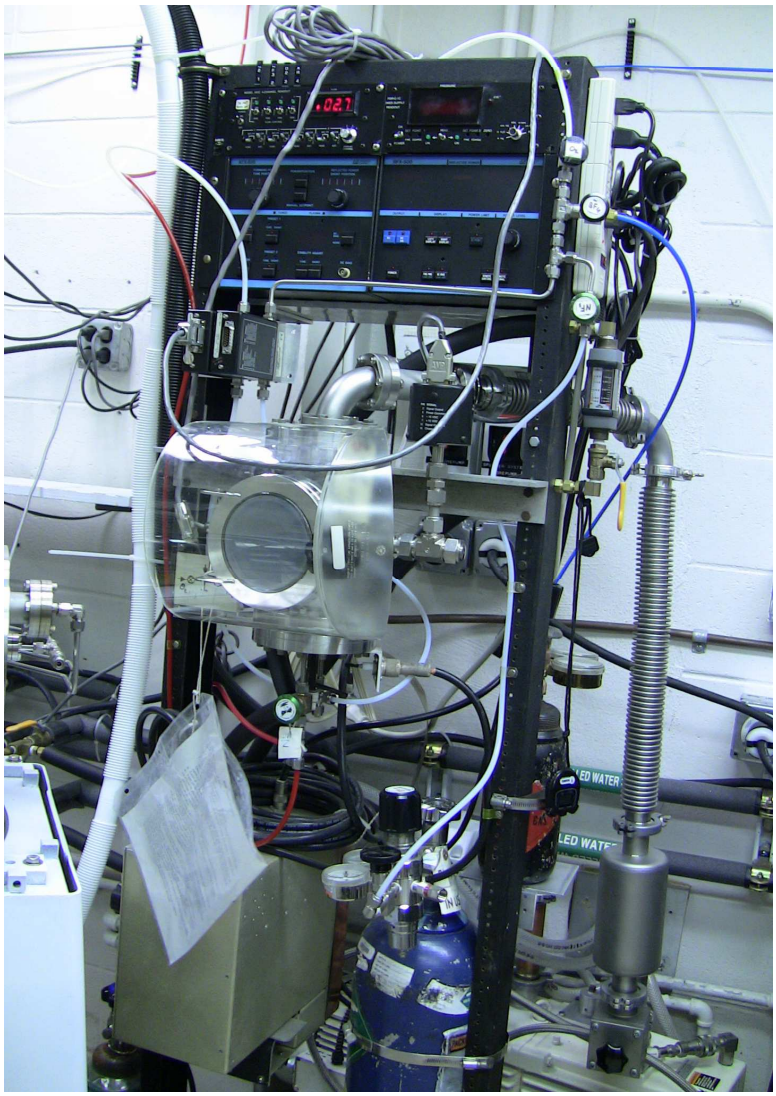

Fig. 4.10: Equipment for reactive ion etching.

## 4.8 Capacitance-Voltage Measurements

In order to understand the electrical properties of MOS devices, especially interface characteristics, capacitance-voltage measurements are employed. The C-V measurements in our laboratory are made with Keithley 595 analyzer and a Keithley 590 CV meter, shown in figure 4.11. The Keithley 595 analyzer measures the high-frequency capacitance, and 590 CV meter measures the quasi-static capacitance. Both measurements are made simultaneously.

A typical high-low CV curve for an n-type MOS capacitor is shown in figure 4.12. In the figure, the red curve represents the quasi-static capacitance, and the black curve represents the high frequency capacitance. The high frequency curve does not reflect the effects of interface defects because the defects - as they fill an empty - cannot follow the high frequency signal. However at room temperature, the interface traps with energies between $E_C$ and approximately $E_C$-0.6eV do follow the much slower quasi-sttic signal as they trap and emit electrons. This additional charge motion contributes to the measured capacitance, making the quasi-static capacitance higher than the high-frequency capacitance for a given bias voltage. The energy level of a trap in the band gap is determined by the position of the Fermi level at the SiC surface for a given bias voltage. The difference between $C_{QS}$ and $C_{HF}$ is used to calculate the defect state density at a specific energy level.

For CV measurements, temperature has an important effect on the results. Since SiC is a wide gap semiconductor material, the defects states which are at deep energy levels ($\sim E_C$-0.6eV to mid-gap)can not respond to quasi-static bias changes at room temperature. Therefore, to obtain the defect state density between the conduction band edge and

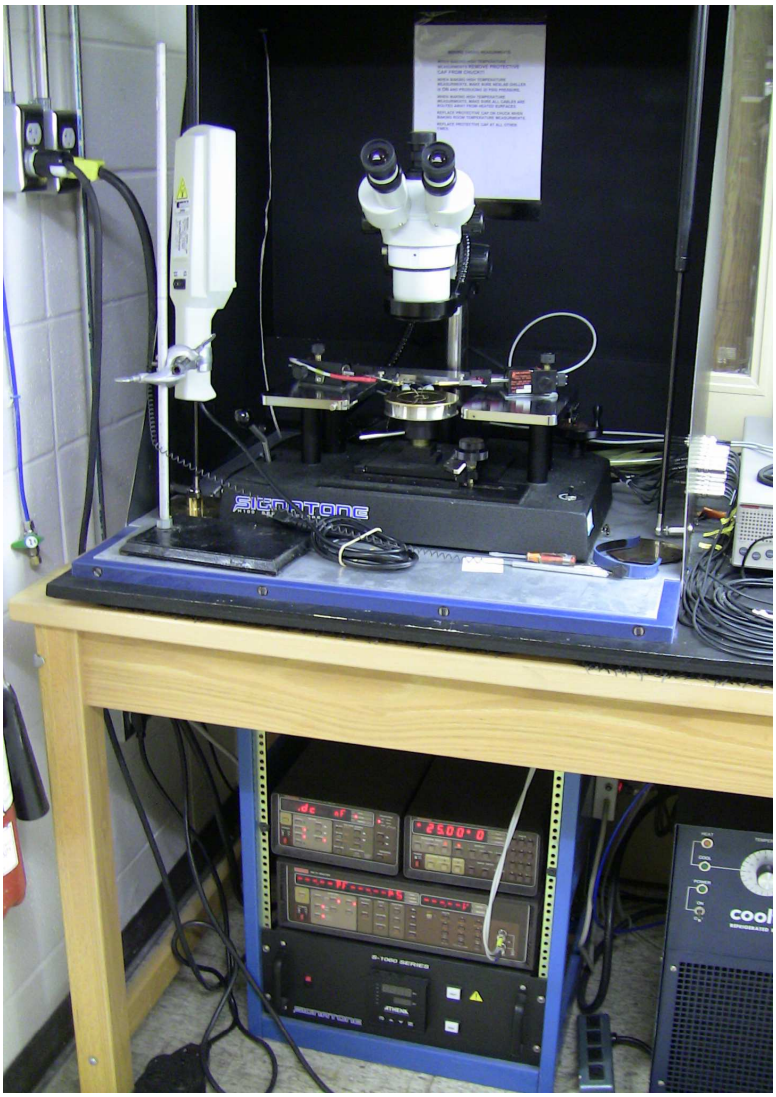


Fig. 4.11: Simultaneous high-low capacitance-voltage station.

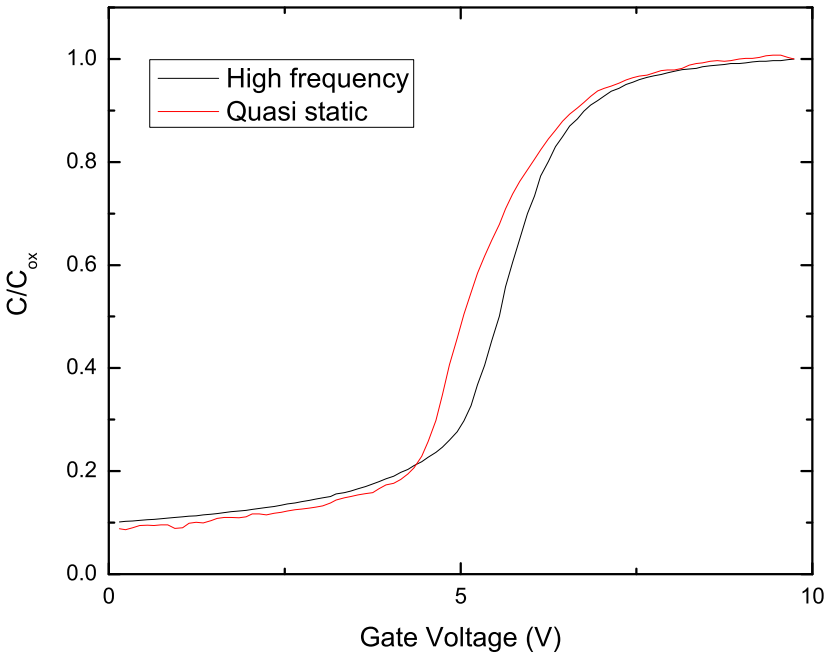


Fig. 4.12: A typical plot of capacitance v.s. gate voltage of n-type MOS capacitor with a thermal oxide annealed in NO.

mid-gap, different CV measurements are normally made at $23^oC$ and $300^oC$. The $300^oC$ measurements are used to measure defects states 0.6eV$\sim$1.6eV below the conduction band edge. Sometimes, to make the two regions connect smoothly, one extra measurement will be made at $150^oC$.

Measurements with N-type material only give trap densities in the upper half states of the band gap. P-type material can be used to obtain trap densities in the bottom half of the gap.

## 4.9 Current-Voltage Measurements

Current-voltage (I-V) measurements are used to obtain breakdown information for the oxides in MOS devices. The voltage is applied on the gate of the devices, and the current flowing through the oxide layer is detected. When a preset limit for current is achieved, the test is usually stopped in order to prevent catastrophic oxide breakdown.

I-V measurements can be made not only at room temperature, but also at high temperature for the purpose of accelerated reliability testing. Figure 4.13 shows the I-V measurements station.

### 4.9.1 TDDB

Time Dependent Dielectric Breakdown (TDDB) measurements are used to test the reliability of devices. Compared to anticipated operating conditions, devices are subject to higher temperature and higher voltage (i.e., higher oxide field) in order to shorten the testing time. Figure 4.14 shows the measurement board layout, which allows 36 MOS capacitors

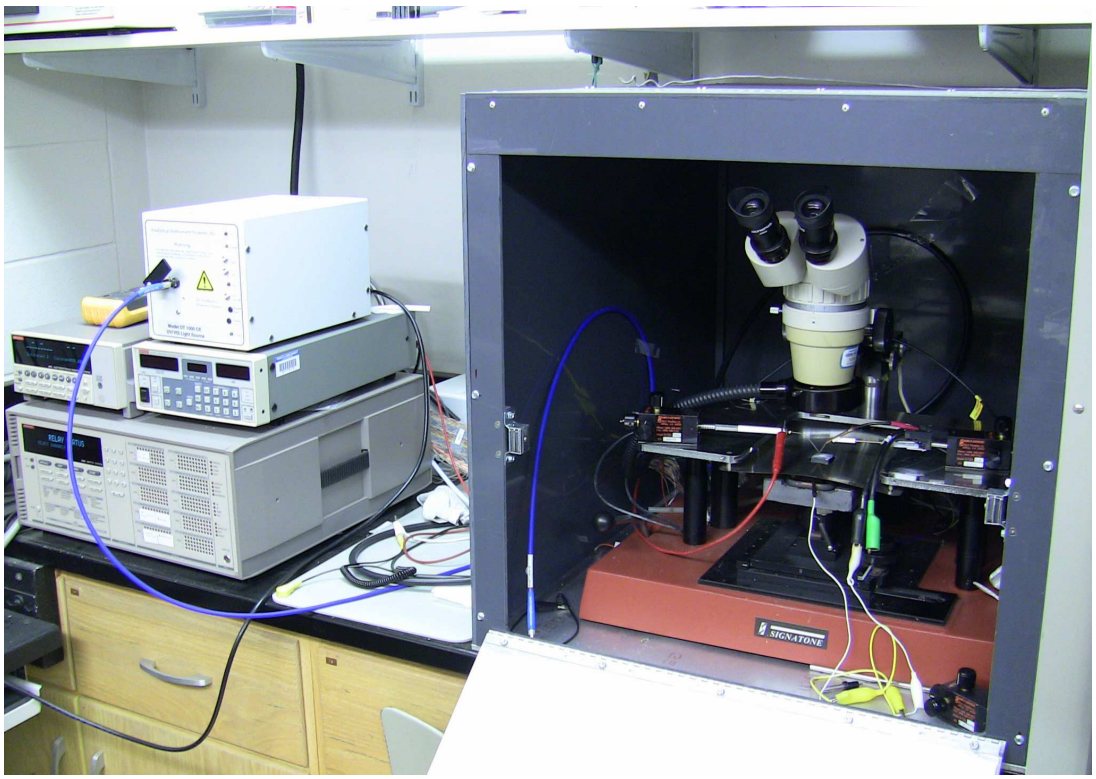


Fig. 4.13: Current-voltage station.

to be monitored simultaneously with software programed in Labview. The Labview user interface is shown in figure 4.15.

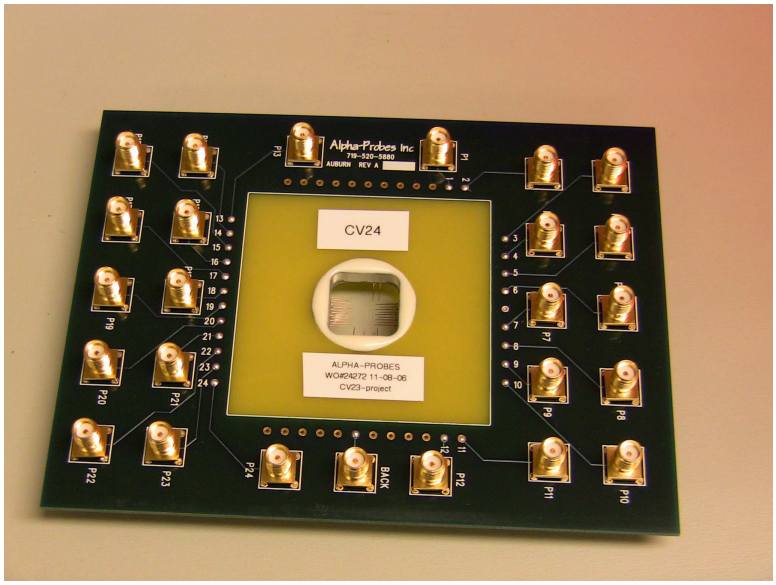


Fig. 4.14: TDDB measurement board.

## 4.10 MOSFET Measurements

MOSFET devices have gate, source and drain contacts. Therefore, three probes are needed for characterization measurements. The effective channel mobility is usually measured by setting a constant source-drain voltage (typically 25mV) and measuring the source-drain current as a function of gate voltage. Figure 4.16 shows the station that used for these measurements,and figure 4.17 shows the user interface of MOSFET measurement program.

As mentioned, a small voltage is applied between the source and drain contacts, and the gate voltage is stepped during the measurement. The gate current is monitored while the source-drain current is measured. Since $V_d$ (drain voltage) is small compared with $V_g$, the linear model can be used to describe operation of the MOSFET. According to chapter

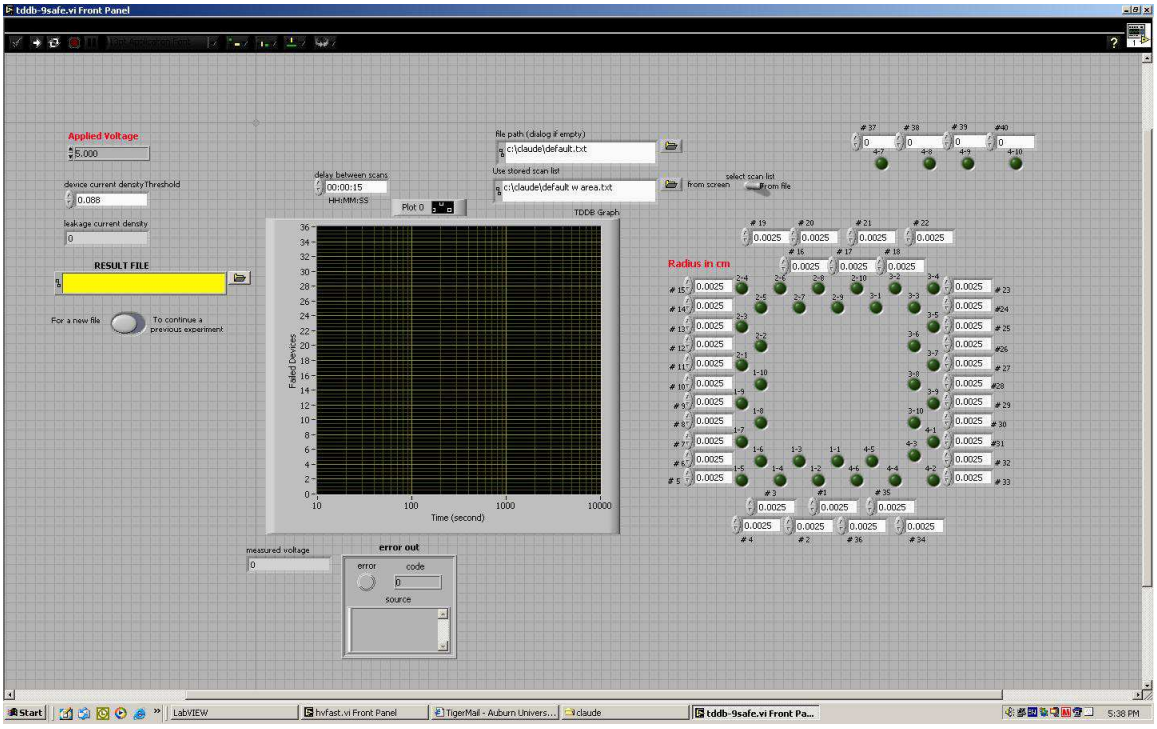


Fig. 4.15: The user interface of TDDB measurement program.

2, the mobility can be evaluated as a function of $V_g$. Simply speaking, the peak value of mobility will occur when the slope of $I_d$ (drain current) versus $V_g$ has the maximum value. It should be noted that the gate current should be kept small ($\sim 10^{-10}$A or less), otherwise current leakage through the oxide of the oxide layer will be a concern.

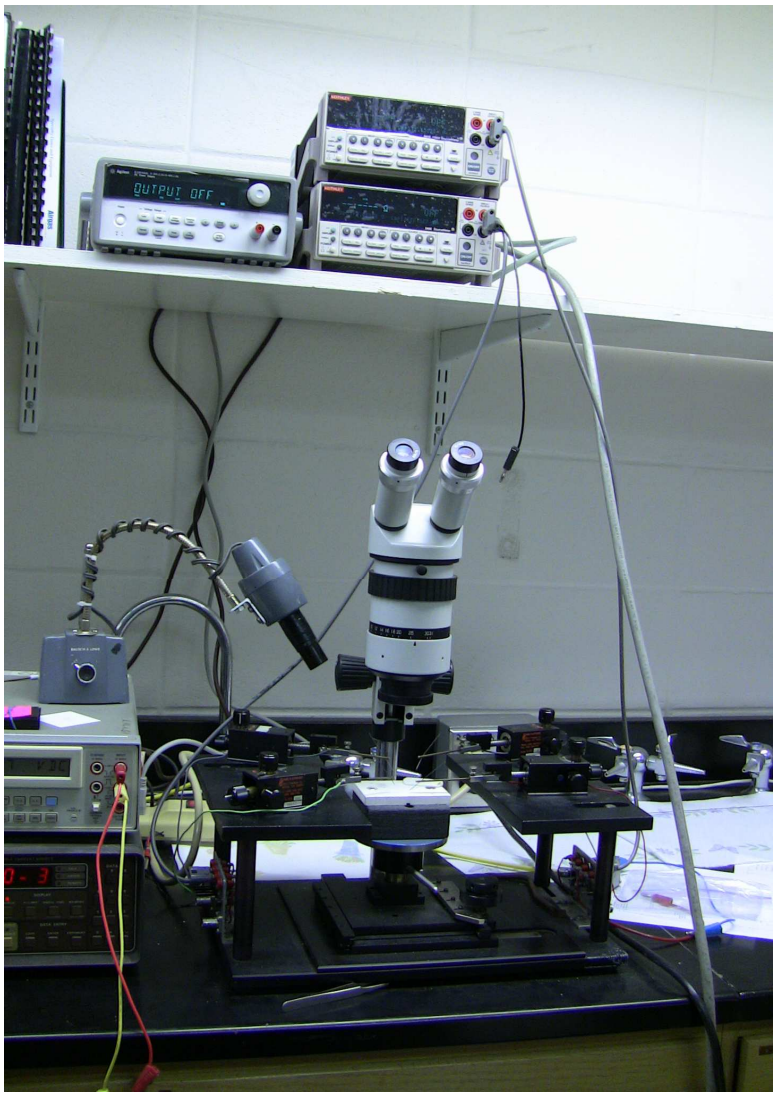


Fig. 4.16: The three probe current-voltage measurement station consisting of a KI-2400 source meter, a KI-2410 source meter, a microscope and a sample holder.

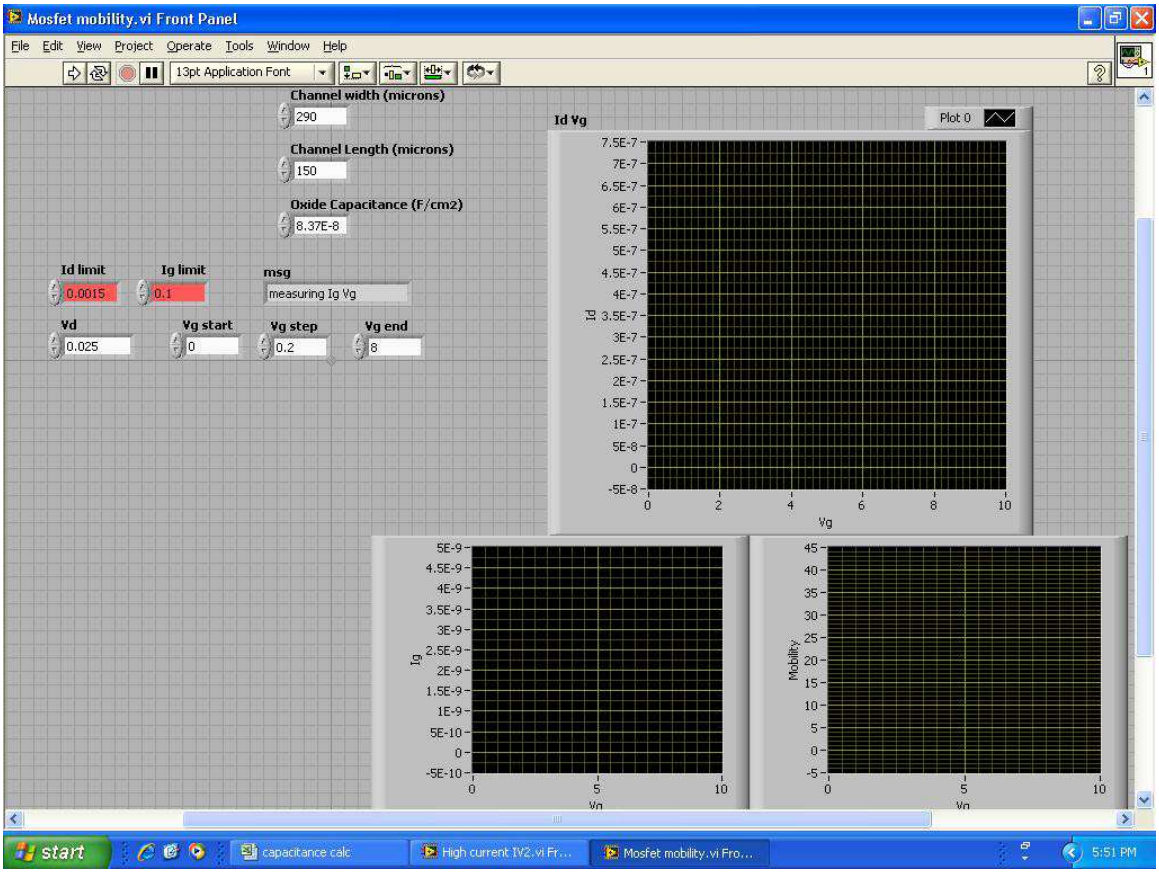


Fig. 4.17: The user interface of MOSFET measurement program.

# Chapter 5

## Characterization of MOS Devices Fabricated on Carbon Face 4H-SiC

In this chapter, MOS capacitors and MOSFETs built on carbon face 4H-SiC will be discussed. High-low capacitance-voltage measurements and current-voltage measurements are used to study the properties of carbon face 4H-SiC/$SiO_2$: interface trap density, oxide breakdown field and inversion channel mobility. Several different oxidation processes are used to grow $SiO_2$ on SiC wafer and improve the interface quality of SiC/$SiO_2$. The results are discussed and compared to the case of the silicon face.

### 5.1 Background

From the previous chapters, it has been shown that SiC has a higher thermal conductivity, wider band gap, and higher critical breakdown field than silicon. 4H-SiC also has comparable bulk electronic mobility to silicon. All of these properties make SiC an excellent candidate for power MOSFET construction. However, the channel mobility of SiC is significantly lower than that of silicon and many people believe it is because the interface trap density of SiC/$SiO_2$ is high[63, 100, 101]. In order to improve the channel mobility of SiC, as well as the interface quality, much work has been done on various polytypes and different orientations[58, 95, 100, 102–104]. The carbon face 4H-SiC has a higher oxidation rate than the silicon face. The higher oxidation rate will save time during MOS devices fabrication and lead to potentially large savings in cost. The carbon face 4H-SiC also has been reported to

Table 5.1: The oxidation rates of (0001) and (000$\bar{1}$) 4H-SiC

| | $O_2$ | NO |
|---|---|---|
| (0001) 4H-SiC | 80Å/hr | 6Å/hr |
| (000$\bar{1}$) 4H-SiC | 730Å/hr | 50Å/hr |

have high channel mobility[98]. Therefore much interest has been attracted in the carbon face 4H-SiC.

## 5.2 Oxidation Rate

The oxidation rate on different orientations of 4H-SiC is studied. The carbon terminal and the silicon terminal are compared for the speed of oxidation. For sake of simplicity, the carbon terminal will be written as (000$\bar{1}$) and the silicon terminal will be written as (0001). The results are shown in table 5.1.

The growth rate of oxide on the carbon face 4H-SiC is approximately 9 times higher than that on the silicon face.

## 5.3 (000$\bar{1}$)4H-SiC/$SiO_2$ Interface

### 5.3.1 Experiments

In order to investigate the interface issue of carbon face 4H-SiC/$SiO_2$, MOS capacitors were fabricated as test devices. The experiments started with 4H-SiC wafers bought from Cree. Diced into 5mm×5mm pieces, wafers were cleaned with organic cleaning and RCA cleaning (see appendix A for details on cleaning). An oxide layer with the thickness of ∼75nm was grown on the surface of SiC in 1150$^o$C furnace, followed by post-oxidation annealing. Nitric oxide (NO) post-oxidation annealing was done for 2hr at a temperature

of 1175$^o$C, while $H_2$ annealing was done at 500$^o$C for 1hr with a thin layer of platinum coating on the surface of $SiO_2$. Photo-lithography was then used to define the pattern of MOS capacitors on the oxide layer. High purity Mo was deposited as the gate metal by sputtering. Another thin layer of oxide was usually grown on the backside of SiC at the time of oxidation, must be removed by buffered oxide etchant (BOE) to make ohmic like contacts. Silver paste was finally used to attach the MOS capacitor sample to Au-coated ceramic prior to measurement.

### 5.3.2 Results and Analysis

Room temperature (23$^o$C) and High temperature (300$^o$C) hi-lo CV measurements are employed to collect capacitance versus gate voltage of MOS capacitor devices. Figure 5.1 shows the room temperature CV curves of an MOS capacitor with as-oxidized oxide. The difference between high frequency and quasi-static curves is large, and this implies that the interface trap density $D_{it}$ at the near end of the conduction band is high. The $D_{it}$ profile is shown in figure 5.2. Since the oxide is "weak", it is difficult to make the device stay at accumulation. Therefore it is difficult to get an accurate interface trap density profile. It should be noted that the high temperature CV measurements could not be performed due to the same reason. Thus, it is reasonable to imply that $D_{it}$ of as-oxidized sample is very high and it is not necessary to discuss as-oxidized method later in this chapter.

#### NO Passivation

To improve the interface quality or decrease the defects states density in the band gap, post-oxidation annealing must be carried out. Since NO has been proved effective

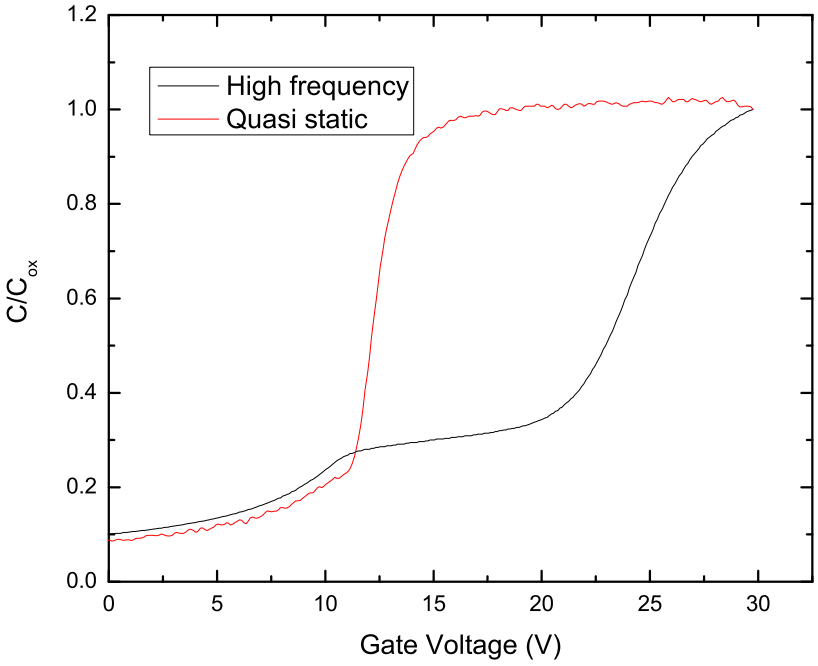


Fig. 5.1: Capacitance v.s. gate voltage of an MOS capacitor with as-oxidized oxide.

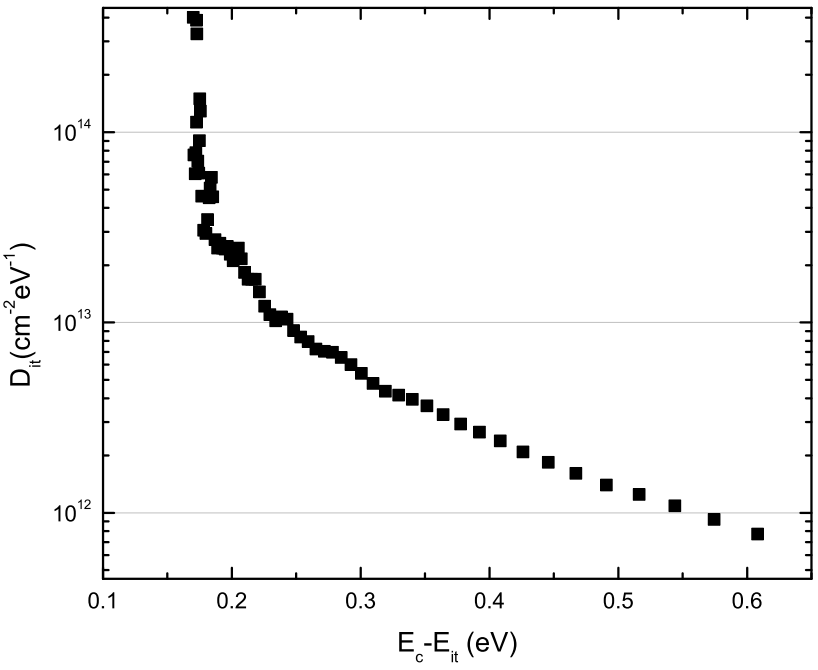


Fig. 5.2: Interface trap density profile of an MOS capacitor with as-oxidized oxide.

for enhancing the silicon face 4H-SiC/$SiO_2$ interface[58], it was used in the post-oxidation annealing for the carbon face 4H-SiC/$SiO_2$. The capacitance versus gate voltage plot of the carbon face MOS capacitor is shown in figure 4.12. It is interesting to compare figure 5.1 and figure 4.12. After NO annealing, high frequency and quasi-static curves are much closer. Moreover, a more stable accumulation region exists. Figure 4.12 suggests that the interface defects states are reduced dramatically and the oxide is "stronger" compared to the as-oxidized sample. From figure 4.12, the interface trap density can be estimated, as shown in figure 5.3. Both shallow levels and deep levels are presented. It should be noted that NO creates a new thin layer of oxide over the original oxide.

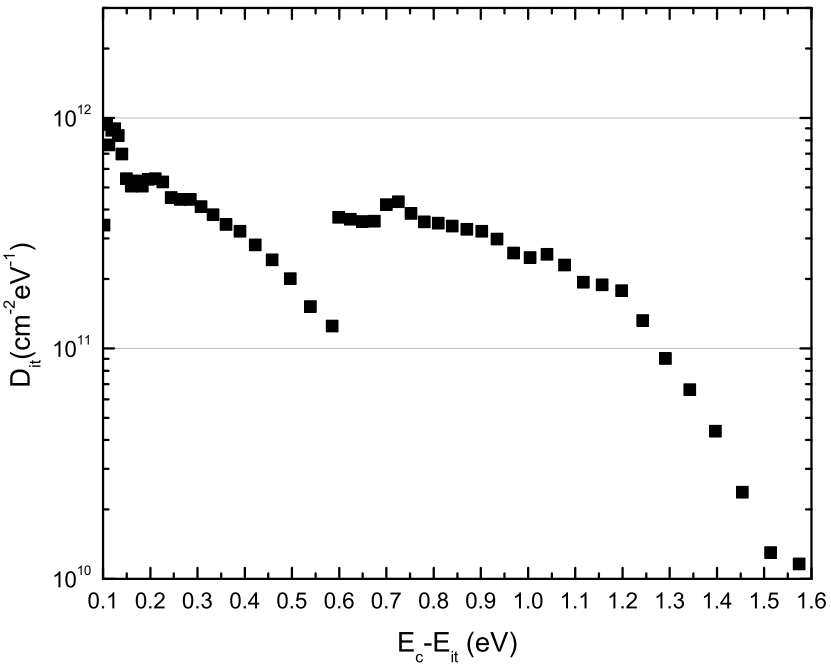


Fig. 5.3: Interface trap density profile of an MOS capacitor with NO passivated oxide.

The effectiveness of NO passivation on enhancement of interface quality for other polytypes of SiC has also been reported[57, 58, 77]. It is suggested that the carbon clusters produced during the oxidation are passivated by nitrogen atoms and, as a result, lead to the lower interface states density. In the case of the carbon face 4H-SiC, carbon clusters are the main cause of the interface defects[56]. Therefore, it is not surprising that NO passivation has a significant effect on reduction of interface defects of the carbon face 4H-SiC.

### $H_2$ Passivation

$H_2$ passivation has been shown capable reducing the interface defects states for $Si/SiO_2$[83]. $H_2$ was also tried to improve the interface of the silicon face $4H\text{-}SiC/SiO_2$[56], but the results were not as good as on $Si/SiO_2$. In the research on the carbon face 4H-SiC, $H_2$, cracked by platinum into atoms, is used again to test the effectiveness on improvement of interface. Figure 5.4 shows the interface defects states density after $H_2$ passivation. Comparison with the interface defects states density of as-oxidized oxide shows that $H_2$ passivation does not yield much improvement. This means that using only $H_2$ in the passivation can not improve the interface of the carbon face 4H-SiC enough. Since $H_2$ can effectively passivate slicon-related defects[56], it is suggested that the main defects at the interface of 4H-SiC, both the silicon face and the carbon face, are not silicon-related.

### Wet Re-oxidation

An alternative approach to introduce H atoms into the interface of $SiC/SiO_2$ is the wet re-oxidation. The experiment details have been discussed in Chapter 4. With similar results to platinum $H_2$ passivation, this method does not enhance significantly the carbon

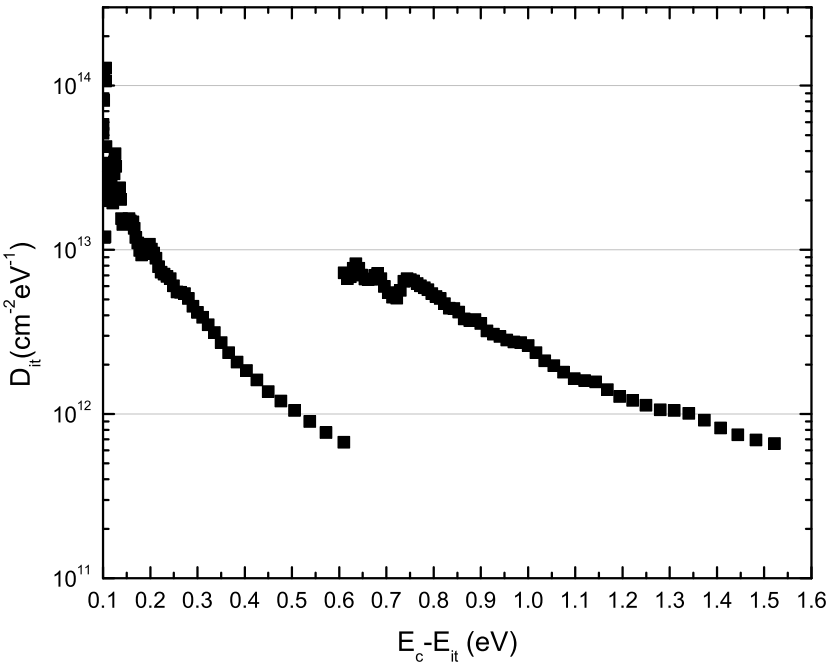


Fig. 5.4: Interface trap density profile of an MOS capacitor with Pt-$H_2$ passivated oxide.

face 4H-SiC/$SiO_2$ interface[58]. Similar as NO passivation, this process will grow another layer of oxide and growth rate is even higher than dry oxidation.

### Combination of NO and $H_2$ Passivation

Although pure $H_2$ passivation does not work successfully to enhance the interface of SiC/$SiO_2$, the combination of NO and $H_2$ passivation has been found effective in reducing the interface defects states density of the silicon face 4H-SiC/$SiO_2$[85]. In case of the carbon face, this combination also works. In this approach, $H_2$ passivation is performed after NO treatment. Figure 5.5 shows the interface trap density of the carbon face 4H-SiC/$SiO_2$ after NO and $H_2$ post-oxidation annealing. For both shallow levels and deep levels, the trap densities are apparently lower than only NO annealing. At 0.2eV below the conduction band, the $D_{it}$ is approximately $5\times10^{11}cm^{-2}eV^{-1}$.

### Wet Re-oxidation Followed by NO Passivation

When NO passivation is performed after wet re-oxidation, the interface quality of the carbon face is better than only NO treatment. Figure 5.6 shows the results.

In summary, the $D_{it}$ of the carbon face 4H-SiC/$SiO_2$ profiles for different post-oxidation annealing methods are shown in figure 5.7. For comparison, the silicon face $D_{it}$ is shown in figure 5.8. Clearly, the combination of NO and $H_2$ passivation results in the best interface quality for the carbon face 4H-SiC/$SiO_2$. However, it is still worse than the best silicon face interface which is also passivated by NO and $H_2$.

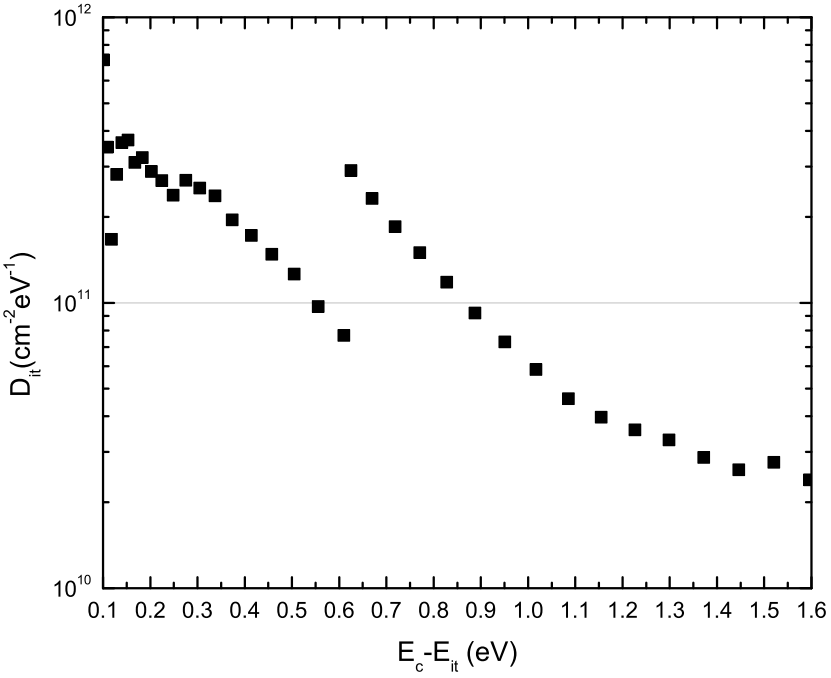


Fig. 5.5: Interface trap density profile of an MOS capacitor with NO and Pt-$H_2$ passivated oxide.

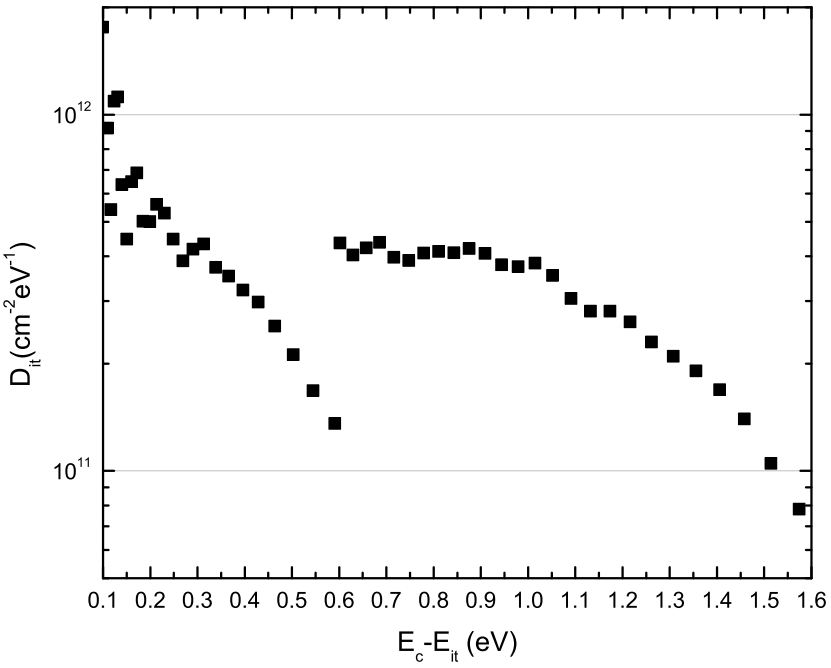


Fig. 5.6: Interface trap density profile of an MOS capacitor with wet re-oxidation and Pt-$H_2$ passivated oxide.

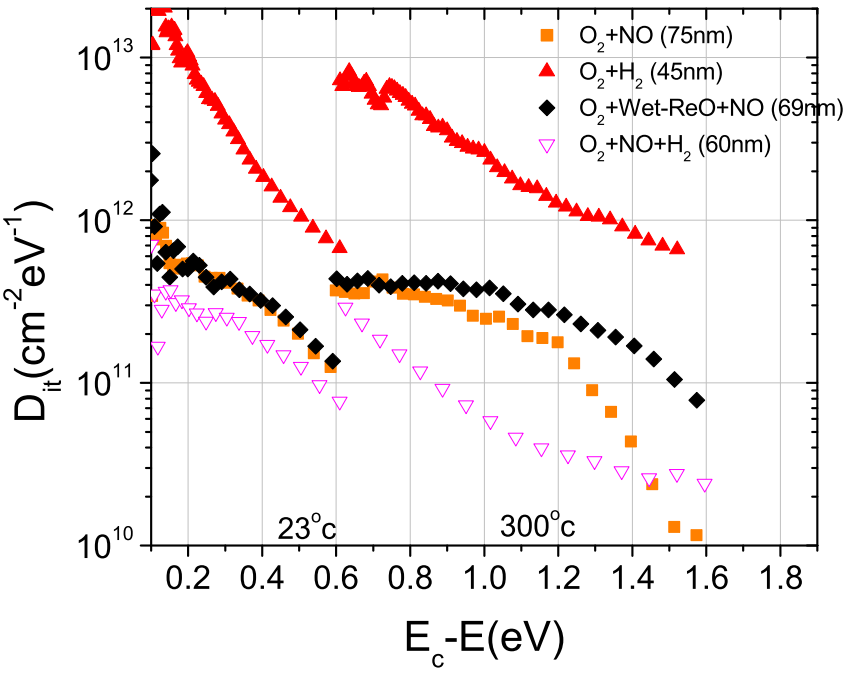


Fig. 5.7: Interface trap density profiles of carbon face 4H-SiC/$SiO_2$ with different interface treatments.

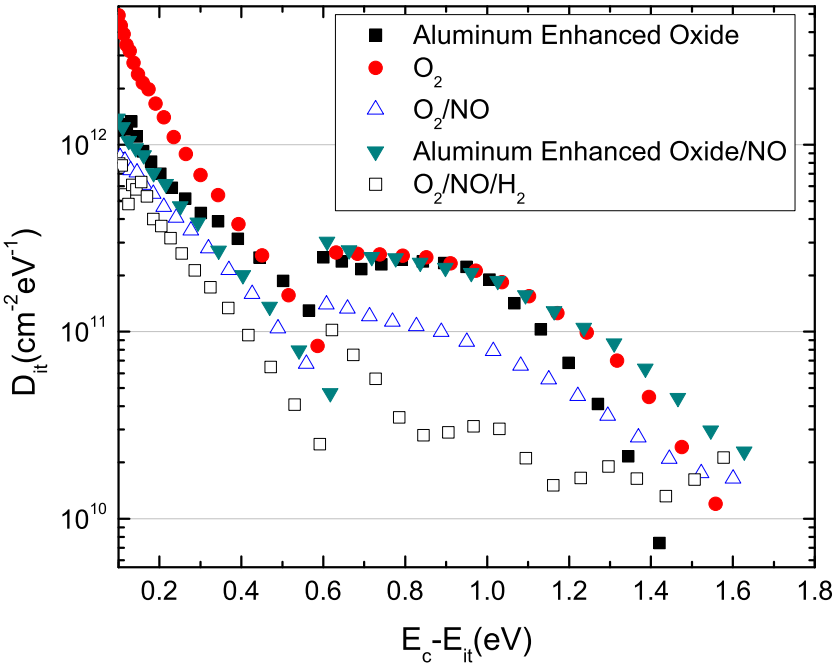


Fig. 5.8: Interface trap density profiles of silicon face 4H-SiC/$SiO_2$ with different interface treatments.

## 5.4 Oxide Breakdown

### 5.4.1 Experiments

In order to test the reliability of oxide layer, I-V measurements were performed. In I-V measurements, voltage was applied on the gate of a MOS capacitor and scanned from 0 to a high value at which the breakdown of the oxide occurred. Given the thickness of the oxide and the interface information, the breakdown voltage can be converted into breakdown field (see equation 3.1).

### 5.4.2 Results and Analysis

Similar as in the section of the interface, different oxidation methods are investigated in oxide breakdown experiments. Figure 5.9 shows the I-V curves of these MOS capacitors.

From figure 5.9, all oxides perform similarly at high field. If breakdown current density is set to be $1\times10^{-4}$A/cm$^2$, then all oxides will breakdown at nearly the same breakdown field ($\sim$5.5MV/cm). At low field, different behaviors are shown for different oxide growth. The oxide with wet re-oxidation and NO passivation maintains a low current density until 4MV/cm, while other oxides show slight leakage at low field.

Two different types of gate materials are used in the MOS capacitors. The comparison results are shown in figure 5.10, which suggests that the gate materials do not have obvious effect on the breakdown of the oxide. However, at the low field, the leakage of the oxide passivated by $H_2$ is higher compared to other oxides. This is likely because the deposition and removal of platinum may damage the oxide.

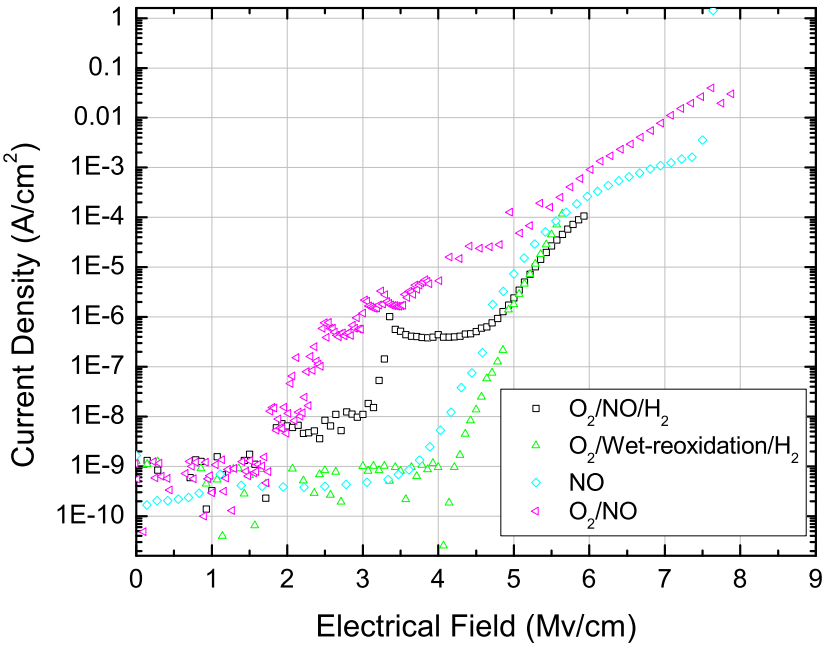


Fig. 5.9: Current-voltage measurements for carbon face 4H-SiC MOS capacitors.

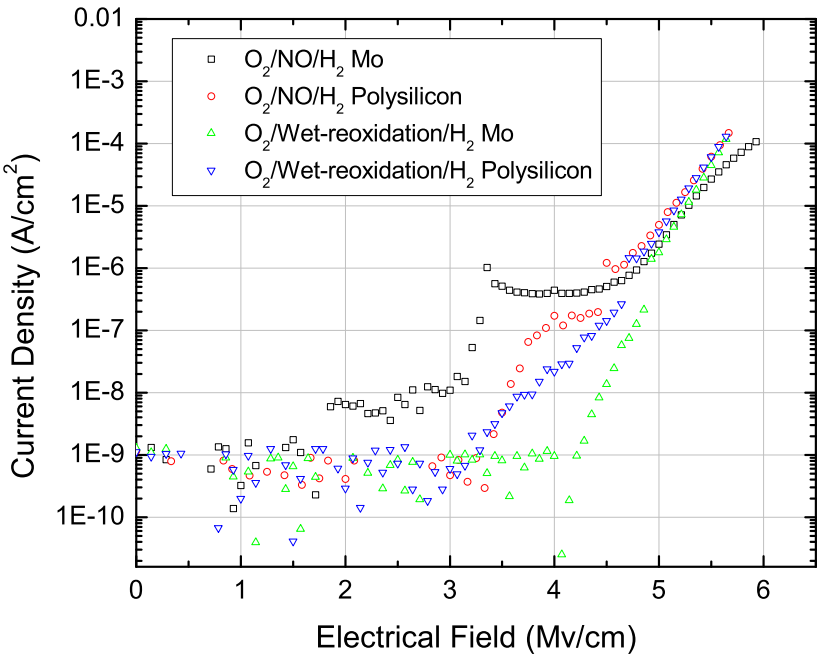


Fig. 5.10: Current-voltage measurements for carbon face 4H-SiC MOS capacitors with different gate metals.

The I-V measurements for the silicon face 4H-SiC MOS capacitors are shown in figure 5.11. Apparently, the best silicon face MOS capacitor has a breakdown field 2MV/cm higher than that of the carbon face. This means the silicon face oxide has better oxide quality than the carbon face oxide.

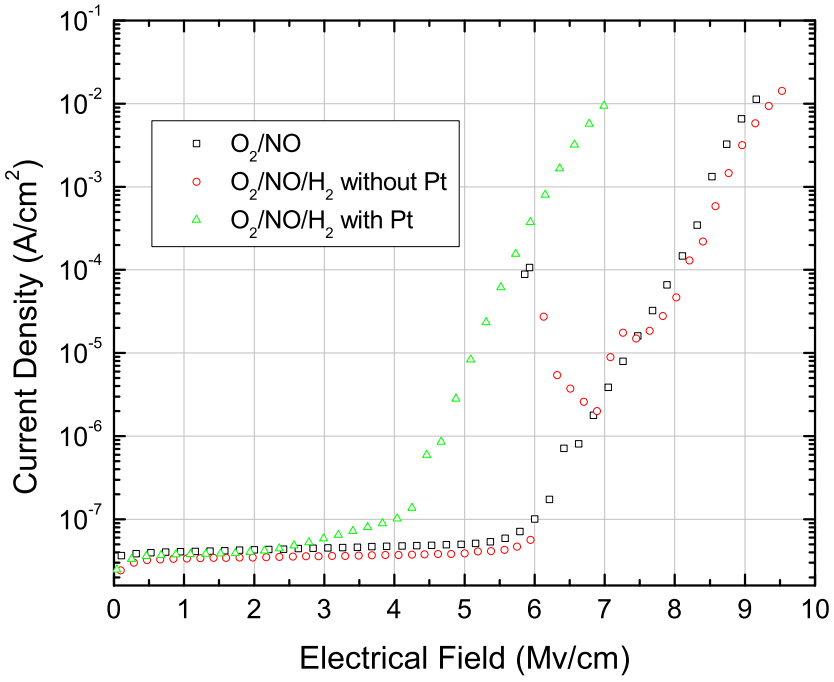


Fig. 5.11: Current-voltage measurements for silicon face 4H-SiC MOS capacitors with different gate metals.

## 5.5 MOSFET Channel Mobility

### 5.5.1 Experiments

The fabrication process for MOSFETs is more complicated than that of MOS capacitors. Each sample was 5mm×5mm in size. The substrate was the p-type carbon face

4H-SiC. Two kinds of substrates were used. One was p-implanted material with the implant concentration of $2\times10^{17}\text{cm}^{-3}$, which was formed by implanting $Al^+$ into the n-type carbon face 4H-SiC at $700^o$C. The other, bought from Cree, was p-epi material with doping concentration of $5\times10^{15}\text{cm}^{-3}$. The source and drain regions were 4000Å in depth, formed by N implantation at $700^o$C with the implant concentration of $6\times10^{19}\text{cm}^{-3}$. Figure 5.12 and figure 5.13 show the N and Al implantation profiles simulated by SRIM. The activation temperatures after implantations were $1550^o$C and $1650^o$C for N implantation and $Al^+$ implantation, respectively. During the activation, the surface of sample was covered with carbon cap, which was carbonized photo-resist, in order to avoid out-flow of silicon atoms from SiC surface. The carbon cap was removed afterward by reactive ion etching (RIE) in oxygen environment. A layer of sacrificial oxide was grown on the surface of sample and then removed to reduce the effect of surface roughness on the device. The gate oxide with the thickness ranging from 40nm to 75nm was grown under the same conditions as used when the oxide of MOS capacitor was grown. BOE was used to open windows in the oxide above source and drain regions. Nickel was sputtered onto the source/drain regions prior to ohmic contact annealing. Optimized conditions for ohmic contacts formation were found to be $950^o$C for time of 4min. Figure 5.14 shows the measurement results of a TLM sample after ohmic contact annealing (see Appendix B for details of TLM measurements). After ohmic contact annealing was complete, high purity Mo was sputtered as the gate metal. The MOSFET devices had a channel length of 150$\mu$m and a channel width of 290$\mu$m.

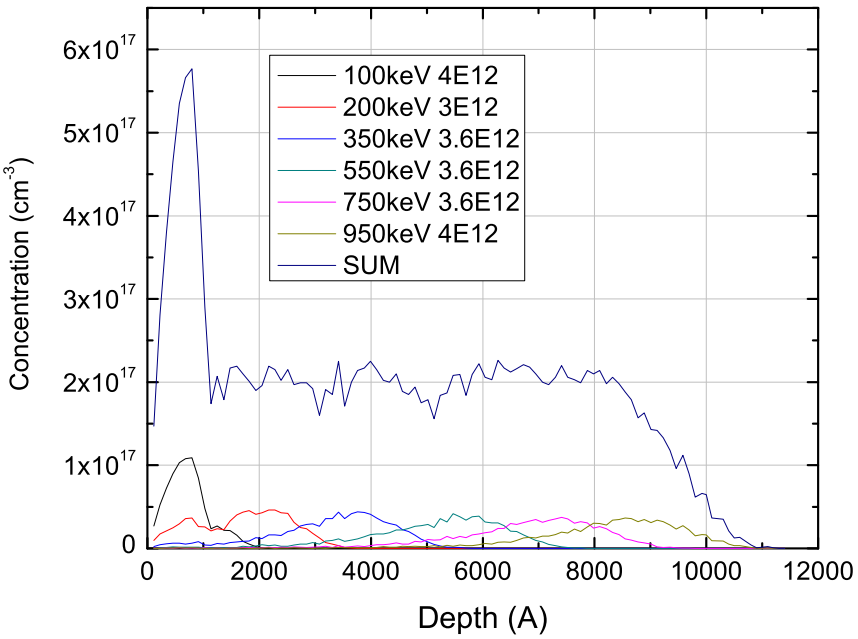


Fig. 5.12: Aluminum implantation profiles on carbon face 4H-SiC. SiC layer starts from 1200Å.

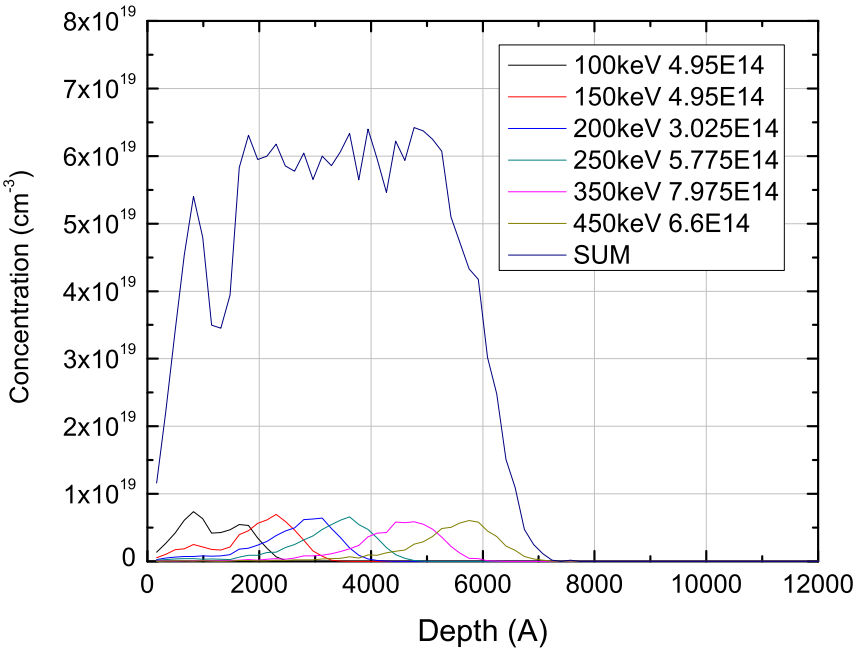


Fig. 5.13: Nitrogen implantation profiles on carbon face 4H-SiC. SiC layer starts from 1800Å.

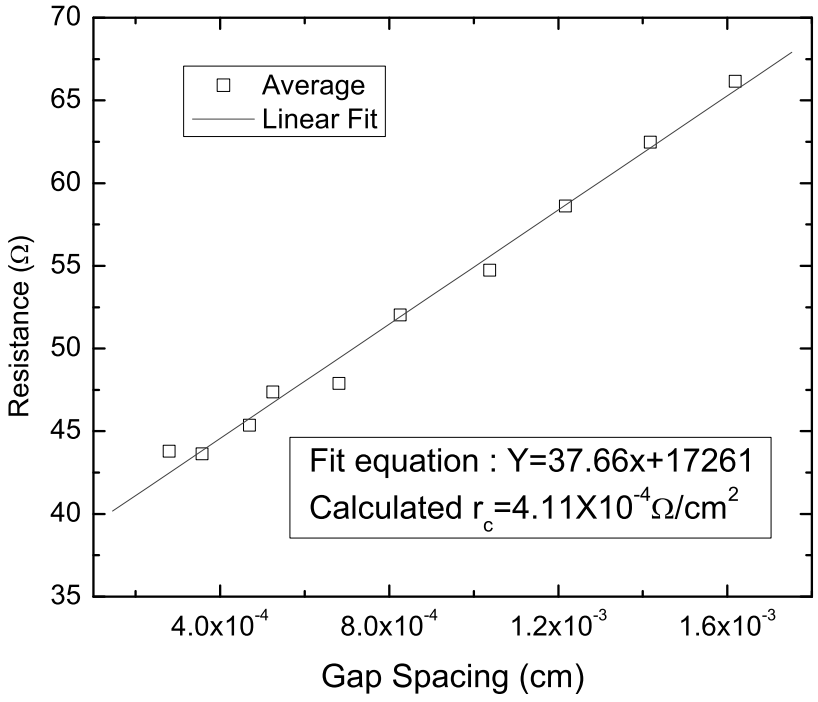


Fig. 5.14: TLM measurements results for doping concentration of 1E20cm$^{-3}$after Ohmic Contact Annealing at 850$^o$C for 4-minute.

### 5.5.2 Results and Analysis

Three-probe I-V measurements were used to study the source-drain current $I_d$ as gate voltage $V_g$ scans from off-state to on-state. The voltage between the source and the drain ($V_d$) was fixed to be 0.025v, which is smaller compared to $V_g$. The channel mobility can be simply estimated by using the surface-channel device formula.[105].

$$\mu = \frac{\partial I_d}{\partial V_g} \frac{L}{W} \frac{1}{C_{ox}} \tag{5.1}$$

Here, $\mu$ is the channel mobility, W is the channel width, L is the channel length, and $C_{ox}$ is the capacitance per unit area. $C_{ox}$ can be determined by $\epsilon_0 \epsilon_r A/d$, where $\epsilon_0$ is permittivity of free space, $\epsilon_r$ is relative dielectric constant of silicon dioxide, $A$ is unit area, and $d$ is the thickness of the oxide.

The channel mobility plots may be classified into two groups. Figure 5.15 shows the first group, in which the channel mobility increases slowly before arriving the highest point and maintains peak mobility for a wide range of fields without significant change. In this group, P-epi materials seem to have higher channel mobilities than P-implanted materials. Two possible reasons are: the doping concentration of the P-epi material is $5\times15\text{cm}^{-3}$, 1 order of magnitude lower than that of P-imp material, and the P-epi material should have better crystal quality than the P-implanted material since the damage produced by the implantation process may not be recovered completely by the activation process. However, with optimized oxidation techniques, the P-implanted MOSFETs have comparable channel mobilities to that of P-epi MOSFETs. As shown in figure 5.15, the wet re-oxidation plus NO passivation leads to the highest channel mobility, $40\text{cm}^2$/V-s, on P-implanted materials.

Since the interface quality of $SiC/SiO_2$ has been believed to be the main reason for the low channel mobility of SiC MOSFETs, the lower interface trap density is expected to result in the higher channel mobility. But the NO and $H_2$ post-oxidation passivation, giving the best interface quality, does not yield the highest channel mobility. This implies the MOSFET fabrication process is much more complicated and there must be existing other factors influencing the channel mobility. Although the $H_2$ passivation enhances the interface quality, it may simultaneously hurt the performance of other parts of MOSFETs, and the whole effect of the passivation may not benefit the channel mobility.

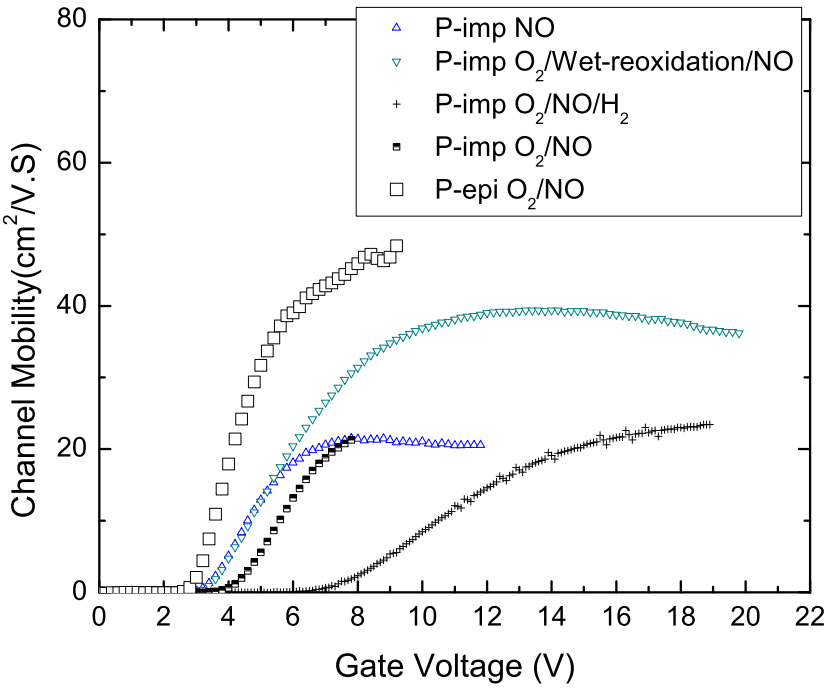


Fig. 5.15: The channel mobility of carbon face 4H-SiC.

The second group of channel mobilities behave much differently, as shown in figure 5.16. One obvious property is the threshold voltage is very close to zero, and low threshold

voltage will hurt the operating stability of MOSFET devices. When the devices are turned on, the channel mobility increases very quickly to a peak, usually much higher than the peak value of the first group, and then drops fast after the peak value depending on the field. This behavior has been observed only on P-epi materials. Common on both of these groups are the similar channel mobilities at high field. It should be noted that the similar results have been reported previously[98, 106].

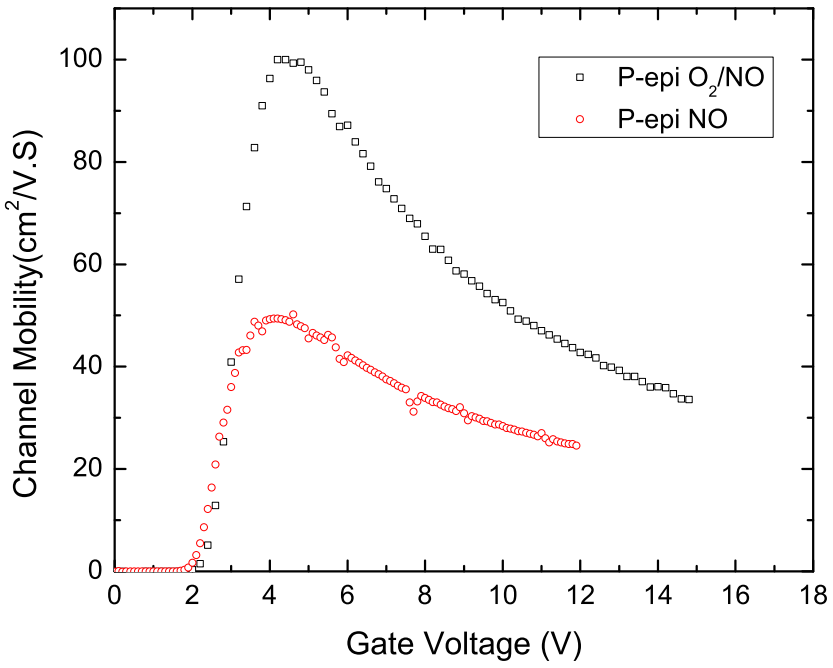


Fig. 5.16: The channel mobility of carbon face 4H-SiC.

For comparison, the channel mobility of (0001) 4H-SiC is shown in figure 5.17. It should be noted that all (0001) 4H-SiC are p-epi materials. The best channel mobility is obtained on MOSFETs treated by NO and $H_2$ post-oxidation passivation. At low field, $(000\bar{1})$ 4H-SiC yields higher channel mobility than (0001) 4H-SiC, but (0001) 4H-SiC shows

a slightly better performance on stability and value of the channel mobility at high field. This is probably because most carriers (electrons) in the channel have to move closer along the interface at high field and the better interface quality of (0001) 4H-SiC reduces the numbers of scattering and leads to a higher mobility. It should also be noted that the channel mobilities on $(000\bar{1})$ 4H-SiC show a wide range of values ($60\text{cm}^2/\text{V-s} \sim 120\text{cm}^2/\text{V-s}$). The large difference of the channel mobilities suggests the performance of the carbon face 4H-SiC MOSFETs is more sensitive to the fabrication process.

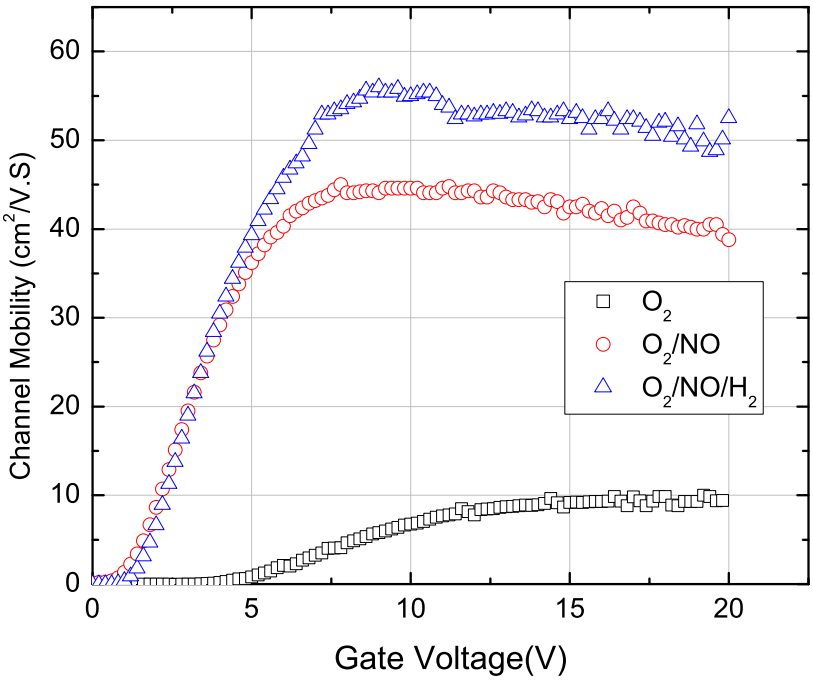


Fig. 5.17: The channel mobility of silicon face 4H-SiC.

The reason of the high channel mobilities on the carbon face 4H-SiC MOSFETs was also investigated. Gudjonsson *et.al*[106] have shown that mobile ions (mostly sodium) at

interface are able to apparently increase the channel mobility. In the MOSFETs' fabrication processes, sodium could be introduced into the devices. In order to verify the effect of the mobile ions, which also result in the shift of the threshold voltages of MOSFET devices, bias at temperature stressing (BTS) was used. When negative bias is applied on the gate at high temperature ($250^oC$), the mobile ions (carrying positive charges) will be attracted by the electric field in the oxide and move away from the $SiC/SiO_2$ interface to the $SiO_2$/metal interface. The devices were measured again after BTS and the results are shown in figure 5.18. The peak value of channel mobility drops from $65cm^2$/V-s to $35cm^2$/V-s, and the shape of the curve resembles that of the first group. This suggests that the mobile ions could be the reason for the high low-field channel mobilities. Meanwhile, since the introduction of the mobile ions depends strongly on the fabrication procedures, the amount of the mobile ions introduced at the interface varies. Therefore, the loose distribution of the mobility values can also be explained. If BTS is done on the first group of devices, the results can be seen in figure 5.19, showing that the oxide is "clean".

As shown above, to obtain a real channel mobility, the mobile ions need to be reduced as much as possible during the fabrication processes. The ohmic contact anneal is a very important step. BTS on MOS capacitors demonstrated sodium contaminations occurred during this step before employing low sodium quartz. It should be also noted that the nickel deposition step is critical for the reduction of the mobile ions. The pressure of sputtering system needs to be as low as possible before the deposition operation. This can reduce the possibility of sodium contamination in the nickel, as well as amount of oxygen, which may damage the ohmic contacts by forming nickel oxide during the ohmic contact annealing process.

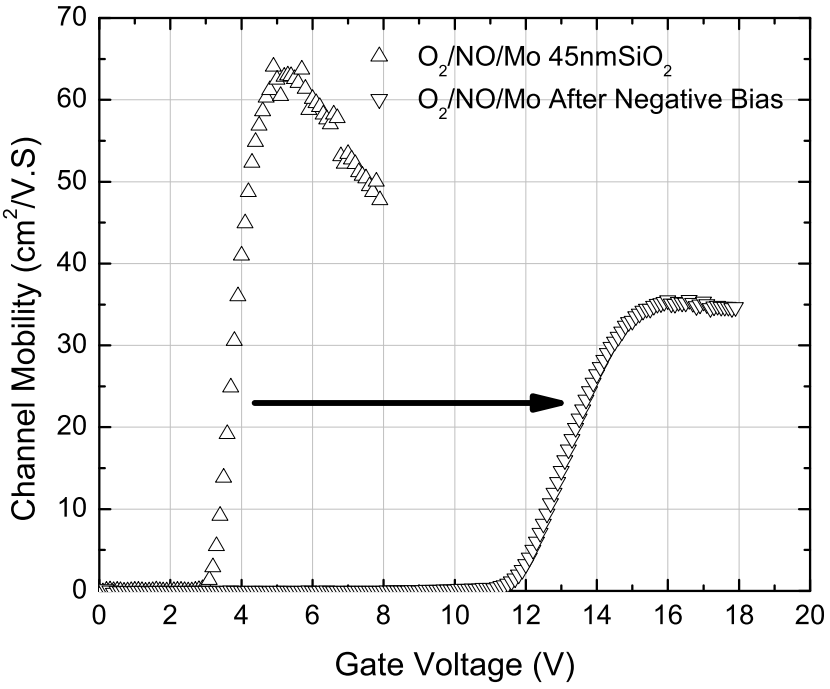


Fig. 5.18: The channel mobility of carbon face 4H-SiC after negative bias.

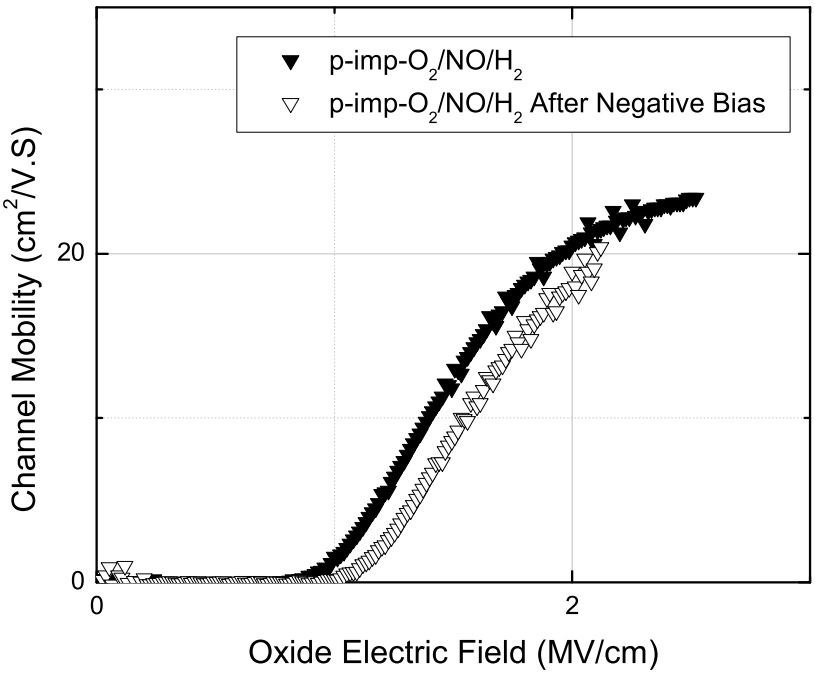


Fig. 5.19: The channel mobility of carbon face 4H-SiC after negative bias.

## 5.6 Conclusions

In this chapter, MOS capacitors and MOSFETs fabricated on the 4H carbon face SiC are investigated to provide a comprehensive view of the material. Both implanted and epitaxial layers are used to build MOSFETs. The oxide layer is grown thermally in furnace at 1150$^o$C, followed by post-oxidation annealing. High-purity Mo is sputtered as the gate metal, and silver paste is used as a broad area back contact for all measurements. The source and drain ohmic contacts of the lateral test MOSFETs are produced by sputtering Ni on heavily doped implanted regions ($6\times10^{19}$/cm$^3$), followed by an anneal at 950$^o$C for 4min. Hi-lo capacitance-voltage measurements at both 23$^o$C and 300$^o$C are used to obtain the interface trap density ($D_{it}$). Current-voltage measurements at room temperature are used to collect information about oxide leakage and breakdown field ($E_{bd}$). A three-probe I-V system is employed to determine $I_d$-$V_g$ characteristics of the MOSFETs at room temperature, and the inversion channel mobility ($\mu$) is extracted from these characteristics.

Results are compared for different post-oxidation interface passivation anneals. As shown in figure 5.7, the combination of NO and $H_2$ annealing gives the best $D_{it}$ ($\sim2\times10^{-11}$ cm$^{-2}$eV$^{-1}$ at $E_c$-E=0.2eV). Wet re-oxidation plus NO passivation produces the most reliable oxide, but the measured breakdown field of 6MV/cm is still approximately 2MV/cm lower than the average field measured for the Si-face. Compared with the value reported by Fukuda, *et al.*[98], the low field mobility value is not remarkable. However, the high field mobilities are similar. It was observed that the presence of mobile ions may increase the low field channel mobility. However, after negative bias stress at temperatures as high as 250$^o$C, the mobility peak value drops from 65cm$^2$/V-s to 35cm$^2$/V-s. These results suggest

that the effective mobility for carbon face may not be significantly higher compared to the Si face.

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# Appendix A

## Wafer Cleaning

All devices start with 4H-SiC wafers. The wafers were cut into small pieces in size of 5mm×5mm in our laboratory. To have better quality on the final devices, the cleaning process was executed prior to other steps. Usually, our cleaning process includes two parts: organic cleaning and RCA cleaning. The details of these two parts can be described as follows.

(1) Acetone cleaning for 5minutes in ultrasound;

(2) TCE cleaning for 5minutes in ultrasound;

(3) Acetone cleaning for 5minutes in ultrasound;

(4) Methanone cleaning for 5minutes in ultrasound;

(5) Methanone cleaning for 5minutes in ultrasound;

(6) Deionized water cleaning for 5minutes in ultrasound;

(7) BOE soak for 5minutes;

(8) Rinse in Deionized water for 5minutes;

(9) Soak in the solution ($H_2SO_4$:$H_2O_2$=1:1) for 15minutes;

(10) Rinse roughly in Deionized water;

(11) BOE soak for 1 minutes;

(12) Rinse roughly in Deionized water;

(13) Soak in the boiling solution ($H_2O$:$NH_4OH$:$H_2O_2$=3:1:1) for 15minutes;

(14) Rinse roughly in Deionized water;

(15) BOE soak for 1 minutes;

(16) Rinse roughly in Deionized water;

(17) Soak in the boiling solution ($H_2O$:HCl:$H_2O_2$=3:1:1) for 15minutes;

(18) Rinse roughly in Deionized water;

(19) BOE soak for 1 minutes;

(20) Rinse roughly in Deionized water;

(21) Dry with $N_2$.

Sometimes, small dusts can be observed on the surface of wafer before cleaning and could be removed by acetone. The microscope check after cleaning is necessary. The extra cleaning with step (17) through (21) might be performed again if needed.

# Appendix B

## Transmission Line Measurement

The transmission line measurement(TLM) is a convenient way to determine how well the ohmic contact annealing is done. It was originally proposed by Shockley[107]. To make TLM, a specific device must be fabricated, named by TLM device, which can be shown in figure B.1.In this device, there are several strips of pads. In one strip, each two neighboring

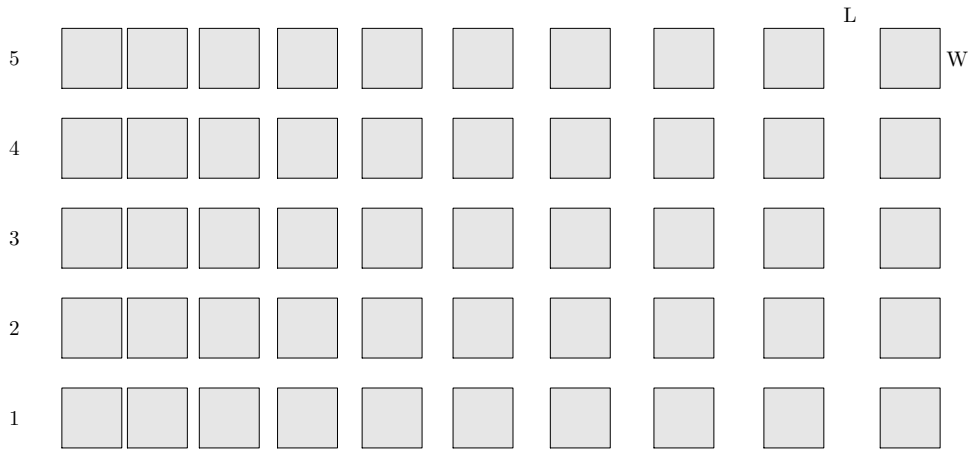


Fig. B.1: Schematic pattern of a transmission line measurement device.

pads are separated by varying distances($L$). The smallest value of $L$ is around 2$\mu$m and the largest one is around 16$\mu$m. The resistance between each two pads in one strip can be determined by using 4-probe I-V measurement, as shown in figure B.2. A constant current($I$) flows through two probes and the corresponding voltage($V$) is measured by the other two. The two probes contacting with the same pad don't have to be close, if

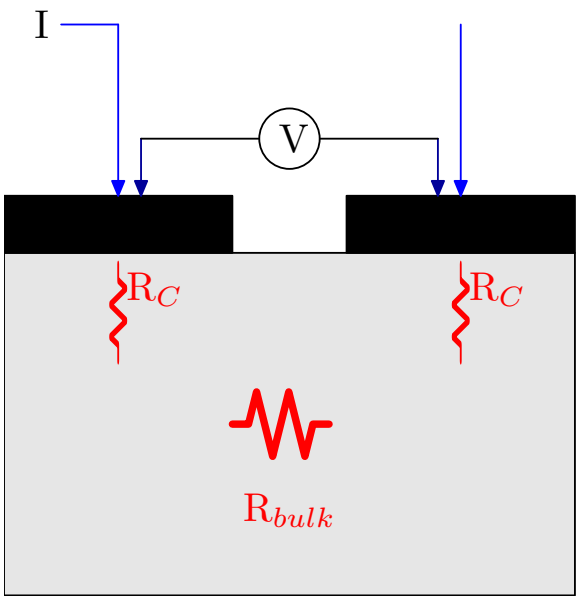


Fig. B.2: Diagram of a 4-probe I-V measurement in TLM.

the condition that each pad is at equal potential is satisfied. Deposition of gold on the pads is generally used to meet this condition. The resistance calculated from Ohm's law, $R = V/I$, consists of contact resistances of two pads and bulk resistance between these two, $R = 2R_C + R_S$. $R_S = R_{sh}L/W$, where $R_{sh}$ is the sheet resistance, $L$ is the distance between two pads, and $W$ is the width of each pad. In this equation, It has been assumed that the contact resistances for all pads are equal. After knowing all resistances and distances between every two pads, a plot of resistance v.s. distance can be made, as shown in figure B.3.

In figure B.3, the slope of the line is

$$Slope = R_{sh}/W. \tag{B.1}$$

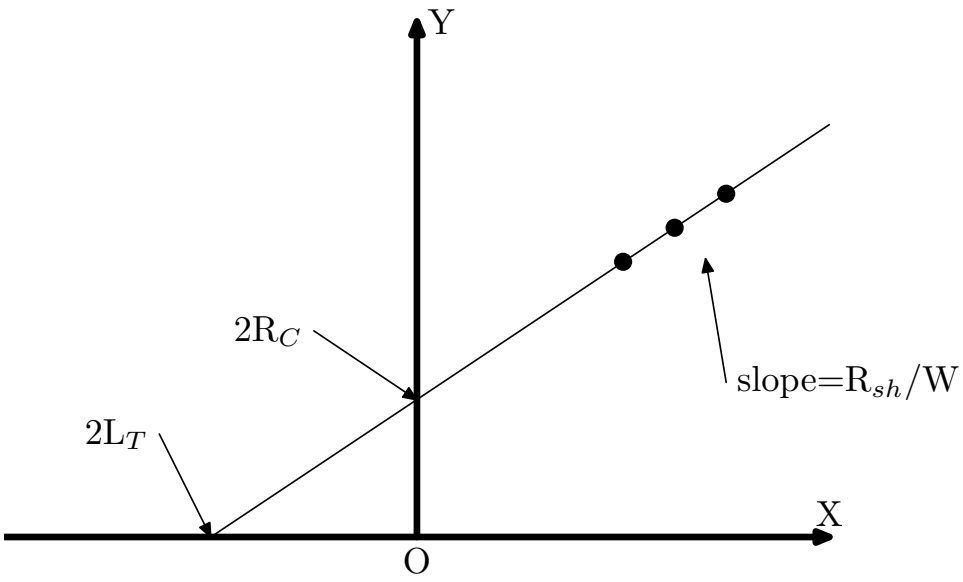


Fig. B.3: Plot of total contact to contact resistance as a function of $L$ to obtain transfer length and contact resistance values.

The $y$-axis intercept is $2R_C$, and $x$-axis intercept(the transfer length($2L_T$)) is $2R_CW/R_{sh}$. Because specific contact resistance($r_c$) is defined as $r_c = R_{sh}L_T^2$,

$$r_c = \frac{R_C^2 W^2}{R_{sh}}. \tag{B.2}$$

In practical measurements, $R_C$ and $R_{sh}$ can be determined from the fitting linear equation of TLM plot. To get more accurate parameters, the distances between two pads must be measured individually, because although the same mask is used to fabricate the TLM devices, such errors as misalignments and overdevelopment still can affect the gaps between pads.

# Appendix C

## Metal and Metal Film Etchants

Table C.1:

| Metal | Composition (volume Ratio) | Comments |
|---|---|---|
| Ag | $NH_4OH:H_2O_2$=1:1 | |
| Al | (1) $HNO_3:CH_3COOH:H_3PO_4:H_2O$=5:5:85:5 at 40-45$^oC$ | Rinse in deionized water followed by $HCl:H_2O$=1:3 to remove phosphorus. |
| | (2) $NaOH:H_2O$=1:5 | |
| | (3) Hot $H_3PO_4$ Photoresist safe | Not recommended for production use when Na contamination is of concern. |
| Au | $HNO_3$:HCl=3:1 | 1000-1200Å/S |
| Bi | $HCl:H_2O$=1:10 | |

| Metal | Composition (volume Ratio) | Comments |
|---|---|---|
| Co | (1) $HNO_3$:$H_2SO_4$:$CH_3COOH$:$H_3PO_4$=3:1:5:1 | |
| | (2) $HNO_3$:$H_2O$=1:1 | |
| | (3) HCl:$H_2O_2$=3:1 | |
| Cr | (1) HCl:$H_2O$=3:1 | |
| | (2) HCl:glycerin=1:1 | |
| | (3) $KMnO_4$:NaOH:$H_2O$=8:4:100 by weight | |
| Cu | (1) $HNO_3H_2O$=5:1 | |
| | (2) $(NH_4)_2S_2O_8$ | |
| | (3) $CH_2O_2$:$H_2O_2$:$H_2O$=6:1:3 | |
| Fe | HCl:$H_2O$=1:1 | |
| Hf | HF:$H_2O_2$:$H_2O$=1:1:20 | |
| In | $HNO_3$:HCl=1:3 at $40^oC$ | |
| Ir | $HNO_3$:HCl=1:3 at $40^oC$ | |
| Mg | NaOH:$H_2O$=1:1 by weight followed by | |
| | $CrO_3$:$H_2O$=1:5 by weight | |

| Metal | Composition (volume Ratio) | Comments |
|---|---|---|
| Mo | (1) $H_3PO_3$:$CH_3COOH$:$HNO_3$:$H_2O$=85:5:1:5 | at $40^oC$. |
| | followed by HCl:$H_2O$=1:3 | A slow etch for patterning use. |
| | (2) $H_2SO_4$:$HNO_3$=1:4 (dry) | A fast etch for non patterning. |
| | (3) $H_2SO_4$:$HNO_3$:$H_2O$=1:1:2 | |
| Nb | $HNO_3$:HF=1:1 | |
| Ni | (1) $FeCl_3$ 40% | |
| | (2) $HNO_3$:HCl=1:5 | |
| | (3) $CH_3COOH$:$HNO_3$:HCl=150:50:3 at $70^oC$ | |
| NiCr | (1)$HNO_3$:HCl:$H_2O$=1:1:3 | |
| | (2)$FeCl_3$:HCl(37%)=3:20 on Ta thin film cir- | |
| | cuits | |
| Pb | $CH_3COOH$:$H_2O_2$:$H_2O$=4:4:10 | |
| Pd | $HNO_3$:HCl:$H_2O$=1:3:4 | |
| Pt | (1) $HNO_3$:HCl:$H_2O$=1:3:4 | At $95^oC$ |
| | (2) $HNO_3$:HCl=1:8 | Age 1 hour etch at $70^oC$ |
| Rh | HBr (62%) | At $100^oC$ |

| Metal | Composition (volume Ratio) | Comments |
|---|---|---|
| Ru | Anode in HCl or $H_2SO_4$ (A.C.) | |
| Sb | $HNO_3$:HCl:$H_2O$=1:1:1 | |
| Sn | (1) HCl:$H_2O$=1:4 | |
| | (2) HF:HCl=1:1 | |
| Ta | $HNO_3$:HF:$H_2O$=4:4:10 | |
| $TaSi_2$ | $HNO_3$:BHF(7:1 dilution)=4:6 | |
| Ti | (1) $H_2SO_4$:$H_2O$=1:1 | At 115-120$^o$C in ultrasonic |
| | (2) HF:$H_2SO_4$:$H_2O$=1:30:69 | At 65$^o$C |
| | (3) $H_2O_2$:EDTA=1:2 | At 70$^o$C |
| V | $HNO_3$:HF:$H_2O$=1:1:1 | |
| W | (1) $KH_2PO_4$:KOH:$K_3Fe(CN)_6$=0.25:0.24:0.1 | |
| | (2) $HNO_3$:HF=1:1 | |
| | (3) $H_2O_2$:EDTA=1:2 | |
| Zr | $HNO_3$:HF:$H_2O$=1:1:50 | |
| Polysilicon | $HNO_3$:$H_2O$:HF=50:20:1 | At 25$^o$C |