EXPLICIT FINITE ELEMENT MODELING IN CONJUNCTION WITH DIGITAL IMAGE CORRELATION BASED LIFE PREDICTION OF LEAD-FREE ELECTRONICS UNDER SHOCK–IMPACT

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EXPLICIT FINITE ELEMENT MODELING IN CONJUNCTION WITH DIGITAL IMAGE CORRELATION BASED LIFE PREDICTION OF LEAD-FREE ELECTRONICS UNDER SHOCK-IMPACT

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THESIS ABSTRACT

EXPLICIT FINITE ELEMENT MODELING IN CONJUNCTION WITH DIGITAL IMAGE CORRELATION BASED LIFE PREDICTION OF LEAD-FREE ELECTRONICS UNDER SHOCK-IMPACT

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Increasing demand for smaller consumer electronics with multi-function capabilities has driven the packaging architectures trends for the finer-pitch interconnects thus increasing chances of failure of the electronic packages under shock and vibration environment. In this work, digital image correlation (DIC) in conjunction with ultra high speed cameras for full-field measurement of transient strain has been investigated. DIC data has been used as input for the finite element models for development of transient strain histories in second-level interconnects. Test boards according to JEDEC standard subjected to shock and vibration at zero horizontal drop orientation were examined. The effect of sequential stresses of thermal aging and shock–impact on the failure mechanism

has also been investigated. The thermal aging condition used for the study includes 125°C for 100hrs. Solder alloy system studied include Sn1Ag0.5Cu, Sn3Ag0.5Cu and 96.5Sn3.5Ag. Explicit finite element modeling approaches for second-level package in drop and shock of electronic assemblies have been developed without any assumptions of geometric or loading symmetry. Approaches examined include smeared property with conventional-shell global model, Timoshenko-beam element with continuum shell element global model, node-based explicit sub-model and cohesive zone failure model. Model predictions have been correlated with experimental data. Relative damage-index based on the lead-free interconnect transient strain history and component's survivability envelope has been developed for life prediction of lead free electronics alloy systems. Damage index based survivability envelope is intended for component integration to ensure reliability in extremely harsh environments.

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CHAPTER 1

INTRODUCTION

1.1 Electronic Packaging and its Evolution

Electronic Packaging is the art (based on science) of establishing interconnection between various levels of electronic devices, component, modules and systems. Packaging of electronics refers to the placement and connections of many electronic and electromechanical components in an enclosure which protects the system from environment and provides easy access for routine maintenance. Packaged electronics is the embodiment of all electronic equipments (example: calculator, computers, etc.) and they typically consists of active components (Examples: Integrated Circuit (IC) chips, etc.). In a study of packaging of electronics, many of the components can be heavy and/ or bulky, such as power-supply transformer, cathode-ray-display tubes etc. In this thesis, term electronic packaging is referred to as Packaging of Microelectronics (i.e. Semiconductor chips). Functions of electronic packaging include signal distribution, power distribution, heat dissipation and protection (mechanical, chemical and electromagnetic). Figure 1.1 shows hierarchy of electronic packaging. The packaging process starts with chip which has been diced from a wafer of silicon that was fabricated using photolithographic semiconductor fabrication process. The chip comprises of electronic devices (example: transistors, resistors, etc.) that are interconnected in a

planned manner to form IC that perform a desired electrical function. After testing, the chip is housed in a chip carrier and small wires or solder balls are used to electrically connect the chip to the carrier. The chip carrier or component is called first level of packaging and electrical connection to the chip carrier or component is often referred to as first level interconnects. Next, several chip carriers are placed on the circuit board or substrate called second level packaging and connected together with wiring traces know as second level interconnects which have been formed by photo-etching the circuit board. The edge connectors on the circuit board are then inserted into contacts on a back panel called third level of packaging which carries higher level connections that permit communication from one circuit board to the next.

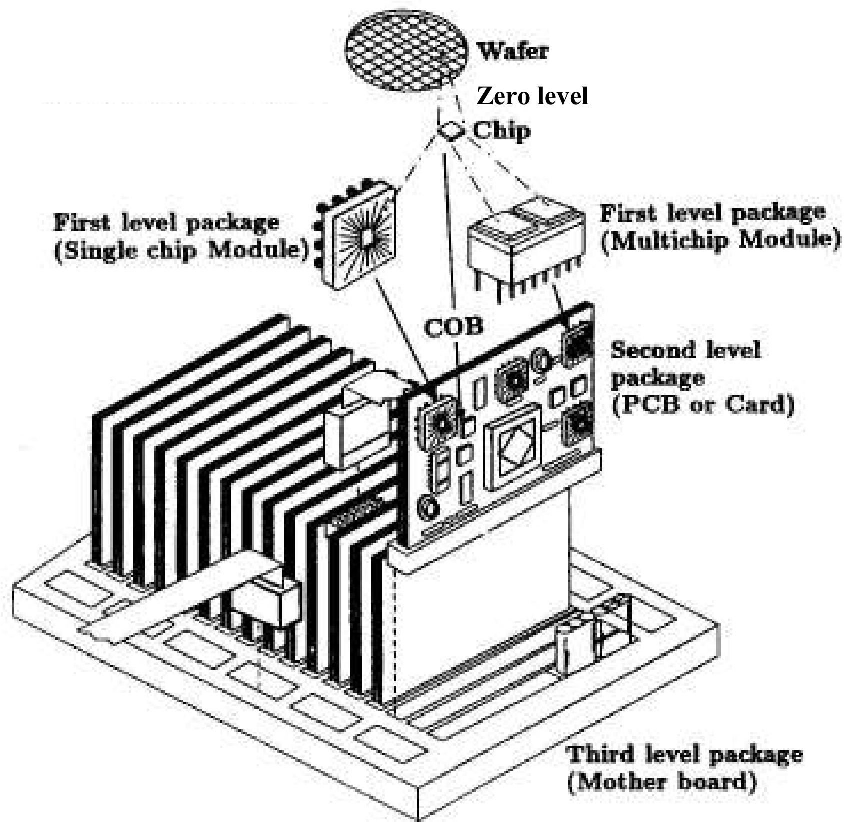


Figure 1.1: Hierarchy of Electronic Packaging [Mech6310 Course Notes]

The current trend in the manufacturing conventional electronic assemblies has essentially reached its limit as far as weight, volume, reliability and cost is concerned. Surface mount technology (SMT) where components are mounted directly on to surface of printed circuit boards has largely replaced the through-hole technology. SMT results in more reliable assemblies at reduced weight, volume and cost. Every component on typical printed circuit board was through-hole component until surface-mount technology became popular in the late 1980s. Though through-hole mounting provides strong mechanical bonds when compared to SMT techniques, SMT is more preferred over through-hole mounting because of various advantages such as smaller component size, much higher number of components and many more connections per component, fewer holes need to be drilled through abrasive boards, simpler automated assembly etc. Figure 1.2 shows evolution of electronic packages for the past three decades.

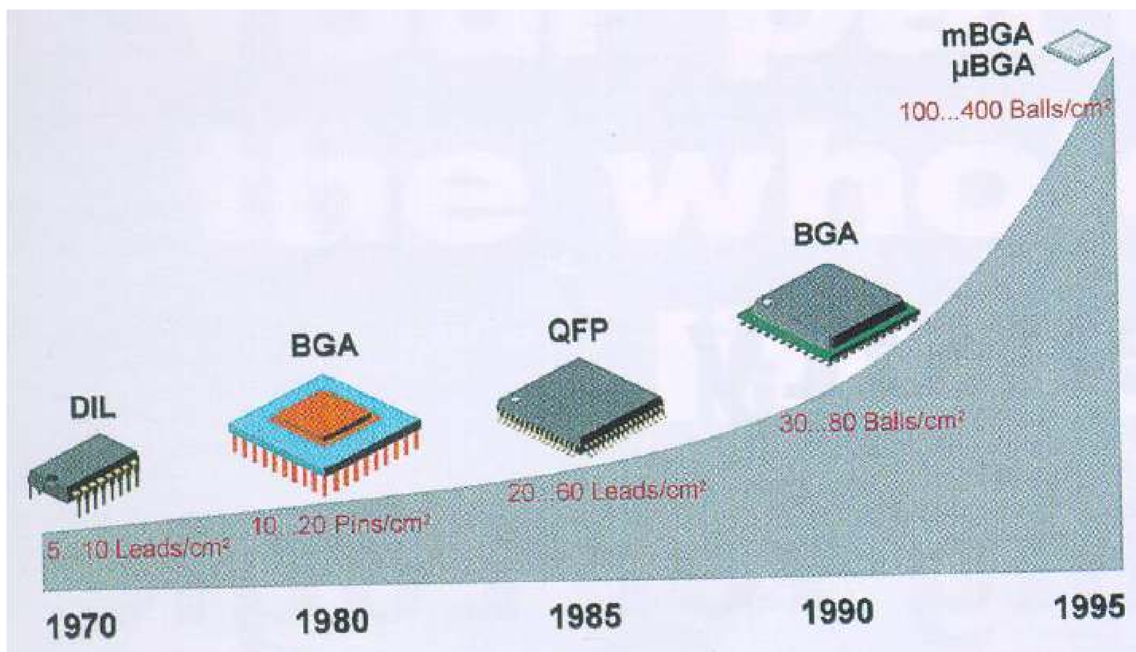


Figure 1.2: Evolution of electronic packages for the past three decades [ME6310 Course Notes]

The current trends in electronic packaging lead to many mechanical challenges, packaging material can be exposed to high temperature changes due to operation of high power density devices or extreme ambient environments. Thermally induced stresses often occur due large mismatches in the co-efficient of thermal expansion of various materials in the package. Stresses also occur due to mechanical loading such as shock and vibration. Experimental measurements are difficult due to the small size of the structure and material interest

1.2 Lead-free Technology

Lead (Pb) usage had been widely implemented in the electronic industry (utilized in a variety of application for more than five decades), most notably the use of eutectic tin-lead (Sn-Pb) solder to attach discrete components to printed circuit board (PCB) and also these attachment mainly serves as the electrical interconnections between the attached component and PCB. However, due too rise in the awareness of the potential health hazards associated with the toxicity of lead in human and environment, actions have been taken by electronic industry to come up with regulation on its usage. Europe, Japan, US (not all states) have implemented the regulations suggested by Restriction of Hazard Substances (RoHS) and Waste from Electrical and Electronic Equipment (WEE) directive. As a result of this, eutectic tin-lead solder joint has been replaced with lead-free SAC alloys. Due to this change in technology we now have to face new challenges (Figure 1.3).

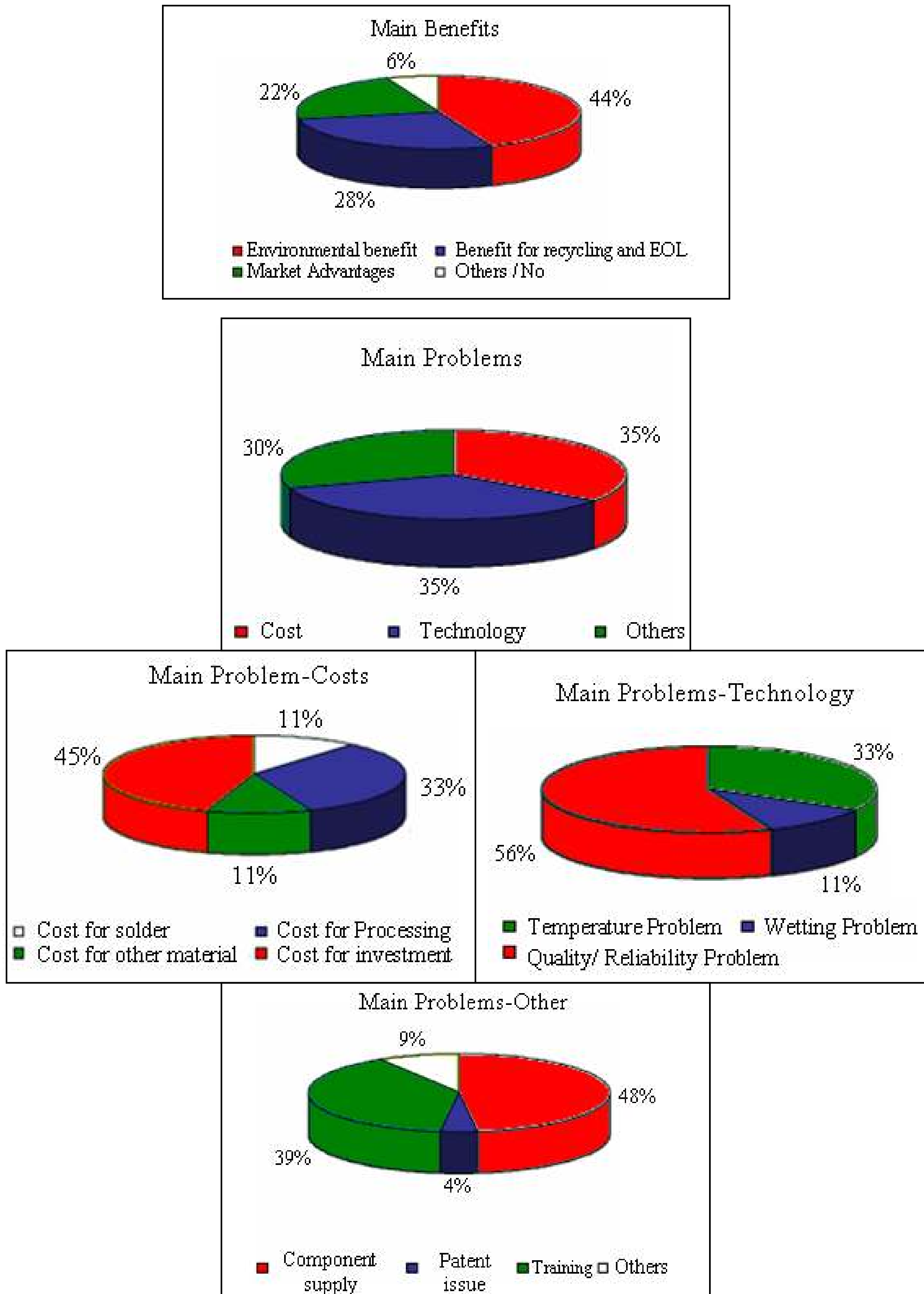


Figure 1.3: Statistics of Lead-free Technology in Electronic packaging

1.3 Shock and Vibration in Electronic Systems

Electronic product may be subjected to shock and/or vibration during manufacturing, shipping, operational periods. During manufacturing, products may be subjected to a combination of thermal aging, thermal cycling and random vibration as a screening environment to eliminate flaws. During shipping the products in a container from plant through the distribution chain to the customer, products may be loaded and off-loaded on multiple occasions, subjecting product to shock, and vibration in conjunction with thermal stresses. Operational life may involve shock, vibration (an example is accidental drop of the product during normal usage). Also trends towards miniaturized fine pitch electronics, have increased the susceptibility of failure in shock, vibration and high strain rate stresses. Fundamental understanding regarding the failure mechanism equipped with analytical, experimental and predictive techniques is necessary to enable product reliability over the design life.

Mechanical systems such as printed circuit board assemblies respond to a dynamic disturbance imposed either by forces or displacement by shock and vibration. The shock and vibratory response is often complex with several different time dependent motions occurring simultaneously. In some cases, the dynamic parameters of complex system can be developed using lumped mass analysis for computational efficiency. In these situations, mechanical systems can be treated as single degree of freedom system without introducing significant error. Shock and vibrations are usually considered together because the system for both are modeled with spring and dashpot supported mass as shown in Figure 1.4. In case of vibration, steady state periodic input such as sinusoid is considered. In shock, transient input which results in the application of velocity (usually

time dependent) to the structure is considered. Shock is defined as a transient condition where a single impulse of energy is transferred to a system in a short period of time (milliseconds) with large acceleration.

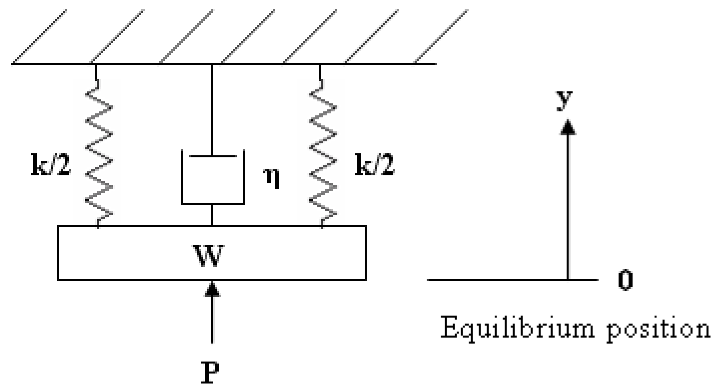


Figure 1.4: Spring-mass assembly representing a single degree system with damping.

1.4 Thermo-Mechanical Deformation in Electronic Systems

Apart from shock and vibration in electronics, one of the most important problems in the design of electronic systems is the generation of strain in the solder interconnects joints by the change in temperature which occur in shipping, storage and operation. The chip carriers are soldered to printed circuit boards to mount them mechanically and connect them electrically. But there is often a larger mismatch in the effective coefficient of thermal expansion between the chip carrier and the printed circuit board. The coefficient of thermal expansion of the PCB is higher than that of the chip carrier

($\alpha_{PCB} > \alpha_{CC}$). As a consequence, temperature changes ΔT produce differential expansion 'd' (contraction) resulting in shearing strain γ in the solder joints.

1.5 Digital Image Correlation

Digital image correlation (DIC) is a state-of-the-art non contact optical technique for measuring full field quantities and their derivatives. DIC technique is less demanding optically-ordinary incoherent light is sufficient, vibration isolation table is not required, and the optical components such as beam splitter, prism, spatial filter, piezoelectric actuators, etc. are eliminated. DIC technique supercedes other experimental techniques such as holographic interferometry, Moiré Interferomerty because other techniques often consumes more time and involve expensive grates etc. In this thesis, DIC technique is used to obtain full field strain, displacement, velocity contours of PCB subjected to an impact test to get reliable results.

1.6 Modeling Shock with Finite Elements

Modeling shock response of an electronic product is very challenging task due to the scale difference between the dimension of the individual layers, such as solder interconnects, copper pad, chip-interconnects, and the dimensions of the electronic assembly. These scale difference makes the computational effort required to attain fine mesh necessary to model solder joints while capturing the system-level dynamic behavior very difficult. In this work, explicit time-integration scheme is implemented which is suitable for solving wave propagation equation necessary to model drop impact event.

1.7 Current Issues with Solder Interconnects

Solder alloy deformation under high strain rates has been previously incorporated in simulation frameworks using linear-elastic models and elastic-plastic models for interconnects. However, solder has been shown to undergo micro-structural evolution and change in stress-strain behavior when exposed to thermal loads. Modeling interconnect deformation behavior under high strain rates in the presence of overlapping thermal loads is presently beyond the state of art. Primary impediments include scale differences in the packaging architectures from the assemblies to interconnects, lack of insight into the modeling high-strain rate deformation characteristics, and their evolution in presence of thermal loads and competing failure interfaces progressing towards failure simultaneously. Traditionally, an experimental iterative product development approach has been used. Unconventional accelerated design techniques are required to find acceptable solutions beyond today's packages and ICs to address many new materials which will be introduced in IC packages in next few years in order to meet requirements of environmental regulations. Present lack of predictive and optimization tools for interconnect/packaging architecture design makes total optimization of interconnect system difficult.

1.8 Thesis Organization

The thesis will involve the measurement of material deformation at high strain rates using optical techniques in conjunction with high-speed imaging, and development of material models into explicit finite element for prediction of transient dynamics and interconnect-deformation under overlapping stresses. Packaging architectures targeted

will include area-array architectures, with lead-free solder interconnect. The proposed thesis will enable: (a) models for lead-free interconnect deformation at high strain rates under overlapping stresses, (b) computational framework for prediction of transient dynamics of electronic assemblies (c) effect of sequential stresses on deformation behavior. Several lead-free solder alloys will be investigated including the SnAgCu formulations. Optical measurement techniques including digital image correlation will be used to measure the speckle displacements in three dimensions with multiple high speed cameras working at 50,000 frames/sec. Displacement gradients will be used to calculate gradients and strains. Strain data will be used to develop a unified model incorporating the thermal and high-strain rate transient mechanical stresses. Computational techniques enabling the simultaneous assessment and prediction of transient dynamics and interconnect deformation will be investigated. Finite element techniques investigated will include, explicit global modeling and explicit sub-modeling techniques. Explicit finite element method allow for prediction of transient dynamics without any assumption regarding of symmetry of geometry, boundary conditions, or loading. Capability for deformation behavior in the computational framework will be coupled with the damage relationships developed based on damage proxies. The results from coupling will enable the life prediction under high strain events, overlapping stresses (thermal ageing and drop impact) and cumulative damage accumulation.

CHAPTER 2

LITERATURE REVIEW

The handheld electronic products such as cell phones, cameras, calculators etc are subjected to shock and drop during their actual service life because of their lesser weight and smaller dimension. As a result, interconnect fails due to bending of PCB and mechanical shocks which are the most common failure modes seen in shock and vibration environment.

2.1 Shock and Vibration Testing for Electronics

Board and Package Level Testing

JEDEC drop test is one of the most common experimental methods used to address shock and vibration reliability, which involves subjecting the board to a 1500g pulse for 0.5 milliseconds half-sine pulse in 0° horizontal drop orientation. Figure 2.1 shows typical drop test apparatus and mounting scheme for PCB assembly. JEDEC drop test is considered as a common ground for an assortment of semiconductor component manufacturers to compare the solder joint reliability under impact. This standard has been widely accepted and used by researchers to compare their reliability results. However, the JEDEC standard has some limitations. One of the limitations is that it has too many loading conditions, which may be unnecessary, and results in reduced sample sizes of

each loading condition for statistical analyses. To overcome this drawback, Zhao et. al [Zhao 2007] proposed an alternative board design with only one loading condition and a sufficiently large sample size, while Tsai et. al. [Tsai 2007] demonstrated applications of the response spectra to a JEDEC standard drop test board subjected to different JEDEC drop test conditions.

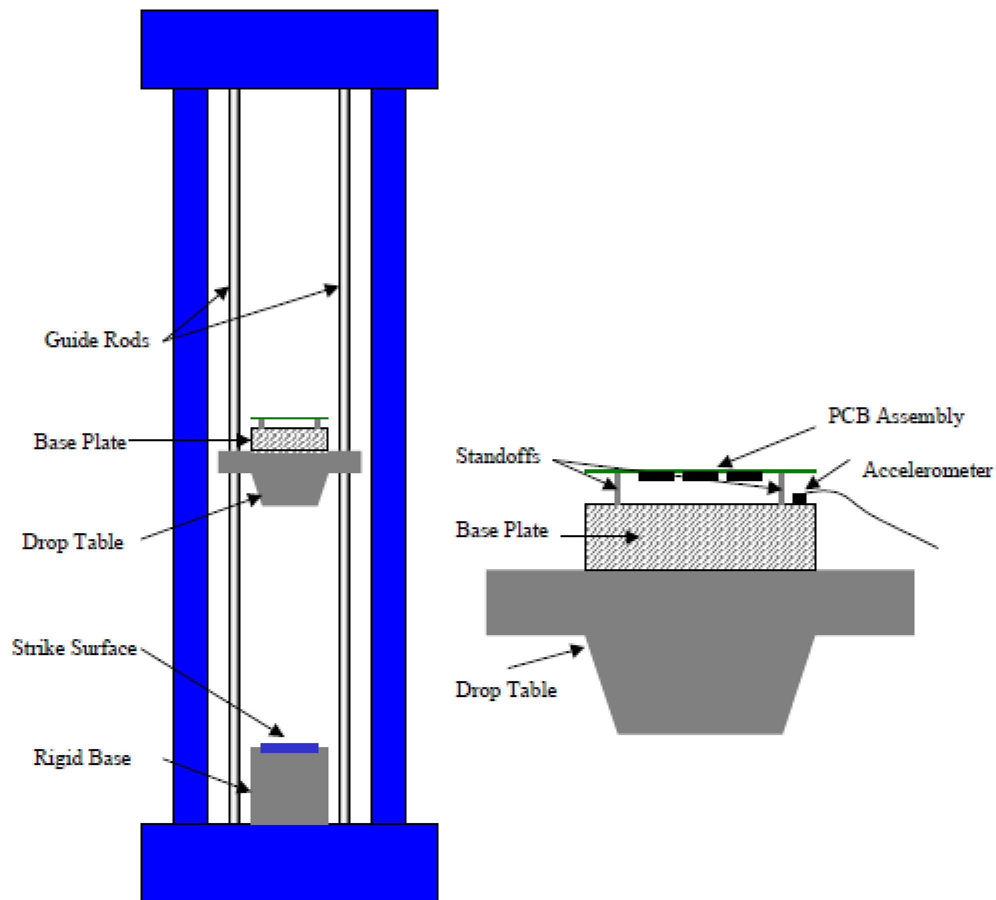


Figure 2.1: Typical drop test apparatus and mounting scheme for PCB assembly (Source: Board Level Drop Test Method of Components for Handheld Electronic Products JESD22-B111)

In spite of its drawbacks, JEDEC is the most frequently used drop test standard. The JEDEC standard specifies that the test vehicle should be mounted with the package side

facing downwards to create a more critical loading condition [Yeh 2004]. It also states that the drop orientation should be horizontal or at zero degrees during the drop test. But this is not the only angle at which a product might hit the floor. Experiments conducted on cell phones by Liu et. al. [Liu 2005], Seah et. al. [Seah 2002], Ong et. al. [Ong 2003] and Lall et. al. [Lall 2006] have shown that impact reliability is very sensitive to the impact angle of the product. Chong et. al. [Chong 2005] reported that pin-supported vertical drop of PCB generated much lower PCB flexing and impact stress damage to the solder joints compared to the horizontal orientation drop.

2.2 Effect of Thermal Aging in Electronics

It is necessary to conduct combination of impact test, thermal cycling, and thermal ageing tests for electronics products such as cellular phone before it reaches the market to ensure its reliability for long term. [Yang 1994] conducted drop test and shear tests of ball-grid-arrays with SnAg-Cu solder balls on Cu pads after thermal aging at different temperature and for durations. [Chiu 2004] carried out effect of thermal ageing on board level drop reliability for Pb-free BGA packages Thermal ageing at homologous temperature between 0.76 and 0.91 with microstructural analysis was conducted by Chiu to analyze the solid phase IMC growth at the solder to BGA pad interface. Kirkendall voids were observed at the Cu to Cu3Sn interface. Voids occupied 25% of pad/solder interface after only 3 days of 125°C ageing, and the void density increased with the ageing time and temperature. The drop performance degraded 80% from time 0 to 10 days at 125°C. [Ahat 2001] reported a study of interface microstructure and shear strength of 96.5Sn3.5Ag and 62Sn36Pb2Agon Cu after aging at 2500C for 0, 50, 250,

500, and 1000 hrs. The shear strength of both the Sn-Ag and Sn-Pb-Ag decreased with aging time, and the fracture mode changed from mixture of solder and IMC at zero aging time, to a complete fracture of the IMC layer after 1000 hrs aging. [Mei 2005] carried out a study that focused on two issues: the conditions for void formation and the effect of voids on solder joint reliability. Drop tests showed aged BGAs did not fail at the voided interface; rather the failures occurred inside the solder joint or PCB laminate. The shock strength at 400 G of BGA packages aged for 20 days at 125°C did not degrade. [Ma 2006] reported the reliability of aging lead free solder joint. [Zhang 2008] showed the effects of aging on mechanical behavior of lead free solders by performing creep tests on four different SAC alloys (SAC105, SAC205, SAC305, SAC405) that were aged for various durations (0-4 months) at room temperature (25 °C), and several elevated temperatures (75, 100, and 125 °C). Analogous tests were performed with 63Sn-37Pb eutectic solder samples for comparison purposes. The results demonstrated the significant effects of elevated temperature exposure on the creep behavior of solder joints. In addition, the effects of aging were shown to be significant even for aging temperature slightly above room temperature (e.g. T = 75°C). The recorded data demonstrate that the creep behaviors of lead free and tin-lead solders experience a “cross-over point” where the lead free solders begin to creep at higher rates than standard 63Sn-37Pb solder for the same stress level. These cross-over points were observed to exist for all four of the SAC solder alloys, and for all of the aging temperatures except for room temperature.

2.3 Effect of Lead-Free Solder Interconnects

In the recent past, lead free based solder alloys-system are being used as solder interconnects in electronic packages. It is important to determine the life of these lead free alloy-systems in order to consider them as the replacement for the lead based solder alloys. In order to evaluate the reliability of lead free interconnects they have been subjected to various mechanical tests such as drop and shock, thermal ageing, thermal cycling. Previously, many researchers have studied the variation of solder alloy composition. Low silver content SAC alloys are resistant to high strain rate under drop shock and improves drop reliability [Zhu 2008, Che 2008, Lall 2008a, Pandher 2008, 2007, Kim 2007]. Increase in the creep rate by lowering silver content of SAC alloys [Zhang 2008]. Improving drop reliability by adding Ni in SnAgCu alloys [Song 2008, Huang 2007]. Improvement in the drop performance of Sn-Ag-Cu BGA on Ni/Cu/Au surface finishes [Kawashiro 2008]. Solder joint reliability enhances with UBM/penetration layer/SnAg lead free solder bump structure [Choi 2007]. SnAgCu and SnPb on OSP have similar fracture energy at lower shear speed as shear speed increases beyond 100mm/sec fracture energy of SnAgCu drops to zero [Sweatman 2008].

2.4 Digital Image Correlation

Digital Image Correlation (DIC) is a technique based upon tracking a geometric point before and after deformation that enables full field displacement and their derivatives measurement during a transient event such as shock and impact. Tracking points on the test vehicle is done by speckle coating the surface of the structure which is of interest. Studies reveal that size, consistency and density of the speckle pattern affect the accuracy

of the method [Zhou 2001, Amodio 2003, Srinivasan 2005]. This method is extremely favorable in comparison to the use of strain gage which measure strain only at discrete locations on the test structure. It is also advantageous over interferometry as this technique is non-contact and has reduced sample preparation time and lower costs. The DIC technique was used in the electronics industry for various applications. Investigating stresses in solder interconnects of BGA packages under thermal loading [Zhou 2001, Yogel 2001, Rajendra 2002, Zhang 2004, Zhang 2005, Xu 2006, Bieler 2006, Sun 2006], stresses and strain in flip-chip die under thermal loading [Kehoe 2006], and monitoring crack propagation and calculating Young's modulus of the underfill at elevated temperatures during four-point bending tests [Park 2007[a], Shi 2007] are some of the areas for which this technique has proven to be valuable. Deformation measurement in micro-system structure subjected to milling [Vogel 2007], In addition, DIC technique was used in the study of behavior of materials like polyurethane foams. [Jin 2007], polymer films [Park 2007[b]] and coating materials [Thompson 2007]. It was also used for material characterization at high strain rates [Tiwari 2005]. Although this technique has become popular in the thermal area of electronic packaging, it is fairly new in the field of drop and shock. DIC has been used to measure full field displacement and deformation gradient in electronic assemblies subjected to drop and shock [Lall 2007b, 2008a,b,Miller 2007, Park 2007a,b, 2008], [Scheijgrond 2005]examination of velocity, rotation, bending on portable products subjected to impact test. Damping ratio on the surface of the board [Peterson 2008].

2.5 Finite Element Analysis (FEA)

During Impact test, it is difficult to measure displacement and their derivatives across board-joint interface using strain gage and other experimental techniques. In the past, many researchers have tried to predict the transient dynamic behavior of board and product levels using various simulations. Prediction of transient dynamics has been investigated using equivalent layer models [Gu 2005], smeared property models [Lall 2004, 2005], Conventional shell with Timoshenko-beam Element Model and the Continuum Shell with Timoshenko-Beam Element Model [Lall 2006a,b, 2007a-e, 2008a-d], implicit global models [Irving 2004, Pitaressi 2004], and global-local sub-models [Tee 2003, Wong 2003, Zhu 2001, 2003, 2004]. Implicit transient analysis with Input-G Method [Luan 2004]. [Yeh 2004] used an implicit solver by translating the input acceleration pulse into effective support excitation load on the test vehicle.

However, in product application transient dynamic stresses may be imposed on parts with accrued thermo-mechanical damage. Life prediction in presence of sequential and simultaneous transient-dynamic and thermal loads is presently beyond the state of art. Insight into the nature of damage initiation and progression will enable the formulation of damage relationships for life-prediction in shock environments. Material deformation under high strain rates, previously, has been incorporated in simulation frameworks using linear elastic models and elastic-plastic models [Lall 2004, 2005, 2006a-c, 2007a-e, 2008a-d, Xie 2002, 2003, Wu 1998, 2000] for interconnects.

2.6 Failure Analysis

Failure analysis is necessary to understand the mechanisms that cause deterioration in reliability of electronic packaging. Prediction of failure was investigated using fracture mechanics [Shah 2004], von-misses stress [Tee 2004], and board-strain based damage index [Lall 2005]. Failure in the interconnect occurs at the interface close to the device or board side as these are the highest stressed locations in the joint.

The extent of damage and failure modes varies for different alloy systems. [Tsai 2005] impact failure modes of SnPb solder were predominated by bulk failures as the bulk solder deformation absorbs some of the impact strain and cracks through solder rather than through the interfacial intermetallic. Lead-free solder, on the other hand, exhibits a mixture of IMC and bulk failure that occur along the bond interface. [Jang 2007] The imposed strain in the SnAgCu joints moves away from the bulk solder into the lower strength brittle IMC as the apparent strength of the solder increases at higher strain rates. [Kim 2007] Comparison of the failure modes of SAC alloys indicated that crack propagation through the bulk solder was more in SAC105, due to a lower elastic modulus, than brittle IMC layer in SAC405.

The addition of impurities and different combinations of alloy systems and surface finishes cause variations in failure mechanisms. A comparison of the failure modes in SAC305 and Sn1.2Ag0.5Cu0.05Ni shows an increase in drop reliability and a shift in fracture mode from interface failure to bulk failure [Kim 2006]. Syed et. al. [Syed 2007] compared a number of solder alloys to illustrate that the interfacial failure on the package side was the primary mode of failure for SAC305 with the ENIG surface finish. The failure shifted to board side through the bulk solder for the SAC125Ni solder alloy in

combination with Cu-OSP. [Lall 2008d] Failure modes in drop-impact for CABGA package with six different solder alloys (SAC105, SAC305, SAC0307, SAC0307+Bi, SAC0307+Bi+Ni, Sn3.5Ag) have been discussed. And results show that SAC305, SAC0307 and SAC105 exhibit superior characteristic life amongst all the SAC alloy system and Sn3.5Ag is the least reliable.

2.7 Life Prediction Models

Life prediction models based on strain range, accumulated creep strain or accumulated strain energy strain density during a temperature cycle have been proposed [Coffin 1954, Manson 1965, Darveaux 1995, Lee 2000]. BGA solder joint strain from finite element analysis in conjunction with empirically derived formula of universal slopes (Manson, 1965) based on high cycle fatigue test data for life prediction of BGA solder joint under vibration [Wong 1999]. Life prediction parameters used are Monkmann-Grant equation for creep rupture and time-fraction rule [Syed 2004]. Coffin-Manson fatigue models [Che 2004] have been implemented for packages subjected to temperature cycling. Various packages including TFBGA (Thin-profile Fine- Pitch BGA), VFBA (Very-thin-profile Fine-Pitch BGA), CSPs have been tested with thermal cycling and life prediction models based on Anand's constants provided by Darveaux [Ng 2005] have been spotted in the literature. Linear superposition method by Miner's Law has been assumed for electronic assemblies subjected to vibration with clamped-clamped boundary conditions [Pang 2004, Wong 2004], the number of cycles required to produce failure are extracted from mean-time-to-failure (MTTF). The actual number of fatigue cycles accumulated in different environment was calculated experimentally.

Stress based fatigue models are developed [Pang 2004, Perkins 2004] for flip-chip, and ceramic column grid array (CCGA) packages. For JEDEC drop tests of electronic assemblies, peeling stress and mean impact life based life prediction models have been proposed [Luan 2005]. Fracture mechanics based fatigue life-prediction model Paris' law for life prediction on high cycle vibration fatigue in BGA packages [Liu 2006]. Random vibration testing of motherboards for fatigue-life prediction of BGA package solder joints based on Miner's cumulative damage theory [Wong 2007]. Morrow's energy based life prediction model for leaded and lead free solder joints under thermal cycling test and cyclic bending test and model shows average volume energy dissipation in leaded solder joint is larger than lead-free one for same loading conditions [Kim 2007]. Two failure prediction model namely the Timoshenko-beam failure model and the cohesive zone failure model to predict the location and mode of failures in the solder interconnections subjected to drop impact [Lall 2007]. Life prediction model based upon the relationship between the maximum stress at the package/substrate interface of critical solder joint and corresponding drop impact life [Luan 2008].

CHAPTER 3

HIGH SPEED DIGITAL IMAGE CORRELATION TECHNIQUES FOR TRANSIENT STRAIN MEASUREMENT IN ELECTRONICS SUBJECTED TO DROP AND SHOCK

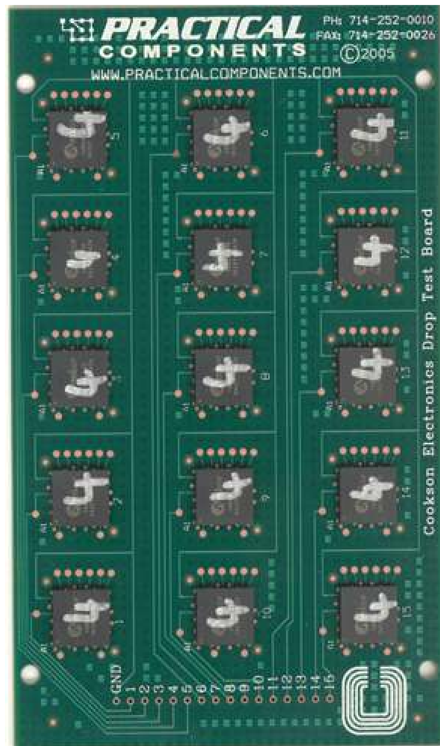
3.1 Introduction

Digital image correlation (DIC) technique is a non contact optical method for full-field deformation and their derivatives measurement. In this work, DIC in conjunction with high speed cameras have been used to measure the displacement field quantities and their derivatives in electronic assembly subjected to drop and shock. DIC data has been correlated with the experimental data across various locations of the test vehicle. Electrical continuity was monitored for all the daisy chained packages during the transient event. And the data extracted from DIC technique is used to develop fatigue constants for lead-free solder interconnects subjected to drop and shock by conjoining it with explicit finite element models for the first time.

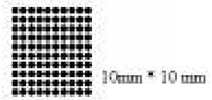
3.2 Experimental Test Boards, Setup and Procedure

In this study, test board used for experimentation is according to JEDEC standards (JESD22-B111) with overall board dimension being 132mm$\times$77mm$\times$1mm and 15 chip-array ball-grid array (CABGA) packages populated on one side having I/O count of 100

and pitch of 0.8mm in a three-row, five-column format. Printed Circuit board is made up of FR4-06. All the packages used in the test configuration were daisy chained. The surface finish of the test boards were ENIG on populated side and Cu-OSP on unpopulated side. Solder interconnects were manufactured as solder masked defined (SMD) on populated side and as non solder masked defined on unpopulated side (NSMD). Table 3.1 shows the package architecture and geometry details. Three different alloy composition including Sn1Ag0.5Cu (*SAC105*), Sn3Ag0.5Cu (*SAC305*) and 96.5Sn3.5Ag (*Sn3.5Ag*) were examined for this board. The composition of the various alloy system are shown in Table 3.2. First set of three different alloy composition based boards were examined at pristine conditions and second set of three different alloy composition based boards were subjected to sequential stresses of thermal aging (100hrs, 125°C), followed by shock impact to investigate the effect of cumulative damage of the overlapping stresses. Two configurations each solder alloy test boards were tested. The first configuration was without any weights attached to test board and second configuration with weights attached to the test board to simulate the weight of shields and other component on the test board. Figure 3.1 shows the test board used.



Interconnect array configuration



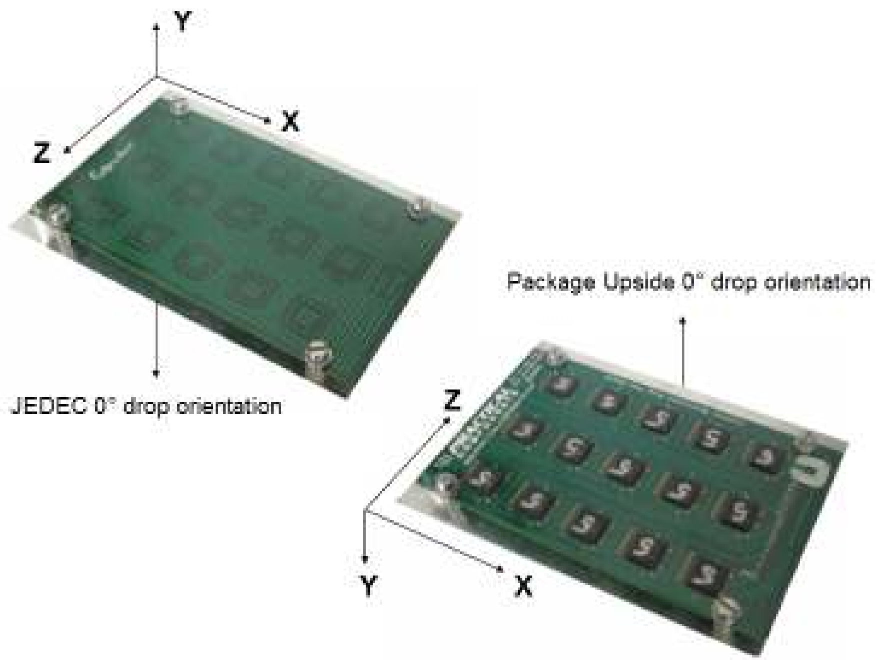


Figure 3.1: Test Board.

Table 3.1: Package Architecture of 100 I/O CABGA

	10mm, 100 I/O, CABGA
Ball Count	100
Ball pitch(mm)	0.8
Die Size(mm)	0.55
Substrate Thickness(mm)	0.232
Ball Diameter(mm)	0.48

Table 3.2: Lead Free Alloy Composition

Alloys	**Composition**
SAC105	Sn: 98.5%,Ag: 1%, Cu: 0.5%
SAC305	Sn: 96.5%,Ag: 3%, Cu: 0.5%
Sn3.5Ag	Sn: 96.5%,Ag: 3.5%,

The four corners of the test board were constrained to the drop table with four screws there by eliminating the translation and rotation d.o.f at four corners of the board. The test assemblies have been subjected to a 1500g, 0.5ms pulse consistent with the JESD22-B111. The drop height and pulse shape has been adjusted using pulse shapers between the impacting surfaces. A half-since pulse has been achieved. Test boards were also subjected at intermittent height to reach different G levels. The lansmont Model23 drop tower has been used for the shock-test. Figure 3.2 shows the test board mounted on the shock platform and schematic of the high-speed camera locations. The drop-event was simultaneously monitored with ultra high-speed video camera operating at 50,000 frames per second. Figure 3.3 shows calibration images which are necessary to calibrate cameras before recording the drop event. Calibration involves capturing the images of the predefined target at various orientations near the impact location. In our study, target used consisted of a 9 x 9 grid of black points on the white background with a 10 mm pitch. About 25 such images were taken in order to get good calibration. Strain and continuity data were simultaneously acquired during the drop event using a high-speed data acquisition system at a sampling frequency of 5 million samples per second. Figure 3.4 shows the detection of failure on one of package interconnects with corresponding transient-strain history during JEDEC drop-test for a thermally aged SAC105 Package 12. Failure in the device has been identified as an increase in voltage drop. Different packages on the test board exhibit different strain histories during the same drop and different number of drops to failure.

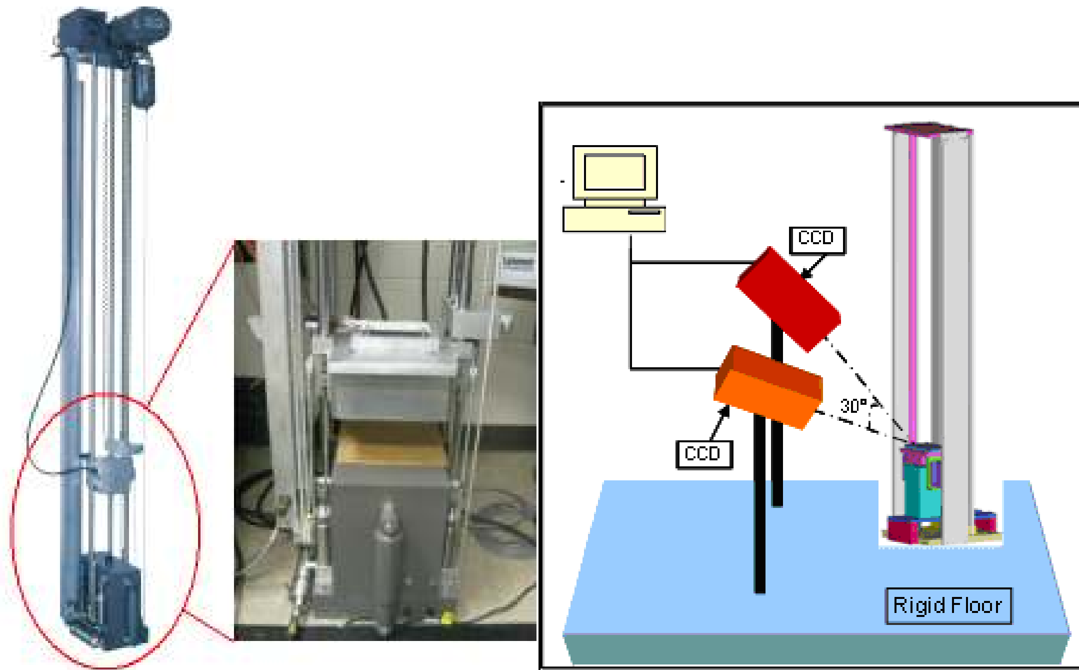


Figure 3.2: Experimental Set-up for Controlled JEDEC Drop Test using LANSMONT Drop Test Tower.

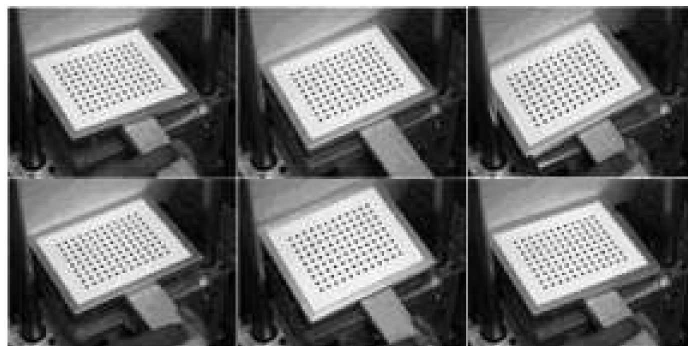


Figure 3.3: Calibration Images

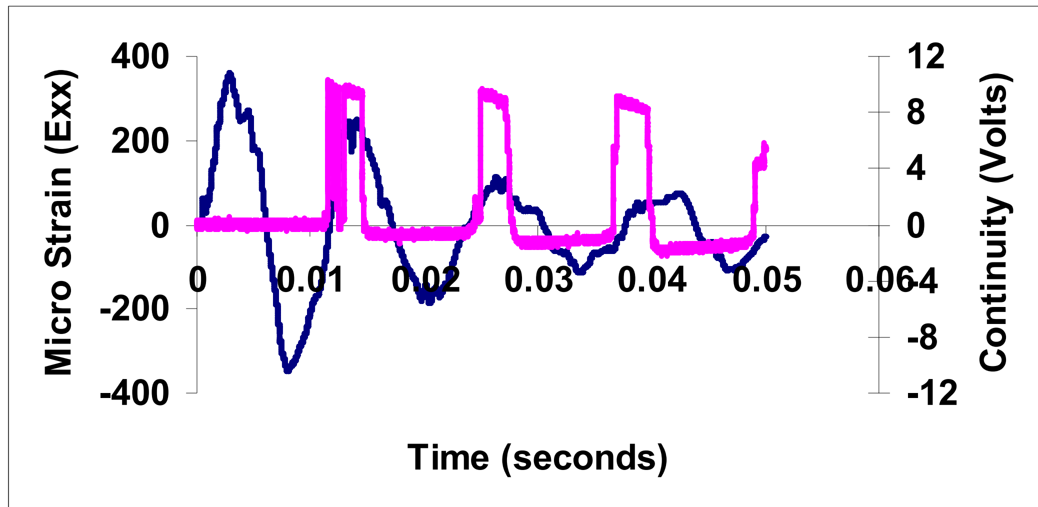


Figure 3.4: Package Strain and corresponding Continuity Transient History in JEDEC Drop-Shock for Failed Package (Thermally aged SAC105 Package 12 failure indication).

3.3 Digital Image Correlation Technique

Digital image correlation (DIC) is an optical method to measure full field deformation and their derivatives on the surface of a loaded structure. Previously, the feasibility of using DIC for transient strain measurement in electronic assemblies, in the presence of rigid body motion has been demonstrated [Lall 2007[a-e], 2008a-d]. The technique involves the application of speckle pattern on the surface of the printed circuit board assembly and tracking a geometric point on the speckle patterned surface before and after loading and using it to compute both in-plane as well as out-of-plane deformations in the structure.

Displacement field quantities are obtained by tracking a geometric point before and after deformation [Zhou 2001, Amodio 2003, Srinivasan 2005, Kehoe 2006, Lall 2007c, 2008c,d]. The tracking is achieved using digital image processing of speckle pattern on the specimen surface. Figure 3.5 shows. 3D-Digital Image Correlation Measurement in Printed Circuit board Assembly

The sub image before impact is referred as I_1 (r) a reference image and the one after impact is referred as I_2 (r) a deformed image respectively, which are related as follows:

$$I_2(r) = I_1[r - U(r)] \quad 3.1$$

$$I_1(r) = I_2[r + U(r)] \quad 3.2$$

Where U(r) is the displacement vector at pixel $r = (x, y)^T$.

The difference in the positions of the current pixel and the reference pixel gives the in-plane as well as out-of-plane displacement U(r) of this reference pixel. Full-field displacement can thus be found out by changing the reference pixel location on the speckle patterned surface and following the same procedure described as above.

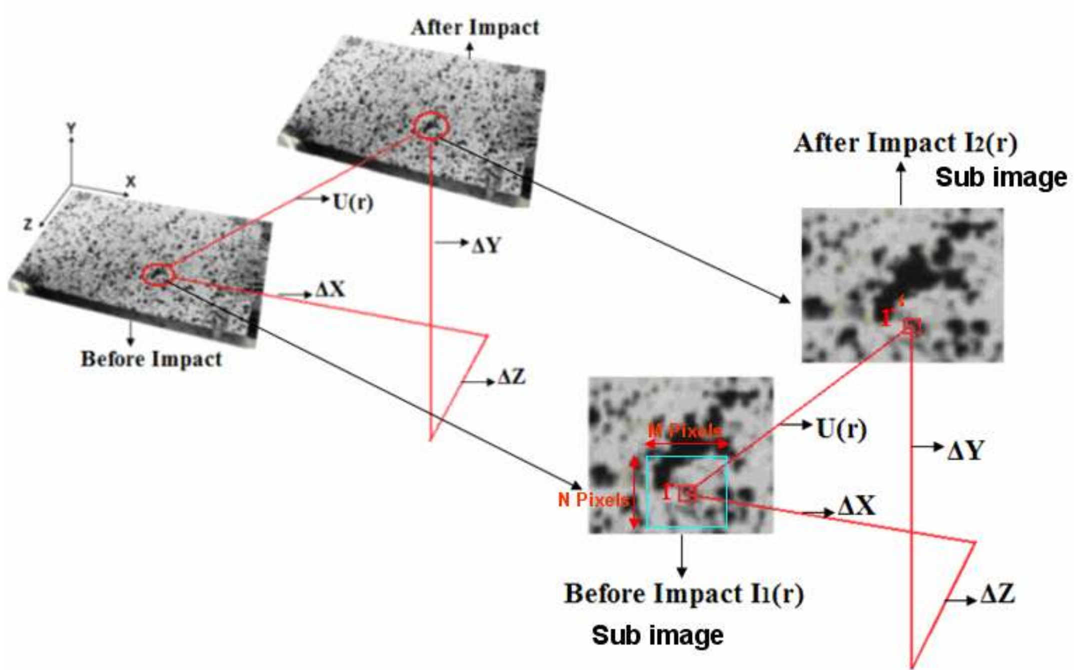


Figure 3.5: 3D-Digital Image Correlation Measurement in Printed Circuit board Assembly.

An algorithm based on the mutual correlation coefficient or other statistical functions are used to correlate the change in a reference pixel in the original image and the corresponding reference pixel in the deformed image. Three such typical correlations include absolute difference, least square and cross correlation. There are three typical correlation functions which are used and are defined as follows:

Absolute difference:

$$C_A(r') = 1 - \frac{\iint_\Omega |I_2(r + r') - I_1(r)| dr}{\iint_\Omega I_1(r) dr} \quad 3.3$$

Least square:

$$C_L(r') = 1 - \frac{\iint_\Omega [I_2(r + r') - I_1(r)]^2 dr}{\iint_\Omega I_1^2(r) dr} \quad 3.4$$

Cross-Correlation:

$$C_C(r') = 1 - \frac{\iint_\Omega I_1(r) I_2(r + r') dr}{\left[\iint_\Omega I_1^2(r) dr \iint_\Omega I_2^2(r + r') dr\right]^{1/2}} \quad 3.5$$

where Ω (M x N) is the area of the subimage around reference pixel r, r\` is the current pixel, $C_A$(r\`) is the current absolute correlation function, C_L(r\`) is the current least square correlation function, and $C_C$(r\`) is the current cross-correlation function. The absolute and least square correlation functions require less computation since constant brightness is assumed. In some cases there is a need to handle the changes in illumination; then the normalized cross-correlation is used, which is computationally demanding.

Correlation functions determine the difference between the current pixel r’ and the reference pixel r, by matching the two sub-images. To estimate sub-pixel displacements,

U(r) in a sub-image corresponding to a pixel $r_0 = (x_0, y_0, z_0)^T$ in the current image $I_2(r)$ is assumed to be constant [Davis 1998].

$$U(r) = U(r_o) = U_o = (u_o, v_o, w_o)^T \tag{3.6}$$

Equations (3.1) and (3.2) can then be written as; [Zhou 2001]

$$I_2(r) = I_1[r - U_0] \tag{3.7}$$

$$I_1(r) = I_2[r + U_0] \tag{3.8}$$

Taylor expansion of these two equations yields:

$$I_2(r) = I_1(r)U_0^0 - \frac{\partial I_1}{\partial r^1}U_0^1 + \frac{\partial I_1}{\partial r^2}U_0^2 - \frac{\partial I_1}{\partial r^3}U_0^3 + K$$

$$I_2(r) = I_1(r) - \nabla I_1(r)U_0^1 + \nabla I_1(r)U_0^2 - \nabla I_1(r)U_0^3 + K \tag{3.9}$$

Neglecting higher order terms,

$$I_2(r) = I_1(r) - \nabla I_1(r).U_0 \tag{3.10}$$

$$I_1(r) = I_2(r) + \nabla I_2(r).U_0 \tag{3.11}$$

where $\nabla I_1(r)$ and $\nabla I_2(r)$ are spatial gradients of two images.

Equations (3.10) and (3.11) can be rearranged as [Zhou 2001]:

$$[\nabla I_1(r) + \nabla I_2(r)].U_0 = 2[I_1(r) - I_2(r)] \tag{3.12}$$

Equation (3.11) holds for M x N pixels in a sub image Ω around r_0 and therefore leads to M x N equations. The least squares approximate solution to these equations is then determined by [Zhou 2001]:

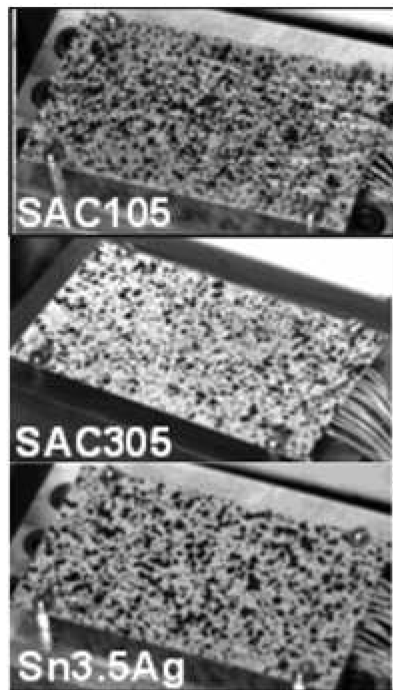
$$U_0 = (A^T A)^{-1} A^T.b \tag{3.13}$$

where,

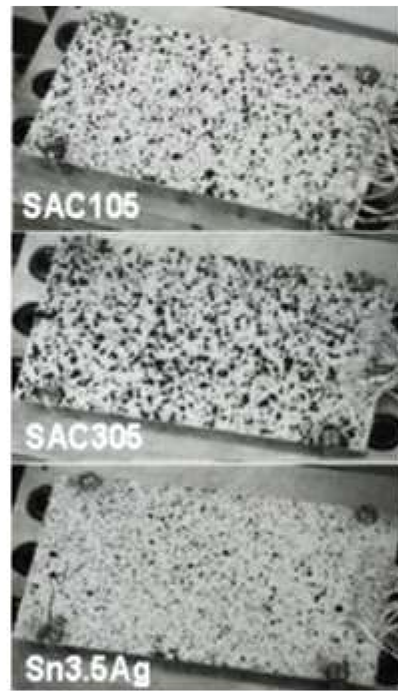
$$A = \begin{pmatrix} \cdot \\ \cdot \\ \nabla^T I_1(r) + \nabla^T I_2(r) \\ \cdot \\ \cdot \end{pmatrix}_{M.Nx2, r \in \Omega} \qquad 3.14$$

$$b = \begin{pmatrix} \cdot \\ \cdot \\ 2[I_1(r) - I_2(r)] \\ \cdot \\ \cdot \end{pmatrix}_{M.Nx1, r \in \Omega} \qquad 3.15$$

Transient strain was measured using two methods simultaneously including, digital image correlation in conjunction with high-speed imaging and strain gages with high-speed data acquisition. Strain gages were mounted at different locations on the test board on both package and board side. Figure 3.6 shows the speckle pattern on the pristine and thermally aged board. Figure 3.7 shows the speckle coated image of test board on both package side and board side with strain gages. Previous researchers have demonstrated the effect of speckle size and distribution on accuracy of the measurements [Zhou 2001, Gu 2006]. Effort has been made to maintain consistency of speckle patterns on all the test boards. The package deformation and printed circuit assembly deformation has been measured using digital image correlation. The data has been used to develop transient strain histories during the shock event.



(A) Pristine boards



(B) Thermally-Aged boards

Figure 3.6: Speckle Patterns for various Test Boards

(A) Package Side **(B) Board Side**

Figure 3.7: Speckle Coated Image of Test Board with Strain Gages

3.4 Correlation of Strains from DIC Technique and Strain Gage and Discussion on Repeatability of Shock Input

Transient strain histories extracted from DIC technique was correlated with discrete strain gages at multiple location on both package side as well as on board side of the test boards. Figure 3.8 shows package numbering scheme and strain gages locations on pristine SAC105 test board. Figure 3.9, Figure 3.10 and Figure 3.11 shows the comparison of strain values from DIC and strain gages at three discrete locations on pristine SAC105 test board. DIC strain data were accurate and consistent with strain gage sensor.

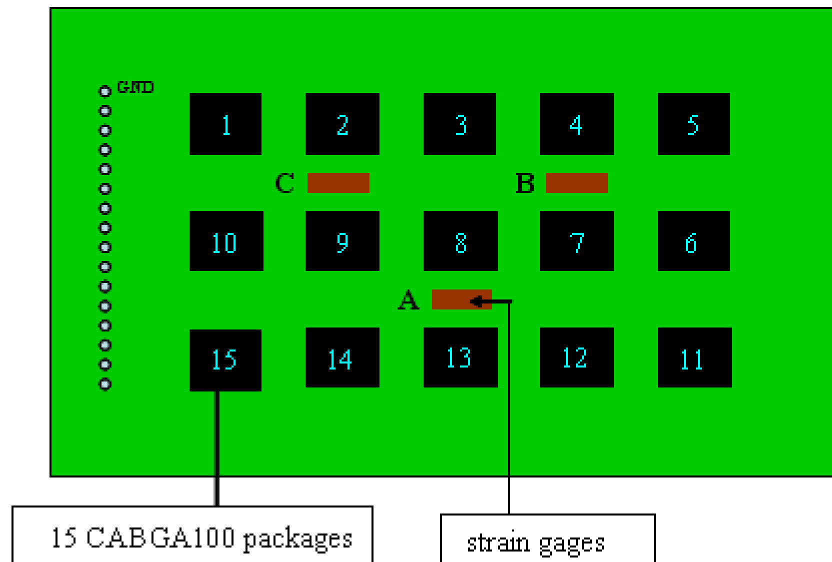


Figure 3.8: Package Numbering Scheme and Strain Gage Locations on SAC105 Pristine Test Board.

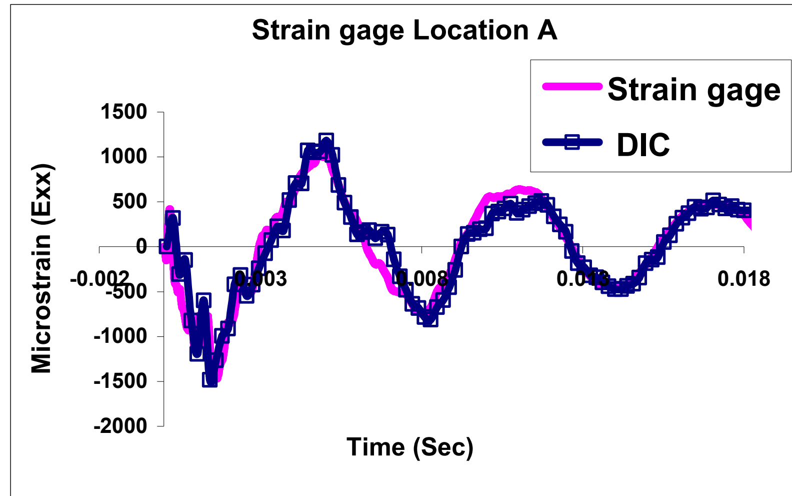


Figure 3.9: Strain (E_{xx}) Correlation from DIC and Strain Gage for SAC105 Pristine Test Board at location A.

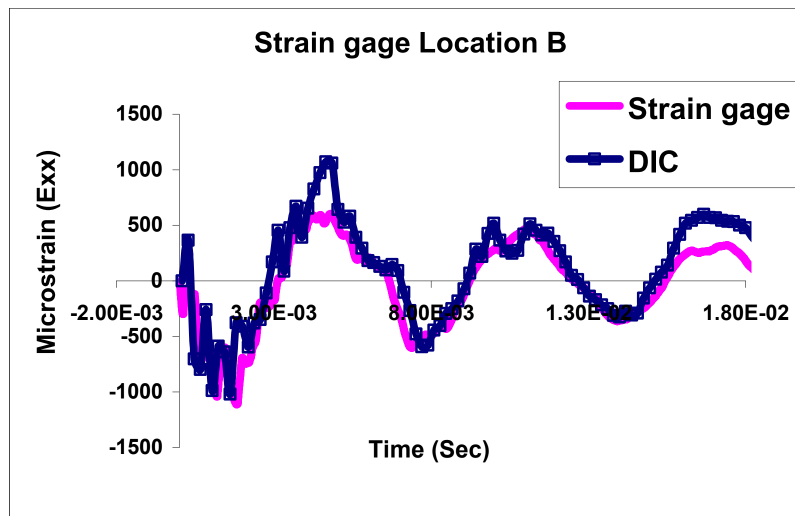


Figure 3.10: Strain (E_{xx}) Correlation from DIC and Strain Gage for SAC105 Pristine Test Board at location B.

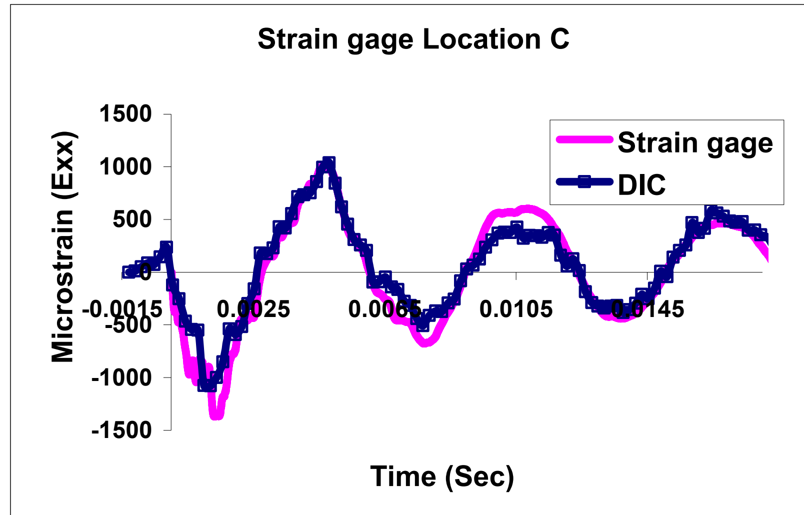


Figure 3.11: Strain (E_{xx}) Correlation from DIC and Strain gage for SAC105 Pristine Test Board at location C.

Previous works have shown that small variations in the drop orientation can produce vastly varying transient-dynamic board responses. Significant effort was invested in developing a repeatable drop set-up. Repeatability of the shock input has been quantified for the experimental test assemblies. Repeatability of the shock orientation and shock pulse is critical in developing model correlations. The strain histories measured are very consistent and repeatable for all component location on the test board for various drops. Figure 3.12, Figure 3.13 and Figure 3.14 shows the repeatability of the transient strain at location 2, 9, 14 on printed circuit assembly with Sn1Ag0.5Cu solder interconnect for five-consecutive shock events . Figure 3.15 shows the DIC based deformation contour with the corresponding actual deformation contour of the test board. Figure 3.16 shows the DIC measured strain contour along the length of the board at different time steps for the same drop event.

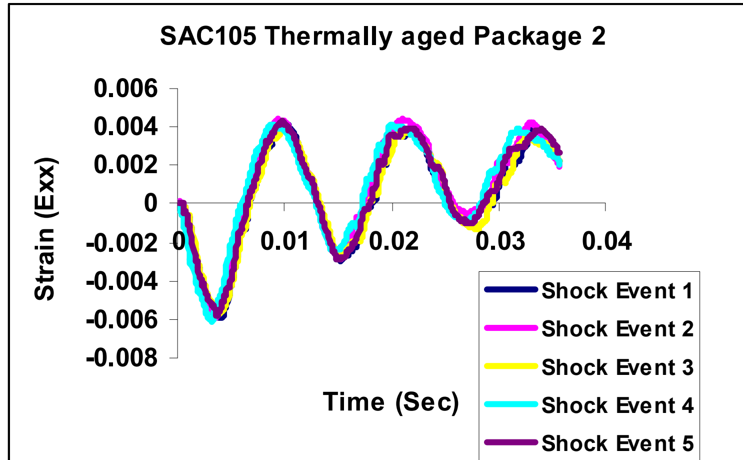


Figure 3.12: Strain Repeatability for SAC105 thermally aged test board at Package 2 on Board Side.

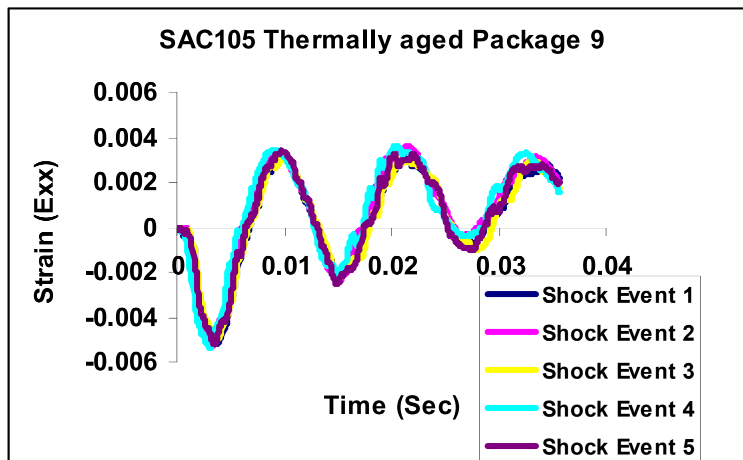


Figure 3.13: Strain Repeatability for SAC105 Thermally Aged Test Board at Package 9 on Board Side.

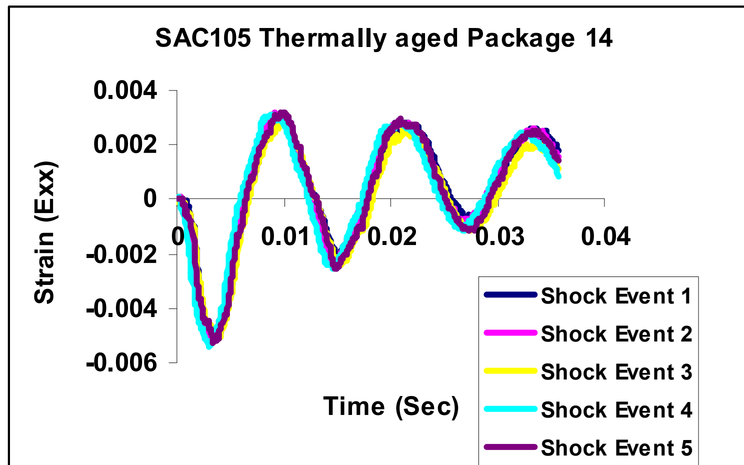


Figure 3.14: Strain Repeatability for SAC105 Thermally Aged Test Board at Package14 on Board Side.

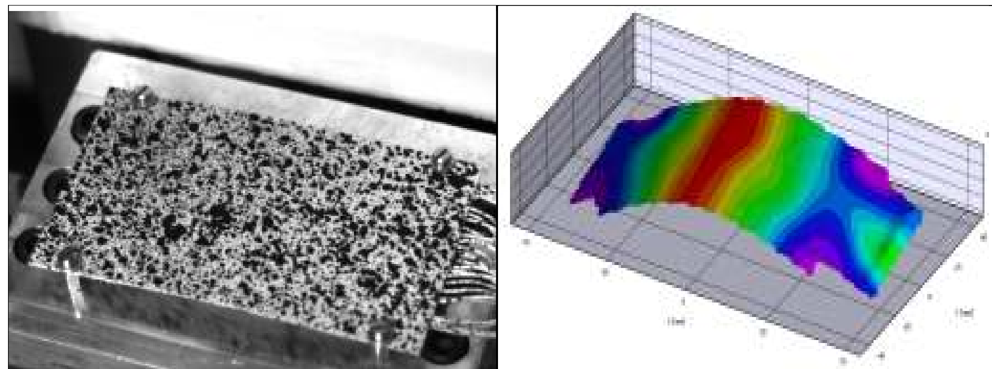
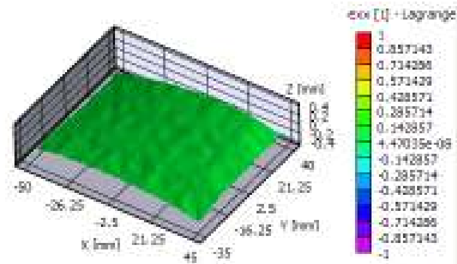
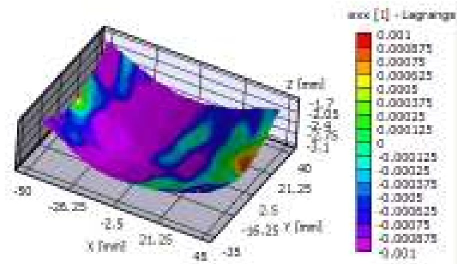


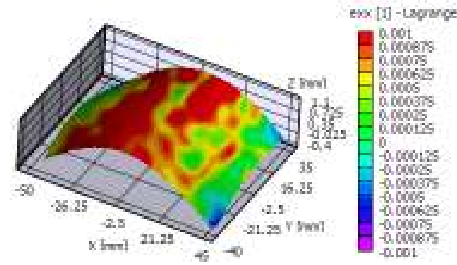
Figure 3.15: Comparison of DIC Strain Contour with the Actual Contour.



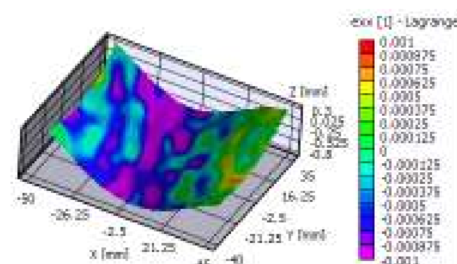
Before Impact



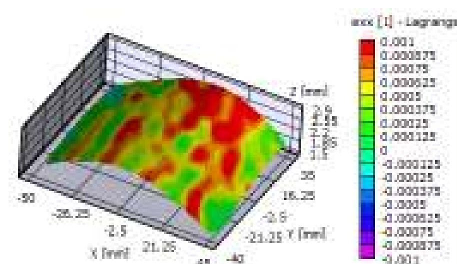
Time=1.15ms



Time=4.5ms



Time=7.5ms



Time=10.5ms

Figure 3.16: DIC Measured Strain Contour along the Length of the Board (E_{XX}) at Different Time Steps.

DIC technique has been applied on images obtained from high speed cameras at the particular package both on package side as well as on board side. The data obtained from these images has been used to study whether there is any significant change in the strain contour at same package with different solder alloy system. Figure 3.17:, Figure 3.18, Figure 3.19 and Figure 3.20 shows the 2D strain contour of package 12 on package side as well as on board side in the longitudinal direction (E_{XX}) obtained from DIC at 2.5 milliseconds after impact for all the three solder alloys system for both pristine and thermally aged conditions.

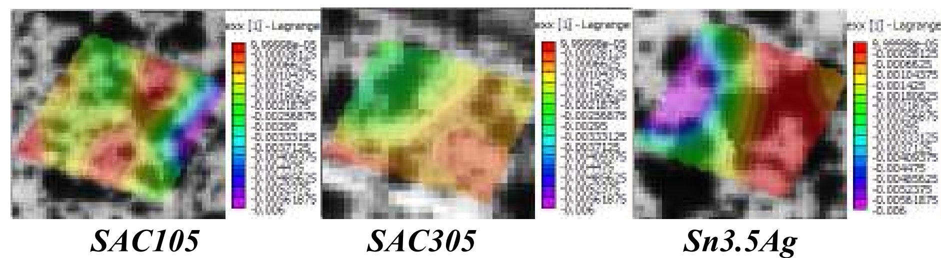


Figure 3.17: Package side 2D-Strain (E_{XX}) contour on package 12 at 2.5ms after impact for PRISTINE Assemblies.

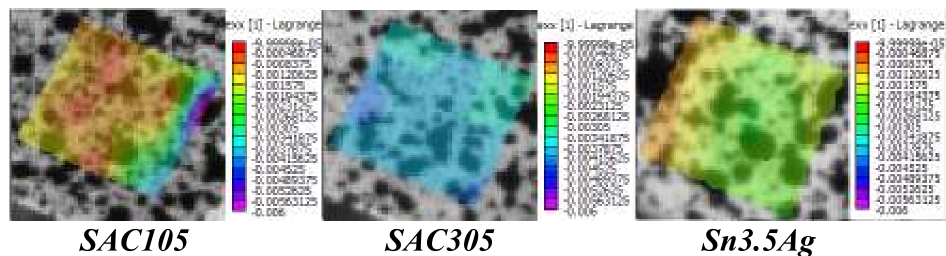


Figure 3.18: Board Side 2D-Strain (E_{XX}) contour on package 12 at 2.5ms after impact for PRISTINE Assemblies.

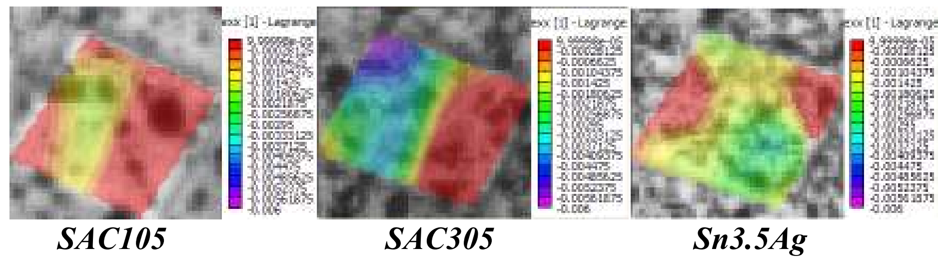


Figure 3.19: Package Side 2D-Strain (E_{xx}) contour on package 12 at 2.5ms after impact for THERMAL AGED Assemblies.

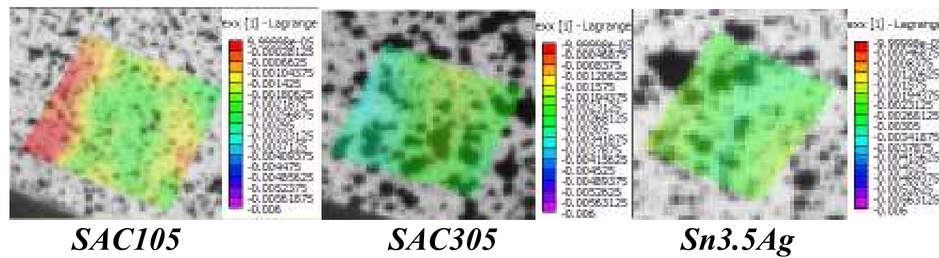


Figure 3.20: Board Side 2D-Strain (E_{xx}) contour on package 12 at 2.5ms after impact for THERMAL AGED Assemblies.

CHAPTER 4

MODELING METHODOLOGY FOR DROP SIMULATION

4.1 Introduction

Finite element analysis is used as a numerical tool to understand the transient dynamic behavior of electronic assemblies subjected to Shock-Impact. In this work, life prediction of electronic assemblies based on the lead-free solder interconnects strain histories have been carried out. Various element formulations have been employed to model the second level packaging. State of the art modeling techniques has been employed to model the PCB assemblies. Three main modeling approaches includes smeared property model with conventional shell elements, continuum shell with Timoshenko-beam model and node based explicit sub-model. First and the second modeling approach are independent from the actual drop test where as node based sub-modeling approach is an experimental data driven numerical technique. Transient dynamic deformation of the test boards is a wave propagation problem and hence explicit time integration scheme has been implemented to simulate the drop phenomenon. Reduced integration elements have been employed to achieve computational efficiency and save time. Transient dynamic behavior of the PCB assembly in horizontal JEDEC drop has been measured using DIC technique conjoined with high speed imaging at

50,000 frames per second. Finite element modeling results have been correlated with digital image correlation data at various locations on the printed circuit board assembly.

4.2 Modeling Methodology Adopted for Drop Impact Simulation.

Board level drop simulations were carried out in the 0-degree horizontal JEDEC drop orientations. Figure 4.1 shows the modeling methodologies adopted for horizontal drop simulation. Smeared property model with conventional shell elements, continuum shell models with Timoshenko beam elements and the node based sub-model are the three modeling techniques which were implemented successfully. The finite element analysis was performed using commercial software ABAQUS V6.7 using the explicit time integration scheme. The use of the explicit finite elements enables the calculation of response history using step-by-step integration in time without changing the form of dynamic equations as done in modal methods. Various element formulations such as continuum solid elements, conventional and continuum shell elements, Timoshenko beam elements and rigid elements were used to create the global models. Local model were modeled with a fine mesh to capture the detailed distribution of strains of interconnects and the various individual layers. Cohesive zone elements were deployed in the explicit sub-model across the inter-metallic layer (IMC) for life prediction of the solder interconnects. The printed circuit board assemblies were dropped from drop heights of 0.75 feet for JEDEC drop. Figure 4.2 show the finite element model for PCB assembly and Figure 4.3 shows the schematic representation of the drop simulation of the PCB assemblies in JEDEC drop. The impact event has been modeled for the total time duration of 15 milliseconds since the maximum strain occur during the first 10 to 15

milliseconds after impact. Time history of the displacement field quantity and their derivatives were output to correlate with the experimental data.

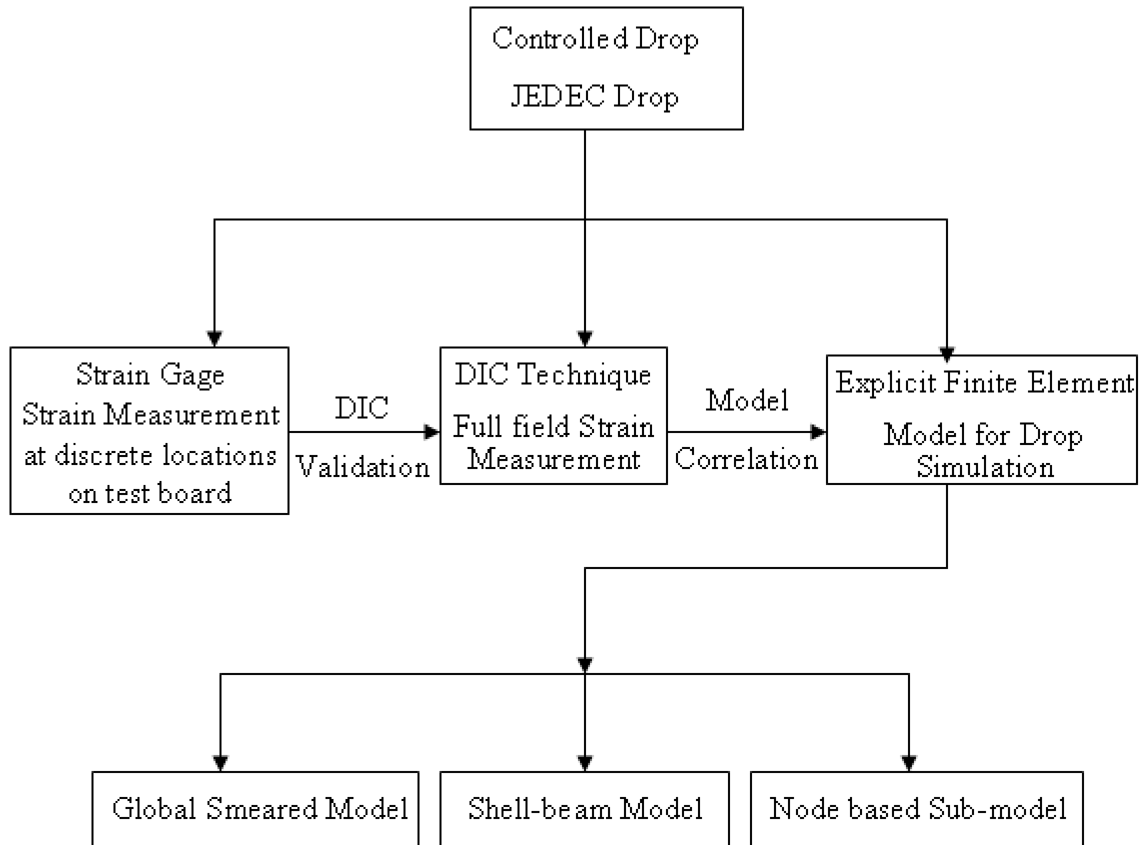
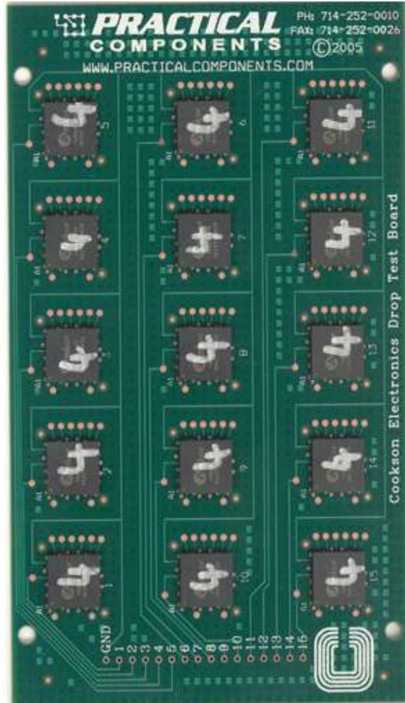
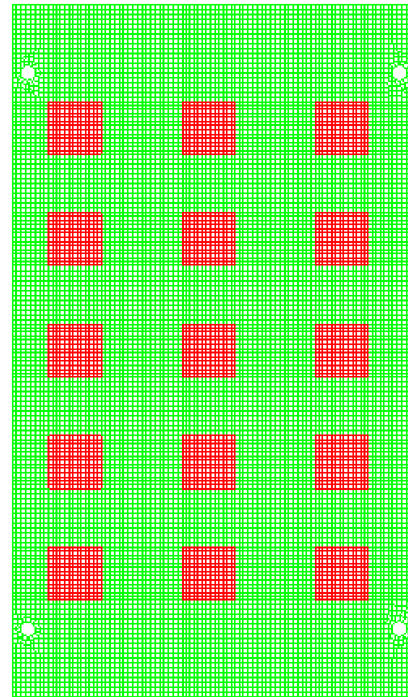


Figure 4.1: Modeling Methodologies Adopted for Horizontal Drop Simulation.



(A) Actual Test Board



(B) Finite Element Model of a Test Board

Figure 4.2 : Finite Element Model created using Hypermesh.

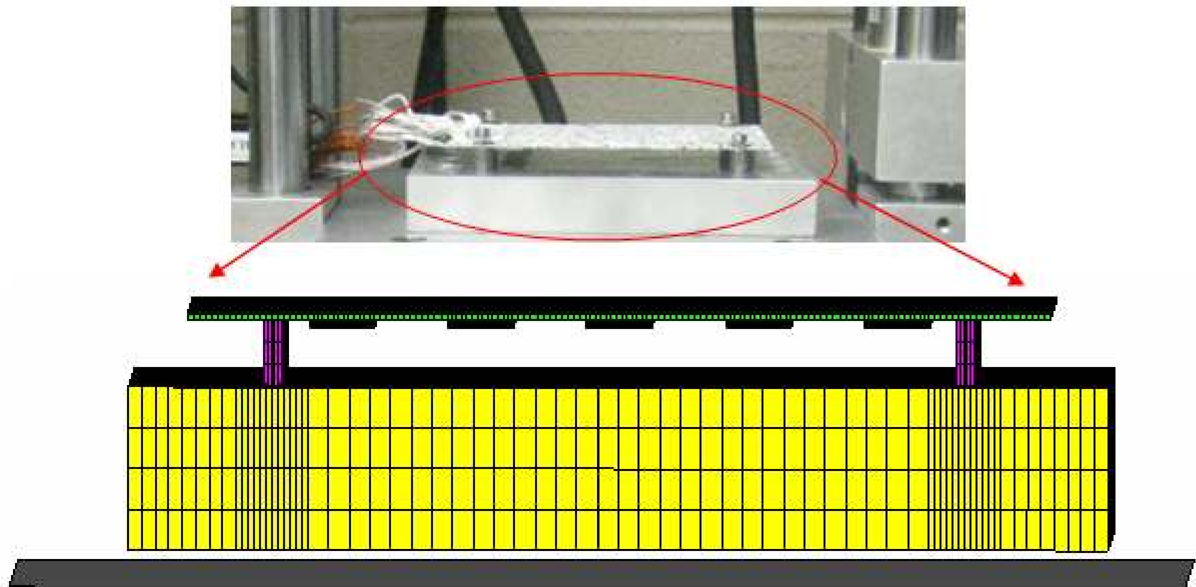


Figure 4.3: Schematic Representation of the Drop Simulation of the PCB Assemblies in JEDEC Drop.

4.3 Direct Integration Scheme

In the direct integration method the word "Direct" means before the numerical integration is performed no transformation of the equation (4.1) (*equation of equilibrium governing the linear dynamic response of a system of the finite elements*) from one form into another is carried out and the equations are integrated numerically step by step procedure. The objective of the direct integration method is to satisfy equation (4.1) only at discrete time interval Δt instead of trying to satisfy it at any time interval, t. In this method, the effects of inertia and damping forces are searched at discrete time point within the solution interval. Secondly in the direct integration method, variation of displacement, velocity and acceleration are assumed at particular time interval. Hence, based on the assumptions accuracy, stability and cost of the solution will vary significantly. In this method problems are solved using constant time step Δt (linear analysis) and can be expanded to varying time step size (nonlinear analysis).

$$M\{\ddot{D}(t)\} + C\{\dot{D}(t)\} + K\{D(t)\} = R(t) \qquad 4.1$$

Where M is the mass matrix, C is the damping matrix, K is the stiffness matrix, R is the vector of externally applied loads, D is the displacement vector, $\dot{D}$ is the velocity vector and $\ddot{D}$ is the acceleration vector of the finite element assemblage. Equation (4.1) can be rewritten by considering statics at time t as follows

$$F_{Inertia}(t) + F_{Damping}(t) + F_{Elatic}(t) = R(t) \qquad 4.2$$

Where $F_{Inertia}(t) = M\{\ddot{D}\}$, $F_{Damping}(t) = M\{\dot{D}\}$ $F_{Elatic}(t) = K\{D\}$ all are time dependent.

In dynamic analysis acceleration dependent inertia force, velocity dependent damping forces are considered unlike in static analysis where these two forces are neglected. In non-linear analysis effect of velocity dependent forces and acceleration dependent forces are always included to attain accurate solution.

Equation of motion at n^{th} time step is written as equation (4.3) and this form is better suited to a nonlinear problem in which [k] may change from one time step to the next

$$[M]\{\ddot{D}\}_n + [C]\{\dot{D}\}_n + \{R^{int}\}_n = \{R^{ext}\}_n \qquad 4.3$$

Direct integration method compute conditions at time step n+1 from the equation of motion, a difference expression and known condition at one or more preceding time steps. Algorithms are categorized as explicit or implicit. An explicit algorithm uses a difference expression of the general form

$$\{D\}_{n+1} = f\left(\{D\}_n, \{\dot{D}\}_n, \{\ddot{D}\}_n, \{D\}_{n-1}, ...\right) \qquad 4.4$$

which contains only historical information on its right-hand side. Equation (4.4) is combined with equation of motion at time step n.

An implicit algorithm uses a difference expression of the general form

$$\{D\}_{n+1} = f\left(\{\dot{D}\}_{n+1}, \{\ddot{D}\}_{n+1}, \{D\}_n, \{\dot{D}\}_n, \{\ddot{D}\}_n, ...\right) \qquad 4.5$$

which is combined with the equation (4.3) at time step n+1.

In order to implement the direct integration scheme in practical application, choice between explicit and implicit methods are made based on stability and economy. Explicit methods are conditionally stable, which means there is a critical time step Δt_{cr} that must not exceed if the numerical process is not to blow up by becoming unstable. Since Δt_{cr} is quite small, great many times steps are needed, but each is executed quickly. But implicit

methods are unconditionally stable regardless of how large Δt becomes. In explicit method, the coefficient matrix of $\{D\}_{n+1}$ can be made diagonal, so that $\{D\}_{n+1}$ is cheaply computed in each time step. Where as in case of implicit method $\{D\}_{n+1}$ can not be made diagonal, so the cost per time step is greater, increasing so as the finite element mesh increases in dimensionality. It is important to choose the appropriate direct integration scheme to tackle the problem. Problems are categorized as the wave propagation type and structural dynamics type. A wave problem is created by blast or impact loading where high-frequency modes must be represented in analysis. Response analysis is usually needed to span only a small time interval. A structural problem is created by loads that vary more slowly, such as loads created by earth quake where response is dominated by lower modes. The explicit formulation is better suited to accommodate material and geometric non-linearity without any global matrix manipulation. For these reasons, the explicit time integration formulation is used in the drop impact analysis of a test board.

For the explicit formulation, $\{D\}_{n+1}$ and $\{D\}_{n-1}$ can be expanded using the Taylor series to obtain:

$$\{D\}_{n+1} = \{D\}_n + \Delta t \{\dot{D}\}_n + \frac{\Delta t^2}{2}\{\ddot{D}\}_n + \frac{\Delta t^3}{6}\{\dddot{D}\}_n + \cdots \quad 4.6$$

$$\{D\}_{n-1} = \{D\}_n - \Delta t \{\dot{D}\}_n + \frac{\Delta t^2}{2}\{\ddot{D}\}_n - \frac{\Delta t^3}{6}\{\dddot{D}\}_n + \cdots \quad 4.7$$

Subtracting equation (4.7) from equation (4.6) and neglected terms with orders of Δt greater than two, the velocity and acceleration at time step n can be approximated by the central difference equations as:

$$\{\dot{D}\}_n = \frac{1}{2\Delta t}\left(\{D\}_{n+1} - \{D\}_{n-1}\right) \quad 4.8$$

$$\{\ddot{D}\}_n = \frac{1}{\Delta t^2}\left(\{D\}_{n+1} - 2\{D\}_n + \{D\}_{n-1}\right) \quad 4.9$$

Substituting Equations (4.8) and (4.9) in the equation of motion, equation (4.3) written at time step n and solving for $\{D\}_{n+1}$, we get:

$$\left[\frac{1}{\Delta t^2}M + \frac{1}{2\Delta t}C\right]\{D\}_{n+1} = \{R^{ext}\}_n - \{R^{int}\}_n + \frac{2}{\Delta t^2}[M]\{D\}_n - \left[\frac{1}{\Delta t^2}M - \frac{1}{2\Delta t}C\right]\{D\}_{n-1} \quad 4.10$$

In order to have equation (4.10) to be conditionally stable we need to have,

$$\Delta t \le \left(\frac{2}{\omega_{max}}\right) = \Delta t_{cr}$$

or 4.11

$$\Delta t \le \left(\frac{T_{min}}{\Pi}\right)$$

where frequency ω_{max} and its period T_{min} corresponds to the highest natural frequency of

$$\left([K] - \omega^2[M]\right)\{D\} = \{0\} \quad 4.12$$

The critical time step is also closely related to the time required for a stress wave to cross the smallest element dimension in the model given by

$$\Delta t = l\sqrt{\frac{\rho}{E}} \quad 4.13$$

where l is the characteristic element length, ρ is the density and E is the elastic modulus.

Maximum natural frequency of the system i.e. ω_{max}, is being determined since explicit integration fails whenever Δt is very large number or Δt is unnecessarily small leading to expensive calculations. The estimation of ω_{max} is provided by the Gerschgorin bound, which may be stated in the following form for lumped (diagonal) mass matrix,

$$\omega^2{}_{max} \le \max_i\left(\frac{1}{M_{ii}}\sum_{j=1}^{n}\left|K_{ij}\right|\right) \quad 4.14$$

where, i = 1, 2, 3,….,n, and n is the matrix order of number of degrees of freedom, K and M are the stiffness and mass matrices respectively.

Courant number is used measure the time step which is defined as,

$$C_n = \frac{\Delta t_{actual}}{\Delta t_{cr}} \tag{4.15}$$

where Δt_{cr} is the maximum time step consistent with the numerical stability.

4.4 Element Formulation and Characteristics

In this work, three modeling approaches have been employed to create the global and local PCB assembly models. The explicit models investigated includes smeared property model with conventional shell elements, Timoshenko beam element interconnect model with continuum shell element, node based explicit sub-model with the combination of Timoshenko-beam elements and Continuum solid element and also cohesive zone elements are investigated. The PCB in the global model has been modeled using shell elements because the thickness of the PCB is significantly smaller compared to its in-plane direction. In Abaqus, two types of shell elements are available: reduced integration conventional shell elements (S4R) and reduced integration continuum shell elements (SC8R) both are used to model the transient dynamic behavior which accounts for large strain. The concrete floor has been modeled using rigid element (R3D4) and its nodes are completely constrained so that there is no translation or rotation motion. In the first approach, smeared properties have been derived for all the individual components based on the volumetric averaging [Lall 2004, 2005] and have been modeled using reduced integration continuum elements (C3D8R). In the second approach, solder

interconnections have been modeled with two-node Timoshenko beam element (B31) and the various layers of electronic packages namely the substrate, die, mold compound have been modeled using reduced integration solid elements (C3D8R). In the third approach i.e. node based sub-modeling were further categorized with three different modeling technique, in all the case PCB was modeled using S4R elements, C3D8R elements were used to model the component layers such as substrate, mold compound and copper pad. In the first case all solder interconnects is modeled using B31 element. In the second case all four corner solder interconnects modeled as continuum solid elements (C3D8R) and remaining interconnect as Timoshenko beam elements. In the case three cohesive elements (COH3D) are incorporated between the copper pad and solder interconnect interface in all four corners of package and retaining rest of the interconnects as Timoshenko-beam element. In all 3 cases, Timoshenko-beam element (B31) has six degrees of freedom at each node including, three translational and three rotational degrees of freedom. Rotational degrees of freedom has been constrained to model the interconnect behavior.

Table 4.1: Explicit elements used in first modeling approach

Component	Element Type
PCB	S4R
CSP	C3D8R
Rigid Floor	R3D4
Base and Screws (JEDEC Drop)	C3D8R

Table 4.2: Explicit element used in second Modeling Approach

Component	Element Type
PCB	SC8R
CSP (Substrate, Mold)	C3D8R
Solder Interconnections	B31
Rigid Floor	R3D4
Base and Screws (JEDEC Drop)	C3D8R

Table 4.3: Explicit elements used in third modeling approach

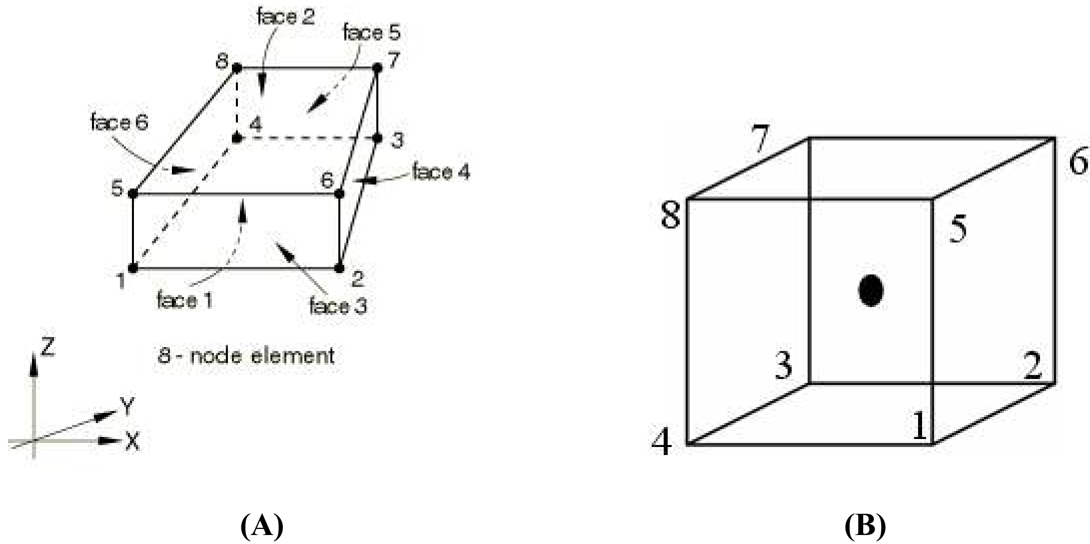
Component	Element Type
PCB	S4R, C3D8R
CSP (Substrate, Mold, copper pad)	C3D8R
4 Corner Solder Interconnections	C3D8R, COH3D8
Remaining Solder Interconnections	B31

Table 4.4: Characteristics of explicit elements

Element Type	Number of Nodes	Characteristics	Degrees of Freedom
C3D8R	8	First order, linear interpolation, hexahedral element with reduced integration and hourglass control.	Translational (1,2,3)
S4R	4	Quadrilateral shell element, linear interpolation with reduced integration and a large-strain formulation.	Translational and Rotational (1,2,3,4,5,6)
SC8R	8	Hexahedral, first-order interpolation, continuum shell element with reduced integration, finite membrane strain	Translational (1,2,3)
B31	2	Timoshenko beam, linear interpolation formulation.	Translational and Rotational (1,2,3,4,5,6)
R3D4	4	Rigid element	All the d.o.f are constrained

Characteristics of explicit elements types used are discussed in detail in the following literature.

1) C3D8R: Reduced Integrated Solid (Continuum) Element:



(A) **(B)**

Figure 4.4: (A) Node ordering and face numbering on elements (B) Reduced integration point at the centre of mass for output

Solid (continuum) elements are the standard volume element of Abaqus, it can be composed of single homogeneous material or can include several layers of different materials for the analysis of laminated composite solids and are more accurate if not distorted particularly for hexahedra. Solid elements allow for finite strains and rotations in large displacement analysis. C3D8R is a first order, eight node linear interpolation, hexahedral element with reduced integration and hourglass control. It has three translational degrees of freedom at each of its corner nodes. In first order hexahedral solid elements, the strain operator provides constant volumetric strain throughout the element. This constant strain prevents mesh locking when the material response is approximately in compressible. Reduced integration uses a lower-order integration to

form the element stiffness. Reduced integration reduces running time which is significant in three dimensional analyses. Reduced integration are also referred to as uniform strain or centroid strain elements with hourglass control. First order hexahedral solid elements are generally preferred over first order triangular and tetrahedral elements in stress analysis cases since the latter elements are extremely stiff and show slow convergence with mesh refinement. First-order elements are recommended when large strains or very high strain gradients are expected as in the case of impact. They are better suited to tackling complex contact conditions and severe element distortions. Higher order elements have higher frequencies than lower order elements and tend to produce noise when stress waves move across an FE mesh. Therefore, lower order elements are better than higher order elements at modeling a shock wave front.

2) S4R: Reduced Conventional Shell Element:

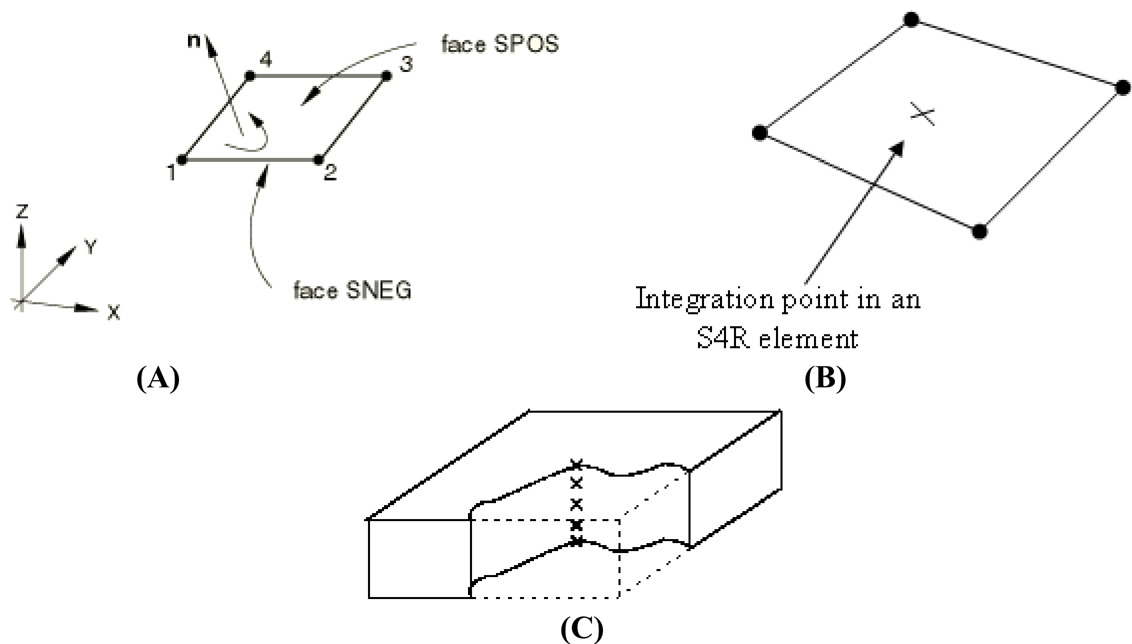


Figure 4.5: (A) Node ordering and face numbering on element (B) Numbering of integration points for output (C) Section Points through thickness of Shell element

S4R is a quadrilateral shell element, linear interpolation with reduced integration and a large-strain formulation. The conventional shell elements discretize the surface by defining the element's planar dimensions, its surface normal, and its initial curvature. Surface thickness is defined through section properties. Shell elements are used for printed circuit board since, the thickness dimension is significantly smaller than the other dimensions and the stresses and strains in the thickness direction are smaller than in the in-plane directions. The conventional shell-element is a four-node reduced integration element which accounts for large strains and large rotations. It has six degrees of freedom- 3 translational and 3 rotational degrees of freedom per node.

3) SC8R: Continuum Shell Elements

SC8R is a hexahedral, first-order interpolation, continuum shell element with reduced integration. Continuum shell elements (SC8R) resemble three-dimensional solid elements and discretize the entire three-dimensional body.

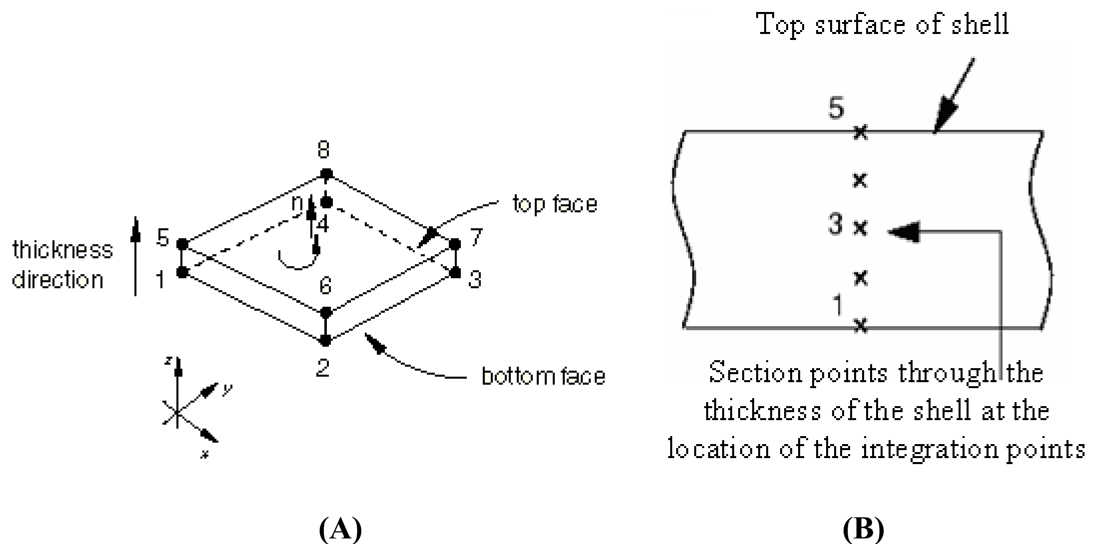
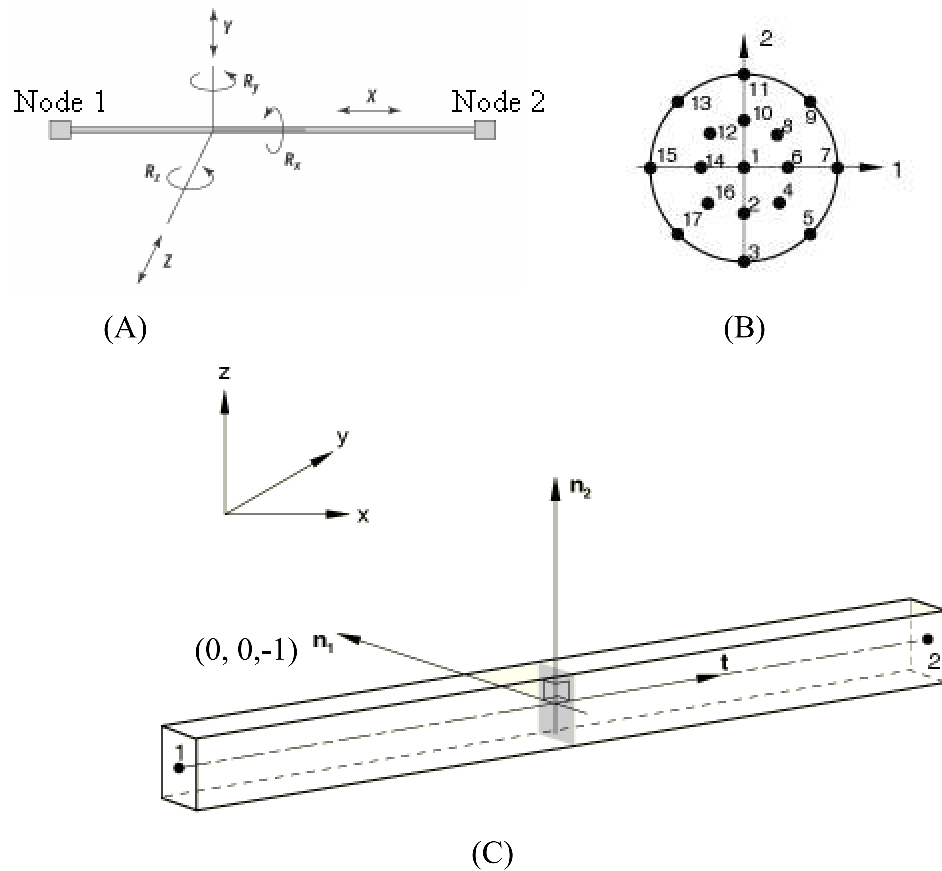


Figure 4.6: (A) Normal and Thickness Direction for Continuum Shell Elements (B) Section Points through Thickness of Shell Element

The continuum shell elements are formulated such that their kinematic and constitutive behavior is similar to conventional shell elements. The continuum shell element (SC8R) has three-translational degrees of freedom at each node and the element accounts for finite membrane strains and arbitrarily large rotations [Abaqus V6.7[a]]. Continuum shell elements provide a refined response through the thickness and are more accurate in modeling contact than conventional shell elements.

4) B31: Timoshenko-beam Element



(C)

Figure 4.7: (A) Timoshenko-beam element indicating the three translations and three rotations degrees of freedom (B) Integration point for beam in space (C) Beam element cross section orientation

Beam theory is the one-dimensional approximation of a three-dimensional continuum. The reduction in dimensionality is a direct result of slenderness assumption, that is, the dimensions of the cross-section are small compared to typical dimensions along the axis of the beam. Timoshenko (shear flexible) beam elements (B31) available in Abaqus are 3D beams in space. They use linear interpolation schemes and are useful in dynamic problems such as impact. They have six degrees of freedom at each node including, three translational degrees of freedom (1–3) and three rotational degrees of freedom (4–6). The beam is modeled with a circular cross-section with an equivalent radius so that it has the same mass as that of an actual solder interconnection. The rotary inertia is calculated from the cross-sectional geometry. The rotational degrees-of-freedom have been constrained to model interconnect behavior. The Timoshenko beam elements use a lumped mass formulation. The B31 elements allow for shear deformation, i.e., the cross-section may not necessarily remain normal to the beam axis [Abaqus V6.7[b]]. Shear deformation is useful for first-level interconnects, since it is anticipated that the shear flexibility may be important. Abaqus assumes that the transverse shear behavior of Timoshenko beams is linear elastic with fixed modulus and thus independent of the response of the beam section to axial stretch and bending. It is assumed throughout the simulation that, the radius of curvature of the beam is large compared to distances in the cross-section and that the beam cannot fold into a tight hinge. It is also assumed that the strain in the beam's cross-section is the same in any direction in the cross-section and throughout the section. For fine pitch solder interconnects, with very low stand-off heights, the constant cross-section assumption is fairly good approximation.

5) R3D4: Rigid element

R3D4 is a 4 node 3 dimensional rigid element. Rigid elements are used to define the surface of rigid bodies for contact. In this work, rigid element used to represent concrete floor where the test board is subject to impact. Figure 4.8 shows the rigid element normal definition.

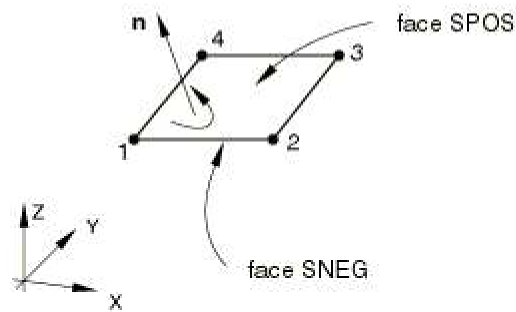


Figure 4.8: Rigid Element Normal Definition

CHAPTER 5

EXPLICIT FINITE ELEMENT MODELS FOR SHOCK-IMPACT SIMULATION

5.1 Introduction

Three varieties of explicit finite element models were developed to predict the transient dynamic behavior of printed circuit board assemblies which were subjected to 0°-horizontal drop according to JEDEC Standards, JESD22-B111. The models developed to simulate JEDEC drop included smeared property global model with conventional shell elements, Timoshenko-beam elements with continuum shell elements and node-based explicit sub-model. The board-level assembly comprised of 15 chip-array-ball-grid-array (CABGA) components mounted on one side of the printed circuit board. Figure 5.1 shows the typical architecture for the CABGA package investigated in this work.

5.2 Smeared Property Global Model with Conventional Shell Elements

Clech [1996, 1998] proposed smeared property approach which was based on the principle of volumetric averaging for the development of closed form models for solder interconnect subjected to thermal fatigue. This approach was successfully implemented by Lall [2007[b]] for the solder joint reliability in electronics under shock and the corresponding package used in this case was tape-array-ball-grid-array [TABGA].

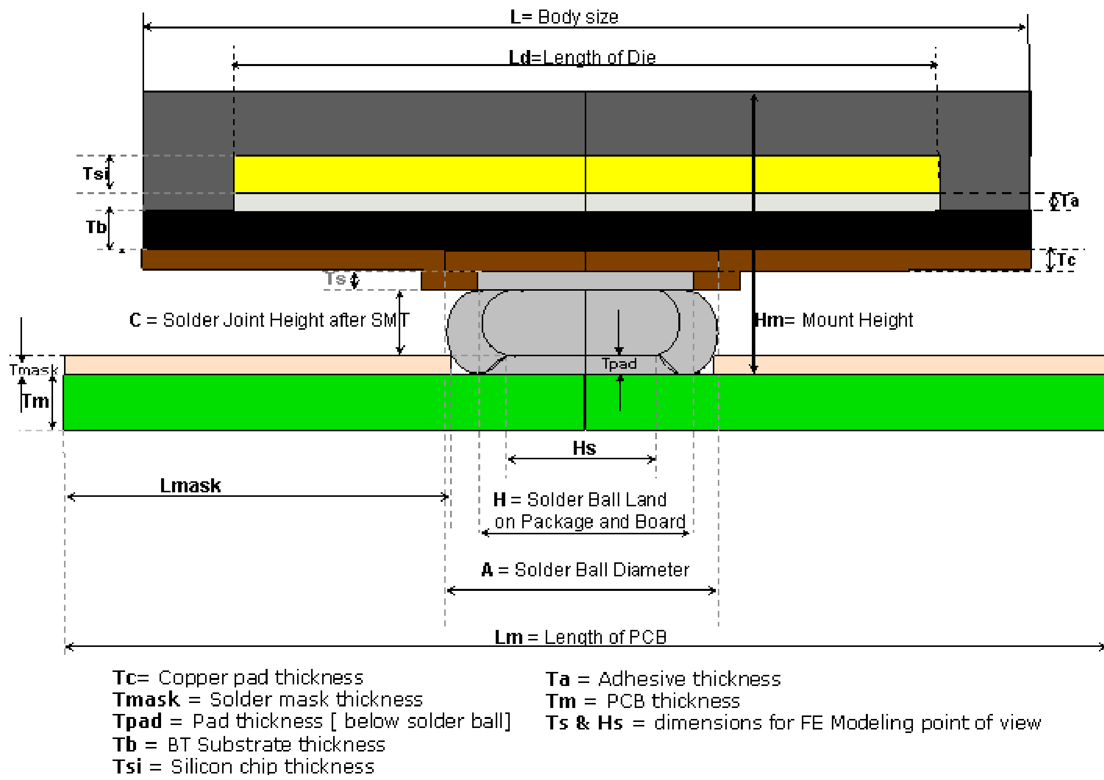


Figure 5.1: Typical Architecture for CABGA Package

Smeared property method considers various individual layers of the chip scale package (CSP) namely substrate, silicon die, die-attach, mold compound and solder interconnects

as homogeneous block of elements such that finite element model's package mass is identical to the original package. Printed circuit board is modeled using conventional shell elements (S4R) and smeared property elements are modeled using continuum solid elements (C3D8R). In order to simulate drop phenomenon, screws and base plate were modeled using C3D8R elements and concrete floor as rigid element R3D4. Figure 5.2 shows component modeled using continuum solid elements which have smeared properties and PCB using conventional shell elements. Table 5.1 provides summary of various element formulations adopted to create the component of the smeared model. It is necessary to calculate the equivalent material properties of the smeared element so that smeared elements closely match with the actual component. The method to obtain these parameters is explained below. Table 5.2 shows the masses, volumes and the equivalent layers considered for the calculation of smeared properties. The equivalent thickness of the each individual layer is calculated by considering each layer to have a 10mm square cross section which is actual size of each individual component. Table 5.3 shows the comparison of simulated mass and actual mass of all the components. It can be seen that the simulated weight of the PCB assembly closely approximates the actual weight. Table 5.4 shows the material properties used for individual layers of CABGA package. Table 5.5 shows material properties of smeared elements calculated with respect to lead-free solder alloys.

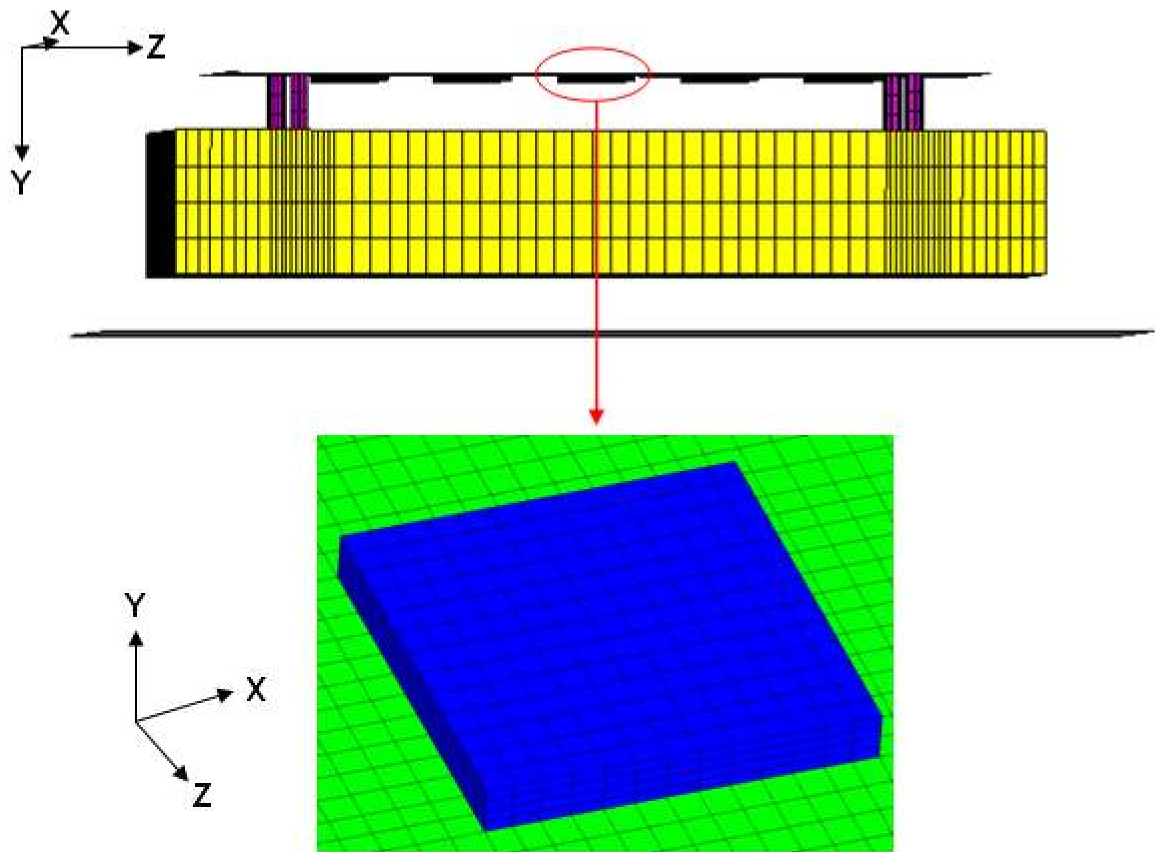


Figure 5.2: Component Modeled using Continuum Solid Elements which have Smeared Properties and PCB using Conventional Shell Elements

Table 5.1: Element types used in smeared property models

Component	Element Type
PCB	S4R
CABGA (Smeared Elements)	C3D8R
Rigid Floor	R3D4

Table 5.2: Dimension and masses of individual layers in the package

Component	Volume (m^3)	Mass(kg)	Equivalent Layer Thickness (m)
Solder (SAC 105)	2.12E-09	1.5573E-05	2.12E-05
Solder (SAC 305	2.12E-09	1.5709E-05	2.12E-05
Solder (Sn3.5Ag)	2.12E-09	1.5733E-05	2.12E-05
Die Attach	9.41E-10	2.07E-07	9.41E-06
Silicon Die	6.51E-09	1.5161E-05	6.51E-05
Mold Compound	8.76E-08	1.6644E-04	8.76E-04
Substrate	2.50E-08	3.5E-05	2.50E-04

Table 5.3: Comparison of Actual and Simulated Component Masses

Component	Actual Mass	Simulated Mass
PCB	22.8 gm	22.74 gm
Package (each)	0.2 gm	0.2 gm
Base Plate	11.52 Kg	12 Kg
Steel plates (weights)	46gm	46gm

Table 5.4: Material Properties for individual layers of CABGA package

Component	Elastic Modulus, E (Pa)	Poisson's Ratio (ν)	Density, ρ (kg/m^3)
Printed Circuit Board	16E+09	0.33	2243
SAC105	47E+09	0.34	7346
SAC305	51E+09	0.38	7410
Sn3.5Ag	33.6E+09	0.40	7421
Silicon Die	112.4E+09	0.28	2329
Copper Pad	129E+09	0.34	8900
Substrate	24.13E+09	0.33	1400
Mold Compound	15.5E+09	0.25	1970
Steel plates (Analysis with weights)	200E+09	0.29	7850

The nomenclature used in the equations used below is as follows:

υ_c – Poisson's Ratio of smeared element.
υ_k – Poisson's Ratio of individual components.
h_k – Layer Thickness of individual components.
E_c – Elastic Modulus of smeared element.
E_k – Elastic Modulus of individual components.
v_k – Volume of individual components.

Equation of Equivalent Poisson's Ratio

$$\upsilon_c = \frac{\sum_{k=1}^{n} \upsilon_k h_k}{\sum_{k=1}^{n} h_k}$$

Equation of Equivalent Elastic Modulus

$$\frac{E_c h_c^3}{12(1-\upsilon_c)} = \sum_{k=1}^{n} \frac{E_k h_k^3}{12(1-\upsilon_k)}$$

Equation of Equivalent Density

$$\rho_c = \frac{\sum_{k=1}^{n} \rho_k v_k}{\sum_{k=1}^{n} v_k}$$

Table 5.5: Material Properties of Smeared Elements

Solder Alloys	Poisson Ratio (υ_c)	Elastic Modulus (E_c) Pa	Density (ρ_c) Kg/ m^3
SAC105	0.2641	5.8513E+09	1917.398
SAC305	0.2648	5.8458E+09	1918.51
Sn3.5Ag	0.2629	6.1093E+09	1822.4

The printed circuit board assemblies were dropped from a height of 0.75 feet in the horizontal orientation for JEDEC drop in order to attain 1500G level. Computational time is saved by applying the near-impact velocity of the test assembly, which is a function of drop height as an initial condition to the various components of the PCB assembly. The relation is given by:

$$V = \sqrt{2gH}$$

where V is the impact velocity corresponding to drop height H.

For JEDEC drop, the initial velocity corresponding to a height of 0.75 feet i.e. 0.2286 meters is given by:

$$V = \sqrt{2 \times 9.81 \times 0.2286}$$

$$V = 2.1178 m/s.$$

A reference node was placed behind the rigid floor (R3D4) for application of constraints such that all the degrees of freedom of that node were constrained. Node to surface contact definition was specified between the impacting bottom surface of the base and the rigid floor for JEDEC drop. The impact event was modeled for the total time duration of 20ms. Time history of the strain across various locations on PCB assembly was output to correlate with the DIC data. Figure 5.5 shows the package strain correlation between DIC and FEM on pristine SAC305 test board during 0° JEDEC-Drop. Strain correlation for the test board is shown for the first 20 ms after impact since maximum strain occurs within this period. Figure 5.6 shows the correlation between transient mode shapes obtained from DIC and FEM at time interval 1.5ms and 3.5 ms after impact. Prediction of the transient mode shape from simulation shows good correlation with those obtained from DIC.

5.3 Timoshenko-beam Element with Continuum Shell Elements Global Model

In this modeling technique, continuum shell elements (SC8R) are used to model the printed circuit board. The continuum shell elements resemble three-dimensional solid elements and discretize the entire three-dimensional body. Timoshenko-beam elements (B31) were used to model each solder interconnects. Beam elements are modeled with a circular cross-section with an equivalent radius so that it has the same mass and volume as that of an actual solder interconnection as shown below:

$$\text{Volume of single solder joint} = 3.878 \times 10^{-11}\,\text{m}^3$$
$$\text{Height of solder joint (h)} = 0.3 \times 10^{-3}\ \text{m}$$

Considering the beam to be cylindrical in volume, we have:

$$\text{Volume of single solder beam} = \pi r^2 h$$
$$\text{Therefore, } \pi r^2 h = 3.878 \times 10^{-11}\,\text{m}^3$$
$$\text{Radius} = r = 0.20248 \times 10^{-3}\ \text{m}$$

In this modeling technique all the other individual layers of the package such as the substrate and mold compound have been modeled in detail using first order reduced integration continuum solid elements (C3D8R). Die-attach is not considered in this case in order to save computational time due to its negligible thickness which affects the critical time step. The concrete floor was modeled with R3D4 elements. Element types used to model the various components of this model are listed in Table 5.6. The Table 5.7 shows the simulated weight of the various components of the continuum shell-beam model and the actual weights. It can be seen that the simulated weight of the PCB assembly closely approximates the actual weight. Figure 5.3 show the zoomed view of one of the packages with the PCB modeled using SC8R elements and its cross-sectional view with all the individual layers.

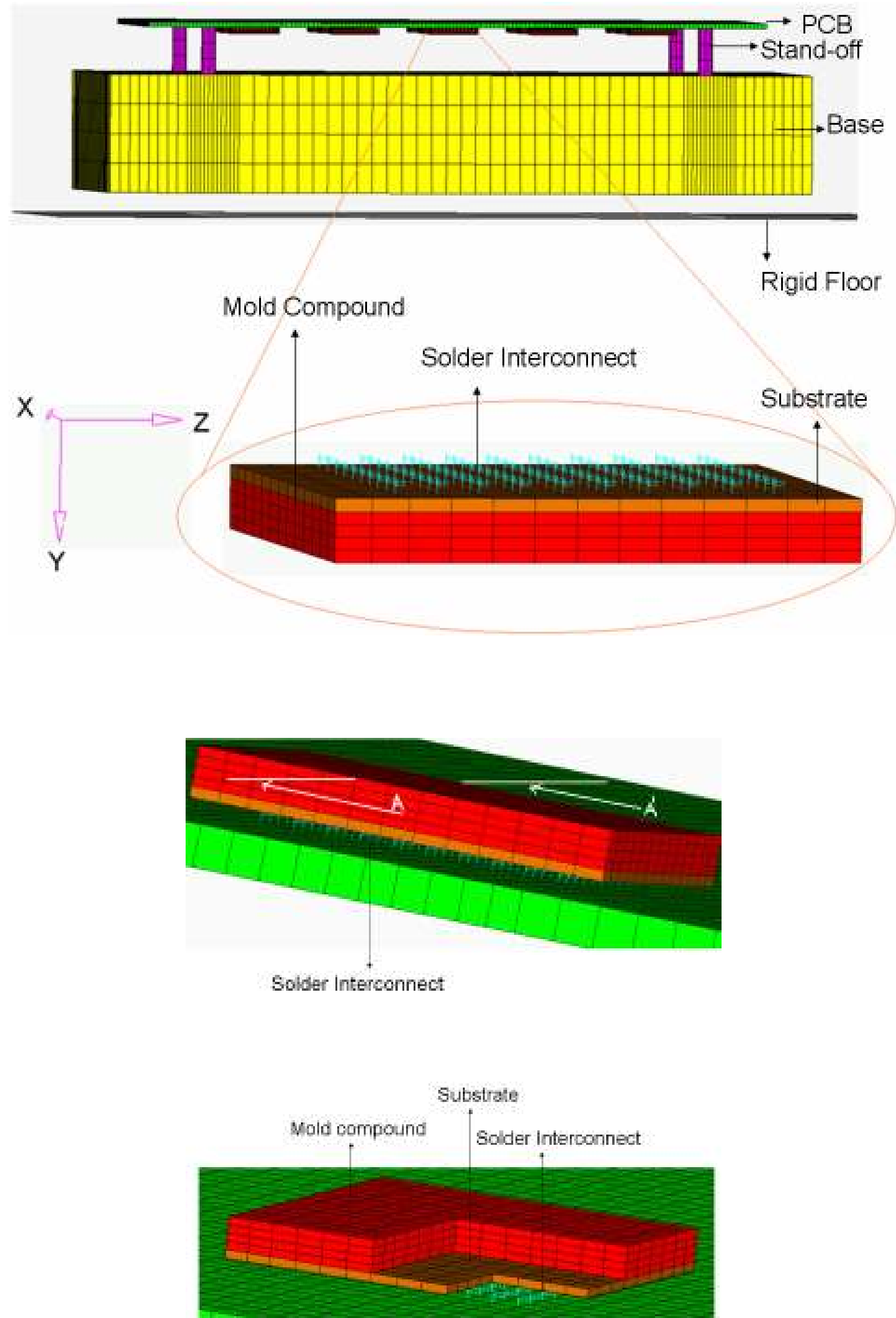


Figure 5.3: Printed Circuit Board Assembly with Timoshenko-Beam Elements and Continuum Shell Elements.

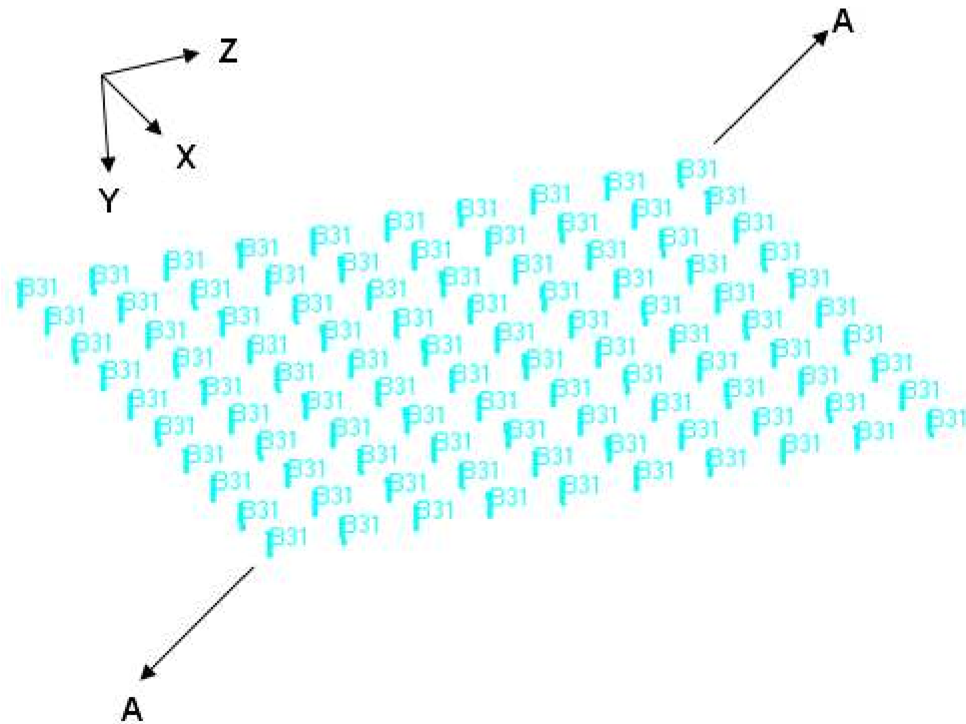


Figure 5.4: Solder Interconnection Layout Modeled Using Timoshenko-Beam Elements.

Figure 5.4 shows the layout of the solder interconnections modeled using the Timoshenko beam elements (B31). Drop simulation of the PCB assembly was carried out from a height of 0.75 feet in the horizontal orientation. To save computational time, initial velocities of 2.1178m/s corresponding to heights of 0.75 feet were applied to the nodes of all the components in the assembly for JEDEC drop simulation. Timoshenko beam elements rotational degrees of freedom were constrained to model interconnect behavior. Node to surface contact has been implemented between the impacting surface of the base and the reference node of the rigid floor which was constrained in all degrees of freedom for the JEDEC drop. The impact event was modeled for the total time

duration of 20 milliseconds. PCB strain histories at various component locations were output to correlate with the DIC data. Figure 5.5 shows the package strain correlation between DIC and FEM on pristine SAC105 test board during 0° JEDEC-Drop. Validated models that have been correlated with the DIC transient strain response of the printed circuit assemblies, have been used for second-level interconnect strain history prediction. Figure 5.7 shows the prediction of the transient strain history at the package corner interconnects for different solder alloys.

Table 5.6: Element types used in Continuum Shell-Beam model.

Component	Element Type
PCB	SC8R
Solder Interconnections	B31
Substrate	C3D8R
Mold Compound	C3D8R
Rigid Floor	R3D4
Connecting Screws (JEDEC Drop)	C3D8R
Steel Base (JEDEC Drop)	C3D8R

Table 5.7: Comparison of Actual and Simulated Component Masses using Continuum Shell-Beam Model.

Component	Actual Mass	Simulated Mass
PCB	22.8 gm	22.74 gm
Package	0.2 gm	0.2 gm
Base Plate	11.52 Kg	12 Kg

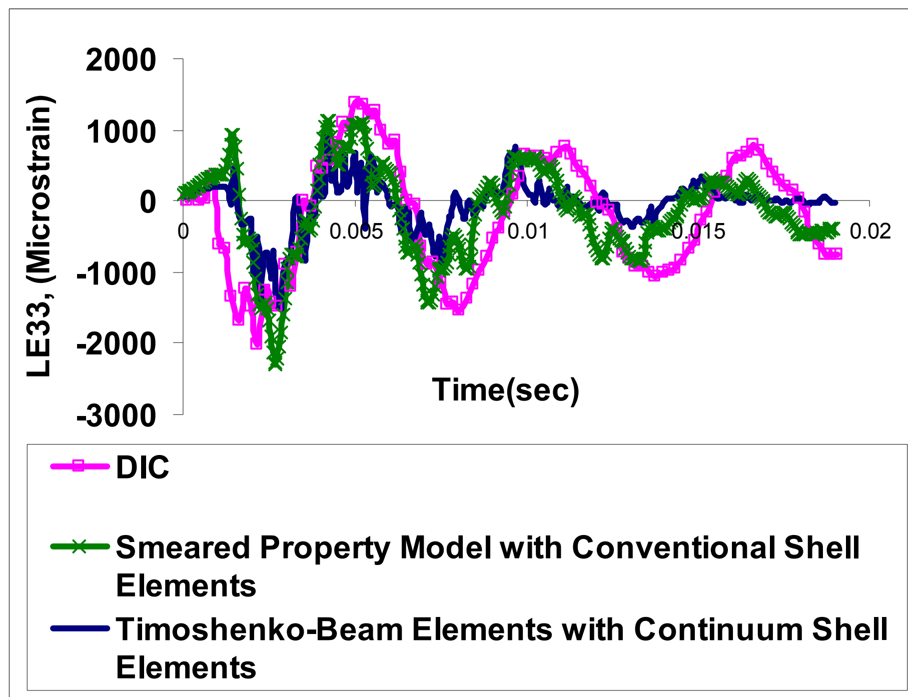
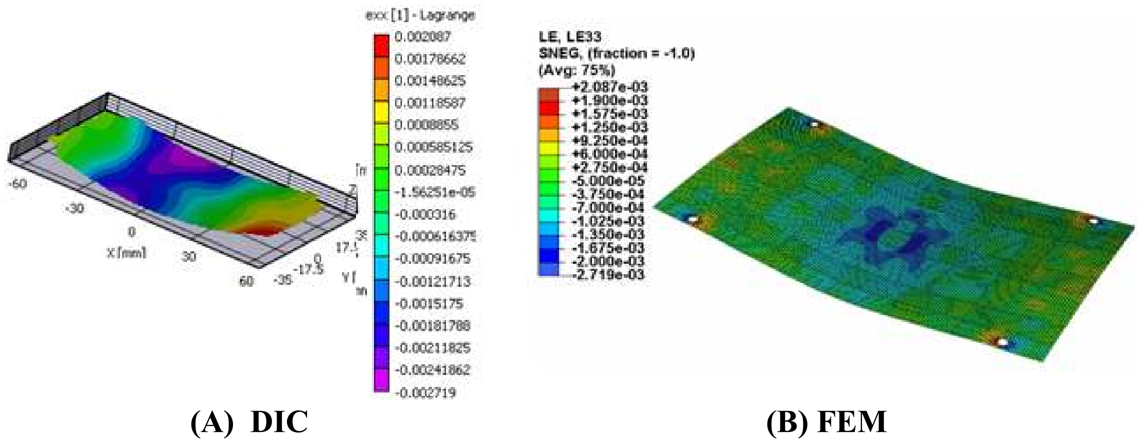
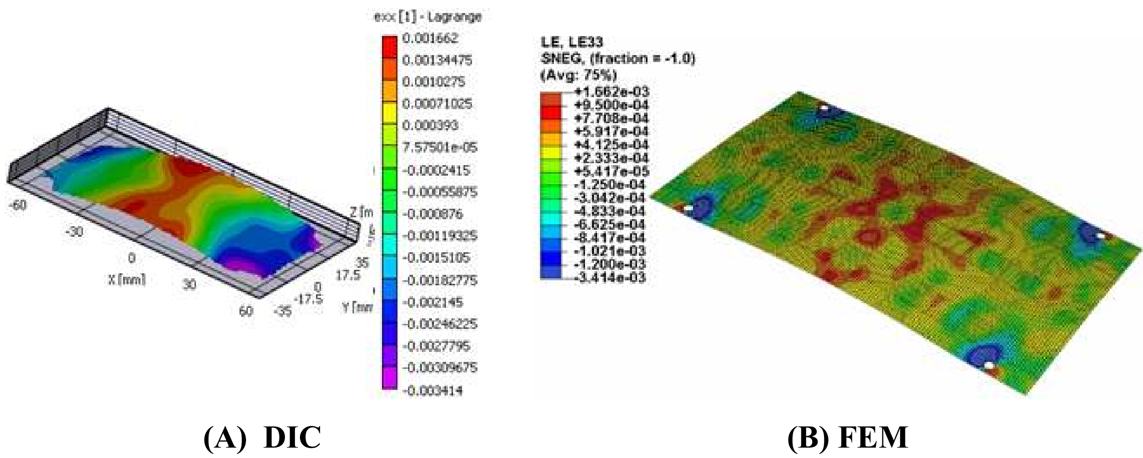


Figure 5.5: Package Strain correlation between DIC and FEM on Pristine SAC105 Test Board during 0° JEDEC-Drop



(A) DIC **(B) FEM**

Time Interval = 1.5milliseconds



(A) DIC **(B) FEM**

Time Interval = 3.5milliseconds

Figure 5.6: Correlation of DIC and FEM full field 3D Strain Contour of the Test Board (JEDEC 0° Drop)

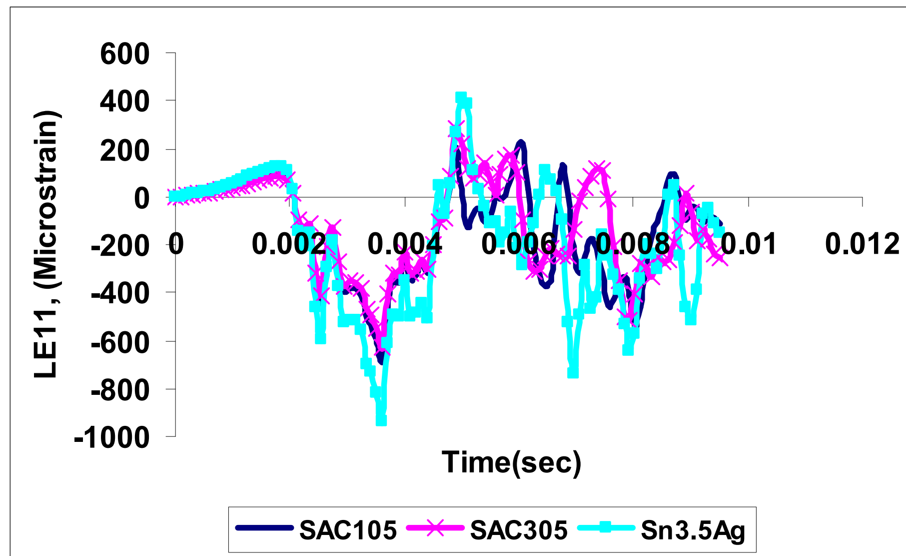


Figure 5.7: Prediction of Transient Strain History at the Package Corner Interconnect of Package 13 for different Solder Alloys during 0°JEDEC-drop.

5.4 Node based Explicit Sub-model

Node-based sub-modeling involves interpolation of results obtained from global model onto the nodes on the appropriate parts of the boundary of the submodel. Inputs at the boundary of the local region are defined by the solution for the global model. The attachment nodes are the driven nodes which determine the solution in the submodel. Previously, various shock-impact modeling techniques have been developed to reduce the computational time required for simulation including equivalent layer models for solder interconnect [Gu 2004, 2005, lall 2004, 2006a,b] solid-to-solid submodeling technique using half PCB board [Zhu 2001], shell-to-solid submodeling using beam-shell-based quarter symmetry models [Ren 2003, 2004], shell-to-solid sub-modeling without any assumption of symmetry [Lall 2007a].

In this work, the global output of the experiment data has been used to develop boundary conditions for the sub-modeling of the individual packages in the printed circuit assembly. The approach has been used to develop correlation of the printed circuit assembly and package strains to solder interconnect strains. Digital Image Correlation has been used to extract velocity components at discrete speckle patterned location on test board. Transient velocity histories on the package and in the package vicinity on the printed circuit board have been measured during the shock impact. Measurements show that the in-plane velocity components are significantly smaller compared to out-of-plane velocity component since test board is rigidly fixed at four corners. Figure 5.8 shows speckle patterned test board with the region of interest being package 3 identified with red square. Relative velocity vectors have been extracted at the specific locations in the vicinity of package 3 shown in Figure 5.8. Figure 5.9 shows relative velocity vectors.

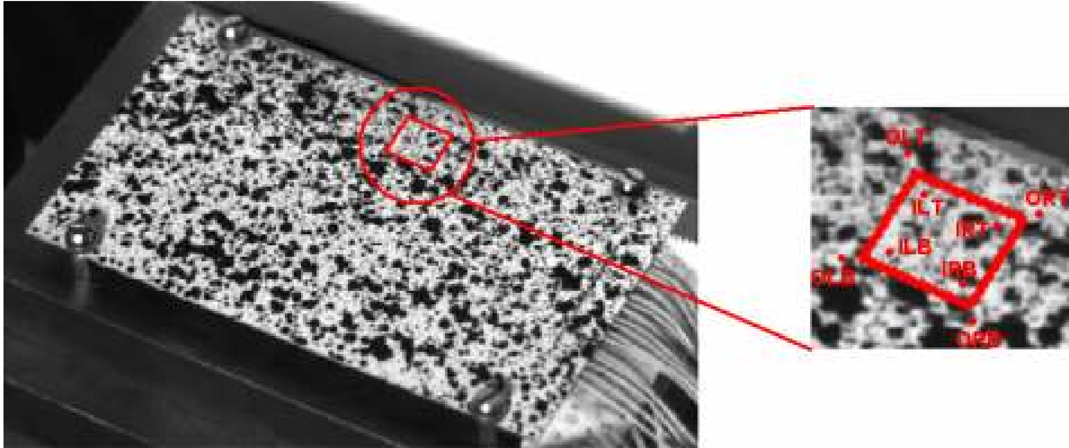


Figure 5.8: SAC105 test board indicating discrete locations where velocity vectors are extracted using DIC.

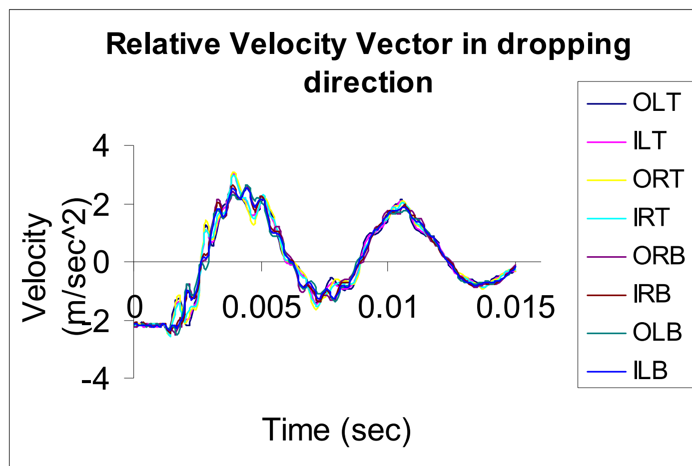


Figure 5.9: Relative Velocity Vectors Extracted from DIC at Discrete Locations on Package 3 SAC105 Test Board.

extracted from DIC at discrete locations of SAC105 test board. Specific locations have been identified by OLT: outer left top; ILT: inner left top; ORT: outer right top; IRT: inner right top; ORB: outer right bottom; IRB: inner right bottom; OLB: outer left bottom. Validity of the model prediction of solder interconnect strain has been established by correlating the model predictions of the package strains and printed circuit board strain with experimental strain histories. The extracted velocity vector is implemented in finite element model as follows:

Displacement= $U(r) = U(r_o) = U_o = (u_o, v_o, w_o)^T$ 5.1

Velocity (V) = $\dfrac{dU(r)}{dt}$ 5.2

The velocity (V) is compute using Central difference method,

$$\dot{d}^{n+(1/2)} = v^{n+(1/2)} = \frac{d^{n+1} - d^{n}}{t^{n+1} - t^{n}} = \frac{1}{\Delta t^{n+(1/2)}}(d^{n+1} - d^{n}) \qquad 5.3$$

Where, t^n and $d^n = d(t^n)$ are the time and displacement respectively at time step n.

The acceleration has been computed as follows,

$$\ddot{d}^{n} = a^{n} = \left(\frac{v^{n+(1/2)} - v^{n-(1/2)}}{t^{n+(1/2)} - t^{n-(1/2)}}\right) \qquad 5.4$$

Explicit finite element models have been developed to model the drop impact of the test boards. Prediction of the response of the printed circuit board under 0°-JEDEC drop orientations has been simulated and experimental measurements obtained from DIC have been correlated with the simulation results. Model Prediction have been used to determine the interconnect strain histories. Equation 5.4 is used in equation of motion to solve for $\{D\}_{n+1}$. Figure 5.10 explains Node-based explicit sub-modeling technique.

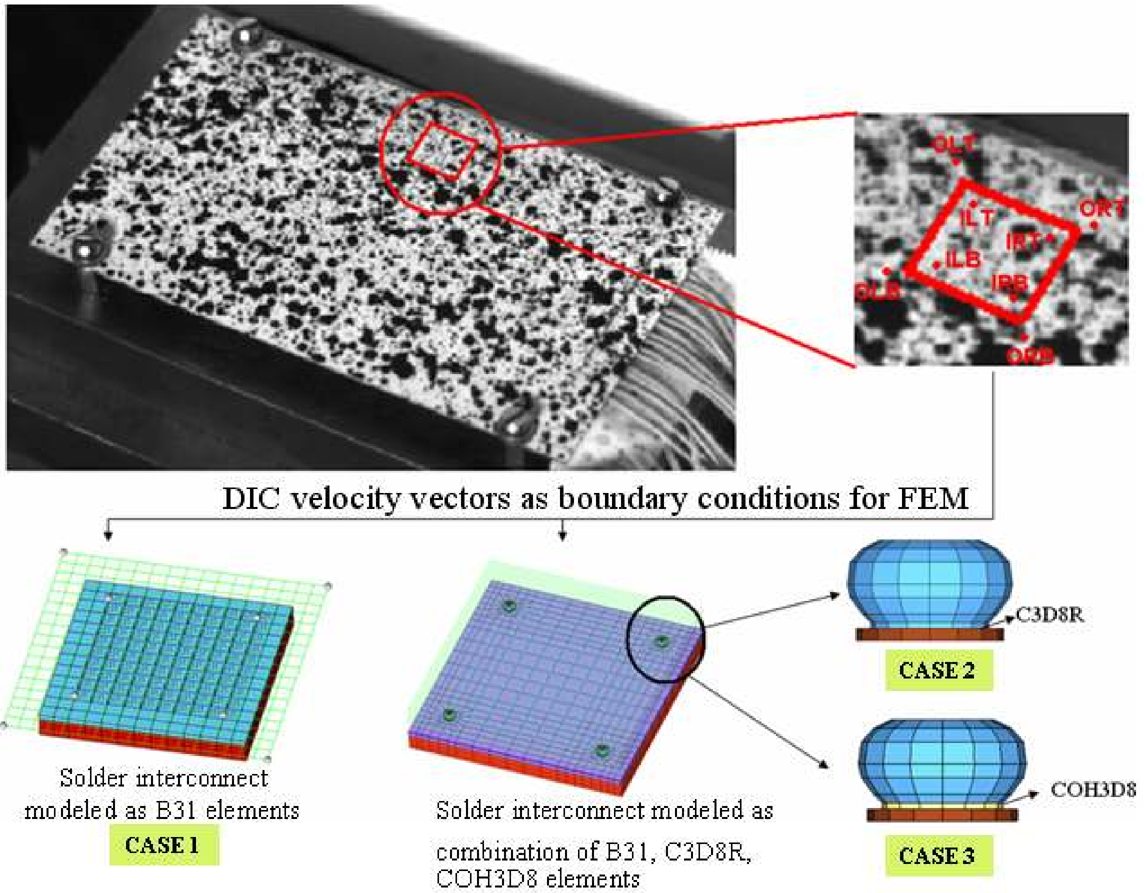


Figure 5.10: Node-based Explicit Sub-modeling technique.

Computational time of the transient dynamic event is reduced by incorporating reduced integration elements in the analysis because these element types use fewer integration points to form the element stiffness matrices in other words internal load vector scales with number of integration points. Lower order elements have been implemented since they perform better when the strain is large or very high strain gradient would be expected during drop impact events. Figure 5.11, Figure 5.12 and Figure 5.13 shows three explicit models used to simulate drop phenomenon. Printed circuit board is modeled using shell elements. Both the types of shell elements have been used to model PCB which includes conventional shell elements and continuum shell element. Three dimensional continuum elements C3D8R are used to model the components layers such as substrate, mold compound and copper pad. Three cases have been formulated with incrementally increasing complexity to model competing failure modes of solder-package pad failure, solder-board pad failure and solder interconnect failure. In the first case all solder interconnects is modeled using three-dimensional, linear, Timoshenko-beam element (B31) as sown in Figure 5.11 . In the second case all four corner solder interconnects modeled as Continuum Solid elements and remaining interconnect as Timoshenko beam elements as shown in Figure 5.12. In the case three cohesive elements are incorporated between the copper pad and solder interconnect interface in all four corners of package and retaining rest of the interconnects as Timoshenko-beam elements as shown in Figure 5.13. In all 3 cases B31 element has six d.o.f at each node including, three translational and three rotational degrees of freedom. Rotational degrees of freedom has been constrained to model the interconnect behavior. Table 5.8 shows package components modeled.

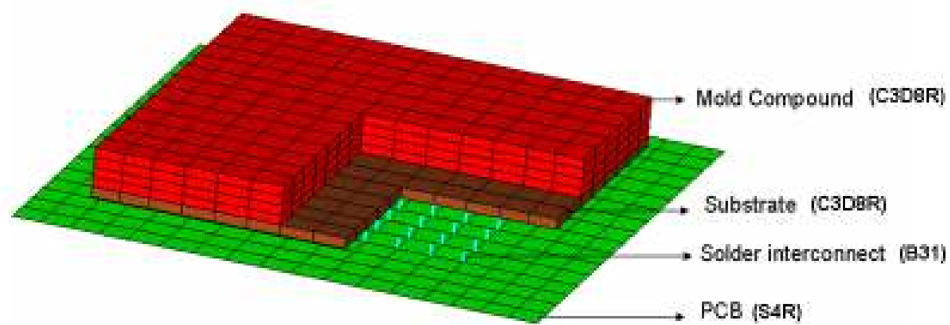


Figure 5.11: PCB with Timoshenko-Beam and Conventional Shell-Elements (*Case 1*).

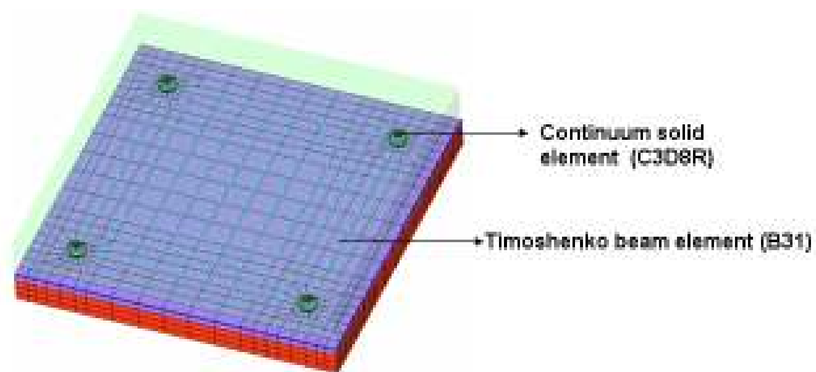


Figure 5.12: PCB with corner solder interconnects modeled as Continuum Solid element and remaining interconnect as Timoshenko beam elements (*Case 2*).

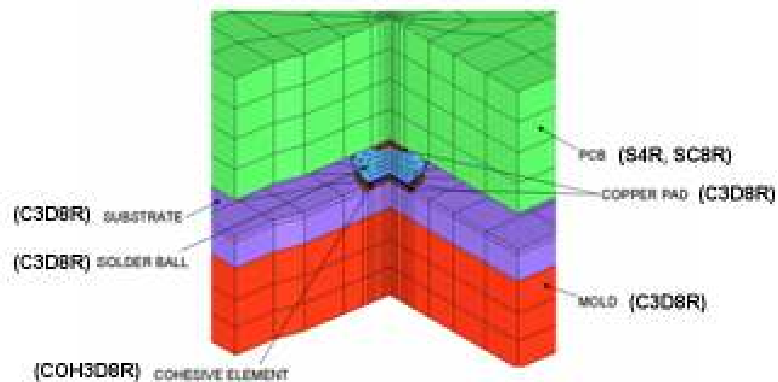


Figure 5.13: Cohesive Element incorporated between the Copper Pad and Solder Interconnect interface in all four corners of the package retaining rest of the Solder Interconnects as Timoshenko Beam Elements (*Case 3*).

Table 5.8: Components modeled in the sub-model and corresponding element types

Components	Element Types
PCB	S4R, SC8R, C3D8R
Substrate, Mold, Copper Pad	C3D8R
4 Corner Solder Interconnect	C3D8R, COH3D8
Remaining Solder Interconnects	B31

Correlation between transient dynamic package and printed circuit board strain histories from DIC and simulation have been compared at particular package on board side and prediction of in-plane solder strain for the JEDEC 0° drop from node based modeling approach. Figure 5.14 shows the location of corner interconnects in the finite element model. Figure 5.15 show the strain correlation at all four corners of particular package on PCB side for first 15 milliseconds after impact since maximum strain occurs in this period. In addition, the correlation of transient mode-shapes during JEDEC 0° drop at different time intervals has also been shown.

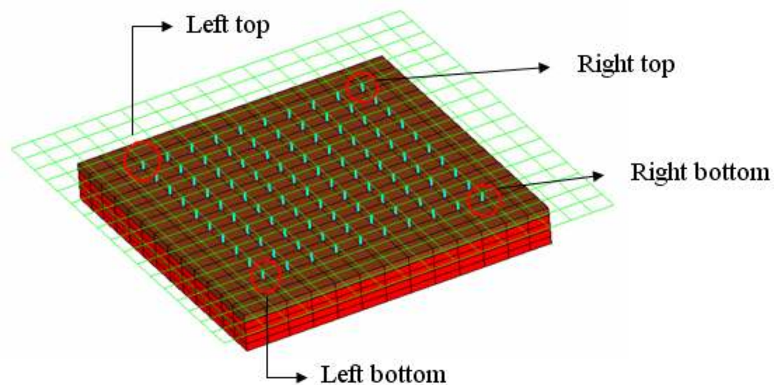
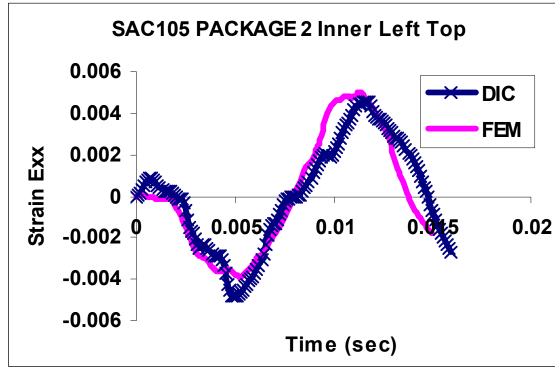
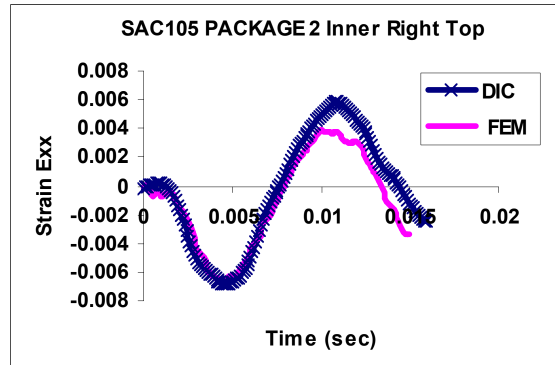
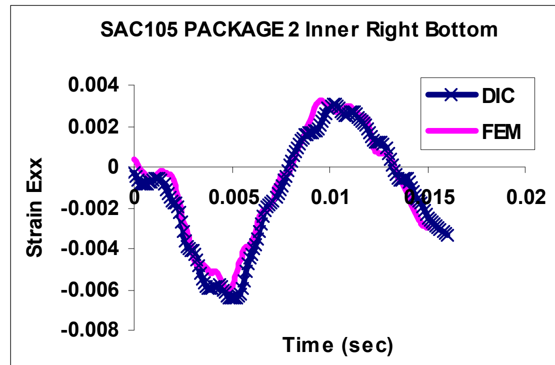


Figure 5.14: Location of corner solder interconnects in FEM.







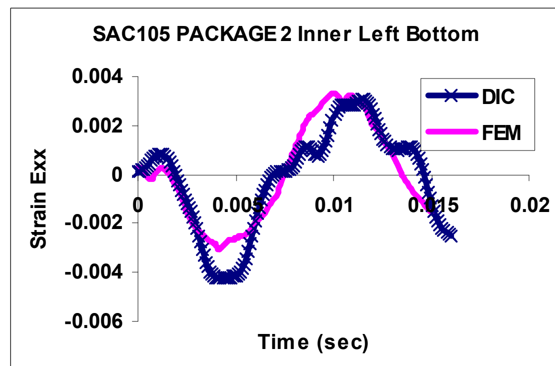


Figure 5.15: SAC105 *WEIGHTS ADDED* Transient Strain correlation between DIC and FEM

Once the strain correlation between DIC and simulation on board side has been demonstrated is possible to predict transient history for entire array of solder interconnect. Corner interconnects undergo maximum strain when PCB is subjected to drop and shock. Figure 5.16 shows the prediction of transient strain history in longitudinal direction at four package corner interconnects for package 2 of SAC105 thermally aged test board (*with weights to the printed circuit board assembly*). Solder interconnect strains have been used for developing fatigue constants for lead-free solder interconnects in drop and shock environment. Figure 5.17 shows the transient mode shapes obtained from digital image correlation and simulation at time intervals 1.6ms and 4.8ms after impact. Predicted transient mode shape correlates well with simulation.

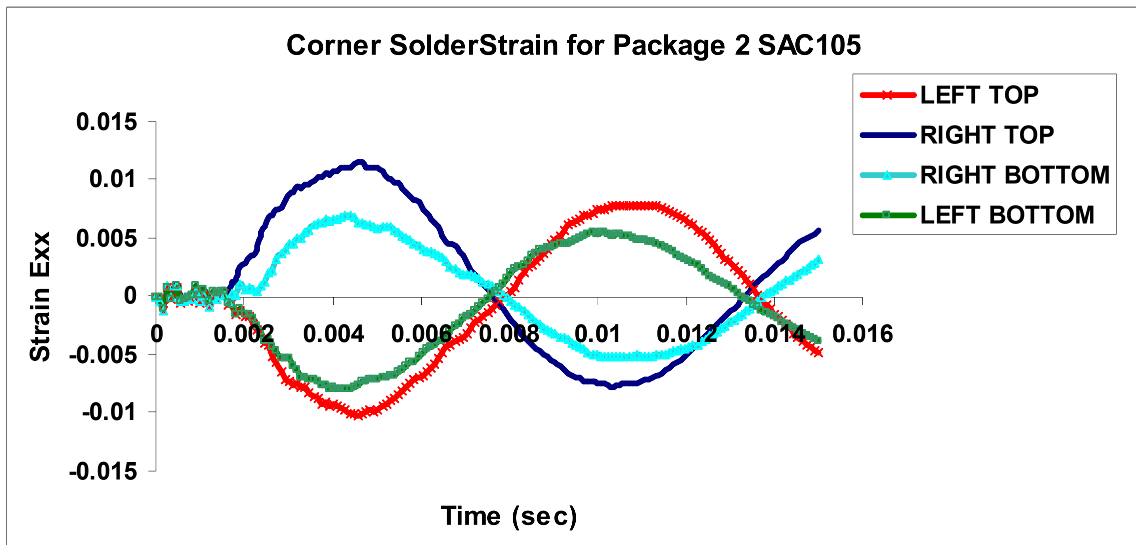
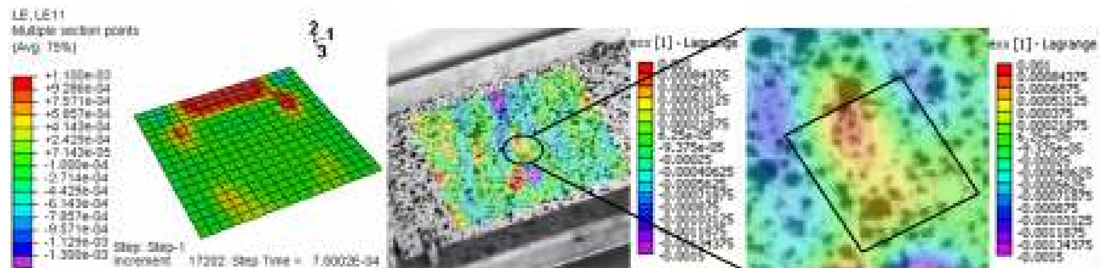
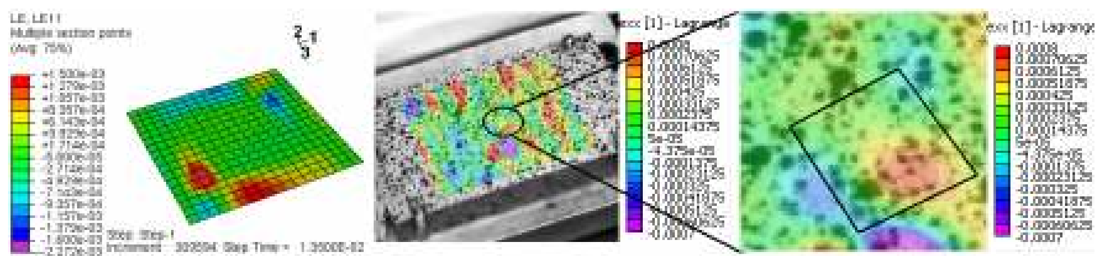


Figure 5.16: Prediction of Corner Solder Strain History for Package 2 SAC105



Time interval = 0.75 ms after impact



Time interval = 4.8 ms after impact

Figure 5.17: Contour Comparison between DIC and Simulation for SAC105 Pristine centre package (Package 8/Centre package) JEDEC 0° Drop orientation.

5.5 Cohesive Zone Failure Model

During high strain rates events such as impact loading, brittle interfacial fracture failure at solder joint copper pad interface on components side or on board side is commonly observed in electronic products [Tee 2003, Chai 2005]. It is found that the crack propagation during interfacial failure is in or near inter-metallic compound (IMC) layer formed between the regions of solder alloy and copper pad. Fracture strength of brittle IMC decreases with increase in strain rate where as bulk solder fracture strength is proportional to strain rate. Events such as drop and shock causes high stress to build up at the IMC region resulting interconnect to become weakest link in the entire structure and the interface failure occurs [Bansal 2005, Date 2004, Wong 2005, Newman 2005, Harada 2003, Lall 2005].

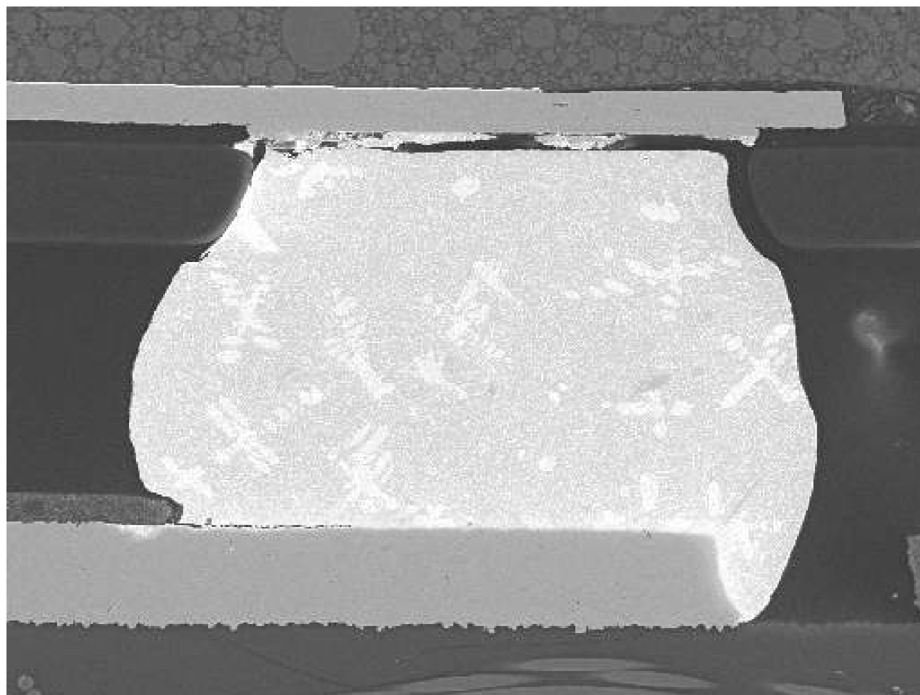


Figure 5.18: Failure mechanism showing failed solder joint at package interface [Lall 2004]

In the present study, cohesive zone modeling methodology has been incorporated to predict life of the lead-free alloy system in drop and shock environment. A thin layer of cohesive zone elements with thickness equivalent to 2.0e-05m has been modeled at the solder ball and copper pad interface at the component side. Cohesive element model the initial loading, initial damage and propagation of the crack at the layer between solder ball and the copper pad leading to eventual failure. When damage occurs, cohesive zone elements loose their stiffness completely at the failure and the continuum elements get disconnected showing failure of the solder joint. Mechanical constitutive behavior of the cohesive element is defined by using a constitutive model based on traction versus separation relationship suitable since interface thickness is very small. Traction versus separation relationship is derived from fracture mechanics to describe the mechanical integrity of the interface. Needleman's model [1987] used nonlinear traction–separation relationship. In this present work, linear traction-separation relationship is assumed for simplicity as shown in Figure 5.21.

Needleman Interface Model:

Needleman model [1987] comprised of nonlinear response of the cohesive zone incorporated at the interface in terms of traction-separation relationship. Needleman model has been successfully implemented by Towashiraporn et. al. [Towashiraporn 2006] where cohesive zone is used to describe the mechanical integrity of the interface near crack tip. Darveaux et. al. [Darveaux 2006] obtained similar response during high strain rate tensile testing of solder joints showing that the tensile stress value reaching the

maximum value at the point of the interface and decreases since there is no resistance to the force applied due to de-cohesion of solder joint and copper pad interface. Lall et. al. [Lall 2007b] incorporated cohesive elements in the local model at the solder joint-copper pad interface at both the PCB and component side in order to detect failure initiation and propagation leading to IMC brittle failure in PCB assemblies subjected to drop impact.

In Needleman's modeling approach attention is directed towards an interface supporting a nominal traction field T (force/unit reference area) which includes both normal and shearing components. Two material points A and B initially on opposite sides of the interface are considered and the interfacial traction is taken to depend only on the displacement difference across the interface, $\Delta U_{AB.}$ At each points of the interface we define,

$$u_n = n.\Delta u_{AB} \qquad 5.5$$

$$u_t = t.\Delta u_{AB} \qquad 5.6$$

$$u_b = b.\Delta u_{AB} \qquad 5.7$$

and

$$T_n = n.T \qquad 5.8$$

$$T_t = t.T \qquad 5.9$$

$$T_b = b.T \qquad 5.10$$

In equations (5.5) to (5.10), n, t, b form right-hand co-ordinate systems chosen so that positive u_n corresponds to increasing interfacial separation and negative u_n corresponds to decreasing interfacial separation.

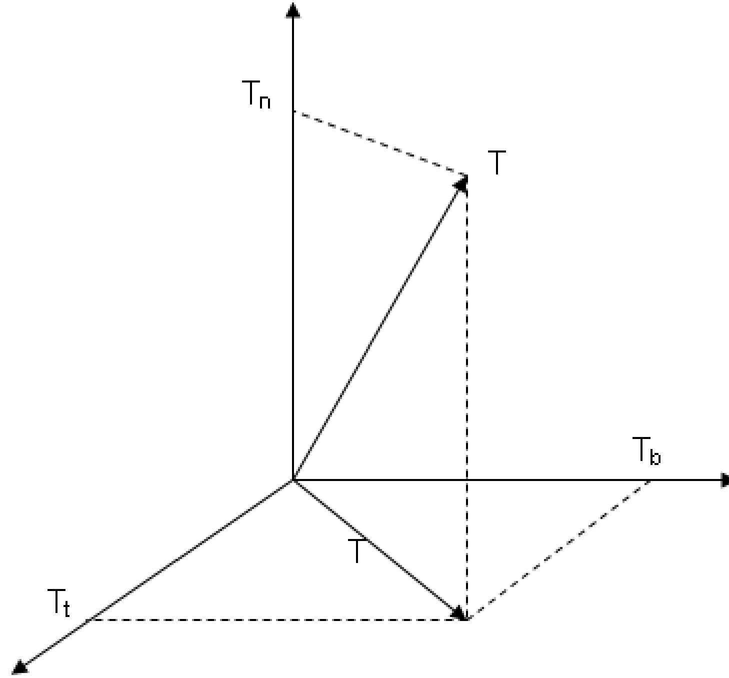


Figure 5.19: Traction components at the interface.

The mechanical response of the interface is described through a constitutive relationship that gives the dependence of the tractions T_n, T_t and T_b on U_n, U_t and U_b. Here, this response is specified in terms of potential $\phi(u_n, u_t, u_b)$ where:

$$\phi(u_n, u_t, u_b) = -\int_0^u [T_n du_n + T_t du_t + T_b du_b] \qquad 5.11$$

As the interface separates, the magnitude of the traction increases achieves a maximum and ultimately falls to zero when complete separation occurs. Relative shearing across the interface leads to the development of shear traction but the dependence of the shear traction on U_t and U_b is taken to be linear. The specific potential function used for $u_n \leq \delta$, is given by

$$\phi(u_n,u_t,u_b)=\frac{27}{4}\sigma_{max}\delta\left\{\begin{array}{l}\frac{1}{2}\left(\frac{u_n}{\delta}\right)^2\left[1-\frac{4}{3}\left(\frac{u_n}{\delta}\right)+\frac{1}{2}\left(\frac{u_n}{\delta}\right)^2\right]\\+\frac{1}{2}\alpha\left(\frac{u_t}{\delta}\right)^2\left[1-2\left(\frac{u_n}{\delta}\right)+\left(\frac{u_n}{\delta}\right)^2\right]+\\\frac{1}{2}\alpha\left(\frac{u_b}{\delta}\right)^2\left[1-2\left(\frac{u_n}{\delta}\right)+\left(\frac{u_n}{\delta}\right)^2\right]\end{array}\right\} \qquad 5.12$$

Where: σ_{max} = maximum traction carried by the interface undergoing a purely normal separation that is $u_t \equiv 0$ and $u_b \equiv 0$, δ = characteristic length, α = ratio of shear stiffness of interface to the normal stiffness of interface. When $u_n > \delta$, $\phi \equiv \phi_{separation}$ where $\phi_{separation}$ is the work of separation. The intention for choosing a potential form (5.12) is to obtain response of the type shown in Figure 5.20, where normal traction T_n is plotted as a function of u_n with $u_t \equiv u_b \equiv 0$.

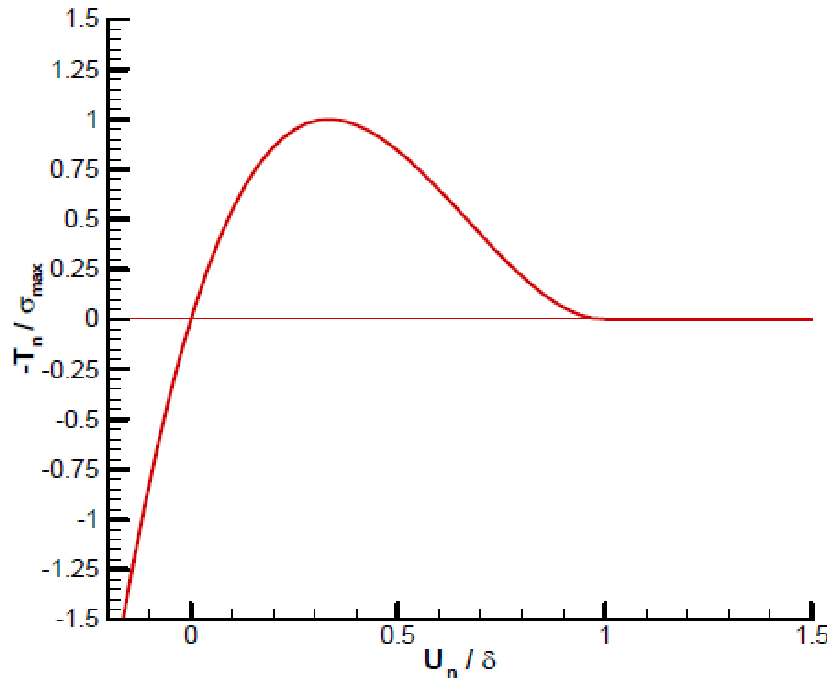


Figure 5.20: Normal traction across the interface as a function of u_n with $u_t \equiv u_b \equiv 0$

The interfacial traction are obtained by differentiating equation (5.12) to give

$$T_n = -\frac{27}{4}\sigma_{max}\left\{\begin{array}{l}\left(\frac{u_n}{\delta}\right)\left[1-2\left(\frac{u_n}{\delta}\right)+\left(\frac{u_n}{\delta}\right)^2\right]+ \\ \alpha\left(\frac{u_t}{\delta}\right)^2\left[\left(\frac{u_n}{\delta}\right)-1\right]+\alpha\left(\frac{u_b}{\delta}\right)^2\left[\left(\frac{u_n}{\delta}\right)-1\right]\end{array}\right\} \quad 5.13$$

$$T_t = -\frac{27}{4}\sigma_{max}\left\{\alpha\left(\frac{u_t}{\delta}\right)\left[1-2\left(\frac{u_n}{\delta}\right)+\left(\frac{u_n}{\delta}\right)^2\right]\right\} \quad 5.14$$

$$T_b = -\frac{27}{4}\sigma_{max}\left\{\alpha\left(\frac{u_b}{\delta}\right)\left[1-2\left(\frac{u_n}{\delta}\right)+\left(\frac{u_n}{\delta}\right)^2\right]\right\} \quad 5.15$$

for $u_n \leq \delta$ and

$T_n \equiv T_t \equiv T_b \equiv 0$ when $u_n > \delta$.

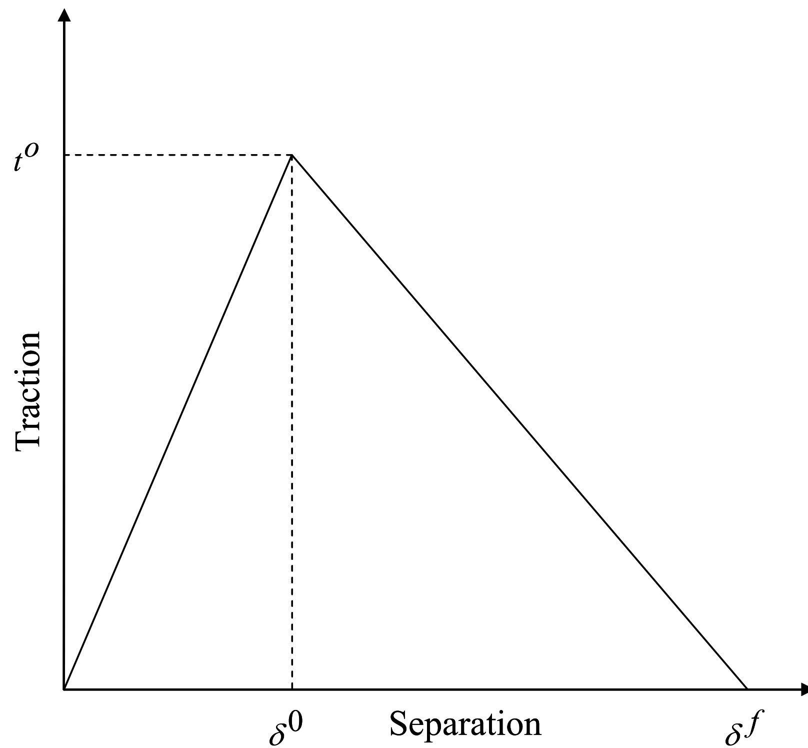


Figure 5.21: Linear Traction-Separation response for cohesive elements [Abaqus 2007[c]].

The stiffness matrix for cohesive element is written as [Abdul-Baqi 2005]

$$K = \int_s [N]^T \left\{ \frac{\partial T}{\partial u} \right\} [N] dS \qquad 5.16$$

Nodal force for cohesive elements can be written as [Abdul-Baqi 2005]

$$f = \int_s [N]^T \{T\} dS \qquad 5.17$$

Where: [N] = shape function; S = cohesive zone area for cohesive elements.

Cohesive zone frame work incorporated in Abaqus is assumed to follow the same principle of virtual work. Damage initiation i.e. onset of crack initiation and beginning of material degradation begin when quadratic nominal stress criterion is met. This criterion is defined as follows

$$\left\{ \frac{(t_n)}{t_n^0} \right\}^2 + \left\{ \frac{(t_t)}{t_t^0} \right\}^2 + \left\{ \frac{(t_b)}{t_b^0} \right\}^2 = 1 \qquad 5.18$$

Where: $t_n^0, t_t^0, t_b^0 =$ peak values of the nominal stress when deformation is either pure normal to the interface or pure in first shear or the second shear direction respectively.

The evolution of damage under the combination of normal and shear deformation can be expressed in terms of an effective displacement. Damage due to combination of normal and shear deformation expressed in terms of δ_n, δ_t and δ_b gives the displacement.

$$\delta = \sqrt{\delta_n^2 + \delta_t^2 + \delta_b^2} \qquad 5.19$$

The degradation of material stiffness is specified in terms of the damage variable, D given by

$$D = \frac{\delta^f \left(\delta^{max} - \delta^0 \right)}{\delta^{max} \left(\delta^f - \delta^0 \right)} \qquad 5.20$$

Where δ^{max} is the maximum effective displacement achieved during the loading history and $\delta^{f} - \delta^{0}$ is the effective displacement at failure relative to the effective displacement at damage initiation. The scalar damage variable, D monotonically evolves from 0 to 1 upon further loading after the initiation of damage. When all the material points in the cohesive element reach the maximum damage variable, the traction between the surfaces no longer exists and elements are deleted.

Node Based Sub-modeling Approach for Cohesive zone failure Model

In cohesive-zone failure model study, same JEDEC test board has been used. Relative velocity vectors extracted from DIC at discrete locations during drop event have been implemented as boundary condition for the attachment degrees of freedom in the cohesive zone model. A thin layer of cohesive element is incorporated between copper pad and solder ball at four corner locations of the package. Cohesive layer is modeled with COH3D8 element [Abaqus 2007[c]]. Solder balls at four corners are modeled as 3 dimensional continuum reduced integration (C3D8R) elements while remaining solder interconnects are modeled as Timoshenko-beam element (B31). Failure stress value of 110Mpa [Darveaux 2006] has been used in damage initiation criteria in simulation. Stiffness degradation variable is used to relate the failure of the package with number of drops i.e. number of times the PCB is subjected to shock.

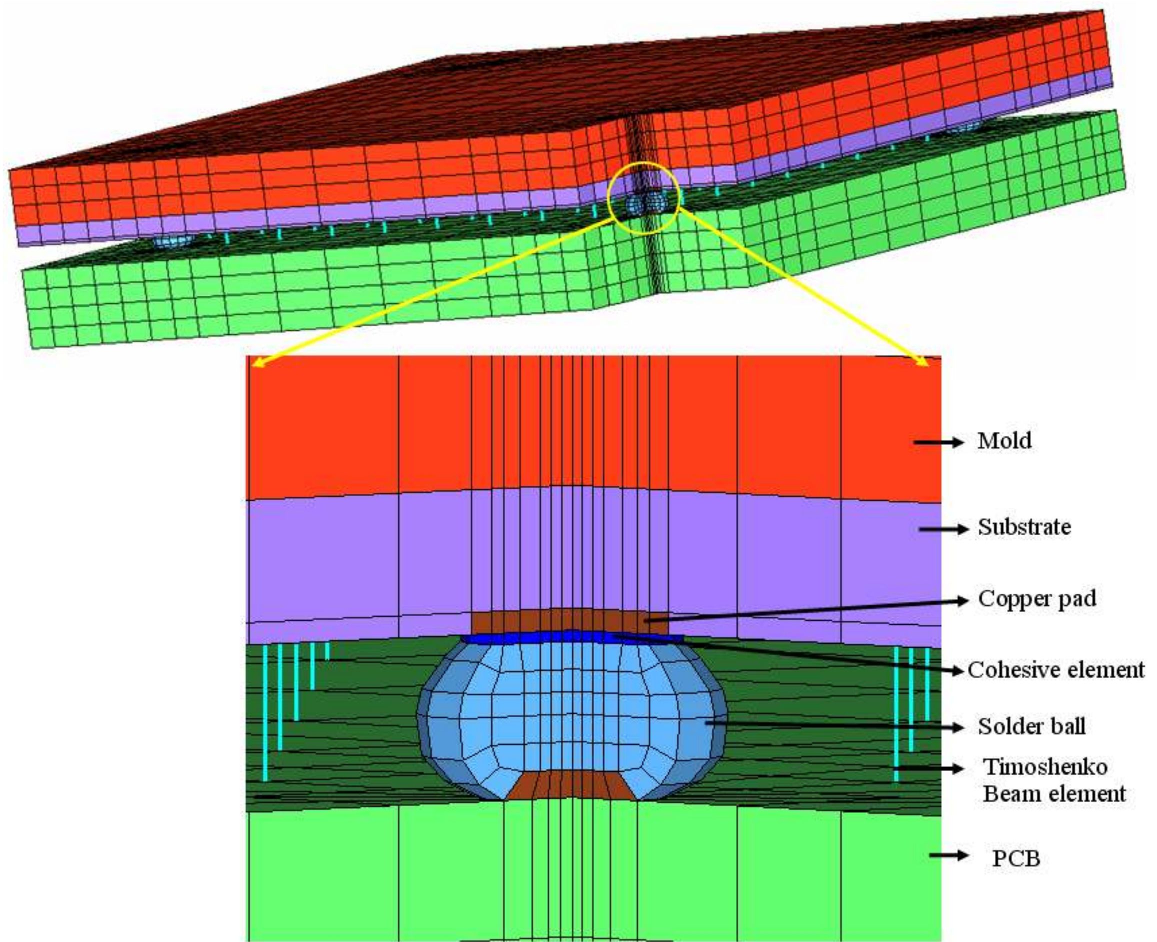
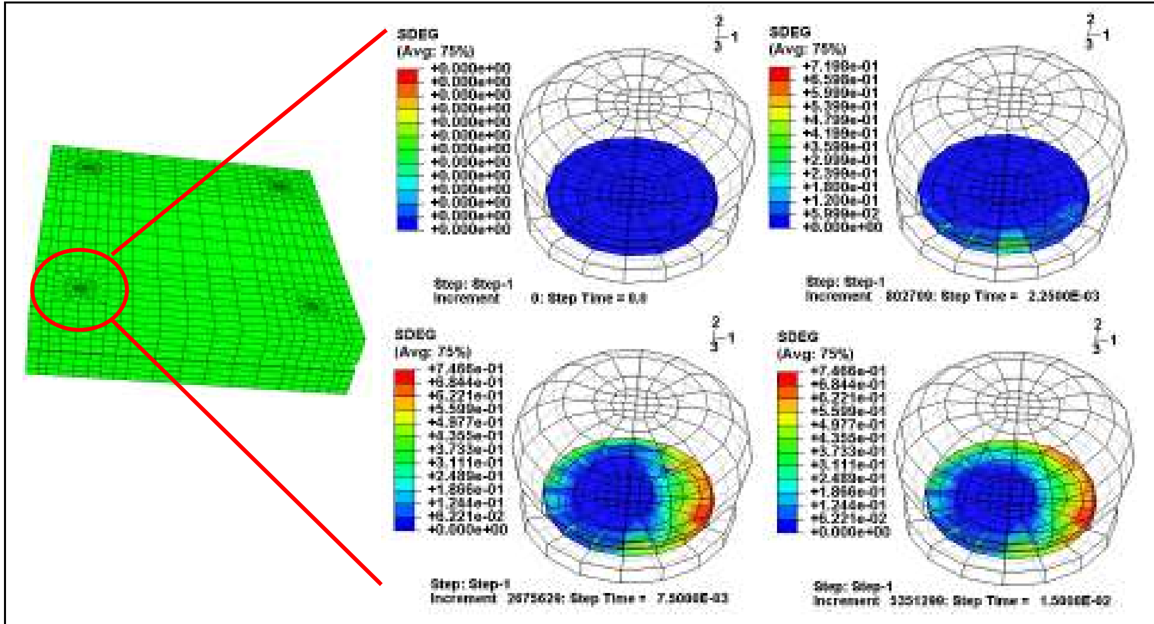


Figure 5.22: Printed Circuit Assembly with cohesive element incorporated between the copper pad and the solder interconnect interface in all four corners of the package and retaining remaining interconnects as Timoshenko beam elements

Modeling Correlation for Cohesive zone failure model



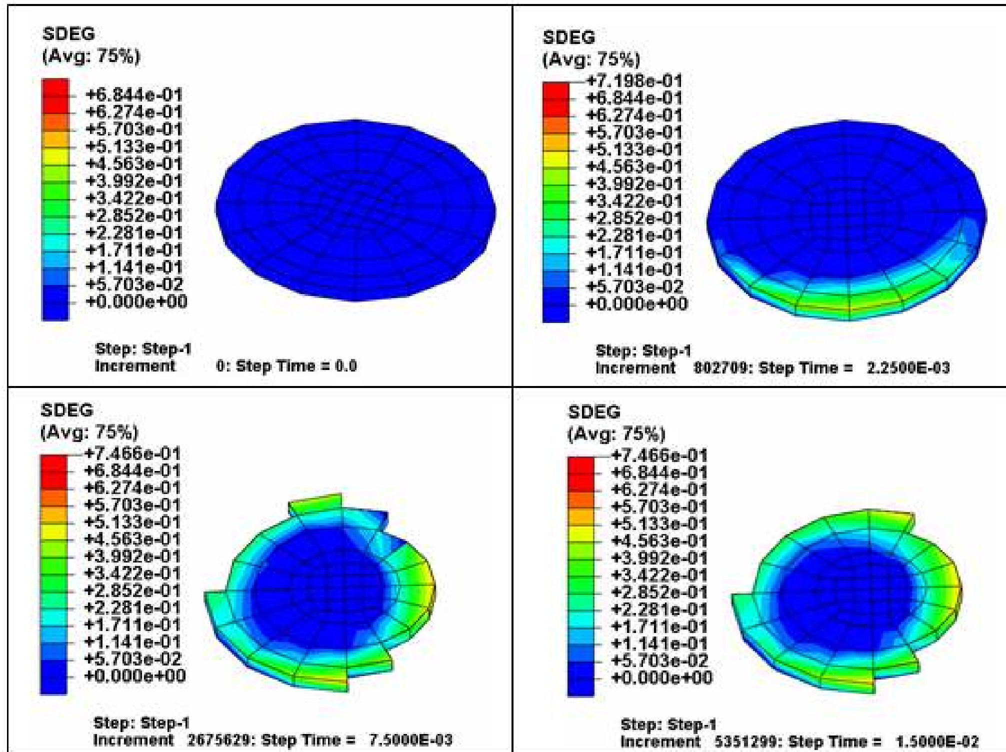


Figure 5.23: Prediction of crack initiation and crack propagation across cohesive zone at different time interval for SAC105 (Pristine board) Package 8.

CHAPTER 6

RELIABILITY ANALYSIS OF LEAD-FREE INTERCONNECTS

6.1 Introduction:

In this chapter, failure analyses for pristine and thermally aged lead free solder alloy system have been presented. Reliability predictions were based on Weibull plots. Failure modes have been classified as ductile and brittle at the bulk solder and IMC interface on the package and the PCB side.

6.2 Weibull Distribution and Failure Modes:

All the failed packages were cross-sectioned to investigate the failure modes. Observed failure modes include, failure at the solder copper interface board side, as well as on component side, copper trace crack, bulk solder crack and resin crack. Thermally aged solder interconnects were observed to have lower shock survivability compared to pristine interconnects (Figure 6.1, Figure 6.3, Figure 6.5). Solder interconnect and copper pad interface failure on component side were dominant failure modes for pristine samples in all the three alloy system studied (Figure 6.2a, Figure 6.4a, Figure 6.6a). But in the case of thermally aged SAC105 and Sn3.5Ag, solder interconnect and copper pad interface failure on board side were dominant failure modes (Figure 6.2b, Figure 6.6b)

and bulk solder crack was dominant failure mode in thermally aged SAC305 alloy system (Figure 6.4b). For all the three solder alloy systems weibull distribution exhibit different slopes between pristine and thermally aged samples indicating the change in the failure modes. Failure of the packages were random in nature. Figure 6.7 shows the schematic representation of various failure modes observed across solder interconnect and Table 6.1 shows the corresponding description of various failure modes. Figure 6.8 shows the distribution of failure modes observed in the first 5 failed packages in each printed circuit board assemblies.

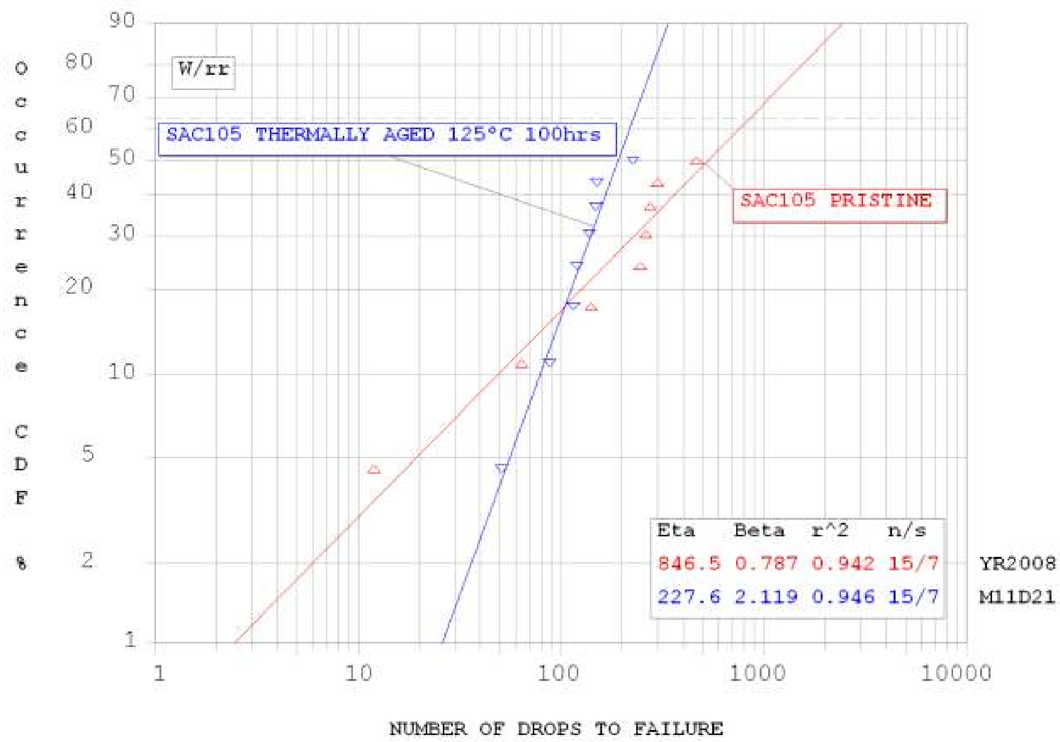
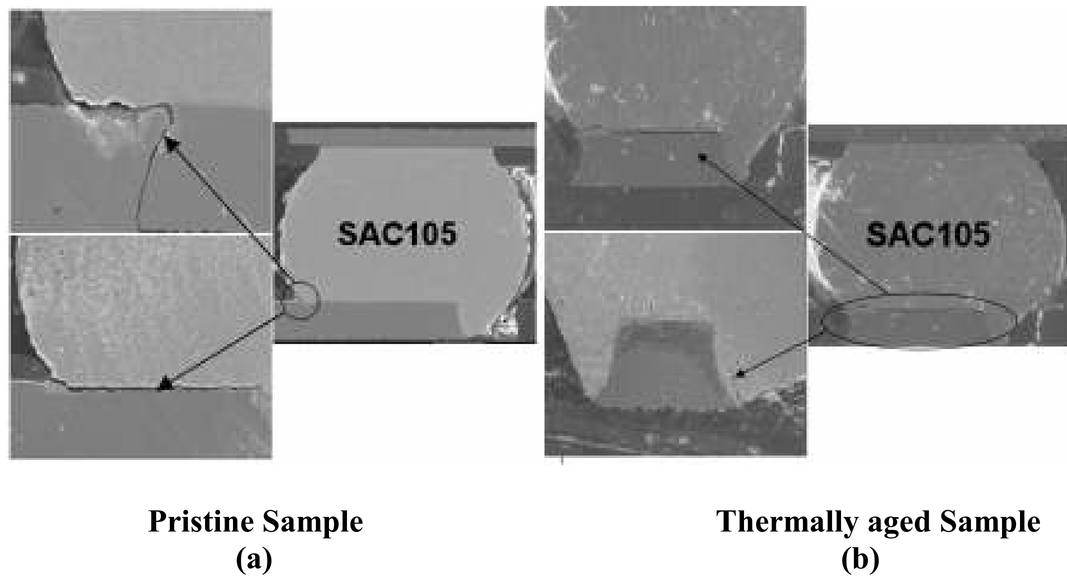


Figure 6.1: Weibull Distribution for Pristine and Thermally Aged SAC105 Lead-free alloys



Pristine Sample (a)

Thermally aged Sample (b)

Figure 6.2: Failure Modes observed in solder joints for Sn1Ag0.5Cu

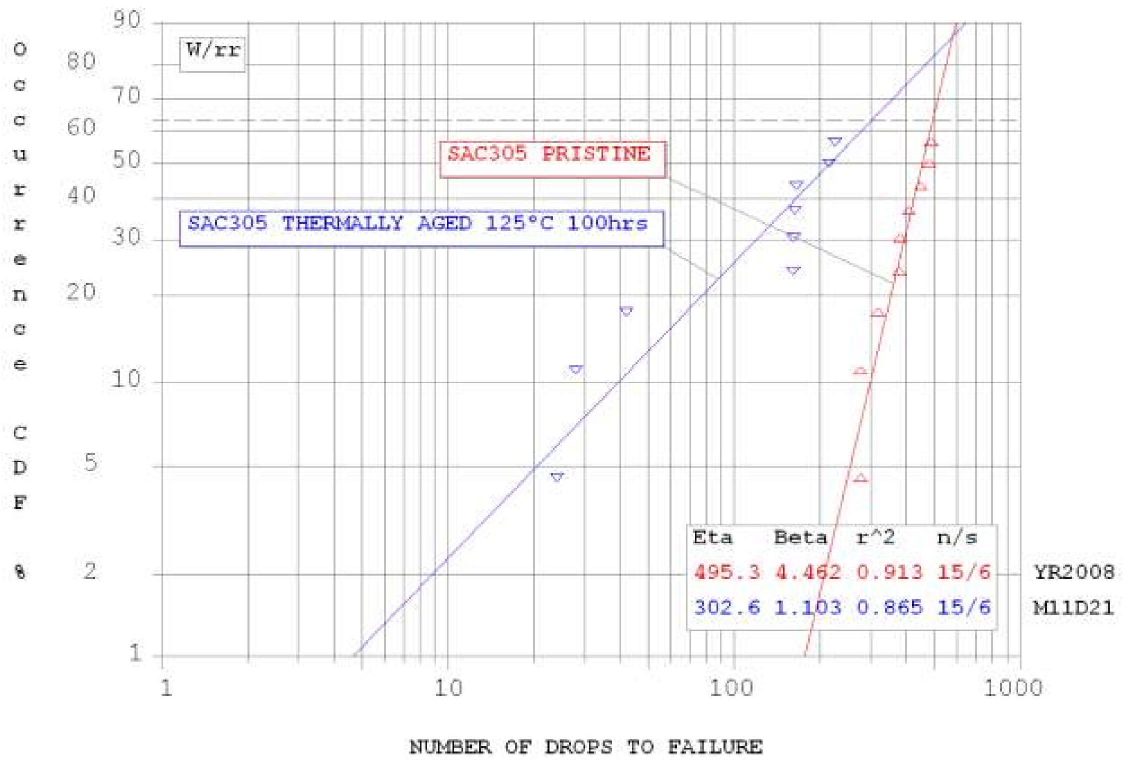
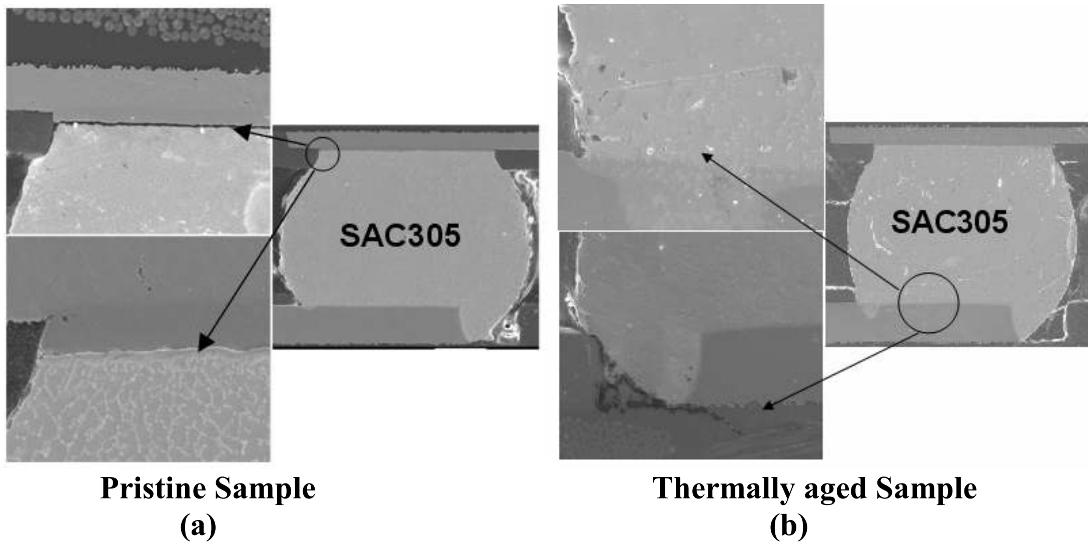


Figure 6.3: Weibull Distribution for Pristine and Thermally Aged Sn3Ag0.5Cu lead free alloys



Pristine Sample
(a)

Thermally aged Sample
(b)

Figure 6.4: Failure Modes observed in solder joints for Sn3Ag0.5Cu

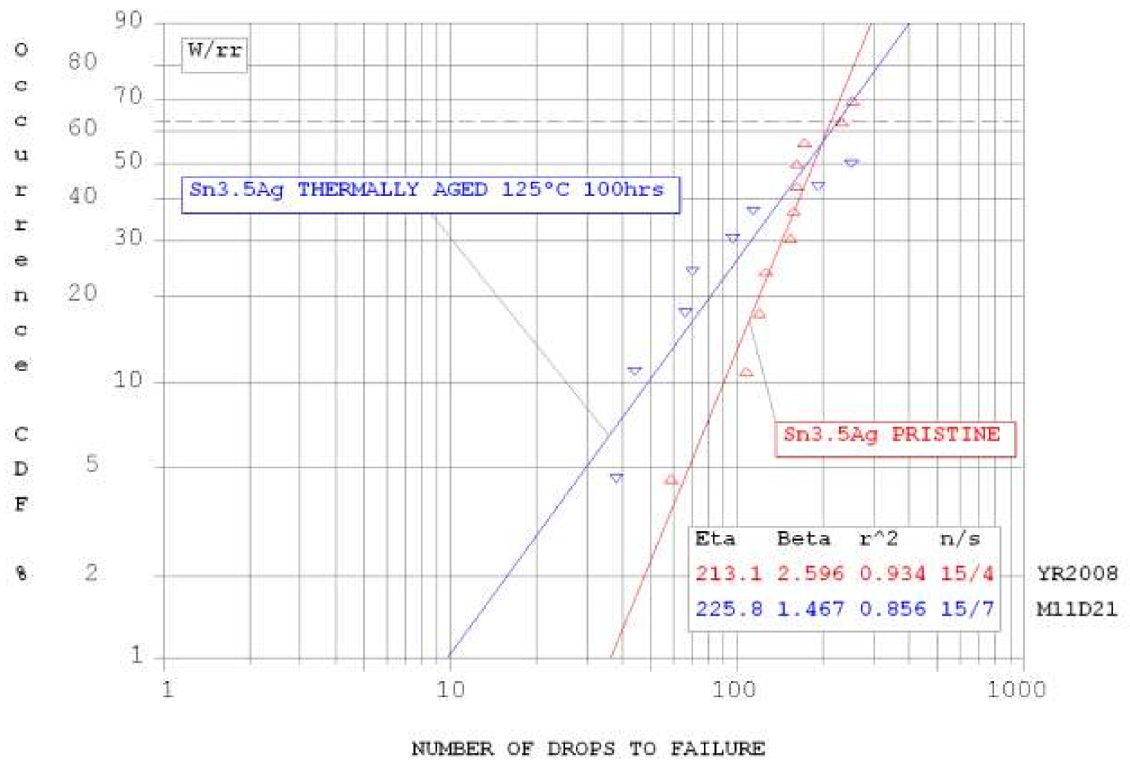
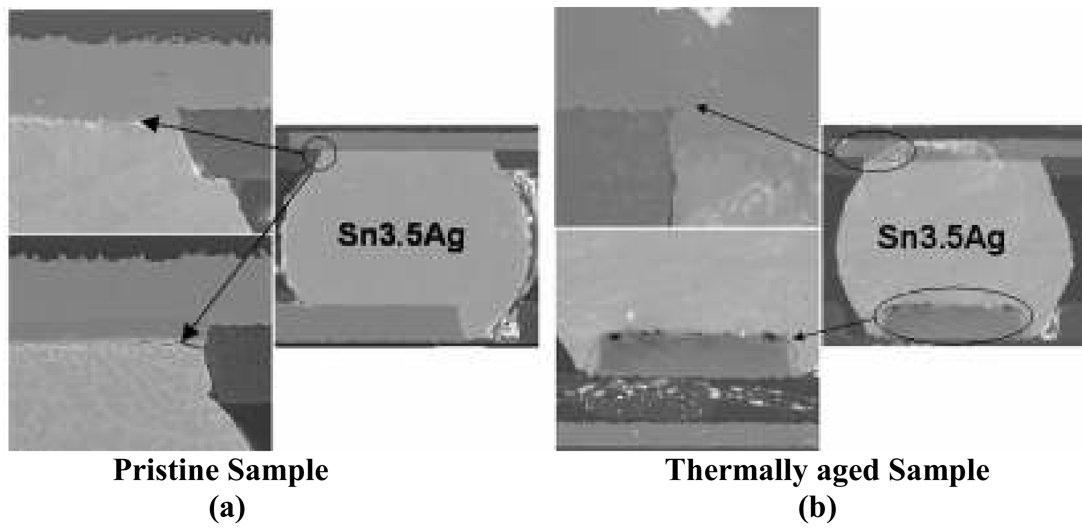


Figure 6.5: Weibull Distribution for Pristine and Thermally Aged Sn3.5Ag lead free alloys



Pristine Sample (a) **Thermally aged Sample (b)**

Figure 6.6: Failure Modes observed in solder joints for Sn3.5Ag

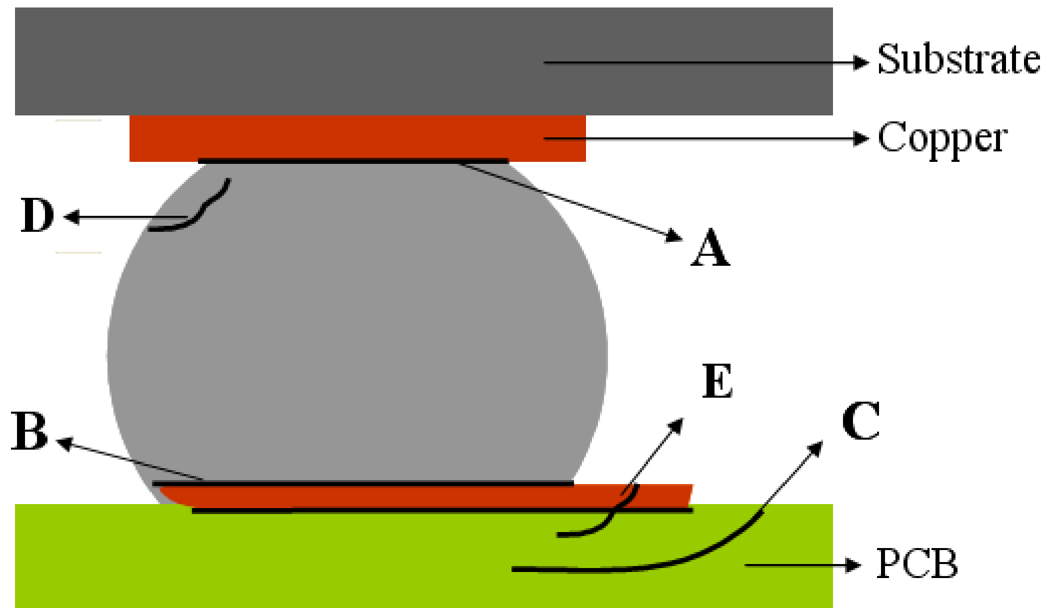


Figure 6.7: Failure Modes

Table 6.1: Failure Modes Description

Failure Mode	Description
A	Solder-Copper pad interfacial failure on Package side
B	Solder-Copper pad interfacial failure on PCB side
C	Resin Crack
D	Bulk Solder
E	Copper Trace Failure

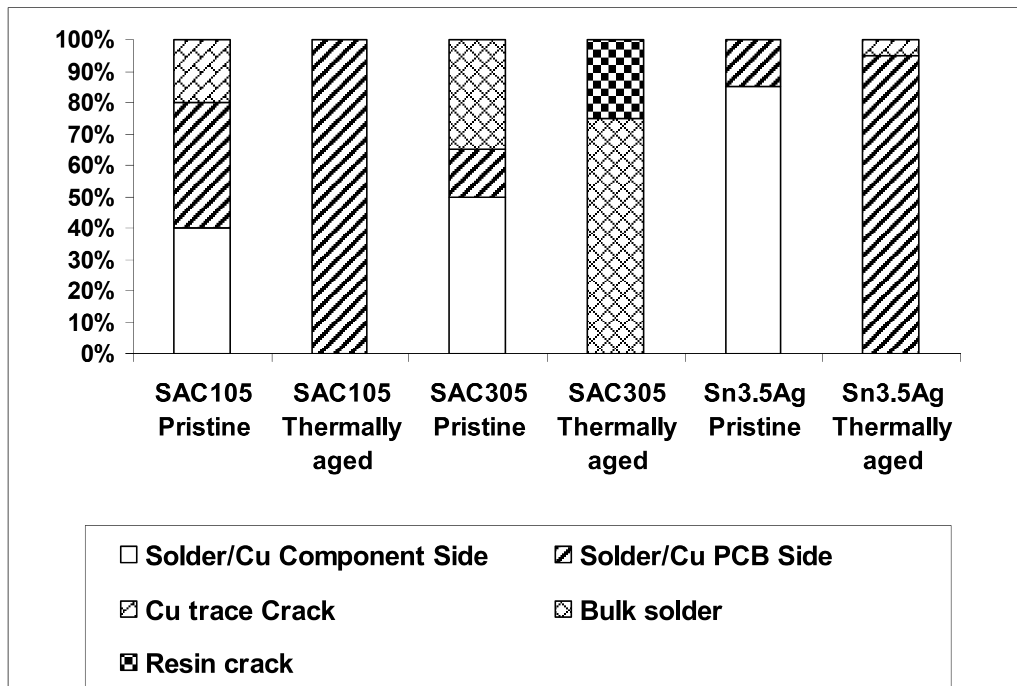


Figure 6.8: Comparison of Failure Modes in the 3 Different Alloy Systems at Pristine and Thermally aged Conditions.

CHAPTER 7

LIFE PREDICTION MODEL FOR LEAD-FREE SOLDER INTERCONNECTS SUBJECTED TO SHOCK-IMPACT

7.1 Introduction

Printed circuit board assemblies were subjected to shock impact. Failure of the package has been identified as an increase in the voltage drop. As mentioned earlier, different locations on the test board exhibits different strain histories during same drop and different number of drops to failure. However, the strain histories are very consistent and repeatable at the same component locations across various test boards. Strain correlation between DIC and simulation on board side has been demonstrated in chapter 5. Transient strain history for entire array of solder interconnects on various test boards have been predicted using explicit finite element analysis. Rain-flow analysis was then used to extract constant amplitude cycles from a non-uniform time history of a transient dynamic solder interconnect stain. Linear damage superposition principle has been used for life prediction of solder interconnect. Figure 7.1 shows flow chart for damage superposition based on solder interconnect strain data.

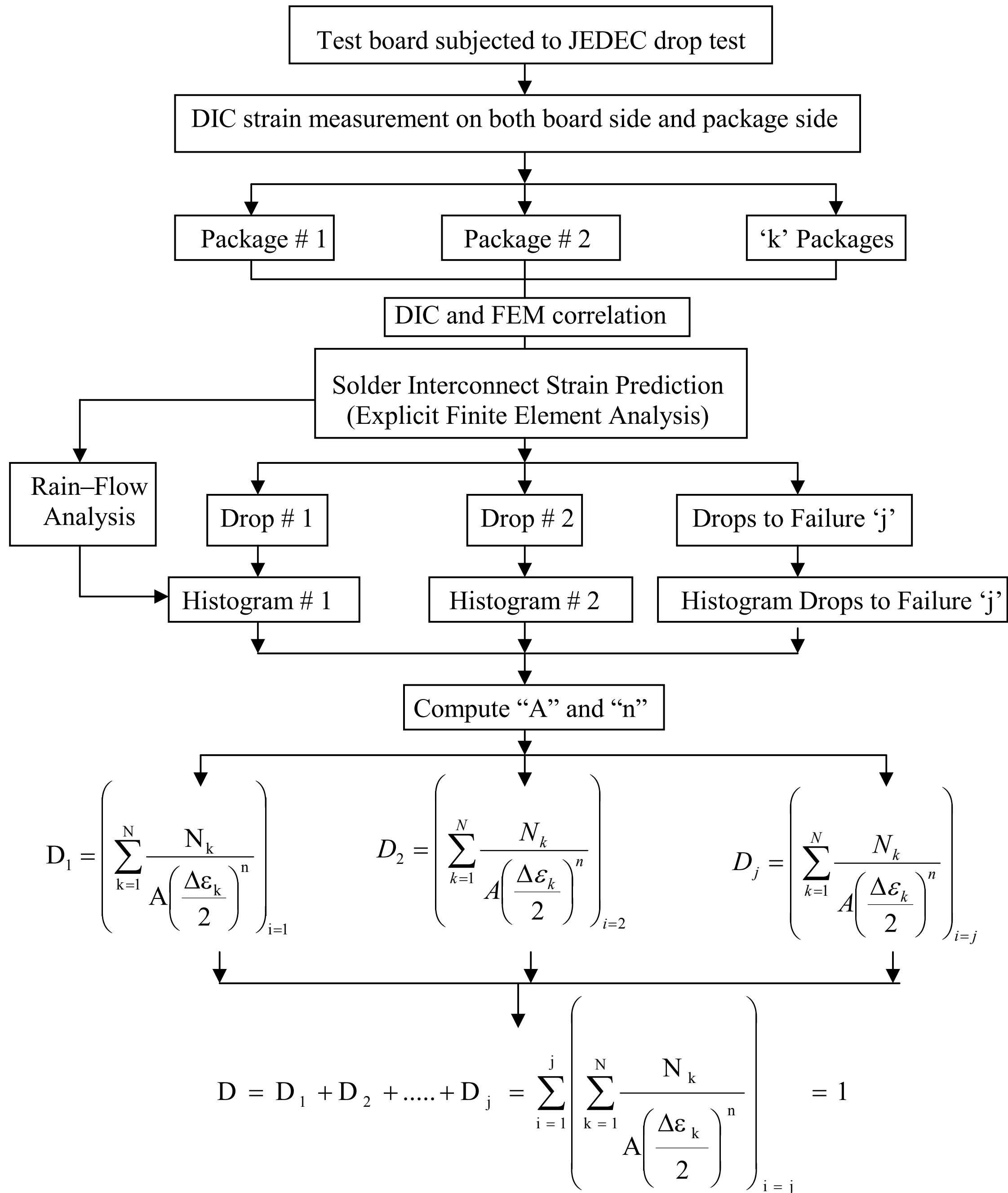


Figure 7.1: Flow chart for Damage Superposition based on Solder Interconnect Strain

7.2 Rain-flow analysis

In transient shock and drop, the loads vary in amplitude and frequency. Electronic structures very rarely experience constant amplitude loading. In general, rain-flow counting algorithm is used in the analysis of fatigue data in order to reduce a spectrum of varying strain into a set of simple strain reversals. Rain-flow analysis allows the application of Miner's rule in order to assess the fatigue life of an electronic package subjected to complex loading. In this study, for cycle-counting analysis solder interconnect strain has been used as input to the rain-flow algorithm. The non-uniform sequence of strain peaks and valleys have been decomposed into an equivalent set of strain amplitude and cycle counts. A flow of rain is begun at each strain reversal in the history and is allowed to continue to flow unless, (a) the rain began at local maximum point (peak) and fall opposite a local maximum point greater than that from which it came. (b) the rain began at a local minimum point (valley) and falls opposite a local minimum point greater (in magnitude) than that from which it came. (c) it encounters a previous rain-flow. Detailed rules for cycle counting are described in [ASME 1997, Bannantine 1990, and Downing 1982].

Strain history of all solder interconnects in the 10*10 array for each package has been extracted. The solder interconnect which is subjected to maximum strain is chosen for rainflow analysis. Interconnect strain history has large number of very small strain amplitude cycles and very few number of large strain amplitude cycles.

7.3 Damage Superposition and Life Prediction of Lead-Free Solder Interconnect based on Relative Damage Index

JEDEC configuration results in repeatable drops leading to repeating solder interconnect strain history and hence damage has been extrapolated till failure using linear superposition principle Simultaneous solving method has been implemented to predict damage level.

Linear superposition of damage has been assumed in this study [Lall 2005]. Relative damage index is defined such that it achieves magnitude of the damage equal to "1" at failure. Re-writing Miner rule and Coffin-mansion relationship based on the assumed logarithmic relationship between strain amplitudes and number of cycles we have,

$$\sum_{k=1}^{N} \frac{D_k}{D} = 1 \qquad 7.1$$

$$\sum_{k=1}^{N} \frac{M_k}{A\left(\frac{\Delta\varepsilon_k}{2}\right)^n} = 1 \qquad 7.2$$

where, "k" is the bin-index for the histogram, $\Delta\varepsilon/2$ is the solder interconnect strain amplitude, M is the total number of bins in the histogram, N is the number of cycles subjected on the sample in the kth histogram bin during all the drops until-failure of the device, and D is the damage index. Data from data sets has been solved as follows,

$$\left(\sum_{i}^{j} \left(\sum_{k=1}^{N} \frac{N_k}{A\left(\frac{\Delta\varepsilon_k}{2}\right)^n} \right)_j \right)_X = 1 \qquad 7.3$$

$$\left(\sum_{i}^{j}\left(\sum_{k=1}^{N}\frac{N_k}{A(\frac{\Delta\varepsilon_k}{2})^n}\right)_j\right)_Y = 1 \quad 7.4$$

$$\left(\sum_{i}^{j}\left(\sum_{k=1}^{N}\frac{N_k}{A(\frac{\Delta\varepsilon_k}{2})^n}\right)_j\right)_Z = 1 \quad 7.5$$

Where the indices "X", "Y" and "Z" is related to solder interconnect strain extracted from 3 distinct packages of same alloy system. Simulated data of the solder interconnect strain is for only one drop by applying principle of superposition, cumulative relative damage index will be equivalent to 1 at failure.

$$\left(\sum_{i}^{j}\left(\sum_{k=1}^{N}\frac{N_k}{A(\frac{\Delta\varepsilon_k}{2})^n}\right)_j\right)_X - \left(\sum_{i}^{j}\left(\sum_{k=1}^{N}\frac{N_k}{A(\frac{\Delta\varepsilon_k}{2})^n}\right)_j\right)_Y = 0 \quad 7.6$$

$$\left(\sum_{i}^{j}\left(\sum_{k=1}^{N}\frac{N_k}{A(\frac{\Delta\varepsilon_k}{2})^n}\right)_j\right)_Y - \left(\sum_{i}^{j}\left(\sum_{k=1}^{N}\frac{N_k}{A(\frac{\Delta\varepsilon_k}{2})^n}\right)_j\right)_Z = 0 \quad 7.7$$

$$\left(\sum_{i}^{j}\left(\sum_{k=1}^{N}\frac{N_k}{A(\frac{\Delta\varepsilon_k}{2})^n}\right)_j\right)_X - \left(\sum_{i}^{j}\left(\sum_{k=1}^{N}\frac{N_k}{A(\frac{\Delta\varepsilon_k}{2})^n}\right)_j\right)_Z = 0 \quad 7.8$$

By solving above set of equations simultaneously, three pairs of constants "A" and "n" are evaluated and the particular pair which gives cumulative damage index value equal to "1" for all data sets is chosen as damage constant.

Damage during the life of the product should not exceed “1” for the design to have good survivability in drop and shock application. Table 7.1 shows the correlation of predicted fatigue life with experimentally measured life for pristine Sn3.5Ag lead free solder alloy. Predicted life shows good correlation with experimental data. The proposed methodology enables evaluation of the damage equivalency in the application of interest and for the packaging interconnect query.

Table 7.1: Correlation of Model Predictions of Component Life under Mechanical Impact versus Experimental Data for Pristine Sn3.5Ag Test Structure.

	Package Location	**Actual Failure Drop**	**Predicted Life**	**Error (%)**
Sn3.5Ag Pristine	1	172	154	-10.7
	2	162	149	-8.2
	12	233	151	-35.6

CHAPTER 8

SUMMARY AND CONCLUSION

In this thesis, transient dynamic response of the board level assemblies subjected to drop impact has been investigated in order to predict the life of the lead-free solder interconnects under high strain rates.

Digital image processing (DIC) technique for full-field high-speed measurement of board assembly deformation has been implemented. DIC technique in conjunction with high speed imaging has used to acquire full filed strain, displacement and velocity component for lead-free board assemblies subjected to impact. Full-field strain data from DIC has been accurately correlated with high-speed strain measurement (strain gage) at discrete printed circuit board assembly locations. Three explicit modeling techniques have been investigated for modeling shock loading of PCB assemblies. Modeling techniques investigated included smeared property with conventional-shell element based global model, Timoshenko-beam with continuum-shell element based global model and node-based explicit sub-model. First and the second modeling techniques were independent from DIC data and model prediction of transient strain have been correlated with optical measurement from DIC. The models have been used to compute solder interconnect strain histories during the drop event for all the three lead free assemblies.

The third modeling technique was dependent upon DIC data, obtained velocity component from DIC technique have been used for boundary condition of the attachment d.o.f of the sub-model. Model prediction from FEM have been correlated with transient strain histories extracted using DIC technique on package and PCB , solder interconnect strain histories during shock impact have been predicted from explicit FEM. Cohesive zone model have also been incorporated in node-based sub-modeling technique to predict the location and the mode of failure in solder interconnect. Failure modes for the both pristine and thermally aged lead-free alloys have been studied with the help of scanning electron microscope (SEM).

Linear damage superposition has been used for life prediction of solder interconnect. Solder interconnect strain based relative damage index has been developed for pristine Sn3.5Ag lead-free alloys. Fatigue constants are solved using averaging of simultaneous equation pair solution. The model prediction shows good correlation to experimental data. The present approach can be used for damage equivalency and life prediction of package as a function of package location in the electronic assembly.

BIBLIOGRAPHY

Abaqus Documentation, Finite Elements and Rigid Bodies, Getting Started with Abaqus Explicit: Keywords Version, Version 6.7[a].

Abaqus Documentation, Element Overview, Abaqus Theory Manual, Version 6.7[b].

Abaqus Documentation, Cohesive Elements, Abaqus Analysis User's Manual, Version 6.6, Section 26.5, 2007[c].

Abdul-Baqi, A., Schreurs, P. J. G., Geers, M. G. D., "Fatigue damage modeling in solder interconnects using a cohesive zone approach", International Journal of Solids and Structures, Volume 42, pp. 927-942, 2005.

Ahat, S, Sheng, M., Luo, L., "Microstructure And Shear Strength Evolution Of Sn/Ag/Cu Surface Solder Joint During Aging", Journal of Electronic Mater., Vol. 30, No. 10, pp. 1317-1332, 2001.

American Society of Mechanical Engineers (ASME), Standard Practices for Cycle Counting in Fatigue Analysis, ASTM E1049-85, 1997.

Amodio, D., Broggiato, G., Campana, F., Newaz, G., Digital Speckle Correlation for Strain Measurement by Image Analysis, Society for Experimental Mechanics, Vol. 43, No. 4, December 2003.

Bannantine, J. A., Comer, J.J., Handrock, J.L., "Fundamentals of Metal Fatigue Analysis", Prentice Hall, 1990.

Bansal, A., Yoon, S., Mahadev, V., "Flexural Strength of BGA Solder Joints with ENIG Substrate Finish using 4-Point Bend Test", Proceedings of the SMTA Pan Pacific Microelectronics Symposium, pp. 1-8, 2005.

Bieler, T., Jiang, H., Influence of Sn Grain Size and Orientation on the Thermomechanical Response and Reliability of Pb-free Solder Joints, Electronic Components and Technology Conference, pp. 1462- 14671, May 2006.

Chai, T. C., Quek, S., Hnin, W. Y., Wong, E. H., "Drop Level Drop Test Reliabilityof IC Packages", Proceedings of the 55th Electronic Components and Technology Conference, pp. 630-636, 2005.

Che, F.X., Luan, J.E., Baraton, X., Effect of Silver Content and Nickel Dopant on Mechanical Properties of Sn-Agbased Solders, Proceedings of the 58th Electronic Components and Technology Conference, Orlando, Florida, pp.485-490, May 27-30, 2008.

Che, F., Low, T., Pang, J., "Modeling Thermo-Mechanical Reliability of Bumpless Flip Chip Package", Electronic Components and Technology Conference, pp. 421-426, 2004.

Chiu, T., Zeng, K., Stierman, R., Edwards, D., Ano, K., "Effect of Thermal Aging on Board level drop reliability for Pb-free BGA Packages", Electronic Components and Technology Conference, pp. 1256-1262, June 2004.

Choi, J.Y., Kang, I.S., Park, B.J., Park, Y. M., Jung, G.J., Study on Inter-Metallic Compound (IMC) at Interface of Pb-Free Solder and Nickel UBM for Mobile Application, Proceedings of the 57th ECTC, Reno, Nevada, pp.1802-1808, May29th-June 1st, 2007.

Chong, D.Y.R., Toh, H.J., Lim, B.K., Low, P. T.H., Drop Reliability Performance Assessment for PCB Assemblies of Chip Scale Packages (CSP), Electronic Packaging Technology Conference, pp. 262-269, June, 2005.

Clech., J-P., "Flip-chip /CSP Assembly Reliability and Solder Volume Effects", Proceedings of the Surface Mount International Conference, pp. 315-324, 1998.

Clech., J-P., "Solder Reliability Solutions: a PC-based Design-for-reliability Tool", Proceedings of the Surface Mount International Conference, pp. 136-151, 1996.

Coffin, L., "A Study Of The Effect Of Cyclic Thermal Stresses On A Ductile Metal", ASME Transactions, Vol. 76, pp. 931-950, 1954.

Darveaux, R., Reichman, C., Islam, N., "Interface Failure in Lead Free Solder Joints", Electronic Components and Technology Conference, pp. 906-917, 2006.

Darveaux, R., et al., "Reliability of Plastic Ball Grid Array Assembly", Chapter 13, Ball Grid Array Technology, Ed. Lau, J.H. McGraw-Hill, 1995.

Date, M., Shoji, T., Fujiyoshi, M., Sato, K., Tu, K. N., "Impact Reliability of Solder Joints", Proceedings of the 54th Electronic Components and Technology Conference, pp. 668-674, 2004.

Davis, C., Freeman, D., Statistics of subpixel registration algorithms based on spatiotemporal gradients or block matching, Optical Engineering, Vol. 37, pp. 1290-1298, 1998.

Downing, S. D., and Socie, D. F., Simple Rainflow Counting Algorithms, International Journal of Fatigue, Vol. 4, No. 1, pp. 31-40, 1982.

Gu, J., Cooreman, S., et al., Full-Field Optical Measurement For Material Parameter Identification With Inverse Methods, WIT Transactions on The Built Environment, Vol. 85, 2006.

Gu, J., Lim, C. T., Tay, A. A. Y., "Simulation of Mechanical Response of Solder Joints under Drop Impact Using Equivalent Layer Models", Proceedings of the 55th Electronic Components and Technology Conference, pp. 522-529, 2005.

Gu, J., Lim, C. T., Tay, A. A. Y., "Equivalent Solder Joint and Equivalent Layer Models for the Simulation of Solder Column Failure under Drop Impact", Proceedings of the 6th Electronic Packaging Technology Conference, pp. 547-552, 2004.

Gu, J., Lim, C. T., Tay, A. A. Y., "Modeling of Solder Joint Failure due to PCB Bending during Drop Impact", Proceedings of the 6th Electronic Packaging Technology Conference, pp. 678-683, 2004.

Harada, K., Baba, S., Wu, Q., Matsushima, H., Matsunaga, T., Uegai, Y., Kimura, M., "Analysis of Solder Joint Fracture under Mechanical Bending Test", Electronic Components and Technology Conference, pp. 1731-1737, 2003.

Huang, B., Hwang, H., Lee, N., A Compliant and Creep resistant SAC-Al(Ni) Alloy, Proceedings of the 57th ECTC, Reno, Nevada, pp. 184- 191, May 29-June 1, 2007.

Irving, S., Liu, Y., "Free Drop Test Simulation for Portable IC Package by Implicit Transient Dynamics FEM", Proceedings of the 54th Electronic Components and Technology Conference, pp. 1062-1066, 2004.

Jang. J., De Silva, A.P.,Drye, J.E., Post, S. L., Owens, N.L., Lin, J., Frear, D.R., Failure Morphology After Drop Impact Test of Ball Grid Array (BGA) Package With Lead-Free Sn–3.8Ag–0.7Cu and Eutectic SnPb Solders, IEEE Transactions On Electronics Packaging Manufacturing, Volume:30, Issue 1, pp. 49 – 53, January, 2007.

Jin, H., Lu, W., Hong, S., Connelly, K., Fracture Behavior of Polyurethane Foams, Proceedings of the 2007 SEM Annual Conference and Exposition on Experimental and Applied Mechanics, Springfield, Massachusetts, June 4-6, 2007.

Kawashiro, F., Ujiie, M., Shibuya, K., Kurita, Y., Soejima, K., Kawano, M., Reliability Studies of Sn-Ag-Cu BGA Solder Joints on Ni/Cu/Au Surface Finish for SMAFTI Packaging Technology, Proceedings of the 58th Electronic Components and Technology Conference, Orlando, Florida, pp.283 -289, May 27-May 30, 2008.

Kehoe, L., Lynch, P., Guénebaut, V., Measurement of Deformation and Strain in First Level C4 Interconnect and Stacked Die using Optical Digital Image Correlation, Electronic Components and Technology Conference, pp. 1874-1881, May 2006.

Kim, H., Zhang, M., Kumar, C., Liu, p., kim, D., Xie, m., Wang, Z., Improved Drop Reliability Performance with Lead Free Solders of Low Ag Content and Their Failure Modes, Proceedings of 57th ECTC, Reno, Nevada, pp 962- 967, May 29-June 1, 2007.

Kim, P., Kim, B., Ahn, E., Chung, T., Improvement of Drop Reliability in OSP/Cu Pad Finished Packages, Electronic Packaging Technology Conference, pp. 168-173, December, 2006.

Lall, P., Choudhary, P., Gupte, S., Suhling, J., Health Monitoring for Damage Initiation and Progression during Mechanical Shock in Electronic Assemblies, IEEE Transactions on Components and Packaging Technologies, Vol. 31, No. 1, pp. 173-183, March 2008a.

Lall, P., Panchagade, D., Choudhary, P., Gupte, S., Suhling, J., Failure-Envelope Approach to Modeling Shock and Vibration Survivability of Electronic and MEMS Packaging, IEEE Transactions on Components and Packaging Technologies, Vol. 31, No. 1, pp. 104-113, March 2008b.

Lall, P., Iyengar, D., Shantaram, S., S., Gupta, P., Panchagade, D., Suhling, J., KEYNOTE PRESENTATION: Feature Extraction and Health Monitoring using Image Correlation for Survivability of Leadfree Packaging under Shock and Vibration, Proceedings of the 9th International Conference on Thermal, Mechanical, and Multi-Physics Simulation and Experiments in Micro-Electronics and Micro-Systems (EuroSIME), Freiburg, Germany, pp. 594-608, April 16-18, 2008c.

Lall, P., Iyengar, D., Shantaram, S., Pandher, R., Panchagade, D., Suhling, J., Design Envelopes and Optical Feature Extraction Techniques for Survivability of SnAg Leadfree Packaging Architectures under Shock and Vibration, Proceedings of the 58th Electronic Components and Technology Conference (ECTC), Orlando, Florida, pp. 1036-1047, May 27-30, 2008d.

Lall, P., Choudhary, P., Gupte, S., Suhling, J., Hofmeister, J., Statistical Pattern Recognition and Built-In Reliability Test for Feature Extraction and Health Monitoring of Electronics under Shock Loads, 57th Electronics Components and Technology Conference, Reno, Nevada, pp. 1161-1178, May 30-June 1, 2007a.

Lall, P., Gupte, S., Choudhary, P., Suhling, J., Solder-Joint Reliability in Electronics Under Shock and Vibration using Explicit Finite Element Sub-modeling, IEEE Transactions on Electronic Packaging Manufacturing, Volume 30, No. 1, pp. 74-83, January 2007b.

Lall, P., Panchagade, D., Iyengar, D., Shantaram, S., Suhling, J., Schrier, H., High Speed Digital Image Correlation for Transient-Shock Reliability of Electronics, Proceedings of the 57th ECTC, Reno, Nevada, pp. 924-939, May 29 – June 1, 2007c.

Lall, P. Panchagade, D., Liu, Y., Johnson, W., Suhling, J., Smeared Property Models for Shock-Impact Reliability of Area-Array Packages, ASME Journal of Electronic Packaging, Volume 129, pp. 373-381, December 2007d.

Lall, P., Hande, M., Bhat, C., Islam, N., Suhling, J., Lee, J., Feature Extraction and Damage-Precursors for Prognostication of Lead-Free Electronics, Microelectronics Reliability, Volume 47, pp. 1907–1920, December 2007e.

Lall, P., Choudhary, P., Gupte, S., Health Monitoring for Damage Initiation & Progression during Mechanical Shock in Electronic Assemblies, Proceedings of the 56th ECTC, San Diego, California, pp.85-94, May 30-June 2, 2006a.

Lall, P., Gupte, S., Choudhary, P., Suhling, J., Solder-Joint Reliability in Electronics Under Shock and Vibration using Explicit Finite-Element Sub-modeling, Proceedings of the 56th ECTC, pp. 428 – 435, 2006b.

Lall, P., Panchagade, D., Choudhary, P., Suhling, J., Gupte, S., "Failure-Envelope Approach to Modeling Shock and Vibration Survivability of Electronic and MEMS Packaging", Proceedings of the 55th Electronic Components and Technology Conference, pp. 522-529, 2005.

Lall, P., Panchagade, D., Liu, Y., Johnson, W., Suhling, J., "Models for Reliability Prediction of Fine-Pitch BGAs and CSPs in Shock and Drop Impact", Proceedings of the 54th Electronic Components and Technology Conference, pp. 1296-1303, 2004.

Lee, W. W., et al., "Solder Joint Fatigue Models: Review And Applicability To Chip Scale Packages", Microelectronics Reliability, Vol. 40, pp. 231-244, 2000.

Liu, X., Sooklal, V.K., Verges, M.A., Larson, M.C., Experimental Study and Life Prediction on High Cycle Vibration Fatigue in BGA Packages, Microelectronics and Reliability, Volume 46, Issue 7, , pp. 1128-1138, July 2006.

Liu, S., Wang, X., Ma, B., Gan, Z., Zhang, H., Drop Test and Simulation of Portable Electronic Devices, International Conference on Electronic Packaging Technology, pp.701-704, June, 2005.

Luan, J., Goh, K., Baraton, X., "A Novel Methodology for Virtual Qualification of IC Packages under Board Level Drop Test", Electronic Component and Technology Conference, pp-1212-1217, 2008

Luan, J., Tee, T., "Effect of Impact Pulse Parameters on Consistency of Board Level Drop Test and Dynamic Responses", Electronic Components and Technology Conference, pp. 665-673, 2005.

Luan, J., Tee, T. Y., "Novel Board Level Drop Test Simulation using Implicit Transient Analysis with Input-G Method", Proceedings of the 6th Electronic Packaging Technology Conference, pp. 671-677, 2004.

Ma, H., Suhling, J., Lall, P., Bozack, M., "Reliability of the aging Lead Free Solder Joint", Electronic Component and Technology Conference, pp 849-864, 2006.

Manson, S., "Fatigue: A Complex Subject – Some Simple Approximations", Experimental Mechanics 5, No. 7, pp. 193-226, 1965.

Mei, Z., Ahmad, M., Hu, M., Ramakrishna, G., "Kirkendall Voids at Cu/Solder Interface and their effects on solder joint reliability", Electronic Components and Technology Conference, pp. 415-420, 2005.

Miller, T., Schreier, H., Reu, P, High-speed DIC Data Analysis from a Shaking Camera System, Proceedings of the SEM Conference, Springfield, Massachusetts, June 4-6, 2007.

Needleman, A., "A Continuum Model for Void Nucleation by Inclusion Debonding", Journal of Applied Mechanics, Volume 54, pp. 525-531, 1987.

Newman, K., "BGA Brittle Fracture - Alternative Solder Joint Integrity Test Methods", Electronic Components and Technology Conference, pp. 1194-1201, 2005.

Ng, H., Tee, T., et al., "Absolute and Relative Fatigue Life Prediction Methodology for Virtual Qualification and Design Enhancement of Lead-free BGA", Electronic Components and Technology Conference, pp. 1282-1291, 2005.

Ong,Y.C., Shim,V.P.W., Chai, T.C., LimC.T., Comparison of Mechanical Response of PCBs Subjected to Product-Level and Board-Level Drop Impact Tests, Electronic Packaging Technology Conference, pp. 223-227, June, 2003.

Pandher, R., Healey, R., Reliability of Pb-Free Solder Alloys in Demanding BGA and CSP Applications, Electronic Systems, Proceedings of the 58th Electronic Component & Technology Conference, Orlando, Florida, pp. 2018-2023, May27th-May30th, 2008.

Pandher, R., Lewis, Brian., Vangaveti, R., Singh, B., Drop Shock Reliability of lead free Alloys – Effect of Micro- Additives, Proceedings of the 57th ECTC, Reno, Nevada, pp. 669 - 676, May 29- June 1, 2007.

Pang, J., Che, F., Low, T., “Vibration Fatigue Analysis For FCOB Solder Joints”, Electronic Components and Technology Conference, pp. 1055-1061, 2004.

Park, S., Al-Yafawi, A., Yu, D., Kwak, J., Lee, J., Goo, N., Influence of Fastening Methods on the Dynamic Response and Reliability Assessment of PCBS in Cellular Phones Under Free Drop, Proceedings of the ITherm, Intersociety Conference on Thermal and Thermo-mechanical Phenomena, Orlando, Florida, pp.876-882, May 28-31, 2008

Park, S., Shah, C., Kwak, J., Jang, C., Pitarresi, J., Transient Dynamic Simulation and Full-Field Test Validation for A Slim-PCB of Mobile Phone under Drop Impact, Proceedings of the 57th ECTC, Reno, Nevada, pp. 914-923, May 29 – June 1, 2007a.

Park, S., Reichman, A., Kwak, J., Chung, S., Whole Field Analysis of Polymer Film, Proceedings of the SEM Conference, Springfield, Massachusetts, June 4-6, 2007b.

Perkins, A., Sitaraman, K., “Vibration-Induced Solder Joint Failure of a Ceramic Grid Array (CCGA) Package”, Electronic Components and Technology Conference, pp. 1271-12787, 2004.

Peterson, D., Cheng, C., Karulkar, P.C., Characterization of Drop Impact Survivability of a 3D-CSP Stack Module, Proceedings of the 58th Electronic Component and Technology Conference, Orlando, Florida, pp. 1648-1653, May 27-30, 2008.

Pitarressi, J., Roggeman, B., Chaparala, S., “Mechanical Shock Testing and Modelingof PC Motherboards”, Proceedings of the 54th Electronic Components and Technology Conference, pp. 1047-1054, 2004.

Rajendra, Pendse, D., Zhou, P., Methodology For Predicting Solder Joint Reliability In Semiconductor Packages, Microelectronics Reliability, Vol. 42, pp. 301-305, 2002.

Ren, W., Wang, J., Reinikainen, T., Application of ABAQUS/Explicit submodeling technique in drop simulation of system assembly, Proceeding of Electronic Packaging Technology Conference, pp. 541–546, 2004.

Ren, W., Wang, J., Shell-based simplified electronic package model development and its application for reliability analysis, Proceeding of Electronic Packaging Technology Conference, pp. 217–222, 2003.

Seah, S.K.W., Lim, C.T.,Wong, E.H., Tan, V.B.C., Shim, V.P.W., Mechanical Response of PCBs in Portable Electronic Products During Drop Test, Electronic Packaging Technology Conference, pp. 120-125, May, 2002.

Scheijgrond,P.L.W., Shi, D.X.Q., Driel, W.D.V., Zhang,G.Q., Nijmeijer, H., Digital Image Correlation for Analyzing Poratable Electronic Products during Drop Impact Tests, 6th International Conference on Electronic Packaging Technology, pp. 121 – 126, Aug 30.-Sept 2. 2005.

Shah, K., Mello, M., Ball Grid Array Solder Joint Failure Envelope Development for Dynamic Loading, Electronic Components and technology Conference, Las Vegas, Nevada, pp. 1067-1074, June 1-4, 2004.

Shi, D., Fan, X., Wafer-Level Film Selection for Stacked-Die Chip Scale Packages, Proceedings of the 57th Electronic Component & Technology Conference, Reno, Nevada, pp. 1731-1736, May 29 – June 1, 2007.

Song, F., Lo, C.C.J., Lam, J., Jiang, T., Lee, S.W., A Comprehensive Paralell Study on the Board Level Reliability of SAC, SACX and SACN Solders, Proceedings of the 58th ECTC, Orlando, Florida, pp.146-154, May27th-May30th, 2008.

Srinivasan, V., Radhakrishnan, S., Zhang, X., Subbarayan, G., Baughn, T., Nguyen, L., High Resolution Characterization of Materials Used In Packages Through Digital Image Correlation, InterPACK Conference Proceedings, July 17-22, 2005.

Sun, Y., Pang, J., Shi, X., Tew, J., Thermal Deformation Measurement by Digital Image Correlation Method, Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronics Systems, pp. 921-927, May 2006.

Sweatman, K., Suenaga, S., Nishimura, T., Strength of Lead-free BGA Sphere in High Speed Loading, Surface Mount Technology Association Pan Pacific, Kauai, Hawaii, pp.127-133, Jan22-Jan24, 2008

Syed, A., Kim, T.S., Cha, S.W., Scanlon, J., Ryu, C.G., Effect of Pb free Alloy Composition on Drop/Impact Reliability of 0.4, 0.5 & 0.8mm Pitch Chip Scale Packages with NiAu Pad Finish, Electronic Components and Technology Conference, pp. 951-956, 2007.

Syed, A., "Accumulated Creep Strain and Energy Density Based Thermal Fatigue Life Prediction Models for SnAgCu Solder Joints", Electronic Components and Technology Conference, pp. 737-746, 2004.

Tee, T. Y., Luan, J., Pek, E., Lim, C. T., Zhing, Z., Advanced Experimental and Simulation Techniques for Analysis of Dynamic Responses during Drop Impact, Electronic Components and Technology Conference, Las Vegas, Nevada, pp. 1088-1094, June 1-4, 2004.

Tee, T. Y., Ng, H. S., Lim, C.T., Pek, E., "Drop Impact and Impact Life Prediction Model for QFN Packages", Journal of SMT, Volume 16, Issue 3, pp. 31-39, 2003.

Tee, T. Y. , Hun Shen Ng, Chwee Teck Lim, Eric Pek , Zhaowei Zhong , Board Level Drop Test and Simulation of TFBGA Packages for Telecommunication Applications, Proceedings of the 53rd ECTC, pp. 121-129, 2003.

Thompson, R. J., Hemker, K. J., Thermal Expansion Measurements on Coating Materials by Digital Image Correlation, Proceedings of the 2007 SEM Annual Conference and Exposition on Experimental and Applied Mechanics, Springfield, Massachusetts, June 4-6, 2007.

Tiwari, V., Williams, S., Sutton, M., McNeill, S., Application of Digital Image Correlation in Impact Testing, Proceedings of the 2005 SEM Annual Conference and Exposition on Experimental and Applied Mechanics, June 7-9, 2005.

Towashiraporn, P., Xie, C., "Cohesive Modeling of Solder Interconnect Failure in Board Level Drop Test", Proceedings of the ITHERM, pp. 817-825, 2006.

Tsai, K.T., Liu, F.L., Wong, E.H., Rajoo, R., High Strain Rate Testing of Solder Interconnections, Conference on High Density Microsystem Design and Packaging and Component Failure Analysis, pp. 1-6, June, 2005.

Tsai, T., Yeh, C., Lai, Y., Chen, R., Incorporating Response Spectra and Modal Superposition in Analyzing Transient Responses of Structural Systems Subjected to Half-Sine Impact Acceleration Pulses, Electronic Components and Technology Conference, pp. 543-547, 2007.

Vogel, D., Gollhardt, A., Sabate, N., Keller, J., Michel, B., Reichl, H., Fraunhofer, I.Z.M., Localized Stress Measurements – A New Approach Covering Needs for Advanced Micro and Nanoscale System Development, Proceedings of the 57th Electronic Component & Technology Conference, Reno, Nevada, pp. 1490-1497, May 29 – June 1, 2007.

Wong, S. F., Malatkar, P., Rick, C., Kulkarni, V., Chin, I., Vibration Testing and Analysis of Ball Grid Array Package Solder Joints, Proceedings of the 57th Electronic Component & Technology Conference, Reno, Nevada, pp. 373-380, May 29 – June 1, 2007.

Wong, E. H., Rajoo, R., Mai, Y. W., Seah, S. K. W., Tsai, K. T., Yap, L. M., "Drop Impact: Fundamentals & Impact Characteristics of Solder Joints", Proceedings of the 55th Electronic Components and Technology Conference, pp. 1202-1209, 2005.

Wong, T., Fenger, H., "Vibration and Thermo-Mechanical Durability Assessments in Advanced Electronic Package Interconnects", Electronic Components and Technology Conference, pp. 1080-1087, 2004.

Wong, E. H., Lim, C. T., Field, J. E., Tan, V. B. C., Shim, V. P. M., Lim, K. T., Seah, S. K. W., Tackling the Drop Impact Reliability of Electronic Packaging, ASME InterPAK, July 6 -11, Maui, pp. 1 – 9, 2003.

Wong, T.E., Reed, B.A., Cohen, H. M., Chu, D. W., Development of BGA Solder Joint Vibration Fatigue Life Prediction Model, Proceedings of the 49th ECTC, pp. 149-154, 1999.

Wu, J., Global and Local Coupling Analysis for Small Components in Drop Simulation, 6th International LSDYNA Users Conference, pp. 11:17 - 11:26, 2000.

Wu, J., Song, G., Yeh, C-P., Wyatt, K., Drop/Impact Simulation and Test Validation of Telecommunication Products, Intersociety Conference on Thermal Phenomena, pp. 330- 336, 1998.

Xie, D., Arra, M., Yi, S., Rooney, D., Solder Joint Behavior of Area Array Packages in Board-Level Drop for Handheld Devices, 53rd Electronic Components and Technology Conference, pp. 130 – 135, 2003.

Xie, D., Arra, M., Shangkai, D., Phan, H., Geiger, D., Yi, S., Life Prediction of Lead free Solder Joints for Handheld Products, Telecom Hardware Solutions Conference, Plano, Texas, May 15-16, 2002.

Xu, L., Pang, H., Combined Thermal and Electromigration Exposure Effect on SnAgCu BGA Solder Joint Reliability, Electronic Components and Technology Conference, pp. 1154-1159, May 2006. Yang, W., Messle, R., "Microstructure evolution of eutectic Sn-Ag solder joints", Journal of Electronic Materr., Vol. 23, No. 8, pp. 767-772, 1994.

Yeh, C., Lai, Y., Transient Analysis of Board-level Drop Response of Lead-free Chipscale Packages with Experimental Verifications, Electronic Components and Technology Conference, pp. 695-700, June, 2004.

Yogel, D., Grosser, V., Schubert, A., Michel, B., MicroDAC Strain Measurement for Electronics Packaging Structures, Optics and Lasers in Engineering, Vol. 36, pp. 195-211, 2001.

Zhao, J., Liu, F., Zhou, X., Zhou, H., Jing, J., Zhao, M., Improvement of JEDEC Drop Test in SJR Qualification through Alternative Test Board Design, Electronic Components and Technology Conference, pp. 946-950, 2007.

Zhang, Y., Cai, Z., Suhling, J., Lall, P., Bozack, M., “The Effect of Aging Temperature on SAC Solder Joint Material Behavior and Reliability”, Electronic Component and Technology Conference, pp99-112, 2008.

Zhang, F., Li, M., Xiong, C., Fang, F., Yi, S., Thermal Deformation Analysis of BGA Package by Digital Image Correlation Technique, Microelectronics International, Vol. 22, No. 1, pp. 34-42, 2005.

Zhang, Y., Shi, X., Zhou, W., Effect of Hygrothermal Aging on Interfacial Reliability of Flip Chip on Board (FCOB) Assembly, Electronic Packaging Technology Conference, pp. 404-409, 2004.

Zhou, P., Goodson, K. E., Sub-pixel Displacement and Deformation Gradient Measurement Using Digital Image- Speckle Correlation (DISC), Optical Engineering, Vol. 40, No. 8, pp 1613-1620, August 2001.

Zhu, W. H., Xu, L., Pang, J., Zhang, X., Poh, E., Sun, Y., Sun, A., Wang, C. K., Tan, H.B., Drop Reliability Study of PBGA Assemblies with SAC305, SAC105 and SAC105-Ni Solder Ball on Cu-OSP and ENIG Surface Finish, Proceedings of the 58th ECTC, Orlando, Florida, pp.1667-1672, May27th-May30th, 2008.

Zhu, L., Marccinkiewicz, W., Drop Impact Reliablity Analysis of CSP Packages at Board and Product System Levels Through Modeling Approaches, Proceedings of the ITherm Conference, pp. 296 – 303, 2004.

Zhu, L., Modeling Technique for Reliability Assessment of Portable Electronic Product Subjected to Drop Impact Loads, Proceedings of the 53rd ECTC, pp. 100-104, 2003.

Zhu, L., Submodeling Technique for BGA Reliability Analysis of CSP Packaging Subjected to an Impact Loading,” InterPACK Conference Proceedings, 2001.

APPENDIX

LIST OF SYMBOLS

Symbol	Description
$I_1(r)$	Reference image
$I_2(r)$	Deformed Image
r	Reference Pixel
$U(r)$	Displacement Vector
$C_A(r')$	Current Absolute Correlation Function
$C_L(r')$	Current Least-square Correlation Function
$C_C(r')$	Current Cross correlation Function
∇	Gradient
G	Acceleration due to gravity
M	Mass Matrix
C	Damping Matrix
T	Period
R	Externally Applied Load Vector
F	Force

n	Time Step
Δ	Increment
ω	Angular Frequency
l	Length
ρ	Density
E	Elastic Modulus
K	Stiffness Matrix
Cn	Courant Number
Δt_{cr}	Critical Time Increment
D	Displacement Vector
$\dot{D}$	Velocity Vector
$\ddot{D}$	Acceleration Vector
υ_c	Poisson’s ratio of smeared element
υ_k	Poisson’s ratio of individual element
h_k	Layer thickness of individual components
E_c	Elastic Modulus of smeared element
E_k	Elastic modulus of individual components

v_k	Volume of individual component
V	impact velocity
H	drop height
T	Nominal Traction
α	ratio of shear stiffness of interface to the normal stiffness of interface
S	cohesive zone area for cohesive elements
D (*Section 5.5*)	Scalar damage variable
t^0	Peak value of nominal stress
A	Fatigue Constant
n (Chapter 7)	Fatigue constant
D (Chapter 7)	Damage Index